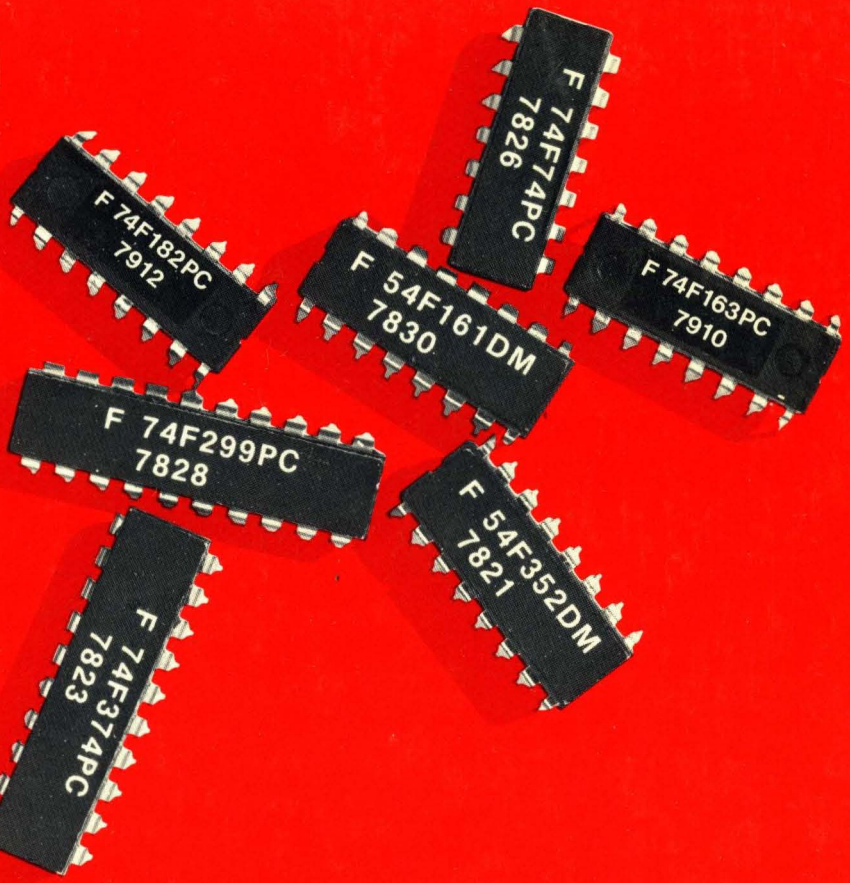
FAST

Fairchild Advanced Schottky TTL



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54F/74F FAMILY DC CHARACTERISTICS[1]

SYMBOL	PARAMETER		LIMITS[2] Min	LIMITS[2] Typ[3]	LIMITS[2] Max	UNITS	V_{CC}[4]	CONDITIONS[2]
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	Std 6 Mil.	2.5	3.4		V	Min	I_{OH} = 40 μA Multiplied by Output HIGH U.L. Shown on Data Sheet
		Std 6 Com.	2.7	3.4				
V_{OL}	Output LOW Voltage			0.35	0.5	V	Min	I_{OL} = 1.6 mA Multiplied by Output LOW U.L. Shown on Data Sheet
I_{IH}	Input HIGH Current	0.5 U.L.			20	μA	Max	I_{IH} = 40 μA Multiplied by Input HIGH U.L. Shown on Data Sheet; V_{IN} = 2.7 V
		1.0 U.L.			40			
		n U.L.			n(40)			
	Input HIGH Current, Breakdown Test, All Inputs				100	μA	Max	V_{IN} = 7.0 V
I_{IL}	Input LOW Current	0.375 U.L.			-0.6	mA	Max	I_{IL} = -1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet; V_{IN} = 0.5 V
		0.75 U.L.			-1.2			
		n U.L.			n(-1.6)			
I_{OZH}	3-State Output OFF Current HIGH				50	μA	Max	V_{OUT} = 2.4 V
I_{OZL}	3-State Output OFF Current LOW				-50	μA	Max	V_{OUT} = 0.5 V
I_{OS}[5]	Output Short-Circuit Current	Standard[6]/ 3-State	-60[7]		-150	mA	Max	V_{OUT} = 0 V
		Buffers/ Line Dvrs	-100		-225			

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to T_A = +25°C and V_{CC} = +5.0 V.
4. Min and Max refer to the values listed in the table of recommended operating conditions.
5. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
6. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.
7. Some of the circuits manufactured in 1979 may exhibit I_{OS} values slightly less than 60 mA.

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Fairchild Advanced Schottky TTL

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Introduction

This is an introductory brochure for Fairchild Advanced Schottky TTL, FAST, a family of TTL circuits that exhibits a combination of performance and efficiency unapproached by any other TTL family. Made with the proven Isoplanar process, 54F/74F circuits offer the switching speed and output drive capability of Schottky TTL, with superior noise margins and only one-fourth the power consumption.

Section 1 Product Index
Lists 54F/74F circuits currently planned; more circuits will be added as market needs are identified.

Section 2 Family Characteristics
Discusses FAST circuit characteristics and noise margins and contains family ratings, dc specifications and ac waveforms.

Section 3 Circuit Selection Guides
Contains pinouts, features and functional descriptions; circuits are grouped functionally rather than numerically.

Section 4 Data Sheets
Contains data sheets for currently available and pending new products.

Section 5 Ordering Information and Package Outlines
The simplified purchasing code which identifies not only the device type, but also the package type and temperature range, is explained. Detailed physical dimension drawings for each package are given.

Section 6 Field Sales Offices, Representatives and Distributor Locations

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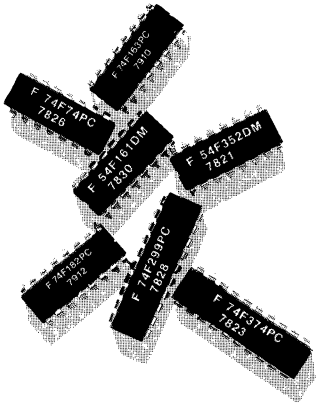
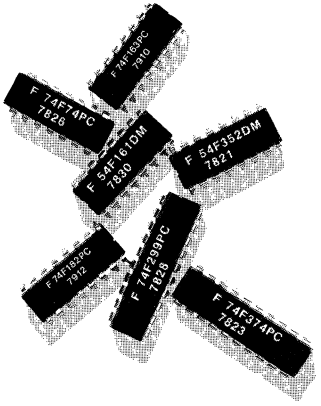
*Also shown on inside cover



Section 1 Product Index



Section 2 Circuit Characteristics

FAST Technology

FAST is an acronym for Fairchild Advanced Schottky TTL. FAST circuits are made with the advanced Isoplanar II process, which produces transistors with very high, well-controlled switching speeds, extremely small parasitic capacitances and f_T in excess of 5 GHz. Isoplanar is an established Fairchild process, used for years in the manufacture of bipolar memories, CMOS, subnanosecond ECL and I^3L™ (Isoplanar Intergrated Injection Logic) LSI devices.

In the Isoplanar process, components are isolated by a selectively grown thick oxide rather than the P^+ isolation region used in the Planar process. Since this oxide needs no separation from the base-collector regions, component and chip sizes are substantially reduced. The base and emitter ends terminate in the oxide wall; masks can thus overlap the device area into the isolation oxide. This overlap feature eliminates the extremely close tolerances normally required for base and emitter masking, and the standard photolithographic processes can be used.

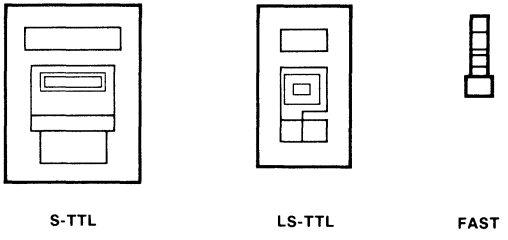


Fig. 2-1 Relative Transistor Size in Various TTL Families

Figure 2-1 shows the relative size of phase-splitter transistors (Q2 in *Figure 2-3*) used in Schottky, Low Power Schottky and FAST circuits. The LS-TTL transistor is smaller than that of S-TTL because of process refinements, shallower diffusions and smaller operating currents. The relative size of the FAST transistor illustrates the remarkable reduction afforded by the Isoplanar process. This in turn reduces junction capacitances, while the oxide isolation reduces side-wall capacitance. The effect of these reductions is an increase in frequency response by a factor of three or more. *Figure 2-2* shows the frequency response of two sizes of transistors made with the Isoplanar II process. Because they have modest, well-defined loads and thus can use smaller, faster transistors, internal gates of MSI devices are faster than SSI gates such as the 74F00 or 74F02. SSI gates, on the other hand, are designed to have high output drive capability and thus use larger transistors.

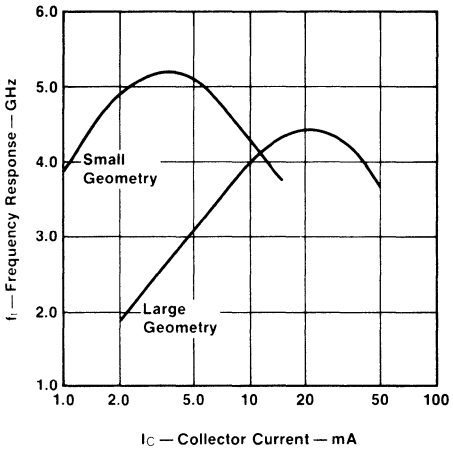


Fig. 2-2 Isoplanar Transistor Frequency Response

FAST Circuitry

The 2-input NAND gate, shown in *Figure 2-3*, has three stages of gain (Q1, Q2, Q3) instead of two stages as in other TTL families. This raises the input threshold voltage and increases the output drive. The higher threshold makes it possible to use pn diodes for the input AND function (D1 and D2) and still achieve an input threshold of 1.5 V. The capacitance of these diodes is comparatively low, which results in improved ac noise immunity. The effect of the threshold adjustment can be seen in the voltage transfer characteristics of *Figures 2-4, 2-5* and *2-6*. At 25°C (*Figure 2-5*) the FAST circuit threshold is nearly centered between the 0.8 V and 2.0 V limits specified for TTL circuits. This gives a better balance between the HIGH- and LOW-state noise margins. The +125°C characteristics (*Figure 2-6*) show that the FAST circuit threshold is comfortably above the 0.8 V specification, more so than in S-TTL or LS-TTL circuits. At -55°C, the FAST circuit threshold is still well below the 2.0 V specification, as shown in *Figure 2-4*.

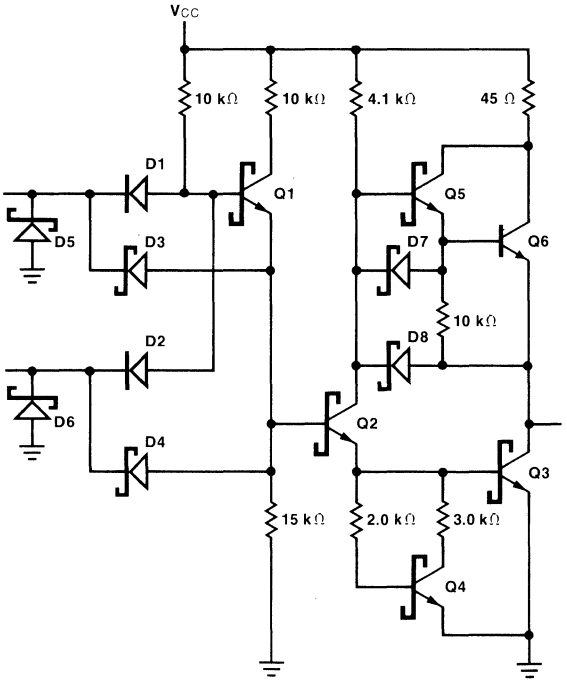


Fig. 2-3 Basic FAST Gate Schematic

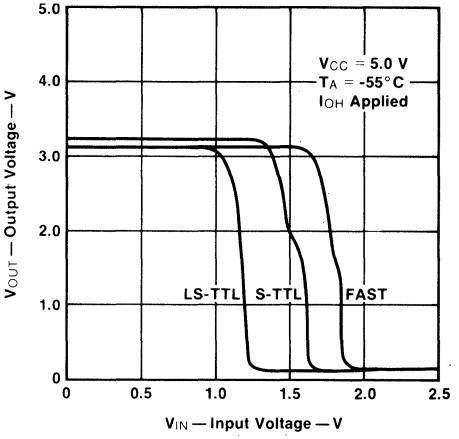


Fig. 2-4 Transfer Functions at Low Temperature

FAST circuits contain several speed-up diodes to help discharge internal capacitances. Referring again to *Figure 2-3*, when a HIGH-to-LOW transition occurs at the D1 input, for example, Schottky diode D3 acts as a low-resistance path to discharge the several parasitic capacitances connected to the base of Q2. This effect only comes into play, however, as the input signal falls below about 1.2 V; D3 does not act as an entry path for negative spikes superimposed on a HIGH input level. When Q2 turns on and its collector voltage falls, D7 provides a discharge path for capacitance at the base of Q6. Whereas D3, D4 and D7 enhance switching speed by helping to discharge internal nodes, D8 contributes to the ability of a FAST circuit to rapidly discharge load capacitance. Part of the charge stored in load capacitance passes through D8 and Q2 to increase the base current of Q3 and increase Q3's current sinking capability during the HIGH-to-LOW output voltage transition.

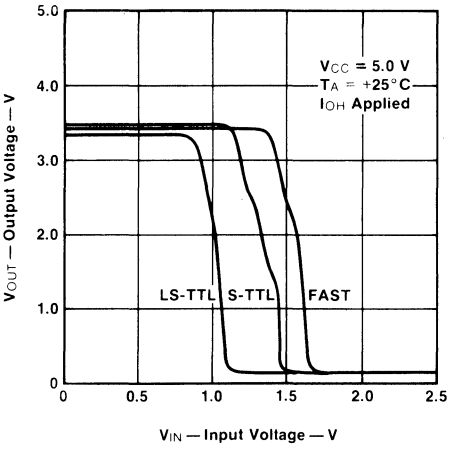


Fig. 2-5 Transfer Functions at Room Temperature

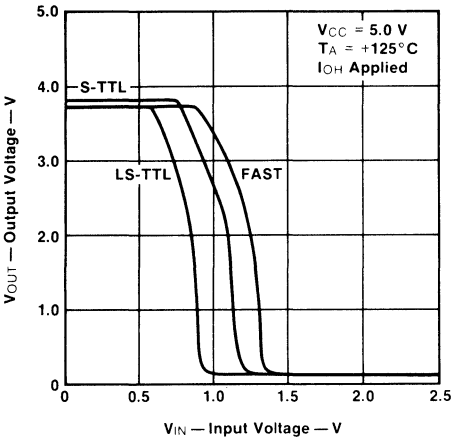


Fig. 2-6 Transfer Functions at High Temperature

The Schottky clamping diodes built into the transistors prevent saturation, thereby eliminating storage time as a factor in switching speed. Similarily, the speed-up diodes tend to minimize the impact of other variables on switching speed. The overall effect is to minimize variation in switching speed of FAST circuits with variations in supply voltage and ambient temperature (*Figures 2-8* through *2-11*). Propagation delay is specified not only under nominal supply voltage and temperature conditions, but also over the recommended operating range of V_{CC} and T_A for both military and commercial grade devices.

The internal switching speed of a logic circuit is only one aspect of the circuit's suitability for high-speed operation at the system or subsystem level; the other aspect is the ability of the circuit to drive load capacitance. FAST circuit outputs are structured to sink at least 20 mA in the LOW state, the same as S-TTL. This capability plus the effect of the aforementioned feedback through D8 assures that the circuit can rapidly discharge capacitance. During a LOW-to-HIGH transition, the pull-up current is limited by the 45 Ω resistor, versus 55 Ω for S-TTL.

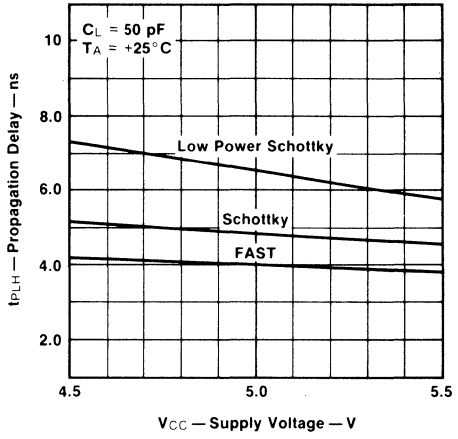


Fig. 2-8 Propagation Delay t_{PLH} vs V_{CC}

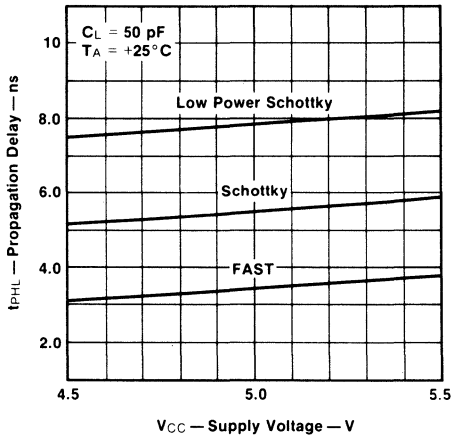


Fig. 2-9 Propagation Delay t_{PHL} vs V_{CC}

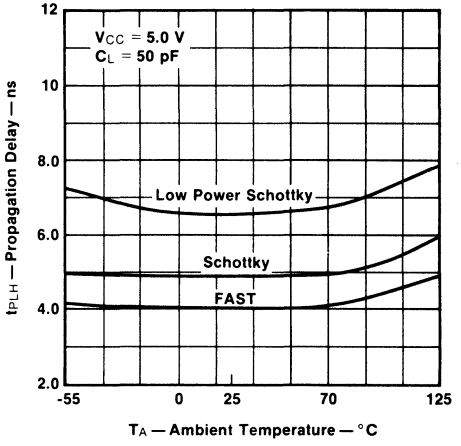


Fig. 2-10 Propagation Delay t_{PLH} vs Temperature

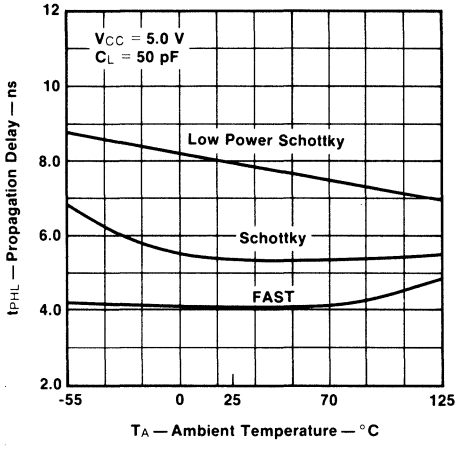


Fig. 2-11 Propagation Delay t_{PHL} vs Temperature

Therefore, FAST circuits are inherently more capable than S-TTL of charging load capacitance. *Figures 2-12* and *2-13* indicate the effect of load capacitance on propagation delays and transition times of FAST circuits. *Figure 2-14* shows the typical output LOW voltage V_{OL} as a function of load current. The typical I-V characteristic in the quiescent HIGH state is shown in *Figure 2-15*. In the lower left, the intercept along the vertical axis indicates the short-circuit output current I_{OS}. From this point to approximately -10 mA, the slope is about 50 Ω, indicating that the totem-pole pull-up is saturated and current is limited principally by the 45 Ω resistor. From -10 mA upward almost to the horizontal axis, the slope is the dynamic output resistance of transistor Q6. That part of the characteristic in the upper right shows that a bi-state output cannot be pulled up much above V_{CC} because of the sneak path through D8 and the 4.1 kΩ resistor back to V_{CC}.

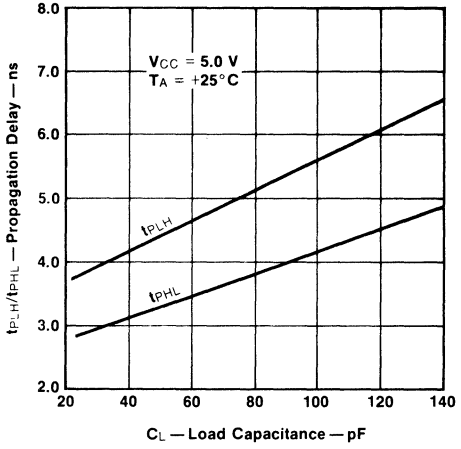


Fig. 2-12 Propagation Delay vs Load Capacitance

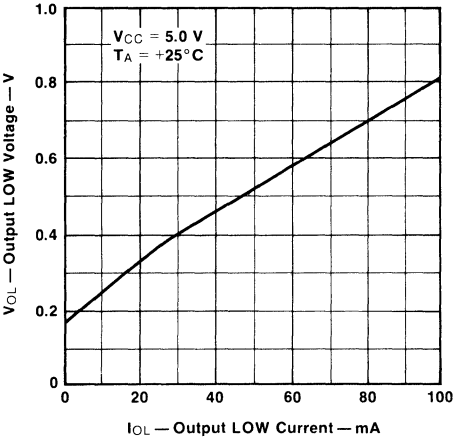


Fig. 2-14 Output LOW Characteristic

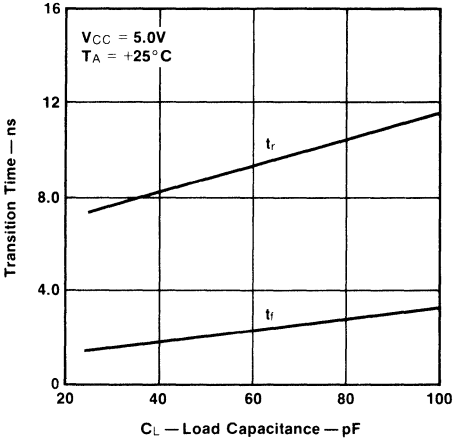


Fig. 2-13 Transition Time vs Load Capacitance

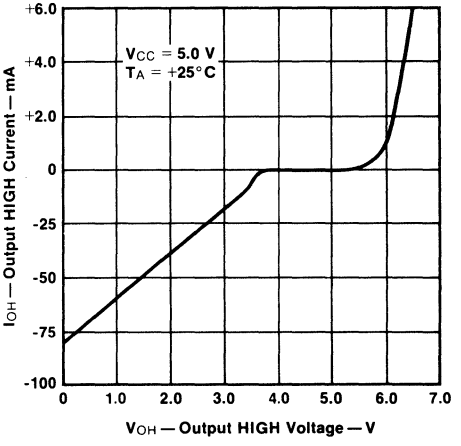
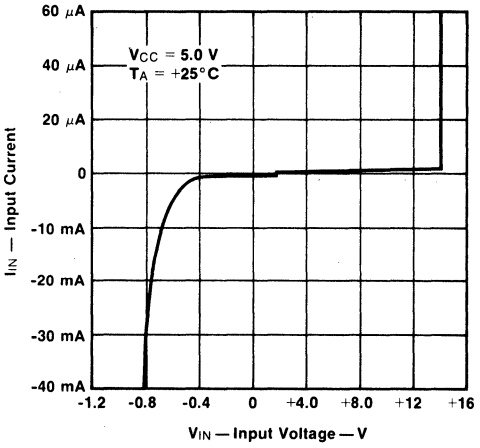


Fig. 2-15 Output HIGH Characteristic

A typical input I-V characteristic is shown in *Figure 2-16*. An input clamping diode (D5 or D6 in *Figure 2-3*) conducts if an input signal tends to go more negative than about -0.4 V. This limits the undershoot that might occur at the end of a long line following a HIGH-to-LOW transition. The clamping diodes in FAST circuits have been improved over those used in LS-TTL to prevent parasitic coupling through sneak paths to other components on the chip. For input voltage in the range of -0.4 V to about +1.5 V, the input current is governed principally by the 10 kΩ pull-up resistor of the input gate. With V_{CC} at the recommended maximum (+5.5 V or +5.25 V) and the input at +0.4 V, the specified maximum input current is 0.6 mA. This compares favorably with the 0.4 mA specified maximum for LS-TTL and is far below the 2.0 mA maximum for an S-TTL input. Thus, in a system comprised of FAST devices, there is less need for buffering to increase fan-out.



Input Characteristic

Unit Loads (U.L.)

For convenience in system design, the input loading and fan-out characteristics of each circuit are specified in terms of unit loads. One unit load in the HIGH state is defined as 40 μA; thus both the input HIGH leakage current I_{IH} and the output HIGH current-sourcing capability I_{OH} are normalized to 40 μA. The specified maximum I_{IH} for a standard FAST input is 20 uA, or 0.5 U.L., while the I_{OH} rating for a standard output is 1.0 mA, or 25 U.L. Similarly, one unit load in the LOW state is defined as 1.6 mA and both the input LOW current I_{IL} and the output LOW current-sinking capability I_{OL} are normalized to 1.6 mA. The specified maximum I_{IL} for a standard FAST input is 0.6 mA, or 0.375 U.L., while the I_{OL} rating for a standard output is 20 mA, or 12.5 U.L. On the data sheets, the input and output load factors are listed in the Input Loading/Fan-Out Table. The table from the 54F/74F04 Hex Inverter is reproduced below.

In the right-hand column the input HIGH/LOW load factors are 0.5/0.375, with the first number representing I_{IH} and the second representing I_{IL}. For testing or procurement purposes, these load factors can easily be translated to actual test limits by multiplying them by 40 μA and 1.6 mA, respectively. The second set of numbers represents the rated output HIGH/LOW load currents I_{OH} and I_{OL}, respectively. The indicated HIGH/LOW drive factors of 25/12.5 translate to 1.0 mA and 20 mA by multiplying them by 40 μA and 1.6 mA, respectively.

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

Absolute Maximum Ratings[1]
(beyond which useful life may be impaired)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V_{CC} Pin Potential to Ground Pin	-0.5 V to +7.0 V
Input Voltage[2]	-0.5 V to +7.0 V
Input Current[2]	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State:	
Standard Output	-0.5 V to V_{CC} Value
3-State Output (with V_{CC} = 0 V)	-0.5 V to +5.5 V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL}

Recommended Operating Conditions[1]

	Min	Max
Free Air Ambient Temperature		
Military (XM)	-55°C	+125°C
Commercial (XC)	0°C	+70°C
Supply Voltage		
Military (XM)	+4.5 V	+5.5 V
Commercial (XC)	+4.75 V	+5.25 V

1. Unless otherwise restricted or extended by detail specifications.
2. Either input voltage or current limit sufficient to protect inputs.

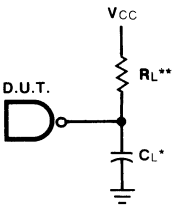
54F/74F FAMILY DC CHARACTERISTICS[1]

SYMBOL	PARAMETER		LIMITS[2] Min	Typ[3]	Max	UNITS	V_{CC}[4]	CONDITIONS[2]
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal Over Recommended V_{CC} and T_A Range
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal Over Recommended V_{CC} and T_A Range
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage	Std 6 Mil.	2.5	3.4		V	Min	I_{OH} = 40 μA Multiplied by Output HIGH U.L. Shown on Data Sheet
		Std 6 Com.	2.7	3.4				
V_{OL}	Output LOW Voltage			0.35	0.5	V	Min	I_{OL} = 1.6 mA Multiplied by Output LOW U.L. Shown on Data Sheet
I_{IH}	Input HIGH Current	0.5 U.L.			20	μA	Max	I_{IH} = 40 μA Multiplied by Input HIGH U.L. Shown on Data Sheet; V_{IN} = 2.7 V
		1.0 U.L.			40			
		n U.L.			n(40)			
	Input HIGH Current, Breakdown Test, All Inputs				100	μA	Max	V_{IN} = 7.0 V
I_{IL}	Input LOW Current	0.375 U.L.			-0.6	mA	Max	I_{IL} = -1.6 mA Multiplied by Input LOW U.L. Shown on Data Sheet; V_{IN} = 0.5 V
		0.75 U.L.			-1.2			
		n U.L.			n(-1.6)			
I_{OZH}	3-State Output OFF Current HIGH				50	μA	Max	V_{OUT} = 2.4 V
I_{OZL}	3-State Output OFF Current LOW				-50	μA	Max	V_{OUT} = 0.5 V
I_{OS}[5]	Output Short-Circuit Current	Standard[6]/ 3-State	-60[7]		-150	mA	Max	V_{OUT} = 0 V
		Buffers/ Line Dvrs	-100		-225			

1. Unless otherwise noted, conditions and limits apply throughout the temperature range for which the particular device type is rated. The ground pin is the reference level for all applied and resultant voltages.
2. Unless otherwise stated on individual data sheets.
3. Typical characteristics refer to T_A = +25°C and V_{CC} = +5.0 V.
4. Min and Max refer to the values listed in the table of recommended operating conditions.
5. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
6. Standard refers to the totem-pole pull-up circuitry commonly used for the particular family, as distinguished from buffers, line drivers or 3-state outputs.
7. Some of the circuits manufactured in 1979 may exhibit I_{OS} values slightly less than 60 mA.

AC Loading and Waveforms

Figure 2-17 shows the load circuit configuration used for ac testing of bi-state outputs. The appropriate value of C_L is shown on each individual data sheet in the ac table column headings. A pulse generator signal swing of 0 V to +3.0 V, terminated at the test socket, is recommended for ac testing. A 1.0 MHz square wave is recommended for most propagation delay tests, with rise and fall times of 2.5 ns. The generator pulse repetition rate must necessarily be increased for testing f_{max}. Two pulse generators are usually required for testing such parameters as set-up time, hold time, recovery time, etc. Low inductance type load capacitors are recommended for best correlation with factory test results.



*Includes Jig and Probe Capacitance
**Used only for open collector outputs

Fig. 2-17 Test Load for Bi-State Mode

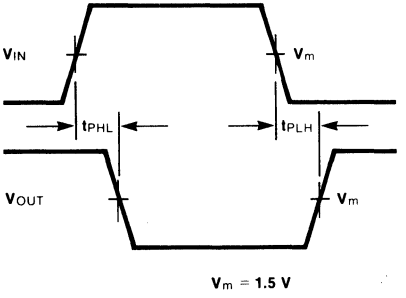


Fig. 2-18 Waveform for Inverting Functions

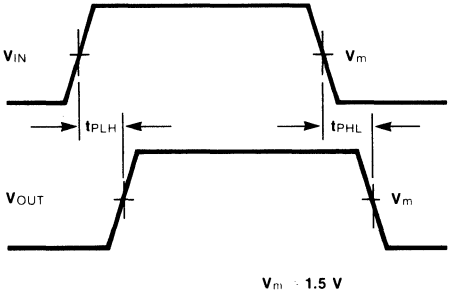


Fig. 2-19 Waveform for Non-Inverting Functions

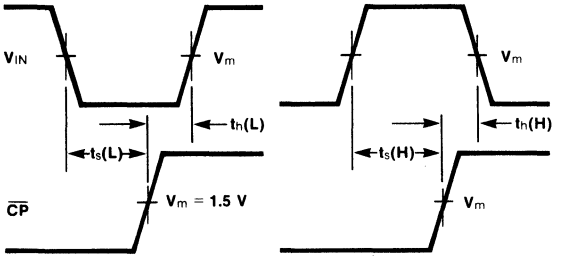


Fig. 2-20 Set-up and Hold Times, Rising-Edge Clock

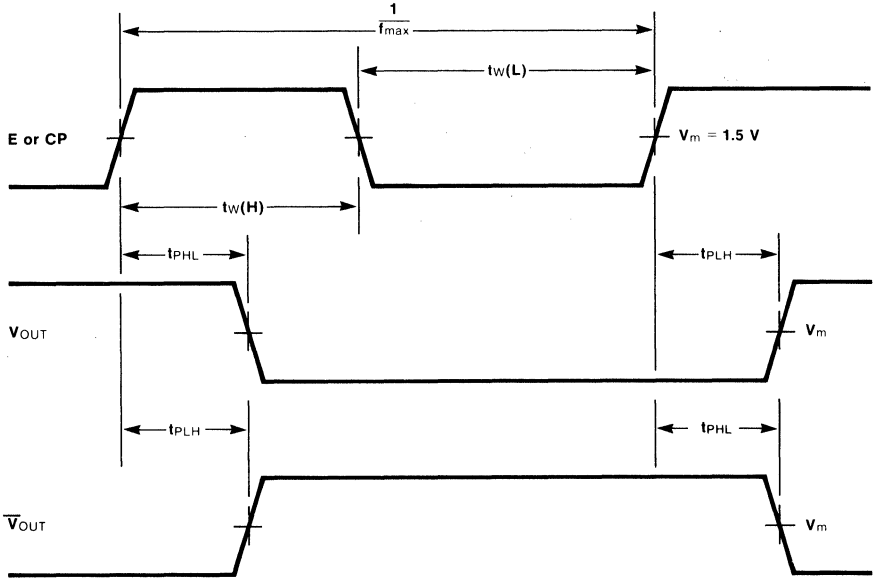


Fig. 2-21 Propagation Delays from Rising-Edge Clock or Enable

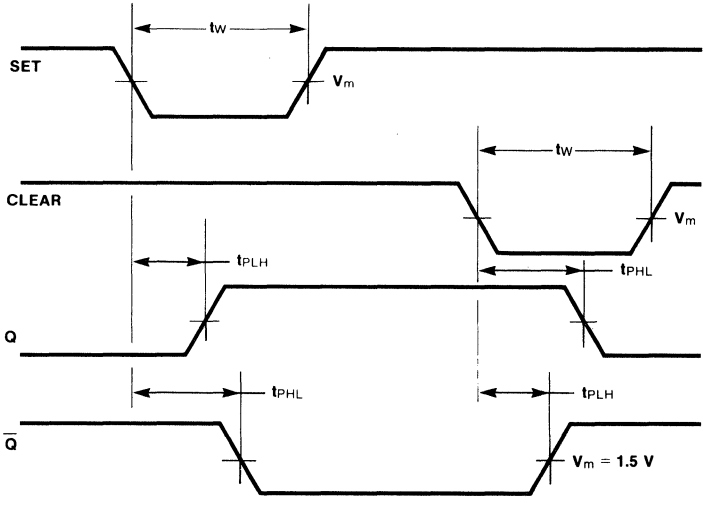


Fig. 2-22 Propagation Delays from Set and Clear (or Reset)

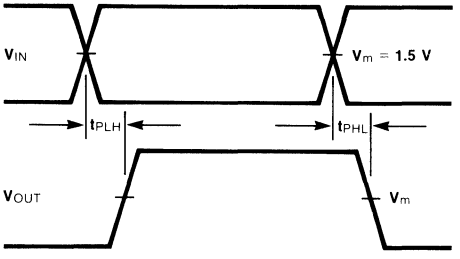


Fig. 2-23 Whether Response is Inverting or Non-Inverting Depends on Specific Truth Table Conditions

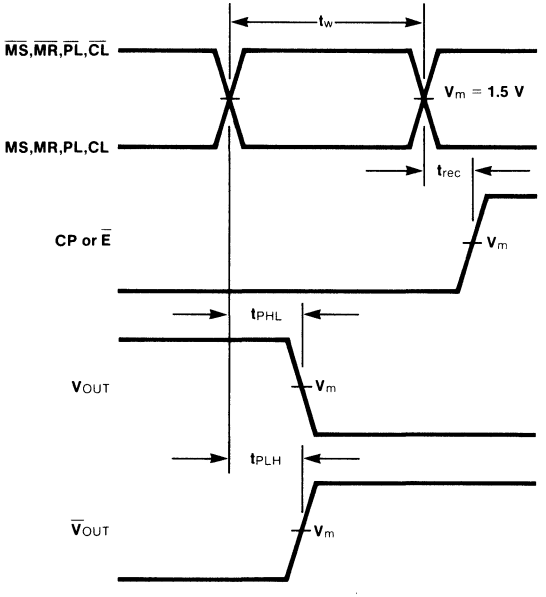
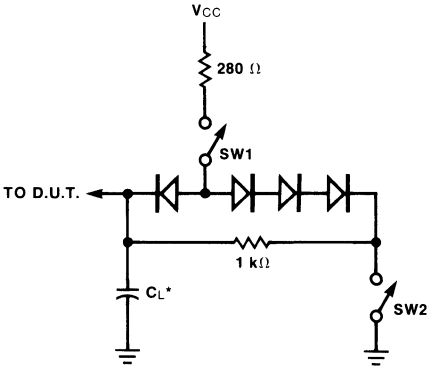


Fig. 2-24 Asynchronous Set, Reset, Parallel Load or Clear, Active Rising-Edge Clock or Active-LOW Enable



*Includes Jig and Probe Capacitance

PARAMETER	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 2-25 Enable and Disable Test Loads for 3-State Outputs

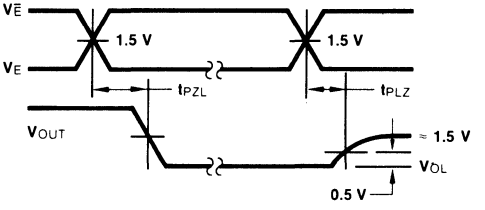


Fig. 2-26 3-State Output LOW Enable and Disable Times

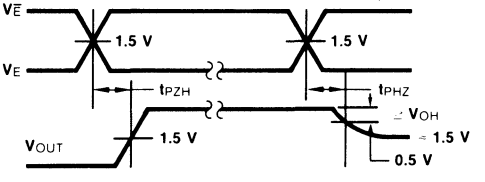


Fig. 2-27 3-State Output HIGH Enable and Disable Times

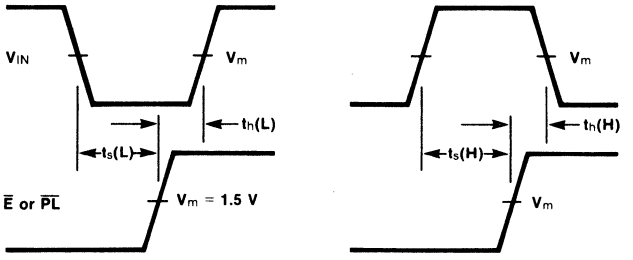


Fig. 2-28 Setup and Hold Times to Active-LOW Enable or Parallel Load

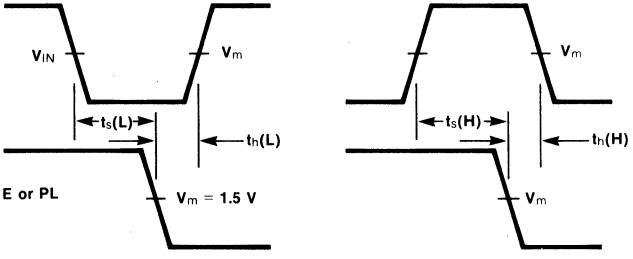


Fig. 2-29 Setup and Hold Times to Active-HIGH Enable or Parallel Load

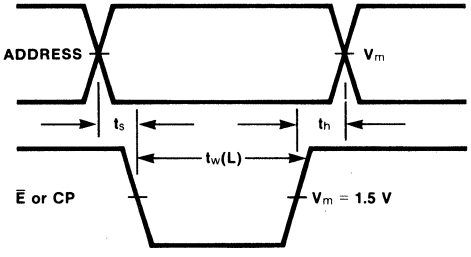
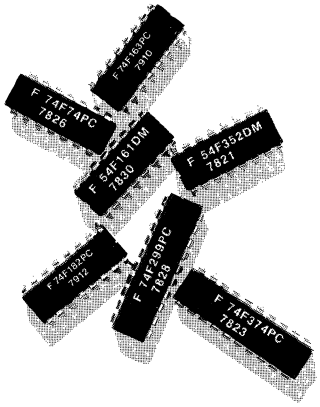
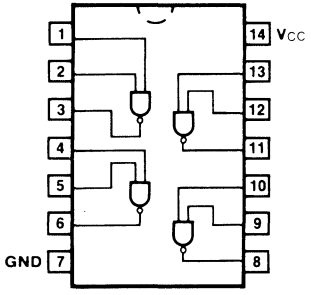


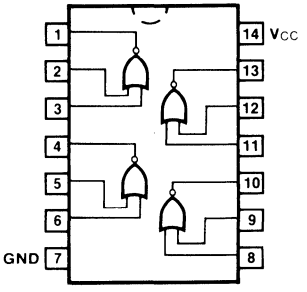
Fig. 2-30 Storage Address Setup and Hold Times



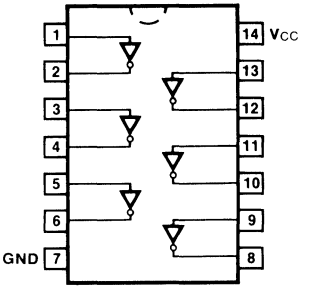
54F/74F00
Quad 2-Input NAND Gate



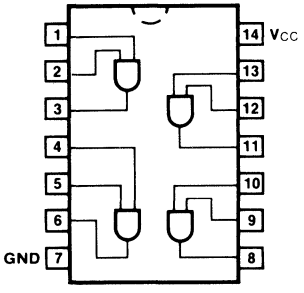
54F/74F02
Quad 2-Input NOR Gate



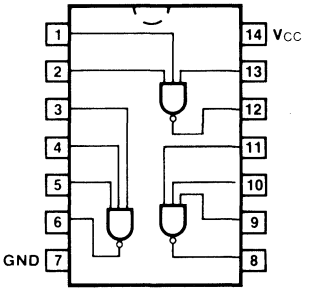
54F/74F04
Hex Inverter



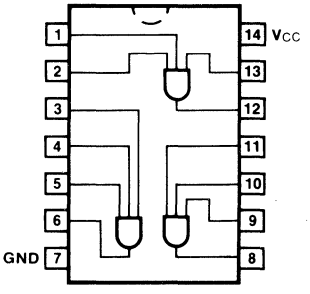
54F/74F08
Quad 2-Input AND Gate



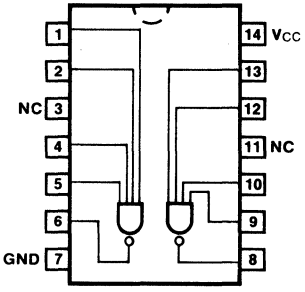
54F/74F10
Triple 3-Input NAND Gate



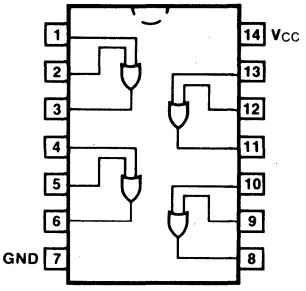
54F/74F11
Triple 3-Input AND Gate



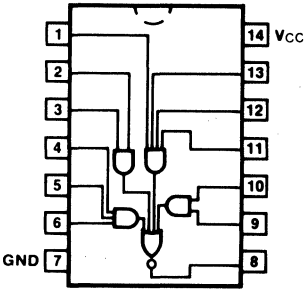
54F/74F20
Dual 4-Input NAND Gate



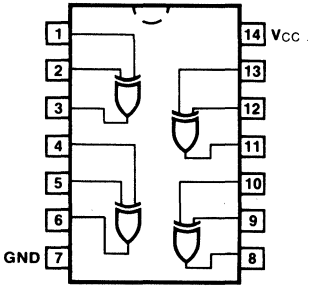
54F/74F32
Quad 2-Input OR Gate



54F/74F64
AND OR-Invert Gate



54F/74F86
Quad Ex-OR Gate



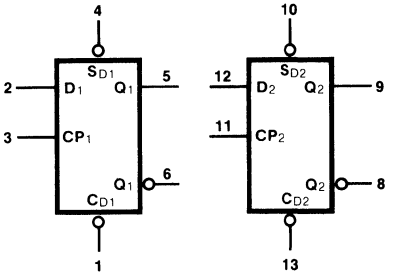
Dual D-Type Positive Edge-Triggered Flip-Flop

54F/74F74

Description — The 'F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. The D input can change when the clock is in either state without affecting the flip-flop, provided that the D signal is in the desired state during the recommended setup and hold times relative to the rising edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{C}_D$ and $\overline{S}_D$ force both Q and $\overline{Q}$ HIGH.

Buffered Outputs
Fully Edge-Triggered
Overriding Direct Set and Clear
Clock Frequency 125 MHz TYP
Propagation Delay 5.2 ns TYP
Supply Current 10.5 mA Typ

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

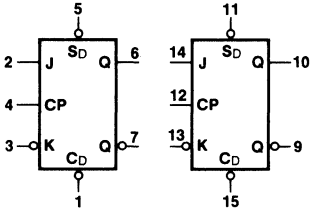
Dual J$\overline{K}$ Positive Edge-Triggered Flip-Flop

54F/74F109

Description — The 'F109 contains two independent, high speed J$\overline{K}$ flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the rising edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and $\overline{K}$ inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the rising edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH. A D input is available by tying J and $\overline{K}$ together.

Buffered Outputs
Fully Edge-Triggered
Overriding Direct Set and Clear
Clock Frequency 125 MHz TYP
Propagation Delay 5.2 ns TYP
Supply Current 11.7 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

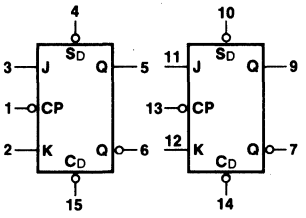
Dual JK Negative Edge-Triggered Flip-Flop

54F/74F112

Description — The 'F112 contains two independent, high speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S}_D$ or $\overline{C}_D$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S}_D$ and $\overline{C}_D$ force both Q and $\overline{Q}$ HIGH.

Buffered Outputs
Fully Edge-Triggered
Overriding Direct Set and Clear
Clock Frequency 125 MHz Typ
Propagation Delay 5.2 ns Typ
Supply Current 11.7 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

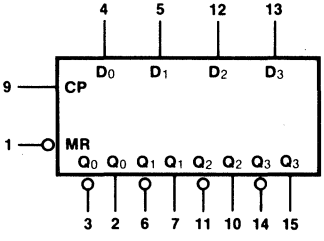
Quad D Flip-Flop

54F/74F175

Description — The 'F175 contains four high speed, edge-triggered D flip-flops with common Clock and Master Reset inputs, and individual D inputs and Q and $\overline{Q}$ outputs. Information on the D inputs is entered by the rising edge of the clock, provided that the recommended setup and hold times are observed. A LOW signal on $\overline{MR}$ forces all Q outputs LOW and $\overline{Q}$ outputs HIGH, independent of Clock or Data inputs.

True and Complement Outputs
Fully Edge-Triggered
Asynchronous Common Reset
Clock Frequency 150 MHz Typ
Propagation Delay 6.3 ns Typ
Supply Current 21 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Octal D-Type Flip-Flop

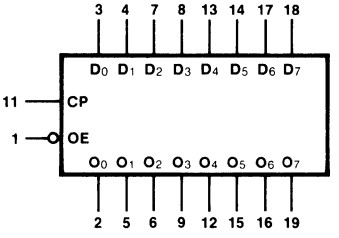
(With 3-State Outputs)

54F/74F374

Description — The 'F374 contains eight edge-triggered flip-flops with buffered 3-state outputs for bus oriented applications. Information on the D inputs is entered on the rising edge of the common Clock input, provided that the recommended setup and hold times are observed. A HIGH signal on the common Output Enable forces the outputs to the high impedance state but does not affect the state of the flip-flops or subsequent data entry.

Buffered 3-State Outputs
D-Type Inputs
Fully Edge-Triggered
Clock Frequency 110 MHz Typ
Propagation Delay 5.5 ns Typ
Supply Current 55 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

Quad Parallel Register

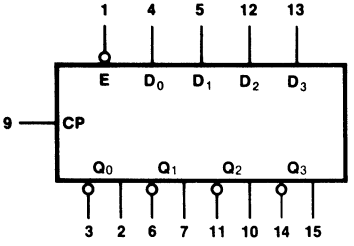
(With Enable)

54F/74F379

Description — The 'F379 storage register contains four edge-triggered flip-flops with individual D inputs and Q and $\overline{Q}$ outputs and with common Clock and input Enable inputs. Information present on the D inputs is entered on the rising edge of the clock, provided that $\overline{E}$ is LOW and the recommended setup and hold times are observed. When the $\overline{E}$ input is HIGH, the register retains the present data independent of the clock and D inputs.

Buffered Input Enable
Buffered Common Clock
Fully Edge-Triggered
Clock Frequency 150 MHz Typ
Propagation Delay 6.3 ns Typ
Supply Current 27 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Octal D-Type Flip-Flop

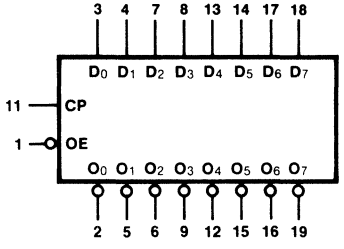
(With 3-State Outputs)

54F/74F534

Description — The 'F534 contains eight edge-triggered flip-flops with individual D inputs and $\overline{Q}$ outputs, and with common Clock and 3-state Output Enable inputs. Information on the D inputs is entered on the rising edge of the clock, provided that the recommended setup and hold times are observed. A HIGH signal on $\overline{OE}$ forces the outputs to the high impedance state but does not affect the state of the flip-flops or subsequent data entry. The 'F534 is the same as the 'F374 but with inverted outputs.

Inverted 3-State Outputs
D-Type Inputs
Fully Edge-Triggered
Clock Frequency 110 MHz Typ
Propagation Delay 5.5 ns Typ
Supply Current 52 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

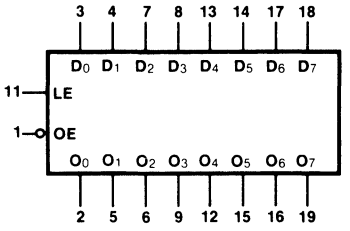
Octal Transparent Latch **54F/74F373**

(With 3-State Outputs)

Description — The 'F373 contains eight D-type latches with 3-state outputs for bus organized applications. When the common Latch Enable input is HIGH the latches are transparent, i.e. an output will change state each time its D input changes. When LE is LOW, the data that meets the recommended setup and hold times is latched. A HIGH signal on the common Output Enable input forces the outputs to the high impedance state but does not affect the state of the latches or subsequent data entry.

Buffered 3-State Outputs
D-Type Inputs
Transparent Latches
Propagation Delay 4.3 ns Typ
Supply Current 35 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

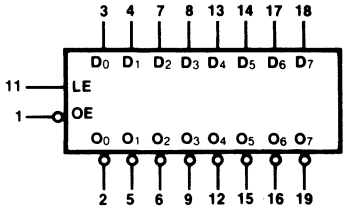
Octal Transparent Latch **54F/74F533**

(With 3-State Outputs)

Description — The 'F533 contains eight D-type latches with inverted 3-state outputs for bus organized applications. When the common Latch Enable input is HIGH the latches are transparent, i.e. an output will change state each time its D input changes. When LE is LOW, the data that meets the recommended setup and hold times is latched. A HIGH signal on the common Output Enable input forces the outputs to the high impedance state but does not affect the state of the latches or subsequent data entry. The 'F533 is the same as the 'F373 except that the outputs are inverted.

Inverted 3-State Outputs
D-Type Inputs
Transparent Latches
Propagation Delay 5.3 ns Typ
Supply Current 35 mA Typ

Logic Symbol



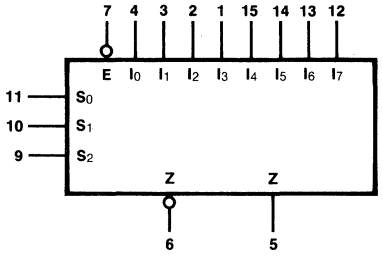
V_{CC} = Pin 20
GND = Pin 10

8-Input Multiplexer 54F/74F151

Description — The 'F151 is a high speed 8-input digital multiplexer with complementary outputs. It can select one line of data from up to eight sources. Signals on the Select inputs $S_0 - S_2$ determine which of the inputs is routed to the output. A LOW signal on the Enable input $\overline{E}$ allows the Z output to follow the selected input. A HIGH on $\overline{E}$ forces the Z output LOW and $\overline{Z}$ HIGH.

Complementary Outputs
Data to Output Delay 2.9 and 4.7 ns Typ
Select to Output Delay 6.3 and 8.1 ns Typ
Supply Current 11 mA Typ

Logic Symbol



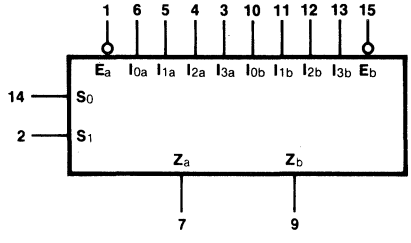
V_{CC} = Pin 16
GND = Pin 8

Dual 4-Input Multiplexer 54F/74F153

Description — The 'F153 contains two 4-input multiplexers with common Select inputs and separate Enable inputs. Signals applied to the Select inputs determine, within each section, which of the four data inputs is routed to the output. A LOW signal on an Enable input allows the output to follow the selected input. A HIGH signal on an Enable forces the output LOW.

Separate Enable Inputs
Common Select Inputs
Data to Output Delay 5.0 ns Typ
Select to Output Delay 9.5 ns Typ
Supply Current 12 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

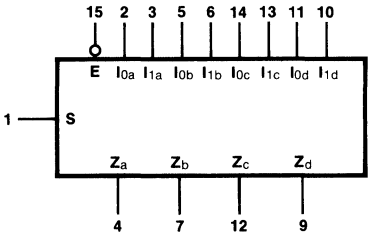
Quad 2-Input Multiplexer

54F/74F157

Description — The 'F157 contains four 2-input multiplexers with common Select and Enable inputs. It can select four bits of data from either of two sources. A LOW signal on the Enable input allows the selected data to be routed to the output. A HIGH signal on the Enable forces the outputs LOW.

Common Select Input
Common Enable Input
Data to Output Delay 4.5 ns Typ
Select to Output Delay 8.5 ns Typ
Supply Current 14 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

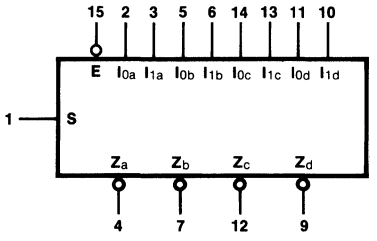
Quad 2-Input Multiplexer

54F/74F158

Description — The 'F158 contains four 2-input multiplexers with common Select and Enable inputs and with inverting outputs. It selects four bits of data from either of two sources. A LOW signal on the Enable input allows the selected data to be routed to the outputs. A HIGH signal on the Enable forces the outputs HIGH.

Inverting Outputs
Common Select Input
Common Enable Input
Data to Output Delay 2.9 ns Typ
Select to Output Delay 6.3 ns Typ
Supply Current 10 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

8-Input Multiplexer

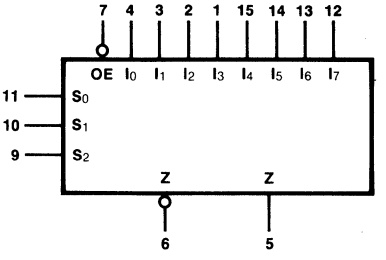
(With 3-State Outputs)

54F/74F251

Description — The 'F251 is a high speed 8-input multiplexer with complementary 3-state outputs. It provides the capability of selecting one line of data from up to eight sources, as determined by signals applied to the Select inputs $\overline{S_0}$ — S_2. A LOW signal on the Output Enable input $\overline{OE}$ allows the Z output to follow the selected input. A HIGH signal on $\overline{OE}$ forces both outputs to the high impedance state.

Complementary 3-State Outputs
Data to Output Delay 2.9 and 4.7 ns Typ
Select to Output Delay 6.3 and 8.1 ns Typ
Supply Current 10.5 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Dual 4-Input Multiplexer

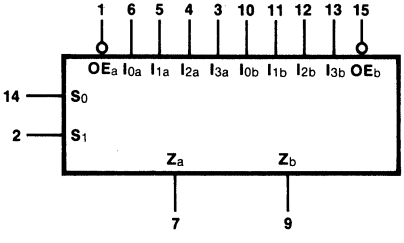
(With 3-State Outputs)

54F/74F253

Description — The 'F253 contains two 4-input multiplexers with common Select inputs, separate Output Enable ($\overline{OE}$) and 3-state outputs. Signals applied to the Select inputs determine, in each section, which of the four data inputs is routed to the output. A LOW signal on $\overline{OE}$ allows the output to follow the selected input. A HIGH on $\overline{OE}$ forces the output to the high impedance state. Outputs are thus capable of interfacing directly with bus oriented systems.

3-State Outputs
Common Select Inputs
Separate Enable Inputs
Data to Output Delay 4.4 ns Typ
Select to Output Delay 9.5 ns Typ
Supply Current 18 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Quad 2-Input Multiplexer

(With 3-State Outputs)

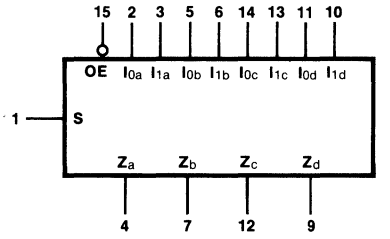
54F/74F257

3

Description — The 'F257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input; therefore, the outputs can interface directly with bus oriented systems.

3-State Outputs
Common Select Input
Common Enable Input
Data to Output Delay 4.0 ns Typ
Select to Output Delay 10 ns Typ
Supply Current 14.6 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Quad 2-Input Multiplexer

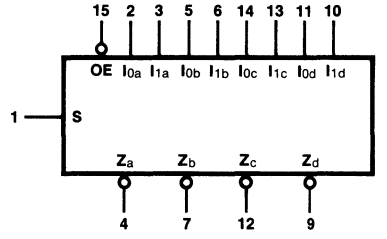
(With 3-State Outputs)

54F/74F258

Description — The 'F258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input; therefore, the outputs can interface directly with bus oriented systems. The 'F258 is the same as the 'F257 except that the outputs are inverted.

Inverting 3-State Outputs
Common Select Input
Common Enable Input
Data to Output Delay 2.9 ns Typ
Select to Output Delay 6.3 ns Typ
Supply Current 14 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

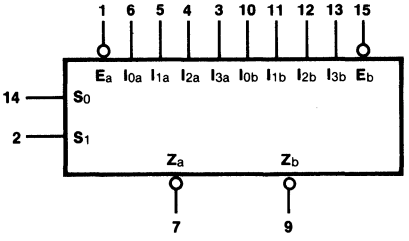
Dual 4-Input Multiplexer

54F/74F352

Description — The 'F352 contains two inverting 4-input multiplexers with common Select inputs and separate Enable inputs. Signals applied to the Select inputs determine, within each section, which of the four data inputs is routed to the output. A HIGH signal on an Enable input forces the related output HIGH. The 'F352 is the functional equivalent of the 'F153 with inverted outputs.

Inverting Outputs
Common Select Inputs
Separate Enable Inputs
Data To Output Delay 4.6 ns Typ
Select to Output Delay 6.3 ns Typ
Supply Current 8.0 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Dual 4-Input Multiplexer

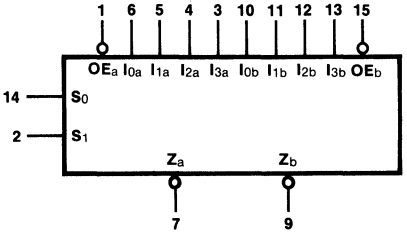
(With 3-State Outputs)

54F/74F353

Description — The 'F353 is a dual 4-input multiplexer with inverting 3-state outputs. It selects two bits of data from any four of sources using common Select inputs. An output can be switched to the high impedance state by a HIGH signal on the respective Output Enable input. Outputs are thus capable of interfacing directly with bus oriented systems. The 'F353 is the functional equivalent of the 'F253 with inverted outputs.

Inverting 3-State Outputs
Common Select Inputs
Separate Enable Inputs
Data to Output Delay 2.9 ns Typ
Select to Output Delay 6.3 ns Typ
Supply Current 13.5 mA Typ

Logic Symbol



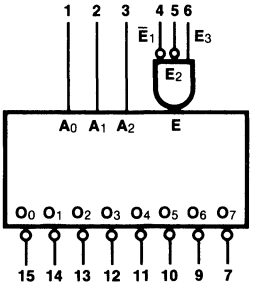
V_{CC} = Pin 16
GND = Pin 8

1-of-8 Decoder **54F/74F138**

Description — The 'F138 decoder/demultiplexer accepts three Address (A_0 — A_2) input signals and decodes them to select one of eight mutually exclusive outputs. This device is ideally suited for high speed bipolar memory chip select address decoding. Two active-LOW and one active-HIGH input enables allow parallel expansion to a 1-of-24 decoder using just three 'F138 devices, or to a 1-of-32 decoder using four 'F138 devices and one inverter.

Data Demultiplexing Capability
Multiple Enables for Expansion
Address Delay 9.0 ns Typ
Enable Delay 9.0 ns Typ
Supply Current 18 mA Typ

Logic Symbol



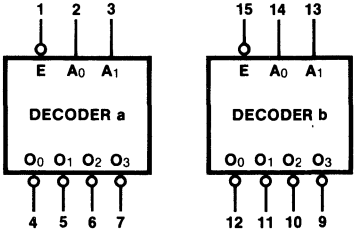
V_{CC} = Pin 16
GND = Pin 8

Dual 1-of-4 Decoder **54F/74F139**

Description — The 'F139 contains two independent 1-of-4 decoder/demultiplexers. Each accepts two Address (A_0, A_1) inputs signals and decodes them to select one of four mutually exclusive outputs. Each decoder has an active-LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the 'F139 can be used as a function generator providing all four minterms of two variables.

Two Functionally Independent Decoders
Active-LOW Mutually Exclusive Outputs
Multifunction Capability
Address Delay 9.0 ns Typ
Enable Delay 9.0 ns Typ
Supply Current 18 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

1-of-10 Decoder

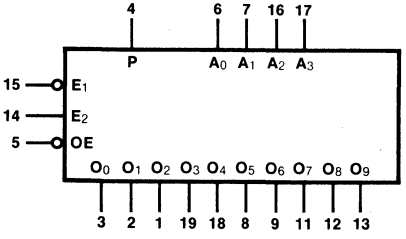
(With 3-State Outputs)

54F/74F537

Description — The 'F537 is a one-of-ten decoder/demultiplexer with four active-HIGH BCD inputs and ten mutually exclusive outputs. A polarity control input determines whether the outputs are active-LOW or active-HIGH. The 'F537 has 3-state outputs, and a HIGH signal on the Output Enable ($\overline{OE}$) input forces all outputs to the high impedance state. Two input enables, active-HIGH E_2 and active-LOW $\overline{E}_1$, are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine cause all outputs to go to the inactive state (i.e., same polarity as the P input).

Output Polarity Control
Complementary Input Enables
3-State Outputs
Ignores Input Codes Above Nine
Address Delay 12 ns Typ
Enable Delay 11 ns Typ
Supply Current 44 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

1-of-8 Decoder

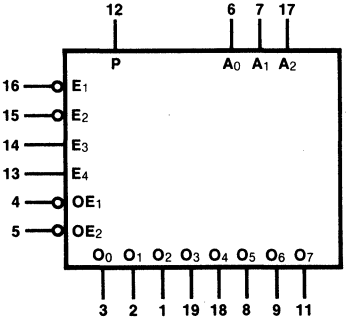
(With 3-State Outputs)

54F/74F538

Description — The 'F538 decoder/demultiplexer accepts three Address (A_0 — A_2) input signals and decodes them to select one of eight mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active-LOW or active-HIGH. A HIGH signal on either of the active-LOW Output Enable ($\overline{OE}$) inputs forces all outputs to the high impedance state. Two active-HIGH and two active-LOW input enables are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to one of eight or one of 16 destinations.

Output Polarity Control
Data Demultiplexing Capability
Multiple Enables for Expansion
3-State Outputs
Address Delay 12 ns Typ
Enable Delay 11 ns Typ
Supply Current 38 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

Dual 1-of-4 Decoder

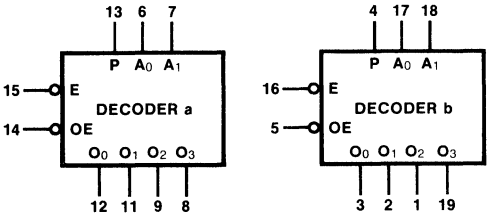
(With 3-State Outputs)

54F/74F539

Description — The 'F539 contains two independent decoders. Each accepts two Address (A_0, A_1) input signals and decodes them to select one of four mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active-HIGH (P = L) or active-LOW (P = H). An active-LOW input Enable ($\overline{E}$) is available for data demultiplexing; data is routed to the selected output in non-inverted form in the active-LOW mode or in inverted form in the active-HIGH mode. A HIGH signal on the active-LOW Output Enable ($\overline{OE}$) input forces the 3-state outputs to the high impedance state.

Two Functionally Independent Decoders
Output Polarity Control
Input Enable for Demultiplexing
3-State Outputs
Address Delay 12 ns Typ
Enable Delay 11 ns Typ
Supply Current 42 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

4-Bit Bidirectional Universal Shift Register

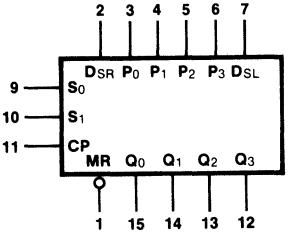
54F/74F194

Description — The 'F194 is a high speed 4-bit bidirectional shift register. Signals applied to the Select (S_0, S_1) inputs determine the mode of operation — shift left, shift right, parallel entry or hold. Except for the reset function, the 'F194 is fully synchronous and state changes are initiated by the rising edge of the clock. The flip-flops are edge-triggered and the inputs can change when the clock is in either state, provided that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on the Master Reset ($\overline{MR}$) input overrides clocked operations and forces the outputs LOW. The circuit is useful for serial-in, serial/parallel-out or parallel-in, serial/parallel-out applications.

Serial and Parallel Entry Ports
Synchronous Serial and Parallel Operation
Fully Edge-Triggered
Asynchronous Master Reset
Shift Frequency 150 MHz Typ

Propagation Delay 7.0 ns Typ
Supply Current 26 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

8-Input Universal Shift/Storage Register

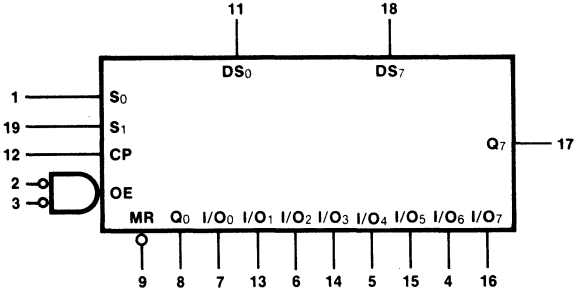
(With Common Parallel I/O Pins)

54F/74F299

Description — The 'F299 is an 8-bit register with multiplexed 3-state I/O ports for bus oriented parallel operations and with separate serial inputs and outputs for expansion. Signals applied to the Select (S_0, S_1) inputs determine the mode of operation — shift left, shift right, parallel entry or hold. State changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed, relative to the clock rising edge. An active-LOW Master Reset input overrides clocked operations and clears the register. A HIGH signal on either Output Enable ($\overline{OE}$) input forces the I/O pins to the high impedance state but does not interfere with other operations.

Multiplexed Parallel I/O Ports
Separate Serial Inputs and Outputs
Expandable Bidirectional Shifting
3-State Outputs for Bus Applications
Shift Frequency 80 MHz Typ
Propagation Delay 9.0 ns Typ
Supply Current 68 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

8-Bit Serial/Parallel Register

(With Sign Extend)

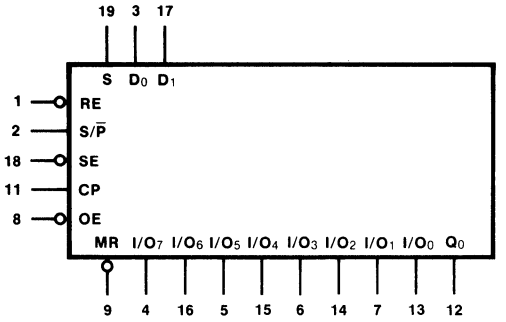
54F/74F322

3

Description — The 'F322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-state parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with signal extend, and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register. A HIGH signal on the Output Enable ($\overline{OE}$) input forces the I/O pins to the high impedance state but does not interfere with other operations. The 'F322 operates with the 'LS384 Multiplier and provides the sign extend function for twos complement arithmetic.

Multiplexed Parallel I/O Ports
Separate Serial Input and Output
Sign Extend Function
3-State Outputs for Bus Applications
Shift Frequency 80 MHz Typ
Propagation Delay 9.0 ns Typ
Supply Current 70 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

8-Bit Universal Shift/Storage Register

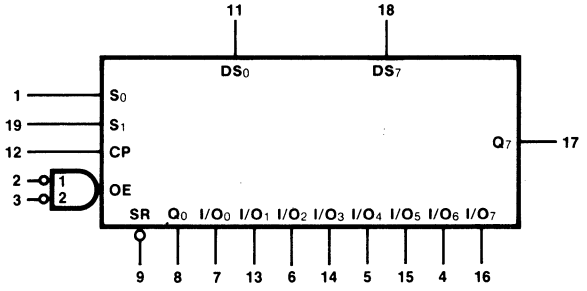
(With Synchronous Reset and Common I/O Pins)

54F/74F323

Description — The 'F323 is an 8-bit universal shift/register with 3-state outputs. Its function is similar to the 'F299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate inputs and outputs are provided for flip-flops Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load. The flip-flops are edge-triggered and state changes are initiated by the rising edge of the clock.

Multiplexed Parallel I/O Ports
Separate Serial Inputs and Outputs
Expandable Bidirectional Shifting
3-State Outputs for Bus Applications
Shift Frequency 80 MHz Typ
Propagation Delay 9.0 ns Typ
Supply Current 66 mA Typ

Logic Symbol



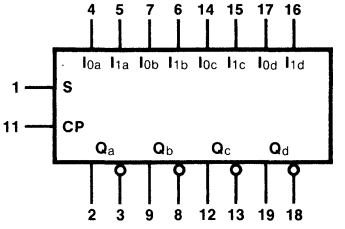
V_{CC} = Pin 20
GND = Pin 10

Quad 2-Port Register **54F/74F398**

Description — The 'F398 is the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. Both the true and complement outputs of the flip-flops are available.

Select Inputs from Two Sources
Fully Edge-Triggered
True and Complement Outputs
Propagation Delay 6.3 ns Typ
Clock Frequency 150 MHz Typ
Supply Current 21 mA Typ

Logic Symbol



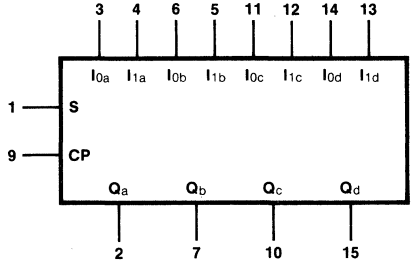
V_{CC} = Pin 20
GND = Pin 10

Quad 2-Port Register **54F/74F399**

Description — The 'F399 is the logical equivalent of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flops on the rising edge of the clock. The 'F399 is the 16-pin version of the 'F398, with only the Q outputs of the flip-flops available.

Select Inputs from Two Sources
Fully Edge-Triggered
Propagation Delay 6.3 ns Typ
Clock Frequency 150 MHz Typ
Supply Current 21 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

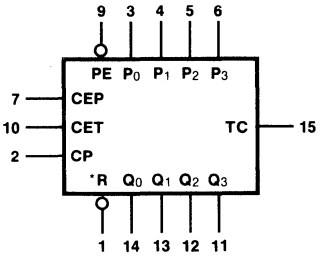
Synchronous Presettable BCD Decade Counter

54F/74F160
54F/74F162

Description — The 'F160 and 'F162 are high speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'F160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'F162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

Synchronous Counting and Loading
High Speed Synchronous Expansion
Propagation Delay 7.5 ns Typ
Count Frequency 120 MHz Typ
Supply Current 35 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8
*MR for '160
*SR for '162

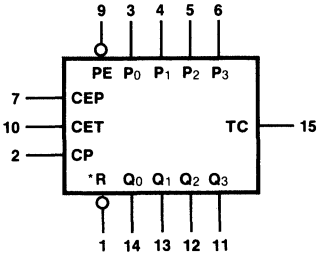
Synchronous Presettable Binary Counter

54F/74F161
54F/74F163

Description — The 'F161 and 'F163 are high speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'F161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'F163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

Synchronous Counting and Loading
High Speed Synchronous Expansion
Propagation Delay 7.5 ns Typ
Count Frequency 120 MHz Typ
Supply Current 35 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8
*MR for '161
*SR for '163

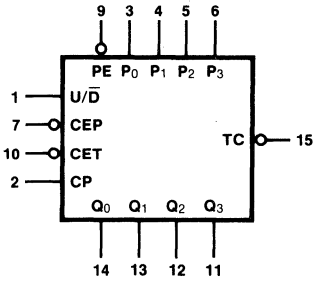
Synchronous Bidirectional BCD Decade Counter

54F/74F168

Description — The 'F168 is a fully synchronous 4-stage up/down counter. This device features preset capability for programmable operation, carry lookahead for easy cascading, and an U/D input to control the direction of counting. It counts in the BCD (8421) sequence and all state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

Synchronous Counting and Loading
Built-in Lookahead Carry Capability
Propagation Delay 7.0 ns Typ
Count Frequency 100 MHz Typ
Supply Current 37 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

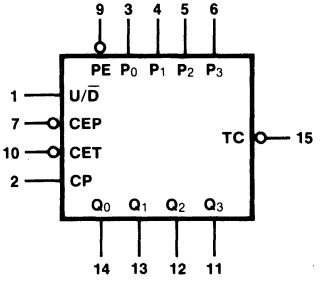
Synchronous Bidirectional Modulo-16 Binary Counter

54F/74F169

Description — The 'F169 is a fully synchronous 4-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

Synchronous Counting and Loading
Built-in Lookahead Carry Capability
Propagation Delay 7.0 ns Typ
Count Frequency 100 MHz Typ
Supply Current 37 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Up/Down Decade Counter

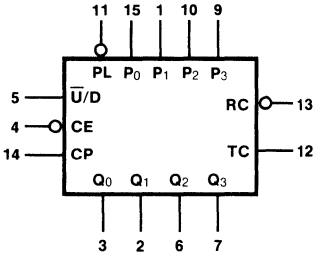
(With Preset and Ripple Clock)

54F/74F190

Description — The 'F190 is a reversible BCD (8421) decade counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock. The Count Enable and Up/Down control inputs can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Synchronous Counting
Asynchronous Parallel Load
Propagation Delay 5.5 ns Typ
Count Frequency 130 MHz Typ
Supply Current 38 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Up/Down Binary Counter

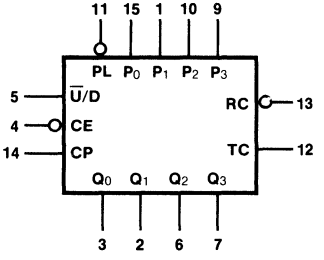
(With Preset and Ripple Clock)

54F/74F191

Description — The 'F191 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are intiated by the rising edge of the clock. The Count Enable and Up/Down control inputs can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Synchronous Counting
Asynchronous Parallel Load
Propagation Delay 5.5 ns Typ
Count Frequency 130 MHz Typ
Supply Current 38 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Up/Down Decade Counter

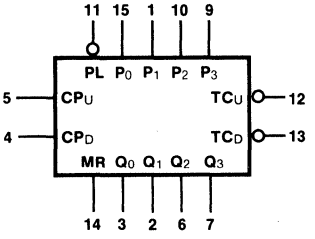
54F/74F192

(With Separate Up/Down Clocks)

Description — The 'F192 is a reversible BCD decade (8421) counter featuring synchronous counting and asynchronous parallel loading. Separate Count Up and Count Down clock inputs determine the direction of counting and in either mode the circuits operate synchronously. State changes are initiated by the rising edge of the clock. Separate Terminal Count Up (carry) and Terminal Count Down (borrow) outputs are gated clocks for a subsequent stage, thus simplifying multistage counter designs. Preset data inputs make the 'F192 useful in programmable counters. The Parallel Load ($\overline{PL}$) input overrides counting, while the Master Reset (MR) input overrides both counting and parallel loading.

Separate Up and Down Clocks
Asynchronous Parallel Loading
Carry and Borrow Outputs for Cascading
Propagation Delay 5.5 ns Typ
Count Frequency 130 MHz Typ
Supply Current 35 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Up/Down Binary Counter

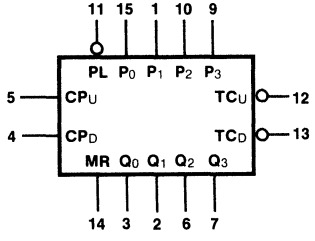
54F/74F193

(With Separate Up/Down Clocks)

Description — The 'F193 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous parallel loading. Separate Count Up and Count Down clocks determine the direction of counting and in either mode the circuits operate synchronously. State changes are initiated by the rising edge of the clock. Separate Teminal Count Up (carry) and Terminal Count Down (borrow) outputs are gated clocks that need no external logic to serve as clocks for a subsequent stage, thus simplifying multistage counter designs. Preset data inputs make the 'F193 useful in programmable counters. The Parallel Load ($\overline{PL}$) input overrides counting, while the Master Reset (MR) input overrides both counting and parallel loading.

Separate Up and Down Clocks
Asynchronous Parallel Loading
Carry and Borrow Outputs for Cascading
Propagation Delay 5.5 ns Typ
Count Frequency 130 MHz Typ
Supply Current 35 ns Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Synchronous Bidirectional BCD Decade Counter

(With 3-State Outputs)

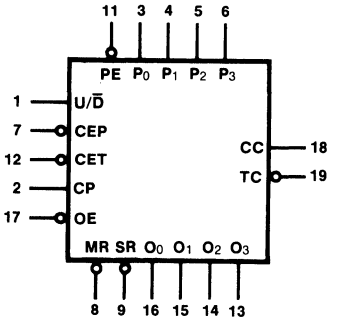
54F/74F568

3

Description — The 'F568 is a fully synchronous, reversible decade counter with 3-state outputs. It features a preset capability for programmable operation, carry lookahead for easy cascading, and a U/$\overline{D}$ input to control the direction of counting. For maximum flexibility there are both synchronous and asynchronous reset inputs as well as both a Clocked Carry (CC) and a Terminal Count ($\overline{TC}$). All state changes, except Master Reset, are initiated by the rising edge of the clock. A HIGH signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high-Z state but does not prevent counting, resetting or parallel loading.

Synchronous Counting and Loading
Built-in Lookahead Carry Capability
Propagation Delay 7.5 ns Typ
Count Frequency 100 MHz Typ
Supply Current 45 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

Synchronous Bidirectional Binary Counter

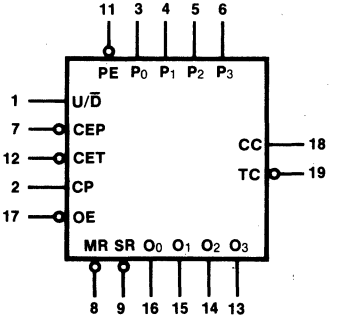
(With 3-State Outputs)

54F/74F569

Description — The 'F569 is a fully synchronous, reversible binary counter with 3-state outputs. It features a preset capability for programmable operation, carry lookahead for easy cascading, and a U/$\overline{D}$ input to control the direction of counting. For maximum flexibility there are both synchronous and asynchronous reset inputs as well as both a Clocked Carry (CC) and a Terminal Count ($\overline{TC}$). All state changes except Master Reset are initiated by the rising edge of the clock. A HIGH signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high-Z state but does not prevent counting, resetting or parallel loading.

Synchronous Counting and Loading
Built-in Lookahead Carry Capability
Propagation Delay 7.5 ns Typ
Count Frequency 100 MHz Typ
Supply Current 45 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

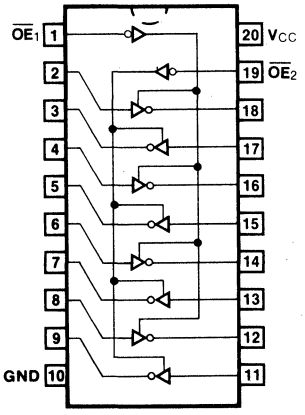
Octal Buffer/Line Driver **54F/74F240**

(With 3-State Outputs)

Description — The 'F240 contains eight inverting buffers with 3-state outputs. They offer improved PC board density and are well suited as memory address drivers, clock drivers and bus oriented transmitters or receivers. The 'F240 has a pair of active-LOW Output Enable ($\overline{OE}$) inputs, each of which controls four of the buffers. The data inputs are designed with Schmitt-type hysteresis to increase noise margins. Outputs are designed to exhibit low leakage in the power-down condition.

Inverting Buffers
Separate 4-Bit Enables
Output Sink 64 mA, Source 15 mA
Hysteresis on Data Inputs
Propagation Delay 4.5 ns Typ
Supply Current 64 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

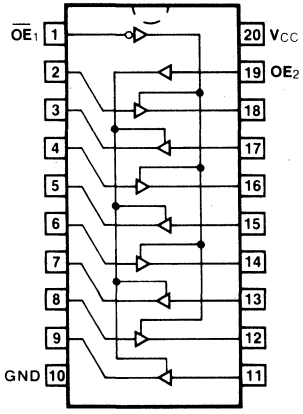
Octal Buffer/Line Driver **54F/74F241**

(With 3-State Outputs)

Description — The 'F241 contains eight non-inverting buffers with 3-state outputs. Four of the buffers are controlled by an active-HIGH Output Enable (OE) input and four are controlled by an active-LOW $\overline{OE}$ input. This makes them well suited for pairing in transceiver applications. The data inputs are designed with Schmitt-type hysteresis to increase noise margins. Outputs are designed to exhibit low leakage in the power-down condition.

Non-Inverting Buffers
Opposite Polarity 4-Bit Enables
Outputs Sink 64 mA, Source 15 mA
Hysteresis on Data Inputs
Propagation Delay 6.0 ns Typ
Supply Current 64 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

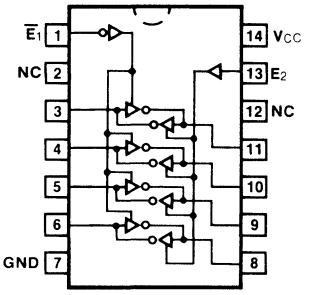
Quad Bus Transceiver **54F/74F242**

(With 3-State Outputs)

Description — The 'F242 contains four inverting transceivers with 3-state outputs. They are designed for 4-line asynchronous 2-way communication between data or control busses. An active-LOW Output Enable ($\overline{OE}$) input controls data flow in one direction; an active-HIGH OE input controls data flow in the other direction. The data inputs are designed with Schmitt-type hysteresis to increase noise margins. Outputs are designed to exhibit low leakage in the power-down condition.

Inverting Buffers
2-Way Bus Communication
Outputs Sink 64 mA, Source 15 mA
Hysteresis on Data Inputs
Propagation Delay 4.5 ns Typ
Supply Current 64 mA Typ

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

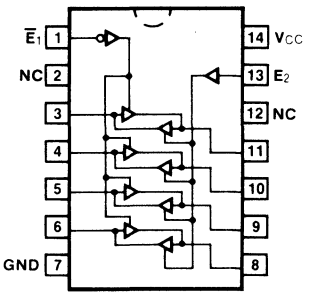
Quad Bus Transceiver **54F/74F243**

(With 3-State Outputs)

Description — The 'F243 contains four non-inverting transceivers with 3-state outputs. They are designed for 4-line asynchronous 2-way communication between data or control busses. An active-LOW Output Enable ($\overline{OE}$) input controls data flow in one direction; an active-HIGH OE input controls data flow in the other direction. The data inputs are designed with Schmitt-type hysteresis to increase noise margins. Outputs are designed to exhibit low leakage in the power-down condition.

Non-Inverting Buffers
2-Way Bus Communication
Outputs Sink 64 mA, Source 15 mA
Hysteresis on Data Inputs
Propagation Delay 6.0 ns Typ
Supply Current 64 mA Typ

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

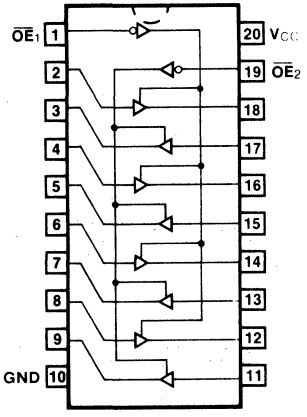
Octal Buffer/Line Driver 54F/74F244

(With 3-State Outputs)

Description — The 'F244 contains eight non-inverting buffers with 3-state outputs. They offer improved PC board density and are well suited as memory address drivers, clock drivers and bus oriented transmitters or receivers. The 'F244 has a pair of active-LOW Output Enable ($\overline{OE}$) inputs, each of which controls four of the buffers. The data inputs are designed with Schmitt-type hysteresis to increase noise margins. Outputs are designed to exhibit low leakage in the power-down condition.

Non-Inverting Buffers
Separate 4-Bit Enables
Outputs Sink 64 mA, Source 15 mA
Hysteresis on Data Inputs
Propagation Delay 6.0 ns Typ
Supply Current 64 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

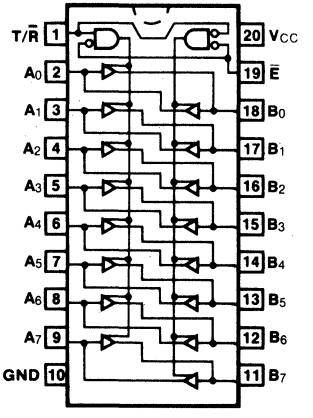
Octal Bidirectional Transceiver 54F/74F245

(With 3-State Inputs/Outputs)

Description — The 'F245 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. Current sinking capability is 20 mA at the A ports and 64 mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a 3-state condition. Output HIGH voltage V_{OH} is specified as 3.6 V for MOS interfacing.

Non-Inverting Buffers
Bidirectional Data-Path
B Outputs Sink 64 mA, Source 15 mA
V_{OH} Specified as 3.6 V at 0.4 mA
Propagation Delay 6.0 ns Typ
Supply Current 128 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

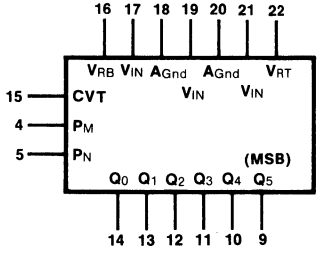
Analog-to-Digital Converter

54F/74F500

Description — The 'F500 is a 6-bit, fully parallel analog-to-digital converter capable of sampling at rates from 0 to 50 MHz. Conversion is accomplished by 64 comparators spaced one quanta apart on a voltage reference ladder. All comparators measure the analog input against their reference simultaneously. The most significant comparator that finds the analog input to be greater than its reference has its output encoded to a 6-bit, active-HIGH binary number, stored in latches. Two polarity control inputs are provided: P_M complements the most significant output bit and P_L complements the lesser five output bits. The circuit operates from +5.0 V and -6.0 V supplies and has separate digital and analog grounds. Both ends of the reference ladder are brought out, one to V_{RT} (nominally zero volts) and the other to V_{RB} (nominally -1.0 V).

No Sample and Hold Required
Sampling Rate 40 MHz Typ
Aperture Time 4.0 ns Typ
V_{CC} Supply Current 20 mA Typ
V_{EE} Supply Current 102 mA Typ

Logic Symbol



V_{CC} = Pin 7
V_{EE} = Pins 1, 6
D_{Gnd} = Pin 8
NC = Pins 2, 3

Octal Bidirectional Transceiver

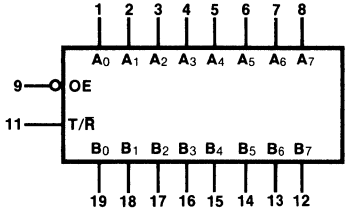
(With 3-State Inputs/Outputs)

54F/74F545

Description — The 'F545 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. Current sinking capability is 20 mA at the A ports and 64 mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a 3-state condition. Output HIGH voltage V_{OH} is specified as 3.6 V for MOS interfacing.

Non-Inverting Buffers
Bidirectional Data Path
B Outputs Sink 64 mA, Source 15 mA
V_{OH} Specified as 3.6 V at 0.4 mA
Propagation Delay 6.0 ns Typ
Supply Current 128 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

Octal Bidirectional Transceiver

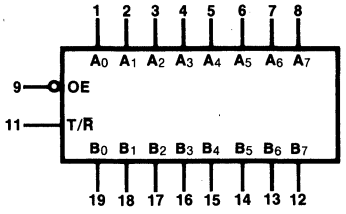
(With 3-State Inputs/Outputs and IEEE-488 Termination Resistors)

54F/74F588

Description — The 'F588 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applicaitons. The B ports have termination resistors as specified in the IEEE-488 specifications. Current sinking capability is 20 mA at the A ports and 48 mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a 3-state condition.

Non-Inverting Buffers
Bidirectional Data Path
B Outputs Sink 48 mA, Source 15 mA
Propagation Delay 6.0 ns Typ
Supply Current 128 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

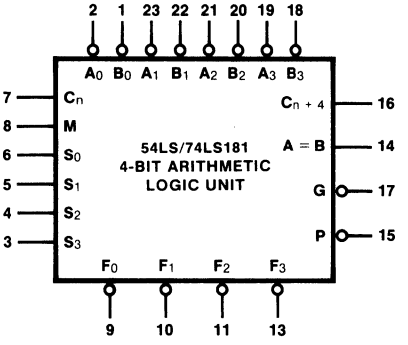
4-Bit Arithmetic Logic Unit

54F/74F181

Description — The 'F181 is a 4-bit Arithmetic Logic Unit capable of performing 16 arithmetic or 16 logic operations on two 4-bit operands $A_0 — A_3$ and $B_0 — B_3$. The Carry Out (C_{n+4}) output is provided for ripple carry expansion, while the Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs can be used with an 'F182 or similar Carry Lookahead Generators for faster operations on longer words. The Mode Control (M) input determines whether a logic (M = H) or an arithmetic (M = L) operation is performed. Signals applied to the Select ($S_0 — S_3$) inputs determine the specific function or operation.

Performs 16 Arithmetic Operations
Performs 16 Logic Functions
Internal Lookahead for Fast Ripple Carry
$\overline{G}$ and $\overline{P}$ Outputs for External Lookahead
A or B to Carry Delay 9.0 ns Typ
Ex-OR Logic Delay 5.0 ns Typ
Supply Current 39 mA Typ

Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

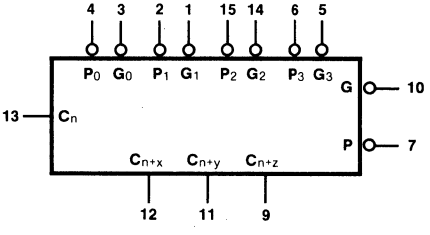
Carry Lookahead Generator

54F/74F182

Description — The 'F182 is a high-speed carry lookahead generator for use with the 'F181, 'F381, 2901A or other 4-bit ALUs in arithmetic operations on words longer than four bits. It accepts up to four pairs of active-LOW Carry Propagate ($\overline{P}_0 — \overline{P}_3$) and Carry Generate ($\overline{G}_0 — \overline{G}_3$) signals, an active-HIGH Carry input (C_n) and provides anticipated active-HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four ALUs. It also has active-LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs for optional use in further levels of lookahead. The 'F182 works equally well when the ALU operand inputs follow either the active-LOW or the active-HIGH convention.

Provides Lookahead Across Four ALUs
Multi-Level Capability for Longer Words
Less Loading of ALU Outputs
Propagation Delay 4.6 ns Typ
Supply Current 19 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

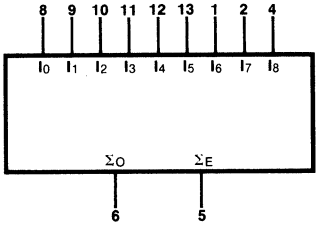
9-Bit Parity Generator/Checker

54F/74F280

Description — The 'F280 is a high-speed parity generator/checker that accepts nine bits of input data and detects whether the number of HIGH inputs is even or odd. If even, the Sum Even output is HIGH; if odd, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output. For longer words, the Sum Even output is used as an input to the next package.

Nine Input Lines
Odd or Even Parity
Propagation Delay 12.5 ns Typ
Supply Current 25 mA Typ

Logic Symbol



V_{CC} = Pin 14
GND = Pin 7

4-Bit Binary Full Adder

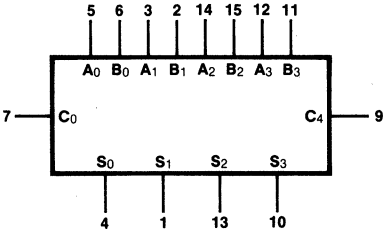
(With Fast Carry)

54F/74F283

Description — The 'F283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words ($A_0 - A_3$, $B_0 - B_3$) and a Carry input (C_0). It generates the binary Sum outputs ($S_0 - S_3$) and the Carry output (C_4) from the most significant bit. The 'F283 will operate with either active-HIGH or active-LOW operands (positive or negative logic).

Adds Two 4-Bit Numbers
Full Internal Carry Lookahead
Fast Ripple Carry for Economical Expansion
Ripple Carry Delay 4.7 ns Typ
Sum Output Delay 8.5 Typ
Supply Current 30 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

4-Bit Shifter

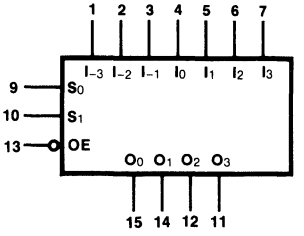
(With 3-State Outputs)

54F/74F350

Description — The 'F350 is a specialized multiplexer that accepts a 4-bit word and shifts it 0, 1, 2 or 3 places, as determined by two Select (S_0, S_1) inputs. For expansion to longer words, three linking inputs are provided for lower-order bits; thus two packages can shift an 8-bit word, four packages a 16-bit word, etc. Shifting by more than three places is accomplished by paralleling the 3-state outputs of different packages and using the Output Enable (OE) inputs as a third Select level. With appropriate interconnections, the 'F350 can perform zero-backfill, sign-extend or end-around (barrel) shift functions. This circuit is the functional equivalent of the AM25S10.

Linking Inputs for Word Expansion
3-State Outputs for Extending Shift Range
Propagation Delay 4.5 ns Typ
Supply Current 28 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

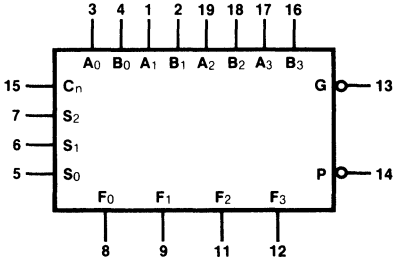
4-Bit Arithmetic Logic Unit

54F/74F381

Description — The 'F381 is a 20-pin ALU that performs three arithmetic operations (A plus B, A minus B, B minus A) and three logic functions (AND, OR, Exclusive-OR) on two 4-bit words, A and B. Two additional Select input codes force the Function (F_0 — F_3) outputs LOW or HIGH. Carry Propagate ($\overline{P}$) and Generate ($\overline{G}$) outputs are provided for use with the 'F182 Carry Lookahead Generator for high-speed expansion to longer word lengths. For ripple expansion, please refer to the 'F382 ALU.

20-Pin Space-Saving Package
Minimum Input Drive Required
Performs Eight Functions
$\overline{P}$ and $\overline{G}$ Outputs for Expansion
Subtract Delay 8.5 ns Typ
Lookahead Delay 7.6 ns Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

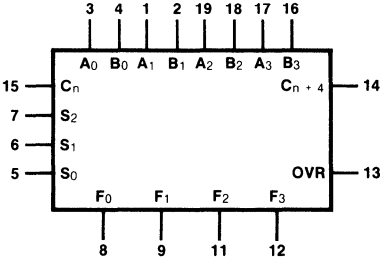
4-Bit Arithmetic Logic Unit

54F/74F382

Description — The 'F382 is a 20-pin ALU that performs three arithmetic operations (A plus B, A minus B, B minus A) and three logic functions (AND, OR, Exclusive-OR) on two 4-bit words, A and B. Two additional Select input codes force the Function (F_0 — F_3) outputs LOW or HIGH. An Overflow output is provided for convenience in twos complement arithmetic. A Carry output is provided for ripple expansion. For high-speed expansion using a Carry Lookahead Generator, please refer to the 'F381.

20-Pin Space-Saving Package
Minimum Input Drive Required
Performs Eight Functions
Ripple Carry and Overflow Outputs
A or B to Carry Output Delay 10 ns Typ
Select to Output Delay 14.5 ns Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

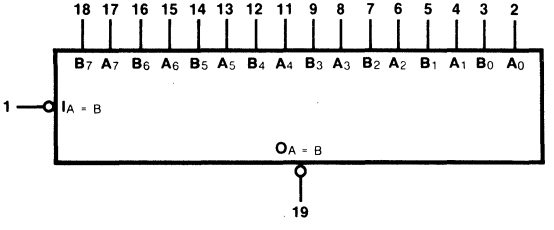
8-Bit Identity Comparator

54F/74F521

Description — The 'F521 is an expandable 8-bit comparator. It compares two words of up to eight bits each and provides a LOW output when the two words match bit for bit. For longer words, two or more packages can be cascaded by means of the $\overline{I}_{A=B}$ input, which also serves as an active-LOW enable input.

Compares Two 8-Bit Words
Expandable for Longer Words
Space-Saving 20-Pin Package
Propagation Delay 7.5 ns Typ
Supply Current 28 mA Typ

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

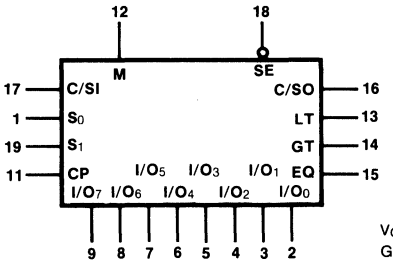
Registered Comparator

54F/74F524

Description — The 'F524 contains an 8-bit register with common parallel I/O pins and a comparator operating from the register contents and the I/O signals. Two select inputs (S_0, S_1) determine whether the circuit is operating in Parallel Load, Parallel Output, Serial Shift or Hold modes. Serial data (LSB first) enters the C/SI pin and exits via the C/SO pin for linking to the next lower order package for longer word lengths. C/SI and C/SO linking also establishes the status output priority of a more significant package over a lesser one. Three active-HIGH open-collector status outputs — register contents greater than (GT), less than (LT) and equal to (EQ) the I/O bus data — are used in a wired-AND configuration when word length requires two or more packages. A HIGH signal on the Status Enable ($\overline{SE}$) input forces all three status outputs to the OFF state. The Mode control (M) input complements the MSB input to each part of the comparator for use with twos complement numbers.

Compare 8-Bit Magnitude or Twos Complement
Expandable in 8-Bit Increments
Serial or Parallel Entry
Linking Pins for Serial Entry and Status Priority
Shift Frequency 75 MHz Typ
Parallel Data to Status Output Delay 16 ns Typ
Supply Current 128 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

8-Bit by 8-Bit Multiplier

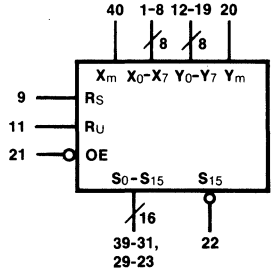
(With 3-State Outputs)

54F/74F557
54F/74F558

Description — The 'F558 is a high-speed combinatorial array that multiplies two 8-bit unsigned or signed twos complement numbers and provides the 16-bit unsigned or signed product. Each input operand X and Y has a mode control input that determines whether the number is treated as signed or unsigned. Two additional inputs, R_S and R_U, allow the addition of a bit for rounding to the best signed or unsigned fractional 8-bit result. For expansion during signed or mixed multiplication, both the true and complement outputs of the most significant bit are available.The 'F557 is identical to the 'F558 except that it has output latches that store the results when OE is LOW.

Unsigned, Signed or Mixed Multiplication
Full 16-Bit Product Outputs
MSB Complement Output for Signed Expansion
Rounding Inputs for Fractional 8-Bit Product
Propagation Delay 50 ns Typ
Supply Current 200 mA Typ

Logic Symbol



V_{CC} = Pin 10
GND = Pin 30

Expandable 8-Bit Twos Complement Multiplier/Divider

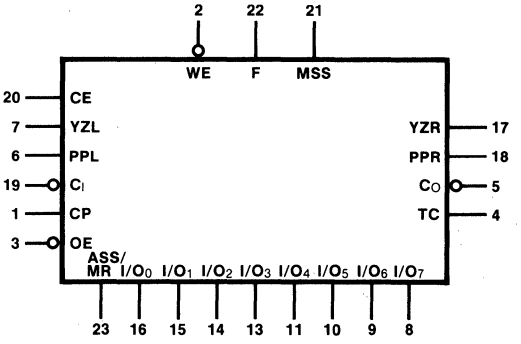
(With 3-State Outputs)

54F/74F559

Description — The 'F559 implements fast signed twos complement multiplication and division as an asynchronous peripheral in microprocessor and minicomputer systems. It contains an 8-bit ALU, three 8-bit registers, a 4-bit sequence counter and the control logic necessary to perform multiply, rounded multiply, fractional divide and integer divide operations. The two 8-bit operands are entered successively at the I/O ports, whereupon the circuit operates internally at a rate determined by an externally applied clock frequency of up to 25 MHz. Upon completion, and upon command, results are presented at the I/O ports in successive 8-bit words. Linking inputs and outputs are provided for expansion to longer words by using two or more multipliers operating on the same 8-bit bus.

Signed Twos Complement Arithmetic
Increases Processor Efficiency
Low System Parts Count
Expandable in 8-Bit Increments
8-Bit Bus Oriented 3-State I/O
16-Bit Multiply in 1.2 μs Typ
16-Bit Divide in 1.6 μs Typ

Logic Symbol



V_{CC} = Pin 24
GND = Pin 12

64-Bit Random Access Memory

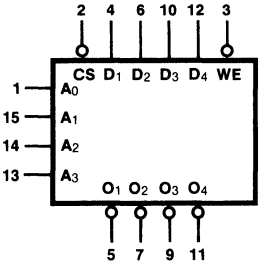
(With 3-State Outputs)

54F/74F189

Description — The 'F189 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

3-State Outputs for Bus Applications
Buffered Inputs for Minimum Loading
Address Decoding On-Chip
Address Access Time 20 ns Typ
Chip Select Access Time 12 ns Typ
Supply Current 43 mA Typ

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

64-Bit Random Access Memory

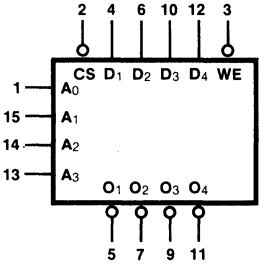
(With Open-Collector Outputs)

54F/74F289

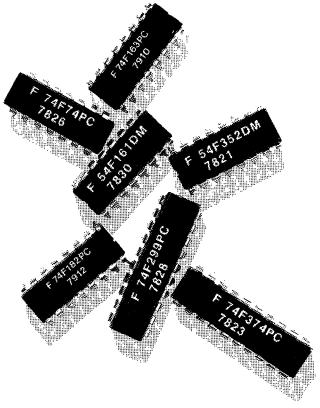
Description — The 'F289 is a high-speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode; output data is the complement of the stored data.

Open-Collector Outputs
Buffered Inputs Minimize Loading
Address Decoding On-Chip
Address Access Time 20 ns Typ
Chip Select Access Time 12 ns Typ
Supply Current 43 mA Typ

Logic Symbol



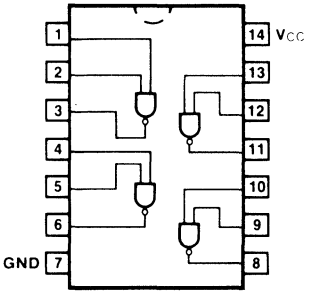
V_{CC} = Pin 16
GND = Pin 8



54F/74F00

QUAD 2-INPUT NAND GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F00PC		9A
Ceramic DIP (D)	74F00DC	54F00DM	6A
Flatpak (F)	74F00FC	54F00FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			2.8	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}				10.2		V_{IN} = Open	

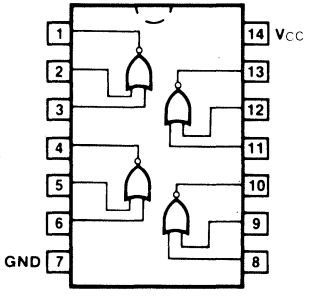
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	1.5	2.9	3.9	2.0	7.0	2.0	6.0	ns	2-17
t_{PHL}		1.5	2.6	3.6	2.0	6.5	2.0	5.5		2-18

54F/74F02

QUAD 2-INPUT NOR GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F02PC		9A
Ceramic DIP (D)	74F02DC	54F02DM	6A
Flatpak (F)	74F02FC	54F02FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			5.6	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}				13		*	

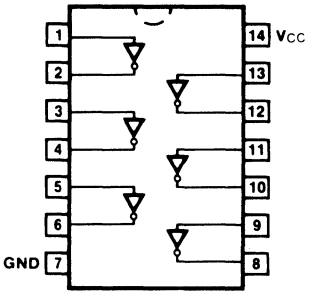
AC CHARACTERISITCS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.0	3.5	4.8	2.5	8.0	2.5	7.0	ns	2-17
t_{PHL}		1.5	2.6	3.5	2.0	6.5	2.0	5.5		2-18

*Measured with one input HIGH, one input LOW for each gate.

54F/74F04
HEX INVERTER

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F04PC		9A
Ceramic DIP (D)	74F04DC	54F04DM	6A
Flatpak (F)	74F04FC	54F04FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC CHARACTERISITCS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			4.2	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}				15.3		V_{IN} = Open	

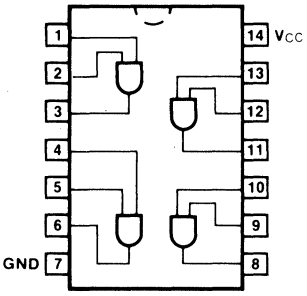
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	1.5	2.7	3.8	2.0	7.0	2.0	6.0	ns	2-17
t_{PHL}		1.5	2.5	3.5	2.0	6.5	2.0	5.5		2-18

54F/74F08

QUAD 2-INPUT AND GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F08PC		9A
Ceramic DIP (D)	74F08DC	54F08DM	6A
Flatpak (F)	74F08FC	54F08FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC CHARACTERISITCS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			8.3	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}				12.9		V_{IN} = Gnd	

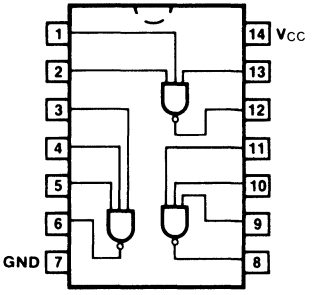
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.0	4.1	5.5	3.0	8.8	3.0	7.0	ns	2-17
t_{PHL}		2.5	3.6	5.0	3.0	7.0	3.0	6.0		2-19

54F/74F10

TRIPLE 3-INPUT NAND GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F10PC		9A
Ceramic DIP (D)	74F10DC	54F10DM	6A
Flatpak (F)	74F10FC	54F10FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC CHARACTERISITCS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			2.1	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}				7.7		V_{IN} = Open	

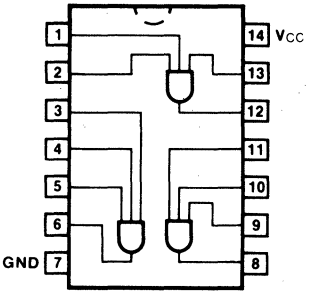
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = 5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	1.5	2.9	3.9	2.0	7.0	2.0	6.0	ns	2-17
t_{PHL}		1.5	2.7	3.7	2.0	6.5	2.0	5.5		2-18

54F/74F11

TRIPLE 3-INPUT AND GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F11PC		9A
Ceramic DIP (D)	74F11DC	54F11DM	6A
Flatpak (F)	74F11FC	54F11FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs Outputs	0.5/0.375 25/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH} I_{CCL}	Power Supply Current			6.2 9.7	mA	V_{IN} = Open V_{IN} = Gnd	V_{CC} = Max

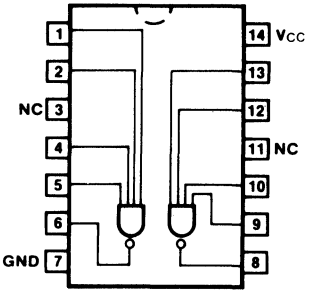
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	2.5 2.5	4.2 3.7	5.5 5.0	3.0 3.0	8.0 7.0	3.0 3.0	7.0 6.0	ns	2-17 2-19

54F/74F20

DUAL 4-INPUT NAND GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F20PC		9A
Ceramic DIP (D)	74F20DC	54F20DM	6A
Flatpak (F)	74F20FC	54F20FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			1.4	mA	V_{IN} = Gnd	V_{CC} = Max
I_{CCL}				5.1		V_{IN} = Open	

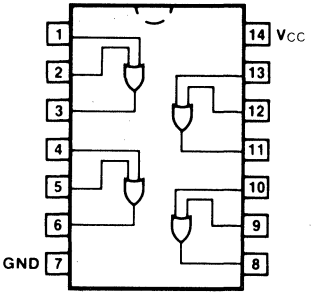
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	1.5	2.9	3.9	2.0	7.0	2.0	6.0	ns	2-17
t_{PHL}		1.5	2.8	3.8	2.0	6.5	2.0	5.5		2-18

54F/74F32

QUAD 2-INPUT OR GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F32PC		9A
Ceramic DIP (D)	74F32DC	54F32DM	6A
Flatpak (F)	74F32FC	54F32FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH}	Power Supply Current			8.3	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}				15.5		V_{IN} = Gnd	

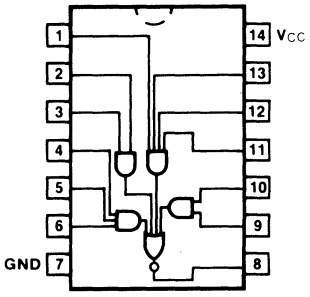
AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	2.5	3.9	5.5	3.0	8.0	3.0	7.0	ns	2-17
t_{PHL}		2.5	3.5	5.0	3.0	7.0	3.0	6.0		2-19

54F/74F64

4-2-3-2-INPUT AND OR-INVERT GATE

CONNECTION DIAGRAM



ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F64PC		9A
Ceramic DIP (P)	74F64DC	54F64DM	6A
Flatpak (F)	74F64FC	54F64FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
	Inputs	0.5/0.375
	Outputs	25/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS	
		Min	Typ	Max			
I_{CCH} I_{CCL}	Power Supply Current			2.8 4.7	mA	V_{IN} = Gnd *	V_{CC} = Max

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay	1.5 1.5	3.6 2.8	4.8 3.8	2.0 2.0	8.0 6.5	2.0 2.0	7.0 5.5	ns	2-17 2-18

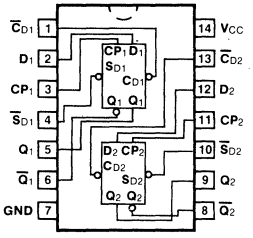
*I_{CCL} is measured with all inputs of one gate open and remaining inputs grounded.

54F/74F74

DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The 'F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

CONNECTION DIAGRAM



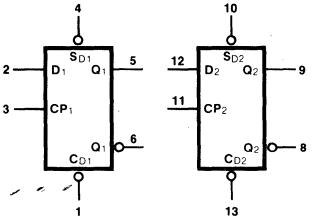
TRUTH TABLE
(Each Half)

INPUT	OUTPUTS	
@ t_n	@ t_{n+1}	
D	Q	$\overline{Q}$
L	L	H
H	H	L

Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

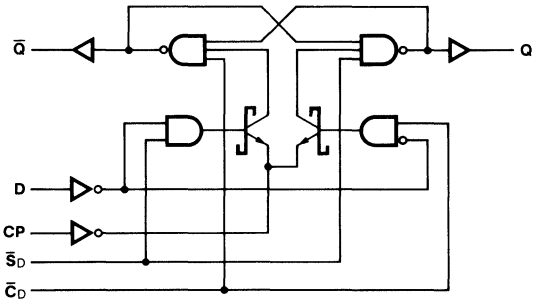
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F74PC		9A
Ceramic DIP (D)	74F74DC	54F74DM	6A
Flatpak (F)	74F74FC	54F74FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
D_1, D_2	Data Inputs	0.5/0.375
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	0.5/0.375
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	0.5/1.125
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.125
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs	25/12.5

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		10.5	16	mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	125						MHz	2-17/21
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	2.0 2.0	4.4 5.2	6.0 7.0					ns	2-17 2-21
t_{PLH} t_{PHL}	Propagation Delay $V_{CP} \geq 2.0$ V $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	2.0 2.0	3.6 6.5	5.5 8.0					ns	2-17 2-22
t_{PLH} t_{PHL}	Propagation Delay $V_{CP} \leq 0.8$ V $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		2.8 5.5						ns	2-17 2-22

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = MIL		T_A, V_{CC} = COM			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to CP_n	2.0 3.0							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to CP_n	1.0 1.0								
t_w (H) t_w (L)	CP_n Pulse Width, HIGH or LOW	4.0 5.0							ns	2-21
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.0							ns	2-22
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0							ns	2-24

54F/74F109

DUAL J$\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP

DESCRIPTION — The 'F109 consists of two high speed, completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop (refer to 'F74 data sheet) by connecting the J and $\overline{K}$ inputs together.

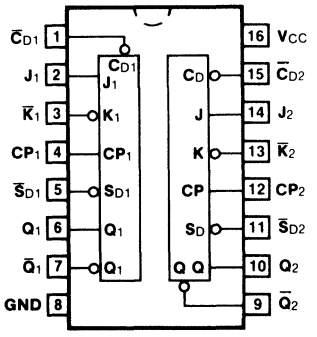
TRUTH TABLE

INPUTS		OUTPUTS
@ t_n		@ t_{n+1}
J	$\overline{K}$	Q $\overline{Q}$
L	H	No Change
L	L	L H
H	H	H L
H	L	Toggles

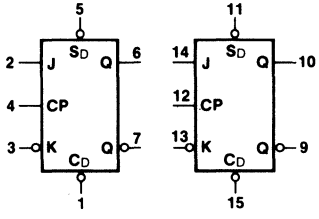
Asynchronous Inputs:
LOW input to $\overline{S}_D$ sets Q to HIGH level
LOW input to $\overline{C}_D$ sets Q to LOW level
Clear and Set are independent of clock
Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.
H = HIGH Voltage Level
L = LOW Voltage Level

CONNECTION DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

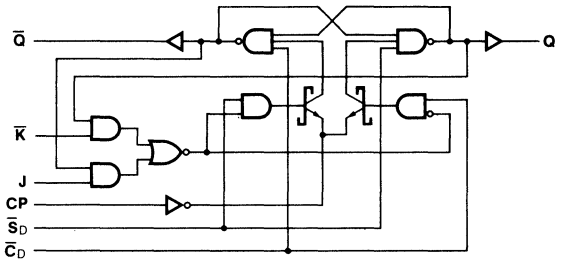
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F109PC		9B
Ceramic DIP (D)	74F109DC	54F109DM	6B
Flatpak (F)	74F109FC	54F109FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
J_1, J_2, $\overline{K}_1$, $\overline{K}_2$	Data Inputs	0.5/0.375
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	0.5/0.375
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs (Active LOW)	0.5/1.125
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs (Active LOW)	0.5/1.125
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs	25/12.5

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		11.7		mA	V_{CC} = Max, V_{CP} = 0 V

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency		125						MHz	2-17/21
t_{PLH} t_{PHL}	Propagation Delay CP_n to Q_n to $\overline{Q}_n$		4.4 5.2						ns	2-17/21
t_{PLH} t_{PHL}	Propagation Delay ($V_{CP} \geq 2.0$ V) $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		3.6 6.5						ns	2-17/22
t_{PLH} t_{PHL}	Propagation Delay ($V_{CP} \leq 0.8$ V) $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$		2.8 5.5						ns	2-17/22

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

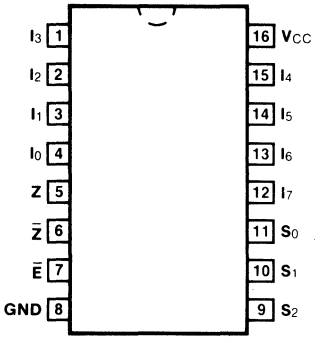
SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V			54F T_A, V_{CC} = MIL		74F T_A, V_{CC} = COM		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	2.0 3.0							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	1.0 1.0								
t_w (H) t_w (L)	CP_n Pulse Width, HIGH or LOW	4.0 5.0							ns	2-21
t_w (L)	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width LOW	4.0							ns	2-22
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	2.0							ns	2-24

54F/74F151

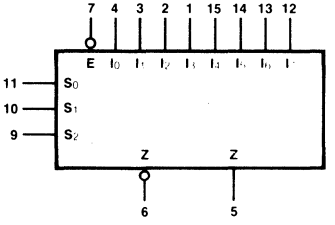
8-INPUT MULTIPLEXER

DESCRIPTION — The 'F151 is a high speed 8-input digital multiplexer. It provides in one package, the ability to select one line of data from up to eight sources. The 'F151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

CONNECTION DIAGRAM



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	74F151PC		9B
Ceramic DIP (D)	74F151DC	54F151DM	6B
Flatpak (F)	74F151FC	54F151FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$I_0 - I_7$	Data Inputs	0.5/0.375
$S_0 - S_2$	Select Inputs	0.5/0.375
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
Z	Data Output	25/12.5
$\overline{Z}$	Inverted Data Output	25/12.5

FUNCTIONAL DESCRIPTION — The 'F151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2).$$

The 'F151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 'F151 can provide any logic function of four variables and its negation.

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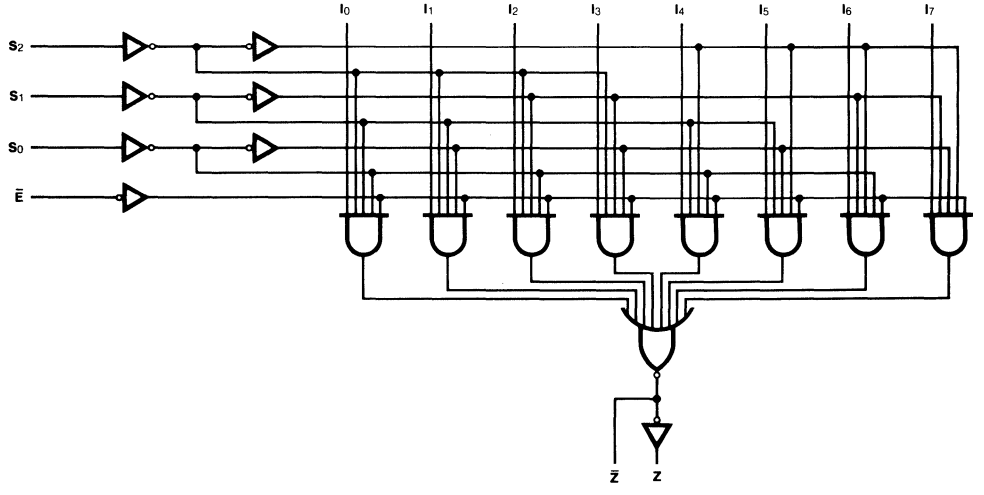
TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		11		mA	V_{CC} = Max, V_{IN} = 4.5 V

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

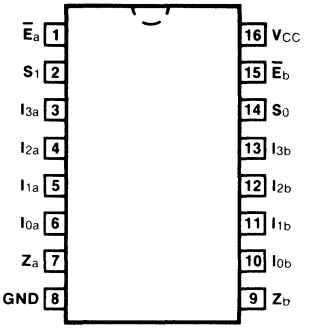
SYMBOL	PARAMETER	54F/74F			54F		54F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}$		6.3 6.2						ns	2-17 2-18
t_{PLH} t_{PHL}	Propagation Delay S_n to Z		8.1 7.9						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$		4.6 4.5						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z		6.4 6.2						ns	2-17 2-18
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$		2.9 2.8						ns	2-17 2-18
t_{PLH} t_{PHL}	Propagation Delay I_n to Z		4.7 4.5						ns	2-17 2-19

54F/74F153

DUAL 4-INPUT MULTIPLEXER

DESCRIPTION — The 'F153 is a high speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the 'F153 can generate any two functions of three variables.

CONNECTION DIAGRAM



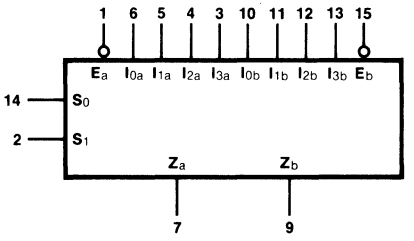
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F153PC		9B
Ceramic DIP (D)	74F153DC	54F153DM	6B
Flatpak (F)	74F153FC	54F153FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
I_{0a} — I_{3a}	Side A Data Inputs	0.5/0.375
I_{0b} — I_{3b}	Side B Data Inputs	0.5/0.375
S_0, S_1	Common Select Inputs	0.5/0.375
$\overline{E}_a$	Side A Enable Input (Active LOW)	0.5/0.375
$\overline{E}_b$	Side B Enable Input (Active LOW)	0.5/0.375
Z_a	Side A Output	25/12.5
Z_b	Side B Output	25/12.5

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The 'F153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The 'F153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$
$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

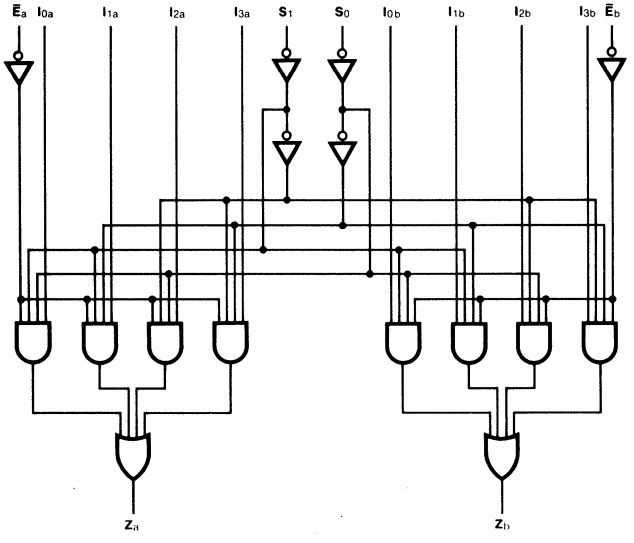
The 'F153 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'F153 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	DESCRIPTION	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		12	20	mA	V_{CC} = Max, V_{IN} = Gnd

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

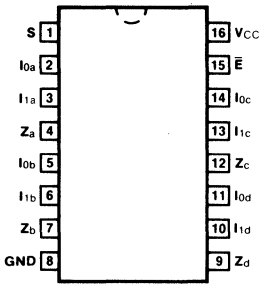
SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.0	9.5	13					ns	2-17
t_{PHL}	S_n to Z_n	3.0	8.0	10						2-23
t_{PLH}	Propagation Delay	3.0	8.0	12					ns	2-17
t_{PHL}	$\overline{E}_n$ to Z_n	3.0	7.5	12						2-18
t_{PLH}	Propagation Delay	2.0	5.0	8.0					ns	2-17
t_{PHL}	I_n to Z_n	2.0	4.5	6.5						2-19

4

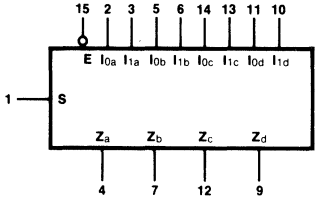
54F/74F157

QUAD 2-INPUT MULTIPLEXER

CONNECTION DIAGRAM



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

DESCRIPTION — The 'F157 is a high speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The 'F157 can also be used to generate any four of the 16 different functions to two variables.

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	74F157PC		9B
Ceramic DIP (D)	74F157DC	54F157DM	6B
Flatpak (F)	74F157FC	54F157FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
I_{0a} — I_{0d}	Source 0 Data Inputs	0.5/0.375
I_{1a} — I_{1d}	Source 1 Data Inputs	0.5/0.375
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
S	Select Input	0.5/0.375
Z_a — Z_d	Outputs	25/12.5

FUNCTIONAL DESCRIPTION — The 'F157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The 'F157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \qquad Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \qquad Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

A common use of the 'F157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'F157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

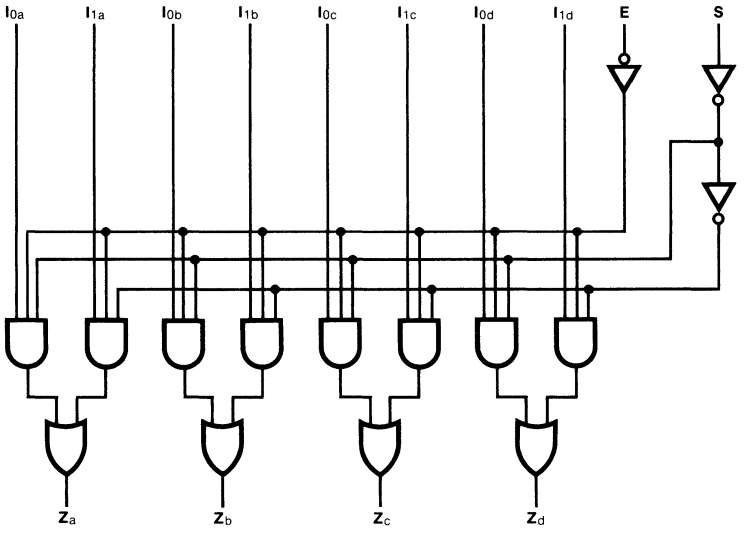
4

TRUTH TABLE

INPUTS				OUTPUT
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		14	23	mA	V_{CC} = Max, All Inputs = 4.5 V

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

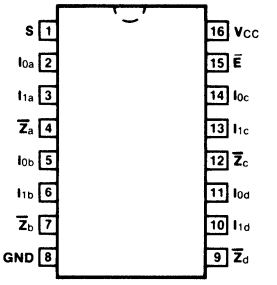
SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S to Z_n	4.0 3.0	8.5 6.0	13 9.0					ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	2.0 2.0	6.5 4.5	8.0 7.0					ns	2-17 2-18
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	2.0 2.0	4.5 3.5	6.0 4.5					ns	2-17 2-19

54F/74F158

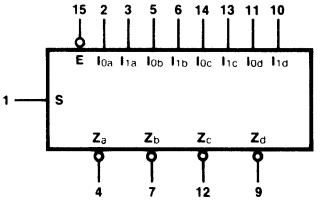
QUAD 2-INPUT MULTIPLEXER

DESCRIPTION — The 'F158 is a high speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The 'F158 can also generate any four of the 16 different functions of two variables.

CONNECTION DIAGRAM



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	74F158PC		9B
Ceramic DIP (D)	74F158DC	54F158DM	6B
Flatpak (F)	74F158FC	54F158FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$I_{0a} - I_{0d}$	Source 0 Data Inputs	0.5/0.375
$I_{1a} - I_{1d}$	Source 1 Data Inputs	0.5/0.375
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
S	Select Input	0.5/0.375
$\overline{Z}_a - \overline{Z}_d$	Inverted Outputs	25/12.5

TRUTH TABLE

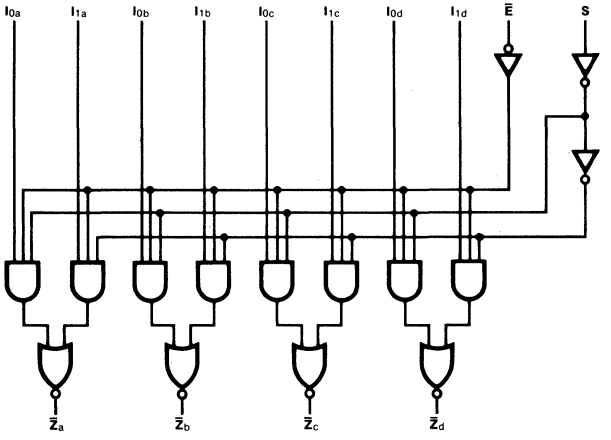
INPUTS				OUTPUTS
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

FUNCTIONAL DESCRIPTION — The 'F158 is a quad 2-input multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ($\overline{E}$) is a active LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs. The 'F158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

A common use of the 'F158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'F158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		10		mA	V_{CC} = Max*

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25° C V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S to $\overline{Z}$		6.3 6.2						ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$		4.6 4.5						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$		2.9 2.8						ns	2-17 2-18

*I_{CC} measured with outputs open and 4.5 V applied to all inputs.

54F/74F160 • 54F/74F162

SYNCHRONOUS PRESETTABLE BCD DECADE COUNTER

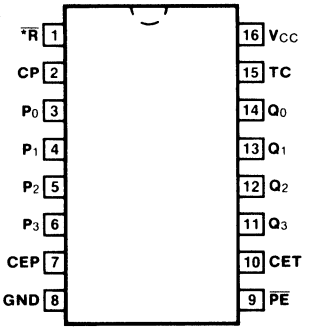
DESCRIPTION — The 'F160 and 'F162 are high speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'F160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'F162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

- **SYNCHRONOUS COUNTING AND LOADING**
- **HIGH SPEED SYNCHRONOUS EXPANSION**
- **TYPICAL COUNT RATE OF 120 MHz**

ORDERING CODE: See Section 5

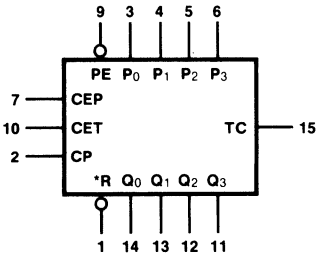
PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F160PC, 74F162PC		9B
Ceramic DIP (D)	74F160DC, 74F162DC	54F160DM, 54F162DM	7B
Flatpak (F)	74F160FC, 74F162FC	54F160FM, 54F162FM	4L

CONNECTION DIAGRAM



*$\overline{MR}$ for '160
*$\overline{SR}$ for '162

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8
*$\overline{MR}$ for '160
*$\overline{SR}$ for '162

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
CEP	Count Enable Parallel Input	0.5/0.375
CET	Count Enable Trickle Input	0.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$ ('F160)	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
$\overline{SR}$ ('F162)	Synchronous Reset Input (Active LOW)	0.5/0.75
P_0 — P_3	Parallel Data Inputs	0.5/0.375
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.75
Q_0 — Q_3	Flip-flop Outputs	25/12.5
TC	Terminal Count Output	25/12.5

FUNCTIONAL DESCRIPTION — The 'F160 and 'F162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The 'F161 and 'F163 count modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 'F160 and 'F161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('F160 and 'F161), synchronous reset ('F162 and 'F163), parallel load, count-up and hold. Five control inputs — Master Reset ($\overline{MR}$, 'F160 and 'F161), Synchronous Reset ($\overline{SR}$, 'F162 and 'F163), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) —determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('F160, 'F161) or $\overline{SR}$ ('F162, 'F163) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'F160 — 'F163 use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

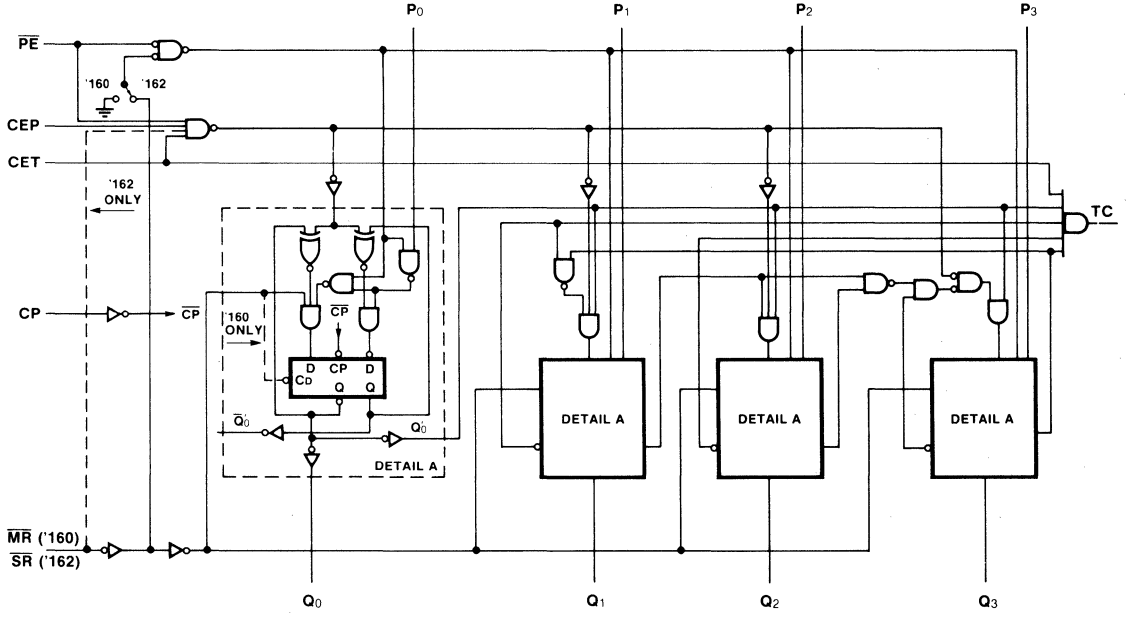
The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state (9 for the decade counters, 15 for the binary counters). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the 'F160, 'F162 decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the state diagram.

LOGIC EQUATIONS: Count Enable = CEP • CET • PE

('F160, 'F162) $TC = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3 \bullet CET$

('F161, 'F163) $TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

LOGIC DIAGRAM



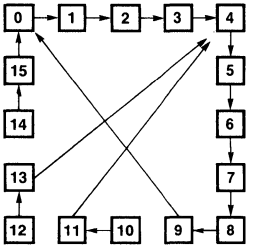
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MODE SELECT TABLE

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐¬)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the '162 and '163 only.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAM



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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		35		mA	V_{CC} = Max

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	100	120						MHz	2-17/21
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n (Load Input HIGH)		6.0 7.5						ns	2-17 2-21
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n (Load Input LOW)		6.0 7.5							
t_{PLH} t_{PHL}	Propagation Delay CP to TC		12 8.0						ns	2-17 2-21
t_{PLH} t_{PHL}	Propagation Delay CET to TC		6.5 6.5						ns	2-17 2-19
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('F160)		10						ns	2-17 2-24

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V			54F T_A, V_{CC} = MIL		74F T_A, V_{CC} = COM		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to CP	5.0 5.0							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	12 12							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW CEP or CET to CP	9.0 9.0							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW CEP or CET to CP	0 0								
t_w (H) t_w (L)	Clock Pulse Width, HIGH or LOW	5.0 5.0							ns	2-21
t_w (L)	$\overline{MR}$ Pulse Width LOW ('F160)	10							ns	2-24
t_{rec}	Recovery Time $\overline{MR}$ to CP ('F160)	6.0								

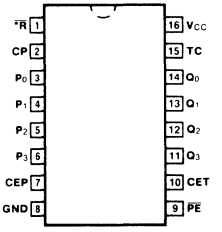
54F/74F161 • 54F/74F163

SYNCHRONOUS PRESETTABLE BINARY COUNTER

DESCRIPTION — The 'F161 and 'F163 are high speed synchronus modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'F161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'F163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. For functional description and dc specifications please refer to the 'F160 data sheet.

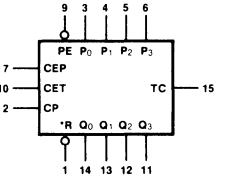
- **SYNCHRONOUS COUNTING AND LOADING**
- **HIGH SPEED SYNCHRONOUS EXPANSION**
- **TYPICAL COUNT FREQUENCY OF 120 MHz**

CONNECTION DIAGRAM



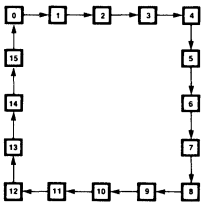
*$\overline{MR}$ for '161
*$\overline{SR}$ for '163

LOGIC SYMBOL



*$\overline{MR}$ for '161 V_{CC} = Pin 16
*$\overline{SR}$ for '163 Gnd = Pin 8

STATE DIAGRAM



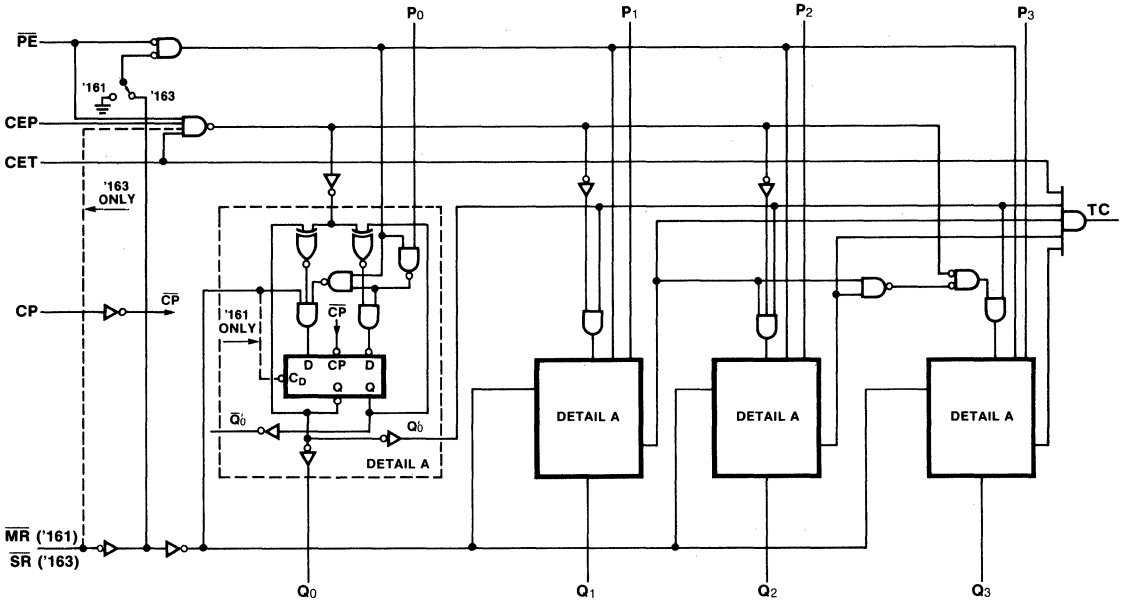
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 ±5%, T_A = 0°C to +70°C	V_{CC} = + 5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F161PC, 74F163PC		9B
Ceramic DIP (D)	74F161DC, 74F163DC	54F161DM, 54F163DM	7B
Flatpak (F)	74F161FC, 74F163FC	54F161FM, 54F163FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
CEP	Count Enable Parallel Input	0.5/0.375
CET	Count Enable Trickle Input	0.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$ ('F161)	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
$\overline{SR}$ ('F163)	Synchronous Reset Input (Active LOW)	0.5/0.75
$P_0 - P_3$	Parallel Data Inputs	0.5/0.375
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.75
$Q_0 - Q_3$	Flip-flop Outputs	25/12.5
TC	Terminal Count Output	25/12.5

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	100	120						MHz	2-17/21
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n (Load Input HIGH)		6.0 7.5						ns	2-17 2-21
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n (Load Input LOW)		6.0 7.5							
t_{PLH} t_{PHL}	Propagation Delay CP to TC		12 8.0						ns	2-17 2-21
t_{PLH} t_{PHL}	Propagation Delay CET to TC		6.5 6.5						ns	2-17 2-19
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('F161)		10						ns	2-17 2-24

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V			54F T_A, V_{CC} = MIL		74F T_A, V_{CC} = COM		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to CP	5.0 5.0							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	12 12							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW CEP or CET to CP	9.0 9.0							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW CEP or CET to CP	0 0								
t_w (H) t_w (L)	Clock Pulse Width, HIGH or LOW	5.0 5.0							ns	2-21
t_w (L)	$\overline{MR}$ Pulse Width LOW ('F161)	10							ns	2-24
t_{rec}	Recovery Time $\overline{MR}$ to CP ('F161)	6.0								

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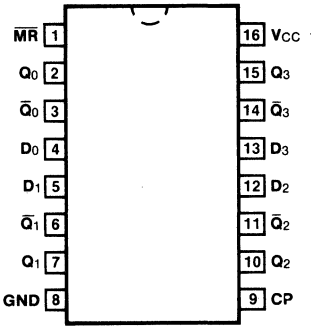
54F/74F175

QUAD D FLIP-FLOP

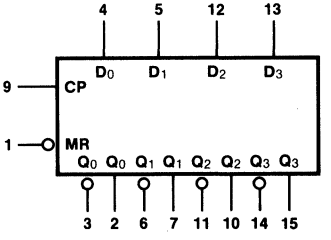
DESCRIPTION — The 'F175 is a high speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **ASYNCHRONOUS COMMON RESET**
- **TRUE AND COMPLEMENT OUTPUT**

CONNECTION DIAGRAM



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F175PC		9B
Ceramic DIP (D)	74F175DC	54F175DM	6B
Flatpak (F)	74F175FC	54F175FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$D_0 - D_3$	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Master Reset Input (Active LOW)	0.5/0.375
$Q_0 - Q_3$	True Outputs	25/12.5
$\overline{Q}_0 - \overline{Q}_3$	Complement Outputs	25/12.5

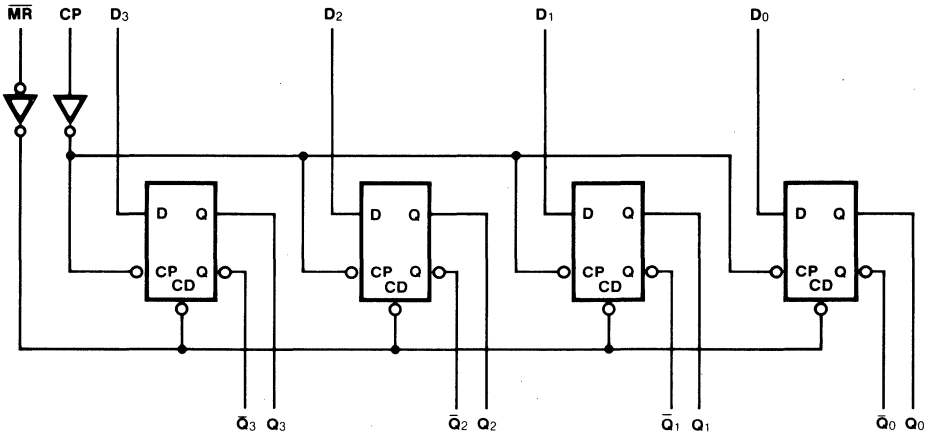
FUNCTIONAL DESCRIPTION — The 'F175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The 'F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

TRUTH TABLE

INPUTS	OUTPUTS
@ t_n, $\overline{MR}$ = H	@ t_{n+1}
D_n	Q_n $\overline{Q}_n$
L	L H
H	H L

t_n = Bit time before clock positive-going transition
t_{n+1} = Bit time after clock positive-going transition
H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		21		mA	V_{CC} = Max D_n = $\overline{MR}$ = 4.5 V CP = ⎍

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	110	150						MHz	2-17/21
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		6.1 6.3						ns	2-17 2-21
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n		7.2						ns	2-17 2-24
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$		6.4						ns	2-17 2-24

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V			54F T_A, V_{CC} = MIL		74F T_A, V_{CC} = COM		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to CP	3.0 3.0							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to CP	2.0 2.0								
t_w (H)	CP Pulse Width HIGH	4.5							ns	2-21
t_w (L)	$\overline{MR}$ Pulse Width LOW	5.0							ns	2-24
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3							ns	2-24

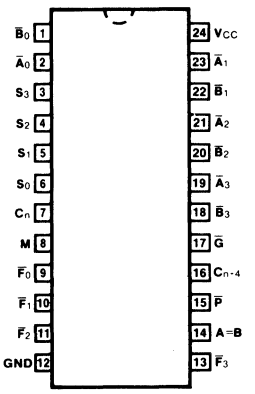
54F/74F181

4-BIT ARITHMETIC LOGIC UNIT

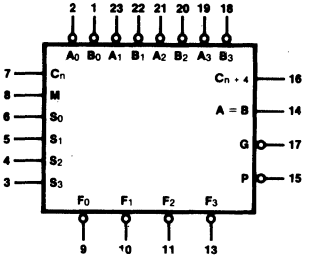
DESCRIPTION — The '181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

- **PROVIDES 16 ARITHMETIC OPERATIONS**
  ADD, SUBTRACT, COMPARE, DOUBLE, PLUS
  TWELVE OTHER ARITHMETIC OPERATIONS
- **PROVIDES ALL 16 LOGIC OPERATIONS OF TWO VARIABLES**
  EXCLUSIVE-OR, COMPARE, AND, NAND, OR, NOR,
  PLUS TEN OTHER LOGIC OPERATIONS
- **FULL LOOKAHEAD FOR HIGH SPEED ARITHMETIC**
  OPERATION ON LONG WORDS

CONNECTION DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F181PC		9N
Ceramic DIP (D)	74F181DC	54F181DM	6N
Flatpak (F)	74F181FC	54F181FM	4M

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$\overline{A}_0 - \overline{A}_3$	Operand Inputs (Active LOW)	0.5/1.125
$\overline{B}_0 - \overline{B}_3$	Operand Inputs (Active LOW)	0.5/1.125
$S_0 - S_3$	Function Select Inputs	0.5/1.50
M	Mode Control Input	0.5/0.375
C_n	Carry Input	0.5/1.875
$\overline{F}_0 - \overline{F}_3$	Function Outputs (Active LOW)	25/12.5
A = B	Comparator Output	OC*/12.5
$\overline{G}$	Carry Generate Output (Active LOW)	25/12.5
$\overline{P}$	Carry Propagate Output (Active LOW)	25/12.5
C_{n+4}	Carry Output	25/12.5

*OC — Open Collector

FUNCTIONAL DESCRIPTION — The 'F181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0 — S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the ADD mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the SUBTRACT mode, $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for each group of four 'F181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means $\overline{\text{borrow}}$; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

FUNCTION TABLE

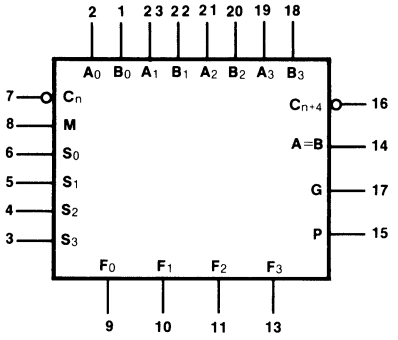
MODE SELECT INPUTS				ACTIVE LOW OPERANDS & F_n OUTPUTS		ACTIVE HIGH OPERANDS & F_n OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
L	L	H	L	$\overline{A+B}$	A$\overline{B}$ minus 1	$\overline{AB}$	A + $\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A + $\overline{B}$)	$\overline{A\overline{B}}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	A $\oplus$ B	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	A$\overline{B}$	AB minus 1
H	L	L	L	$\overline{AB}$	A plus (A + B)	$\overline{A+B}$	A plus AB
H	L	L	H	A $\oplus$ B	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A*	Logic 1	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H	H	H	L	AB	A$\overline{B}$ minus A	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A	A	A minus 1

*each bit is shifted to the next more significant position

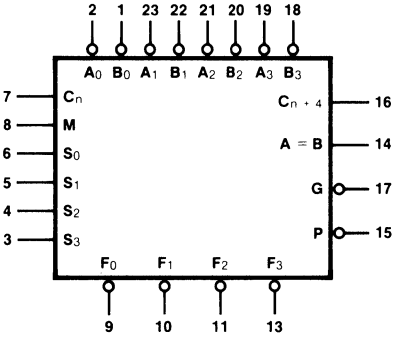
**arithmetic operations expressed in 2s complement notation

LOGIC SYMBOLS

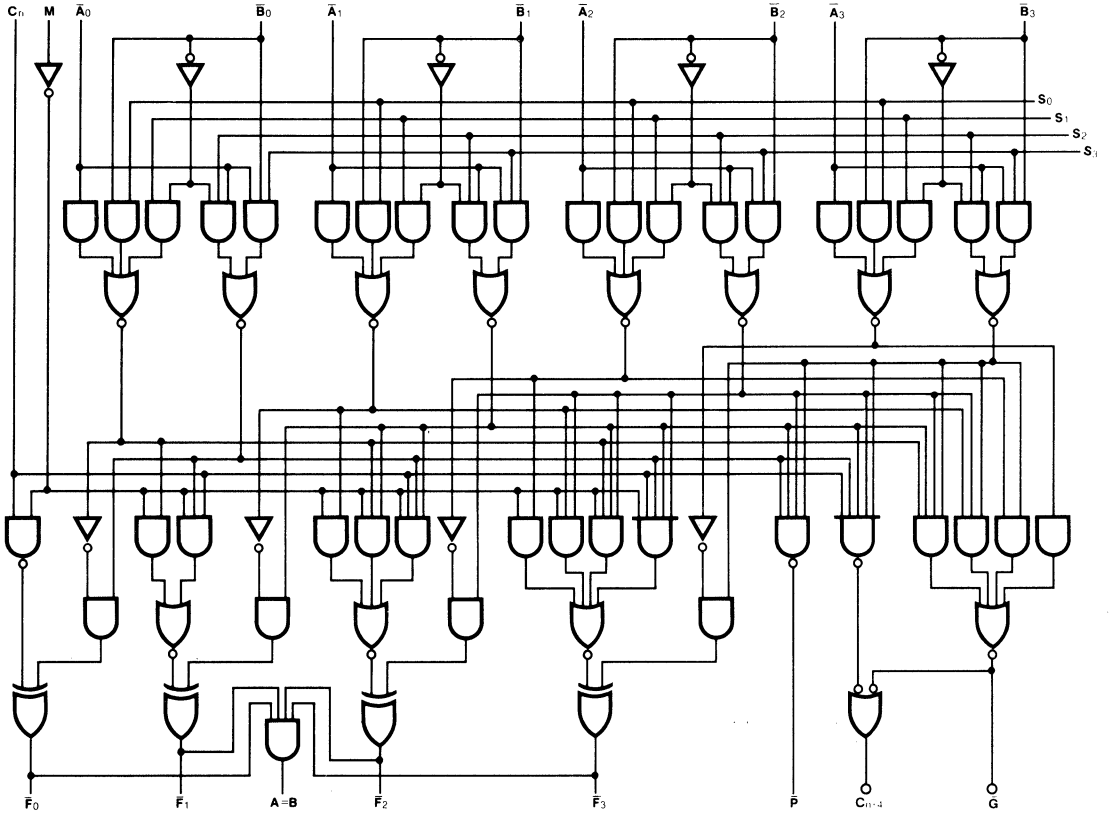
ACTIVE HIGH OPERANDS



ACTIVE LOW OPERANDS



LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{OH}	Output HIGH Current, A = B			250	μA	$V_{OH} = V_{CC}$ = Min
I_{CC}	Power Supply Current		39	60	mA	V_{CC} = Max $\overline{B}_n$, C_n = Gnd S_n, M, $\overline{A}_n$ = 4.5 V
			39	60	mA	V_{CC} = Max $\overline{A}_n$, B_n, C_n = Gnd M, S_n = 4.5 V

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 2 for waveforms and load configurations)

SYMBOL	PROPAGATION DELAY		54F/74F C_L = 15 pF			UNITS	CONDITIONS
	PATH	MODE	Min	Typ	Max		
t_{PLH} t_{PHL}	C_n to C_{n+4}		2.0 2.0	5.0 5.0	6.5 6.5	ns	Figs 2-17, 2-19
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to C_{n+4}	Sum	6.0 6.0	8.5 9.0	11.5 11.5	ns	Figs 2-17, 2-18
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to C_{n+4}	Dif	6.0 6.0	9.0 9.0	11.5 11.5	ns	Figs 2.-17, 2-18
t_{PLH} t_{PHL}	C_n to $\overline{F}$	Any	2.0 2.0	5.0 4.5	6.7 6.0	ns	Figs. 2-17, 2-19
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{G}$	Sum	2.0 2.0	4.0 4.0	7.0 7.0	ns	Figs. 2-17, 2-19
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{G}$	Dif	2.0 2.0	5.0 5.0	7.0 8.0	ns	Figs. 2-17, 2-18
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{P}$	Sum	2.0 2.0	4.0 4.0	6.8 7.5	ns	Figs. 2-17, 2-18
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{P}$	Dif	3.0 3.0	5.0 5.0	7.0 7.5	ns	Figs. 2-17, 2-18
t_{PLH} t_{PHL}	$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	3.0 3.0	5.5 4.5	8.0 9.0	ns	Figs. 2-17, 2-18, 2-19
t_{PLH} t_{PHL}	$\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Dif	4.0 4.0	6.0 5.0	10 10	ns	Figs. 2-17, 2-18, 2-19
t_{PLH} t_{PHL}	Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Sum	3.0 3.0	6.0 6.0	10 10	ns	Figs. 2-17, 2-18, 2-19
t_{PLH} t_{PHL}	Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Dif	3.5 3.5	7.0 7.0	11 11	ns	Figs. 2-17, 2-18, 2-19
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to $\overline{F}$	Logic	3.0 3.0	5.0 5.0	8.0 9.0	ns	Figs. 2-17, 2-18, 2-19
t_{PLH} t_{PHL}	$\overline{A}$ or $\overline{B}$ to A = B	Dif	8.0 6.0	13 10	16 12.5	ns	Figs. 2-17, 2-18, 2-19 R_L = 280 Ω to 5.0 V

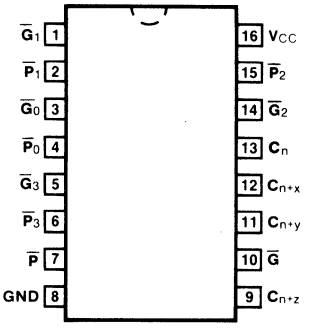
54F/74F182

CARRY LOOKAHEAD GENERATOR

DESCRIPTION — The 'F182 is a high speed carry lookahead generator. It is generally used with the 'F181, 'F381 or 2901A 4-bit arithmetic logic unit to provide high speed lookahead over word lengths of more than four bits.

- **PROVIDES LOOKAHEAD CARRIES ACROSS A GROUP OF FOUR ALU'S**
- **MULTI-LEVEL LOOKAHEAD FOR HIGH SPEED ARITHMETIC OPERATION OVER LONG WORD LENGTHS**

CONNECTION DIAGRAM



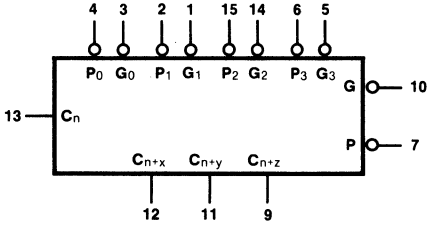
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F182PC		9B
Ceramic DIP (D)	74F182DC	54F182DM	7B
Flatpak (F)	74F182FC	54F182FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
C_n	Carry Input	0.5/0.375
$\overline{G}_0$, $\overline{G}_2$	Carry Generate Inputs (Active LOW)	0.5/2.625
$\overline{G}_1$	Carry Generate Input (Active LOW)	0.5/3.0
$\overline{G}_3$	Carry Generate Input (Active LOW)	0.5/1.5
$\overline{P}_0$, $\overline{P}_1$	Carry Propagate Inputs (Active LOW)	0.5/1.5
$\overline{P}_2$	Carry Propagate Input (Active LOW)	0.5/1.125
$\overline{P}_3$	Carry Propagate Input (Active LOW)	0.5/1.75
C_{n+x} — C_{n+z}	Carry Outputs	25/12.5
$\overline{G}$	Carry Generate Output (Active LOW)	25/12.5
$\overline{P}$	Carry Propagate Output (Active LOW)	25/12.5

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The 'F182 carry lookahead generator accepts up to four pairs of active LOW Carry Propagate ($\overline{P}_0 - \overline{P}_3$) and Carry Generate ($\overline{G}_0 - \overline{G}_3$) signals and an active HIGH Carry input (C_n) and provides anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The 'F182 also has active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead. The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

Also, the 'F182 can be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections *(Figure a)* to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last 'F181 or 'F381.

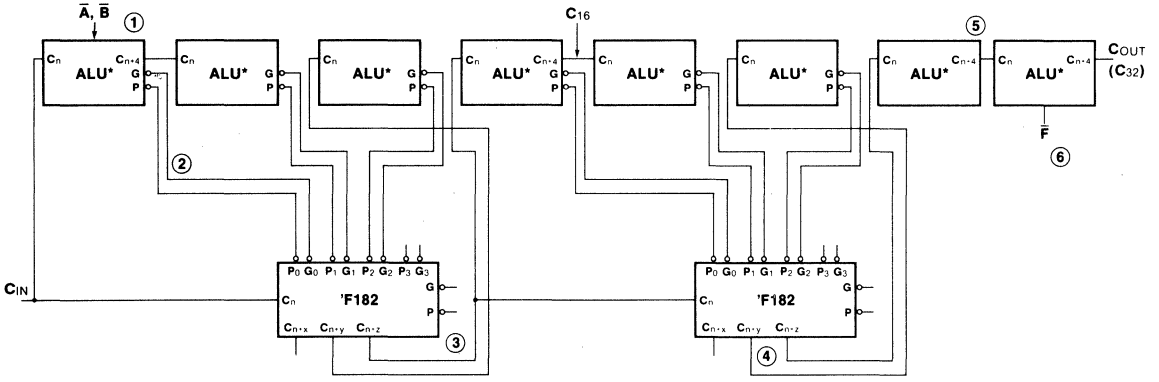
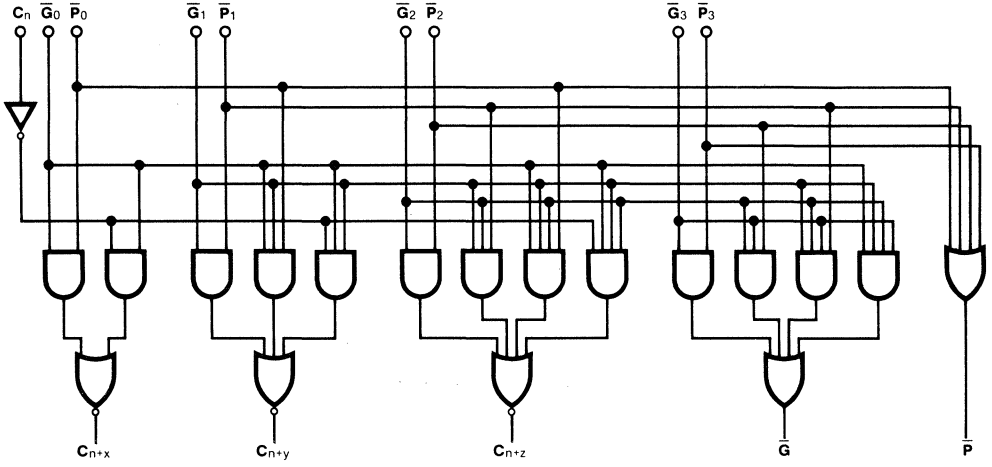


Fig. a 32-Bit ALU with Ripple Carry Between 16-Bit Lookahead ALUs

LOGIC DIAGRAM



TRUTH TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CCH}	Power Supply Current (All Outputs HIGH)		11		mA	V_{CC} = Max; $\overline{P}_3$, $\overline{G}_3$ = 4.5 V All Other Inputs = Gnd
I_{CCL}	Power Supply Current (All Outputs LOW)		19		mA	V_{CC} = Max; $\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$ = 4.5 V All Other Inputs = Gnd

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+x}, C_{n+y}, C_{n+z}		4.6 4.5						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_0$, $\overline{P}_1$ or $\overline{P}_2$ to C_{n+x}, C_{n+y}, C_{n+z}		2.9 2.8						ns	2-17 2-18
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_0$, $\overline{G}_1$ or $\overline{G}_2$ to C_{n+x}, C_{n+y}, C_{n+z}		2.9 2.8						ns	2-17 2-18
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_1$, $\overline{P}_2$ or $\overline{P}_3$ to $\overline{G}$		4.5 4.3						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay $\overline{G}_n$ to $\overline{G}$		4.5 4.3						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay $\overline{P}_n$ to $\overline{P}$		5.0 4.8						ns	2-17 2-19

54F/74F189

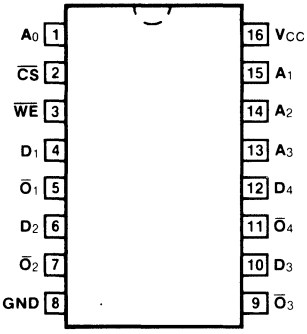
64-BIT RANDOM ACCESS MEMORY

(With 3-State Outputs)

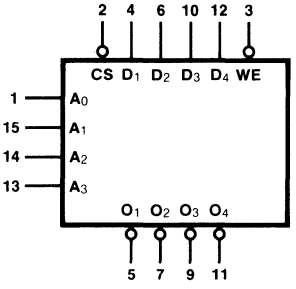
DESCRIPTION — The 'F189 ia a high speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

- **3-STATE OUTPUTS FOR DATA BUS APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**

CONNECTION DIAGRAM



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	74F189PC		9B
Ceramic DIP (D)	74F189DC	54F189DM	6B
Flatpak (F)	74F189FC	54F189FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

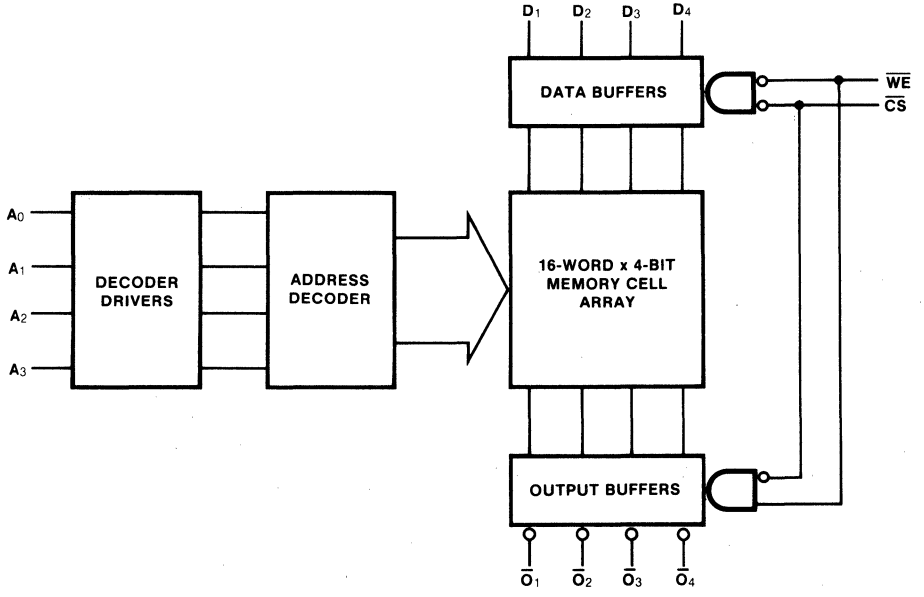
PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.75
$\overline{WE}$	Write Enable Input (Active LOW)	0.5/0.75
$D_1 - D_4$	Data Inputs	0.5/0.375
$\overline{O}_1 - \overline{O}_4$	Inverted Data Outputs	25/12.5

FUNCTION TABLE

INPUTS		OPERATION	CONDITION OF OUTPUTS
$\overline{CS}$	$\overline{WE}$		
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		43		mA	V_{CC} = Max; $\overline{WE}$, $\overline{CS}$, Gnd

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Access Time, HIGH or LOW A_n to $\overline{O}_n$		20 20						ns	2-17 2-23
t_{PZH} t_{PZL}	Access Time, HIGH or LOW $\overline{CS}$ to $\overline{O}_n$		12 12						ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW $\overline{CS}$ to $\overline{O}_n$		12 12						ns	2-25 2-26 2-27
t_{PZH} t_{PZL}	Access Time, HIGH or LOW $\overline{WE}$ to $\overline{O}_n$		12 12						ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Disable Time, HIGH or LOW $\overline{WE}$ to $\overline{O}_n$		12 12						ns	2-25 2-26 2-27

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V			54F T_A, V_{CC} = MIL		74F T_A, V_{CC} = COM		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW A_n to $\overline{WE}$	0 0							ns	2-30
t_h (H) t_h (L)	Hold Time, HIGH or LOW A_n to $\overline{WE}$	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to $\overline{WE}$	20 20							ns	2-28
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to $\overline{WE}$	0 0								
t_s (L)	Setup Time, LOW $\overline{CS}$ to $\overline{WE}$								ns	2-28
t_h (L)	Hold Time, LOW $\overline{CS}$ to $\overline{WE}$								ns	2-28
t_w (L)	$\overline{WE}$ Pulse Width LOW	20							ns	2-29

54F/74F190

UP/DOWN DECADE COUNTER

(With Preset and Ripple Clock)

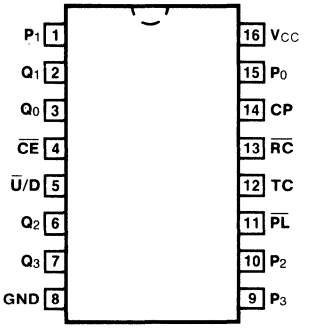
DESCRIPTION — The 'F190 is a reversible BCD (8421) decade counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F190 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- **HIGH SPEED — 70 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS PARALLEL LOAD**
- **CASCADABLE**

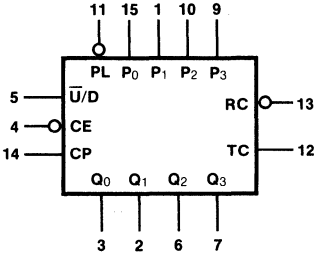
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F190PC		9B
Ceramic DIP (D)	74F190DC	54F190DM	7B
Flatpak (F)	74F190FC	54F190FM	4L

CONNECTION DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

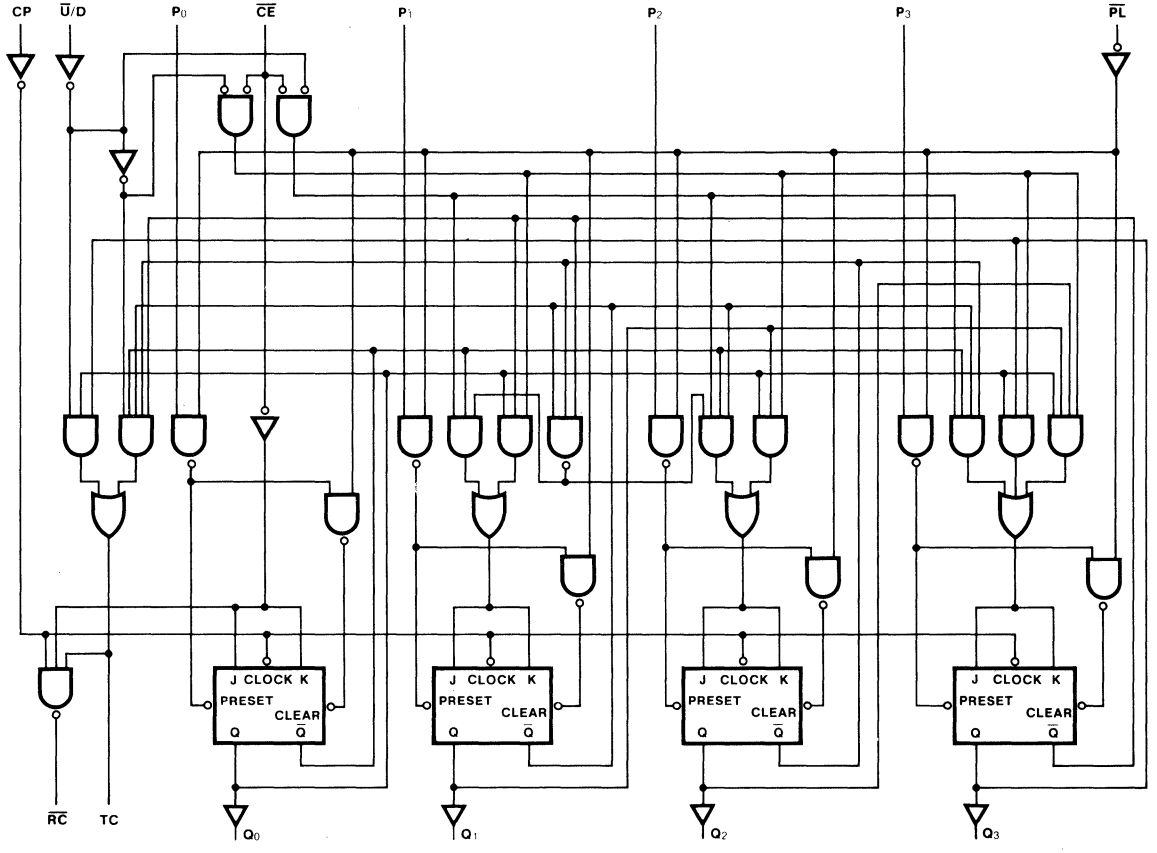
PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$\overline{CE}$	Count Enable Input (Active LOW)	0.5/1.125
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$P_0 - P_0$	Parallel Data Inputs	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.375
$\overline{U}/D$	Up/Down Count Control Input	0.5/0.375
$Q_0 - Q_3$	Flip-flop Outputs	25/12.5
$\overline{RC}$	Ripple Clock Output (Active LOW)	25/12.5
TC	Terminal Count Output (Active HIGH)	25/12.5

FUNCTIONAL DESCRIPTION — The 'F190 is a synchronous up/down BCD decade counter containing four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations. It has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs ($P_0 - P_3$) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table. A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 9 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes. The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters. For a discussion and illustrations of the various methods of implementing multistage counters, please see the 'F191 data sheet.

4

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⎍	Count Up
H	L	H	⎍	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

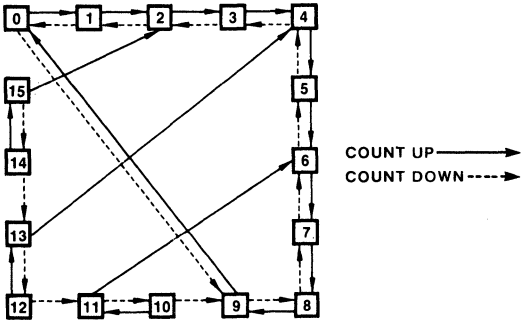
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

RC TRUTH TABLE

INPUTS			OUTPUT
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⎍	⎍
H	X	X	H
X	L	X	H

*TC is generated internally

STATE DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		38		mA	V_{CC} = Max

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	90	130						MHz	2-17/21
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		4.5 5.5						ns	2-17 2-21
t_{PLH} t_{PHL}	Propagation Delay CP to TC		6.5 8.5							
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$		4.5 4.0						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$		3.6 3.5							
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$		10 8.0						ns	2-17 Fig.d*
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to TC		5.0 5.5							
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		3.6 6.3						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n, $\overline{RC}$ or TC		5.7 6.2						ns	2-17 2-24

*shown on 'F191 data sheet.

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = MIL		T_A, V_{CC} = COM			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to $\overline{PL}$	5.0 5.0							ns	2-28
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.0 3.0								
t_s (L)	Setup Time LOW $\overline{CE}$ to CP	10							ns	2-20
t_h (L)	Hold Time LOW $\overline{CE}$ to CP	0								
t_w (L)	$\overline{PL}$ Pulse Width LOW	5.0							ns	2-24
t_w (L)	CP Pulse Width LOW	5.5							ns	2-21
t_{rec}	Recovery Time $\overline{PL}$ to CP	6.0							ns	2-24

4

54F/74F191

UP/DOWN BINARY COUNTER

(With Preset and Ripple Clock)

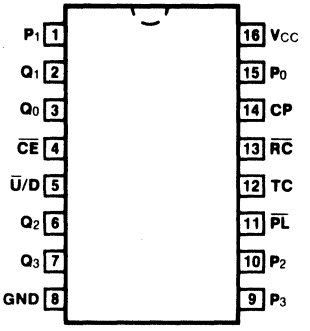
DESCRIPTION — The 'F191 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

- **HIGH SPEED — 130 MHz TYPICAL COUNT FREQUENCY**
- **SYNCHRONOUS COUNTING**
- **ASYNCHRONOUS PARALLEL LOAD**
- **CASCADABLE**

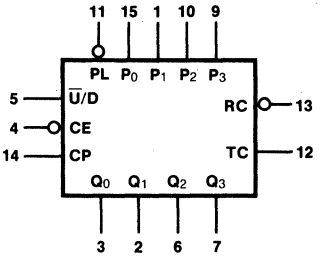
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F191PC		9B
Ceramic DIP (D)	74F191DC	54F191DM	7B
Flatpak (F)	74F191FC	54F191FM	4L

CONNECTION DIAGRAM



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F HIGH/LOW
$\overline{CE}$	Count Enable Input (Active LOW)	0.5/1.125
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$P_0 - P_3$	Parallel Data Inputs	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.375
$\overline{U}/D$	Up/Down Count Control Input	0.5/0.375
$Q_0 - Q_3$	Flip-flop Outputs	25/12.5
$\overline{RC}$	Ripple Clock Output (Active LOW)	25/12.5
TC	Terminal Count Output (Active HIGH)	25/12.5

FUNCTIONAL DESCRIPTION — The 'F191 is a synchronous up/down 4-bit binary counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Data inputs ($P_0 - P_3$) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches maximum (15 for the 'F191) in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The RC output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, the $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in *Figures a* and *b*. In *Figure a*, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the RC Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages in shown in *Figure b*. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the RC output of any package goes HIGH shortly after its CP input goes HIGH.

The configuration shown in *Figure c* avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of *Figures a* and *b* doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

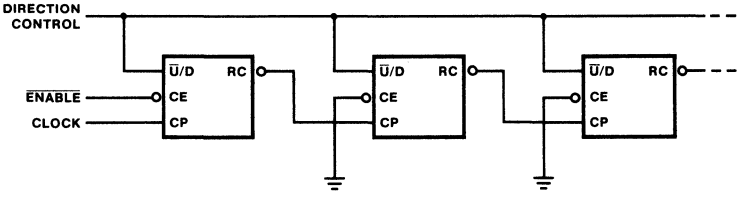


Fig. a N-Stage Counter Using Ripple Clock

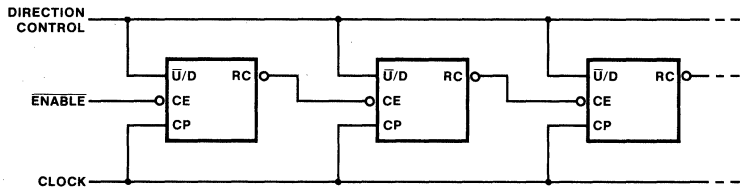


Fig. b Synchronous N-Stage Counter Using Ripple Carry/Borrow

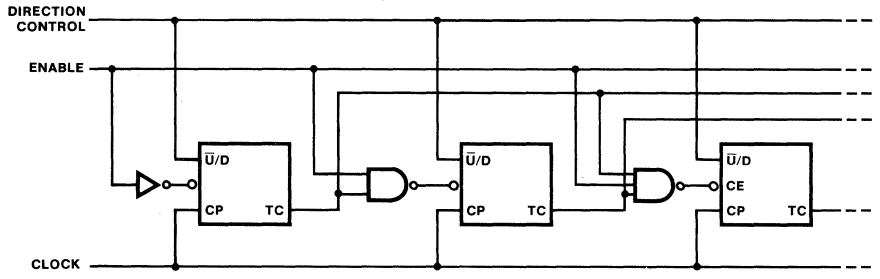


Fig. c Synchronous N-Stage Counter with Parallel Gated Carry/Borrow

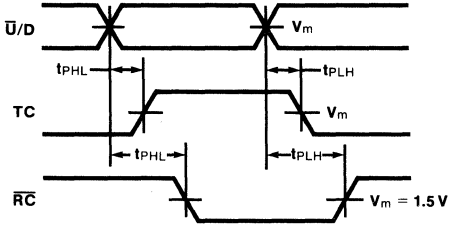


Figure d

MODE SELECT TABLE

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

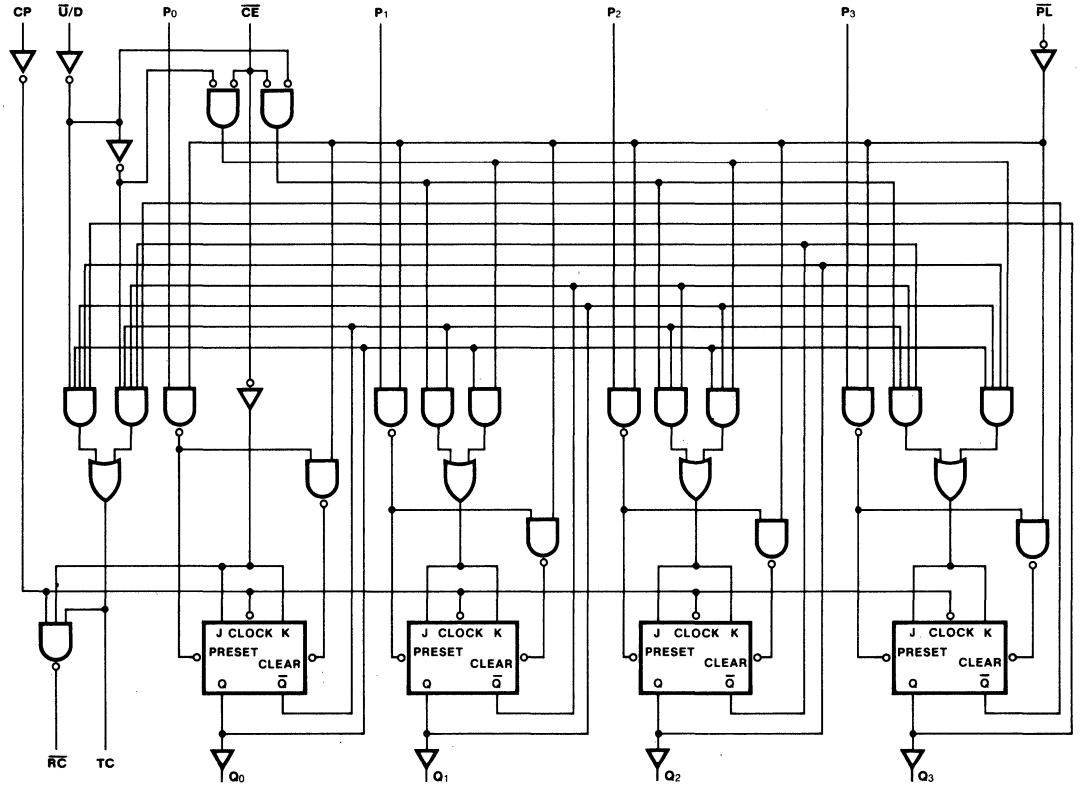
RC TRUTH TABLE

INPUTS			OUTPUT
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⌐	⌐
H	X	X	H
X	L	X	H

*TC is generated internally

4

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		38	55	mA	V_{CC} = Max

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	90	130						MHz	2-17/21
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	2.0 2.0	4.5 5.5	8.0 9.0					ns	2-17 2-21
t_{PLH} t_{PHL}	Propagation Delay CP to TC	3.0 4.0	6.5 8.5	10 12						
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$	2.0 2.0	4.5 4.0	7.0 7.0					ns	2-17 Fig. d
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	2.0 2.0	3.6 3.5	6.0 6.0						
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	6.0 4.0	10 8.0	16 12					ns	2-18 2-19
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to TC	2.0 2.0	5.0 5.5	9.0 9.0						
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n	2.0 3.0	3.6 6.3	6.0 10					ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	2.0 3.0	5.7 6.2	9.0 10					ns	2-17 2-24

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = MIL		T_A, V_{CC} = COM			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to $\overline{PL}$	5.0 5.0							ns	2-28
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.0 3.0								
t_s (L)	Setup Time LOW $\overline{CE}$ to CP	10							ns	2-20
t_h (L)	Hold Time LOW $\overline{CE}$ to CP	0								
t_w (L)	$\overline{PL}$ Pulse Width, LOW	5.0							ns	2-24
t_w (L)	CP Pulse Width, LOW	5.5							ns	2-21
t_{rec}	Recovery Time $\overline{PL}$ to CP	6.0							ns	2-24

54F/74F192

UP/DOWN DECADE COUNTER

(With Separate Up/Down Clocks)

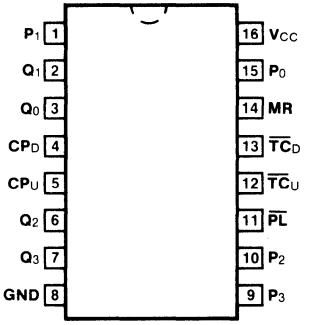
DESCRIPTION — The 'F192 is an up/down BCD decade (8421) counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

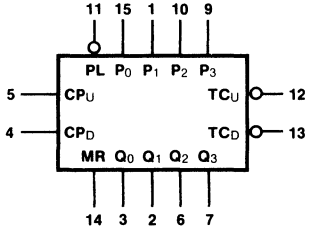
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F192PC		9B
Ceramic DIP (D)	74F192DC	54F192DM	6B
Flatpak (F)	74F192FC	54F192FM	4L

CONNECTION DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
CP_U	Count Up Clock Input (Active Rising Edge)	0.5/0.75
CP_D	Count Down Clock Input (Active Rising Edge)	0.5/0.75
MR	Asynchronous Master Reset Input (Active HIGH)	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.375
$P_0 - P_3$	Parallel Data Inputs	0.5/0.375
$Q_0 - Q_3$	Flip-flop Outputs	25/12.5
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)	25/12.5
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)	25/12.5

FUNCTIONAL DESCRIPTION — The 'F192 and 'F193 are asynchronously presettable decade and 4-bit binary synchronous up/down (reversible) counters. The operating modes of the 'F192 decade counter and the 'F193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagram. Each circuit contains four edge-triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

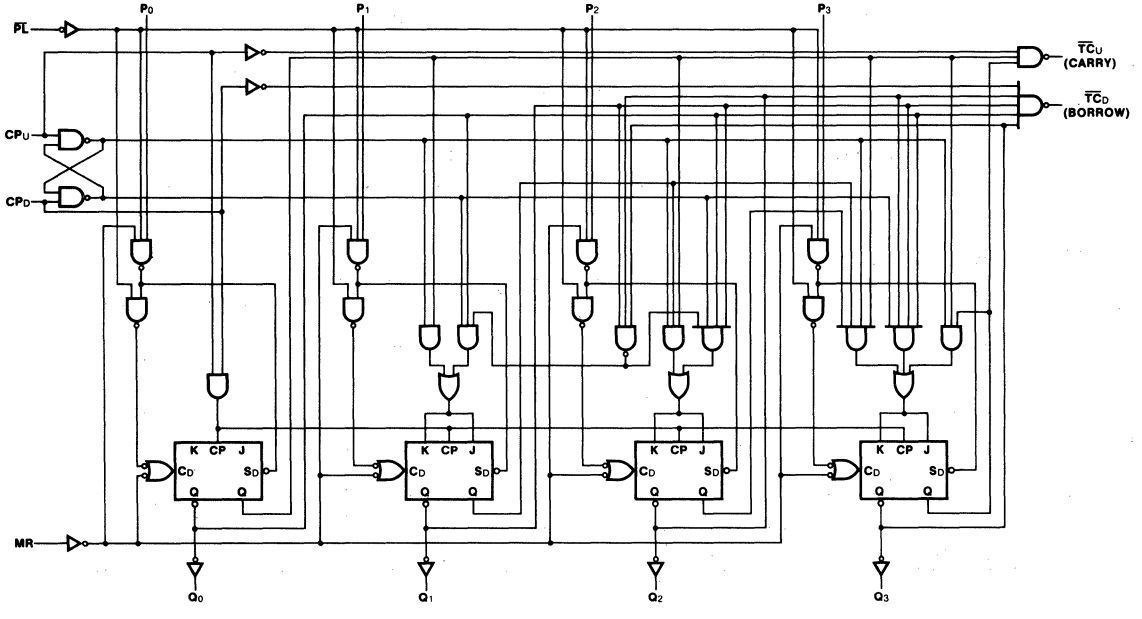
A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the 'F192, 15 for the 'F193), the next HIGH-to-LOW transition of the Count up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays, Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q_0 \bullet Q_3 \bullet \overline{CP}_U$$
$$\overline{TC}_D = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$$

Each circuit has an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input ($P_0 - P_3$) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

LOGIC DIAGRAM



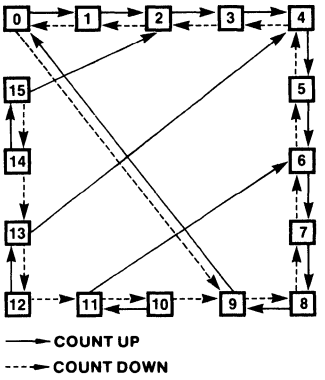
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAM



4

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		35		mA	V_{CC} = Max

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	90	130						MHz	2-17/21
t_{PLH} t_{PHL}	Propagation Delay CP_U to $\overline{TC}_U$		5.0 4.5						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay CP_D to $\overline{TC}_D$		5.0 4.5							
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n		4.5 5.5						ns	2-17 2-21
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		3.6 6.3						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		5.7 6.2						ns	2-17 2-23
t_{PHL}	Propagation Delay MR to Q_n		5.2						ns	2-17 2-24
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$		7.5							
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$		5.5							

AC CHARACTERISTICS (Cont'd): See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$		8.5						ns	2-17, 2-24
t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC}_D$		8.5						ns	2-17, 2-24
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$		8.5 6.7						ns	2-17 2-23

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = MIL		T_A, V_{CC} = COM			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to $\overline{PL}$		5.0 5.0						ns	2-28
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to $\overline{PL}$		3.0 3.0						ns	2-28
t_w (L)	$\overline{PL}$ Pulse Width, LOW		5.0						ns	2-24
t_w (L)	CP_U Pulse Width LOW		5.5						ns	2-21
t_w (L)	CP_D Pulse Width LOW		5.5						ns	2-21
t_w (H)	MR Pulse Width HIGH		5.5						ns	2-24
t_{rec}	Recovery Time $\overline{PL}$ to CP_U or CP_D		6.0						ns	2-24
t_{rec}	Recovery Time MR to CP_U or CP_D		6.0						ns	2-24

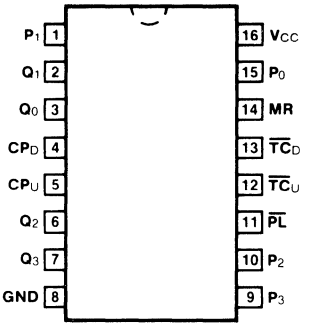
54F/74F193

UP/DOWN BINARY COUNTER

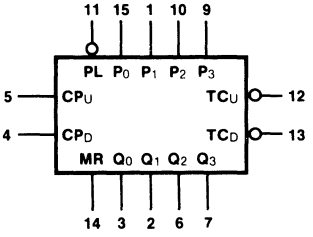
(With Separate Up/Down Clocks)

DESCRIPTION — The 'F193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs. Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks. For functional description please refer to the 'F192 data sheet.

CONNECTION DIAGRAM



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F193PC		9B
Ceramic DIP (D)	74F193DC	54F193DM	6B
Flatpak (F)	74F193FC	54F193FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

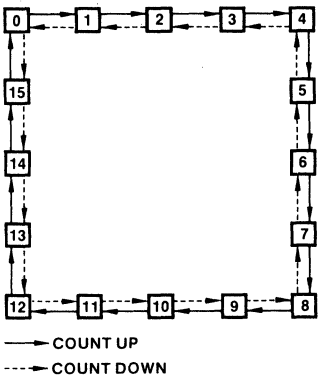
PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
CP_U	Count Up Clock Input (Active Rising Edge)	0.5/0.75
CP_D	Count Down Clock Input (Active Rising Edge)	0.5/0.75
MR	Asynchronous Master Reset Input (Active HIGH)	0.5/0.375
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)	0.5/0.375
$P_0 - P_3$	Parallel Data Inputs	0.5/0.375
$Q_0 - Q_3$	Flip-flop Outputs	25/12.5
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)	25/12.5
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)	25/12.5

MODE SELECT TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

STATE DIAGRAM

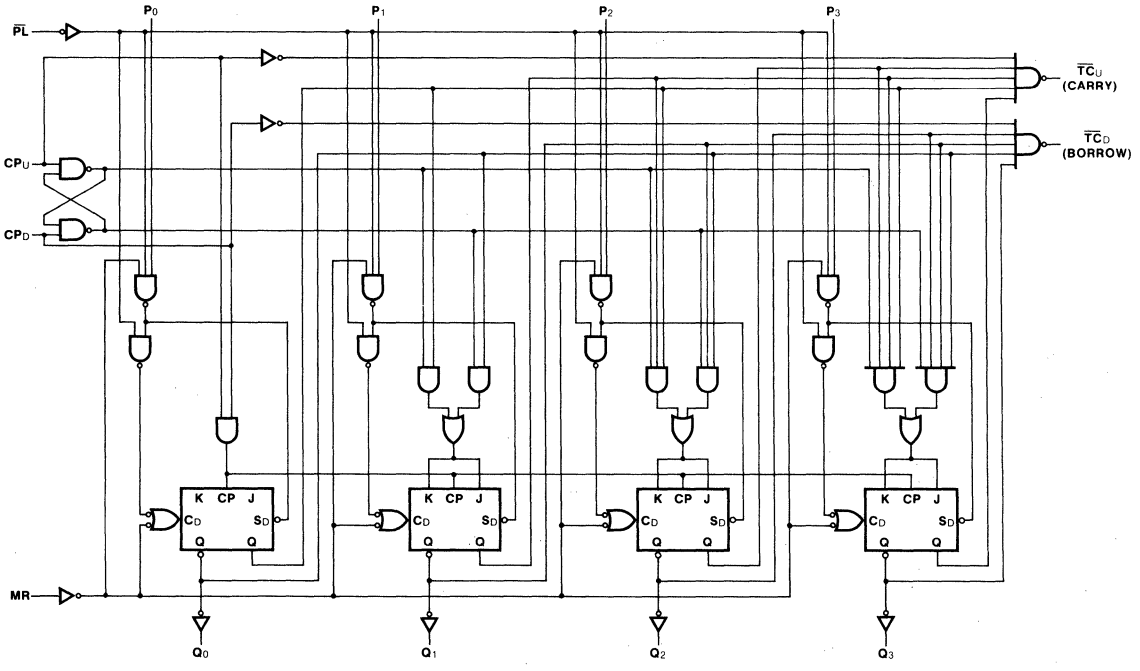


LOGIC EQUATIONS FOR TERMINAL COUNT

$$\overline{TC}_U = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$$

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		35		mA	V_{CC} = Max

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	90	130						MHz	2-17/21
t_{PLH} t_{PHL}	Propagation Delay CP_U to $\overline{TC}_U$		5.0 4.5						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay CP_D to $\overline{TC}_D$		5.0 4.5							
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n		4.5 5.5						ns	2-17 2-21
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		3.6 6.3						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		5.7 6.2						ns	2-17 2-23
t_{PHL}	Propagation Delay MR to Q_n		5.2						ns	2-17 2-24
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$		7.5							
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$		5.5							
t_{PLH}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$		8.5						ns	2-17 2-24
t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC}_D$		8.5							
t_{PLH} t_{PHL}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$		8.5 6.7						ns	2-17 2-24

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = MIL		T_A, V_{CC} = COM			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n to $\overline{PL}$	5.0 5.0							ns	2-28
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.0 3.0								
t_w (L)	$\overline{PL}$ Pulse Width, LOW	5.0							ns	2-24
t_w (L)	CP_U Pulse Width LOW	5.5							ns	2-21
t_w (L)	CP_D Pulse Width LOW	5.5								
t_w (H)	MR Pulse Width HIGH	5.5							ns	2-24
t_{rec}	Recovery Time $\overline{PL}$ to CP_U or CP_D	6.0							ns	2-24
t_{rec}	Recovery Time MR to CP_U or CP_D	6.0							ns	2-24

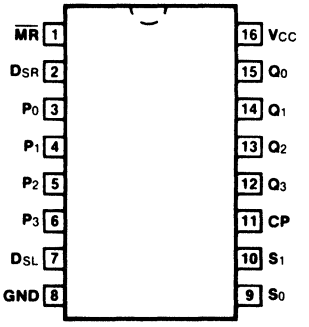
54F/74F194

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

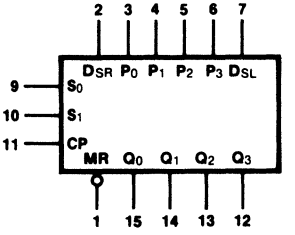
DESCRIPTION — The 'F194 is a high speed 4-bit bidirectional universal shift register. As a high speed multifunctional sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers. The 'F194 is similar in operation to the 'S195 universal shift register, with added features of shift left without external connections and hold (do nothing) modes of operation.

- **TYPICAL SHIFT FREQUENCY OF 150 MHz**
- **ASYNCHRONOUS MASTER RESET**
- **HOLD (DO NOTHING) MODE**
- **FULLY SYNCHRONOUS SERIAL OR PARALLEL DATA TRANSFERS**

CONNECTION DIAGRAM



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F194PC		9B
Ceramic DIP (D)	74F194DC	54F194DM	6B
Flatpak (F)	74F194FC	54F194FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
S_0, S_1	Mode Control Inputs	0.5/0.375
P_0 — P_3	Parallel Data Inputs	0.5/0.375
D_{SR}	Serial Data Input (Shift Right)	0.5/0.375
D_{SL}	Serial Data Input (Shift Left)	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
Q_0 — Q_3	Parallel Outputs	25/12.5

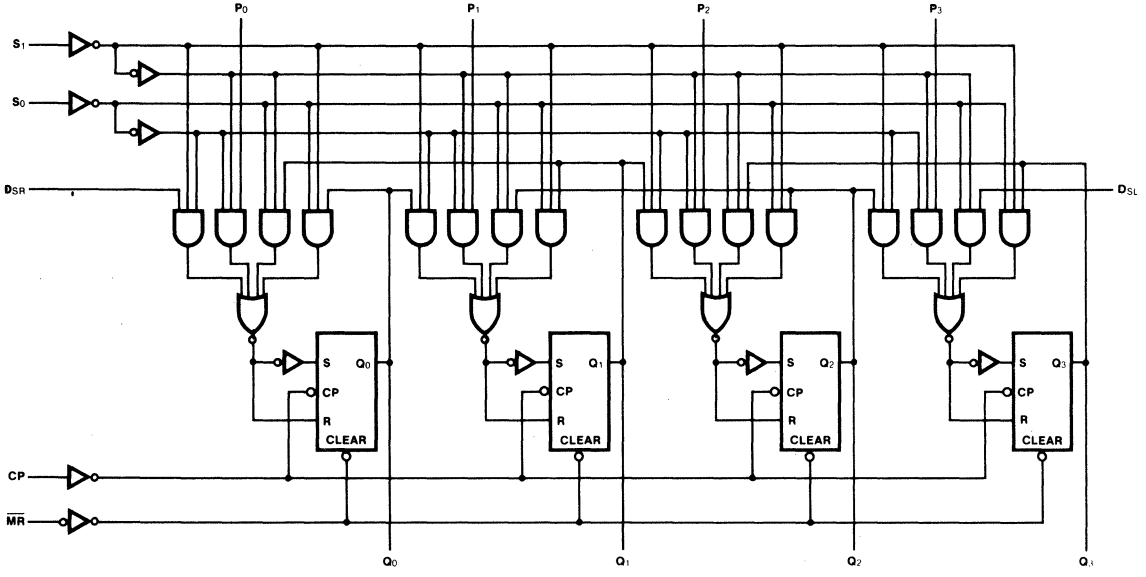
FUNCTIONAL DESCRIPTION — The 'F194 contains four edge-triggered D flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select (S_0, S_1) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data (P_0 — P_3) and Serial data (D_{SR}, D_{SL}) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset ($\overline{MR}$) overrides all other inputs and forces the outputs LOW.

MODE SELECT TABLE

OPERATING MODE	INPUTS						OUTPUTS			
	$\overline{MR}$	S_1	S_0	D_{SR}	D_{SL}	P_n	Q_0	Q_1	Q_2	Q_3
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	q_0	q_1	q_2	q_3
Shift Left	H	h	l	X	l	X	q_1	q_2	q_3	L
	H	h	l	X	h	X	q_1	q_2	q_3	H
Shift Right	H	l	h	l	X	X	L	q_0	q_1	q_2
	H	l	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	H	h	h	X	X	p_n	p_0	p_1	p_2	p_3

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		33	46	mA	V_{CC} = Max S_n, $\overline{MR}$, D_{SR}, D_{SL} = 4.5 V P_n = Gnd, CP = ⎍

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Shift Frequency	105	150						MHz	2-17/21
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	2.0 2.0	4.0 4.5	7.0 9.0					ns	2-17 2-21
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	10	13					ns	2-17 2-24

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW P_n, D_{SR} or D_{SL} to CP	4.0 4.0							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW P_n, D_{SR} or D_{SL} to CP	0 0							ns	
t_s (H) t_s (L)	Setup Time, HIGH or LOW S_n to CP	8.0 8.0							ns	
t_h (H) t_h (L)	Hold Time, HIGH or LOW S_n to CP	0 0							ns	
t_w (H)	CP Pulse Width HIGH	5.0							ns	2-21
t_w (L)	$\overline{MR}$ Pulse Width LOW	5.0							ns	2-24
t_{rec}	Recovery Time $\overline{MR}$ to CP	7.0							ns	2-24

54F/74F240 • 54F/74F241
54F/74F244

OCTAL BUFFER/LINE DRIVER

(With 3-State Outputs)

DESCRIPTION — The 'F240, 'F241 and 'F244 are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers and bus oriented transmitters/receivers which provide improved PC board density.

- **HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGINS**
- **3-STATE OUTPUTS DRIVE BUS LINES OR BUFFER MEMORY ADDRESS REGISTERS**
- **OUTPUTS SINK 64 mA**
- **15 mA SOURCE CURRENT**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

ORDERING CODE: See Section 5

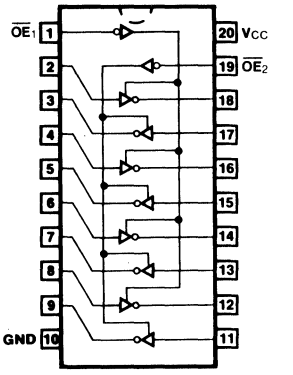
PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F240PC, 74F241PC 74F244PC		9Z
Ceramic DIP (D)	74F240DC, 74F241DC 74F244DC	54F240DM, 54F241DM 54F244DM	4E
Flatpak (F)	74F240FC, 74F241FC 74F244FC	54F240FM, 54F241FM 54F244FM	4F

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

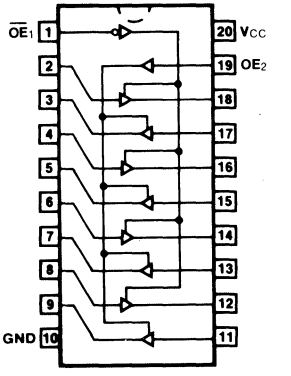
PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable (Active LOW)	0.5/0.625
OE_2	3-State Output Enable (Active HIGH)	0.5/0.625
	Inputs	0.5/1.0
	Outputs	75/40 (30)

CONNECTION DIAGRAMS

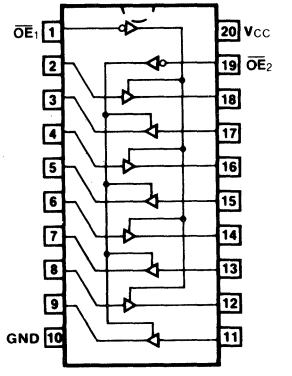
'F240



'F241



'F244



'F240

INPUTS			OUTPUT
$\overline{OE_1}$, $\overline{OE_2}$		D	
L		L	H
L		H	L
H		X	Z

'F241

INPUTS			OUTPUT
$\overline{OE_1}$	OE_2	D	
L	H	L	L
L	H	H	H
H	L	X	Z

'F244

INPUTS			OUTPUT
$\overline{OE_1}$, $\overline{OE_2}$		D	
L		L	L
L		H	H
H		X	Z

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER			54F/74F Min	54F/74F Typ	54F/74F Max	UNITS	CONDITIONS	
V_{OH}	Output HIGH Voltage		XM, XC	2.4			V	I_{OH} = -3.0 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	
			XM	2.0			V	I_{OH} = -12 mA	V_{IH} = 2.0 V V_{CC} = Min V_{IL} = 0.5 V
			XC	2.0				I_{OH} = -15 mA	
V_{OL}	Output LOW Voltage		XM			0.55	V	I_{OL} = 48 mA	V_{IN} = V_{IH} or V_{IL} V_{CC} = Min
			XC			0.55		I_{OL} = 64 mA	
$V_{T+} - V_{T-}$	Hysteresis Voltage			0.2	0.4		V	V_{CC} = Min	
I_{OS}	Output Short Circuit Current			-100		-225	mA	V_{CC} = Max, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	HIGH	'F240		57		mA	V_{CC} = Max	
			'F241, 'F244		57				
		LOW	'F240		64				
			'F241, 'F244		64				
		OFF	'F240		64				
			'F241, 'F244		71				

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F: T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF Min	Typ	Max	54F: T_A, V_{CC} = MIL, C_L = 50 pF Min	Max	74F: T_A, V_{CC} = COM, C_L = 50 pF Min	Max	UNITS	FIG. NO.
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('F240)		4.5 4.5						ns	2-17 2-18
t_{PZH} t_{PZL}	Output Enable Time ('F240)		6.0 10						ns	2-25 2-26
t_{PHZ} t_{PLZ}	Output Disable Time* ('F240)		10 6.0						ns	2-27
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('F241, 'F244)		6.0 6.0						ns	2-17 2-19
t_{PZH} t_{PZL}	Output Enable Time ('F241, 'F244)		6.0 10						ns	2-25 2-26
t_{PHZ} t_{PLZ}	Output Disable Time* ('F241, 'F244)		10 6.0						ns	2-27

*C_L = 5.0 pF, R_L = 90 Ω

54F/74F242 • 54F/74F243

QUAD BUS TRANSCEIVER

(With 3-State Outputs)

DESCRIPTION — The 'F242 and 'F243 are quad bus transmitters/receivers designed for 4-line asynchronous 2-way data communications between data buses.

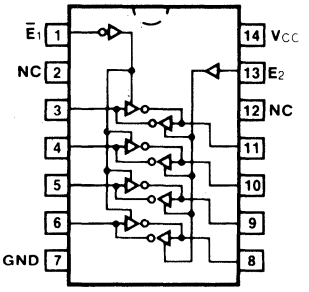
- **HYSTERESIS AT INPUTS TO IMPROVE NOISE IMMUNITY**
- **2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION**
- **INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS**

ORDERING CODE: See Section 5

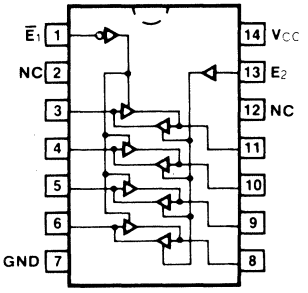
PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F242PC, 74F243PC		9A
Ceramic DIP (D)	74F242DC, 74F243DC	54F242DM, 54F243DM	6A
Flatpak (F)	74F242FC, 74F243FC	54F242FM, 54F243FM	3I

CONNECTION DIAGRAMS

'F242



'F243



INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$\overline{E}_1$	Enable Input (Active LOW)	0.5/0.625
E_2	Enable Input (Active HIGH)	0.5/0.625
	Inputs	1.75/1.0
	Outputs	75/40 (30)

TRUTH TABLES

'F242

INPUTS		OUTPUT
$\overline{E}_1$	D	
L	L	H
L	H	L
H	X	Z

INPUTS		OUTPUT
E_2	D	
L	X	Z
H	L	H
H	H	L

'F243

INPUTS		OUTPUT
$\overline{E}_1$	D	
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUT
E_2	D	
L	X	Z
H	L	L
H	H	H

H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial Z = High Impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54F/74F Min	54F/74F Typ	54F/74F Max	UNITS	CONDITIONS
V_{OH}	Output HIGH Voltage	XM, XC	2.4			V	I_{OH} = -3.0 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}
		XM	2.0			V	I_{OH} = -12 mA, V_{IH} = 2.0 V, V_{CC} = Min, V_{IL} = 0.5 V
		XC	2.0				I_{OH} = -15 mA
V_{OL}	Output LOW Voltage	XM			0.55	V	I_{OL} = 48 mA, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min
		XC			0.55		I_{OL} = 64 mA
$V_{T+} - V_{T-}$	Hysteresis Voltage		0.2	0.4		V	V_{CC} = Min
I_{OZH}	Output OFF Current HIGH				70	μA	V_{OUT} = 2.7V, V_{IN} = V_{IH} or V_{IL}, V_{CC} = Max
					100		V_{OUT} = 5.5V
I_{OZL}	Output OFF Current LOW				-1.6	mA	V_{CC} = Max, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 0.4 V
I_{OS}	Output Short Circuit Current		-100		-225	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current	HIGH	'F242		64	mA	V_{CC} = Max
			'F243		64		
		LOW	'F242		64		
			'F243		64		
		OFF	'F242		71		
			'F243		71		

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('F242)		6.0 6.0						ns	2-17 2-18
t_{PLH} t_{PHL}	Propagation Delay Data to Output ('F243)		4.5 4.5						ns	2-17 2-19
t_{PZH} t_{PZL}	Output Enable Time		6.0 10						ns	2-25 2-26
t_{PHZ} t_{PLZ}	Output Disable Time*		10 6.0						ns	2-27

*C_L = 5.0 pF, R_L = 90 Ω

54F/74F251

8-INPUT MULTIPLEXER

(With 3-State Outputs)

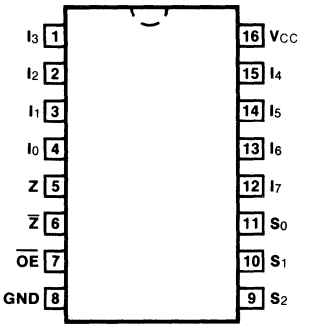
DESCRIPTION — The 'F251 is a high speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided.

- **MULTIFUNCTIONAL CAPABILITY**
- **ON-CHIP SELECT LOGIC DECODING**
- **INVERTING AND NON-INVERTING 3-STATE OUTPUTS**

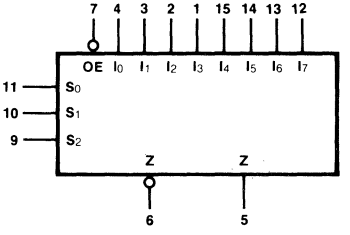
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F251PC		9B
Ceramic DIP (D)	74F251DC	54F251DM	6B
Flatpak (F)	74F251FC	54F251FM	4L

CONNECTION DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$S_0 - S_2$	Select Inputs	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
$I_0 - I_7$	Multiplexer Inputs	0.5/0.375
Z	Multiplexer Output	25/12.5
$\overline{Z}$	Complementary Multiplexer Output	25/12.5

FUNCTIONAL DESCRIPTION — This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

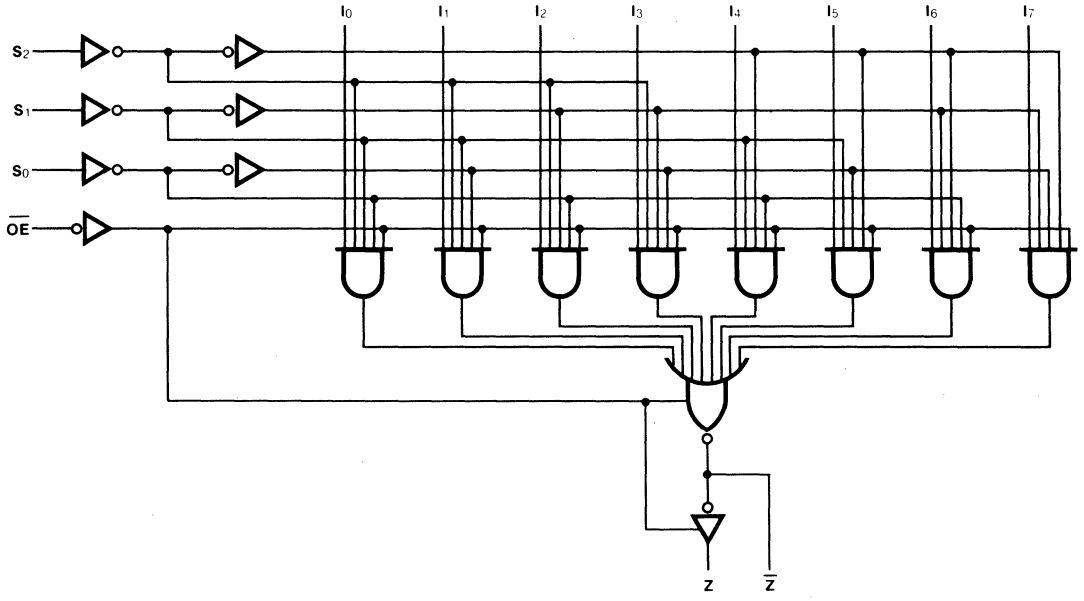
When the Output Enable is HIGH, both outputs are in the high impedance (high Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active LOW portion of the enable voltages.

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I_0}$	I_0
L	L	L	H	$\overline{I_1}$	I_1
L	L	H	L	$\overline{I_2}$	I_2
L	L	H	H	$\overline{I_3}$	I_3
L	H	L	L	$\overline{I_4}$	I_4
L	H	L	H	$\overline{I_5}$	I_5
L	H	H	L	$\overline{I_6}$	I_6
L	H	H	H	$\overline{I_7}$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54F/74F			UNITS	CONDITIONS	
			Min	Typ	Max			
I_{CC}	Power Supply Current	ON		10		mA	I_n, S_n = 4.5 V $\overline{OE}$ = Gnd	V_{CC} = Max
		OFF		10.5			$\overline{OE}$, I_n = 4.5 V	

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$		6.3 6.2						ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay S_n to Z_n		8.1 7.9						ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}$		2.9 2.8						ns	2-17 2-18
t_{PLH} t_{PHL}	Propagation Delay I_n to Z		4.7 4.5						ns	2-17 2-19
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to $\overline{Z}$								ns	2-25 2-26 2-27
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Z								ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Output Disable Time* $\overline{OE}$ to $\overline{Z}$								ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Output Disable Time* $\overline{OE}$ to Z								ns	2-25 2-26 2-27

*C_L = 5 pF

54F/74F253

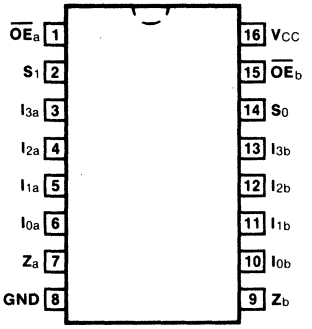
DUAL 4-INPUT MULTIPLEXER

(With 3-State Outputs)

DESCRIPTION — The 'F253 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

- **ADVANCED SCHOTTKY PROCESS FOR HIGH SPEED**
- **MULTIFUNCTION CAPABILITY**
- **NON-INVERTING 3-STATE OUTPUTS**

CONNECTION DIAGRAM



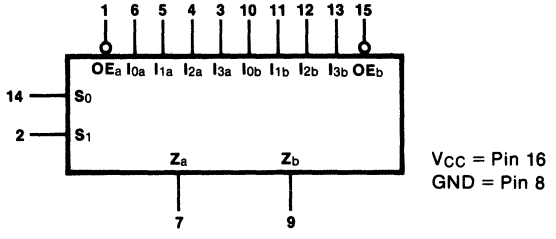
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F253PC		9B
Ceramic DIP (D)	74F253DC	54F253DM	6B
Flatpak (F)	74F253FC	54F253FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
I_{0a} — I_{3a}	Side A Data Inputs	0.5/0.375
I_{0b} — I_{3b}	Side B Data Inputs	0.5/0.375
S_0, S_1	Common Select Inputs	0.5/0.375
$\overline{OE}_a$	Side A Output Enable Input (Active LOW)	0.5/0.375
$\overline{OE}_b$	Side B Output Enable Input (Active LOW)	0.5/0.375
Z_a, Z_b	3-State Outputs	25/12.5

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — This device contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (high Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

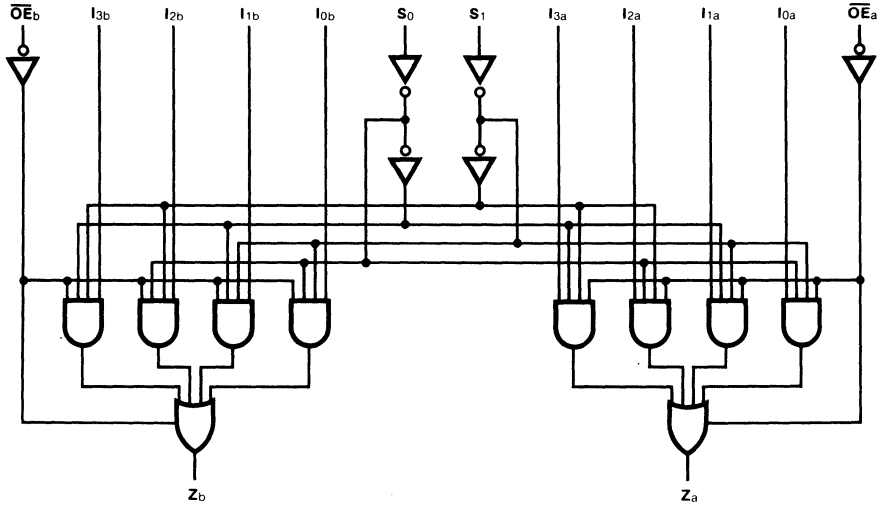
4

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S_0 and S_1 are common to both sections.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z)= High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54F/74F			UNITS	CONDITIONS
			Min	Typ	Max		
I_{CC}	Power Supply Current	HIGH		14	20	mA	V_{CC} = Max, $\overline{OE}_n$ = Gnd I_0, S_n = 4.5 V; I_1 — I_3 = Gnd
		LOW		14	20		V_{CC} = Max I_n, S_n, $\overline{OE}_n$ = Gnd
		OFF		14	25		V_{CC} = Max, $\overline{OE}_n$ = 4.5 V I_n, S_n = Gnd

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to Z_n	4.0 3.0	9.5 8.0	13 10					ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	2.0 2.0	4.4 4.4	6.0 6.0					ns	2-17 2-19
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	5.3 6.5	7.0 8.0					ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Output Disable Time*	2.0 2.0	4.3 4.0	6.0 6.0					ns	2-25 2-26 2-27

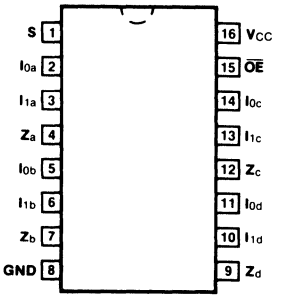
*C_L = 5.0 pF

54F/74F257

QUAD 2-INPUT MULTIPLEXER

(With 3-State Outputs)

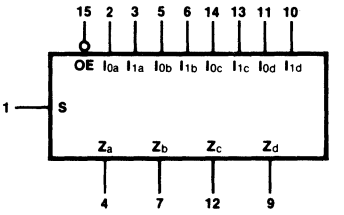
CONNECTION DIAGRAM



DESCRIPTION — The 'F257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (non-inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus oriented systems.

- **MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER**
- **NON-INVERTING 3-STATE OUTPUTS**
- **INPUT CLAMP DIOES LIMIT HIGH SPEED TERMINATION EFFECTS**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	74F257PC		9B
Ceramic DIP (D)	74F257DC	54F257DM	6B
Flatpak (F)	74F257FC	54F257FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
S	Common Data Select Input	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
I_{0a} — I_{0d}	Data Inputs from Source 0	0.5/0.375
I_{1a} — I_{1d}	Data Inputs from Source 1	0.5/0.375
Z_a — Z_d	Multiplexer Outputs	25/12.5

FUNCTIONAL DESCRIPTION — The 'F257 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (non-inverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S}) \qquad Z_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S}) \qquad Z_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

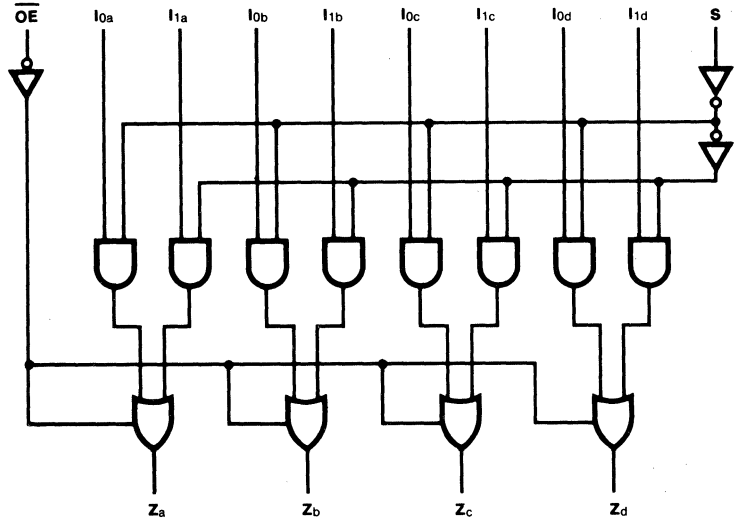
When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	Z
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z)= High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54F/74F			UNITS	CONDITIONS
			Min	Typ	Max		
I_{CC}	Power Supply Current	HIGH		9.0	15	mA	V_{CC} = Max; S, I_{1x} = 4.5 V $\overline{OE}$, I_{0x} = Gnd
		LOW		14.5	22		V_{CC} = Max; I_{1x} = 4.5 V $\overline{OE}$, I_{0x}, S = Gnd
		OFF		15	23		V_{CC} = Max; S, I_{0x} = Gnd $\overline{OE}$, I_{1x} = 4.5 V

4

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_n to Z_n	2.0 2.0	4.0 3.5	6.0 4.5					ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay S to Z_n	4.0 3.0	10 7.5	13 9.0					ns	2-17 2-23
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	5.0 5.5	7.0 7.0					ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Output Disable Time*	2.0 2.0	4.0 4.0	6.0 6.0					ns	2-25 2-26 2-27

*C_L = 5 pF

54F/74F258

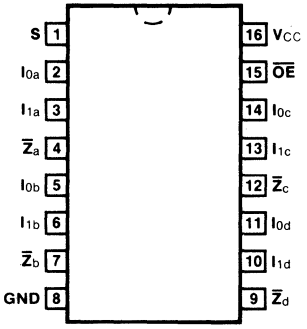
QUAD 2-INPUT MULTIPLEXER

(With 3-State Outputs)

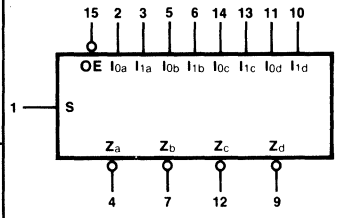
DESCRIPTION — The 'F258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus oriented systems.

- **MULTIPLEXER EXPANSION BY TYING OUTPUTS TOGETHER**
- **INVERTING 3-STATE OUTPUTS**

CONNECTION DIAGRAM



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F258PC		9B
Ceramic DIP (D)	74F258DC	54F258DM	6B
Flatpak (F)	74F258FC	54F258FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
S	Common Data Select Input	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
$I_{0a} - I_{0d}$	Data Inputs from Source 0	0.5/0.375
$I_{1a} - I_{1d}$	Data Inputs from Source 1	0.5/0.375
$\overline{Z}_a - \overline{Z}_d$	Inverting Data Outputs	25/12.5

FUNCTIONAL DESCRIPTION — The 'F258 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The 'F258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\bar{Z}_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \bar{S}) \qquad \bar{Z}_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \bar{S})$$
$$\bar{Z}_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \bar{S}) \qquad \bar{Z}_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \bar{S})$$

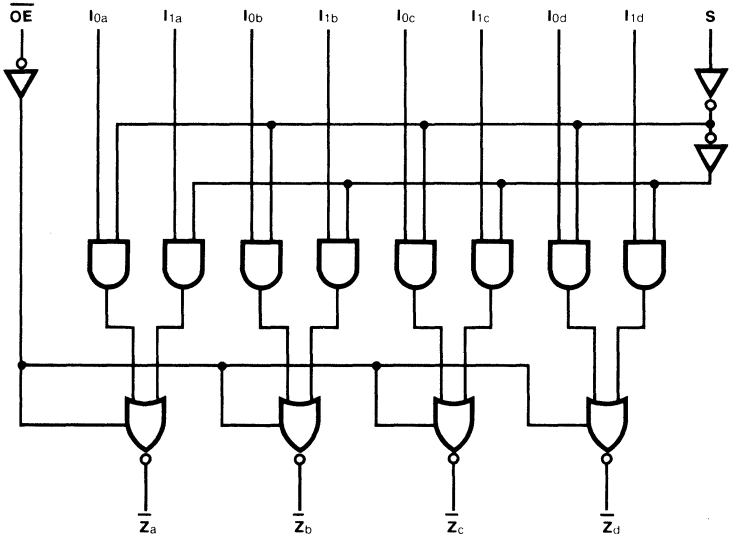
When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance OFF state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

TRUTH TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	$\bar{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54F/74F			UNITS	CONDITIONS
			Min	Typ	Max		
I_{CC}	Power Supply Current	HIGH		5.8		mA	V_{CC} = Max; S, I_{1x} = 4.5 V $\overline{OE}$, I_{0x} = Gnd
		LOW		14			V_{CC} = Max; I_{1x} = 4.5 V $\overline{OE}$, I_{0x}, S = Gnd
		OFF		16.8			V_{CC} = Max; S, I_{0x} = Gnd $\overline{OE}$, I_{1x} = 4.5 V

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$		2.9 2.8						ns	2-17 2-18
t_{PLH} t_{PHL}	Propagation Delay S to $\overline{Z}_n$		6.3 6.2						ns	2-17 2-23
t_{PZH} t_{PZL}	Output Enable Time								ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Output Disable Time*								ns	2-25 2-26 2-27

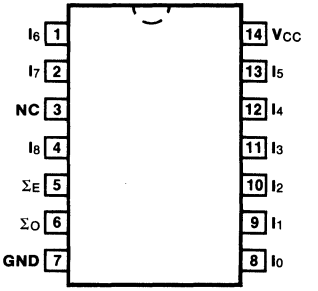
*C_L = 5 pF

54F/74F280

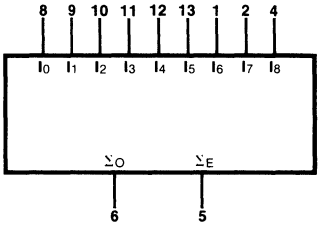
9-BIT PARITY GENERATOR/CHECKER

DESCRIPTION— The 'F280 is a high speed parity generator/checker that accepts nine bits of input data and detects whether an even or an odd number of these inputs is HIGH. If an even number of inputs is HIGH, the Sum Even output is HIGH. If an odd number is HIGH, the Sum Even output is LOW. The Sum Odd output is the complement of the Sum Even output.

CONNECTION DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F280PC		9A
Ceramic DIP (D)	74F280DC	54F280DM	6A
Flatpak (F)	74F280FC	54F280FM	3I

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

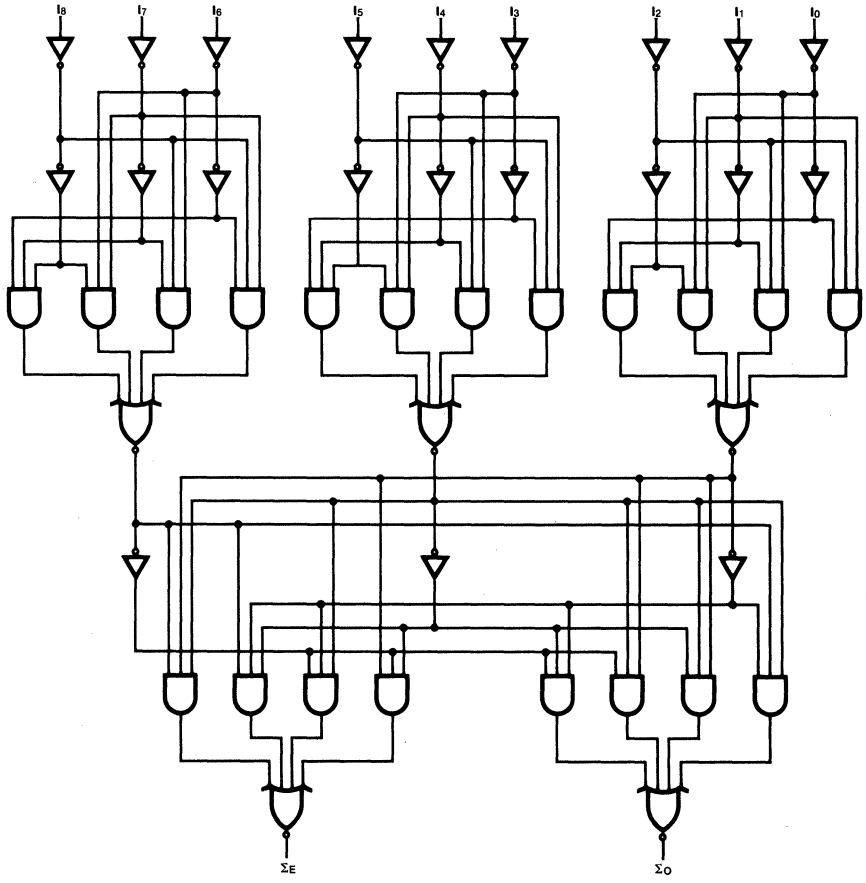
PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
I_0 — I_8	Data Inputs	0.5/0.375
Σ_O	Odd Parity Output	25/12.5
Σ_E	Even Parity Output	25/12.5

TRUTH TABLE

NUMBER OF INPUTS I_0 — I_8 THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8,	H	L
1, 3, 5, 7, 9	L	H

H = HIGH Voltage Level
L = LOW Voltage Level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		25		mA	V_{CC} = Max

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_E		12.5 10.5						ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay I_n to Σ_O		12.5 10.5						ns	2-17 2-23

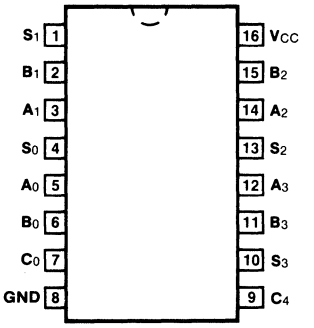
54F/74F283

4-BIT BINARY FULL ADDER

(With Fast Carry)

DESCRIPTION—The 'F283 high speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words (A_0—A_3, B_0—B_3) and a Carry input (C_0). It generates the binary Sum outputs (S_0—S_3) and the Carry output (C_4) from the most significant bit. The 'F283 will operate with either active HIGH or active LOW operands (positive or negative logic).

CONNECTION DIAGRAM



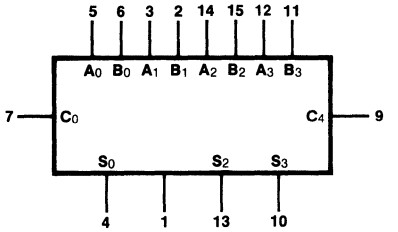
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F283PC		9B
Ceramic DIP (D)	74F283DC	54F283DM	6B
Flatpak (F)	74F283FC	54F283FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
A_0—A_3	A Operand Inputs	0.5/0.375
B_0—B_3	B Operand Inputs	0.5/0.375
C_0	Carry Input	0.5/0.375
S_0—S_3	Sum Outputs	25/12.5
C_4	Carry Output	25/12.5

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The 'F283 adds two 4-bit binary words (A plus B) plus the incoming carry C_0. The binary sum appears on the Sum (S_0 — S_3) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1) + 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3) = S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$

Where (+) = plus

Interchanging inputs of equal weight does not affect the operation. Thus C_0, A_0, B_0 can be arbitrarily assigned to pins 5, 6 and 7. Due to the symmetry of the binary add function, the 'F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). Note that if C_0 is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Example:

	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: 0 + 10 + 9 = 3 + 16 Active LOW: 1 + 5 + 6 = 12 + 0

Due to pin limitations, the intermediate carries of the 'F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. *Figure a* shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) LOW makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, *Figure b* shows a way of dividing the 'F283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2. Note that as long as A_2 and B_2 are the same, whether HIGH or LOW, they do not influence S_2. Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third stage. *Figure c* shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0, S_1 and S_2 present a binary number equal to the number of inputs I_1 — I_5 that are true. *Figure d* shows one method of implementing a 5-input majority gate. When three or more of the inputs I_1 — I_5 are true, the output M_5 is true.

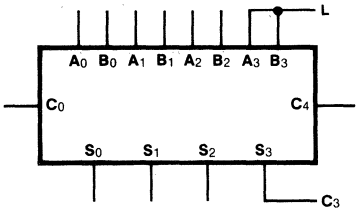


Fig. a 3-Bit Adder

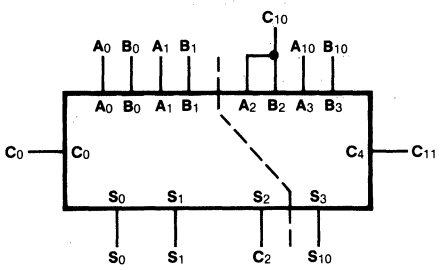


Fig. b 2-Bit and 1-Bit Adders

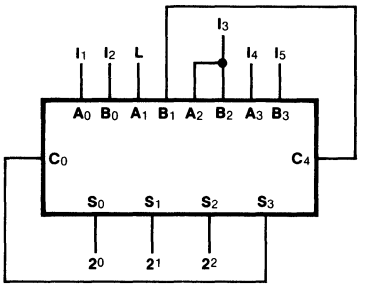


Fig. c 5-Input Encoder

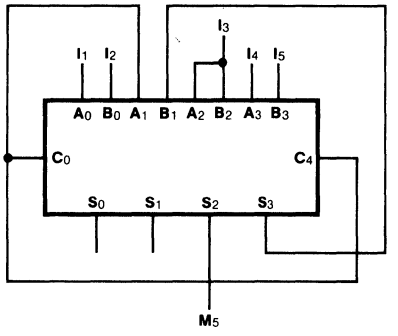
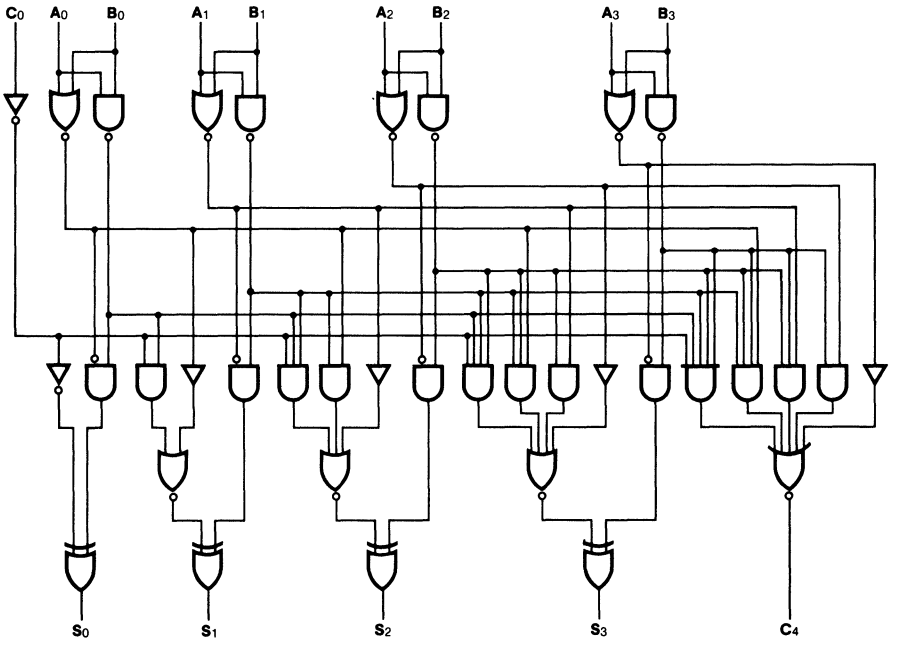


Fig. d 5-Input Majority Gate

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		30		mA	V_{CC} = Max Inputs = 4.5 V

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay C_0 to S_n		8.2 7.5						ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to S_n		8.5 8.5						ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay C_0 to C_4		4.7 4.7						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to C_4		4.7 4.7						ns	2-17 2-19

54F/74F289

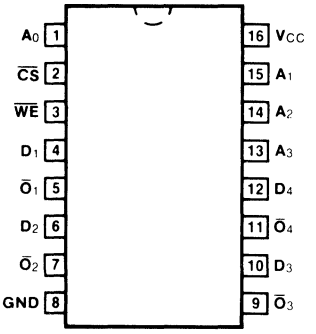
64-BIT RANDOM ACCESS MEMORY

(With Open-Collector Outputs)

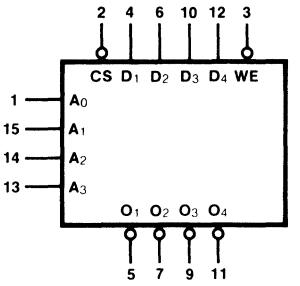
DESCRIPTION — The 'F289 is a high speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading, and addresses are fully decoded on-chip. Outputs are open-collector type and are in the off (HIGH) state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode; output data is the complement of the stored data.

- **OPEN-COLLECTOR OUTPUTS FOR WIRED-AND APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**

CONNECTION DIAGRAM



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	74F289PC		9B
Ceramic DIP (D)	74F289DC	54F289DM	6B
Flatpak (F)	74F289FC	54F289FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.375
$\overline{WE}$	Write Enable Input (Active LOW)	0.5/0.375
$D_1 - D_4$	Data Inputs	0.5/0.375
$\overline{O}_1 - \overline{O}_4$	Inverted Data Outputs	OC*/12.5

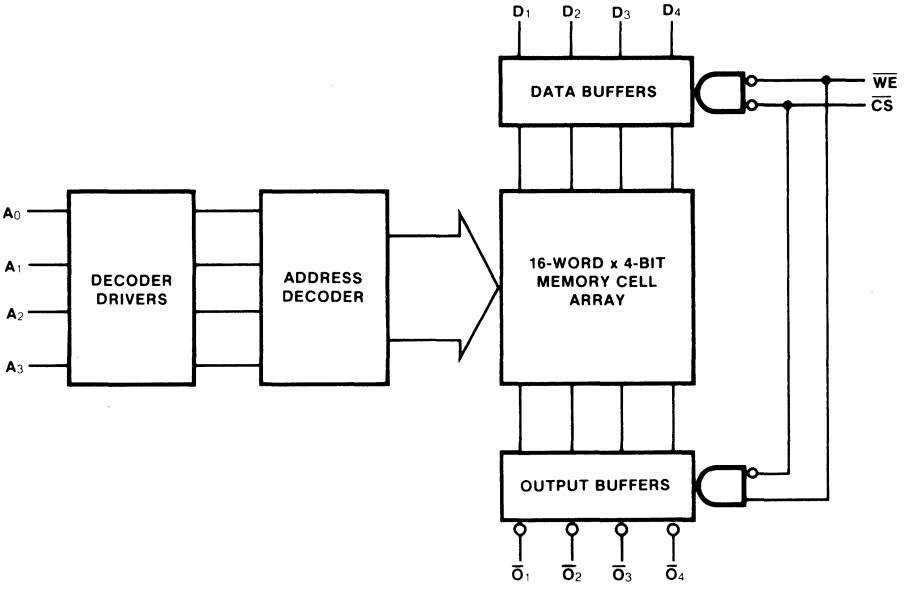
*OC — Open Collector

FUNCTION TABLE

INPUTS		OPERATION	CONDITION OF OUTPUTS
$\overline{CS}$	$\overline{WE}$		
L	L	Write	Off (HIGH)
L	H	Read	Complement of Stored Data
H	X	Inhibit	Off (HIGH)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		43		mA	V_{CC} = Max; $\overline{WE}$, $\overline{CS}$ = Gnd

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Access Time, HIGH or LOW[1] A_n to $\overline{O}_n$		20 20						ns	2-17 2-23
t_{PHL}	Access Time[1] $\overline{CS}$ to $\overline{O}_n$		12						ns	2-17 2-19
t_{PLH}	Disable Time[1] $\overline{CS}$ to $\overline{O}_n$		12							
t_{PHL}	Recovery Time* $\overline{WE}$ to $\overline{O}_n$		12						ns	2-17 2-18
t_{PLH}	Disable Time[1] $\overline{WE}$ to $\overline{O}_n$		12							

1. R_L = 280 Ω

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = MIL		T_A, V_{CC} = COM			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW A_n to $\overline{WE}$	0 0							ns	2-30
t_h (H) t_h (L)	Hold Time, HIGH or LOW A_n to $\overline{WE}$	0 0								
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to $\overline{WE}$	20 20							ns	2-28
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to $\overline{WE}$	0 0								
t_s (L)	Setup Time LOW $\overline{CS}$ to $\overline{WE}$								ns	2-28
t_h (L)	Hold Time LOW $\overline{CS}$ to $\overline{WE}$								ns	2-28
t_w (L)	$\overline{WE}$ Pulse Width LOW	20							ns	2-29

*R_L = 280 Ω

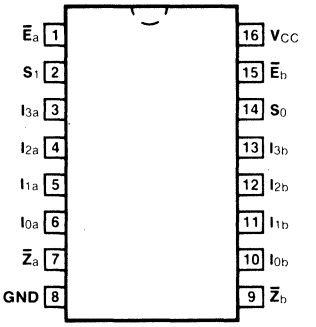
54F/74F352

DUAL 4-INPUT MULTIPLEXER

DESCRIPTION — The 'F352 is a very high speed dual 4-input multiplexer with Common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The 'F352 is the functional equivalent of the 'F153 except with inverted outputs.

- **INVERTED VERSION OF THE 'F153**
- **SEPARATE ENABLES FOR EACH MULTIPLEXER**
- **INPUT CLAMP DIODE LIMITS HIGH SPEED TERMINATION EFFECTS**

CONNECTION DIAGRAM



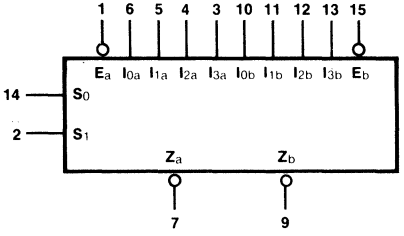
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F352PC		9B
Ceramic DIP (D)	74F352DC	54F352DM	6B
Flatpak (F)	74F352FC	54F352FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
I_{0a} — I_{3a}	Side A Data Inputs	0.5/0.375
I_{0b} — I_{3b}	Side B Data Inputs	0.5/0.375
S_0, S_1	Common Select Inputs	0.5/0.375
$\overline{E}_a$	Side A Enable Input (Active LOW)	0.5/0.375
$\overline{E}_b$	Side B Enable Input (Active LOW)	0.5/0.375
$\overline{Z}_a$, $\overline{Z}_b$	Multiplexer Outputs (Inverted)	25/12.5

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The 'F352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs ($\overline{Z}_a$, $\overline{Z}_b$) are forced HIGH.

The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{E_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)}$$

$$\overline{Z}_b = \overline{E_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)}$$

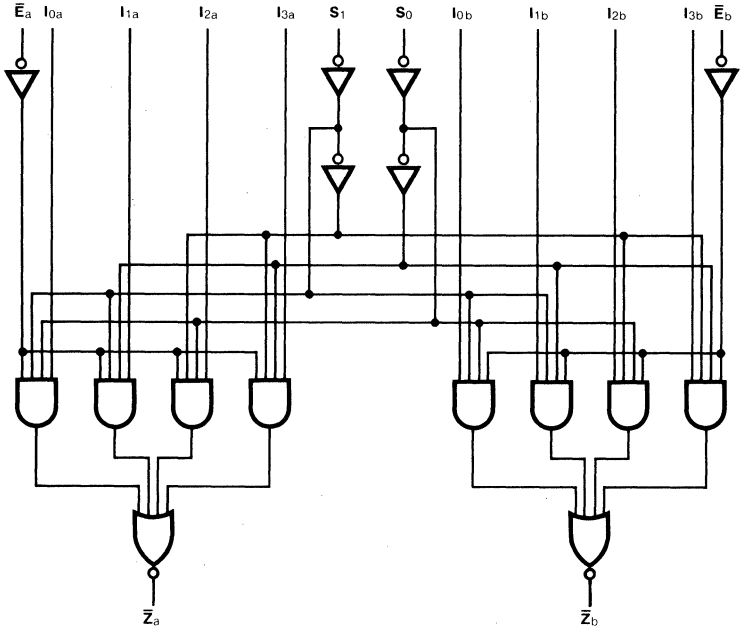
The 'F352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'F352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	$\overline{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		8.0		mA	V_{CC} = Max; V_{IN} = Gnd

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$		6.3 6.2						ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$		4.6 4.5						ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$		2.9 2.8						ns	2-17 2-18

54F/74F353

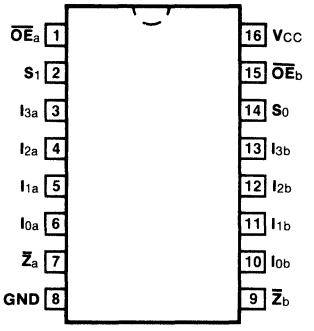
DUAL 4-INPUT MULTIPLEXER

(With 3-State Outputs)

DESCRIPTION — The 'F353 is a dual 4-input mulitplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable($\overline{OE}$)inputs, allowing the outputs to interface directly with bus oriented systems.

- **INVERTED VERSION OF 'F253**
- **MULTIFUNCTION CAPABILITY**
- **SEPARATE ENABLES FOR EACH MULTIPLEXER**

CONNECTION DIAGRAM



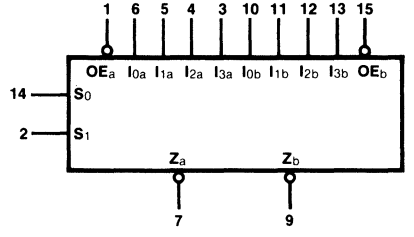
ORDERING CODE: See Section 5

PKG	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F353PC		9B
Ceramic DIP (D)	74F353DC	54F353DM	6B
Flatpak (F)	74F353FC	54F353FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
I_{0a} — I_{3a}	Side A Data Inputs	0.5/0.375
I_{0b} — I_{3b}	Side B Data Inputs	0.5/0.375
S_0, S_1	Common Select Inputs	0.5/0.375
$\overline{OE}_a$	Side A Output Enable Input (Active LOW)	0.5/0.375
$\overline{OE}_b$	Side B Output Enable Input (Active LOW)	0.5/0.375
$\overline{Z}_a$, $\overline{Z}_b$	3-State Outputs (Inverted)	25/12.5

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The 'F353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0,S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (high Z) state. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$\overline{Z}_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

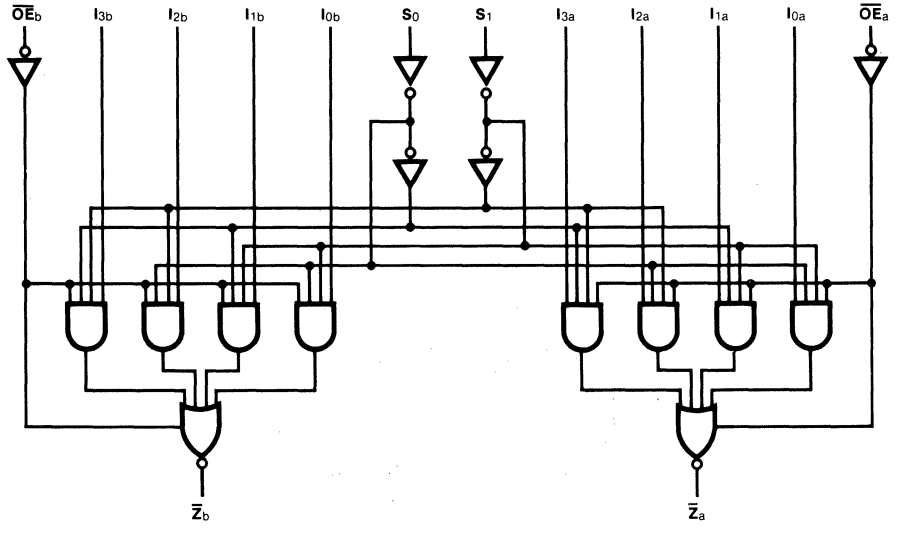
If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs S_0 and S_1 are common to both sections.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54F/74F			UNITS	CONDITIONS	
			Min	Typ	Max			
I_{CC}	Power Supply Current	HIGH		8.0		mA	I_n, S_n, $\overline{OE}_n$ = Gnd	
		OFF		15.3			I_n, S_n = Gnd; $\overline{OE}_n$ = 4.5 V	V_{CC} = Max

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$		6.3 6.2						ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$		2.9 2.8						ns	2-17 2-18
t_{PZH} t_{PZL}	Output Enable Time								ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Output Disable Time*								ns	2-25 2-26 2-27

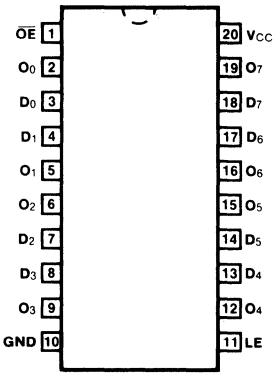
*C_L = 5 pF

54F/74F373

OCTAL TRANSPARENT LATCH

(With 3-State Outputs)

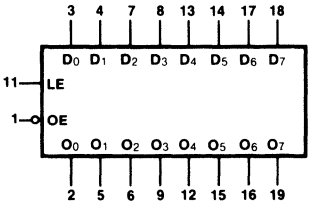
CONNECTION DIAGRAM



DESCRIPTION — The 'F373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

- **EIGHT LATCHES IN A SINGLE PACKAGE**
- **3-STATE OUTPUTS FOR BUS INTERFACING**

LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

ORDERING CODE: See Section 5

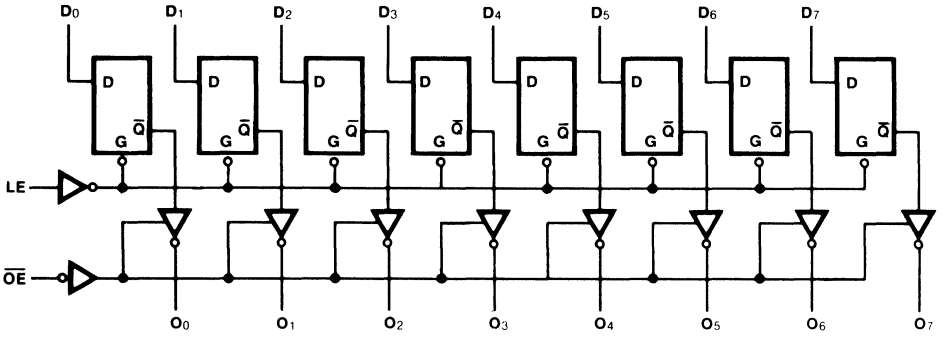
PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	74F373PC		9Z
Ceramic DIP (D)	74F373DC	54F373DM	4E
Flatpak (F)	74F373FC	54F373FM	4F

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
D0 — D7	Data Inputs	0.5/0 375
LE	Latch Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
O0 — O7	3-State Latch Outputs	25/12.5

FUNCTIONAL DESCRIPTION — The 'F373 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current (All Outputs OFF)		35	55	mA	V_{CC} = Max, $\overline{OE}$ = 4.5 V D_n, LE = Gnd

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to O_n	2.0 1.0	4.3 2.7	6.5 4.5					ns	2-17 2-19
t_{PLH} t_{PHL}	Propagation Delay LE to O_n	4.0 2.0	9.2 4.2	13 6.5					ns	2-17 2-21
t_{PZH} t_{PZL}	Output Enable Time	3.0 3.0	6.8 6.0	11 10					ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Output Disable Time*	3.0 3.0	5.7 6.2	9.0 9.0					ns	2-25 2-26 2-27

*C_L = 5.0 pF

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = MIL		T_A, V_{CC} = COM			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to LE	2.0 2.0							ns	2-29
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to LE	3.0 3.0							ns	2-29
t_w (H)	LE Pulse Width HIGH	6.0							ns	2-21

54F/74F374

OCTAL D-TYPE FLIP-FLOP

(With 3-State Outputs)

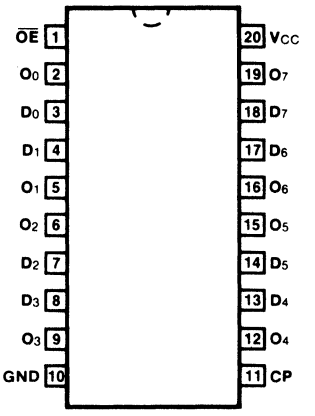
DESCRIPTION — The 'F374 is a high speed, low power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**

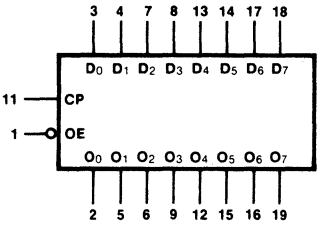
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	74F374PC		9Z
Ceramic DIP (D)	74F374DC	54F374DM	4E
Flatpak (F)	74F374FC	54F374FM	4F

CONNECTION DIAGRAM



LOGIC SYMBOL

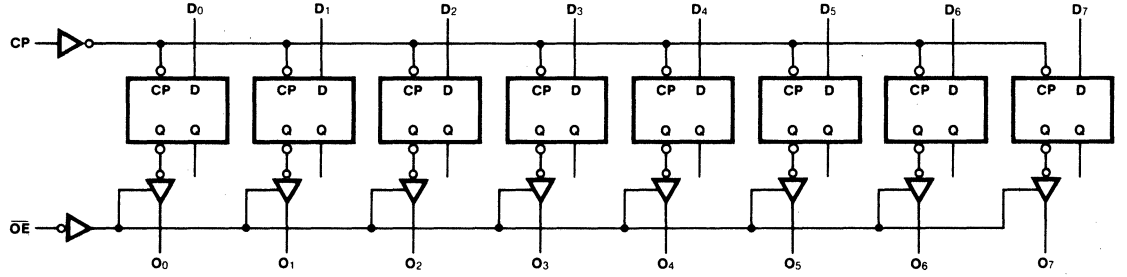


V_{CC} = Pin 20
GND = Pin 10

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
$O_0 - O_7$	3-State Outputs	25/12.5

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — The 'F374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

TRUTH TABLE

INPUTS		OUTPUTS	
D_n	CP	$\overline{OE}$	O_n
H	⎍	L	H
L	⎍	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current (All Outputs OFF)		55	86	mA	V_{CC} = Max, D_n = Gnd $\overline{OE}$ = 4.5 V

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			T_A, V_{CC} = MIL, C_L = 50 pF		T_A, V_{CC} = COM, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency								MHz	2-17/21
t_{PLH} t_{PHL}	Propagation Delay CP to O_n	3.0 3.0	5.5 5.5	9.0 9.0					ns	2-17 2-21
t_{PZH} t_{PZL}	Output Enable Time	3.0 3.0	6.5 6.5	10 10					ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Output Disable Time*	3.0 3.0	5.5 4.5	8.0 7.0					ns	2-25 2-26 2-27

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = MIL		T_A, V_{CC} = COM			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to CP	2.0 2.0							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to CP	2.0 2.0								
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	7.0 6.0							ns	2-21

*C_L = 5 pF

54F/74F379

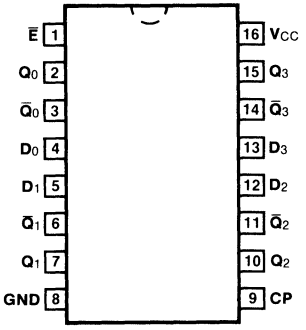
QUAD PARALLEL REGISTER

(With Enable)

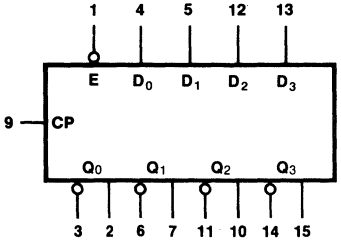
DESCRIPTION — The 'F379 is a 4-bit register with buffered common Enable. This device is similar to the 'F175 but features the common Enable rather than common Master Reset.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **BUFFERED COMMON ENABLE INPUT**
- **TRUE AND COMPLEMENT OUTPUTS**

CONNECTION DIAGRAM



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
	VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	74F379PC		9B
Ceramic DIP (D)	74F379DC	54F379DM	6B
Flatpak (F)	74F379FC	54F379FM	4L

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$\overline{E}$	Enable Input (Active LOW)	0.5/0.375
$D_0 - D_3$	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$Q_0 - Q_3$	Flip-flop Outputs	25/12.5
$\overline{Q}_0 - \overline{Q}_3$	Complement Outputs	25/12.5

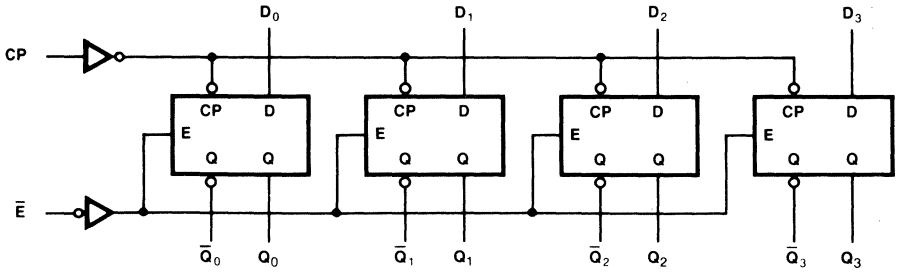
FUNCTIONAL DESCRIPTION — The 'F379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input. The D_n and $\overline{E}$ inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

TRUTH TABLE

INPUTS			OUTPUTS	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q}_n$
H	⎍	X	No Change	No Change
L	⎍	H	H	L
L	⎍	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current		27		mA	V_{CC} = Max; D, $\overline{E}$ = Gnd CP = ⌐¬

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	110	150						MHz	2-17/21
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		6.1 6.3						ns	2-17 2-21

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V			54F T_A, V_{CC} = MIL		74F T_A, V_{CC} = COM		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to CP	3.0 3.0							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to CP	2.0 2.0							ns	
t_s (H) t_s (L)	Setup Time, HIGH or LOW $\overline{E}$ to CP	5.0 6.0							ns	
t_h (H) t_h (L)	Hold Time, HIGH or LOW $\overline{E}$ to CP	0 0							ns	
t_w (L)	CP Pulse Width LOW	4.5							ns	2-21

54F/74F533

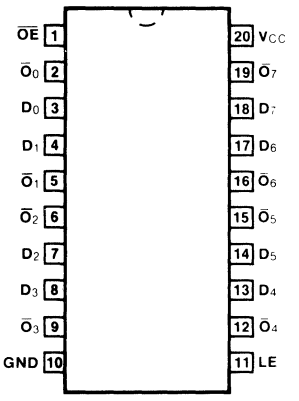
OCTAL TRANSPARENT LATCH

(With 3-State Outputs)

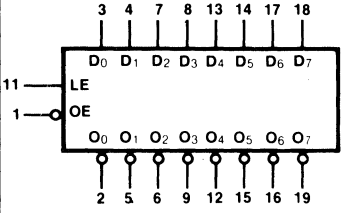
DESCRIPTION — The 'F533 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state. The 'F533 is the same as the 'F373, except that the outputs are inverted. For description and logic diagram please see the 'F373 data sheet.

- **EIGHT LATCHES IN A SINGLE PACKAGE**
- **3-STATE OUTPUTS FOR BUS INTERFACING**

CONNECTION DIAGRAM



LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F533PC		9Z
Ceramic DIP (D)	74F533DC	54F533DM	4E
Flatpak (F)	74F533FC	54F533FM	4F

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.375
LE	Latch Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
$\overline{O}_0 - \overline{O}_7$	Complementary 3-State Outputs	25/12.5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current (All Outputs OFF)		35		mA	V_{CC} = Max, $\overline{OE}$ = 4.5 V D_n, LE = Gnd

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$		5.3 3.7						ns	2-17 2-18
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$		9.2 4.2						ns	2-17 2-21
t_{PZH} t_{PZL}	Output Enable Time								ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Output Disable Time*								ns	2-25 2-26 2-27

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V			54F T_A, V_{CC} = MIL		74F T_A, V_{CC} = COM		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to LE	3.0 3.0							ns	2-29
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to LE	2.0 2.0							ns	2-29
t_w (H)	LE Pulse Width HIGH	6.0							ns	2-21

*C_L = 5.0 pF

54F/74F534

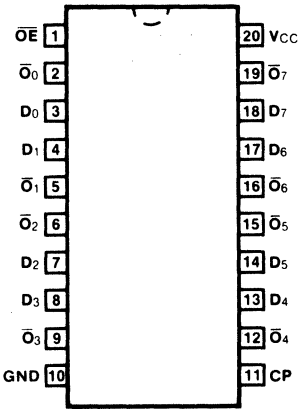
OCTAL D-TYPE FLIP-FLOP

(With 3-State Outputs)

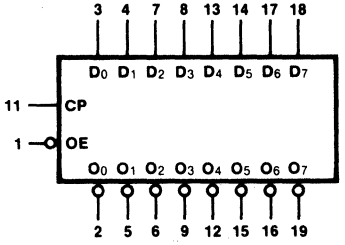
DESCRIPTION — The 'F534 is a high speed, low power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The 'F534 is the same as the 'F374 except that the outputs are inverted.

- **EDGE-TRIGGERED D-TYPE INPUTS**
- **BUFFERED POSITIVE EDGE-TRIGGERED CLOCK**
- **3-STATE OUTPUTS FOR BUS ORIENTED APPLICATIONS**

CONNECTION DIAGRAM



LOGIC SYMBOL



VCC = Pin 20
GND = Pin 10

ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F534PC		9Z
Ceramic DIP (D)	74F534DC	54F534DM	4E
Flatpak (F)	74F534FC	54F534FM	4F

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitons

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$D_0 - D_7$	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
$\overline{O}_0 - \overline{O}_7$	Complementray 3-State Outputs	25/12.5

FUNCTIONAL DESCRIPTION — The 'F534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current (All Outputs OFF)		55		mA	V_{CC} = Max, D_n = Gnd $\overline{OE}$ = 4.5 V

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V C_L = 15 pF			T_A, V_{CC} = MIL C_L = 50 pF		T_A, V_{CC} = COM C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency								MHz	2-17/21
t_{PLH} t_{PHL}	Propagation Delay CP to O_n		5.5 5.5						ns	2-17 2-21
t_{PZH} t_{PZL}	Output Enable Time		6.5 6.5						ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Output Disable Time*		5.5 4.5						ns	2-25 2-26 2-27

AC OPERATING REQUIREMENTS: See Section 2 for waveforms

SYMBOL	PARAMETER	54F/74F			54F		74F		UNITS	FIG. NO.
		T_A = +25°C, V_{CC} = +5.0 V			T_A, V_{CC} = MIL		T_A, V_{CC} = COM			
		Min	Typ	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to CP	2.0 2.0							ns	2-20
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to CP	2.0 2.0								
t_w (H) t_w (L)	CP Pulse Width, HIGH or LOW	7.0 6.0							ns	2-21

*C_L = 5 pF

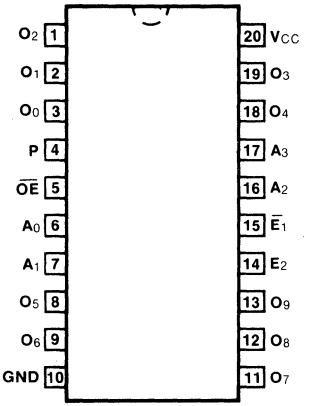
54F/74F537

1-of-10 DECODER

(With 3-State Outputs)

DESCRIPTION — The 'F537 is a one-of-ten decoder/demultiplexer with four active-HIGH BCD inputs and ten mutually exclusive outputs. A polarity control input determines whether the outputs are active-LOW or active-HIGH. The 'F537 has 3-state outputs, and a HIGH signal on the Output Enable ($\overline{OE}$) input forces all outputs to the high impedance state. Two input enables, active-HIGH E_2 and active-LOW $\overline{E}_1$, are available for demultiplexing data to the selected output in either non-inverted or inverted form. Input codes greater than BCD nine cause all outputs to go to the inactive state (i.e., same polarity as the P input).

CONNECTION DIAGRAM



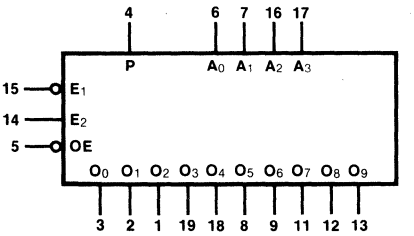
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F537PC		9Z
Ceramic DIP (D)	74F537DC	54F537DM	4E
Flatpak (F)	74F537FC	54F537FM	4F

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	0.5/0.375
$\overline{E}_1$	Enable Input (Active LOW)	0.5/0.375
E_2	Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	Output Enable Input (Active LOW)	0.5/0.375
P	Polarity Control Input	0.5/0.375
$O_0 - O_9$	3-State Outputs	25/12.5

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

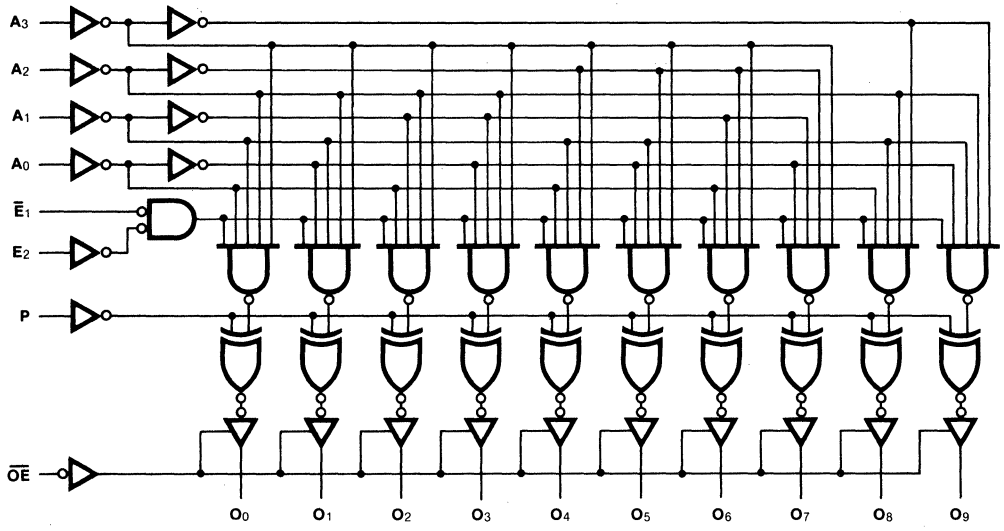
TRUTH TABLE

FUNCTION	INPUTS							OUTPUTS									
	$\overline{OE}$	$\overline{E}_1$	E_2	A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9
High Impedance	H	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	H	X	X	X	X	X	Outputs Equal P Input									
	L	X	L	X	X	X	X										
Active-HIGH Output (P = L)	L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L
	L	L	H	L	L	L	H	L	H	L	L	L	L	L	L	L	L
	L	L	H	L	L	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	H	L	L	H	H	L	L	L	H	L	L	L	L	L	L
	L	L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L
	L	L	H	L	H	L	H	L	L	L	L	L	H	L	L	L	L
	L	L	H	L	H	H	L	L	L	L	L	L	L	H	L	L	L
	L	L	H	L	H	H	H	L	L	L	L	L	L	L	H	L	L
	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
	L	L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H
	L	L	H	H	X	H	X	L	L	L	L	L	L	L	L	L	L
	L	L	H	H	H	X	X	L	L	L	L	L	L	L	L	L	L
Active-LOW Output (P = H)	L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H
	L	L	H	L	L	L	H	H	L	H	H	H	H	H	H	H	H
	L	L	H	L	L	H	L	H	H	L	H	H	H	H	H	H	H
	L	L	H	L	L	H	H	H	H	H	L	H	H	H	H	H	H
	L	L	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
	L	L	H	L	H	L	H	H	H	H	H	H	L	H	H	H	H
	L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	H
	L	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H
	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	L	H
	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L
	L	L	H	H	X	H	X	H	X	H	H	H	H	H	H	H	H
	L	L	H	H	H	X	X	H	H	H	H	H	H	H	H	H	H

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

4

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current (All Outputs OFF)		44		mA	$A_0 - A_3$, $\overline{E}_1$ = Gnd $\overline{OE}$, E_2, P = HIGH

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n		12.5 11.5						ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ to O_n		11.5 11							
t_{PLH} t_{PHL}	Propagation Delay E_2 to O_n		14 14.5						ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay P to O_n		13 12							
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n		5.0 5.5						ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Output Disable Time* $\overline{OE}$ to O_n		5.0 5.0							

*C_L = 5.0 pF

54F/74F538

1-of-8 DECODER

(With 3-State Outputs)

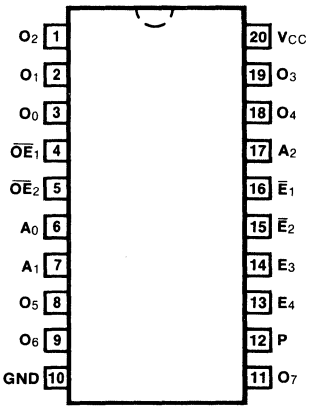
DESCRIPTION — The 'F538 decoder/demultiplexer accepts three Address (A_0 — A_2) input signals and decodes them to select one of eight mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active-LOW or active-HIGH. A HIGH signal on either of the active-LOW Output Enable ($\overline{OE}$) inputs forces all outputs to the high impedance state. Two active-HIGH and two active-LOW input enables are available for easy expansion to 1-of-32 decoding with four packages, or for data demultiplexing to one of eight or one of 16 destinations.

- **OUTPUT POLARITY CONTROL**
- **DATA DEMULTIPLEXING CAPABILITY**
- **MULTIPLE ENABLES FOR EXPANSION**
- **3-STATE OUTPUTS**

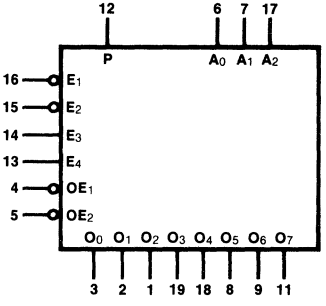
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F538PC		9Z
Ceramic DIP (D)	74F538DC	54F538DM	4E
Flatpak (F)	74F538FC	54F538FM	4F

CONNECTION DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

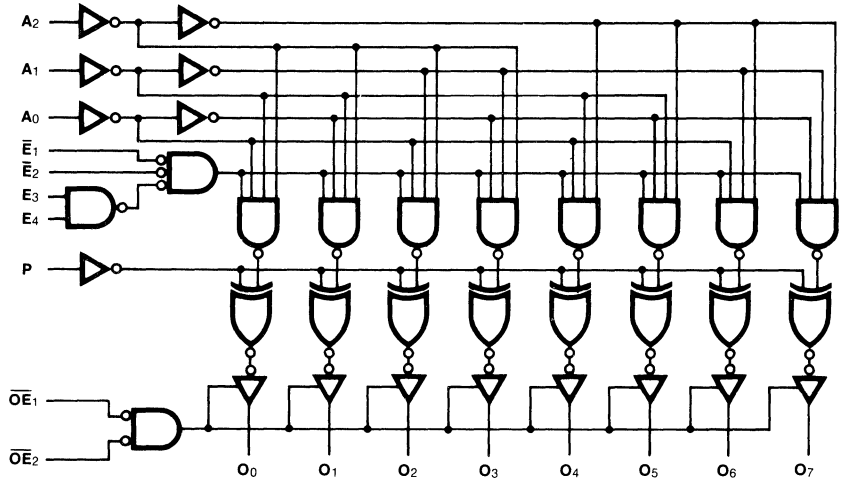
SYMBOL	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
A_0 — A_2	Address Inputs	0.5/0.375
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)	0.5/0.375
E_3, E_4	Enable Inputs (Active HIGH)	0.5/0.375
P	Polarity Control Input	0.5/0.375
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Inputs (Active LOW)	0.5/0.375
O_0 — O_7	3-State Outputs	25/12.5

TRUTH TABLE

FUNCTION	INPUTS									OUTPUTS							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
High Impedance	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	X	X	X	Outputs Equal P Input							
	L	L	X	H	X	X	X	X	X								
	L	L	X	X	L	X	X	X	X								
	L	L	X	X	X	L	X	X	X								
Active-HIGH Output (P = L)	L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H
Active-LOW Output (P = H)	L	L	L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current (All Outputs OFF)		38		mA	$A_0 - A_2$, $\bar{E}_1$, $\bar{E}_2$ = Gnd $\overline{OE}_1$, $\overline{OE}_2$, E_3, E_4, P = HIGH

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n		12.5 11.5						ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay $\bar{E}_1$ or $\bar{E}_2$ to O_n		11.5 11							
t_{PLH} t_{PHL}	Propagation Delay E_3 or E_4 to O_n		14 14.5						ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay P to O_n		13 12							
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_1$ or $\overline{OE}_2$ to O_n		5.0 5.5						ns	2-25 2-26 2-27
t_{PHZ} t_{PLZ}	Output Disable Time* $\overline{OE}_1$ or $\overline{OE}_2$ to O_n		5.0 5.5							

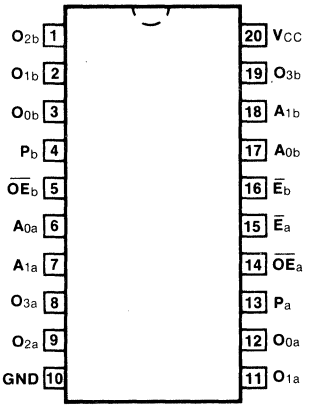
*C_L = 5.0 pF

54F/74F539

DUAL 1-of-4 DECODER

(With 3-State Outputs)

CONNECTION DIAGRAM



DESCRIPTION — The 'F539 contains two independent decoders. Each accepts two Address (A_0, A_1) input signals and decodes them to select one of four mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active-HIGH (P = L) or active-LOW (P = H). An active-LOW input Enable ($\overline{E}$) is available for data demultiplexing; data is routed to the selected output in non-inverted form in the active-LOW mode or in inverted form in the active-HIGH mode. A HIGH signal on the active-LOW Output Enable ($\overline{OE}$) input forces the 3-state outputs to the high impedance state.

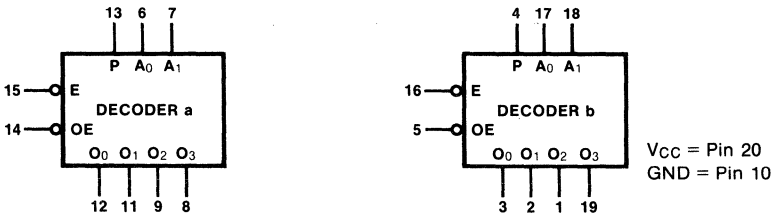
ORDERING CODE: See Section 5

PKGS	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	74F539PC		9Z
Ceramic DIP (D)	74F539DC	54F539DM	4E
Flatpak (F)	74F539FC	54F539FM	4F

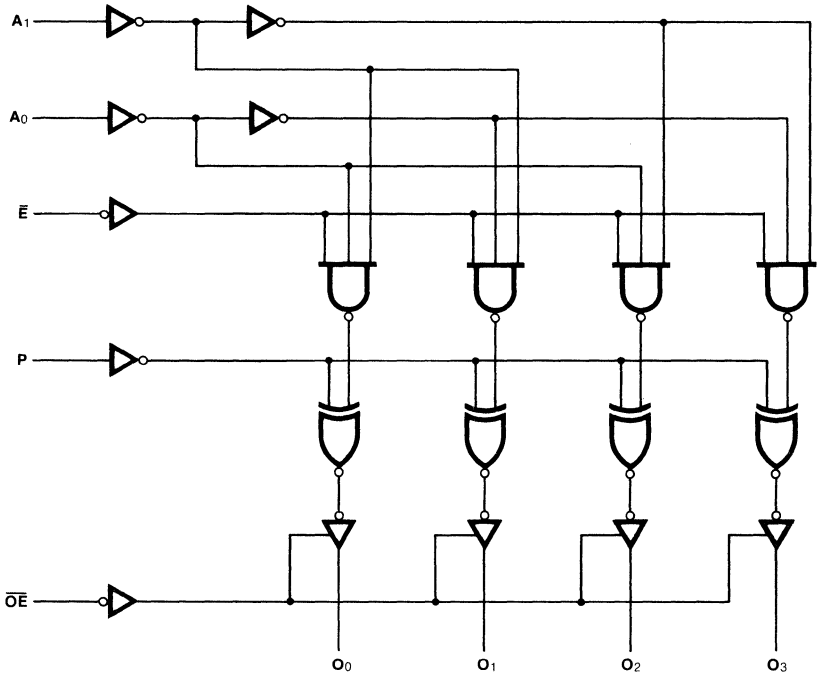
INPUT LOADING/FAN-OUT: See Section 2 for U.L. definitions

PIN NAMES	DESCRIPTION	54F/74F (U.L.) HIGH/LOW
A_{0a} — A_{1a}	Side A Address Inputs	0.5/0.375
A_{0b} — A_{1b}	Side B Address Inputs	0.5/0.375
$\overline{E}_a$, $\overline{E}_b$	Enable Inputs (Active LOW)	0.5/0.375
$\overline{OE}_a$, $\overline{OE}_b$	Output Enable Inputs (Active LOW)	0.5/0.375
P_a, P_b	Polarity Control Inputs	0.5/0.375
O_{0a} — O_{3a}	Side A 3-State Outputs	25/12.5
O_{0b} — O_{3b}	Side B 3-State Outputs	25/12.5

LOGIC SYMBOL



LOGIC DIAGRAM (one half shown)



Please note that this diagram is provided only for tne understanding of logic operations and should not be used to estimate propagation delays.

TRUTH TABLE (each half)

FUNCTION	INPUTS				OUTPUTS			
	$\overline{OE}$	$\overline{E}$	A_1	A_0	O_0	O_1	O_2	O_3
High Impedance	H	X	X	X	Z	Z	Z	Z
Disable	L	H	X	X	$O_n = P$			
Active-HIGH Output (P = L)	L	L	L	L	H	L	L	L
	L	L	L	H	L	H	L	L
	L	L	H	L	L	L	H	L
	L	L	H	H	L	L	L	H
Active-LOW Output (P = H)	L	L	L	L	L	H	H	H
	L	L	L	H	H	L	H	H
	L	L	H	L	H	H	L	H
	L	L	H	H	H	H	H	L

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

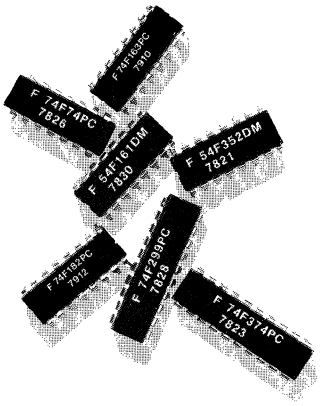
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54F/74F			UNITS	CONDITIONS
		Min	Typ	Max		
I_{CC}	Power Supply Current (All Outputs OFF)		42		mA	A_0, A_1, $\overline{E}$ = Gnd $\overline{OE}$, P = HIGH

AC CHARACTERISTICS: See Section 2 for waveforms and load configurations

SYMBOL	PARAMETER	54F/74F T_A = +25°C, V_{CC} = +5.0 V, C_L = 15 pF			54F T_A, V_{CC} = MIL, C_L = 50 pF		74F T_A, V_{CC} = COM, C_L = 50 pF		UNITS	FIG. NO.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n		12.5 11.5						ns	2-17 2-23
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to O_n		11.5 11							
t_{PLH} t_{PHL}	Progagation Delay P to O_n		13 12						ns	2-17 2-23
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to O_n		5.0 5.5						ns	2-25 2-26
t_{PHZ} t_{PLZ}	Output Disable Time* $\overline{OE}$ to O_n		5.0 5.0							2-27

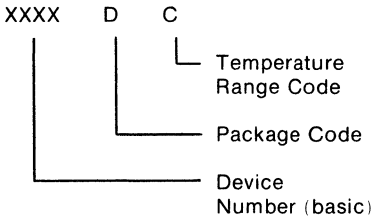
*C_L = 5.0 pF



Section 5

Ordering Information/ Package Outlines

Specific ordering codes, as well as the temperature ranges and package types available, are listed on each data sheet in Section 4. The Product Index and Selection Guides given in Sections 1 and 3, respectively, list only the "basic device numbers." This basic number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Temperature Range — Two basic temperature grades are in common use:

C = Commercial
0°C to +70°C

M = Military
-55°C to +125°C

Package Code — One letter represents the basic package type. Different package outlines exist within each package type to accommodate varying die sizes and number of pins, as indicated below:

D — Ceramic/Hermetic Dual In-line
4E, 6A, 6B, 6I, 6N, 7B

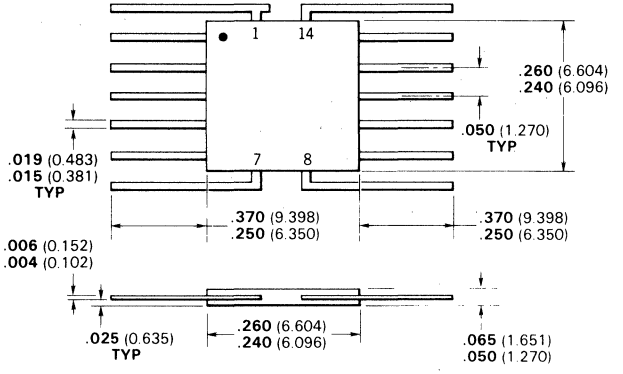
F — Flatpak
3I, 4F, 4L, 4M

P — Plastic Dual In-line
8P, 9A, 9B, 9N, 9Z

Package Outlines — The package outlines indicated by the codes above are shown in the detailed outline drawings in this section.

JEDEC TO-86 Outline

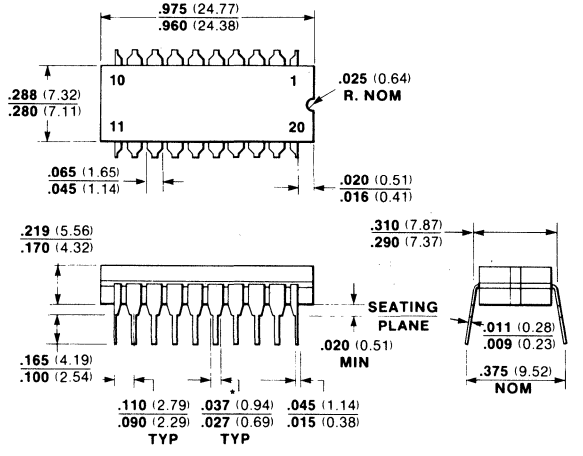
3I



Notes:
Pins are tin-plated 42 alloy
Hermetically sealed alumina package
Pin 1 orientation may be either tab or dot
Cavity size is **.130** (3.30)
Package weight is 0.26 gram

20-Pin CERDIP

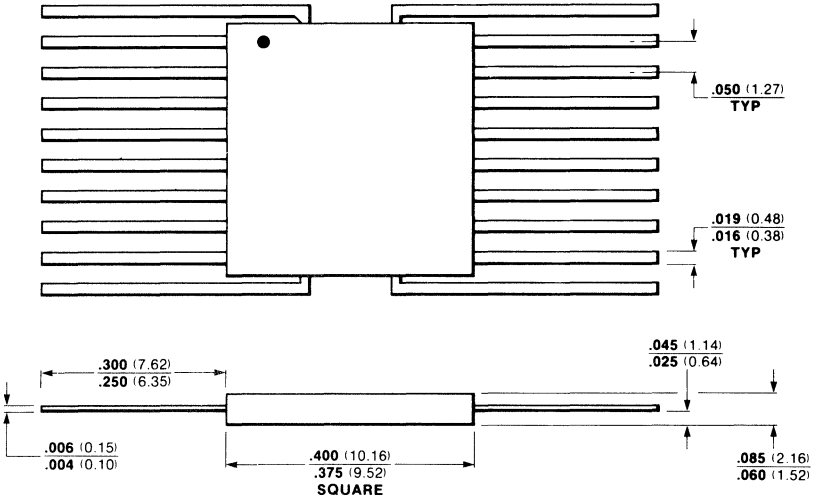
4E



Notes:
Pins are tin-plated kovar or nickel alloy 42
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.030** (0.76) diameter pins
Hermetically sealed alumina package (black)
Cavity size is **.140 x .250** (3.56 x 6.35)
*The **.037-.027** (0.94-0.69) dimension does not apply to the corner pins
Package weight is 2.4 grams

All dimensions in inches (bold) and millimeters (parentheses)

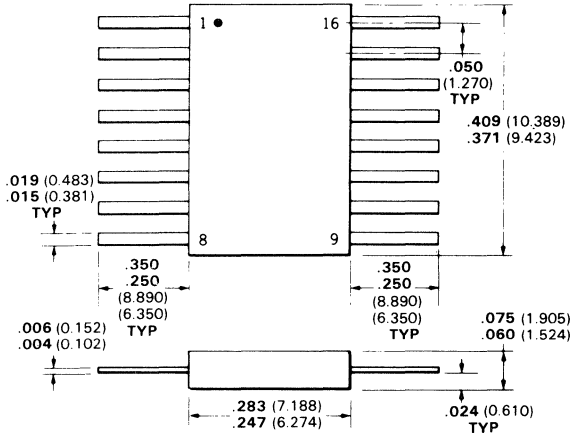
20-Pin CERPAK 4F



Notes:
Pins are tin -plated nickel ally
Base is Al_2O_3
Cavity size **.200 x .200**
Package weight = 0.8 grams

5

16-Pin BeO CERPAK 4L

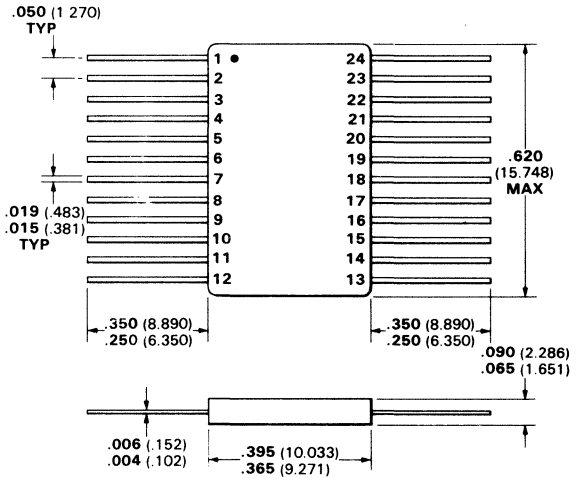


Notes:
Pins are alloy 42
Package weight is 0.4 gram
Hermetically sealed beryllia package

All dimensions in inches (bold) and millimeters (parentheses)

24-Pin CERPAK

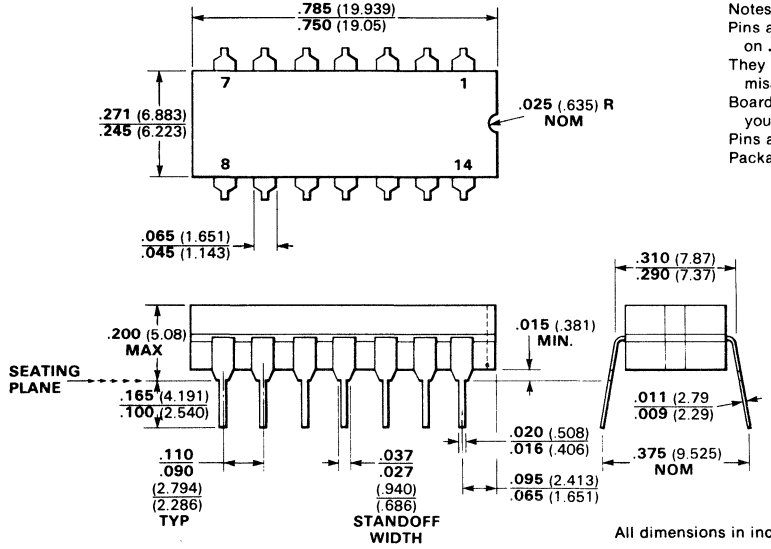
4M



Notes:
Pins are tin-plated nickel alloy
Base is Al_2O_3 or BeO
Cavity size is **.200 x .200**
Package weight is 0.8 grams

14-Pin Hermetic Dual In-Line (JEDEC TO-116 Outline)

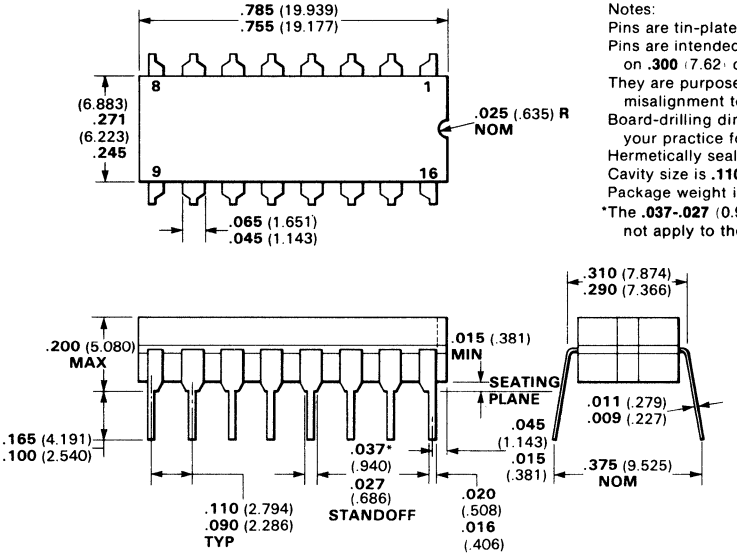
6A



Notes:
Pins are intended for insertion in hole rows on **.300** (7.620) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020** (0.508) diameter pin
Pins are alloy 42
Package weight is 2.0 grams

All dimensions in inches (bold) and millimeters (parentheses)

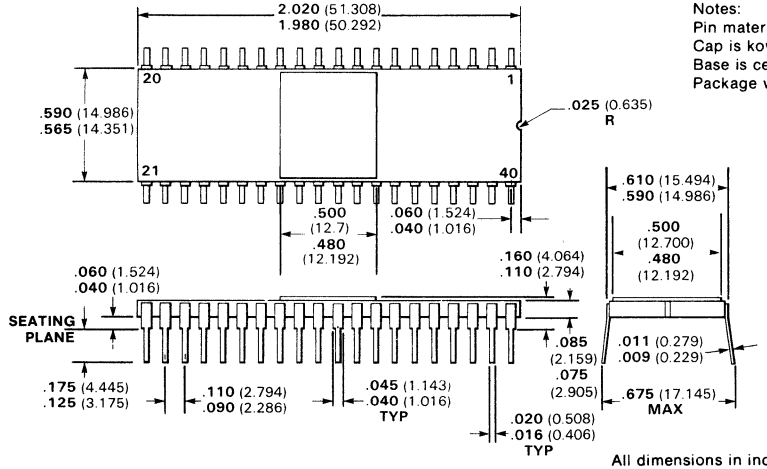
16-Pin Dual In-Line 6B



Notes:
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020** (0.51) diameter pin
Hermetically sealed alumina package
Cavity size is **.110 x .140** (2.79 x 3.56)
Package weight is 2.0 grams
*The **.037-.027** (0.94-069) dimension does not apply to the corner pins

5

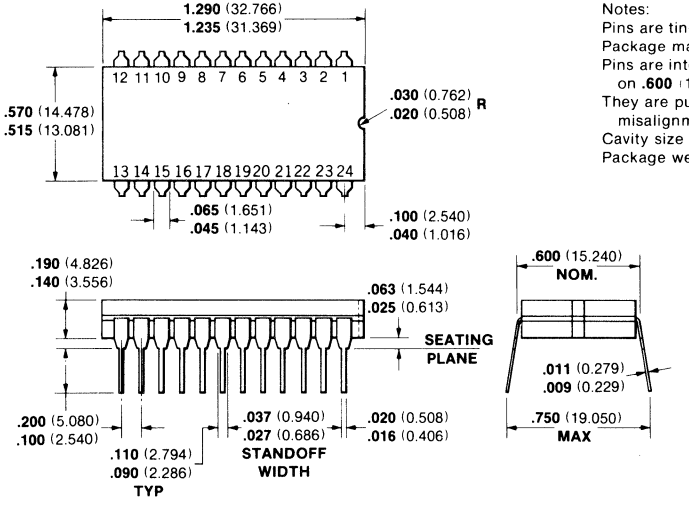
40-Pin Dual In-Line Side-Brazed Dual In-Line 6I



Notes:
Pin material nickel gold-plated kovar
Cap is kovar
Base is ceramic
Package weight is 6.5 grams

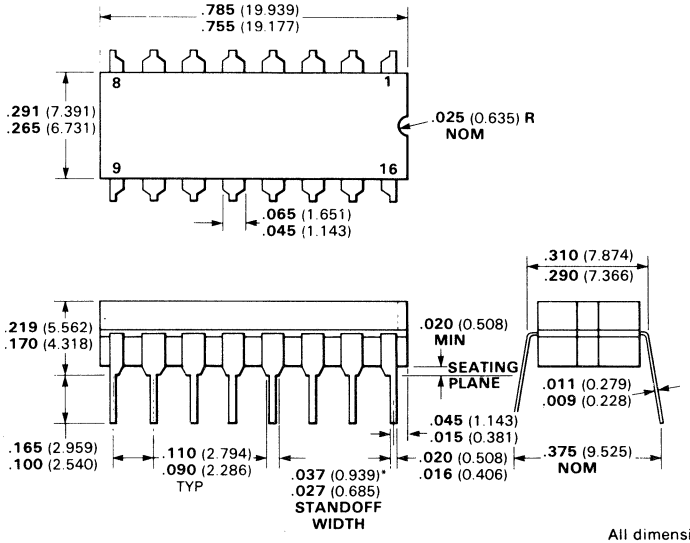
All dimensions in inches (bold) and millimeters (parentheses)

24-Pin Dual In-Line 6N



Notes:
Pins are tin-plated 42 alloy
Package material is alumina
Pins are intended for insertion in hole rows on **.600** (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Cavity size is **.230 x .230** (5.84 x 5.84)
Package weight is 6.5 grams

16-Pin Dual In-Line 7B

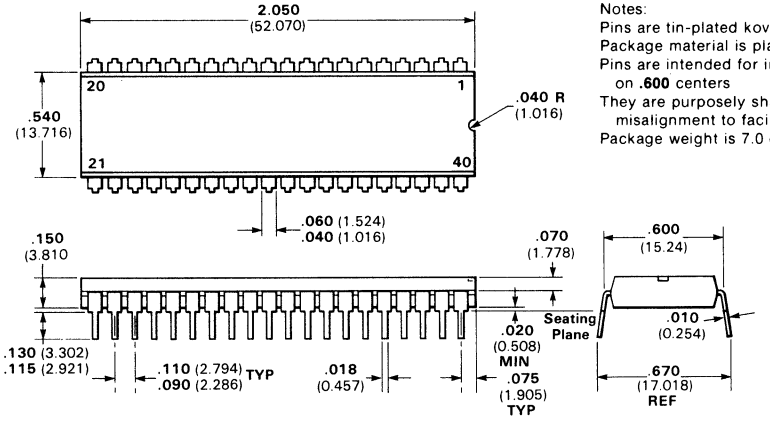


Notes:
Pins are tin-plated 42 alloy
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020** (0.51) diameter pin
Hermetically sealed alumina package
Cavity size is **.130 x .230**
*The **.037-.027** (0.94-0.69) dimension does not apply to the corner pins
Package weight is 2.2 grams

All dimensions in inches (bold) and millimeters (parentheses)

40-Pin Plastic Dual In-Line

8P

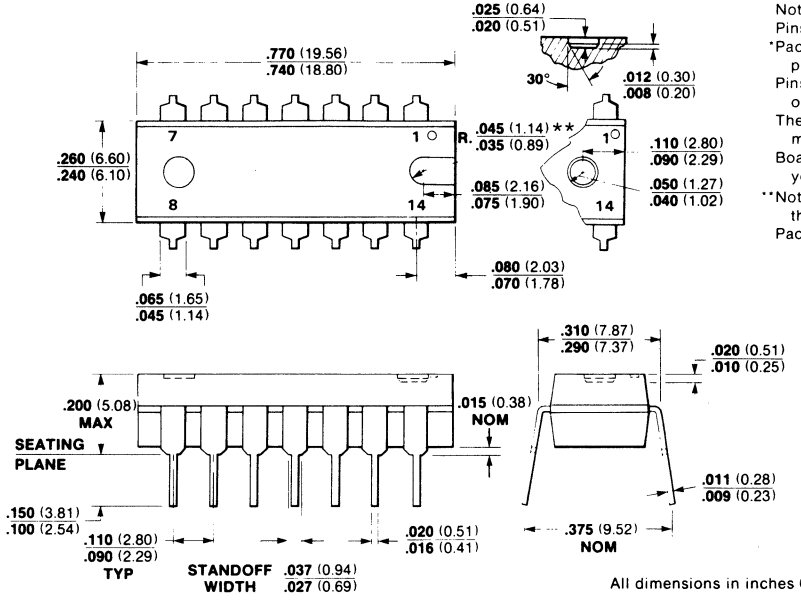


Notes:
Pins are tin-plated kovar
Package material is plastic
Pins are intended for insertion in hole rows on **.600** centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Package weight is 7.0 grams

5

14-Pin Plastic* Dual In-Line (JEDEC TO-116 Outline)

9A

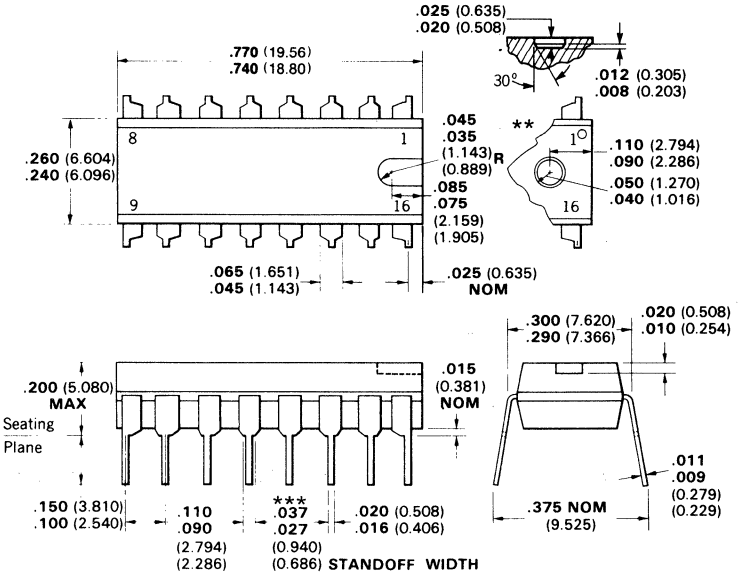


Notes:
Pins are tin-plated kovar
*Package material varies depending on the product line
Pins are intended for insertion in hole rows on **.300** 7.62 centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020** 0.508 diameter pin
**Notch or ejector hole varies depending on the product line
Package weight is 0.9 grams

All dimensions in inches (bold) and millimeters (parentheses)

16-Pin Plastic* Dual In-Line

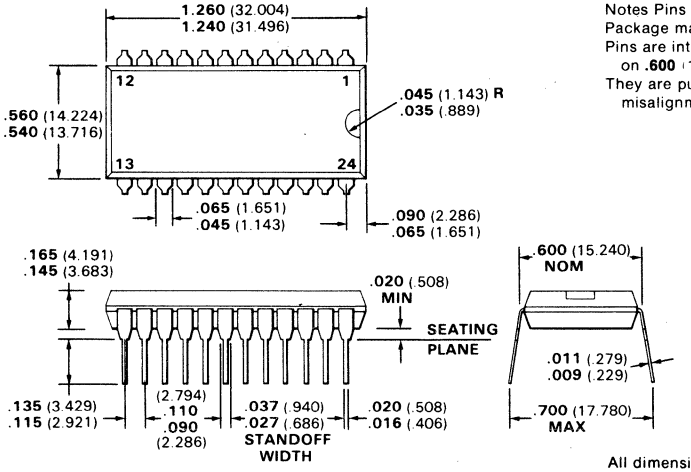
9B



Notes:
Pins are tin-plated kovar or alloy 42 nickel
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board drilling dimensions should equal your practice for **.0210** (0.51) diameter pin
Package weight is 0.9 grams
*Package material varies depending on the product line
***The **.037-0.27** (0.94-0.69) dimension does not apply to the corner pins
***Notch or ejector hole varies depending on the product line

24-Pin Plastic Dual In-Line

9N

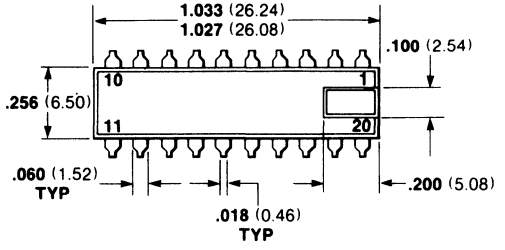


Notes Pins are tin-plated kovar
Package material is plastic
Pins are intended for insertion in hole rows on **.600** (15.24) centers
They are purposely shipped with "positive" misalignment to facilitate insertion

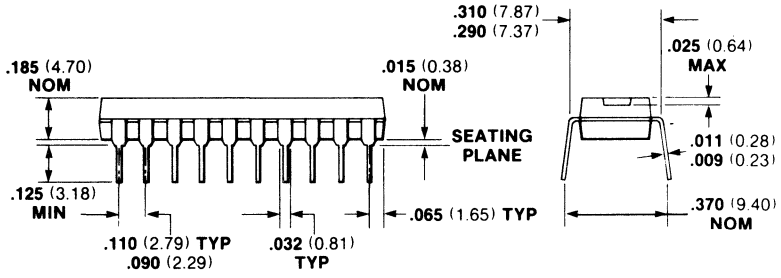
All dimensions in inches (bold) and millimeters (parentheses)

20-Pin Plastic Dual In-Line

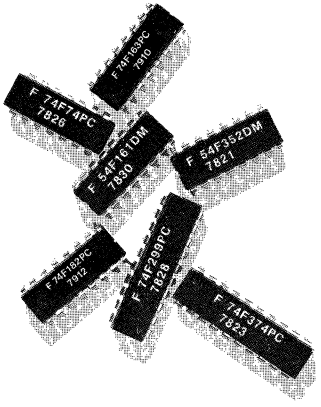
9Z



Notes:
Pins are tin-plated alloy 42 copper (olin 195)
Package material varies depending on the product line
Pins are intended for insertion in hole rows on **.300** (7.62) centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for **.020** (0.51) diameter pin
Package weight is a little over 1.0 gram



All dimensions in inches (bold) and millimeters (parentheses)



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Tel: 714-979-6864

Hamilton Electro Sales
10912 W. Washington Blvd.
Culver City, California 90230
Tel: 213-558-2121 TWX: 910-340-6364

Hamilton/Avnet Electronics
1175 Bordeaux Drive
Sunnyvale, California 94086
Tel: 408-743-3355 TWX: 910-379-6486

Hamilton/Avnet Electronics
4545 Viewridge Avenue
San Diego, California 92123
Tel: 714-571-7527
Telex: HAMAVELEC SDG 69-5415

Anthem Electronics
1020 Stewart Drive
P.O. Box 9085
Sunnyvale, California 94086
Tel: 408-738-1111

Anthem Electronics, Inc.
4040 Sorrento Valley Blvd.
San Diego, California 92121
Tel: 714-279-5200

Anthem Electronics, Inc.
2661 Dow Avenue
Tustin, California 92680
Tel: 714-730-8000

Wyle Electronics
124 Maryland Street
El Segundo, California 90245
Tel: 213-322-8100 TWX: 910-348-7111

Wyle Distributor Group
17872 Cowan Avenue
Irvine, California 92714
Tel: 714-641-1600
Telex: 910-595-1572

**This distributor carries Fairchild *die* products only.

**Sertech Laboratories
2120 Main Street, Suite 190
Huntington Beach, California 92647
Tel: 714-960-1403

Wyle Distribution Group
9525 Chesapeake
San Diego, California 92123
Tel: 714-565-9171 TWX: 910-335-1590

Colorado
Bell Industries
8155 West 48th Avenue
Wheatridge, Colorado 80033
Tel: 303-424-1985 TWX: 910-938-0393

Arrow Electronics
2121 South Hudson
Denver, Colorado 80222
Tel: 303-758-2100

Wyle Distribution Group
6777 E. 50th Avenue
Commerce City, Colorado 80022
Tel: 303-287-9611 TWX: 910-936-0770

Hamilton/Avnet Electronics
8765 E. Orchard Rd., Suite 708
Englewood, Colorado 80111
Tel: 303-740-1000 TWX: 910-931-0510

Connecticut
Arrow Electronics, Inc.
12 Beaumont Road
Wallingford, Connecticut 06492
Tel: 203-265-7741 TWX: 710-465-0780

Hamilton/Avnet Electronics
643 Danbury Road
Georgetown, Connecticut 06829
Tel: 203-762-0361
TWX: None — use 710-897-1405
(Regional Hq. in Mt. Laurel, N.J.)

Harvey Electronics
112 Main Street
Norwalk, Connecticut 06851
Tel: 203-853-1515

Schweber Electronics
Finance Drive
Commerce Industrial Park
Danbury, Connecticut 06810
Tel: 203-792-3500

Florida
Arrow Electronics
1001 Northwest 62nd Street
Suite 402
Ft. Lauderdale, Florida 33309
Tel: 305-776-7790

Arrow Electronics
115 Palm Bay Road N.W.
Suite 10 Bldg. #200
Palm Bay, Florida 32905
Tel: 305-725-1408

Hallmark Electronics
1671 W. McNab Road
Ft. Lauderdale, Florida 33309
Tel: 305-971-9280 TWX: 510-956-3092

Hallmark Electronics
7233 Lake Ellenor Drive
Orlando, Florida 32809
Tel: 305-855-4020 TWX: 810-850-0183

Hamilton/Avnet Electronics
6800 N.W. 20th Avenue
Ft. Lauderdale, Florida 33309
Tel: 305-971-2900 TWX: 510-954-9808

Hamilton/Avnet Electronics
3197 Tech Drive, North
St. Petersburg, Florida 33702

Schweber Electronics
2830 North 28th Terrace
Hollywood, Florida 33020
Tel: 305-927-0511 TWX: 510-954-0304

Georgia
Arrow Electronics
2979 Pacific Drive
Norcross, Georgia 30071
Tel: 404-449-8252
Telex: 810-766-0439

Hamilton/Avnet Electronics
6700 Interstate 85 Access Road, Suite 1E
Norcross, Georgia 30071
Tel: 404-448-0800
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

Illinois
Hallmark Electronics, Inc.
1177 Industrial Drive
Bensenville, Illinois 60106
Tel: 312-860-3800

Hamilton/Avnet Electronics
3901 N. 25th Avenue
Schiller Park, Illinois 60176
Tel: 312-678-6310 TWX: 910-227-0060

Kierulff Electronics
1536 Landmeier Road
Elk Grove Village, Illinois 60007
Tel: 312-640-0200 TWX: 910-227-3166

Schweber Electronics, Inc.
1275 Brummel Avenue
Elk Grove Village, Illinois 60007
Tel: 312-593-2740 TWX: 910-222-3453

Semiconductor Specialists, Inc.
(mailing address)
O'Hare International Airport
P.O. Box 66125
Chicago, Illinois 60666

(shipping address)
195 Spangler Avenue
Elmhurst Industrial Park
Elmhurst, Illinois 60126
Tel: 312-279-1000 TWX: 910-254-0169

Indiana
Graham Electronics Supply, Inc.
133 S. Pennsylvania St.
Indianapolis, Indiana 46204
Tel: 317-634-8486 TWX: 810-341-3481

Pioneer Indiana Electronics, Inc.
6408 Castle Place Drive
Indianapolis, Indiana 46250
Tel: 317-849-7300 TWX: 810-260-1794

Kansas
Hallmark Electronics, Inc.
11870 W. 91st Street
Shawnee Mission, Kansas 66214
Tel: 913-888-4746

Hamilton/Avnet Electronics
9219 Guivira Road
Overland Park, Kansas 66215
Tel: 913-888-8900
Telex: None — use HAMAVLECB DAL 73-0511
(Regional Hq. in Dallas, Texas)

Louisiana
Sterling Electronics Corp.
4613 Fairfield
Metairie, Louisiana 70002
Tel: 504-887-7610
Telex: STERLE LEC MRIE 58-328

Maryland
Hallmark Electronics, Inc.
6655 Amberton Drive
Baltimore, Maryland 21227
Tel: 301-796-9300

Hamilton/Avent Electronics
(mailing address)
Friendship International Airport
P.O. Box 8647
Baltimore, Maryland 21240

(shipping address)
7235 Standard Drive
Hanover, Maryland 21076
Tel: 301-796-5000 TWX: 710-862-1861
Telex: HAMAVLECA HNVE 87-968

Pioneer Washington Electronics, Inc.
9100 Gaither Road
Gaithersburg, Maryland 20760
Tel: 301-948-0710 TWX: 710-828-9784

Schweber Electronics
9218 Gaither Road
Gaithersburg, Maryland 20760
Tel: 301-840-5900 TWX: 710-828-0536

Massachusetts
Arrow Electronics, Inc.
96 D Commerce Way
Woburn, Massachusetts 01801
Tel: 617-933-8130 TWX: 710-393-6770

Arrow Electronics
85 Wells Avenue
Newton Centre, Massachusetts 02159
Tel: 617-964-4000

Gerber Electronics
128 Carnegie Row
Norwood, Massachusetts 02026
Tel: 617-329-2400

Hamilton/Avnet Electronics
50 Tower Office Park
Woburn, Massachusetts 01801
Tel: 617-273-7500 TWX: 710-393-0382

Harvey Electronics
44 Hartwell Avenue
Lexington, Massachusetts 02173
Tel: 617-861-9200 TWX: 710-326-6617

Schweber Electronics
25 Wiggins Avenue
Bedford, Massachusetts 01730
Tel: 617-275-5100

**Sertech Laboratories
1 Peabody Street
Salem, Massachusetts 01970
Tel: 617-745-2450

Michigan
Hamilton/Avnet Electronics
32487 Schoolcraft
Livonia, Michigan 48150
Tel: 313-522-4700 TWX: 810-242-8775

Pioneer/Detroit
13485 Stamford
Livonia, Michigan 48150
Tel: 313-525-1800

R-M Electronics
4310 Roger B. Chaffee
Wyoming, Michigan 49508
Tel: 616-531-9300

Schweber Electronics
33540 Schoolcraft
Livonia, Michigan 48150
Tel: 313-525-8100

Arrow Electronics
3921 Varsity Drive
Ann Arbor, Michigan 48104
Tel: 313-971-8220

Minnesota
Arrow Electronics
5230 West 73rd Street
Edina, Minnesota 55435
Tel: 612-830-1800

Hamilton/Avnet Electronics
7449 Cahill Road
Edina, Minnesota 55435
Tel: 612-941-3801
TWX: None — use 910-227-0060
(Regional Hq. in Chicago, Ill.)

Schweber Electronics
7402 Washington Avenue S.
Eden Prairie, Minnesota 55344
Tel: 612-941-5280

Missouri
Hallmark Electronics, Inc.
13789 Rider Trail
Earth City, Missouri 63045
Tel: 314-291-5350

Hamilton/Avnet Electronics
13743 Shoreline Ct., East
Earth City, Missouri 63042
Tel: 314-344-1200 TWX: 910-762-0684

New Jersey
Hamilton/Avnet Electronics
10 Industrial Road
Fairfield, New Jersey 07006
Tel: 201-575-3390 TWX: 710-994-5787

Hamilton/Avnet Electronics
#1 Keystone Avenue
Cherry Hill, New Jersey 08003
Tel: 609-424-0100 TWX: 710-940-0262

Schweber Electronics
18 Madison Road
Fairfield, New Jersey 07006
Tel: 201-227-7880 TWX: 710-480-4733

Sterling Electronics
774 Pfeiffer Blvd.
Perth Amboy, N.J. 08861
Tel: 201-442-8000 Telex: 138-679

Wilshire Electronics
102 Gaither Drive
Mt. Laurel, N.J. 08057
Tel: 215-627-1920

Wilshire Electronics
1111 Paulison Avenue
Clifton, N.J. 07015
Tel: 201-365-2600 TWX: 710-989-7052

New Mexico
Bell Industries
11728 Linn Avenue N.E.
Albuquerque, New Mexico 87123
Tel: 505-292-2700 TWX: 910-989-0625

Hamilton/Avnet Electronics
2450 Byalor Drive S.E.
Albuquerque, New Mexico 87119
Tel: 505-765-1500
TWX: None — use 910-379-6486
(Regional Hq. in Mt. View, Ca.)

New York
Arrow Electronics
20 Oser Avenue
Hauppauge, New York 11787
Tel: 516-231-1000

*Cadence Electronics
40-17 Oser Avenue
Hauppauge, New York 11787
Tel: 516-231-6722

Arrow Electronics
P.O. Box 370
7705 Maltlage Drive
Liverpool, New York 13088
Tel: 315-652-1000
TWX: 710-545-0230

Components Plus, Inc.
40 Oser Avenue
Hauppauge, L.I., New York 11787
Tel: 516-231-9200 TWX: 510-227-9869

Hamilton/Avnet Electronics
167 Clay Road
Rochester, New York 14623
Tel: 716-442-7820
TWX: None — use 710-332-1201
(Regional Hq. in Burlington, Ma.)

Hamilton/Avnet Electronics
16 Corporate Circle
E. Syracuse, New York 13057
Tel: 315-437-2642 TWX: 710-541-0959

Hamilton/Avnet Electronics
5 Hub Drive
Melville, New York 11746
Tel: 516-454-6000 TWX: 510-224-6166

Harvey Electronics
(mailing address)
P.O. Box 1208
Binghampton, New York 13902
(shipping address)
1911 Vestal Parkway East
Vestal, New York 13850
Tel: 607-748-8211

Rochester Radio Supply Co., Inc.
140 W. Main Street
(P.O. Box 1971) Rochester, New York 14603
Tel: 716-454-7800

Schweber Electronics
Jericho Turnpike
Westbury, L.I., New York 11590
Tel: 516-334-7474 TWX: 510-222-3660

Jaco Electronics, Inc
145 Oser Avenue
Hauppauge, L.I., New York 11787
Tel: 516-273-1234 TWX: 510-227-6232

Summit Distributors, Inc
916 Main Street
Buffalo, New York 14202
Tel: 716-884-3450 TWX: 710-522-1692

North Carolina
Arrow Electronics
938 Burke Street
Winston Salem, North Carolina 27102
Tel: 919-725-8711 TWX: 510-922-4765

Hamilton/Avnet
2803 Industrial Drive
Raleigh, North Carolina 27609
Tel: 919-829-8030

Hallmark Electronics
1208 Front Street, Bldg. K
Raleigh, North Carolina 27609
Tel: 919-823-4465 TWX: 510-928-1831

Resco
Highway 70 West
Rural Route 8, P.O. Box 116-B
Raleigh, North Carolina 27612
Tel: 919-781-5700

Pioneer/Carolina Electronics
103 Industrial Drive
Greensboro, North Carolina 27406
Tel: 919-273-4441

Ohio
Arrow Electronics
3100 Plainfield Road
Dayton, Ohio 45432
Tel: 513-253-9176

Hamilton/Avnet Electronics
4588 Emery Industrial Parkway
Cleveland, Ohio 44128
Tel: 216-831-3500
TWX: None — use 910-227-0060
(Regional Hq. in Chicago, Ill.

Hamilton/Avnet Electronics
954 Senate Drive
Dayton, Ohio 45459
Tel: 513-433-0610 TWX: 810-450-2531

Pioneer/Cleveland
4800 E. 131st Street
Cleveland, Ohio 44105
Tel: 216-587-3600

Pioneer/Dayton
1900 Troy Street
Dayton, Ohio 45404
Tel: 513-236-9900 TWX: 810-459-1622

Schweber Electronics
23880 Commerce Park Road
Beachwood, Ohio 44122
Tel: 216-464-2970 TWX: 810-427-9441

Arrow Electronics
6238 Cochran Road
Solon, Ohio 44139
Tel: 216-248-3990 TWX: 810-427-9409

Arrow Electronics
(mailing address)
P.O. Box 37826
Cincinnati, Ohio 45222
(shipping address)
10 Knollcrest Drive
Reading, Ohio 45237
Tel: 513-761-5432 TWX: 810-461-2670

*Minority Distributor

**This distributor carries Fairchild *die* products only.

Oklahoma
Hallmark Electronics
5460 S. 103rd East Avenue
Tulsa, Oklahoma 74145
Tel: 918-835-8458 TWX: 910-845-2290

Radio Inc. Industrial Electronics
1000 S. Main
Tulsa, Oklahoma 74119
Tel: 918-587-9123

Pennsylvania
Hallmark Electronics, Inc.
458 Pike Road
Huntingdon Valley, Pennsylvania 19006
Tel: 215-355-7300 TWX: 510-667-1727

Pioneer/Delaware Valley Electronics
261 Gibraltar Road
Horsham, Pennsylvania 19044
Tel: 215-674-4000 TWX: 510-665-6778

Pioneer Electronics, Inc.
560 Alpha Drive
Pittsburgh, Pennsylvania 15238
Tel: 412-782-2300 TWX: 710-795-3122

Schweber Electronics
101 Rock Road
Horsham, Pennsylvania 19044
Tel: 215-441-0600

Arrow Electronics
4297 Greensburgh Pike
Suite 314
Pittsburgh, Pennsylvania 15221
Tel: 412-351-4000

South Carolina
Dixie Electronics, Inc.
P.O. Box 408 (Zip Code 29202)
1900 Barnwell Street
Columbia, South Carolina 29201
Tel: 803-779-5332

Texas
Allied Electronics
401 E. 8th Street
Fort Worth, Texas 76102
Tel: 817-336-5401

Arrow Electronics
13715 Gamma Road
Dallas, Texas 75234
Tel: 214-386-7500 TWX: 910-860-5377

Hallmark Electronics Corp.
10109 McKalla Place Suite F
Austin, Texas 78758
Tel: 512-837-2814

Hallmark Electronics
11333 Pagemill Drive
Dallas, Texas 75243
Tel: 214-234-7300 TWX: 910-867-4721

Hallmark Electronics, Inc.
8000 Westglen
Houston, Texas 77063
Tel: 713-781-6100

Hamilton/Avnet Electronics
10508A Boyer Boulevard
Austin, Texas 78758
Tel: 512-837-8911

Hamilton/Avnet Electronics
4445 Sigma Road
Dallas, Texas 75240
Tel: 214-661-8661
Telex: HAMAVLECB DAL 73-0511

Hamilton/Avnet Electronics
3939 Ann Arbor
Houston, Texas 77042
Tel: 713-780-1771
Telex: HAMAVLECB HOU 76-2589

Schweber Electronics, Inc.
14177 Proton Road
Dallas, Texas 75240
Tel: 214-661-5010 TWX: 910-860-5493

Schweber Electronics, Inc.
7420 Harwin Drive
Houston, Texas 77036
Tel: 713-784-3600 TWX: 910-881-1109

Sterling Electronics
4201 Southwest Freeway
Houston, Texas 77027
Tel: 713-627-9800 TWX: 901-881-504
Telex: STELECO HOUA 77-5299

Utah
Bell Industries
3639 W. 2150 South
Salt Lake City, Utah 84120
Tel: 801-972-6969 TWX: 910-925-5686

Hamilton/Avnet Electronics
1585 W. 2100 South
Salt Lake City, Utah 84119
Tel: 801-972-2800
TWX: None — use 910-379-6486
(Regional Hq. in Mt. View, Ca.)

Washington
Hamilton/Avnet Electronics
14212 N.E. 21st Street
Bellevue, Washington 98005
Tel: 206-746-8750 TWX: 910-443-2449

Wyle Distribution Group
1750 132nd Avenue N.E.
Bellevue, Washington 98005
Tel: 206-453-8300 TWX: 910-444-1379

Radar Electronic Co., Inc.
168 Western Avenue W.
Seattle, Washington 98119
Tel: 206-282-2511 TWX: 910-444-2052

Wisconsin
Hamilton/Avnet Electronics
2975 Moorland Road
New Berlin, Wisconsin 53151
Tel: 414-784-4510 TWX: 910-262-1182

Marsh Electronics, Inc.
1563 South 100st Street
Milwaukee, Wisconsin 53214
Tel: 414-475-6000 TWX: 910-262-3321

Canada
Cam Gard Supply Ltd.
640 42nd Avenue S.E.
Calgary, Alberta, T2G 1Y6, Canada
Tel: 403-287-0520 Telex: 03-822811

Cam Gard Supply Ltd.
16236 116th Avenue
Edmonton, Alberta T5M 3V4, Canada
Tel: 403-453-6691 Telex: 03-72960

Cam Gard Supply Ltd.
4910 52nd Street
Red Deer, Alberta, T4N 2C8, Canada
Tel: 403-346-2088

Cam Gard Supply Ltd.
825 Notre Dame Drive
Kamloops, British Columbia, V2C 5N8, Canada
Tel: 604-372-3338

Cam Gard Supply Ltd.
1777 Ellice Avenue
Winnepeg, Manitoba, R3H 0W5, Canada
Tel: 204-786-8401 Telex: 07-57622

Cam Gard Supply Ltd.
Rookwood Avenue
Fredericton, New Brunswick, E3B 4Y9, Canada
Tel: 506-455-8891

Cam Gard Supply Ltd.
15 Mount Royal Blvd.
Moncton, New Brunswick, E1C 8N6, Canada
Tel: 506-855-2200

Cam Gard Supply Ltd.
3065 Robie Street
Halifax, Nova Scotia, B3K 4P6, Canada
Tel: 902-454-8581 Telex: 01-921528

Cam Gard Supply Ltd.
1303 Scarth Street
Regina, Saskatchewan, S4R 2E7, Canada
Tel: 306-525-1317 Telex: 07-12667

Cam Gard Supply Ltd.
1501 Ontario Avenue
Saskatoon, Saskatchewan, S7K 1S7, Canada
Tel: 306-652-6424 Telex: 07-42825

Electro Sonic Industrial Sales
(Toronto) Ltd.
1100 Gordon Baker Rd
Willowdale, Ontario, M2H 3B3, Canada
Tel: 416-494-1666
Telex: ESSCO TOR 06-22030

Future Electronics Inc
Baxter Center
1050 Baxter Road
Ottawa, Ontario, K2C 3P2, Canada
Tel: 613-820-9471

Future Electronics Inc.
4800 Dufferin Street
Downsview, Ontario, M3H 5S8, Canada
Tel: 416-663-5563

Future Electronics Corporation
5647 Ferrier Street
Montreal, Quebec, H4P 2K5, Canada
Tel: 514-731-7441

Hamilton/Avnet International
(Canada) Ltd.
3688 Nashua Drive, Units 6 & H
Mississauga, Ontario, L4V 1M5, Canada
Tel: 416-677-7432 TWX: 610-492-8867

Hamilton/Avnet International
(Canada) Ltd.
1735 Courtwood Crescent
Ottawa, Ontario, K1Z 5L9, Canada
Tel: 613-226-1700

Hamilton/Avnet International
2670 Sabourin Street
St. Laurent, Quebec
H4S 1M2, Canada
Tel: 514-331-6443 TWX: 610-421-3731

R.A.E. Industrial Electronics, Ltd.
3455 Gardner Court
Burnaby, British Columbia Z5G 4J7
Tel: 604-291-8866 TWX: 610-929-3065
Telex: RAE-VCR 04-54550

Semad Electronics Ltd.
620 Meloche Avenue
Dorval, Quebec, H9P 2P4, Canada
Tel: 604-2998-866 TWX: 610-422-3048

Semad Electronics Ltd.
105 Brisbane Avenue
Downsview, Ontario, M3J 2K6, Canada
Tel: 416-663-5670 TWX: 610-492-2510

Semad Electronics Ltd.
1485 Laperriere Avenue
Ottawa, Ontario, K1Z 7S8, Canada
Tel: 613-722-6571 TWX: 610-562-8966

Fairchild Semiconductor Sales Representatives

United States and Canada

Alabama
Cartwright & Bean, Inc.
2400 Bob Wallace Ave., Suite 201
Huntsville, Alabama 35805
Tel: 205-533-3509

California
Celtec Company
18009 Sky Park Circle Suite B
Irvine, California 92714
Tel: 714-557-5021 TWX: 910-595-2512

Celtec Company
7867 Convoy Court, Suite 312
San Diego, California 92111
Tel: 714-279-7961 TWX: 910-335-1512

Magna Sales, Inc.
3333 Bowers Avenue
Suite 295
Santa Clara, California 95051
Tel: 408-985-1750 TWX: 910-338-0241

Colorado
Simpson Associates, Inc.
2552 Ridge Road
Littleton, Colorado 80120
Tel: 303-794-8381 TWX: 910-935-0719

Connecticut
Phoenix Sales Company
389 Main Street
Ridgefield, Connecticut 06877
Tel: 203-438-9644 TWX: 710-467-0662

Florida
Lectromech, Inc.
399 Whooping Loop
Altamonte Springs, Florida 32701
Tel: 305-831-1577 TWX: 810-853-0262

Lectromech, Inc.
2280 U.S. Highway 19 North
Suite 119 Bldg. L
Clearwater, Florida 33515
Tel: 813-726-0541
TWX: 810-866-0884

Lectromech, Inc.
17 E. Hibiscus Blvd.
Suite A
Melbourne, Florida 32901
Tel: 305-725-1950
TWX: 810-853-0262

Lectromech, Inc.
1350 S. Powerline Road, Suite 104
Pompano Beach, Florida 33060
Tel: 305-974-6780 TWX: 510-954-9793

Georgia
Cartwright & Bean, Inc.
P.O. Box 52846 (Zip Code 30355)
90 W. Wieuca Square, Suite 155
Atlanta, Georgia 30342
Tel: 404-255-5262 TWX: 810-751-3220

Illinois
Micro Sales, Inc.
2258-B Landmeir Road
Elk Grove Village, Illinois 60007
Tel: 312-956-1000 TWX: 910-222-1833

Maryland
Delta III Associates
1000 Century Plaza Suite 224
Columbia, Maryland 21044
Tel: 301-730-4700 TWX: 710-826-9654

Massachusetts
Spectrum Associates, Inc.
109 Highland Avenue
Needham, Massachusetts 02192
Tel: 617-444-8600 TWX: 710-325-6665

Minnesota
PSI Company
5315 W. 74th Street
Edina, Minnesota 55435
Tel: 612-835-1777 TWX: 910-576-3483

Mississippi
Cartwright & Bean, Inc.
P.O. Box 16728
5150 Keele Street
Jackson, Mississippi 39206
Tel: 601-981-1368
TWX: 810-751-3220

Nevada
Magna Sales
4560 Wagon Wheel Road
Carson City, Nevada 89701
Tel: 702-883-1471

New Jersey
BGR Associates
3001 Greentree Executive Campus
Marlton, New Jersey 08053
Tel: 609-428-2440

Lorac Sales, Inc.
1200 Route 23 North
Butler, New Jersey 07405
Tel: 201-696-8875 TWX: 710-988-5846

New York
Lorac Sales, Inc.
550 Old Country Road, Room 410
Hicksville, New York 11801
Tel: 516-681-8746 TWX: 510-224-6480

Tri-Tech Electronics, Inc.
3215 E. Main Street
Endwell, New York 13760
Tel: 607-754-1094 TWX: 510-252-0891

Tri-Tech Electronics, Inc.
590 Perinton Hills Office Park
Fairport, New York 14450
Tel: 716-223-5720
TWX: 510-253-6356

Tri-Tech Electronics, Inc.
6836 E. Genesee Street
Fayetteville, New York 13066
Tel: 315-446-2881 TWX: 710-541-0604

Tri-Tech Electronics, Inc.
19 Davis Avenue
Poughkeepsie, New York 12603
Tel: 914-473-3880
TWX: 510-253-6356

North Carolina
Cartwright & Bean, Inc.
1165 Commercial Ave.
Charlotte, North Carolina 28205
Tel: 704-377-5673

Cartwright & Bean, Inc.
P.O. Box 18465
3948 Browning Place
Raleigh, North Carolina 27619
Tel: 919-781-6560

Ohio
The Lyons Corporation
4812 Frederick Road, Suite 101
Dayton, Ohio 45414
Tel: 513-278-0714
TWX: 810-459-1803

The Lyons Corporation
6151 Wilson Mills Road, Suite 101
Highland Heights, Ohio 44143
Tel: 216-461-8288
TWX: 810-459-1803

Oklahoma
Technical Marketing
9717 E. 42nd Street, Suite 221
Tulsa, Oklahoma 74145
Tel: 918-622-5984

Oregon
Magna Sales, Inc.
8285 S.W. Nimbus Ave., Suite 138
Beaverton, Oregon 97005
Tel: 503-641-7045
TWX: 910-467-8742

Pennsylvania
The Lyons Corporation
Affler Building
2787 Babcock Boulevard
Pittsburgh, Pennsylvania 15237
Tel: 412-931-7751

Tennessee
Cartwright & Bean, Inc.
P.O. Box 4760
560 S. Cooper Street
Memphis, Tennessee 38104
Tel: 901-276-4442
TWX: 810-751-3220

Cartwright & Bean, Inc.
8705 Unicorn Drive
Suite B120
Knoxville, Tennessee 37923
Tel: 615-693-7450
TWX: 810-751-3220

Texas
Technical Marketing
3320 Wiley Post Road
Carrollton, Texas 75006
Tel: 214-387-3601 TWX: 910-860-5158

Technical Marketing, Inc.
9027 North Gate Blvd.
Suite 140
Austin, Texas 78758

Technical Marketing
6430 Hillcroft, Suite 104
Houston, Texas 77036
Tel: 713-777-9228

Utah
Simpson Associates, Inc.
7324 South 1300 East
Midvale, Utah 94047
Tel: 801-566-3691
TWX: 910-925-4031

Washington
Magna Sales, Inc.
Benaroya Business Park
Building 3, Suite 115
300-120th Avenue, N.E.
Bellevue, Washington 98004
Tel: 206-455-3190

Wisconsin
Larsen Associates
10855 West Potter Road
Wauwatosa, Wisconsin 53226
Tel: 414-258-0529 TWX: 910-262-3160

Canada
R.N. Longman Sales, Inc. (L.S.I.)
1715 Meyerside Drive
Suite 1
Mississauga, Ontario, L5T 1C5 Canada
Tel: 416-677-8100 TWX: 610-492-8976

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Printed in U.S.A./2022-223-A-22-020 25M March, 1980