FERRANTI

Technical Handbook
Standard ICs

Converter
Voltage Reference
Telecom
Industrial

Änderungen und Irrtümer sind vorbehalten.

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Standard IC Datahandbook

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1. Digital-to-Analogue Converters

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PRODUCT SELECTION GUIDE D TO A CONVERTERS

TYPE	USEFUL RESOLUTION (BITS)	SETTLING TIME (μs)	ON-CHIP REFERENCE	INPUT LATCH	TEMPERATURE RANGE (°C)	FEATURES	PAGE
ZN425E SERIES	8 to 6	1	+	–	0 to 70	D to A with on-chip counter	1-11
ZN425J-8	8	1	+	–	-55 to +125	D to A with on-chip counter	1-11
ZN426E SERIES	8 to 6	1	+	–	0 to 70	TTL and CMOS compatible	1-19
ZN426J-8	8	1	+	–	-55 to +125	TTL and CMOS compatible	1-19
ZN428E-8	8	0,8	+	+	0 to 70	Microprocessor, TTL and CMOS compatible	1-25
ZN428J-8	8	0,8	+	+	-55 to +125	Microprocessor, TTL and CMOS compatible	1-25
ZN429E-8	8	1	–	–	0 to 70	Low cost, TTL and CMOS compatible	1-35
ZN429J-8	8	1	–	–	-55 to +125	Low cost, TTL and CMOS compatible	1-35
ZN434E	4	0,3	$V_{CC}/2$	–	0 to 70	Low cost, TTL and CMOS compatible	1-41
ZN435E	8	0,8	+	–	0 to 70	D to A, up/down counter, clock-generator	1-44
ZN435J	8	0,8	+	–	-55 to +125	D to A, up/down counter, clock-generator	1-44
ZN436E	6	1	–	–	0 to 70	Low cost, TTL and CMOS compatible	1-63
ZN436J	6	1	–	–	-55 to +125	Low cost, TTL and CMOS compatible	1-63
ZN558E	8	0,8	+	+	0 to 70	compatible to AD558 8 Bit Latched Input	1-63
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1. DIGITAL TO ANALOGUE CONVERTERS

A Digital to Analogue converter (DAC) is a device which converts a digital data input into a corresponding analogue output. This output usually takes the form of a voltage or current.

1.1 Ideal Output Characteristics

If a unipolar voltage output and normal binary input coding are assumed, then the ideal transfer function of a linear DAC may be written as:

$$V_{out} = V_{FS}\,(B_1.2^{-1} + B_2.2^{-2} + B_3.2^{-3} + \ldots\ldots + B_n.2^{-n})$$

where B_1 is the most significant bit input (MSB) and B_n is the least significant bit input (LSB). Bits 1 to n can each assume a value of '1' or '0'. The number of bit inputs a DAC possesses is known as the RESOLUTION of the converter.

The smallest increment of output voltage is that contributed by the LSB and is equal to $V_{FS}.2^{-n}$.

The terms 'MSB', 'LSB' etc., are frequently used interchangeably to describe either the digital input or the corresponding analogue output.

The maximum output from a DAC is known as full-scale output (V_{FSO}). It occurs when all inputs are '1' and is equal to $V_{FS}\left(\frac{(2^n-1)}{2^n}\right)$. For example the maximum output of a 3-bit DAC is $\frac{7}{8}\,V_{FS}$.

The transfer function graph of an ideal 3-bit DAC is shown in figure 1. For each of the 8 input codes there exists a discrete analogue output

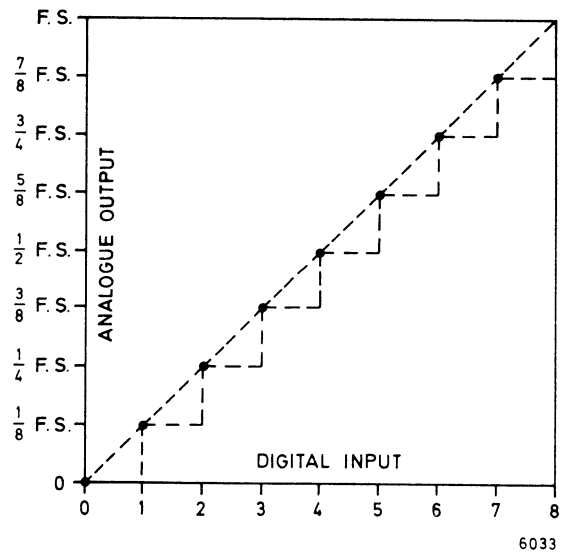


Fig. 1. Transfer Characteristic of Ideal 3-bit DAC

level, represented by a point on the graph. It should be emphasised that the transfer characteristic is not a continuous function and it is, therefore, not strictly correct to join the points with a continuous line, since this would imply that non-integral input codes and corresponding levels existed. However, a straight line is often drawn between zero and full scale to represent the 'ideal' transfer function on which all the points should lie.

Similarly, if the input code of a DAC is incremented using, say, a binary counter and clock generator, then the analogue output will be a staircase waveform. DAC transfer functions are frequently drawn as a staircase, since this is a convenient way of illustrating various errors that may occur in a DAC. However, such a graph is, strictly speaking, a plot of analogue output v. time rather than output v. input code.

1.2 Practical DAC Circuits

Figure 2 shows an example of a 3-bit DAC circuit based on a voltage-switching R-2R ladder network, a technique widely used in Ferranti converters.

Each 2R element is connected either to 0 volts or V_{FS} (V_{REF}) by transistor switches. Binary weighted voltages are produced at the output of the R-2R ladder, the value being proportional to the digital input number.

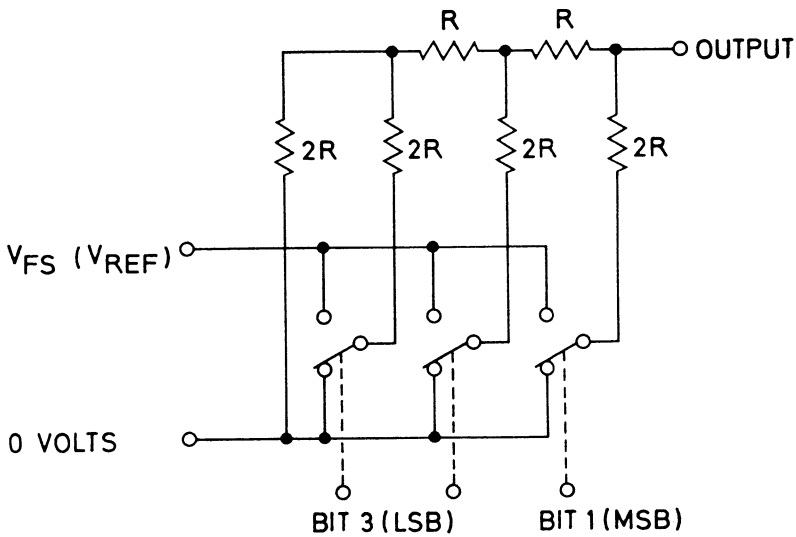


Fig. 2. 3-bit Voltage Switching DAC

For example, it is fairly easy to see that if bit 1 is '1' and bits 2 and 3 are '0' then an output of $V_{FS}/2$ is produced. This is because the resistance of the ladder looking from the output through the first R is 2R, which forms a 2:1 attenuator with the 2R in series with the MSB switch. Output voltages for other input codes can similarly be calculated, and it can be seen that the ladder may be extended to any number of bits.

The voltage switching ladder technique is used in the ZN426, ZN428 and ZN429 series of D to A converters and also in the ZN425 dual-purpose A to D/D to A converter.

1.3 D to A Parameters and Definitions

1.3.1 Converter Errors

The ideal DAC assumes that all the resistors are perfectly matched and that the switches have zero resistance. In a practical converter this will not be the case and various errors will occur in the output.

1.3.2 Monotonicity

When the input code of a DAC is increased in 1 LSB steps the analogue output of the DAC should also increase, staircase fashion. If the output always increases in this manner then the DAC is said to be monotonic, i.e. the output is a single-valued function of the input. If, due to errors in the bit weighting, the output of the DAC decreases at any step, as shown in figure 3, then the DAC is said to be non-monotonic.

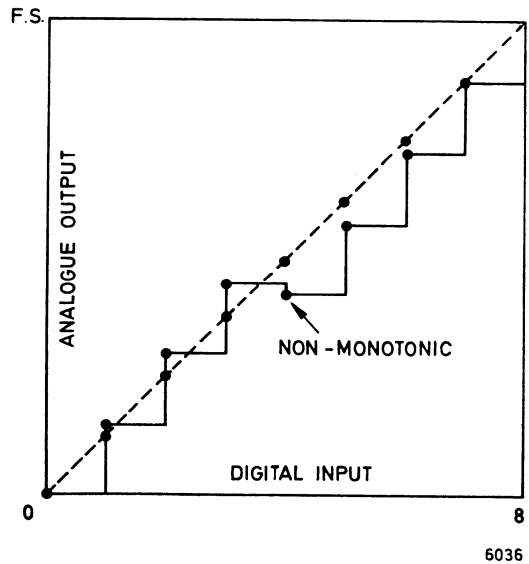


Fig. 3. Non-monotonic DAC

1.3.3 Offset (Zero Error)

Assuming unipolar operation and normal binary coding, when the input code is zero then the DAC output should also be zero. However, due to package lead resistances and offset voltages in the switches this will not be the case, and a small output offset may exist. This has the effect of shifting the transfer function so that it no longer passes through zero, as shown in figure 4.

1.3.4 Gain Error

If the reference voltage of a DAC is exactly the nominal value then the transfer characteristics of the converter should follow the ideal straight line. However, due to imperfections in the converter the transfer function may diverge from this line, as shown in figure 4. This error is known as gain error and is the difference between the slope of the actual transfer characteristic and the slope of the ideal transfer characteristic.

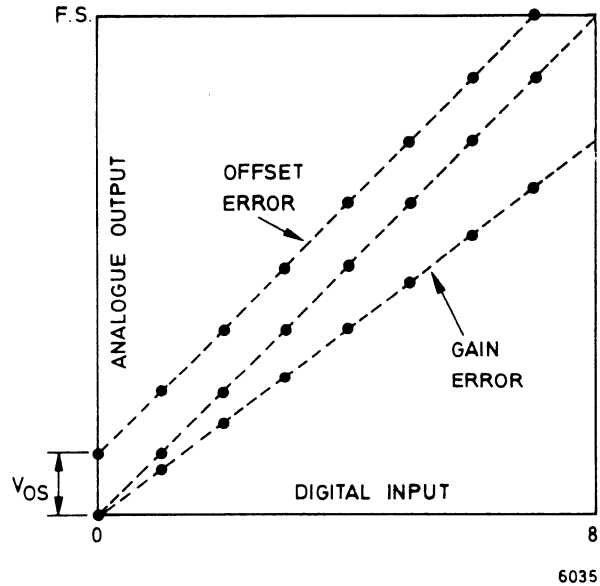


Fig. 4. Illustrating Offset and Gain Errors

1.3.5 Linearity Errors

Offset and gain errors may be trimmed out so that the end points of the transfer characteristic lie at zero and V_{FSO}. However, even when this has been done, some or all of the intermediate points may not lie on the 'ideal' line. These errors, which cannot be trimmed out, are known as linearity errors.

1.3.6 Non-Linearity (Linearity Error)

This is the maximum amount, given either as a percentage of full scale or a fraction of an LSB, by which any point on the transfer characteristic deviates from the ideal straight line passing through zero and V_{FSO}. Non-linearity is illustrated in figure 5. A linearity error within the range $\pm\frac{1}{2}$ LSB assures monotonic operation. Note however that the converse is not true and a DAC may still be monotonic with large linearity errors, which is also shown by figure 5.

1.3.7 Differential Non-linearity

This is the maximum difference, specified as a fraction of an LSB, between the actual and ideal size of any one LSB analogue increment. This can be seen as an error in the step height of a DAC staircase. A positive value of differential non-linearity means that the step height is larger than nominal, whilst a negative value means that it is smaller than nominal. If it is more negative than –1 LSB then the DAC is non-monotonic. However, positive differential non-linearity may assume any value and a DAC can still be monotonic, as shown in figure 5.

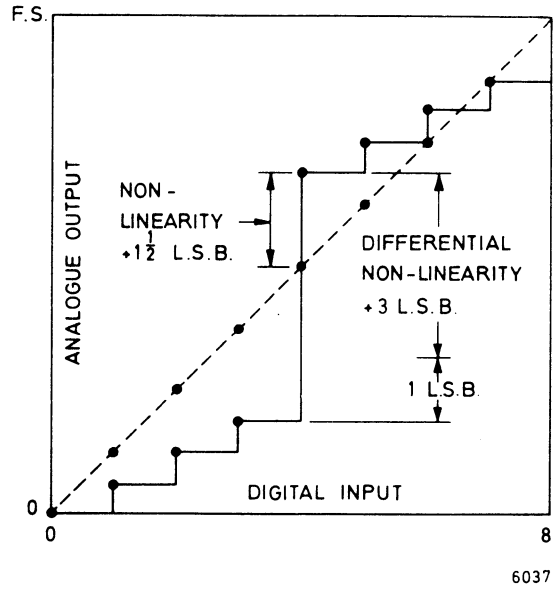


Fig. 5. Illustrating Linearity Errors

1.3.8 Resolution

As stated earlier, the resolution of a DAC is simply the number of bit inputs that a DAC possesses, which indicates the smallest analogue increment that the converter can produce as a fraction of V_{FS}, e.g. 8 bits = 1 part in 2^8 (256). Resolution implies nothing about the accuracy of a DAC, which is defined by linearity and other errors.

1.3.9 Useful Resolution

If an n bit DAC has a differential non-linearity of say –1.5 LSB then it is non-monotonic. However, if the LSB input is made permanently '0' then the DAC becomes an n – 1 bit device with an LSB equal to twice the original LSB. The differential non-linearity error thus becomes –0.75 (new) LSB and the device is monotonic at a resolution of n – 1 bits. This is illustrated in figure 6, which shows the transfer characteristic of a 3-bit DAC that has a useful resolution of 2 bits.

Due to manufacturing tolerances a proportion of n-bit converters will have only n – 1 or n – 2 bit useful resolution. In applications not requiring n –bit useful resolution these reduced resolution versions offer a significant price advantage. The useful resolution of Ferranti DACs is guaranteed over their full operating temperature range.

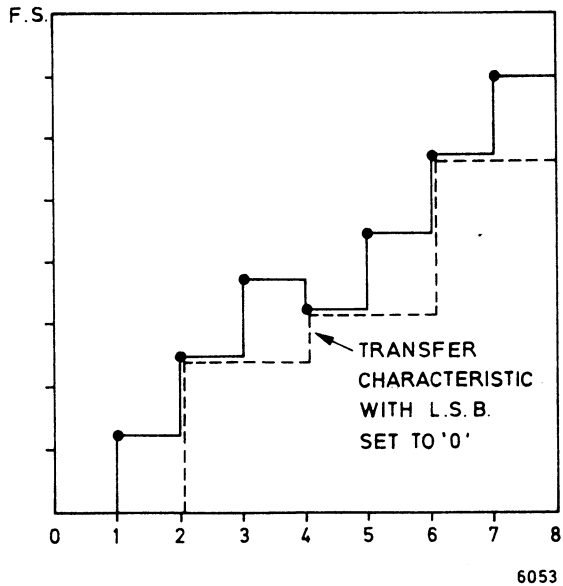


Fig. 6. Non-monotonic 3-bit DAC With a Useful Resolution of 2 bits

1.3.10 Settling Time is the time taken after a transition of the input code for the output of a DAC to settle to within $\pm\frac{1}{2}$ LSB of its final value. This varies depending on which bits are being changed. It may be specified for a change of 1 LSB which generally gives the most optimistic (fastest) figure. More conservative figures are given by the most major transition (where the MSB changes in one direction and all other bits change in the opposite direction, e.g. 01111111 to 10000000 or vice versa) or by a change from all bits off to all bits on (00000000 to 11111111) or vice versa.

1.4 Bipolar Operation

The discussion so far has been concerned only with DACs producing a single polarity (usually positive) output voltage. In some applications a bipolar (both positive and negative) output range may be required. This can be achieved by adding a negative offset of $\frac{V_{REF}}{2}$ to the analogue output, as shown in figure 7. For all input codes where the MSB is '0' the output voltage is then negative, and for output codes where the MSB is '1' the output voltage is positive. Where the input coding is normally binary but the output voltage is offset by $\frac{-V_{REF}}{2}$ then the input code is referred to as offset binary.

The transfer function of a 3-bit DAC with offset binary coding is shown in figure 8.

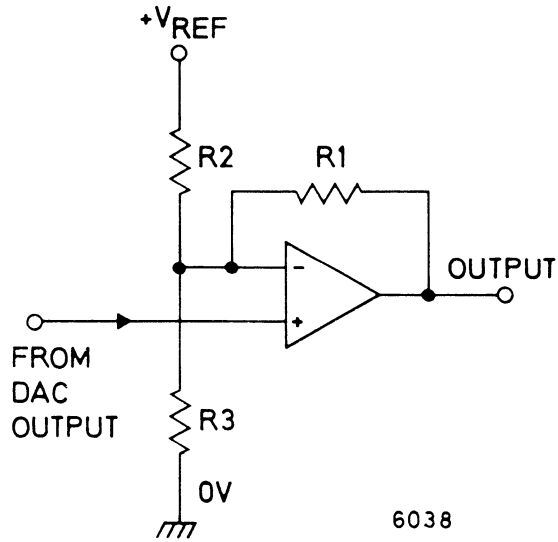


Fig. 7. Bipolar Operation of a DAC

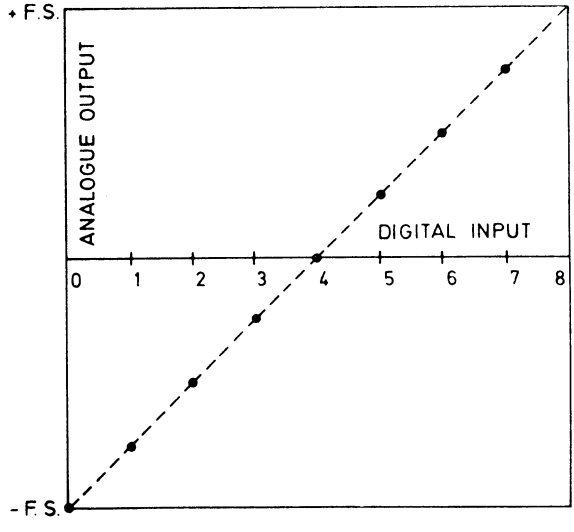


Fig. 8. Bipolar Operation of a 3-bit DAC

FERRANTI semiconductors

ZN425 Series

8 Bit D/A-A/D-Converter

FEATURES

- **8, 7 and 6 bit Accuracy**
- **0°C to +70°C (ZN425E Series)**
- **–55°C to +125°C (ZN425J-8)**
- **TTL and 5V CMOS Compatible**
- **Single +5V Supply**
- **Settling Time (D to A) 1 μsec Typical**
- **Conversion Time (A to D) 1 msec typical, using ramp and compare.**
- **Extra Components Required**

  D-A : Reference capacitor (direct voltage output through 10 kΩ typ.)

  A-D : Comparator, gate, clock and reference capacitor

DESCRIPTION

The ZN425 is a monolithic 8-bit digital to analogue converter containing an R-2R ladder network of diffused resistors with precision bipolar switches, and in addition a counter and a 2.5V precision voltage reference. The counter is a powerful addition which allows a precision staircase to be generated very simply merely by clocking the counter.

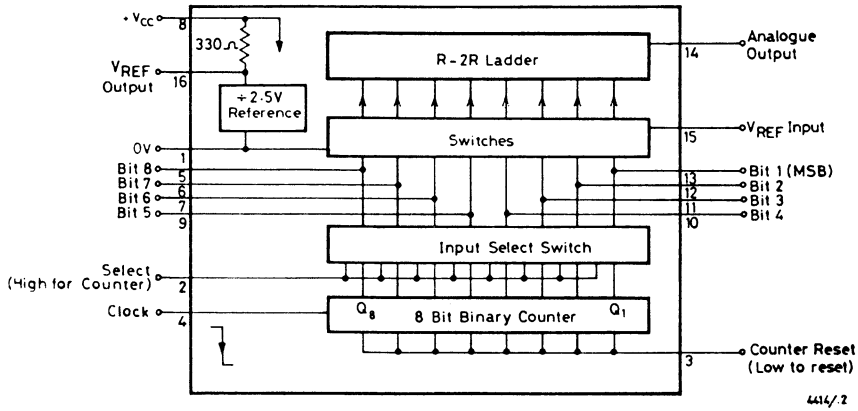


Fig. 1 – System Diagram

ZN425 Series

INTRODUCTION

The ZN425 is an 8-bit dual mode digital to analogue/analogue to digital converter. It contains an 8-bit D to A converter using an advanced design of R-2R ladder network and an array of precision bipolar switches plus an 8-bit binary counter and a 2.5 volt precision voltage reference all on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The use of the on-chip reference voltage is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

By including on the chip an 8-bit binary counter, analogue to digital conversion can be obtained simply by adding an external comparator (ZN424P) and clock inhibit gating (ZN7400E).

By simply clocking the counter the ZN425 can be used as a self-contained precision ramp generator.

A logic input select switch is incorporated which determines whether the precision switches accept the outputs from the binary counter or external digital inputs depending upon whether the control signal is respectively high or low.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

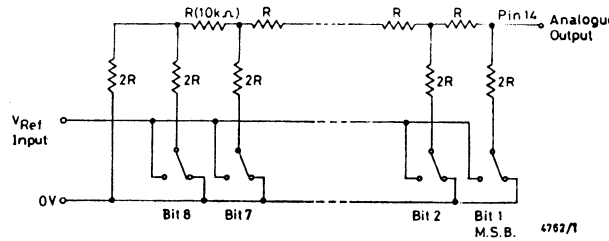


Fig. 2 – The R-2R Ladder Network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1 millivolt).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

ORDERING INFORMATION

Operating Temperature	8-bit Accuracy	7-bit Accuracy	6-bit Accuracy	Package
0°C to +70°C	ZN425E-8	ZN425E-7	ZN425E-6	Plastic
–55°C to +125°C	ZN425J-8	—	—	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7·0 volts
Max. voltage, logic and V_{REF} inputs .. .. +5·5 volts *See note 3*
Operating temperature range .. .. .. 0°C to +70°C (ZN425E Series)
–55°C to +125°C (ZN425J-8)
Storage temperature range .. .. –55°C to +125°C

CHARACTERISTICS (at T_{amb} = 25°C and V_{CC} = +5 volts unless otherwise specified).

Internal voltage reference

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output voltage	V_{REF}	2·4	2·55	2·7	volts	I = 7·5 mA (internal)
Slope resistance	R_s	—	2	4	ohms	I = 7·5 mA (internal)
V_{REF} Temperature coefficient		—	40	—	ppm/°C	I = 7·5 mA (internal)

Note: The internal reference requires a 0·22 μF stabilising capacitor between pins 1 and 16.

8-Bit D to A Converter and Counter

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Resolution		8	—	—	bits	
Accuracy (useful resolution) ZN425J-8		8	—	—	bits	V_{REF} Input = 2 to 3V
ZN425E-8		8	—	—	bits	
ZN425E-7		7	—	—	bits	
ZN425E-6		6	—	—	bits	
Non-linearity		—	—	±0·5	L.S.B.	*See Note 3*
Differential non-linearity		—	±0·5	—	L.S.B.	*See Note 6*
Settling time		—	1·0	—	μs	1 L.S.B. step
Settling time to 0·5 L.S.B.		—	1·5	2·5	μs	All bits ON to OFF or OFF to ON
Offset voltage ZN425J-8	V_{OS}	—	8	12	mV	All bits OFF *See Note 3*
ZN425E-8, ZN425E-6, ZN425E-7		—	3	8	mV	
Full scale output		2·545	2·550	2·555	volts	All bits ON Ext. V_{REF}=2·56V
Full scale temperature coeff.		—	3	—	ppm/°C	Ext. V_{REF}=2·56V
Non-linearity error temp. coeff.		—	7·5	—	ppm/°C	Relative to F.S.R.
Analogue output resistance	R_o	—	10	—	kΩ	
External reference voltage		0	—	3·0	volts	
Supply voltage	V_{CC}	4·5	—	5·5	volts	*See Note 3*
Supply current	I_s	—	25	35	mA	
High level input voltage	V_{IH}	2·0	—	—	volts	*See Notes 1 and 2*
Low level input voltage	V_{IL}	—	—	0·7	volts	

CHARACTERISTICS *(continued)*.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
High level input current	I_{IH}	—	—	10	μA	V_{CC} = max. V_I = 2·4V
		—	—	100	μA	V_{CC} = max. V_I = 5·5V
Low level input current, bit inputs	I_{IL}	—	—	–0·68	mA	V_{CC} = max. V_I = 0·3V
Low level input current, clock reset and input select	I_L	—	—	–0·18	mA	
High level output current	I_{OH}	—	—	–40	μA	
Low level output current	I_{OL}	—	—	1·6	mA	
High level output voltage	V_{OH}	2·4	—	—	volts	V_{CC} = min. Q = 1 I_{load} = –40 μA
Low level output voltage	V_{OL}	—	—	0·4	volts	V_{CC} = min. Q = 0 I_{load} = 1·6 mA
Maximum counter clock frequency	f_c	3	5	—	MHz	*See Note 5*
Reset pulse width	t_R	200	—	—	ns	*See Note 4*

Notes:

1. The Input Select pin (2) must be held low when the bit pins (5, 6, 7, 9, 10, 11, 12 and 13) are driven externally.
2. To obtain counter outputs on bit pins the Input Select pin (2) should be taken to $+V_{CC}$ via a 1 kΩ resistor.
3. The ZN425J differs from the ZN425E in the following respects:
   (a) For the ZN425J, the maximum linearity error may increase to ±1 LSB over the temperature ranges –55°C to 0°C and +70°C to +125°C.
   (b) Maximum operating voltage. Between 70°C and 125°C the maximum supply voltage is reduced to 5.0V.
   (c) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
4. The device may be reset by gating from its own counter.
5. F_{max} in A/D mode is 300 kHz, see page 1–18
6. Monotonic over full operating temperature range at resolution appropriate to accuracy.

If Pin 2 is high then the output equals the Q output of the corresponding counter.

If Pin 2 is low then the output transistor, Tr1 is held off.

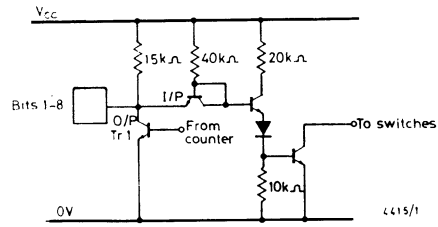


Fig. 3 – Bit Inputs/Outputs

APPLICATIONS

1. 8-bit D to A Converter

The ZN425 gives an analogue voltage output directly from pin 14 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the Analogue Output Resistance R_o, will be less than 0·004% per °C (or 1 L.S.B./100°C) if R_L is chosen to be $\geqslant 650\ k\Omega$.

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 4 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6 kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until $V_{out} = 0 \cdot 000V$.

ii. Set all bits to ON (high) and adjust R_1 until V_{out} = Nominal full scale reading – 1 L.S.B.

iii. Repeat *i.* and *ii.*

e.g. Set F.S.R. to +3·840 volts – 1 L.S.B.

= 3·825 volts

$$(1\ \text{L.S.B.} = \frac{3 \cdot 84}{256} = 15 \cdot 0\ \text{millivolts.})$$

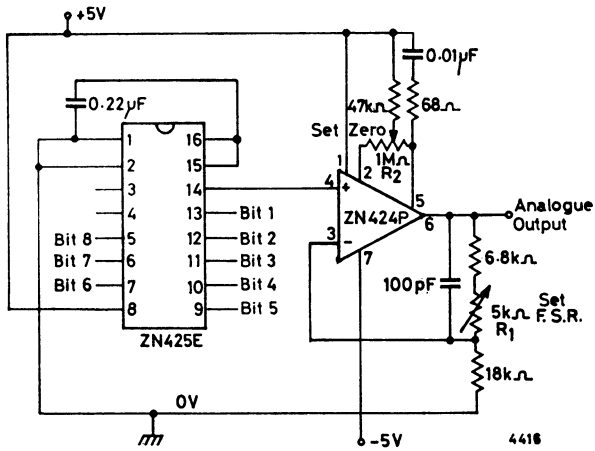


Fig. 4 – 8-bit Digital to Analogue Converter

2. 8-bit Analogue to Digital Converter

A counter type ADC can be constructed by adding a voltage comparator and a latch as in Fig. 5. On the negative edge of the CONVERT COMMAND pulse (15 μs minimum) the counter is set to zero and the STATUS latch to logical 1. On the positive edge the gate is opened, enabling clock pulses to be fed to the counter input of the ZN425. The minimum negative clock pulse width to the ZN425 is 100 ns. The analogue output of the ZN425 ramps until it equals the voltage on the other input of the comparator. At this point the comparator output goes low and resets the STATUS latch to inhibit further clock pulses. The logical 0 from the status latch indicates that the 8 bit digital output is a valid representation of the analogue input voltage.

A small capacitor of 47 pF is added to the ZN425 output to stop any positive going glitches prematurely resetting the status latch. This capacitance is in parallel with the ZN425 output capacitance (20–30 pF) and they form a time constant with the ZN425 output resistance (10 kΩ). This time constant is the main limit to the maximum clock frequency. With a fast comparator the clock frequency can be up to 300 kHz. Using the ZN424P as a comparator the clock frequency should be restricted to 100 kHz. The conversion time varies with the input, being a maximum for full scale input.

$$\text{Maximum conversion time} = \frac{256}{\text{clock frequency in Hz}} \text{ seconds}$$

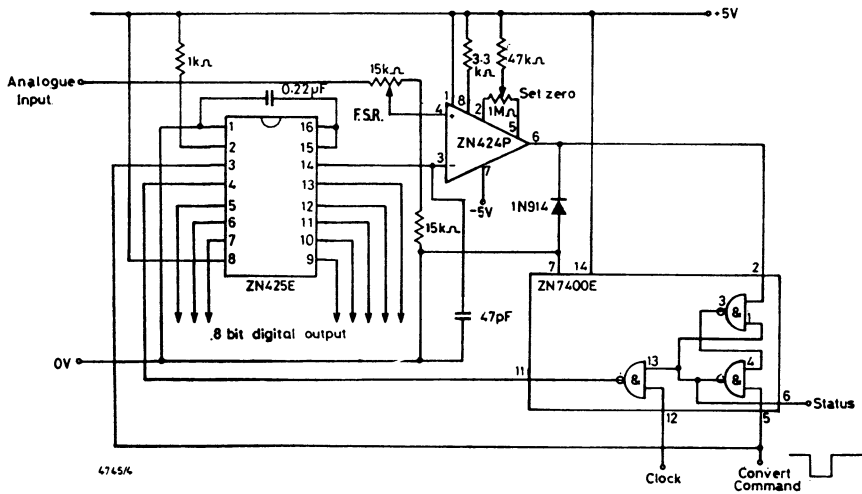


Fig. 5 – 8-bit Analogue to Digital Converter

3. Precision Ramp Generator

The inclusion of an 8-bit binary counter on the chip gives the ZN425 a useful ramp generator function. The circuit, Fig. 6 uses the same buffer stages as the D to A converter. The calibration procedure is also the same. Holding pin 2 low will set all bits to ON and if RESET is taken low with pin 2 high all the bits are turned OFF. If the end voltages of the ramp are not required to be set accurately then the buffer stage could be omitted and the voltage ramp will appear directly at pin 14.

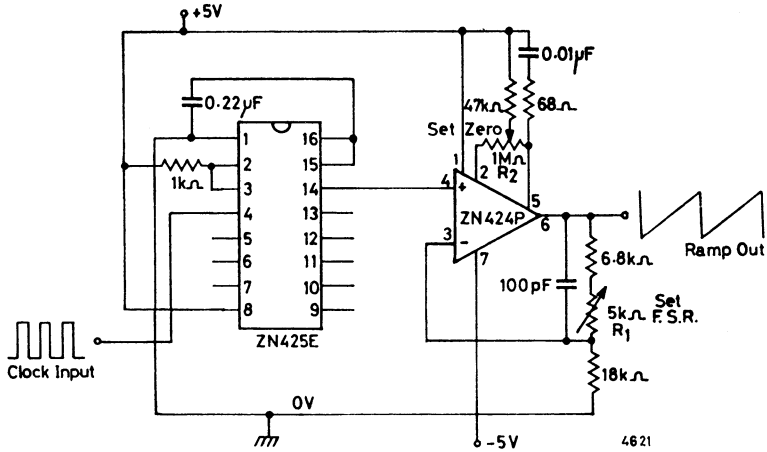


Fig. 6 – Precision Ramp Generator

4. Alternative Output Buffer using the ZLD741

The following circuit, employing the ZLD741 operational amplifier, may be used as the output buffer for both the 8-bit Digital to Analogue Converter (Fig. 4) and the Precision Ramp Generator (Fig. 6).

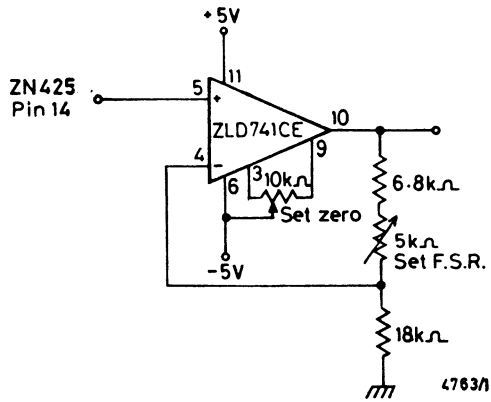
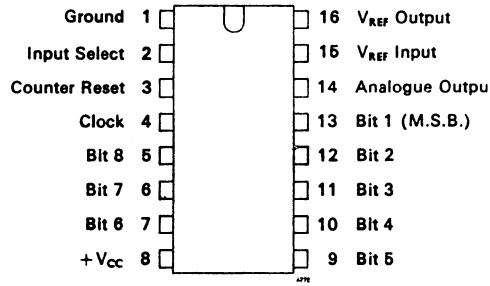


Fig. 7 – The ZLD741 as Output Buffer

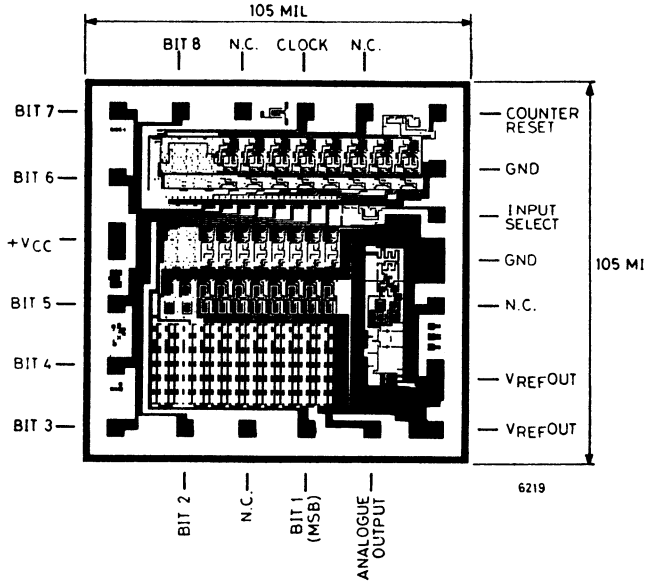
5. Further Applications

Details of a wide range of additional applications, described in the Ferranti publication 'Application Report–ZN425 8-bit A-D/D-A Converter', are also available.

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

ZN426 Series

8 Bit Monolithic D to A Converter

FEATURES

- 8, 7 and 6-bit Accuracy
- ZN426E Series Commercial Temp. Range 0°C to +70°C
- ZN426J-8 Military Temp. Range −55°C to +125°C
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time 1 μsec. Typical
- Only Reference Capacitor and Resistor required

DESCRIPTION

The ZN426 is a monolithic 8-bit digital to analogue converter containing an R-2R ladder network of diffused resistors with precision bipolar switches and a 2.5V precision voltage reference.

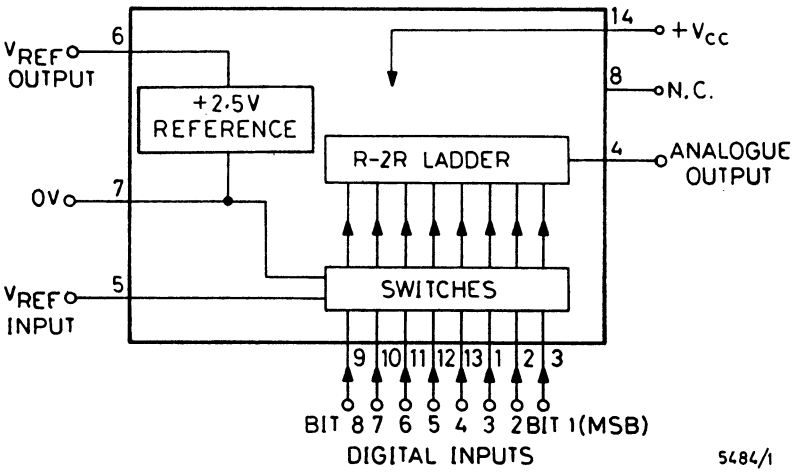


Fig. 1. System Diagram

ZN426 Series

INTRODUCTION

The ZN426 is an 8-bit digital to analogue converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches plus a 2.5 volt precision voltage reference all on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The use of the on-chip reference voltage is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted. In this case there is no need to supply power to the internal reference so R_{REF} and C_{REF} can be omitted.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

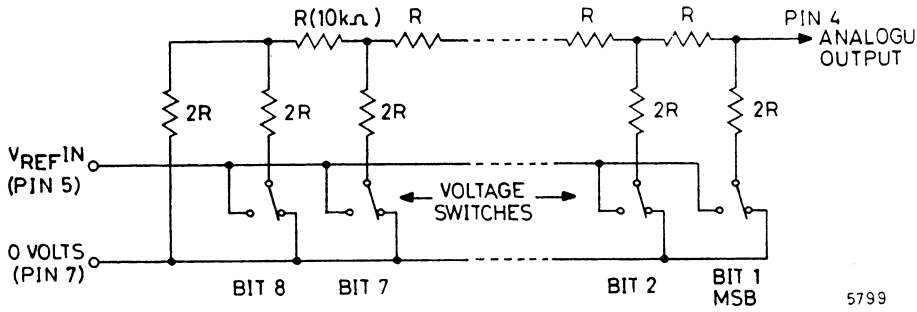


Fig. 2. The R-2R Ladder Network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1 millivolt).

Binary weighted voltages are produced at the output of the R-2R ladder. the value depending on the digital number applied to the bit inputs.

ORDERING INFORMATION

Operating Temperature	8-bit accuracy	7-bit accuracy	6-bit accuracy	Package
0 to +70°C	ZN426E-8	ZN426E-7	ZN426E-6	Plastic
−55 to +125°C	ZN426J-8	—	—	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7.0 volts
Max. voltage, logic and V_{REF} inputs .. .. +5.5 volts
Storage temperature range .. .. −55 to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 volts, T_{amb} = 25°C unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter Resolution		8	—	—	bits	
Accuracy (useful resolution) ZN426J-8, ZN426E-8		8	—	—	bits	V_{REF} input = 2.0 to 3.0 volts
ZN426E-7		7	—	—	bits	
ZN426E-6		6	—	—	bits	
Non-linearity		—	—	±0.5	L.S.B.	*Note 1*
Differential non-linearity		—	±0.5	—	L.S.B.	*Note 2*
Settling time to 0.5 L.S.B.		—	1.0	—	μs	1 L.S.B. step
Settling time to 0.5 L.S.B.		—	2.0	—	μs	All bits ON to OFF or OFF to ON
Offset voltage ZN426J-8	V_{OS}	—	5.0	8.0	mV	All bits OFF *Note 1*
ZN426E-8, ZN426E-7		—	3.0	5.0	mV	
ZN426E-6						
V_{OS} temperature coefficient		—	5	—	μV/°C	
Full scale output		2.545	2.550	2.555	volts	All bits ON Ext. V_{REF} = 2.560V
Full scale temp. coefficient		—	3	—	ppm/°C	Ext. V_{REF} = 2.560V
Non-linearity temp. coeff.		—	7.5	—	ppm/°C	Relative to F.S.R.

Notes:

1. The ZN426J-8 differs from the ZN426E-8 in the following respects:
   (a) For the ZN426J-8, the maximum linearity error may increase to ±0.4% FSR i.e. ±1 LSB over the temperature ranges −55°C to 0°C and +70°C to +125°C.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
2. Monotonic over full temperature range at resolution appropriate to accuracy.

ELECTRICAL CHARACTERISTICS *(continued)*

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Analogue output resistance	R_o	—	10	—	kΩ	
External reference voltage		0	—	3.0	volts	
Supply voltage	V_{CC}	4.5	—	5.5	Volts	
Supply current	I_s	—	5	9	mA	
High level input voltage	V_{IH}	2.0	—	—	volts	
Low level input voltage	V_{IL}	—	—	0.7	volts	
High level input current	I_{IH}	—	—	10	μA	V_{CC} = max., V_I = 2.4V
		—	—	100	μA	V_{CC} = max., V_I = 5.5V
Low level input current	I_{IL}	—	—	–0.18	mA	V_{CC} = max., V_I = 0.3V
Internal Voltage Reference Output voltage	V_{REF}	2.475	2.55	2.625	volts	*Note** R_{REF} = 390Ω
Slope resistance	R_s	—	1	2	ohms	R_{REF} = 390Ω
V_{REF} temperature coefficient		—	40	—	ppm/°C	R_{REF} = 390Ω

*Note** The internal reference requires a 1 μF stabilising capacitor between pins 7 and 6 (C_{REF}) and a 390Ω resistor between pins 14 and 6 (R_{REF}).

APPLICATIONS

1. 8-bit D to A Converter

The ZN426 gives an analogue voltage output directly from pin 4 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the Analogue Output Resistance R_o, will be less than 0.004% per °C (or 1 L.S.B./100°C) if R_L is chosen to be $\geqslant$650 kΩ

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 3 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6 kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{out} = 0.000V.

ii. Set all bits to ON (high) and adjust R_1 until V_{out} = Nominal full scale reading –1 L.S.B.

iii. Repeat *i.* and *ii.*

e.g. Set F.S.R. to +3·840 volts – 1 L.S.B. = 3·825 volts

$$(1 \text{ L.S.B.} = \frac{3 \cdot 84}{256} = 15.0 \text{ millivolts.})$$

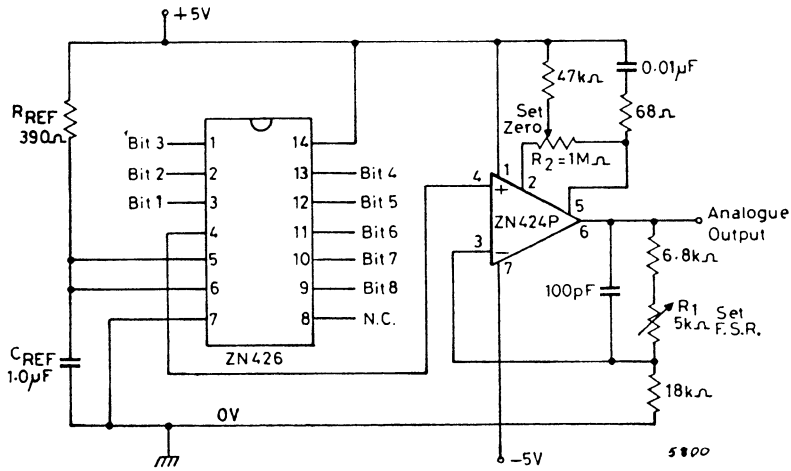


Fig. 3. 8-bit Digital to Analogue Converter

Alternative Output Buffer using the ZLD741

The following circuit, employing the ZLD741 operational amplifier, may be used as the output buffer (Fig. 3).

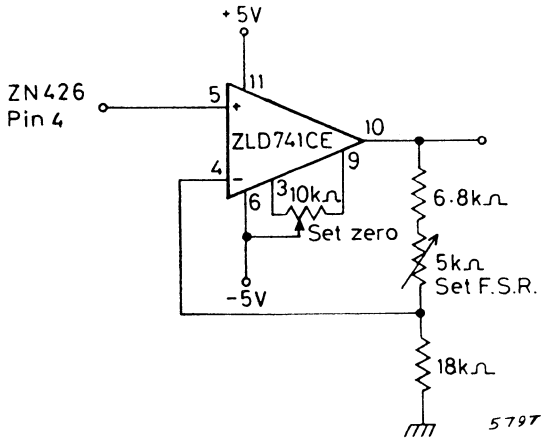
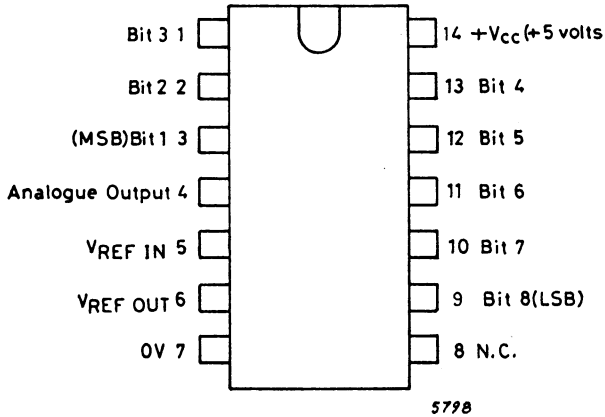
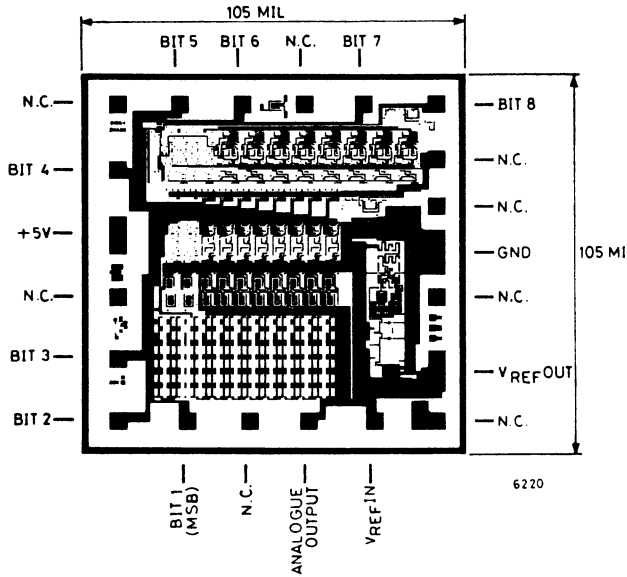


Fig. 4. The ZLD741 as Output Buffer

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

ZN428E-8
ZN428J-8

8 Bit Latched Input Monolithic D to A Converter

FEATURES

- Contains DAC with data latch and on-chip reference.
- Guaranteed monotonic over the full operating temperature range
- Single +5V supply
- Microprocessor compatible
- TTL and 5V CMOS compatible
- 800 ns settling time
- Complementary to ZN427 A to D Series
- ZN428E-8 Commercial temperature range 0°C to +70°C
- ZN428J-8 Military temperature range −55°C to +125°C

GENERAL DESCRIPTION

The ZN428 is a Monolithic 8 bit D to A converter with input latches to facilitate updating from a data bus. The latch is transparent when $\overline{\text{Enable}}$ is LOW and the data is held when $\overline{\text{Enable}}$ is taken HIGH. The ZN428 also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

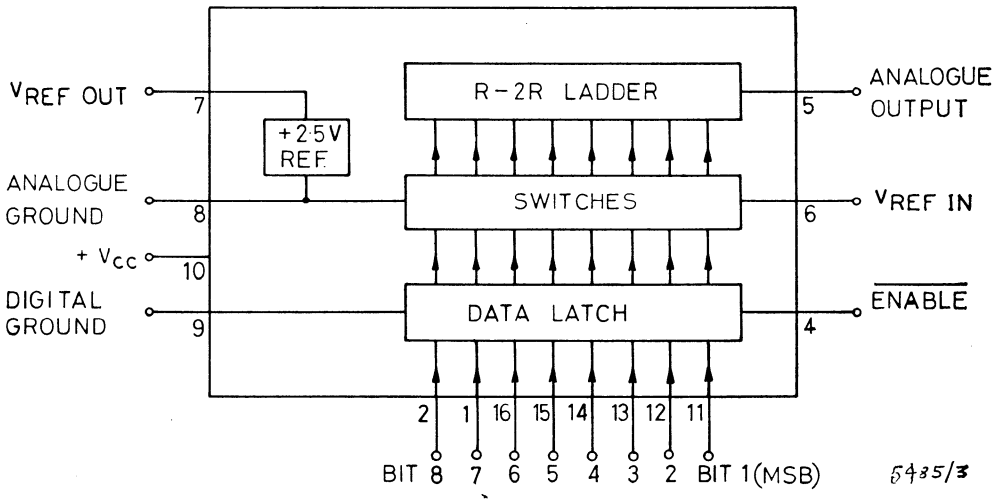


Fig. 1 SYSTEM DIAGRAM

ZN428E-8/J-8

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7.0 volts
Max. voltage, logic and V_{REF} input .. .. $+V_{CC}$
Operating temperature range .. .. 0°C to +70°C (ZN428E-8)
–55°C to +125°C (ZN428J-8)
Storage temperature range .. .. –55°C to +125°C
Analogue Ground to Digital Ground .. .. ±200 mV

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 volts, T_{amb} = 25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
Internal Voltage Reference					
Output voltage	2.475	2.550	2.625	volts	R_{REF} = 390Ω, C_{REF} = 1 µF
Slope resistance		0.5	2	Ω	R_{REF} = 390Ω, C_{REF} = 1 µF
$V_{REF\,OUT}$ T.C.		50		ppm/°C	
Reference current	4		15	mA	Note 1
D to A Converter					
Linearity error			±0.5	LSB	2.0V ≤ $V_{REF\,IN}$ ≤ 3.0V
Differential non-linearity		±0.5		LSB	
Linearity error T.C.		±3		ppm/°C	
Differential non-linearity T.C.		±6		ppm/°C	
Offset voltage		2	5	mV	All bits OFF
Offset voltage T.C.		±6		µV/°C	
Full scale output	2.545	2.550	2.555		External reference $V_{REF\,IN}$ = 2.560 volts, all bits ON
Full scale output T.C.		2		ppm/°C	External reference $V_{REF\,IN}$ = 2.560 volts, all bits ON
Analogue output resistance		4		kΩ	
External reference voltage	0		3.0	volts	
Settling time to 0.5 LSB		800		ns	1 LSB Major Transition (Note 2)
		1.25		µs	All bits ON to OFF or OFF to ON (Note 2)
Operating temperature range:					
ZN428E-8	0		70	C	
ZN428J-8	–55		125	C	
Supply voltage (V_{CC})	4.5	5.0	5.5	volts	

Note 1 See REFERENCE
Note 2 R_L = 10 MΩ, C_L = 10 pF.

ELECTRICAL CHARACTERISTICS *(continued)*

	Min.	Typ.	Max.	Units	Conditions
Supply current		20	30	mA	Note 3
Power consumption		100		mW	
Logic (over specified operating temperature range) High level input voltage	2.0			V	
Low level input voltage			0.8	V	
High level input current			60	μA	V_{IN} = 5.5V V_{CC} = Max.
			20	μA	V_{IN} = 2.4V V_{CC} = Max.
Low level input current			−5	μA	V_{IN} = 0.4V V_{CC} = Max.
Input Clamp Diode Voltage		−1.5		V	I_{IN} = −8 mA
Enable pulse width	100			ns	
Data set-up time	150			ns	Note 4
Data hold time	10			ns	Note 5

Note 3 All inputs HIGH (V_{IH} = 3.5 volts).

Note 4 Set up time before $\overline{\text{Enable}}$ goes high.

Note 5 Hold time after $\overline{\text{Enable}}$ goes high.

D to A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 2. Each 2R element is connected to 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder.

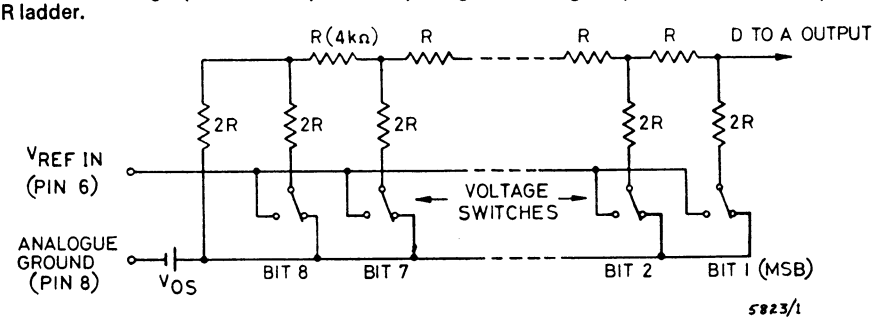


Fig. 2. The R-2R Ladder Network

$$\text{Analogue Output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D to A from the data latch.

V_{OS} is a small offset voltage produced by the D to A switch currents flowing through the package lead resistance. The value of V_{OS} is tyically 1 mV. This offset will normally be removed by the setting up procedure (see APPLICATIONS section) and because the offset temperature coefficient is low ($\pm 6\ \mu V/°C$) the effect on accuracy is negligible.

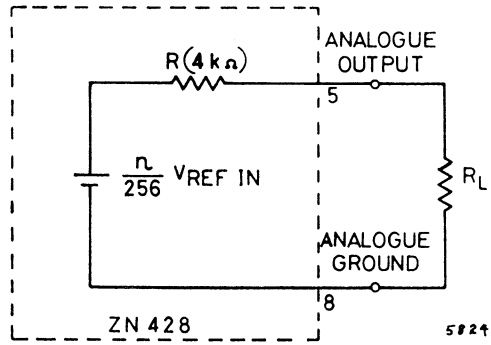


Fig. 3. Analogue Output Equivalent Circuit

Fig. 3 shows an equivalent circuit of the output (ignoring V_{OS}). The output resistance R has a temperature coefficient of +0.2% per °C.

The gain drift due to this is $\frac{0.2R}{R+R_L}$ % per °C

RL should be chosen to be as large as possible to make the gain drift small. As an example if R_L = 400 kΩ then the gain drift due to the T.C. of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN428 can be buffered by an amplifier (see APPLICATIONS section).

REFERENCE

(a) Internal Reference

The internal reference is an active band gap circuit which is equivalent to a 2.5 volt Zener diode with a very low slope impedance (Fig. 4). A resistor (R_{REF}), should be connected between $+V_{CC}$ (pin 10) and pin 7. The recommended value of 390Ω will supply a nominal reference current of (5.0–2.5)/0.39 = 6.4 mA. A stabilising/decoupling capacitor, C_{REF} = 1 μF is required between pins 7 and 8 for internal reference operation, $V_{REF\ OUT}$ (pin 7) being connected to $V_{REF\ IN}$ (pin 6).

Up to five ZN428s may be driven from one internal reference (there is no need to reduce R_{REF}) This useful feature saves power and gives excellent gain tracking between the converters.

(b) External Reference

If required an external reference voltage may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5}{n}$ Ω, where n is the number of converters supplied.

$V_{REF\ IN}$ can be varied from 0 to +3 volts for ratiometric operation. The ZN428 is guaranteed monotonic for $V_{REF\ IN}$ above 2 volts.

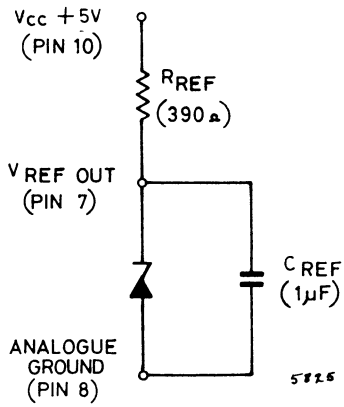


Fig. 4. Internal Voltage Reference

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the Enable input is low the data inputs drive the D to A directly. When Enable goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig. 5.

The ZN428 is provided with separate analogue and digital ground connections. The circuit will operate correctly with as much as ±200 mV between the two grounds.

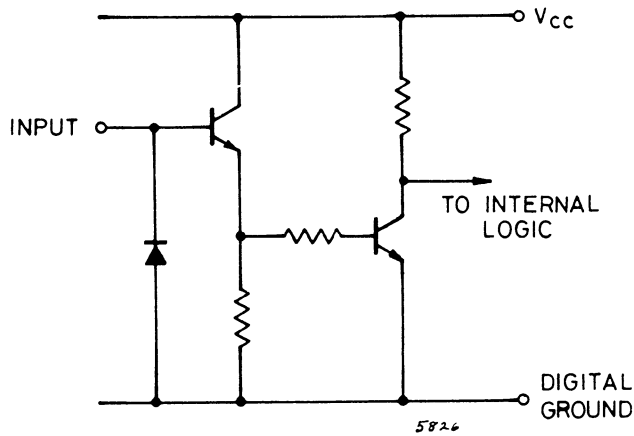


Fig. 5. Equivalent Circuit of All Inputs

ZN428E-8/J-8

APPLICATIONS

(1) Unipolar D to A Converter

The nominal output range of the ZN428 is 0 to $V_{REF\ IN}$ through a 4 kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The general scheme (Fig. 6) is suitable for amplifiers with input bias currents less than 1.5 μA.

The resulting full scale range is given by

$$V_{OUT}\ FS = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.\ V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (4 kΩ). The required nominal values of R1 and R2 are given by R1 = 4G kΩ and $R_2 = 4G/(G-1)$ kΩ.

Using these relationships a table of nominal resistance values for R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5 volts.

Output Range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

For gain setting R_1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5V and +10V output ranges are given in Fig. 7. Settling time for a major transition is 1.5 μs typical.

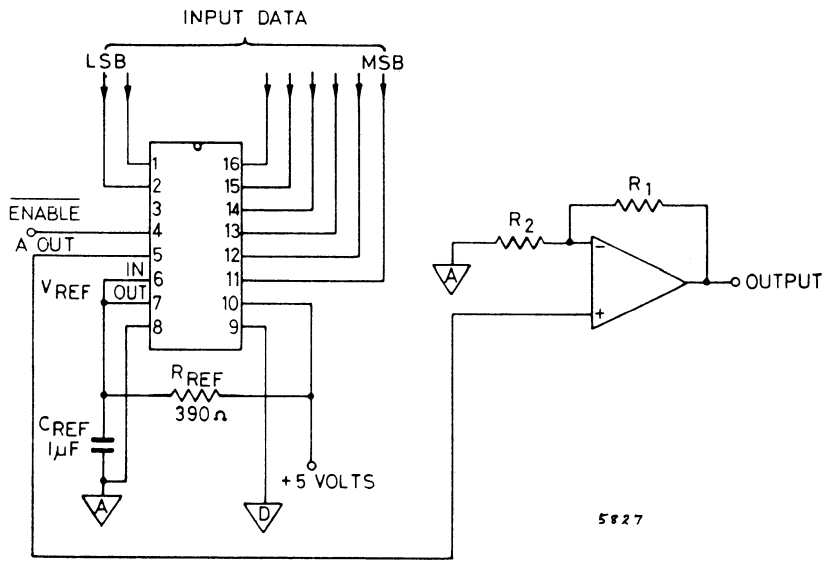


Fig. 6. Unipolar operation – Basic Circuit

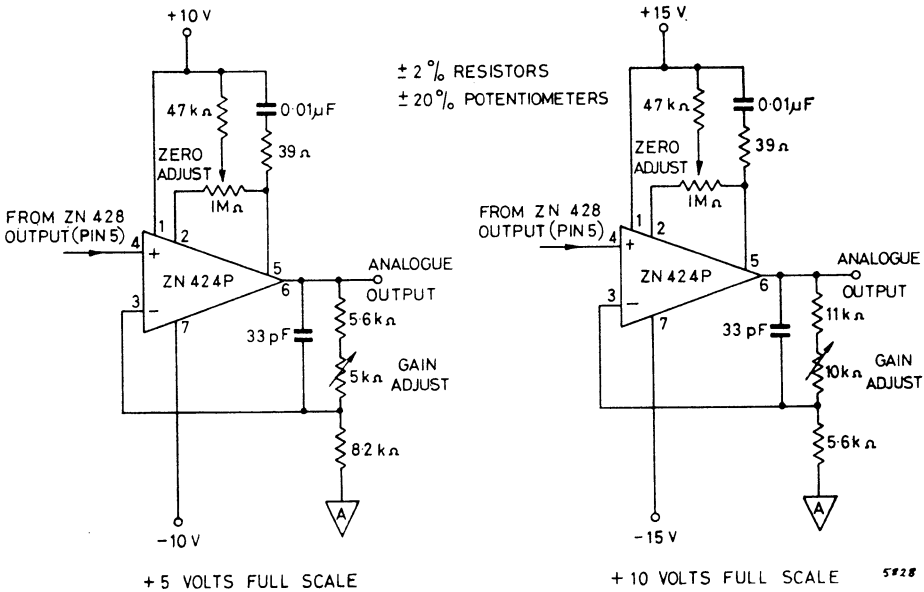


Fig. 7. Unipolar Operation – Component Values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{Enable}}$ low and adjust zero until $V_{OUT} = 0.0000V$.

(ii) Set all bits ON (high) and adjust gain until V_{OUT} = FS –1 LSB.

UNIPOLAR SETTING UP POINTS

Output Range, +FS	LSB	FS – 1LSB
+5V	19.5 mV	4.9805V
+10V	39.1 mV	9.9609V

$$1LSB = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Input Code (Binary)	Analogue Output (Nominal value)
11111111	FS – 1LSB
11111110	FS – 2LSB
11000000	$\frac{3}{4}$ FS
10000001	$\frac{1}{2}$ FS + 1LSB
10000000	$\frac{1}{2}$ FS
01111111	$\frac{1}{2}$ FS – 1LSB
01000000	$\frac{1}{4}$ FS
00000001	1LSB
00000000	0

(2) Bipolar D to A Converter

For bipolar operation the output from the ZN428 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig. 8).

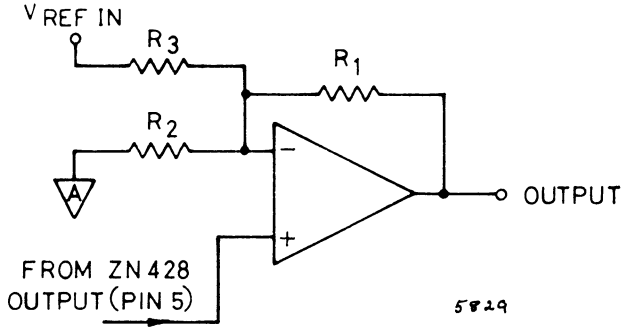


Fig. 8. Bipolar Operation – Basic Circuit

When the digital input to the ZN428 is zero the analogue output is zero and the amplifier output should be –Full scale. An input of all ones to the D to A will give a ZN428 output of $V_{REF\ IN}$ and the amplifier output required is +Full scale. Also, to match the ladder resistance the parallel combination of R_1, R_2 and R_3 should be 4 kΩ.

The nominal values of R_1, R_2 and R_3 which meet these conditions are given by

$$R_1 = 8G\ k\Omega,\ R_2 = 8G/(G-1)\ k\Omega \text{ and } R_3 = 8\ k\Omega$$

where the resultant output range is $\pm G\ V_{REF\ IN}$.

A bipolar output range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) is obtained if $R_1 = R_3 = 8\ k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5$ volts the nominal values of resistors for ±5V and ±10V output ranges are given in the following table:

Output Range	G	R_1	R_2	R_3
±5V	2	16 kΩ	16 kΩ	8 kΩ
±10V	4	32 kΩ	10.66 kΩ	8 kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig. 9. Note that in the ±5V case R_3 has been chosen as 7.5 kΩ (instead of 8.2 kΩ) to get a more symmetrical range of adjustment using standard potentiometers. Settling time for a major transition is 1.5 μs typical.

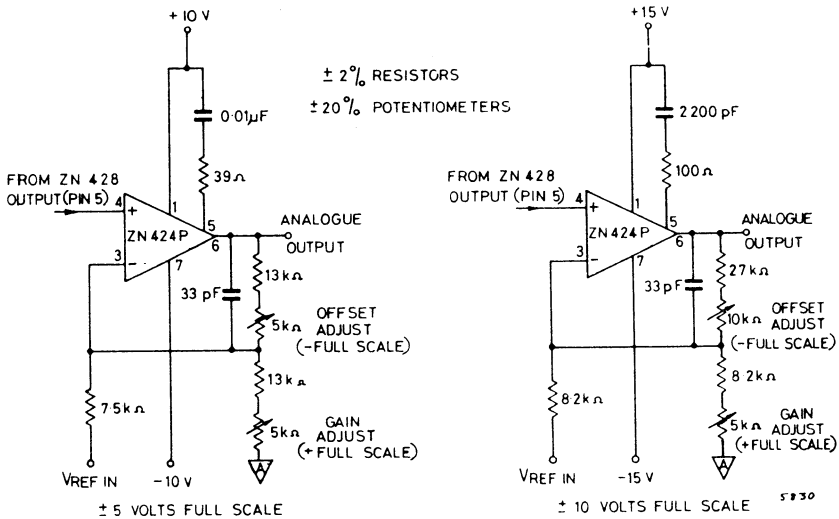


Fig. 9. Bipolar Operation – Component Values

Bipolar Adjustment Procedure

(1) Set all bits to OFF (low) with $\overline{\text{Enable}}$ low and adjust offset until the amplifier output reads –Full Scale.

(2) Set all bits ON (high) and adjust gain until the amplifier output reads + (Full Scale – 1LSB).

BIPOLAR SETTING UP POINTS

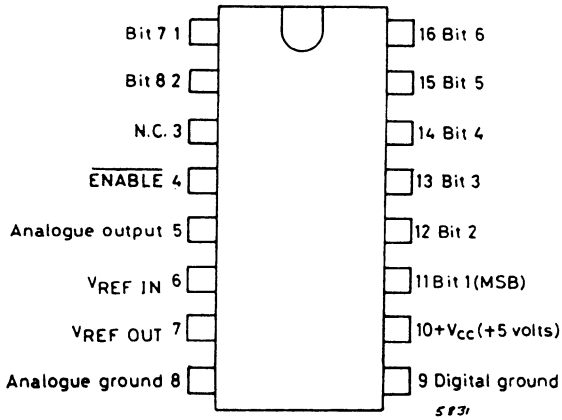
Input Range, ±FS	LSB	–FS	+(FS–1LSB)
±5V	39.1 mV	–5.0000V	+4.9609V
±10V	78.1 mV	–10.0000V	+9.9219V

$$1\text{LSB} = \frac{2\text{FS}}{256}$$

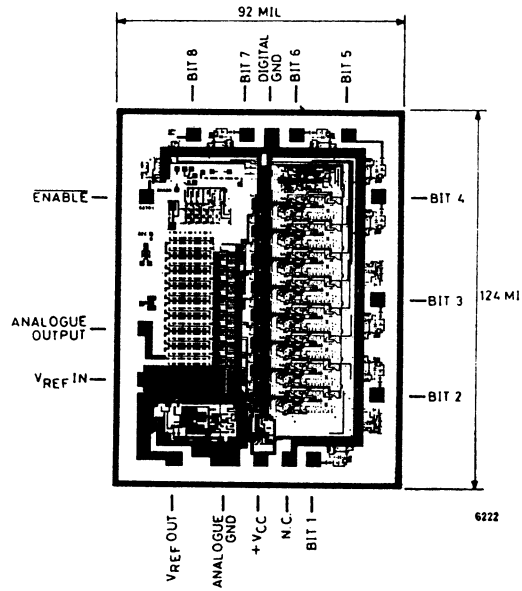
BIPOLAR LOGIC CODING

Input Code (Offset Binary)	Analogue Output (Nominal Value)
11111111	+(FS – 1LSB)
11111110	+(FS – 2LSB)
11000000	+½FS
10000001	+1LSB
10000000	0
01111111	–1LSB
01000000	–½FS
00000001	–(FS – 1LSB)
00000000	–FS

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

ZN429 Series

8 Bit D/A-Converter, Low Cost

FEATURES

- **8, 7 and 6-bit Accuracy**
- **ZN429E Series Commercial Temp. Range 0°C to +70°C**
- **ZN429J-8 Military Temp. Range −55°C to +125°C**
- **TTL and 5V CMOS Compatible**
- **Single +5V Supply**
- **Settling Time 1 μsec. Typical**
- **Designed for low-cost applications**

DESCRIPTION

The ZN429 is a monolithic 8-bit digital to analogue converter containing an R-2R ladder network of diffused resistors with precision bipolar switches.

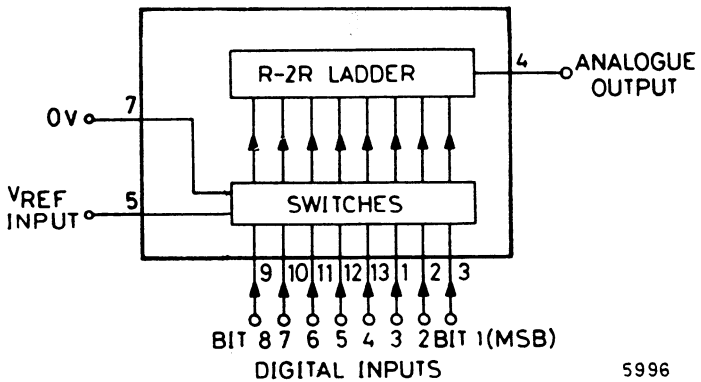


Fig. 1. System Diagram

ZN429 Series

INTRODUCTION

The ZN429 is an 8-bit digital to analogue converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

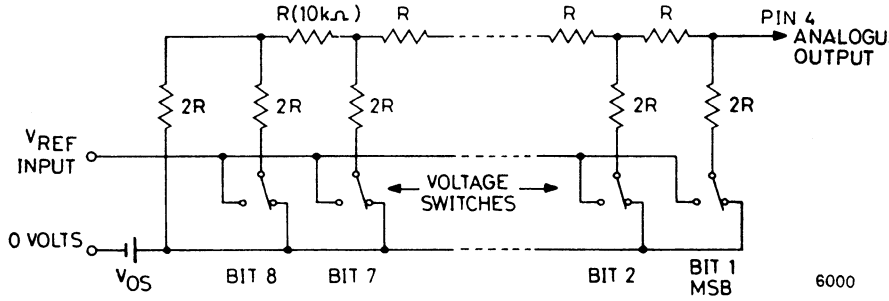


Fig. 2. The R-2R Ladder Network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1 millivolt).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

An external fixed or varying reference is required which should have a slope resistance less than 2 ohms.

Suggested external reference sources are the ZN404 or one of the ZN458 range. Each ZN404 is capable of supplying up to five ZN429 circuits and this is increased to ten for the ZN458 range.

ORDERING INFORMATION

Operating Temperature	8-bit accuracy	7-bit accuracy	6-bit accuracy	Package
0 to +70°C	ZN429E-8	ZN429E-7	ZN429E-6	Plastic
–55 to +125°C	ZN429J-8	—	—	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7.0 volts
Max. voltage, logic and V_{REF} inputs .. .. +5.5 volts
Storage temperature range .. .. –55 to +125°C

CHARACTERISTICS (at T_{amb} = 25°C and V_{CC} = +5 volts unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter Resolution		8	—	—	bits	
Accuracy (useful resolution) ZN429J-8, ZN429E-8		8	—	—	bits	V_{REF} input = 2.0 to 3.0 volts
ZN429E-7		7	—	—	bits	
ZN429E-6		6	—	—	bits	
Non-linearity		—	—	±0.5	L.S.B.	*Note 1*
Differential non-linearity		—	±0.5	—	L.S.B.	*Note 2*
Settling time to 0.5 L.S.B.		—	1.0	—	μs	1 L.S.B. step
Settling time to 0.5 L.S.B.		—	2.0	—	μs	All bits ON to OFF or OFF to ON
Offset voltage ZN429J-8, ZN429E-8	V_{OS}	—	5.0	8.0	mV	All bits OFF *Note 1*
ZN429E-7, ZN429E-6		—	3.0	5.0	mV	
V_{OS} temperature coefficient		—	5	—	μV/°C	
Full scale output		2.545	2.550	2.555	volts	All bits ON Ext. V_{REF} = 2.560V
Full scale temp. coefficient		—	3	—	ppm/°C	Ext. V_{REF} = 2.560V
Non-linearity temp. coeff.		—	7.5	—	ppm/°C	Relative to F.S.R.

Notes:

1. The ZN429J-8 differs from the ZN429E-8 in the following respects:
   (a) For the ZN429J-8, the maximum linearity error may increase to ±0.4% FSR i.e. ±1 LSB over the temperature ranges −55°C to 0°C and +70°C to +125°C.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
2. Monotonic over full temperature range at resolution appropriate to accuracy.

CHARACTERISTICS (*continued*)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Analogue output resistance	R_o	—	10	—	kΩ	
External reference voltage		0	—	3.0	volts	
Supply voltage	V_{CC}	4.5	—	5.5	volts	
Supply current	I_s	—	5	9	mA	
High level input voltage	V_{IH}	2.0	—	—	volts	
Low level input voltage	V_{IL}	—	—	0.7	volts	
High level input current	I_{IH}	—	—	10	μA	V_{CC} = max., V_I = 2.4V
		—	—	100	μA	V_{CC} = max., V_I = 5.5V
Low level input current	I_{IL}	—	—	–0.18	mA	V_{CC} = max., V_I = 0.3V

APPLICATIONS

1. 8-bit D to A Converter

The ZN429 gives an analogue voltage output directly from pin 4 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the Analogue Output Resistance R_o, will be less than 0.004% per °C (or 1 L.S.B./ 100°C) if R_L is chosen to be $\geqslant$650 kΩ

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 3 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6 kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{out} = 0.000V.

ii. Set all bits to ON (high) and adjust R_1 until V_{out} = Nominal full scale reading –1 L.S.B.

iii. Repeat *i.* and *ii.*

e.g. Set F.S.R. to +3.840 volts – 1 L.S.B.
= 3.825 volts

$$(1 \text{ L.S.B.} = \frac{3.84}{256} = 15.0 \text{ millivolts})$$

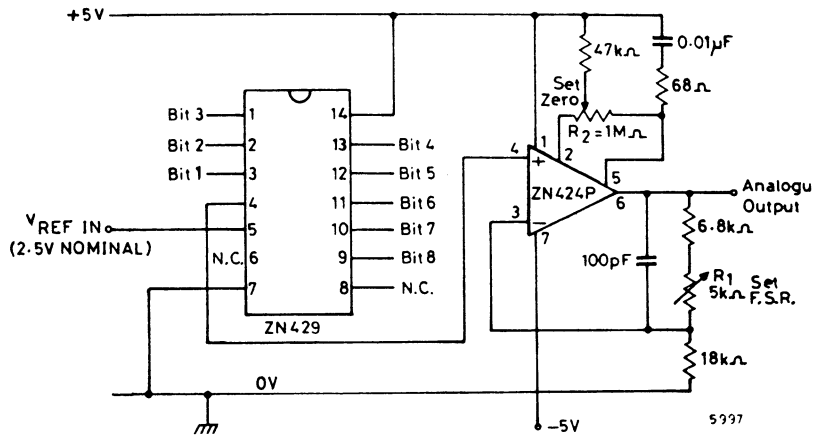


Fig. 3. 8-bit Digital to Analogue Converter

Alternative Output Buffer using the ZLD741

The following circuit, employing the ZLD741 operational amplifier, may be used as the output buffer (Fig. 3).

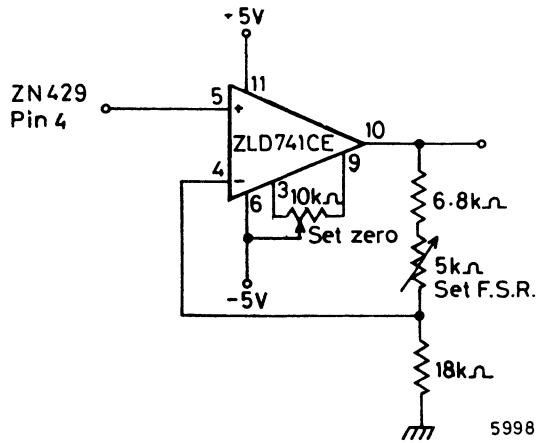
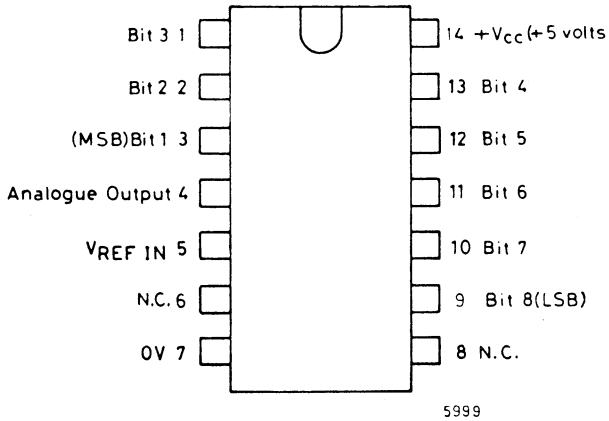
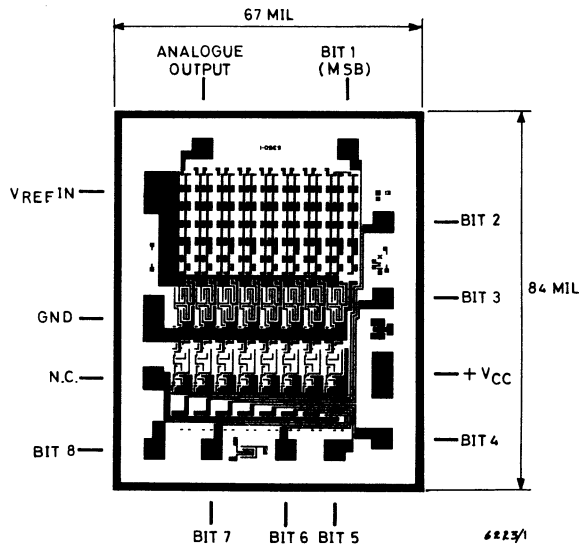


Fig. 4. The ZLD741 as Output Buffer

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

ZN434

4 Bit D/A-Converter, Low Cost

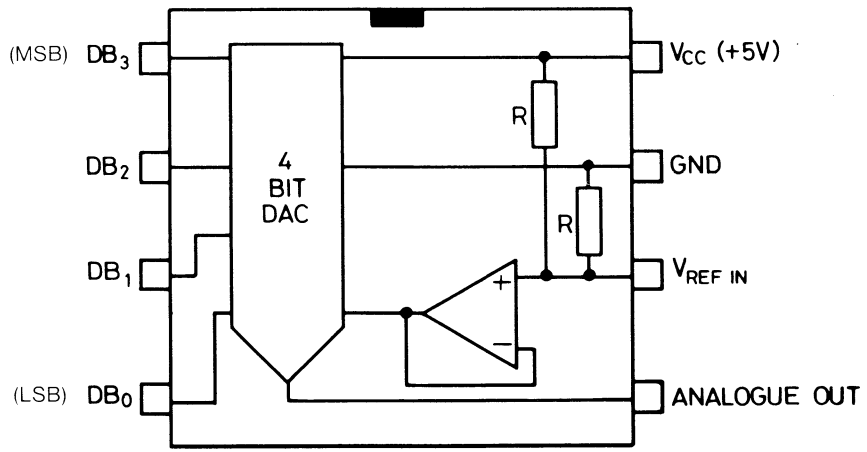
ADVANCE PRODUCT INFORMATION

FEATURES

- 4 bit resolution
- ¼ LSB linearity
- Voltage output
- 300ns settling time
- TTL and CMOS compatible
- Single + 5V supply
- On-chip $\frac{V_{CC}}{2}$ reference
- 0°C to +70°C or −40°C to +85°C temperature range.

DESCRIPTION

The ZN 434 is a 4-bit DAC containing an R-2R ladder network of diffused resistors and precision bipolar switches. An on-chip reference amplifier and attenuator provide a reference voltage of $\frac{V_{CC}}{2}$, allowing the IC to function with no external components.



ZN 434 SYSTEM DIAGRAM

ZN434

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} .. .. +7.0 volts
Logic and V_{REF} inputs .. .. 0 to V_{CC}

	Min	Max
Operating Temperature (ZN 434E)	0°C	+70°C
(ZN 434BE)	−40°C	+85°C
Storage Temperature	−55°C	+125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, T_{amb} = 25°C unless otherwise stated)

Parameter	Min.	Typ.	Max.	Units	Conditions
D to A Converter Resolution	4	—	—	Bits	
Linearity error	—	—	±0.25	LSB	1.5V<$V_{REF\ in}$ < 3V
Differential Linearity error	—	—	±0.25	LSB	
Linearity error tempco	—	±3	—	ppm/°C	
Differential linearity error tempco	—	±6	—	ppm/°C	
Zero error	—	3.0	5.0	mV	
Zero error tempco	—	+6	—	µV/°C	
Full-scale output (V_{CC} as reference)	2.235	2.345	2.456	volts	
Full-scale output (External reference)	0.922	0.938	0.954	V_{ref} in	1.5V<$V_{REF\ in}$ < 3V
Full scale tempco	—	±3	—	ppm/°C	
Analogue output resistance	1.75	2.5	3.25	k	
Analogue output capacitance	—	15	—	pF	
Settling time to 0.5 LSB	—	200	300	ns	Code transition 0000 or 1111 1111 0000
	—	100	150	ns	1 LSB step
Supply voltage	+4.5	+5	+5.5	V	
Supply current	—	10	15	mA	

Parameter	Min.	Typ.	Max.	Units	Conditions
On chip reference amplifier					
Output voltage	$\frac{V_{CC} \times 0.97}{2}$	$\frac{V_{CC}}{2}$	$\frac{V_{CC} \times 1.03}{2}$		
Input current	—	1	—	μA	
Offset voltage		±10		mV	
Input resistance	9	18	27	k	
Logic Inputs					
High level input voltage V_{IH}	2.0	—	—	V	
Low level input voltage V_{IL}	—	—	0.8	V	
High level input current I_{IH}	—	—	10	μA	$V_{CC} = 5.5V, V_I = 2.4V$
	—	—	100	μA	$V_{CC} = V_I = 5.5V$
Low level input current I_{IL}	—	—	180	μA	$V_{CC} = 5.5V, V_I = 0.3V$

CIRCUIT DESCRIPTION

D to A Converter

The ZN 434 is a 4 bit DAC consisting of an R-2R ladder of diffused resistors and precision bipolar switches designed for low offset voltage.

The ladder operates in the voltage switching mode and produces an output voltage $V_{out} = \frac{n}{16} (V_{REF\ IN} - V_{OS}) + V_{OS}$, where n is the digital code set at the bit inputs and V_{OS} is a small offset voltage caused by the supply current flowing through the lead resistance of the ground pin.

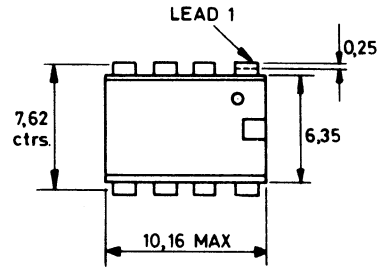
On-chip Reference Amplifier

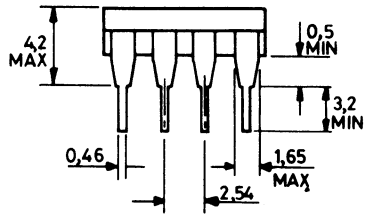
The ZN 434 contains a reference amplifier and attenuator that provide a reference voltage of nominally $\frac{V_{CC}}{2}$ without any external components. Taking into account the attenuator error, input current and offset voltage of the amplifier and gain error of the DAC the full-scale output will be within ± ½ LSB of the nominal value of $0.369 \times V_{CC}$.

By maintaining an accurate and stable supply voltage the ZN 434 may thus be used without an external reference. Where several ZN 434s are used in a system the V_{REF} inputs may be joined together to improve V_{REF} matching.

If a reference voltage other than $\frac{V_{CC}}{2}$ is required then the on-chip attenuator may be overridden, either by connecting a lower resistance attenuator in parallel or by using an active reference such as a bandgap reference source.

PACKAGE OUTLINE





4882 MD/2

8 Lead Moulded D.I.L.
Dimensions in millimetres.

FERRANTI semiconductors

ZN435 E/J

8 Bit D/A-A/D-Converter

ADVANCE PRODUCT INFORMATION

FEATURES

- Multimode device operates as:
  - —DAC
  - —ADC
  - —Tracking ADC
  - —Voltage to Frequency Converter
  - —Ramp and Sawtooth Generator
  - —Nonlinear Waveform Generator
  - —Voltage—Controlled Oscillator
  - —Track-and-Hold Circuit
- 8-bit Accuracy
- 800ns DAC Settling Time
- On-chip Up/down Counter
- On-chip Clock
- On-chip Voltage Reference
- Single + 5V supply
- Commercial or Military Temperature Range.

DESCRIPTION

The ZN435 is a versatile, multifunction 8-bit data conversion system. A voltage-output DAC, 8 bit up/down counter, stable 2.5V bandgap reference and clock generator are contained on a single chip.

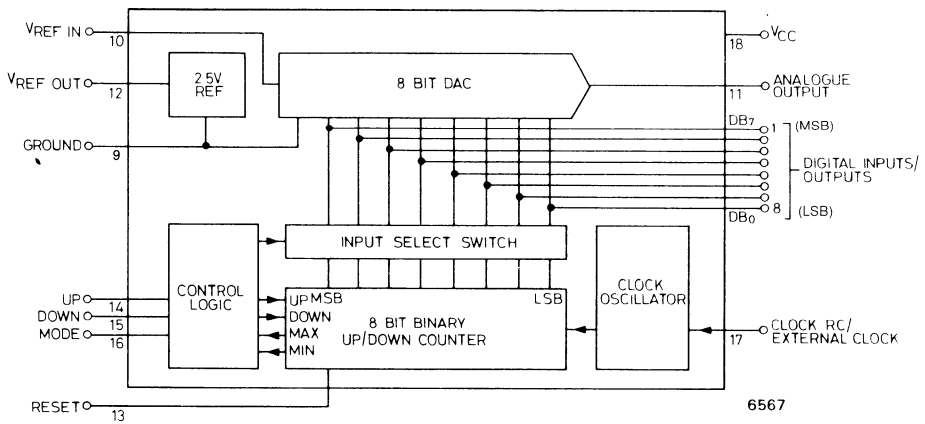


Fig. 1 SYSTEM DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .. .. +7.0 volts
Max. Voltage, Logic and V_{REF} inputs .. .. V_{CC}

Operating Temperature Range

TYPE	T_{min}(°C)	T_{max}(°C)
ZN435E	0	+70
ZN435J	−55	+125

Storage Temperature Range .. −55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, V_{REF} = 1.5−3.0V T_{amb} = +25°C unless otherwise stated).

Parameter	Min.	Typ.	Max.	Units	Conditions
D TO A CONVERTER					
Resolution	8	—	—	bits	
Linearity Error	—	±0.25	±0.5	L.S.B.	T_{min} T_{amb} T_{max}
Differential Linearity Error	—	±0.25	±1	L.S.B.	
Zero Error	—	5.0	10.0	mV	ZN435E All bits OFF
	—	5.0	10.0	mV	ZN435J
Settling time to 0.5LSB	—	500	—	ns	All bits OFF to ON or
	—	800	—	ns	vice versa
Full-scale output	2.545	2.550	2.555	V	All bits ON, V_{REF} = 2.56V
Output Resistance	—	4	—	k	
Full-scale Temperature Coefficient	—	4	—	ppm/°C	Ext V_{REF} = 2.56V
Reference Voltage	0	—	3	V	

Parameter	Min.	Typ.	Max.	Units	Conditions
On-chip Voltage Reference					
Output Voltage	2.4	2.59	2.7	V	R_{REF} = 390 ~
Slope Resistance	—	2	4	~	C_{REF} = 220n
Temperature Coefficient of V_{REF}	—	50	—	ppm/°C	
Reference Current	4	—	15	mA	
Counter (with external clock)					
High Level Threshold Voltage V_{T+}	—	—	2.3	V	
Low Level Threshold Voltage V_{T-}	1.7	—	—	V	
Maximum Clock Frequency	1	1.5	—	MHz	
On-chip Clock					
Maximum Frequency	500	—	—	KHz	
Clock Frequency Tempco	—	100	—	ppm/°C	
Clock Resistor	10	—	100	k	
Clock Capacitor	470	—	—	pF	
High Level Threshold Voltage V_{T+}	—	4.6	—	V	
Low Level Threshold Voltage V_{T-}	—	1.5	—	V	
Supply Rejection	—	0.8	—	%/V	
Logic Circuits					
BIT INPUTS					
High Level Input Voltage V_{IH}	2.0	—	—	V	
Low Level Input Voltage V_{IL}	—	—	0.8	V	
High Level Input Current I_{IH}	—	—	−100	µA	V_{IN} = 2.4V
Low Level Input Current I_{IL}	—	—	−220	µA	V_{IN} = 0.4V
BIT OUTPUTS					
High Level Output Voltage V_{OH}	—	5.0	—		No Load
Low Level Output Voltage V_{OL}	—	0.1	—		
High Level Output Voltage V_{OH}	2,4	—	—	V	I_{IH}= −40 µA
Low Level Output Voltage V_{OL}			0.4	V	I_{IL}= 2,5mA

Parameter	Min.	Typ.	Max.	Units	Conditions
CONTROL INPUTS					
High Level Input Voltage V_{IH}	2	—	—	V	
Low Level Input Voltage V_{IL}	—	—	0.8	V	
High Level Input Current I_{IH}	—	—	−25	µA	V_{IN} = 2.4V
Low Level Input Current I_{IL}	—	—	−95	µA	V_{IN} = 0.4V
Reset Pulse Width	200	—		nS	
Power Supply					
Supply Voltage	4.5	5	5.5	V	
Supply Current	—	35	45	mA	V_{CC} = 5.5V

GENERAL CIRCUIT OPERATION

The ZN435 incorporates an 8-bit DAC based on a voltage switching R-2R ladder network. The reference voltage for this ladder may be derived from the on-chip precision bandgap reference, or an external reference voltage may be supplied.

The ZN435 also contains an 8-bit up/down counter and control logic. The DAC may receive its digital input data from the counter, the counter outputs being simultaneously available at an 8-bit I/O port. Alternatively the counter outputs may be inhibited and the I/O port used to feed data direct to the DAC inputs.

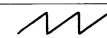
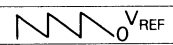
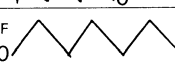
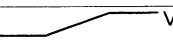
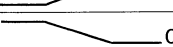
An on-chip oscillator is provided to drive the clock input of the up-down counter. The on-chip clock may be overridden by an external clock signal.

UP/DOWN COUNTER AND CONTROL LOGIC

The counter is a high-speed, synchronous up/down type, whose operation is determined by four control pins. The functions of the UP, DOWN and RESET inputs are fairly self explanatory. the MODE input determines the behaviour of the counter at zero and full-scale. When the MODE input is high the counter will reset to zero if it is clocked past full-scale in the UP direction and will reset to 255 if it is clocked past zero in the DOWN direction. When the MODE input is low the counter will stop on reaching full-scale or zero.

The normally invalid state of UP and DOWN inputs low simultaneously is also utilised in the ZN435. With the MODE input high and UP and DOWN inputs low the counter will cycle up and down continuously, reversing at full-scale and zero. With all three control inputs low the counter outputs are disabled and the DAC inputs are accessible from the I/O port.

A truth table for the control inputs is given in Table 1.

RESET	MODE	DOWN	UP	DIGITAL FUNCTION	ANALOGUE WAVEFORM
1	1	1	1	Counter Stopped.	
1	1	1	0	Count up continuously.	
1	1	0	1	Count down continuously.	
1	1	0	0	Count up, reverse at F.S., count down, reverse at zero.	
1	0	1	1	Counter Stopped.	
1	0	1	0	Count up, Stop at F.S.	
1	0	0	1	Count down, Stop at zero.	
X	0	0	0	DAC MODE, Counter output disabled. Counter can still be reset by taking reset input low.	
0	X	X	X	Counter reset. Does not affect analogue output in DAC MODE.	

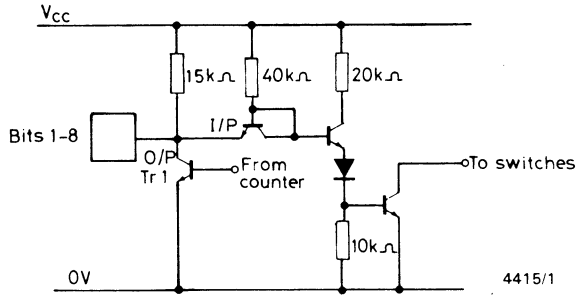


Fig. 2—BIT INPUTS/OUTPUTS

DATA PORT

One bit of the data port is shown in figure 2. The input/output pin is the junction of the counter output buffer and the DAC input buffer.

Normally the DAC is driven from the counter and the counter data is also available at the port. However, when the counter outputs are disabled the output transistors are turned off and the DAC inputs may be accessed from the data port.

The data port can drive or be driven from B-series CMOS and all TTL families.

CLOCK CIRCUIT

The on-chip clock circuit of the ZN435 is shown in figure 3.

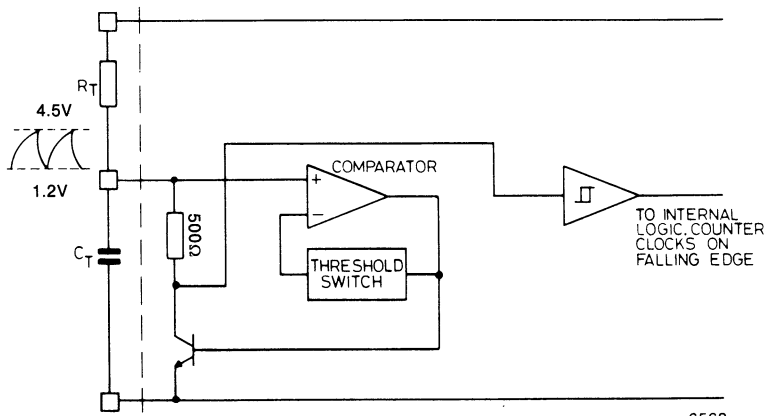


Fig. 3

The frequency of the clock is given by $f_{CLK} = \frac{1}{4R_TC_C}$ (Hz, ~, F)

Graphs of oscillator frequency versus resistor and capacitor values are given in figure 4.

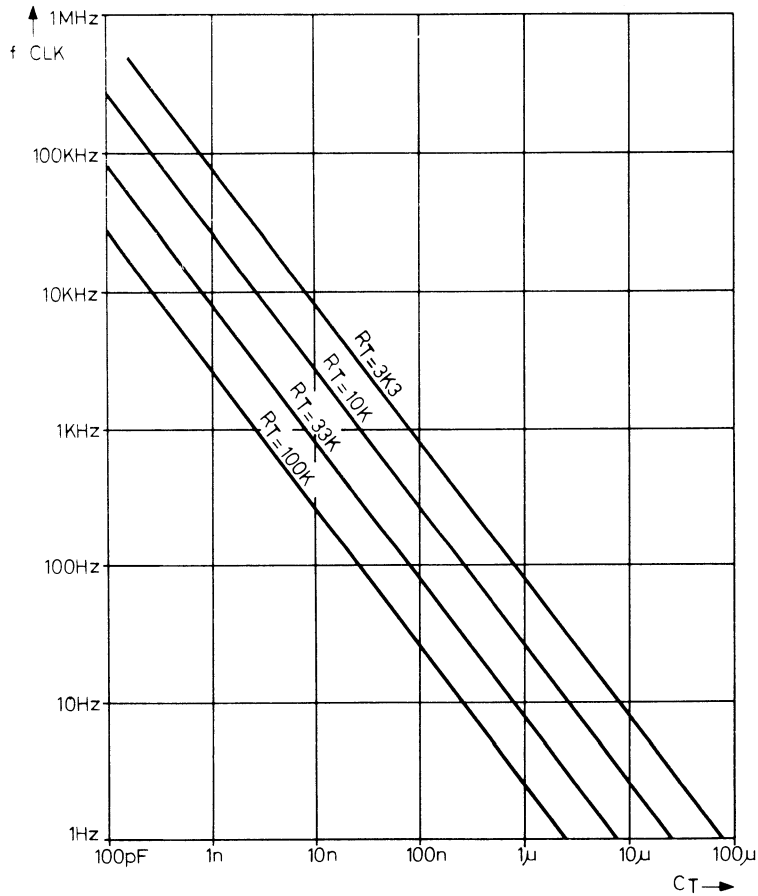


Fig. 4 6569

The external capacitor C_T is charged via the external resistor R_T to the upper threshold of the comparator (about +4.5V with V_{CC} = + 5V). The comparator turns on the discharge C_T and switches its threshold to the lower value of about 1.5V.
When the voltage on C_T has fallen to this level the comparator turns off the discharge transistor and the cycle repeats.

The clock can be overdriven direct from a TTL totem-pole output, as shown in Figure 5a. If open collector or CMOS-Gates are used then their V_{OH} must be attenuated to below 4.5V, as shown in Figures 5b and 5c.

The output low, V_{OL}, may be the normal low level for either CMOS or open collector output.
This slightly complicated arrangement, has the advantage that the clock can be overdriven without turning-on the discharge transistor, provided that the drive voltage V_{OH}-level does not exceed 4.5V.

With these thresholds the Schmitt-Trigger delivers clock pulses to the internal logic.

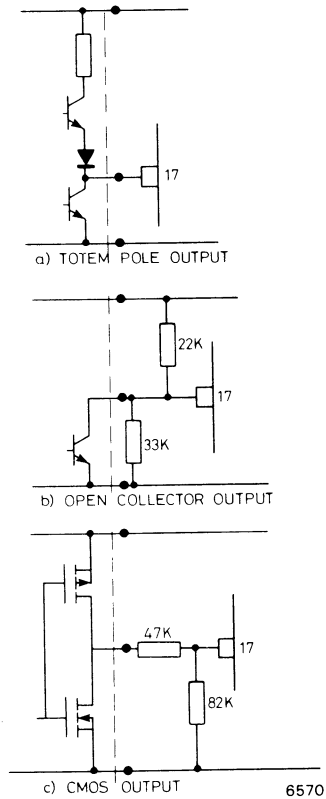


Fig. 5. OVERDRIVING THE CLOCK INPUT

ANALOGUE CIRCUITS

D TO A CONVERTER

The DAC is of the voltage switching type and uses an R-2R ladder network as shown in figure 6.

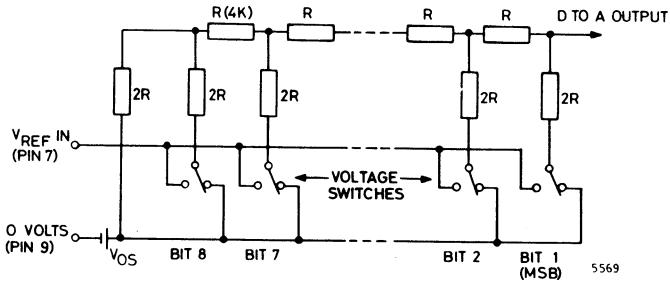


Fig. 6 R2-R LADDER NETWORK

Each 2R element is connected to either OV or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder.

$$V_{OUT} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input from the counter or data port.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of V_{OS} is typically 3mV for the ZN435E and 5mV for the ZN435J. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is small the zero drift will be small. The DAC output range can be considered to be 0 volts to $V_{REF\ IN}$ with an output resistance R (4kΩ).

REFERENCE

ON-CHIP REFERENCE
The internal reference is an active bandgap circuit which is equivalent to a 2.5V zener diode with a very low slope impedance (Fig. 7).

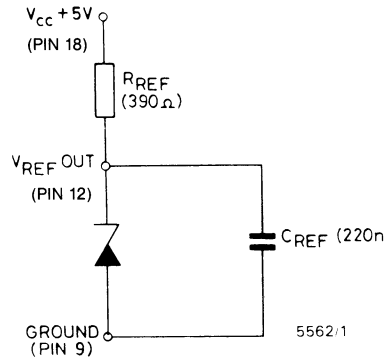


Fig. 7 INTERNAL VOLTAGE REFERENCE

An external resistor (R_{REF}) should be connected between pins 12 and 18 to bias up the on-chip reference, whilst a stabilising/decoupling capacitor (C_{REF}) is required between pins 12 and 9.

To use the internal reference $V_{REF\ OUT}$ (Pin 12) is connected to $V_{REF\ IN}$ (Pin 10).

The recommended reference resistor of 390Ω will supply a nominal reference current of 6.4mA which is sufficient to drive the reference inputs of up to five ZN435s. Where several ZN435s are used in a system this useful feature can save up to four resistors and capacitors as well as reducing power consumption and giving excellent gain tracking.

APPLICATIONS

The applications of the ZN435 are too many and varied to detail in this data sheet. However a few basic configurations are illustrated.

WAVEFORM GENERATOR

The circuit of a low-frequency waveform generator is illustrated in figure 8.

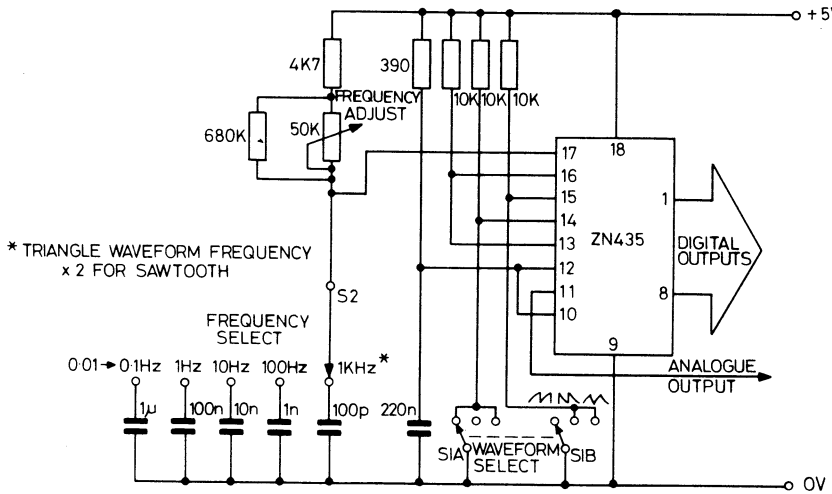


Fig. 8 WAVEFORM GENERATOR 6571

This will produce stable, linear, sawtooth and triangle waveforms.

RAMP AND COMPARE A TO D CONVERTER

A simple ramp and compare A to D converter can be constructed using the ZN435 and an external comparator, as shown in figure 9.

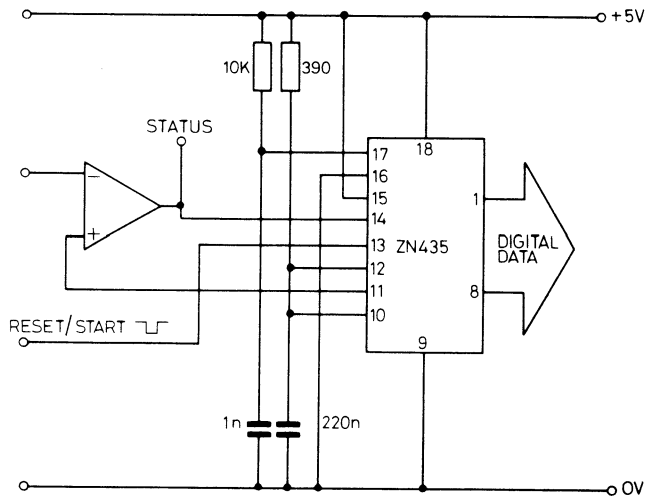


Fig. 9 RAMP AND COMPARE ADC 6572

The counter is set to count up from zero, producing a positive-going ramp at the analogue output. When the ramp voltage exceeds the analogue input the comparator output will go high, inhibiting the clock and stopping the counter. The converter can be reset and re-started by applying a low-going pulse to the reset input.

The basic analogue input range is $0 - V_{REF}$, but other ranges can be accommodated by adding an attenuator to the comparator input. The comparator offset adjustment can be used for zero adjustment. Note that in this circuit the mode input is tied low to make the counter stop at full-scale. This prevents the counter cycling in the event of an overrange input.

TRACKING A TO D CONVERTER

The on-chip up-down counter allows the ZN435 to be configured very simply as a tracking A to D converter using an external comparator, as shown in figure 10.

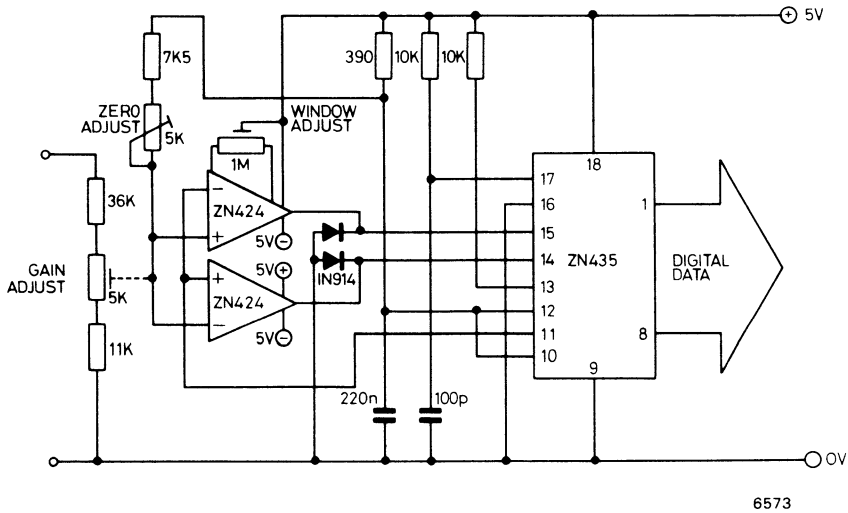


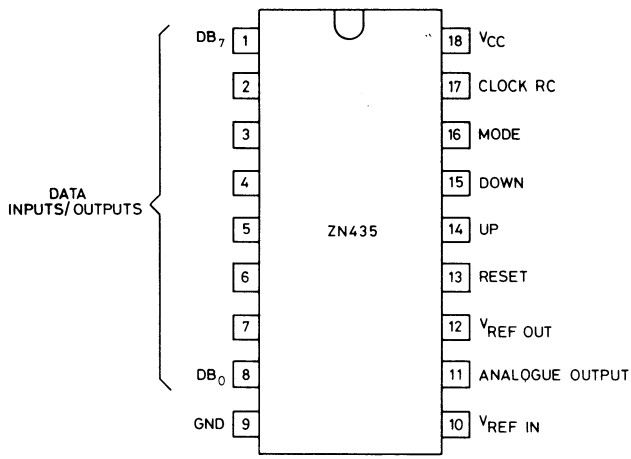
Fig. 10 TRACKING ADC

In this circuit two ZN424 op amps are used to make a window comparator. This has a deadband equal to one LSB of the DAC output (10mV), which is set by adjusting the offset of A1 until its threshold is 10mV above that of A2.

Whenever the analogue voltage is above the threshold of A1 the counter will count up so that the DAC output increases to follow the analogue voltage. Whenever the analogue voltage is below the threshold of A2 the counter will count down to make the DAC follow the analogue voltage. When the analogue voltage is between the two thresholds the outputs of A1 and A2 will be high and the counter will be stopped.
The circuit here has an analogue input range of $\pm$10V. Other ranges may be accommodated by suitable choice of input resistors.

Note that in this circuit the mode input is tied low. This causes the counter to stop when full-scale or zero is reached, i.e. when the analogue input exceeds plus or minus full-scale. Without this feature the counter would simply cycle continuously.

PIN CONNECTIONS



6574

FERRANTI semiconductors

ZN436E/J

6 Bit D/A-Converter, Low Cost

ADVANCE PRODUCT INFORMATION

FEATURES

- 6-bit Accuracy
- ZN436E Commercial Temp. Range 0°C to +70°C
- ZN436J Military Temp. Range −55°C to +125°C
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time 1 μsec. Typical
- Designed for low-cost applications

DESCRIPTION

The ZN436 is a monolithic 6-bit digital to analogue converter containing an R-2R ladder network of diffused resistors with precision bipolar switches.

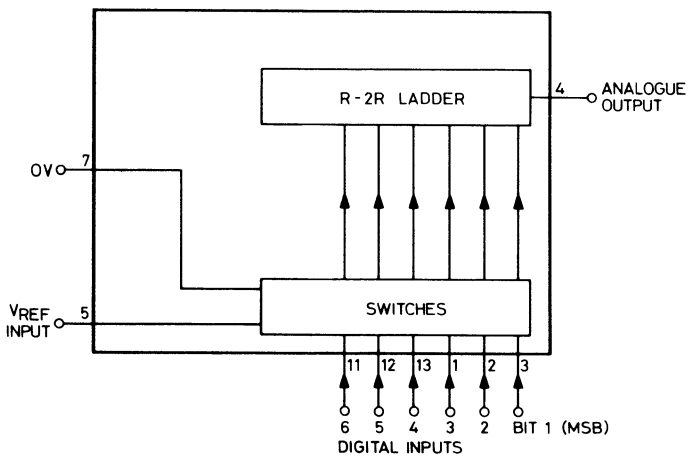


Fig. 1. SYSTEM DIAGRAM

ZN436E/J

INTRODUCTION

The ZN436 is a 6-bit digital to analogue converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches on a single monolithic chip.

The special design of ladder network results in full 6-bit accuracy using normal diffused resistors.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

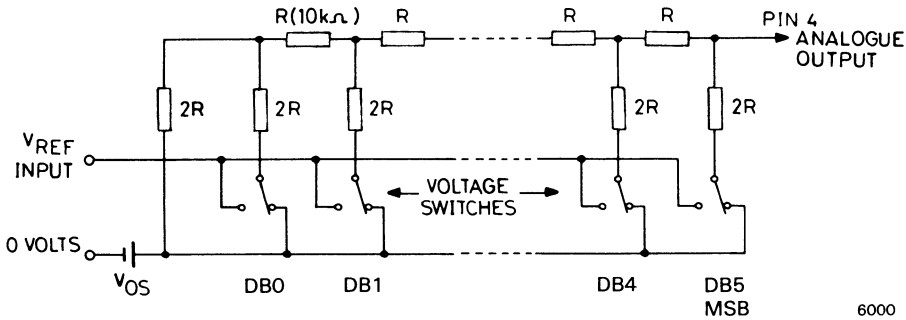


Fig. 2 THE R-2R LADDER NETWORK

Each 2R element is connected either to OV or V_{REF} by transistor switches specially designed for low offset voltage (typically 1 millivolt).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

An external fixed or varying reference is required which should have a slope resistance less than 2 ohms.

Suggested external reference sources are the ZN404 or one of the ZN458 range. Each ZN404 is capable of supplying up to five ZN436 circuits and this is increased to ten for the ZN458 range.

ORDERING INFORMATION

Operating Temperature	6-bit accuracy			Package
0 to +70°C	ZN436E			Plastic
−55 to +125°C	ZN436J			Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7.0 volts
Max. voltage, logic and V_{REF} inputs .. .. +5.5 volts
Storage temperature range .. .. .. −55 to +125°C

CHARACTERISTICS (at T_{amb} = 25°C and V_{CC} = +5 volts unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Converter Resolution			—	—	bits	
Accuracy (useful resolution) ZN436J		6	—	—	bits	V_{REF} input = 2.0 to 3.0 volts
ZN436E		6	—	—	bits	
Non-linearity		—	—	±0.5	L.S.B.	*Note 1*
Differential non-linearity		—	±0.5	—	L.S.B.	*Note 2*
Settling time to 0.5 L.S.B.		—	1.0	—	μs	1 L.S.B. step
Settling time ot 0.5 L.S.B.		—	2.0	—	μs	All bits ON to OFF or OFF to ON
Offset voltage ZN436J	V_{OS}	—	5.0	8.0	mV	All bits OFF *Note 1*
ZN436E		—	3.0	5.0	mV	
V_{OS} temperature coefficient		—	5	—	μV/°C	
Full scale output		2.510	2.520	2.530	volts	All bits ON Ext V_{REF} = 2.560V
Full scale temp. coefficient		—	3	—	ppm/°C	Ext. V_{REF} = 2.560V
Non-linearity temp. coeff.		—	7.5	—	ppm/°C	Relative to F.S.R.

CHARACTERISTICS (*continued*)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Analogue output resistance	R_O	–	10	–	kΩ	
External reference voltage		0	–	3.0	volts	
Supply voltage	V_{CC}	4.5	–	5.5	volts	
Supply current	I_S,	–	5	9	mA	
High level input voltage	V_{IH}	2.0	–	–	volts	
Low level input voltage	V_{IL}	–	–	0.7	volts	
High level input current	V_{IH}	–	–	10	μA	V_{CC} = max., V_I = 2.4V
		–	–	100	μA	V_{CC} = max., V_I = 5.5V
Low level input current	I_{IL}	–	–	−0.18	mA	V_{CC} = max., V_I = 0.3V

APPLICATIONS

1. 6-bit D to A Converter

The ZN436 gives an analogue voltage output directly from pin 4 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the Analogue Output Resistance R_O, will be less than 0.004% per °C (or 1 L.S.B./100°C) if R_L is chosen to be $>$ 650kΩ

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 3 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until V_{out} = 0.000V.

ii. Set all bits to ON (high) and adjust R_1 until V_{out} = Nominal full scale reading −1 L.S.B.

iii. Repeat *i.* and *ii.*

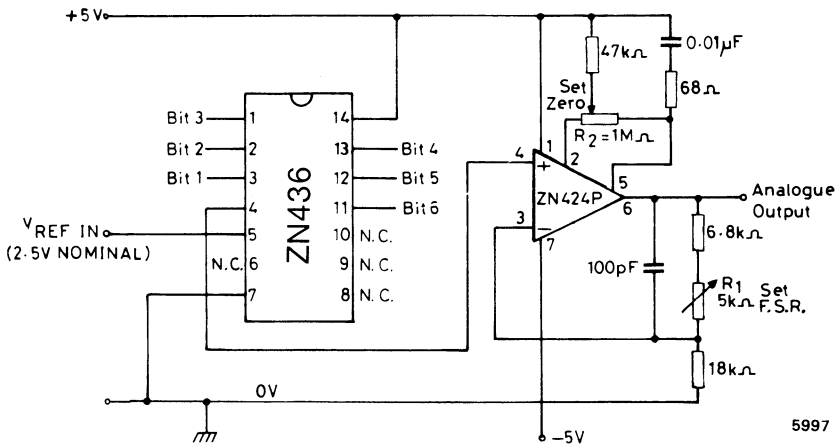


Fig. 3 6-BIT DIGITAL TO ANALOGUE CONVERTER

Alternative Output Buffer using the ZLD741

The following circuit, employing the ZLD741 operational amplifier, may be used as the output buffer (Fig. 3).

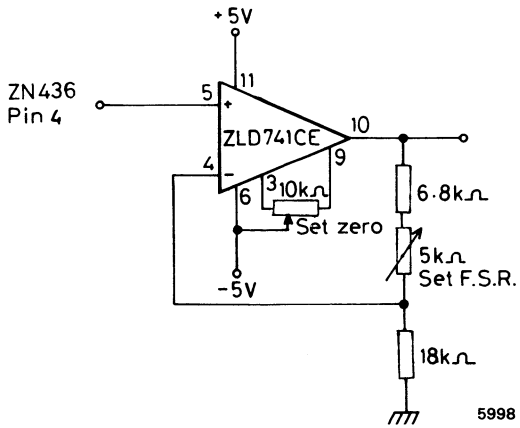
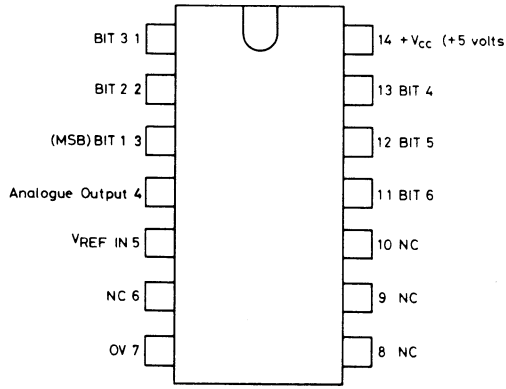


Fig. 4 THE ZLD741 AS OUTPUT BUFFER

PIN CONNECTIONS



6596

FERRANTI semiconductors

ZN558E-8
ZN558J-8

8 Bit DAC with latched Input

ADVANCE PRODUCT INFORMATION

FEATURES

- Contains DAC with data latch and on-chip reference
- Guaranteed monotonic over the full operating temperature range
- Single +5V supply
- Microprocessor compatible
- TTL and 5V CMOS compatible
- 800ns settling time
- Complementary to ZN447 A to D Series
- ZN558E-8 commercial temperature range 0 to +70°C
- ZN558J-8 military temperature range −55 to +125°C

GENERAL DESCRIPTION

The ZN558 is a Monolithic 8 bit D to A converter with input latches to facilitate updating from a data bus. The latch is transparent when Enable is LOW and the data is held when Enable is taken HIGH. The ZN558 also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

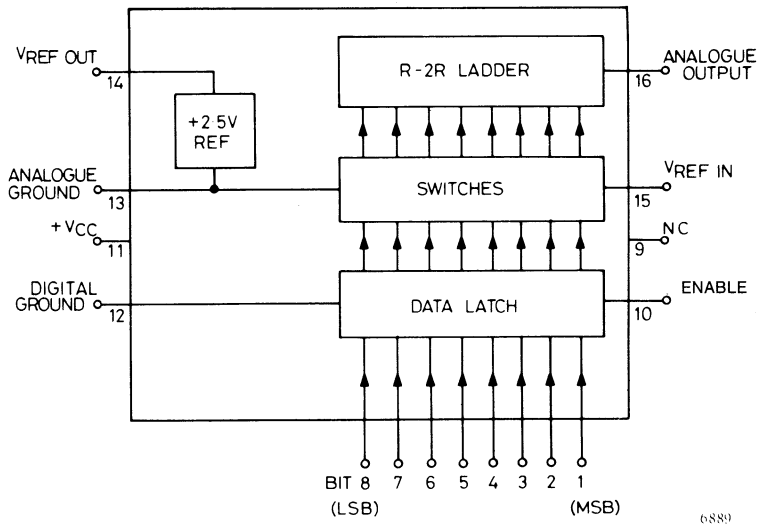


Fig. 1 System Diagram

ZN558E-8/J-8

ABSOLUTE MAXIMUM RATING

Supply voltage V_{CC}	+7.0 volts
Max. voltage, logic and V_{REF} input	$+V_{CC}$
Operating temperature range	0 to +70°C (ZN558E-8)
	−55 to +125°C (ZN558J-8)
Storage temperature range	−55 to +125°C
Analogue Ground to Digital Ground	±200mV

ELECTRICAL CHARACTERISTICS (V_{CC} = +5 volts, T_{amb} = 25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
Internal Voltage Reference					
Output voltage	2.475	2.550	2.625	volts	R_{REF} = 390Ω, C_{REF} = 1μF
Slope resistance		0.5	2	Ω	
$V_{REF\ OUT}$ T.C.		50		ppm/°C	
Reference current	4		15	mA	Note 1
D to A Converter					
Linearity error			±0.5	LSB	2.0V ≤ $V_{REF\ IN}$ ≤ 3.0V
Differential non-linearity		±0.5		LSB	
Linearity error T.C.		±3		ppm/°C	
Differential non-linearity T.C.		±6		ppm/°C	
Offset voltage		2	5	mV	All bits OFF
Offset voltage		±6		μV/°C	
Full scale output	2.545	2.550	2.555		External reference $V_{REF\ IN}$ = 2.560 volts, all bits ON
Full scale output T.C.		2		ppm/°C	
Analogue output resistance		4		kΩ	
External reference voltage	0		3.0	volts	
Settling time to 0.5 LSB		800		ns	1 LSB Major Transition (Note 2)
		1.25		μs	All bits ON to OFF or OFF to ON (Note 2)
Operating temperature range:					
ZN558E-8	0		70	C	
ZN558J-8	−55		125	C	
Supply voltage (V_{CC})	4.5	5.0	5.5	volts	

Note 1 See REFERENCE, page 4.

Note 2 R_L = 10MΩ, C_L = 10pF.

ELECTRICAL CHARACTERISTICS *(continued)*

	Min.	Typ.	Max.	Units	Conditions
Supply current		20	30	mA	Note 3
Power consumption		100		mW	
Logic (over specified operating temperature range)					
High level input voltage	2.0			V	
Low level input voltage			0.8	V	
High level input current			60	μA	$V_{IN} = 5.5V$, $V_{CC} = Max.$
			20	μA	$V_{IN} = 2.4V$, $V_{CC} = Max.$
Low level input current			−5	μA	$V_{IN} = 0.4V$, $V_{CC} = Max.$
Input Clamp Diode Voltage		−1.5		V	$I_{IN} = -8mA$
Enable pulse width	100			ns	
Data set-up time	150			ns	Note 4
Data hold time	10			ns	Note 5

Note 3 All inputs HIGH ($V_{IH} = 3.5$ volts).
Note 4 Set up time before $\overline{\text{Enable}}$ goes high.
Note 5 Hold time after $\overline{\text{Enable}}$ goes high.

D to A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 2. Each 2R element is connected to 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder.

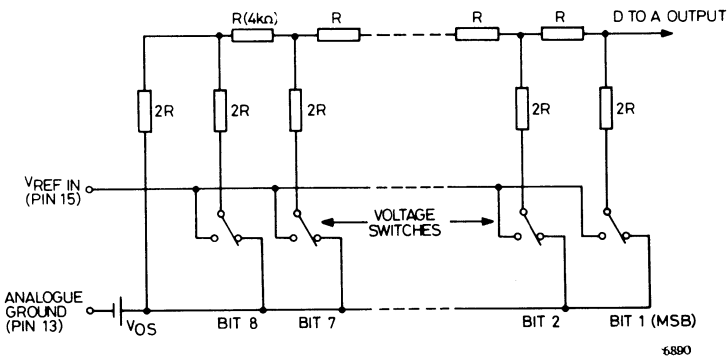


Fig. 2 The R-2R Ladder Network

$$\text{Analogue Output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D to A from the data latch.

V_{OS} is a small offset voltage produced by the D to A switch currents flowing through the package lead resistance. The value of V_{OS} is typically 1mV. This offset will normally be removed by the setting up procedure (see APPLICATIONS section) and because the offset temperature coefficient is low ($\pm 6\mu V/°C$) the effect on accuracy is negligible.

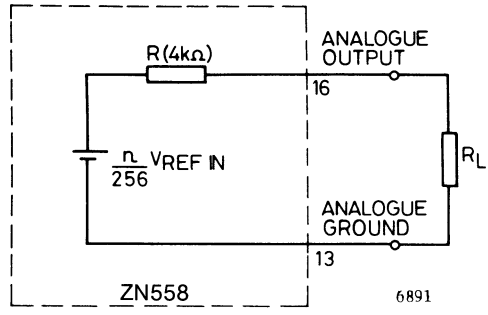


Fig. 3 Analogue Output Equivalent Circuit

Fig. 3 shows an equivalent circuit of the output (ignoring V_{OS}). The output resistance R has a temperature coefficient of +0.2% per °C.

The gain drift due to this is $\frac{0.2R}{R + R_L}$ % per °C

R_L should be chosen to be as large as possible to make the gain drift small. As an example if $R_L = 400k\Omega$ then the gain drift due to the T.C. of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN558 can be buffered by an amplifier (see APPLICATIONS section).

REFERENCE

(a) Internal Reference

The internal reference is an active band gap circuit which is equivalent to a 2.5 volt Zener diode with a very low slope impedance (Fig. 4). A resistor (R_{REF}), should be connected between $+V_{CC}$ (pin 11) and pin 14. The recommended value of 390Ω will supply a nominal reference current of (5.0-2.5)/0.39 = 6.4mA. A stabilising/decoupling capacitor $C_{REF} = 1\mu F$ is required between pins 14 and 13 for internal reference option, $V_{REF\ OUT}$ (pin 14) being connected to $V_{REF\ IN}$ (pin 15).

Up to five ZN558's may be driven from one internal reference (there is no need to reduce R_{REF}). This useful feature saves power and gives excellent gain tracking between the converters.

(b) External Reference

If required an external reference voltage may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5}{n}\Omega$, where n is the number of converters supplied.

$V_{REF\ IN}$ can be varied from 0 to +3 volts for ratiometric operation. The ZN558 is guaranteed monotonic for $V_{REF\ IN}$ above 2 volts.

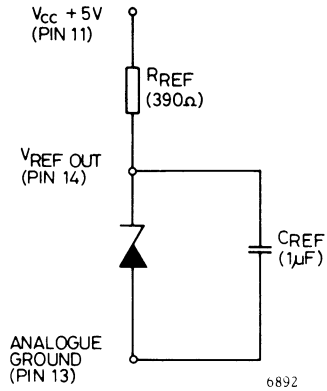


Fig. 4 Internal Voltage Reference

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the Enable input is low the data inputs drive the D to A directly. When Enable goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig.5.

The ZN558 is provided with seperate analogue and digital ground connections. The circuit will operate correctly with as much as ± 200mV between the two grounds.

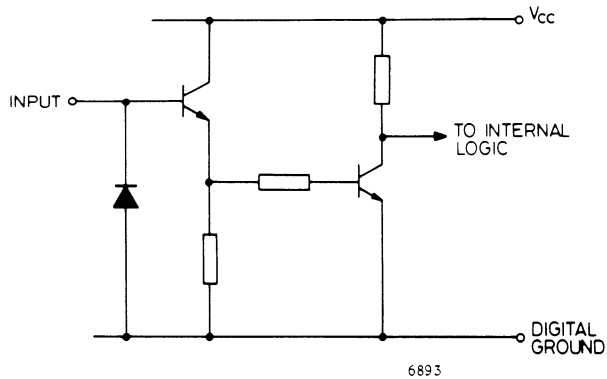


Fig. 5 Equivalent Circuit of All Inputs

APPLICATIONS

(1) Unipolar D to A Converter

The nominal output range of the ZN558 is 0 to $V_{REF\ IN}$ through 4kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The general scheme (Fig. 6) is suitable for amplifiers with input bias currents less than 1.5μA.

The resulting full scale range is given by

$$V_{OUT}\ FS = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.V_{REF\ IN}$$

The impedance at the inverting input is R1/R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (4kΩ) The required nominal values of R1 and R2 are given by R1 = 4GkΩ and R_2 = 4G/(G-1)kΩ.

Using these relationships a table of nominal resistance values for R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5 volts.

Output Range	G	R_1	R_2
+ 5V	2	8kΩ	8kΩ
+ 10V	4	16kΩ	5.33kΩ

For gain setting R_1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for + 5V and + 10V output ranges are given in Fig. 7. Settling time for a major transistion is 1.5μs typical.

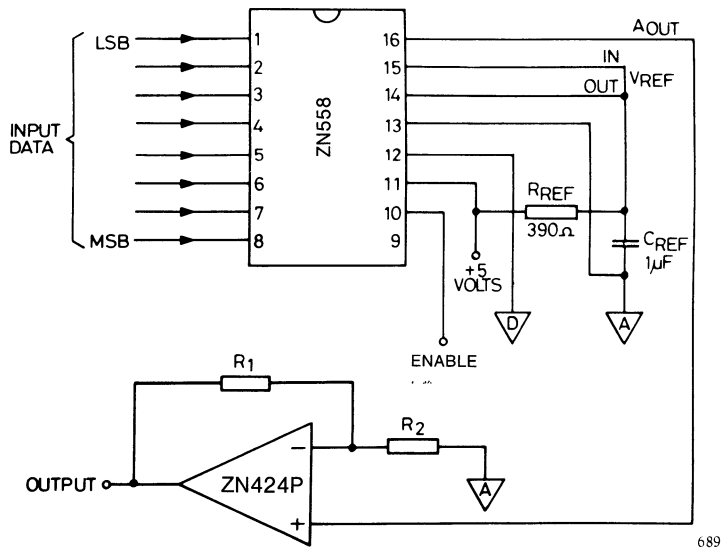
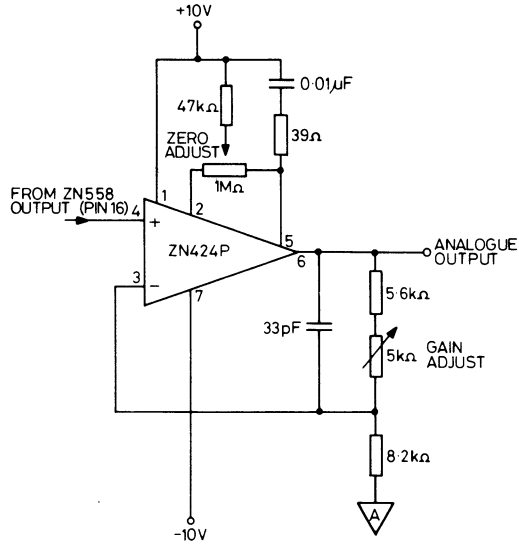


Fig. 6 Unipolar operation - Basic Circuit



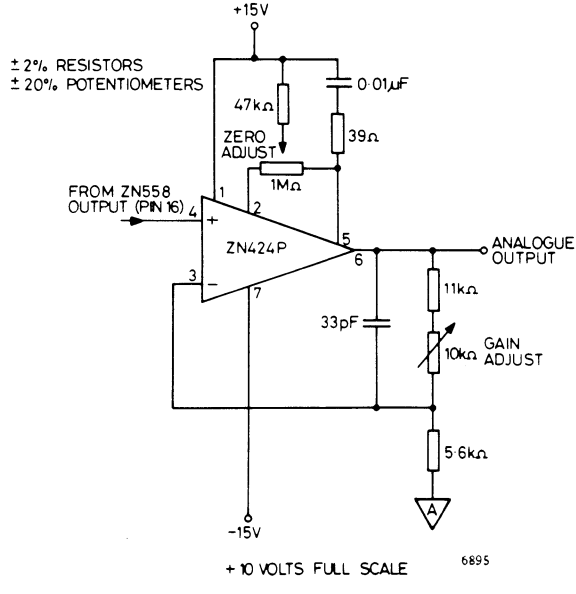


Fig. 7 Unipolar Operation - Component Values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{Enable}}$ low and adjust zero until $V_{OUT} = 0.0000V$.
(ii) Set all bits ON (high) and adjust gain until V_{OUT} FS 1LSB.

UNIPOLAR SETTING UP POINTS

Output Range, +FS	LSB	FS - 1LSB
+5V	19.5mV	4.9805V
+10V	39.1mV	9.9609V

$$1LSB = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Input Code (Binary)	Analogue Output (Nominal value)
11111111	FS - 1LSB
11111110	FS - 2LSB
11000000	¾ FS
10000001	½FS + 1LSB
10000000	½FS
01111111	½FS - 1LSB
01000000	¼FS
00000001	1LSB
00000000	0

(2) Bipolar D to A Converter

For bipolar operation the output from the ZN558 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig. 8).

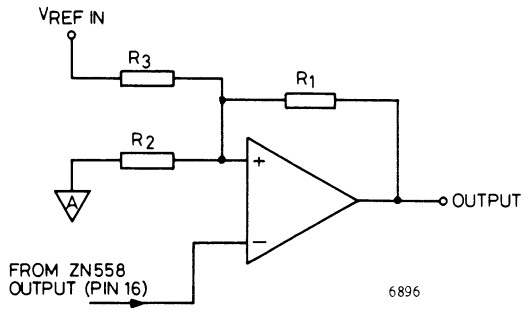


Fig. 8 Bipolar Operation - Basic Circuit

When the digital input to the ZN558 is zero the analogue output is zero and the amplifier output should be −Full scale. An input of all ones to the D to A will give a ZN558 output of $V_{REF\ IN}$ and the amplifier output required is +Full scale. Also, to match the ladder resistance the parallel combination of R_1, R_2 and R_3 should be 4kΩ.

The nominal values of R_1, R_2 and R_3 which meet these conditions are given by

$$R_1 = 8Gk\Omega,\ R_2 = 8G/(G-1)k\Omega \text{ and } R_3 = 8k\Omega$$

where the resultant output range is $\pm G\ V_{REF\ IN}$.

A bipolar output range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) is obtained if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5$ volts the nominal values of resistors for ±5V and ±10V output ranges are given in the following table:

Output Range	G	R_1	R_2	R_3
±5V	2	16kΩ	16kΩ	8kΩ
±10V	4	32kΩ	10.66kΩ	8kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig. 9. Note that in the ±5V case R_3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to get a more symmetrical range of adjustment using standard potentiometers. Settling time for a major transition is 1.5μs typical.

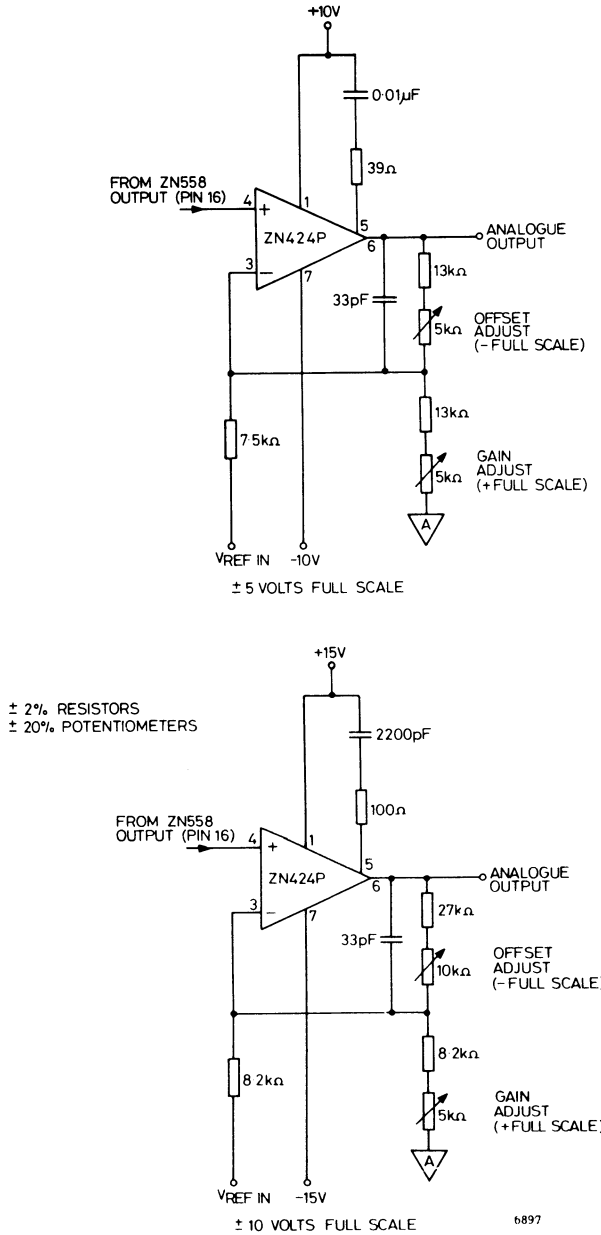


Fig. 9 Bipolar Operation - Component Values

Bipolar Adjustment Procedure

(1) Set all bits to OFF (low) with $\overline{\text{Enable}}$ low and adjust offset until the amplifier output reads – Full scale.

(2) Set all bits ON (high) and adjust gain until the amplifier output reads + (Full Scale - 1LSB).

BIPOLAR SETTING UP POINT

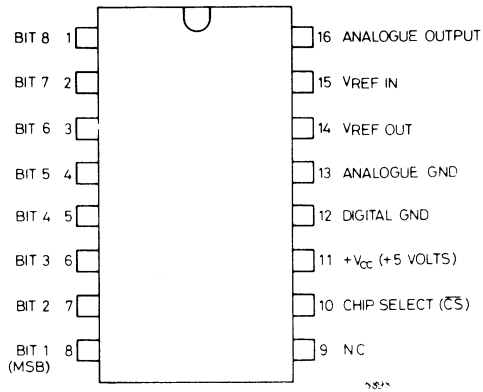
Input Range, ±FS	LSB	– FS	+ (FS - 1LSB)
± 5V	39.1mV	– 5.0000V	+ 4.9609V
± 10V	78.1mV	– 10.0000V	+ 9.9219V

$$1LSB = \frac{2FS}{256}$$

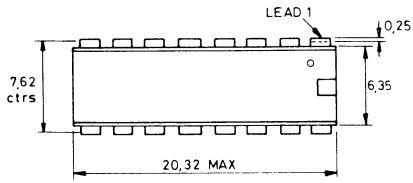
BIPOLAR LOGIC CODING

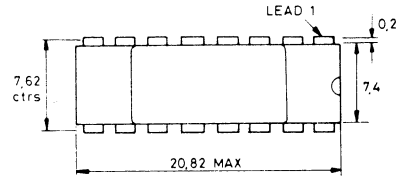
Input Code (Offset Binary)	Analogue Output (Nominal value)
11111111	+ (FS - 1LSB)
11111110	+ (FS - 2LSB)
11000000	+ ½ FS
10000001	+ 1LSB
10000000	0
01111111	– 1LSB
01000000	– ½ FS
00000001	– (FS - 1LSB)
00000000	– FS

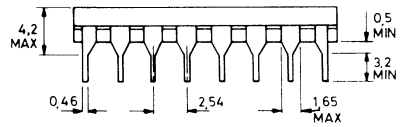
PIN CONNECTIONS



PACKAGE DETAILS

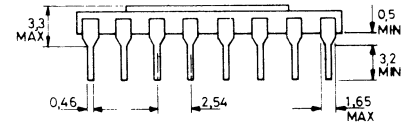






4681 MD/1

16 - Lead Moulded D.I.L.



5365 C/1

16 - Lead Ceramic D.I.L.

Dimensions in millimetres

2. Analogue-to-Digital Converters

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ZN448	8 Bit ADC, ½LSB Version of ZN447	2-77
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ZN450	3½Digit DVM Circuit for direct LC-Display Drive 200mV FS	2-99
ZN451	3½Digit DVM Circuit for direct LC-Display Drive 2 mV FS	2-122
ZN501/2	10 Bit ADC µP-compatible, Tristate outputs	2-146
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ZNA216	3¾Digit DVM Circuit for MPX-LED-Displays	2-176
ZN412	Digital Clinical Thermometer	2-192

PRODUCT SELECTION GUIDE A TO D CONVERTERS

TYPE	USEFUL RESOLUTION (BITS)	CONVERSION TIME (μs)	CONVERSION METHOD	ON-CHIP REFERENCE	TEMPERATURE RANGE (°C)	FEATURES	PAGE
ZN425E Series	8-6	1000	Ramp and compare	+	0 to 70	Low cost dual purpose A/D-D/A converter	1-11
ZN425J	8	1000	Ramp and compare	+	-55 to +125	Low cost dual purpose A/D-D/A converter	1-11
ZN427E-8	8	10	Succ. Approx.	+	0 to 70	Microprocessor, TTL and CMOS compatible	2-15
ZN427-J8	8	10	Succ. Approx.	+	-55 to +125	Microprocessor, TTL and CMOS compatible	2-15
ZN432 Series	10-8	15	Succ. Approx.	+	0 to 70	Parallel/serial Output, TTL and CMOS compatible	2-33
ZN432 Series	10-8	15	Succ. Approx.	+	-55 to +125	Parallel/serial Output, TTL and CMOS compatible	2-33
ZN433 Series	10-8	1(ΔU_{in}=1LSB)	Tracking	+	0 to 70	Parallel/serial Output, TTL and CMOS compatible	2-51
ZN433 Series	10-8	1(ΔU_{in}=1LSB)	Tracking	+	-55 to +125	Parallel/serial Output, TTL and CMOS compatible	2-51
ZN435E	8	800	Ramp and compare	+	0 to 70	Dual purpose A/D-D/A converter (up/down counter)	1-47
ZN435J	8	800	Ramp and compare	+	-55 to +125	Dual purpose A/D-D/A converter (up/down counter)	1-47
ZN440/441	6	0.06	Parallel (Flash)	-	0 to 70	Ultra fast monolithic Video A/D converter	2-61
ZN447-449E Series	8-6	9	Succ. Approx.	+	0 to 70	Clock generator, Microproc. TTL and CMOS compatible	2-77
ZN447-449J Series	8-6	9	Succ. Approx.	+	-55 to +125	Clock generator, Microproc. TTL and CMOS compatible	2-77
ZN450E, CJ	3 ½ Digit BCD	250ms	Charge balancing	+	0 to 70	Single chip DVM for direct LCD drive	2-99
ZN451E, CJ	3 ½ Digit BCD	250ms	Charge balancing	+	0 to 70	as ZN450, Full scale 1.999 mV	2-122
ZNA116E	3 ½ Digit BCD	160ms	Dual Slope	-	0 to 70	DVM logic subsystem for LED MPX display	2-162
ZNA216E, J	3 ¾ Digit BCD	160ms	Dual Slope	-	0 to 70	DVM logic subsystem for LED MPX display	2-176
ZN501/502	10	15	Succ. Approx.	+	-55 to +125	Three state output Processor compatible	2-146
ZN412	3 Digit	5 sec.	–	+	0 to 70	Thermometer 35°C to 47,6°C	2-192

2. ANALOGUE TO DIGITAL CONVERTERS

An analogue to digital Converter (ADC) is a device which converts an analogue input into a corresponding digital output code.

2.1 Ideal Output Characteristics

Assuming a unipolar input voltage and binary coded output, the transfer function of an ideal n-bit ADC is given by:

$$V_{FS}\ (B_1.2^{-1} + B_2.2^{-2} + \ldots . + B_n.2^{-n}) = V_{in} \pm \tfrac{1}{2}LSB$$

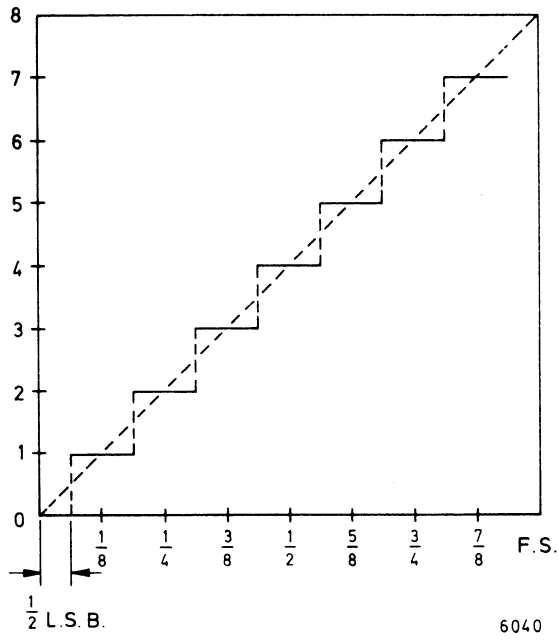


Fig. 9. Ideal 3-bit ADC Transfer Characteristic

The transfer function of an ideal 3-bit ADC is shown in figure 9. In this case there are 8 digital output codes corresponding to the 8 input codes of a DAC. However, unlike the analogue output of a DAC, the analogue input of an ADC can vary continuously, which means that each digital output code, with the exception of 0 and 7, exists over an analogue increment of 1 LSB. The zero of an ADC is usually trimmed so that the transitions between codes occur $\frac{1}{2}$ LSB on either side of the nominal analogue input for a particular code. For example, the nominal input for output code 2 is $\frac{1}{4}$ V_{FS}. The transition from 1 to 2 occurs at $\frac{3}{16}$ V_{FS} and the transition from 2 to 3 occurs at $\frac{5}{16}$ V_{FS}.

As with a DAC, an 'ideal' straight line may be drawn through the transfer characteristic of an ADC.

A to D Converters

2.2 Practical A to D Conversion Methods

There are many methods of performing an analogue to digital conversion. Although not all of these methods are used in the current range of Ferranti A-D converters, they are all, nonetheless, mentioned for the sake of completeness.

2.2.1 Parallel (Flash) Conversion

In an n-bit parallel converter (Fig. 10) a resistor ladder is used to generate $2^n - 1$ voltage levels from 1 LSB to $(2^n - 1) \times$ LSB which are fed to the reference inputs of $2^n - 1$ voltage comparators. The analogue input signal is fed to the second input of each comparator, and is thus compared simultaneously with each of the $2^n - 1$ voltage levels. At the point in the comparator chain where the reference voltage exceeds the input voltage the comparator outputs will change over from low to high. The comparator outputs are encoded into whatever digital output coding is required.

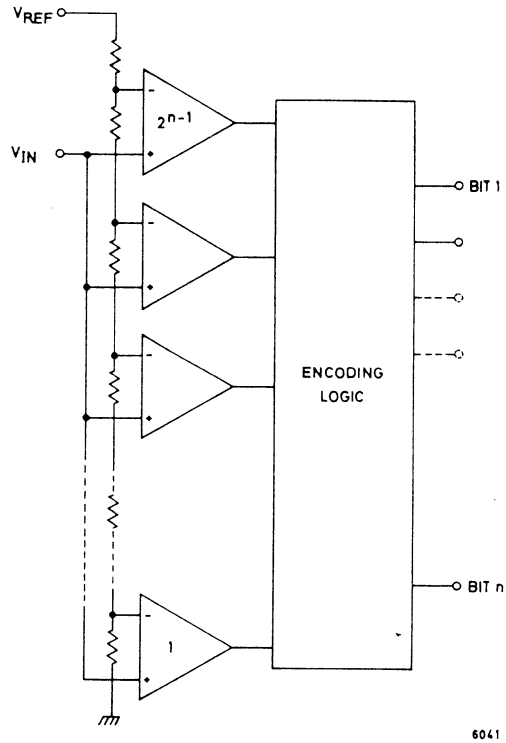


Fig. 10. Parallel A-D Converter

Since the only delays involved in the conversion are the propagation delay of one comparator plus the logic propagation delays, parallel converters are very fast and may perform in excess of 10 million conversions per second. However, due to the large number of comparators required (63 for a 6-bit converter, 255 for an 8-bit converter) they are expensive to produce. Applications include digital video systems, digital storage oscilloscopes and radar data processing.

2.2.2 Staircase and Comparator

In this type of ADC the input code of a DAC is incremented by a binary counter to give a staircase waveform, as shown in figure 11. This is compared with the analogue input and when the staircase exceeds the analogue voltage the comparator output changes state and stops the clock. The count reached by the binary counter is thus the ADC output code. This method of A to D conversion is relatively simple and cheap, but is also relatively slow, requiring $2^n - 1$ clock pulses for a full scale conversion, where n is the number of bits. This conversion method is used in the ZN425 series of dual-purpose D-A/A-D converters.

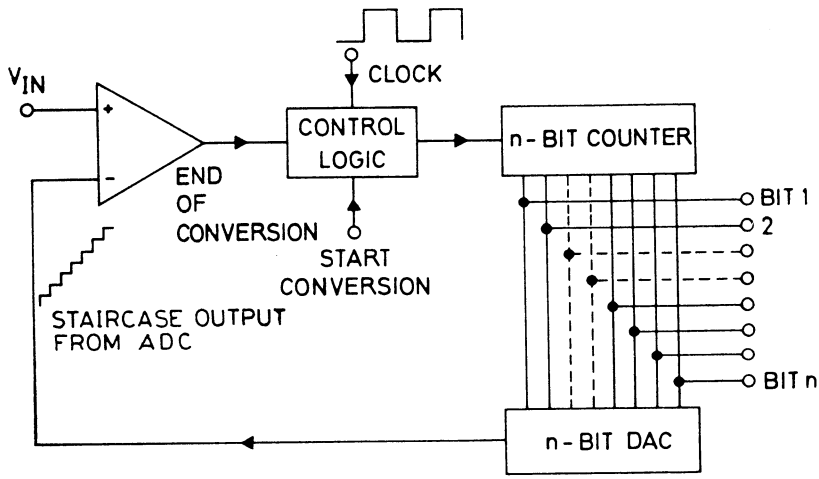


Fig. 11. Staircase (Ramp) and Compare ADC

2.2.3 Tracking Converters

As its name implies, a tracking converter can follow changing analogue inputs. The principle operation is similar to that of the staircase and compare type of converter, but it uses an up/down counter and a window comparator, as shown in figure 12. When the DAC output is less than the analogue input the comparator instructs the counter to count up and the DAC output thus increases. If the DAC output is greater than the analogue input the comparator causes the counter to count down, thus decreasing the DAC output. When the DAC output is equal to the analogue input $\pm\frac{1}{2}$ LSB, the input is within the 'window' of the comparator and the counter is stopped. This is illustrated in figure 13. A tracking converter has speed advantages over a staircase and compare type, since the counter of the latter type can only count up, and must therefore be reset between conversions. In the case of a tracking converter, once it has performed an initial conversion starting from zero, any subsequent conversions require only that number of clock pulses necessary to track any increase or decrease in input voltage.

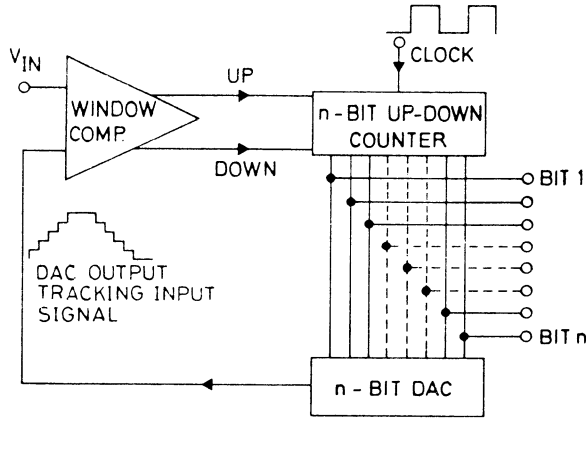


Fig. 12. Tracking ADC

As an extreme example consider an analogue input that changes from V_{FSO} to (V_{FSO} −1 LSB). The staircase and compare converter will require 2^n −1 clock pulses for the first conversion and 2^n −2 clock pulses for the second conversion. The tracking converter on the other hand, will require 2^n −1 clock pulses for the first conversion but only one clock pulse for the second conversion. This is illustrated in figure 14.

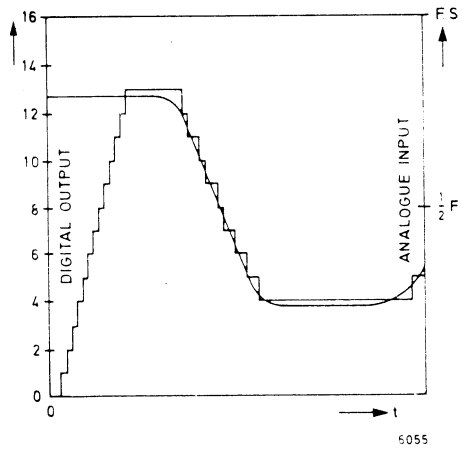


Fig. 13. Operation of Tracking ADC

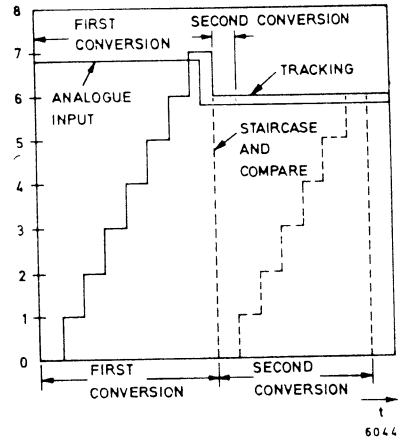


Fig. 14. Comparison of ramp and compare and tracking ADCs

In general it can be said that a tracking converter will follow signals whose rate of change is less than ± 1 LSB $\times$ clock frequency. If this condition is met there is no need to use a sample-and-hold circuit on the analogue input.

A tracking technique is used in the ZN433 series of converters.

2.2.4 Successive Approximation Converters

The operation of a staircase and compare ADC is analogous to weighing, say an 11 gramme weight, on a balance by adding one gramme weights until the scale tips, which is clearly a very slow method. A faster procedure, known as successive approximation, uses weights of 16, 8, 4, 2 and 1 grammes. The 16 gramme weight is tried first and is discarded because it tips the scale. The 8 gramme weight is tried next, and is left on the pan. Next the 4 gramme weight is tried and discarded, and the 2 and 1 gramme weights are tried and retained. The final result is the sum of the weights remaining on the scale pan, and the operation has taken 5 'cycles' as opposed to 11 'cycles' for the staircase and compare method.

The principle of a successive approximation ADC is identical. The MSB of a DAC is first set to '1' and the output is compared to the analogue input. If it is greater than the input the MSB is reset to '0', otherwise it is left at '1'. The next bit is then set to '1' and the DAC output is again compared to the analogue input. Again it is either reset or left at '1' depending on the result of the comparison. This procedure is repeated for every bit down to the LSB, and the final input code to the DAC is the output code of the ADC. A successive approximation cycle is illustrated in figure 15.

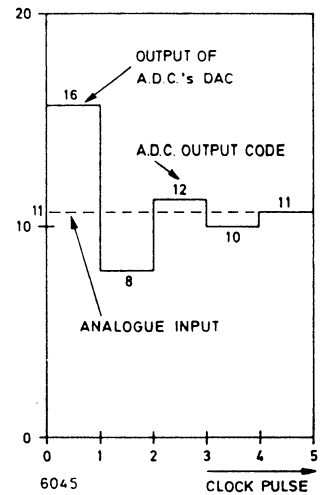


Fig. 15. Operation of a Successive Approximation ADC

Successive approximation is used in the ZN427 and ZN432 series of converters.

2.2.5 Dual Slope Converters

Dual slope integration is one of the slowest methods of A to D conversion, but it offers high resolution at a modest cost.

A block diagram of a dual-slope converter is shown in figure 16. It operates in the following manner: Switch S1 is closed by the control logic, S4 is opened and the input voltage is integrated for n clock periods, where n is usually the maximum count of the counter. At the end of this time the integrator output voltage, V_O, is $\frac{-V_{in}\, n\, T_c}{RC}$ where T_c is the clock period. This is shown in figure 17.

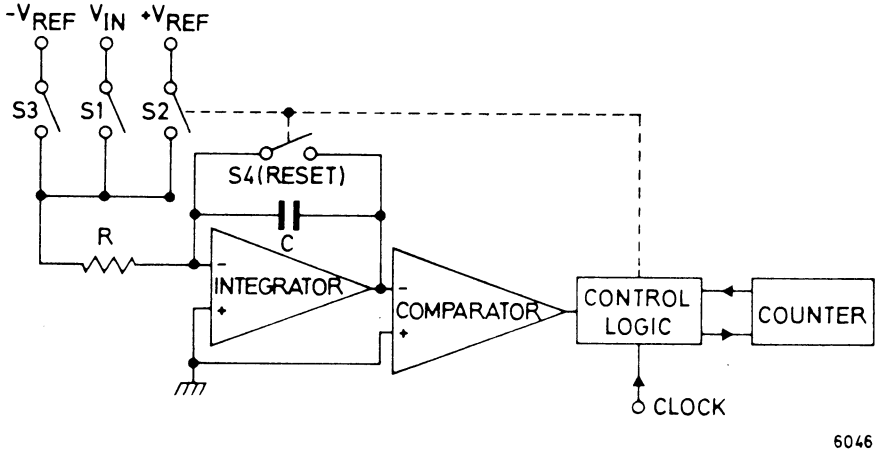


Fig. 16. Dual-Slope ADC

During this period the polarity of the input signal is detected by the comparator. At the end of the integration period S1 is opened and, depending on the polarity of V_{in}, either S2 or S3 is closed to connect the integrator to a reference voltage of opposite polarity to V_{in}. The counter is now allowed to count from zero until the integrator output reaches 0 volts, when the comparator output changes state and the counter is stopped. Since the integration is over the same voltage range (V_O), $V_O = \frac{-V_{REF} \times T_c}{RC}$, where x is the count

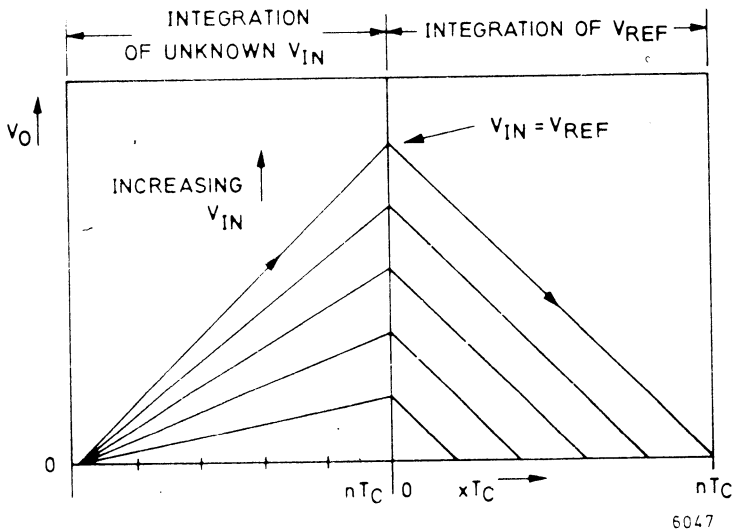


Fig. 17. Operation of Dual-Slope ADC

reached by the time the integrator output crosses zero. Thus

$$\frac{V_{in}.n\,T_c}{RC} = \frac{V_{REF}\,x\,T_c}{RC}$$

$$\text{or } x = \frac{V_{in}.n}{V_{REF}}$$

Since n and V_{REF} are both fixed the output count is proportional to the input voltage. Since both the first and second integrations occur under identical conditions the converter is unaffected by any long-term variations in T_c, R or C, as demonstrated by the disappearance of these terms from the final equation. The only factors affecting the accuracy of the converter are (1) the stability of V_{REF} (2) the stability of the 'on' resistance of S1 to S3 and (3) drift in the integrator and comparator op-amps. These effects can be minimised by careful design.

Dual slope converters are generally used where high resolution and low cost are more important than speed, for example in digital voltmeters.

The ZNA116 and ZNA216 are DVM logic subsystems containing the clock, counter and all control logic necessary for dual slope converter or DVM.

2.3 A to D Parameters and Definitions

2.3.1 A to D Converter Errors

Like DACs, practical ADCs are subject to a number of error sources, and since most ADCs contain a reference DAC, many of these error sources are the same for both types of converter.

2.3.2 Quantising Error (Uncertainty)

Quantising error is an ADC specification that has no counterpart in DAC specifications. For each input code of a DAC there is a unique analogue output level, but for any ADC output code there is a 1 LSB range of analogue input levels. It is thus not possible to tell from the output code the precise value of the analogue input level, there being a quantising error or uncertainty of $\pm\frac{1}{2}$ LSB. Since all ADCs have this inherent quantising error the parameter is frequently not quoted in specifications.

2.3.3 Missing Codes

Missing codes are perhaps best explained by considering the operation of a staircase and compare type 3-bit ADC which has a non-monotonic DAC, as shown in figure 18. The reference DAC exhibits non-monotonicity at input code 4, i.e. step 4 of the staircase decreases. There is thus no way in which the counter can be stopped at this code. If the analogue input is less than the DAC output for code 3 then the comparator will stop the counter before 4 is reached. If the analogue input is greater than output 3 it must also be greater than output 4, so the comparator will not change state at code 4.

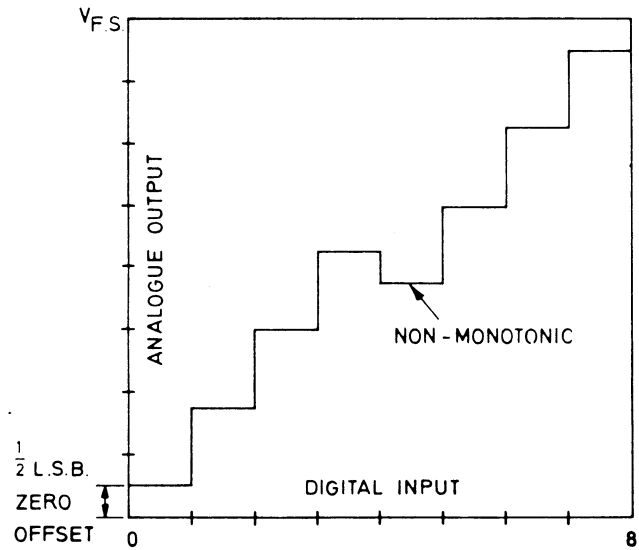


Fig. 18. Non-monotonic DAC used in an ADC

Output code 4 will thus never appear and is known as a 'missing' code. The transfer function of an ADC with a missing code is shown in figure 19.

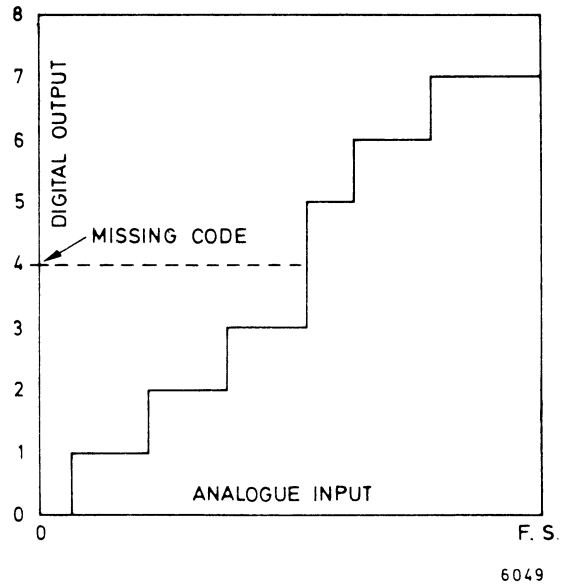


Fig. 19. ADC With Missing Code

2.3.4 Zero Transition

As explained earlier, the zero of an ADC is usually trimmed so that the output transition from 0 to 1 occurs at an input level corresponding to $\frac{1}{2}$ LSB, i.e. $\frac{1}{2}\frac{V_{FS}}{2^n}$. However, as supplied the reference DAC of an ADC I.C. will not have the $\frac{1}{2}$ LSB offset necessary to achieve this. The zero transition will thus occur at 1 LSB plus the DAC zero error, plus the comparator offset voltage. These three parameters are frequently lumped together as the (untrimmed) zero transition of the ADC.

2.3.5 Gain Error

This is the difference between the slope of a line drawn between the actual zero and full scale transition points and that of a line drawn through the ideal transition points.

2.3.6 Non-linearity (Linearity Error)

Non-linearity is the maximum amount by which any actual transition points deviates from the corresponding ideal transition point. It is specified as a percentage of full-scale or a fraction of an LSB. A linearity error of less than $\pm\frac{1}{2}$ LSB assures no missing codes.

2.3.7 Differential Non-linearity

This is the maximum difference between any 1 LSB increment of the analogue input and the ideal size of an LSB increment $\frac{V_{FS}}{2^n}$. Differential non-linearity of less than 1 LSB guarantees no missing codes.

2.3.8 Resolution

The resolution of an ADC is simply the number of bit outputs that the converter possesses. As with a DAC, resolution implies nothing about the accuracy of a device.

2.3.9 Useful Resolution

Useful resolution is the resolution (number of bits) at which an ADC has no missing codes, which for Ferranti ADCs is guaranteed over the operating temperature range. As with DACs, an n-bit ADC may have a useful resolution less than n bits, for reasons previously explained.

2.3.10 Conversion Time

The time taken for an ADC to perform a complete conversion is known as the conversion time. For successive approximation converters conversion time is fixed by the number of bits and the clock frequency. However, for other types, conversion time may vary with input voltage. For example, a ramp and compare ADC requires $2^n - 1$ clock pulses for a full scale conversion but only one clock pulse for a one bit conversion. It is thus important to check exactly what is being specified.

2.4 Bipolar Operation

As with a DAC, an ADC may be used for bipolar operation. Taking the ZN427 as an example the input is offset by $\frac{+V_{REF}}{2}$ so that the input voltage presented to the ADC is always positive, even with negative input voltages down to $\frac{-V_{REF}}{2}$. The principle of offsetting an ADC input is illustrated in figure 20, whilst the transfer function of a 3 bit bipolar ADC is shown in figure 21. In this case the **output** coding is known as offset binary.

A to D Converters

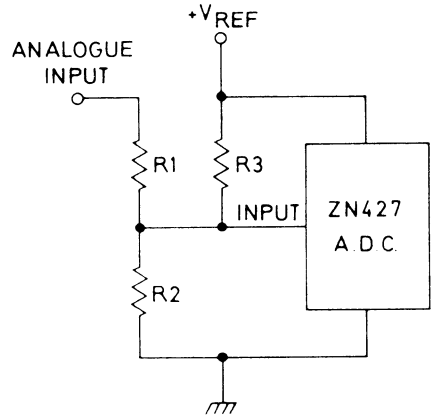


Fig. 20. Bipolar Operation of an ADC

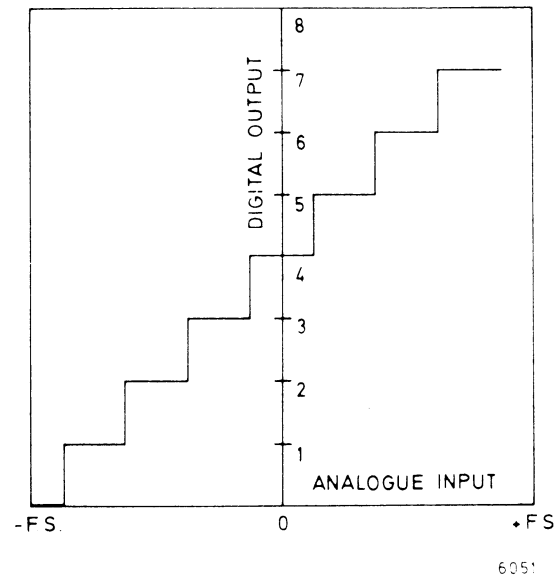


Fig. 21. Bipolar Transfer Characteristic of an ADC

FERRANTI semiconductors

ZN427E-8
ZN427J-8

8 Bit A/D-Converter, μP-compatible

FEATURES

- Easy interfacing to microprocessors, or operates as a 'stand-alone' converter
- Fast: 10 μs conversion time guaranteed
- No missing codes over operating temperature range
- Data outputs 3-state TTL compatible, other logic inputs and outputs TTL and CMOS compatible
- Choice of on-chip or external voltage reference
- Ratiometric operation
- Unipolar and bipolar input ranges
- Complementary to ZN428 DAC
- Choice of commercial or military temperature range

DESCRIPTION

The ZN427 is an 8-bit successive approximation converter with 3-state outputs to permit easy interfacing to a common data bus. The IC contains a voltage switching DAC, a fast comparator, successive approximation logic and a 2.56 volt precision band-gap reference, the use of which is pin-optional to retain flexibility. An external fixed or varying reference may therefore be substituted, thus allowing ratiometric operation.

Only passive external components are required for operation of the converter.

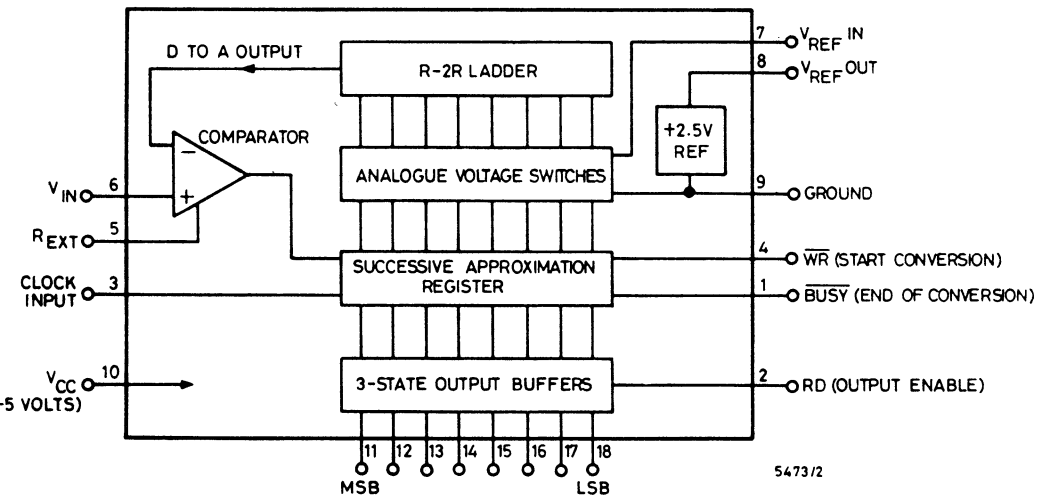


Fig. 1 – System Diagram

ZN427E-8/J-8

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .. .. +7.0 volts
Max. Voltage, Logic and V_{REF} inputs .. .. V_{CC}
Operating temperature range .. .. 0°C to +70°C (ZN427E-8)
–55°C to +125°C (ZN427J-8)
Storage temperature range .. .. –55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units	Conditions
CONVERTER					
Resolution	8	—	—	Bits	
Linearity Error	—	—	±0.5	LSB	
Differential Non-Linearity	—	±0.5	—	LSB	
Linearity Error T.C.	—	±3	—	ppm/°C	
Differential Non-Linearity T.C.	—	±6	—	ppm/°C	
Full Scale (Gain) T.C.	—	±2.5	—	ppm/°C	External Ref. 2.5V
Zero T.C.	—	±8	—	µV/°C	
Zero Transition 00000000 to 00000001	12	15	18	mV	$V_{REF\ IN}$ = 2.560V
F.S. Transition 11111110 to 11111111	2.545	2.550	2.555	V	$V_{REF\ IN}$ = 2.560V
Conversion Time	—	—	10	µs	See Note 1
External Reference Voltage	1.5	—	3.0	V	
Supply Voltage (V_{CC})	4.5	—	5.5	V	
Supply Current	—	25	40	mA	
Power Consumption	—	125	—	mW	
COMPARATOR					
Input Current	—	1	—	µA	V_{IN} = 3V, R_{EXT} = 82kΩ
Input Resistance	—	100	—	kΩ	V_- = –5V
Tail Current, I_{EXT}	25	—	150	µA	
Negative Supply, V–	–3.0	—	–30.0	V	See COMPARATOR
Input Voltage	–0.5	—	3.5	V	
INTERNAL VOLTAGE REFERENCE					
Output Voltage	2.475	2.560	2.625	V	R_{REF} = 390Ω C_{REF} = 4 µ7
Slope Resistance	—	0.5	2	Ω	
V_{REF} Temperature Coefficient	—	50	—	ppm/°C	
Reference Current	4	—	15	mA	See REFERENCE

ELECTRICAL CHARACTERISTICS (continued)

	Min.	Typ.	Max.	Units	Conditions
LOGIC					
(over operating temp.)					
High Level Input Voltage V_{IH}	2	—	—	V	
Low Level Input Voltage V_{IL}	—	—	0.8	V	
High Level Input Current,	—	—	50	μA	V_{IN} = 5.5V, V_{CC} = max.
$\overline{WR}$ and RD inputs I_{IH}	—	—	15	μA	V_{IN} = 2.4V, V_{CC} = max.
High Level Input Current,	—	—	100	μA	V_{IN} = 5.5V, V_{CC} = max.
Clock Input I_{IH}	—	—	30	μA	V_{IN} = 2.4V, V_{CC} = max.
Low Level Input Current I_{IL}	—	—	–5	μA	V_{IN} = 0.4V, V_{CC} = max.
High Level Output Current I_{OL}	—	—	–100	μA	
Low Level Output Current I_{OL}	—	—	1.6	mA	
High Level Output Voltage V_{OH}	2.4	—	—	V	I_{OH} = max., V_{CC} = min.
Low Level Output Voltage V_{OL}	—	—	0.4	V	I_{OL} = max., V_{CC} = min.
Disabled Output Leakage	—	—	2	μA	V_O = 2.4V
Input Clamp Diode Voltage	—	—	–1.5	V	
Read Input to Data Output	—	—	250	ns	See Fig. 8
Enable/Disable Delay Time t_{RD}	—	180	250	ns	
Start Pulse Width t_{WR}	250	160	—	ns	See Fig. 8
$\overline{WR}$ to $\overline{BUSY}$ Propagation	—	—	250	ns	
Delay t_{BD}	—	—	—		
Clock Pulse Width	500	—	—	ns	
Maximum Clock Frequency	900	1000	—	kHz	See Note 1

Note 1 : A 900 kHz clock gives a conversion time of 10μs (9 clock periods).

GENERAL CIRCUIT OPERATION

The ZN427 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{WR}$ input the $\overline{BUSY}$ output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF}/2$ from the DAC. This is compared to the input voltage V_{IN}; a decision is made on the next negative clock edge to reset the MSB to 0 if $\frac{V_{REF}}{2} > V_{IN}$ or leave it set to 1 if $\frac{V_{REF}}{2} < V_{IN}$. Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2} + \frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to V_{IN} and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the ninth negative clock edge $\overline{BUSY}$ goes high indicating that the conversion is complete.

During a conversion the RD input will normally be held low to keep the 3-state buffers in their high impedance state. Data can be read out by taking RD high, thus enabling the 3-state outputs. Readout is non-destructive. The $\overline{BUSY}$ output may be tied to the RD input to automatically enable the outputs when the data is valid.

For reliable operation of the converter the start pulse applied to the $\overline{WR}$ input must meet certain timing criteria with respect to the converter clock. These are detailed in the timing diagram of figure 2.

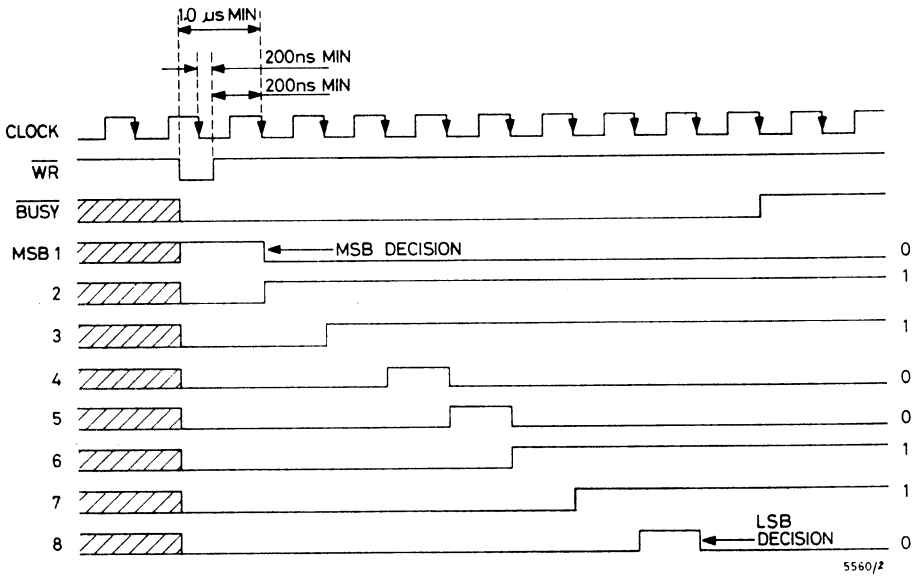


Fig. 2 Timing Diagram

NOTES ON TIMING DIAGRAM

1. A conversion sequence is shown for the digital word 01100110. For clarity the 3-state outputs are shown as being enabled during the conversion, but normal practice would be to disable them until the conversion was complete.

2. The $\overline{BUSY}$ output goes low during a conversion. When $\overline{BUSY}$ goes high at the end of a conversion the output data is valid. In a microprocessor system the $\overline{BUSY}$ output can be used to generate an interrupt request when the conversion is complete.

3. In the timing diagram cross hatching indicates a 'don't care' condition.

4. The start pulse operates as an asynchronous (independent of clock) reset that sets the MSB output to 1 and sets all other outputs and the end of conversion flag to 0. This resetting occurs on the low-going edge of the start pulse and as long as $\overline{WR}$ is low the converter is inhibited. Conversion commences on the first active (negative going) clock edge after the $\overline{WR}$ input has gone high again, when the MSB decision is made. A number of timing constraints thus apply to the start pulse.

(a) The minimum duration of the start pulse is 250ns, to allow reliable resetting of the converter logic circuits.

(b) There is no limit to the maximum duration of the start pulse.

(c) To allow the MSB to settle at least 1.5μs must elapse between the negative going edge of the start pulse and the first active clock edge that initiates the MSB desicion.

(d) To ensure reliable clocking the positive-going edge of the start pulse should not occur within 200 ns of an active (negative-going) clock edge. The ideal place for the positive-going edge of the start pulse is coincident with a positive-going clock edge. As a special case of the above conditions the start pulse may be synchronous with a negative-going clock pulse.

PRACTICAL CLOCK AND SYNCHRONISING CIRCUITS

The actual method of generating the clock signal and synchronising it to the start conversion pulse (or vice versa) will depend on the system in which the ZN427 is incorporated.

When used with a microprocessor the ZN427 can be treated as RAM and can be assigned a memory address using an address decoder. If the μP clock is used to drive the ZN427 and the μP write pulse meets the ZN427 timing criteria with respect to the μP clock then generating the start pulse is simply a matter of gating the decoded address with the microprocessor write pulse. Whilst the conversion is being performed the microprocessor can perform other instructions or No operation (NOP). When the conversion is complete the outputs can be enabled onto the data bus by gating the decoded address with the read pulse. A timing diagram for this sequence of operations is given in figure 3.

An advantage of using the microprocessor clock is that the conversion time is known precisely in terms of machine cycles. The data outputs may therefore be read after a fixed delay of at least nine clock cycles after the end of the $\overline{WR}$ pulse, when the conversion will be complete.

Alternatively the read operation may be initiated by using the $\overline{BUSY}$ output to generate an interrupt request.

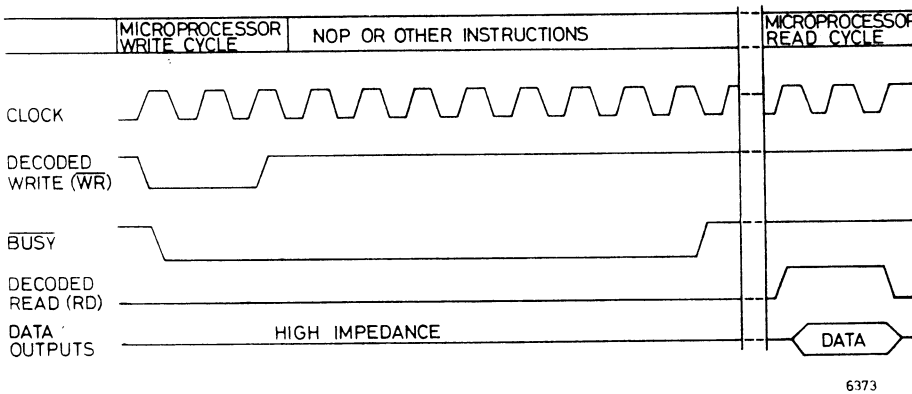


Fig. 3 Typical Timing Diagram Using μP clock and Write Pulse

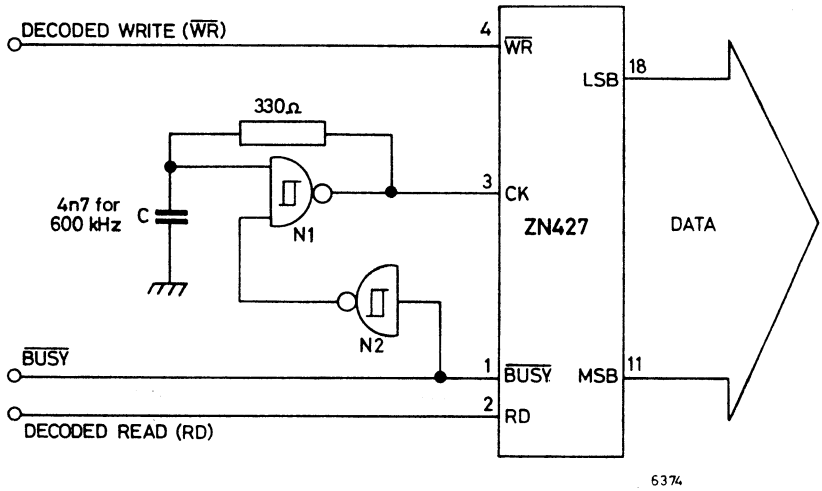
In some systems, for example single-chip microcomputers such as the 8048, this simple method may not be feasible for one or more of the following reasons:

(a) The MPU clock is not available externally.

(b) The clock frequency is too high.

(c) The write pulse timing criteria make it unsuitable for direct use as a start conversion pulse.

If any of these conditions apply then the self-synchronising clock circuit of figure 4a is recommended.



N1 N2 = ZN7413 or ½ 74132 Schmitt Trigger

$$f_{CK} = \frac{1}{360.C} \text{ (Hz, F)}$$

Fig. 4a. Self-Synchronising Clock Circuit

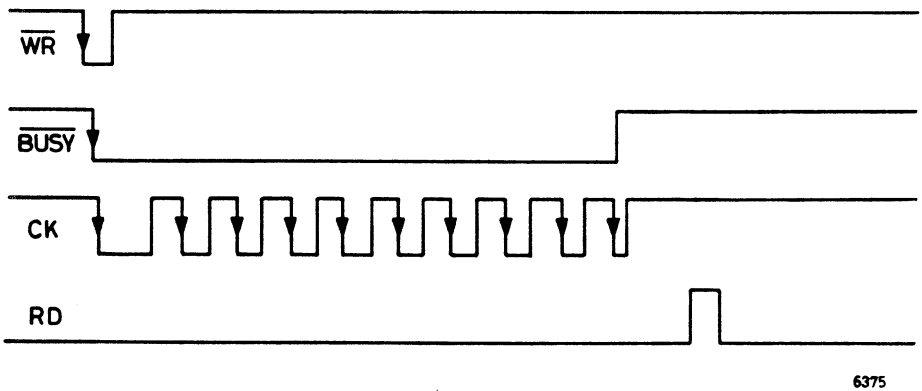


Fig 4b. Timing Diagram For Circuit of Figure 4a.

N1 is connected as an astable multivibrator which, when the $\overline{BUSY}$ output is high, is inhibited by the output of N2 holding one of its inputs low. The start conversion pulse resets the $\overline{BUSY}$ flag and N1 begins to oscillate. When the conversion is completed $\overline{BUSY}$ goes high and the clock is inhibited.

Since the start pulse starts the clock it may occur at any time. The only constraints on the start pulse are that it must be longer than 250 ns but at least 200 ns shorter than the first clock pulse. The first clock pulse is in fact longer than the rest since C1 starts from a fully charged condition whereas on subsequent cycles it charges between the upper and lower thresholds (V_{T+} and V_{T-}) of the Schmitt trigger.

LOGIC INPUTS AND OUTPUTS

The logic inputs of the ZN427 utilise the emitter-follower configuration shown in fig. 5. This gives extremely low input currents for CMOS as well as TTL compatibility.

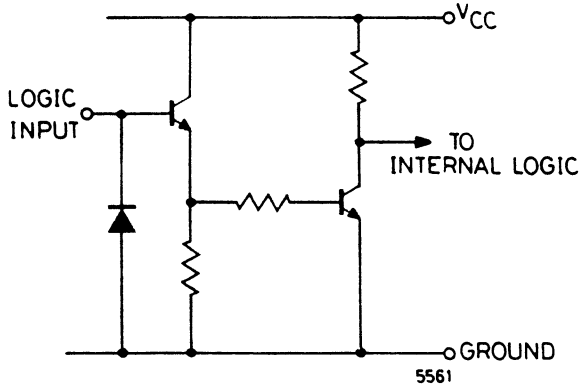
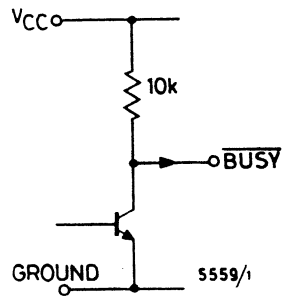


Fig. 5. Equivalent Circuit of all Inputs

The $\overline{BUSY}$ output, shown in figure 6, utilises a passive pullup for CMOS/TTL compatibility



The data outputs have 3-state buffers, an equivalent circuit of which is shown in figure 7. Whilst the RD input is low both output transistors are turned off and the output is in a high impedance state. When RD is high the data output will assume the appropriate logic state (0 or 1).

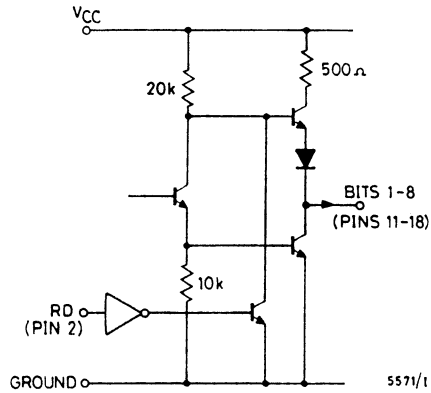


Fig. 7. Equivalent Circuit of Data Outputs

A test circuit and timing diagram for the output enable/disable delays are given in figure 8.

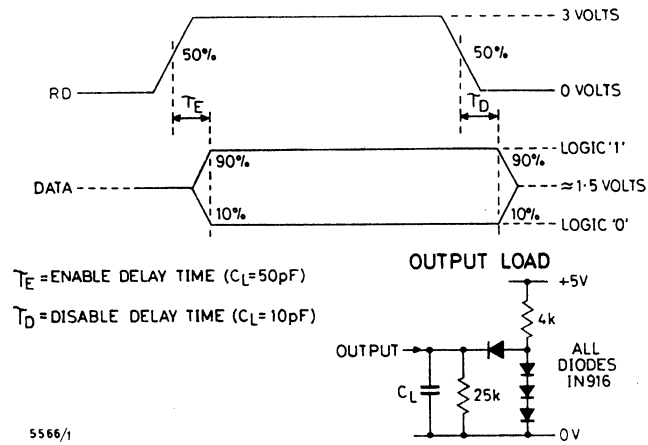


Fig. 8. Output Enable/Disable Waveforms

ANALOGUE CIRCUITS

D to A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in figure 9. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (<1 millivolt).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$\text{D to A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D to A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of V_{OS} is typically 2 mV for the ZN427E-8 (4 mV, ZN427J-8). This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (8 μV/°C) the effect on accuracy will be negligible.

The D to A output range can be considered to be 0-$V_{REF\ IN}$ through an output resistance R (4kΩ)

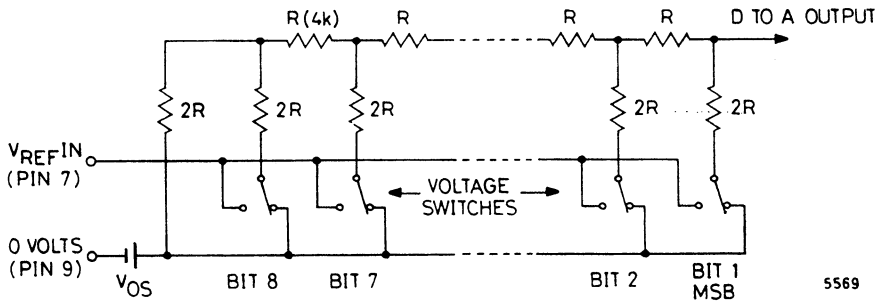


Fig. 9. R2-R Ladder Network

REFERENCE

(a) Internal Reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 10). A resistor (R_{REF}) should be connected between pins 8 and 10. The recommended value of 390Ω will supply a nominal reference current of (5.0 -2.5) /0.39 = 6.4mA. A stabilising/decoupling capacitor, C_{REF} (4μ7), is required between pins 8 and 9. For internal reference operation $V_{REF\ OUT}$ (Pin 8) is connected to $V_{REF\ IN}$ (Pin 7).

Up to five ZN427's may be driven from one internal reference, there being no need to reduce R_{REF}. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 3mA.

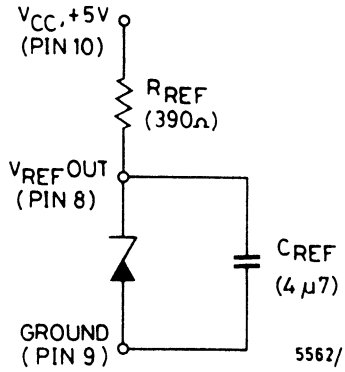


Fig. 10 Internal Voltage Reference

(b) External Reference

If required an external reference voltage in the range +1.5 to +3.0 volts may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN427 should be derived from the same supply. The external reference can vary from +1.5 volts to +3.0 volts. The ZN427 will operate if $V_{REF\ IN}$ is less than +1.5 volts but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

COMPARATOR

The ZN427 contains a fast comparator, the equivalent input circuit of which is shown in Fig. 11.

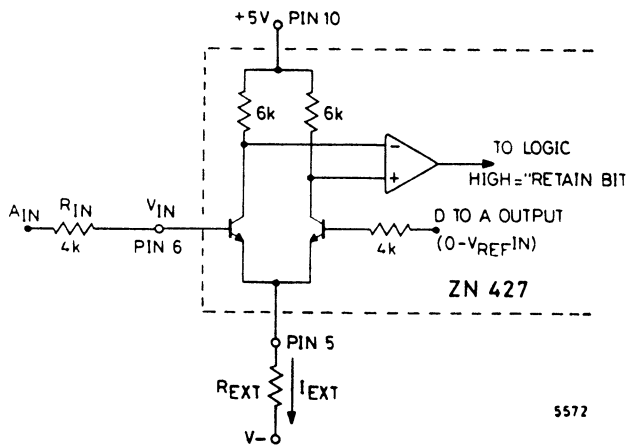


Fig. 11 Comparator Equivalent Circuit

The comparator derives the tail current, I_{EXT}, for its first stage from an external resistor, R_{EXT}, which is taken to a negative supply V–.

This arrangement allows the ZN427 to work with any negative supply in the range –3 to –30 volts. The ZN427 is designed to be insensitive to changes in I_{EXT} from 25μA to 150μA. The suggested nominal value of I_{EXT} is 65μA and a suitable value for R_{EXT} is given by $R_{EXT} = |V-|15k\Omega$.

V– (Volts)	R_{EXT} (±10%)
–3	47kΩ
–5	82kΩ
–10	150kΩ
–12	180kΩ
–15	220kΩ
–20	330kΩ
–25	390kΩ
–30	470kΩ

The output from the D to A converter is connected through the 4kΩ ladder resistance to one side of the comparator. The analogue input to be converted could be connected directly to the other comparator input (V_{IN}, Pin 6) but for optimum stability with temperature the analogue input should be applied through a source resistance ($R_{IN} = 4k\Omega$) to match the ladder resistance.

ANALOGUE INPUT RANGES

The basic connection of the ZN427 shown in fig. 12 has an analogue input range 0 to $V_{REF\,IN}$, which, in some applications, may be made available from previous signal conditioning/scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by offsetting the analogue input range so that the comparator always sees a positive input voltage.

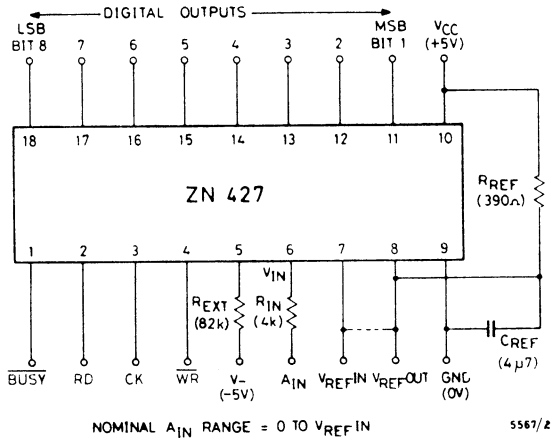


Fig. 12. External Components for Basic Operation

UNIPOLAR OPERATION

The general connection for unipolar operation is shown in figure 13.

The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the Analogue Input(A_{IN}) is at full scale. The resulting full scale range is given by:

$$A_{IN}\ FS = (1+\frac{R1}{R2}),\ V_{REF\ IN} = G.\ V_{REF\ IN}.$$

To match the ladder resistance R1//R2 ($\approx R_{IN}$) = 4kΩ.

The required nominal values of R_1 and R_2 are given by $R_1 = 4G$ kΩ, $R_2 = \frac{4G}{G-1}$ kΩ.

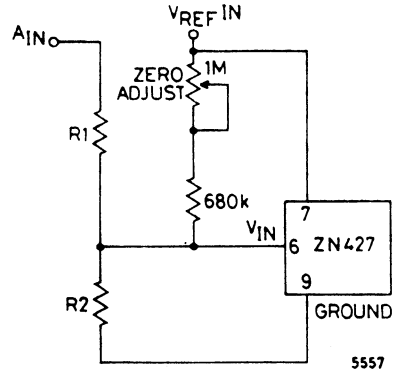


Fig. 13 Unipolar Operation - General Connection

Using these relationhips a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5 volts.

Input Range	G	R_1	R_2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

GAIN ADJUSTMENT

Due to tolerances in R_1 and R_2, tolerances in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least ±5% of its nominal value is suggested.

ZERO ADJUSTMENTS

Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 15mV applied to the comparator input, which corresponds to +1½ LSB with a 2.56 volt reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of $+\frac{1}{2}$ LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than $1\frac{1}{2}$ times $V_{REF\,IN}$.

Practical circuit values for +5V and +10V input ranges are given in fig. 14, which incorporate both zero and gain adjustments.

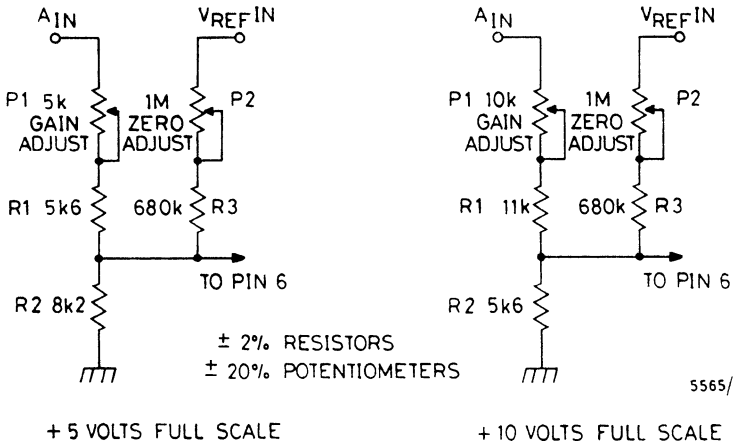


Fig. 14. Unipolar Operation - Component Values

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply full scale minus $1\frac{1}{2}$ LSB to A_{IN} and adjust gain until Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 1.

(iii) Apply $\frac{1}{2}$ LSB to A_{IN} and adjust zero until Bit 8 just flickers between 0 and 1 with all other bits at 0.

UNIPOLAR SETTING-UP POINTS

Input Range, +FS	$\frac{1}{2}$ LSB	FS $-1\frac{1}{2}$ LSB
+5V	9.8 mV	4.9707 volts
+10V	19.5 mV	9.9414 volts

$$1\ \text{LSB} = \frac{FS}{256}$$

UNIPOLAR LOGIC CODING

Analogue Input (A_{IN}) (Nominal code centre value)	Output Code (Binary)
FS –1 LSB	11111111
FS –2 LSB	11111110
$\frac{3}{4}$ FS	11000000
$\frac{1}{2}$ FS + 1 LSB	10000001
$\frac{1}{2}$ FS	10000000
$\frac{1}{2}$ FS – 1 LSB	01111111
$\frac{1}{4}$ FS	01000000
1 LSB	00000001
0	00000000

BIPOLAR OPERATION

For bipolar operation the input to the ZN427 is offset by half full scale by connecting a resistor R_3 between $V_{REF\ IN}$ and V_{IN} (Fig. 15).

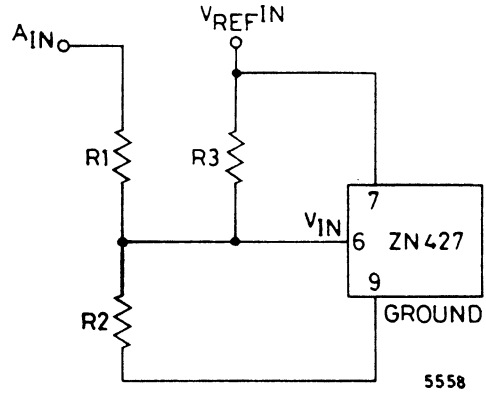


Fig. 15. Bipolar Operation - General Connection

When $A_{IN} = -FS$, V_{IN} needs to be equal to zero.

When $A_{IN} = +FS$, V_{IN} needs to be equal to $V_{REF\ IN}$.

If the full scale range is $\pm G$. $V_{REF\ IN}$ then $R_1 = (G - 1)$. R_2 and $R_1 = G$. R_3 fulfil the required conditions.

To match the ladder resistance $R_1/R_2/R_3$ $(=R_{IN}) = 4k\Omega$.

Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 8\ Gk\Omega$, $R_2 = 8G/(G - 1)k\Omega$, $R_3 = 8k\Omega$.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $+V_{REF\ IN}$) results if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5$ volts the nominal values of resistors for $\pm 5V$ and $\pm 10V$ input ranges are given in the following table.

Input Range	G	R_1	R_2	R_3
±5V	2	16 kΩ	16 kΩ	8 kΩ
±10V	4	32 kΩ	10.66 kΩ	8 kΩ

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.

Practical circuit realisations are given in Fig. 16.

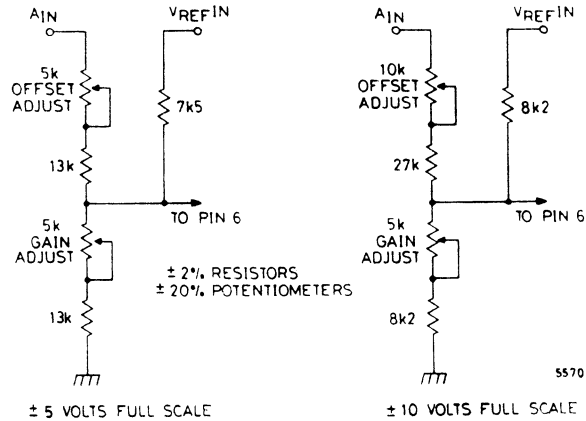


Fig. 16 Bipolar Operation - Component Values

Note that in the ±5V case R_3 has been chosen as 7.5 kΩ (instead of 8.2 kΩ) to obtain a more symmetrical range of adjustment using standard potentometers.

BIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply −(FS - ½ LSB) to A_{IN} and adjust offset until the Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply +(FS - 1½ LSB) to A_{IN} and adjust gain until Bit 8 just flickers between 0 and 1 with all other bits at 1.

(iv) Repeat step (ii).

BIPOLAR SETTING-UP POINTS

Input Range, ±FS	−(FS −½ LSB)	+(FS −1½ LSB)
±5V	−4.9805V	+4.9414V
±10V	−9.9609V	+9.8828V

$$1\ \text{LSB} = \frac{2FS}{256}$$

ZN427E-8/J-8

BIPOLAR LOGIC CODING

Analogue Input (A_{IN}) (Nominal code centre value)	Output Code (Offset Binary)
+(FS – 1 LSB)	11111111
+(FS – 2 LSB)	11111110
+½ FS	11000000
+1 LSB	10000001
0	10000000
–1 LSB	01111111
–½ FS	01000000
–(FS – 1 LSB)	00000001
–FS	00000000

SINGLE 5 VOLT SUPPLY RAIL OPERATION

The ZN427 takes very little power from the negative rail and so a suitable negative supply can be generated very easily using a 'diode pump' circuit. The circuit shown in Fig. 17 works with any clock frequency from 10 kHz to 1 MHz and can supply up to five ZN427s.

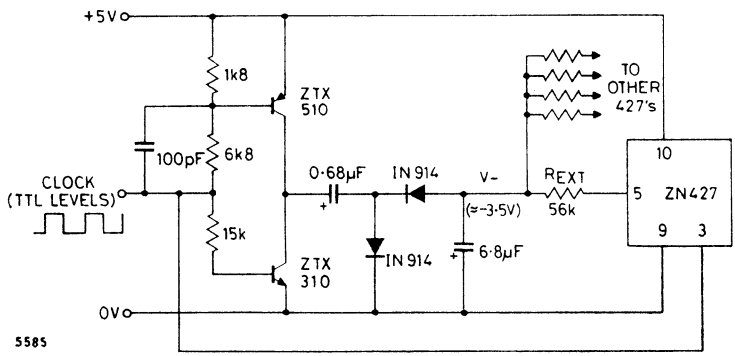
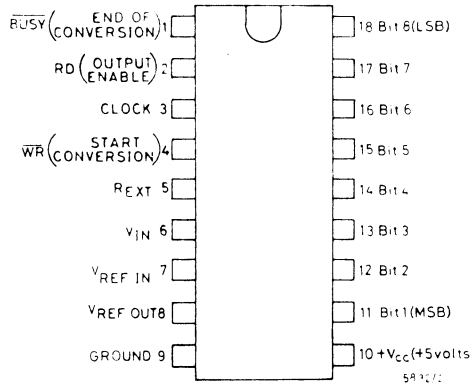
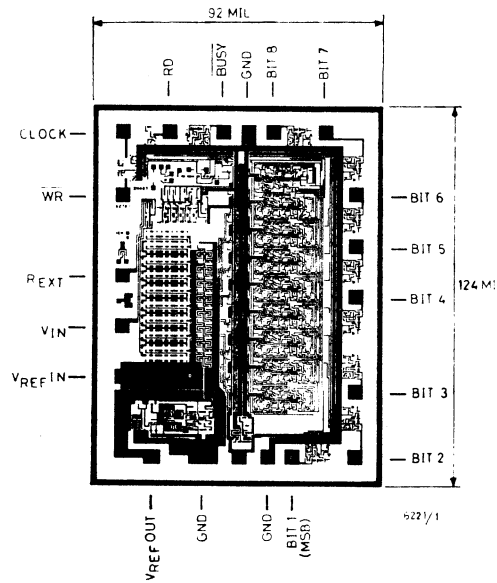


Fig. 17. Single 5 Volt Supply Operation

Pin Connections





Chip Dimensions and Layout

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	OPERATING TEMP. RANGE
ZN427E-8	Plastic	0°C to +70°C
ZN427J-8	Ceramic	−55°C to +125°C

FERRANTI semiconductors

ZN432 Series

10-Bit Successive Approximation Monolithic A/D Converter

FEATURES

- 10, 9 and 8-Bit Accuracies
- 3 Operating Temperature Ranges
- 20 μs Conversion Time Guaranteed
- Input Range as Desired
- ±5V Supplies, TTL/CMOS Compatible
- Parallel and Serial Outputs
- Bipolar Monolithic Construction

DESCRIPTION

The ZN432 range of successive approximation analogue to digital converters combine several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), successive approximation logic with TTL interfacing, 2.5V precision voltage reference with reference amplifier, and fast comparator with good overload recovery. The overall accuracy of the A-D system is sufficient to provide guaranteed monotonicity over the operating temperature range.

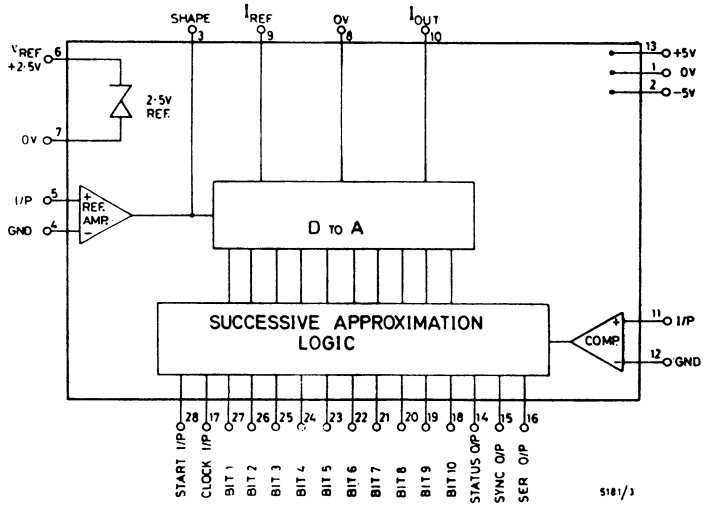


Fig. 1 – INTEGRATED CIRCUIT BLOCK DIAGRAM

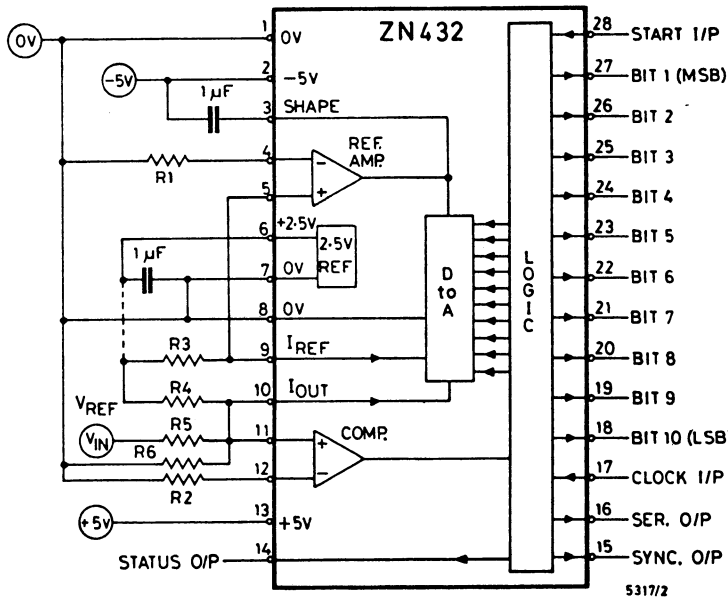


Fig. 2—TYPICAL EXTERNAL COMPONENTS

ORDERING INFORMATION

Operating Temperature	10-bit accuracy	9-bit accuracy	8-bit accuracy	Package
–55 to +125°C	ZN432J-10	ZN432J-9	ZN432J-8	Ceramic
–40 to +85°C	ZN432BJ-10	ZN432BJ-9	ZN432BJ-8	Ceramic
0 to +70°C	ZN432CJ-10	ZN432CJ-9	ZN432CJ-8	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply Voltages .. .. ±7 volts
Logic Input Voltage .. .. .. $+V_{CC}$ and 0V
Storage Temperature Range .. −55°C to +125°C

CHARACTERISTICS (at ±5V supplies and internal reference unless otherwise specified).

Parameter	Version	t_{amb} = +25°C			Over Spec. Temp. Range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
CONVERTER								
Accuracy (useful resolution)	ZN432J-10, ZN432BJ-10, ZN432CJ-10	10			10		Bits	Note 1
	ZN432J-9, ZN432BJ-9, ZN432CJ-9	9			9		Bits	
	ZN432J-8, ZN432BJ-8, ZN432CJ-8	8			8		Bits	
Non-linearity	All types			±0.5			LSB	
Differential non-linearity	All types		±0.5				LSB	Note 1
Operating temp. range	ZN432J-10, ZN432J-9, ZN432J-8				−55	+125	°C	
	ZN432BJ-10, ZN432BJ-9, ZN432BJ-8				−40	+85	°C	
	ZN432CJ-10, ZN432CJ-9, ZN432CJ-8				0	+70	°C	
D to A reference current, I_{REF} (pin 9)	All types	0.25		1.0	0.25	1.0	mA	Note 6
Conversion time	All types		15	20		20	µs	Note 2
Nominal analogue input range	All types	−2.5		+2.5			V	Note 3
Supply rejection	All types		0.1				% per V	
Gain error	All types		±0.05				%	Note 4

CHARACTERISTICS (*continued*)

Parameter	Version	t_{amb} = +25°C			Over Spec. Temp. Range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
Gain temperature coefficient (Note 4)	ZN432J-10 ZN432BJ-10 ZN432CJ-10		10				ppm/°C	
	ZN432J-9 ZN432BJ-9 ZN432CJ-9 ZN432J-8 ZN432BJ-8 ZN432CJ-8		20				ppm/°C	
Zero temperature coefficient	ZN432J-10 ZN432BJ-10 ZN432CJ-10		7				ppm/°C of FSR	
	ZN432J-9 ZN432BJ-9 ZN432CJ-9 ZN432J-8 ZN432BJ-8 ZN432CJ-8		15				ppm/°C of FSR	
Supply voltage	All types	±4.5	±5	±5.5	±4.5	±5.5	V	
Supply current	All types		35				mA	
Power consumption	All types		350				mW	
INTERNAL VOLTAGE REFERENCE Output voltage	All types		2.480				V	
Output voltage tolerance (Note 5)	ZN432J-10 ZN432BJ-10 ZN432CJ-10			±1.5			%	
	ZN432J-9 ZN432BJ-9 ZN432CJ-9			±2.0			%	
	ZN432J-8 ZN432BJ-8 ZN432CJ-8			±5.0			%	
Slope impedance	All types		0.75				Ω	
Maximum Reference load current			±2				mA	

CHARACTERISTICS *(continued)*

Parameter	Version	t_{amb} = +25°C			Over Spec. Temp. Range		Units	Conditions
		Min.	Typ.	Max.	Min.	Max.		
LOGIC	All types							
High level input voltage		2.0			2.0		V	
Low level input voltage				0.8		0.8	V	
High level input current			7				μA	V_S = ±5.5V V_I = 2.4V
			50				μA	V_S = ±5.5V V_I = 5.5V
Low level input current			1				μA	V_S = ±5.5V V_I = 0.4V
High level output voltage		2.4			2.4		V	I_{load} = –40 μA
Low level output voltage				0.4		0.4	V	I_{load} = 1.6 mA

NOTE 1. No missing codes over full temperature range at resolution appropriate to accuracy.

NOTE 2. This corresponds to a maximum clock rate of 550 kHz based on 11 clock periods per conversion cycle (see timing diagram, This provides an update rate of 45 kHz.

NOTE 3. Single polarity and other input ranges may be provided by different input resistor values. (see page 2–41)

NOTE 4. Excluding reference.

NOTE 5. For typical temperature performance see Fig. 6

NOTE 6. The full scale D to A output current I_{OUT} = 4 times I_{REF}. For optimum performance I_{REF} = 0.5 mA.

TEST CIRCUIT

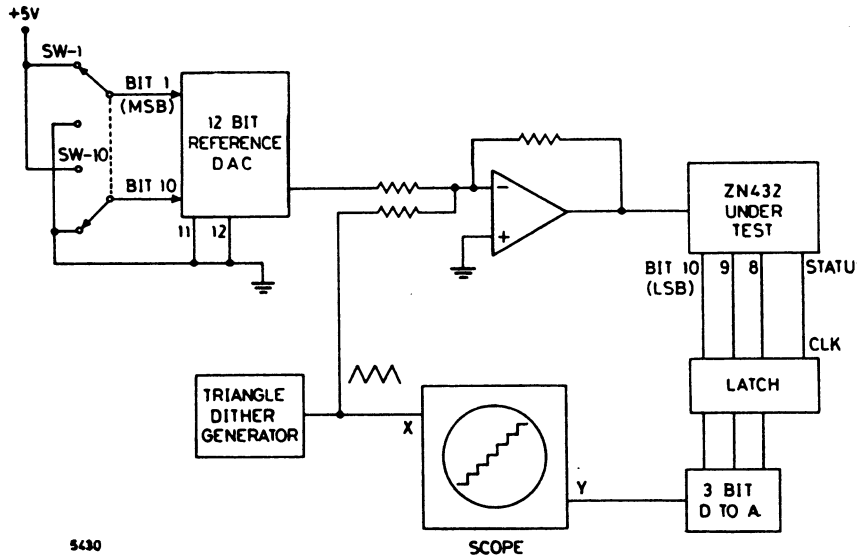


Fig. 3 – DYNAMIC CROSSPLOT ACCURACY TEST

Switches SW-1 to SW-10 are set to the appropriate digital code to select the point on the characteristic to be displayed. For example, code 10000 00000 would select half full scale, i.e. the major transition.

The output from the dither generator (suggested peak to peak amplitude = $\pm 4 \times$ L.S.B.) is used as the X deflection for the scope and is also superimposed on the analogue output from the reference D.A.C. in the summing amplifier. The resulting analogue signal including dither is used as V_{IN} for the ZN432 under test.

Bit 10, 9 and 8 outputs are fed to the inputs of a 3-bit D.A.C. of at least 6-bit accuracy and the analogue output used as the Y deflection for the scope. Differential non-linearity is shown by horizontal lines which are longer or shorter than the rest.

CALCULATION OF EXTERNAL RESISTORS (See Fig. 2)

1. R_3, R_4, R_5 can affect gain and offset stability and thus require to be of high quality.
2. R_1 and R_2 are to allow for the bias current of the reference amplifier and comparator, thus:
   $$R_1 = R_3$$
   And R_2 = parallel combination of R_4, R_5 and R_6.
3. I_{REF} should be 0.5 mA
   Therefore
   $$R_3 = \frac{V_{REF}}{0.5\ mA}$$
   $I_{out\ FS}$ is four times I_{REF}, i.e., 2 mA
4. Analysing the network yields the following:
   $$R_4 = \frac{-V_{REF}\ R_5}{V_{in}\ min}$$
   $$R_5 = \frac{V_{in}\ max - V_{in}\ min}{I_{out\ FS}}$$
   Where V_{in} max is the voltage for the logic output to be all 1's.
   V_{in} min is the voltage for the logic output to be all 0's.
5. R_6 should be chosen such that the parallel combination of R_4, R_5 and R_6 is about 1.25 kΩ as this determines the D to A time constant and hence conversion time.
6. The following is a table of values to give examples of the above equations.

V_{in} max	V_{in} min	V_{REF}	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
+2.5	−2.5	2.5	5 kΩ	1.25 kΩ	5 kΩ	2.5 kΩ	2.5 kΩ	∞
+2.5	−2.5	5*	10 kΩ	1.25 kΩ	10 kΩ	5 kΩ	2.5 kΩ	5 kΩ
+2.5	0	2.5	5 kΩ	1.25 kΩ	5 kΩ	∞	1.25 kΩ	∞
+5	0	2.5	5 kΩ	1.25 kΩ	5 kΩ	∞	2.5 kΩ	2.5 kΩ
+4	−2	2.5	5 kΩ	1.25 kΩ	5 kΩ	3.75 kΩ	3 kΩ	5 kΩ
+4	−2	12*	24 kΩ	1.25 kΩ	24 kΩ	3.75 kΩ	3 kΩ	5 kΩ
+10	−10	2.5	5 kΩ	1.25 kΩ	5 kΩ	2.5 kΩ	10 kΩ	3.33 kΩ

Note 1. Nearest preferred value may be used for R_1, R_2 and R_6
*Note 2. External reference

7. For setting up R_4 will adjust the offset.
   R_3 will adjust the gain.

For unipolar operation where R_4 approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of R_4 (Typical values only).

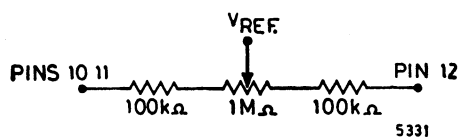


Fig. 4 – OFFSET CIRCUIT WITH UNIPOLAR OPERATION

TIMING DETAILS

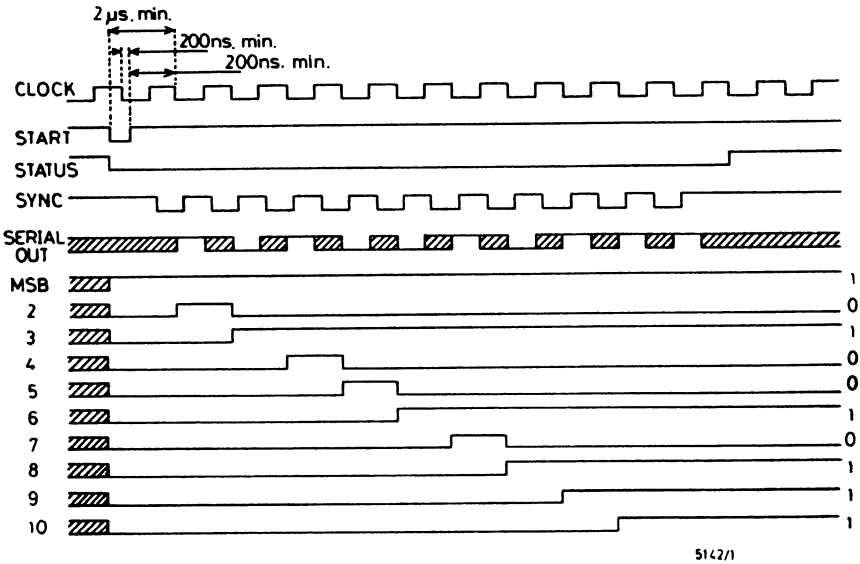


Fig. 5 – TIMING DIAGRAM

NOTES ON TIMING DIAGRAM

1. Conversion is initiated by a 'START' pulse which sets the MSB to 1 and all the other bits to 0.

2. The first active (negative going) edge of Clock after the trailing edge of the 'START' pulse should not occur until at least 2 µs after the leading edge of the 'START' pulse to allow for MSB settling.

3. A negative going edge of Clock must not occur within 200 ns either side of the trailing edge of the 'START' pulse.

4. As a special case of conditions (2) and (3) the 'START' pulse may be coincident with, and of the same duration as, a negative going clock pulse.

5. Serial data is available during conversion at the Serial Output.
   Ten SYNC pulses are provided to facilitate data transmission.
   The serial output data is valid on the positive going edge of the SYNC pulse.

6. Cross hatching indicates a 'don't care' condition or, in the case of serial output, invalid data.

7. The conversion sequence shown is for the digital word 1010010111.

8. The parallel output data is valid when the Status Output goes HIGH.

LOGIC CODING

Table 1. Unipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
FS –1LSB	1111111111
FS –2LSB	1111111110
¾ FS	1100000000
½ FS +1LSB	1000000001
½ FS	1000000000
½ FS –1LSB	0111111111
¼ FS	0100000000
1LSB	0000000001
0	0000000000

Table 2. Bipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
+(FS –1LSB)	1111111111
+(FS –2LSB)	1111111110
+(½ FS)	1100000000
+(1LSB)	1000000001
0	1000000000
–(1LSB)	0111111111
–(½ FS)	0100000000
–(FS–1LSB)	0000000001
–FS	0000000000

NOTES:

1. Analogue inputs shown are nominal centre values of code.
2. "FS" is full scale.

OFFSET AND GAIN SETTING

For unipolar, supply an input of ½ LSB for transition 0000000000 to 0000000001, and of (full scale –1½ LSB) for transition 1111111111 to 1111111110.

For bipolar, supply an input of –(full scale –½ LSB) for transition 0000000000 to 0000000001, and of (full scale –1½ LSB) for transition 1111111111 to 1111111110.

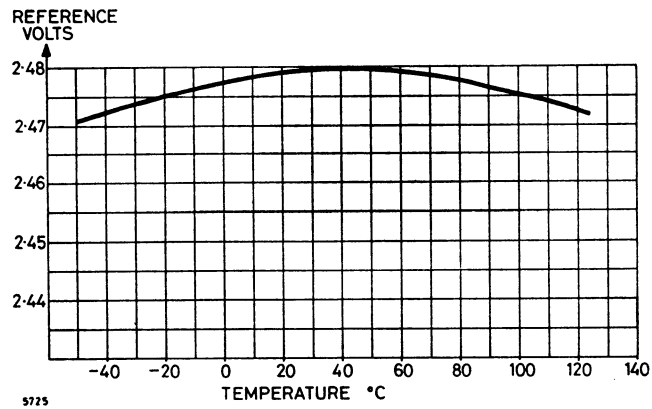
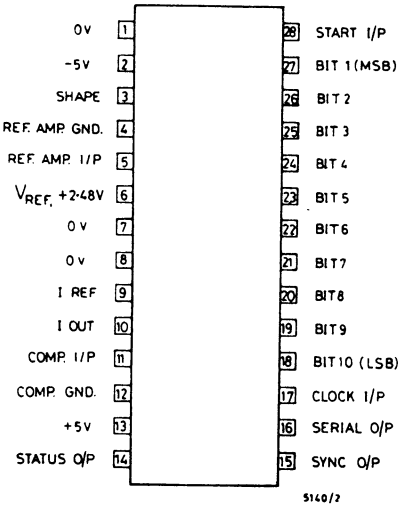
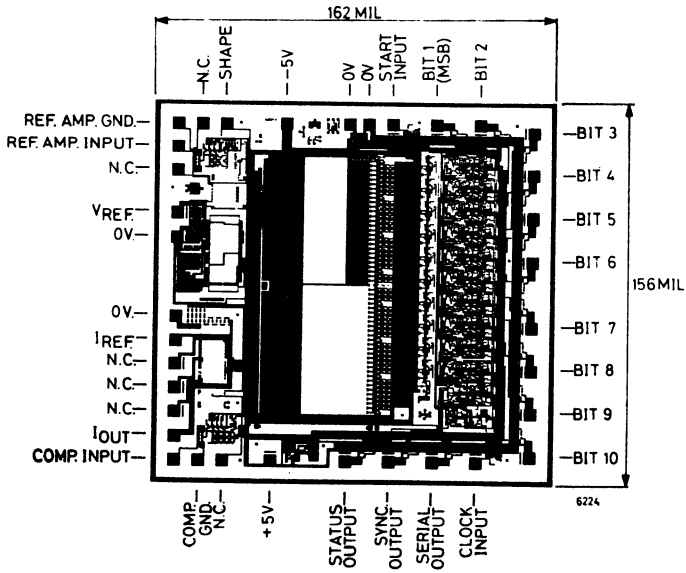


Fig. 6 – TYPICAL REFERENCE VOLTAGE v TEMPERATURE (ALL TYPES)

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

A to D CONVERTER

ZN432E

10-Bit Successive Approximation Monolithic A/D Converter

ADVANCE PRODUCT INFORMATION

FEATURES

- 10 Bit Resolution
- No Missing Codes
- 20 μs Conversion Time Guaranteed
- Input Range as Desired
- $\pm$ 5V Supplies, TTL/CMOS Compatible
- Parallel and Serial Outputs
- Bipolar Monolithic Construction
- Low Cost Moulded Package

DESCRIPTION

The ZN432E successive approximation analogue to digital converter combines several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), successive approximation logic with TTL interfacing, 2.5V precision voltage reference with reference amplifier, and fast comparator with good overload recovery. The overall accuracy of the A-D system is sufficient to guarantee no missing codes over the operating temperature range.

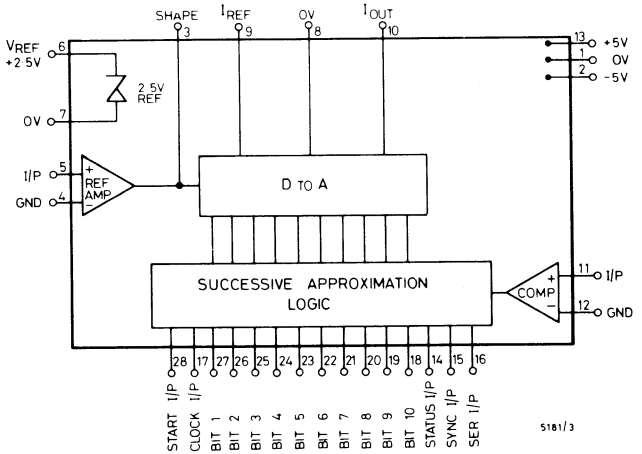


Fig. 1 – INTEGRATED CIRCUIT BLOCK DIAGRAM

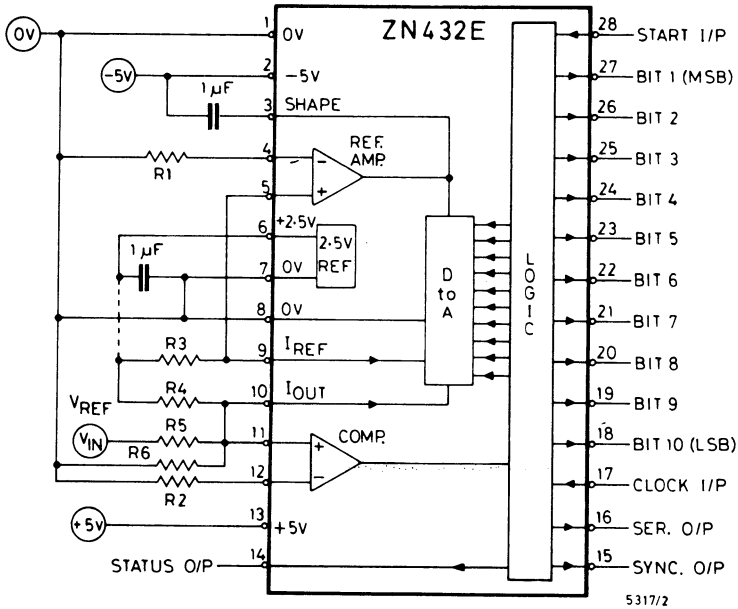


Fig. 2 – TYPICAL EXTERNAL COMPONENTS

ORDERING INFORMATION

TYPE No.	OPERATING TEMPERATURE RANGE	PACKAGE
ZN432E	0 to + 70°C	28 Pin Moulded DIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	± 7 volts	
Logic Input Voltage	$+V_{cc}$ and OV	
	Min.	Max.
Operating Temperature	0°C	+ 70°C
Storage Temperature	−55°C	+125°C

ELECTRICAL CHARACTERISTICS

(Supply Voltage = ± 5V, Tamb = + 25°C unless otherwise stated)

Parameter	Min.	Typ.	Max.	Units	Conditions
CONVERTER					
Resolution	10	–	–	Bits	
Linearity Error	−1	0	+1	LSB	
Differential Linearity Error	−0.8	0	+1	LSB	Note 1
DAC Reference Current (I_{REF})	0.25	0.5	1	mA	Note 6
Conversion Time	–	15	20	μS	Note 2
Nominal Analogue Input Range	−2.5	–	+2.5	V	Note 3
Supply Rejection		0.1		% per V	
Gain Error		+0.05		%	Note 4
Gain Tempco		20		ppm/°C	
Zero Tempco		15		ppm/°C	
Supply Voltage	± 4.5	± 5	+5.5	V	
Supply Current		35		mA	
Power Consumption		350		mW	
INTERNAL VOLTAGE REFERENCE					
Output Voltage	2.38	2.46	2.54	V	Note 5
Slope Impedance		0.75			
Maximum Load Current		± 2		mA	

CHARACTERISTICS *(continued)*

Parameter	$t_{amb} = +25°C$			Over Spec. Temp. Range		Units	Conditions
	Min.	Typ.	Max.	Min.	Max.		
LOGIC							
High level input voltage	2.0			2.0		V	
Low level input voltage			0.8		0.8	V	
High level input current		7				μA	$V_S = \pm 5.5V$ $V_I = 2.4V$
		50				μA	$V_S = \pm 5.5V$ $V_I = 5.5V$
Low level input current		1				μA	$V_S = \pm 5.5V$ $V_I = 0.4V$
High level output voltage	2.4			2.4		V	$I_{load} = -40\ \mu A$
Low level output voltage			0.4		0.4	V	$I_{load} = 1.6\ mA$

NOTE 1. No missing codes over full temperature range at resolution appropriate to accuracy.

NOTE 2. This corresponds to a maximum clock rate of 550 kHz based on 11 clock periods per conversion cycle (see timing diagram, 2-5). This provides an update rate of 45 kHz.

NOTE 3. Single polarity and other input ranges may be provided by different input resistor values. (See page 2–49)

NOTE 4. Excluding reference.

NOTE 5. For typical temperature performance see Fig. 5

NOTE 6. The full scale D to A output current I_{OUT} = 4 times I_{REF}. For optimum performance I_{REF} = 0.5 mA.

CALCULATION OF EXTERNAL RESISTORS (See Fig. 2)

1. R_3, R_4, R_5 can affect gain and offset stability and thus require to be of high quality.
2. R_1 and R_2 are to allow for the bias current of the reference amplifier and comparator, thus:

$$R_1 = R_3$$

And R_2 = parallel combination of R_4, R_5, and R_6.

3. I_{REF} should be 0.5mA
   Therefore

$$R_3 = \frac{V_{REF}}{0.5\ mA}$$

   $I_{out\ FS}$ is four times I_{REF}, i.e., 2 mA
4. Analysing the network yields the following:

$$R_4 = \frac{-V_{REF}\ R_5}{V_{in}\ min}$$

$$R_5 = \frac{V_{in}\ max - V_{in}\ min}{I_{out\ FS}}$$

   Where V_{in} max is the voltage for the logic output to be all 1's.
   V_{in} min is the voltage for the logic output to be all 0's.
5. R_6 should be chosen such that the parallel combination of R_4, R_5 and R_6 is about 1.25 k Ω as this determines the D to A time constant and hence conversion time.
6. The following is a table of values to give examples of the above equations.

V_{in} max	V_{in} min	V_{REF}	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
+2.5	–2.5	2.5	5 kΩ	1.25 kΩ	5 kΩ	2.5 kΩ	2.5 kΩ	∞
+2.5	–2.5	5*	10 kΩ	1.25 kΩ	10 kΩ	5 kΩ	2.5 kΩ	5 kΩ
+2.5	0	2.5	5 kΩ	1.25 kΩ	5 kΩ	∞	1.25 kΩ	∞
+5	0	2.5	5 kΩ	1.25 kΩ	5 kΩ	∞	2.5 kΩ	2.5 kΩ
+4	–2	2.5	5 kΩ	1.25 kΩ	5 kΩ	3.75 kΩ	3 kΩ	5 kΩ
+4	–2	12*	24 kΩ	1.25 kΩ	24 kΩ	3.75 kΩ	3 kΩ	5 kΩ
+10	–10	2.5	5 kΩ	1.25 kΩ	5 kΩ	2.5 kΩ	10 kΩ	3.33 kΩ

Note 1. Nearest preferred value may be used for R_1, R_2 and R_6
Note 2. External reference.

7. For setting up R_4 will adjust the offset.
   R_3 will adjust the gain.

For unipolar operation where R_4 approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of R_4 (Typical values only).

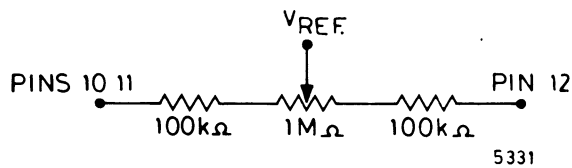


Fig. 3 – OFFSET CIRCUIT WITH UNIPOLAR OPERATION

TIMING DETAILS

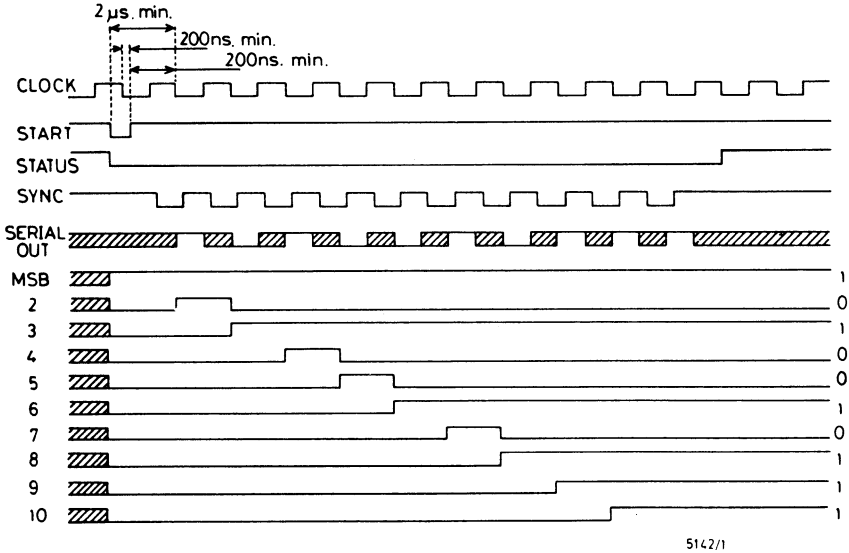


Fig. 4 – TIMING DIAGRAM

NOTES ON TIMING DIAGRAM

1. Conversion is initiated by a 'START' pulse which sets the MSB to 1 and all the other bits to 0.

2. The first active (negative going) edge of Clock after the trailing edge of the 'START' pulse should not occur until at least 2 µs after the leading edge of the 'START' pulse to allow for MSB settling.

3. A negative going edge of Clock must not occur within 200 ns either side of the trailing edge of the 'START' pulse.

4. As a special case of conditions (2) and (3) the 'START' pulse may be coincident with, and of the same duration as, a negative going clock pulse.

5. Serial data is available during conversion at the Serial Output.
   Ten SYNC pulses are provided to facilitate data transmission.
   The serial output data is valid on the positive going edge of the SYNC pulse.

6. Cross hatching indicates a 'don't care' condition or, in the case of serial output, invalid data.

7. The conversion sequence shown is for the digital word 1010010111.

8. The parallel output data is valid when the Status Output goes HIGH.

LOGIC CODING

Table 1. Unipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
FS −1LSB	1111111111
FS −2LSB	1111111110
¾ FS	1100000000
½ FS +1LSB	1000000001
½ FS	1000000000
½ FS −1LSB	0111111111
¼ FS	0100000000
1 LSB	0000000001
0	0000000000

Table 2. Bipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
+(FS −1LSB)	1111111111
+(FS −2LSB)	1111111110
+(½ FS)	1100000000
+(1LSB)	1000000001
0	1000000000
−(1LSB)	0111111111
−(½ FS)	0100000000
−(FS −1LSB)	0000000001
−FS	0000000000

NOTES:

1. Analogue inputs shown are nominal centre values of code.
2. "FS" is full scale.

OFFSET AND GAIN SETTING

For unipolar, supply an input of ½ LSB for transition 0000000000 to 0000000001, and of (full scale −1½ LSB) for transition 1111111111 to 1111111110.

For bipolar, supply an input of −(full scale −½LSB) for transition 0000000000 to 0000000001, and of (full scale −1½LSB) for transition 111111111111 to 1111111110.

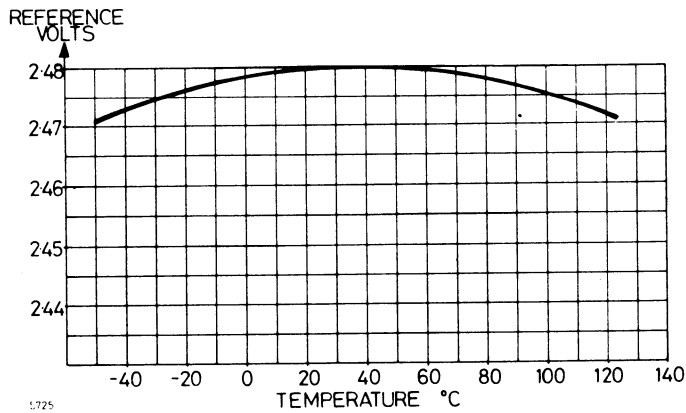


Fig. 5 – TYPICAL REFERENCE VOLTAGE v TEMPERATURE

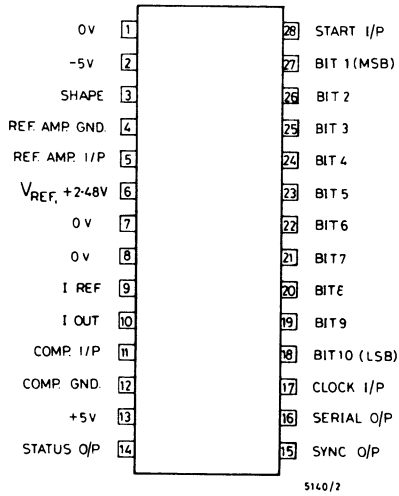


Fig. 6 – PIN CONNECTIONS

FERRANTI semiconductors

ZN433 Series

10 Bit A/D-Converter, Tracking

FEATURES

- 10, 9 and 8-Bit Accuracies
- 3 Operating Temperature Ranges
- 1μs Conversion Time (Assuming Continuous Tracking)
- Input Range as Desired
- ±5V Supplies, TTL/CMOS Compatible
- Parallel and Serial Outputs
- Bipolar Monolithic Construction

DESCRIPTION

The ZN433 range of tracking analogue to digital converters combines several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), tracking logic with TTL interfacing, 2.5V precision voltage reference with reference amplifier, and fast window comparator with good overload recovery. At a resolution appropriate to the accuracy specification, no missing codes are obtained over the full temperature range.

The tracking principle ensures continuous up to date conversion data. This is suitable for single channel conversion, e.g. digital transducers, and often obviates the need for sample and hold.

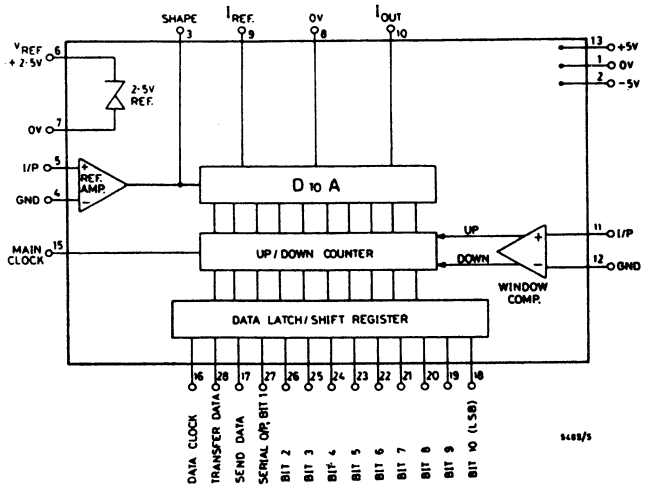


Fig. 1 – SYSTEM DIAGRAM

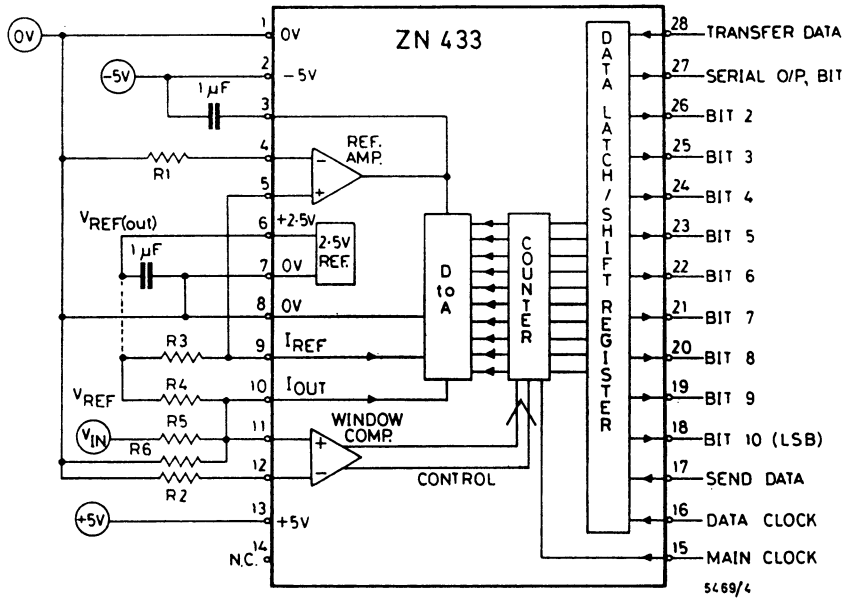


Fig. 2 – TYPICAL EXTERNAL COMPONENTS

See page 93 for calculation of resistor values. When the internal reference is used, $V_{REF(out)}$ (pin 6) is connected to R3 and R4 as shown. An external reference may also be used, which for ratiometric operation can vary by ±20% of nominal.

ORDERING INFORMATION

Operating Temperature	10-bit accuracy	9-bit accuracy	8-bit accuracy	Package
–55 to +125°C	ZN433J-10	ZN433J-9	ZN433J-8	Ceramic
–40 to +85°C	ZN433BJ-10	ZN433BJ-9	ZN433BJ-8	Ceramic
0 to +70°C	ZN433CJ-10	ZN433CJ-9	ZN433CJ-8	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply Voltages .. .. ±7 volts
Logic Input Voltage .. .. .. $+V_{CC}$ and 0V
Storage Temperature Range .. .. –55°C to +125°C

CHARACTERISTICS (at ±5V supplies and internal reference unless otherwise specified).

Parameter	Version	T_{amb} = +25°C			Over Spec. Temp. Range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
CONVERTER								
Accuracy (useful resolution)	ZN433J-10 ZN433BJ-10 ZN433CJ-10	10			10		Bits	Note 1
	ZN433J-9 ZN433BJ-9 ZN433CJ-9	9			9		Bits	
	ZN433J-8 ZN433BJ-8 ZN433CJ-8	8			8		Bits	
Non-linearity	All types			±0.5			LSB	
Differential non-linearity	All types		±0.5				LSB	Note 1
Operating temp. range	ZN433J-10 ZN433J-9 ZN433J-8				–55	+125	°C	
	ZN433BJ-10 ZN433BJ-9 ZN433BJ-8				–40	+85	°C	
	ZN433CJ-10 ZN433CJ-9 ZN433CJ-8				0	+70	°C	
D to A reference current, I_{REF} (pin 9)	All types	0.8		1.2	0.8	1.2	mA	Note 2
Max. Clock Rate	All types	1	1.2		1		MHz	Note 3
Nominal analogue input range	All types	–2.5		+2.5			V	Note 4
Supply rejection	All types		0.1				% per V	

ZN433 Series

CHARACTERISTICS *(continued)*

Parameter	Version	T_{amb} = +25°C			Over Spec. Temp. Range		Units	Conds.
		Min.	Typ.	Max.	Min.	Max.		
Gain temperature coefficient (Note 5)	ZN433J-10 ZN433BJ-10 ZN433CJ-10		10				ppm/°C	
	ZN433J-9 ZN433BJ-9 ZN433CJ-9 ZN433J-8 ZN433BJ-8 ZN433CJ-8		20				ppm/°C	
Zero temperature coefficient	ZN433J-10 ZN433BJ-10 ZN433CJ-10		7				ppm/°C of FSR	
	ZN433J-9 ZN433BJ-9 ZN433CJ-9 ZN433J-8 ZN433BJ-8 ZN433CJ-8		15				ppm/°C of FSR	
Supply voltage	All types	±4.5	±5	±5.5	±4.5	±5.5	V	
Supply current	All types		50				mA	
Power consumption	All types		500				mW	
INTERNAL VOLTAGE REFERENCE								
Output voltage	All types		2.480				V	
Output voltage tolerance (Note 6	ZN433J-10 ZN433BJ-10 ZN433CJ-10			±1.5			%	
	ZN433J-9 ZN433BJ-9 ZN433CJ-9			±2.0			%	
	ZN433J-8 ZN433BJ-8 ZN433CJ-8			±5.0			%	
Slope impedance	All types		0.75				Ω	
Maximum reference load current			±4				mA	

CHARACTERISTICS (*continued*)

Parameter	Version	T_{amb} = +25°C			Over Spec. Temp. Range		Units	Conditions
		Min.	Typ.	Max.	Min.	Max.		
LOGIC	All types							
High level input voltage		2.0			2.0		V	
Low level input voltage				0.8		0.8	V	
High level input current			7				μA	V_S = ±5.5V V_I = 2.4V
			50				μA	V_S = ±5.5V V_I = 5.5V
Low level input current			1				μA	V_S = ±5.5V V_I = 0.4V
High level output voltage		2.4			2.4		V	I_{load} = –40 μA
Low level output voltage				0.4		0.4	V	I_{load} = 1.6 mA

NOTE 1. No missing codes over full temperature range at resolution appropriate to accuracy.

NOTE 2. The full scale D to A output current I_{out} = 4 times I_{REF}. For optimum performance I_{REF} = 1.0 mA.

NOTE 3. For main clock waveform see Fig. 5, 2-60 . Input signals which do not change by more than 1 LSB/μs may be tracked continuously without the need for a sample and hold. This corresponds to a full scale bandwidth of 300 Hz. Higher frequencies may be tracked if the amplitude is reduced, e.g. the half full scale bandwidth is 600 Hz.

NOTE 4. Single polarity and other input ranges may be provided by different input resistor values (see 2-59)

NOTE 5. Excluding reference.

NOTE 6. For typical temperature performance see Fig. 6

TEST CIRCUIT

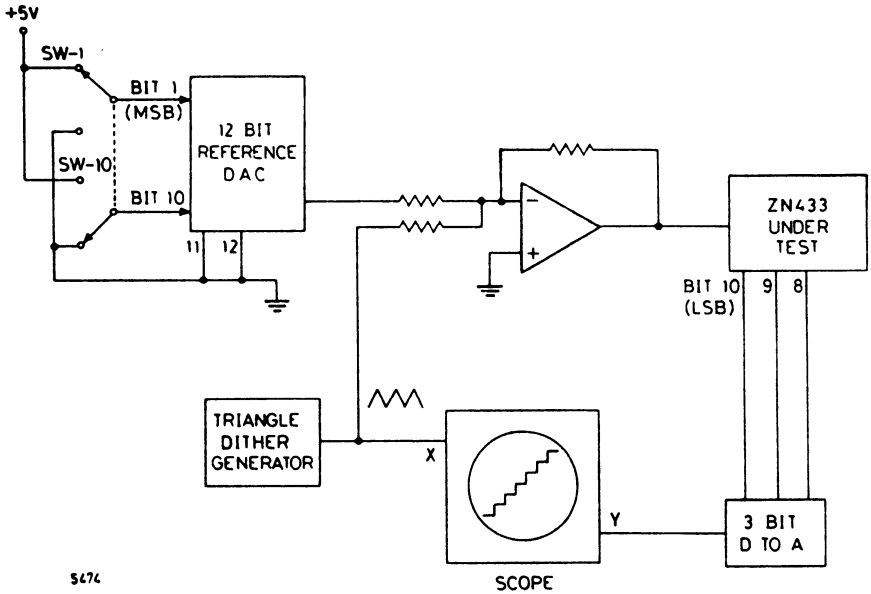


Fig. 3 – DYNAMIC CROSSPLOT ACCURACY TEST

Switches SW-1 to SW-10 are set to the appropriate digital code to select the point on the characteristic to be displayed. For example, code 10000 00000 would select half full scale, i.e. the major transition.

The output from the dither generator (suggested peak to peak amplitude = $\pm 4 \times$ L.S.B.) is used as the X deflection for the scope and is also superimposed on the analogue output from the reference D.A.C. in the summing amplifier. The resulting analogue signal including dither is used as V_{IN} for the ZN433 under test.

Bit 10, 9 and 8 outputs are fed to the inputs of a 3 bit D.A.C. of at least 6 bit accuracy and the analogue output used as the Y deflection for the scope. Differential non-linearity is shown by horizontal lines which are longer or shorter than the rest.

CALCULATION OF EXTERNAL RESISTORS (See Fig. 2)

1. R_3, R_4, R_5 can affect gain and offset stability and thus require to be of high quality.
2. R_1 and R_2 are to allow for the bias current of the reference amplifier and comparator which both operate in a virtual earth mode. Thus: $R_1 = R_3$
   And R_2 = parallel combination of R_4, R_5 and R_6.
3. I_{REF} should be 1.0 mA, though it may be varied from 0.8 mA to 1.2 mA,
   Therefore $$R_3 = \frac{V_{REF}}{1.0\ mA}$$
   $I_{out\ FS}$ is four times I_{REF}, i.e., 4 mA (I_{out} for zero reading is 0 mA).
4. Analysing the network yields the following:
   $$R_4 = \frac{-V_{REF}\ R_5}{V_{in}\ min}$$
   $$R_5 = \frac{V_{in}\ max - V_{in}\ min}{I_{out\ FS}}$$
   Where V_{in} max is the voltage for the logic output to be all 1's.
   V_{in} min is the voltage for the logic output to be all 0's.
5. R_6 should be chosen such that the parallel combination of R_4, R_5 and R_6 is about 625Ω as this determines the D to A time constant and hence conversion time.
6. The following is a table of values to give examples of the above equations.

V_{in} max	V_{in} min	V_{REF}	R_1[1]	R_2[1]	R_3	R_4	R_5	R_6[1]
+2.5	−2.5	2.5	2.5 kΩ	625Ω	2.5 kΩ	1.25 kΩ	1.25 kΩ	∞
+2.5	−2.5	5*	5 kΩ	625Ω	5 kΩ	2.5 kΩ	1.25 kΩ	2.5 kΩ
+2.5	0	2.5	2.5 kΩ	625Ω	2.5 kΩ	∞	625Ω	∞
+5	0	2.5	2.5 kΩ	625Ω	2.5 kΩ	∞	1.25 kΩ	1.25 kΩ
+4	−2	2.5	2.5 kΩ	625Ω	2.5 kΩ	1.875 kΩ	1.5 kΩ	2.5 kΩ
+4	−2	12*	12 kΩ	625Ω	12 kΩ	1.875 kΩ	1.5 kΩ	2.5 kΩ
+10	−10	2.5	2.5 kΩ	625Ω	2.5 kΩ	1.25 kΩ	5 kΩ	1.67 kΩ

Note 1. Nearest preferred value may be used for R_1, R_2 and R_6

*Note 2. External reference

7. For setting up: R_4 will adjust the offset.
   R_3 will adjust the gain.

For unipolar operation where R_4 approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of R_4 (Typical values only).

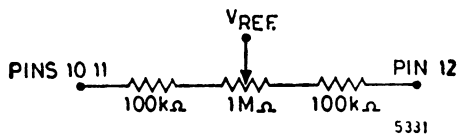


Fig. 4 – OFFSET CIRCUIT WITH UNIPOLAR OPERATION

LOGIC DETAILS

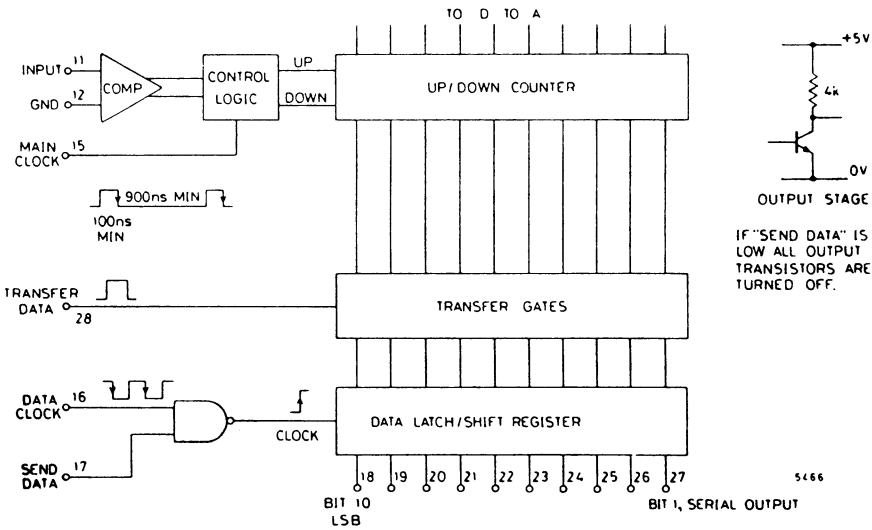


Fig. 5 – LOGIC SYSTEM

NOTES ON LOGIC DIAGRAM

1. The Window Comparator and Control Logic determine whether the Counter will clock up or down or keep the same value on an active (negative going) edge of the Main Clock.

2. Parallel data from the Up/Down Counter will be loaded into the output Data Latch/Shift Register when the TRANSFER DATA input is HIGH. TRANSFER DATA should not be taken HIGH until 150 ns after the MAIN CLOCK edge and should go LOW before the next MAIN CLOCK edge. The minimum TRANSFER DATA pulse width is 50 ns.

   If TRANSFER DATA is held permanently HIGH then the Counter outputs will appear directly at the bit outputs.

3. Serial output data (MSB first) can be obtained from the MSB output (Pin 27) by applying a DATA CLOCK (Pin 16, 1 MHz maximum, 100 ns minimum pulse width).

4. A LOW on SEND DATA (Pin 17) disables the DATA CLOCK and turns off all the output transistors so that all the bit outputs are HIGH (see diagram of output).

LOGIC CODING

Table 1. Unipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
FS –1LSB	1111111111
FS –2LSB	1111111110
¾ FS	1100000000
½ FS +1LSB	1000000001
½ FS	1000000000
½ FS –1LSB	0111111111
¼ FS	0100000000
1LSB	0000000001
0	0000000000

Table 2. Bipolar Operation

Analogue Input Notes 1, 2	Digital Output Code MSB LSB
+(FS –1LSB)	1111111111
+(FS –2LSB)	1111111110
+(½ FS)	1100000000
+(1LSB)	1000000001
0	1000000000
–(1LSB)	0111111111
–(½ FS)	0100000000
–(FS –1LSB)	0000000001
–FS	0000000000

NOTES:

1. Analogue inputs shown are nominal centre values of code.
2. "FS" is full scale.

OFFSET AND GAIN SETTING

For unipolar, supply an input of ½LSB for transition 0000000000 to 0000000001, and of (full scale –1½LSB) for transition 1111111111 to 1111111110.

For bipolar, supply an input of –(full scale –½LSB) for transition 0000000000 to 0000000001, and of (full scale –1½LSB) for transition 1111111111 to 1111111110.

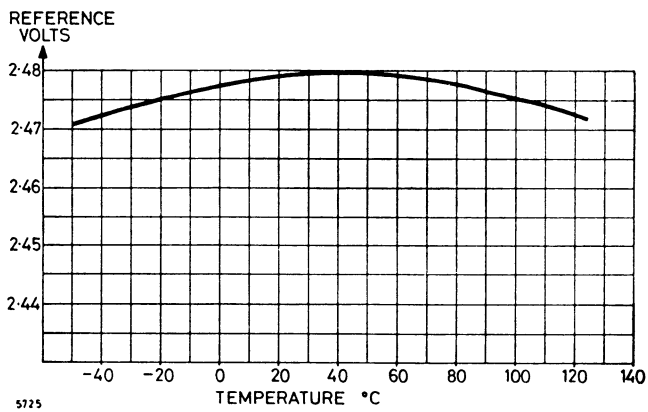
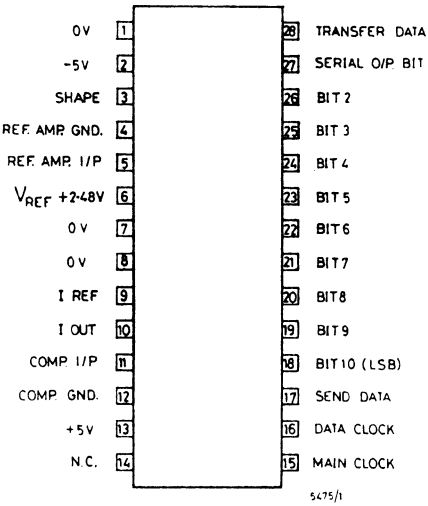


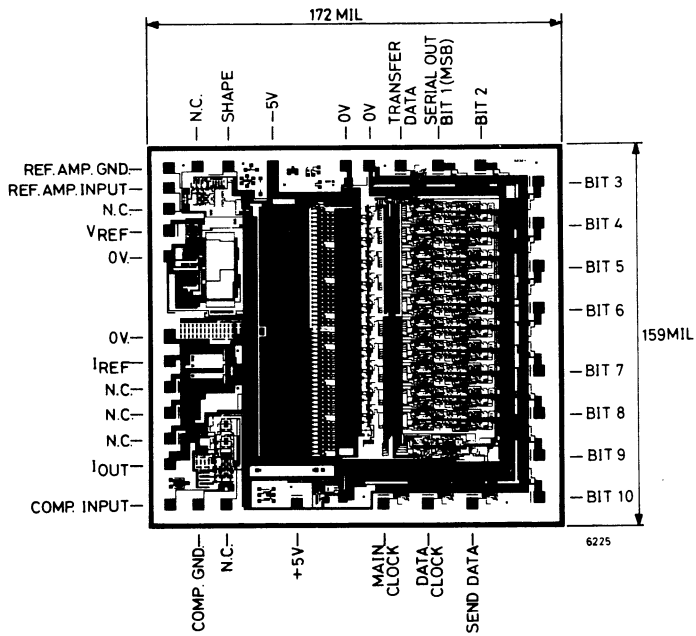
Fig. 6 – TYPICAL REFERENCE VOLTAGE v TEMPERATURE (ALL TYPES)

ZN433 Series

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



FERRANTI semiconductors

ZN440
ZN441

6 Bit Flash Video-Converter, 16/10 MHz

ADVANCE PRODUCT INFORMATION

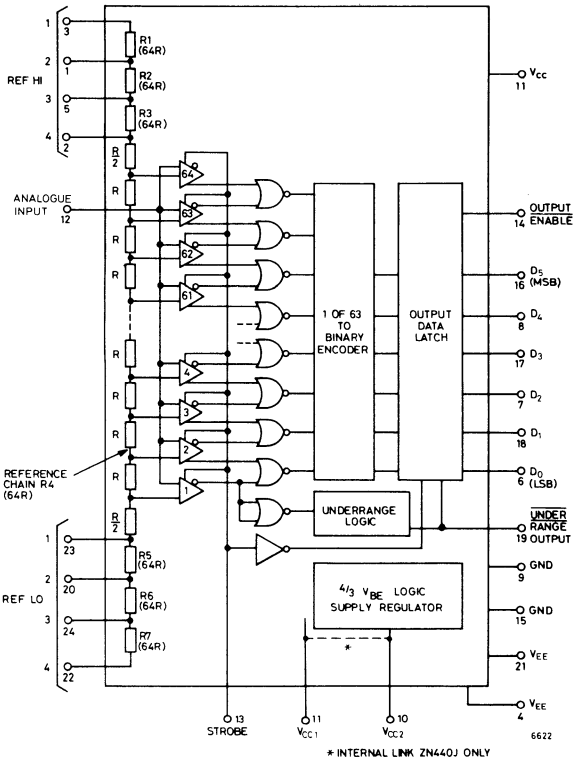
FEATURES

- 16MHz sample rate - ZN440
- 6-bit resolution
- Expandable to 7 or 8 bits
- ± ½ LSB linearity
- No sample and hold required
- Unipolar or bipolar analogue input
- TTL compatible outputs
- ± 5V supply
- 700mW power dissipation

DESCRIPTION

The ZN440 is a high speed, 6-bit, parallel A to D converter capable of digitising analogue signals at rates up to 16 mega-samples per second. AC signals with frequency components up to several MHz can accurately be digitised without the need for a sample-and-hold circuit. Two or four ZN440/1's can be stacked to give a 7- or 8-bit converter with a minimum of external components. The ZN441 is a lower speed selection from the ZN440 giving a minimum sample rate of 10MHz.

Applications include high-speed data acquisition, video and radar data conversion digital signal storage and image processing.



ZN440/1 System Diagram

ABSOLUTE MAXIMUM RATINGS

V_{CC}	0 to +5.5V
V_{EE}	0 to −5.5V
Inputs, digital	0 to +5V
Inputs, V_{REF} and analogue signal	−4.2 to +1.4V
Reference resistor current	60mA
Operating temperature range	0°C to +70°C
Storage temperature range	−55°C to +125°C

Electrical characteristics (±5V supply, T_{amb} = +25°C unless otherwise stated, test circuit as fig.15).

Parameter	Min.	Typ.	Max.	Units	Conditions
POWER SUPPLY					
Recommended supply voltage					
V_{CC1}	4.75	5	5.25	volts	
V_{CC2}	1.8	2	V_{CC}	volts	(See Note 1)
V_{EE}	−4.75	−5	−5.25	volts	
Supply current					
I_{CC1}	–	10	25	mA	
I_{CC2}	–	90	125	mA	
I_{EE}	–	95	115	mA	
ANALOGUE					
Comparator common-mode voltage	−4.0	–	+0.5	volts	
Reference voltage span - V_{REF}	–	–	1.0	volts	
Analogue span - V_{FSR}	–	–	1.0	volts	
Linearity error	–	–	±0.5	LSB	V_{REF} = 1V
	–	–	±1	LSB	V_{REF} = 0.5V
Input resistance, R_{IN}	8	–	–	kΩ	
Input bias current, I_{IN}	–	–	90	μA	V_{REF} = 1V
Input capacitance, C_{IN}	–	–	100	pF	

Parameter	Min.	Typ.	Max.	Units	Conditions
DIGITAL					
High level output voltage V_{OH}	2.4	–	–	volts	
Low level output voltage V_{OL}	–	–	0.4	volts	
(Strobe)					
High level input voltage, V_{IH}	3.0	–	–	volts	
Low level input voltage, V_{IL}	–	–	0	volts	(See Note 2)
High level input current, I_{IH}	–	–	150	μA	$V_{IH} = 3V$
Low level input current, I_{IL}	–	–	150	μA	$V_{IL} = 0V$
(Output Enable)					
High level input voltage V_{IH}	2	–	–	volts	
Low level input voltage V_{IL}	–	–	0.8	volts	
High level input current I_{IH}	–	–	–	–	(See Note 3)
Low level input current I_{IL}	–	–	4	mA	
DIGITAL					
(Dynamic)					
Minimum convert pulse width - T_H	–	20	–	ns	
Minimum strobe low period - T_L	–	40	–	ns	See STROBE circuit and text on digital delays
Maximum sampling frequency	14	16	–	MHz	ZN440
	10	12	-	MHz	ZN441
Transient response	–	15	–	ns	Full scale step input
Aperture delay T_{ad}	–	20	–	ns	
Aperture jitter	–	–	300	ps	
Digital output delays					
t_1	50	75	100	ns	
t_2	90	105	120	ns	
t_3	50	65	80	ns	
t_4	65	78	100	ns	
Differential output					
Delays (max. variation in output delays within one device)					
$(t_2 - t_4)$	25	–	40	ns	
$(t_1 - t_3)$	0	–	40	ns	
Output enable/disable delays					
t_{D1}	7	8	15	ns	
t_{D2}	27	28	40	ns	
t_{E1}	22	25	35	ns	
t_{E2}	35	40	80	ns	

Note 1 : Linearity performance is improved by connecting V_{CC2} to a nominal 2V supply (see section "Power Supply Connections").

Note 2 : To enable the Input of the ZN440/1 to be driven from TTL outputs a simple emitter-follower buffer can be used as shown in section "Clock Generator and strobe Driver Circuit" (page 13).

Note 3 : See page 9, section "Output Enable".

GENERAL DESCRIPTION

The ZN440/1 is an ultra high-speed parallel (flash) A to D converter comprising an array of 64 strobed comparators, encoding logic and an output latch.

A reference voltage applied across a tapped resistor chain defines 63 quantisation levels plus under-range and overrange, one input of each comparator being connected to the resistor string and the other input to the analogue signal. When an analogue voltage is applied all comparators whose reference voltage is less than the input voltage will change state i.e. if the input voltage is $\frac{n}{64}$ of V_{REF} then n comparators will have tripped. The comparator outputs are decoded into a 1 of 64 format by NOR gates then re-encoded into binary by a high-speed ROM and stored in an output latch.

STROBE INPUT

The strobe input controls the comparators and output data latch. Whilst strobe is high the comparators are sampling the input signal and the result of a previous sample is stored in the output latch.

When strobe goes low the comparator outputs are latched in their current state, the latch becomes transparent and the results of the new sample propagate through the latch to the data outputs.

The strobe input is buffered by an emitter follower circuit which is TTL compatible. However, for maximum speed a minimum high level of + 3V is recommended. When driving from a totem pole output this may be achieved using an external 1k pullup resistor.

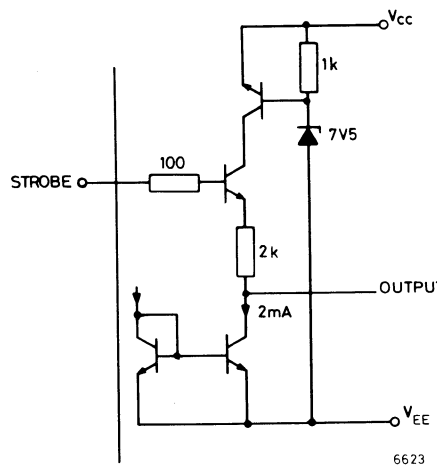


Fig. 2 Equivalent Circuit of STROBE Input

DEFINITIONS OF FLASH CONVERTER PARAMETERS

Digital Output Delays

These effectively define the response time of the ADC, i.e. the time which elapses between strobe going low to sample the input and the appearance at the outputs of the data word corresponding to the sample.

Digital output delay is made up of three components.

1) Aperture delay. This is the time elapsed between the strobe input going low and the actual instant at which the comparator outputs 'freeze'. It is due mainly to the propogation delay of the strobe driver circuit.

2) Internal logic delays through the encoder. These determine the minimum strobe low period since strobe must not go high to latch the data before the new data word appears at the latch inputs

   The minimum strobe high period is determined by the time the comparators need to respond after strobe goes high.

   The minimum strobe low and high periods determine the maximum permissible strobe (sampling) frequency.

3) Latch and output stage delays. Since these occur after the point in the circuit at which the data is latched they do not affect maximum sampling rate but only add an extra delay onto the output data.

   A timing diagram for the digital output delays is given in fig. 3. This shows typical timing waveforms for a 13.3 MHz sample rate.

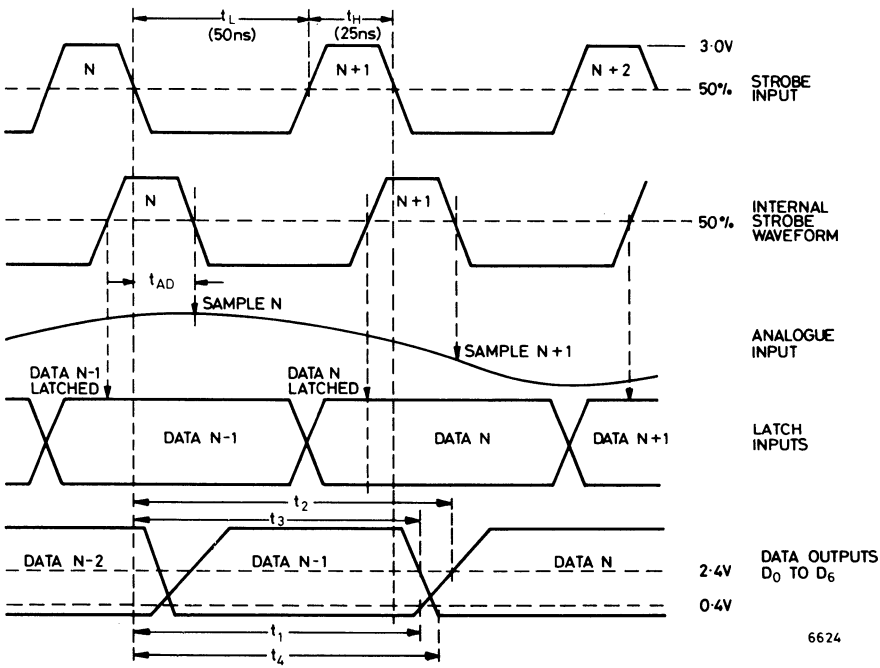


Fig. 3 Typical Timing Diagram at 13.3 MHz Sample Rate

One question which is often not discussed thoroughly in flash converter specifications is when to sample the outputs to ensure a valid data word, taking into account device-to-device tolerances in digital output delays.

Consider the case of two converters, one with the maximum output delays and one with the minimum output delays in a situation where a data bit changes to a '1' on the Nth sample and an 'O' on the (N + 1)th sample. In the case of the slower converter the data N will not become valid until 120 ns after the Nth falling strobe edge, ($t_{2\ MAX.}$), whereas in the case of the faster converter the data N will become invalid 50ns after the (N + 1)th falling strobe edge ($t_{3\ MIN.}$).

There is thus a window during which the output data will be valid for any device. Its width is ($t_S + t_{3\ MIN.} - t_{2\ MAX.}$) This is illustrated in fig. 4.

The choice of when to sample the output data therefore depends on the sampling frequency and the strobe duty-cycle.

Where $t_L > t_{2(MAX.)}$ [120ns] data N will always be valid by the (N + 1)th rising strobe edge, as shown in fig. 4. The highest sampling frequency for which this holds is about 7.1 MHz ($t_L = 120ns$, $t_H = 20ns$).

Up to about 8.3 MHz data N may be sampled on the (N + 1)th falling strobe edge. Above 8.3 MHz the strobe period t_S becomes less than 120ns so data N may not have become valid on this edge for devices with the longest output delays. This is shown in fig. 5.

Alternatively, if $t_L < 50ns$ then data N-1 will still be valid on the (N + 1)th rising strobe edge, even for a device with the minimum output delays. This is also shown in fig. 5.

This holds up to about 14 MHz, when the data valid window disappears, as illustrated in fig. 6. Above this frequency the data sampling point must be adjusted on test for each device.

When operating near the maximum sample rate it will be necessary to make provision for adjusting the strobe duty-cycle since the strobe high and low periods for reliable strobing at the maximum sample rate can vary from device to device. For example at 16 MHz one device may require $t_H = 15ns$ and $t_L = 47.5ns$ whilst another requires $t_H = 25ns$ and $t_L = 37.5ns$.

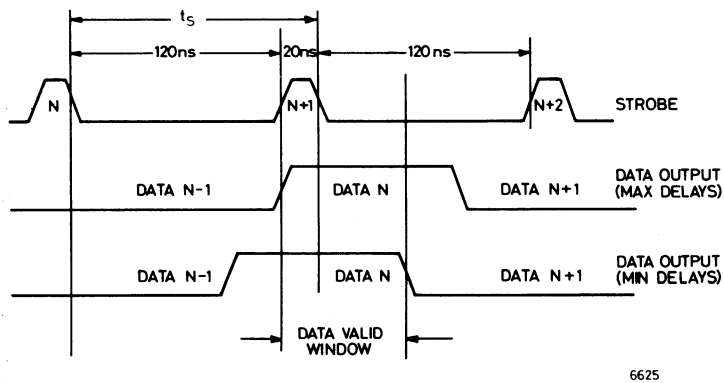


Fig. 4 If $t_L > 120ns$ output data N is valid on rising strobe edge N + 1. Limiting sample rate is 7.1 MHz as shown here.

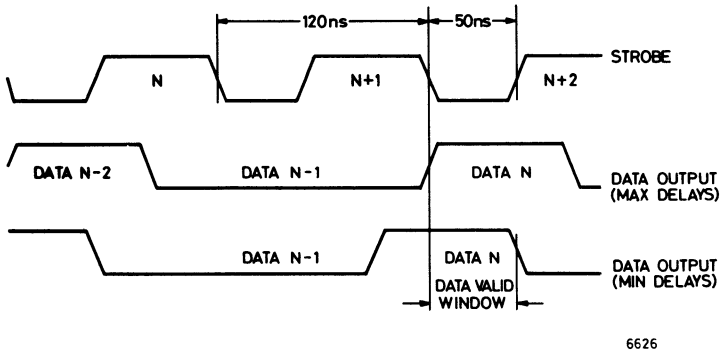


Fig. 5 Up to 8.3 MHz sample rate output data N may be sampled on negative strobe edge N + 1. Alternatively data may be sampled on positive strobe edge N + 2 provided $t_L < 50ns$.

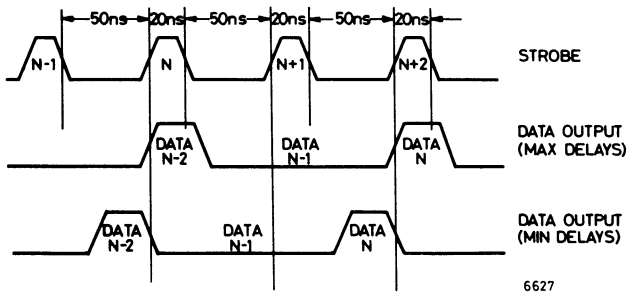


Fig. 6 At around 14 MHz the data valid window vanishes and data sampling instant must be adjusted on test for each device.

MAXIMUM SIGNAL FREQUENCY

The maximum analogue input frequency that can be digitised is determined by the sampling frequency. However, the accuracy with which it can be digitised is determined by aperture jitter.

Due to differing on-chip path lengths the aperture delay is not identical for each comparator. This variation in aperture delay is known as differential aperture delay or aperture jitter.

The effect of aperture jitter is that the aperture delay is dependent on the highest active comparator in the chain, which depends on signal level. The aperture delay and thus the sampling interval varies with signal level, which means that some samples occur earlier and some occur later than nominal. When sampling an A.C. signal this makes the sampled voltage higher or lower than the ideal value, depending on the slope of the signal waveform.

As the slew rate increases the effect becomes worse.

The effect of aperture jitter is illustrated in fig. 7, which shows what happens when a triangular waveform is digitised, then reconstituted using a DAC with a constant sampling interval.

The maximum slew rate that can satisfactorily be digitised can be calculated by considering the effect of aperture jitter as a slew rate dependent linearity error and defining an acceptable limit for its contribution to total error budget. Alternatively the error due to aperture jitter for a given slew rate can easily be calculated.

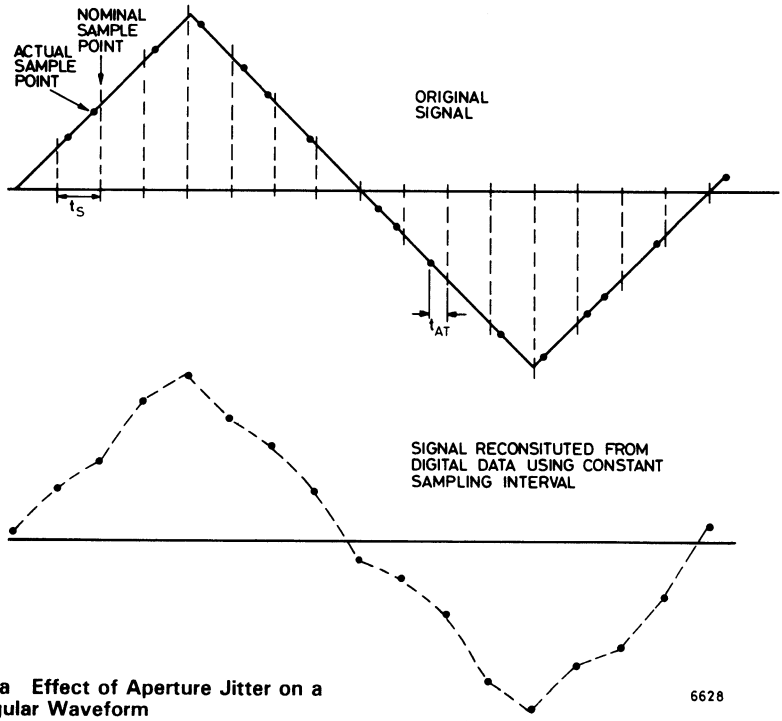


Fig. 7a Effect of Aperture Jitter on a Triangular Waveform

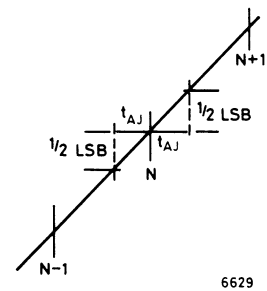


Fig. 7b Linearity Errors due to Aperture Jitter

Fig. 7b shows three consecutive samples, with the centre one being subject to aperture jitter. The aperture jitter error (L.S.B.) is $\frac{\text{slew rate (L.S.B./ps).}}{2t_{AJ}\text{ (ps)}}$

Alternatively, defining the maximum acceptable error as ± ½ LSB the limiting slew rate is $\frac{1\text{ LSB.}}{2t_{AJ}}$

For the ZN440/1 with a maximum aperture jitter of 300ps this gives a maximum slew rate of 1.65 LSB/ns or 1650 LSB/μs.

Perhaps of more interest is the maximum signal frequency that can accurately be digitised.

A sinewave signal is described by the equation $A = A_{PEAK} \sin 2\pi ft$.

For a full-scale sinewave applied to the ZN440/1 A_{PEAK} may be written as 32 L.S.B.

$$V = 32 \sin 2\pi ft.$$

$$\text{and } \frac{dV}{dt} = 32x2x\pi f. \cos 2\pi ft.$$

A sinewave has its maximum slew rate at zero where $\cos 2\pi ft. = \cos 0 = 1$. Therefore, substituting the previously calculated value of 1.65 LSB/ns or 1650 LSB/μs

$$\frac{dV}{dt} \text{ MAX.} = 1650 = 32.2\ \pi f_{MAX.(MHz)}$$

$$f_{MAX.} = \frac{1650}{32x2} = 8.2 \text{ MHz}$$

i.e. the maximum input frequency for the ZN440/1 is limited by sampling rate rather than aperture jitter.

OUTPUT $\overline{\text{ENABLE}}$

All logic outputs of the ZN440/1 are of the open-collector type requiring an external pullup resistor of nominally 2k. The data output transistors may be turned off by taking the $\overline{\text{ENABLE}}$ pin high. A timing diagram for output enable/disable delays is given in fig. 8.

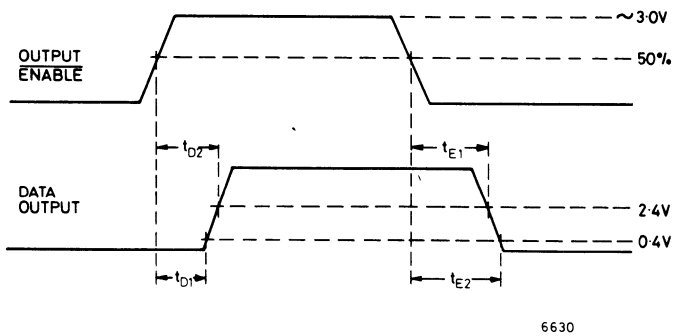


Fig. 8 Output $\overline{\text{ENABLE}}$ Timing

The $\overline{\text{ENABLE}}$ input is a high-speed current driven input. It may be driven from a standard TTL output but the output may not achieve a logic '1' level and should not be used to drive other gates. If driven from any other type of circuit the input current should be limited to 1mA. An equivalent circuit of the $\overline{\text{ENABLE}}$ input is shown in fig. 9.

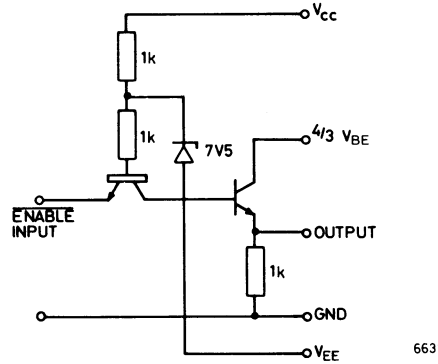


Fig. 9 $\overline{\text{ENABLE}}$ Input Equivalent Circuit

UNDERRANGE/OVERRANGE

To facilitate stacking of two or more converters the data outputs are active only when the analogue voltage is within the full-scale range of the ADC.

If V_{IN} is greater than $+V_{REF} - \frac{1}{2}$ LSB then the data outputs are at full-scale (111111) and the output transistors are turned off in any event.

If V_{IN} is less than $-V_{REF} + \frac{1}{2}$ LSB then the $\overline{\text{UNDERRANGE}}$ output is low and the data output transistors are also turned off.

LOGIC CODING

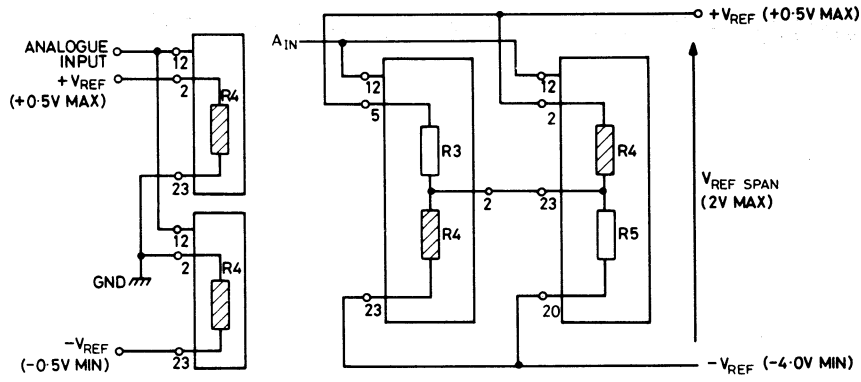
ANALOGUE INPUT VALUE (A_{IN})	UNDER RANGE OUTPUT $\overline{UR}$	DIGITAL OUTPUTS D_S.....D_O
$A_{IN} > +V_{REF} - \frac{1}{2}$LSB	1	111111
$+V_{REF} - \frac{1}{2}$LSB $> A_{IN} > +V_{REF} - 1\frac{1}{2}$LSB	1	111110
"	"	"
"	"	"
"	"	"
"	"	"
"	"	"
"	"	"
$-V_{REF} + 2\frac{1}{2}$LSB $> A_{IN} > -V_{REF} + 1\frac{1}{2}$LSB	1	000001
$-V_{REF} + 1\frac{1}{2}$LSB $> A_{IN} > -V_{REF} + \frac{1}{2}$LSB	1	000000
$A_{IN} < -V_{REF} + \frac{1}{2}$LSB	0	111111

STACKING

Provision of an underrange output and the fact that both ends of the reference resistor chain are accessible means that two or four ZN440/1's can easily be stacked to form a 7– or 8– bit converter. In theory the reference chains of two or four ZN440/1's could simply be connected in series to give an array of 128 or 256 comparators and thus 7– or 8– bit resolution.

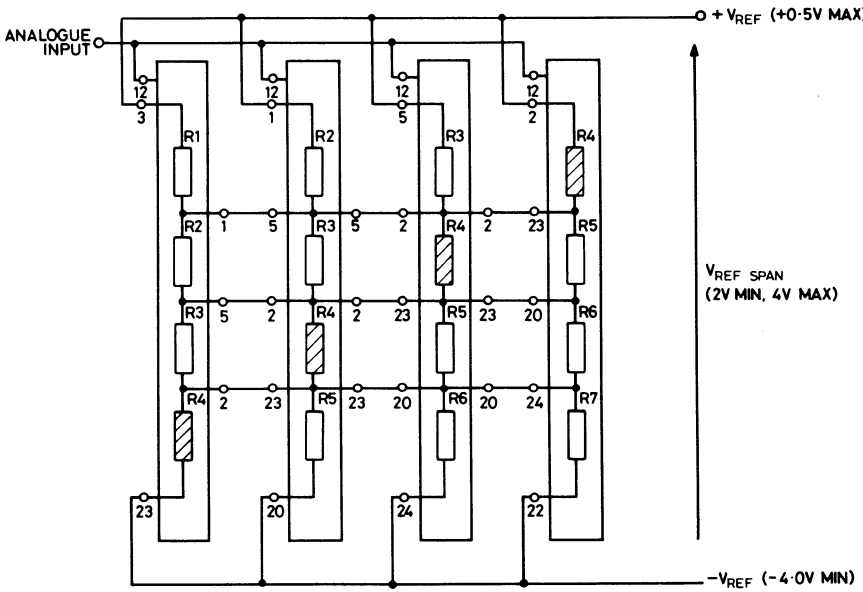
However, due to differences in the absolute value of resistor between different IC's the voltage drop across each reference chain might not be the same, giving rise to linearity errors.

To overcome this problem the ZN440/1 is provided with additional (untapped) resistors at each end of the reference chain. By making suitable connection to these resistors it is possible to make each ZN440/1 operate over half the total reference voltage in the case of the 7– bit stack or one-quarter of the total reference voltage in the case of the 8– bit stack. The reference chain connections for 7– and 8– bit stacks, for both unipolar and bipolar operation, are shown in fig. 10.



a) 7-BIT STACK WITH SYMMETRICAL BIPOLAR FSR

b) 7-BIT STACK



c) 8 BIT STACK

Fig. 10 Reference Connections for Stacking

Fig. 11 Logic Connections for 7 – bit Stacking

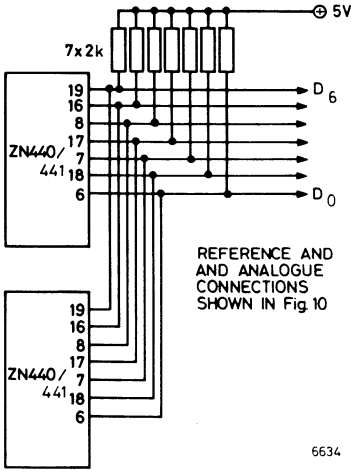
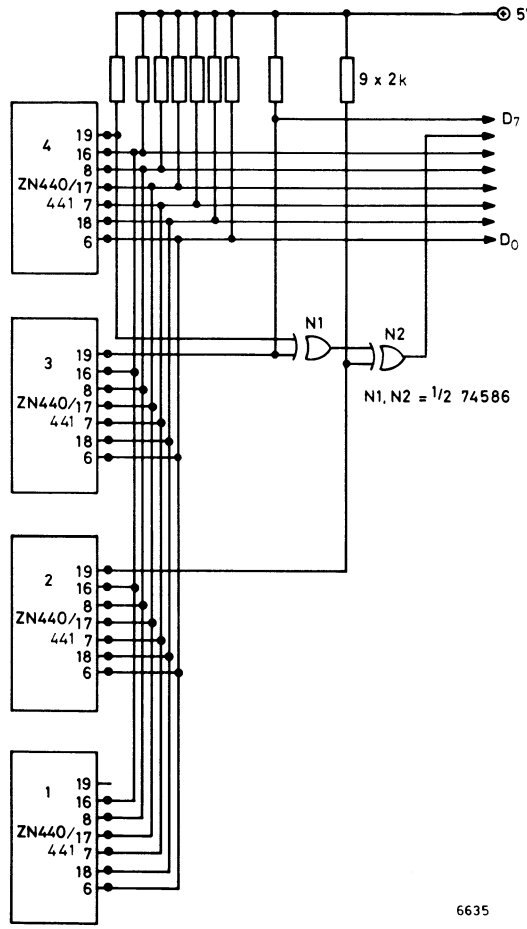


Fig. 12 Logic Connections for 8 – bit Stacking



The matching of the reference resistors is sufficiently accurate to ensure that linearity is maintained for the 7 – and 8 – bit stacks. Each converter operates over its own portion of the reference range without any overlap or gaps at the transition points.

Note that the total reference voltage for the stacked converters should be chosen so that the reference voltage across the reference chain (R4) in each converter is within the 0.5 to 1V limit, e.g. for the 8 – bit unipolar stack the total reference voltage should be between 2V and 4V.

In stacking configurations the six least significant bits are obtained simply by bussing together the D_0 to D_5 outputs of all the converters. In the case of a 7 – bit stack the MSB (D_6) is simply the underrange output of the second converter, as shown in fig. 11. In order to give the same loading conditions as the other six outputs it is wire AND-ed to the output of the first converter though this has no effect from a logic point of view.

For the eight bit configuration D_6 and D_7 are obtained by decoding the underrange outputs using two exclusive-OR gates as shown in fig. 12. This, of course, increases the output delays due to the additional propagation delays introduced into the D_6 and D_7 outputs.

POWER SUPPLY CONNECTIONS

The internal current-mode logic of the ZN440/1 operates from a $\frac{4}{3}$ V_{BE} supply (approx. 1V) which is supplied by an on-chip series regulator. In the ZN440/1CJ the regulator input is available at pin 10 and may be supplied with a nominal 2V supply to reduce chip dissipation.

This reduces chip temperature which reduces thermal gradients across the chip, improving linearity. A suitable circuit for providing this voltage is given in fig. 13.

The original version of the ZN440 - the ZN440J - has pins 10 and 11 linked internally. No external connection should be made to pin 10.

The ZN440J is a maintenance type and is not recommended for new designs.

When powering up the ZN440/1 care must be taken not to apply V_{CC} before V_{EE} as this may occasionally cause a latch-up condition.

A 50Ω resistor in series with pin 11 will prevent this condition.

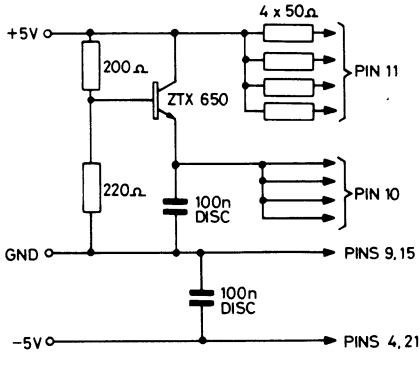


Fig. 13 Suggested Supply Connections for up to Four ZN440/1's

CLOCK GENERATOR AND STROBE DRIVER CIRCUIT

A suggested circuit for generating the STROBE pulses to the ZN440/1 is shown in fig. 14. This consists of an oscillator based on Schmitt trigger N1 driving a pulse shaper circuit comprising N3-N6. The clock frequency and STROBE high period can be independently adjusted using P1 and P2 respectively.

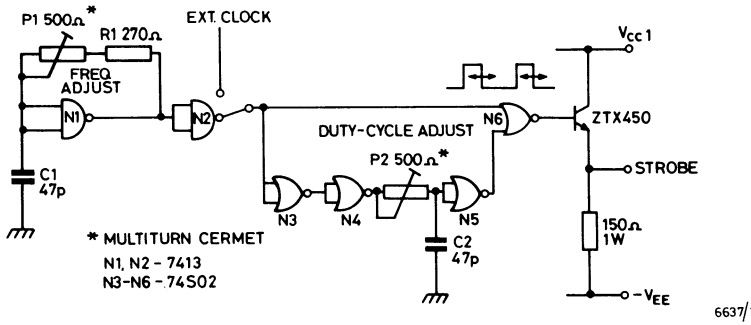
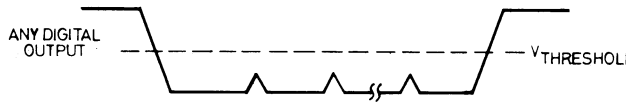


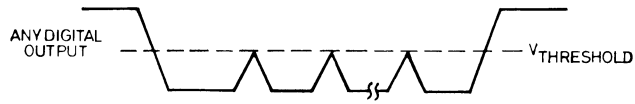
Fig. 14 Suggested Clock and Strobe Drive Circuit

The ZN440/1 may be operated at higher frequencies than those specified, if precautions are taken to avoid encoding errors, caused by clock related glitches on the digital outputs. The amplitude of these glitches which are frequency dependant will vary according to the settings of the clock waveform and will produce encoding errors if they exceed the input threshold of the following external logic gates. The following are recommended solutions:

a) By using logic gates with higher input threshold levels e.g. Schmitt trigger inputs.
b) By using latched inputs - care must be taken though to ensure that the data is actually read whilst the digital outputs are below the latch input threshold voltage. Also, allowances must be made for the device output delays.
c) The clock can be trimmed to give a minimum glitch amplitude - but this setting can be subject to drift with temperature.
d) By taking the negative supply rail (V_{EE}) more negative e.g. -5.5V (but with $V_{EE} = -5.5V$, $V_{CCmax} = 5V$). Conversely if V_{EE} is more positive than $-5V$ the effective speed of the device will be reduced.



Glitches well below the threshold voltage.



Glitches just reaching threshold voltage - precautions need to be taken.

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TEST CIRCUIT

A suggested test circuit for the ZN440/1 is shown in fig. 15. The loading conditions on all data outputs should be as shown.

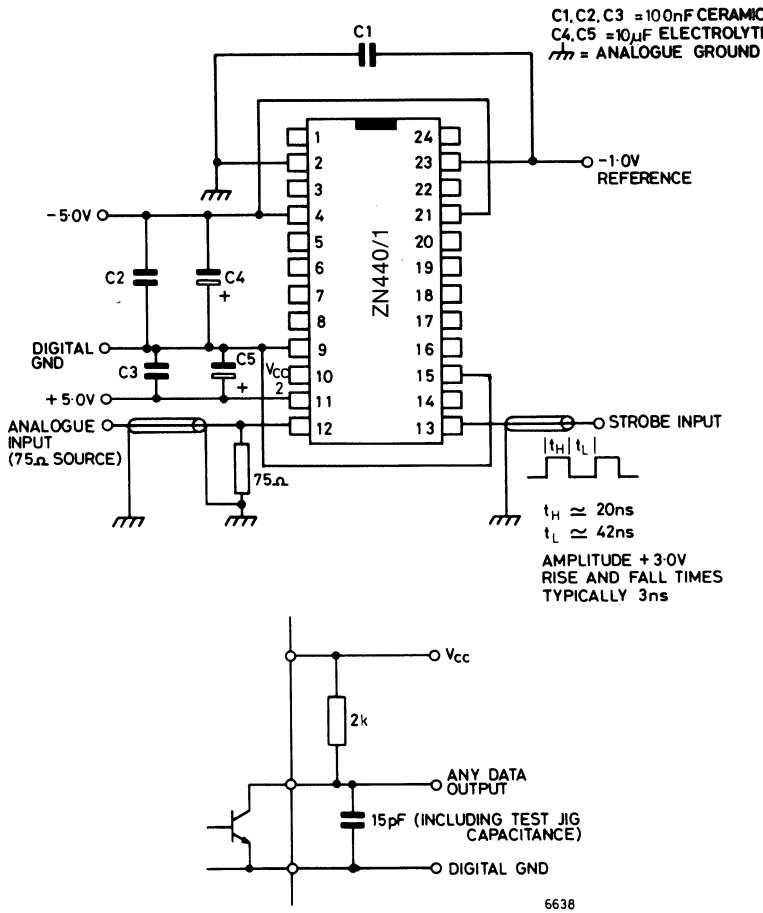
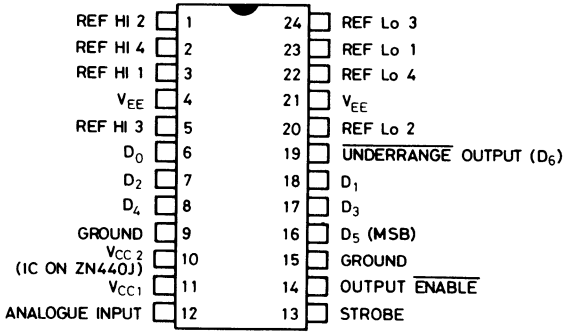


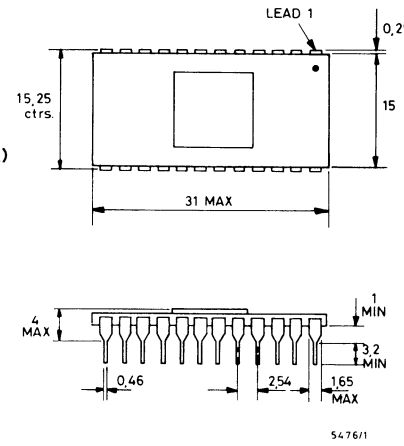
Fig. 15 ZN440/1 Test Circuit and Output Loading

ZN440/1

PIN CONNECTIONS



PACKAGE DETAILS



24 Lead Ceramic D.I.L.
Dimensions in millimetres

ORDERING INFORMATION

Type Number	Operating Temperature Range	Package
ZN440J*	0°C to +70°C	Ceramic
ZN440CJ	0°C to +70°C	Ceramic
ZN441CJ	0°C to +70°C	Ceramic

* Maintenance type, not recommended for new designs.

FERRANTI semiconductors

ZN447
ZN448
ZN449

8 Bit A/D-Converter, μP-compatible

ADVANCE PRODUCT INFORMATION

FEATURES

- **Easy interfacing to microprocessors or operates as a 'stand alone' converter**
- **Fast 9 µs conversion time guaranteed**
- **Choice of linearity: ¼LSB—ZN447, ½LSB—ZN448, 1LSB—ZN449**
- **On-chip clock**
- **Choice of on-chip or external reference voltage**
- **Unipolar or bipolar input ranges**
- **Choice of commercial or military temperature range**

DESCRIPTION

The ZN447, ZN448 and ZN449 are 8-bit, successive approximation A to D converters designed for easy interfacing to microprocessors. All active circuitry is contained on-chip including a clock generator and stable 2.5V bandgap reference.

Only a reference resistor and capacitor, clock resistor and capacitor and input resistors are required for operation with either unipolar or bipolar input voltages. The ZN447, -8 and 9 are the most complete 8-bit monolithic ADCs available.

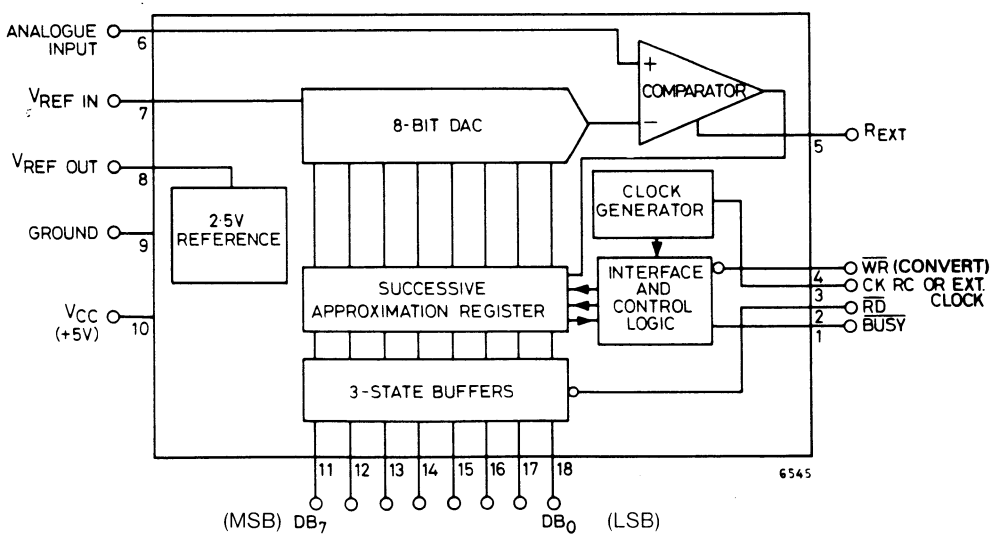


Fig. 1 SYSTEM DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... +7.0 volts
Max. Voltage, Logic and V_{REF} Inputs ..... V_{CC}
Operating Temperature Range ..... 0°C to +70°C ('E' package)
−55°C to +125°C ('J' package)
Storage Temperature Range ..... −55°C to +125°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, Tamb = 25°C, f_{c1k} = 900kHz, unless otherwise stated).

Parameter	Min.	Typ.	Max.	Units	Conditions
ZN447					
Linearity Error	—	—	±¼	LSB	
Differential Linearity Error	—	—	±½	LSB	
Zero Transition	13.5	15	16.5	mV	Moulded 'E' package
(00000000→00000001)	15.0	16.5	18.0	mV	Ceramic 'J'package
Full-scale Transition (11111110→11111111)	2.548	2.550	2.552	V	V_{REF} = 2.560V
ZN448					
Linearity Error	—	—	±½	LSB	
Differential Linearity Error	—	—	±1	LSB	
Zero Transition	12.0	15.0	18.0	mV	Moulded 'E' package
(00000000→00000001)	13.0	16.5	20.0	mV	Ceramic 'J'package
Full-scale Transition (11111110→11111111)	2.545	2.550	2.555	V	V_{REF} = 2.560V
ZN449					
Linearity Error	—	—	±1	LSB	
Differential Linearity Error	—	—	±2	LSB	
Zero Transition	10.0	15.0	20.0	mV	Moulded 'E'package
(00000000→00000001)	11.5	16.5	21.5	mV	Ceramic 'J'package
Full-scale Transition (11111110→11111111)	2.542	2.550	2.558	V	V_{REF} = 2.560V
ALL TYPES					
Resolution	8	—	—	Bits	
Linearity Temperature Coefficient	—	±3.0	—	ppm/°C	
Differential Lienarity Temperature Coefficient	—	±6.0	—	ppm/°C	
Full-scale Temperature Coefficient	—	±2.5	—	ppm/°C	
Zero Temperature Coefficient	—	±8.0	—	µV/°C	
Reference Input Range	1	—	3	V	
Supply Voltage	4.5	5	5.5	V	
Supply Current	—	25	40	mA	
Power Consumption	—	125	—	mW	

ELECTRICAL CHARACTERISTICS (V_{cc} = +5V, Tamb = 25°C, f_{c1k} = 900kHz, unless otherwise stated).

Parameter	Min.	Typ.	Max.	Units	Conditions
COMPARATOR					
Input Current	—	1	—	μA	V_{IN} = +3V, R_{EXT} = 82k
Input Resistance	—	100	—		
Tail Current	25	65	150	μA	V− = −5v
Negative Supply	-3	-5	-30	V	
Input Voltage	-0.5	—	+3.5	V	
ON CHIP REFERENCE					
Output Voltage ZN447	2.530	2.550	2.570		R_{REF} = 390
ZN448	2.520	2.550	2.580	V	
ZN449	2.500	2.550	2.600		C_{REF} = 4μ7
Slope Resistance	—	0.5	2	ohms	
V_{REF} Temperature Coefficient	—	50	—	ppm/°C	
Reference Current	4	—	15	mA	
CLOCK					
On-chip Clock Frequency	—	—	1	MHz	
Clock Frequency Tempco	—	+0.5	—	%/°C	
Clock Resistor	—	—	2.0	kohms	
Maximum External Clock Frequency	—	0.9	1	MHz	
Clock Pulse Width	500	—	—	ns	
High Level Input Voltage V_{IH}	4.0	—	—	V	
Low Level Input Voltage V_{IL}	—	—	0.8	V	
High Level Input Current I_{IH}	—	—	800	μA	V_{IN} = + 4.0 V, V_{CC} = MAX
Low Level Input Current I_{IL}	—	—	−500	μA	V_{IN} = +0.8 V, V_{CC} = MAX
LOGIC (over operating temperature range)					
CONVERT INPUT					
High Level Input Voltage V_{IH}	2	—	—	V	
Low Level Input Voltage V_{IL}	—	—	0.8	V	
High Level Input Current I_{IH}	—	300	—	μA	V_{IN} = +2.4 V, V_{CC} = MAX
Low Level Input Current I_{IL}	—	±10	—	μA	V_{IN} = +0.4 V, V_{CC} = MAX
$\overline{RD}$ INPUT					
High Level Input Voltage V_{IH}	2.0	—	—	V	
Low Level Input Voltage V_{IL}	—	—	0.8	V	
High Level Input Current I_{IH}	—	−150	—	μA	V_{IN} = +2.4V, V_{CC} = MAX
Low Level Input Current I_{IL}	—	−300	—	μA	V_{IN} = +0.4V, V_{CC} = MAX

ELECTRICAL CHARACTERISTICS (V_{cc} = +5V, Tamb = 25°C, f_{c1k} = 900kHz, unless otherwise stated).

Parameter	Min.	Typ.	Max.	Units	Conditions
High Level Output Voltage V_{OH}	2.4	—	—	V	I_{OH} = MAX, V_{CC} = MIN
Low Level Output Voltage V_{OL}	—	—	0.4	V	I_{OL} = MAX, V_{CC} = MIN
High Level Output Current I_{OH}	—	—	-100	μA	
Low Level Output Current I_{OL}	—	—	1.6	mA	
Three-state Disabled Output Leakage	—	—	2	μA	V_{OUT} = +2.0V
Input Clamp Diode Voltage	—	—	-1.5	V	
$\overline{RD}$ Input to Data Output Enable/Disable	—	180	250	ns	
Delay Times T_{E1}	180	210	260	ns	
T_{E0}	60	80	100	ns	
T_{D1}	80	110	140	ns	
T_{D0}	60	80	100	ns	
Convert Pulse Width $T_{\overline{WR}}$	200	—	—	ns	
$\overline{WR}$ Input to $\overline{BUSY}$ Output	—	—	250	ns	
Propagation Delay T_{BD}	—	—	—	—	

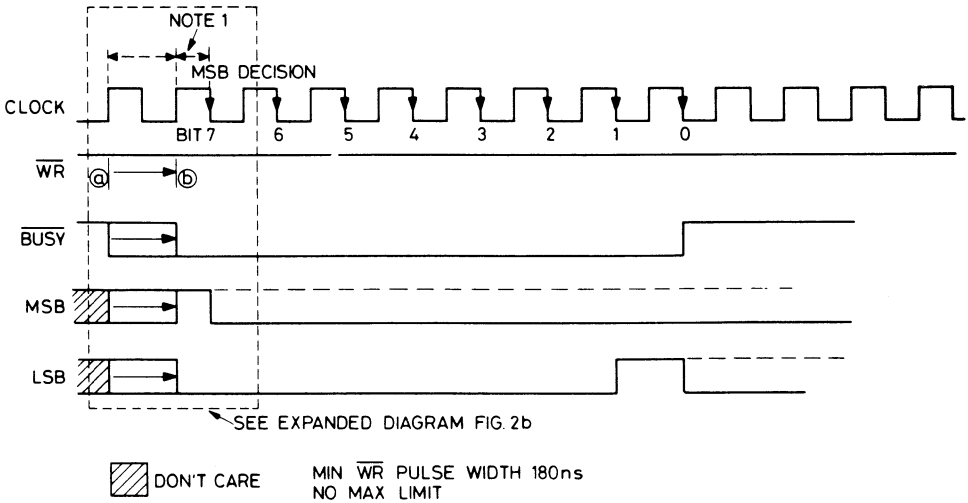
GENERAL CIRCUIT OPERATION

The ZN447 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{WR}$ input the $\overline{BUSY}$ output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF/2}$ from the DAC. This is compared to the input voltage V_{IN}; a decision is made on the next negative clock edge to reset the MSB to 0 if $\frac{V_{REF}}{2}$ V_{IN} or leave it set to 1 if $\frac{V_{REF}}{2}$ V_{IN}. Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2}$ + $\frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to V_{IN} and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the eighth negative clock edge $\overline{BUSY}$ goes high indicating that the conversion is complete.

During a conversion the $\overline{RD}$ input will normally be held high to keep the 3-state buffers in their high impedance state. Data can be read out by taking $\overline{RD}$ low, thus enabling the 3-state outputs. Readout is non-destructive.

CONVERSION TIMING

The ZN447 will accept a low-going CONVERT pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 7½ and 8½ clock pulses later depending on the relative timing of the clock and CONVERT signals. Timing diagrams for a conversion are shown in figure 2.



NOTE 1. GUARANTEED PERIOD OF ½ CLOCK CYCLE MIN. 1½ CLOCK CYCLES MAX. ALLOWS MSB TO SETTLE BEFORE MSB DECISION

FIG. 2a

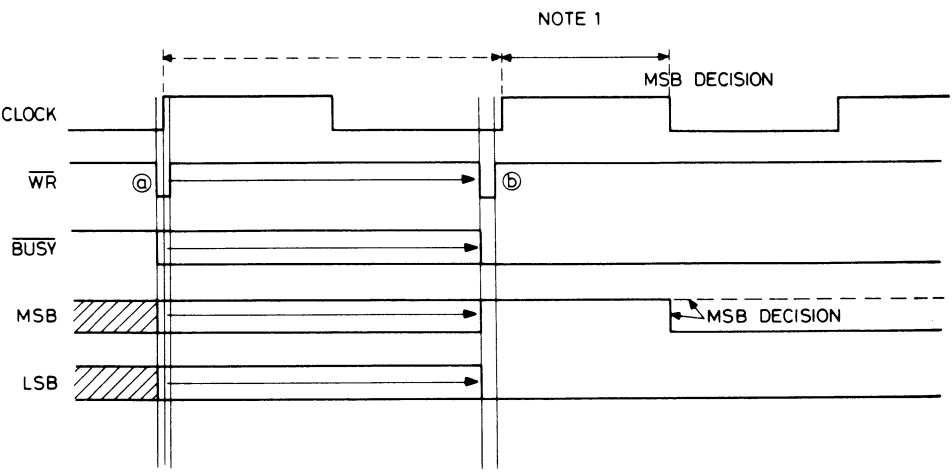


FIG. 2b (EXPANDED INSET)

6554

Fig. 2 ZN447 TIMING DIAGRAMS

The converter is cleared by a low-going CONVERT pulse, which sets the most significant bit and resets all the other bits and the $\overline{\text{BUSY}}$ flag. Whilst the CONVERT input is low the MSB output of the DAC is continuously compared with the analogue input, but otherwise the converter is inhibited.

After the CONVERT input goes high again the MSB decision is made and the successive approximation routine runs to completion.

The CONVERT pulse can be as short as 200ns; however the MSB must be allowed to settle for at least 550ns before the MSB decision is made. To ensure that this criterion is met even with short CONVERT pulses the converter waits, after the CONVERT input goes high, for a rising clock edge followed by a falling clock edge, the MSB decision being taken on the falling clock edge. This ensures that the MSB is allowed to settle for at least half a clock period, or 550ns at maximum clock frequency. The CONVERT input is not locked out during a conversion and if it is pulsed low at any time the conversion will restart.

The $\overline{\text{BUSY}}$ output goes high at the end of a conversion indicating data valid. Note that if the three-state data outputs are enabled during a conversion then valid data will be available at the outputs on the rising edge of the $\overline{\text{BUSY}}$ signal. If, however the outputs are not enabled until after $\overline{\text{BUSY}}$ goes high then the data will be subject to the propagation delay of the three-state buffers. (See under DATA OUTPUTS).

CONTINUOUS CONVERSION

If a free-running conversion is required then the converter can be made to cycle by inverting the $\overline{\text{BUSY}}$ output and feeding it to the CONVERT input. To ensure that the converter starts reliably after power up an inital start pulse is required. This can be ensured by using a NOR gate instead of an inverter and feeding it with a positive going pulse which can be derived from a simple RC network that gives a single pulse when power is applied, as shown in figure 3a.

The ADC will complete a conversion on every eighth clock pulse, with the $\overline{\text{BUSY}}$ output going high for a period determined by the propagation delay of the NOR gate, during which time the data can be stored in a latch. The time available for storing the data can be increased by inserting delays into the inverter path.

A timing diagram for the continuous conversion mode is shown in figure 3b.

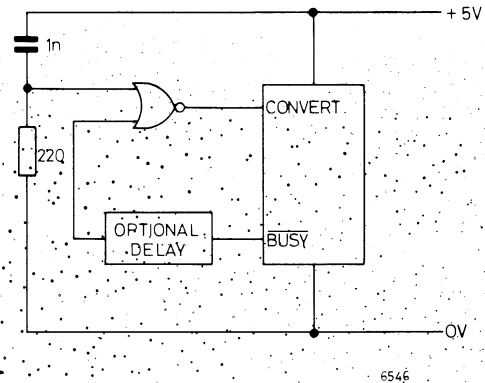


Fig. 3a CIRCUIT FOR CONTINUOUS CONVERSION

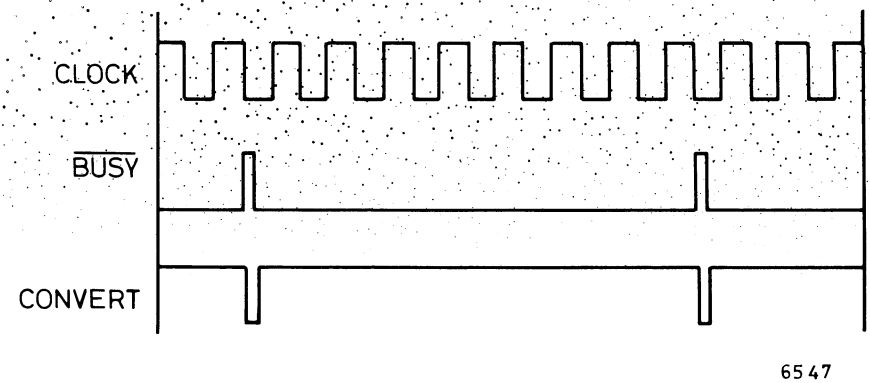


Fig. 3b TIMING FOR CONTINUOUS CONVERSION

As the $\overline{\text{BUSY}}$ output uses a passive pullup the rise time of this output depends on the RC time constant of the pullup resistor and load capacitance. In the continuous conversion mode the use of a 4k7 external pullup resistor is recommended to reduce the risetime and ensure that a logic 1 level is reached.

DATA OUTPUTS

The data outputs are provided with 3-state buffers to allow connection to a commmon data bus. An equivalent circuit is shown in figure 4. Whilst the $\overline{\text{RD}}$ input is high both ouput transistors are turned off and the ZN447 presents only a high impedance load to the bus. When $\overline{\text{RD}}$ is low the data ouputs will assume the logic states present at the outputs of the successive approximation register.

A test circuit and timing diagram for the output enable/disable delays are given in figure 5.

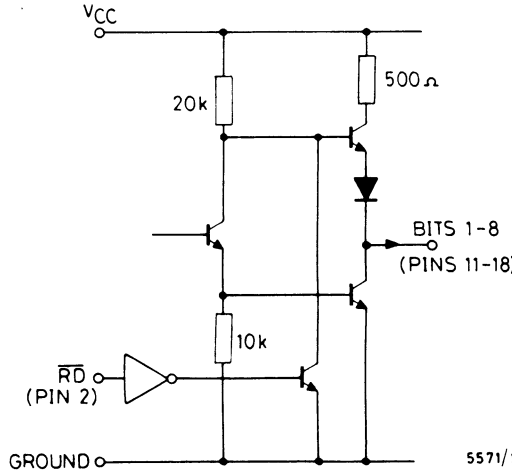
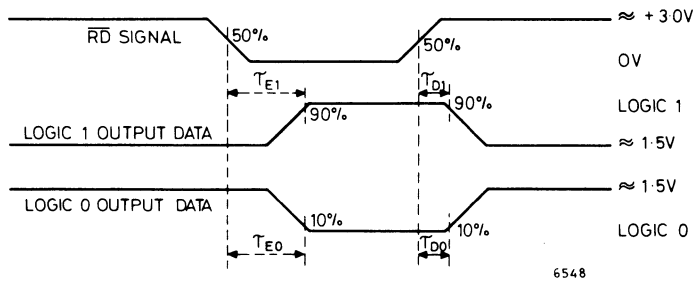


Fig. 4 DATA OUTPUT



OUTPUT LOAD

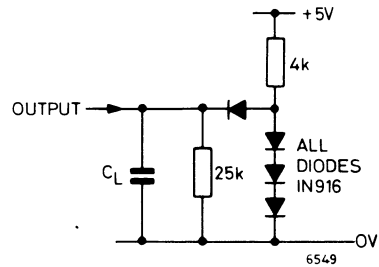


Fig. 5 OUTPUT ENABLE/DISABLE DELAYS

$\overline{\text{BUSY}}$ OUTPUT

The $\overline{\text{BUSY}}$ output, shown in figure 6, utilises a passive pullup for CMOS/TTL compatibility. This also allows up to four $\overline{\text{BUSY}}$ outputs to be wire-ANDed together to form a common interrupt line.

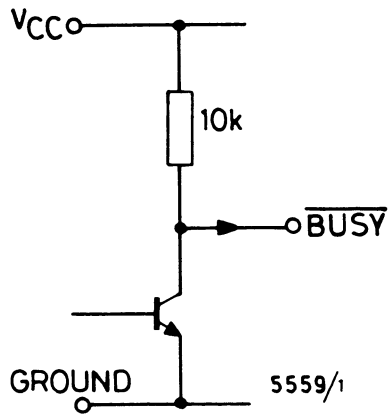


Fig. 6 $\overline{\text{BUSY}}$ OUTPUT

ON-CHIP CLOCK

The on-chip clock operates with only a single external capacitor connected between pin 3 and ground as shown in figure 7a. A graph of typical oscillator frequency versus capacitance is given in figure 8. The oscillator frequency may be trimmed by means of an external resistor in series with the capacitor, as shown in figure 7b. For optimum accuracy and stability of the oscillator frequency without trimming the use of a crystal or ceramic resonator is recommended, as shown in figure 7c. The final option is to overdrive the oscillator input with an external clock signal from a TTL or CMOS gate, as shown in figure 7d.

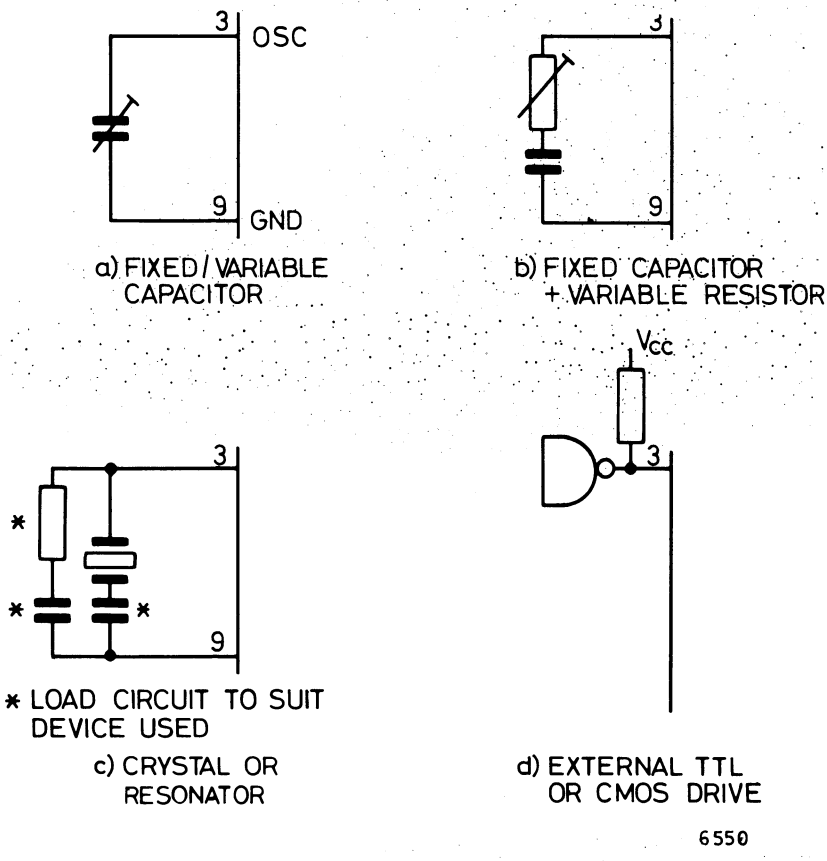


Fig. 7 CLOCK CIRCUIT EXTERNAL COMPONENTS

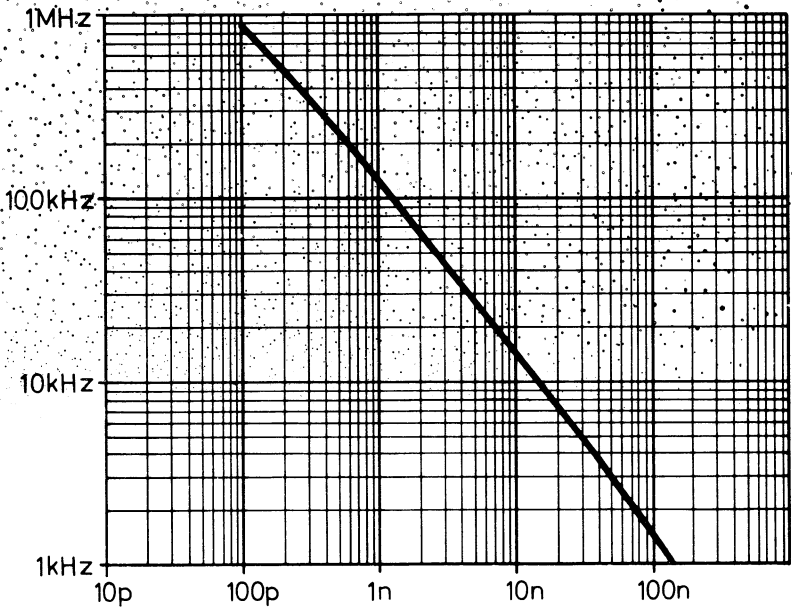


Fig. 8 TYPICAL CLOCK FREQUENCY vs. C_{CR} (R_{CK} = 0)

ANALOGUE CIRCUITS

D to A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in figure 9. Each element is connected to either OV or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1 millivolt).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$\text{D to A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D to A from the successive approximation register.

V_{OS} is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (8 μV/°C) the effect on accuracy will be negligible.

The D to A output range can be considered to be $0-V_{REF\ IN}$ through an output resistance R (4k).

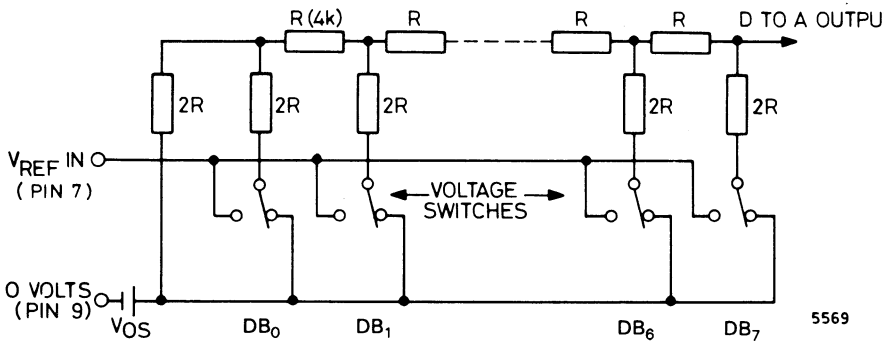


Fig. 9 R2-R LADDER NETWORK

REFERENCE

(a) Internal Reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (figure 10). A resistor (R_{REF}) should be connected between pins 8 and 10.

The recommmended value of 390Ω will supply a nominal reference current of (5.0−2.5) /0.39 = 6.4mA. A stabilising/decoupling capacitor, C_{REF} (4 μ7), is required between pins 8 and 9. For internal reference operation $V_{REF\ OUT}$ (Pin 8) is connected to $V_{REF\ IN}$ (Pin 7).

Up to five ZN447s may be driven from one internal reference, there being no need to reduce R_{REF}. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 3mA.

(b) External Reference

If required an external reference voltage in the range +1.5 to +3.0 volts may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

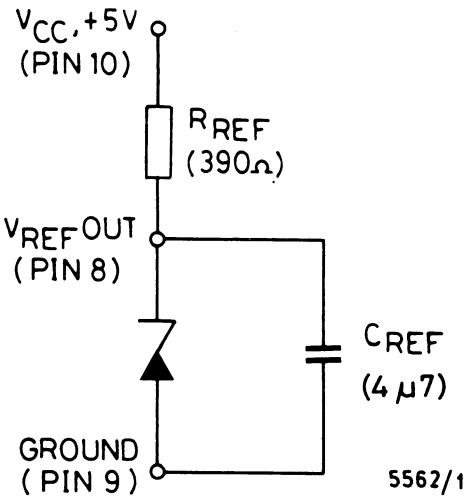


Fig. 10 INTERNAL VOLTAGE REFERENCE

RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN447 should be derived from the same supply. The external reference can vary from +1.5 volts to +3.0 volts. The ZN447 will operate if $V_{REF\ IN}$ is less than +1.5 volts but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

COMPARATOR

The ZN447 contains a fast comparator, the equivalent input circuit of which is shown in figure 11. A negative supply voltage is required to supply the tail current of the comparator. However as this is only 25 to 150 μA and need not be well stabilised it can be supplied by a simple diode pump circuit driven from the $\overline{BUSY}$ output.

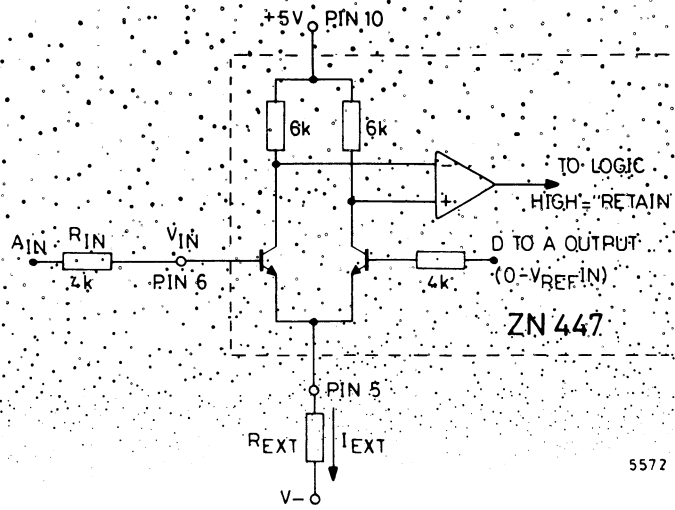


Fig. 11 COMPARATOR EQUIVALENT CIRCUIT

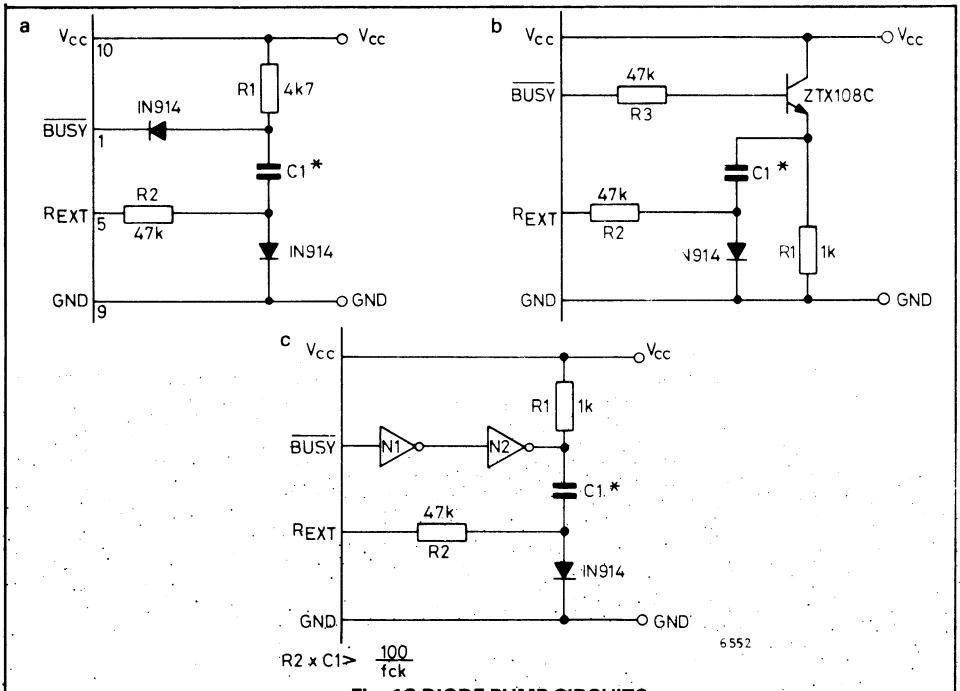


Fig. 12 DIODE PUMP CIRCUITS TO SUPPLY COMPARATOR TAIL CURRENT

Several suitable circuits are shown in figure 12. The principle of operation is the same in each case. Whilst the $\overline{BUSY}$ output is high capacitor C1 is charged to about 4.—4.5 volts. During a conversion the $\overline{BUSY}$ output goes low and the upper end of C1 is thus also pulled low. The lower end of C1 therefore applies about —4V to R2, thus providing the tail current for the comparator. The time constant R2. C1 is chosen according to the clock frequency so that droop of the capacitor voltage is not significant during a conversion.

The constraint on using this type of circuit is that C1 must be recharged whilst the $\overline{BUSY}$ output is high. If the $\overline{BUSY}$ output is high for greater than one converter clock period then the circuit of figure 12a will suffice. If this is not the case, for example, in the continuous conversion mode, then the circuits of figures 12b and 12c are recommended, since these can pump more current into the capacitor.

Where several ZN447s are used in a system the self-oscillating diode pump circuit of figure 13 is recommended. Alternatively, if a negative supply is available in the system then this may be utilised. A list of suitable resistor values for different supply voltages is given in table 1.

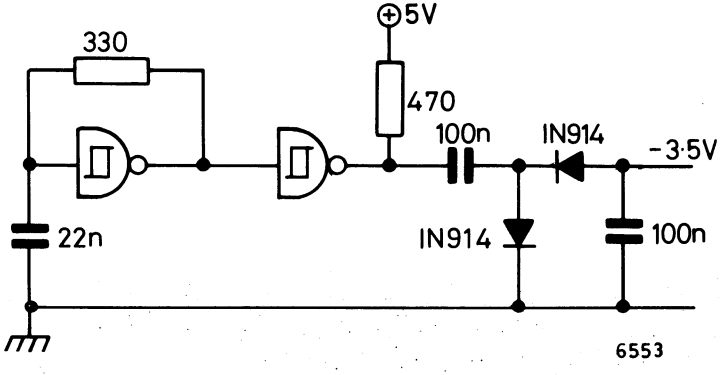


Fig. 13 DIODE PUMP CIRCUIT TO SUPPLY COMPARATOR TAIL CURRENT FOR UP TO FIVE ZN447's.

V– (Volts)	R_{EXT} (k~)
3	47
5	82
10	150
12	180
15	220
20	330
25	390
30	470

ANALOGUE INPUT RANGES

The basic connection of the ZN447 shown in figure 14 has an analogue input range 0 to $V_{REF\ IN}$ which, in some applications, may be made available from previous signal conditioning /scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by offsetting the analogue input range so that the comparator always sees a positive input voltage.

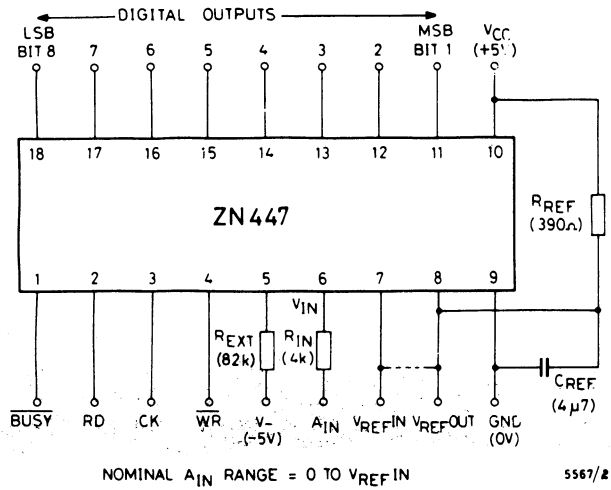


Fig. 14 EXTERNAL COMPONENTS FOR BASIC OPERATION

UNIPOLAR OPERATION

The general connection for unipolar operation is shown in figure 15.
The values of R_1 and R_2 are chosen so that $V_{IN} = V_{REF\ IN}$ when the Analogue Input (A_{IN}) is at full scale.

The resulting full scale range is given by: $A_{IN}\ FS = (1 + \frac{R1}{R2}),\ V_{REF\ IN} = G.\ V_{REF\ IN}$.

To match the ladder resistance R1/R2 (R_{IN}) = 4k.

The required nominal values of R_1 and R_2 are given by $R_1 = 4G$ k, $R_2 = \frac{4G}{G-1}$ k.

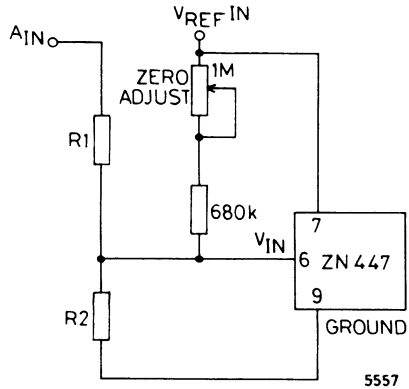


Fig. 15 GENERAL UNIPOLAR INPUT CONNECTIONS

Using these relationships a table of nominal values of R_1 and R_2 can be constructed for $V_{REF\ IN}$ = 2.5 volts.

INPUT RANGE	G	R_1	R_2
+5V	2	8k	8k
+10V	4	16k	5.33k

GAIN ADJUSTMENT

Due to tolerances in R_1 and R_2, tolerances in V_{REF} and the gain (full-scale) error of the DAC, some adjustment should be incorporated into R_1 to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting R_1 by at least ± 5% of its nominal value is suggested.

ZERO ADJUSTMENTS

Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 1.5mV applied to the comparator input, which corresponds to 1½ LSB with a 2.56 volt reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of + ½ LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than 1½ times $V_{REF\ IN}$.

Practical circuit values for +5V and +10V input ranges are given in figure 16 which incorporates both zero and gain adjustments.

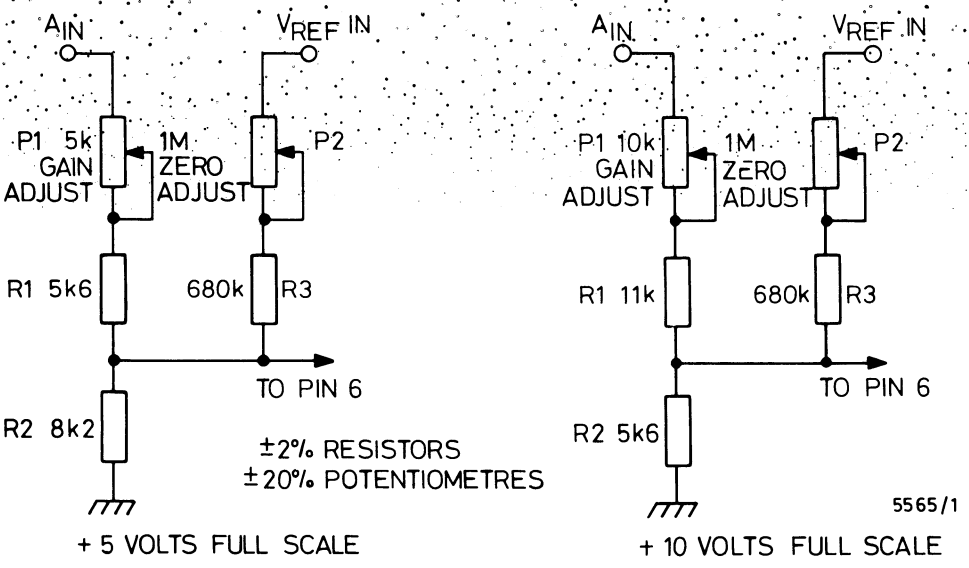


Fig. 16 UNIPOLAR OPERATION COMPONENT VALUES

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous convert pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply full scale minus 1½ LSB to A_{IN} and adjust gain until Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 1.

(iii) Apply ½ LSB to A_{IN} and adjust zero until Bit 8 just flickers between 0 and 1 with all other bits at 0.

UNIPOLAR SETTING – UP POINTS

INPUT RANGE, + FS	½ LSB	FS – 1½ LSB
+5V	9.8mV	4.9797 volts
+10V	19.5mV	9.9414 volts

$1\,LSB = \frac{FS}{256}$

UNIPOLAR LOGIC CODING

ANALOGUE INPUT (A_{IN}) (NOMINAL CODE CENTRE VALUE)	OUTPUT CODE (BINARY)
FS – 1 LSB	11111111
FS – 2 LSB	11111110
¾ FS	11000000
½ FS + 1 LSB	10000001
½ FS	10000000
½ FS – 1 LSB	01111111
¼ FS	01000000
1 LSB	00000001
0	00000000

BIPOLAR OPERATION

For bipolar operation the input to the ZN447 is offset by half full scale by connecting a resistor R_3 between $V_{REF\,IN}$ and V_{IN} (figure 17).

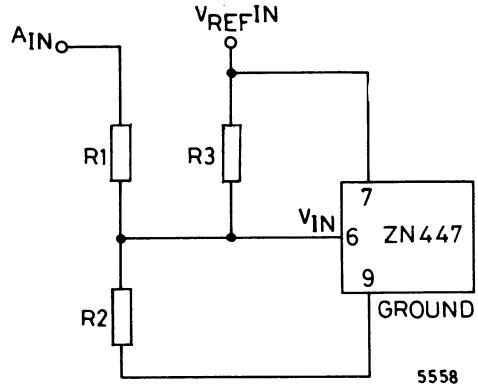


Fig. 17 BASIC BIPOLAR INPUT CONNECTION

When $A_{IN} = -FS$, V_{IN} needs to be equal to zero.

When $A_{IN} = +FS$, V_{IN} needs to be equal to $V_{REF\ IN}$.

If the full scale range is $\pm$ G. $V_{REF\ IN}$ then $R_1 = (G-1)$. R_2 and $R_1 = G$. R_3 fulfil the required conditions.

To match the ladder resistance $R_1/R_2/R_3$ ($= R_{IN}$) = 4k.

Thus the nominal values of R_1, R_2, R_3 are given by $R_1 = 8\,Gk$, $R_2 = 8G/(G-1)k$, $R_3 = 8k$.

A bipolar range of $\pm$ $V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) results if $R_1 = R_3 = 8k$ and $R_2 = \infty$.

Assuming the $V_{REF\ IN}$ = 2.5 volts the nominal values of resistors for $\pm$ 5V and $\pm$ 10V input ranges are given in the following table.

INPUT RANGE	G	R_1	R_2	R_3
$\pm$5V	2	16k	16k	8k
$\pm$10V	4	32k	10.66k	8k

Minus full scale (offset) is set by adjusting R_1 about its nominal value relative to R_3. Plus full scale (gain) is set by adjusting R_2 relative to R_1.
Practical circuit realisations are given in figure 18.

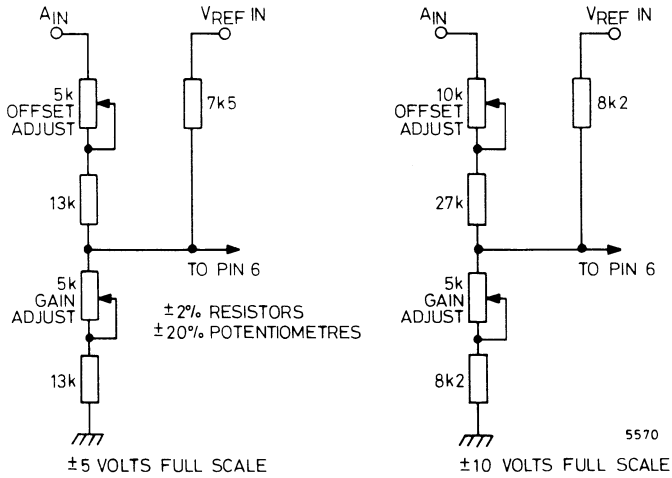


Fig. 18 BIPOLAR OPERATION—COMPONENT VALUES

Note that in the ± 5V case R_3 has been chosen as 7.5 k (instead of 8.2 k) to obtain a more symmetrical range of adjustment using standard potentiometers.

BIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.
(ii) Apply − (FS − ½ LSB) to A_{IN} and adjust offset until the Bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.
(iii) Apply + (FS − 1½ LSB) to A_{IN} and adjust gain until Bit 8 just flickers between 0 and 1 with all other bits at 1.
(iv) Repeat step (ii).

BIPOLAR SETTING—UP POINTS

INPUT RANGE, ± FS	−(FS − ½ LSB)	+ (FS − 1½ LSB)
±5V	−4.9805V	+4.9414V
±10V	−9.9609V	+9.8828V

1 LSB = $\frac{2FS}{256}$

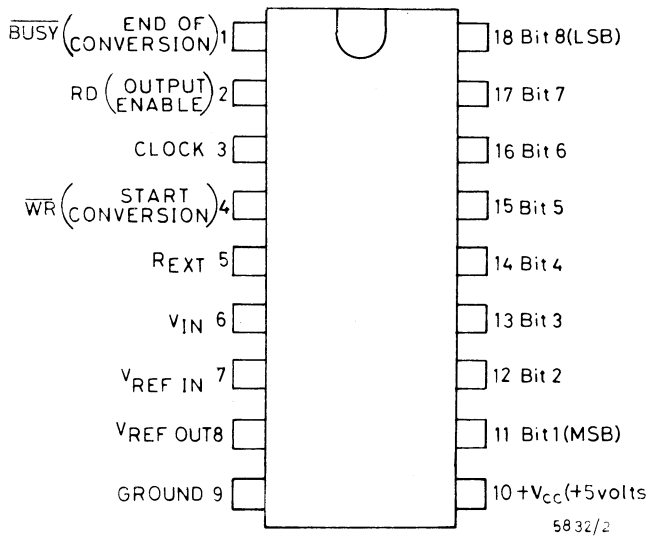
BIPOLAR LOGIC CODING

ANALOGUE INPUT (A_{IN}) (NOMINAL CODE CENTRE VALUE)	OUTPUT CODE (OFFSET BINARY)
+ (FS − 1 LSB)	11111111
+ (FS − 2 LSB)	11111110
+ ½ FS	11000000
+ 1 LSB	10000001
0	10000000
− 1 LSB	01111111
− ½ FS	01000000
− (FS − 1 LSB)	00000001
− FS	00000000

ORDERING INFORMATION

TYPE	LINEARITY (LSB)	OPERATING TEMPERATURE RANGE	PACKAGE
ZN447E	¼	0°C to + 70°C	Moulded
ZN447J	¼	−55°C to + 125°C	Ceramic
ZN448E	½	0°C to + 70°C	Moulded
ZN448J	½	−55°C to + 125°C	Ceramic
ZN449E	1	0°C to + 70°C	Moulded
ZN449J	1	−55°C to + 125°C	Ceramic

PIN CONNECTIONS



FERRANTI semiconductors

ZN450E
ZN450CJ

Single Chip 3½ Digit DVM IC

FEATURES

- **199.9 mV full-scale reading**
- **Digital Auto-zero with guaranteed zero reading for 0V input**
- **True polarity at zero for null detection**
- **True differential inputs**
- **Direct drive of Liquid Crystal Display**
- **On-chip clock and precision reference**
- **Underrange/overrange indication**
- **Low power consumption, less than 35 mW**
- **Wide supply voltage range, single supply rail**
- **No external active circuits required**

DESCRIPTION

The ZN450 is a complete digital voltmeter fabricated on a monolithic chip and requires only ten external, passive components for operation. A novel charge-balancing conversion technique ensures good linearity. The auto-zero function is completely digital in operation, thus obviating the need for a capacitor to store the error voltage. This versatile I.C. can be used as the basis not only for digital voltmeters and multimeters but also for other instruments such as digital thermometers.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}	−0.5 to +7 volts
Maximum Voltage, all other inputs	−0.5 to (V_{CC} +0.5) volts
Operating Temperature range	0 to +70°C
Storage Temperature Range	−55°C to +125°C

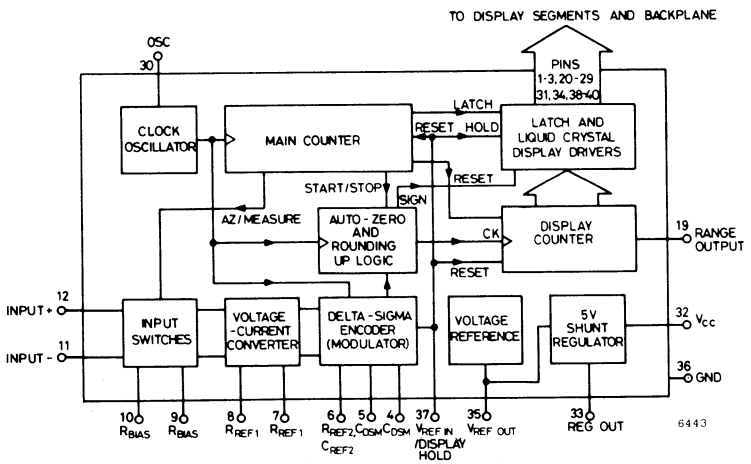


Fig. 1 – ZN450 SYSTEM DIAGRAM

Parameter	Min.	Typ.	Max.	Units	Conditions
Full-scale Reading	−1999	—	+1999		
Zero Reading	−000.0	±000.0	+000.0	Digital Reading	$V_{IN}=0$, $V_{FS}=200\,mV$
Rollover Error	−2	0	+2	Count	$-V_{IN}=+V_{IN}=\pm 200\,mV$ conversion time ≥0.5 sec.
Linearity	−1	0	+1	Count	$V_{FS}=200\,mV$ conversion time ≥0.5 sec.
Common Mode Range	1.8	–	3.8	Volts	
Common Mode Rejection	—	120	—	μV/V	
Supply Rejection	—	100	—	μV/V	
Input Offset Current	—	0.1	1	nA	Input bias resistors matched to 0.1%
Input Resistance	7	10	13	MΩ	With 10 M input resistors
Zero Temperature Coefficient	—	—	1	μV/°C	
Full-scale Temperature Coefficient	Determined by tracking of external resistors				Ref T.C. = 0 ppm/°C
Oscillator Frequency Range	—	—	300	kHz	
Conversion Time (48000 Oscillator Periods)	0.25	—	—	Seconds	
VOLTAGE REFERENCE Output Voltage	1.26	1.3	1.35	Volts	
Temperature Coefficient	—	50	80	ppm/°C	
Knee Current	—	—	150	μA	
Maximum Sink Current	1	2	—	mA	
SUPPLY VOLTAGE (a) Direct (b) Using on-chip Shunt Regulator (c) Using external NPN transistor (d) Using two transistor regulator	 4.5 6.0 6.5 5.5	 5 — — —	 5.5 — — —	 Volts Volts Volts Volts	
Supply Current	—	4	6.5	mA	
SHUNT REGULATOR Output Voltage Sink Current	 4.5 —	 5 —	 5.5 15	 Volts mA	
DISPLAY OUTPUTS Peak Voltage	—	$\pm V_{CC}$	—		
D.C. Component	—	—	±25	mV	
Backplane Frequency	—	$\frac{1}{2000}$	—	Oscillator Frequency	

GENERAL DESCRIPTION

The ZN450 utilises a charge-balancing conversion principle, which offers a number of advantages over the more common dual-slope integration method.

These include a fixed conversion time which is independent of the analogue input voltage, completely digital auto-zero and inherently bipolar operation. Linearity is also extremely good over the entire input voltage range, unlike some dual slope designs where stray capacitance can cause problems around zero.

The conversion time of the ZN450 is divided into two periods, measure and auto-zero, unlike the dual-slope system which has three distinct phases, signal integrate, reference integrate and auto-zero.

The heart of the ZN450 is the delta-sigma encoder, a simplified circuit of which is shown in figure 2.

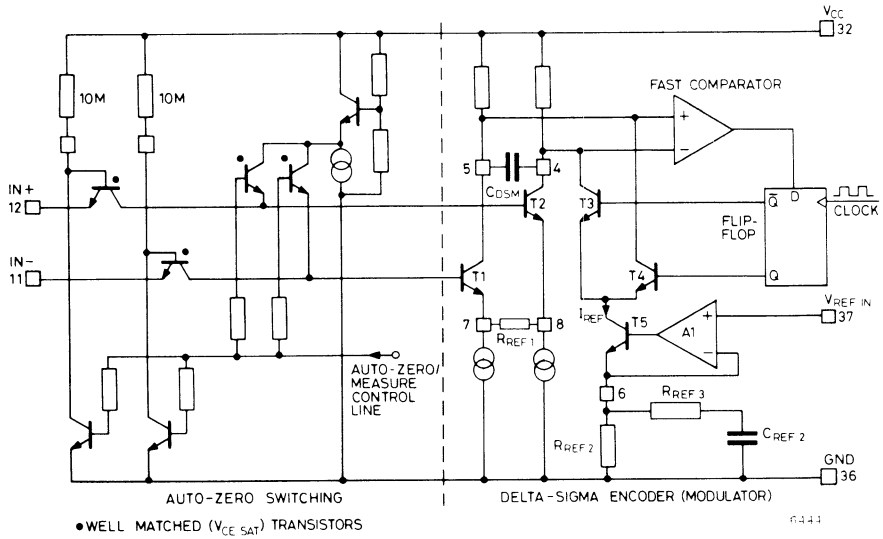


Fig. 2 – INPUT SWITCHING AND DELTA-SIGMA ENCODER

The delta-sigma encoder of the ZN450 consists of a voltage-current converter comprising T1 and T2, a reference current generator A1/T5 and a feedback loop containing a fast comparator, D-type flip-flop and current switches T3 and T4. These can switch a current $I_{REF} = \frac{V_{REF}}{R_{REF2}}$ into the collector circuit of either T1 or T2, depending on the state of the flip-flop.

The polarity of the voltage across capacitor C_{DSM} is monitored by the comparator, whose output is sampled on every clock pulse by the flip-flop. The outputs of the flip-flop switch I_{REF} into the collector circuit of either T1 or T2 so as to oppose the existing voltage on C_{DSM} i.e. to maintain the average charge acquired by C_{DSM} at zero, thus keeping the circuit in equilibrium.

Assuming perfect symmetry in the circuit, with zero volts applied between the bases of T_1 and T_2 their collector currents will be equal, and the only charge acquired by C_{DSM} will be that put on it by I_{REF}. The flip-flop will thus change state on every clock pulse so that C_{DSM} will alternately acquire charge quanta of $+I_{REF}T_C$ and $-I_{REF}T_C$ (where T_C is the clock period) and the nett charge acquired will be zero. The output of the flip-flop will thus be a square-wave with a 50% duty cycle.

During the measurement phase the voltage to be measured is applied between the bases of T1 and T2 and is converted into a current $I_{IN} = \frac{V_{IN}}{R_{REF1}}$ flowing in R_{REF1}. This produces a difference current $2I_{IN}$ in the collector currents of T1 and T2, so that the charge acquired by C_{DSM} is no longer equal and opposite ($\pm I_{REF}$) but is now ($I_{REF} - 2I_{IN}$) T_C when T_4 is turned on and ($-I_{REF} - 2I_{IN}$) T_C when T3 is turned on.

In order to maintain equilibrium the flip-flop will now no longer change state on every clock pulse but will remain in one state for a longer period than it remains in the opposite state.

$$\text{i.e. } N_1T_C(I_{REF} - 2I_{IN}) + (N - N_1)T_C\,(-I_{REF} - 2I_{IN}) = 0$$

where N_1 is the number of clock pulses for which the flip-flop output is a '1' and N is the total number of clock pulses over which the measurement is made and assuming N is so large that quantising error can be ignored.

$$\text{Thus } N_1(I_{REF} - 2I_{IN}) = (N - N_1)(I_{REF} + 2I_{IN})$$

At this point it is perhaps worth noting that the DSM saturates (0% or 100% duty cycle) when I_{IN} is plus or minus $\frac{I_{REF}}{2}$.

In order to provide an overload margin for series mode rejection the ZN450's DSM operates with a peak duty-cycle of nominally 10% for minus full-scale and 90% for plus full-scale ($I_{IN} = \pm\frac{2}{5}I_{REF}$) giving an overload margin of 25% of the full-scale input voltage.

$$\text{Now } \frac{2N_1 - N}{N} = \frac{2I_{IN}}{I_{REF}} \quad \text{i.e. } N_1 - \frac{N}{2} = \frac{NI_{IN}}{I_{REF}} = \frac{NV_{IN}\,R_{REF2}}{R_{REF1}\,V_{REF}}$$

What this means is that an up counter preset to $-\frac{N}{2}$ and allowed to count N_1 will accumulate a number proportional to V_{IN}, assuming N, R_{REF1}, R_{REF2} and V_{REF} are fixed. By suitable choice of these parameters $N_1 - \frac{N}{2}$ can be made directly equal to V_{IN} in volts or millivolts. Furthermore, by making the preset number greater or less than $\frac{N}{2}$ in proportion to any zero error in the system it is possible to provide a digital auto-zero.

The ZN450 indicates positive overrange at a count of +2000 when the duty cycle is 90% and $I_{IN} = \frac{2}{5}I_{REF}$. The required value of N can thus be obtained by substituting the overrange reading of 2000 for $N_1 - \frac{N}{2}$ and the corresponding value of $\frac{2}{5}$. for $\frac{I_{IN}}{I_{REF}}$, $2000 = \frac{2N}{5}$, $N = 5000$.

In fact the display counter is preceded by a ÷4 stage which is part of the auto-zero logic so the actual measurement period must be 20,000 clock periods to give a maximum of 5000 pulses at the display counter.

The display counter of the ZN450 can count from −5000 to +5000. It is preset to nominally −2500 during the auto-zero phase by allowing it to count from −5000 to −2500, as explained below.

Auto-Zero

Due to offsets and component mismatching in the delta-sigma encoder the displayed count accumulated for zero input voltage will not be zero. In order to remove this error and give a true zero reading for 0V input the ZN450 incorporates an auto-zero facility. This is completely digital in operation and there is no need to store the error as an analogue voltage on a capacitor, as is the case with some dual slope-designs. Furthermore the conversion period of the ZN450 comprises two well-defined phases, measure and auto-zero, unlike dual-slope DVMs which have signal integrate, reference integrate and auto-zero phases.

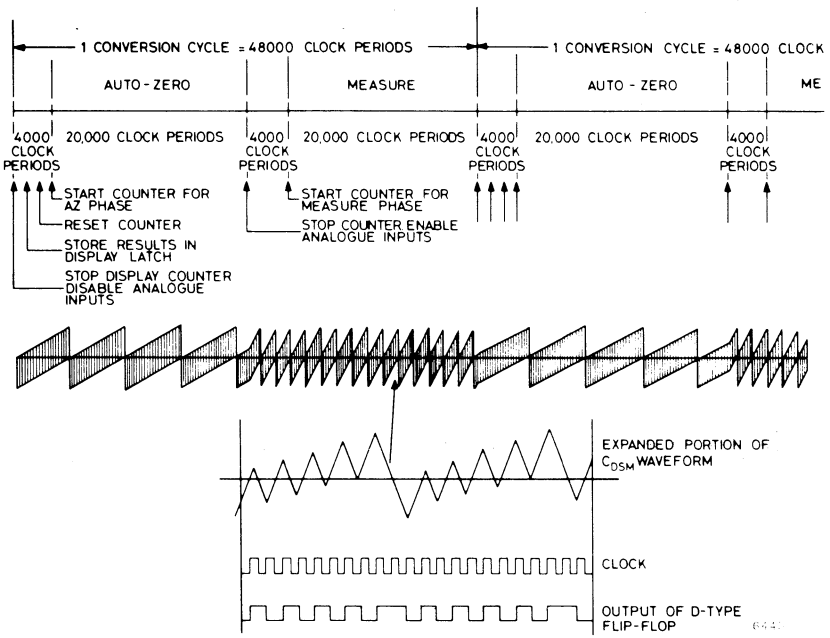


Fig. 3 – TIMING DIAGRAM OF ZN450

A timing diagram of the ZN450 is shown in figure 3. Its duration is 48000 clock periods and its two principal components are the measurement phase and the auto-zero phase which each occupy 20,000 clock periods. Each phase is separated by a space of 4000 clock periods to allow the input switches to settle. This also illustrates another advantage of the charge balancing conversion technique. Since the delta sigma encoder can run continuously without saturating and its average duty-cycle is always a measure of the input voltage, it is possible to allow the input switches to settle in this way before starting a measurement by activating the system counters.

Contrast this with the dual-slope DVM where the integrator capacitor begins to accumulate charge immediately the input voltage is connected. The system counter must start at the precise instant that the input voltage is connected which means that the input switches must be fast and noise-free. Furthermore termination of the measurement is determined by the comparator accurately detecting a single zero-crossing, so noise in the comparator or from other sources can cause errors. In the charge balancing DVM the comparator detects many zero crossings and noise tends to be integrated out.

Operation of the auto-zero system is best understood by considering what happens when an auto-zero phase is followed by a measurement with zero volts input. During the auto-zero phase the inputs of the DSM are disconnected from the analogue inputs and shorted to a point within common-mode range of the DVM. The counter is reset to -5000 and the system is allowed to run for 20,000 clock periods, but with the DSM output inverted. This means that the number of clock pulses counted will be, not N_1 but $(N - N_1)$. During the subsequent measurement with zero input voltage N_1 pulses will be counted, so that the total count will be N, i.e. 5000. The display counter will thus have counted from -5000 up to zero and zero will be displayed.

Due to the quantising error inherent in any digital measurement it is possible that the result of the measurement with zero input could differ from the result of the auto-zero by 1 count, thus giving rise to a zero error of ±1 digit. To avoid this problem the ZN450 incorporates two guard bits in the form of a ÷4 stage and rounding up logic preceding the display counter. This means that although the display resolution is 1 part in ±2000 the resolution of the measurement is four times better. Any zero error in the two (non-displayed) guard bits will not appear in the display and the logic also subdivides the zero state into +0000 and −0000 for true polarity indication.

As an additional benefit flicker in the last digit of the display is minimised.

Input Resistance

The input resistance of the ZN450 is determined by the two 10M bias resistors, the value of R_{REF1}, and h_{fe} and r_e of T1 and T2.

An equivalent input circuit is shown in figure 4. The input resistance comprises h_{fe} $(R_{REF1} + 2_{re})$ in parallel with 20M due to the two 10M input resistors.

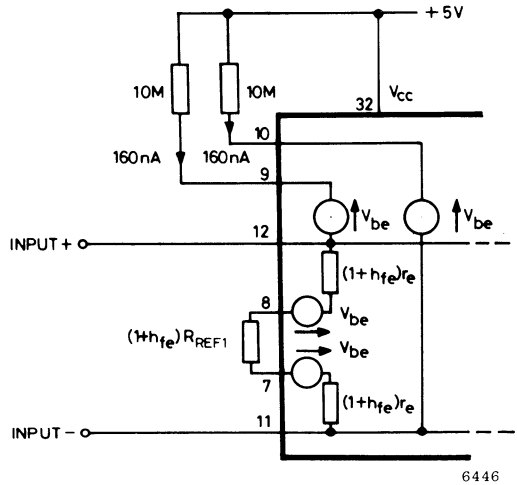


Fig. 4 – EQUIVALENT INPUT CIRCUIT OF ZN450

The h_{fe} of T1 and T2 is typically about 100 and r_e is around 2.5k, therefore:

$$R_{IN} = \frac{100\,(R_{REF1} + 5k) \times 20M}{100\,(R_{REF1} + 5k) + 20M}$$

For 200 mV full-scale, when $R_{REF1} = 200k$ the input resistance is around 10M.

Reference Loop and Supply Regulator

The reference current defining loop is shown in more detail in figure 5.

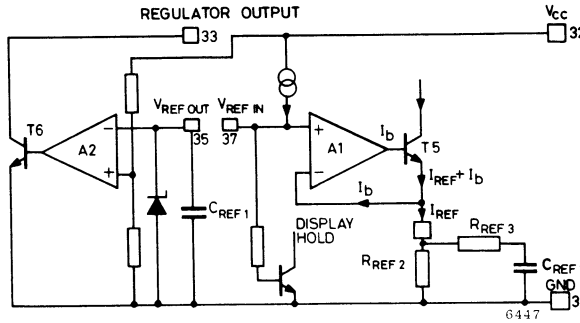


Fig. 5 – REFERENCE CURRENT LOOP AND SUPPLY REGULATOR

A reference input voltage applied to the non-inverting input of A1 causes the output of A1 to bias T5 such that the inverting input of A1 assumes the same potential and a current $\frac{V_{REF\ IN}}{R_{REF2}}$ flows in R_{REF2}. By making the input bias current of A1 the same as the base current of T5 this base current flows into the inverting input of A1 instead of through R_{REF2}. The reference current flowing in the collector of T5 is therefore almost identical to the current flowing in R_{REF2}. The reference loop is stabilized by C_{REF2} and R_{REF3}.

A highly stable on-chip bandgap reference of approximately 1.28V is provided and this may be used by linking $V_{REF\ OUT}$ to $V_{REF\ IN}$ when the reference will be biased on by the 150 μA current source connected to the non-inverting input of A1. The on-chip reference is stabilised by C_{REF1}. The on-chip reference also provides the reference voltage for the on-chip supply regulator A2. This compares V_{REF} against $\frac{V_{CC}}{4}$ and controls V_{CC} with transistor T6 such that the two are kept equal, i.e. $V_{CC} \simeq 5V$.

The supply regulator can be configured as a shunt or series regulator using only a few external components.

If $V_{REF\ OUT}$ is not connected to $V_{REF\ IN}$ but supply regulation is still required then the on-chip reference must be biased on by a 22k resistor to V_{CC}.

Setting Full-Scale Range

The described equation previously arrived at for the charge-balancing converter was:

$$\frac{NV_{IN}.R_{REF2}}{V_{REF}.R_{REF1}} = N_1 - \frac{N}{2}$$

i.e. displayed reading $= \frac{NV_{IN}.R_{REF2}}{V_{REF}.R_{REF1}}$

and since N = 5000

Displayed reading $= 5{,}000\ \frac{V_{IN}.R_{REF2}}{V_{REF}.R_{REF1}}$

or, substituting the maximum reading of ± 1999 and rearranging again:

V_{IN}(full-scale) $= \frac{\pm 1999\,V_{REF}.R_{REF1}}{5000.R_{REF2}}$

$\simeq \frac{\pm 0.4\,V_{REF}.R_{REF1}}{R_{REF2}}$

These equations are in fact not exact since they do not take account of the reference amplifier offset

voltage, which is typically ±5mV. This offset means that I_{REF} is not precisely $\frac{V_{REF}}{R_{REF2}}$. r_e of T1 and T2 in the voltage-current converter also appears in series with R_{REF2} (typically 5k). In practice this is not a problem since the tolerance of the on-chip reference means that a calibration adjustment must be provided anyway.

Using the on-chip reference voltage of 1.26 – 1.35 volts the recommended component values for a full-scale reading of 199.9mV would be $R_{REF1} = 200k$, $R_{REF2} = 500k$ (min.), 520k (max.). Allowing for the use of 2% tolerance components for R_{REF1} and R_{REF2} an adequate adjustment range for calibration purposes will be provided if R_{REF2} is made up of a 470k resistor in series with a 100k multiturn trimmer. Full-scale ranges less than 200mV can be accommodated by reducing the value of R_{REF1}, thus producing the same full-scale input current for a smaller input voltage. The limitations on the minimum value of R_{REF1} are caused by non-linearity in the voltage-current converter, offsets in the auto-zero switches, and the fact that r_e becomes a much larger proportion of R_{REF1}. These factors place a practical limit of about 20k on R_{REF1}.

Similarly full-scale ranges greater than ±200mV can be accommodated by the value of R_{REF1}. The maximum input voltage that can be applied is limited by the common-mode range of the differential inputs. Provided the common-mode range of either input terminal is not exceeded the maximum differential voltage that can be applied between the inputs is about ±2V.

The full-scale range can also be adjusted by varying R_{REF2} which determines the reference current, and indeed placing a preset in series with R_{REF2} is the recommended method of calibration.

I_{REF} can also be varied by using an adjustable external reference voltage instead of the internal reference, which makes ratiometric operation possible.

The minimum value of I_{REF} is limited to about 3μA since above this value the voltage-current converter becomes non-linear. The maximum value of I_{REF} is not quite so well defined as it is determined by deterioration in the performance of current switches T3 and T4 at low collector currents. The minimum useable value of I_{REF} is typically 500nA. This means that the upper and lower limits are $\frac{V_{REF}}{500\,nA}$ and $\frac{V_{REF}}{3\,\mu A}$ respectively. The upper and lower limits on V_{REF} itself are determined by the common-mode range of the reference current amplifier A1 which is 1V to 1.5V. Ratiometric operation with a variable V_{REF} within these limits is possible provided that the upper or lower limit of I_{REF} is not exceeded.

Supply Voltage Options

The ZN450 is designed to be extremely flexible with regard to supply voltage and four power supply options are possible allowing operation over a wide range of supply voltages. These options are illustrated in figure 6.

The first option is to ignore the on-chip regulator and to connect an externally stabilised voltage of 4.5V to 5.5V direct to pin 32, for example a 5V logic supply.

For supply voltages greater than 6V the on-chip shunt regulator (pin 33) may be used by linking pins 32 and 33. When using the shunt regulator an external resistor must be placed in series with the supply to limit the regulator current as shown in figure 6b. The value of this resistor is given by:

$$R = \frac{V_{supply} - 5\ volts}{5}\ (k, \frac{V}{mA})$$ which allows for the maximum 5mA current consumption of the I.C.

If the supply voltage is unstabilised then R should be calculated using the minimum supply voltage that will be encountered. The current drawn by this configuration increases with supply voltage as the shunt regulator sinks more current in order to maintain V_{CC} at 5V. The maximum allowable supply voltage is thus determined by the 15mA maximum rating of the shunt regulator, assuming very little current is drawn by the DVM circuitry, i.e.

$$V_{max} = 15(mA) \times R(k\Omega) + 5\ volts$$
$$= (3V_{min} - 10)\ volts$$

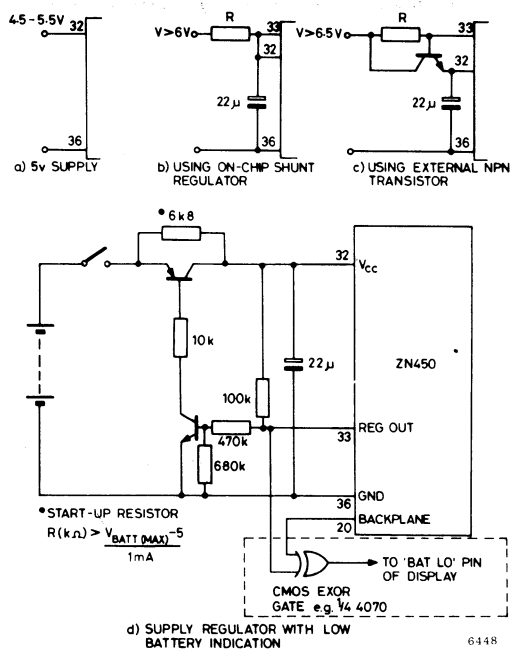


Fig. 6 – SUPPLY VOLTAGE OPTIONS

Since the current drawn by the shunt regulator increases with supply voltage this configuration is not recommended for battery operation where long battery life is a prime criterion, as the current drawn from a new battery could be up to three times the maximum current consumption of the DVM.

For battery operation a series regulator circuit is recommended which can be constructed using one or two external transistors controlled by pin 33. The simplest series regulator, shown in figure 6c, uses a single NPN transistor and allows operation down to about 6.5V. Current consumption of this circuit is the normal current consumption of the DVM plus the base current of the transistor.

The base resistor must be chosen such that it can supply sufficient base drive when the supply voltage is a minimum assuming

(a) Maximum DVM current of 6.5 mA

(b) Maximum shunt regulator voltage of 5.5V

(c) Minimum gain of the transistor

$$\text{Now base current } I_b \text{ (mA)} = \frac{V_{min} - V_{reg} - V_{be\,T1}}{R_b}$$

$$\text{required base current} = \frac{6.5\,mA}{h_{fe\,(min)}}$$

$$\text{Therefore } R_b(k\Omega) = \frac{(V_{min} - V_{reg} - V_{be\,T1}) \times h_{fe}}{6.5} \simeq \frac{(V_{min} - 6) \times h_{fe}}{6.5}$$

Example. The circuit is to operate down to 6.5V with a transistor type whose minimum gain is 80

$$R_b = \frac{(6.5-6)\times 80}{6.5}$$

$$= 6.1k$$

Nearest value of 5k6 is used.

Although a great improvement on the shunt regulator, the circuit of figure 6c still does not achieve maximum battery life since V_{min} must always exceed the regulator voltage by $V_{be\ T1}$ plus the voltage drop across R_b.

For the ultimate in battery life the circuit of figure 6d is suggested. This allows operation down to voltages as low as $V_{reg} + V_{CE(sat)\ T1}$ and, as an added bonus, it automatically detects the end of useful battery life, i.e. the point at which the regulator ceases to function.

T1 is a PNP series regulator transistor controlled by pin 33 via T2, which provides the required signal inversion. During normal operation the voltage drop across R1 is small since the base current required by T2 is only a few hundred nanoamps, and the voltage at pin 33 is not much above the V_{be} of T2 (about 0.6V).

When the battery voltage drops to $V_{reg} + V_{CE(sat)\ T1}$ the voltage at the non-inverting input of the regulator amplifier will fall below V_{REF} and the shunt regulator output transistor will turn off causing the voltage at pin 33 to rise to about 80% of supply.

Pin 33 can conveniently be connected to a low battery indicator consisting of a CMOS EXOR gate, as shown in the dotted box. When pin 33 is low the output of the EXOR gate will be in phase with the backplane and the LO BAT indicator will be extinguished. When pin 33 is high the output will be out of phase with the backplane and LO BAT will be visible.

Oscillator Options

The on-chip oscillator of the ZN450 may be used with various configurations of external components, as shown in figure 7. It will operate with only an external capacitor, which may be fixed, or variable to adjust the oscillator frequency. Alternatively the frequency may be adjusted by placing a variable resistor in series with the capacitor. Graphs of oscillator frequency versus capacitor and resistor values are given in figure 8. If absolute accuracy of the oscillator frequency is required then a crystal or ceramic resonator may be used as the frequency determining element. By making the integration time a whole number of mains cycles a degree of mains interference rejection can be provided. For example a 100 kHz crystal gives an integration time of 200 ms which is 10 cycles at 50 Hz mains frequency or 12 cycles at 60 Hz, the total measurement interval being 480 ms or just over two conversions/second.

If mains interference is superimposed on the input signal it is important that its peak amplitude should be less than 25% of full-scale to avoid saturation of the DSM. If this is not the case then the ZN450 should be preceded by a lowpass filter to give additional mains rejection.

The final option is to overdrive the oscillator input from a TTL or CMOS gate, as shown in figure 7d.

In order to maintain an adequate drive to the comparator the value of C_{DSM} must also be changed in proportion to the oscillator period. A table of suitable values is given below.

Oscillator frequency	C_{DSM}	
(kHz)	Min.	Max.
50	200n	2μ
100	100n	1μ
150	68n	680n

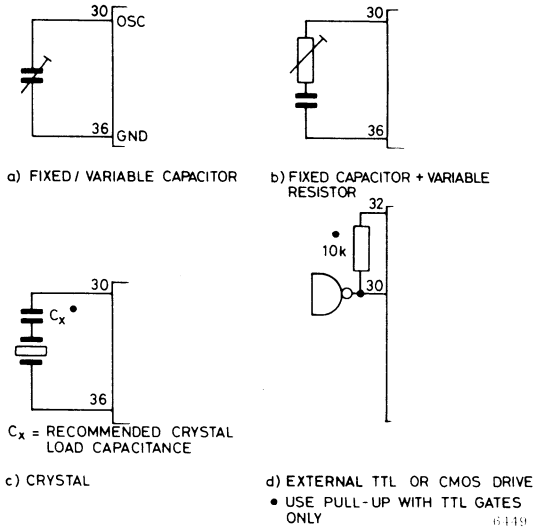


Fig. 7 – OSCILLATOR OPTIONS

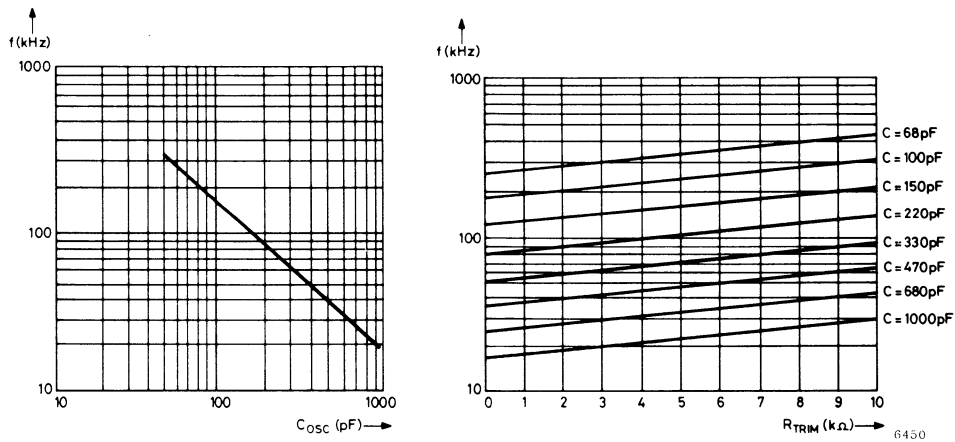


Fig. 8 – OSCILLATOR FREQUENCY vs EXTERNAL CAPACITOR AND RESISTOR

Range Output

To simplify the design of auto-ranging instruments, underrange and overrange detection circuits are provided in the ZN450. Overrange is indicated when the count exceeds 1999, whilst underrange is indicated for counts less than 150. This provides a degree of hysteresis to prevent the instrument jittering between ranges, which could occur if underrange was indicated at a count of 199 and there was a mismatch in the attenuators or other signal conditioning circuits.

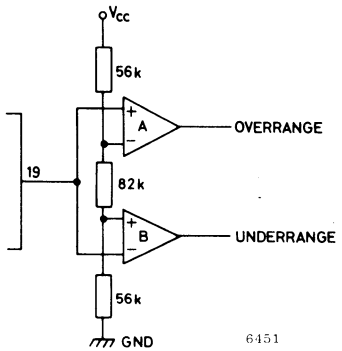
Because the pins of the ZN450 are fully utilised it is not possible to provide separate underrange and overrange pins, so a single three-state output is provided.

If the measurement is in range then pin 19 will be at $\frac{V_{CC}}{2} \pm 0.5V$ with a source resistance of approx. 40k.

For an overrange measurement pin 19 will go HIGH for 1000 clock pulses synchronous with the data store pulse at the end of the measurement. For an underrange measurement pin 19 will pulse LOW in a similar manner. In each case the output resistance is approx. 80k.

The range output can be fully decoded using a dual comparator, as shown in figure 9.

A visual overrange indication is also provided. In this condition the leading digit of the display shows a '1' whilst all other digits are blanked.



Range Output	Output A	Output B
Underrange (GND)	0	⎍
In Range ($\frac{1}{2}V_{CC}$)	0	0
Overrange (V_{CC})	⎍	0

Fig. 9 – DECODING THE RANGE OUTPUT

Display Hold

The reference input, pin 37, also doubles as a display hold pin. If this pin is grounded then the display will continue to show the results of the last valid measurement until pin 37 is released. Display hold also resets the system counters and a new measurement begins immediately display hold is released. The method of activating display hold depends on whether or not the on-chip reference and shunt regulator are being utilised.

If an external reference voltage is used (pins 35 and 37 not joined) then display hold can be activated by grounding pin 37 with a single-pole switch, transistor or open-collector logic gate, provided that the external reference is not required to supply other circuits. If the on-chip regulator is to be used then pin 35 must, of course, be biased up with an external 22k resistor so that V_{REF} can supply the reference voltage for the regulator. If the on-chip reference is used but the on-chip regulator is not then display hold can be activated in a similar manner by grounding the junction of pin 35 and pin 37.

However, since the on-chip reference also provides the reference voltage for the on-chip regulator pin 35 must not be grounded if the regulator is in use or the supply voltage will drop to zero. If the on-chip reference and shunt regulator are both used then pin 37 must be disconnected from pin 35 before it is grounded to activate display hold. This is illustrated in figure 10. As pin 37 normally supplies the bias current for the on-chip reference this must be provided by an external 22k resistor when these pins are not linked.

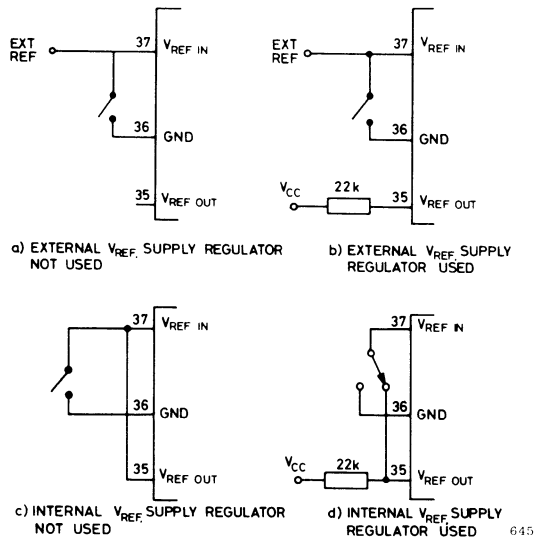


Fig. 10 – DISPLAY HOLD OPTIONS

Backplane Output

The backplane output normally provides a squarewave of the same frequency as, but 180° out of phase with, the active segment outputs. This provides the necessary a.c. drive to the L.C. display. By grounding the backplane output the a.c. drive to the segments may be inhibited and the segment outputs become normal active low (TRUE = 0) outputs. This facility is useful if the output data is to be used for some purpose other than display driving. An L.C. display should not be connected to the ZN450 in this condition as d.c. drive will eventually damage it.

Decimal Point Drive

The ZN450 provides all the outputs necessary to drive the segments of a 3½ digit liquid crystal display. However, in order to drive decimal points and annunciators such as low battery indicators, some external components are required. To turn on a decimal point it is necessary to provide it with a drive signal of the same frequency as, but 180° out of phase with, the backplane output. For driving a single, fixed decimal point, the simple inverter circuit of figure 11a can be used.

If more than one decimal point is to be selected then it is necessary for the unused decimal points to be switched off by arranging their drive waveforms to be in phase with the backplane output. This is simply achieved using exclusive OR gates as shown in figure 11b.

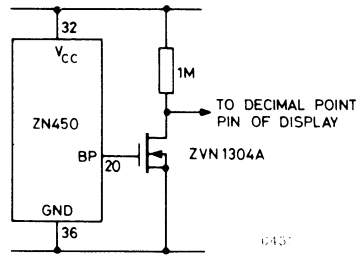
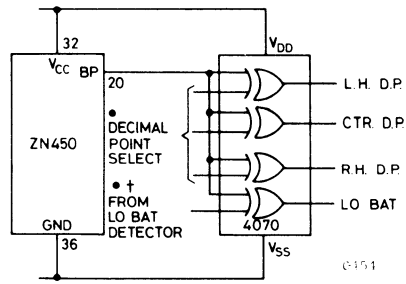


Fig. 11a – DRIVING A FIXED DECIMAL POINT



*Logic 1 = ON
Logic 0 = OFF
†See also figure 6

Fig. 11b – DECIMAL POINT SELECT AND 'LO BAT' INDICATOR DRIVE USING EXCLUSIVE OR GATES

A logic '1' on the input causes the output waveform to be out of phase with the backplane and the appropriate decimal point is activated. Conversely a logic '0' causes the output to be in phase with the backplane. A single 4070 CMOS quad-EXOR gate I.C. will provide the drive for the three decimal points of a 3½ digit liquid crystal display plus the drive to a low battery indicator. A suitable low battery detection circuit is shown in figure 6d.

External Components

A basic 200 mV DVM can be built using only ten external passive components, as shown in figure 12. In addition to these components it is good practice to include input protection resistors to limit the maximum input current to 50 mA in the event of an input overload. The resistance and power rating of these components depends on the maximum voltage against which the inputs are to be protected.

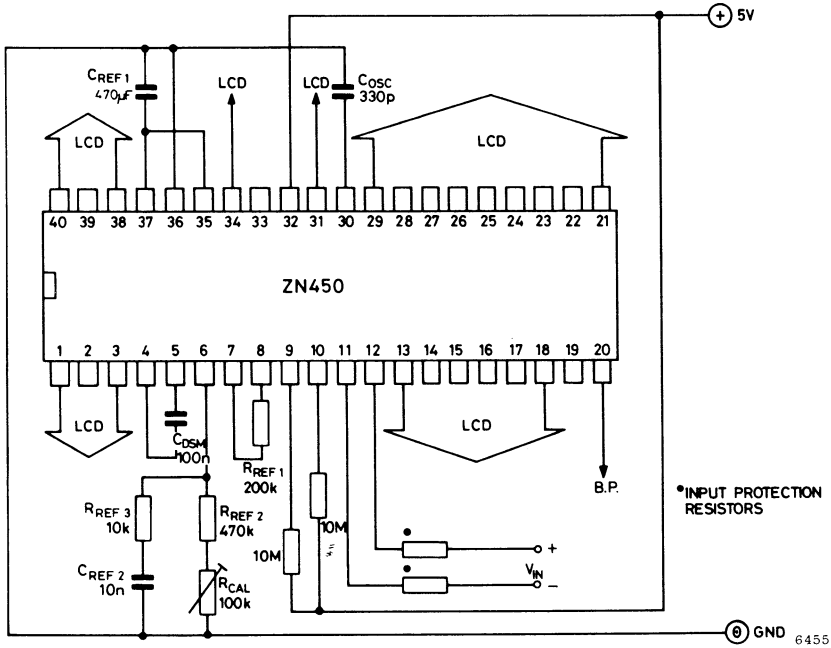


Fig. 12 – EXTERNAL COMPONENTS FOR A BASIC 200 mV DVM WITH 5V SUPPLY

Signal Conditioning

The ZN450 can be used with a wide variety of signal conditioning circuits and transducers to provide a digital display of any parameter that can be converted into a suitable d.c. voltage.

Voltage Measurement

The most obvious signal conditioning circuit is a switched input attenuator which will allow d.c. voltages greater than 200 mV to be measured. To minimise time-consuming calibration procedures it should be possible to calibrate the DVM on only one range and to rely on the precision of the attenuator resistors to give accurate results on other ranges.

However, since the input resistance of the ZN450 is about 10 MΩ its loading effect on the attenuator cannot be ignored. Fortunately this effect can be eliminated by designing an attenuator with a constant output resistance so that the ZN450 sees the attenuator as a 199.9 mV (full-scale) source with a constant source resistance on all ranges.

Three suitable types of attenuator circuit are shown in figure 13, a ladder attenuator and two types of T attenuator. The ladder attenuator has the advantage that the input resistance is fairly constant and only 3 resistor values are required, but the switching is somewhat complicated.

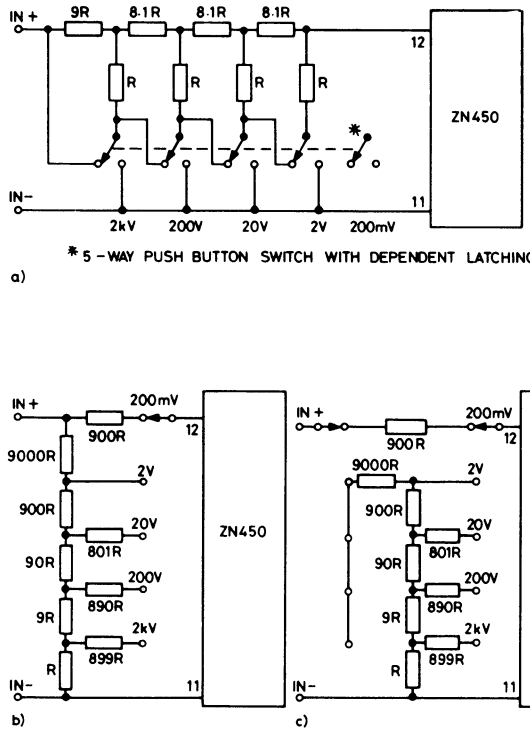


Fig. 13 – ATTENUATORS FOR MULTIRANGE VOLTMETER

The T attenuator of figure 13b has the advantage of simplicity, using only a single-pole switch, but the resistor values are slightly odd. Furthermore the input resistance drops to about 5 MΩ on the 200 mV range since the attenuator appears in parallel with the ZN450's input resistance. This problem can be overcome by using a two-pole switch so that the attenuator is disconnected on the 200 mV range as shown in figure 13c.

When designing signal conditioning circuits for use with the ZN450 care must be taken to ensure that the input offset current does not cause errors. The offset current generates an error voltage $I_{OS} \times R_O$ where R_O is the output resistance of the attenuator. There are two components in the offset current; that due to the ZN450 itself, typically 100 pA, and a component due to the mismatch of the 10 MΩ input resistors, typically 150 pA per kΩ mismatch. The offset current can be minimised by using well matched 10 MΩ resistors, or can be nulled out entirely using the circuit of figure 14.

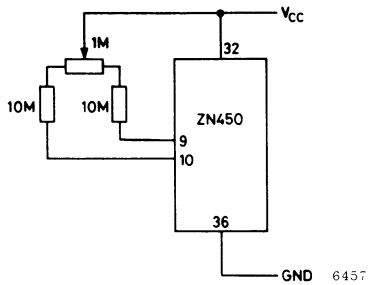


Fig. 14 – OFFSET CURRENT NULLING CIRCUIT

Current Measurement

Measurement of d.c. current is also very simple. The current to be measured is allowed to flow through a shunt resistor connected across the input terminals of the ZN450, the voltage measured being equal to the product of the current and the shunt resistors.

Currents as low as 20 μA full-scale can be measured before the input resistance and offset current of the ZN450 become significant.

For multi-range current measurement the preferred circuit is the so-called universal shunt, an example of which is shown in figure 15.

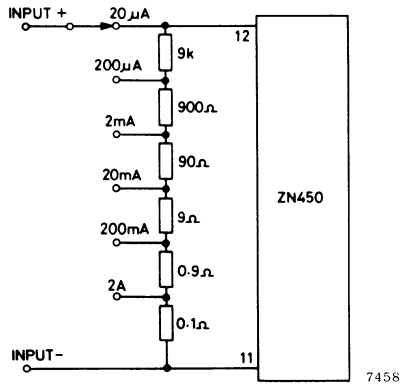


Fig. 15 – MULTIRANGE AMMETER CIRCUIT USING UNIVERSAL SHUNT

Although the full-scale voltage drop of this circuit is 200 mV it is perfectly feasible to design an ammeter with a smaller voltage drop by increasing the sensitivity of the ZN450. This has two advantages. Firstly, the voltage loss in the ammeter is reduced, which can be useful when making measurements in low-voltage circuits. Secondly, the power dissipation in the shunt resistors is reduced.

Example:
Measuring 20A full-scale with a 200 mV voltage drop the required shunt resistor will be $\frac{0.2}{20} = 10\,\text{m}\Omega$ and the full-scale power dissipation will be 4 watts. With a 20 mV drop the required resistor will be 1 mΩ and the power dissipation 400 mW.

Transducer Bridge Circuits

The high sensitivity and true differential inputs of the ZN450 make it ideal for use with transducers, particularly those which function best in a bridge configuration. The regulated 5V supply can also provide a stable excitation voltage for passive transducers such as semiconductor pressure gauges, platinum resistance thermometers and semiconductor temperature sensors.

Figure 16 shows a thermometer circuit using a silicon diode as the temperature sensor. The forward voltage drop has a temperature coefficient of approximately $-2\,mV/°C$ when the device is run at a constant current. In the bridge circuit shown this gives an increase of about $1.28\,mV/°C$ at the + input of the ZN450. The full-scale reading of the ZN450 is set to about 256 mV so that one digit corresponds to 0.1°C and the full-scale reading is 199.9°C.

The bridge configuration allows the forward voltage drop of the diode to be nulled out using P1 to give a reading of 000.0 at 0°C, whilst P2 adjusts the full-scale range of the ZN450 to read 100.0 at 100°C.

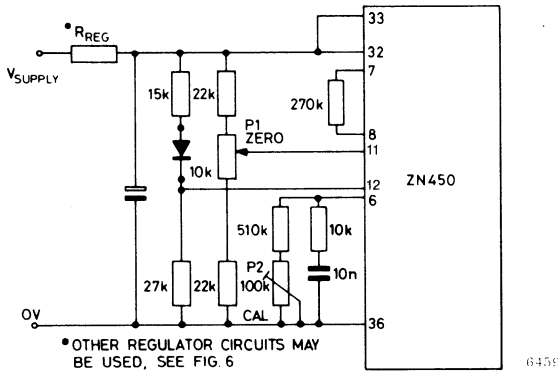


Fig. 16 – DIGITAL THERMOMETER CIRCUIT

Common-Mode Performance

The ZN450 has true differential inputs with a common-mode range of 1.8 – 3.8 volts and good common-mode rejection. However, if the full potential of the differential inputs is to be realised then care must be taken when designing with the ZN450.

When open-circuit, the inputs of the ZN450 are biased at about 2.8 volts above supply common. If a common-mode voltage other than this is applied to the inputs then care must be taken to ensure that any impedances between the inputs and the common-mode voltage (attenuators, series resistors, etc.) are the same for each input, otherwise the common-mode rejection will be impaired. This is illustrated in figure 17. Balancing the input of impedances of differential inputs to ensure good common-mode rejection is, of course, normal practice.

This is generally a problem only in systems where the voltage to be measured is referenced to the ZN450's supply ground. In battery-powered applications no common-mode voltage exists between the measured voltage and the inputs, since the supply voltage of the ZN450 is floating. However, care must be taken in battery-powered systems to ensure good a.c. rejection.

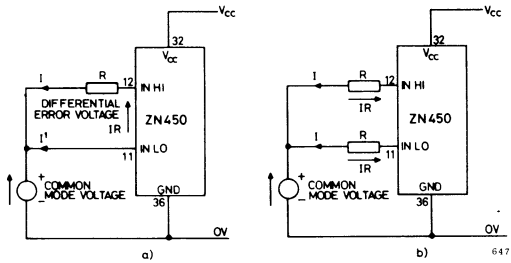


Fig. 17 – (a) UNBALANCED INPUT RESISTANCES IMPAIR COMMON-MODE REJECTION.

(b) WITH BALANCED INPUT RESISTANCES COMMON-MODE VOLTAGE DOES NOT CAUSE DIFFERENTIAL ERROR VOLTAGE.

If the voltage being measured has a large a.c. common-mode signal superimposed upon it then the supply voltage of the ZN450 will normally float up and down with the a.c. component, thus keeping the inputs of the ZN450 within their common-mode range. However, the resistance between the a.c. signal at the inputs and the ZN450 supply rails is the 5MΩ common-mode resistance of the ZN450 inputs. If significant stray capacitance exists between the ZN450 supplies and ground (for example if the battery is close to an earthed metal surface) then this can form a low pass filter with the common-mode input resistance with the result that the ZN450 supply rails do not follow the a.c. common-mode voltage at the inputs. This is shown in figure 18.

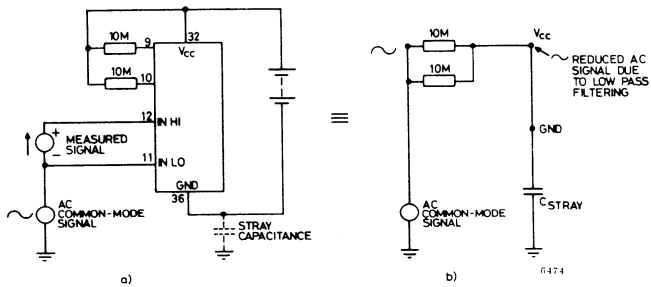


Fig. 18 – (a) BATTERY-POWERED ZN450 CONNECTED TO SIGNAL WITH LARGE A.C. COMMON-MODE SIGNAL. (SUPPLY REGULATOR NOT SHOWN).

(b) EQUIVALENT A.C. CIRCUIT.

The problem can be overcome in one of two ways. The simpler method, shown in figure 19a, is to connect a capacitor between input low and supply ground. This provides a low impedance a.c. path between these two points so that the supply rails will track the a.c. common-mode voltage.

The value of this capacitor should be several times greater than the maximum stray capacitance. On the other hand, at switch-on it must charge up via the 10M input resistance of the ZN450, so it should not be too large. A value of 22n is about the optimum.

An alternative solution is to mount the DVM in a screened enclosure, the screening being connected to input LO. This has the effect of producing a stray capacitance between the ZN450 supply rails and screen. However, since the screen is not at a fixed potential, but follows the common-mode signal, the effect of this capacitance is bootstrapped out.

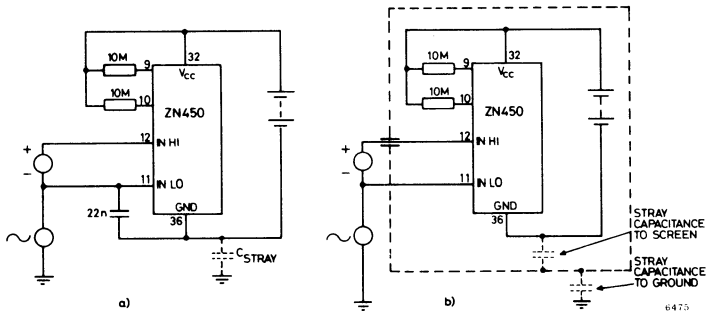


Fig. 19 – TWO METHODS OF ENSURING A.C. REJECTION IN BATTERY-POWERED CIRCUITS.

A.C. Measurements

To measure a.c. voltage or current it is first necessary to convert it into a proportional d.c. voltage. The simplest way to do this is to interpose a precision active rectifier circuit between the attenuator or shunt and the inputs of the ZN450. Such a circuit produces d.c. voltage proportional to the mean of the rectified voltage rather than a true R.M.S. result and for true R.M.S. measurements an R.M.S. converter must be used. The rectifier can be calibrated to read R.M.S. but the result is true only if the input signals have a constant form factor.

A simple precision rectifier circuit is shown in figure 20. It is completely a.c. coupled throughout by C2, C3 and C4, so the offset voltage of A1 does not appear at the output and no zero adjustment is required. To prevent the offset voltage of A1 causing it to saturate in the absence of an input signal, 100% d.c. feedback is provided by R3.

R1 and R2 provide a d.c. bias path for the non-inverting input of A1, whilst C2 provides bootstrapping to increase the a.c. input impedance.

Amplifier A2 is a voltage follower biased into the middle of the ZN450's common-mode range to provide a low impedance analogue common point. The output of the rectifier is connected to a lowpass filter comprising R6 and C5. So that both inputs of the ZN450 see the same d.c. resistance R6 is placed in series with the input LO terminal and is made equal to R4 + R5. This in no way affects the performance of the filter. With the component values shown the circuit is calibrated to read R.M.S. for sinewave inputs, so the use of this type of waveform will be assumed throughout.

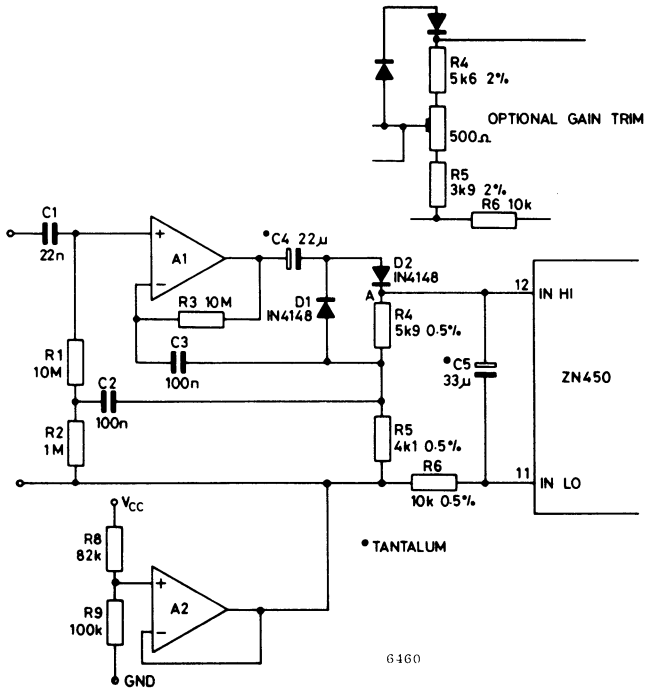


Fig. 20 – PRECISION RECTIFIER FOR A.C. MEASUREMENTS

The circuit functions as follows: when the input signal crosses zero in a positive going direction the output of A1 slews positive until D2 conducts after which the voltage at point A is defined by the equation:

$$V_A = G \times V_{IN}, \text{ where } G = \frac{R_4 + R_5}{R_5}$$

and since

$$R_6 = R_4 + R_5$$

$$G = \frac{R_6}{R_6 - R_4}$$

and

$$R_4 = R_6 \frac{(G-1)}{G}$$

This voltage tends to charge up C_5 in a positive direction via R_6. When the signal crosses zero in a negative going direction the output of A1 slews negative until D1 conducts, after which the output voltage at point B is equal to (minus) V_{IN}. This voltage tends to charge up C_5 in a negative direction via R_6 and R_4.
Now, assuming the time constant R_6/C_5 is long compared to the period of the input waveform, the voltage on C_5 will eventually reach equilibrium. When this is the case the mean current flowing into C_5 during the positive half cycle must equal that flowing out of C_5 during the negative half cycle.

i.e.

$$\frac{V_{A(MEAN)} - V_C}{R_6} = \frac{-V_{B(MEAN)} + V_C}{R_6 + R_4}$$

Now the mean value of a rectified sinewave signal is 0.9 times the R.M.S. value therefore

$$V_{A(MEAN)} = 0.9.G.V_{IN(RMS)}$$

and

$$V_{B(MEAN)} = -0.9\,V_{IN(RMS)}$$

In order for the ZN450 to read correctly V_C must equal V_{RMS} therefore

$$V_A = 0.9.G.V_C$$

and

$$V_B = -0.9\,V_C$$

therefore

$$\frac{V_C(0.9G-1)}{R_6} = \frac{1.9V_C}{R_6+R_4}$$

substituting for R_4 and eliminating V_C

$$\frac{0.9G-1}{R_6} = \frac{1.9}{R_6 + R_6\dfrac{(G-1)}{G}}$$

eliminate R_6

$$0.9G-1 = \frac{1.9G}{2G-1}$$

$$(0.9G-1)\,(2G-1) = 1.9G$$

$$1.8G^2 - 4.8G + 1 = 0$$

Solving the above quadratic equation gives

$$G = 2.439$$

or

$$R_4 = 0.59R_6$$

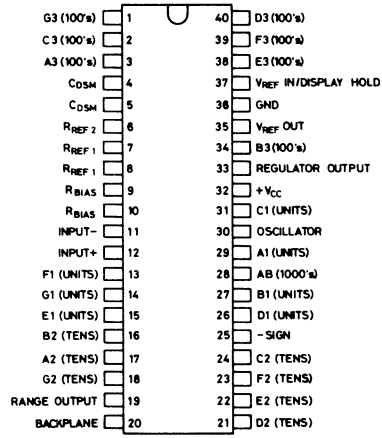
$$R_5 = \frac{R_6}{2.439}$$

These equations allow the values of R_4 and R_5 to be calculated for any value of filter resistor R_6. With the values shown the circuit is accurate to about $\pm 1.5\%$ over the frequency range 40 Hz to 1 kHz.

Ordering Information

Type Number	Package	Operating Temperature Range
ZN450E	Plastic	0°C to +70°C
ZN450CJ	Ceramic	0°C to +70°C

PIN CONNECTIONS



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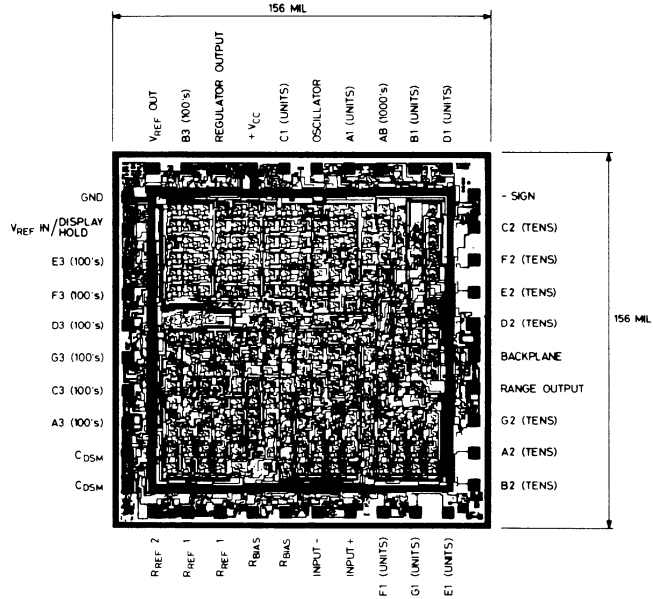
CHIP DIMENSIONS AND LAYOUT



ZN451E/CJ

FERRANTI semiconductors

3½ Digit DVM IC with External Auto-Zero

FEATURES

- External circuits may be included in the auto-zero loop
- Full-scale reading 1.999mV or lower
- Measures sum or difference of two inputs
- Digital Auto-zero with guaranteed zero reading for 0V input
- True polarity at zero for null detection
- True differential inputs
- Direct drive of Liquid Crystal Display
- On-chip clock and precision reference
- Underrange/overrange indication
- Low power consumption, less than 35mW
- Wide supply voltage range, single supply rail

DESCRIPTION

The ZN451 is a complete digital voltmeter fabricated on a monolithic chip. A novel charge-balancing conversion technique ensures good linearity. The auto-zero function is completely digital in operation, thus obviating the need for a capacitor to store the error voltage. Output signals are provided to control external auto-zero switches so that op-amps or other signal conditioning circuits can be included in the auto-zero loop to boost input impedance and/or improve sensitivity to as low as 1.999mV full-scale.

This versatile I.C. can be used as the basis not only for digital voltmeters and multimeters but also in other instruments such as thermometers and pressure gauges where its sensitivity allows interfacing to low output transducers such as thermocouples and strain gauges.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} .. .. -0.5 to $+7$ volts
Maximum Voltage, all other inputs .. .. -0.5 to $(V_{CC}+0.5)$ volts
Operating Temperature Range .. .. 0 to $+70°C$
Storage Temperature Range .. .. -55 to $+125°C$

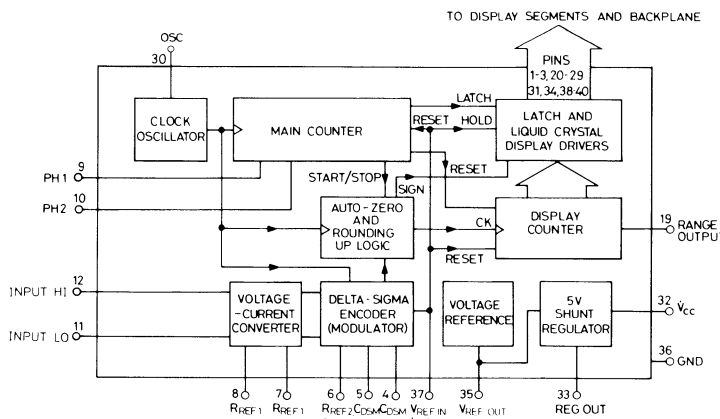


Fig. 1 ZN451 System Diagram

ELECTRICAL CHARACTERISTICS (V_{CC} = +5V, T_{amb} = +25°C unless otherwise specified)

Parameter	Min.	Typ.	Max.	Unit	Conditions
Full-scale reading	−1999	–	+1999		
Zero reading	−000.0	±000.0	+000.0	digital reading	V_{IN} = 0, V_{FS} = 200mV
Rollover error	−2	0	+2	count	$-V_{IN} = +V_{IN} = \pm 200$mV conversion time ⩾0.5 sec.
Linearity	−1	0	+1	count	V_{FS} = 200mV conversion time ⩾0.5 sec.
Common mode range	1.8	–	3.8	volts	
Common mode rejection	–	120	–	μV/V	
Supply rejection	–	100	–	μV/V	
Input offset current	–	0.1	1	nA	
Input resistance	–	20	–	MΩ	
Zero temperature coefficient	–	–	1	μV/°C	
Full-scale temperature coefficient	Determined by tracking of external resistors				ref. T.C. = 0ppm/°C
Oscillator frequency range	–	–	300	kHz	
Conversion time (48000 oscillator periods)	0.25	–	–	seconds	
VOLTAGE REFERENCE					
Output voltage	1.26	1.3	1.35	volts	
Temperature coefficient	–	±50	±80	ppm/°C	
Knee current	–	–	150	μA	
Maximum sink current	1	2	–	mA	
SUPPLY VOLTAGE					
(a) Direct	4.5	5	5.5	volts	
(b) Using on-chip shunt regulator	6.0	–	–	volts	
(c) Using external NPN transistor	6.5	–	–	volts	
(d) Using two transistor regulator	5.5	–	–	volts	
Supply current	–	4	6.5	mA	
SHUNT REGULATOR					
Output voltage	4.5	5	5.5	volts	
Sink current	–	–	15	mA	
DISPLAY OUTPUTS					
Peak voltage	–	$\pm V_{CC}$	–		
D.C. component	–	–	±25	mV	
Backplane frequency	–	$\frac{1}{2000}$	–	oscillator frequency	

GENERAL DESCRIPTION

The ZN451 utilises a charge-balancing conversion principle, which offers a number of advantages over the more common dual-slope integration method.

These include a fixed conversion time which is independent of the analogue input voltage, completely digital auto-zero and inherently bipolar operation. Linearity is also extremely good over the entire input voltage range, unlike some dual-slope designs where stray capacitance can cause problems around zero.

The auto-zero loop of the ZN451 is external to the device so that op-amps and other signal-conditioning circuits can be included within it and thus have their zero errors removed.

The conversion time of the ZN451 is divided into two periods, Phase 1 and Phase 2, unlike the dual-slope system which has three distinct phases, signal integrate, reference integration and auto-zero.

The heart of the ZN451 is the delta-sigma encoder, a simplified circuit of which is shown in fig. 2.

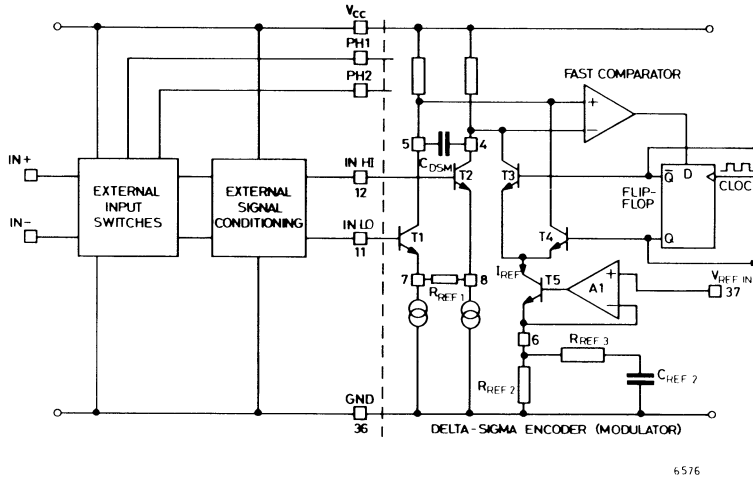


Fig. 2 Input Switching and Delta-sigma Encoder

The delta-sigma encoder of the ZN451 consists of a voltage-current converter comprising T_1 and T_2, a reference generator A_1/T_5 and a feedback loop containing a fast comparator, D-type flip-flop and current switches T_3 and T_4. These can switch a current $I_{REF} = \frac{V_{REF}}{R_{REF2}}$ into the collector circuit of either T_1 or T_2, depending on the state of the flip-flop.

The polarity of the voltage across capacitor C_{DSM} is monitored by the comparator, whose output is sampled on every clock pulse by the flip-flop. The outputs of the flip-flop switch I_{REF} into the collector circuit of either T_1 or T_2 so as to oppose the existing voltage on C_{DSM} i.e. to maintain the average charge acquired by D_{DSM} at zero, thus keeping the circuit in equilibrium.

Assuming perfect symmetry in the circuit, with zero volts applied between the bases of T_1 and T_2 their collector currents will be equal, and the only charge acquired by C_{DSM} will be that put on it by I_{REF}. The flip-flop will thus change state on every clock pulse so that C_{DSM} will alternately acquire charge quanta of $+I_{REF}T_C$ and $-I_{REF}T_C$ (where T_C is the clock period) and the nett charge acquired will be zero. The output of the flip-flop will thus be a square-wave with a 50% duty cycle.

During the measurement the voltage to be measured is applied between the bases of T_1 and T_2 and is converted into a current $I_{IN} = \frac{V_{IN}}{R_{REF1}}$ flowing in R_{REF1}. This produces a different current 21_{IN} in the collector currents of T_1 and T_2, so that the charge acquired by C_{DSM} is no longer equal and opposite ($\pm I_{REF}$) but is now ($I_{REF} - 21_{IN}$) T_C when T_4 is turned on and ($-I_{REF} - 21_{IN}$) T_C when T_3 is turned on.

In order to maintain equilibrium the flip-flop will now no longer change state on every clock pulse but will remain in one state for a longer period than it remains in the opposite state. i.e.
$N_1 T_C(I_{REF} - 21_{IN}) + (N - N_1)T_C(-I_{REF} - 21_{IN}) = 0$
where N_1 is the number of clock pulses for which the flip-flop Q output is a '1' and N is the total number of clock pulses over which the measurement is made and assuming N is so large that quantising error can be ignored.

Thus $N_1(I_{REF} - 21_{IN}) = (N - N_1)(I_{REF} + 21_{IN})$

And $\frac{2N_1 - N}{N} = \frac{21_{IN}}{I_{REF}}$ i.e. $N_1 - \frac{N}{2} = \frac{NI_{IN}}{I_{REF}} = \frac{NV_{IN}R_{REF2}}{R_{REF1}V_{REF}}$

In other words, if a counter is allowed to count N_1 and $\frac{N}{2}$ is subtracted from it (by initially presetting the counter to $-\frac{N}{2}$ then the result is directly proportional to V_{IN}, assuming N, V_{REF1} and R_{REF2} are fixed. With zero input voltage the DSM duty-cycle should be 50%, N_1 should equal $\frac{N}{2}$ and the accumulated count should be zero. In practice, of course, this will not be the case due to offsets and component mismatching in the DSM. Fortunately, an interesting property of the DSM allows the zero error to be removed digitally.

If the DSM output is taken from the $\overline{Q}$ output of the flip-flop instead of the Q output then the number of pulses counted over a period of N clock pulses will be not N_1 but $N\text{-}N_1$. Thus, if the counter is preset to $-N$ instead of $-\frac{N}{2}$ the number accumulated in the counter after N clock pulses will be $-N_1$. In other words, taking the $\overline{Q}$ output of the DSM and presetting the counter to $-N$ gives a result proportional to minus the input voltage. This is what occurs during phase 1.

Clearly, if the input voltage is the same during phase 1 and phase 2 the counter will accumulate a count of $-N_1$ during phase 1 and add a further N_1 pulses during phase 2, giving a total count of zero. If the input voltage is zero during both phases the system will measure minus the zero error during phase 1 and plus the zero error during phase 2, thus giving an automatic zero reading.

Obviously when measuring an actual input voltage the DSM must not see the same voltage during both phases, otherwise a zero reading will always result whatever the input. The input voltage must thus be switched, and this can be achieved in two ways. Most obvious is to disconnect the input voltage during phase 1 and connect it during phase 2, so that the result is proportional to $-V_{OS} + (V_{OS} + V_{IN}) = V_{IN}$. Alternatively the polarity of the input voltage can be reversed during phase 1 so that the result is proportional to $-(V_{OS} - V_{IN}) + (V_{OS} + V_{IN}) = 2V_{IN}$. This of course means that the component values must be calculated for twice the required full-scale reading, i.e. for 200mV full-scale the components would be calculated for 400mV. This can be achieved simply by doubling the value R_{REF1}.

The second method has advantages where a large input overload margin is required before the DSM saturates. This occurs when its duty-cycle is 0% or 100%, i.e. when $I_{IN} = \pm \frac{I_{REF}}{2}$ and N_1 = zero or N. (N = 5000 in the ZN451).

Overrange occurs at a reading of ± 2000. The duty-cycle of the DSM at this point depends on the input switching method used.

Whatever method is used, with zero input voltage the counter will count 2500 clock pulses during phase 1 and 2500 during phase 2 to give a reading of zero (assuming negligible zero-error). Using the first input switching method the signal is measured only during phase 2, so an additional 2000 clock pulses must be counted during phase 2, i.e. a total of 4500 clock pulses must be counted during phase 2.

Substituting in $I_{IN} = (N_1 - \frac{N}{2})\frac{I_{REF}}{N}$ to find the required value of I_{IN} for overrange $I_{IN} = 0.4 \times I_{REF}$FS.

The overload margin before the DSM saturates is thus $\frac{1}{10} I_{REF}$ or 25% of full-scale.

Using the second input switching method the input signal is measured during both phases, so for a full-scale reading an additional 1000 clock pulses will be counted due to the input voltage in each phase, giving a clock total of 3500 clock pulses in each phase.

Therefore substituting $I_{IN} = (N_1 - \frac{N}{2})\frac{I_{REF}}{N}$ to find the required I_{IN} for overrange.

$I_{IN} = 0.2\ I_{REF}$.

The overload margin before the DSM saturates is thus 0.3 I_{REF} or 150% of full-scale. i.e. input switching method (b) gives six times the overload margin of method (a).

Input switching method (b) has several other interesting properties, some of which can usefully be exploited.

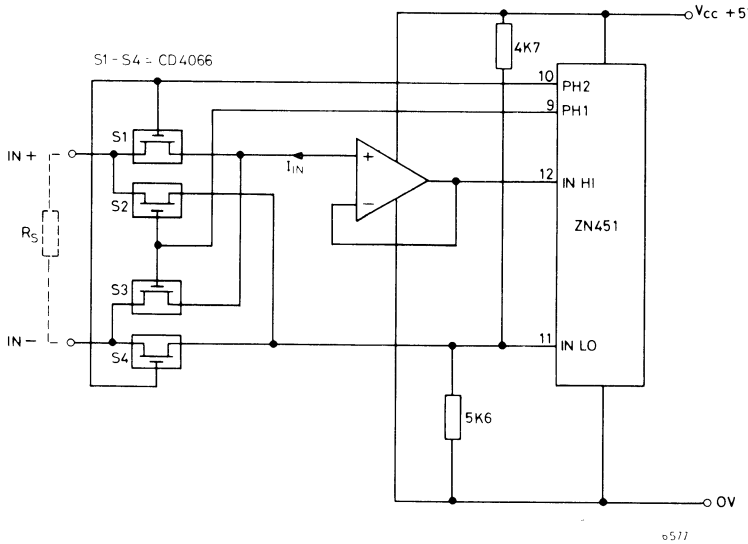


Fig. 3

Fig. 3 shows the simplest possible configuration using an op-amp as a voltage follower to boost the input resistance. Suppose this is a J-FET op-amp with an input current of around 100pA. Suppose a 10M resistor is connected between input + and input – . The input current of the op-amp will generate a voltage of 1mV across this resistor. However, this will not cause a zero error since the direction of current flow, and hence the polarity of the voltage, is the same during phase 1 and phase 2.

Therefore, using switching method (b), high resistance sources will not cause zero errors, subject to the proviso that the error voltage does not cause saturation of the DSM.

The two measurement phases of the ZN451 can also be used to perform other functions. By re-configuring the input switches to measure one input voltage during phase 1 and a second input voltage during phase 2 it is possible to measure the sum or difference of the two voltages, depending on their relative polarity. This is shown in fig. 4.

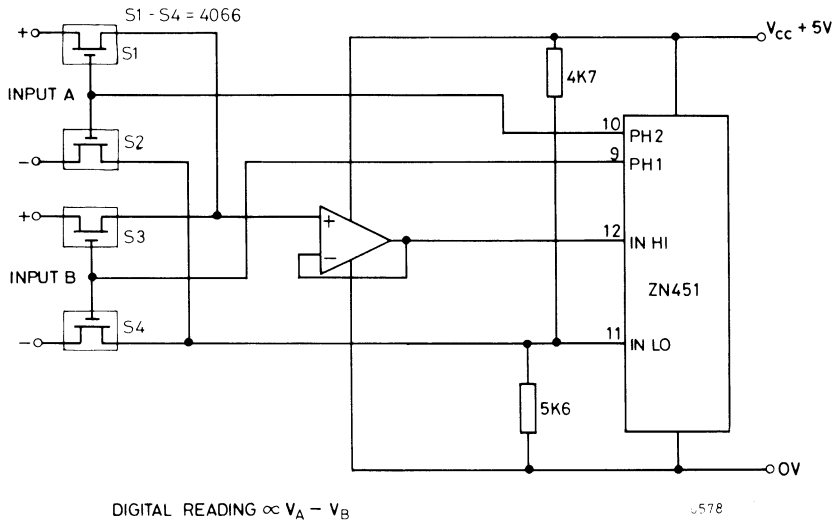


Fig. 4

TIMING DIAGRAM

The value of N chosen for the ZN451 is 5000, so each phase of the measurement should take 5000 clock pulses, a total of 10,000 for the whole measurement. However, the display counter of the ZN451 is preceded by a divide-by-four counter which performs several functions.

Firstly it provides two guard bits so that quantising errors between phase 1 and phase 2 measurements do not give rise to spurious zero errors of ± 1, but are confined to the (non-displayed) guard bits.

Secondly, it provides information to the polarity and rounding up logic, which drives the − sign. The divide-by-four stage means that the display counter sees only one-quarter of the pulses from the DSM and each phase must thus run for 20,000 clock pulses. Furthermore, each measurement phase is separated by a pause of 4000 clock periods to allow the input switches to settle. One measurement cycle thus takes a total of 48,000 clock periods.

Fig. 5 is a timing diagram of the ZN451 which clearly shows the two measurement phases and the operation of the DSM. Two control signals PH_1 and PH_2 indicate which measurement phase is active. These outputs are CMOS compatible and can be used directly to drive input switches such as the 4066.

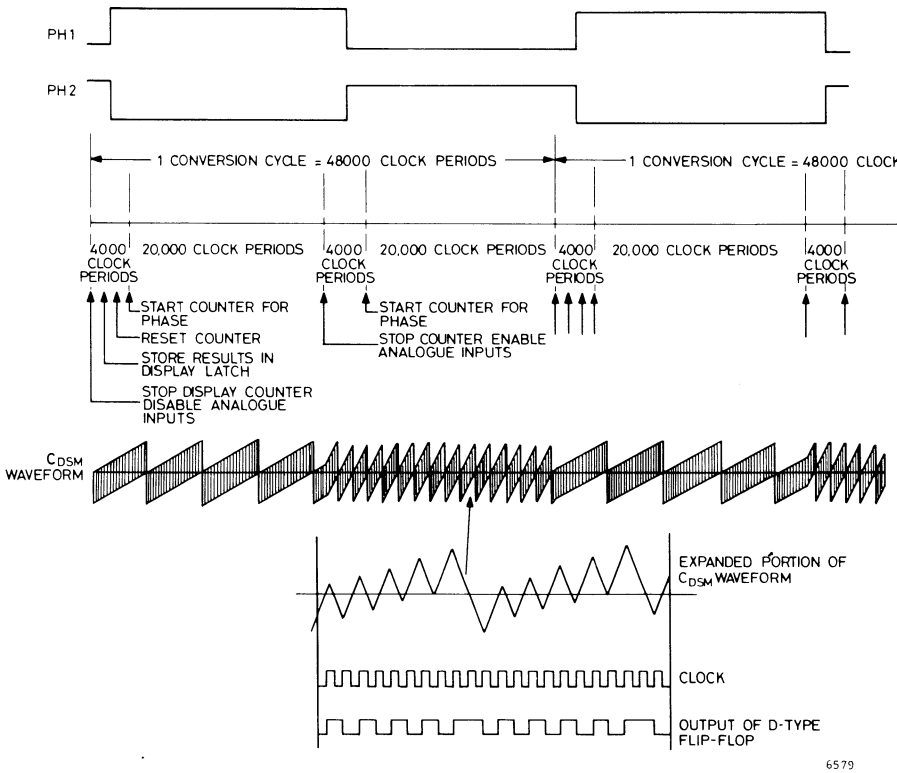


Fig. 5 Timing Diagram of ZN451

REFERENCE LOOP AND SUPPLY REGULATOR

The reference current defining loop is shown in more detail in fig. 6.

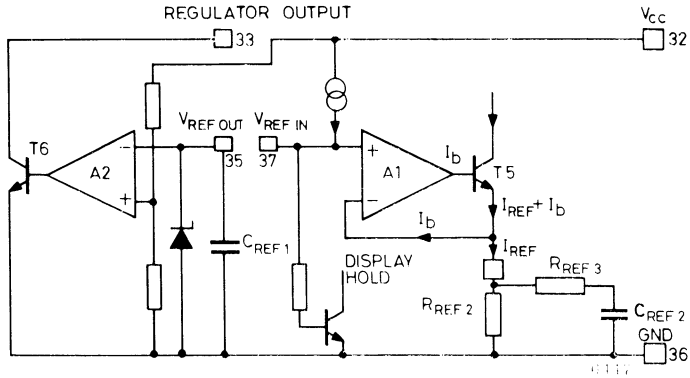


Fig. 6 Reference Current Loop and Supply Regulator

A reference input voltage applied to the non-inverting input of A_1 causes the output of A_1 to bias T_5 such that the inverting input of A_1 assumes the same potential and a current $\frac{V_{REF\ IN}}{R_{REF2}}$ flows in R_{REF2}. By making the input bias current of A_1 the same as the base current of T_5 this base current flows into the inverting input of A_1 instead of through R_{REF2}. The reference current flowing in the collector of T_5 is therefore almost identical to the current flowing in R_{REF2}. The reference loop is stabilised by C_{REF2} and R_{REF3}.

A highly stable on-chip bandgap reference of approximately 1.28V is provided and this may be used by linking $V_{REF\ OUT}$ to $V_{REF\ IN}$ when the reference will be biased on by the 150μA current source connected to the non-inverting input of A_1. The on-chip reference is stabilised by C_{REF1}. The on-chip reference also provides the reference voltage for the on-chip supply regulator A_2. This compares V_{REF} against $\frac{V_{CC}}{4}$ and controls V_{CC} with transistor T_6 such that the two are kept equal, i.e. $V_{CC} = 5V$. The supply regulator can be configured as a shunt or series regulator using only a few external components. If $V_{REF\ OUT}$ is not connected to $V_{REF\ IN}$ but supply regulation is still required then the on-chip reference must be biased on by a 22k resistor to V_{CC}.

SUPPLY VOLTAGE OPTIONS

The ZN451 is designed to be extremely flexible with regard to supply voltage and four power supply options are possible allowing operation over a wide range of supply voltages. These options are illustrated in fig. 7.

The first option is to ignore the on-chip regulator and to connect an externally stabilised voltage of 4.5 to 5.5V direct to pin 32, for example a 5V logic supply.

For supply voltages greater than 6V the on-chip shunt regulator (pin 33) may be used by linking pins 32 and 33. When using the shunt regulator an external resistor must be placed in series with the supply to limit the regulator current as shown in fig. 7b. The value of this resistor is given by:

$R = \frac{V_{supply} - 5}{6.5}$ volts $\left(k\Omega = \frac{V}{mA}\right)$ which allows for the maximum 6.5mA current consumption of the I.C.

If the supply voltage is unstabilised then R should be calculated using the minimum supply voltage that will be encountered. The current drawn by this configuration increases with supply voltage as the shunt regulator sinks more current in order to maintain V_{CC} at 5V. The maximum allowable supply voltage is thus determined by the 15mA maximum rating of the shunt regulator, assuming very little current is drawn by the DVM circuitry, i.e.

$V_{max} = 15(mA) \times R(k\Omega) + 5$ volts

$= (3V_{min} - 10)$ volts

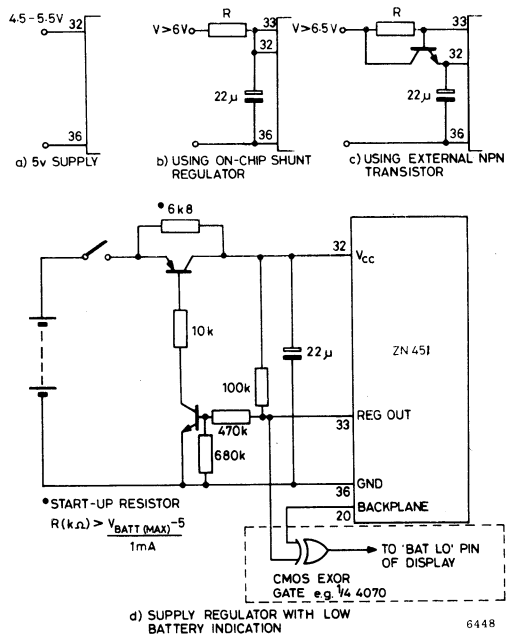


Fig. 7 Supply Voltage Options

Since the current drawn by the shunt regulator increases with supply voltage this configuration is not recommended for battery operation where long battery life is a prime criterion, as the current drawn from a new battery could be up to 2.3 times the maximum current consumption of the DVM.

For battery operation a series regulator circuit is recommended which can be constructed using one or two external transistors controlled by pin 33. The simplest series regulator, shown in fig. 7c, uses a single NPN transistor and allows operation down to about 6.5V. Current consumption of this circuit is the normal current consumption of the DVM plus the base current of the transistor.

The base resistor must be chosen such that it can supply sufficient base drive when the supply voltage is a mimimum assuming

(a) Maximum DVM current of 6.5mA

(b) Maximum shunt regulator voltage of 5.5V

(c) Minimum gain of the transistor

Now base current I_b (mA) $= \dfrac{V_{min} - V_{reg} - V_{beT1}}{R_b}$

required base current $= \dfrac{6.5mA}{h_{fe\ (min)}}$

Therefore $R_b(k\Omega) = \dfrac{(V_{min} - V_{reg} - V_{beT1}) \times h_{fe}}{6.5}$

$= \dfrac{(V_{min} - 6) \times h_{fe}}{6.5}$

Example. The circuit is to operate down to 6.5V with a transistor type whose minimum gain is 80

$R_b = \dfrac{(6.5 - 6) \times 80}{6.5}$

$= 6.1k$

Nearest value of 5k6 is used.

Although a great improvement on the shunt regulator, the circuit of fig. 7c still does not achieve maximum battery life since V_{min} must always exceed the regulator voltage by V_{beT1} plus the voltage drop across R_b.

For the ultimate in battery life the circuit of fig. 7d is suggested. This allows operation down to voltages as low as $V_{reg} + V_{CE(sat)T1}$ and, as an added bonus, it automatically detects the end of useful battery life, i.e. the point at which the regulator ceases to funtion.

T_1 is a PNP series regulator transistor controlled by pin 33 via T_2, which provides the required signal inversion. During normal operation the voltage drop across R_1 is small since the base current required by T_2 is only a few hundred nanoamps, and the voltage at pin 33 is not much above the V_{be} of T_2 (about 0.6V).

When the battery voltage drops to $V_{reg} + V_{CE(sat)T1}$ the voltage at the non-inverting input of the regulator amplifier will fall below V_{REF} and the shunt regulator output transistor will turn off causing the voltage at pin 33 to rise to about 80% of supply.

Pin 33 can conveniently be connected to a low battery indicator consisting of a CMOS EXOR gate, as shown in the dotted box. When pin 33 is low the output of the EXOR gate will be in phase with the backplane and the LO BAT indicator will be extinguished. When pin 33 is high the output will be out of phase with the backplane and LO BAT will be visible.

OSCILLATOR OPTIONS

The on-chip oscillator of the ZN451 may be used with various configurations of external components, as show in fig. 8. It will operate with only an external capacitor, which may be fixed, or variable to adjust the oscillator frequency. Alternatively the frequency may be adjusted by placing a variable resistor in series with the capacitor. Graphs of oscillator frequency versus capacitor and resistor values are given in fig. 9. If absolute accuracy of the oscillator frequency is required then a crystal or ceramic resonator may be used as the frequency determining element. By making the integration time a whole number of mains cycles a degree of mains interference rejection can be provided. For example a 100kHz crystal gives an integration time of 200ms which is 10 cycles at 50Hz mains frequency or 12 cycles at 60Hz, the total measurement interval being 480ms or just over two conversions/second.

If mains interference is superimposed on the input signal it is important that its peak amplitude should not be large enough to cause saturation of the DSM. If this is not the case then the ZN451 should be preceded by a lowpass filter to give additional mains rejection.

The final option is to overdrive the oscillator input from a TTL or CMOS gate, as shown in fig. 8d.

In order to maintain an adequate drive to the comparator the value of C_{DSM} must also be changed in proportion to the oscillator period. A table of suitable values is given below.

Oscillator frequency (kHz)	C_{DSM} Min.	Max.
50	200n	2μ
100	100n	1μ
150	68n	680n

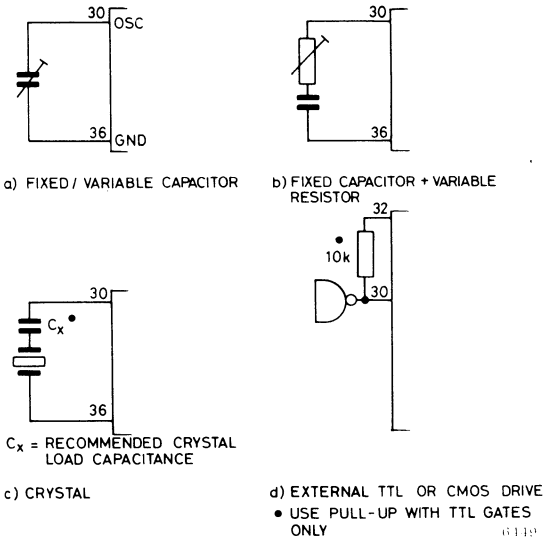


Fig. 8 Oscillator Options

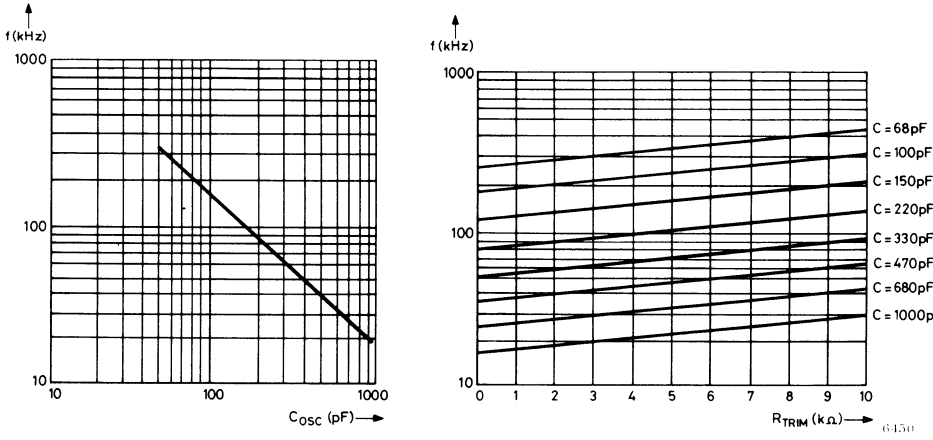


Fig. 9 Oscillator Frequency vs External Capacitor and Resistor

RANGE OUTPUT

To simplify the design of auto-ranging instruments, underrange and overrange detection circuits are provided in the ZN451. Overrange is indicated when the count exceeds 1999, whilst underrange is indicated for counts less than 150. This provides a degree of hysteresis to prevent the instrument jittering between ranges, which could occur if underrange was indicated at a count of 199 and there was a mismatch in the attenuators or other signal conditioning circuits.

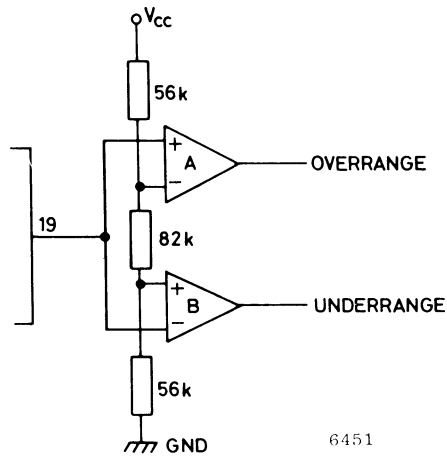
Because the pins of the ZN451 are fully utilised it is not possible to provide separate underrange and overrange pins, so a single three-state output is provided.

If the measurement is in range then pin 19 will be at $\frac{V_{CC}}{2} \pm 0.5V$ with a source resistance of approx. 40k.

For an overrange measurement pin 19 will go HIGH for 1000 clock pulses synchronous with the data store pulse at the end of the measurement. For an underrange measurement pin 19 will pulse LOW in a similar manner. In each case the output resistance is approx. 80k.

The range output can be fully decoded using a dual comparator, as shown in fig. 10.

A visual overrange indication is also provided. In this condition the leading digit of the display shows a '1' whilst all other digits are blanked.



Range Output	Output A	Output B
Underrange (GND)	0	⎍
In Range (½ V_{CC})	0	0
Overrange (V_{CC})	⎍	0

Fig. 10 Decoding the Range Output

DISPLAY HOLD

The reference input, pin 37, also doubles as a display hold pin. If this pin is grounded then the display will continue to show the results of the last valid measurement until pin 37 is released. Display hold also resets the system counters and a new measurement begins immediately display hold is released. The method of activating display hold depends on whether or not the on-chip reference and shunt regulator are being utilised.

If an external reference voltage is used (pins 35 and 37 not joined) then display hold can be activated by grounding pin 37 with a single-pole switch, transistor or open-collector logic gate, provided that the external reference is not required to supply other circuits. If the on-chip regulator is to be used then pin 35 must, of course, be biased up with an external 22k resistor so that V_{REF} can supply the reference voltage for the regulator. If the on-chip reference is used but the on-chip regulator is not then display hold can be activated in a similar manner by grounding the junction of pin 35 and pin 37.

However, since the on-chip reference also provides the reference voltage for the on-chip regulator pin 35 must not be grounded if the regulator is in use or the supply voltage will drop to zero. If the on-chip reference and shunt regulator are both used then pin 37 must be disconnected from pin 35 before it is grounded to activate display hold. This is illustrated in fig. 11. As pin 37 normally supplies the bias current for the on-chip reference this must be provided by an external 22k resistor when these pins are not linked.

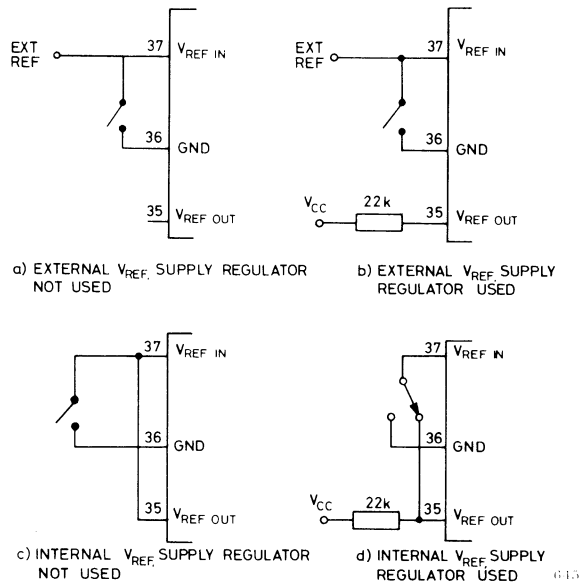


Fig. 11 Display Hold Options

BACKPLANE OUTPUT

The backplane output normally supplies a squarewave of the same frequency as, but 180° out of phase with, the active segment outputs. This provides the necessary a.c. drive to the L.C. display. By grounding the backplane output the a.c. drive to the segments may be inhibited and the segment outputs become normal active low (TRUE = 0) outputs. This facility is useful if the output data is to be used for some purpose other than display driving. An L.C. display should not be connected to the ZN451 in this condition as d.c. drive will eventually damage it.

DECIMAL POINT DRIVE

The ZN451 provides all the output necessary to drive the segments of a 3½ digit liquid crystal display. However, in order to drive decimal points and annunciators such as low battery indicators, some external components are required. To turn on a decimal point it is necessary to provide it with a drive signal of the same frequency as, but 180° out of phase with, the backplane output. For driving a single, fixed decimal point, the simple inverter circuit of figure 12a can be used.

If more than one decimal point is to be selected then it is necessary for the unused decimal points to be switched off by arranging their drive waveforms to be in phase with the backplane output. This is simply achieved using exclusive OR gates as shown in figure 12b.

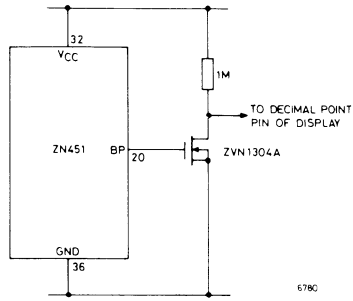


Fig. 12a Driving a Fixed Decimal Point

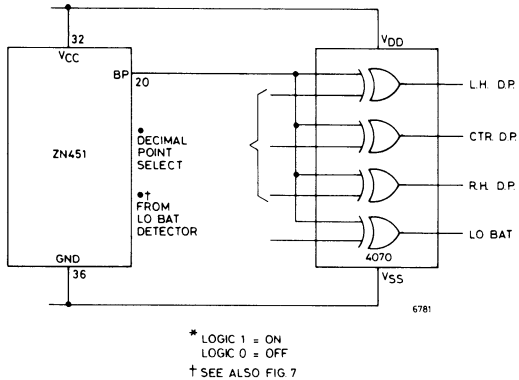


Fig. 12b Decimal Point Select and 'LO BAT' Indicator Drive using Exclusive OR Gates

A logic '1' on the input causes the output waveform to be out of phase with the backplane and the appropriate decimal point is activated. Conversely a logic '0' causes the output to be in phase with the backplane. A single 4070 CMOS quad-EXOR gate I.C. will provide the drive for the three decimal points of a 3½ digit liquid crystal display plus the drive to a low battery indicator. A suitable low battery detection circuit is shown in fig. 7d.

CALCULATION OF FULL-SCALE RANGE

The component values for any full-scale range depend on the input switching method used. Using method (a) the input voltage is measured only during phase 2, so the equation $\frac{NV_{IN}R_{REF2}}{V_{REF}R_{REF1}} = N_1 - \frac{N}{2}$ holds.

Since N = 5000 and full-scale reading = ± 1999 this equation can be rewritten as

$$V_{IN}\ (\text{full-scale}) = \frac{\pm 1999\ V_{REF}R_{REF1}}{5000\ R_{REF2}}$$

$$\frac{\pm 0.4\ V_{REF}R_{REF1}}{R_{REF2}}$$

from which required values of R_{REF1} and R_{REF2} can be calculated for any required full-scale input voltage, using either the internal reference of 1.3V or an external reference.

Using input switching method (b) the input voltage is measured during both phases so the displayed count is twice as large for the same input voltage and component values.

The describing equation thus becomes

$$V_{IN}\ (\text{full scale}) = \frac{\pm 0.2\ V_{REF}R_{REF1}}{R_{REF2}}$$

Using input switching method (b) the same full-scale range as method (a) can be obtained if the value of R_{REF1} is doubled or the input signal is attenuated by a factor of two.

These equations are in fact not exact since they do not take account of the reference amplifier offset voltage, which is typically ± 5mV. This offset means that I_{REF} is not precisely $\frac{V_{REF}}{R_{REF2}}$ of r_e of T_1 and T_2 in the voltage-current converter also appears in series with R_{REF2} (typically 5k). In practice this is not a problem since the tolerance of the on-chip reference means that a calibration adjustment must be provided anyway. Using the on-chip reference voltage of 1.26-1.35 volts the recommended component values for a full-scale reading of 199.9mV would be R_{REF1} = 200k or 400k, R_{REF2} = 500k (min.), 520k (max.). Allowing for the use of 2% tolerance components for R_{REF1} and R_{REF2} an adequate adjustment range for calibration purposes will be provided if R_{REF2} is made up of a 470k resistor in series with a 100k multiturn trimmer. Full-scale ranges less than 200mV can be accommodated by reducing the value of R_{REF1}, thus producing the same full-scale input current for a smaller input voltage. The limitations on the minimum value of R_{REF1} are caused by non-linearity in the voltage-current converter, offsets in the auto-zero switches, and the fact that r_e becomes a much larger proportion of R_{REF1}. These factors place a practical limit of about 20k on R_{REF1}. As R_{REF1} is reduced, the gain temperature coefficient will also tend to increase.

Similarly full-scale ranges greater than ± 200mV can be accommodated by increasing the value of R_{REF1}. The maximum input voltage that can be applied is limited by the common-mode range of the differential inputs.

The full-scale range can also be adjusted by varying R_{REF2} which determines the reference current, and indeed placing a preset in series with R_{REF2} is the recommended method of calibration.

I_{REF} can also be varied by using an adjustable external reference voltage instead of the internal reference, which makes ratiometric operation possible.

The maximum value of I_{REF} is limited to about 3μA since above this value the voltage-current converter becomes non-linear. The minimum value of I_{REF} is not quite so well defined as it is determined by deterioration in the performance of current switches T_3 and T_4 at low collector currents. The minimum useable value of I_{REF} is typically 500nA. This means that the upper and lower limits are $\frac{V_{REF}}{500nA}$ and $\frac{V_{REF}}{3\mu A}$ respectively. The upper and lower limits on V_{REF} itself are determined by the common-mode range of the reference current amplifier A_1 which is 1 to 1.5V. Radiometric operation with a variable V_{REF} within these limits is possible provided that the upper or lower limit of I_{REF} is not exceeded.

PRACTICAL APPLICATIONS AND DESIGN PRECAUTIONS

Since the input switching of the ZN451 is external to the device it is possible to include op-amps and other signal conditioning circuits within the auto-zero loop and thus eliminate their zero errors.

The two methods of input switching are shown in figs. 13a and 13b. In fig. 13a a series switch and shunt switch disconnect the input signal during phase 1. In fig. 13b a switch bridge reverses the polarity of the input signal during phase 1.

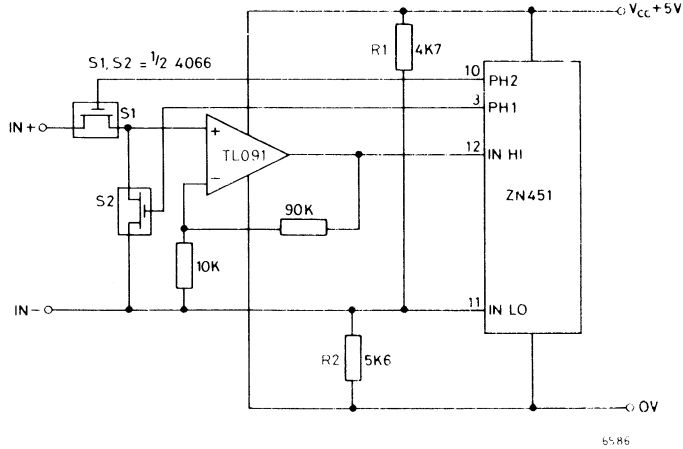


Fig. 13a

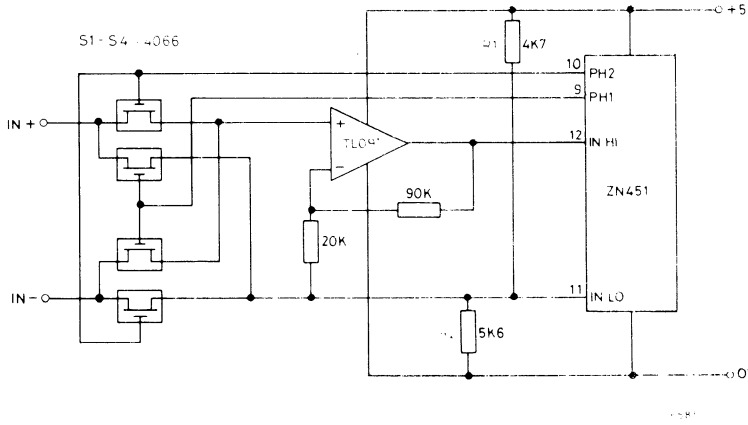


Fig. 13b

Two practical circuits for 20mV full-scale DVM are given in figs. 13a and 13b. In the circuit of fig. 13b note that the gain of the op-amp is 5 since the effective full-scale sensitivity of the ZN451 is 100mV, whereas in fig. 13a it is 200mV. The same result could be achieved by making the op-amp gain 10 in both cases but doubling the value of R_{REF1} in fig. 13b.

These simple circuits can be used to illustrate some design precautions that must be observed when using the ZN451.

1) The output voltage of the signal conditioning circuits should be within the common-mode range of the ZN451.

2) The common-mode and differential input voltages must be within the input range of the switches and signal conditioning circuits.

These two criteria are met in figs. 13a and 13b by providing an analogue common point at approximately +2.5V by means of R_1 and R_2. Assuming battery operation of the ZN451 this analogue common point will float up and down with the common mode voltage of the input signal thus keeping the input voltage within the common-mode range of ZN451 and the input circuits.

3) The offset error at the input of the ZN451, when added to the full-scale input voltage, must not cause saturation of the DSM. Using input switching method (b) this means that the zero error can be 150% of the full-scale range of the DVM.

When designing signal conditioning circuits care must be taken to ensure that this limit is not exceeded.

In many circuits the principal source of zero error will be the offset voltage of the op-amp, in which case a good rule of thumb is that the input offset voltage should not exceed the full-scale input voltage, to allow some overload margin to be retained.

However, in some signal conditioning circuits there may be sources of zero error other than the op-amp, in which case care must be taken to meet the offset criteria at the ZN451 inputs. An example of such a circuit is given in fig. 15.

Using low-cost monolithic op-amps it is a simple matter to design for full-scale inputs of ±20mV or less. For inputs below 2mV more expensive instrumentation amplifiers must be used. Alternatively the offset can be nulled out when calibrating the DVM, leaving the auto-zero to cope with long-term and temperature drift of the zero.

4) There should be no rapid temperature fluctuations in the signal conditioning circuits as this could cause the zero error to vary from phase 1 to phase 2.

Example, with full-scale input of 1.999mV and an op-amp with an offset tempco of 10μV/°C a 0.1°C change in temperature between phase 1 and phase 2 will cause a zero error of 1μV = 1 count.

This is likely to be a problem only with very small full-scale ranges. It can be reduced by thermally insulating the signal conditioning circuits or by plotting them to increase the thermal inertia so that the temperature can only change slowly.

5) With very small input voltages thermal e.m.f.'s may become a problem. In this case care should be taken to ensure that the input + and input − signal paths to the signal conditioning circuits are identical so that thermal e.m.f.'s cancel out. Such precautions may include the use of identical input switches in series with both the input + and input − leads.

Although fig. 13b shows the simplest way of implementing input switching method (b), using only one op-amp, this configuration may have disadvantages in some applications, since the input LO terminal of the ZN451 is tied permanently to analogue common, whilst the input voltage is reversed. This means that the supply rails of the ZN451 shift up and down with respect to the input signal common. This is generally not a problem in battery-powered circuits unless the signal source impedance is very high, when charging and discharging of stray capacitance may cause errors.

Fig. 14 shows a circuit in which the signal 0V is connected to a fixed analogue common whilst the inputs of the ZN451 are reversed. In order that the input impedanced seen by the signal is the same during both measurement phases both inputs of the ZN451 are driven from identical op-amp circuits. These are shown as voltage followers but can be given greater than unity gain by adding the dotted components.

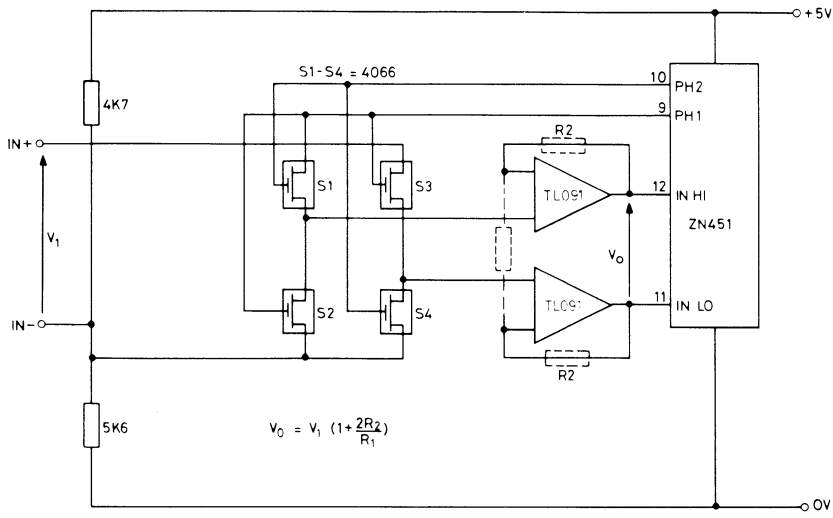


Fig. 14

In some systems it may be necessary for analogue common to be the 0V supply rail or some other voltage not within the common-mode range of the ZN451.

This can be achieved by offsetting the output voltage of the signal-conditioning circuits to bring it within the common-mode range of the ZN451. Also if the input voltage falls outside the V_{CC} and 0V rails of the ZN451 the supply voltage to the analogue switches must be such that they can accommodate the signal, and the PH_1 and PH_2 outputs of the ZN451 must be level-shifted in order to control the switches. An example of such a circuit is shown in fig. 15. This is a $\pm$200mV DVM operating from $\pm$5V with the 0V rail as analogue common.

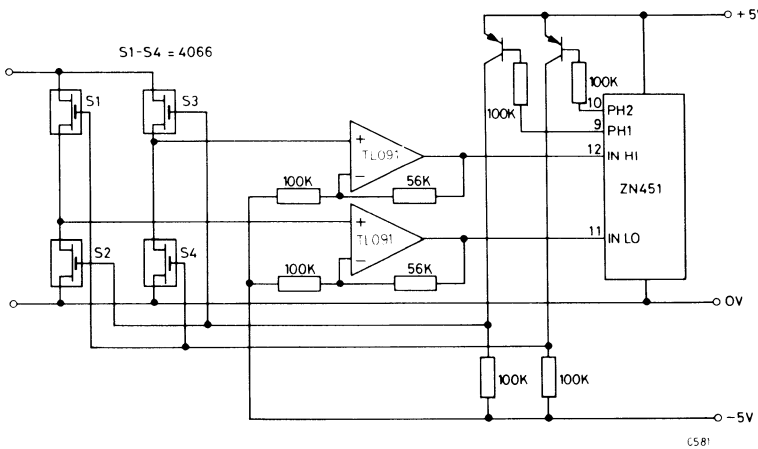


Fig. 15

The ZN451 operates from the +5V and 0V rails whilst the input switches and op-amps operate from ±5V. Two PNP transistors convert the 0 to +5V swing of the PH_1 and PH_2 outputs to a ±5V swing. Since they also invert the outputs the PH_1 and PH_2 outputs are transposed.

The two op-amps are connected in a non-inverting configuration but with the feed-back network returned to −5V instead of 0V. By making the op-amp gain 1.56 this gives an offset of approx. +2.8V with a 0V input which brings the output within the common-mode range of the ZN451.

Since the op-amp gain is 1.56 the values of R_{REF1} and R_{REF2} must be chosen for ±312mV full-scale to give a full-scale input range of ±200mV.

In this circuit there are two sources of zero error for which the ZN451 must compensate: firstly the offset voltages of the two op-amps multiplied by their gain; secondly and more significant the difference in the quiescent op-amp output voltages caused by gain mismatching between the two op-amps.

$$\pm \{5 \times (\text{max. gain } A_1 - \text{min. gain } A_2)\}$$
$$= \pm \left\{5 \times \left(\frac{98 + 57}{98} - \frac{102 + 55}{102}\right)\right\}$$
$$= \pm 212\text{mV}$$

This is 68% of the full-scale input range of the ZN451, which is acceptable.

ADDITIONAL INPUT CONDITIONING

For use in a multirange instrument such as a DVM, additional signal conditioning circuits will be required for the measuring of a.c. and d.c. voltages, a.c. and d.c. current, and resistance. Some suggested circuits are shown on the following pages.

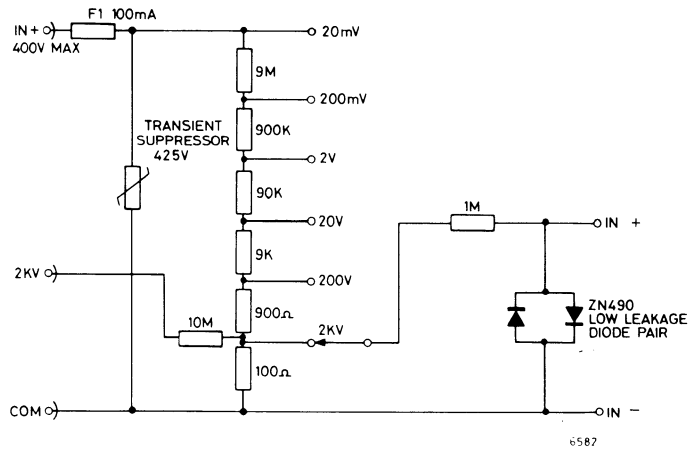


Fig. 16

Fig. 16 shows an input attenuator for the measurement of voltages from 20mV to 2kV. This has a standard input resistance of 10M.

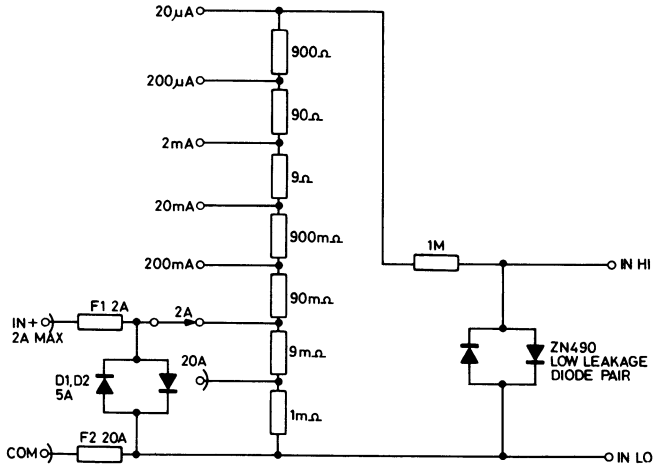


Fig. 17

Fig. 17 shows a universal shunt for the measurement of currents from 20μA to 20A with a full-scale voltage drop of ±20mV.

Resistance can be measured by passing a known, constant current through an unknown resistor and measuring the voltage drop across it.

An ohmmeter circuit is given in fig. 18.

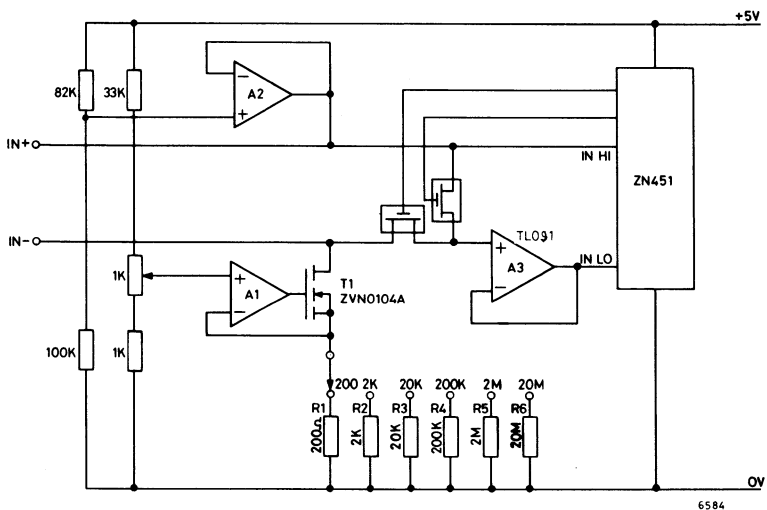


Fig. 18

Op-amp A_1 and Mosfet T_1 form a constant current sink whose output current is defined by resistors R_1-R_6 and a reference voltage derived from the stabilised +5V rail.

Op-amp A_2 provides a low impedance analogue common point which can source the current from the +5V rail without its voltage changing. The maximum full-scale voltage drop across the resistor under test is 200mV.

A.C. MEASUREMENTS

To measure a.c. voltage or current it is first necessary to convert it into a proportional d.c. voltage. The simplest way to do this is to interpose a precision active rectifier circuit between the attenuator or shunt and the inputs of the ZN451. Such a circuit produces d.c. voltage proportional to the mean of the rectifier voltage rather than a true R.M.S. result and for true R.M.S. measurements an R.M.S. converter must be used. The rectifier can be calibrated to read R.M.S. but the result is true only if the input signals have a constant form factor.

A simple precision rectifier circuit is shown in fig. 19. It is completely a.c. coupled throughout by C_2, C_3 and C_4, so the offset voltage of A_1 does not appear at the output and no zero adjustment is required. To prevent the offset voltage of A_1 causing it to saturate in the absence of an input signal, 100% d.c. feedback is provided by R_3.

R_1 and R_2 provide a d.c. bias path for the non-inverting input of A_1, whilst C_2 provides boot-strapping to increase the a.c. input impedance.

Amplifier A_2 is a voltage follower biased into the middle of the ZN451's common-mode range to provide a low impedance analogue common point. The output of the rectifier is connected to a lowpass filter comprising R_6 and C_5. These components are chosen to give a time constant of 300ms which allows input frequencies down to 40Hz whilst maintaining an acceptably short response time.

With the component values shown the circuit is calibrated to read R.M.S. for sine-wave input, so the use of this waveform will be assumed throughout.

The circuit functions as follows: when the input signal crosses zero in a positive going direction the output of A_1 slews positive until D_2 conducts, after which the voltage at point A is defined by the equation: $V_A = G\ V_{IN}$, where G is the gain defined by R_4 and R_5 shunted by R_2.

This voltage attempts to charge up C_5 via R_6 in a positive direction.

When the signal crosses zero in a negative-going direction the output of A_1 slews negative until D_1 conducts, after which the output voltage at point B is equal to (minus) V_{IN}. This voltage attempts to charge up C_5 in a negative direction via R_4 and R_6.

When the circuit has reached equilibrium there will be a constant d.c. voltage (V_C) on C_5 with negligible a.c. ripple (otherwise it could not be measured by the DVM without flicker of the display).

This means that the mean current flowing into C_5 during the positive half-cycle must exactly equal that flowing out of C_5 during the negative half-cycle.

i.e. $$\frac{V_A(\text{MEAN}) - V_C}{R_6} = \frac{-V_B(\text{MEAN}) + V_C}{R_6 + R_4}$$

Now the mean value of a rectifier sinewave is 0.9 times the R.M.S. value therefore

$V_A(\text{MEAN}) = 0.9.G.\ V_{IN\ (RMS)}$

and $V_B(\text{MEAN}) = -0.9\ V_{IN\ (RMS)}$

For the DVM to read correctly V_C must equal $V_{IN\ (RMS)}$

therefore $V_A = 0.9.G.V_C$

and $V_B = -0.9.V_C$

thus $$\frac{V_C(0.9G - 1)}{R_6} = \frac{1.9V_C}{R_6 + R_4}$$

$$\frac{0.9G - 1}{R_6} = \frac{1.9}{R_6 + R_4}$$

R_4 and R_6 can be chosen arbitrarily provided that the values are "sensible", and that the time constant R_6, C_5 is correct.

Therefore, choosing a value of 200k for R_6 and 10k for R_4 and substituting these values in the above equation.

$$\frac{0.9G-1}{200} = \frac{1.9}{21.0}$$

$$189G - 210 = 380$$

$$G = \frac{590}{189}$$

$$= 3.122$$

Therefore the value of the parallel combination of R_5 and R_2 is 4.712k. Since $R_2 = 1M$ $R_5 = 4.73k$.

Using the component values shown the circuit is accurate at about $\pm 1.5\%$ over the frequency range 40Hz to 1KHz.

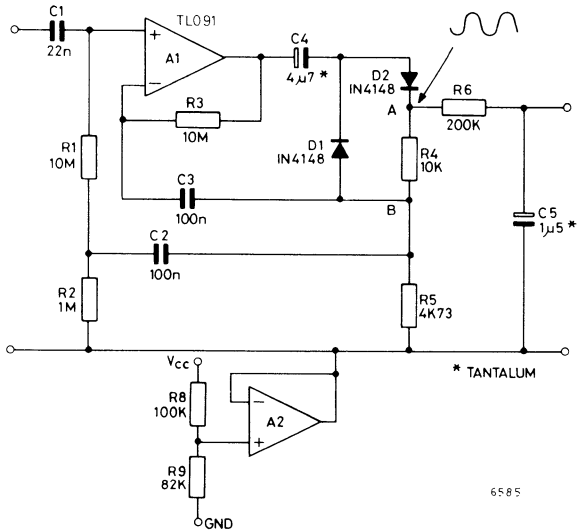
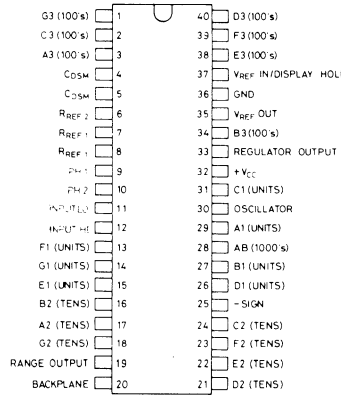
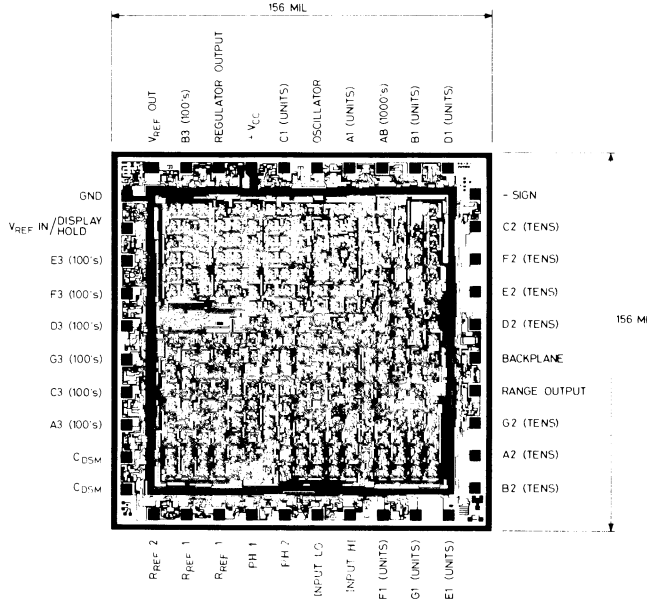


Fig. 19

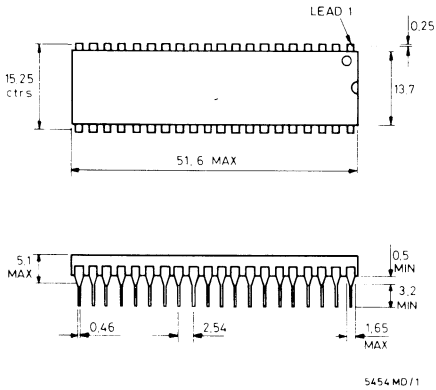
PIN CONNECTIONS



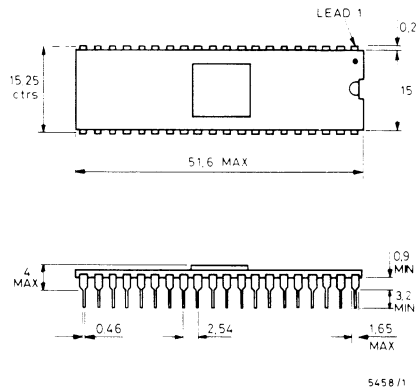
CHIP DIMENSIONS AND LAYOUT



PACKAGE DETAILS



ZN451E
40 Lead Moulded D.I.L.



ZN451CJ
40 Lead Ceramic D.I.L.

ORDERING INFORMATION

Type Number	Package	Operating Temperature Range
ZN451E	Plastic	0 to +70°C
ZN451CJ	Ceramic	0 to +70°C

ZN501
ZN502

FERRANTI semiconductors

10 Bit ADC μP-compatible, Tristate

ADVANCE PRODUCT INFORMATION

FEATURES

- **Choice of linearity: ½LSB-ZN501, 1LSB-ZN502**
- **3-state outputs, TTL compatible**
- **15μS typical, 20μS guaranteed conversion time**
- **Input range as desired**
- **+5V, −5V supplies, microprocessor and TTL/CMOS compatible**
- **Choice of commercial or military temperature range**
- **Full 8- or 16-bit MICRO-Bus interface**
- **Available in ceramic or moulded package**
- **Asynchronous Start Converter**

DESCRIPTION

The ZN501 and ZN502 range of successive approximation A to D converters combine several inovations to provide this function on a fully monolithic silicon integrated circuit. The chip consists of a current switching array (requiring no trim), successive approximation logic, 2.5V precision reference, reference amp, comparator and 3-state output buffers.

With the aid of $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 the 10 bits of O/P data can be read as a 10-bit word or as 8- and 2-bit words.

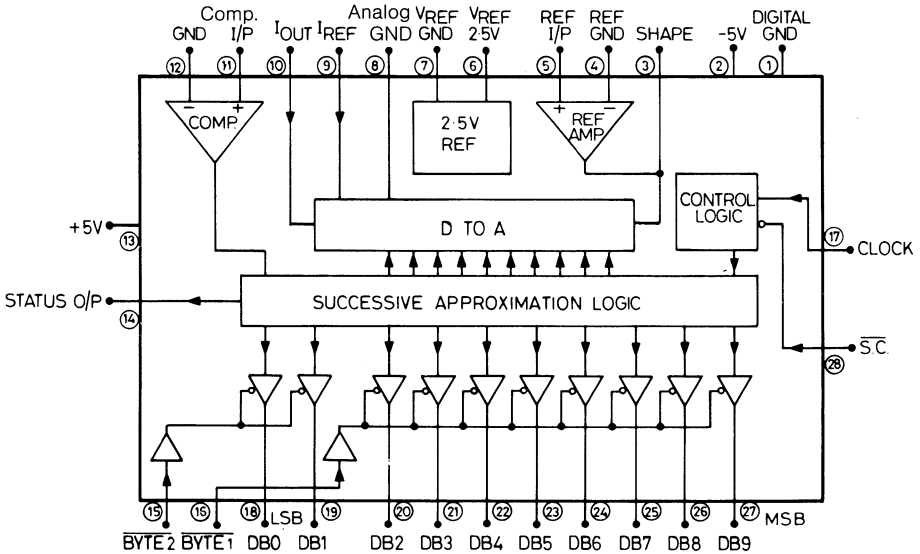


Fig. 1 System Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC+} .. .. +7 volts
V_{CC-} .. .. −7 volts
Logic Input Voltage .. .. $+V_{CC}$ and 0 volts
Operating Temperature Range .. .. .. 0 to 70°C ('E' package)
0 to +70°C ('CJ' package)
−55 to +125°C ('AJ' package)
Storage Temperature Range .. .. −55 to +125°C

ELECTRICAL CHARACTERISTICS (at +5 and −5 volts supplies and internal reference unless otherwise stated).

Parameter	Version	T_{amb} = +25°C Min.	Typ.	Max.	Over Spec Min.	Max.	Units	Conditions
	ZN501							Cer. AJ. Cer. CJ.
Linearity error				±0.5		±0.5	LSB	
Diff. linearity error				±0.5		±0.5	LSB	Note 1
Unipolar offset			±0.55	±1.0		±1.0	LSB	Ext. Ref.
			±0.55	±1.0		±1.0	LSB	Int. Ref.
Bipolar offset			±0.55	±1.0		±1.0	LSB	Ext. Ref.
			±0.55	±1.0		±1.0	LSB	Int. Ref.
Gain error			±0.55				LSB	Ext. Ref.*
			±3				LSB	Int. Ref.*
TEMPERATURE COEFFICIENTS (T_{min} to T_{max})								
Unipolar offset			7 typ., 10 max.				ppm/°C	Ext. Ref.
			7 typ., 10 max.				ppm/°C	Int. Ref.
Bipolar offset			7 typ., 10 max.				ppm/°C	Ext. Ref.
			7 typ., 10 max				ppm/°C	Int. Ref.
Gain			10 typ.				ppm/°C	Ext. Ref.
			50 typ.				ppm/°C	Int. Ref.
	ZN502							Cer. AJ. Cer. CJ.
Linearity error				±1.0		±1.0	LSB	
Diff. linearity error				±0.5		±0.5	LSB	Note 1
Unipolar offset			±0.55	±1.0		±1.0	LSB	Ext. Ref.
			±0.55	±1.0		±1.0	LSB	Int. Ref.
Bipolar offset			±0.55	±1.0		±1.0	LSB	Ext. Ref.
			±0.55	±1.0		±1.0	LSB	Int. Ref.
Gain error			±0.55				LSB	Ext. Ref.*
			±3				LSB	Int. Ref.*

*See Note 4

ELECTRICAL CHARACTERISTICS *(Continued)*

Parameter	Version	T_{amb} = +25°C Min.	Typ.	Max.	Over Spec Min.	Max.	Units	Conditions
TEMPERATURE COEFFICIENTS (T_{min} to T_{max})								
Unipolar offset			15 typ., 20 max.				ppm/°C	Ext. Ref.
			15 typ., 20 max.				ppm/°C	Int. Ref.
Bipolar offset			15 typ., 20 max.				ppm/°C	Ext. Ref.
			15 typ., 20 max.				ppm/°C	Int. Ref.
Gain			20 typ.				ppm/°C	Ext. Ref.*
			50 typ.				ppm/°C	Int. Ref.*
	ZN502E	Parameter values as for ZN502						Plas. E.
	All types							
Resolution		10	–	–	–	–	bits	
Conversion time min.		10	15	20	15	20	μS	Note 2
DAC reference I_{ref}		0.25	0.5	1.0	0.25	1.0	mA	Note 5
Nominal analogue input range		−2.5	–	+2.5	–	–	volts	Note 3
Supply rejection		–	0.1				% per V	
Supply voltage $+V_{CC}$		+4.5	+5	+5.5	+4.5	+5.5	volts	
$-V_{CC}$		−4.5	−5	−5.5	−4.5	−5.5	volts	
Supply current $+I_{CC}$		–	30	36			mA	$+V_{CC}+5V$
$-I_{CC}$		–	21	28			mA	$-V_{CC}-5V$
Power consumption		–	300	360			mW	
INTERNAL VOLTAGE REFERENCE								
Output voltage	All types		2.480				volts	
Output voltage TOLERANCE	ZN501AJ ZN501CJ			±3.0			%	
	ZN502AJ ZN502CJ			±5.0			%	
	ZN502E			±5.0			%	
V_{REF} temp. coeff.	All types	–	–	–	26	50	ppm/°C	
Slope impedance		–	0.75	–			ohms	
Max. load current		–	±2.0	–			mA	
LOGIC $\overline{START}$ $\overline{CONVERT}$ $\overline{SC}$	All types							
High level inpV V_{ih}		2.0	–	–	2.0	–	volts	
Low level inpV V_i				0.8	–	0.8	volts	
High level inpl I_{ih}		–	18.0				μA	$V_{CC}=\pm5.5V$ $V_{in}=5.5V$
High level inpl I_{ih}		–	8.0	–	–	–	μA	$V_{CC}\pm5.5V$ $V_{in}=2.4V$
Low level inpl I_i		–	4.0	–			μA	$V_{CC}\pm5.5V$ $V_{in}+0.4V$

*See Note 4

ELECTRICAL CHARACTERISTICS *(Continued)*

Parameter	Version	$T_{amb} = +25°C$ Min.	Typ.	Max.	Over Spec Min.	Max.	Units	Conditions
LOGIC	All types							
$\overline{BYTE}$ 1 and 2								
High level inpV V_{ih}		2.0	–	–	2.0	–	volts	
Low level inpV V_{il}		–	–	0.8	–	0.8	volts	
High level inpI I_{ih}		–	18.0	–	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 5.5V$
High level inpI I_{ih}	–		12.0	–	–	–	μA	$V_{CC} = +5.5V$ $V_{in} = 2.4V$
Low level inpI I_{il}		–	2.0	–	–	–	μA	$V_{CC} = +5.5V$ $V_{in} = 0.4V$
CLOCK	All types							
CLOCK high period		0.5					μS	
Max. clock frequency		550	730	1100	550	730	KHz	
High level inpV V_{ih}		2.0	–	–	2.0	–	volts	
Low level inpV V_{il}				0.8		0.8	volts	
High level inpI I_{ih}		–	–	25	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 5.5V$
High level inpI I_{ih}		–	–	5	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 2.4V$
Low level inpI I_{il}		–	–	3	–	–	μA	$V_{CC} = \pm 5.5V$ $V_{in} = 0.4V$
High level OPV V_{oh}	All types	2.4	–	–	2.4	–	volts	$V_{CC} = \pm 5V$
Low level OPV V_{ol}		–	–	0.4	–	0.4	volts	
High level OPI I_{oh}		–	–	-700	–	–	μA	
Low level OPI I_{ol}		–	–	2.0	–	–	mA	
Three-state DISABLE output leakage		–	–	±2.0	–	–	μA	$V_{out} = 1.3V$
$\overline{BYTE}$ input to data output delays		–	200	260	–	–	ns	
ENABLE/DISABLE								
Delay time TE1		100	220	260	–	–	ns	
TEO		60	80	100	–	–	ns	
TD1		100	120	140	–	–	ns	Note 6
TDO		30	60	100	–	–	ns	
$\overline{SC}$ pulse width		100	–	–	–	–	ns	
$\overline{SC}$ input to STATUS		–	180	–	–	–	ns	

Note 1 No missing codes over full temperature range at appropriate accuracy.

Note 2 The maximum conversion time is 20μS. This corresponds to a clock rate of 550KHz based on 11 clock periods per conversion cycle (see timing diagram). This provides an update rate of **50KHz.**

Note 3 Single polarity and other input ranges may be provided by different input resistor values.

Note 4 Gain error is trimmable to zero with the aid of R3.

Note 5 The full scale D to A output current $I_{out} = 4$ times I_{ref}. For optimum performance $I_{ref} = 0.5mA$.

Note 6 Refer to figure 9

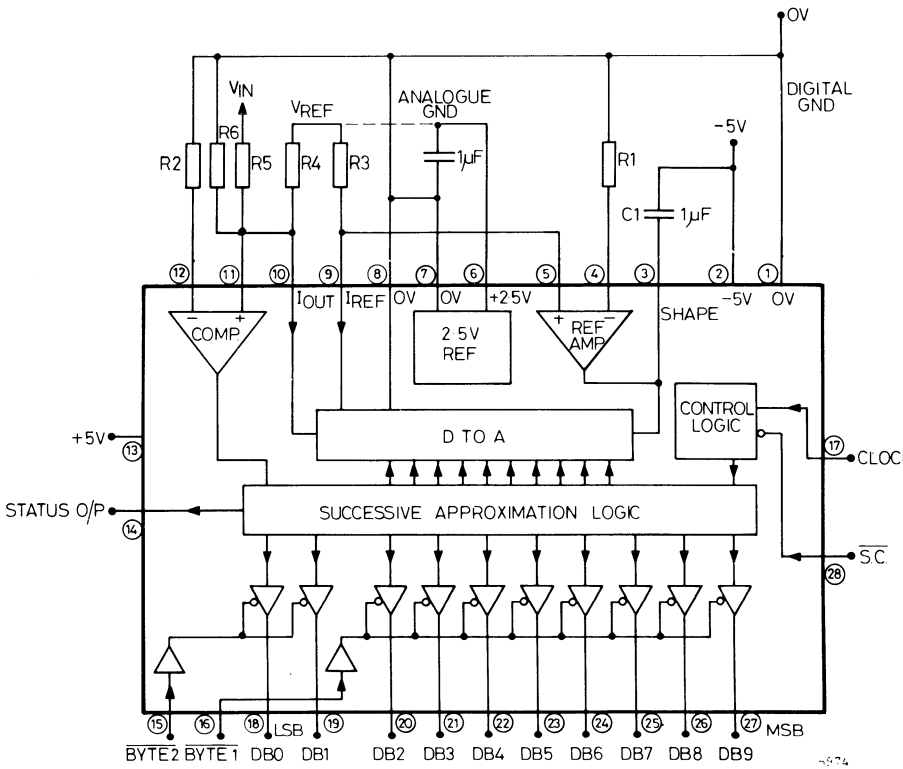


Fig. 2 Typical External Components

GENERAL CIRCUIT OPERATION

The ZN501 utilises the successive approximation technique. Upon receipt of a negative-going pulse at $\overline{SC}$ input the STATUS output goes low, and the DAC input is set to the MSB. The resulting analogue output is compared with the unknown analogue input signal by means of the comparator. So if the analogue input is the larger, the MSB is left in circuit and if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all the 10-bits have been compared. On the 11th negative clock edge STATUS goes high indicating that the conversion is complete.

During a conversion $\overline{BYTE}$ 1 and $\overline{BYTE}$ 2 will normally be held high to keep the 3-state buffers in their high impedance state. Data can be read out by taking either $\overline{BYTE}$ 1 or $\overline{BYTE}$ 2 low, thus enabling the 3-state outputs. BYTE 1 controls the 2 LSB bits and BYTE 2 controls the 8 MSB bits. Readout is non-destructive.

CONVERSION TIMING

The ZN501 will accept a low-going $\overline{\text{START CONVERT}}$ pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 10.5 and 11.5 clock pulses later depending on the relative timing of the CLOCK and $\overline{\text{START CONVERT}}$ signals.

The converter is cleared by a low-going $\overline{\text{START CONVERT}}$ pulse, which sets the most significant bit and resets all the other bits and the STATUS. Whilst the $\overline{\text{START CONVERT}}$ input is low the MSB output of the DAC is continuously compared with the analogue input, but otherwise the converter is inhibited. After the $\overline{\text{START CONVERT}}$ input goes high again the MSB decision is made and the successive approximation routine runs to completion.

The $\overline{\text{SC}}$ pulse can be as short as 100ns; however the MSB must be allowed to settle for at least (625ns) before the MSB decision is made. To ensure that this criterion is met even with short $\overline{\text{SC}}$ pulses the converter waits, after the $\overline{\text{SC}}$ input goes high, for a rising clock edge followed by a falling clock edge, the MSB decision being taken on the falling clock edge. This ensures that the MSB is allowed to settle for at least half a clock period, or (625ns) at maximum clock frequency. The clock high Period and the $\overline{\text{sc}}$ Pulse width must comply with this setting time i.e. clock high period and $\overline{\text{sc}}$ Pulse width is $\leqq$ 625 ns.

During a conversion the $\overline{\text{SC}}$ input is not locked out and if it is pulsed low at any time the conversion will restart.

At the end of a conversion STATUS waits 1 clock cycle before going high, so indicating that data is valid. So the data outputs can be enabled anytime during a conversion and valid data will be available on the rising edge of STATUS signal.

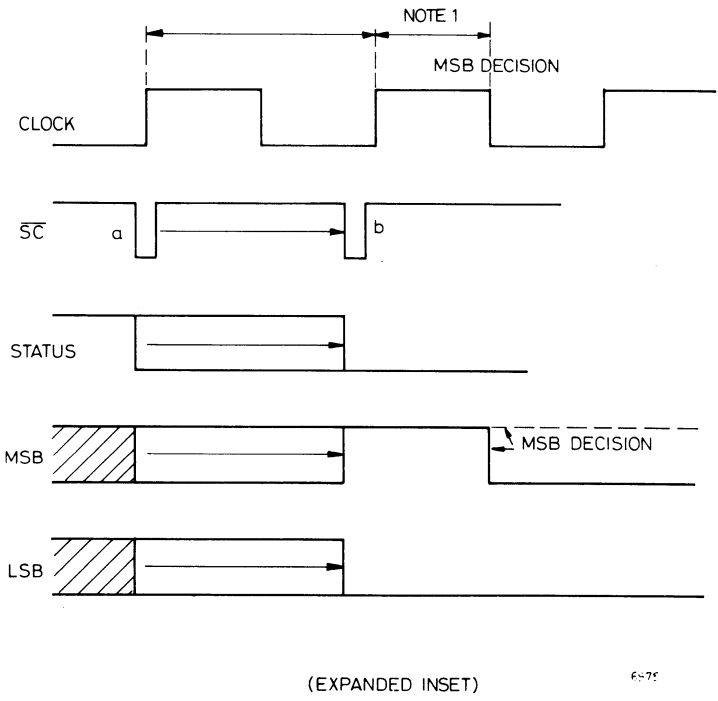


Fig. 3 Expanded Timing Diagram

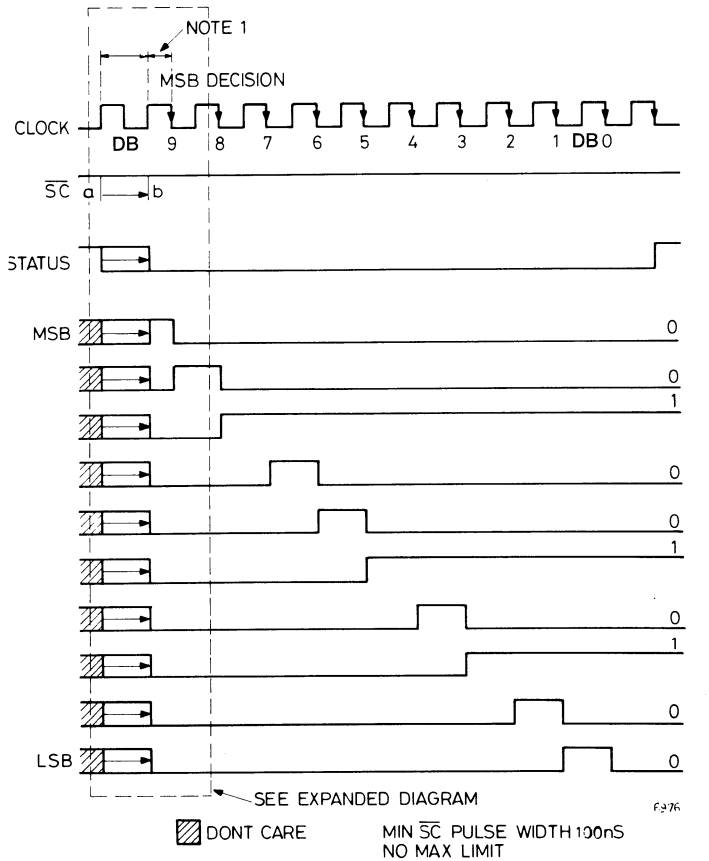


Fig. 4 Timing Diagram

CONTINUOUS CONVERSION

The converter can be made to cycle by inverting the STATUS output and feeding back to the $\overline{SC}$ input. To ensure that the converter starts reliably after power up an initial start pulse is required. This can be ensured by using a NOR gate instead of an inverter and feeding it with a positive going pulse which can be derived from a simple RC network that gives a single pulse when power is applied.

The propogation delay of the NOR gate determines the period over which STATUS remains high, during which time the data can be stored into latches. The time available for storing the data can be increased by inserting delays into the inverter path.

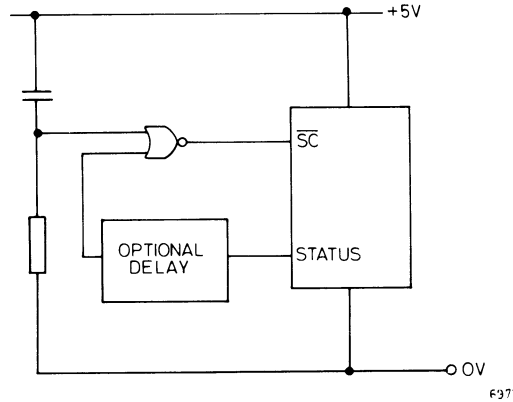


Fig. 5 Circuit for Continuous Conversion

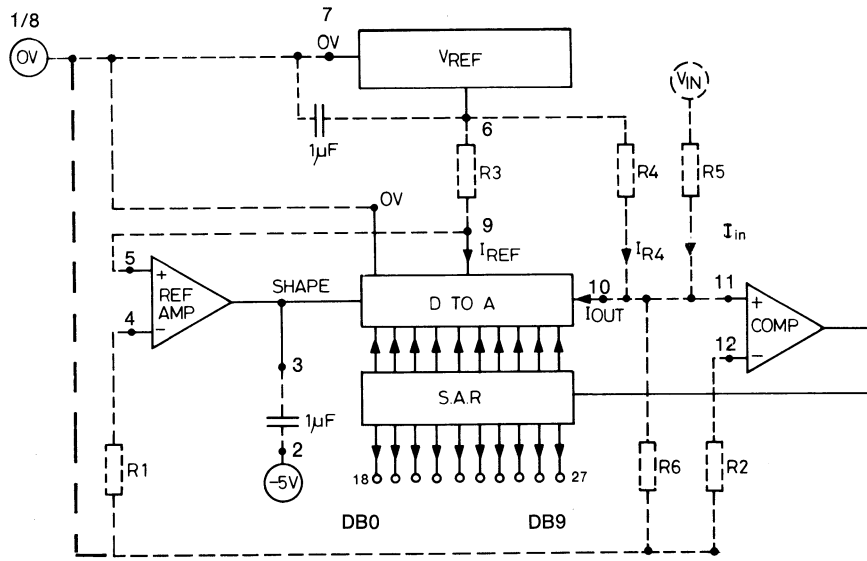


Fig. 6 External Component Connections

calculation of external Resistors

If $V_{in\ max}$ is the voltage for the logic output to be all 1's.
$V_{in\ min}$ is the voltage for the logic output to be all 0's.

$$I_{out} = I_{R4} + I_{in}$$
$$I_{out} = \frac{V_{ref}}{R4} + \frac{V_{in}}{R5}$$

$I_{out} = 0$
(when $V_{in} = V_{in\ min}$)

$$\frac{V_{in\ min}}{R5} = -\frac{V_{ref}}{R4}$$
$$R4 = \frac{-V_{ref}\ R5}{V_{in\ min}}$$

I_{out}(f.s.) = 2mA:
(when $V_{in} = V_{in\ max}$)

$$\frac{V_{in\ max}}{R5} + \frac{V_{ref}}{R4} = I_{out}(f.s.)$$
$$-\frac{V_{in\ min}}{R5} + \frac{V_{in\ max}}{R5} = I_{out}(f.s.)$$
$$R5 = \frac{V_{in\ max} - V_{in\ min}}{I_{out}(f.s.)}$$

It is important for gain stability that I_{out}(f.s.) of 2mA be kept constant, and this is done by the reference amplifier loop.

The current sources in the D to A itself cannot be checked directly so a number of references current sources are distributed across the chip to monitor conditions all along the array.

$$\text{So } I_{ref} = 0.5\text{mA}$$
$$R3 = \frac{V_{ref}}{0.5\text{mA}}$$

I_{out}(f.s.) is four times I_{ref}.

R3 can affect gain stability and thus requires to be of high quality.
(Also slight variation in its value can act as a gain control).

R4 and R5 can affect offset stability and thus requires to be of high quality.
(Also slight variations in the value of R4 value can act as a offset control).

R1 and R2 are to supply the bias current of the reference amplifier and comparator.

$$\text{So} \quad R1 = R3$$
$$\text{and} \quad R2 = \text{parallel combination of R4, R5 and R6}$$

R6 should be chosen such that the parallel combination of R4, R5 and R6 is about 1.25Kohms as this determines the D to A time constant and hence conversion time.

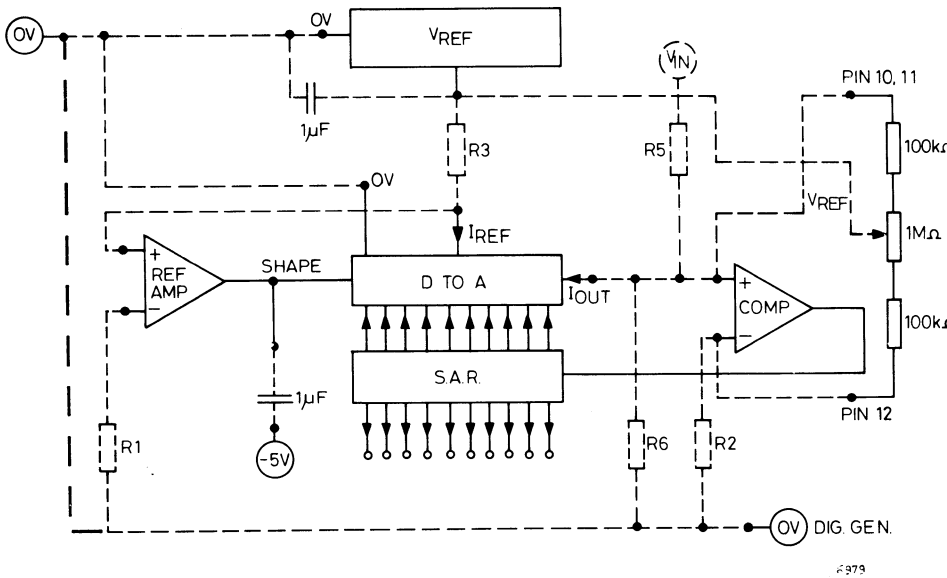
(THE FOLLOWING IS A TABLE OF VALUES TO GIVE EXAMPLES OF THE ABOVE EQUATIONS):

$V_{in\ max}$	$V_{in\ min}$	V_{ref}	R1 (1)	R2 (1)	R3	R4	R5	R6 (1)
+2.5	−2.5	2.5	5K	1.25K	5K	2.5K	2.5K	∞
+2.5	−2.5	5*	10K	1.25K	10K	5.0K	2.5K	5.0K
+2.5	0	2.5	5K	1.25K	5K	∞	1.25K	∞
+5.0	0	2.5	5K	1.25K	5K	∞	2.5K	2.5K
+4.0	−2.0	2.5	5K	1.25K	5K	3.75K	3.0K	5.0K
+4.0	−2.0	12*	24K	1.25K	24K	3.75K	3.0K	5.0K
+10	−10	2.5	5K	1.25K	5K	2.5K	10K	3.33K
+10	0	2.5	5K	1.25K	5K	∞	5K	1.66K

Note 1 Nearest prefered value may be used for R1, R2 and R6.

*Note 2 External reference.

For unipolar operation where R4 approaches (∞) and a zero adjustment is required, the following offset circuit is suggested in place of R4.



– – – – – External Components and Wiring

Fig. 7 Offset Circuit for Unipolar Operation

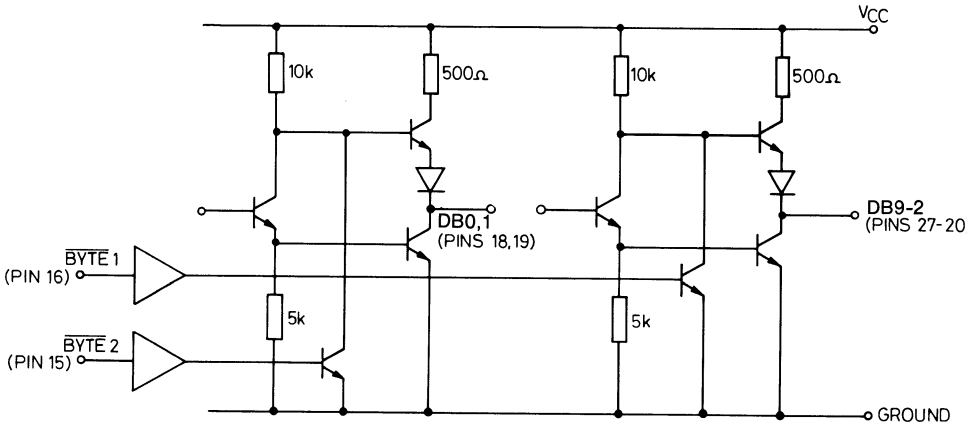
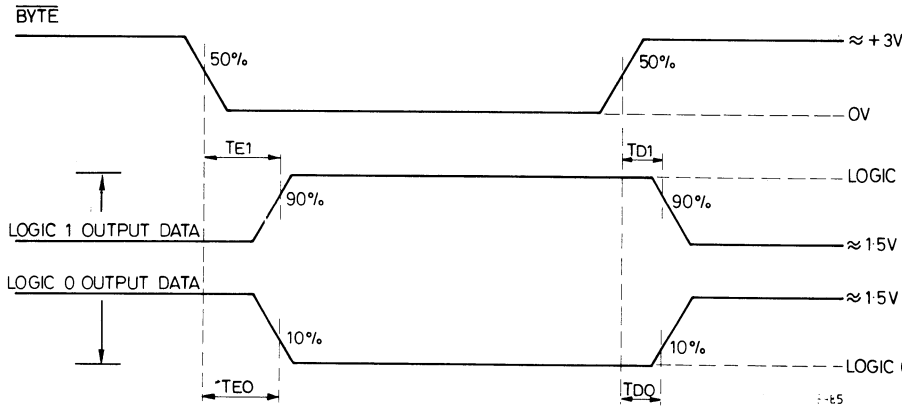


Fig. 8 Data Outputs



TE = BYTE ENABLE DELAY TIME (CL = 50pF)
TD = BYTE DISABLE DELAY TIME (LL = 10pF)

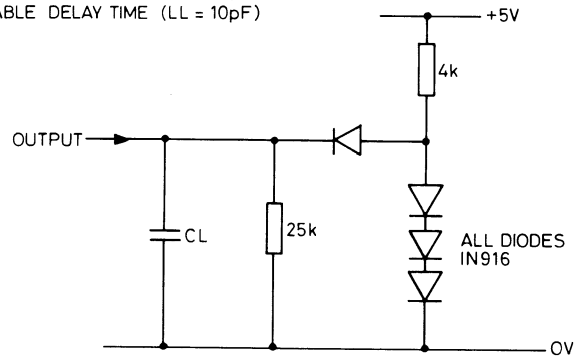


Fig. 9 Output Enable/Disable Delays

DATA OUTPUTS

The ZN501 has true 3-state output buffers on chip, hence eliminating the need for external buffers and latch circuitry.

The two $\overline{\text{BYTE}}$ select pins $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2, control outputs DB9 to DB2, and outputs DB1 to DB0 respectively.

$\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 will normally be held high during a conversion to keep the TRI-state buffers in their high impedance state, and when data is ready, which will be signalled by a high going STATUS pulse, it can easily be read out by taking $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 low.

(A test circuit and timing diagram for the output enable/disable delays are given).

The STATUS output shown utilises a 5K internal pullup resistor for CMOS/TTL compatibility.

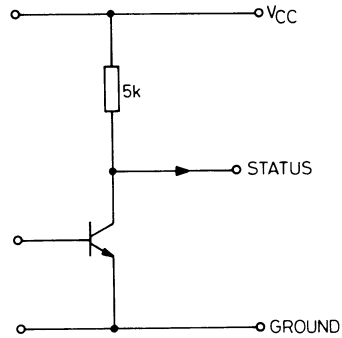


Fig. 10 Status Output

DATA BUS CONNECTIONS

The ZN501 can be connected directly, to an 8-bit microprocessor bus, where the two LSB's would normally be hardwired to the desired upper bits, usually the 2 MSB's. Hence the data would be transferred in two words with control of them, from $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2.

For use with a 16-bit microprocessor, $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 would be tied together and all 10 bits would be enabled simultaneously. The 10-bit word could then be placed, at either the higher or lower end of the 16-bit bus.

e.g.

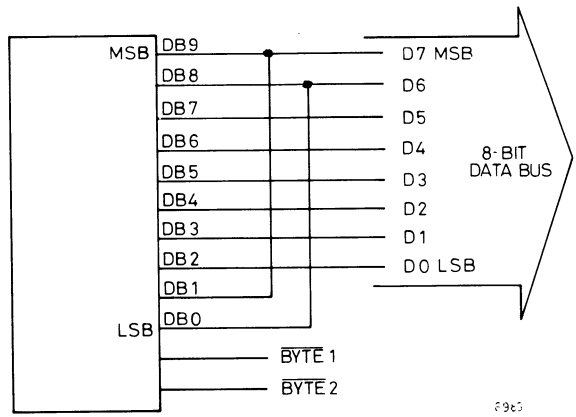


Fig. 11 Data Bus Connections

$\overline{\text{BYTE}}$ 1	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2
	D7	D6	D5	D4	D3	D2	D1	D0
$\overline{\text{BYTE}}$ 2	DB1	DB0	X	X	X	X	X	X

DATA TRANSFERRED IN TWO WORDS

UNIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous $\overline{\text{START CONVERT}}$ pulse at intervals long enough to allow a complete conversion and monitor the digital outputs.

OFFSET SETTING

(ii) Apply ½LSB to V_{in} and adjust the offset CIRCUIT until DB0 (LSB) just flickers between 0 and 1 with all the other bits at 0.
i.e. for transition 0000000000 to 0000000001.

GAIN SETTING

(iii) Apply full-scale minus 1.½LSB to V_{in} and adjust gain until DB0 (LSB) just flickers between 0 and 1 with all other bits at 1.
i.e. for transition 1111111111 to 1111111110.

Note: R3 GAIN ADJUSTMENT.

UNIPOLAR SETTING-UP POINTS

Input Range +FS	½LSB	F.S. − 1.½LSB
+2.5V	1.22mV	2.4963V
+5.0V	2.441mV	4.9926V

$1\text{LSB} = \frac{FS}{1024}$

UNIPOLAR LOGIC CODING

Analogue Input (Nominal Code Centre Value)	Digital Output Code MSB LSB
FS - 1LSB	1111111111
FS - 2LSB	1111111110
¾.FS	1100000000
½. + LSB	1000000001
½.FS	1000000000
½.FS - 1LSB	0111111111
¼.FS	0100000000
1LSB	0000000001
0	0000000000

BIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous $\overline{\text{START CONVERT}}$ pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

OFFSET SETTING

(ii) Apply −(FS - ½.LSB) to V_{in} and adjust offset control until DB0 (LSB) output just flickers between 0 and 1 with all other bits at 0.
i.e. for transistions 0000000000 to 0000000001.

Note: R4 OFFSET ADJUSTMENT.

GAIN SETTING

(iii) Apply +(FS - 1½.LSB) to V_{in} and adjust gain until DB0 (LSB) just flickers between 0 and 1 with all other bits at 0.
i.e. for transition 1111111111 to 1111111110.

Note: R3 GAIN ADJUSTMENT.

BIPOLAR SETTING-UP POINTS

Input Range ±FS	−(FS − ½.LSB)	+(F.S. − 1.½.LSB)
±2.5V	−2.4976V	+2.4927V
±5.0V	−4.9951V	+4.9854V

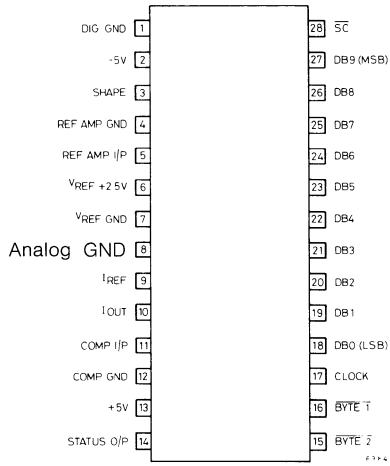
$$1\text{LSB} = \frac{2FS}{1024}$$

BIPOLAR LOGIC CODING

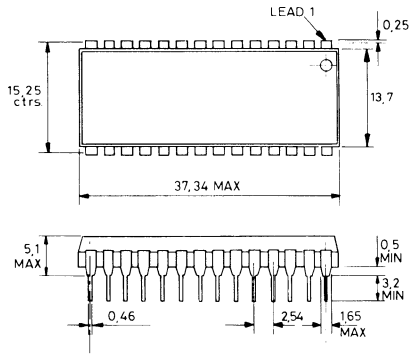
Analogue Input (Nominal Code Centre Value)	Digital Output Code MSB LSB
+(FS - 1LSB)	1111111111
+(FS - 2LSB)	1111111110
+(½.FS)	1100000000
+(1LSB)	1000000001
0	1000000000
−(1LSB)	0111111111
−(½.FS)	0100000000
−(FS - 1LSB)	0000000001
−FS	0000000000

ZN501/2

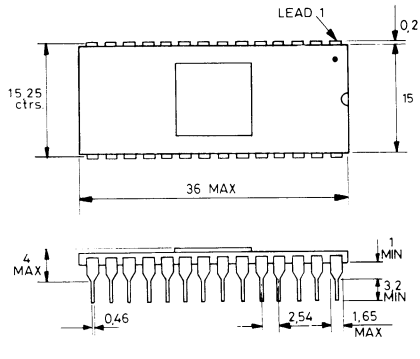
PIN CONNECTIONS



PACKAGE DETAILS



28 Lead Moulded D.I.L. 4116MD/2



28 Lead Ceramic D.I.L. 5457/3

Dimensions in millimetres

ZNA116E

FERRANTI semiconductors

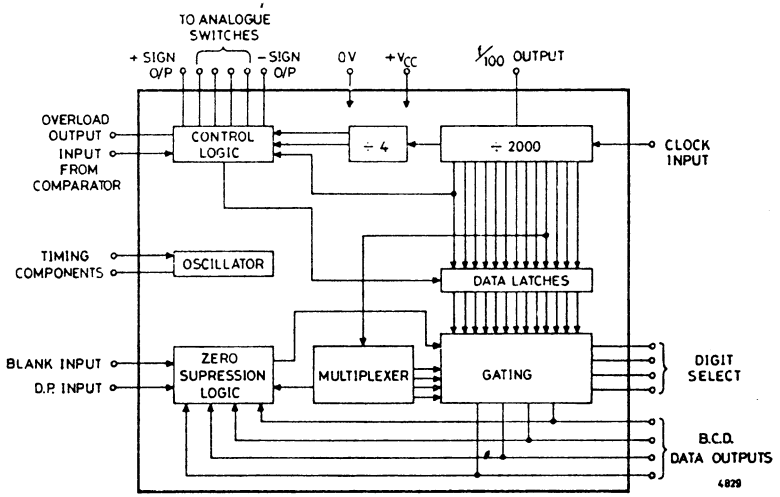
3 1/2 Digit DVM-Circuit for MPX-LED-Displays

FEATURES

- 3½ Decade display (±1999 max. reading)
- Automatic polarity detection and indication
- Leading zero suppression
- Overload indication
- Multiplexed B.C.D. outputs capable of driving a T.T.L. decoder/driver directly (e.g. ZNA7447A)
- External input to blank display
- Internal oscillator, adjustable externally
- An output at $^1/_{100}$ clock frequency for under range indication, or for synchronising the clock frequency for optimum mains rejection
- Single rail, 5 volt supply operation (at 10 mA typical)

GENERAL DESCRIPTION

The ZNA116E allows a precision 3½ digit D.V.M to be constructed very easily. It provides all the control logic necessary for a D.V.M using the well known dual slope integration technique. The low power requirements of the device make it attractive for portable battery operated applications and, since it is bipolar, requires no special handling precautions.



System Diagram

PINNING AND FUNCTIONAL DETAILS

Pin number	Name	Function
1	Earth	Supply 0 volts
2	f/100 output	An output at $^1/_{100}$ of the clock frequency is available at this pin.
3	Clock input	An external clock can be applied at this pin, or the internal oscillator can be used by linking it to pin 14. A measurement is made every 8000 clock periods. Transfer of a number to the latches occurs at the first –VE going clock edge after comparison has been made. The counter toggles on +VE going clock edges. Max. clock frequency = 50 kHz, Min. logic 0 time at clock input = 8 μsec.
4	M1	Digit drive output. When this output is low, the most significant digit is displayed.
5	M2	Digit drive output. When this output is low, the second most significant digit is displayed.
6	M3	Digit drive output. When this output is low, the third most significant digit is displayed.
7	M4	Digit drive output. When this output is low, the least significant digit is displayed. The multiplexed frequency = $^1/_{40}$ clock frequency.
8	Blank input	When this input is held at logic 1, the data outputs, A,B,C,D, will also all be at a logic 1. This is detected by the T.T.L. decoder/driver and the display is switched off.
9	D.P. input	When this input is at logic 1, leading zeroes are blanked off. Pins 5 and 6 can be wired to the D.P. input to give the correct display when a decimal point is displayed. (see diagrams).
10	A	2^0 BCD data output
11	B	2^1 BCD data output
12	C	2^2 BCD data output
13	D	2^3 BCD data output
14	Oscillator output	Link to pin 3 if internal oscillator is to be used.
15	Oscillator input	External components, connected to this pin, control oscillator frequency. (see figure 1).
16	+VE reference switch output	When this output is at logic 1, it connects the +VE reference voltage into the integrator.
17	–VE reference switch output	When this output is at logic 1, it connects the –VE reference voltage into the integrator.
18	–Sign output	This output is at logic 1 when a negative input voltage is being measured.

PINNING AND FUNCTIONAL DETAILS

Pin number	Name	Function
19	+Sign output	This output is at logic 1 when a positive input voltage is being measured.
20	Comparator input	This input is connected to the output of the external compartaor.
21	Signal switch output	When this output goes to logic 1, it connects the voltage to be measured into the integrator.
22	V_{CC}	Supply +5 volts.
23	Reset switch output	When this output is at logic 1, the switch across the integrator capacitor is turned on to completely discharge it.
24	Overload output	If the integrator capacitor does not discharge completely until after the counter has reached 2000, this output will go to logic 1.

TECHNICAL DATA

(a) Maximum Ratings:

Supply voltage .. .. 5.5 volts
Operating temperature .. .. 0°C to +70°C
Storage temperature .. .. .. −55°C to +125°C

(b) Electrical Characteristics (T_A = 0°C to +70°C)

Parameter	Min.	Typ.	Max.	Units	Test conditions
Supply voltage V_{OC}	4.75		5.25	Volts	
Supply current I_{CC}			15.0	mA	V_{CC} = 5 volts
Logic 0 level V_{IL} All input pins except pin 15			0.8	Volts	
Logic 1 level V_{IH} All input pins except pin 15	2.0			Volts	
High-level input current I_{IH} All input pins except pin 15			4.0	μA	$V_{in} = V_{CC}$
Low-level input current All input pins I_{IL}			−4.0	μA	V_{in} = 0V
Logic 0 level V_{OL} Output pins 2,4,5,6,7,10, 11,12,13			0.4	Volts	I_{sink} = 1.6 mA
Logic 0 level V_{OL} Output pins 14,18,19,21,24			0.4	Volts	I_{sink} = 1.0 mA
Logic 0 level V_{OL} Output pins 16,17,23			0.4	Volts	I_{sink} = 0.5 mA
Logic 1 level V_{OH} All output pins except pin 14	2.4			Volts	I_{out} = 10 μA
Oscillator frequency		20.0		kHz	With timing components shown in figure 1
Temperature coefficient of oscillator		±0.02		% per °C	Excluding temp. coefficient of the external timing components
Variation in oscillator frequency with changes in V_{CC}		−0.4		% per volt	T_A = 25°C

(c) Notes:

1. Pin 14 is an open-collector output. All other outputs have a nominal 100 kΩ pull-up resistor to V_{CC} rail.
2. Although the oscillator and logic will function up to 50 kHz, this is not recommended as the analogue circuitry becomes more critical.

ZNA116E

OSCILLATOR CIRCUIT

RECOMMENDED COMPONENTS FOR 20 kHz OPERATION

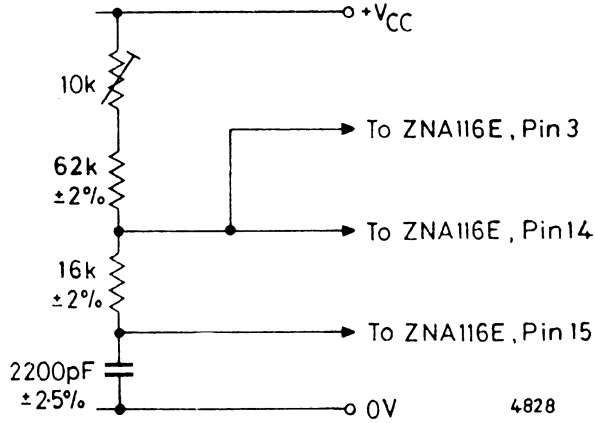


Figure 1.

Notes:

(a) Oscillator stability is better than 0.02% per °C.

(b) The potentiometer should be set so that the frequency of oscillation is 20 kHz. This is best monitored at pin 2, to avoid loading the oscillator while setting up.

(c) The potentiometer and the 62k resistor can be replaced by a single 68k ±2% high stablity resistor at the loss of some mains rejection only.

THE DUAL SLOPE SYSTEM

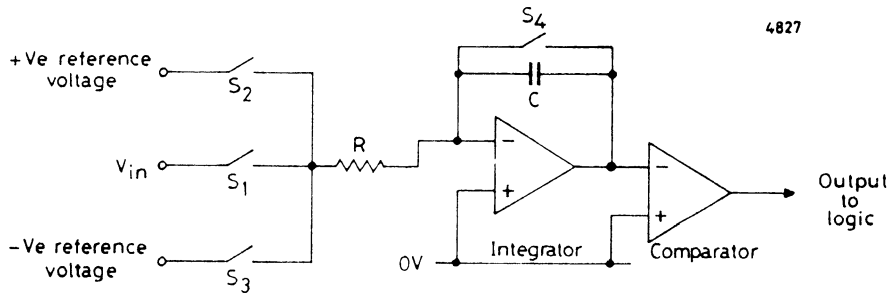


Figure 2.
(Refer to timing diagram, figure 3)

At time T_1 ; S2, S3 and S4 are open and S1 closes to apply the input voltage, V_{in}, to the integrator. The integrator capacitor, C, charges up linearly until time T_2 which is 4000 clock periods after T_1. The voltage at the integrator output, V_x, at time T_2 is proportional to V_{in}.

At time T_2, S1 is opened and either S2 or S3 is closed, to apply a reference voltage, of the opposite polarity to V_{in}, to the integrator, Thus C is made to discharge at a constant rate and at time T_3 the output voltage of the integrator will again be zero. This is detected by the comparator and the reference voltage is now switched off and the number of clock pulses corresponding to T_x will be transferrred to latches and displayed. This number is proportional to V_x and hence is proportional to V_{in}. If T_x exceeds 2000 clock periods, an overload condition is indicated.

At time T_4, which is 3000 clock periods after T_2, S4 closes to completely discharge the capacitor. At time T_5, which is 4000 clock periods after T_2, S4 opens and the cycle is repeated.

If S1 is closed for a time which is a multiple of 20 msec., any 50 Hz mains ripple superimposed on V_{in} will be integrated to zero and thus good mains rejection is obtained.

The dual slope D.V.M. does not require a high stability capacitor or high stability oscillator (unlike single slope systems) to achieve high accuracy.

ZNA116E TIMING

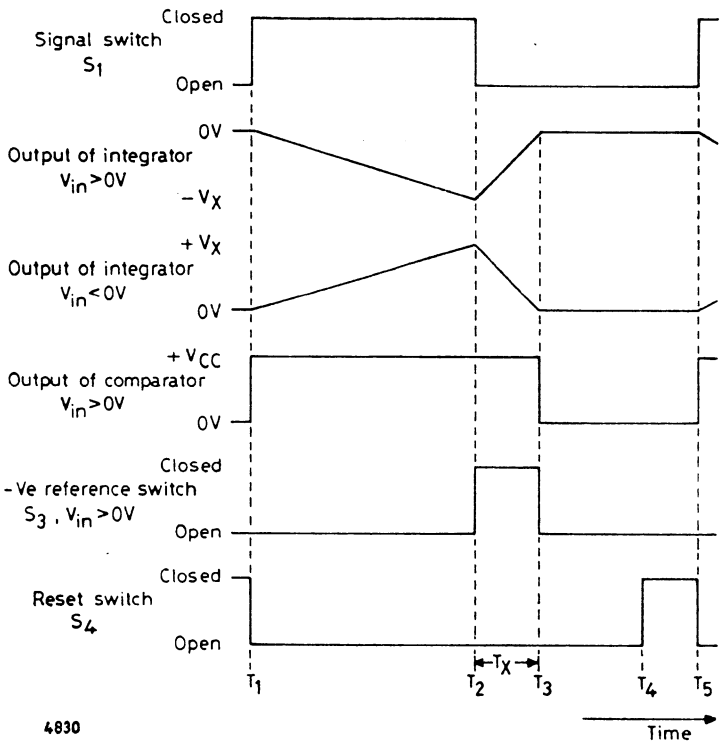


Figure 3.

ZNA116E

THE DESIGN OF D.V.M. CIRCUITS USING THE ZNA116E

The ZNA116E provides the control logic necessary to construct a D.V.M. with a $3\frac{1}{2}$ digit display having an accuracy of $\pm\frac{1}{2}$ digit. The actual accuracy obtained will depend on four factors:

(a) Accuracy of calibration.

(b) Stability of reference sources.

(c) Stability of transistor switches.

(d) Operational amplifier drift.

The circuit details are given for the construction of a simple D.V.M. circuit which runs off a single 5 volt supply rail. The accuracy of this D.V.M., typically 0.1% $\pm$1 mV., (on the 1v. range) should be adequate for many applications.

To achieve this accuracy, the nominal 5 volt supply rail should be held stable to $\pm$50 mV. An I.C. voltage regulator is ideal for this purpose.

The main factor limiting the performance of this circuit is (d). If a better performance is required, an amplifier with a lower bias current must be used (e.g. ZN741) running of $\pm$5 volt supply rails, so that the drift becomes less significant. More elaborate interfacing with the ZNA116E will be required in this case.

D.V.M. CONSTRUCTION

Due to the clearly defined application of the ZNA116E, the full circuit is given for a simple $3\frac{1}{2}$ digit D.V.M. together with full printed circuit board details.

The construction is defined in two distinct halves an analogue board containing integrator, comparator, reference supplies and transistor switches; and a digital board containing the ZNA116E, display, driver and oscillator components. This allows the constructor the chance to alter the 'front end' (analogue circuit) if desired, without disturbing the digital board.

PRINTED CIRCUIT BOARD

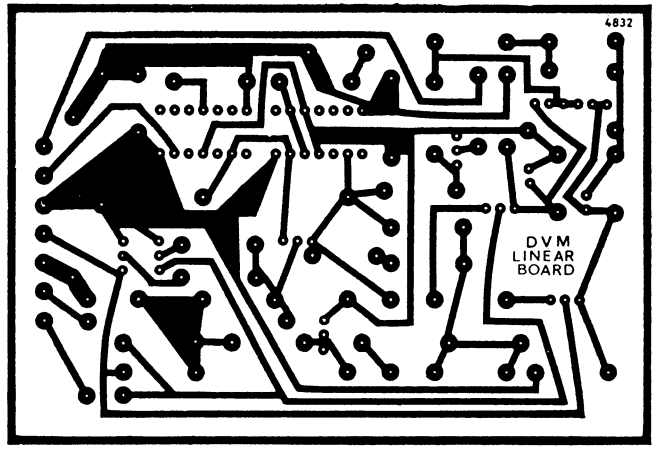


Figure 4. ANALOGUE BOARD (copper side) ¾ FULL SIZE

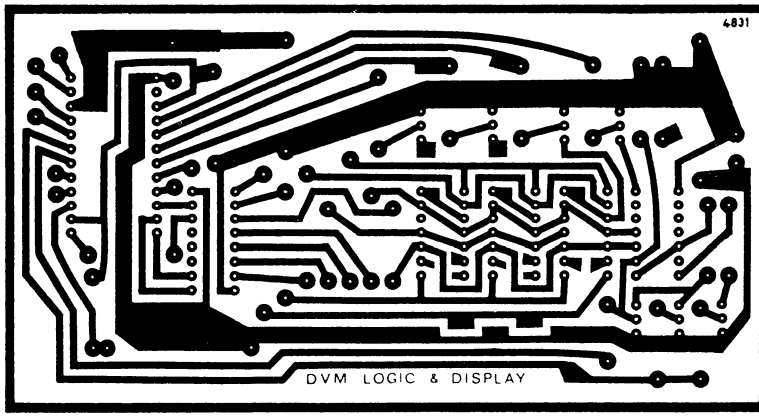
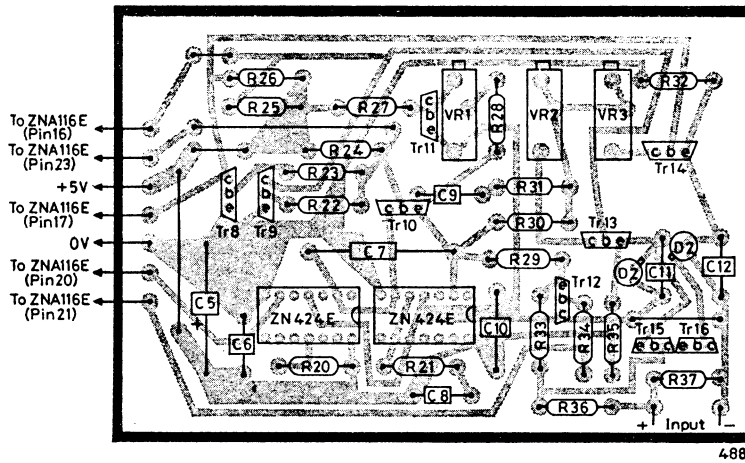
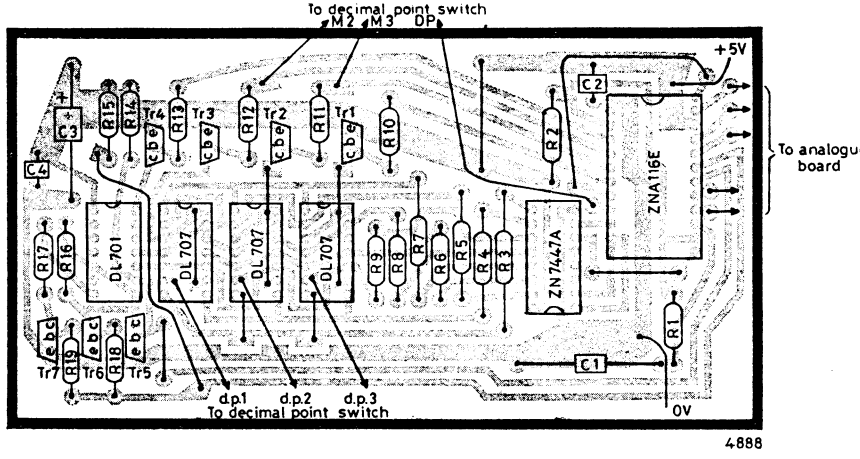


Figure 5. DIGITAL BOARD (copper side) ¾ FULL SIZE



ANALOGUE BOARD – Component positions

Figure 6.



DIGITAL BOARD – Component positions

Figure 7.

CIRCUIT DIAGRAM OF ANALOGUE BOARD

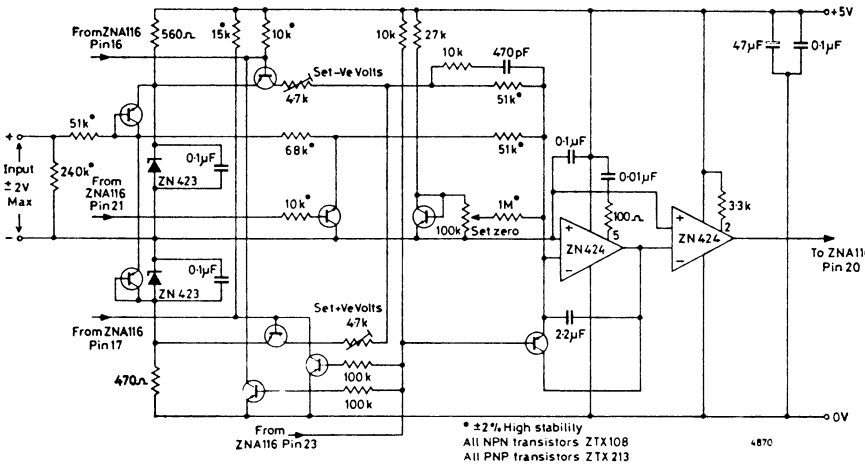


Figure 8.

CIRCUIT DIAGRAM OF DIGITAL BOARD

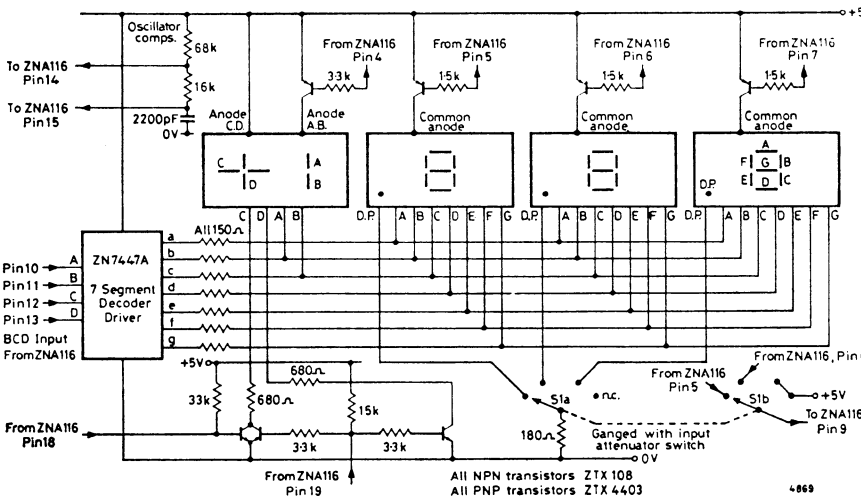


Figure 9.

ZNA116E

D.V.M. COMPONENT LIST

R1	16k ±2%	R14	33k	R27	27k
R2	68k ±2%	R15	15k	R28	1M ±2%
R3	150	R16	680	R29	51k ±2%
R4	150	R17	680	R30	51k ±2%
R5	150	R18	3.3k	R31	10k
R6	150	R19	3.3k	R32	470
R7	150	R20	3.3k	R33	68k ±2%
R8	150	R21	100	R34	10k ±2%
R9	150	R22	100k	R35	560
R10	1.5k	R23	100k	R36	51k ±2%
R11	1.5k	R24	10k	R37	240k ±2%
R12	1.5k	R25	10k	R38	180
R13	3.3k	R26	15k		

VR1 100k
VR2 5k } Bourns 3009P
VR3 5k

All values given in ohms.

All resistors ±10% unless stated otherwise.

C1 2200 pF ±2.5%
C2 0.033 μF
C3 68 μF 10 vw. electrolytic ±50%
C4 0.033 μF
C5 68 μF 10 vw. electrolytic ±50%
C6 0.1 μF
C7 2.2 μF ±10%
C8 0.01 μF
C9 470 pF
C10 0.1 μF
C11 0.1 μF
C11 0.1 μF
C12 0.1 μF

All capacitors ±20% non-electrolytic unless stated otherwise.

Tr1, Tr2, Tr3 Tr4 — all ZTX4403
Tr5, Tr6, Tr7, Tr8, Tr9, Tr10, Tr11, Tr13 Tr14, Tr15, Tr16, — all ZTX 108
Tr12 — ZTX213

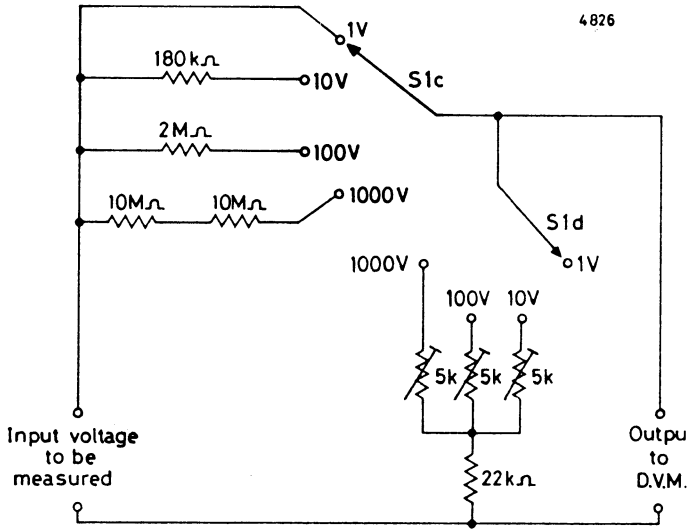
D1, D2 — both ZN423

ZNA116E 1 off
ZN424E 2 off
ZN7447A 1 off

DL707L display 3 off
DL701 display 1 off

ATTENUATION OF INPUT VOLTAGE

For measuring voltages of ±2 volts or more, the following input attenuator circuit may be used.



All resistors ±2% high stability, presets ±20% carbon.

Figure 10.

The input impedance is 100 kΩ on the 1 volt range and 20 kΩ/volt on the other three ranges. If a greater impedance than this is required, an attenuator using higher value resistors followed by an F.E.T. input buffer amplifier should be used.

Note: In the above diagram, switches S1c and S1d are ganged with S1a and S1b, the decimal point switch, shown in figure 9.

CONSTRUCTIONAL NOTES

(1) The leads joining the analogue board to the digital board should not be longer than about six inches.

(2) Before connecting the circuit to a power supply, make sure that all the external links, shown in figures 6 and 7, have been connected to the printed circuit boards. There should be five links on the analogue board and twelve on the digital board.

(3) If the applied input voltage is too large, the display will be blanked off as an overload indication. If a diode is connected between pins 8, 24 and 21 of the ZNA116E, as shown below in figure 11, the display will flash for overload conditions.

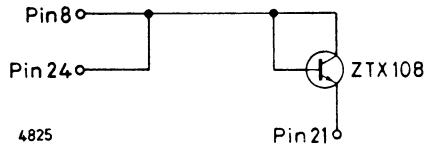


Figure 11.

CALIBRATION PROCEDURE

The range switch is placed in the 1 volt position and the input terminals are shorted together. VR2 and VR3 should be set about half-way. The set-zero preset VR1 is now adjusted until the display just flickers between +0 and –0.

A known positive voltage, between one and two volts, is now connected to the input terminals and VR3 is adjusted until this voltage is displayed.

The input voltage is then reversed and VR2 is adjusted until the display is again correct.

VR1, VR2 and VR3 are now correctly set and should not need altering again.

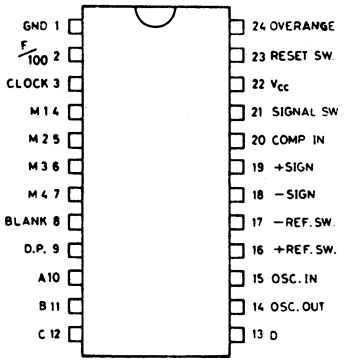
Since the three 5k presets in the attenuator section are completely independent of each other, these can be easily set to give the required attenuation of 10, 100 and 1000.

Calibration is now complete.

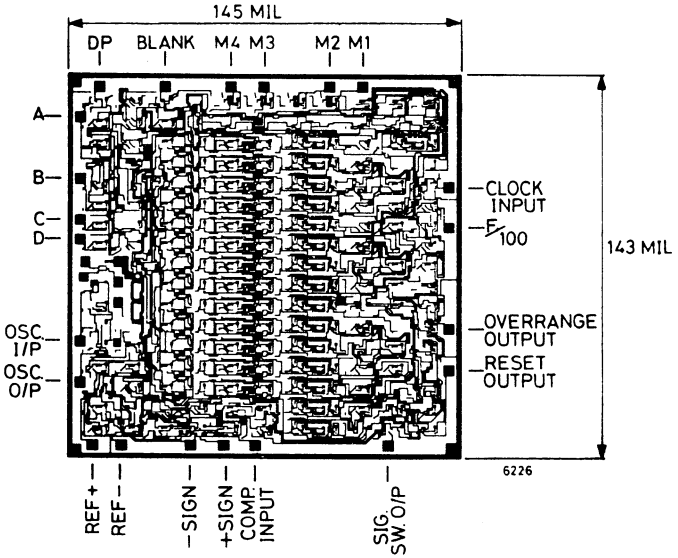
SPECIFICATION OF D.V.M.

Maximum reading	±1999
Readings per second	2½ typical
Typical accuracy (1 volt range)	0.1% of reading ±1 mV
Temperature coefficient (1 volt range)	±0.1 mV per °C typical
Input impedance	100 kΩ for 1 volt range 200 kΩ for 10 volt range 2 MΩ for 100 volt range 20 MΩ for 1000 volt range
Total supply current (with all segments on)	200 mA typical

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



ZNA216E
ZNA216J

FERRANTI semiconductors

3 3/4 Digit DVM-Circuit for MPX-LED-Displays

FEATURES

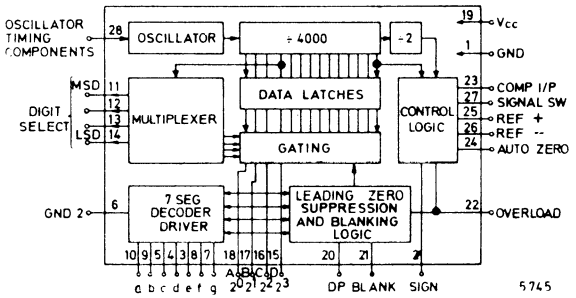
- 3¾ digit display (±3999 max. reading)
- Automatic zero adjustment with 1 μV/°C temperature coefficient
- Seven-segment outputs for direct drive of LED displays
- BCD outputs
- Automatic polarity detection and indication
- Flashing overload indication, separate overload output
- Blanking input, e.g. for low battery indication
- Automatic blanking of display leading zeroes
- On-chip clock, may be externally synchronised
- TTL and CMOS compatible
- Single +5V supply
- Pinning optimised for easy p.c.b. layout

DESCRIPTION

The ZNA216 D.V.M. I.C. is a versatile D.V.M. system component which contains all the control logic necessary to construct a dual-slope digital voltmeter, whilst leaving the designer free to configure the analogue circuitry to his own requirements.

The I.C. has multiplexed data outputs, both in BCD format and in seven-segment format for direct drive of LED displays. A number of useful features are incorporated into the device, including leading zero blanking of the display, flashing over range indication and an auto zero facility which removes the need for manual zero adjustment.

Apart from the more obvious applications of D.V.M. and D.P.M. the I. C. can be used to construct any other instrument where an analogue input from, say, a transducer is to be converted into a digital reading, for example a digital thermometer. The ZNA216 may also be used as an A-D converter in single-channel data acquisition systems, or to interface to a microprocessor system.



System Diagram

PINNING AND FUNCTIONAL DETAILS

Pin number	Name	Function
1	Gnd 1	Supply 0 volts
2	Sign	Open collector output, goes low when –ve input voltage is being measured.
3	e	Open collector segment output, goes low when segment is on.
4	d	Segment output as above.
5	c	Segment output as above
6	Gnd 2	0 volt supply for segment drivers, must be connected to Pin 1.
7	g	Segment output as above
8	f	Segment output as above
9	b	Segment output as above.
10	a	Segment output as above
11	M1	Digit drive output, goes low for the most significant digit to be displayed, first in digit scan sequence.
12	M2	Digit drive output, goes low for the second most significant digit fo be displayed, second in digit scan sequence.
13	M3	Digit drive output, goes low for the third most significant digit to be displayed, third in digit scan sequence.
14	M4	Digit drive output, goes low for the least significant digit to be displayed, fourth in digit scan sequence.
15	D	2^3 BCD data output.
16	C	2^2 BCD data output.
17	B	2^1 BCD data output.
18	A	2^0 BCD data output.
19	V_{CC}	Supply +5 volts.
20	DP	When this input is at logic 1, leading zeroes are blanked.
21	Blank	While this input is at logic 1, all segment outputs are off and all BCD data outputs are at logic 1.
22	Overload	If the integrator capacitor does not discharge before the conter reaches 4000, this output goes to logic 1.
23	Comp.	This input is connected to the output of the external comparator.
24	Azero	When this output is high, auto zero correction is applied to the integrator.

Pin number	Name	Function
25	Ref+	When this output is at logic 1, the +ve reference voltage is connected to the integrator.
26	Ref–	When this output is at logic 1, –ve reference voltage is connected to the integrator.
27	Signal switch	When this output is at logic 1, the input voltage to be measured is connected into the integrator.
28	Clock	The external clock oscillator components are connected to this pin (see diagrams). Alternatively, this pin may be driven by an external signal. A measurement is made every 8000 clock periods. The counter toggles on –ve going clock edges and transfer to the latches occurs at the first +ve going clock edge after comparison has been made which avoids false triggering from the integrator output. Max. clock frequency 50 kHz.

(a) Absolute Maximum Ratings:

Supply voltage	7.0 volts
Operating temperature	0°C to +70°C
Storage temperature	−55°C to +125°C

(b) Electrical Characteristics (T_A = 0°C to +70°C, V_{CC} = 5.0V unless otherwise specified).

Parameter		Min.	Typ.	Max.	Unit	Test conditions
Supply voltage		4.5		5.5	V	
Supply current				20	mA	
Low level input voltage	All inputs			0.8	V	
Low level input current	All inputs			−4	μA	V_{in} = 0V
Input clamp diode voltage	All inputs			−1.5 V_{CC} +1.5	V V	I_{in} = −12 mA I_{in} = 10 mA
High level input voltage	Oscillator RC input	2.5			V	
	All other inputs	2.0			V	
High level input current	Oscillator RC input			100	μA	V_{in} = 2.5V
	All other inputs			4	μA	V_{in} = 5.0V
Low level output voltage	a, b, c, d, e, f, g			0.8	V	I_{sink} = 20 mA
	Sign			0.4	V	I_{sink} = 5 mA
	Overload, Ref+, Ref−, Azero, Signal switch, a,b,c,d,M1,M2, M3, M4			0.4	V	I_{sink} = 1.6 mA
High level output voltage	Overload, Ref+, Ref−, Azero, Signal switch, a,b,c,d,M1,M2, M3, M4	2.4			V	I_{out} = 10 μA
			V_{CC} −0.1		V	I_{out} = 0
High level output current	a,b,c,d,e,f,g Sign			−10	μA	V_{out} = 5.0V

(c) Note:

Although the oscillator and logic will function up to 50 kHz, this is not recommended as the analogue circuitry becomes more critical.

THE DUAL SLOPE SYSTEM

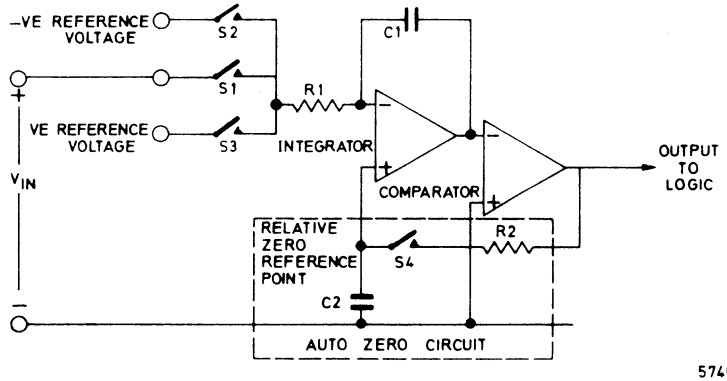


Figure 1. Dual Slope Block Diagram.

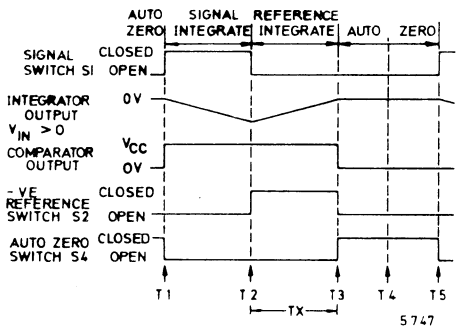


Figure 2a. Timing Diagram for in-range input.

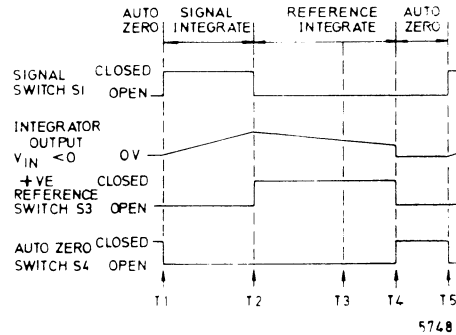


Figure 2b. Timing diagram for overrange input

Dual slope integration is a D.V.M. circuit technique designed to cancel out the effects of drift in circuit components. A block diagram of the analogue section of a dual-slope D.V.M. is shown in figure 1, whilst a timing diagram for its operation is shown in figure 2.

At time T_1, S1 is closed by the D.V.M. logic, connecting the input signal to the integrator until time T_2, which is 2000 clock periods after T_1. During this time the integrator output ramps positive or negative, depending on input voltage polatrity, to a voltage

$$V_o = \frac{-V_{in}\, 2000\, t_c}{R_1 C_1}$$

where t_c is the clock period.

The polarity of the integrator output voltage during this period, and hence of the input voltage, is sensed by the comparator, whose output is connected to the control logic.

At time T_2, S1 is opened and, depending on the input voltage polarity, either S2 or S3 is closed. This connects a reference voltage of opposite polarity to V_{in} to the integrator input, so that the integrator output ramps back towards zero. The number of clock periods required for the integrator output to reach zero is counted by the DVM counter. When the output reaches zero the comparator output changes state, S2 or S3 opens and the count is stopped. Since the second integration also takes place over a voltage V_o then,

$$V_o = \frac{-V_{REF}\, nt_c}{R_1 C_1} \text{ where n is the count at time } T_3$$

but V_o also equals $\dfrac{-V_{in}\, 2000 t_c}{R_1 C_1}$

$$\text{thus } n = \frac{2000\, V_{in}}{V_{REF}}$$

R_1, C_1 and t_c have disappeared from this final equation, so the accuracy of the D.V.M. is unaffected by the long-term stability of these parameters. The only factors influencing accuracy are the stability of V_{REF} and variations in the 'on' resistance of the analogue switches S1 to S3. The former can be assured by careful choice of a reference source, e.g. the Ferranti ZN423 or ZN458, whilst the effect of the latter can be minimised by making R_1 lage compared to the on resistance of S1 to S3.

If V_{REF} is exactly 2V then $n = 1000\, V_{in}$, i.e. the count will be equal to the input voltage in millivolts. For the ZNA216 the maximum reading is 3999. If a count of 4000 occurs before the integrator output reaches zero, as shown in figure 2b, then S2 or S3 will open and the overrange output will go high.

In a practical D.V.M. it is unlikely that a reference voltage of exactly 2V will be available, or an input range other than 3.999V may be required. In this case a different resistor value (R_{REF}) will be used for the reference integration. The equation then becomes :

$$n = \frac{2000\, V_{in} \cdot R_{REF}}{V_{REF} \cdot R_1}$$

R_1 and R_{REF} should be high-stability types.

AUTO ZERO

Any offset voltage and bias current in the integrator will be integrated along with the input signal and since, for example, a 3.999V D.V.M. has a resolution of 1 mV an offset of a few hundred microvolts can lead to errors in the least significant digit. Manual zero adjustment is time-consuming and has to be repeated frequently due to temperature drift.

The auto zero of the ZNA216 operates during the period T_3 to T_5, or T_4 to T_5 in the case of an overrange input. S4 is closed, S1 S2 and S3 are opened so that only the integrator offset voltage is integrated, thus causing the integrator output to drift either positive or negative. The integrator output is amplified by the comparator (which is nothing more than an extremely high gain amplifier) and this charges C2 via R2 to apply a voltage to the non-inverting input of the integrator. The polarity of this voltage is such as to null out the effects of integrator offset voltage and bias current and thus cancel integrator drift. Depending on comparator gain a zero error of a few hundred nanovolts may be achieved by this method.

HUM REJECTION

Any mains hum pickup superimposed on the input signal will cause errors in the D.V.M. reading. However, if the period $T_2 - T_1$ is made a multiple of the mains period then equal numbers of positive and negative half-cycles of the mains waveform will be integrated and will cancel each other out. For 50 Hz mains $T_2 - T_1$ should be 20 ms or a multiple thereof, while for 60 Hz mains $T_2 - T_1$ should be 16.67 ms or a multiple thereof.

Adjustment of the period $T_2 - T_1$ is achieved by varying the frequency of the clock oscillator which controls the operation of the D.V.M.

DISPLAY MULTIPLEXING

The BCD and seven-segment data outputs are multiplexed, the data appearing in the sequence MSD to LSD. To identify which digit is present at the outputs at any time the four digit select outputs go low in turn, synchronous with the relevant digit appearing at the data outputs. The seven segment outputs can be used to drive the cathodes of a multiplexed common-anode LED display whilst the digit select outputs may be used to turn on digit-drive transistors, which activate each display digit in sequence.

DECIMAL POINT (ZERO BLANKING) INPUT

Before the start of each multiplex cycle a latch in the I.C. is set. This holds the display blanked until non-zero data appears at the BCD outputs, when the latch is reset and the disply is unblanked. For example, if the MSD were non-zero the latch could reset immediately the MSD appeared, so all four digits would be displayed. Conversely if the MSD were zero but the second digit were non-zero then the display would be blanked for the MSD and only three digits would appear. In this way leading zeroes in the display are suppressed. The LSD is always displayed whether zero or not.

The D.P. input can be used to override the zero blanking by taking this pin to logic '0'. This facility allows a correct display to be obtained when a decimal point is used.

For example, if the decimal point is to the left of the MSD then a low-going pulse to the D.P. input synchronous with the MSD output will cause all digits to the right of the decimal point to be displayed, whether zero or not. Thus, if the input voltage were, say .0056 volts then the display would be .0056. If the zero blanking were not overridden in this way the display would be .--56, which is clearly unsatisfactory.

OSCILLATOR CIRCUIT

The operation of the D.V.M. circuit is controlled by a clock oscillator, which provides drive for the counter, control logic and display multiplexing. Two external components, a resistor and a capacitor, are required to make the oscillator function. The oscillator temperature stability is typically $\pm 0.02\%$ per °C.

As mentioned earlier, the oscillator frequency should be chosen so that $T_2 - T_1$ is a multiple of the mains period. It should not be chosen so low as to cause noticeable flicker in the display multiplexing, but on the other hand it should not be chosen too high or the design of the analogue circuitry becomes more critical.

The optimum oscillator frequency is 20 kHz since this makes $T_2 - T_1 = 100$ ms which gives good hum rejection at either 50 Hz or 60 Hz. This frequency can be obtained by using the component values shown in figure 3. The potentiometer may be adjusted to give a frequency of 20 kHz measured at pin 28, in which case a high impedance, low capacitance probe should be used to avoid loading the oscillator. Alternatively, the trimmer may be adjusted to give a frequency of 500 Hz at any of the digit select outputs, when no special precautions are required.

If required the oscillator timing components may be omitted and the oscillator input may be driven by an external clock at TTL logic levels.

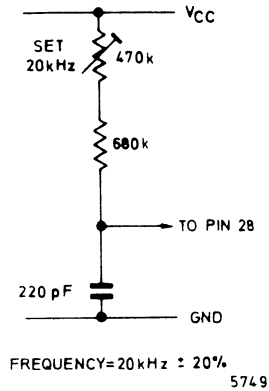


Figure 3. Oscillator external components.

INPUT AND OUTPUT CIRCUITS

Apart from the oscillator input (which is a Schmitt trigger type of circuit) all other inputs are as shown in figure 4a. All outputs are as shown in figure 4b, except for those designated as open-collector, which have no pull-up resistor.

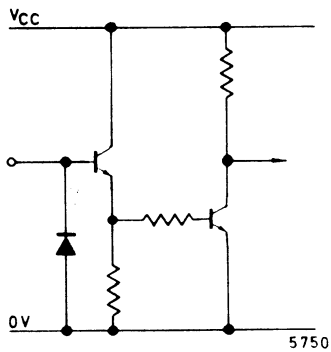


Figure 4a. Input circuit

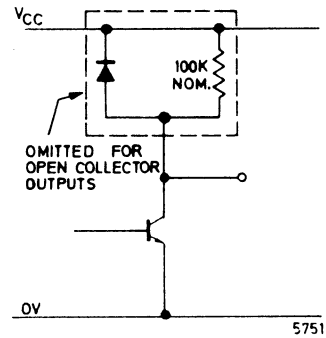


Figure 4b. Output circuit

DISPLAY DRIVING

The 20 mA sink capability of the segment outputs allows common anode LED displays to be driven with a minimum of external components, as shown in figure 5. The segment current limit resistors should be chosen to give the desired segment current, allowing for the forward voltage drop of the LED, whilst the digit output resistors should be chosen to give sufficient base current to saturate the digit drive transistors.

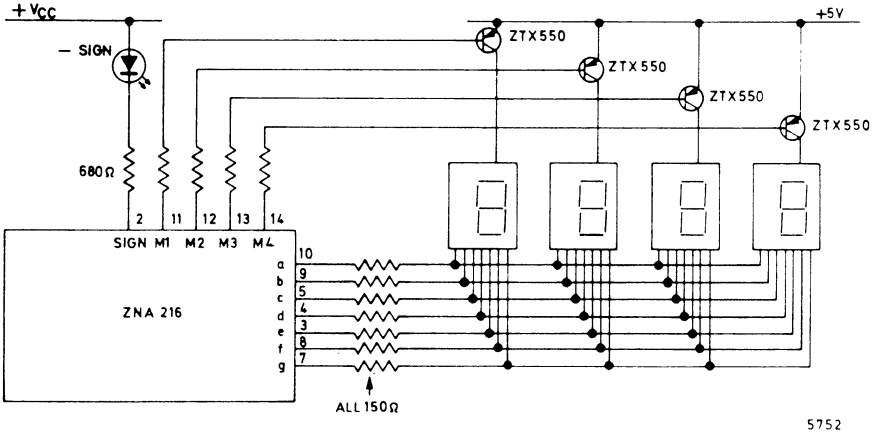


Figure 5. Display drive circuit

OVERRANGE AND LOW BATTERY INDICATION

If the input voltage exceeds the full-scale range then the display will flash all 'eights' and the over-range output, pin 22, will go high. Low battery indication may also be provided by the addition of the simple circuit shown in figure 6.

Whilst the battery voltage is above 4.4V T_1 will be turned on via R1 and R2. Below this volage the base potential supplied by these resistors will be insufficient to turn on T_1 and it will then be turned on and off cyclically by the auto-zero output, causing the display to flash whatever reading is present.

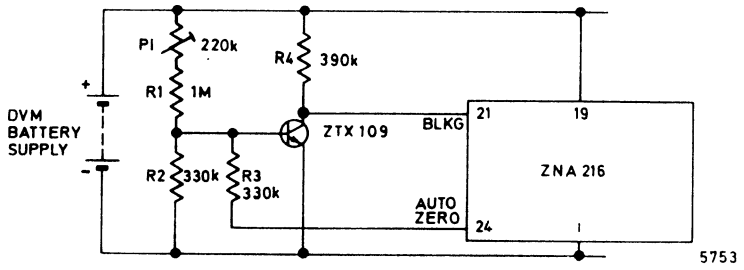


Figure 6. Low battery indication

A PORTABLE D.V.M.

Figure 7 shows the circuit of a battery-powered D.V.M. based on the ZNA216, which uses readily available components. ZN424 op-amps are used for the integrator and comparator, whilst bipolar silicon transistors are used for the analogue switches. The basic sensitivity of the instrument is 4V, and additional ranges of 40V and 400V are provided by means of an input attenuator. Printed circuit board and component layouts for the D.V.M. are given in figures 8a to 9b.

However, this circuit design should by no means be considered as immutable. Since the analogue circuitry is external to the ZNA216 it may be configured to suit the designer's needs to give higher input impedance, increased sensitivity etc.

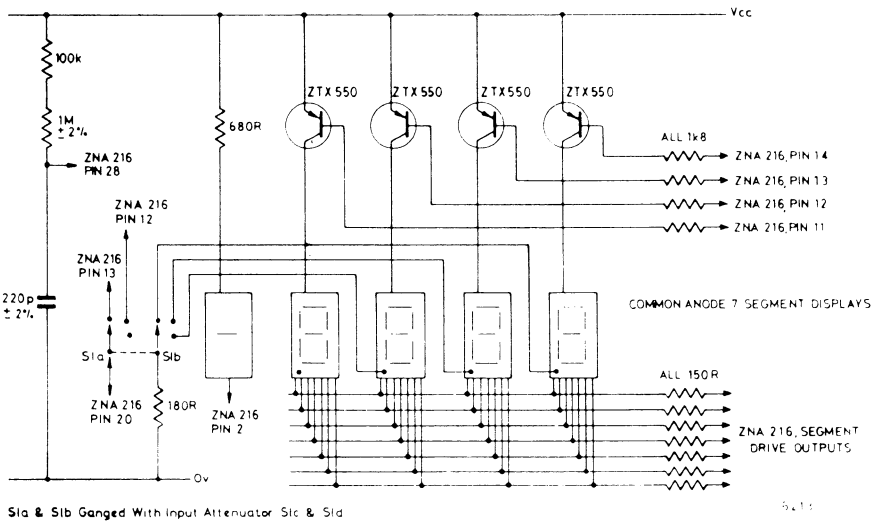


Figure 7a. Battery-powered D.V.M. circuit, display section.

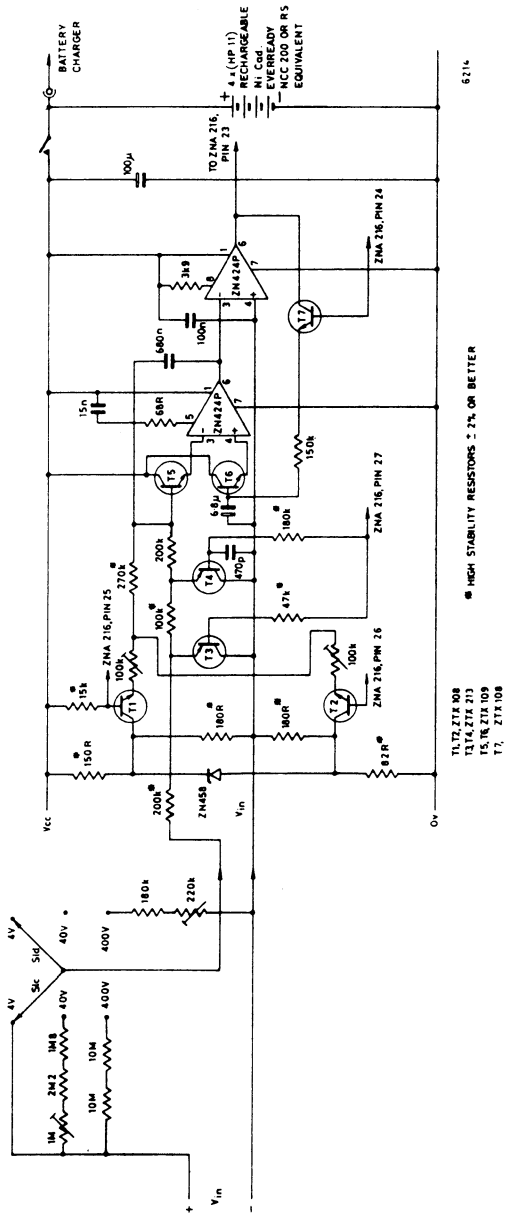
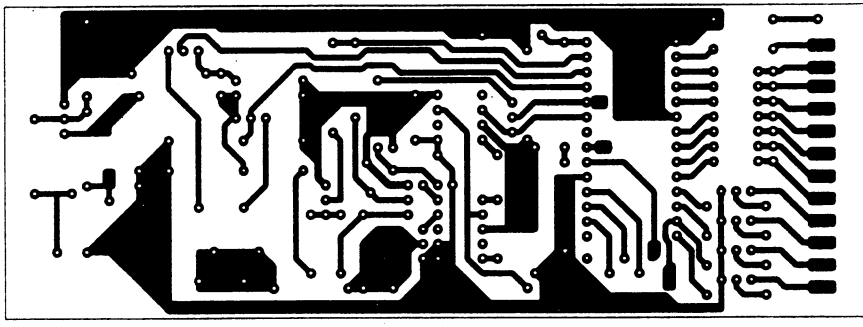


Figure 7b. Battery-powered D.V.M. circuit, analogue section.



6216

Figure 8a. D.V.M. Main Board

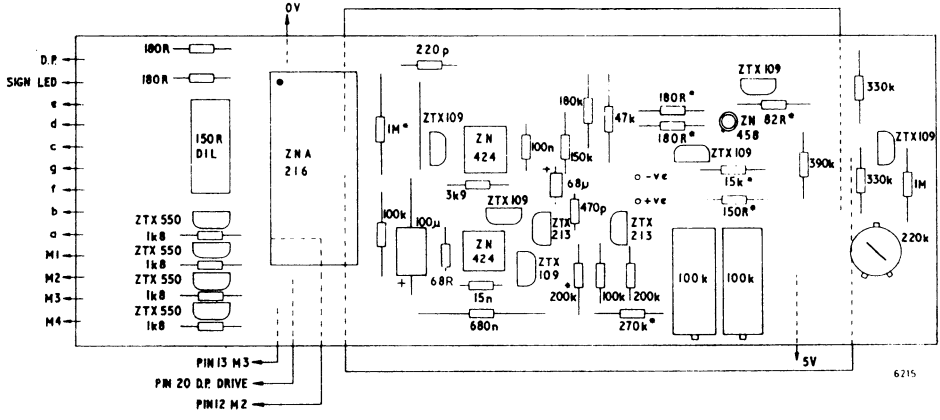


Figure 8b. Component Layout for Figure 8a.

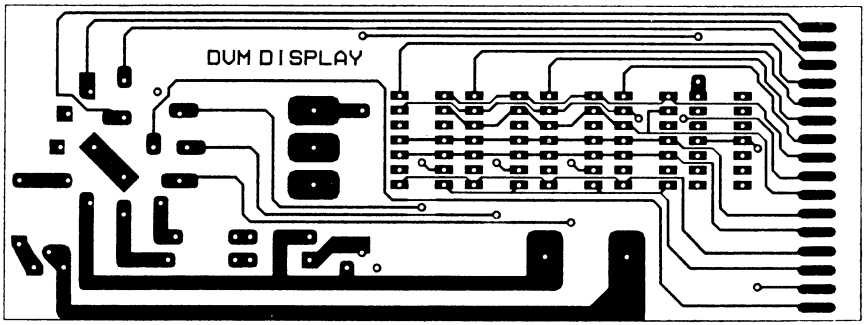


Figure 9a D.V.M. Display Board

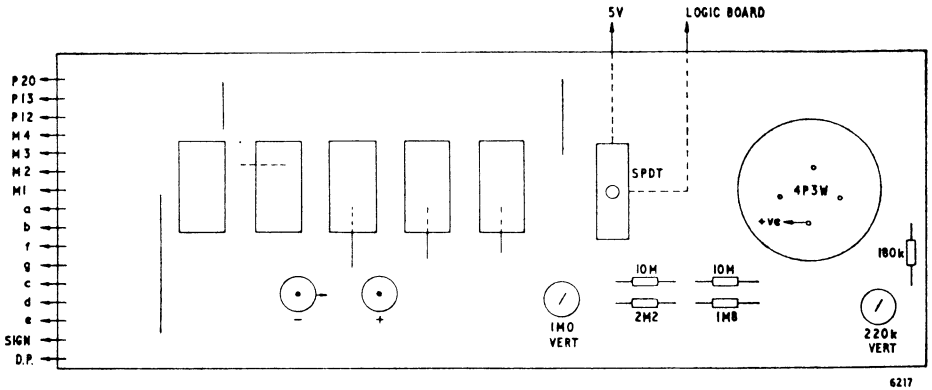


Figure 9b. Component Layout for Figure 9a.

MICROPROCESSOR INTERFACING

The ZNA216 may be used as a dual-slope A to D converter in data loggers and other data acquisiton systems, where its $3\frac{3}{4}$ decade range offers a resolution comparable to a 13 bit binary ADC, but in a more convenient BCD format.

Figure 10 is a block diagram which illustrates how the ZNA216 may be interfaced to an 8-bit microprocessor. The principle of operation is that the four multiplexed BCD digits of the ZNA216, plus the sign and overrange bits, are stored in four 4-bit latches so that they are available in parallel form. The contents of the latches can then be read into the microprocessor as two 8-bit words. The latches used are type 74173 which have three-state outputs for direct connection to the μP data bus. Data is clocked into the latches using the positive-going edge of the appropriate digit drive outputs.

The latches are treated as two memory locations by using an address decoder which is connected to their output enable pins. In this way data can be read out of the latches just as from any other memory locations. Once data is in the latches it may be read out whilst the ZNA216 performs the next measurement, thus eliminating any waiting time. The only time when data cannot be read out of the latches is just after the ZNA216 has completed a measurement. At this time the data in the internal latches of the ZNA216 will have been updated and the data in the 74173s may thus be changing. The data in the latches will be stable after two multiplexed cycles of the ZNA216, which is 4 ms if a 20 kHz clock is used.

Since the auto-zero output of the ZNA216 goes high when a measurement has been completed this output may be used as a BUSY signal. Data should not be read from the 74173 latches until at least 4 ms after the auto-zero output has gone high.

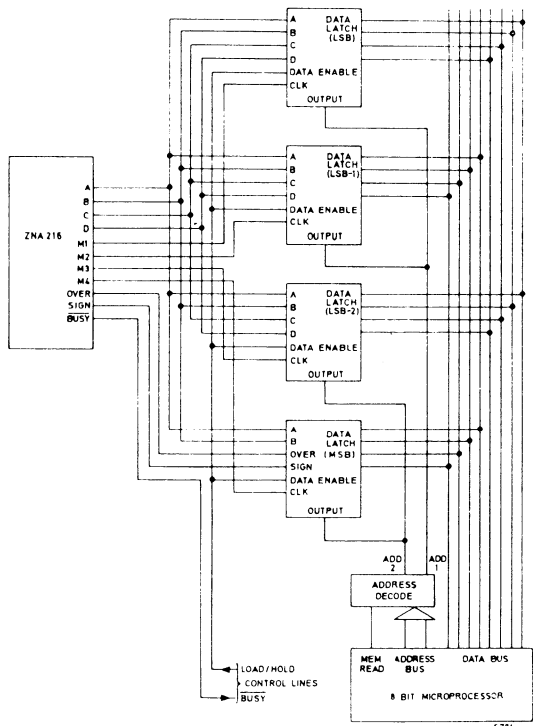
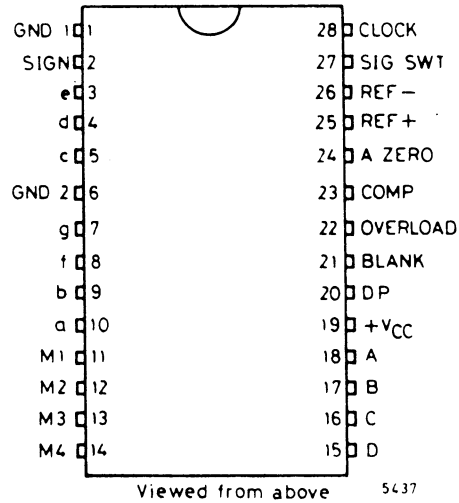


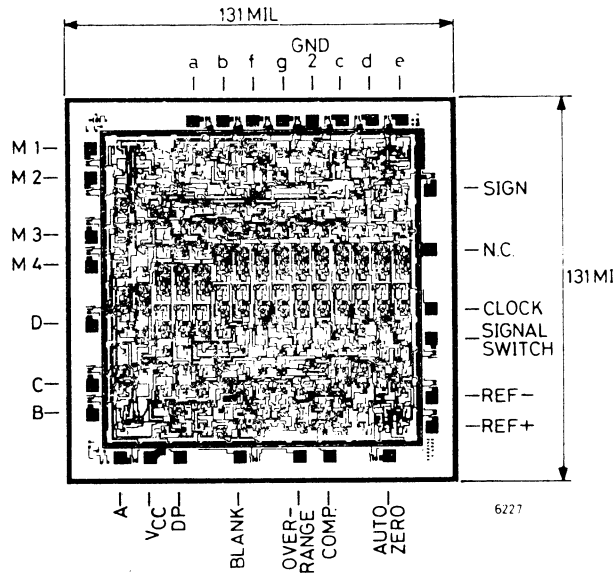
Figure 10. Interfacing the ZNA216 to a Microprocessor

ZNA216E/J

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT



Notes

ZN412

FERRANTI semiconductors

DIGITAL CLINICAL THERMOMETER INTEGRATED CIRCUIT

Advance Product Information

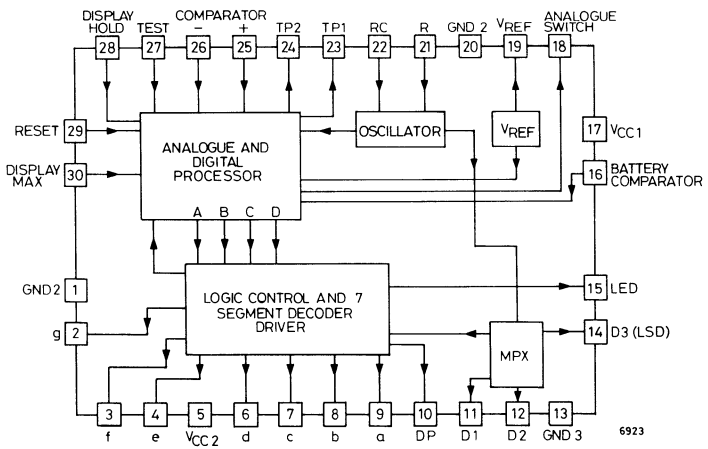
FEATURES

- Low external component count
- Low supply current
- Accuracy ±1LSD (0.1°C)
- Direct drive of LED display
- Self testing facility
- Battery status indication
- Consistent and repeatable performance
- 5 second response time

DESCRIPTION

By combining all the complex linear and digital functions on the same chip the ZN412 enables a digital clinical thermometer to be constucted with few external components.

The ZN412 has multiplexed data outputs capable of directly driving a 3 digit seven segment LED display. These outputs are controlled by an on-chip A/D processor which converts the output from an external probe element into a digital number. Temperature can be displayed from 35.0°C to 47.6°C with a resolution of 0.1°C at a sample rate of 3 per second. Above 42.9°C, however, all the decimal points will be on whereas below 35°C 3.4.9. will be displayed. A number of useful features are incorporated into the ZN 412, including a self check facility, battery status indication reset and display hold.



Absolute Maximum Ratings .. .. 0°C to +70°C
Dissipation .. .. t.b.a.
Supply Output Current (Source) 4.5mA
Multiplex Output Current (Sink) 25mA
Operating Temperature Range (Ambient) .. .. 0°C to +70°C
Storage Temperature Range .. .. −55°C to +125°C

FUNCTION	PARAMETER AT 25°C AMB.	MIN.	TYP	MAX.	UNITS
V_{REF} with external shaping cap. 1uF min.	Output Voltage	1.75	1.85	1.95	V
	Temp. Coefficient	+1.0		+3.0	mV/°C
	Slope Resistance			5	Ω
Comparator 1	Input Bias Current			30	nA
	Input Offset Current			±10	nA
	Input Offset Voltage			±5	mV
	Open Loop Voltage gain		74		dB
	Bias Current Drift			−2.0	%/°C
	Offset Current Drift			−2.0	%/°C
	Offset Voltage Drift			±20	μV/°C
Comparator 2	Input Bias Current			200	nA
	High Level Input Voltage	0.6x V_{REF} +0.1			V_{REF}
	Low Level Input Voltage			0.6x V_{REF}−0.1	V_{REF}
Comparator 3	Input Bias Current			2	μA
	High Level Input Voltage	0.6x V_{REF} +0.1			V
	Low Level Input Voltage			0.6x V_{REF}−0.1	V
Analogue Switch	Low Level Output Voltage			2	mV
	High Level Output Voltage	V_{REF} −0.002		V_{REF} +0.002	V
Oscillator with R = 100K C = 150pF	Frequency	4.8		5.8	kHz
	Temp. Coefficient		−0.01		%/°C
	Volt. Coefficient		+1.0		%/V

D.C. characteristics over the operating temperature range (V_{CC} = 4.5V)

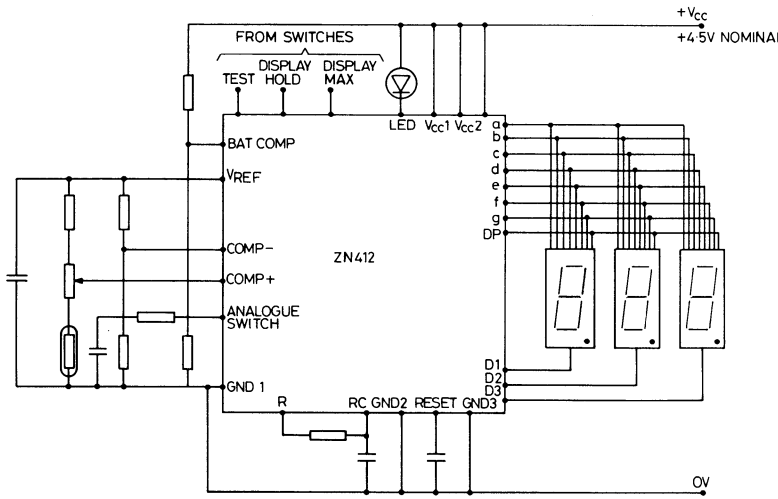
Parameter		Test Conditions	Min.	Typ	Max.	Units
Supply Current		No connection to DP,a,b,c,d,e,f,g		7	14	mA
Low level input voltage	Display Hold, Display max.				0.8	V
V_{T-}	Test, Reset			2.5		V
Low level input current	Test, Display Hold, Display max., Reset.	V_{in} = OV		−10	−20	μS
High level input voltage	Display Hold, Display max.		2.0			V
V_{T+}	Test, Reset			3.0		V
High level input current	Display max. Display Hold.	V_{in} = 4.5V			50	μA
	Test, Reset	V_{in} = 4.5V			10	μA
Low level output voltage	D1, D2, D3	I_{SINK} = 24mA	0.9	1.1	1.3	V
	a,b,c,d,e,f, g, DP.	I_{OUT} = 10μA			1.5	V
Low level output current	LED	V_{OUT} = 3.0V	1.0	2.0	4.0	mA
High level output current	D1, D2, D3, LED	V_{OUT} = 4.5V			10	μA
	a,b,c,d,e,f, g, DP.	V_{OUT} = 2.6V	2.0	3.0	4.1	mA

MODE	FUNCTION
Power on Reset	8.8.8. is displayed for up to 1 second after switch on and all internal circuits are reset. This overrides all other functions.
Low Temperature Measurement	3.4.9. will be displayed for temperatures lower than 35.0°C.
High Temperature Measurement	For temperatures greater than 42.9°C, the temperature will be displayed up to a maximum of 47.6°C but all the decimal points will be on.
Normal Temperature Measurement	The temperature will be displayed for temperatures from 35.0°C to 42.9°C with a resolution of 0.1°C at a sample rate of approximately 3 per second.
Maximum Temperature Measurement	When the display maximum input is low, the maximum recorded temperature is displayed.
Hold Reading	While the display hold input is held low, the reading in the display will remain the same.
Test Sequence	While the test input is held low, the display will count from 3.4.9. up to a maximum of 4.7.9. and then back to 3.4.9. etc. at a rate of approximately 3Hz.
Lamp Test	8.8.8. is displayed during power on reset and also if the battery voltage is below a preset level.
Green LED	The green LED will be on if the battery voltage is above a preset level.

ZN412

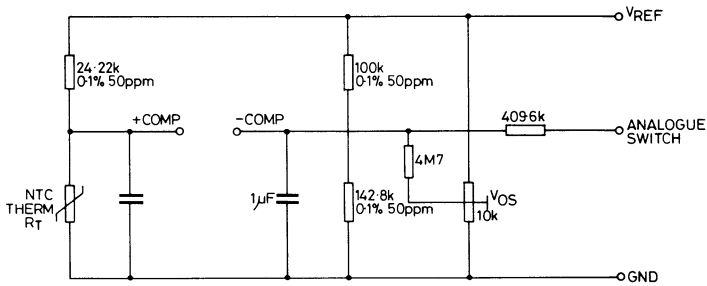
Application

All the external components required are shown except the test resistor which is switched into circuit instead of the thermister to give a reading of 45.0°C.



Input Circuit

A possible circuit configuration that can be used to null out comparator offsets without introductions. Additional gain errors is given below:–



The thermister used had the following approximate characteristics:–

T°C	RTKΩ
25	60
35	39.441
36	37.883
37	36.366
38	34.931
39	33.560
40	32.249
45	26.508

$$R_T = R_O \times e^{B^*\left(\frac{1}{T} - \frac{1}{T_O}\right)}$$

with $B^* = B\,(1 - 5 \times 10^{-4}\,(t - 100))$

B = material constant = 3980°K

T_O = Reference temp. in °K (25°C = 293°K)

T = Probe Temp. in °K

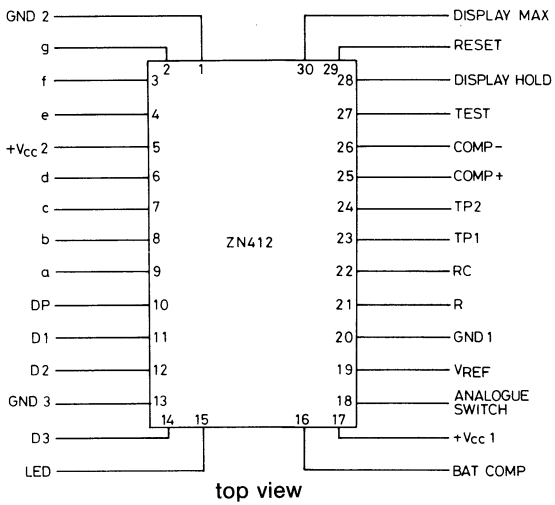
R_O = Thermistor value at 25°C (60KΩ)

R_T = Thermistor value at temp. T°K in KΩ

t = probe temp. in °C

The above information is given for guidance only and may not represent an optimum circuit configuration.

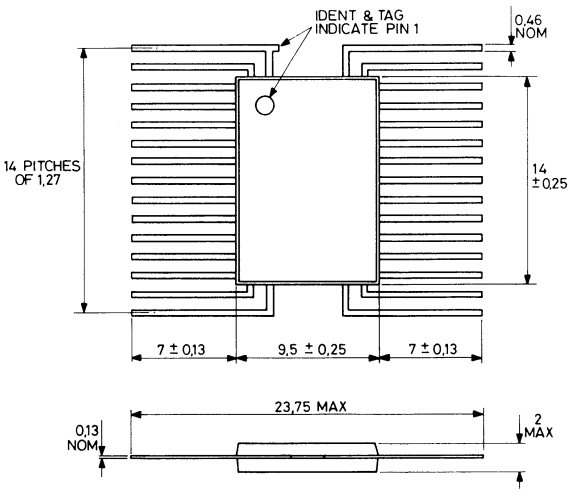
PINNING DIAGRAM



top view

30 Pin Plastic Flat Pack

PACKAGE OUTLINE



Dimensions in millimetres

3. Precision Voltage References

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ZNREF 040	4,0 V Precision Voltage Reference (trimmable)	3-26
ZNREF 050	5,0 V Precision Voltage Reference (trimmable)	3-30
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PRODUCT SELECTION GUIDE
PRECISION VOLTAGE REFERENCES

Type Number	Nominal Output Voltage	Output Voltage Tolerance	Current Range (mA)		Dynamik Impedance (Ω)		Temperature Coefficient (ppm/°C)		Temperature Range (°C)		Package	Features	Page
			min.	max.	typ.	max.	typ.	max.	min.	max.			
ZN423	1.26	± 4.76%	1.5	12	0.5	1.0	30	100	−55	125	TO-18 2 Lead	60dB Power Supply Rejection 6 μV RMS Noise	3-6
ZN404	2.45	± 2.86%	2.0	120	0.2	0.4	35	145	0	70	TO-18 2 Lead	Low Cost no shaping capacitor requ.	3-3
ZN458	2.45	+ 1.6% − 1.2%	2.0	120	0.1	0.2	58	100	−20	70	TO-18 2 Lead	Low Slope Resistance 10 μV RMS Noise No shaping capacitor requ.	3-13
ZN458A	2.45	+ 1.6% − 1.2%	2.0	120	0.1	0.2	35	50	−20	70	TO-18 2 Lead	Medium Voltage Change 6mV over Temperature	3-13
ZN458B	2.45	+ 1.6% − 1.2%	2.0	120	0.1	0.2	23	29	−20	70	TO-18 2 Lead	Low Temp. Coefficient	3-13
ZNREF025A1	2.50	± 1%	0.15	10	1.5	2	35	50	−55	125	TO-18 3 Lead	ZNREF parts are also available with 2% and 3% Output Voltage Tolerance. This Tolerance can be trimmed ± 5% (± 2,5% for ZNREF100) ZNREF Series parts are maskprogrammable between 2,5 V and 10 V	3-21
C1							15	50	0	70			
ZNREF040A1	4.01	± 1%	0.15	75	2	3	35	50	−55	125	TO-18 3 Lead		3-25
C1							15	50	0	70			
ZNREF050A1	4.90	± 1%	0.15	60	1.5	2	35	50	−55	125	TO-18 3 Lead		3-29
C1							15	50	0	70			
ZNREF062AB1	6.17	± 1%	0.15	50	2	3	25	40	−55	110	TO-18 3 Lead		3-33
C1							15	50	0	70			
ZNREF100A1	9.80	± 1%	0.15	50	3	4	35	50	−55	125	TO-39 6 Lead		3-37
C1							15	60	0	70			

FERRANTI semiconductors

ZN404

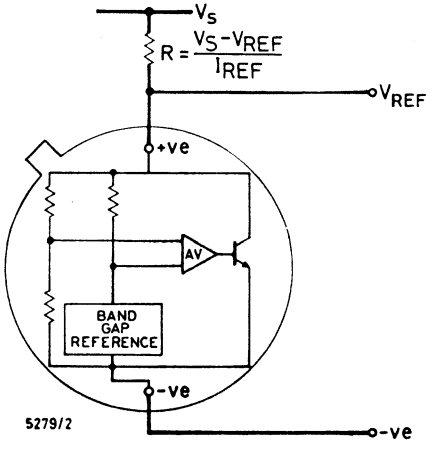
2·45 Volt Precision Reference Regulator

FEATURES

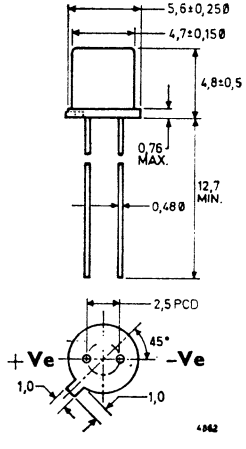
- **Low temperature coefficient**
- **Low slope resistance**
- **Very good long term stability**
- **Low noise**
- **Internally shaped**
- **Tight tolerance**
- **Two pin package**

DESCRIPTION

The ZN404 is a monolithic integrated circuit providing a precise stable regulator source of 2.45 volts in a two lead package without the need for an external shaping capacitor.



Circuit diagram



Lead Configuration
Dimensions in millimetres

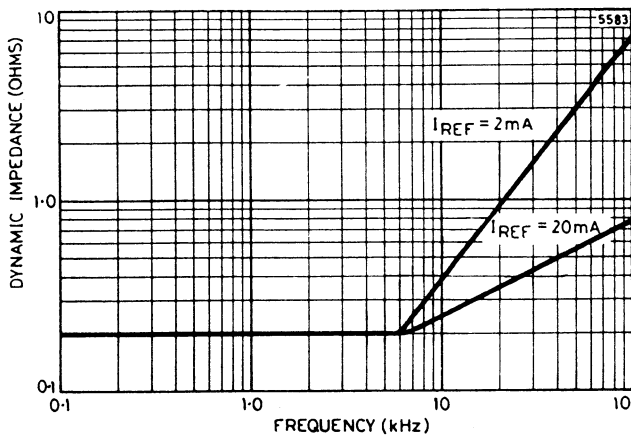
ZN404

MAXIMUM RATINGS

Dissipation .. .. 300 mW
Operating Temperature Range .. .. 0 to + 70°C
Storage Temperature Range .. .. –55 to +150°C

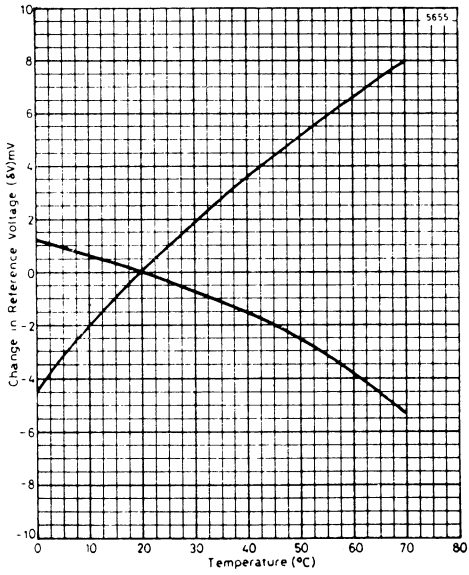
ELECTRICAL CHARACTERISTICS (at 25°C ambient temperature unless otherwise stated).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage	V_{REF}	2.38	2.45	2.52	V	Measured at 2 mA
Slope Resistance	R_{REF}	—	0.2	0.4	Ω	
Reference Current	I_{REF}	2	—	120	mA	
Maximum Change in V_{REF}	ΔV_{REF}	—	6	25	mV	0 to +70°C
Temperature coefficient		—	35	145	ppm/°C	

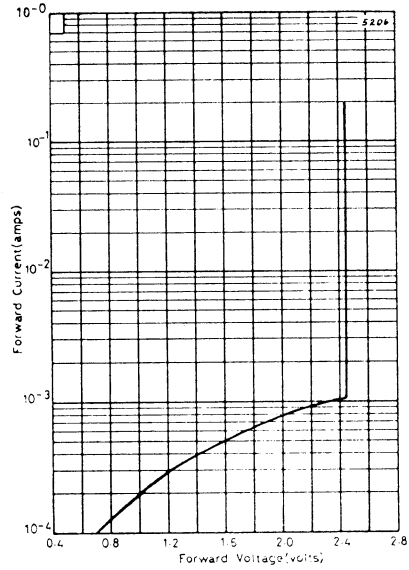


DYNAMIC IMPEDANCE

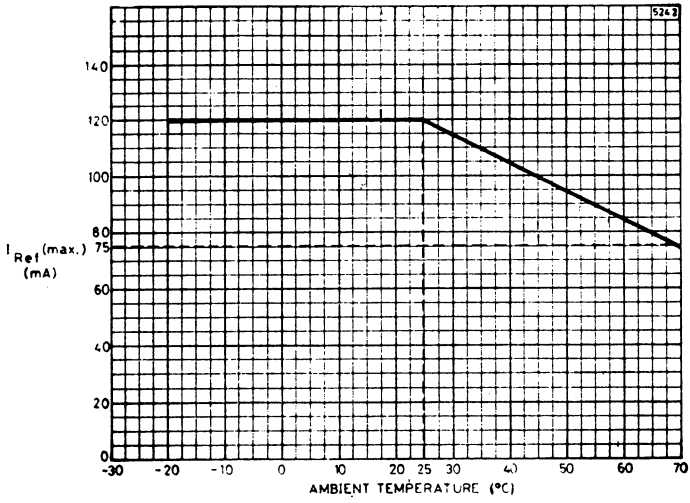
TEMPERATURE CHARACTERISTIC
(Typical)



FORWARD CHARACTERISTIC
(Typical)



DERATING CURVE



ZN423

FERRANTI semiconductors

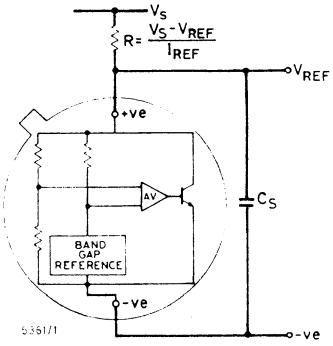
1·26 Volt Precision Voltage Reference Source

FEATURES

- Low voltage
- Low temperature coefficient
- Very good long term stability
- Low slope resistance
- Low RMS noise
- Tight tolerance
- High power supply rejection ratio
- Two pin package

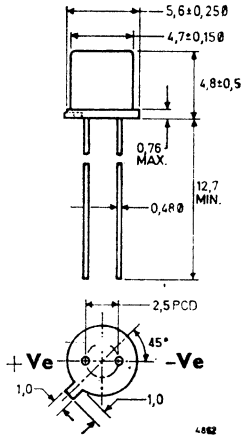
DESCRIPTION

The ZN423 is a monolithic integrated circuit utilising the energy band gap voltage of a base-emitter junction to produce a precise, stable, reference source of 1.26 volts. This is derived via an external dropping resistor for supply voltages of 1.5 volts upwards. The temperature coefficient of the ZN423, unlike conventional Zener diodes, remains constant with reference current. The noise figure associated with breakdown mechanisms is also considerably reduced.



Circuit diagram

PACKAGE OUTLINE



2 LEAD TO-18
Pinning configuration

Dimensions in millimetres

ABSOLUTE MAXIMUM RATINGS

Reference current I_{REF} .. .. 20 mA
Operating temperature range .. .. 0°C to + 70°C
–55°C to +125°C
Storage temperature range .. .. –65°C to +165°C

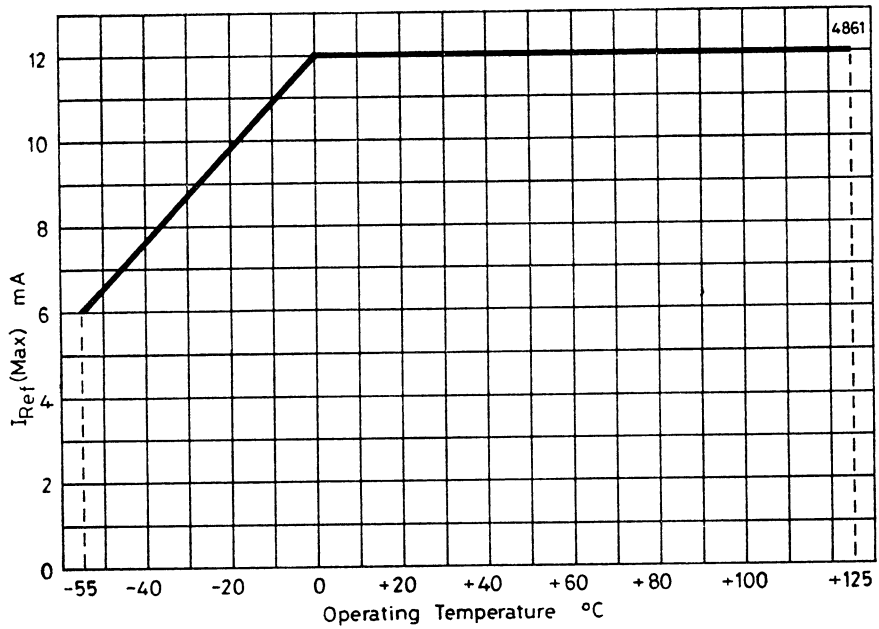
ELECTRICAL CHARACTERISTICS (at ambient temperature of 25°C unless otherwise stated).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Output voltage	V_{REF}	1.2	1.26	1.32	V	
Slope resistance	R_{REF}	—	0.5	1.0	Ω	1
Reference current	I_{REF}	1.5	—	12	mA	
Temperature coefficient		—	30	100	ppm/°C	
Shaping capacitance	C_S	0.1	—	—	μF	
External resistance	R_{EXT}	100	—	—	Ω	2
R.M.S. noise voltage 1 Hz to 10 kHz		—	6	—	μV	
Power supply rejection ratio $V_{REF} = 1.26V$ $I_{REF} = 2 \cdot 5mA$ $V_{CC} = 5.0V$	PSRR	—	60	—	dB	3
V_{REF} drift at 125°C	σV_{REF}	— —	10 100	— —		ppm/1000 hours ppm/year

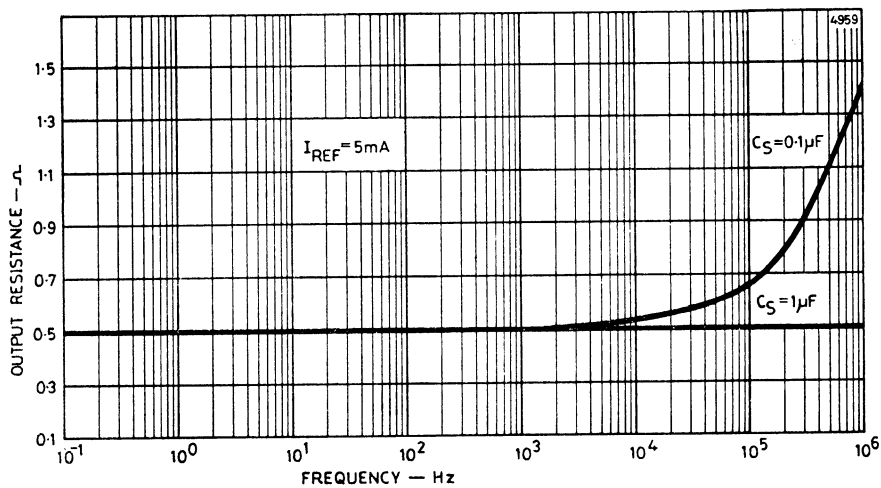
Note 1 $I_{REF} = 5$ mA
Note 2 $R_{EXT} = (V_{CC} - V_{REF})/I_{REF}$
Note 3 PSRR = R_{EXT}/R_{REF}

DERATING CURVE

Reference current I_{REF} (max.) vs Operating temperature.



Slope resistance vs Frequency (I_{REF} = 5 mA).



APPLICATIONS

1. 5 Volt, 0.5 Amp Power Supply.

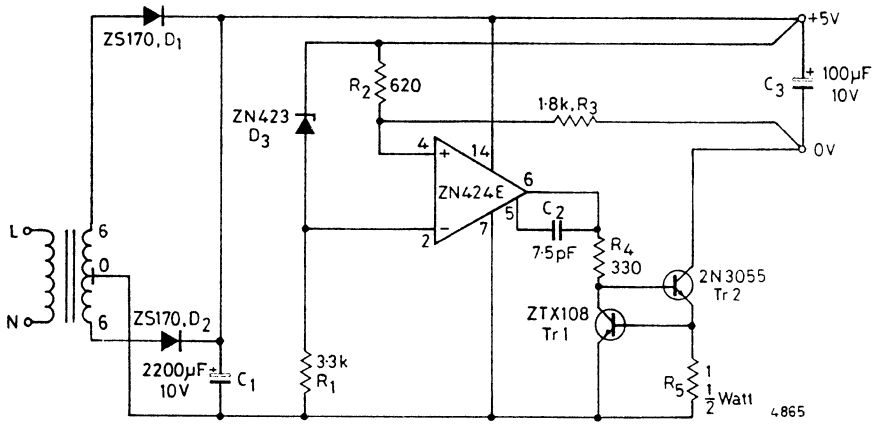


Figure 1.

This circuit is essentially a constant current source modified by the feedback components R_2 and R_3 to give a constant voltage output.

The output of the ZN424E need only be 2 volts above the negative rail, by placing the load in the collector of the output transistor Tr_2. Current circuit is achieved by Tr_1 and R_5 This simple circuit has the following performance characteristics:

Output noise and ripple (Full load) = 1 mV r.m.s.

Load regulation (0 to 0.5A) = 0.1%.

Temperature coefficient = ±100 ppm/°C.

Current limit = 0.65A.

2. 5 Volt, 1.0 Amp Power supply.

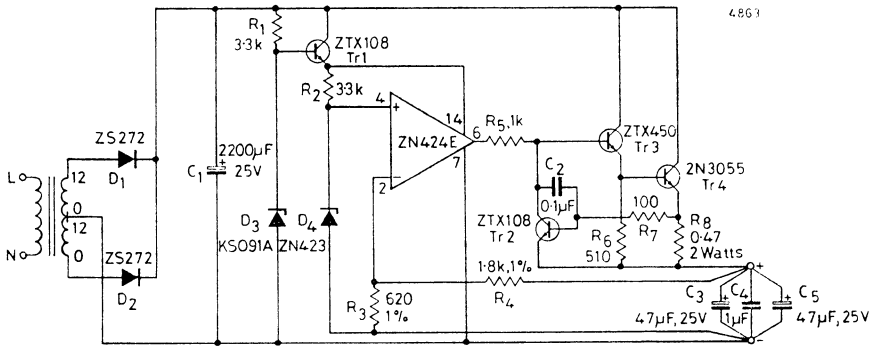


Figure 2.

The circuit detailed in Figure 2 provides improved performance over that in Figure 1. This is achieved by feeding the ZN423 reference and the ZN424E error amplifier from a more stable source, derived from the emitter-follower stage (Tr_1). The supply rejection ratio is improved by the factor R_1/R_S, where R_S is the slope resistance of D_3. The output voltage is given by: $\frac{(R_3 + R_4)}{R_3} . V_{REF}$ and may be adjusted by replacing R_3 with a 220Ω and a 500Ω preset potentiometer.

The output is protected against short circuits by Tr_2 setting a current limit of 1.6A.

3. 0 to 12 Volt, 1 Amp Power Supply.

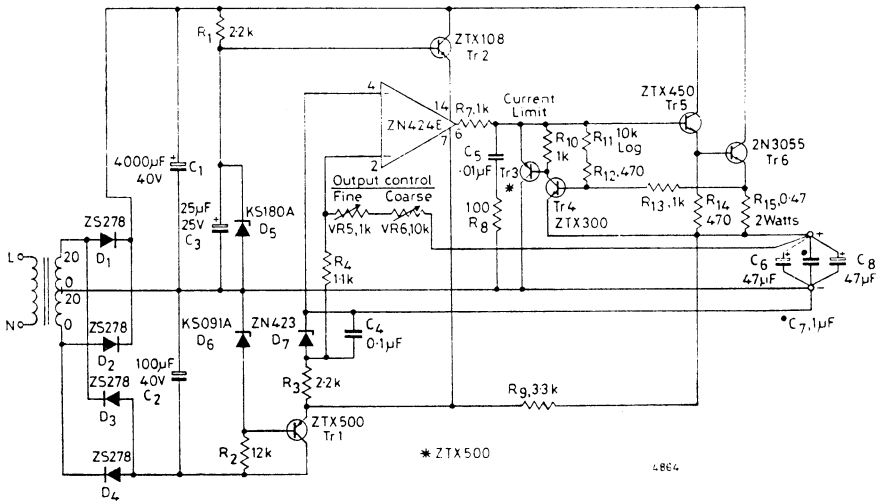


Figure 3.

The above circuit provides a continuously variable, highly stable voltage for load currents up to 1A.

The output voltage is given by: $V_O = \frac{(V_{R5} + V_{R6})}{R_4} V_{REF}$,

and is controlled by V_{R5} and V_{R6} which should be high quality components (preferably wire wound).

The emitter follower stages Tr_1 and Tr_2 buffer the bias and reference from the output stage. The negative rail allows the output to operate down to 0 volts.

The current limit stage monitors output current through R_{15}. As the potential across R_{15} increases due to load current, Tr_4 conducts and supplies base current for Tr_3, thus diverting part of the output from the ZN424E, via Tr_3 to Tr_5.

Shaping is achieved by the network C_5, R_8 together with the output decoupling capacitors which also maintain low output resistance at frequencies above 100 kHz.

The power supply has the following performance characteristics:

Output noise and ripple (Full load)	<100 μV r.m.s.
Output resistance (0 to 1 Amp)	1 mΩ
Temperature coefficient	±100 ppm/°C

4. Variable Current Source, 100 mA to 2 Amps.

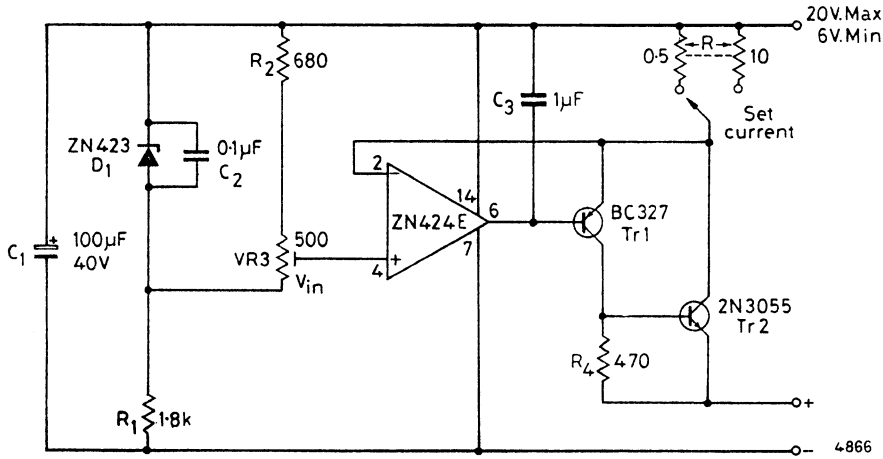


Figure 4.

In this circuit the output current is set by the resistor R in the collector of Tr_2, which may be switched to offer a range of output currents from 100 mA to 2A with fine control by means of VR3 which varies the reference voltage to the non-inverting input of the ZN424E.

The feedback path from the output to the inverting input of the ZN424E maintains a constant voltage across R, equal to $(V_{CC} - V_{in})$ and hence a constant current to the load given by $(V_{CC} - V_{in})/R$.

FERRANTI
semiconductors

ZN458, A, B

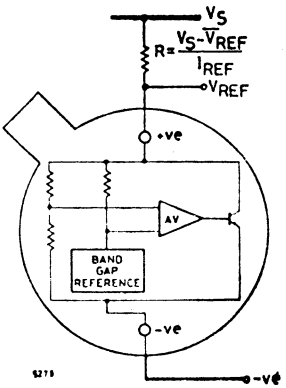
2,45 V Precision Voltage Reference

FEATURES

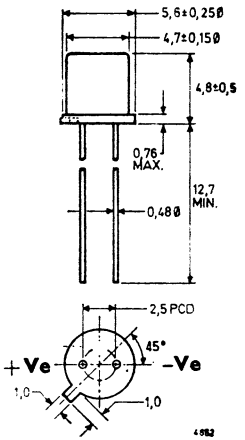
- Guaranteed 5 mV maximum deviation over full temperature range
- Low temperature coefficient 0·003%/°C
- Low slope resistance – 0·1Ω
- Very good long term stability – 10 ppm
- Low noise – 10 μV
- Internally shaped
- Tight tolerance ±1·43%
- Two pin package
- Wide operating current 2 – 120 mA

DESCRIPTION

The ZN458 is a monolithic integrated circuit providing a precise stable reference source of 2·45 volts in a two lead package without the need for an external shaping capacitor.



Circuit Diagram



Pinning Configuration
Dimensions in millimetres

ZN458, A, B

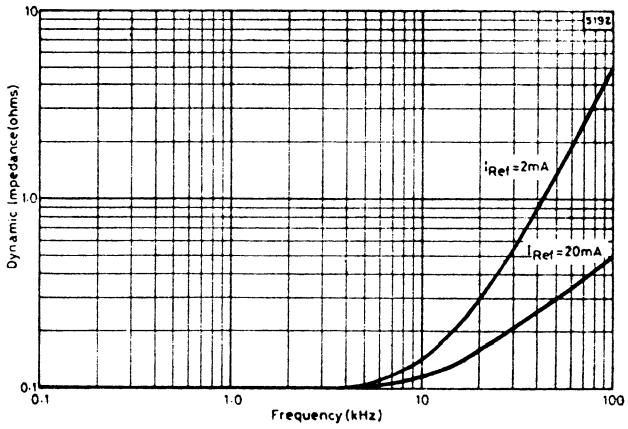
MAXIMUM RATINGS

Dissipation .. .. 300 mW
Operating Temperature Range .. .. −20 to +70°C
Storage Temperature Range .. .. −55 to +150°C

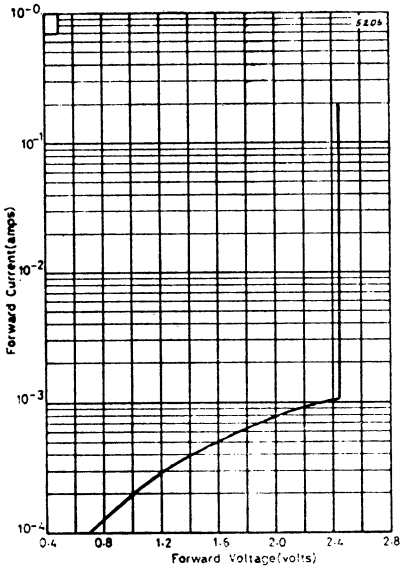
ELECTRICAL CHARACTERISTICS (at 25°C ambient temperature unless otherwise stated).

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Output Voltage		V_{REF}	2·42	2·45	2·49	V	Measured at 2 mA
Slope Resistance		R_{REF}	—	0·1	0·2	Ω	
Reference Current		I_{REF}	2·0	—	120	mA	
Maximum Change in V_{REF}	ZN458	ΔV_{REF}	—	10	17	mV	0° to +70°C
	ZN458A		—	6	8·5		
	ZN458B		—	4	5		
RMS Noise Voltage 1 Hz to 10 kHz			—	10	—	μV	
V_{REF} Drift at 70°C			—	±10	—	ppm/1000 hours	

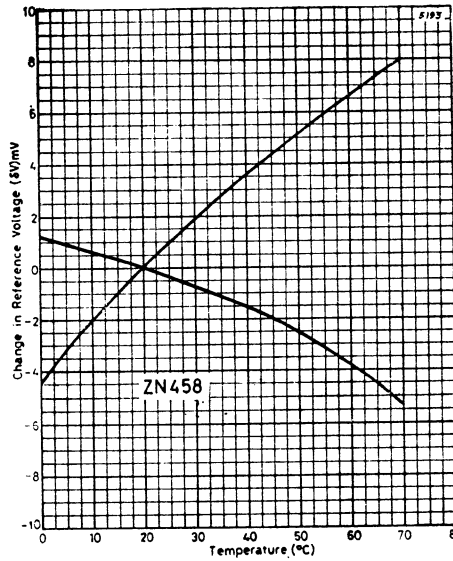
DYNAMIC IMPEDANCE



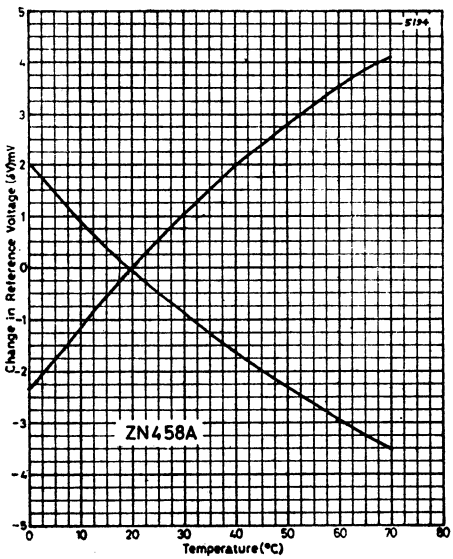
FORWARD CHARACTERISTIC

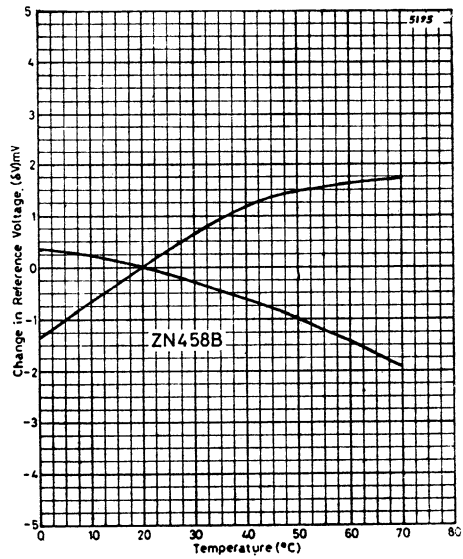


TEMPERATURE CHARACTERISTIC (Typical)

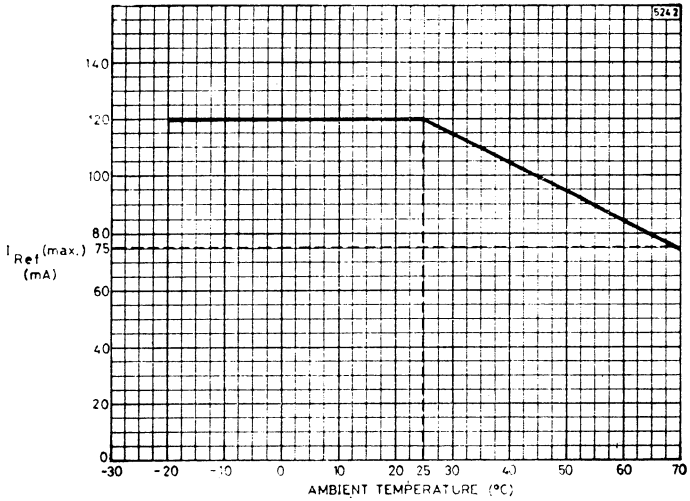


TEMPERATURE CHARACTERISTICS (Typical)





DERATING CURVE



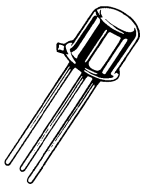
FERRANTI semiconductors

ZNREF SERIES

ZNREF Low Power Precision Reference Sources

FEATURES

- Trimmable output
- Excellent temperature stability
- Low output noise figure
- Available in two temperature ranges
- 1, 2 and 3% initial voltage tolerance versions available
- No external stabilising capacitor required in most cases
- Low slope resistance



TO-18 PACKAGE

TO-39 (6 Lead) PACKAGE

DESCRIPTION

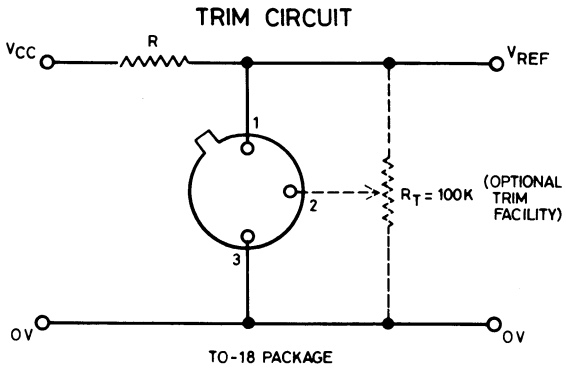
The ZNREF series is a range of monolithic integrated circuits providing precise stable reference voltages from 2.5 volts (ZNREF025) to 10 volts (ZNREF100).

The range features a knee current of 150μA and operation over a wide range of temperatures and currents.

The devices are available in metal can packages with one of the pins offering a trim facility whereby the output voltage can be adjusted using the circuits overleaf - (Fig. 2 for ZNREF100 and Fig. 1 for other voltages). This facility is used when compensating for system errors or setting the reference output to a particular value. When the trim facility is not used the relevant pin should be left open circuit.

Fig. 1 ZNREF025/040/050 and 062

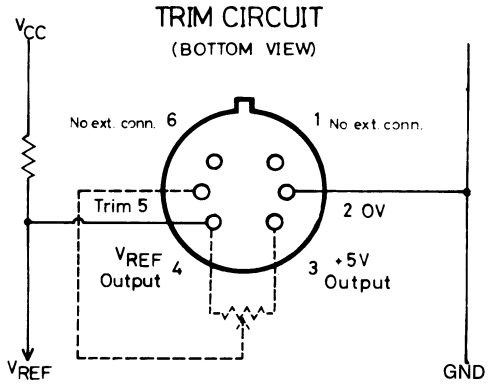
$$R = \frac{V_{CC} - V_{REF}}{I_{REF}}$$



N.B. Case is internally connected to 0V

Fig. 2 ZNREF100

$$R = \frac{V_{CC} - V_{REF}}{I_{REF}}$$



No connection should be made to pins 1 and 6

Type Number	Nominal Output Voltage*	Maximum Operating Current (mA)	Dynamic Impedance		Trim Range	Package
			Typ.	Max.		
ZNREF025	2.50	10	1.5	2.0	±5%	TO-18
ZNREF040	4.01	75	2.0	3.0	±5%	TO-18
ZNREF050	4.90	60	1.5	2.0	±5%	TO-18
ZNREF062	6.17	50	2.0	3.0	±5%	TO-18
ZNREF100	9.80	50	3.0	4.0	±2.5%	6 lead TO-39

*Measured at 500μA

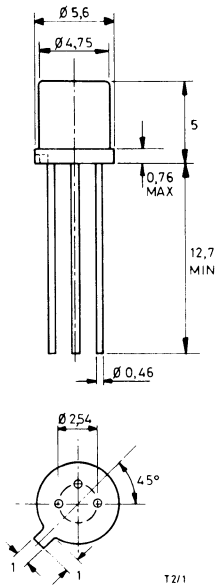
ORDERING INFORMATION

Device		Tol. %	(max.)T.C. (ppm/°C)	Temperature Range
ZNREF	†A1	1	50	−55 to +125°C
ZNREF	†A2	2		
ZNREF	†A3	3	80	
ZNREF	C1	1	50	0 to +70°C
ZNREF	C2	2		
ZNREF	C3	3	60	

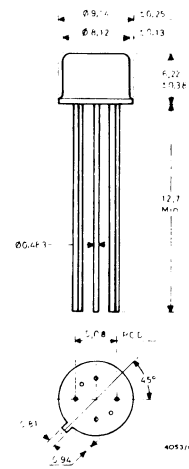
†AB Grade (−55 to +110°C) for ZNREF062

ZNREF SERIES

PACKAGE OUTLINE
Dimensions in mm.
(TO-18)

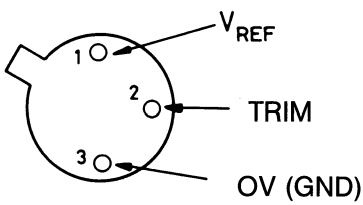


(TO-39)

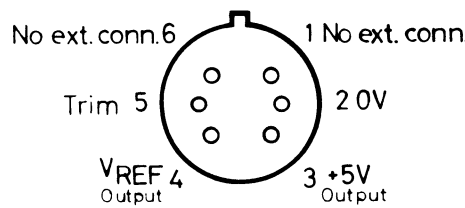


CONNECTION DIAGRAM

TO-18 Metal Can
(Bottom View)



TO-39 Metal Can
(Bottom View)



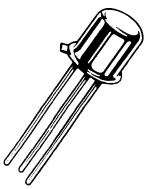
FERRANTI
semiconductors

ZNREF 025

2.5 Volt Low Power Precision Reference Source

FEATURES

- Trimmable output
- Excellent Temperature Stability
- Low output noise figure
- Low Dynamic Impedance
- Available in two temperature ranges
- 1%, 2% and 3% initial voltage tolerance versions available



TO-18 PACKAGE

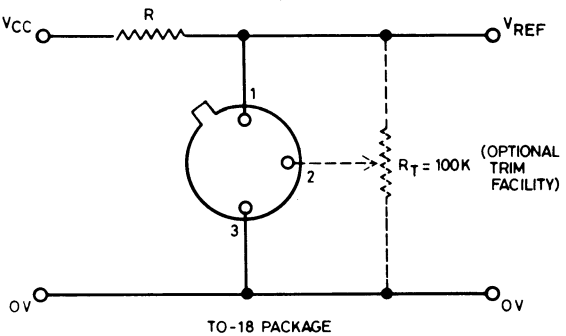
DESCRIPTION

The ZNREFO25 is a monolithic integrated circuit providing a precise, stable reference source of 2.5 volts in a three pin TO-18 metal can transistor package.

The use of the third pin is optional and enables V_{REF} to be trimmed by ±5%. This is useful for taking out system errors or setting V_{REF} to specific values, e.g. 2.500 volts for a standard calibration source or 2.56 volts for binary systems.

$$R = \frac{V_{CC} - V_{REF}}{I_{REF}}$$

TRIM CIRCUIT



TO-18 PACKAGE

N.B. Case is internally connected to 0V

ZNREF 025

ABSOLUTE MAXIMUM RATINGS

Reference Current	10mA*
Power Dissipation	300mW
Operating Temperature Range	See below
Storage Temperature Range	−55 to +175°C
Soldering temperature for a maximum time of 10s within $^1/_{16}$" of the seating plane	300°C
within $^1/_{32}$" of the seating plane	265°C

*Below −25°C this figure should be linearly derated to 1.5mA maximum at −55°C.

TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial Voltage Tolerance %	Grade A −55 to 125°C		Grade C 0 to 70°C		Units
			Typ.	Max.	Typ.	Max.	
Output voltage change over relevant temperature range (See Note (a))	ΔV_{REF}	1 & 2	16.0	22.5	2.7	8.8	mV
		3	25.0	36.0	3.2	10.5	
Output voltage temperature coefficient (See Note (b))	TCV_{REF}	1 & 2	35	50	15	50	ppm/°C
		3	56	80	18	60	

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C and Pin 2 o/c unless otherwise noted). **(LOAD CAPACITANCE** should be less than 220pF or greater than 22nF).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage	V_{REF}					
1% Tolerance (A1 C1)		2.475	2.500	2.525	V	I_{REF} = 500μA
2% Tolerance (A2 C2)		2.450	2.500	2.550		
3% Tolerance (A3 C3)		2.425	2.500	2.575		
Output voltage adjustment range	ΔV_{TRIM}	–	±5	–	%	R_T = 100kΩ
Change in TCV_{REF} with output adjustment	$TC\Delta V_{TRIM}$	–	0.8	–	ppm/°C/%	
Operating current range	I_{REF}	0.15	–	10	mA	See Note (c)
Turn-on time	t_{on}	–	40	–	μS	R_L = 1kΩ
Turn-off time	t_{off}	–	0.3	–		
Output voltage noise (over the range 0.1Hz to 10Hz)	e_{np-p}	–	50	–	μV	Peak to peak measurement
Slope resistance	R_{REF}	–	1.5	2.0	Ω	I_{REF} 0.5mA to 5mA See Note (d)

NOTES

a) OUTPUT CHANGE WITH TEMPERATURE (ΔV_{REF}) the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{REF} = V_{max} - V_{min}$$

b) OUTPUT TEMPERATURE COEFFICIENT (TCV_{REF})
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/C°}$$

ΔT = Full temperature change.

c) OPERATING CURRENT (I_{REF})
Maximum operating current must be derated as indicated in Maximum Ratings.

d) SLOPE RESISTANCE (R_{REF})
The dynamic impedance is defined as

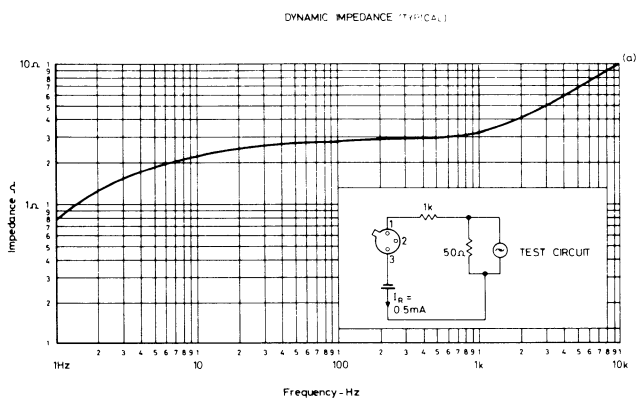
$$R_{REF} = \frac{\text{CHANGE IN } V_{REF} \text{ OVER SPECIFIED CURRENT RANGE}}{\Delta I_{REF}}$$

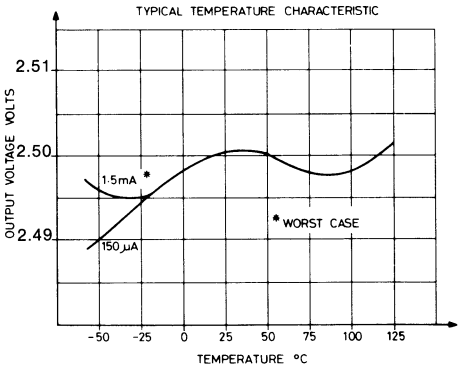
$\Delta I_{REF} = 5 - 0.5 = 4.5\text{mA}$ (typically)

e) LINE REGULATION
The ratio of change in output voltage to the change in input voltage producting it.

$$\frac{R_{REF} \times 100 \text{ \%/V}}{V_{REF} \times R_S}$$

R_S = Source resistance.



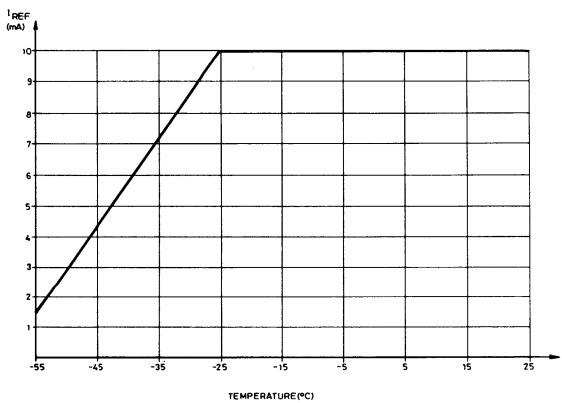


ZNREF 025

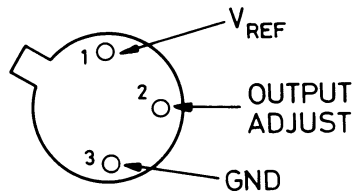
ORDERING INFORMATION

DEVICE	TOL %	(max.)T.C.(ppm/°C)	Temp. Range
ZNREF A1	1	50	−55°C to + 125°C
ZNREF A2	2		
ZNREF A3	3	80	
ZNREF C1	1	50	0°C to + 70°C
ZNREF C2	2		
ZNREF C3	3	60	

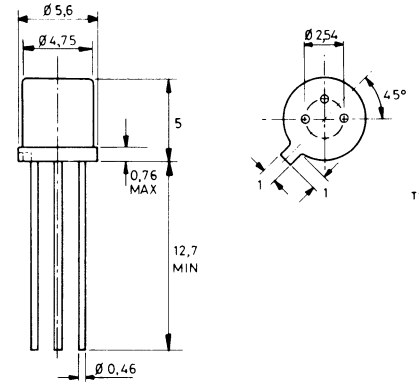
I_{REF} DERATING FOR ZNREF025A



CONNECTION DIAGRAM
TO-18 Metal Can (Bottom View)



PACKAGE OUTLINE
(TO-18) Dimensions in mm.



BS.3934
JEDEC

SO-12A
TO-18

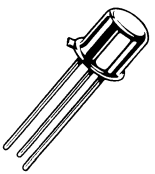
FERRANTI semiconductors

ZNREF 040

4 Volt Low Power Precision Reference Source

FEATURES

- Trimmable output
- Excellent Temperature Stability
- Low output noise figure
- Low Dynamic Impedance
- Available in two temperature ranges
- 1, 2 and 3% initial voltage tolerance versions available
- No external stabilising capacitor required in most cases



TO-18 PACKAGE

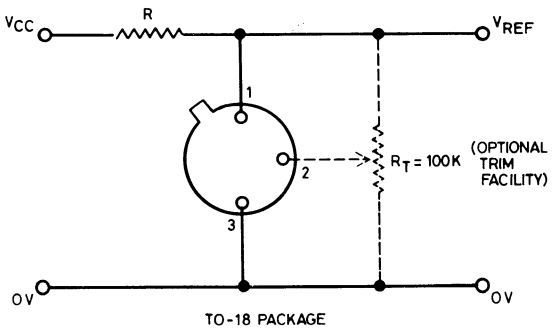
DESCRIPTION

The ZNREF040 is a monolithic integrated circuit providing a precise, stable reference source of 4 volts in a three pin TO-18 metal can transistor package.

The ZNREF040 is unconditionally stable under all load conditions without the need for an external shaping capacitor.

The use of the third pin is optional and enables V_{REF} to be trimmed by $\pm 5\%$. This is useful for taking out system errors or setting V_{REF} to specific values, e.g. 4.000 volts for a standard calibration source or 4.096 volts for binary systems.

TRIM CIRCUIT



$$R = \frac{V_{CC} - V_{REF}}{I_{REF}}$$

N.B. Case is internally connected to 0V

ZNREF 040

ABSOLUTE MAXIMUM RATINGS

Reference Current 75mA*
Power Dissipation 300mW
Operating Temperature Range .. .. See below
Storage Temperature Range .. .. −55 to +175°C
Soldering temperature for a maximum time of 10s
within $^1/_{16}$" of the seating plane .. .. 300°C
within $^1/_{32}$" of the seating plane .. .. 265°C

*Above 25°C this figure should be linearly derated to 25mA at +125°C.

TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial Voltage Tolerance %	Grade A −55 to 125°C		Grade C 0 to 70°C		Units
			Typ.	Max.	Typ.	Max.	
Output voltage change over relevant temperature range (See Note (a))	ΔV_{REF}	1 & 2	25.6	36	4.2	14	mV
		3	40	57	5.1	16.8	
Output voltage temperature coefficient (See Note (b))	TCV_{REF}	1 & 2	35	50	15	50	ppm/°C
		3	56	80	18	60	

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C and Pin 2 o/c unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage	V_{REF}					
1% Tolerance (A1 C1)		3.97	4.01	4.05	V	I_{REF} = 500μA
2% Tolerance (A2 C2)		3.93	4.01	4.09		
3% Tolerance (A3 C3)		3.89	4.01	4.13		
Output voltage adjustment range	ΔV_{TRIM}	−	±5	−	%	R_T = 100kΩ
Change in TCV_{REF} with output adjustment	$TC\Delta V_{TRIM}$	−	0.8	−	ppm/°C/%	
Operating current range	I_{REF}	0.15	−	75	mA	See Note (c)
Turn-on time	t_{on}	−	40	−	μS	R_L = 1kΩ
Turn-off time	t_{off}	−	0.3	−		
Output voltage noise (over the range 0.1Hz to 10Hz)	e_{np-p}	−	50	−	μV	Peak to peak measurement
Slope resistance	R_{REF}	−	2	3	Ω	I_{REF} 0.5mA to 5mA, See Note (d)

NOTES

(a) OUTPUT CHANGE WITH TEMPERATURE (ΔV_{OT}) the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{OT} = V_{max} - V_{min}$$

(b) OUTPUT TEMPERATURE COEFFICIENT (TCV_o)
The ratio of the output voltage change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_o = \frac{\Delta V_{OT} \times 10^6}{V_O \times \Delta T} \text{ ppm/°C} \qquad \Delta T = \text{Full temperature change.}$$

(c) OPERATING CURRENT (I_{REF})
Maximum operating current must be derated as indicated in Maximum Ratings.

(d) DYNAMIC IMPEDANCE (R_D)
The dynamic impedance is defined as

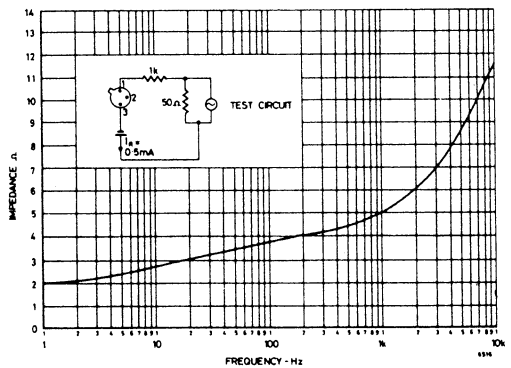
$$R_D = \frac{\text{CHANGE IN } V_O \text{ OVER SPECIFIED CURRENT RANGE}}{\Delta I_{REF}}$$

$$\Delta I_{REF} = 5 - 0.5 = 4.5\text{mA (typically)}$$

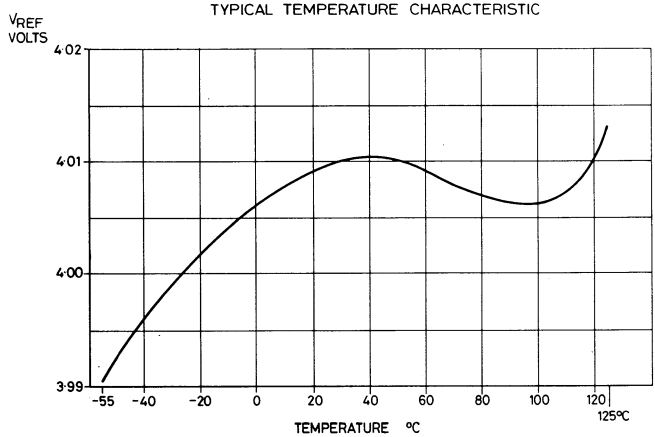
(e) LINE REGULATION (ΔV_{OL})
The ratio of the change in output voltage to the change in input voltage producing it.

$$\Delta V_{OL} = \frac{R_D \times 100}{V_O \times R_S} \%/V \qquad R_S = \text{Source resistance}$$

DYNAMIC IMPEDANCE (TYPICAL)



TYPICAL TEMPERATURE CHARACTERISTIC

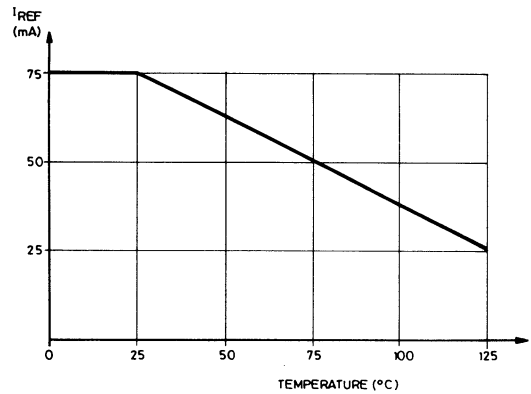


ZNREF 040

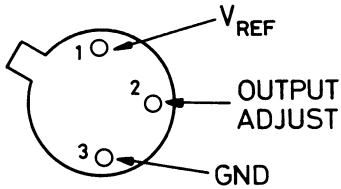
ORDERING INFORMATION

DEVICE	TOLERANCE (%)	T.C. (Max) – ppm/°C	Temperature Range
ZNREF040 A1	1	50	–55°C to +125°C
ZNREF040 A2	2		
ZNREF040 A3	3	80	
ZNREF040 C1	1	50	0°C to +70°C
ZNREF040 C2	2		
ZNREF040 C3	3	60	

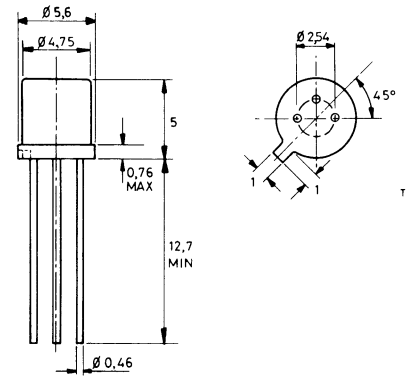
I_{REF} DERATING FOR ZNREF040



CONNECTION DIAGRAM
TO-18 Metal Can (Bottom View)



PACKAGE OUTLINE
(TO-18) Dimensions in mm.



BS.3934
JEDEC

SO-12A
TO-18

FERRANTI semiconductors

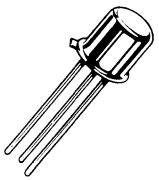
ZNREF 050

5 Volt Low Power Precision Reference Source

ADVANCE PRODUCT INFORMATION

FEATURES

- Trimmable output
- Excellent Temperature Stability
- Low output noise figure
- Low Dynamic Impedance
- Available in two temperature ranges
- 1%, 2% and 3% initial voltage tolerance versions available
- No external stabilising capacitor required

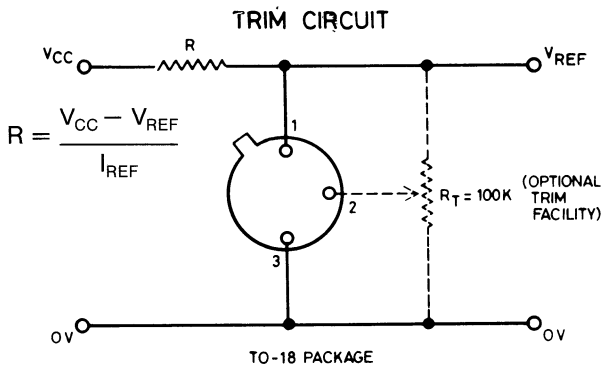


TO-18 PACKAGE

DESCRIPTION

The ZNREFO50 is a monolithic integrated circuit providing a precise, stable reference source of 5 volts in a three pin TO-18 metal can transistor package.
The ZNREFO50 is unconditionally stable under all load conditions without the need for an external shaping capacitor.

The use of the third pin is optional and enables V_{REF} to be trimmed by ±5%. This is useful for taking out system errors or setting V_{REF} to specific values.



N.B. Case is internally connected to 0V

ZNREF O50

ABSOLUTE MAXIMUM RATINGS

Reference Current 60mA*
Power Dissipation 300mW
Operating Temperature Range .. .. See below
Storage Temperature Range .. .. −55 to +175°C
Soldering temperature for a maximum time of 10s
within $^1/_{16}$" of the seating plane .. .. 300°C
within $^1/_{32}$" of the seating plane .. .. 265°C

*Above 25°C this figure should be linearly derated to 20mA at +125°C.

TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial Voltage Tolerance %	Grade A −55 to 125°C		Grade C 0 to 70°C		Units
			Typ.	Max.	Typ.	Max.	
Output voltage change over relevant temperature range (See Note (a))	ΔV_{REF}	1 & 2	32	45	5.4	17.2	mV
		3	51	72	6.4	20.6	
Output voltage temperature coefficient (See Note (b))	TCV_{REF}	1 & 2	35	50	15	50	ppm/°C
		3	57	80	18	60	

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C and Pin 2 o/c unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage	V_{REF}					
1% Tolerance (A1 C1)		4.85	4.90	4.95	V	I_{REF} = 500μA
2% Tolerance (A2 C2)		4.80	4.90	5.00		
3% Tolerance (A3 C3)		4.75	4.90	5.05		
Output voltage adjustment range	ΔV_{TRIM}	–	±5	–	%	R_T = 100kΩ
Change in TCV_{REF} with output adjustment	$TC\Delta V_{TRIM}$	–	0.8	–	ppm/°C/%	
Operating current range	I_{REF}	0.15	–	60	mA	See Note (c)
Turn-on time	t_{on}	–	40	–	μS	R_L = 1kΩ
Turn-off time	t_{off}	–	0.3	–		
Output voltage noise (over the range 0.1Hz to 10Hz)	e_{np-p}	–	50	–	μV	Peak to peak measurement
Slope resistance	R_{REF}	–	1.5	2	Ω	I_{REF} 0.5mA to 5mA See Note (d)

a) OUTPUT CHANGE WITH TEMPERATURE(ΔV_{OT}) the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$V_{OT} = V_{max} - V_{min}$$

b) OUTPUT TEMPERATURE COEFFICIENT (TCVo)
The ratio of the output voltage change with temperature to the specified temperature range expressed in p.p.m/°C.

$$TCV_o = \frac{\Delta V_{OT} \times 10^6}{V_O \times \Delta T} \text{ ppm/°C}$$

ΔT = Full temperature change.

c) OPERATING CURRENT (I_{REF})
Maximum operating current must be derated as indicated in Maximum Ratings.

d) DYNAMIC IMPEDANCE (R_D)
The dynamic impedance is defined as

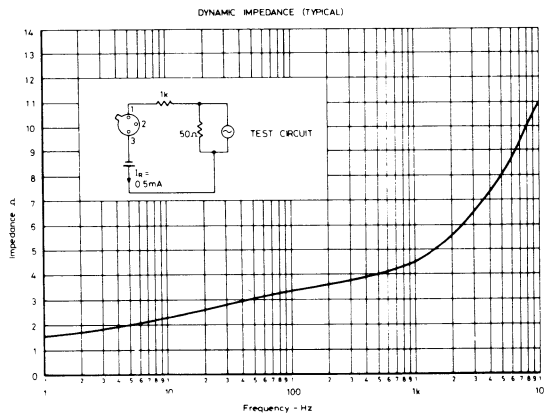
$$R_D = \frac{\text{CHANGE IN } V_O \text{ OVER SPECIFIED CURRENT RANGE}}{\Delta I_{REF}}$$

$\Delta I_{REF} = 5 - 0.5 = 4.5\text{mA}$ (typically)

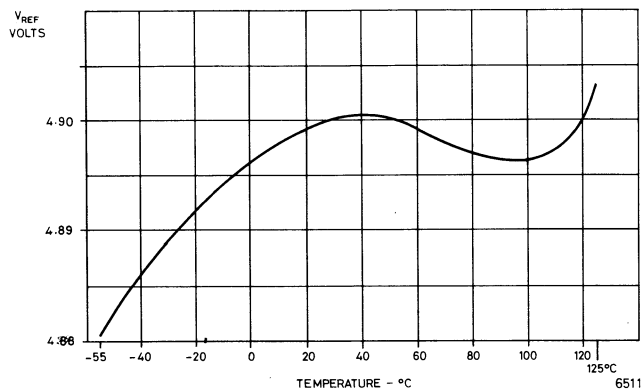
e) LINE REGULATION (ΔV_{OL})
The ratio of the change in output voltage to the change in input voltage producing it.

$$\Delta V_{OL} = \frac{R_D \times 100}{V_o \times R_s} \text{ \% /V}$$

R_S = Source resistance.



TYPICAL TEMPERATURE CHARACTERISTIC

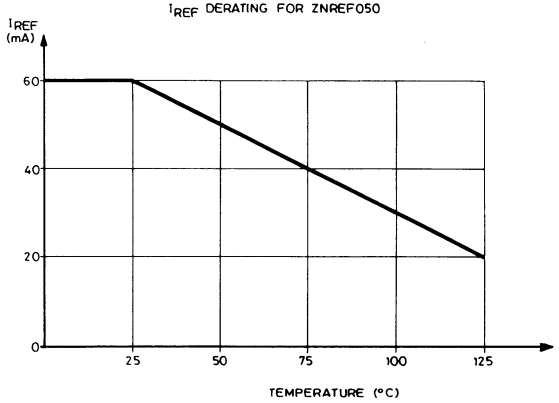


ZNREF 050

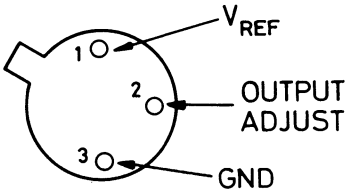
ORDERING INFORMATION

DEVICE	TOL %	(max.)T.C. (ppm/°C)	Temp. Range
ZNREF A1	1	50	−55°C to + 125°C
ZNREF A2	2		
ZNREF A3	3	80	
ZNREF C1	1	50	0°C to 70°C
ZNREF C2	2		
ZNREF C3	3	60	

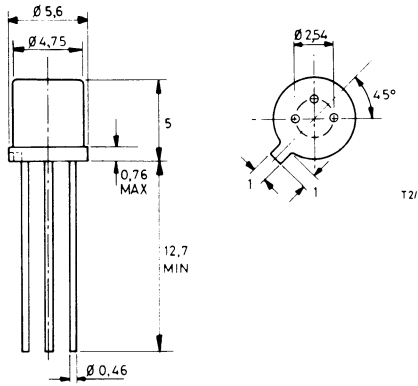
I_{REF} DERATING FOR ZNREF050



CONNECTION DIAGRAM
TO-18 Metal Can (Bottom View)



PACKAGE OUTLINE
(TO-18) Dimensions in mm.



BS.3934 SO-12A
JEDEC TO-18

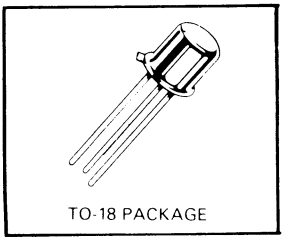
FERRANTI semiconductors

ZNREF 062

6.2 Volt Low Power Precision Reference Source

FEATURES

- Trimmable output
- Excellent Temperature Stability
- Low output noise figure
- Low Dynamic Impedance
- Available in two temperature ranges
- 1%, 2% and 3% initial voltage tolerance versions available
- No external stabilising capacitor required



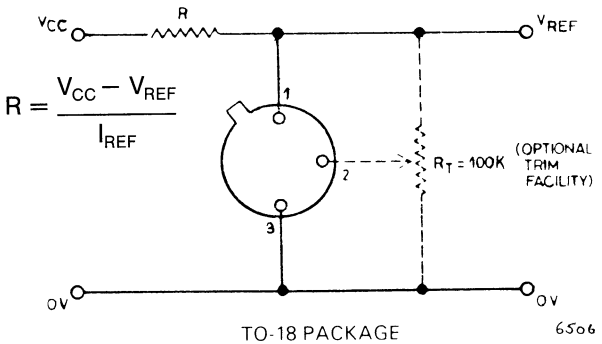
DESCRIPTION

The ZNREF062 is a monolithic integrated circuit providing a precise, stable reference source of 6.2 volts in a three pin TO-18 metal can transistor package.

The ZNREF062 is unconditionally stable under all load conditions without the need for an external shaping capacitor.

The use of the third pin is optional and enables V_{REF} to be trimmed by $\pm 5\%$. This is useful for taking out system errors or setting V_{REF} to specific values, e.g. 6.000 volts for a standard calibration source.

TRIM CIRCUIT



N.B. Case is internally connected to 0V

ZNREF 062

ABSOLUTE MAXIMUM RATINGS

Reference Current 50mA*
Power Dissipation 300mW
Operating Temperature Range .. .. See below
Storage Temperature Range .. .. −55 to +175°C
Soldering temperature for a maximum time of 10s
within $^1/_{16}$" of the seating plane .. .. 300°C
within $^1/_{32}$" of the seating plane .. .. 265°C

*Above 25°C this figure should be linearly derated to 20mA at +110°C.

TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial Voltage Tolerance %	Grade A B −55 to 110°C		Grade C 0 to 70°C		Units
			Typ.	Max.	Typ.	Max.	
Output voltage change over relevant temperature range (See Note (a))	ΔV_{REF}	1 & 2	26	40	6.5	22	mV
		3	50	71	11	26	
Output voltage temperature coefficient (See Note (b))	TCV_{REF}	1 & 2	25	40	15	50	ppm/°C
		3	50	70	25	60	

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C and Pin 2 o/c unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage	V_{REF}					
1% Tolerance (AB1 C1)		6.11	6.17	6.23	V	I_{REF} = 500μA
2% Tolerance (AB2 C2)		6.05	6.17	6.29		
3% Tolerance (AB3 C3)		5.98	6.17	6.36		
Output voltage adjustment range	ΔV_{TRIM}	–	±5	–	%	R_T = 100kΩ
Change in TCV_{REF} with output adjustment	$TC\Delta V_{TRIM}$	–	0.8	–	ppm/°C/%	
Operating current range	I_{REF}	0.15	–	50	mA	See Note (c)
Turn-on time	t_{on}	–	40	–	μS	R_L = 1kΩ
Turn-off time	t_{off}	–	0.3	–		
Output voltage noise (over the range 0.1Hz to 10Hz)	e_{np-p}	–	50	–	μV	Peak to peak measurement
Slope resistance	R_{REF}	–	2	3	Ω	I_{REF} 0.5mA to 5mA See Note (d)

NOTES

(a) OUTPUT CHANGE WITH TEMPERATURE (ΔV_{OT}) the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{OT} = V_{max} - V_{min}$$

(b) OUTPUT TEMPERATURE COEFFICIENT (TCV_o)
The ratio of the output voltage change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_o = \frac{\Delta V_{OT} \times 10^6}{V_O \times \Delta T} \text{ ppm/°C} \qquad \Delta T = \text{Full temperature change.}$$

(c) OPERATING CURRENT (I_{REF})
Maximum operating current must be derated as indicated in Maximum Ratings.

(d) DYNAMIC IMPEDANCE (R_D)
The dynamic impedance is defined as

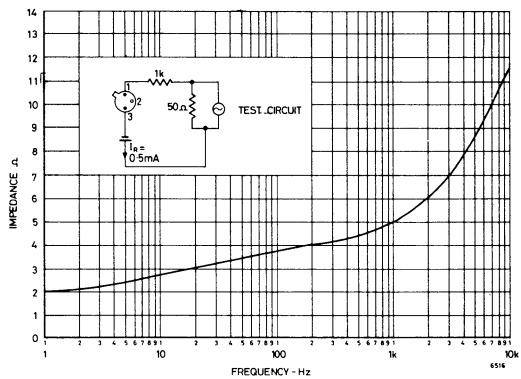
$$R_D = \frac{\text{CHANGE IN } V_O \text{ OVER SPECIFIED CURRENT RANGE}}{\Delta I_{REF}}$$

$$\Delta I_{REF} = 5 - 0.5 = 4.5\text{mA (typically)}$$

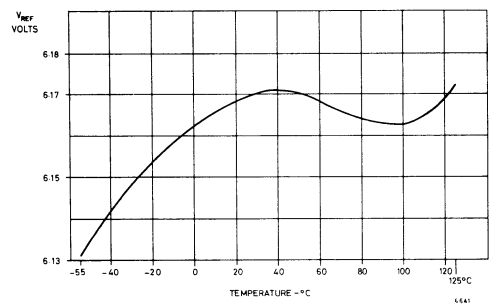
(e) LINE REGULATION (ΔV_{OL})
The ratio of the change in output voltage to the change in input voltage producing it.

$$\Delta V_{OL} = \frac{R_D \times 100}{V_O \times R_S} \%/V \qquad R_S = \text{Source resistance}$$

DYNAMIC IMPEDANCE (TYPICAL)



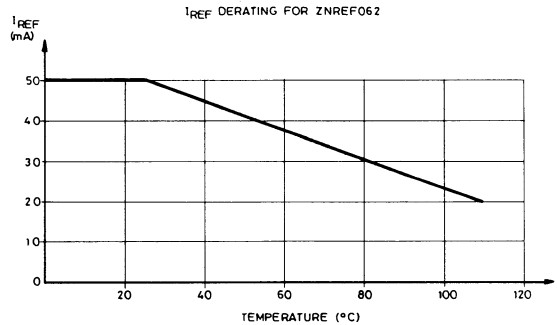
TYPICAL TEMPERATURE CHARACTERISTIC



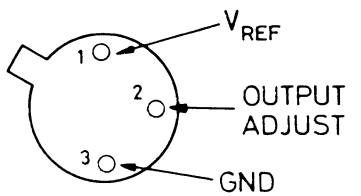
ZNREF 062

ORDERING INFORMATION

DEVICE	TOLERANCE (%)	T.C. (Max) – ppm/°C	Temperature Range
ZNREF062 A 1	1	40	– 55°C to + 110°C
ZNREF062 A 2	2		
ZNREF062 A 3	3	70	
ZNREF062 C1	1	50	0°C to + 70°C
ZNREF062 C2	2		
ZNREF062 C3	3	60	

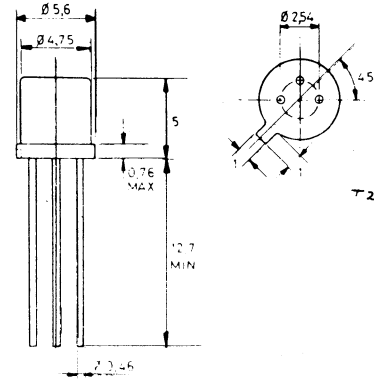


CONNECTION DIAGRAM
TO-18 Metal Can (Bottom View)



6509

PACKAGE OUTLINE
(TO-18) Dimensions in millimetres



FERRANTI semiconductors

ZNREF100

10 Volt Low Power Precision Reference Source

FEATURES

- Trimmable output
- Excellent Temperature Stability
- Low output noise figure
- Low Dynamic Impedance
- Available in two temperature ranges
- 1, 2 and 3% initial voltage tolerance versions available
- No external stabilising capacitor required in most cases

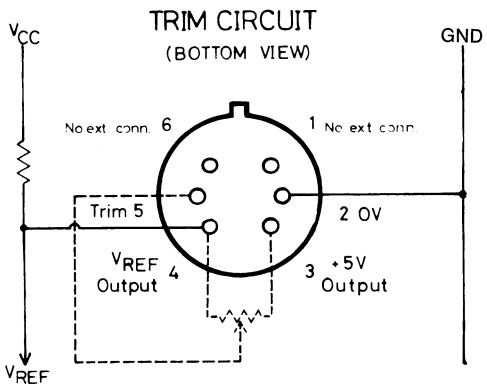
TO-39 (6 Lead) PACKAGE

DESCRIPTION

The ZNREF100 is a monolithic integrated circuit providing a precise, stable reference source of 10 volts in a six pin TO-39 metal can transistor package.
The ZNREF100 is unconditionally stable under all load conditions without the need for an external shaping capacitor.

The use of the third pin is optional and enables V_{REF} to be trimmed by ±2.5%. This is useful for taking out system errors or setting V_{REF} to specific values.

$$R = \frac{V_{CC} - V_{REF}}{I_{REF}}$$



Optional Trim Facility

ZNREF 100

ABSOLUTE MAXIMUM RATINGS

Reference Current	50mA*
Power Dissipation	500mW
Operating Temperature Range	See below
Storage Temperature Range	−55 to +175°C
Soldering temperature for a maximum time of 10s	
within $^1/_{16}$" of the seating plane	300°C
within $^1/_{32}$" of the seating plane	265°C

*Above 25°C this figure should be linearly derated to 16mA at +125°C.

TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Initial Voltage Tolerance %	Grade A −55 to 125°C		Grade C 0 to 70°C		Units
			Typ.	Max.	Typ.	Max.	
Output voltage change over relevant temperature range (See Note (a))	ΔV_{REF}	1 & 2	64	90	10.8	34.4	mV
		3	102	144	13	42	
Output voltage temperature coefficient (See Note (b))	TCV_{REF}	1 & 2	35	50	15	50	ppm/°C
		3	57	80	18	60	

ELECTRICAL CHARACTERISTICS (at T_{amb} = 25°C and Pins 3 & 5 o/c unless otherwise noted).

Parameter	Symbol	Min.	Typ.	Max.	Units	Comments
Output voltage	V_{REF}					
1% Tolerance (A1 C1)		9.70	9.80	9.90		
2% Tolerance (A2 C2)		9.60	9.80	10.00	V	I_{REF} = 500μA
3% Tolerance (A3 C3)		9.51	9.80	10.09		
Output voltage adjustment range	ΔV_{TRIM}	–	±2.5	–	%	R_T = 100kΩ
Change in TCV_{REF} with output adjustment	$TC\Delta V_{TRIM}$	–	0.8	–	ppm/°C/%	
Operating current range	I_{REF}	0.15	–	50	mA	See Note (c)
Turn-on time	t_{on}	–	40	–	μS	R_L = 1kΩ
Turn-off time	t_{off}	–	0.3	–		
Output voltage noise (over the range 0.1Hz to 10Hz)	e_{np-p}	–	50	–	μV	Peak to peak measurement
Slope resistance	R_{REF}	–	3	4	Ω	I_{REF} 0.5mA to 5mA See Note (d)

NOTES

a) OUTPUT CHANGE WITH TEMPERATURE(ΔV_{OT}) the absolute difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$V_{OT} = V_{max} - V_{min}$$

b) OUTPUT TEMPERATURE COEFFICIENT (TCVo)
The ratio of the output voltage change with temperature to the specified temperature range expressed in p.p.m/°C.

$$TCV_o = \frac{\Delta V_{OT} \times 10^6}{V_O \times \Delta T} \text{ ppm/°C}$$

ΔT = Full temperature change.

c) OPERATING CURRENT (I_{REF})
Maximum operating current must be derated as indicated in Maximum Ratings.

d) DYNAMIC IMPEDANCE (R_D)
The dynamic impedance is defined as

$$R_D = \frac{\text{CHANGE IN } V_O \text{ OVER SPECIFIED CURRENT RANGE}}{\Delta I_{REF}}$$

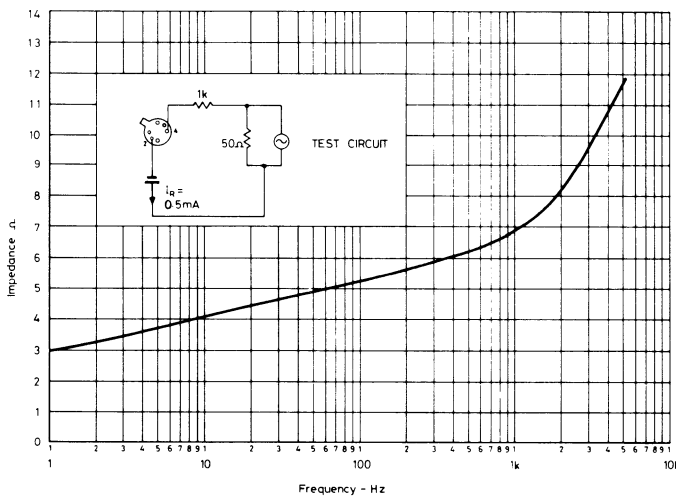
$\Delta I_{REF} = 5 - 0.5 = 4.5\text{mA}$ (typically)

e) LINE REGULATION (ΔV_{OL})
The ratio of the change in output voltage to the change in input voltage producing it.

$$\Delta V_{OL} = \frac{R_D \times 100}{V_o \times R_s} \text{ \% /V}$$

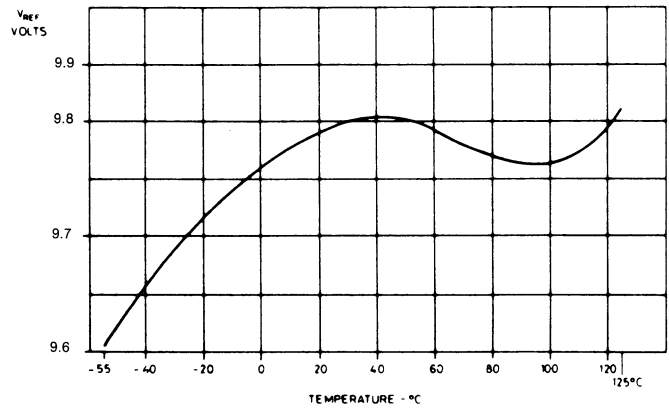
R_S = Source resistance.

DYNAMIC IMPEDANCE (TYPICAL)

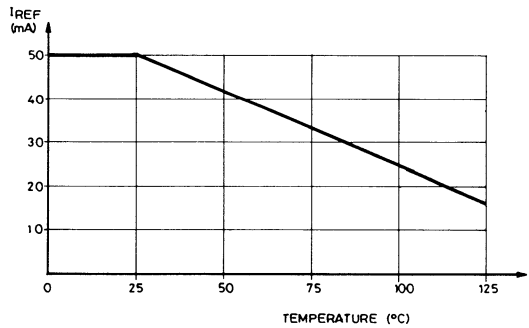


ZNREF 100

TYPICAL TEMPERATURE CHARACTERISTIC



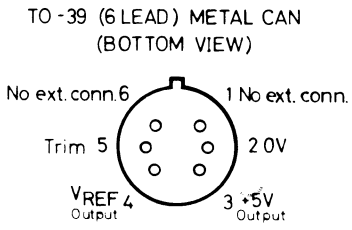
I_{REF} DERATING FOR ZNREF100



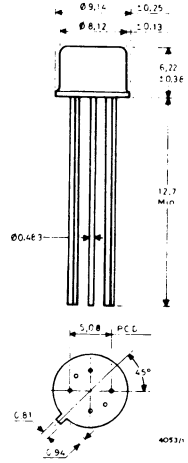
ORDERING INFORMATION

DEVICE	TOL %	(max.)T.C. (ppm/°C)	Temp. Range
ZNREF100 A1	1	50	−55°C to + 125°C
ZNREF 100 A2	2		
ZNREF100 A3	3	80	
ZNREF 100 C1	1	50	0°C to 70°C
ZNREF100 C2	2		
ZNREF**100** C3	3	60	

CONNECTION DIAGRAM
TO-39 Metal Can (Bottom View)



PACKAGE OUTLINE
(TO-39) Dimensions in mm.



TO-39 (6 Lead) PACKAGE

4. Telecom Circuits

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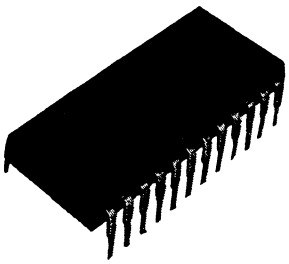
FERRANTI semiconductors

ZNPCM1

Single Channel Codec

FEATURES

- Converts a delta-sigma modulated digital pulse stream into compressed 'A' law pcm and vice-versa.
- Enables realisation of a single channel codec circuit with minimum component usage.
- Pin selectable input/output interface providing either single channel operation at 64K bit/s (2,048 kHz external clock) or up to 2,048K bit/s (2,048 kHz external clock) for multi-channel burst format.
- Encoder and decoder can be clocked asynchronously (useful for pcm multiplex applications).
- Optional alternate digit inversion.
- Electrically and pin compatible with AY-3-9900
- Fully TTL compatible.
- Requires only a single 5V supply.



24-lead D.I.L.

DESCRIPTION

The ZNPCM1 integrated circuit is the result of a joint development programme between the British Post Office and Ferranti Electronics Limited. Designed for use in single channel codec systems the device accepts a delta-sigma modulated pulse stream at 2,048K bit/s (2,048 kHz external clock) and converts it into 8K sample/s compressed 'A' law pcm. In the decode direction the device performs the reverse function. A flexible serial pcm input/output interface is provided allowing operation in a single channel mode at 64K bit/s or at up to 2,048K bit/s (2,048 kHz external clock) for a multi-channel burst format. Digit delay control is provided to compensate for transmission delays. Optional alternate digit inversion is provided and the encoder and decoder can be clocked asynchronously if required for use in pcm multiplex applications.

Designed for use with a 2,048 kHz system clock, when operated with the required delta-sigma modulator and demodulator (see application report 'a single channel codec') The device performance complies with B.P.O. specification RC5549B and CCITT recommendations G711/G712 (1972).

The ZNPCM1 is guaranteed to operate up to 2,048 kHz and will typically operate up to 4 MHz. Operation is from a single 5V power supply with a typical power dissipation of 400 mW. All inputs and outputs are TTL compatible. Available in either a 24-lead ceramic (ZNPCM1J) or moulded (ZNPCM1CE) dual in-line package, the device is designed to operate over the temperature range 0°C to +70°C.

ZNPCM1

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .. .. +7 Volts
Input Voltage, V_{IN} .. .. +5.5 Volts
Operating Temperature Range .. 0°C to +70°C
Storage Temperature Range .. .. –65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage, V_{CC}	4.75	5.0	5.25	V
High-level Output Current, I_{OH}	—	—	–400	μA
Low-level Output Current, I_{OL}	—	—	4	mA
Operating Temperature Range, T_{amb}	0	—	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating temperature range).

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage		2.5	—	—	V
V_{IL}	Low level input voltage		—	—	0.8	V
V_{OH}	High level output voltage	V_{CC} = Min., I_{OH} = Max.	2.4	3.5	—	V
V_{OL}	Low level output voltage	V_{CC} = Min., I_{OL} = Max.	—	—	0.4	V
I_{IH}	High level input current	V_{CC} = Max., V_{IH} = Min.	—	0.2	0.4	mA
I_{IL}	Low level input current	V_{CC} = Max., V_{IL} = Max.	—	–1	–10	μA
I_{CC}	Supply current	V_{CC} = Max.	—	80	110	mA
t_{vw}	Encoder timing vector pulse width		—	488	—	ns
t_{vv}	Encoding timing vector pulse width with edge variation		—	—	100	ns
t_{ww}	Decoder timing waveform pulse width		10	15.6	—	μs
f_{max}	Operating frequency		2.048	4	—	MHz
t_r & t_f	Rise and fall times	0.4V to 3V Transition	5	--	40	ns
t_{pw}	Pulse width	Between 1.5V levels	200	—	—	ns
C_I	Input capacitance		—	—	10	pF

PIN CONFIGURATIONS

Pin	Notation	Comments
1	0V	
2	MS	MODE SELECT (Note 1) Logic 0 = External pcm I/O interface timing Logic 1 = Internal pcm I/O interface timing
3	DS1	DECODER SELECT 1 and 2 (Note 2)
4	DS2	A two bit binary word selects required digit delay between encoder and decoder. DS1 DS2 Digit Delay 0 0 0 0 1 1 1 0 2 1 1 3
5	ADI	ALTERNATE DIGIT INVERSION Logic 0 = No. ADI Logic 1 = ADI
6	N.C.	NO CONNECTION
7	0V	
8	V_{CC}	
9	DSMO	DELTA-SIGMA MODULATED OUTPUT SIGNAL
10	SGN	SIGN BIT OUTPUT Sign bit from the encoder, used to operate on the delta-sigma modulator to reduce d.c. offset effects.
11	DSMI	DELTA-SIGMA MODULATED INPUT
12	SRF	SPECTRAL REDISTRIBUTION FUNCTION Output signal used to operate on the delta-sigma modulator to reduce low frequency quantisation noise.
13	PCMO	PCM OUTPUT
14	SGBI	SIGNALLING BIT INPUT Facility for adding signalling bit(s) to the output pcm stream.
15	ETV	ENCODER TIMING VECTOR A pulse defining the beginning of each frame used to maintain encoder timing.
16	PCMI	PCM INPUT
17	SGBO	SIGNALLING BIT OUTPUT Serial output for extracting signalling bit(s) from the incoming pcm stream.

PIN CONFIGURATIONS *(continued)*

Pin	Notation	Comments
18	DTW	DECODER TIMING WAVEFORM A pulse used to indicate to the decoder when the input pcm stream is in the input register (required only when external shift clocks are used).
19	SCE	ENCODER SHIFT CLOCK Used to control the output of serial pcm data from the encoder (when MS is low).
20	CLKD	DECODER MAIN CLOCK
21	CLKE	ENCODER MAIN CLOCK
22	SCD	DECODER SHIFT CLOCK Used to control the input of the serial pcm data to the decoder (when MS is low).
23	N.C.	NO CONNECTION
24	I.C.	INTERNAL CONNECTION Make no external connection to this pin.

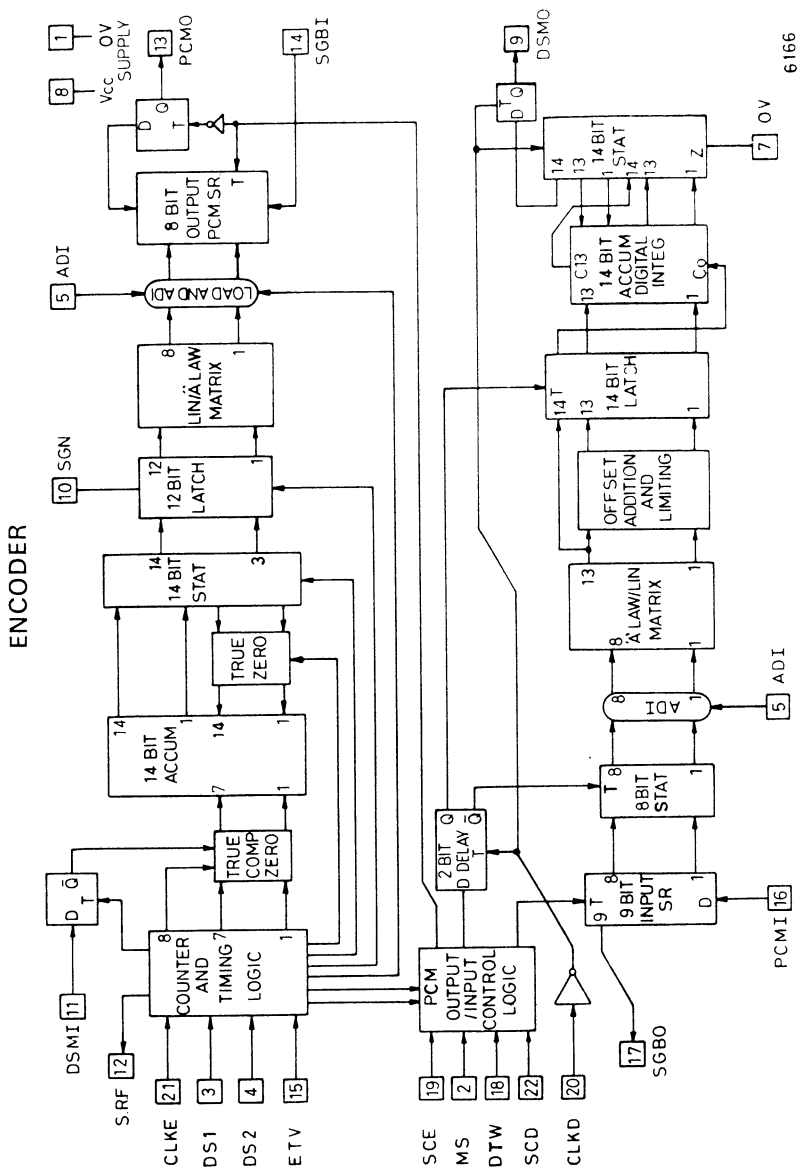
Notes:

1. With MS low (logic 0) serial PCM transmission is under the control of an externally generated shift clock SCE which can vary from 64 kHz to 2,048 kHz. The timing of this input function allows the insertion of a number of signalling bits into the PCM stream via the SGB1 input. In the high (logic 1) state the 8 bit PCM codeword will be transmitted at a rate of 64K bit/sec and each codeword will occupy the full 125 μs frame period with the leading edge of the first bit occurring at a time defined by the ETV pulse.

2. Delays through the transmission network, normally under the control of transmission switches, may cause the decoder input pulse stream to be delayed in time by a number of digits from the original transmitted pulse. To compensate for this delay two control inputs, DS1 and DS2, are provided. Consequently when MS is in the high state discrete digit delays of 0 to 3 periods may be selected resulting in a controlled shift of decoder timing in order to re-align Bit 1 in its correct position in the input register.

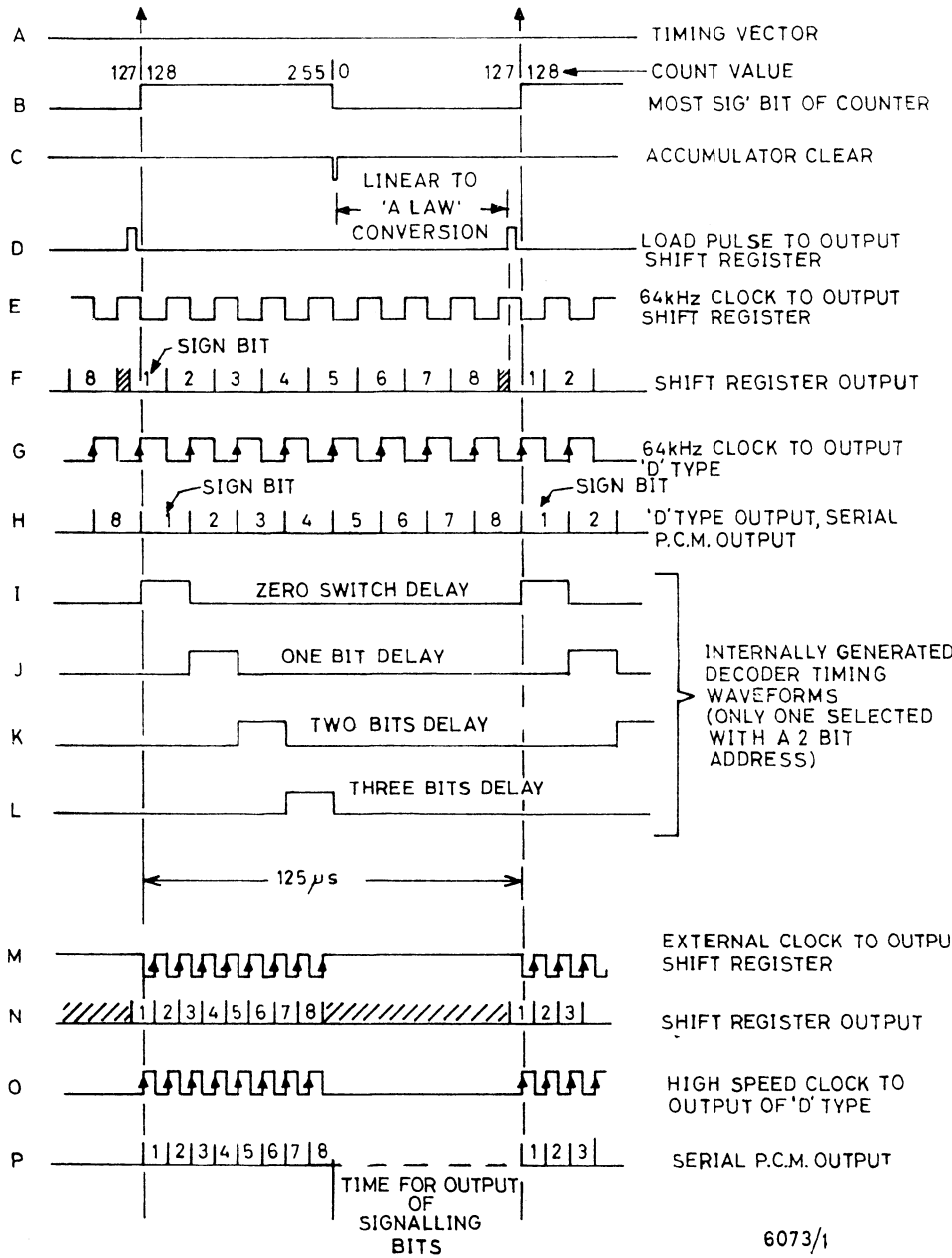
   When using an externally generated clock (i.e. MS in low state) an input shift clock (SCD) and timing waveform (DTW) are required to ensure that Bit 1 of the input codeword occupies its correct position in the input shift register.

FUNCTIONAL DIAGRAM



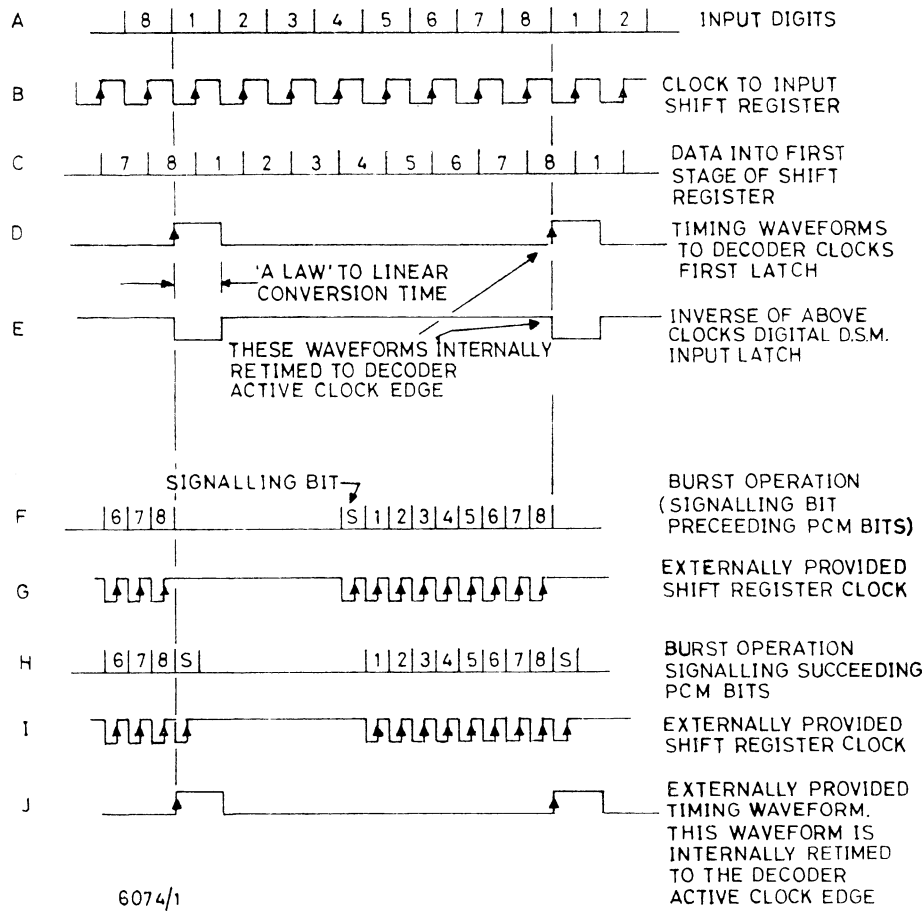
ZNPCM1

TIMING DIAGRAM
ENCODER



TIMING DIAGRAM

DECODER



ZNPCM1

APPLICATIONS INFORMATION

(a) A Single Channel Codec

Fig. 1 shows a block diagram of a single channel Codec using the ZNPCM1. The circuit accepts a band limited analogue input signal (300 – 3,400 kHz) and converts it to one bit/sample delta sigma code format at a high sampling rate. The dsm bit stream is then converted by the ZNPCM1 into 8-bit compressed pulse code modulation (pcm) code words at the standard rate of 8K samples/sec, which is then converted into serial format for transmission serially at 64K bit/sec. External timing signals can be used to increase the transmission bit rate to 2,048K bit/sec. to allow for multiplexing in a burst format (see application b).

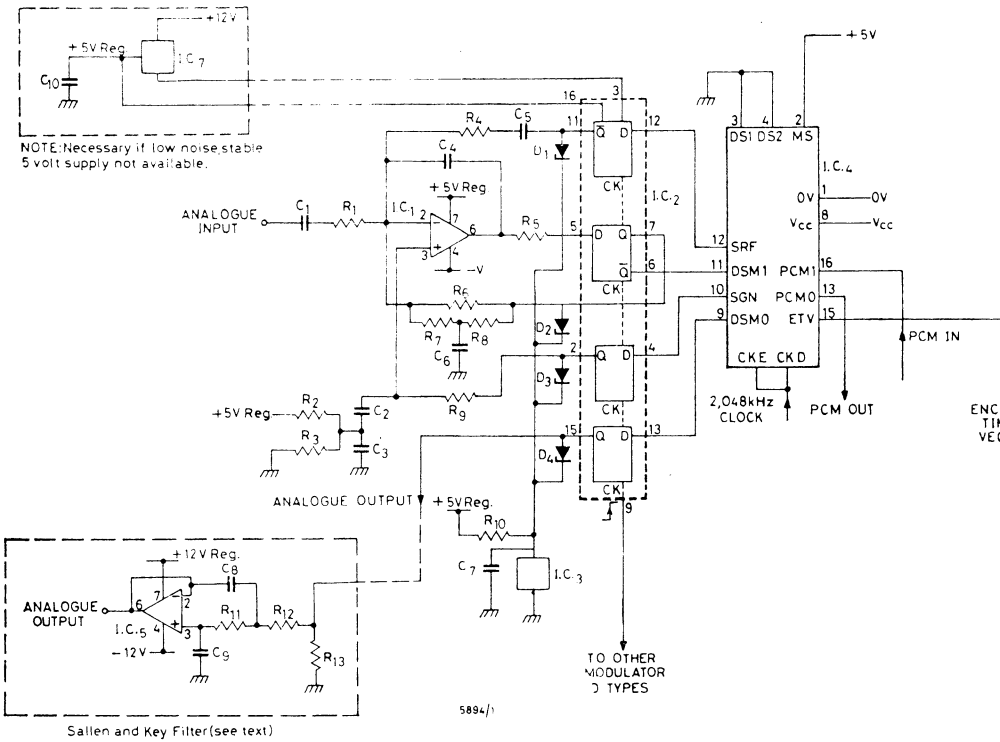


Fig. 1.

The pcm input interface will accept either a 64K bit/sec. bit stream or, by the application of external timing signals, a bit rate of 2,048K bit/sec. in burst format. This is then converted by the ZNPCM1 into a dsm bit stream at 2,048K bit/sec. The dsm demodulator accepts this bit stream and produces one of two precisely defined analogue levels per single bit sample. The analogue waveform can then be recovered via a low pass filter, cutting off just above the highest signal frequency to be recovered (3.4 kHz).

Output voltages of the dsm circuit are stabilised by supplying the quad D-type from a 5 volt regulator, which is always associated with the Codec, and clamping the high state output voltages to a 2.45V reference by the use of Schottky diodes. These also help to match the voltages influencing the d.c. alignment conditions and minimise the effects of power supply variations and noise. Resistor ratio stability is obtained, along with a small modulator/demodulator physical size by implementing the resistors and small capacitors as an in-line hybrid. More details of the operation of the dsm circuit are outlined in the Ferranti brochure 'A Single Channel Codec'.

An interesting development, again in co-operation with the British Post Office, is the integrated circuit dsm solution now approaching completion. This will reduce the circuitry surrounding the ZNPCM1 to a single I.C. and seven capacitors, the latter almost certainly to be made available as a single in-line hybrid.

The Codec performance related to CCITT criteria is outlined in Fig. 2.

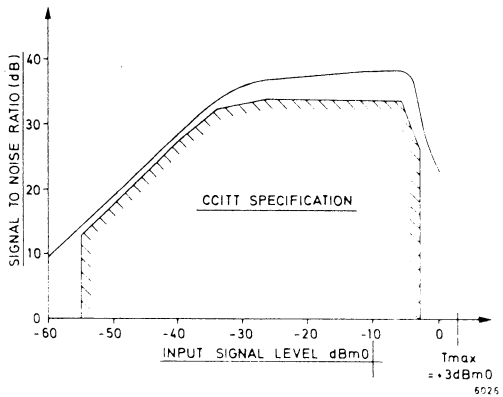


Fig. 2.

(b) A 30 Channel PCM Codec Solution

Traditionally the code conversion process on branch-to-main telephone exchange systems has been performed using multiplexed codecs. Historically the reason for this has been the codec specification where the signal-to-noise and gain-linearity constraints imposed on the systems have resulted in the use of expensive hybrid codecs. It might seem immediately obvious that the use of single channel codecs offers a more attractive solution, however a comparison of one of the major performance criteria is first of all necessary, that of power dissipation. Indeed, an initial comparison using the conventional 30 Channel PCM system shows the single channel codec approach to disadvantage. However, a more detailed analysis, using the single channel codecs in a power switching mode, shows this technique to be compatible with time shared codecs. This is described in section (d).

Let us first of all consider the system approach for using the single channel codecs in a 30 Channle PCM system by looking at Fig. 3.

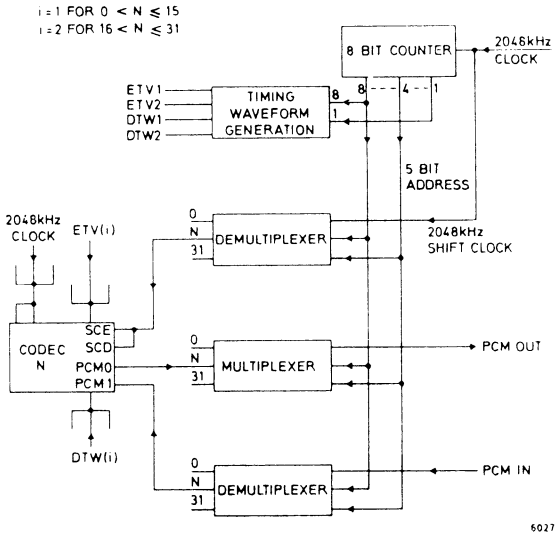


Fig. 3.

Fig. 3 shows how a 32 time slot (Note: A 30 Channel system has in fact, 32 time slots, the two additional ones being for signalling notation and synchronisation), 2,048K bit/sec. multiplex can be formed and decoded using 30 single channel codecs, when the two directions of transmission operate synchronously. Only the Nth codec is shown, connected to the 'Nth' port of the 32 port multiplexer and demultiplexers. When the 5-bit address equals N the 2,048 kHz shift clock is routed through the 'Nth' codec for eight clock pulses as shown in Fig. 4(a). The shift-in and shift-out clock terminals of the codec are commoned together. Since the shift-out terminal uses a negative active clock edge and the shift-in terminal uses a positive active clock edge the pcm digits for the two directions may be in exact time alignment. This is compatible with using the same 5-bit address for the multiplexer and the other demultiplexer.

The Encoder Timing Vector (ETV) and the Decoder Timing Waveform (DTW) may be derived from a counter driven by the 2,048 kHz clock and commoned across a number of codecs. For a 32 time slot multiplex, two sets of ETV's and DTW's should be generated with a half frame displacement as shown in Figs. 4(b) and 4(c). The first pair will supply ports 0 to 15 and the second pair ports 16 to 31, and consequently allowing the shift activity to be kept well clear of the timing waveforms for a given codec.

For a conventional 32 time slot codec ports 0 and 16 correspond to the synchronisation and signalling channels respectively.

Fig. 5 shows a similar arrangement for generating and decoding a 32 time slot multiplex when the two directions of transmission operate asynchronously. The two directions are operated quite independently but using similar principals to those previously discussed. It should again be noted that two sets of ETV's and DTW's should be used.

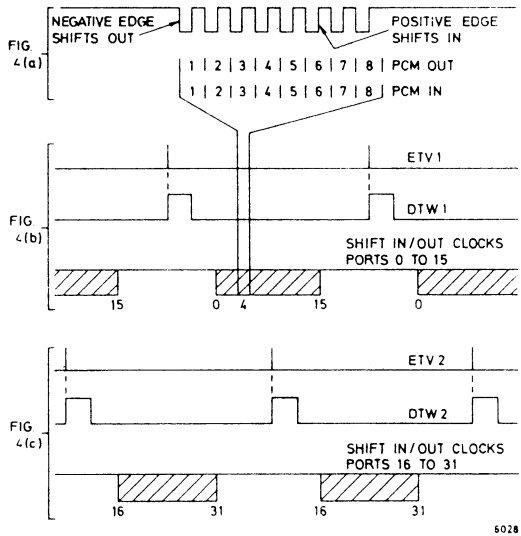
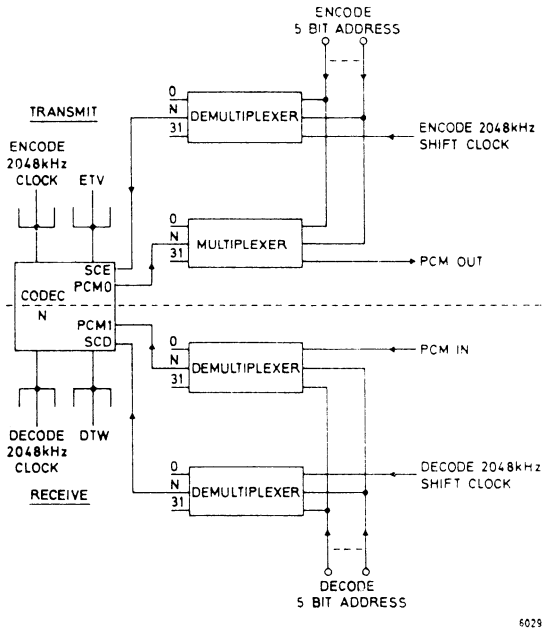

NEGATIVE EDGE
SHIFTS OUT
POSITIVE EDGE
SHIFTS IN
FIG 4(a)
1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | PCM OUT
1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | PCM IN
ETV1
DTW1
FIG 4(b)
SHIFT IN/OUT CLOCKS
PORTS 0 TO 15
15
0 4
15
0
ETV2
DTW2
FIG 4(c)
SHIFT IN/OUT CLOCKS
PORTS 16 TO 31
16
31
16
31
6028

Fig. 4.


ENCODE
5 BIT ADDRESS
TRANSMIT
0
N
31
DEMULTIPLEXER
ENCODE 2048kHz
SHIFT CLOCK
ENCODE
2048kHz
CLOCK
ETV
MULTIPLEXER
PCM OUT
SCE
PCM0
CODEC
N
PCM1
SCD
DEMULTIPLEXER
PCM IN
DECODE
2048kHz
CLOCK
DTW
RECEIVE
DEMULTIPLEXER
DECODE 2048kHz
SHIFT CLOCK
DECODE
5 BIT ADDRESS
6029

(c) Switching Applications

The ZNPCM1 can be used in a variety of ways to satisfy switching applications. One technique is to operate directly on the 2,048K bit/s digit stream produced by the circuit arrangement shown in Fig. 3, where each codec has a defined time slot in the bit stream. An alternative technique would be to derive the address applied to the multiplexer and demultiplexer from the contents of a random access memory (RAM) which defines the codec to be used in a given time slot, in an exchange of PCM codewords between the codec and an intermediate store. In this mode of use the codec interface is effectively used as a time switch store.

The circuit shown in Fig 5 can be used without an intermediate store where again the codec addresses are derived from RAM's. The encode address defines the 'source' and the decode address the 'sink' in a given time slot. The decode address may be delayed with respect to the encode address by an integer number of 2,048 kHz clock periods to take account of any small, fixed switching delay.

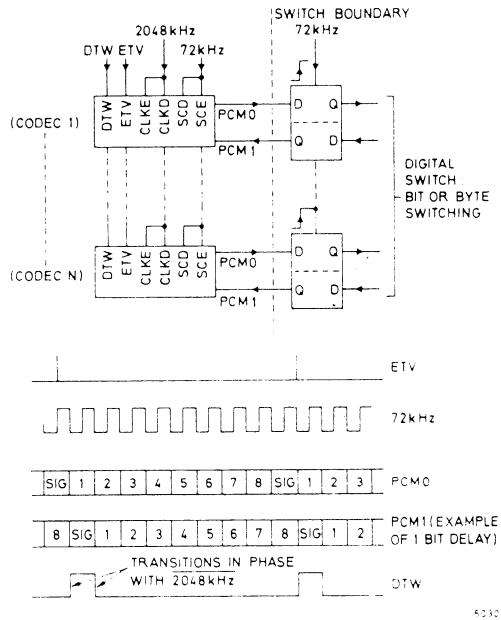


Fig. 6.

Fig. 6 shows an arrangement where the codecs input and output continuously, allowing 9-bits (8 PCM plus 1 signalling) to be exchanged in each 125 μs sample period. All the codecs may be supplied with common ETV, DTW, 2,048 kHz and 72 kHz waveforms. Each bit is retimed in the digital switch using a latch.

The digital switch may be operated using a bit switching arrangement, combined with the extraction and insertion of the signalling bits. Alternatively the bits may be reformatted into bytes and then byte switching performed. If the signalling is handled separately to the pcm codewords then a 64K bit/s rate can be used to and from the codec. This is compatible with using the codecs internal clock mode (MS = 1) in which case the only common timing waveforms required at the codec are the 2,048 kHz clock and the ETV.

(d) Power Switching

Comparisons have previously been made between shared and single channel codecs where these comparisions were reduced to one of power dissipation. Considerable power savings can be made by using the codecs in such a mode that they are only powered-up when required for use.

It is interesting to compare the power dissipation of an eight channel system using in one case eight ZNPCM1s in a power switching mode and, in the other case, one of the more popular time shared codecs which caters for eight channels. One single channel codec dissipates 600 mW and the time shared codec dissipates 1500 mW.

If the channel occupancy is p, then the average power dissipation per channel for the time shared codec is given by

$$W_{TS} = 1 - (1-p)^8 \frac{1500}{8} \text{ mW}$$

This assumes the time shared codec is only powered-up when any of the eight channels are required for use.

The average power dissipation per channel using the single channel codecs is simply given by,

$$W_{SC} = p.600 \text{ mW}$$

Fig. 7 shows a plot of power dissipation versus channel occupancy ; p for both approaches. The busy period average channel occupancies are likely to be in the range 0.2 to 0.15, clearly the lower end of the curves. Taking a figure of p = 0.06, for example, then the single channel codec dissipates only 36 mW per channel, approximately 50% less than the time shared codec. As the graph shows even for very busy exchanges given values for p of up to 0.3 shows the ZNPCM1 system to dissipate less power.

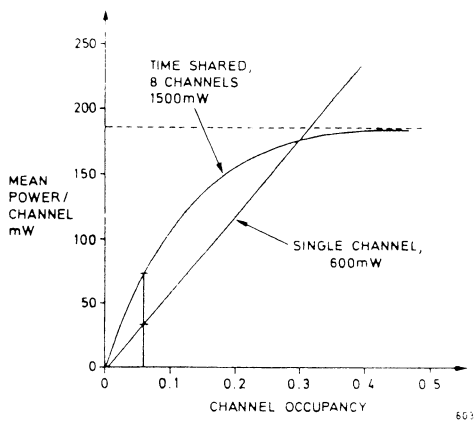
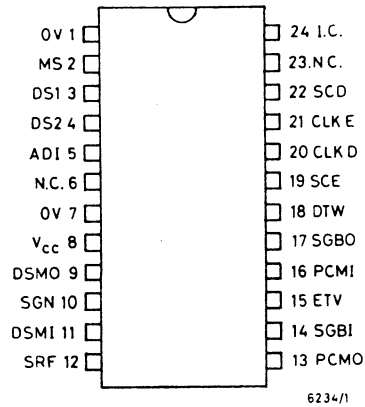


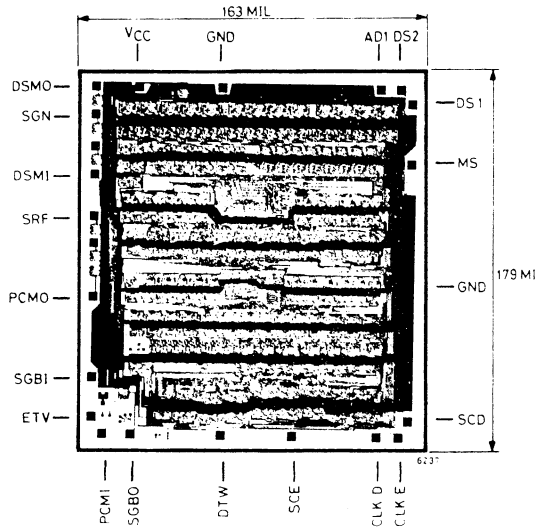
Fig. 7.

ZNPCM1

PIN CONNECTIONS



CHIP DIMENSIONS AND LYAOUT



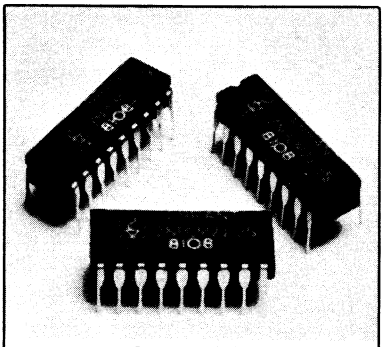
FERRANTI semiconductors

ZNPCM2

Delta Sigma Modulator/Demodulator I.C.

FEATURES

- Converts analogue input signal into delta sigma modulated (DSM) signal to be used as input for ZNPCM1 Codec I.C.
- Converts DSM signal produced by ZNPCM1 into level defined digital pulse stream for conversion to the analogue equivalent signal using low-pass filter techniques.
- High signal-to-noise ratio.
- Monolithic integrated circuit combining digital and analogue circuitry.
- Single 5V supply.
- 18-lead ceramic or modulated D.I.L. package.



18-LEAD D.I.L.

DESCRIPTION

The ZNPCM2 Delta Sigma Modulator/Demodulator (DSM) Integrated Circuit is designed for use in conjunction with the ZNPCM1 (manufactured by Ferranti Electronics Ltd.) or AY-3-9900 (manufactured by General Instruments Ltd.) Codec I.C's as the conversion unit in pulse code modulation communication systems. The ZNPCM2 modulator function converts analogue speech or data signals into a sampled signal having one bit per sample at a high sampling rate. The demodulator function produces an output signal having one of two well defined voltage levels in response to the signal bit per sample input signal. The original signal can then be recovered by low-pass filter techniques.

The ZNPCM2 provides excellent signal-to-noise ratio as a result of innovative circuit techniques developed at the British Post Office Research Centre. A rectangular input waveform designated as a spectral redistribution function (SRF) is provided and this modifies the quantisation noise spectrum, moving the noise components to higher frequencies. By varying the amplitude and phase of the SRF waveform, the net effects on the PCB outputs from the Codec system can be made to be ZERO if the SRF is sampled synchronously within the system. In addition a complex feedback network is utilised in the DSM circuit to provide increased feedback at low frequency which results in the relative attenuation of low frequency quantisation noise components below 32 kHz.

D.C. alignment to better than 0.01% at low signal ampitudes is achieved at the output by use of a feedback loop minimising both the DSM voltage offset and the digital code offset. This technique makes use of the fact that the PCM code words have a sign and magnitude format and the result eliminates the need for component trimming.

ZNPCM2

Designed using the same technology as the ZNPCM1 Codec I.C., the ZNPCM2 combines both linear and digital circuits on the same monolithic I.C. Packaged in an 18-lead ceramic (ZNPCM2J) or moulded D.I.L. (ZNPCM2E), the device is designed to operate over the the temperature range 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... +7 volts
Digital Input Voltage, $V_{IN(D)}$ ..... +5.5 volts
Analogue Input Voltage, $V_{IN(A)}$ ..... 4 volts pk-to-pk
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Nom.	Max.	Unit
Supply Voltage	4.75	5.0	5.25	V
High-level Output Current, I_{OH} (Digital Outputs)	—	—	−400	μA
Low-level Output Current, I_{OL} (Digital Outputs)	—	—	4	mA
Analogue Output Impedance, Z_{AO}	—	100	—	Ω
Operating Temperature Range, T_{amb}	0	—	70	°C

ELECTRICAL CHARACTERISTICS (over the recommended operating temperature range).

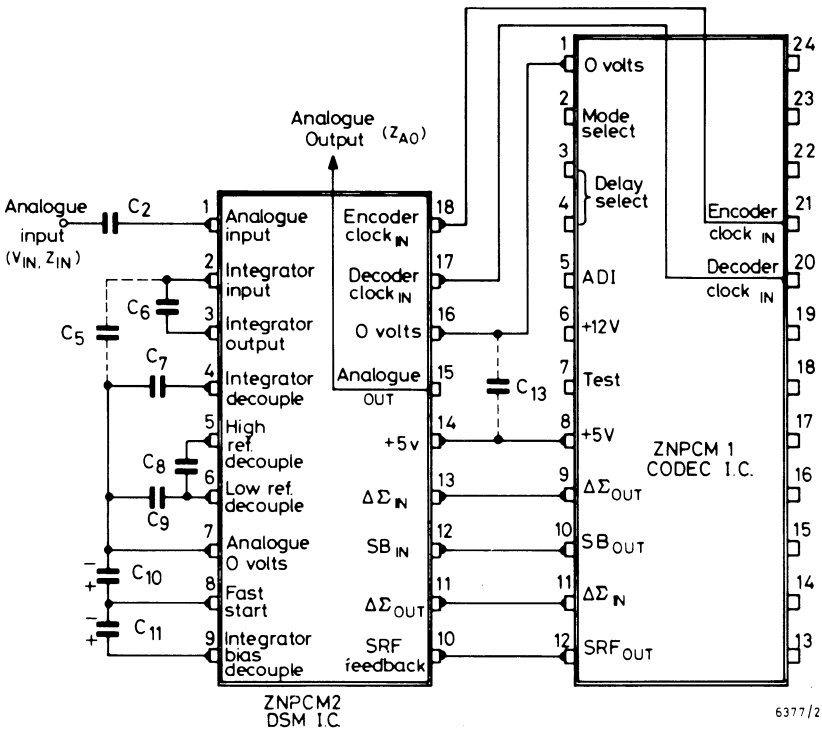
(a) Digital Inputs and Outputs.

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage		2.3	—	—	V
V_{IL}	Low-level input voltage		—	—	0.8	V
V_{OH}	High-level output voltage	V_{CC} = Min, I_{OH} = Max.	2.4	4	—	V
V_{OL}	Low-level output voltage	V_{CC} = Min, I_{OL} = Max.	—	—	0.4	V
I_{IH}	High-level input current	V_{CC} = Max, V_{IH} = Min.	—	0.2	0.4	mA
I_{IL}	Low-level input current	V_{CC} = Max, V_{IL} = Min.	—	—	10	μA
I_{CC}	Supply current	V_{CC} = Max.	—	24	—	mA
f	Operating frequency		—	2,048	—	kHz
t_r & t_f	Rise and fall time	0.4V − 3.0V transition	5	—	40	ns
t_{pd}	Propagation delay	Clock $\varnothing_E$ or $\varnothing_D$ to DSM output 2.5V level	—	40	60	ns
t_{pw}	Pulse width	Between 1.5V levels	200	—	—	ns

(b) Analogue Input and Output.

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Analogue Input Voltage for 0dBm0	Peak-to-peak	—	1.4	—	V
Z_{IN}	Analogue Input Impedance	Measured at 1kHz	80	100	—	kΩ
V_C	D.C. Voltage across C_{11}	V_{CC} = Max.	—	±3.0	±3.0	mV

DSM CODEC INTERFACE



NOTES

1 The external high frequency decoupling between pins 5, 6 and 7 should be of minimal impedance (i.e. in the range of 1 to 20MHz). Low loss capacitors connected via minimal conductor path lengths and inductances are required. Suitable capacitors are 0.22μF monoblock types. Total connection length and resistance including capacitor leads should be as follows:

Pins 5 to 6 <10mm and <0.1Ω
Pins 6 to 7 <16mm and <0.1Ω

2 Analogue ground pin 7 and digital ground pin 16 must be linked externally. Ideally, this should be their only connection; however, if it is essential that the two 0V systems are connected at a point remote from the ZNPCM2 then pin 16 should remain connected to the analogue ground only.

3 Performance of the ZNPCM1 and ZNPCM2 is layout dependent and an optimum layout is shown on page 6. Capacitor C_5 and C_{13} are optional but may improve performance in some instances.

PERFORMANCE

The codec combination of the ZNPCM1 and ZNPCM2 meets all the performance requirements of the C.C.I.T.T. recommendation G712 with good safety margins. Using a standard pcm multiplex tester and a spectrum analyser the following performance figures result:

(1) Idle Channel noise: −70dBm0p (See Fig. 1).
C.C.I.T.T. recommendation = −65dBm0p

(2) Signal-to-noise ratio and gain level linearity: Figs. 2(a) and 2(b) show the results using a 450 − 550kHz pseudo-random noise test.

(3) Intermodulation distortion: measured products are at least 10dB and on average 18dB better than C.C.I.T.T. recommendations.

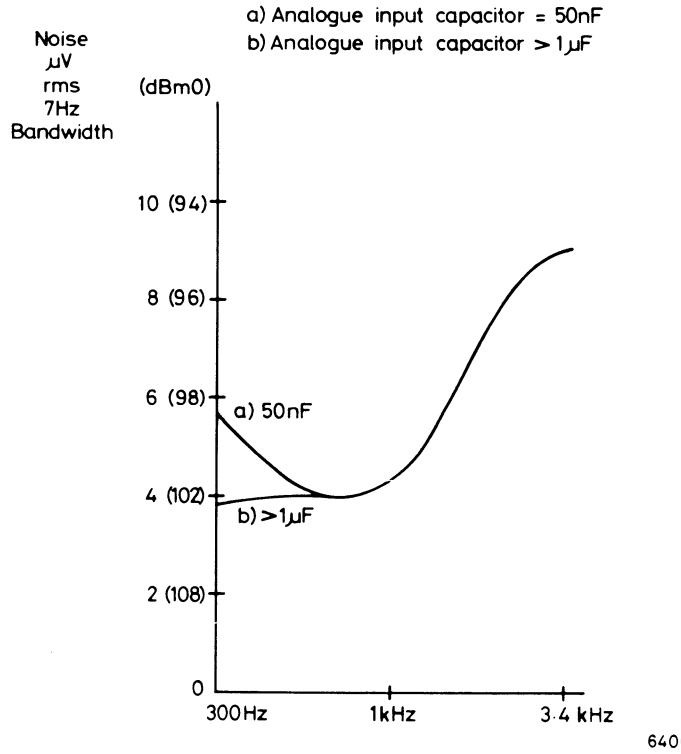


Fig. 1. Idle Channel Noise Spectrum

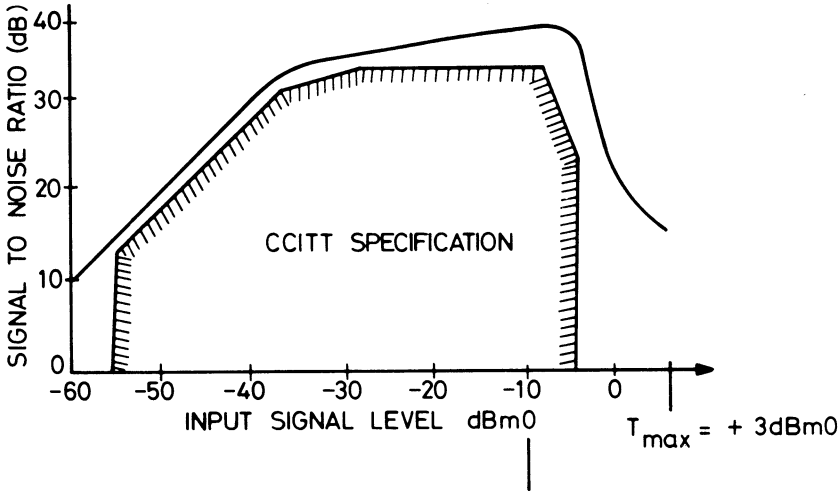


Fig. 2(a). Signal to Noise Ratio 'A Law'

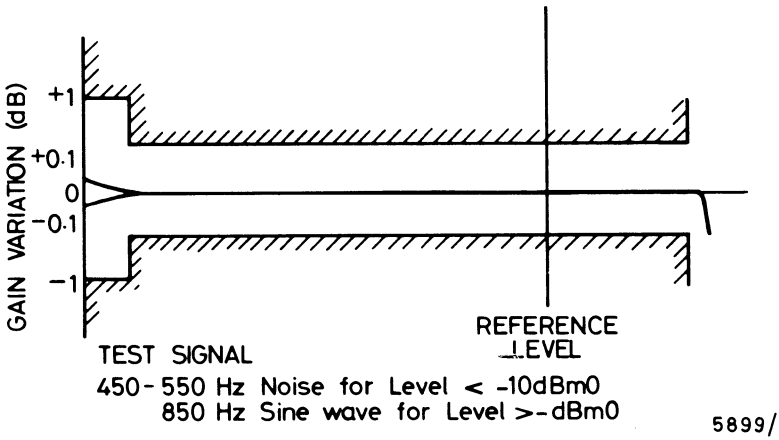
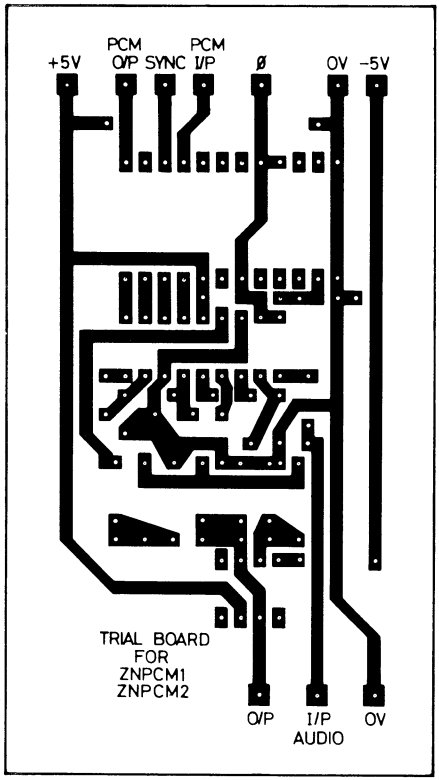


Fig. 2(b). Gain to Signal Level 'A Law'

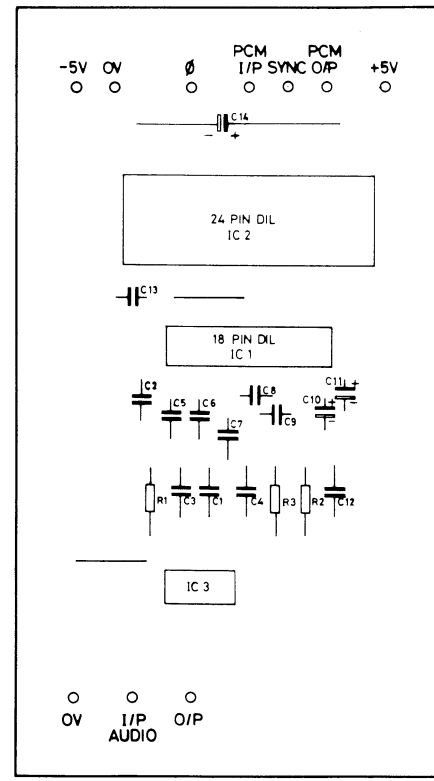
ZNPCM2

BASIC SYSTEM BOARD FOR ANALOGUE TO ANALOGUE PERFORMANCE EVALUATION



6410

P.C. BOARD



6411/2

COMPONENT LAYOUT

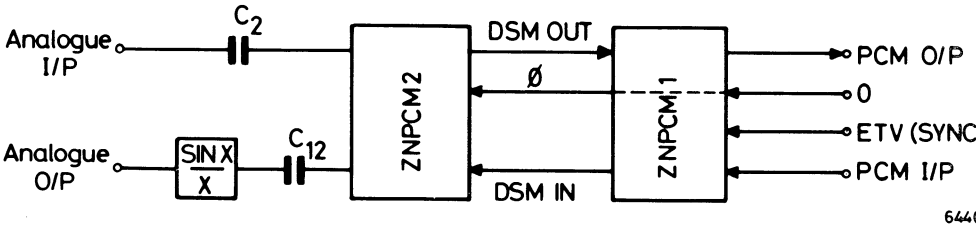
ACTUAL SIZE

ZNPCM1 & ZNPCM2 TRIAL UNIT

Component List (Tolerances ±20% unless otherwise shown)

IC1	ZNPCM2	C6	47pF ±5%
IC2	ZNPCM1	C7	4.7nF ±5%
IC3	741 or Amp	C8	0.22μF
R1	91k0 2%	C9	0.22μF
R2	91k0 2%	C10	10μF, 16V Tantalum Electrolytic
R3	100k0	C11	10μF, 16V Tantalum Electrolytic
C1	0.022μF	C12	47nF
C2	47nF	C13	0.1μF Ceramic
C3	100pF ±2%	C14	6.8μF, 10V Electrolytic
C4	1nF ±2%		
C5	10pF		

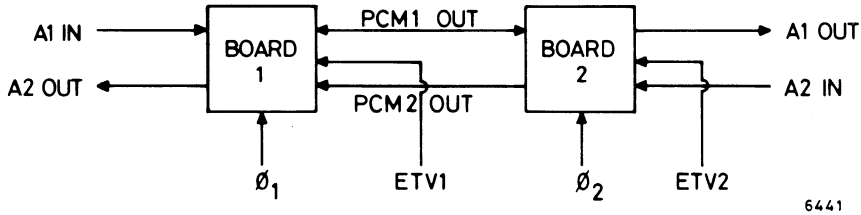
SCHEMATIC



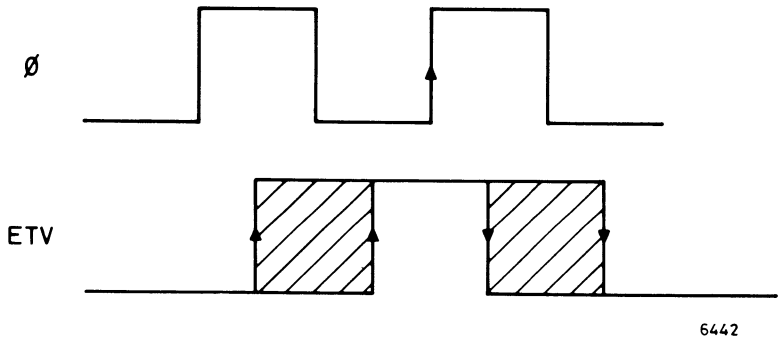
Single Channel Codec System Operating in Internal Mode (PCM at 64K bits/sec. without ADI).

Performance of the ZNPCM1/2 may be simply evaluated by linking PCM O/P to PCM I/P and comparing Analogue O/P to Analogue I/P. No ETV (Sync) signal is required for this.

For a more comprehensive evaluation two boards are required connected on the configuration shown,



$Ø_1$ and $Ø_2$ must be the same frequency and ETV1 and ETV2 can be common or up to 30 clock periods displaced.



WAVEFORMS SHOWING ETV TOLERANCE

ZNPCM2

PINNING CONFIGURATION

Pin 1 Analogue Input
Pin 2 Integrator Input
Pin 3 Integrator Output
Pin 4 Integrator Feedback Decouple
Pin 5 High-level Reference Voltage Decouple
Pin 6 Low-level Reference Voltage Decouple
Pin 7 Analogue 0V
Pin 8 Centre-level Reference Voltage Decouple
Pin 9 D.C. Feedback Decouple
Pin 10 SRF Input
Pin 11 DSM Output
Pin 12 Sign Bit Input
Pin 13 DSM Input
Pin 14 V_{CC}
Pin 15 Unfiltered Analogue Output
Pin 16 Digital 0V
Pin 17 Decoder Clock
Pin 18 Encoder Clock

FERRANTI semiconductors

ZNPCM3

Single Chip Synchronous Codec

ADVANCE PRODUCT INFORMATION

A Single Chip Synchronous Codec

FEATURES

- Converts analogue voice signals into compressed pcm and vice-versa, using an on-chip delta sigma modulated (DSM) code converter.
- A-law companding characteristic.
- Incorporates fixed ADI.
- Single +5V power supply option.
- Low power option by use of +2V digital supply pin.
- On-chip digital transmit/receive low pass-filters (LPF)
- On-chip 3rd order analogue input high pass filter (HPF). (Optional)
- Power down facility
- On-chip voltage references; wide band, low noise.
- Moulded chip carrier encapsulation

DESCRIPTION

The ZNPCM3 monolithic codec integrated circuit is the result of a joint development programme between British Telecom and Ferranti Electronics Limited. Developed for use in single channel codec systems, the device converts unfiltered audio signals into 8k samples/s compressed 'A' law pcm; the reverse function being performed in the decode direction.

The ZNPCM3 combines the essential features of the popular ZNPCM1 Codec I.C. and the ZNPCM2 Delta-sigma modulator I.C. in addition to providing the transmit/receive filter functions and a time-slot assignment facility.

The ZNPCM3 operates from a 2,048 kHz system clock in the synchronous mode. Operating from a single +5V supply the ZNPCM3 dissipates 300mW when active and 25mW when powered down. Alternatively use of pin 18 with a 2V digital supply reduces the active dissipation by 50%. The device is supplied in a 28 lead moulded or ceramic DIL or a 28 leaded moulded chip carrier, and is designed to operate over the temperature range 0°C to +70°C.

The ZNPCM3 is manufactured using the Ferranti advanced bipolar process (FAB II) which is a simple six mask process. The chip is 95% digital in construction minimising analogue circuit content and precision requirements, enabling a design which has predictable and easily testable transmission characteristics.

The ZNPCM3 performance complies with CCITT system recommendations G711/G712 (1972).

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} .. .. +7 volts
Digital Input Voltage, $V_{IN(D)}$ .. .. +5.5 volts
Analogue Input Voltage, $V_{IN(A)}$ .. .. .. 4 volts pk-to-pk
Operating Temperature Range .. .. .. 0°C to +70°C
Storage Temperature Range .. .. −65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Nom.	Max.	Unit
Analogue Supply Voltage Pin 5 (See Note)	4.75	5.0	5.25	V
Digital Supply Voltage Pin 19 (See Note)	4.75	5.0	5.25	V
Digital Power Pin 18 (See Note)	2.0	–	5.25	V
High-level Output Current, I_{OH}	–	–	−400	μA
Low-level Output Current, I_{OL}	–	–	4	mA
Operating Temperature Range, T_{amb}	0	–	70	°C

ELECTRICAL CHARACTERISTICS (over the recommended operating temperature range).
(a) Digital Inputs and Outputs

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High-level input voltage		2.3	–	–	V
V_{IL}	Low-level input voltage		–	–	0.8	V
V_{OH}	High-level output voltage	V_{CC} = Min. I_{OH} = Max.	2.4	3.5	–	V
V_{OL}	Low-level output voltage	V_{CC} = Min. I_{OL} = Max.	–	–	0.4	V
I_{IH}	High-level input current	V_{CC} = Max. V_{IH} = Min.	–	1	10	μA
I_{IL}	Low-level input current	V_{CC} = Max. V_{IL} = Min.	–	0.2	0.4	mA
I_{CC1}	Supply current	Pin 5 = Pin 18 = Pin 19 = $V_{CC(Max)}$	5 p.dn.	60 act.	–	mA
I_{CC2}	Supply current	Pin 5 = Pin 19 = $V_{CC(Max)}$, Pin 18 = 2V	5 p.dn.	60 act.	–	mA
f	Operating frequency		–	2.048	–	kHz
t_r & t_f	Clock rise and fall time	0.4V - 3.0V transition	5	–	20	ns
t_{pd}	Propagation delay	Clock to PCM output 2.5V level	–	80	100	ns
t_{pw}	Clock pulse width	Between 1.5V levels	200	–	–	ns
C_I	Input capacitance		–	–	10	pF

(b) Analogue Inputs and Outputs

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{AI}	Analogue input voltage for 0dBm0	Measured at 1 kHz	–	1.3	–	V_{pp}
Z_{AI}	Analogue input impedance (Relative to HPF requirements)	Measured at 1 kHz	80	100	1000	kΩ
V_{AO}	Analogue output voltage for 0dBm0	Measured at 1 kHz and 20kΩ	–	1.3	–	V_{pp}
Z_{AO}	Analogue output impedance		–	20	50	Ω
V_C	D.C. voltage across C_5	V_{CC} = max.	10	30	50	mV

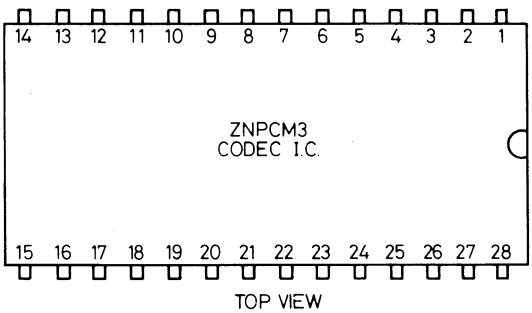
(c) Power Supply Rejection Ratio (Transmit = Receive)

	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
PSSR	Power supply rejection ratio	Over frequency range 200Hz to 50 kHz	40.0	–	–	dB

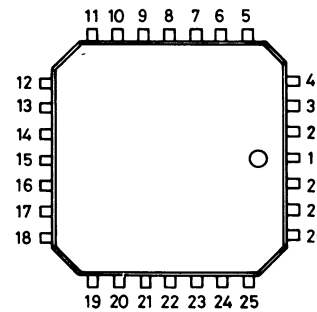
SYSTEM CHARACTERISTICS (Refer to Pages 6 & 7)

Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Idle channel noise	−73	−70	−68	dBm0p	Terminated, no signal, and weighted
Signal-to-distortion ratio CCITT-5385-G712	36 28 23	39 31 26		dB dB dB	Analogue input = 0 to −30dBm0 Analogue input = −40dBm0 Analogue input = −45dBm0
Gain level linearity CCITT-5625. 3-G712	−0.1 −0.1 −0.2	±0.1 ±0.1 ±0.2	+0.1 +0.3 +0.5	dB dB dB	Analogue input = +3 to −40dBm0 Analogue input = −40 to −50dBm0 Analogue input = −50 to −55dBm0
Crosstalk: Encoder on decoder Decoder on encoder		−75 −85		dB dB	Signal level = dBm0

28 Lead Moulded D.I.L. Pin Connections



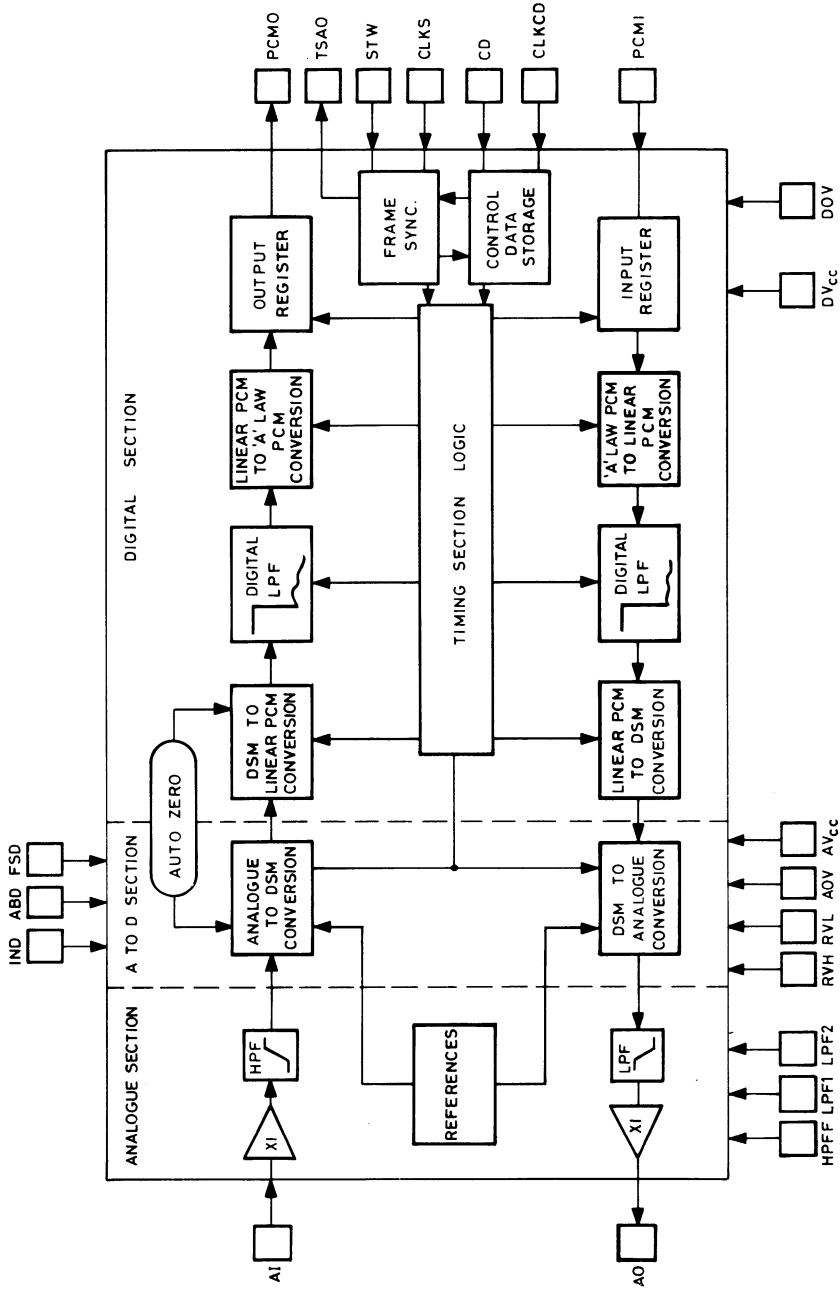
28 Lead Moulded Chip Carrier



ZNPCM3

PIN CONFIGURATIONS

Pin	Notation	Comments
1	CD	CONTROL DATA - Time slot and power up/down data input
2	AI	ANALOGUE INPUT - $0.455V_{rms}$ = 0dBm0
3	HPFF	HIGH PASS FILTER FEEDBACK
4	IND	INTEGRATOR DECOUPLE - DSM gain shaping
5	AV_{CC}	ANALOGUE +5V SUPPLY - Not internally connected to DV_{CC}
6	ABD	AUTO BIAS DECOUPLE
7	FSB	FAST START BIAS - On chip fast start reference voltage
8	RVH	REFERENCE VOLTAGE HIGH - On chip analogue reference voltage
9	RVL	REFERENCE VOLTAGE LOW - On chip analogue reference voltage
10	A0V	ANALOGUE 0 VOLTS - Not internally connected to D0V
11	LPF1	LOW PASS FILTER CAPACITOR - Analogue output filter
12	AO	ANALOGUE OUTPUT - $0.455V_{rms}$ = 0dBm0
13	LPF2	LOW PASS FILTER CAPACITOR - Analogue output filter
14	N.C.	NO CONNECTION
15	TSAO	TIME SLOT ACTIVE OUTPUT - Open collector 'low' with time slot active
16	PCMO	PCM OUTPUT - Fixed data rate 2048k Bit/s
17	D0V	DIGITAL 0 VOLTS - Supply
18	DV_{CC2}	DIGITAL 2V SUPPLY
19	DV_{CC1}	DIGITAL +5V SUPPLY
20	N.C.	NO CONNECTION
21	N.C.	NO CONNECTION
22	N.C.	NO CONNECTION
23	N.C.	NO CONNECTION
24	N.C.	NO CONNECTION
25	PCMI	PCM INPUT - Fixed data rate 2048k Bit/s
26	STW	SYSTEM TIMING WAVEFORM - Codec transmit and receive frame sink
27	CLKCD	CONTROL DATA CLOCK (øC)
28	CLKS	SYSTEM CLOCK (øS) - 2048 kHz



System Diagram

PERFORMANCE

The ZNPCM3 single chip codec meets all the performance requirements of the CCITT recommendation G712 with good safety margins. Using a standard pcm multiplex tester and a spectrum analyser the following performance figures result:

1. Idle channel noise: −70dBm0 (See Fig. 1). CCITT recommendation = −65dBm0p.
2. Signal-to-noise ratio and gain level linearity: Figs. 2(a) and 2(b) show the results using a 450 −550 kHz pseudo-random noise test.
3. Intermodulation distortion: measured products are at least 10dB and on average 18dB better than CCITT recommendations.

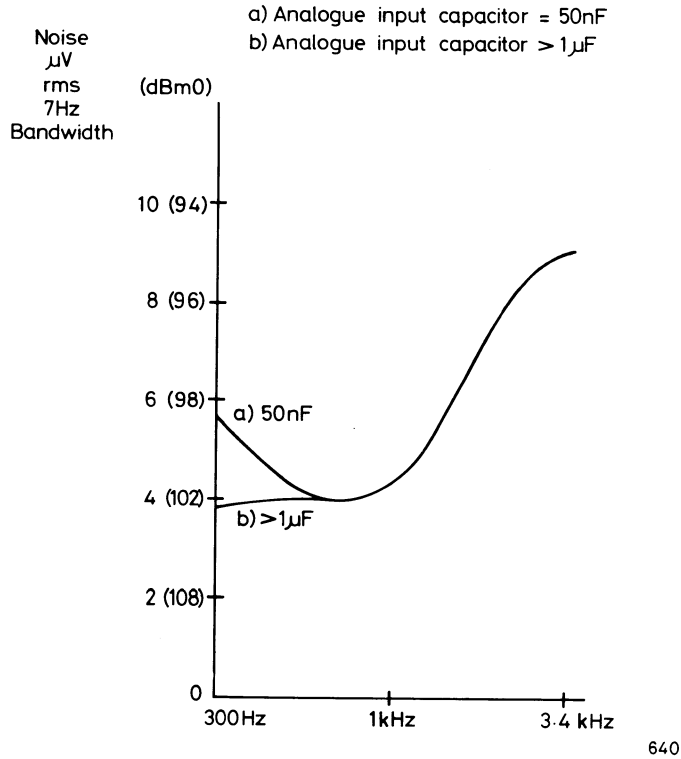


Fig. 1 Idle Channel Noise Spectrum

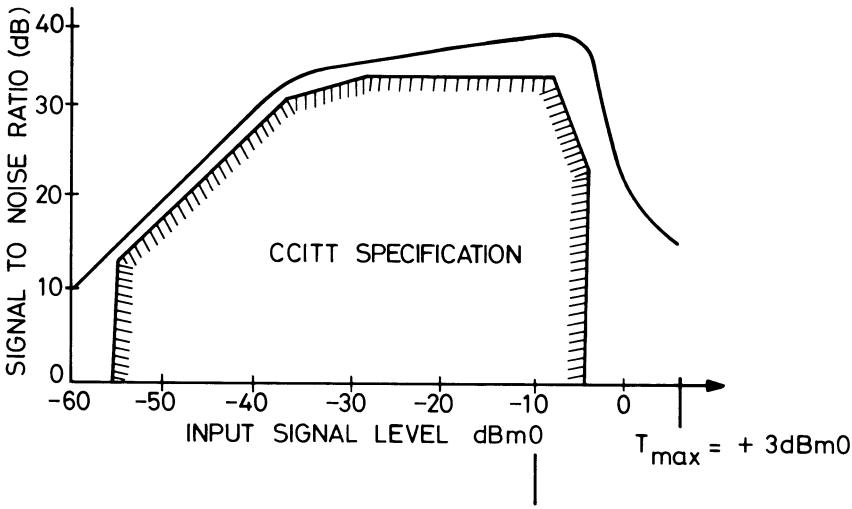


Fig. 2(a) Signal to Noise Ratio 'A Law'

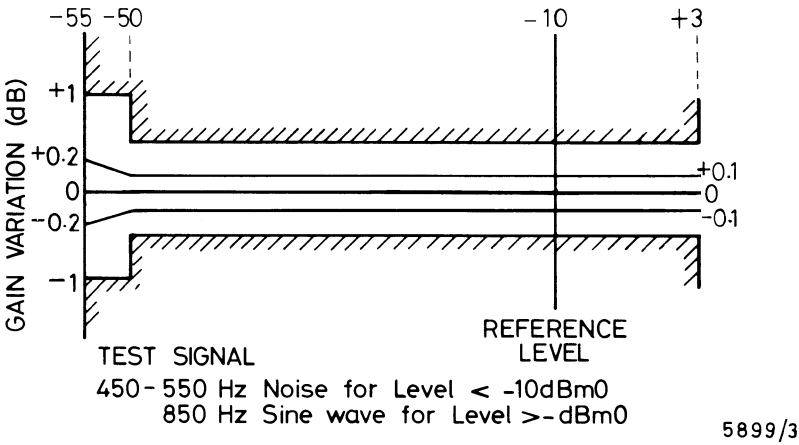


Fig. 2(b) Gain to Signal Level 'A Law'

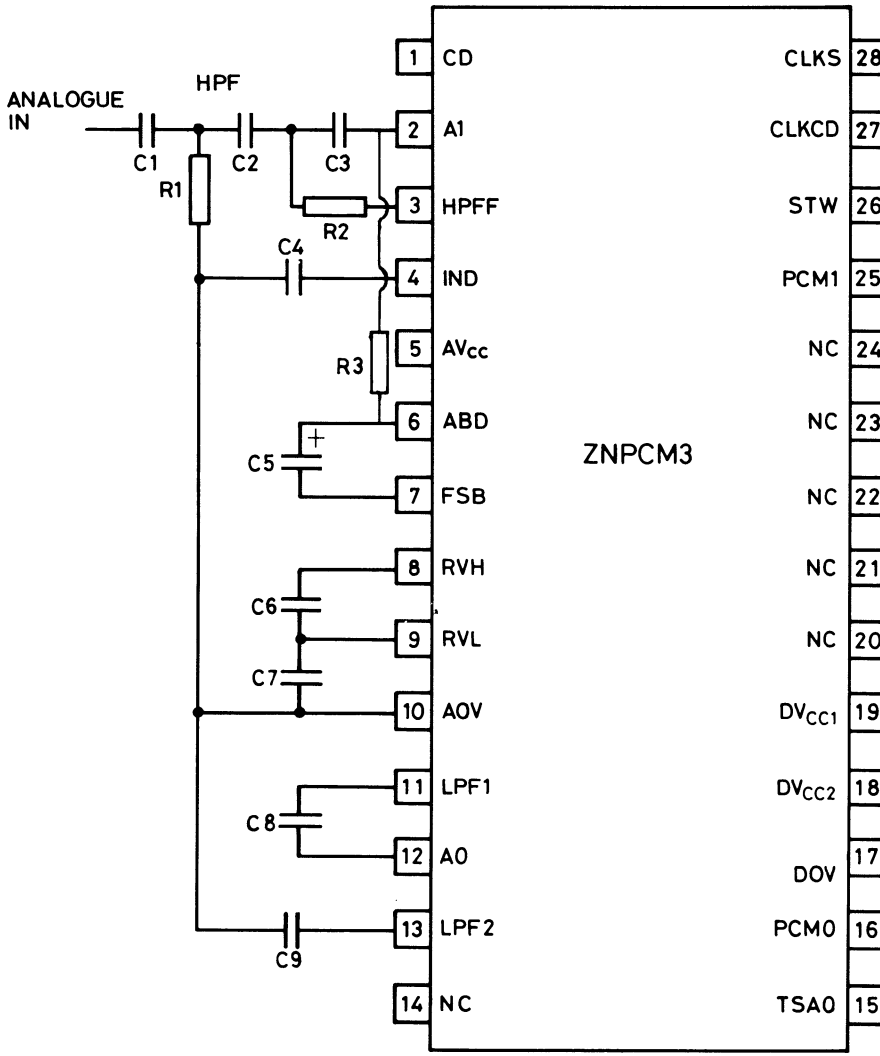


Fig. 3 External Components Required for the ZNPCM3

COMPONENT LIST (for 3rd order HPF input requirements).

C_1	10nF	C_7	0.22μF 20%
C_2	1nF	C_8	470pF 5%
C_3	10nF	C_9	1nF 5%
C_4	5nF 10%	R_1	111KΩ
C_5	4.7μF Tantalum Electrolytic (1st order HPF) 47μF Tantalum Electrolytic (3rd order HPF)	R_2	71KΩ
C_6	0.22μF 20%	R_3	1MΩ

Notes

1. The external high frequency decoupling between pins 8, 9 and 10, should be of minimal impedance (i.e. in the range of 1 to 20 MHz). Low loss capacitors connected via minimal conductor path lengths and inductances are required. Suitable capacitors are 0.22μF monoblock types. Total connection length and resistance including capacitor leads should be as follows:

   Pins 8 to 9 $<$16mm and $<0.1\Omega$
   Pins 9 to 10 $<$20mm and $<0.1\Omega$

2. When commoning system analogue and digital 0V supplies it is recommended that the link be close to pins 10 and 17.
3. Time constants formed by combinations C1R1, C2R2 and C3R3 should have tolerances of $\pm 5\%$.
4. For basic 1st order HPF only R_3, (1MΩ max.) which determines the input impedance and C_3 are required.

General Operation of ZNPCM3

Digital conversion for both ENCODE and DECODE sections operates essentially at the immediate sample rate of 32kHz with the consequence that sin x/x correction is not required and that 4 PCM output samples are available in each 125μs frame enabling the normal PCM transport delay to be reduced by a factor of 4 to 31μs.

Transmit and receive gain variation is determined by the A to D and D to A voltage references. Individually gains are held to within ± 0.3dB absolute and matched to typically ± 0.05dB.

Power up/down is achieved via program data control.

Transmit Operation

The analogue input signal is passed directly via a unity gain 3rd order analogue HPF (to reject DC to 60Hz noise frequencies) to a unity gain tracking A-D converter delivering 2048 kHz sample rate DSM to the ENCODER digital section for subsequent conversion to 8 kHz sample rate 'A' law PCM with ADI. The entire DSM to PCM conversion including 5th order elliptic LPF and 'A' law compression is realised digitally and hence completely free from performance variations. The ENCODER transmission frame is set by the system timing waveform and PCM is transmitted at a fixed 2048k Bit/s rate during one of the 32 time slot allocations defined by the program data control. (See Time Slot Assignment).

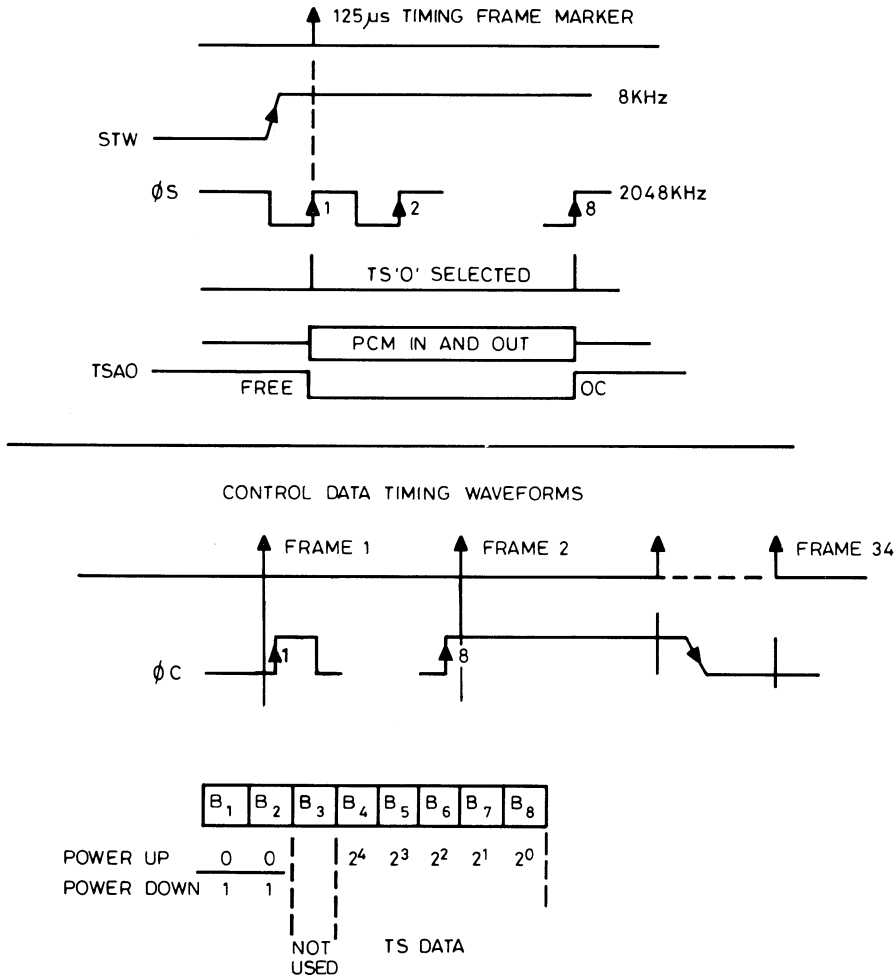
Receive Operation

PCM is accepted by the DECODE section synchronously i.e. time slot and frame timing being identical for both ENCODE and DECODE sections. Additional non quantized PCM transmission delays of up to 200ns can be tolerated. Conversion from 'A' law PCM to 2048 kHz sample rate DSM including necessary 5th order elliptic LP filtering is again realised digitally. The DSM output samples are level quantized and the analogue output signal is recovered via a second order unity gain buffered LPF with low output impedance capable of driving a maximum of 10kΩ load.

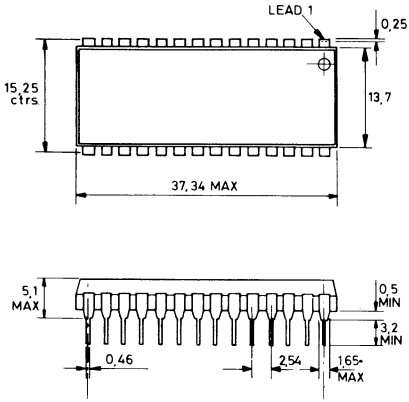
Time Slot Assignment and Power UP/DOWN

A control data clock CLKCD (øC) of eight positive pulses at ≥ 64 kHz inputs the 8-bit Control Data (CD) word. The first two bits are power up/down data and the last five bits are normal binary encoded TSA '0' to '31' data with the LSB being bit 8. Bit 3 is not used. The last CLKCD pulse should remain positive for greater than one frame when the new data will be latched in and acted upon but less than 33 frames or operation will automatically revert to time slot 0. If CLKCD remains positive for less than one frame the old data will be retained.

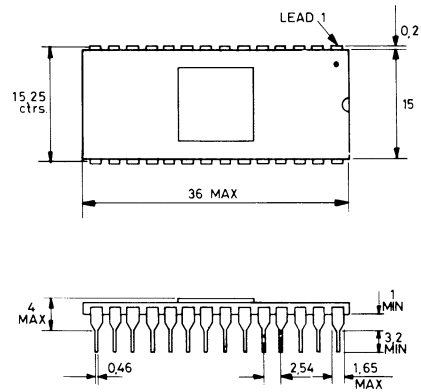
Fig. 4 Time Slot Assignment Waveforms for ZNPCM3



PACKAGE DETAILS

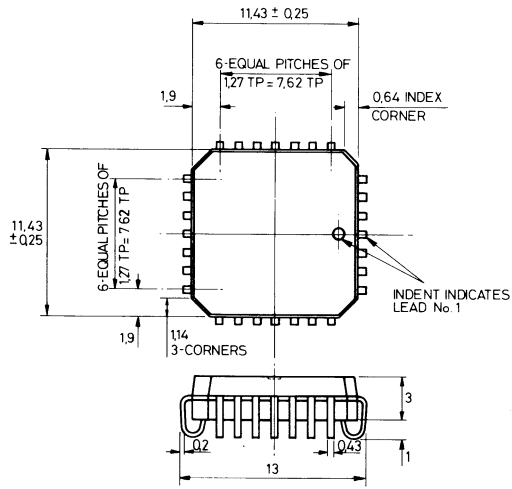


28 Lead Moulded D.I.L.



28 Lead Ceramic D.I.L.

Dimensions in Millimetres



28 Lead Moulded Chip Carrier

ZN470AE
ZN472E

FERRANTI semiconductors

Microphone Amplifier For Telephone Circuits

FEATURES

- Conforms to BT Specification S1377
- On Chip Bridge Allows Dual Supply Polarity Operation
- Direct Matching to Electret Transducers
- 4 Gain Settings by Adjustable Links
- Operates from 1mA to 100mA Line Current
- 220mA 20 Second Overload Capacity
- Low Noise
- Low Distortion
- Operates on Telephone Supply Lines
- Meets BT Lightning Surge Requirements
- Minimum External Components in Telephone Circuits
- Two different pinnings available

DESCRIPTION

This microphone amplifier was developed in conjunction with British Telecom for use with an electret transducer to replace the carbon transmitter. Dual polarity operation is accommodated by an on-chip bridge. Full lightning surge protection is given by on-chip components thus eliminating the need for an external surge suppression diode. The high input impedance makes it suitable for use with high or low impedance microphones that provide a high output voltage.

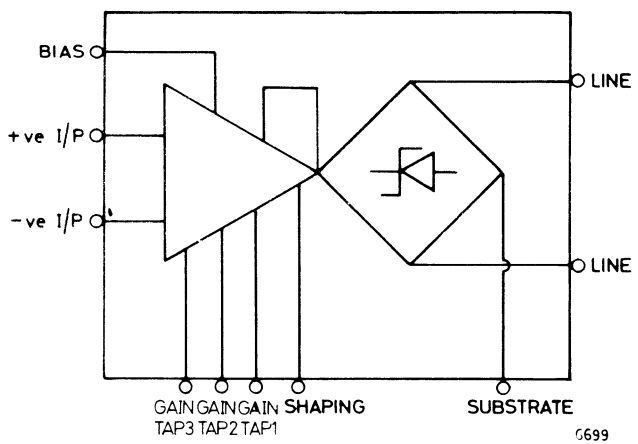


Fig. 1 System Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Current .. .. 120mA continuous
(220mA for 20 seconds)
Operating Temp. Range .. .. .. −20°C to +80°C
Storage Temp. Range .. .. −55°C to +125°C

A.C. CHARACTERISTICS

T_{amb} = 25°C R_L = 100Ω R_O = 15Ω C = 1000pF I_S = 50mA
Pins 2, 3, 6 Open-circuit f = 1kHz V_O = 300mV unless otherwise stated.
Circuit as Fig. 2.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Voltage gain Note 1	A_V	–	20	–	dB	
		–	21.5	–	dB	Pins 3 & 6 shorted
		–	23.4	–	dB	Pins 2 & 3 shorted
		–	25.7	–	dB	Pins 2, 3 & 6 shorted
Change in voltage gain from typical at I_S = 50mA when I_S is changed	$\Delta A_V(I_S)$	−1	−0.1	+1	dB	I_S = 100mA
		−1	−0.5	+1	dB	I_S = 20mA
			−0.9	0	dB	I_S = 10mA
Change in voltage gain with V_O relative to V_O of 300mV	$\Delta A_V(V_O)$	−1	+0.2	+1	dB	V_O = 95mV
		−1	−0.6	+1	dB	V_O = 950mV
Change in voltage gain with line polarity	$\Delta A_V(P)$	–	0.2	0.5	dB	
Output impedance	R_{out}	–	50	–	Ω	
Total harmonic distortion	DH(300)	–	1	3	%	V_O = 300mV
	DH(900)	–	4.5	6	%	V_O = 900mV
Lower cut off frequency	f_{Lco}	–	500	–	Hz	R_b = 6M8Ω C_s = 39pF
Upper cut off frequency	f_{Uco}	–	10	–	kHz	C = 5600pF
		–	200	–	kHz	C = 0
Output noise Note 2	V_{on}	–	170	316	μV	V_{in} = 0
Temperature co-efficient of A_V	$T_c(A_V)$	–	0.1	–	%/°C	T_{amb} = −20°C to +80°C

Note 1 Gains are for circuit in Fig. 2. The actual device gain is higher by about 6dB but a 20pF input capacitance attenuates the electret signal to give 20dB to 25.7dB typical gain.

Note 2 Output noise is measured through a psophometer (CCITT recommendation P53).

ZN470AE
ZN472AE

D.C. CHARACTERISTICS

$T_{amb} = 25°C$, $V_{in} = 0$ with pins 2, 3 and 6 not connected and for either supply polarity unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_S	–	5.55	6.0	volts	$I_S = 21mA$
		6.4	6.8	–	volts	$I_S = 50mA$
		–	9.2	9.7	volts	$I_S = 100mA$
Input Current		–	2	–	nA	$I_S = 50mA$
Input Offset Current		–	0.2	–	nA	$I_S = 50mA$
Input Offset Voltage		–	2.5	–	mV	$I_S = 50mA$

MICROPHONE AMPLIFIER APPLICATION

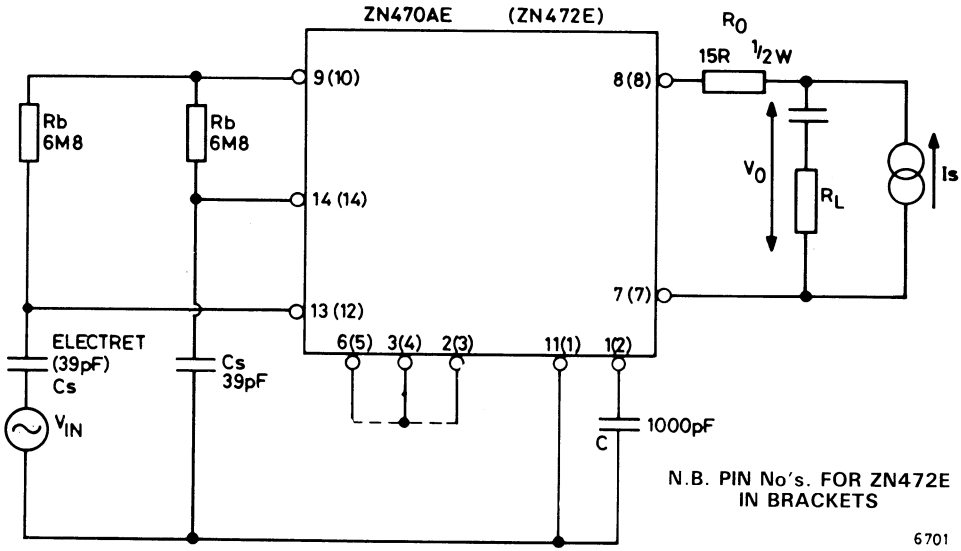


Fig. 2 Typical Electret Microphone Amplifier

The circuit shows ZN470AE/ZN472E with an electret transducer in a typical telephone handset application but with load test included. The gain setting taps may be used to select the appropriate voltage gain to compensate for production spreads in electret sensitivity.

The low frequency cut off is determined by the time constant $C_S R_b$ and a similar matching time constant is required on the other input. C_S is the capacitance of the electret microphone including stray capacitance and its value is therefore determined by the size and characteristics of the types used. The upper frequency cut off is determined by the shaping capacitor C. In addition the overall high frequency response is often controlled by acoustic means.

The leads to the high impedance inputs should be kept as short as possible to avoid the risk of pickup from stray fields.

In locations where high levels of humidity are likely to be encountered it is recommended that precautions are taken to prevent formation of leakage paths between +ve I/P and −ve I/P and between each of these inputs and substrate.

These precautions may take the form of:

a) Guard ring techniques

b) Varnishing or lacquering of the appropriate areas of the PCB.

c) Encapsulation of the complete amplifier module.

The guard ring technique involves completely enclosing the high impedance +ve I/P and −ve I/P nodes by a separate ring of copper. This ring should then be connected to the bias pin as this has a voltage much nearer to the operating voltage of the input pins compared with the substrate, hence current flowing in any leakage path will be minimised.

Note that the guard ring technique is easier to implement using the ZN472E pinning as indicated in Fig. 3.

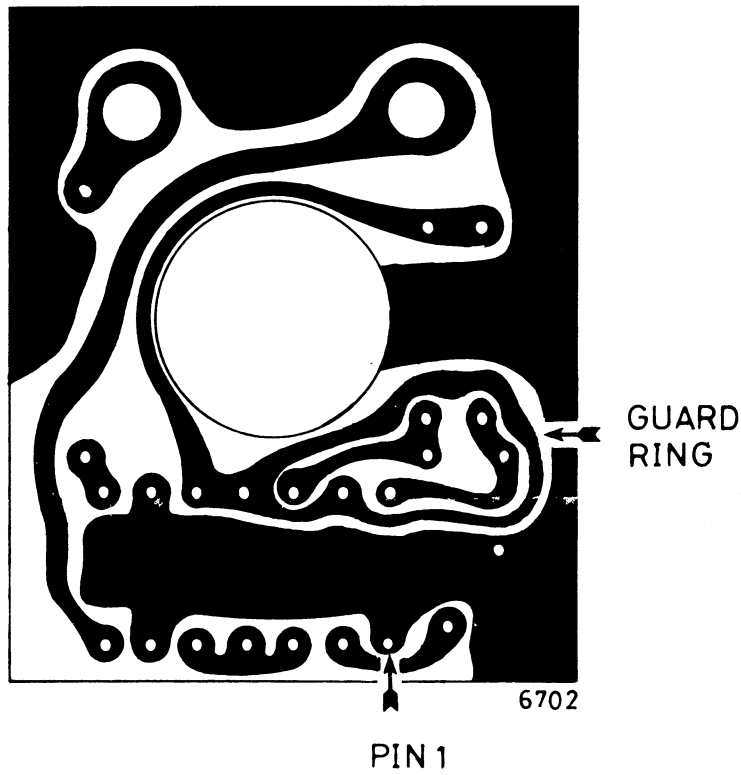
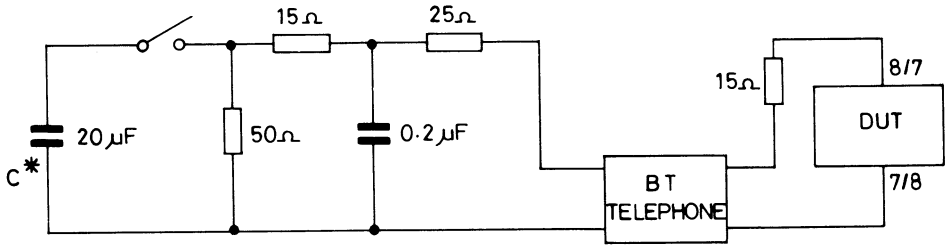


Fig. 3 Reverse Side of a PCB Indicating Guard Ring Screening on the ZN472E.

BT LIGHTNING SURGE TEST CIRCUIT



*C CHARGED TO 1500 VOLTS

6412

When the capacitance is fully charged the switch is closed thus discharging the capacitance into the test network. The device under test, DUT, is connected via a 15ohm resistor to the standard microphone wires. The DUT must survive the discharge on either line polarity.

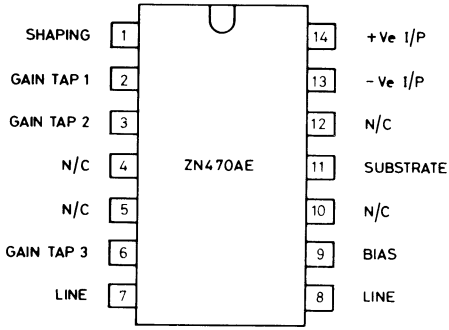
RELIABILITY

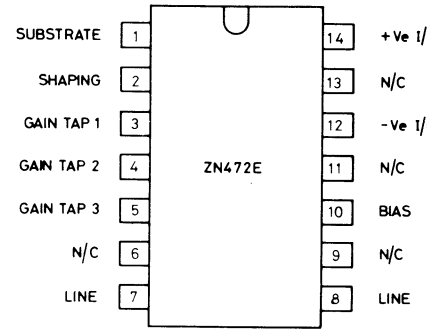
The ZN470AE is fully approved by British Telecom to their specification D3006 for 10 year life applications.

From extensive very long life tests, a predicted failure rate (at 95% confidence level) of less than 0.005% per annum has been calculated for service applications at 45°C and 50mA line current.

ZN470AE
ZN472E

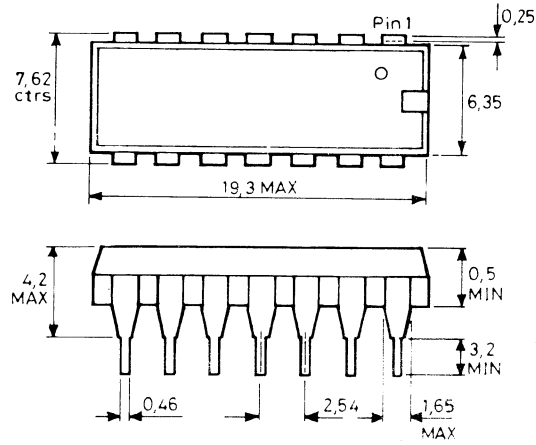
PIN CONNECTIONS





6700

PACKAGE OUTLINE



14 Lead Moulded D.I.L.

Dimensions in Millimetres

FERRANTI semiconductors

ZN473E

Tone Caller with Dial Pulse Reject

ADVANCE PRODUCT INFORMATION

FEATURES

- Full rectifier bridge for direct operation from ringing supply.
- Balanced output for piezo electric or electromagnetic transducers.
- Digital dial pulse rejection.
- Frequency drift eliminated by ceramic resonator.
- Choice of output tones.
- Built-in lightning protection.
- Low external component count.
- Built-in supply voltage regulator.
- Supply voltage threshold.
- Low cost 8 pin DIL package.

GENERAL DESCRIPTION

The ZN473E integrated circuit tone caller is intended to replace existing electromechanical bells in telephone handsets.

The A.C. ringing voltage, V_R, normally supplied to energise the bell is rectified by an on-chip bridge and used to power up the complete circuit.

A standard 560 KHz ceramic resonator is used to control the clock oscillator frequency which is then divided down to give two frequencies with a small separation. The output is switched between these two frequencies at 10 Hz to give a warble tone.

Pin 5 is used to select output frequencies of either 1000 Hz and 1250 Hz or 1167 Hz and 1333 Hz.

To prevent operation of the circuit on dial pulses a digital dial pulse rejection circuit inhibits the output except in the presence of the ringing supply.

The use of the ceramic resonator for clock control gives excellent tone frequency stability with temperature and life and eliminates complicated frequency setting procedures.

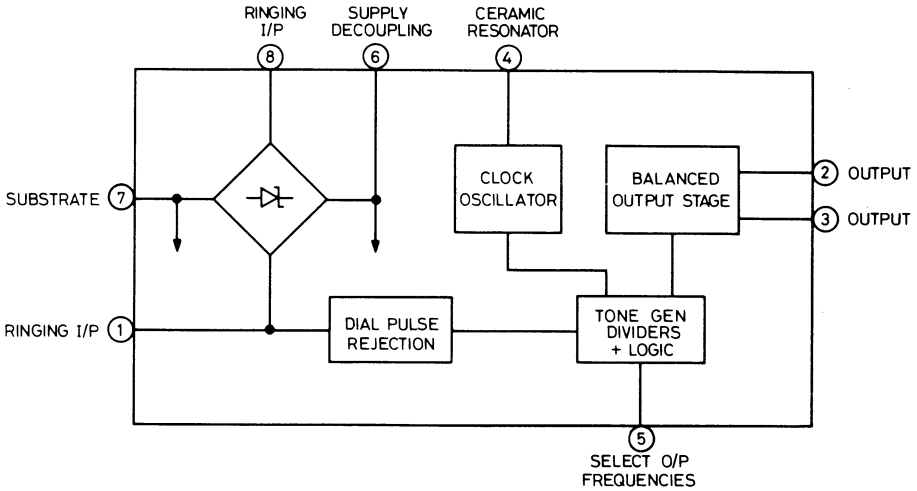


Fig. 1 INTEGRATED CIRCUIT BLOCK DIAGRAM

ZN473E

ABSOLUTE MAXIMUM RATINGS

Ringing input voltage, (V_R)	
a) approx. sinusoidal, via 1200Ω, 14-66 Hz	100 V RMS.
b) distorted sinusoidal, via 100Ω, 25 Hz	53.7 V RMS.
distorted sinusoidal, via 100Ω, 75 Hz	29.6 V RMS.
Power dissipation	500 mW.
Operating temperature	−10°C to +70°C
Storage temperature	−55°C to +125°C

ELE TRICAL CHARACTERISTICS

TEST CIRCUIT See Fig 4 Tambient = 25°C, fc = 560 KHz, V_R = 75v, f_R = 25 Hz unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
High frequency O/P	fH1	–	1333	–	Hz	Pin 5 to Pin 6
Low frequency O/P	fL1	–	1167	–	Hz	
High frequency O/P	fH2	–	1250	–	Hz	Pin 5 to Pin 7
Low frequency O/P	fL2	–	1000	–	Hz	
Warble frequency	fw	–	9.8	–	Hz	
Threshold voltage	V_T	–	9	–	V	
Hysteresis of V_T	V_H	–	2.25	–	V	
Supply current (no load)	Is	–	0.25	0.45	mA	Vs = 20v (Note 1)
Output voltage swing	V_O	50	56	–	Vp.p.	R_L = 3 kΩ
Dial pulse discriminator:—						
Acceptance frequencies	fa	14	–	100	Hz	
Rejection frequencies	fr	0	–	12	Hz	
Small signal standly impedance	Zin	–	100	–	KΩ	V_R = 1.5v f_R = 1 KHz
Noise rejection (hum, speech)	Vr	–	5	–	V peak	
Difference between turn-on & turn-off times. (note 2)	t diff	–	–	100	mS	

Note 1 Vs = D.C. test voltage applied to Pin 6.

Note 2 The turn-on time is the time between the application of the ringing voltage and the output appearing at Pins 2 & 3. Similarly the turn-off time is the time between removal of the ringing voltage and the output turning off.

LIGHTNING PROTECTION.

The I.C. is designed to withstand lightning surges on the line provided a resistor, R in figure 3, is connected in series with the ringing input pins.

Using a value of R = 2 kz the device will survive and still operate to specification after a lightning simulation test as defined in figure 2.

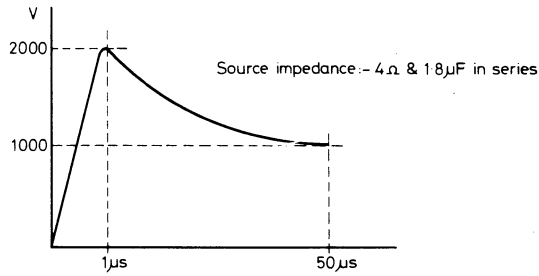


Fig 2 LIGHTNING SURGE TEST 6556

CIRCUIT OPERATION

The operation of the ZN473E is most readily explained with reference to a typical circuit as shown in figure 3.

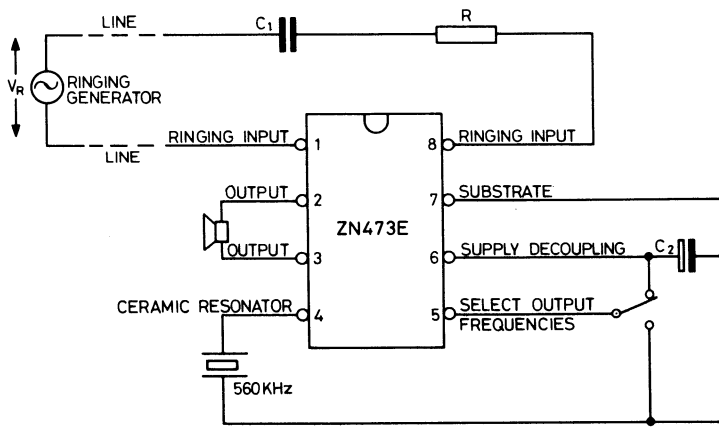


Fig 3 TYPICAL CIRCUIT 6557

The incoming ringing voltage from the line, V_R, typically 70 volts 25Hz, is connected to pins 1 and 8 via a D.C. blocking capacitor C_1, and a current surge limiting resistor R. This applies the ringing voltage to the built-in full wave rectifier bridge and the output is filtered by the reservoir capacitor C_2. This smoothed D.C. supply is then used to power up the remaining circuits.

The frequency of the clock oscillator, fc, is 560 KHz nominal frequency. This is divided down to produce two audio tones fH1 and fL1 or, alternatively, fH2 and fL2 which are selectable using pin 5. The two selected frequencies are switched alternately to the output stage at a fixed rate fw which is obtained by further frequency dividers.

This produces an insistent but pleasant warble tone. An A.C. voltage appearing on the line causes the voltage across C_2 to rise but the output is inhibited until this voltage exceeds the threshold voltage, V_T, and the dial pulse discriminator has detected the presence of the ringing supply.

The ringing supply frequency is normally between 14 Hz and 66 Hz whereas dial pulses occur at 10 Hz to 12 Hz. A digital bandpass filter technique is used to differentiate between the two and inhibit the output when dial pulses are present.

A balanced bridge output stage is used to deliver a square wave output of 50 volts p.p. suitable for driving a transducer of approximately 3 KΩ impedance. The transducer may be either an eletromagnetic, e.g. rocking armature type or a piezo electric ceramic disc.

APPLICATIONS

- Replacement for electromechanical bell in telephone handsets.
- Ring detector/tone caller in all-electronic telephones.
- Extension tone callers.

The main application for the ZN473E is to perform the tone caller function in new generation all-electronic telephone handsets. Very few discrete components are required as shown by the typical circuit of figure 4.

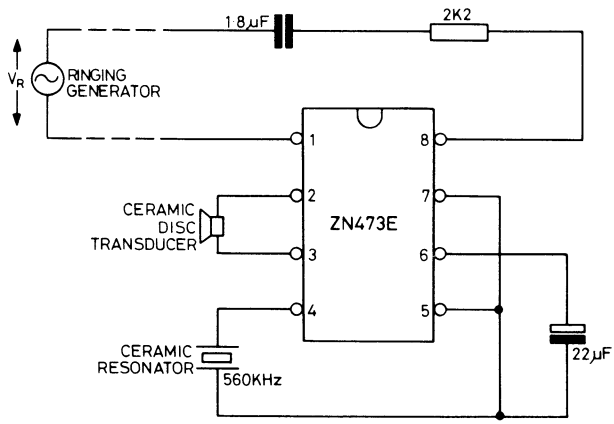
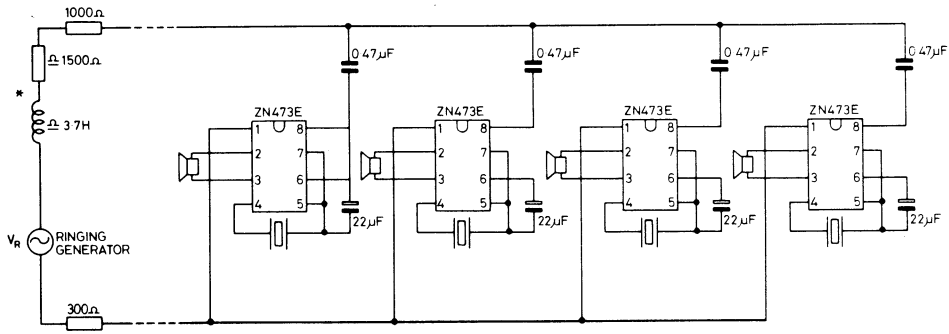


Fig. 4 TYPICAL TELEPHONE APPLICATION CIRCUIT 6558

In this example pin 5 is connected to pin 7 (substrate) which selects ouput frequencies fH2 and fL2. No frequency setting up procedures are called for because the clock frequency, fc, is set by the ceramic resonator. This also ensures very good frequency stability with ambient temperature changes and life.

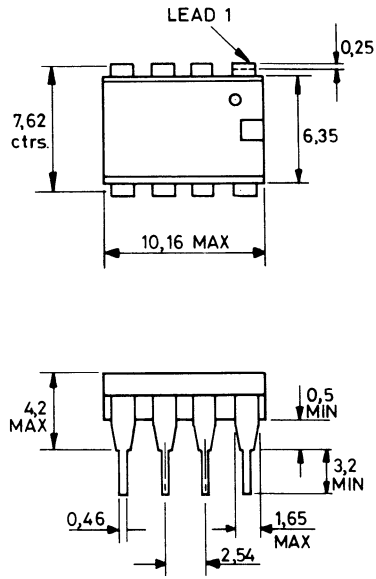
Up to four ZN473E circuits may be operated in parallel on a typical limit length line as shown in Figure 5.



*P.O. F-relay with 400Ω coil shorted and armature open

Fig. 5 PARALLEL OPERATION ON LIMIT LENGTH TELEPHONE LINE

PACKAGE OUTLINE



8 Lead Moulded D.I.L.
Dimensions in millimetres.

ZN475E

FERRANTI semiconductors

Microphone Amplifier for Telephone Circuits

FEATURES

- Direct Matching to Electret Transducers
- Gain Adjustable by External Resistor
- Operates from 1mA to 100mA Line Current
- Low Noise
- Low Distortion
- Operates on Telephone Supply Lines
- Minimum External Components in Telephone Circuits

DESCRIPTION

Some electret transducers are supplied with a built in impedance matching junction FET buffer to operate with a microphone amplifier of low input impedance. The ZN475E has been designed with a high input impedance to match directly with electret transducers without the need for an FET buffer.

The device operates from a single polarity supply, but includes protection from inadvertent supply reversal.

The amplifier gain can be adjusted over a wide range by an external resistor to suit a variety of different electret transducer sensitivities.

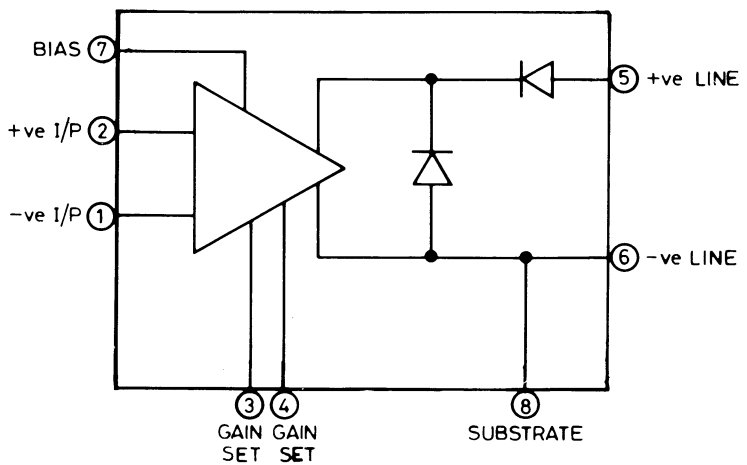


Fig. 1 System Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Current .. .. 100mA continuous (220mA for 20 seconds)
Operating Temp. Range .. .. .. −20°C to +80°C
Storage Temp. Range .. .. −55°C to +125°C

A.C. CHARACTERISTICS

T_{amb} = 25°C R_G = 80kΩ R_L = 100Ω R_O = 15Ω C_G = 100nF I_S = 50mA f = 1kHz V_O = 300mV unless otherwise stated
Circuit as Fig. 2.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Voltage gain Note 1	A_V	–	20	–	dB	
		–	45	–	dB	R_G = 0 C_G = 2μ2F
Change in voltage gain from typical at I_S = 50mA when I_S is changed	ΔA_V (I_S)	−1	−0.1	+1	dB	I_S = 100mA
		−1	−0.5	+1	dB	I_S = 20mA
		–	−0.9	0	dB	I_S = 10mA
Change in voltage gain with V_O relative to V_O of 300mV	ΔA_V (V_O)	−1	+0.2	+1	dB	V_O = 95mV
		−1	−0.6	+1	dB	V_O = 950mV
Output impedance	R_{out}	–	50	–	Ω	
Total harmonic distortion	DH(300)	–	1	3	%	V_O = 300mV
	DH(900)	–	4.5	6	%	V_O = 900mV
Lower cut off frequency	f_{Lco}	–	500	–	Hz	R_b = 6.8MΩ C_s = 39pF
Upper cut off Frequency	f_{Uco}	–	200	–	kHz	
Output noise Note 2	V_{on}	–	170	316	μV	V_{in} = 0
Temperature co-efficient of A_V	T_c (A_V)	–	0.2	–	%/°C	T_{amb} = −20 to +80°C

Note 1 Gains are for circuit in Fig. 2. The actual device gain is higher by about 6dB but a 20pF input capacitance attenuates the electret signal to give 20dB to 25.7dB typical gain.
Note 2 Output noise is measured through a psophometer (CCITT recommendation P53).

D.C. CHARACTERISTICS

$T_{amb} = 25°C$, $V_{in} = 0$, $R_G = 51k\Omega$

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_S	–	4.95	5.4	volts	$I_S = 21mA$
		5.8	6.2	–	volts	$I_S = 50mA$
		–	8.5	9.0	volts	$I_S = 100mA$
Input Current		–	2	–	nA	$I_S = 50mA$
Input Offset Current		–	0.2	–	nA	$I_S = 50mA$
Input Offset Voltage		–	2.5	–	mV	$I_S = 50mA$

MICROPHONE AMPLIFIER APPLICATION

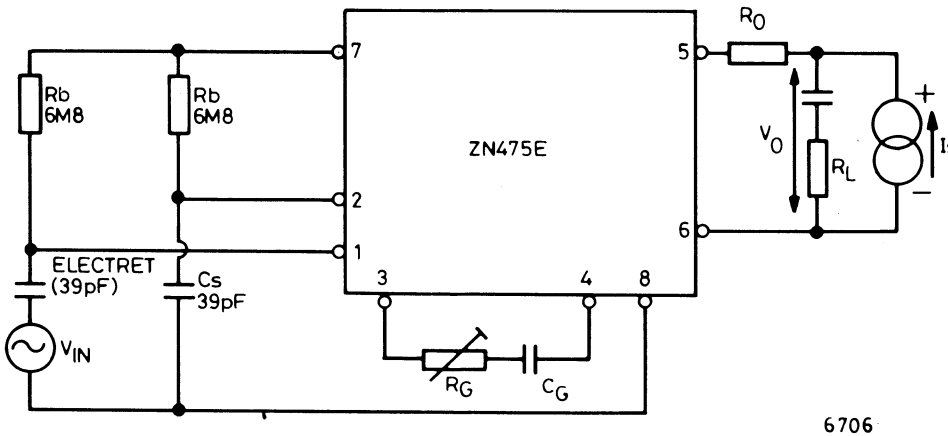


Fig. 2 Typical Electret Microphone Amplifier

The circuit shows ZN475 with an electret transducer in a typical telephone handset application but with load test included.

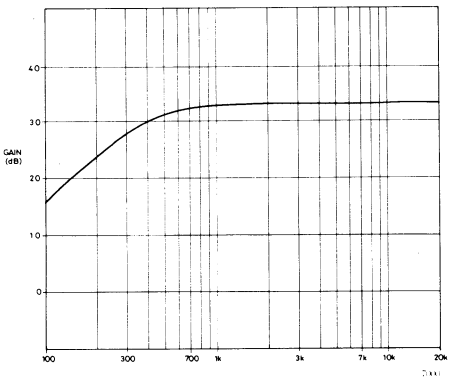
The low frequency cut off is determined by the time constant $C_S R_b$ and a similar matching time constant is required on the other input. C_S is the capacitance of the electret microphone including stray capacitance and its value is therefore determined by the size and characteristics of the types used. It is recommended that the overall high frequency response is controlled by acoustic means.

The leads to the high impedance input should be kept as short as possible to avoid the risk of pickup from stray fields.

In addition to the lower cut-off frequency f_{LCO} due to the time constant at the input there is an additional break-point at frequency f_L determined by C_G and R_G from the expression

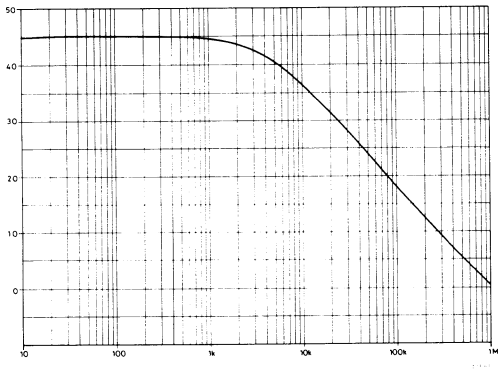
$$f_L \simeq \frac{1}{2\pi C_G (R_G + 5000)}$$

Conditions I_S = 50mA R_O = 15Ω C_G = 100nF R_G = 10kΩ



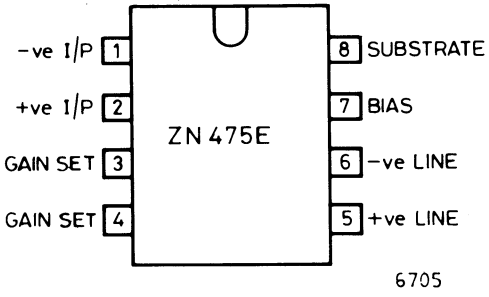
Gain (dB) vs Frequency (Hz)

Conditions I_S = 50mA R_O = 15Ω R_L = 100Ω C_G = 2.2μF f = 1kHz



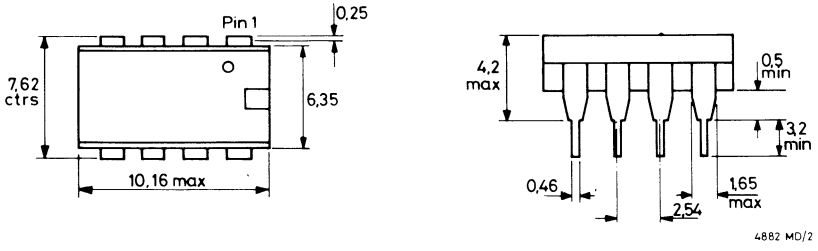
Gain (dB) vs R_G (I.C.)

PIN CONNECTIONS



6705

PACKAGE OUTLINE



4882 MD/2

8 Lead Moulded D.I.L.
Dimensions in Millimetres

ZN476E

FERRANTI semiconductors

Microphone Amplifier for Telephone Circuits

FEATURES

- On Chip Bridge Allows Dual Supply Polarity Operation
- Direct Matching to Low Impedance (Moving Coil) Transducers
- Gain Adjustable by External Resistor
- Operates from 1mA to 100mA Line Current
- Low Noise
- Operates on Telephone Supply Lines
- Minimum External Components in Telephone Circuits

DESCRIPTION

The ZN476E was developed specifically for use with low impedance transducers such as moving coil microphones to replace the carbon transmitter in telephone handsets. Dual polarity operation is accommodated by an on-chip bridge. Full lightning surge protection is given by on-chip components thus eliminating the need for an external surge suppression diode.

The amplifier gain can be adjusted over a wide range by an external resistor to suit a variety of different low impedance (moving coil) transducer sensitivities.

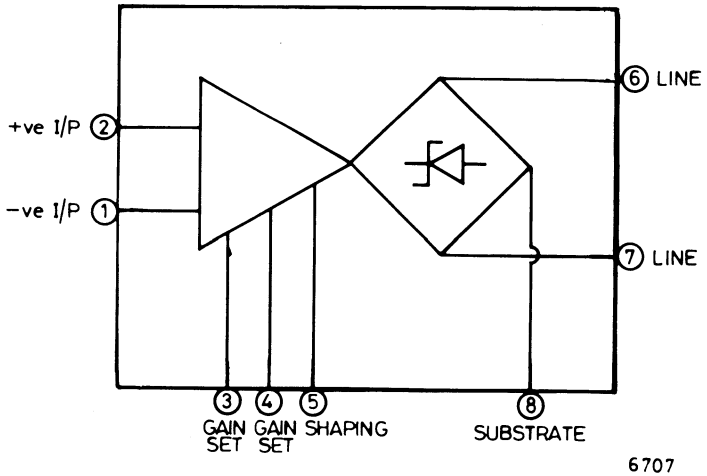


Fig. 1 System Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Current .. .. 100mA continuous
Operating Temp. Range .. .. .. −20°C to +80°C
Storage Temp. Range .. .. −55°C to +125°C

A.C. CHARACTERISTICS

$T_{amb} = 25°C$ $R_G = 25k\Omega$ $R_L = 100\Omega$ $C_G = 100nF$ $R_O = 15\Omega$ $I_S = 50mA$ $C_S = 1nF$ $f = 1kHz$
$V_O = 300mV$ unless otherwise stated.
Circuit as Fig. 2.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Voltage gain	A_V	17	20	23	dB	
		37	40	43	dB	$R_G = 1.5k\Omega$ $C_G = 2.2\mu F$
Change in voltage gain from typical at $I_S = 50mA$ when I_S is changed	ΔA_V (I_S)	−1	−0.1	+1	dB	$I_S = 100mA$
		−1	−0.5	+1	dB	$I_S = 20mA$
		–	−0.9	0	dB	$I_S = 10mA$
Change in voltage gain with V_O relative to V_O of 300mV	ΔA_V (V_O)	−1	+0.2	+1	dB	$V_O = 95mV$
		−1	−0.6	+1	dB	$V_O = 950mV$
Change in voltage gain with line polarity	ΔA_V (P)	–	0.2	0.5	dB	
Output impedance	R_{out}	–	50	–	Ω	
Total harmonic distortion	DH(300)	–	1	3	%	$V_O = 300mV$
	DH(900)	–	4.5	6	%	$V_O = 900mV$
Temperature co-efficient of A_V	T_c (A_V)	–	0.2	–	%/°C	$T_{amb} = -20°C$ to $+80°C$

D.C. CHARACTERISTICS

$T_{amb} = 25°C$, $V_{in} = 0$ $R_G = 25k\Omega$ for either supply polarity unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_S	–	5.55	6.0	volts	$I_S = 21mA$
		5.4	6.8	–	volts	$I_S = 50mA$
		–	9.2	9.7	volts	$I_S = 100mA$

MICROPHONE AMPLIFIER APPLICATION

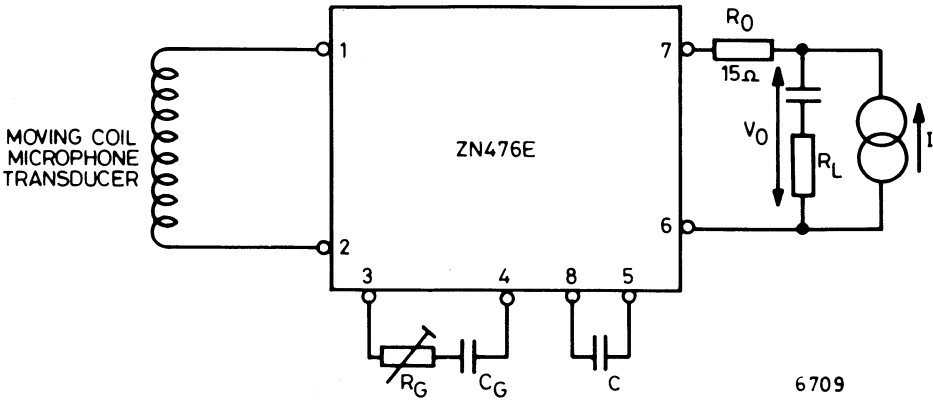


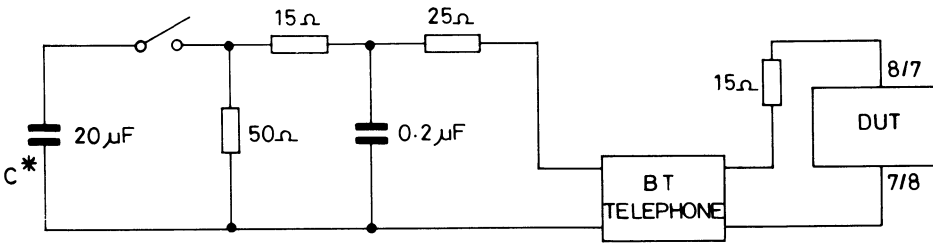
Fig. 2 Typical Application Circuit

The circuit shows ZN476E with a moving coil transducer in a typical telephone handset application but with load test included. The value of R_G is set to give the appropriate voltage gain for the particular transducer in use.

The value of the lower cut-off frequency f_L is determined by C_G and R_G from the expression

$$f_L \simeq \frac{1}{2\pi C_G(R_G + 500)}$$

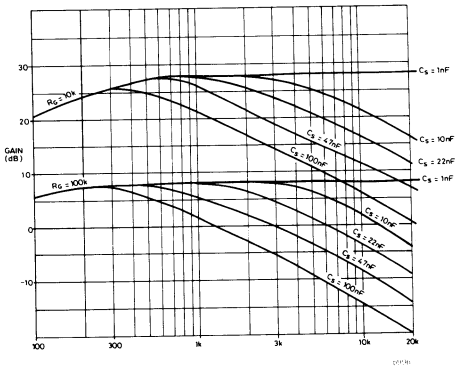
BT LIGHTNING SURGE TEST CIRCUIT



*C CHARGED TO 1500 VOLTS

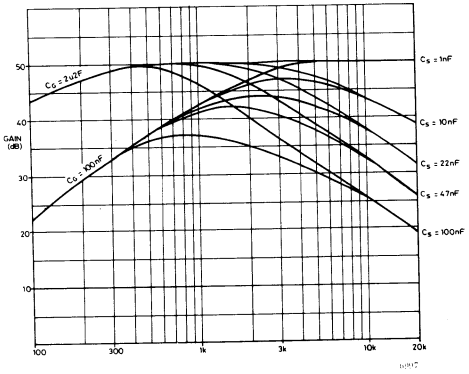
When the capacitor is fully charged the switch is closed thus discharging the capacitor into the test network. The device under test, DUT, is connected via a 15ohm resistor to the standard microphone wires. The DUT must survive the discharge on either line polarity.

Conditions R_G = 10k and R_G = 100k I_C = 50mA C_G = 100nF



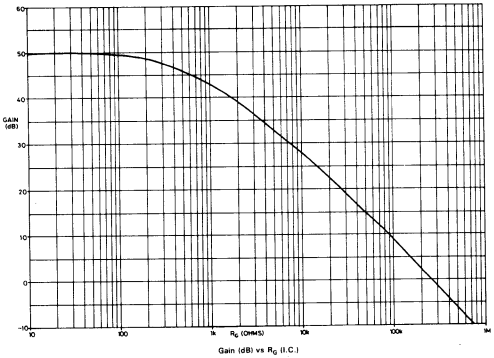
Gain (dB) vs Frequency (Hz)

Conditions R_G = 0Ω I_C = 50mA



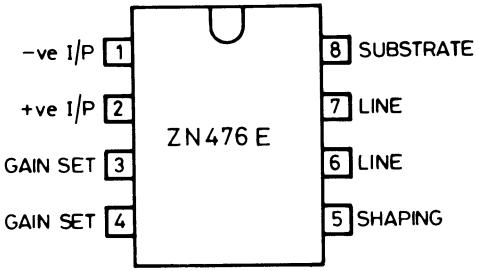
Gain (dB) vs Frequency (Hz)

Conditions C_G = 2.2μF f = 1kHz I_C = 50mA C_S = 1nF

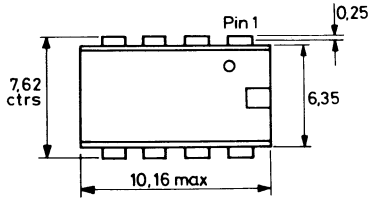


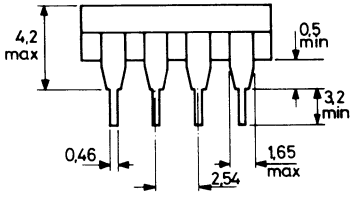
Gain (dB) vs R_G (I.C.)

PIN CONNECTIONS



PACKAGE OUTLINE





4882 MD/2

8 Lead Moulded D.I.L.
Dimensions in Millimetre

ZN477E

FERRANTI semiconductors

Microphone Amplifier for Telephone Circuits

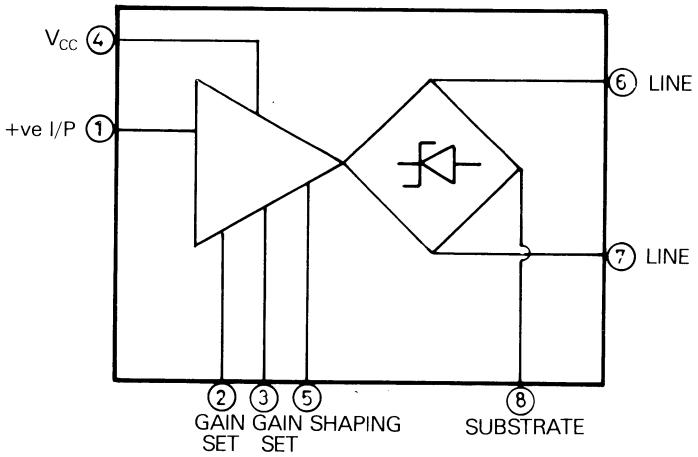
FEATURES

- On Chip Bridge Allows Dual Supply Polarity Operation
- Designed to match electrets with FET buffers
- Gain Adjustable by External Resistor
- Operates from 1mA to 100mA Line Current
- Low Noise
- Low Distortion
- Operates on Telephone Supply Lines
- Minimum External Components in Telephone Circuits

DESCRIPTION

The ZN477E was developed specifically for use with low impedance transducers such as electrets (with FET buffers) microphones to replace the carbon transmitter in telephone handsets. Dual polarity operation is accommodated by an on-chip bridge. Full lightning surge protection is given by on-chip components thus eliminating the need for an external surge suppression diode.

The amplifier gain can be adjusted over a wide range by an external resistor to suit a variety of different low impedance transducer sensitivities.



6728

Fig. 1 System Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Current .. .. 100mA continuous
Operating Temp. Range .. .. .. −20°C to +80°C
Storage Temp. Range .. .. −55°C to +125°C

A.C. CHARACTERISTICS

T_{amb} = 25°C R_G = 25kΩ R_L = 100Ω C_G = 100nF R_O = 15Ω I_S = 50mA C_S = 1nF f = 1kHz
V_O = 300mV unless otherwise stated.
Circuit as Fig. 2.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Voltage gain	A_V	17	20	23	dB	
		–	28	–	dB	R_G = 10kΩ min. rec. value
Change in voltage gain from typical at I_S = 50mA when I_S is changed	ΔA_V (I_S)	−1	−0.1	+1	dB	I_S = 100mA
		−1	−0.5	+1	dB	I_S = 20mA
		–	−0.9	0	dB	I_S = 10mA
Change in voltage gain with V_O relative to V_O of 300mV	ΔA_V (V_O)	−1	+0.2	+1	dB	V_O = 95mV
		−1	−0.6	+1	dB	V_O = 950mV
Change in voltage gain with line polarity	ΔA_V (P)	–	0.2	0.5	dB	
Output impedance	R_{out}	–	50	–	Ω	
Total harmonic distortion	DH(300)	–	1	3	%	V_O = 300mV
	DH(900)	–	4.5	6	%	V_O = 900mV
Temperature co-efficient of A_V	T_c (A_V)	–	0.2	–	%/°C	T_{amb} = −20°C to +80°C

I_{FET} to be ⩽ 1mA

D.C. CHARACTERISTICS

T_{amb} = 25°C, V_{in} = 0 R_G = 25kΩ for either supply polarity unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_S	–	5.55	6.0	volts	I_S = 21mA
		5.4	6.8	–	volts	I_S = 50mA
		–	9.2	9.7	volts	I_S = 100mA

MICROPHONE AMPLIFIER APPLICATION

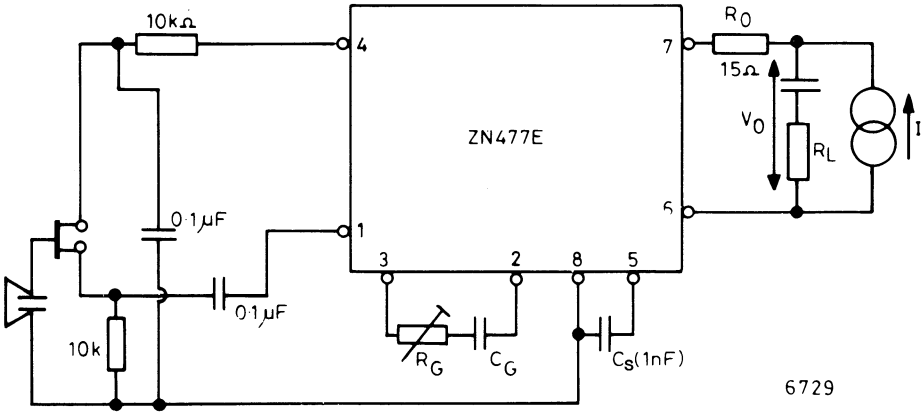


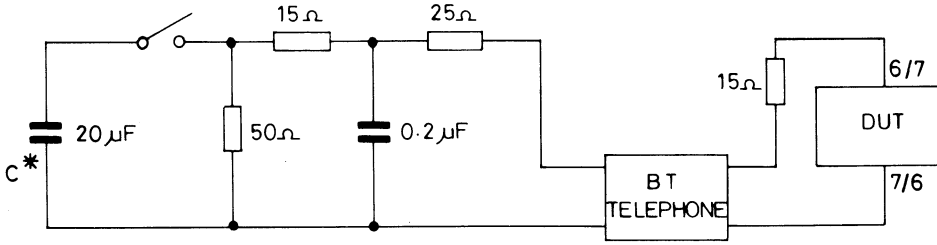
Fig. 2 Typical Application Circuit

The circuit shows ZN477E with a electret plus FET transducer in a typical telephone handset application but with load test included. The value of R_G is set to give the appropriate voltage gain for the particular transducer in use.

The value of the lower cut-off frequency f_L is determined by C_G and R_G from the expression

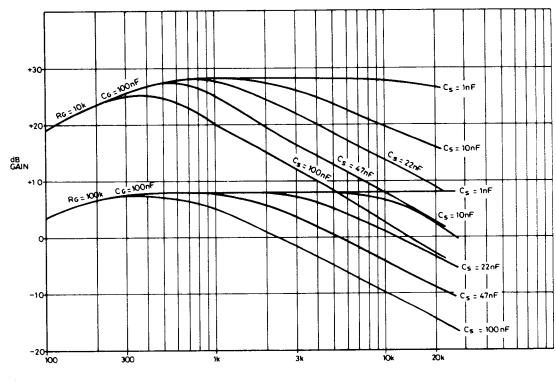
$$f_L = \frac{1}{2\pi C_G(R_G + 500)}$$

BT LIGHTNING SURGE TEST CIRCUIT



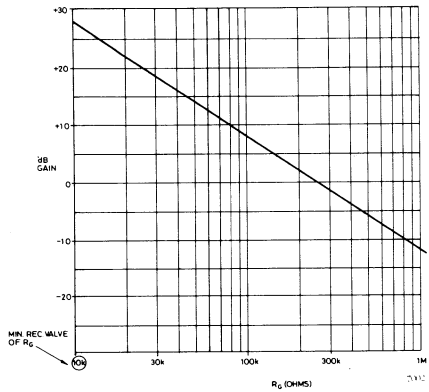
When the capacitor is fully charged the switch is closed thus discharging the capacitor into the test network. The device under test, DUT, is connected via a 15ohm resistor to the standard microphone wires. The DUT must survive the discharge on either line polarity.

Conditions I_L = 50mA

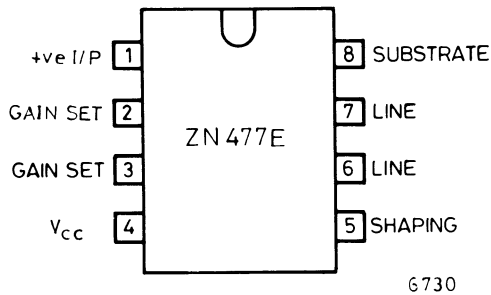


Gain (dB) vs Frequency (Hz)

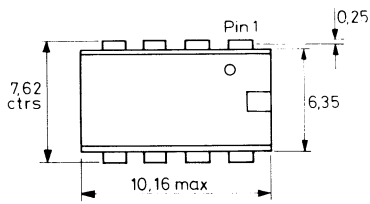
Conditions C_S = 1nF C_G = 100nF f = 1kHz I_L = 50mA

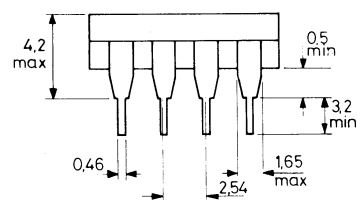


PIN CONNECTIONS



PACKAGE OUTLINE





8 Lead Moulded D.I.L.
Dimensions in Millimetres

ZN478E

FERRANTI semiconductors

Microphone Amplifier for Telephone Circuits

FEATURES

- Low Working Voltage
- Designed to match electrets with FET buffers
- Gain Adjustable by External Resistor
- Operates from 1mA to 100mA Line Current
- Low Noise
- Low Distortion
- Operates on Telephone Supply Lines
- Minimum External Components in Telephone Circuits
- Low Cost

DESCRIPTION

The ZN478E was developed specifically for use with low impedance transducers such as electrets (with FET buffers) microphones to replace the carbon transmitter in telephone handsets. The ZN478E is especially useful where a low operating voltage is required.

The amplifier gain can be adjusted over a wide range by an external resistor to suit a variety of different low impedance transducer sensitivities.

This is a single polarity device and care should be taken over line connection.

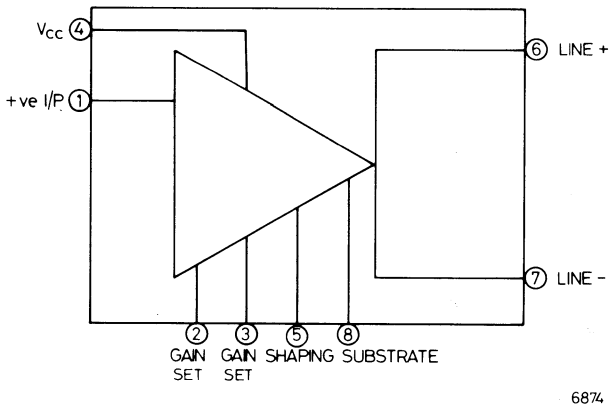


Fig. 1 System Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Current .. .. 100mA continuous
Operating Temp. Range .. .. .. −20 to +80°C
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A.C. CHARACTERISTICS

$T_{amb} = 25°C$ $R_G = 25k\Omega$ $R_L = 100\Omega$ $C_G = 100nF$ $R_O = 15\Omega$ $I_S = 50mA$ $C_S = 1nF$ $f = 1kHz$
$V_O = 300mV$ unless otherwise stated.
Circuit as Fig. 2.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Voltage gain	A_V	17	20	23	dB	
		–	28	–	dB	$R_G = 10k\Omega$ min. rec. value
Change in voltage gain from typical at $I_S = 50mA$ when I_S is changed	ΔA_V (I_S)	−1	−0.1	+1	dB	$I_S = 100mA$
		−1	−0.5	+1	dB	$I_S = 20mA$
		–	−0.9	0	dB	$I_S = 10mA$
Change in voltage gain with V_O relative to V_O of 300mV	ΔA_V (V_O)	−1	+0.2	+1	dB	$V_O = 95mV$
		−1	−0.6	+1	dB	$V_O = 950mV$
Output impedance	R_{out}	–	50	–	Ω	
Total harmonic distortion	DH(300)	–	1	3	%	$V_O = 300mV$
	DH(900)	–	4.5	6	%	$V_O = 900mV$

I_{FET} to be $\leqslant 1mA$

D.C. CHARACTERISTICS

$T_{amb} = 25°C$, $V_{in} = 0$ $R_G = 25k\Omega$ unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	V_S	–	3.9	4.4	volts	$I_S = 21mA$
		4.3	4.6	–	volts	$I_S = 50mA$
		–	7.0	8.5	volts	$I_S = 100mA$

MICROPHONE AMPLIFIER APPLICATION

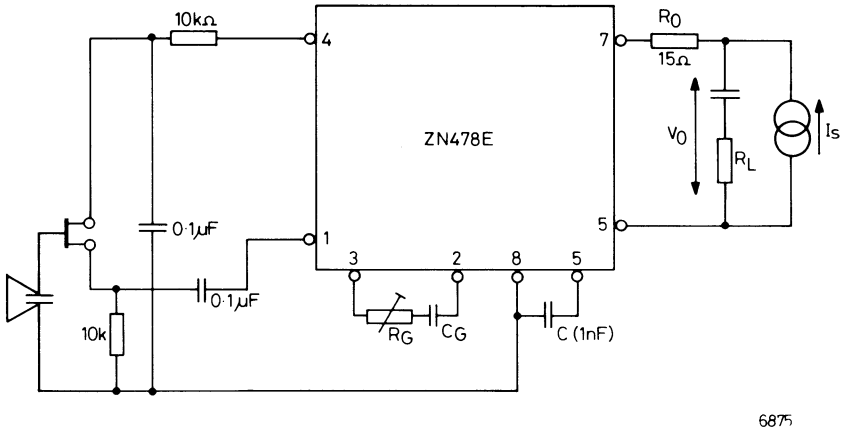


Fig. 2 Typical Application Circuit

The circuit shows ZN478E with a electret plus FET transducer in a typical telephone handset application but with load test included. The value of R_G is set to give the appropriate voltage gain for the particular transducer in use.

The value of the lower cut-off frequency f_L is determined by C_G and R_G from the expression

$$f_L \simeq \frac{1}{2\pi C_G(R_G + 500)}$$

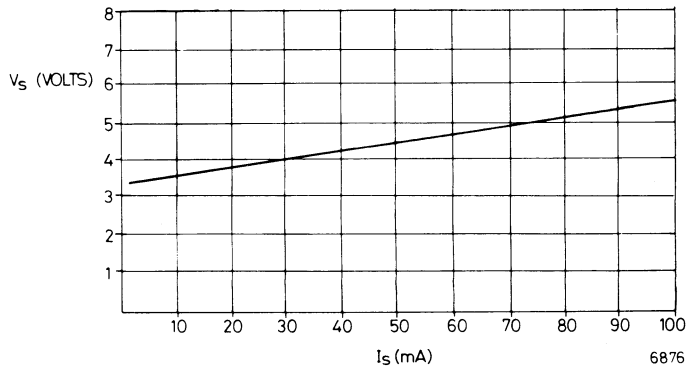
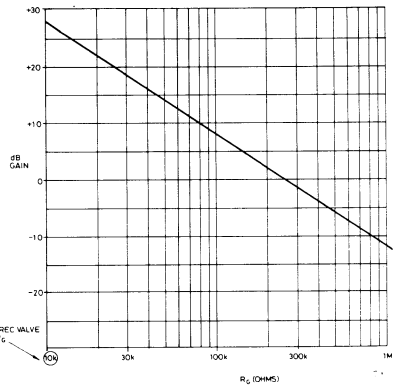
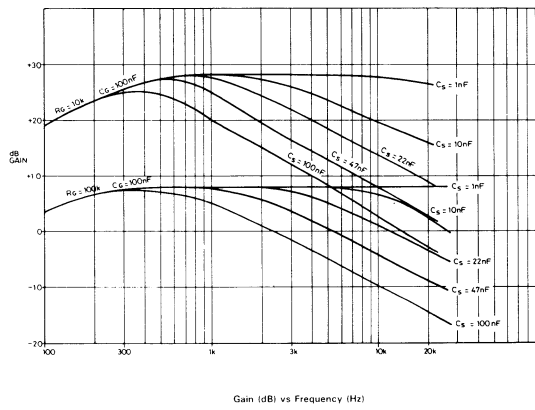


Fig. 3 Average Supply Voltage vs Supply Current for ZN478E

Conditions C_S = 1nF C_G = 100nF f = 1kHz I_L = 50mA

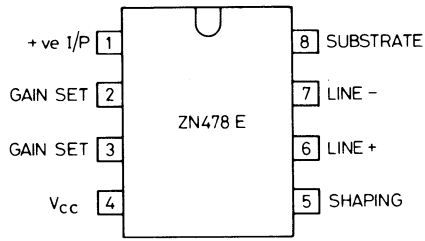


Conditions I_L = 50mA

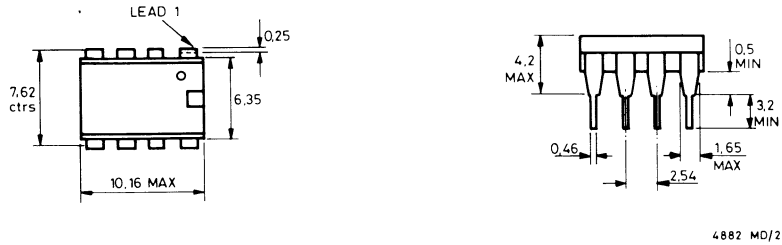


Gain (dB) vs Frequency (Hz)

PIN CONNECTIONS



PACKAGE OUTLINE



8 Lead Moulded D.I.L.
Dimensions in Millimetres

ZN480E

FERRANTI semiconductors

Ring detector with dial pulse reject

ADVANCE PRODUCT INFORMATION

FEATURES

- Full rectifier bridge for direct operation from ringing supply
- TTL logic output
- Digital dial pulse rejection
- Frequency drift eliminated by ceramic resonator
- Built-in lightning protection
- Low external component count
- Built-in supply voltage regulator
- Supply voltage threshold
- Low cost 8 pin DIL package

DESCRIPTION

The ZN480E Ring Detector is intended for use when a special function is required in response to an incoming ringing signal.

A TTL logic output is provided which can be interfaced directly to a wide variety of equipment including microprocessors, answering machines, modems and lamp indicators.

The A.C. ringing voltage V_R is rectified by an on-chip bridge and used to power up the complete circuit.

A standard 560KHz ceramic resonator is used to control the clock oscillator which provides a reference for the dial pulse rejection circuitry inhibiting the output except in the presence of a ringing signal.

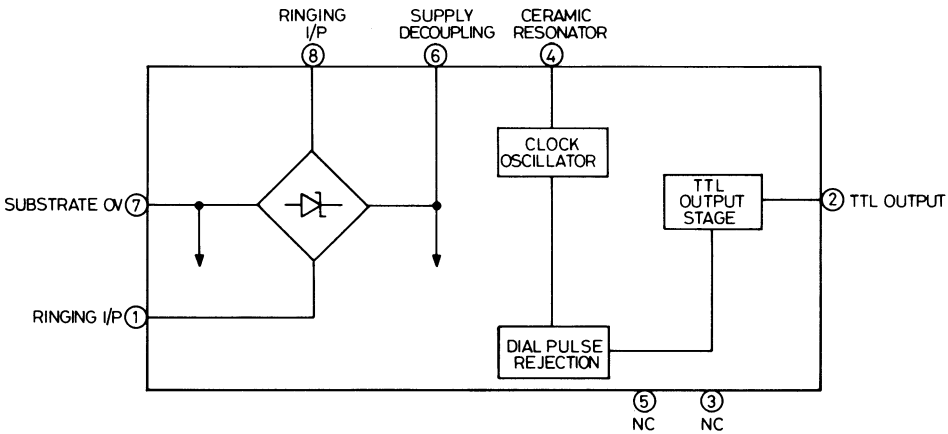


Fig. 1 System Diagram

6878

ABSOLUTE MAXIMUM RATINGS

Ringing input voltage, (V_R)

a) approx. sinusoidal, via 1200Ω, 14-66Hz .. .. $100V_{rms}$

b) distorted sinusoidal, via 100Ω, { 25Hz .. .. $53.7V_{rms}$ } in phase = $60V_{rms}$
{ 75Hz .. .. $29.6V_{rms}$ }

Power dissipation 500mW

Operating temperature .. .. −10°C to +50°C

Storage temperature .. .. −55°C to +125°C

ELECTRICAL CHARACTERISTICS

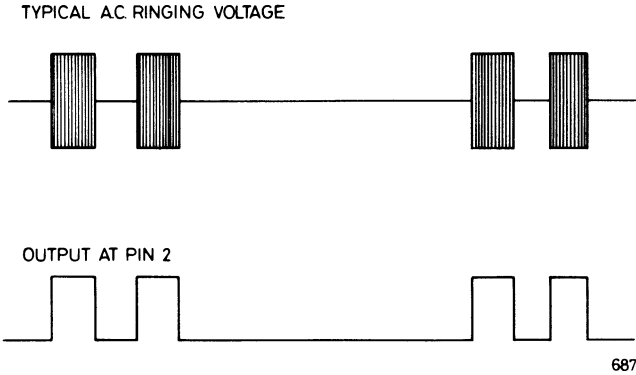
$T_G = 25°C$, $f_C = 560kHz$, $V_R = 75V$, $f_R = 25Hz$ unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
TTL OUTPUT						
Low level output voltage	V_{OL}	–	0.2	0.4	V	$I_{OL} = 3.6mA$
High level output voltage	V_{OH}	2.4	3.3	–	V	$I_{OH} = 200\mu A$
Threshold voltage	V_T	–	9	–	V	
Hysteresis of V_T	V_H	–	2.25	–	V	
Supply current (no load)	I_S		0.25	0.45	mA	$V_S = 20V$ (Note 1)
DIAL PULSE DISCRIMINATOR						
Acceptance frequencies	f_a	14	–	100	Hz	
Rejection frequencies	f_r	0	–	12	Hz	
Small signal standby impedance	Z_{in}	–	100	–	kΩ	$V_R = 1.5V$ $f_r = 1KHz$
Difference between turn-on and turn-off times (Note 2)	t_{diff}			100	mS	

Note 1 V_S = D.C. test voltage applied to Pin 6.

Note 2 The turn-on time is the time between the application of the ringing voltage and the output appearing at Pin 2. Similarly the turn-off time is the time between removal of the ringing voltage and the output turning off.

OPERATING WAVEFORMS



CIRCUIT OPERATION

The operation of the ZN480E is most readily explained with reference to a typical circuit as shown in Fig. 2.

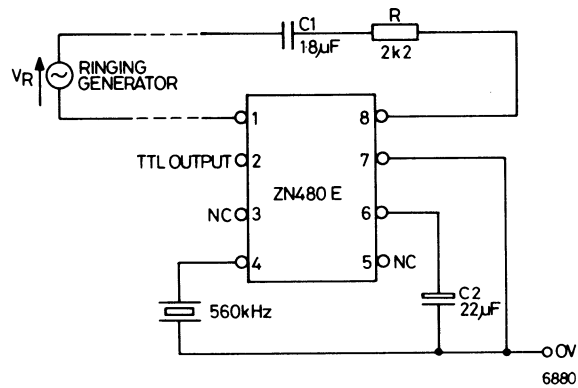


Fig. 2 Typical Circuit - Ring Detector

The incoming ringing voltage from the line, V_R, typically 75 volts 25Hz is connected to pins 1 and 8 via a D.C. blocking capacitor C1, and a current surge limiting resistor R. This applies the ringing voltage to the built-in full wave rectifier bridge and the output is filtered by the reservoir capacitor C2. This smoothed D.C. supply is then used to power up the remaining circuits.

The nominal frequency of the clock oscillator, f_C, is 560kHz. This is divided down to 25Hz i.e. the same frequency as the standard A.C. ringing voltage.

An A.C. voltage appearing on the line causes the voltage across C_2 to rise but the output is inhibited until this voltage exceeds the threshold voltage, V_T, and the dial pulse discriminator has detected the presence of the ringing supply.

The ringing supply frequency is normally between 14 and 66Hz, whereas dial pulses occur at 8 to 12Hz. A digital bandpass filter technique is used to differentiate between the two and inhibit the output when dial pulses are present.

The output from the dial pulse discriminator is used to drive a TTL compatible totem pole output.

LIGHTNING PROTECTION

The I.C. is designed to withstand surges on the line provided a resistor, R in Fig. 2, is connected in series with the ringing input pins.

Using a value of R = 2k2 the device will survive and still operate to specification after a lightning simulation test as defined in Fig. 3.

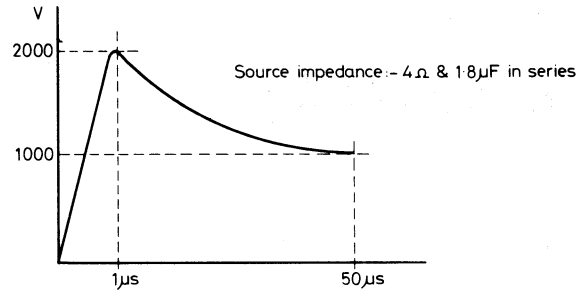
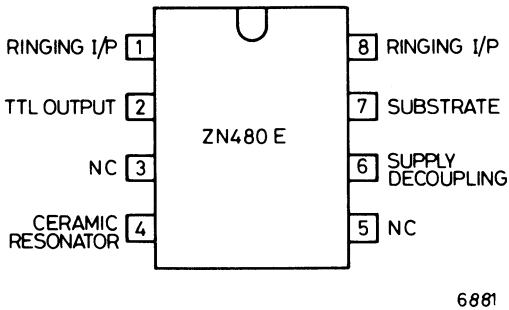
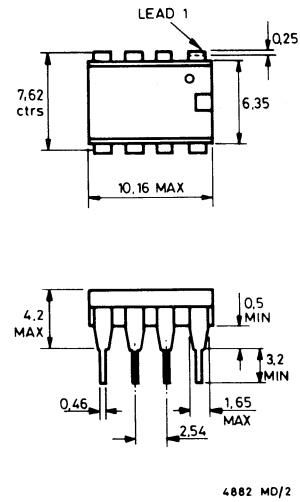


Fig. 3 Lightning Surge Test

PIN CONNECTIONS



PACKAGE OUTLINE



8 Lead Moulded D.I.L.
Dimensions in millimetres

ZN1003

FERRANTI semiconductors

Time Slot Assigner

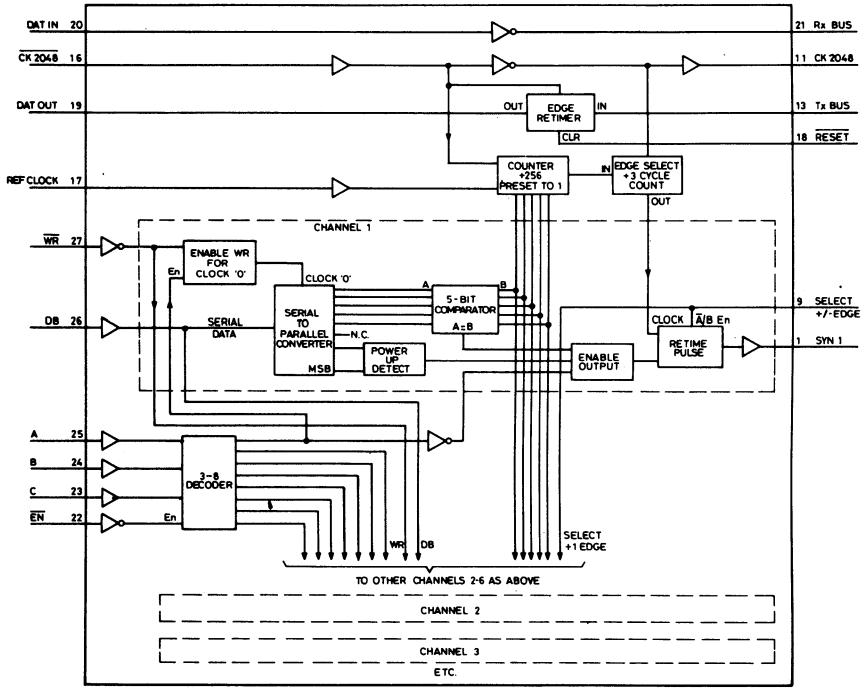
FEATURES

- Dynamic time-slot assignment
- Clock buffering
- DATOUT buffering and retiming
- Direct microprocessor control
- Syn pulse derived from either edge of the 2.048MHz clock

GENERAL DESCRIPTION

The ZN1003 Eight Channel Time-slot Assigner has been designed for use with those single chip codec/filters which do not have a time-slot assignment function built-in. The TSAC operates under the control of the board intelligence and provides synchronous pulses to each of up to eight devices. The synchronising pulses are of 8 clock cycles duration and can be selected to be derived from either the rising or the falling edge of the 2.048MHz clock.

The TSAC will be able to drive the majority of codec/filter devices. Also provided on the chip are waveform buffers and a re-timing circuit for the PCM signals.



System Diagram ZN1003

6901

ABSOLUTE MAXIMUM RATINGS

Supply voltage .. .. +7.0 volts
Operating temperature range .. .. .. 0 to 70°C
Storage temperature range .. .. −55 to +125°C

D.C. CHARACTERISTICS (over operating temperature range V_{CC} = 4.75 to 5.25 volts)

Parameter		Test Conditions	Min.	Typ.	Max.	Units
Supply current				77	113	mA
Low level input voltage	All Inputs		0		0.8	V
Low level input current	All Inputs except Pin 16	V_{IN} = 0V		−0.34	−0.6	mA
	Pin 16	V_{IN} = 0V		−1.0	−1.6	mA
High level input voltage	All Inputs		2.0		V_{CC}	V
High level input current	All Inputs except Pin 16	$V_{IN} = V_{CC}$			10	μA
	Pin 16	$V_{IN} = V_{CC}$			20	μA
Low level output voltage	All Outputs	I_{OL} = 8mA			0.5	V
High level output voltage	All Outputs	I_{OH} = 400μA	2.4			V

FUNCTIONAL DESCRIPTION

Time-slot Assignment Operation

This is the main area of the chip and can be regarded as eight separate channels 1-8, port select area, time count area and +/− select.

The basic function of a channel is to convert the serial data information on DB, from the card controller into a positive pulse at the syn 'n' output pin at a fixed time relative to an externally provided control pulse. When a channel is not active no pulse is produced at the associated syn output.

PORT SELECT

One of eight ports is selected using binary coded information presented to the ZN1003 on input lines A, B and C. The code is valid when $\overline{EN}$ is low. During the period when $\overline{EN}$ is low, eight bits of serial data on DB containing time-slot and power up/down information are clocked into the selected ports serial to parallel converter under the control of the $\overline{WR}$ signal. (SEE TABLES 1, 2, and 3).

Table 1 Port Select

A	B	C	$\overline{EN}$	Syn 1	Syn 2	Syn 3	Syn 4	Syn 5	Syn 6	Syn 7	Syn 8
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Control Word

P2	P1	N.U.	T5	T4	T3	T2	T1

MSB LSB

N.U. = Not used

Table 2 Time Slot Selection

T5	T4	T3	T2	T1	Time Slot
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
1	1	1	1	1	31

Table 3 Power Up/Down Selection

P2	P1	Status
0	0	Power Up
0	1	Power Down
1	0	Power Down
1	1	Power Down

TIME COUNT

$\overline{\text{REF CLOCK}}$ resets a synchronous counter to +1, clocked at 2.048MHz the counter will give a count of 256 before the next reset pulse. Outputs are taken so as to give 32 period counts of 8 cycles of 2.048MHz. i.e. one for each timeslot.

SELECT +/− EDGE

The syn 'n' output is the frame syn pulse for the Codec/filter devices. PCM is coded/decoded relative to this pulse and the 2.048KHz clock. Some manufacturers require the frame syn pulse to be relative to the rising edge, others to the falling edge of the 2.048KHz clock. Applying a positive condition to the select pin enables the frame syn pulse to be driven from the rising edge, an earth on the select pin, from the falling edge.

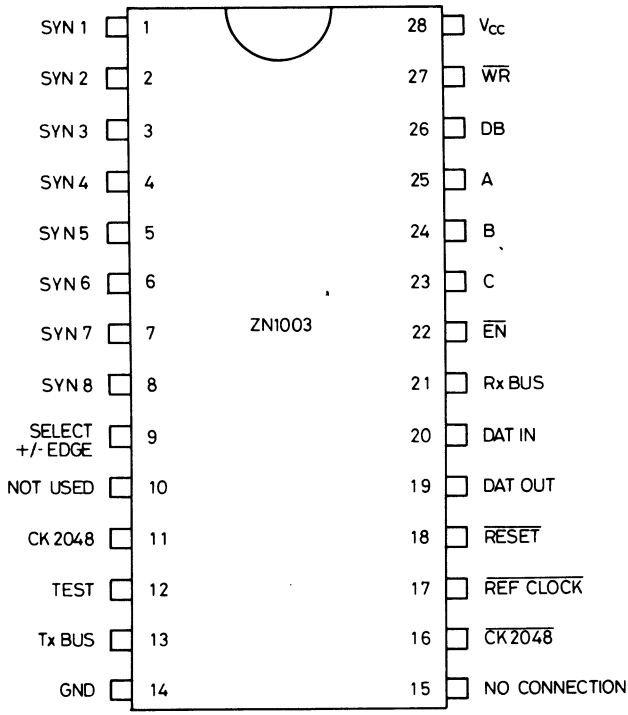
CLOCK BUFFERING

The 2.048MHz clock required to drive the codec/filter chips is derived from the $\overline{2.048\text{MHz}}$ clock used by the ZN1003 thus inversion and buffering is provided on chip.

DATOUT BUFFERING AND RETIMING

Datout is buffered by the ZN1003 and retimed by $\overline{2048}$ clock to ensure correct phase relationship on the output.

Pin Connections



6902

ZN1003

Pin Description

No.	Name	Function
25 24 23	A B C	Parallel data on these three pins is the address of the 8 ports.
22	$\overline{EN}$	Enabling pulse for the selected port address on the A, B and C pins held low while 8 $\overline{WR}$ pulses input 8 bits of serially encoded data into the ZN1003.
26	DB	8 bit serially encoded data derived from the binary representation of the selected timeslot for a particular port, plus, two bits to represent power up/power down.
27	$\overline{WR}$	Write pulse for DB. DB is read into the ZN1003 on the rising edges of the $\overline{WR}$ pulses.
18	$\overline{RESET}$	Upon receipt of logic '0' on this I/P pin, the ZN1003 will reset all timeslots to zero.
9	+/−SELECT	A +ve 5V or ground applied at this pin selects whether the syn output is derived from the rising edge of the 2048 clock or the falling edge.
19	DATOUT	Speech data highway for data from the codec/filter chip to the line unit edge connector, after edge retiming of the Tx BUS on the ZN1003.
20	DATIN	Speech data highway for the data from the line unit edge connector to the codec/filter chip via the ZN1003. After buffering and inversion becomes Rx BUS.
13	Tx BUS	PCM data from the codec/filter chip to the ZN1003.
21	Rx BUS	PCM data from the ZN1003 to the codec/filter chip.
17	$\overline{REF\ CLOCK}$	Timing signal of approximately 1 cycle of the 2048kHz clock in duration, repetition rate of 8kHz. Used as the framing signal for the ZN1003. It is synchronised to the 2048kHz clock.
16	$\overline{CK2048}$	Master clock for the system used for timing on the ZN1003
11	CK2048	Inverted master clock $\overline{2048}$, used for timing of the codec/filter chip etc. outgoing from the ZN1003 to the codec/filter chip.
1 to 8	Syn 1 to Syn 8	Frame syn pulse, a positive pulse of 8 periods of the 2048 clock for each individual codec/filter chip generated by the ZN1003 in a selected timeslot, referenced to the 2048 and REF CLOCK signals.

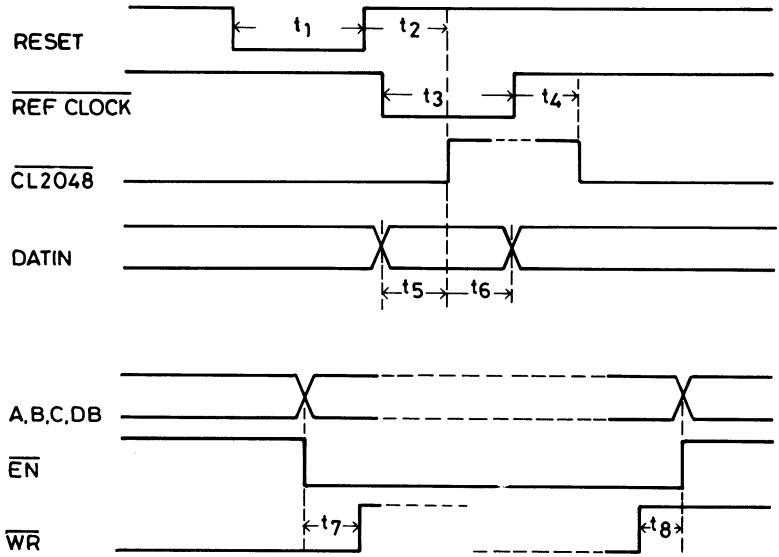
Input Timing Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units
t_1	Reset pulse width	50			nS
t_2	Delay from rising edge reset pulse to rising edge of $\overline{CK2048}$	25			nS
t_3	Reference clock pulse width	100			nS
t_4	Delay from rising edge reference clock to falling edge of $\overline{CK2048}$	50			nS
t_5	Delay from DATIN to rising edge of $\overline{CK2048}$	60			nS
t_6	Delay from rising edge of $\overline{CK2048}$ to DATIN	50			nS
t_7	Delay from A,B,C, and DB to the write pulse	70			nS
t_8	Delay from rising edge write pulse to A,B,C, and DB	100			nS

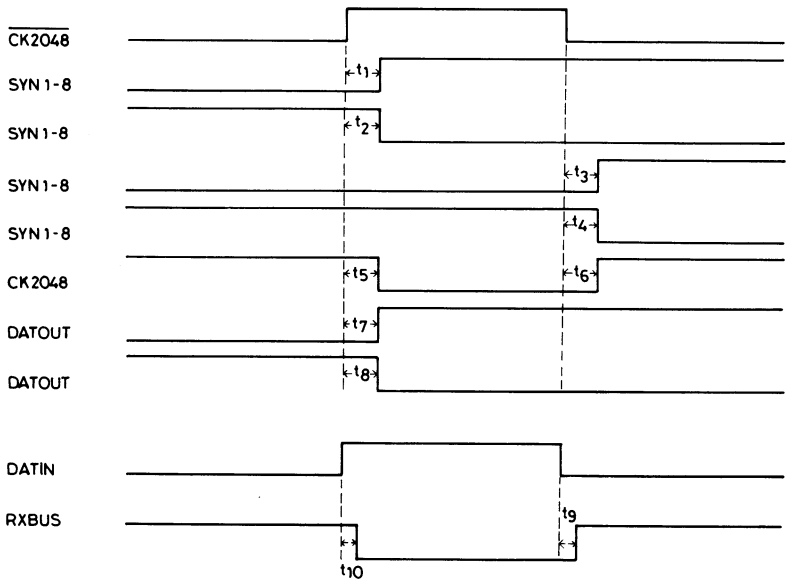
Output Timing Requirements

Symbol	Parameter	Min.	Typ.	Max.	Units
t_1	Syn out rising edge delay from rising edge $\overline{CK2048}$. $C_L = 300pf$	60	100	170	nS
t_2	Syn out falling edge delay from rising edge $\overline{CK2048}$. $C_L = 30pF$	60	100	170	nS
t_3	Syn out rising edge delay from falling edge $\overline{CK2048}$. $C_L = 30pF$	60	100	170	nS
t_4	Syn out falling edge delay from falling edge $\overline{CK2048}$. $C_L = 30pF$	60	100	170	nS
t_5	Delay from rising edge $\overline{CK2048}$ to falling edge CK2048. $C_L = 480pF$	22	31	53	nS
t_6	Delay from falling edge $\overline{CK2048}$ to rising edge CK2048. $C_L = 480pF$	25	36	61	nS
t_7	Delay from rising edge $\overline{CK2048}$ to rising edge DATOUT	35	51	90	nS
t_8	Delay from rising edge $\overline{CK2048}$ to falling edge DATOUT	30	42	75	nS
t_9	Delay from rising edge DATIN to falling edge R_X bus	22	32	55	nS
t_{10}	Delay from falling edge DATIN to rising edge R_X bus	20	29	50	nS
	DATOUT delay from falling edge $\overline{CK2048}$. $C_L = 120pF$	30		106	nS
	$\overline{CK2048}$ rise time or fall time			50	nS

C_L = Load Capacitance

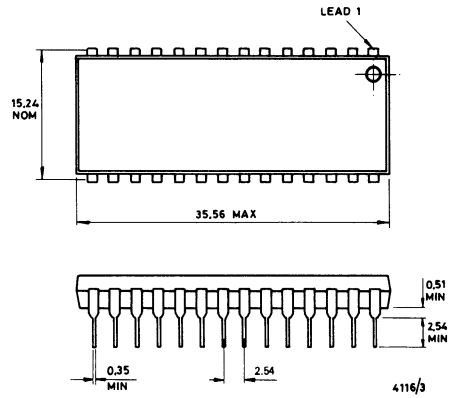


Input Timing Requirements



Output Timing Requirements

Package Details



28 Lead Moulded D.I.L.

Dimensions in millimetres

5. Industrial

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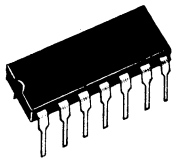
FERRANTI semiconductors

ZN409CE

Precision Servo Integrated Circuit

FEATURES

- Low External Component Count
- Low Quiescent Current (7 mA typical at 4.8V)
- Excellent Voltage and Temperature Stability
- High Output Drive Capability
- Consistent and Repeatable Performance
- Precision Internal Voltage Stabilisation
- Time Shared Error Pulse Expansion
- Balanced Deadband Control
- Schmitt Trigger Input Shaping
- Reversing Relay Output (D.C. Motor Speed Control)



14 lead D.I.L.

DESCRIPTION

The ZN409CE is a precision monolithic integrated circuit designed particularly for pulse-width position servo mechanisms used in all types of control applications. The low number of components required with the ZN409CE, together with its low power consumption, make this integrated circuit ideal for use in model aircraft, boats and cars where space, weight and battery life are at a premium. The amplifier will operate over a wide range of repetition rates and pulse widths and is therefore suitable for the majority of systems. The ZN409CE can also be used in motor speed control circuits.

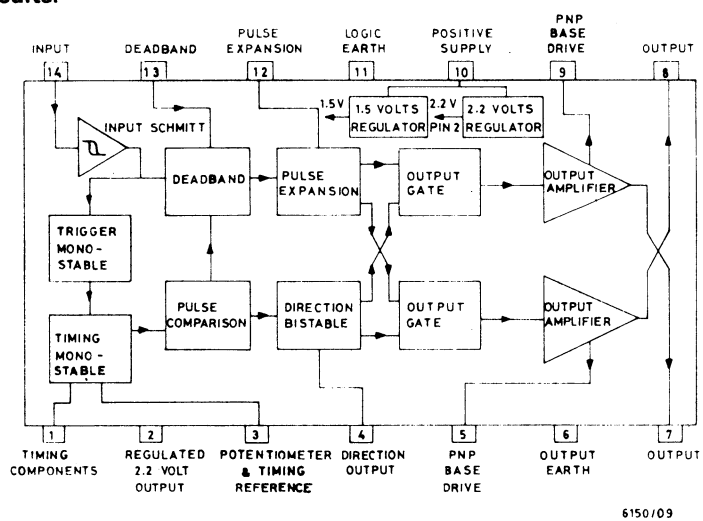


Fig. 1. SYSTEM DIAGRAM

ZN409CE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .. .. 6.5 Volts
Package Dissipation .. .. .. 300 Milliwatts
Operating Temperature Range .. .. −20°C to +65°C
Storage Temperature Range .. .. −65°C to +150°C

CHARACTERISTICS (V_S = 5V. At 25°C ambient temperature unless otherwise stated).

Parameter	Min.	Typ.	Max.	Unit	Conditions
Input threshold (lower)	1.15	1.25	1.35	V	Pin 14
Input threshold (upper)	1.4	1.5	1.6	V	Pin 14
Ratio upper/lower threshold	1:1	1:2	1:3		−10 to +65°C
Input resistance	20	27	35	kΩ	
Input current	350	500	650	μA	
Regulator voltage	2.1	2.2	2.3	V	−10 to +65°C, 1.3 mA load current
Regulator supply rejection ratio	200	300	—		V_S = 3.5 to 6.5V $RSRR = \frac{dV_{in}}{dV_{out}}$
Monostable linearity	—	3.5	4.0	%	±45°, R_p = 1.5 kΩ R_1 = 12 kΩ
Monostable period temperature coefficient	—	+0.01	—	%/°C	Excluding R_T, C_T. R_p = 1.5 kΩ, R_1 = 12 kΩ (potentiometer slider set mid-way)
Output Schmitt deadband	±1	±1.5	±3	μs	C_E = 0.47 μF
Minimum output pulse	2.5	3.5	4.5	ms	C_E = 0.47 μF, R_E = 180 kΩ
Error pulse for full drive	70	100	130	μs	15 ms repetition rate C_E = 0.47 μF, R_E = 180 kΩ
Total deadband	±3.5	±5	±6.5	μs	C_D = 1000 pF
P.N.P. drive	40 35	55 50	70 65	mA mA	T = 25°C T = −10°C
Output saturation voltage	—	300	400	mV	I_L = 400 mA
Direction bistable output	2	2.8	3.6	mA	
Supply voltage range	3.5	5	6.5	V	
Supply current	4.6	6.7	10	mA	Quiescent
Total external current from regulator	1.3	—	—	mA	V_S = 3.5V
Peak voltage $V_{C\ EXT}$ (with respect to 2V regulated voltage)	— —	0.7 0.5	— —	V V	T = 25°C T = −10°C

OPERATING AND DESIGN NOTES

1. SERVO APPLICATION

Component Function	Circuit Reference	Value	Comments
Monostable Timing Components	R_T	100 kΩ	Note 1(e)
	C_T	0.1 μF	
Potentiometer and Timing Reference Components	R_p	1.5 kΩ	Note 1(e)
		5 kΩ	Note 1(g)
	R_1	4.7 kΩ	Note 1(e)
Pulse Expansion	CE	0.47 μF	Note 1(d)
	RE	180 kΩ	11Ω Motor
		150 kΩ	8Ω Motor
Deadband (Note 1(c))	C_D	1000 pF	11Ω Motor
		1500 pF	8Ω Motor
Dynamic Feedback	R_F	330 kΩ	Note 1(f)
	R_B	330 kΩ	
	R_2	1.2 kΩ	
Input Coupling	C_C	2.2 μF	Note 1(b)
Motor Decoupling	C_2	0.01 μF	
	C_3	0.01 μF	
R.F. Decoupling	C_1	0.1 μF	Note 1(h)
Drive Transistors	T1, T2		Note 1(i)

(a) Introduction

In the standard servo application the displacement of a control stick varies the pulse width of a timing circuit and many such pulses are time division multiplexed and typically modulate a 27 MHz transmitter. A receiver then decodes the transmitted signal and reconstitutes an independent train of pulses for each servo channel. The servo shown in Fig. 2 consists of the ZN409CE integrated circuit, several external components, a power amplifier consisting of two external PNP transistors and two on-chip NPN transistors which form a bridge circuit to drive the d.c. motor. The motor drives a reduction gear box which has a potentiometer attached to the output shaft. This potentiometer in association with R_1 and the timing components C_T and R_T controls the pulse width of the

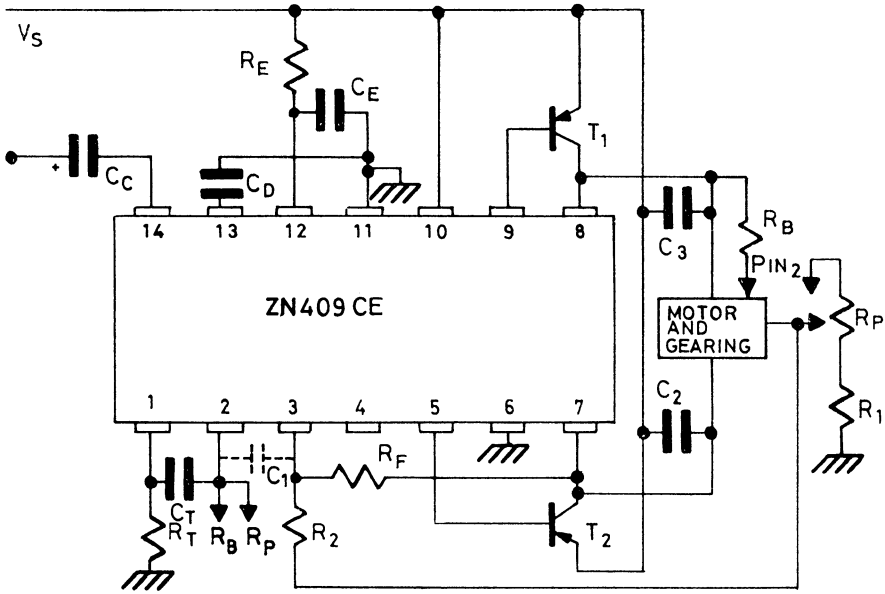
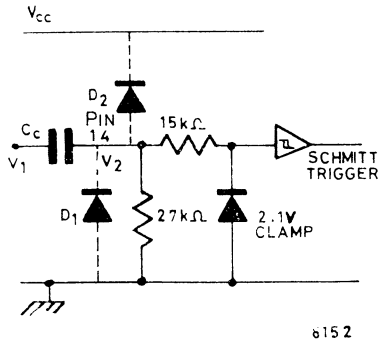


Fig. 2. SERVO SYSTEM USING THE ZN409CE

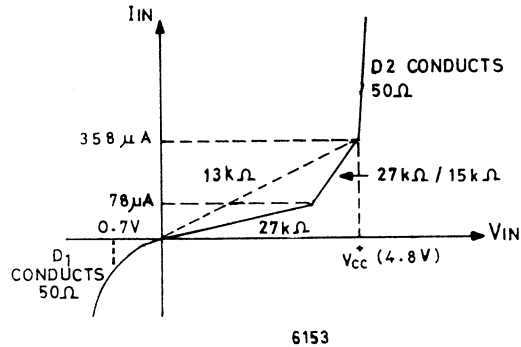
timing monostable. The input pulse is compared with the monostable pulse in a comparison circuit and one output is used to enable the correct phase of an on-chip power amplifier. The other output from the pulse comparison circuit drives the pulse expansion circuit (C_E, R_E) via the deadband circuit (C_D). Thus any difference between the input and monostable pulses is expanded and used to drive the motor in such a direction as to reduce this difference so that the servo takes up a position which corresponds to the position of the control stick.

(b) Input Circuit

The ZN409CE operates with positive going input pulses which can be coupled either directly or via a capacitor to pin 14. The advantage of a.c. coupling is that should a fault occur in the multiplex decoder which causes the input signal to become a continuous positive level, the servo will remain in its last quiescent position, whereas with direct coupling the servo output arm will rotate continuously. A nominal 27 kΩ resistor is shunted across the input on chip to provide d.c. restoration of the input signal when a.c. coupling is used. The active input circuit is a Schmitt trigger which allows the servo to operate consistently with slow input edges and supplies the fast edge required by the trigger monostable independent of input edge speed.



INPUT CIRCUIT



INPUT CHARACTERISTICS

Fig. 3.

The input circuit and its V/I characteristic are shown above. D_1 and D_2 are the parasitic substrate and isolation diodes associated with the input resistors. It is advisable that the pulse input amplitude should not fall below 0V nor exceed the supply voltage V_{CC} in order to prevent these diodes from conducting, although a small amount of conduction will not cause the circuit to malfunction. When a.c. coupling is used the value of C_C should be chosen to give a pulse droop not exceeding 0.3 volts

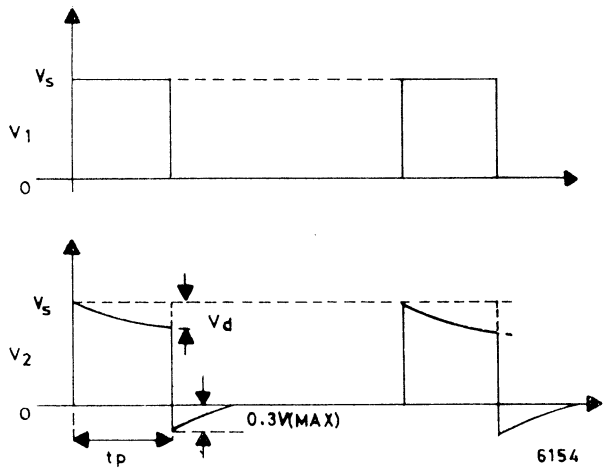


Fig. 4. INPUT WAVEFORMS

Assuming that the input signal swings between 0V and V_s and taking the input chord resistance R_{in} of 13 kΩ, the droop for a pulse of duration t_p msec will be:

$$v_d = \frac{V_s\, t_p}{C_C \cdot R_{in}} \text{ volts} \qquad \begin{matrix} t_p \text{ (msec)} \\ C_C \text{ (μF)} \\ R_{in} \text{ (kΩ)} \end{matrix}$$

For a nominal pulse width of 1.5 msec and v_d equal to 0.3 volts the required minimum value of C_C can be found as follows:

$$C_C = \frac{4.8 \;.\; 1.5}{0.3 \;.\; 13} = 1.85\ \mu F$$

A nominal value of 2.2 μF is chosen (Nearest preferred value).

If it is required to operate the servo with reduced input pulse amplitude the input pulse should exceed the upper Schmitt threshold voltage of 1.5 volts by a reasonable margin and a minimum input pulse amplitude of 2.4 volts is recommended.

(c) Deadband Circuit

The function of the deadband circuit is to provide a small range of output shaft position about the quiescent position where the difference pulse does not drive the motor. This is necessary to eliminate hunting around the quiescent position caused by servo inertia and overshoot. The minimum deadband required is also a function of the pulse expansion characteristics and dynamic feedback component values.

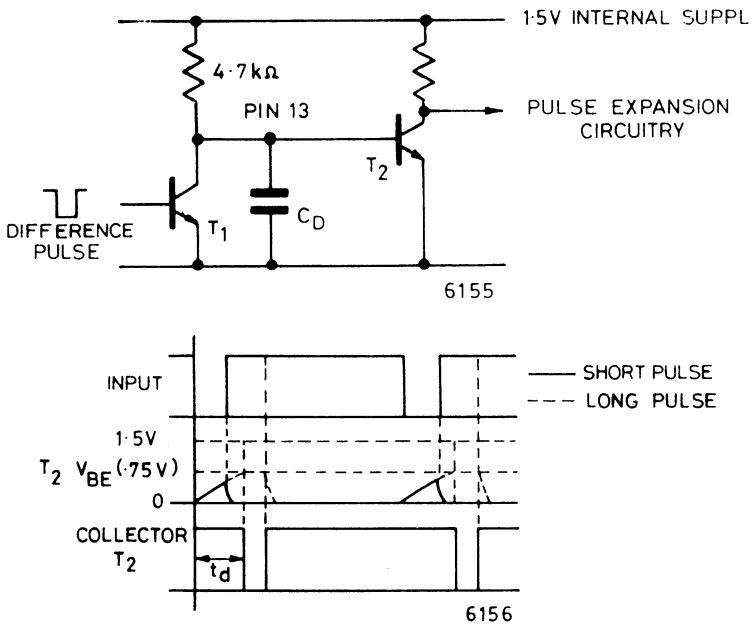


Fig. 5. DEADBAND CIRCUIT AND WAVEFORMS

When the difference pulse is applied T_1 turns off and the base of T_2 rises on an exponential waveform with a time constant of 4.7 kΩ × C_D. If the difference pulse is small the potential reached on the base of T_2 is insufficient to turn T_2 on and no output results.

The pulse expansion circuit has a built in deadband of 1.5 μsec with C_E = 0.47 μF and this must be added to the deadband caused by C_D to obtain the total T_d.

$$\therefore \quad T_d = 1.5 + t_d \ \mu\text{sec}$$

t_d is found from the exponential equation.

$$V_{be} = V_1 \left[1 - \exp\left(\frac{-t_d}{C_D \ . \ 4.7\ k\Omega}\right)\right]$$

$$\therefore \quad t_d = C_D . \ 4.7 \log_e \left(\frac{V_1}{V_1 - V_{be}}\right)$$

$$\therefore \quad = 3.3\ C_D \ \mu\text{sec} \ (C_D \text{ in nF})$$

(Taking V_1 = 1.5 volts and V_{be} = 0.75 volts)

Thus with C_D equal to 1000 pF (1 nF) t_d = 3.3 μsec and T_d = 4.8 μsec.

The mechanical deadband Ød depends on the chosen sensitivity S_1 of the servo and in the usual radio control application a ±500 μsec input pulse variation causes ±50° rotation, i.e. S_1 = 10 μsec per degree.

Thus $\text{Ød} = \dfrac{2.T_d}{S_1}$ degrees (T_d in μsec. S_1 in μsec per degree).

Thus a value for T_d of 5 μsec provides a mechanical deadband Ød of 1°.

And generally:

$$\text{Ød} = \frac{2.\ (1.5 + t_d)}{S_1}$$

$$\text{Ød} = \frac{3 + 6.6\ C_D}{S_1} \text{ degrees} \quad \begin{cases} C_D \text{ in nF.} \\ S_1 \text{ in μsec per degree.} \end{cases}$$

(d) Pulse Expansion

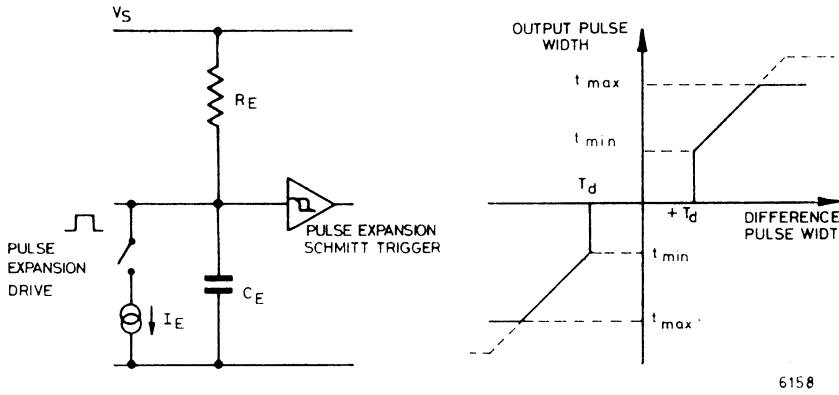


Fig. 6. PULSE EXPANSION CIRCUIT AND CHARACTERISTIC

A schematic of the pulse expansion circuit is shown in Fig. 6. In the quiescent state with no drive the Schmitt trigger input is biased via R_E and takes up a level just above the lower threshold V_L.

A drive pulse causes a current I_E to be switched on for the duration of the pulse and this discharges C_E linearly with time. Thus, at the end of the pulse the voltage on C_E depends on the duration of the pulse. If the pulse is narrow and just causes the potential on C_E to fall to V_L the Schmitt trigger will switch to the upper threshold V_H and at the end of the drive pulse C_E will start to charge to V_H with a time constant C_ER_E. When the potential on C_E reaches V_H the Schmitt will switch to V_L and C_E will discharge to the quiescent level. The output drive is taken from the Schmitt output.

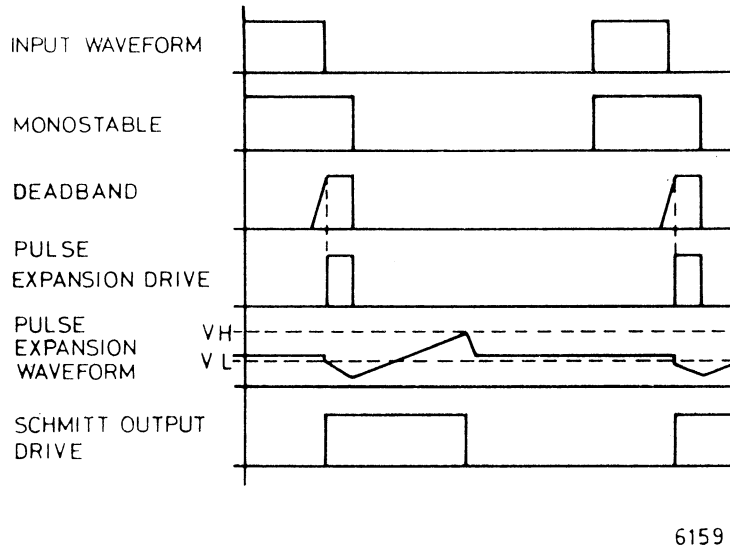


Fig. 7. PULSE EXPANSION TIMING DIAGRAM

D.C. motors need a certain amount of drive to overcome static friction and the minimum output pulse obtained from this form of pulse expansion characteristic is chosen to ensure that the motor will rotate when driven. A linear initial pulse expansion characteristic would result in the motor remaining stationary and drawing full stall current for small drive periods. If the motor needs 2 msec of drive at a repetition rate of 20 msec to cause rotation, this is equivalent to an average drain of 50 mA for a 0.5A stall current. This is many times more than the quiescent current of the ZN409CE (7 mA) and could considerably reduce flying time for the standard battery operated airborne multichannel radio control system. This effect also causes an annoying buzz from the motor and gearbox. The use of the Schmitt trigger removes these two deficiencies.

The value of t_{min} is determined by the Schmitt trigger hysteresis and the exponential waveform on C_E in the following equation.

$$V_H = (V_{CC} - V_L)\left(1 - \exp\left[\frac{-t_{min}}{C_E R_E}\right]\right)$$

because V_H is small the following linear relationship is sufficiently accurate.

$$V_H = \frac{(V_{CC} - V_L)}{C_E R_E} . t_{min}$$

$$\therefore \quad t_{min} = \frac{V_H}{(V_{CC} - V_L)} . C_E R_E \text{ msec}$$

For nominal operation $V_{CC} = 4.8V$; $V_L = 1.5V$; $V_H = 0.12V$ and:

$$t_{min} \simeq \frac{C_E R_E}{30} \text{ msec} \qquad \begin{cases} C_E \text{ in } \mu F \\ R_E \text{ in } k\Omega \end{cases}$$

and for $C_E = 0.47\ \mu F$ and $R_E = 180\ k\Omega$, $t_{min} = 3.5$ msec.

It can be seen from the simple equation that t_{min} is dependent on V_{CC}, and t_{min} will increase with reducing V_{CC}. This variation is put to good use to maintain the initial motor drive, $V_{CC} \times t_{min}$ reasonably constant over the operating voltage range of 3.5 to 6.5 volts.

When the pulse expansion drive is increased above the minimum value the output pulse increases from t_{min} almost linearly until full pulse expansion is reached, i.e. when the output pulse width equals the input pulse repetition rate. The pulse expansion will be almost linear provided that the current source I_E does not saturate, i.e. provided that C_E is not discharged to almost zero volts. Ideally the current source should saturate when full motor drive is obtained but due to component tolerances it is usual to allow some margin to ensure that full motor drive can be obtained. If a margin is allowed, an extended pulse expansion characteristic results (shown dotted in Fig. 6) and if this is excessive it can lead to the servo exhibiting an underdamped characteristic causing jittering or hunting. Thus for full pulse expansion the voltage on C_E should discharge from its quiescent value of 1.5V to 0.75 volts. Thus with $I_E = 3$ mA for the current source:

$$\frac{1.5 - 0.75}{t_e} = \frac{I_E}{C_E}$$

$$\therefore \quad C_E = 4.\ t_e\ \mu F \ (t_e \text{ in msec})$$

For $t_e = 0.1$ msec, a value of 0.47 μF was chosen for C_E.

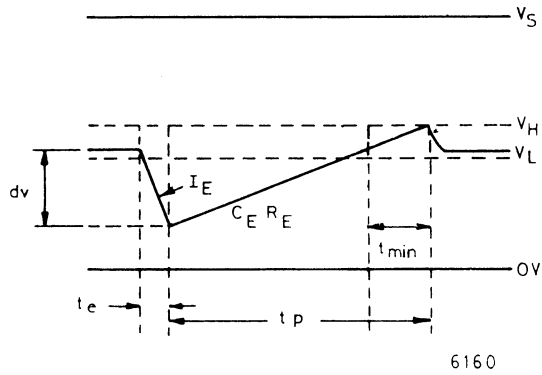


Fig. 8. PULSE EXPANSION WAVEFORM

If t_p is the maximum motor drive pulse length required, i.e. equal to the input pulse repetition period for full pulse expansion, and the mean value of the potential on C_E is taken as 1.2 volts, then :

$$dv = \frac{(t_p - t_{min})}{C_E R_E}. \quad (V_{CC} - 1.2)$$

And for the discharge period t_e :

$$dv = \frac{I_E . t_e}{C_E}$$

$$\therefore \quad R_E = \frac{(t_p - t_{min})}{I_E t_e}. \quad (V_{CC} - 1.2)$$

For nominal values of $V_{CC} = 4.8V$ and $I_E = 3$ mA

$$R_E = 1.2 \frac{(t_p - t_{min})}{t_e} \text{ k}\Omega$$

and for $t_p = 20$ msec, $t_{min} = 3.5$ msec, $t_e = 0.1$ msec, $R_E = 180$ kΩ (Nearest preferred value).

(e) Monostable Timing

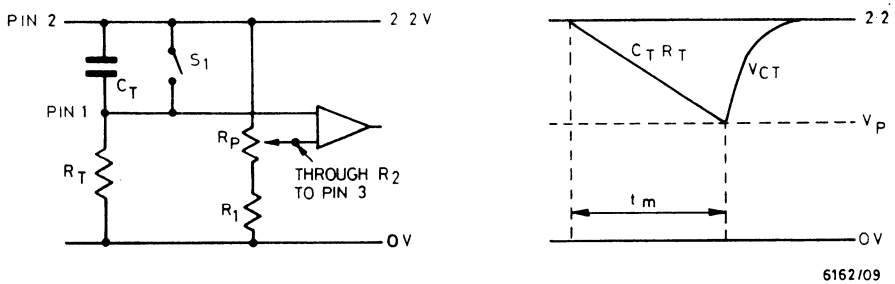


Fig. 9. MONOSTABLE TIMING CIRCUIT AND WAVEFORM

The leading edge of the input waveform triggers the timing monostable by opening switch S_1. C_T then charges until the differential amplifier detects that the timing waveform potential has fallen to V_p, the potential on the potentiometer wiper and switch S_1 is closed to terminate the timing pulse. Thus the monostable period is determined by the setting of the potentiometer wiper. In the standard application the servo centre position pulse width is 1.5 msec with a range of ±50° rotation at 10 μsec per degree. Thus the 2.0 msec maximum monostable period $t_{mono(max)}$ corresponds to a potentiometer setting of 200° (for a linear relationship) and since the potentiometer has a total rotation of approximately 270° and the maximum allowable swing on pin 3 is specified as 0.5 volt, the value of C_TR_T can be calculated as follows:

$$\frac{0.5}{t_{mono(max)}} \simeq \frac{2}{C_TR_T}$$

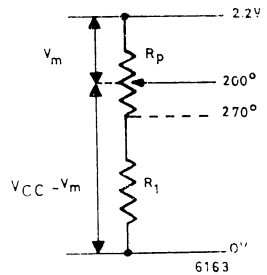
$$C_TR_T = 4.\ t_{mono(max)}$$

Thus if $t_{mono(max)} = 2$ msec, $C_TR_T = 8$ msec.

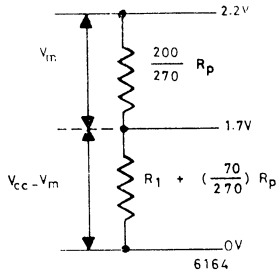
The optimum value of R_T is 100 kΩ due to the design of the on-chip monostable circuit, giving $C_T = 0.1$ μF (nearest preferred value).

$$R_T = 100\ k\Omega \qquad C_T = 0.1\ \mu F$$

The value of R_1 can now be calculated from the actual voltage swing with a potentiometer setting of Øp = 200° and Ømax = 270°.



POTENTIOMETER SET AT 200°



EQUIVALENT CIRCUIT

Fig. 10

Thus from the equivalent circuit

$$\frac{V_m}{\frac{200}{270}.\ R_p} = \frac{(V_{CC} - V_m)}{R_1 + \frac{70}{270} R_p}$$

where V_m is calculated from the actual values of C_T and R_T chosen using the relationship

$$V_m = \frac{2.0\ .\ t_{mono(max)}}{C_TR_T}$$

since $C_T = 0.1$ μF (nearest preferred value) was chosen with $R_T = 100$ kΩ, $V_m = 0.4$V and hence

$$R_1 = 3.1\ R_p$$

If $R_p = 1.5$ kΩ then $R_1 = 4.7$ kΩ.

(f) Dynamic Feedback

Without dynamic feedback in the standard application the inertia of the motor and gearbox causes the servo output shaft to overshoot the set position which results in the servo 'hunting'. If the deadband was widened to stop this effect an unacceptably large deadband would result and the servo would still be underdamped. The dynamic feedback circuit utilises the motor back emf (which is proportional to motor speed) and feeds back a proportion of this signal to the wiper of the potentiometer. The phase of the feedback signal is chosen to modify the potential on the wiper so that the monostable period is dynamically varied to reduce the motor drive as the servo output shaft approaches the set position and the values of the feedback resistors are chosen to achieve optimum settling characteristics.

The value for R_F and R_B of 330 kΩ will suit the normal type of servo mechanism, however if the servo is fairly fast this can be decreased to 300 kΩ to minimise any tendency to overshoot. Where the servo is slow R_F and R_B can be increased to 360 kΩ or 390 kΩ.

(g) Alternative Value of R_p

Although a 1.5 kΩ feedback potentiometer is the most common value of R_p, 5 kΩ potentiometers are used in some servo mechanisms. In order to use this value with the ZN409CE a 2.2 kΩ resistor is usually connected across the potentiometer to maintain the values of R_F and R_B at 330 kΩ and R_1 at 4.7 kΩ. R_2 is omitted. i.e. the wiper of the potentiometer is connected directly to Pin 3 of the ZN409CE.

(h) R.F. Decoupling

C_1 (typical value 0.1 μF) is only necessary where strong R.F. fields may affect the operation of the circuit.

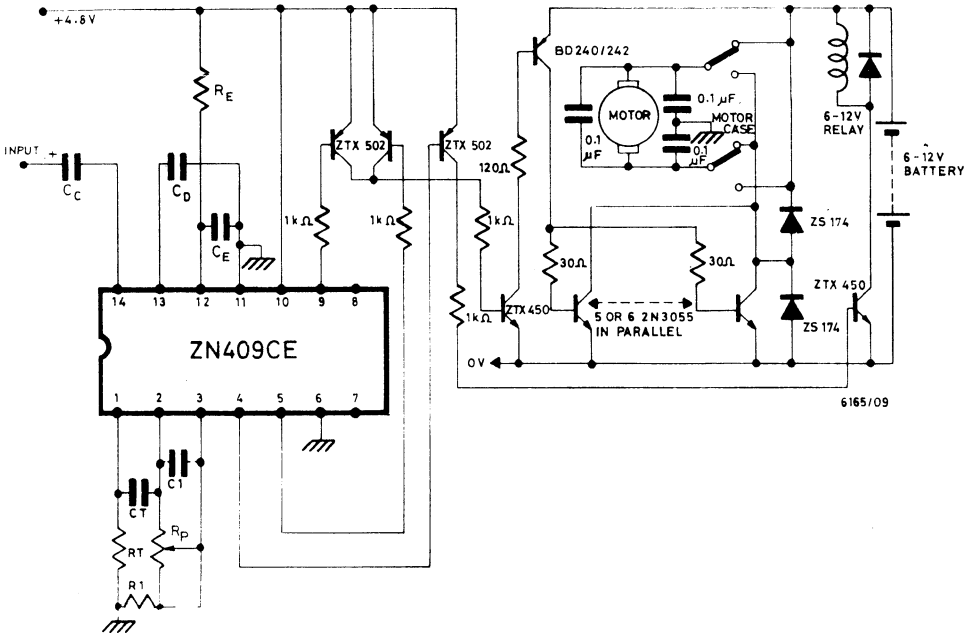
(i) Transistors T1 and T2

The external PNP transistors are usually selected for a low $V_{CE(sat)}$ to obtain maximum output drive and the recommended types are the ZTX550 or ZTX750.

2. MOTOR SPEED CONTROL

(a) Introduction

In the motor speed control application the ZN409CE is used as a linear pulse width amplifier. The d.c. motor is driven via a power amplifier with a train of pulses whose mark/space ratio can vary between zero and one to control the motor speed from zero to maximum. The ZN409CE operates



Component Function	Circuit Reference	Value
Monostable timing components	R_T	100 kΩ
	C_T	0.1 μF
Potentiometer and timing reference components	R_P	1 kΩ
	R_1	4.7 kΩ
Pulse expansion	R_E	82 kΩ
	C_E	1 μF
Deadband	C_D	0.022 μF
Input coupling	C_C	2.2 μF
Motor decoupling. See note 1(h)	C_1	0.01 μF

Fig. 11. HIGH PERFORMANCE PROPORTIONAL MOTOR SPEED CONTROL CIRCUIT AND RECOMMENDED COMPONENT VALUES

with fixed timing components and a fixed resistor replaces the position feedback potentiometer. The nominal monostable period represents zero motor speed and input pulses less than or greater than nominal drive the motor in the forward and reverse direction respectively. The motor direction is usually controlled by a relay operated from pin 4, the direction output. Pulse expansion components C_E and R_E are chosen to obtain the required relation between control stick deplacement and motor speed and it is usual to operate with a much larger deadband than that used in the servo application.

Because high current motors are used to drive the wheels or propellors of model cars or boats a separate supply of 6 to 12 volts is used, and to provide reasonable running time between recharging the battery, a capacity of 1.2 Amp. hr. is usual.

$^1/_{12}$ scale cars with reasonable performance can be powered by a 5 amp stall current motor such as the 'Marx Monoperm' (6 – 12 volts) driven from a single 2N3055 power transistor. However, if very high performance is required then five or six 2N3055 power transistors are used in parallel as shown in Fig. 11 to drive a 25 amp stall current motor. The 'Mabuchi RS54' operates from 6 to 8 volts and will provide a top speed of about 25 mph in a $^1/_8$ scale car. Acceleration is superb and the car wheels can be spun easily even on the best surfaces although the 1.2 amp hr. battery will need a full recharge after some ten minutes of racing. The motor and 2N3055 transistors dissipate a great deal of power especially at low speed and almost full stall current drive so the power transistors need to be mounted on a good heat sink such as the aluminium chassis of the car and a motor with crimped commutator connections rather than soldered connections is necessary since soldered connections have been seen to melt under stall conditions.

The outputs from pins 9 and 5 of the ZN409CE integrated circuit are combined using two ZTX502 PNP transistors to provide a pulsed output whose mark/space ratio varies from 0 to 1 depending on the deflection of the control stick.

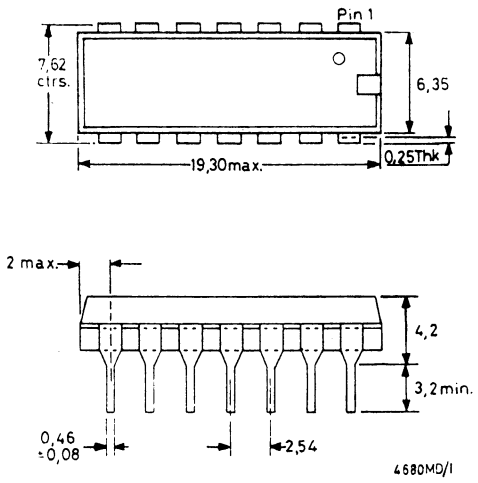
This signal is then used to drive the motor via the power amplifier.

The ZN409CE has additional circuitry which performs the motor reversing function by taking the output from the direction bistable and provides either zero current or approximately 3 mA sink current at pin 4, depending on the state of the direction bistable. This current is amplified and used to drive the relay coil (100 mA) via the ZTX450 transistor thus controlling the motor direction via the relay changeover contacts.

It is usual to have a relatively wide deadband and $C_D = 0.022\ \mu F$ provides a deadband of about 14% (± 7 degrees).

The pulse expansion components C_E and R_E are chosen to give full motor drive at about 90% full stick displacement and using the formulae derived earlier yields values of $C_E = 1\ \mu F$, $R_E = 82\ k\Omega$. The monostable timing component values remain unchanged at $C_T = 0.1\ \mu F$, $R_T = 100\ k\Omega$. A 1 kΩ potentiometer (R_p) can be used to set up the zero output condition with the control stick in its central position.

PACKAGE OUTLINE



14 Lead Moulded D.I.L.

Dimensions in millimetres

ZN411

FERRANTI semiconductors

Motor Speed Controller

FEATURES

- Direct Supply from a.c. mains or d.c. power source
- On Chip Shunt Regulator
- Low External Component Count
- Soft start Ramp Circuit
- Circuit Reset on power down
- Negative Triac firing pulses
- Triac Retrigger facility
- Current Limit
- Guaranteed Full Cycle Conduction with inductive load
- Tacho Input compatible with hall effect switch devices
- Electronic Interlock for use with reverse switch
- Speed Limited in reverse mode

DESCRIPTION

The ZN411 is a monolithic silicon integrated circuit designed primarily for the purpose of closed loop speed control of Universal Motors for use in power tools, food mixers, vacuum cleaners etc. The IC will also function in open loop and with both resistive or inductive loads in a multiplicity of phase control applications.

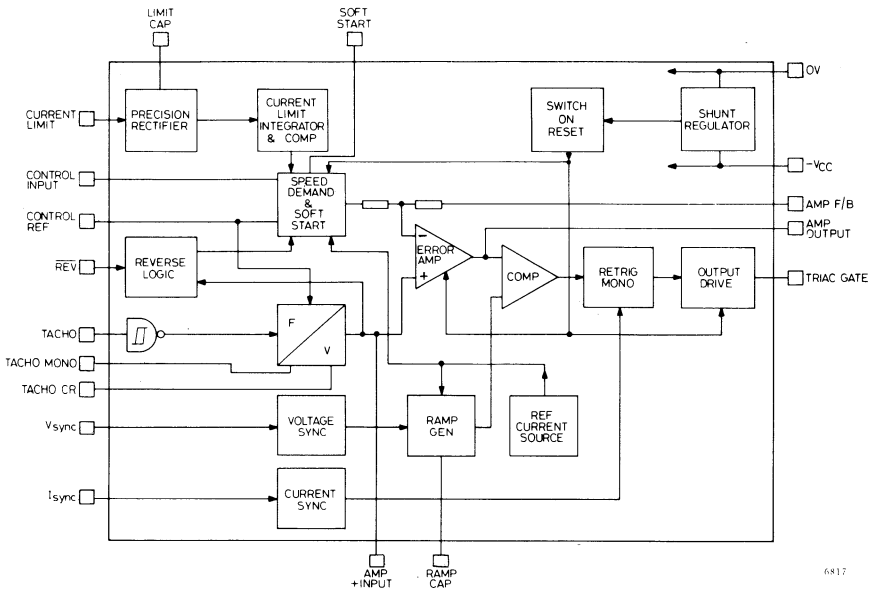


Fig. 1 System Diagram

ABSOLUTE MAXIMUM RATINGS
(all voltages measured with respect to $-V_{CC}$ Pin 2)

Maximum shunt regulator current 25mA
Input voltage on pins 15 and 18 .. .. Maximum 7.5V
Minimum −0.5V
Maximum input current on pins 13 and 14 .. .. ±2mA
Output voltage on pin 3 .. .. Maximum 7.5V
Minimum −0.5V
Operating temperature range .. .. 0 to 70°C
Storage temperature range .. .. −55 to 125°C

D.C. characteristics at (T_{amb} = 25°C unless otherwise stated).
All voltages measured w.r.t.0V pin 16 unless otherwise stated.

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Minimum operating voltage			−4.5		V
Supply current I_{CC}	$-V_{CC}$ = 4.5V All other pins O/C		−4.0	−8.0	mA
Shunt regulator voltage V_S	I_{CC} = 10mA	−4.75	−5.1	−5.4	V
Shunt regulator slope resistance	I_{CC} = 10mA		4.0	10.0	ohm
$\overline{\text{Rev}}$ input threshold voltage Pin 15 V_{TH} High state V_{TL} Low state (w.r.t. $-V_{CC}$ Pin 2)		 1.1	 2.9 1.3	 3.4 1.7	 V V
$\overline{\text{Rev}}$ input current Pin 15 I_{IH} High state I_{IL} Low state	 V_{IN} = 0V V_{IN} = $-V_{CC}$		 150	 −1	 μA μA
Tacho input threshold voltage Pin 11 V_{TH} High state V_{TL} Low state (w.r.t. $-V_{CC}$ Pin 2)			 2.9 1.3		 V V
Tacho input current Pin 11 I_{IH} High state I_{IL} Low state	 V_{IN} = 0V V_{IN} = $-V_{CC}$		 20 −125		 μA μA
Control input voltage range Pin 7	R_{V1} = 100k Pin 15 = 0V	V_{p8} (Note 1)		0	V
Control input voltage range Pin 7-Reverse mode	R_{V1} = 100k Pin 15 = $-V_{CC}$	$.23V_{p8}$ (Note 1)		0	V
Control input current Pin 7	V_{IN} = 0V		100		nA
Control potentiometer input bias current Pin 8			20		μA
Soft start capacitor charge current Pin 6			10		μA
Current limit input threshold voltage Pin 18	C_7 = 470nF		540		mV mean a.c.

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Error amplifier open loop d.c. voltage gain		29	40	59	
Error amplifier closed loop a.c. voltage gain	$C_3 = 220nf$ $R_1 = \infty$ F = 1KHz	2.9	4.4	5.9	
Minimum error amplifier output voltage	$R_{V1} = 100k$		−3.4		V
Maximum error amplifier output voltage			0		V
Voltage synch input, Pin 13 Positive input threshold current			42		μA
Negative input threshold current			14		μA
Clamp voltage (w.r.t $-V_{CC}$)	$I_{in} = +1mA$		+1.4		V
	$I_{in} = -1mA$		−100		mV
Current synch. input Pin 14 Threshold current			±110		μA
Clamp voltage (w.r.t. $-V_{CC}$)	$I_{in} = +1mA$		+1.4		V
	$I_{in} = -1mA$		−100		mV
Timing ramp amplitude, Pin 12	supply freq. at Pin 13 = 50Hz $C_5 = .1\mu F$	1.5	2.0	2.8	V pk-pk
Timing ramp capacitor charge current, Pin 12		15	20	28	μA
Triac gate pulse output, Pin 3 output voltage (V_G)	R.load Pins 3-16 = 68 ohm	−3.5			V
Output current (On state) } (I_G)	$V_{out} = -3V$	80	110	140	mA
Output current (Off state) } (I_G)	$V_{out} = 0V$			20	μA
Output pulse width (t_G)		40	80	150	μs
Minimum tacho input Pulse width, Pin 11			10		μs

Notes (1) V_{p8} = Voltage measured at pin 8 with $R_{V1} = 100k$ ohm. Typically = −2V.

OPERATING AND DESIGN NOTES

1. GENERAL DESCRIPTION

The ZN411 basically operates by comparing a voltage set on a potentiometer, proportional to speed demand, with a voltage derived from a frequency to voltage converter, proportional to motor speed. This difference or error voltage is amplified and used to define the conduction angle of a triac connected in series with the motor supply.

The input to the f/V converter is normally a signal from a tacho generator connected directly to the motor, the output frequency of the tacho being proportional to motor speed. The two voltages representing speed demand and motor speed are subtracted and the results amplified by the Error Amplifier, the output of which is connected to one input of the Ramp Comparator. The other input to the Comparator is driven from the Ramp Generator with a negative going sawtooth waveform which is synchronised to the signal on the Voltage Synch input, normally the 50Hz mains. The ramp is allowed to start shortly after the mains voltage passes through zero volts. When the ramp voltage becomes more negative than the Error Amplifier output then the Comparator output switches low and triggers a Retriggerable Monostable, which via the Output Drive Buffer will fire the Triac with a negative going current pulse. The firing angle of the triac will be dependant on the difference between the speed demand and the actual motor speed. Hence if the speed falls due to increased mechanical load, then the f/V output will go more positive, driving the Error Amplifier output positive also. The Ramp voltage will now charge to a voltage equal to the Amplifier output in a shorter time resulting in the triac gate pulse occurring at an earlier time in the mains half cycle, and consequently more power will be applied to the motor to maintain a constant speed.

When driving inductive loads, with a lagging phase angle, at or near to full conduction angle, it is necessary to ensure that the load current from the previous half cycle has fallen to zero and the triac switched off, before applying the next triac gate pulse. This is accomplished by means of the current crossing sense input which actually monitors the voltage on the live side of the triac. This input is also used to retrigger the Monostable by detecting if, for some reason due to interruptions of the load current (e.g. brush bounce), the triac inadvertantly switches off during the conduction phase.

A soft start function is provided at switch-on by ramping the speed demand voltage in a negative direction at a constant rate up to a level dependant on the voltage on the Control input. This ramp is reset whenever the supply to the ZN411 is interrupted. The switch-on reset circuit also inhibits the Output Drive Buffer until the ZN411 supply has reached operating level.

The current limit circuit operates on the average current level flowing in the load. This is achieved by monitoring across a low value resistor connected in series with the load. This signal is rectified by a precision half wave rectifier and the negative cycles fed to an integrator. The output from this integrator feeds one input of a threshold comparator, the other input of which is maintained at a fixed reference level. When the voltage output from the integrator exceeds the reference level the comparator switches and the output is used to reduce the speed demand level until the average load current drops below the set limit. In effect the motor output changes from a constant speed to a constant torque characteristic.

The reverse logic is activated by detecting a change in logic state (i.e. Low to High or vice versa) at the $\overline{\text{REV}}$ input pin. When this occurs the Soft Start Ramp is reset, removing the Triac gate drive until the motor speed, as detected by monitoring the f/V output falls to almost zero. At this point the reset is removed allowing the Soft Start Ramp to commence. With the $\overline{\text{REV}}$ input low the speed demand signal level is clamped to nominally 25% of its full scale range. The purpose of this is to limit the maximum speed of the motor in the reverse direction, primarily to minimise wear on the brush gear and commutator. For normal applications the reverse switch would be one-pole of a three-pole changeover switch used to reverse the connections to the armature.

2. TYPICAL APPLICATION FOR UNIVERSAL MOTOR SPEED CONTROL - CLOSED LOOP

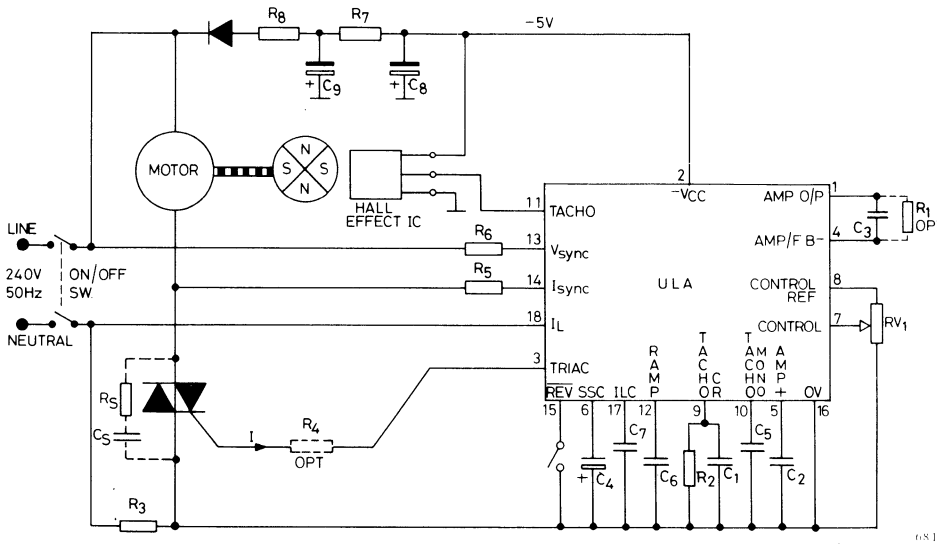


Fig. 2 Arrangement of External Components

Table 1 Typical External Component Values

Component Function	Circuit Ref.	Typical Value	Relevant Section(s)
Error amplifier gain resistor	R1	infinity	6
Tacho integrator resistor	R2	180k ohm	5
Current limit resistor	R3	0.1 ohm 2.5W	10
Triac gate current limit resistor	R4	zero	9
Current synch sense resistor	R5	270k ohm	8
Voltage synch sense resistor	R6	330k ohm	8
Supply filter resistor	R7	430 ohm	3, 9
Supply dropper resistor	R8	5.6k ohm 4W	3
Tacho integrator capacitor	C1	0.1μF	5, 6
Tacho output filter capacitor	C2	47nF	5, 6
Dynamic response capacitor	C3	0.22μF	6
Soft start ramp capacitor	C4	10μF	4, 6, 10, 11
Tacho monostable capacitor	C5	6800pF	5
Timing ramp capacitor	C6	0.1μF	7
Current limit integrator capacitor	C7	0.47μF	10
Supply decoupling capacitor	C8	22μF 6.3V	3, 4
Supply filter capacitor	C9	68μF 16V	3
Speed control potentiometer	RV1	100k ohm	4

Fig. 1 illustrates a circuit for a closed loop Universal Motor Speed Control. Feedback is provided by a 2-pole magnetic rotor connected directly to the motor armature which is sensed via an hall effect IC. A list of typical external component values is shown in Table 1 and a graph of Speed/torque curves is shown in Fig. 3. These were taken from a 400 watt motor driving a 10:1 ratio gearbox with a no load output shaft speed of 2800 r.p.m.

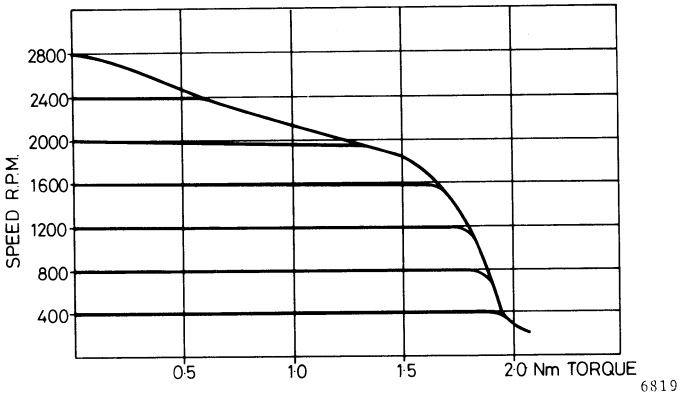


Fig. 3 Speed/Torque Curves

3. POWER SUPPLY OPTIONS

The ZN411 contains an on chip 5V shunt regulator which allows the device supply to be generated by several different methods. The most convenient method will normally be to power the device from the a.c. mains supply, via a half wave rectifier diode and dropper resistor (R_8) as shown below:

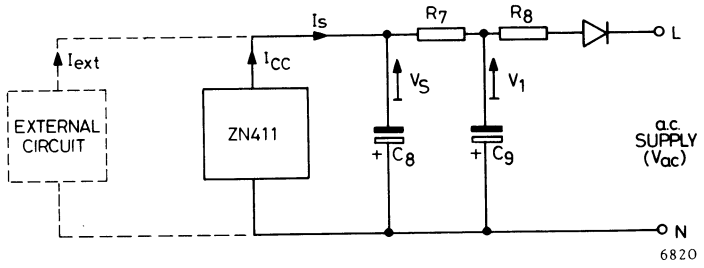


Fig. 4 Power Supply using Diode and Dropper Resistor

The component values can be found from the following formula:

Let total supply current $I_S = I_{CC} - I_{ext}$ where I_{ext} is the current taken by any additional external circuitry (i.e. Hall Effect Tacho device).

Initially we need to select a capacitor for C_9 with a maximum working voltage, V_{wkg} of normally 16 or 25V (with 240V mains supply).

Now let $V_{1(max)} = V_{wkg} - 20\%$ (1)

to allow for mains voltage variation etc.

In order to keep the ripple voltage, V_r on C_9 down to an acceptable level, make the time constant $C_9 R_7 \geqslant 30ms$ (2)

Since the voltage supplied to C_9 is half wave rectified the ripple voltage will be:

$V_r = I_S \times 10ms/C_9$ volts pk-pk

Substituting in Eq. (2) gives:

$V_r \leqslant 0.33\ I_S\ R_7$ volts pk-pk (3)

Now $R_7 = \dfrac{V_1 - V_S}{I_S}$

and since the mean value of $V_1 = V_{1(max)} - \frac{1}{2} V_r$

*Then $R_7 = \dfrac{V_{1(max)} - \frac{1}{2}V_r - V_S \text{ ohms}}{I_S}$ (4)

where V_S = Shunt regulator voltage (5.1V typical)

Substituting for R_7 in Eq. (3) gives:

$V_r \triangleq 0.3(V_{1(max)} - V_S)$ volts pk-pk (5)

If the voltage V_1 on C_9 is made much less than the a.c. supply voltage, (say $\leqslant 10\%$ of V_{ac} (rms)), then the value of R_8 approximates to:

$$R_8 \triangleq \frac{\sqrt{2} \times V_{ac} - V_1}{\pi \times I_S} \quad (6)$$

where V_{ac} is the rms value of the mains supply.

The power dissipation in R_8 also approximates to:

$$P_d = \left(\frac{I_{S(max)} \times \pi}{2}\right)^2 \times R_8 \text{ watts} \quad (7)$$

The function of capacitor C_8 is to maintain the ZN411 supply voltage at a value above the switch-on reset level during the triac gate pulse period. C_8 should be chosen so that the voltage drop during the pulse period is $\leqslant 0.5V$.

Hence $C_8 \geqslant I_G \times t_G/\delta V_S$ (8)

$\geqslant 2(I_G \times t_G)\ \mu F$

where I_G = Gate output current (mA)

t_G = Gate output pulse width (ms)

To consider an example:

Let maximum supply current I_S = 8mA

Mains voltage	V_{ac} = 240V rms
ZN411 supply voltage	V_S = 5.1V

Let V_{wkg} of C_9 = 25V d.c. working voltage
Then from Eq. (1) $V_{1(max)}$ = 25V - 20% = 20V

The ripple voltage on C_9 given by Eq. (5) is
V_r = 0.3 (20-5.1) = 4.4V pk-pk

Now from Eq. (4)

$$R_7 = \frac{20 - \frac{1}{2} \times 4.47 - 5.1}{8mA}$$

= 1583 ohms, say 1.5k ohm (Nearest prefered value)

Now if R_7 C_9 ⩾30ms
Then C_9 ⩾ 30ms/1.5k ⩾20μF
Hence let C_9 = 22μF

Now $V_{1(nom)} = V_{1(max)} - \frac{1}{2}V_r$
= 20 - ½ × 4.47 = 17.7V

From Eq. (6)

$$R_8 = \frac{\sqrt{2} \times 240 - 17.7}{\pi \times 8mA} = 12.8k \text{ ohm}$$

Hence let R_8 = 12k ohm

Now substituting R_8 back in Eq. (6) to find $I_{S(max)}$ gives

$$I_S = \frac{\sqrt{2}\,(240 + 10\%) - 17.7}{\pi \times 12000}$$

$I_{S(max)}$ = 9.43mA

Therefore from Eq. (7) the maximum dissipation in R_8 will be:

$$P_d = \left(\frac{9.43mA \times \pi}{2}\right)^2 \times 12{,}000$$

= 2.63W

Let rating of R_8 = 3 watts

Finally taking $I_{G(max)}$ = 140mA
$t_{G(max)}$ = 150μs

Then C_8, from Eq. (8)
⩾2(140mA × 0.15ms) ⩾42μF
Let C_8 = 47μF (6.3 volt)

In an actual design case the tolerances of the mains supply and components selected should be taken into account.
NOTE: A more accurate formula for R_7 is given by:

$$R_7 = \frac{0.668Vwkg - 4.26}{I_S}$$

The main disadvantage of using a dropper resistor is usually one of heat dissipation in the resistor. This can be overcome by using a reactive dropper circuit as shown below:

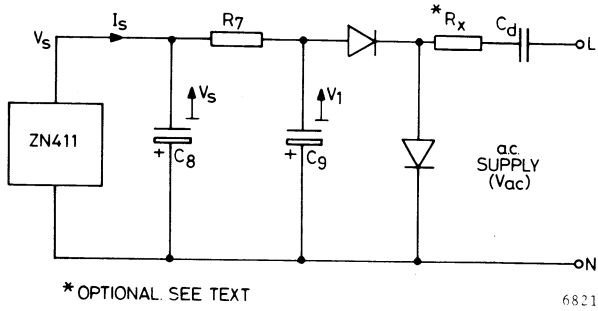


Fig. 5 Power Supply using Reactive Dropper Circuit

In this case the component values are calculated as follows:

Neglecting diode volt drop, the charge transferred via capacitor C_d is given by:
$Q = C_d\ (2V_{pk} - V_1)$
Now $i = Q/_t = Qf$ where f = mains frequency.
Therefore $i = C_d \times f\ (2V_{pk} - V_1)$
Now since $i = I_S$ and $V_{pk} = \sqrt{2}\ V_{ac}$
Then

$$C_d = \frac{I_S}{f\ (2.82\ V_{ac} - V_1)} \qquad (9)$$

Resistor R_x can be included to limit the surge current at switch on. A value of 330 ohms is generally recommended to limit the surge current to the order of 1 amp maximum.

Equations (1) to (5) for the selection of C_9 and R_7 and equation (8) for C_8 still apply for a reactive dropper circuit.

To consider an example, taking the same conditions as previously:
With $V_{1(nom)} = 17.7V$

$$C_d = \frac{I_S}{f\ (2.82\ V_{ac} - V_1)} = 8mA/50\ (2.82 \times 240 - 17.7)$$

$$\underline{C_d = 0.24\mu F}$$

Nearest preferred values are 0.22 and 0.33μF

Using a 0.22μF will give a supply current of
$I_S = C_d \times f\ (2.82\ V_{ac} - V_1)$
$= 0.22.10^{-6} \times 50\ (2.82 \times 240 - 17.7)$

$I_S = 7.25mA$ (nominal)
If this is too low a 0.33μF capacitor will have to be used.

Substituting this value of C_d in Eq. (9) gives:

$I_S = 10.87mA$

With $R_7 = 1.5k$ ohms as calculated in the previous example, the voltage V_1 from Eq. (4) will now be:

$V_{1(nom)} = R_7 \times I_S + V_S = 21.4$ volts

and since $V_r = \frac{I_S \times 10ms}{C_9}$

$V_r = 4.93V$ pk-pk

Hence $V_{1(max)} = 21.4 + 4.93/2 = \underline{23.8 \text{ volts}}$

This is rather close to the maximum d.c. working voltage of C_9 chosen previously of 25V, and it would be advisable to select a higher working voltage capacitor in the range of 35 to 40V.

This example illustrates a problem of using a capacitive dropper. It is not always easy to select a preferred value of C_d for the design characteristics required.

Alternatively the value of R_7 can be reduced to maintain the same value of V_1, and C_9 will have to be increased in value to comply with Eq. (2).

Operation from stabilised or unstabilised d.c. supplies is possible simply by using the following circuit.

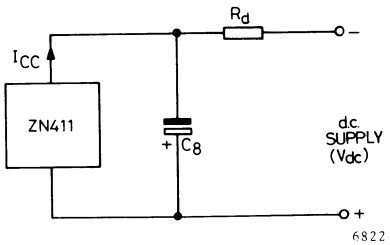


Fig. 6 Operation from Stabilised or Unstabilised DC Power Supplies

The value of R_d can be found from:

$R_d = \frac{V_{dc} - V_{CC}}{I_{CC}}$

The value of C_8 will be the same as that calculated previously.

Note that when designing with unregulated supplies the value of the resistor (R_d) should be calculated by taking into consideration the minimum and maximum peak values of the supply. Where possible the d.c. supply should be made much greater than the shunt regulator voltage in order to keep the supply current within specification.

4. SPEED CONTROL AND SOFT START

The ZN411 has been specially designed so that for the majority of applications no production line adjustments are necessary and satisfactory calibration of the operating characteristics can usually be achieved by using fixed values for all external components. This "built in calibration" was designed around a number of accurately matched current sources which are used in the critical areas of the circuit that affect the speed calibration. One of these current sources is connected to the Control Ref. pin 8, and sources a nominal current of 20 microamps through the Speed Control potentiometer. This develops a voltage of nominally 2.0 volts across the potentiometer, the value of which should be 100k ohms. The circuit was designed to use this particular value of potentiometer and use of a different value will limit the speed control range of the device. The voltage applied to the Control input pin 7 adjusts the conduction angle of the triac and hence the speed of the motor. For certain applications other forms of speed control input, rather than a potentiometer may be necessary, (e.g. microprocessor control via a D/A converter). In these cases a fixed 100k ohms resistor should be connected from 0V to Pin 8, and the control voltage applied to pin 7 should be referenced to the voltage at pin 8. (w.r.t. to 0V rail.) Failure to do this will result in poorer performance over the temperature range, and in addition the system would probably have to be recalibrated if the ZN411 was changed.

The rate of rise of the control voltage applied to the Error Amplifier is governed by the Soft Start capacitor C_4. When power is first applied to the ZN411 the Switch-on Reset circuit ensures that this capacitor is fully discharged. A 10 microamp current source then charges the capacitor and the voltage on the capacitor rises linearly to a level determined by the setting of the speed control pot. Thus with a normal circuit the motor speed will rise at a constant rate (i.e. constant acceleration) until it reaches the preset level. The time for the capacitor to obtain full charge, with V pin 7 = V pin 8 (i.e. maximum speed) is given by the equation:

$$t_{ss} = C/5 \text{ secs} \qquad (10)$$

where C is the value of C_8 in microfarads.

Note that the charge rate is constant irrespective of the voltage applied to the control input, therefore with the control potentiometer set midway (i.e Half full speed), the soft start time will be half of that calculation in Eq. (10). Also it should be borne in mind that the total time for the motor to attain the set speed will also be affected by mechanical considerations, such as the inertia of the system, and the load torque.

5. TACHO INPUT AND f/V CONVERTER

The Tacho input, pin 11 was designed primarily for use with Hall Effect Switch IC's such as the UGN-3013 T device, although magnetic coil pickups can also be used and are easily interfaced.

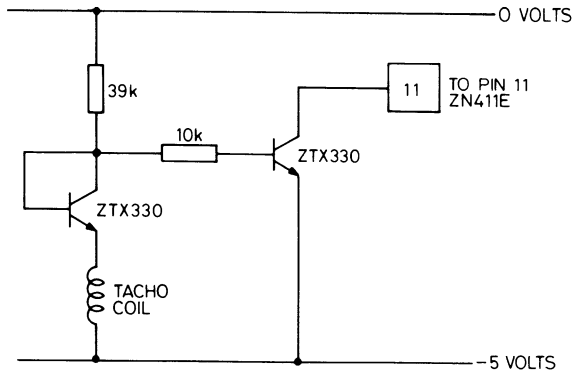


Fig. 7 Magnetic Coil Pickup Buffer

The input circuit on pin 11 is as shown below:

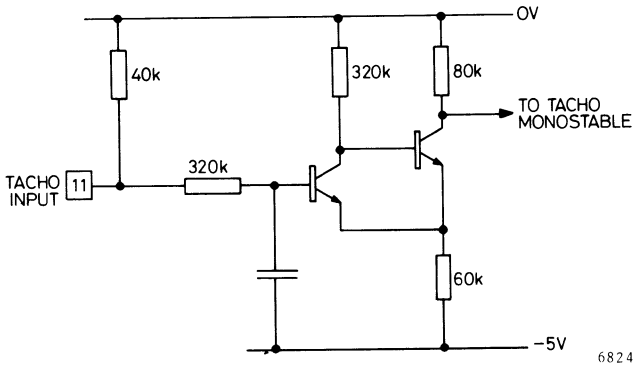


Fig. 8 Input Circuit on Pin 11

The open collector output of the Hall Effect Switch IC can be directly connected to pin 11 so that the internal 40k ohm resistor will act as a pull up resistor for the IC output. The 320k ohm input resistor and capacitor form a low pass filter to reject any hf noise spikes on the input.

The Tacho Monostable time is given by the equation:

$$t_{mono} = \frac{C_5 \times V_{ref}}{I_1} \text{ (sec)} \qquad (11)$$

where V_{ref} = Voltage at pin 8 (nominally 2.0V).

I_1 = 55μA, the value of the current source on pin 10.

C_5 = Capacitor connected across pins 10-16 (in mircofarads).

t_{mono} must be less than the minimum period of the Tacho input.

Therefore $t_{mono} < 1/f_{T(max)} < \frac{60}{N_{(max)} \times P}$ (sec)

where $f_{T(max)}$ = Maximum tacho frequency.

$N_{(max)}$ = Maximum armature speed (rpm).

P = Number of poles on the tacho.

Substituting in Eq. (11).

$$\frac{C_5 \times V_{ref}}{I_1} < \frac{60}{N_{(max)} \times P}$$

$$\therefore C_5 < \frac{60 \times I_1}{V_{ref} \times N_{(max)} \times P} \qquad (12)$$

In order to allow for component and processing tolerances the nominal value of the monostable capacitor should be calculated from:

$$C_5 = \frac{500}{N_{(max)} \times P} \ \mu F \qquad (13)$$

The Tacho Monostable circuit gates constant current pulses to an RC integrator formed by C_1 and R_2 on pin 9. At maximum speed the voltage on pin 9 should be equal to the Control Bias voltage on pin 8.

Hence - V_{out} (pin 9) = $V_{ref} = I_{avg} \times R_2$

$= I_2 \times t_{mono} \times f_{T(max)} \times R_2$

Where I_2 = value of pulsed current source.

Substituting t_{mono} from Eq. (11).

$$V_{ref} = I_2 \times \frac{C_5 V_{ref}}{I_1} \times f_{T(max)} \times R_2$$

Now $I_2 = I_1$ (by design) and this equation simplifies to:

$$R_2 = 1/C_5 \times f_{T(max)} = \frac{60}{C_5 \times N_{(max)} \times P} \qquad (14)$$

The value of C_1 determines the tacho integration time constant and therefore the amplitude of the ripple on pin 9. The signal from pin 9 is buffered and fed to the non-inverting input of the Error Amplifier via a second stage of filtering comprising of an internal 160k ohm resistor and capacitor C_2 connected to pin 5. The amplitude of the ripple on the output of the Error Amplifier is then determined by the values of both C_1 and C_2 and also by the a.c. gain of the amplifier. This ripple voltage results in a slight variation of the firing angle of the triac but this is normally damped by the mechanical inertia of the motor and is usually undetectable. However, at low speed the ripple voltage can beat with the mains frequency to produce a low frequency speed variation in the drive. The value of C_1 and C_2 can be increased in order to reduce the ripple and hence "beating" effect. These capacitors also affect the dynamic response of the system and if they are too high sluggish response of the motor will result. In most systems satisfactory dynamic performance and low speed operation can usually be obtained by empirical selections of C_1 and C_2 in conjunction with C_3 as described in the next section. In extreme cases the tacho ripple voltage can always be reduced by using a tacho rotor with a larger number of poles.

As a general rule if low speed operation is required especially for motors with low mechanical inertia then it is good design practise to use a tacho with the maximum number of poles that cost and physical limitations will permit.

6. ERROR AMPLIFIER

The Error Amplifier was designed to have an open loop d.c. gain of typically 40 and a closed loop a.c. gain of typically 4.4. These values were found to give the best overall performance for motors up to the order of 1000 watt rating. Some adjustment can be made to the characteristics of the amplifier by the addition of external resistors, but unless it is for special applications it is recommended that the use of these should be avoided.

The a.c. gain is fixed by an internal feedback resistor and its value cannot be reduced. A resistor connected in series with capacitor C_3 between pins 1 and 4 can be used to increase the a.c. gain but this has the disadvantage that the soft-start function may not operate correctly, due to the fact that C_3 is pre-charged at switch-on as part of the soft-start sequence. The d.c. gain is also fixed by the design of the amplifier but this can be reduced by means of an external resistor (R_1) connected in parallel with C_3, across pins 1 and 4. However, this suffers from two disadvantages. First the tolerance on the absolute value of feedback resistor can be as high as +75 and −50%. (Note that this does not affect the performance of the ZN411 normally since the design relies on the matching of internal resistors and not their absolute value). This could mean that on a production line the value of the external feedback resistor may have to be separately adjusted for each unit incorporating the ZN411. Secondly the external resistor temperature coefficient will probably not match the internal resistors resulting in variations of regulation and dynamic response over the operating temperature range.

A schematic diagram of the amplifier is shown below:

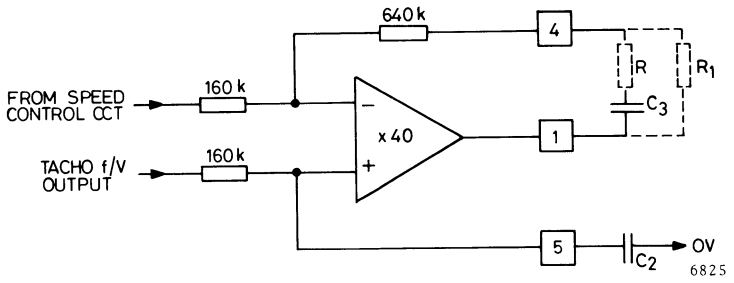


Fig. 9 Schematic Diagram of Error Amplifier

The frequency response of the amplifier can be adjusted by means of C_3 while the overall dynamic response of the system is also governed by the values of C_1 and C_2. The values of these capacitors are best chosen by experimentation with the ZN411 circuit connected to the actual motor/gear box/load combination to be used in the final product. The value of the soft start capacitor C_4 can also be verified at this stage. Only if satisfactory performance cannot be achieved by adjustment of these capacitor values should modifications of the a.c./d.c. gain of the amplifier with external resistors be considered.

7. COMPARATOR RAMP GENERATOR

The comparator ramp circuit consists of a matched current source which is used to charge the timing ramp capacitor, C_6 connected to pin 12. A discharge transistor is connected from pin 12 to the 0V rail and this is switched on by the Voltage Synch logic for 200μs as the mains voltage passes through zero volts. Pin 12 is also connected internally to one input of the Comparator, the other input of which is connected to the Error Amplifier output. The ramp voltage therefore constitutes a timing reference signal which is reset at the start of each mains half cycle. The value of Ramp capacitor C_6 should be selected to produce a nominal 2.0 volts amplitude ramp at pin 12 with a charging current of 20 microamps.

Since $i = C\ dv/dt$

Then $C_6 = I_3/V_{ramp} \times 2f$

Where f = mains supply frequency

For V_{ramp} = 2.0 volts this gives:

$C_6 = 5/f$ (microfarads) (15)

The overall gain of the system is inversely proportional to the amplitude of the ramp signal. This fact can be used to provide some adjustment of gain by selecting different values of C_6 rather than using external feedback resistors as described in the previous section. The designer should take care to ensure that the negative peak amplitude of the ramp is always more positive than the minimum Error Amplifier output voltage, after taking into account all component tolerances. Failure of the ramp signal to meet this requirement will result in the speed control range being restricted at the low speed end of the conduction angle/motor speed characteristic.

8. VOLTAGE AND CURRENT SYNCHRONISATION

The function of the voltage synchronisation circuit is to produce a pulse symetrical in time about the point when the mains voltage crosses zero volts. This pulse is then used to discharge the Ramp capacitor. If this pulse is not symmetrical then the ramp will start at a different time on alternate positive and negative half cycles producing a different triac firing angle for the two half cycles and resulting in a d.c. component being fed to the load, which in most cases is undesirable. Due to other circuit design considerations the input, pin 13, was referenced to the $-V_{CC}$ rail, whereas ideally the input threshold levels should be referenced to the 0V (neutral) rail in order to achieve symmetrical switching. In order to accomplish this the positive input current threshold level was designed to be a factor of three times the negative current threshold. Hence by suitable choice of external resistor R_6, the voltage threshold levels on the mains waveform can be calculated to produce values of $+15$ and -5 volts with respect to the $-V_{CC}$ rail, which is ± 10 volts with respect to the 0 volt rail.

The level is given by:

$$+V_{th} = I_{in} \times R_6$$

and

$$-V_{th} = -I_{in} \times R_6$$

where $\pm V_{th}$ are the threshold voltages with respect to $-V_{CC}$ and $\pm I_{in}$ are the input currents given in the DC characteristics. A resistor of 330k ohms produces the correct levels.

The function of the Current synchronisation circuit is twofold, (a) to trigger the Output Monostable when driving inductive loads and (b) to generate a re-trigger pulse if for any reason the triac prematurely switches off before the end of the mains half cycle. The output Monostable is normally triggered by the Comparator when the ramp voltage crosses the Error Amplifier output level. However, when driving inductive loads at high conduction angles, the Comparator may have switched over before the load current from the previous half cycle has dropped to zero. In this case the trigger to the Output Mono is held off until the triac switches off as the load current drops below the triac hold current level. At this point the voltage across the triac will rapidly switch to the instantaneous value of the mains voltage, which depends on the phase lag of the load current. This voltage step is detected by the Current Synch input, pin 14 and providing that the Comparator output is already low, will trigger the Output Mono. The same thing occurs if the triac shuts off before the end of the mains half cycle causing the voltage across the triac to switch to the instantaneous level of the mains voltage. Unlike the voltage synch input it is not important that the current synch input be symmetrical about the 0V rail. The threshold current is nominally 110 microamps referenced to the $-V_{CC}$ rail and so a 270k ohms input resistor (R_5) will produce a threshold voltage of typically ± 30 volts.

Note that under certain conditions with a faulty triac that will not hold in the on state, the ZN411 will repetitively apply firing pulses to the triac. Due to the relatively high peak level of gate current compared to the ZN411 supply current this will, after several firing pulses, pull the device supply voltage below the Switch-on Reset level. In this situation a faulty triac can easily be mistakenly diagnosed as a malfunctioning IC.

9. TRIAC GATE OUTPUT

The triac Gate output circuit generates constant current negative going pulses, for more balanced firing of the triac, and allows direct connection between the ZN411 output and the gate terminal of the triac. The gate current level and pulse width are set internally in the ZN411 and are suitable for most types of small to medium power triacs (up to the order of 40A load currents). The maximum gate current can additionally be limited by means of an external resistor R_4. The only advantage in doing this would be, when using a sensitive gate triac, to allow the dropper resistor (R_7) wattage and capacitor value (C_8) to be reduced in value, since the normal gate current consitutes approximately 20% of the device supply current. See section 3 for details of selections of components R_7 and C_8. The value of external limiting resistor can be calculated from:

$$R_4 = \frac{4.8 - V_{GT}}{I_G} - 6.5 \quad (16)$$

where V_{GT} = Gate trigger voltage of triac
I_G = Gate current of triac

10. CURRENT LIMIT

The current limit is set by the value of resistor R_3 connected in series with the load. The voltage dropped across this resistor by the load current is rectified and then integrated by capacitor C_7 in conjunction with a 160k ohm on chip resistor. The voltage on C_7 is used to switch the Limit Comparator which discharges the soft start capacitor, C_4, thereby reducing the triac conduction angle and hence load current until it falls below the trip level of the current limit circuit. This level corresponds to a mean voltage across R_3 of 540mV which is equivalent to 6A rms through a 100 milliohm resistor (for a full sine wave). Some variations in the characteristics of the Current Limit circuit can be achieved by changing the value of C_7. Generally the time constant of C_7 and the on-chip 160k ohm resistor should be of the order of several mains supply cycles (i.e. 100 millisecs). A higher value will result in slower response of the circuit to an overload whereas a lower value will produce a fast response, but as the integrator time constant is reduced the circuit will react more to the peak rather than the average value of the current waveform. This will result in foldback of the torque/speed characteristic which may be a useful feature for some types of applications.

Note that the current limit facility should be used more as a torque limiting mechanism rather than as an overload protection for the motor. The problem with relying on the Current Limit circuit to protect the motor is that as the load is applied the motor characteristic will change from constant speed to essentially constant torque at the current limit point, see Fig. 3. If the load is maintained then the motor speed will rapidly fall off towards zero. However, most small universal motors are cooled by a small centrifugal fan mounted on the armature which draws air through the motor casing past the windings. The cooling efficiency of this arrangement is very poor at low armature speeds causing most motors to rapidly overheat if the power is not removed within a short time under current limit conditions.

11. REVERSE SWITCH INPUT

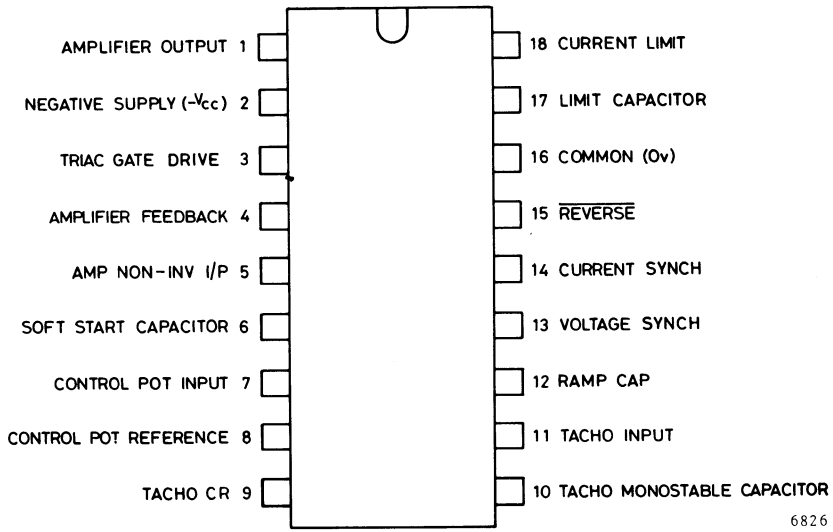
This input was designed to operate in conjunction with a change-over switch which will reverse either field or armature connections of the motor. When a logic change of either polarity is detected at the $\overline{REV}$ input, pin 15, then the soft start capacitor, C_4 is discharged and held discharged until the motor speed falls to almost zero. At this time the hold on C_4 is removed, which enables the triac gate pulses and allows the motor to accelerate under control of the Soft Start Ramp. Without this function very high transient currents can flow in the armature, (leading to damage of the brushes and commutators) if connections are reversed with power applied and the motor in motion. Ideally a 3 pole break-before-make switch should be used with the switch pole for the Reverse input, timed so that it operates while the two poles used for the armature are open-circuit. This will ensure that the output drive will be removed before the armature connections are made when switching in either direction. The Reverse input pin has an on-chip 40k ohm pull down resistor between the input and the $-V_{CC}$ rail. This allows the use of a single way on/off switch to be used as the control pole of the change-over switch, so that with pin 15 open circuit the forward mode is selected. With pin 15 connected to the 0 volt rail the reverse mode is activated. Note that the speed is internally limited to 25% of the speed control range when in the reverse mode.

Note that if the motor reversing switch poles are omitted the Reverse control can be used to change the speed range of the motor. However, when the control switch is operated the motor speed will immediately be reduced to zero and will then run up to the new speed with a normal soft start.

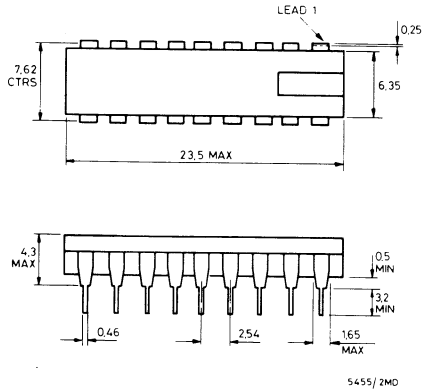
12. LIST OF SYMBOLS

Symbol		Definition	Relevant Section(s)
f	-	Mains frequency	7
f_T	-	Tacho frequency	5
I_1	-	Current source value, pin 10	5
I_2	-	Current source value, pin 9	5
I_{CC}	-	Chip supply current	3
I_{ext}	-	External circuitry d.c. supply current	3
I_G	-	Triac gate output current, pin 3	3, 9
I_S	-	Total d.c. supply current	3
N	-	Armature speed	5
P	-	Number of Tacho Poles	5
P_d	-	Power dissipation	3
t_G	-	Triac gate pulse width	3
t_{mono}	-	Tacho monostable time period	5
t_{ss}	-	Soft start time period	4
V_1	-	d.c. voltage on C_9	3
V_{ac}	-	Mains a.c. supply voltage (rms)	3
V_{CC}	-	d.c. voltage on pin 2	3
V_{dc}	-	Unstabilised d.c. supply voltage	3
V_G	-	Triac gate output voltage, pin 3	9
V_{GT}	-	Gate trigger voltage of triac	9
V_r	-	Ripple voltage on C_9 (pk-pk)	3
V_s	-	Shunt regulator voltage	3
V_{wkg}	-	Maximum working voltage of C_9	3
V_{ramp}	-	Ramp amplitude, pin 12 (pk-pk)	7
V_{ref}	-	Control reference voltage, pin 8	5
$\pm V_{th}$	-	Voltage sense threshold voltages	8
$\pm V_{TH}$	-	$\overline{REV}$ input threshold voltage	11

PIN CONNECTIONS



PACKAGE DETAILS



18 LEAD MOULDED D.I.L.

Dimensions in millimetres

ZN414Z
ZN415E
ZN416E

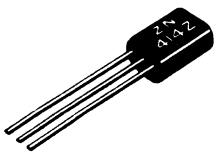
FERRANTI semiconductors

AM Radio Receivers

FEATURES

- Single cell operation (1.1 to 1.6 volt operating range)
- Low current consumption
- 150kHz to 3MHz frequency range (i.e. full coverage of medium and long wavebands)
- Easy to assemble, no alignment necessary
- Simple and effective AGC action
- Will drive crystal earphone direct (ZN414Z)
- Will drive headphones direct (ZN415E and ZN416E)
- Excellent audio quality
- Typical power gain of 72dB (ZN414Z)
- Minimum of external components required

ZN414Z



PLASTIC (TO-92)

ZN415E
ZN416E

8-Lead D.I.L.

GENERAL DESCRIPTION

The ZN414Z is a 10 transistor tuned radio frequency (TRF) circuit packaged in a 3-pin TO-92 plastic package for simplicity and space economy.

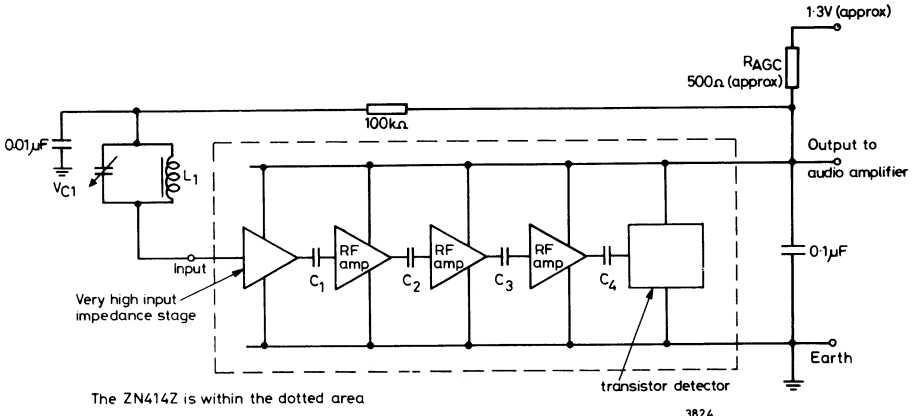
The circuit provides a complete R.F. amplifier, detector and AGC circuit which requires only six external components to give a high quality A.M. tuner. Effective AGC action is available and is simply adjusted by selecting one external resistor value. Excellent audio quality can be achieved, and current consumption is extremely low. No setting-up or alignment is required and the circuit is completely stable in use.

The ZN415E retains all the features of the ZN414Z but also incorporates a buffer stage giving sufficient output to drive headphones directly from the 8 pin DIL.

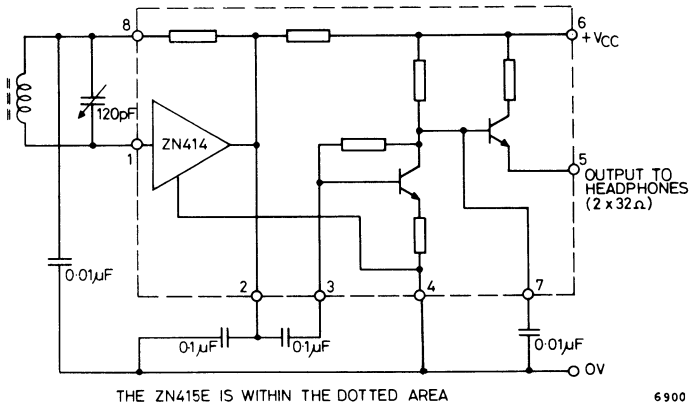
Similarly the ZN416E is a buffered output version of the ZN414Z giving typically 120mV (r.m.s.) output into a 64Ω load. The same package and pinning is used for the ZN416E as the ZN415E.

DEVICE SPECIFICATIONS $T_{amb} = 25°C$, $V_{CC} = 1.4V$. Parameters apply to all types unless otherwise stated.

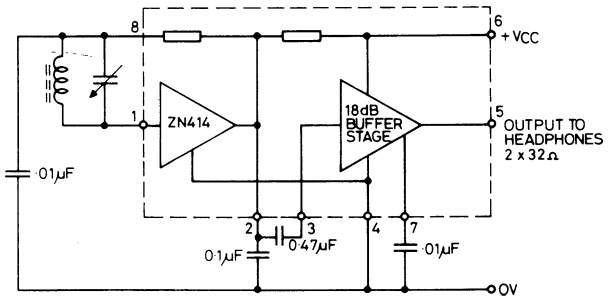
Parameter		Min.	Typ	Max.	Units
Supply voltage, V_{CC}		1.1	1.3	1.6	volts
Supply current, I_S with 64Ω headphones	ZN414Z	-	0.3	0.5	mA
	ZN415E		2.3	3	
	ZN416E		4	5	
Input frequency range		0.15	-	3.0	MHz
Input resistance		-	4.0	-	MΩ
Threshold sensitivity (Dependant on Q of coil)			50		μV
Selectivity		-	4.0	-	kHz
Total harmonic distortion		-	3.0	-	%
AGC range		-	20	-	dB
Power gain (ZN414Z)			72		dB
Voltage gain of output stage	ZN415E	-	6	-	dB
	ZN416E		18		
Output voltage into 64Ω load before clipping	ZN414Z	-	60	-	mVpp
	ZN415E		120		
	ZN416E		340		
Upper cut-off frequency of output stage, No capacitor, (ZN415E and ZN416E)		20	-	-	kHz
With 0.01μF between pin 7 and 0V (ZN415E)		-	6	-	kHz
With 0.01μF between pin 7 and 0V (ZN416E)		-	10	-	kHz
Lower cut-off frequency of output stage 0.1μF between pins 2 and 3 for ZN415E 0.47μF between pins 2 and 3 for ZN416E		-	50	-	Hz
Quiescent output voltage	ZN414Z	-	40	-	mV
	ZN415E		80		
	ZN416E		200		
Operating temperature range		0	-	70	°C
Maximum storage temperature		−65	-	125	°C



ZN414Z System Diagram



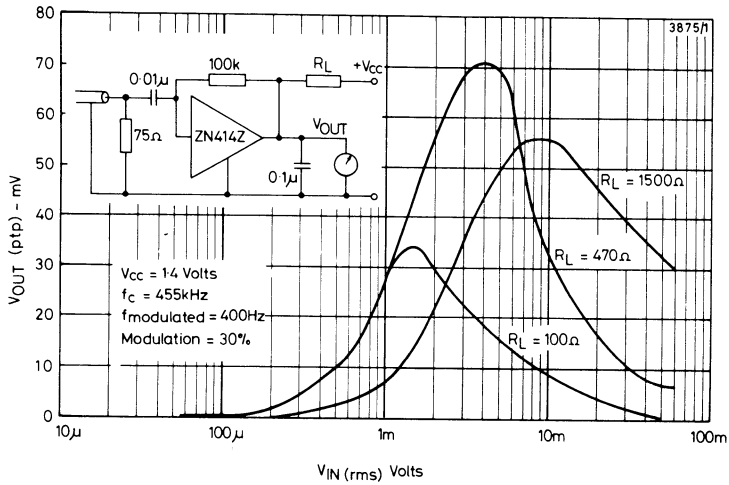
ZN415E System Diagram



ZN416E System Diagram

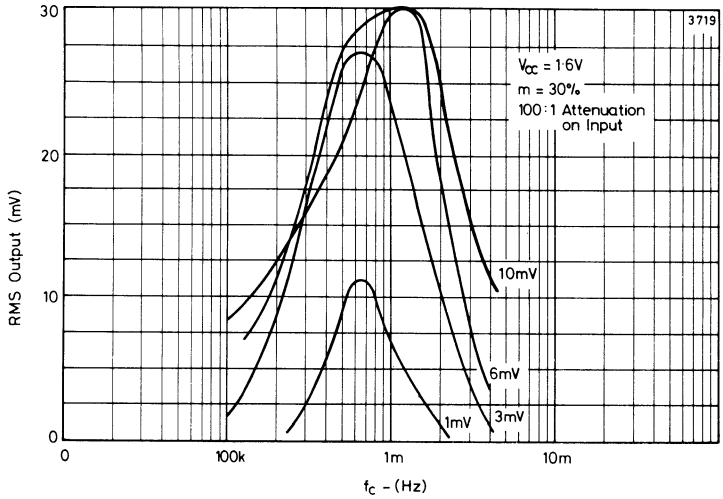
ZN414Z CHARACTERISTICS – All measurements performed with 30% modulation, $F_M = 400Hz$

Gain and AGC characteristics



See operating notes for explanation of AGC action.

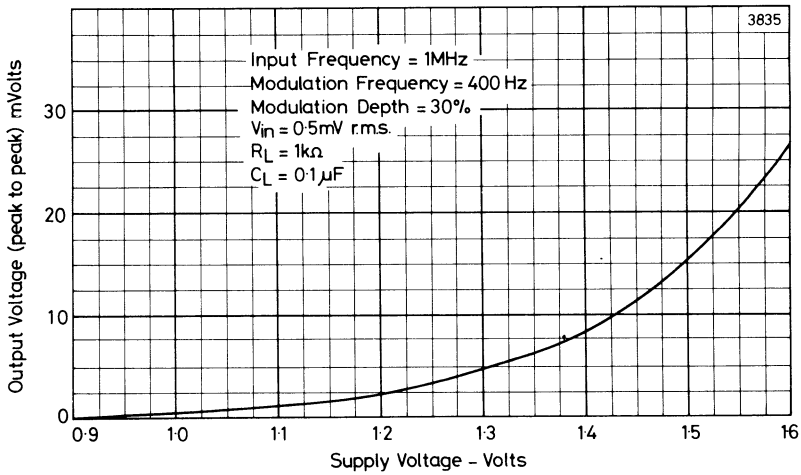
Frequency response of the ZN414Z



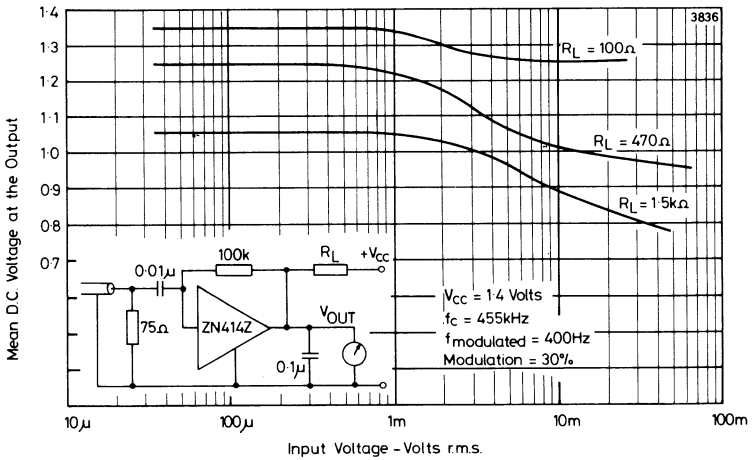
Note that this graph represents the chip response, and not the receiver bandwidth.

ZN414Z CHARACTERISTICS – *(Continued)*

Gain variation with supply volts.



D.C. level at output



LAYOUT REQUIREMENTS

As with any high gain R.F. device, certain basic layout rules must be adhered to if stable and reliable operation is to be obtained. These are listed below:

1. The output decoupling capacitor should be soldered as near as possible to the output and earth leads of the ZN414Z. Furthermore, its value together with the AGC resistor (R_{AGC}) should be calculated at $\approx$4kHz, i.e.:

$$C \text{ (farads)} = \frac{1}{2\pi \cdot R_{AGC} \cdot 4 \cdot 10^3}$$

2. All leads should be kept as short as possible, especially those in close proximity to the ZN414Z.
3. The tuning assembly should be some distance from the battery, loudspeaker and their associated leads.
4. The 'earthy' side of the tuning capacitor should be connected to the junction of the 100kΩ resistor and the 0.01μF capacitor.

OPERATING NOTES

(a) Selectivity

To obtain good selectivity, essential with any T.R.F. device, the ZN414Z must be fed from an efficient, high 'Q' coil and capacitor tuning network. With suitable components the selectivity is comparable to superhet designs, except that a very strong signal in proximity to the receiver may swamp the device unless the ferrite rod aerial is rotated to "null-out" the strong signal.

Two other factors affect the apparent selectivity of the device. Firstly, the gain of the ZN414Z is voltage sensitive *(shown on page 5)* so that, in strong signal areas, less supply voltage will be needed to obtain correct AGC action. Incorrect adjustment of the AGC causes a strong station to occupy a much wider bandwidth than necessary and in extreme cases can cause the RF stages to saturate before the AGC can limit RF gain. This gives the effect of swamping together with reduced AF output. All the above factors have to be considered if optimum performance is to be obtained.

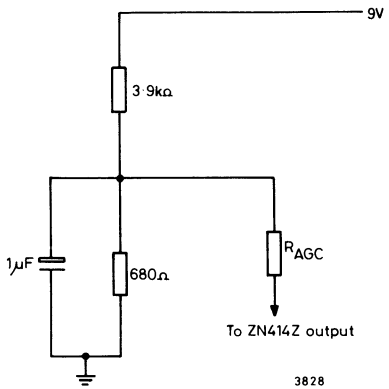
(b) Ferrite aerial size

Because of the gain variation available by altering supply voltage, the size of the ferrite rod is relatively unimportant. However, the ratio of aerial rod length to diameter should ideally be large to give the receiver better directional properties. Successful receivers have been constructed with ferrite rod aerials of 4cm (1.5") and up to 20cm (8").

DRIVE CIRCUITS

Three types of drive circuit are shown, each has been used successfully. The choice is largely an economic one, but circuit 3 is recommended wherever possible, having several advantages over the other circuits. Values for 9V supplies are shown, simple calculations will give values for other supplies.

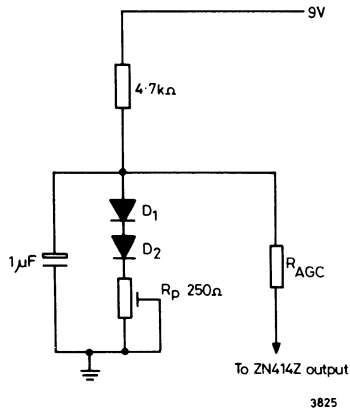
1. Resistive Divider



Current consumption = 2mA

Note: Replacing the 680Ω resistor with a 500Ω resistor and a 250Ω preset, sensitivity may be adjusted and will enable optimum reception to be realised under most conditions.

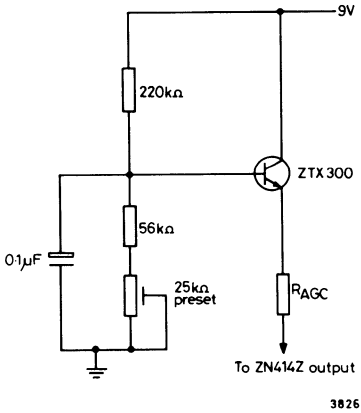
2. Diode Drive



$D_1 = D_2$ = Any general purpose silicon diode
R_p = Optional sensitivity control, a recommended value being 250Ω.

Current consumption ≈ 1.5mA

3. Transistor Drive

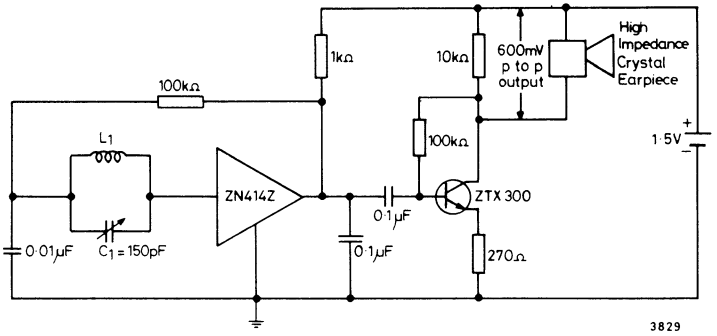


Current consumption is virtually that which is taken by the ZN414Z (0.3mA)

RECOMMENDED CIRCUITS

(a) Earphone radio

The ZN414Z will drive a sensitive earpiece directly. In this case, an earpiece of equivalent impedance to R_{AGC} is substituted for R_{AGC} in the basic tuner circuit. Unfortunately, the cost of a sensitive earpiece is high, and unless an ultra-miniature radio is wanted, it is considerably cheaper to use a low cost crystal earpiece and add a single gain stage. One further advantage of this technique is that provision for a volume control can be made. A suitable circuit is shown below.

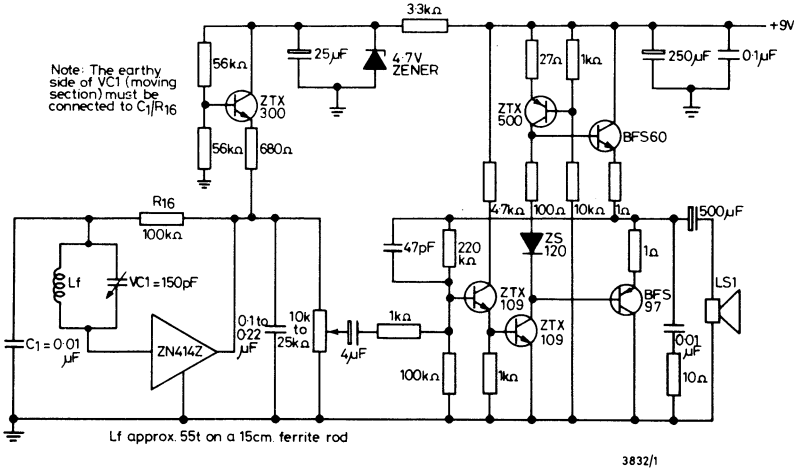


$L_1 \approx 80$ turns of 0.3mm dia. enamelled copper wire on a 5cm or 7.5cm long ferrite rod. Do not expect to adhere rigidly to the coil-capacitor details given. Any value of L_1 and C_1 which will give a high 'Q' at the desired frequency may be used.

Volume Control: a 250Ω potentiometer in series with a 100Ω fixed resistor substituted for the 270Ω emitter resistor provides an effective volume control.

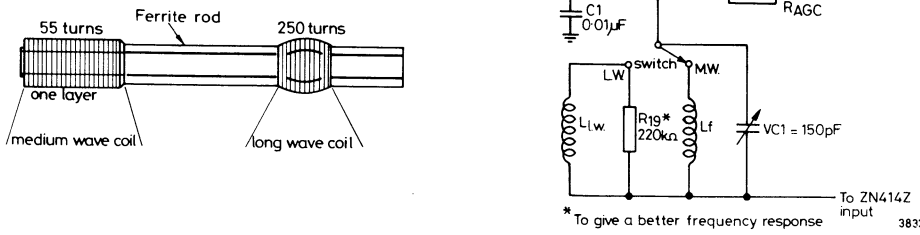
(b) Domestic portable receiver

The circuit shown is capable of excellent quality, and its cost relative to conventional designs is much lower.



The complete circuit diagram of the Triffid receiver

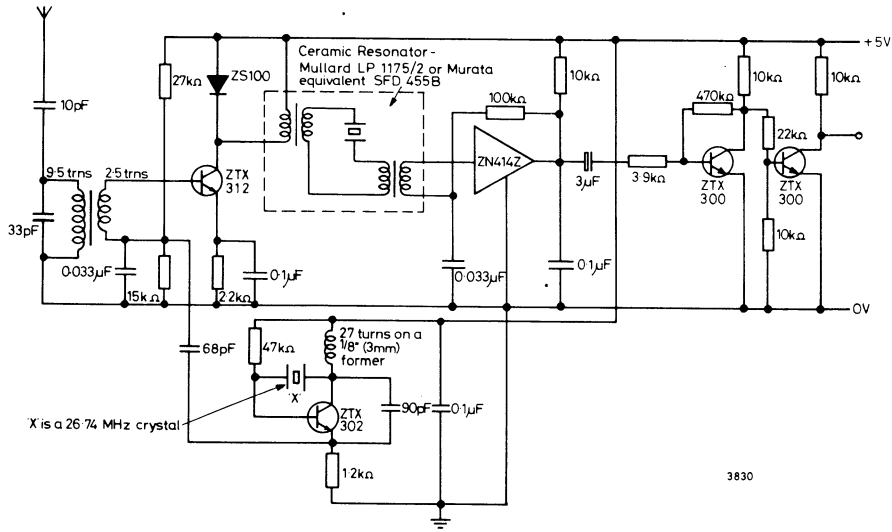
(b)i



Coil winding details and waveband selection

(c) Use in model control receiver

The circuit below shows a ZN414Z used as an I.F. amplifier for a 27MHz superhet receiver.



Performance Details:

Sensitivity = 2.5μV for a 5V p.t.p. output measured at f_C = 27.21MHz, 100% modulated with 100Hz square wave.

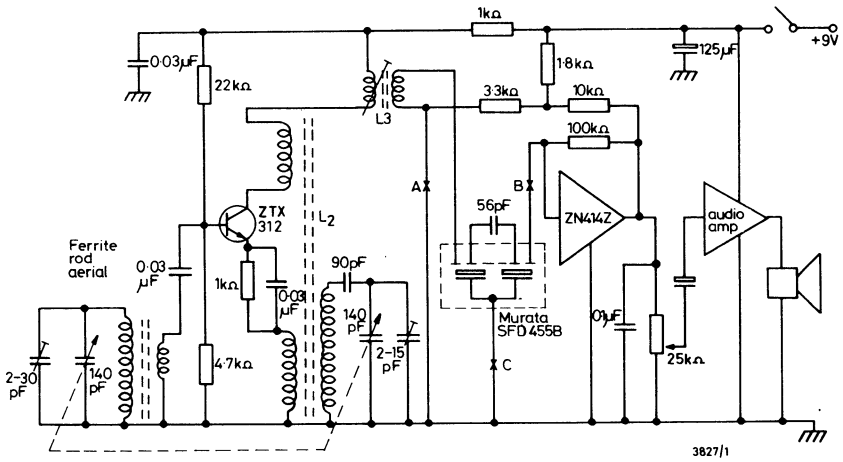
Selectivity: ±5kHz for <100mV p.t.p. output.

Input Signal Range: 2.5μV to 25mV (i.e. 80dB)

Supply Current: ≈4.5mA.

(d) Broadcast band superhet using ZN414Z

The ZN414Z coupled with the modern ceramic resonators offers a very good I.F. amplifier at modest cost, whilst maintaining simplicity and minimal alignment requirements. A typical circuit is shown below:

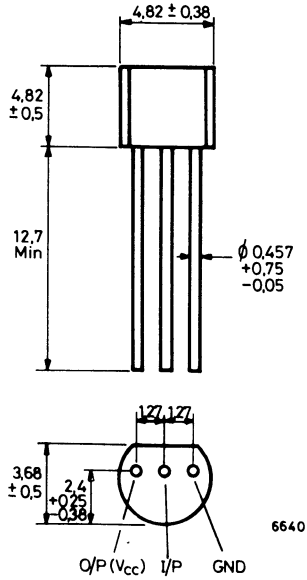


– 6dB Bandwidth = 6kHz
– 30dB Bandwidth = 8kHz
AGC Range ≈ 40dB
(For 10dB change in A.F. output).

FURTHER APPLICATIONS

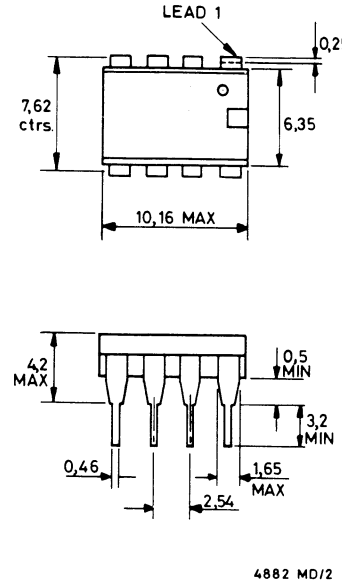
The ZN414Z is an extremely versatile device and, in a data sheet, it is not possible to show all its varied applications. A comprehensive applications note on the device is available which gives full details of various radio receivers, I.F. amplifiers and frequency standards together with comprehensive technical information.

PACKAGE OUTLINE (ZN414Z)



TO-92

PACKAGE OUTLINE (ZN415E & ZN416E)



8 pin DIL

Dimensions in millimetres

ZN424

FERRANTI semiconductors

Gated Operational Amplifier

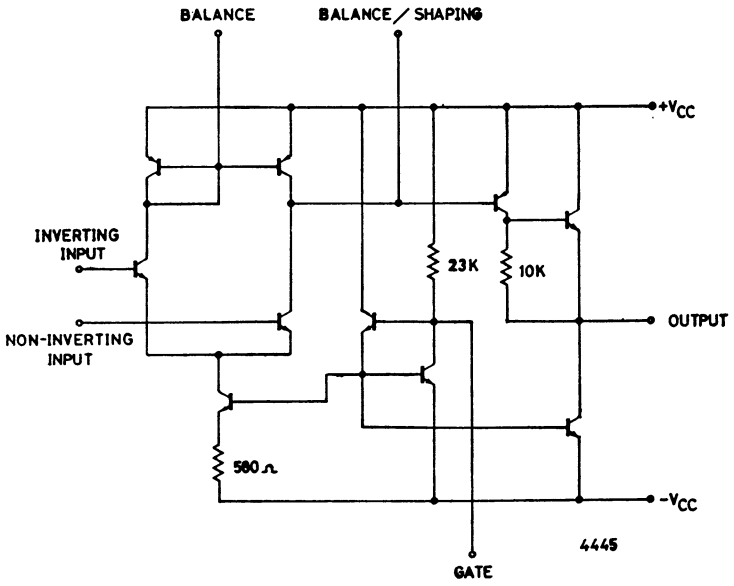
FEATURES

- 86 dB typical gain
- Very low open loop distortion
- Low noise ($e_n^2 = 4 \times 10^{-17}$ V²/Hz; 100 Hz to 20 kHz)
- 200 kΩ input resistance
- 20 kHz open loop bandwidth (–3 dB)
- 0·1 μs closed loop rise time
- Class A output stage
- 100 V/μs slew rate (rising edge)
- Maximum output swing ±11 volts, ±17V at $V_{CC} = \pm 18$V
- Operation at 5 volts, TTL compatible
- Logic gate current drive capability
- Input-output isolation gating facility

GENERAL DESCRIPTION

The ZN424 is a versatile linear amplifier designed to satisfy the growing requirement for high quality signal processing. As a voltage amplifier the very low distortion and low noise performance makes the device ideally suited for audio applications. The gating facility, coupled with the ability to operate from a TTL supply, gives the device broad appeal in the instrumentation, computing and allied fields. The device is readily stabilised using an external capacitor, or capacitor/resistor combination.

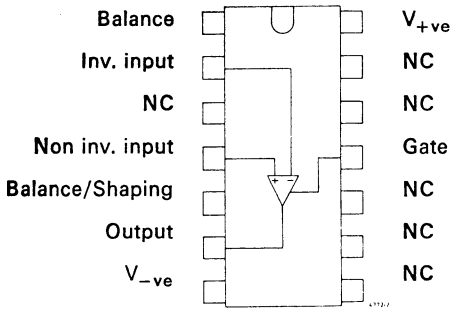
CIRCUIT DIAGRAM



PIN CONFIGURATION

Dual in-line packages

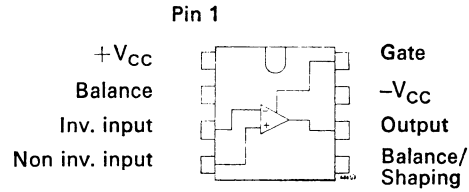
Pin 1

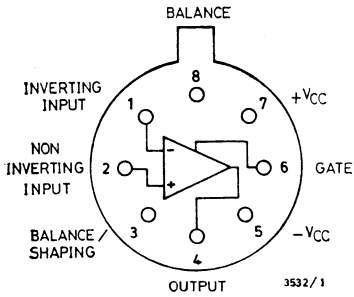


ZN424E
(14 lead Moulded Dual in-line)

ZN424P
(8 lead Moulded Dual in-line)

Pin 1





ZN424T
(8 lead Metal Can)

All packages viewed from top

ABSOLUTE MAXIMUM RATINGS

Supply voltage	±18 volts
Internal power dissipation (DIL)*	250 mW
Internal power dissipation (TO-39)	300 mW
Differential input voltage	5 volts
Storage temperature range	−65°C to +125°C

*Derating above 55°C = 5·6 mW/°C., 8 pin derating above 55°C = 7·6 mW/°C.

RECOMMENDED RATINGS

Supply voltage range	±2 to ±18 volts
Operating temperature range	0°C to +70°C

ZN424

ELECTRICAL CHARACTERISTICS

($V_S = \pm 12V$, Load = 20 kΩ, $T_{amb} = 25°C$ unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units
Input Offset Voltage		2	6	mV
Input Current		0·5	1·2	μA
Input Offset Current		0·1	0·5	μA
Input Offset Voltage Drift		5		μV/°C
Input Current Drift		2·0		nA/°C
Input Offset Current Drift		0·4		nA/°C
Input Resistance		200		kΩ
Output Resistance		4		kΩ
Voltage Gain	10,000	20,000		
Mutual Conductance		5		A/V
Common Mode Range	±10	±11		V
Output Voltage Swing	±10	±11		V
Maximum Negative Output Current (Load = 1 kΩ)		3·0		mA
Supply Current		5·5	7·0	mA
Open Loop Bandwidth (–3 dB)		20		kHz
Unity Gain Bandwidth (–3 dB) (0·01 μF used as shaping capacitor, see Note 2)		4		MHz
Common Mode Rejection Ratio	70	100		dB
Supply Rejection Ratio	80	85		dB
Unity Gain Risetime (Slew-Rate 4V/μs)		0·1		μs
Unity Gain Overshoot (0·022 μF, 22Ω)		10		%
Output Leakage Current (Gated Off)		5	30	nA
Voltage Gain $V_S = \pm 2·5V$, 3·3 kΩ between Gating Input and $+V_{CC}$, Load = 10 kΩ	5,000	12,000		
Slew Rate Rising Edge		100		V/μs
Slew Rate Falling Edge		12		V/μs
Open Loop Distortion (2V ptp swing)		<1·5		%T.H.D.
Open Loop Distortion (10V ptp swing)		6		%T.H.D.

OPERATING NOTES

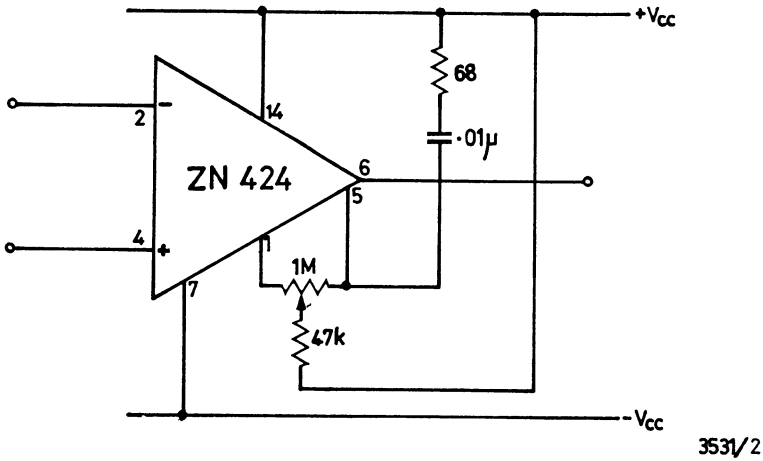
1. When operating with low supply voltages the output bias current may be maintained at about 3 mA by connecting an external resistor between the gating input and $+V_{CC}$. Under these conditions the output current is given approximately by:

$$I_C = \frac{(V_{CC} - 1 \cdot 4) \times 3}{R}$$

R is the parallel combination of the external and internal (23 kΩ) resistors.

2. Unity gain frequency stability is achieved by connecting a 0·01 μF capacitor and a 68Ω resistor in series between 'shaping' and $+V_{CC}$.

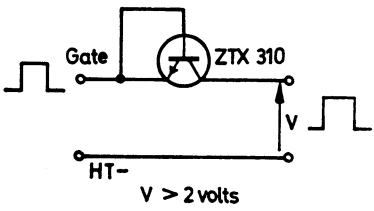
3. Input Offset Voltage is nullified by connecting a 1 MΩ potentiometer between 'balance' and 'balance/shaping' with the wiper connected through a 47 kΩ resistor to $+V_{CC}$.

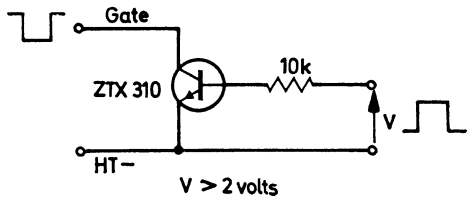


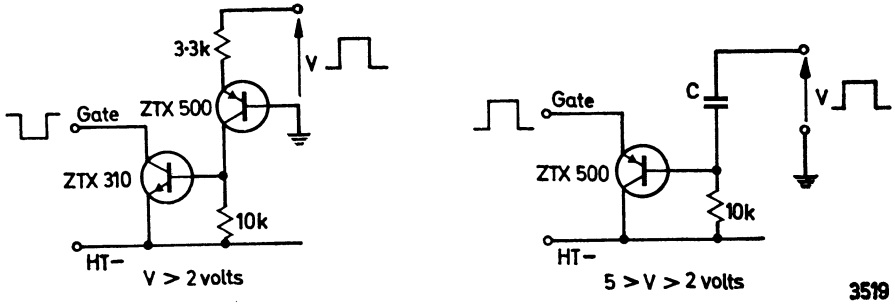
Offset and Frequency Compensation Circuit

(14 Lead pinning indicated)

4. The ZN424 is gated 'off' by shunting the current source bias current to the negative rail. Four methods of gating the ZN424 are illustrated below, two of which require a drive voltage with respect to the negative rail (e.g. from another ZN424 or from logic, when using a single supply), and the other two allowing the drive pulse to be with respect to earth or another convenient point.





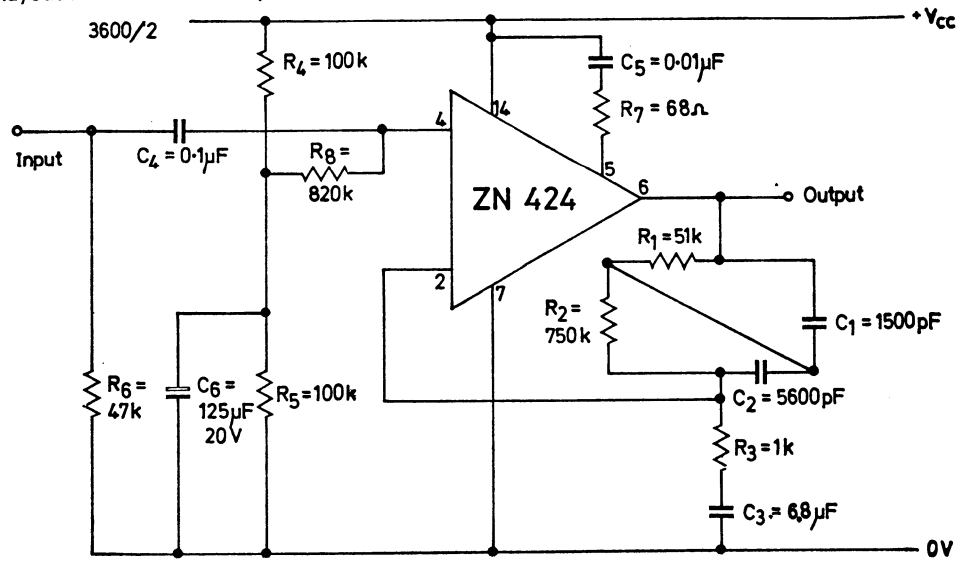


5. When gated off, the inputs become effectively, representable by a 1 pF capacitor to the output.

APPLICATIONS

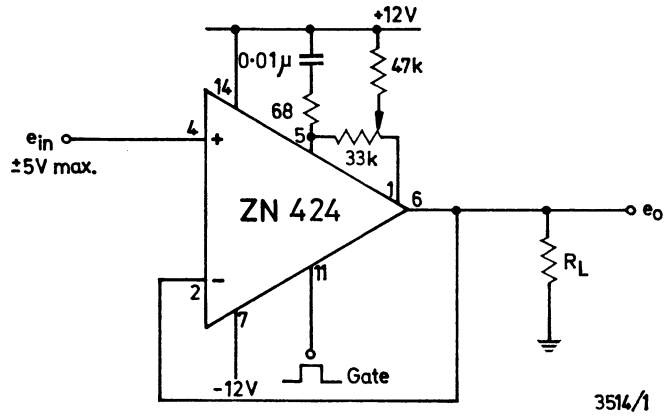
1. Magnetic cartridge (R.I.A.A.) preamplifier:

The open loop gain of the ZN424 is 20,000 (86 dB) and the open loop distortion is, typically, 1·5% corresponding to a 2 volt peak output swing (this is the maximum output ever likely to be encountered from a magnetic cartridge). To feed most power amplifiers a voltage gain, at 1 kHz, of 50 (34 dB) is necessary between cartridge and amplifier. Thus by applying 52 dB of feedback (86 dB to 34 dB) the distortion figure at 1 kHz becomes 0·004%. If more gain is required R_3 may be made smaller but C_3 must be increased proportionately to avoid loss of bass. $C_1C_2R_1R_2$ provide R.I.A.A. equalisation, and in addition C_3 and R_3 provide an effective rumble filter. C_5 and C_7 provide stability for all supply voltages. Assuming a 30 volts supply the overload factor of the circuit is ≃ 40 dB referred to a 5 mV input. The signal to noise ratio is better than 70 dB below a 5 mV input. The layout of the circuit is unimportant.



Magnetic cartridge preamplifier circuit
(14 Lead pinning indicated)

2(a) X1 Non-inverting Amplifier:



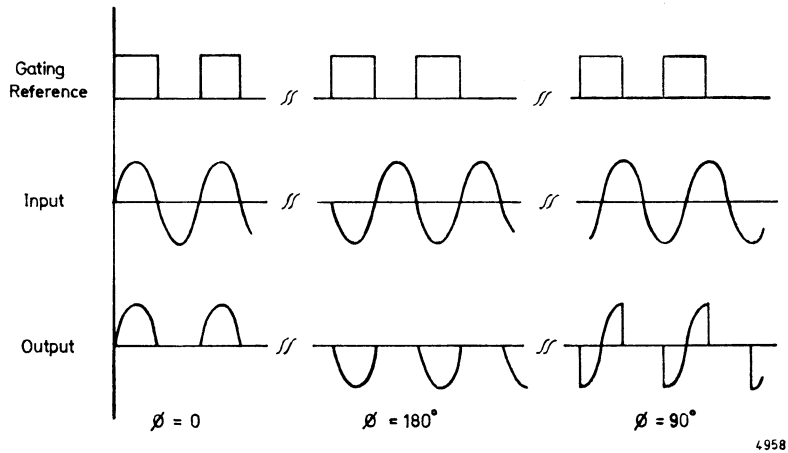
(14 Lead pinning indicated)

The circuit diagram is shown above. Feedback is applied in the normal way. When the amplifier is gated 'off' the input and output become open circuited as long as the maximum differential input voltage is not exceeded. This limits the input voltage range to ±5V. This may be effectively increased by attenuating the input suitably and defining the gain of the amplifier to give an overall gain of unity. An attenuator of 47 kΩ and 10 kΩ requires $R_F = 47\ k\Omega$, $R_S = 10\ k\Omega$ to give an overall gain of unity.

This method has the disadvantage of requiring four accurate resistors and giving a higher output offset voltage (unless an offset control is used) and lower input resistance (57 kΩ). However, the settling time is reduced from about 30 μsecs to 1 μsec. since a 10 pF shaping capacitor between pins 5 and 6 can be used.

By applying a square wave to the gating point, an output may be obtained which is an amplified square wave modulated version of the input.

2(b) Rectification/Demodulation (no transformers necessary):



The previous circuit may be used as a half-wave phase sensitive detector by applying a square wave reference voltage to the gating point and a phase related signal to the input. Typical waveforms are illustrated above for phase differences (⌀) of 0, 90 and 180 degrees..

The mean d.c. output level is proportional to R cos⌀, where R is the input amplitude. For a half-wave detector with a gain of A:

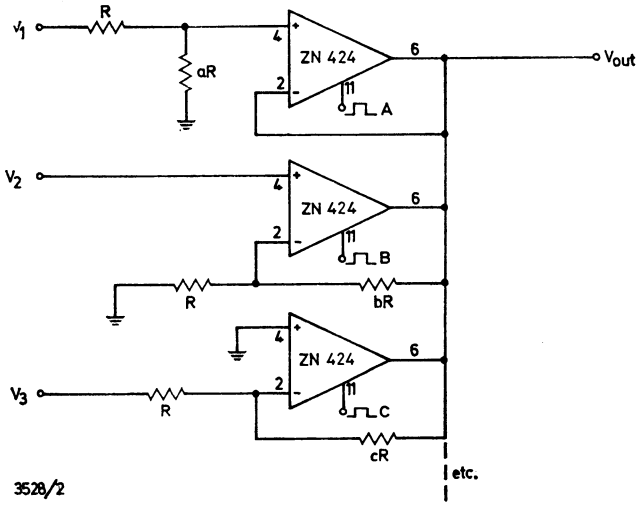
$$\overline{e_O} = \frac{AR\cos\varnothing}{\pi}$$

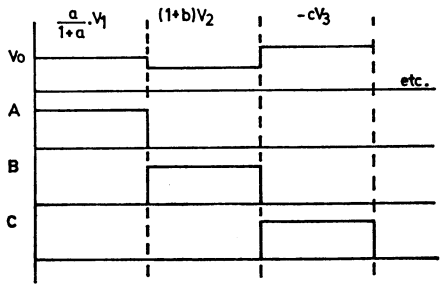
Using two phase sensitive detectors driven from square wave reference voltages 90 degrees out of phase, outputs proportional to Rcos⌀ and Rsin⌀ may be obtained. If these voltages are applied to the X and Y plates of a cathode ray tube the spot will describe the polar plot (R,⌀). Nyquist plots may thus be obtained directly.

The square wave reference voltages may be generated using a ring counter.

3. Multiplexing:

A ring counter is used to provide a gating pulse to enable the ZN424 to give a multiplexed output as shown below.

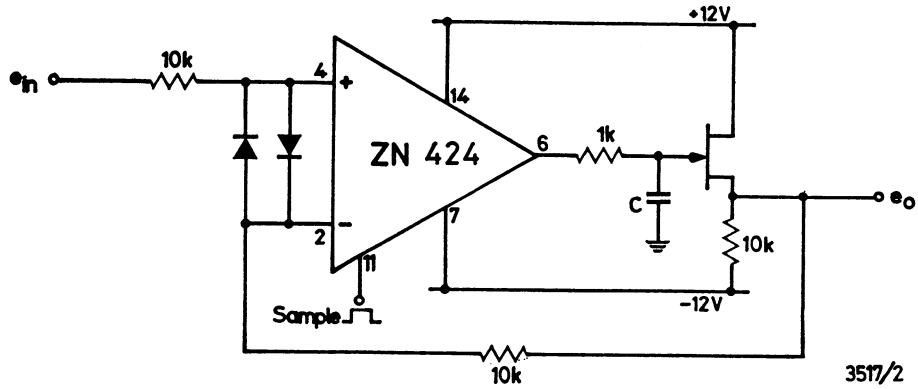




(14 Lead pinning indicated)

4. Sample and Hold Circuits:

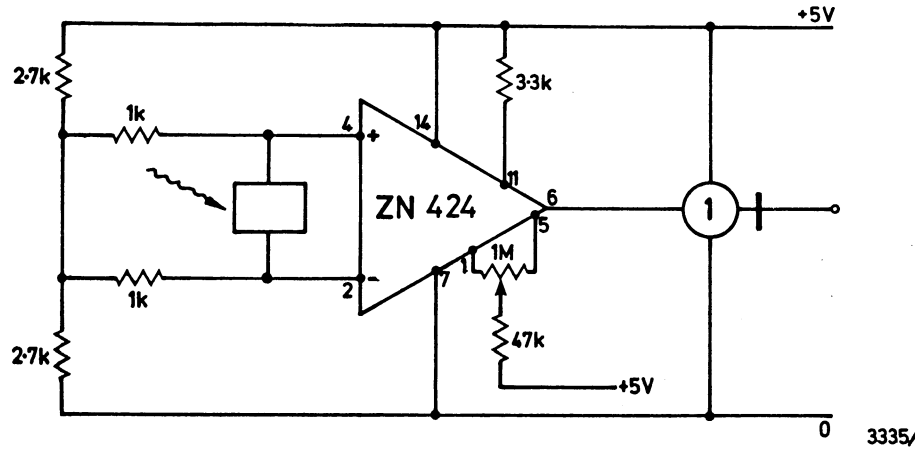
A typical circuit is shown below. The output voltage, e_O, is determined by the choice of feedback resistor when the ZN424 is gated 'on'. When gated 'off', e_O is held for a time, which is dependent on 'C', the leakage of the FET and the ZN424. The value of the capacitor also determines the sampling time necessary. Integrator/Reset circuits can readily be derived from this type of circuit.



(14 Lead pinning indicated)

5. Photocell Trigger Circuit Driving TTL Gate(s):

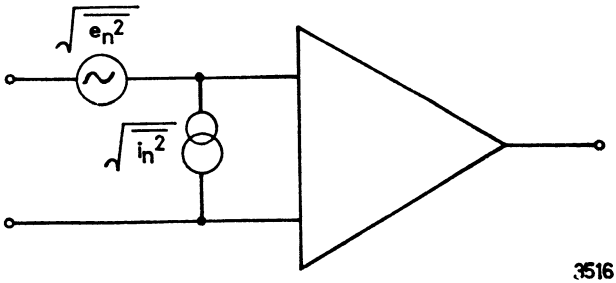
A typical circuit is shown below. The input is biased, so the output is low, when the photocell is irradiated. With no output from the photocell the output is high. The photocell used below gave an output of 60 mV, 30 μA when irradiated. In this type of circuit the gating facility can be used to switch various combinations of photoelectric, encoder/decoder circuitry.



(14 Lead pinning indicated)

NOISE

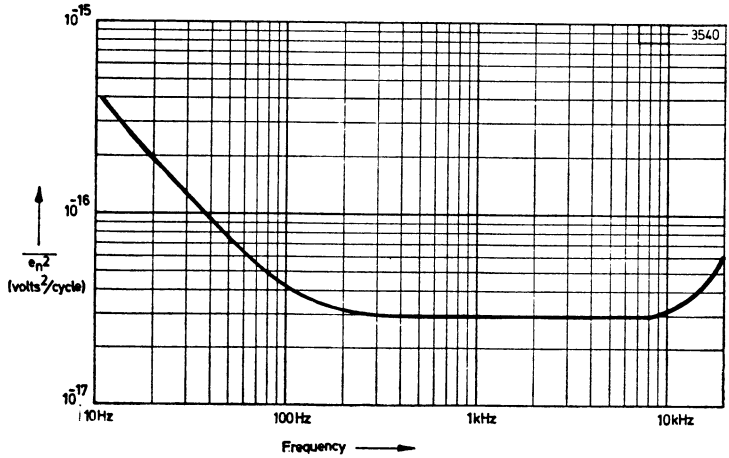
An amplifier always generates noise. At low frequencies flicker noise predominates and increases inversely with the frequency (though presumably not indefinitely). At a sufficiently high frequency this source of noise becomes insignificant compared with shot noise. This is white noise, i.e., has a constant energy/cycle.

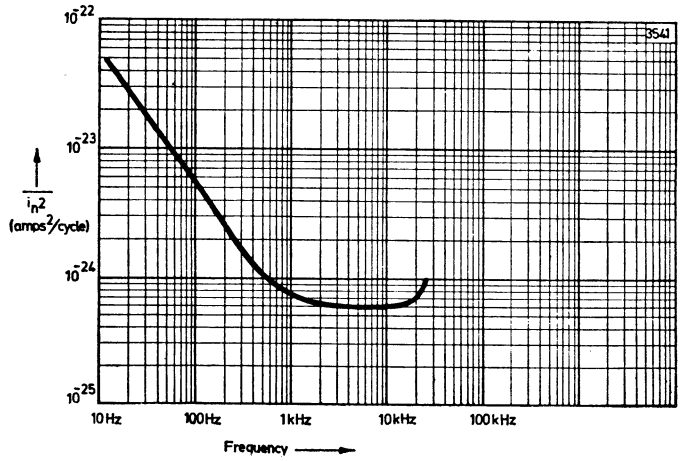


Any amplifier may be represented by an ideal amplifier with equivalent noise voltage and current generators at the input as shown above. The mean square noise voltage is shown as $\overline{e_n^2}$ volts^2/cycle and the mean square noise current as $\overline{i_n^2}$ amps^2/cycle. The noise voltage may be measured by short-circuiting the input so that no noise current flows into the amplifier. When the input terminals are open-circuited all the noise current flows into the amplifier and the noise voltage generator is open-circuited. The noise that appears at the output of the amplifier will obviously depend upon the shape of the frequency response. If the frequency response is measured the noise measured at the output may be referred back to the input. This is shown below where $\overline{e_n^2}$ and $\overline{i_n^2}$ are plotted against frequency. In an actual case, a source resistance R_S will be connected across the input terminals.

This resistance will itself generate white noise known as Johnson noise of magnitude $\overline{e_r^2} = 4\,kTR_S$ volts^2/cycle, where k is the Boltzmann constant and T is the absolute temperature. The noise current flowing in this resistance will also produce a mean square noise voltage of $\overline{i_n^2}\,R_S^2$ volts^2/cycle.

TYPICAL CHARACTERISTICS





Graph 1. $\overline{e_n^2}$ and $\overline{i_n^2}$ against frequency for ZN424.

Stabilizing the ZN424 in various gain configurations.

The ZN424 is designed such that any resistive feedback circuit can be stabilized with less than 50% overshoot using $C_1 = 0{\cdot}1\ \mu F$.

Closed loop gain	R_F	C_F	R_1	C_1	C_2
100 and above	10 kΩ	—	—	—	—
50	10 kΩ	5 pF	—	—	—
50	10 kΩ	—	—	—	2·2 pF
20	10 kΩ	—	—	—	5 pF
10	10 kΩ	5 pF	270Ω	1000 pF	—
5	10 kΩ	5 pF	100Ω	2200 pF	—
2	10 kΩ	5 pF	39Ω	0·01 μF	—
1	0	—	22Ω	0·022 μF	—

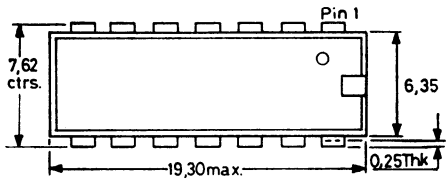
R_1/C_1 are connected in series between pins 5 and 14 (14 pin DIP)
pins 5 and 1 (8 pin DIP).

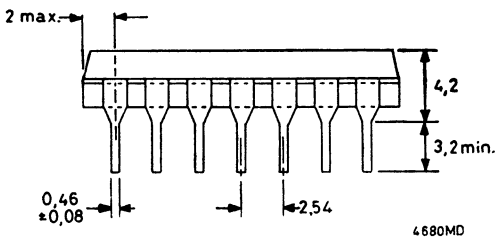
C_2 is connected between pins 5 and 6 (14 pin DIP)
pins 5 and 6 (8 pin DIP).

ZN402 Gated Op-Amp.

The ZN402 series is electrically similar to the ZN424 series, and the devices can be interchanged with each other. However, because the testing procedure is more rigorous for the ZN424, the noise performance and gain is often consistently better than the ZN402.

PACKAGE OUTLINES

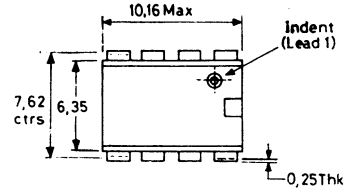


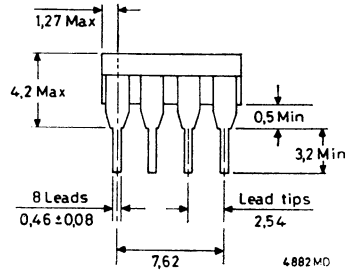


ZN424E

14–Lead Moulded D.I.L.

Conforms to: Vasca SO-87 Type A
JEDEC TO-116

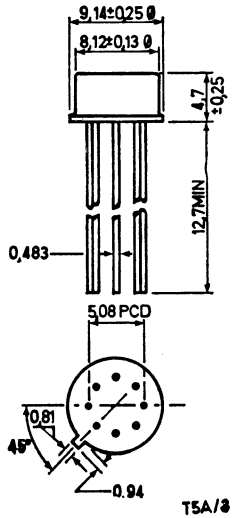




ZN424P

8–Lead Moulded D.I.L.

Conforms to SO-87 Type D



ZN424T

8–Lead Metal Can

SO-44B
SB8-7B

Dimensions in millimetres

ZN459
ZN459C
ZN459CP

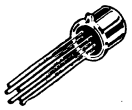
FERRANTI semiconductors

Ultra Low Noise Amplifier

FEATURES

- **High Controlled Gain** : **60 dB ±1 dB typical**
- **Low Noise** : **40Ω Equivalent Noise Resistance, or 800 pV/√Hz**
- **Wide Bandwidth** : **15 MHz typical**
- **Low Supply Current** : **<3 mA from 5V**

ZN459/ZN459C



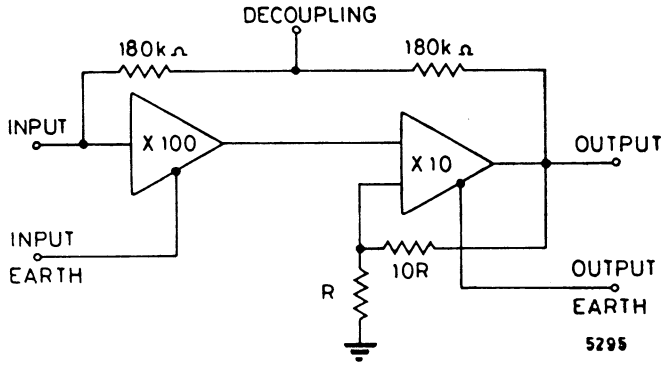
TO-71

ZN459CP

8-Lead D.I.L.

DESCRIPTION

A versatile high grade a.c. pre-amplifier designed for applications requiring ultra low noise such as infra-red imaging and low noise wide band amplifiers e.g. microphone, acoustic emission, transducer bridge amplifier. The matching of open loop gain coupled with small physical size make the ZN459 series ideal for multichannel amplification.



ZN459 OUTLINE CIRCUIT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .. .. 6·0 Volts

Operating Temperature Range:
for ZN459 .. .. –55 to +125°C
for ZN459C and ZN459CP .. .. .. 0 to +70 °C

Storage Temperature Range .. .. .. –55 to +125°C

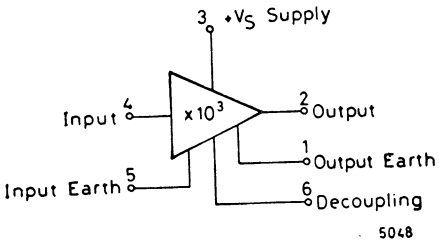
CHARACTERISTICS (at V_{CC} = 5V, T_{amb} = 25°C).

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Current	2·0	2·5	3·0	mA	
Voltage Gain	59	60	61	dB	10 kHz
TC of Voltage Gain	—	–0·2	—	%/°C	
V_{CC} Coefficient of Voltage Gain	—	25	—	%/V	
Cut-off Frequency	—	15	—	MHz	3 dB down
Input Resistance	3·5	7	—	kΩ	10 kHz
Input Capacitance	—	80	—	pF	Note 1
Noise Resistance	—	40	—	Ω	$R_S = 0$
White Noise Voltage	—	800	1100	$pV/\sqrt{Hz}$	$R_S = 0$
L.F. Spot Noise	—	3	—	$nV/\sqrt{Hz}$	$R_S = 0$, f = 25 Hz
White Noise Current	—	1	—	$pA/\sqrt{Hz}$	
Output Level	1·5	2·0	2·5	V	
Supply Voltage Coefficient of Output Level	—	0·34	—	V/V	
Output Current Limit	0·6	0·8	1·1	mA	Sink current
Total Harmonic Distortion ..	—	0·15	—	%	1 V_{pp} at 10 kHz
Output Resistance	—	75	—	Ω	10 kHz
Supply Rejection Ratio ..	—	42·5	—	dB	
Delay Time	—	20	—	ns	Small signal
Delay Time	—	40	—	ns	100 mV rms input
Positive Input Overdrive ..	—	10	—	mA	
Negative Input Overdrive ..	—	–5	—	V	

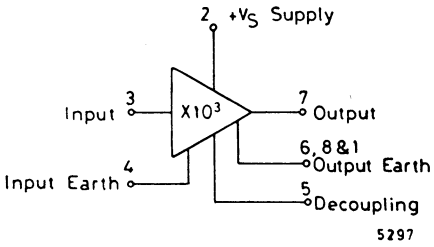
Note 1: In P.C.B. The Input Capacitance may be reduced to 25pF by screening between output and input.

ZN459 Series

PINNING CONFIGURATIONS

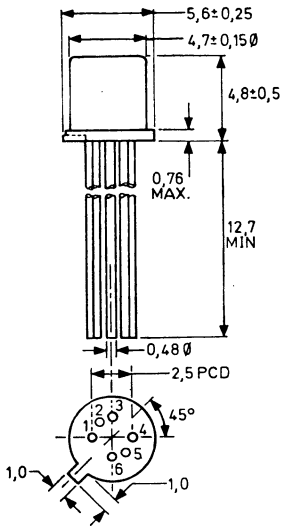


METAL CAN

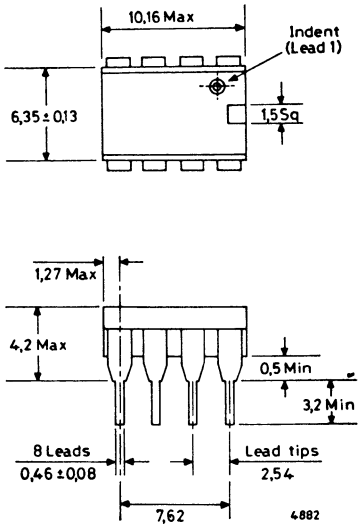


P PACKAGE

PACKAGE DETAILS



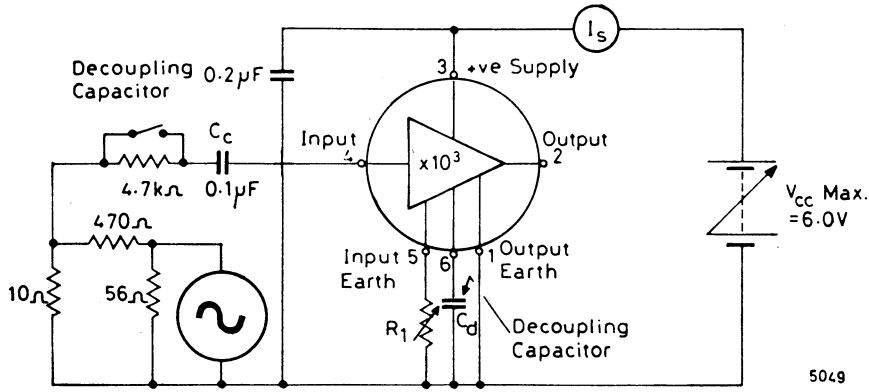
TO-71 (6 lead TO-18)



8 PIN PLASTIC DUAL IN-LINE

Dimensions in millimetres

GAIN TEST CIRCUIT (Metal Can)

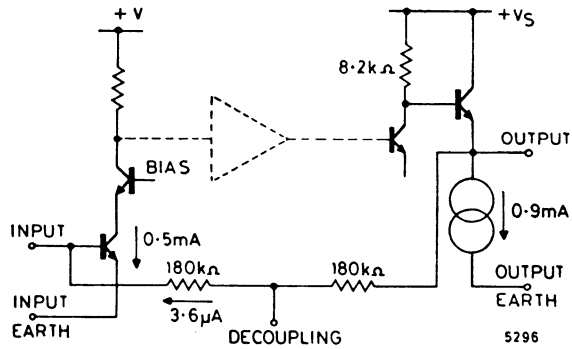


The input impedance may be increased at the expense of noise by including R_1 to vary the gain ($R_1 = 0$, gain $= 10^3$; $R_1 = 470\Omega$, gain $= 10^2$).

C_d is required to decouple the internal feedback loop and in order to obtain a flat frequency response make $C_d \geqslant C_c$.

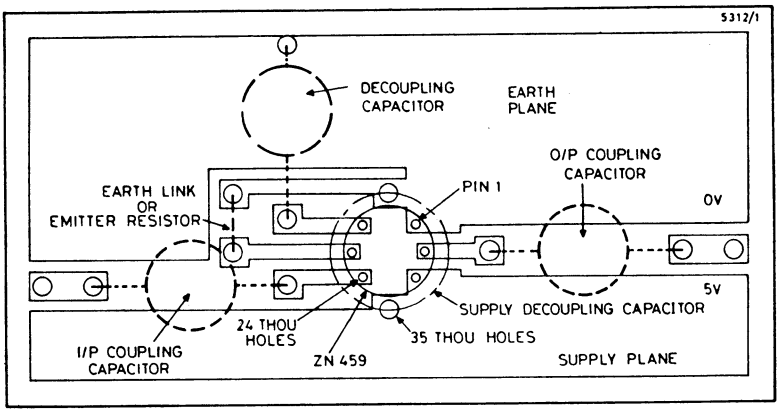
The earth lead of the supply decoupling capacitor should be as close as possible to that of R_1.

For optimum Common Mode Rejection connect a twisted pair between source and pins 4 and 5 of the device, and complete the earth return from source ground.

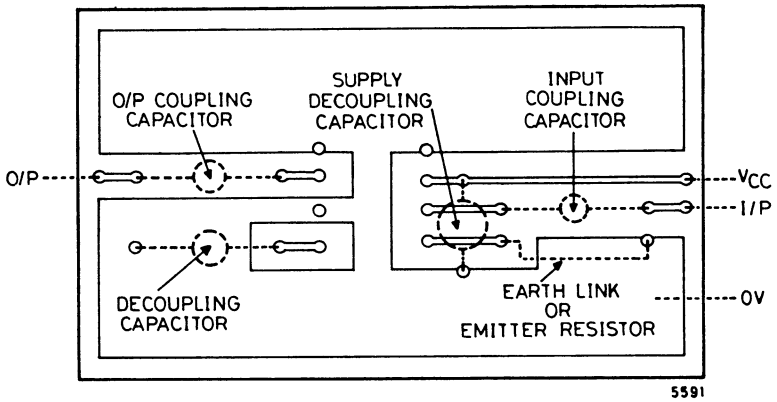


ZN459 INPUT AND OUTPUT CIRCUIT

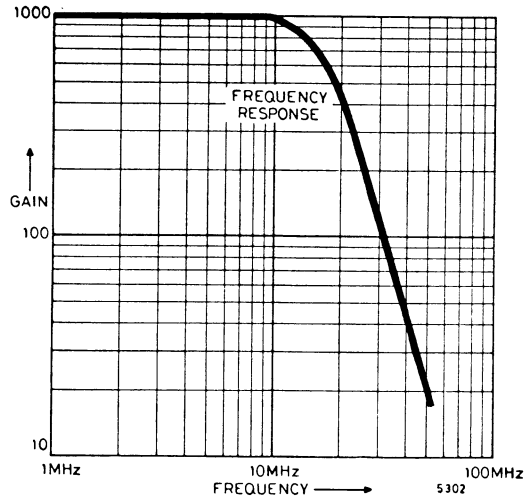
P.C.B. LAYOUT (Metal Can)



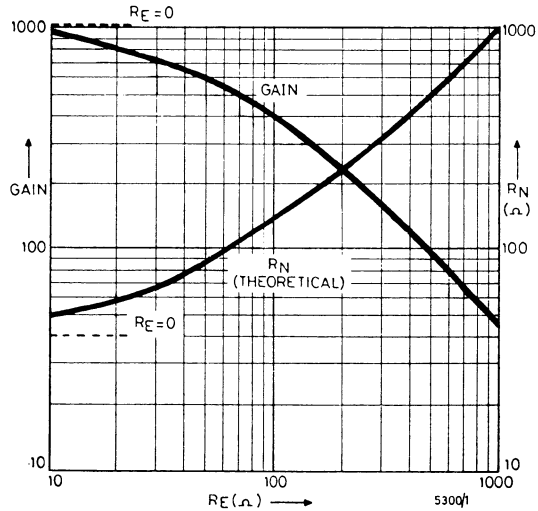
P.C.B. LAYOUT (Plastic D.I.L.)



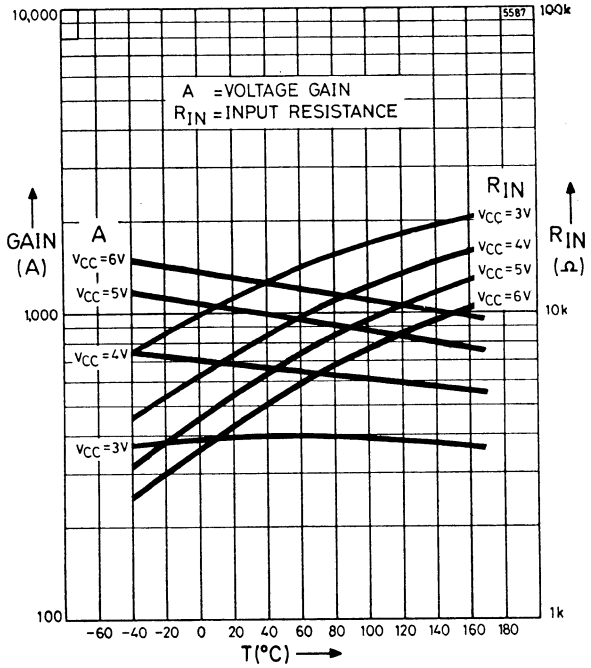
TYPICAL CHARACTERISTICS



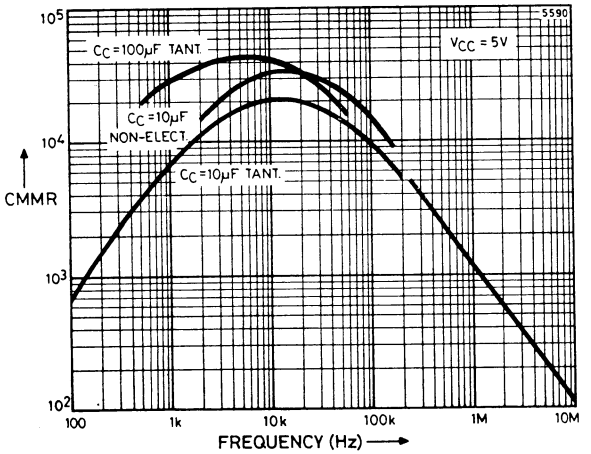
GAIN V_S FREQUENCY



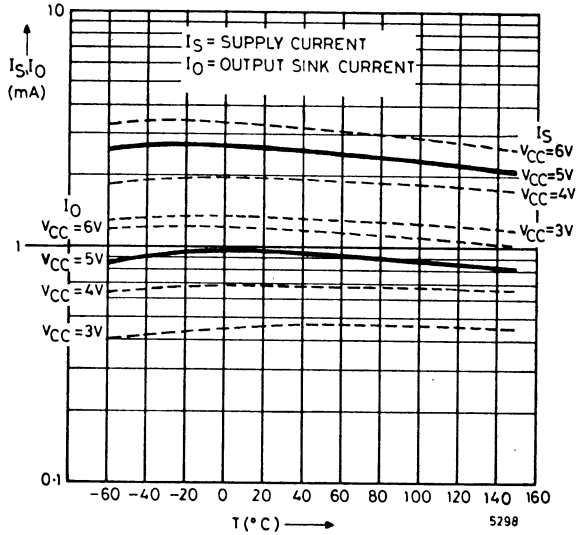
GAIN AND NOISE RESISTANCE V_S EMITTER RESISTANCE



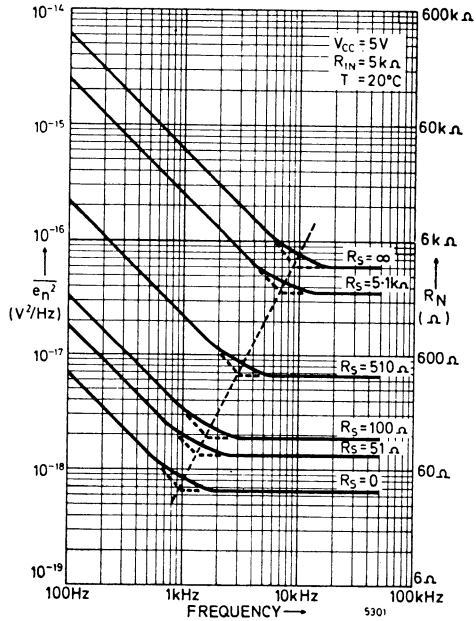
GAIN AND INPUT IMPEDANCE



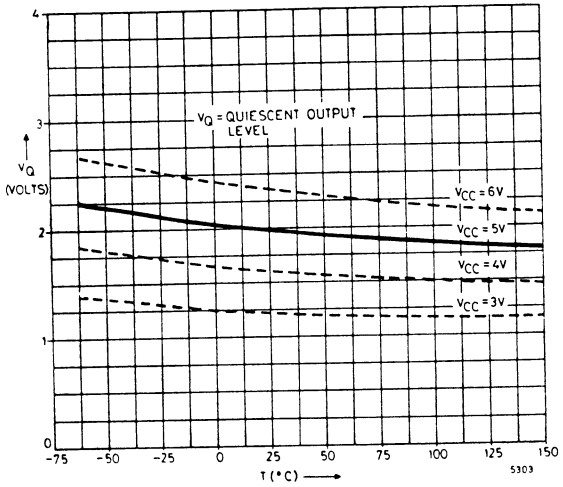
COMMON MODE REJECTION Vs FREQUENCY
(Measured between input earth and output earth)



SUPPLY CURRENT AND OUTPUT SINK CURRENT



NOISE VOLTAGE



QUIESCENT OUTPUT LEVEL

FERRANTI semiconductors

ZN460 Series

Ultra Low Noise Preamplifier

FEATURES

- **High Controlled Gain** : **60 dB ± 1 dB typical**
- **Programmable Gain** : **50-60 dB typical**
- **Programmable Bandwidth** : **6MHz downwards**
- **Low Noise** : **40Ω Equivalent Noise Resistance, or 800 pV/$\sqrt{Hz}$**
- **Low Supply Current** : **<3 mA from 5V**

ZN460/ZN460C

TO-78

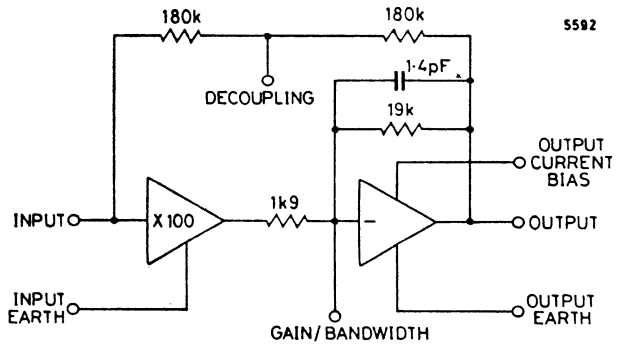
ZN460CP

8-Lead D.I.L.

DESCRIPTION

A versatile high grade a.c. pre-amplifier designed for applications requiring ultra low noise such as infra-red imaging and low noise wide band amplifiers e.g. microphone, acoustic emission, transducer bridge amplifier. The matching of open loop gain coupled with small physical size make the ZN460 series ideal for multichannel amplification.

The programmable gain feature allows variable detector gain factors to be trimmed out. The programmable bandwidth feature allows the noise bandwidth to be reduced to the required signal bandwidth thus minimising the wideband output noise.



CIRCUIT DIAGRAM

ZN460 Series

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .. .. 6.0 Volts

Operating Temperature Range:

for ZN460 .. .. –55 to +125°C

for ZN460C and ZN460CP .. .. .. 0 to +70 °C

Storage Temperature Range .. .. .. –55 to +125°C

CHARACTERISTICS (at V_{CC} = 5V, T_{amb} = 25°C).

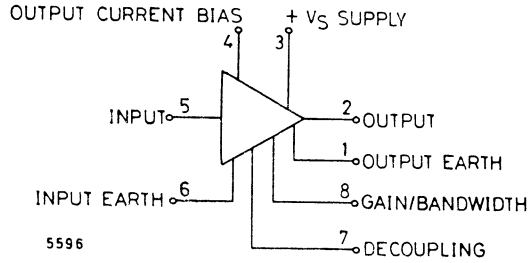
Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Current	2.0	2.5	3.0	mA	
Voltage Gain	59	60	61	dB	10 kHz (Note 1)
TC of Voltage Gain	—	–0.2	—	%/°C	
V_{CC} Coefficient of Voltage Gain	—	25	—	%/V	
Cut-off Frequency	—	6	—	MHz	3 dB down (Note 1)
Input Resistance	3.5	7	—	kΩ	10 kHz
Input Capacitance	—	80	—	pF	Note 2
Noise Resistance	—	40	—	Ω	$R_S = 0$
White Noise Voltage	—	800	1100	$pV/\sqrt{Hz}$	$R_S = 0$
L.F. Spot Noise	—	3	—	$nV/\sqrt{Hz}$	$R_S = 0$, f = 25 Hz
White Noise Current	—	1	—	$pA/\sqrt{Hz}$	
Output Level	1.5	2.0	2.5	V	
Output Swing	— 2	4 —	— —	V_{pp} V_{pp}	$R_F = \infty$ R_F = 6 kΩ
Supply Voltage Coefficient of Output Level	—	0.34	—	V/V	
Output Current Limit	0.6	0.8	1.1	mA	Note 3
Total Harmonic Distortion ..	—	0.15	—	%	1 V_{pp} at 10 kHz
Output Resistance	—	75	—	Ω	10 kHz
Supply Rejection Ratio ..	—	42.5	—	dB	
Delay Time	—	20	—	ns	Small signal
Delay Time	—	40	—	ns	100 mV rms input
Positive Input Overdrive ..	—	—	10	mA	
Negative Input Overdrive ..	—	—	–5	V	

NOTE 1. Without external components.

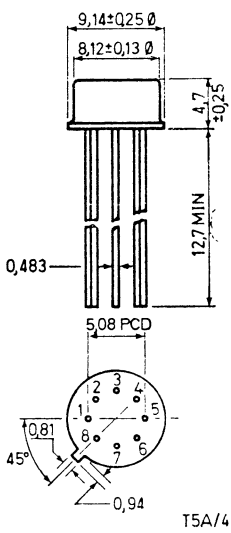
NOTE 2. In P.C.B. The Input Capacitance may be reduced to 25 pF by screening between output and input

NOTE 3. Sink current without external bias resistor.

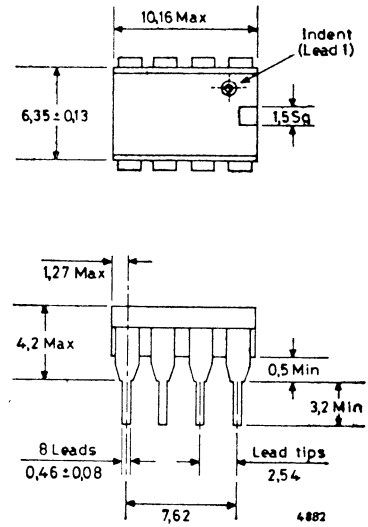
PINNING CONFIGURATIONS (Metal Can and P-Package)



PACKAGE DETAILS



TO-78 (8-lead TO-5)

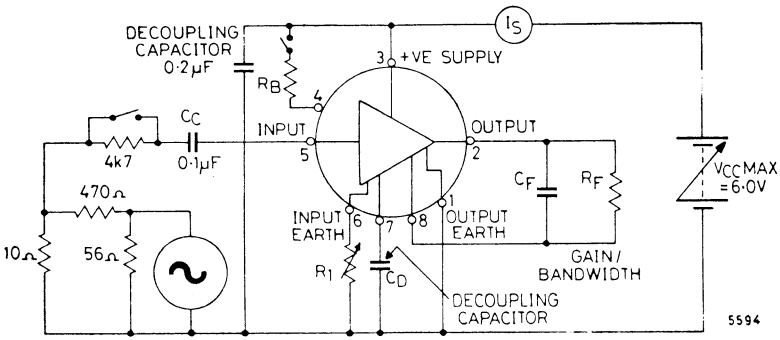


8 PIN PLASTIC DUAL IN-LINE

Dimensions in millimetres

ZN460 Series

GAIN TEST CIRCUIT (Metal Can)



The input impedance may be increased at the expense of noise by including R_1 to vary the gain ($R_1 = 0$, gain $= 10^3$; $R_1 = 470\Omega$, gain $= 10^2$).

C_D is required to decouple the internal feedback loop and in order to obtain a flat frequency response make $C_D \geqslant C_C$.

The earth lead of the supply decoupling capacitor should be as close as possible to that of R_1.

R_B may be used to increase the output quiescent current up to a maximum of 5 mA. The value is given by:

$$I_O = \frac{10(V_{CC} - 1.34)}{R_B'}$$

where R_B' is the parallel combination of R_B and 40 kΩ.

The gain and bandwidth may be modified by means of R_F and C_F. The gain is given by:

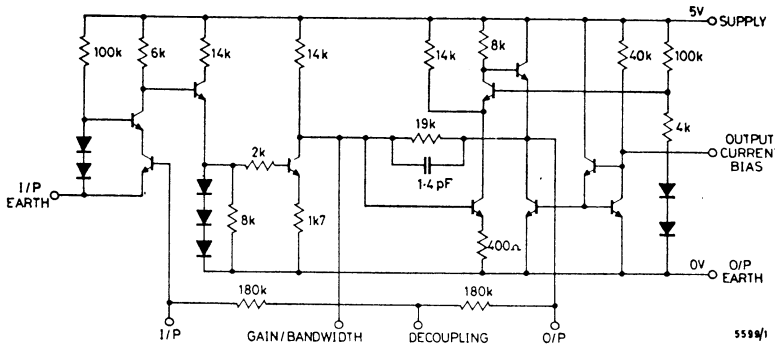
$$A = \frac{10^3 . R_F}{R_F + 19} \text{ with } R_F \text{ in k}\Omega$$

and the bandwidth by:

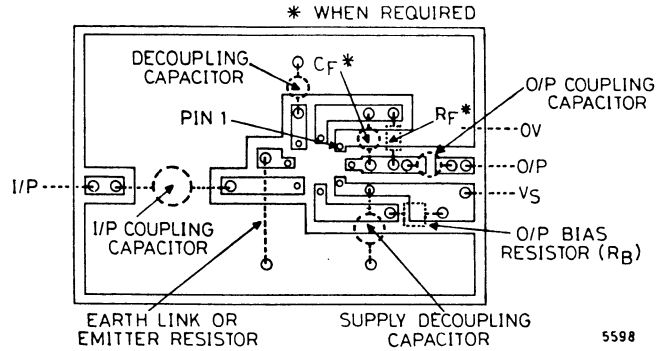
$$f_C = \frac{10^{12}}{2\pi R_F' (C_F + 1.4)} \text{ Hz with } C_F \text{ in pF}$$

where R_F' is the parallel combination of R_F and 19 kΩ.

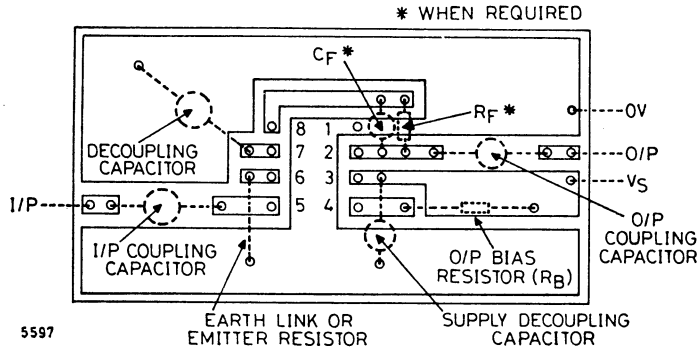
The recommended minimum value of R_F is 6 kΩ since a lesser value reduces the output swing below $2V_{pp}$.



ZN460 CIRCUIT DIAGRAM (Typical Values)



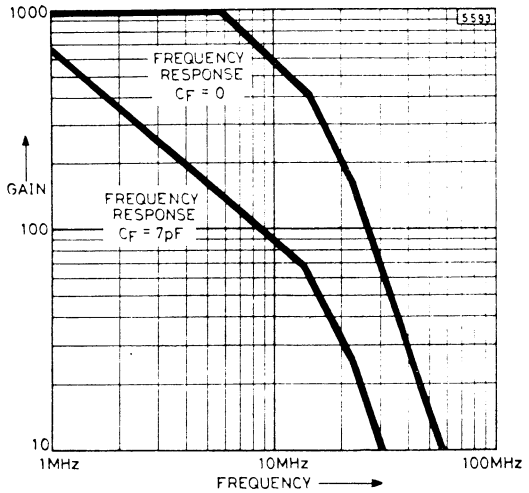
P.C.B. LAYOUT (Metal Can)



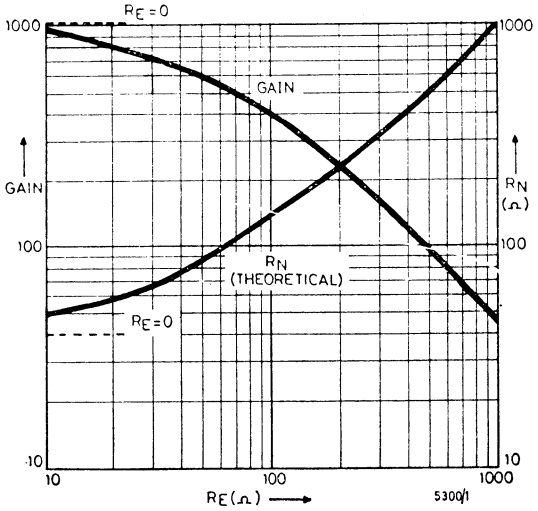
P.C.B. LAYOUT (P Package)

ZN460 Series

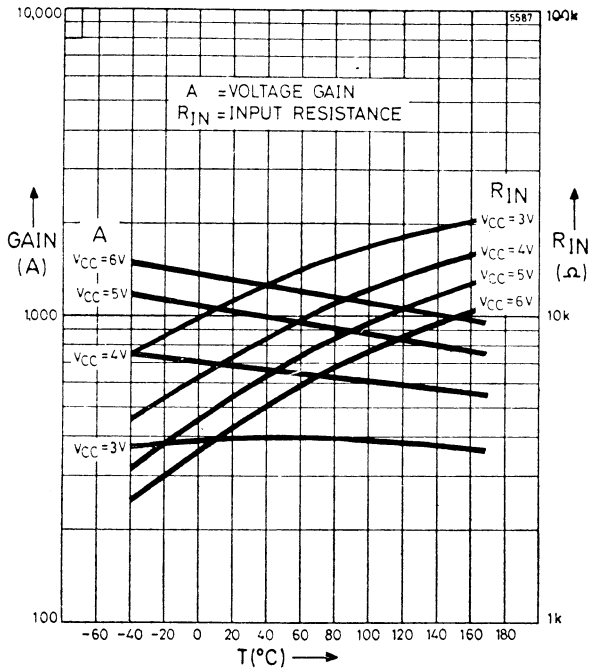
TYPICAL CHARACTERISTICS



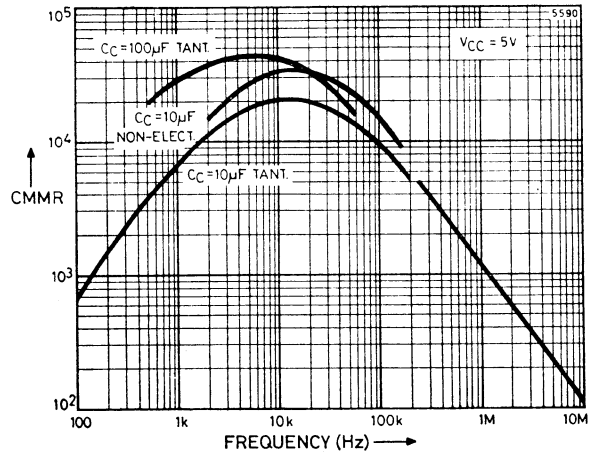
GAIN V_S FREQUENCY ($R_F = \infty$)



GAIN AND NOISE RESISTANCE V_S EMITTER RESISTANCE ($R_F = \infty$)

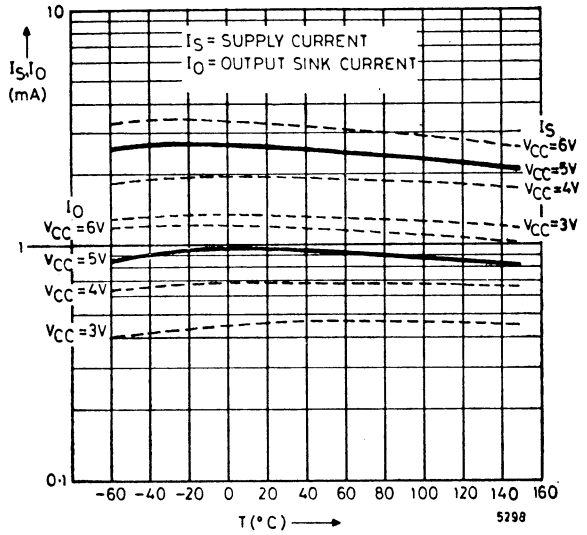


GAIN AND INPUT IMPEDANCE

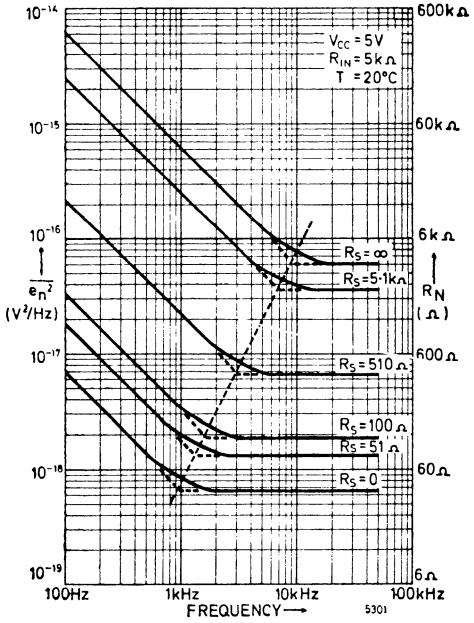


COMMON MODE REJECTION V_S FREQUENCY
(Measured between input earth and output earth)

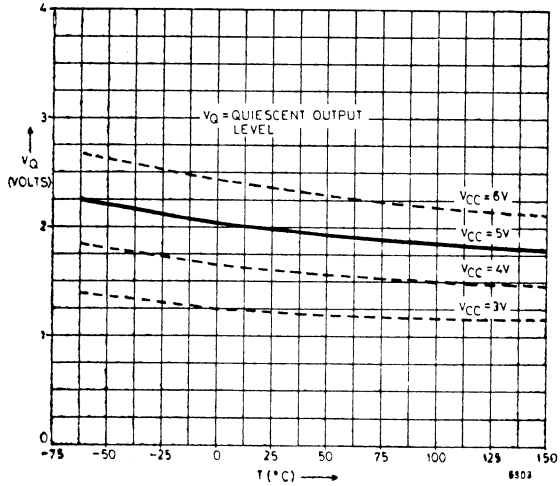
ZN460 Series



SUPPLY CURRENT AND OUTPUT SINK CURRENT ($R_B = \infty$)



NOISE VOLTAGE



QUIESCENT OUTPUT LEVEL

ZN490

FERRANTI semiconductors

Dual Pico-Ampere Diode

FEATURES

- **Ultra Low Leakage Diode**
- **Matched Forward Voltage Drop**
- **High Reverse Impedance**
- **Low Capacitance**

ABSOLUTE MAXIMUM RATINGS

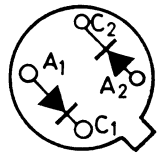
Reverse Voltage	7 Volts
Forward Current (each side)	5 mA
Total Power Dissipation	300 mW
Operating Temperature Range	−20 to +60°C
Storage Temperature Range	−55 to +150°C

ELECTRICAL CHARACTERISTICS (at 25°C ambient temperature unless otherwise stated).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Reverse current	I_R	—	0.5	2	pA	at 1V
Reverse voltage	V_R	6	—	—	V	at 1μA
Forward voltage drop	V_F	—	0.8	1	V	at 2 mA
Differential forward voltage drop	ΔV_F	—	1	5	mV	at 1 μA
Capacitance	C	—	2	—	pF	at 5V/1 MHz
Leakage current diode 1 to substrate	I_S	—	0.5	2	pA	at 1V*
Slope resistance of diode 2	R_F	—	40	100	Ω	at 1 to 2 mA

*Pin 1 connected to Pin 2.

PINNING DIAGRAM

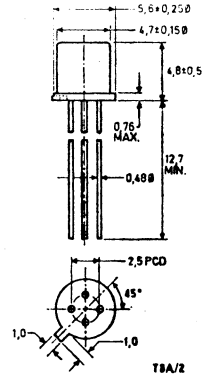


5653

Pin	Out
1	C_1
2	A_1
3	C_2
4	A_2

Substrate connected to pin 3

PACKAGE DETAILS



TO-72

Dimensions in millimetres

ZN1034E

FERRANTI semiconductors

Precision Counter Timer

FEATURES

- Time periods up to 7500 CR
- Time period trimming facility
- Repetitive timing 0.01%
- Temperature stability 0.01%/°C
- Complementary TTL compatible outputs
- Supply or Trigger input timing initiation
- On-chip regulator or TTL supply option

GENERAL DESCRIPTION

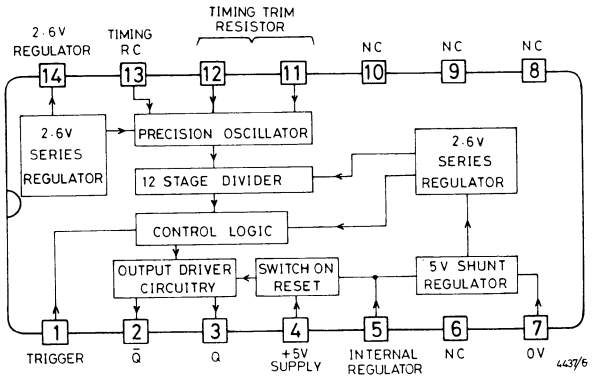
By combining complex linear and digital functions on the same chip, the ZN1034E enables the construction of simple precision timers using low cost components.

The frequency of an on-chip oscillator is determined by an externally connected capacitor and resistor. Fine adjustment of the frequency can be achieved by varying the value of an external trimming resistor. Pulses from the oscillator are fed into a 12 stage binary divider and the divider output changes state after 4095 pulses.

In this way precise time periods can be defined by timing capacitors and resistors of much smaller values than would be required by a single RC time constant timer.

A control circuit enables the division, or count, to begin when either (a) with trigger input LO the supply goes HI (supply initiation), or (b) with supply HI the trigger input goes LO (trigger initiation).

The I.C. can operate from normal +5V logic supplies or from any higher voltage by using a suitable voltage dropping resistor and by connecting the internal shunt regulator to the supply pin.



ABSOLUTE MAXIMUM RATINGS

Dissipation . . . . . 250 mW derate above 30°C at 5 mW/°C
Output Source Current . . . . . 25 mA
Output Sink Current . . . . . 25 mA
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −55°C to +125°C

ELECTRICAL CHARACTERISTICS (at 25°C ambient temperature)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Timing Section						
Timing Resistor	R_T	3k3		5M	Ω	See Figs. 4 and 5
Timing Capacitor	C_T	1			nF	See Figs. 4 and 5
Time Multiplying factor	K_o K_{50}		2800 3700			$R_{Trim} = 0$ $R_{Trim} = 50k$ $R_T > 12k$, $C_T > 33$ nF
Multiplying Factor Trim Resistor	R_{Trim}	0		500	kΩ	
Trimming Range	T_p		±50 ±25 ±12		% % %	R_{Trim} = 0 to 500k R_{Trim} = 0 to 100k R_{Trim} = 0 to 50k
Multiplying Factor Temperature Coefficient			+0.01 ±0.08		%/°C %/°C	$R_{Trim} = 0$ R_{Trim} = 500k
Repetitive Timing Error			0.01		%	
Multiplying Factor Linearity			±2		%	1 M > R_T > 12k See Fig. 5
Multiplying Factor/ Supply Voltage Coefficient			1		%/V	
External Clock Input						
Frequency				250	kHz	Clock input to Pin 12 via a 10k resistor
Drive Current	I_{clk}		0.1		mA	
Pulse Width	t_{clk}	1			µs	
Pulse Amplitude	V_{clk}	3.0		6	V	

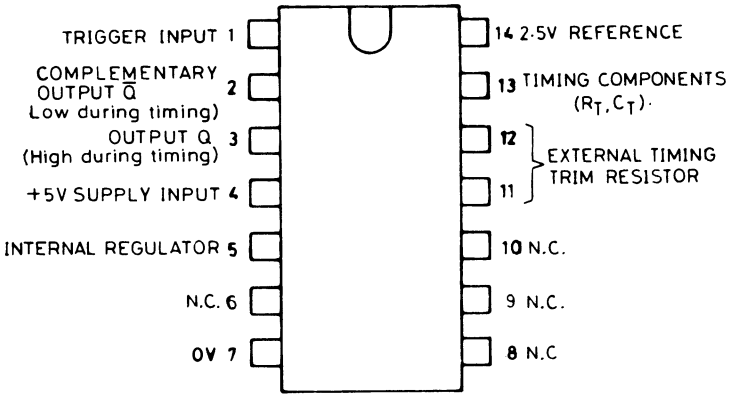
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Timing Initiation and Reset						
(a) *Supply Voltage Initiation*						
Voltage to initiate timing	V_{CC}	4.7			V	Supply applied to Pin 4 with Pin 1 connected to Pin 7
Rate of change of V_{CC}				0.25	V/μs	
(b) *Trigger Input Initiation*						
Voltage to initiate timing	$V_{T(LO)}$			1	V	Trigger input applied to Pin 1
Voltage to prevent initiation of timing	$V_{T(HI)}$	2.2			V	
Minimum pulse to trigger			2		μs	
(c) *Supply Voltage Reset*						
Voltage to Reset	V_{CC}		3.6		V	See Note 1
Output Drive Q and $\overline{Q}$						V_{CC} = 5V
Output Voltage	$V_{O(HI)}$ $V_{O(LO)}$	2.5	3.6 0.2	 0.4	V V	$I_{O(HI)}$ = 25 mA $I_{O(LO)}$ = –25 mA
Output Current	$I_{O(HI)}$ $I_{O(LO)}$			25 –25	mA mA	Source Sink
Rise Time	t_r		300		ns	I_O = 5 mA, V_{CC} = 5V
Fall Time	t_f		100		ns	I_O = 5 mA, V_{CC} = 5V
Propagation Delay V_T Low to V_O High	t_p		2		μs	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Supply						
(a) *Externally regulated*						Connected to Pin 4
Supply Voltage Supply Current	V_{CC} I_{CC}	4.7	5.0 3.5	5.3 5	V mA	$V_{CC} = 5V$ Outputs unloaded
(b) *Internally regulated* (5V Shunt regulator)						Connect Pin 4 to Pin 5
Operating Current Range	I_R	7		55	mA	See Note 2
Regulated Voltage	V_R	4.7	5.0	5.3	V	$I_R = 10$ mA
Slope Resistance			1		Ω	$I_R = 7 - 55$ mA
Regulated Voltage Change with temperature			35		mV	$I_R = 7 - 55$ mA $t = 0 + 70°C$
Reference Voltage						
(2.6V Series Regulator)						
Regulated Voltage	V_{REF}	2.4	2.6	2.8	V	$V_{CC} = 5V$ Pin 14 unloaded
Load Current	I_{REF}			5	mA	$V_{CC} = 5V$
Output Resistance			15	40	Ω	
Regulated Voltage Change with Temperature			10		mV	$V_{CC} = 5V$ $t = 0$ to $+70°C$ Pin 14 unloaded

Note 1. In order to reset the timer the supply voltage should be reduced to 2V although reset may be typically achieved at 3.6V. Reset will not occur with the supply greater than 4V.

Note 2. Since the +5V regulator cannot be used on its own without the rest of the circuit, the minimum operating current includes the 5 mA maximum supply current taken by the timer circuits.

ZN1034E



N.C. Not connected.

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ZN1034E

SECTION 1 THE TIMING FUNCTION

NOTE 1.1 FIXED TIME PERIOD

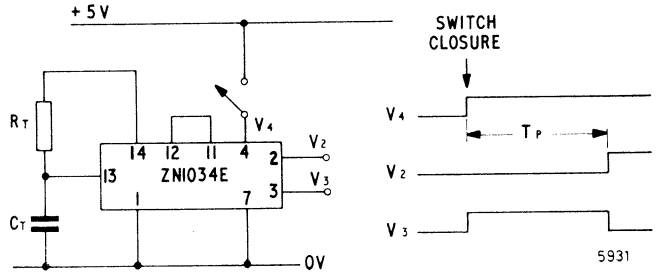


Fig. 1

External components R_T and C_T determine the length of the period T_p and if values of $R_T > 12k$ and $C_T > 33$ nF are used then the relationship $T_p = K C_T R_T$ applies and the time multiplying factor $K = 2800 \pm 10\%$.

(The timing components set the period of an internal oscillator to $0.68 C_T R_T \pm 10\%$ and an internal divider causes a change in the output state after 4095 oscillator cycles).

When the time period is initiated pin 3 goes 'High' and remains 'High' for a time period T_p. On completion of the time period, Pin 3 goes 'Low' and Pin 2, which was previously 'Low' goes 'High' and remains High until the timing sequence is re-initiated.

NOTE 1.2 TRIMMING THE TIME PERIOD

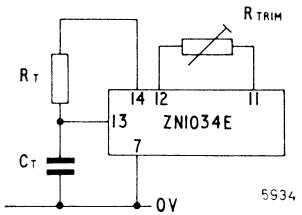


Fig. 2

The time period multiplier K varies with the value of external resistance between pins 11 and 12 (R_{Trim}). Hence the time period for given values of timing components R_T and C_T can be independently TRIMMED.

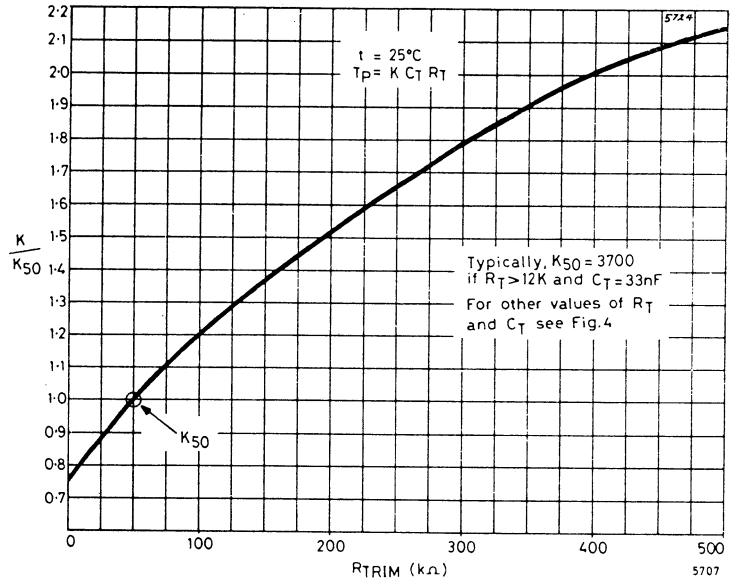


Fig. 3

The graph Fig. 3 gives the variation of time period multiplier with R_{Trim} normalised to the value of multiplier obtained for $R_{Trim} = 50K$ (referred to as K_{50}).

For values of $R_T > 12k$ and $C_T > 33$ nF

$$\text{Typically } K_{50} = 3700 \pm 10\%.$$

Choosing $R_{Trim} = 50k$ makes it possible to provide a $\pm 25\%$ trim on the time period obtained when a 100k potentiometer connected between pins 11 and 12 is set at midpoint. Such a trim would enable inexpensive wide tolerance timing components to be used in an accurate timer.

NOTE 1.3 DESIGN OF VARIABLE PERIOD TIMERS

Time periods from 16 ms to infinity may theoretically be obtained using the ZN1034E integrated timer circuit. However the designer is usually limited by component availability and other restrictions to a narrower range than this. The following sections should enable the designer to get the best possible circuit configuration to be achieved within the design limits. The necessary information is presented below in the form of a Timing Component Guide and a Graph of Time Period Multiplier variation with the Time Period. All graphs have been plotted using a 100k variable resistor set at mid-point for R_{Trim}.

For the component guide and the graph of multiplier against time period the value of R_{Trim} has been chosen as a 100k variable resistor at midpoint setting thus giving a possible change of approximately $\pm$25% on time periods obtained from the graphs.

NOTE 1.4 TIMING COMPONENT GUIDE

The graph, Fig. 4, gives an idea of the values of timing components necessary for a given time period. It is plotted assuming a 100k variable resistor between pins 11 and 12 is set at midpoint. The periods obtained with the timing components selected from the graph may then be trimmed with the variable resistor to the exact time required.

The maximum range possible for a particular value of Timing Capacitor can be easily obtained from the graph. For example, a range of 50 ms to 75 seconds can be achieved with a 3.3 nF capacitor or 40 seconds to 100 mins with 3.3 μF.

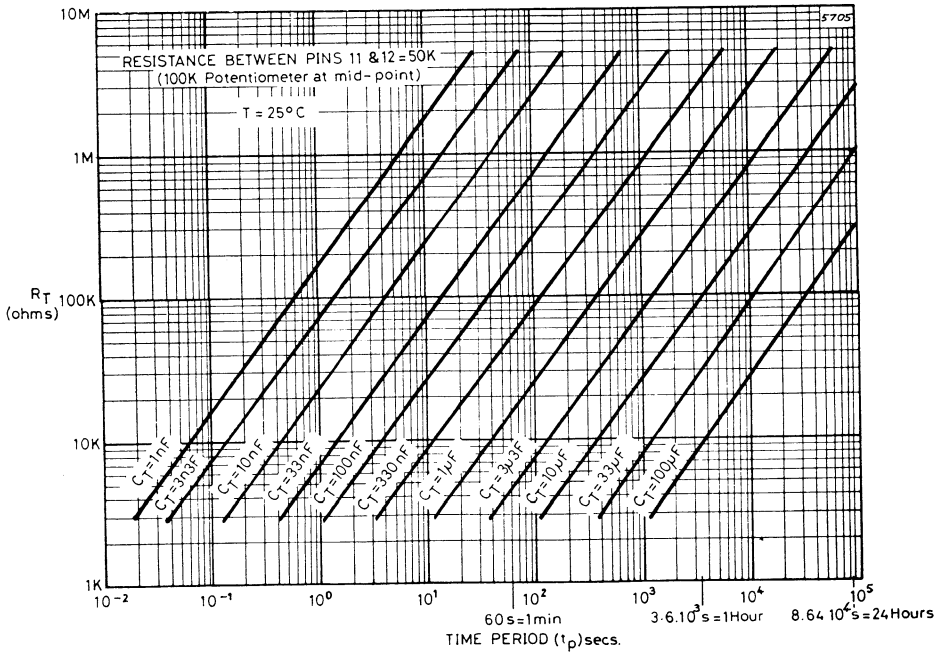


Fig. 4

NOTE 1.5 VARIATION OF TIME PERIOD MULTIPLIER WITH TIME PERIOD

The linear relationship implied by the equation $T_p = K C_T R_T$ is modified when extreme values of timing components are used. Typical variations in the multiplier, K, are shown in Fig. 5, again assuming that a 100k variable resistor set at midpoint is connected between pins 11 and 12.

Using this graph the example of the 3.3 nF capacitor which was used to illustrate the timing component guide graph above will be seen to give a slightly different range, 52 ms to 74 seconds for a 3k3 to 5M change in R_T.

The multiplier (K_{50}), for this example, varies from a minimum of 4200 to a maximum of 4975, a total variation of $\pm 8.5\%$.

The graph may be used to determine the linearity of the time period variation with timing resistance for various values of timing capacitor and for various ranges of time period as illustrated by the following examples.

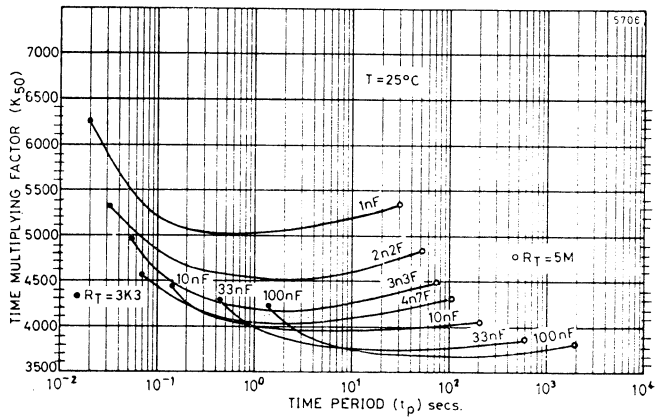


Fig. 5

NOTE 1.6 DESIGN A 1500 : 1 VARIABLE TIMER

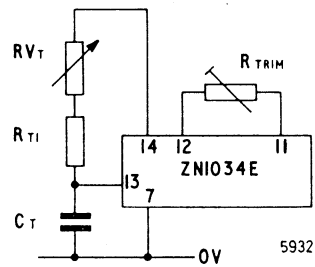


Fig. 6

A wide range continuously variable timer circuit is shown in Fig. 6 and if the values of the above example are used then a variation of approximately 1 :1500 is obtainable (or 50 ms :75 seconds).

For R_{T1} = 3k3

R_{VT} = 5M

R_{Trim} = 50k (100k variable resistor set to midpoint)

C_T = 3.3 nF

The maximum period $T_{p(Max)} = K\,C_T\,(R_{VT} + R_{TI})$

and the minimum period $T_{p(Min)} = K\,C_T\,R_{TI}$

Hence the range is $1 : \frac{T_{p(Max)}}{T_{p(Min)}}$

i.e. $1 : \frac{R_{VT}}{R_{TI}} + 1$

approximately $1 : \frac{R_{VT}}{R_{TI}}$

If the variable resistor R_{VT} is scaled linearly in terms of time period then the predicted linearity error from Fig. 5 will be ±8.5%.

NOTE 1.7 A 400 : 1 LINEARLY VARIABLE TIMER

Restricting the range to about 400:1 enables the designer to achieve a better linearity than the 1500:1 timer. The design of the circuit of Fig. 7 illustrates this point.

$R_{T(Max)}$ = 5M

$R_{T(Min)}$ = 12k

C_T = 33 nF

R_{Trim} = 50k

range is $1 : \frac{5M}{12k} + 1$

i.e. $1 : 418$

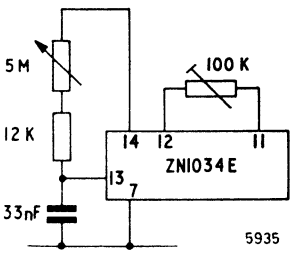


Fig. 7

The values selected are such as to give approximately

$T_{p(Min)}$ = 1.5 sec. from graph, Fig. 4

and $T_{p(Max)}$ = 10 min. from graph, Fig. 4

These values are used to obtain those of K_{50} from the graph of Fig. 5.

The maximum value of K_{50} = 3950 from Fig. 5

and the minimum value of K_{50} = 3800 from Fig. 5

This indicates that the maximum linearity error is ±2%.

(Excluding errors due to R_{TI} end resistance at minimum settings)

NOTE 1.8 A 3 DECADE SWITCHED TIMER

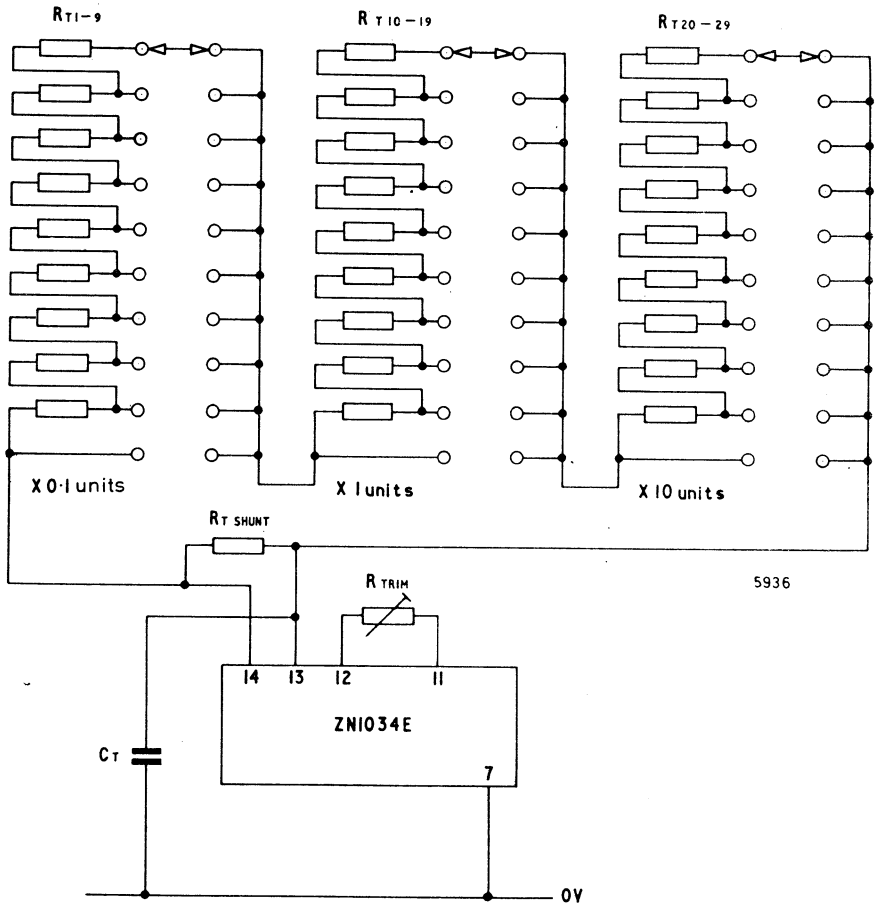


Fig. 8

A wide range timer with switched timing resistors can be designed in a similar manner to the circuit described in Note 1.6.

Switched resistors are preferable in some circumstances for setting the time period of timer circuits. In addition to the ability to set a time precisely, advantage can be taken of the capability of the ZN1034E circuit of operating linearly over a wide range of values of timing resistor up to 5M. There is also the possibility of correcting for errors at the extremes of the range if this is thought worthwhile.

The design of the timer illustrated in Fig. 8 can be taken as an example. Here the aim is to achieve a 0.1 to 99.9 second range with an accuracy consistent with the use of 1% resistors,

The **Timing Component Guide** shows that for the maximum time of about 100 secs R_T is required to be about 5M and the value of C_T to be between 3·3 nF and 10 nF.

The graph depicting **Variation of multiplying factor with time** indicates that a 4.7nF capacitor will give 100 secs with 5M and the 4.7 nF curve shows a minimum value of K_{50} of 4030 at 2 seconds and a value of 4280 at 100 seconds, an error of +6% on the linearity taking 2 secs as standard.

Such a steady increase of time error can be corrected by shunting the switched resistors by the appropriate high value, $R_{T(Shunt)}$. The value required in this particular case will be such as to reduce $R_{T(Max)}$ by 6%.

$$\text{i.e.} \quad R_{T(Shunt)} = 5M\left(\frac{100-6}{6}\right)$$

$$= 82M \text{ (Nearest preferred value)}$$

This will have no effect on the linearity error at the bottom end of the range.

Assuming the effect of the variation in multiplying factor over the production spread of devices and also the capacitor tolerance is trimmed out by R_{Trim} we can specify the resistors as:

$$R_{T1} - R_{T9} = 5k1 \pm 0.5\%$$

$$R_{T10} - R_{T19} = 51k \pm 0.5\%$$

$$R_{T20} - R_{T29} = 510k \pm 0.5\%$$

$$\text{and } C_T = 4.7 \text{ nF} \pm 5\%$$

Typical errors derived from the graph shown in Fig. 5 (multiplying factor against time), are tabulated on page 14.

NOTES (see table page 14)

1 The timing resistance as specified above but allowing for the effect of an 82M ohm overall shunt resistor. (Only the significant values shown).

2 The multiplying factor used in the calculation of the time period should strictly be that appertaining to the calculated time which will differ from the set time by the error. Since this error is small the error in using the set time to derive the multiplying factor from the graph is negligible.

3 Normalising the error by adjusting the trim resistor to give correct timing on the 10 second setting.

4 The timing resistors as specified above but with 82M overall shunt resistance and a 4k7 in place of a 5k1 for the 0.1 sec. position. (Only the significant values shown).

Using Shunt Resistor Correction						Using Shunt and Series Resistor			
Timing Period Setting Secs	Multiplying Factor	Timing Resistance (Note 1) k ohms	Calculated Time (Note 2) Secs	Calculated Error %	Normalised Error (Note 3) %	Timing Resistance (Note 4) k ohms	Calculated Time (Note 2) Secs	Calculated Error %	Normalised Error (Note3) %
0.1	4475	5.1	0.107	+7	+10	4.7	0.099	−1.2	+1.8
0.2	4230	10.2	0.203	+1.5	+4.5	9.8	0.195	−2.6	+0.4
0.3	4150		0.298	−0.6	+2.4	14.9	0.291	−3.1	−0.1
0.4	4100		0.393	−1.8	+1.2	20	0.39	−3.7	−0.7
0.5	4080		0.489	−2.2	+0.8	25.1	0.48	−3.7	−0.7
0.6	4070		0.585	−2.4	+0.6	30.2	0.58	−3.7	−0.7
0.7	4062		0.681	−2.7	+0.3	35.3	0.67	−3.7	−0.7
0.8	4055		0.778	−2.8	+0.2	40.4	0.77	−3.8	−0.8
0.9	4050		0.873	−3.0	0	45.5	0.87	−3.8	−0.8
1.0	4045		0.970	−3.0	0	51	0.97	−3.0	0
1.1	4040		1.07	−3.2	−0.2	55.7	1.06	−3.9	−0.9
1.2	4040		1.16	−3.2	−0.2	60.8	1.15	−3.8	−0.8
1.3	4040		1.26	−3.2	−0.2	65.9	1.25	−3.7	−0.7
1.4	4040		1.36	−3.2	−0.2	71.0	1.35	−3.7	−0.7
1.5	4040		1.45	−3.2	−0.2	76.1	1.44	−3.7	−0.7
1.9	4040		1.84	−3.2	−0.2	96.5	1.83	−3.6	−0.6
2.0	4040		1.94	−3.2	−0.2	102	1.94	−3.2	−0.2
2.1	4040		2.03	−3.2	−0.2	106.7	2.03	−3.5	−0.5
3.0	4040		2.90	−3.2	−0.2	153	2.91	−3.2	−0.2
10.0	4070	507	9.70	−3.0	0	507	9.70	−3.0	0
11.0	4075	557	10.67	−3.0	0				0
13.0	4080	658	12.61	−3.0	0				0
20.0	4110	1008	19.46	−2.7	+0.3				+0.3
30.0	4150	1502	29.30	−2.3	+0.7				+0.7
80.0	4260	3889	77.86	−2.7	+0.3				+0.3
90.0	4275	4349	87.4	−2.9	+0.1				+0.1
99.9	4280	4800	96.6	−3.3	−0.3		96.6		−0.3

The predicted maximum error is approxiamtely ±5% of setting overall but with a shunt resistor across the switched resistors this can be reduced to ±0.5% for settings above 0.4 secs. By altering one of the switched resistor values in addition to having a shunt resistor the overall predicted error becomes ±1.5% of setting.

N.B. Setting all three decade switches to zero should be avoided since this will disable the oscillator and stop the timer.

NOTE 1.9 EFFECT OF TEMPERATURE ON TIME PERIOD

For optimum temperature coefficient of time period it is necessary to use as low a resistance as possible between pins 11 and 12 (R_{Trim}) consistent with the maximum amount of adjustment of the time period required. This is illustrated by the graph Fig. 9.

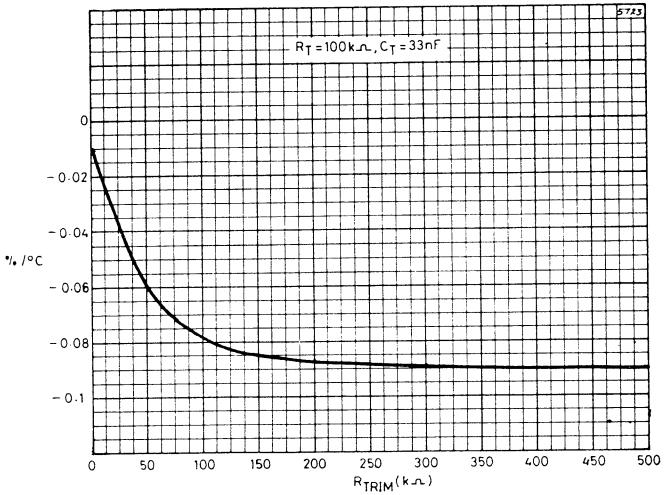


Fig. 9

The effect of varying the value of the timing resistance on the time period temperature coefficient is shown in Fig. 10.

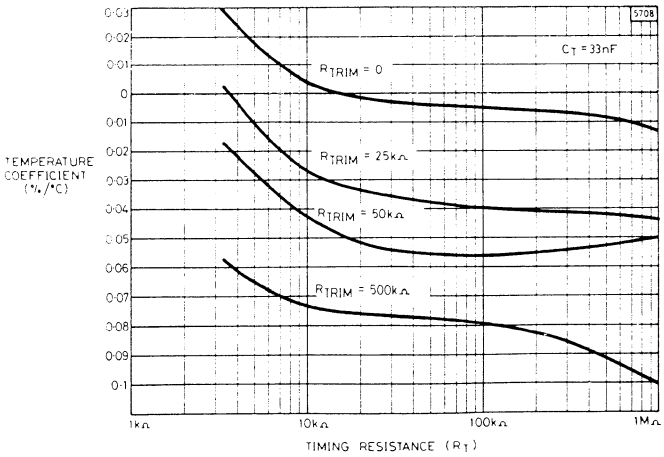


Fig. 10

Optimum temperature coefficient may be obtained with $R_{Trim} = 0$, $R_T = 20k$ and $C_T > 33$ nF.

SECTION 2 INPUT AND OUTPUT CIRCUITS

NOTE 2.1 EXTERNAL CLOCK

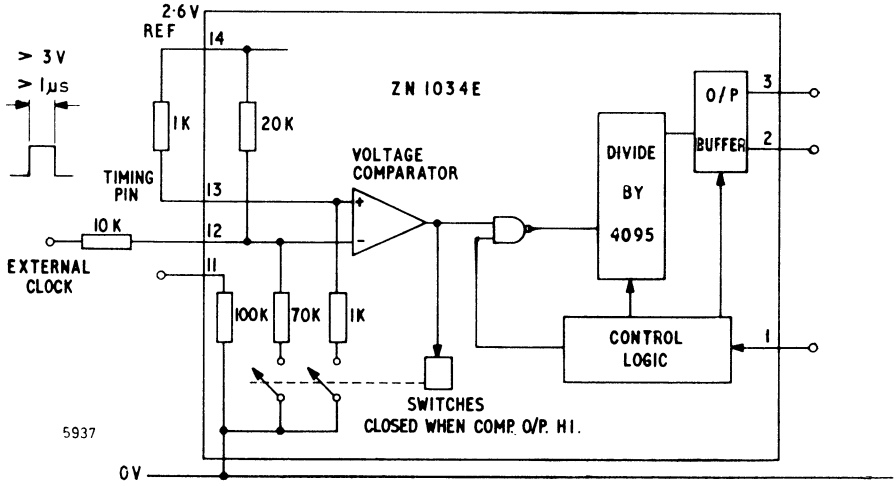


Fig. 11

The ZN1034E can be used with an external clock as shown in the circuit of Fig. 11.

The internal clock is disabled by connecting a 1k resistor from the timing Pin 13 to the +2.5V reference pin 14 thus preventing the non-inverting i/p to the amplifier dropping below the inverting input voltage. The amplifier output is therefore HI and the internal switches are closed. An external clock pulse, provided it meets the limits defined in the characteristics, will override the disabling on pin 13 and, if the trigger i/p on pin 1 is LO, will cause a pulse to be passed to the divider circuit.

The outputs Q and $\overline{Q}$ will change from LO to HI and vice versa at the end of 4095 external clock pulses.

NOTE 2.2 TIMING INITIATION AND RESET

2.2.1 Supply initiated

When pin 1 is held 'LO' and the supply is switched on the control logic and counters are automatically reset as the supply rises to its on voltage, this also initiates timing at the same instant by gating the oscillator output into the counter. After the set time (period 1), the outputs change state and remain thus until the supply is switched off or another period is initiated.

If during such a timing cycle (period 2) the trigger input is taken HI, no matter how many times or for how long, the condition of the outputs and the length of the timing period will not be affected. But if the supply is dropped below the reset level even for a few micro-seconds then the timing period will be terminated. It will be reset and restarted when the supply rises again above the reset level. Thus a supply drop-out has the effect of increasing the time period ; $\overline{Q}$ output remains low for (period 2) plus (period 3).

2.2.2 Trigger initiated

Allowing pin 1 to rise with the supply prevents timer initiation by the supply. To make certain that the trigger is not held down by stray capacitance from pin 1 to ground, inadvertently initiating timing when the supply is switched on, it may be necessary to connect a capacitor from pin 1 to the reference voltage, pin 14.

Pulling the trigger input 'LO' now initiates a normal timing period (perido 4). A further period may be initiated by dropping the trigger LO again (period 5). As for supply initiation, this period is not affected either in duration or in the condition of the outputs when the trigger input level is altered during timing. Similarly the period is terminated by the supply falling below the reset level but since the normal condition of the trigger is HI the timing will not restart on restoration of the supply. A supply drop-out during a trigger initiated timing period has the effect of shortening the set time.

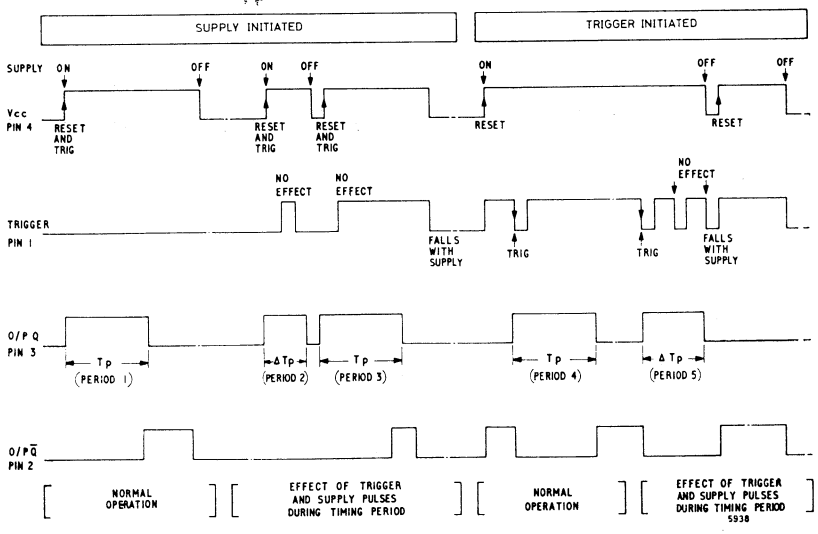


Fig. 12

NOTE 2.3 TRIGGER INPUT CIRCUIT

The input is a 'schmitt trigger' circuit with a hysteresis of about 0.3V. With no input applied the input is pulled HI thus preventing initiation of the timer. When remote triggering is used especially with mechanical contacts it is advisable to provide a more positive pull-up of 10k and 0.1 μF (shown dotted) bearing in mind that the trigger source must be of sufficiently low impedance to pull the input down.

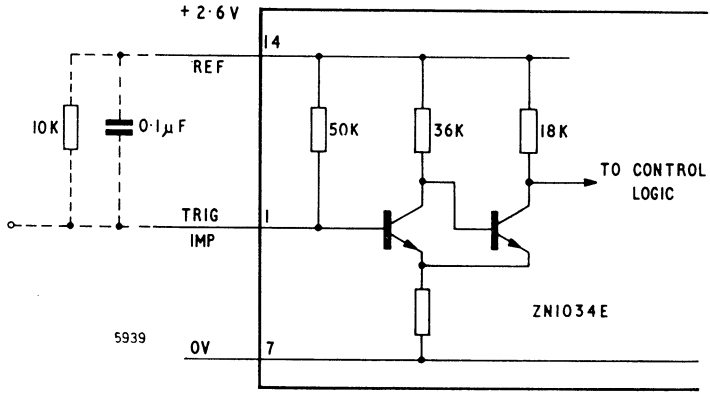


Fig. 13

NOTE 2.4 TRIGGER INPUT TIME PERIOD INITIATION

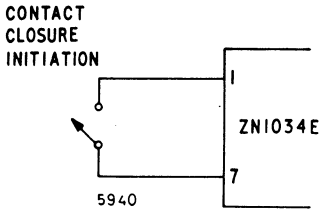


Fig. 14

NOTE 2.5 **OUTPUT DRIVE CIRCUITS**

The Q and $\overline{Q}$ output drive circuits both have the form illustrated in Fig. 18.

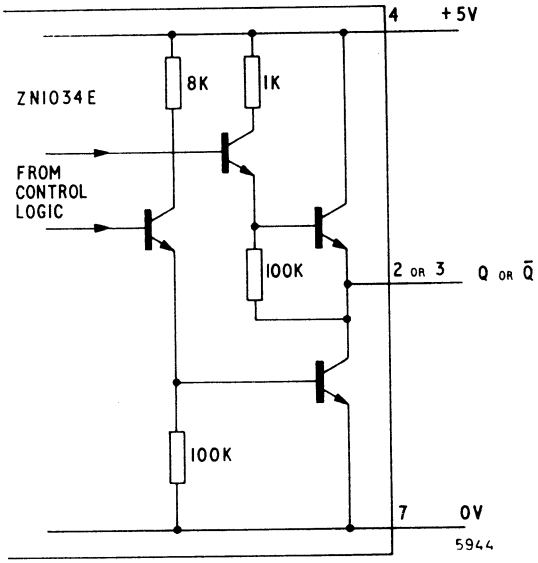


Fig. 18

An external resistor is required to limit the drive current to the requirements of the load circuit and to the current capability of the +5V supply taking into account the needs of the ZN1034E itself (minimum 5 mA externally regulated or 7 mA internally regulated).

NOTE 2.6 LOAD CIRCUITS

2.6.1 TRANSISTOR DRIVEN RELAY

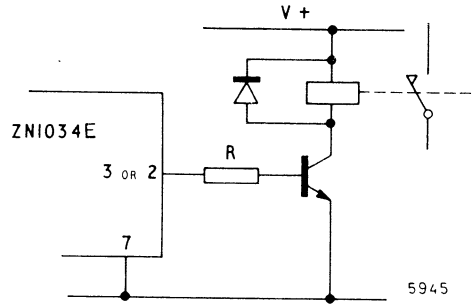


Fig. 19

The value of R is chosen to limit current to minimum required by transistor under the worst condition.

2.6.2 THYRISTOR DRIVEN RELAY

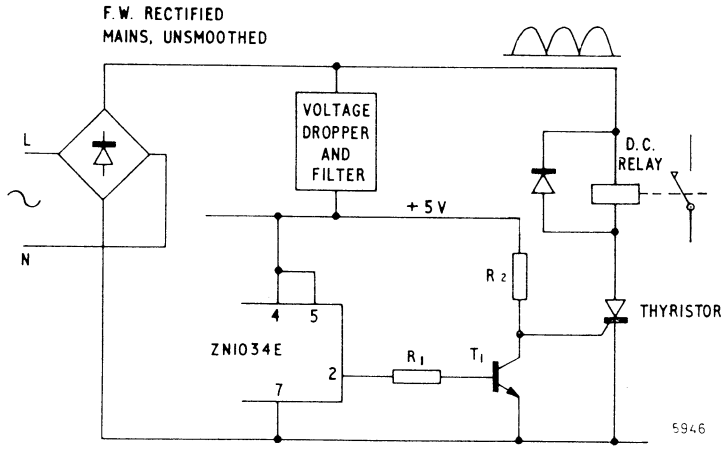


Fig. 20

A thyristor gate may be driven via a limiting resistor directly from pin 2 for DELAY-TO-ON timers. Fig. 20 illustrates a circuit for achieving DELAY-TO-OFF using a thyristor. R_2 can be as high as 10k for low gate current thyristors. The thyristor is chosen such that the reduction in gate-cathode impedance achieved with a saturated transistor is sufficient to increase the holding current to a value which ensures turn OFF and R_1 is chosen so that the transistor (T_1) just reaches saturation.

For 240 volts a.c. mains it may be necessary to use a 110 volt d.c. relay with a dropping resistor of equal resistance since 220 volts d.c. relays are not easily obtainable.

2.6.3 TRIAC A.C. LOAD CIRCUIT POSITIVE FIRING

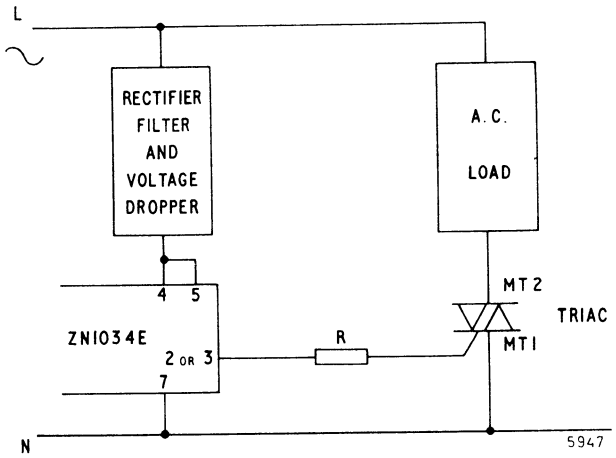


Fig. 21

The value of R is chosen to limit the current to the minimum required by the triac for positive firing in both quadrants.

2.6.4 TRIAC A.C. LOAD CIRCUIT NEGATIVE FIRING

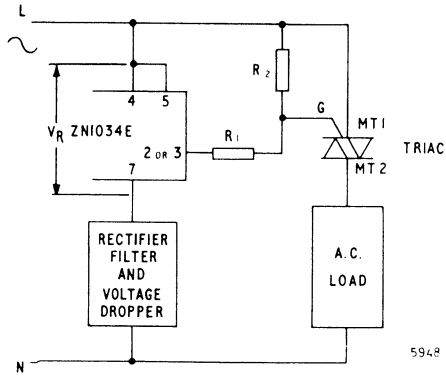


Fig. 22

The value of R_2 is chosen to prevent any leakage currents biasing the triac gate ON during OFF periods. R_1 is chosen to limit the gate current to the maximum required by the triac for negative firing in both quadrants.

Triacs in general are easier to fire in the negative gate mode than the positive and in this configuration the 1034 output drive voltage is a maximum since the total output swing would be $V_{R\,Min} - V_{O(LO)\,Max} \simeq 4.3$ volts for a current of 25 mA. Negative firing triac circuits therefore enable triacs of greater power to be driven directly from the ZN1034E outputs than would be the case for positive firing circuits.

2.6.5 OUTPUT STATE INDICATION

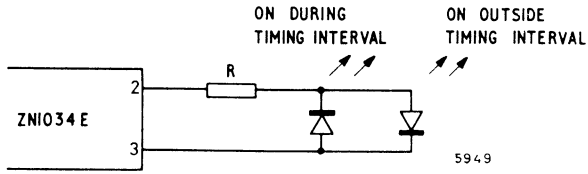


Fig. 23

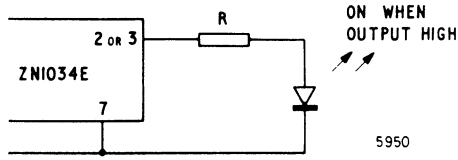


Fig. 24

The value of R is chosen to limit the current to the LED requirement. When mains supplies are used the extra power in the dropper resistor may make the use of neon indicators across the load preferable to LEDs.

SECTION 3 POWER SUPPLIES AND REFERENCE

NOTE 3.1 EXTERNALLY REGULATED SUPPLIES

If a 5V ±6% supply rail is available then the internal shunt regulator is not necessary and by leaving pin 5 unconnected the minimum current drain of 2 mA required by the regulator is avoided. The current available from the supply should not fall below a level of:

$$I_{CC} = (5\text{ mA} + \text{the output current from pins 3 or 2})$$

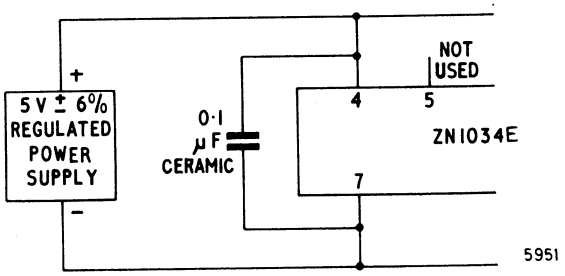


Fig. 25

N.B. The supply should be decoupled by a 0.1 μF capacitor connected as close as possible to pins 4 and 7.

NOTE 3.2 INTERNALLY REGULATED SUPPLIES

3 2 1 D.C. SUPPLIES GREATER THAN 5 VOLTS

By connecting pin 5 to pin 4 an on-chip shunt regulator allows the use of unregulated d.c. supplies higher than 5 volts. To illustrate the use of the shunt regulator a supply circuit design for operation with a typical process equipment supply of +24V ±25% is given on page **104**

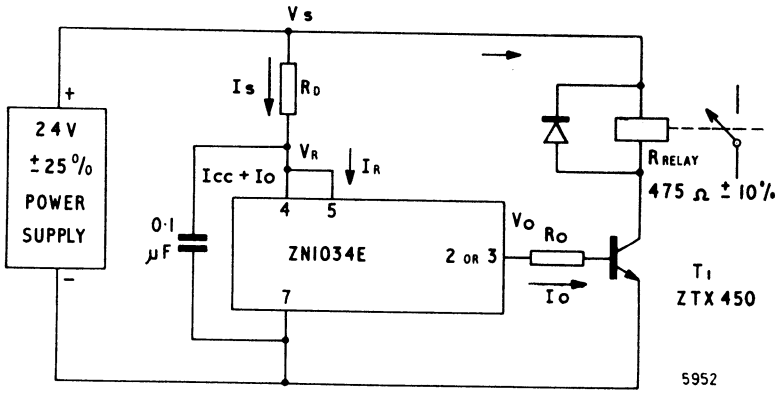


Fig. 26

N.B. The supply decoupling capacitor also acts as stabilisation for the internal regulator and the connection between pins 4 and 5 should therefore be as short as possible.

The values of R_O and R_D used in the circuit of Fig. 26 are calculated as follows. For R_O we need $I_{O(Min)}$, the minimum current required into the base of T_1 for worst case conditions.

$$I_{O(Min)} = I_{B(Max)}$$

$$= \frac{1}{h_{FE(Min)}} \times \frac{24\,(+25\%)}{475(-10\%)}$$

$$= \frac{1}{50} \cdot \frac{30}{427}$$

$$\mathbf{I_{O(Min)} = 1.4\ mA}$$

Deriving $V_{O(Min)}$ from the output circuit (Fig. 18)

$$V_{O(Min)} = V_{R(Min)} - 2 \times (\text{Internal } V_{BE})$$

$$= 4.7 - 1.4$$

$$\mathbf{V_{O(Min)} = 3.3\ Volts}$$

Hence

$$R_O = \frac{3.3 - V_{BE\,T_1}}{1.4} \text{ k ohms} \quad (V_{BE\,T_1} = 0.6V)$$

$$= 1.9k$$

Choose $\mathbf{R_O = 1.8k}$ (Nearest lower preferred value)

To calculate R_D we need $V_{O(Max)}$ and $I_{S(Min)}$

As above

$$V_{O(Max)} = V_{R(Max)} - 2 \times (\text{Internal } V_{BE})$$

$$= 5.3 - 1.4V$$

$$V_{O(Max)} = \mathbf{3.9\ Volts}$$

and with the value of R_O chosen the actual current is

$$I_{O(Max)} = \frac{3.9 - V_{BE\,T1}}{1.8} = 1.8\ mA$$

From which the minimum allowable supply current can be obtained

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$
$$= 5 + 2 + 1.8$$
$$\mathbf{I_{S(Min)} = 8.8\ mA}$$

Hence

$$R_D = \frac{V_{S(Min)} - V_{R(Max)}}{I_{S(Min)}}$$
$$= \frac{18 - 5.3}{8.8}k$$
$$\mathbf{R_D} = \mathbf{1.5k}\ \text{(Nearest preferred value)}$$

The power dissipated in the dropping resistor and the ZN1034E can be obtained also from

$$I_{S(Max)} = \frac{V_{S(Max)} - V_{R(Min)}}{1.5k(-5\%)}$$
$$= \frac{30 - 4.7}{1.425}mA$$
$$\mathbf{I_{S(Max)} = 18\ mA}$$

Hence the ZN1034E dissipation = 90 mW max. and power dissipated by dropping resistor = 450 mW max.

The calculations assume ±2% tolerance resistors.

3.2.2 A.C. MAINS SUPPLIES

A transformer may be used to drop the voltage from the mains and a rectified d.c. supply provided as discussed in 3.2.1 above.

However the on-chip shunt regulator makes the transformer unnecessary since the supply may be obtained directly from the mains or from any other source of a.c. or d.c. higher than 5 volts. With a load such as the directly driven triac (sections 2.6.3 and 2.6.4) a half wave rectifier is used since either the line or neutral has a connection common to the load circuit and the I.C. supply thus preventing the use of a bridge rectifier.

The calculation of the smoothing and voltage dropping components is described below.

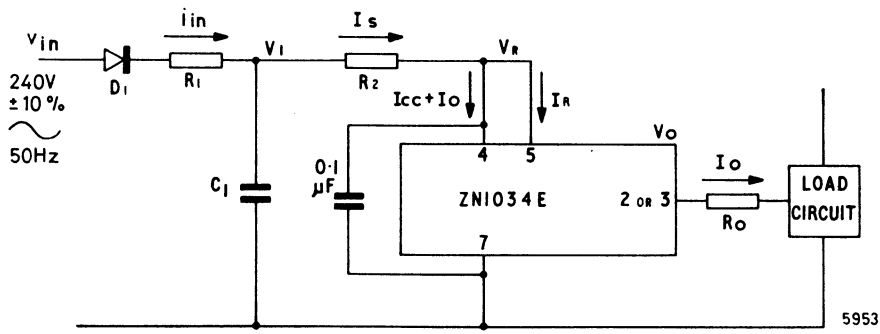


Fig. 27

The value of R_O and $I_{O(Max)}$ are calculated as in 3.2.1 above and as an example a current $I_{O(Min)}$ of 10 mA is assumed (the gate current for a 0.35A Triac, RS 202).

Therefore $\mathbf{V_{O(Min)} = 3.3V}$

$$R_O = \frac{3.3 - V_G}{10.10^{-3}} \text{ ohms } (V_G T_1 = 2V \text{ for RS 202})$$

$\mathbf{R_O = 120 \text{ ohms}}$ (Nearest lower preferred value)

$\mathbf{V_{O(Max)} = 3.9V}$

Hence $$I_{O(Max)} = \frac{3.9 - V_G}{0.12} \text{ mA}$$

$\mathbf{I_{O(Max)} = 16 \text{ mA}}$

And the minimum value of supply current for correct operation is therefore

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)}$$
$$= 5 + 2 + 16$$

$\mathbf{I_{S(Min)} = 23 \text{ mA}}$

If we assume that C1 is a 25 volt working capacitor and that 3 volts peak to peak ripple is allowable then the highest value for $V_{1(Min)}$ will be

$V_{1(Min)} = 25(-20\%) - 3$ (Allowing for ±10% variation in mains supply).

$\mathbf{V_{1(Min)} = 17 \text{ V}}$

Therefore $$R_2 = \frac{17 - V_{R(Max)}}{23} \text{ k ohms}$$

$\mathbf{R_2 = 510\Omega}$ (Nearest preferred value)

The current i_{in} will flow for very nearly the full half cycle, 10 ms in the case of 50 Hz supplies, since V_1 is low compared to the peak mains voltage.

Now $$i_{in(avg)} = \frac{V_{in(pk)} - V_{1(avg)}}{\pi R_1}$$

and this current from the rectifier must be equal to the current into the timer circuit.

$$i_{in(avg)} = I_{S(avg)}$$

and the average value of this current is

$$I_{S(avg)} = \frac{V_{1(Min)} + V_{Ripple\ (avg)} - V_{R(Min)}}{R_2}$$

$$= \frac{17 + 1.5 - 4.7}{510}$$

$$= 27\ \text{mA}$$

Therefore $$R_1 = \frac{\sqrt{2} \times 240\ (-10\%) - (17 + 1.5)}{\pi \times 27}\ \text{k ohms}$$

$$= \textbf{3k3}\ \text{(Nearest preferred value)}$$

For the required ripple of 3V pk.pk we can obtain

$$C_1 = \frac{I_{S(avg)} \times 10\ \text{ms}}{3}$$

$$C_1 = \frac{27 \times 10^{-5}}{3}$$

$$C_1 = \textbf{100}\ \mu\textbf{F}\ \text{(Nearest higher preferred value)}$$

In order to calculate the maximum power dissipation in the dropping resistor we need to know $i_{in(avg)}$ for the upper limit of mains voltage.

Maximum value of $$i_{in(avg)} = \frac{V_{in(pk)\ (Max)} - V_{1(Max)}}{\pi R_1}$$

$$= \frac{2 \times 240\ (+10\%) - 20}{\pi \times 3.3 \times 10^3}$$

$$\textbf{Max. } i_{in(avg)} = \textbf{34 mA}$$

and Max dissipation in $$R_1 = \frac{\pi^2}{4} \times i_{in}{}^2{}_{(avg)} \times R_1$$

$$P_{R1} = \textbf{9.4 Watts}$$

When a d.c. load such as the thyristor relay driver of section 2.5.2 is required then a full wave bridge circuit can be used as shown below.

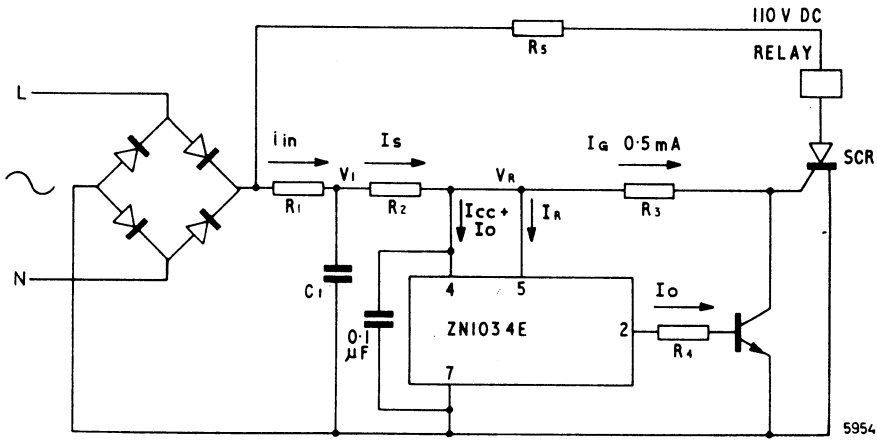


Fig. 28

The DELAY-TO-OFF timer circuit of Fig. 20 has been taken as an example. A typical circuit might have the relay resistance equal to $R_5 = 10k$ and for a 240V ±10% mains supply the SCR could be a BRX49 which requires less than 0.5 mA on gate current. To ensure gate turn-off a ZTX450 transistor with a base current of 0.5 mA is sufficient with the above load.

Hence

$$I_{S(Min)} = I_{CC(Max)} + I_{R(Min)} + I_{O(Max)} + I_G$$
$$= 5 + 2 + 0.5 + 0.5$$
$$\mathbf{I_{S(Min)} = 8\ mA}$$

Choosing C_1 to be 25 volt working and 3 volts peak to peak ripple as in the previous example. Then

$$V_{1(Min)} = 25\ (-20\%) - 3$$
$$= \mathbf{17\ Volts}$$

And

$$R_2 = \frac{17 - V_{R(Max)}}{8}\ \text{K ohm}$$
$$= \mathbf{1.5k}\ \text{(Nearest preferred value)}$$

To find the value of C_1 required estimate the angle of conduction. Thus for a sine wave input conduction with change when the voltage on the smoothing capacitor is equal to the instantaneous value of the input voltage less the rectifier voltage drop.

So $V_1 + 1.2 = V_{in(pk)} \sin \theta$

and for small values $\theta = \sin \theta$

Hence $\theta = \dfrac{V_1 + 1.2}{V_{in(pk)}}$

(assuming 1.2 volt drop across the bridge rectifier).

for the rising sine wave $\theta_r = \dfrac{V_{1(Min)} + 1.2}{V_{in(pk)}}$

and for the falling sine wave $\theta_f = \dfrac{V_{1(Max)} + 1.2}{V_{in(pk)}}$

$$\theta_{tot} = \frac{V_{1(Min)} + V_{1(Max)} + 2.4}{V_{in(pk)}}$$

$$= \frac{17 + 20 + 2.4}{305} \quad \text{(Taking lowest mains input as worst case).}$$

$$= 0.13 \text{ radian}$$

The angle of non conduction $\theta_{tot} \simeq 8°$ and the capacitor will discharge by 3 volts in this period which in terms of time is

$$t = \frac{8}{180°} \times 10 \text{ ms (for 50 Hz mains)}$$

$$= 0.44 \text{ ms}$$

and since $C \simeq \dfrac{\Delta t}{\Delta V} \cdot I_{S(Max)} \qquad (I_{S(Max)} \simeq I_{S(Min)} + 20\%)$

$$\simeq \frac{44 \times 10^{-5}}{3} \times 8 \times 10^{-3} \ (+20\%)$$

$$\simeq 1 \cdot 4 \ \mu F$$

So we can choose a $2 \cdot 2 \ \mu F$ of 25 volt working or higher for C_1.

The mains dropping resistor can be simply obtained with sufficient accuracy by assuming 100% conduction. Thus

$$R_1 = \frac{2}{\pi} \times \frac{v_{in(pk)} - V_{1(Max)}}{I_{S(Min)}}$$

$$= \frac{2 \times 305 - 20}{\pi \times 8 \times 10^{-3}}$$

(Lowest mains voltage gives worst case).

$$\simeq 22k \text{ (Next lower preferred value)}$$

In order to calculate the power dissipated by the dropping resistor P_{R1} we need to know $i_{in(avg)}$ for the higher limit of the supply.

Maximum value of $i_{in(avg)} \simeq \dfrac{2\,(v_{in(pk)\,(Max)} - V_{1(Max)})}{\pi R_1}$

$$= \frac{2}{\pi}\left(\frac{2 \times 240\ (+10\%) - 20}{22 \times 10^3}\right)$$

$$i_{in(avg)} = \mathbf{10\ mA}$$

Hence

$$P_{R1} = \frac{\pi^2}{8} \times 10^{-4} \times 22 \times 10^3$$

$$P_{R1} = \mathbf{2.7\ Watts}$$

The calculations have been performed using the 235V ±10% 50 Hz mains figures. Similar calculations may be done for 110V 60 Hz or whatever supplies are available.

NOTE 3.3 REFERENCE SUPPLY

The 2.6V reference on pin 14 may be used for an external reference other than for the timing components.

SECTION 4 INTERFERENCE SUPPRESSION

Two types of interference, mains borne and electromagnetically radiated interference, can affect the operation of the timing circuit. In environments where such noise is encountered steps should be taken to reduce its effect on the timing circuit and the following notes should enable the circuit designer to avoid interference problems. The points discussed are illustrated by referring to a mains delay-to-on, plug-in module, timer design illustrated in Figs. 29 30, 31, 32.

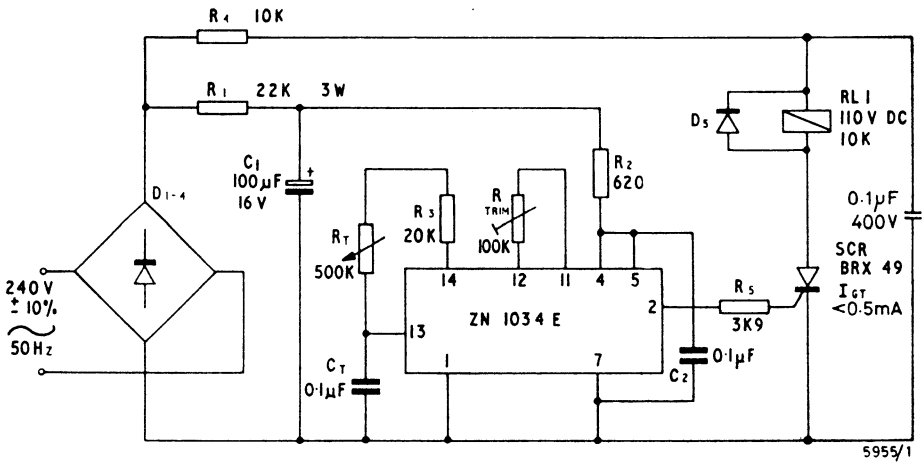


Fig. 29

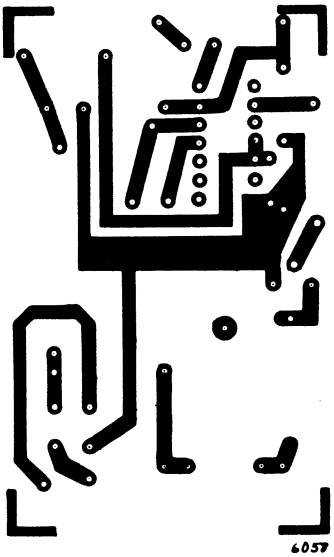


Fig. 30

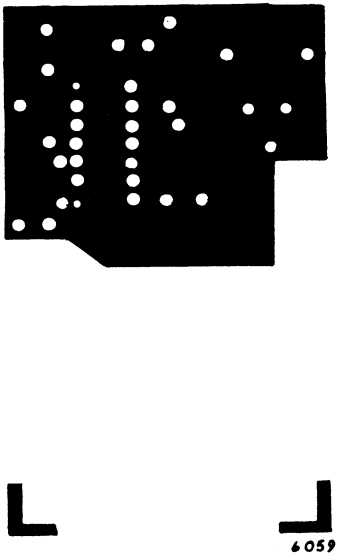


Fig. 31

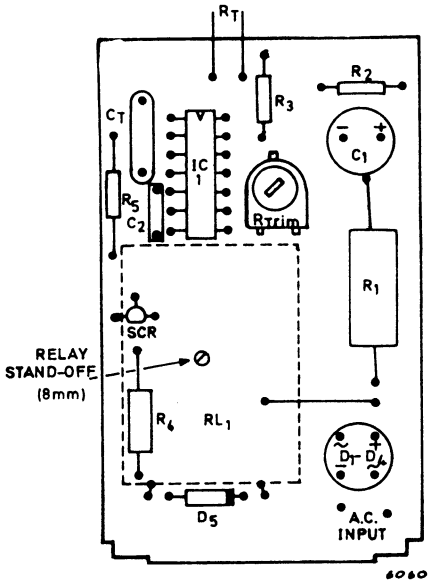


Fig. 32

NOTE 4.1 MAINS BORNE INTERFERENCE

If the supply is reduced below (typically) 3.6V at any time, even for less than a microsecond, then the ZN1034E counter section will be reset and restoration of the normal supply will initiate a new timing period or terminate the period depending on the initiation mode used. The effects of pulses on the supply are described in operating note 2.1.

Positive spikes are effective only when they produce a negative overshoot large enough to cause reset.

Negative spikes can be reduced by using a full diode bridge circuit, as in Fig. 29 which rectifies the spikes as well as the a.c. supply, or a half bridge where an a.c. load is being driven and the timer ground cannot be separated from neutral. The dropping resistor R_1, with C_1, forms a low pass filter for mains smoothing and additional filtration is provided by R_2 and C_2. These filters will also attenuate noise spikes. The shunt regulator in conjunction with the dropping resistors R_1 and R_2 provides considerable spike attenuation as well as d.c. regulation. The circuit of Fig. 29 for example, has an attenuation of supply spikes of 15000:1 due to the regulator alone. When a 5 volt supply designed for TTL, or similar requirements is available and the shunt regulator is not connected, protection against interference is not usually necessary since the supply itself should be capable of suppressing mains borne interference.

If a transformer is used to isolate the timer from the mains then the voltage drop can be divided between the transformer and the series resistor. The greater the series resistance then the greater the attenuation of noise by the shunt regulator and the smoothing capacitor. A transformer drop to 24V d.c. is a useful compromise allowing the use of 24V relays. The transformer itself will attenuate high frequency spikes.

NOTE 4.2 ELECTROMAGNETICALLY INDUCED NOISE

The ZN1034E oscillator frequency is determined by the time taken to charge C_T via R_T from about 1.6 to 2.2 volts on pin 13. A single interference pulse of 0.1V on this pin could cause an error on a single time constant of 20% but since the timing period of a ZN1034E timer is made up of 4095 RC charging times then a large number of interference pulses in a timing period would be required to cause such a timing error. Where such interference exists, and bearing in mind that for a constant rate of interference pulses the effect becomes greater for increasing length of time period, steps should be taken to screen pin 13 from electromagnetically induced noise. Since the oscillator is required to operate at $\frac{4095}{20 \times 10^{-3}}$ Hz, i.e. 200 kHz, pin 13 is sensitive to radiated high frequency interference. Mains borne pulses can be equally troublesome if steps are not taken to isolate pin 13 from such interference. The method used in the design example of Fig. 29 is effective against both EMI and Mains Borne noise. A ground plane is produced by leaving a large area of copper on the component side of a double sided PCB with clearance holes for the component connections. The ground pin (7) is connected to the earth plane and the earthy side of components such as C_T and the decoupling capacitors are also connected directly to the ground plane. In this way the connections have a low impedance to pin 7 and the possibility of coupling interference pulses from the

load or decoupling components into the oscillator circuit via common earth leads is reduced considerably. At the same time the printed circuit connections are screened from EMI.

An external screen such as a metal case can be effective against radiated interference but it does not have the advantage of an earth plane with regard to the reduction of common earth lead interference.

Any leads connected to pin 13 are susceptible to interference pick-up and should be screened. A remote variable timing resistor can be connected to the PCB either by twin screened lead with the screen to ground or single screened with the screen connected to pin 14. It will be noticed that the fixed part of the timing resistance is connected very close to pin 13 to help decouple the connecting leads to the variable resistor.

When the ZN1034E oscillator frequency is near to that of the mains supply, or to low harmonics, care should be taken in the layout of the circuitry and in the position of components such as mains transformers to obviate this effect. Stray coupling of mains frequencies can have the effect of locking the oscillator to that frequency and producing a band over which variation in timing components will not cause a corresponding variation in timing period. The periods most susceptible to such interference are 82 and 41 secs for 50 Hz mains or 68 and 34 secs for 60 Hz mains.

SECTION 5 TIMER CALIBRATION

NOTE 5.1 DIRECT MEASUREMENT

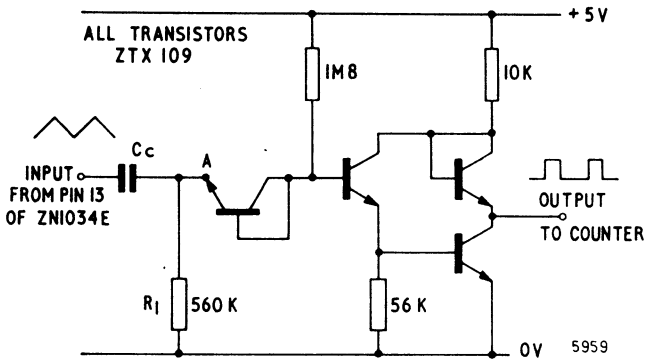
Timer circuits may be calibrated directly by measuring the time period between changes of state on the output pins 2 or 3. This method should be used where accuracies of better than 0.2% are required.

NOTE 5.2 OSCILLATOR PERIOD MEASUREMENT

The measurement of oscillator period is a much quicker method of calibration but it involves measurements at a high impedance point in the circuit where the loading due to the measuring instrument could affect the result. The following notes should assist in calibration by oscillator period measurement:

(a) A passive high impedance probe may be used to connect an oscilloscope or a digital frequency meter to pin 13 and if the probe resistance is greater than 100 R_T and the capacitance less than $C_t/100$ then an accuracy better than 2% should be obtainable. For lower accuracy these requirements may be relaxed proportionally. The period of the oscillator sawtooth waveform is measured and multiplied by 4095 to obtain the time period.

(b) A capacitatively coupled probe illustrated in Fig. 33 below enables calibration accuracies of better than 0.2% to be obtained.



C_T	C_C
0.01	0.333
0.0	0.33
1.0	3.3
10.0	33.0
100.0	330.0
μF	nF

Fig. 33

The maximum value of coupling capacitance for this accuracy is tabulated against timing capacitance above.

It may be advantageous to build-in the probe input capacitor and resistor to the timer and have point 'A' as the input to the external buffer.

(c) An active voltage follower probe such as that illustrated in Fig. 34 may be used instead of the passive probe in (a) above.

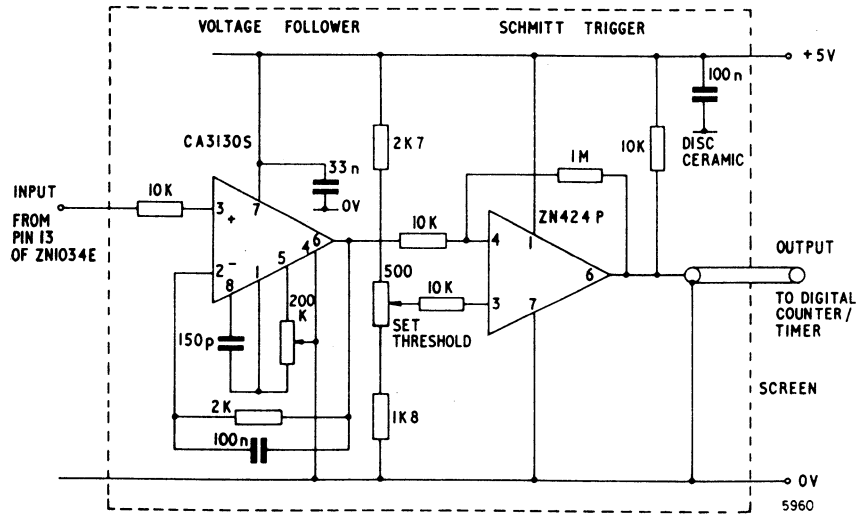
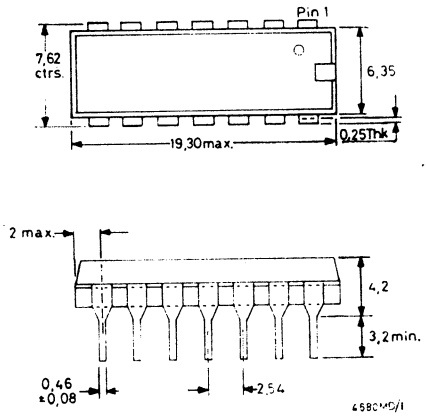


Fig. 34

(d) Connecting extra circuitry to pin 13 increases the possibility of incorrect operation due to interference and the precautions suggested in Section 4 should be borne in mind when devising oscillator period calibration systems.

ZN1034E

PACKAGE DETAILS



14 Lead Moulded D.I.L.

Dimensions in millimetres

FERRANTI semiconductors

ZN1040ERD

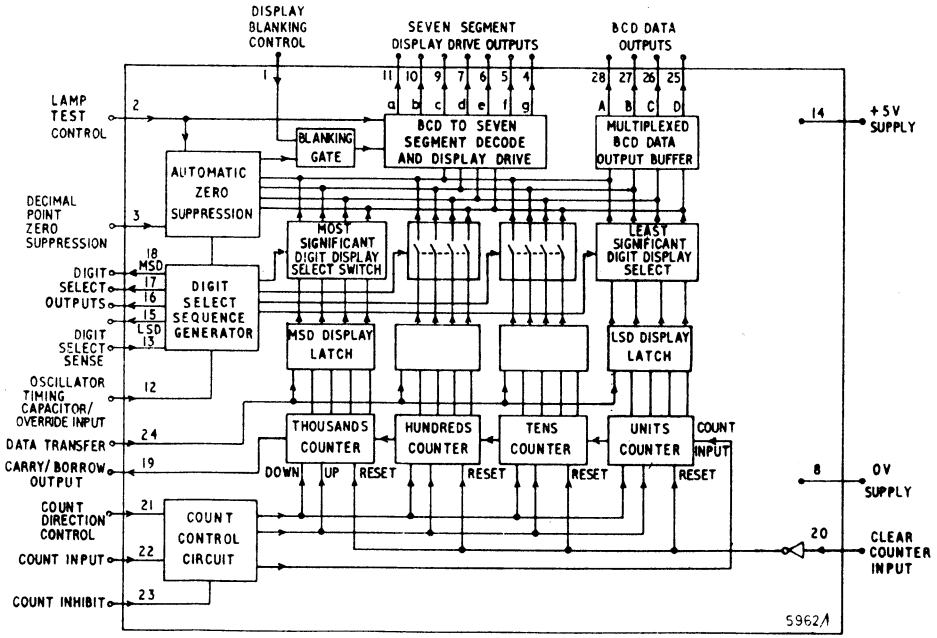
Universal Count/Display Circuit

FEATURES

- 4 decade synchronous up/down counter with memory
- Carry/borrow output for direct synchronous cascading
- BCD and seven-segment outputs
- Segment outputs can drive LED displays directly
- Schmitt trigger on count input for slow input waveforms
- Count inhibit gating
- Two versions: ZN1040E, high-speed; ZN1040AE, low-cost
- Fully TTL compatible

DESCRIPTION

The ZN1040 is designed to satisfy the need for a universal count/display circuit suitable for the widest possible range of applications. This bipolar device allows fast count rates and high output currents to drive seven-segment LED displays, whilst BCD outputs allow interfacing to decoders for other types of display.



Function Diagram

ZN1040ERD

TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	+5.5 volts
Segment Output Currents	100 mA
	80 mA
Other Output Currents	25 mA
Operating Temperature Range	−20°C to +70°C
	0°C to +70°C
Storage Temperature Range	−55°C to +125°C

ELECTRICAL CHARACTERISTICS: V_{CC} = +5V T_{amb} = 25°C (unless otherwise specified).

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Count input positive going threshold	V_T+	—	1.5	—	V	
Count input negative going threshold	V_T-	—	1	—	V	
High level input voltage (1)	V_{IH}	2.0	—	—	V	
Low level input voltage (1)	V_{IL}	—	—	0.8	V	
High level input current	I_{IL}	—	—	20	μA	
Low level input current	I_{IH}	—	—	−600	μA	
High level output voltage (2)	V_{OH}	2.4	3.3	—	V	I_{load} = −0.4 mA
Low level output voltage (2)	V_{OL}	—	0.25	0.5	V	I_{load} = 16 mA
Segment low level output voltage		—	0.3	0.6	V	I_{load} = 50 mA
Segment low level output voltage		—	0.3	0.6	V	I_{load} = 40 mA
Maximum count rate		5	8	—	MHz	
Maximum count rate		3	—	—	MHz	
Transfer pulse width		50	—	—	ns	
Clear pulse width		100	—	—	ns	
Supply voltage	V_{CC}	4.75	—	5.25	V	
Supply current (3)	I_S	—	90	—	mA	

NOTES (1) All inputs except count input
(2) All outputs except segment outputs
(3) All inputs and outputs open circuit

OPERATING NOTES

SECTION 1 : COUNTER

1.1 Counter Operation

The counter section of the ZN1040 is a synchronous four decade BCD counter. Each decade consists of four flip-flops which are clocked simultaneously on the positive going edge of the count input pulse. Suitable steering logic ensures that the 16 flip-flops count in a four decade BCD sequence. The BCD outputs of the counter are connected to data latches in which the count may be stored for subsequent decoding and display.

The counter and count control circuitry are shown in figure 1 whilst the count input and inhibit input circuits are shown in more detail in figure 2.

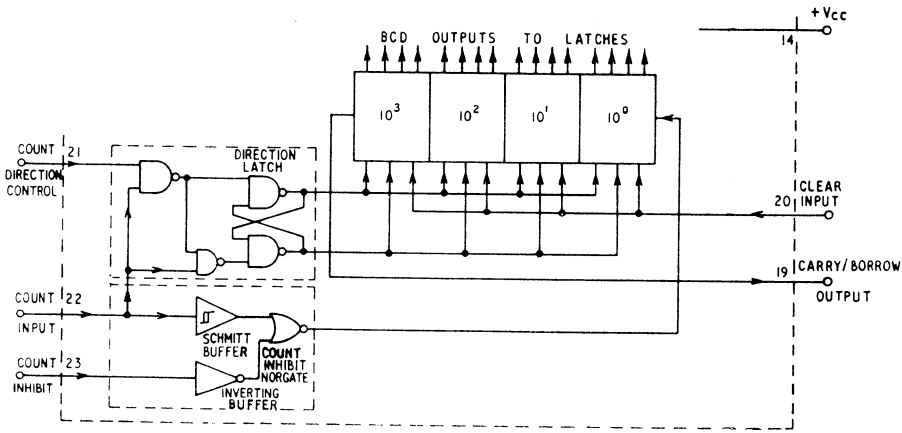


Fig. 1. Count System Functional Diagram

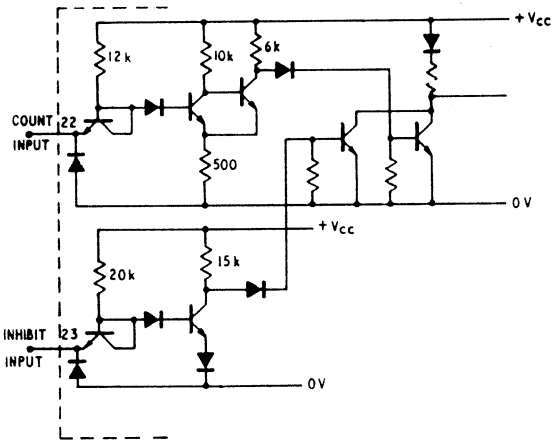


Fig. 2. Count Input and Inhibit Circuit

Counting occurs on the positive going edge of the count input pulse.

The counter input consists of a Schmitt trigger which allows the counter to operate reliably from input waveforms with very slow edges. It also allows a very simple anti-bounce circuit to be used when the count input is taken from a mechanical contact as shown in figure 3.

Bounce occurs mainly on contact closure. R_2 is made very much smaller than R_1 so that when the contact closes C_1 discharges rapidly to below the lower threshold of the Schmitt trigger. However, if the contact subsequently opens due to bounce, the time constant $(R_1 + R_2)\ C_1$ is of sufficient length so that C_1 does not charge to the upper threshold of the Schmitt trigger. When the contact genuinely opens then C_1 will charge and the counter will be clocked. The values of R_1, R_2 and C_1 will depend on the contact characteristics and the maximum count rate.

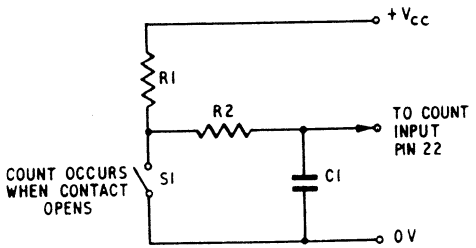


Fig. 3. Anti-Bounce Circuit

1.2 Inhibit Input

The inhibit input is used to gate the count input pulses. When the inhibit input is high then the second input of the inhibit NOR gate is low and count pulses are allowed through. However, when the inhibit input is taken low, the second input of the inhibit NOR gate is taken high. This holds the output low so that the count pulses are blocked. Correct timing of the inhibit control is important. If the inhibit control is taken low when the count input is low then an extra positive going edge will be fed through the inhibit NOR gate and an extra count will result as shown in figure 4a. The inhibit input should thus be operated when the count input is already high as shown in figure 4b. If the count input waveform has a duty cycle which is not 50% then it is advisable to arrange that it is normally high, as in figure 4b, since this makes operation of the inhibit control simpler.

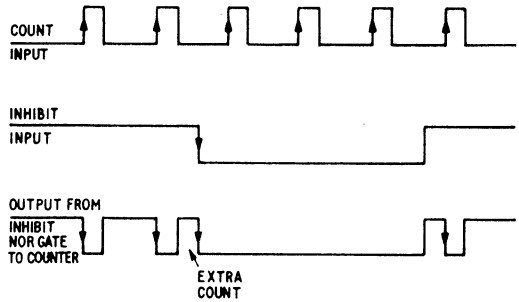


Fig. 4a. Incorrect Inhibit Operation

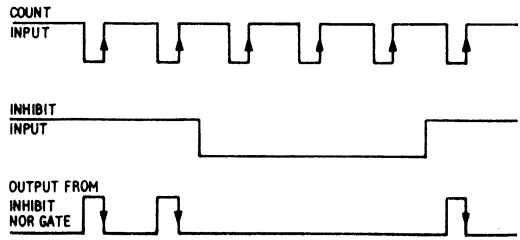


Fig. 4b. Correct Inhibit Operation

1.3 Direction Control

Count direction is controlled by a 'D' latch (see section 1.1) which can be set, for counting up, by taking the mode input high and reset, for counting down, by taking the mode input low. The clock input of this latch is connected to the count input and the state of the latch may therefore be changed only when the count input is high. If the count direction is to be reversed at a particular count then the state of the direction latch must be changed immediately that count is reached, whilst the count input is still high. Waiting until the count input has gone low again will result in the count direction not being reversed until the count input has gone high again, by which time an additional count will have been made in the original direction. Incorrect and correct operation of the direction control is illustrated in figures 5a and 5b.

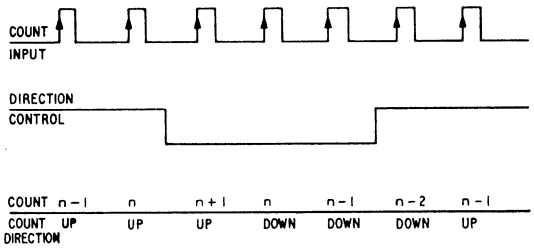


Fig. 5a. Incorrect Operation of Direction Control

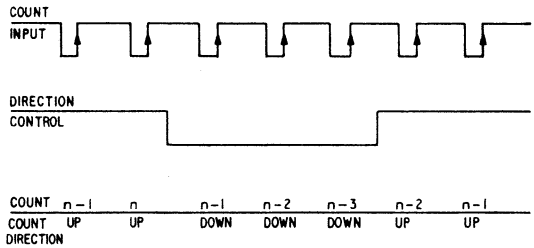


Fig. 5b. Correct Operation of Direction Control

1.4 Counter Reset

The counter may be reset to zero at any time by taking the clear input low. The counter will remain reset until the clear input is taken high again.

Care must be taken to set the direction latch to the correct state immediately after switch-on, otherwise the initial count may be made in the wrong direction. This may occur if the count input is low at switch-on since the direction latch may then set in either state. It is therefore advisable to ensure that the count input is normally high so that the direction latch will be set to the correct state at switch-on by the count direction control.

1.5 Carry/Borrow Output

The carry/borrow output (pin 19) may be used as an overflow indicator or to facilitate direct cascading of ZN1040's. When the count direction is UP then the carry output will go high on the next low-going edge of the count input after a count of 9999 is reached. The carry output will go low again on the next high-going edge at the count input, when the count changes to 0000.

When the ZN1040 is in the count DOWN mode then the carry output will go high on the next low-going edge at the count input after the counter reaches 0000. The carry output will go low again on the next high-going edge at the count input, when the count changes to 9999. In either case the carry output is subject to a propagation delay, t_C of typically 75 ns, relative to the count input edges.

Carry output timing for both up and down counting is shown in figures 6a and 6b.

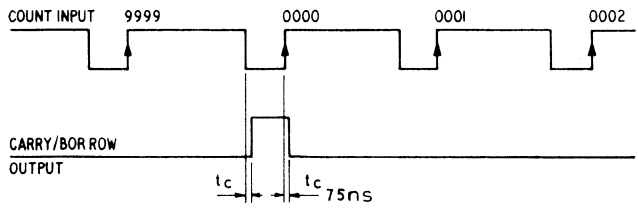


Fig. 6a. Carry Output Timing for Up Count

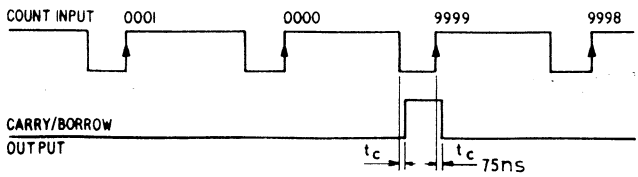


Fig. 6b. Carry Output Timing for Down Count

SECTION 2. COUNT MEMORY

2.1 Display Latch

Each of the decade counters in the ZN1040 produces a binary coded decimal (BCD) number synchronous with the count input. The counter outputs are connected to the inputs of data latches which can store the counter outputs for subsequent display. Whilst the transfer input (pin 24) is high the latches are transparent, and their outputs will follow the data present at the inputs. When the transfer input is taken low the input data present at that instant will be held in the latches and will be unaffected by subsequent changes in the counter outputs.

SECTION 3. DISPLAY MULTIPLEXING

3.1 Multiplex System

In order to economise on pin connections to the ZN1040 and to simplify connection to displays the outputs of the ZN1040 are multiplexed, i.e. the four BCD output digits from the data latches are connected, one at a time, to a common data bus. The multiplexed BCD data is connected to four output pins directly and also via a BCD seven-segment decoder driver so that multiplexed seven-segment outputs are also available. Four digit select outputs indicate which digit is present on the BCD or 7-segment outputs at a particular time.

3.2 Internal Multiplex Oscillator

Clock pulses for the multiplex sequence are generated by the oscillator circuit shown in figure 7. An internal capacitor of nominally 5 pF is charged via a nominal 700k resistor to the upper threshold voltage of the Schmitt trigger. The Schmitt output then goes high, turning on the transistor, and the capacitor discharges through a nominal 10k resistor to the lower threshold of the Schmitt trigger, at which point the output of the Schmitt goes low, the transistor turns off, and the cycle repeats. The nominal frequency of the multiplex oscillator is 500 kHz but this can be altered by adding an external capacitor between pin 12 and ground. A graph of MPX frequency v. external capacitance is shown in figure 8. To ensure stable oscillator operation it is recommended that an external capacitor with a value of at least 100 pF should always be used. When displays are used with the ZN1040 it will frequently be necessary to keep the MPX frequency below 1 kHz to avoid 'ghosting' due to the storage time of the digit-drive transistors. On the other hand the MPX frequency should not be lower than a few hundred Hz otherwise display flicker may become noticeable.

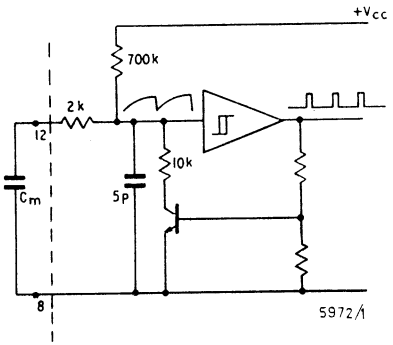


Fig. 7. Multiplex Oscillator Circuit

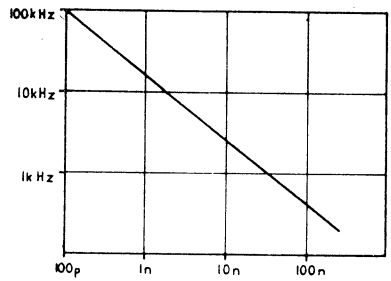


Fig. 8. Nominal MPX Oscillator Frequency v. External Capacitance

3.3 External MPX Oscillator

Since the Schmitt trigger input of the MPX oscillator is only coupled to three fairly high impedances (10k and 700k resistors, and a 5 pF capacitor) it is a simple matter to override the oscillator action by driving pin 12 from a low impedance external source such as a normal TTL output. Taking pin 12 high will hold the MPX oscillator output high, whilst taking pin 12 low will hold the output low. In this way the multiplexed BCD outputs of the ZN1040 can be synchronised to an external clock. This can be useful if, for example, the BCD output data is to be compared, digit by digit, with some preset limit. In this case the MPX frequency must at least be four times the input frequency to ensure that each digit has been compared before the next input pulse arrives.

The MPX input can be overdriven at frequencies up to 1 MHz which means that the BCD outputs can be compared at count frequencies up to 250 kHz.

3.4 Multiplex Sequence Generation

The output of the MPX oscillator is connected to the clock input of a sequence generator which is essentially a four-stage ring counter. This produces a sequence of four output pulses which are used to gate the BCD outputs, in sequence, on to the four output lines as shown in figure 9.

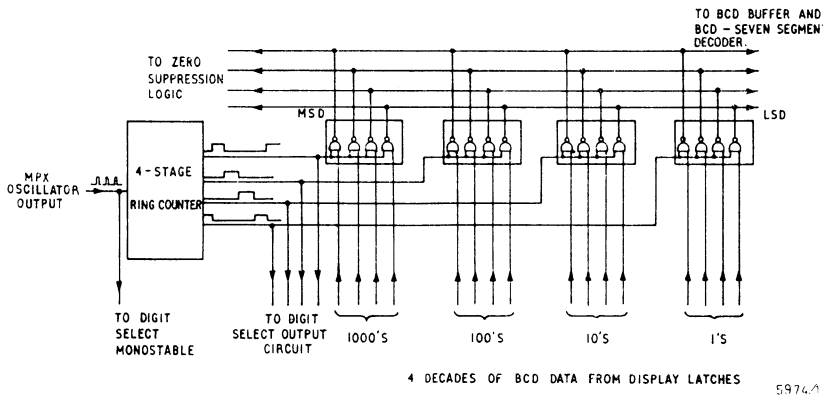


Fig. 9. Operation of Digit Multiplexing Circuit

3.5 Digit Select Output Circuit

The four digit select outputs are derived from the outputs of the MPX sequence ring counter using the circuit shown in figure 10.

To minimise digit drive overlap they are first passed through NAND gates, and a monostable triggered by the MPX oscillator takes a 200 ns 'bite' from the high-going edge of each pulse to provide interdigit blanking.

Further gating allows the selection of either high-going or low-going digit select pulses, thus allowing either common-anode or common-cathode displays to be driven using simple circuits. When the digit select sense input (pin 13) is high then the digit select pulses are high-going, when this input (pin 13) is low the digit select pulses are low-going. A timing diagram for high-going digit select pulses is given in figure 11. For low-going pulses the digit select waveforms are simply inverted. One digit select equivalent output circuit is shown in figure 12.

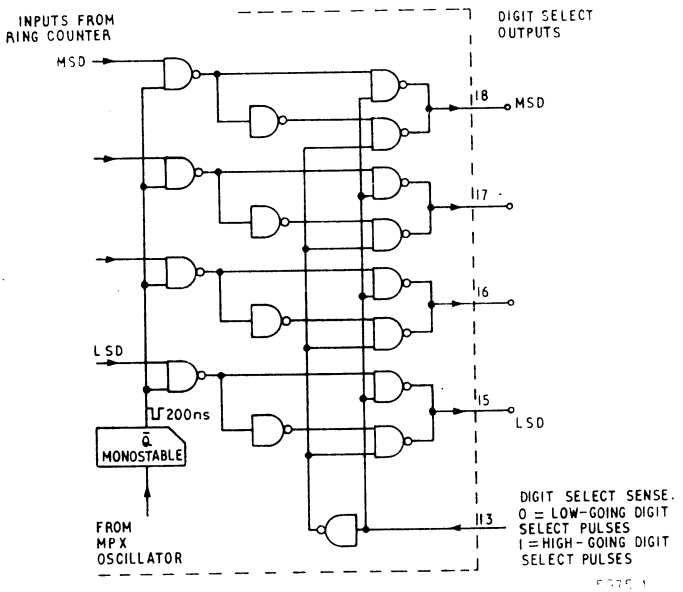


Fig. 10. Digit Select Logic

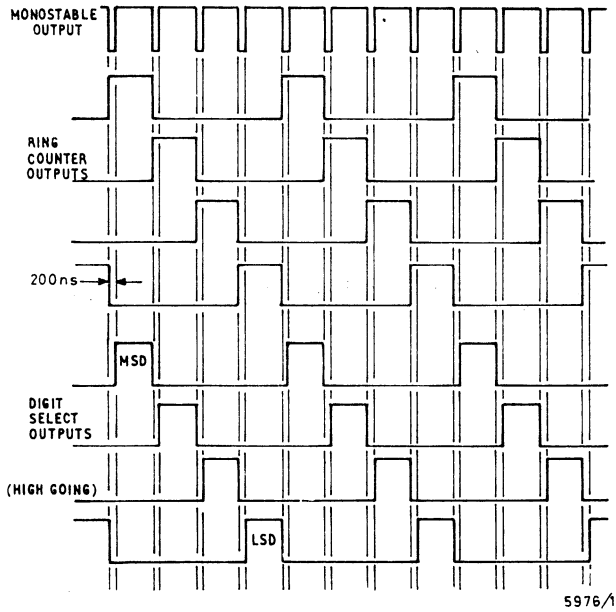


Fig. 11. Digit Select Timing

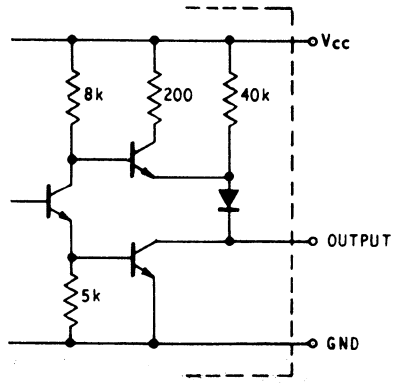


Fig. 12. Digit Select Output Circuit

3.6 Seven-segment Outputs

The seven segment outputs (pins 4-7, 9-11) are active low and can sink at least 50 mA in the case of the ZN1040E and 40 mA in the case of the ZN1040AE. The segment cathodes of common-anode displays may thus be driven directly. Display driving is discussed in detail in section 5. The output circuit for one segment is shown in figure 13.

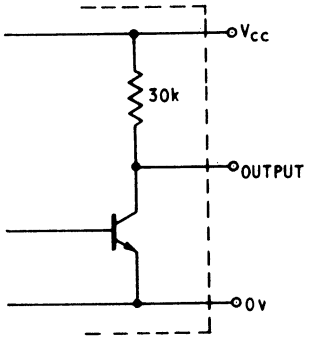


Fig. 13. Segment Output Circuit

3.7 BCD Outputs

The BCD output for each digit appears on the BCD output lines synchronous with the appropriate digit select pulse. However, since the MPX sequence gating is driven directly from the ring counter outputs, there is no inter-digit gap between one set of BCD data and the next. During the transition between digits the BCD data must therefore be considered invalid. If the BCD data is to be utilised (e.g. stored in an external latch or compared) then the simplest way to overcome this problem is to make use of the leading edge of the digit select pulse to indicate when the data is valid. This is illustrated in figure 14.

Similar comments also apply to the seven-segment outputs, but since these are normally used only for display driving, the problem does not usually arise.

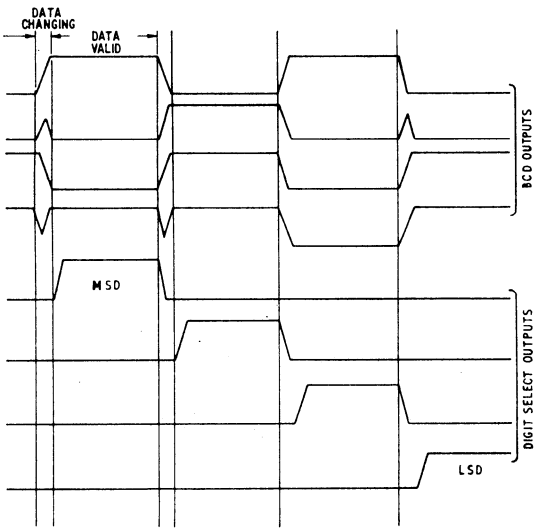


Fig. 14. BCD Output Timing

SECTION 4. ZERO SUPPRESSION, BLANKING, DECIMAL POINT AND LAMP TEST

The ZN1040 provides automatic blanking of leading zeroes in the display, thus improving readability. A decimal point input is also provided which allows leading zeroes to be displayed where these occur after the decimal point. A blanking input is provided to inhibit the display together with a lamp test input to check the operation of all display segments.

These sections of the ZN1040 circuit are shown in figure 15.

4.1 Blanking

Operation of the blanking input is extremely simple. When this input is high the seven-segment decoder functions normally and when this input is taken low the output of AND gate N6 goes low and the seven segment output transistors are all turned off, blanking the display.

4.2 Zero Blanking

Zero blanking operates on the principle of leaving the display blanked until non-zero data is detected at the outputs of the digit select gates. The trailing edge of the LSD output of the ring counter triggers a monostable which sets flip-flop N4/N5. The output of N4 holds one input of N6 low and the display is therefore blanked. It remains blanked until a non-zero digit appears on the BCD data bus, thus taking one or more of the inputs of NOR gate N3 high. The output of N3 then goes low resetting flip-flop N4/N5 so that the leading non-zero digit and all subsequent digits are displayed.

Should all four digits be zero then the flip-flop will be reset when the LSD output of the ring counter goes high and the output of N1 goes low. This ensures that the right hand digit (LSD) is always displayed, even if zero.

4.3 D.P. Input

If not used, the decimal point input is normally held high. If a decimal point is used in the display then the D.P. input can be utilised to prevent the possibility of a blanked digit appearing after the decimal point. This is achieved by feeding a low-going pulse into the D.P. input synchronously with the digit select pulse for the digit where the decimal point is to appear. This resets flip-flops N4/N5 so that the display is unblanked for this digit and all subsequent digits even if there are leading zeroes after the decimal point. Depending on whether the display has left or right-hand decimal points the display will be of the form .0 —— or 0. ——. If there is to be a decimal point before the MSD then left-hand point displays must obviously be used. If no leading zero blanking is required then the D.P. input is simply grounded, when all digits will be displayed.

A timing diagram for the D.P. input is shown in figure 11. Applications circuits using the decimal point are given in section 5. It should be pointed out that the ZN1040 does not produce an output to drive the decimal point of a display, this must be done using a simple external circuit several of which are shown in section 5.

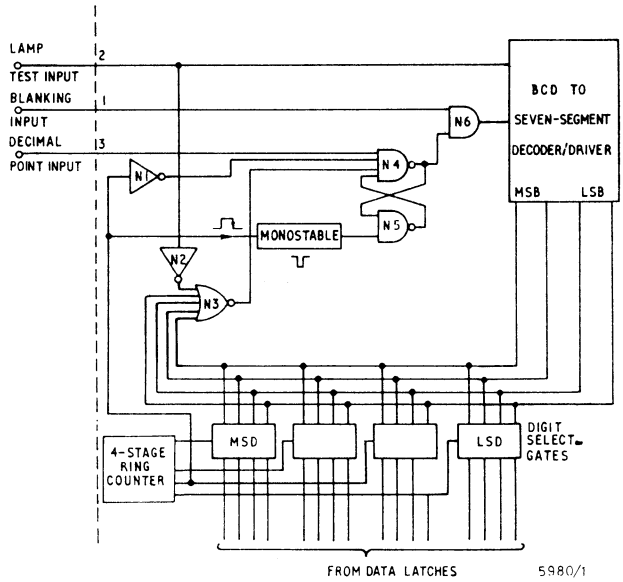


Fig. 15. Zero Suppression, Lamp Test and Blanking

4.4 Lamp Test

Operation of the lamp test function is quite simple. Taking the lamp test input low applies the BCD code 1000 (8) to the inputs of the BCD seven-segment decoder/driver. Simultaneously flip-flop N4/N5 is reset via N2 and N3, the output of N6 goes high, the display is unblanked and displays 8888. The blanking input must be high for lamp test to operate as a low blanking input will override the lamp test input and blank the display.

SECTION 5. USING THE ZN1040

5.1 Driving Common Anode LED Displays

Common anode LED displays can be driven with a minimum of external components, using the circuit of figure 16. The segment cathodes are driven directly (via current limit resistors) whilst the low going digit outputs turn on PNP digit drive transistors. As the display is multiplexed, and each digit is thus active for only a quarter of the time, the segment resistors should be chosen to give a peak current of approximately four times the required average current by using the equation:

$$R = \frac{V_{CC} - V_f}{4I_S}$$

V_{CC} = supply voltage (volts)
V_f = LED forward voltage drop
I_S = average segment current (A)
R = segment resistance (Ω)

The base resistors of the PNP digit drive transistors should be chosen such that the transistors receive sufficient base current to turn them fully on.

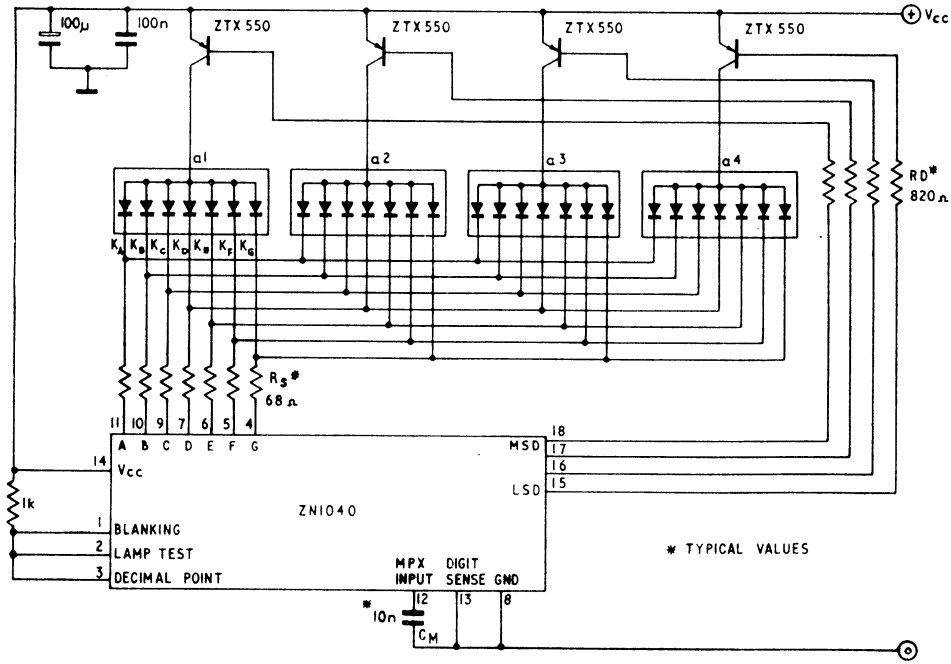


Fig. 16. Interfacing to Common-Anode LED Displays

5.2 Driving Common Cathode LED Displays

A circuit for driving common cathode LED displays is given in figure 17. Since the segment outputs are only active low it is necessary to use PNP segment drive transistors. High going digit select outputs are used to turn on NPN digit drive transistors. As with the common anode display, the segment resistors should be chosen to give the required segment current, and the transistor base resistors should be chosen to turn the transistors hard on. In both cases it is advisable to use displays which are optimised for multiplexed operation. Note that, since the digit outputs have to supply a significant base current to the digit drive transistors, the high level output voltage is less than the minimum specified to drive a TTL input. The digit select outputs therefore cannot be used as normal logic outputs with this circuit configuration.

Good decoupling of the supply to the ZN1040 is essential to avoid erratic counting and other problems. This is especially true when displays are being driven because of the large current pulses taken by these devices. It is therefore recommended that an electrolytic capacitor of between 100 μF and 1000 μF and a 100 nF ceramic capacitor be connected between $+V_{CC}$ and ground, as close as possible to the appropriate pins of the ZN1040.

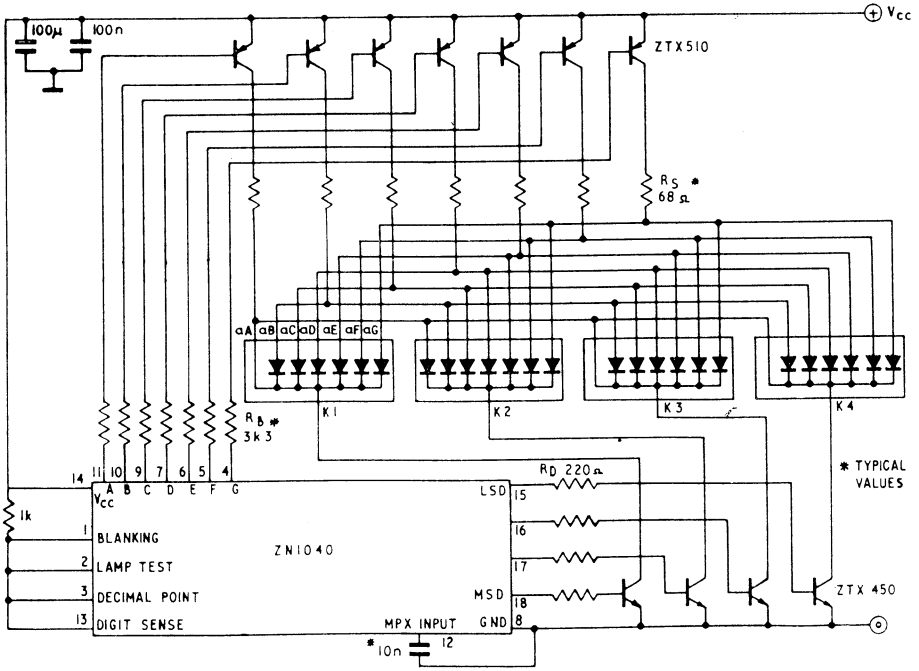


Fig. 17. Interfacing to Common-Cathode LED Displays

5.3 Using the Decimal Point Input

(a) Common Anode Display

Figure 18 shows a circuit which allows a decimal point to be displayed before any one of the display digits. When all the decimal point inputs are low then the 'wire-ANDed' outputs of N5 to N8 are all high and no decimal point is displayed. If for example D.P. input 2 is taken high then, when digit select output 2 goes low, both inputs of N6 will be high. The output of N6 will therefore go low synchronous with the digit 2 select pulse which will apply a low going pulse to the D.P. input of the ZN1040 to unblank the display and also to the decimal point cathode of the display to light decimal point 2.

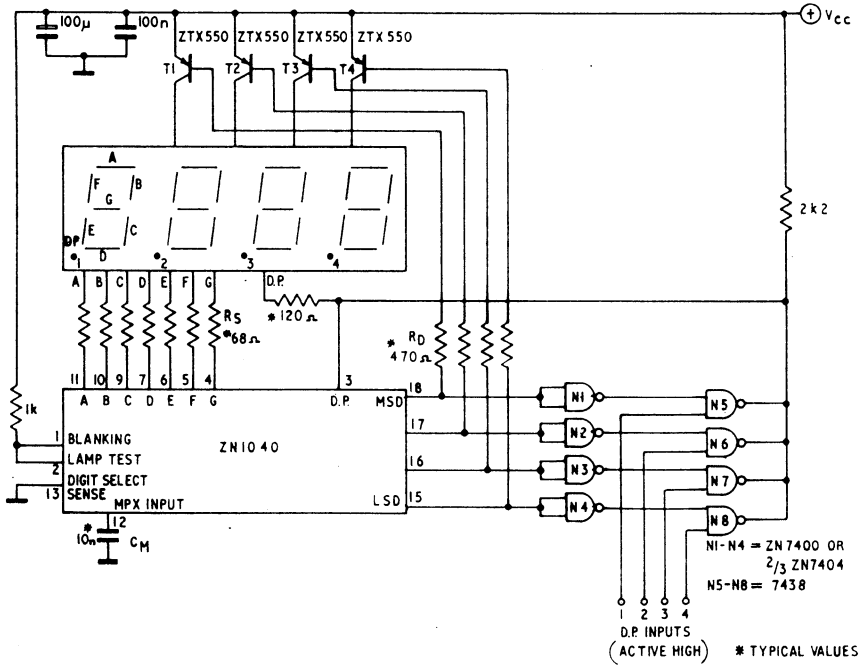


Fig. 18. Driving a Multiplexed Common-Anode Display with Decimal Point

(b) Common Cathode Display

The principle of this circuit is identical to that of figure 18 with minor circuit differences to take account of the different type of display. The digit select outputs are high-going, therefore no inverters are required at the inputs of the NAND gates. However, since the digit select outputs are used as logic outputs (see 5.2), buffers N1-N4 are interposed between them and the digit drive transistors. The wired AND output of N5-N8 turns on T8 when it goes low synchronous with the chosen digit select pulse thus driving the decimal point anode.

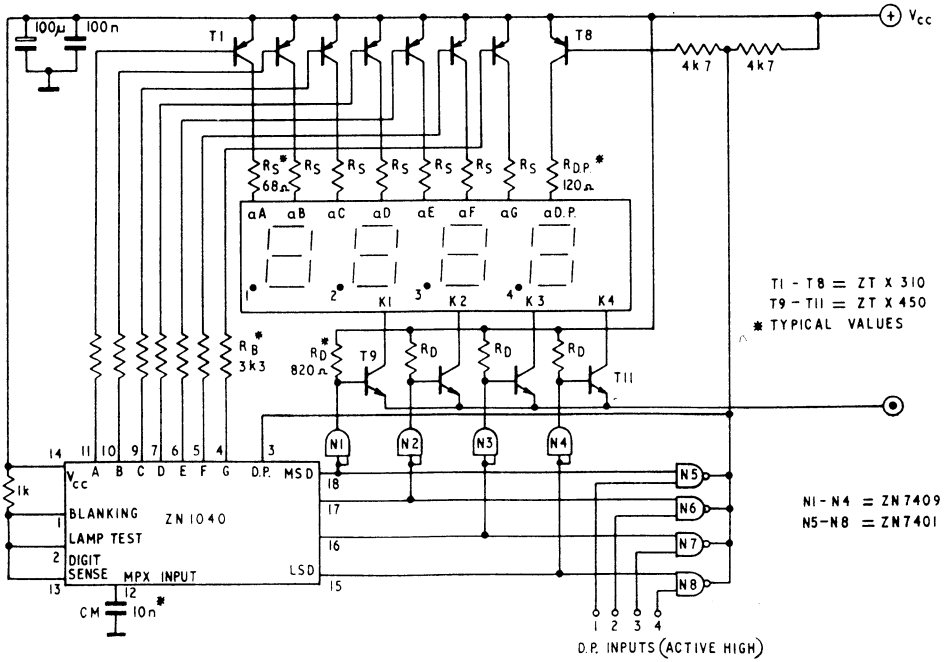


Fig. 19. Driving a Multiplexed Common-Cathode Display with Decimal Point

5.4 Cascading the ZN1040

If a count greater than 4 digits is required then two ZN1040's may be cascaded using the carry/borrow output; or additional TTL decade counters may be added. To cascade two ZN1040's the carry/borrow output of the less significant counter is connected to the inhibit input of the more significant counter and the count inputs are linked as shown in figure 20. The M.S.C. is thus inhibited until after the 9999th clock pulse when the inhibit input will be taken high by the carry output of the L.S.C. On the leading edge of the 1000th clock pulse the M.S.C. count will increase by 1 whilst the L.S.C. count will go to zero. After the carry propagation delay the carry output of the L.S.C. will go low and the M.S.C. will again be inhibited. A timing diagram for this sequence of events is shown in figure 21.

The leading zero blanking facility of the ZN1040 cannot be used directly in this application since the blanking circuits would operate independently for each device, leading to gaps in the display when the count was 999 or less, e.g. – – – 0 – 456.

This problem can be overcome by grounding the D.P. inputs of both counters thus inhibiting the zero blanking, or alternatively the D.P. input of the L.S.C. may be grounded giving zero blanking only on the first three digits of the M.S.C. If full zero blanking is required then the circuit given in Section 5.5 should be used.

When ZN1040's are cascaded then separate display interfacing will be used for each set of four digits.

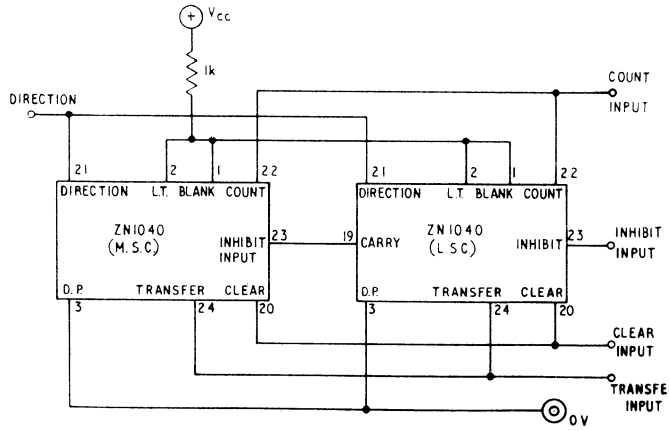


Fig. 20. Cascading ZN1040's without Leading Zero Blanking

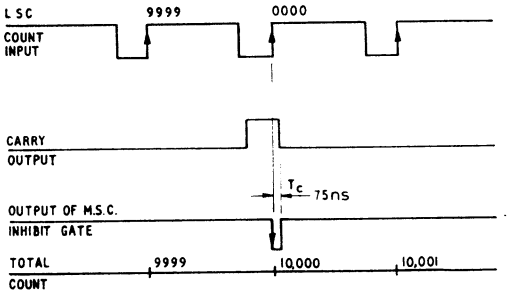


Fig. 21. Timing Diagram for Cascaded ZN1040's

5.5 Cascading ZN1040's with Leading Zero Blanking

The circuit of figure 22 allows cascading of two ZN1040's with full leading zero blanking. It operates by monitoring the BCD outputs of the more significant counter. When these are all zero this counter is blanked and the less significant counter is allowed to operate with leading zero suppression. When any of the BCD outputs is non-zero then the M.S.C. is unblanked and operates with leading zero suppression whilst the zero blanking of the L.S.C. is inhibited. The BCD outputs of the M.S.C. are monitored by a four input open collector NOR gate comprising N2 and N3. Whilst the multiplexed BCD data is zero the outputs of N2 and N3 are high, the output of N1 is low, so that M.S.C. is blanked. The output of N4 holds the D.P. input of the L.S.C. high and therefore the leading zero blanking operates normally.

If, at any time during the multiplex sequence, the BCD data is non-zero, then the output of N2 or N3 will go low discharging C1 rapidly. The D.P. input of the L.S.C. will thus be pulled low, inhibiting the zero blanking, whilst the output of N1 is high, unblanking the M.S.C. If only one of the BCD digits is non-zero, then C1 will be discharged only once during each multiplex sequence and will charge in the interval. The time constant (R2 + R3) C1 must therefore be made considerably longer than one multiplex sequence to ensure that the input to N1 remains low in this event.

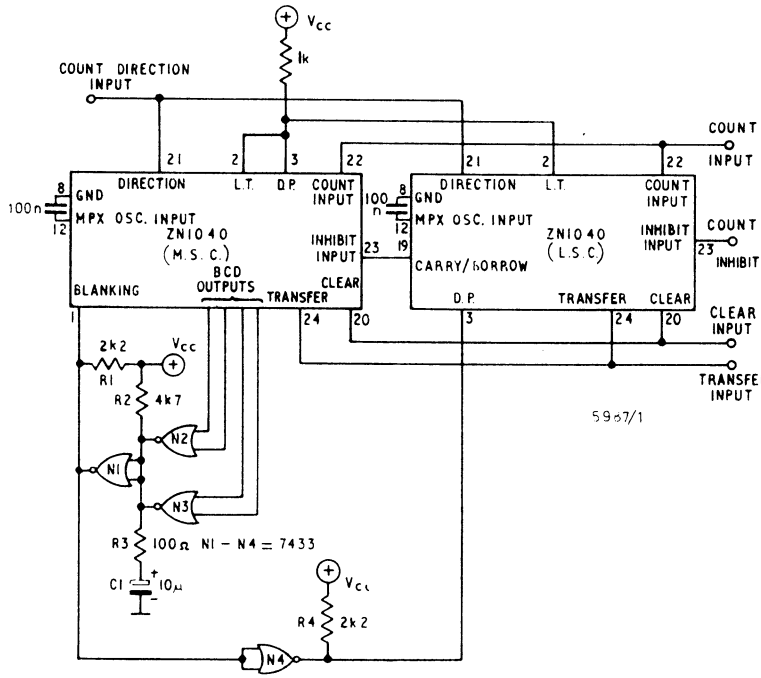
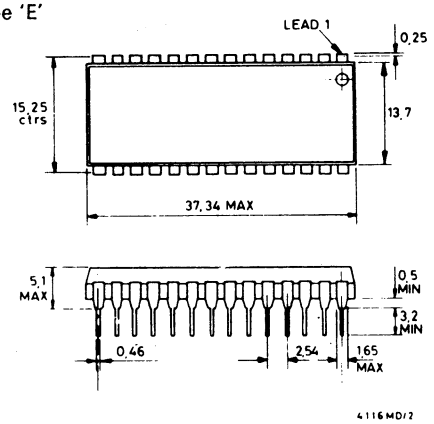


Fig. 22. Cascading ZN1040's with Leading Zero Blanking

ZN1040ERD

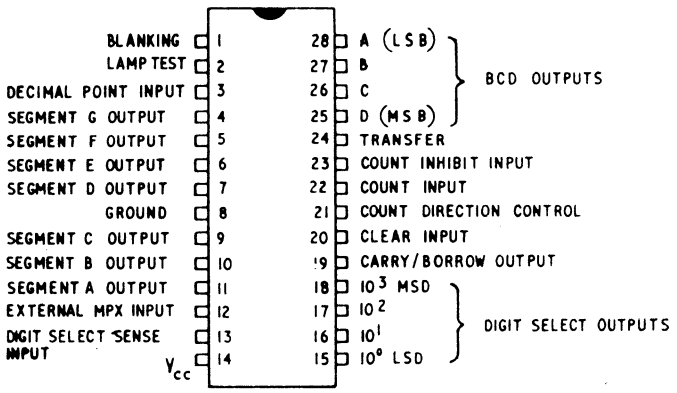
PACKAGE DETAILS

Conforms to SO-119 Type 'E'



28 LEAD MOULDED DIL (E28)

Dimensions in millimetres



Pin Connections

FERRANTI
semiconductors

ZN1060E

Switch Mode Controller-Driver

FEATURES

- Stabilised power supply
- Low supply voltage protection
- Linear pulse width modulator
- Programmable duty cycle
- Programmable soft start
- Double pulse suppression
- High speed current limiting
- Loop fault protection
- Uncommitted error amplifier
- Overvoltage protection
- Remote on/off switching
- Secondary current monitoring
- Multiple device synchronisation
- Core saturation protection

DESCRIPTION

The ZN1060E is a high performance monolithic integrated circuit switching regulator control chip designed for use in a variety of power control applications such as switching power supplies, D.C./D.C. converters and motor speed control.

This 16 pin D.I.L. package incorporates all the control and protection functions required in a switched mode power supply including a linear trailing edge pulse width modulator with double pulse suppression logic, error amplifier, temperature compensated voltage reference, high speed current limit, overvoltage/undervoltage protection, de-magnetising antisaturation protection and remote shut down facilities. The ZN1060E has been characterised for operation over the temperature range −20 to +85°C.

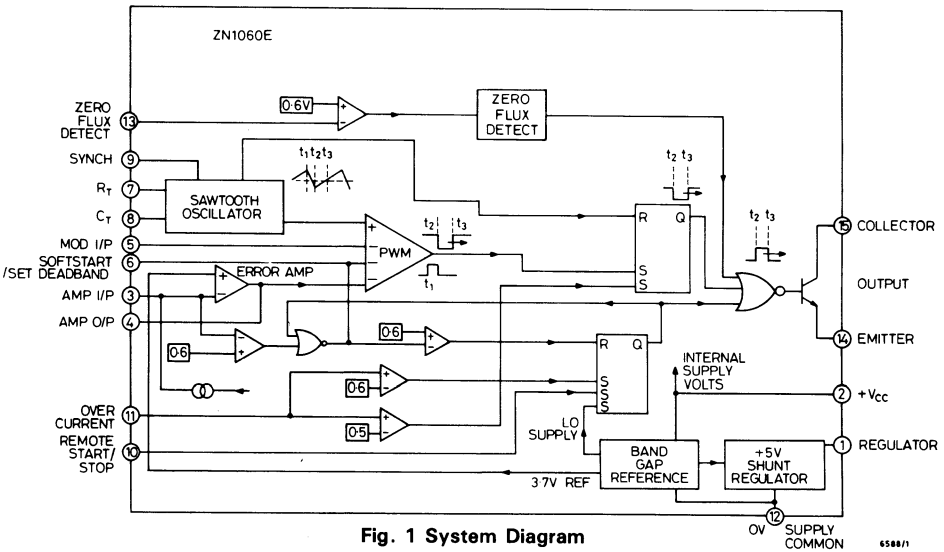


Fig. 1 System Diagram

ZN1060E

ABSOLUTE MAXIMUM RATINGS

Dissipation	350mW
Output Current Sink	40mA
Collector Supply Voltage	6V
Thermal Resistance : Junction/Case	65°C/W
Thermal Resistance : Junction/Ambient	110°C/W
Operating Temperature Range	−20 to +85°C
Storage Temperature Range	−55 to +150°C

D.C. ELECTRICAL CHARACTERISTICS at $T_{amb} = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

Parameter	Symbol	Test Limits			Units	Test Conditions
		Min.	Typ.	Max.		
REFERENCE SECTION						
Output voltage	V_{REF}	4.75	5	5.30	V	$I_C = 20mA$
Slope resistance	R_S	–	2	4	Ω	
Temperature coefficient	TC	–	100	–	ppm/°C	
AMPLIFIER SECTION						
Open loop gain	A_O	–	60	–	dB	
Input bias current	I_3	–	4	40	μA	
External feedback resistor	$R_{3\text{-}12}$	100	–	–	kΩ	
Reference voltage	V_{REF}	3.42	3.72	4.03	V	
Reference temperature coefficient	$\Delta V_{REF}/\Delta T$	–	100	–	ppm/°C	
Output voltage swing positive	V_{oh}	3	–	–	V	
Output voltage swing negative	V_{ol}	–	–	0.4	V	
OSCILLATOR SECTION						
Frequency range	f	50	–	100K	Hz	
External capacitor	C_T	1	–	–	nF	
External resistor (Pin 7)	R_T	10	–	40	K	
Duty cycle range		0	–	98	%	
Sawtooth						
Upper level	V_{RH}	–	3	–		
Lower level	V_{RL}	–	1.1	–	V	

Parameter	Symbol	Test Limits			Units	Test Conditions
		Min.	Typ.	Max.		
MODULATOR						
Modulator input current	I_{5-12}	–	4	40	μA	Voltage on PIN 5 = 1V
PROTECTION FUNCTIONS						
Pin 6 duty cycle limit control	V_6	39	41	43	% of V_Z	{For 50% max. / 15 to 50kHz}
Pin 6 input current	I_{6-12}	–	0.5	20	μA	$V_{IN} = 2V$
Pin 1 low supply voltage protection threshold	V_{LT}	3.5	4	4.5	V	
Pin 3 feedback loop trip on threshold	V_{3-12}	472	600	720	mV	
Pin 3 pull up current	I_3	–	15	35	μA	
Pin 13 demagnetisation/ overvoltage trip on threshold	V_{13-12}	–	600	–	mV	
Pin 13 input current	$I_{\times 13}$	–	1.3	5	mA	$V_{IN} = 2V$
EXTERNAL SYNCHRONISATION						
Pin 9 OFF	V_{9-12}	0	–	0.8	V	
ON		2	–	5.25	V	
Sink current	I_{9-12}	–	–	100	μA	
REMOTE ON/OFF						
Pin 10 ON	V_{10-12}	2	–	5	V	$V_{CC} = 5V$
OFF	V_{10-12}	0	–	0.8	V	
Sink current	I_{10-12}	–	–	100	μA	$V_{11-12} = 250mV$
CURRENT LIMIT						
Pin 11						
Current limit	V_{11-12}	0.40	0.48	0.58	V	
Shutdown/slow start	V_{11-12}	0.47	0.60	0.72	V	
Sink current	I_{11-12}	–	–	450	μA	
OUTPUT STAGE						
Output current Pin 15	I_{15}	40	–	–	mA	
Maximum emitter voltage pin 14	V_{14-12}	–	–	5	V	
Collector saturation voltage pin 15	V_{15-12}	–	0.4	–	V	
SUPPLY CURRENT		–	12	20	mA	$V_{1-12} = 5V$

Figure 1 ZN1060E System Diagram

As with every integrated circuit for use in switching converters it includes:

(i) An internal oscillator that can be synchronised.

(ii) An error amplifier.

(iii) A pulse width modulator P.W.M.

(iv) A precision voltage reference 3.72V internal, 5V external.

(v) A control and starting system.

In addition to the above features the ZN1060E includes:

STOP START CIRCUIT Figure 3.

A RS bistable can be set by three different functions:

1) Remote on/off on pin 10.

2) Overcurrent protection on pin 11.

3) Low supply voltage protection (internal).

As soon as one of these functions cause a setting of the bistable, the output pulses are blocked via the output gate. At the same time transistor T1 is switched-on resulting in a discharge of the soft start capacitor on pin 6. The function of this protection circuit is to stop the output pulses as soon as a fault occurs and to keep the output stopped for several periods. After this dead time, the output starts with a very small gradually increasing duty cycle. When the fault is persistent, this will cause a cyclic switch-off/switch-on condition. This automatic reset mode limits the energy during fault conditions. The realisation and the working of the circuit is indicated in Fig. 6. The dead-time and soft-start are determined by an external capacitor that is connected to pin 6, the duty cycle programme pin (Δmax. setting).

The discharging current is limited by an internal 50Ω resistor in the collector of T1. The voltage at pin 6 decreases to below the lower level of the sawtooth. When V6 has dropped to 0.6V, this will activate a comparator and the bistable is reset. The output stage is no longer blocked and T1 is cut off. Now V_Z will charge the capacitor via R1 to the normal max. voltage. The output starts delivering very narrow pulses as soon as V6 exceeds the lower sawtooth level. The duty-cycle of the output pulse now gradually increases to a value determined by the feedback on pin 3, or by the static Δmax. setting on pin 6.

REMOTE ON/OFF CIRCUIT (PIN 10)

In systems where two or more power supplies are used, it is often necessary to switch these supplies on and off in a sequential way. Furthermore, there are many applications in which a supply must be switched by a logic signal. This can be done via the TTL-compatible remote on/off input on pin 10. The output pulse is inhibited for levels below 0.8V. The output of the IC is no longer blocked when the remote on/off input is left floating or when a voltage of 2V or more is applied. Starting up occurs via the slow-start circuit.

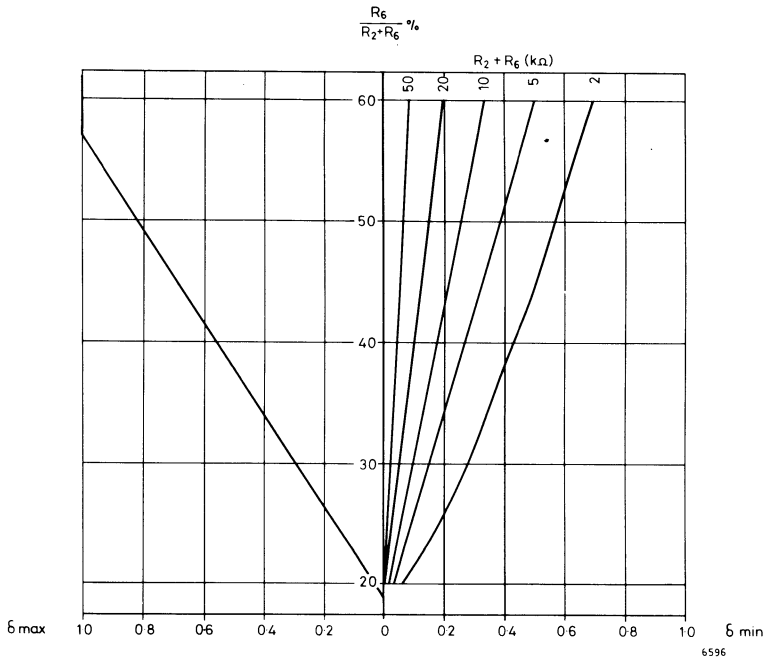


Fig. 2 Typical End Stop Characteristic

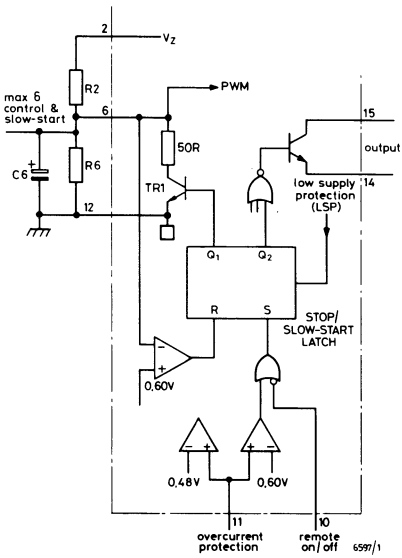


Fig. 3 Stop/Slow-Start Circuit

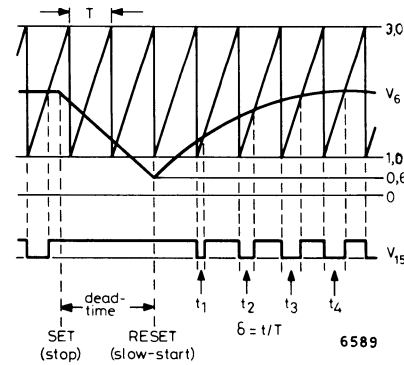


Fig. 4 Waveforms Associated with the Stop/Slow-Start Circuit

LOOP FAULT PROTECTION

When the SMPS feedback loop is interrupted, the error amplifier would settle in the middle of its active region because of the feedback via the resistor connected between pin 3 and pin 4 (3-4). This would result in a large duty cycle. A current source on pin 3 prevents this by pushing the input voltage high via the voltage drop over R(3-4). As a result, the duty cycle will become zero, providied that R(3-4) >100K. If the feedback loop is short circuited, the duty cycle would jump to the adjusted maximum duty cycle. Therefore an additional comparator is active for feedback voltages at pin 3 below 0.6V and an internal resistor of typically 1K is shunted to the impedance on the Δmax. setting pin 6. Depending on this impedance, Δ will be reduced to a value of Δ_0, typically 1% of the total period.

DUTY CYCLE LIMIT AND LOW SUPPLY OPERATION

A potential divider across V_Z and connected to pin 6 allows external adjustment of the duty cycle Δ from 0 to 95%. in the flyback system Δmax. = 45% and $\Delta_0 = 1\%$ i.e. approximately 2μs. Further Δ is maintained at 0 as long as the chip supply remains below V_Z. A capacitor connected to pin 6 can be used to slow down the rate of increase of Δ from 0 to its normal value. A soft start characteristic is thus obtained. See Fig. 4.

SECONDARY CURRENT MONITORING (PIN 13)

The function of this circuit is to provide complete protection against all secondary overload effects with automatic reset. It is only after this input signal has disappeared can a new period of primary current start.

This information can be taken from an auxillary winding on the output transformer that gives a signal similar to the primary collector voltage but referenced to zero voltage as shown in Fig. 9.

As long as the secondary current has not decreased to zero, the primary collector voltage remains high. At the time the secondary current becomes zero the collector voltage on the output transistor decreases to V_{CC} (rectified mains) and stays at this level until the beginning of the new primary current low. On the auxillary winding the voltage remains positive during the flow of secondary current; it stays at zero during the time there is no primary or secondary current and is negative whilst primary current flows.

In the ZN1060E a comparator detects this positive voltage. It has a 600mV sensitivity to take account of the secondary short circuit case. If there is a secondary short circuit, the secondary winding is only loaded by a single diode carrying a high current. The voltage across the secondary winding will then be only about 1 volt. To minimise power losses and utilise a convenient winding ratio a comparator of this sensitivity is required. The logic processor ignores ringing on the input waveforms.

OPERATING PRINCIPLE

The operating principle chosen is a C.E.T. system in which the primary current can only flow if the secondary current has reached zero, i.e. there is zero flux in the transformer core. The various possibilities are shown in the waveform diagrams in Fig. 5 which should be consulted.

Figure 8A-Normal Operation. The primary current flows in an essentially linear mode from 0 to I_{max} and then decreases very rapidly to zero. The secondary current then flows and decreases in a linear mode to zero. In normal regulating operation there is a dead period after the secondary current has stopped. During the dead time, the primary voltage reduces from about twice V_{CC} to V_{CC}. The ringing is due to leakage inductance and stray capacitance.

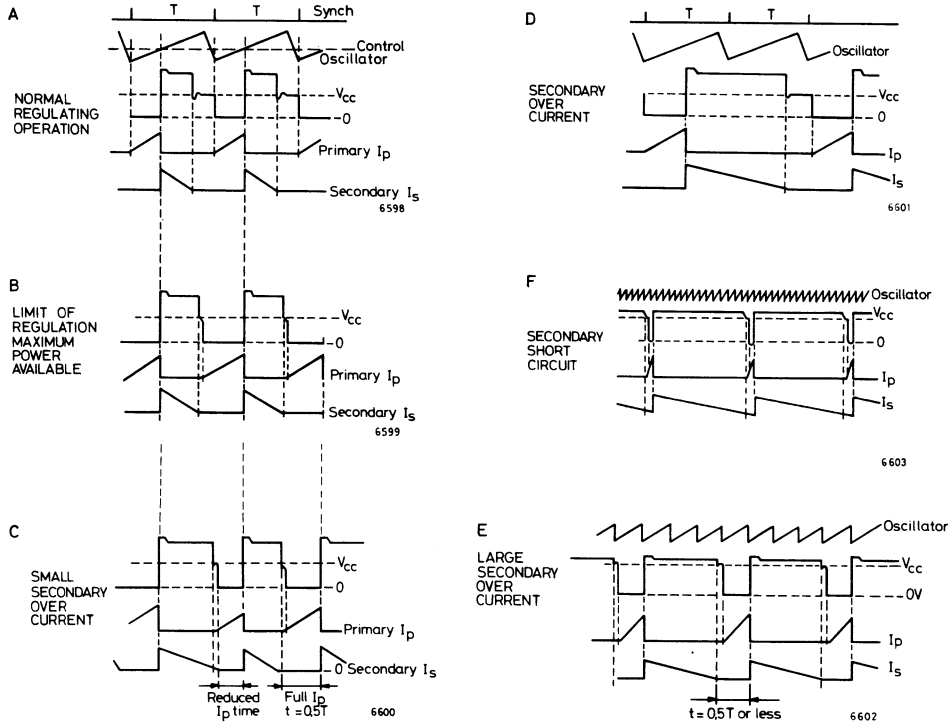


Fig. 5 Complete Energy Transfer Flyback Operating Waveforms

Figure 5B-Maximum Power. When the secondary power increases the control loop makes the primary flow sooner and the secondary circuit flows for a longer time. In the limit case when maximum output power is demanded, the primary current starts just after the previous secondary current has reached zero. This is the limit of regulation and the power is fixed by V_{CC} and the primary inductance.

Figure 5C-Small Overload. If the overload current continues to increase, the secondary current can continue to flow for longer than the total period. The following primary current pulse is inhibited but the next primary current pulse flows for a full half period.

Figure 5E-Large Overload. If there is an even greater secondary overload the primary current will be inhibited during several periods.

Figure 5F-Secondary Short Circuit. If the secondary is short circuited a large number of primary current pulses are inhibited until complete energy transfer has been completed and the secondary current has reached zero. Then a new normal primary current pulse will occur over a full half period.

It can thus be seen that with this principle complete protection is provided against secondary over currents or short circuits with automatic reset. It also provides a starting mode, because at switch-on, the secondary filter capacitors are effectively a short circuit, until they are charged up.

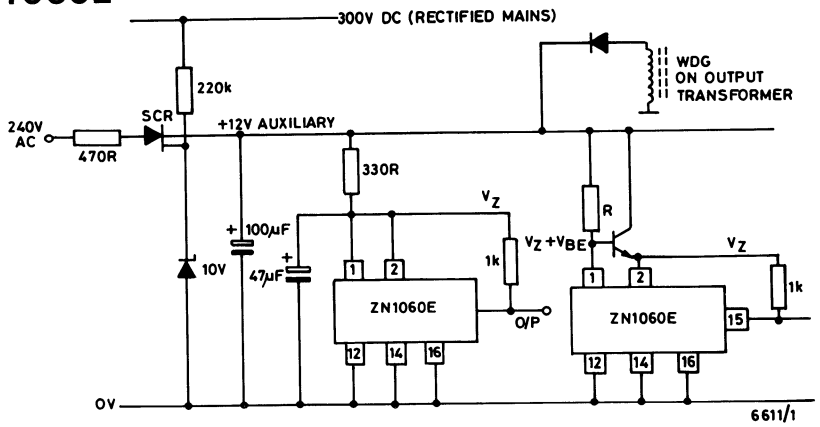


Fig. 6 Powering the ZN1060E

N.B. **Both** Pins 12 and 16 must always be connected to 0V (Ground)

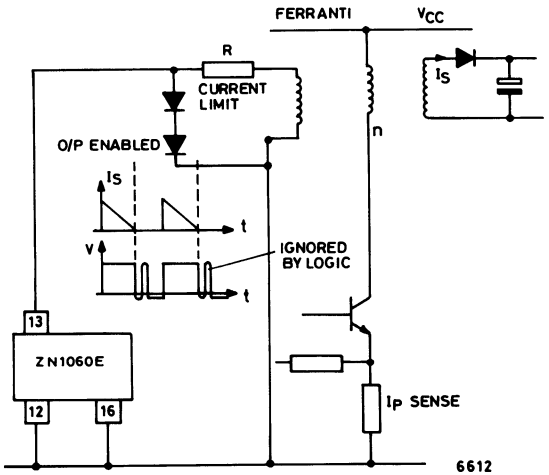


Fig. 7 Secondary Current Monitoring using the ZN1060E

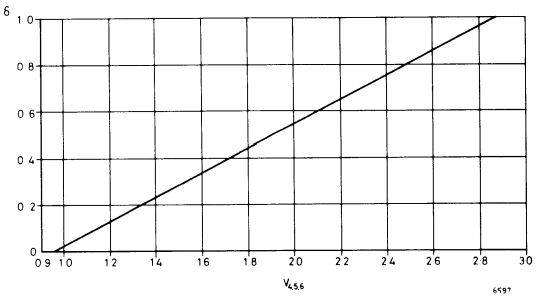


Fig. 8 Typical P.W.M. Characteristic

APPLICATIONS

Fig. 9 shows the schematic diagram for a 150 watt "off line" multiple output C.E.T. flyback circuit designed specifically for use in advanced European colour T.V. receivers. The design fulfills all the relevant specifications (V.D.E., CENELEC, B.S. etc.) with regard to noise E.M.I. and safety.

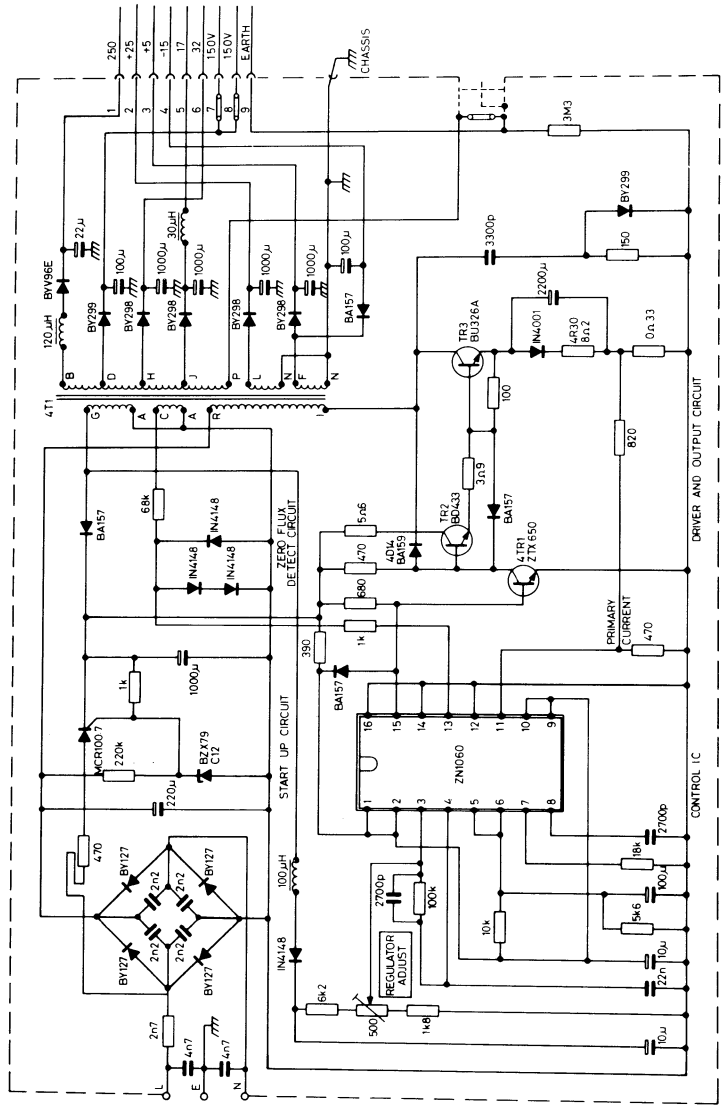


Fig. 9 Power Supply Schematic

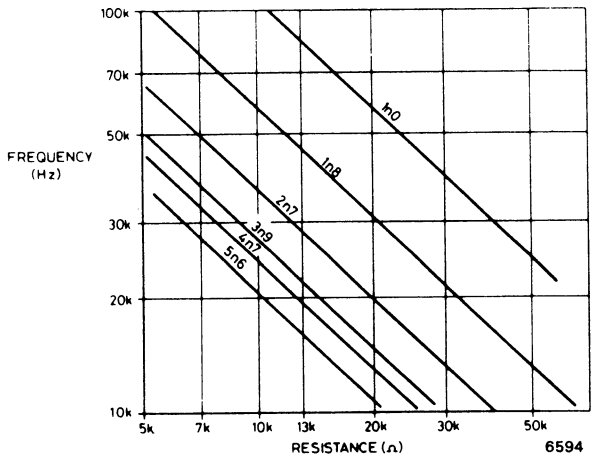
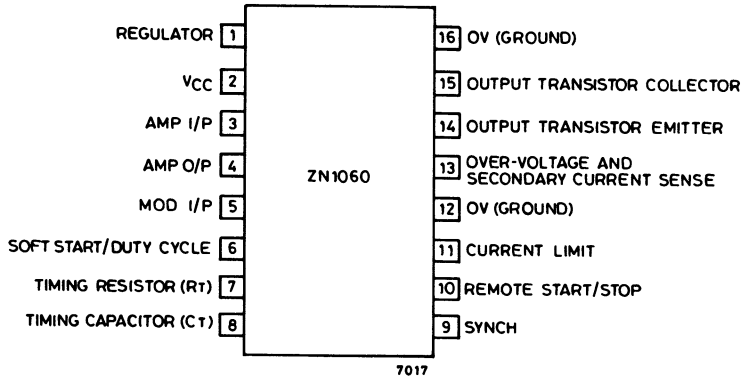


Fig. 10 Typical Oscillator Operating Frequency

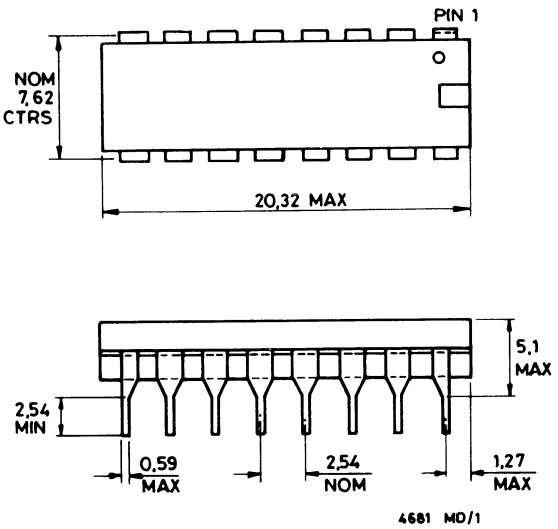
PINNING



N.B. BOTH PINS 12 AND 16 MUST ALWAYS BE CONNECTED TO OV (GROUND)

ZN1060E

PACKAGE DETAILS



16 Lead Moulded D.I.L.

FERRANTI semiconductors

ZN1066E
ZN1066J

Switching Regulator Control and Drive Unit

FEATURES

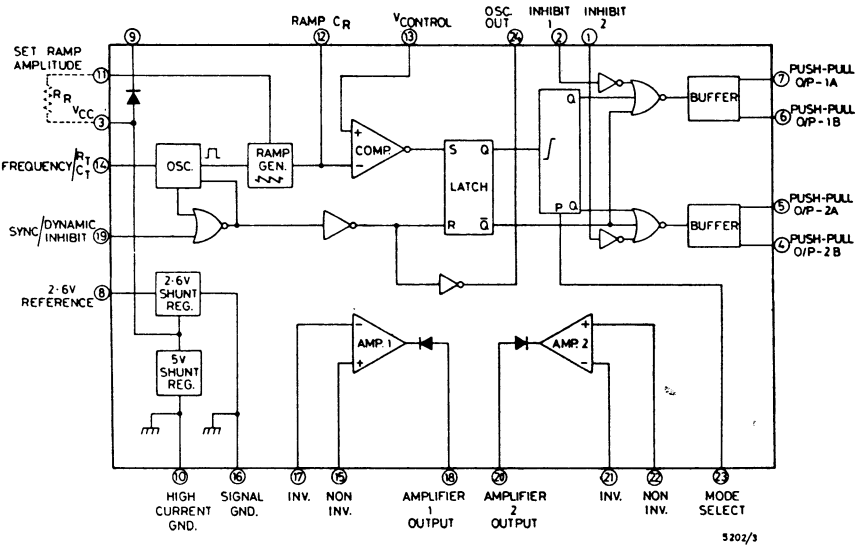
- Complete P.W.M power control circuitry
- Single ended or Push-Pull totem pole type outputs with ±120 mA capability
- 0 – 100% duty cycle control
- Feedback control guarantees non-overlap of output pulses
- No dead time setting required
- Output frequency adjustable up to 500 kHz
- Independent control of output voltage and output current
- 2.6V stable reference ±50 ppm/°C
- Inhibit and synchronising input

DESCRIPTION

The ZN1066 is designed to satisfy the requirement for a general purpose control and drive unit in switching power supplies, transformer coupled DC/DC converters, transformerless voltage doublers, polarity converters, motor speed control and other power control applications.

Included in a 24 lead D.I.L. package is a voltage reference, current control amplifier, voltage control amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating outputs, cross coupled output inhibits and a synchronising and shutdown facility

EQUIVALENT CIRCUIT



ZN1066E/J

ABSOLUTE MAXIMUM RATINGS –55°C to +70°C

Supply Current (I_{CC})	200 mA
Main Output Drive Currents	160 mA total
Clock Output Current (sink)	25 mA
Reference Current (sink)	10 mA
Ramp Control Current	1 mA
Bias Sourcing Current	1 mA
Operating Temperature Range:	
ZN1066J	–55°C to +125°C
ZN1066E	–40°C to + 85°C
Storage Temperature Range	–65°C to +150°C

ELECTRICAL CHARACTERISTICS (at 25°C ambient temperature).

Parameter	Min.	Typ.	Max.	Unit	Comments
Shunt Regulator Section: Output Voltage (I_{CC} = 60 mA)	4.75	5.0	5.25	V	See Notes 1 & 2
Voltage temperature coefficient (I_{CC} = 60 mA)	—	100	—	ppm/°C	
Output impedance	—	1.5	3	Ω	
Supply current	—	40	—	mA	Shunt regulator just on
Amplifier Section: Open loop voltage gain	800	1200	—		
Input bias current	—	1	4	μA	
Input offset current	—	0.2	2	μA	
Input offset voltage	—	2	5	mV	
Offset voltage temp. coefficient	—	10	—	μV/°C	
Output low (sinking 1 mA)	—	0.85	—	V	
Output high (sourcing 0.1 mA)	4.7	—	—	V	With 1k pull up
Output impedance	—	5	—	kΩ	
Common mode range	1	—	2.8	V	
Comparator Section: Common mode range	1	—	4.3	V	
Delay to output drive (±50 mV input)	—	0.17	0.3	μs	
Delay to output drive (±10 mV input)	—	0.2	—	μs	
Input bias current	—	1	4	μA	
Input offset current	—	0.2	2	μA	

Parameter	Min.	Typ.	Max.	Unit	Comments
Reference Section: Reference voltage (at 1 mA source)	2.4	2.52	2.62	V	See Notes 3 & 4
Temperature coefficient	—	50	—	ppm/°C	
Output impedance	—	1.5	—	Ω	
Mode Control Section: Single ended operation control input logic '1' (outputs 1A & 1B)	2.4	—	—	V	May be connected direct to V_{CC}
Push pull operation control input logic '0' (all outputs)	—	—	0.4	V	0V or left open circuit
Cross Couple Inhibits Section: Input logic '1' enables outputs	—	0.07	0.2	mA	See Note 5
Input logic '0' inhibits outputs	—	—	0.4	V	
Oscillator Section: Maximum frequency range	5×10^{-4}	—	500	kHz	Minimum value of $C_T = 1500$ pF
Initial accuracy	—	2	—	%	R_T C_T constant
Temperature stability	—	1	—	%	Over temperature range −55 to +125°C
Output pulse width	—	0.3	—	μs	$C_T = 1500$ pF
Output logic '0' (sinking 10 mA)	—	—	0.4	V	Buffered output Pin 24
Output logic '1' (sourcing 1 mA)	2.4	—	—	V	Buffered output Pin 24
Output Section: Output current	—	±60	—	mA	See page 20
Output logic '0' (sinking 60 mA)	—	0.3	0.4	V	Each output
Output logic '1' (sourcing 60 mA)	1.0	1.45	—	V	100 mA max. under short circuit conditions
Total Standby Current: V_{CC} at 2.5V, Output Current 4 mA	—	17	—	mA	Operation from V_{REF} to V_{CC} is permissible
V_{CC} at 5V, with outputs open	—	40	—	mA	

NOTES:

1. Decouple Pin 3 to GRD with 0.22 μF minimum as close to pins 3 and 10 as possible.
2. Pin 10 GRD for 5V regulator and output buffers.
3. Decouple Pin 8 to GRD with 0.22 μF minimum as close to Pins 8 and 16 as possible. V_{REF} will supply 1 mA max. without additional bias. Maximum sink current is 10 mA.
4. Pin 16 GRD for oscillator, ramp generator, comparator, amplifiers and 2.5V Reference.
5. The inhibit logic 1 current is the source current required to ensure digitally high operation. The base ground resistor is nominally 10 kΩ. Catching diodes to the 5 volt rail are included on-chip.

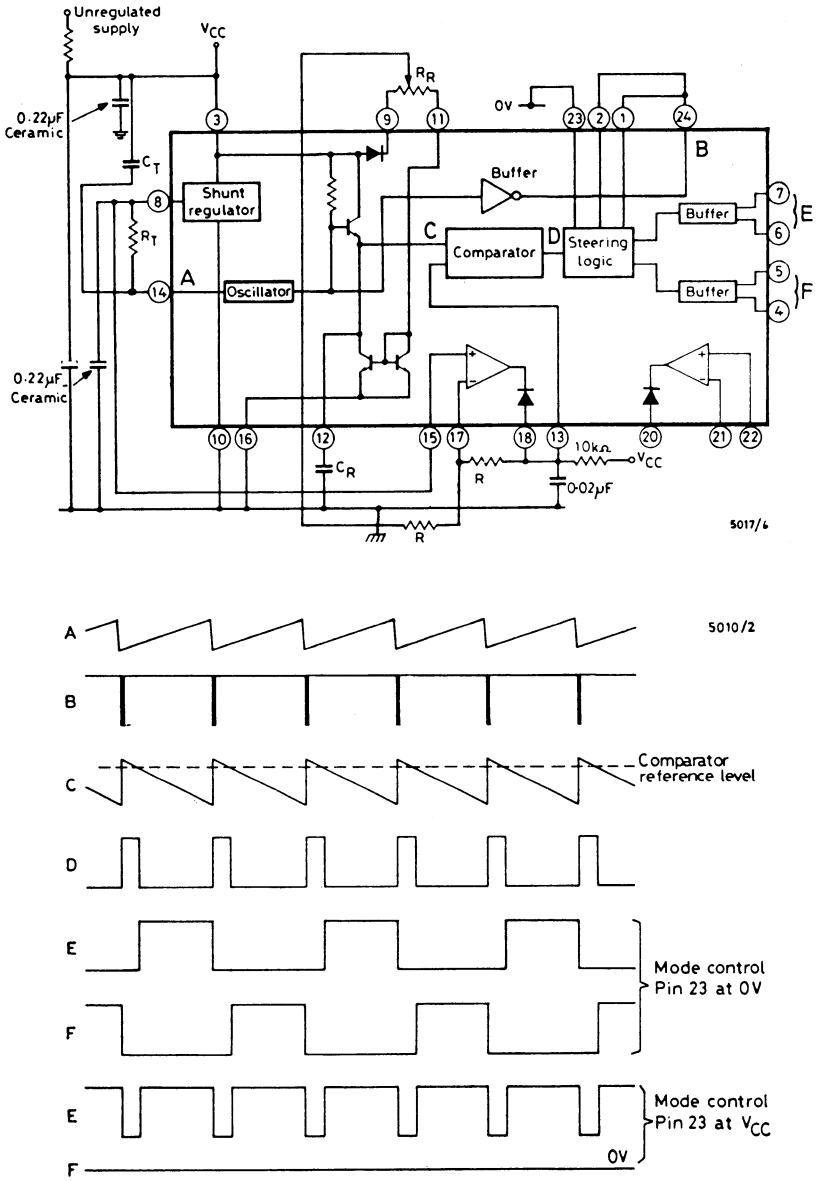
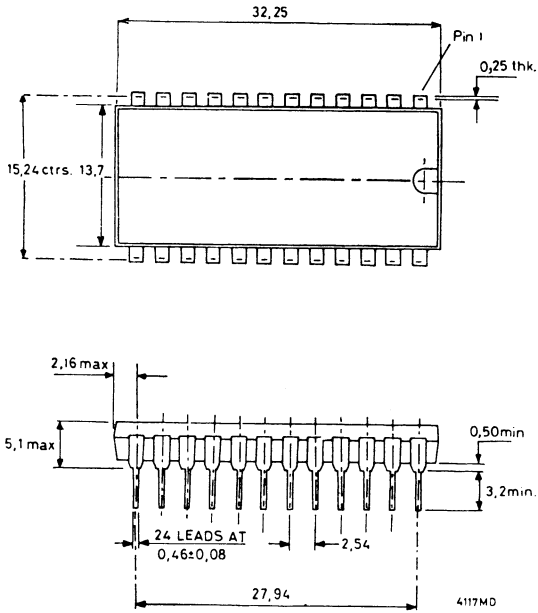


Fig. 1 Open loop Test Circuit and System waveforms



PACKAGE OUTLINE

24 Lead Moulded D.I.L.
SO-119 – Type 'D'

Dimensions in millimetres

PINNING DETAILS

Pin No.	Function	Pin No.	Function
1	Inhibit input 2	13	Comparator reference
2	Inhibit input 1	14	Oscillator frequency
3	V_{CC} (+5V)	15	Amplifier 1 non-inverting input
4	Push-pull output 2B	16	Low current ground
5	Push-pull output 2A	17	Amplifier 1 inverting input
6	Push-pull output 1B	18	Amplifier 1 output
7	Push-pull output 1A	19	Oscillator sync.
8	2.6 volt reference	20	Amplifier 2 output
9	Bias Supply	21	Amplifier 2 inverting input
10	High current ground	22	Amplifier 2 non-inverting input
11	Ramp bias current	23	Mode control
12	Ramp timing capacitor	24	Clock output

ZN1066E/J

APPLICATIONS INFORMATION

OSCILLATOR

The oscillator can be programmed, by means of an external timing resistor R_T and capacitor C_T, to define any time period in the range 2 seconds to 2 microseconds, (0.5 Hz to 500 kHz). The oscillator period is approximately $T_{osc} = 0.33\ C_T\ R_T$ where T_{osc} is in microseconds when R_T = ohms and C_T = microfarads. $3k \leqslant R_T \leqslant 100k$; $C_T \geqslant 1500$ pF.

Fig. 2 illustrates the operation of the oscillator.

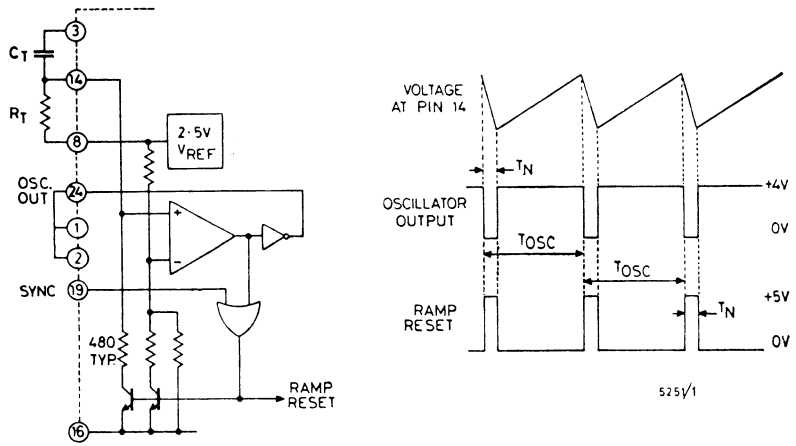


Fig. 2 Oscillator Equivalent Circuit

The discharge time of C_T, T_N, determines the width of the oscillator output pulse and the ramp reset time. In order to achieve satisfactory reset of the ramp generator the value of C_T must be at least 2.7 times that of the ramp capacitor C_R. For most practical applications $C_T = 3C_R$ will be found satisfactory. The oscillator pulse width is also used as a blanking pulse to both outputs to ensure that there is no possibility of having both outputs on simultaneously during transitions. The output dead time can be estimated from the relationship: $T_N \simeq 95\ C_T$ microseconds when C_T = microfarads.

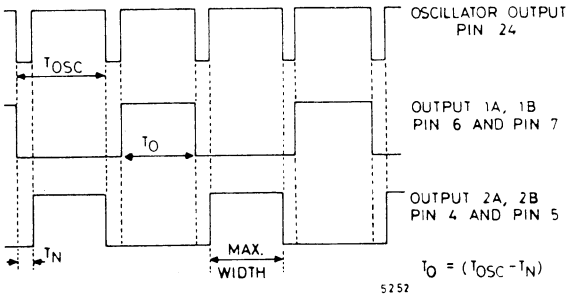


Fig. 3 Relationship between Oscillator & Output Waveforms

The frequency of the output waveform is approximately $f_o = 1.5/C_T R_T$. Note that f_o refers to the frequency of the outputs 1A, 1B (pins 6 and 7) or outputs 2A, 2B (pins 4 and 5). The frequency of the oscillator and ramp generator waveforms is twice f_o.

The oscillator period, T_{osc}, is virtually independent of the supply voltage down to $V_{CC} = 2.6V$. Further, the timing period will generally change by less than $\pm 0.5\%$ for a $\pm 50°C$ change in ambient temperature and the variation in timing period from one device to another is normally less than $\pm 2\%$ assuming R_T and C_T are kept constant.

If it is desired to synchronise a ZN1066 to an external clock, a pulse of +1V to +5V may be applied to the SYNCH input pin 19, with C_T R_T set slightly greater than the clock period. The width of this clock pulse should be greater than 0.2 μsec. If pin 19 is not used it can be left open circuit or connected to low current ground.

RAMP GENERATOR

The simplified equivalent circuit of the ramp generator is shown in Fig. 4.

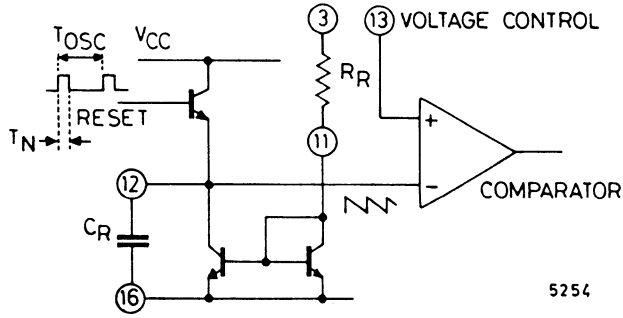


Fig. 4 Ramp Generator and Pulse Width Modulator

The ramp generator is driven by the reset pulse from the oscillator to charge the ramp timing capacitor C_R to 4.3V. This charge time must be sufficiently long to ensure that the ramp generator is reset to at least 4V. This condition is met by making $C_R \leqslant 0.33\ C_T$. At the end of the reset pulse C_R is discharged by a constant current defined by the ramp timing resistor R_R. The period of the ramp generator is identical to the oscillator timing period T_{osc}. The amplitude of the ramp is approximately $V_R = 1.33\ C_T\ R_T/C_R\ R_R$ which for a ramp amplitude of 3V pk – pk and $C_R = 0.33\ C_T$ gives $R_R \simeq 1.3\ R_T$. $4.3k \leqslant R_R \leqslant 100k$; $C_R \geqslant 330$ pF.

Fig. 5 shows the operating conditions for the ramp generator and pulse width modulator circuits.

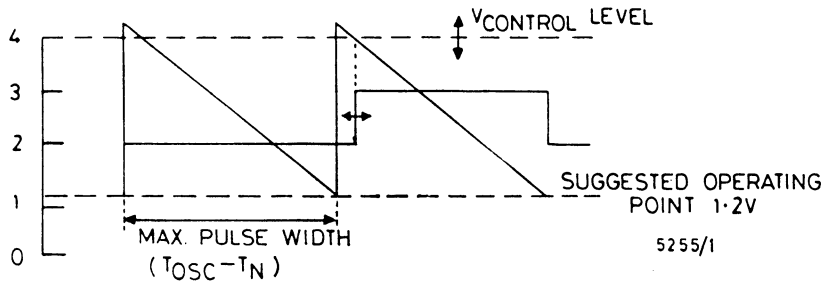


Fig. 5 Pulse Width Modulation

The ramp will cross the comparator reference point ($V_{control}$ level) at essentially the same time after set up independent of supply voltage and temperature. Due to the matching of on-chip components ramp linearity is maintained to within 2%; relatively little variation in performance from integrated circuit to integrated circuit when using a given set of external components. This is beneficial in avoiding the need for individual adjustment once a design has been finalised.

THE VOLTAGE REFERENCE

The temperature coefficient of V_{REF} is typically ±50 ppm/°C, (80 ppm/°C max.). The output current capability is 1 mA. If increased current capability is required a resistor may be connected between pins 3 and 8. The maximum sink current of V_{REF} is 10 mA which limits R_2 to a minimum value of 270 ohms; the temperature coefficient is independent of the current.

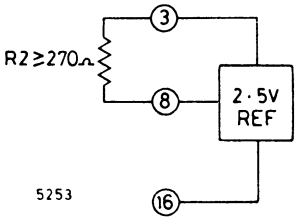


Fig. 6 Extending the Current Capability of V_{REF}

CONTROL AMPLIFIER

These circuits are general purpose, wideband, differential input voltage amplifiers. The frequency response curves of Fig. 7 show the uncompensated amplifier with poles at approximately 240 kHz, 7 MHz, 20 MHz and a unity gain crossover at 45 MHz. The amplifier is compensated by connecting a 0.02 μF capacitor from the output to pin 16, the signal earth point. The compensated curve has a single pole at approximately 10 kHz and a unity gain crossover at 10 MHz.

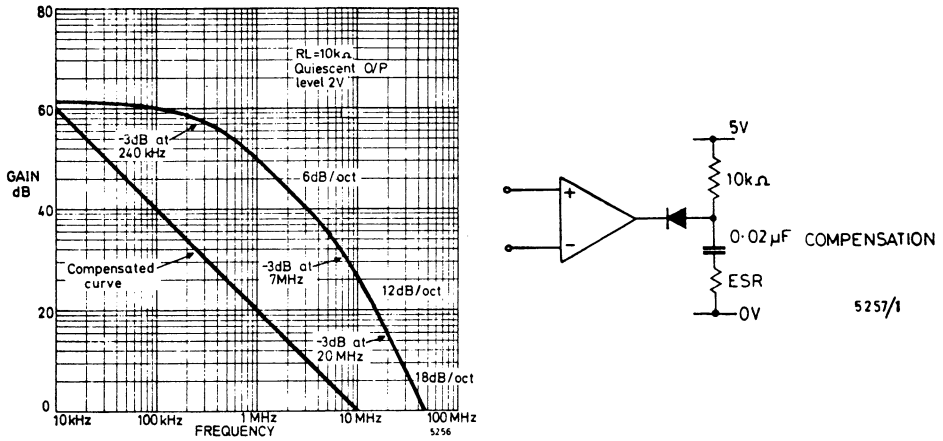


Fig. 7 Amplifier Open Loop Gain as a Function of Frequency

With compensation, both amplifiers are stable in either the inverting of non-inverting mode. Fig. 8 shows typical biasing circuits for achieving voltage control of positive and negative output voltages. Regardless of the connections, however, input common mode limits must be observed or output signal inversion may result.

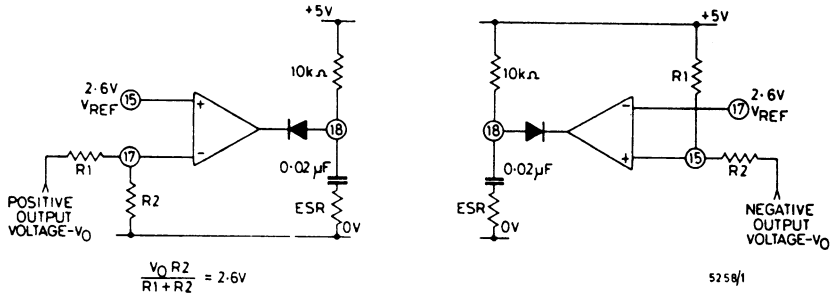


Fig. 8 Voltage Control Biasing Networks

LOOP STABILISATION

Most output filter designs will introduce one or more poles at a relatively low frequency. Typically 300 Hz to 2 kHz. One approach to the loop stability problem is to connect a series RC network which introduces a zero to cancel one of the output filter poles. In practice it has been found that better overall system performance is achieved using the technique outlined in Fig. 9.

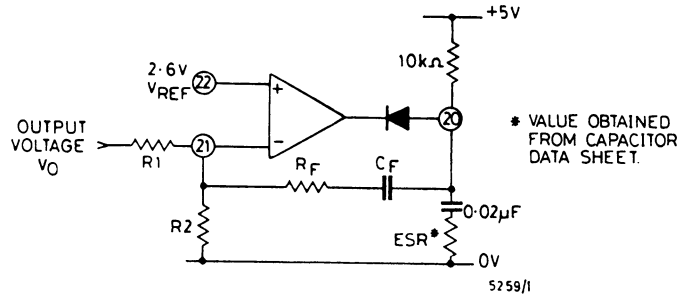


Fig. 9 Closed Loop Stabilisation

A good starting point is to select the time constant of R_F C_F to be approximately equal to the series resonant frequency of the output filter.

CURRENT LIMITING

The output current is controlled indirectly by regulating the voltage drop V_S across a series sensing resistor R_S, the voltage to be regulated being the potential drop caused by the load current flowing through R_S. Whatever V_S drop is chosen its magnitude represents the total amount of load current. To minimise power dissipation in R_S, the size of the sampling drop V_S should be made as small as possible. However the problem of regulating a very small voltage drop should be taken into account and for most practical designs $V_S = 0.05$ volts is a good choice. The maximum power dissipated in R_S is then only 1% ot fhe output power.

ZN1066E/J

To obtain a near perfect constant current characteristic, as distinct from simple current limiting, it is necessary to feedback a small signal proportional to the output voltage of the regulator. Fig. 10 shows the circuit developed for an off line switched mode power supply designed to deliver 0 to 20 amps at 5V d.c.

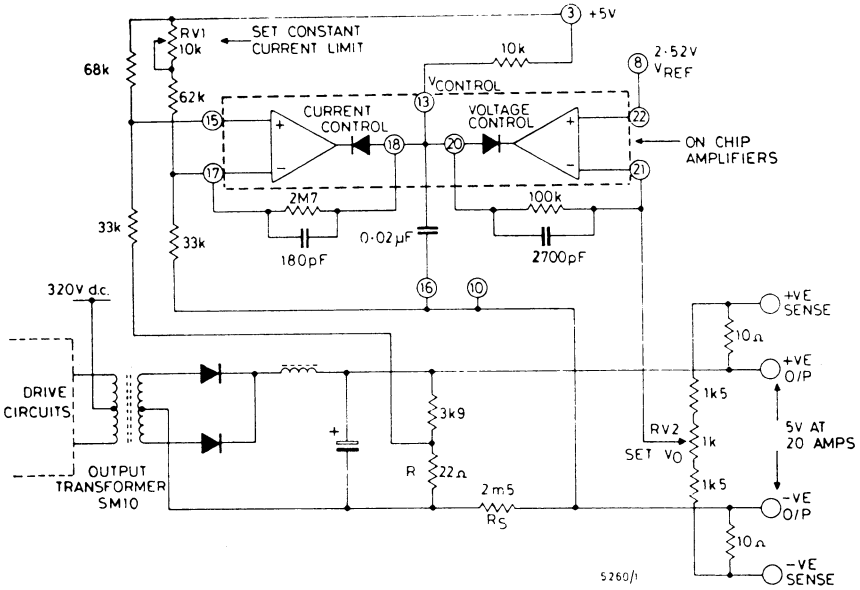


Fig. 10 Current and Voltage Control Circuit

The foldback current limiting characteristic shown in Fig. 11 is obtained by increasing the value of R in Fig 10 i.e. the amount of feedback proportional to output voltage. In this way the short circuit current can be reduced to essentially zero.

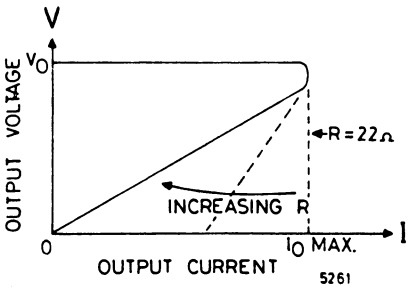


Fig. 11 Output Current Cut-Off

AUTOMATIC CROSSOVER

An automatic crossover power supply is unique in that it cannot be overloaded; it operates with full control into any load resistance from infinity to zero ohms. From infinity to the crossover resistance $= V_o/I_o$ max. it behaves as a voltage regulator holding its output voltage constant as the current increases. From the crossover resistance down to zero ohms the power supply behaves as a current regulator, the terminal current being held constant as the output voltage decreases.

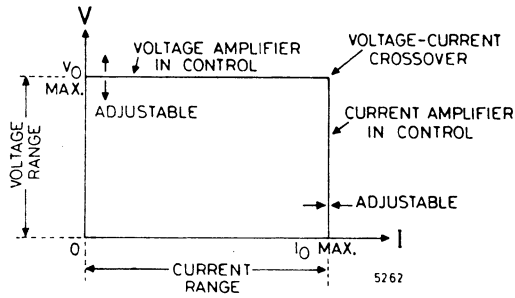


Fig. 12 Automatic Crossover, V/I Characteristic

Since the voltage and current controls are each independently adjustable throughout the full voltage and current output range, the crossover point, which is the intersection of the two control settings, can be located anywhere in the volt-ampere range of the power supply. The curve in Fig. 12 illustrates this type of operation and Fig. 10 shows the circuit details, I_o max. being set by varying RV1 and V_O, by varying RV2.

The amplifier may also be used to sense primary current and produce a constant current characteristic or shorten an output pulse should transformer saturation occur. See Fig. 13.

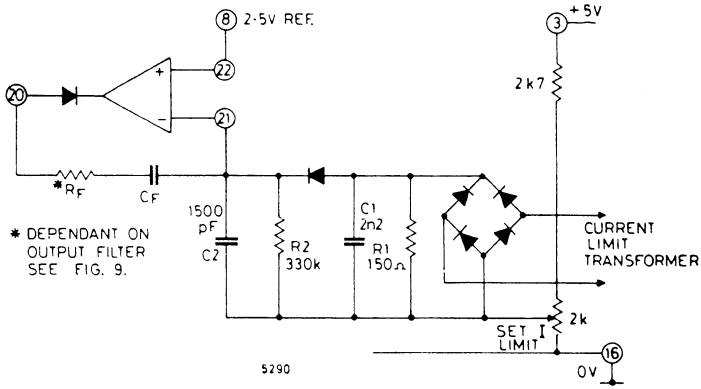


Fig. 13 Constant Current Limit – Sensing Primary Current

CYCLE-BY-CYCLE CURRENT LIMIT

If the design calls for protection against overcurrent in the external switching transistors then the circuit shown in Fig. 14 may be used.

When the peak collector current in either output transistor exceeds a preset level, (set by RV1), the monostable comprising TR1 and TR2 trips. Activating the trip causes a direct cut-off to be applied to the gates which control the output stage and rapidly removes the drive to each of the output transistors and at the same time these reset the soft start circuit. Many power switching transistors have wafer thermal time constants in the 5 ms region, and a monostable delay time of at least 50 ms is recommended to allow the wafer to cool after an overstress.

This protection mechanism protects the power switching transistors even from the effects of a saturating power transformer.

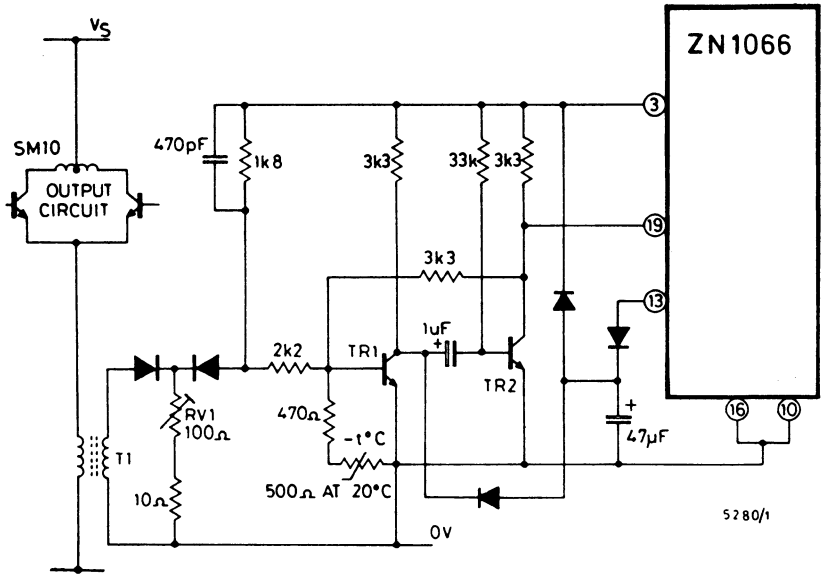


Fig. 14 Current Limit – Primary Side

OPTO-ISOLATION

When the ZN1066 is used to directly drive the output switching elements it is possible using the circuit outlined in Fig. 15 to provide wideband input/output isolation. The two on-chip amplifiers combine with two opto-isolators to produce a tracking voltage source.

Temperature effects are largely confined to the opto-isolators. If these have matched characteristics and are iso-thermally mounted, the circuit has for most applications an acceptably low temperature coefficient. A dual opto-isolator package is a possible alternative.

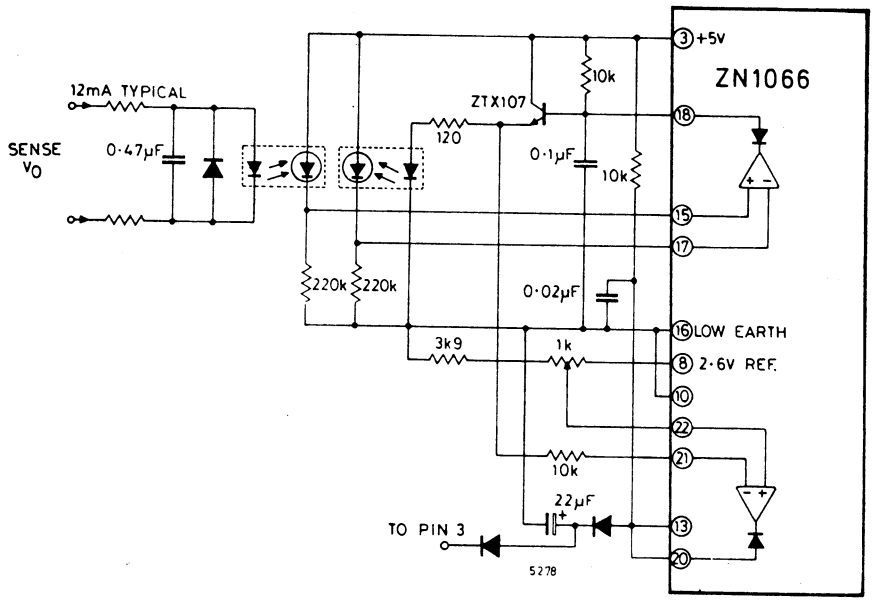


Fig. 15 Opto-Isolator Control Circuit

SOFT START

In most switched mode power supplies a soft start feature is required to prevent output voltage overshoots and magnetising current imbalances in the power transformer primary. This feature forces the duty cycle of the switching transistors to increase gradually from zero to their normal operating point during system power up or after an inhibit. This function is easily implemented with the ZN1066 and one method is shown in Fig. 16.

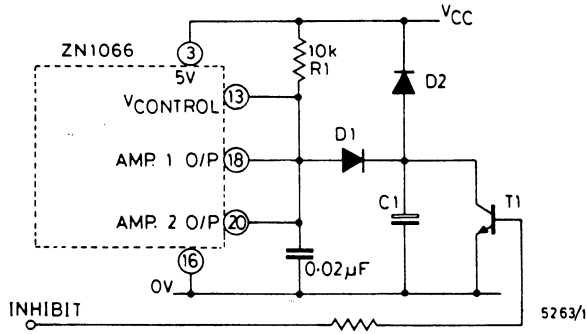


Fig. 16 Soft Start and Inhibit

After an inhibit command or during power up, the voltage at Pin 13 rises exponentially from zero volts toward V_{CC} with a time constant of R1 C1, thus permitting a gradual increase in duty cycle. Diode D1 provides an OR function at $V_{control}$ pin 13, while T1 serves to reset the soft start timing capacitor, C1, when an inhibit command is received thereby resetting the soft start function. D2 allows C1 to reset when the power is turned off.

CROSS COUPLED INHIBITS

One method adopted to try and prevent simultaneous conduction in the output switching transistors is to limit the maximum pulse width of the drive circuits so that a known off state time is defined. (Dead time).

Unfortunately the storage time varies between any two power switching devices and the variation in storage time with temperature, loading and time is unpredictable. With modern switching devices a spread of 0.3 to 10 μsecs is not uncommon. To be 100% safe the dead time should be in excess of 10 μsec and when one considers that at an output frequency of 20 kHz the 100% pulse width is only 25 μsec it is not difficult to see that dead time setting severely limits the range of control. The output transformer must therefore have a higher turns ratio to give full output at minimum input voltages, leading to shorter higher current input pulses and loss of efficiency.

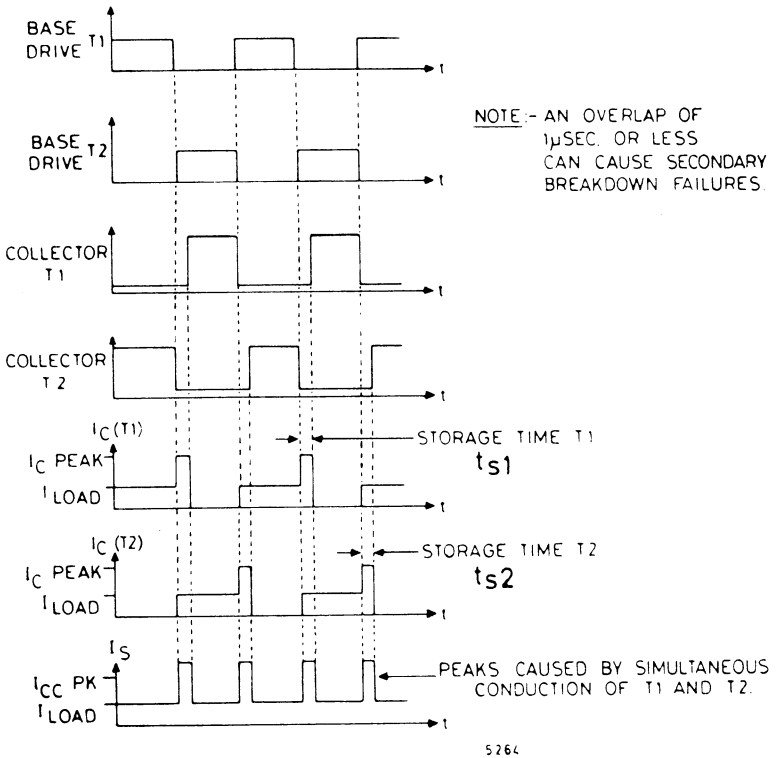


Fig. 17 Effects of Cross Current Conduction (Overlap)

A foolproof solution to this problem is possible using the cross coupled inhibit feature of the ZN1066. The action of this circuit is shown in Fig. 18.

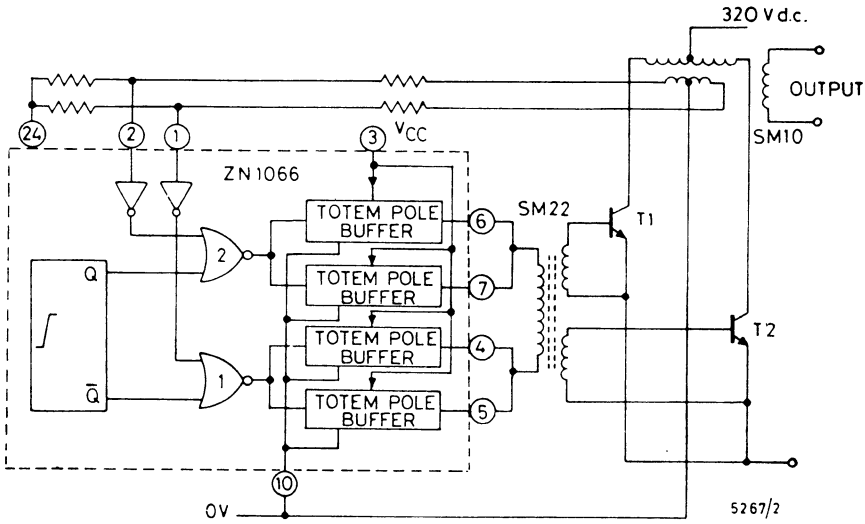


Fig. 18 Automatic Overlap Control

Two fast acting inhibits, pins 1 and 2 are connected to the inputs of the pulse steering gates. A logic '0' at these inputs corresponds with zero drive output. These inhibit pins are effectively cross coupled to the power switching transistor collectors, either directly or via a separate winding specifically wound for this purpose. The storage time delay is sensed and feedback prevents one transistor from turning on until the other is turned off.

If a 100% pulse width drive is now applied to the bases of T1 and T2, cross current conduction is prevented since one transistor base drive is inhibited until the collector voltage of the other transistor has risen to the supply voltage, i.e. the transistor has turned off, irrespective of storage time. The cross coupled inhibit feature therefore automatically compensates for variations in storage time and allows up to 100% output pulse widths without overlap.

When both output transistors are in the OFF state, i.e. pulse widths less than maximum, then the Logic 1 required for normal operation is conveniently obtained by connecting a suitable valve resistor from each inhibit pin to pin 24. See Figs. 18, 34 and 35. Alternatively the centre tap on the feedback winding can be connected to pin 3.

Dead time settings (end stop) is therefore no longer required and the conflict between safe minimum off time and maximum control range no longer exists.

INRUSH CURRENT LIMITING

Since many switched mode power supplies are operated directly off the rectified 240V a.c. line with capacitor input filters, some means of preventing rectifier failure due to inrush current is usually necessary. One method which can be used is shown in Fig. 19

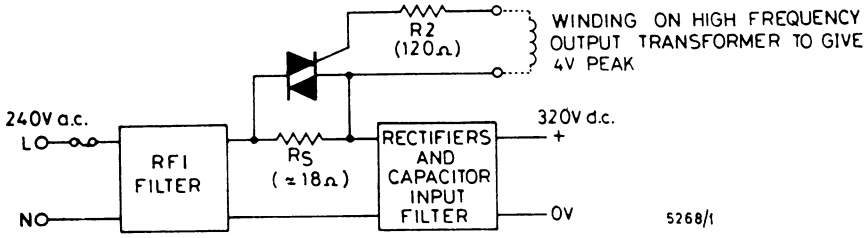


Fig. 19 Inrush Current Limiting

In this circuit a series resistor R_s, is used to provide inrush surge current limiting. After the input filter capacitor has charged and converter action starts, a separate winding on the high frequency transformer applies drive to the gate of the input triac via R2 so that R_s is bypassed and its dissipation reduced to near zero.

A major advantage of this system is that the triac is brought into conduction at a time when the input capacitor is nearly fully charged so that the surge current is low.

OUTPUT CIRCUITS

The ZN1066 provides four identical push pull totem pole type outputs each capable of sinking and sourcing 60 mA. The equivalent output circuit is shown in Fig. 20.

Outputs may be paralleled for greater output drive. The totem pole type output is the most flexible and versatile possible.

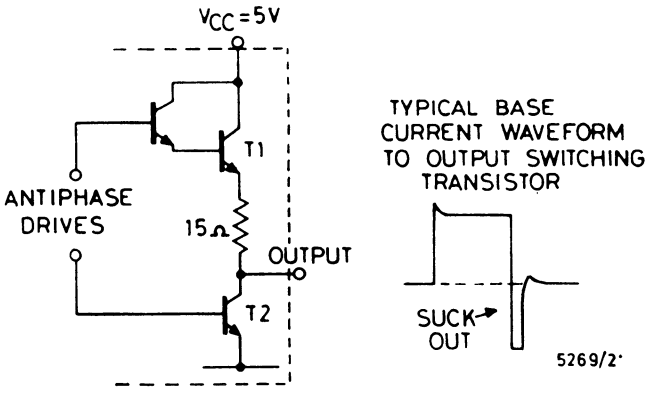


Fig. 20 Output Drive Circuit (1A, 1B, 2A and 2B)

In considering the application of the ZN1066 to switching regulator circuitry, there are a multitude of output configurations possible. The following diagrams do not exhaust the possibilities but serve mainly to illustrate some of the more common types of connection.

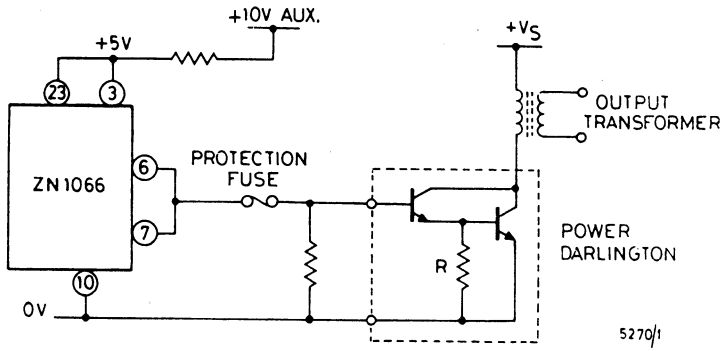


Fig. 21 Direct Drive for Single Ended or Flyback Converters

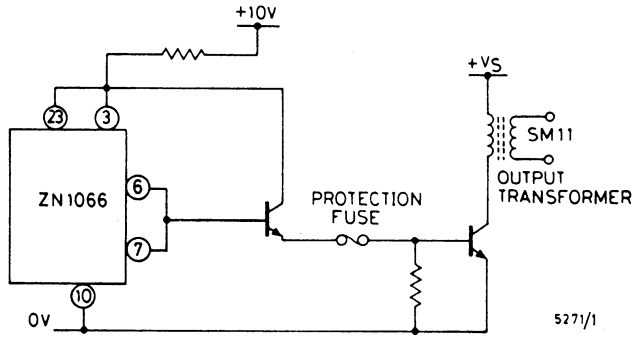
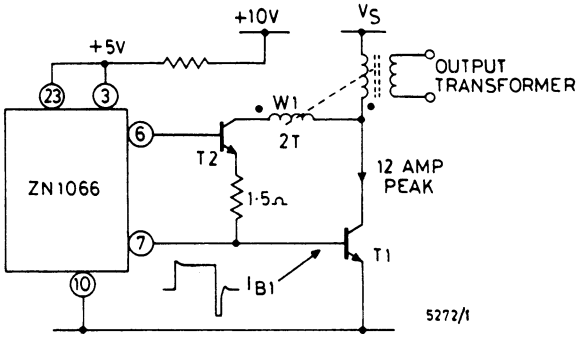


Fig. 22 Alternative Direct Drive for Single Ended or Flyback Converters



Winding W1 provides approximately 3V to the collector of T2 thus ensuring that T1 can fully saturate.

Fig. 23 Direct Drive for High Power Single Ended Converters

The main advantage of this connection is that the current suck-out capability is maintained and T1 can be rapidly turned off.

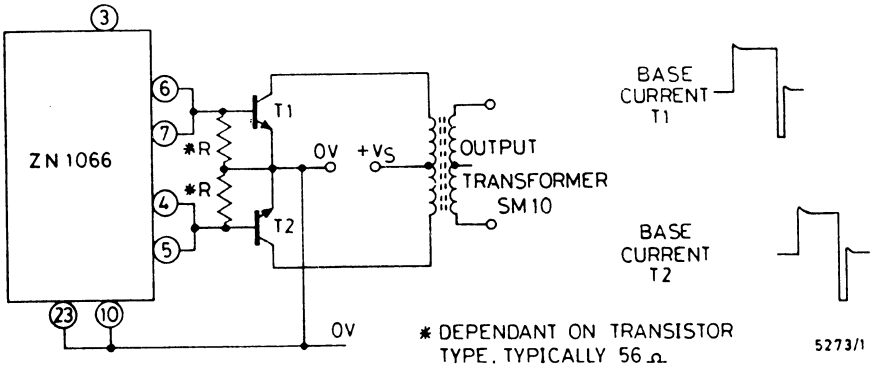


Fig. 24 Typical Direct Coupled Push-Pull Circuit

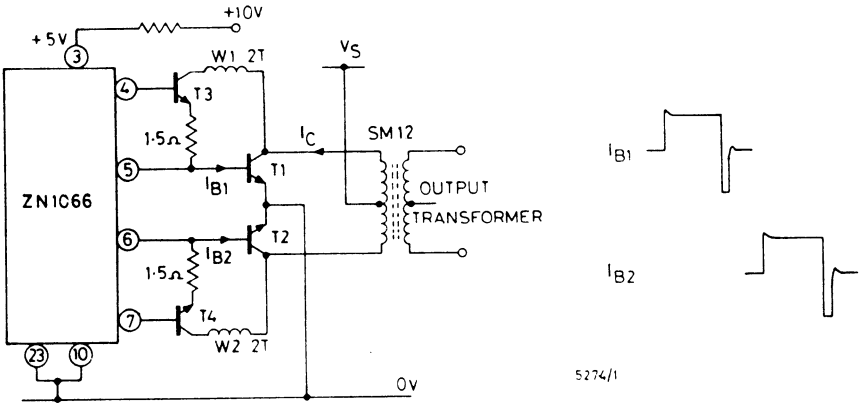


Fig. 25 High Power Direct Coupled Push-Pull Circuit

The windings W1 and W2 are connected in antiphase to the main primary winding. These windings provide an auxiliary supply of about 2.5 volts for the transistor T3 and T4 thus ensuring saturation of the darlington pair. Peak collector currents in T1 and T2 in excess of 12 amps are possible using this method of drive.

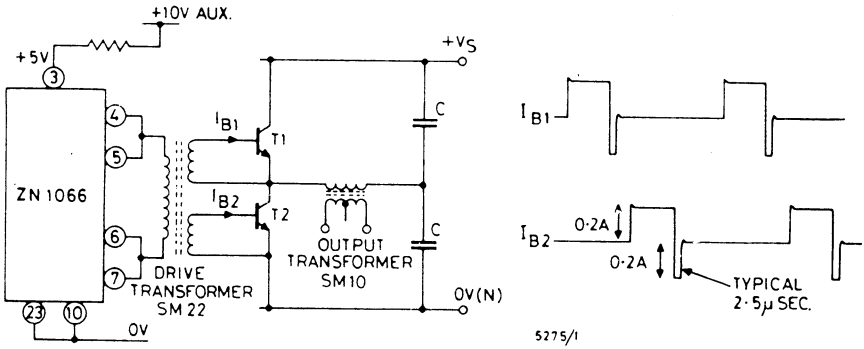


Fig. 26 Transformer Coupled Half Bridge Push-Pull Circuit

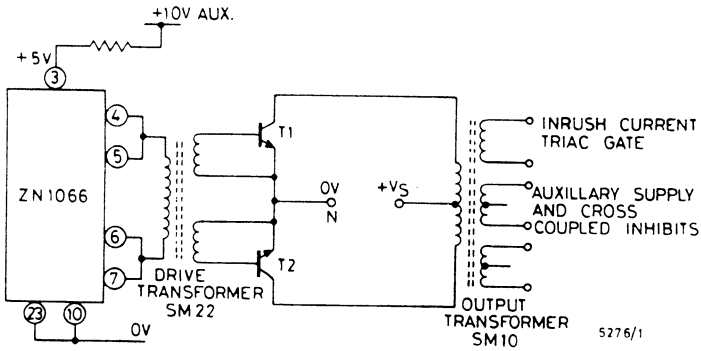


Fig. 27 Typical Transformer Coupled Push-Pull Circuit

The advantage of this type of circuit is that it retains the current suck-out capability of the ZN1066 and powers up to 200W are possible. For higher power applications it is necessary to buffer the output from the ZN1066. Fig. 28 outlines a common method of interfacing.

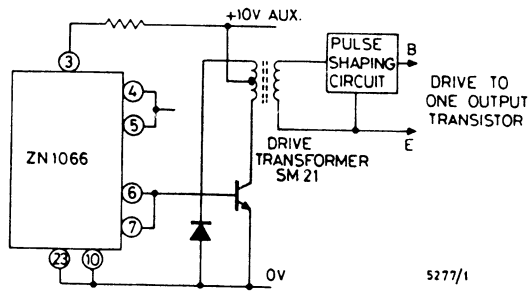


Fig. 28 Typical High Power High Input Voltage Interface Circuit

5V SHUNT REGULATOR

The total supply current to the ZN1066 is divided between three main functional areas :

(a) Internal Control Circuitry
(b) Average output load currents
(c) 5V shunt regulator.

Since the control circuits are fed from the 5V stabilised supply rail, the current drawn is independent of external conditions over the operating range of the shunt regulator. Fig. 30 shows a typical plot of the stabilised supply versus input in the absence of output loads. The supply current at the knee of the characteristic was approximately 35 to 40 mA for the samples tested.

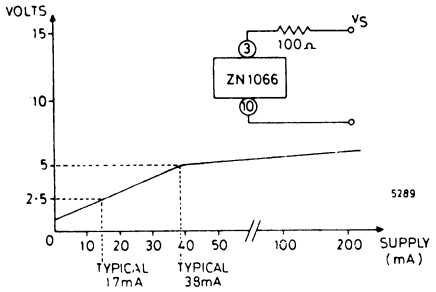


Fig. 29 Shunt Regulator Characteristics

In order to keep the total package dissipation to a minimum in a particular application the supply current should be tailored to suit the output drive requirements. Current in excess of this will be carried by the shunt regulator.

Assuming an operating duty cycle of nominally 50% a suitable current would be :

Peak output current +40 mA

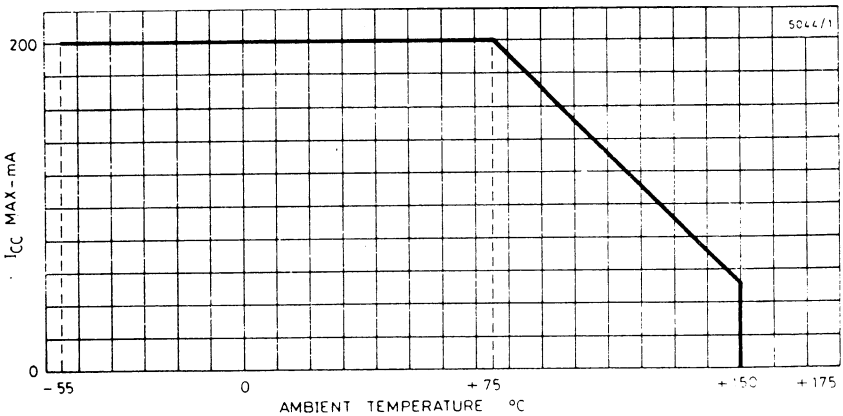


Fig. 30 DERATING CURVE (I_{CC} max. V_s ambient temperature)

AUXILIARY SUPPLY

In some applications it may be advantageous to derive the initial power for the ZN1066 from the main supply, V_s via a start circuit. One method of achieving this is illustrated in Fig. 31.

Initially, current for the ZN1066 is provided via R_s and T1 ;T2 is not conducting. When the output from the additional winding on the high frequency transformer is large enough the current required by the ZN1066 is provided via the 18Ω resistor. When steady-state conditions have been established transistor T2 bottoms and shuts off T1. The operation of the start circuit is inhibited, and there is little further dissipation in it.

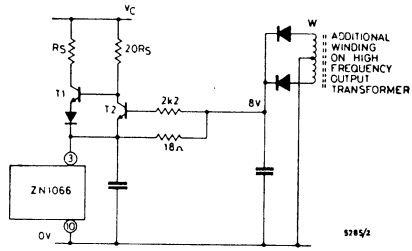


Fig. 31 Start Up Circuit

OUTPUT PULSE WIDTH SETTING

The output pulse width is infinitely variable from 0 to 50%, mode control at 0V, or 0 to 100% mode control at +5V.

The maximum pulse width can be preset to any desired value by simply connecting a resistor of suitable value between pins 13 and 16 as indicated in Fig. 32.

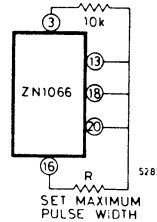
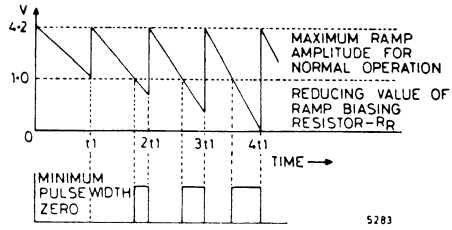


Fig. 32 Presetting Maximum Pulse Width

The minimum pulse can also be preset to any desired value by adjusting the value of the ramp biasing resistor R_R connected to pin 11. The function of this is illustrated in Fig. 30.



Minimum pulse width increasing with reducing value of ramp biasing resistor R_R.

Fig. 33 Presetting Minimum Pulse Width

ZN1066E/J

TYPICAL CIRCUITS

Fig. 34 illustrates a 120VA direct coupled push-pull power supply. Input/output isolation is achieved by means of the voltage tracking opto-isolator circuit previously described in Fig. 15. The design also incorporates the essential soft start circuit to prevent damage to the power transistors on turn-on and current limit is by sensing the transistor collector currents as previously described in Fig. 14. The transistors are also protected against simultaneous conduction by means of the cross coupled inhibits, Pin 1 and Pin 2.

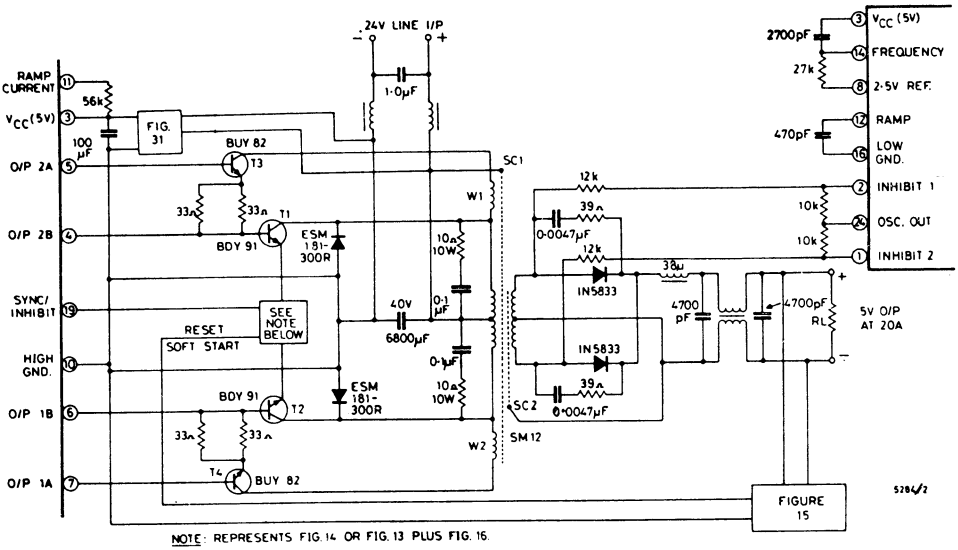


Fig. 34 120VA DC/DC Converter

Fig. 35 illustrates a 120VA push-pull switched mode power supply. The design incorporates soft start, foldback current limiting protection against cross current conduction and a controlled start-up.

This circuit is easily modified to include current limit on the primary side by using the cycle-by-cycle current limit described in Fig. 14. Alternatively if output current sensing is not required the on-chip current control amplifier can be used to provide a constant current characteristic based on sensing the switching transistor collector currents. One method of achieving this is shown in Fig. 13.

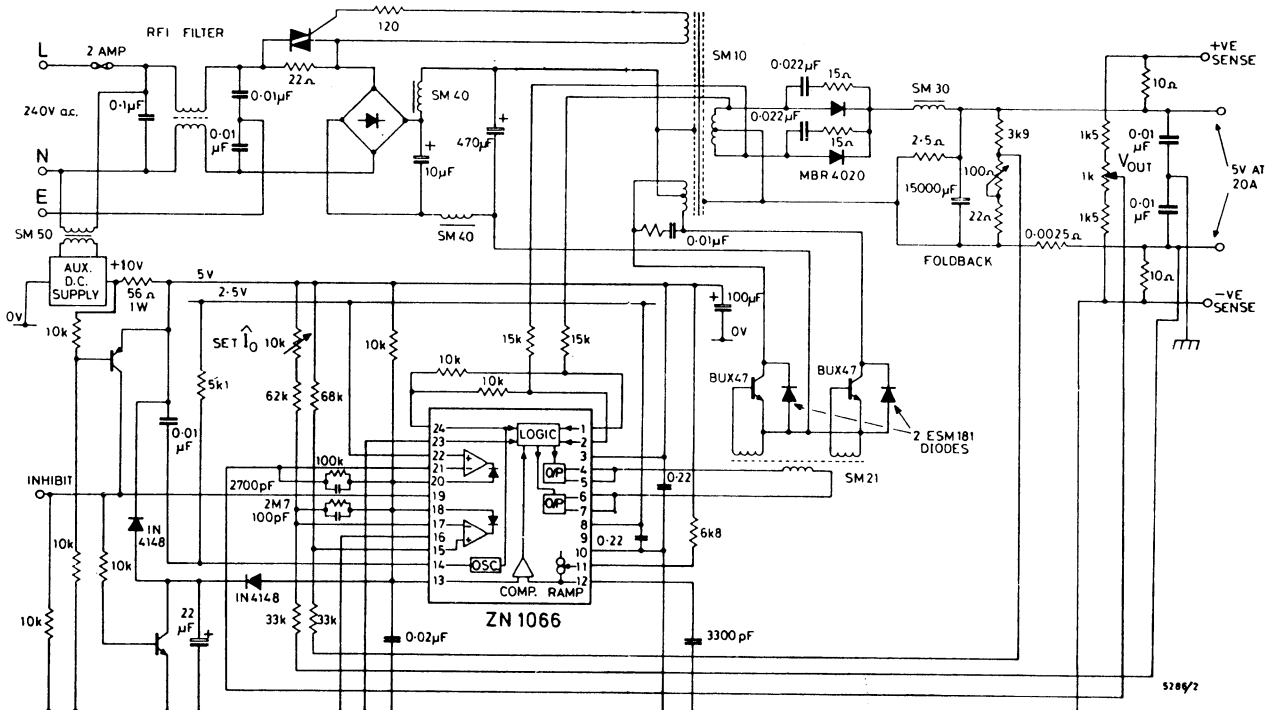


Fig. 35 120 VA Off Line SMPSU

ZNA134

FERRANTI semiconductors

CCIR/EIA TV Synchronising Pulse Generator

FEATURES

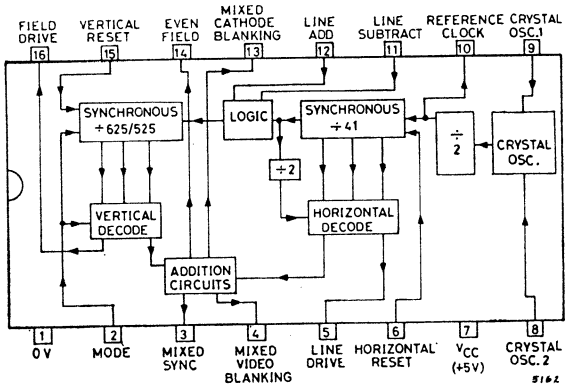
- 625 and 525 line standards.
- CCIR and EIA standard outputs.
- Single 5 volt supply, fully TTL compatible.
- Easy synchronising between generators.
- Direct reset to vertical and horizontal counters.
- Facility for adding and subtracting lines.
- Automatic interlacing.
- On chip oscillator (requiring external crystal).
- Can be driven with an external oscillator.
- Field reference output.
- Extended Temperature Range available ZNA134 H RED

GENERAL DESCRIPTION

The ZNA134 integrated circuit utilises a 2.5 MHz* crystal to generate all the horizontal, vertical, mixed blanking and synchronising pulses necessary for raster generation in 625 or 525 line commercial, industrial or military television systems. The synchronous dividers and decoding logic employed within the unit ensure perfect interlace, together with spike-free output waveforms having precisely defined relative positions and pulse widths. The device is contained in a 16 pin D.I.L. and can be selected to operate over the military temperature range.

*Dependent on line system used, series resonant.

SYSTEM DIAGRAM



CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Maximum value
Supply Voltage	7 volts
Input Voltage	5 volts
Operating Temperature Range	0°C to +70°C*
Storage Temperature Range	−65°C to +150°C

OPERATING CHARACTERISTICS

(over recommended temperature range)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		4.75	5.0	5.25	Volts
Supply Current	I_S		–	100	–	mA
High-level Input Voltage	V_{IH}		2.4	–	–	Volts
Low-level Input Voltage	V_{IL}		–	–	0.8	Volts
High-level Input Current	I_{IH}	V_{CC} = 5V, V_I = 2.4V (See Note 1)	–	–	40	μA
Low-level Input Current	I_{IL}	V_{CC} = 5V, V_I = 0 V. (See Note 1)	–40	–	–	μA
High-level Output Voltage	V_{OH}	V_{CC} = 5V, $I_{source} \leqslant 80\mu A$ (See Note 2)	2.4	–	–	Volts
Low-level Output Voltage	V_{OL}	V_{CC} = 5V, $I_{sink} \leqslant$ 3.2 mA (See Note 2)	–	–	0.5	Volts
Clock frequency	f_{clock}	625 lines, Mode = '1' 525 lines, Mode = '0'	– –	2.56250 2.5830	– –	MHz MHz
External Oscillator Pulse Width	t_w	-ve going pulse, 625/525 lines	150	200	250	ns

Note 1

Input conditions only apply to mode, horizontal reset, vertical reset, line subtract and line add. For input conditions of oscillator inputs C.0.1, C.0.2, see applications section.

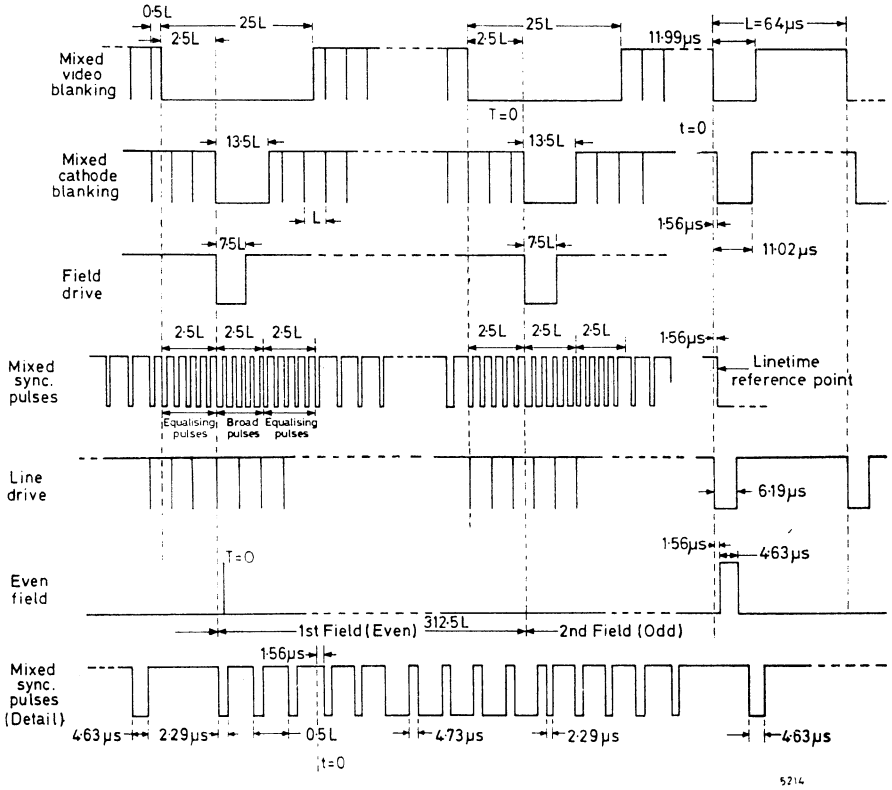
Note 2

All outputs – mixed sync, mixed video blanking, line drive, reference clock, mixed cathode blanking, even field and field drive have internal 10kΩ pull-up resistors. Edge speeds and sourcing capability can be increased, if required, by the addition of external pull-up resistors. These should have a minimum value of 2kΩ.

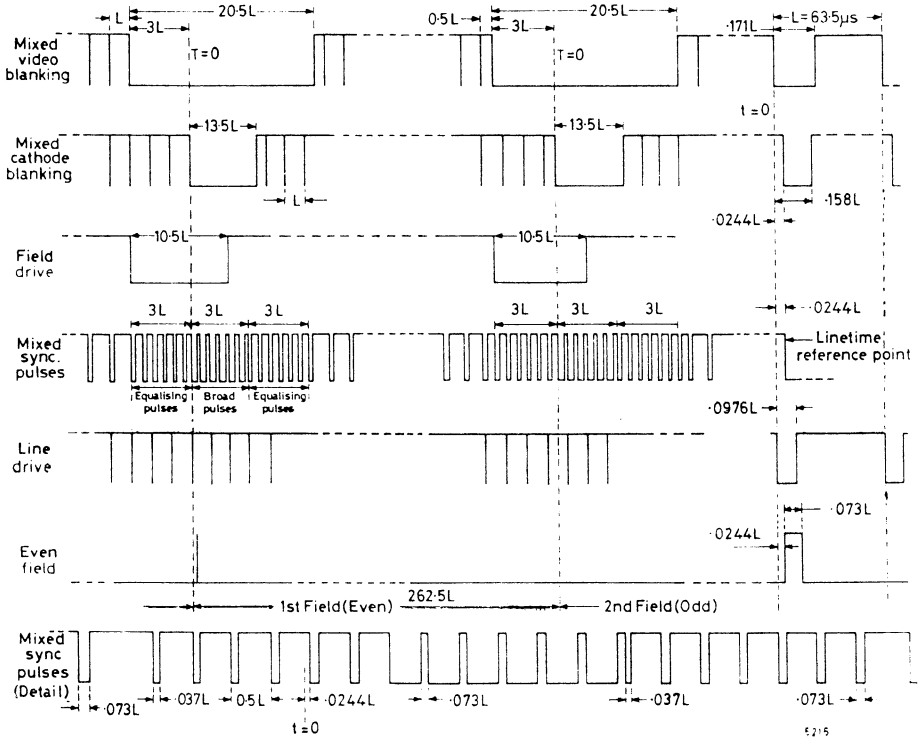
ZNA134

OUTPUT WAVEFORMS

(a) 625 line CCIR standard output (Mode = 1).
Crystal frequency = 2.5625 MHz.
Line frequency = 15.625 kHz, Field frequency = 50 Hz.
Line period = 64 μs, Field period = 20 ms.



(b) 525 line EIA standard output (Mode = 0).
Crystal frequency = 2.5830 MHz
Line frequency = 15.750 kHz, Field frequency = 60 Hz
Line period = 63.5 μs, Field period = 16.66 ms.



APPLICATIONS INFORMATION

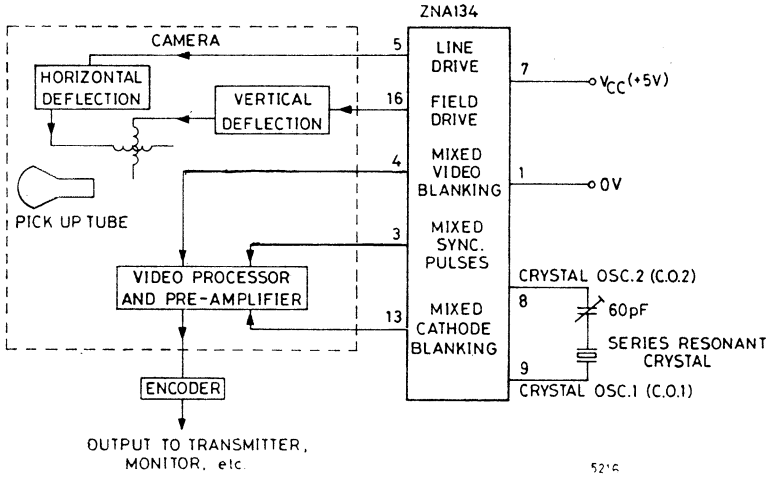


Fig. 1. Application in a TV system

The sync. pulse generator can be driven from an external oscillator if required. C.O.1 must then be connected via a 10kΩ resistor to V_{CC}. The external oscillator can then drive directly into C.O.2 input as shown in Fig. 2.

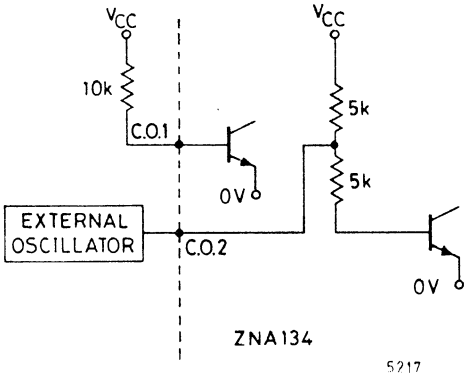


Fig. 2

Mode input (pin 2) can be connected directly to V_{CC} or 0V for 625 or 525 line operation respectively Any of the inputs: vertical reset, horizontal reset, line add, line subtract, not being used should be connected to 0V.

SIMPLE METHOD OF SYNCHRONISATION USING VERTICAL AND HORIZONTAL RESET

Line synchronisation (Fig. 3) is achieved by using a narrow positive going pulse derived from the negative going edge of the Line Drive output of the first generator to drive the Horizontal Reset inputs of the other generators. This monostable pulse, which should have a width of 200 ns ± 40 ns, resets the generators to the start of a line (t = 0). This results in the Line Drive waveforms of the driven generators being one reference clock period (≃800 ns) delayed from the first generator. The C.O.2 pins of the generators must be connected together.

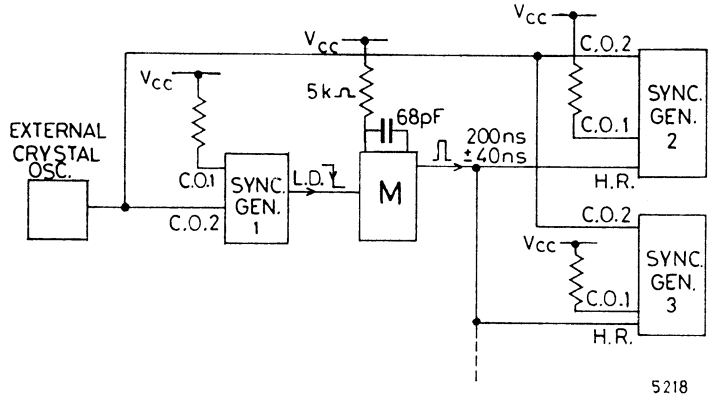


Fig. 3 Line Synchronisation using Horizontal Reset

Field Synchronisation (Fig. 4) is achieved by driving the Vertical Reset inputs of the driven generators directly from the Even Field output of the first generator (the Line drive outputs should already be in phase). This resets the generators to the start of the first field (T = 0, start of broad pulses.)

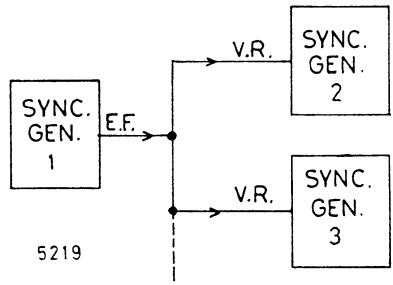


Fig. 4 Field Synchronisation using Vertical Reset

With this method of synchronisation, line sync and field sync are lost at the monitor for a brief period due to a sudden change in the Mixed Sync waveform. Hence it is only suitable for CCTV systems where momentary loss of picture is not critical or where the generators are to be synchronised automatically at power switch on.

SYNCHRONISATION USING THE LINE ADD/SUBTRACT FACILITY

This is suitable where generator lock must be achieved gradually, i.e. without loss of picture at the receiver, as in studio camera systems.
Line Synchronisation can be achieved smoothly by the use of a phase locked loop technique rather than the direct Horizontal Reset technique (Fig. 5).

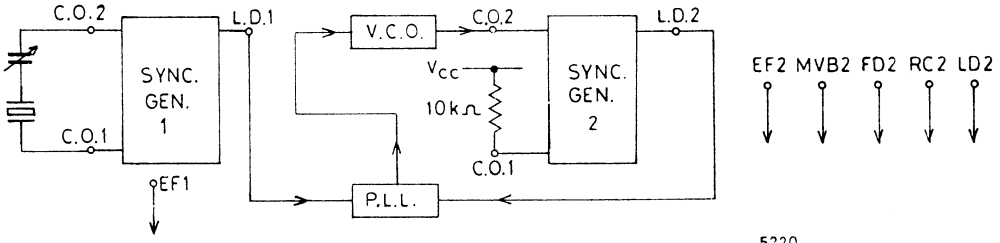


Fig. 5 Line Lock Circuitry

Field Synchronisation (Fig. 6). The generator waveforms are brought into synchronisation by adding or subtracting one line per frame to the second generator until the waveforms are exactly in phase. This is achieved by adding or inhibiting pulses at the start of the first full line after field blanking, thus preventing any changes to the mixed sync. waveform during the broad and equalising pulse periods. Lines are 'added' by clocking the vertical counter faster than the normal half line rate. Setting Line Add high for a period equal to 4 Reference Clock pulses, increments the vertical counter by one line thus effectively reducing the field period by one line.
Lines are 'subtracted' by inhibiting the clock pulses to the vertical counter. Setting Line Subtract high for a period of one line leaves the state of the vertical counter unchanged for one line thus effectively increasing the field period by one line.
Hence the add or subtract periods are generated by counting Reference Clock or Line Drive pulses respectively with a 3 bit counter.
Lines are added or subtracted until the generators are in phase. The two Even Field outputs together generate a pulse which inhibits the add/subtract circuitry when an in-phase condition occurs.

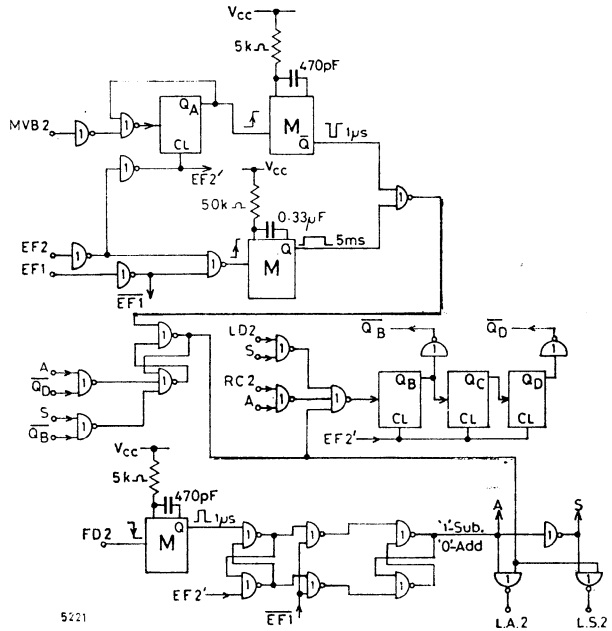


Fig. 6 Field Lock Circuitry

Lines are added to the second generator if EF2 is less than one field period delayed from EF1, and subtracted if EF2 is greater than one field period delayed from EF1 to reduce synchronisation time The add/subtract circuitry can be built using nine TTL packages :-

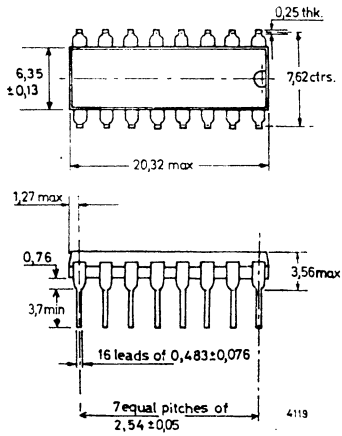
4 off ZN7402
1 off ZN7427
1 off ZN7404
1 off ZN74123
1 off ZN74121
1 off ZN7493

The circuit in Fig. 6 adds or subtracts one line per frame but this could be extended to two or more lines per frame by adding further bits to the 3 bit counter and decoding the relevant states. Similarly half a line per frame can be added by decoding 'QC' instead of 'QB'.

The circuit operates in 625 or 525 line mode without any changes to the component values.

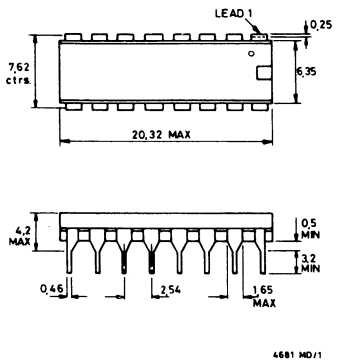
PACKAGE OUTLINE

ZN134H



16 lead Cerdip Dimensions in millimetres

ZN134E



16 lead moulded DIL

ZNA234E

FERRANTI semiconductors

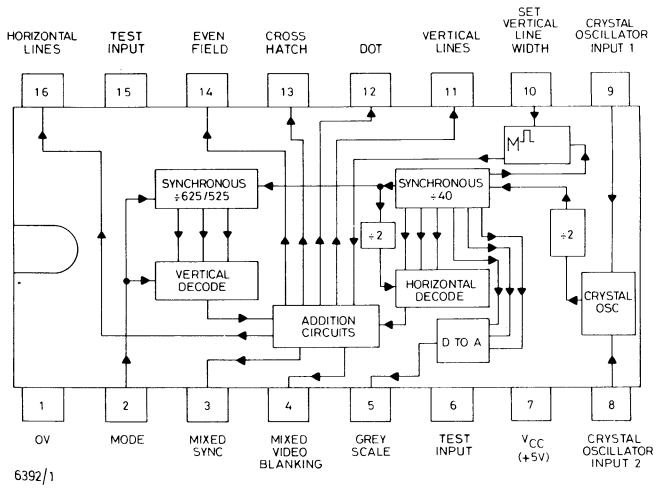
TV Pattern Generator

FEATURES

- Single 5V supply
- 625 or 525 line operation
- Sync and Blanking outputs to CCIR or EIA Standard
- Field Reference output
- Separate outputs for:
  - Crosshatch
  - Dot
  - Vertical Lines
  - Horizontal Lines
  - Greyscale
  - Mixed Sync
  - Mixed Video Blanking
- Adjustable vertical line width

DESCRIPTION

The ZNA234E integrated circuit makes available all the waveforms necessary to produce crosshatch, dot and greyscale test patterns on a television screen. All that is required is a 2.50MHz crystal (or external oscillator) and a minimum number of external components for mixing video, sync blanking pulses to give a composite video signal. This can be either injected directly into the video stages of a receiver, or used to drive a UHF modulator/oscillator for connection to the aerial socket. The device is contained in a 16 pin DIL package.



System Diagram

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .. .. 7 volts
Input Voltage .. .. 5 volts
Operating Temperature Range .. .. 0 to +70°C
Storage Temperature Range .. .. −65 to +150°C

OPERATING CHARACTERISTICS (over recommended temperature range)

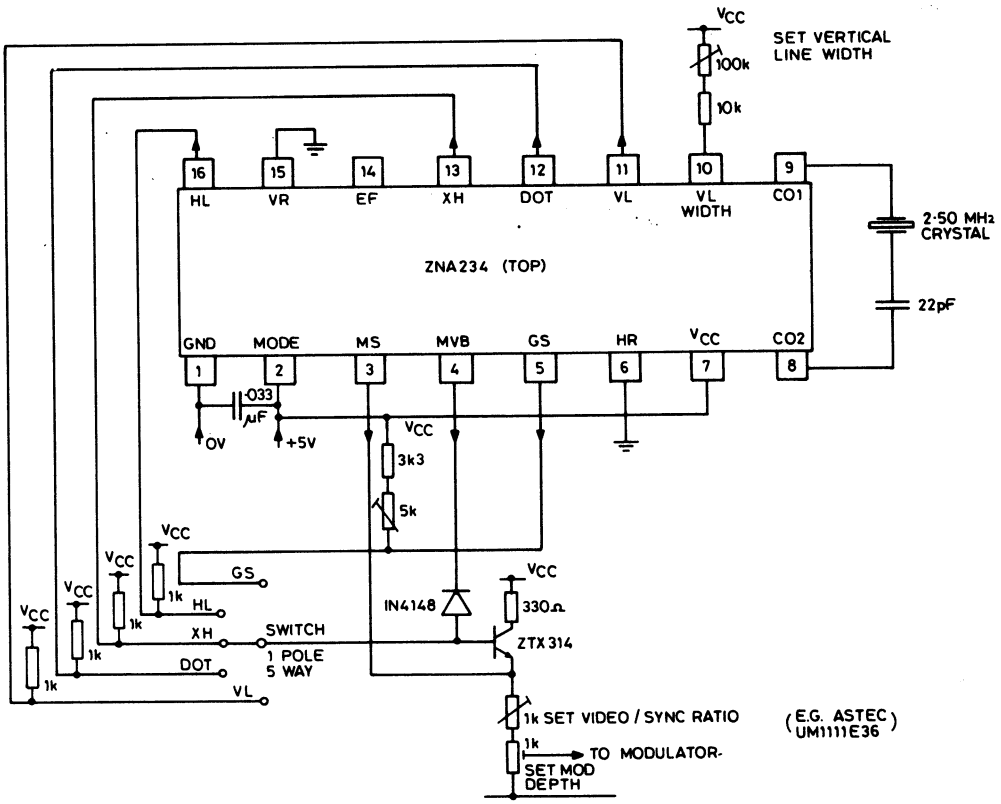
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply voltage	V_{CC}	4.75	5.0	5.25	volts	
Supply current	I_S	–	135	–	mA	
High-level input voltage	V_{IH}	2.4	–	–	volts	
Low-level input voltage	V_{IL}	–	–	0.8	volts	
High-level input current	I_{IH}	–	–	40	μA	$V_{CC}=5V$, $V_I=2.4V$ (See Note 1)
Low-level input current	I_{IL}	−40	–	–	μA	$V_{CC}=5V$, $V_I=0V$ (See Note 1)
High-level output voltage	V_{OH}	2.4	–	–	volts	$V_{CC}=5V$, $I_{Source}\leqslant 250\mu A$ (See Note 2)
Low-level output voltage	V_{OL}	–	–	0.5	volts	$V_{CC}=5V$, $I_{Sink}\leqslant 5.0mA$ (See Note 2)
Clock frequency	f_{clock}	– –	2.500 2.520	– –	MHz MHz	625 lines, Mode='1' 525 lines, Mode='0'
External oscillator pulse width	t_w	150	200	250	ns	−ve going pulse, 625/525 lines

Note 1: Input conditions only apply to mode input. For input conditions of oscillator inputs C01, C02, see applications section.

Note 2: All outputs except greyscale, i.e. mixed sync, mixed video blanking, vertical lines, dots, crosshatch, even field and horizontal lines have internal 3k3 pull-up resistors. Edge speeds and sourcing capability can be increased, if required, by the addition of external pull-up resistors. These should have a minimum value of 1kΩ.

ZNA234E

COMPLETE PATTERN GENERATOR USING THE ZNA234
(for detailed information see applications section)



OUTPUT INFORMATION AND WAVEFORMS

(a) **625 Lines** CCIR Timing (Mode = 1)
Crystal Frequency = 2.50MHz
Line Frequency = 15.625kHz, Line Period = 64μs
Field Frequency = 50Hz, Field Period = 20ms.

Outputs

20 Horizontal Lines; 18 visible, 2 during Field blanking.
20 Vertical Lines; 16 visible, 4 during Line blanking.

Crosshatch squares have approx. 1. 4:1 aspect ratio (0.98" × 0.67" on 20" screen).
For timing diagrams see page 4.

(b) **525 Lines** EIA Timing (Mode = 0)
Crystal Frequency = 2.520MHz
Line Frequency = 15.750kHz, Line Period = 63.5μs
Field Frequency = 60Hz, Field Period = 16.66ms.

Outputs

17 Horizontal Lines; 15 visible, 2 during Field blanking.
20 Vertical Lines; 16 visible, 4 during Line blanking.

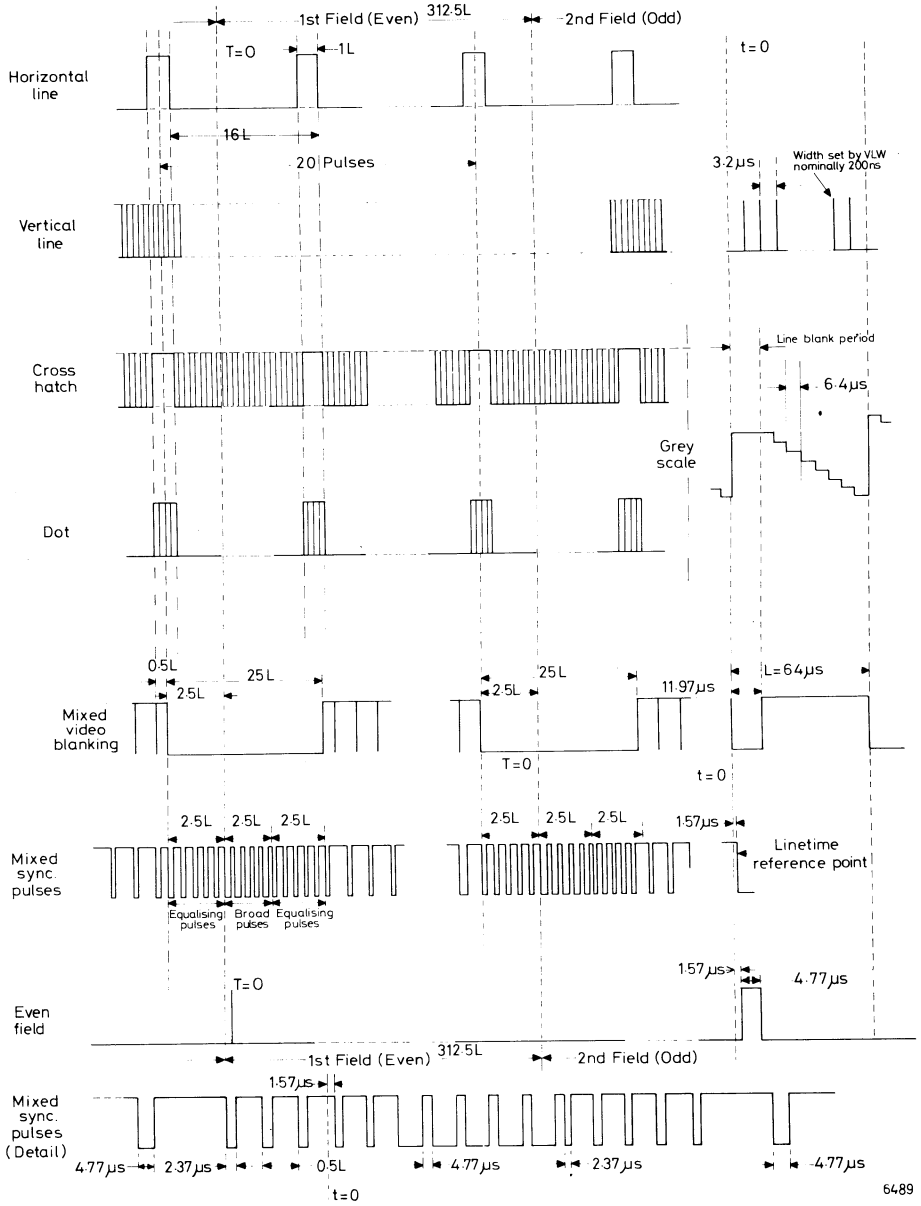
Crosshatch squares have approx. 1. 2:1 aspect ratio (0.97" × 0.79" on 20" screen).
For timing diagrams see page 5.

The horizontal line waveform consists of pulses 1 line wide occuring every 16 lines, producing horizontal lines 2 lines wide (owing to interlacing) on the screen. The vertical line waveform is a continuous series of pulses nominally 300ns wide occuring every 3μs (approximately). As these pulses occur in the same position in every line period the result is a series of vertical lines on the screen.

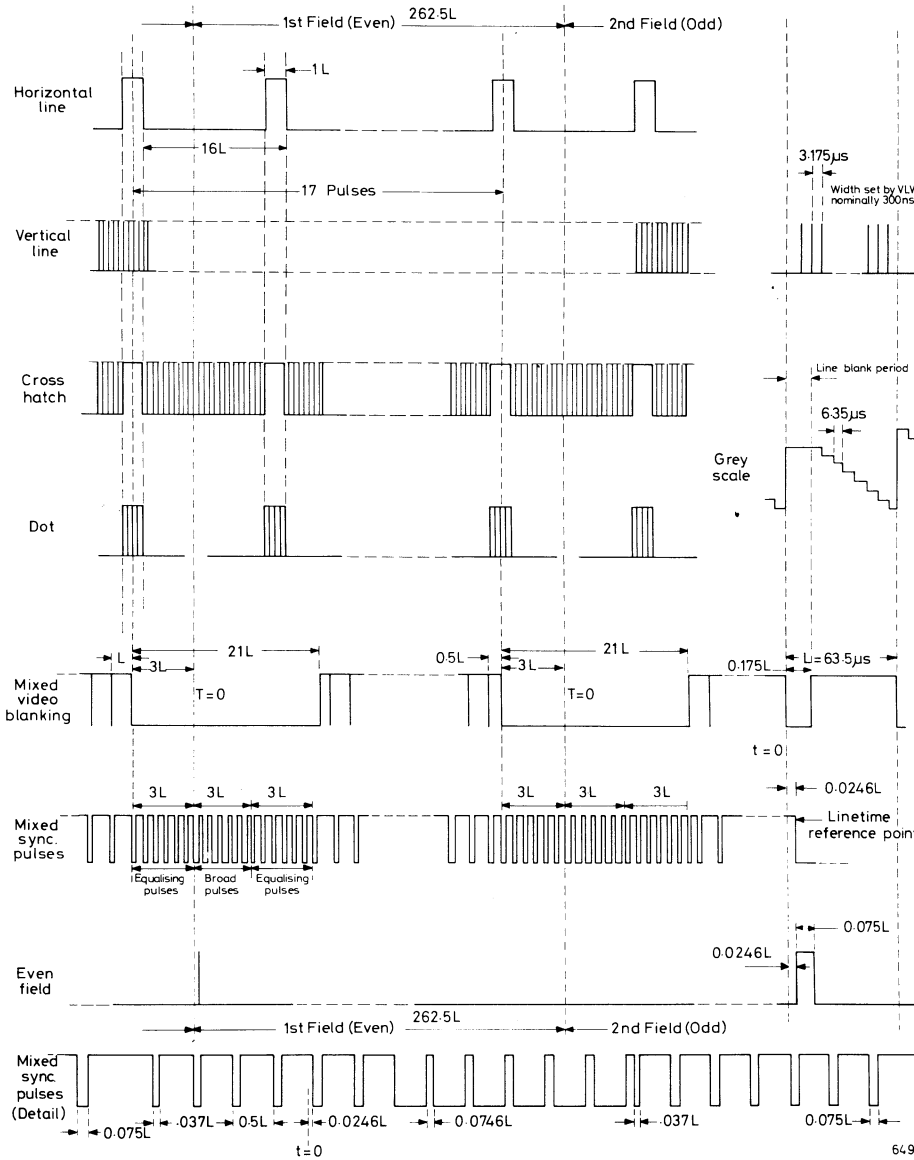
The two waveforms are fed to internal AND and OR gates to produce dot and crosshatch outputs respectively.

ZNA234E

OUTPUT WAVEFORMS - 625 LINES

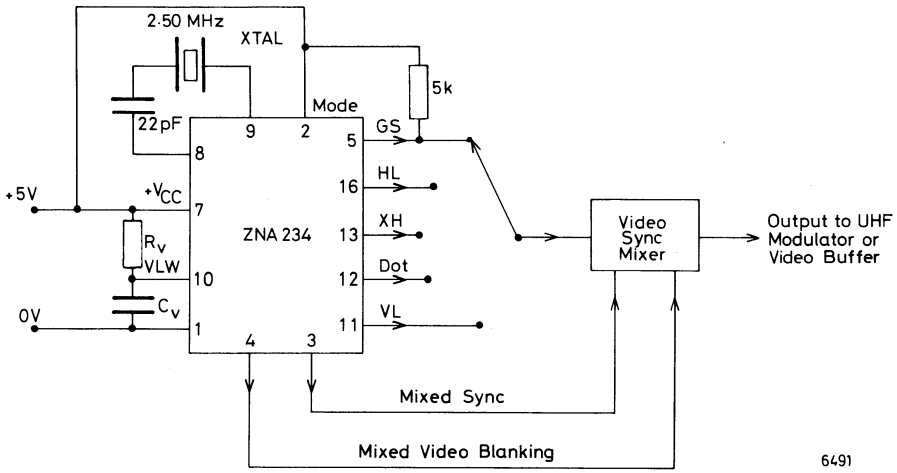


OUTPUT WAVEFORMS - 525 LINES



ZNA234E

APPLICATION INFORMATION



T.V. Pattern Generator using the ZNA234 (625 lines)

NOTES:

Mode, Pin 2

The mode input should be connected to V_{CC} for 625 line or to 0V for 525 line operation.

Greyscale, Pin 5

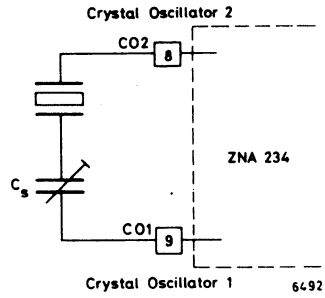
The greyscale output is produced by a D to A converter from the horizontal counter. The D to A converter is effectively a switched current sink providing 8 equal current steps of approx. 60μA/step. When used with an external pull-up resistor, 8 voltage steps are produced (approx. 0.3V/step with $R_L = 5K$). The output has a saturation level of approximately +2V and requires a buffer stage (emitter follower) to match into the video/sync mixer.

Oscillator, Pins 8 and 9

The ZNA234 oscillator can be driven in several ways, depending on the application.

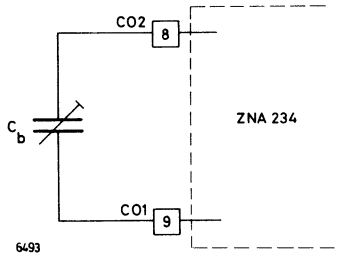
(a) Using external 2.50MHz crystal (625 lines mode)

Series
Resonant
Crystal



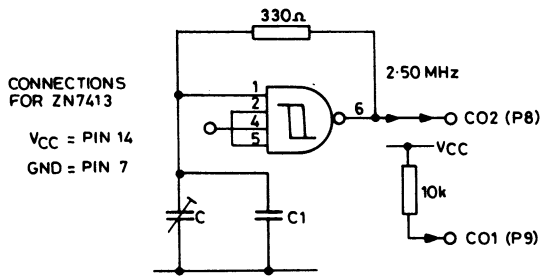
C_s is normally about 22pF

(b) If stability is not important, a capacitor may be used instead of the crystal.



$C_b \approx 15pF$

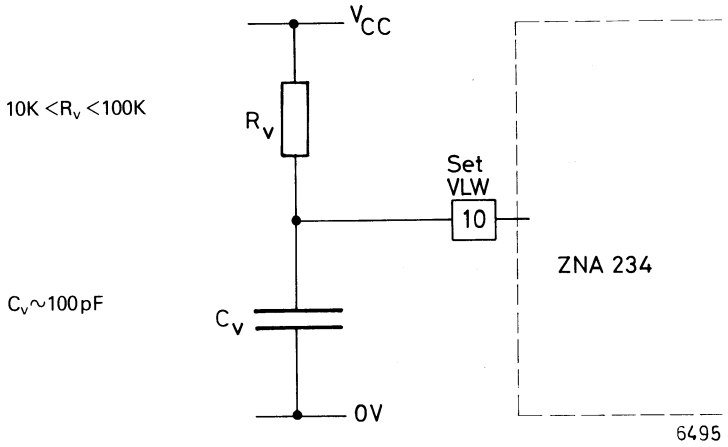
(c) Alternative oscillator circuits.



The external oscillator pulse width t_w, must be within the range shown in the table on page 2.

Vertical Line Width, Pin 10

Provision has been made for the width of the vertical lines to be varied if required. With pin 10 open circuit, the width of the vertical line pulses generated by the device is approximately 300ns. The pulse width may be varied from 100ns to 1μs by connecting a capacitor and resistor to pin 10 as shown below.



Increasing C_V or R_V will produce a wider pulse.

N.B. If pin 10 is left open circuit to give a 300ns pulse width, any external capacitance on the pin (e.g. from long lead or p.c.b. track) will affect the timing. It is, therefore, recommended that if pin 10 is to be left open circuit then no connection at all is made to it.

Test Inputs, Pins 6 and 15

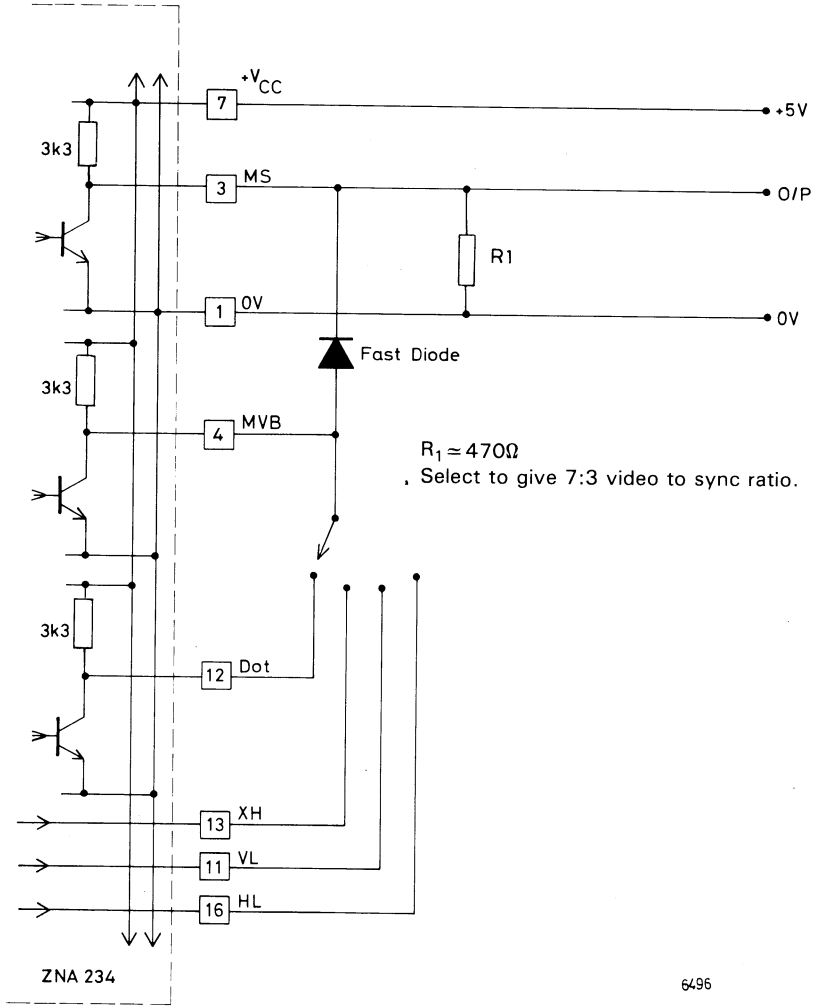
These should be connected to 0V.

Circuits for Video/Sync Mixer

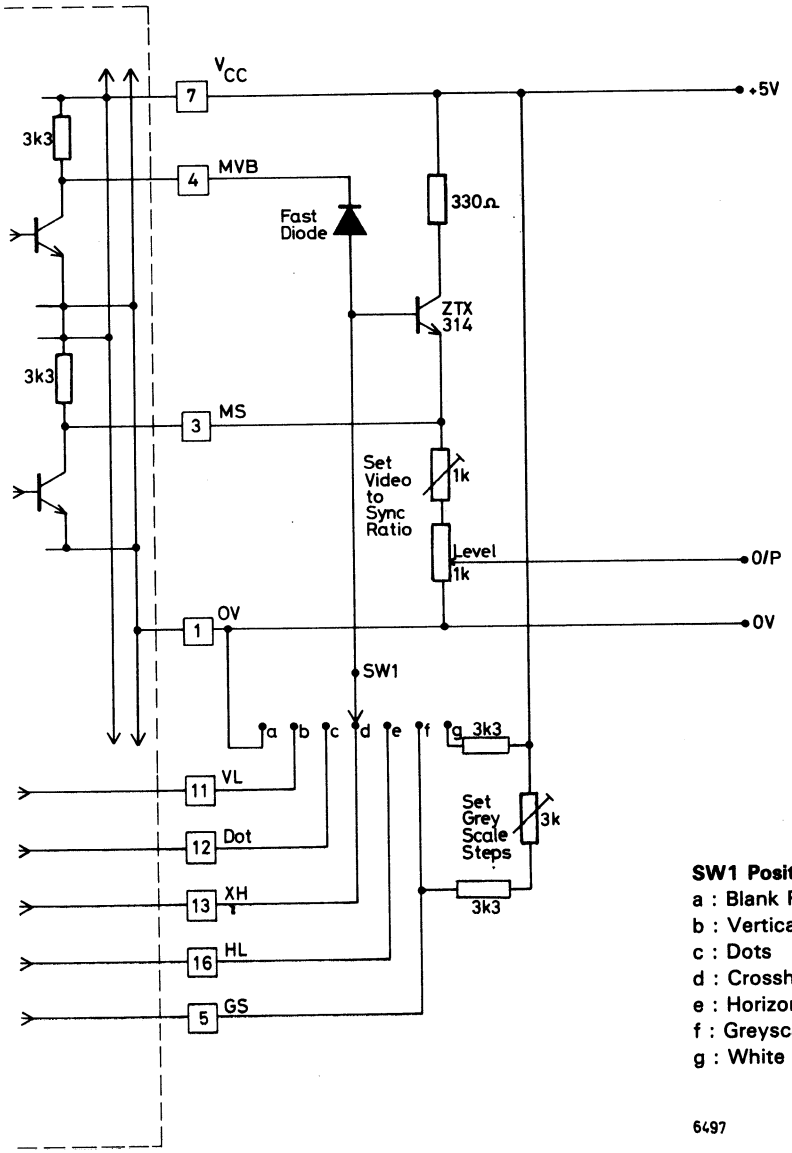
The following two circuits on pages 9 and 10 for the video/sync mixer are suggested as starting points only. They have been found to work on the bench, but no detailed applications work has been carried out to date.

The circuit on page 9 in probably the simplest possible method, but it does have the disadvantage that the Greyscale output cannot be used owing to its different d.c. levels compared with the video outputs. The second circuit, page 10, is hardly any more complex, and does allow the use of the Greyscale output.

SIMPLE CIRCUIT FOR VIDEO/SYNC MIXER (NO GREYSCALE)



CIRCUIT FOR VIDEO/SYNC MIXER ALLOWING USE OF GREYSCALE



SW1 Positions
a : Blank Raster
b : Vertical Lines
c : Dots
d : Crosshatch
e : Horizontal Lines
f : Greyscale
g : White Raster

6497

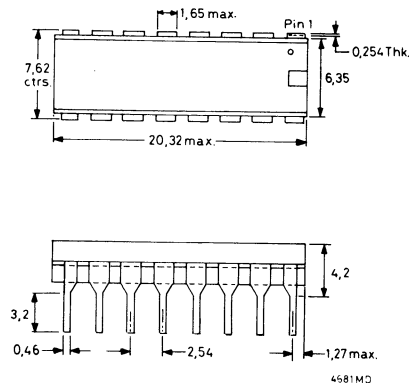
The following Companies can supply suitable crystals for use with the ZNA234

IQD
(Interface Quartz Devices Limited),
Crewkerne,
Somerset.
Tel: 0460 74433 Telex: 46283
Contact: Mr. Jarvis

McKnight Crystal Company,
Hardley Industrial Estate,
Hythe, Southampton.
Tel: 0703 848961 Telex: 47506
Contact: Mr. Carpenter

SEI
(Salford Electrical Instruments Limited)
Times Mill,
Heywood, Lancashire OL10 4NE
Tel: 0706 67501 Telex: 635106
Contact: Mr. P. Kenyon or Mr. D. Standring

PACKAGE DETAILS



16 Lead Moulded D.I.L.
Dimensions in millimetres

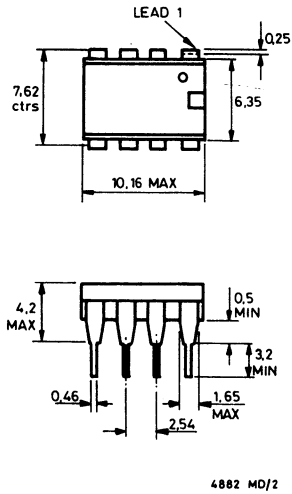
6. Package Details

Contents

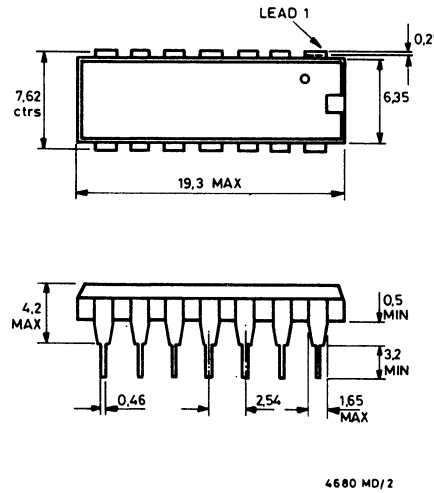
page

Package Drawings and Outlines 6- 2

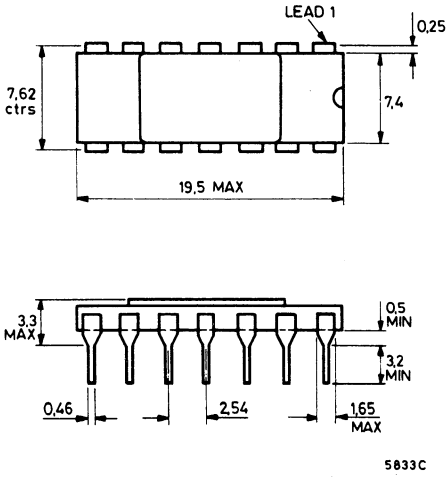
PACKAGE OUTLINES



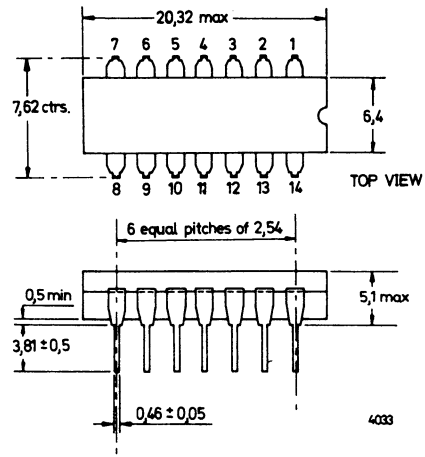
8 LEAD MOULDED DIL (E8)



14 LEAD MOULDED DIL (E14)



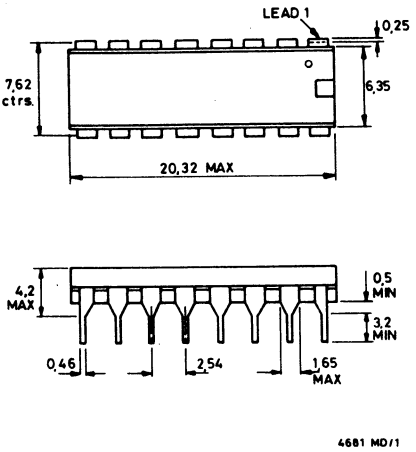
14 LEAD CERAMIC DIL (H14)



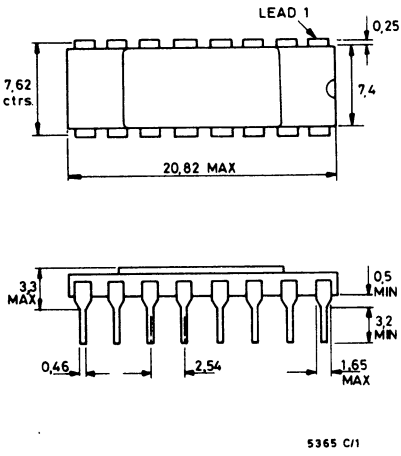
14 LEAD CERDIP (J14)

Dimensions in millimetres

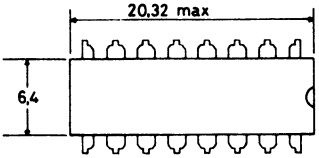
PACKAGE OUTLINES

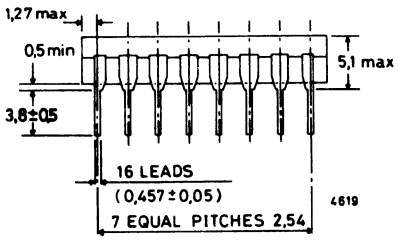


16 LEAD MOULDED DIL (E16)

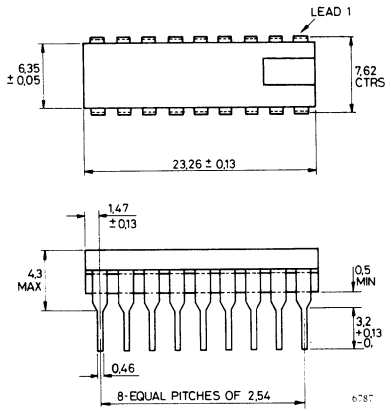


16 LEAD CERAMIC DIL (H16)





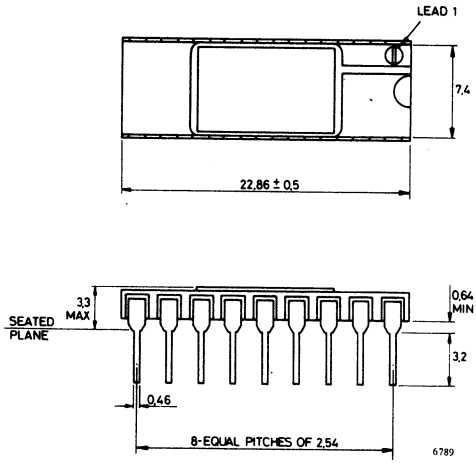
16 LEAD CERDIP (J16)



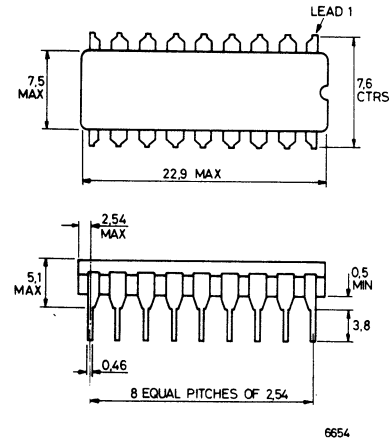
18 LEAD MOULDED DIL (E18)

Dimensions in millimetres

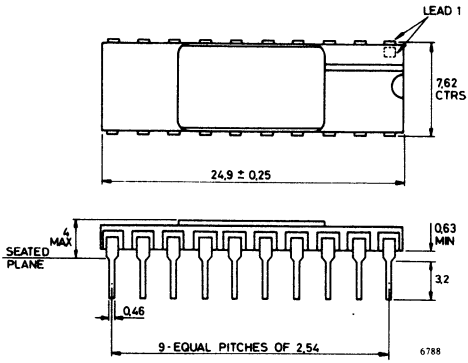
PACKAGE OUTLINES



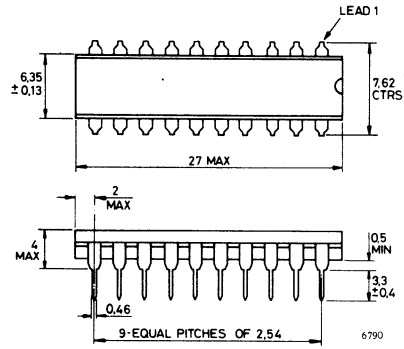
18 LEAD CERAMIC DIL (H18)



18 LEAD CERDIP (J18)



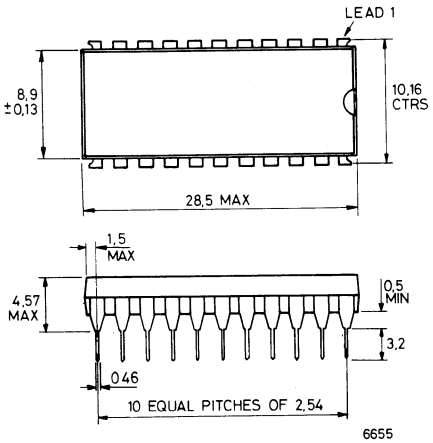
20 LEAD CERAMIC DIL (H20)



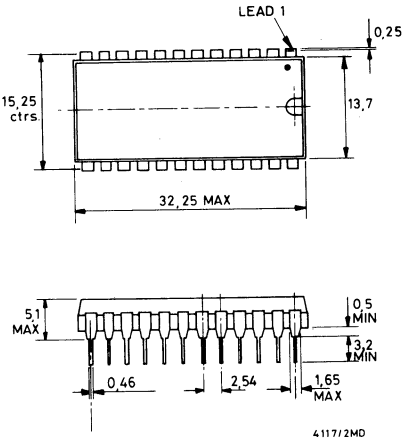
20 LEAD CERDIP DIL (J20)

Dimensions in millimetres

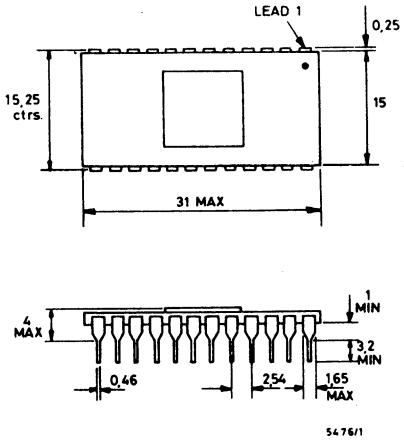
PACKAGE OUTLINES



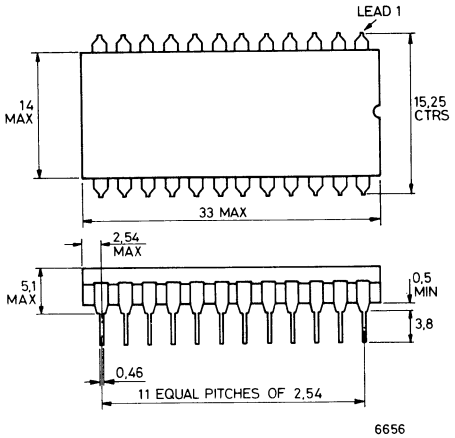
22 LEAD MOULDED DIL (E22)



24 LEAD MOULDED DIL (E24)



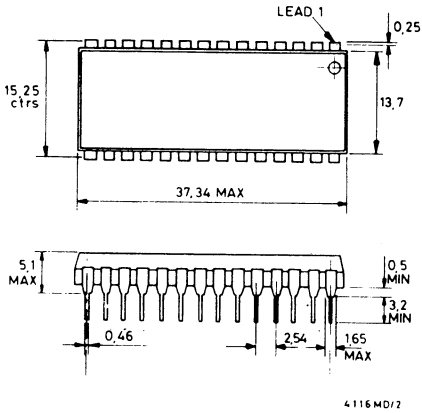
24 LEAD CERAMIC DIL (H24)



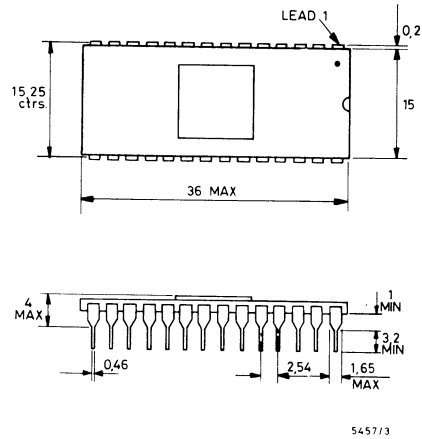
24 LEAD CERDIP DIL (J24)

Dimensions in millimetres

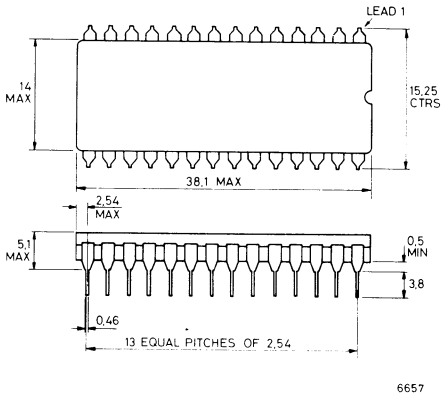
PACKAGE OUTLINES



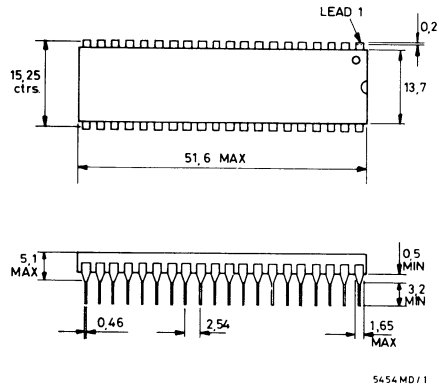
28 LEAD MOULDED DIL (E28)



28 LEAD CERAMIC DIL (H28)



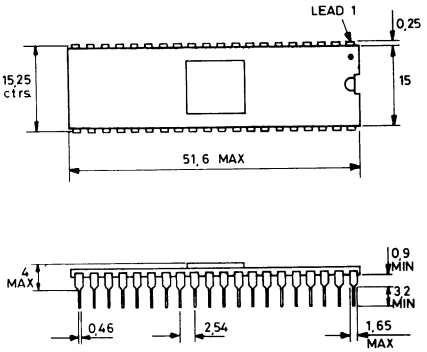
28 LEAD CERDIP (J28)



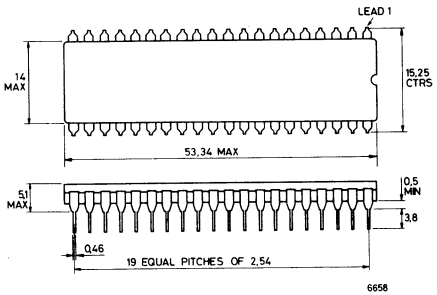
40 LEAD MOULDED DIL (E40)

Dimensions in millimetres

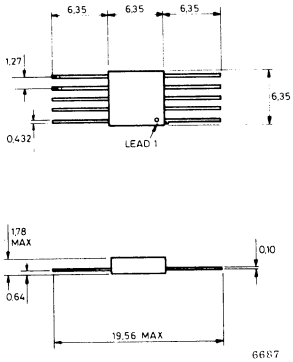
PACKAGE OUTLINES



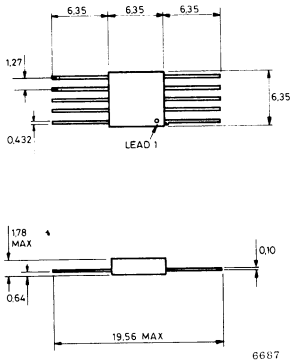
40 LEAD CERAMIC DIL (H40)



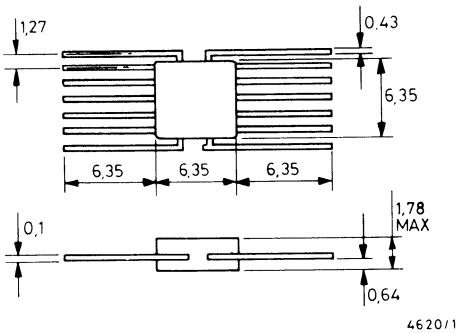
40 LEAD CERDIP (J40)



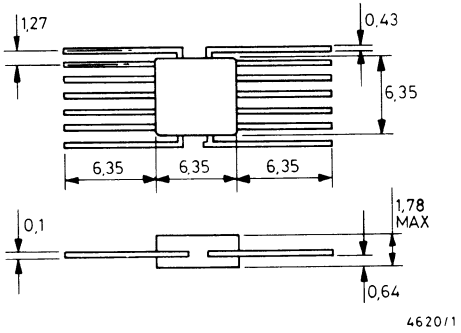
10 LEAD CERAMIC FLAT-PACK (F10)



10 LEAD CERPACK (FM10)



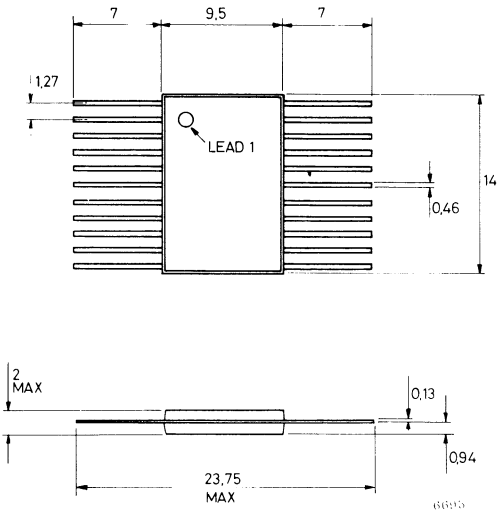
14 LEAD CERAMIC FLAT-PACK (F14)



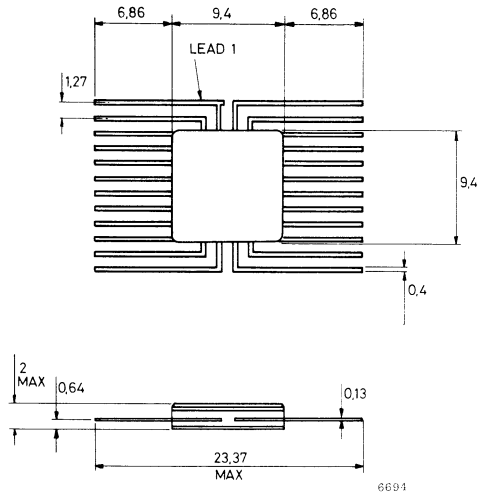
14 LEAD CERPACK (FM14)

Dimensions in millimetres

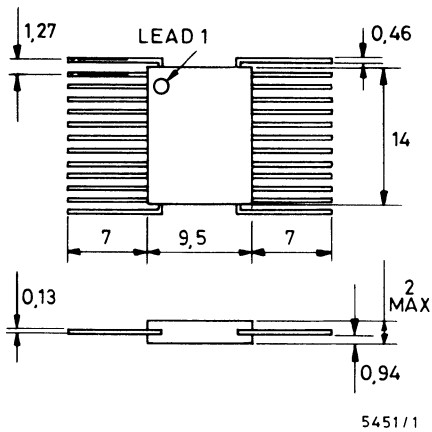
PACKAGE OUTLINES



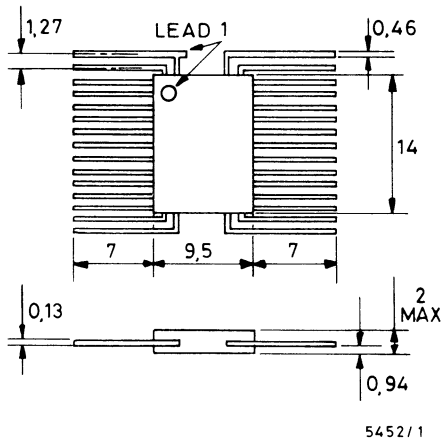
22 LEAD MOULDED FLAT-PACK (G22)



24 LEAD CERAMIC FLAT-PACK (F24)



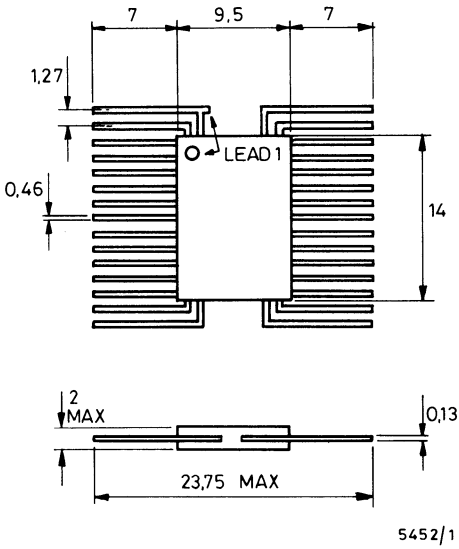
26 LEAD MOULDED FLAT-PACK (G26)



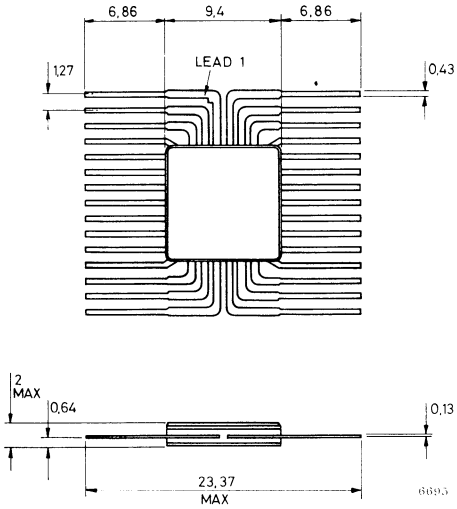
30 LEAD MOULDED FLAT-PACK (G30)

Dimensions in millimetres

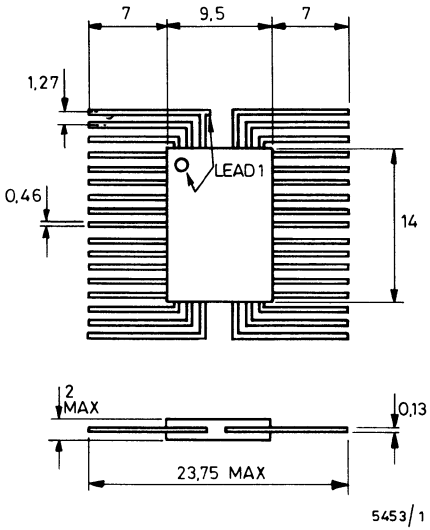
PACKAGE OUTLINES



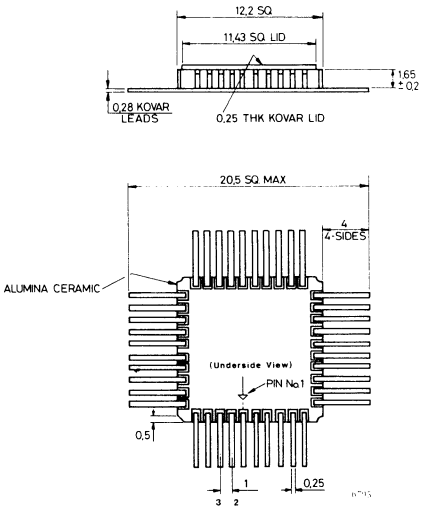
30 LEAD MOULDED FLAT-PACK (G30)



30 LEAD CERAMIC FLAT-PACK (F30)



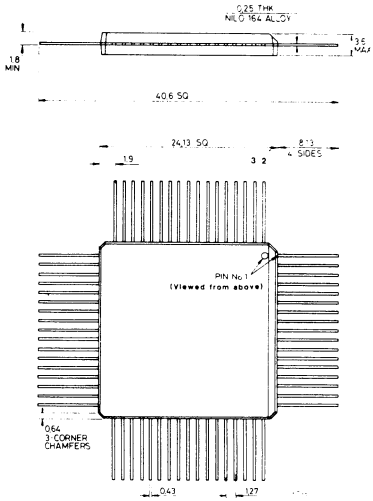
34 LEAD MOULDED FLAT-PACK (G34)



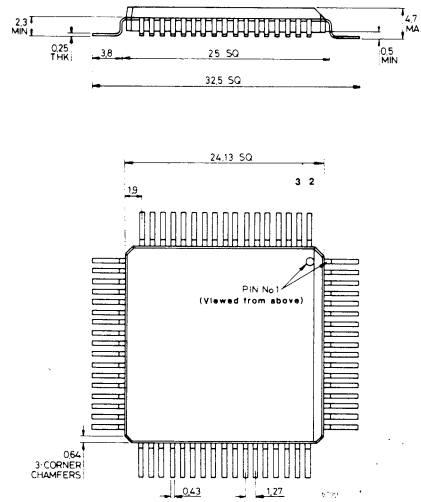
40 LEAD CERAMIC CHIP CARRIER (FM40)

Dimensions in millimetres

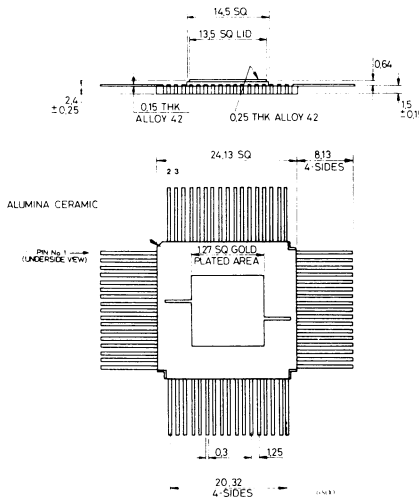
PACKAGE OUTLINES



68 LEAD MOULDED FLAT-PACK (GU68)
(Unjoggled)



68 LEAD MOULDED FLAT-PACK (GJ68)
(Joggled)

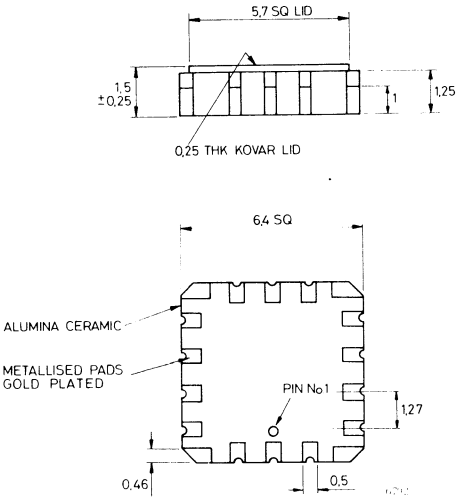


68 LEAD CERAMIC CHIP CARRIER (FM68)

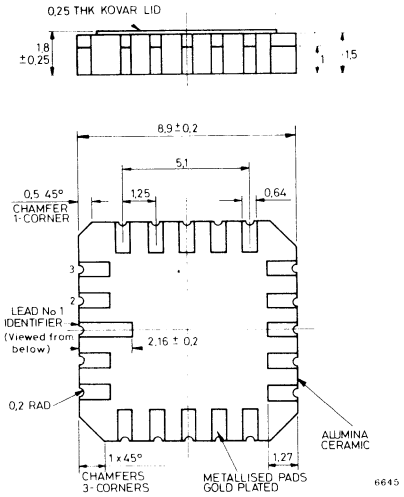
Dimensions in millimetres

PACKAGE OUTLINES

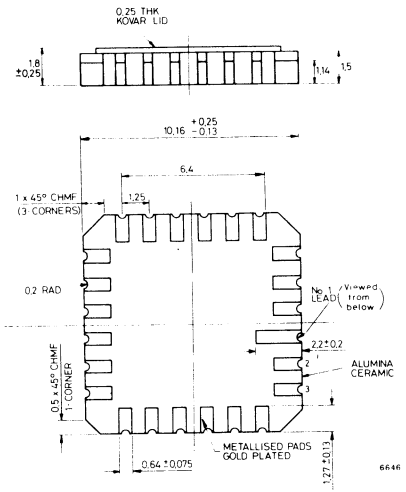
CHIP CARRIERS



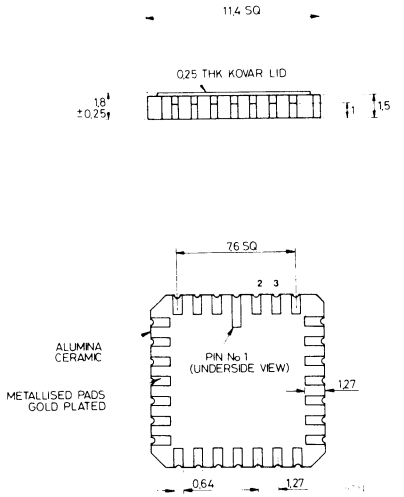
18 LEAD CERAMIC (M18)



20 LEAD CERAMIC (M20)



24 LEAD CERAMIC (M24)

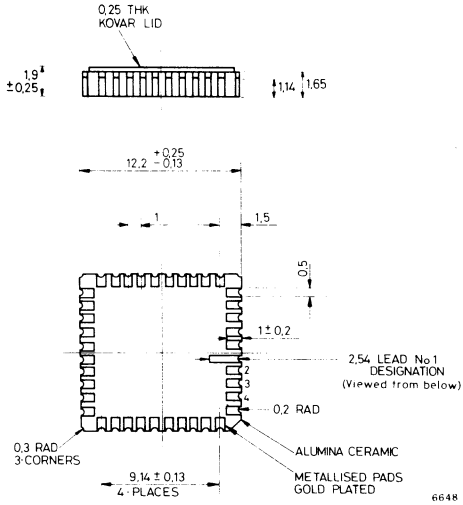


28 LEAD CERAMIC (K28)

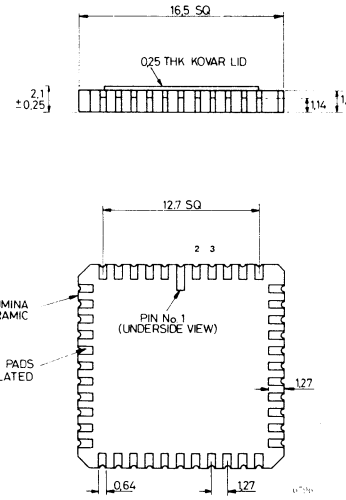
Dimensions in millimetres

PACKAGE OUTLINES

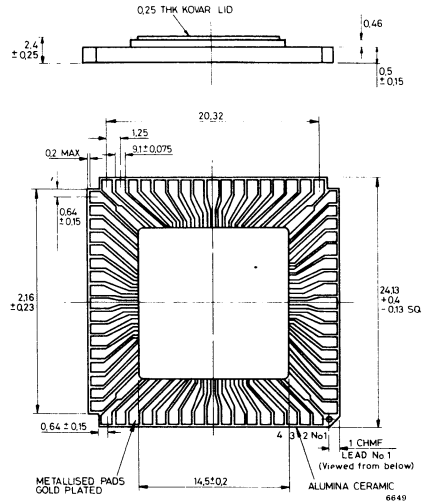
CHIP CARRIERS



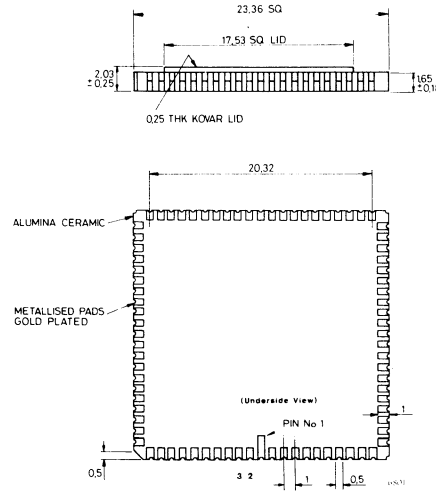
40 LEAD CERAMIC (K40)



44 LEAD CERAMIC (M44)



68 LEAD CERAMIC (M68)

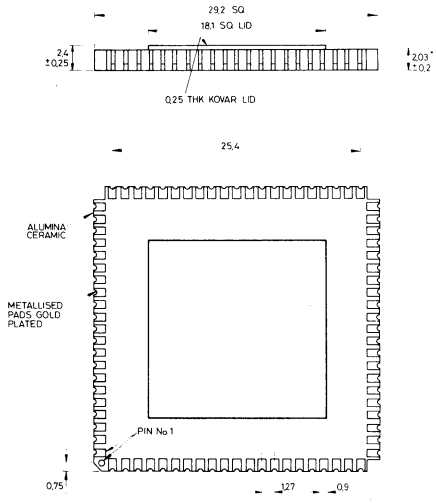


84 LEAD CERAMIC (K84)

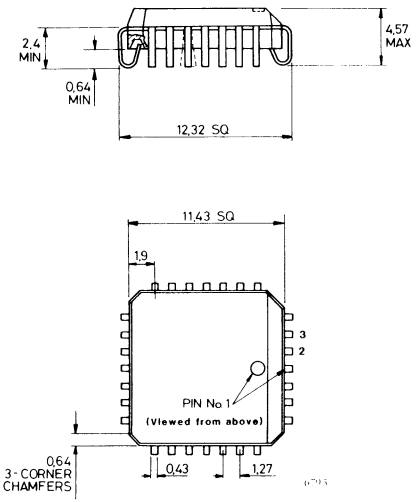
Dimensions in millimetres

PACKAGE OUTLINES

CHIP CARRIERS

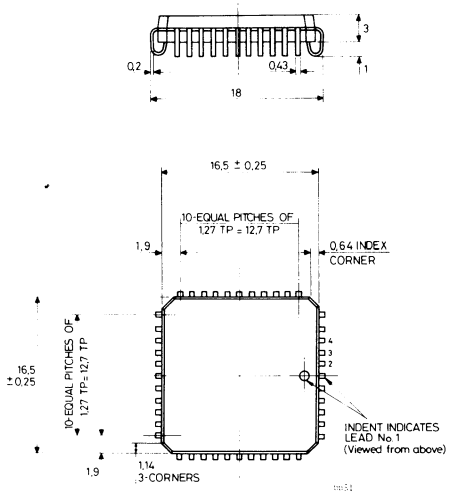


84 LEAD CERAMIC (M84)

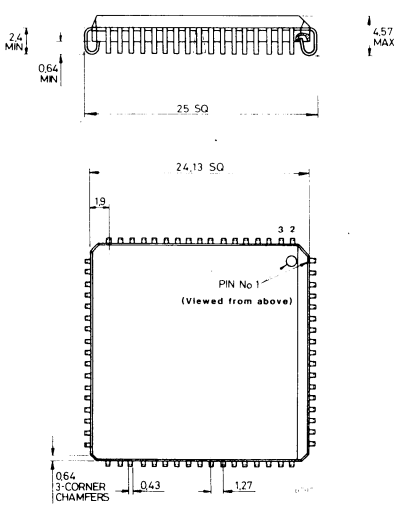


28 LEAD MOULDED (Q28)

Dimensions in millimetres



44 LEAD MOULDED (Q44)



68 LEAD MOULDED (Q68)

Dimensions in millimetres

PO14

7. Application Notes

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7. Application Notes

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A/D-Umsetzer – ihre Parameter, die Wandlungsverfahren und Anwendungsbeispiele

A/D-Umsetzer — ihre Parameter, die Wandlungsverfahren und Anwendungsbeispiele

Ing. (grad.) Jürgen Rymus*

Teil 1

A/D-Umsetzer dienen in der Regel der Aufbereitung von Signalen, deren Werte dann oft weiterverarbeitet werden müssen. Da gibt es einiges zu beachten.

Bis vor einigen Jahren konnte man den Markt der A/D- und D/A-Umsetzer mit kleinen Stückzahlen, vielen speziellen Typen und hohen Einzelstückpreisen gleichsetzen. Diese Wandler waren ausschließlich in Hybrid- oder Modultechnik aufgebaut, mit den mechanischen Abmessungen von etwa 10 cm × 5 cm × 1,2 cm.

In Applikationen, in denen A/D-Umsetzer zur Aufbereitung von Signalen verwendet wurden, hat man meist aus Gründen der hohen Stückkosten solche Bauteile mit der im Bild 1 dargestellten Organisation bevorzugt. Ein Umsetzer wurde für mehrere Kanäle verwendet.
Die in eine Spannung umgewandelten physikalischen Größen — hier Temperatur, Weg und Durchfluß — werden von Anpassungsverstärkern verarbeitet. Vom Anpassungsverstärker wird dann das oft hochohmige, bei 1 Volt liegende, Signal des Meßwertwandlers auf ca. 10 Volt verstärkt und dem A/D-Wandler zugeführt.

Der Wandler mußte so ausgelegt werden, daß er die Anforderungen aller Kanäle abdecken konnte. Da die einzelnen Kanäle über den Multiplexer abgefragt werden, erhöht sich mit der Anzahl der Kanäle die geforderte Wandlungszeit. Der zeitliche Ablauf des analogen Multiplexers, der Sample-Holdbausteine und des A/D-Wandlers wurde durch die CPU gesteuert. Die Hauptnachteile eines solchen Systems liegen in der Schwierigkeit, analoge Signale zu übertragen, denn Spezialkabel sind teuer, platzaufwendig und schwer.
In den letzten Jahren hat sich dieses Bild gewandelt. Durch die Zunahme der Technisierung, die einfachere und kostengünstigere Verarbeitung von digitalen Signalen und den rapid ansteigenden Mikroprozessor-Markt wurde die Forderung nach kostengünstigen A/D- und D/A-Umsetzern immer deutlicher. Die höheren Qualitätsanforderungen an Systeme konnten nur noch digital bewältigt werden.
Die Herausforderung an den Hersteller von integrierten Schaltungen war damit ausgesprochen. Das Ergebnis ließ nicht lange auf sich warten — Wandler bis 12 bit zu bedeutend niedrigeren Preisen sind als integrierte Schaltungen heute erhältlich. Damit steigen die Anwendungsmöglichkeiten, und neue Märkte tun sich auf; was aufgrund der steigenden Gesamtstückzahlen zu einem weiteren Preisverfall führt. Heute ist es nur noch für Ausnahmefälle sinnvoll, Eigenentwicklungen von Wandlern vorzunehmen. Konsequenterweise haben sich auch neue Schnittstellen zwischen der analogen und der digitalen Welt ergeben (Bild 2).
Der Wandler wird unmittelbar in die Nähe des Meßwandlers gebracht, da die digitale Information einfacher zu übertragen ist und die Anforderung an die Wandlungszeit überwiegend nur noch durch die Probleme der zu wandelnden physikalischen Größen des einzelnen Kanals bestimmt wird. Bei dieser Konfiguration entfällt die analoge Mehrfachabfrage. Die analogen Größen aller Kanäle können simultan abgefragt werden.

* Herr Rymus ist Mitarbeiter der Ferranti GmbH in München

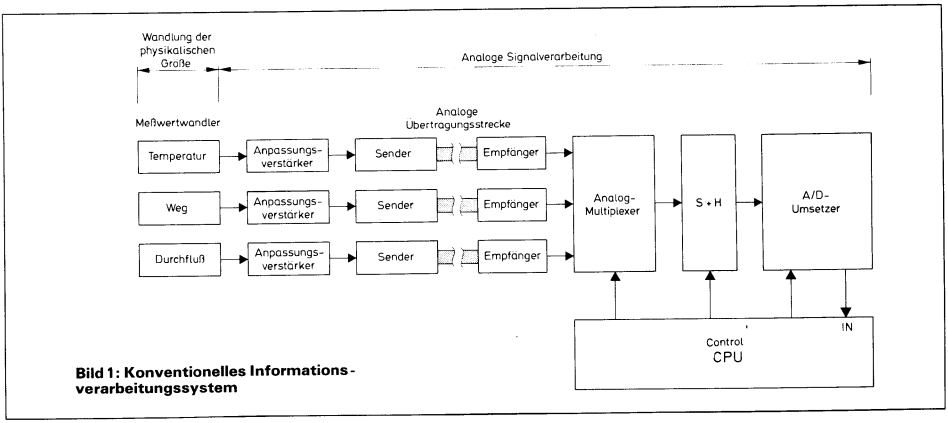

Bild 1: Konventionelles Informationsverarbeitungssystem

Begriffe bei A/D- und D/A-Umsetzern

A/D-Umsetzverfahren
- Wägeverfahren oder schrittweise Annäherung (Successive Approximation)
- Nachlaufverfahren (Tracking-Converter)
- Doppelintegrationsverfahren (Dual-Slope)
- Stufenumsetzverfahren (Staircase and Comparator, Single Slope)

A/D-Parameter
- Wandlungszeit (Conversion Time)
- Informationslücke (Missing Code)
- Quantisierungsfehler (Quantising Error)

D/A-Umsetztechnik
- R-2R Widerstandsnetzwerk

D/A-Parameter
- Einschwingzeit (Settling Time)
- Monotonie (Monotonicity)

Gemeinsame Begriffe für A/D- und D/A-Umsetzer
- Auflösung (Resolution)
- Nichtlinearität (Nonlinearity)
- Differentielle Nichtlinearität (Differential Nonlinearity)
- Skalenfaktorfehler (Scale Factor Error oder Gain Error)
- Offsetfehler (Offset Error)
- FS (Full Scale)
- MSB (Most Significant bit)
- LSB (Least Significant bit)

Code
(Beispiel: 3 bit-Umsetzer)

A/D	Eingang	Ausgang			Eingang	Ausgang		
D/A	Ausgang	Eingang			Ausgang	Eingang		
Code	unipolar	binär			bipolar	offset binär		
		bit 1 (MSB)	bit 2	bit 3 (LSB)		bit 1 (MSB)	bit 2	bit 3 (LSB)
	FS-1 LSB	1	1	1	+(FS-1 LSB)	1	1	1
	FS-2 LSB	1	1	0	1/2 FS	1	1	0
	1/2 FS + 1 LSB	1	0	1	+ 1 LSB	1	0	1
	1/2 FS	1	0	0	0	1	0	0
	1/2 FS-1 LSB	0	1	1	− 1 LSB	0	1	1
	1/2 FS-2 LSB	0	1	0	− 1/2 FS	0	1	0
	1 LSB	0	0	1	−(FS-1 LSB)	0	0	1
	0	0	0	0	− FS	0	0	0

Ob die digitale Größe eine Eingangs- oder Ausgangsgröße ist, wird durch den verwendeten Wandler, ob A/D oder D/A, bestimmt. Der Code ist einfach realisierbar und als rechnerfreundlich zu bezeichnen. Ob ein Wandler analoge Werte zwischen −FS und +(FS-1 LSB) oder 0 und FS-1 LSB verarbeiten soll, ist durch einfache externe Beschaltung an den Bausteinen bestimmbar.

D/A-Umsetzer

Ein D/A-Umsetzer ist ein Baustein, der eine digitale Eingangsinformation in eine korrespondierende analoge Ausgangsinformation umsetzt. Die Ausgangsinformation steht meist als Spannung oder Strom zur Verfügung.

Idealer D/A-Umsetzer

Unter der Annahme, der D/A-Umsetzer liefert eine unipolare Ausgangsspannung U_{out} und am Eingang liegt die digitale Information im Binär-Code an, dann gilt:

$$U_{out} = U_{FS}(B_1 \times 2^{-1} + B_2 \times 2^{-2} + B_3 \times 2^{-3} + ... + B_n \times 2^{-n})$$

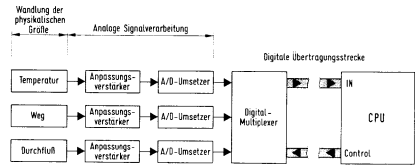

Bild 2: Informationsverarbeitungssystem mit je einem A/D-Umsetzer pro Kanal

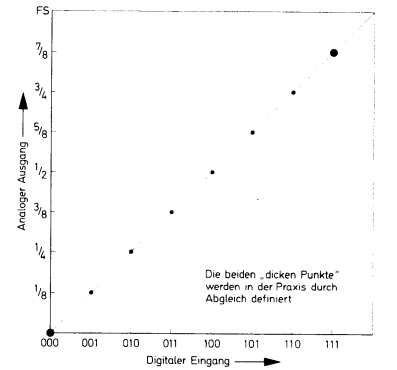

Bild 3: Übertragungskennlinie für den idealen 3 bit D/A-Umsetzer

B_1 ist das „most significant bit" (MSB) und
B_n ist das „least significant bit" (LSB).

Die Bits B_1 und B_n können die Werte „1" oder „0" annehmen. Der kleinste noch mögliche Spannungswert (bzw. Stromwert), der von einem Wandler verarbeitet wird, bestimmt die einzelnen Intervalle. Der kleinste mögliche Schritt, der durch Bauelemente-Toleranzen bestimmt ist, wird als LSB — Wert der kleinsten Stufe — bezeichnet.

$$1\ LSB = U_{FS} \times 2^{-n}$$

Die maximale Ausgangsspannung erhält man, wenn alle Bits = 1 sind.

$$U_{out} = U_{FS}\left(\frac{2^n - 1}{2^n}\right) = U_{FS} - 1\ LSB$$

Mit einem n-bit-Wandler ergibt sich die Anzahl der Stufen zu $2^n - 1$ und der Endwert dadurch zu FS — 1 LSB. Der quasi erreichbare analoge Endwert (Full-Scale) wird mit FS bezeichnet und das führende bit (Most Significant Bit) mit MSB. Beim Anlegen des MSB erhält man beim D/A am analogen Ausgang FS/2.
Die Übertragungskennlinie eines idealen 3 bit-D/A-Wandlers ist in Bild 3 gezeigt. Beim Anlegen jeder der 8 digitalen Eingangsgrößen, erhält man die entsprechende analoge Ausgangsgröße, dargestellt durch einen Punkt auf der Übertragungskennlinie. Im Idealfall liegen alle Punkte auf der gestrichelten Linie. Nicht berücksichtigt ist momentan die Einschwingzeit, die der Wandler benötigt.
Für einen 3 bit D/A-Wandler mit U_{FS} = 2,5 V ergeben sich die nachfolgenden Werte:

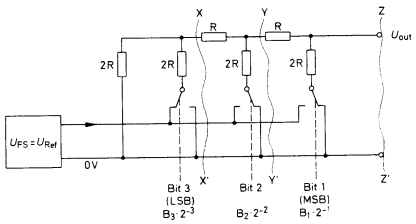

Bild 4: R-2R Widerstandsnetz mit Schaltern und Referenzspannung

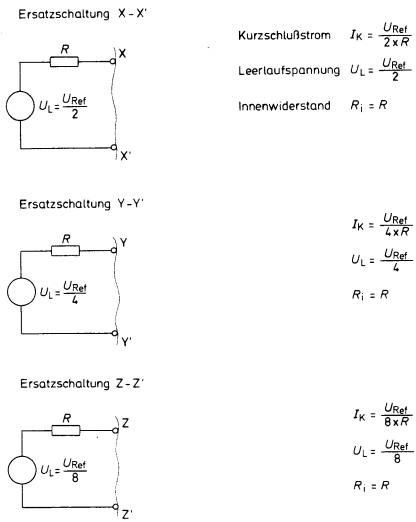

Bild 4a: Ersatzschaltungen

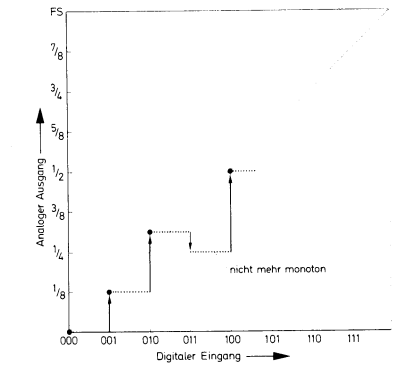

Bild 5: Grenze zwischen monoton und nicht monoton

N ≙ Dezimalzahl des am Wandlereingang angelegten digitalen Codes

$U_{out_N} = U_{FS} (B_1 \times 2^{-1} + B_2 \times 2^{-2} + B_3 \times 2^{-3})$

$U_{out_7} = 2{,}5\ V\ (\frac{1}{2} + \frac{1}{4} + \frac{1}{8}) = 2{,}5\ \frac{7}{8}\ V = U_{FS} - 1\ LSB$

$U_{out_4} = 2{,}5\ V\ (\frac{1}{2} + 0 + 0) = 2{,}5\ \frac{1}{2}\ V = MSB$

$$1\ LSB = \frac{U_{FS}}{2^n} = \frac{2{,}5\ V}{2^3} = 0{,}3125\ V$$

Anzahl der Stufen $= 2^n - 1 = 8 - 1 = 7$.
(bzw. Intervalle)
Die praktische Verwirklichung eines D/A-Umsetzers mit einem R/2R Widerstandsnetzwerk für 3 bit Wandler zeigt Bild 4.
Die Gewichtung wird durch das R-2R Leiternetzwerk vorgenommen. Über den Schalter B_1 bis B_3 werden die 2R-Widerstände entweder an Masse (B_n ≙ „0") oder mit der Referenzspannung U_{Ref} (B_n ≙ „1") verbunden. Der Vorteil des Netzwerkes liegt für die integrierte Schaltungstechnik im niedrigen Widerstandsverhältnis von nur 1:2. Das R-2R Widerstandsnetzwerk ist für monolithische Schaltungen bis zu 8 bit geeignet. Die Referenzspannung U_{Ref}, die bei allen Wandlern benötigt wird, entspricht U_{FS}.
Schneidet man das Netzwerk an der Stelle x—x', y—y' und z—z' auf und betrachtet es nach links, dann erhält man die nachfolgenden Ersatzschaltungen (Bild 4a). Der Schalter B_3 liegt dabei an der Referenzspannung und die beiden anderen Schalter B_2 und B_1 liegen an Masse.
Damit ergibt sich

$$U_{out} = U_{Ref} \times 2^{-3}$$

entsprechend kann abgeleitet werden

$U_{out} = U_{Ref} \times 2^{-2}$ (B_1 ≙ „0", B_2 ≙ „1", B_3 ≙ „0")

und

$U_{out} = U_{Ref} \times 2^{-1}$ (B_1 ≙ „1", B_2 ≙ „0", B_3 ≙ „0")

Überlagert man die einzelne abgeleitete Ausgangsspannung, dann kommt man zum erwarteten Ergebnis:

$U_{out} = U_{Ref} (B_1 \times 2^{-1} + B_2 \times 2^{-2} + B_3 \times 2^{-3})$

Allgemein:

$U_{out} = U_{FS} (B_1 \times 2^{-1} + B_2 \times 2^{-2} + B_3 \times 2^{-3} + \times .. B_n \times 2^{-n})$

Der Innenwiderstand des Netzwerkes ist R.
Wird das Widerstandsnetzwerk extern mit R_L belastet, gilt

$$U_{out} = \frac{R_L}{R + R_L} U_{Ref} (B_1 \times 2^{-1} + B_2 \times 2^{-2} + B_3 \times 2^{-3})$$

D/A-Parameter
Abweichungen vom idealen Umsetzer ergeben sich durch Widerstandstoleranzen, der Offsetspannung an den analogen Schaltern, durch die Temperaturkoeffizienten der genannten Bauelemente und der Referenzspannung.

Monotonie (Monotonicity)
Monotonie ist für einen Wandler gegeben, wenn die Übertragungsfunktion kontinuierlich ansteigt. Eine Änderung des Eingangssignals um + 1LSB muß eine Erhöhung des Ausgangssignals zur Folge haben, sonst ist der Wandler nicht monoton. Nach dieser Definition wird bei Ferranti in der Praxis ausgetestet. Ein Wandler ist z.B. nicht monoton (Bild 5), wenn bei einer Änderung des Eingangssignals um + 1LSB (z.B. 010 auf 011) sich das Ausgangssignal nicht erhöht.

Offsetfehler (Offset Error)
Der Offsetfehler zeigt sich als Abweichung im Nullpunkt der Übertragungskennlinie. Ist der Offsetfehler nicht auf 0 abgeglichen, tritt ein konstanter, absoluter Fehler für die Übertra-

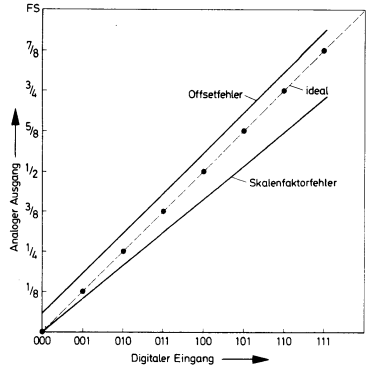

Bild 6: Offsetfehler und Skalenfaktorfehler

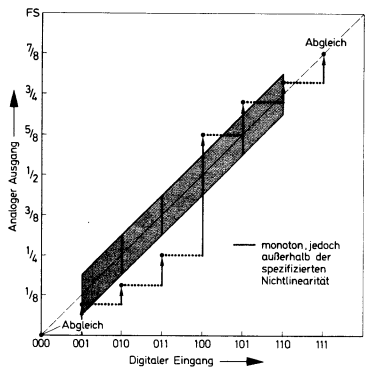

Bild 7: Nichtlinearität beim 3 bit D/A-Umsetzer

gungskennlinie auf. Offsetfehler entstehen durch die Übergangswiderstände der Gehäuseanschlüsse, der Bond-Anschlüsse und die Offsetspannung der analogen Schalter (Bild 6).

Skalenfaktorfehler (Scale Factor Error oder Gain Error)
Die Abweichung wird durch unterschiedliche Verstärkungswerte und die Temperaturkoeffizienten der Bauelemente hervorgerufen und ist die Abweichung zwischen der tatsächlichen und der idealen Übertragungsgeraden. Der Fehler wird meistens in ppm/°C angegeben (Bild 6).

Nichtlinearität (Linearity Error)
Der Offset- und Skalenfaktorfehler können durch Abgleich eliminiert werden. Nicht abgleichbar ist die Nichtlinearität eines Wandlers. Unter der Nichtlinearität versteht man die maximale Abweichung von der idealen Geraden durch den Null- und den Endpunkt. Ist dieser Fehler innerhalb ± 1/2 LSB spezifiziert, dann ist die Umsetzung innerhalb des schraffierten Bereiches zulässig. Liegt ein Übertragungspunkt außerhalb, dann erfüllt der Wandler die Spezifikation nicht.
Ein Wandler kann bezüglich der Nichtlinearität außerhalb der Spezifikation liegen und erfüllt, wie in Bild 7 gezeigt, trotzdem noch die Anforderung der Monotonie.

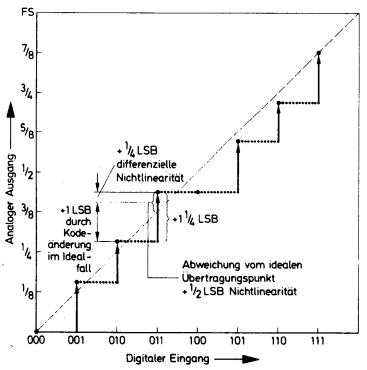

Bild 8: Differentielle Nichtlinearität im Vergleich zur Nichtlinearität. Die Übertragungspunkte würden innerhalb eines mit ±½ LSB Nichtlinearität spezifizierten Wandlers liegen und trotzdem wäre der Wandler nicht monoton

Differentielle Nichtlinearität (Differential Linearity)
Angegeben wird hiermit die Abweichung zweier benachbarter Stufen gegenüber der tatsächlichen Übertragungsfunktion. Die Abweichung wird, wie meistens auch bei der Nichtlinearität, über das LSB spezifiziert (Bild 8). Bei der Darstellung der Übertragungskennlinie wurde von der Annahme ausgegangen, daß der Umsetzer mit nachfolgenden Fehlern behaftet ist:

Bit 1 (MSB) — 1/2 LSB
Bit 2 + 1/4 LSB
Bit 3 (LSB) + 1/4 LSB.

Um den Unterschied zwischen Nichtlinearität und differentieller Nichtlinearität nochmals zu verdeutlichen, sind die Fehler der einzelnen Punkte der Übertragungskennlinie in der folgenden Tabelle festgehalten:

Digitaler Code	differentielle Nichtlinearität	Nichtlinearität
000		0
001	+1/4 LSB	+1/4 LSB
010	0	+1/4 LSB
011	+1/4 LSB	+1/2 LSB
100	−1 LSB	−1/2 LSB
101	+1/4 LSB	−1/4 LSB
110	0	−1/4 LSB
111	+1/4 LSB	0

Auflösung (Resolution)
Die Auflösung hängt von dem kleinstmöglichen Schritt (LSB) ab, der von einem D/A- oder A/D-Wandler noch verarbeitet werden kann. Mit steigender Bitzahl eines Wandlers erhöht sich die Auflösung. Die Auflösung eines Wandlers sagt nichts über die Abweichung zur idealen Übertragungskennlinie hin aus.

A/D-Umsetzer — ihre Parameter, die Wandlungsverfahren und Anwendungsbeispiele

Ing. (grad.) Jürgen Rymus*

Teil 2

Nutzbare Auflösung (Useful Resolution)

Hat ein D/A-Umsetzer z.B. eine differentielle Nichtlinearität von $-1\frac{1}{2}$ LSB, dann ist er nicht mehr monoton und in den meisten Anwendungsbereichen nicht mehr einsetzbar. Setzt man den LSB-Eingang konstant auf „0", dann erhält man einen n-1 bit-Wandler. Das LSB des n-1-Wandlers ist doppelt so groß wie das des n-Wandlers. Die differentielle Nichtlinearität von $-1\frac{1}{2}$ LSB erniedrigt sich für den n-1 Wandler auf $-0{,}75$ LSB — der Wandler ist also monoton mit einer Auflösung von n-1 bits. Dieser Zusammenhang ist in Bild 9 gezeigt. Aus Gründen der Produktionsstreuung fallen neben den n-bit-Wandlern auch n-1 bit-Wandler an, die für den Kunden Preisvorteile bieten.

Einschwingzeit (Settling Time)

Das ist die gesamte Zeit, die notwendig ist, damit ein D/A-Umsetzer bei einem entsprechenden Sprung auf den Ausgangswert innerhalb eines definierten Fehlerbandes einschwingt. Dabei ist der Fehler meist mit $\pm\frac{1}{2}$ LSB spezifiziert, bei Änderungen des Eingangssignals (Beispiel 8 bit) von 01111111 auf 10000000 oder 00000000 auf 11111111. Die Zustandsänderung ist selbstverständlich umkehrbar.

Bipolarer Betrieb

Bis jetzt wurde nur der unipolare Betrieb eines Wandlers betrachtet, d.h. beim D/A-Wandler wurde der Ausgangsspannungsbereich zwischen 0 und +(FS − 1 LSB) festgelegt. In Anwendungen, bei denen es darauf ankommt, daß sich der Ausgangsspannungsbereich zwischen −FS und +(FS − 1 LSB) ändert, kann dies durch Addition einer negativen Komponente von −FS/2 zur Ausgangsspannung des unipolaren Betriebes erreicht werden (Bild 10). Wie man anhand der Übertragungskennlinie (Bild 11) sieht, sind alle Ausgangswerte negativ, wenn das MSB „0" und positiv, wenn das MSB „1" ist. In diesem Anwendungsfall bezeichnet man den Eingangskode als offset binär und die erzeugte Ausgangsspannung als bipolar.

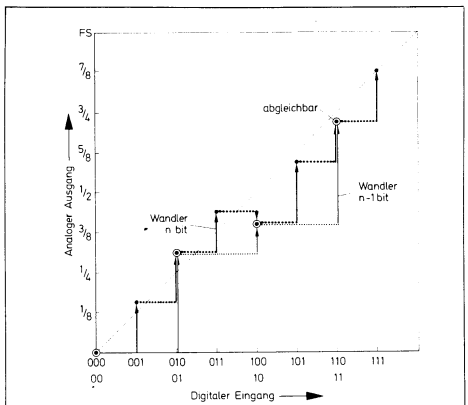

Bild 9: Nutzbare Auflösung

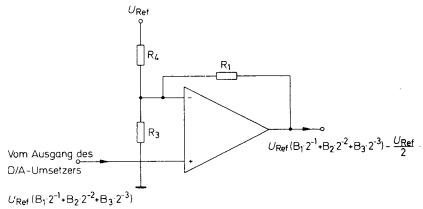

Bild 10: Bipolarer Betrieb eines Umsetzers

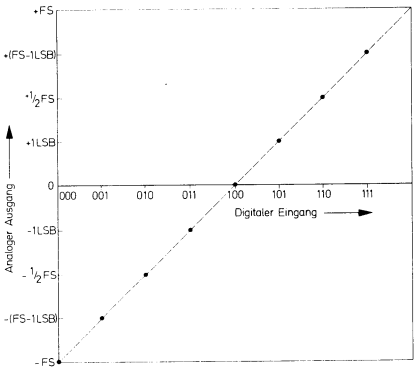

Bild 11: Übertragungskennlinie für einen 3 bit D/A-Umsetzer im bipolaren Betrieb

A/D-Umsetzer

Ein A/D-Umsetzer ist ein Baustein, der eine analoge Eingangsgröße in eine korrespondierende digitale Ausgangsgröße umsetzt. Die digitale Ausgangsinformation steht meist im Binärkode zur Verfügung.

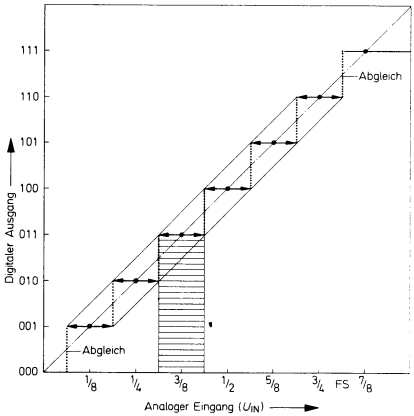

Bild 12: Übertragungskennlinie eines idealen 3 bit A/D-Wandlers

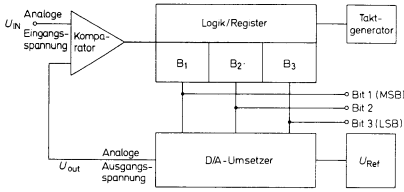

Bild 13: Prinzipschaltbild für einen 3 bit A/D-Wandler nach dem Wägeverfahren

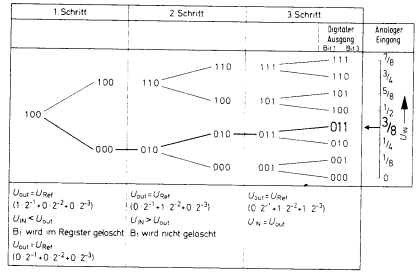

Bild 14: Ablauf eines 3 bit A/D-Wandlers nach dem Wägeverfahren. Es ist angenommen, daß der analoge Eingangswert $U_{in} = \frac{3}{8}$ FS beträgt.

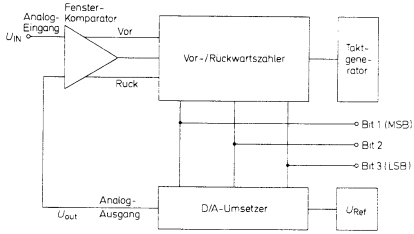

Bild 15: Blockschaltbild für einen 3 bit A/D-Wandler

Idealer A/D-Umsetzer

Unter der Voraussetzung, daß am Eingang eine unipolare Spannung anliegt und am Ausgang der Binärkode vorliegt, gilt:

$$U_{FS}\,(B_1 \times 2^{-1} + B_2 \times 2^{-2} + B_3 \times 2^{-3} + B_n \times 2^{-n})$$

$$= U_{iN} \pm \tfrac{1}{2}\,\text{LSB}$$

Die Übertragungskennlinie für einen idealen 3 bit A/D-Umsetzer ist im Bild 12 dargestellt. Die Entscheidungsunsicherheit ist für jede digitale Ausgangsgröße mit Ausnahme der zwei abgeglichenen Werte (000 auf 001 und 110 auf 111) $\pm \frac{1}{2}$ LSB. Nochmals verdeutlicht ist dies für die analoge Eingangsgröße $\frac{3}{8}$ FS. Das bedeutet, daß die analoge Eingangsspannung, die zu einem bestimmten digitalen Kode gehört, nur mit einer Unsicherheit von $\pm\frac{1}{2}$ LSB bestimmt werden kann. Diese Tatsache wird als Quantisierungsfehler bezeichnet. Der Quantisierungsfehler ist kein echter Fehler, sondern er ist durch die Bandbreite des digitalen Kodes bestimmt.

Analog-Digital-Umsetzungsverfahren

Wägeverfahren (Successive Approximation)

Im Prinzip besteht ein A/D-Wandler in der Praxis aus einem D/A-Wandler und einigen Zusatzfunktionen. Hier im Fall der schrittweisen Approximation benötigt man zusätzlich zum D/A-Umsetzer einen Komparator, etwas Logik und ein Register. Am Ausgang (Bild 13) des D/A-Umsetzers steht in Abhängigkeit der anliegenden Information die Spannung U_{out}. Dieser Wert wird an den Eingang des Komparators gegeben und mit der analogen Eingangsspannung U_{iN} verglichen. Ist $U_{iN} = U_{out}$, dann stoppt der Komparator den fest programmierten Ablauf der Logik. Bei der schrittweisen Annäherung beginnt man mit der höchsten Stelle (MSB) — dieses Bit 1 wird dann an den D/A-Umsetzer angelegt. Damit erhält man am Ausgang des D/A-Umsetzers

$$U_{out} = U_{Ref}\,(1 \times 2^{-1} + 0 \times 2^{-2} + 0 \times 2^{-3}) = U_{Ref}\,2^{-1}$$

Annahme: $U_{in} = \frac{3}{8}$ FS

Da $U_{in} < U_{out}$ wird Bit 1 im Register gelöscht und das Bit 2 über die Logik am D/A angelegt.

$$U_{out} = U_{Ref}\,2^{-2}$$

dieser Wert wird am Komparator mit U_{in} verglichen; $U_{in} > U_{out}$ damit bleibt Bit 2 im Register usw. bis der gesuchte Endwert 011 nach drei Schritten erreicht ist und zur Weiterverarbeitung zur Verfügung steht. Der Ablauf für einen 3 bit A/D-Wandler nach der sukzessiven Approximation ist im Detail für eine Eingangsspannung $U_{in} = \frac{3}{8}$ FS im Bild 14 dargestellt.

Nachlaufverfahren (Tracking Converter)

Der Fenster-Komparator (Bild 15) vergleicht die analoge Eingangsspannung U_{in} mit der analogen Ausgangsspannung U_{out} des D/A-Umsetzers. Ist U_{in} mindestens $\frac{1}{2}$ LSB größer als U_{out}, läuft der Zähler mit der Taktfrequenz in Vorwärtsrichtung. Die

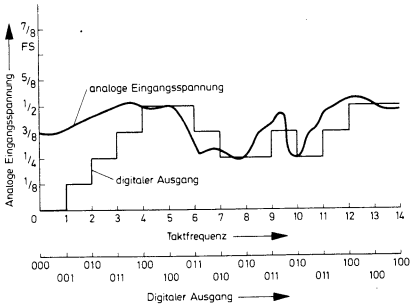

Bild 16: Zusammenhang zwischen analoger Eingangsspannung und digitalem Ausgangssignal

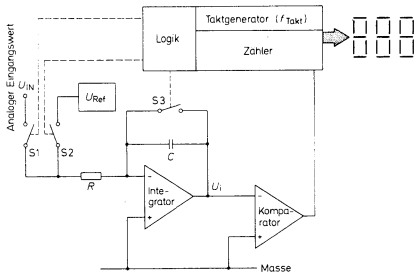

Bild 17: Prinzipschaltbild des Doppelintegrationsverfahrens

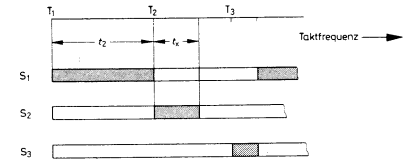

Bild 18: Kontaktdiagramm der Schalter

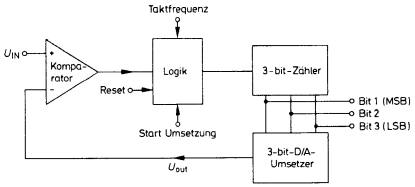

Bild 19: 3 bit A/D-Wandler nach dem Stufenumsetzerverfahren

analoge Größe U_{out} erhöht sich entsprechend der einlaufenden Impulse. Jeder einlaufende Impuls erzeugt eine Spannungserhöhung von U_{out} um 1 LSB. Es kommt zum Zählerstillstand, wenn $U_{in} = U_{out}$ ist. Der Zählerstand entspricht dem gesuchten digitalen Wert. Eine Abweichung zwischen U_{in} und U_{out} um $\frac{1}{2}$ LSB wird vom Fenster-Komparator registriert, der den Zähler aktiviert ($+\frac{1}{2}$ LBS in Vorwärtsrichtung $-\frac{1}{2}$ LSB in Rückwärtsrichtung). Den Zusammenhang zwischen der analogen Eingangsspannung und des digitalen Ausgangs zeigt Bild 16. Nimmt man an, daß die Taktfrequenz 1 MHz ist, dann dauert ein Schritt 1 µs. Nach 4 µs hat hier der Wandler die analoge Eingangsgröße $FS\frac{1}{2}$ in den digitalen Kode 100 umgesetzt; dabei wurde vorausgesetzt, daß am Ausgang 000 anlag.

Doppelintegrationsverfahren (Dual Slope)

Das im folgenden beschriebene Verfahren unterscheidet sich von den bereits erörterten Umsetzverfahren dadurch, daß kein D/A-Umsetzer benötigt wird, d.h. daß auch kein R-2R Widerstandsnetzwerk erforderlich ist (Bild 17). S_1 bis S_3 sind in der Praxis Schalttransistoren. Wie man sieht, wird in der Phase t_2 der Umsetzung, der Kondensator C durch die analoge Eingangsspannung aufgeladen. Die Zeit, während der Kondensator aufgeladen wird, ist konstant – die Ladung auf dem Kondensator ist dem Analogsignal proportional. Der Schalter wird dann auf die Referenzspannung umgelegt und der Kondensator entlädt sich. Die Zeit, die der Kondensator zur Entladung benötigt, wird gemessen, und zwar auf die Weise, daß der Takt vom Zähler gezählt wird. Die digitale Information wird dann kodiert und angezeigt (Bild 18).

Der Schalter S_1 wird zum Zeitpunkt T_1 geschlossen, alle anderen Schalter sind geöffnet. Die umzuwandelnde positive analoge Spannung U_{in} wird vom Integrator während einer konstanten Anzahl von Taktimpulsen von T_1 bis zum Zeitpunkt T_2 integriert. Dabei läuft die Ausgangsspannung U_i am Integrator nach der Gleichung

$$U_i = -\frac{1}{R \times C} \times \int_0^{t_2} U_{in}\, dt = -\frac{U_{in}}{R \times C} \times t_2 \qquad (1)$$

t_2 = konstant
U_i = Ausgangsspannung Integrator
U_{in} = analoge Eingangsspannung

Daß der Schalter S_1 exakt nach t_2 geöffnet bzw. S_2 geschlossen wird, gewährleistet die Logik. Mit dem Schließen des Schalters S_2 wird der Integrationseingang auf $+U_{Ref}$ gelegt; damit läuft seine Ausgangsspannung U_i nach der Gleichung

$$U_i = -\frac{U_{in}}{R \times C} \times t_2 + \frac{1}{R \times C} \int_0^{t_x} U_{Ref}\, dt \qquad (2)$$

$$= -\frac{U_{in}}{R \times C} \times t_2 + \frac{U_{Ref} \times t_x}{R \times C}$$

U_{Ref} = Referenzspannung

Der Zähler zählt während der Zeit t_x die Taktimpulse. Durch die Zustandsänderung am Komparator am Ende der Zeit t_x wird der Zähler gestoppt. Die Zahl der gezählten Taktimpulse entspricht dem analogen Eingangswert.

Da der Integrator von U_i in der Zeit t_x auf Null gelaufen ist, erhält man aus (2)

$$\frac{U_{in}}{R \times C} \times t_2 = \frac{U_{Ref} \times t_x}{R \times C} \qquad (3)$$

$R \times C$ kann in Gleichung (3) herausgekürzt werden, da dieser Wert während der Zeit $t_2 + t_x$ als konsequent anzusehen ist.

$$t_x = \frac{U_{in}}{U_{Ref}} \times t_2 \qquad (4)$$

Die Kurzzeitkonstante für das Zeitglied R × C und den Taktgenerator läßt sich ohne weiteres erreichen:

$$n = \frac{t_2}{1/f_{Takt}} \triangleq \text{Anzahl der Impulse}$$

$$z = \frac{U_{in}}{U_{Ref}} \times n$$

z = Zählerstand

Der Zählerstand z ist proportional der angelegten analogen Eingangsspannung.
Die Zeit t_2 soll so gewählt werden, daß sie durch 20 ms (50 Hz) oder 16,6 ms (60 Hz) teilbar ist. Hält man diese Bedingung ein, dann ist der Mittelwert der überlagerten Netzbrummspannung Null.

Stufenumsetzverfahren (Single Slope)
Liegt die Taktfrequenz an und ist der Startbefehl zur Umsetzung des Analogsignals gegeben, dann läuft der Vorgang wie folgt ab (Bild 19): Die Taktfrequenz wird vom Zähler gezählt und liegt im Binärkode am Eingang des D/A-Umsetzers an. Die Spannung U_{out} steigt solange an, bis der Wert von U_{out} gleich der Analogspannung U_{in} ist. Zu diesem Zeitpunkt ändert der Komparator seinen Zustand. Dies hat zur Folge, daß weitere Taktimpulse nicht mehr an den Zähler gegeben werden. Die am Ausgang des Zählers vorliegende digitale Information entspricht der Analogspannung U_{in}. Soll der Vorgang von neuem ablaufen, so wird über den Resetimpuls der Zähler auf Null gesetzt und die Umsetzung kann von neuem beginnen.
Ebenso wie D/A-Wandler sind auch A/D-Wandler mit Fehlern behaftet. Da die meisten A/D-Umsetzer einen D/A-Umsetzer als Referenz verwenden, sind zum großen Teil auch die Fehlerquellen dieselben.

Quantisierungsfehler (Quantising Error, Uncertainty)
Der Quantisierungsfehler tritt nur bei A/D-Wandlern auf. Jeder Eingangskode beim D/A-Umsetzer ruft einen analogen Ausgangswert hervor. Nicht so beim A/D-Wandler: Hier wird eine Ausgangszustandsänderung erst bei einer Änderung des Eingangswertes um 1 LSB erreicht. Es ist deshalb auch nicht möglich, vom Ausgangskode her den genauen analogen Eingangswert zu bestimmen. Wie schon angedeutet, werden beim A/D-Wandler die Übergänge von „0" auf „1" und von (2^n-2) auf (2^n-1) abgeglichen. Da der Quantisierungsfehler durch die Bandbreite des digitalen Kodes gegeben ist, wird dieser in den Datenblättern nicht erwähnt. Mit Hilfe von Bild 20 soll gezeigt werden, daß der Fehler 0 LSB aber auch 1 LSB (im Idealfall) sein kann. Für die rechnerische Ermittlung der Linearität ordnet man dem digitalen Kode dem mittleren Wert des Spannungsbereiches zu und spezifiziert den Quantisierungsfehler mit $\pm 1/2$ LSB.

Beispiel (FS = 2,56 V)

		3 bit A/D	8 bit A/D
Abgleichpunkte	Nullübergang „0" auf „1"	000 → 001	0000000 → 00000001
	analoge Eingangsspannung 1/2 LSB	320 mV	10 mV
	Übergang (2^n-2) auf (2^n-1)	110 → 111	11111110 → 11111111
	analoge Eingangsspannung FS − 1/2 LSB	2080 mV	2545 mV
Quantisierungsfehler ±1/2 LSB		±160 mV	± 5 mV

Informationslücke (Missing Code)
Das Auftreten einer Informationslücke beim Wandeln läßt sich sehr gut an einem 3-bit-A/D-Wandler, der nach dem Stufenumsetzverfahren arbeitet, erklären (Bild 19), unter der Annahme, daß der verwendete 3-bit-D/A-Umsetzer nach dem Test als nicht monoton klassifiziert wurde, und zwar bei der Digitalkode-Änderung von 011 auf 100. Ist dies der Fall, so erhöht sich U_{out} während der Kodeänderung (011 → 100) nicht um den

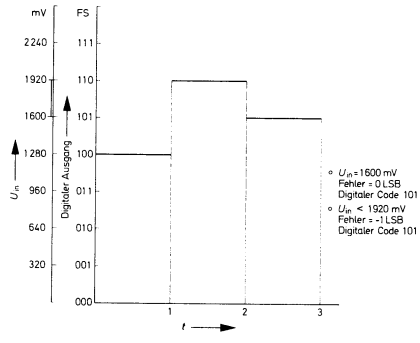

Bild 20: Ein 2-bit-A/D-Wandler, der nach dem Annäherungsverfahren arbeitet. Nach 3 Schritten ist der analoge Eingangswert in die digitale Größe umgesetzt

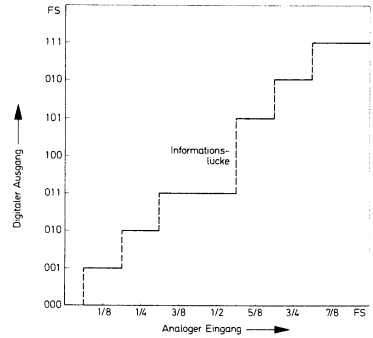

Bild 21: Darstellung der Informationslücke

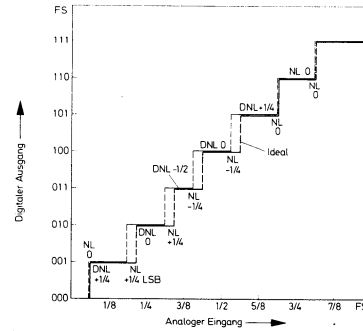

Bild 22: Nichtlinearität und differentielle Nichtlinearität eines 3-bit-A/D-Wandlers

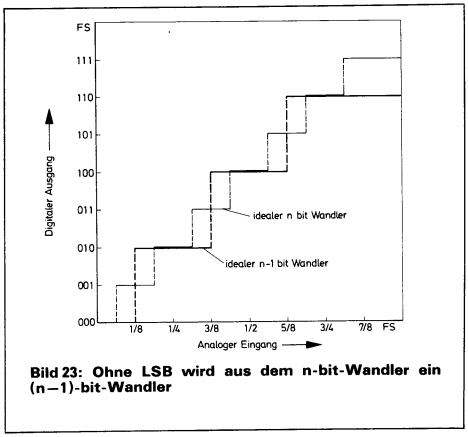

Bild 23: Ohne LSB wird aus dem n-bit-Wandler ein (n−1)-bit-Wandler

gewünschten Betrag. Der 3-bit-Zähler wird nicht gestoppt, der Kode 100 steht am Ausgang des A/D-Wandlers nicht zur Weiterverarbeitung zur Verfügung. Das Fehlen dieses Kodes bezeichnet man als Informationslücke (Bild 21).

Nichtlinearität (Non-Linearity, Linearity Error) und differentielle Nichtlinearität (Differential Nonlinearity)

Die Nichtlinearität ist die Abweichung der idealen Übertragungskennlinie zur tatsächlichen. Die Abweichung wird als Bruchteil eines LSBs angegeben. Bei der differentiellen Nichtlinearität wird die Abweichung mit der idealen A/D-Wandler-Bandbreite verglichen (Bild 22).
Für einen A/D-Wandler, dessen Nichtlinearität mit $\pm 1/2$ LSB spezifiziert ist, muß diese Komponente zu der im Idealfall geltenden Gleichung addiert werden.

$$U_{FS}(B_1 \times 2^{-1} + B_2 \times 2^{-2} + B_3 \times 2^{-3} + \cdots + B_n \times 2^{-n}) = U_{IN} \pm 1/2 \text{ LSB } \pm 1/2 \text{ LSB}.$$

Wandlungszeit (Conversion Time)

Es geht um die Zeit, die ein A/D-Wandler benötigt, bis die anliegende analoge Information in den digitalen Kode umgesetzt ist.

Auflösung (Resolution) und nutzbare Auflösung (Useful Resolution)

Die Auflösung eines A/D-Wandlers entspricht der Anzahl der bits am Ausgang des Wandlers. Sie sagt nichts über die Genauigkeit des Bauteils aus.
Die nutzbare Auflösung ist der Anzahl der bits identisch, bei denen der A/D-Wandler keine Informationslücken aufweist. Aus einem n-bit-Wandler wird ein (n−1)-bit-Wandler, wenn das LSB nicht benutzt wird (Bild 23).
Angenommen 10-bit-A/D-Wandler hält die im Datenblatt garantierte Nichtlinearität nicht ein, jedoch die Spezifikation für einen 9 bit Wandler, so wird der A/D-Wandler mit einer Auflösung von 10 bit mit einer nutzbaren Auflösung von 9 bit angeboten.

Prinzipien der Analog- Digital-Wandlung*

*Nachdruck aus Markt & Technik 50/81

Prinzipien der Analog-Digital-Wandlung

von Gerhard Rösch

Die »Qual der Wahl« hat der Entwickler durchzustehen, der sich mit dem Problem der Datenwandlung befassen muß. Neben den überwiegend englischsprachigen Datenblättern erschwert eine Vielzahl von verschiedenen Wandlungssystemen die Auswahl für den »idealsten« Umsetzbaustein. Die gebräuchlichsten Analog-Digital-Umsetzprinzipien, deren Aufbau sich besonders für monolithische Technologien eignen, werden im folgenden Artikel ausführlich beschrieben.

Das »Flußdiagramm« zur Auswahl des passenden Analog-Digital-Wandlers sieht an erster Stelle die Entscheidung zwischen der Auflösung und der Umsetzgeschwindigkeit vor. Der Grund hierfür liegt in den vollkommen unterschiedlichen Umsetzverfahren der jeweiligen Converter. Ein Wandler für ein 3¾stelliges Digitalvoltmeter (maximal 3999 Stellen entsprechen ungefähr 12 Bit) basiert in den meisten Fällen auf dem Dual-Slope-Prinzip und hat eine Wandlungszeit von ca. 0,3 s; um Größenordnungen schneller sind dagegen Parallelwandler — allerdings mit einer Auflösung von meist »nur« 6 Bit. Die hohe Geschwindigkeit wird hier durch die parallele Verarbeitung mit 63 Komparatoren erzielt. Ein 12-Bit-A-D-Umsetzer nach dem Parallelverfahren würde dafür immerhin 4095 Komparatoren benötigen — mit heutiger Technologie noch ein Ding der Unmöglichkeit.

Anhand der für die Umsetzung verwendeten Verfahren können also in erster Näherung auf Geschwindigkeit, Auflösung und damit auf die Applikation Rückschlüsse gezogen werden. Die zur Zeit (speziell für monolithisch integrierte Wandler) üblichen Umsetzmethoden gliedern sich nach der Geschwindigkeit geordnet ungefähr wie in der untenstehenden Tabelle angegeben.

Kapazitive Wandlung

Diese Wandlungsart ist zur Zeit die wohl bekannteste Umsetzmethode. Dies resultiert nicht zuletzt darin, daß fast alle gebräuchlichen Digitalmultimeter nach diesem Prinzip arbeiten. Das dabei verwendete Verfahren, die Dual-Slope- oder Zweirampen-Umsetzung, garantiert eine hohe Auflösung, eine für den erforderlichen Aufwand sehr gute Stabilität, einfachen automatischen Offsetabgleich und auf-

charge replacement (kapazitive Wandlung)	— Verfahren zur Messung der Ladezeit eines Kondensators bis zum Erreichen der Höhe der Meßspannung.
staircase (Treppenspannungsumsetzung)	— Verfahren zur stufenweisen Annäherung des rückgewandelten Digitalsignales bis zur Übereinstimmung mit dem Meßsignal.
successive approximation (Wägemethode)	— Verfahren der Annäherung an das Eingangssignal variabler Schrittweite; jeweils die Hälfte des vorhergehenden Wertes.
flash (parallel)	— Verfahren der direkten Umsetzung: Jedem Analogwert wird eine Schaltschwelle und ein Komparator zugewiesen.

grund der vollen Integrierbarkeit eine einfache Handhabung mit sehr wenigen externen Komponenten.

Die Arbeitsweise des Dual-Slope-Umsetzers gliedert sich in zwei Hauptabschnitte auf:

— In der ersten Phase wird die angelegte Meß- oder Eingangsspannung über eine feste Zeit integriert.

— In der zweiten Phase wird die durch die Integration erreichte Spannung mittels der (negativen) Referenz wieder erniedrigt, um beim Nulldurchgang den angeschlossenen Zähler zu stoppen. Da die Referenz konstant ist, ist hier die Zeit eine Variable.

Wie in Bild 1 ersichtlich, wird die umzusetzende Spannung über einen elektronischen Schalter auf den Integrator geführt. Bei Beginn des Meßzyklus ist die Integrator-Ausgangsspannung zum Beispiel positiv (Bild 2). Während des Nulldurchganges der Komparator-Eingangsspannung schaltet die Logik den Anzeigezähler ein. Dieser läuft danach mit der Frequenz des Taktsignals hoch. Mit Erreichen des Endwertes wird über die Logik der Eingangsschalter auf die negative Referenz umgestellt. Zu diesem Zeitpunkt ist die Spannung am Kondensator C ein direktes Maß für die Höhe der Eingangsspannung, da diese während einer festen Zeit (Zählerstand x Taktperiode) an dieser Kapazität aufintegriert wurde. Nun wird der Kondensator durch die Integration der negativen Referenzspannung entladen, bis die Logik beim Nulldurchgang wieder den Zähler stoppt. Im Gegensatz zum ersten Zyklus ist diese Zeit nicht konstant, sondern ein direktes Maß für die Spannung des Kondensators zum Umschaltmoment. Der Zählerstand wird über ein Ausgangsregister zur Weiterverarbeitung geführt, zur Anzeige gebracht, und der Zyklus beginnt von neuem.

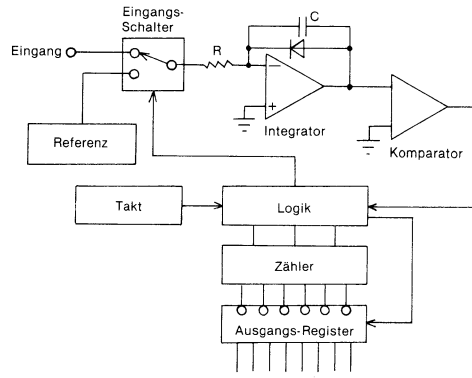

Bild 1: Blockschaltbild eines Dual-Slope-Umsetzers
Werkzeichnungen: Ferranti

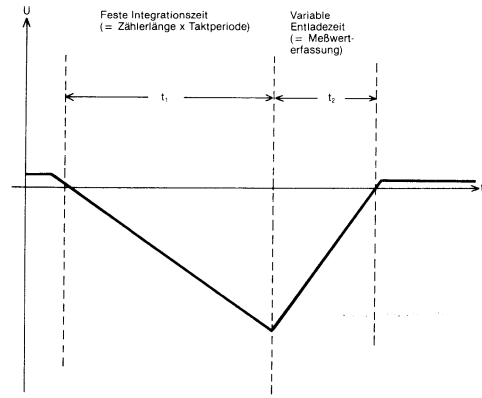

Bild 2: Zeitliche Steuerungsabläufe beim Dual-Slope-Umsetzer

Der Erfolg des Dual-Slope-Umsetzers liegt hauptsächlich in den Eigenschaften der hohen Genauigkeit und Störsicherheit begründet: In die Rechnung für die Genauigkeit beziehungsweise Stabilität des Umsetzers gehen die Langzeitparameter der verwendeten Kondensatoren und Widerstände nicht ein. Nur noch die Kurzzeitwerte können einen Einfluß auf das Meßergebnis ausüben. Da sich typische Zykluszeiten im Bereich von 0,3 s bewegen, kann in erster

Näherung von einem absolut stabilen Verhalten der Bauelemente ausgegangen werden.

Durch das Integrationsverfahren können bei richtiger Auslegung von t_1 (Eingangsspannungs-Integrationsphase) Netzspannungsstörungen vollkommen unterdrückt werden (t_1 = N x 20 ms). Tatsächlich integriert dieser Wandler jede Störung oder Änderung der Eingangsspannung auf; statistisch gesehen werden sich solche Störungen sicherlich nicht auswirken. Daher erübrigt sich im Normalfall die Notwendigkeit eines Sample-and-Hold-Bausteins. Der Nachteil der Dual-Slope-Umsetzer liegt speziell in der niedrigen Umsetzrate von typisch mehreren hundert Millisekunden je nach Auflösung.

Eine schnellere Version ist der sogenannte »Single-Slope-Converter«, der nach einem ähnlichen Verfahren aufgebaut ist: Eine intern erzeugte hochpräzise Sägezahnspannung wird mit Hilfe von zwei Komparatoren im Nulldurchgang und beim Erreichen des Meßwertes erfaßt (Bild 3 und 4). Zwischen dem Erreichen der beiden Schwellwerte wird der angeschlossene Zähler mit einer festen Quarzfrequenz beaufschlagt. Der Zählerstand nach dem Meßzyklus T ist ein direktes Maß für die Potentialdifferenz zwischen den beiden Spannungen. Die Polarität des angelegten Eingangssignals läßt sich aus der logischen Reihenfolge der erreichten Pegel ermitteln.

Obwohl diese Wandlungsart wesentlich schneller als die Zweirampenmethode ist, hat sie fast keinerlei praktische Bedeutung. Es haften ihr alle Probleme der Langzeitkonstanz an, die beim Dual-Slope-Verfahren so elegant gelöst wurden. Quarzfrequenz und hochpräziser Sägezahngenerator sind erforderlich, ebenso ist keine Eliminierung eventuell auftretender Störspannungen möglich.

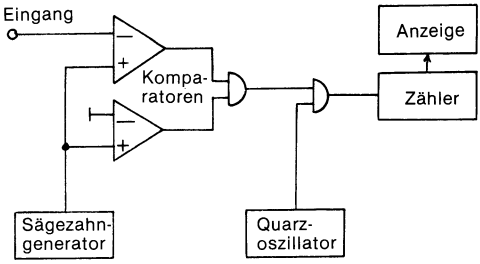

Bild 3: Prinzipschaltung des Single-Slope-Umsetzers

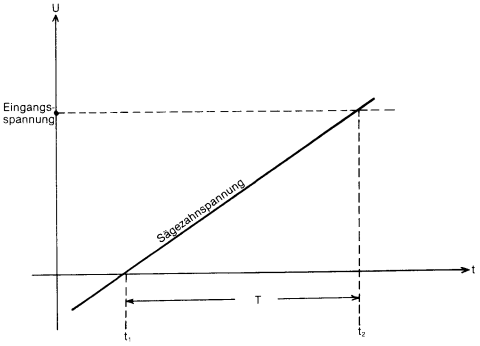

Bild 4: Erfassung der zwei Schwellwerte beim Single-Slope-Umsetzer

Eine weitere Untergruppe aus dem Bereich der Wandler nach der kapazitiven Methode sind Bausteine, die auf dem sogenannten »Charge-Balancing-Verfahren« (Ladungsausgleichs-Verfahren) beruhen. Ein nach diesem Prinzip arbeitender Baustein ist beispielsweise der ZN 450 von Ferranti, eine Einchip-DVM-Schaltung für Flüssigkristallanzeige und 5 V Betriebsspannung (Bild 5). Das zu konvertierende Eingangssignal wird im Delta-Sigma-Modulator (DSM) mit Hilfe des Ladungsausgleichs-Verfahrens in einen Pulsstrom umgewandelt. Die weitere Verarbeitung geschieht voll digital. Sogar die Speicherung der Offsetspannung, normalerweise in einem Kondensator für kurze Zeit festgehalten, wird hier als Teil eines digitalen Zyklus' erfaßt.

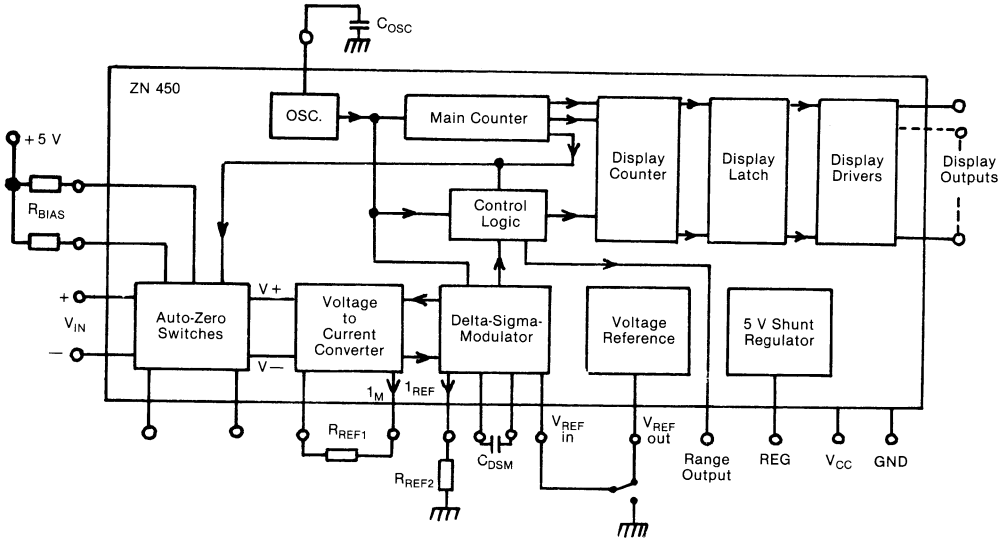

Bild 5: Digitalvoltmeter-Baustein nach dem Ladungsausgleichs-Verfahren (Charge-Balancing)

Der Offset wird als negatives Eingangssignal vom Endwert des Zählers abgezogen und damit ein Vorsetzen der Fehlerspannung erzielt, so daß sich beim nächsten Zyklus dieser Fehler selbst eliminiert.

Treppenspannungsumsetzung

Im Gegensatz zur vorangehend behandelten Methode der Integration der Eingangsspannung an einem Kondensator steht das Verfahren der Umsetzung durch Vergleich mit einer Treppenspannung. Bei dieser Art der Datenwandlung wird zu Beginn der integrierte Zähler auf Null gesetzt, um dann mit dem Systemtakt hochzuzählen. Der integrierte Digital-Analog-Umsetzer wandelt den Zählerzustand sofort zurück. Das Ergebnis dieser Rückwandlung ist das typische »Treppensignal« (Bild 6). Die Treppenspannung wird laufend mit dem Eingangssignal verglichen. Ist die Differenz weniger als ± ½ LSB, so stoppt der Komparator den Vorgang und das Ergebnis kann vom Zähler in das Ausgangsregister übernommen werden. Diese Stufenumsetzung (Bild 7) wird im allgemeinen nur für eine Auflösung bis zu 10 Bit eingesetzt. Die Gründe für diese Einschränkungen sind

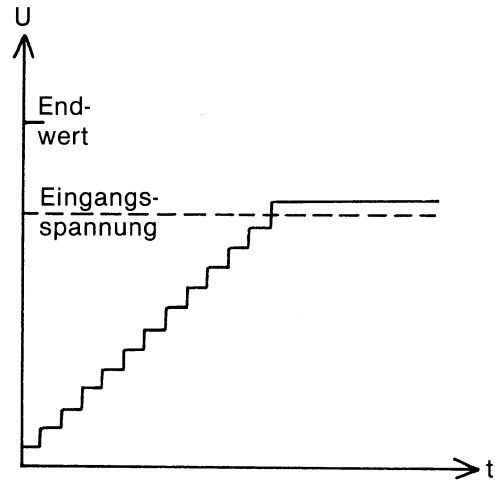

Bild 6: Typisches Treppensignal am Digital-Analog-Umsetzer-Ausgang eines Zählconverters

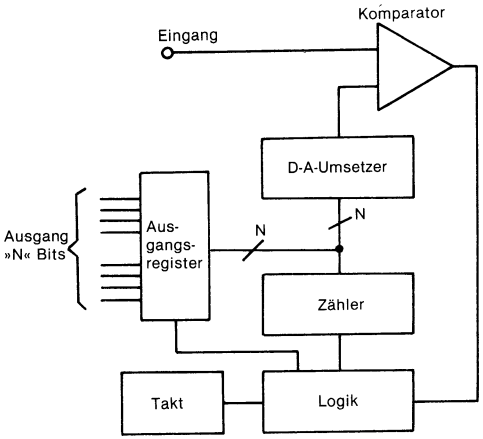

Bild 7: Blockschaltbild eines Stufenumsetzers

vielfacher Art: Der erforderliche D-A-Teil läßt sich bei höherer Auflösung nur relativ schwer integrieren. Hochauflösende DAUs haben meist auch den Nachteil, daß sie relativ langsam sind, das heißt eine lange Einschwingzeit benötigen. Die Umsetzzeit ist extrem lang. Der Zähler muß jeden einzelnen Schritt durchlaufen. Damit muß der Digital-Analog-Wandler ebenso jeden Punkt konvertieren und der Ausgang auf den exakten Pegel einschwingen, um dann im Komparator verglichen zu werden. Dieser notwendige Vorgang verlangsamt eine hochauflösende Wandlung.

Die Kombination eines Zählers und eines D-A-Wandlers mit einigen zusätzlichen Elementen kann jedoch auch sehr sinnvoll ausgenutzt werden. Bild 8 zeigt das Blockschaltbild eines handelsüblichen Converters (ZN 435 von Ferranti) auf der Basis des beschriebenen Verfahrens: Um einen kompletten ADU aufzubauen, sind hier noch der erforderliche Takt und ein Komparator für den Vergleich der rückgewandelten Spannung mit der Eingangsspannung vorzusehen (Bild 9). Bei diesem Bausteins besteht jedoch die Möglichkeit, über den Anschluß »Logic Select« die Ausgänge des Zählers vom D-A-Teil abzutrennen. Damit werden die vorher als Ausgänge betrachteten Anschlüsse zu Eingängen umgeschaltet und aus dem A-D- wird ohne zusätzliche externe Beschaltung ein D-A-Baustein (Bild 10). Ebenso einfach lassen sich damit Wellenformen generieren. Die Synthese einer Sägezahnspannung ist mit dieser Anordnung von Zähler und DAU

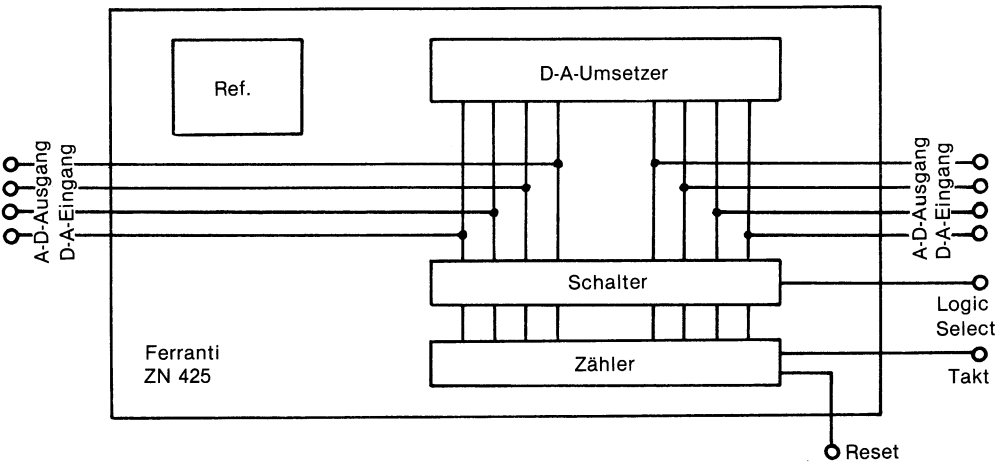

Bild 8: AD-DA-Kombinationsbaustein (Zählverfahren)

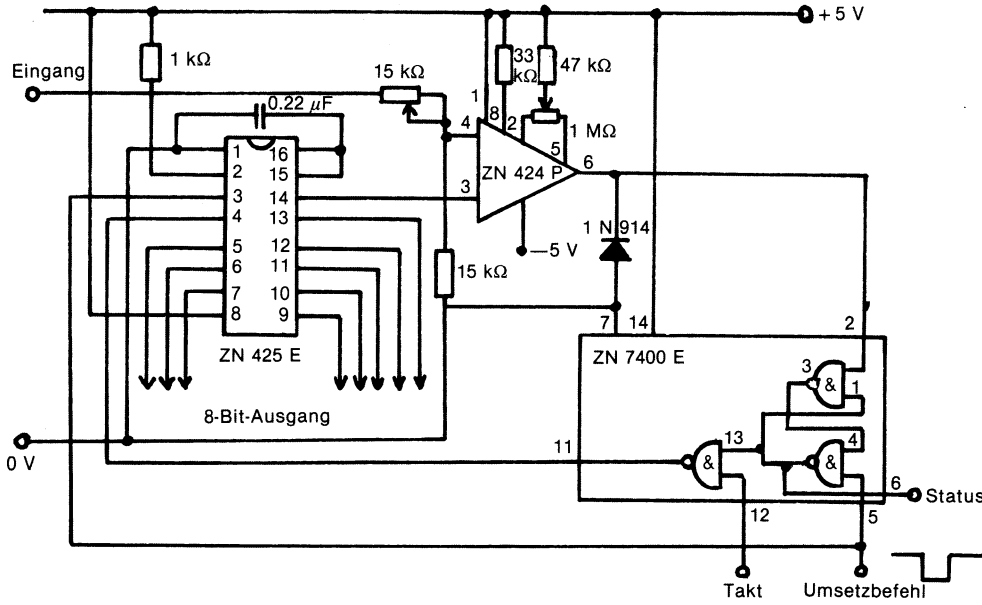

Bild 9: A-D-Umsetzer nach dem Stufenumsetzungsverfahren

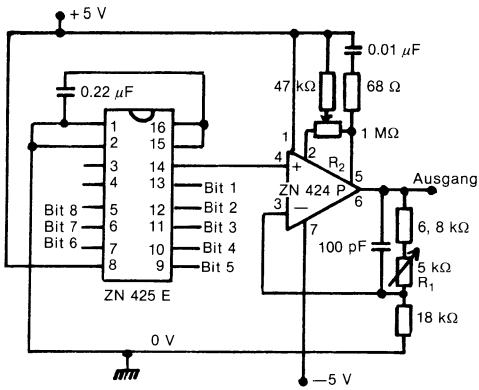

Bild 10: Ausnutzung des D-A-Teils im Stufenumsetzer

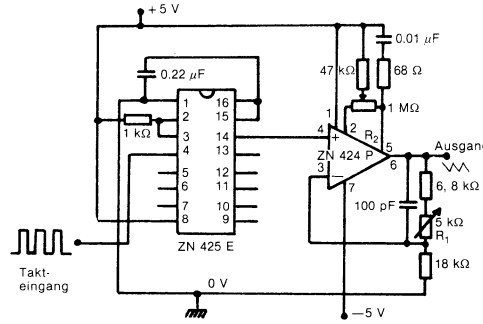

Bild 11: Erzeugung einer Sägezahnspannung mit einem Stufenumsetzer

vorprogrammiert und der Baustein ermöglicht über weitere Zugriffe auf den integrierten Auf/Abwärtszähler eine zusätzliche Auswahl an generierbaren Wellenformen (Bild 11).

Eine weitere Version dieses Prinzips ist der sogenannte Tracking-Converter, in der deutschen Literatur meist als »Nachlauf- oder Kompensationsverfahren« bezeichnet. Bild 12 zeigt das Prinzipschaltbild die-

ser Anordnung. Ein integrierter Auf/Abwärtszähler wird anstatt durch einen normalen Vergleicher durch einen Fensterkomparator angesteuert. Wird nun der Systemtakt fortwährend angelegt, so läuft das digitale Ergebnis kontinuierlich dem angelegten Eingangssignal nach bzw. kompensiert das im DAU rückgewandelte Digitalsignal. Das Verfahren läßt sich mit einem wegoptimierten Schnelldrucker vergleichen, der nicht mehr grundsätzlich vom linken Zeilenrand beginnt, sondern den minimalsten Schritt zur neuen Zeile macht.

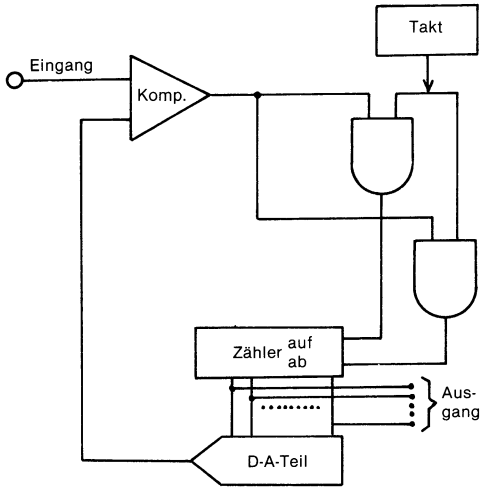

Bild 12: Blockschaltbild des Tracking-Converters (Nachlaufverfahren)

Alle A-D-Wandler kranken im Prinzip an der Erfordernis der Rücksetzung auf Null und der danach notwendigen Annäherung. Bewegt sich das Meßsignal aber immer nahe um den Wert während der vorhergehenden Umsetzung, so ist dieser erforderliche Zyklus zeitraubend und unnötig. Der »Tracking-Converter« vermeidet diesen Nachteil und ermöglicht schnelle Umsetzraten — aber nur solange die Differenz zwischen altem und neuem Meßwert nur geringfügig ist.

Eine weitere Wandlungsart ist der sogenannte »Discretionary Converter«. Hierbei handelt es sich um eine Kombination aus Zählverfahren und sukzessiver Approximation. Aufgebaut wie ein normaler Zähl-ADU besitzt dieser Wandlertyp noch einen weiteren Komparator. Dieser vergleicht laufend das Eingangssignal mit dem bereits erreichten (rückgewandelten) Digitalwert. Liegt die Differenz über einem bestimmten Wert, so wird der interne Zähler nicht auf den Bereich der niederwertigen Bits, sondern in einen wesentlich höheren Bereich gesetzt (Bild 13). Damit nähert er sich dem Endwert wesentlich schneller — ein großer Nachteil des Zählverfahrens wird damit ausgeschaltet. Mit dieser Anordnung lassen sich Umsetzzeiten von ca. 50 μs bei 10 Bit Auflösung erreichen.

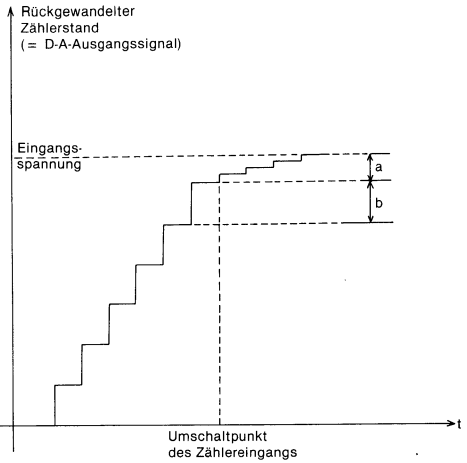

Bild 13: D-A-Ausgangssignal eines »Discretionary«-A-D-Wandlers

Sukzessive Approximation

Die in der deutschen Nomenklatur als »Wägeverfahren« bezeichnete Umsetzmethode ist zur Zeit Standard im Bereich mittelschneller bis schneller Wandler. Die da-

bei angewandte Technik lehnt sich an das vorab beschriebene »Discretionary«-Verfahren an. Das Prinzip beruht auf einer schrittweisen Annäherung des rückgewandelten Digitalwertes an die Eingangsspannung. Die verwendete Schrittweite ist variabel — sie wird von Stufe zu Stufe um die Hälfte verringert. Der erste Puls des erforderlichen Taktsignales setzt alle internen Register auf Null. Mit dem zweiten Puls wird das höchstwertige Bit (MSB) gesetzt, um rückgewandelt mit dem Eingangssignal verglichen zu werden. Je nach dem Ergebnis dieser Operation erfolgt eine Rücksetzung oder ein neuerliches Setzen des darauffolgenden Bits. Dieser Vorgang wiederholt sich, bis alle vorhandenen Register durchgelaufen sind und das Ergebnis in den Ausgangsspeicher übertragen wird. Typische Ausführungsformen benötigen für die interne Verwaltung des Converters ein bis zwei Pulse zusätzlich zu der Anzahl der für die Messungen erforderlichen. (Bei einer Auflösung von N Bit sind N + 2 Pulse erforderlich). Durch die minimierte Anzahl von erforderlichen Schritten zeigt sich diese Umsetzmethode dem normalen Zählverfahren um ungefähr zwei Größenordnungen in der Geschwindigkeit überlegen. Bild 14 zeigt die Prinzipschaltung, und Bild 15 und 16 verdeutlichen die variable Schrittweite beim Herantasten an das Meßsignal.

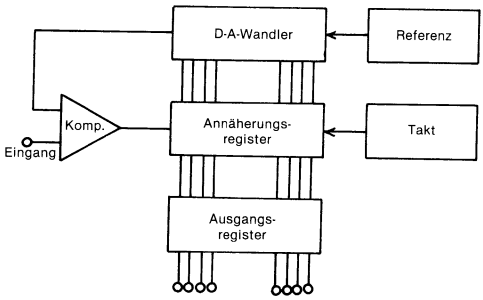

Bild 14: Blockschaltbild eines A-D-Wandlers nach dem Verfahren der sukzessiven Approximation

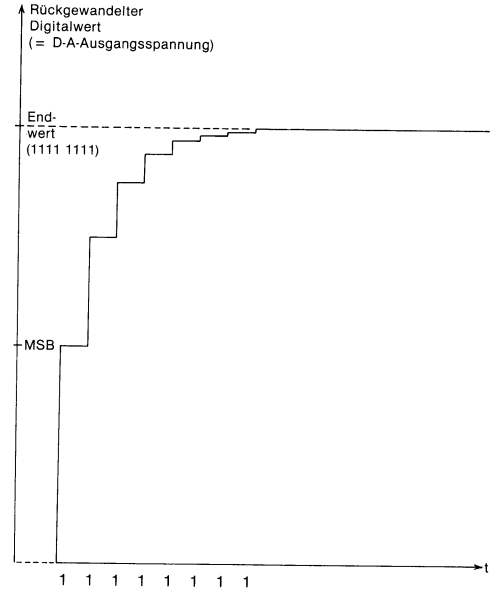

Bild 15: 8-Bit-ADU (sukzessive Approximation): Darstellung des Annäherungsverfahrens zur Erreichung des Endwertes »1111 1111«

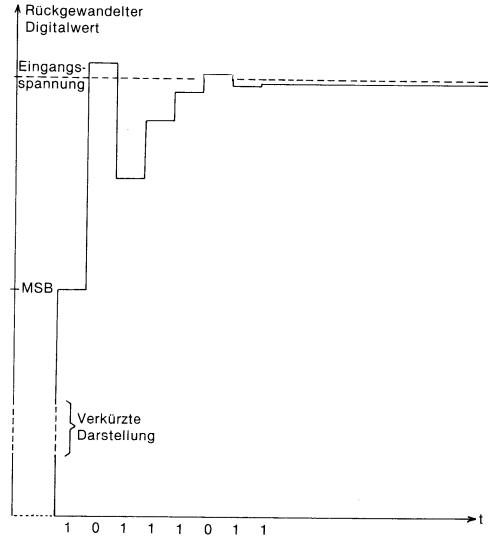

Bild 16: 8-Bit-ADU (sukzessive Approximation): Annäherung an das Ergebniswort »1011 1011« (erforderliche Rücksetzung zweier Bits während der Approximationsphase)

Die erzielbare Auflösung ist relativ hoch; der erforderliche D-A-Umsetzer limitiert jedoch wie beim Treppenspannungsumsetzer die mögliche Auflösung (speziell bei monolithischen Bausteinen). Auch die Geschwindigkeitsanforderung an den D-A-Teil wird relativ hoch, da sich dessen Ausgang bei jeder Stufe auf ± ½ LSB einschwingen muß. (Der Wert ± ½ LSB bezieht sich hier auf die Gesamtauflösung des Wandlers, nicht auf den Wert der jeweiligen Stufe).

Ganz im Gegensatz zum Dual-Slope-Umsetzer erfordert das Verfahren der sukzessiven Approximation einen Abtast- und Haltekreis am Eingang. Dieser ist unbedingt nötig, sofern nicht sichergestellt werden kann, daß sich das Eingangssignal während der Konversion nur unwesentlich ändert. Genaugenommen darf sich das umzusetzende Signal nur um weniger als den einem halben LSB entsprechenden Spannungswert ändern. Ein Nichtbeachten dieser Forderung kann je nach dem jeweiligen Zusammentreffen von Approximationsschritt und Eingangsspannungsänderung ein falsches Ergebnis verursachen.

Parallelverfahren

Die wohl eleganteste, vom theoretischen Prinzip her einfachste, aber auch technisch aufwendigste Bauform eines A-D-Umsetzers ist das Parallelverfahren. Der Grundgedanke ist einfach: Der zu messende Eingangsspannungsbereich wird in 2^N (N = Auflösung des ADU) einzelne Spannungsschritte aufgeteilt. Mittels einer möglichst präzisen Widerstandskette, gespeist durch eine Referenzspannung, werden alle diese möglichen Spannungsschritte erzeugt. Eine Anzahl von 2^N-1-Komparatoren vergleichen nun diese erzeugten diskreten Spannungen mit dem tatsächlichen Eingangssignal. Die Komparatoren sind mit ihrem zweiten Anschluß jeweils kurzgeschlossen. In Bild 17 ist das Prinzipschaltbild anhand einer vereinfachten Darstellung eines 3-Bit-Umsetzers dargestellt.

Wird auf den »Strobe«-Eingang dieser Komparatoren die erforderliche Flanke angelegt, so vergleicht jeder für sich, ob das ihm zugeführte Eingangssignal größer oder kleiner als der anliegende Referenzwert ist. Aufgrund der sofortigen Umsetzung benötigt der Parallel-Wandler keinen Abtast- und Haltekreis. Die Ausgänge stellen dann eine Art »Thermometercode« dar, d.h. alle Vergleicher, deren Referenzsignal kleiner als die angelegte Eingangsspannung ist, erzeugen am Ausgang beispielsweise eine logische Eins. Darüber stehen dann nur logische Nullen. Die angeschlossene Logik hat die Aufgabe, die vorhandenen 2^N-1 einzelnen Werte in die binär codierte Form »N« zurückzuführen. Die dabei angewandten Verfahren sind je nach geforderter Auflösung teilweise recht unterschiedlich und reichen von der direkten Umsetzung per Gatterlogik bis zur ROM-Tabelle.

Um den Datendurchsatz zu erhöhen, wird üblicherweise ein Ausgangsregister benutzt. Dieses Register ist mit dem »Strobe«-Eingang verbunden und speichert das jeweils vorhergehende Umsetzergebnis, während das nachfolgende bereits über die Komparatoren und über die — relativ langsame — Umsetzlogik läuft. Diese im englischen Sprachgebrauch als »one pipeline delay« bezeichnete zeitliche Verschiebung zwischen Takt und Ergebnis tritt aber in den meisten Fällen nicht in Erscheinung. Der Großteil aller Geräte, die so schnelle Wandler benötigen (Umsetzraten von 10 MHz bis 100 MHz), besitzt meist einen zentralen Takt, um den das ganze Sy-

stem leicht verzögert werden kann. Dabei ist nicht die tatsächliche Umsetzzeit von Puls auf Ergebnis wichtig, sondern die erzielbare Durchsetzrate, um laufende schnelle Vorgänge zu digitalisieren. Typische Applikationen für solche schnellen A-D-Wandler sind Videosysteme und Transientenrecorder.

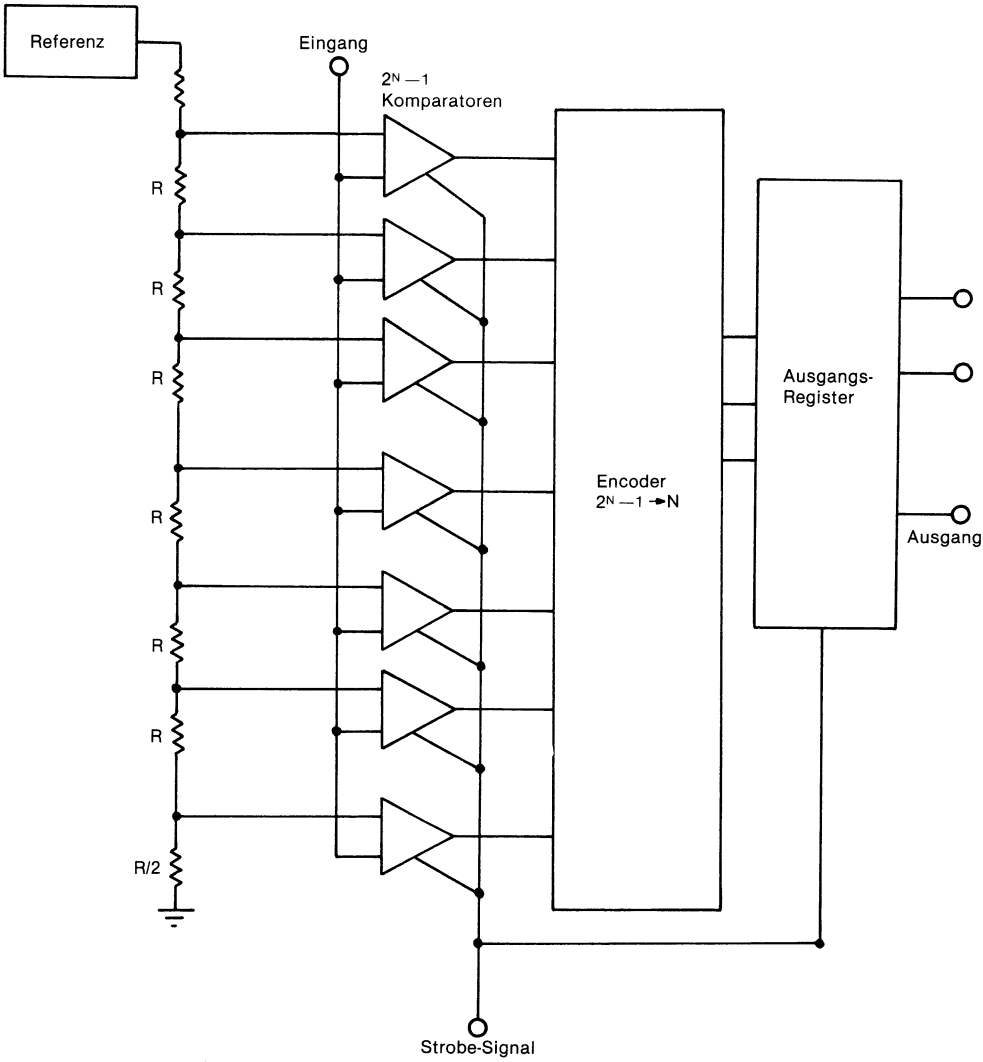

Bild 17: Blockschaltbild eines 3-Bit-Parallel-Umsetzers

Analoges Ein-/Ausgabesystem für den μP 6800

Analoges Ein-/Ausgabesystem für den µP 6800

Scott Bird, Ferranti Electronics Ltd., England

Analoge Ein-/Ausgabesysteme müssen nicht teuer und in ihrer Anwendungsvielfalt beschränkt sein. Dieser Bericht zeigt eine interessante Lösung für den µP 6800

Konventionelle, analoge Ein-/Ausgabesysteme für Mikroprozessoren sind sehr genau und daher teuer, und hybride Moduln bzw. Printplattenaufbauten sind mit einer fest vorgegebenen Anzahl von Ein-/Ausgabekanälen (z.B. 16 Eingangs- und 2 Ausgangskanäle) erhältlich. In dem vorliegenden Applikationsbericht wird geschildert, wie ein preiswertes, analoges Ein-/Ausgabesystem für den Mikroprozessor 6800 gebaut werden kann, wenn man die Bausteine ZN427 (Analog/Digital-Wandler), ZN428 (Digital/Analog-Wandler) von Ferranti und 6820/6821 (PIA = Peripheral Interface Adapter) benutzt. Mit diesen Bausteinen läßt sich ein leistungsfähiges System entwerfen, das speziellen Ein-/Ausgabeanforderungen angeglichen werden kann. Das System läßt sich, ohne wesentliche Änderungen der Hardware, auch erweitern. Der Vorteil, einen Mikroprozessor über einen peripheren Interface-Adapter (PIA) zu verbinden, liegt darin, daß ein einfaches, leicht zu erweiterndes System ohne zusätzliche Adressenkodierung und Pufferhardware für die Zuleitungen geschaffen wird. Außerdem werden zeitliche Probleme, die bei einem direkten Bus-Interface auftreten, hier vereinfacht.

Der A/D-Wandler ZN427

Der Baustein ZN427 (Bild 1) ist ein 8-bit-A/D-Wandler (ADW), der nach dem Verfahren der sukzessiven Approximation arbeitet. (Das Logikdiagramm zeigt Bild 2.) Er hat eine Umwandlungszeit von 15 µs und „3-State"-Ausgänge, um mit üblichen Datenleitungen eine direkte Verbindung herstellen zu können. Außerdem zeigt er keine Kodierungsfehler über den gesamten Betriebstemperaturbereich. Der Baustein ZN427 enthält einen spannungsabhängigen Digital/Analog-Wandler (DAW), eine genaue Spannungsreferenz mit 2,5 V Bandabstand, einen schnellen Komparator, die Logik für die sukzessive Approximation und „3-State"-Ausgabepuffer.

Die Wirkungsweise des Bausteins ZN427 wird verdeutlicht, wenn man das Zeitdiagramm (Bild 3) ansieht. Die Umwandlung wird durch einen SC-Impuls (Start Convert) eingeleitet. Dieser Impuls kann — bezogen auf die Taktimpulse des Bausteines ZN427 — asynchron erfolgen, wenn folgende Kriterien berücksichtigt werden:

1. Die ansteigende Flanke des SC-Impulses sollte vor der ersten (abfallenden) aktiven Flanke des Taktimpulses mindestens einen Abstand von 15 µs haben, damit das höchstwertige Bit gesetzt werden kann.

2. Die abfallende Flanke eines SC-Impulses darf nicht innerhalb ± 200 ns der abfallenden Flanke des Taktimpulses auftreten.

3. Als Sonderfall der Bedingungen (1) und (2) kann der SC-Impuls mit der abfallenden Flanke des Taktimpulses zusammenfallen oder auch von gleicher Dauer sein. Bei Auftreten eines SC-Impulses wird in das höchstwertige Bit (MSB = Most Significant Bit) der Wert „1" eingeschrieben. Alle andere Bits haben den Wert „0". Am Ausgang des D/A-Wandlers liegt dann die halbe Referenzspannung $U_{REF\ EIN}$ an.

Dieser Wert wird mit der Eingangsspannung U_{EIN} verglichen. Eine Abfrage erfolgt bei der abfallenden Flanke eines Taktimpulses. Ist $U_{REF\ EIN}/2 > U_{EIN}$, wird in das MSB der Wert „0" eingeschrieben. Bei $U_{REF\ EIN}/2 < U_{EIN}$ bleibt der Wert des MSB „1". Gleichzeitig wird in Bit 2 der Wert „1" eingeschrieben; eine Abfrage erfolgt dann bei der nachfolgenden, abfallenden Taktflanke, indem man den Ausgang des DAW wieder mit U_{EIN} vergleicht. Der gleiche Vorgang wird für alle acht Bits wiederholt. Dadurch liegt am Digitalausgang des Wandlers dann der digitalisierte Wert von U_{EIN} an, wenn der EOC-Eingang (EOC = End of Conversion) den Wert „1" annimmt. Der Digitalwert liegt bis zum nächsten Start-Impuls vor. Die „3-State"-Dateneingänge befinden sich im AUS-Zustand (hohe Impedanz), wenn der OE-Eingang (Output Enable = Freigabe des Ausganges) ein L-Signal hat. Die Datenausgänge werden freigegeben, wenn der OE-Eingang H-Signal enthält.

Der D/A-Wandler ZN428

Der Baustein ZN428 ist ein monolithischer 8-bit-D/A-Wandler mit statischen Speichern am Eingang, um den Empfang der vom Datenbus kommenden Daten sicherzustellen. Der statische Speicher wird freigegeben, wenn am FREIGABE-Eingang ein „L"-Signal anliegt. Die Daten werden gespeichert, wenn an FREIGABE ein „H"-Signal anliegt. Der Baustein ZN428 benötigt eine Versorgungsspannung von + 5 V, hat eine Ausregelzeit von 800 ns und ist garantiert monoton über den gesamten Arbeitsbereich. Er enthält eine 2,5-V-Referenzspannungsquelle, die jedoch durch äußere Beschaltung umgangen werden kann; d.h., man kann auch eine externe Referenzspannungsquelle benutzen. Der DAW ist vom spannungsschaltenden Typ und verwendet ein R-2R-Widerstandsnetzwerk. Jedes 2R-Element wird über Transistorschalter mit 0 V oder $U_{REF\ EIN}$ verbunden. Hierdurch wird die Offsetspannung besonders klein gehalten (1 mV). Am Ausgang des R-2R-Widerstandsnetzwerkes steht eine binär gewichtete Spannung. Die Nennausgangsspannung liegt beim Baustein ZN428, über einen 4-kΩ-Widerstand, zwischen 0 V und $U_{REF\ EIN}$. Durch Benutzung eines externen Verstärkers können auch andere Spannungsdifferenzen eingestellt werden.

Das Mikroprozessor-System 6800

Es wird davon ausgegangen, daß der Leser die Mikroprozessor-Familie 6800 kennt. Eingehende Informationen können u.a.

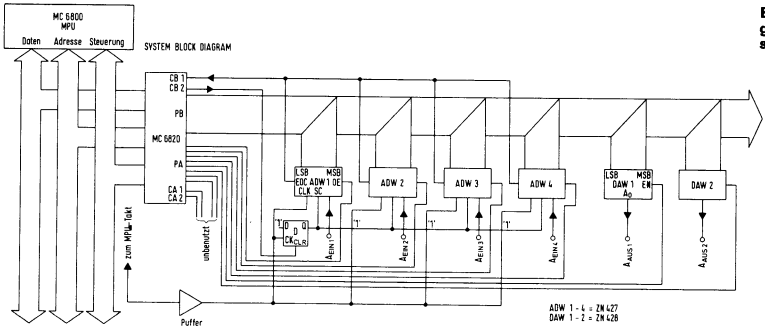

Bild 1: Blockdiagramm des Systems

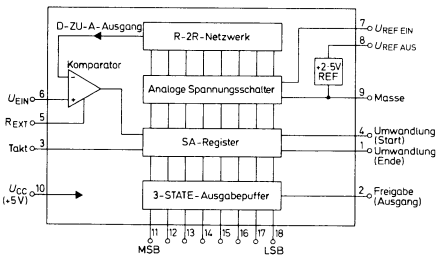

Bild 2: Logikdiagramm des Bausteines ZN427

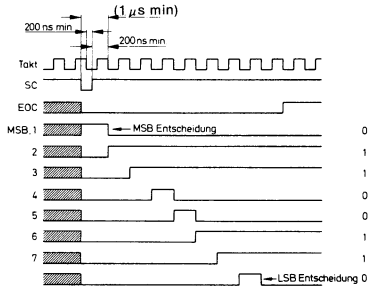

Bild 3: Zeitablaufdiagramm

dem Buch „Microprocessor Applications Manual", McGrawhill, 1975, entnommen werden. Deshalb wird hier nur ein kurzer Überblick über das System gegeben.

Der Baustein 6800 ist ein monolithischer 8-bit-Mikroprozessor, der das „Herz" der 6800-Mikroprozessor-Familie ist. Er ist voll TTL-kompatibel und benötigt eine Versorgungsspannung von nur +5 V. Der Befehlssatz umfaßt 72 Befehle mit sieben Adressierungsarten; es lassen sich externe Speicher mit einer maximalen Kapazität von 65 KBytes anwählen. Die Kommunikation mit dem externen Speicher und allen Ein-/Ausgabeeinheiten erfolgt über einen bidirektionalen 8-bit-Datenbus und einen 16-bit-Adressenbus.

Der PIA6820/21 erlaubt über zwei bidirektionale, periphere 8-bit-Datenleitungen und vier Steuerleitungen die Verbindung von byteorientierten, peripheren Einheiten mit dem Mikroprozessor. Die Funktion des PIA wird vom Mikroprozessor gesteuert. Jede der peripheren Datenleitungen kann so programmiert werden, daß sie als Eingang oder Ausgang wirkt. Jede der vier Steuer-/Interrupt-Leitungen läßt sich für einen der sieben möglichen Steuerarten programmieren. Hierdurch wird die Arbeitsweise des Interface äußerst flexibel gehalten.

Das analoge Ein-/Ausgabe-Interface

Das in diesem Applikationsbericht beschriebene System hat vier analoge Eingangs- und zwei analoge Ausgangskanäle (siehe auch Bilder 1 und 5). Andere Anordnungen können — wie weiter unten beschrieben — sehr einfach realisiert werden.
Die peripheren Datenleitungen PB0 bis PB7 des PIA lassen sich mit den binären Datenausgängen der Bausteine ZN427 und den Dateneingängen der Bausteine ZN428 verbinden, um einen 8-bit-Datenbus für die Wandler zu erzeugen. Die peripheren Leitungen PA0 bis PA5 werden als Ausgänge programmiert. Sie erzeugen einzelne Ausgabefreigaben und FREIGABE-Signale für die Bausteine ZN427 bzw. ZN428. Ein gleichzeitiges Startsignal zur Umwandlung wird für den Baustein ZN427 von der Steuerleitung CB2 erzeugt, die in der „SET/RESET"-Betriebsart programmiert wurde und in Verbindung mit einem D-Flipflop benutzt wird. Die EOC-Ausgänge des Bausteines ZN427 sind zusammengeschaltet und treiben den CB1-Eingang des PIA an, der so programmiert werden kann, daß im Mikroprozessor ein Interrupt-Signal erzeugt wird. Bei dieser Konfiguration werden die peripheren Leitungen PA6, PA7 und die Steuerleitungen CA1 und CA2 nicht benutzt.
Das Taktsignal für den Baustein ZN427 kann entweder asynchron von einem externen Taktgenerator oder vom Takt des Mikroprozessors erzeugt werden. Benutzt man die Takteinheit MC6871B des Mikroprozessors — sie ist in dem Baukastensystem MEK6800D2 vorhanden —, wird ein Taktsignal von 614,4 kHz erzeugt, und es läßt sich der Ø 2 TTL-Ausgang unmittelbar verwenden. Es sei angemerkt, daß für den Baustein ZN427 die maximale Taktfrequenz von 600 kHz angegeben ist. Sie läßt sich — jedoch auf Kosten der Genauigkeit in der Ansprechzeit des Komparators — auf bis zu 1 MHz anheben. Benutzt man deshalb einen Mikroprozessor mit einer größeren Taktfrequenz als 600 kHz, teilt man die Taktfrequenz auf kleiner 600 kHz herunter oder man betreibt den Baustein auf Kosten der Genauigkeit mit 1 MHz. Der Vorteil bei Verwendung des Mikroprozessortaktes gegenüber einem externen Takt liegt darin, daß über die Taktzyklen des Mikroprozessors genaue Berechnungen hinsichtlich der Umsetzzeit vorgenom-

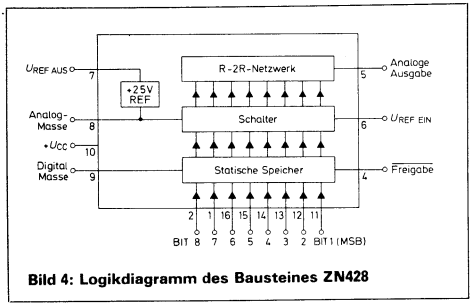

Bild 4: Logikdiagramm des Bausteines ZN428

men werden können; Mikroprozessor-Interrupts werden dann nicht benötigt.
Um die oben besprochenen Zeitbedingungen einzuhalten, wird der Startimpuls zur Umwandlung von einem D-Flipflop (1/2 ZN74L74) erzeugt. Ein Umwandlungszyklus wird eingeleitet, indem man auf der CB2-Leitung des PIA vom L- in den H-Zustand übergeht. Der Ausgang der CB2-Leitung steuert den Rücksetzeingang des D-Flipflops an und setzt den SC-Eingang (Start Convert) eines jeden Bausteines ZN427 über den Q-Ausgang auf L-Pegel. Die erste ansteigende Taktflanke, die auftritt, wenn der Rücksetzeingang wieder H-Pegel hat, taktet das D-Flipflop, wodurch dem SC-Eingang jedes Bausteines ZN427 ein H-Signal zugeführt wird; der Umwandlungszyklus kann nun ablaufen. Ist der SC-Eingang des Bausteines ZN427 auf L-Pegel, liegt am MSB-Ausgang „H"-Signal an. Alle anderen Datenausgänge tragen „L"-Signal; der Umwandlungszyklus wird beibehalten. Bei der neunten abfallenden Taktflanke nach dem Startimpuls gehen die EOC-Ausgänge in den H-Zustand über, wodurch das Ende des Umwandlungszyklus angezeigt wird. Dies kann erkannt werden, indem man den PIA so programmiert, daß der Eingang des Mikroprozessor-Interrupts bei der ansteigenden Flanke der CB1-Steuerleitung gesetzt wird. Um eine gemeinsame Interrupt-Leitung zu bilden, können die EOC-Ausgänge von bis zu vier ZN427-Bausteinen über „WIRED-OR" verknüpft werden (Bild 5). Verwendet man alternativ einen Mikroprozessortakt (bis zu 1 MHz), tritt ein Signal am EOC-Ausgang immer innerhalb von 10 Maschinenzyklen des Mikroprozessors auf, nachdem der Befehl die CB2-Steuerleitung auf H-Pegel gesetzt hat. Deshalb kann eine geeignete, feste Verzögerung, die die Umwandlungszeit berücksichtigt, in das Programm eingebaut werden.

Die binären Ausgangsdaten jedes ADW lassen sich lesen, indem man die peripheren Leitungen PB0 bis PB7 als Eingänge programmiert und die Daten auf dem Wandlerbus durch Setzen der zugehörigen peripheren PA-Leitung in den H-Zustand bringt. Hierdurch werden die „3-State"-Ausgabepuffer freigegeben. Ein Lesebefehl des peripheren PIA-Registers „B" überträgt dann die Daten in den Mikroprozessor. Natürlich sollte das Programm so angeordnet sein, daß — zur Vermeidung von Unklarheiten — zu einer bestimmten Zeit nur ein ADW freigegeben ist.
Das Schaltdiagramm in Bild 5 zeigt eine Zusammenschaltung der Bausteine ZN427 für einen Eingangsspannungsbereich von 0 bis 10 V. Andere Spannungsbereiche, z.B. 5 V, ±10 V und ±5 V sind auch realisierbar, indem man ein einfaches Widerstandsnetzwerk, wie es im Datenblatt des Bausteines ZN427 zu finden ist, verwendet. Die negative Versorgungsspannung von −5 V wird z.B. über einen 82-kΩ-Widerstand erstellt. Bei entsprechender Wahl des Widerstandswertes lassen sich negative Spannungswerte zwischen −3 V und −30 V abgreifen. Bei Anwendungen, in denen nur eine einzige +5-V-Spannungsversorgung zur Verfügung steht, kann eine einfache Diodenpumpschaltung dazu verwendet werden, negative Spannungswerte zu erzeugen. Weitere Informationen über negative Versorgungsspannungen und eine Diodenpumpschaltung für bis zu fünf ZN427-Bausteine sind dem Datenblatt entnehmbar.
Daten werden von dem System ausgegeben, indem man die peripheren Datenleitungen PB0 bis PB7 als Ausgänge programmiert und die binären Daten aus dem Mikroprozessor in das periphere PIA-Register B einschreibt. Der FREIGABE-Eingang des betreffenden Bausteines ZN428 wird auf L-Pegel gelegt und über eine entsprechende PA-Leitung, die die Daten von dem Wandlerbus auf die statischen Eingangsspeicher des Bausteins ZN428 überträgt, wieder auf H-Pegel gebracht. Während der Datenübertragung muß gewährleistet sein, daß alle Bausteine ZN427 und der andere ZN428-Baustein gesperrt sind.
Die analogen Ausgabedaten des Bausteines ZN428 können unmittelbar an den Steckstiften 5 und 8 entnommen werden. Der Ausgangsspannungsbereich wird zwischen 0 V und $U_{REF\ EIN}$ über einen 4-kΩ-Ausgangswiderstand erzeugt. Ein kleiner Kondensator kann zur Vermeidung auftretender Störspitzen zwischen die Ausgabeanschlüsse gelegt werden, wobei der Kapazitätswert des Kondensators von dem Rauschen des Systems und der geforderten Ansprechzeit abhängt. Der Kapazitätswert für eine minimal gewählte Ausregelzeit sollte nicht größer als 100 pF sein. Auf einen Pufferverstärker am Ausgang des Bausteines ZN428 wurde bewußt verzichtet, damit optimale Ausregelzeit und Flexibilität sowie niedrigste Kosten gewährleistet sind. Sowohl unipolare wie bipolare Ausgangsspannungsbereiche können durch einen externen Verstärker

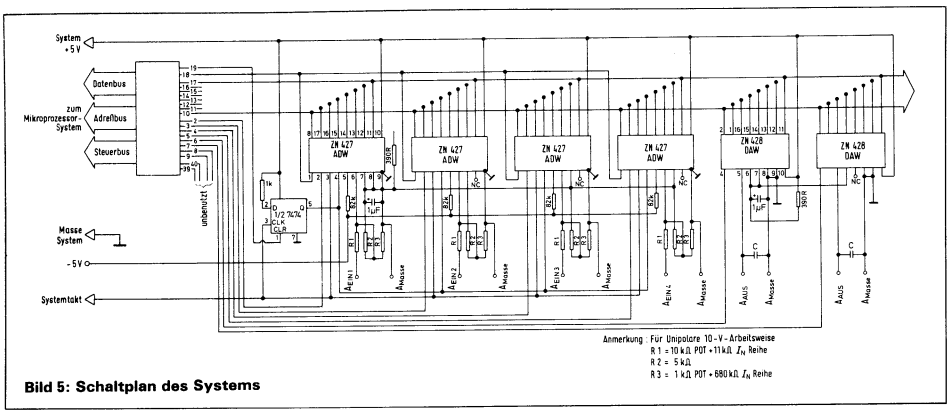

Bild 5: Schaltplan des Systems

Tafel 1:

MC 6820	PA 0–PA 7/CA 2	PB 0–PB 7/CB 2	CA 1/CB 1
I_{IL} I_{IH}	−1,6 mA max −100 µA min	10 µA max	2,5 µA max (bei μ_{EIN} = 0 bis 5,25 V)
I_{OL} I_{OH}	1,6 mA min −100 µA min	1,6 mA min −100 µA min	
MC 6821			
I_{IL} I_{IH}	−2,4 mA max −200 µA min	10 µA max	2,5 µA max (bei μ_{EIN} = 0,5 bis 5,25 V)
I_{OL} I_{OH}	3,2 mA min −200 µA min	3,2 mA min −200 µA min	
ZN 427			
I_{IL} I_{IH} $I_{IH\ (Takt)}$ I_{OL} I_{OH} I_{OHX} Aus-Zustands-Leckstrom	−5 µA max 15 µA max 30 µA max 1,6 mA min −100 µA min 2 µA max		
ZN 428	Alle Eingänge		
I_{IL} I_{IH}	−5 µA max 20 µA max		

Anm.: Die Ströme beziehen sich, wenn nicht anders angegeben, auf 0,4 V und 2,4 V.

mit der Basisadresse des PIA geladen, damit die indizierte Adressierungsbetriebsart zur Adressierung des PIA während des gesamten Programmablaufes benutzt werden kann. Die peripheren Leitungen PA0 bis PA7 werden als Ausgänge programmiert. Das Steuerregister wird gesetzt, so daß die Steuerleitung CB2 in der SET/RESET-Ausgabebetriebsart arbeitet.

Das Interrupt-Flagbit CRB-7 wird bei ansteigender Flanke auf der Steuerleitung CB1 gesetzt, und alle Wandler werden gesperrt, indem auf der PA-Leitung 3mal H-Signal ausgegeben wird. Gleichzeitig erscheinen an den „Ausgabe-/Freigabe"-Eingängen der Bausteine ZN427 L-Signale und an den FREIGABE-Eingängen der Bausteine ZN428 H-Signale. Durch ein „Dummy"-Lesen des Datenregisters B wird das Interrupt-Flagbit CRB-7 gelöscht.

Anschließend läuft ein Startsignal über die Steuerleitung CB2, indem Bit CRB-3 im Steuerregister B einen anderen Wert erhält. Das Ende des Umwandlungszyklus läßt sich durch Abfrage des Interrupt-Flagbits CRB-7 erkennen. Hierbei wird eine Programmschleife durchlaufen, bis das Bit in den „1"-Zustand übergeht. (Anmerkung: Die Interrupt-Leitungen IRQA und IRQB des Mikroprozessors sind gesperrt.) Die Ausgabe von ADW1 wird nun gelesen, indem der peripheren PA0-Leitung ein H-Signal zugeführt wird. Die vom ADW1 kommenden Daten sind im Akkumulator B des Mikroprozessors abgespeichert. ADW2 wird in ähnlicher Weise gelesen, indem die PA1-Leitung ein H-Signal erhält. Die von ADW2 kommenden Daten befinden sich im Akkumulator A. Der Mittelwert ergibt sich durch Addition der Akkumulatorinhalte und anschließendes Rechtsverschieben um 1 bit (entspricht der Division durch 2). Das Ergebnis ist dann in der Speicherstelle „TEMP 1" abgespeichert, und der Ablauf für die Wandler ADW3 und ADW4 wiederholt sich. Die Freigabe der Wandlerausgänge erfolgt durch Belegen der Leitungen PA2 und PA3 mit H-Signalen. Das gemittelte Ergebnis wird in der Speicherstelle „TEMP 2" abgespeichert.

Es folgt nun der Zugriff auf das Datenregister B, und die peripheren Leitungen PB0 bis PB7 werden zu Ausgängen. Die an der Speicherstelle „TEMP 1" befindlichen Daten schiebt man zum Wandlerbus. Der DAW1 wird durch die Pulsfolge H-L-H auf der PA4-Leitung freigegeben, wodurch sich die Binärdaten von dem Bus zu den statischen Eingangsspeichern des DAW und letztlich zum Analogausgang verlagern. Ähnlich ist der Ablauf beim DAW2 mit den Daten aus „TEMP 2", denn man benutzt die PA5-Leitung, um den FREIGABE-Eingang anzusteuern. Das Programm wird mit einem Software-Interrupt (SW1) beendet und die Steuerung wird wieder dem allgemeinen Steuerprogramm übertragen.

Zusammenfassung

Das hier aufgezeigte System ist nicht auf die beschriebene Konfiguration beschränkt. Vorausgesetzt, die Ansteuerungsmöglichkeiten der Systembauteile werden nicht überschritten, ist die Anzahl der verwendbaren Bausteine ZN427/428 nur durch die Anzahl der Ein-/Ausgabeleitungen der PIA beschränkt. Hierdurch erhält der Entwickler sehr viel Freiheit in der Entwicklung des für ihn am besten geeigneten Systems.

Die wesentlichen Last- und Aussteuerungskenndaten der verschiedenen Systemkomponenten sind Tafel 1 zu entnehmen. Puffergatter können verwendet werden, sofern die Aussteuerung von Bauteilen, wie z.B. bei einem langen Bus mit hoher kapazitiver Last, zu erhöhen ist. Man beachte, daß die peripheren Leitungen von Seite B für den Wandlerbus benutzt werden, da sie hohe Impedanz haben, sofern sie als Eingänge programmiert sind. Es wird auch der PIA6821 dem PIA6820 vorgezogen, weil er zwei TTL-Lasten auf den peripheren Leitungen auf sowohl der A- als auch der B-Seite ansteuern kann. Wie weiter oben schon erwähnt, können bis zu vier EOC-Eingänge der Bausteine ZN427 über „WIRED-OR" verbunden werden. Sind mehr als vier „WIRED-OR"-Verknüpfungen vorgesehen, läßt sich jede Gruppe über ein UND-Gatter verbinden, um eine Interruptleitung zu bilden.

Falls erforderlich, sind getrennte Startsignale für jeden Baustein ZN427 generierbar. Dadurch kann der Mikroprozessor einen ADW auslesen, während sich die anderen im Umwandlungszyklus befinden. Diese Konfiguration benötigt aber eine periphere Leitung und ein D-Flipflop pro Startsignalleitung. Soll nur ein Baustein ZN427 oder ZN428 zu irgendeinem Zeitpunkt freigegeben werden, kann man einen oder mehrere integrierte Dekodierer (z.B. ZN74154; 4-aus-16-Demultiplexer/Dekodierer) für die Erweiterung des Systems verwenden. Dieses Bauteil läßt sich mit den vier Dateneingängen verbinden, die bereits mit den vier peripheren PA-Leitungen verbunden sind. Der Freigabeeingang des Dekodierers wird von der CA2-Leitung angesteuert. Durch Verwendung von zwei IC erhält man 32 Ausgabeleitungen, die ein analoges Ein-/Ausgabesystem zulassen, das bis zu 32 analoge Ein-/Ausgabekanäle hat.

Wegen der geringen Wandlerkosten, der geringen Anzahl externer Bauteile und der Flexibilität eines solchen Systems ist die Verwendung eines Wandlers pro Kanal bei Datenerfassungsproblemen mit Mikroprozessoren eine praktikable und preiswerte Lösung. Der hier beschriebene Vorschlag wird viele neue Anwendungen dort finden, wo bisher nur ein einziger, teurer hybrider Analog/Digital-Wandler unter Einsatz von „Sample-and-hold"-Bausteinen und Mehrkanalmultiplexing eingesetzt werden konnte.

Applications of the ZN425 8 bit A-D/D-A Converter

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1. INTRODUCTION

Digital to analogue, (D-A), and analogue to digital, (A-D), conversion is a specialised field of electronics. It is useful to consider first the general principles of such conversion techniques, and definitions commonly used in the general field of A-D and D-A conversion.

The discussion is limited to 8-bit converters of a type similar to the ZN425E, illustrated in Figure 1a.

Digital information, fed in to the converter, normally as parallel bits, generates an analogue output corresponding to the value of the binary coded number entered at the input. Ignoring errors for the moment, and assuming that the analogue output is a voltage, the output can be expressed as:

$$V_{out} = V_{full\ scale} \times \frac{\text{Binary Input}}{\text{Full scale binary input}}$$

which, in the case of the ZN425E, is

$$V_{out} = V_{REF} \times \frac{\text{Binary Input}}{256}$$

The voltage output is obtained using a resistive ladder network shown in Figure 1b. Switches connect resistors within the network either to the reference voltage or to the ground line according to the state of the binary inputs controlling each particular switch.

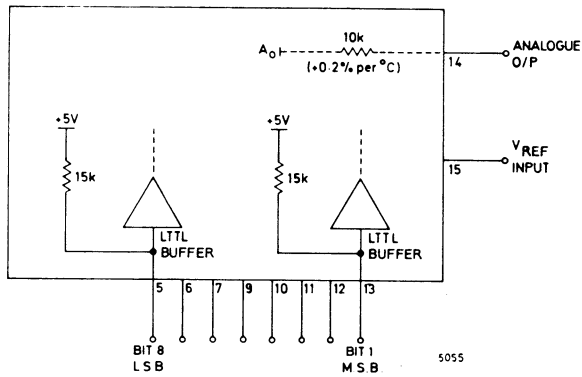


Fig. 1a Basic 8 bit D to A converter

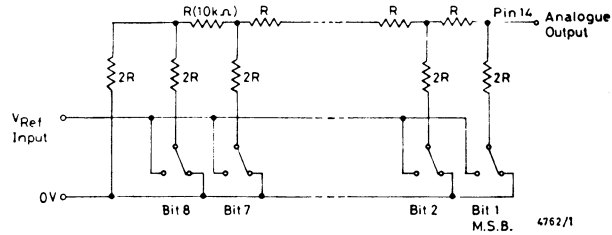


Fig. 1b The R-2R ladder network

The block diagram of the ZN425E circuit is reproduced in Figure 2.

The integrated circuit is fully monolithic, It contains a resistive ladder network, a logic input select switch, voltage switches, an internal reference and a counter. The D-A reference may be connected to the internally generated reference or to an external reference voltage. The inclusion of a counter within the circuit considerably extends its application. A 'staircase' waveform can be very simply generated at the analogue output by feeding a train of clock pulses into the counter.

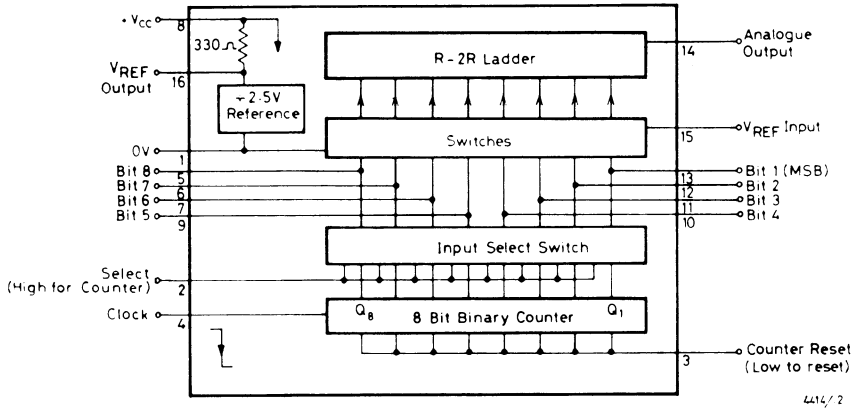


Fig. 2 Block diagram of ZN425E

The ZN425E system operation is outlined in Figure 3. The counter may be clocked by negative going inputs and reset by applying a '0' level to the reset pin.

The digital inputs to the converter may be obtained either from an external source when the 'logic select' pin is at logical '0' ,or from the counter when it is set to logical '1'. In the latter case the state of the counter appears at the digital input terminals as '0' or '1' levels on open collectors with 15 kΩ pull up resistors. In the D-A mode the digital input terminals may be considered as low power TTL inputs.

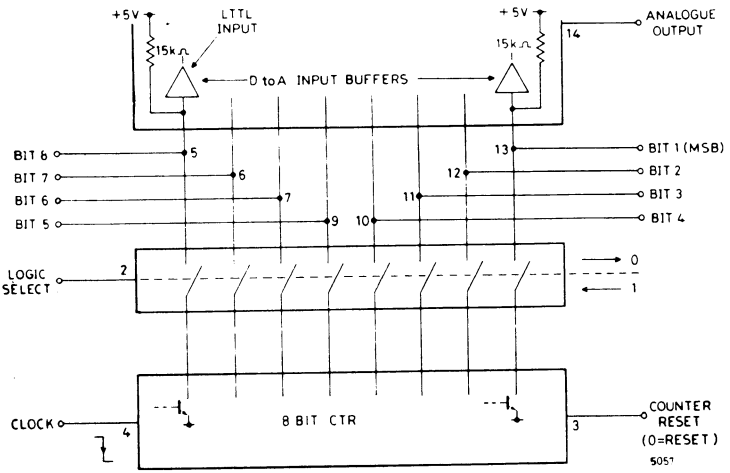


Fig. 3 Outline ZN425E operation

1.1 Definitions

Various terms commonly used when discussing D-A and A-D converter operation are defined below.

Resolution

The resolution is determined by the number of digital inputs, i.e. an 8 bit DAC, (digital to analogue converter), is said to have 8 bit resolution. No particular level of accuracy is implied.

Staircase/Ramp

As the binary code is increased step by step, the analogue output also increases in discrete steps. If the input code increases at a constant rate the resulting output will be a staircase

Since the number of discrete steps is normally large, e.g. 255 for 8 bits, the staircase is frequently termed a ramp, though this is not strictly accurate.

Monotonicity

A DAC is said to be monotonic if an increase in the applied binary coded digital number always produces an increase in the analogue output. Waveforms produced by a D-A 'staircase' generator illustrated in Figure 4a shows the effect of non monotonicity.

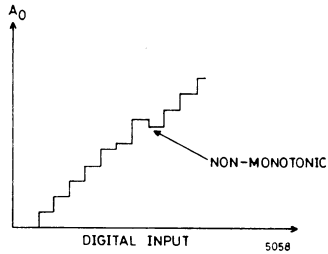


Fig. 4a Non-monotonicity

Ideal DAC Output

The ideal DAC output of a staircase generator is shown in Figure 4b.

The output is defined as a set of points on a straight line between zero and full scale. For an ideal 8-bit DAC:

$$V_{out} = \frac{n}{2^8 - 1} \times V_{FS}$$

$$= \frac{n}{255} \times V_{FS}$$

and $$V_{FS} = \frac{255}{256} \times V_{REFinput}$$

$\therefore$ $$V_{out} = \frac{n}{256} \times V_{REFinput}$$

where 'n' is the number represented by the digital input.

For example $$01101100 = 2^6 + 2^5 + 2^3 + 2^2$$

$$= 108$$

gives an output $$V_{out} = \frac{108}{256} \times V_{FS}$$

$$= \frac{108}{256} \times V_{REFinput}$$

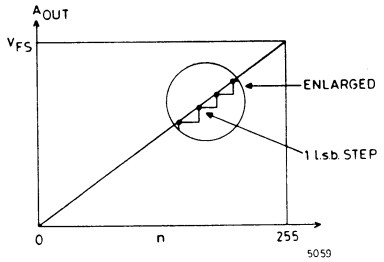


Fig. 4b Ideal DAC output

Linearity Error

A DAC may deviate from the ideal as shown in Figure 4c. The error is usually specified as a maximum deviation of the analogue output, from the ideal output, as a fraction of the 'Least Significant Bit'. The ZN425E has a linearity better than $\pm\frac{1}{2}$LSB, and

$$\tfrac{1}{2}\,\text{LSB} = \tfrac{1}{2} \times \frac{V_{FS}}{255}$$

Relative Accuracy

The error expressed as a percentage of the full scale voltage, V_{FS}, is termed the relative accuracy.

The ZN425E, an 8-bit converter with $\pm\frac{1}{2}$ LSB linearity, has a relative accuracy of $\frac{1}{510} \times 100\%$, i.e. approximately 0.2% accuracy.

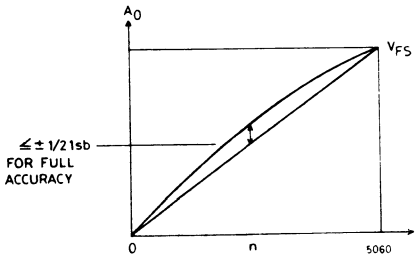


Fig. 4c Error definition

2. D-A and A-D CONVERTER SYSTEMS

2.1 8 bit D-A and Calibration Procedure

The ZN425E gives an analogue voltage output directly from pin 14, so that the usual current to voltage converting amplifier is not required. However, in order to buffer the resistive ladder output impedance, to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Figures 5a and 5b show a typical scheme with either the ZN424P or ZLD741CP as the buffer amplifier. The internal voltage reference source (V_{REFout}) is used, and to minimise temperature drift the source resistance to the inverting input of the buffer amplifier should be approximately 6 kΩ. Calibration procedure is as follows:

(i) Set all bits to LOW and adjust R2 until $V_{out} = 0.000V$

(ii) Set all bits to HIGH and adjust R1 until V_{out} = nominal full scale reading – LSB.

(iii) Repeat (i) and (ii).

e.g. Set F.S.R. to +3.840V – 1 LSB = 3.825V.

$$(1\ LSB = \frac{3.84}{256} = 15\ mV)$$

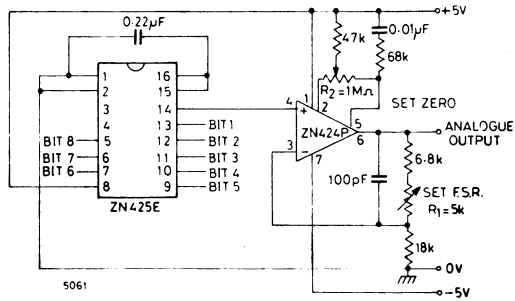


Fig. 5a 8 bit DAC using ZN424P

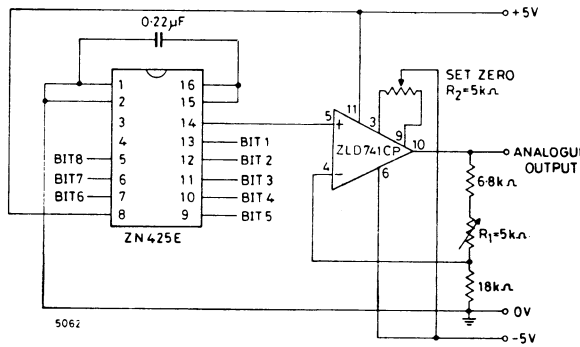


Fig. 5b 8 bit DAC using ZLD741CP

2.2 8 bit A-D and Calibration Procedure

Figure 6 shows the ZN425E in a counter type ADC which comprises a comparator and a latch and requires an external clock. Upon application of a convert command pulse (15 μs minimum) the counter is set to zero and at the same time the state of the latch is altered.

The gate is opened, enabling clock pulses to be fed to the counter input (Pin 4) of the ZN425E. The analogue output of the ZN425E begins to ramp up until its amplitude equals that of the analogue voltage at the non-inverting input of the comparator. At this point the comparator changes state, altering the latch to its initial resting state, thus inhibiting further clock pulses. Hence the digital number stored in the respective bits of the ZN425E is a true representation of the analogue input voltage. The diode is included so that when the comparator changes state, its output is effectively clamped at zero (LOW).

Operating clock frequencies can be as high as 400 kHz. Improved results may be obtained by using narrow clock pulses to avoid the trailing edge affecting ramp settling. At frequencies above 100 kHz a faster comparator than the ZN424 should be used for optimum linearity around zero.

The conversion time is dependent upon the analogue input and for full scale reading (F.S.R.) is given by the clock period multiplied by the number of counts.

$$\text{If } F_{Clock} = 256 \text{ kHz},$$

$$T_{Convert} = \frac{2^8}{256 \times 10^3} \text{ seconds} = 1 \text{ ms}$$

The calibration procedure is as follows:

(i) Apply continuous CONVERT COMMAND PULSES

(ii) Apply full scale minus $1\frac{1}{2}$ LSB to analogue input and adjust F.S.R. pot until the converter LSB just switches between 0 and 1 with all other bits at 1.

(iii) Apply zero $+\frac{1}{2}$ LSB to analogue input and adjust zero pot until the converter LSB just switches between 0 and 1 with all other bits 0.

(iv) Repeat step (ii)

E.g. Full scale = 4 volts.

$$1 \text{ LSB} = \frac{\text{Full Scale}}{256} = \frac{4 \text{ volts}}{256} = 15.63 \text{ mV}$$

Input for zero setting = $\frac{1}{2}$ LSB = 7.82 mV

Input for full scale setting = 4V − $1\frac{1}{2}$ LSB = 3.97656 volts.

After conversion is complete the analogue input is available from the ZN425E in digital and analogue form and therefore the ADC may be used as a sample and hold with infinite hold time. The convert command is replaced by a sample command.

A peak detect circuit may also be constructed using similar techniques, and is described in section 3.4.

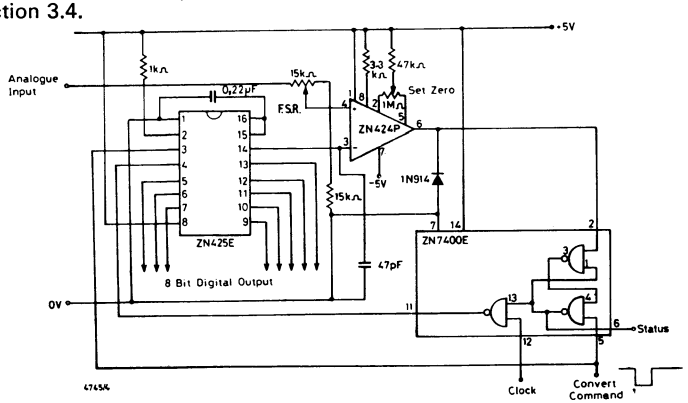


Fig. 6 8 bit Analogue to Digital Converter

2.3 Bipolar Operation

Previous circuits described have entailed the use of a uni-polar buffer amplifier (using ZN424E and ZLD741CP) following a DAC as a means of removing the offset voltage, minimising temperature drift and calibrating the DAC. A natural sequel to this is the derivation of a bi-polar buffer amplifier which fulfils these conditions. This entails buffering the output of a DAC such that the amplified output from the buffer is symmetrical about zero. To effect this, the conditions that have to be satisfied are:

(i) When the DAC output $= \frac{V_{REF}}{2}$ (digital input = 10000000) then the buffer amplifier output = zero.

(ii) Gain can be easily selected and suitable resistor values calculated. Actual gain and offset must be capable of fine adjustment.

The circuit of Figure 7a was first devised as a possible solution.

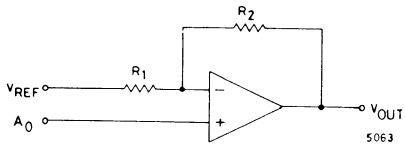


Fig. 7a Bi-polar operation, starting point

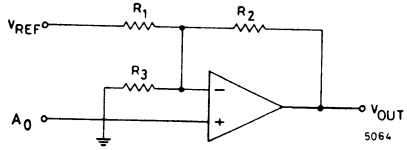


Fig. 7b Bi-polar operation, concept progression

If F_N = non-inverting feedback return $= \frac{R1}{R1 + R2}$ and F_I = inverting feedback return $= \frac{R1}{R2}$

Then V_{out} is given by:

$$V_{out} = \frac{A_O}{F_N} - \frac{V_{REF}}{F_I} = A_O\left(\frac{R1 + R2}{R1}\right) - V_{REF}\frac{R2}{R1} \quad \text{. . . equation 1}$$

If $A_O = \frac{V_{REF}}{2}$ and R1 = R2 then $V_{out} = 0$ satisfying condition (i).

However Gain $\left(\text{defined as } \frac{V_{out}}{A_O}\right) = \frac{R1 + R2}{R1} = 2$ and condition (ii) would not be satisfied since adjusting R1 or R2 would upset the gain on offset. To minimise these disadvantages therefore the circuit of Fig. 7b was devised using an additional resistance, with its Thevenin equivalent of Fig. 7c. Using equation 1 then an expression for the output voltage V_{out} can be shown as:

$$V_{out} = A_O\left[1 + \frac{R2\,(R1 + R3)}{R1\,R3}\right] - V_{REF}\frac{R2}{R1}$$

For $A_O = \frac{V_{REF}}{2}$ (Condition (i)) then $V_{out} = 0$

and $R1 = \frac{R2\,R3}{(R2 + R3)}$ i.e. R1 = parallel combination of R2 and R3.

Substituting this expression for R1

then Gain $G = \left[1 + \left(\frac{2R2 + R3}{R3}\right)\right] = \left[2 + \frac{2R2}{R3}\right]$

If we let say R2 = λR3 then $G = 2\,(1 + \lambda)$ and $\lambda = \left(\frac{G - 2}{2}\right)$

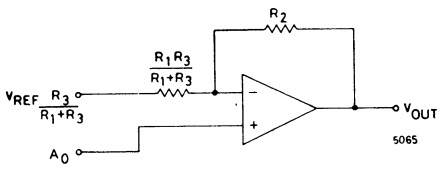


Fig. 7c Thevenin equivalent of Fig. 7b

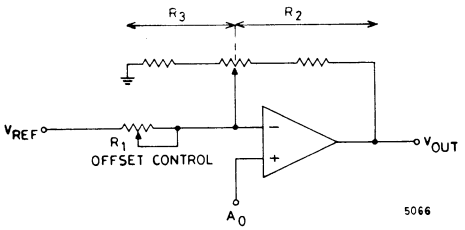


Fig. 7d Bi-polar operation, control schematic

i.e. $G \geqslant 2$ from which $R2 = \left(\frac{G-2}{2}\right) R3$

And $R1 = \left(\frac{R2\,R3}{R2 + R3}\right) = \left(\frac{\lambda}{1+\lambda}\right) R3 = \left(\frac{G-2}{2}\right) R3$

Furthermore the buffer amplifier input impedance =

$$\frac{R1R2\,R3}{R1R2 + R2R3 + R1R3} = \left(\frac{G-2}{2G}\right) R3$$

All the above expressions and relationships form a basis for development of the circuit of Fig. 7d whereby by defining a certain gain (G) all resistor values can be appropriately calculated as illustrated.

e.g. Let $G = 4$, then $R_{in} = \left(\frac{4-2}{8}\right) R3 = \frac{R3}{4}$

If $R_{in} = 10\ k\Omega$ (the value required for minimum offset taking into consideration R_{out} of ZN425E DAC $\simeq 10\ k\Omega$) then $R3 = 40\ k\Omega$.

$$R2 = \left(\frac{G-2}{2}\right) R3 = \left(\frac{4-2}{2}\right) R3 = R3 = 40\ k\Omega$$

$$\text{And } R1 = \left(\frac{G-2}{G}\right) R3 = \left(\frac{4-2}{4}\right) R3 = \frac{R3}{2} = 20\ k\Omega$$

It has been shown that $R1 = \frac{R2\,R3}{R2 + R3}$. The simplest approximation ensuring this relationship is by using a potentiometer as a gain control.

The finalised circuit is shown in Fig. 8.

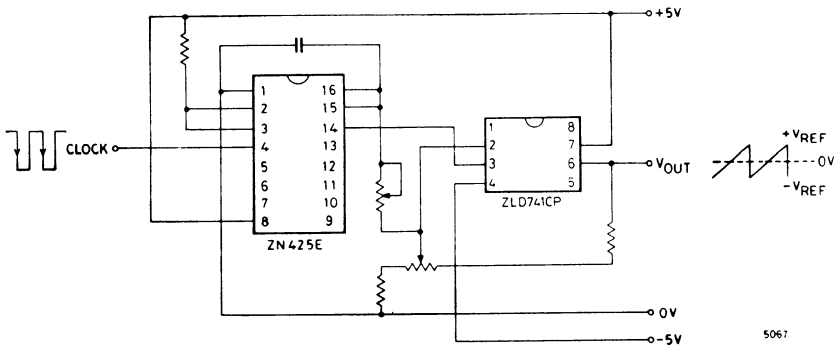


Fig. 8 Bi-polar operation, circuit diagram

2.4 Applications

Applications for the use of the ZN425E in its D-A or A-D mode are those where 8 bit accuracy suffices. This is the majority of transducer applications, particularly as system hierarchy is tending to change with the advent of microprocessors, taking the conversion near to the point of measurement. For example, in data acquisition monitoring say 100 channels, it is feasible and economic to use one D-A per channel and multiplex one A-D per 8 channels using a single microprocessor.

If one reference is required to power several converters, additional source current may be provided by an external parallel resistor from supply to reference providing 1.2 mA per additional converter in excess of three. In this case the additional earth pin current causes an offset due to a pin resistance of around 0.1 Ω

Specific applications of 8 bit A-D are in conjunction with stress or strain gauges, and many temperature applications. 8 bit D-A may be used for driving chart recorders, programmable power supplies and actuators.

3. RAMP GENERATION

The counter in the ZN425E is very convenient for feeding in a clock to generate a staircase. This facility is used in the majority of applications detailed below.

The count rate which may be used to obtain full ramp accuracy, determined by the worst case settling time of 2 μs, is 500 kHz, giving a cycling time of around ½ ms. However, the counters are capable of being clocked at up to 5 MHz, though there will be a loss in staircase accuracy at this speed.

3.1 Continuous

This is illustrated by the circuit of Fig. 9 and is simply accomplished in the normal DAC mode by applying clock pulses to the on chip counter (Pin 4) of the ZN425E, which produces a staircase waveform, When the counter is full it returns to its empty state and counting recommences resulting in a continuous ramp.

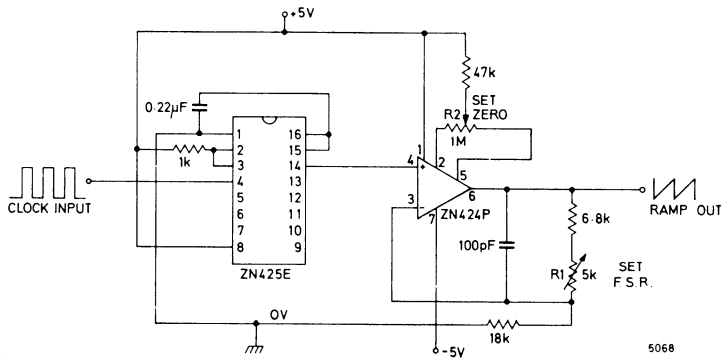


Fig. 9 Precision ramp generator

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary as previously described for the DAC.

The ramp period for 8 bits will be equal to 256 times the clock period, and the maximum amplitude of the ramp from the ZN425E using the internal reference voltage will be $V_{REFout} - 1$ LSB. Therefore, the peak ramp amplitude from the buffer will be this value times the amplifier gain, which, with gain adjustment potentiometer set halfway

$$2.5V \times \frac{3}{2} = 3.75V.$$

A duty cycle drive signal is sometimes required from an input voltage generated by a potentiometer, for example, for actuator drives, or general power control. This may be provided as shown in Fig. 10, where the ZN425E provides a continuous ramp, against which the voltage reference is compared using a ZN424P. The output from the comparator then provides the duty cycle signal directly.

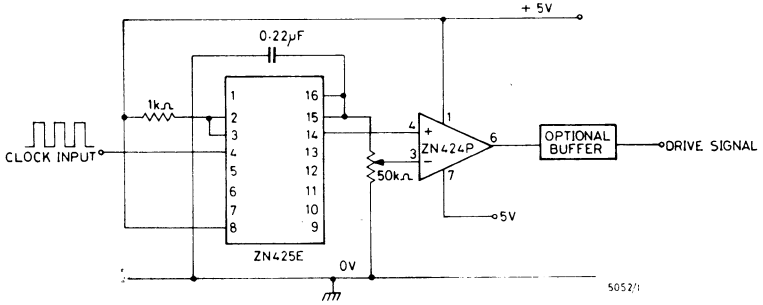


Fig. 10 Duty cycle drive signal

3.2 One Shot

A single one shot ramp can be generated quite simply (Figs 11a and 11b) by using a latch and two capacitors to control the counter reset of a ZN425E DAC. Operation is as follows:

The stationary states of the latch are shown, these being initially determined by the charging times of capacitors C1 and C2 which ensures the counter reset of the ZN425E (Pin 3) is LOW. Upon operating the START button the states of the latch are altered and a HIGH is fed to the counter reset enabling counting of the input clock pulses to commence. The analogue output begins to ramp up until the counter is full at which point the MSB goes LOW altering the latch to its initial resting states. This resets the counter and terminates the ramp. It should be noted that even if the start button is held down at the commencement of the operation, only a one shot ramp results, and not a periodic function.

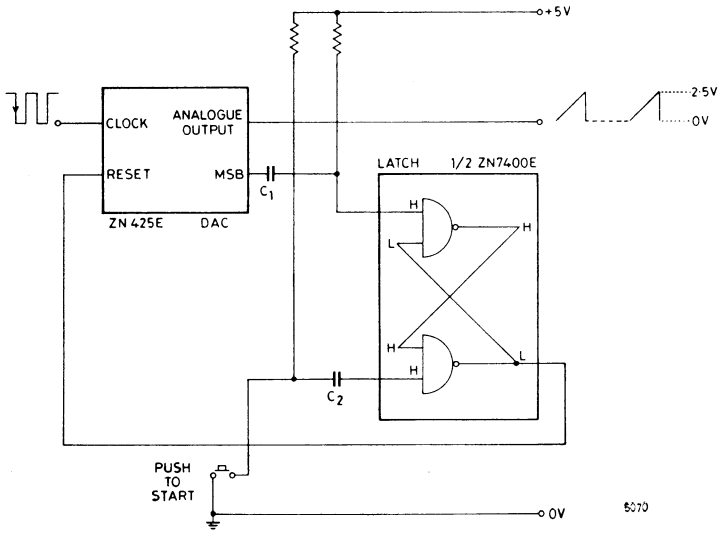


Fig. 11a One shot schematic

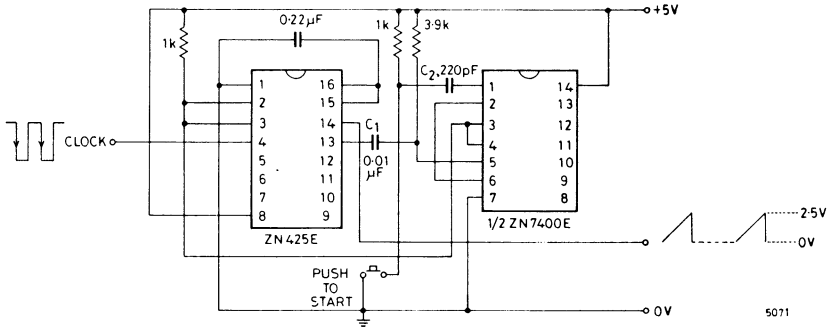


Fig. 11b One shot circuit

A more sophisticated alternative method performing the same function, which replaces capacitors by logic, is outlined in Figs. 11c and 11d. Stationary states of the various logic elements are as indicated. The initial state of the flip-flop is determined by the relative states of the PRESET and CLEAR inputs. Upon switching on the supply the PRESET is held LOW with respect to CLEAR because of the charging time associated with C1 and R1. This results in Q = HIGH, $\overline{Q}$ = LOW, therefore, the counter reset on the ZN425E is LOW.

When the start button is pressed, a pulse from the monostable clears the flip-flop, the counter reset goes HIGH enabling the counting of the input clock pulses to commence. The ZN425E analogue output begins to ramp up until the counter is full, at which point the MSB goes LOW. This is fed to the CLOCK input of the flip-flop which then TOGGLES, reverting to its original state, thereby resetting the counter and terminating the ramp. As with the previous circuit only a one shot ramp will be generated even if the start button is held down.

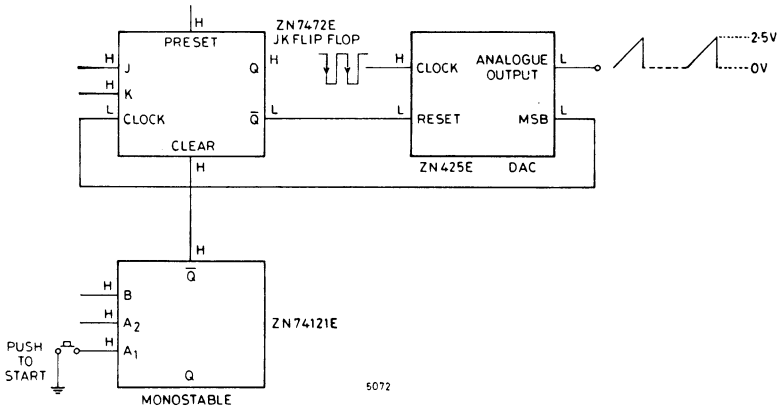


Fig. 11c Alternative one shot schematic

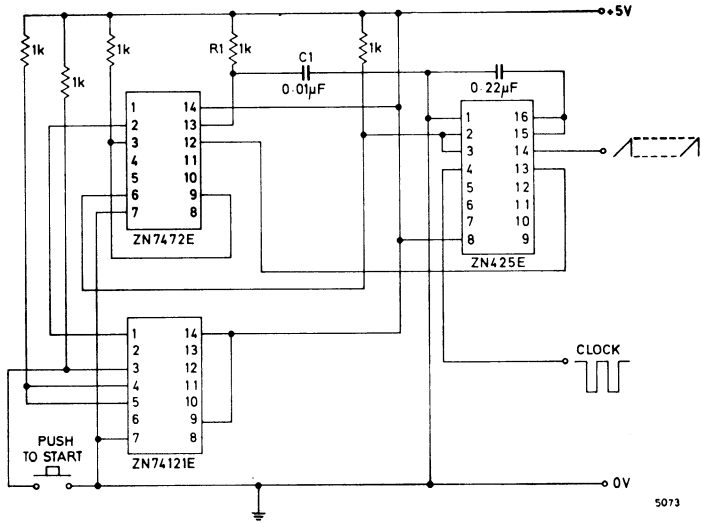


Fig. 11d Alternative one shot circuit

3.3 Weighing System and Auto Zero

The system to be described is intended for either static or on-vehicle load indicating applications and employs integrated circuits from the Ferranti Standard Product range. Variations of the scheme are indicated which increase its range of application. The overall system is shown in the circuit diagrams of Figures 12a to 12e.

The basic measuring function is a $3\frac{1}{2}$ digit DVM using the dual slope analogue to digital converter principle. This displays an analogue input of up to ± 1999 millivolts which is scaled as required. All the DVM digital and control functions are carried out by one C.D.I. integrated circuit from the U.L.A. (Uncommitted Logic Array) range, type ZNA116E.

The DVM input is driven from a separate unity gain summing amplifier which accepts inputs from any number of channels each consisting of transducer and pre-amplifier.

Included in the system is a push button auto-zeroing circuit which automatically sets the output of the summing amplifier to zero. This facility eliminates any small zero errors which may have accumulated in the transducer and pre-amplifier chain or any false zero readings which can appear when on-vehicle systems are operated on uneven ground. For this function the ZN425E 8 bit digital to analogue converter is used. This monolithic integrated circuit also includes an 8 bit binary up-counter and a reference voltage generator and by clocking the counter a voltage ramp of 256 discrete steps is generated. This ramp is level shifted to become symmetrically bipolar with respect to 0V and then applied to the virtual earth of the summing amplifier. This forces the amplifier output through 0V and a comparator circuit detects the 0V condition and inhibits the clock pulses to the counter. The selected ramp output level is therefore held indefinitely unless the auto-zero is switched off when the system reverts to the original zero conditions.

Additional facilities include B.C.D. outputs for data logging purposes and an overload alarm system with warning indication.

The alarm system uses two comparators into which are set two analogue levels, one corresponding to a preset percentage of full load and the other to full load. When the load reaches the first level a 1 Hz square wave output is available and a separate output gives a continuous signal at the second level. These outputs may be wire ORed or used separately to drive visual or audible alarms.

It is not essential for the DVM function to be fully bi-polar in this application because negative readings occur only as small zero errors. A minor modification enables the circuit to display lower accuracy negative readings at the same time eliminating one of the ZN423 reference generators.

Further modification, appropriate for some applications, results in a 3 digit display with a 1 Hz flashing leading zero to indicate a small negative zero error.

This approach, using a mix of standard function integrated circuits gives maximum system flexibility. For example, an on-vehicle application may require separate auto-zero functions on a number of axles or an overload alarm indication may require duplication. By adding the appropriate integrated circuits the system can be tailored to suit a range of vehicle requirements with a minimum of chip function redundancy and therefore minimum cost.

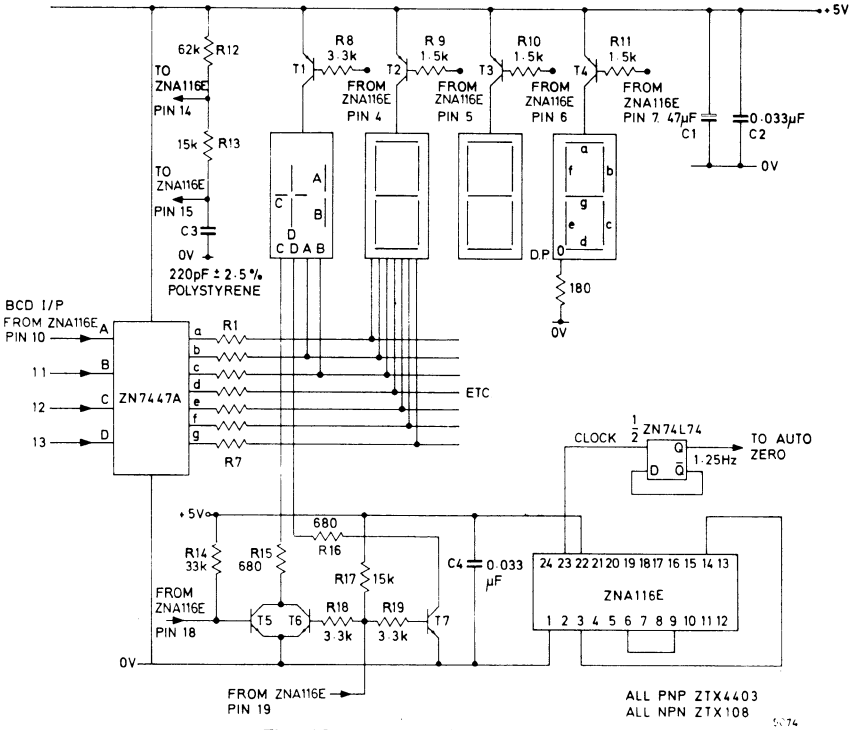


Fig. 12a Display/digital circuit

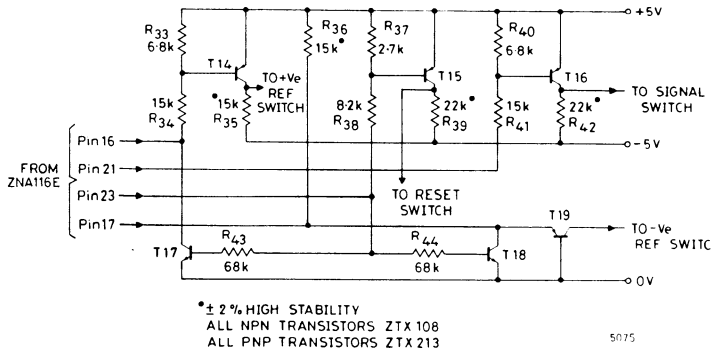


Fig. 12b Analogue switch

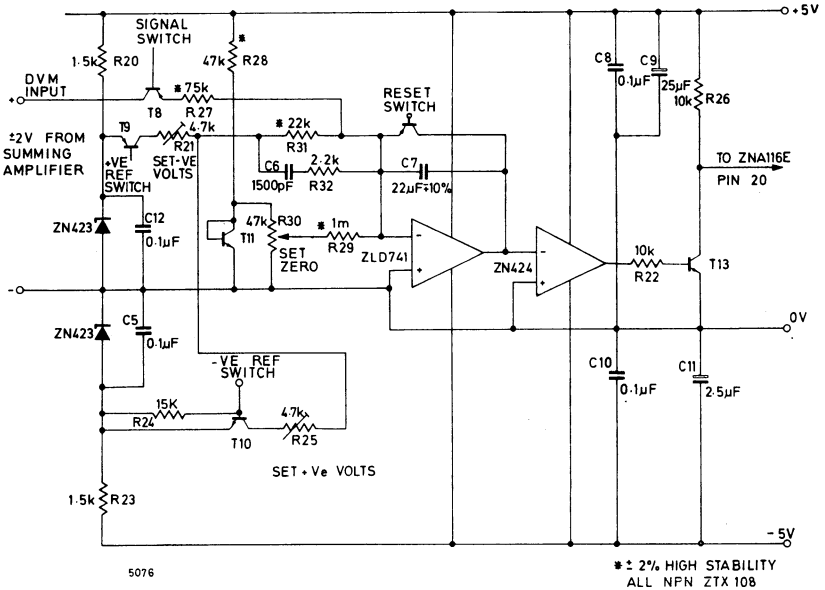


Fig. 12c Dual slope integration circuit

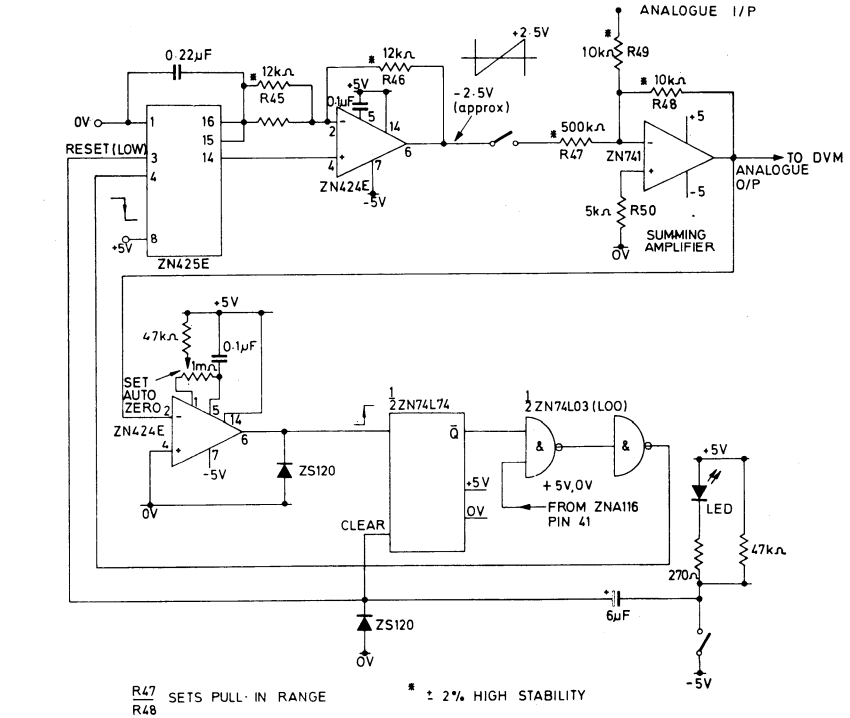


Fig. 12d Auto zero circuit

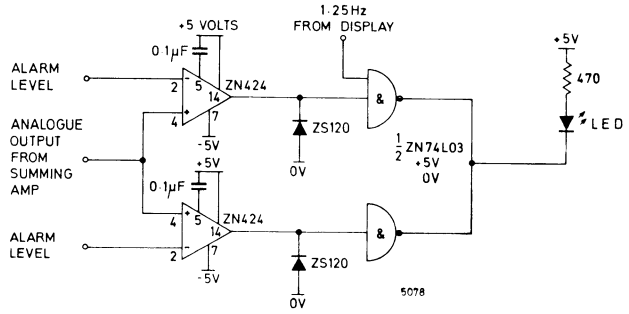


Fig. 12e Alarm circuit

3.4 Peak Detect

A peak detect circuit may be constructed simply using the form of A to D system shown in the schematic of Fig. 13. When left running continuously it will hold the maximum input signal level it is able to track, i.e. peak detect.

After application of a reset pulse, the state of the comparator enables clock pulses from the Schmitt trigger circuit to be fed to the counter of the ZN425E. The analogue output begins to ramp up until it attains the level of the analogue input voltage at which point the comparator changes state and inhibits further clock pulses. Therefore, the analogue output is held and stored digitally in the bits of the converter. It will continue to hold this level until a further increase in analogue input voltage changes the comparator state, enabling the clock, and the sequence is repeated.

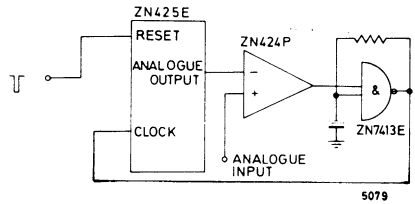


Fig. 13 Peak detect schematic

3.5 Channel Selector

Another interesting application of the A-D principle is for a channel selector in communications, e.g. citizens or amateur band. In effect it replaces a multiway switch, mechanically limited to 24 or 30 channels, by a 10 turn potentiometer which can be used with the system of Fig. 14 to generate many more discrete steps, typically 64 but up to 256.

The ZN425E, with internal counter, provides the A-D conversion function, using a single ZN7400E package for external logic, and a high performance ZN424P op-amp as comparator. A ZN7413E dual Schmitt provides the necessary clock and conversion oscillators, no sync is needed here. Channel selection is by the 10 turn potentiometer 'Main Tune' or, optionally, by preset potentiometers, to preferred channels. Resistance values for the pots are not critical.

The binary output is converted to BCD by the 74185 and latched to provide a steady output signal, i.e. when a particular channel has been selected no jumps occur during cycling. The conversion oscillator periodically checks the state of the input voltage, by a fresh conversion on the ZN425E, and updates the latches when the status command

indicates that the conversion is complete. The BCD signals drive 7-segment indication of channel number and provide the drive outputs for either a modulo-N digital synthesiser, a crystal-bank synthesiser, or a crystal selector. Features of the system are:

1. Bi-directional, quasi-continuous tuning on a single control.
2. Electronic tuning lock.
3. Simple switching between 'tune' and 'preferred channel' operation.
4. Preferred channels selected by preset potentiometers operating through to the synthesiser. Channels are user-alterable.
5. Inherent non-volatile 'memory' on potentiometers.
6. Channel number indication shows channel actually in use, particularly suitable for non-co-channel working, repeaters, etc.

In addition, a scanning facility can be easily added if the receiver used has a squelch switched output.

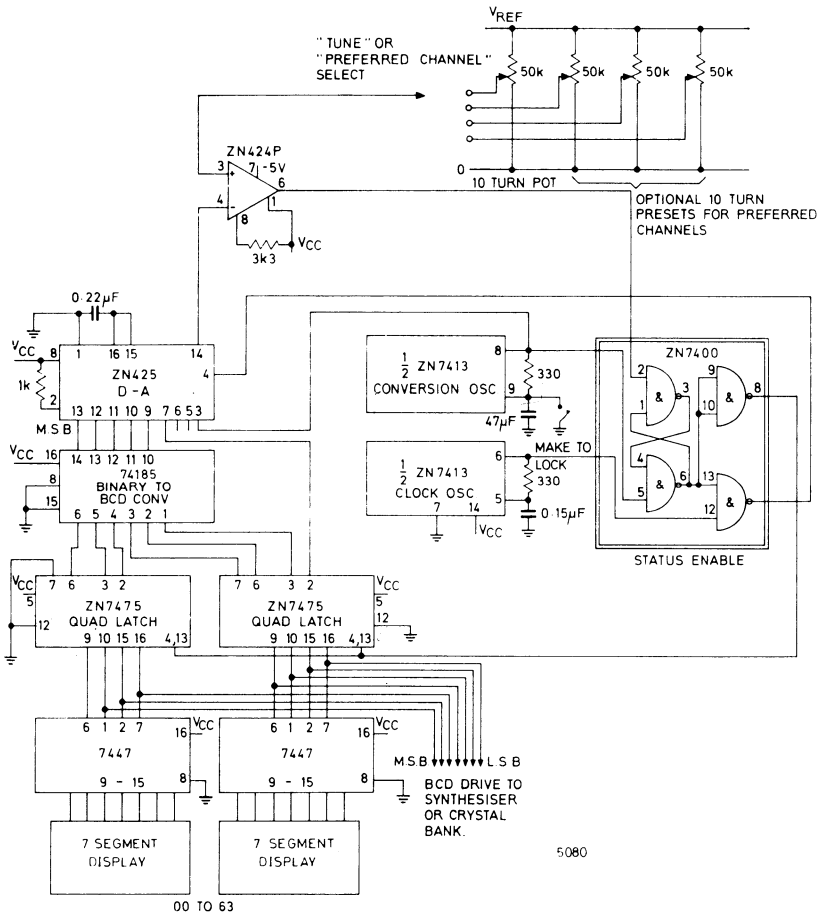


Fig. 14 Channel selector, 64 way

3.6 Bargraph Display Drive System

The ZN425E may be used in its continuous ramp mode very advantageously in conjunction with linear light emitting diode (LED) displays, e.g. Bargraphs. This is because the LED displays lend themselves to being accessed in a matrix fashion using a time sharing or multiplexing technique. This allows a reduction in the number of connections required, to m + n in an array of m n diodes (Fig. 15a) This reduction in connections also allows a simplification of the drive system, as described below.

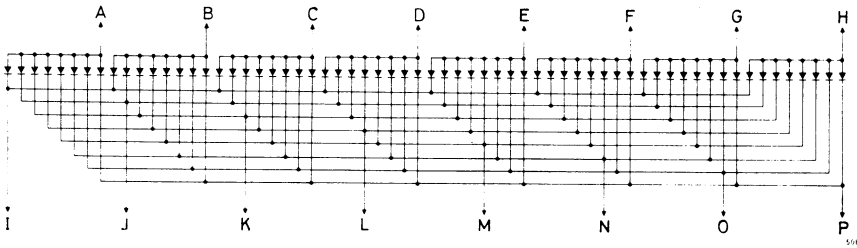


Fig. 15a Diode matrixing connections

The simplest technique for providing for a bar output whose length is proportional to an analogue input is shown in Fig. 15b. The ZN425E is driven in its continuous ramp mode. The six most significant digits from the counter are then decoded into two lots of 1 out of 8 drives. These drives then access the LEDs in a multiplexed fashion, so that the 64 LEDs are accessed once each in turn in a complete scan cycle. A high clock frequency is selected which ensures that the flicker rate is fast enough and thereby indistinguishable to the eye.

At the same time as the LED scan cycle is taking place, the ZN425E provides a staircase analogue output, as shown. This is compared with the analogue input in a comparator, whose output controls the display enable. Thus while the ramp is less than the analogue input, the LEDs being scanned are enabled (the start of the Bargraph line), while once the ramp output is larger than the analogue input, the drives to the LEDs further along the line are inhibited. This, therefore, provides an illuminated bar length proportional to the analogue input.

This system as it stands suffers from a minor disadvantage, in that the duty cycle for accessing each LED is 1/m n, or 1/64 for the case of Fig. 15b. Although the LEDs become more efficient with pulsed operation, 1/64 duty cycle does not provide adequate brightness for some applications.

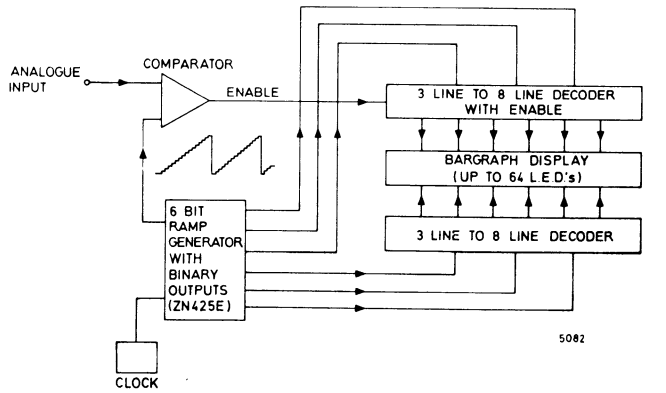


Fig. 15b Simple bar display schematic drive system

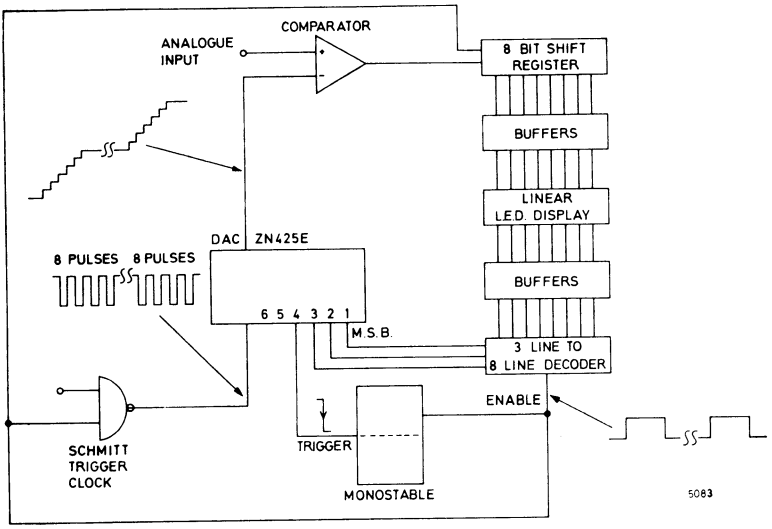


Fig. 15c Improved bar display schematic drive system

A technique to overcome this objection is shown in outline in Fig. 15c. The technique used here is to load a shift register rapidly serially, and subsequently use this register to provide LED multiplex drives in parallel. This means that the duty cycle for accessing the LEDs is improved (for a 64 LED array) from 1/64 to just less than 1/8. This is quite sufficient for acceptable brightness in virtually all applications.

This system operates as follows. While the monostable is in its mode of loading the shift register, the ZN425E staircase output increases in 8 discrete steps. Simultaneously the shift register is loaded with the comparator output to provide serial to parallel conversion. The comparator output is thus effectively changed from serial access to parallel access of the linear LED array.

When the monostable changes over to its (longer period) display mode, the LED array is accessed, and the LEDs are driven or otherwise according to the enable or disable information stored in the shift register. The display is incidentally disabled while the mono is loading the register.

To provide an example of operation, suppose the bar is to have the first 37 LEDs displayed, with the rest blanked. Starting from the ZN425E being reset and the mono in its register load state, operation is as follows.

The mono allows eight clock pulses through the gate to the ZN425E, after which the ZN425E count pulse retriggers the mono. These eight pulses generate the first eight steps from the analogue output, which produce from the comparator a continuous display enable (say logic 1). These are loaded into the shift register which thus finishes with 11111111 in parallel to the LED display.

At this point the mono is tripped into its display mode, and the counter has reached 8 (or 001 000). However the decoder must access the first eight LEDs, so that the second decoder output is connected to the first set of LEDs. These are all illuminated.

During the second register load period, the cycle is repeated, with again all ones being loaded into the register which subsequently brightens up the second eight LEDs (9–16). The same occurs during the third and fourth mono cycles, lighting up the first 32 LEDs.

During the fifth register load period, the analogue output goes up a further eight steps. However after the fifth step the comparator changes over to load zeros for the remainder of this period into the shift register. If loaded from the left the register will then finish up as 00011111. Subsequently during the mono display period LEDs 33 to 37 inclusive will be lit, but 38 to 40 will be blanked off.

The sixth to eighth mono cycles will load zeros into the shift register, blanking off LEDs 41 to 64. The full LED scan cycle is therefore completed with the desired effect.

Typical system clock rates are 400 kHz, and typical monostable periods 500 μs for the values shown

An actual circuit to achieve this is shown in Fig. 16 and it may be seen that this is elegant and simple, The type of display which may be accessed in this way is the Bowmar Microstic R1M-053-66A, which is connected in eights on its common anodes. This has 64 red LEDs and a further two LEDs at the ends, one to show the display is working, and the other for over-range. Similar techniques may be used with the 106 LED version.

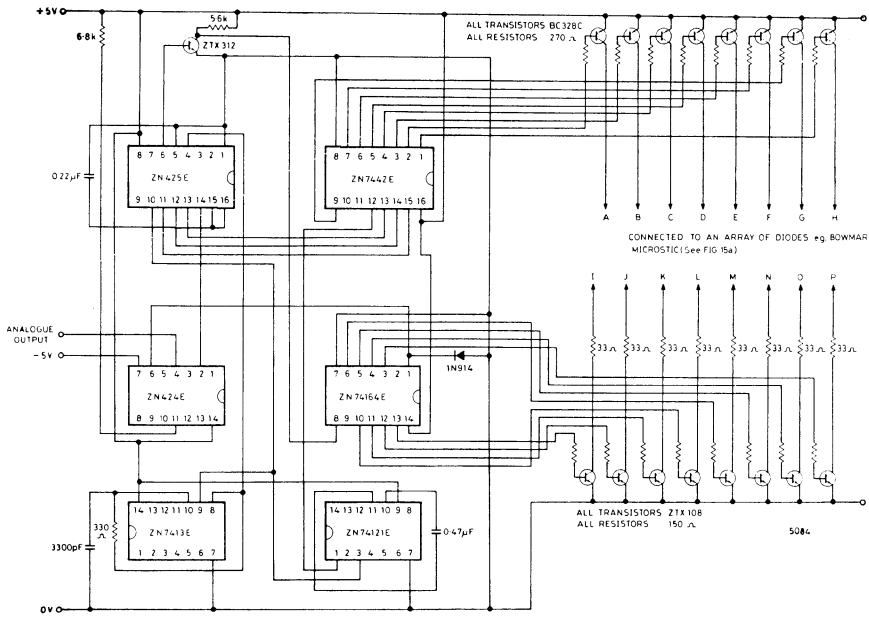


Fig. 16 Column display drive system

3.7 Up Down or Tracking

The counter on the ZN425E is only an up counter, and some systems, e.g. tracking converters or servos, may require an up/down counter. This is conveniently provided externally, e.g. the ZN74193E using the ZN425E purely in its D-A converter mode and ignoring the counter (Fig. 17). While this may appear to be inelegant it is nevertheless economically sound.

4. MULTIPLY/DIVIDE

4.1 Multiplier

The reference supply to the D-A section of the ZN425E has been purposely left on an uncommitted terminal, so as to allow connection either from its own reference or from an external reference. The point about an external reference is that it allows a multiplying effect, in that the analogue output is proportional both to the binary code and the reference voltage. For this reason this type of DAC is called a multiplying DAC.

Practical limits in multiplying voltages are 0V and 3V.

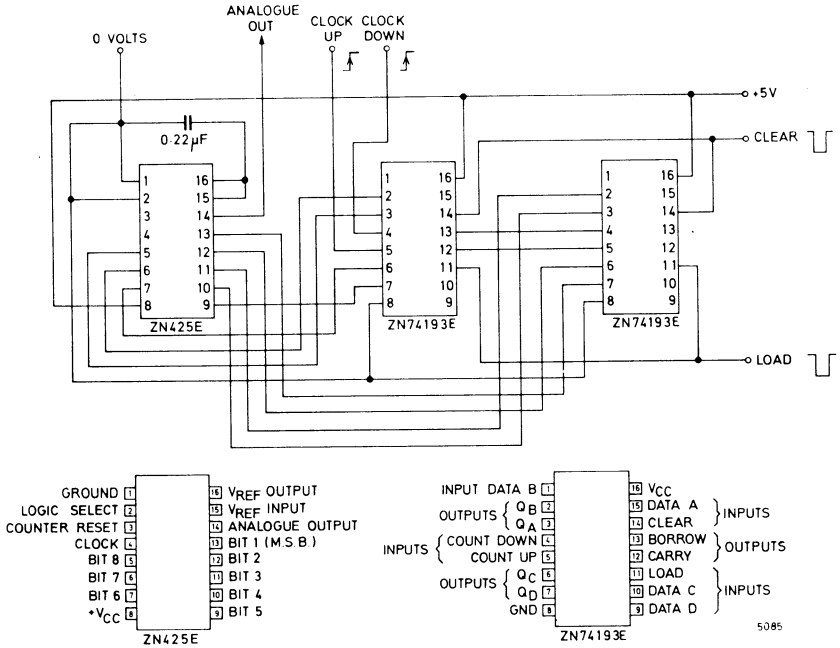


Fig. 17 Up/down counter or tracking DAC circuit

4.2 Variable Frequency Divider

If a ZN425E is operated in its continuous ramp mode in conjunction with a comparator whose output is fed back to the counter reset, a variable frequency divider can be constructed as shown in Fig. 18a. Here an analogue voltage can be used to control the number of steps before reset is applied, the overall effect being to provide variable frequency division under the control of a potentiometer.

4.3 Voltage Controlled Oscillator

The schematic of Fig. 18a may also be used as a voltage controlled oscillator. However the frequency is the inverse of the applied voltage, though the period is, of course, proportional. The corresponding circuit of Fig. 18b gives an output frequency or pulse rate which is inversely proportional to applied voltage as shown in Fig. 18c. It is, however, in some cases more desirable to produce an output frequency directly proportional to applied voltage. This is accomplished by the circuit depicted by Figs. 19a and 19b and involves the use of an inverse scaler described in the next section, for which a brief mention is necessary to understand the basic operation of the V.C.O.

By using a DAC in the feedback loop of an operational amplifier an output voltage is derived which is inversely proportional to a digital input number to the DAC. Clock pulses applied to the DAC counter will produce a repetitive output waveform which is a hyperbolic $\frac{1}{n}$ function. This waveform is applied to the inverting input of a comparator whilst the analogue input voltage to be frequency converted is applied to the non-inverting input. At the instant they become equal the comparator changes state and operates the Schmitt trigger which resets the DAC counter. The result is a train of negative going pulses whose frequency is directly proportional to the applied input voltage. This follows simply because if F_{Clock} = clock frequency to the DAC counter, and F_{out} = output frequency, then $F_{out} = \frac{F_{Clock}}{n}$ where n = digital input number, and analogue input voltage to the comparator $V_{in} \propto \frac{1}{n}$

Therefore, $F_{out} \propto V_{in}$ and the appropriate characteristic is shown in Fig. 19c.

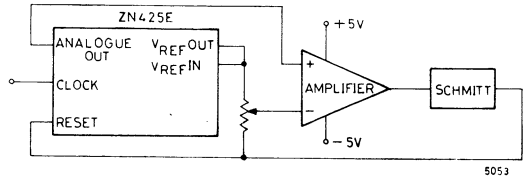


Fig. 18a Variable frequency divider or VCO schematic

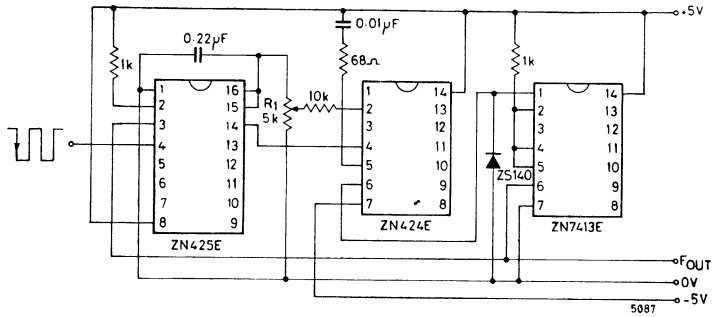


Fig. 18b Variable frequency divider or VCO circuit

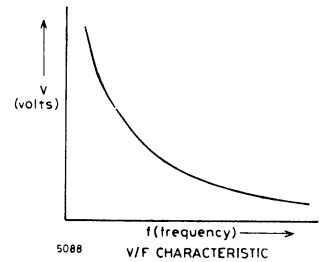


Fig. 18c VCO characteristics

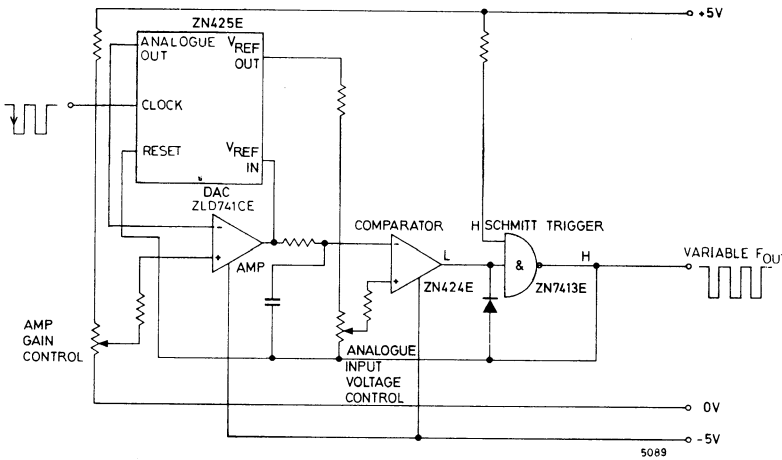


Fig. 19a Schematic of VCO giving frequency proportional to voltage

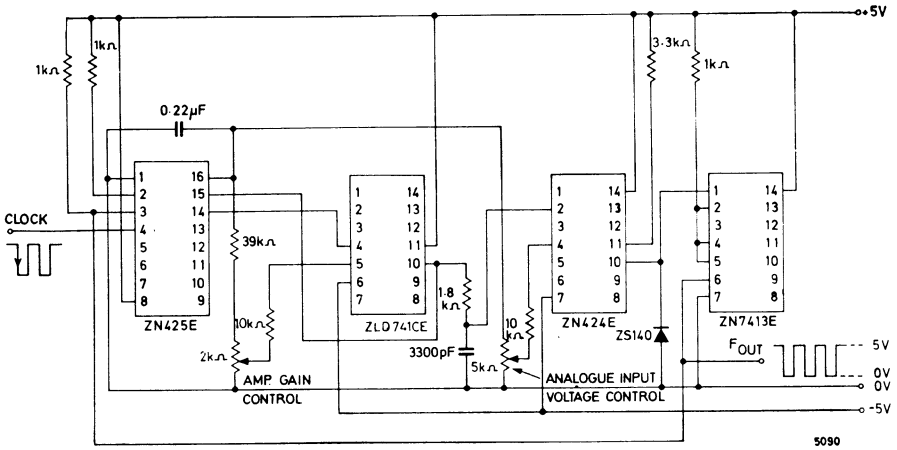


Fig. 19b Circuit of VCO giving frequency proportional to voltage

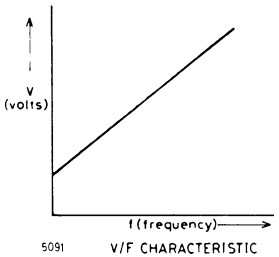


Fig. 19c VCO characteristics

5. FUNCTION GENERATION

By virtue of the multiplying function, the ZN425E may also be used for function generation as described below.

5.1 Inverse Scaler

If a DAC is operated in the feedback loop of an operational amplifier then the amplifier gain is inversely proportional to the input digital number or code to the DAC. The version giving scaling inversely proportional to positive voltage is shown in the schematic of Fig. 20a and the practical circuit of Fig. 20b.

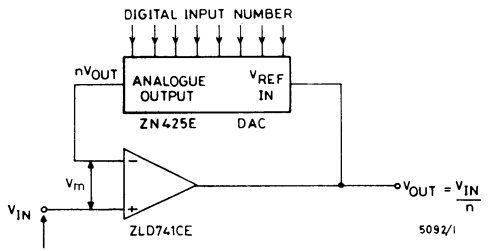


Fig. 20a Inverse scaler schematic

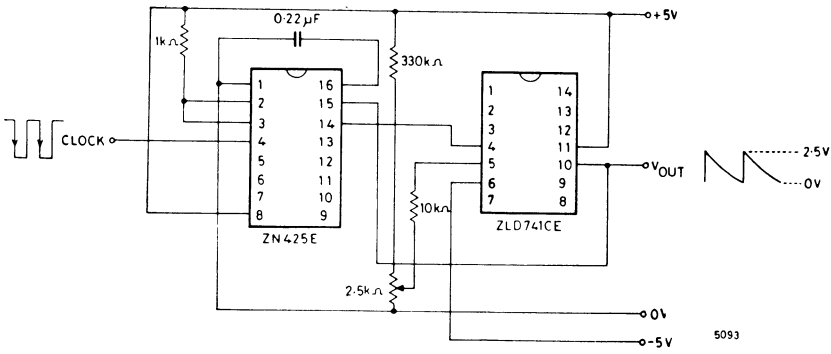


Fig. 20b Inverse scaler circuit

If A = open loop gain of the operational amplifier, and n is a fractional number representing any digital input (00000000 to 11111111 for 8 bits), that is a fractional number between 0 and $\frac{255}{256}$ then from the diagram $V_{out} = AVm$, and $Vm = (V_{in} - n\,V_{out})$

$\therefore\ V_{out} = A\,(V_{in} - n\,V_{out})$ from which $V_{out}\,(1 + An) = AV_{in}$ $\frac{V_{out}}{V_{in}} = \frac{A}{1 + An}$

Since $An \gg 1$, $(A \simeq 100{,}000)$ then $\frac{V_{out}}{V_{in}} = \text{Gain (G)} \simeq \frac{A}{An} = \frac{1}{n}$

For $n = 1\ \text{LSB} = \frac{1}{256}$ then the maximum allowable input voltage V_{in} to prevent saturation $(V_{sat} \simeq 4V) = \frac{4}{256} \simeq 15\ mV$.

If n = 0 then G = A and for a fixed input level the amplifier output will normally be equal to the saturation voltage since $A \simeq 100{,}000$.

The complementary mode (scaling inversely proportional to negative voltage) is shown in Fig. 20c (schematic) and Fig. 20d (practical circuit).

$$V_m = \left[V_{in} - \left(\frac{V_{in} - n\,V_{out}}{R_I + R_F}\right)\right], \text{ and } V_{out} = -AV_m$$

If $\frac{R_I}{R_F} = F_I$ = inverting feedback return then

$$V_{out} = -A\left[V_{in} - \left(\frac{V_{in} - n\,V_{out}}{1 + F_I}\right) F_I\right]$$

From which

$$V_{out} = -\left[\frac{A\,V_{in}}{1 + F_I + nAF_I}\right]$$

If the input voltage V_{in} is negative with respect to ground, then

$$\text{Gain (G)} = \left[\frac{A}{1 + F_I + nAF_I}\right]$$

If we make $F_I = 1$, i.e. $R_I = R_F$ then $G = \left[\frac{A}{2 + nA}\right]$

But $nA \gg 2$ (since $A \simeq 100{,}000$)

and $G = \frac{A}{nA} = \frac{1}{n}$ as with the non-inverting circuit.

Figs. 20a and 20c illustrate both types of inverse scalers, where a repetitive waveform of a $\frac{1}{n}$ function is generated by feeding clock pulses to the counter of the DAC.

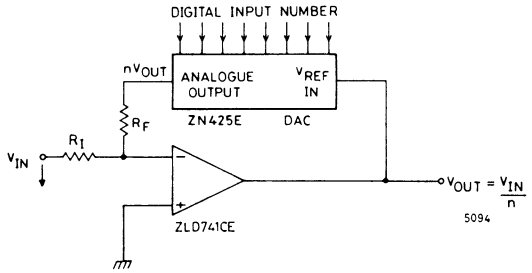


Fig. 20c Complementary inverse scaler schematic

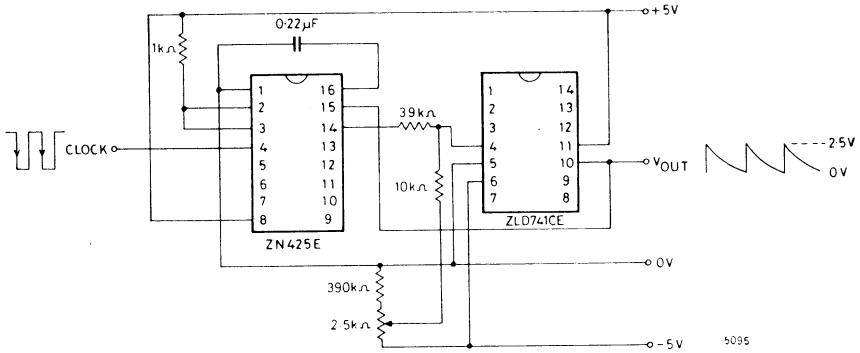


Fig. 20d Complementary inverse scaler circuit

5.2 Parabola

The multiplying action of the ZN425E may be used to generate a parabolic waveform shown schematically in Fig. 21a and a practical circuit Fig. 21b.

Basically the circuit operates as follows:

A continuous ramp output is generated by feeding clock pulses to the counter of a ZN425E DAC using its internal reference which is buffered, level shifted, and finally inverted using two operational amplifiers, so that the inverted ramp starts at a peak amplitude ($V_{1\ REF} = 2.5V$) and decreases linearly to zero. This is then used as an external reference supply for a second ZN425E DAC whose bits are connected to the first DAC for synchronous clocked operation. The resulting analogue output from the second DAC is a repetitive parabolic waveform whose peak amplitude is equal to $\frac{V_{1\ REF}}{4} = \frac{2.5}{4} = 0.625V$.

This follows because,

If N = a fractional number representing the digital input to both DACs then the analogue output voltage from the first DAC = An (where $A = V_{1\ REF} = 2.5V$).

This is then inverted and level shifted to provide the reference voltage to the second DAC = $(A - An) = V_{2\ REF}$.

Therefore the analogue output from the second DAC = $n\ (A - An) = An - An^2$ which is the equation of a parabola about the x axis of the form $y = ax^2 + bx + c$.

Peak amplitude of the parabola occurs when $n = \frac{1}{2}$

for which $V_{out} = \frac{1}{2}\left(A - \frac{A}{2}\right) = \frac{A}{4} = \frac{V_{1\ REF}}{4}$ as stated.

It should be noted that the ramp output from the non-inverting buffer amplifier will inherently have a gain greater than unity, and therefore its peak amplitude will be some factor in excess of $V_{1\ REF}$. However the ramp inverter and level shifter introduces corresponding attenuation to compensate this so that gain and level shift controls provide adequate adjustment in obtaining the desired inverted ramp output of peak amplitude.

$A = V_{1\ REF} = 2.5V.$

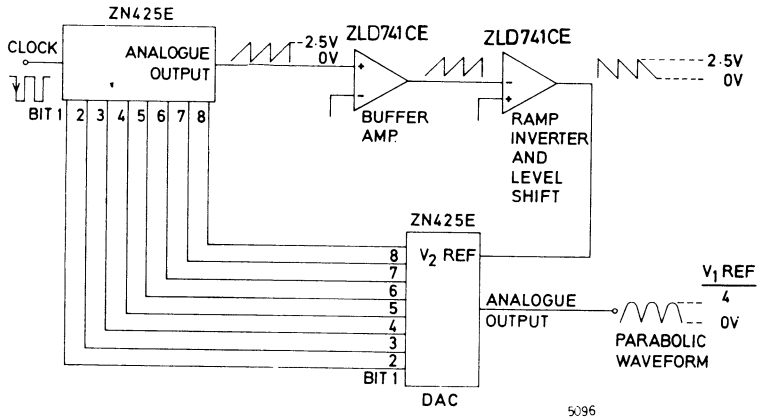


Fig. 21a Parabolic waveform generator schematic

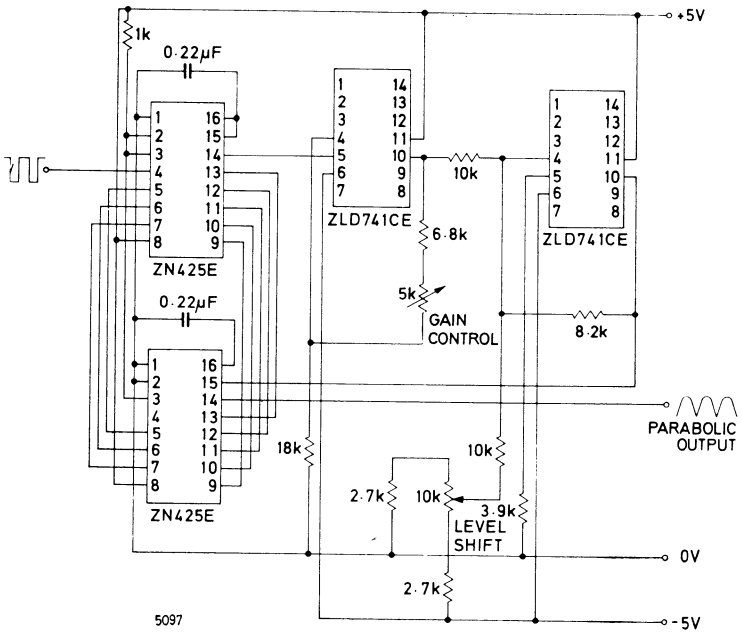


Fig. 21b Parabolic generator circuit

5.3 Log Approximation

A more complex function $y = \log n$ can be performed with the aid of previously described building blocks. A schematic arrangement as shown in Fig. 22a and the corresponding practical circuit of Fig. 22b provides a repetitive logarithmic relationship. The basic method is as follows.

An inverse scaler is used to generate an output voltage which is inversely proportional to a digital input number n to a ZN425E DAC. This voltage is then converted to a frequency or pulse rate using a VCO whose output frequency is proportional to an applied voltage The derived train of pulses of varying mark to space ratio are then fed into the counter of a final ZN425E DAC, these are integrated and a logarithmic output $\int\left(\frac{1}{n}dn = \log n\right)$ is obtained.

The period of the analogue $\frac{1}{n}$ function is dependent upon the input frequency to the inverse scaler. To rapidly convert this function to a pulse train and to generate a sufficient number of pulses for integration during this period, the clock frequency to the VCO derived from the Schmitt trigger must be high. The lower input frequency to the inverse scaler in synchronism with this clock frequency is obtained by using two ZN7493A dividers and, equals the clock frequency divided by 256. For the CR values indicated in the Schmitt trigger $F_{Clock} \simeq 512$ kHz therefore the input frequency to the inverse scaler $= \frac{512 \times 10^3}{256}$ Hz $= 2000$ Hz. And the output repetition frequency of the $\frac{1}{n}$ function $= \frac{2000}{256}$ Hz, for which the period $= \frac{256s}{2000} = 128$ ms.

Some means must be incorporated of resetting the counter on the final ZN425E DAC and thereby the logarithmic analogue output to zero at the completion of a full cycle of input pulses. Otherwise the analogue output would continue to increase with each cycle of pulses until it equalled the internal reference voltage, resulting in a 3 cycle logarithmic waveform. This is accomplished by using the negative going edge from the 4th significant bit which in fact resets the counter on the final DAC before the completion of a full cycle of input pulses. Whereas to be strictly correct resetting should be effected from the MSB ; bit 4 having been selected purely for convenience as it allows the logarithmic characteristic to be more easily displayed on the oscilloscope, since it accounts for a greater proportion of the output waveform, with negligible loss in amplitude.

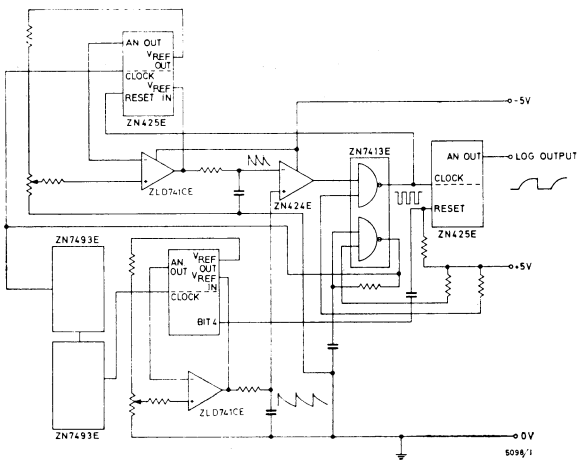


Fig. 22a Logarithmic waveform generator schematic

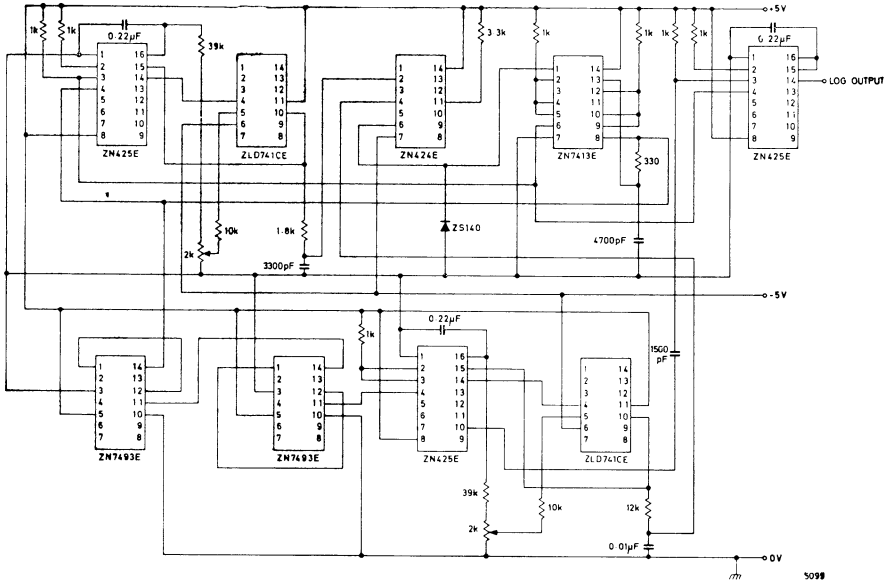


Fig. 22b Logarithmic waveform generator circuit

Microprocessor Interfacing Using The ZN427/ZN428 Data Converters

Analogue I/O Interface System for the 6800 Microprocessor

By SCOTT BIRD, Feranti Electronics Ltd.

Conventional Analogue I/O systems for Microprocessars are generally high accuracy, high cost, hybrid module/P.C. board assemblies, available only in one fixed configuration of I/O channels, (i.e. 16 Input and 2 Output channels). This Application Note describes how a low cost Analogue I/O system may be produced for the 6800 microprocessor using FERRANTI ZN427 A/D and ZN428 D/A converters with the 6820/6821 Peripheral Interface Adapter (PIA) I.C. This combination produces a versatile system which can be configured to the designer's particular I/O requirements, and which can also be expanded without major modifications to the hardware. The advantages of interfacing to the microprocessor via the PIA are that it provides a simple, easily expandable system, without additional address decoding and line buffering hardware, and it also simplifies timing problems associated with a direct bus interface.

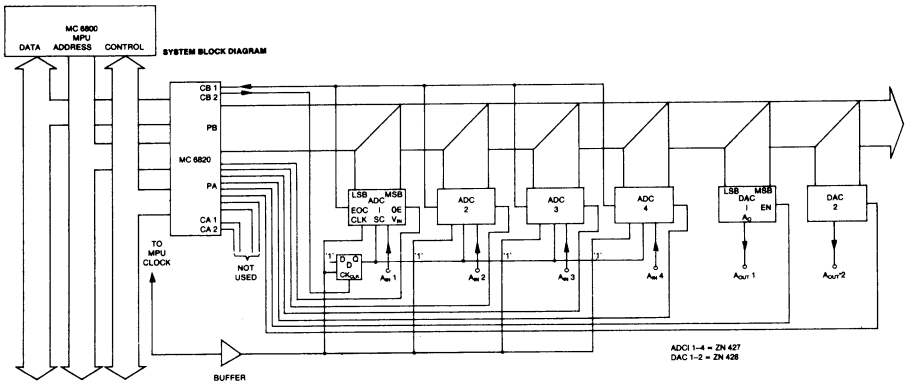


Fig. 1 System Block Diagram

The ZN427 A/D Converter

The ZN427 is an 8-bit, successive approximation A/D Converter. It features fast 15 μs conversion time, three-state outputs to permit bussing on common data lines and no missing codes over the full operating temperature range. The ZN427 contains a voltage switching D/A converter, a 2.5 V precision band gap reference, a fast comparator, successive approximation logic, and three-state output buffers.
Operation of the ZN427 is best described with reference to the timing diagram—Fig. 3. Conversion is initiated by a START CONVERT (SC) pulse which can be applied asynchronously with respect to the ZN427 clock providing the following criteria are met.

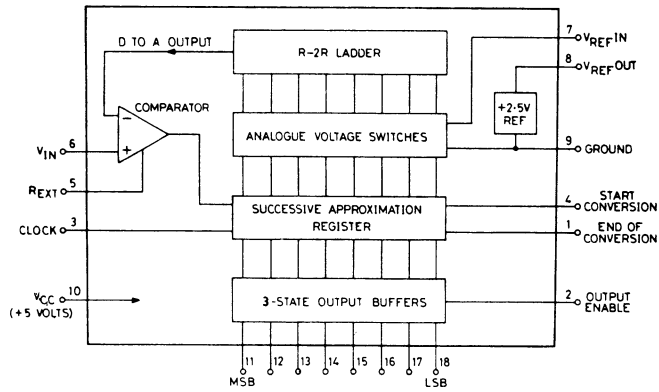


Fig. 2 ZN427 Logic Diagram

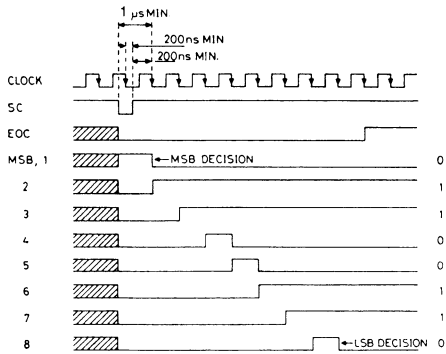


Fig. 3 Timing Diagram

1. The leading edge of the SC–pulse should precede the first active (negative going) edge of the clock (after the trailing edge of the SC pulse) by at least 1.5 μs to allow for MSB setting.
2. The trailing edge of the SC pulse must not occur within ± 200 ns of a negative going edge of the clock.
3. As a special case of conditions (1) and (2) the SC pulse may be coincident with, and of the same duration as, a negative going clock pulse.
   Application of the SC pulse sets MSB to a '1' level and all other bits to a '0', which produces a voltage output from the D to A converter of $V_{REF\ IN/2}$.
   This value is compared with the input voltage V_{IN}, and a decision is made on the first negative clock edge to set the MSB to '0' if $V_{REF\ IN/2} > V_{IN}$, or else to keep it at '1', Bit 2 is switched to '1' on the same clock edge, and on the next edge a decision is made about Bit 2, again by comparing the D/A output with V_{IN}. This process is repeated for all eight bits so that when the END OF CONVERSION (EOC) output goes high the digital output from the converter is a valid representation of V_{IN}. The binary output is latched until the next START pulse. The three-state data outputs are OFF (high impedance) when OUTPUT ENABLE (OE) is an '0' and are enabled when the OE input is taken to '1'.

The ZN428 D/A Converter

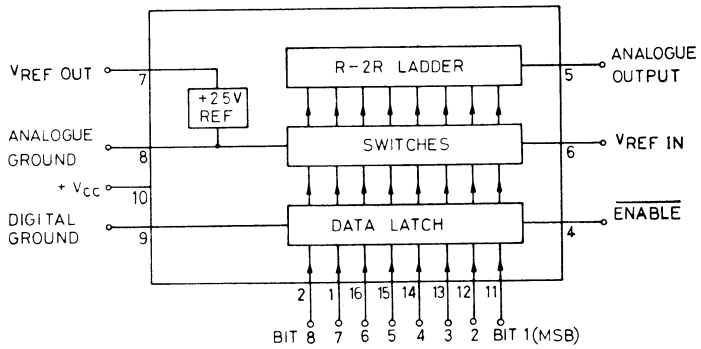


Fig. 4 Logic Diagram

The ZN428 is a monolithic 8-bit D/A converter with input latches to facilitate updating from a data bus. The latch is transparent when $\overline{\text{ENABLE}}$ is at logic '0' and the data is held when $\overline{\text{ENABLE}}$ is taken to logic '1'. The ZN428 features single + 5 volt supply requirements, fast 800 ns settling time and is guaranteed monotonic over the full operating range. It also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted. The converter is of the voltage switching type and uses an R-2R ladder network. Each 2R element is connected to 0 volt or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network the nominal output range of the ZN428 being 0 V to $V_{REF\ IN}$ through a 4 kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The 6800 Microprocessor System

It is assumed that the reader is fully conversant with the 6800 microprocessor family, information on which can be found in the Motorola M6800 Microprocessor Applications Manual, so only a brief description is given here.

The 6800 is an 8-bit monolithic microprocessor which forms the central control function for the 6800 microprocessor family. Fully compatible with TTL the 6800 requires only a single + 5 volt power supply, it features an instruction set of 72 instructions with 7 addressing modes and full 65 k byte memory addressing capability. The microprocessor communicates with its external memory and all I/O devices via an 8-bit bi-directional data bus and a 16-bit address bus.

The 6820/21 Peripheral Interface Adaptor (PIA) provides a flexible means of interfacing byte-orientated peripherals to the microprocessor, through two 8-bit bi-directional peripheral data lines and four control lines. The functional configuration of the PIA is under the full control of the microprocessor. Each of the peripheral data lines can be programmed to act either as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

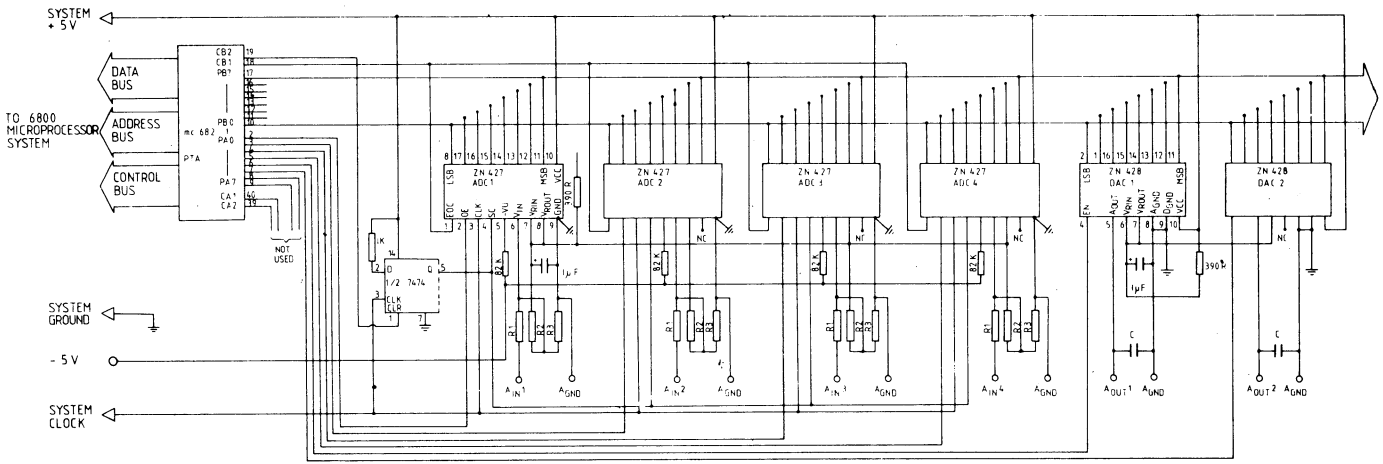
The Analogue I/O Interface

The system described in this application note provides 4 Analogue Input and 2 Analogue Output channels—see the System Block Diagram Fig. 1 and the detailed Circuit Diagram Fig. 5. Other configurations can easily be produced—these are discussed later in this note.

The peripheral data lines PB0—PB7 of the PIA are connected to the binary data outputs of the ZN427s and the data inputs of the ZN428s to produce a common 8-bit data bus for the converters. Peripheral lines PA0—PA5 are programmed as OUTPUTS and provide individual OUTPUT ENABLE and $\overline{\text{ENABLE}}$ signals for the ZN427 and ZN428 respectively. A common, simultaneous START CONVERT signal for the ZN427s is produced from the CB2 control line programmed in the SET/RESET output mode and used in conjunction with a 'D' type flip-flop. The END OF CONVERT outputs from the ZN427s are commoned together and drive the CB1 input of the PIA which can be programmed to generate a microprocessor interrupt signal. In this system configuration, the peripheral lines PA6, PA7 and the control lines CA1, CA2 are not used.

The ZN427 clock signal can be generated either asynchronously from an external source or from the microprocessor clock. If using the MC6871B microprocessor clock device (as supplied with the Motorola MEK6800D2 Evaluation Kit), which produces a 614.4 kHz clock signal, then the ϕ 2 TTL output of this can be used directly. Note that the maximum clock frequency of the ZN427 is specified as 600 kHz, although the device will function up to greater than 1 MHz, but at reduced accuracy due mainly to the response time of the comparator. Therefore, if using a microprocessor with a clock frequency greater than 600 kHz, then this can either be divided down to less than 600 kHz, or it may be used directly up to approximately 1 MHz if some loss of accuracy can be tolerated. The advantage of using the microprocessor clock over an external clock is that it allows an accurate calculation of the conversion time to be made in terms of the microprocessor machine cycles eliminating the need to use microprocessor interrupts.

The START CONVERT pulse is generated using a 'D' type flip flop ($^1/_2$ ZN74L74) in order to meet the timing requirements discussed earlier. A conversion cycle is initiated by outputting a logic '0' followed by a logic '1' from the CB2 line of the PIA. This drives the CLEAR input of the 'D' type and sets the START CONVERT (SC) input of each 427 to a logic '0' via the Q output. The first positive going clock edge after the CLEAR input is returned to a logic '1' will clock the 'D' type and set the SC input of each ZN427 to a '1' allowing the conversion cycle to proceed. Note that while the SC input of the ZN427 is at a logic '0' level the MSB output will be driven to a logic '1' and all other data outputs to a logic '0' and the conversion cycle will be held. On the 9th negative clock edge after the START pulse the END OF CONVERSION outputs will go to a logic '1' signifying the end of the conversion cycle. This can be detected by programming the



NOTE FOR 10 V UNIPOLAR OPERATION -

R1 = 10 K POT + 11 K IN SERIES

R2 = 5 K6

R3 = 1 µ POT + 680 K IN SERIES

FIG 5 - SYSTEM CIRCUIT DIAGRAM

PIA to set the microprocessor interrupt input on the positive going edge of the CB1 control line. The EOC outputs of up to four ZN427s can be "wire or'd" together to produce a common interrupt line as shown in Fig. 5. Alternatively, if using the microprocessor clock (at up to 1 MHz), then the EOC output will always occur within 10 microprocessor machine cycles after the instruction setting the CB2 control line back to a logic '1'. A suitable fixed delay can therefore be built into the program to allow for the conversion time.

The binary output data of each ADC can be read by programming the peripheral lines PB0–PB7 as INPUTS and loading the data onto the converter bus by outputting a logic '1' on the appropriate PA peripheral line in order to enable the 3-state output buffers of the ADC. A microprocessor read instruction of the PIA peripheral register 'B' will then transfer the data to the microprocessor. Obviously the program should be so arranged that, in order to avoid bus contention problems, only one ADC is enabled at any one time.

The circuit diagram, Fig. 5 shows the ZN427s connected for a unipolar input range of 0 to + 10 volts. Other ranges, eg + 5 V, ± 10 V and ± 5 V, can readily be obtained by using a simple resistor network as shown in the ZN427 data sheet.
The negative supply shown for the ZN427 is from − 5 volts through an 82 kΩ resistor. By suitable choice of resistor value any negative supply between − 3 and −30 volts may be used. For applications where only a single + 5 volt supply is available, a simple diode pump circuit can be used to generate the negative supply. Further information on the negative supply and a diode pump circuit suitable for up to 5 ZN427s is shown in the data sheet.

Data is outputted from the system by programming the peripheral data lines PB0–PB7 as OUTPUTS and writing the binary data from the microprocessor into the PIA peripheral register 'B'. The $\overline{\text{ENABLE}}$ input of the relevant ZN428 is driven to a logic '0' and back to logic '1' via the appropriate PA peripheral line, which will transfer the data from the converter bus to the input data latches of the ZN428. Again the programmer must ensure during an output data transfer that all the ZN427s and the other ZN428 are disabled.

The Analogue Outputs of the ZN428 are shown, taken directly from pins 5 and 8 which will provide an output range from 0 volts to $V_{REF\ IN}$ through a 4 kΩ output resistance. A small capacitor can be connected across the output pins as shown in order to remove any "glitches" which may be present. The value of this capacitor depends on the system noise and the response time required, however for the minimum specified settling time it should not be greater than 100 pF. An output buffer amplifier was omitted from the ZN428 design in order to allow optimum settling time, flexibility and lowest cost. Both Unipolar and Bipolar output ranges can readily be obtained by using an external amplifier, details of which are given in the ZN428 data sheet.

The ZN428 is provided with separate Analogue and Digital ground pins. These can normally be connected together close to the device and taken to signal ground. However for noisy systems or environments it may be advisable to keep the Analogue ground pins for each individual ZN428 separate from the Digital ground pin, and to connect each Analogue ground to a single common earth point in the system away from sources of digital noise such as clock oscillators, digital buses, etc. The Analogue output ground line or terminal should also be taken direct to this common earth point. (Note: The maximum voltage between Analogue and Digital grounds is limited to 200 mV.)

A common reference voltage can be provided by connecting the $V_{REF\ OUT}$ pin of one converter to the $V_{REF\ IN}$ pins of up to five converters (i.e. either ZN427s or ZN428s). This useful feature saves power and gives excellent gain tracking between converters. Fig. 5 shows the four ZN427s driven from one internal reference and the two ZN428s from another.

Note that in this application the dynamic characteristic of the ZN427/428 (i.e. Enable/Disable delay times, etc.) should not present any problems since they are much less than the microprocessor instruction execution times and need not be considered in the programming.

Program Example
A simple program which illustrates the ease of controlling the ZN427/428 with the PIA is shown on page together with the Flow Diagram, Fig. 6. The object of the program is to read the analogue voltage inputs to ADCs 1 and 2, calculate the mean value and output this on DAC1. A similar operation is performed on the inputs of ADCs 3 and 4 and outputted on DAC2.

It is assumed that the PIA has been reset which has the effect of zeroing all the PIA registers. This sets all the peripheral and control lines as INPUTS and disables the interrupts. Initially the Index Register is loaded with the PIA base address in order that the Indexed Addressing Mode can be used throughout the program to address the PIA. The peripheral lines PA0–PA7 are programmed as OUTPUTS and the Control Registers set so that control line CB2 operates in the SET/RESET output mode and the interrupt Flag bit CRB-7 is set with a positive going edge on control line CB1. All the converters are disabled by outputting 30H on the PA lines which sets the OUTPUT ENABLE inputs of the ZN427s to a logic '0' and the $\overline{\text{ENABLE}}$ inputs of the ZN428s to a logic '1'. A dummy read is made of the B Data Register to clear the Interrupt Flag bit CRB-7.

A START signal is then generated via control line CB2 by toggling bit CRB-3 in Control Register B. The end of the conversion cycle is detected by testing the Interrupt Flag bit CRB-7 and looping at this point in the program until it goes to a '1'. (Note: The microprocessor interrupt request lines $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ are disabled.) The output of ADC1 is now read by driving peripheral line PA0 to a logic '1', and the data is stored in the microprocessor Accumulator B, ADC2 is read in a similar way by setting PA1 line to a logic '1' and storing the data in Accumulator A. The mean value of the readings is found by adding the Accumulators and rotating the result right, one bit through carry, this is equivalent to dividing by 2. The result is saved in the memory location labelled 'TEMP 1'. The process is repeated on ADC3 and ADC4, enabling the ADC outputs by setting lines PA2 and PA3 in turn to a logic '1', and storing the computated result in location 'TEMP 2'.

The Data Direction Register B is now accessed and the peripheral lines PB0–PB7 changed to OUTPUTS. The data stored in 'TEMP 1' is outputted onto the converter bus and DAC 1 enabled by toggling line PA4 in a logic 1-0-1 sequence, which will transfer the binary data from the bus to the DAC input latches and hence to the Analogue Output. A similar sequence is performed on DAC2 with the data from 'TEMP 2', using PA5 line to drive the $\overline{\text{ENABLE}}$ input. The program is terminated with a Software Interrupt, SWI, returning control to the Monitor Program.

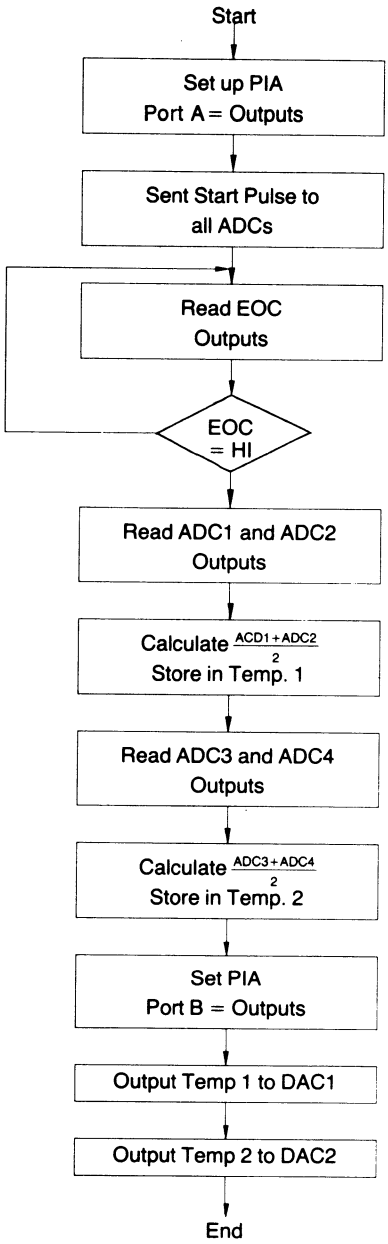


FIG. 6 PROGRAMME FLOW DIAGRAM

PIA PORT ALLOCATIONS

PORT A

PA0	ADC1 OE Input
PA1	ADC2 " "
PA2	ADC3 " "
PA3	ADC4 " "
PA4	DAC1 $\overline{EN}$ Input
PA5	DAC2 " "
PA6	NOT USED
PA7	NOT USED

PORT B

PB0	BINARY DATA	LSB
PB1	" "	LSB + 1
PB2	" "	LSB + 2
PB3	" "	LSB + 3
PB4	" "	LSB + 4
PB5	" "	LSB + 5
PB6	" "	LSB + 6
PB7	" "	MSB

CONTROL

CA1	NOT USED
CA2	NOT USED
CB1	COMMON EOC OUTPUT
CB2	COMMON START LINE

PIA ADDRESSES

8004	PERIPHERAL/DATA DIRECTION REG. A
8005	CONTROL REG. A
8006	PERIPHERAL/DATA DIRECTION REG. B
8007	CONTROL REG. B

6800/6820 I/O INTERFACE – PROGRAM EXAMPLE

LOC	OBJ		COMMENT	SOURCE STATEMENT
0000	CE8004		LDX #$8004	Load PIA address to IX
3	86FF		LDA A #$FF	
5	A700		STA A 0, X	Set Port A as outputs.
7	863E		LDA A #$3E	
9	A701		STA A 1, X	Set Control Reg. A
B	A703		STA A 3, X	Set Control Reg. B
D	8630		LDA A #$30	
F	A700		STA A 0, X	Disable Converters
11	A602		LDA A 2, X	Dummy read to Clear Flag
13	8636		LDA A #$36	
15	A703		STA A 3, X	Set CB2 Low to
17	863E		LDA A #$3E	Generate Start Pulse
19	A703		STA A 3, X	Set CB2 High
1B	A603	TEST	LDA A 3, X	Read Control Reg. B
1D	8580		BIT A #$80	Test for CRB-7 High
1F	27FA		BEQ TEST	ie End of Conversion
21	8631		LDA A #$31	
23	A700		STA A 0, X	Enable ADC1 O/Ps
25	E602		LDA B 2, X	Read ADC1 O/P
27	8632		LDA A #$32	
29	A700		STA A 0, X	Enable ADC2 O/Ps
2B	A602		LDA A 2, X	Read ADC2 O/P
2D	1B		ABA	Add ADC1 + ADC2 Readings
2E	46		RORA	Divide by 2
2F	976E		STA A Temp.1	Save x in Temp. 1
31	8634		LDA A #$34	
33	A700		STA A 0, X	Enable ADC3 O/Ps
35	E602		LDA B 2, X	Read ADC3 O/P
37	8638		LDA A #$ 38	
39	A700		STA A 0, X	Enable ADC4 O/Ps
3B	A602		LDA A 2, X	Read ADC4 O/P
3D	1B		ABA	Add ADC1 + ADC2 Readings
3E	46		RORA	Divide by 2
3F	976F		STA A Temp.2	Save y in Temp. 2
41	8630		LDA A #$30	
43	A700		STA A 0, X	Disable ADC O/Ps
45	863A		LDA A #$ 3A	
47	A703		STA A 3, X	
49	86FF		LDA A #$FF	
4B	A702		STA A 2, X	Set Port B as outputs
4D	863E		LDA A #$ 3E	
4F	A703		STA A 3, X	
51	966E		LDA A Temp. 1	
53	A702		STA A 2, X	Put x Data on bus
55	8620		LDA A #$20	
57	A700		STA A 0, X	Enable DAC1 I/Ps
59	C630		LDA B #$30	
5B	E700		STA B 0, X	Disable DAC1 I/Ps
5D	966F		LDA A Temp. 2	
5F	A702		STA A 2, X	Put y data on bus
61	8610		LDA A #$10	
63	A700		STA A 0, X	Enable DAC2 I/Ps
65	E700		STA B 0, X	Disable DAC2 I/Ps
67	3F		SWI	End
006E	00		Temp. 1	x data
006F	00		Temp. 2	y data

Summary

The system described in this report is by no means restricted to the configuration shown. Provided that the drive capability of the system components is not exceeded, the number and configuration of ZN427s and ZN428s which can be employed is limited only by the I/O lines available from the PIA, hence providing the Design Engineer with a wide degree of freedom in producing the system that best fulfils his requirements.

The major loading and drive characteristics of the various system components are shown in Table 1. Buffer gates can be employed where necessary to expand the drive capability of the components such as when utilising a long bus with high capacitive loading. Note that the peripheral lines from side B are used for the converter bus since these present a high impedance when programmed as inputs. Also the 6821 PIA is preferred to the 6820 because this has a 2-TTL drive capability on both A and B side peripheral lines. As stated previously up to 4 ZN427 EOC outputs can be wire–or'd together; if using more than 4, then each group can be ANDed together using a ZN7409 TTL gate to produce a single interrupt line.

If required separate START signals can be generated for each ZN427 hence allowing a microprocessor read of one ADC to be in progress while the other(s) are in a conversion cycle. However this configuration does require one peripheral line and one 'D' type flip flop per START signal line. Since only one ZN427 or ZN428 should be enabled at any one time, then it is possible to incorporate one or more Decoder types of I.C. such as the ZN74154, 4 Line to 16 Line Demultiplexer/Decoder in order to expand the system. This device could be connected with the 4 data inputs connected to 4 PA peripheral lines and the decoder enable input driven by CA2 line. Use of two such IC's would provide 32 output lines allowing an Analogue I/O system with a combination of up to 32 analogue input and output channels to be produced.

As a result of the low converter cost, low external component count and flexibility of this type of system, designs based on using one converter per analogue channel will be both a practical and economical solution to microprocessor data acqusition problems. This approach should find many new applications in areas which have previously been limited by the necessity of having to use the traditional data acqusition methods involving a single, high cost hybrid A-D converter utilising sample/hold and multichannel multiplexing techniques.

TABLE 1

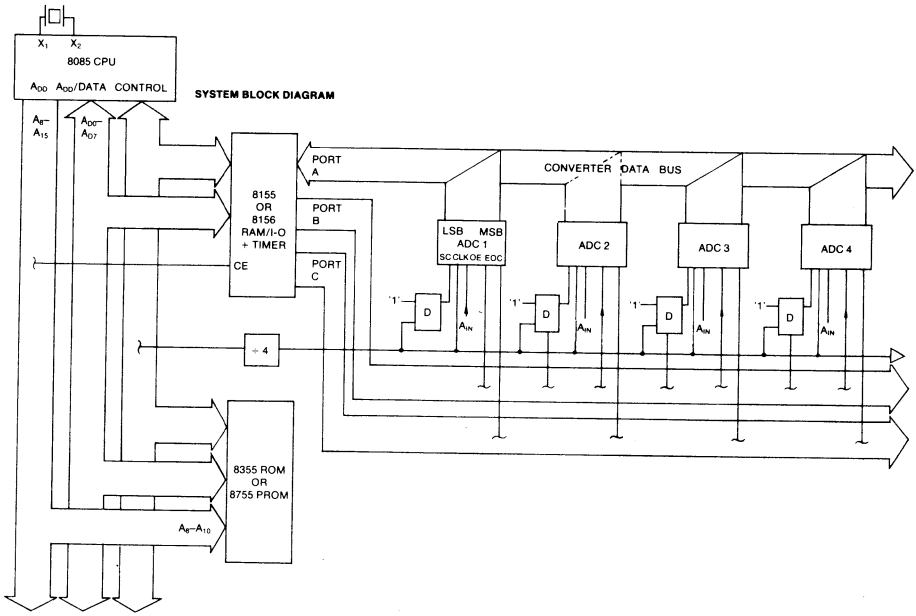
MC6820	PA0 - PA7 / CA2	PB0 - PB7 / CB2	CA1/CB1
I_{IL} I_{IH}	-1.6mA max -100μA min	) 10μA max)	) 2.5μA max) (at V_{IN} = 0 to 5.25V))
I_{OL}	1.6mA min	1.6mA min	
I_{OH}	-100μA min	-100μA min	
MC6821			
I_{IL} I_{IH}	-2.4mA max -200μA min	) 10μA max)	) 2.5μA max) (at V_{IN} = 0.5... 5.25 V))
I_{OL}	3.2mA min	3.2mA min	
I_{OH}	-200μA min	-200μA min	
ZN427			
I_{IL}	-5μA max		
I_{IH}	15μA max		
I_{IH} (Clock)	30μA max		
I_{OL}	1.6mA min		
I_{OH}	-100μA min		
I_{OHX} (Off state leakage)	2μA max		
ZN428	All Inputs		
I_{IL}	-5μA max		
I_{IH}	20μA max		

NOTE Currents specified at 0.4 V and 2.4 V unless otherwise stated.

Interfacing the ZN 427 A to D Converter with the 8085A Microprocessor System

by SCOTT BIRD, Ferranti Electronics Ltd.

The growth of microprocessors has lead to a demand for low cost, fast 8 bit A/D and D/A converters to interface between the real world of analogue values and the digital world of the microprocessor. Converter systems have, until recently, been mainly high cost, multiplexed, sample and hold systems usually built around a 12 bit A/D converter. The system described in this report is a low cost, expandable, one converter per channel system, based on the ZN427 8-bit A/D Converter interfaced directly to the I/O Ports of the 8155 2K bit static 'RAM', which forms part of the basic 8085A microprocessor system.



The ZN427 A/D Converter

The ZN427 is a monolithic 8-bit, successive approximation A/D Converter designed for microprocessor compatibility. It features fast 15 μs conversion time, three-state outputs to permit bussing on common data lines and no missing codes over the full operating temperature range. The ZN427 contains a voltage switching D/A converter, a 2.5 V precision band gap reference, a fast comparator, successive approximation logic, and three-state output buffers.

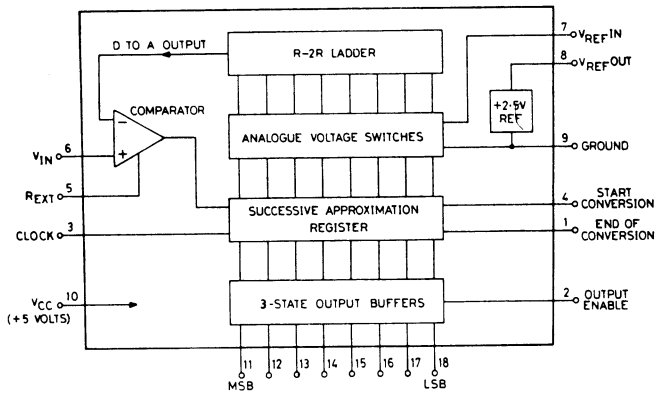


Fig. 2—ZN427 Logic Diagram

Operation of the ZN427 is best described with reference to the timing diagram.—Fig 3. Conversion is initiated by a Start Convert (SC) pulse which can be applied asynchronously with respect to the ZN427 clock providing the following criteria are met.

1. The leading edge of the SC—pulse should precede the first active (negative going) edge of the clock (after the trailling edge of the SC pulse) by at least 1.5 μs to allow for MSB setting.
2. The trailing edge of the SC pulse must not occur within ± 200 ns of a negative going edge of the clock.
3. As a special case of conditions (1) and (2) the SC pulse may be coincident with, and of the same duration as, a negative going clock pulse.
   Application of the SC pulse sets MSB to a '1' level and all other bits to a '0', which produces a voltage output from the D to A converter of $V_{REFIN}/2$. This value is compared with the input voltage V_{IN}, and a decision is made on the first negative clock edge to set the MSB to '0' if $V_{REFIN}/2 > V_{IN}$, or else to keep it at a '1'. Bit 2 is switched to a '1' on the same clock edge, and on the next edge a decision is made about bit 2, again by comparing the D/A output with V_{IN} This process is

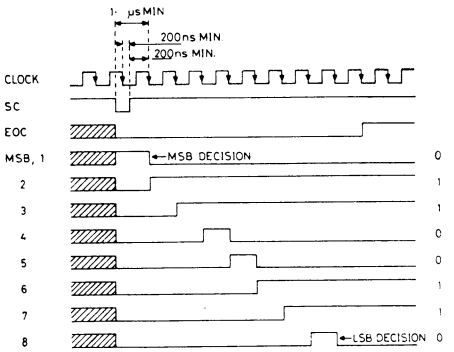


Fig. 3—Timing Diagram

repeated for all eight bits so that when the END OF CONVERSION (EOC) output goes high the digital output from the converter is valid representation of V_{IN}. The binary output is latched until the next START pulse. The three-state data outputs are OFF (high impedance) when OUTPUT ENABLE (OE) is a '0' and are enabled when the OE input is taken to a '1'.

The 8085A Microprocessor System

It is assumed that the reader is totally familiar with the 8085A microprocessor system, information on which can be obtained from the MCS-85 USERS MANUAL, so only a brief description is given here.

The 8085A is a complete 8-bit parallel central processing unit. A minimum component 8085 microcomputer system can be built from just three chips—the 8085A CPU, a 8355 or 8755 ROM or PROM, and a 8155 or 8156 RAM/TIMER/I-O chip. The 8155/8156 provides, in addition to 2k bits of Static RAM, two programmable 8-bit I/O Ports, one programmable 6-bit I/O Port and a programmable 14-bit binary timer counter. (The difference between the 8155 and the 8156 is that on the 8155 the CHIP ENABLE is active LOW, and on the 8156 it is active HIGH.)

The ZN427 Interface

This application note describes how up to 4, ZN427 ADCS can be connected to the I/O Ports of one 8155 RAM to provide 4 Analogue Input Channels to the microprocessor system. Since most 8085 based systems including the SDK-85 System Design Kit will incorporate one or more 8155s, then the addition of Analogue Input Channels would involve minimum additional hardware and design effort. An advantage of using the 8155 I O Ports is that no additional address decoding or bus demultiplexing and buffering hardware is necessary.

For existing systems, if spare I O Ports are available then analogue inputs can easily be added without any major modifications to the hardware. Also the expansion of the number of input channels to a system by addition of extra 8155s should be easily implemented since this device is directly bus compatible with the 8085A.

The 8155 I O Ports are allocated as shown in the Logic Diagram, Fig. 1. Port A is programmed as INPUTS and provides an 8-bit data bus which connects to the three-state binary data outputs of each ZN427. Port B is programmed as OUTPUTS, the lower 4-bits provide the start convert and the upper 4-bits provide the Output Enable Signals to each ZN427. The END OF CONVERT output of each ZN427 is connected to a Port C pin, which are programmed as INPUTS to provide the individual BUSY FLAGS for each ZN427. Note that only 4- of the 6-bits available from Port C are used.

The ZN427 clock can be supplied either from an external source or from the 8085A CLOCK OUTPUT. Since the 8085A clock will normally be at 3 MHz, it will be necessary to divide this down by at least a factor of 4. This is achieved in the circuit, see Fig. 4, by means of a dual JK Flip Flop (7473) connected as a 2-bit binary counter. (Note: This will provide a clock frequency of 750 kHz which is a little higher than the ZN427 clock freqency spec. minimum of 600 kHz. However, for most practical applications the loss in accuracy due to this will be minimal.) An external clock could be used for the ZN427 but the advantage of using the microprocessor clock is that it allows an accurate calculation of the ZN427 conversion time to be made in terms of the microprocessor CLOCK CYCLES (or 'T' STATES).

(Note: To avoid confusion, future reference to 'clock' will mean the ZN427 clock signal unless specifically stated otherwise.)

The START CONVERT pulse is generated using a 'D' type Flip Flop ($^1/_2$ 7474) in order to meet the timing requirements discussed earlier. A conversion cycle is started by outputting a '0' followed by a '1' from the appropriate Port B output to the CLEAR input of the 'D' type which sets the SC input of the ZN427 to '0'. The first positive going clock edge after the CLEAR input is returned to a '1' clocks the 'D' type and sets the SC input to '1'. This sequence is illustrated in the Start Pulse Timing Diagram, Fig. 5.

On the 9th negative clock edge after the Start Pulse the END OF CONVERT output goes to a '1' signifying the end of the conversion process, this can be detected by an I/O read on Port C. However, when generating the ZN427 clock from the microprocessor clock as shown, the EOC output will always occur within 35 microprocessor clock cycles after the OUT instruction returning the SC input to a '1'. In this case it is not

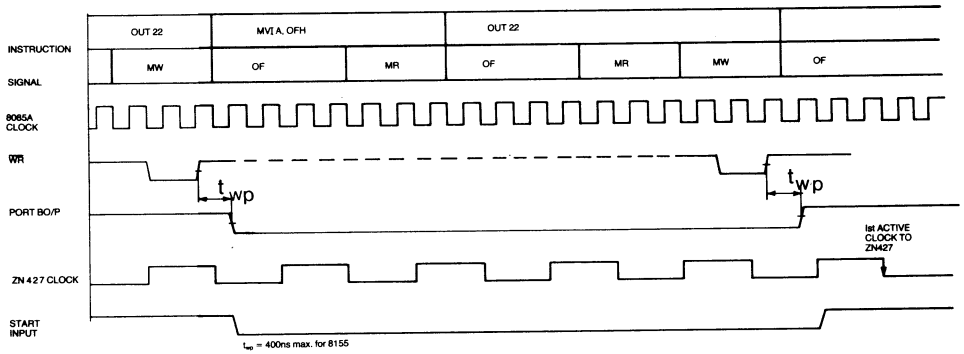


FIG. 5 START PULSE TIMING DIAGRAM

necessary to poll the EOC outputs, the ZN427 data outputs can be read after a suitable fixed delay in the programme. For application where processor time is at a premium or if immediate response is required to an EOC output, a microprocessor interrupt can be generated by connecting the EOC output direct to one of the 8085A restart inputs. The EOC outputs of to 4-ZN427s can be 'wire-OR'd' to produce a common interrupt line. Usually, however, the fast conversion time of the ZN427 (15 μs) will make it not worthwhile to employ microprocessor interrupts since the conversion time takes less than 6/7 typical microprocessor instructions.

The binary output data is applied via the converter data bus to Port A of the 8155 by driving the OE output to a '1' from the appropriate Port B bit. Obviously the programme should be arranged so that the outputs of only one ZN427 are enabled at any one time, in order to avoid bus contention problems. Note that in this application the Output Enable and Disable switching times (which are specified at 250 ns max.), need not be considered since they are much less than the instruction execution times.

The circuit diagram, Fig. 4 shows the ZN427s connected for a unipolar input range of 0 to + 10 V. Other ranges, e.g. + 5 V, ± 10 V, and ± 5 V can be readily obtained by using the appropriate resistors as shown in the ZN427 data sheet. Note also that the reference, $V_{REF\ IN}$, of up to five ZN427s may be driven from one internal reference. This useful feature saves power, discrete components, and gives excellent gain tracking between the converters.

In the circuit the negative supply to the ZN427s is through an 82K resistor from − 5 V. By suitable choice of resistor any negative supply of − 3 to − 30 volts may be used. For applications where only a positive 5 volt supply is available, a simple diode pump circuit suitable for up to 5-ZN427s is shown in the ZN427 data sheet.

Programme Example

A simple programme is given on page 9 together with the flow diagram in Fig. 6, which illustrates the ease of controlling and reading the ZN427 with the 8155 I/O Ports.

Following the flow diagram it is seen that after initialisation of the stack pointer the I/O Ports of the 8155 are defined—Ports A and C as INPUTS, Port B as OUTPUTS. A simultaneous START CONVERT pulse is sent to all the ADCs by outputting logic '0' folowed by logic '1' to the lower 4-bits of Port B. The EOC outputs of the ADCs are then read via Port C and tested for a logic '1/ to check if the conversion process has finished. The microprocessor will loop on this part of the programme until the EOC output of all the ADCs go to '1'. When this occurs the programme proceeds by enabling the outputs of each ADC in turn and reading the binary data via Port A. The ADC outputs are enabled in turn by outputting a logic '1' to each of the upper 4-bits of Port B (keeping the other 3-bits at '0' and the lower 4-bits at a '1'). The data from each ADC is stored in consecutive memory locations, starting at the address labelled 'DATA'. The H and L register pair hold the memory address at which data is to be saved; these are incremented for each read of an ADC.

This programme could easily be modified to act as a sub-routine for another main programme. As mentioned previously a fixed delay could be substituted for the programme loop which tests the EOC outputs. Also instead of generating a simultaneous START pulse separate START signals may be sent to each ADC at different times in a control cycle.

Summary

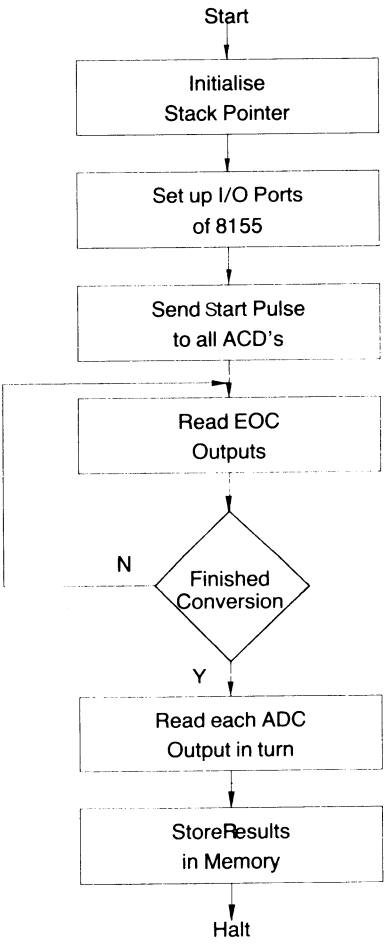
The system described in this report should be suitable for most applications since it allows complete control of each individual ADC. However, the configuration can easily by changed for particular requirements,—a few ideas are briefly described below.

1. If a simultaneous START pulse is adequate, then the START CONVERT inputs of the ZN427s can be commoned together and driven via one 'D' type from one Port output.
2. The EOC outputs of up to 4-ZN427s can be commoned and either taken to one Port input or used as a microprocessor interrupt signal.
3. Adoption of methods 1 and/or 2 above would use less 8155 Port bits and hence allow more ZN427s to be connected to each 8155.
4. Instead of generating the START pulse from the 8155 it could be asynchronously produced externally by a process timer, photo transistor or proximity detector circuit etc., the only timing requirement being that the pulse width fed to the CLEAR input of the 'D' type is at least half a clock period. (i.e. 640 ns with a 320 ns microprocessor clock) or 1.5 μs, whichever is smaller.
5. If D/A channels as well as A/D are required in one system then ZN428, 8-bit D/A Converters can be mixed on the same converter data bus as the ZN427. This will allow a designer to tailor a system to his specific A/D and D/A requirements. (See FERRANTI APPLICATION NOTE ANO11 for details of interfacing the ZN428 to the 8155.)

It is hoped that after reading this application note, the reader will have a much better insight into the operation and versatility of the ZN427, and into how it can easily be interfaced to a microprocessor system.

In order to avoid duplication only the relevant ZN427 characteristics were discussed in this report. For a full description and specification of the ZN427 please refer to the data sheet.

FIG. 6 PROGRAMME FLOW DIAGRAM



8155 PORT ALLOCATIONS

PORT A

PA0	Binary Data LSB
PA1	Binary Data LSB + 1
PA6	Binary Data MSB - 1
PA7	Binary Data MSB

PORT B

PB0	ADC1 SC Input
PB1	ADC2 SC Input
PB2	ADC3 SC Input
PB3	ADC4 SC Input
PB4	ADC1 OE Input
PB5	ADC2 OE Input
PB6	ADC3 OE Input
PB7	ADC4 OE Input

PORT C

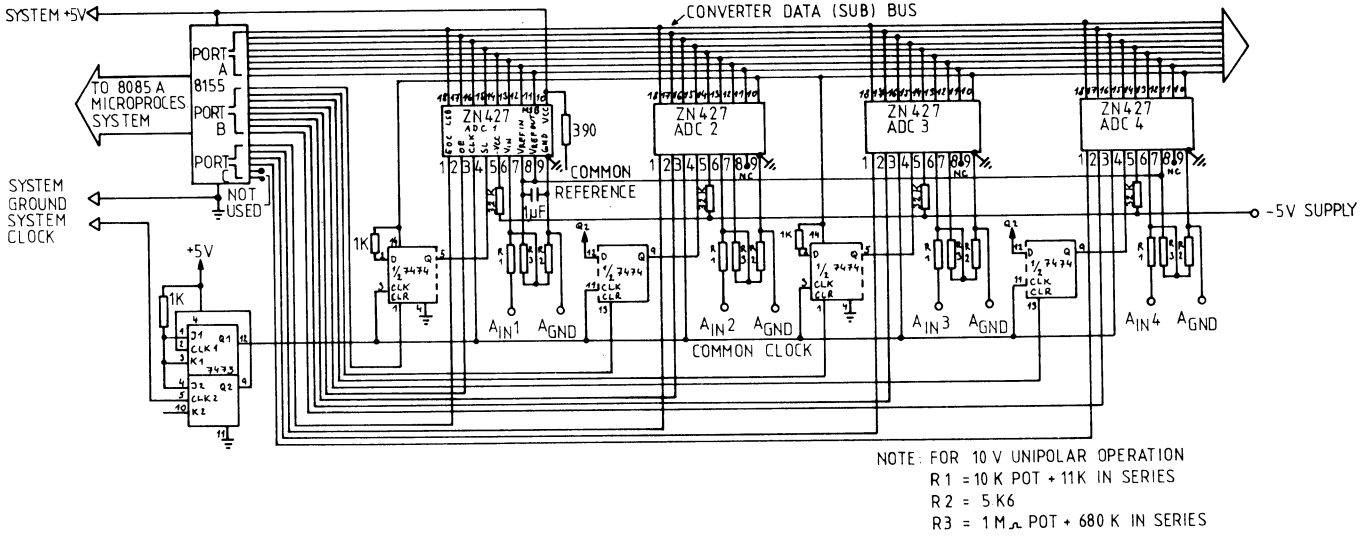
PC0	ADC1 EOC Output
PC1	ADC2 EOC Output
PC2	ADC3 EOC Output
PC3	ADC4 EOC Output

I/O PORT ADDRESSES

20	Command/Status Reg
21	RAM Port A
22	RAM Port B
23	RAM Port C

ZN427 – 8085A PROGRAMME EXAMPLE

LOC	OBJ	SOURCE STATEMENT		
2000	31C820		LXI SP, 20C8	Initialise Stack Pointer
2003	3E02		MVI A, 02H	Define I/O Ports
2005	D320		OUT 20	
2007	3E00		MVI A, 00H	
2009	D322		OUT 22	Send Start To All ACD s
200B	3EOF		MVI A, OFH	
200D	D322		OUT 22	
200F	060F		MV1 B OFH	
2011	DB23	LOOP:	IN 23	Read EOC s
2013	AO		ANA B	Strip Upper 4 Bits
2014	B8		CMP B	Test If All EOC s
2015	C21720		JNZ LOOP	Are A '1'
2018	213B20		LXI H, DATA	
201B	3EIF		MVI A, 1FH	
201D	D322		OUT 22	Enable ADC 1
201F	DB21		IN21	Read ADC 1
2021	77		MOV M, A	Save In Loc, DATA
2022	23		INX H	Increment Pointer
2023	3E2F		MVI A 2FH	
2025	D322		OUT 22	
2027	DB21		IN21	Read ADC 2
2029	77		MOV M, A	Save In LOC. DATA + 1
202A	23		INX H	
202B	3E4F		MVI A 4FH	
202D	D322		OUT 22	
202F	DB21		IN 21	Read ADC 3
2031	77		MOV M,A	Save In Loc DATA + 2
2032	23		INX H	
2033	3E8F		MVI A 8 FH	
2035	D322		OUT 22	
2037	DB 21		IN 21	Read ADC 4
2039	77		MOV M, A	Save In Loc. DATA + 4
203A	76		HLT	
203B		DATA:		
203C				
203D				
203E				


SYSTEM +5V
TO 8085 A MICROPROCES SYSTEM
PORT A
8155
PORT B
PORT C
NOT USED
SYSTEM GROUND
SYSTEM CLOCK
+5V
1K
7473
CONVERTER DATA (SUB) BUS
ZN427 ADC 1
ZN427 ADC 2
ZN427 ADC 3
ZN427 ADC 4
390
COMMON
REFERENCE
1µF
7474
$A_{IN}1$
A_{GND}
$A_{IN}2$
A_{GND}
$A_{IN}3$
A_{GND}
$A_{IN}4$
A_{GND}
COMMON CLOCK
-5V SUPPLY
NOTE: FOR 10 V UNIPOLAR OPERATION
R1 = 10 K POT + 11K IN SERIES
R2 = 5·K6
R3 = 1 MΩ POT + 680 K IN SERIES

Interfacing the ZN 428 D to A Converter with the 8085A Microprocessor System

by SCOTT BIRD, Ferranti Electronics Ltd.

The growth of the microprocessor has led to a demand for low cost, 8-bit A/D and D/A converters to interface between the real world of Analogue values and the Digital world of the microprocessor. This report values a simple, low cost, expandable multichannel D/A system based on the ZN428, 8-bit D/A converter interfaced directly to the I/O Ports of the 8155, 2K bit static RAM, which forms part of the basic 8085 microprocessor system.

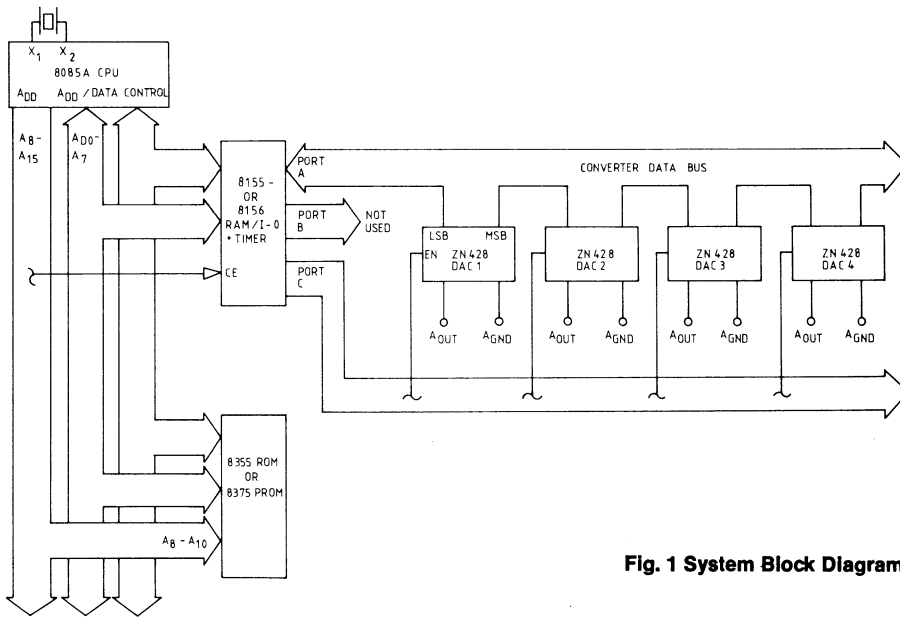


Fig. 1 System Block Diagram

The ZN428 D/A Converter

The ZN428 is a monolithic 8-bit D/A converter with input latches to facilitate updating from a data bus. The latch is transparent when $\overline{\text{ENABLE}}$ is at logic '0' and the data is held when $\overline{\text{ENABLE}}$ is taken to logic '1'. The ZN428 features single + 5 volt supply requirements, fast 800 ns setting time and is guaranteed monotonic over the full operating range. It also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

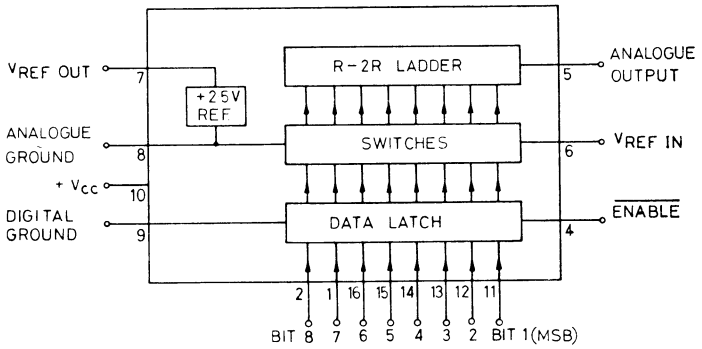


Fig. 2 ZN428 Logic Diagram

The converter is of the voltage switching type and uses an R-2R ladder network. Each 2R element is connected to 0 volt or V ref IN by transistor voltage switches specially designed for low offset voltage (1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network the nominal output range of the ZN428 being 0 volt to $V_{REF\ IN}$ through a 4 kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The 8085A Microprocessor System

It is assumed that the reader is totally familiar with the 8085A microprocessor system, information on which can be obtained from the MCS-85 USERS MANUAL; so only a brief description is given here.

The 8085A is a complete 8-bit, parallel central processing unit. A minimum component 8085A microcomputer system can be built from just three I.C.s—the 8085A CPU, an 8355 or 8755 ROM or PROM, and a 8155 or 8755 RAM/TIMER/I-O I.C. The 8155/8156 in addition to 2K Bits of Static RAM, provides two programmable 8-bit I/O Ports, one programmable 6-bit I/O Port and a programmable 14-bit binary timer counter. (The difference between the 8155 and 8156 is simply that on the 8155 the CHIP ENABLE is active LOW and on the 8156 it is active HIGH.)

The ZN428 Interface

This application report describes how one or more ZN428 DACs can be connected directly to the I/O Ports of an 8155 RAM to provide analogue output channels from the microprocessor system.

Since most 8085 based systems, including the SDK-85 System Design Kit, will incorporate one or more 8155s then the addition of Analogue output channels can be made with the minimum of extra hardware and design effort. An advantage of using the 8155 I/O Ports is that no additional address decoding or bus multiplexing and buffering hardware is necessary. For existing systems, if spare I/O Ports are available then analogue outputs can easily be added without major modifications to the hardware.

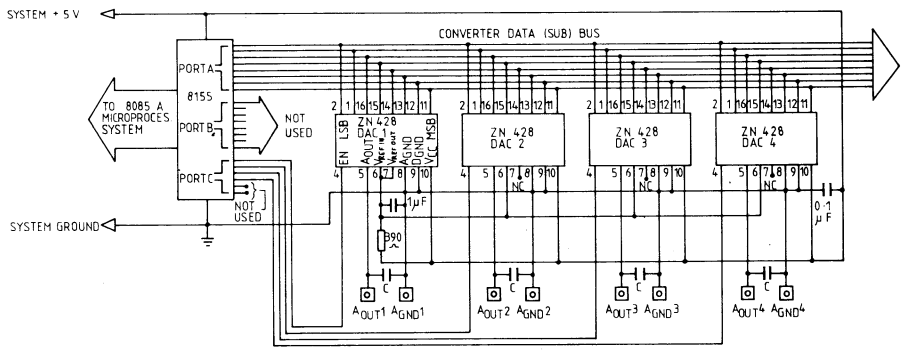
Also expanding the number of output channels by means of addition of extra 8155s should be easy to implement, since the 8155 is directly bus compatible with the 8085A. Figure 3 shows 4—ZN428s connected to the I/O Ports of one 8155. Port A is programmed as OUTPUTS and provides a common 8-bit data bus which is connected to the binary data inputs of each ZN428. The $\overline{\text{ENABLE}}$ inputs of each ZN428 are connected to separate pins on Port C which is also programmed as OUTPUTS. Note that in this configuration only 4 of the 6 Port C pins are used and Port B is also unused.

The reference voltage of all converters is provided by connecting the V_{REF} OUT pin of one ZN428 to the V_{REF} IN pins of all the ZN428s as shown. This useful feature saves power, components and gives excellent gain tracking between converters. Up to five ZN428s may be driven from one internal reference in this way.

The circuit, Fig. 3, shows the outputs of the ZN428s taken directly from pins 5 and 8. This will provide an output range of 0 volt to V_{REF} IN through a 4 kΩ output resistance. A small capacitor can be connected across the output pins as shown in order to remove any "glitches" which may be present. The value of this capacitor depends on the noise in the system and the response time required, however, for the minimum settling time it should not be greater that 100 pF. The output buffer amplifier was omitted from the ZN428 in order to allow greatest system speed, flexibility and lowest cost. Both Unipolar and Bipolar output ranges can readily be obtained by using an external amplifier, details of which are given in the ZN428 data sheet.

The ZN428 is provided with separate Analogue and Digital ground pins. These can be connected together close to the I.C. pins. However, for noisy systems or environments it may be better to keep the Analogue ground pins for each individual ZN428 separate from the Digital ground, and to connect each Analogue ground to a single common earth point in the system, away from sources of digital noise such as clock oscillators, digital buses etc. The Analogue ground output line or terminals should also be taken direct to this common earth point. (Note: The maximum voltage between Analogue and Digital grounds is limited to 200 mV.)

Data is fed to a converter simply by outputting the binary data onto the common bus from Port A of the 8155. The appropriate output from Port C is then driven to a logic '0' level then back to a logic '1'. This will transfer the binary data on the bus into the input latches of the ZN428. The $\overline{\text{ENABLE}}$ inputs of converters which are not being updated are held at logic '1'. The data from Port A can now be changed and the next converter updated as and when required as determined by the controlling programme of the microprocessor. Note that in this application the Data Set-up and Data Hold times and Enable pulse widths need not be considered since they are much less than the microprocessor instruction execution times.



NOTE FOR VALUE OF C PLEASE REFER TO TEXT

Programme Example

A simple programme is given on page 6 together with the flow diagram in Fig. 4, which illustrates the ease of controlling the ZN428 in conjunction with the 8155 I/O Ports.

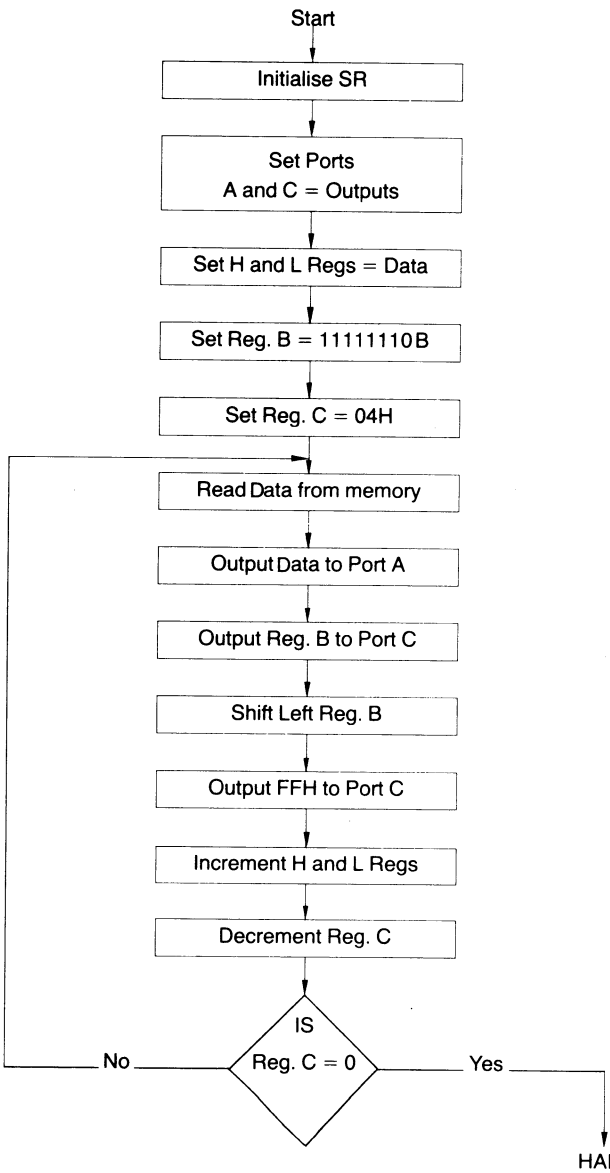
The object of the programme is to read the binary data from four successive memory locations and to output this data sequentially to each of the four DACs. In practice this programme would probably act as a sub-routine outputting data derived from some external source and operated on by the main programme.

With reference to the flow diagram Fig. 5 it is seen that after initialisation of the stack pointer the I/O Ports A and C are defined as OUTPUTS. The H and L register pair are loaded with the starting address in memory of where the data to be outputted is stored. Register B determines which DAC is to be enabled, this is set initially to 11 111 110; while Register C, which acts as a loop counter is set to 4. Data is then read from memory into the Accumulator using the H and L registers in the Register Indirect addressing mode. This data is outputted onto the converter data bus via Port A by sending the contents of the **Accumulator** directly to the 8155 with the 'OUT' instruction. DAC 1 is now enabled by transferring the contents of Register B to the Accumulator and outputting this via Port C. The Accumulator contents are rotated one bit left before being transferred back to Register B, ready to enable the next DAC. Next $\overline{\text{ENABLE}}$ is removed by outputting all 1's via Port C, H and L are incremented to address the next data byte and Register C is decremented and tested for zero. In this case Register C will contain 03 and the programme will branch back to the address labelled 'LOOP' via a conditional jump instruction, and the next data byte will be read into the Accumulator. Since Register B was shifted one bit left the new data will be loaded into DAC 2 on this cycle of the loop. The programme cycles round the loop 4 times, reading the data from memory and outputting it to each DAC in turn until Register C is decremented to zero, at which point the programme halts.

ZN428 – 8085A PROGRAMME EXAMPLE

LOC	OBJ	SOURCE STATEMENT	COMMENT
2000	31C820	LXI SP, 20C8	Initialise SP
2003	3E0D	MVI A, 0D	Define I/O Ports
2005	D320	OUT 20	
2007	212020	LXI H, DATA	Set H & L = Data
200A	06FE	MVI B, FEH	
200C	0E04	MVI C, 04H	
200E	7E	LOOP: MOV A,M	Read Data
200F	D321	OUT 21	Put Data on Bus
2011	78	MOV A,B	
2012	D323	OUT 23	Set $\overline{\text{Enable}}$ low
2014	07	RLC	Rotate left for next DAC
2015	47	MOV B,A	
2016	3EFF	MVI A, FF	Set $\overline{\text{Enable}}$ high
2018	D323	OUT 23	
201A	23	INX H	
201B	0D	DCR C	
201C	C2 0E 20	JNZ Loop	Jump IF C = 0
201F	76	HLT	
2020	-	DATA :	
2021			
2022			
2023			

FIG. 4 PROGRAMME FLOW DIAGRAM



8155 PORT ALLOCATIONS

PORT A

PA0	Binary Data LSB
PA1	Binary Data LSB + 1
PA6	Binary Data MSB - 1
PA7	Binary Data MSB

PORT B

NOT USED

PORT C

PC0	DAC1 $\overline{\text{Enable}}$ Input
PC1	DAC2 $\overline{\text{Enable}}$ Input
PC2	DAC3 $\overline{\text{Enable}}$ Input
PC3	DAC4 $\overline{\text{Enable}}$ Input
PC4	Not Used
PC5	Not Used

I/O PORT ADDRESSES

20	Command/Status Reg
21	RAM Port A
22	RAM Port B
23	RAM Port C

Summary

The system described in this report should be satisfactory for most applications, however, this configuration is by no means rigid, but is only intended as one example to demonstrate how easily the ZN428 can be used with the 8085A microprocessor system. A few ideas and notes are briefly described below, and it is hoped that these will help the Design Engineer to produce the most efficient system for his particular requirements.

1. The 8155 I/O Ports can be allocated as dictated by system requirements and availability. In the example all of Port A and four of the six Port C I/O pins are used. Port B could have been used equally as well either for the converter data bus or to provide the $\overline{\text{ENABLE}}$ signals.
2. If I/O Port pins are limited and only one DAC needs to be enabled at any one time, then a Decoder I.C. (i.e. 8205, 1 out of 8 binary decoder) can be used to drive the $\overline{\text{ENABLE}}$ inputs. For Example 4 I/O Port pins, 3 for the address code and 1 for the decoder enable would drive 8 DAC ENABLE inputs.
3. In order to update 2 DACs simultaneously but with different data, then the binary inputs of one (or more) DACs could be connected to Port A and the other DAC to Port B. The relevant data could then be outputted on Ports A and B and then the $\overline{\text{ENABLE}}$ inputs of both DACs driven to logic '0' together, either by commoning the two inputs to one Port C pin or by using separate I/O pins from Port C but programming both bits to go low together.
4. The number of ZN428s which can be connected to a common data bus is limited only by the bus capacitance and the drive capability of the 8155 I/O Ports. Note the low inputs currents of the ZN428—
   $I_{IH} = 20\ \mu A$ at 2.4 V, $I_{IL} = -5\ \mu A$ at 400 mV.
5. When the ZN428 $\overline{\text{ENABLE}}$ input is held at logic '0' the input latches are held open and the data is transferred directly to the ladder switches. Therefore, if repeatedly updating only one DAC the $\overline{\text{ENABLE}}$ input can be held at logic '0' instead of returning to logic '1' after each update.
6. If A/D channels as well as D/A are required in one system, then ZN427, 8-bit A/D Converters can be mixed on the same converter data bus as the ZN428. This will allow the design engineer to tailor a system to his specific A/D and D/A requirements. (See FERRANTI APPLICATION NOTE AN 010/OSB for details of interfacing the ZN427 to the 8155.)

It is hoped that after reading this application note the reader will have a much better insight into the operation and versatility of the ZN428, and into how it can easily be interfaced to a microprocessor system. In order to avoid duplication only the relevant characteristics of the ZN428 were discussed in this report. For a full description and specification of the ZN428 please refer to the data sheet.

Direct Bus Interfacing Using The ZN427/ZN428 Data Converters

INTRODUCTION

The rapid growth of the microprocessor coupled with its diminishing cost has opened up many potentially new applications in the measurement, control and data acquisition fields of the electronics industry. This growth has, however, been so fast that a vacuum has been created in the data conversion market for low cost, microprocessor compatible converters which can interface the digital microprocessor with the real analogue world. Without some form of interface to the outside world a microprocessor is simply a non-entity. No matter how powerful and fast the microprocessor itself is, if it cannot communicate efficiently with the world around it then its usefulness is limited and its power wasted. It is to meet this requirement that two fast, low-cost, microprocessor compatible data converters have been introduced by Ferranti Electronics Ltd. This application note introduces these two converters and describes how they can easily be interfaced directly to most of the popular types of microprocessor with particular reference to the 6800 and 8085A.

THE ZN427 A to D CONVERTER

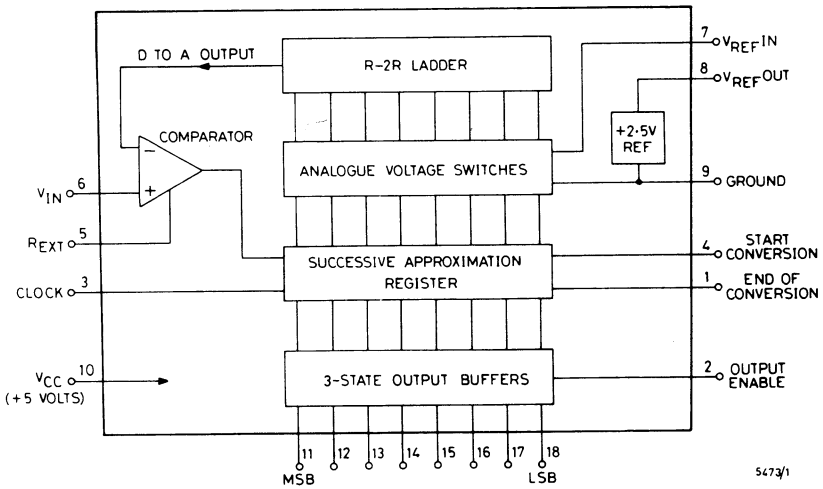


Fig. 1. ZN427 LOGIC DIAGRAM

The ZN427 is an 8-bit successive approximation A to D converter (ADC).

It features 3-state output buffers to permit bussing on to common data lines, fast 15 μs conversion time and no missing codes over its full operating temperature range. The ZN427 contains a voltage switching D to A converter, a fast comparator, successive approximation logic, three-state output buffers and a 2.5 volt precision band-gap reference.

The use of the on chip reference is pin optional to retain flexibility, an external fixed or varying reference for ratiometric operation may, therefore, be substituted. Only a few passive external components are required. For basic operation these are an input resistor, a reference current resistor and stabilising capacitor, and a resistor from the R_{EXT} pin 5 to the negative supply rail.

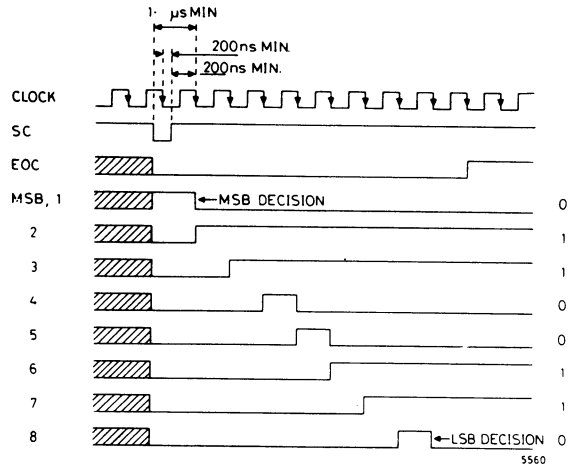


Fig. 2. ZN427 TIMING DIAGRAM

The conversion cycle is initiated by a negative going pulse applied to the START CONVERSION (SC) input, this sets the END OF CONVERSION (EOC) output to a logic '0' indicating that the converter is busy, see Fig. 2. On the ninth negative clock edge after the start pulse the EOC output goes back to a logic '1' signalling that the cycle is complete. The binary output data is latched until the next start pulse. The three-state data outputs are switched OFF (high impedance state) when the OUTPUT ENABLE (OE) input is at a logic '0' .and they are enabled when the OE input is taken to a logic '1'.

THE ZN428 D to A CONVERTER

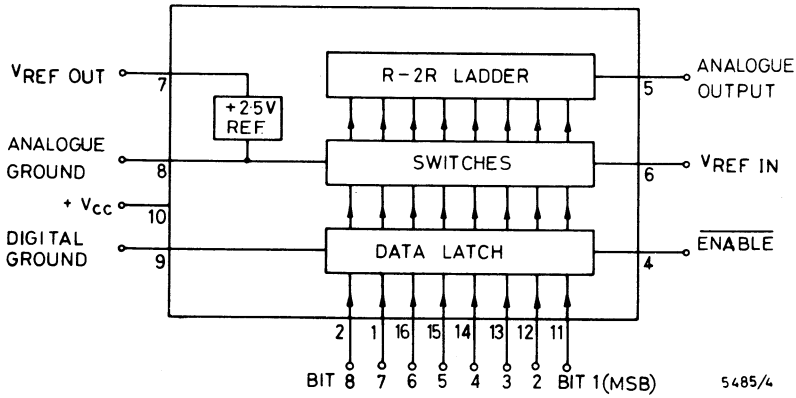


Fig. 3. ZN428 LOGIC DIAGRAM

The ZN428 is a monolithic 8-bit D to A converter (DAC), with input latches to facilitate updating from a microprocessor data bus. The latch is transparent when the ENABLE ($\overline{EN}$) input is at a logic '0' and the data is held when $\overline{EN}$ is taken to a logic '1'.

The ZN428 features single +5V supply requirements, fast 800 ns settling time and is guaranteed monotonic over its full temperature range. It contains a pin optional 2.5V precision band-gap reference identical to the ZN427. The converter is of the voltage switching type and uses an R-2R ladder network. Each 2R element is connected to 0 volt or $V_{REF\ IN}$ by transistor logic switches especially designed for low offset voltage (<1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network, the nominal range being $0 - V_{REF\ IN}$ volts with a 4 kΩ resistance. Other output ranges can readily be obtained by the use of an external amplifier allowing complete versatility in its application.

THE ZN427 MICROPROCESSOR BUS INTERFACE

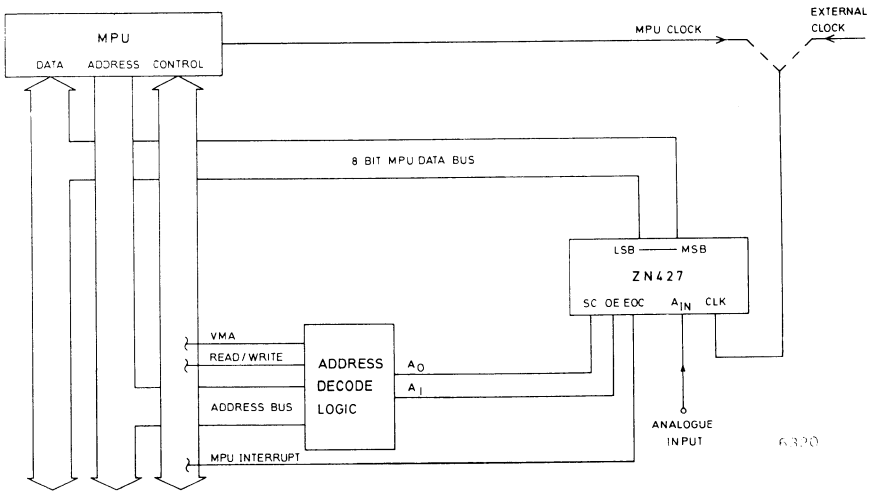


Fig. 4.

Peripheral devices can be connected to a microprocessor system by two basic methods. The first and usually the simplest from the point of view of design effort required is to use a Peripheral Interface I/O device usually found as a support IC in most of the MPU families. With this method the peripheral device is simply connected to the I/O lines of the Peripheral Interface device and generally no considerations have to be made in terms of bus buffering, bus timing or address decoding.

The second method is to connect the peripheral device directly to the microprocessor data bus. This method is termed "Memory Mapped I/O" which as its name implies is to make each peripheral I/O function appear to the MPU as a normal memory location, in which case the MPU cannot tell whether it is addressing memory or I/O. This allows the full set of memory reference instructions to be used for I/O data transfer, but it does imply that the peripheral device must be capable of responding at least as fast as the MPU memory and hence it should be compatible with the bus timing characteristics. The disadvantages of Memory Mapped I/O are that it usually requires additional address decoding logic, and also, since the I/O device will be addressed as memory, then there will consequently be fewer addresses available for actual memory.

It is with this second method of interfacing that this Application Note is primarily concerned. The Peripheral Interface I/O method of interfacing the ZN427 and ZN428 is covered in Application Notes AN010 – AN012.

A variation of Memory Mapped I/O, sometimes known as "I/O Mapped I/O" is available on some MPUs which overcomes the last disadvantage referred to. This allows a defined range of memory address also to be used for I/O by means of separate I/O instructions. A special control line is required to inform the memory and I/O device whether the address of the current READ or WRITE cycle refers to memory or to I/O. This technique however does restrict the freedom of the programmer to the use of these I/O instructions which normally only operate on data in the microprocessor accumulator.

Figure 4 shows the basic Memory Mapped interface for the ZN427 where the 8 binary outputs of the ADC are connected directly to the MPU data bus. The control inputs, START CONVERSION and OUTPUT ENABLE are shown driven from address decoder logic, the function of which is to drive the appropriate input when the address which has been allocated to that particular input is present on the address bus and the control bus signals indicate a valid memory read or write operation. Note that the level of address decode logic used must ensure that the three-state data outputs of the ZN427 are disabled at all times except when the actual ADC data is required on the data bus, otherwise bus contention problems may occur with other devices using the bus. The END OF CONVERSION output can be connected directly to an MPU interrupt input to signal the completion of the conversion cycle by the ADC. The ZN427 clock can be derived either from the MPU clock or from an external source. If however the former method is employed, it may simplify the design of the interface with regard to the timing criteria of the SC input. (This is covered in more detail later in this report).

THE ZN428 MICROPROCESSOR BUS INTERFACE

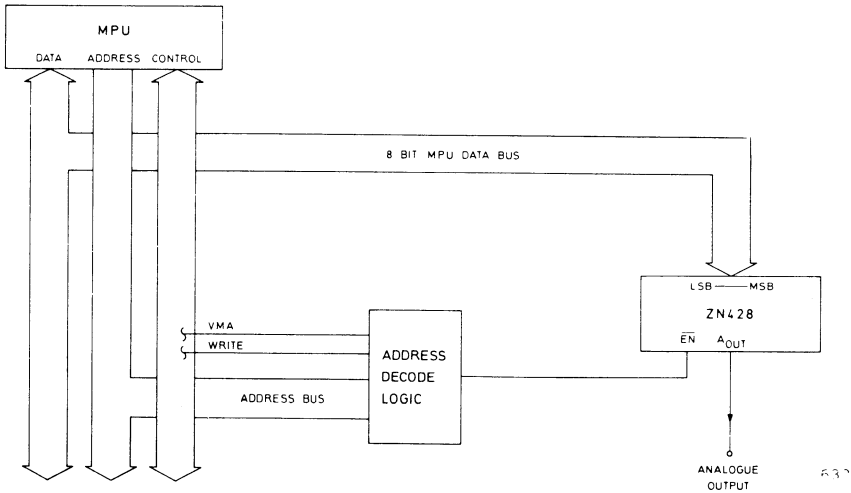


Fig. 5.

The ZN428 data inputs can be directly connected to an MPU data bus when used in the Memory Mapped configuration, this is illustrated in Fig. 5. For this application the address decode logic has only to generate the NOT ENABLE signal for the DAC. This is accomplished by gating the MPU

WRITE signal with the decoded address signal in order that when a memory write instruction to the DAC address location is executed, then a negative going pulse is applied to the $\overline{EN}$ input which will transfer the binary code from the data bus to the ZN428 input latches.

INTERFACING TO THE 6800 BUS

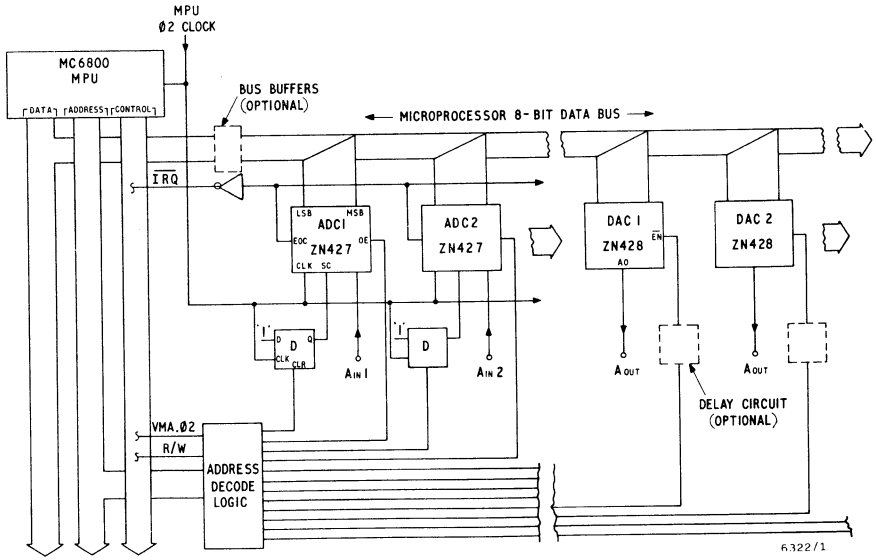


Fig. 6. ZN427/ZN428 TO 6800 BUS INTERFACE

With the ability of the ZN427 and ZN428 to be bus compatible it is possible to produce a complete Analogue I/O system, specifically configured to the designer's own requirements with the converters connected directly to the MPU data bus. Such a system is illustrated in figure 6 built around a 6800 MPU.

The 6800 is an 8-bit monolithic microprocessor which forms the central control function for the 6800 microprocessor family. Fully compatible with TTL logic the 6800 requires only a single +5 volt power supply, it features a set of 72 instructions with 7 addressing modes and full 65K byte memory addressing capability. The microprocessor communicates with its external memory and all I/O peripherals over an 8-bit bi-directional data bus and a 16-bit address bus. (Full data on the 6800 microprocessor is readily available from its manufacturers and their distributors).

The number of ZN427s and ZN428s which can be hung on the data bus is not limited, the only restrictions being the total load presented to the data bus and the number of decoded address lines available. The loading and drive characteristics of the converters are summarised in Table 1. Optional bi-directional bus buffers are shown in the diagram, these can be used to expand the system. Use of these will be dependent on the total number of converters used, other peripheral and memory devices on the data bus, and other loading factors such as the physical length of bus required.

ZN427		ZN428	
Parameter	Specification	Parameter	Specification
I_{IL}	–5 μA max.	I_{IL}	–5 μA max.
I_{IH}	15 μA max.	I_{IH}	20 μA max.
I_{IH} (Clock)	30 μA max.		
I_{OL}	1.6 mA min.		
I_{OH}	–100 μA min.		
I_{OHX} (Off state leakage)	2 μA max.		

(NOTE: Currents specified at 0.4V and 2.4V).

TABLE 1. LOADING CHARACTERISTICS OF THE ZN427 and ZN428

The level of address decoding will depend on the overall MPU system design. This can range from merely using the upper address lines directly with no hardware decoding to provide the control lines for the converters – which rapidly depletes the number of address locations available for memory, through to full address decoding where all 65K addresses can be utilised. The address decode hardware can usually be produced from a few TTL gates in association with an Address Decoder I/C such as the ZN74154. In order to avoid addressing problems it is necessary on the 6800 to qualify the decoded address with the Valid Memory Address (VMA) and ∅2 clock signals. The READ/WRITE control line can also be utilised to permit a single decoded address to control each ZN427, i.e. a WRITE instruction to the specific address would generate the SC signal and a READ instruction of the same address would enable the converter outputs and read the data. The function of the 'D' type flip flops shown in the diagram is to ensure that the timing criteria of the SC pulse are met. The requirements for this are that the SC pulse should start at least 1.5 μs before the first active (negative going) clock edge after the SC pulse, and that the trailing edge of the SC pulse must not occur within ±200 ns of a negative going clock edge, see figure 2. By careful design of the address decode logic when deriving the converter clock from the MPU it is possible to produce the correct timing for the SC pulse and to dispense with the 'D' type flip-flops.

The other advantage of using the MPU clock is that it allows an accurate calculation of the ZN427 conversion time to be made in terms of MPU machine cycles. Again with reference to figure 2 it can be seen that the conversion cycle always takes less than 10 clock cycles after the end of the SC pulse. Hence instead of using the EOC output to drive the MPU $\overline{IRQ}$ input a simple programme delay loop can be substituted. Note that the EOC outputs of up to five ZN427s can be 'wire-anded' together to form a common interrupt line.

The clock frequency of the standard 6800 is 1 MHz which can be used directly to drive the ZN427s if a small loss of accuracy can be tolerated. The 6871B MPU clock generator is produced in a version with a 614.4 kHz clock signal. This is only marginally higher than the specified ZN427 clock rate of 600 kHz and the ∅2 TTL output of this can be used directly for the converter clock if full accuracy is essential.

With the 6800 it may be necessary to delay the decoded address enable signal to the ZN428 converters if glitch free operation is desired. This is due to the fact that during a write operation on the 6800 the address and address qualifying control signals become valid before the data bus signals are valid, thereby enabling the DAC before the data is established on the data bus.

The Analogue output can be taken directly from the ZN428 output pin which provides a nominal output range from zero volts to $V_{REF\ IN}$ with a 4kΩ output resistance. For most applications higher output ranges or drive will be required. This can easily be accomplished on the ZN428 by the addition of an external buffer amplifier which can be chosen for the specific characteristics required. The ZN428 is provided with separate Analogue and Digital ground pins which should normally be connected together close to the I.C. For noisy systems or environments an improvement may be obtained, in some cases, by running the two ground pins to supply ground separately, taking the Analogue ground of each ZN428 to a single common earth point in the system away from the sources of high noise such as clock oscillators, digital buses, etc. Note that the maximum voltage between the Analogue and Digital ground pins should not be allowed to exceed 200 mV.

Both the ZN427 and ZN428 contain a nominal 2.5V internal band-gap voltage reference. Use of this on-chip reference is pin optional to retain flexibility and an external reference can be substituted which allows ratiometric operation over the range of typically 1.5 to 3V. The on-chip reference is capable of supplying the reference voltage for up to five ZN427s and ZN428s. This useful feature saves power, discrete components and gives excellent gain tracking between the converters in a system. The tail current for the comparator on the ZN427 is derived via an external resistor from a negative supply. By suitable choice of resistor any negative supply of between –3 and –30 volts may be used. Since the negative current is only of the order of 65microamps per converter then for applications where only a positive supply is available a simple diode pump circuit can be used.

With a memory mapped interface the full range of memory reference instructions are available to the programmer in order to control the converters, and programming becomes a relatively simple matter of reading and writing data to the addresses allocated to the converters. For example, for the ADCs a conversion cycle could be initiated by a store accumulator command (STA A) to address location ALOC 1, where ALOC 1 is the address of the ADC to be accessed. The contents of the MPU accumulator 'A' at this time are irrelevant since we only want to generate a memory write cycle to produce a pulse at the SC input. Now one can either enable the MPU interrupt and wait for the EOC output to generate an interrupt request signal if this is the method used or alternatively a simple programme delay loop can be entered to produce a delay of $\geqslant 9$ converter clock cycles (i.e. $\geqslant 15$ μs if a 600 kHz clock is used). Upon receipt of an interrupt or completion of the delay a load accumulator command (LDA A) can be performed on address ALOC 1. This will read the binary data from the converter into the MPU accumulator 'A'. It is even simpler to programme the DACs. All one needs to do is to load the value to be outputted to say accumulator 'A' in binary format. A store accumulator command (STA A) is then programmed to address location ALOC 2, where ALOC 2 is the address allocated to the DAC. Upon execution of this the data will be transferred from the accumulator via the data bus to the DAC input latches, and be present at the DAC output in analogue form within 1.25 microseconds of the enable pulse.

INTERFACING TO THE 8085 BUS

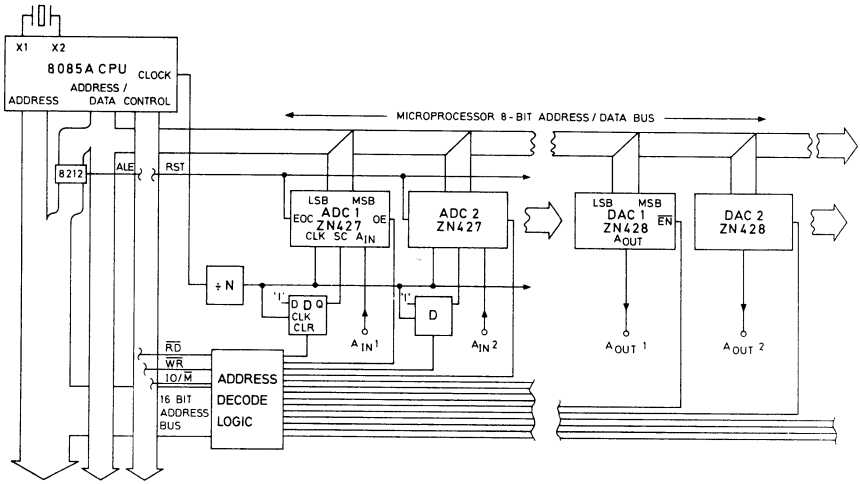


Fig. 7. ZN427/ZN428 TO 8085 BUS INTERFACE

An analogue I/O system for the 8085A microprocessor is shown in figure 7. This is similar to the 6800 system but the following exceptions should be noted.

The 8085A is another popular 8-bit microprocessor. However, unlike the 6800 this MPU uses a multiplexed data bus whereby the lower 8 address bits A0-A7 are time shared with the 8 data bits. The address bus contains the upper 8 bits A8-A15. If the lower 8 address bits are to be used for address decoding then it is preferable to de-multiplex the bus using an 8 bit latch, such as the 8212, strobed with the Address Latch Enable (ALE) signal from the MPU. The 8085A offers either Memory Mapped I/O or I/O Mapped I/O by means of a separate control line (IO/$\overline{M}$). This allows use of the 'IN' and 'OUT' instructions to control I/O data transfers and the retention of the full 65K memory locations. If using this method then it is unnecessary to de-multiplex the Address/Data Bus, since only the lower 256 addresses are used for I/O transfers, and the address in the lower 8 bits is mirrored into the upper 8 address bits during this operation.

The standard 8085A clock frequency is 3 MHz. Hence it is necessary to divide the output from the 8085A CLK output pin down by a factor of at least 4 to produce an acceptable ZN427 clock. Because of this it is more difficult to synchronise the decoded address signals with the ZN427 clock in order to meet the start pulse timing criteria, and one will usually have to incorporate the 'D' type flip-flops as indicated to generate the SC pulse.

Note that with the 8085A the common EOC line can be used directly to generate an interrupt via one of the 3 Restart Interrupt inputs. The decoded address input to the ZN428s $\overline{EN}$ input can also be used without any additional delay since, with this MPU the bus data is valid during the time that the WRITE signal is established.

Again programming is very straightforward. With a Memory Mapped I/O configuration the Data Transfer commands – Move (MOV), Load (LDA), and Store (STA) can be used to control data transfers between the converters and the MPU. If an I/O Mapped I/O configuration is adapted then the input (IN) and Output (OUT) commands are used to transfer data between the MPU accumulator and the converters.

SUMMARY

The Analogue I/O systems described in this report are intended only as a guide to illustrate to design engineers the ease and versatility with which these two converters can be used to produce analogue I/O channels for popular 8-bit microprocessors. As a result of the low cost, low external component count and flexibility of these converters, designs based on the 'one converter per channel concept' will be both a practical and economical solution to microprocessor data acquisition problems. This approach should find many new applications in areas which have previously been limited by the necessary usage of traditional data acquisition methods involving a single high cost hybrid ADC utilising sample and hold and multichannel multiplexing techniques.

Microprocessor Interfacing Using The ZN432 10-Bit Data Converter

INTRODUCTION

The use of Microprocessors in the fields of Process Control, Automotive applications, Industrial Data Acquisition and Logging and Domestic Consumer Products is becoming increasingly widespread. Indeed the fall in the price of the microprocessor itself is creating new applications in fields previously uneconomical to develop, and whilst the price of the microprocessor has fallen dramatically over the past two or three years the fall in the price of compatible Data Conversion products has not been so sharp. This is partially due to the fact that most Data Conversion products cannot be produced by using a single semiconductor process (as can microprocessors), but have to be manufactured in hybrid form using different processes for the digital and linear elements plus thin film technology and laser trimming for the precision resistor networks. Currently one may purchase a Microprocessor Integrated Circuit for only a few pounds whilst a microprocessor compatible Data Acquisition module may well cost in the region of £200. This module will of course probably provide 16 channels at 12 bit accuracy, but not every user wants all these channels or accuracy and though lower cost Converter I.C's are available the system manufacturer may well be disinclined to spend the time and manpower in designing a converter interface for his microprocessor system due to the complexities with which he fears he may be faced.

This Application Note describes a monolithic 10 bit accurate Analogue to Digital (A/D) Converter integrated circuit and explains the different techniques of interfacing this to common 8-bit microprocessors using the minimum of external discrete components and standard TTL logic elements.

THE ZN432 A/D CONVERTER

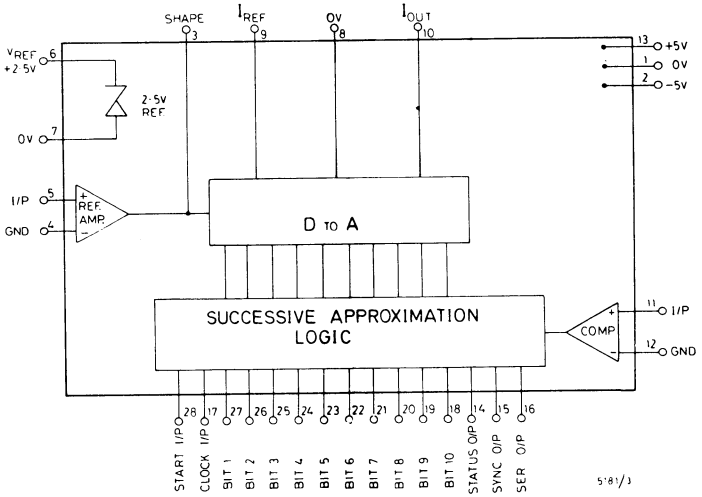


Fig. 1. ZN432 LOGIC DIAGRAM

The ZN432 is a 10-bit Analogue to Digital Converter produced in monolithic form by a silicon bipolar process. The converter is of the Successive Approximation type and includes an on-chip precision reference, reference amplifier, comparator, successive approximation logic and a D to A Converter. The D to A converter operates on the unit current source principle with a current switching

array using a matrix of diffused resistors. As a result of incorporating several design and layout innovations and the use of highly developed processing and photomask techniques, 10-bit accuracy is obtained without the need for post diffusion trimming operations. Only a few external components are required, including two capacitors, to shape the internal reference and reference amplifier outputs, and several resistors which define the input voltage range of the converter, which can be either unipolar or bipolar over whichever range is required by selecting suitable external resistors. The ZN432 is available in 3 temperature ranges, including full military temperature range, and in either 8 9 or full 10-bit accurate versions, packaged in a 28 lead hermetically sealed ceramic D.I.L. encapsulation.

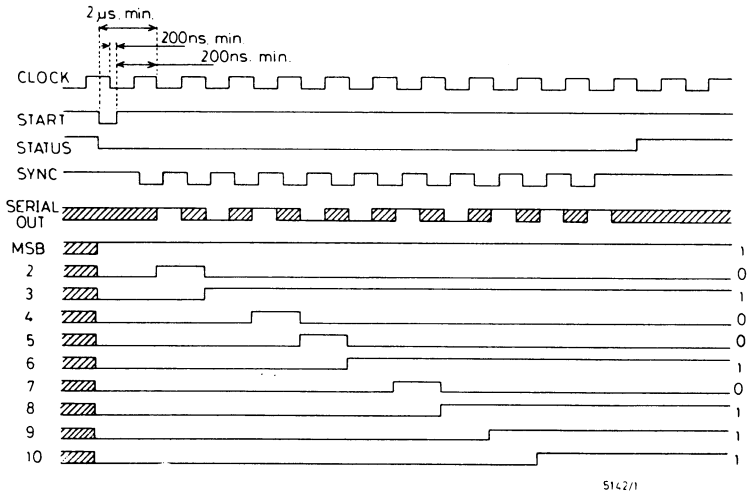


Fig. 2. TIMING DIAGRAM

The operation of the converter can best be described by reference to the timing diagram, Fig. 2. Conversion is initiated by a negative going START pulse which sets the MSB to a logic '1' and all other bits to a logic '0'. The STATUS output is also set to a logic '0' at this time indicating that the converter is busy. The leading edge of the START pulse should occur at least 2 µs before the 1st active negative going edge of the clock and the trailing edge of the START pulse must not occur within ±200 ns of a negative going clock edge. On the next negative going clock edge a decision is made on whether to set the MSB back to a logic '0' if the input current is less than the D to A output or, if not, it is left at a logic '1'. Bit 2 is switched to a logic '1' on the same clock edge and on the next negative edge a decision is made about Bit 2, again by comparing the input current with the internal D to A output. This process is repeated for all 10 bits so that when the STATUS output goes to a logic '1' on the 11th negative clock the digital output from the converter is a valid representation of V_{in}. A SERIAL DATA output is also provided on the ZN432, this data is outputted during the conversion cycle and is valid on the positive going edge of the pulses on the SYNCH output.

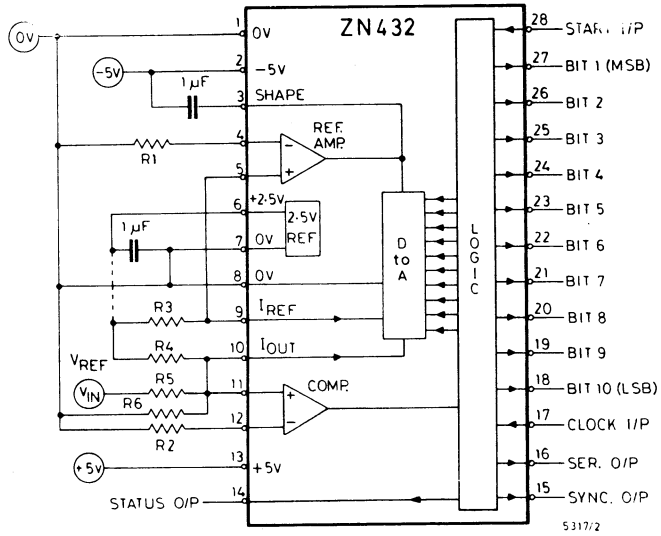


Fig. 3. TYPICAL EXTERNAL COMPONENTS

A diagram showing typical external components for the ZN432 is shown in Figure 3. The capacitor on pin 3 is used to stabilise the reference loop whilst that on pin 6 is for stabilisation and decoupling of the voltage reference output. Resistors R1 and R2 control the bias current of the reference amplifier and comparator, R3 defines the D to A reference current, R4 and R5 set the input voltage range and R6 is selected to obtain a suitable D to A time constant. For setting up, R3 will adjust the converter gain and R4 the offset. As an example, the resistor values for a ± 10 volt input range are:

R1 = 5 kΩ
R2 = 1.25 kΩ
R3 = 5 kΩ
R4 = 2.5 kΩ
R5 = 10 kΩ
R6 = 3.33 kΩ

Resistors R3, R4 and R5 affect gain and offset and hence high stability types should be used whereas the nearest preferred values may be chosen for R1, R2 and R6. Refer to the ZN432 Series Data Sheet for more information on the selection of external components.

INTERFACING DATA CONVERTERS TO MICROPROCESSORS

Peripheral devices can be interfaced to microprocessor systems by two basic methods. The first and simplest is to use a general purpose I/O device, (also known as Peripheral Interface Adapters, Versatile Interface Adaptors or Programmable Peripheral Interfaces, etc.). Most microprocessor systems on the market usually include one or more of these components in their Microprocessor Systems Family. They normally consist of one or more data ports, usually of 8 bits which can be programmed to function either as inputs or outputs. With some devices the complete port has to be programmed to function either as all Inputs or all Outputs, but the more useful I/O devices allow the individual pins of each data port to be programmed separately as Inputs or Outputs. In addition most devices also feature several control lines for the purposes of generating handshake signals with peripherals and generating microprocessor interrupts etc.

The second interface method is to connect the peripheral device directly to the microprocessor Data Bus. This method is termed Memory Mapped I/O which as its name implies, is to make each peripheral I/O function appear to the microprocessor as a normal memory location. This allows the full set of memory reference instructions to be used for I/O data transfer, but also implies that the peripheral device must be capable of responding at least as fast as memory, and hence it should be compatible with the MPU bus timing characteristics. With 10-bit converters a problem exists when using this method in that the 8-bit data bus is not wide enough to handle the converter data as a single word. It is therefore necessary to split the data into two words usually of 8 and 2 bits which are fed to the data bus in two separate bytes by means of appropriate gating on the converter outputs. Naturally when using a 16-bit microprocessor this problem does not arise, as converter data can then be read as a single word on the data bus. The disadvantages of Memory Mapped I/O are that it usually requires additional address decoding logic and also, since the I/O will be addressed as memory, there will consequently be fewer addresses available for actual memory. A variation of Memory Mapped I/O commonly referred to as I/O Mapped I/O or Isolated I/O is available on some microprocessors which overcomes this last disadvantage. This allows a defined range of memory addresses to be used also for I/O by means of separate Input and Output instructions. A special control output is used to tell the memory I/O devices whether the address of the current Read to Write cycle refers to memory or to I/O. This technique, does, however, restrict the freedom of the programmer to the use of these Input/Output instructions which usually operate only on data in the microprocessor accumulator.

So far we have dealt with interfacing to the ZN432 using the parallel binary outputs, alternatively the Serial Output can be used in applications which demand that the number of lines to the converter need to be kept to a minimum. Two schemes are briefly described here although other variations are possible. The first would be to connect the Serial Output to one I/O pin of an I/O device and to use the Status Output to generate microprocessor interrupts via one of the I/O device control inputs, thereby reading the serial data from the I/O device on the positive going edge of each pulse on the Status Output. The other method is to use a microprocessor with a direct Serial input part such as the 8085A. This would either involve synchronising the converter clock to a sub-multiple of the microprocessor clock and programming the microprocessor to read the data at the correct time, or by again using the Status Output to generate an interrupt. Unfortunately both these methods restrict the maximum converter clock period to a minimum of at least several instruction execution times i.e. the time needed to interrupt the microprocessor, read the data and store it in memory. Another option open to the designer would be to use a cascadeable shift register with 3-state outputs (i.e. a TTL 74LS395A) at the microprocessor and to convert from 10-bit serial to parallel data which would then be applied direct to the data bus in 2 words via the three-state outputs.

A ZN432 I/O INTERFACE

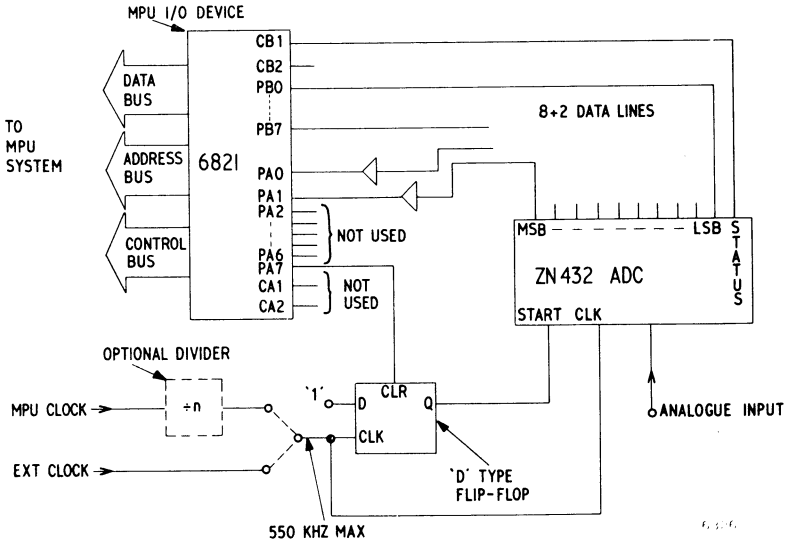


Fig. 4. ZN432 – 6800 I/O INTERFACE

Figure 4 illustrates one configuration of interfacing the ZN432 to an I/O device; in this case the 6821 Peripheral Interface Adaptor (PIA) device of the 6800 microprocessor family.

The PIA provides a flexible means of interfacing byte orientated peripherals to the microprocessor through two 8-bit bi-directional peripheral data lines and four control lines. The functional configuration of the PIA is under the full control of the microprocessor. Each of the peripheral data lines can be programmed individually to act either as an Input or an Output and each of the four control lines may be programmed for one of several control modes.

The diagram shows all 8 lines from Port B and 2 lines from Port A connected to the binary outputs of the ZN432. These lines are programmed as Inputs and allow the microprocessor to read the converted data by the execution of a microprocessor read peripheral data operation. Note the use of the two buffers on data lines PA1 snd PA2, these are necessary due to the higher input current of the Port A inputs.

The converter clock can be suppled either from the microprocessor clock or from an external source. Use of the microprocessor clock is preferrable since this allows a precise calculation to be made of the conversion time in terms of microprocessor machine cycles. If, however, the microprocessor clock is greater than the maximum converter clock rate of 550 kHz then it must be divided down to an acceptable level.

The 'D' type flip-flop is used to generate the Start pulse for the converter from the PA7 line, programmed as an output. The function of this flip-flop is to ensure that the Start pulse timing criteria with respect to the clock are met as explained earlier.

The STATUS output from the ZN432 is connected to CB1 control line. This can be programmed to set the interrupt flag bit-7 in Control Register B of the PIA, on occurrence of a positive transition of the CB1 input signal. The contents of this register can be read by the microprocessor and the state of this bit tested to determine the completion of the conversion cycle. Alternatively the PIA can be

programmed to generate a direct microprocessor interrupt from the Status signal on CB1. In this case, an interrupt routine in the program would be accessed on completion of a conversion and this would transfer the converter data via the PIA to defined storage locations in microprocessor registers or memory. This method is really only necessary if maximum utilisation of microprocessor time or converter data throughput is required. For situations where this is not critical the converter clock can be synchronised to the microprocessor clock as previously described, and a delay loop built into the program to allow for the conversion time. Since this is only 20 μs when running at the maximum clock rate a delay loop of only a few instructions will be sufficient to produce adequate delay.

A typical program to control the converter may be organised as follows:
Initially the PIA would be set-up with PB0 – PB7, PA0 and PA1 as Inputs, PA7 as an Output and Control Register B set to generate a microprocessor interrupt on a positive transition of the CB1 input. Note that the remaining lines PA2 – PA7, CA1, CA2 and CB2 are unused. A logic '0' followed by a logic '1' is then written to PA7; this clears the 'D' type and sets the START input, via the Q output, to a logic '0'. On the first positive going clock edge after PA7 returns to a logic '1' the Q output is clocked to a logic '1' allowing the ZN432 conversion cycle to proceed. (Note that it is not important if the START input is held low for several clock cycles, it will simply hold the converter with the MSB at a logic '1' and all other bits at a '0'). On the 11th negative clock edge after the Start pulse the STATUS output goes to a logic '1' indicating that the ZN432 has finished the conversion. This positive transition activates the $\overline{IRQ}$ line of the 6800, via the PIA, causing an interrupt. The 6800 stops execution of the current program sequence and begins an interrupt sequence. This involves saving the microprocessor register contents on the stack and setting the Interrupt Mask Bit so that no further interrupts will be serviced. The microprocessor is then directed to a vectoring address and branches to an interrupt routine in memory. This routine will read the converter data, via the PIA by addressing Ports A and B in turn and will then either store the data away in memory for future use, or will test the data and act accordingly on the results. Reading the data on Port B of PIA also has the effect of clearing the Interrupt Flag Bit. Resumption of the interrupted program sequence can now be made by execution of a Return from Interrupt (RTI) instruction.

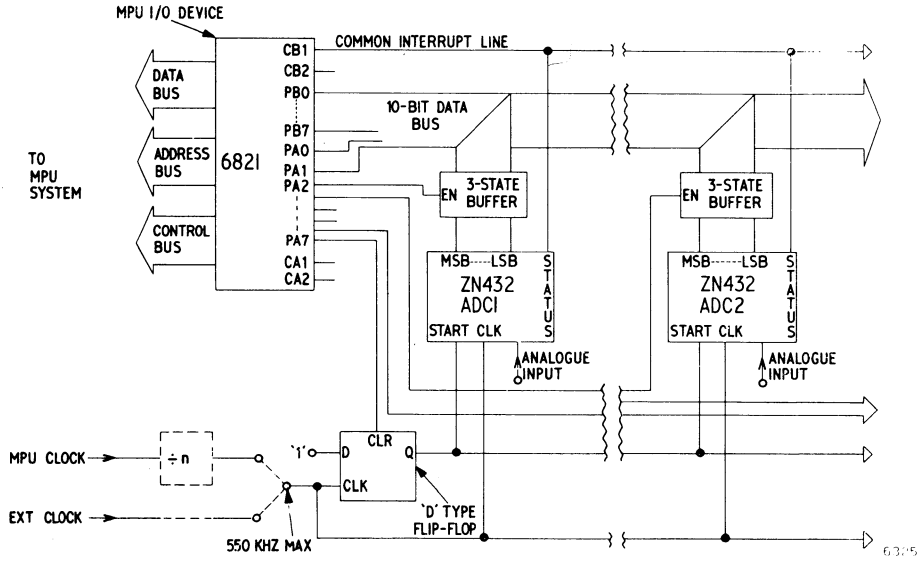


Fig. 5. MULTIPLE ZN432 – 6800 I/O INTERFACE

The configuration illustrated in figure 5 shows a suggested scheme for interfacing several ZN432's to an I/O device. This arrangement is similar to that previously described but in this circuit three-state buffers are used to interface each ZN432 to a common 10 bit bus from the PIA. The previously redundant lines PA2 – PA6 are now used to provide the enable signals for the three-state buffers. Note that the buffers of only one converter should be enabled at any one time otherwise false data will be read from the PIA.

The STATUS output of the ZN432 has a resistive pull-up load allowing typically up to 4 outputs to be 'wire-anded' together to form a common interrupt line. With the particular configuration shown a common Start signal for all the converters is produced, again from PA7 via the 'D' type flip-flop. Application of this signal would start all the converters simultaneously and a positive transition on the CB1 line would signify that all the converters had finished. Data from each converter would then be read by enabling the 3-state buffers via lines PA2 – PA6 in turn.

A ZN432 BUS INTERFACE

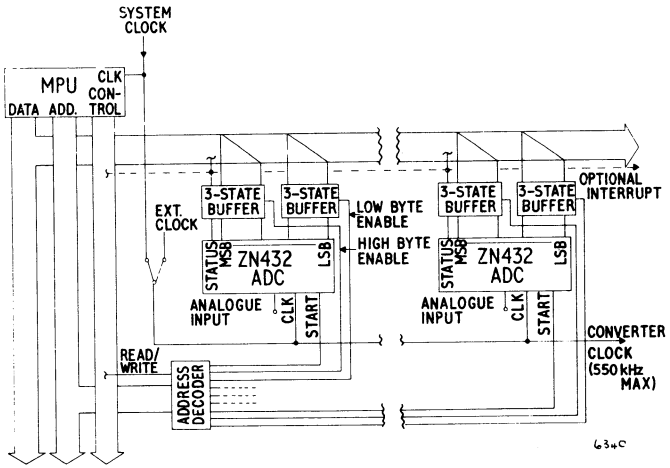


Fig. 6. MULTIPLE ZN432 MICROPROCESSOR BUS INTERFACE

The most versatile way of interfacing to a microprocessor is to go directly onto the Data Bus. Figure 6 illustrates this concept with the ZN432 where three-state buffers are again used but this time connected directly to the Data Bus of an 8-bit microprocessor such as the 6800. Since it is only an 8 bit bus the converter data has to be read in two words by enabling the buffers per converter in two groups as indicated by the High and Low Byte Enable lines per converter. One suggested scheme would be to transfer the output data as shown in Table 1. (Note that in converter terminology Bit 10 is the least significant bit (LSB).

TABLE 1

Data Bus Lines	Low Byte	High Byte
D7	Bit 3	—
D6	Bit 4	—
D5	Bit 5	—
D4	Bit 6	—
D3	Bit 7	—
D2	Bit 8	(Status)
D1	Bit 9	Bit 1 (MSB)
D0	Bit 10 (LSB)	Bit 2

The STATUS output can be read on the Data Bus with the High Data Byte or alternatively these outputs can be 'wire-anded' or gated together to produce a common interrupt signal.

The Start pulse and High and Low Byte Enable signals are generated from a logic block labled 'Address Decode Logic'. The function of this is to drive the appropriate input when the address, which has been allocated to that particular input, is present on the Address Bus and the Control Bus signals indicate a valid Memory Read or Write operation. Note that the level of address decoding used must ensure that the three-state buffers are disabled at all times except when the actual converter data should be on the bus, otherwise bus contention problems, with other devices using the bus may occur. A convenient means of address utilisation for the system in figure 6 is shown in Table 2, which allocates two consecutive addresses to each converter.

TABLE 2

ADDRESS	MPU READ	MPU WRITE
XXX 0	High Byte Enable ADC1	Start ADC1
XXX 2	Low Byte Enable ADC1	Start ADC1
XXX 2	High Byte Enable ADC2	Start ADC2
XXX 3	Low Byte Enable ADC2	Start ADC2
XXX 4	High Byte Enable ADC3	Start ADC3
etc.	etc.	etc.

(XXX = unique address for particular MPU system.)

A Write instruction to either address will then start that converter. On completion of the conversion, detected either by interrupt, testing of the Status Bit, or fixed program delay, the converter data can be read by a double byte load instruction which will load the data into two consecutive RAM memory locations or into a 16 bit microprocessor register, (i.e. Instruction LDX – Load Index Register of the 6800, loads the more significant byte of the index register from the byte of memory at the address specified by the program and loads the less significant byte of the index register from the next byte of memory at one plus the address specified by the program).

Note that the 'D' type flip-flop is not shown in figure 6. With a direct microprocessor clock it is possible to design the address decode logic so that the timing criteria of the Start pulse with respect to the clock input is complied with.

SUMMARY

Numerous different microprocessors are currently available and each microprocessor based control system will have its own individual data acquisition requirements. It is impossible in a paper of this type to cover all possible permutations of microprocessor/converter interfaces, but adoption of one of the two basic methods described here should be possible with most 8-bit microprocessors, allowing the design engineer to produce the most efficient data acquisition system to meet his design objectives. The ZN432's versatility and ease of use, coupled with its wide operating temperature range and TTL compatibility, will allow it to be used in a diverse range of applications where 10-bit accuracy is necessary.

Further information on the device characteristics and gain selection components, etc., is given in the ZN432 Series Data Sheet.

A Serial Interface For The ZN427 A/D Converter

A SERIAL INTERFACE FOR THE ZN427 A/D CONVERTER

In many data aquisition applications it is advantageous to situate the A/D converter close to the transducer and to transmit the digital data in serial form back to the data collection centre of the system. The serial data link uses less conductors and provides better noise immunity than a parallel data bus. This application note describes a RS-232C compatible serial data interface for the ZN427 8-bit A to D converter using an industry standard 6402 UART.

A simplified block diagram is shown in Fig. 1.

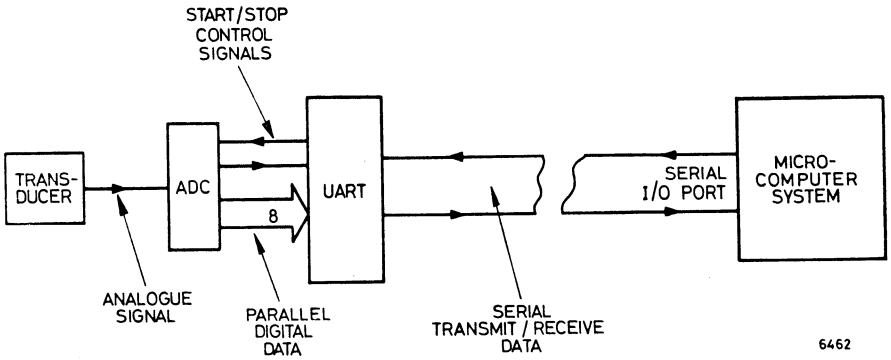


Fig. 1 Serial Data Interface

In order to initiate a conversion cycle a character is transmitted by the microcomputer. Upon receipt of this character by the UART its DR (Data Received) output goes to a high level which generates a start pulse for the A/D converter triggering a conversion cycle. At the end of the cycle the EOC (End of Convert) output is used to load the converted data into the UART which performs a parallel to serial conversion and transmits the data back to the microcomputer.

The ZN427 is an 8-bit successive approximation A to D converter. It features 3-state output buffers to permit bussing onto common data lines, fast 10 μs conversion time and no missing codes over the full operating temperature range. The ZN427 contains a voltage switching D to A converter, a fast comparator, successive approximation logic, three-state output buffers and a 2.5V precision band-gap reference. A logic diagram of the converter is shown in Fig. 2. Only a few passive external components are required. For basic operation these are an input resistor, a reference current resistor and stabilising capacitor, and a limiting resistor for the negative supply current. This will provide a nominal input voltage range of 0 to $V_{REF\ IN}$. Other input ranges both Unipolar and Bipolar can be obtained by connecting a simple resistor network to V_{IN} (Pin 6) as illustrated in Figs. 3(a) and (b). Further information on the ZN427 can be found in the Data Sheet.

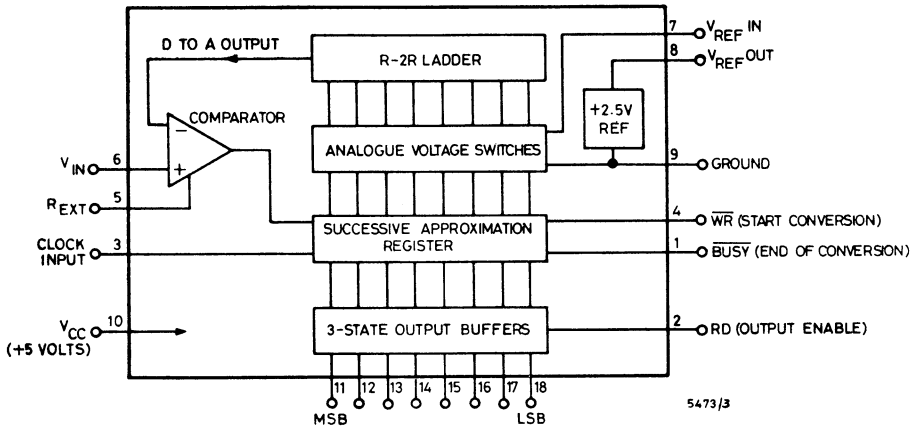


Fig. 2 System Diagram

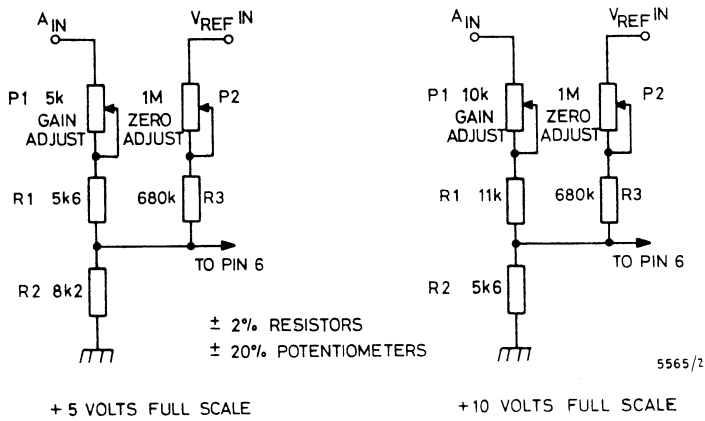


Fig. 3a Unipolar Operation - Component Values

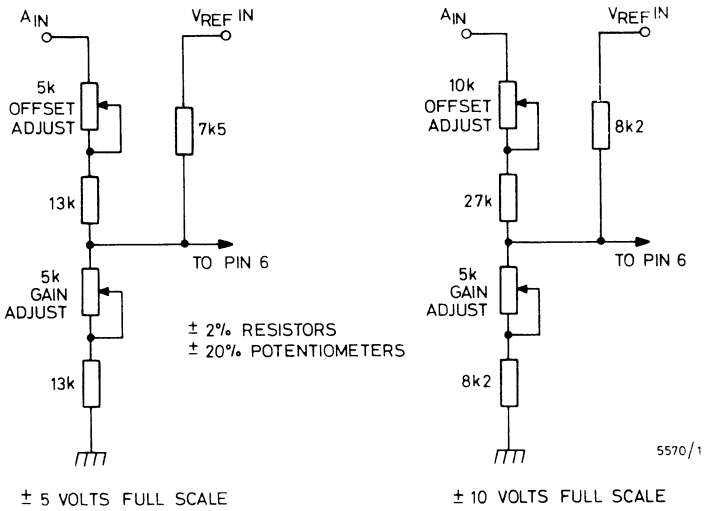


Fig. 3b Bipolar Operation – Component Values

A detailed circuit diagram of the converter interface is shown in Fig. 4.

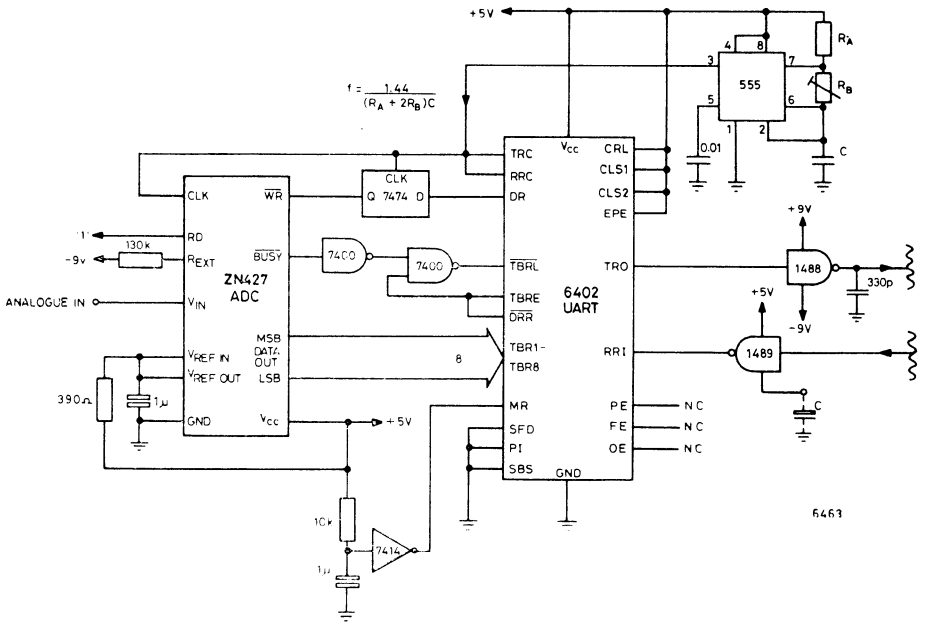


Fig 4. ZN427 UART Interface

The DR output of the UART is connected to the 'D' input of the 7474 latch, the 'Q' output of which drives the $\overline{WR}$ (Start Convert) input of the ADC. The use of this ensures that the timing of the $\overline{WR}$ pulse with respect to the converter clock input is correct. On the ninth negative clock edge after the $\overline{WR}$ pulse the $\overline{BUSY}$ output goes to a high level signalling that the conversion cycle is complete. This low to high transition is used to load the data into the UART via the TBRL (Transmitter Buffer Register Load Input). The signal is gated with the TBRE (Transmitter Buffer Register Empty) signal which holds the TBRL input high until the UART transfers the data to its transmitter register. If TBRL were allowed to return low before TBRE went high the converter data would be overwritten since the TBR (Transmitter Buffer Register) is a transparent latch. The TBRE signal is also used to drive the DRR (Data Received Reset) input which clears the DR output to a low level allowing another character to be received.

The waveforms associated with this operation are shown in Fig. 5. A simple oscillator using a 555 I.C. is shown which generates both the ADC clock and the Transmit/Receive clocks for the UART. The external clock is 16 times the data rate, the signal being divided internally by the UART. If a more stable data rate is an important factor then the 6403 UART, which is functionally similar but which uses a crystal oscillator as the timing source, may be substituted. In this case the ADC clock would still be generated by the 555 since it is not necessary for the converter and UART clocks to be synchronous. The UART control inputs CLS1, CLS2 (Character Length Select) ; PI (Parity Inhibit) ; EPE (Even Parity Enable) ; SBS (Stop Bit Select) are hard wired for whatever data format is wanted.

The MR (Master Reset) input is driven via a 7414 Schmitt trigger I.C. from a R-C delay circuit to generate the recommended reset pulse after power-up.

The 1488 and 1489 I.C.'s shown buffering the UART TRO (Transmitter Register Output) and RRI (Receive Register Input) pins are RS-232C compatible line drivers and receivers.

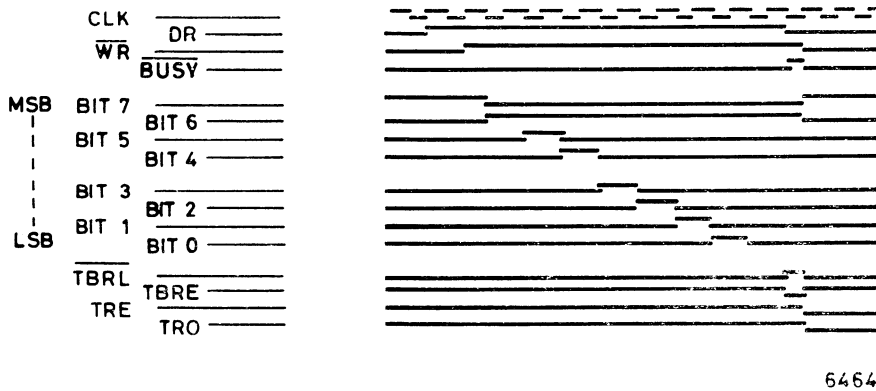


Fig. 5 ZN427 UART Interface Waveforms

In some applications incorporating microcomputers with RS-232C serial I/O ports no additional interfacing at the data collection centre end will be necessary. However if only a parallel I/O port is provided then another UART to convert the serial data back to parallel will be needed. An interface for the PET microcomputer which connects to the Parallel User Port on connector J2 is shown in Fig. 6. This uses the eight I/O data lines. PA0-PA7 and two control lines CA1 and CB2 which originate from a 6522 Versatile Interface Adaptor I.C. The data lines PA0-PA7 are connected to the RBR (Receive Buffer Register) outputs of the UART. The CA1 input is driven by the UART DR output and is operated in the latched mode which stores the received data within the VIA on a positive transistion of this pin. In order to initiate a new reading from the ADC the remaining control pin CB2 is used. This is connected to the UART inputs DRR and TBRL. When programmed to produce a negative going pulse the DR output is reset and a character is transmitted to the converter UART to start a new conversion cycle.

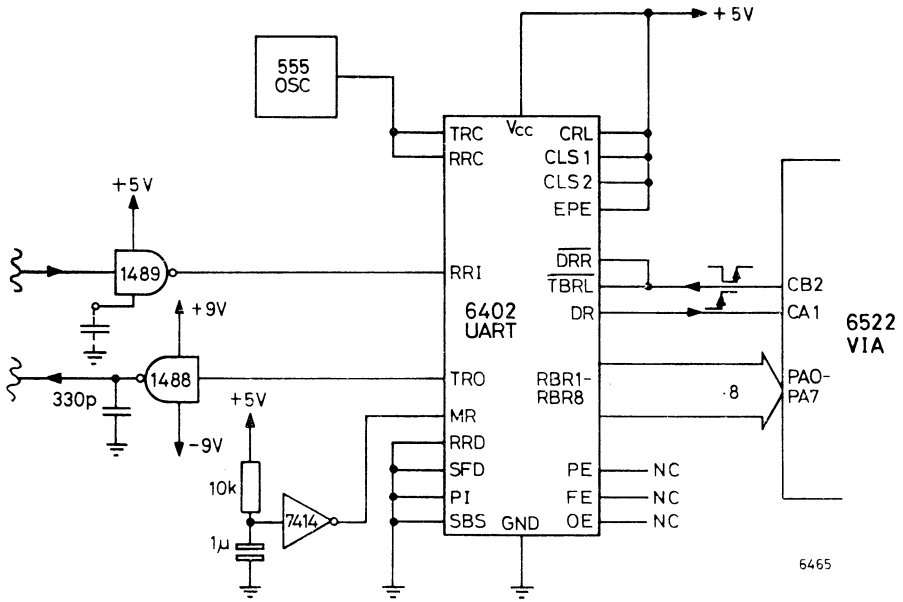


Fig. 6 6522 VIA UART Interface

A simple program example written in PET Basic is shown below.

PROGRAM EXAMPLE

```
10  REM UART INTERFACE REV. 3
20  REM SET PORT A TO INPUTS
30  POKE 59459, 0
40  REM DISABLE CA1 INTERRUPT
50  POKE 59470, 2
60  REM SET PCR TO 111XXXX1
70  POKE 59468, PEEK (59468) OR 225
80  REM SET ACR TO XXX000X1
90  POKE 59467, PEEK (59467) AND 227 OR 1
100 REM CLEAR CA1 FLAG IN IFR
110 A = PEEK (59457)
120 REM PULSE CB2 LOW-HIGH
130 POKE 59468, PEEK (59468) AND 31 OR 192
140 POKE 59468, PEEK (59468) OR 225
150 REM WAIT FOR +TRAN ON CA1
160 REM TEST CA1 FLAG IN IFR
170 IF (PEEK (59469) AND 2) THEN 190
180 GOTO 170
190 REM READ IRA AND CLEAR CA1 FLAG
200 A = PEEK (59457)
210 PRINT A
220 GOTO 120
```

Initially the appropriate VIA internal registers are set up and then a negative going pulse is produced on the CB2 pin. This starts a conversion sequence and when the new data is received the CA1 input goes high, latching the data in the VIA, and setting the CA1 Flag bit in the Interrupt Flag Register. This flag is tested by the program and when set the data is read and printed out. CB2 is again pulsed low and the sequence repeated.

For 6502 based microcomputer systems where all I/O lines of a 6522 VIA are available the CA2 pin can be used in the Read Handshake Mode in place of the CB2 pin, simplifying the program. Also the Status Flag of the UART can be monitored by the other I/O port lines for error checking purposes.

A Single Channel Codec

Acknowledgement: Ferranti wish to thank Mr. J. Everard and his colleagues of the British Post Office whose work this report is based upon and the Institute of Electrical and Electronic Engineers Inc. for permission to use extracts from a paper titled 'A Single Channel Codec' written by J. Everard and presented at ISSCC 78–Toronto.

INTRODUCTION

Conventional techniques for pulse code modulation (pcm) conversion for use in completely digital switching systems employ ladder networks requiring many high precision components to define the quantiser characteristic to sufficient accuracy. Alternative techniques employ linear ramps requiring either excessively high clock speeds or a number of ramps of precisely relative slopes.

In order to meet the signal-to-noise and gain-linearity constraints usually imposed on such systems, particularly for the telecommunications market, the use of expensive analogue to digital and digital to analogue hybrid circuitry is necessary. Due to the very high cost of the A/D and D/A component, multi-channel multiplexing techniques are usually employed.

The system described herein uses an advanced approach to a pcm codec (coder/decoder) designed at the British Post Office Research Centre at Martlesham Heath. The original aim was to produce an inexpensive codec capable of fully meeting the relevant C.C.I.T.T. recommendations. The B.P.O. realised that the way to achieve this was to make optimum use of state-of-the-art semiconductor L.S.I. technology. One such technology chosen was the Ferranti L.S.I. bipolar process. The result is a single channel codec of the type outlined in figure 1. The L.S.I. codec chip is the Ferranti ZNPCM1, the performance of which completely meets the performance specification defined by the British Post Office. The operation and realisation of the single channel codec is described in the following pages.

SYSTEM CONSIDERATIONS

The B.P.O. adopted an approach based on the principle of conversion to and from pcm via an intermediate digital code format, i.e. the encoder may consist of a waveform tracking encoder to provide highly oversampled A/D conversion followed by digital processing logic to convert the intermediate code to pcm. The decoder may consist of digital processing logic to convert pcm to some intermediate code format and a simple D/A to convert from the intermediate code to analogue. B.P.O. studies revealed that a trade-off was necessary between analogue A/D and D/A simplicity and conversion logic speed and complexity.

The trade-off was taken to its limit resulting in the simplest form of A/D and D/A converters possible providing that circuitry was realisable with state-of-the-art L.S.I. technology. Fig. 1 shows a block schematic of the basic codec.

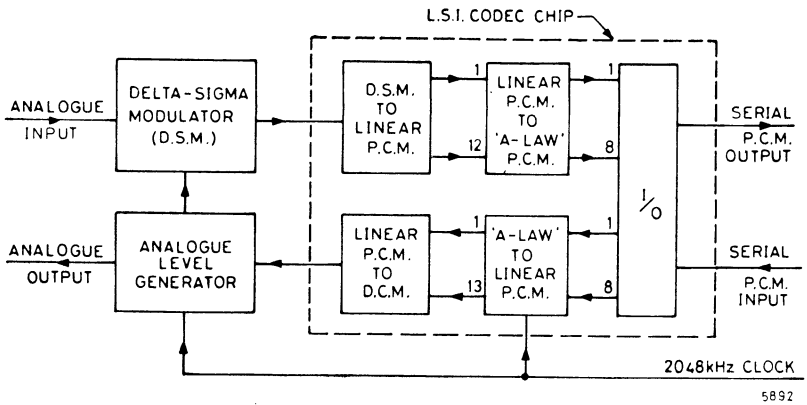


Fig. 1. Codec Schematic

The intermediate code format chosen for both encoder and decoder is that produced by a delta sigma modulator (dsm). It is especially simple to convert from this format back to analogue as one only has to pass the digital stream through a low pass filter cutting off just above the highest signal frequency to be recovered (3.4 kHz).

The area enclosed by the dotted line indicates the functions integrated into the L.S.I. codec chip ZNPCM1. The dsm circuitry is presently realised using discrete TTL logic, a differential amplifier, resistors and capacitors. However under development at present at Ferranti is an I.C. dsm solution which will be available by mid-1979.

THE DELTA SIGMA MODULATOR (DSM)

A modified form of delta sigma modulator/demodulator is used, resulting in an adequate performance using a clock rate as low as 2.048 kHz. Fig. 2 shows the functional circuit of the dsm, incorporating an operational amplifier integrator, and a D-type bistable for the threshold detector and approximation level generator. The modulator accepts a band-limited analogue input signal (300-3400 Hz) and converts it to one bit/sample delta sigma code format at a high sampling rate. The demodulator produces one of two precisely defined analogue levels in response to the single bit/sample delta sigma bit stream.

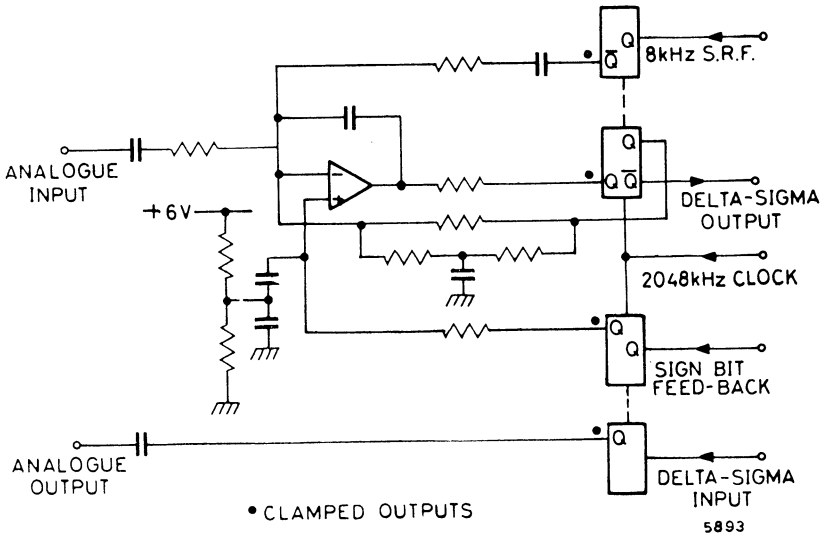


Fig. 2. Modulator/Demodulator Circuit

The modulator circuit relies on the use of two logic signals being fed back from the code converter; the sign bit of the generated pcm codewords, used to control the d.c. alignment conditions, and an 8 kHz square wave (Spectral Redistribution Function) which is added to the input signal to improve performance. A complex feedback network is also used to feed back a higher level of quantisation noise below approximately 16 kHz to shift quantisation noise to higher frequencies where the code converter provides greater suppression. In the reverse direction the decoder delta sigma stream coming from the code converter is passed through a D-type bistable for edge re-timing and level definition before the required analogue signal is recovered by low-pass filtering.

Encoder and decoder gain errors due to initial component variations from their nominal values are corrected at a gain adjustment point in the system. The main requirement is on gain stability, rather than absolute gain. The gain is a factor of both resistor ratios and the D-type output voltages. The output voltages are stabilised by supplying the quad D-type from a 5 volt regulator, which is always associated with the codec, and clamping the high state output voltages to a 2.45V reference by the use of schottky diodes. These also help to match the voltages influencing the d.c. alignment conditions and minimise the effects of power supply variations and noise. Resistor ratio stability is obtained, together with a small modulator/demodulator physical size, by implementing the resistors and small capacitors as an in-line passive hybrid.

The modulator also includes a 'fast start' circuit to ensure rapid stabilisation of the d.c. conditions when the codec is powered-up. This is important when the codec is used in switching applications where considerable power savings arise if the codec is only powered-up when required.

The detail circuit of the dsm is shown in Fig. 3. In addition to the basic modulator and demodulator circuit the decoded output is shown being fed into a simple second order Sallen and Key filter. This is shown as a technique for demonstrating the equalisation of sin.x/x distortion resulting from the sample and hold process of the decode function. The compensation would normally be provided as an integral part of the decoder band limiting filter.

Ferranti have under development an integrated circuit version of the dsm and samples will be available by mid-1979. The I.C. version will be much less dependent on external component tolerances than the discrete version. Only 7 or 8 external R and Cs will be required. The I.C. will be available in an 18 pin plastic or ceramic package and should also allow improved speed performance compared to the discrete solution. Fig. 4 shows an advance drawing of what the two I.C. single channel codec is expected to be, however this may be subject to change depending upon the final evaluation of the dsm integrated circuit.

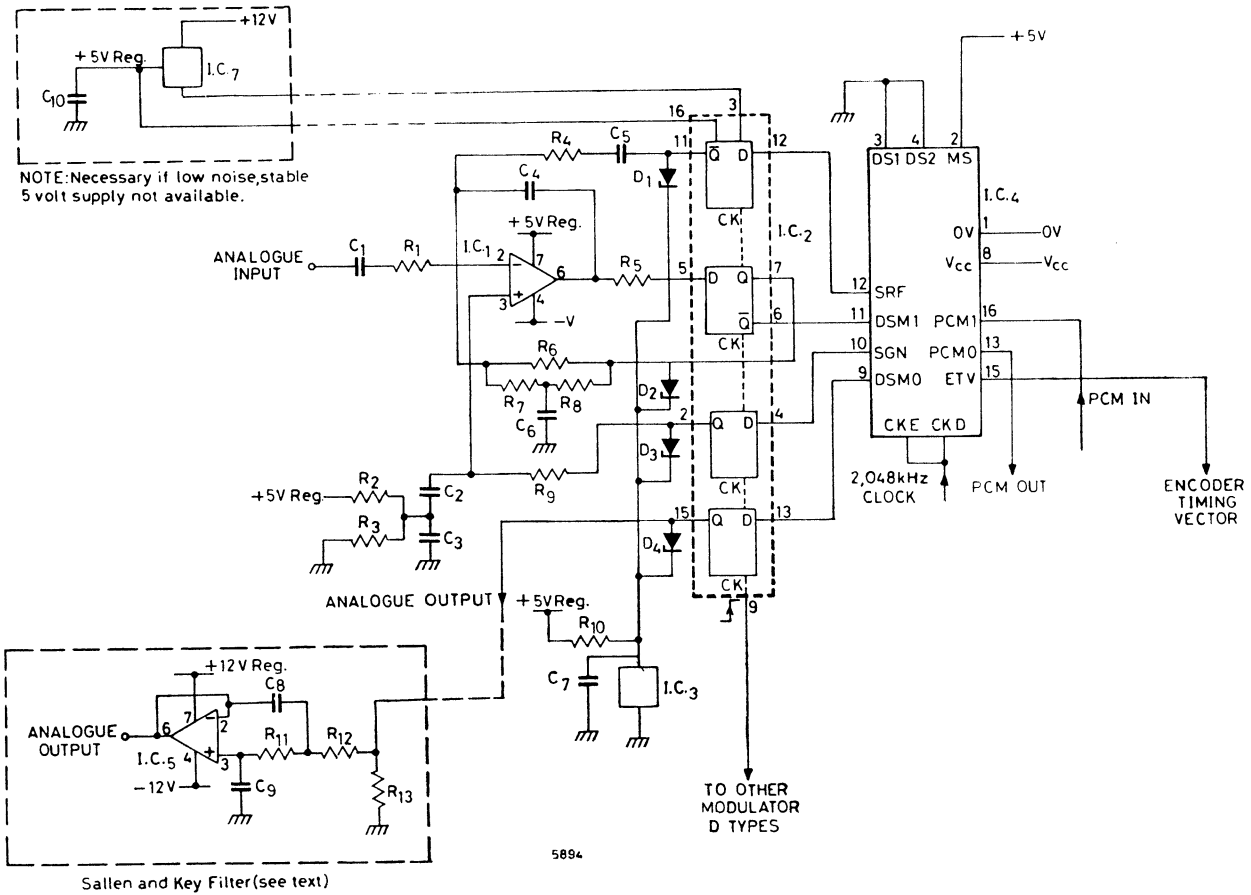


Fig. 3. Discrete Delta Sigma Modulation Circuit

COMPONENTS LISTING FOR COMPLETE CODEC CIRCUIT

1. MAIN CIRCUIT

Integrated Circuits

I.C.1	—	CA3140S/T
I.C.2	—	SN74175N J or ZN74175 E/J
I.C.3	—	ZN458
I.C.4	—	ZNPCM1E or J

Diodes

D1, D2, D3 and D4	—	ZC2800 or 1N6263

Capacitors

C1	—	3.3 μF ±20%
C2 & C3	—	6.8 μF ±20% (6.3V)
C4	—	68 pF ±20% }
C5	—	15 nF ±10% } +15%, −18% (See Note 1)
C6	—	10 nF ±2% }
C7	—	6.8 μF ±20% (6.3V)

Resistors

R1	—	2.7kΩ ±2% (High Stability Resistor)
R2	—	10kΩ ±2%
R3	—	4.7kΩ ±2%
R4	—	47kΩ ±2%
R5	—	620Ω ±5%
R6	—	10kΩ ±2% (High Stability Resistor)
R7 and R8	—	2kΩ ±2% (High Stability Resistor)
R9	—	2.7kΩ ±10%
R10	—	260Ω ±10%

NOTE 1. Limits apply over temperature range and equipment working life.

NOTE 2. High stability resistors should track each other to ±1% to meet British Post Office Specification Requirements.

2. SUBSIDIARY CIRCUITS

Integrated Circuits

I.C.5	—	ZLD741C
I.C.7	—	LM78LO5ACH

Capacitors

C8	—	1 nF ±2%
C9	—	10 nF ±2%
C10	—	2.2 μF ±20%

Resistors

R11 & R12	—	91.8kΩ ±1%
R13	—	100kΩ ±5%

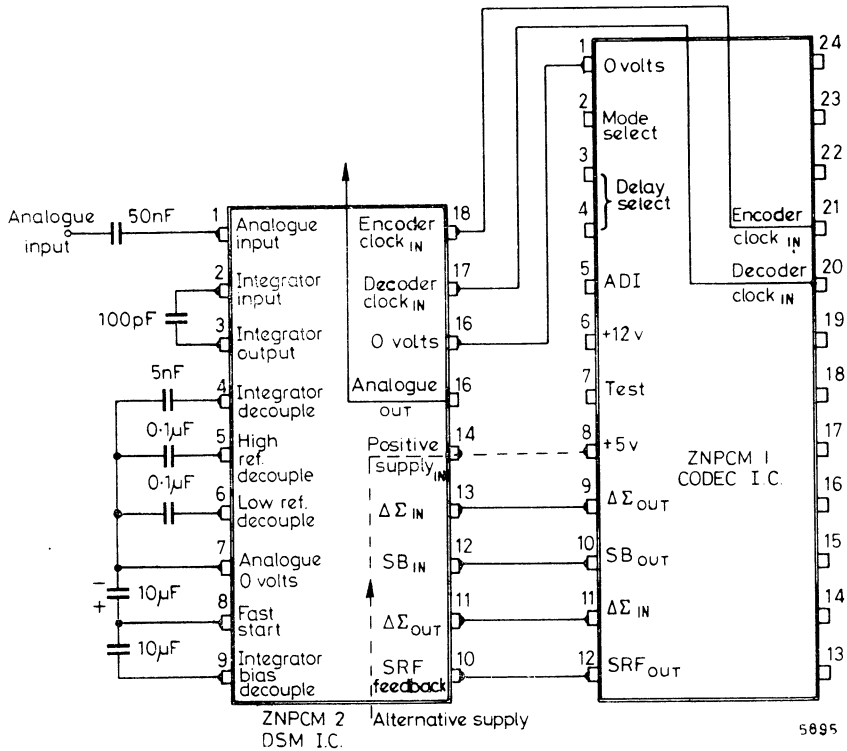


Fig. 4. DSM-Codec Interface

THE CODE CONVERSION

The dsm signal is fed into the integrated circuit at 2,048 kbits/second and converted to compressed pcm at a bit rate of 64 kbits/s or, by the application of external timing signals a maximum of 2,048 kbits/s for multiplexing in a burst format. Conversely the I.C. will accept at the pcm interface either a 64 kbit/s stream or, by the application of external timing signals, a bit rate of up to 2,048 kbit/s in a burst format. This is then converted to a delta sigma pulse stream of 2,048 kbit/s. The actual code conversion can be broken down into two stages; (i) Delta Sigma to linear pcm and vice-versa; (ii) Linear pcm to compressed pcm and vice-versa.

(i) *Delta sigma to Linear pcm*

The converter operates by multiplying the 256 delta sigma input samples occurring in each 125 microsecond pcm sample period by coefficients according to a triangular profile and accumulating the products to form the required linear pcm codeword at the end of the interval. Fig. 5 shows the converter logic structure.

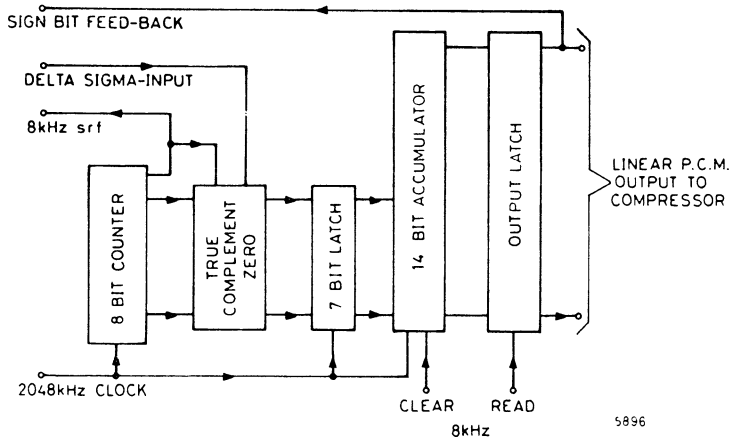


Fig. 5. Delta sigma to Linear pcm Converter

It consists of an eight bit counter, logic for operating on the seven least significant bits of the counter, a re-timing buffer, a 14 bit accumulator and an output latch. The first seven bits of the counter generate numbers zero to 127 as shown in Fig. 6(a). The eighth bit divides the generated number sawtooth into odd and even phases as shown in Fig. 6(b). Bit eight is also used in conjunction with the delta sigma ($\Delta\Sigma_i$) output to operate on the seven bit count sequence to produce the correct value of $\Delta\Sigma_i W_i$ to be added into the accumulator, where W_i is the required weight from the triangular profile during the ith clock period.

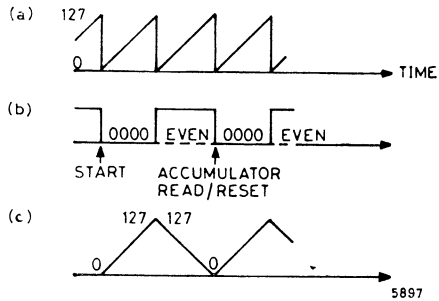


Fig. 6. a) 7 Bit Counter Number Sawtooth
b) Counter Most Significant Bit
c) Effective Available Weight Sequence

The technique of generating a triangular co-efficient profile allows a continuous up-counter to be used, which in turn allows the easy generation of the required timing waveforms to drive different parts of the codec. The 8 kHz square wave used within the modulator is taken from the most significant bit of the counter and the sign bit feedback to the modulator is derived from the output latch.

The converter produces 14 bit linear pcm codewords at 8k samples/s with an effective accuracy such that the signal to noise ratio obtained, after converting the 'A' law pcm, complies with C.C.I.T.T. recommendations.

In the decode direction the principle of conversion is the implementation of the delta sigma algorithm (see appendix 1) in all digital logic. The linear pcm input appears as a sample and held signal, the digital dsm performing a continuous conversion to the delta sigma format. The realisation of the circuitry is shown in Fig. 11.

(ii) *Linear PCM to Compressed PCM*

A useful relationship exists between linear pcm codewords and their 'A law' compressed equivalents allowing conversion between the two formats to be readily accomplished using data selection techniques. Fig. 7 shows a linear pcm to 'A law' pcm converter where the segment code is derived directly from the linear codeword using combinational logic. The segment code is then used to control a data selection matrix to extract the required interval code.

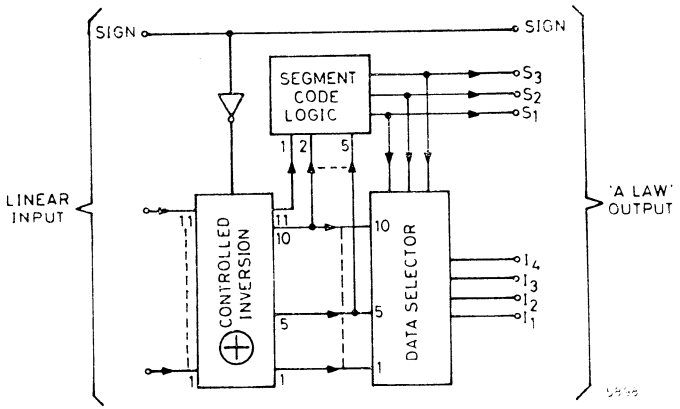


Fig. 7. Linear to 'A Law' Converter

Facilities are provided for controlled alternate digit inversion of the 'A law' codewords prior to parallel to serial conversion for serial output. In most applications ADI must be provided but for testing purposes it is useful if it can be removed.

Similar techniques are used in the decode direction to convert the compressed pcm into linear pcm.

INPUT-OUTPUT INTERFACE

One of the most important features of a pcm codec is the structure of its input-output interface as this directly influences the ease with which the codec can be used in a given application. A very flexible I/O interface has been included which can operate in either of two modes by means of pin selection.

In the first mode the pcm codewords are clocked in and out automatically at 64 kbits using clocks internally derived from the applied 2,048 kHz clock. The only timing waveform required is a timing vector to indicate when the first bit (the sign bit) of each codeword is required (which automatically defines the positions of the other bits at this rate). To take account of many applications where the received pcm codewords are not in the frame alignment with the transmitted codewords, two pins are provided for the user to strap appropriately to indicate the actual displacement. The four possibilities allow for zero to three digits delay of the received with respect to the transmitted codewords.

In the second mode, a much wider range of operation is possible. The pcm codewords may be clocked in and out at any rate in the range 64 to 2,048 kbits. Access is provided to the output and input shift registers to allow the multiplexing and demultiplexing of signalling bits if required. Also separate encoder and decoder 2,048 kHz clock inputs are provided to allow asynchronous working between the two directions of transmission, which is typical of pcm multiplex applications.

ZNPCM1 – THE L.S.I. CODEC

From its initial conception the codec has been designed with a view to producing the circuit in an L.S.I. semiconductor technology. Using advanced circuit design, photographic mask making and processing techniques developed originally for the F100L 16 bit bipolar microprocessor[2] Ferranti have produced a single chip codec incorporating all the circuit functions shown in the dotted rectangle in Fig. 1. The device operates from a single 5V supply with a maximum operating frequency of 6 MHz and all inputs and outputs are TTL compatible. For reduced power requirements the device will operate down to 3.5V maintaining TTL compatibility and as low as 3V with some degradation of input/output voltage levels.

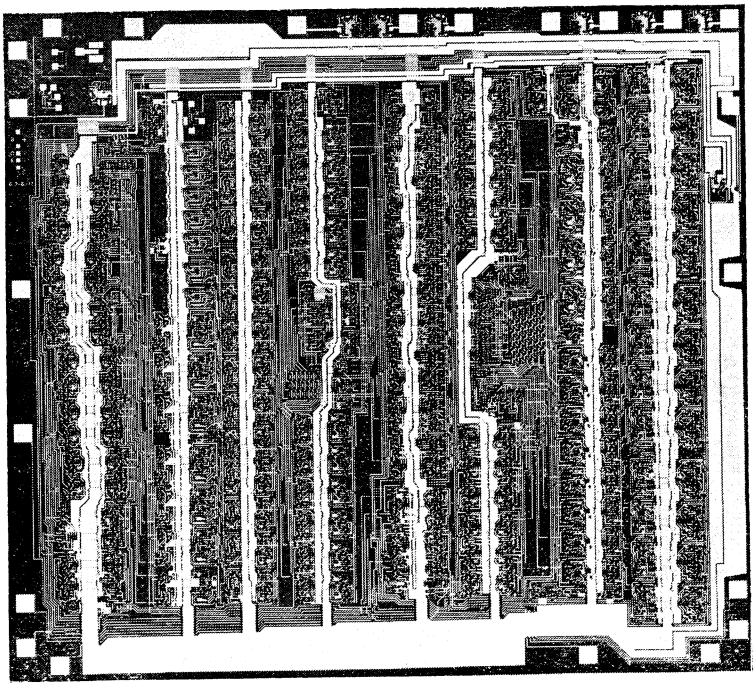


Fig. 8. Codec Chip Photograph

The chip size is 178 thou. by 163 thou. (see Fig. 8) and is available in a 24 lead D.I.L. ceramic (ZNPCM1J) or moulded package (ZNPCM1E).

Performance

The codec described meets all the performance requirements of the C.C.I.T.T. Recommendation G712 with good safety margins. Using a standard pcm multiplex tester and a spectrum analyser the following performance figures result:

1. Idle channel noise: –69 dBmOp
   (C.C.I.T.T. recommendation = –65 dBmOp)

2. Signal-to-noise ratio and Gain-level linearity: Figs. 9(a) and 9(b) show the results using a 450-550 kHz pseudo-random noise test.

3. Intermodulation distortion:
   Measured products are at least 10 dB and on average 18 dB better than the C.C.I.T.T. recommendations.

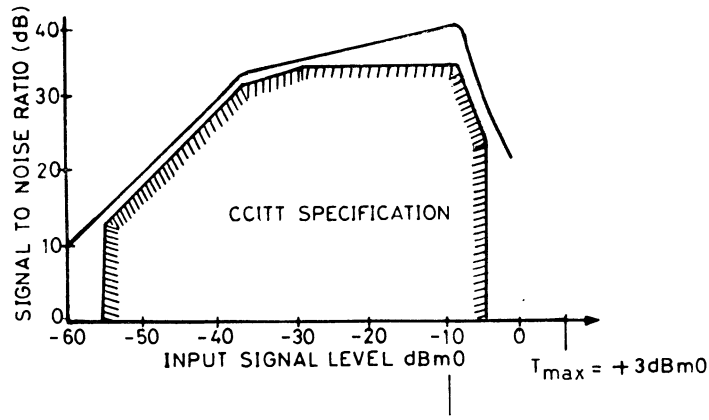


Fig. 9(a). Signal to Noise Ratio, 'A law'

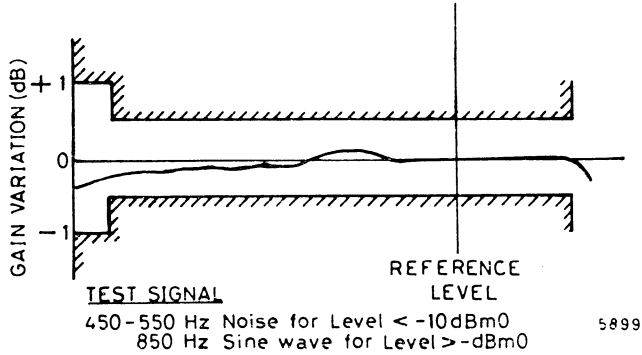


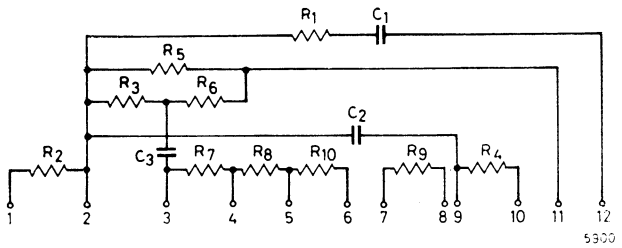
Fig. 9(b). Gain to Signal Level, 'A law'

Another aspect of the codec performance is the Sinc (π ft) decoder frequency characteristic, having infinite attenuation at 8 kHz and multiples thereof, introduced by the digital full-width sample and hold process occurring within the code converter. Although this requires equalisation in-band with an appropriate analogue post filter design, the characteristic ensures complete suppression of the sampling frequency components and harmonics, independent of any d.c. offset in the received codewords.

The sinc (π ft) characteristic is also useful when considering the design of less complex analogue filters to be used with the codec in digital switching applications, where codecs may be provided on a per customers line basis. A less complex filter may be allowable since, in the local telephone networks, there is not the problem of interworking with frequency division multiphase systems.

APPENDIX 1

DSM Hybrid



Component Values

R1	47kΩ	±5%	R4	620Ω	±20%
R2	2.7kΩ		R9	2.7MΩ	
R3	2kΩ		R10	260Ω	
R5	10kΩ				
R6	2kΩ				
R7	4.3kΩ				
R8	10kΩ				
C1	15 nF	+15%, −18%			
C2	68 pF				
C3	10 nF				

Resistor Ratio Tolerances

If, $R_p = \dfrac{(R_3 + R_6)\,R_5}{(R_3 + R_6 + R_5)}$

then R_p/R_2 shall commence with ±5% of the nominal ratio and then remain with ±1% of the starting ratio over operating temperature range and equipment life.

The ratios R_p/R_1 and $R_7/R_7 + R_8$ will remain within ±5% of nominal ratios.

The tolerances quoted are those required over the temperature range and working life to obtain a performance compatible with that required by the British Post Office and may be relaxed for less stringent requirements.

The hybrid is packaged in a single in-line package with 0,24 mm lead pitch and a maximum length of 33 mm, width of 6,35 mm and height of 17,8 mm. For further details contact:–

Type: CN466A

Allen Bradley Electronics Ltd.,
Bede Trading Estate,
Jarrow,
Tyne and Wear, NE32 3HG
Telephone: 0632 (Jarrow) 897771.

Type: TIM529

Tectronic (Electronics Ltd.),
Cirtec Works,
Wokingham,
Berkshire, RCH 2YD
Telephone: 0346 (Crowthorne) 5115.

APPENDIX 2

Fig. 10 shows the algebraic notation used for the numbers existing within the modulator during the nth clock cycle.

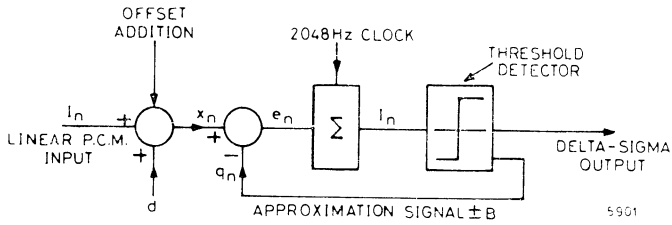


Fig. 10. The Digital DSM

The 13 bit linear pcm input I_n has a constant offset d added to it, resulting in a number $x_n = I_n + d$ being presented to the digital dsm. The offset d, equal to 1/16th of the peak pcm codeword magnitude, acts as a spectral redistribution function[3] which improves the performances considerably. The approximation signal q used in the feedback loop can take one of two binary numbers +B or −B. The difference $e_n = x_n - q_n$ is presented to a digital integrator. At the end of clock period 'n', e_n is added to I_n, the integral or sum of all previous differences to form $I_n + 1$.

$$\text{i.e., } I_n + 1 = I_n + e_n = \sum_{o}^{n} (x_i - q_i)$$

The threshold detector outputs the sign of $I_n + 1$ which is used to control the sign of the approximation signal during the $(n + 1)$th period the sign being chosen so as to minimise the integral,

$$\text{i.e., } q_n + 1 \text{ B sgn } (I_n + 1)$$

over a period of m dsm cycles

$$I_n = I_n - m + \sum_{n-m}^{m-1} (x_i - q_i)$$

Rearranging and dividing by m:

$$\frac{1}{m} \sum_{n-m}^{n-1} q_i = \frac{1}{m} \sum_{n-m}^{n-1} x_i - \frac{1}{m} (I_n - I_{(n\ m)})$$

i.e., the mean value of q over m cycles is equal to the mean value of the input x plus some error term. The larger the value of m the smaller the error term becomes. Viewed in the frequency domain the feedback loop causes the low frequency components of q to track the baseband frequency components of the input x, any difference being the inband quantisation noise due to the transformation or coding process.

Fig. 11 shows the circuit realisation of the digital dsm. The simplicity of the configuration arises from choosing the magnitude of the approximation levels $\pm B$, such that the difference between x_n and q_n can be formed by combinational logic techniques on the most significant bits of x_n and q_n without performing a full subtraction operation. Generalising, if x is represented by a two's complement number k bits in length, then,

$$-2^{k-1} \leqslant x \leqslant 2^{k-1} - 1$$

The two possible values of q are made

$$+B = 2^{k-1} \text{ and } -B = -2^{k-1}$$

As a consequence the $k + 1$ bit value of e can be formed by using the $k - 1$ least significant bits of x (unchanged) combined with two bits in the most significant positions which are inverses of the sign bits of x and q, hence the logic structure shown in Fig. 11. The digital dsm cycle rate is governed by the rate at which the accumulator latch is clocked, the delta sigma output being taken from the sign bit of the accumulator.

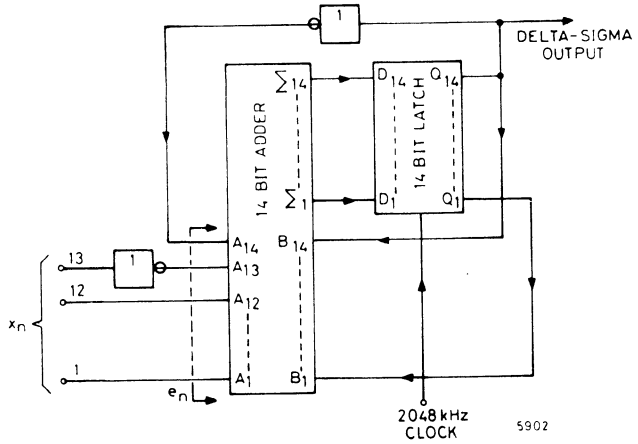


Fig. 11. Digital DSM Circuit Realisation

References

1. C.C.I.T.T. Orange Book Vol. III – 2 Rec. G711, 712.
2. F100L circuit, Design and Manufacture by Mr. D. Grundy – Electronic Equipment News, May 1978.
3. Everard, J.D. 'Single Channel PCM Codec' IEE Journal –Solid State CCTS Vol. COM 27 No. 2. Feb. 1979 par. 1 pp 25-38.

Introduction to a Monolithic 10-Bit Tracking ADC and how to Evaluate Design Performance

INTRODUCTION

The Ferranti ZN433 is a monolithic 10-bit tracking A to D converter and as its name implies, it is capable of following changing analogue inputs. It uses an UP/DOWN counter, a D/A and a window comparator as shown in the Schematic diagram (Fig. 1A). A window comparator is similar to a normal comparator except that, at the input, there is a 'dead band' or 'window' within which the output will not change state. This window is normally ± ½LSB wide.

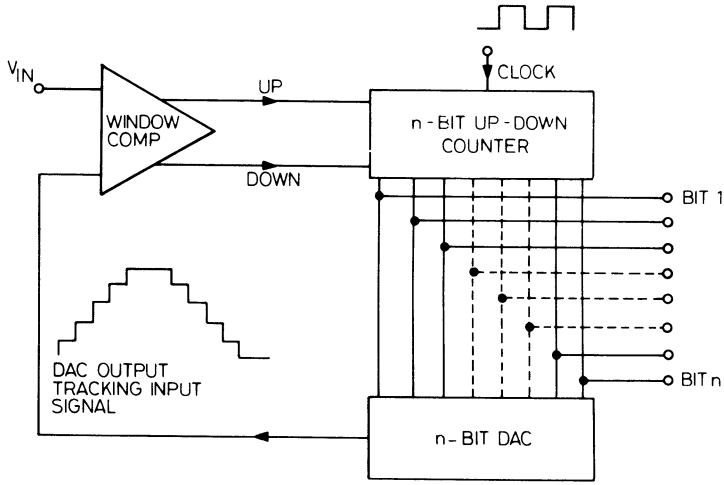


Fig. 1A TRACKING ADC

When the DAC output is less than the analogue input the comparator instructs the counter to count up and the DAC output thus increases. If the DAC output is greater than the analogue input the comparator causes the counter to count down, thus decreasing the DAC output. When the DAC output is equal to the analogue input ± ½LSB, the input is within the 'window' of the comparator and the counter is stopped. This is illustrated in Fig. 1B.

A tracking converter can have speed advantages over the staircase and compare and successive approximation type of converters, since the counter of the latter two can only count up and must therefore be reset between conversions.

If the rate of change of the analogue input is always less than 1LSB per clock period then a tracking converter will acquire and track accurately the input voltage and the conversion time will be one clock period. The staircase and compare converter would have to reset its counter to zero and then count up again until the new count is reached. A successive approximation converter would take at least n-½ clock pulses, where n is the number of bits.

As an extreme example consider an analogue input that changes from VFSO to (VFSO-1LSB). The staircase and compare converter will require $2^n - 1$ clock pulses for the first conversion and $2^n - 2$ clock pulses for the second conversion. The tracking converter on the other hand, will require $2^n - 1$ clock pulses for the first conversion but only 1 clock pulse for the second conversion. This is illustrated in Fig. 1C.

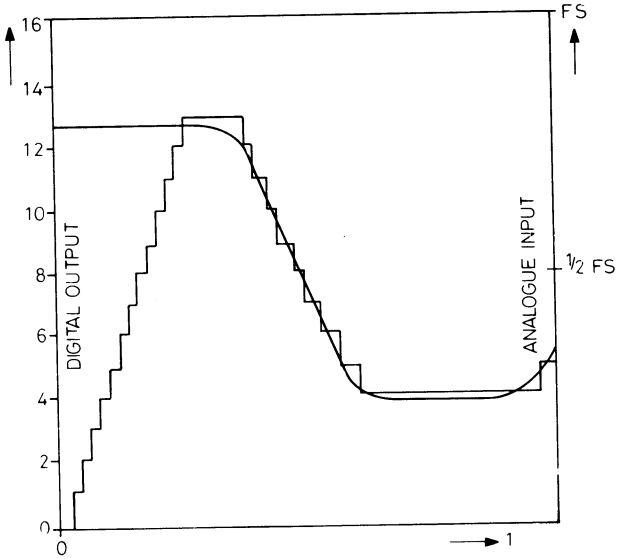


Fig. 1B OPERATION OF TRACKING ADC

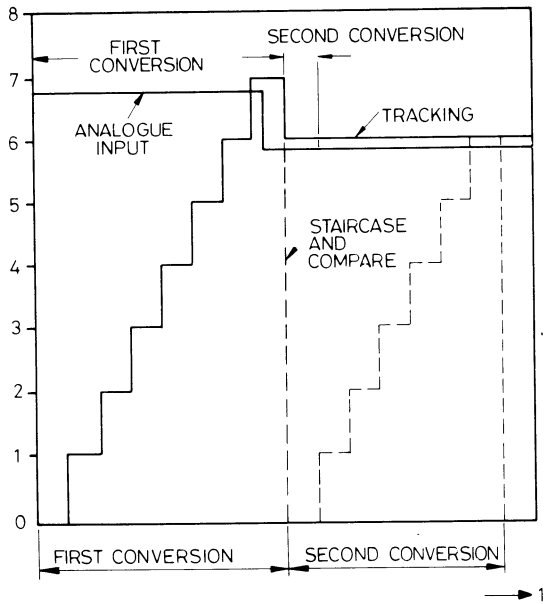


Fig. 1C COMPARISON OF RAMP AND COMPARE AND TRACKING ADCs

In general it can be said that a tracking converter will follow signals whose rate of change is less than $\pm$ 1LSB/clock period. If this condition is met there is no need to use a sample and hold circuit on the analogue input.

The Ferranti ZN433 has a maximum clock rate of 1MHz. It is capable of generating parallel or serial output data. The data can be latched (by pin 28) and read out serially or in parallel as required. If desired the outputs can also be disabled by applying a low to Send Data (pin 17).

The evaluation board is designed to be versatile in demonstrating the properties of the ZN433. The outputs can either drive LED's via inverting buffers and give a visual indication of the output states, or be connected to a bus via non-inverting tristate buffers. The outputs and $\overline{\text{Enables}}$ of these buffers are connected to a 20-way speedbloc connector (allowing data to be read as 1 or 2 bytes) as are the control pins for the ZN433 (allowing data latching and serial data manipulation).

The ZN433 can be driven from either an external or on board clock.

The Analogue input and power supplies enter via a 9-way D-type connector.

HOW THE ZN433 WORKS

The chip basically comprises a 2.5V reference, a reference amplifier, a D to A converter, an UP/DOWN counter controlled by a window comparator, and a data latch/shift register (see Fig. 2A).

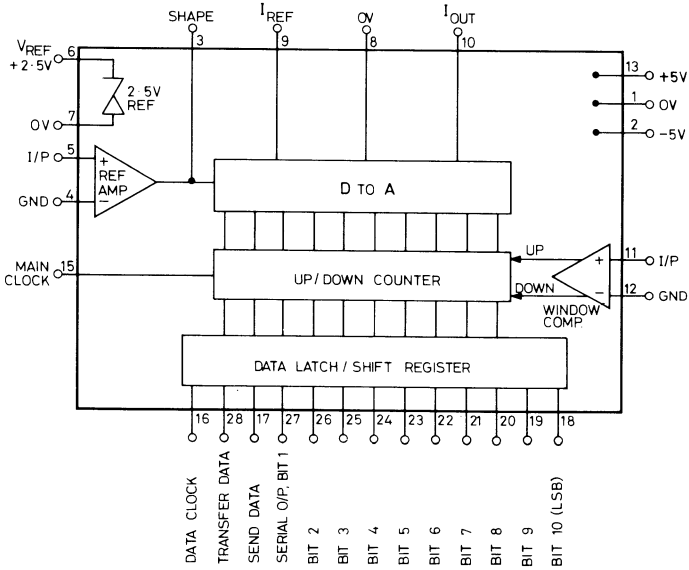


Fig. 2A SYSTEM DIAGRAM OF ZN433

At the heart of the device is the Current Source Array (C.S.A.) D to A converter (see Fig. 2B). The unit current in each source is controlled by the output of the reference amplifier (approximately 1.7V). If the logic input is higher than V_{bias} the current is switched to the 0V line, if not, the current is switched to the current summing line.

The bits are weighted by their number of current sources. Bit 1 has 16 current sources, bit 2 has 8, bit 5 has 1. Bits 6-10 current sources have a divide by 16 current divider. Bit 6 has 8 sources, bit 9 has 1. Bit 10 also has 1 but at half the unit current by using twice the resistor value for the emitter resistor. (This enables overall reduction in chip size due to the use of smaller resistors). Hence all the bits have correct weighting. The current sources for the different bits are interleaved to reduce any errors due to temperature gradients and process variations etc.

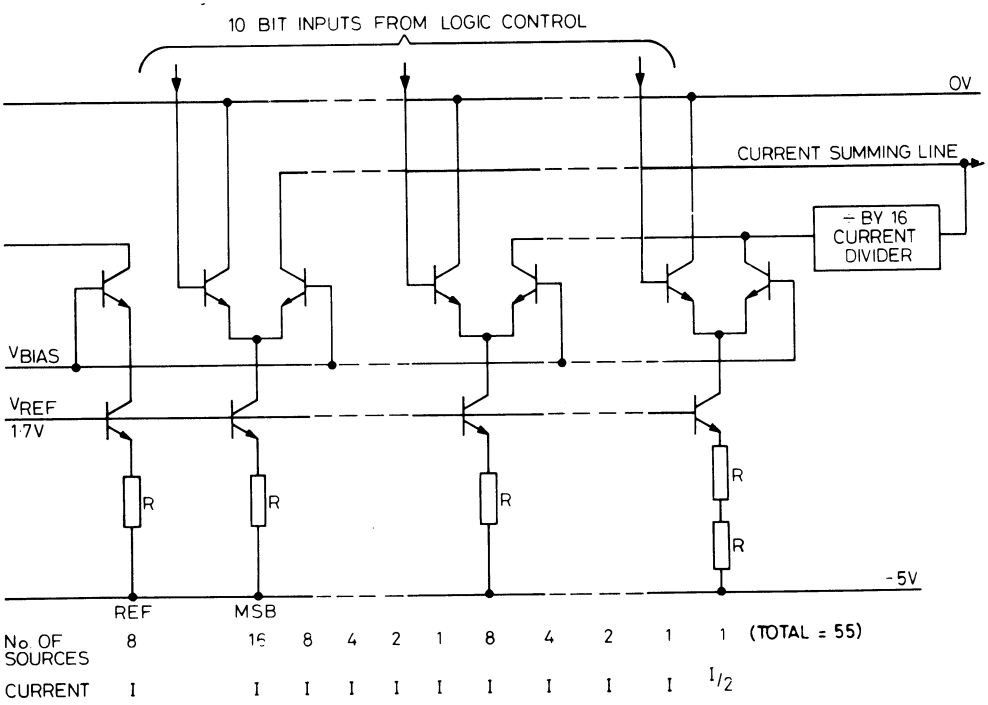


Fig. 2B CIRCUIT DIAGRAM OF CURRENT SOURCE ARRAY (C.S.A.)

There are 8 reference current sources distributed along the array. The reference amplifier controls these and also all the current sources for the bits.

The logic to control the current switching comes from the counter. The counter is instructed to COUNT UP, COUNT DOWN or HOLD by the window comparator. The 'window' is 1LSB wide.

If the input is within ± ½LSB of the digital outputs then the comparator output will instruct the counter to HOLD the count. This means the output will not hunt or exhibit hysteresis. If the input is not within ± ½LSB then the counter will count UP or DOWN as dictated by the comparator.

The counter outputs are connected to the Data Latch/Shift Register via transfer gates which are controlled by the Transfer Data Pin (pin 28). If pin 28 is held permantely high then the counter outputs will appear directly at the bit outputs. Data can be latched by taking Transfer Data high (150nS min.) after the main clock negative going edge and low again before the next main clock negative going edge (50nS min. pulse width). Data is latched on the negative going edge of the Transfer Data pulse. Once the data is latched it can be read out serially, from the MSB pin, by applying a data clock to pin 16 (1MHz max., min. pulse width 100nS). Also the outputs can be turned off at any time by applying a low to Send Data (pin 17). This means that the outputs of a few ZN433's can be wireAND-ed and each device selected individually for reading. However this may cause the V_{OL} of the selected device to exceed the normal TTL low level due to the extra sink current from the additional pull-up resistor(s) on the other device(s). If this presents a problem then the outputs can be connected to logic with a higher input threshold e.g. CMOS.

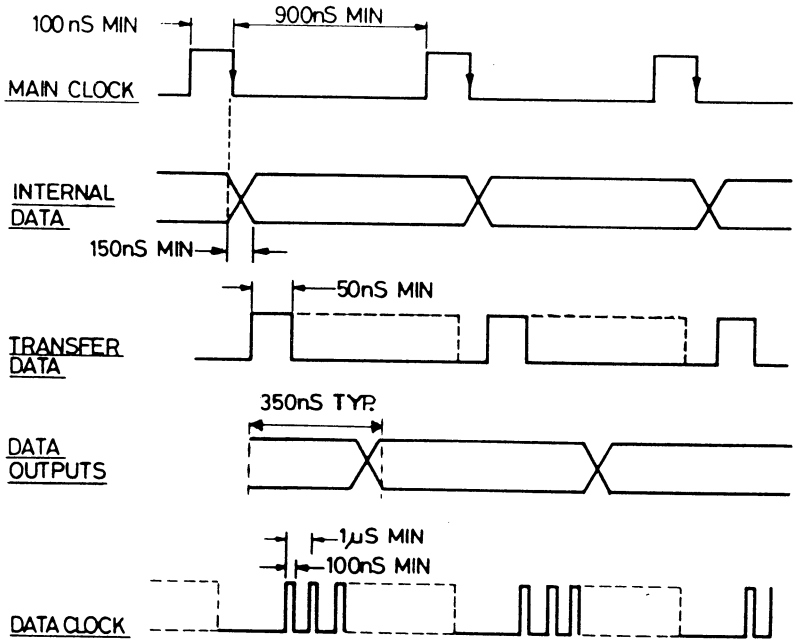


Fig. 3 TIMING DIAGRAM

EXTERNAL COMPONENT CONNECTIONS

Basically the only external components required for the ZN433 to function are two 1 microfarad capacitors and 6 resistors (or less). The basic connections are as shown overleaf.

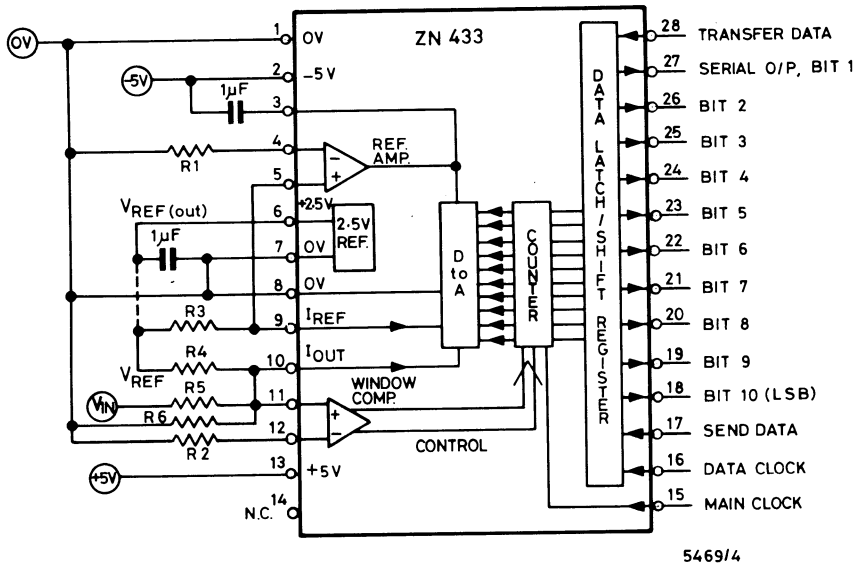


Fig. 4 BASIC COMPONENT CONNECTIONS

R1 and R2 tie the inverting inputs of the reference amplifier and the window comparator to ground. The resistance seen by the non-inverting inputs should be equal to that seen by the inverting inputs for low offset and good temperature performance.

R3 sets the reference current which should be 1mA. R4 is only needed when using a bipolar input voltage and is chosen to offset I_{out} as required. R5 is chosen to give a full-scale current of 4mA or if a bipolar voltage is used, a current swing of 4mA. R6 is chosen such that the resistance seen at the non-inverting input of the window comparator is the same as that seen at the inverting input. If a different reference voltage is used and hence a different R3, R1 should still be chosen to be equal to R3. R2 will always be 625ohms.

Resistors R3, R4 and R5 can affect offset and gain and thus require to be of high quality.

The two 1 microfarad capacitors are connected to stabilise the voltage reference and the output of the voltage reference amplifier.

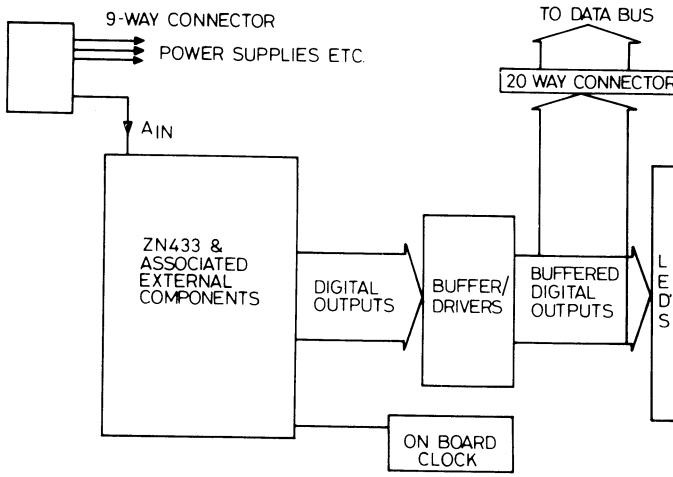


Fig. 5 SCHEMATIC DIAGRAM OF EVALUATION BOARD

The board basically consists of the ZN433 and associated components, an optional on board clock and buffer/drivers to drive either LED's or data bus lines. Inverting buffers are used to drive the LED's and non-inverting buffers are used to drive the bus lines via the 20-way connector. The supplies enter via the 9-way D-type connector.

The outputs from the buffers connect to both the LED's (via resistors) and the 20-way connector. If the LED's are not required they can be omitted and likewise if it is not required to connect to a bus, the 20-way connector can be omitted.

The supply tracks on the board have been made as large as possible in order to minimise any errors due to voltage drops.

The outputs of the ZN433 go to two 16 pin I.C. sockets. In these sockets can be placed either two 16 lead non-inverting buffer/drivers or two 14 lead inverting buffers. At first it may seem odd putting a 14 lead device in a 16 pin socket. The reason is that the 16 pin devices have two pins for controlling the tristate outputs. These are used for connections to a bus.

Obviously these 2 extra control pins are not required when driving LED's hence the use of 14 lead devices. The pin assignments for the two different devices are shown below.

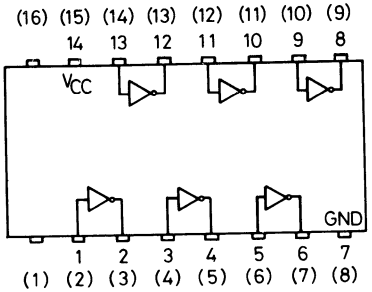


Fig. 6A PINNING FOR 7404, 7405 OR 7406

The numbers in brackets represent the corresponding socket pin numbers.

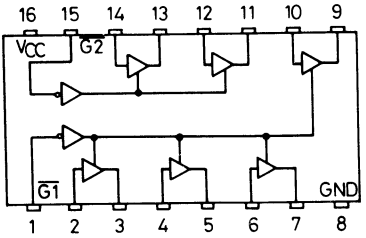


Fig. 6B PINNING FOR 74367

It can be seen that the 14 lead device can be placed in the 16 pin socket as shown and the inputs and outputs of the buffers will be the same for both devices. When the 14 pin device is used the socket pins 15 and 16 must be linked to provide its V_{CC}. As previously stated the outputs go to both the 20-way connector and to the LED's via resistors. By applying the appropriate control waveforms to pins 1 and 15 of the 74367 tristate buffers when certain outputs are connected together, data can be read in two successive bytes on an 8-bit bus.

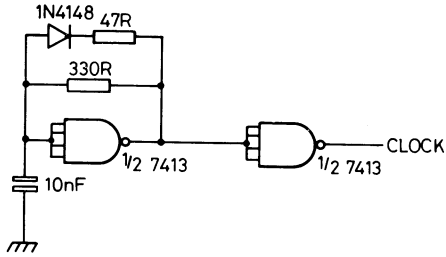


Fig. 7 ON BOARD CLOCK GENERATOR

The main clock can be generated on board using a TTL dual Schmitt trigger circuit as shown in Fig. 7. With the component values given in Fig. 7 the frequency is approximately 0.5MHz and the waveform as shown in Fig. 8.

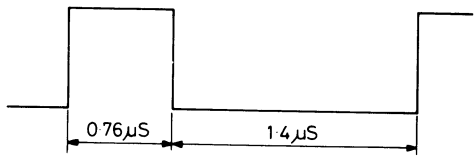


Fig. 8 ON BOARD CLOCK WAVEFORM

On the negative going edge of the clock the counter is instructed to count UP, DOWN or HOLD. The counter drives the D/A which needs 900ns to settle to the 10-bit accuracy required.

The window comparator compares the D/A output with the Analogue input. The positive going edge of the clock then latches the comparator outputs which subsequently set the counter. The clock must stay high for a minimum of 100ns.

Providing the clock low period is at least 900ns and the high period at least 100ns as stated, the duty cycle doesn't matter. This means that below about 550kHz the clock can be symmetrical because the low period will always be at least 900ns.

If the on board clock is not required, the clock components can be omitted and the ZN433 can be driven from an external clock. This can enter via the 20-way speedbloc connector or can enter the board just below the LED's. Here a round BNC connector can either be secured to the board digital ground track directly or be mounted on a bracket which connects to the digital ground track. Connection can then be made to the clock line. Alternatively, the clock input can be soldered to terminal pins at these points.

The maximum Analogue input frequency that the ZN433 can track accurately is related to the clock frequency and also the input signal amplitude. The outputs can only change 1LSB at a time and so the input signal must not change by more than 1LSB/clock period.

At its maximum rate of change, the ZN433 would take 2^{10} or 1024 clock cycles for its outputs to ramp up from zero (or $-$ full-scale) to + full-scale. Likewise 1024 clock cycles would be needed to ramp back down. Thus 2048 clock cycles are needed for a full-scale change from zero (or -f.s.) to + f.s. and back again. This corresponds to one cycle of a full-scale triangular wave. With a 1MHz clock applied, the ZN433 can accurately track an input signal which changes less than 1LSB/μS. This means that it can track a full-scale triangular wave input upto a frequency of $^1/_{2048\mu S} = 488$Hz. The maximum full-scale sinewave frequency is about 311Hz - due to the fact that the rate of change is not constant but is greatest around zero, hence the maximum slew rate is encountered here.

The maximum frequency that can be tracked is increased when the input signal amplitude is reduced e.g. a half full-scale sinewave input can be tracked up to a frequency of 622Hz etc. However this does mean that resolution is effectively reduced.

The complete circuit diagram for the circuit board is shown in Fig. 9. The resistor numbers are the same as used in the diagram on page 2 of the data sheet, where applicable. Resistors R3A and R3B make up the resistor R3 in the data sheet. R3A allows the gain to be adjusted. R4A, R4B and R4C make up resistor R4 in the data sheet and R4B allows the zero offset to be adjusted. R4C is only used when R4 is supposed to be infinite but offset is still required. Otherwise R4A is used with R4B to provide the adjustment, R4C being omitted.

BOARD USED WITH LED DISPLAYS

Primarily to give a visual indication of the state of the outputs during device evaluation. In this configuration the 14 lead inverters are used with pin 1 of the device in pin 2 of the socket etc. Pin 16 of the socket has to be linked to pin 15 of the socket to supply V_{CC} to the inverters.

For parallel output data, transfer data (pin 28), data clock (pin 16) and send data (pin 17) must all be taken high through links (J4, J5 and J6). If serial output data is required then these pins are used to control the latching and movement of the data (see data sheet). They can be accessed via the 20-way connector.

If serial data is not required, this connector can be omitted.

BOARD USED FOR CONNECTION TO A BUS SYSTEM

The 20-way connector allows the ZN433 outputs to be latched and subsequently read via tri-state outputs. Hence the 16 lead non-inverting buffers are used (74367's). The LED's and their resistors need not be connected. However if they are connected, the LED's will be off when the buffer outputs are high or are in the high impedance state!

The outputs of the buffers connect directly to the 20-way connector and so do their control pins to enable them to be turned off as required. Also connected to the 20-way connector are: the ZN433 clock, the transfer data and data clock to allow manipulation of serial data, the send data to turn off all the outputs thus sending them high.

The bit outputs are arranged so that if pin 1, IC2 is linked to pin 1, IC3 (with J12) then bits 3 to 8 will be under the control of this common connection. These $\overline{\text{Enable}}$ pins correspond to 10b and 6b on the 20-way connector. Bits 1 and 2 are controlled by pin 15, IC2 (10a) and bits 9 and 10 are controlled by pin 15, IC3 (5b). The outputs are enabled when the $\overline{\text{Enable}}$ pins are taken low and are in the high impedance state when the $\overline{\text{Enable}}$ pins are taken high.

This arrangement allows the outputs to be read as two words with either bits 1 to 8 and bits 9 and 10 or bits 1 and 2 and bits 3 to 10 as the two words. This is illustrated in the following table:

20-Way Connector Pins			Outputs Selected
10a	5b	10b and 6b linked	
L	L	L	All bits
L	H	L	Bits 1 to 8
H	L	H	Bits 9 and 10
L	H	H	Bits 1 and 2
H	L	L	Bits 3 to 10
H	H	H	No bits

TABLE 1

Also, as can be seen in the table, all the outputs can be disabled or enabled at the same time.

BOARD USED WITH EXTERNAL CLOCK

Here the on board clock components can be omitted. Using an external clock enables the ZN433 to be run at any desired frequency within its range. This would be useful if it is wished to synchronise the ZN433 with some other system.

The use of an external clock would probably give better results than the on board clock because the latter tends to generate a lot of noise.

OFFSET AND GAIN SETTING PROCEDURE

The offset and gain are adjusted by R4B and R3A respectively. These are placed near the edge of the board for easy adjustment. The value of the fixed and variable resistor in each case is such that together their values can be adjusted to around the value stated in the data sheet i.e. R3A + R3B = R3, R4A + R4B = R4 (remember R4C is only used when R4 = ∞). The value of the variable resistors is dependant on how fine the adjustment is required to be, but the combination must be chosen to allow sufficient adjustment. The resistors must be of high stability.

Unipolar Operation

R4B is used to adjust the zero, it should be adjusted so that for an input of ½LSB, the LSB just flickers between '0' and '1' with all the other bits at '0'. R3A is used to adjust the gain. This should be adjusted so that for an input of full-scale − 1½LSB, the LSB just flickers between '0' and '1' with all the other bits at '1'.

The setting of one control may affect the other so the above procedure should be repeated until both settings are satisfactory.

Bipolar Operation

Again R4B adjusts the offset but this time the input is − (full-scale − ½LSB). Again the LSB is required to flicker between '0' and '1' with all the other bits at '0'.

R3A adjusts the gain as above. For an input of full-scale − 1½LSB, R3A is adjusted until the LSB just flickers between '0' and '1' with all the other bits at '1', as for unipolar operation.

The procedure should again be repeated until both settings are satisfactory.

9-WAY CONNECTOR

Pins 2 and 7 are not connected. The wipers of R3A and R4B connect to the voltage reference which is brought out to pin 1. This allows an external reference to be used. The external reference and the internal reference share the same decoupling point on the analogue ground - as they will not both need it at the same time. A capacitor decoupling the external reference can thus be positioned 90° anti clockwise to C5 (the internal reference decoupling capacitor). The internal reference (pin 6) on the ZN433, can be connected to the wipers of R3A and R4B via a link (J2).

The analogue input enters via pin 6. The analogue and digital grounds connect to pins 4 and 8 respectively, and may either be connected together near the chip (using J3) or brought out separately depending on which will give the best results for a particular application.

The − 5V and + 5V supplies connect to pins 3 and 5 respectively and the + 5V auxiliary supply is connected to pin 9. If desired this auxiliary supply can be linked to the + 5V supply (with J1) and used for example to power an external transducer.

Note: The above pin connections apply when the 9-way P.C.B. connector is a socket and will be different if a plug is used.

USING THE BOARD WITH DIFFERENT INPUT VOLTAGE RANGES

Whatever maximum analogue input voltage is used I_{ref} should always be about 1mA and I_{out} full-scale should always be about 4mA. Thus in order to accommodate different input voltage ranges and different reference voltages, the resistors associated with these currents must be changed. How these resistors are calculated and a table of calculated values, for various input voltages, are given in the data sheet.

BOARD LINKS

Optional:

J1 – Links the board +5V to the auxiliary +5V on the 9-way connector to provide a +5V auxiliary output.

J2 – Applies the internal reference to the ZN433 and thus configures the board for operation with the on chip 2.5V reference.

J3 – Connects the Analogue and Digital grounds together near the ZN433 - may be desirable in some applications.

J4 – Ties Transfer Data (pin 28) high making the output data latch transparant. Used when the data does not need to be latched.

J5 and J6 – Tie Send Data and Data Clock high. Used when the outputs do not need to be turned off, and when serial output data is not required.

J9 and J13 – Connect +5V to the 14 lead inverters, if they are chosen to drive the LED's.

J12 – Links 6b and 10b (on the 20-way connector) together to allow either pin to control bits 3 to 8.

J14 – Links on board clock output to ZN433 clock input, when the on board clock is required.

Mandatory:

J7 and J8 – Provide the ground connections for IC2 and IC3.

J10 – Links bit 2 output from IC2 to the 20-way connector and the relevant LED feed resistor.

J11 – Connects +5V to IC3 socket - pin 16.

COMPONENT LIST

I.C.'s

I.C. 1	=	ZN433
I.C. 2	=	7404 or 74367
I.C. 3	=	7404 or 74367
I.C. 4	=	7413

Resistors

Depending on Input Voltage Range

R1	=	2.4K
R2	=	620R
R3A	=	1K 20 turn trimpot
R3B	=	1.8K
R4A	=	100K
R4B	=	1M 20 turn trimpot
R4C	=	100K
R5	=	620R
R6	=	∞
R7-R16	=	330R
R17	=	330R
R18	=	47R

Capacitors

C1	=	100μF electrolytic - axial
C2	=	100μF electrolytic - axial
C3	=	0.1μF disc ceramic
C4	=	1μF tantalum bead
C5	=	1μF tantalum bead
C6	=	0.1μF disc ceramic
C7	=	0.1μF disc ceramic
C8	=	10nF ceramic
C9	=	100μF tantalum bead

Miscellaneous

D1-D10	=	LED's
D11	=	1N4148
I.C. 2 socket	=	16 pin DIL socket
I.C. 3 socket	=	16 pin DIL socket
I.C. 4 socket	=	14 pin DIL socket

Connectors

9-way connector	=	D-type sub miniature
20-way connector	=	Speedbloc system
Round chassis mounting connector	=	BNC type

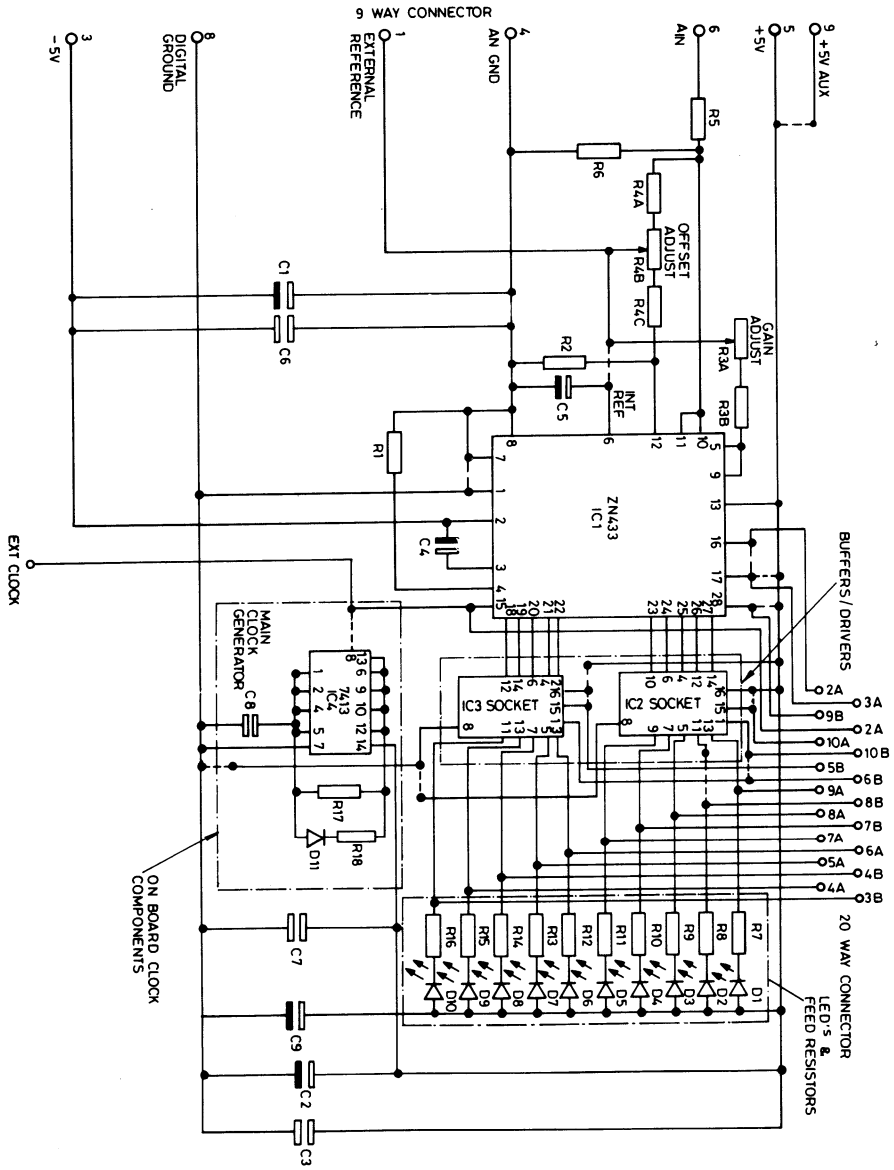


Fig. 9 EVALUATION BOARD CIRCUIT DIAGRAM

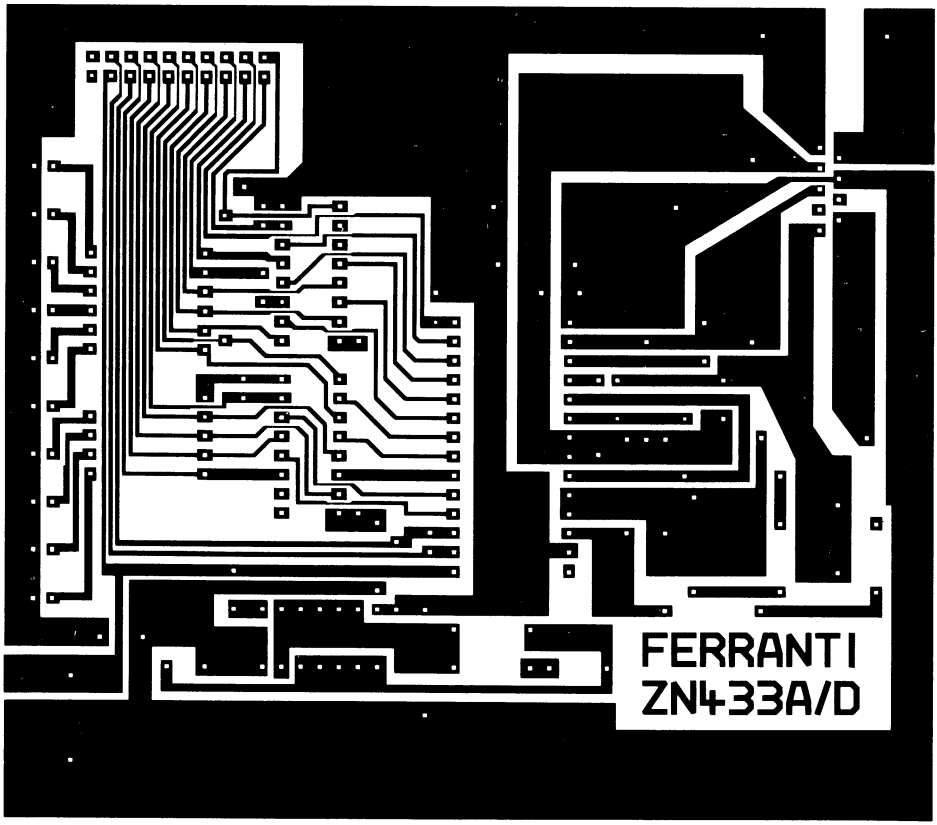


Fig. 10 P.B.C. PATTERN - ACTUAL SIZE
(Viewed from Copper Side)

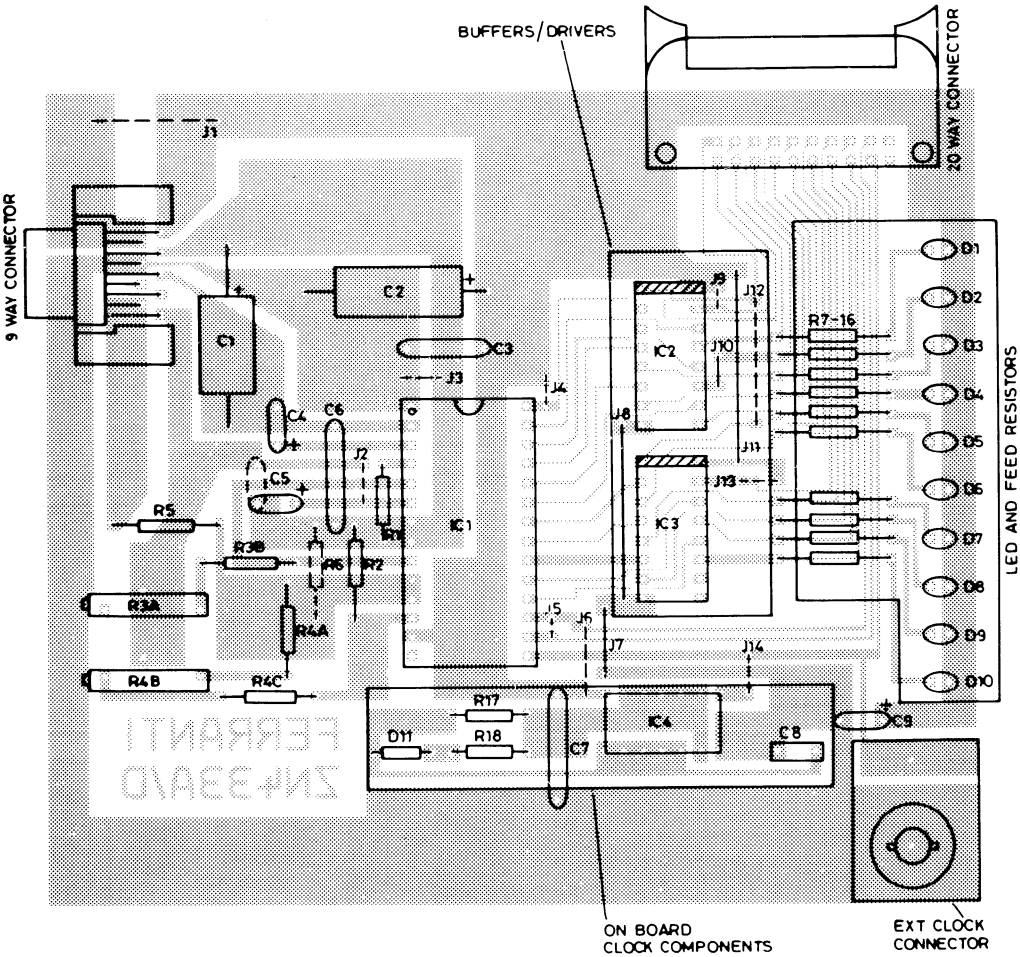


Fig. 11 COMPONENT LAYOUT - ACTUAL SIZE

PIN ASSIGNMENT FOR CONNECTORS

9-Way D-Type Socket

1	=	External Reference
2	=	N.C.
3	=	−5V Supply
4	=	Analogue Ground
5	=	+5V Supply
6	=	A_{IN}
7	=	N.C.
8	=	Digital Ground
9	=	Auxiliary +5V

TABLE 2

20-Way, Speedbloc Plug

1a	=	N.C.	1b	=	N.C.
2a	=	Main clock	2b	=	Data clock
3a	=	Send Data	3b	=	bit 10
4a	=	bit 9	4b	=	bit 8
5a	=	bit 7	5b	=	I.C. 3, Output $\overline{\text{Enable}}$ 2
6a	=	bit 6	6b	=	I.C. 3, Output $\overline{\text{Enable}}$ 1
7a	=	bit 5	7b	=	bit 4
8a	=	bit 3	8b	=	bit 2
9a	=	bit 1	9b	=	Transfer Data
10a	=	I.C. 2, Output $\overline{\text{Enable}}$ 2	10b	=	I.C. 2, Output $\overline{\text{Enable}}$ 1

TABLE 3

8. Quality Assurance Program

Contents

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Ferranti Quality Assurance Program	8-2
Processing	8-2
Assembly	8-2
Screening	8-5
Testing	8-5
Quality Assurance	8-5
Acceptable Quality Levels	8-6

8. QUALITY ASSURANCE PROGRAMME

The quality control procedures at Ferranti Electronics Limited are based on British Standard 9000, the relevant documents being:

BS 9002: Qualified products list for electronic components of assessed quality (including list of approved firms).

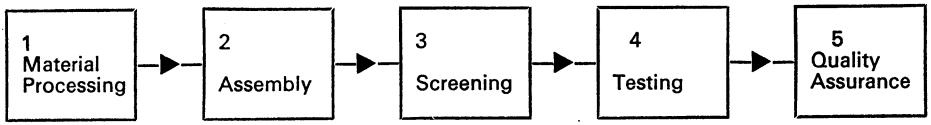
BS 9400: Integrated electronic circuits and micro-assemblies of assessed quality.

BS 9450: Custom-built integrated circuits of assessed quality.

BS 6001: Sampling procedures and tables for inspection by attributes.

The quality emphasis at Ferranti is on process control (as indicated by the use of many monitors and audits) in addition to gate inspections. This philosophy is consistent with building in quality and reliability rather than attempting solely to screen for it.

There are five basic stages in the manufacture of Ferranti data converters, as shown below:



Each of these stages has associated with it a number of quality control checks to ensure that components will meet the standards required by the most stringent environments encountered in the field of electronics.

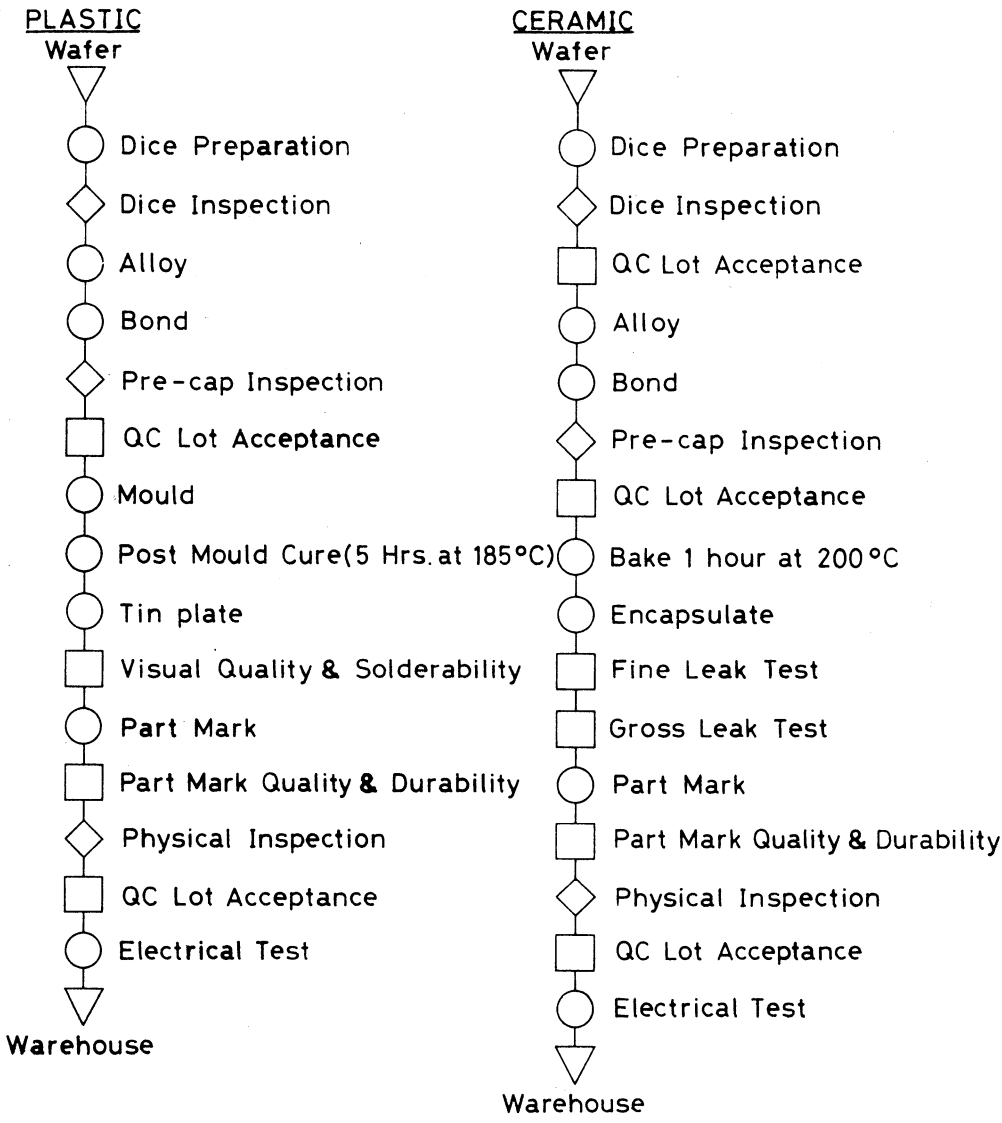
8.1 Processing

The technology used to fabricate the Ferranti range of data converters is a five mask bipolar process (see publication ref. ESA 480673). This process is used to manufacture the whole range of Ferranti LSI products, but is especially suited to converter products since it allows analogue and digital circuits to be fabricated on the same chip, with good yields and high packing densities. The process has full BS 9450 capability approval and is the first bipolar process in the U.K. to receive such approval.

8.2 Assembly

Ferranti data converters are available in either moulded or hermetically sealed ceramic dual in-line (DIL) packages (though certain types are available only in ceramic package). The assembly flow-charts for both types of package are shown in Table 1. All products are manufactured by the same routes and using the same techniques as BS 9000 approved products.

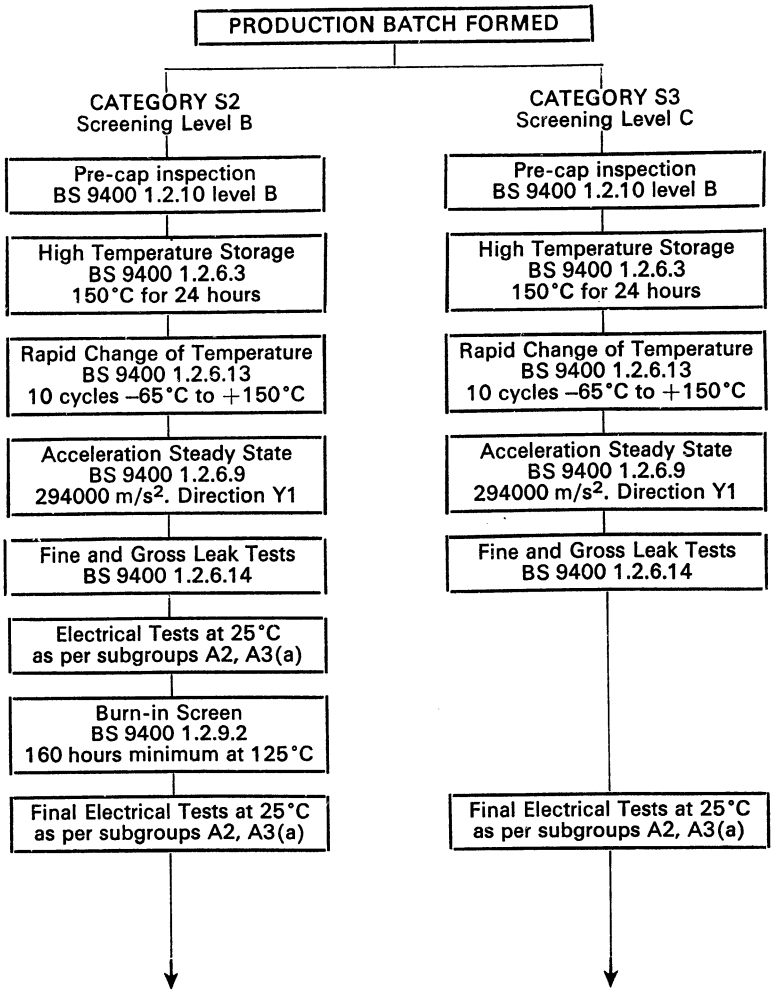
Q A Programme



6083

Q A Programme

TABLE 2



8.3 Screening

In addition to the standard manufacturing cycle, optional screening procedures are available to produce high-reliability products. A full breakdown of the options available, related to their BS 9400 procedures, is shown in Table 2.

8.4 Testing

On completion of assembly all devices are subjected to 100% functional and d.c. testing in addition to either an S4, 2.5% sample or 100% check on a.c. characteristics depending on device type. The d.c. tests are inset to tighter limits than those shown on the data sheet in order to ensure that the device will function within the specified conditions over its full operating temperature range.

In addition to the 100% test already described, devices manufactured to commercial specifications also undergo sample tests to the AQLs in Table 3, including the temperature extreme tests mentioned above.

TABLE 3

Inspected Parameter	Inspection Level	AQL
Visual & Mechanical including major external workmanship and marking permanency	I	1%
Function	II	0.15%
Major Electrical Parameters at $T_{amb} = 25°C$	II	0.65%
Major Electrical Parameters over operating temperature range	II	2.5%

8.5 Quality Assurance

Despite all the measures taken to ensure that commercial product is of a high standard it is inevitable that certain market sectors will require a higher level of quality assurance. These market sectors are predominantly military and telecommunications orientated.

Wherever devices are supplied to these more stringent QA requirements they are re-routed at the end of the assembly cycle through our QA Bond Department. They are subjected, on a lot-by-lot basis, to a more rigorous examination of ther quality using methods laid down in BS 9000 or its equivalent for the specification concerned.

In addition to lot-by-lot testing, long term life testing of product is performed continually. This enables constant monitoring of process stability and any undesirable deviations from the norm are quickly brought to light so that corrective measures may be implemented.

Q A Programme

8.6 Acceptable Quality Levels

As explained earlier the procedures and manufacturing techniques used by Ferranti are consistent with producing an inherently reliable product rather than screening out unreliable product. This is achieved by careful process control combined with numerous gate inspections.

In order for such a system to be effective it is necessary to implement a sampling procedure where the sample size and inspection levels of the various stages are adequate to assure satisfactory quality of the end product whilst remaining cost effective. This can be achieved only after a long history of semiconductor manufacture, which gives an intimate knowledge of the problems likely to arise at each stage of manufacture, and the best methods of inspecting for them.

The sampling procedures used by Ferranti are those outlined in BS 6001. The Acceptable Quality Level (AQL) is the maximum percentage of defective devices that can, for the purposes of inspection, be considered satisfactory as a process average.

The AQL sample size codes and sampling plan used by Ferranti are reproduced in tables 4 and 5.

Q A Programme

TABLE 4

SAMPLE SIZE CODE LETTERS

Lot or batch size			Special inspection levels				General inspection levels		
			S-1	S-2	S-3	S-4	I	II	III
2	to	8	A	A	A	A	A	A	B
9	to	15	A	A	A	A	A	B	C
16	to	25	A	A	B	B	B	C	D
26	to	50	A	B	B	C	C	D	E
51	to	90	B	B	C	C	C	E	F
91	to	150	B	B	C	D	D	F	G
151	to	280	B	C	D	E	E	G	H
281	to	500	B	C	D	E	F	H	J
501	to	1200	C	C	E	F	G	J	K
1201	to	3200	C	D	E	G	H	K	L
3201	to	10000	C	D	F	G	J	L	M
10001	to	35000	C	D	F	H	K	M	N
35001	to	150000	D	E	G	J	L	N	P
150001	to	500000	D	E	G	J	M	P	Q
500001	and	over	D	E	H	K	N	Q	R

Q A Programme – TABLE 4

Sample size code letter	Sample size	Acceptable Quality Levels (normal inspection)																									
		0.010	0.015	0.025	0.040	0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5	10	15	25	40	65	100	150	250	400	650	1000
		Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re	Ac Re
A	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↓	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31
B	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45
C	5	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	↑
D	8	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	↑	↑
E	13	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	30 31	44 45	↑	↑	↑
F	20	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑
G	32	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑
H	50	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑
J	80	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑
K	125	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
L	200	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
M	315	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
N	500	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
P	800	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
Q	1250	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑
R	2000	↑	↑	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑	↑

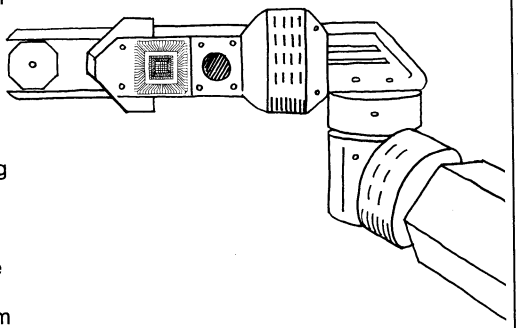
↓ = Use first sampling plan below arrow. If sample size equals, or exceeds, lot or batch size, do 100 percent inspection.

↑ = Use first sampling plan above arrow.

Ac = Acceptance number.

Re = Rejection number.

Semi-Kunden-ICs: Mehr als eine Philosophie



In Zeiten des immer härter werdenden Wettbewerbs in nahezu sämtlichen Industriebereichen sowie auf allen Märkten sind Produktentwicklungen von zum Teil völlig neuartigen Zielsetzungen geprägt. Faktoren wie Innovation, kurze Entwicklungszeit, Nachbauschutz, Ertragssicherung, Werbewirksamkeit oder Erschließung neuer Märkte rücken mehr und mehr in den Vordergrund, um der obersten Prämisse "Wettbewerbsfähigkeit" gerecht zu werden. Eine zunehmend dominante Rolle spielt hierbei die Mikroelektronik.

Modernste Technologien kommen zum Tragen, die geeignet sind, einem ganz speziellen Produkt seine Position im Markt zu verschaffen: die anwendungsspezifischen ICs. Integrierte Schaltkreise, die in wenigen Monaten für einen ganz spezifischen Anwendungsfall entwickelt und gefertigt werden, komplette Elektroniksysteme auf einem einzigen Chip enthalten, damit wesentlich raum- und energiesparender sind als der Aufbau einer Schaltung mit Standard-ICs oder als Hybrid-Schaltkreis, oft den Einsatz aufwendiger Mikroprozessorlösungen ersparen und vor allem von Mitbewerbern nicht nachempfunden werden können.

Außerdem wird mit dem Hilfsmittel des rechnergestützten Entwerfens von Semi-Kunden-ICs der Entwickler von zeitaufwendigen Routinearbeiten entlastet und gewinnt dadurch mehr Zeit für die eigentlichen kreativen Designaufgaben. Zeitraubende Zeichen-, Schreib-, Korrektur-, Kontroll- und Verifikationsaufgaben werden von CAD-Systemen übernommen und auf ein Minimum reduziert.

Die Überlegung – herkömmlicher Schaltungsentwurf oder Semi-Kunden-IC – gehört als eher philosophische Betrachtungsweise der Vergangenheit an: Ferranti-Semi-Kunden-ICs sind bei Stückzahlen von 500 bis über 500 000 pro Typ und Jahr in jedem Fall die wirtschaftlichere Alternative. Dies gilt für alle nur denkbaren Industriebereiche: angefangen von der MIL-Elektronik, wo Nachahmungsschutz und besonders hohe Zuverlässigkeit gegeben sein müssen, über den Telecom-Bereich, die Kfz- und Medizinelektronik bis hin zu hochwertigen Produkten der Computertechnik, Industrieautomation oder Unterhaltungselektronik.

Das Ferranti-Konzept

Im expandierenden Bereich der kundenspezifischen LSI- und VLSI-Schaltungen nimmt ein Konzept zusehends für sich in Anspruch, der wirkungsvollste Weg zur Realisierung von leistungsfähiger Technik, Wirtschaftlichkeit und Nachbauschutz zu sein: Semi-Kunden-ICs von Ferranti. Das von Ferranti entwickelte Konzept für anwendungsspezifische ICs gestattet die Integration analoger und digitaler Schaltungen auf einem einzigen Chip. Die große Palette von Gate-Arrays sowie Digilin-und Linear-Arrays in Bipolar-und CMOS-Technologien spiegelt die Erfahrung und vor allem die Bedeutung wider, die Ferranti seit 1972 als Pionier und Marktführer vorweisen kann.

Chip-Organisation

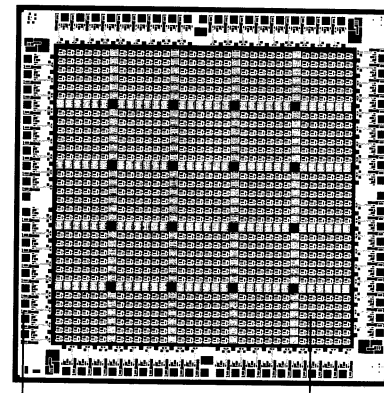
Die ULAs und Monochips von Ferranti sind eine Familie von serienmäßig vorgefertigten LSI- und VLSI-Schaltungen, die nur noch eine spezifische Aluminiumverdrahtung erhalten und damit zur Kundenschaltung werden. Bei den Gate-Arrays und Digilin-Arrays unterscheidet man auf dem Chip zwischen den Matrix- und Peripheriebereichen.

Matrix-Zellen

Jede der in einer Matrix regelmäßig angeordneten Zellen besteht aus einer Anzahl von Transistoren und Widerständen. Im Matrixbereich sind die digitalen Funktionen der VLSI-Schaltung untergebracht. Innerhalb jeder Komplexitätsstufe besteht die Möglichkeit, durch variable Auslegung der Matrixzellen die elektrischen Daten des Systems zu bestimmen.

Peripherie-Zellen

Diese Zellen bestehen aus einer Anzahl von unverdrahteten Bauelementen, mit denen Interface-Schaltungen und analoge Funktionen mit hohen Anforderungen integriert werden können.



Peripherie-Zelle — *für analoge und Interface-Funktionen*

Matrix-Zelle — *für digitale Funktionen*

Produktübersicht Semi-Kunden-ICs von Ferranti

Das Ferranti-Produktspektrum der anwendungsspezifischen ICs gliedert sich in drei große Bereiche: Gate-Arrays, Digilin-Arrays und Linear-Arrays. Ihnen gemeinsam ist ein jeweils fein abgestuftes Spektrum von Komplexitätsstufen. Der Arbeitstemperaturbereich ist innerhalb von −55 bis + 125°C spezifizierbar.

Bipolare **Gate-Arrays** ULAs

Gatter-komplexität	Clockfrequenz MHz	Gatter-laufzeit ns	Gatter-verlustl. µW	Peripherie-zellen	Bondpads	Typ
133	60	2,5	300	20	20	ULA1RA
133	20	7,5	90	20	20	ULA1RB
133	10	15	30	20	20	ULA1RC
133	3	60	8	20	20	ULA1RD
144	20	7	250	12	18	ULA1C
150	0,25	200	180	28	28	ULA1L
150	3	25	2100	28	28	ULA1
150	10	10	2800	28	28	ULA1H
314	60	2,5	300	30	30	ULA3RA
314	20	7,5	90	30	30	ULA3RB
314	10	15	30	30	30	ULA3RC
314	3	60	8	30	30	ULA3RD
337	0,25	200	180	40	40	ULA2L
337	3	25	2100	40	40	ULA2
337	10	10	2800	40	40	ULA2H
450	6	25	60	39	40	ULA2N
450	20	8	210	39	40	ULA2C
500	60	2,5	300	38	40	ULA5RA
500	20	7,5	90	38	40	ULA5RB

Bipolare **Gate-Arrays** ULAs

Gatter-komplexität	Clockfrequenz MHz	Gatter-laufzeit ns	Gatter-verlustl. µW	Peripherie-zellen	Bondpads	Typ
500	10	15	30	38	40	ULA5RC
500	3	60	8	38	40	ULA5RD
512	0,04	2000	0,4	40	40	ULA2M
726	0,25	200	180	48	48	ULA5L
880	6	25	60	48	52	ULA5N
880	20	8	210	48	52	ULA5C
900	60	2,5	300	48	50	ULA9RA
900	20	7,5	90	48	50	ULA9RB
900	10	15	30	48	50	ULA9RC
900	3	60	8	48	50	ULA9RD
1200	60	2,5	300	52	58	ULA12RA
1200	20	7,5	90	52	58	ULA12RB
1200	10	15	30	52	58	ULA12RC
1200	3	60	8	52	58	ULA12RD
1600	60	2,5	300	62	68	ULA16RA
1600	20	7,5	90	62	68	ULA16RB
1600	10	15	30	62	68	ULA16RC
1600	3	60	8	62	68	ULA16RD
1800	60	2,5	300	64	72	ULA18RA
1800	20	7,5	90	64	72	ULA18RB
1800	10	15	30	64	72	ULA18RC
1800	3	60	8	64	72	ULA18RD
1980	20	8	120	64	64	ULA9C
2000	6	25	35	64	64	ULA9N
2000	60	2,5	300	72	80	ULA20RA
2000	20	7,5	90	72	80	ULA20RB
2000	10	15	30	72	80	ULA20RC
2000	3	60	8	72	80	ULA20RD
2400	60	2,5	300	80	88	ULA24RA
2400	20	7,5	90	80	88	ULA24RB
2400	10	15	30	80	88	ULA24RC
2400	3	60	8	80	88	ULA24RD
2400	6	25	35	68	70	ULA12N
2640	20	8	120	68	70	ULA12C
3000	60	2,5	300	82	96	ULA30RA
3000	20	7,5	90	82	96	ULA30RB
3000	10	15	30	82	96	ULA30RC
3000	3	60	8	82	96	ULA30RD
4000	60	2,5	300	118	130	ULA40RA
4000	20	7,5	90	118	130	ULA40RB
4000	10	15	30	118	130	ULA40RC
4000	3	60	8	118	130	ULA40RD

Autoroutable **Gate-Arrays** ULAs

Gatter-komplexität	Clock-frequenz MHz	Gatter-laufzeit ns	Gatter-verlustl. µW	Peripherie-Zellen	Bondpads	Typ
1000	Typ ARA: 130	1,5	150	70	78	ULA10AR*
1300	Typ ARB: 65	3	70	87	95	ULA13AR*
1600	Typ ARC: 20	10	20	92	102	ULA16AR*
1800	Typ ARD: 10	20	10	94	104	ULA18AR*
2400				113	123	ULA24AR*
3000				121	131	ULA30AR*

*** Erhältlich als A-, B-, C- und D-Ausführung.**

CMOS **Gate-Arrays** Monochips

Gatter-komplexität	Clock-frequenz MHz	Matrix-Zellen Gatter-laufzeit ns	Matrix-Zellen Gatter-verlustl. µW/kHz	Peripherie-Zellen N/P Channel Buffers	Peripherie-Zellen N-Channel Treiber	Bondpads	Typ
140	·	·	·	16	14	32	MCA
200	·	·	·	18	18	38	MCB
270	·	·	·	24	18	44	MCC
440	4/10	20/8	0,02/0,2	32	16	52	MCD
340	(bei 5/15V)	(bei 5/15V)	(bei 5/15V)	24	18	44	MCE
630	·	·	·	36	14	60	MCF
800	·	·	·	40	18	68	MCG

Bipolare **Digilin®-Arrays** ULAs

Gatter-komplexität	Clock-frequenz kHz	Gatter-laufzeit ns	Gatter-verlustl. µW	Peripherie-zellen	Transistoren	Widerstände	Bondpads	Typ
30	270	750	1,9	10	120	200	18	ULA03G
98	270	750	1,9	16	192	336	24	ULA1G
162	270	750	1,9	20	240	400	28	ULA2G
286	440	450	3,4	26	104	286	30	ULA1U
288	270	750	1,9	24	288	480	32	ULA3G
338	270	750	1,9	28	336	560	36	ULA4G
450	270	750	1,9	32	384	640	40	ULA5G
512	440	450	3,4	40	240	328	40	ULA2U
578	270	750	1,9	36	432	720	44	ULA6G
598	440	450	3,4	36	144	432	40	ULA3U

Bipolare **Linear-Arrays** Monochips

NPN Transistoren 20mA	NPN Transistoren 100/200mA	PNP Transistoren 200 µA	PNP Transistoren dual 200 µA	Schottky-Dioden	Widerstände 200 Ohm	Widerstände 450 Ohm	Widerstände 900 Ohm	1K8	3K6	(1) 30K	(1) 60K	(1) 100K	V_{CC}(V)	Bond-pads	Typ
57	2	18		15	16	43	43	29	28	4		4	20	16	MOA
69		12		16	27	44	45	39	36	6		6	20	24	MOB
22		8		6	8	18	20	13	12	2			20	14	MOC
50			16		15	30	28	29	24		2		36	16	MOD
48			15		8	32	28	25	26	5			20	18	MOE
96	4		36		18	88	68	61	61	9			20	24	MOF
58	2		18		19	68	65	44	27		8		20	18	MOG
70	2		22		29	82	75	54	36		8		20	18	MOH
36	2		12		8	34	30	24	20		4		20	18	MOJ
76	4		22		23	103	77	53	36		10		20	24	MOL
137	8		44		60	188	140	104	84		16		20	28	MOM
170	12		64		68	244	226	161	111		24		20	40	MON
71	4		54		21	140	142	96	64		24		20	24	MOP
55	2		21		18	68	57	40	26		8		20	18	MOQ

(1) Pinch-Widerstände

® Digilin ist ein eingetragenes Warenzeichen der Ferranti plc.

Ihre Einstiegsmöglichkeiten in die anwendungsspezifische IC-Technik bei Ferranti

Anwendungsspezifischer LSI-Entwurf ist bei Ferranti durch ein hohes Maß an Flexibilität gekennzeichnet. Die optimale Schnittstelle zwischen dem Kunden und dem Ferranti-Entwicklungsteam wird individuell vereinbart.

Denn durch das partnerschaftliche Miteinander ist gewährleistet, daß die Projektabwicklung erfolgreich durchgeführt wird. Ferranti bietet Ihnen vier Basis-Varianten für Ihren Einstieg in diese zukunftsweisende Technik.

Produktidee

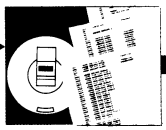
Sie erstellen eine Systembeschreibung und beauftragen Ferranti mit der Entwicklung Ihres ganz speziellen ICs.

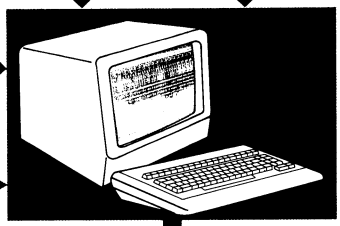
Logikplan

Sie übergeben uns das fertige Schaltschema, das bereits alle analogen und digitalen Funktionen aufweist.

Computergerechte Logikbeschreibung

Sie übergeben uns die von Ihnen simulierte Schaltung in einer computergerechten Beschreibung, mit der wir in unserem CAD-Center unmittelbar weiterarbeiten können.

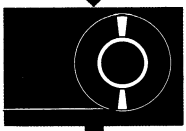


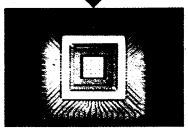


Testprogramm

Maskenband

Sie haben einen Semi-Kunden-IC mit Ferranti-Software auf Ihrem eigenen CAD-System entwickelt, liefern ein fertiges Maskenband und übertragen uns die IC-Produktion.



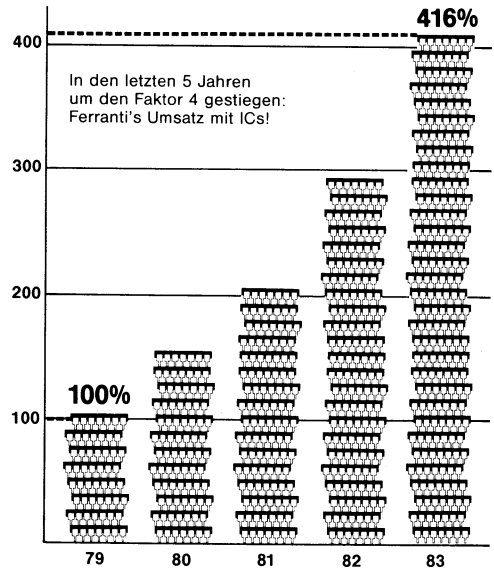


Bei welcher Stufe Sie auch eingestiegen sind – immer erhalten Sie von Ferranti Prototypen, die Sie auf 100%ige Funktionstüchtigkeit untersuchen, bevor wir mit der Serienfertigung Ihres Semi-Kunden-ICs beginnen.

Semi-Kunden-ICs
Eine Pionierleistung von Ferranti

Wenn Ferranti heute die wohl umfangreichste Produktpalette von anwendungsspezifischen Schaltungen anbieten kann, dann kommt das nicht von ungefähr. Die Erfahrung dreier Jahrzehnte Halbleiterfertigung und ein intensives Engagement in die Gate-Array-Technik während der letzten zwölf Jahre stehen ebenso dahinter wie die Tatsache, daß der gesamte Leistungsumfang in puncto Entwicklung und Produktion im eigenen Hause erbracht wird.

Die herausragenden Merkmale der anwendungsspezifischen ICs von Ferranti sprechen für sich:
Gate-Arrays mit Komplexitäten von 100 bis 10 000 Gatter-Funktionen, ECL-Geschwindigkeiten und Verlustleistungen im CMOS-Bereich.
Digilin-Arrays mit der Kombinationsmöglichkeit von analogen und digitalen Funktionen auf demselben Chip zur Erschließung neuer Märkte dort, wo komplexe Subsysteme integriert werden müssen.
Linear-Arrays mit 300 bis 1 000 Bauelementen pro Chip zur Integration kompletter analoger LSI-Systeme.



Da anwendungsspezifische ICs heute in nahezu allen Bereichen eingesetzt werden, sind auch die unterschiedlichsten Anforderungen an die Gehäuse bzw. die Verkapselung dieser ICs gestellt. Ferranti wird diesem Bedarf durch ein breites Gehäuseangebot gerecht: DIL-Gehäuse und Chip-Carriers gibt es in Plastik und Keramik, Flatpacks in Plastik und Pin-Grids in Keramik.

Voraussetzung für die serienmäßige Realisierung zukunftsweisender Halbleiterprodukte auf dem Sektor der Semi-Kunden-ICs sind modernste Designsysteme. Ferranti hat deshalb weltweit CAD-Designzentren installiert, die mit dem Ferranti "Silicon Design System" arbeiten. Es handelt sich dabei um ein leistungsfähiges, in sich selbständiges CAD-System, das dem Ingenieur gestattet, einen vollständigen ULA-Entwurf durchzuführen: ausgehend von der Logikbeschreibung bis hin zu den verifizierten Daten des Steuerbands für den Pattern-Generator.
Die Entwicklung von anwendungsspezifischen ICs mittels CAD ist bei Ferranti seit Jahren Standard, so daß heute dem Anwender eine ausgereifte Hard- und Software zur Verfügung steht.

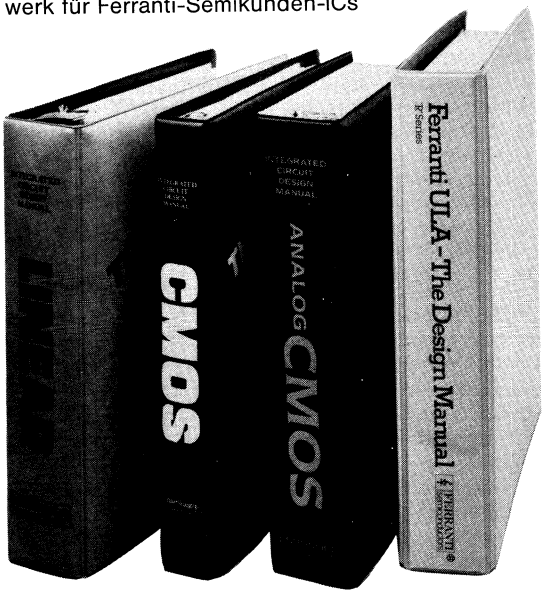
Auf dem Gebiet der anwendungsspezifischen ICs gilt deshalb Ferranti als Pionier und Marktführer gleichermaßen. Daß Ferranti zum Halbleiterhersteller mit der weltweit größten Wachstumsrate wurde, liegt in erster Linie am internationalen Erfolg auf diesem Spezialgebiet der Mikroelektronik.

Semi-Kunden-ICs bedeuten für uns Engagement in den vergangenen Jahren und Verpflichtung für die Zukunft.

Ferranti stellt Ihnen lückenlose Information zur Verfügung:

Design Manuals:

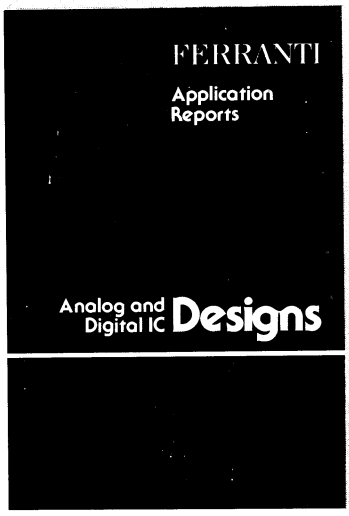
– zur Einarbeitung und als Nachschlagewerk für Ferranti-Semikunden-ICs



ULA Design Manual
(R-Serie, G-Serie)
MOK Design Manual (Linear)
CMOS Design Manual (Digital)
MLA Design Manual
(Linear CMOS)

Applikationsbuch:

– unter mehreren hundert bereits realisierten Schaltungen schöpfen Sie „aus dem Vollen".



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- ☐ Halbleiter Handbuch 85

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