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FUJITSU

DATA SHEET

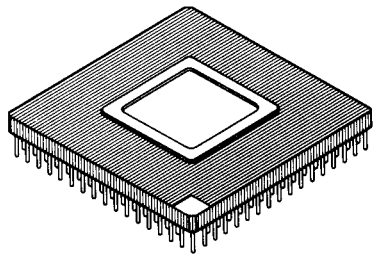
MB86232
32-BIT GENERAL PURPOSE DSP

DIGITAL SIGNAL PROCESSOR

The Fujitsu MB86232 32-bit General Purpose Digital Signal Processor is a flagship of the Fujitsu next generation DSP series.

It supports 32-bit floating point, 32-bit fixed point, and 24-bit integer data format and all those three formats can coexist within a single program with type conversion handled by an instruction.

The MB86232 has a Harvard type architecture with separate program and data memory, thus allowing instructions to be fetched in parallel with the data on two internal data buses. This feature allows more efficient data structures to be developed and therefore higher operational speeds can be achieved for a variety of signal processing applications.



PGA-208C-A02

- **HARVARD ARCHITECTURE:**
  - — Separate Program/Data Memories with two 32-bit Internal Buses
- **HIGH SPEED OPERATION:**
  - — 75ns Cycle Time
- **THREE TYPES OF HIGH PRECISION DATA FORMATS:**
  - — 32-bit Floating Point (24E8 IEEE Format)
  - — 32-bit Fixed Point
  - — 24-bit Integer
- **HIGH PRECISE ARITHMETIC OPERATION:**

— MLT/ACC	Floating	:	24E8	x	24E8 ±	24E8	→ 24E8
	Fixed	:	24	x	24 ±	36	→ 36
	Integer	:	24	x	24 ±	24	→ 24
— DIVIDE	Floating	:	24E8	÷	24E8		→ 24E8
— ADD/SUB	Floating	:	24E8	±	24E8		→ 24E8
	Fixed	:	32	±	36		→ 36
	Integer	:	24	±	24		→ 24

- **PROGRAM MEMORY:**
  - — On-Chip 1024 words/External 65536 words
- **DATA MEMORY:**
  - — On-Chip 512 words Three-port RAM/1M x 32 External Addressing in 64K pages
  - — 16 Words Working Register File
- **POWERFUL INSTRUCTION SET:**
  - — 57 ALU Operations
  - — Concurrent Operation of ALU operation with Triple Data Transfer
  - — Flexible Addressing Functions for Program/Data Memories
- **FLEXIBLE I/O INTERFACE:**
  - — 32/16-bit Programmable Parallel Interface (1-port)
  - — 32/16/8-bit Programmable Serial Interface (2-ports)
  - — On-Chip DMA Capability
- **INTELLIGENT FUNCTIONS:**
  - — 9 Programmable Interrupt Functions with Priority
  - — Halt Function (One-step Execution)
  - — Master/Slave System Operation Modes
- **COMPLETE SET OF PROGRAM DEVELOPMENT SUPPORT TOOLS:**
  - — Assembler/Software Simulator/Hardware Evaluator
- **SILICON-GATE CMOS PROCESS**
- **208-PIN PGA PACKAGE**

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FUNCTIONAL DESCRIPTION

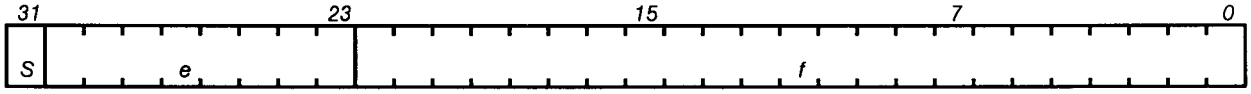
DATA FORMAT

Three types of data formats are available on MB86232. They are:

(1) 32-bit Floating-point (24E8)
(2) 32-bit Fixed-point
(3) 24-bit Integer

These data modes are identified by a mode setting or by instructions. The fixed-point (FIX) and integer (INT) modes are selected by operation mode. However, the floating-point mode is not set this way but is automatically recognized by dedicated floating-point instructions.

32-bit Floating-point (IEEE format)



S: sign bit *e:* exponent *f:* fraction

A floating-point data format consists of 1-sign bit, 8-exponent bits, and 23-fraction bits. A representative value (υ) is expressed as:

$$\upsilon = (-1)^S * 2^{e-127} * (1.f)$$

The most significant bit of the fraction does not appear on the data format as it is always zero.

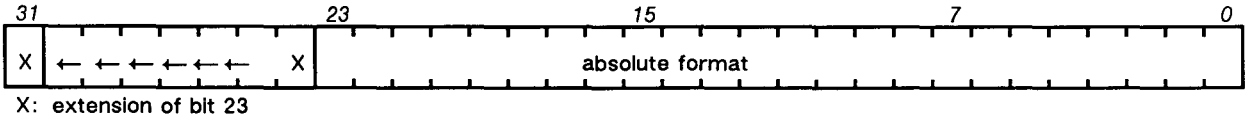
e	*f*	υ
1111 1111	*any*	$2^{128} * (2 - 2^{-23})$
1111 1110	*111 1111 1111 1111 1111 1111*	$2^{127} * (2 - 2^{-23})$ *(max normalized number)*
:	:	:
0111 1111	*any*	$2^{0} * (1.f)$
:	:	:
0000 0001	*000 0000 0000 0000 0000 0000*	$2^{-126} * (1.0)$ *(min normalized number)*
0000 0000	*any*	*0.0*

The range of expressible values:

$$-2.0 * 2^{127} < \upsilon < -1.0 * 2^{-126}$$
$$1.0 * 2^{-126} < \upsilon < 2.0 * 2^{127}$$

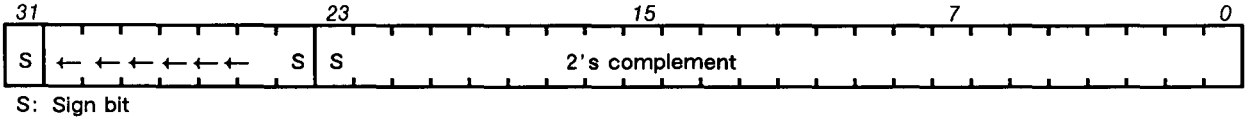
24-bit Integer

I) without sign



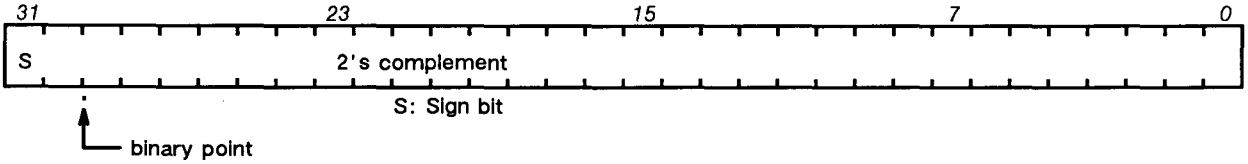
X: extension of bit 23

ii) with sign



S: Sign bit

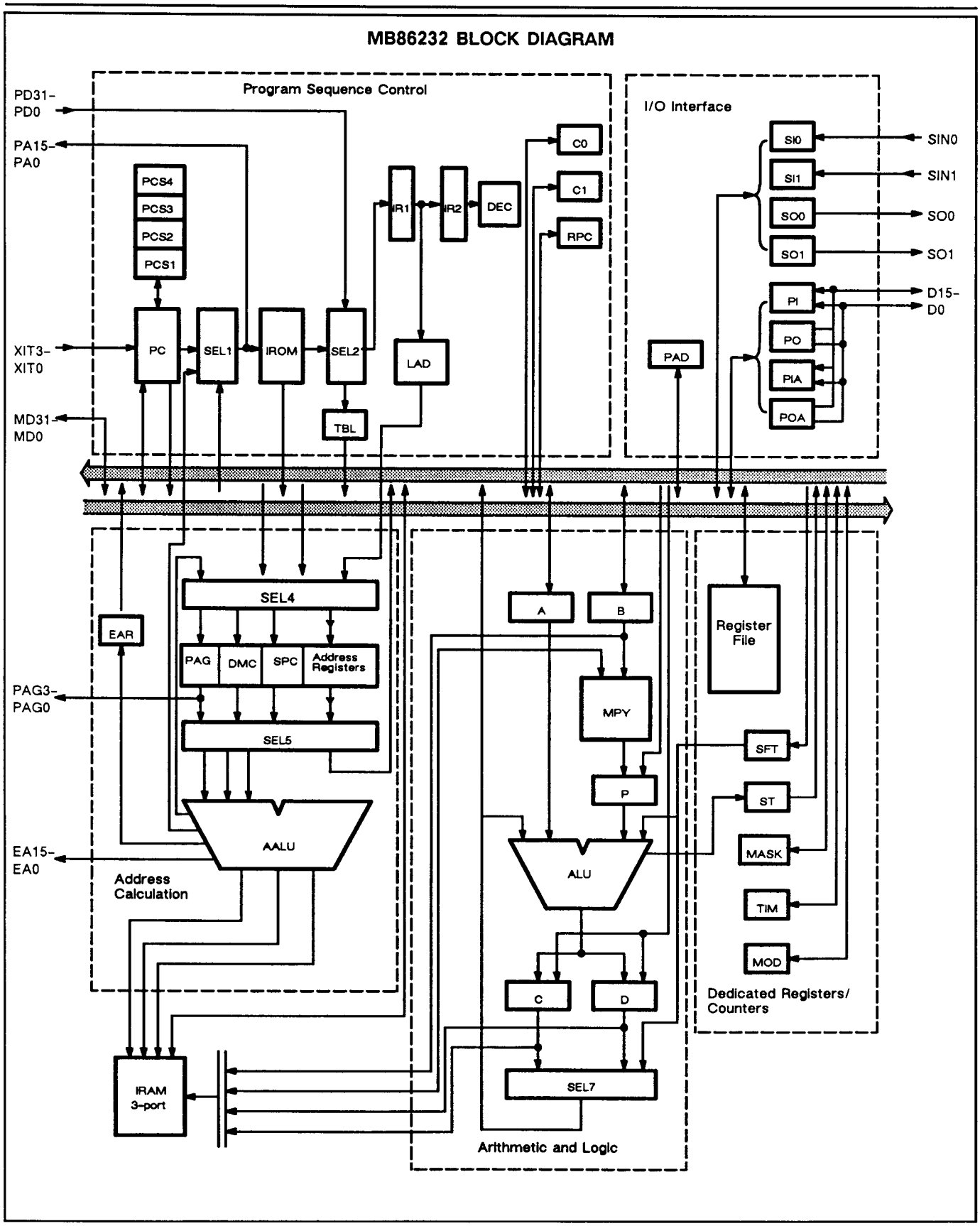
32-bit Fixed Point



In Fixed-point operations, the correct operational result is located in the accumulator where intermediate operational results are in the range, $-32 \leq x < 32$, and the final result is in the range, $-2 \leq x < 2$.

When an intermediate result is out of the range $-32 \leq x < 32$, the final result becomes plus/minus the maximum value.

MB86232 BLOCK DIAGRAM



BLOCK DESCRIPTION

The Functional Block

The MB86232 consists of six functional blocks:

(1) Program Sequence Control Block
(2) Address Calculation Block
(3) Internal 3-port Data RAM Block
(4) Arithmetic and Logic Block
(5) Dedicated Registers/Counter Block
(6) I/O Interface Block

All of these blocks are connected to the internal twin 32-bit wide data buses. Having these two data buses within the device allows concurrent multiple data transfers internally as well as externally.

Program Sequence Control Block

This block controls the instruction execution sequence and is the micro-coded engine of the device. It is responsible for the fetch, decode, and execution of instructions. The Resident Program Counter (PC) can access up to 64K of program memory for instructions.

The PC counter is reset to address 0 by the Reset input, and incremented by one at each leading edge of the internal master clock. The PC output is connected to the address input of the instruction ROM through SEL1 (selector). SEL1 selects the program and table address of the data table. When a branch instruction is executed or an interrupt is accepted, a branch address is loaded into the PC and the current PC value is saved in the PC stack (PCS). There are four PCS registers (PC1~PC4) so that 4 levels of direct subroutine nesting is allowed. The output data from the internal ROM (IROM) or external ROM (EROM) is transferred to the instruction register IR1 at the beginning of each cycle.

Address Calculation Block

This block calculates the effective (execution) address for RAM (IRAM/ERAM) and ROM (table ROM).

Due to the nature of many signal processing routines where accessing of multiple data is required, this address calculation block provides a mechanism to generate up to three independent effective addresses.

This block contains Base registers B0 and B1, Index registers X0 and X1, and a Virtual shift amount register VSM. The VSM is a 3-bit register that allows a maximum 1024 words of virtual shifting.

I0, I1, and I2 are Index registers that specify the amount of indexing increment.

In addition to these registers, this block contains a DMA (Direct Memory Access) counter DMC, and a page register PAG. The PAG is a general purpose register whose contents are output through PAG3-PAG0 pins, and can be used as a page register for ERAM mapping (4-bits: 16 pages).

IRAM Block

The IRAM block consists of 512 words x 32 bits of three-port RAM, two read ports and one write port. Each port has an independent address that allows two read operations and one write operation to be executed concurrently in a single cycle.

In the case where there is a conflict and the read address and the write address are identical, the write operation precedes the read operations.

Arithmetic and Logic Block

All arithmetic and logic operations are executed in this block.

Three data formats, including 32-bit Floating point, 32-bit Fixed point, and 24-bit Integer, are supported.

This block consist of Input registers A and B, Multiplier MPY, Multiplication Register P, Arithmetic and Logic Unit ALU, and Accumulator Registers C and D.

This block also contains a barrel shifter that enables the accumulator value to be shifted (arithmetic/logical) for a maximum of 32-bits.

When a triple data transfer operation is executed, a transfer from A, B, C, or D to RAM is performed through a dedicated data bus.

Dedicated Registers/Counter Block

This block contains several dedicated registers which include the Timer Counter (TIM), the Mode Register (MOD), the Status Register (ST), the Mask Register (MASK), and a Register File. The 16-bit TIM Counter generates an interrupt when it reaches a specific final state. The Status and MASK registers are used to handle incoming interrupts while the MOD register sets the mode of operation for the device. The Register files consist of sixteen 32-bit registers used as a scratch pad or as general purpose registers.

I/O Interface Block

The I/O interface block performs data exchange between the processor and external circuitry.

Each of the two serial ports can be programmed to interface with a variety of data formats (8/16/32) with an operational speed of 50 n Sec/bit. Parallel interfacing is accomplished with a 32-bit port. There are two modes of operation, one containing only data (16/32) and the other containing data and its corresponding address.

The parallel port contains a parallel address output register PAD which is used when parallel data is input in the address-attached mode.

EXTRA FUNCTIONS

Interrupt Function

The MB86232 has 10 types of interrupt functions, each with a set priority. This ensures that while a higher priority interrupt is being executed, a lower priority interrupt is not accepted.

There are 6 types of hardware interrupt modes including hardware reset, and 4 types of software interrupt modes.

INTERRUPT
- HARDWARE INTERRUPT : RST, INT0, INT1 INT2, INT3, IPF
- SOFTWARE INTERRUPT : TIM, ZDV, OVF, UNF

Interrupt conditions and given priorities are as shown below:

Interrupt Type	Jump Address	Condition Causing Interrupt	Priority
RST	0000	XRST pin = 0	1 highest
TIM	0001	TIMER counter TIM is 0	2
ZDV	0002	Division by zero performed in Floating-point arithmetic	3
OVF	0003	Overflow occurs in Floating-point/Fixed-point arithmetic	4
UNF	0004	Underflow occurs in Floating-point arithmetic	5
INT0	0005	Falling pulse input to XIT0 pin	6
INT1	0006	Falling pulse input to XIT1 pin	7
INT2	0007	Falling pulse input to XIT2 pin	8
INT3	0008	Falling pulse input to XIT3 pin	9
IPF	0009	Data ready in SI0, SI1, PI	10 lowest

Halt Function

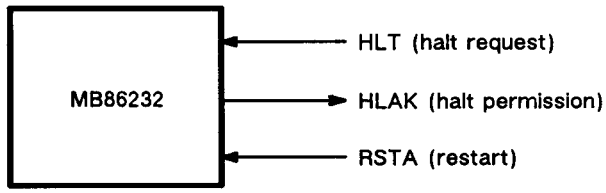
The internal operation is kept holding when a halt request is issued from external pin 'HLT'. When a halt request is issued ('HLT' = 1), the chip returns 'HLAK = 1' to indicate halt request is accepted.

In the halt state, the internal RAM and registers of the DSP can be accessed through MD0 ~ MD31 (data bus) by sending addresses through EA15 ~ EA0.

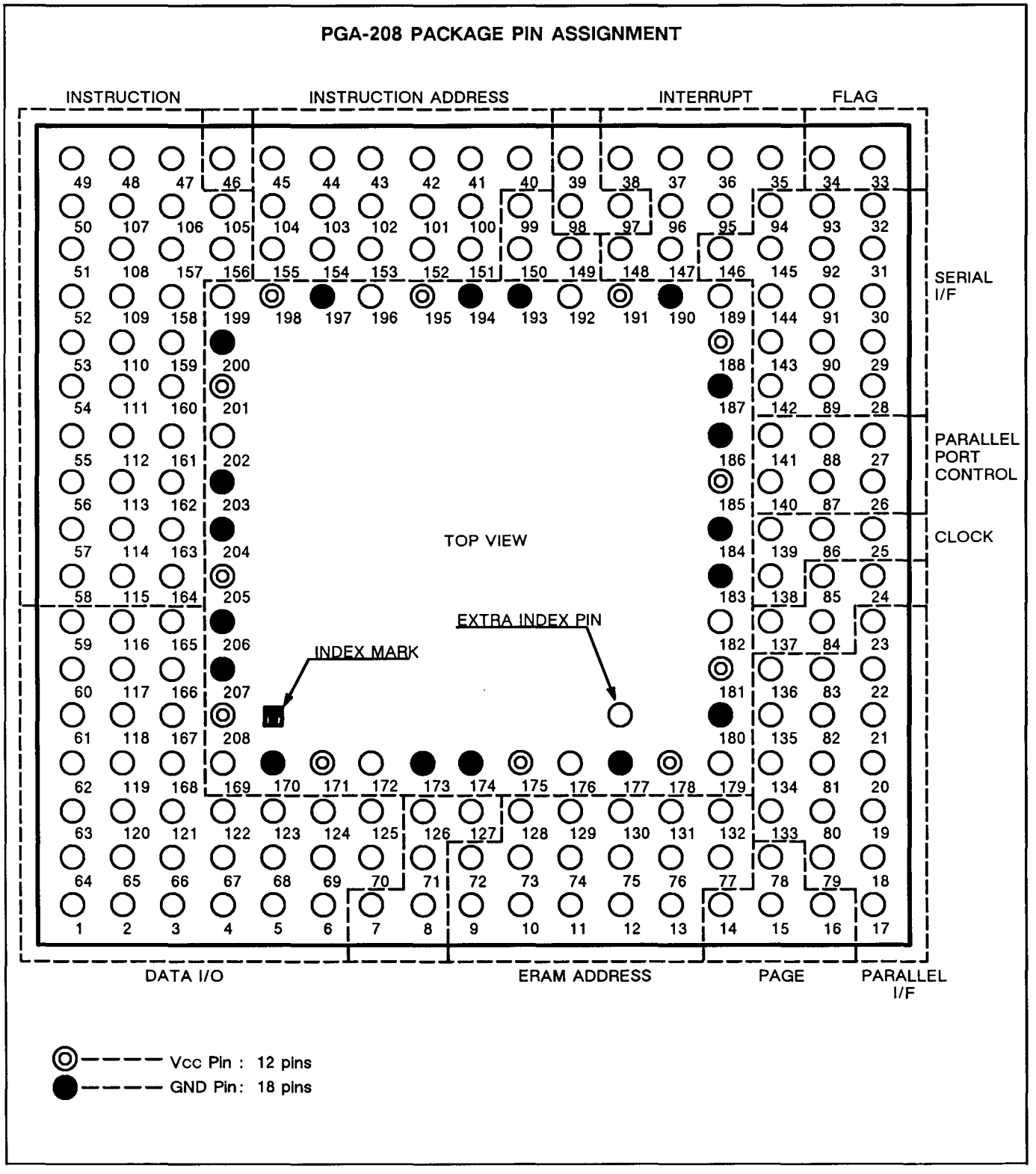
An execution restart can be made by releasing HLT to '0'.

(ONE STEP EXECUTION)

In the halt state (while HLAK = '1'), the DSP executes a one-step instruction by the input of a rising pulse to RSTA. After executing the one-step instruction, the DSP returns to the halt state.



PIN ASSIGNMENT



PIN DESCRIPTION

PIN ASSIGNMENT TABLE

Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name	Pin No.	I/O	Pin Name
1	I/O	MD18	53	I	PD14	105	I	PD0	157	I	PD4
2	I/O	MD19	54	I	PD17	106	I	PD3	158	I	PD13
3	I/O	MD20	55	I	PD20	107	I	PD6	159	I	PD16
4	I/O	MD21	56	I	PD23	108	I	PD7	160	I	PD19
5	I/O	MD24	57	I	PD26	109	I	PD12	161	I	PD22
6	I/O	MD27	58	I	PD29	110	I	PD15	162	I	PD25
7	I	MXS	59	I/O	MD0	111	I	PD18	163	I	PD28
8	I/O	XRDY	60	I/O	MD3	112	I	PD21	164	I	PD31
9	I/O	EA0	61	I/O	MD6	113	I	PD24	165	I/O	MD2
10	I/O	EA2	62	I/O	MD9	114	I	PD27	166	I/O	MD5
11	I/O	EA5	63	I/O	MD12	115	I	PD30	167	I/O	MD8
12	I/O	EA8	64	I/O	MD15	116	I/O	MD1	168	I/O	MD11
13	I/O	EA11	65	I/O	MD16	117	I/O	MD4	169	—	—
14	O	PAG0	66	I/O	MD17	118	I/O	MD7	170	—	GND
15	O	PAG1	67	I/O	MD22	119	I/O	MD10	171	—	Vcc
16	O	PAG3	68	I/O	MD25	120	I/O	MD13	172	—	—
17	I/O	D0	69	I/O	MD28	121	I/O	MD14	173	—	GND
18	I/O	D1	70	I/O	MD30	122	I/O	MD23	174	—	GND
19	I/O	D3	71	I/O	RXW	123	I/O	MD26	175	—	Vcc
20	I/O	D6	72	I/O	EA1	124	I/O	MD29	176	—	—
21	I/O	D9	73	I/O	EA3	125	I/O	MD31	177	—	GND
22	I/O	D12	74	I/O	EA6	126	I/O	XAS	178	—	Vcc
23	I/O	D15	75	I/O	EA9	127	O	BA	179	—	—
24	I	XAIN	76	I/O	EA12	128	I/O	EA4	180	—	GND
25	I	XRST	77	I/O	EA14	129	I/O	EA7	181	—	Vcc
26	I	XPIR	78	O	PAG2	130	I/O	EA10	182	—	—
27	O	XPIA	79	I/O	D2	131	I/O	EA13	183	—	GND
28	I	SYI0	80	I/O	D4	132	I/O	EA15	184	—	GND
29	O	SIB0	81	I/O	D7	133	I/O	D5	185	—	Vcc
30	O	SIB1	82	I/O	D10	134	I/O	D8	186	—	GND
31	I	SIC1	83	I/O	D13	135	I/O	D11	187	—	GND
32	O	SO0	84	I	IES0	136	I/O	D14	188	—	Vcc
33	I	F0	85	O	XA0	137	I	IES1	189	—	—
34	I	F1	86	I	CKIN	138	O	SCK0	190	—	GND
35	I	XIT0	87	O	XPOR	139	I	MCLK	191	—	Vcc
36	O	XAK0	88	I	XPOA	140	I	XPOS	192	—	—
37	I	XIT1	89	I	SIN0	141	O	XPIS	193	—	GND
38	O	XAK1	90	I	SYI1	142	I	SIC0	194	—	GND
39	O	MON1	91	I	SOC0	143	I	SIN1	195	—	Vcc
40	O	PA0	92	I/O	SYO0	144	I/O	SOB0	196	—	—
41	O	PA1	93	I	SOC1	145	I/O	SYO1	197	—	GND
42	O	PA4	94	I/O	SOB1	146	O	SO1	198	—	Vcc
43	O	PA7	95	I	XIT2	147	I	XIT3	199	—	—
44	O	PA10	96	O	XAK2	148	O	XAK3	200	—	GND
45	O	PA13	97	O	MON2	149	I	RSTA	201	—	Vcc
46	I	IRM	98	O	MON3	150	I	HLT	202	—	—
47	I	PD2	99	O	HLAK	151	O	PA3	203	—	GND
48	I	PD5	100	O	PA2	152	O	PA6	204	—	GND
49	I	PD8	101	O	PA5	153	O	PA9	205	—	Vcc
50	I	PD9	102	O	PA8	154	O	PA12	206	—	GND
51	I	PD10	103	O	PA11	155	O	PA15	207	—	GND
52	I	PD11	104	O	PA14	156	I	PD1	208	—	Vcc

PIN DESCRIPTION

PIN ASSIGNMENT TABLE

Pin Name	I/O	Description
MD31-MD0	I/O	Data bus I/O MD31 (MSB) to MD0 (LSB)
PD31-PD0	I	Instruction Data Inputs PD31 (MSB) to PD0 (LSB)
EA15-EA0	I/O	ERAM Address Output IRAM/Register Address Input (Halt)
D15-D0	I/O	Parallel I/O D15 (MSB) to D0 (LSB)
PA15-PA0	O	Program Address Output PA15 (MSB) to PA0 (LSB)
PAG3-PAG0	O	Page Register Output
MON1	O	IR1 (Instruction Register-1) Enable Output
MON2	O	IR2 (Instruction Register-2) Enable Output
MON3	O	RPC (Repeat Counter) Enable Output
XIT3-XIT0	I	Hardware Interrupt Requests
XAK3-XAK0	O	Hardware Interrupt Acknowledge
MXS	I	Master/Slave System Mode Selection
XRDY	I/O	ERAM Access Ready Signal
SCKO	O	System Clock Output
MCLK	I	Master Clock Input
CKIN	I	Synchronize Clock Input for System Clock
XRST	I	System Reset Input
HLT	I	Halt Request Input
HLAK	O	Halt Acknowledge Output
BA	O	ERAM Interface Enable Indication
RSTA	I	Single Step Execution Control (while halt state)
IRM	I	Internal/External ROM Selection
XAS	I/O	ERAM Address Strobe Signal
RXW	I/O	RAM Read/Write Control
F0	I	F0 Flag Set
F1	I	F1 Flag Set
IES0	I	Direction Control for SYO0 and SOB0
IES1	I	Direction Control for SYO1 and SOB1
SIN0	I	Serial Input Port 0
SIN1	I	Serial Input Port 1
SIC0	I	Write Clock for SIN0
SIC1	I	Write Clock for SIN1
SYI0	I	Data Input Synchronize Signal for SIN0
SYI1	I	Data Input Synchronize Signal for SIN1
SIB0	O	Input Busy Identification from SIN0
SIB1	O	Input Busy Identification from SIN1
SOC0	I	Data Read Clock for SIN0
SOC1	I	Data Read Clock for SIN1
SOB0	I/O	Output Busy Identification from SO0
SOB1	I/O	Output Busy Identification from SO1
SYO0	I/O	Data Output Synchronize Signal for SO0
SYO1	I/O	Data Output Synchronize Signal for SO1
SO0	O	Serial Output Port 0
SO1	O	Serial Output Port 1
XPOR	O	Parallel Output Request
XPOA	I	Parallel Output Permission
XPIR	I	Parallel Input Request
XPIA	O	Parallel Input Permission
XAO	O	Address Output Request
XAIN	I	Address Input Request
XPIS	O	Parallel Input Upper/Lower 16-bit Selection
XPOS	I	Parallel Output Upper/Lower 16-bit Selection

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS *1

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage	V_{DD}	-0.3 *2	6.0	V
Input Voltage	V_I	-0.3 *2	V_{DD} + 0.3 *2	V
Output Voltage	V_O	-0.3 *2	V_{DD} + 0.3 *2	V
Operating Temperature	T_{OP}	0	70	°C
Storage Temperature	T_{STG}	-65	150	°C

Notes:

*1. Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*2. This value applies in a steady condition. It may be 0.5V in a transient condition (for 20 to 30ns).

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Operating Temperature	T_{OP}	0		70	°C

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise specified)

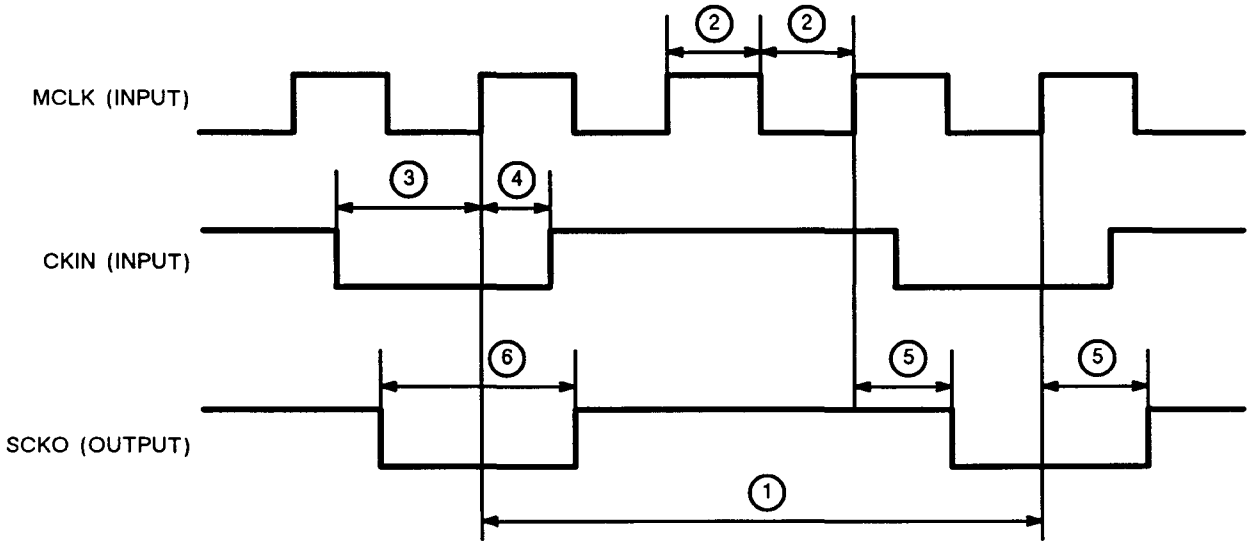
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}	—	2.4	—	V_{DD} + 0.3	V
Low Level Input Voltage	V_{IL}	—	-0.3	—	0.8	V
High Level Output Voltage	V_{OH}	I_{OH} = -2mA	4.2	—	V_{DD}	V
Low Level Output Voltage	V_{OL}	I_{OL} = -3.2mA	Vss	—	0.4	V
Input Leakage Current	I_L	V_I = 0 ~ 5.25V	-10	—	10	µA
Input Leakage Current (High-Z)	I_{LZ}	V_I = 0 ~ 5.25V	-10	—	10	µA
Static Current	I_{CCS}	—	—	—	2	mA
Supply Current	I_{CC}	tCYC = 75ns	—	240	—	µA

INPUT/OUTPUT CAPACITANCE (V_{CC} = V_I = 0V, fM = 8MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin	C_{IN}			16	pF
Output Pin	C_{OUT}			16	pF
I/O Pin	$C_{I/O}$			16	pF

AC CHARACTERISTICS

INTERNAL MASTER CLOCK (MCLK) TIMING

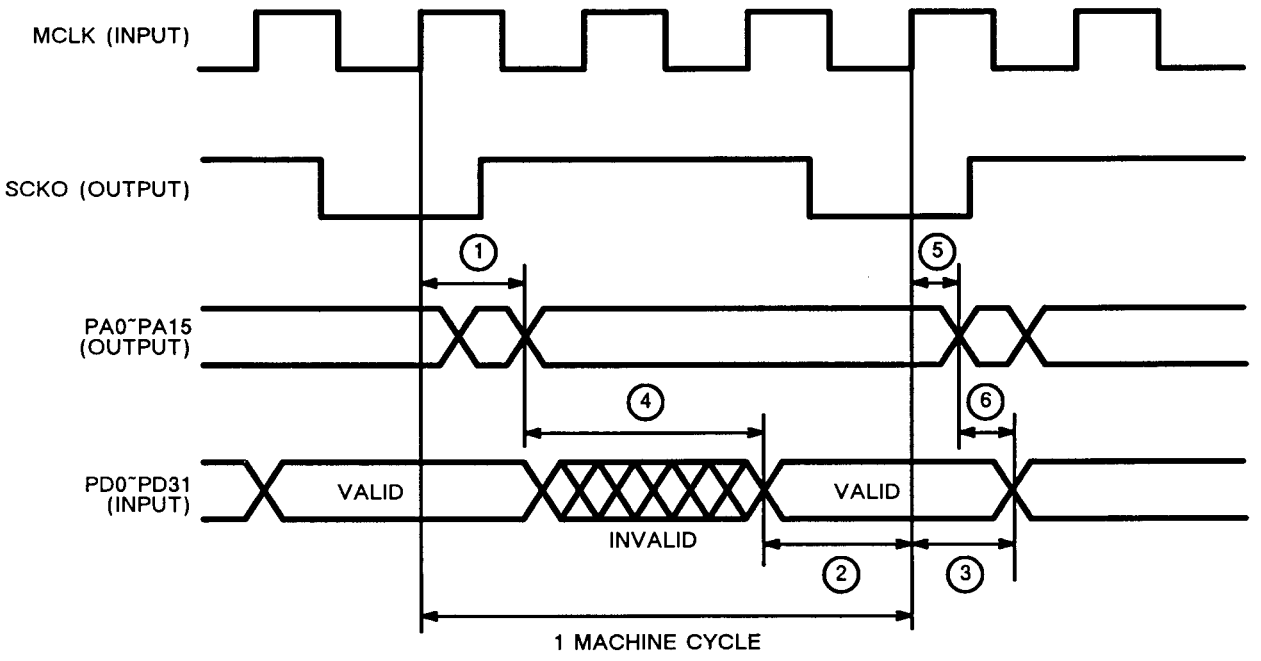


Parameter	Symbol	Min	Typ	Max	Unit	Note
MCLK Frequency	fMCLK			40	MHz	
(1) Machine Cycle	tSC	75			ns	
(2) MCLK Pulse Width	tWMCK	10			ns	
(3) CKIN Setup Time	tSCKI	9			ns	*1
(4) CKIN Hold Time	tHCKI	4			ns	*1
(5) SCKO Output Delay	tPSCK		20	29	ns	
(6) SCKO Pulse Width	tWSCK		25		ns	MCLK = 40MHz

Note:
*1. Applied when CKIN input from external.

AC CHARACTERISTICS (Continued)

EXTERNAL ROM INTERFACE TIMING

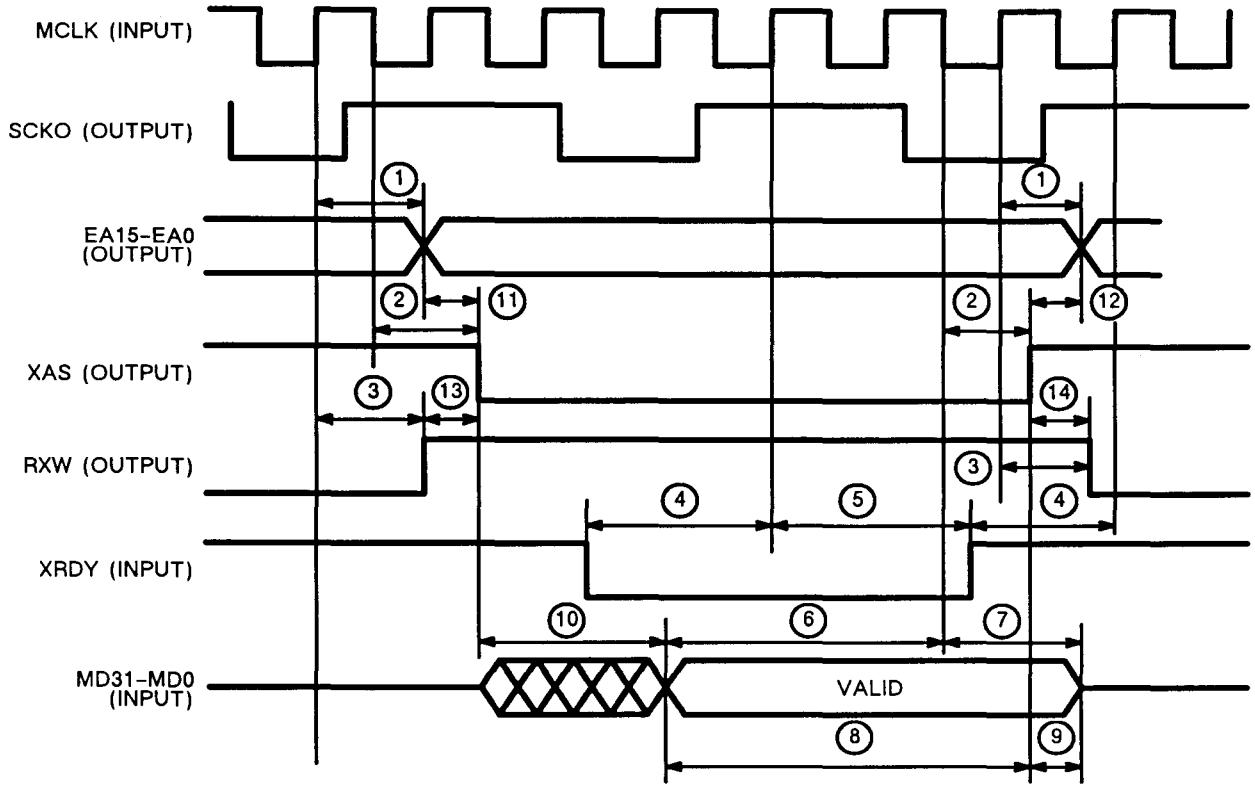


Parameter	Symbol	Min	Typ	Max	Unit	Note
① ROM Address Output Delay	t_{PPA}		30	43	ns	
② ROM Data Setup to MCLK	t_{SPD}		10	14	ns	
③ ROM Data Hold to MCLK	t_{HPD}	4	5		ns	
④ ROM Access Time	t_{ROAC}		40		ns	1*
⑤ ROM Address Hold Time	t_{HPPA}	16	25		ns	
⑥ ROM Data Hold Time	t_{HPDPA}		0		ns	

Note:
*1. $t_{ROAC} - t_{SC} - t_{PPA} - t_{SPD}$ (t_{SC} = 75ns)

AC CHARACTERISTICS (Continued)

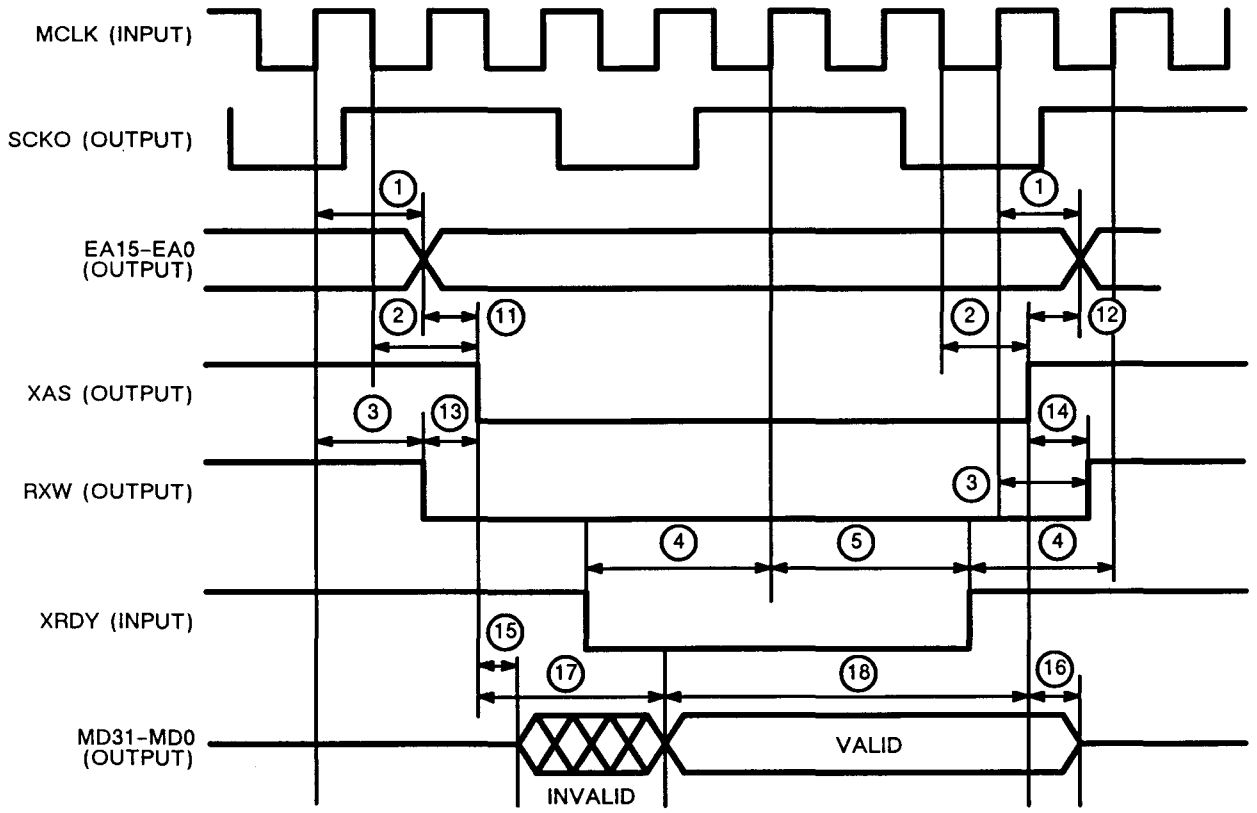
EXTERNAL RAM INTERFACE TIMING (READ CYCLE)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① Address Output Delay	t_{PEA}	14	20	29	ns	
② XAS Output Delay	t_{PAS}	16	22	32	ns	
③ RXW Output Delay	t_{PRXW}	14	20	29	ns	
④ XRDY Input Setup Time	t_{SRDY}	14	10		ns	
⑤ XRDY Input Hold Time	t_{HRDY}	7	10		ns	
⑥ Data Setup Time	t_{SMD}	14	10		ns	
⑦ Data Hold Time	t_{HMD}	11	15		ns	
⑧ Data Setup Time to XAS	t_{SMDAS}	14	10		ns	
⑨ Data Hold Time to XAS	t_{HMDAS}		0		ns	
⑩ Data Access Time	t_{ACAS}		25		ns	
⑪ Address Setup Time to XAS	t_{SEAAS}	7	10		ns	
⑫ Address Hold Time to XAS	t_{HEAAS}	7	10		ns	
⑬ RXW Setup Time to XAS	t_{SRWAS}	7	10		ns	
⑭ RXW Hold Time to XAS	t_{HRWAS}	7	10		ns	

AC CHARACTERISTICS (Continued)

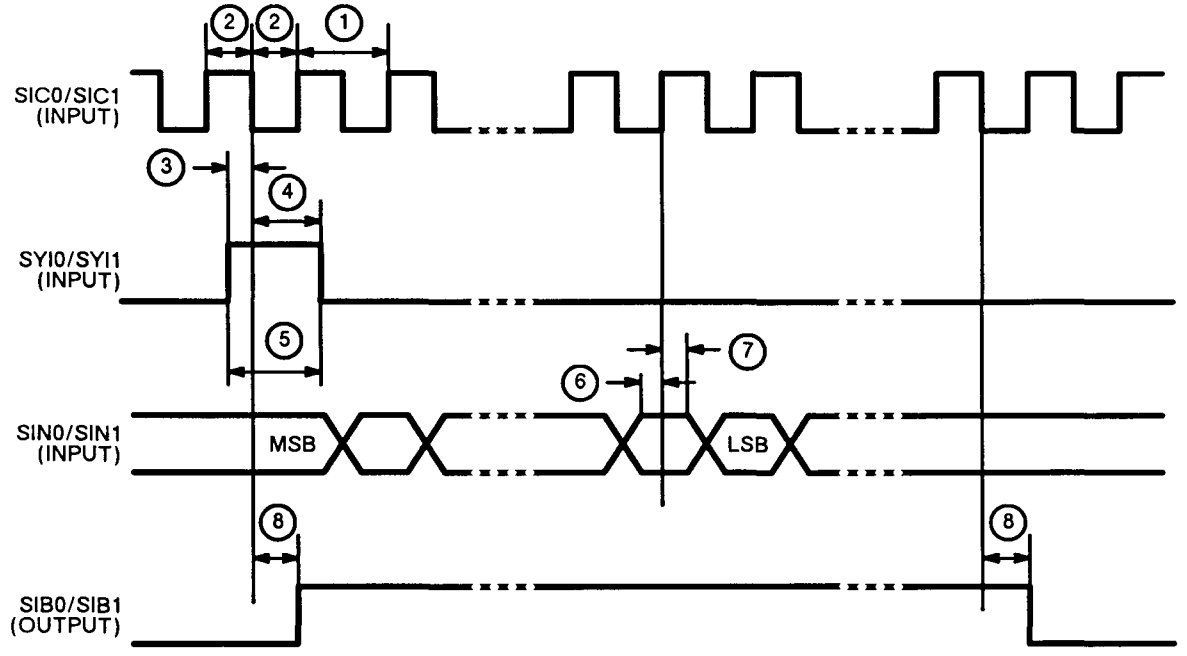
EXTERNAL RAM INTERFACE TIMING (WRITE CYCLE)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① Address Output Delay	t_{PEA}	14	20	29	ns	
② XAS Output Delay	t_{PAS}	16	22	32	ns	
③ RXW Output Delay	t_{PRXW}	14	20	29	ns	
④ XRDY Input Setup Time	t_{SRDY}	14	10		ns	
⑤ XRDY Input Hold Time	t_{HRDY}	7	10		ns	
⑪ Address Setup Time to XAS	t_{SEAAS}	7	10		ns	
⑫ Address Hold Time to XAS	t_{HEAAS}	7	10		ns	
⑬ RXW Setup Time to XAS	t_{SRWAS}	7	10		ns	
⑭ RXW Hold Time to XAS	t_{HRWAS}	7	10		ns	
⑮ Data Output Enable Time	t_{EMD}	11	15		ns	
⑯ Data Output Disable Time	t_{DSMD}	11	15	21	ns	
⑰ Data Output Delay	t_{PMD}		38	54	ns	
⑱ Data Setup Time to XAS	t_{SMDOAS}		5 + n cyc		ns	

AC CHARACTERISTICS (Continued)

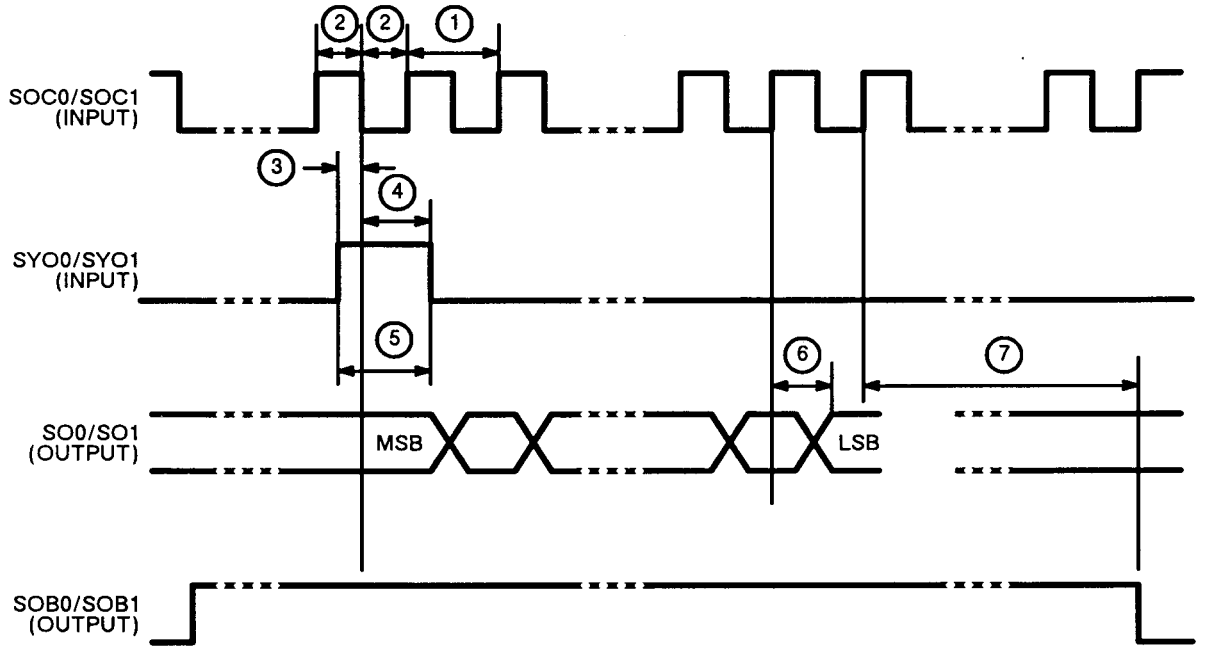
SERIAL INPUT INTERFACE TIMING



Parameter	Symbol	Min	Typ	Max	Unit	Note
① Read Clock Cycle	t_{CSIC}	50			ns	
② Read Clock Pulse Width	t_{WSIC}	20			ns	
③ SYI Setup Time to Clock	t_{SSYI}	3			ns	
④ SYI Hold Time to Clock	t_{HSYI}	10			ns	
⑤ SYI Pulse Width	t_{WSYI}	20			ns	
⑥ Data Setup Time	t_{SSIN}	20			ns	
⑦ Data Hold Time	t_{HSIN}	0			ns	
⑧ BUSY Output Delay	t_{PSIB}		30		ns	

AC CHARACTERISTICS (Continued)

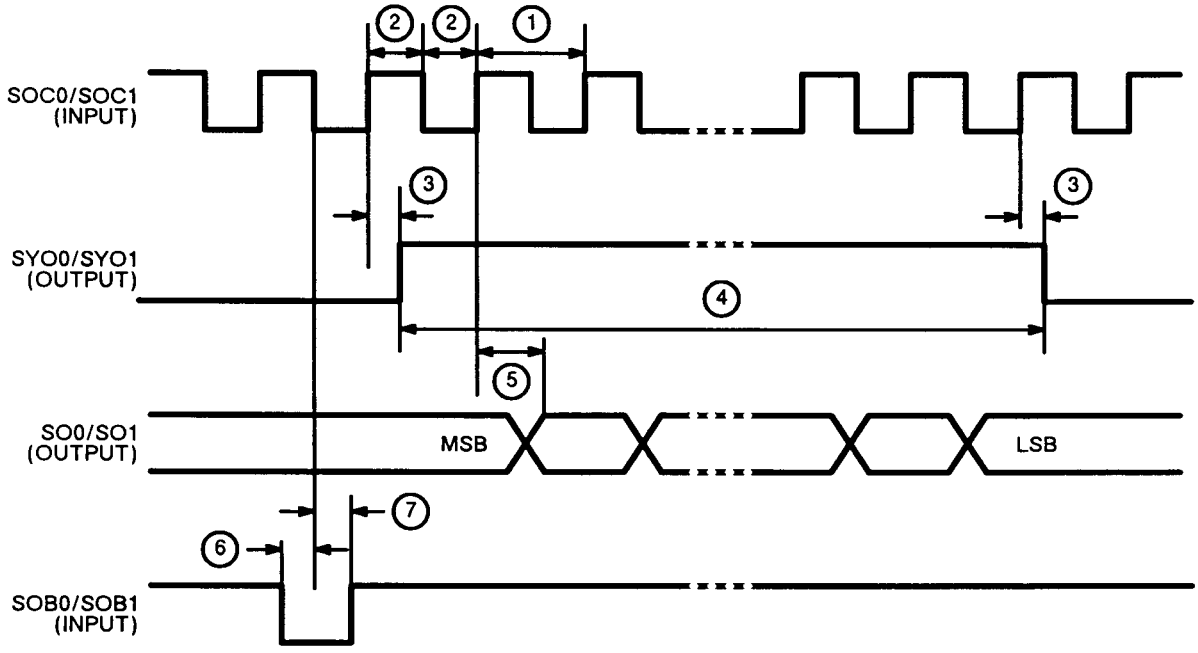
SERIAL OUTPUT INTERFACE TIMING (EXTERNAL SYO0/SYO1 INPUT)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① Read Clock Cycle	t_{CSOC}	50			ns	
② Read Clock Pulse Width	t_{WSOC}	20			ns	
③ SYO Setup Time to Clock	t_{SSYO}	3			ns	
④ SYO Hold Time to Clock	t_{HSYO}	10			ns	
⑤ SYO Pulse Width	t_{WSYO}	20			ns	
⑥ Data Output Delay	t_{SSIN}		23	32	ns	
⑦ BUSY Output Delay	t_{PSIB}		75* n+23	75* n+32	ns	t_{SC} = 75ns

AC CHARACTERISTICS (Continued)

SERIAL OUTPUT INTERFACE TIMING (INTERNAL SYO0/SYO1 OUTPUT)

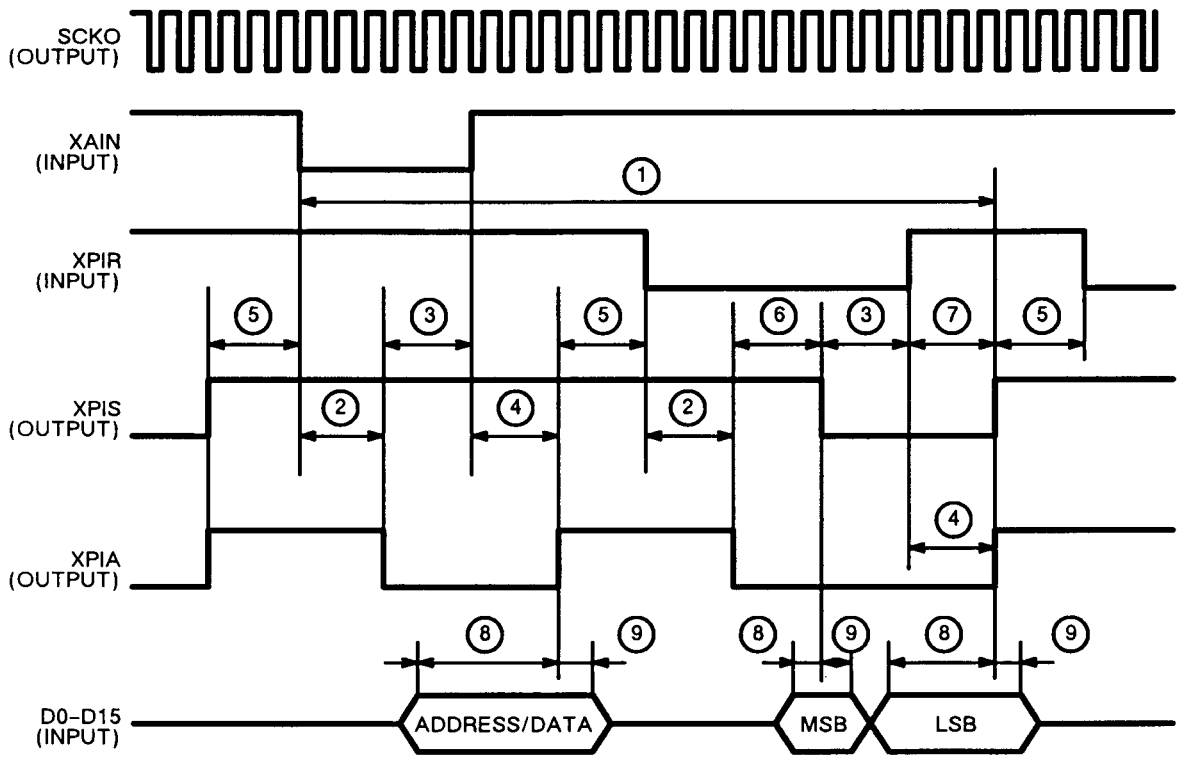


Parameter	Symbol	Min	Typ	Max	Unit	Note
① Read Clock Cycle	t_{CSOC}	50			ns	
② Read Clock Pulse Width	t_{WSOC}	20			ns	
③ SYO Output Delay	t_{PSYO}		15	22	ns	
④ SYO Pulse Width	t_{WSYO}		n* t_{CSOC}		ns	*1
⑤ Data Output Delay	t_{PSO}		23	32	ns	
⑥ BUSY Setup Time	t_{SSOB}	7	5		ns	
⑦ BUSY Hold Time	t_{HSOB}	10			ns	

Note:
*1. n = 8/16/32 (bit length of serial output data).

AC CHARACTERISTICS (Continued)

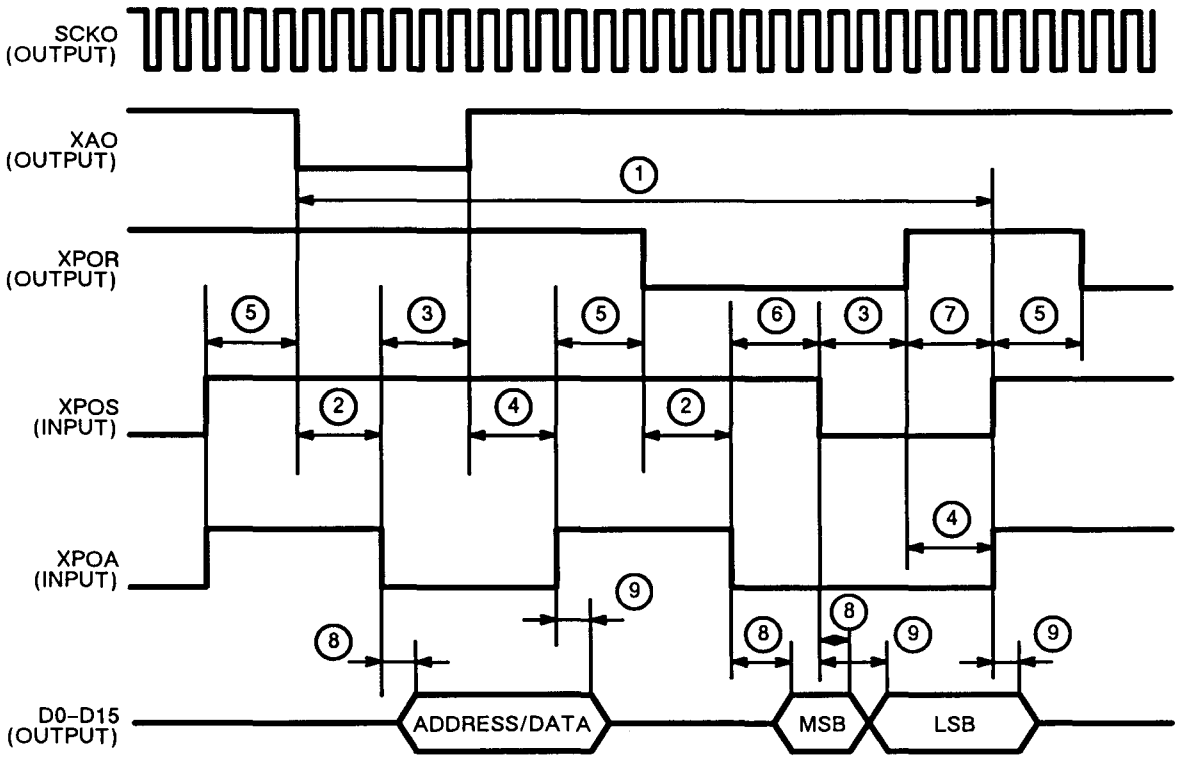
PARALLEL INPUT INTERFACE TIMING (ADDRESS-ATTACHED 32-BIT)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① Parallel Input Cycle	t_{CPI}		24		Machine Cycle	
② Input Permission ON Time	t_{ONPIA}	4/3	2		Machine Cycle	
③ Input Request OFF Time	t_{OFFPIR}	0			ns	
④ Input Permission OFF Time	t_{OFFPIA}	4/3	3		Machine Cycle	
⑤ Input Request Hold Time	t_{HPIR}	0			ns	
⑥ XPIS ON Time	t_{ONPIS}	3			Machine Cycle	
⑦ XPIS OFF Time	t_{OFFPIS}	1	3		Machine Cycle	
⑧ Data Setup Time	t_{SD}	5			ns	
⑨ Data Hold Time	t_{HD}	10			ns	

AC CHARACTERISTICS (Continued)

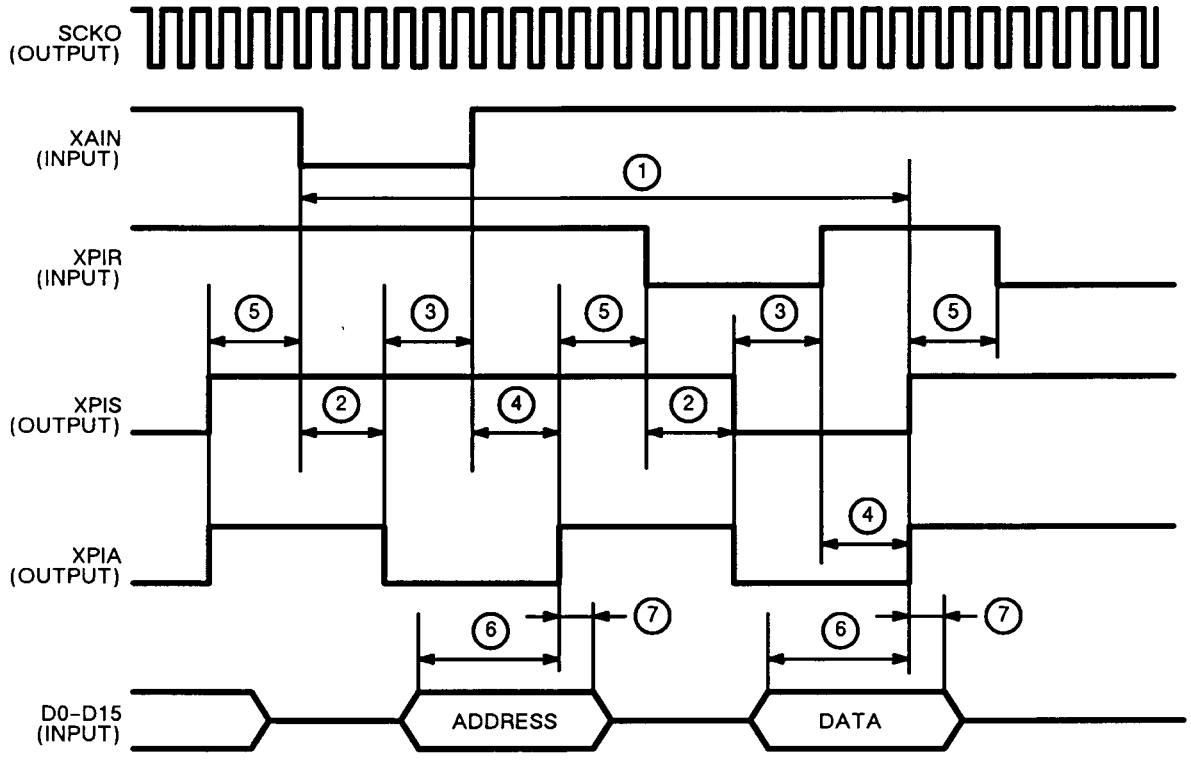
PARALLEL OUTPUT INTERFACE TIMING (ADDRESS-ATTACHED 32-BIT)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① Parallel Output Cycle	t_{CPO}		24		Machine Cycle	
② Output Permission ON Time	t_{ONPOA}	0			ns	
③ Output Request OFF Time	t_{OFFPOR}	4/3	2		Machine Cycle	
④ Output Permission OFF Time	t_{OFFPOA}	0			ns	
⑤ Output Request Hold Time	t_{HPOR}	4/3	2		Machine Cycle	
⑥ XPOS ON Time	t_{ONPOS}	1			Machine Cycle	
⑦ XPOS OFF Time	t_{OFFPOS}	0			ns	
⑧ Data Delay Time	t_{PD}			30	ns	
⑨ Data Hold Time	t_{HD}			50	ns	

AC CHARACTERISTICS (Continued)

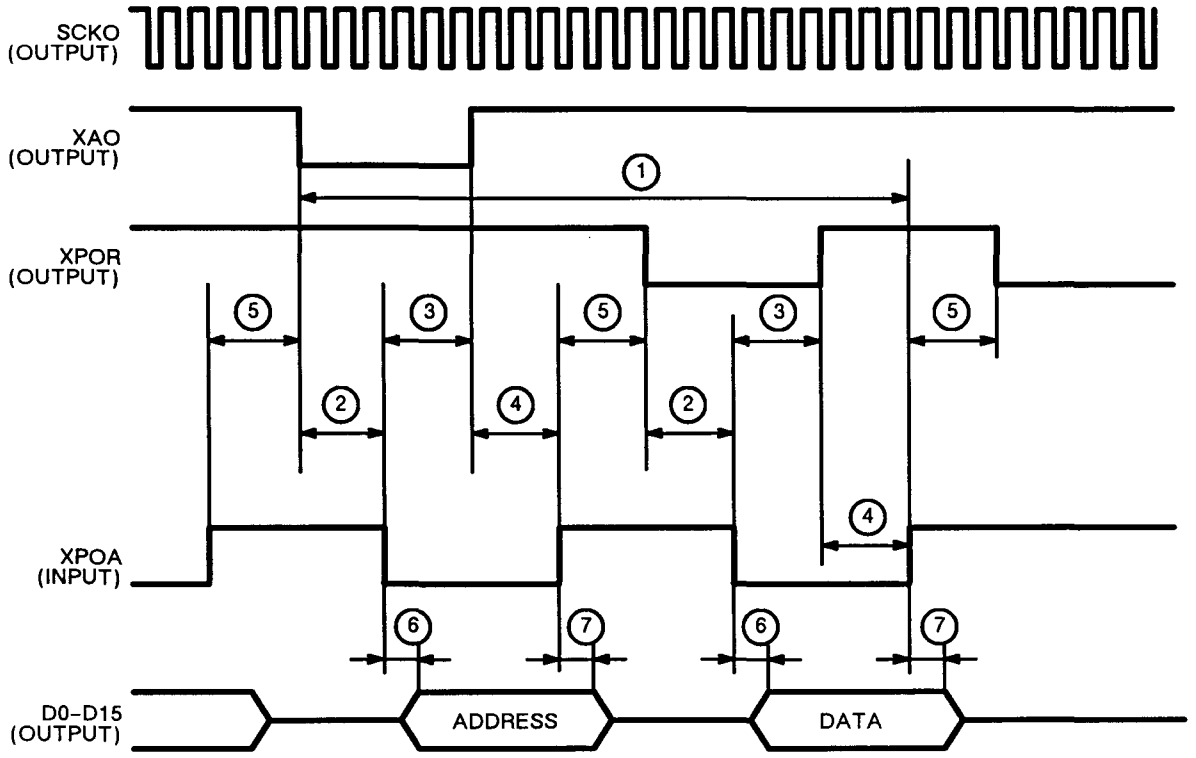
PARALLEL INPUT INTERFACE TIMING (ADDRESS-ATTACHED 16-BIT)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① Parallel Input Cycle	t_{CPI}		24		Machine Cycle	
② Input Permission ON Time	t_{ONPIA}	4/3	2		Machine Cycle	
③ Input Request OFF Time	t_{OFFPIR}	0			ns	
④ Input Permission OFF Time	t_{OFFPIA}	4/3	2		Machine Cycle	
⑤ Input Request Hold Time	t_{HPIR}	0			ns	
⑥ Data Setup Time	t_{SD}	5			ns	
⑦ Data Hold Time	t_{HD}	10			ns	

AC CHARACTERISTICS (Continued)

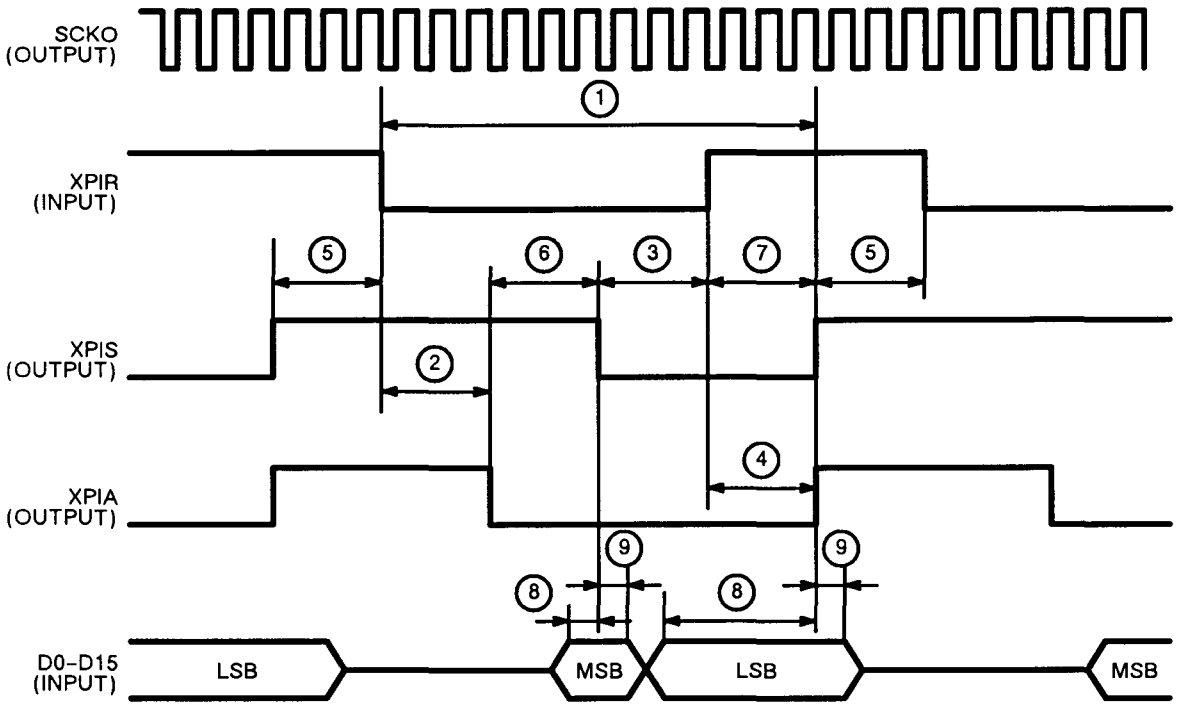
PARALLEL OUTPUT INTERFACE TIMING (ADDRESS-ATTACHED 16-BIT)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① Parallel Output Cycle	t_{CPO}		24		Machine Cycle	
② Output Permission ON Time	t_{ONPOA}	0			ns	
③ Output Request OFF Time	t_{OFFPOR}	4/3	2		Machine Cycle	
④ Output Permission OFF Time	t_{OFFPOA}	0			ns	
⑤ Output Request Hold Time	t_{HPR}	4/3	2		Machine Cycle	
⑥ Data Delay Time	t_{PD}			30	ns	
⑦ Data Hold Time	t_{HD}			50	ns	

AC CHARACTERISTICS (Continued)

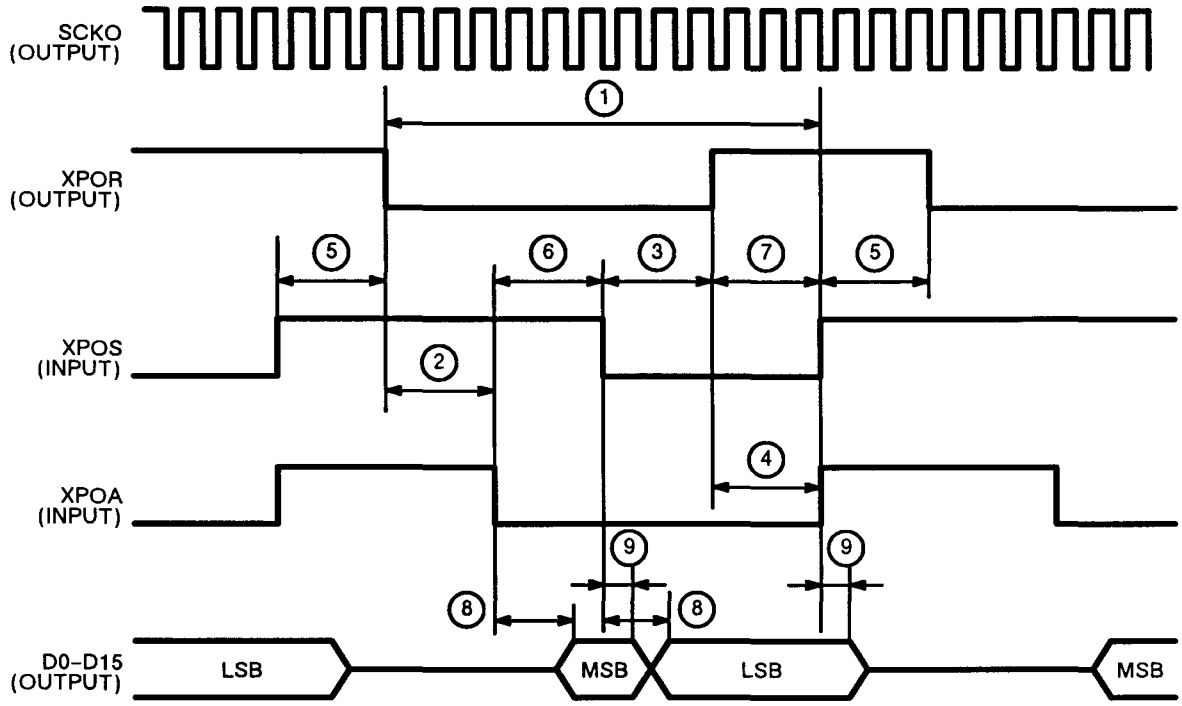
PARALLEL INPUT INTERFACE TIMING (NON ADDRESS-ATTACHED 32-BIT)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① Parallel Input Cycle	t_{CPI}	6			Machine Cycle	
② Input Permission ON Time	t_{ONPIA}	4/3	2		Machine Cycle	
③ Input Request OFF Time	t_{OFFPIR}	0			ns	
④ Input Permission OFF Time	t_{OFFPIA}	4/3	2		Machine Cycle	
⑤ Input Request Hold Time	t_{HPIR}	0			ns	
⑥ XPIS ON Time	t_{ONPIS}	3			Machine Cycle	
⑦ XPIS OFF Time	t_{OFFPIS}	4/3	2		Machine Cycle	
⑧ Data Setup Time	t_{SD}	5			ns	
⑨ Data Hold Time	t_{HD}	10			ns	

AC CHARACTERISTICS (Continued)

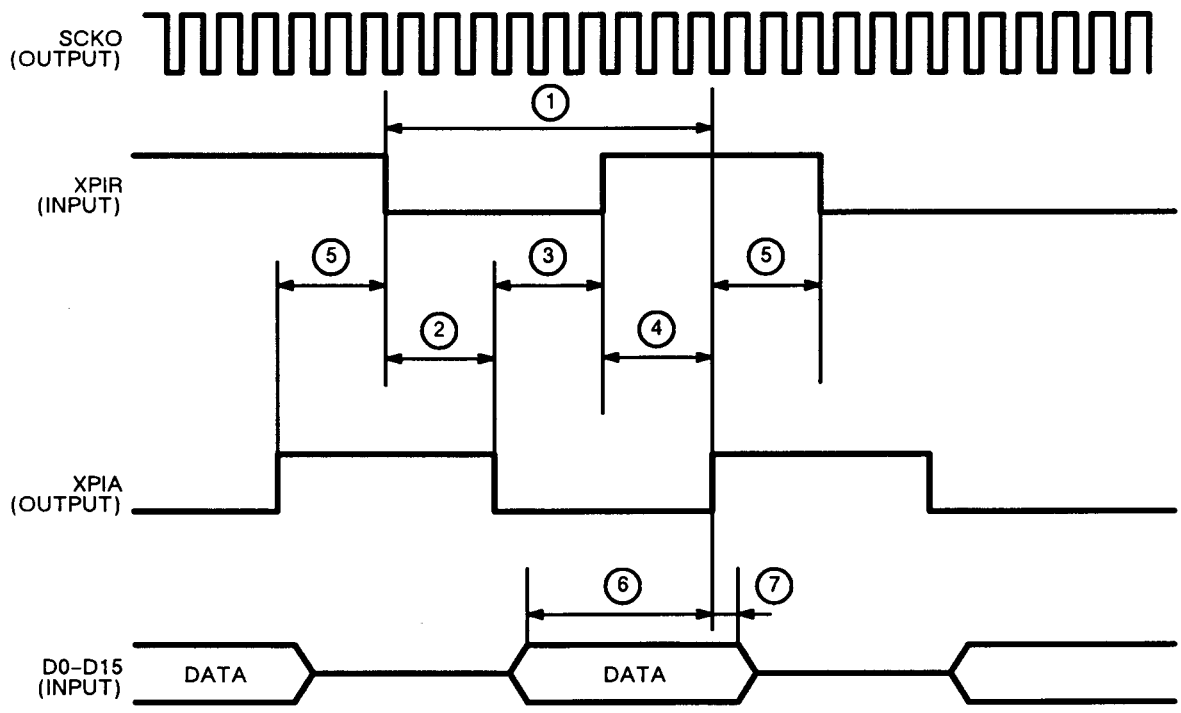
PARALLEL OUTPUT INTERFACE TIMING (NON ADDRESS-ATTACHED 32-BIT)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① Parallel Output Cycle	t_{CPO}	4			Machine Cycle	
② Output Permission ON Time	t_{ONPOA}	0			ns	
③ Output Request OFF Time	t_{OFFPOR}	4/3	2		Machine Cycle	
④ Output Permission OFF Time	t_{OFFPOA}	0			ns	
⑤ Output Request Hold Time	t_{HPOR}	4/3	2		Machine Cycle	
⑥ XPOS ON Time	t_{ONPOS}	1	3		Machine Cycle	
⑦ XPOS OFF Time	t_{OFFPOS}	0			ns	
⑧ Data Delay Time	t_{PD}			30	ns	
⑨ Data Hold Time	t_{HD}			50	ns	

AC CHARACTERISTICS (Continued)

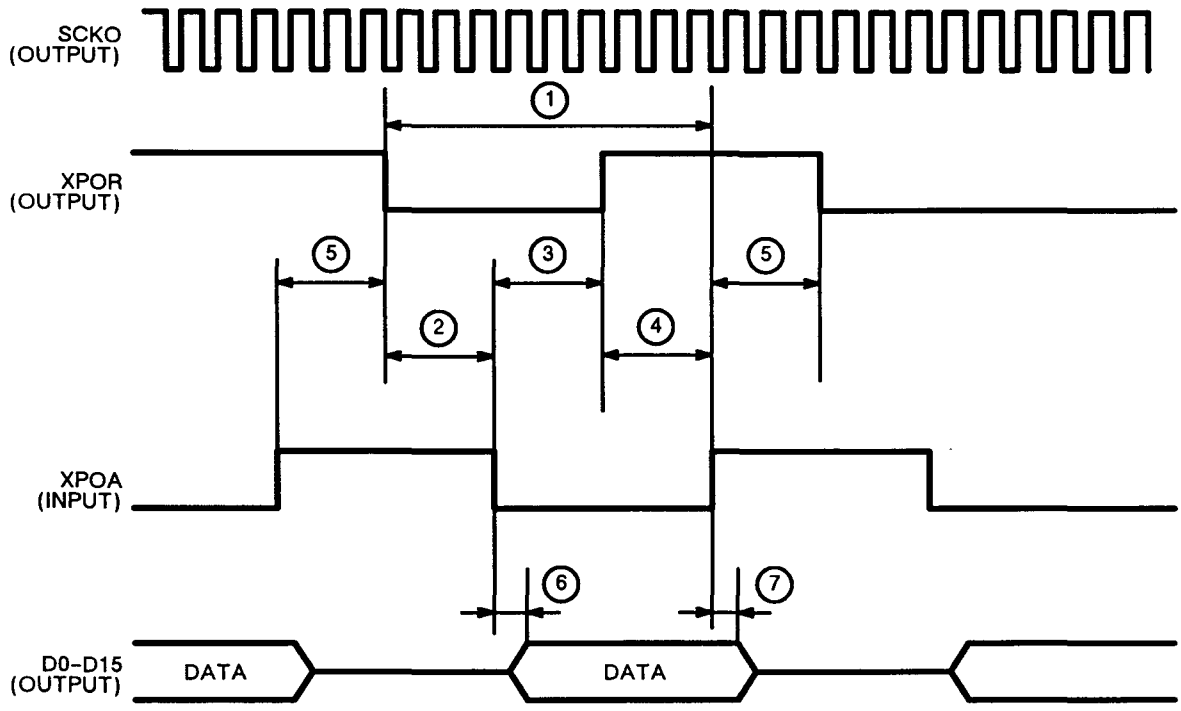
PARALLEL INPUT INTERFACE TIMING (NON ADDRESS-ATTACHED 16-BIT)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① Parallel Input Cycle	t_{CPI}	5			Machine Cycle	
② Input Permission ON Time	t_{ONPIA}	4/3	2		Machine Cycle	
③ Input Request OFF Time	t_{OFFPIR}	0			ns	
④ Input Permission OFF Time	t_{OFFPIA}	4/3	2		Machine Cycle	
⑤ Input Request Hold Time	t_{HPIR}	0			ns	
⑥ Data Setup Time	t_{SD}	5			ns	
⑦ Data Hold Time	t_{HD}	10			ns	

AC CHARACTERISTICS (Continued)

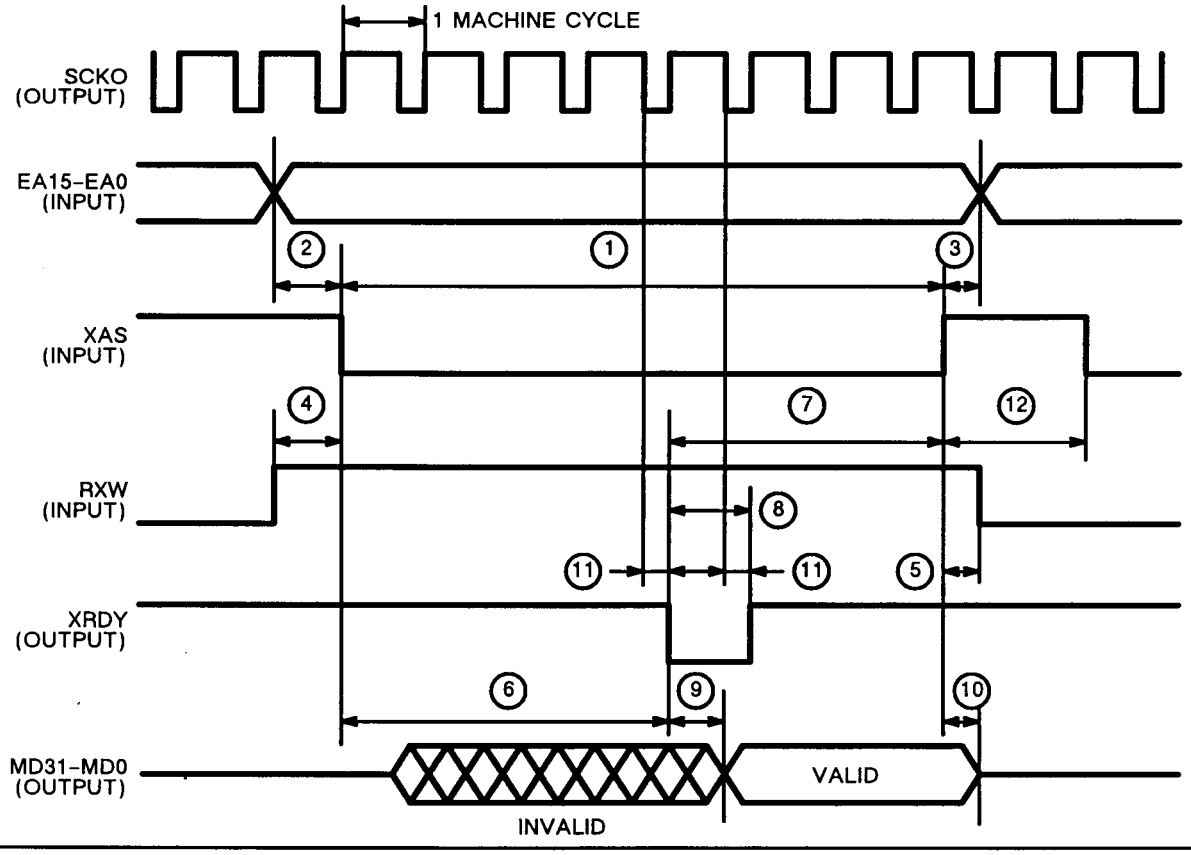
PARALLEL OUTPUT INTERFACE TIMING (NON ADDRESS-ATTACHED 16-BIT)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① Parallel Output Cycle	t_{CPO}	4			Machine Cycle	
② Output Permission ON Time	t_{ONPOA}	4/3	3		Machine Cycle	
③ Output Request OFF Time	t_{OFFPOR}	0			ns	
④ Output Permission OFF Time	t_{OFFPOA}	0			ns	
⑤ Output Request Hold Time	t_{HPOR}	4/3			Machine Cycle	
⑥ Data Delay Time	t_{PD}			30	ns	
⑦ Data Hold Time	t_{HD}			50	ns	

AC CHARACTERISTICS (Continued)

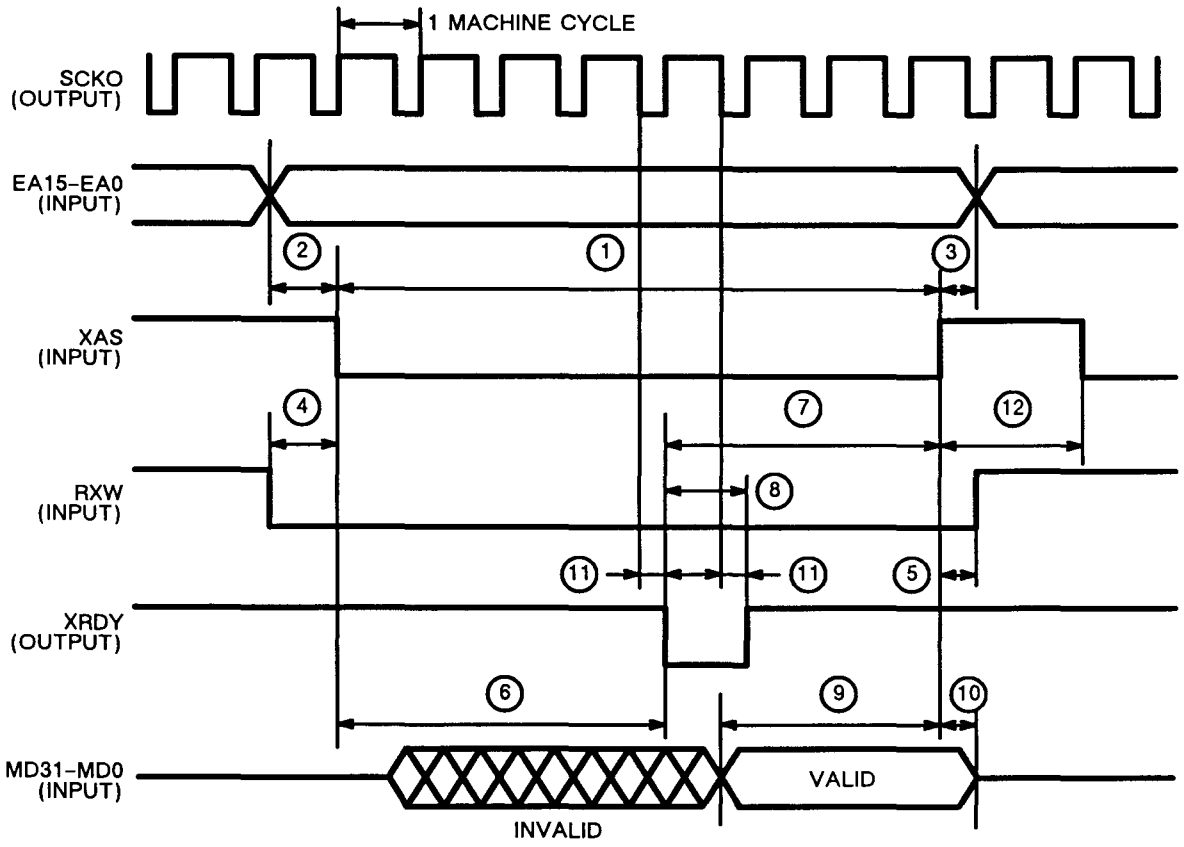
MICROPROCESSOR INTERFACE TIMING (SLAVE MODE, READ CYCLE)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① READ Cycle Time	t_{RDCYC}	3	5		Machine Cycle	
② Address Setup Time	t_{SEA}	0			ns	
③ Address Hold Time	t_{HEA}	0			ns	
④ RXW Setup Time	t_{SRXW}	0			ns	
⑤ RXW Hold Time	t_{HRXW}	0			ns	
⑥ XRDY ON Time	t_{ONRDY}	0	4		Machine Cycle	
⑦ XAS Hold Time	t_{HAS}	0			ns	
⑧ XRDY Pulse Width	t_{WRDY}		1		Machine Cycle	
⑨ Read Data Output Delay	t_{PMD}		TBD		ns	
⑩ Read Data Hold Time	t_{HMD}	29	40		ns	
⑪ XRDY Output Delay	t_{PRDY}		30		ns	
⑫ XAS "High" Pulse Width	t_{WHAS}	20			ns	

AC CHARACTERISTICS (Continued)

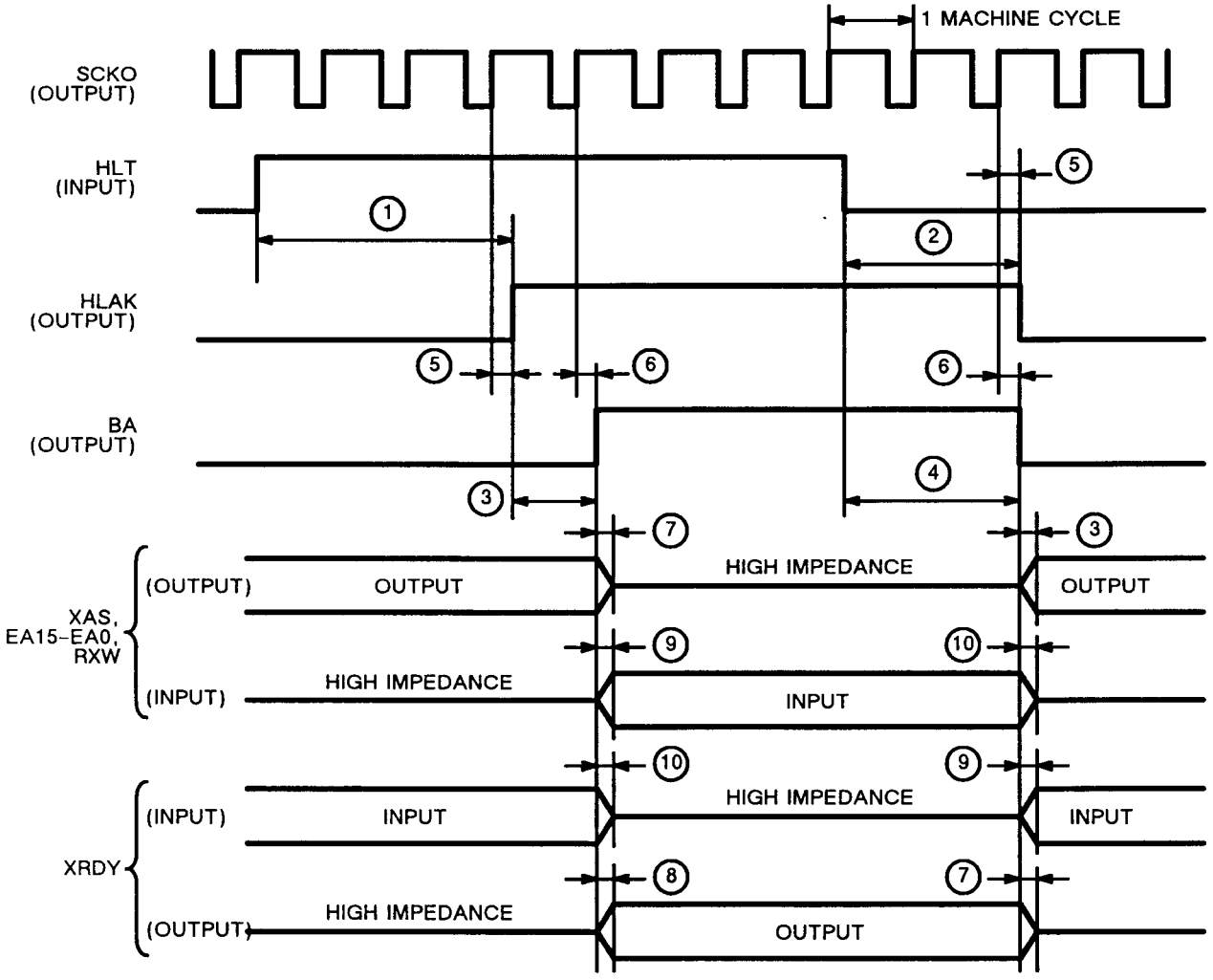
MICROPROCESSOR INTERFACE TIMING (SLAVE MODE, WRITE CYCLE)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① WRITE Cycle Time	t_{RDCYC}	3	5		Machine Cycle	
② Address Setup Time	t_{SEA}	0			ns	
③ Address Hold Time	t_{HEA}	0			ns	
④ RXW Setup Time	t_{SRXW}	0			ns	
⑤ RXW Hold Time	t_{HRXW}	0			ns	
⑥ XRDY ON Time	t_{ONRDY}	3	4		Machine Cycle	
⑦ XAS Hold Time	t_{HAS}	0			ns	
⑧ XRDY Pulse Width	t_{WRDY}		1		Machine Cycle	
⑨ Write Data Setup Time	t_{PMD}		TBD		ns	
⑩ Write Data Hold Time	t_{HMD}		TBD		ns	
⑪ XRDY Output Delay	t_{PRDY}		30		ns	
⑫ XAS "High" Pulse Width	t_{WHAS}	20			ns	

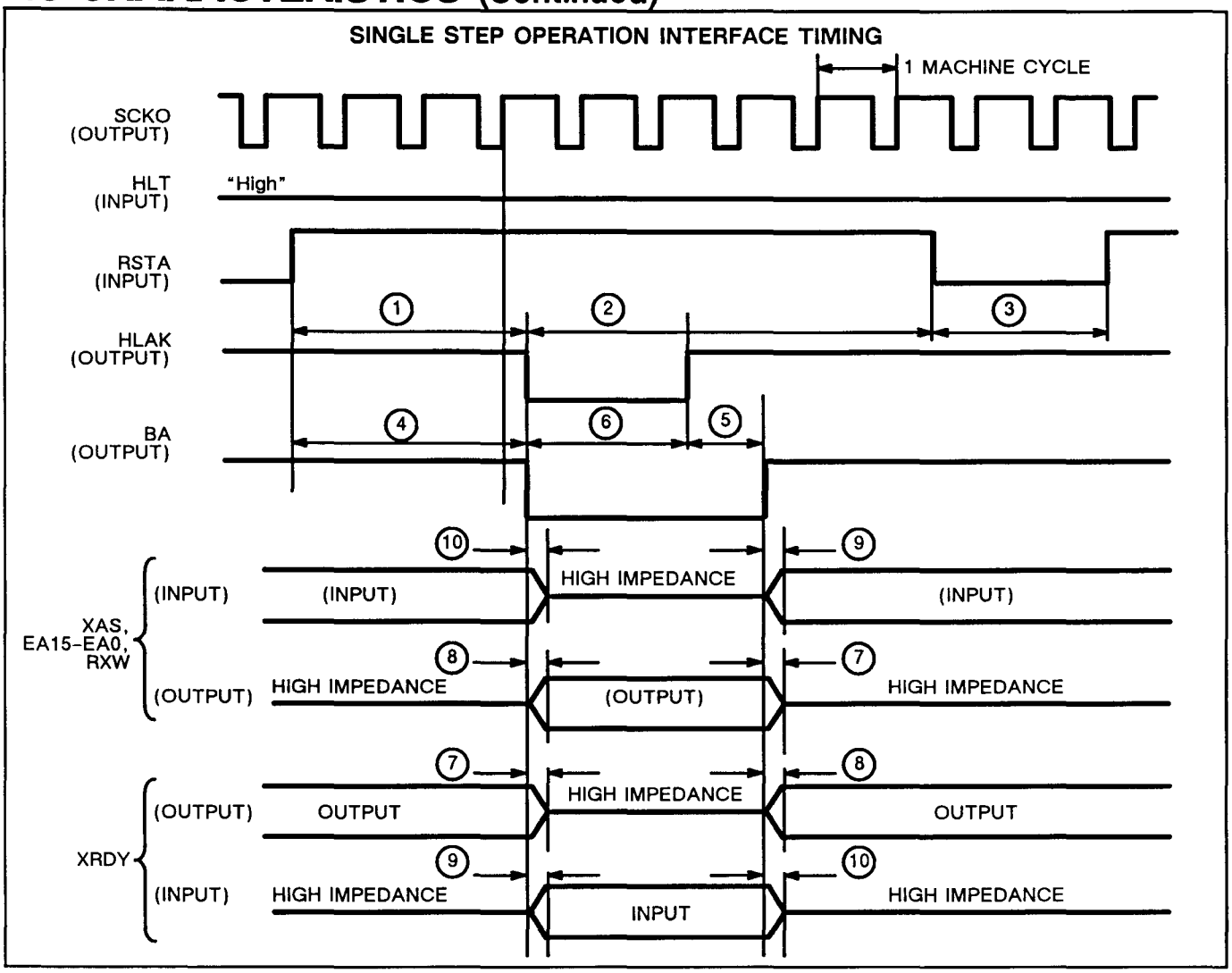
AC CHARACTERISTICS (Continued)

HALT OPERATION INTERFACE TIMING



Parameter	Symbol	Min	Typ	Max	Unit	Note
① HLAK ON Time	t_{ONMAX}	5/3	3		Machine Cycle	
② HLAK OFF Time	t_{OFMAX}	2/3	2		Machine Cycle	
③ BA ON Time	t_{ONBA}		1		Machine Cycle	
④ BA OFF Time	t_{OFBA}	2/3	2		Machine Cycle	
⑤ HLAK Delay Time	t_{PHAK}		35		ns	
⑥ BA Delay Time	t_{PBA}		40		ns	
⑦ Output Disable Time	t_{DOUT}			0	ns	
⑧ Output Enable Time	t_{EOUT}		TBD		Machine Cycle	
⑨ Input ON Time	t_{SIN}	1			Machine Cycle	
⑩ Input Hold Time	t_{HIN}	0			ns	

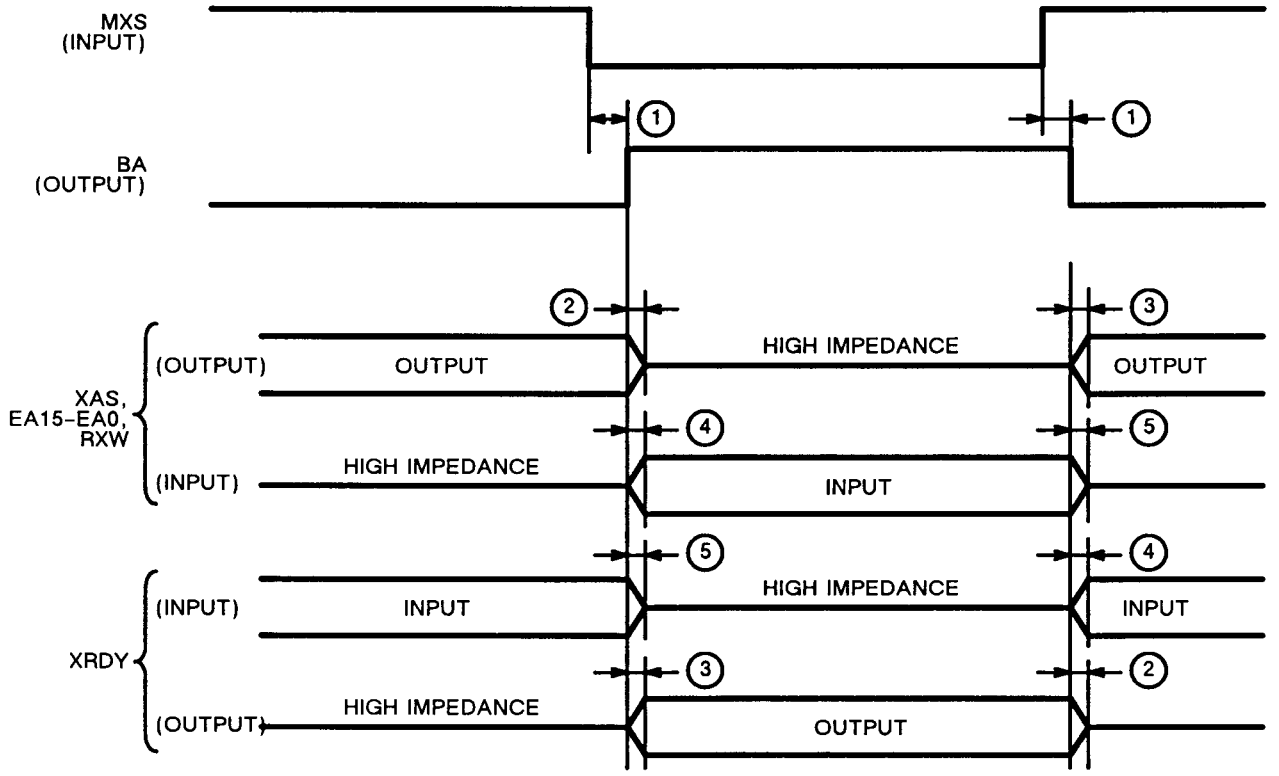
AC CHARACTERISTICS (Continued)



Parameter	Symbol	Min	Typ	Max	Unit	Note
① HLAK OFF Delay Time	t_{DOFHAK}	5/3	3		Machine Cycle	
② RSTA ON Time	t_{ONRST}	2/3	2		Machine Cycle	
③ RSTA OFF Time	t_{OFRST}		1		Machine Cycle	
④ BA OFF Delay Time	t_{DOFBA}	2/3	2		Machine Cycle	
⑤ BA Delay Time	t_{DBA}		TBD		ns	
⑥ BA OFF Time	t_{OFBA}		TBD		ns	
⑦ Output Disable Time	t_{DSOUT}	0			ns	
⑧ Output Enable Time	t_{ENOUT}		TBD		Machine Cycle	
⑨ Input Setup Time	t_{SIN}	0			ns	
⑩ Input Hold Time	t_{HIN}	0			ns	

AC CHARACTERISTICS (Continued)

MASTER/SLAVE MODE INTERFACE TIMING

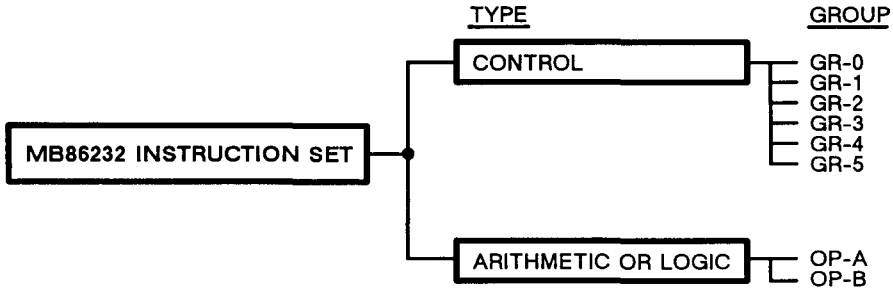


Parameter	Symbol	Min	Typ	Max	Unit	Note
① BA Delay	t_{PBA}		20		ns	
② Output Disable Time	t_{DOUT}		TBD		ns	
③ Output ON Time	t_{EOUT}		TBD		ns	
④ Input ON Time	t_{SIN}	1			Machine Cycle	
⑤ Input Hold Time	t_{HIN}	0			ns	

INSTRUCTION SET

INSTRUCTION SET STRUCTURE

The MB86232 instructions are classified as follows:



The control instructions are classified into five sub-groups GR-0 to GR-5 and most of them can be executed together with Arithmetic or Logic Instructions.

Arithmetic or Logic Instructions are divided into two sub-groups OP-A and OP-B. These divisions are only used for the description of instruction classification and facilitation of available instruction combinations.

(Example of Combined Instructions)

MSMC: LABSC $5, $6: Operation A x B → P
P + C → C
RAM($5) → A
RAM($6) → B
C → RAM($2)

CONTROL INSTRUCTIONS

Group	Function	Instructions (Mnemonic)							Combinable ALU Instructions
GR-0	Double Data Transfer	LAB	LAC	LAD	LASC	LASD	LCSC	LDSD	OP-A/OP-B
	Single Data Transfer	MOV							OP-A/OP-B
GR-1	Triple Data Transfer	LABSA	LABSB	LABSC	LACSC	LACSD	DABSC	DABSD	OP-A
GR-2	Immediate Data Load	LDI	IALB						—
	Mode Setting	STM	CLM						OP-A
	Register File Operation	WFWF	WFRF	RFRF					OP-A
	Register Data Exchange	CHG							OP-A
GR-3	Immediate Data Operation	ANI	ORI	ADI	AIC				—
	Immediate Data Load	LIA	LIB	LIC	LID	LIPH	LIPL		—
GR-4	Clear	CLR0	CLR1						OP-A
	Set	SET							OP-A
	Address Register Addition	ADR							OP-A
	Address Register Logical Operation	ANR							OP-A
	Repeat	REP							OP-A
	Stack Operation	PUSH	POP						—
	Shift Rotation	LSR	ASR	LSL	ASL				—
	No Operation	NOP							—
GR-5	Branch	BRIF	BRUL						—
	Subroutine Jump/Return	BSIF	BSUL	RTIF	RTUL				—
	Conditional Data Transfer	LDIF	LDUL						—
	Return from Interrupt	RIIF	RIUL	IRET					—

ARITHMETIC OR LOGIC INSTRUCTIONS

OP-A Instructions

FIXED POINT/INTEGER OPERATION

Type	Mnemonic	Fixed Mode (32-bit)	Integer Mode (24-bit)	Cycle
OP-A	NOP	No Operation	No Operation	1
OP-A	ADD	a+A → a *1	a+A → a	1
OP-A	SUBa	a-A → a	a-A → a	1
OP-A	ADXa	No Operation	a+A + ca → a*3	1
OP-A	SBXa	No Operation	a-A - ca → a	1
OP-A	MLS	AxB→P(w/sign)*2	AxB→P(w/ sign)*4	1
OP-A	MLU	No Operation	AxB→P(w/o sign)*5	1
OP-A	MSMa	a+P→a, AxB→P	a+PL→a, AxB→P	1
OP-A	MSPa	P→a, AxB→P	PL→a, AxB→P	1
OP-A	SMPa	a+P → a	a+PL → a	1
OP-A	MRDa	a-P→a, AxB→P	a-PL→a, AxB→P	1
OP-A	AND	a AND A → a	a AND A → a	1
OP-A	ORA	a OR A → a	a OR A → a	1
OP-A	EOR	a EOR A → a	a EOR A → a	1
OP-A	NOTa	$\overline{a}$ → a	$\overline{a}$ → a	1
OP-A	ABSa	| a | → a	| a | → a	1
OP-A	ADLa	No Operation*6	a+PL → a	1
OP-A	ALCa	No Operation	a+PL + ca → a	1
OP-A	ADHa	No Operation	a+PH → a	1
OP-A	AHCa	No Operation	a+PH + ca → a	1
OP-A	NEGa	-a → a	-a → a	1
OP-A	NEXa	No Operation	-a - ca → a	1
OP-A	CMPa	a-A	a-A	1

FLOATING POINT OPERATION *7

Type	Mnemonic	Fixed Mode (32-bit)	Integer Mode (24-bit)	Cycle
OP-A	FCPa	a - A		2
OP-A	FADa	a + A → a		2
OP-A	FSBa	a - A → a		2
OP-A	FMLa	A x B → P		2
OP-A	FMSa	a + P → a, A x B → P		2
OP-A	FMRa	a - P → a, A x B → P		2
OP-A	FABa	| a | → a		2
OP-A	FSMa	P + a → a		2
OP-A	FSPa	P → a, A x B → P		2

OP-B Instructions

FIXED POINT/INTEGER OPERATION

Type	Mnemonic	Fixed Mode (32-bit)	Integer Mode (24-bit)	Cycle
OP-A	NOP	No Operation	No Operation	1
OP-A	ADD	a+A → a *1	a+A → a	1
OP-A	SUBa	a-A → a	a-A → a	1
OP-A	ADXa	No Operation	a+A + ca → a*3	1
OP-A	SBXa	No Operation	a-A - ca → a	1
OP-A	MLS	AxB→P(w/sign)*2	AxB→P(w/ sign)*4	1
OP-A	MLU	No Operation	AxB→P(w/o sign)*5	1
OP-A	MSMa	a+P→a, AxB→P	a+PL→a, AxB→P	1
OP-A	MSPa	P → a, AxB → P	PL → a, AxB → P	1
OP-A	SMPa	a+P → a	a+PL → a	1
OP-A	MRDa	a-P→a, AxB→P	a-PL→a, AxB→P	1
OP-A	AND	a AND A → a	a AND A → a	1
OP-A	ORA	a OR A → a	a OR A → a	1
OP-A	EOR	a EOR A → a	a EOR A → a	1
OP-A	NOTa	$\overline{a}$ → a	$\overline{a}$ → a	1
OP-A	ABSa	| a | → a	| a | → a	1
OP-A	ADLa	No Operation*6	a + PL → a	1
OP-A	ALCa	No Operation	a + PL + ca → a	1
OP-A	ADHa	No Operation	a + PH → a	1
OP-A	AHCa	No Operation	a + PH + ca → a	1
OP-A	NEGa	-a → a	-a → a	1
OP-A	NEXa	No Operation	-a - ca → a	1
OP-A	CMPa	a - A	a - A	1

FLOATING POINT OPERATION *7

Type	Mnemonic	Fixed Mode (32-bit)	Integer Mode (24-bit)	Cycle
OP-A	FCPa	a - A		2
OP-A	FADa	a + A → a		2
OP-A	FSBa	a - A → a		2
OP-A	FMLa	A x B → P		2
OP-A	FMSa	a + P → a, A x B → P		2
OP-A	FMRa	a - P → a, A x B → P		2
OP-A	FABa	| a | → a		2
OP-A	FSMa	P + a → a		2
OP-A	FSPa	P → a, A x B → P		2

Notes:

*1. a = accumulator C or D

*2. 24 bits x 24 bits → 48 bits (Fixed point multiplication)

*3. ca = carry

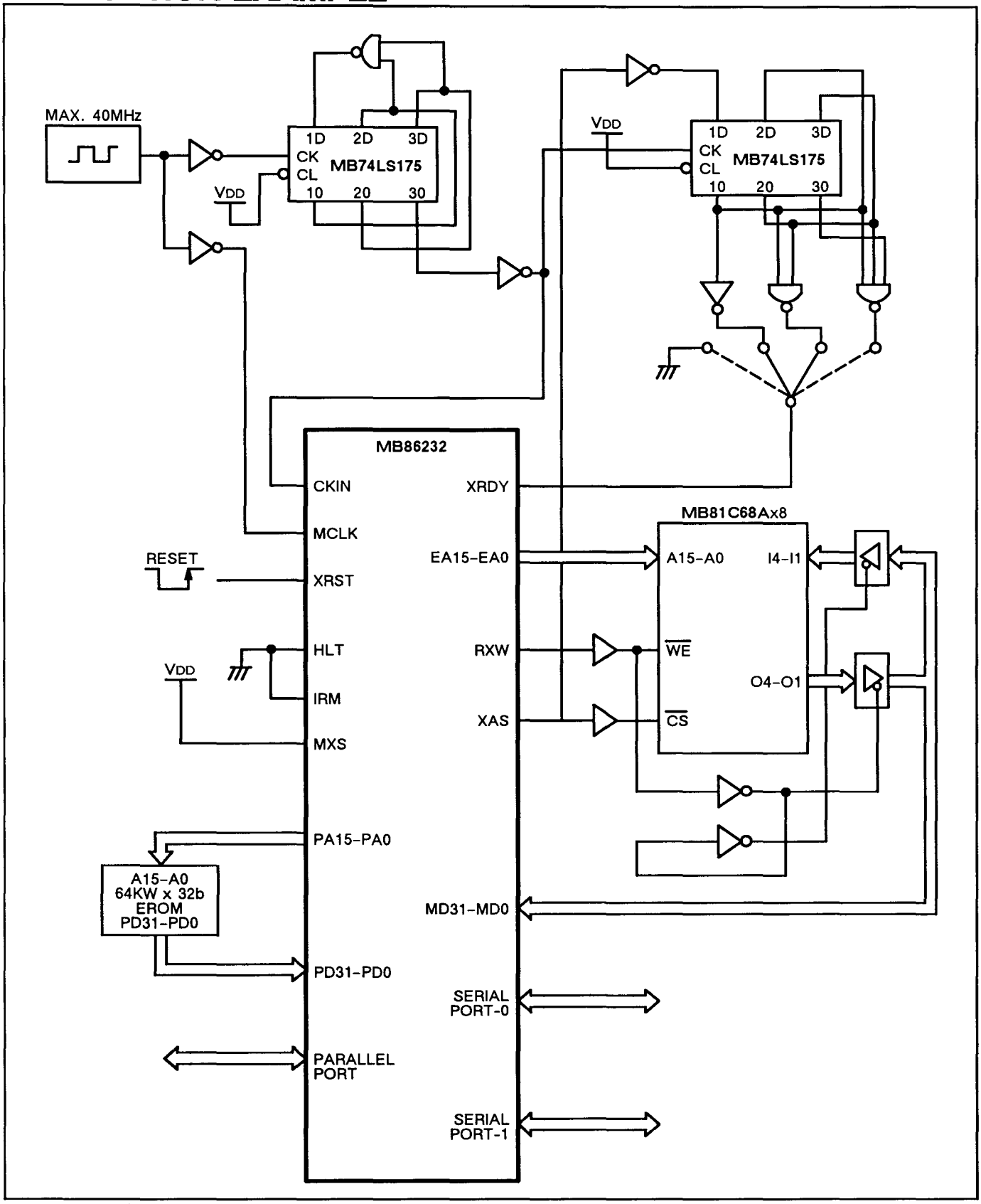
*4. 24 bits x 24 bits → 48 bits (2's complement format)

*5. 24 bits x 24 bits → 48 bits (Absolute format)

*6. "No Operation" indication means that no operation is performed due to an inapplicable operation mode. However, it should be noticed that the operation register values may change.

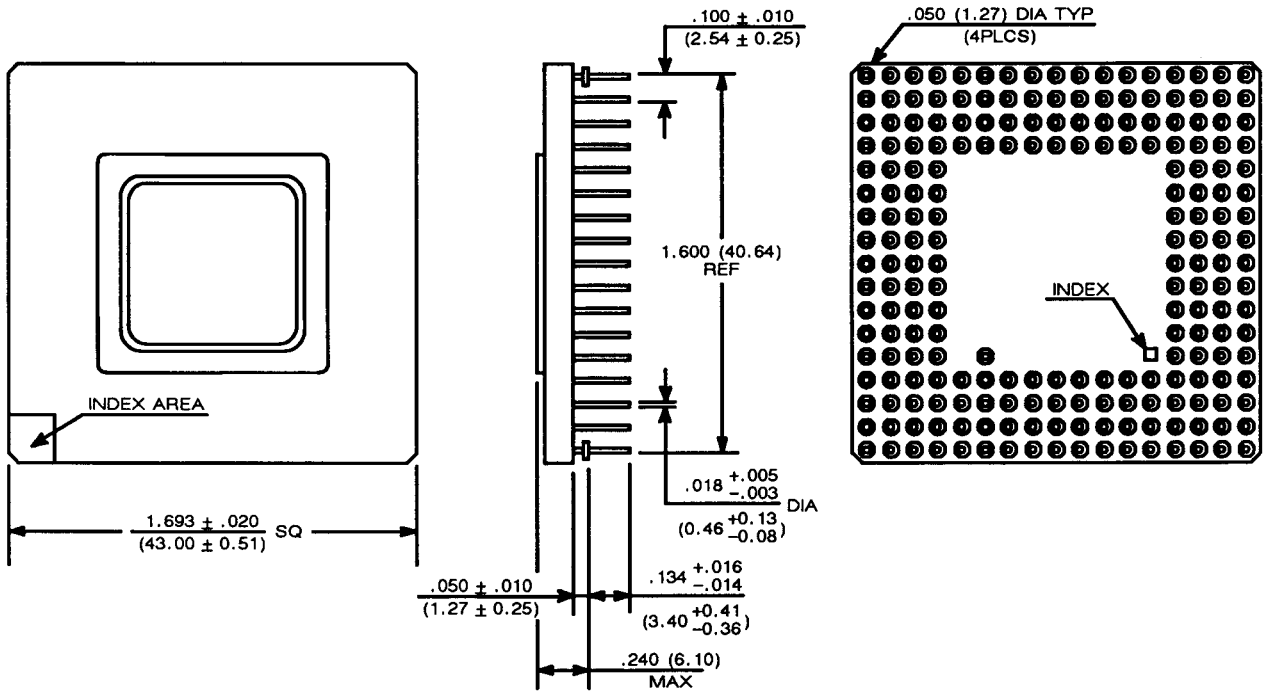
*7. Floating point operations are identical whatever the operation mode.

APPLICATION EXAMPLE



PACKAGE DIMENSION

208-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE
(CASE No.: PGA-208C-A02)



Dimensions in
inches (millimeters)