Volume 1
$2.95

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION

LINEAR & DATA ACQUISITION PRODUCTS

ANALOG DATA BOOK

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION

Harris Linear & Data Acquisition Products

Harris Semiconductor Analog Products represent the state of the art in precision and high speed performance. Capitalizing on the advanced linear processing technologies developed over the past 15 years, Harris Semiconductor Analog Products offer high quality and unmatched performance.

This book describes Harris Semiconductor's complete line of Linear and Data Acquisition products, and includes a complete set of product specifications and data sheets, application notes and a separate section describing our quality and high reliability program.

Please fill out the registration card at the back of this book and return it to us so we may keep you informed of our latest new product developments over the next year.

If you need more information on these and other Harris products, please contact the nearest Harris sales office listed in the back of this data book.

Harris Semiconductor's products are sold by description only. Harris reserves the right to make changes in circuit design, specifications and other information at any time without prior notice. Accordingly, the reader is cautioned to verify that data sheets and other information in this publication are current before placing orders. Information contained in application notes is intended solely for general guidance; use of the information for user's specific application is at user's risk. Reference to products of other manufacturers are solely for convenience of comparison and do not imply total equivalency of design, performance, or otherwise.

Printed in USA

Contents

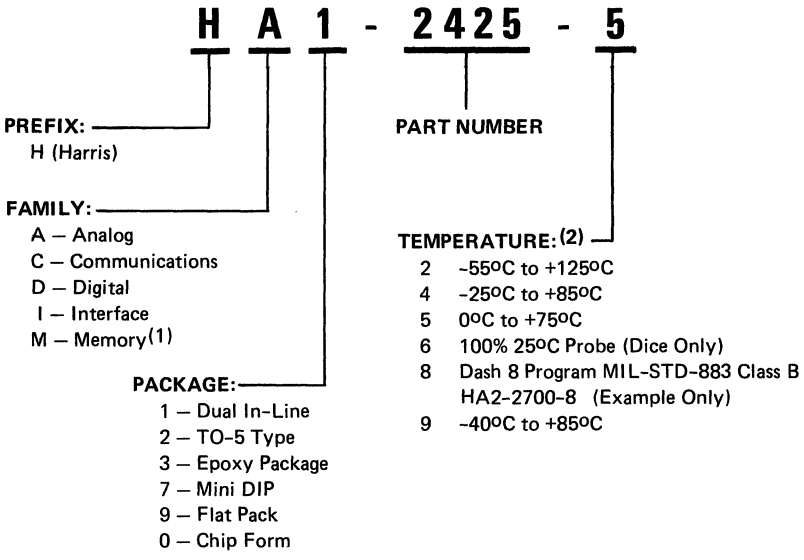
Alpha-Numeric Product Index

(continued)

Ordering Information

Harris Products are designated by "Product Code". When ordering please refer to products by the full code. Harris products will always begin with H. Specific device numbers will always be isolated by hyphens.

PRODUCT CODE EXAMPLE



NOTE:
(1) EXCEPT –
HPROM X-1024-X
HPROM X-8256-X
HPROM X-0152-X

(2) The 54C/74C CMOS Family temperature designation is contained in the Part Number.
54CXX -55°C to +125°C
74CXX 0°C to +70°C

HARRIS DASH 8 PROGRAM

As a service to users of High Rel products Harris makes readily available via the high reliability DASH 8 program many products from our product lines. Parts screened to MIL-STD-883 Method 5004 Class B are simply branded with the post-script "-8" to the appropriate Harris part numbers, in effect, offering "off the shelf" delivery. For details concerning this special Harris program for High Rel users, see the Dash 8 section of this Data Book.

SPECIAL ORDERS

For best availability and price, it is urged that standard "Product Code" devices be specified, which are available worldwide from authorized distributors. Where enhanced reliability is needed, note standard "Dash 8" screening described in this Data Book. Harris application engineers may be consulted for advice about suitability of a part for a given application.

If additional electrical parameter guarantees or reliability screening are absolutely required, a Request for Quotation and Source Control Drawing should be submitted through the local Harris Sales Office or Sales Representative. Since, many electrical parameters may be economically assured through design analysis, characterization, or correlation with other parameters, additionally desired parameters should be labeled, "Vendor will guarantee, but not necessarily test".

Harris reserves the right to decline to quote, or to request modification to special screening requirements.

I. C. Handling Procedures

Harris Analog I.C. processes produce circuits more rugged than similar ones. However, no semiconductor is immune from damage resulting from the sudden application of many thousands of volts of static electricity. While the phenomenon of catastrophic failure of devices containing MOS transistors or capacitors is well known, even bipolar circuits can be damaged by static discharge, with altered electrical properties and diminished reliability. None of the common I.C. internal protection networks operate quickly enough to positively prevent damage.

It is suggested that all semiconductors be handled, tested, and installed using standard "MOS handling techniques" of proper grounding of personnel and equipment. Parts and subassemblies should not be in contact with untreated plastic bags or wrapping material. High impedance I.C. inputs wired to a P.C. connector should have a path to ground on the card.

HANDLING RULES

Since the introduction of integrated circuits with MOS structures and high quality junctions, a safe and effective means of handling these devices has been of primary importance. One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existance in the industry. In addition most compensation networks in linear circuits are located at high impedance nodes, where protection networks would disturb normal circuit operation. If static discharge occurs at sufficient magnitude (2KV or more), some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10KV in a low humidity environment; thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. It is evident, therefore, that proper handling procedures or rules should be adopted.

Elimination or reduction of static charge can be accomplished as follows:

- Use conductive work stations. Metallic or conductive plastic* tops on work benches connected to ground help eliminate static build-up.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1-M ohm to ground. The 1-M ohm resistor will prevent electroshock injury to personnel.
- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold, or aid, in the generation of a static change. Where they cannot be eliminated natural materials such as cotton etc. should be used to minimize charge generation capacity.
- Control relative humidity to as high as a level as practical. (RH 50%).
- Ionized air blowers reduce charge build-up in areas where grounding is not possible or desirable.
- Devices should be in conductive carriers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam or foil.
- In automated handling equipment, the belts, chutes, or other surfaces should be of conducting material. If this is not possible, ionized air blowers may be a good alternative.

* Supplier 3M Company "Velostat"

Harris Analog I. C. Technologies

JUNCTION ISOLATION (J.I.)

This is the most common integrated circuit process. Bipolar I.C.'s generally begin with a p-type wafer into which a buried layer pattern, if used, is first diffused. Then the n-type epitaxial layer is grown, and p-type isolation walls are diffused around each area which is to be electrically isolated from the other circuitry. These isolation walls must be diffused deeply into the wafer in order to contact the original p-substrate. In operation, the p-substrate and isolation walls are connected to the most negative circuit potential, so that each active area is surrounded on the sides and bottom by a reverse biased junction through which negligible current flows (Figure 1).

To complete the I.C., base and emitter diffusions are performed, the wafer is coated with aluminum and the conductor pattern is etched.

Representative Harris devices using this process are HA-2820, HA-4741 and HD-0165.

DIELECTRIC ISOLATION (D.I.)

A somewhat different process has been proven particularly advantageous for fabricating high performance analog I.C.'s. This is dielectric isolation (D.I.), where each active area is surrounded on the sides and bottom by an insulating layer of silicon dioxide, and for mechanical strength imbedded in polycrystalline silicon. This process for bipolar I.C.'s begins with a wafer of n-type silicon. The side of the wafer which will eventually be the bottom is deeply etched to form the sidewall pattern, then silicon dioxide and polycrystalline silicon are grown to fill the etched "moats". The opposite side of the wafer is then polished until the insulating sidewalls appear at the wafer surface (Figure 2). Conventional diffusion and metallization processes follow to complete the I.C. D.I. for analog I.C.'s has a number of advantages:

1. Almost all op amp designs require at least one PNP transistor in the signal path. Typical J.I. op amps must use a lateral PNP which inherently has very low frequency response, limiting typical compensated bandwidth to 1MHz. The D.I. process makes it practical to build a vertical PNP with much higher bandwidth making possible compensated op amp bandwidths of 12MHz or higher (Figure 3). Also, transistor collector to substrate capacitance is 2/3 less using D.I., further enhancing high frequency performance.
2. Other devices such as optimally specified MOS or JFET transistors may be fabricated on the same chip. Isolated diffused and thin film resistors are also practical.
3. The isolation removes the possibility of parasitic SCR's which might create latchup under certain sequences of power and signal application.
4. Leakage currents to the substrate under high temperature or nuclear radiation conditions are greatly reduced. While the circuits in this catalog were not specifically designed for high radiation environments or operating temperatures greater than +125°C, many have shown superior performance. For I.C.'s requiring the ultimate in radiation resistance, Harris Semiconductor Programs Division should be consulted.

DIELECTRIC ISOLATED CMOS

J.I. processed CMOS Analog I.C.'s, which are generally used in conjunction with several power supplies, are particularly prone to parasitic SCR latchup failures and failures due to input voltage spikes. The D.I. CMOS process, which is compared in detail in Harris Application Note 521, has proved to be the best solution.

Since analog multiplexers are often used at the input of a data acquisition system, particular attention must be paid to the possibility of damaging input overvoltage conditions. Harris has provided an effective answer in the HI-506A through HI-509A multiplexers with built-in overvoltage protection.

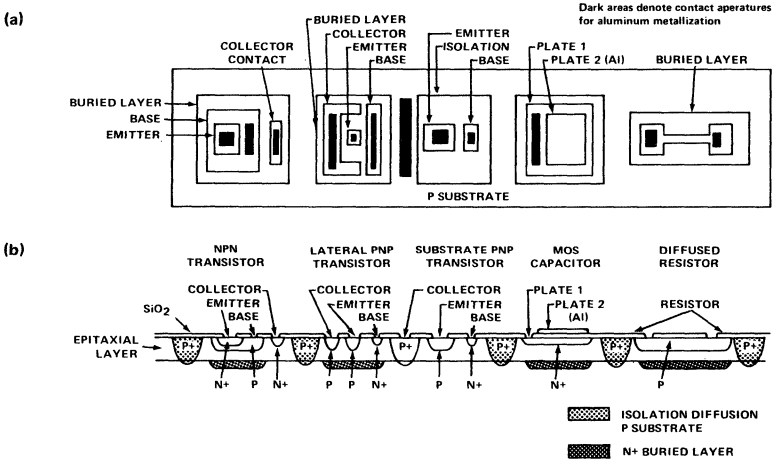


Figure 1 — Structures of various components formed in the junction-isolation process. (a) Topological view. (b) Cross-sectional view.

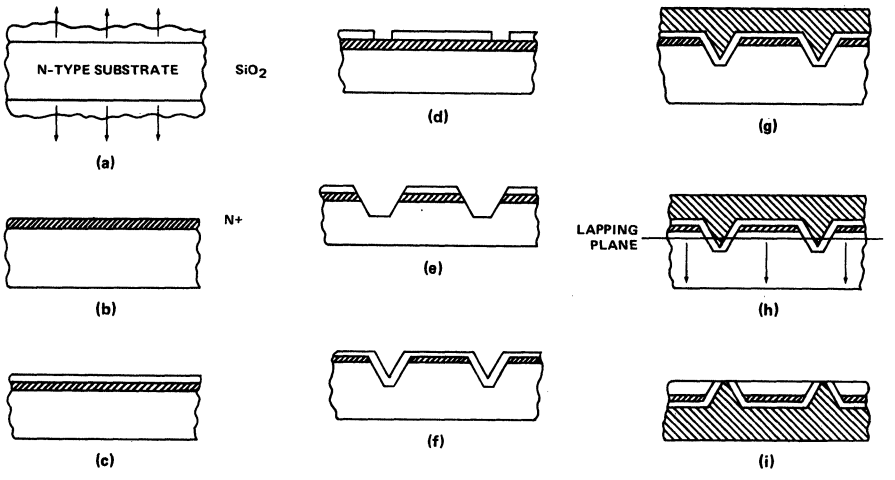


Figure 2 — Process steps for dielectric isolation. (a) Surface preparation, (b) N- buried layer diffsuion, (c) masking oxide, (d) isolation pattern, (e) silicon etch, (f) dielectric oxide, (g) polycrystalline deposition, (h) backlap and polish, (i) finished slice.

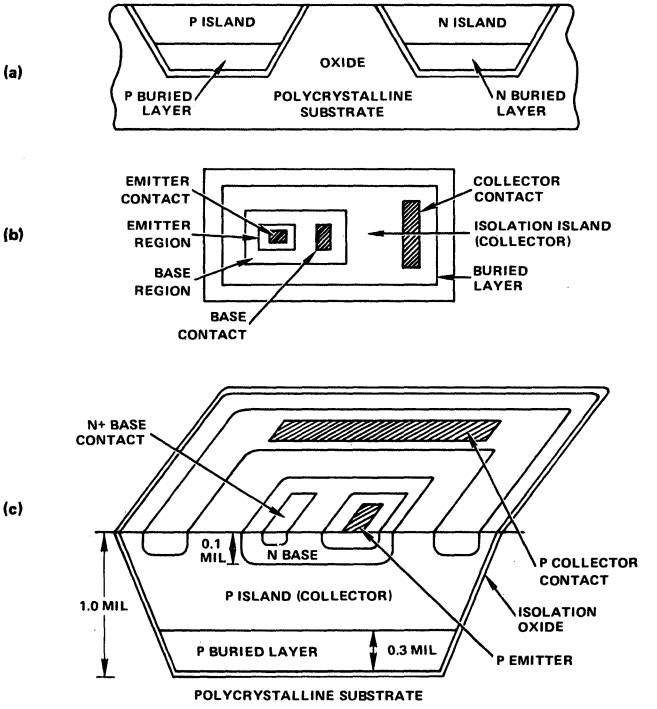


Figure 3 — The high-frequency process. (a) Cross-sectional view of P and N islands for PNP and NPN transistors. (b) Topological view showing relative placement of transistor regions. (c) Cross-sectional view of high-frequency PNP device formation in the D.I. process.

Cross Reference

MANUFACTURER	PART NUMBER	HARRIS EQUIVALENT	NOTES
Advanced Micro Devices	AM118/318	HA-2510/2515	B2
	AM715	HA-2520/2525	B2
	AM1660	HA-2500/2505	B2
		HA-2600/2605	B2
		HA-2700/2705	B2
Analog Devices	AD505	HA-2530/2535	C2
	AD507J*	HA-2625	A1
	AD507S	HA-2620	A1
	AD509J*	HA-2525	A1
	AD509S	HA-2520	A1
	AD518	HA-2510/2515	B2
	AD562	HI-562	B2
	AD582	HA-2420/2425	C2
	AD583K	HA-2425	A1
	AD7501	HI-1818A	B2
	AD7502	HI-1828A	B2
	AD7503	HI-1818A	B2
	AD7506	HI-506	A1
	AD7507	HI-507	A1
	AD7510	HI-201	C2
	AD7511	HI-201	C2
	AD7512	HI-5043	C2
	AD7513	HI-200	A1
Burr Brown	3500A/3501A	HA-2605	B2
	3500R/3501R	HA-2600	B2
	3505J	HA-2505	A1
	3506J	HA-2605	A1
	3507J	HA-2525	A1
	3508J	HA-2625	A1
	3550J	HA-2055	B2
	3550K	HA-2050	B2
	3550S	HA-2055	B2
	3553AM	HA-2630	C3
	MPC4D	HI-509A-5	A1
	MPC8S	HI-508A-5	A1
	MPC8D	HI-507A-5	A1
	MPC16S	HI-506A-5	A1
Datel	AM-405-2	HA2-2055-5	A1
	AM-406-2	HA2-2065-5	A1
	AM-450-2	HA-2505	A1
	AM-452-2	HA2-2525-5	A1
	AM-460-2	HA-2605	A1
	AM-462-1	HA1-2625-5	A1
	AM-462-2	HA2-2625-5	A1
	AM-464-2	HA-2645	A1
	AM-490-2A	HA-2905	A1
	MX-808	HI-508A-5	A1
	MX-1606	HI-506A-5	A1
	MXD-409	HI-509A-5	A1
	MXD-807	HI-507A-5	A1
	SHM-1C-1	HA-2425	A1
Exar	XR215	HA-2820/2825	C3
	XR4212	HA-4741	A2

* "K" equivalent is either military device or selected commercial device.

NOTES: A. Pin-for-pin replacement.
B. Minor pinout difference (offset adj., compensation, etc.).
C. Not pin compatible — consult data sheets.

1. Identical electrical specifications.
2. Harris part superior in most parameters.
3. Parameter tradeoffs — consult data sheets.

Cross Reference

MANUFACTURER	PART NUMBER	HARRIS EQUIVALENT	NOTES
Fairchild Semiconductor	μA702	HA-2620/2625	C2
	μA709	HA-909/911	B2
	μA715	HA-2520/2525	B2
	μA725	HA-2700/2705	A3
	μA727	HA-2900/2905	C2
	μA740	HA-2060/2065	B2
	μA741	HA-909/911, 2600/2605	B2
		2700/2705	B2
		2640/2645	A2
	μA747	HA-2650/2655	C2
	μA748	HA-2620/2625	B2
	μA772	HA-2510/2515	A2
	μA776	HA-2720/2725	A2
	μA791	HA-2630/2635	C2
	SH3002	HI-1800A	C2
	1558/1458	HA-2650/2655	A2
Intersil	4250	HA-2720	A2
	4250C	HA-2725	A2
	IH5040* thru IH5051	HI-5040 thru HI-5051	A1
	8007	HA-2060/2065	B2
	8008	HA-2600/2605	B2
	8017	HA-2520/2525	B2
	8021M	HA-2720	A2
	8021C	HA-2725	A2
	8022M	HA-2730	C2
	8022C	HA-2735	C2
	IH5110/5111	HA-2420/2425	C2
	IH5060	HI-506A	A2
	IH5070	HI-507A	A2
		M = -2 C = -5 DE = HI 1 PE = HI 1 TW = HI 2 IH-5040MDE	
	*Part Numbers: Intersil		
	Harris	HI 1-5040-2	
Intronics	FA-550	HA-2055	A1
	FA-551	HA-2065	A1
	A-560	HA-2525	A1
	A-561	HA-2625	A1
	A-570	HA-2535	A1
	CA-580	HA-2905	A1
Motorola	MC1508/1408	HI-1080/1085	C2
	MC1520/1420	HA-2600/2605	C2
	MC1530/1531/1430/1431	HA-2600/2605	C2
	MC1522/1433	HA-2700/2705	C2
	MC1536/1436	HA-2640/2645	A2
	MC1538/1438	HA-2630/2635	C2
	MC1539/1439	HA-2620/2625	B2

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Cross Reference

MANUFACTURER	PART NUMBER	HARRIS EQUIVALENT	NOTES
Motorola (continued)	MC1545/1445	HA-2400/2405	C3
	MC1554/1454	HA-2630/2635	C3
	MC1556/1456	HA-2600/2605	B2
	MC1558/1458	HA-2650/2655	A2
	MC1582L	HD-245	C2
	MC1583L	HD-246	C2
	MC1584L	HD-249	C2
	MC3301/3401	HA-4741	C2
	MC3302	HA-4900	C2
	MC3403/3503	HA-4741	A2
	MC4741	HA-4741	A2
National Semiconductor	LF155/156/157/355/356/357	HA-2060/2065	B2
	LF198/398	HA-2420/2425	C2
	LH0001	HA-2700	C2
	LH0002	HA-2630	C2
	LH0003	HA-2520	C2
	LH0004	HA-2640	C2
	LH0005	HA-2620	C2
	LH0022/42/52	HA-2060/2065	B2
	LH0023/43	HA-2420/2425	C2
	LH0024	HA-2530/2535	B2
	LH0032	HA-2050/2055	C3
	LH0033/63	HA-2630/2635	C3
	LH0062	HA-2050/2055	B2
	LM101/301/107/307	HA-909/911, 2600/2605, 2700/2705	B2
	LM102/302	HA-2600/2605	B2
	LM108/208/308	HA-2700/2704/2705	B3
	LM110/310	HA-2500/2505	B2
	LM112/212/312	HA-2700/2704/2705	B3
	LM216/316	HA-2060/2065	B3
	LM118/318	HA-2510/2515	B2
	LM124/324	HA-4741	A2
	LM139/339	HA-4900/4905	C2
	LM143/343	HA-2640/2645	A2
	LM144/344	HA-2640/2645	A2
	LM148/348	HA-4741	A2
	LM149/349	HA-4602/4605	A2
	LM163/363	HD-248/548	C3
Precision Monolithics	OP-01	HA-2600/2605/2500/2505	B2
	OP-05/07	HA-2900/2905	B2
	CMP-01/02	HA-2111/2311	B3
	SSS1558/1458	HA-2650/2655	A2
	DAC-02/04/100	HI-1080/1085	C3
	DAC-12	HI-562A	C2
RCA	CA3020	HA-2630/2635	C2
	CA3078	HA-2720/2730	B2
	CA3100	HA-2520/2525	B2
	CA3130	HA-2060/2065	B2
	CA3558/3458	HA-2650/2655	A2
	CA6078	HA-2720/2730	B2
	CD4016	HI-201	C2
	CD4046	HA-2820/2825	C2

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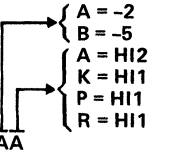
Cross Reference

MANUFACTURER	PART NUMBER	HARRIS EQUIVALENT	NOTES
Raytheon	RM/RC1556A	HA-2600/2605	B2
	RM/RC4131	HA-2600/2605	B2
	RM/RC4132	HA-2700/2705	B2
	RM/RC4136	HA-4741	C2
	RM/RC4156	HA-4741 (selected)	A1
	HA-4741	HA-4741	A1
	RM/RC4531	HA-2500/2505	B2
	RM/RC4558	HA-2650/2655	A2
	111/211/311	HA-2111/2211/2311	A1
	1488	HD-1488	A1
	1489/1489A	HA-1489/1489A	A1
Signetics	531	HA-2510/2515	B2
	536	HA-2060/2065	B2
	560	HA-2820/2825	C2
	561	HA-2820/2825	C2
	562	HA-2820/2825	C2
	565	HA-2820/2825	C2
	5556	HA-2600/2605	B2
	5558	HA-2650/2655	A2
Silicon General	SG741S	HA-2500	B2
	SG741SG	HA-2505	B2
Siliconix	DG181*	HI-5048	C2
	DG184	HI-5049	A2
	DG185	HI-5045	A2
	DG187	HI-5050	C2
	DG188	HI-5042	C2
	DG190	HI-5051	A2
	DG191	HI-5043	A2
	DG200	HI-200	A2
	DG201	HI-201	A2
	DG506	HI-506	A1
	DG507	HI-507	A1
	DG508	HI-508A	A3
	DG509	HI-509A	A3
	L120	HA-2060/2065	B2
	L140	HA-2720/2725	B2
	*Part Numbers: Siliconix	DG200AA	
	Harris	HI2-200-2	



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Solitron	CM4016A	HI-201	C2
	μc4000/4001/4002	HA-2600	C2
	μc4000C/4001C/4002C	HA-2605	C2
	μc4250	HA-2720	A2
	μc4250c	HA-2725	A2
Sprague	μLS/μLN2139	HA-2600/2605	B2
	μLS/μLN2151	HA-2600/2605	B2
	μLS/μLN2156	HA-2600/2605	B2
	μLS/μLN2157	HA-2650/2655	B2
	μLS/μLN2158	HA-2620/2625	B2
	μLS/μLN2171	HA-2600/2605	B2
	μLS/μLN2172	HA-2620/2625	B2
	μLS/μLN2173	HA-2600/2605	B2
	μLS/μLN2174	HA-2620/2625	B2
	μLS/μLN2175	HA-2600/2605	B2
	μLS/μLN2176	HA-2620/2625	B2
	μLS/μLN2177	HA-2060/2065	B2
	μLS/μLN2178	HA-2060/2065	B2
Teledyne Philbrick	1321	HA-2625	A1
	1322	HA-2525	A1
	1323	HA-2705	A1
	1324	HA-2505	B2
	1332	HA-2645	A1
	1339	HA-2625	B2
	1340	HA-2905	A1
	1422	HA-2055/2065	B2
	1427	HA-2065	C2
	1433	HA-2065A	A1
	1433-01	HA-2060A	A1
	1434	HA-2055A	A1
	1434-01	HA-2050A	A1
	4551	HI-507A-5	A1
	4552	HI-506A-5	A1
	4856	HA-2425	A1
Texas Instruments	TL022M/C	HA-2730/2735	B2
	TL044	HA-4741	C2
	TL084	HA-4602	A2
	TL0891/089C	HA-2904/2905	A2
	52/72310	HA-2500/2505	B2
	52111/72311	HA-2111/2311	A1
	52/72558	HA-2650/2655	A2
	52/72660	HA-2700/2705	B2
	52/72770	HA-2600/2605	B2
	52/72771	HA-2620/2625	B2
	75107A/108A	HD-549	C2
	75109/110	HD-545	C2
	75150	HD-1488	C2
	75152	HD-1489/A	C2
	75154	HD-1489/A	C2
Transitron	TOA7709	HA-2600	B2
	TOA8709	HA-2605	B2
	TOA7809	HA-2060A	B2
	TOA8809	HA-2065A	B2

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Operational Amplifiers and Comparators

Operational Amplifiers Selection Guide

PARAMETER†	-55°C to +125°C															UNITS
		F.E.T. PREAMP						PRAM™	S/H							
	HA-909	HA-2000	HA-2000A	HA-2050	HA-2050A	HA-2060	HA-2060A	HA-2400	HA-2420	HA-2500	HA-2502	HA-2510	HA-2512	HA-2520	HA-2522	
INPUT CHARACTERISTICS																
Offset Voltage	6	25	12	30	17	30	15	7	6	8	10	11	14	11	14	mV
Drift (Typ.)	10	50	20	50	20	50	20	20	5	20	20	20	25	20	25	μV/°C
Bias Current	300(1)	10	10	10	10	10	10	400	400	400	500	400	500	400	500	nA
Offset Current	300	5	5	5	5	5	5	100	100	50	100	50	100	50	100	nA
Common Mode Range	±12	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	V
INPUT NOISE (1)	5															μVRMS
TRANSFER CHARACTERISTICS																
Large Signal Voltage Gain	25K	.98	.98	5K	5K	60K	60K	25K	25K	15K	10K	7.5K	5K	7.5K	5K	V/V
Common Mode Rejection Ratio	80	80	80	74	74	74	74	80	80	80	74	80	74	80	74	dB
Bandwidth (Typ.)(1)	7	10	10	20(3)	20(3)	24(3)	24(3)	16(3)	2	12	12	12	12	25	25	MHz
OUTPUT CHARACTERISTICS																
Output Voltage Swing	±12	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	V
Output Current (1)	±20	+5(1)	+5(1)	±10(1)	±10(1)	±10(1)	±10(1)	±20(1)	±10	±10	±10	±10	±10	±10	±10	mA
Full Power Bandwidth (Typ.)(1)	25	1,000(3)	1,000(3)	2,000(3)	2,000(3)	600(3)	600(3)	500(3)	70	500	500	1,000	1,000	1,500	1,500	kHz
TRANSIENT RESPONSE																
Rise Time (1)	75	50(3)	50(3)	50(3)	50(3)	50(3)	50(3)	20(3)	100(3)	50	50	50	50	50	50	ns
Overshoot (1)	40	5(3)	5(3)	25(3)	25(3)	25(3)	25(3)	25(3)	20(3)	40	50	40	50	40	50	%
Slew Rate (1)	±1.2	100(3)	100(3)	120(3)	120(3)	35(3)	35(3)	50(3)	5(3)	±25	±20	±50	±40	±100	±80	V/μs
Settling Time (Typ.)(1)	(2)	0.4(3)	0.4(3)	0.4(3)	0.4(3)	0.8(3)	0.8(3)	1.5(3)		0.33	0.33	0.25	0.25	0.20	0.20	μs
POWER SUPPLY CHARACTERISTICS																
Supply Current (1)	2.5	1.7(1)	1.7(1)	8.0(1)	8.0(1)	6.0(1)	6.0(1)	6.0(1)	5.0	6.0	6.0	6.0	6.0	6.0	6.0	mA
Power Supply Rejection Ratio	80	80	80	74	74	74	74	80	80	80	74	80	74	80	74	dB
FUNCTIONAL CHARACTERISTICS																
Offset Adjust	Yes*	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Compensation Components	0	0	0	OAV>3	OAV>3	OAV>5	OAV>5	OAV>10	0	0	0	0	0	OAV>3	OAV>3	
Output Protection	No	No	No	No	No	Yes	Yes	Yes	Yes	No	No	No	No	No	No	

(1) At +25°C
(2) Not applicable or not specified
(3) Typical
(4) V_{SUPPLY} = ±40V
(5) Dependent upon I_{SET} value

* TO-86 only † Guaranteed for ±15V supplies and applicable temperature range unless otherwise specified.

Operational Amplifiers Selection Guide

PARAMETER†	-55°C to +125°C														UNITS
	HA-2530	HA-2600	HA-2602	HA-2620	HA-2622	HA-2630	HA-2640	HA-2650	HA-2700	HA-2720	HA-2730	HA-2900	HA-4741	HA-4602	
INPUT CHARACTERISTICS										(5)	(5)				
Offset Voltage	3	6	7	6	7	±300	6	±5	5	5	5	.06	5.0	3.0	mV
Drift (Typ.)	5	5	5	5	5	(2)	15	8	5	8 to 10	8 to 10	.3	5	2	μV/°C
Bias Current	100	30	60	35	60	200	50	200	50	10 to 40	10 to 40	1	325	325	nA
Offset Current	20	30	60	35	60	(2)	35	60	30	7.5 to 20	7.5 to 20	.5	75	125	nA
Common Mode Range	±.5	±11	±11	±11	11	±10	±35(4)	±13	±11	±10	±10	±10	±12	±12	V
INPUT NOISE (1)															μVRMS
TRANSFER CHARACTERISTICS										(5)	(5)				
Large Signal Voltage Gain	100K	70K	60K	70K	60K	.85	75K	20K	100K	25K	25K	10^6	25K	100K	V/V
Common Mode Rejection Ratio	86	80	74	80	74	(2)	80	80	86	80	80	120	74	86	dB
Bandwidth (Typ.)(1)	20	12	12	35	35	8	4	8	1	.01 to 10	.01 to 10	3	3.5	8	MHz
OUTPUT CHARACTERISTICS										(5)	(5)				
Output Voltage Swing	±10	±10	±10	±10	±10	±10	±35(4)	±13	±11	±13.5(3)	±13.5(3)	±10	±10	±10	V
Output Current (1)	±25	±15	±10	±10	±10	±400	±12	20(3)	±22(3)	±.5 to 5.0(3)	±.5 to 5.0(3)	±10	±5.0	±10	mA
Full Power Bandwidth (Typ.)(1)	5,000	75	75	600	600	8,000	23	30	50	1.5 to 80(3)	1.5 to 80(3)	40	25	60	kHz
TRANSIENT RESPONSE										(5)	(5)				
Rise Time	40	60	60	45	45	30(3)	60(3)	40(3)	(2)	200 to 2,000(3)	200 to 2,000(3)	200(3)	75	50(3)	ns
Overshoot (1)	45	40	40	(2)	(2)	25(3)	15(3)	15(3)	(2)	5 to 15(3)	5 to 15(3)	20(3)	25	30(3)	%
Slew Rate (1)	±280	±4	±4	±25	±20	200	5(3)	±2	±10	.1 to .8(3)	.1 to .8(3)	2.5(3)	±1.6	±4.0(3)	V/μs
Settling Time (Typ.)(1)	.5	1.5	1.5	0.30	0.30	.5(3)	1.5(3)	1.5(3)	5.0	(2)	(2)	(2)	12	4.2(3)	μs
POWER SUPPLY CHARACTERISTICS										(5)	(5)				
Supply Current (1)	6	3.7	4.0	3.7	4.0	20	3.8	3	0.15	.02 to .2	.02 to .2	5	5.0	5.5	mA
Power Supply Rejection Ratio	86	80	74	80	74	66	80	80	86	80	80	120	80	86	dB
FUNCTIONAL CHARACTERISTICS															
Offset Adjust	No	Yes	Yes	Yes	Yes	No	Yes	DIP Pkg. Only	Yes	Yes	Yes	No	No	No	
Compensation Components	1	0	0	OAV>5	OAV>5	0	0	0	0	0	0	3	0	0	
Output Protection	No	Yes	Yes	Yes	Yes	External	Yes	Yes	Yes	Yes	Yes	Yes	Yes(6)	Yes(6)	

(1) At +25°C
(2) Not applicable or not specified
(3) Typical
(4) V_{SUPPLY} = ±40V
(5) Dependent upon I_{SET} value

* TO-86 only † Guaranteed for ±15V supplies and applicable temperature range unless otherwise specified.

Operational Amplifiers Selection Guide

PARAMETER†	0°C to +75°C														UNITS
		F.E.T. PREAMP						PRAM™	S/H						
	HA-911	HA-2005	HA-2005A	HA-2055	HA-2055A	HA-2065	HA-2065A	HA-2405	HA-2425	HA-2505	HA-2515	HA-2525	HA-2535	HA2605	
INPUT CHARACTERISTICS															
Offset Voltage	7.5	55	12	65	17	65	15	11	8	10	14	14	5	7	mV
Drift (Typ.)	15	60	40	60	40	60	40	30	5	20	30	20	5	5	μV/°C
Bias Current	750	1	1	1	1	1	1	500	400	500	500	500	200	40	nA
Offset Current	450	.5	.5	.5	.5	.5	.5	100	100	100	100	100	20	40	nA
Common Mode Range	±12	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±.5	±11	V
INPUT NOISE (3)	1														μVRMS
TRANSFER CHARACTERISTICS															
Large Signal Voltage Gain	15K	.98	.98	5K	5K	70K	70K	25K	25K	10K	5K	5K	100K	70K	V/V
Common Mode Rejection Ratio	74	70	70	70	70	70	70	74	74	74	74	74	80	74	dB
Bandwidth (Typ.)	7	10(3)	10(3)	20(3)	20(3)	24(3)	24(3)	18(3)	2(3)	12(3)	12(3)	25	20	12	MHz
OUTPUT CHARACTERISTICS															
Output Voltage Swing	±11	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	±10	V
Output Current (1)	±15	±5	±5	±10(1)	±10(1)	±10(1)	±10(1)	20(3)	±10	±10	±10	±10	±25	±10	mA
Full Power Bandwidth (Typ.)(1)	35	1,000(3)	1,000(3)	2,000(3)	2,000(3)	600(3)	600(3)	200(3)	70(3)	500	1,000	1,500	5,000	75	kHz
TRANSIENT RESPONSE															
Rise Time (1)	75	50(3)	50(3)	50(3)	50(3)	50(3)	50(3)	20	100(3)	50	50	50	40	60	ns
Overshoot (1)	40	5(3)	5(3)	25(3)	25(3)	25(3)	25(3)	25	20(3)	50	50	50	50	40	%
Slew Rate (1)	±2.3	100(3)	100(3)	120(3)	120(3)	35(3)	35(3)	15	5(3)	±20	±40	±80	±250	±4	V/μs
Settling Time (Typ.)(1)	(2)	0.4(3)	0.4(3)	0.4(3)	0.4(3)	.8(3)	.8(3)	1.5		0.33	0.25	0.20	.5	1.5	μs
POWER SUPPLY CHARACTERISTICS															
Supply Current (1)	2.5	1.7	1.7	8.0	8.0	6.0	6.0	6.0	5.0	6.0	6.0	6.0	6	4.0	mA
Power Supply Rejection Ratio	74	70	70	70	70	70	70	74	74	74	74	74	80	74	dB
FUNCTIONAL CHARACTERISTICS															
Offset Adjust	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	No	Yes	
Compensation Components	0	0	0	OAV>3	OAV>5	OAV>5	OAV>5	OAV>10	0	0	0	OAV>3	1	0	
Output Protection	No	No	No	No	No	Yes	Yes	No	Yes	No	No	No	No	Yes	

(1) At +25°C
(2) Not applicable or not specified
(3) Typical
(4) $V_{SUPPLY} = \pm 40V$
(5) Dependent upon I_{SET} value

* TO-86 only † Guaranteed for ±15V supplies and applicable temperature range unless otherwise specified.

Operational Amplifiers Selection Guide

PARAMETER†	0°C to +75°C										-25°C to +85°C			UNITS
											PRAM™			
	HA-2625	HA-2635	HA-2645	HA-2655	HA-2705	HA-2725	HA-2735	HA-2905	HA-4741	HA-4605	HA-2404	HA-2704	HA-2904	
INPUT CHARACTERISTICS														
Offset Voltage	7	300	7	7	7	7	7	.08	6.5	4.0	7	6	.05	mV
Drift (Typ.)	5	(2)	15	8	5	8 to 10	8 to 10	.2	5	2	20	5	.2	μV/°C
Bias Current	40	200	50	300	70	10 to 40	10 to 40	1	400	400	400	50	1	nA
Offset Current	40	(2)	50	100	40	7.5 to 20	7.5 to 20	.5	100	120	100	30	.5	nA
Common Mode Range	±11	(2)	±35(4)	±13	±11	±10	±10	±10	±12	±12	±10	±11	±10	V
INPUT NOISE (3)														μVRMS
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain	70K	.85	75K	15K	100K	20K	20K	10^6	15K	75K	25K	100K	10^7	V/V
Common Mode Rejection Ratio	74	(2)	74	74	80	74	74	120	74	80	80	86	130	dB
Bandwidth (Typ.)(1)	35	8	4	8	1	.01 to 10	.01 to 10	3	3.5	8	16(3)	1	3	MHz
OUTPUT CHARACTERISTICS														
Output Voltage Swing	±10	±10	±35(4)	±13	±11	±13.5(3)	±13.5(3)	±10	±10	±10	±10	±11	±10	V
Output Current (1)	±10	±300	±10	18(3)	±22(3)	.5 to 5.0(3)	.5 to 5.0(3)	±7	±5	±8	20(1)	±22(3)	±10	mA
Full Power Bandwidth (Typ.)	600	8,000	23	30	50	1.5 to 80(3)	1.5 to 80	40	2.5	60	500(3)	50	40	kHz
TRANSIENT RESPONSE														
Rise Time (1)	45	30(3)	60(3)	40(3)	(2)	200 to 2,000(3)	200 to 2,000(3)	200(3)	75(3)	50(3)	20(3)	(2)	200(3)	ns
Overshoot (1)	(2)	25(3)	15(3)	15(3)	(2)	5 to 15(3)	5 to 15(3)	20(3)	25(3)	30(3)	25(3)	(2)	20(3)	%
Slew Rate (1)	±20	200	5(3)	2	±10	.1 to .8(3)	.1 to.8	2.5(3)	±1.6(3)	±4.0(3)	50	10	2.5(3)	V/μs
Settling Time (Typ.)(1)	0.30	.5(3)	1.5(3)	1.5(3)	5.0	(2)	(2)	(2)	12(3)	4.2(3)	1.5(3)	5.0	(2)	μs
POWER SUPPLY CHARACTERISTICS														
Supply Current (1)	4.0	23	4.5	4	0.150	.02 to .2	.02 to .2	5	7.0	6.5	6.0(1)	0.150	5	mA
Power Supply Rejection Ratio	74	66	74	74	80	76	76	120	80	80	80	86	130	dB
FUNCTIONAL CHARACTERISTICS														
Offset Adjust	Yes	No	Yes	DIP Pkg. Only	Yes	Yes	Yes	No	No	No	No	Yes	No	
Compensation Components	0(AV≥5)	0	0	0	0	0	0	3	0	0	0AV>10	0	3	
Output Protection	Yes	External	Yes	Yes	Yes	Yes	Yes	Yes	Yes(6)	Yes(6)	Yes	Yes	Yes	

(1) At +25°C
(2) Not applicable or not specified
(3) Typical
(4) V_{SUPPLY} = ±40V
(5) Dependent upon I_{SET} value

* TO-86 only † Guaranteed for ±15V supplies and applicable temperature range unless otherwise specified.

Comparators Selection Guide

PARAMETER†	-55°C to +125°C HA-4900	0°C to +75°C HA-4905	UNITS
Offset Voltage	4	10	mV
Bias Current	150	300	nA
Offset Current	35	70	nA
Response Time (TYP)	130	130	ns
Output Current (+25°C)	3.5	3.5	mA
Supply Current (1) I_{ps}(+)	12	13	mA
I_{ps} (-)	6	7	mA
I_{ps} (Logic)	2	2.5	mA

† Guaranteed for Applicable Temperature range, unless otherwise specified.

(1) At +25°C

PRAM PROGRAMMABLE AMPLIFIER HA-2400/2404/2405

One of four op amp input stages may be digitally selected to be connected to a single output. Replaces 5 op amps and a four channel multiplexer to obtain programmable gain, signal selection or countless other functions.

CURRENT BOOSTER AMPLIFIER HA-2630/2635

A unity gain amplifier with output current up to ±400mA, and 600V/μ s slew rate, designed for use in series with any op amp output. For Coax line drivers, servo amps, audio amps, clock drivers etc.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-909/911

Wideband, Low Noise, Operational Amplifiers

FEATURES

- LOW BROADBAND NOISE — 1μV R.M.S.
- LOW NOISE VOLTAGE — $7nV/\sqrt{Hz}$
- LOW OFFSET VOLTAGE — 2mV
- WIDE BANDWIDTH — 7MHz
- POWER BANDWIDTH — 20kHz
- SUPPLY RANGE — ±5V TO ±20V
- INTERNALLY COMPENSATED

APPLICATIONS

- HIGH Q, WIDEBAND FILTERS
- AUDIO AMPLIFIERS
- SIGNAL GENERATORS

DESCRIPTION

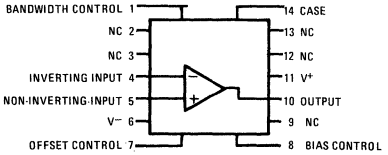
HA-909 and HA-911 are monolithic ampliifers delivering very low noise and excellent bandwidth specifications without the need for external compensation. Additional features of these dielectrically isolated devices include low offset voltage, offset trim capabitlity (14-pin flat package only), and high output current drive capabitlity.

With 7MHz bandwidth and internal compensation these amplifiers are extremely useful in many active filter designs. In audio circuitry requiring quiet operation these devices offer 1 μ V typical broadband noise (10Hz to 1kHz) and 20kHz power bandwidth. 2mV typical offset voltage, offset trim capability, and 20mA output current drive capability (±10.0V swing) make these amplifiers useful in signal conditioning circuits.

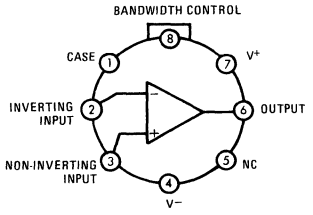
HA-909 and HA-911 are available in metal can (TO-99) and 14-pin flat packages. HA-909 is specified over the -55°C to +125°C range. HA-911 is specified from 0°C to +75°C.

PINOUT

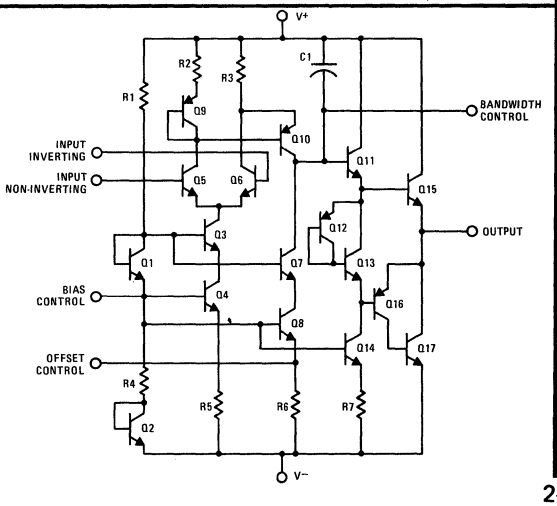
TO-86 — TOP VIEW — **Package Code 9V**



TO-99 — TOP VIEW — **Package Code 2A**



SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals		50.0V
Differential Input Voltage		±7.0V
Peak Output Current		±50mA
Internal Power Dissipation (Note 10)		300mW
Operating Temperature Range –	HA-909	$-55^oC \leq T_A \leq +125^oC$
	HA-911	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: V_{Supply} = ±15.0V unless otherwise specified.

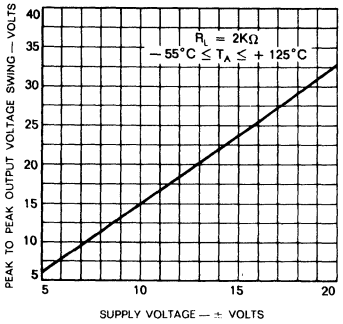
PARAMETER	TEMP.	HA-909 -55°C to +125°C MIN.	HA-909 TYP.	HA-909 MAX.	HA-911 0°C to +75°C MIN.	HA-911 TYP.	HA-911 MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2.0	5.0		2.0	6.0	mV
	Full			6.0			7.5	mV
Equivalent Input Noise (Note 9)	+25°C		1.0	5.0		1.0		μV
Input Noise Voltage	+25°C		7			7		$nV/\sqrt{Hz}$
* Bias Current	+25°C		87	300		200	500	nA
	Full			750		300	750	nA
* Offset Current	+25°C		25	150		100	300	nA
	Full		50	300		150	450	nA
Offset Current Average Drift	Full		1.0			1.0		nA/°C
Input Resistance	+25°C	200	600		100	250		KΩ
	Full	100	300					KΩ
Common Mode Range	Full	+12.0			+12.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Notes 1, 4)	+25°C	25K	45K		20K	45K		V/V
	Full	25K	45K		15K	45K		V/V
Full Power BW	+25°C		20			20		KHz
* Common Mode Rejection Ratio (Note 2)	Full	80	96		74	90		dB
Unity Gain Bandwidth (Note 3)	+25°C		7			7		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	+12.0			+11.0			V
* Output Current (Note 4)	+25°C	+20			+15			mA
Output Resistance	+25°C		150			500		Ohms
TRANSIENT RESPONSE								
Rise Time (Notes 1, 5, 6 & 8)	+25°C		40	75		40	75	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		15	40		15	40	%
* Slew Rate (Notes 1, 5 & 8)	+25°C	+3.5	+5.0			+5.0		V/μs
		-1.2	-2.0			-2.0		
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		1.8	2.5		1.8	2.5	mA
* Power Supply Rejection Ratio (Note 7)	Full	80	92		74	90		dB

NOTES:
1. R_L = 2KΩ
2. V_{CM} = ±5.0V
3. V_O < 90mV
4. V_O = ±10.0V
5. C_L = 100pF
6. V_O = ±200mV
7. V_{Sup} = ±9.0V to ±15.0V
8. See Transient Response test circuits and waveforms – page 3.
9. 10 – 1000Hz, R_S = 10K
10. Derate by 6.6mW/°C above 105°C

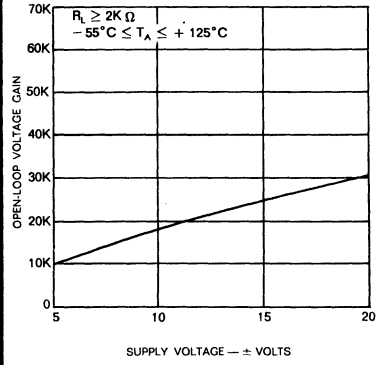
*100% Tested For DASH 8

GUARANTEED ELECTRICAL CHARACTERISTICS

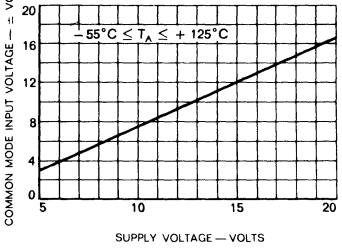
OUTPUT VOLTAGE SWING VS. SUPPLY VOLTAGE



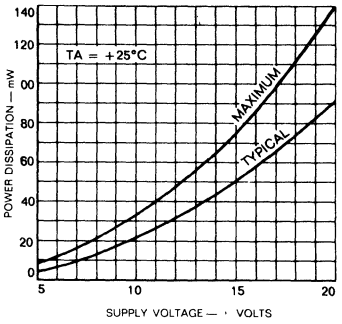
OPEN LOOP VOLTAGE GAIN VS. SUPPLY VOLTAGE



COMMON MODE INPUT VOLTAGE VS. SUPPLY VOLTAGE

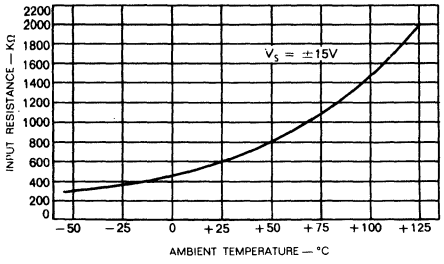


POWER DISSIPATION VS. SUPPLY VOLTAGE

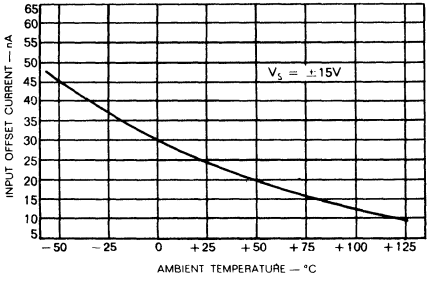


TYPICAL PERFORMANCE CURVES

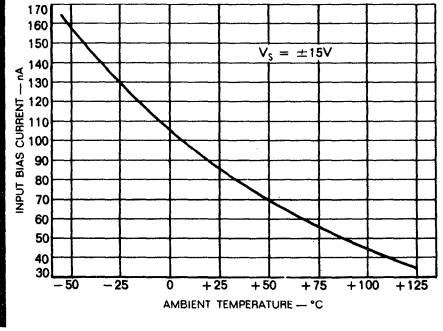
INPUT RESISTANCE VS. AMBIENT TEMPERATURE



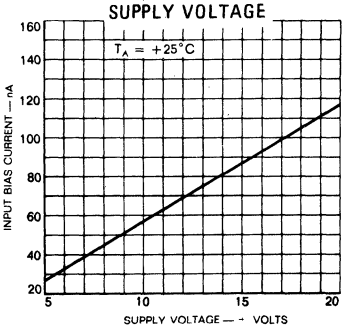
INPUT OFFSET CURRENT VS. AMBIENT TEMPERATURE



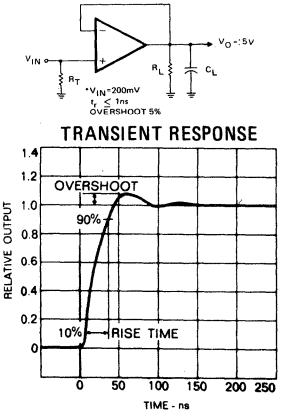
INPUT BIAS CURRENT VS. AMBIENT TEMPERATURE



INPUT BIAS CURRENT VS. SUPPLY VOLTAGE

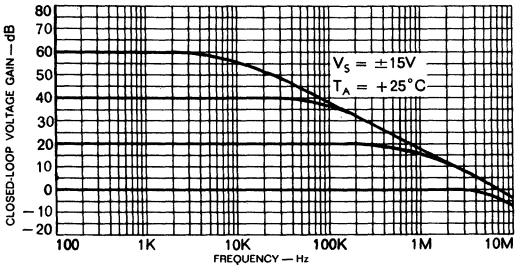


TRANSIENT RESPONSE

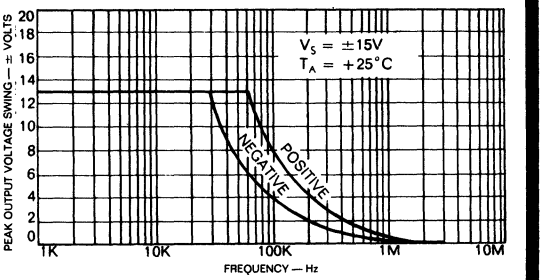


TYPICAL PERFORMANCE CURVES(continued)

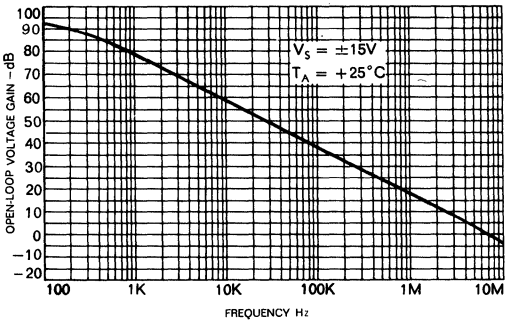
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



OUTPUT VOLTAGE SWING VS. FREQUENCY



OPEN LOOP FREQUENCY RESPONSE



DEFINITIONS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT – The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE – The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE – The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO – The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING – The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE – The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE – The ratio of the change in output voltage to the change in output current.

POSITIVE OUTPUT VOLTAGE SWING – The peak positive output voltage swing, referred to ground, that can be obtained without clipping.

NEGATIVE OUTPUT VOLTAGE SWING – The peak negative output voltage swing, referred to ground, that can be obtained without clipping.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in input voltage producing it.

BANDWIDTH – The frequency at which the voltage gain is 3dB below its low frequency value.

UNITY GAIN BANDWIDTH – The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO – The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE – The closed loop step function response of the amplifier under small signal conditions.

PHASE MARGIN – $(180^o - (\phi_1 - \phi_2))$ where ϕ_1 is the phase shift at the frequency where the absolute magnitude of gain is unity ϕ_2 is the phase shift at a frequency much lower than the open loop bandwidth.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2050/2055/2050A/2055A

High Slew Rate F.E.T. Input Operational Amplifiers

FEATURES

- HIGH SLEW RATE — 120V/μs
- FAST SETTLING — 400ns
- WIDE POWER BANDWIDTH — 2MHz
- HIGH GAIN BANDWIDTH — 20MHz
- HIGH INPUT IMPEDANCE — 10^{12} OHMS
- LOW BIAS CURRENT — 1pA
- TRUE OP AMP – CAN BE OPERATED INVERTING OR NON-INVERTING

APPLICATIONS

- DATA ACQUISITION
- SIGNAL CONDITIONING
- R.F. AND VIDEO AMPLIFICATION

DESCRIPTION

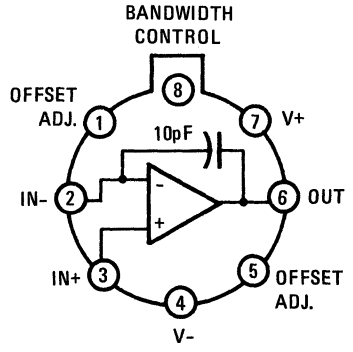
The HA-2050/2055 is an operational amplifier combining the advantages of very high slew rate and wide bandwidth with ultra-low input current and high input resistance. These devices are ideal for use in sample-and-hold circuits, A/D, D/A and sampled data systems; and for use in wide band R.F. or video systems where wide bandwidth at high output levels is required. The device may be operated inverting or noninverting; and external compensation is required only when operated at closed loop gains less than three. An internal feedback capacitor is provided to cancel phase shift in the feedback loop due to input capacitance.

The HA-2050 is guaranteed for operation from -55°C to +125°C and the HA-2055 is guaranteed from 0°C to +75°C.

PINOUT

TO-99
Top View

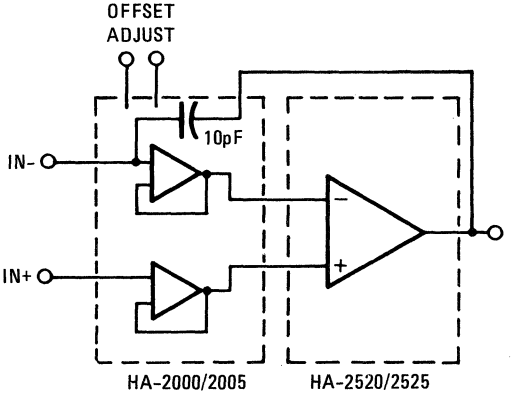
Package Code 2A



Case Connected to V+

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V– Terminals	35.0V	Internal Power Dissipation (Note 10)	300mW	
Differential Input Voltage	±15.0V	Operating Temp. Range	$-55^{o}C \leq T_A \leq +125^{o}C$	(HA-2050)
Output Current	50mA		$0^{o}C \leq T_A \leq +75^{o}C$	(HA-2055)
		Storage Temp. Range	$-65^{o}C \leq T_A \leq +150^{o}C$	

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{Supply} = ±15.0V unless otherwise specified.

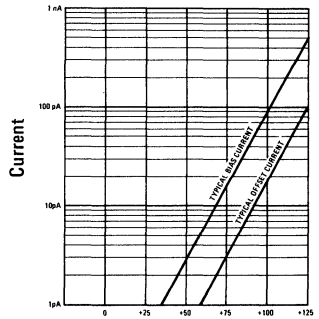
		HA-2050/HA-2050A -55°C to +125°C			HA-2055/HA-2055A 0°C to +75°C			
		LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage (Note 1)								
HA-2050 / HA-2055	+25°C		15	25		30	60	mV
	Full			30			65	mV
HA-2050A / HA-2055A	+25°C		7	14		7	14	mV
	Full			17			17	mV
Bias Current	+25°C		1	20		1	20	ρA
* (125°C)	Full		0.5	10		0.02	1	nA
Offset Current	+25°C		0.5	20		0.5	20	ρA
* (125°C)	Full		0.1	5		.005	0.5	nA
Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Capacitance	+25°C		5			5		ρF
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 2,5)	+25°C	7.5K	15K		7.5K	15K		V/V
	Full	5K			5K			V/V
* Common Mode Rejection Ratio (Note 3)	Full	74	90		70	90		dB
Gain Bandwidth Product (Note 4)	+25°C		20			20		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
* Output Current	+25°C	±10	±20		±10	±20		mA
Full Power Bandwidth (Note 5)	+25°C		2,000			2,000		kHz
TRANSIENT RESPONSE (NOTES 2, 8, 9)								
Rise Time (Note 6)	+25°C		50			50		ns
Overshoot (Note 6)	+25°C		25			25		%
Slew Rate (Note 5)	+25°C		120			120		V/μs
Settling Time	+25°C		0.4			0.4		μs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		6.0	8.0		6.0	8.0	mA
* Power Supply Rejection Ratio (Note 7)	Full	74	90		70	90		dB

NOTES:
1. Adjustable to zero with 100KΩ pot between pins 1 and 5; wiper to V+.
2. R_L = 2K
3. V_{CM} = ±5.0V
4. $A_V > 10$
5. V_O = ±10V
6. V_O = ±200mV
7. ΔV = ±5.0V
8. C_L = 50pF
9. A_V = +3, See transient response test circuit and wave forms, page 4.
10. Derate by 6.6mW/°C above 105°C

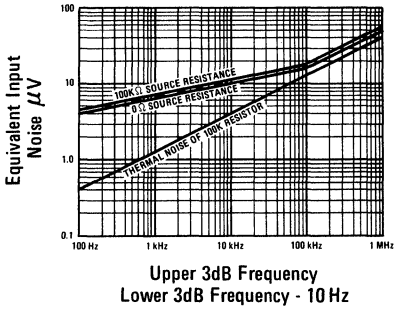
*100% Tested for DASH 8

V+ = 15 VDC, V- = 15 VDC, T_A = 25°C UNLESS OTHERWISE STATED.

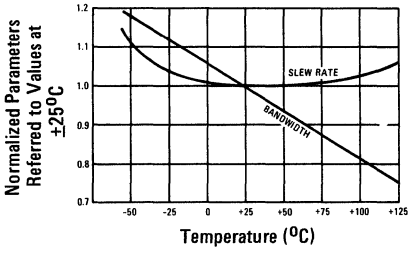
INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



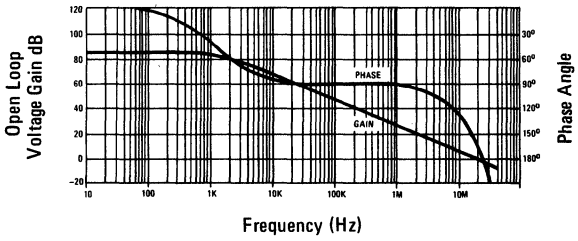
EQUIVALENT INPUT NOISE VS. BANDWIDTH



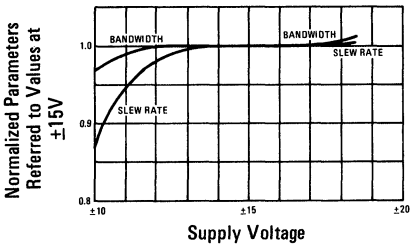
NORMALIZED AC PARAMETERS VS. TEMPERATURE



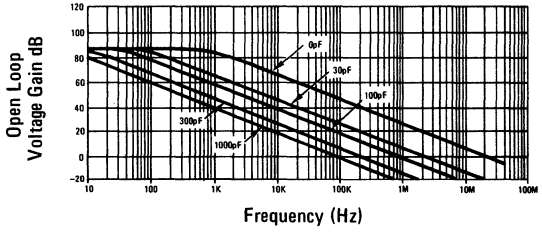
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



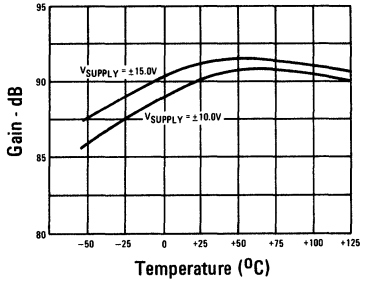
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE AT +25°C



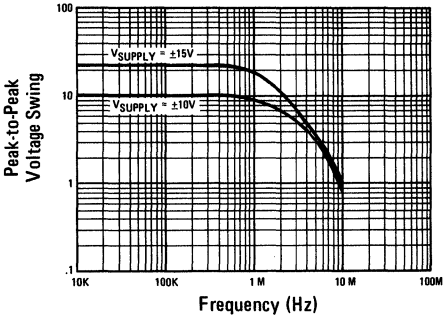
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

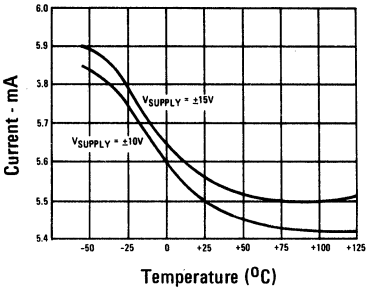


OUTPUT VOLTAGE SWING VS. FREQUENCY AT +25°C

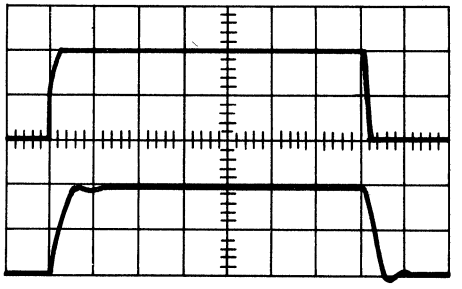


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT
VS. TEMPERATURE

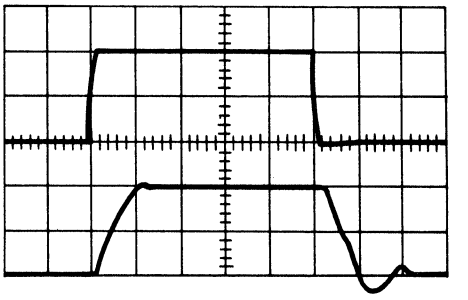


TRANSIENT RESPONSE; A_V = +3



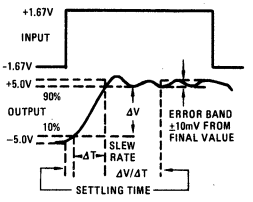
R_L = 2K Ohms, C_L = 50pF
Upper Trace: Input; 33mV/Div.
Lower Trace: Output; 100mV/Div.
Horizontal = 100ns/Div.
T_A = +25°C, V_S = ±15V

SLEWING WAVEFORM

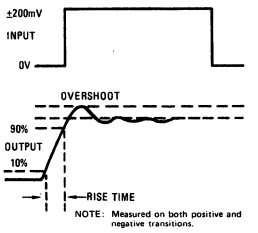


Horizontal Scale: 100ns/Div.
Upper Trace: Input; 1.67V/Div.
Lower Trace: Output; 5.0V/Div.
Gain = +3, R_L = 2K Ohms, C_L = 50pF

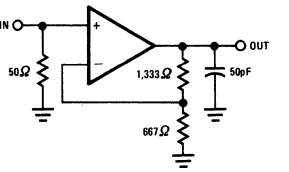
SLEW RATE AND
SETTLING TIME



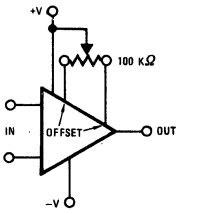
TRANSIENT
RESPONSE



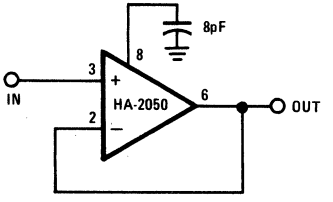
SLEW RATE AND
TRANSIENT RESPONSE



SUGGESTED
OFFSET ZERO
ADJUST HOOK-UP



TYPICAL APPLICATIONS



COMPENSATION CIRCUIT FOR UNITY GAIN

Slew Rate ≈ 40V/μs

Bandwidth ≈ 8 MHz

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2060/2065/ 2060A/2065A

Wide Band F.E.T. Input Operational Amplifier

FEATURES

- GAIN BANDWIDTH PRODUCT 100MHz
- HIGH INPUT IMPEDANCE 10^{12} OHMS
- LOW BIAS CURRENT 1pA
- HIGH SLEW RATE 35V/μs
- WIDE POWER BANDWIDTH 600kHz
- TRUE OP AMP – CAN BE OPERATED INVERTING OR NON-INVERTING

APPLICATIONS

- SIGNAL CONDITIONING
- ACTIVE FILTERS
- SIGNAL GENERATORS

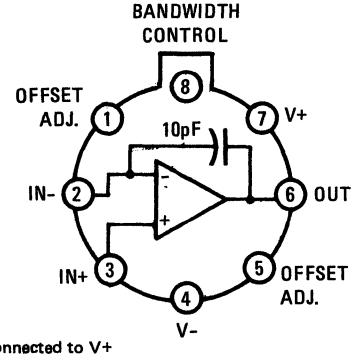
DESCRIPTION

The HA-2060/2065 is an operational amplifier combining the advantages of very wide bandwidth and high slew rate with ultra-low input current and high input resistance. These devices are ideal for use in sample-and-hold circuits, active filters, wide band amplifiers, high gain amplifiers with superior bandwidth, and wherever very low closed loop gain and phase shift errors are required. The device may be operated inverting or noninverting; and external compensation is required only when operating at closed loop gains less than five. An internal feedback capacitor is provided to cancel phase shift in the feedback loop due to input capacitance.

The HA-2060 is guaranteed for operation from -55°C to +125°C and the HA-2065 is guaranteed from 0°C to +75°C.

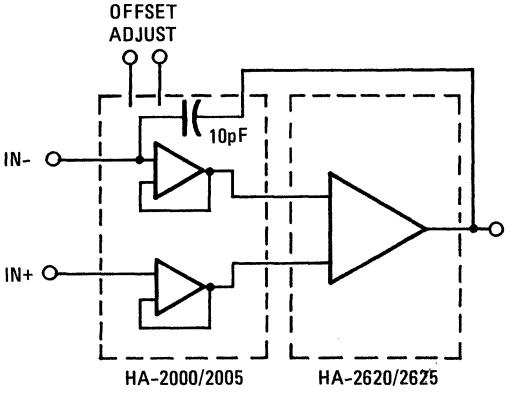
PINOUT

TO-99 Top View Package Code 2A



Case Connected to V+

FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	35.0V	Internal Power Dissipation (Note 10)	300mW
Differential Input Voltage	±12V	Operating Temp. Range	$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2060)
Output Current / Full Short Circuit Protection			$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2065)
		Storage Temp. Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

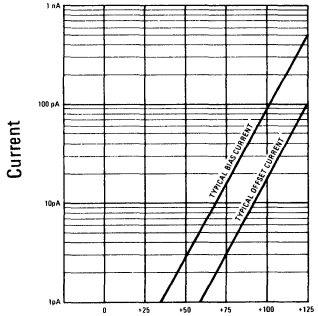
PARAMETER	TEMP.	HA-2060/HA-2060A -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2065/HA-2065A 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage (Note 1)								
HA-2060 / HA-2065	+25°C		15	25		15	60	mV
	Full			30			65	mV
HA-2060A / HA-2065A	+25°C		7	12		7	12	mV
	Full			15			15	mV
Bias Current	+25°C		1	20		1	20	ρA
* (125°C)	Full		0.5	10		0.02	1	nA
Offset Current	+25°C		0.5	20		0.5	20	ρA
* (125°C)	Full		0.1	5		.005	.5	nA
Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Capacitance	+25°C		5			5		ρF
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 2 5)	+25°C	80K	150K		80K	150K		V/V
	Full	60K			70K			V/V
* Common Mode Rejection Ratio (Note 3)	Full	74	90		70	90		dB
Gain Bandwidth Product (Note 4)	+25°C		100			100		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
* Output Current	+25°C	±10	±18		±10	±18		mA
Full Power Bandwidth (Note 5)	+25°C		600			600		kHz
TRANSIENT RESPONSE (NOTES 2, 8, 9)								
Rise Time (Note 6)	+25°C		50			50		ns
Overshoot (Note 6)	+25°C		25			25		%
Slew Rate (Note 5)	+25°C		35			35		V/μs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		4.0	6.0		4.0	6.0	mA
* Power Supply Rejection Ratio (Note 7)	Full	74	90		70	90		dB

NOTES:
1. Adjustable to zero with 100KΩ pot between pins 1 and 5; wiper to V+.
2. $R_L = 2K$
3. $V_{CM} = \pm 5.0V$
4. $A_V > 10$
5. $V_O = \pm 10V$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. $C_L = 50\rho F$
9. $A_V = +5$, See transient response test circuits and waveforms, page 4.
10. Derate by 6.6mW/°C above 105°C

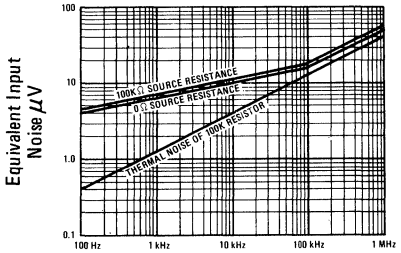
*100% Tested for DASH 8

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

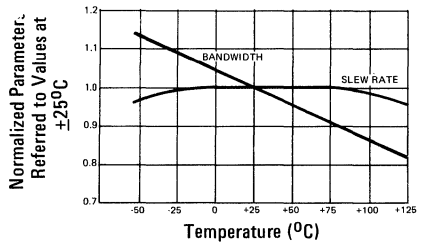
INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



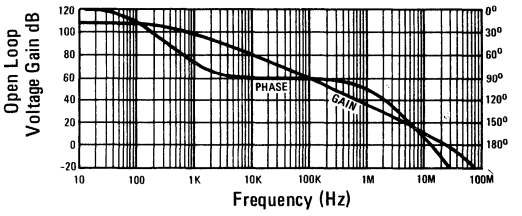
EQUIVALENT INPUT NOISE VS. BANDWIDTH



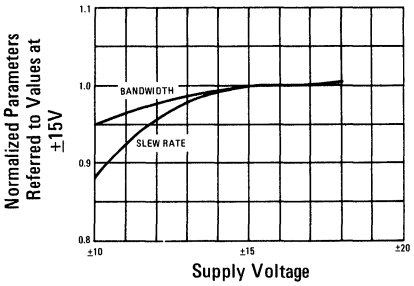
NORMALIZED AC PARAMETERS VS. TEMPERATURE



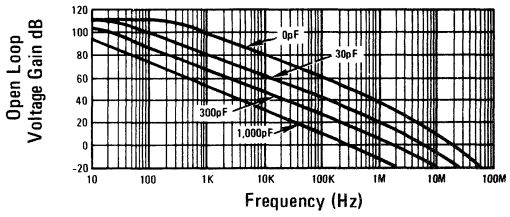
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



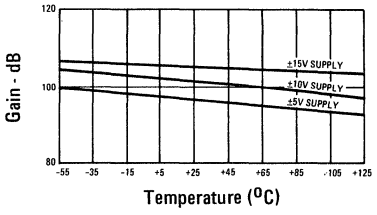
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE AT +25°C



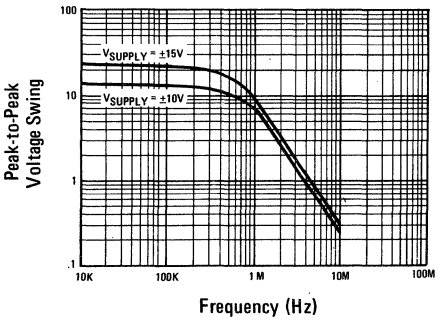
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE



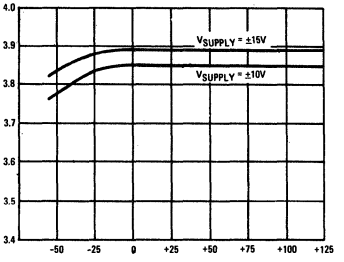
OUTPUT VOLTAGE SWING VS. FREQUENCY AT +25°C



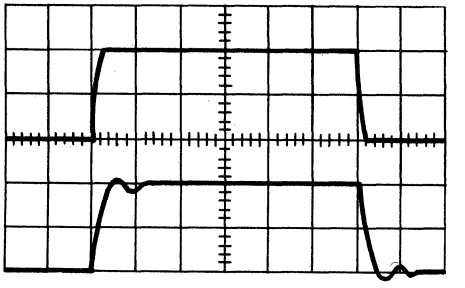
2

PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT VS. TEMPERATURE

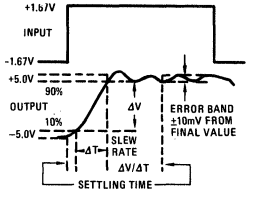


TRANSIENT RESPONSE; A_V = +5

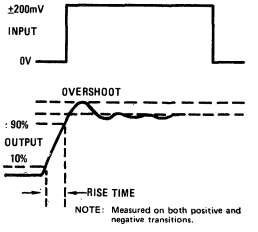


R_L = 2K Ohms, C_L = 50pF
Upper Trace: Input; 20mV/Div.
Lower Trace: Output; 100mV/Div.
Horizontal = 100ns/Div.
T_A = +25°C, V_S = ±15V

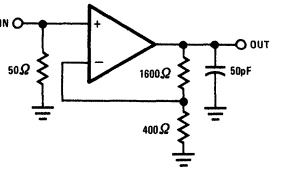
SLEW RATE AND SETTLING TIME



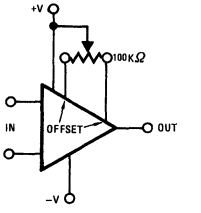
TRANSIENT RESPONSE



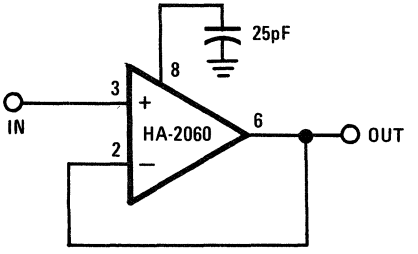
SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



TYPICAL APPLICATIONS



COMPENSATION CIRCUIT FOR UNITY GAIN

SLEW RATE ≈ 5 V/μs

BANDWIDTH ≈ 10 MHz

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2400/2404/2405

PRAM™ Four Channel Programmable Amplifier

FEATURES

- PROGRAMMABILITY
- HIGH SLEW RATE 30V/μs
- WIDE GAIN BANDWIDTH 40MHz
- HIGH GAIN 150,000
- LOW OFFSET CURRENT 5nA
- HIGH INPUT IMPEDANCE 30MΩ
- SINGLE CAPACITOR COMPENSATION
- DTL/TTL COMPATIBLE INPUTS

APPLICATIONS

- THOUSANDS OF NEW APPLICATIONS; PROGRAM
  - SIGNAL SELECTION/MULTIPLEXING
  - OP AMP GAIN
  - OSCILLATOR FREQUENCY
  - FILTER CHARACTERISTICS
  - ADD-SUBTRACT FUNCTIONS
  - INTEGRATOR CHARACTERISTICS
  - COMPARATOR LEVELS

DESCRIPTION

HA-2400/2404/2405 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

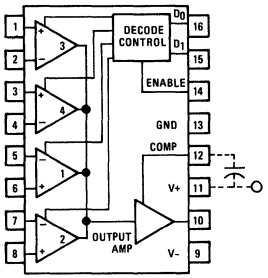
Each channel of the HA-2400/2404/2405 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing, signal selection, and mathematical function designs. With 30V/μs slew rate, 40MHz gain bandwidth, and 30M ohms input impedance these devices are ideal building blocks for signal generators, active filters, and data acquisition designs. Programmability coupled with 2mV typical offset voltage and 5nA offset current makes these amplifiers outstanding components for signal conditioning circuits.

HA-2400/2404/2405 are available in a 16 pin dual-in-line package. HA-2400 is specified from -55°C to +125°C. HA-2404 is specified over the -25°C to +85°C range, while HA-2405 operates from 0°C to +75°C.

PINOUT

(TOP VIEW)

Package Code 4B



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

SCHEMATIC

Condensed circuit diagram for a programmable amplifier (PRAM HA-2400)

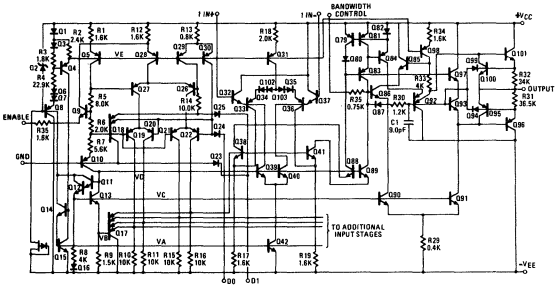


Diagram includes: ONE INPUT STAGE, DECODE CONTROL, BIAS NETWORK AND OUTPUT STAGE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V– Terminals	45.0V	Internal Power Dissipation (Note 13)	300mW
Differential Input Voltage	$\pm V_{Supply}$	Operating Temperature Range	$-55^oC \leq T_A \leq +125^oC$ (HA-2400)
Digital Input Voltage	–0.76V to +10.0V		$-25^oC \leq T_A \leq +85^oC$ (HA-2404)
Output Current	Short Circuit Protected		$0^oC \leq T_A \leq +75^oC$ (HA-2405)
		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

Digital inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$
Limits apply to each of the four channels, when addressed.

PARAMETER	TEMP.	HA-2400/HA-2404 LIMITS MIN.	TYP.	MAX.	HA-2405 LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2	5		4	9	mV
	Full			7			11	mV
* Bias Current (Note 12)	+25°C		50	200		50	250	nA
	Full			400			500	nA
* Offset Current (Note 12)	+25°C		5	50		5	50	nA
	Full			100			100	nA
Input Resistance (Note 12)	+25°C		30			30		MΩ
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 1,5)	+25°C	50K	150K		50K	150K		V/V
	Full	25K			25K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		dB
Gain Bandwidth (Note 3)	+25°C		40			40		MHz
(Note 4)	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current	+25°C		20			20		mA
Full Power Bandwidth (Notes 3, 5)	+25°C		500			500		kHz
(Notes 4,5)	+25°C		200			200		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	+25°C		20			20		ns
Overshoot (Notes 4,6)	+25°C		25			25		%
Slew Rate (Notes 3,7)	+25°C		30			30		V/μs
(Notes 4,7)	+25°C		8			8		V/μs
Settling Time (Notes 4, 7, 8)	+25°C		1.5			1.5		μs
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current (V_{IN} = 0V)	Full		1			1		mA
Digital Input Current (V_{IN} = +5.0V)	Full		5			5		nA
Output Delay (Note 9)	+25°C		100			100		ns
Crosstalk (Note 10)	+25°C	-80	-110		-74	-110		dB
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		4.8	6.0		4.8	6.0	mA
* Power Supply Rejection Ratio (Note 11)	Full	74	90		74	90		dB

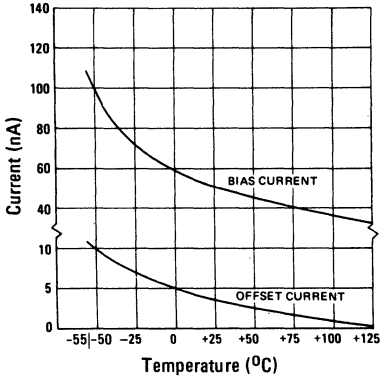
NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 5$ V.D.C.
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2K\Omega$, $C_L = 50pF$
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2K\Omega$, $C_L = 50pF$
5. $V_{OUT} = 20V$ peak-to-peak
6. $V_{OUT} = 400$ mV peak-to-peak
7. $V_{OUT} = 10.0V$ peak-to-peak
8. To 0.1% of final value
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10$ V.D.C.
11. $V_{SUPP} = \pm 10V$.D.C. to $\pm 20V$.D.C.
12. Unselected channels have approximately the same input parameters.
13. Derate by 4.3mW/°C above 105°C

*100% Tested For DASH 8

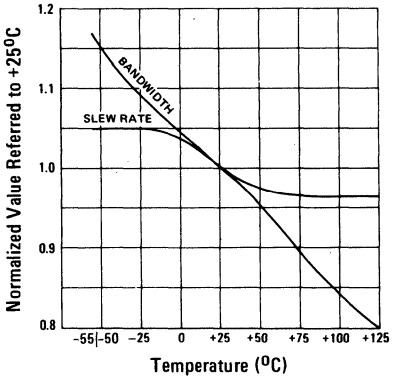
CHARACTERISTIC CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.

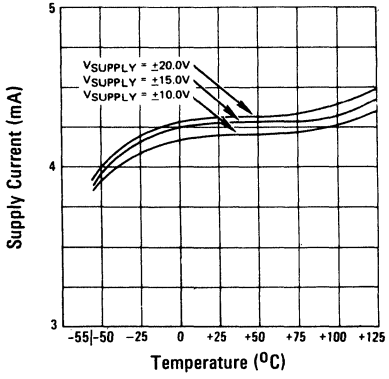
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



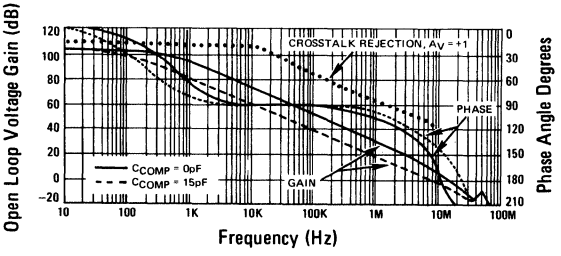
NORMALIZED A.C. PARAMETERS VS. TEMPERATURE



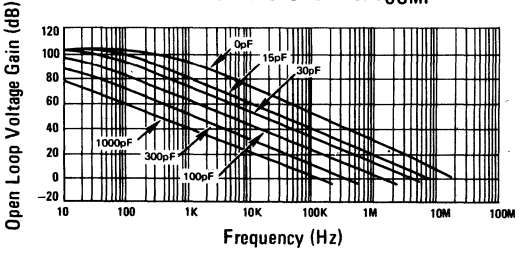
POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



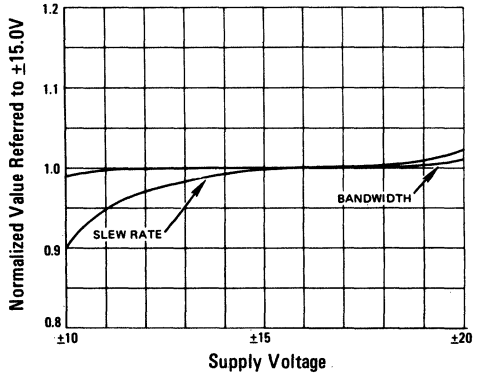
OPEN LOOP FREQUENCY AND PHASE RESPONSE



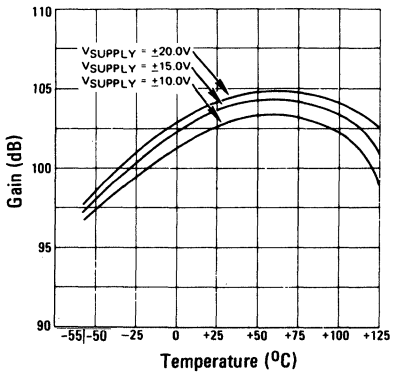
FREQUENCY RESPONSE VS. C_{COMP}



NORMALIZED A.C. PARAMETERS VS. SUPPLY VOLTAGE

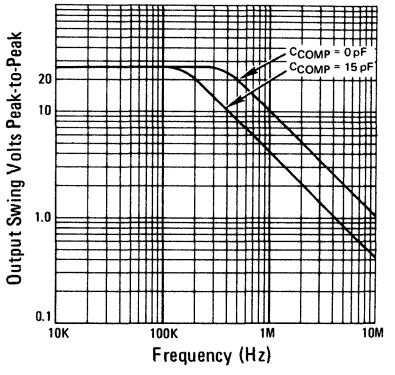


OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

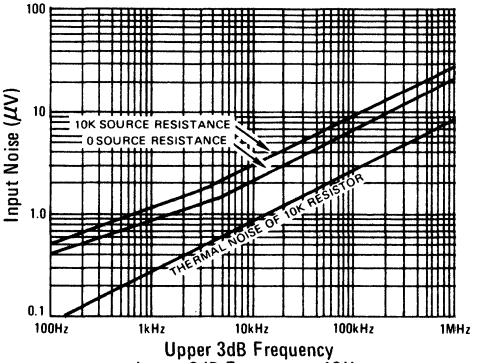


CHARACTERISTIC CURVES (continued)

OUTPUT VOLTAGE SWING VS. FREQUENCY

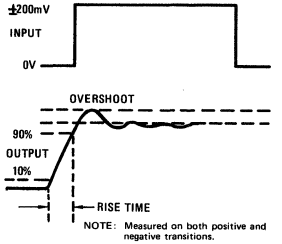


EQUIVALENT INPUT NOISE VS. BANDWIDTH

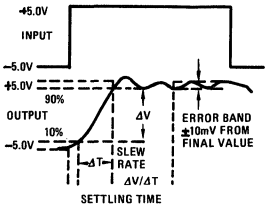


Upper 3dB Frequency
Lower 3dB Frequency - 10Hz
Broadband Noise Characteristics

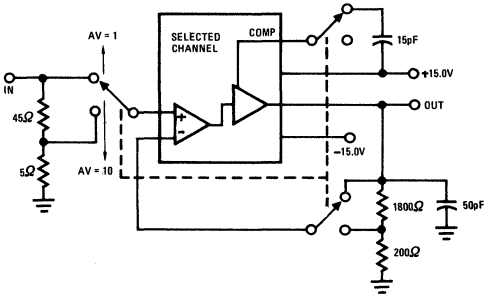
TRANSIENT RESPONSE



SLEW RATE AND SETTLING

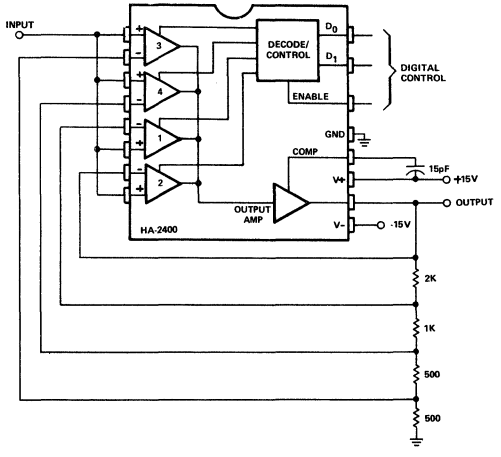


SLEW RATE AND TRANSIENT RESPONSE

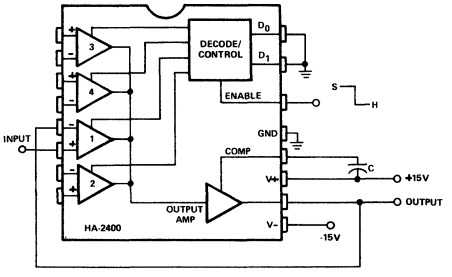


TYPICAL APPLICATIONS

AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN



SAMPLE AND HOLD



Sample charging rate = $\frac{I_1}{C}$ V/sec.

Hold drift rate = $\frac{I_2}{C}$ V/sec.

Switch pedistal error = $\frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$ A
$I_2 \approx 200 \times 10^{-9}$ A @ +25°C
$\approx 600 \times 10^{-9}$ A @ -55°C
$\approx 100 \times 10^{-9}$ A @ +125°C
$Q \approx 2 \times 10^{-12}$ Coul.

FOR MORE EXAMPLES, SEE HARRIS APPLICATION NOTE 514

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2500/02/05

Precision High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE 30V/μS
- FAST SETTLING 330ns
- WIDE POWER BANDWIDTH 500kHz
- HIGH GAIN BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 100MΩ
- LOW OFFSET CURRENT 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISTION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

HA-2500/2502/2505 comprise a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Slew rate of ±25V/μs and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12 MHz bandwidth and 500kHz power bandwidth make these devices well suited to R.F. and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2500/2502/2505 are particularly useful components in signal conditioning designs.

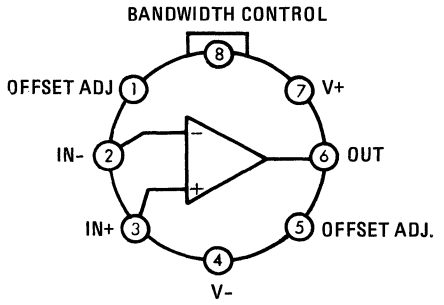
The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

HA-2500/2502/2505 are available in metal can (TO-99) packages. HA-2500 and HA-2502 are specified over the -55°C to +125°C range. HA-2505 is specified from 0°C to +75°C.

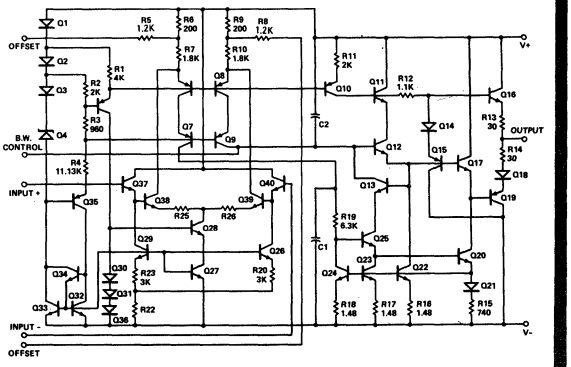
PINOUT

TO-99 **Package Code 2A**

Top View



SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range –	HA-2500/HA-2502	$-55^oC \leq T_A \leq +125^oC$
Differential Input Voltage	±15.0V		HA-2505	$0^oC \leq T_A \leq +75^oC$
Peak Output Current	50mA	Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$
Internal Power Dissipation	300mW			

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V- = -15V D.C.

PARAMETER	TEMP.	HA-2500 -55°C to +125°C LIMITS MIN.	HA-2500 TYP.	HA-2500 MAX.	HA-2502 -55°C to +125°C LIMITS MIN.	HA-2502 TYP.	HA-2502 MAX.	HA-2505 0°C to +75°C LIMITS MIN.	HA-2505 TYP.	HA-2505 MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		2	5		4	8		4	8	mV
	Full			8			10			10	mV
Offset Voltage Average Drift	Full		20			20			20		µV/°C
* Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
* Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance	+25°C	25	50		20	50		20	50		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C	20K	30K		15K	25K		15K	25K		V/V
	Full	15K			10K			10K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	350	500		300	500		300	500		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1,4,5 & 8)	+25°C	±25	±30		±20	±30		±20	±30		V/µs
Settling Time to 0.1% (Notes 1,4,5 & 8)	+25°C		0.33			0.33			0.33		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

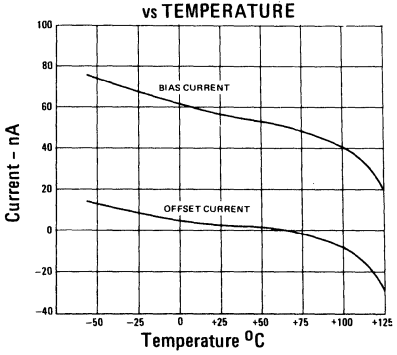
NOTES:
1. R_L = 2K
2. V_{CM} = ±5.0V
3. A_V >10
4. V_O = ±10.0V
5. C_L = 50pF
6. V_O = ±400mV
7. V_O = ±600mV
8. See transient response test circuits and waveforms page four.
9. ΔV = ±5.0V

100% Tested For DASH 8

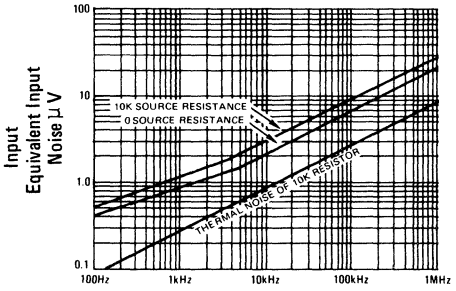
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

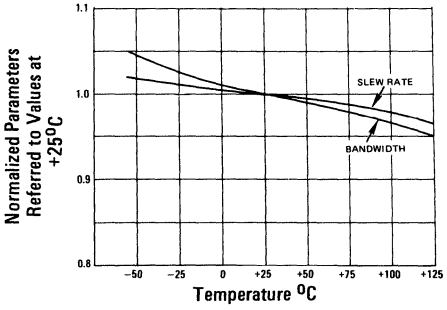
INPUT BIAS AND OFFSET CURRENT
vs TEMPERATURE



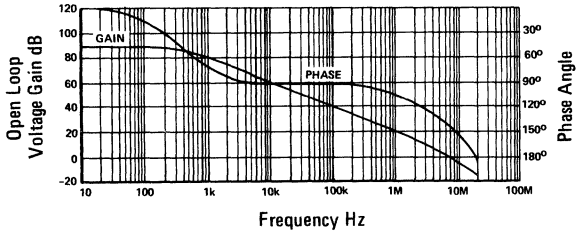
EQUIVALENT INPUT NOISE
vs BANDWIDTH



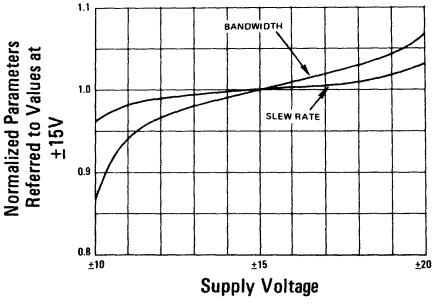
NORMALIZED AC PARAMETERS
vs TEMPERATURE



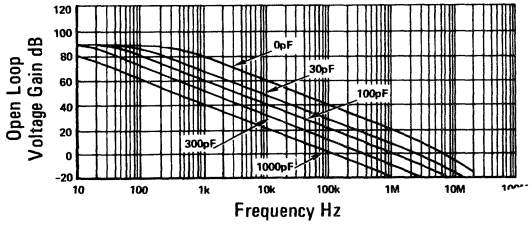
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS
vs SUPPLY VOLTAGE AT +25°C

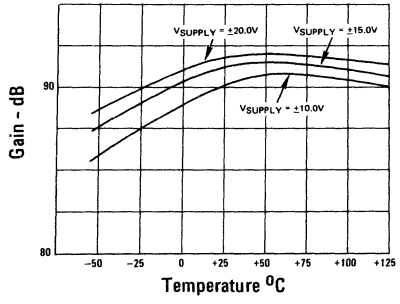


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

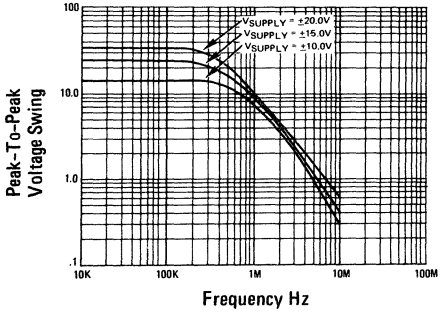


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN
vs TEMPERATURE

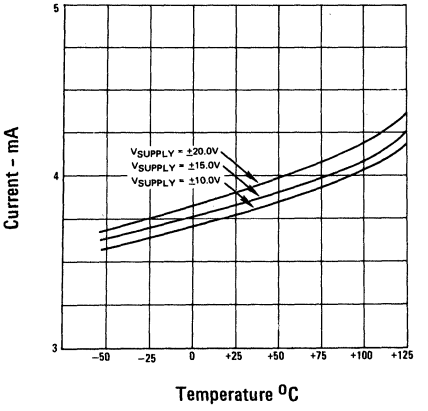


OUTPUT VOLTAGE SWING
vs FREQUENCY AT +25°C

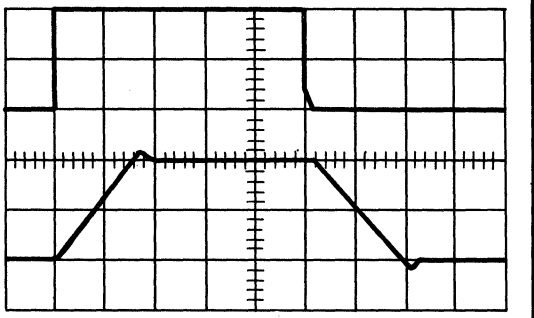


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT vs TEMPERATURE



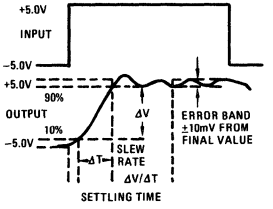
VOLTAGE FOLLOWER PULSE RESPONSE



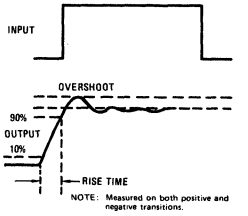
R_L = 2KΩ, C_L = 50pF
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 200ns/Div.
T_A = +25°C, V_S = ±15.0V

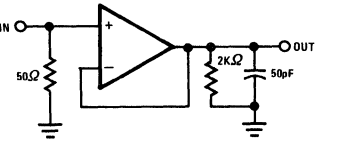
SLEW RATE AND SETTLING TIME



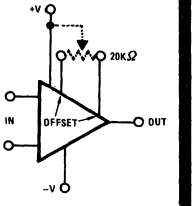
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED OFFSET ZERO ADJUST HOOK-UP



DEFINITIONS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT — The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE — The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE — The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

TRANSIENT RESPONSE — The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT — The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rating Limiting) — The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing) . . . restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

SETTLING TIME — Time required for output waveform to remain within 0.1 percent of final value.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2510/2512/2515

High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE — 60V/μs
- FAST SETTLING — 250ns
- WIDE POWER BANDWIDTH — 1,000kHz
- HIGH GAIN BANDWIDTH — 12MHz
- HIGH INPUT IMPEDANCE — 100MΩ
- LOW OFFSET CURRENT — 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

The HA-2510/2512/2515 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidth for internally compensated monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

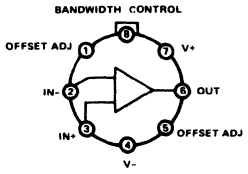
The $\pm$60V/ μs slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/2512/2515's superior 12MHz gain bandwidth and 1000kHz power bandwidth is extremely useful in R.F. and video applications. For accurate signal conditioning these amplifiers also provide 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

The HA-2510/2512 are available in metal can (TO-99) and 14-pin flat packages. HA-2510 and HA-2512 are specified from -55°C to +125°C. HA-2515 is specified over the 0°C to +75°C range, and is available in the TO-99 package.

PINOUT

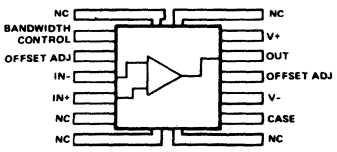
TO-99 TOP VIEW

Package Code 2A

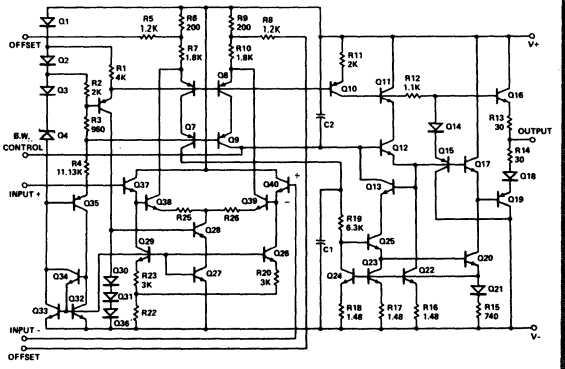


TO-86 TOP VIEW

Package Code 9V
(HA-2510/2512 Only)



SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2510/HA-2512	$-55^oC \leq T_A \leq +125^oC$		
HA-2515	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V– = 15V D.C.

PARAMETER	TEMP.	HA-2510 -55^oC to $+125^oC$ LIMITS			HA-2512 -55^oC to $+125^oC$ LIMITS			HA-2515 0^oC to $+75^oC$ LIMITS			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
* Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
* Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	750	1000		600	1000		600	1000		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±50	±65		±40	±60		±40	±60		V/µs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		0.25			0.25			0.25		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

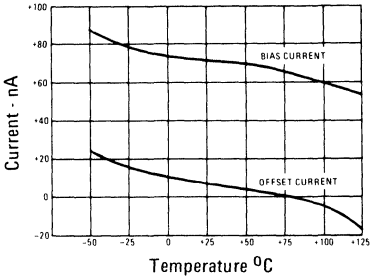
NOTES:
1. R_L = 2K
2. $V_{CM} = \pm 5.0V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. C_L = 50pF
6. $V_O = \pm 400mV$
7. $V_O = \pm 600mV$
8. See transient response test circuits and waveforms page four.
9. $\Delta V = \pm 5.0V$

*100% Tested For DASH 8

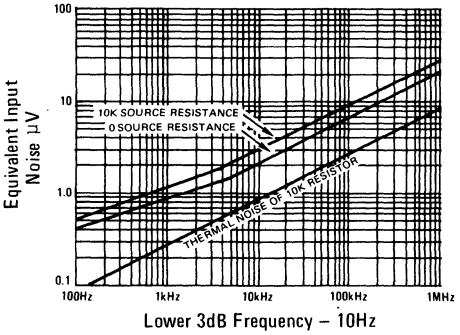
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.

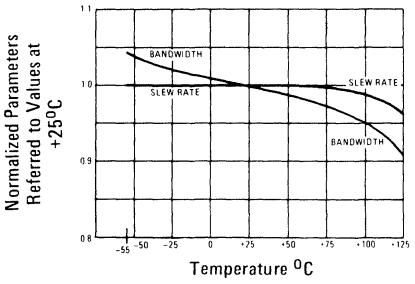
INPUT BIAS AND OFFSET CURRENT
vs TEMPERATURE



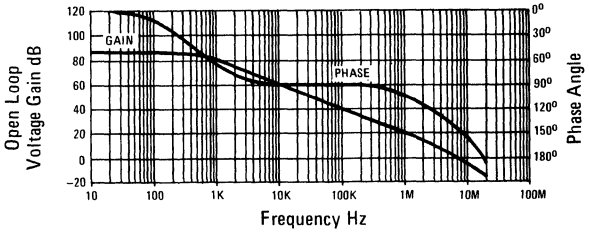
EQUIVALENT INPUT NOISE
vs BANDWIDTH



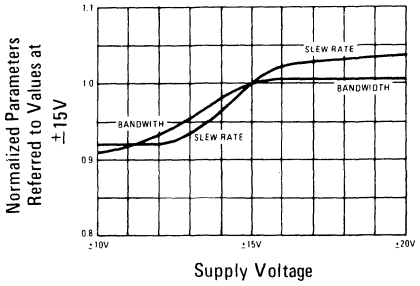
NORMALIZED AC PARAMETERS
vs TEMPERATURE



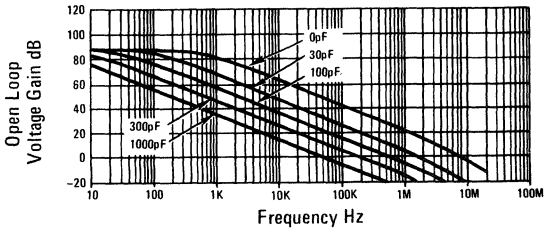
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS
vs SUPPLY VOLTAGE

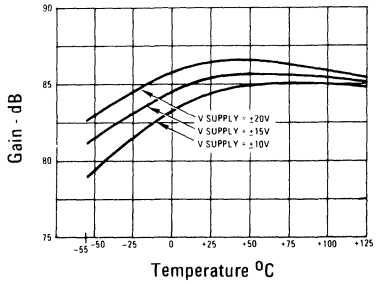


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

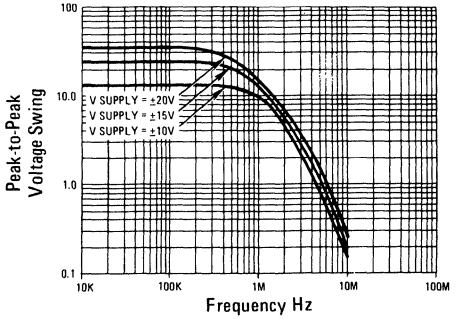


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN
vs TEMPERATURE



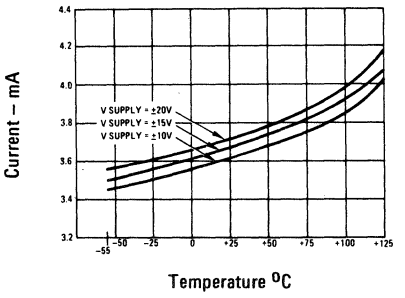
OUTPUT VOLTAGE SWING
vs FREQUENCY AT +25°C



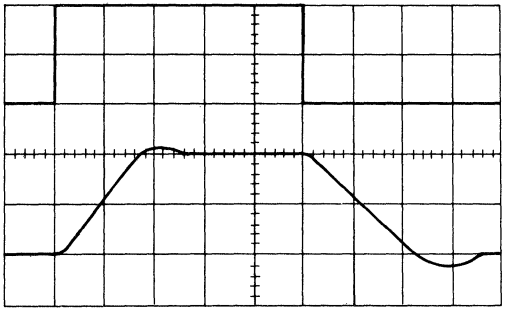
2

PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT
VS
TEMPERATURE



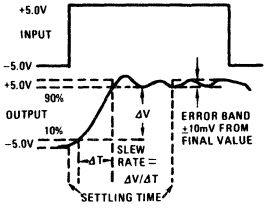
VOLTAGE FOLLOWER PULSE RESPONSE



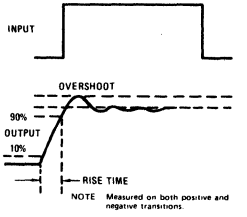
R_L = 2K Ω , C_L = 50pF
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 100n/Div.
T_A = +25°C, V_S = ±15.0V

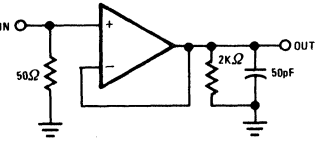
SLEW RATE AND
SETTLING TIME



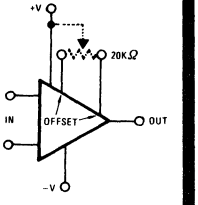
TRANSIENT RESPONSE



SLEW RATE AND
TRANSIENT RESPONSE



SUGGESTED
OFFSET ZERO
ADJUST HOOK-UP



DEFINITIONS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT – The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE – The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE – The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO – The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING – The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE – The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE – The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in input voltage producing it.

UNITY GAIN BANDWIDTH – The frequency at which the voltage gain of the amplifier is unity.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2520/22/25

Uncompensated High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE — 120V/μs
- FAST SETTLING — 200ns
- WIDE POWER BANDWIDTH — 2,000kHz
- HIGH GAIN BANDWIDTH — 20MHz
- HIGH INPUT IMPEDANCE — 100MΩ
- LOW OFFSET CURRENT — 10nA

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

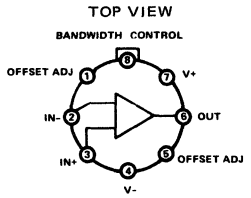
HA-2520/2522/2525 comprise a series of monolithic operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at closed loop gains greater than 3 without external compensation. In additon, these high performance components also provide low offset current and high input impedance.

120V/μs slew rate and 200ns (0.1%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for R.F. and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complimented by 10nA offset current, 100MΩ input impedance and offset trim capability.

The HA-2520/2522 are available in metal can (TO-99) and 14-pin flat packages. HA-2520 and HA-2522 are specified over -55°C to +125°C range. HA-2525 is specified from 0°C to +75°C, and is available in the TO-99 package.

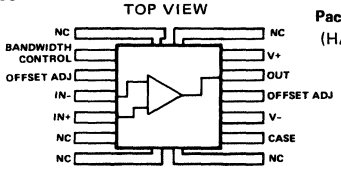
PINOUT

TO-99



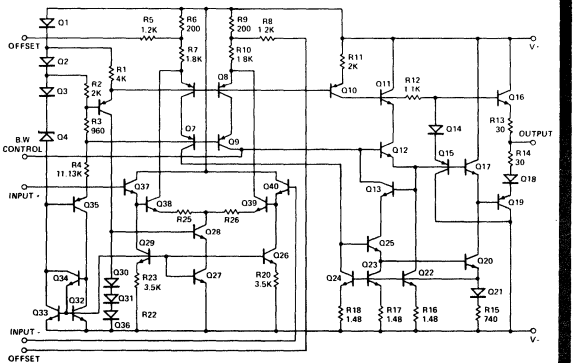
Package Code 2A

TO-86



Package Code 9V
(HA-2520/2522 Only)

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range			
HA-2520/2522	$-55^oC \leq T_A \leq +125^oC$	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2525	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

$V+ = +15V$ D.C., $V- = -15V$ D.C.

PARAMETER	TEMP.	HA-2520 -55^oC to $+125^oC$ LIMITS			HA-2522 -55^oC to $+125^oC$ LIMITS			HA-2525 0^oC to $+75^oC$ LIMITS			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
* Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
* Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		20			20			20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	1500	2000		1200	1600		1200	1600		kHz
TRANSIENT RESPONSE ($A_V = +3$)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±100	±120		±80	±120		±80	±120		V/µs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		0.20			0.20			0.20		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

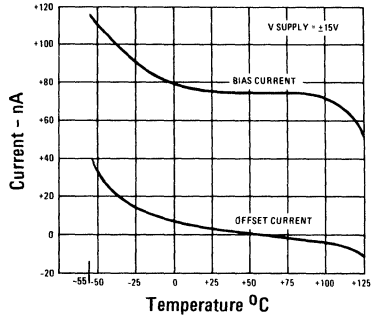
NOTES:
1. $R_L = 2K$
2. $V_{CM} = \pm 5.0V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. See transient response test circuits and waveforms page four.

*100% Tested For DASH 8

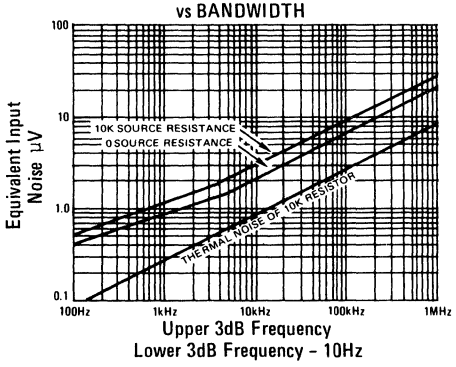
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

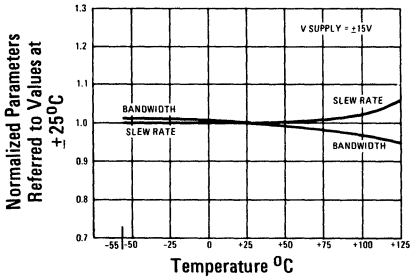
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



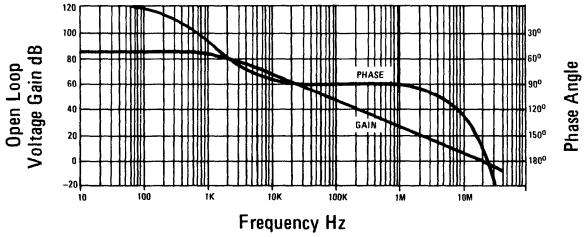
EQUIVALENT INPUT NOISE vs BANDWIDTH



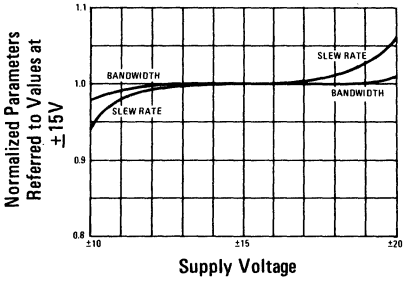
NORMALIZED AC PARAMETERS vs TEMPERATURE



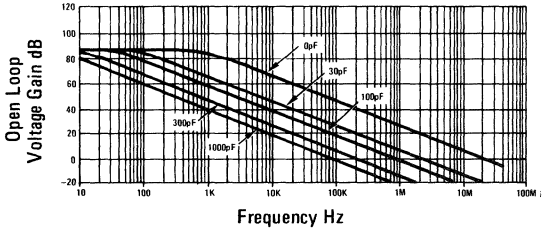
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



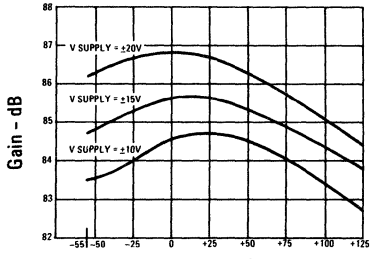
NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



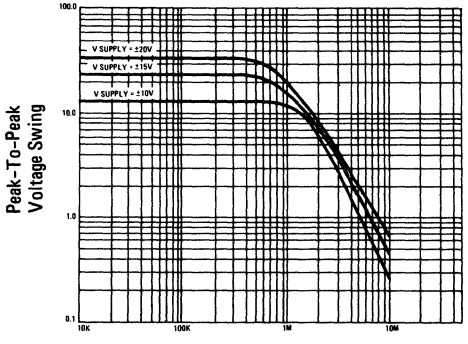
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



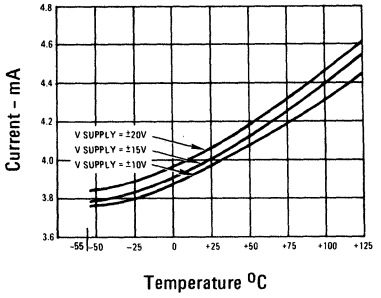
OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C



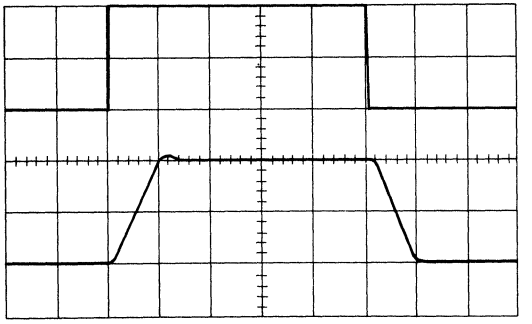
2

PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT vs TEMPERATURE



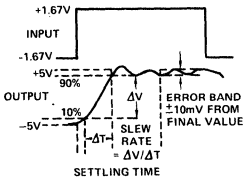
VOLTAGE FOLLOWER PULSE RESPONSE



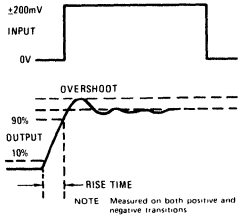
$R_L = 2K\Omega$, $C_L = 50pF$
Upper Trace: Input; 1.33V/Div.
Lower Trace: Output; 5V/Div.

Horizontal = 100ns/Div.
$T_A = +25^oC$, $V_S = \pm 15V$

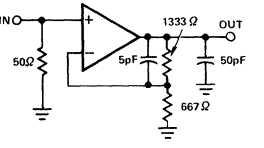
SLEW RATE AND SETTLING TIME



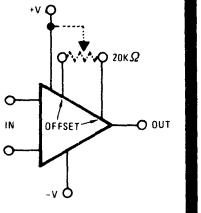
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE

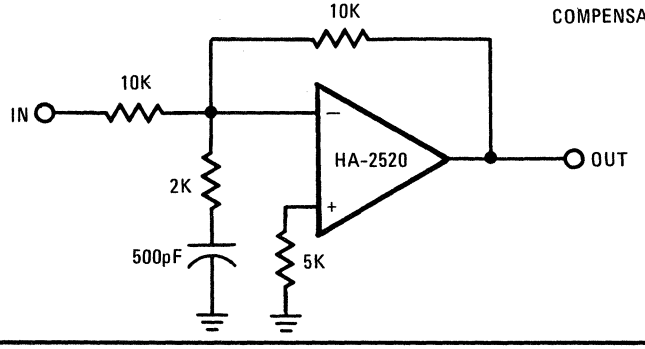


SUGGESTED OFFSET ZERO ADJUST HOOK-UP



TYPICAL APPLICATIONS

COMPENSATION CIRCUIT FOR INVERTING UNITY GAIN



Slew Rate	≈	120V/μs
Bandwidth	≈	10MHz
Settling Time	≈	500ns

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2530/2535

High Slew Rate, Wideband Inverting Amplifier

FEATURES

- HIGH SLEW RATE ±320V/μs
- FAST SETTLING TIME 550ns
- WIDE POWER BANDWIDTH 5MHz
- HIGH GAIN BANDWIDTH PRODUCT 70MHz
- LOW OFFSET VOLTAGE 0.8mV
- LOW POWER SUPPLY CURRENT 3.5mA

APPLICATIONS

- PULSE AMPLIFICATION
- SIGNAL CONDITIONING
- SIGNAL GENERATORS
- COAXIAL CABLE DRIVERS
- INTEGRATORS

DESCRIPTION

HA-2530 and HA-2535 are monolithic high speed inverting amplifiers which deliver superior slew rate, bandwidth, and accuracy specifications compared to any other amplifier in its class. Designs of these dielectrically isolated amplifiers utilize the feed forward amplifier technique to produce excellent dynamic and DC specifications coupled with low power consumption. These devices require no external compensation at closed loop gains greater than 10.

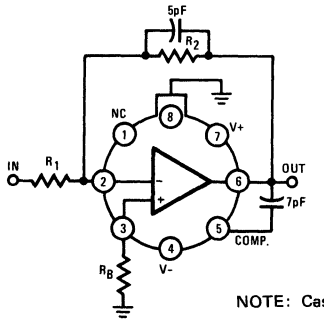
These amplifiers are excellent components for pulse circuits, data acquisition designs, and high speed integrators that can take advantage of the ±320V/μs slew rate and 550ns (0.1%) settling time. 70MHz gain bandwidth product, 5MHz power bandwidth coupled with 0.8mV offset voltage and ±50mA typical output current levels make these amplifiers ideally suited for signal conditioning, signal generation, and coaxial driver applications.

The HA-2530 and HA-2535 are available in metal can (TO-99) packages. HA-2530 is specified over the -55°C to +125°C range while HA-2535 is specified from 0°C to +75°C.

PINOUT

TO-99 **Package Code 2A**

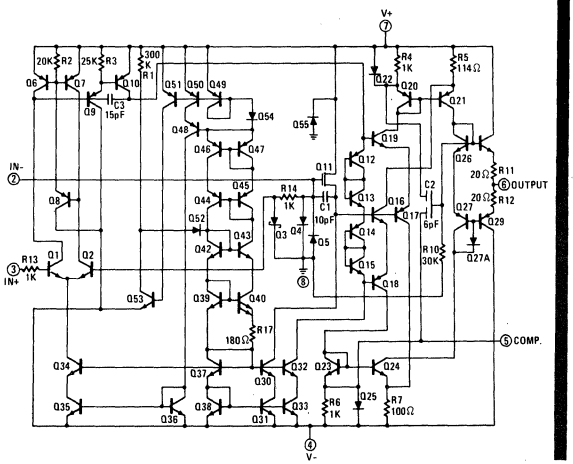
Top View



NOTE: Case tied to V-

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Internal Power Dissipation (Note 1)	550mW	
		Operating Temperature Range	$-55^{o}C \leq T_A \leq +125^{o}C$	(HA-2530)
Peak Output Current	±100mA		$0^{o}C \leq T_A \leq +75^{o}C$	(HA-2535)
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$	

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{Supply} = ±15.0V Unless Otherwise Specified.

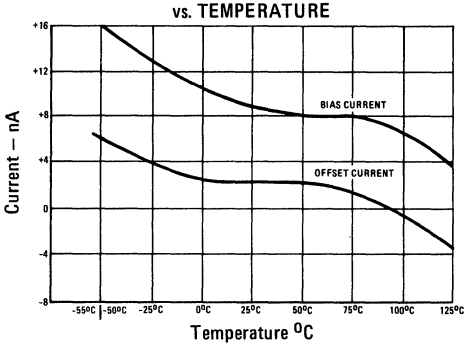
		HA-2530 -55°C to +125°C			HA-2535 0°C to +75°C			
		LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		0.8			0.8		mV
	Full			3			5	mV
Average Offset Voltage Drift	Full		5			5		µV/°C
* Bias Current	+25°C		15			15		nA
	Full			100			200	nA
* Offset Current	+25°C		5			5		nA
	Full			20			20	nA
Input Resistance	+25°C		2			2		MΩ
Input Capacitance	+25°C		10			10		pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 2,5)	+25°C		$2X10^6$			$2X10^6$		V/V
*	Full	10^5			10^5			V/V
* Common-Mode Rejection Ratio (Note 3)	Full	86	100		80	100		dB
Gain Bandwidth Product (Note 4)	+25°C		70			70		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
* Output Current (Note 5)	+25°C	±25	±50		±25	±50		mA
Full Power Bandwidth (Note 5)	+25°C	4	5		4	5		MHz
TRANSIENT RESPONSE (NOTES 6&7)								
* Rise Time	+25°C		20	40		20	40	ns
* Overshoot	+25°C		30	45		30	50	%
* Slew Rate	+25°C	±280	±320		±250	±320		V/µs
Settling Time	+25°C		500			500		ns
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		3.5	6		3.5	6	mA
* Power Supply Rejection Ratio (Note 8)	Full	86	100		80	100		dB

NOTES:
1. Derate at 5.5mW/°C for Operation at Ambient Temperature Above 75°C.
2. R_L = 2K
3. $V_{CM} = \pm 5.0V$
4. $A_V > 10$
5. $V_O = \pm 10V$
6. C_L = 50pF
7. See Transient Response Test Circuit and Wave Forms, Page 4.
8. $\Delta V = \pm 5.0V$

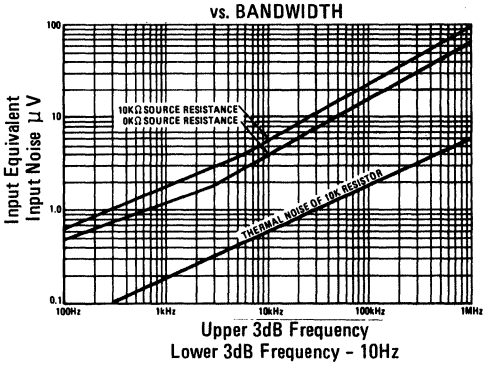
*100% Tested For DASH 8

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

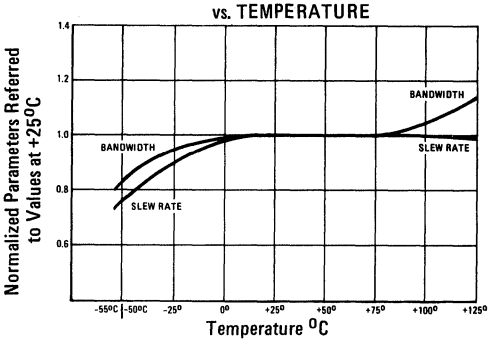
INPUT BIAS AND OFFSET CURRENT
vs. TEMPERATURE



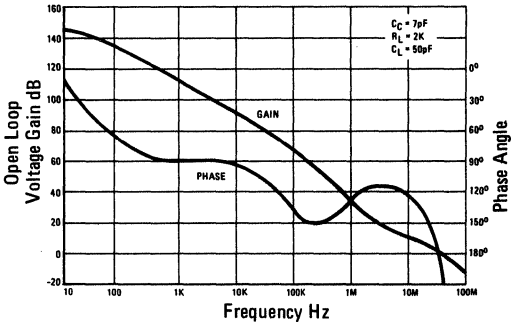
EQUIVALENT INPUT NOISE
vs. BANDWIDTH



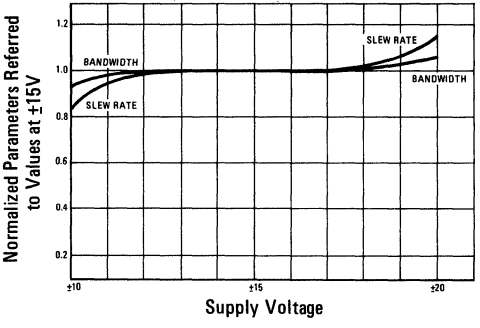
NORMALIZED AC PARAMETERS
vs. TEMPERATURE



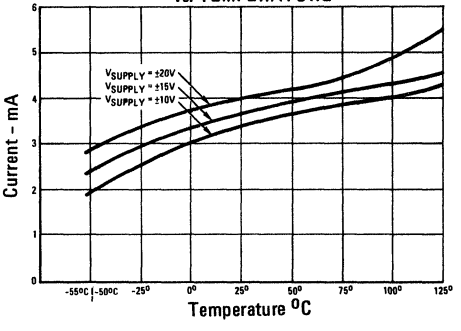
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



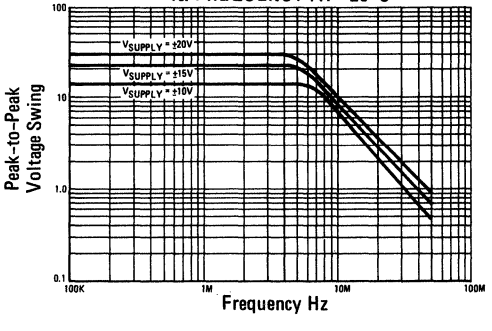
NORMALIZED AC PARAMETERS
vs. SUPPLY VOLTAGE AT +25°C



POWER SUPPLY CURRENT
vs. TEMPERATURE

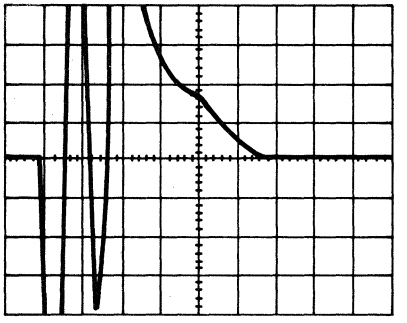


OUTPUT VOLTAGE SWING
vs. FREQUENCY AT +25°C



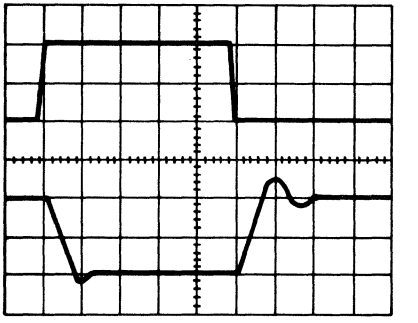
2

SETTLING TIME MEASUREMENT *1



VERTICAL = 5mV/DIV.
HORIZONTAL = 100ns/DIV.
T_A = +25°C, V_S = ±15V

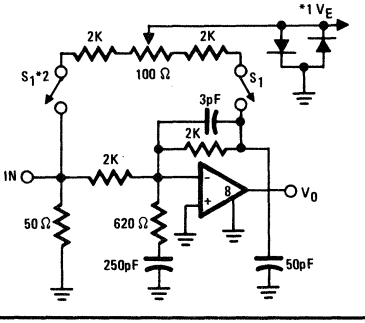
UNITY GAIN PULSE RESPONSE

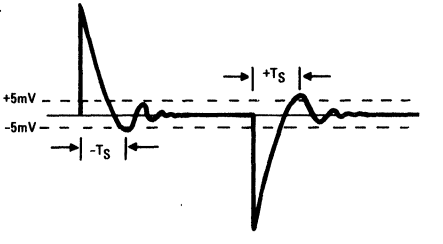


UPPER TRACE: INPUT VERTICAL = 5V/DIV.
LOWER TRACE: OUTPUT HORIZONTAL = 50ns/DIV.
T_A = +25°C, V_S = ±15V

2

SLEW RATE/SETTLING TIME/TRANSIENT RESPONSE TEST CIRCUIT

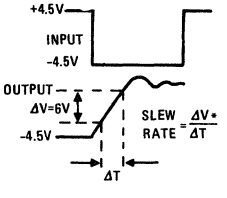




*1 Settling time (T_S) is measured using a high speed high recovery oscilloscope to display the error voltage V_E. When V_E is within ±5mV of final value the output V_O will be within ±10mV (0.1%).

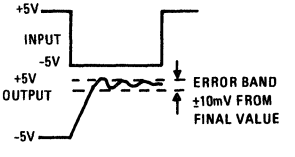
*2 S_1 closed for settling time.

SLEW RATE

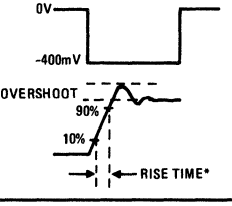


* MEASURED ON BOTH POSITIVE AND NEGATIVE EXCURSIONS.

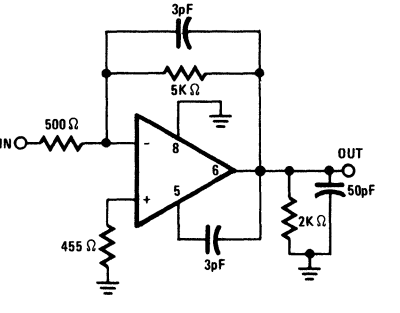
SETTLING TIME



TRANSIENT RESPONSE



5MHz VIDEO AMPLIFIER (A_V = 10)



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2600/2602/2605

Wide Band, High Impedance Operational Amplifier

FEATURES

- WIDE BANDWIDTH — 12MHz
- HIGH INPUT IMPEDANCE — 500MΩ
- LOW INPUT BIAS CURRENT — 1nA
- LOW INPUT OFFSET CURRENT — 1nA
- LOW INPUT OFFSET VOLTAGE — 0.5mV
- HIGH GAIN — 150K V/V
- HIGH SLEW RATE — 7V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- VIDEO AMPLIFIER
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

DESCRIPTION

HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500 MΩ, HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth product, 7V/μs slew rate and 150,000V/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characterisitics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

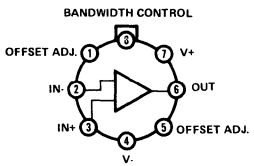
In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

HA-2600 and HA-2602 are guaranteed over -55°C to +125°C. HA-2605 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and HA-2600/2602 are available in 10 lead flat packages.

PINOUT

TO-99 TOP VIEW

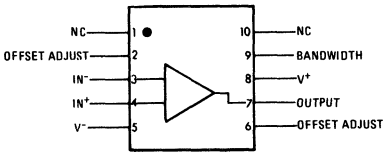
Package Code 2A



Case Connected to V-

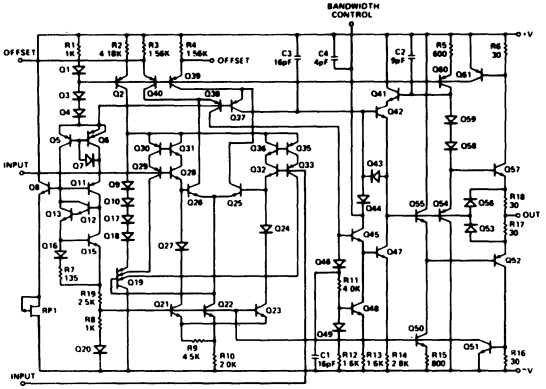
TO-91 TOP VIEW

Package Code 9V
(HA-2600/2602 Only)



Case Connected to V-

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Operating Temperature Range – HA-2600/HA-2602	$-55^oC \leq T_A \leq +125^oC$
HA-2605	$0^o \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS V+=+15VDC, V- = -15VDC

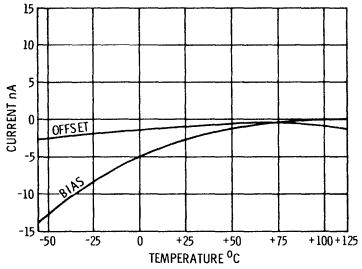
		HA-2600 −55°C to +125°C			HA-2602 −55°C to +125°C			HA-2605 0°C to +75°C			
		LIMITS			LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		0.5	4		3	5		3	5	mV
	Full		2	6			7			7	mV
Offset Voltage Average Drift	Full		5								µV/°C
* Bias Current	+25°C		1	10		15	25		5	25	nA
	Full		10	30			60			40	nA
* Offset Current	+25°C		1	10		5	25		5	25	nA
	Full		5	30			60			40	nA
Input Resistance	+25°C	100	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 1, 4)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		74	100		dB
Unity Gain Bandwidth (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Note 4)	+25°C	50	75		50	75		50	75		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		30	60		30	60		30	60	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	40		25	40	%
* Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±4	±7		±4	±7		±4	±7		V/µs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		1.5			1.5			1.5		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

TEST CONDITIONS

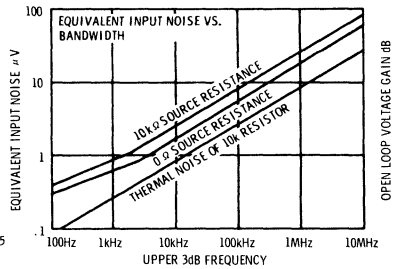
NOTES:
1. R_L = 2K
2. $V_{CM} = \pm 5.0V$
3. $V_O < 90mV$
4. $V_O = \pm 10V$
5. C_L = 100pF
6. $V_O = \pm 200mV$
7. $V_O = \pm 400mV$
8. See Transient response test circuits and waveforms page three.
9. $V_S = \pm 9.0V$ to $\pm 15V$

*100% Tested For DASH 8

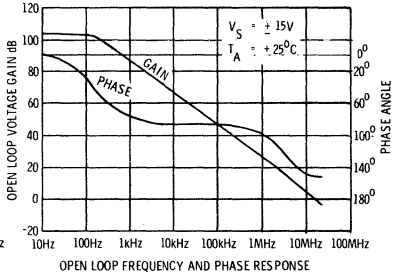
V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.



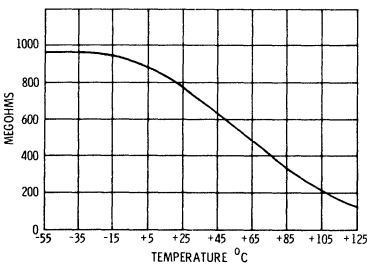
INPUT BIAS CURRENT AND OFFSET CURRENT
AS A FUNCTION OF TEMPERATURE



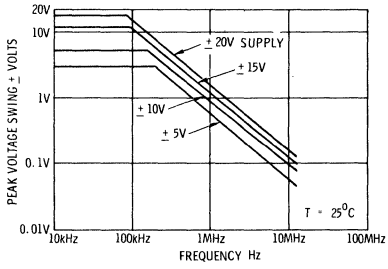
LOWER 3dB FREQUENCY - 10Hz
BROADBAND NOISE CHARACTERISTICS



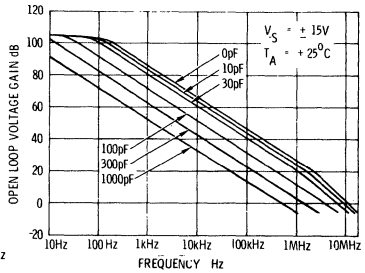
OPEN LOOP FREQUENCY AND PHASE RESPONSE



INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

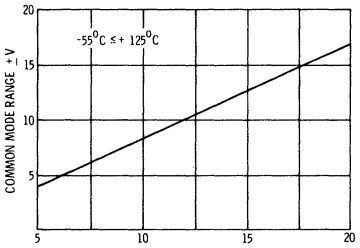


OUTPUT VOLTAGE SWING VS. FREQUENCY

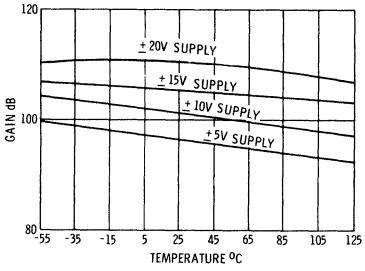


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

Note: External Compensation Components are not Required for Stability, But May be Added to Reduce Bandwidth if Desired. If External Compensation is Used, Also Connect 100pF Capacitor From Output to Ground.

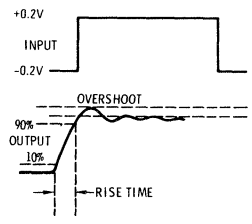


COMMON MODE VOLTAGE RANGE
AS A FUNCTION OF SUPPLY VOLTAGE



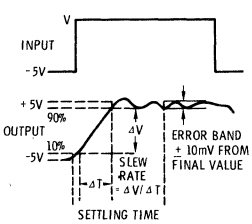
OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE

TRANSIENT RESPONSE

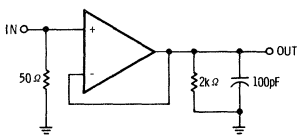


NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

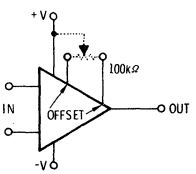
SLEW RATE AND SETTLING TIME



SLEW RATE AND TRANSIENT RESPONSE

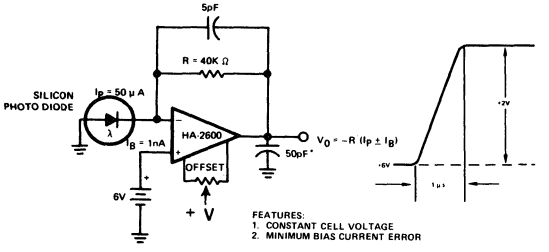


SUGGESTED OFFSET ZERO ADJUST HOOK-UP



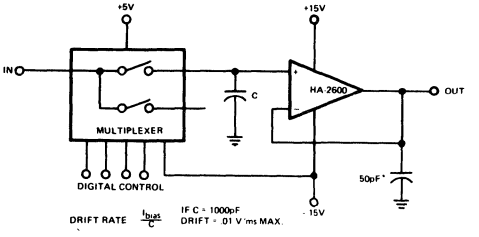
TYPICAL APPLICATIONS

PHOTO-CURRENT TO VOLTAGE CONVERTER



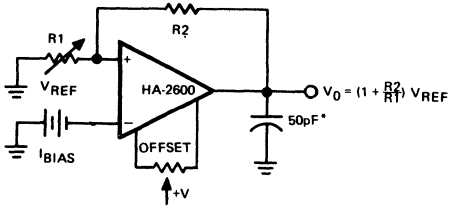
FEATURES:
1. CONSTANT CELL VOLTAGE
2. MINIMUM BIAS CURRENT ERROR

SAMPLE – AND – HOLD



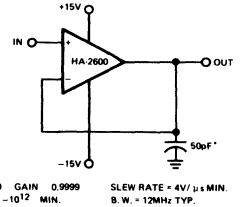
DRIFT RATE $\frac{I_{bias}}{C}$ IF C = 1000pF DRIFT = .01 V/ms MAX.

REFERENCE VOLTAGE AMPLIFIER



FEATURES:
1. MINIMUM BIAS CURRENT IN REFERENCE CELL
2. SHORT-CIRCUIT PROTECTION

VOLTAGE FOLLOWER



1.000 GAIN 0.9999
$Z_{in} = -10^{12}$ MIN.
Z_{out} = .01 MAX.

SLEW RATE = 4V/ μs MIN.
B.W. = 12MHz TYP.
OUTPUT SWING = ± 10V MIN. TO 50kHz

*A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

DEFINITIONS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT – The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE – The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE – The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO – The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING – The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE – The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE – The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in input voltage producing it.

BANDWIDTH – The frequency at which the voltage gain is 3dB below its low frequency value.

UNITY GAIN BANDWIDTH – The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO – The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE – The closed loop step function response of the amplifier under small signal conditions.

PHASE MARGIN – $(180^o - (\phi_1 - \phi_2))$ where ϕ_1 is the phase shift at the frequency where the absolute magnitude of gain is unity ϕ_2 is the phase shift at a frequency much lower than the open loop bandwidth.

SLEW RATE (Rate Limiting) – The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing) . . . restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

SETTLING TIME – Time required for output waveform to remain within 0.1% of final value.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2620/2622/2625

Very Wide Band, Uncompensated Operational Amplifiers

FEATURES

- GAIN BANDWIDTH PRODUCT(A_V = 5) 100MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 0.5mV
- HIGH GAIN 150K V/V
- HIGH SLEW RATE 35V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- VIDEO AND R.F. AMPLIFIERS
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

DESCRIPTION

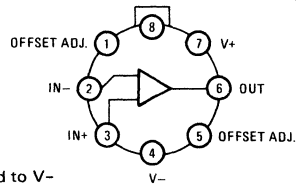
HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 100MHz gain-bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/ μs slew rate and 150,000V/V open-loop gain enables HA-2620/2622/2625 to perform high-gain amplification of very fast, wideband signals. These dynamic characterisitcs, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequiency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

HA-2620 and HA-2622 are guaranteed over -55°C to +125°C. HA-2625 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and 14 lead D.I.P. packages.

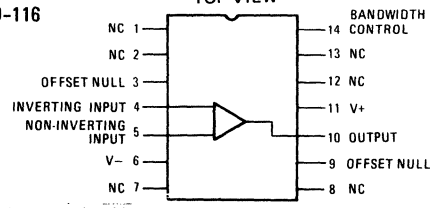
PINOUT

TO-99 — TOP VIEW — **Package Code 2A**



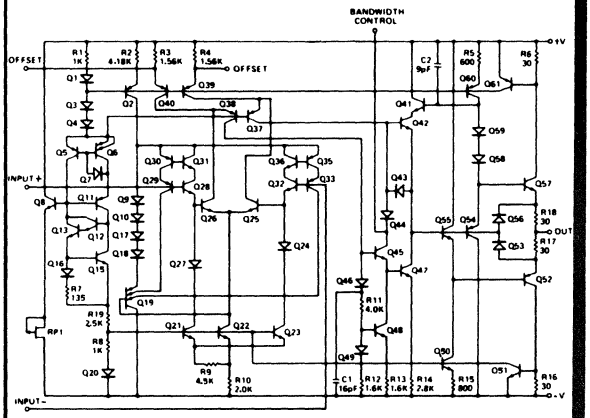
Case Connected to V−

TO-116 — TOP VIEW — **Package Code 4U**



Case Connected to V−

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

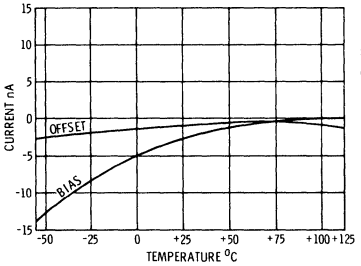
$V^+ = +15$ VDC, $V^- = -15$ VDC

PARAMETER	TEMPERATURE	HA-2620 −55°C to +125°C MIN.	HA-2620 −55°C to +125°C TYP.	HA-2620 −55°C to +125°C MAX.	HA-2622 −55°C to +125°C MIN.	HA-2622 −55°C to +125°C TYP.	HA-2622 −55°C to +125°C MAX.	HA-2625 0°C to +75°C MIN.	HA-2625 0°C to +75°C TYP.	HA-2625 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage (Note 1)	+25°C		0.5	4		3	5		3	5	mV
	Full			6			7			7	mV
* Bias Current	+25°C		1	15		5	25		5	25	nA
	Full		10	35			60			40	nA
* Offset Current	+25°C		1	15		5	25		5	25	nA
	Full		5	35			60			40	nA
Input Resistance	+25°C	65	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 2 & 3)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
* Common Mode Rejection Ratio (Note 4)	Full	80	100		74	100		74	100		dB
Gain Bandwidth Product (Notes 2, 5, &6)	+25°C		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 3)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Notes 2, 3 & 7)	+25°C	400	600		320	600		320	600		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 2, 5, 7 & 8)	+25°C		17	45		17	45		17	45	ns
* Slew Rate (Notes 2, 7, 8 & 10)	+25°C	±25	±35		± 20	±35		± 20	±35		V/μs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

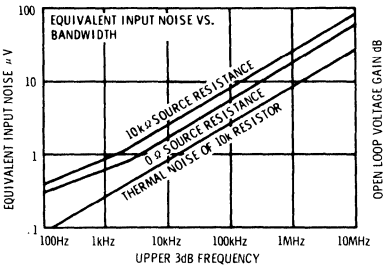
NOTES:
1. Offset may be externally adjusted to zero.
2. $R_L = 2K\Omega$, $C_L = 50pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 5.0V$
5. $V_O < 90mV$
6. 40dB Gain
7. See transient response test circuits and waveforms page 3.
8. $A_V = 5.0V$ (The HA-2620 family is not stable at unity gain without external compensation.)
9. $V_{Sup} = \pm 9.0V$ to $\pm 15.0V$
10. $V_O = 5.0V$

*100% Tested For DASH 8

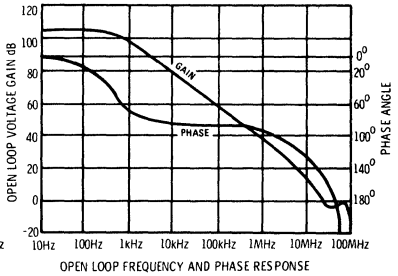
V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.



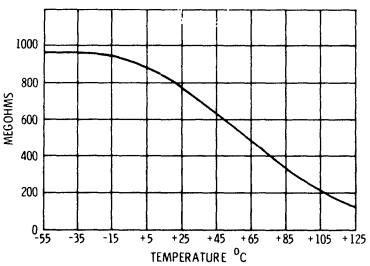
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



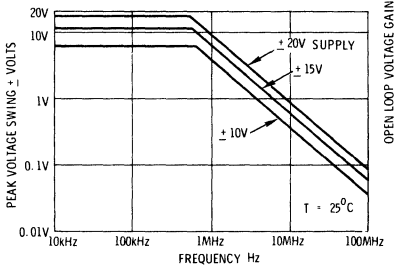
BROADBAND NOISE CHARACTERISTICS



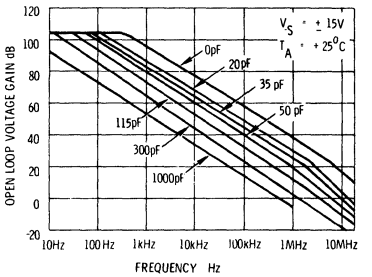
OPEN LOOP FREQUENCY AND PHASE RESPONSE



INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

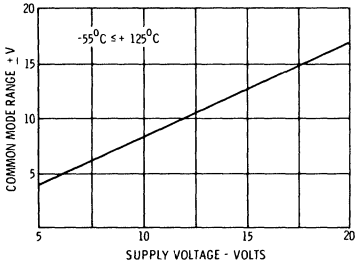


OUTPUT VOLTAGE SWING VS. FREQUENCY

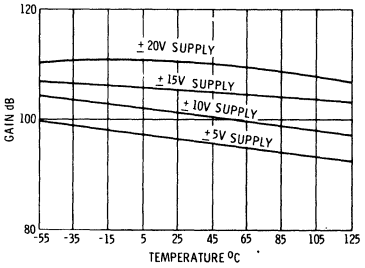


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

Note: External Compensation is Required For Closed Loop Gain <5. If External Compensation is Used, Also Connect 100 pF Capacitor From Output to Ground.

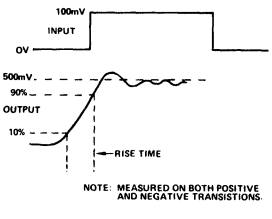


COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



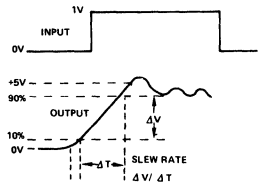
OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE

TRANSIENT RESPONSE

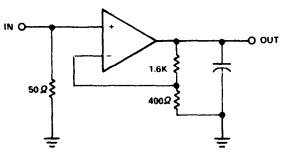


NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSISTIONS.

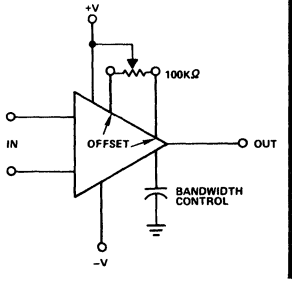
SLEW RATE



SLEW RATE AND TRANSIENT RESPONSE

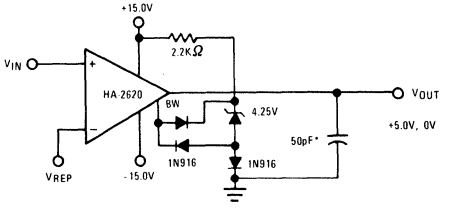


SUGGESTED OFFSET ZERO ADJUST AND BANDWIDTH CONTROL HOOK-UP

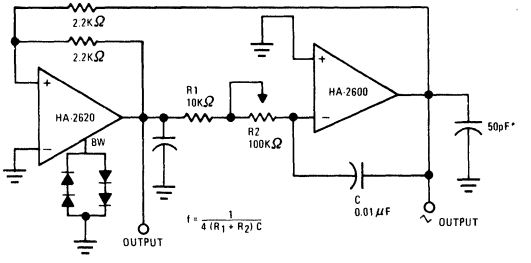


TYPICAL APPLICATIONS

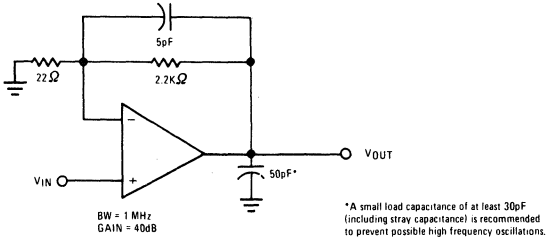
HIGH IMPEDANCE COMPARATOR



FUNCTION GENERATOR



VIDEO AMPLIFIER



*A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations.

DEFINITIONS

INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals through two equal resistances to force the output voltage to zero.

INPUT OFFSET CURRENT—The difference in the currents into the two input terminals when the output is at zero voltage.

INPUT BIAS CURRENT—The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT COMMON MODE VOLTAGE—The average referred to ground of the voltages at the two input terminals.

COMMON MODE RANGE—The range of voltages which is exceeded at either input terminal will cause the amplifier to cease operating.

COMMON MODE REJECTION RATIO—The ratio of a specified range of input common mode voltage to the peak-to-peak change in input offset voltage over this range.

OUTPUT VOLTAGE SWING—The peak symmetrical output voltage swing, referred to ground, that can be obtained without clipping.

INPUT RESISTANCE—The ratio of the change in input voltage to the change in input current.

OUTPUT RESISTANCE—The ratio of the change in output voltage to the change in output current.

VOLTAGE GAIN—The ratio of the change in output voltage to the change in input voltage producing it.

UNITY GAIN BANDWIDTH—The frequency at which the voltage gain of the amplifier is unity.

POWER SUPPLY REJECTION RATIO—The ratio of the change in input offset voltage to the change in power supply voltage producing it.

TRANSIENT RESPONSE—The closed loop step function response of the amplifier under small signal conditions.

GAIN BANDWIDTH PRODUCT—The product of the gain and the bandwidth at a given gain.

SLEW RATE (Rate Limiting)—The rate at which the output will move between full scale stops, measured in terms of volts per unit time. This limit to an ideal step function response is due to the non-linear behavior in an amplifier due to its limited ability to produce large, rapid changes in output voltage (slewing)...restricting it to rates of change of voltage lower than might be predicted by observing the small signal frequency response.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2630/2635

High Performance Current Booster

FEATURES

- OUTPUT CURRENT ±400mA
- SLEW RATE 500V/μs
- BANDWIDTH 8MHz
- FULL POWER BANDWIDTH 8MHz
- INPUT RESISTANCE $2.0 \times 10^6 \Omega$
- OUTPUT RESISTANCE 2.0Ω
- POWER SUPPLY RANGE ±5V to ±20V
- PACKAGE IS ELECTRICALLY ISOLATED

APPLICATIONS

- COAXIAL CABLE DRIVERS
- AUDIO OUTPUT AMPLIFIERS
- SERVO MOTOR DRIVERS
- POWER SUPPLIES (BIPOLAR)
- PRECISION DATA RECORDING

DESCRIPTION

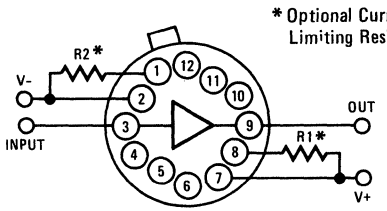
HA-2630 and HA-2635 are monolithic, unity voltage gain current amplifiers delivering extremely high slew rate, wide bandwidth, and full power bandwidth even under heavy output loading conditions. This dielectrically isolated current booster also offers high input impedance and low output resistance. These devices are intended to be used in series with an operational amplifier and inside the feedback loop whenever additional output current is required. Output current levels are programmable by selecting two optional external resistors.

These current amplifiers offer an exceptional 500V/μs slew rate and 8MHz bandwidth which allows them to be used with many high performance op amps in precision data recording and high speed coaxial cable driver designs. 2.0M ohm input resistance and 2 ohm output resistance coupled with ±400mA output current make HA-2630 and HA-2635 ideal components in high fidelity audio output amplifier designs.

HA-2630 and HA-2635 are available in an electrically isolated TO-8 type can for ease of mounting with or without a heat sink. HA-2630 is specified over the -55°C to +125°C range. HA-2635 is specified from 0°C to +75°C.

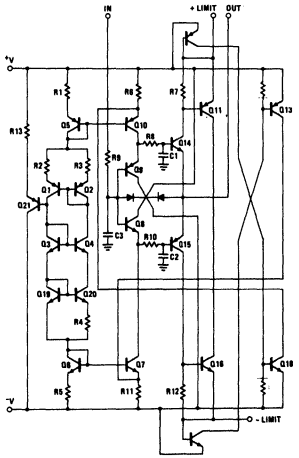
PINOUT

TO-8 **Package Code 2G**



Top View

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V
Input Voltage Range	± V Supply
Output Current (Note 2)	±700mA
Internal Power Dissipation (Note 6) Free Air:	1W
In Heat Sink:	4W

Operating Temperature Range:
$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2630)
$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2635)
Storage Temperature Range:
$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

V_{Supply} = ±15 Volts R_L = 50 Ohms $R_1 = R_2$ = 0 Ohms Unless otherwise specified.

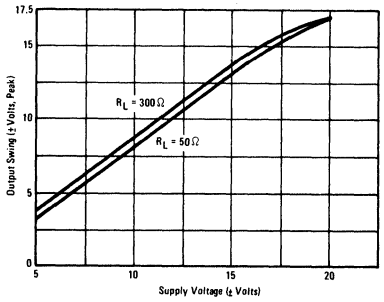
		HA-2630 -55°C to +125°C			HA-2635 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
*Bias Current	+25°C		30	150		30	150	µA
	Full			200			200	µA
Input Resistance	+25°C		2.0			2.0		MΩ
Input Capacitance	+25°C		5.0			5.0		pF
TRANSFER CHARACTERISTICS								
Voltage Gain (Note 1)	Full	.85	.95		.85	.95		V/V
*Offset Voltage ($V_{OUT} - V_{IN}$)	+25°C		70	±200		70	±200	mV
	Full			±300			±300	mV
Bandwidth (-3dB)	+25°C		8.0			8.0		MHz
OUTPUT CHARACTERISTICS								
*Output Voltage Swing	Full	±10			±10			V
*Output Current (Note 1)	Full	±300	±400		±300	±400		mA
Output Resistance	+25°C		2.0			2.0		Ω
Full Power Bandwidth (Note 1)	+25°C		8.0			8.0		MHz
TRANSIENT RESPONSE								
Rise Time (Note 3)	+25°C		30			30		ns
Slew Rate (Note 4)	+25°C	200	500		200	500		V/µs
POWER SUPPLY CHARACTERISTICS								
*Supply Current	Full		15	20		15	23	mA
Supply Voltage Range	Full	±5		±20	±5		±20	V
Power Supply Rejection Ratio (Note 5)	Full		66			66		dB

NOTES:
1. V_O = ±10V
2. Heat sink is required for continuous short circuit protection, regardless of current limit setting.
3. V_O = 0.4V p-p.
4. V_O = 10V p-p.
5. ΔV_{SUPPLY} = ±5V.
6. Without heat sink, derate by 14mW/°C ambient temperature above 100°C ambient, with heat sink, derate by 67mW/°C case temperature above 115°C case.

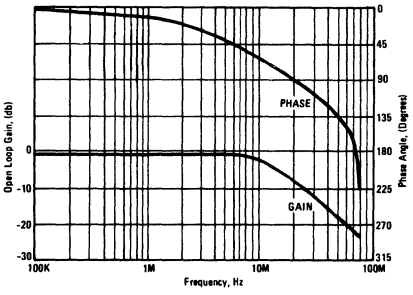
*100% Tested For DASH 8

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

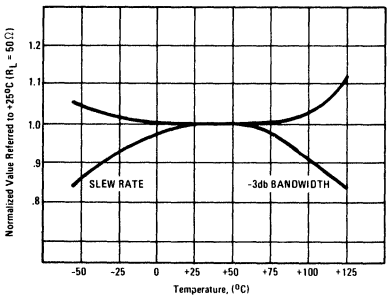
OUTPUT SWING
(R_{LIMIT} = 0Ω)



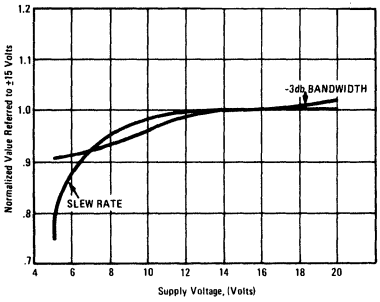
OPEN LOOP FREQUENCY AND
PHASE RESPONSE (R_L = 50Ω, C_L ≈10pf)



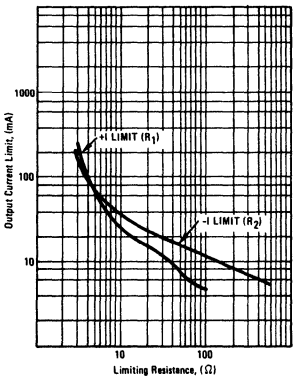
NORMALIZED AC PARAMETERS vs.
TEMPERATURE (R_L = 50Ω)



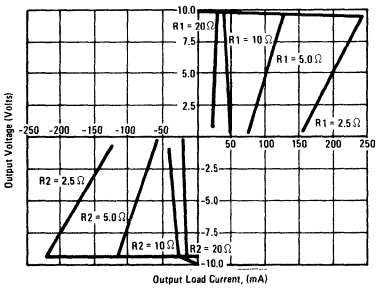
NORMALIZED AC PARAMETERS vs.
SUPPLY VOLTAGE (R_L = 50Ω)



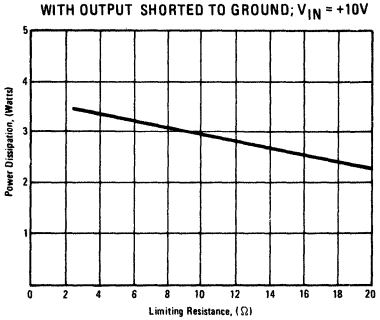
OUTPUT CURRENT LIMITING vs.
LIMITING RESISTANCE



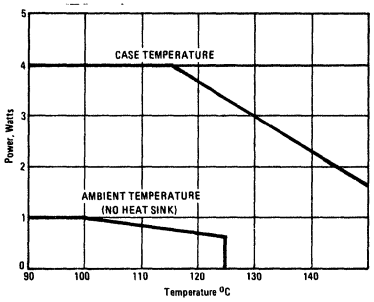
OUTPUT CURRENT CHARACTERISTIC



POWER DISSIPATION vs. LIMITING RESISTANCE
WITH OUTPUT SHORTED TO GROUND; V_{IN} = +10V



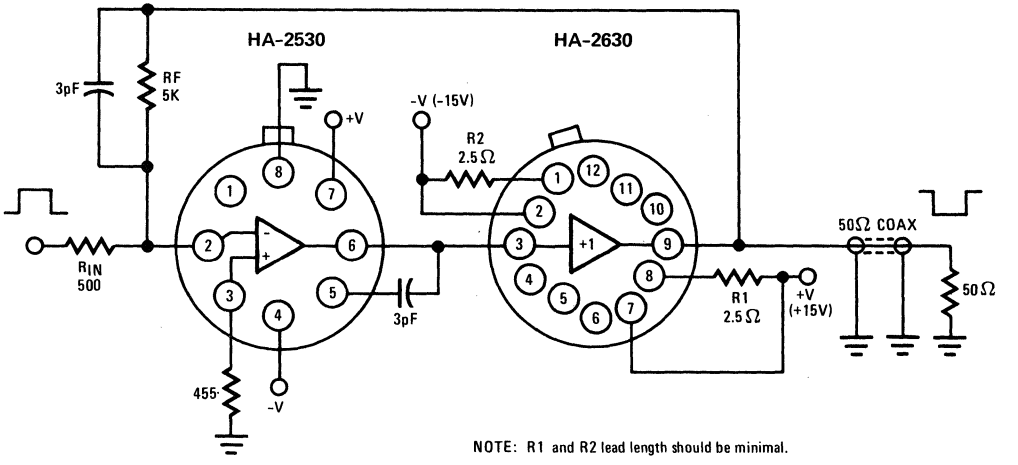
MAXIMUM ALLOWABLE INTERNAL
POWER DISSIPATION vs. TEMPERATURE



2

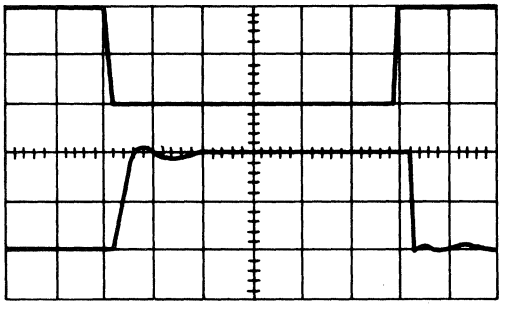
TYPICAL APPLICATION

20db, 5MHz VIDEO COAXIAL LINE DRIVER



NOTE: R1 and R2 lead length should be minimal.

LINE DRIVER PULSE RESPONSE



Horizontal Scale = 200ns/Div.
Upper Trace: Input, 200mV/Div.
Lower Trace: Output, 2V/Div.

SOME OTHER APPLICATIONS

- BIPOLAR POWER SUPPLY
- FUNCTION GENERATOR OUTPUT
- DEFLECTION COIL DRIVE
- AUDIO OUTPUT AMPLIFIER

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2640/2645

High Voltage Operational Amplifier

FEATURES

- OUTPUT VOLTAGE SWING ±35V
- SUPPLY VOLTAGE ±10V TO ±40V
- OFFSET CURRENT 5nA
- BANDWIDTH 4MHz
- SLEW RATE 5V/μs
- COMMON MODE INPUT VOLTAGE SWING ±35V
- OUTPUT OVERLOAD PROTECTION

APPLICATIONS

- INDUSTRIAL CONTROL SYSTEMS
- POWER SUPPLIES
- HIGH VOLTAGE REGULATORS
- RESOLVER EXCITATION
- SIGNAL CONDITIONING

DESCRIPTION

HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

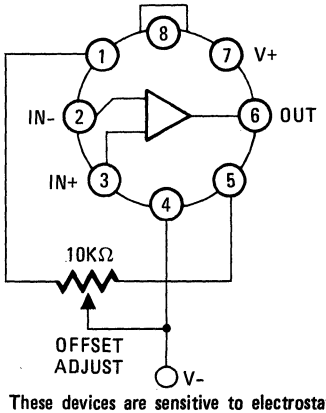
These amplifers deliver ±35V common mode input voltage swing, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and 5V/μs slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excellent components for resolver excitation designs.

HA-2640 and HA-2645 are available in metal can (TO-99) packages and can be used as high performance pin-to-pin replacements for many general purpose op amps. HA-2640 is specified from -55°C to +125°C and HA-2645 is specified over the 0°C to +75°C range.

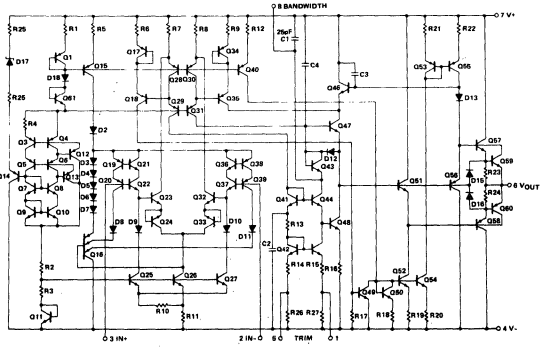
PINOUT

TO-99 **Package Code 2A**

Top View



SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals 100V
Input Voltage Range ±37V
Output Current/Full Short Circuit Protection
Internal Power Dissipation 680mW*

*Derate by 4.6mW/°C above +25°C

Operating Temperature Range
$-55^{\circ}C \leq T_A \leq +125^{\circ}C$ (HA-2640)
$0^{\circ}C \leq T_A \leq +75^{\circ}C$ (HA-2645)
Storage Temperature Range
$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm 40V$, $R_L = 5K$, Unless Otherwise Specified.

PARAMETER	TEMP.	HA-2640 -55°C to +125°C MIN.	HA-2640 -55°C to +125°C TYP.	HA-2640 -55°C to +125°C MAX.	HA-2645 0°C to +75°C MIN.	HA-2645 0°C to +75°C TYP.	HA-2645 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2	4		2	6	mV
	Full			6			7	mV
Offset Voltage Average Drift	Full		15			15		µV/°C
* Bias Current	+25°C		10	25		12	30	nA
	Full			50			50	nA
* Offset Current	+25°C		5	12		15	30	nA
	Full			35			50	nA
Input Resistance	+25°C	50	250		40	200		MΩ
Common Mode Range	Full	±35			±35			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 8)	+25°C	100K	200K		100K	200K		V/V
	Full	75K			75K			V/V
* Common Mode Rejection Ratio (Note 1)	Full	80	100		74	100		dB
Unity Gain Bandwidth (Note 2)	+25°C		4			4		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing	Full	±35			±35			V
* Output Current (Note 9)	+25°C	±12	±15		±10	±12		mA
Output Resistance	+25°C		500			500		Ω
Full Power Bandwidth (Note 3)	+25°C		23			23		kHz
TRANSIENT RESPONSE (Note 7)								
Rise Time (Notes 4, 6)	+25°C		60			60		ns
Overshoot (Notes 4, 6)	+25°C		15			15		%
Slew Rate (Note 6)	+25°C		5			5		V/µs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		3.2	3.8		3.2	4.5	mA
Supply Voltage Range	Full	±10		±40	±10		±40	V
* Power Supply Rejection Ratio (Note 5)	Full	80	90		74	90		dB

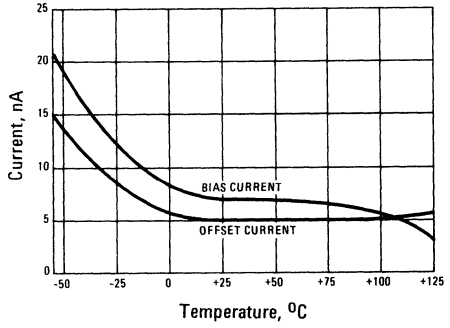
*100% Tested For DASH 8

NOTES:
1. $V_{CM} = \pm 30V$
2. $V_O = 90mV$
3. $V_O = \pm 35V$
4. $V_O = \pm 200mV$
5. $V_S = \pm 10V$ to $\pm 40V$
6. $A_V = 1$
7. $C_L = 50pF$
8. $\Delta V_O =$
9. $R_L = 1K\Omega$

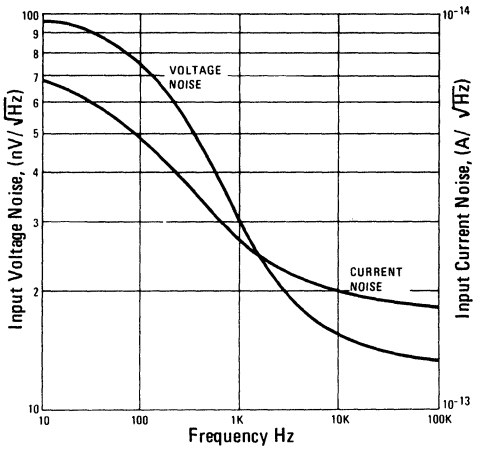
PERFORMANCE CURVES

V+ = V- = 40VDC, T_A = +25°C UNLESS OTHERWISE STATED

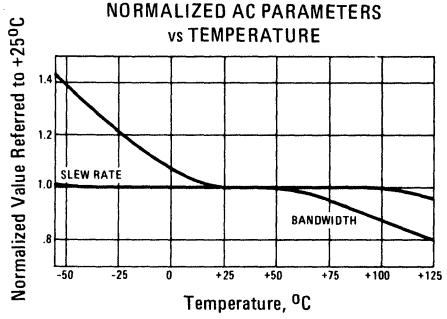
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



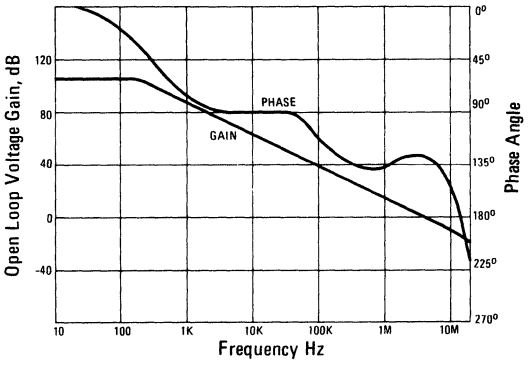
INPUT NOISE CHARACTERISTICS



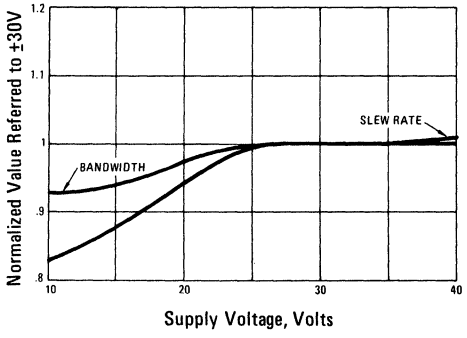
NORMALIZED AC PARAMETERS vs TEMPERATURE



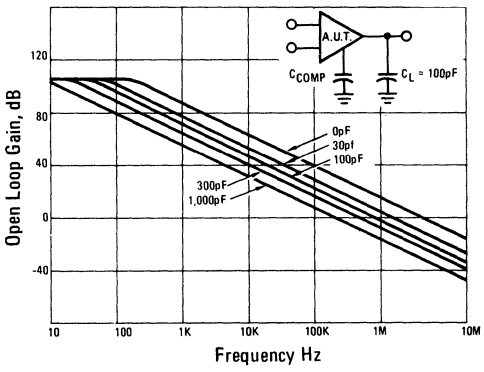
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



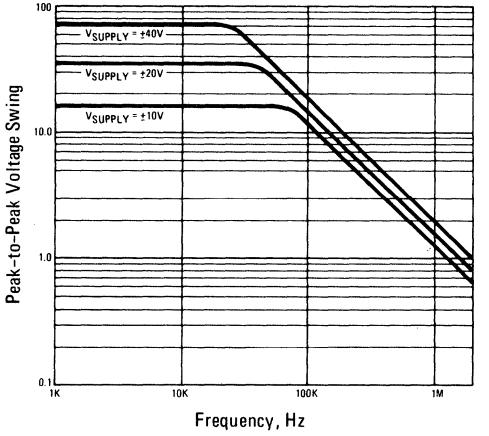
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



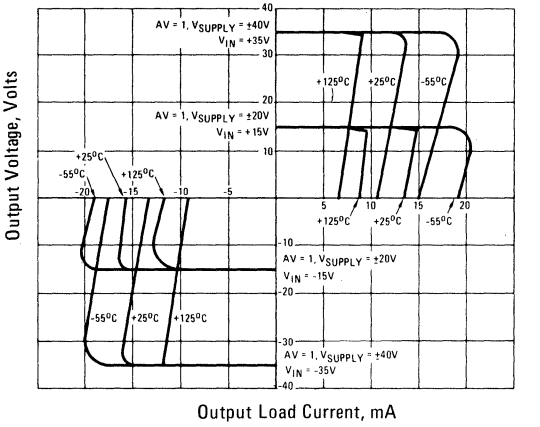
NOTE: External Compensation Components are not Required for Stability. But May be Added to Reduce Bandwidth if Desided. C_L = 100pF is Also Required for Stability Only if External Compensation Capacitor is Used.

PERFORMANCE CURVES (continued)

OUTPUT VOLTAGE SWING
vs FREQUENCY AT +25°C

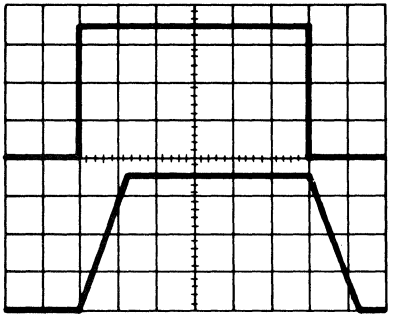


OUTPUT CURRENT CHARACTERISTIC



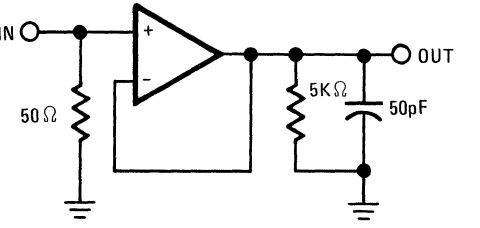
SWITCHING WAVEFORM AND TEST CIRCUIT

VOLTAGE FOLLOWER
PULSE RESPONSE



R_L = 5K, C_L = 50pF
Vertical = 10V/Div. T_A = +25°C
Horizontal = 5µs/Div. V_S = ±40V

SLEW RATE AND TRANSIENT
RESPONSE TEST CIRCUIT



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2650/2655

Dual High Performance Operational Amplifier

FEATURES

- SLEW RATE — 5V/μs
- BANDWIDTH — 8MHz
- BIAS CURRENT — 35nA
- AV. OFFSET VOLTAGE DRIFT — 8μV/^{o}C
- POWER CONSUMPTION — 75mW
- SUPPLY VOLTAGE RANGE — ±2V TO ±20V

APPLICATIONS

- VIDEO AMPLIFIERS
- HIGH IMPEDANCE, WIDEBAND BUFFERS
- INTEGRATORS
- AUDIO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

HA-2650/2655 contains two internally compensated operational amplifiers offering high slew rate and high frequency performance combined with exceptional DC characteristics. 5V/μ sec slew rate and 8MHz bandwidth make these amplifiers suitable for processing fast, wideband signals extending into the video frequency spectrum. Signal processing accuracy is enhanced by front-end performance that includes 1.5mV offset voltage, 8 μ V/^{o}C offset voltage drift and low offset and bias current (1nA and 35nA respectively). Offset voltage can be trimmed to zero on the devices offered in dual-in-line packages. Signal conditioning is further enhanced by 500MΩ input impedance.

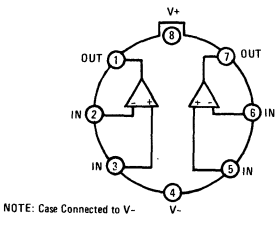
Applications for HA-2650/2655 include video circuit designs such as high impedance buffers, integrators, tone generators and filters. These amplifiers are also ideal components for active filtering of audio and voice signals.

HA-2650/2655 are offered in 14 pin D.I.P. and metal TO-99 packages and are also available in dice form. HA-2650 is specified from -55^{o}C to +125^{o}C. HA-2655 operates from 0^{o}C to +75^{o}C.

PINOUT

TO-99 — **Package Code 2A**

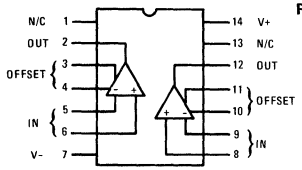
TOP VIEW



NOTE: Case Connected to V-

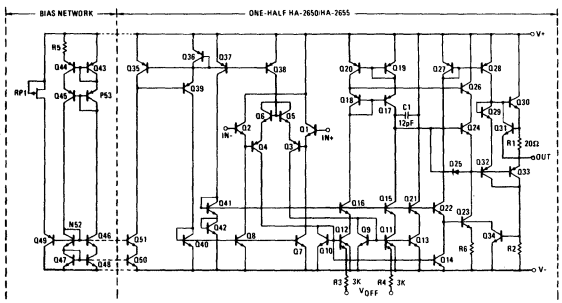
TO-116 — **Package Code 4U**

TOP VIEW



NOTE: Bottom of package is connected to V-.

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration	Indefinite

Power Dissipation (Note 2)	TO-99	300 mW
	TO-116	300 mW
Operating Temperature Range:		
HA-2650	$-55^oC \leq T_A \leq +125^oC$	
HA-2655	$0^oC \leq T_A \leq +75^oC$	
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$	

ELECTRICAL CHARACTERISTICS

V+ = 15V V- = -15V

PARAMETER	TEMP.	HA-2650 -55°C to +125°C MIN.	HA-2650 TYP.	HA-2650 MAX.	HA-2655 0°C to +75°C MIN.	HA-2655 TYP.	HA-2655 MAX.	UNITS
INPUT CHARACTERISTICS								
*Offset Voltage	+25°C		1.5	3		2	5	mV
	Full			5			7	mV
Av. Offset Voltage Drift	Full		8			8		µV/°C
*Bias Current	+25°C		35	100		50	200	nA
	Full			200			300	nA
*Offset Current	+25°C		1	30		2	60	nA
	Full			60			100	nA
Common Mode Range	Full	±13			±13			V
Differential Input Resistance	+25°C	5	20		5	20		MΩ
Common Mode Input Resistance	+25°C		500			500		MΩ
Input Capacitance	+25°C		5			5		pF
TRANSFER CHARACTERISTICS								
*Large Signal Voltage Gain (Note 3ab)	+25°C	25K	40K		20K	40K		V/V
	Full	20K			15K			V/V
*Common Mode Rejection Ratio (Note 4)	+25°C	80	100		74	100		dB
	Full	80			74			dB
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 3c)	+25°C	±13	±14		±13	±14		V
	Full	±13			±13			V
Full Power Bandwidth (Note 5)	+25°C	30	80		30	80		KHz
Output Current (Note 3a)	+25°C		±20			±18		mA
Output Resistance	+25°C		100			100		Ω
TRANSIENT RESPONSE (Note 6)								
Rise Time (Note 7)	+25°C		40			40		ns
Overshoot (Note 7)	+25°C		15			15		%
Slew Rate	+25°C	±2	±5		±2	±5		V/µs
POWER SUPPLY CHARACTERISTICS								
*Supply Current	+25°C		2.5	3		3	4	mA
*Power Supply Rejection Ratio (Note 8)	+25°C	80	100		74	100		dB
	Full	80			74			dB

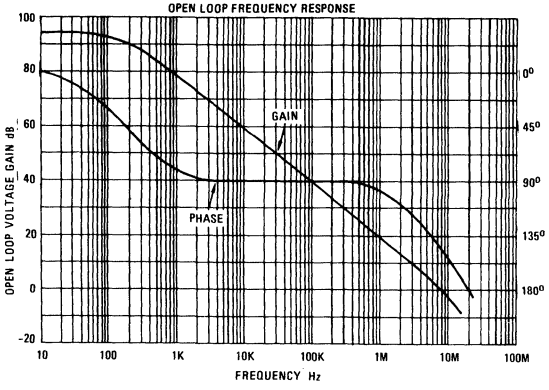
NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above +110°C.
3. (a) V_O = ±10V (b) R_L = 2K (c) R_L = 10K
4. V_{CM} = ±5.0V
5. A_V = 1, R_L = 2K, V_O = 20V_{pp}
6. See transient response/slew rate circuit.
7. V_{in} = 200mV
8. Δ V = ±5.0V

*100% Tested For DASH 8

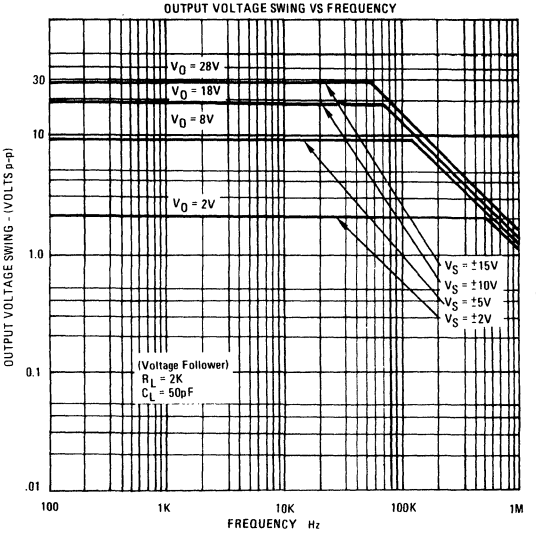
PERFORMANCE CURVES

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

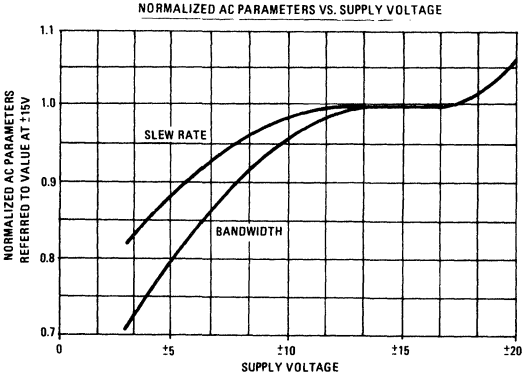
OPEN LOOP FREQUENCY RESPONSE



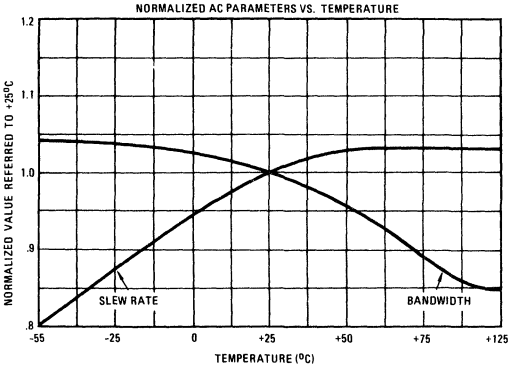
OUTPUT VOLTAGE SWING VS FREQUENCY



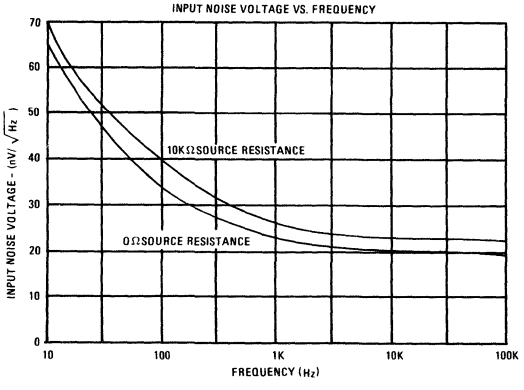
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



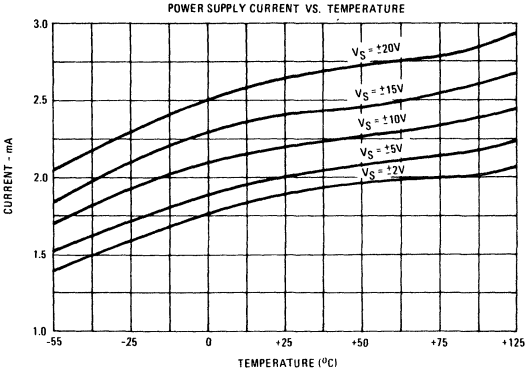
NORMALIZED AC PARAMETERS VS. TEMPERATURE



INPUT NOISE VOLTAGE VS. FREQUENCY



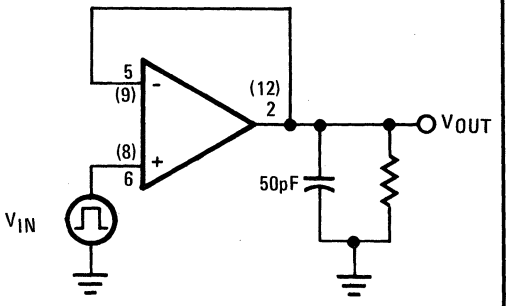
POWER SUPPLY CURRENT VS. TEMPERATURE



2

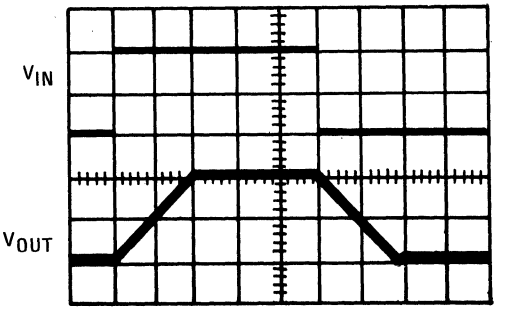
PERFORMANCE CHARACTERISTICS

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



Note: Numbers in parentheses refer to the second half of TO-116 package.

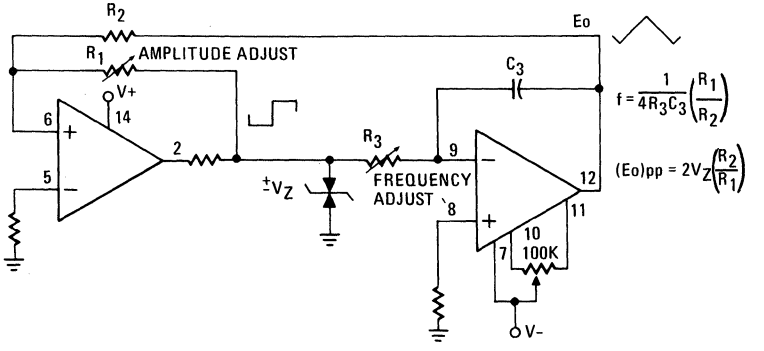
SLEWING WAVEFORM



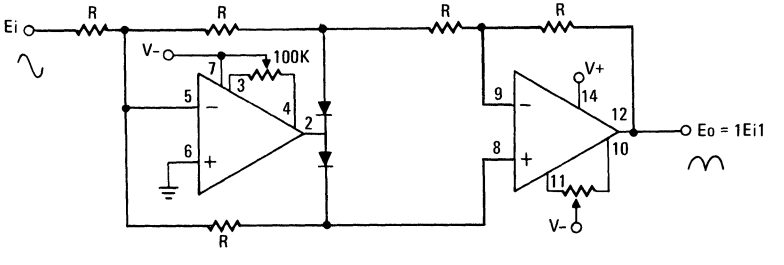
VERTICAL 5V/DIV. HORIZONTAL 1 μs/DIV.

TYPICAL APPLICATIONS

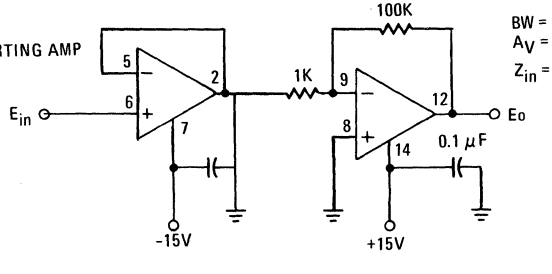
LOW COST HIGH FREQUENCY GENERATOR



ABSOLUTE-VALUE CIRCUIT



HIGH IMPEDANCE
HIGH GAIN
HIGH FREQUENCY INVERTING AMP



BW = 100KHz
A_V = 100
Z_{in} = 2 x 10^9 Ω

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2700/2704/2705

Low Power, High Performance Operational Amplifiers

FEATURES

- LOW POWER DISSIPATION — 2.24mW AT ±15.0V
- HIGH SLEW RATE — 20V/μs
- HIGH OPEN LOOP GAIN — 300K(R_L = 2KΩ)
- LOW INPUT BIAS CURRENT — 5nA
- LOW OFFSET VOLTAGE — 0.5mV
- HIGH CM_{rr} — 106dB
- WIDE POWER SUPPLY RANGE — ±5.5V TO ±20.0V

APPLICATIONS

- HIGH GAIN AMPLIFIER
- INSTRUMENTATION AMPLIFIERS
- ACTIVE FILTERS
- TELEMETRY SYSTEMS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2700/2704/2705 are internally compensated operational amplifiers which employ dielectric isolation to achieve excellent DC and dynamic performance with very low quiescent power consumption.

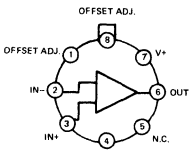
DC performance of the amplifier input is characterized by high CMRR (106dB), low offset voltage (0.5mV, HA-2700 and HA-2704; 1mV, HA-2705) along with low bias and offset current (5.0nA and 2.5nA respectively). These input specifications, in conjunction with offset null capability and open-loop gain of 300,000V/V, enable HA-2700/2704/2705 to provide accurate, high-gain signal amplification. Gain bandwidth 1MHz and slew rate of 20V/μs allow for processing of fast, wideband signals. Input and output signal amplitudes of at least ±11 volts can be accomodated while providing output drive capability of 10mA. For maximum reliability, the output is protected in the event of short circuits to ground.

These amplifiers operate from a wide range of supplies (±5.5V to ±20V) with a maximum quiescent supply drain of only 150μA. HA-2700/2704/2705 are, therefore, ideally suited to low-power instrumentation and filtering applications that require fast, accurate response over a wide range of signal frequency.

These amplifers are available in three performance grades: HA-2700 is rated for operation from -55°C to +125°C; HA-2704 is specified over -25°C to +85°C; HA-2705 is specified from 0°C to +75°C. All three devices are available in TO-99 cans or 14 lead D.I.P. packages.

PINOUT

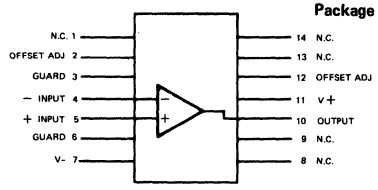
TO-99 — **Package Code 2A**



Case Connected to V-

TOP VIEW

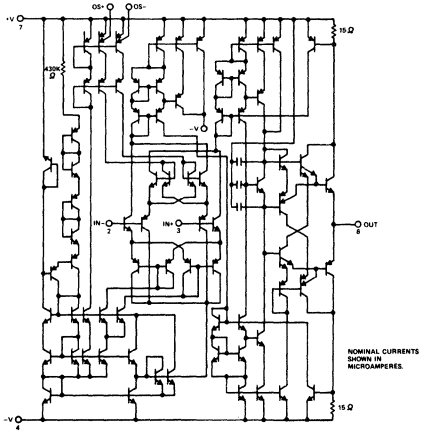
TO-116 — **Package Code 4U**



Case Connected to V-

TOP VIEW

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	44.0V
Differential Input Voltage	±18.0V
Internal Power Dissipation (Note 7)	300mW
Storage Temperature	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

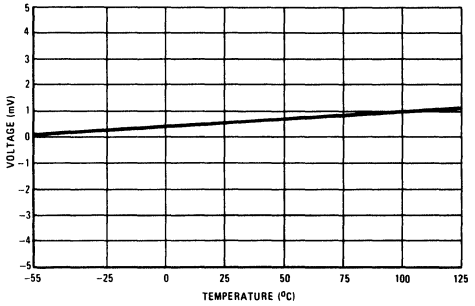
$V^+ = +15.0$ V.D.C. $V^- = -15.0$ V.D.C.

PARAMETER	TEMP.	HA-2700 −55°C to +125°C			HA-2704 −25°C to +85°C			HA-2705 0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
* Offset Voltage (Note 1)	+25°C		0.5	3.0		0.5	3.0		1.0	5.0	mV
	Full			5.0			6.0			7.0	mV
* Bias Current	+25°C		5.0	20.0		5.0	20.0		5.0	40.0	nA
	Full			50.0			50.0			70.0	nA
* Offset Current	+25°C		2.5	10.0		2.5	10.0		2.5	15.0	nA
	Full			30.0			30.0			40.0	nA
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 2 & 3)	+25°C	200K	300K		200K	300K		200K	300K		V/V
	Full	100K			100K			100K			V/V
* Common Mode Rejection Ratio (Note 4)	Full	86	106		86	106		80	106		dB
Gain Bandwidth Product (Note 2)	+25°C		1.0			1.0			1.0		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	+25°C	±12.0	±13.0		±12.0	±13.0		±12.0	±13.0		V
	Full	±11.0			±11.0			±11.0			V
Output Current (Note 3)	+25°C		10			10			10		mA
TRANSIENT RESPONSE CHARACTERISTICS											
* Slew Rate (Notes 2 & 6)	+25°C	10	20		10	20		10	20		V/µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		75	150		75	150		75	150	µA
* Power Supply Rejection Ratio (Note 5)	Full	86	100		86	100		80	100		dB

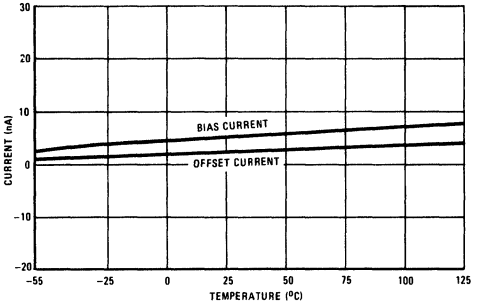
NOTES:
1. Can be adjusted to zero with 1 megohm pot between Pins 1 and 8 with the tap to Pin 7.
2. $R_L = 2K$, $C_L = 100pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 5.0V$
5. $V_S = \pm 10.0V$ to $\pm 2[illegible]0V$
6. $A_V = 5$
7. Derate by 6.6 mW/°C above 105°C.

*100% Tested For DASH 8

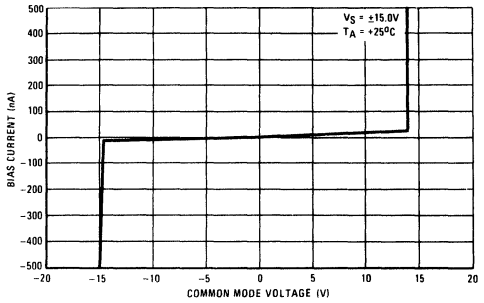
OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



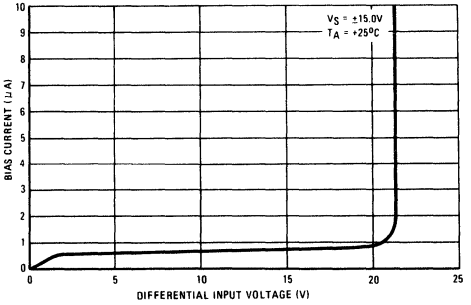
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



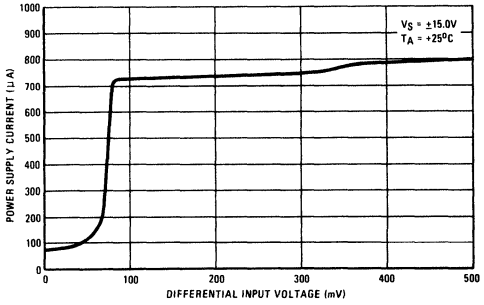
BIAS CURRENT AS A FUNCTION OF COMMON MODE VOLTAGE



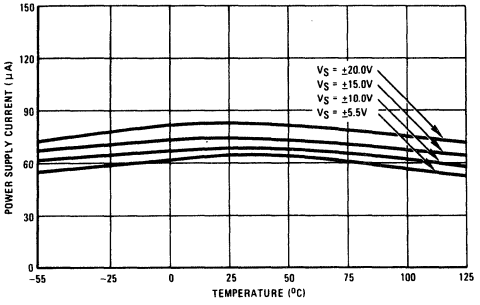
BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



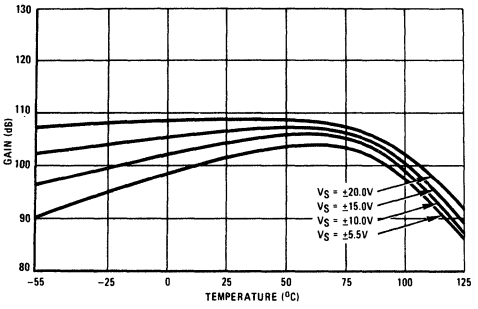
POWER SUPPLY CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



POWER SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



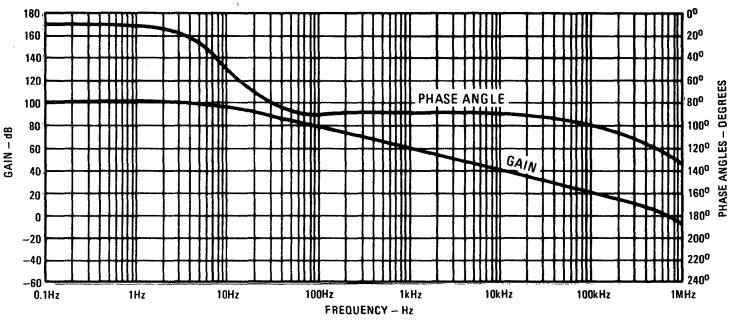
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



NOTE: Open loop (comparator) applications are not recommended, because of the above characteristic.

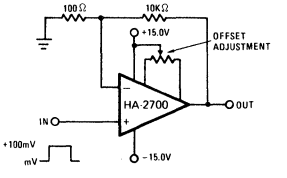
TYPICAL PERFORMANCE CURVES (continued)

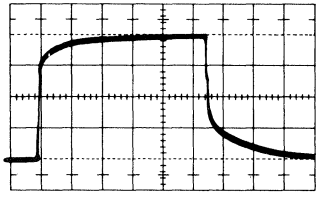
PHASE-FREQUENCY RESPONSE FOR THE HA-2700



TYPICAL APPLICATIONS

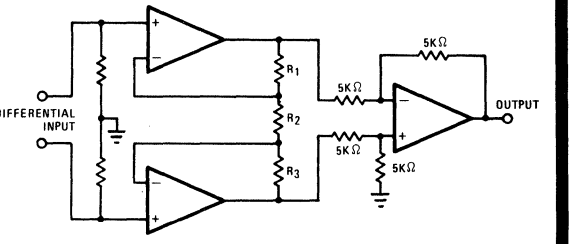
HIGH GAIN AMPLIFIER (100 V/V)





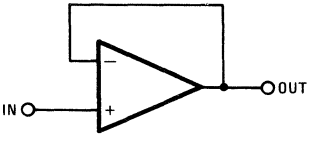
SCALE:
Horizontal – 20μs/division
Vertical – 5.0V/division

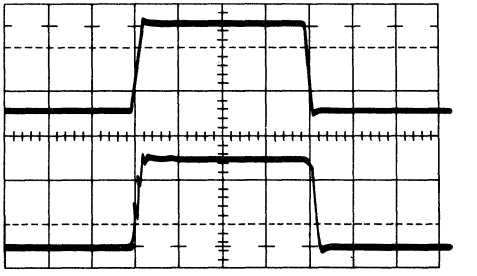
DIFFERENTIAL INPUT INSTRUMENTATION AMPLIFIER



THE GAIN IS GIVEN BY: $\frac{(R_1 + R_2 + R_3)}{R_2} = G$

UNITY GAIN VOLTAGE FOLLOWER





Non-inverting unity gain with a 2KΩand 100pF load
TOP: V_{IN} = 10.0V Peak to Peak
BOTTOM: V_{OUT}
SCALE: Horizontal -1 μs/division
Vertical -5.0V/division

NOTE: Faster increase rise and fall time and increase distortion on output wave form.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2720/25

Wide Range Programmable Operational Amplifier

FEATURES

- WIDE PROGRAMMING RANGE

SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2720/2725 programmable amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables HA-2720/2725 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2720 and HA-2725 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

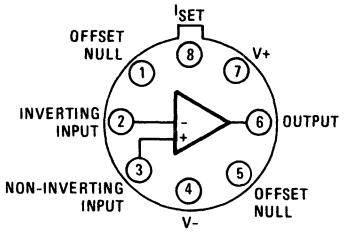
A major advantage of HA-2720/2725 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipment. A primary application for HA-2720/2725 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2720/2725 can be used for designs such as current controlled oscillators modulators, sample and hold circuits and variable active filters.

HA-2720 is guaranteed over -55°C to +125°C. HA-2725 is specified from 0°C to +75°C. Both parts are available in TO-99 cans or dice form.

PINOUT

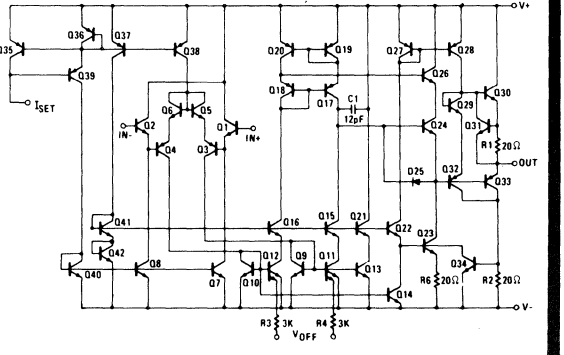
TO-99 **Package Code 2A**

Top View



NOTE: Case tied to V⁻

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	300mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2720	$-55^{o}C \leq T_A \leq +125^{o}C$
I_{SET} (Current at I_{SET})	500μA	HA-2725	$0^{o}C \leq T_A \leq +75^{o}C$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

V+ = +3.0V, V- = -3.0V

		HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Note 9)	25°C	20K	40K		20K	40K		15K	40K		15K	40K		V/V
	Full	15K			15K			10K			10K			V/V
*Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		15			170			15			170		μA
	Full			20			200			20			200	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

*100% Tested For DASH 8

ELECTRICAL CHARACTERISTICS

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
*Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
*Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Notes 3 & 9)	25°C	40K	100K		40K	120K		25K	100K		25K	120K		V/V
	Full	25K			25K			20K			20K			V/V
*Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current	25°C		20			210			20			210		μA
	Full			25			250			25			250	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

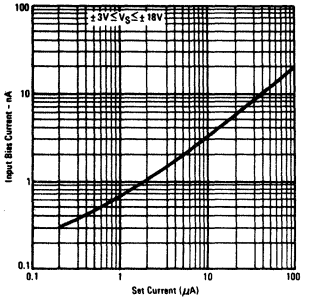
NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 6.8mW/°C for operation ambient temperatures above 75°C.

	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	RR_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

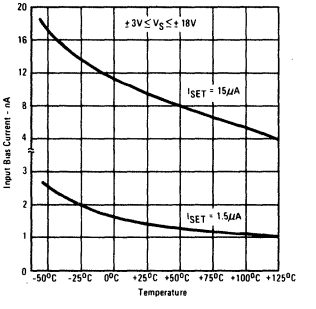
*100% Tested For DASH 8

UNLESS OTHERWISE NOTED: $T_A = +25^0C$, $V_S = \pm 15VDC$

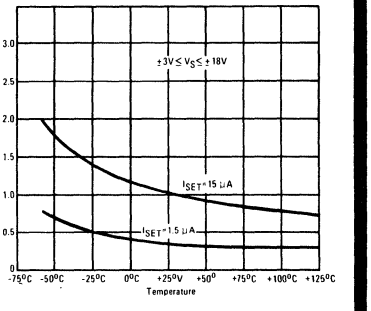
INPUT BIAS CURRENT
vs. SET CURRENT



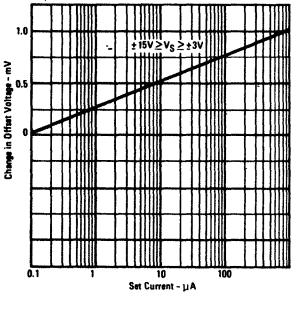
INPUT BIAS CURRENT
vs. TEMPERATURE



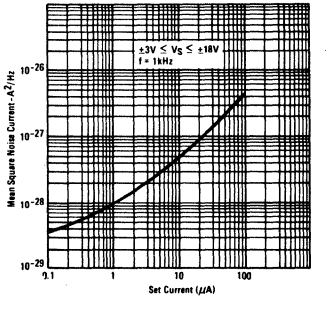
INPUT OFFSET CURRENT
vs. TEMPERATURE



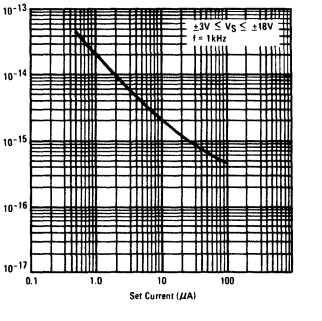
CHANGE IN OFFSET VOLTAGE
vs. I_{SET} (UNNULLED)



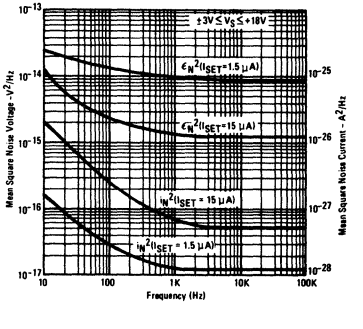
INPUT NOISE CURRENT
vs. I_{SET}



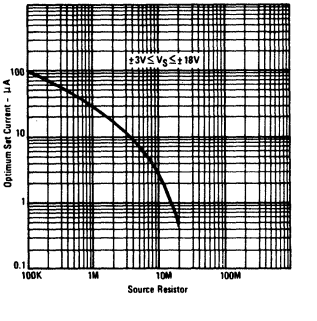
INPUT NOISE VOLTAGE
vs. I_{SET}



INPUT NOISE VOLTAGE AND CURRENT
vs. FREQUENCY

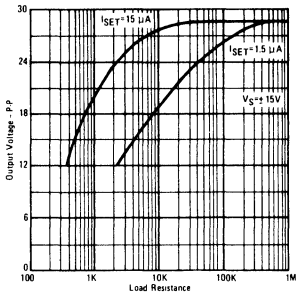


OPTIMUM SET CURRENT FOR MINIMUM
NOISE vs. SOURCE RESISTOR

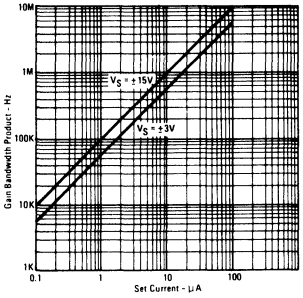


UNLESS OTHERWISE NOTED: $T_A = +25^oC$, $V_S = \pm 15VDC$

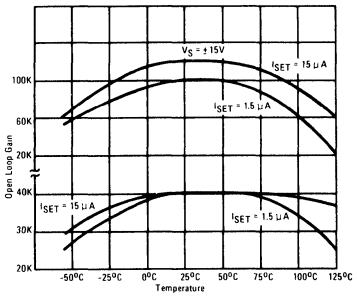
MAXIMUM OUTPUT VOLTAGE SWING
vs. LOAD RESISTANCE



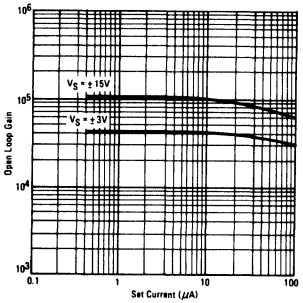
GAIN BANDWIDTH PRODUCT
vs. I_{SET}



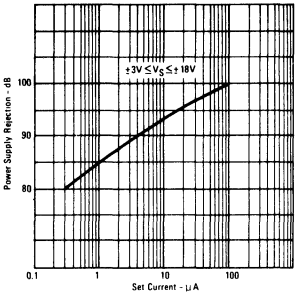
OPEN LOOP VOLTAGE GAIN
vs. TEMPERATURE



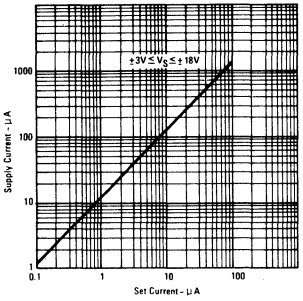
OPEN LOOP VOLTAGE GAIN
vs. I_{SET}



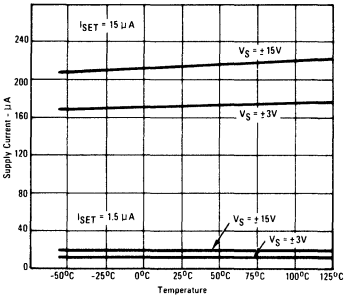
POWER SUPPLY REJECTION
vs. I_{SET}



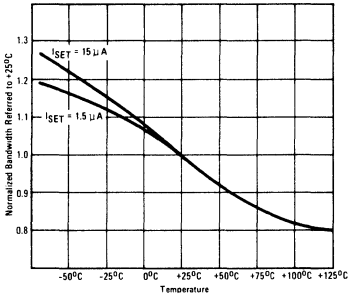
STANDBY SUPPLY CURRENT
vs. I_{SET}



SUPPLY CURRENT vs.
TEMPERATURE



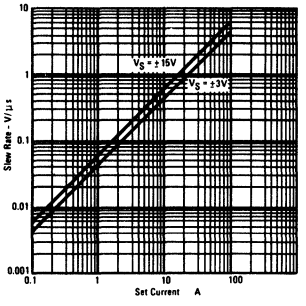
NORMALIZED BANDWIDTH
vs. TEMPERATURE



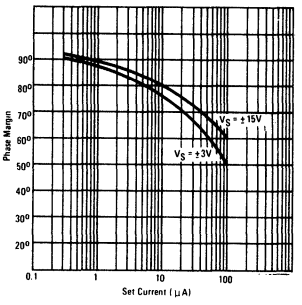
2

PERFORMANCE CURVES

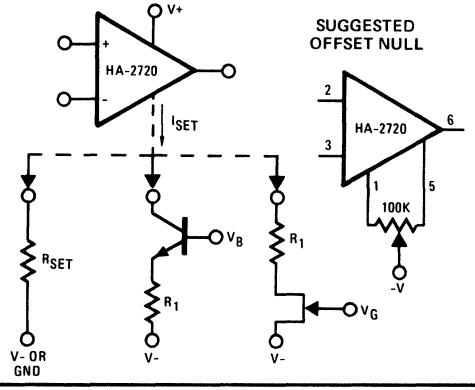
SLEW RATE vs. I_{SET}



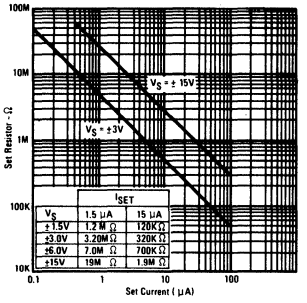
PHASE MARGIN vs. SET CURRENT



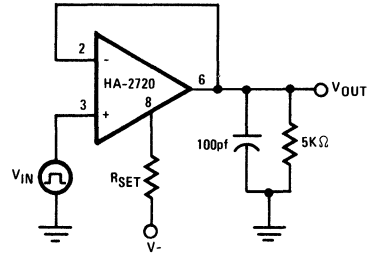
TYPICAL BIASING CIRCUITS



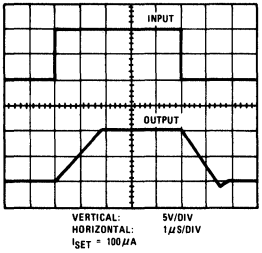
SET CURRENT VS. SET RESISTOR



TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEWING WAVEFORM



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2730/35

Wide Range Dual Programmable Operational Amplifier

FEATURES

- WIDE PROGRAMMING RANGE

SET CURRENT	0.1 TO 100μA
SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE $+1.2$ TO $+18$V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2730/2735 Dual Programmable Amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. Each amplifier on the chip can be adjusted independently. This versatile adjustment capability enables HA-2730/2735 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2730/2735 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

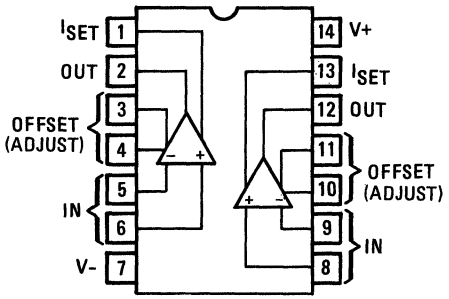
A major advantage of HA-2730/2735 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipement. A primary application for HA-2730/2735 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2730/2735 can be used for designs such as current controlled oscillators, modulators, sample and hold circuits and variable active filters.

HA-2730 is guaranteed over -55°C to +125°C. HA-2735 is specified from 0°C to +75°C. Both parts are available in 14 lead D.I.P. package or dice form.

PINOUT

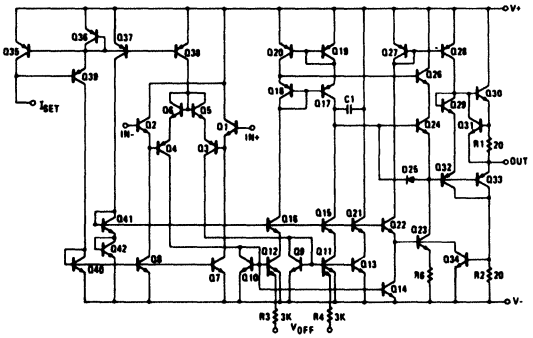
Package Code 4U

Top View



NOTE: Bottom of package is connected to V-

SCHEMATIC



(ONE HALF ONLY)
HA-2730/35

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	500mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2730	$-55^{o}C \leq T_A \leq +125^{o}C$
I_{SET} (Current at I_{SET})	500μA	HA-2735	$0^{o}C \leq T_A \leq +75^{o}C$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +3.0V, V- = -3.0V

		HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Notes 3 & 9)	25°C	20K	40K		20K	40K		15K	40K		15K	40K		V/V
	Full	15K			15K			10K			10K			V/V
*Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current (Each Amp)	25°C		15			170			15			170		μA
	Full			20			200			20			200	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

*100% Tested For DASH 8

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
*Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
*Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Notes 3 & 9)	25°C	40K	100K		40K	120K		25K	100K		25K	120K		V/V
	Full	25K			25K			20K			20K			V/V
*Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current (Each Amp)	25°C		20			210			20			210		μA
	Full			25			250			25			250	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

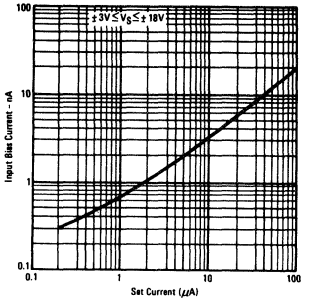
NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above 68°C.

	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	RR$_L$ = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

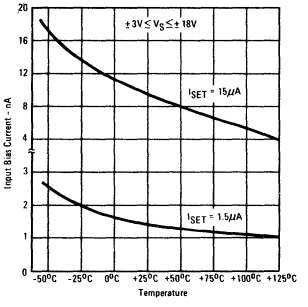
*100% Tested For DASH 8

UNLESS OTHERWISE NOTED: $T_A = 25^oC$, $V_S = \pm 15VDC$

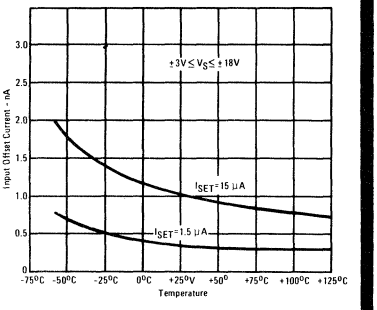
INPUT BIAS CURRENT
vs. SET CURRENT



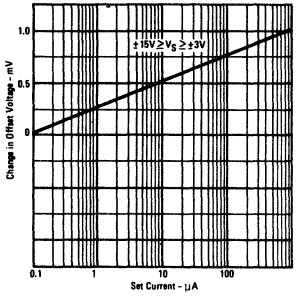
INPUT BIAS CURRENT
vs. TEMPERATURE



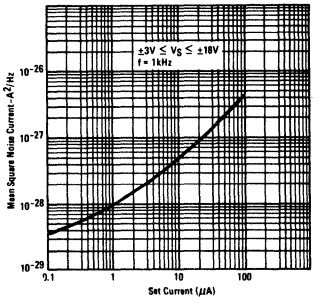
INPUT OFFSET CURRENT
vs. TEMPERATURE



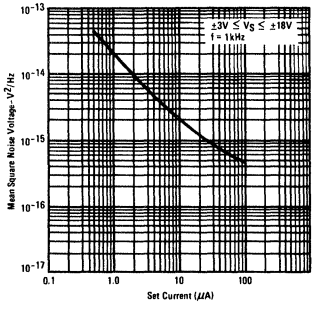
CHANGE IN OFFSET VOLTAGE
vs. I_{SET} (UNNULLED)



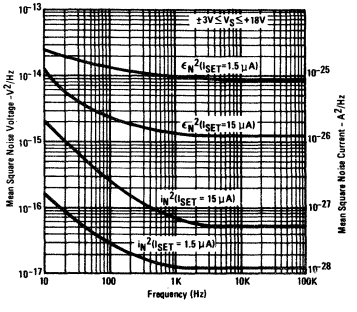
INPUT NOISE CURRENT
vs. I_{SET}



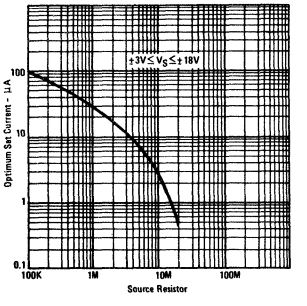
INPUT NOISE VOLTAGE
vs. I_{SET}



INPUT NOISE VOLTAGE AND CURRENT
vs. FREQUENCY

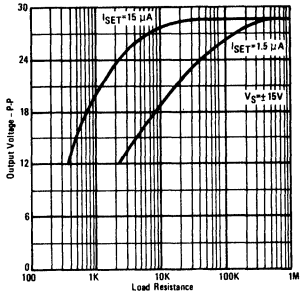


OPTIMUM SET CURRENT FOR MINIMUM
NOISE vs. SOURCE RESISTOR

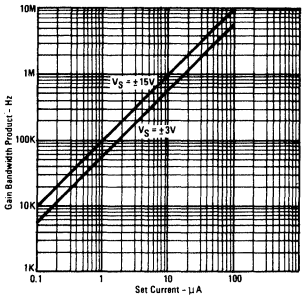


UNLESS OTHERWISE NOTED: $T_A = 25^oC$, $V_S = \pm 15VDC$

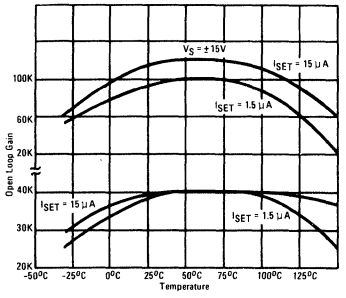
MAXIMUM OUTPUT VOLTAGE SWING
vs. LOAD RESISTANCE



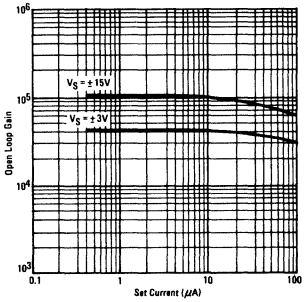
GAIN BANDWIDTH PRODUCT
vs. I_{SET}



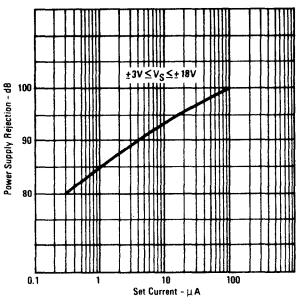
OPEN LOOP VOLTAGE GAIN
vs. TEMPERATURE



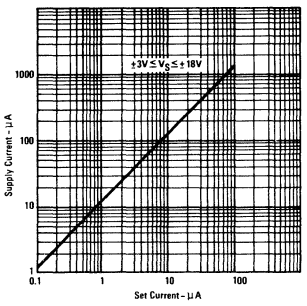
OPEN LOOP VOLTAGE GAIN
vs. I_{SET}



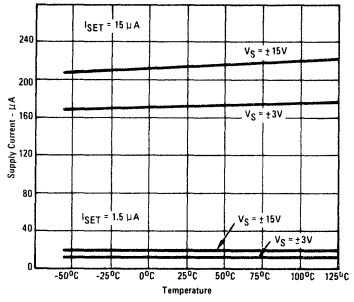
POWER SUPPLY REJECTION
vs. I_{SET}



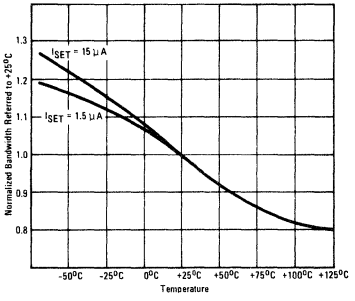
STANDBY SUPPLY CURRENT
vs. I_{SET}



SUPPLY CURRENT vs.
TEMPERATURE

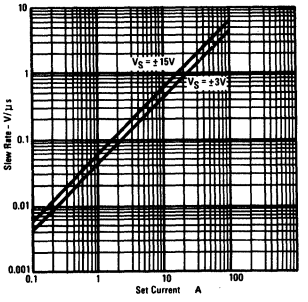


NORMALIZED BANDWIDTH
vs. TEMPERATURE

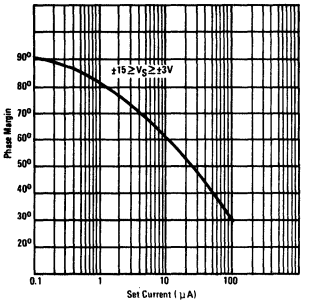


PERFORMANCE CURVES

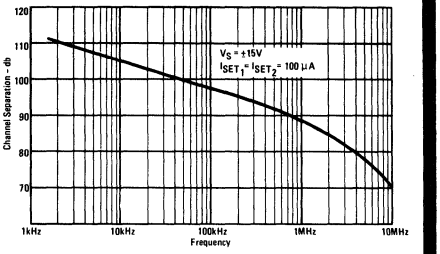
SLEW RATE vs. I_{SET}



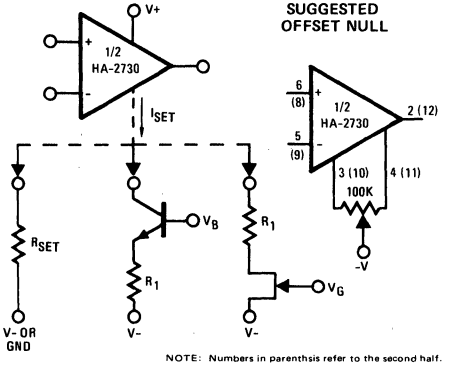
PHASE MARGIN vs. SET CURRENT



CHANNEL SEPARATION vs. FREQUENCY

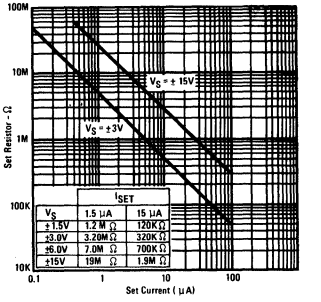


TYPICAL BIASING CIRCUITS



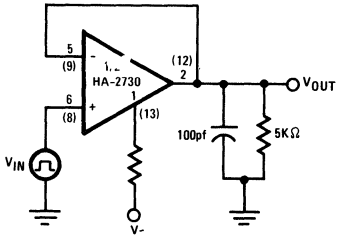
NOTE: Numbers in parenthsis refer to the second half.

SET CURRENT VS. SET RESISTOR



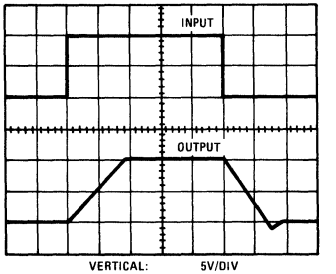
V_S	I_{SET} 1.5 µA	15 µA
±1.5V	1.2 MΩ	120KΩ
±3.0V	3.20MΩ	320KΩ
±6.0V	7.0MΩ	700KΩ
±15V	19MΩ	1.9MΩ

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



NOTE: Numbers in parenthsis refer to the second half.

SLEWING WAVEFORM



VERTICAL: 5V/DIV
HORIZONTAL: 1µS/DIV
I_{SET} = 100µA

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2900/04/05

Chopper Stabilized Operational Amplifier

FEATURES

- OFFSET VOLTAGE DRIFT — 0.2 μV/°C
- OFFSET CURRENT DRIFT — 1pA/°C
- OPEN LOOP GAIN — 5×10^8
- BANDWIDTH — 3MHz
- SLEW RATE — 2.5V/μs
- TRUE DIFFERENTIAL INPUTS

APPLICATIONS

- HIGH-GAIN DC INSTRUMENTATION
- HIGH-ACCURACY WEIGHING EQUIPMENT
- BIOMEDICAL AMPLIFIERS
- PRECISION INTEGRATORS AND TIMERS

DESCRIPTION

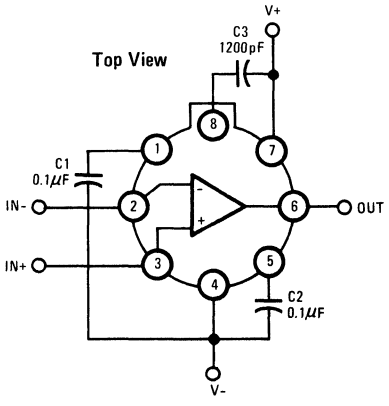
HA-2900/2904/2905 are monolithic chopper-stabilized operational amplifiers that employ dielectric isolation achieving superior offset drift, extremely low input currents and excellent AC performance. Input drift is characterized by offset voltage drift of 0.2 μV/°C and offset current drift of 1pA/°C. Initial offset voltage is only 20 μV while offset current is 50pA. These input specifications make HA-2900/2904/2905 ideally suited to high accuracy applications such as high-gain DC instrumentation, and precision integration. The amplifiers can be used to replace other op amps in designs where much lower errors are required without external adjustments. 3MHz gain-bandwidth product makes HA-2900/2904/2905 valuable for processing wide band signals as well as for low frequency measurements.

In addition to offering high-accuracy performance, these "choppers" also offer versatility by virtue of their symmetrical, differential inputs which permit operation in any op amp configuration – inverting, non-inverting or balanced. These devices require only three external capacitors for proper operation.

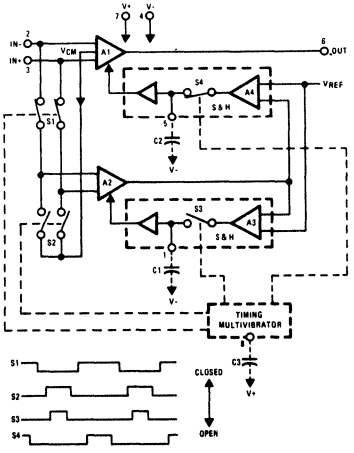
HA-2900 is guaranteed over -55°C to +125°C; HA-2904 operates from -25°C to +85°C; HA-2905 operates from 0°C to +75°C. All devices are available in a hermetically sealed metal can.

PINOUT AND SUGGESTED HOOKUP

TO-99 — **Package Code 2E**



FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	42.0V	Operating Temperature Range	$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2900)
Differential Input Voltage (Note 1)	±15V		$-25^{o}C \leq T_A \leq +85^{o}C$ (HA-2904)
Output Current/Full Short Circuit Protection		Storage Temperature Range	$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2905)
Internal Power Dissipation	300mW*		$-65^{o}C \leq T_A \leq +150^{o}C$

*Derate by 6.6mW/^{o}C above +105^{o}C

ELECTRICAL CHARACTERISTICS

Test Conditions: C1 = C2 = 0.1μF, C3 = 1500pF, V_{Supply} = ±15.0V unless otherwise specified.

PARAMETER	TEMP.	HA-2900 -55°C to +125°C MIN.	HA-2900 TYP.	HA-2900 MAX.	HA-2904 -25°C to +85°C MIN.	HA-2904 TYP.	HA-2904 MAX.	HA-2905 0°C to +75°C MIN.	HA-2905 TYP.	HA-2905 MAX.	UNITS
INPUT CHARACTERISTICS											
*Offset Voltage	+25°C		20			20			20		µV
	Full			60			50			80	µV
Offset Voltage Average Drift	Full		0.3	0.6		0.2	0.4		0.2		µV/°C
*Bias Current	+25°C		150			150			150		pA
	Full			1,000			1,000			1,000	pA
*Offset Current	+25°C		50			50			50		pA
	Full			500			500			500	pA
Offset Current Average Drift	Full		1	4		1	3		1		pA/°C
Input Resistance	+25°C		100			100			100		MΩ
Input Capacitance	+25°C		10			10			10		pF
Common Mode Range	Full	±10			±10			±10			V
TRANSFER CHARACTERISTICS											
*Large Signal Voltage Gain (Note 2)	+25°C		$5x10^8$			5×10^8			5×10^8		V/V
	Full	10^6			10^7			10^6			V/V
Chopper Frequency	+25°C		750			750			750		Hz
*Common Mode Rejection Ratio (Note 3)	Full	120	160		130	160		120	160		dB
Gain Bandwidth Product (Note 4)	+25°C		3			3			3		MHz
OUTPUT CHARACTERISTICS											
*Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		±10	±12		V
*Output Current	+25°C	±10			±10			±7			mA
Output Resistance	Full		200			200			200		Ω
Full Power Bandwidth (Note 5)	+25°C		40			40			40		kHz
TRANSIENT RESPONSE (NOTES 2, 8, and 9)											
Rise Time (Note 6)	+25°C		200			200			200		ns
Overshoot (Note 6)	+25°C		20			20			20		%
Slew Rate (Note 5)	+25°C		2.5			2.5			2.5		V/µs
POWER SUPPLY CHARACTERISTICS											
*Supply Current	+25°C		3.5	5.0		3.5	5.0		3.5	5.0	mA
*Supply Voltage Range	Full	±12		±20	±10		±20	±12		±20	V
*Power Supply Rejection Ratio (Note 7)	Full	120	160		130	160		120	160		dB

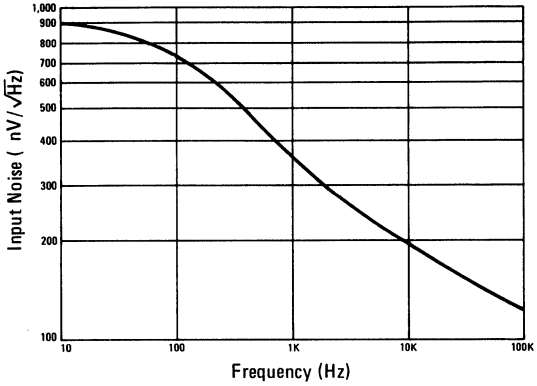
NOTES:
1. Input terminals should be protected against static discharge during handling and installation. Input voltage should never exceed supply voltages.
2. R_L = 2K
3. V_{CM} = ±5.0V
4. A_V = 10
5. V_O = ±10V
6. V_O = ±200mV
7. ΔV_S = ±5V
8. C_L = 50pF
9. A_V = +1 See transient response test circuits and waveforms, page 4.

*100% Tested For DASH 8

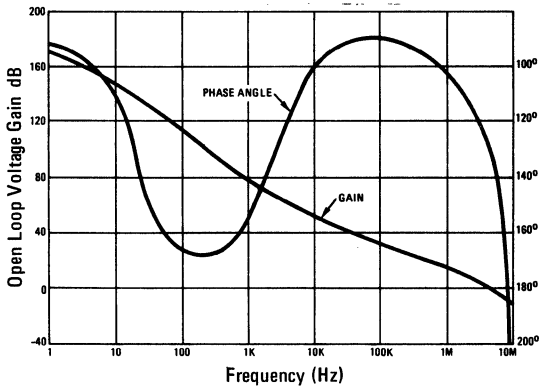
PERFORMANCE CURVES

$V+ = V- = 15VDC$, $T_A = 25^oC$ UNLESS OTHERWISE STATED

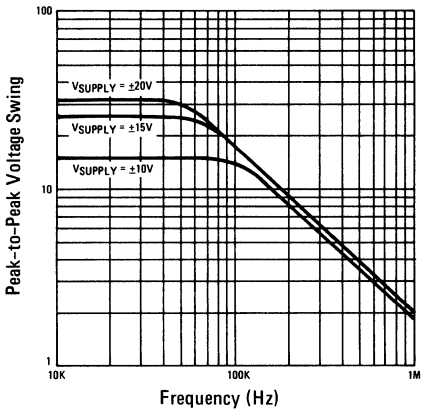
INPUT VOLTAGE NOISE



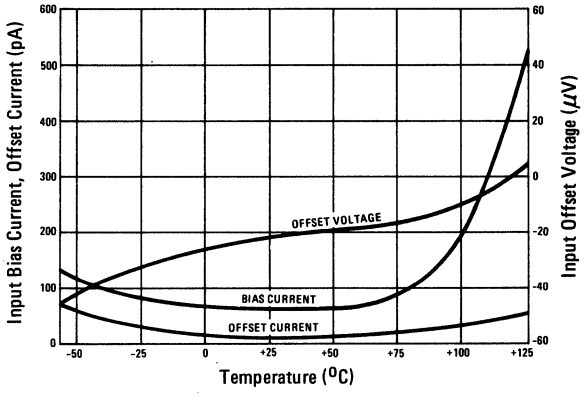
OPEN LOOP FREQUENCY AND PHASE RESPONSE



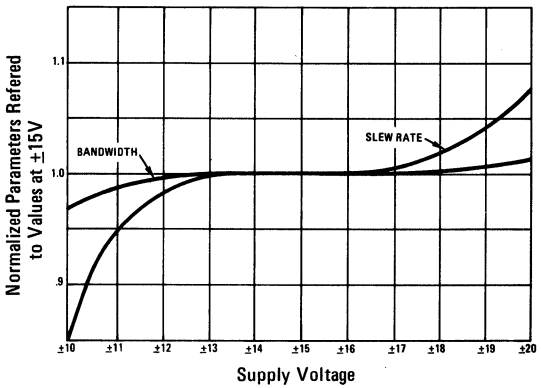
OUTPUT VOLTAGE SWING vs. FREQUENCY



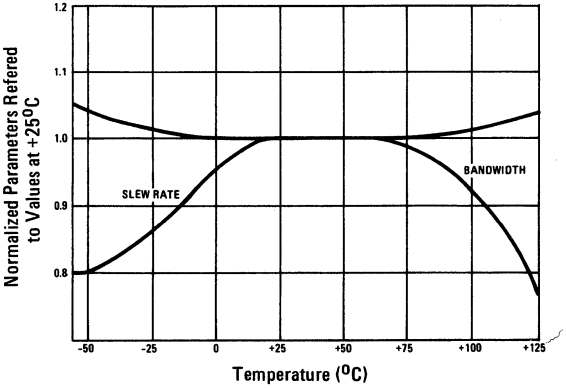
TYPICAL INPUT CHARACTERISTICS vs. TEMPERATURE



NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE

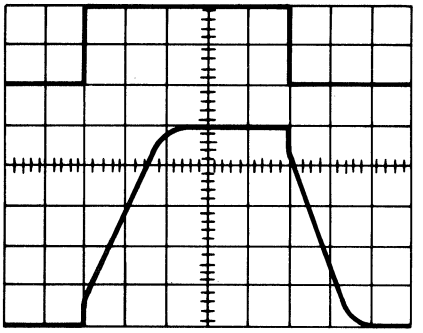


NORMALIZED A.C. PARAMETERS vs. TEMPERATURE



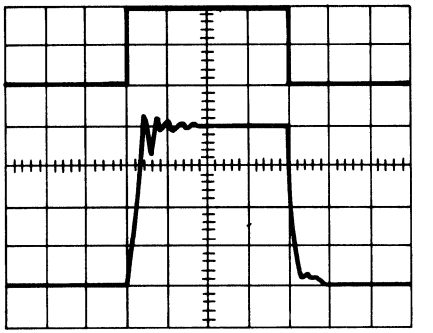
PERFORMANCE CURVES (continued)

VOLTAGE FOLLOWER
SLEWING WAVEFORM



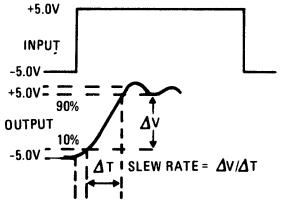
Upper Trace: Input: 5V/Div.
Lower Trace: Output; 2V/Div.
Horizontal: 2μS/Div.

VOLTAGE FOLLOWER
TRANSIENT RESPONSE WAVEFORM

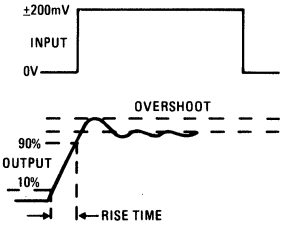


Upper Trace: Input; 100mV/Div.
Lower Trace: Output; 50mV/Div.
Horizontal: 500ns/Div.

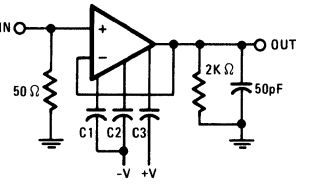
SLEW RATE



TRANSIENT RESPONSE



SLEW RATE AND
TRANSIENT RESPONSE



NOTE: Measured on both positive and negative transitions.

APPLICATION TIPS

(1) Device inputs should be protected against exceeding either supply voltage from static discharge or inadvertent connection, particularly when wired directly to a connector or instrument panel.

(2) External capacitors C1, C2, and C3 should have good temperature stability, low leakage, and low dielectric absorption. Polystyrene (below +85°C), teflon types or polycarbonate are recommended. C3 could also be silver mica.

(3) Particular care must be exercised in system layout and material and component selection to realize the full performance potential of the HA-2900/2904/2905. External sources of drift error may include the thermocouple and electrochemical EMF's generated at junctions of dissimilar metals, leakage across insulating materials, static charges created by moving air, and improper grounding and shielding practices.

(4) Chopper noise is present chiefly as a common mode input current signal, and may be minimized by matching the impedances at the two inputs. Random noise may be reduced at the expense of bandwidth using active or passive filtering.

(5) Input frequencies near the chopper frequency (750Hz) or its harmonics may result in small components of difference frequency in the output. This effect should be checked in the individual application, and if objectionable, a low pass filter may be added in series with the input.

(6) When operating at closed loop gains between 70 dB and 140 dB, compensation networks may be required, because of open loop phase shift in this gain region. In most cases, a capacitor placed in parallel with the feedback resistor to yield a gain-bandwidth product < 2MHz will be sufficient.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-4602/4605

High Performance Quad Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE 0.3mV
- HIGH SLEW RATE ±4V/μs
- WIDE BANDWIDTH 8MHz
- LOW DRIFT 2μV/°C
- FAST SETTLING (0.01%, 10V STEP) 4.2μs
- LOW POWER CONSUMPTION 35mW/AMP
- SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

- HIGH Q, WIDE BAND FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- DATA ACQUISITION SYSTEMS
- INTEGRATORS
- ABSOLUTE VALUE CIRCUITS
- TONE DETECTORS

DESCRIPTION

The HA-4602 and HA-4605 are high performance dielectrically isolated monolithic quad operational amplifiers with superior specifications not previously available in a quad amplifier. These amplifiers offer excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

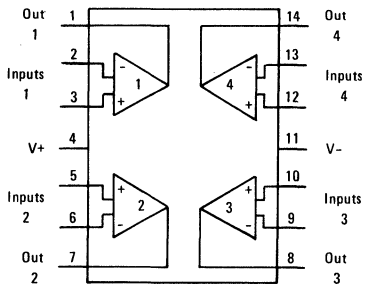
A wide range of applications can be achieved by using the features made available by the HA-4602/4605. With wide bandwidth (8MHz), low power (35mW/amp), and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise ($8nV/\sqrt{Hz}$) and excellent full power bandwidth (60kHz). The HA-4602/4605 is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2 μV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/μs) and fast settling time (4.2 μs to 0.01%, 10V step) makes these amplifiers useful components in fast, accurate data acquisition systems.

The HA-4602 and 4605's are available in 14 pin CERDIP packages which are interchangeable with most other quad op amps. HA-4602 is specified from -55°C to +125°C, and HA-4605 is specified over 0°C to +75°C range.

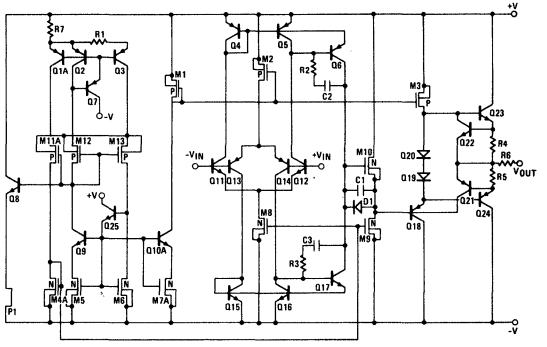
PINOUT

Package Code 4U

TOP VIEW



SCHEMATIC



ONE FOURTH ONLY (HA-4602/4605)

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V	Power Dissipation (Note 4)	880mW
Differential Input Voltage	±7V	Operating Temperature Range	
Input Voltage (Note 2)	±15.0V	HA-4602-2	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
Output Short Circuit Duration (Note 3)	Indefinite	HA-4605-5	$0^{\circ}C \leq T_A \leq +75^{\circ}C$
		Storage Temperature Range	$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS

V+ = 15V, V- = -15V

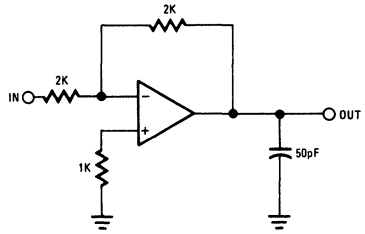
PARAMETER	TEMP.	HA-4602-2 -55°C to +125°C MIN.	TYP.	MAX.	HA-4605-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		0.3	2.5		0.5	3.5	mV
	Full			3.0			4.0	mV
Av. Offset Voltage Drift	Full		2			2		µV/°C
* Bias Current	+25°C		130	200		130	300	nA
	Full			325			400	nA
* Offset Current	+25°C		30	75		30	100	nA
	Full			125			120	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1KHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance			500			500		KΩ
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
* Common Mode Rejection Ratio (Note 9)	Full	86			80			dB
Channel Separation (Note 6)	+25°C		-108			-108		dB
Small Signal Bandwidth	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60			60		KHz
Output Current (Note 7)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		50			50		ns
Overshoot	+25°C		30			30		%
Slew Rate	+25°C		±4			±4		V/µs
Settling Time (Note 10)			4.2			4.2		µs
POWER SUPPLY CHARACTERISTICS								
* Supply Current (I^+ or I^-)	+25°C		4.6	5.5		5.0	6.5	mA
* Power Supply Rejection Ratio (Note 9)	Full	86			80			dB

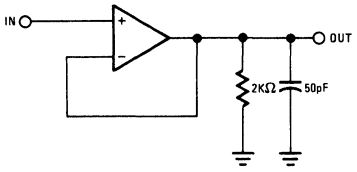
*100% tested for HA1-4602-8

NOTES

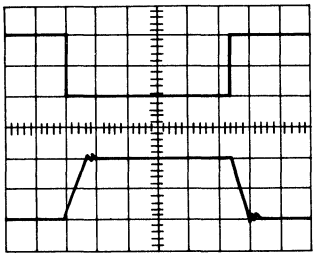
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 2K ohms.
6. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak-to-peak; R_S = 1K ohms. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
7. Output current is measured with V_{OUT} = ±5 volts. The output current specified can also be applied to V_{OUT} = ±10V.
8. For transient response test circuits and measurement conditions refer to Test Circuits section of the data sheet.
9. ΔV = ±5.0 volts.
10. Settling time is measured to 0.01% of final value for a 10 volt input step, A_V = -1.

TEST CIRCUITS



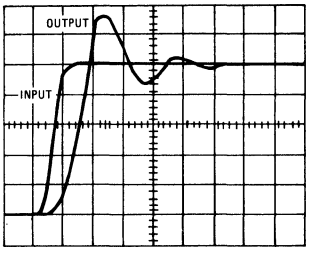


LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5μs/Div.)



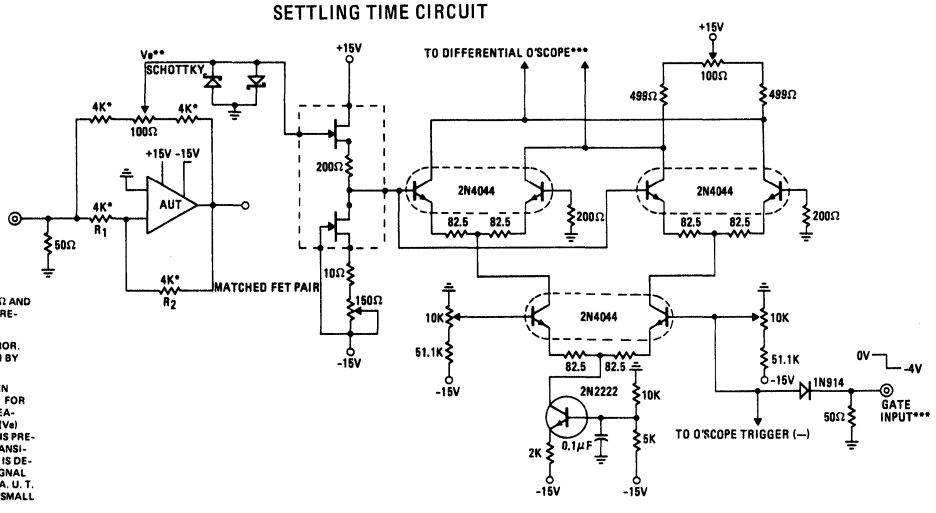
VERT. 5V/DIV.
HORZ. 5 μs/DIV.

SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.)



HORIZONTAL: 50 NSEC/DIV.
VERTICAL: 10mV/DIV

SETTLING TIME CIRCUIT



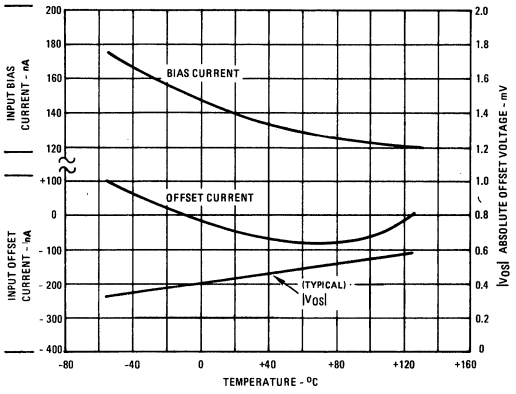
* SHOWN FOR AV = -1. USE 800Ω AND 400Ω FOR AV = -5, AV = -10, RESPECTIVELY.

** THIS IS SUMMING POINT ERROR. OUTPUT ERROR, ε, IS GIVEN BY ε = (1 + AV) Ve.

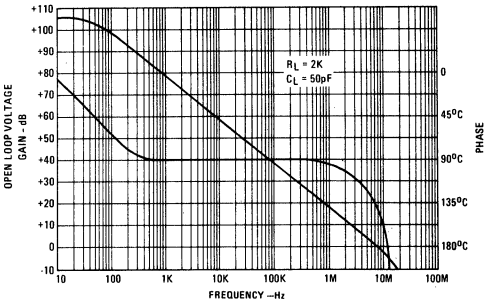
*** MEASUREMENT IS 5 × Ve WHEN GATE INPUT IS "LOW" (-4V). FOR GATE INPUT "HIGH" (0V), MEASUREMENT IGNORES INPUT (Ve) SO THAT SCOPE OVERLOAD IS PREVENTED DURING LARGE TRANSITIONS. GATE INPUT SIGNAL IS DELAYED WITH RESPECT TO SIGNAL INPUT TO ALLOW TIME FOR A. U. T. SLEWING AND SETTLING TO SMALL ERROR VOLTAGES.

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

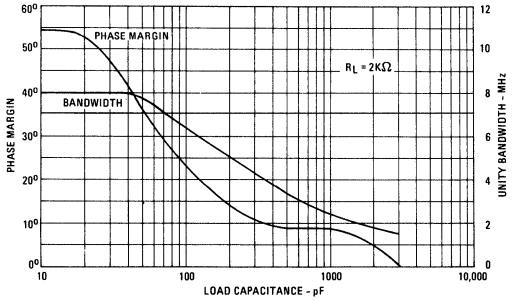
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



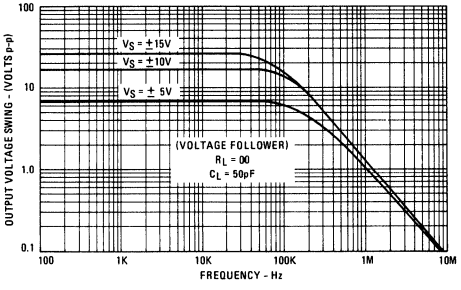
OPEN LOOP FREQUENCY RESPONSE



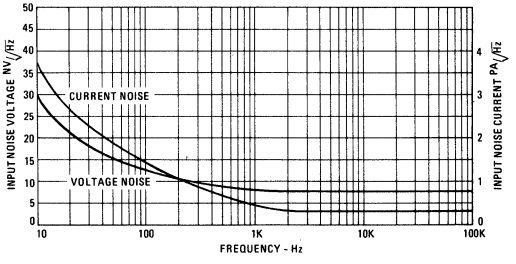
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



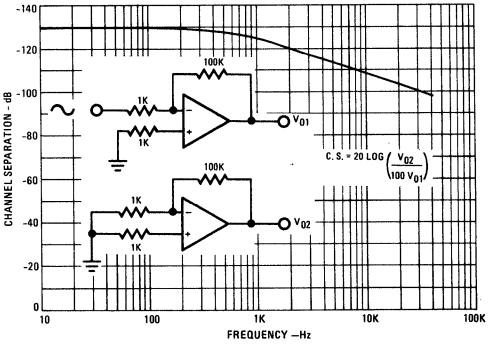
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



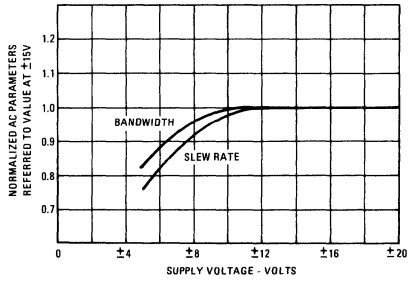
INPUT NOISE VS. FREQUENCY



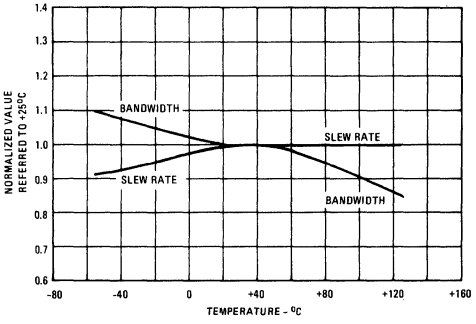
CHANNEL SEPARATION VS. FREQUENCY



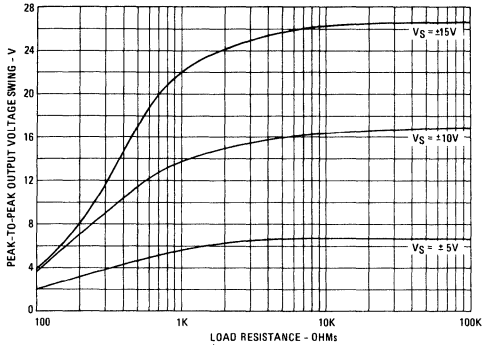
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



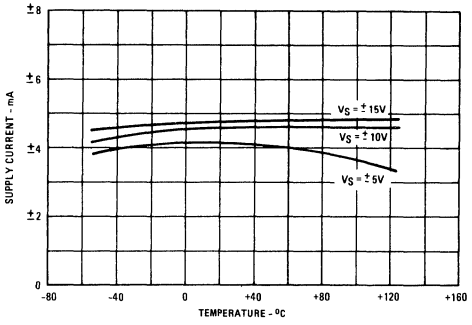
NORMALIZED AC PARAMETERS VS. TEMPERATURE



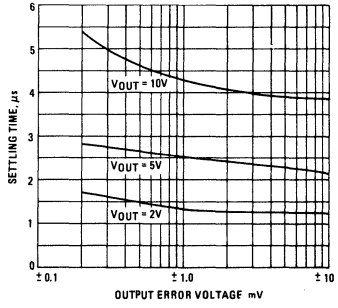
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



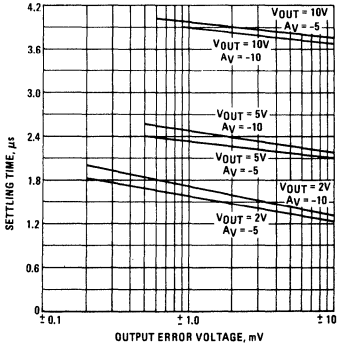
POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



SETTLING TIME VS. OUTPUT AMPLITUDE (A_V = -1)



SETTLING TIME VS. OUTPUT AMPLITUDE AND SIGNAL GAIN (A_V = -5 AND A_V = -10)



2

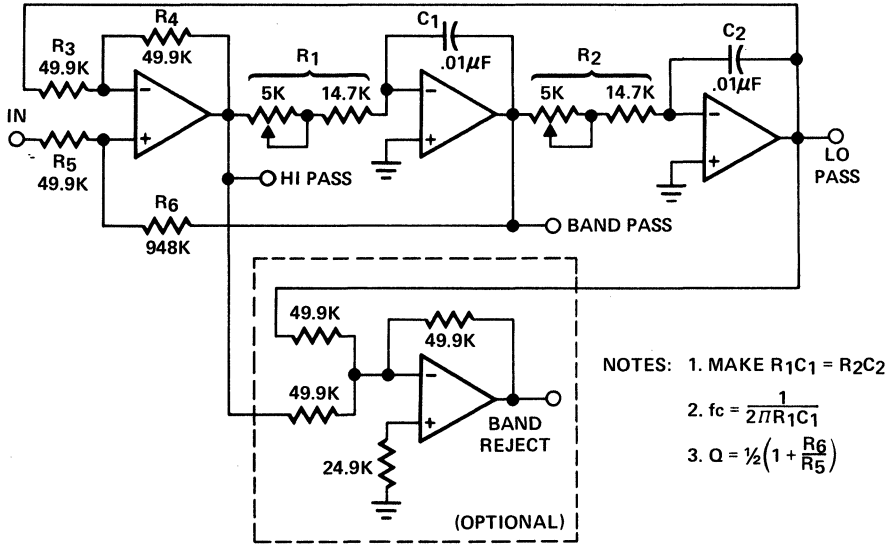
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. UNUSED OP AMPS: Unused op amp sections should be connected in a non-inverting follower configuration with the (+) input tied to ground in order to insure optimum performance of devices being used.

3. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

APPLICATIONS

2ND ORDER STATE VARIABLE FILTER (1kHz, Q = 10)



NOTES: 1. MAKE $R_1C_1 = R_2C_2$

2. $fc = \frac{1}{2\pi R_1 C_1}$

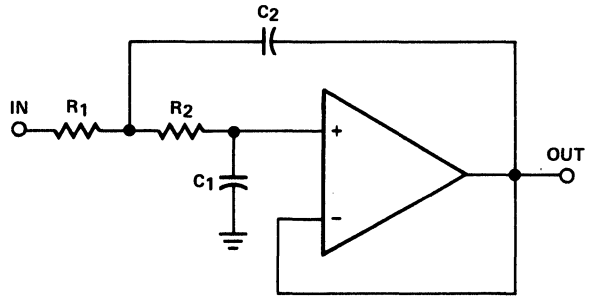
3. $Q = \frac{1}{2}\left(1 + \frac{R_6}{R_5}\right)$

The state variable filter is relatively insensitive to component changes (changes can be adjusted out with potentiometers) and also has low sensitivity to amplifier bandwidths. (Amplifier gain bandwidth product should be $\gg Q \times f_C$). The bandwidth criteria will determine whether a general purpose op amp like Harris HA-4741 or the wide band HA-4602/4605 should be used.

This filter finds wide application because multiple filtering functions are available simultaneously (High pass, Lo pass, Band pass, Band reject). In this circuit the various RC products are matched with pot adjustments allowing for non-interactive adjustment of Q and f_C. This allows capacitors (C_1, C_2) with loose tolerances to be used. To tune for f_C, apply a sine wave at f_C to the input, adjust R_1 for equal amplitudes at the Hi pass and Band pass terminals (they will be phased 90° apart) then adjust R_2 for equal amplitudes at the Band pass and Lo pass terminals.

The state variable filter is often used as building blocks in multiple pole Butterworth of Chebyshev filters. Many references contain normalized tables indicating settings for Q and f_C of each pole-pair section.

SALLEN AND KEY 2ND ORDER LO PASS FILTER



NOTES:

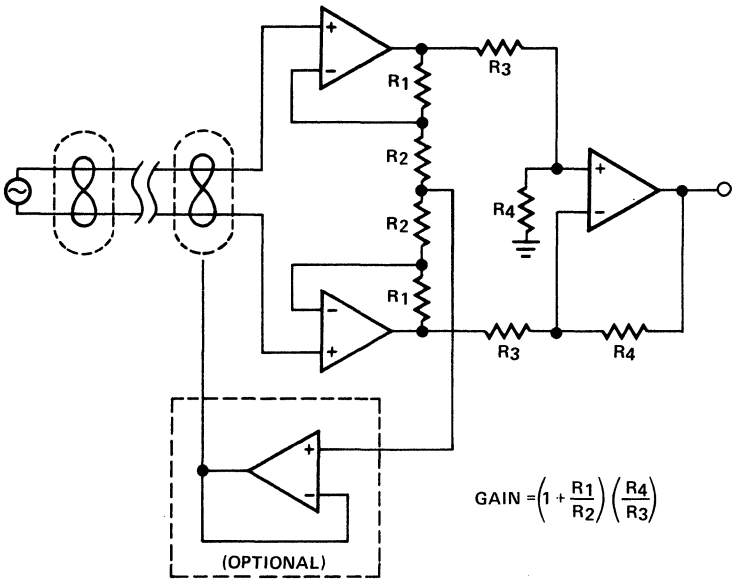
1. Make $R_1 = R_2$
2. $f_c = \frac{1}{2\pi R_1\sqrt{C_1C_2}}$
3. $Q = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}$

The advantage of using the Sallen and Key filter is simplicity, but in any application this must be weighed against the state-variable type filter for accuracy, practicality, and cost. Amplifier bandwidth limitations are much more apparent at moderate frequencies and Q values with this filter design. (For accuracy, amplifier gain-bandwidth product should be $\gg f_C \times Q^2$). The wide bandwidth of the HA-4602/4605 is particularly advantageous in this design even at audio frequencies.

In this filter all component values affect both Q and f_C. Precision, temperature stable resistors and capacitors must be used.

For economy, this filter could be used in the low Q stages of multiple-pole filter design, while the state variable type is used in the more critical stages.

INSTRUMENTATION AMPLIFIER



Instrumentation amplifiers (differential amplifiers) are specifically designed to extract and amplify small differential signals from much larger common mode voltages.

To serve as building blocks in instrumentation amplifiers, op amps must have very low offset voltage drift, high gain and wide bandwidth. The HA-4602/4605 is ideally suited for this application, delivering superior input and speed characteristics.

The optional circuitry makes use of the fourth amplifier section as a shield driver which enhances the AC common mode rejection by nullifying the effects of capacitance-to-ground mismatch between input conductors.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-4741

Quad Operational Amplifier

FEATURES

- SLEW RATE — 1.6V/μs (TYP.)
- BANDWIDTH — 3.5MHz (TYP.)
- INPUT VOLTAGE NOISE — 9nV/$\sqrt{Hz}$ (TYP.)
- INPUT OFFSET VOLTAGE — 0.5mV (TYP.)
- INPUT BIAS CURRENT — 60nA (TYP.)
- SUPPLY RANGE — ±2V TO ±20V
- NO CROSSOVER DISTORTION
- STANDARD QUAD PIN-OUT

APPLICATIONS

- UNIVERSAL ACTIVE FILTERS
- D3 COMMUNICATIONS FILTERS
- AUDIO AMPLIFIERS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

The HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

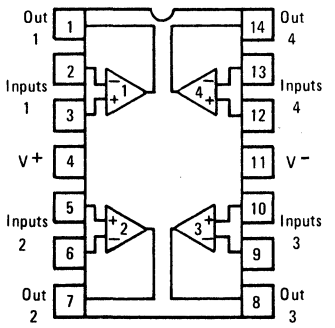
HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/ $\sqrt{Hz}$ at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion. These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (108dB at 1kHz).

A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

The HA-4741 has guaranteed operation over -55°C to +125°C and can be furnished to meet MIL-STD-883 (HA-4741-8). The HA-4741-5 is guaranteed over 0°C to +75°C and is available in ceramic and plastic dual-in-line packages and in dice form.

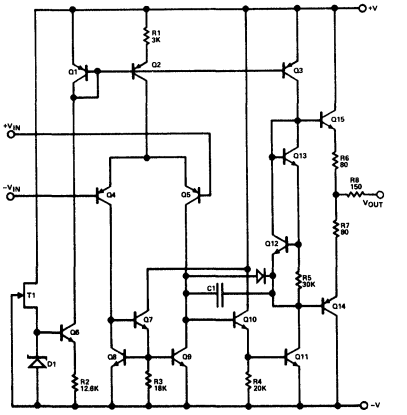
PINOUT

Package Code 4U
Package Code 3B (-5 Only)



QUAD OP AMP

SCHEMATIC



(¼) HA-4741

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V	Power Dissipation (Note 3)	880mW
Differential Input Voltage	±30.0V	Operating Temperature Range	
Input Voltage (Note 1)	±15.0V	HA-4741-2	$-55°C \leq T_A \leq +125°C$
Output Short Circuit Duration (Note 2)	Indefinite	HA-4741-5	$0°C \leq T_A \leq +75°C$
		Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS

V+ = 15V, V- = -15V

PARAMETER	TEMP.	HA-4741-2 -55°C to +125°C MIN.	TYP.	MAX.	HA-4741-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		0.5	3.0		1.0	5.0	mV
	Full		4.0	5.0		5.0	6.5	mV
Av. Offset Voltage Drift	Full		5			5		µV/°C
* Bias Current	+25°C		60	200		60	300	nA
	Full			325			400	nA
* Offset Current	+25°C		15	30		30	50	nA
	Full			75			100	nA
Common Mode Range	Full	±12			±12			V
Differential Input Resistance	+25°C		5			5		MΩ
Input Noise Voltage (f = 1KHz)	+25°C		9			9		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 4)	+25°C	50K	100K		25K	50K		V/V
	Full	25K			15K			V/V
* Common Mode Rejection Ratio (Note 8)	+25°C	80			80			dB
	Full	74			74			dB
Channel Separation (Note 5)	+25°C		-108			-108		dB
Small Signal Bandwidth	+25°C		3.5			3.5		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (R_L = 10K)	Full	±12	±13.7		±12	±13.7		V
(R_L = 2K)	Full	±10	±12.5		±10	±12.5		V
Full Power Bandwidth (Note 4)	+25°C		25			25		KHz
Output Current (Note 6)	Full	±5	±15		±5	±15		mA
Output Resistance	+25°C		300			300		Ω
TRANSIENT RESPONSE (Note 7)								
Rise Time	+25°C		75			75		ns
Overshoot	+25°C		25			25		%
Slew Rate	+25°C		±1.6			±1.6		V/µs
POWER SUPPLY CHARACTERISTICS								
* Supply Current (I^+ or I^-)	+25°C			5.0			7.0	mA
* Power Supply Rejection Ratio (Note 8)	Full	80			80			dB

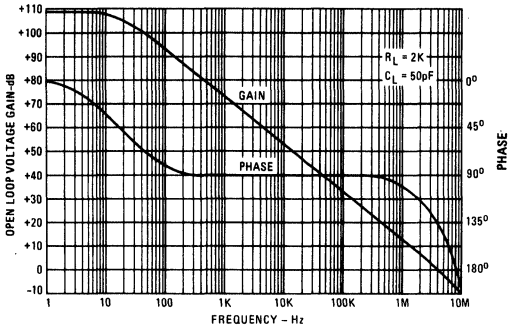
NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K
5. Referred to input; f = 10KHz, R_S = 1K
6. V_{OUT} = ±10
7. See pulse response characteristics
8. ΔV = ±5.0V

*100% Tested for DASH 8.

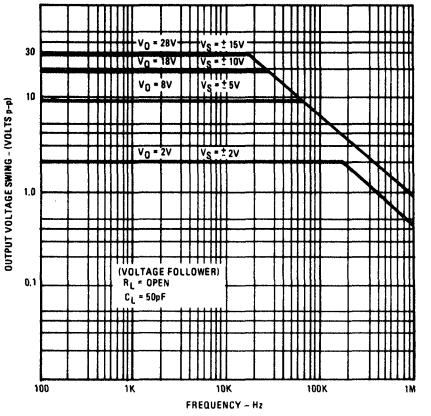
PERFORMANCE CURVES

$V+ = +15V, V^- = -15V, T_A = +25^oC$
Unless Otherwise Stated.

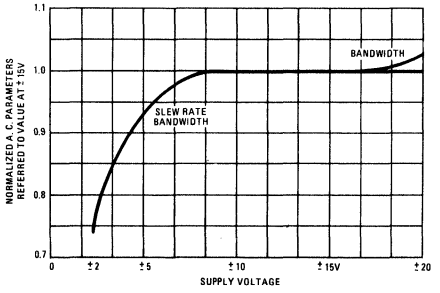
OPEN LOOP FREQUENCY RESPONSE



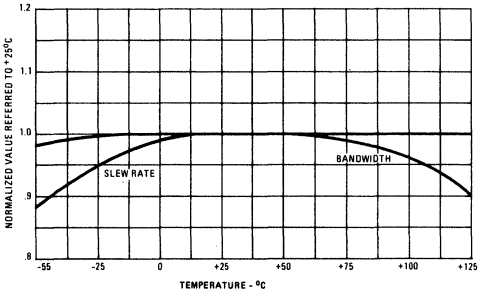
OUTPUT VOLTAGE SWING VS. FREQUENCY



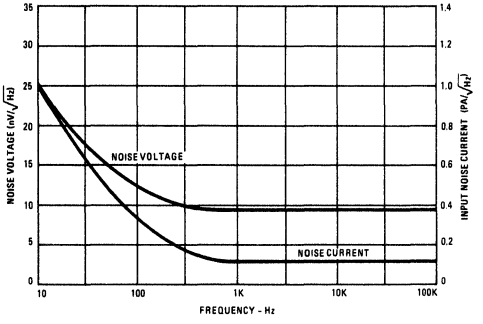
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



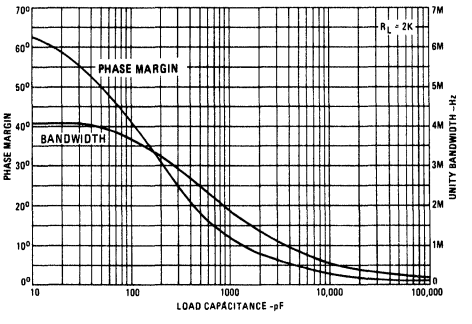
NORMALIZED AC PARAMETERS VS. TEMPERATURE



INPUT NOISE VS. FREQUENCY

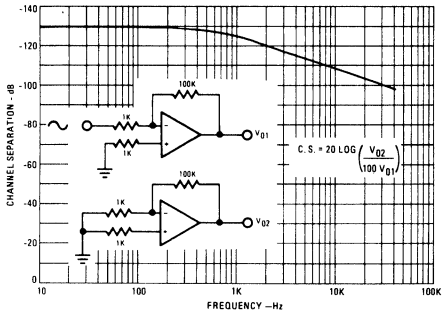


SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE

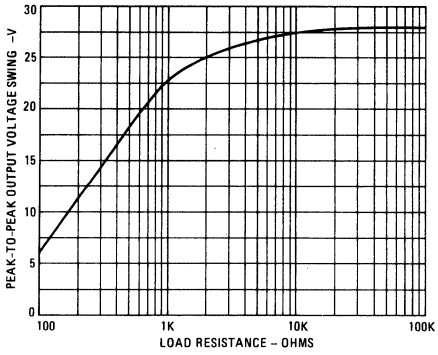


PERFORMANCE CURVES (cont'd.)

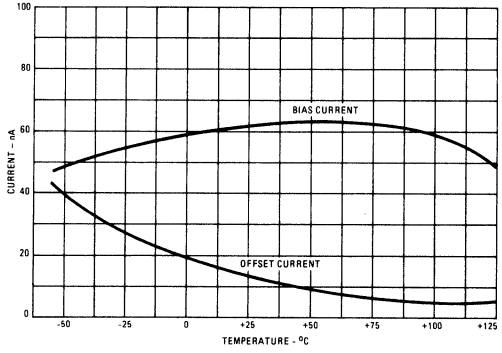
CHANNEL SEPARATION VS. FREQUENCY



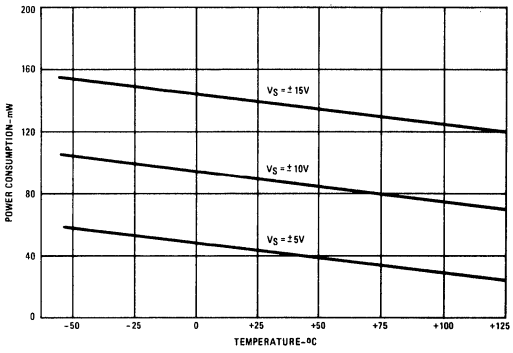
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

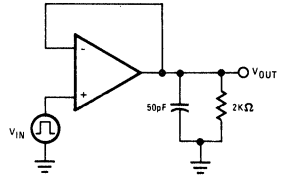


POWER CONSUMPTION VS. TEMPERATURE

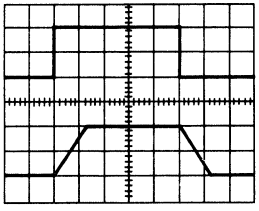


PULSE RESPONSE

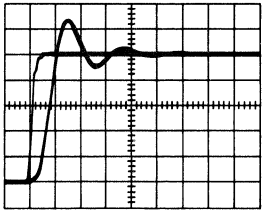
TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEW RESPONSE
(Volts: 5^{V}/Div, Time: 5μ^{s}/Div)



TRANSIENT RESPONSE
(Volts: 10^{mv}/Div , Time: 100^{ns}/Div)



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-4900/4905

Precision Quad Comparator

2

FEATURES

- FAST RESPONSE TIME 130ns
- LOW OFFSET VOLTAGE 2.0mV
- LOW OFFSET CURRENT 10nA
- SINGLE OR DUAL-VOLTAGE SUPPLY OPERATION
- SELECTABLE OUTPUT LOGIC LEVELS
- ACTIVE PULL-UP/PULL-DOWN OUTPUT CIRCUIT - NO EXTERNAL RESISTORS REQUIRED

APPLICATIONS

- THRESHOLD DETECTOR
- ZERO-CROSSING DETECTOR
- WINDOW DETECTOR
- ANALOG INTERFACES FOR MICROPROCESSORS
- HIGH STABILITY OSCILLATORS
- LOGIC SYSTEM INTERFACES

DESCRIPTION

The HA-4900/4905 are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current, and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5 volt supply (digital systems) or from dual supplies (analog networks) up to ±15 volts. The HA-4900/4905 contains a unique current driven output stage which can be connected to logic system supplies (V_{Logic}+ and V_{Logic}-) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900/4905 input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

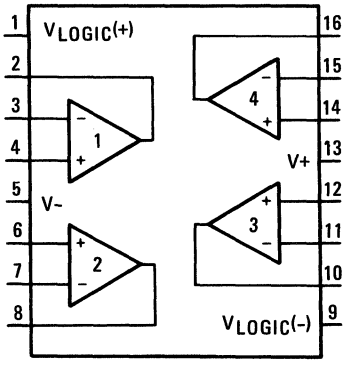
These comparators' combination of features makes them ideal components for signal detection and processing in data acquisition systems, test equipment, and microprocessor/analog signal interface networks.

Both devices are available in 16 pin dual-in-line ceramic packages. The HA-4900 operates from -55°C to +125°C and the HA-4905 operates over a 0°C to +75°C temperature range.

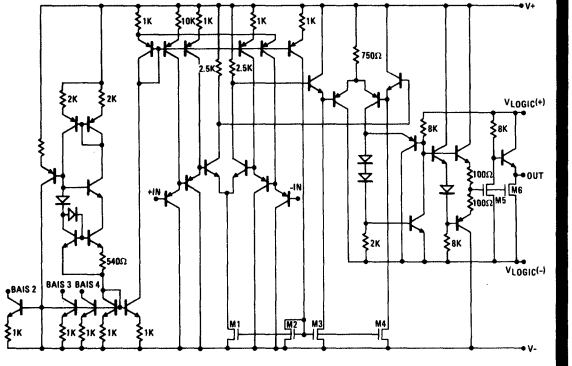
PIN OUT

Package Code 4B

Top View



SCHEMATIC



One Fourth Only (HA-4900/4905)

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	33V
Voltage Between $V_{Logic}(+)$ and $V_{Logic}(-)$	18V
Differential Input Voltage	±15V
Peak Output Current	±50mA
Internal Power Dissipation (Note 7, 8)	580mW
Storage Temperature Range	$-65^{o}C \leq T_A \leq 150^{o}C$

ELECTRICAL CHARACTERISTICS

V+ = +15.0V
V- = -15.0V
$V_{Logic}(+)$ = 5.0V
$V_{Logic}(-)$ = GND.

PARAMETER	TEMP.	HA-4900 -55°C to +125°C MIN.	HA-4900 -55°C to +125°C TYP.	HA-4900 -55°C to +125°C MAX.	HA-4905 0°C to +75°C MIN.	HA-4905 0°C to +75°C TYP.	HA-4905 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage (Note 2)	25°C		2.0	3.0		4.0	7.5	mV
	Full			4.0			10.0	mV
* Offset Current	25°C		10	25		25	50	nA
	Full			35			70	nA
* Bias Current (Note 3)	25°C		50	75		100	150	nA
	Full			150			300	nA
Input Sensitivity (Note 4)	25°C			3.1			7.6	mV
	Full			4.1			10.1	mV
* Common Mode Range	Full	V-		V+ -2.4	V-		V+ -2.4	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain	25°C		400K			400K		V/V
Response Time (T_{pd0})(Note 5)	25°C		130			130		ns
Response Time (T_{pd1})(Note 5)	25°C		180			180		ns
OUTPUT CHARACTERISTICS								
* Output Voltage Level								
Logic "Low State" (V_{OL})(Note6)	Full		0.2	0.4		0.2	0.4	V
Logic "High State" (V_{OH})(Note6)	Full	3.5	4.2		3.5	4.2		V
Output Current								
I_{Sink}	Full	3.5			3.5			mA
I_{Source}	Full	3.0			3.0			mA
POWER SUPPLY CHARACTERISTICS								
* Supply Current, $I_{ps}(+)$	25°C		6.5	12		7	13	mA
* Supply Current, $I_{ps}(-)$	25°C		4	6		5	7	mA
* Supply Current, I_{ps}(Logic)	25°C		1.7	2.0		1.7	2.5	mA
Supply Voltage Range								
V+	Full	+5.0		+15.0	+5.0		+15.0	V
V-	Full	-15.0		0	-15.0		0	V
$V_{Logic}(+)$ (Note 7)	Full	0		+15.0	0		+15.0	V
$V_{Logic}(-)$ (Note 7)	Full	-15.0		0	-15.0		0	V

*100% tested for HA1-4900-8.

NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

2. Minimum differential input voltage required to ensure a defined output state.

3. Input bias currents are essentially constant with differential input voltages up to ±9 volts. With differential input voltages from ±9 to ±15 volts, bias current on the more negative input can rise to approximately 500 μA.

4. $R_S \leq 200$ ohms; $V_{in} \leq$ Common Mode Range. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state. This parameter includes the effects of offset voltage, offset current, common mode rejection, and voltage gain.

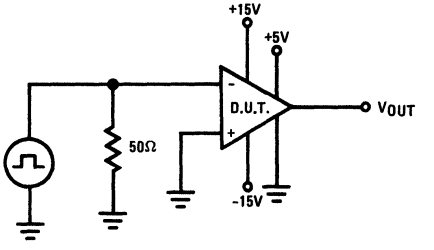
5. For $T_{pd}(1)$; 100mV input step,-5mV overdrive. For $T_{pd}(0)$; -100mV input step, 5mV overdrive. Frequency ≈ 100Hz; Duty Cycle ≈ 50%; Inverting input driven. See Test Circuit below.

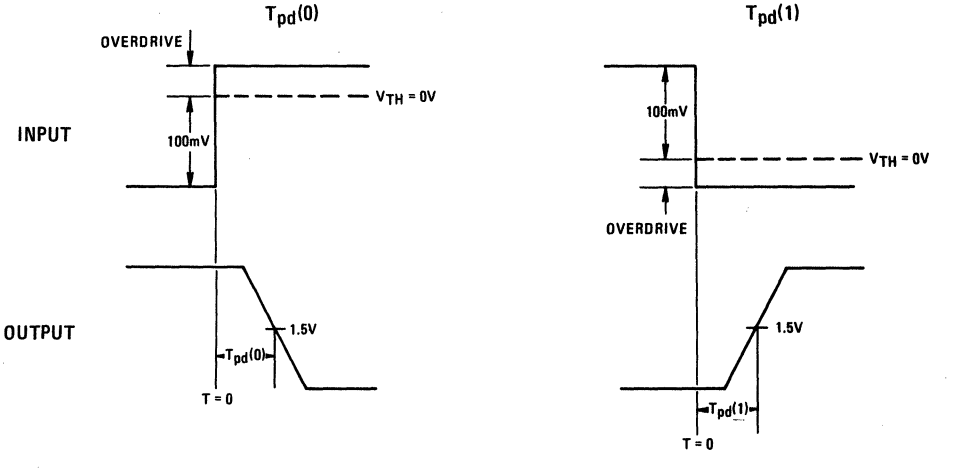
6. For V_{OH} and V_{OL}: I_{Sink} = 3.5mA, I_{Source} = 3.0mA. For other values of V_{Logic}; V_{OH} (min.) = V_{Logic} + -1.5V.

7. Total Power Dissipation (T.P.D.) is the sum of individual dissipation contributions of V+, V- and V_{Logic} shown in curves of Power Dissipation vs. Supply Voltages (see page 5). The calculated T.P.D. is then located on the graph of Maximum Allowable Package Dissipation vs. Ambient Temperature (see page 5) to determine ambient temperature operating limits imposed by the calculated T.P.D.. For instance, the combination of +15V, -15V, +5V, 0V (V+, V-, V_{Logic}+, V_{Logic}-) gives a T.P.D. of 350mW which allows operation to +125°C; the combination +15V, -15V, +15V, 0V gives a T.P.D. of 450mW and an operating limit of T_A = +95°C.

8. Derate by 5.8mW/°C above T_A = +75°C.

RESPONSE TIME TEST CIRCUITS



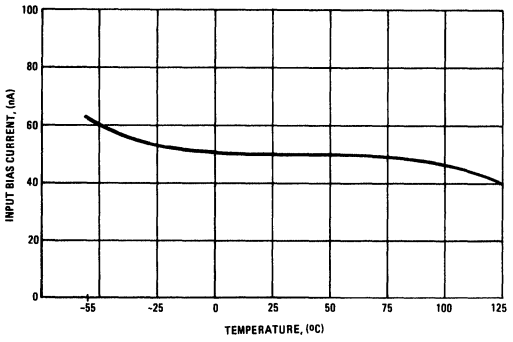


Input and output voltage waveforms for various input overdrives is shown on page 5.

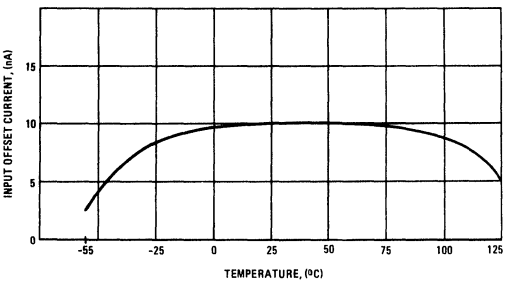
PERFORMANCE CURVES

V+ = 15V, V- = -15V, $V_{Logic}(+)$ = 5.0V, $V_{Logic}(-)$ = 0V, T_A = +25°C, Unless Otherwise Stated.

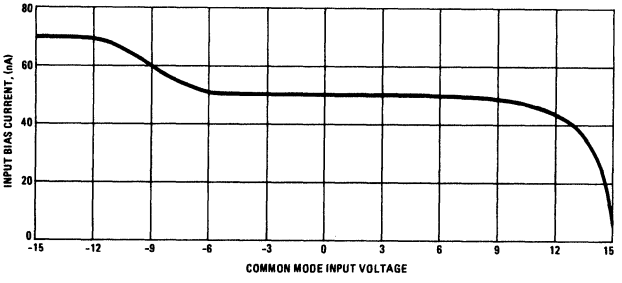
INPUT BIAS CURRENT vs. TEMPERATURE



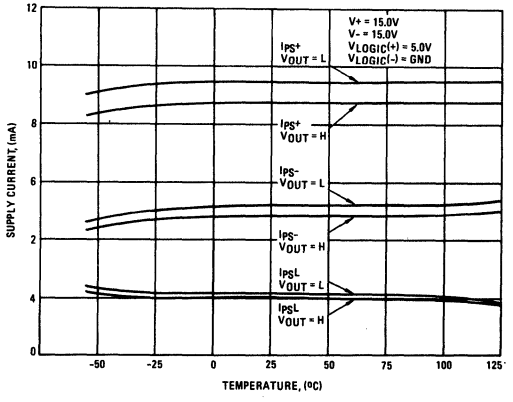
INPUT OFFSET CURRENT vs. TEMPERATURE



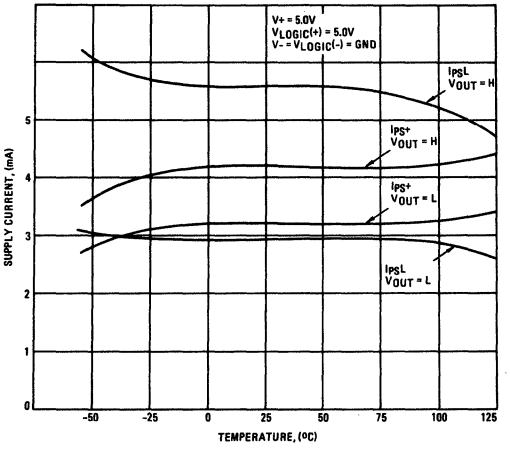
INPUT BIAS CURRENT vs. COMMON MODE INPUT VOLTAGE
($V_{DIFF.}$ = 0V)



SUPPLY CURRENT vs. TEMPERATURE
FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY

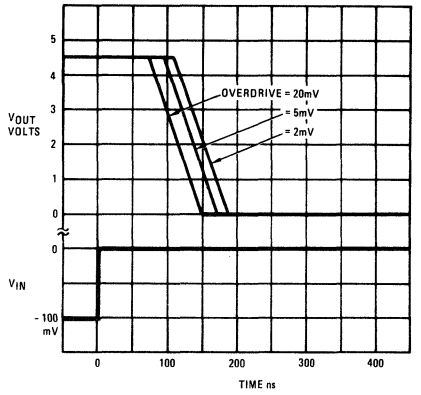


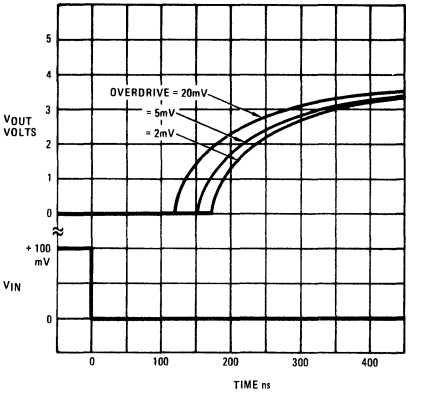
SUPPLY CURRENT vs. TEMPERATURE
FOR SINGLE +5V OPERATION



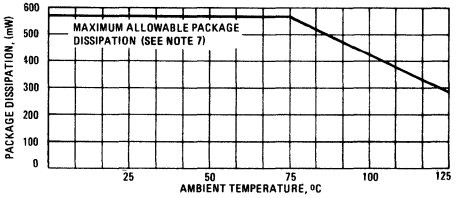
PERFORMANCE CURVES (continued)

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

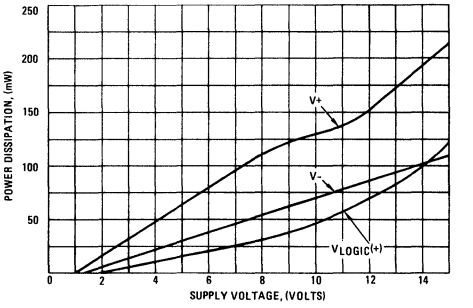




MAXIMUM PACKAGE DISSIPATION vs. $T_{AMBIENT}$



MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE (NO LOAD CONDITION)



APPLYING THE HA-4900/4905 COMPARATORS

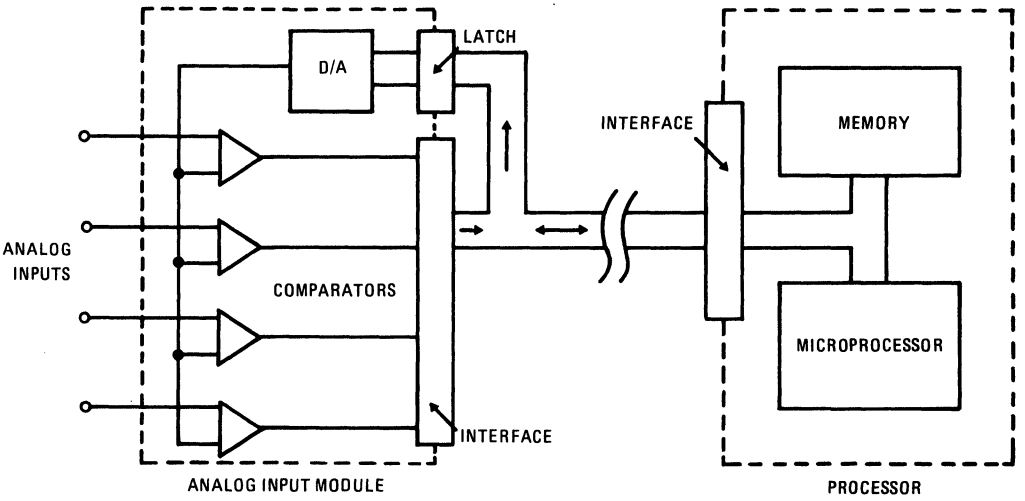
1. SUPPLY CONNECTIONS: This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to V_{Logic}+ and V_{Logic}-. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings (15V P-P, max.) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to +15V), V+ and V_{Logic}+ may be connected together to the positive supply while V- and V_{Logic}- are grounded. If an input signal could swing negative with respect the V- terminal, a resistor should be connected in series with the input to limit input current to < 5mA since the C-B junction of the input transistor would be forward biased.

2. UNUSED INPUTS: Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter".

3. CROSSTALK: Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{OS}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

4. POWER SUPPLY DECOUPLING: Decouple all power supply lines with .01 μ F ceramic capacitors to a ground line located near the package to reduce coupling between channnels or from external sources.

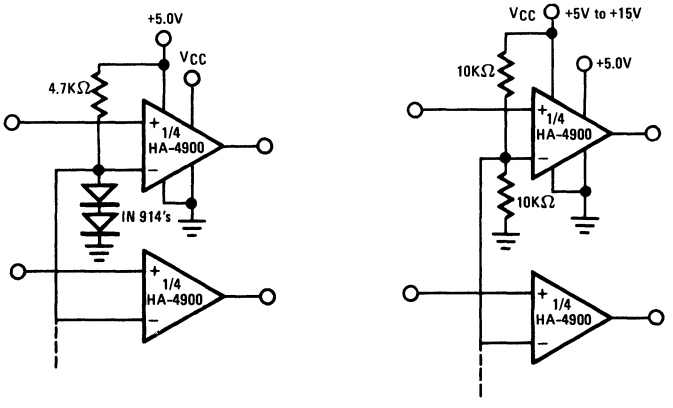
5. RESPONSE TIME: Fast rise time (< 200ns) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.



DATA ACQUISITION SYSTEM

In this circuit the HA-4900/4905 is used in conjunction with a D to A converter to form a simple, versatile, multi-channel analog input for a data acquisition system. In operation the processor first sends an address to the D to A, then the processor reads the digital word generated by the comparator outputs.

To perform a simple comparison, the processor sets the D to A to a given reference level, then examines one or more comparator outputs to determine if their inputs are above or below the reference. A window comparison consists of two such cycles with 2 reference levels set by the D to A. One way to digitize the inputs would be for the processor to increment the D to A in steps. The D to A address, as each comparator switches, is the digitized level of the input. While stairstepping the D to A is slower than successive approximation, all channels are digitized during one staircase ramp.



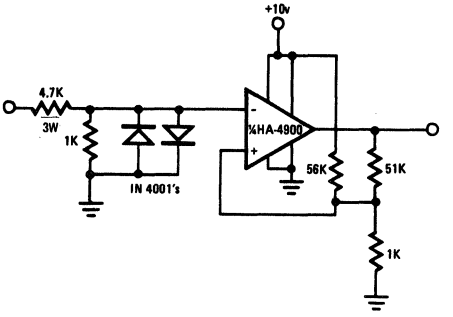
TTL TO CMOS

CMOS TO TTL

LOGIC LEVEL TRANSLATORS

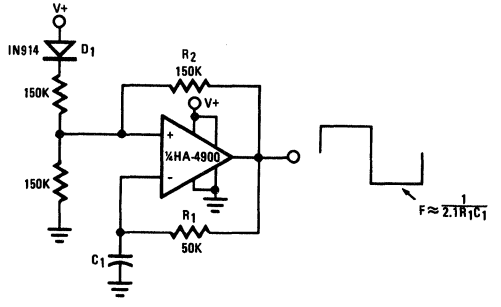
The HA-4900/4905 comparators can be used as versatile logic interface devices as shown in the circuits above. Negative logic devices may also be interfaced with appropriate supply connections.

If separate supplies are used for V- and V_{Logic}-, these logic level translators will tolerate several volts of ground line differential noise.



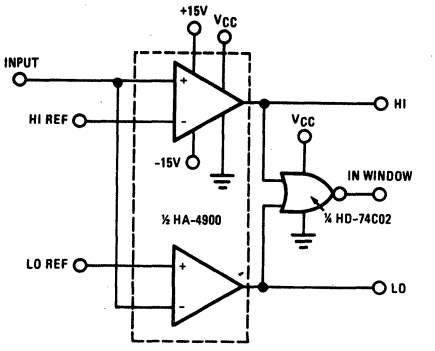
RS-232 TO CMOS LINE RECEIVER

This RS-232 type line receiver to drive CMOS logic uses a Schmitt trigger feedback network to give about 1 volt input hysteresis for added noise immunity. A possible problem in an interface which connects two equipments, each plugged into a different AC receptacle, is that the power line voltage may appear at the receiver input when the interface connection is made or broken. The two diodes and a 3 watt input resistor will protect the inputs under these conditions.



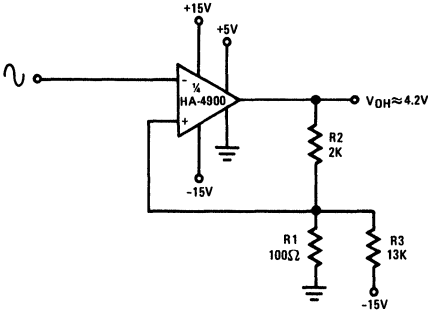
OSCILLATOR/CLOCK GENERATOR

This self-starting fixed frequency oscillator circuit gives excellent frequency stability. R_1 and C_1 comprise the frequency determining network while R_2 provides the regenerative feedback. Diode D_1 enhances the stability by compensating for the difference between V_{OH} and V_{Supply}. In applications where a precision clock generator up to 100kHz is required, such as in automatic test equipment, C_1 may be replaced by a crystal.



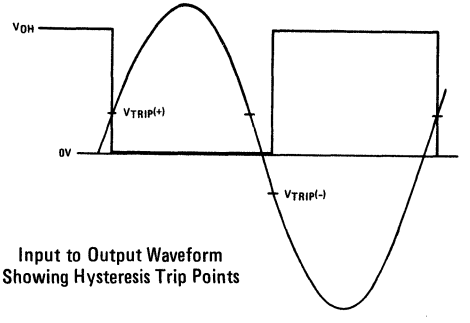
WINDOW DETECTOR

The high switching speed, low offset current and low offset voltage of the HA-4900/4905 makes this window detector circuit extremely well suited to applications requiring fast, accurate, decision-making. The circuit above is ideal for industrial process system feedback controllers or "out-of-limit" alarm indicators.



SCHMITT TRIGGER (ZERO CROSSING DETECTOR WITH HYSTERESIS)

This circuit has a 100mV hysteresis which can be used in applications where very fast transition times are required at the output even though the signal input is very slow. The hysteresis loop also reduces false triggering due to noise on the input. The waveforms below show the trip points developed by the hysteresis loop.



Input to Output Waveform
Showing Hysteresis Trip Points

CMOS Analog Switches and Multiplexers

CMOS Switches Selection Guide

FUNCTION	DEVICE	$R_{ON}(\Omega)$ (TYP)	$I_{D(OFF)}$(NA) (TYP)	$t_{(ON)}$(NS) (TYP)	$t_{(OFF)}$(NS) (TYP)	P_D(mW) (TYP)	PAGE
5PST	HI-5040	50	0.5	370	280	1.5	20
2 x SPST	HI-200	55	1	240	180	15	4
	HI-5048	25	0.5	370	280	1.5	20
	HI-5041	50	0.5	370	280	1.5	20
4 x SPST	HI-201	65	2	180	155	15	10
SPDT	HI-5050	25	0.5	370	280	1.5	20
	HI-5042	50	0.5	370	280	1.5	20
2 x SPDT	HI-5051	25	0.5	370	280	1.5	20
	HI-5043	50	0.5	370	280	1.5	20
DPST	HI-5044	50	0.5	370	280	1.5	20
2 x DPST	HI-5049	25	0.5	370	280	1.5	20
	HI-5045	50	0.5	370	280	1.5	20
2 x DPST (3 ADDRESS)	HI-1800A	125	0.02	500	300	10	16
DPDT	HI-5046A	25	0.5	370	280	1.5	20
	HI-5046	50	0.5	370	280	1.5	20
4PST	HI-5047A	25	0.5	370	280	1.5	20
	HI-5047	50	0.5	370	280	1.5	20

NOTE: All data typical room temperature specifications at $\pm$ 15V supplies. For guaranteed and tested specifications consult the device data sheet.

CMOS Multiplexers Selection Guide

FUNCTION	DEVICE	FEATURE	TTL "HIGH" MIN(V)	$R_{ON}(\Omega)$ (TYP)	$I_{D(OFF)}$ (NA) (TYP)	$t_{(ON)}$ (NS) (TYP)	$t_{(OFF)}$ (NS) (TYP)	P_D(mW) (TYP)	PAGE
4-CHANNEL DIFFERENTIAL	HI-1828A	LOW R_{ON} LOW LEAKAGE	4.0	250	0.05	350	250	5	46
	HI-509A	ANALOG INPUT OVERVOLTAGE PROTECTION	4.0	1200	1.0	500	420	7.5	40
8-CHANNEL	HI-1818A	LOW R_{ON} LOW LEAKAGE	4.0	250	0.1	350	250	5	46
	HI-508A	ANALOG OVERVOLTAGE PROTECTION	4.0	1200	1.0	500	420	7.5	40
8-CHANNEL DIFFERENTIAL	HI-507	LOW R_{ON}	2.4	170	1.0	300	220	30	28
	HI-507A	ANALOG OVERVOLTAGE PROTECTION	4.0	1200	1.0	500	420	7.5	34
16-CHANNEL	HI-506	LOW R_{ON}	2.4	170	1.0	300	220	30	28
	HI-506A	ANALOG OVERVOLTAGE PROTECTION	4.0	1200	1.0	500	420	7.5	34
	HI-1840	HIGH-Z OVERVOLTAGE PROTECTION	4.0	2000	1.0	500	420	0.6	50

NOTE: All data typical room temperature specifications at $\pm$15V supplies. For guaranteed and tested specifications consult the device data sheet.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-200

Dual SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 240ns
- LOW R_{ON} 55Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE
- NO DIGITAL INPUT CURRENT SPIKE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

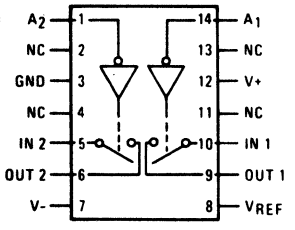
HI-200 is a monolithic device comprising two independently selectable SPST switches which feature fast switching speeds (290ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and Complementary CMOS processing, HI-200 operates without any applications problems induced by latch-up or SCR mode phenomena.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters and op amp gain switching networks.

HI-200 is available in D.I.P. (TO-116) and metal (TO-100) cans. HI-200-2 is specified from -55°C to +125°C while HI-200-5 operates from 0°C to +75°C. HI-200 is functionally and pin compatible with other available "200 series" switches.

PINOUT

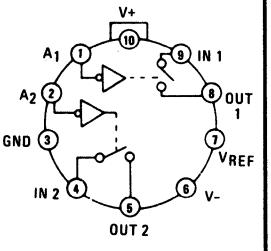
Package Code 4B



TO-116

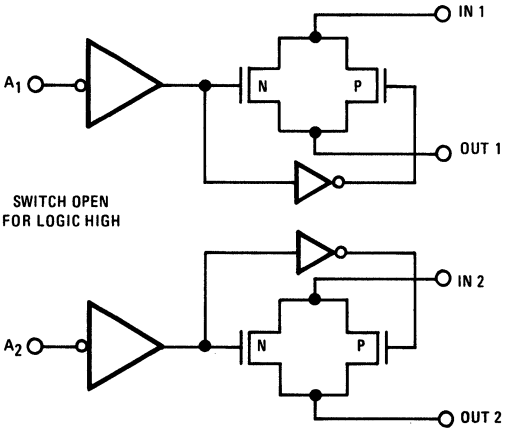
Package Code 2D

Top View



TO-100

FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 6 and 10	+40V	Total Power Dissipation*	450mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	$+V_{Supply}$ +4V	HI-200-2	-55°C to +125°C
	$-V_{Supply}$ -4V	HI-200-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-200-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 6mW/°C Above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH}(Logic Level High) = 3.0V V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

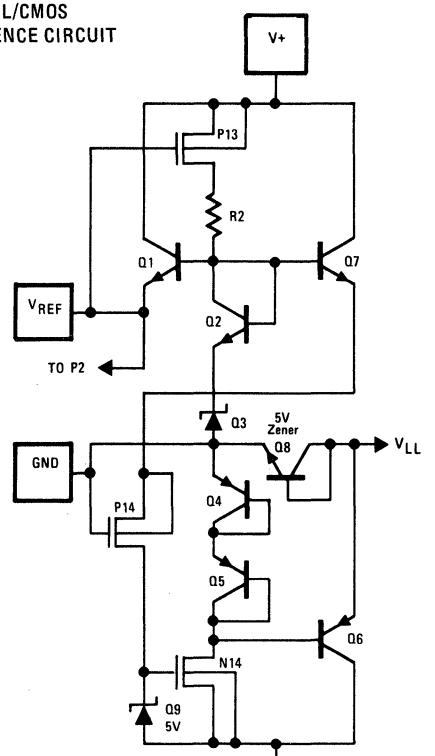
		HI-200-2** -55°C to +125°C			HI-200-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
* V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		72	100	Ω
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		1			1		nA
	Full		100	500		10	500	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		1			1		nA
	Full		100	500		10	500	nA
* $I_{D(ON)}$, On Leakage Current	+25°C		.02			.02		nA
	Full		6	500		6	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
* I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		60			60		ns
t_{on}, Switch on Time	+25°C		240	500		240		ns
t_{off}, Switch off Time	+25°C		330	500		500		ns
"Off Isolation" (Note 4)	+25°C		70			70		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
* I^+, Current (Pin 10)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
* I^-, Current (Pin 6)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = +3V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f, 100 kHz
5. V_A = +3V or V_A = OV For Both Switches

*100% Tested For Dash 8 At +25°C And +125°C Only

**Note: HI-200-4 has same specifications as HI-200-2 over the reduced temperature range -20°C to +85°C

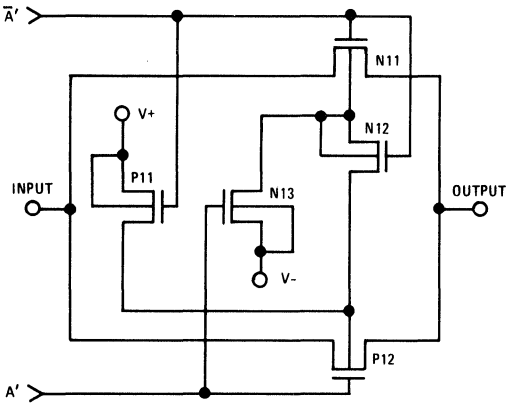
TTL/CMOS
REFERENCE CIRCUIT



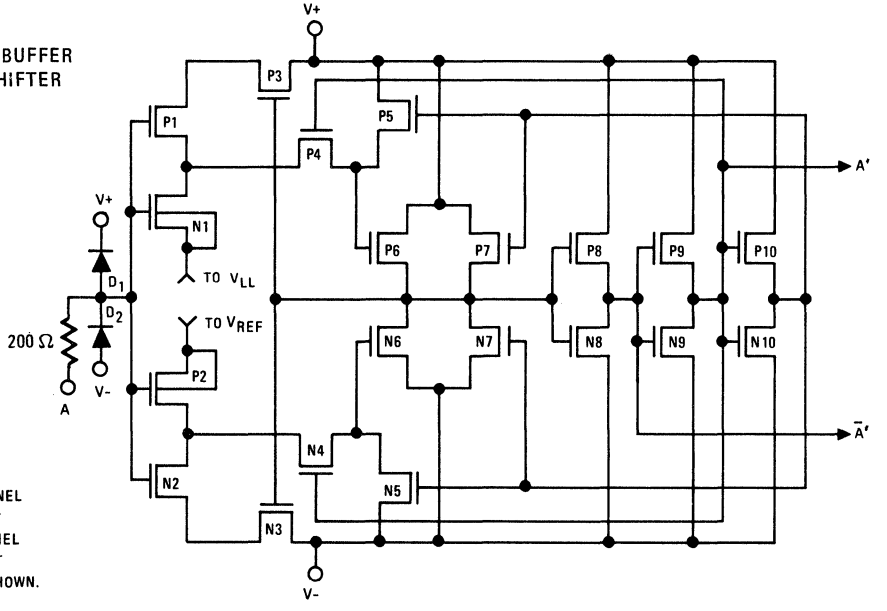
*TTL Interface: Leave V_{REF} Open

*CMOS Interface: If $V_{DD} > +5.5V$, Connect V_{DD} to V_{REF} for Higher Noise Immunity; Otherwise Leave Open.

SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER



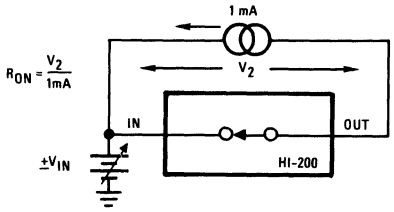
ALL N-CHANNEL
BODIES TO V-

ALL P-CHANNEL
BODIES TO V+

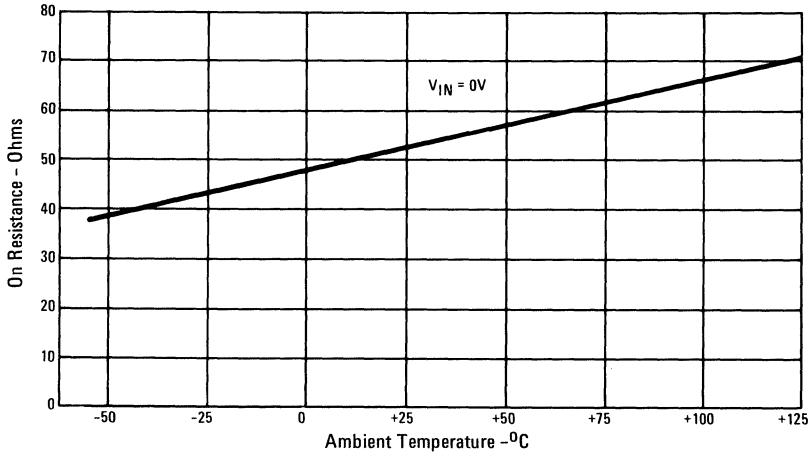
EXCEPT AS SHOWN.

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 3.0V$ $V_{AL} = 0.8V$ AND V_{REF} = OPEN).

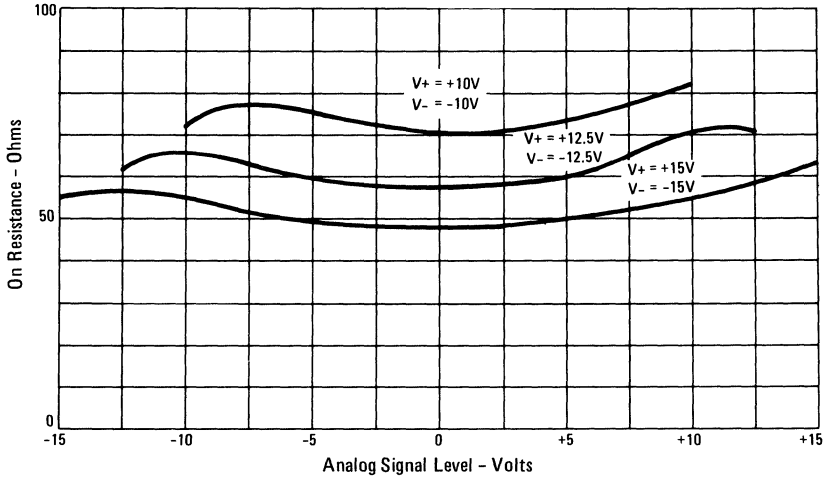
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



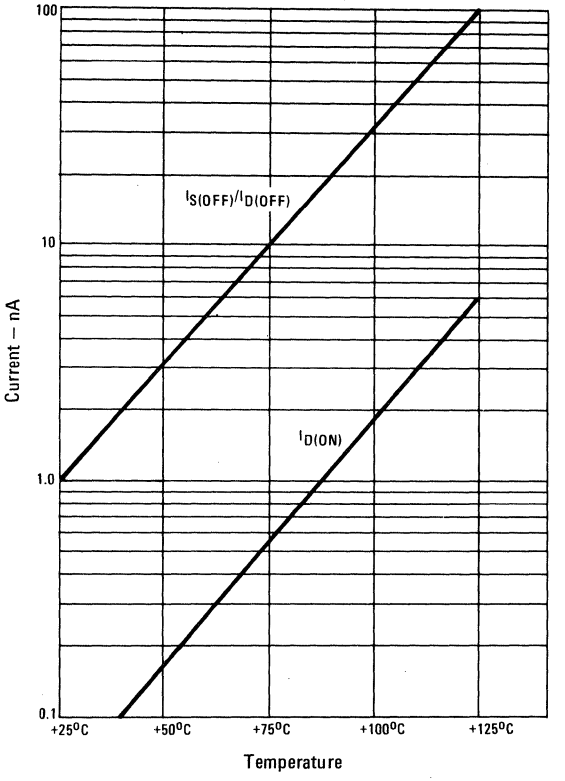
ON RESISTANCE vs. TEMPERATURE



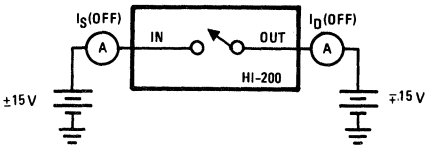
(HI-200)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE



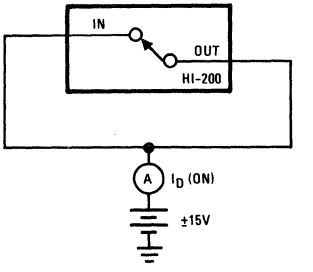
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-200)



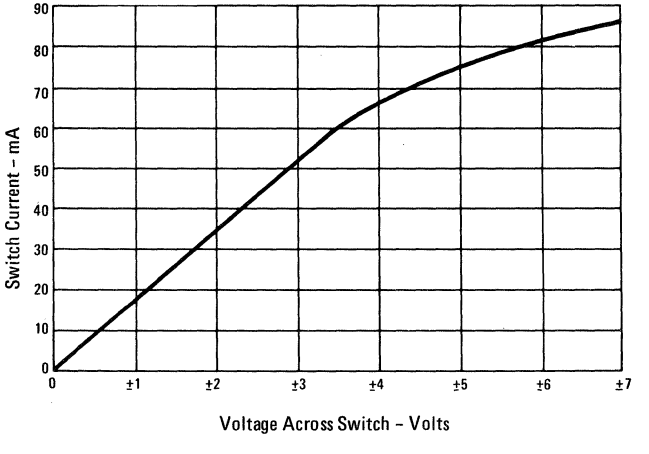
OFF LEAKAGE CURRENT vs. TEMPERATURE



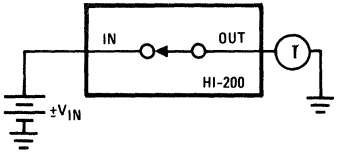
ON LEAKAGE CURRENT vs. TEMPERATURE



SWITCH CURRENT vs. VOLTAGE

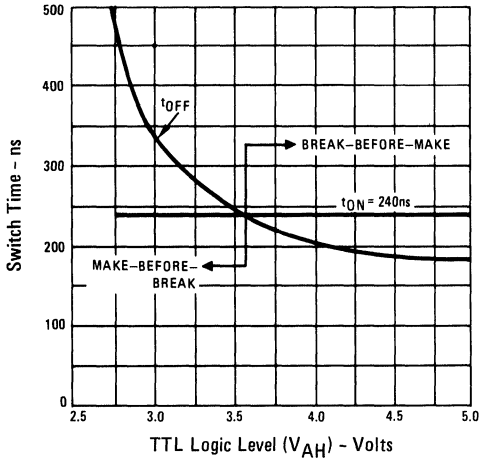


SWITCH CURRENT vs. VOLTAGE

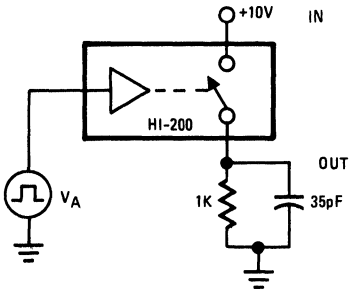


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

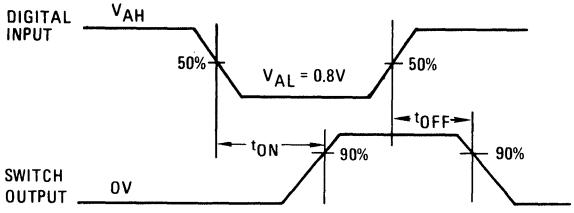
(HI-200)
SWITCH TIME vs. TTL LOGIC LEVEL



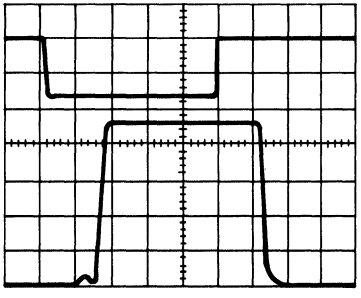
ON/OFF SWITCH TIME vs.
LOGIC LEVEL



SWITCHING WAVEFORMS

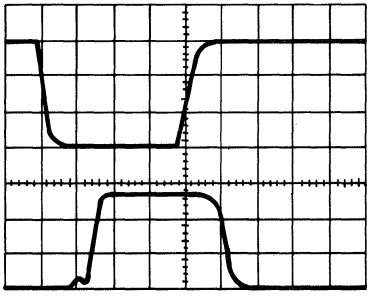


t_{ON}, t_{OFF} (TTL INPUT)
V_{AH} = +4.0V



Top: TTL Input Vertical: 2V/Div.
Bottom: Output Horizontal: 200ns/Div.

t_{ON}, t_{OFF} (CMOS INPUT)
V_{REF} = OPEN, V_{AH} = +15V



Top: CMOS Input Vertical: 5V/Div.
Bottom: Output Horizontal: 200ns/Div.

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HI-201

Quad SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 185ns
- LOW R_{ON} 65Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE
- NO DIGITAL INPUT CURRENT SPIKE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

HI-201 is a monolithic device comprising four independently selectable SPST switches which feature fast switching speeds (185ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and Complementary CMOS processing, HI-201 operates without any applications problems induced by latch-up or SCR-mode phenomena.

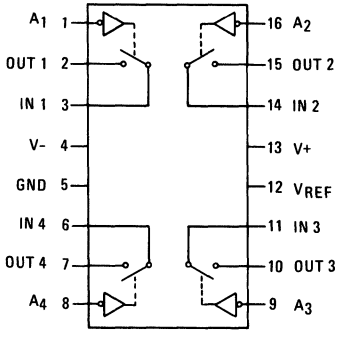
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-201 is an ideal component for use in high frequency analog switching. Typical appliations include signal path switching, sample and hold circuit, digital filters and op amp gain switching networks.

HI-201 is available in a 16 lead dual-in-line package. HI-201-2 is specified from -55°C to +125°C while HI-201-5 operates from 0°C to +75°C. HI-201 is functionally and pin compatible with other available "200 series" switches.

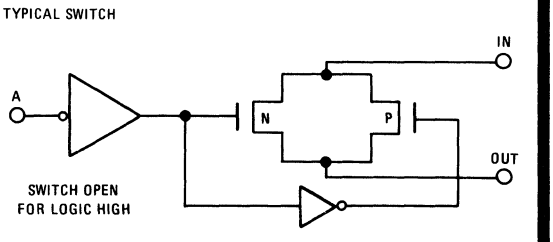
PIN OUT

Package Code 4B

Top View



FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 4 and 13	+40V	Total Power Dissipation*	750mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	$V_{Supply}(+)$ +4V	HI-201-2	-55°C to +125°C
	$V_{Supply}(-)$ -4V	HI-201-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-201-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 3.0V V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

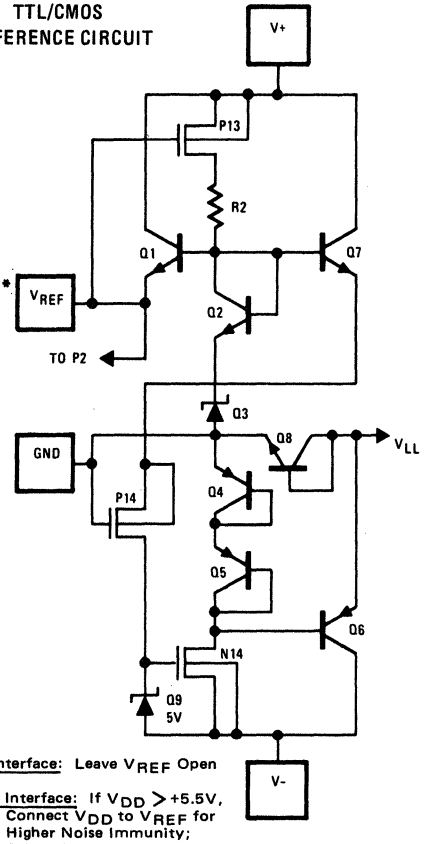
		HI-201-2** -55°C to +125°C			HI-201-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		65	80		65	100	Ω
	Full		85	125		75	125	Ω
*$I_{S(OFF)}$, Off Input Leakage Current	+25°C		2			2		nA
	Full			500			250	nA
*$I_{D(OFF)}$, Off Output Leakage Current	+25°C		2			2		nA
	Full			500			250	nA
*$I_{D(ON)}$, On Leakage Current	+25°C		2			2		nA
	Full			500			250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
*I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		30			30		ns
t_{on}, Switch ON Time	+25°C		185	500		185		ns
t_{off}, Switch OFF Time	+25°C		220	500		220		ns
"Off Isolation" (Note 4)	+25°C		80			80		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
*I+, Current (Pin 13)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
*I- Current (Pin 4)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = 5V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f = 100KHz
5. V_A = +3V or V_A = 0V For all Switches

* 100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)
** Note: HI-201-4 has same specifications as HI-201-2 over the reduced temperature range -20°C to +85°C

SCHEMATIC DIAGRAMS

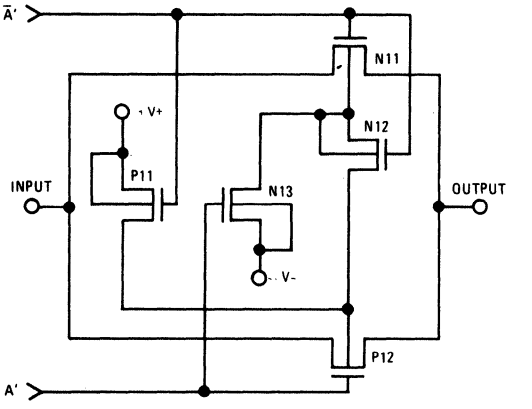
TTL/CMOS REFERENCE CIRCUIT



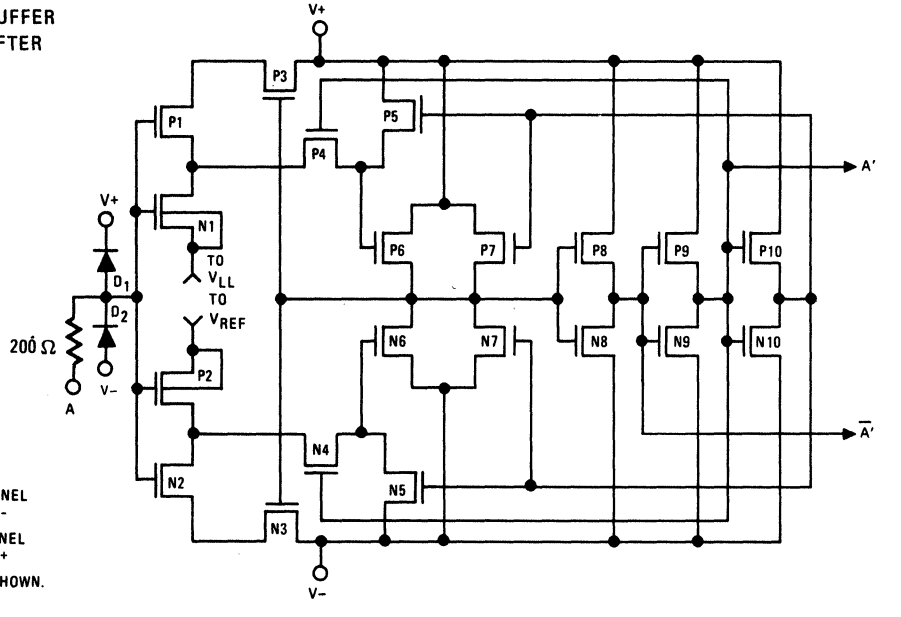
*TTL Interface: Leave V_{REF} Open

*CMOS Interface: If $V_{DD} > +5.5V$, Connect V_{DD} to V_{REF} for Higher Noise Immunity; Otherwise Leave Open.

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



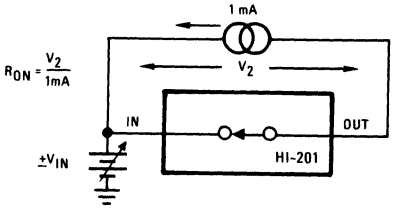
ALL N-CHANNEL BODIES TO V-

ALL P-CHANNEL BODIES TO V+

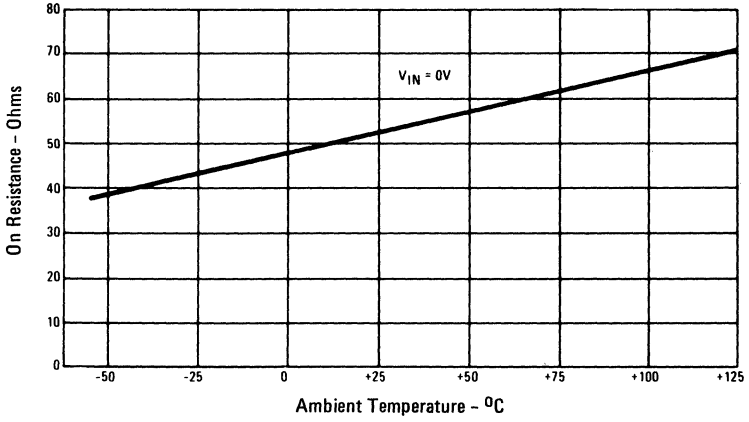
EXCEPT AS SHOWN.

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 3.0V$ $V_{AL} = 0.8V$ AND V_{REF} = OPEN).

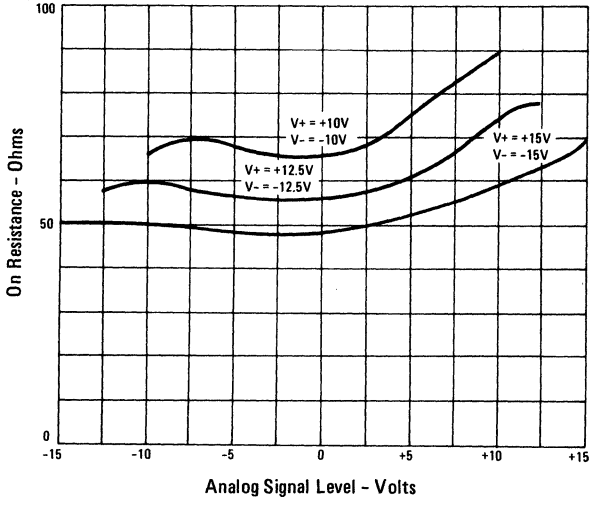
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



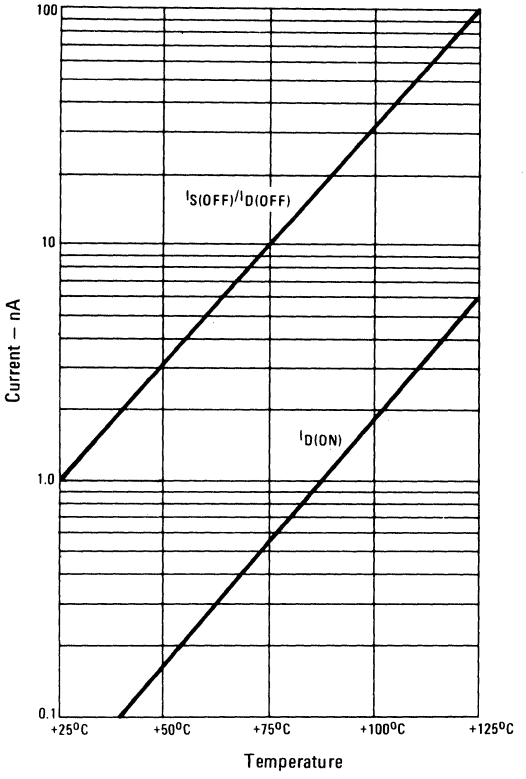
ON RESISTANCE vs. TEMPERATURE



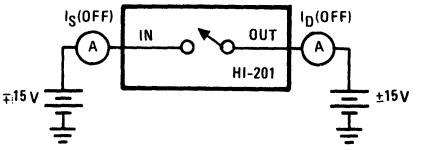
(HI-201)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE



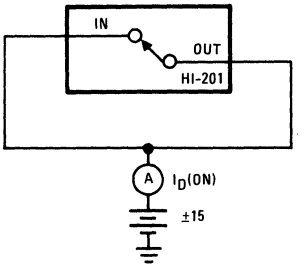
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-201)



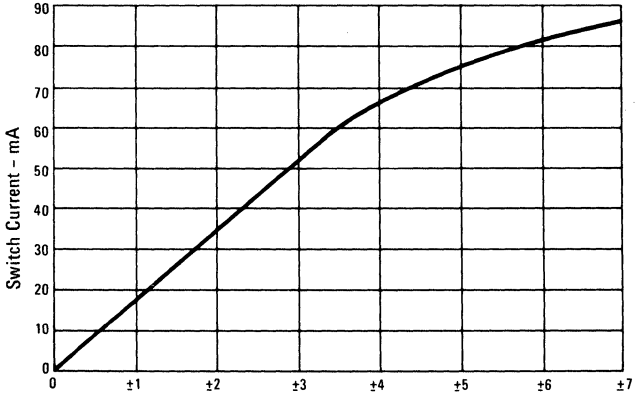
OFF LEAKAGE CURRENT vs. TEMPERATURE



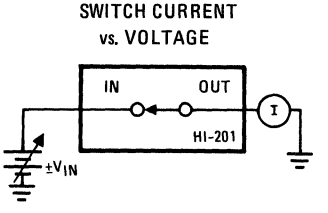
ON LEAKAGE CURRENT vs. TEMPERATURE



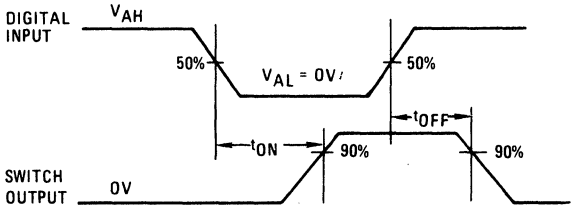
SWITCH CURRENT vs. VOLTAGE



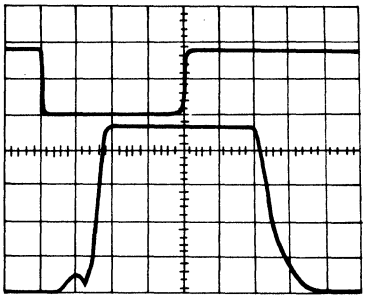
SWITCH CURRENT vs. VOLTAGE



SWITCHING WAVEFORMS



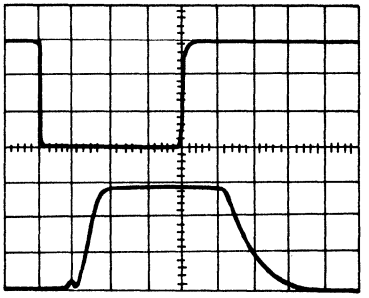
t_{ON}, t_{OFF}(TTL INPUT)
V_{IN} = 3.5V



Top: TTL Input
Bottom: Output

Horizontal: 100ns/Div.
Vertical: 2V/Div.

t_{ON}, t_{OFF}(CMOS INPUT)
V_{REF} = OPEN, V_{IN} = +15V



Top: CMOS Input
Bottom: Output

Vertical: 5V/Div.
Horizontal: 100ns/Div.

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HI-1800A

Low Leakage Dual DPDT Analog Switch

FEATURES

- LEAKAGE AT +125°C (TYP.) 40nA
- SIGNAL RANGE ±15V
- "ON" RESISTANCE (TYP.) 125Ω
- ACCESS TIME (TYP.) 500ns
- DTL/TTL COMPATIBLE ADDRESS
- -55°C TO +125°C OPERATION

APPLICATIONS

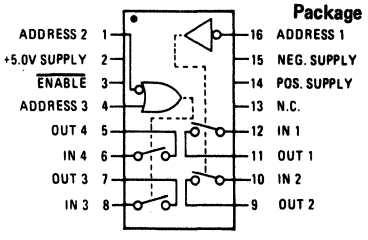
- SIGNAL SELECTOR
- CHOPPER
- SAMPLE AND HOLD
- GAIN SWITCHING

DESCRIPTION

The HI-1800A is a general purpose analog switch which may be used as a signal selector, multiplexer, chopper, or cross-point switch for signals from D.C. to R.F. The configuration is two independent DPST switches with versatile TTL compatibile addressing logic which allows connection as two SPDT, or as a single DPDT, SPDT, or SPST switch by connection of external jumpers. ON resistance decreases correspondingly when switching elements are connected in parallel. The HI-1800A is fabricated on a single dielectrically isolated chip using complementary N and P channel MOS devices. This unique process produces exceptionally low leakage currents (even at +125°C), constant ON resistance, low power dissipation, and fast switching. The HI-1800A is available in a hermetic 16 pin dual-in-line package.

PINOUT

Package Code 4B

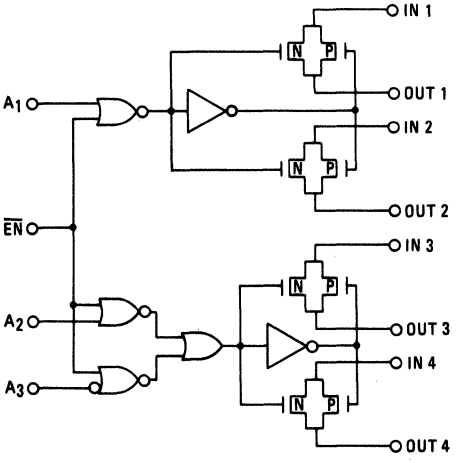


TRUTH TABLE

INPUT ADDRESS				SWITCH CHANNELS			
A1	A2	A3	$\overline{EN}$	1	2	3	4
L	X	X	L	ON	ON		
H	X	X	L	OFF	OFF		
X	L	X	L			ON	ON
X	X	H	L			ON	ON
X	H	L	L			OFF	OFF
X	X	X	H	OFF	OFF	OFF	OFF

H ≥ +4.0V L ≤ +0.4V

FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	V^-Supply, V^+Supply
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation	780 mW (Note 2)
Analog Input Voltage: V^+Supply +2V	V^-Supply -2V	Storage Temperature Range	−65°C to +150°C

ELECTRICAL CHARACTERISTICS

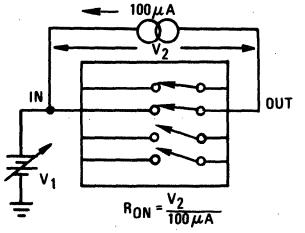
Supplies = +15V, -15V, +5.0V

PARAMETER	TEMP.	HI-1800A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-1800A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
* V_{IN}, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, ON Resistance (Note 3)	+25°C		125	200		125	200	Ω
	Full			250			250	Ω
* I_S (OFF), Input Leakage Current	Full		40	100		40	100	nA
* I_D (OFF), Output Leakage Current	Full		40	100		40	100	nA
* I_D (ON), On Channel Leakage Current	Full		40	100		40	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{IL}, Input Low Threshold	Full			0.4			0.4	V
V_{IH}, Input High Threshold (Note 4)	Full	4.0			4.0			V
* I_{IN}, Input Leakage Current	Full		.01	1		.01	1	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time (Note 5)	+25°C		500			500		ns
Break-Before-Make Delay	+25°C		200			200		ns
C_{IN}, Channel Input Capacitance	+25°C		8			8		pF
C_{OUT}, Channel Output Capacitance	+25°C		8			8		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		10			10		mW
P_{DS}, Standby Power (Note 6)	Full		10			10		mW
* I_+, Current Pin 14	Full		0.001	0.5		0.001	1	mA
* I_-, Current Pin 15	Full		0.5	1		0.5	2	mA
* I_L, Current Pin 2	Full		0.5	1		0.5	2	mA

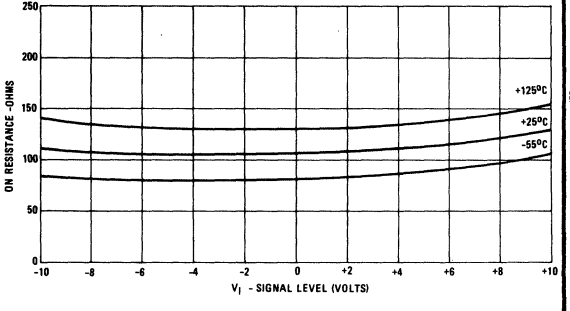
NOTES:
1. Voltage ratings apply when voltages at all other pins are within their nominal operating ranges.
2. Derate 9.25 mW/°C above t_A = +75°C
3. V_{OUT} = ±10V I_{OUT} = -100μA.
4. To drive from DTL/TTL circuits, 1K pullup resistors to +5.0V supply are recommended.
5. Time measured to 90% of final output level; V_{OUT} = -5.0V to +5.0V, Digital Inputs = 0.4V to +4.0V.
6. Voltage at Pin 3, $\overline{\text{ENABLE}} \geq$ +4.0V.

*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)

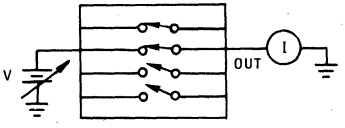
ON RESISTANCE vs ANALOG SIGNAL LEVEL



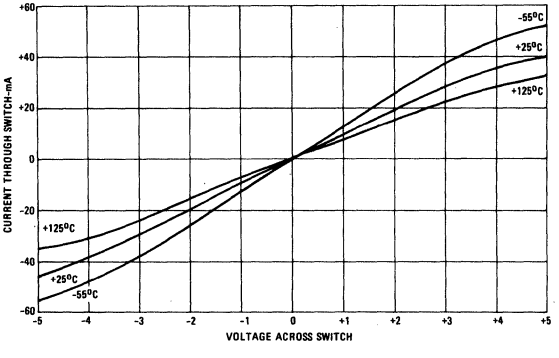
Test Circuit



ON CHANNEL CURRENT vs VOLTAGE

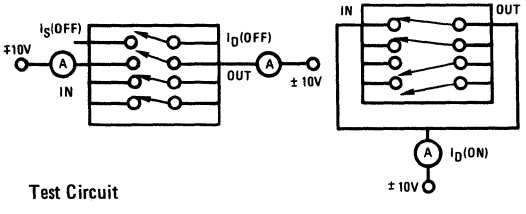


Test Circuit

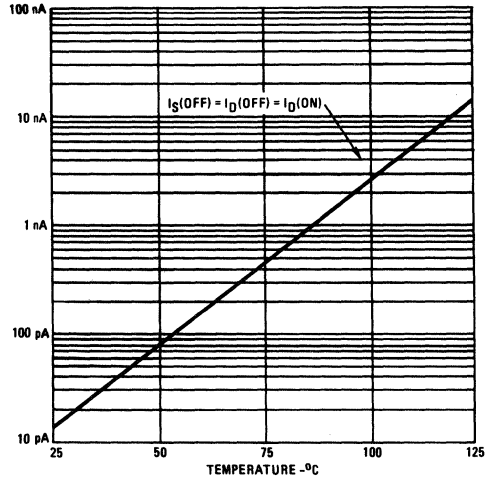


ON/OFF LEAKAGE CURRENTS vs TEMPERATURE

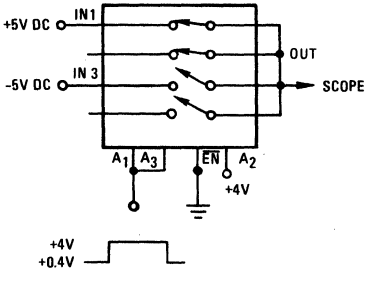
OFF LEAKAGE ON LEAKAGE

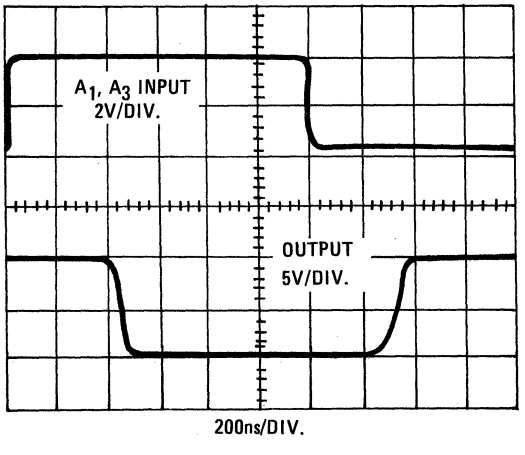


Test Circuit



ACCESS TIME

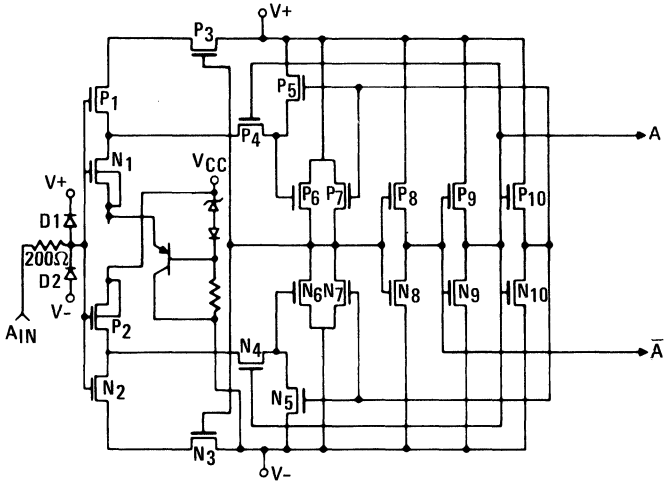




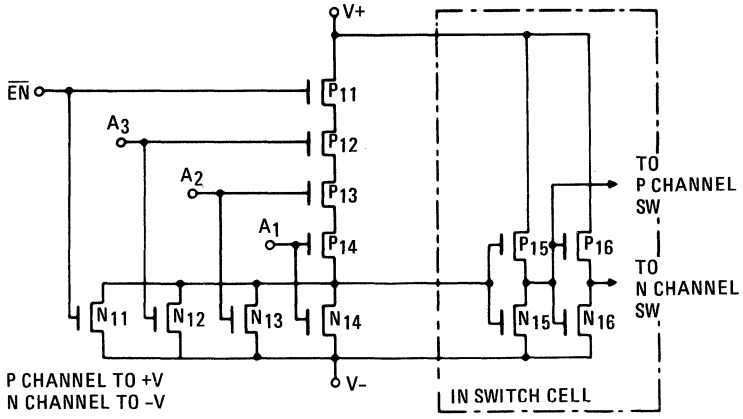
SCHEMATIC DIAGRAM

ADDRESS INPUT BUFFER

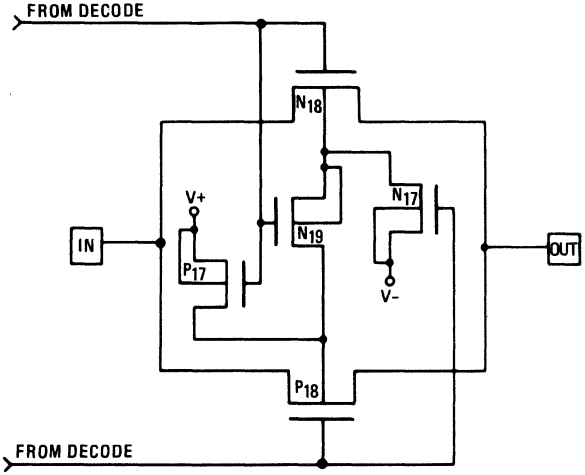
ALL N-CHANNEL BODIES TO V-
ALL P-CHANNEL BODIES TO V+
UNLESS OTHERWISE INDICATED



DECODER GATE



MULTIPLEX SWITCH



3

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-5040 thru HI-5051
HI-5046A and HI-5047A

CMOS Analog Switches

FEATURES

- WIDE ANALOG SIGNAL RANGE ±15V
- LOW "ON" RESISTANCE (TYP) 25Ω
- HIGH CURRENT CAPABILITY (TYP) 80mA
- BREAK-BEFORE-MAKE SWITCHING
  - TURN-ON TIME (TYP) 370ns
  - TURN-OFF TIME (TYP) 280ns
- NO LATCH-UP
- INPUT MOS GATES ARE PROTECTED FROM ELECTROSTATIS DISCHARGE
- DTL, TTL, CMOS, PMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY SWITCHING
- SAMPLE AND HOLD
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING

DESCRIPTION

This family of CMOS analog switches offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25 ohms for HI-5048 through HI-5051 and HI-5046A/5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at 25°C). This family of switches also features very low power operation (1.5mW at 25°C).

There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional diagram). All devices are available in 16 pin D.I.P. packages. The HI-5040/5050 switches can directly replace IH-5040 series devices and are functionally compatible with the DG 180/190 family. Each switch type is available in the -55°C to +125°C and 0°C to +75°C performance grades.

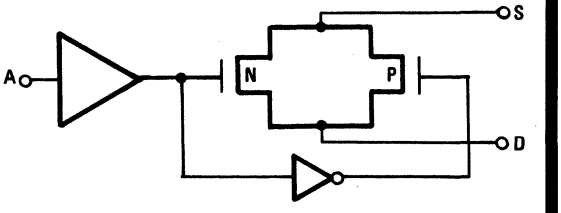
FUNCTIONAL DESCRIPTION

Package Code 4B

PART NUMBER	TYPE	RON
HI-5040	SPST	75Ω
HI-5041	DUAL SPST	75Ω
HI-5042	SPDT	75Ω
HI-5043	DUAL SPDT	75Ω
HI-5044	DPST	75Ω
HI-5045	DUAL DPST	75Ω
HI-5046	DPDT	75Ω
HI-5046A	DPDT	30Ω
HI-5047	4PST	75Ω
HI-5047A	4PST	30Ω
HI-5048	DUAL SPST	30Ω
HI-5049	DUAL DPST	30Ω
HI-5050	SPDT	30Ω
HI-5051	DUAL SPDT	30Ω

FUNCTIONAL DIAGRAM

TYPICAL SWITCH



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$)	36V	Analog Current (S to D)	80mA
V_R to Ground	V^+, V^-	Total Power Dissipation*	450mW
Digital and Analog	$V^+ + 4V$	Operating Temperature	
Input Voltage	$V^- - 4V$	HI-50XX-2	-55°C to +125°C
		HI-50XX-5	0°C to +75°C
		Storage Temperature	-65°C to +150°C

*Derate 6mW/°C above T_A = 75°C

ELECTRICAL CHARACTERISTICS

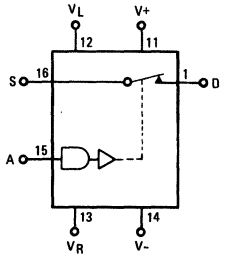
Unless Otherwise Specified
Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 3.0V; V_{AL} (Logic Level Low) = +0.8V, V_L = +5V
For Test Conditions, consult Performance Characteristics

PARAMETER	TEMP	-55°C to +125°C MIN	-55°C to +125°C TYP	-55°C to +125°C MAX	0°C to +75°C MIN	0°C to +75°C TYP	0°C to +75°C MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
* Analog Signal Range	Full	-15		+15	-15		+15	V
* Ron, "ON" Resistance (Note 1a)	+25°C		50			50		Ω
	Full			75			75	Ω
* Ron, "ON" Resistance (Note 1b)	+25°C		25			25		Ω
	Full			50			50	Ω
Ron, Channel-to-Channel Match (Note 1a)	+25°C		2	10		2	10	Ω
Ron, Channel-to-Channel Match (Note 1b)	+25°C		1	5		1	5	Ω
* $I_{S(OFF)}$ = $I_{D(OFF)}$, Off Input or Output Leakage Current	+25°C		0.8			0.8		nA
	Full		100	500		100	500	nA
* $I_{D(ON)}$, On Leakage Current	+25°C		0.01			0.01		nA
	Full		2	500		2	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
* I_A, Input Leakage Current (High or Low)	Full		.01	1.0		.01	1.0	μA
SWITCHING CHARACTERISTICS								
t_{on}, Switch "ON" Time	+25°C		370	1000		370		ns
t_{off}, Switch "OFF" Time	+25°C		280	500		280		ns
Charge Injection (Note 2)	+25°C		5	20		5		mV
"OFF Isolation" (Note 3)	+25°C	75	80			80		dB
"Crosstalk" (Note 3)	+25°C	80	88			88		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		11			11		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		11			11		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS								
P_D, Quiescent Power Dissipation	+25°C		1.5			1.5		mW
* I^+, +15V Quiescent Current	Full			0.3			0.5	mA
* I^-, -15V Quiescent Current	Full			0.3			0.5	mA
* I_L, +5V Quiescent Current	Full			0.3			0.5	mA
* I_R, Gnd Quiescent Current	Full			0.3			0.5	mA

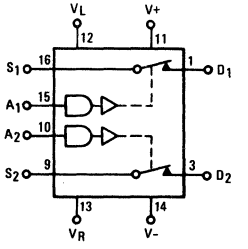
NOTES: 1. V_{OUT} = ±10V, I_{OUT} = 1mA
a) For HI-5040 thru HI-5047
b) For HI-5048 thru HI-5051, HI-5046A/5047A
2. V_{IN} = 0V, C_L = 10,000pF
3. R_L = 100Ω, f= 100 KHz, V_{IN} = 2 V_{PP}, C_L = 5pF

*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)

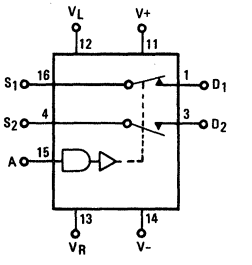
SPST
HI-5040 (75Ω)



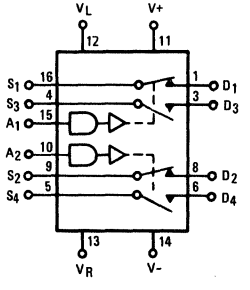
DUAL SPST
HI-5041 (75Ω)



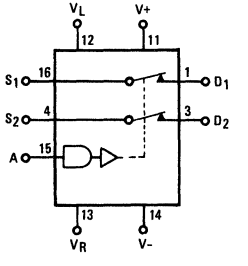
SPST
HI-5042 (75Ω)



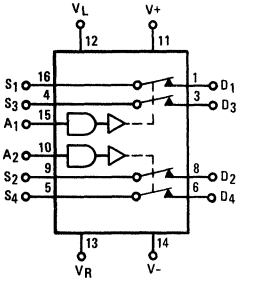
DUAL SPST
HI-5043 (75Ω)



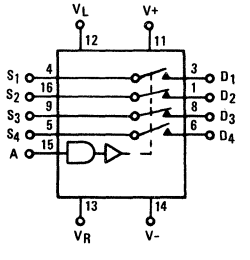
DPST
HI-5044 (75Ω)



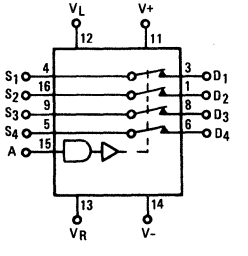
DUAL DPST
HI-5045 (75Ω)



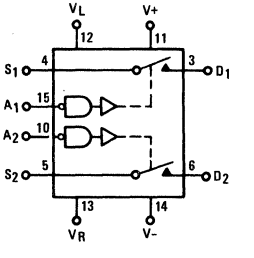
DPDT
HI-5046 (75Ω)
HI-5046A (30Ω)



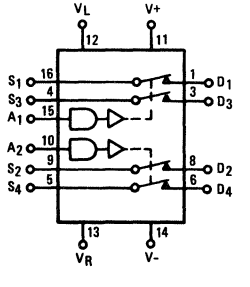
4PST
HI-5047 (75Ω)
HI-5047A (30Ω)



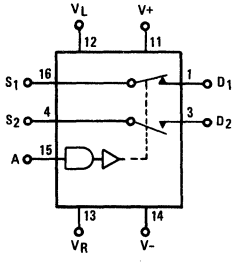
DUAL SPST
HI-5048 (30Ω)



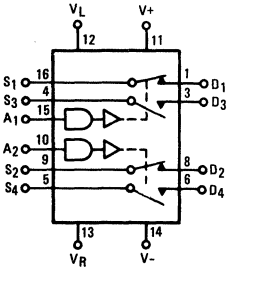
DUAL DPST
HI-5049 (30Ω)



SPST
HI-5050 (30Ω)

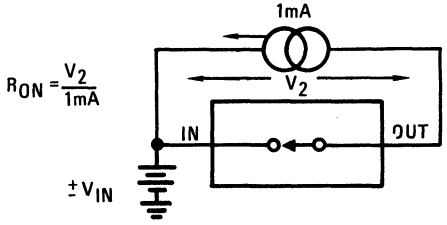


DUAL SPST
HI-5051 (30Ω)

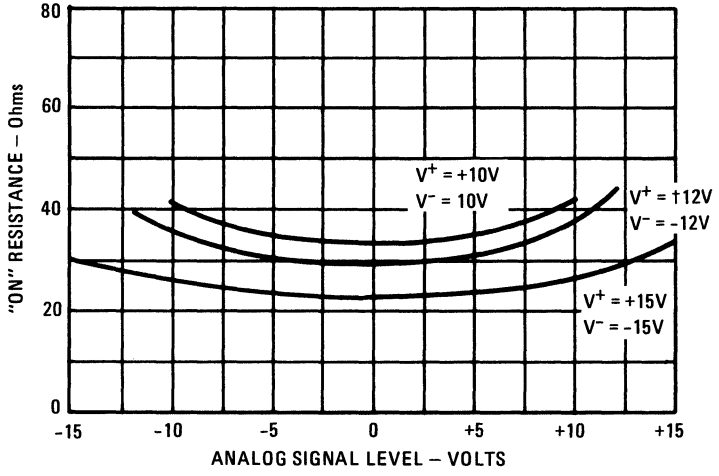


(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$, $V_R = 0V$, $V_{AH} = 3.0V$ and $V_{AL} = 0.8V$

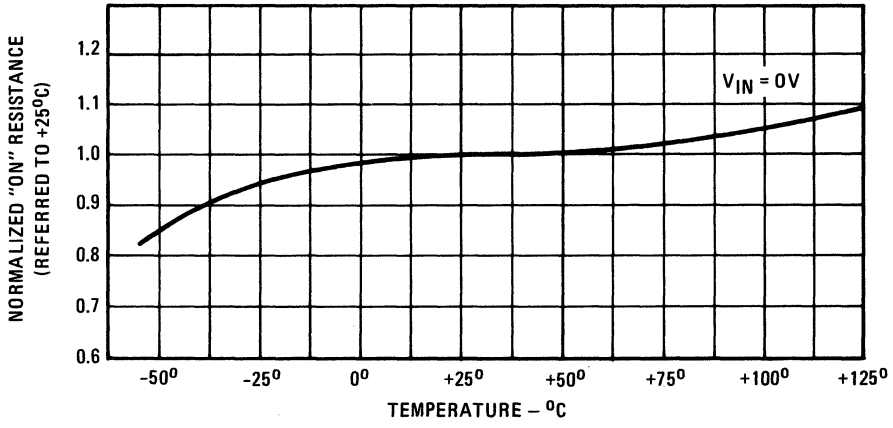
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



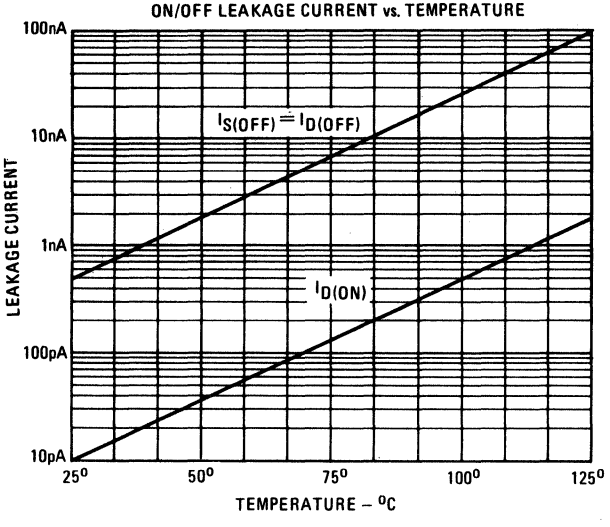
"ON"" RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE



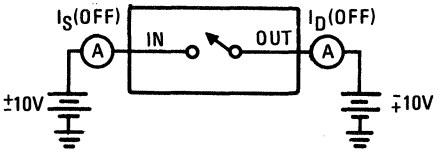
NORMALIZED "ON" RESISTANCE vs. TEMPERATURE



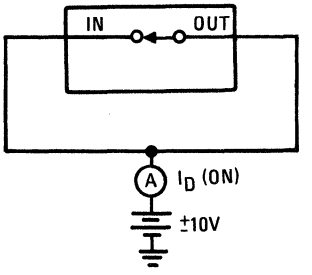
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



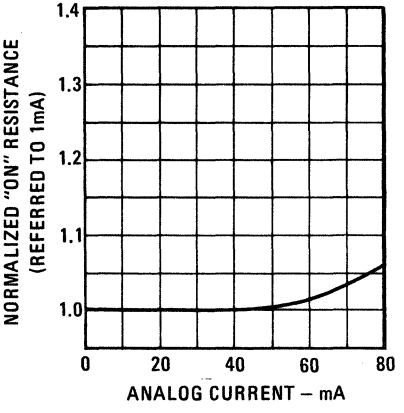
OFF LEAKAGE CURRENT vs. TEMPERATURE



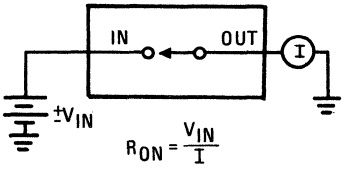
ON LEAKAGE CURRENT vs. TEMPERATURE



NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT

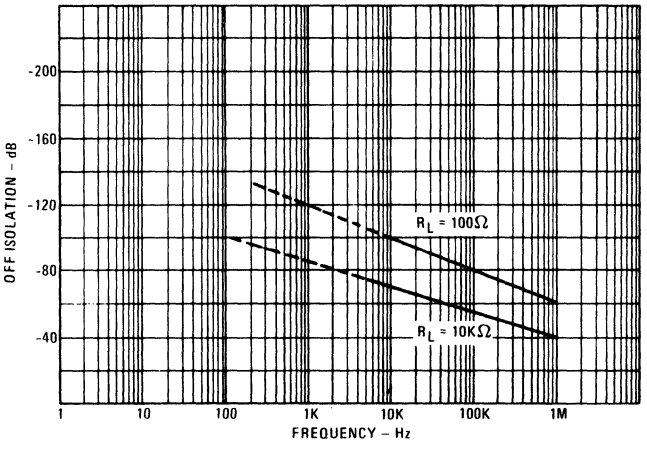


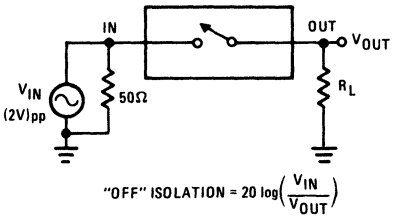
"ON" RESISTANCE vs. ANALOG CURRENT



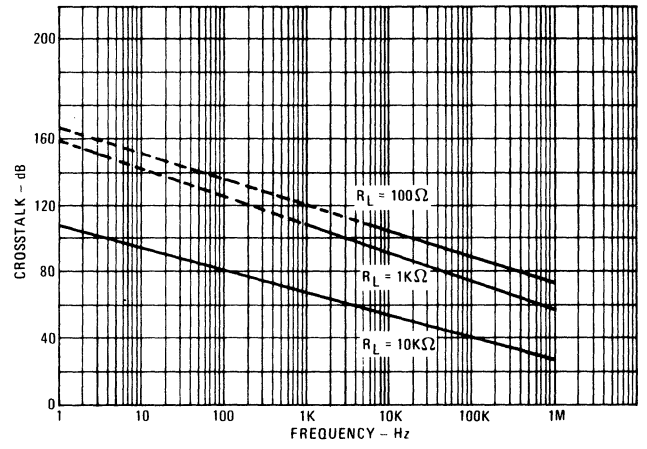
3

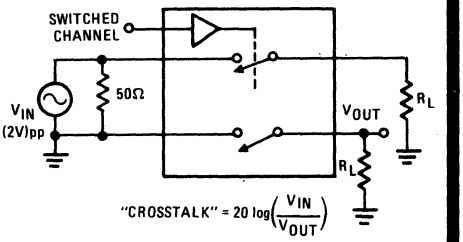
"OFF" ISOLATION vs. FREQUENCY



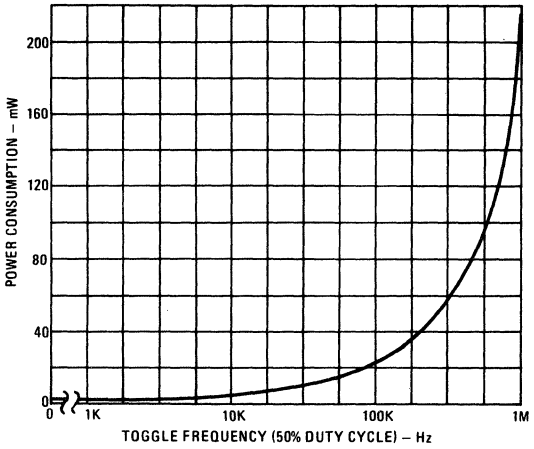


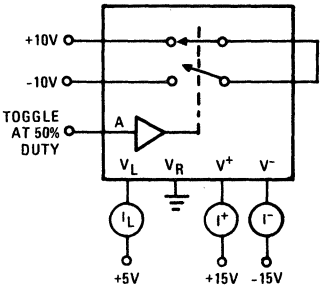
CROSSTALK vs. FREQUENCY





POWER CONSUMPTION vs. FREQUENCY

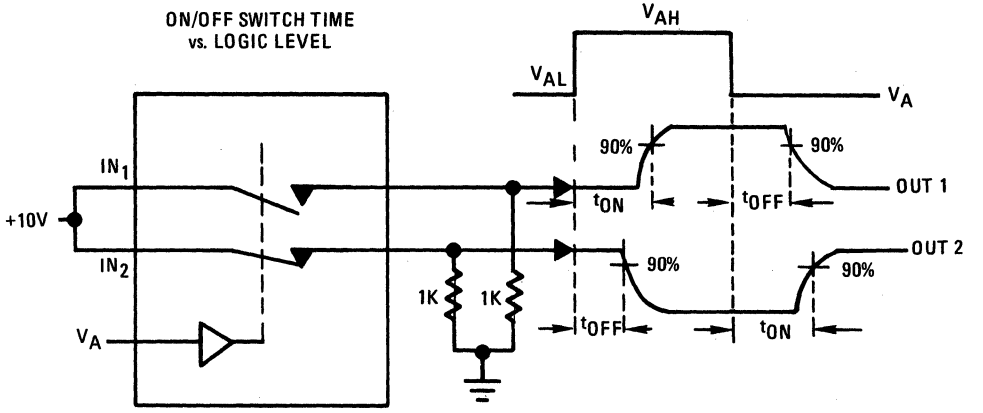




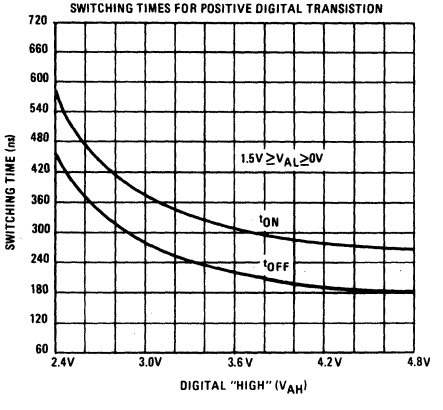
3

SWITCHING CHARACTERISTICS

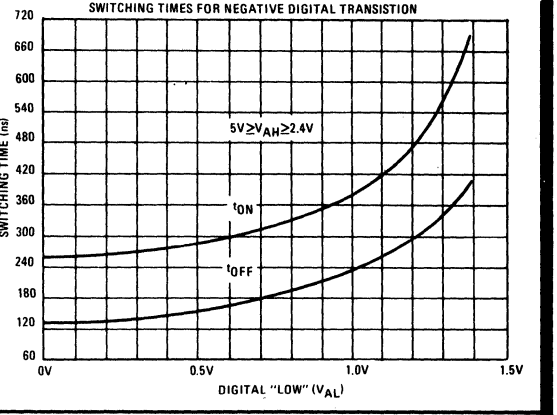
ON/OFF SWITCH TIME
vs. LOGIC LEVEL



SWITCHING TIMES FOR POSITIVE DIGITAL TRANSISTION

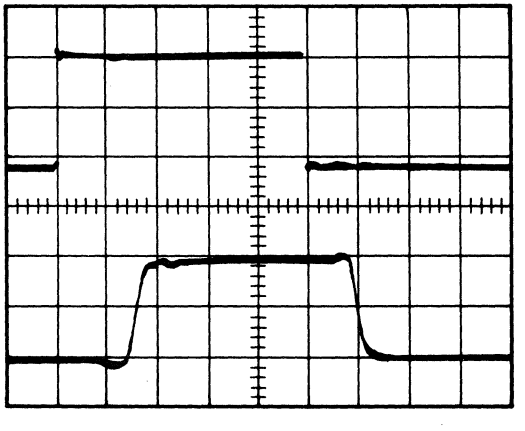


SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSISTION



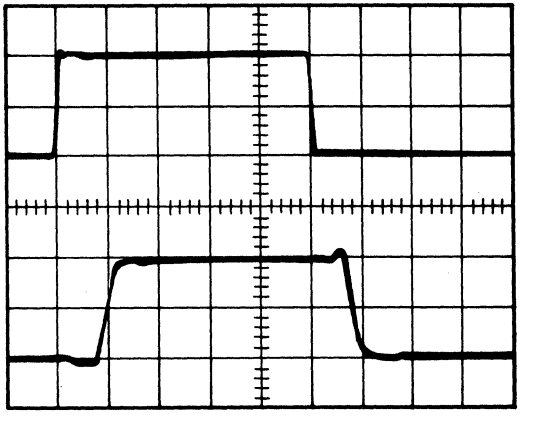
SWITCHING WAVEFORMS

TOP: TTL INPUT (1V/DIV)
V_{AH} = 3V, V_{AL} = 0.8V
BOTTOM: OUTPUT (5V/DIV)



200ns/DIV

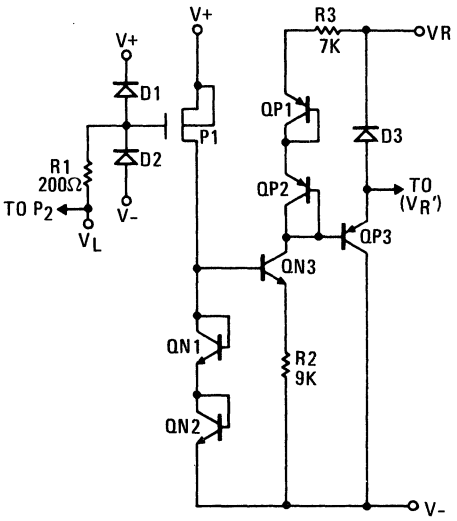
TOP: CMOS INPUT (5V/DIV)
V_{AH} = 10V, V_{AL} = 0V
BOTTOM: OUTPUT (5V/DIV



200ns/DIV

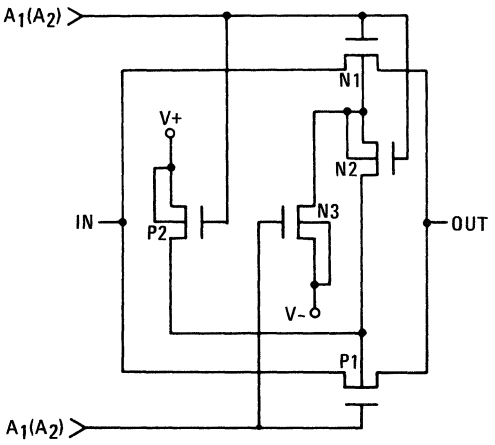
SCHEMATIC DIAGRAMS

TTL/CMOS REFERENCE CIRCUIT*

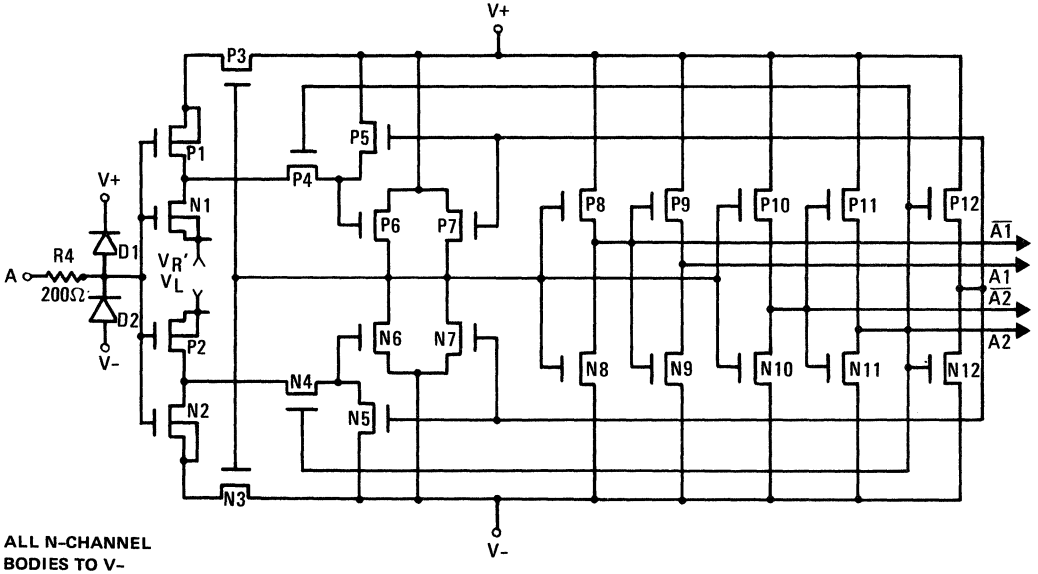


*Connect V^+ to V_L for minimizing power consumption when driving from CMOS circuits

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



ALL N-CHANNEL BODIES TO V-

ALL P-CHANNEL BODIES TO V+

EXCEPT AS SHOWN

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-506/HI-507

Single 16/Differential 8 Channel CMOS Analog Multiplexers

FEATURES

- LOW ON RESISTANCE (TYP.) 170Ω
- WIDE ANALOG SIGNAL RANGE ±15V
- DIRECTLY TTL/CMOS COMPATIBLE 2.4V (LOGIC "1")
- ACCESS TIME (TYP.) 300ns
- HIGH CURRENT CAPABILITY (TYP.) 50mA
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

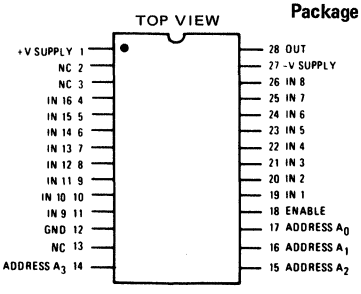
The HI-506/507 are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit input for disabling all channels. Dielectric Isolation (DI) is used to fabricate these devices for enhanced reliability and performance over conventional Junction-Isolated (JI) devices. (See Application Note 521). Substrate leakages and parasitic capacitance are much lower in DI resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.3nA) and low channel ON resistance (170Ω) assure optimum performance in low level or current mode applications. Operation is specified with nominal ±15V supplies, however, supplies as low as ±7V can be used at somewhat lower performance. The HI-506/507 internally develops a +5V digital logic reference from the positive supply which eliminates an additional supply and provides direct TTL/CMOS compatibility without interface pull-up resistors.

The HI-506 is a single-ended 16 channel multiplexer while the HI-507 is a differential 8 channel version. Either device is ideally suited for medical instrumentation, telemetry systems and microprocessor based data acquisition systems.

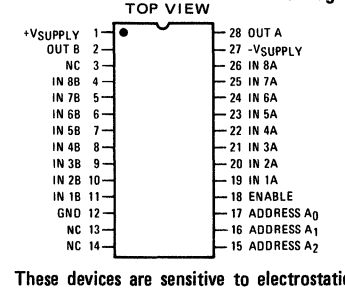
The HI-506-2 and HI-507-2 are specified over -55°C to +125°C, while the -5 versions are specified over 0°C to +75°C.

PINOUT

HI-506 TOP VIEW **Package Code 1M**

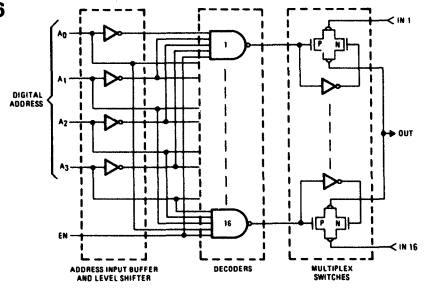


HI-507 TOP VIEW **Package Code 1M**

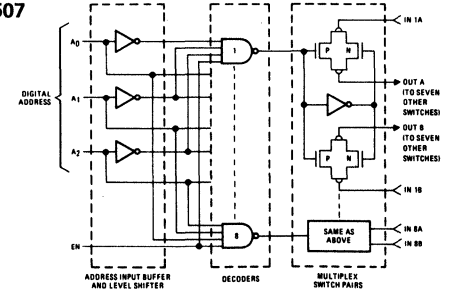


FUNCTIONAL DIAGRAM

HI-506



HI-507



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 — 40V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { V_{Supply} (+) +4V; V_{Supply} (-) -4V

Analog Input Overvoltage: (Note 6)

V_D or V_S { V_{Supply} (+) +2V; V_{Supply} (-) -2V

Total Power Dissipation* — 1200 mW

Operating Temperature:

HI-506/HI-507-2 — -55°C to +125°C

HI-506/HI-507-5 — 0°C to +75°C

Storage Temperature — -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: Supplies = +15V, -15V; V_{AH}(Logic Level High) = +2.4V, V_{AL}(Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics section.

		HI-506/HI-507-2 -55°C to +125°C			HI-506/HI-507-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
* V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C Full		170	300 400		270	400 500	Ω Ω
* ΔR_{ON}, (Between Channels)	+25°C		6			6		%
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C Full		0.03	 ±50		0.03	 ±50	nA nA
* $I_{D(OFF)}$, Off Output Leakage Current HI-506 HI-507	+25°C Full Full		0.3	 ±500 ±250		1.0	 ±500 ±250	nA nA nA
* $I_{D(ON)}$, On Channel Leakage Current HI-506 HI-507	+25°C Full Full		0.3	 ±500 ±250		1.0	 ±500 ±250	nA nA nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			+0.8			+0.8	V
V_{AH}, Input High Threshold	Full	+2.4			+2.4			V
* I_A, Input Leakage Current (High or Low)(Note 2)	Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		300	1000		300		ns
t_{OPEN}, Break-Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300	1000		300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300	1000		300		ns
Settling Time (0.1%) (0.025%)	+25°C +25°C		1.2 2.4			1.2 2.4		μs μs
"Off Isolation" (Note 3)	+25°C		75			75		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		4			4		pF
$C_{D(OFF)}$, Channel Output Capacitance HI-506 HI-507	 +25°C +25°C		 44 22			 44 22		 pF pF
C_A, Digital Input Capacitance	+25°C		2.2			2.2		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.08			0.08		pF
POWER REQUIREMENTS								
* I+, Current Pin 1 (Note 4)	Full		1.7	3.0		3.4	5.0	mA
* I-, Current Pin 27 (Note 4)	Full		0.4	1.0		0.8	2.0	mA
* I+, Standby (Note 5)	Full		1.7	3.0		3.4	5.0	mA
* I-, Standby (Note 5)	Full		0.4	1.0		0.8	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -1mA
2. Digital Inputs are Mos Gates. Typical Leakage Less Than 1nA.
3. V_{EN} = 0.8V, R_L = 1K, C_L = 28pF, V_S = 7VRMS, f = 500kHz.
4. V_{EN} = 4.0V, All V_A = 4.0V
5. V_{EN} = 0V, All V_A = 0V
6. If Analog Input Overvoltage Conditions are Anticipated, Use of HI-506A/507A Protected Multiplexers is Recommended. See HI-506A/507A Data Sheet.

*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)

TRUTH TABLES

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

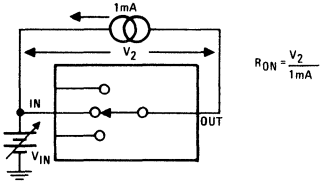
HI-507

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Unless Otherwise Specified; $T_A = 25^oC$, $V_{Supply} = \pm 15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$.

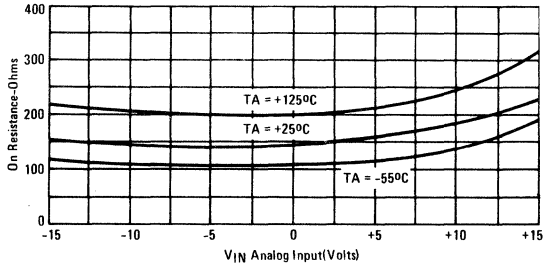
TEST CIRCUIT NO. 1

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

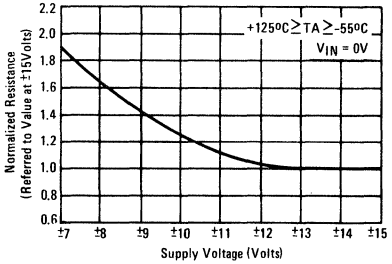


$R_{ON} = \frac{V_2}{1mA}$

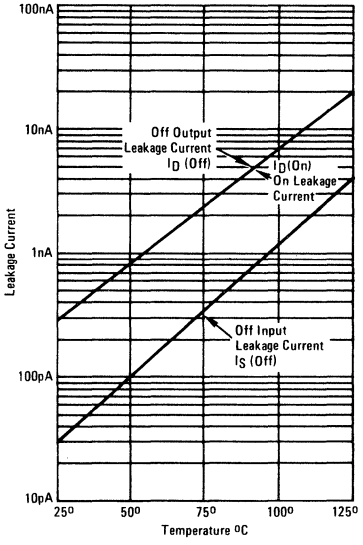
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE

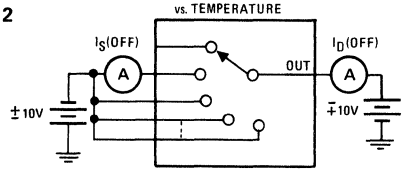


LEAKAGE CURRENT vs. TEMPERATURE



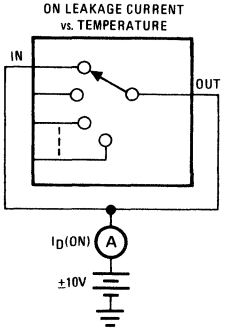
TEST CIRCUIT NO. 2

OFF LEAKAGE CURRENT vs. TEMPERATURE

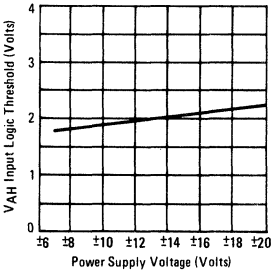


TEST CIRCUIT NO. 3

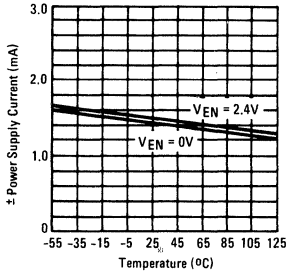
ON LEAKAGE CURRENT vs. TEMPERATURE



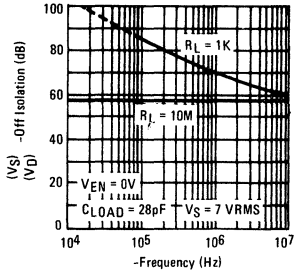
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



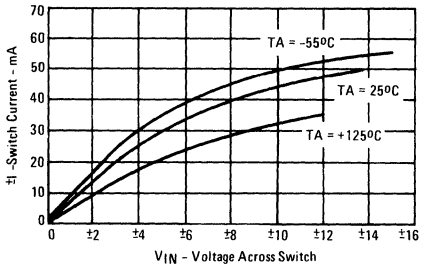
POWER SUPPLY CURRENT vs. TEMPERATURE



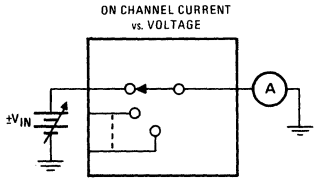
OFF ISOLATION vs. FREQUENCY



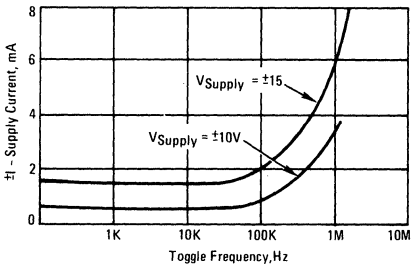
ON CHANNEL CURRENT vs. VOLTAGE



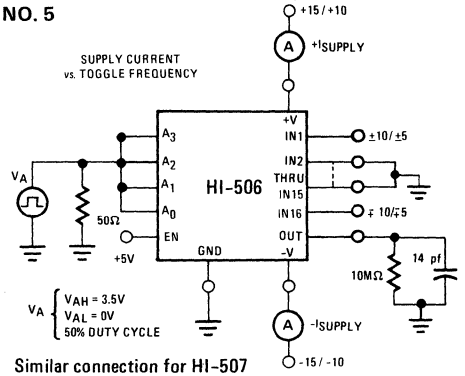
TEST CIRCUIT NO. 4



SUPPLY CURRENT vs. TOGGLE FREQUENCY

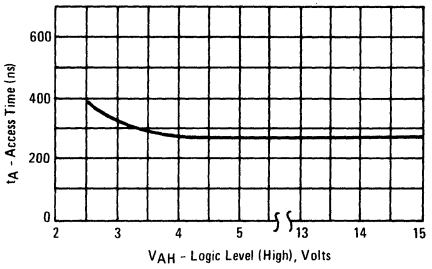


TEST CIRCUIT NO. 5

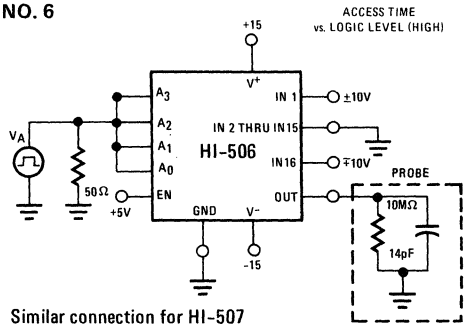


Similar connection for HI-507

ACCESS TIME vs. LOGIC LEVEL (HIGH)

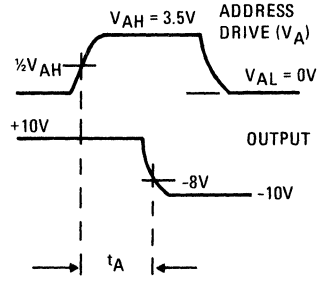


TEST CIRCUIT NO. 6

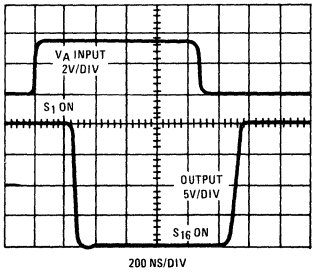


Similar connection for HI-507

SWITCHING WAVEFORMS

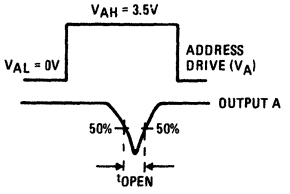


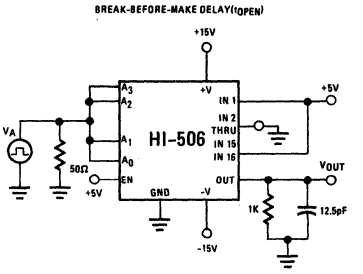
ACCESS TIME



SWITCHING WAVEFORMS (continued)

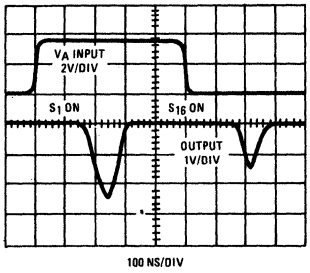
TEST CIRCUIT NO. 7



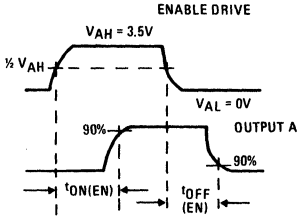


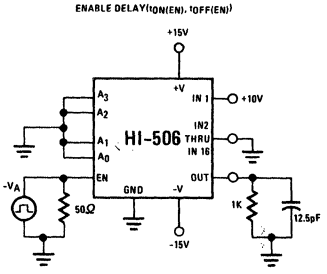
Similar connection for HI-507

BREAK-BEFORE-MAKE DELAY (t_{OPEN})



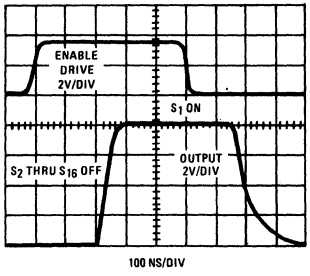
TEST CIRCUIT NO. 8





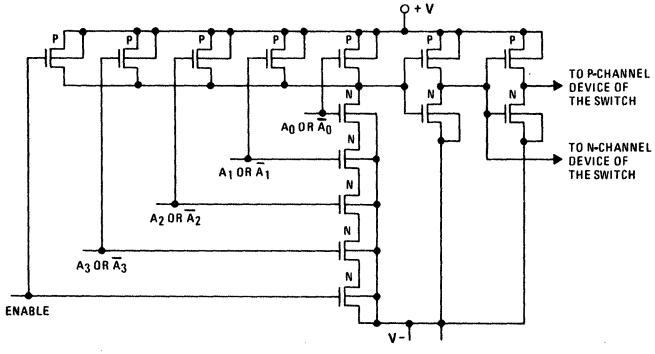
Similar connection for HI-507

ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



SCHEMATIC DIAGRAMS

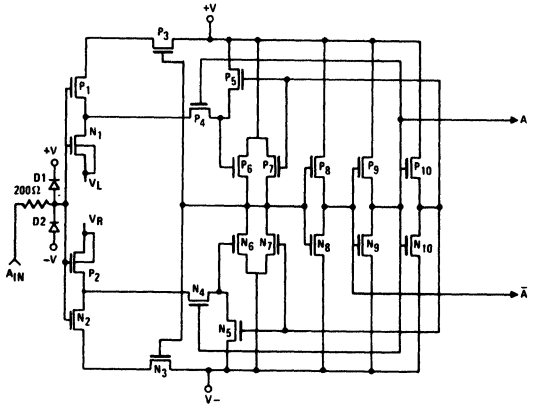
ADDRESS DECODER



Delete A_3 or $\overline{A_3}$ Input for HI-507

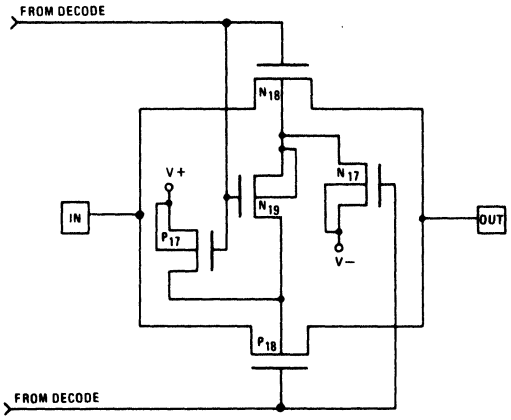
SCHEMATIC DIAGRAM (continued)

ADDRESS INPUT BUFFER LEVER SHIFTER

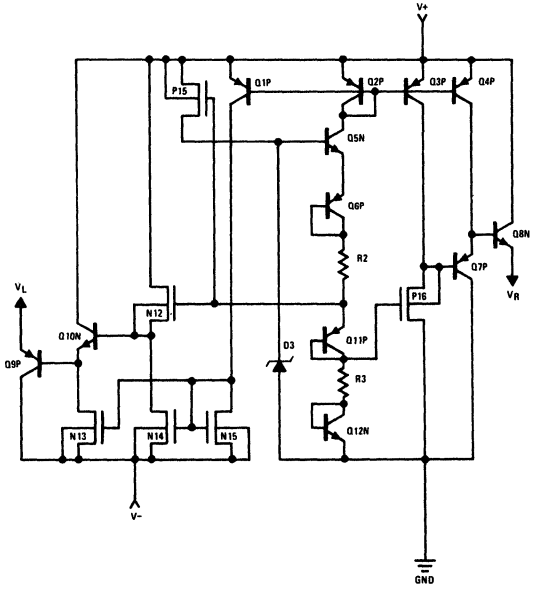


All N-Channel Bodies to V-
All P-Channel Bodies to V+ Unless Otherwise Indicated.

MULTIPLEX SWITCH



TTL REFERENCE CIRCUIT



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-506A/HI-507A

16 Channel CMOS Analog Multiplexer with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

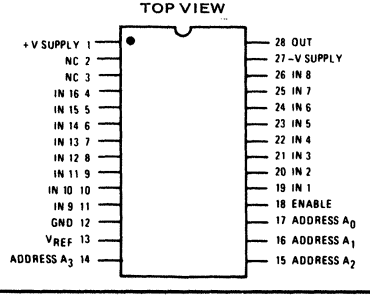
DESCRIPTION

The HI-506A and HI-507A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

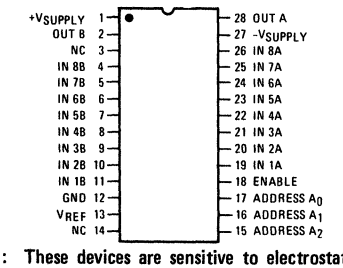
The HI-506A-2 and HI-507A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

PINOUT

HI-506A **Package Code 1M**

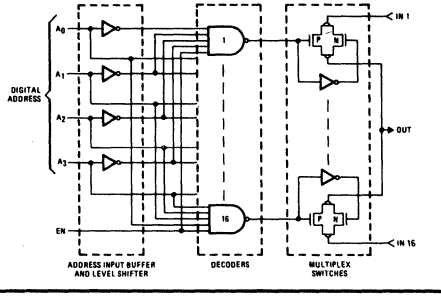


HI-507A **Package Code 1M**

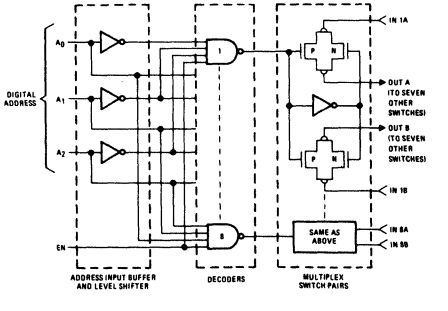


FUNCTIONAL DIAGRAM

HI-506A



HI-507A



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27	40V	Total Power Dissipation*	1200mW
V_{REF} to Ground V+ to Ground	+20V	Operating Temperature	
V_{EN}, V_A, Digital Input Overvoltage:		HI-506A/507A-2	-55°C to +125°C
V_A { V_{Supply} (+)	+4V	HI-506A/507A-5	0°C to +75°C
V_A { V_{Supply} (–)	-4V	Storage Temperature	-65°C to +150°C
Analog Overvoltage:			
V_S { V_{Supply} (+)	+20V		
V_S { V_{Supply} (–)	-20V	*Derate 8mW/°C above T_A = +25°C	

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characterisitcs section.

PARAMETER	TEMP.	HI-506A/507A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-506A/507A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	2.0		1.8	2.0	KΩ
*I_S (OFF), Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
*I_D (OFF), Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-506A	Full			±500			±500	nA
HI-507A	Full			±250			±250	nA
*I_D (OFF) with Input Overvoltage Applied	+25°C		4.0			4.0		nA
(Note 2)	Full			2.0				μA
*I_D (ON), On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-506A	Full			±500			±500	nA
HI-507A	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold } TTL Drive	Full			0.8			0.8	V
V_{AH}, Input High Threshold } (Note 7)	Full	4.0			4.0			V
V_{AL} } MOS Drive (Note 3)	+25°C			0.8			0.8	V
V_{AH} }	+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break-Before Make Delay	+25°C		80			80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		300			300		ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		300			300		ns
Settling Time (0.1%)	+25°C		1.3			1.3		μs
(0.025%)	+25°C		4.4			4.4		μs
"Off Isolation" (Note 4)	+25°C		65			65		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-506A	+25°C		50			50		pF
HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current Pin 1 (Note 5)	Full		0.5	2.0		0.5	5.0	mA
*I-, Current Pin 27 (Note 5)	Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 6)	Full		0.5	2.0		0.5	5.0	mA
*I-, Standby (Note 6)	Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = - 100 μA.
2. Analog Overvoltage = ±33V.
3. V_{REF} = +10V.
4. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500KHz.
5. V_{EN} = +4.0V.
6. V_{EN} = 0.8V.
7. To drive from DTL/TTL circuits, 1KΩ pull-up resistors to +5.0V supply are recommended.

*100% Tested for Dash 8.
("Full" Tested at +25°C to +125°C)

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

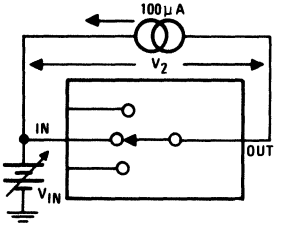
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$ AND V_{REF} = OPEN.)

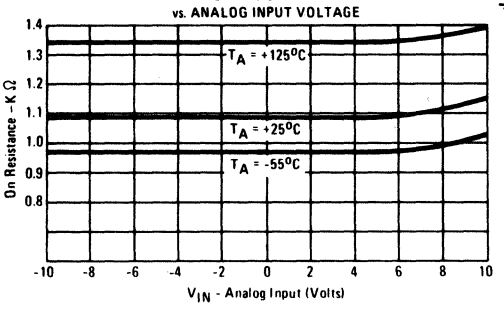
TEST CIRCUIT NO.1

$$R_{ON} = \frac{V_2}{100\mu A}$$

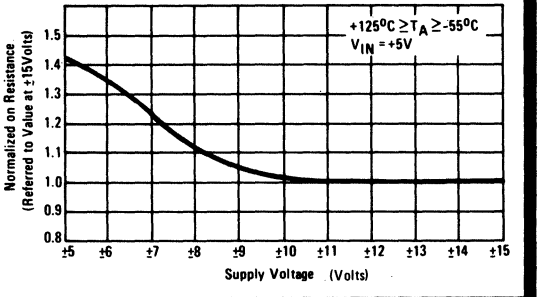
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE



ON RESISTANCE vs. ANALOG INPUT VOLTAGE

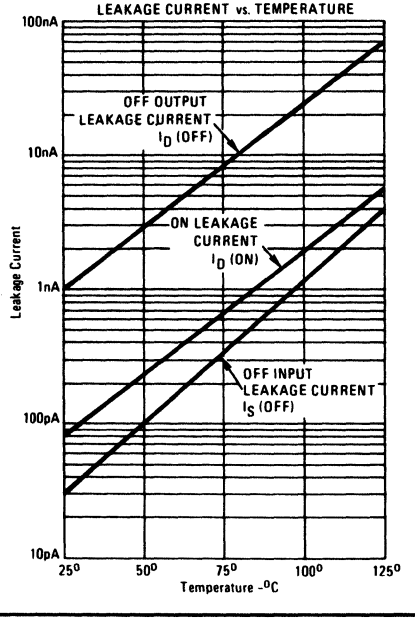


NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



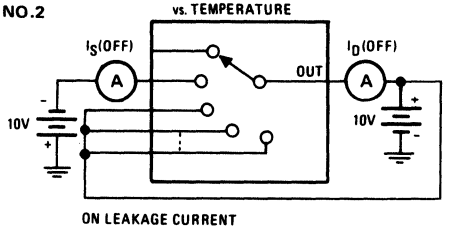
3

LEAKAGE CURRENT vs. TEMPERATURE



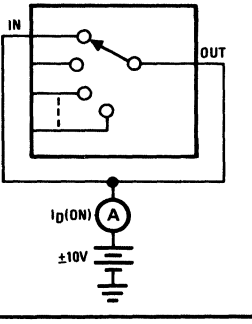
TEST CIRCUIT NO.2

OFF LEAKAGE CURRENT vs. TEMPERATURE

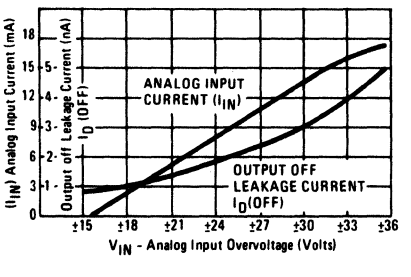


ON LEAKAGE CURRENT vs. TEMPERATURE

TEST CIRCUIT NO.3

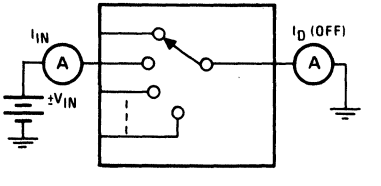


ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

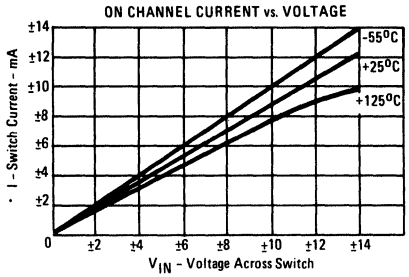


ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

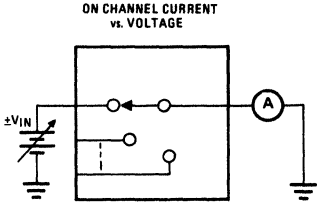
TEST CIRCUIT NO.4

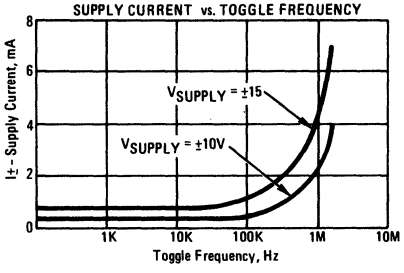


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

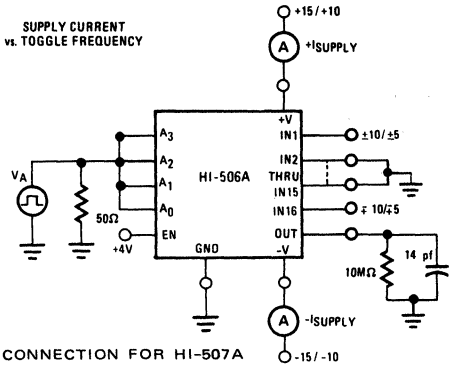


TEST CIRCUIT NO.5

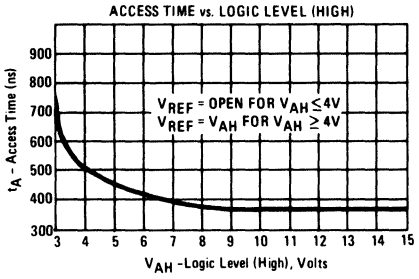




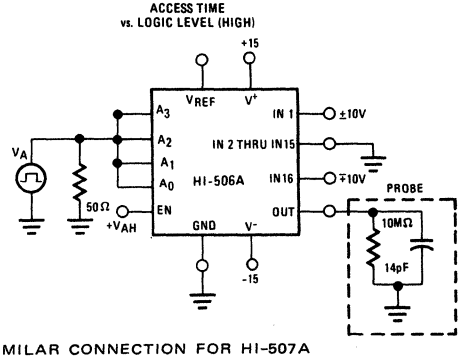
TEST CIRCUIT NO.6



SIMILAR CONNECTION FOR HI-507A

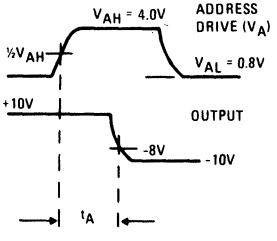


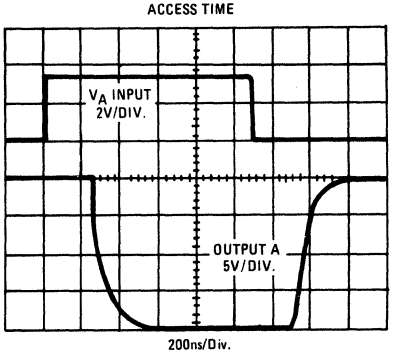
TEST CIRCUIT NO.7



SIMILAR CONNECTION FOR HI-507A

SWITCHING WAVEFORMS

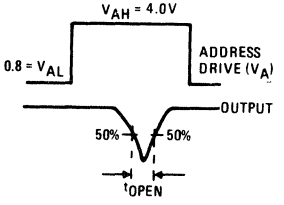


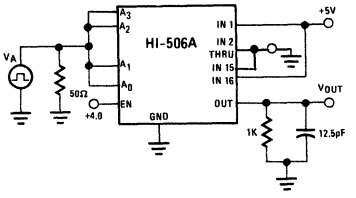


SWITCHING WAVEFORMS (continued)

TEST CIRCUIT
NO.8

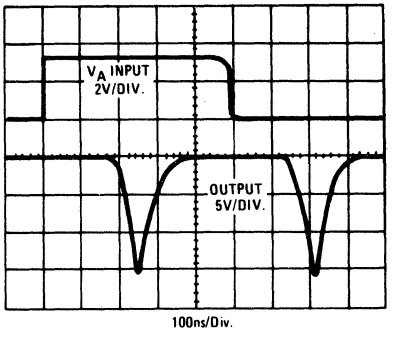
BREAK BEFORE MAKE DELAY (t_{OPEN})





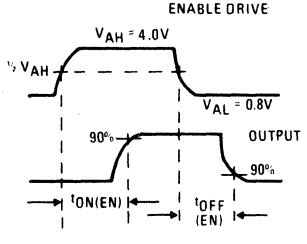
SIMILAR CONNECTION FOR HI-507A

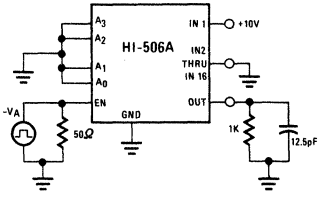
BREAK BEFORE MAKE DELAY (t_{OPEN})



TEST CIRCUIT
NO.9

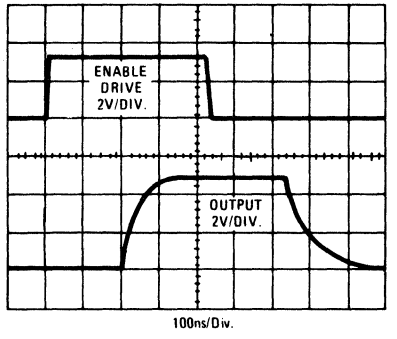
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)





SIMILAR CONNECTION FOR HI-507A

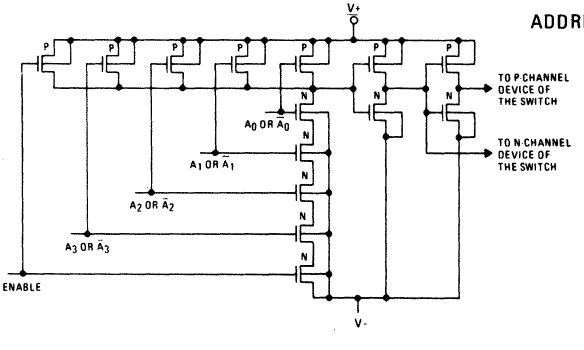
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

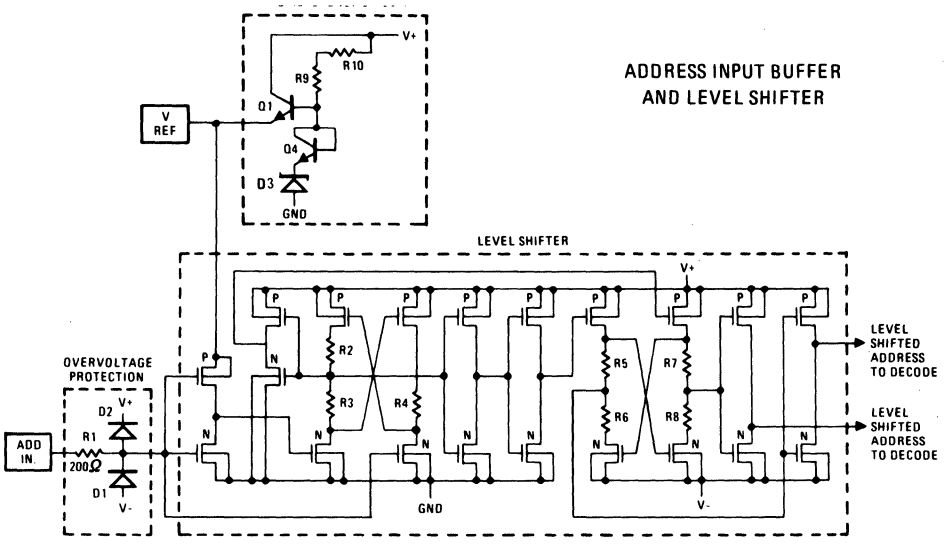


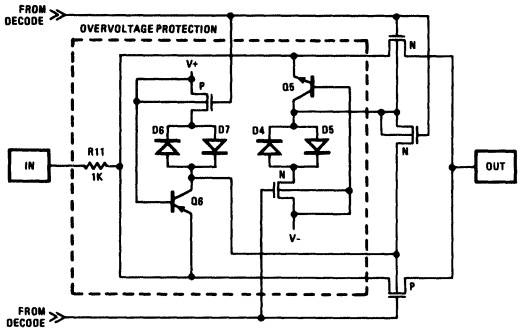
SCHEMATIC DIAGRAMS

DELETE A_3 or $\overline{A}_3$
INPUT FOR HI-507A

ADDRESS DECODER




ADDRESS INPUT BUFFER
AND LEVEL SHIFTER
V+
R10
R9
Q1
V REF
Q4
D3
GND
LEVEL SHIFTER
OVERVOLTAGE
PROTECTION
D2
R1
200Ω
ADD
IN
D1
V-
R2
R3
R4
R5
R6
R7
R8
GND
LEVEL
SHIFTED
ADDRESS
TO DECODE
LEVEL
SHIFTED
ADDRESS
TO DECODE


MULTIPLEX SWITCH
FROM
DECODE
OVERVOLTAGE PROTECTION
V+
Q5
D6
D7
D4
D5
IN
R11
1K
Q6
V-
OUT
FROM
DECODE

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-508A/509A

8 Channel CMOS Analog Multiplexers with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

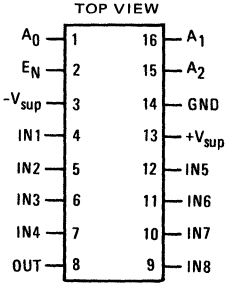
The HI-508A and HI-509A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

The HI-508A-2 and HI-509A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

PINOUT

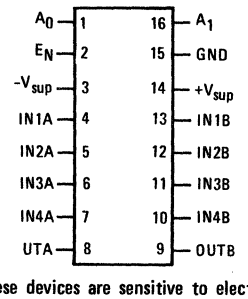
HI-508A — **Package Code 4B**

TOP VIEW



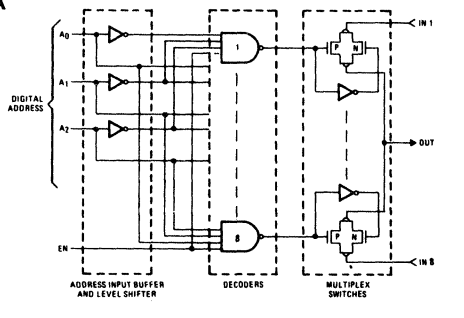
HI-509A — **Package Code 4B**

TOP VIEW

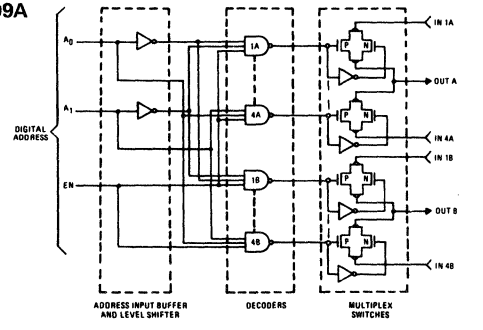


FUNCTIONAL DIAGRAM

HI-508A



HI-509A



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins 40V

V+ to Ground 20V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { V_{Supply} (+) +4V; V_{Supply} (-) -4V

Analog Input Overvoltage:

V_S { V_{Supply} (+) +20V; V_{Supply} (-) -20V

Total Power Dissipation* 725 mW

Operating Temperature:

HI-508A/HI-509A-2 -55°C to +125°C

HI-508A/HI-509A-5 0°C to +75°C

Storage Temperature -65°C to +150°C

*Derate 8mW/°C above t_A = 75°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characterisitcs section.

PARAMETER	TEMP.	HI-508A/509A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-508A/509A-5 0°C to +75°C MIN.	TYP	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
*$I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
*$I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-508A	Full			±250			±250	nA
*$I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				μA
*$I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-508A	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold (Note 6)	Full			0.8			0.8	V
V_{AH}, Input High Threshold (Note 6)	Full	4.0			4.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break - Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300			300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300			300		ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.0 25%)	+25°C		3.5			3.5		μs
"OFF Isolation" (Note 3)	+25°C		65			65		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D(OFF)}$, Channel Output Capacitance								
HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current (Note 4)	Full		0.5	2.0		0.5	5.0	mA
*I-, Current (Note 4)	Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 5)	Full		0.5	2.0		0.5	5.0	mA
*I-, Standby (Note 5)	Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100μA
2. Analog Overvoltage = ±33V
3. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3V RMS, f = 500KHz
4. V_{EN} = +4.0V
5. V_{EN} = 0.8V
6. To drive from DTL/TTL Circuits, 1KΩ pull-up resistors to +5.0V supply are recommended

*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)

TRUTH TABLES

HI-508A

A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

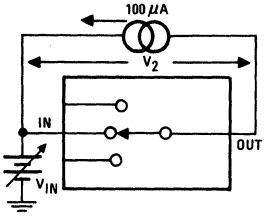
A_1	A_0	EN	ON SWITCH PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

UNLESS OTHERWISE SPECIFIED: $T_A = 25^oC$, $V_{SUPPLY} = +15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$

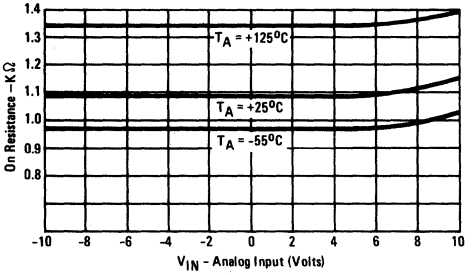
TEST CIRCUIT NO. 1

$R_{ON} = \frac{V_2}{100\mu A}$

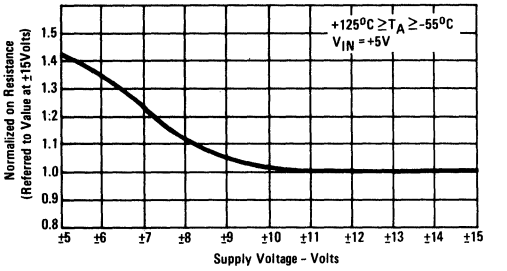


ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

ON RESISTANCE vs. ANALOG INPUT VOLTAGE

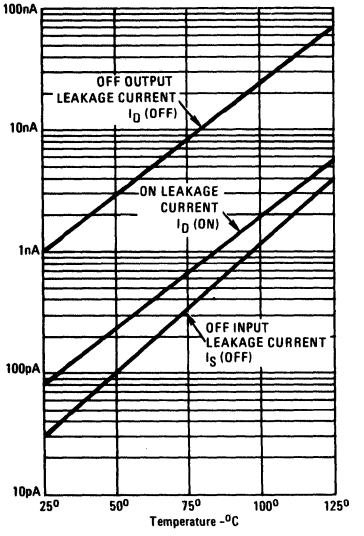


NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



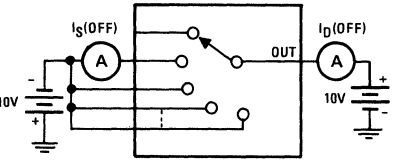
3

LEAKAGE CURRENT vs. TEMPERATURE



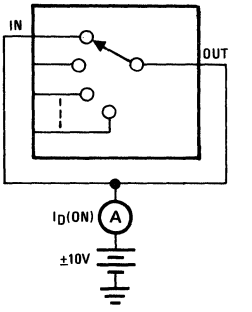
TEST CIRCUIT NO. 2

OFF LEAKAGE CURRENT vs. TEMPERATURE

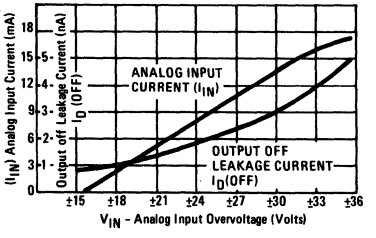


ON LEAKAGE CURRENT vs. TEMPERATURE

TEST CIRCUIT NO. 3

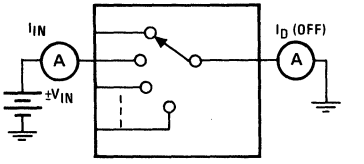


ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



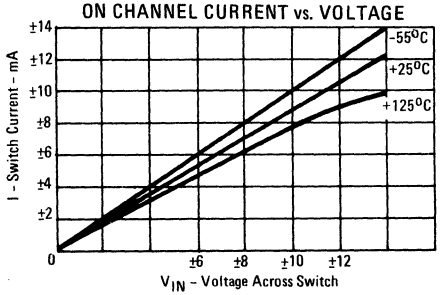
TEST CIRCUIT NO. 4

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



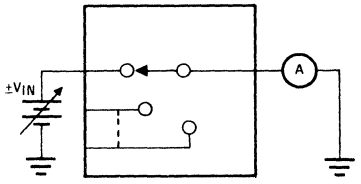
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

ON CHANNEL CURRENT vs. VOLTAGE

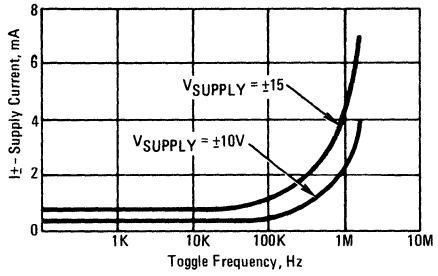


TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

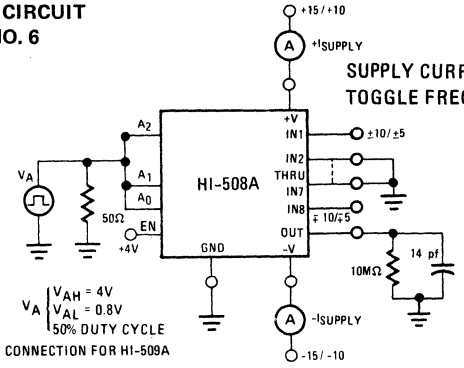


SUPPLY CURRENT vs. TOGGLE FREQUENCY



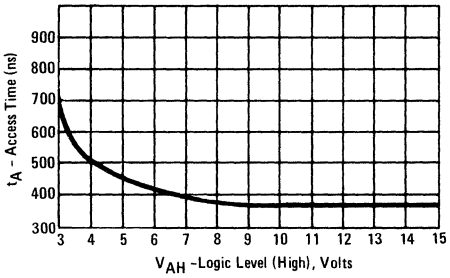
TEST CIRCUIT NO. 6

SUPPLY CURRENT vs. TOGGLE FREQUENCY



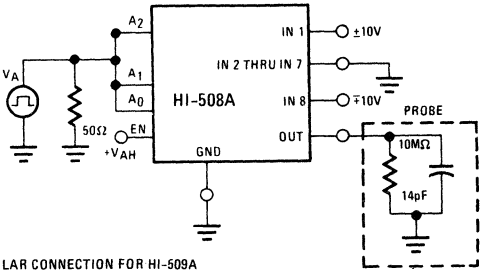
*SIMILAR CONNECTION FOR HI-509A

ACCESS TIME vs. LOGIC LEVEL (HIGH)



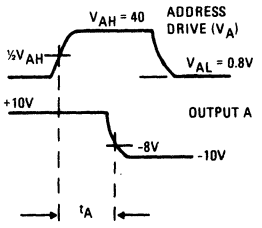
TEST CIRCUIT NO. 7

ACCESS TIME vs. LOGIC LEVEL(HIGH)

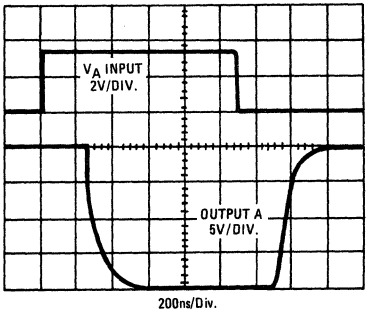


* SIMILAR CONNECTION FOR HI-509A

SWITCHING WAVEFORMS



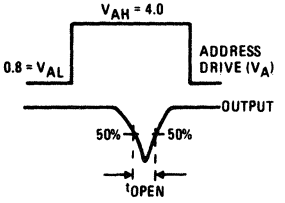
ACCESS TIME

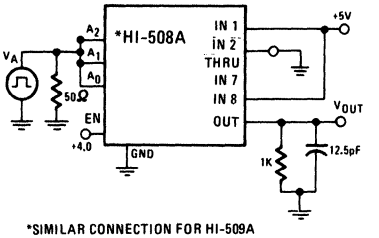


3

SWITCHING WAVEFORMS (continued)

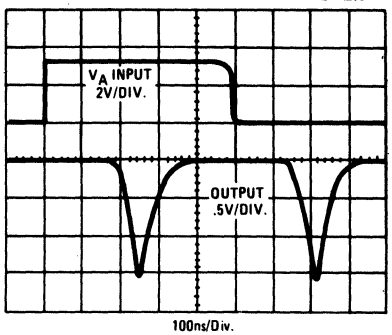
TEST CIRCUIT
NO. 8
BREAK BEFORE MAKE DELAY (t_{OPEN})



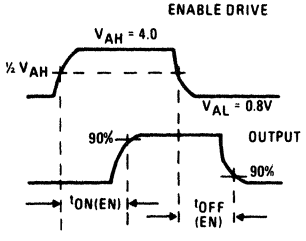


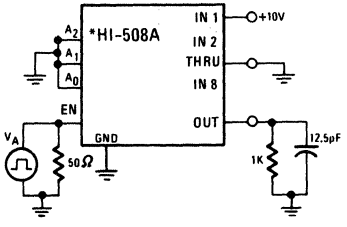
*SIMILAR CONNECTION FOR HI-509A

BREAK BEFORE MAKE DELAY (t_{OPEN})



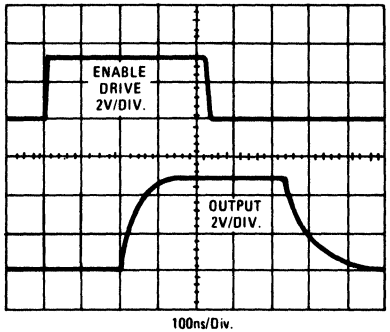
TEST CIRCUIT
NO. 9
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



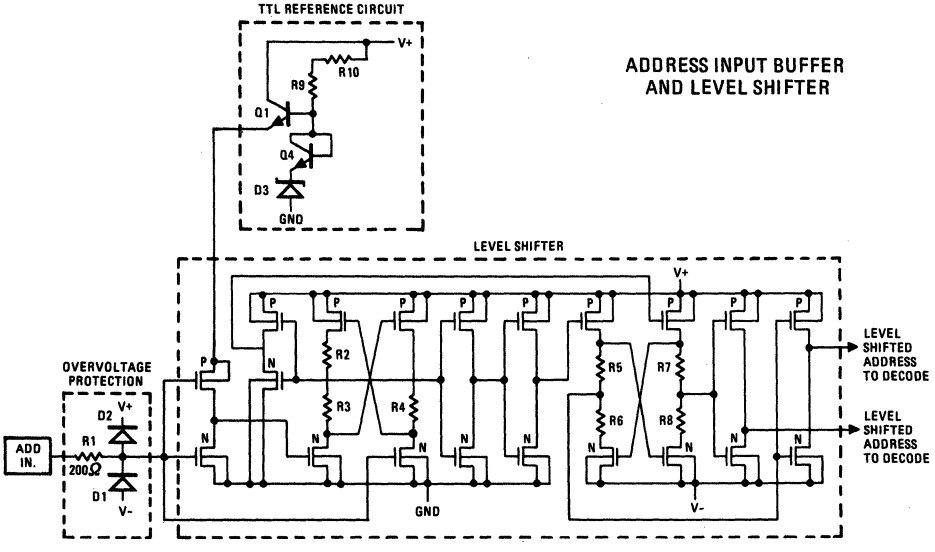


* SIMILAR CONNECTION FOR HI-509A

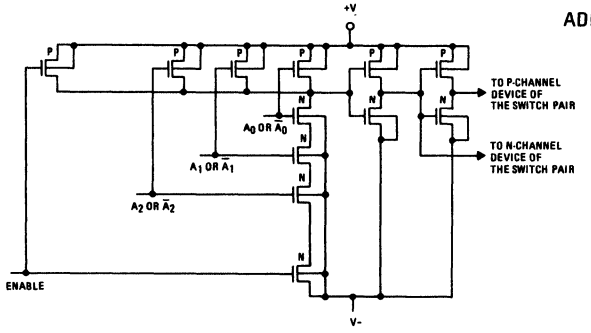
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



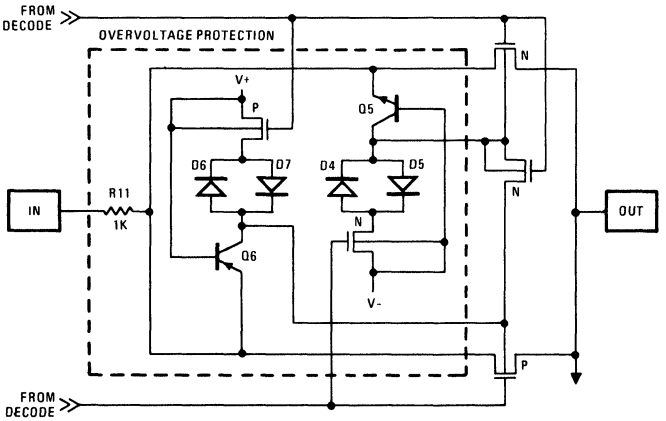
SCHEMATIC DIAGRAMS



ADDRESS DECODER



MULTIPLEX SWITCH



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-1818A/1828A

Low Resistance 8 Channel CMOS Analog Multiplexers

FEATURES

- SIGNAL RANGE ±15V
- "ON" RESISTANCE (TYP.) 250Ω
- INPUT LEAKAGE AT +125°C (TYP.) 20nA
- ACCESS TIME (TYP.) 350ns
- POWER CONSUMPTION (TYP.) 5mW
- DTL/TTL COMPATIBLE ADDRESS
- -55°C to +125°C OPERATION

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

The HI-1818A/1828A are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250Ω) assure optimum performance in low level or current mode applications.

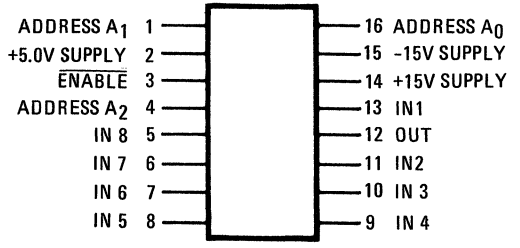
The 1818A is a single-ended 8 channel multiplexer, while the HI-1828A is a differential 8 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

The HI-1818A-2 and HI-1828A are specified over -55°C to +125°C, while the -5 versions are specified over 0°C to +75°C.

PINOUT

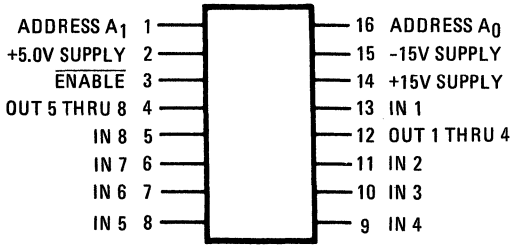
HI-1818A

Top View — Package Code 4B



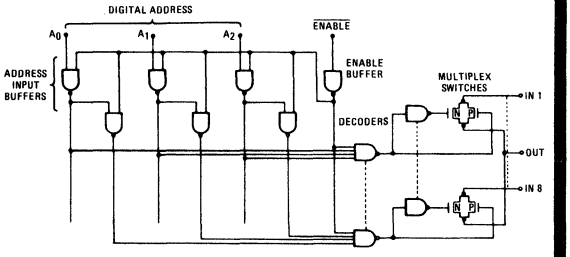
HI-1828A

Top View — Package Code 4B

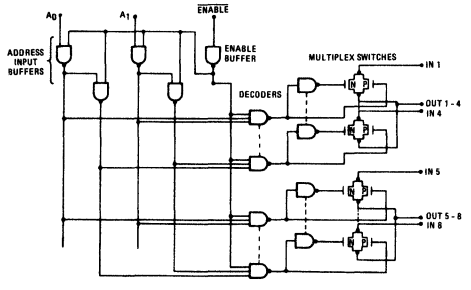


FUNCTIONAL DIAGRAM

HI-1818A



HI-1828A



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	V-Supply to V+ Supply
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation (Note 2)	780mW
Analog Input Voltage: V^+_{Supply}	+2V	Storage Temperature Range	-65°C to +150°C
V^-_{Supply}	-2V		

ELECTRICAL CHARACTERISTICS

Supplies = +15V, -15V, +5V

PARAMETER	TEMP.	HI-1818A-2/1828A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-1818A-5/1828A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_{IN}, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, ON Resistance (Note 3)	+25°C		250	400		250	400	Ω
	Full		300	500		300	500	Ω
*I_S(OFF), Input Leakage Current	Full		20	50		20	50	nA
*I_D(ON), On Channel Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
*I_D(OFF) Output Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{IL}, Input Low Threshold	Full			0.4			0.4	V
V_{IH}, Input High Threshold (Note 4)	Full	4.0			4.0			V
*I_{IN}, Input Leakage Current	Full		.01	1		.01	1	μA
SWITCHING CHARACTERISTICS								
T_S, Access Time (Note 5)	+25°C		350			350		ns
Break-Before-Make Delay	+25°C		100			100		ns
Settling Time (0.1%)	+25°C		1.08			1.08		μs
(0.025%)	+25°C		2.8			2.8		μs
C_{IN}, Channel Input Capacitance	+25°C		4			4		pF
C_{OUT}, Channel Output Capacitance								
(HI-1818A)	+25°C		20			20		pF
(HI-1828A)	+25°C		10			10		pF
C_{DS}(OFF), Drain-To-Source Capacitance	+25°C		0.6			0.6		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		5			5		mW
P_{DS}, Standby Power (Note 6)	Full		5			5		mW
*I_+, Current Pin 14	Full		0.1	0.5		0.1	1	mA
*I_-, Current Pin 15	Full		0.3	1		0.3	2	mA
*I_L, Current Pin 2	Full		0.3	1		0.3	2	mA

NOTES:
1. Voltage ratings apply when voltages at all other pins are within their normal operating ranges.
2. Derate 9.25 mW/°C above 75°C.
3. V_{OUT} = ± 10V I_{OUT} = - 1mA.
4. To drive from DTL/TTL circuits, 1K pull-up resistors to + 5.0V supply are recommended.
5. Time measured to 90% of final output level; V_{OUT} = - 5.0V to +5.0V, Digital Inputs = 0V to + 4.0V.
6. Voltage at Pin 3, $\overline{ENABLE}$ = + 4.0V.

*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)

TRUTH TABLES

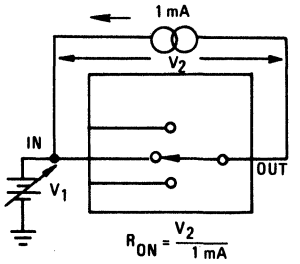
HI-1818A

ADDRESS A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	NONE

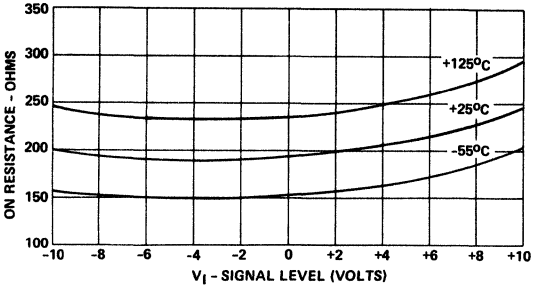
HI-1828A

ADDRESS A_1	A_0	$\overline{EN}$	"ON" CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	NONE

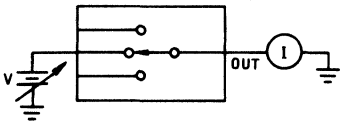
ON RESISTANCE vs ANALOG SIGNAL LEVEL



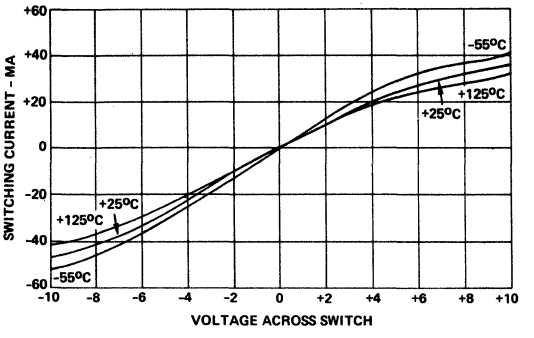
Test Circuit



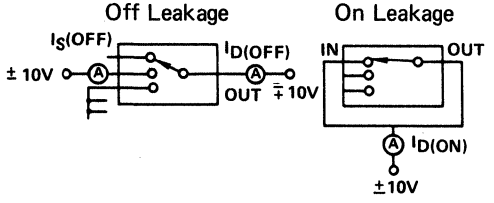
ON CHANNEL CURRENT vs VOLTAGE

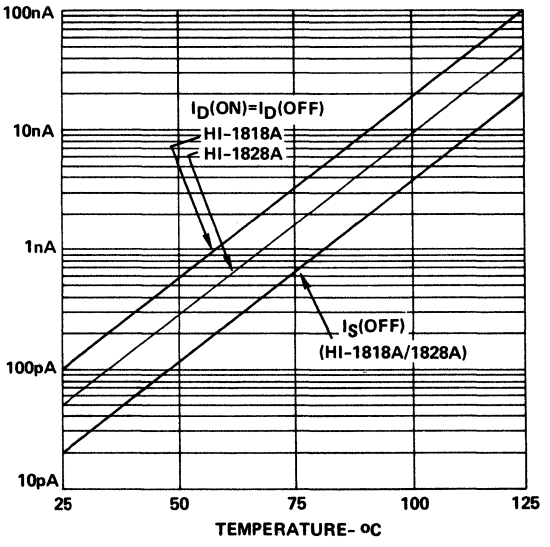


Test Circuit

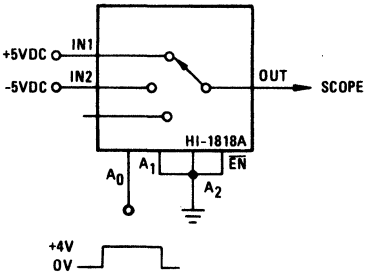


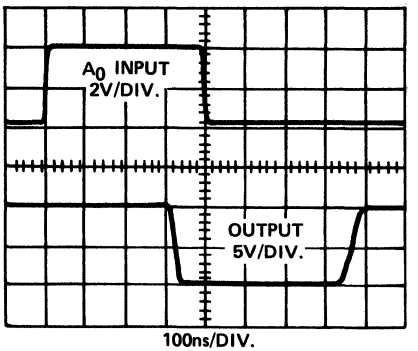
ON/OFF LEAKAGE CURRENTS vs TEMPERATURE





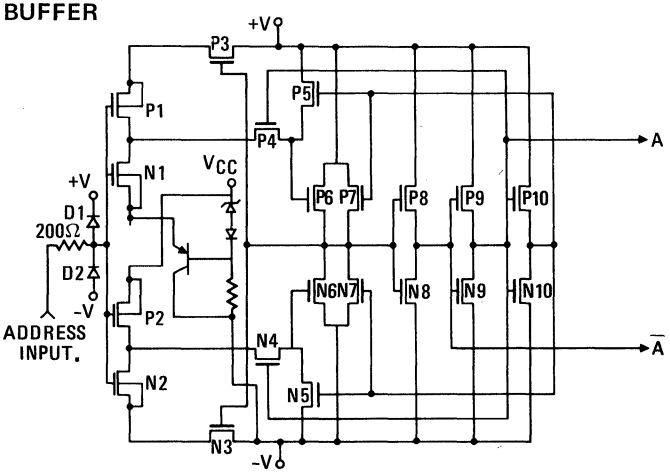
ACCESS TIME





SCHEMATIC DIAGRAM

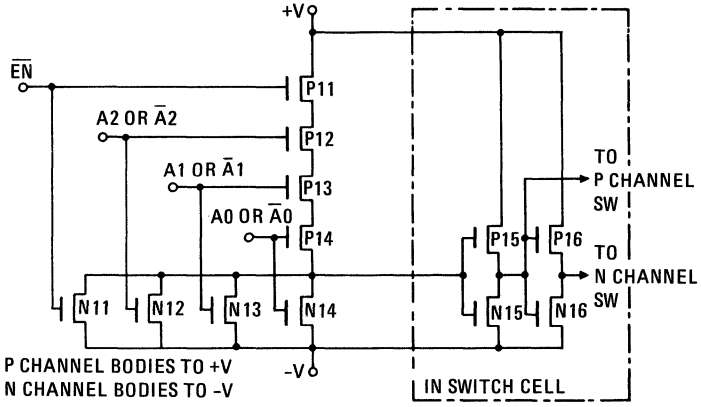
ADDRESS INPUT BUFFER



ALL N-CHANNEL BODIES TO V-

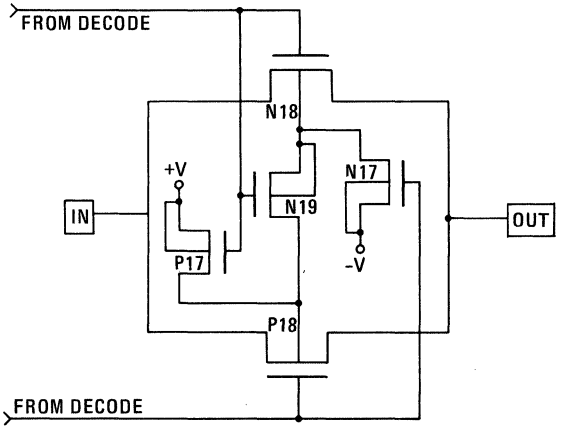
ALL P-CHANNEL BODIES TO V+ UNLESS OTHERWISE INDICATED.

DECODER GATE



A2 OR Ā2 NOT USED FOR HI-1828A

MULTIPLEX SWITCH



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-1840

16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection

FEATURES

- HIGH ANALOG INPUT IMPEDANCE DURING POWER LOSS (OPEN) 500MΩ
- LOW POWER CONSUMPTION (STANDBY) 600μW
- ACCESS TIME 500ns
- EXCELLENT IN HI-REL REDUNDANT SYSTEMS
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- FAIL-SAFE DATA ACQUISITION SYSTEMS
- FAIL-SAFE TELEMETRY SYSTEMS
- AIRCRAFT INSTRUMENTATION AND CONTROL

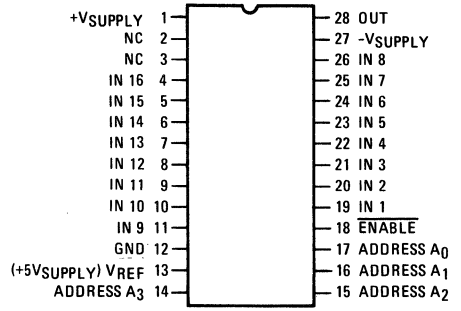
DESCRIPTION

The HI-1840 is a monolithic 16 channel multiplexer constructed with the Harris Linear Dielectric Isolation CMOS process. It is designed to provide a high input impedance to the analog source if device power fails (open) or the analog signal voltage inadvertently exceeds the supply rails during powered operation. Excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. But more significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. All digital inputs have electrostatic discharge protection. The HI-1840 is tested and guaranteed within the military temperature range and is available in a 28 pin dual-in-line package.

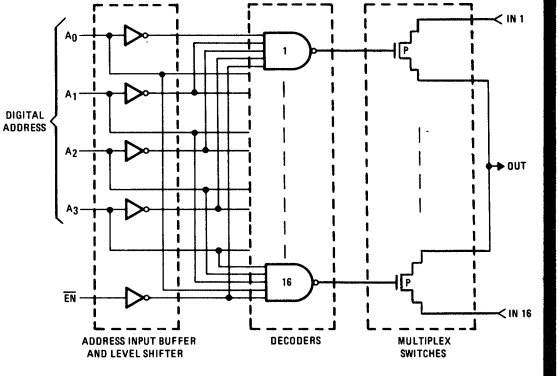
PINOUT

Package Code 1M

Top View



FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 +40V
V_{REF} to Ground +20V
V_{EN}, V_A, Digital Input Overvoltage:
V_A V_{Supply} (+) +4V
V_{Supply} (-) -4V
Analog Input Overvoltage:
V_S V_{Supply} (+) +10V
V_{Supply} (-) -10V

Total Power Dissipation* 1200mW
Operating Temperature:
HI-1840-2 -55°C to +125°C
Storage Temperature -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified:
Supplies = +15V, -15V: V_{REF}(Pin 13) = +5V; V_{AH}(Logic Level High) = 4.0V; V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	-55°C to +125°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS					
*V_S, Analog Signal Range	Full	-5		+15	V
*R_{ON}, On Resistance (Note 1) V_{IN} = +15V	Full		0.5	1.0	KΩ
V_{IN} = -5V	Full		2.5	5.0	KΩ
*I_S(OFF), Off Input Leakage Current	+25°C		0.03		nA
	Full			±100	nA
*I_S(OFF), with Power Off (Note 8)	Full			±100	nA
*I_D(OFF), Off Output Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
* I_D(OFF), or I_S(OFF) with Input Overvoltage Applied (Note 2)	+25°C		50		nA
	Full			±1000	nA
*I_D(ON), On Channel Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold | TTL Drive	Full			0.8	V
V_{AH}, Input High Threshold | (Note 7)	Full	4.0			V
V_{AL} | MOS Drive (Note 3)	+25°C			0.8	V
V_{AH} |	+25°C	6.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0	µA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		500	1000	ns
t_{OPEN}, Break-Before-Make Delay	+25°C	20	80		ns
t_{ON}(EN), Enable Delay (ON)	+25°C		300	1000	ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		300	1000	ns
Settling Time (0.1%)	+25°C		1.2		µs
(0.025%)	+25°C		4.1		µs
"Off Isolation" (Note 4)	+25°C		65		dB
C_S(OFF), Channel Input Capacitance	+25°C		5		pF
C_D(OFF), Channel Output Capacitance :	+25°C		50		pF
C_A, Digital Input Capacitance	+25°C		5		pF
C_{DS}(OFF), Input ot Output Capacitance	+25°C		0.15		pF
POWER REQUIREMENTS					
P_D, Power Dissipation (Note 5)	+25°C		0.6	15.0	mW
(Note 6)	+25°C		0.6	15.0	mW
*I+, Current Pin 1 (Note 5)	Full		0.02	0.5	mA
*I-, Current Pin 27 (Note 5)	Full		0.02	0.5	mA
*I+, Standby (Note 6)	Full		0.02	0.5	mA
*I-, Standby (Note 6)	Full		0.02	0.5	mA

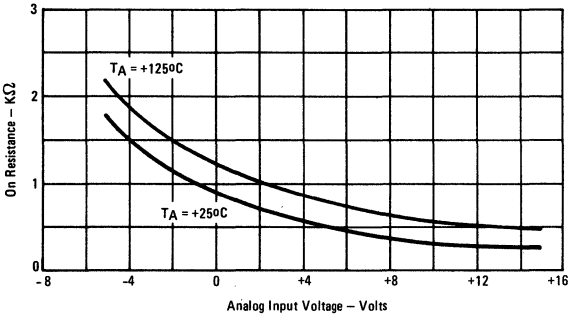
NOTES:
1. I_{OUT} = 1mA
2. Analog Overvoltage = ±20V
3. V_{REF} = +10V
4. V_{EN} = 4.0V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500kHz
5. V_{EN} = 0.8V
6. V_{EN} = 4.0V
7. To drive from DTL/TTL circuits 1K pull-up resistors to +5.0V supply are recommended.
8. All supplies (V+, V-, +5V) and digital inputs (A_0, A_1, A_2, A_3, EN) opened. Analog input ±10V.

TRUTH TABLE

A_3	A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
X	X	X	X	H	NONE
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

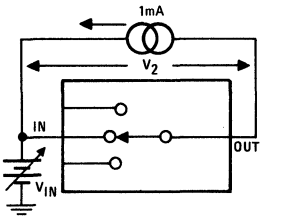
Unless Otherwise Specified: T_A = 25°C, V_{SUPPLY} = ±15V, V_{AH} = +4V, V_{AL} = 0.8V and V_{REF} = 5V.

ON RESISTANCE VS. ANALOG INPUT VOLTAGE

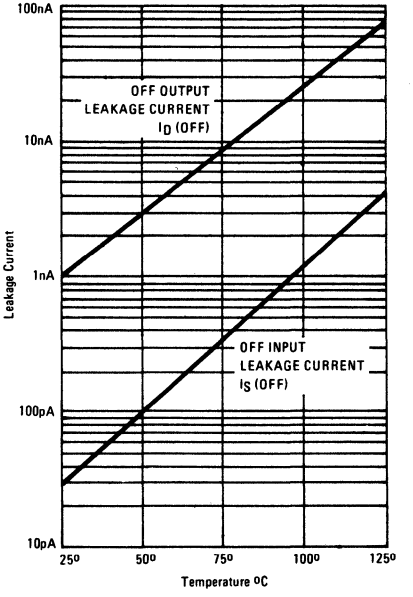


ON RESISTANCE vs. INPUT SIGNAL LEVEL

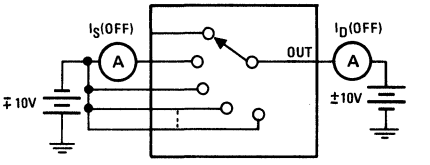
$R_{ON} = \frac{V_2}{1mA}$



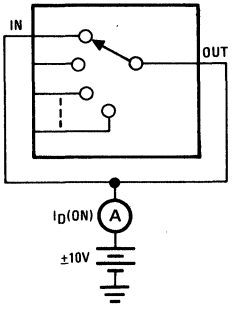
LEAKAGE CURRENT VS. TEMPERATURE



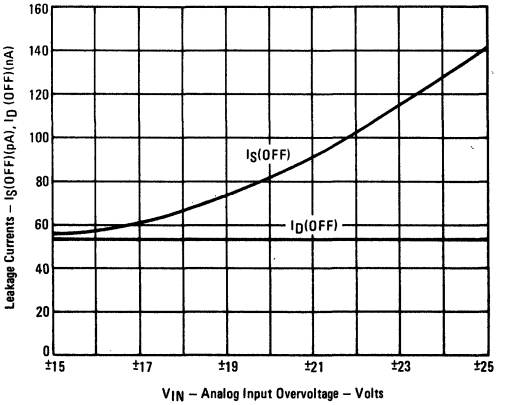
OFF LEAKAGE CURRENT vs. TEMPERATURE



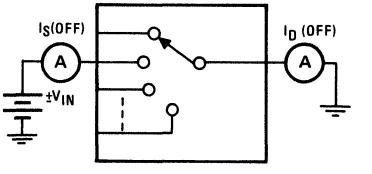
ON LEAKAGE CURRENT vs. TEMPERATURE



ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

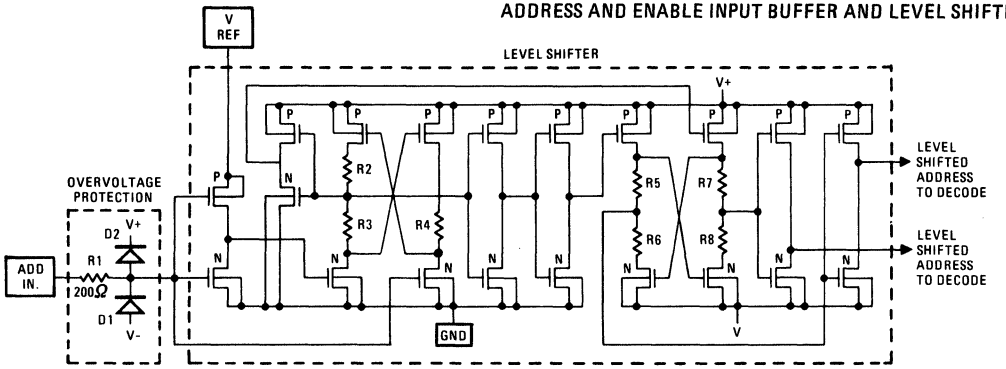


ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

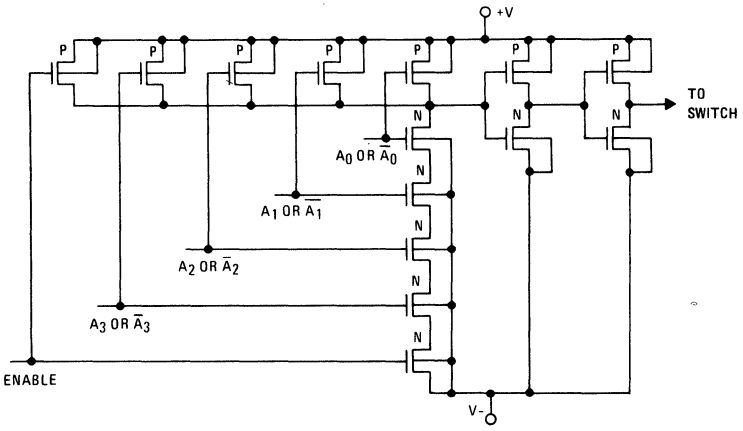


SCHEMATIC DIAGRAMS

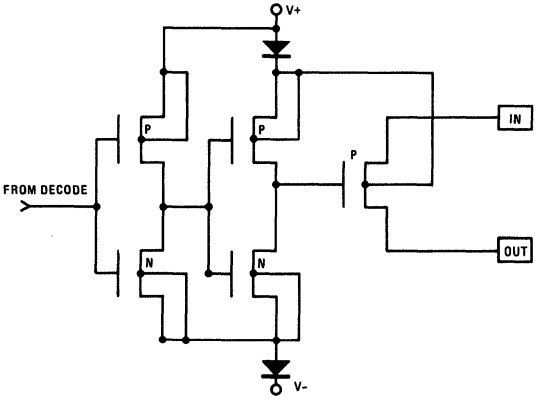
ADDRESS AND ENABLE INPUT BUFFER AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEX SWITCH



Data Conversion Products

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2420/2425

Fast Sample and Hold Gated Operational Amplifier

FEATURES

- SAMPLE CURRENT/HOLD RATIO 10^6
- ACQUISITION TIME (0.01%) 5μs
- SLEW RATE 5V/μs
- BANDWIDTH 2MHz
- APERTURE DELAY 50ns
- LOW CHARGE TRANSFER 10pC
- DTL/TTL COMPATIBLE CONTROL INPUT

APPLICATIONS

- A TO D INPUT (TO 13 BITS)
- D TO A DEGLITCHER
- AUTO ZERO SYSTEMS
- PEAK DETECTOR
- GATED OP AMP

DESCRIPTION

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier.

With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

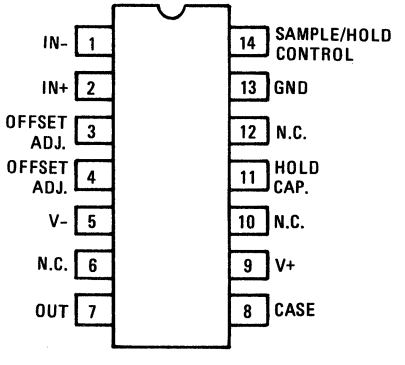
Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

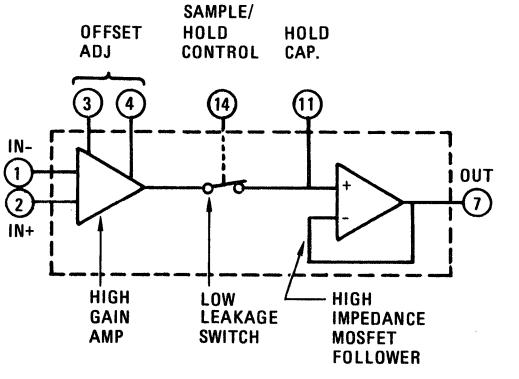
PINOUT

Package Code 4U

Top View



FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures specified on pg. 1-4.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Internal Power Dissipation	300mW (Note 7)
Differential Input Voltage	±30V	Operating Temperature Range	
Digital Input Voltage (Pin 14)	+8V, -15V	HA-2420	$-55^{o}C \leq T_A \leq +125^{o}C$
Output Current	Short Circuit Protected	HA-2425	$0^{o}C \leq T_A \leq +75^{o}C$
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions $V_{Supply} = \pm 15.0V$, $C_H = 1000pF$ Unless Otherwise Specified. Digital Input (Pin 14) $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold)

		HA-2420			HA-2425			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2	4		3	6	mV
	Full		3	6		4	8	mV
*Bias Current	+25°C		50	200		50	200	nA
	Full			400			400	nA
* Offset Current	+25°C		10	50		10	50	nA
	Full			100			100	nA
Input Resistance	+25°C	5	10		5	10		MΩ
Common Mode Range	Full	±10			±10			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 1, 4)	Full	25K	50K		25K	50K		V/V
*Common Mode Rejection (Note 2)	Full	80	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 1)	Full	±10			±10			V
Output Current	+25°C	±10			±10			mA
Full Power Bandwidth (Note 3, 4)	+25°C		70			70		kHz
Output Resistance	+25°C		5			5		Ω
TRANSIENT RESPONSE								
Rise Time (Note 3, 5)	+25°C		100			100		ns
Overshoot (Note 3, 5)	+25°C		20			20		%
Slew Rate (Note 3, 6)	+25°C		5			5		V/µs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current (V_{IN} = 0V)	Full			0.8			0.8	mA
Digital Input Current (V_{IN} = +5.0V)	Full			20			20	µA
Digital Input Voltage (Low)	Full			0.8			0.8	V
Digital Input Voltage (High)	Full	2.0			2.0			V
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time to .1% 10V Step (3)	+25°C		4			4		µs
Acquisition Time to .01% 10V Step (3)	+25°C		5			5		µs
Aperture Delay	+25°C		50			50		ns
Aperture Uncertainty	+25°C		5			5		ns
* Drift Current	+25°C		5			5		pA
	Full		0.5	10		.05	1.0	nA
* Charge Transfer	+25°C		10	20		10	20	pC
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		2.5	5.0		2.5	5.0	mA
* Power Supply Rejection Ratio	Full	80	90		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10VDC$
3. $A_V = +1$, $R_L = 2K\Omega$, $C_L = 50pF$
4. $V_{OUT} = 20V$ peak-to-peak
5. $V_{OUT} = 400mV$ peak-to-peak
6. $V_{OUT} = 10.0V$ peak-to-peak
7. Derate Power Dissipation by 4.3mW/°C above +105°C Ambient Temperature.

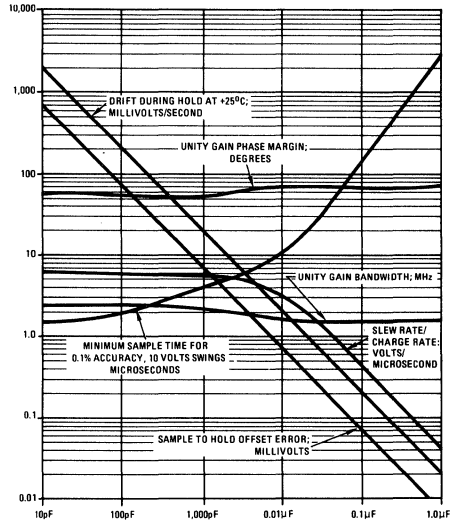
*100% Tested For DASH 8

4

PERFORMANCE CURVES

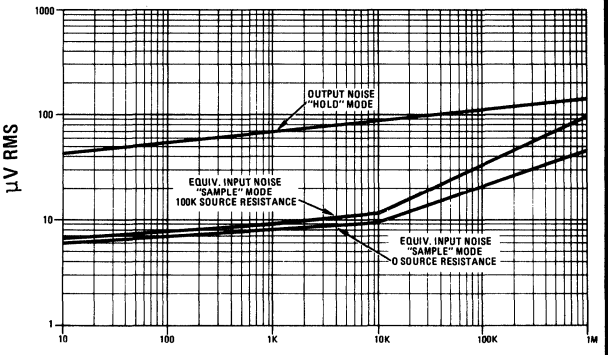
V_{SUPPLY} = ±15VDC, T_A = +25°C, C_H = 1,000pF UNLESS OTHERWISE SPECIFIED

TYPICAL SAMPLE-AND-HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITANCE



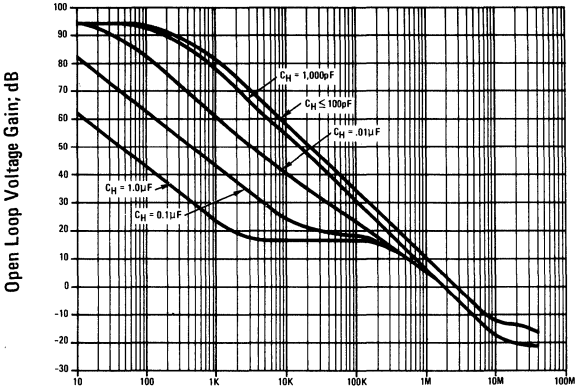
C_H Value

BROADBAND NOISE CHARACTERISTICS



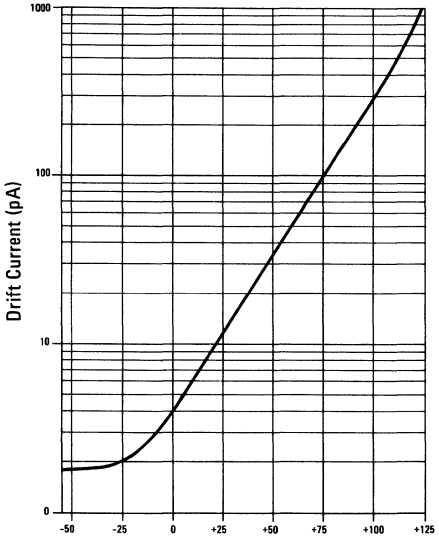
Bandwidth
(Lower 3db Frequency = 10Hz)

OPEN LOOP FREQUENCY RESPONSE



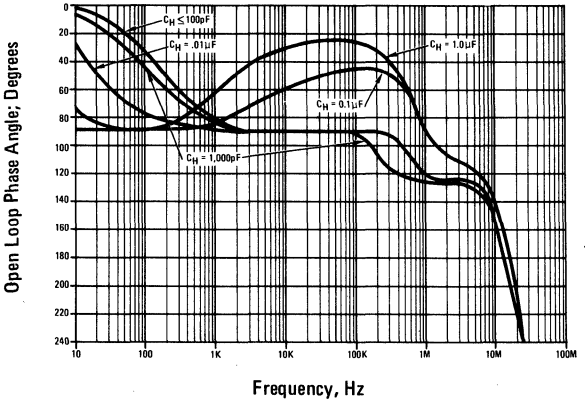
Frequency, Hz

DRIFT CURRENT vs TEMPERATURE



Temperature, (Degrees C)

OPEN LOOP PHASE RESPONSE



Frequency, Hz

4

APPLICATIONS

BASIC
SAMPLE-AND-HOLD

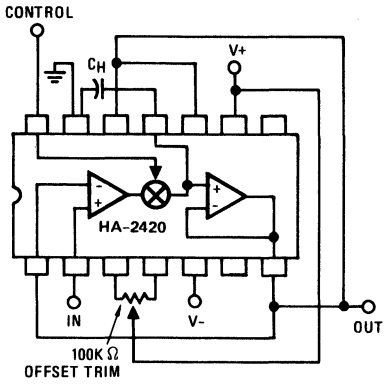


Figure 1

GUARD RING LAYOUT
(BOTTOM VIEW)

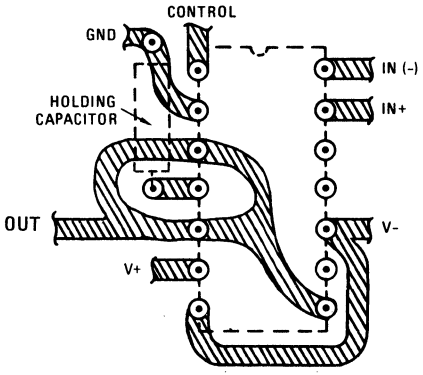


Figure 2

NOTES: 1) Figure 1 shows a typical unity gain circuit, with offset zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420/2425. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.

2) The method used to reduce leakage paths on the P.C. board and the device package is shown in Figure 2. This guard ring is recommended to minimize the drift during hold characteristic.

3) The holding capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), Teflon, or Parlene types are recommended.

For more applications, consult Harris Application Note 517.

GLOSSARY OF TERMS

ACQUISITION TIME:

The time required by the device after the "sample" command to reach its final value within +0.1% or ±0.01%. This time includes switch delay time, slewing time and settling time. This is the minimum sample time required to obtain a given accuracy.

CHARGE TRANSFER:

The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the Hold mode. Sample-to-Hold offset error is directly proportional to this charge, where:

$$\text{Offset Error (V)} = \frac{\text{Charge (pC)}}{C_H\text{(pF)}}$$

APERTURE DELAY:

The time required after the "hold" command until the switch is fully open. This delays the effective sample timing with rapidly changing input signals.

DRIFT CURRENT:

Leakage currents from the holding capacitor during the Hold mode which cause the output voltage to drift. Drift rate (droop rate) can be calculated from drift current values using the formula:

$$\frac{\Delta V}{\Delta T}\text{(Volts/Sec)} = \frac{I\text{(pA)}}{C_H\text{(pF)}}$$

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

PRELIMINARY HI-562

12 Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING — 200ns TO 0.01% (TYP.)
- LOW GAIN DRIFT — ±2ppm/°C (MAX.)
- EXCELLENT LINEARITY OVER TEMPERATURE — ±1/2 LSB (MAX.)
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH-REL APPLICATIONS
- PRECISION INSTRUMENTS

DESCRIPTION

The Harris HI-562 is the first monolithic digital-to-analog converter to combine both ultra-high speed performance and true 12-bit accuracy on the same chip. The HI-562's fast output current settling of 200ns to 0.01% is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-562 by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-ON and turn-OFF switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also completely eliminates thermal transients during switching. High stability thin film resistor processing together with laser trimming provide the HI-562 with guaranteed true 12-bit linearity to within ±1/2 LSB maximum over the -55°C to +125°C temperature range. Beyond that, the HI-562's low offset and gain drift over this temperature range assure that its absolute accuracy when referred to a fixed 10V reference will not deviate more than ±3/2 LSB for unipolar mode operation (±2 LSB for bipolar operation). The input reference can be varied from +2V to +10V for two quadrant multiplying mode operation.

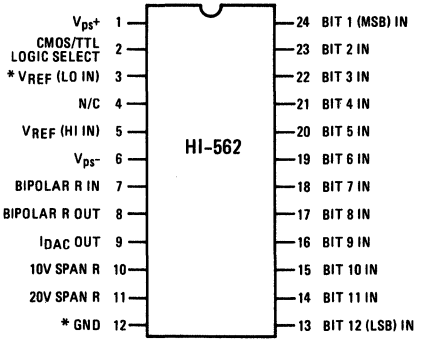
The HI-562 is recommended as a replacement for higher cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 5MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-562 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-562-5 is specified for operation over 0°C to +70°C, the HI-562-4 over -25°C to +85°C and the HI-562-2 and HI-562-8 over -55°C to +125°C. Processing to MIL-STD-883A Class B screening is available by selecting the HI-562-8. All are available in a hermetically sealed 24-lead dual-in-line package.

PINOUT

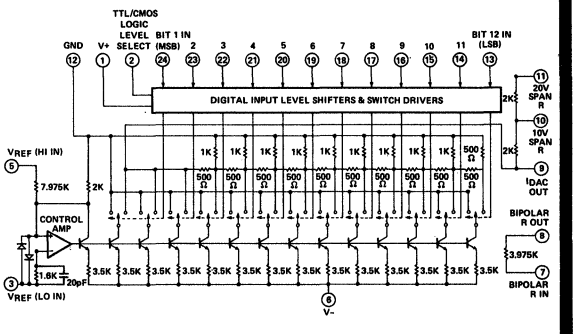
Package Code 1H

TOP VIEW



* Pins 3 and 12 connected to top and bottom case for high frequency shielding.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{PS}+$	+20V
	$V_{PS}-$	-20V
Reference Inputs	V_{REF} (Hi)	$\pm V_{PS}$
	V_{REF} (Lo)	0V
Digital Inputs	Bits 1-12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	$\pm V_{PS}$
	Pin 9	$+V_{PS}$, -5V

Power Dissipation Pd, Package	1000mW
Operating Temperature Range	
HI-562-2	-55°C to +125°C
HI-562-4	-25°C to +85°C
HI-562-5	0°C to +70°C
HI-562-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{PS}+$, = +5V, $V_{PS}-$ = -15V, V_{REF} = +10V, pin 2 open circuit unless otherwise noted)

PARAMETER	CONDITIONS	HI-562-2/HI-562-8 MIN	HI-562-2/HI-562-8 TYP	HI-562-2/HI-562-8 MAX	HI-562-4/HI-562-5 MIN	HI-562-4/HI-562-5 TYP	HI-562-4/HI-562-5 MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (3)	Bit ON "Logic 1" Bit OFF "Logic 0"							
TTL Input Voltage (2) Logic "1"	Over full temp. range	2.0			2.0			V
TTL Logic "0"				0.8			0.8	V
TTL Input Current (2) Logic "1"			20	100		20	100	nA
TTL Logic "0"			-50	-100		-50	-100	µA
CMOS Input Voltage Logic "1"	Pin 1 tied to pin 2, $+4.75V \leq V_{PS}+ \leq +12V$ over full temp. range	$0.7V_{PS}+$			$0.7V_{PS}+$			V
CMOS Logic "0"				$0.3V_{PS}+$			$0.3V_{PS}+$	V
CMOS Input Current Logic "1"			20	100		20	100	nA
CMOS Logic "0"			-50	-100		-50	-100	µA
Reference Input Input Resistance	I_{OUT} = 5mA (±20%)		8K			8K		Ω
Input Voltage			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Over full temp. range			12			12	Bits
Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range			±1/2			±1	
Differential Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range			MONOTONICITY GUARANTEED				
Relative Accuracy (6)	With 24.9Ω(1%) Trim Resistors							
Gain Error	All Bits ON			±0.024			±0.024	% FSR (4)
Bipolar Offset Error	All Bits OFF			±0.024			±0.024	
Unipolar Offset Error				±0.012			±0.012	
Adjustment Range	See Operating Instructions							
Gain	With 50Ω Trim		±0.3			±0.3		% FSR
Bipolar Offset	Potentiometers		±0.6			±0.6		
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (3)	Over full temp. range			±2			±3	ppm of FSR/°C
Offset Drift (3) Unipolar Offset	All Bits OFF			±0.4			±1	
Bipolar Offset				±1			±3	
Differential Nonlinearity	Over full temp. range		±1	±2		±2	±3	
Settling Time (3) to ±1/2 LSB	All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns

PARAMETER	CONDITIONS	HI-562-2/HI-562-8 MIN	HI-562-2/HI-562-8 TYP	HI-562-2/HI-562-8 MAX	HI-562-4/HI-562-5 MIN	HI-562-4/HI-562-5 TYP	HI-562-4/HI-562-5 MAX	UNITS
Major Carry Transient								
Peak Amplitude	From 011...1 to 100...0 or 100...0 to 011...1		0.7			0.7		mA
Settling Time to 90% Complete			35			35		ns
Power Supply Sensitivity (3)								
Unipolar Offset	All Bits OFF							
V_{ps}+ @ +5V or +15V			±0.5			±0.5		
V_{ps}- @ -15V			±0.5			±0.5		
Bipolar Offset	All Bits OFF, Bipolar mode							ppm of FSR/% V_{ps}
V_{ps}+ @ 5V or +15V			±1.5			±1.5		
V_{ps}- @ -15V			±1.5			±1.5		
Gain	All Bits ON							
V_{ps}+ @ +5V or +15V				±1			±1	
V_{ps}- @ -15V				±2			±2	

OUTPUT CHARACTERISTICS

Output Current								
Unipolar			-5.0			-5.0		mA
Bipolar			±2.5			±2.5		
Resistance			1000			1000		ohms
Capacitance			20			20		pF
Output Voltage Ranges								
Unipolar	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections		0 to +5 0 to +10			0 to +5 0 to +10		V
Bipolar			±2.5 ±5 ±10			±2.5 ±5 ±10		
Compliance Limit (3)		-3		+10	-3		+10	V
Compliance Voltage (3)	Over full temp. range		±1.0			±1.0		V
Output Noise	0.1 to 10Hz (All Bits ON) 0.1 to 5MHz (All Bits ON)		30 100			30 100		µV (p-p)

MULTIPLYING MODE PERFORMANCE

Quadrants	Bipolar Mode Reference Input; 2V to +10V		2			2		
Reference Voltage Feedthrough	Unipolar mode, all Bits OFF and +2V to +10V (p-p), 2kHz Sinewave		1			1		LSB (p-p)
Relative Accuracy	Reference Input @ $2V_{DC}$		±0.05			±0.05		% FSR
Output Slew Rate	All Bits ON and +2 to +10V Step change at reference input.		6			6		mA/µs
Settling Time to ±1/2 LSB			3			3		µs
Control Amplifier Bandwidth	Small signal		10			10		MHz

POWER REQUIREMENTS

V_{ps}+ (7)	Over full temp. range	4.5	5	15	4.75	5	15	V
V_{ps}-		13.5	15	16.5	13.5	15	16.5	
I_{ps}+ (5)	All Bits ON or OFF in either TTL or CMOS mode		9			9		mA
I_{ps}- (5)			28			28		
I_{ps}+ (5)	Same as above except over full temp. range		11			11		mA
I_{ps}- (5)			33			33		

NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

2. V_{ps}+ tolerance is ±10% for HI-562-2, -8. and ±5% for HI-562-4, -5.

3. See Definitions.

4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.; or 5mA(±20%) for current output.

5. After 30 seconds warm-up.

6. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Operating Instructions Figure 2.)

7. Maximum V_{ps}+ is +12V for high level logic only, i.e. when pin 1 is tied to pin 2.

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-562 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement, or Offset Binary, (See Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	½FS – 1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonictiy; i.e., the output always increases and never decreases for an increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches to zero output. Matched switching times and fast switching will reduce glitches considerably.

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-562 (preferrably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

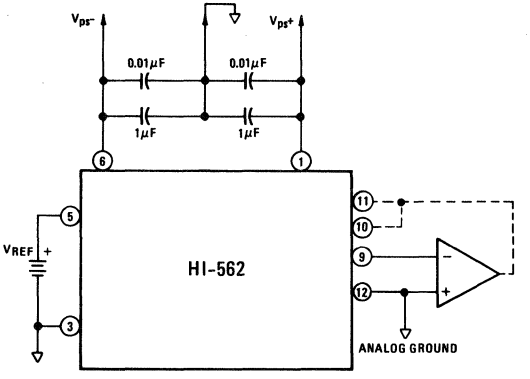
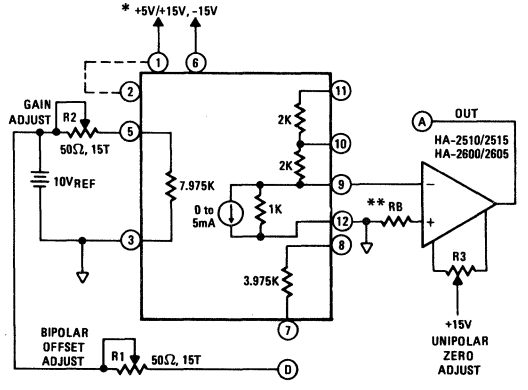


Figure 1

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

CONNECTIONS – Using an external resistive load, the output compliance should not exceed ±1V to maintain specified accuracy. For higher output voltages, accuracy can be maintained by using an external op amp and the internal span resistors as shown in Figure 2 and defined in Table 1 for unipolar and bipolar modes.



* For TTL and DTL compatibility, connect +5V to pin 1 and leave pin 2 open. For CMOS compatibility, connect digital power supply (+4.85V ≤ VDD ≤ +12V) to pin 1 and short pin 2 to pin 1.

** Bias resistor, RB, should be chosen to equalize op amp offset voltage due to bias current. Its value is calculated from the parallel combination of the current source output resistance (1K) and the op amp feedback resistor. See Table 1 for values of RB.

Figure 2

Table 1

	OUTPUT RANGE	CONNECTIONS Pin 7 to	Pin 8 to	Pin 10 to	Pin 11 to	BIAS (R_B) RESISTOR
Unipolar Mode	0 to +10V	N.C.	N.C.	A	N.C.	667Ω
	0 to +5V	N.C.	N.C.	A	9	500Ω
Bipolar Mode	±10V	D	9	N.C.	A	667Ω
	±5V	D	9	A	N.C.	580Ω
	±2.5V	D	9	A	9	444Ω

EXTERNAL GAIN AND ZERO CALIBRATION (See Figure 2)

The input reference resistor (7.975K) and bipolar offset resistors shown in Figure 2 are both intentionally set low by 25Ω to allow the user to externally trim-out initial errors to a very high degree of precision. The adjustments are made in the voltage output mode using an external op amp as current-to-voltage converter and the HI-562 internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. For best accuracy over temperature, select an op amp that has good front-end temperature coefficients such as the HA-2600/2605 with offset voltage and offset current tempco's of 5μV/°C and 1nA/°C, respectively. For high speed voltage mode applications where fast settling is required, the HA-2510/2515 is recommended for better than 1.5μs settling to 0.01%. Using either one, potentiometer R_3 conveniently nulls unipolar offset plus op amp offset in one operation (for HA-2510/2515 and HA-2600/2605 use R_3 = 20K and 100K, respectively). For bipolar mode operation, R_3 should be used to null op amp offset to optimize its tempco (i.e., short 9 to A and adjust R_3 for zero before calibrating in bipolar mode). The gain and bipolar offset adjustment range using 50Ω potentiometers is ±12 LSB and ±25 LSB respectively. If desired, the potentiometers can be replaced with fixed 24.9 Ω (1%) resistors resulting in an initial gain and bipolar offset accuracy of typically ±1/2 LSB.

UNIPOLAR CALIBRATION

Step 1: Unipolar Offset
- Turn all bits OFF
- Adjust R3 for zero volts output

Step 2: Gain
- Turn all bits ON
- Adjust R2 for an output of FS -1 LSB
  That is, adjust for:
  9.9976V for 0V to +10V range
  4.9988V for 0V to +5V range

BIPOLAR CALIBRATION

Step 1: Bipolar Offset
- Turn all bits OFF
- Adjust R1 for an output of:
  -10V for ±10V range
  -5V for ±5V range
  -2.5V for ±2.5V range

Step 2: Gain
- Turn bit 1 (MSB) ON; all other bits OFF
- Adjust R2 for zero volts output

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HI-1080/1085

Precision Monolithic 8-Bit D to A Converter

FEATURES

- GUARANTEED ±1 L.S.B. ACCURACY OVER TEMPERATURE
  - HI-1080 -55°C to +125°C
  - HI-1085 0°C to +75°C
- FAST SETTLING 1.5 μs to ½ L.S.B.
- EXPANDABLE FOR HIGHER RESOLUTIONS
- MONOLITHIC CONSTRUCTION
- DTL/TTL COMPATIBLE INPUTS
- RELIABLE MONOLITHIC CONSTRUCTION MEETS REQUIREMENTS OF MIL-STD-883

APPLICATIONS

- WAVEFORM SYNTHESIZERS
- MICROPROCESSOR I/O INTERFACE
- HIGH REL APPLICATIONS
- A TO D CONVERTER (USING COMPARATOR AND DIGITAL LOGIC)
- DATA ACQUISITION SYSTEMS

DESCRIPTION

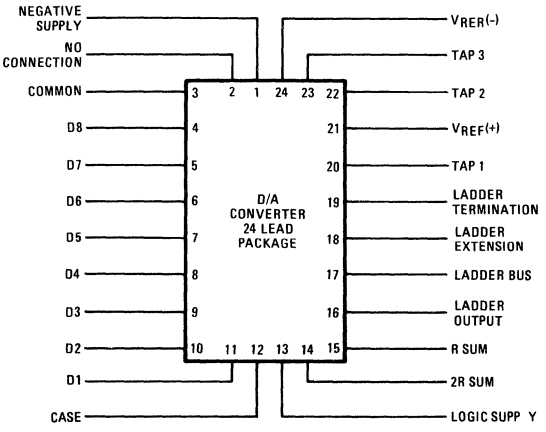
The HI-1080/1085 is a monolithic 8 bit digital-to-analog converter employing bipolar current switches feeding a thin film R-2R ladder network.

Because of the excellent stability of this device, it is practical to specify one all-inclusive accuracy parameter: ±1L.S.B. accuracy over the operating temperature range. This means that once the desired full scale output level is set at room temperature by adjustment of the input reference current, each of the 256 output levels will always measure within ±1 L.S.B. of the corresponding output of a "perfect" DAC. Thus the accuracy specification includes the worst case effects of all of the normally published errors such as non-linearity, zero drift, full scale drift, etc.

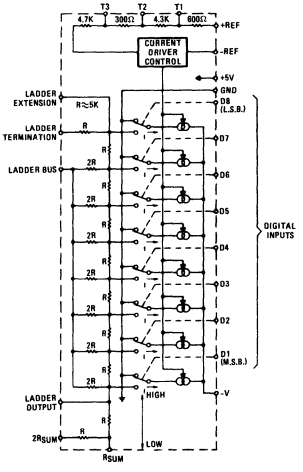
The device is exceptionally versatile, since it may be used in a voltage or current output mode, and may be offset to produce bipolar operation. Matched auxillary resistors are provided for amplifier feedback or current summing. Provisions are also made for scale factor adjustment and for cascading of additional D/A converters for extended resolution.

PINOUT

Top View — Package Code 4K



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Maximum Ratings are limiting values above which permanent circuit damage may occur.

Voltage
- V+ +8.0V
- V- -18.0V

Digital Inputs: +5.5V

Ladder Common: +8.0V

I_{REF}: 1.6mA

Storage Temperature: $-65^{o}C \leq TA \leq +150^{o}C$

Power Dissipation: 450mW *

*Derate at 4mW/°C above 85°C ambient.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated all measurements taken at V+ = +5V, V- = -15V
V_{REF} = +5V, V_{in}High = +2.4V, V_{in}Low = +0.4V
Unipolar, zero reference connection (Figure 3)

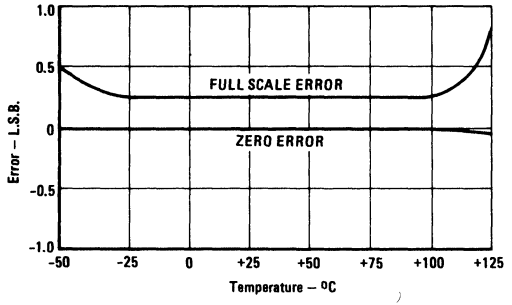
	TEMP	HI-1080 MIN	HI-1080 TYP	HI-1080 MAX	TEMP	HI-1085 MIN	HI-1085 TYP	HI-1085 MAX	UNITS
Resolution		8				8			Bits
Accuracy	+25°C		1/4	1/2					
(Calibrated at 25°C) (Note 1)	-55°C to +125°C		1/2	1	0°C to +75°C		1/2	1	L.S.B.
$V_{Full\ Scale}$ (Note 2) (Uncalibrated)	+25°C	-4.5	-4.98	-5.5	+25°C	-4.5	-4.98	-5.5	Volts
Power Supply Rejection (Note 3)	-55°C to +125°C	.05	.001		0°C to +75°C	.05	.001		L.S.B. per Volt
Settling Time (Note 4)	+25°C		1.5	3.0	+25°C		1.5		μs
Digital Inputs:									
High Threshold				2.0				2.0	Volts
Low Threshold (Note 5)		0.8				0.8			Volts
I_{in}High			.01	1	0°C to +75°C		.01	1	mA
I_{in} Low (Note 6)	-55°C to +125°C		-0.7	-1.0			-0.7	-1.0	mA
Supply Current:									
I+	-55°C		8	10	0°C		8	10	mA
I-	to		8	10	to		8	10	mA
I_{REF} (Note 7)	+125°C		0.5	0.6	+75°C		0.5	0.6	mA

NOTES: Test Conditions -

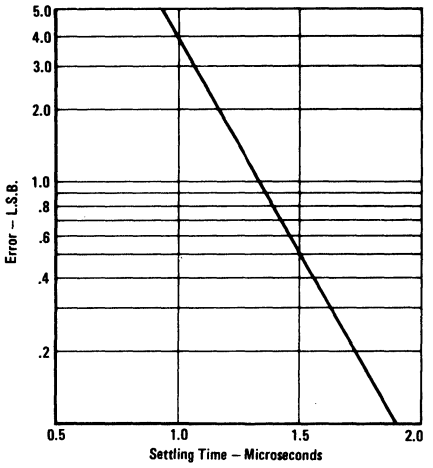
1. Any Input Combination
2. Inputs all low
3. $\Delta V_{OUT}/\Delta V_{SUPPLY}$
   V+ = +5 ± 0.5V
   V- = -15 ± 3V
4. To ±0.2% of full scale after full scale input step
   $R_L > 10M$
   $C_L < 5pF$
5. V+ = 4.5V
6. V_{in} = 2.4 Volts
   V+ = 5.5V
   V_{in} = 0.4 Volts
   V+ = 5.5V
7. V+ = +5.0V
   V- = -15.0V
   V_{REF} = +5.0V
   Inputs all low

PERFORMANCE CURVES

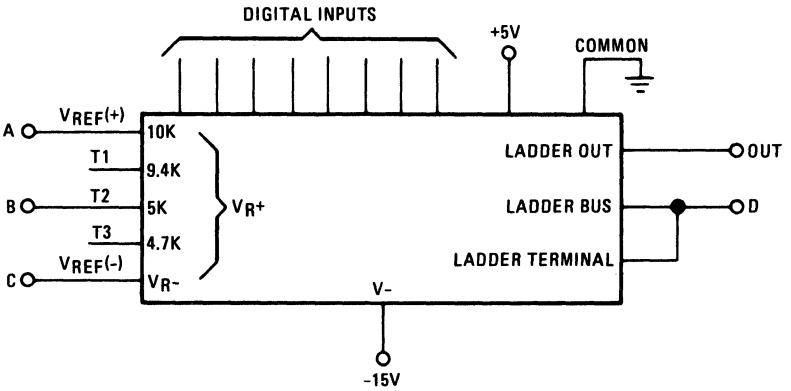
TYPICAL OUTPUT ACCURACY vs. TEMPERATURE



TYPICAL SETTLING TIME



D/A CONVERTER OPERATION MODES



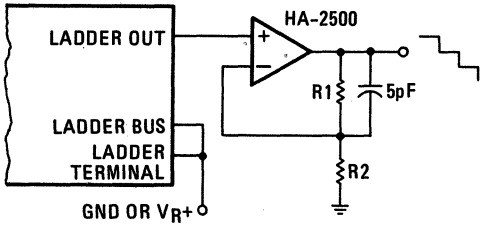
MODE	OUTPUT RANGE INPUTS: ALL HIGH TO ALLLOW	CONNECTIONS			
		A*	B*	C	D
UNIPOLAR ZERO REFERENCE	0 TO -V_{R+} -1L.S.B.	V_{R+}	N.C.	GND	GND
UNIPOLAR ZERO F.S.	+/V_{R+}/TO 0 +1L.S.B.	V_{R+}	N.C.	GND	V_R
BIPOLAR	/V_{R+}/TO -V_R +1L.S.B.	N.C.	V_{R+}	GND	V_{R+}

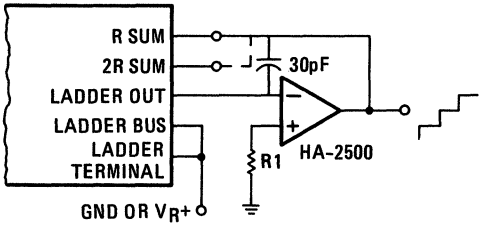
OPERATING MODES

*Tap 1 or Tap 3 with selected external series resistors may be substituted for points A or B, respectively, for fine adjustment of output range.

TYPICAL APPLICATIONS

BUFFER AMPLIFIER CONNECTION





NON-INVERTING OUTPUT

(MORE NEGATIVE WITH INCREASING COMPLEMENT OF INPUT NUMBER)

OUTPUT RANGE: SAME AS SHOWN ON 'OPERATING MODE' CHART

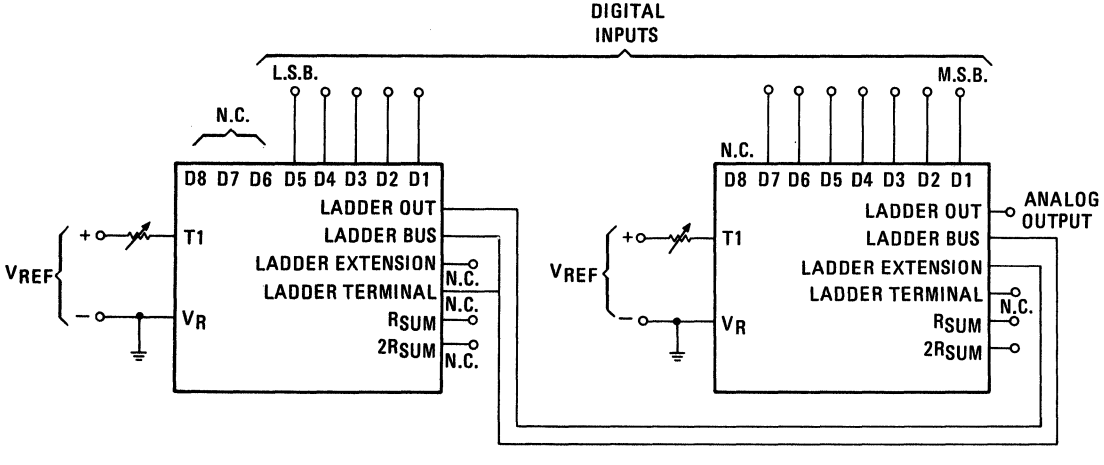
MULTIPLIED BY $1+\frac{R1}{R2}$

INVERTING OUTPUT

(MORE POSITIVE WITH INCREASING COMPLEMENT OF INPUT NUMBER)

FULL SCALE OUTPUT	OUTPUT FEEDBACK CONNECTED TO	R1
+4.98V	SUM	2.5K
+9.96V	$2R_{SUM}$	3.3K

CASCADED UNITS FOR 12 BIT RESOLUTION



HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HA-2820/2825

Phase Locked Loop

FEATURES

- FREQUENCY RANGE 0.01Hz tTO 3MHz
- INDEPENDENT PHASE DETECTOR AND OSCILLATOR FOR VERSATILITY
- TWO ISOLATED PHASE DETECTOR OUTPUTS
- DTL/TTL COMPATIBLE OSCILLATOR OUTPUT

APPLICATIONS

- DISCRIMINATORS
- RECEIVERS
- DATA DECODERS (DATA MODEMS)
- DATA SYNCHRONIZERS

DESCRIPTION

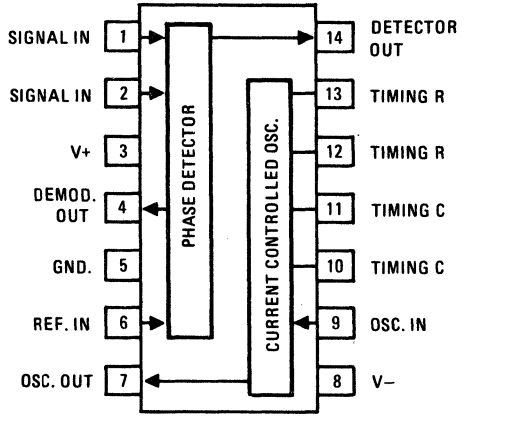
The HA-2820/2825 Phase Locked Loop is useful for many operations in the frequency domain in the sub-audio to low R. F. bands. It features a number of functional and parametric improvements over other similar monolithic circuits.

A major feature is a high impedance current source phase detector output with provisions for external connection to the oscillator input which is a low impedance current sink. This allows connection of complex passive or active filters, amplifiers, sweep circuits, etc. within the loop. Also, the two phase detector outputs are isolated from one another so that different filter functions can be connected at the two outputs without interaction. The capability of independently adjusting loop bandwidth allows phase modulation detectors to be constructed.

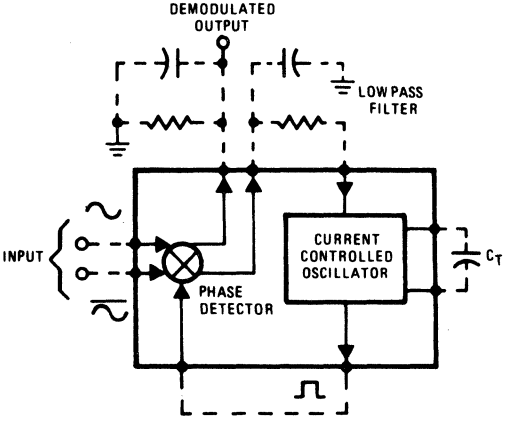
Applications include modulators and demodulators for F.M., phase modulation, and F.S.K.. frequency multiplication; data synchronization. tracking filters. and speed controls.

PINOUT

Top View — Package Code 4U



FUNCTIONAL DIAGRAM



5

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	27.0V	Power Dissipation	300mW (Note 3)
Input Voltage	2 VRMS	Operating Temperature	
		HA-2820	$-55^{o}C > T_A > +125^{o}C$
		HA-2825	$0^{o}C > T_A > +75^{o}C$
Output Current, Pin 7	10mA	Storage Temperature	$-65^{o}C > T_A > +150^{o}C$

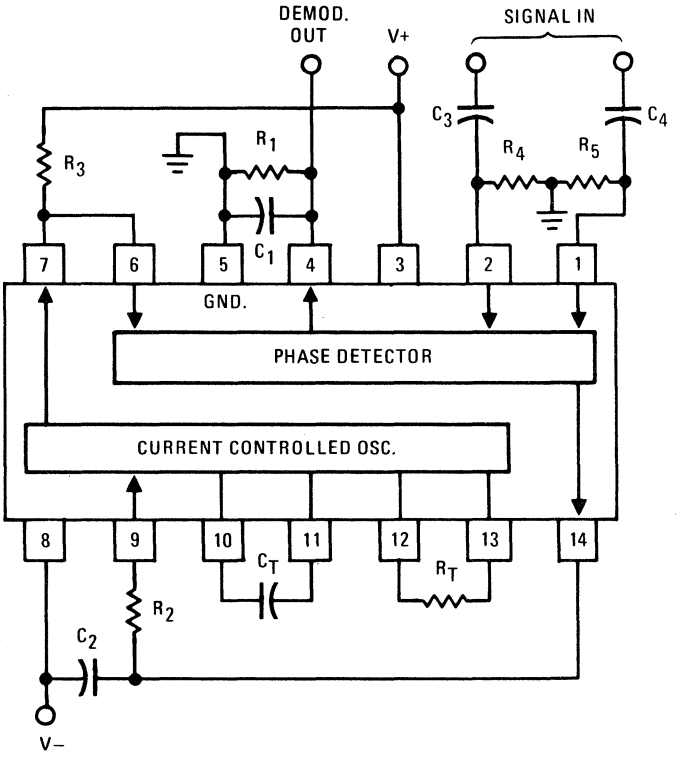
ELECTRICAL CHARACTERISTICS

V+ = +6.0V, V- = -6.0V, Pin 5 = Ground; V_{IN} = 100mV RMS, $F_O \approx$ 50kHz, See Test Circuit, Page 3. Unless otherwise specified

PARAMETER	TEMP.	HA-2820 -55°C to +125°C LIMITS MIN.	HA-2820 TYP.	HA-2820 MAX.	HA-2825 0°C to +75°C LIMITS MIN.	HA-2825 TYP.	HA-2825 MAX.	UNITS
PHASE DETECTOR								
Input Impedance, Pins 1 - 2	+25°C		100K			100K		Ω
Input Voltage Range, Pins 1 - 2 (Note 1)	Full	10	5		10	5		mV RMS
Output Impedance, Pins 4 & 14	+25°C		10			10		MΩ
Output Offset Current, Pins 4 & 14	+25°C		10	15		10	15	μA
Output Offset Current, Pins 4 & 14	Full			20			20	μA
Conversion Gain, Pins 4 & 14	+25°C		50			50		μA/Radian
CURRENT CONTROLLED OSCILLATOR								
Maximum Frequency	Full	3	5		3	5		MHz
Frequency Drift	Full		200			200		ppm/°C
Frequency Change with Supply Voltage	Full		.01			.01		%/V
Input Resistance, Pin 9 (Note 4)	+25°C		500			500		Ω
Input Open Circuit Voltage, Pin 9	+25°C		-3.5			-3.5		V
Conversion Gain	+25°C		1.0			1.0		% Δf/μA
Output Voltage, High	+25°C	+1.9			+1.9			V
Output Voltage, Low	+25°C			+0.4			+0.4	V
Output Rise Time	+25°C		100			100		ns
Output Fall Time	+25°C		125			125		ns
CLOSED LOOP CHARACTERISTICS								
Loop Gain	+25°C		50			50		% Δf/Radian
Tracking Range	+25°C		50			50		%Δf
Demod. Output Swing, Pin 4 (Note 5)	+25°C		±700			±700		mV
Frequency Drift	Full		200			200		ppm/°C
POWER SUPPLY CHARACTERISTICS								
Supply Current, V+	Full		3	5		3	5	mA
Supply Current, V-	Full		7	10		7	10	mA
Supply Voltage Range (Notes 2, 3)	Full	±6		±12	±6		±12	V

NOTES
1. For ±10% Tracking range.
2. +5.0V,-7.0V may be used alternatively.
3. Derate power dissipation by 6.6mW/°C above +105°C ambient temperature.
4. $\Delta V_S = \pm 2V$
5. When not in use pin 4 should be grounded.

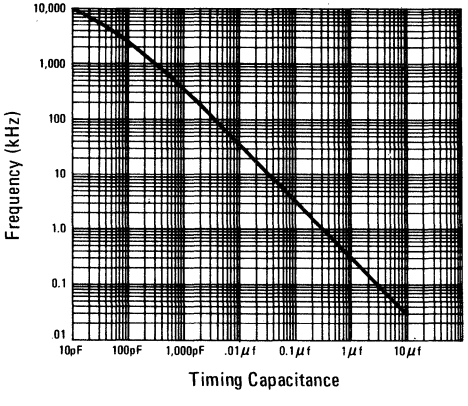
TEST CIRCUIT



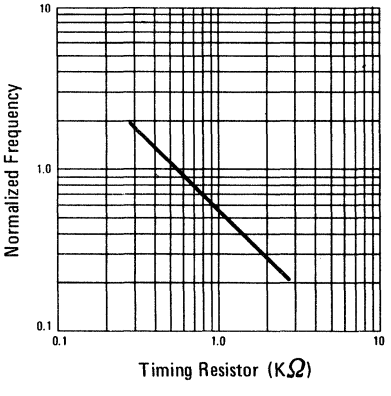
Unless otherwise specified: V+ = +6.0V; V– = -6.0V; $R_1 = R_3 = 10K\Omega$; $R_2 = 1K\Omega$; $R_4 = R_5 = 300\Omega$; $R_T = 540\Omega$; $C_1 = .015\mu f$; $C_2 = C_3 = C_4 = 0.1\mu f$; $C_T = 0.01\mu f$ ($f_o \approx 50kHz$); $V_{IN} = 100mV$ RMS; $T_A = +25^oC$

PERFORMANCE CURVES

CENTER FREQUENCY, f_o vs.
TIMING CAPACITOR, C_T ($R_T = 540\Omega$)

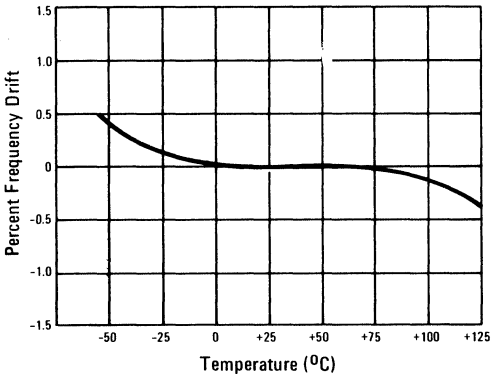


CENTER FREQUENCY, f_o vs.
TIMING RESISTOR, R_T ($C_T = .01\mu f$)

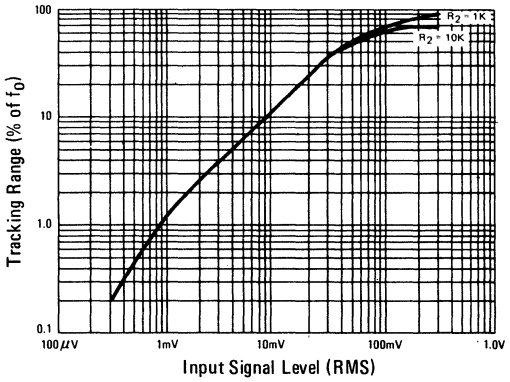


PERFORMANCE CURVES *(continued)*

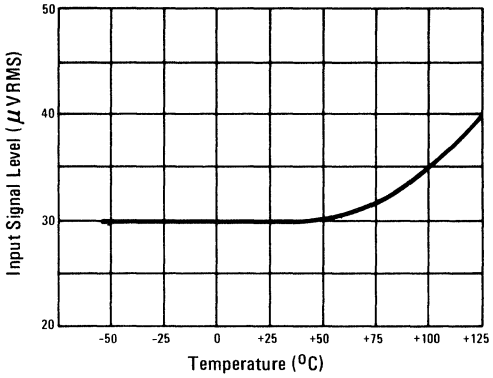
CENTER FREQUENCY DRIFT vs. TEMPERATURE



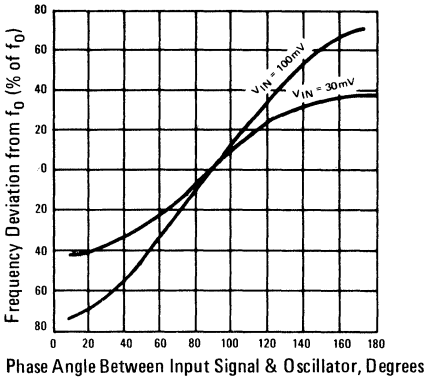
TRACKING RANGE vs. INPUT SIGNAL LEVEL



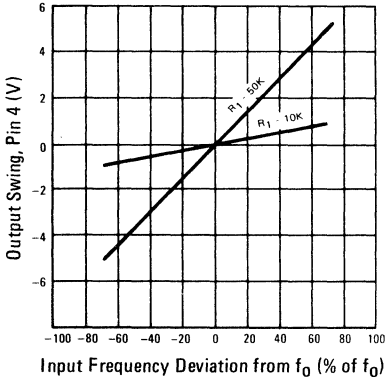
MINIMUM SIGNAL TO MAINTAIN LOCK



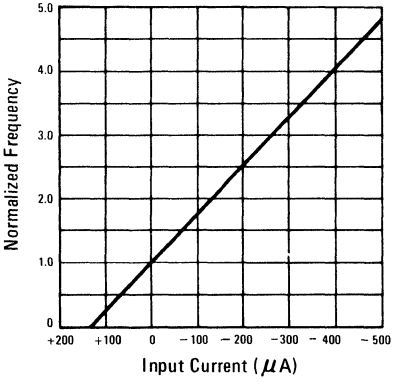
LOOP GAIN CHARACTERISTIC



DEMODULATED OUTPUT SWING



OSCILLATOR FREQUENCY vs. INPUT CURRENT, PIN 9 (f_0 = 50kHz)



5

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HC-55516/55532

All-Digital Continuously Variable Slope Delta Modulator (CVSD)

FEATURES

- REQUIRES FEWER EXTERNAL PARTS
- LOW POWER DRAIN: 6mW FROM SINGLE 5V-7V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- HALF DUPLEX OPERATION BY DIGITAL CONTROL
- FILTER RESET BY DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY
- AUTOMATIC "QUIET" PATTERN GENERATION
- AGC CONTROL SIGNAL AVAILABLE

APPLICATIONS

- VOICE TRANSMISSION OVER DATA CHANNELS
- VOICE ENCRYPTION/SCRAMBLING
- VOICE I/O FOR DIGITAL SYSTEMS
- AUDIO MANIPULATIONS: DELAY LINES, TIME COMPRESSION, ECHO GENERATION/ SURPRESSION, SPECIAL EFFECTS, ETC.

DESCRIPTION

The HC-55516 and HC-55532 are half duplex modulator/ demodulator CMOS integrated circuits used to convert voice signals into serial NRZ digital data, and to reconvert that data into voice. The conversion is by delta modulation, using the continuously variable slope (CVSD) method of companding.

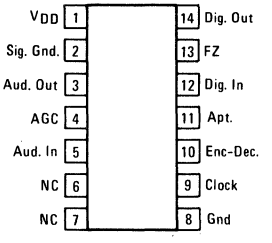
While signals are compatible with other CVSD circuits, internal design is unique. The analog loop filters have been replaced by digital filters, using very low power, and requiring no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The HC-55516 has internal time constants optimized for 16K bits/sec data rate and is usable down to 9K bits/sec. The HC-55532 is optimized for 32K bits/sec and is usable beyond 64K bits/sec. Both units are available in 14 pin D.I.P. (HC1) or flat packages (HC9) in two temperature ranges; -55°C to +125°C (-2 or -8) and -40°C to +85°C (-9).

PINOUT

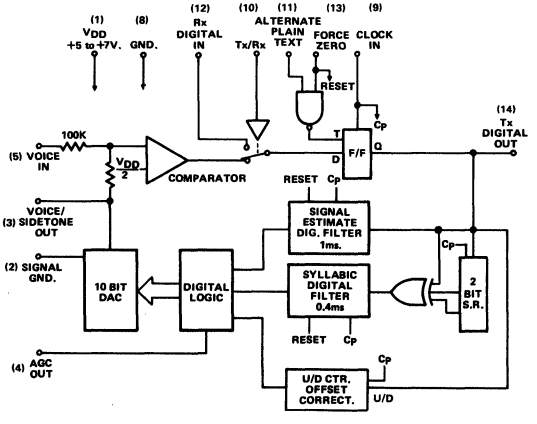
Package Code 9R, 4Q

Top View



14 PIN D.I.P. AND FLAT PACK

FUNCTIONAL DIAGRAM



5

PIN # 14-LEAD F.P. & D.I.P.	SYMBOL	ACTIVE* LEVEL	DESCRIPTION
1	V_{DD}		Positive supply voltage.
2	Sig. Gnd.		Ground connection to D/A ladders and comparator; i.e. audio ground.
3	Aud. Out		Recovered audio out. May be used as side tone at the transmitter. Presents approximately 100 kilohm source. Zero signal reference is $V_{DD}/2$.
4	AGC		A logic "Low" level will appear at this output when the recovered signal excursion reaches one-half of full scale value.
5	Aud. In		Audio input. Should be externally AC coupled. Presents approximately 100 kilohms in series with $V_{DD}/2$.
6,7			No internal connection is made to these pins.
8	Gnd.		Logic ground. Negative supply voltage.
9	Clock		Receiver clock must be phased with digital input such that a positive clock transition occurs near the middle of each received data bit.
10	Encode (Decode)	Low (High)	A single CVSD can provide half-duplex operation. The encode and decode functions are selected by the logic level applied to this input. A low level selects the encode mode, a high level, the decode mode.
11	APT.	Low	Activating this input causes an "alternate plain text" (quieting pattern) to be transmitted without affecting the internal operation of the CVSD.
12	Dig. In		Input for the received digital data.
13	FZ	Low	Activating this input forces the transmitted output, the internal logic, and the recovered audio output into the "quieting" condition.
14	Dig. Out		Output for transmitted digital data.

*Note: No active input should be left in a "floating condition".

ABSOLUTE MAXIMUM RATINGS

Voltage At Any Pin	-3.0V to V_{DD} +0.3V	Operating Temperature (-9)	-40°C to +85°C
Maximum V_{DD} Voltage	+7.0V	(-2)	-55°C to +125°C
Operating V_{DD} Range	+5.0V to +7.0V	(-8)	-55°C to +125°C
		Storage Temperature	-65°C to +150°C

ELECTRICAL CHARACTERISTICS @ T_A = 25°C

Test Conditions V_{DD} = 6.0V, Bit Rate = 16Kb/s, (HC-55516)
Bit Rate = 32Kb/s, (HC-55532)

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Bit Rate	0		64	Kb/s	(1)
Clock Duty Cycle	30		70	%	
Supply Voltage	+5.0		+7.0	V	
Supply Current		1.0		mA	
Digital "1" Input		4.5		V	(2)
Digital "0" Input		1.5		V	(2)
Digital "1" Output		5.5		V	(3)
Digital "0" Output		0.5		V	(3)
Audio Input Voltage		0.5	1.4	Vrms	(4)
Audio Output Voltage		0.5	1.4	Vrms	(5)
Audio Input Impedance		100		KΩ	(6)
Audio Output Impedance		100		KΩ	(7)
Transfer Gain	-0.5		+0.5	dB	(8)
Syllabic Time Constant		4.0		mS	(9)
L.P. Filter Time Constant (55516) (55532)		0.94 0.47		mS mS	(9)
Step Size Ratio (55516) (55532)		24 18		dB dB	(10)
Resolution (55516) (55532)		0.1 0.2		% %	(11)
Min. Step Size (55516) (55532)		0.2 0.4		% %	(12)
Slope Overload		Fig. 1			(13)
Signal/Noise Ratio			Tab. 1		(14)
Quieting Pattern Amplitude (55516) (55532)		12 24		mV P-P mV P-P	(15)
AGC Threshold		0.5		F.S.	(16)
Clamping Threshold		0.75		F.S.	(17)

1. There is one NRZ data bit per clock period. Clock must be phased with digital data such that a positive clock transition occurs in the middle of each received data bit; i.e., the transmitter and receiver clock are in phase.

2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.

3. Logic outputs are CMOS compatible at supply voltage and withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions.

4. Recommended voice input range for best voice performance.

5. May be used for side-tone in encode mode.

6. Should be externally AC coupled. Presents 100 Kilohms in series with $V_{DD}/2$.

7. Presents 100 Kilohms in series with recovered audio voltage. Zero-signal references is $V_{DD}/2$.

8. Unloaded, for linear signals.

9. Note that filter time constants are inversely proportional to clock rate.

10. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.

11. Minimum quantization voltage level expressed as a percentage of supply voltage.

12. The minimum step size between levels is twice the resolution.

13. For large signal amplitudes or high frequencies, the encoder may become slope-overloaded. Figure 1 shows the frequency response at various signal levels,measured with a 3kHz low-pass filter having a 130dB/octave roll-off to -50dB. See Table II.

14. Table I shows the SNR under various conditions, using the output filter described in 13 (above) at a bit rate of 16Kb/s. See Table II.

15. The "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.

16. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative).

17. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

TABLE I

INPUT FREQUENCY Hz	INPUT AMPLITUDE mV RMS	OUTPUT SNR dB MIN.
300	1400	20
300	45	15
1000	500	14
1000	16	9

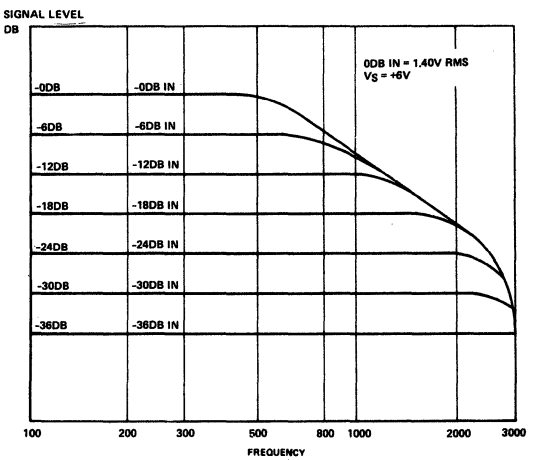


Figure 1 — Transfer Function for CVSD at 16KB

TABLE II

INPUT FILTER FREQUENCY RESPONSE		OUTPUT FILTER FREQUENCY RESPONSE	
FREQUENCY	RELATIVE OUTPUT	FREQUENCY	RELATIVE OUTPUT
100Hz	0±0.5dB	100Hz to 1500Hz	0±1.5dB
200Hz	0±0.1dB	1500Hz to 3000Hz	0±2.5dB
1000Hz	0±0.1dB	3800Hz to 100KHz	Less Than -45dB
3000Hz	-3±0.5dB		
9000Hz	-20±2.0dB		

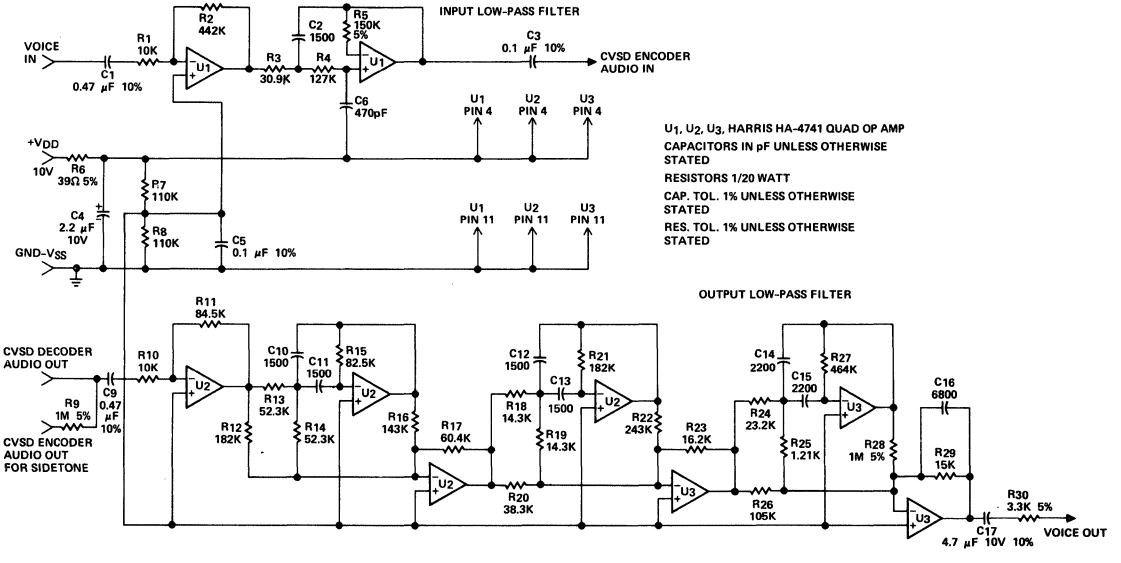


Figure 2 – Suggested Input/Output Audio Filters for SNR Measurement

NOTE: An output filter similar to the input filter section above will generally suffice for good voice intelligibility.

Interface Products

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-0165

Keyboard Encoder

FEATURES

- STROBE OUTPUT
- KEY ROLLOVER OUTPUT
- EXPANDABLE: 2 PACKAGES REQUIRED FOR FULL TELETYPEWRITER, EIGHT-BIT ENCODING
- SINGLE +5.0V SUPPLY REQUIRED
- DTL/TTL OUTPUTS
- MONOLITHIC RELIABILITY

APPLICATIONS

- MICROPROCESSOR DATA ENTRY (16 KEY TO HEX CODE)
- BCD DATA ENTRY
- TYPEWRITER TYPE KEYBOARDS
- CONTROL PANELS

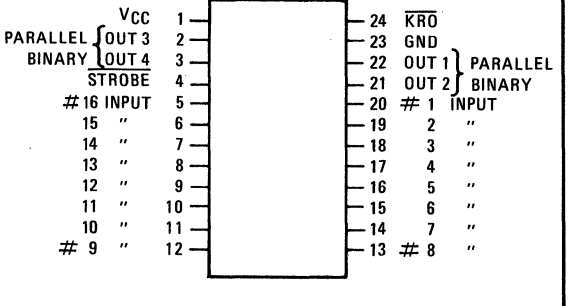
DESCRIPTION

The HD-0165 Keyboard Encoder is a 16 line to four-bit parallel encoder intended for use with manual data entry devices such as calculator or typewriter keyboards. In addition to the encoding function, there is a Strobe output and a Key Rollover output which energizes whenever two or more inputs are energized simultaneously. Any four-bit code can be implemented by proper wiring of the input lines. Inputs are normally wired through the key switches to the +5.0V power supply. Full typewriter keyboard encoding up to eight bits can be accomplished with two Encoder circuits by the use of double pole key switches or single pole switches with two isolation diodes per key. Outputs will interface with all popular DTL and TTL logic families. The circuit is packaged in a hermetic 24-pin dual-in-line package and operates over the temperature range of 0°C to +75°C.

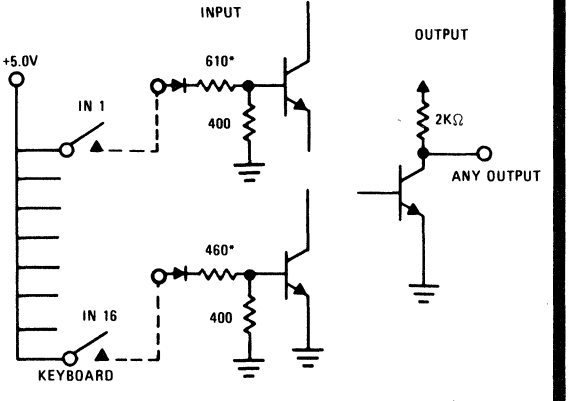
PINOUT

Package Code 4K

Top View



EQUIVALENT CIRCUITS



* EQUIVALENT RESISTORS FOR OTHER INPUTS ARE BETWEEN THESE TWO VALUES

6

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V	Output Current	30mA
Input Voltage	+5.5V	Storage Temperature	-65^{o} to $+150^{o}C$
Output Voltage	+5.5V	Operating Temperature (Case)	$0^{o}C$ to $+75^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = +5.0V \pm 5\%$
$T_{Case} = 0^{o}C$ to $+75^{o}C$
Unless otherwise specified

	PARAMETER	SYM.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
	Input Current "1"	I_{IH}			17	mA	$V_{IN} = +5.0V$
D.C.	Output Voltage "0"	V_{OL}		+0.2	+0.4	V	$V_{IH} = +4.5V$ $I_{OL} = 10mA$
	Output Voltage "0"	V_{OL}			+0.4	V	$V_{IH} = +3.5V$ $I_{OL} = 3.2mA$
	Output Voltage "1"	V_{OH}	+2.4	+4.0		V	V_{IL} = Open Circuit, $I_{OH} = -240\mu A$
	Power Supply Current Operating	I_{CC}			52	mA	One Input at +5.25V
	Power Supply Current Maximum	I_{CCM}			88	mA	All Inputs at +5.25V
A.C.	Skew Time (Note 1)	T_{SK}		80	200	ns	$T_{Case} = 25^{o}C$, $V_{CC} = V_{IN} = +5.0V$, $C_L < 50pF$

NOTE: (1) Skew time is the maximum time differential between propagation delay times of any outputs including $\overline{strobe}$ and $\overline{K_{RO}}$.

TRUTH TABLE

INPUTS 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	OUTPUTS 1	2	3	4	$\overline{St.}$	$\overline{K_{RO}}$
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H
L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	H
L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H
L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H	L	H
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	H	L	H
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H
L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	H	L	L	H
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L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
ANY TWO OR MORE HIGH																X	X	X	X	L	L

INPUTS: L = Open Circuit or < +1.0V H = > +4.5V Current Source
OUTPUTS: L = < +0.4V H = > +2.4V X = Erroneous Data

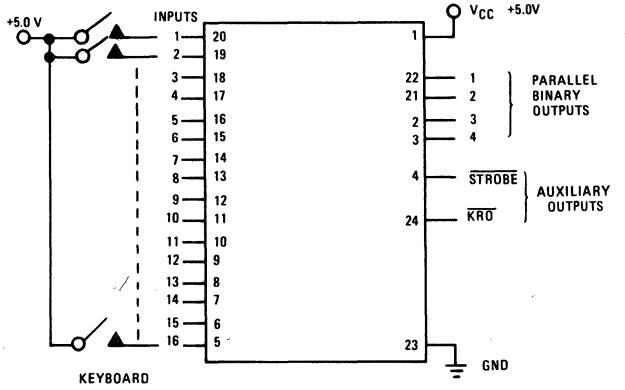


Figure 1. GENERAL CONFIGURATION FOR ENCODING TWO TO SIXTEEN KEYS

The Truth Table is used to determine wiring from the key switches to Encoder inputs to produce desired output codes.

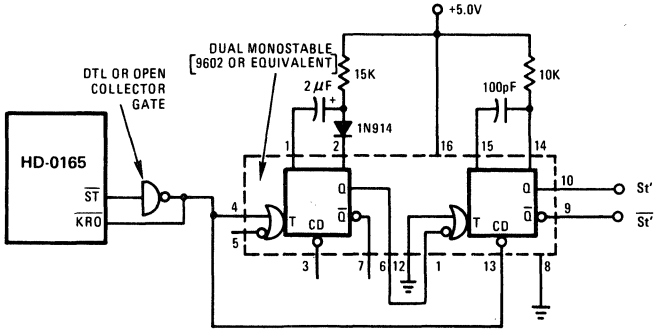
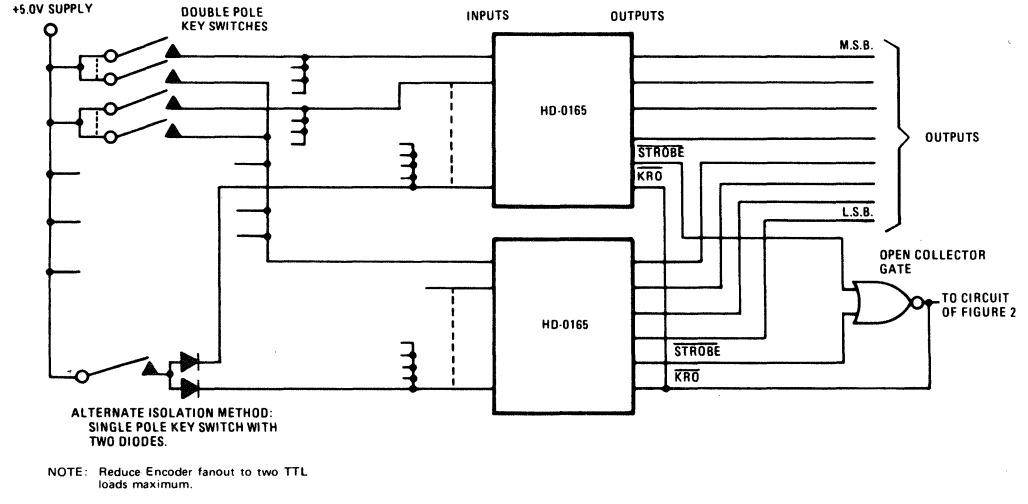


Figure 2. SWITCH BOUNCE ELIMINATION

This circuit generates a delayed Strobe pulse (St'). Delay time is determined by first monostable and should be about 10ms. Pulse width is determined by second monostable and should be set according to system requirements. Effect of switch bounce or arcing on make or break is positively eliminated and proper encoding will take place under two key rollover conditions.



NOTE: Reduce Encoder fanout to two TTL loads maximum.

Figure 3. ENCODING UP TO 256 KEYS

Use upper Encoder to produce the four most significant output bits; the lower to produce the least significant bits. Use Truth Table and required output codes to determine wiring from each key to the two Encoders.

SHIFT and CONTROL functions can be implemented by logic gates in series with the output lines.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

HD-245/545 *Triple Line Transmitter*
HD-246/546/249/549 *Triple Line Receivers*
HD-248/548 *Triple Party Line Receiver*

FEATURES

- CURRENT MODE OPERATION
- HIGH SPEED: 15MHz WITH 50 FT. CABLE; 2MHz WITH 1,000 FT. CABLE
- HIGH NOISE IMMUNITY
- LOW EMI GENERATION
- LOW POWER DISSIPATION
- HIGH COMMON MODE REJECTION
- TRANSMITTER AND RECEIVER PARTY LINE CAPABILITY
- TOLERATES -2.0V GROUND DIFFERENTIAL (Transmitter with respect to receiver)
- TRANSMITTER INPUT/RECEIVER OUTPUT TTL/DTL COMPATIBLE

APPLICATIONS

- AIRCRAFT INSTRUMENTATION
- TELEMETRY
- INDUSTRIAL CONTROLS
- DATA EXCHANGE WITHIN AND BETWEEN BUILDINGS

DESCRIPTION

Each transmitter-receiver combination provides a digital interface between systems linked by 100Ω twisted pair, shielded cable. Each device contains three circuits fabricated within a single monliithic chip. Data rates greater than 15MHz are possible depending on transmission line loss characteristics and length.

The transmitter employs constant current switching which provides high noise immunity along with high speeds, low power dissipation, low EMI generation and the ability to drive high capacitance loads. In addition, the transmitters can be turned "off", allowing several transmitters to time-share a single line.

Receiver input/output differences are shown in the following table:

	INPUT	OUTPUT
HD-246 / 546	100 Ω	OPEN COLLECTOR
HD-248 / 548	HI-Z	6K PULL-UP RES.
HD-249 / 549	100Ω	6K PULL-UP RES.

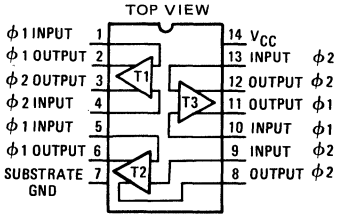
The internal 100Ω cable termination consists of 50Ω from each input to ground.

HD-248/548 "party line" receivers have a high-Z input such that as many as ten of these receivers can be used on a single transmission line.

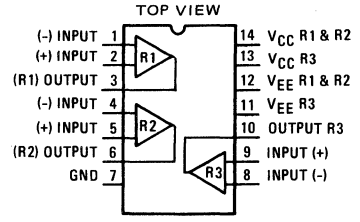
Each transmitter input and receiver output can be connected to TTL and DTL systems. When used with shielded transmission line, the transmitter-receiver system has very high immunity to capacitive and magnetic noise coupling from adjacent conductors. The system can tolerate ground differentials of -2.0V to +20.0V (transmitter with respect to receiver).

PINOUTS

TRANSMITTERS — **Package Codes 9V, 1S**

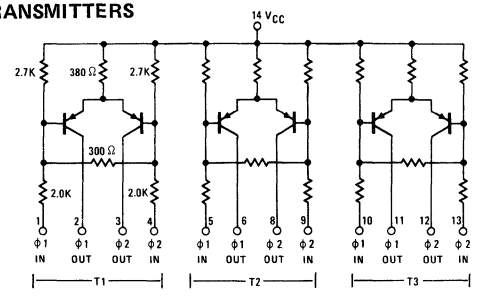


RECEIVERS — **Package Codes 9V, 1S**

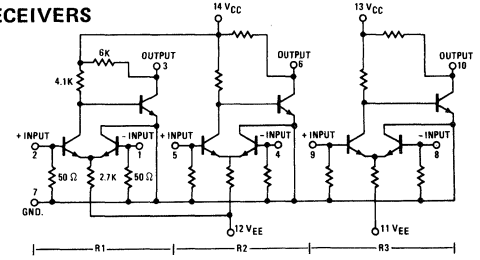


SCHEMATIC DIAGRAMS

TRANSMITTERS



RECEIVERS



NOTES:
1. HD- 249/549 is as shown
2. HD- 246/546 does not have 6K output pull- up resistors.
3. HD- 248/548 does not have 50 Ω input termination
4. Resistor values are nominal resistors.

6

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range: -0.5V to +10V
Output Voltage Range: -30V to +0.5V with respect to V_{CC}

V_{CC} Range: -0.5V to +10V
Storage Temperature Range: -65°C to +150°C

ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	TEMP.	HD-245 -55°C to +125°C MIN.	HD-245 -55°C to +125°C TYP.	HD-245 -55°C to +125°C MAX.	HD-545 0°C to +75°C MIN.	HD-545 0°C to +75°C TYP.	HD-545 0°C to +75°C MAX.	UNITS	TEST CONDITION V_{CC}	TEST CONDITION NOTES
DC	INPUT LOW CURRENT	I_{IL}	25°C Full		-1.5	-2.2 -2.5		-1.5	-2.3 -2.4	mA	5.5	1
DC	"ON" OUTPUT CURRENT	I_{OUT} "ON"	25°C Full Full	-2.3 -2.0 -1.6			-1.9 -1.8 -1.5			mA mA mA	4.5 4.5 4.5	1 1 2
DC			25°C Full		-4.1	-5.4 -5.6		-4.1	-6.3 -6.7	mA	5.5	1
DC	"ON" OUTPUT CURRENT UNBALANCE	ΔI_{OUT}	25°C Full		0.1	0.25 0.3		0.1	0.25 0.3	mA	5.5	3
DC	"OFF" OUTPUT CURRENT	I_{OUT} "OFF"	25°C Full		-30	-100 -100		-30	-100 -100	μA	4.5	1
DC	OUTPUT BREAKDOWN	BV_{CER}	25°C	-30	-50		-30	-50		V	GND	4
DC	POWER SUPPLY CURRENT-TOTAL		25°C 25°C		15	18.6 0.6		15	24 0.6	mA	5.0	5 6
AC	PROPAGATION DELAY	t_{PLH}	25°C Full		3	10 14		3	10 14	ns	5.0	
AC	TEST CIRCUIT 1, PAGE 4	t_{PHL}	25°C Full		3.2	10 14		3.2	10 14	ns	5.0	

NOTES:
1. One input at Gnd. one input open, each output at
2. One input at 0.45V, one input open, each output at Gnd.
3. Difference between $\phi 1$ and $\phi 2$ "ON" output data current.
4. Each input at Gnd., one output at Gnd., $I_{Limit} \geq 100\mu A$ on output tested with -30V applied.
5. One input of each transmitter at Gnd. and the other input open. All six output lines at Gnd.
6. All six input lines open, all six output lines at Gnd.

ABSOLUTE MAXIMUM RATINGS

Input Voltage Range	-1.0V to +1.0V	Input Current	±25mA
Output Voltage Range	-0.5V to +6.0V	Output Current	+50mA
V_{CC} Range	-0.5V to +8.0V	Storage Temperature	-65°C to +150°C
V_{EE} Range	-8.0V to +0.5V		

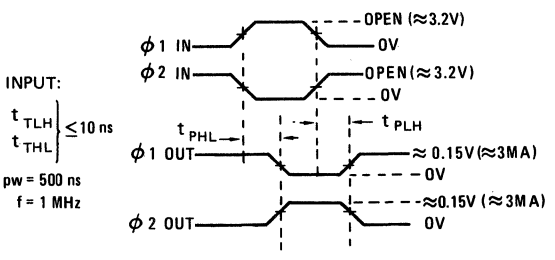
ELECTRICAL CHARACTERISTICS

	PARAMETER	SYM.	TEMP.	HD-246 / 248 / 249 -55°C to +125°C MIN.	TYP.	MAX	HD-546 / 548 / 549 0°C to +75°C MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS V_{EE} = -5V V_{CC}	NOTES
	INPUT RESISTANCE (HD-246/546 & HD-249/549	R_{IN}	+25°C Full	40 39	47	61 68	35 33	47	65 70	Ohms		
	PULL-UP RESISTOR (HD-248/548 & HD-249/549)		+25°C Full	4.2 4.1	6	7.8 8.6	4.0 3.9	6	8.1 8.6	K Ohms		
	OUTPUT VOLTAGE (HIGH)	V_{OH}	+25°C Full	2.6 2.5			2.6 2.5			V	4.5	Note 1 I_{OH}=-120μA Ext. 6K Res. For HD-246/546
DC	OUTPUT VOLTAGE (LOW)	V_{OL}	+25°C Full			0.45 0.45			0.45 0.45	V	4.5	Note 2 I_{OL}=9.6mA 10mA For HD-246/546
	OUTPUT VOLTAGE (LOW) (INPUT SHORTCIRCUIT)	V_{OLSC}	+25°C		0.4			0.4		V	5.0	Note 3 I_{OL} = 3.2mA
	POWER SUPPLY CURRENT (TOTAL) HD-246 / 546	I_{CC} I_{EE}	+25°C		3.3 5.1	4.8 6.3		3.3 5.1	5.7 6.3	mA	5.0	Note 4
		I_{CC} I_{EE}	+25°C		3.9 5.1	6.6 6.3		3.9 5.1	7.5 6.3	mA	5.0	Note 5
	HD-248 / 548	I_{CC} I_{EE}	+25°C		6.3 5.1	7.8 6.3		6.3 5.1	8.7 6.3	mA	5.0	Note 4
		I_{CC} I_{EE}	+25°C		3.9 5.1	6.6 6.3		3.9 5.1	7.5 6.3	mA	5.0	Note 5
	HD-249 / 549	I_{CC} I_{EE}	+25°C		6.3 5.1	7.8 6.3		6.3 5.1	8.7 6.3	mA	5.0	Note 6
		I_{CC} I_{EE}	+25°C		3.9 5.1	6.6 6.3		3.9 5.1	7.5 6.3	mA	5.0	Note 7
	PROPAGATION DELAY	t_{PLH}	+25°C Full		18	30 30		18	30 30	ns	5.0	
AC	TEST CIRCUIT 2 PAGE 4	t_{PHL}	+25°C Full		25	30 30		25	30 30	ns	5.0	

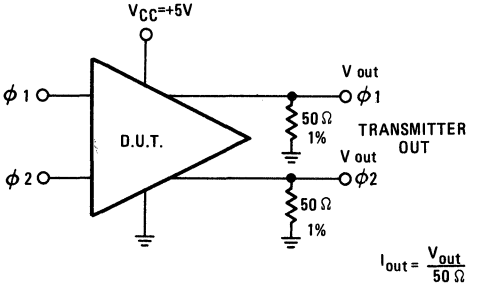
NOTES:
1. (+) I_{IN} = 1.5mA; (-) Input = open (For HD-248/548; Ext. 50 Res. or 75mV).
2. (+) Input = open; (-) I_{IN} = 1.5mA. (For HD-248/548; Ext. 50 Res. or 75mA).=
3. Both inputs shorted to Gnd; or both inputs open such that 50 termination resistors are in the circuit.
4. (+) Input = open; (-) I_{IN} = 3mA.
5. (+) I_{IN} = 3mA; (-) Input = open.
6. (+) Input = Gnd.; (-) Input = .15V.
7. (+) Input = .15V; (-) Input = Gnd.

TEST CIRCUITS

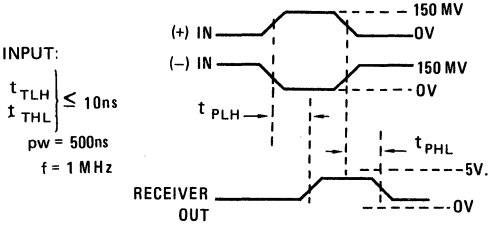
TEST CIRCUIT 1 - TRANSMITTER PROPAGATION DELAY



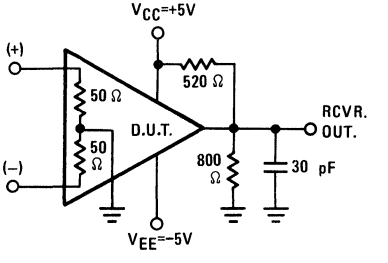
All measurements referenced to 50 % V points



TEST CIRCUIT 2 - RECEIVER PROPAGATION DELAY



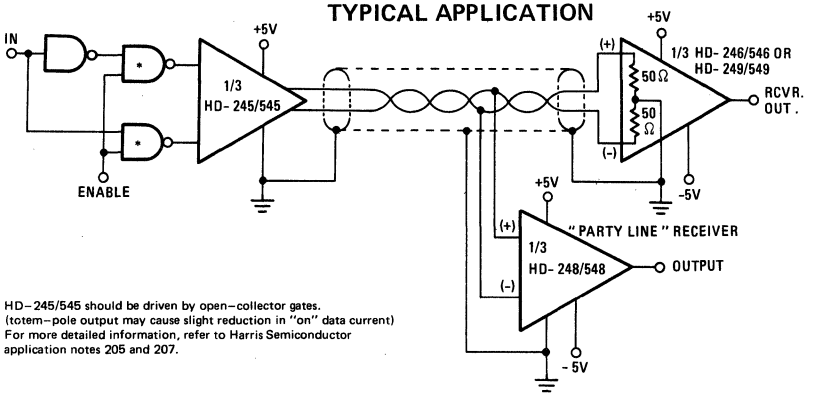
All measurements referenced to 50%V points.



NOTE: External 50Ω resistors needed for HD–248/548.

APPLICATIONS

TYPICAL APPLICATION



* HD–245/545 should be driven by open–collector gates. (totem–pole output may cause slight reduction in "on" data current) For more detailed information, refer to Harris Semiconductor application notes 205 and 207.

Analog Application Notes

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 204

DESIGNING WITH THE HD-0165 KEYBOARD ENCODER

BY D. F. JONES

The Harris Semiconductor type HD-0165 Keyboard Encoder integrated circuit provides an ideal low cost means of transforming signals from any manual keyboard into a TTL compatible parallel binary code.

CODE IMPLEMENTATION

The organization and truth table for the HD-0165 are shown in Figure 1 and Table 1. Basically, there are sixteen input lines, only one of which is normally connected at a time through the keyboard to the +5V supply. There are four output lines which produce a parallel binary code which is determined by the actuated input lines. The outputs will drive any DTL or TTL circuits with a fanout of six normal loads. The function of the two auxiliary outputs will be explained later.

To produce a certain output code by actuating a particular key, simply look down the output columns (1–4) of the truth table until the desired four-bit code is found; then look across to see which input is high (H) and connect that input pin to the key.

One fact which should be obvious is that since all sixteen possible combinations of four bits are available on the output lines, the numbering system for the input and output lines is arbitrary. The ordering of the truth table arbitrarily shows an ascending negative logic (H=0, L=1) output in binary code with output line 4 the most significant bit. But we do not need to be governed by this. If we want the "zero" key to produce LLLL, we do not need to tie input 1 to that key and put inverter gates in series with the outputs; we can simply tie input 16 to the "zero" key. Similarly, we could wire up a ten button keyboard to yield a 1–2–4–8 BCD code, a 1–2–4–2 BCD code, a 1–2–2–5 code, a Gray code, or any other code up to four bits simply by using the truth table and wiring the inputs to the appropriate keys. Redundant codes can be generated, if desired, by wiring one input line to more than one key.

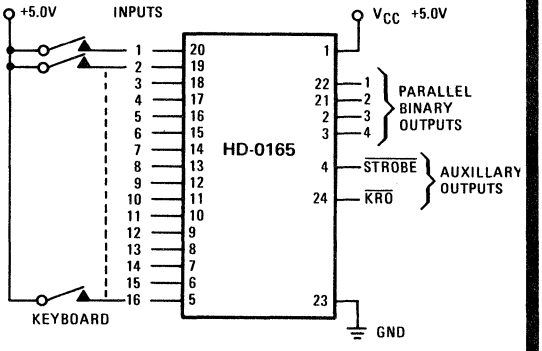


Figure 1. Keyboard Encoder Organization

ENCODING MORE THAN SIXTEEN KEYS

Two keyboard encoder circuits may be used to encode up to 256 keys, represented by eight bits.

The general scheme is to let the outputs from one device represent the four most significant bits and the output from the other device represent the four least significant bits of the output word. Each key is wired to one input on each of the two devices to produce the desired output code.

It is necessary to isolate the two wires from each key, since each device input usually is connected to more than one key. This is accomplished either by using double-pole key switches, or by using two diodes per key in series with the device input lines. The general scheme for cascading two encoders is shown in Figure 2.

TABLE I
TRUTH TABLE, HD-0165

INPUTS																OUTPUTS					
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	1	2	3	4	St.	K_{RO}
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H
L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	H
L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H
L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H	L	H
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	H	L	H
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H
L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	H	L	L	H
L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	L	L	H
L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
ANY TWO OR MORE HIGH																X	X	X	X	L	L

INPUTS: L = Open Circuit or < +1.0V H = > +4.5V Current Source
OUTPUTS: L = >+0.4V H = > +2.4V X = Erroneous Data

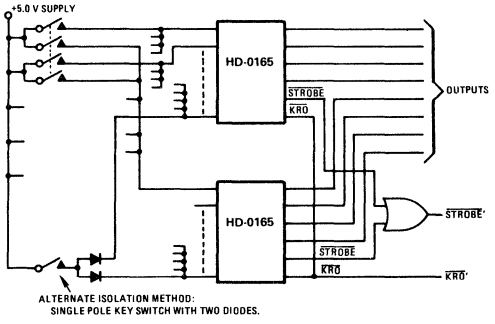


Figure 2

An important fact – when diode input isolation is used the diode forward voltage drop decreases the input current available to the encoder, and the result is that the encoder output fanout should be reduced to two TTL loads. The fanout capability could be restored by returning the keys to a higher voltage (+5.7V to +6.0V). This voltage could be generated by placing a high-current diode between the normal supply regulator output and its sense line, as shown in Figure 3.

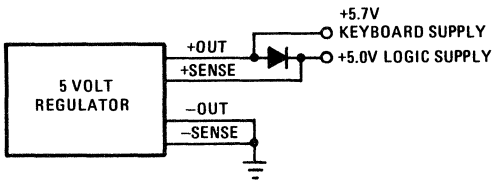


Figure 3

AUXILIARY OUTPUTS

As shown in the truth table, the STROBE output is high if no keys are actuated, and becomes low when any key is actuated. This signal is normally used to gate the encoded signal into other circuitry, and may be conditioned to eliminate any effects of switch bounce or skew in output propagation delays.

The KEY ROLLOVER (K_{RO}) output is normally high, and goes low only when two or more keys are actuated simultaneously. This signals that the output data word is not valid during that time.

Figure 4 illustrates one method of switch bounce surpression which also gives correct data input under key rollover conditions. One dual retriggerable monostable multivibrator device is required per keyboard to suppress multiple strobe pulses resulting from key bounce or arcing on either "make" or "break". With this scheme, there is no necessity for the use of mercury-wetted or other exotic key switches to prevent bounce effects.

The strobe and K_{RO} outputs from one or more encoders are combined at point A; so that the signal at point A is high when any one key is depressed, and low when no key or two or more keys are depressed.

The time delay, T_1, generated by the first monostable must be longer than the worst expected interval between switching spikes –

about 3 to 10 milliseconds is usually sufficient.

The time delay, T_2, generated by the second monostable depends on system requirements – about 0.5 microseconds will result from the values shown.

The waveforms shown at A, B, and C show a typical situation. At interval I, a key is depressed and the first monostable generates a delay, T_1, sufficiently long to allow any switch bounce spikes to die out. At the trailing edge of T_1, the second monostable generates a strobe pulse, T_2, for entering the data into the system. The delayed strobe also assures that the parallel data are stabilized when strobed into the system.

At interval II, a second key is depressed while the first key is not released until interval III. The first monostable might be triggered at this time, but this will not cause an output at C, because the clear (C_D) terminal of the second monostable will be held low. At interval III, when the first key is released, the two monostables will again be triggered, entering the data from the second key into the system.

If noise occurs at interval IV, when the second key is released, no signal will appear at C since C_D will again be low before the trailing edge at B is generated.

For data entry, it is necessary that a key be held down for longer than T_1, but since this interval is only a few milliseconds, it is highly unlikely that any deliberate key depression would be for a shorter interval.

The delayed strobe pulse, S_t, is used to signal the presence of new data to the system. The pulse can be used to gate a latch circuit or, if a serial data format is required, the pulse can be used to enable the parallel loading of a shift register.

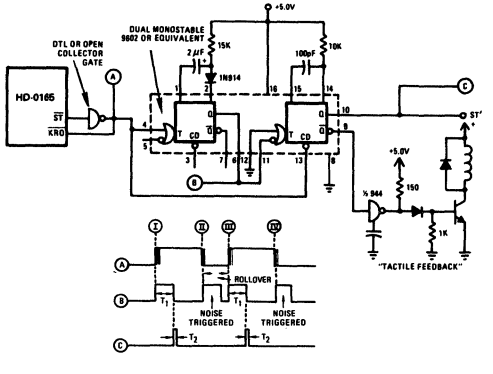


Figure 4. Switch Bounce Elimination

An optional "tactile feedback" circuit is also shown in Figure 4, which for a small increase in cost will greatly increase operator accuracy at high entry speeds. The transistor load is either a small solenoid hammer which taps the keyboard area, or a small loudspeaker which produces an audible "tick" each time data is entered. Since the "tick" only occurs when data entry actually occurs in the system, this scheme will give more accuracy (probably at lower cost) than special "tactile feel" key switches. Actual circuitry will depend on the type of load used. A capacitor is shown at the gate expander terminal to stretch the pulse at this point.

BATTERY OPERATED KEYBOARD

The circuit shown in Figure 5 will help conserve battery life in a portable keyboard. When no key is depressed, the PNP transistor is turned off, and there is no battery drain. When any key is pressed, the input current causes the transistor to turn on, supplying power to the encoder and to any other digital circuitry. The transistor should be capable of switching the necessary current and should have low $V_{CE(Sat)}$ for low power dissipation.

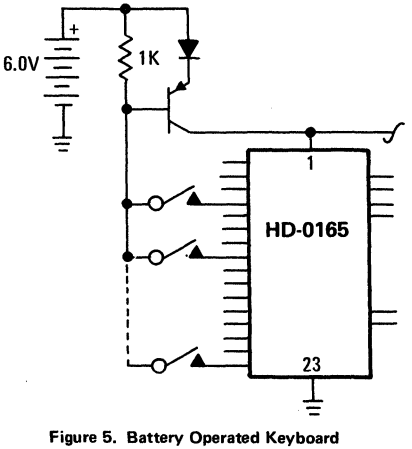


Figure 5. Battery Operated Keyboard

DESIGN EXAMPLE: TELETYPEWRITER KEYBOARD ENCODER

Each keyboard encoding design task must start with an analysis of the code to be produced and the arrangement of the keyboard. A minor complication arises when a single key must produce more than one code; for example when SHIFT and CONTROL keys are used.

7

As an example we will design a keyboard encoder for a teletypewriter or CRT terminal using the standard ASCII code for capital letters only, plus symbols and control functions.

First, for convenience, using the encoder truth table, we will assign a hexidecimal character to each device input line. The conventions for the output will be: positive logic (L=0, H=1); output line 1 will be the L.S.B., and output line 4 will be the M.S.B. This results in Table II.

Now, we tabulate the desired output words as a two digit hex code (Table III) with the first digit representing the four most significant bits and the second digit representing the four least significant bits. This now gives us the wiring list to correct each key in the normal (unshifted) mode to the two encoder circuits as in Figure 2. Since the hex code for "A" is CI, we can connect the two wires from the "A" key to the C input (Pin 17) of the top encoder and to the 1 input (Pin 6) of the bottom encoder of Figure 2. The rest of the keys are wired similarly for the specified output code in the unshifted state.

TABLE II
HEX CHARACTER ASSIGNMENT

HEX CHARACTER	INPUT LINE	PIN NUMBER
0	16	5
1	15	6
2	14	7
3	13	8
4	12	9
5	11	10
6	10	11
7	9	12
8	8	13
9	7	14
A	6	15
B	5	16
C	4	17
D	3	18
E	2	19
F	1	20

TABLE III
ASCII TELETYPEWRITER CODE

CHARACTER	HEX	CHARACTER	HEX	CHARACTER	HEX	CHARACTER	HEX
@	C0	Blank	A0	NULL	80	ACK	FC
A	C1	!	A1	SOH	81	ALT	FD
B	C2	"	A2	STX	82	ESC	FE
C	C3	#	A3	ETX	83	Rubout	FF
D	C4	$	A4	EOT	84		
E	C5	%	A5	WRU	85		
F	C6	&	A6	RU	86		
G	C7	'	A7	BELL	87		
H	C8	(	A8	FE	88		
I	C9	)	A9	HT	89		
J	CA	*	AA	LF	8A		
K	CB	+	AB	VT	8B		
L	CC	,	AC	FF	8C		
M	CD	–	AD	CR	8D		
N	CE	.	AE	SO	8E		
O	CF	/	AF	AI	8F		
P	D0	0	B0	DC0	90		
Q	D1	1	B1	X-ON	91		
R	D2	2	B2	Tape-ON	92		
S	D3	3	B3	X-OFF	93		
T	D4	4	B4	Tape-OFF	94		
U	D5	5	B5	ERR	95		
V	D6	6	B6	SYN	96		
W	D7	7	B7	LEM	97		
X	D8	8	B8	S_0	98		
Y	D9	9	B9	S_1	99		
Z	DA	:	BA	S_2	9A		
[	DB	;	BB	S_3	9B		
\	DC	<	BC	S_4	9C		
]	DD	=	BD	S_5	9D		
↑	DE	>	BE	S_6	9E		
←	DF	?	BF	S_7	9F		

TABLE IV

KEY			ENCODER INPUT	
NORMAL	SHIFT	CONTROL	MSB	LSB
A		SOH	C	1
B		STX	C	2
C		ETX	C	3
D		EOT	C	4
E		WRU	C	5
F		RU	C	6
G		BELL	C	7
H		FE	C	8
I		HT	C	9
J		LF	C	A
K	[	VT	C	B
L	\	FF	C	C
M	]	CR	C	D
N	↑	SO	C	E
O	←	SI	C	F
P	@	NUL	D	0
Q		X-ON	D	1
R		Tape-ON	D	2
S		X-OFF	D	3
T		Tape-OFF	D	4
U		ERR	D	5
V		SYN	D	6
W		LEM	D	7
X		S_0	D	8
Y		S_1	D	9
Z		S_2	D	A

KEY			ENCODER INPUT	
NORMAL	SHIFT	CONTROL	MSB	LSB
1	!		B	1
2	"		B	2
3	#		B	3
4	$		B	4
5	%		B	5
6	&		B	6
7	'		B	7
8	(		B	8
9	)		B	9
0			B	0
:	*		B	A
–	=		A	D
.	>		A	E
,	<		A	C
;	+		B	B
/	?		A	F
Line Feed			8	A
Return			8	D
Rubout			F	F
Space			A	0
ACK			F	C
ALT			F	D
ESC			F	E

For this example, we will design one of the more popular terminal keyboard arrangements as shown in Table IV.

Comparing Table IV with Table III, we note that the L.S.B.'s change in a particular pattern: A→B, B→A, C→D, D→C. Further investigation shows that this is simply an inversion of the fifth output bit. So, we could make the SHIFT key control a group of gates in series with the fifth output bit to pass this bit either inverted or not inverted.

Investigation of the control mode codes shows that bits 6 and 7 must always be "0" when the CONTROL key is depressed, the other bits remaining the same as in the normal mode for that key. This can easily be implemented by connecting DTL gates in "wired-OR" to these outputs. Control functions S_3 through S_7 can be generated by holding both the SHIFT and CONTROL keys down and pressing "L" through "P", respectively; or these could be implemented by additional wiring.

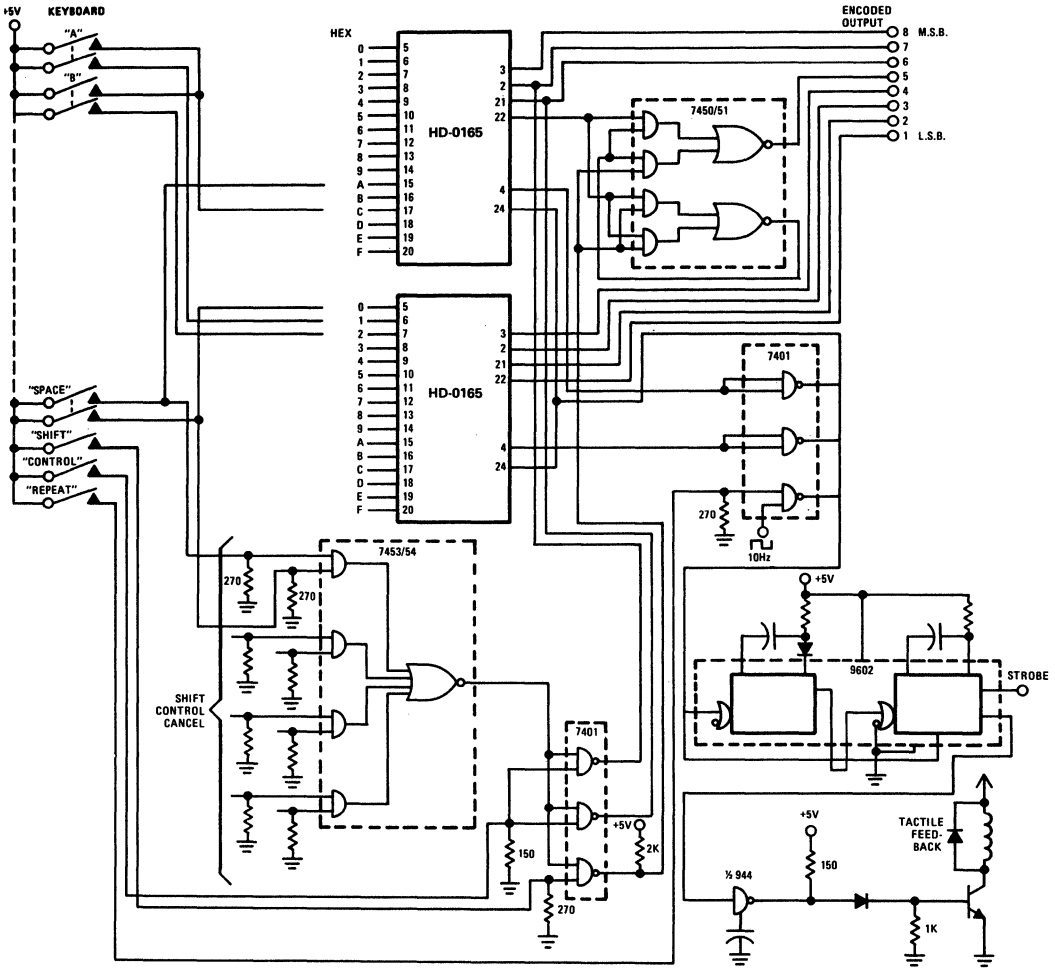


Figure 6. Teletypewriter (ASCII) Encoder

Figure 6 shows the finished design, with the wiring from keys to encoder input indicated in Table IV.

It may be desirable to have some keys, such as the SPACE bar, produce the same output in all three modes. If the "cancel" inputs shown in Figure 6, are wired to those keys, the effect of the SHIFT and CONTROL keys will be nullified for those particular keys.

An optional feature shown is the REPEAT key which pulses the strobe output at about 10cps as long as it and another key are held down.

A full typewriter ASCII keyboard with upper and lower case letters can be implemented in a similar fashion. The "shift" requires inversion of either bit 5 or bit 6 depending on the state of bit 7, so the logic at the output is somewhat more complex.

UNIVERSAL KEYBOARD ENCODER

Suppose we required a keyboard with a code in which there was no simple logical relationships between shifted and unshifted output words—or a keyboard which could produce several entirely different codes at the flip of a switch—or one which could be supplied with any desired code on very short notice. Any of these problems can be readily solved by using keyboard encoder circuits to generate a universal code—which can then be translated to the desired output code using programmable read-only memories.

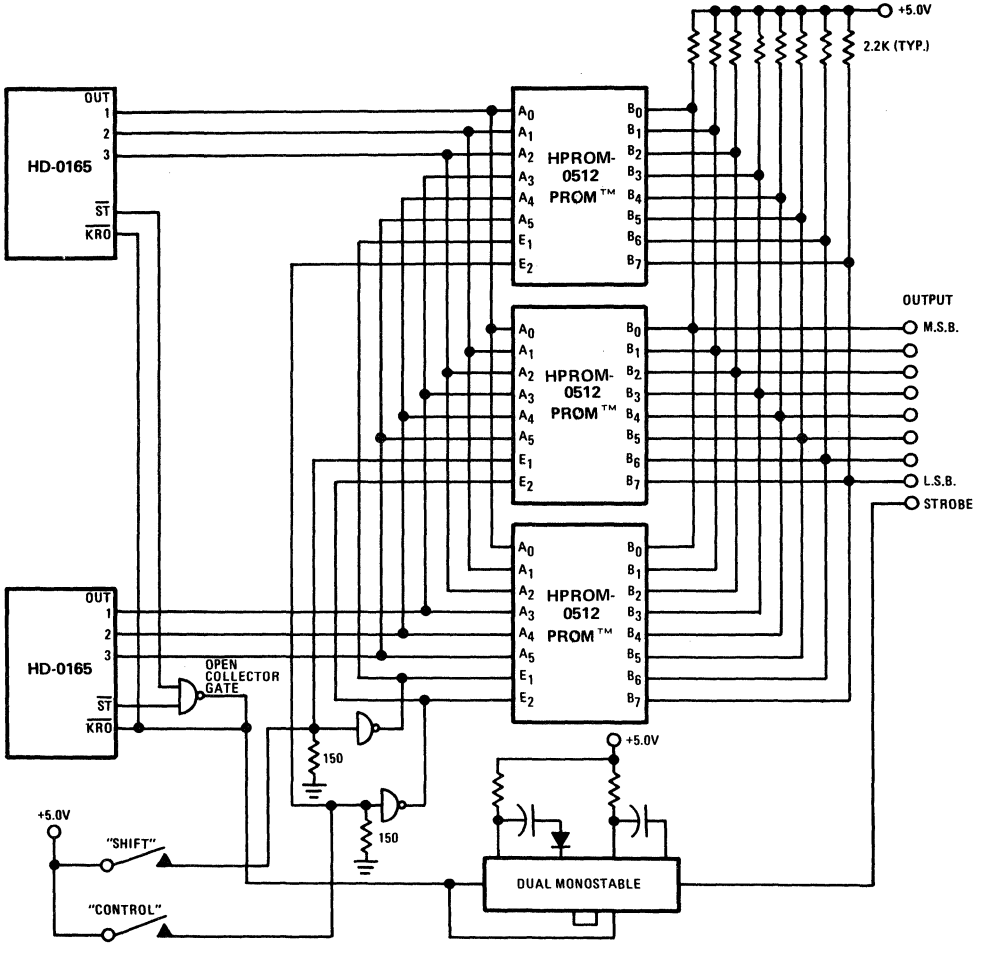


Figure 7. Universal Keyboard Encoder

Figure 7 shows the organization for a universal keyboard encoder. Up to 64 keys are wired to two encoder circuits which produce a six-bit output code (the fourth output bit of each encoder is not used). The key to encoder wiring is arbitrary as long as each key produces a unique six-bit output code from the encoders.

The six-bit code forms the address for one of three ROM's wired in parallel. Each HROM-0512 stores 64 eight-bit words, which can be programmed electrically by the user (contact Harris Semiconductor for data sheets and programming instructions).

Each ROM is initially programmed for the desired output word at the address location corresponding to a certain key. One ROM contains all 64 output words for the unshifted mode, the second contains all words for the shifted mode, and the third contains all words for the control mode. Selection of the particular ROM is accomplished through its enable inputs.

Obviously, there is no requirement for a logical relationship between corresponding words in the three ROM's, which greatly simplifies implementation of special codes. If it is desired that a particular word remain the same in all three modes, simply program the same word at the same address in the three ROM's.

A great advantage of this system is that any eight-bit code can be produced without any changes in wiring or P.C. board layout, simply by plugging in ROM's programmed to desired code. Additional ROM's could be wired in parallel with the enable inputs wired appropriately to produce multiple codes (both ASCII and EBCDIC codes, for example) either simultaneously or selectively.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 205

HIGH SPEED DIGITAL COMMUNICATIONS

BY G. G. MILER

INTRODUCTION

The use of high speed digital communications is rapidly increasing. This is partially due to the FCC decision to allow competition in data communications as well as the great increase in the use of computers with data communications capability. The use of management information systems is expected to continue to grow at a rapid rate. This will result in increased usage of sophisticated data collection systems , as well as the increased usage of remote data entry terminals and display systems.

There are several general classes of digital communications systems discussed in this application note. Low and moderate speed local digital systems are defined by EIA Standard RS-232. This type of system is intended for local (less than 100 feet) communications between the computer system and the long distance communications system interface (modem). Modems are generally required for long distance (greater than 10 miles) digital communications systems. Coaxial lines and microwave links are generally required for high speed, long distance data communications systems. Another general class of digital communications which is rapidly growing is that used for communications within a company. Distances of up to several thousand feet are generally required for high speed communications between a data acquisition, system, or process control system and the central computer system.

VOLTAGE MODE TRANSMISSION

Data rates of up to 10 million bits per second can be obtained with standard TTL logic; however, the transmission distance must be very short. For example, a typical 50 foot low capacitance cable will have a capacitance of approximately 750pF which requires a current of greater than 50mA to drive 5V into this cable at 10MHz; therefore, voltage mode transmitters are undesirable for long transmission lines at high data rates due to the large current required to charge the transmission line capacitance.

CURRENT MODE TRANSMISSION

An alternate method of driving high data rates down long transmission lines is to use a current mode transmitter. Current mode logic changes the current in a low impedance transmission line and requires very little change in voltage. For example, a 2mA change in transmitter current will produce a 100mV change in receiver voltage independent of the series transmission line resistance. The rise time at the receiver for a typical 50 foot cable (750pF) is approximately 30ns for a 2mA pulse.

An emitter coupled logic gate is frequently used for a current mode transmitter. However, ECL gates are not compatible with TTL and DTL logic and they require considerable power. The Harris Semiconductor HD-245/545 is a TTL/DTL compatible current mode transmitter designed for high data rates on long transmission lines. Data rates of 15 megabits per second can be obtained with 50 feet of transmission line when using the companion HD-246/546 or HD-249/549 receiver. Data rates of 2 megabits per second are easily obtained on transmission lines as

long as 1,000 feet. The Harris transmitter and receivers feature very low power, typically 25mW for the transmitter and 15mW for the receiver.

HARRIS TRANSMITTER/RECEIVERS

The Harris transmitter/receiver family consists of a triple line transmitter, two triple line receivers with internal terminations and a triple party-line receiver. The general characteristics of the transmitter and receivers are outlined in Table I.

Triple Line Transmitter

PARAMETER	HD-245	HD-545	UNITS	COMMENTS
Operating Temp. Range	-55 to +125	0 to +75	°C	
"ON" Output Current	2.0 MIN	1.8 MIN	mA	Over full temp. range
Power Supply Current	6.2 MAX	8.0 MAX	mA	Per transmitter section
Standby Current	33 MAX	33 MAX	µA	Per transmitter section
Propagation Delay	10 MAX	10 MAX	ns	25°C

Triple Line Receiver

PARAMETER	RECEIVER TYPE	LIMITS	UNITS	COMMENTS
Operating Temp Range	HD-246/248/249	-55 to+125	°C	
Power Supply I_{CC} (V_{CC}=+5.0V)	HD-246/248/249	2.2	mA	Per receiver section
	HD-546/548/549	2.5	mA	With Output High
Propagation Delay	All Receivers	30	ns	25°C
Input Impedance and Output Circuit	HD-246/546	Input 100	Ohm	Output Open Collector
	HD-248/548	Hi-Z		6K Pull-up Resistor
	HD-249/549	100	Ohm	6K Pull-up Resistor

Table I. General Transmitter/Receiver Characteristics

TRANSMITTER

The HD-245/545 transmitters have two inputs per transmitter, either of which is low while the other is open during normal operation and both inputs are open during standby. For optimum transmitter performance, the "off" input should be open circuit rather than being pulled towards +5V, because this will reduce the "on" output data current. On the other hand, the "on" and "off" output data current will be increased if the "off" input is held below its open circuit voltage. Open collector gates such as the 7401 and 7403 or 7405 Hex-Inverter are suitable for driving the HD-245/545 transmitter inputs. By using 2-input gates as shown in Figure 1, an enable line can be provided so that more than one transmitter may be connected to a line for time sharing. When the enable line is low the transmitter will be disabled and will present a high impedance to the transmission line as well as requiring very little power supply current.

Complementary input signals may be derived from high speed inverter gates as shown, or by using the complementary outputs of a flip-flop. When the transmitter is connected near the midpoint of a long transmission line or to a line with terminations at both ends, two transmitter sections should be paralleled with respective inputs and outputs connected together in order to drive the reduced impedance. This parallel transmitter technique can also be used to increase the data rate on long transmission lines.

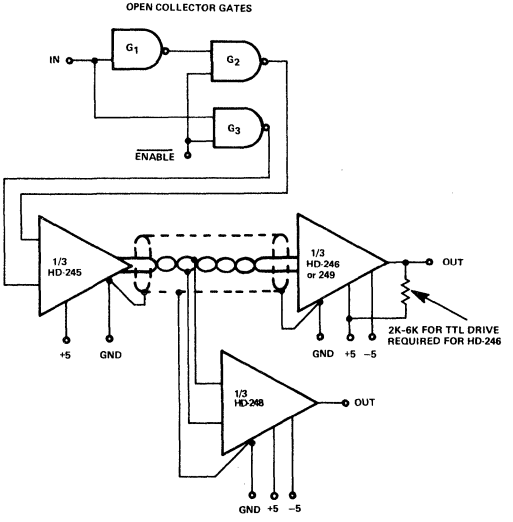


Figure 1. Typical Data Transmission System

TRANSMITTER OPERATION

The transmitter alternately applies the current to each of the two conductors in the twisted pair line such that the total current in the twisted pair is constant and always in the same direction. This current flows through either of the two 50 ohm terminating resistors at the receiver and returns to the transmitter as a steady D.C. current on the transmission line shield. The D.C. power supply return for the transmitter is through the receiver terminating resistors (the transmitter

ground pin is only a substrate ground). Therefore, it is essential that the shield be connected to the power supply common at both the transmitter and receiver, preferably at the integrated circuit "ground" pin. More than fifteen twisted pair lines can share the the same shield without crosstalk.

RECEIVERS

The HD-248/548 "party-line" receiver presents a high impedance load to the transmission line allowing as many as ten HD-248/548 receivers to be distributed along a line without excessive loading. Figure 1 shows a typical system of a transmitter, a terminating receiver and a party-line receiver. The transmission line is terminated in its characteristics impedance by an HD-246/546, HD-249/549, or by a pair of 50 ohm resistors connecting each line to the ground return shield.

TRANSMISSION LINES

The maximum frequency (or minimum pulse width) which can be carried by a certain length of a given transmission line is dependent on the loss characteristics of the particular line. At low frequencies, there will be virtually no loss in pulse amplitude, but there will be a degradation of rise and fall-time which is roughly proportional to the square of the line length. This is shown in Figure 2. If the pulse width is less than the rise-time at the receiver end, the pulse amplitude will be diminished, approaching the point where it cannot be detected by the receiver.

The transmission line used with the Harris HD-245/545 series transmitter and receivers can be any ordinary shielded, twisted pair line with a characteristic impedance of 100 ohms. Twisted pair lines consisting of number 20 or 22 guage wire will generally have this characteristic impedance. Special high quality transmission lines are not necessary and standard audio, shielded-twisted pair, cable is generally suitable.

Since the necessary characteristics for various twisted pair lines are not readily available, it may be necessary to take some measurements on a length of the proposed line. To do this, connect an HD-245/545 transmitter to one end of the line (100 feet or more) and an HD-246/546 or an HD-249/549 receiver to the other end. The rise and fall-times can be measured on the line at both ends and the constant "K", for that line can be computed as shown in Figure 2 so that the minimum pulse width can be determined for any length of line.

Data rates of 2MHz have been obtained using 1,000 feet of standard shielded, twisted pair, audio cable. Data rates of 15MHz are possible on shorter lengths of transmission line (50 feet).

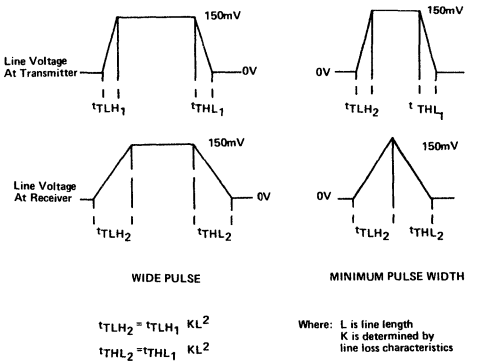


Figure 2. Transmission Line Wave-Shaping

ELECTROMAGNETIC INTERFERENCE

Very little electromagnetic interference is generated by the Harris current mode system because the total current through the twisted pair is constant, while the current through the shield is also constant and in the opposite direction. This can be verified by observing, with a current probe, the total current through the twisted pair, through the shield and through the complete shielded, twisted pair cable. In each case a constant current will be observed with only small variations. Small pulses may be observed if the complementary inputs to the transmitter do not switch at the same time. The current will decrease during the time both inputs are high, and will increase during the time both inputs are low. These switching pulses may be observed when using the circuit shown in Figure

1. The amplitude and shape of these pulses will depend on the propagation delay of G_1, and transition times of G_2 and G_3. These pulses are generally of no concern because of their small amplitude and width, but they may be reduced by increasing the similarity of the waveforms and timing synchronization of the complementary signals applied to the transmitter.

In addition to generating very little noise, the system is also highly immune to outside noise since it is difficult to capacitively couple a differential signal into the low impedance twisted pair cable and it is even more difficult in induce a differential current into the line due to the very high impedance of the constant current transmitter. Therefore, differential mode interference is generally not a problem with the Harris current mode system. Large common mode voltages can also be tolerated because the output current of the transmitter is constant as long as the receiver termination ground is less than 2V positive with respect to the grounded input of the transmitter, and is less than 25V negative with respect to the transmitter V_{CC}. The current mode system is totally unaffected by ground differential noise of $\pm 2V$ at frequencies as high as 1 MHz.

PROPAGATION DELAY

CHARACTERISTICS	-55°C to +125°C HD-245/246/248/249			0°C to +75°C HD-545/546/548/549			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay T_{PLH}		18	40		18	40	ns
Propagation Delay T_{PHL}		18	40		18	40	ns
Duty Cycle Distortion $T_{PLH} - T_{PHL}$		2	15		4	20	ns

V_{CC}=+5V, V_{EE}= −5V

Table II. Overall Transmitter/Receiver Switching Characteristics

The worst case propagation delay of a transmitter and receiver, connected as shown in Figure 1, can be determined by adding the maximum delay shown on the data sheet for the transmitter and receiver. These overall switching characteristics are shown in Table II.

For the entire system, however, the propagation delay of the transmission line must also be considered. This delay, of course, depends on the length of the line and the characteristics of the line, but in general, delays of between 1.5ns and 3.0ns per foot can be expected.

SUMMARY

The optimum data communications system for very high speed data transfer over long transmission lines is the current mode system. The Harris current mode transmitter/receiver system provides a combination of: the high speed required, excellent noise immunity, low power consumption and very low levels of RFI.

Complex digital communications systems design can be simplified by fully utilizing the unique features of the Harris HD-245 family current mode system.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 207

RECEIVER/TRANSMITTER NOISE IMMUNITY

BY DON JONES &
GEORGE MILER, JR.

INTRODUCTION

This paper is intended to answer many questions which have arisen about the noise immunity of Harris Semiconductor's HD-245 family digital line transmitter/receiver system relative to other systems.

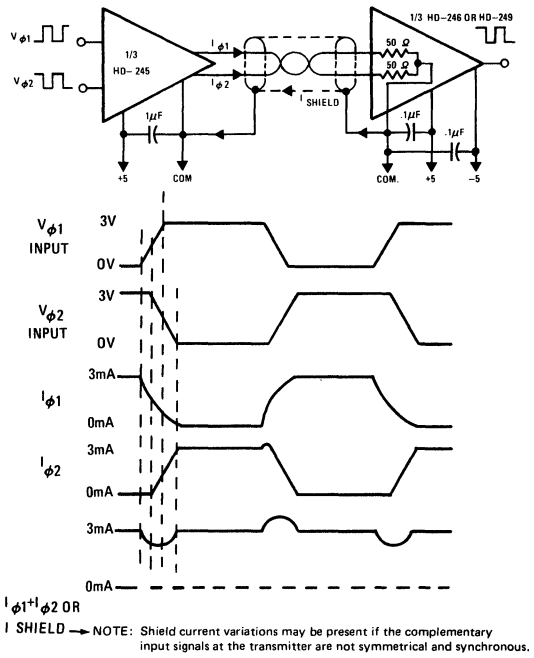


Figure 1- Harris Current Mode System

Shown in Figure 1 is the operation of the HD-245/249 system. First, line $\phi1$ conducts a current of about 3mA which travels down the line through one of the 50Ω terminating resistors in the receiver and returns through the transmission line shield to the transmitter power supply common. Then, the current on line $\phi1$ shuts off and line $\phi2$ conducts current which is also returned through the shield. The shield essentially carries the same DC current since lines $\phi1$ and $\phi2$ alternate in conduction. There may be small variations in the transmission line current if both transmitter inputs are high or low simultaneously during the data transition times. The important fact concerning noise immunity is that this is essentially a three conductor transmission system, and in most instances, externally generated noise affects all three conductors.

The noise which can affect a digital line transmission system includes several types:

1. Magnetic and capacitive pickup from other electrical conductors in the near proximity to the transmission line.
2. Magnetic and capacitive crosstalk between transmission lines sharing a common shield.
3. Ground line noise between the transmitter and receiver.

All of these types of noise will be considered in this discussion.

EXTERNAL MAGNETIC EFFECTS

Changing magnetic lines of force from an adjacent AC power line which intersect the digital transmission line will induce a voltage difference between the transmitter and receiver. The induced voltage will be equal and of the same polarity on the two signal lines and return line at any point. Even though large excursions can be measured between the transmitter and receiver ground points, this has no effect on the digital transmission quality. To the transmitter and to the re-

ceiver, their respective ends of the transmission line appear normal since they have not shifted with respect to ground at that end of the line.

This has been verified experimentally by winding a transmission line around a ferrite core to form a pulse transformer secondary. When a primary winding was connected to a pulse generator (0 to 20MHz, 20V Peak) no adverse effects could be noted on a receiver output (Figure 2).

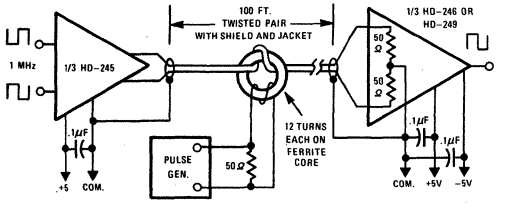


Figure 2- External Magnetic Field

The effect of a ground loop outside the magnetic circuit is only to reduce the coupled noise. For maximum immunity, the power supplies should be filtered by 0.1μF or larger capacitors to the common lines at the transmitter and receiver pins.

EXTERNAL CAPACITIVE EFFECT

The effect of capacitive coupling of AC signals from adjacent conductors is to tend to produce noise with respect to ground on both signal lines which is uniform along the length of the line. Here, a shield on the transmission line is highly effective in preventing adverse effects. The foil type shields, in addition to being less expensive, give more perfect protection than braided wire types.

The ability to reject capacitively coupled noise has also been verified experimentally as shown in Figure 3. Power supply filtering is again essential. No erroneous receiver output was noted.

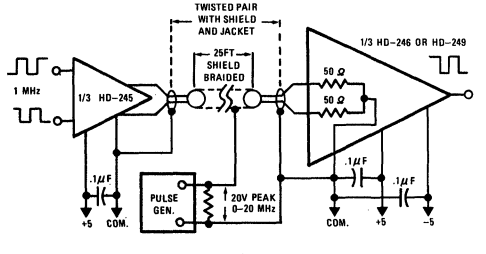


Figure 3- External Capacitive Field

CROSSTALK

It is possible to contain a number of individual twisted-pair transmission lines within a single overall shield. Perfectly balanced signals on a twisted pair will produce an unchanging magnetic and electric field which will not couple to other lines. The delay between the complementary inputs to the transmitter must be small compared with the transition times of the transmitter inputs to minimize the small current pulses during switching. The HD-245 transmitter worstcase current unbalance is guaranteed so that it is possible to enclose more than 15 twisted pairs without exceeding the common mode range of a receiver even if 14 of the pairs should switch at the same instant. Power lines, single ended signal lines, or high level twisted pair signal lines should not be enclosed in the same shield.

GROUND LINE NOISE

In systems where transmission line shields are the only connections between the transmitter and receiver power supplies, interference from noise currents on the shield will be negligible, since the only current on the shield will be signal return current and the system can withstand noise up to 2V peak. If severe ground loop currents are present, for example, if both transmitter and receiver power supply commons are connected to different points on a noisy AC power line ground, interference can be encountered. The best solution is to remove the ground loop and use DC power supplies which are well isolated from the AC line.

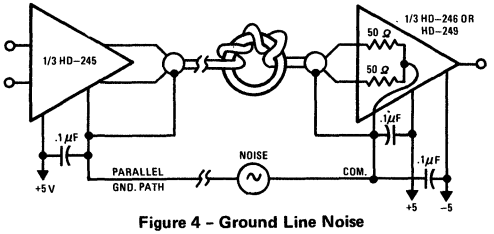


Figure 4 - Ground Line Noise

Another effective solution is to wind a portion of each transmission line around a magnetic core to form a balun transformer as shown in Figure 4. Flux produced by the signal currents and the shield return cancel one another, so the signal remains unaffected. Ground loop current produces a flux in the core so that the current is reduced by the inductance and by core losses. Thus, the coils form a low impedance to signals but a high impedance to noise.

This transmitter/receiver system is unaffected by ground differentials as long as the receiver ground is between 3V positive and 25V negative with respect to the transmitter V_{CC}. Therefore, large low frequency ground noises can be tolerated as well as large ground error signals.

Precautions should be taken to minimize ground differentials between the line termination and the HD-248 party line receiver. For best performance, the inputs of the party line receiver should remain within ±0.5V of the HD-248 ground.

OTHER TRANSMISSION SYSTEMS

A popular low speed transmission system which conforms with EIA Standard No. RS-232C is shown in Figure 5. This standard was established for low speed local digital communications.

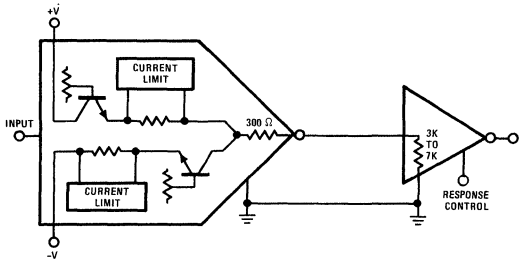


Figure 5 - EIA STD. RS-232C Data System

RS-232C specifies that the output of the transmitter swings between +6V and −6V while the receiver thresholds are between +0.8V and +2V. This is a simple system to implement, requiring only one signal line and a common ground return. Shielded or twisted transmission lines are generally not used with this system and several communications circuits can share the same ground return. A terminated transmission line is not practical with this system because it is designed to operate with an impedance of between 3KΩ and 7KΩ.

Another popular high speed transmission system is the differential voltage switching type shown in Figure 6.

First, line A is connected to +5V and current flows through the terminating resistor to line B which is connected to common. Then, the current is reversed for the next half cycle.

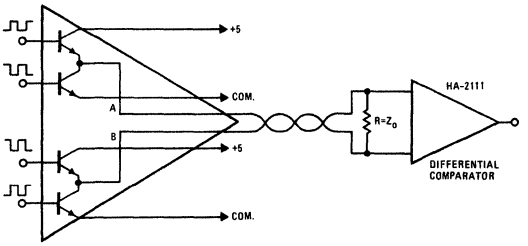


Figure 6- Differential Voltage Switching

In the absence of noise, no ground return or shield is required; however, shielding is definitely necessary in any practical system.

In an unshielded environment, the receiver must have a high common mode noise rejection, and some systems boast the ability to reject common mode noise up to ±15V. Common mode currents cannot return to ground through the terminating resistor, but must travel through the high impedance receiver input. Therefore, very little induced noise power is required to exceed the common mode voltage range of the receiver, and an unshielded line could not be used in the vicinity of AC power lines, teletypewriter lines, etc., carrying signals over 15V peak.

Also, the voltage switching type transmitter is often a source of noise. Ringing resulting from high speed low impedance switching will be present on the lines. Most transmitters have diode clamps to reduce ringing, but it still may exceed 1VRMS which would make an unshielded line a strong source of radiated RF interference.

The "totem pole" transmitter output will draw sharp current spikes from the power supply, since at the instant of switching, the formerly saturated transistor will turn off slower than the other transistor turns on, creating a power supply short circuit for a few nanoseconds. This requires very drastic power supply decoupling at the transmitter to prevent interference with other circuitry, and the transmitter will dissipate increasing amounts of power at high signal frequencies. The current spikes also often couple to the signal line creating additional differential and common mode noise. Obviously, the use of shielded transmission lines is usually a necessity in this type of system.

CONCLUSION

A comparison of noise rejection of the three types of systems, Harris' current switching type (HD-245), RS-232C voltage mode, and the differential voltage switching types, are given below for various noise sources:

1. Externally generated magnetic and capacitive coupled noise: Using shielded line, which is generally necessary for other reasons, the three system types should reject noise equally well.

2. Crosstalk between lines: In Harris' current switching system, parameters which can cause crosstalk (current unbalance) are well defined. Spikes and ringing on the lines are negligible. Operation of more than 15 twisted pair lines in a single shield without mutual interference is assured.

   Crosstalk between a few lines can be eliminated in the RS-232C system by filtering the transmitter. However, this severely limits the maximum data rate.

   In differential voltage switching type systems, caution should be taken when using more than one line pair in a single shield, because spikes and ringing will be significant and are not easily predicted.

3. Ground line noise: The current switching type and the RS-232C type systems are not as good as the differential voltage type in this respect, but the problem can be avoided by eliminating noisy ground loops as dictated by standard system design practices.

4. Self-generated noise: The current switching type system is far superior in generating lower levels of conducted and radiated RF interference. The signal swings on the line are 20 times smaller. The non-saturating current switching transmitter generates smooth ramps without overshoot or ringing. Power supply lines are free of current spikes and power drain is constant with signal frequency.

   The noise generated by the differential and the RS-232C voltage mode types can be greatly reduced by filtering if high data rates are not required.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 502

HA-909 OPERATIONAL AMPLIFIERS PERFORMANCE TAILORING

BY DON JONES

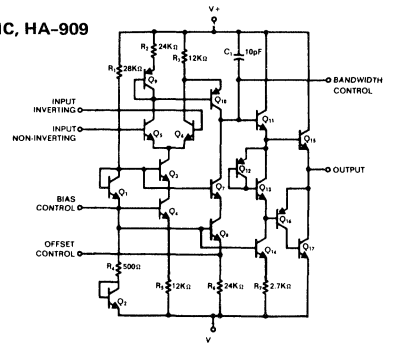
INTRODUCTION

In most applications, the HA-909 operational amplifier family will approach the theoretical "ideal" op amp requiring only connections to the power supplies and to feedback components determined from classical analog computer theory. This results from the exceptionally wide bandwidth of the HA-909 combined with internally compensated 6 dB per octave frequency rolloff and high impedance, low drift, low noise input characteristics.

Nevertheless, in the unlimited number of possible operational amplifier applications, there are those in which certain performance factors may need to be optimized. These performance factors include offset, power dissipation, bandwidth, large signal bandwidth, slew rate, transient response, and stability with reactive loads. The Harris HA-909 combines a design which minimizes the necessity for added external components with the availability of internal circuit points which allow the altering of performance characteristics.

The schematic of the HA-909 family is shown in Figure 1. The circuit nodes connected to the device pins on the HA-909 for performance tailoring are the Offset Control, the Bandwidth Control, and the Bias Control. The HA2-909, an 8-lead metal can version, has only the Bandwidth Control available.

FIGURE 1.
SCHEMATIC, HA-909



OFFSET ADJUSTMENT

In many applications, the guaranteed offset voltage of the HA-909 family is sufficiently small that no connection to the offset control pin is required. In some high precision or high gain DC amplifier applications, it may be desired to set the room temperature offset voltage to zero. Figure 2 shows the proper connection of a single 200K ohm potentiometer to accomplish this. Selected fixed resistors in a voltage divider circuit could also be used; the upper leg between the bias control pin and the offset control pin could be a fixed value of about 120K ohms and the lower leg between the offset control pin and -V could be a value usually between 50K and 100K ohms selected to yield zero offset.

Figure 3 shows offset voltage change with temperature for one unit with and without room temperature offset zeroing. These curves should not be regarded as "typical" since offset can be of either polarity and the temperature slope can be in either direction. In general, room temperature zeroing of offset voltage results in lower temperature coefficients of offset voltage.

FIGURE 2.
OFFSET ADJUSTMENT, HA-909

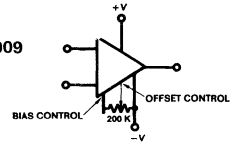
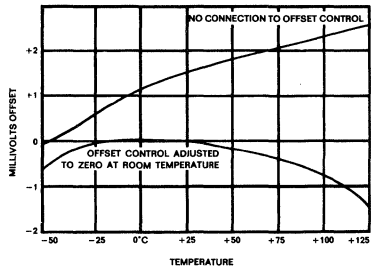


FIGURE 3.
OFFSET VOLTAGE vs. TEMPERATURE



BANDWIDTH ADJUSTMENT

A unique feature of the HA-909 family of operational amplifiers is wide bandwidth (typically 7 MHz) combined with internal compensation for 6 dB per octave rolloff. This assures stable operation at any gain with resistive loads, plus superior transient response and full power bandwidth.

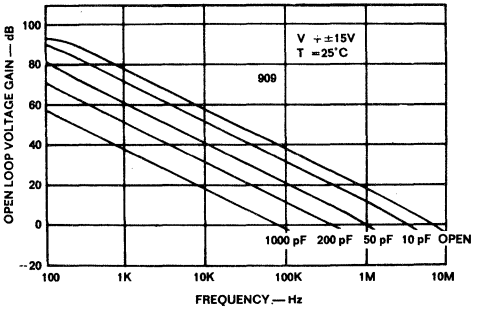
In certain instances, such as when driving reactive loads or when the amplifier is part of a servo loop, it may be desirable for stability to reduce the bandwidth while maintaining the 6 dB per octave rolloff characteristic. Also, in certain systems, it may be desirable to attenuate frequencies above a certain value or to limit transient response.

Connection of a capacitor from the bandwidth control pin to ground will move the first break point on the open loop frequency response curve to a lower frequency while retaining the 6 dB per octave rolloff (Figure 4).

The effective built in capacitance is about 10 pF, so the new bandwidth with external capacitance connected is approximately $Bw = Bwo \times \frac{10}{C+10}$; where Bwo is the bandwidth without external capacitance and C is the external capacitance in pF. Slew rate and full power bandwidth will be reduced by the same factor as the bandwidth.

The Bandwidth Control pin may also be used to limit the output swing by connecting diodes at this point to reference voltages. This pin is a high impedance point which carries the same voltage swing as the output pin offset by about +1.5 volts.

FIGURE 4.
OPEN LOOP FREQUENCY RESPONSE



FREQUENCY RESPONSE VS. CAPACITANCE FROM BANDWIDTH CONTROL PIN TO GROUND.

BIAS CONTROL ADJUSTMENT

Bias Control refers to control of internal device quiescent currents and should not be confused with the Input Bias Current parameter.

Referring to the HA-909 schematic in Figure 1, the current in all stages of the amplifier is determined by the resistor-diode string consisting of R1, Q1, R4, and Q2. The impedance at the collector of Q10 which drives the rolloff capacitor, C1, is directly proportional to the current through R4 and Q2. This current is approximately 1.0 mA at supply voltage of ±15 volts; 0.65 mA at ±10 volts; or 1.35 mA at ±20 volts. As a result, the bandwidth and slew rate measured with supplies of ±20 volts are nearly double the values measured at ±10 volts. It is possible to control bandwidth, slew rate, and to some extent open loop gain by adding or subtracting current through R4 and Q2 by connecting a resistor from the supply voltage to the Bias Control pin.

Adding bias control current by connecting a resistor between the positive supply and the Bias Control pin may be desirable to achieve maximum bandwidth or slew rate, particularly when supply voltages less than ±15 volts must be utilized. Reducing bias control current by connecting a resistor between the negative supply and the bias control pin has much the same effect as adding capacitance to the Bandwidth Control pin but may be desirable to minimize power supply current.

Figure 5 shows the change in D. C. open loop gain with supply voltage and external bias control current normalized to the gain measured at ±15 volt supplies and the Bias Control pin open.

FIGURE 5.
OPEN LOOP GAIN WITH BIAS CURRENT

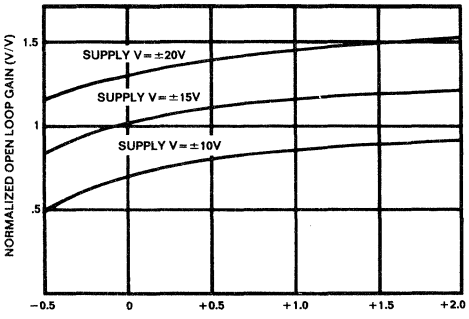


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FIGURE 6.
OTHER PARAMETER CHANGES WITH BIAS CURRENT

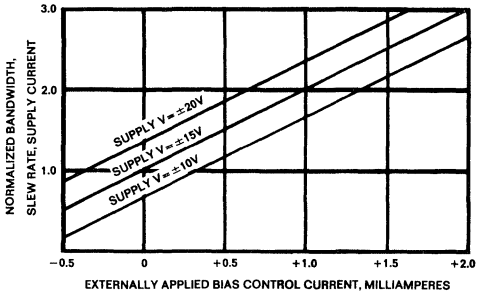
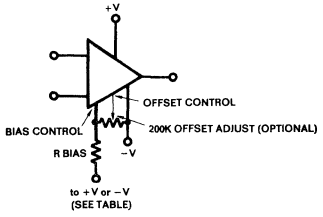


Figure 6 refers to changes in slew rate, bandwidth, large signal bandwidth for a fixed output level, and power supply current with respect to changes in supply voltage and external bias control current. These curves are normalized with respect to the parameters measured at ±15 volt supplies and the Bias Control pin open. It can be seen that these parameters can be increased to those normal at a higher supply voltage by adding bias control current; 0.35 mA added at ±10 volts brings the performance up to the normal 15 volt level and 0.35 mA added at ±15 volts brings the performance up to the normal 20 volt level.

Obviously the maximum output voltage swing cannot be increased by adding bias control current, but actually tends to decrease by about 1 volt at 2 mA bias control current. Bias control currents from 2 to 5 mA increase the parameters even more but instability at unity gain may result from reduced phase margin.

Figure 7 shows the typical external resistance required for various bias control currents at different supply voltage levels.

FIGURE 7.



BIAS RESISTOR SELECTION

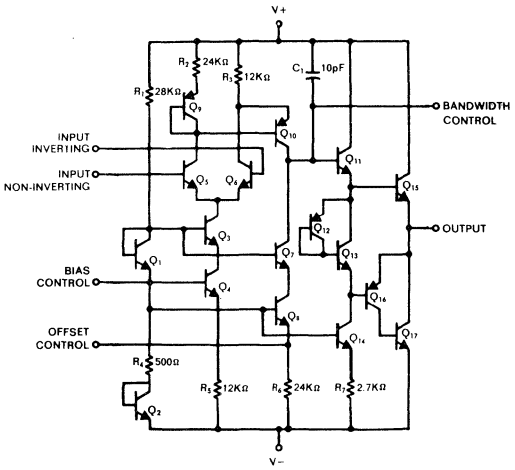
External Bias Current mA	Connect R Bias to:	R Bias In Ohms At Supply Voltage: ±10V	±15V	±20V
−0.5	−V	1.7K	2K	2.4K
+0.5	+V	39K	57K	77K
+1.0	+V	18K	28K	38K
+1.5	+V	12K	21K	27K
+2.0	+V	9K	14K	19K

CONCLUSION

For most applications, no connections are required at the Offset, Bandwidth, or Bias Control pins; they are simply terminated at an isolated solder pad on the PC Card.

The versatility provided by these control points allows the HA-909 to be used in many special applications so that a single op amp type can be used for virtually all op amp requirements in a system.

HA-909 SCHEMATIC



HARRIS SEMICONDUCTOR
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APPLICATION NOTE 505

A HIGH IMPEDANCE HYSTERSIS CIRCUIT

BY G. G. MILER

A hysteresis amplifier is often needed for Schmitt triggers, analog simulation, differential comparators, and for servomechanisms. Frequently the hysteresis amplifiers used in these circuits are required to have a high input impedance and a low input current to avoid disturbing the input signal. The threshold voltages should be independent of the signal source impedances.

The input current introduces an error in the thresholds, which is equal to the product of the input current and the source resistance. The hysteresis circuit uses positive feedback from the output to the noninverting input of the operational amplifier. Coupling between the output and the source through the input resistance of the operational amplifier can cause multiple triggering unless the differential input resistance of the operational amplifier is large compared with the source resistance. An input impedance of 100 megohms and a bias current of two nanoamperes is obtainable with modern high impedance operational amplifiers.

It is frequently necessary to limit the output swing to some convenient levels, such as standard logic levels. The output voltage of current limited devices can be clamped; however, this will create an unnecessary amount of power dissipation.

The output voltage of the circuit can also be limited by using a series resistor between the operational amplifier and a clamp. In this case, the output of the operational amplifier is allowed to swing through its full range. However, this will limit the available output current and will require additional switching time for the output to slew through its full range. On the HA-2520 or HA-2620 the output voltage can be limited by placing a clamp at the bandwidth control point. The bandwidth control point is a high impedance point, which is at the same voltage as the output.

Figure 1 shows a simple hysteresis circuit in which the output voltage is clamped at the bandwidth control point. Let the thresholds, E_T, be defined by:

$$E_T = E_{10} \pm \frac{\Delta E_1}{2} \qquad (1)$$

Where E_{10} is the input threshold offset voltage. The output voltage limits are E_0, defined by:

$$E_O = E_{00} \pm \frac{\Delta E_0}{2} \qquad (2)$$

Where E_{00} is the output offset. The total threshold offset, E_{TO} is defined as:

$$E_{TO} = E_{00} - E_{10} \qquad (3)$$

The voltage at the noninverting input, E_1, is given by:

$$E_+ = \frac{R_1}{R_1 + R_2} E_0 \qquad (4)$$

The threshold of the hysteresis circuit occurs when E_- is equal to E_+. It can be shown that:

$$\Delta E_+ = \frac{R_1}{R_1 + R_2} \Delta E_0 \qquad (5)$$

Since ΔE_I is equal to ΔE_+ it is obvious that R_1 can be found by:

$$R_1 = \frac{\Delta E_I}{\Delta E_0} (R_1 + R_2) \qquad (6)$$

$R_1 + R_2$ is chosen to be some convenient resistance.

The next step is to calculate the reference voltage, E_R. R_1 and R_2 form a voltage divider between E_R and E_0. Therefore, the reference voltage can be calculated by:

$$E_R = E_{00} - E_{TO} \left(\frac{R_1 + R_2}{R_2}\right) \qquad (7)$$

As an example, let the output swing between -0.5 and 5.5 volts. The output is diode clamped to these levels as shown in Figure 2. Let the threshold be at ±1.5 volts and let $R_1 + R_2$ be 4.4K.

$$R_1 = \frac{\Delta E_I}{\Delta E_O} (R_1 + R_2) =$$

$$\frac{3.0}{6.0} \times 4.4K = 2.2K \qquad (8)$$

Therefore:

$$R_2 = (R_1 + R_2) - R_1 =$$

$$4.4K - 2.2K = 2.2K \qquad (9)$$

The output offset is 2.5 volts and the input offset is zero. Therefore, the total offset voltage is 2.5 volts.

$$E_R = E_{OO} - E_{TO} \left(\frac{R_1 + R_2}{R_2}\right) =$$

$$2.5 - 2.5 \left(\frac{4.4K}{2.2K}\right) = 2.5 \text{ volts.} \qquad (10)$$

An HA-2620 is used because it has an extremely high input impedance. An HA-2520 could also be used if faster switching times are desired.

The hysteresis circuit triggers approximately 70 millivolts early because the output voltage begins to drop when the input is within 75 millivolts of the threshold. The maximum current through the diode clamps is only several hundred microamps and remains constant if the differential input voltage is greater than 100 millivolts. Therefore, output voltage remains constant within a few millivolts unless the input is near the threshold. The threshold voltages and the output voltages vary by only a few millivolts from one device to the next. The circuit functions properly with a variation in the threshold voltage of less than ten millivolts when the source resistance is 10 megohms.

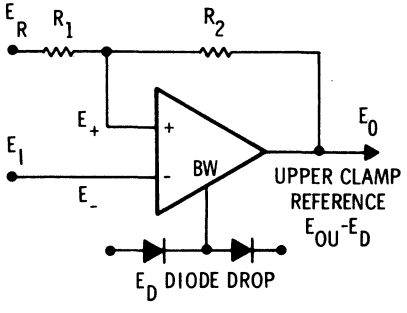

Figure 1

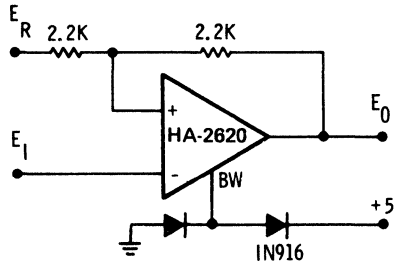

Figure 2

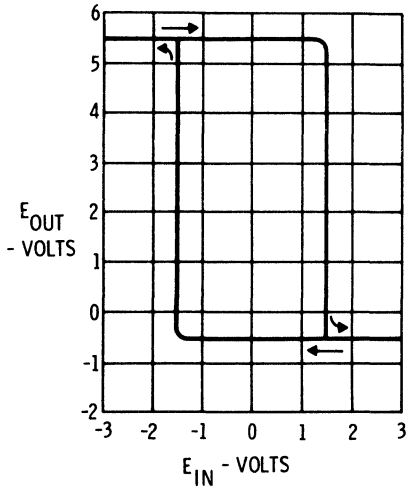

Figure 3. Output Voltage vs. Input Voltage for HA-2620 Hysteresis Amplifier

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APPLICATION NOTE 508

TEST PROCEDURES FOR OPERATIONAL AMPLIFIERS

BY G. G. MILER

The offset voltage of the amplifier under test (A.U.T.) is measured as follows:

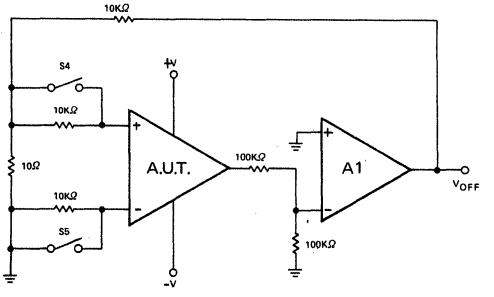
1. Set + and -V to the desired supply voltage and close S4 and S5.
2. Measure the voltage at V_{OFF}.

The offset voltage is equal to (V_{OFF}) (10^{-3}). The feedback amplifier, A1, drives the input of the A.U.T. so that the output is at ground reference, V_{OFF} is driven to 1000 times the voltage necessary to compensate for the offset voltage.

The bias current is measured as follows:

1. Measure the offset voltage, V_{OFF1}, as above.
2. Open S4 and measure V_{OFF2}.
3. The plus input current is equal to ($V_{OFF2} - V_{OFF1}$) x 10^{-7}.
4. Close S4 and open S5 and measure V_{OFF4}.
5. The minus input current is equal to ($V_{OFF4} - V_{OFF1}$) x 10^{-7}.

TEST CIRCUIT FOR MEASUREMENT OF OFFSET VOLTAGE, BIAS CURRENT, AND OFFSET CURRENT 10KΩ

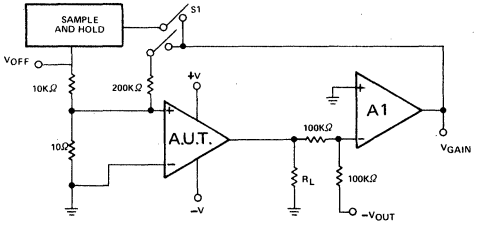


The bias current is equal to the average of the plus and minus input currents.

The input offset current is measured as follows:

1. Measure the offset voltage, V_{OFF1}, as above.
2. Open S4 and S5 and measure V_{OFF2}.
3. The offset current is equal to ($V_{OFF2} - V_{OFF1}$) x 10^{-7}.

TEST CIRCUIT FOR MEASURING OPEN LOOP VOLTAGE GAIN



The open loop voltage gain is measured as follows:

1. Set the +V and -V supply voltages to the desired value and set -V_{OUT} to ground.
2. Close S1 so that the sample and hold will null the offset voltage.
3. S1 can be opened when the circuit stabilizes. The sample and hold will maintain the voltage which nulls the offset voltage.
4. Set -V_{OUT} to the desired output voltage, -V_4 and measure V_{GAIN4}.
5. Set -V_{OUT} to another output voltage, -V5 and measure V_{GAIN5}.

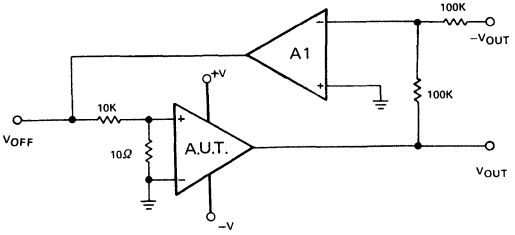
7

6. The gain is equal to

$$\left[\frac{V4 - V5}{V_{GAIN4} - V_{GAIN5}}\right] \times 20{,}000.$$

$-V_{OUT}$ can be first set to zero and then to −10 volts. This gives the gain in the plus direction. The gain in the minus direction can be determined by using zero and +10 volts. The average gain can be determined by using output voltages of −10 and +10 volts.

TEST CIRCUITS FOR MEASUREMENT OF COMMON MODE REJECTION RATIO AND POWER SUPPLY REJECTION RATIO



Common Mode Rejection Ratio:

1. Set +V to +20 VDC, -V to -10 VDC, V_{OUT} +5 VDC by applying -5 VDC to $-V_{OUT}$.
2. Measure V_{OFF2}.
3. Set +V to +10 VDC, -V to -20 VDC, V_{OUT} to -5 VDC by applying +5 VDC to $-V_{OUT}$.
4. Measure $| V_{OFF2} - V_{OFF4} |$ <1.0 VDC.

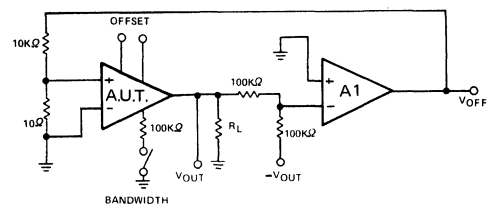
The +1.0 volt limit corresponds to a rejection ratio of 80 dB.

Power Supply Rejection Ratio:

1. Set +V to +20 VDC, -V to 15 VDC, V_{OUT} to ground by grounding $-V_{OUT}$.
2. Measure V_{OFF2}.
3. Set +V to +10 VDC.
4. Measure $| V_{OFF2} - V_{OFF4} |$ <1.0 VDC.
5. Set +V to +15 VDC, -V to -10 VDC.
6. Measure V_{OFF6}.
7. Set -V to -20 VDC.
8. Measure $| V_{OFF6} - V_{OFF8} |$ <1.0 VDC.

The ±1.0 volt limit corresponds to a rejection ratio of 80 dB.

TEST CIRCUITS FOR MEASURING OUTPUT VOLTAGE/CURRENT, POWER DISSIPATION, AND CONTINUITY CHECKS

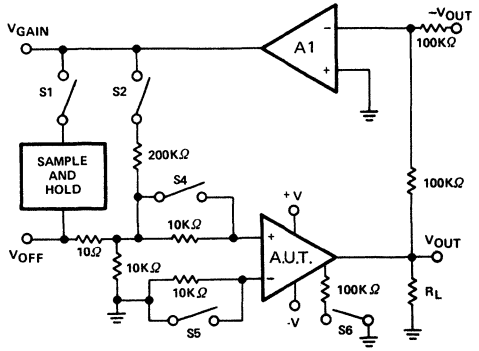


The output voltage/current is measured by connecting a load resistor, R_L, to the output of the A.U.T. The value of R_L is chosen to yield an output current which is the minimum acceptable output current at the desired output voltage. The amplifier under test is programed to a voltage greater than the desired output voltage by applying an equal but opposite polarity voltage to $=V_{OUT}$. The output voltage, V_{OUT}, is measured to see if it reaches the desired output voltage. This test is performed driving the output positive and driving the output negative.

The power dissipation is measured by driving the output voltage to zero by grounding $-V_{OUT}$ and measuring the current in one of the power supply leads.

The continuity of the bandwidth control point is checked by applying −5V to $-V_{OUT}$ and grounding the bandwidth control point through a 100K resistor. V_{OUT} should be less than one volt. There is a known relationship between the voltage at the bandwidth control point and the output voltage, V_{OUT}. This relationship depends on the device type. The continuity of the offset control points is determined by measuring the voltage at these points. These voltages will be slightly less than the positive supply voltage for the HA-2600 and the HA-2500.

SIMPLIFIED SCHEMATIC OF THE COMPLETE D.C. TEST CIRCUIT FOR OPERATIONAL AMPLIFIERS



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APPLICATION NOTE 509

A SIMPLE COMPARATOR USING THE HA-2620

BY G. G. MILER

The input current and impedance of a comparator circuit frequently loads the source and reference signals enough to cause significant errors. This problem is frequently eliminated by using a high impedance operational amplifier between the signal and the comparator. Figure 1 shows a simple circuit in which the operational amplifier is used as a comparator which is capable of driving approximately ten logic gates. The input impedance of the HA-2620 is typically 500 MΩ. The input current is typically 1 nA. The minimum output current of 15 mA is obtainable with an output swing of up to ±10 volts.

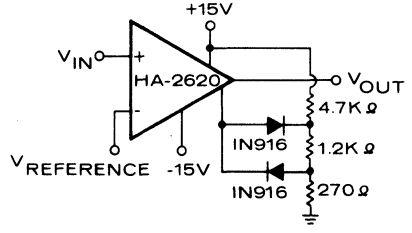

FIGURE 1 - HIGH IMPEDANCE COMPARATOR

The bandwidth control point is a very high impedance point having the same voltage as the amplifier output. The output swing can be conveniently limited by clamping the swing of the bandwidth control point. The maximum current through the clamp diodes is approximately 300 μA. The switching time is dependent on the output voltage swing and the stray capacitance at the bandwidth control point.

Figure 2 shows the waveforms for the comparator. The stray capacitance at the bandwidth control point can be reduced considerably below that of the breadboard circuit; this would improve the switching time. The switching time begins to increase more rapidly as the overdrive is reduced below 10 mV and is approximately 1μs for an overdrive of 5 mV. Dependable switching can be obtained with an overdrive as small as 1 mV. However, the switching time increases to almost 12 μs.

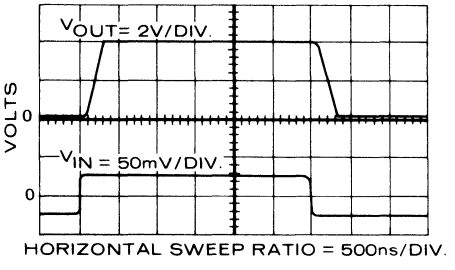

FIGURE 2 - WAVEFORMS FOR HA-2620 COMPARATOR

A common mode range of ±11 volts and a differential input range of ±12 volts makes the HA-2620 a very versatile comparator. The HA-2620 can sink or supply a minimum of 15 mA. The ability to externally clamp the output to any desired range makes the HA-2620 a very flexible comparator which is capable of driving unusual loads.

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APPLICATION NOTE 510

A SIMPLE SQUARE-TRIANGLE WAVEFORM GENERATOR

BY G. G. MILER

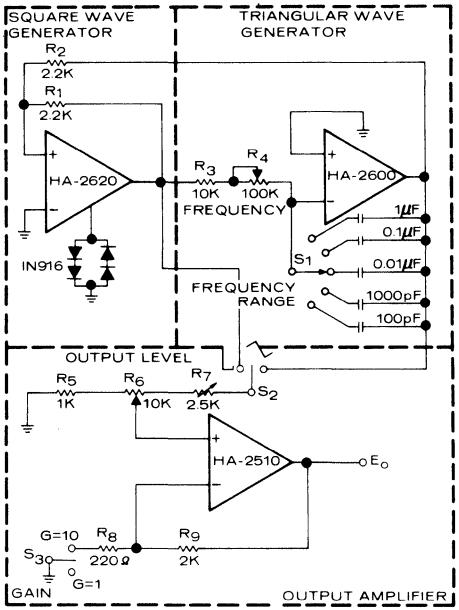

FIGURE 1

Figure 1 shows a very simple function generator which uses only three operational amplifiers. The amplitude of the square and triangular waveforms is variable from 0.2 to 20 volts peak-to-peak. The frequency range is from 2.5Hz to 250kHz. The rise time of the square wave is less than 100 nanoseconds. The slope of the triangular waveform is very linear. Very little change in frequency, amplitude, or waveform is observed with changes in supply voltages between 10 and 20 volts.

The square wave generator consists of a simple hysteresis circuit which is triggered by the triangular wave generator. The output voltage of the square wave generator is clamped to the desired level by diodes connected to the bandwidth control point. The circuit shown gives an output of two volts peak-to-peak. The ratio of the amplitude of the square wave to the triangular wave is equal to the ratio of R_1 to R_2. An HA-2620 is chosen for the comparator because it has very low input currents, high slew rate and wide bandwidth.

The triangular wave generator consists of an integrator which integrates the output of the square wave generator. The frequency of the function generator is controlled by the ramp rate of the triangular wave and the threshold levels of the hysteresis circuit. S_1 selects the integrating capacitor which changes the frequency range in decade steps. R_4 is the variable frequency control. The frequency of the function generator, f, is given by:

$$f = \frac{1}{4(R_3 + R_4)\,C}\left(\frac{R_1}{R_2}\right)$$

Better high frequency operation can be obtained by reducing the value of R_3 and R_4. Very long periods can be obtained by increasing the value of R_3, R_4 and the integrating capacitor. The HA-2600 is chosen because it produces the most accurate integration, having a typical input bias current of 1nA. The HA-2620 can be used for the integrator. It may be necessary to add some external compensation to prevent ringing if an HA-2620 is used.

The output amplifier consists of a simple non-inverting amplifier using a HA-2510. The HA-2510 is chosen for its high slew rate of 50 volts per microsecond. S_3 selects a gain of one or ten. The variable output attenuator, R_6, sets the input level to the amplifier. R_7 serves as an output level calibration control. The maximum output current should be limited to 20mA. The load impedance should not be less than 600Ω for a gain of ten and 50Ω for unity gain.

HARRIS SEMICONDUCTOR
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APPLICATION NOTE 511

HI-1080 DIGITAL TO ANALOG CONVERTER APPLICATIONS

BY DON JONES

GENERAL USES

D to A converters are useful in any system where both digital and analog signals are present. Some of the more common applications include:

1. Data processing output interface; driver for displays, plotters, etc.
2. Programmable power supply or function generator in automatic test equipment.
3. Tool interface in numerical controlled machining.
4. Interface for automatic process control to control temperature, flow rates, etc.
5. Digital communications: digital to audio interface.
6. Feedback network in A to D converters.

TERMINOLOGY

A definition of some of the terms and parameters encountered in D to A conversion will be helpful to those being introduced to the field.

Resolution: An indication of the number of possible analog output levels, usually expressed as the number of input bits that the converter will handle. For example, an eight (8) bit binary weighted converter will have $2^8 = 256$ possible output levels (including zero). This should not be confused with accuracy, which is sometimes also expressed as a number of bits.

Accuracy: A measure of the deviation of the analog output level from its predicted value under any input combination. This can be expressed as a percentage of full scale, a number of bits (N bits accuracy = $\frac{1}{2}^N$ possible error,) or a fraction of the least significant bit (if a converter with M bits resolution has 1/2 L.S.B. accuracy the possible error is $\frac{1}{2} \times \frac{1}{2^M}$). Accuracy may be of the same, higher, or lower order of magnitude as the resolution. The importance of accuracy vs. resolution depends on the application. Possible errors in individual bit weights which may be cumulative with combinations of bits; errors in the summation of individual bit weights and changes in these due to temperature variations.

Least Significant Bit (L.S.B.): The digital input bit carrying the lowest numerical weight; or the analog level shift associated with this bit, which is the smallest possible analog step.

Most Significant Bit (M.S.B.): The digital input bit carrying the highest numerical weight; or the analog level shift associated with this bit. In a binary weighted converter the M.S.B. creates a half of full scale level shift.

Settling Time: The total time measured from a digital input change to the time the analog output reaches its new value within a specified error band. It should be noted that the transition from one level to another is not always smooth; spikes and ringing may occur.

THE HI-1080 MONOLITHIC D TO A CONVERTER

The Harris Semiconductor HI-1080 is the first monolithic integrated circuit D to A converter complete with the thin film resistor ladder network on the same chip as the switching devices. Along with the advantages of small size and monolithic reliability, this allows higher speed and faster settling. Also it has the advantage over separate switches and ladder networks in that overall performance is guaranteed and there is no need to add the possible errors of separate components.

The functional diagram of the HI-1080 is shown in Figure 1. An external reference supply, usually 5 volts, is connected between the +REF and the -REF pins. The output levels will be directly proportional to the differential reference voltage. Variations of the other +5 volt and the -15 volt power supplies have negligible effect on the analog output. Either the +REF or the -REF pin may be grounded, so reference supplies of either polarity may be accomodated. The smaller value resistors between +REF and T_1 or between T_2 and T_3 may be externally shorted out, or an external trimmer substituted, for fine adjustment of the full scale output level. The positive side of the reference supply may be connected to T_2 or T_3 for a 10 volt nominal output swing, which is useful in bipolar operation.

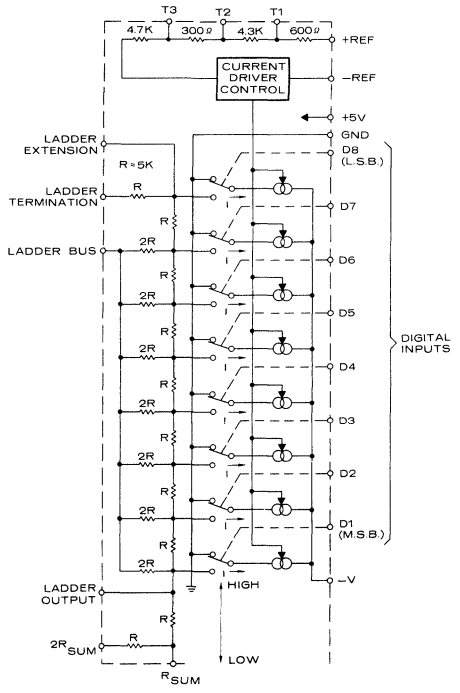


Figure 1. Functional Diagram HI-1080

The reference level is conditioned through the current driver control where the output current of each of the eight current drivers is determined.

The use of current sources to drive the ladder network has several advantages over voltage sources. Within the constant current range of the sources, the current, and hence the differential ladder output voltage, will remain constant regardless of variations in the negative supply voltage and the voltage of the ladder return bus. The ladder bus may be returned to a voltage other than ground if desired for offset or bipolar outputs without affecting its output. The digital and analog grounds can be effectively separated for noise free operation. Also switching of a current source rather than a voltage source generally is faster, creates less ringing at the output, and produces smaller power supply transients.

The digital inputs effectively switch the current source outputs either to the ladder network or to ground. The inputs are fully compatible with any standard 5 volt DTL or TTL logic circuits. A "high" input ($>$ +2 volts) switches the current source to ground; a "low" input ($<$+0.8 volts) switches the current source to the ladder, creating a more negative output voltage. This polarity convention should be kept in mind when designing with the HI-1080.

The ladder network is constructed from high stability metal film resistors deposited on the same silicon chip. Identical material is used for the resistors in the reference supply network and in the current source circuitry to achieve good temperature stability. The "R – 2R" ladder network is used rather than a weighted resistor network because identical resistors will match better in value and temperature coefficient. Extra resistors are provided at the R Sum and 2R Sum terminals which are very useful for feedback or summing with external amplifiers or comparators, since these resistors will track almost perfectly with the ladder source resistance. Provision is made at the other end of the ladder for cascading converters for higher resolution.

A block diagram is shown in Figure 2 and schematics of the block in Figures 3 – 5.

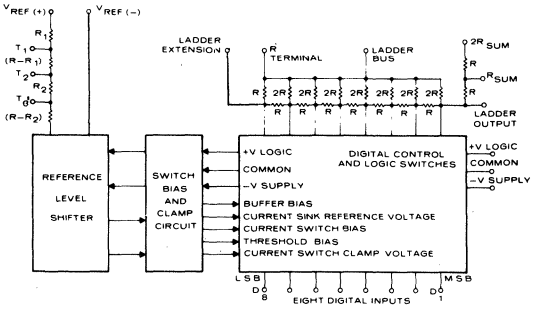


Figure 2. 8 Bit D/A Converter Block Diagram

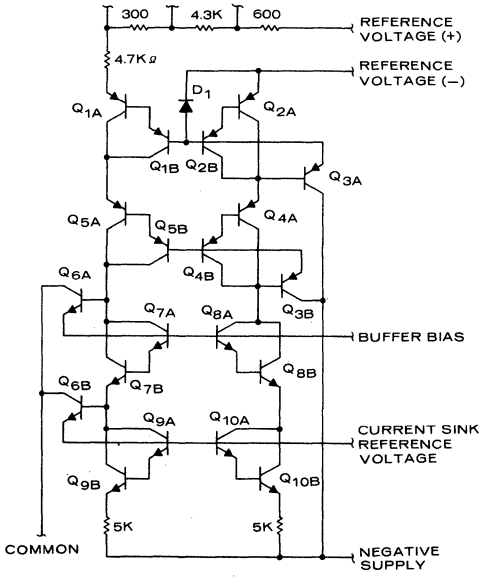


Figure 3. D/A Converter Reference Level Shifter

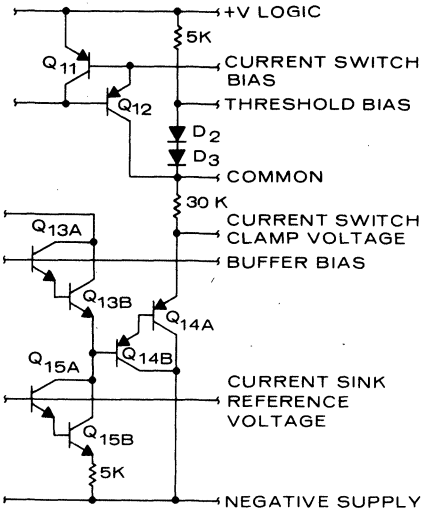


Figure 4. D/A Converter Current Switch Bias & Clamp Circuit

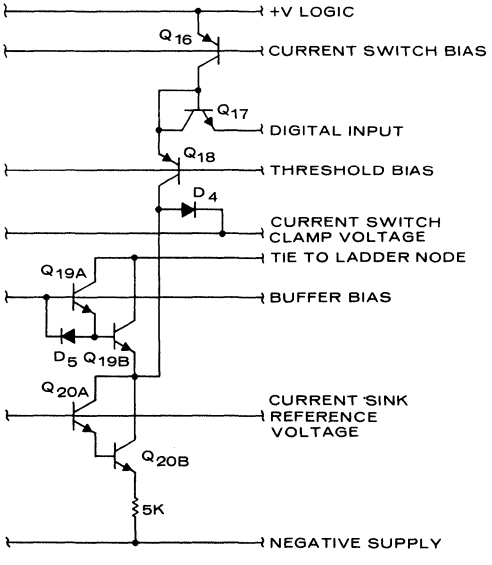
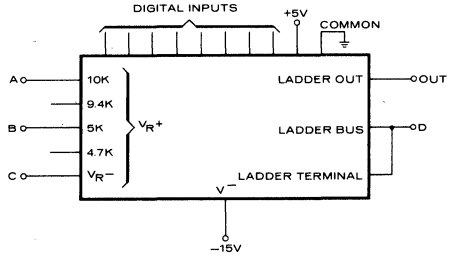


Figure 5. D/A Converter Ladder Current Switch

OPERATING MODES

Some of the possible operating modes of the HI-1080 are illustrated in Figure 6. Since both the reference supply terminals and the ladder bus terminal can be connected to any voltage within ±5 volts with respect to power supply ground, a number of output polarity modes can be achieved. In all cases the ladder output will become more negative with respect to the ladder bus as a digital input is changed from the high to the low state.



MODE	OUTPUT RANGE INPUTS: ALL HIGH TO ALL LOW	CONNECTIONS			
		A	B	C	D
UNIPOLAR ZERO REFERENCE	0 TO − [V_R+ − 1 L.S.B.]	V_R+	N.C.	GND	GND
UNIPOLAR ZERO F.S.	+ / V_R+/ TO [0 + 1 L.S.B.]	V_R+	N.C.	GND	V_R+
BIPOLAR	/V_R+/ TO [−V_R+ 1 L.S.B.]	N.C.	V_R+	GND	V_R+

Figure 6. D/A Converter Operation Modes

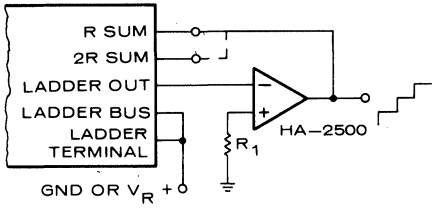
In the unipolar – zero reference mode, the ladder bus is grounded. Using negative logic convention (high = 0, low = 1), the output will increase in the negative direction with increasing input binary number. Either side of the reference supply may be grounded.

In the unipolar – zero full scale mode, the ladder bus is connected to the positive reference voltage, so the output will be always positive with respect to the reference ground. Now, using positive logic convention (low = 0, high = 1), the output will increase in the positive direction with increasing binary number. It may be necessary to connect V_R+ to a lower tap in series with a potentiometer to adjust the zero level.

The bipolar mode connection is similar to the previous mode except the V_R+ is connected to T_2 (or T_3 through a pot), so that the full scale excursion is now 10 volts. With all inputs low, the output will be most negative (about -4.96V). With only the M.S.B. high, the output will be zero volts. With all inputs high, the output will be at V_R+.

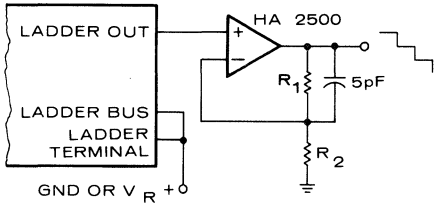
AMPLIFIER CONNECTIONS

Figure 7 illustrates connections from the converter to an operational amplifier. The inverting connection uses the summing registers provided on the chip for amplifier feedback. Since the ladder impedance is nominally 5K ohms, connection of the output to R Sum will result in a gain of -1. Connection to 2_R Sum will result in a gain of -2. Any of the operating modes discussed previously may be used.



FULL SCALE OUTPUT	OUTPUT FEEDBACK CONNECTED TO	R_1
+4.98V	R_{SUM}	2.5K
+9.96V	$2R_{SUM}$	3.3K

INVERTING OUTPUT
(MORE POSITIVE WITH INCREASING COMPLEMENT OF INPUT NUMBER)



OUTPUT RANGE: SAME AS SHOWN ON 'OPERATING MODE' CHART

MULTIPLIED BY $\frac{R2}{R1 + R2}$

NON-INVERTING OUTPUT
(MORE NEGATIVE WITH INCREASING COMPLEMENT OF INPUT NUMBER)

Figure 7. Buffer Amplifier Connection

For a noninverting output the operational amplifier is wired in the conventional manner. The R Sum or 2R Sum resistor could be used to sum an external analog signal of opposite polarity at the amplifier input.

The Harris Semiconductor HA-2500 operational amplifier is recommended for high speed applications since its slew rate of 25 volts per microsecond is sufficient to follow the converter output steps very closely. For more moderate speed applications, the Harris Semiconductor HA-2600 operational amplifier is recommended for better offset drift while retaining a minimum slew rate of 4 volts per microsecond. Booster stages may be added to the amplifier outputs to drive any required load.

CASCADED D TO A CONVERTERS

Two HI-1080 units may be cascaded to achieve resolutions from 9 to 15 bits, using the ladder extension terminals, as illustrated in Figure 8. Note that input D8 of the higher significant bit unit is not used. This is necessary in order to join the two ladders correctly.

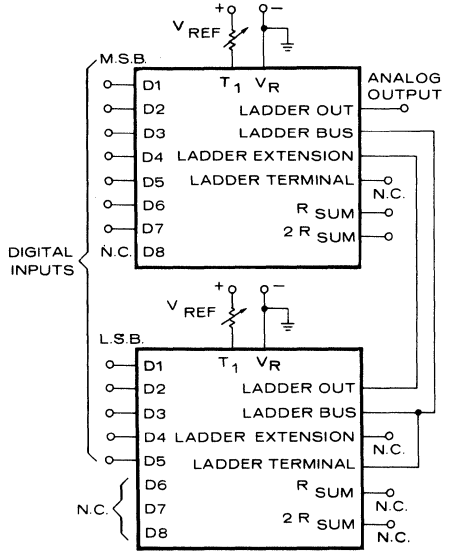


Figure 8. Cascaded Units for 12 Bit Resolution

A person might ask, "Why would anyone want a 12 bit converter with only 8-1/2 bit accuracy?" The answer is that most applications require accuracy expressed as a percentage of actual output rather than as a percentage of full scale output. One feature of the R − 2R ladder network is that errors in terms of millivolt deviation from the predicted output tend to become smaller as the lesser significant bits only are exercised. So for the 12 bit converter shown, with outputs between 1.25 and 5 volts the errors may be on the order of ±10 millivolts; but for outputs between 0 and 20 millivolts the errors will tend to be less than 0.7 millivolts.

A TO D CONVERTER; UP-DOWN COUNTER TYPE

A high speed D to A converter can be used as the heart of several very useful types of A to D converters. The up-down counter, or servo type converter is most efficient in monitoring one analog signal continuously, rather than monitoring multiplexed analog signals.

The converter works basically by balancing the input analog signal with the D to A output, adjusting the D to A by running a digital counter up or down as required to balance the signal. When the two analog signals balance, the counter state represents the digital equivalent of the input signal.

In the example shown in Figure 9, the two analog signals are fed differentially into an op-amp. For a positive input signal, the D to A could be run in the positive output mode, or in the negative output mode by summing the two signals at the inverting amplifier input. The amplifier gain should be set at 2 or greater to allow less critical thresholds for the comparators.

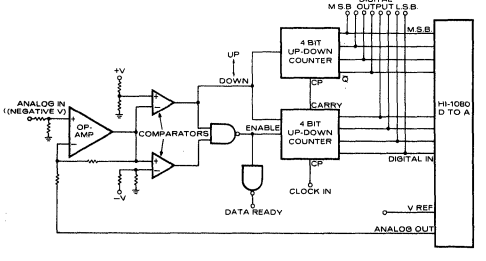


Figure 9. "Up-Down Counter" Type A to D Converter

The two comparator thresholds are set up by voltage dividers to correspond to unbalances of approximately ±1/2 L.S.B. When the analog signals are balanced within this range, the comparator outputs are both high, which stops the counters and gives a Data Ready signal to indicate that the digital outputs are correct.

If the analog signals are unbalanced by more than ±1/2 L.S.B., the counter is enabled and driven in the up or down direction depending on the polarity of the unbalance.

If the D to A converter is operated in the negative output mode, the digital outputs will follow negative logic convention.

If the analog input signal varies by less than 1 L.S.B. per clock period, the converter will continuously track the signal.

The Data Ready signal could be useful in adaptive systems for most efficient data transfer, since that signal changes state only when there is a significant change in the analog input. When monitoring a slowly varying input, it would be necessary to read-out the digital output only after a change has taken place. The Data Ready signal could trigger a flip-flop to flag this condition and the flip-flop would be reset after read-out.

The main disadvantage of the up-down counter converter is the time required to initially acquire a signal, which in an 8 bit system, could be up to 256 clock periods. The input signal usually must be filtered so that its rate of change does not exceed the tracking rate of the converter.

A TO D CONVERTER, SUCCESSIVE APPROXIMATION TYPE

Suppose you were asked to guess a secret number between 0 and 15 by asking the least number of questions answerable by yes or no. One of the most efficient ways might work as follows:

"Is it 8 or greater?"

"Yes"

"Is it 12 or greater?"

"No"

"Is it 10 or greater?"

"Yes"

"Is it 11?"

"No"

If you had jotted down a "1" for each "yes" and a "0" for each "no", you would have 1010, which of course, is the binary notation for ten. So it is possible to find one number out of 16 with 4 questions. Likewise 8 questions would be required to find a number between 0 and 255. Obviously this technique is usually much quicker than saying, "Is it zero?", "Is it one?", etc., or guessing numbers at random.

The successive approximation converter shown in Figure 10 uses the same technique to find which proportional number between 0 and 255 best approximates the input analog voltage.

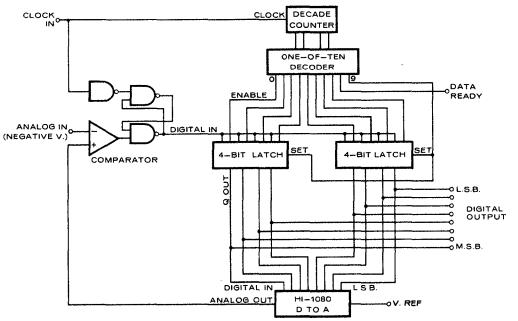


Figure 10. Successive Approximation Type A to D Converter

This is accomplished in 8 clock cycles – two additional cycles are used in this design to hold the data and to clear the registers, but this could be done during the eighth cycle, if necessary. The measurement starts with all zeros programmed into the D to A and the decade counter set to zero. The decoder enables the first of eight latches and the clock pulse sets a flip-flop composed of two cross-coupled gates setting a "1" in the first latch, so the D to A has a 10,000,000 input. The D to A consequently produces a half-scale output which goes to one side of the comparator. The comparator now effectly asks the question "Is the input greater than half-scale?". If the answer is "yes", the comparator output is high and the flip-flop remains set. If the answer is "no" the comparator resets the flip-flop during the second half cycle of the clock, resetting the first latch to zero.

On the second clock cycle the decoder enables the second latch while the last state of the first latch remains stored in it and remains as the D to A, M.S.B. input. In a similar manner, the state of the second M.S.B. is decided and the decoder moves on to the third. After the eighth clock cycle the conversion is complete, which is signaled by the Data Ready line on the ninth cycle. At the tenth cycle all latches are reset to be ready for the next conversion.

In practice, the delay of the clock pulse through the counter and decoder should be less than the delay through the three gates for proper timing.

Polarities shown are correct for the D to A connected in the negative output mode, and the digital output will be correct in negative logic. A positive analog input can be handled by summing with the D to A output at one comparator input, or by operating the D to A in the positive output mode and shifting the digital polarities as necessary.

It is necessary in any successive approximation converter for the analog input to remain constant during the conversion.

In multiplexed systems this is usually accomplished with a sample-and-hold circuit in the analog line.

It can be seen that the successive approximation type will give the correct output in eight clock cycles while the up-down counter type could take up to 255 cycles to acquire a signal. Once acquired, the up-down counter can indicate a change in a slowly varying signal within one clock cycle, while the successive approximation type must step through another eight cycles. The choice really depends on the type of signals to be monitored.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 512

COUNTER TYPE A TO D CONVERTER

BY DON JONES

INTRODUCTION

This paper describes circuit details for a full temperature range eight-bit A to D converter employing a unidirectional digital counter and a D to A converter. As shown in the simplified diagram in Figure 1, circuit operation is quite simple. A multiple stage counter circuit is driven from a clock and the counter output drives a D to A converter producing a staircase voltage ramp. When the D to A output voltage equals the analog input voltage, the comparator changes state, and at that instant, the counter state represents the digital equivalent of the analog input.

The heart of this circuit is the HI-1080 Eight-Bit D to A Converter, which is a monolithic integrated circuit containing both the current switches and the R-2R ladder network. This features good speed and accuracy over $-55^{o}C$ to $+125^{o}C$ temperature range. The HI-1080 D to A converter is also very effective in up-down counter and successive approximation type A to D converters, which are described in other application notes.

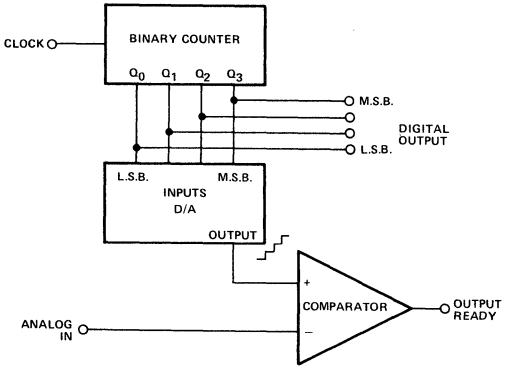


Figure 1. Simplified Diagram, Counter Type A/D

COUNTER vs. SUCCESSIVE APPROXIMATION TYPE CONVERTERS

The most popular A to D converter employing a D to A circuit is the successive approximation type. This type is useful for high speed conversion, since it requires only N clock cycles for an N-bit conversion, while the counter type requires up to 2^N cycles. One disadvantage, where many conversions per second are not needed, is that a sample-and-hold circuit is nearly always required in the analog signal path. The sample-and-hold circuit is an additional error source which is difficult to control over a wide temperature range. The counter type converter does not require a sample-and-hold circuit, since its output is a parallel digital number taken at the instant that the D to A and input signals are equal, although filtering of the input signal may be desirable in some applications. The counter type converter illustrated here can perform 1,000 conversions per second, which is adequate for many applications.

CIRCUIT DETAILS

The complete circuit schematic is shown in Figure 2 and typical waveforms are illustrated in Figure 3. The digital circuits shown are 9300 types, but comparable circuits from other TTL families will work equally well if any functional differences are taken into account.

Since the D to A converter normally has a negative output level, a positive input signal is compared by resistive summation at one comparator input, using the summing resistor internal to the D to A which closely matches the D to A equivalent output resistance.

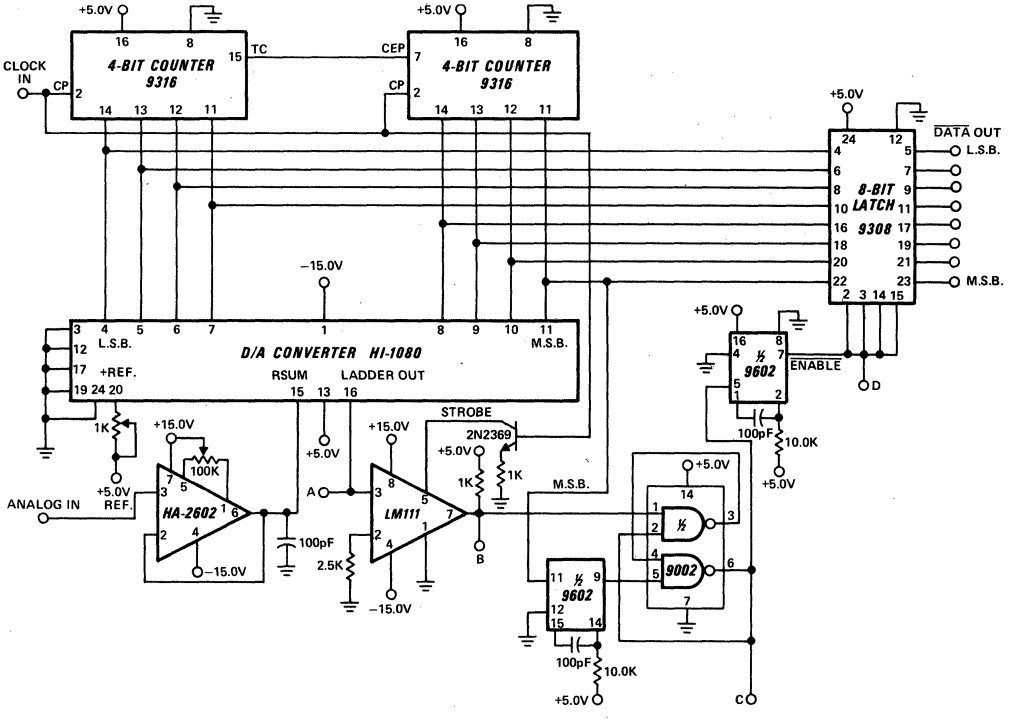


Figure 2. Complete A/D Schematic

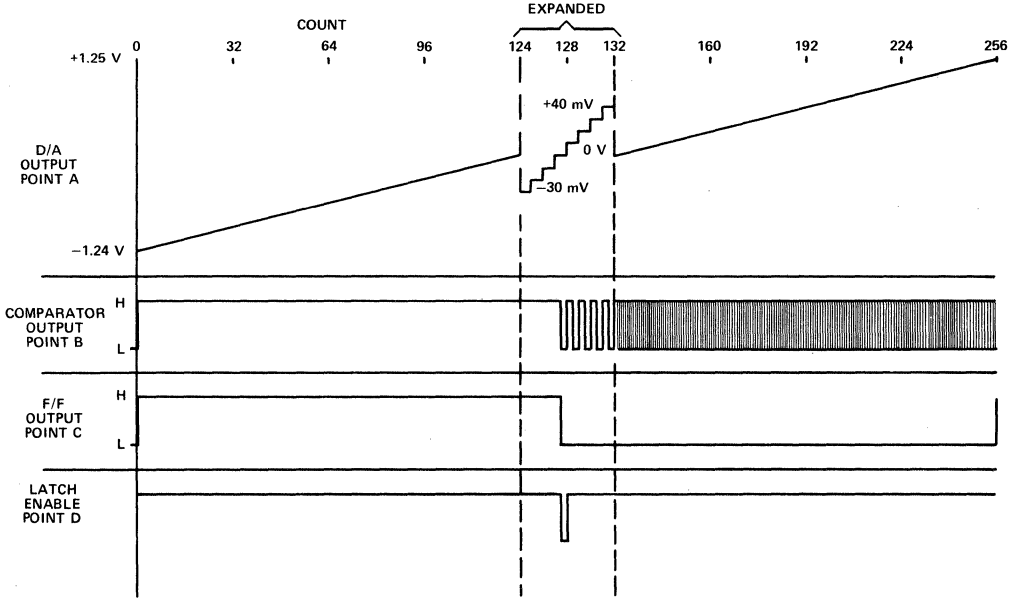


Figure 3. Waveforms with +2.50 Volts Analog Input

The comparator is strobed with the clock to prevent any D to A switching spikes from prematurely triggering the comparator. The strobing necessitates the use of the set-reset flip-flop formed by the cross-coupled gates so that the latch receives only one enable pulse per conversion cycle.

Note that the data output from the latch is the complement of the digital value, due to the polarity conventions of the D to A.

CIRCUIT ADJUSTMENT

For 0 to +5 volt input range the input op-amp is first zeroed in the conventional manner. Then +2.500 volts is applied to the input, and the pot between the reference supply and the D to A is adjusted so that the M.S.B. just trips in at this level. The full scale input will then be 1 L.S.B. below +5.000 volts which is +4.980 volts.

For 0 to +10 volts input range, connect the op-amp output to the 2R sum terminal on the D to A.

For 0 to −5 volt range, connect the op-amp output to the negative input of the comparator through a 5K ohm resistor.

For −5 volt to +5 volt bipolar operation, connect the ladder bus terminal on the D to A to the +5 volt reference, and connect the reference through the potentiometer to the T3 terminal of the D to A.

Virtually any other input range is possible by changing the op-amp gain or polarity, or adjusting the reference potentiometer. Zero shift may be accomplished by offsetting the ladder bus, or summing voltages at the op-amp or comparator inputs.

CIRCUIT PERFORMANCE

Accuracy is affected primarily by the D to A accuracy, and to a lesser degree by offsets in the input op-amp and the comparator. This circuit proved to be accurate within +½ L.S.B. at room temperature, and ±1 L.S.B. from −55°C to +125°C. This accuracy was maintained at clock rates up to 330 KHz. Clock rates up to 1 MHz could be used with about 1 additional L.S.B. of inaccuracy.

CIRCUIT VARIATIONS

Using the illustrated circuit as a starting point, many modifications to the digital circuitry are possible to suit the application.

For convert-on-command operation, the circuitry beyond the comparator, including the latch could be eliminated and the comparator output used to gate off the clock signal. The counters will hold their value until a command to convert again is issued by resetting the counters to zero.

For continuous conversion, a reduction in average (but not maximum) conversion time can be made by resetting the counters immediately after data is entered in the latches.

Another possible improvement in conversion time can be acheived by running the clock at a variable rate - fast while the D to A output is far from the input level and slower when the comparator is about ready to trip. One possibility is to use a VCO as the clock, controlled in frequency by an op-amp with inputs wired across the comparator inputs. Another possibility would be to use a fixed 5 MHz clock and insert a ÷16 counter in series with the clock line when the D to A and input voltages are nearly equal. This could be controlled by a second comparator with the trip point offset from that of the main comparator.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

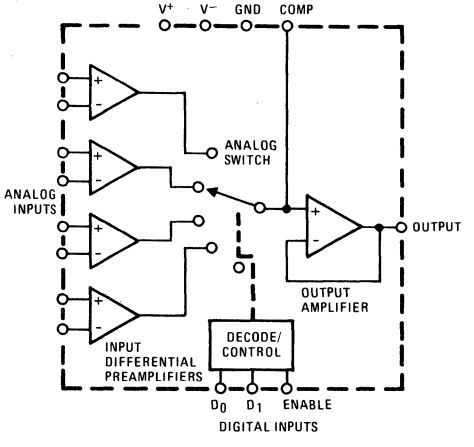
APPLICATION NOTE 514

THE HA-2400 PRAM™ FOUR CHANNEL OPERATIONAL AMPLIFIER

BY DON JONES

INTRODUCTION

Harris Semiconductor has announced a new linear device, the HA-2400/HA-2405 Four Channel Operational Amplifier. This combines the functions of an analog switch and a high performance operational amplifier, and makes practical a large number of new linear circuit applications.



A functional diagram of the HA-2400 is shown above. There are four preamplifier sections, one of which is selected through the DTL/TTL compatible inputs and connected to the output amplifier. The selected analog input terminals and the output terminal form a high performance operational amplifier.

In actuality, the circuit consists of four conventional op-amp input circuits connected in parallel to a conventional op-amp output circuit. The decode/control circuitry furnishes operating current only to the selected input section.

CIRCUIT CONNECTIONS

These inputs control the selection of the amplifier input channels in accordance with the truth table below:

D_0	D_1	ENABLE	CHANNEL 1	CHANNEL 2	CHANNEL 3	CHANNEL 4
L	L	H	ON	OFF	OFF	OFF
H	L	H	OFF	ON	OFF	OFF
L	H	H	OFF	OFF	ON	OFF
H	H	H	OFF	OFF	OFF	ON
L or H	L or H	L	OFF	OFF	OFF	OFF

$0V \leq L \leq +0.8V$ $\quad +2.0V \geq H \geq +5.0V$

The digital inputs can be driven with any DTL or TTL circuit which uses a standard +5.0V supply.

COMPENSATION

Frequency compensation for closed loop stability is recommended for closed loop gains less than 10. This is accomplished by connection of a single external capacitor from Pin 12 to A.C. ground (the V+ supply is recommended). The following table shows the minimum suggested compensation for various closed loop gains, with the resultant bandwidth and slew rate. Obviously, when the four channels are connected with different feedback networks, the channel with the lowest closed loop gain will govern the required compensation.

GAIN, VOLTS/VOLT		C_{COMP}	BANDWIDTH (TYPICAL)	SLEW RATE (TYPICAL)
NON-INVERTING	INVERTING	pF	(-3dB), MHz	VOLTS/μs
1	-	15	8.0	15
2	1	7	8.0	20
3	2	4	8.0	22
5	4	3	6.0	25
8	7	2	5.0	30
>10	>9	0	40÷GAIN	50

Compensation capacitors of greater value can be used to obtain lower bandwidth, greater

7

phase margin, and reduced overshoot, at the expense of proportionately reduced slew rate.

External lead-lag networks could also be used to optimize bandwidth and/or slew rate at a particular gain.

APPLICATIONS

Any circuit function which can be constructed using a conventional operational amplifier can also be constructed using any channel of the HA-2400. Similar or different networks can be wired from the output to each channel input pair. The device can therefore be used to select and condition different input signals, or to select between different op-amp functions to be performed on a single input signal.

To wire a particular op-amp function to a channel, simply connect the appropriate network between the two inputs for that channel and the common output in the same manner as in wiring a conventional op-amp. It is often possible to design with fewer external components than would be required in wiring four separate op-amps (see Application Numbers 2 and 3 on the following pages). It should be remembered that the networks for unselected channels may still constitute a load at the amplifier output and the signal input, as if the unselected input terminals were disconnected from the network.

If offset adjustment is required, it can generally be accomplished by resistive summation at either of the inputs for each channel (see Application Number 8).

The analog input terminals of the OFF channels draw the same bias current as the ON inputs. The maximum differential input voltage of these terminals must be observed and their voltage levels must never exceed the supply voltages.

When the Enable input is held low, all four input channels are disconnected from the output. When this occurs, the output voltage will generally slowly drift towards the negative supply. If a zero volt output condition is required, one channel should be wired as a voltage follower with its positive input grounded.

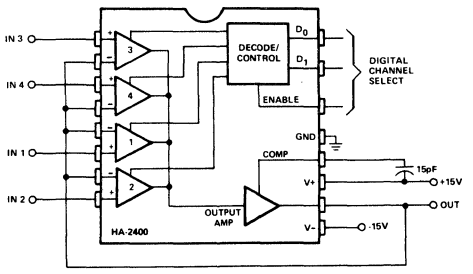
The amplifier output impedance remains low, even when the inputs are disabled; so it is not generally practical to wire the outputs of two or more devices directly together. The compensation pins of two devices, however, could be wired together to produce a switch with one output and more than four input channels.

The voltage at the compensation pin is about 0.7V more positive than the output signal, but has a very high source impedance. Maximum current from this pin is about 300μA, which makes it a convenient point for limiting the output swing through clamping diodes and divider networks (see Application Number 13).

Even if the application only requires a single channel to be switched on and off, it is often more economical to use the HA-2400, rather than a separate analog switch and high performance op-amp. Unused analog channel inputs should be grounded. Unused digital inputs may be wired to ground for a permanent "low" input, or either left open or wired to +5.0V for a permanent "high" input.

Illustrated on the following pages are a few of the thousands of possible applications for the Four Channel Operational Amplifier. These will give the reader a general impression of how the units can be connected; and probably will help generate many other ideas for applications. Also included are some "challenges" for the reader to modify the illustrated designs to perform different functions.

APPLICATION NO. 1



ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

This circuit is used for analog signal selection or time division multiplexing. As shown, the feedback signal places the selected amplifier channel in a voltage follower (non-inverting unity gain) configuration, and provides very high input impedance and low output impedance. The single package replaces four input buffer amplifiers, four analog switches with decoding, and one output buffer amplifier.

For low level input signals, gain can be added to one or more channels by connecting the (–) inputs to a voltage divider between output and ground. Bandwidth is approximately 8 MHz, and the output will slew from one level to another at about 15.0V per microsecond.

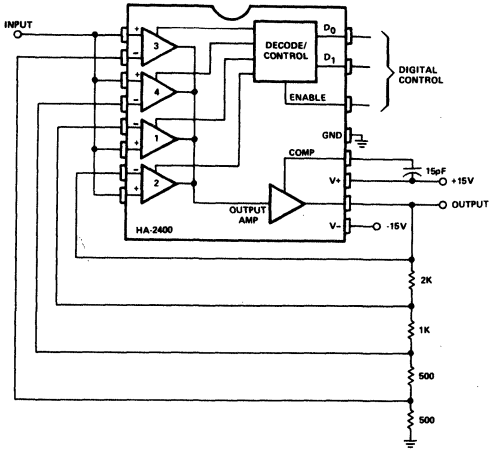
Expansion to multiplex 5 to 12 channels can be accomplished by connecting the compensation pins of two or three devices together, and using the output of only one of the devices. The Enable input on the unselected devices must be low.

Expansion to 16 or more channels is accomplished in a straightforward manner by connecting outputs of 4 four-channel multiplexers to the inputs of another four-channel multiplexer.

Differential signals can be handled by two identical multiplexers addressed in parallel.

Inverting amplifier configurations can also be used, but the feedback resistors may cause crosstalk from the output to unselected inputs.

APPLICATION NO. 2



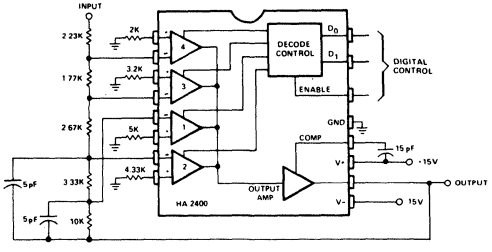
AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN

This is a non-inverting amplifier configuration with feedback resistors chosen to produce a gain of 0, 1, 2, 4, or 8 depending on the Digital Control inputs.

Comparators at the output could be used for automatic gain selection for auto-ranging meters, etc.

CHALLENGE: Design a circuit using only two HA-2400's which can be programmed to any of 16 different gains.

APPLICATION NO. 3

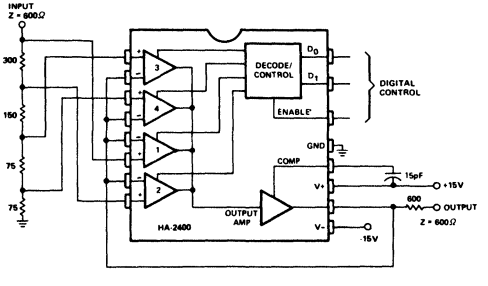


AMPLIFIER, INVERTING PROGRAMMABLE GAIN

The circuit above can be programmed for a gain of 0, –1, –2, –4 or –8.

This could also have been accomplished with one input resistor and one feedback resistor per channel in the conventional manner, but this would require eight resistors rather than five.

APPLICATION NO. 4

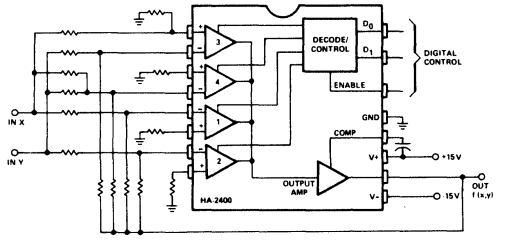


ATTENUATOR PROGRAMMABLE

This circuit performs the function of dividing the input signal by a selected constant (1, 2, 4, 8, or ∞ as illustrated). To multiply by a selected constant, see circuit No. 2. While T, π, or L sections could be used in the input attenuator, this is not necessary since the amplifier loading is negligible and a constant input impedance is maintained. The circuit is thus much simpler and more accurate than the usual method of constructing a constant impedance ladder and switching sections in and out with analog switches.

Two identical circuits may be used to attenuate a balanced line.

APPLICATION NO. 5

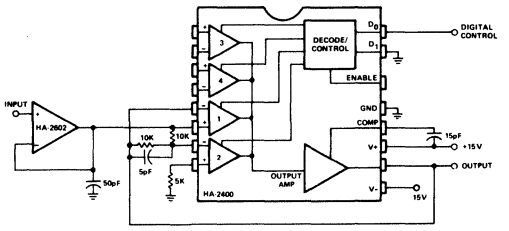


ADDER/SUBTRACTOR PROGRAMMABLE FUNCTION

The circuit shown above can be programmed to give the output functions $-K_1X$, $-K_2Y$, $-(K_3X + K_4Y)$, or $K_5X - K_6Y$. Obviously, many other functions of one or more variables can be constructed, including combinations with analog multiplier or logarithmic modules.

This device opens up many new design approaches in digitally controlled analog computation or signal manipulation.

APPLICATION NO. 6

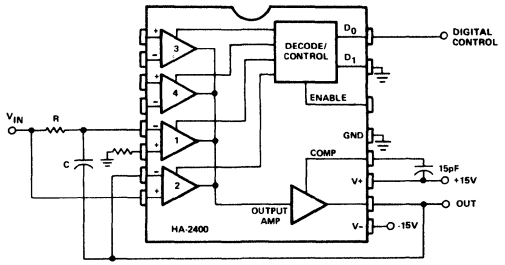


PHASE SELECTOR/PHASE DETECTOR/ SYNCHRONOUS RECTIFIER/BALANCED MODULATOR

This circuit passes the input signal at unity gain, either unchanged, or inverted depending on the Digital Control input. A buffered input is shown, since low source impedance is essential. Gain can be added by modifications to the feedback networks. Signals up to 100 kHz can be handled with 20.0V peak-to-peak output. The circuit becomes a phase detector by driving the Digital Control input with a reference phase at the same frequency as the input signal, the average D.C. output being proportional to the phase difference, with zero volts at $\pm 90^{o}$. By connecting the output to a comparator, which in turn drives the Digital Control, a synchronous full-wave rectifier is formed.

With a low frequency input signal and a high frequency digital control signal, a balanced (surpressed carrier) modulator is formed.

APPLICATION NO. 7

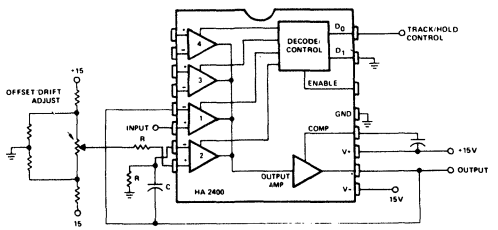


INTEGRATOR/RAMP GENERATOR WITH INITIAL CONDITION RESET

It is difficult in practice to set the initial conditions accurately in an integrator. This usually requires wiring contacts of a mechanical relay across the capacitor - - leakage currents of solid state switches produce integration inaccuracy. The scheme shown above eliminates these reliability and accuracy problems.

Channel 1 is wired as a conventional integrator, Channel 2 as a voltage follower. When Channel 2 is switched on, the output will follow V_{IN}, and C will discharge to maintain zero volts across it. When Channel 1 is then switched on the output will initially be at the instantaneous value of V_{IN}, and then will commence integrating towards the opposite polarity. This circuit is particularly suitable for timing ramp generation using a fixed D.C. input. Many variations are possible, such as programmable time constant integrators.

APPLICATION NO. 8



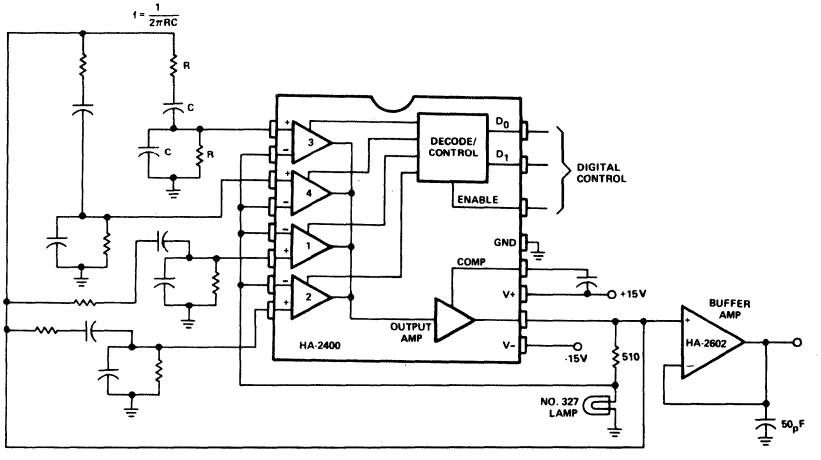
TRACK AND HOLD/SAMPLE AND HOLD

Channel 1 is wired as a voltage follower and

is turned on during the track/sample time. If the product of R x C is sufficiently short compared to the period of maximum output frequency, or sample time, C will charge to the output level. Channel 2 is an integrator with zero input signal. When Channel 2 is then turned on, the output will remain at the voltage across C.

An even simpler circuit can be made by wiring one channel as an amplifier, choosing the compensation capacitor to yield the minimum required bandwidth or slew rate. When the Enable input is pulled low, the output will tend to remain at its last level, because of the charge remaining on the compensating capacitor.

APPLICATION NO. 9

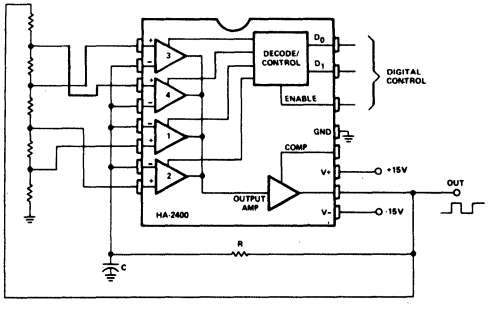


SINE WAVE OSCILLATOR PROGRAMMABLE FREQUENCY

Any oscillator which can be constructed using an op-amp, such as the twin-T, phase shift, crystal controlled types, etc. can be made programmable by using the HA-2400. Illustrated above is a Wien Bridge type, which is very popular for signal generators, since it is easily tunable over a wide frequency range, and has a very low distortion sine wave output. The frequency determining networks can be designed from about 10Hz to greater than 1MHz. Output level is about 6.0V RMS. By substituting a programmable attenuator (Circuit No. 4) for the Buffer Amplifier, a very versatile sine wave source for automatic testing, etc. can be constructed.

CHALLENGE: A high Q, narrow band filter can be made by feeding back greater than 1/3 of the output to the negative input. Design a circuit using the HA-2400 and an RC network which can be programmed either to generate or to detect an audio tone of the same frequency. Such a circuit would be quite useful for data communications.

APPLICATION NO. 10



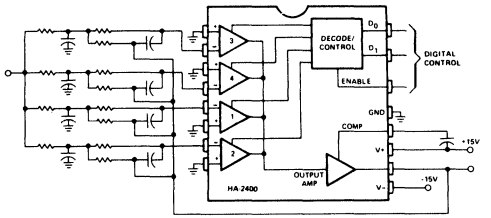
MULTIVIBRATOR, FREE RUNNING, PROGRAMMABLE FREQUENCY

This is the simplest of any programmable oscillator circuit, since only one stable timing capacitor is required. The output square wave is about 25.0V peak-to-peak and has

rise and fall times of about 0.5 μs. If a programmable attenuator circuit (No. 4) is placed between the output and the divider network, 16 frequencies can be produced with two HA-2400's and still only one timing capacitor.

A precision programmable square-triangle generator can also be constructed by adapting circuit described in Harris Application Note 507 to the HA-2400.

APPLICATION NO. 11



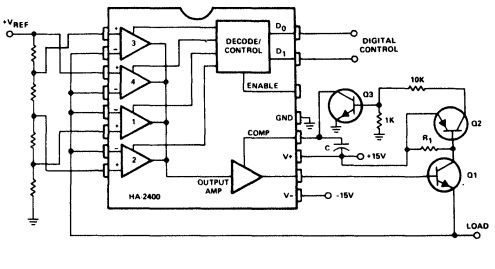
ACTIVE FILTER PROGRAMMABLE

Shown above is a second order low pass filter with programmable cutoff frequency. This circuit should be driven from a low source impedance since there are paths from the output to the input through the unselected networks.

Virtually any filter function which can be constructed with a conventional op-amp can be made programmable with the HA-2400.

A useful variation would be to wire one channel as a unity gain amplifier, so that one could select the unfiltered signal, or the same signal filtered in various manners. These could be cascaded to provide a wide variety of programmable filter functions.

APPLICATION NO. 12

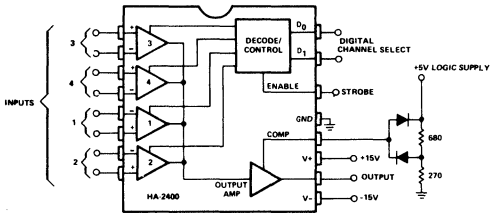


POWER SUPPLY PROGRAMMABLE

Many systems require one or more relatively low current voltage sources which can be programmed to a few predetermined levels. It is no longer necessary to purchase a programmable power supply with far more capability than needed. The circuit shown above produces positive output levels, but could be modified for negative or bipolar outputs. Q1 is the series regulator transistor, selected for the required current and power capability. R1, Q2 and Q3 form an optional short circuit protection circuit, with R1 chosen to drop about 0.7V at the maximum output current. The compensation capacitor, C. should be chosen to keep the overshoot, when switching, to an acceptable level.

CHALLENGE: Design a supply using only two HA-2400's which can be programmed to 16 binary weighted (or 10 BCD weighted) output levels.

APPLICATION NO. 13



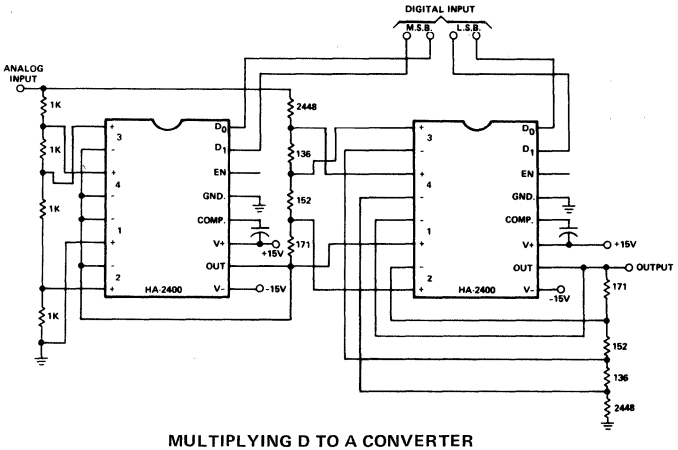
COMPARATOR, FOUR CHANNEL

When operated open loop without compensation, the HA-2400 becomes a comparator with four selectable input channels. The clamping network at the compensation pin limits the output voltage to allow DTL or TTL digital circuits to be driven with a fanout of up to ten loads.

Output rise and fall times will be about 100ns for differential input signals of several hundred millivolts, but will be in the microsecond region for small differential signals.

The circuit can be used to compare several signals against each other or against fixed references; or a single signal can be compared against several references. A "window comparator", which assures that a signal is within a voltage range, can be formed by monitoring the output polarity while rapidly switching between two channels with different reference inputs and the same signal input.

APPLICATION NO. 14



MULTIPLYING D TO A CONVERTER

The circuit above performs the function, $V_{OUT} = V_{IN} \cdot \frac{N}{16}$, where N is the binary number from 0 to 15 formed by the digital input. If the analog input is a fixed D.C. reference, the circuit is a conventional 4-bit D to A. The input could also be a variable or A.C. signal, in which case the output is the product of the analog signal and the digital signal.

The circuit on the left is a programmable attenuator with weights of 0, 1/4, 1/2 or 3/4. The circuit on the right is a non-inverting adder which adds weights to the first output of 0, 1/16, 1/8 or 3/16.

If four quadrant multiplication is required, place the Phase Selector circuit (No. 6) in series with either the analog input or output. The D_0 input of that stage becomes the + or – sign bit of the digital input.

MORE CHALLENGES

One of our favorite college textbooks paused at each climactic point with a statement to the effect that, "Proof of the following theorem is omitted, and is suggested as an exercise for the student."

The following is a list of some additional applications in which we believe the HA-2400 will prove very valuable. The "proofs", at present, remain as exercises for our ingenious readers.

- A to D Converter, Dual Slope Integrating
- Active Filter, State Variable Type with Programmable Frequency and/or Programmable "Q"
- Amplifier with Programmable D.C. Level Shift
- Chopper Amplifiers
- Crossbar Switches
- Current Source, Programmable
- F.M. Stereo Modulator
- F.S.K. Modem
- Function Generators, Programmable
- Gyrator, Programmable
- Monostable Multivibrator, Programmable
- Multiplier, Pulse Averaging
- Peak Detector with Reset
- Resistance Bridge Amplifier/Comparator with Programmable Range
- Sense Amp/Line Receiver with Programmable Threshold
- Spectrum Analyzer, Scanning Type
- Sweep Generator, Programmable
- Switching Regulator
- Touch-Tone™ Generator/Detector (Use Harris HD-0165 Keyboard Encoder I.C.)

FEEDBACK

We believe we have only scratched the surface of possible applications for a multiple channel operational amplifier.

If you have a solution for any of the previous "challenges" or any new application, please let us know. Anything from a one word description to a tested design will be welcome.

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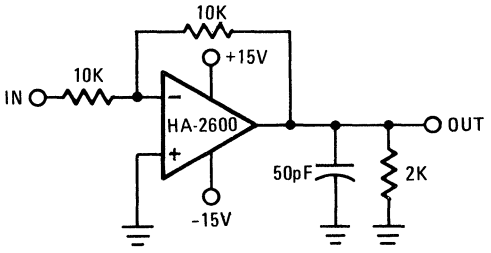
APPLICATION NOTE 515

OPERATIONAL AMPLIFIER STABILITY: INPUT CAPACITANCE CONSIDERATIONS

BY DON JONES

This is the first in a series of notes dealing with stabilization and optimization of A.C. response in operational amplifiers. One of the more common difficulties in applying operational amplifiers will be discussed.

Let's consider the unity gain inverting amplifier circuit shown below:



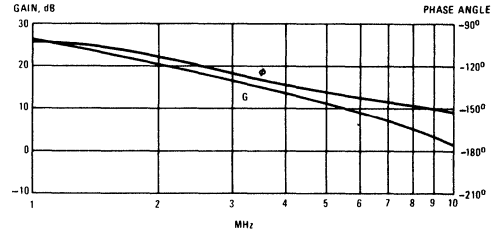
This appears to be a straightforward application with reasonable component values.

But, with the input grounded, the circuit output shows an oscillation at about 5 MHz.

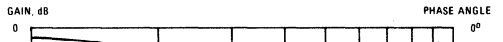
Even more surprising, if the same device is connected as a voltage follower with the same load, it is perfectly stable. Since the inverting amplifier has 6 dB less feedback than the voltage follower, shouldn't it be more stable?

The culprit here is capacitance at the amplifier inverting input. The HA-2600 in the TO-99 can has an input capacitance of about 2 or 3 pF. When soldered on a P.C. card, or inserted in a socket, wiring capacitance might add another 3 to 6 pF. With only 5K effective resistance at this point, 5 to 10 pF seems pretty negligible, doesn't it? But let's find out.

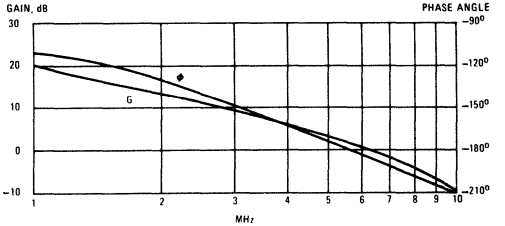
The open loop amplitude and phase response characteristics of the amplifier between 1 and 10 MHz looks like this:



The characteristics of the feedback network alone with 5 pF capacitance to ground looks like this:

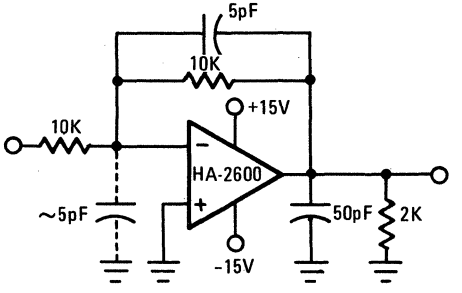


Combining these two graphs by algebraically adding the dB gains together and adding the phase shifts together gives us the open loop response at the summing point:



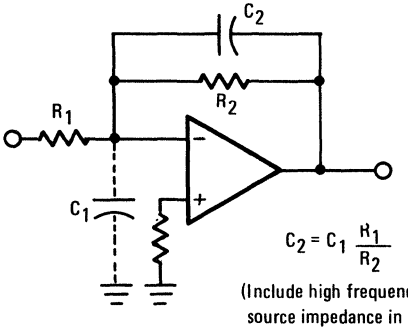
We can see that on the composite response curves, the phase shift crosses 180° at 5.5 MHz, and that there is still about +2 dB of gain at this frequency. Therefore, closing the loop automatically creates an oscillator.

How can we overcome this effect? If we add a capacitor across the feedback resistor, we can cancel the effects of the input capacitance:

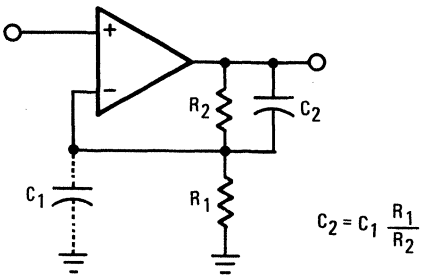


If the feedback capacitance matches the input capacitance, the response curves of the feedback network alone will be a flat -6 dB and 0° across the frequency band. The composite curves will then show a bandwidth of 7.5 MHz and a positive phase margin of 33°. So the circuit will now be quite stable. It's amazing how much difference that small capacitance can make.

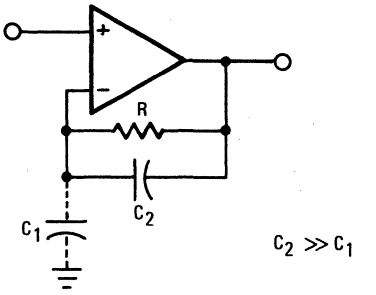
The general scheme for compensation of various circuit types is shown below:



INVERTING AMPLIFIER



NON-INVERTING AMPLIFIER



FOLLOWER WITH FEEDBACK RESISTOR

It's not really necessary to know the exact value of stray capacitance, C_1 - for most layouts, about 5 to 10 pF is a good guess. Unless you are trying to squeeze out the last Hz of frequency response, it doesn't hurt to guess on the high side. At higher gains, where C_2 calculates out to less than 1 or 2 pF, it isn't necessary to use C_2 - but it won't disturb anything if you do use it.

If you are uncertain about whether compensation is necessary, check the pulse response or frequency response of the closed loop stage. Hook a pulse generator to the input, and adjust the amplitude for about a 200 millivolt step at the output - if the output overshoot is less than 40% of the step, the circuit will be stable. Alternately, check the small signal frequency response of the stage - if the high frequency peaking is less than +6 dB, more than the low frequency gain, the circuit is stable. Of course, you can increase the compensation capacitor if you need even smoother response.

The phenomena we have described are not peculiar to any one amplifier type. Wideband amplifiers require a little more care in the design of feedback networks; but the same type oscillations will show up on 741 type amplifiers with higher feedback resistor values.

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APPLICATION NOTE 516

THE HA-2530/2535 WIDEBAND HIGH SLEW INVERTING AMPLIFIER

BY ERNIE THIBODEAUX

INTRODUCTION

The HA-2530/2535 is a monolithic inverting amplifier constructed using the Harris dielectric isolation process. It incorporates both bipolar and MOS devices on the same chip allowing excellent D.C. characteristics not normally achieved in most high performance A.C. amplifiers. The HA-2530/2535 is a continuation of the HA-2500 family of high slew rate amplifiers and represents a factor of 3 improvement in A.C. performance over the HA-2520 op amp. Its superior A.C. performance is achieved by using a two amplifier feedforward scheme on the same chip. Among the many applications best suited for this device are video amplifiers/linedrivers, high speed integrators, signal separators, waveform generators, A/D, D/A and sampled data systems. This application note will briefly discuss the internal circuitry, show how closed-loop frequency response can be predicted and present a few of the above mentioned applications.

INSIDE THE HA-2530/2535

The detailed schematic shown in Figure 1 can be simplified with the functional diagram shown in Figure 2.

Amplifier A_1 is a low frequency, high gain stage providing high accuracy at low frequencies with excellent D.C. input characteristics while A_2 is a high frequency, relatively low gain stage that dominates and controls the overall amplifier response at high frequencies. The overall input bias current is the sum of the bias currents of both amplifiers but A_2's MOSFET input stage adds little to the overall current. The high offset voltage of the MOSFET is of no significant consequence, since this offset is divided by the high open

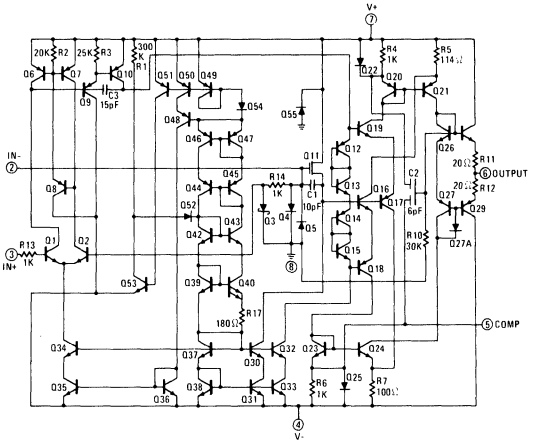


Figure 1

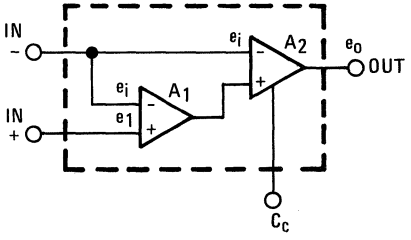


Figure 2

loop gain of A_1. Therefore, the effective D.C. input characteristics of the composite amplifier are that of A_1 alone.

The overall amplifier gain is given by the algebraic sum of the amplifier transfer functions. That is, referring to Figure 2, the open loop equation can be written as:

$$e_o = [(e_1 - e_i)A_1 - e_i]\,A_2 \qquad \text{Equation (1)}$$

7

BODE PREDICTION OF OPEN-LOOP
RESPONSE USING EQ. (5)

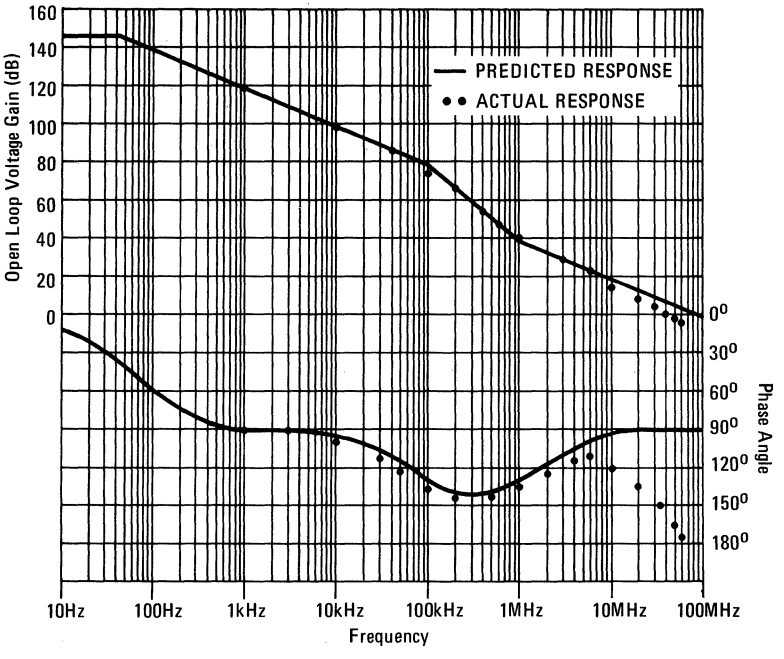


Figure 3

OPEN-LOOP RESPONSE vs.
COMPENSATION CAPACITANCE

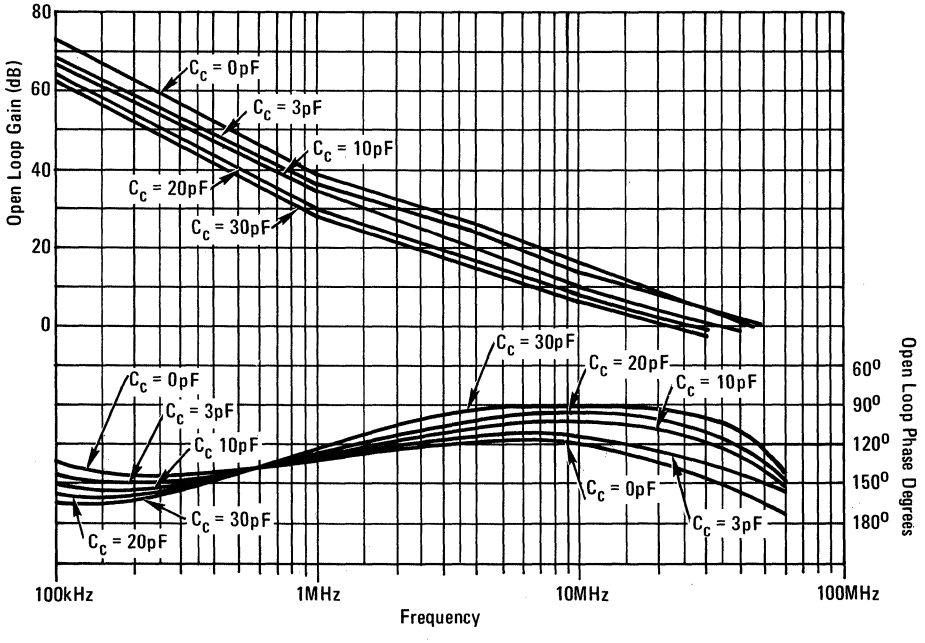


Figure 4

For the inverting configuration $e_1 = 0$ and the total amplifier gain is:

$$A_T = -(A_1A_2 + A_2) \quad \text{Equation (2)}$$

$$\text{Where } A_1(S) = \frac{G_1}{1 + T_1S} \quad \text{Equation (3)}$$

$$A_2(S) = \frac{G_2}{1 + T_2S} \quad \text{Equation (4)}$$

Solving for the overall transfer function results in the following expression:

$$A_T(S) = \frac{G_1G_2[1 + 1/G_1 + (T_1/G_1)S]}{(1 + T_1S)(1 + T_2S)} \quad \text{Equation (5)}$$

Since the D.C. voltage gain (G_1) of amplifier A_1 is typically 20,000 V/V then $1/G_1 << 1$ resulting in:

$$A_T(S) = \frac{G_1G_2\left(1 + \frac{T_1}{G_1}S\right)}{(1 + T_1S)(1 + T_2S)} \quad \text{Equation (6)}$$

The composite transfer function reveals a D.C. gain equal to the product of the D.C. gains of each amplifier (G_1G_2), a pole at the break frequency of each amplifier and a zero at the unity gain frequency of amplifier A_1. The amplifier was designed using the following:

$G_1 = 22K$ Poles: $f_{p1} = 48Hz$
$G_2 = 940$ $f_{p2} = 100kHz$
$f_{z1} = 1MHz$

A comparison of the calculated open-loop response with the actual under no load and no compensation conditions is shown in Figure 3. The two curves compare very closely up to approximately 6MHz where higher order effects dominate, causing the response to deviate from the predicted. The effect of adding compensation capacitance is to lower the pole frequency of A_2 while adding a high frequency zero. Several response curves for different compensation capacitors are shown in Figure 4.

CURVE FITTING THE HA-2530 OPEN LOOP RESPONSE

In many instances a closed-form equation defining completely the characteristics of the HA-2530 beyond it's predictable bandwidth given by Equation 6 would be desirable. This would allow modeling the device on a computer or calculator resulting in the prediction of system performance for various closed-loop configurations. Using a trial and error graphical procedure, a close-fit beyond 6MHz was obtained using several poles and a simple zero as shown below.

$$A_O(S) = \frac{1 + T_6S}{(1 + T_3S)(1 + T_4S)(1 + T_5S)}$$

Equation (7)

Poles: $f_{p3} = 6MHz$ Zero: $f_{z6} = 7MHz$
$f_{p4} = 30MHz$
$f_{p5} = 150MHz$

A comparison of the actual uncompensated ($C_C = 0$) response with that given by Equation 7 above is shown in Figure 5. Combining Equation 6 and 7, the calculated open-loop transfer function from D.C. to 50MHz is obtained.

APPROXIMATION OF HIGH FREQUENCY CHARACTERISTIC USING EQUATION (7)

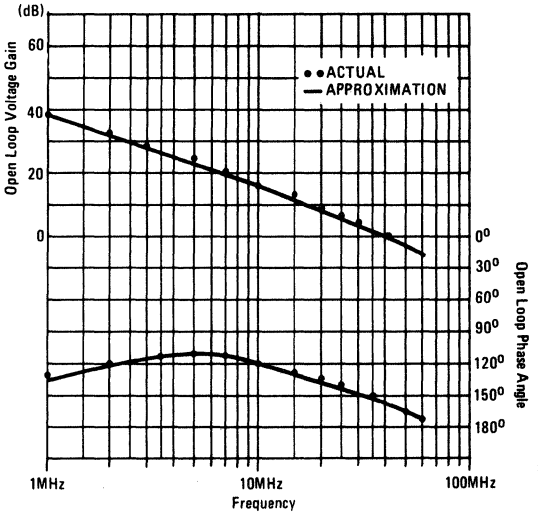


Figure 5

$$A_T'(S) = A_0(S) \cdot A_T(S) = \frac{G_1G_2(1+T_1/G_1S)(1+T_6S)}{(1+T_1S)(1+T_2S)(T+T_3S)(1+T_4S)(1+T_5S)}$$

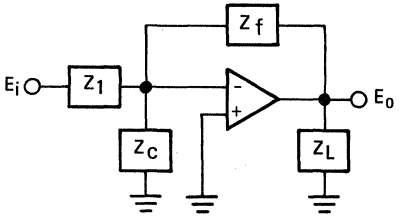
Equation (8)

This equation represents a working transfer function for the typical HA-2530/2535 and may be useful in many synthesis applications.

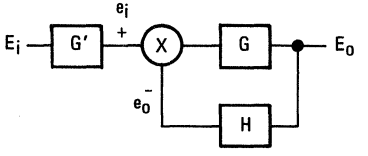
THE INVERTING AMPLIFIER

GENERAL REPRESENTATION

Consider the general inverting configuration below:

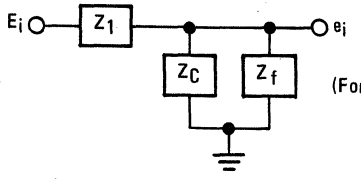


The control system representation of the circuit is:



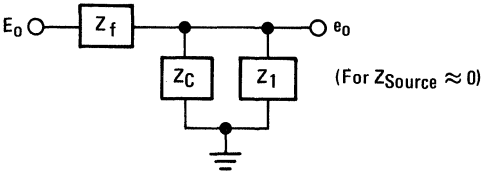
Where: $\frac{E_O}{E_i} = \frac{-G'G}{1+GH}$ **Equation (9)**

The transfer functions G' and H can be solved very simply by assuming the ideal operational amplifier and using the principle of superposition. First, G' is calculated by disconnecting the amplifier summing point from the rest of the circuit and calculating the voltage e_i with ideal voltage source E_i impressed as shown below.



$$G' = \frac{e_i}{E_i} = \frac{Z_CZ_f}{Z_1Z_C + Z_1Z_f + Z_CZ_f}$$ **Equation (10)**

The feedback transfer function is calculated similarly by calculating e_o with E_o impressed.



$$H = \frac{e_o}{E_o} = \frac{Z_CZ_1}{Z_fZ_1 + Z_fZ_C + Z_CZ_1}$$ **Equation (11)**

Writing G' in terms of H we have:

$$G' = (Z_f/Z_1)(H)$$ **Equation (12)**

Finally, the closed-loop transfer function is obtained below by combining Equation 9 and Equation 12.

$$\frac{E_o}{E_i} = \frac{-Z_f}{Z_1}\left[\frac{GH}{1+GH}\right]$$ **Equation (13)**

As will be seen later, the closed-loop equation is in a very convenient form for the graphical evaluation of closed-loop response.

PHASE MARGIN DETERMINATION

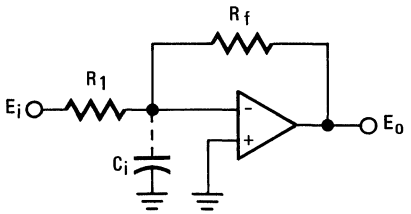
Phase margin for the unity gain inverting amplifier is not evaluated at the 0dB crossing of the open loop gain response as might be expected. By definition phase margin is evaluated when the magnitude of the loop gain |GH| is 1. For the non-inverting amplifier the feedback factor (H) is unity (full feedback) and phase margin is evaluated at |G| = 1 or 0dB. However, for the unity gain inverting amplifier H is 1/2 (equal voltage division caused by input and feedback resistors) so that phase margin is evaluated at |G| = 2 or 6dB.

In general, for the inverting amplifier, the phase margin would be determined at:

$$|G| = \frac{R_1 + R_f}{R_1}$$ **Equation (14)**

EFFECTS OF INPUT CAPACITANCE ON HIGH FREQUENCY STABILITY

The effects of input capacitance (C_i) can probably best be illustrated by evaluating phase margin under this condition. Calculating the feedback factor, H, from the circuit below:



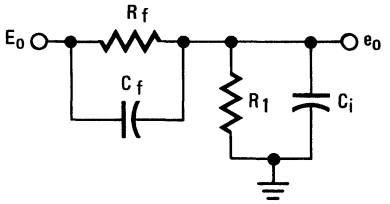
We obtain from Equation 11:

$$H = \frac{R_1/(R_f + R_1)}{1 + S(R_{1f}C_i)}$$

where $R_{1f} = R_1 \,||\, R_f$ **Equation (15)**

Therefore, the input capacitance creates a pole at wp = $1/R_{1f}C_i$ producing additional phase shift about this frequency. This will reduce the phase margin resulting in possible oscillation. For example, if $R_1 = R_f = 2K$ and $C_i = 10pF$, the pole frequency is found to be fp = 16MHz. The loop gain plot $(GH)_i$ in Figure 6 reveals a perfect oscillatory condition at 18MHz; i.e. IGHI = 0dB and ϕ_i (phase margin) = 0. If input capacitance were neglected, our prediction would have erroneously resulted in a phase margin (ϕ_o) of 38°.

The effects of input capacitance can be cancelled by adding a feedback capacitor (C_f) across resistor R_f. Recalculating H from the feedback network below:



We have:

$$H = \frac{[R_1/(R_1 + R_f)](1 + SR_fC_f)}{1 + SR_{1f}(C_i + C_f)}$$ **Equation (16)**

From this equation we see that adding C_f creates a zero that can be adjusted to cancel the denominator pole, resulting in a pure resistive feedback factor.

The condition for this cancellation is:

$$R_fC_f = R_{1f}(C_i + C_f)$$ **Equation (17)**

or

$$C_f = (R_1/R_f)C_i$$ **Equation (18)**

For unity gain, the feedback capacitance should equal the input capacitance. Adding C_f for gains greater than 10 becomes academic, since C_f calculates to be less than 1pF. Although adding C_f alleviates phase shift caused by C_i, it should be noted that it also creates a closed-loop pole at $1/R_fC_f$ that could limit the attainable bandwidth. For example, if the 6dB open-loop bandwidth is 30MHz, $C_i = C_f = 10pF$, and $R_1 = R_f = 2K$, the closed-loop pole occurs at 8MHz causing the frequency response to roll-off prematurely at this frequency. Decreasing the resistor values by a factor of 4 would increase the pole frequency to 32MHz and the attainable bandwidth would only be limited by the open-loop bandwidth and not the external circuit components. However, care must be taken not to make input and feedback resistors too small, since loading problems may result. That is, the input resistor, R_1, represents a load to the

input driving source, since R_1 is connected to the amplifier summing point which is at "virtual" ground. Furthermore, the feedback resistor, R_f, loads the amplifier output for the same reason.

EFFECTS OF INPUT CAPACITANCE ON PHASE MARGIN

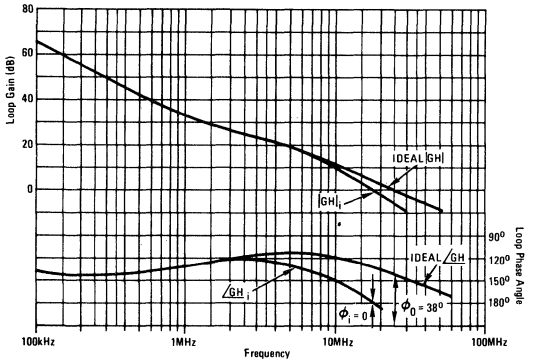


Figure 6

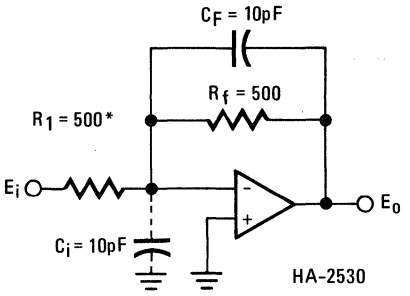
In summary, the effects of input capacitance can be negated by providing a feedback capacitor according to Equation 18. For closed-loop gains greater than 10, no feedback capacitor is required. Finally, trade-offs between maximum bandwidth, circuit component values and stability will have to be made in most cases.

PREDICTION OF CLOSED-LOOP RESPONSE USING A GRAPHICAL PROCEDURE

The closed-loop response of any amplifier can be graphically determined from its open-loop response curve. The generalized closed-loop transfer function is restated and given below:

$$\frac{E_o}{E_i} = -\frac{Z_f}{Z_1}\left[\frac{GH}{1+GH}\right] \qquad \textbf{Equation (19)}$$

The graphical procedure using the Nichols chart (Figure 7) conveniently determines the above function in brackets from the amplifier loop gain (GH) plot. Using the following circuit, let's graphically obtian its closed loop response and compare it with actual experimental results.



*Note: $R_1 = R_f = 500\ \Omega$
Chosen to obtain maximum bandwidth.

The complete procedure is:

(1) Plot both gain and phase of the GH function on semi-log paper (see ideal GH curve Figure 6). The following points were tabulated:

f (MHz)	1	2	4	6	10	15
|GH| (dB)	33	26	21	17	12	6
∠GH	-132°	-120°	-114°	-114°	-120°	-128°
f (MHz)	17	20	25	30	38	42
|GH|(dB)	5	3	0	-2	-5	-7
∠GH	-132°	-137°	-142°	-148°	-155°	-160°

(2) Transfer gain/phase points obtained above at selected frequencies to create a smooth curve on the Nichols chart using the rectangular coordinates.

(3) Obtain directly from the chart gain/phase of the function ($\frac{GH}{1+GH}$) at the selected data points. The following was tabulated:

f (MHz)	1	2	4	6	10	15
$\left\lvert\frac{GH}{1+GH}\right\rvert$ (dB)	0.14	0.22	0.3	0.45	0.7	2
$\angle\frac{GH}{1+GH}$	-1°	-2.5°	-5°	-8°	-15°	-30°
f (MHz)	17	20	25	30	38	42
$\left\lvert\frac{GH}{1+GH}\right\rvert$ (dB)	2.3	3.2	4.0	3.5	0	-2.5
$\angle\frac{GH}{1+GH}$	-35°	-45°	-70°	-75°	-130°	-145°

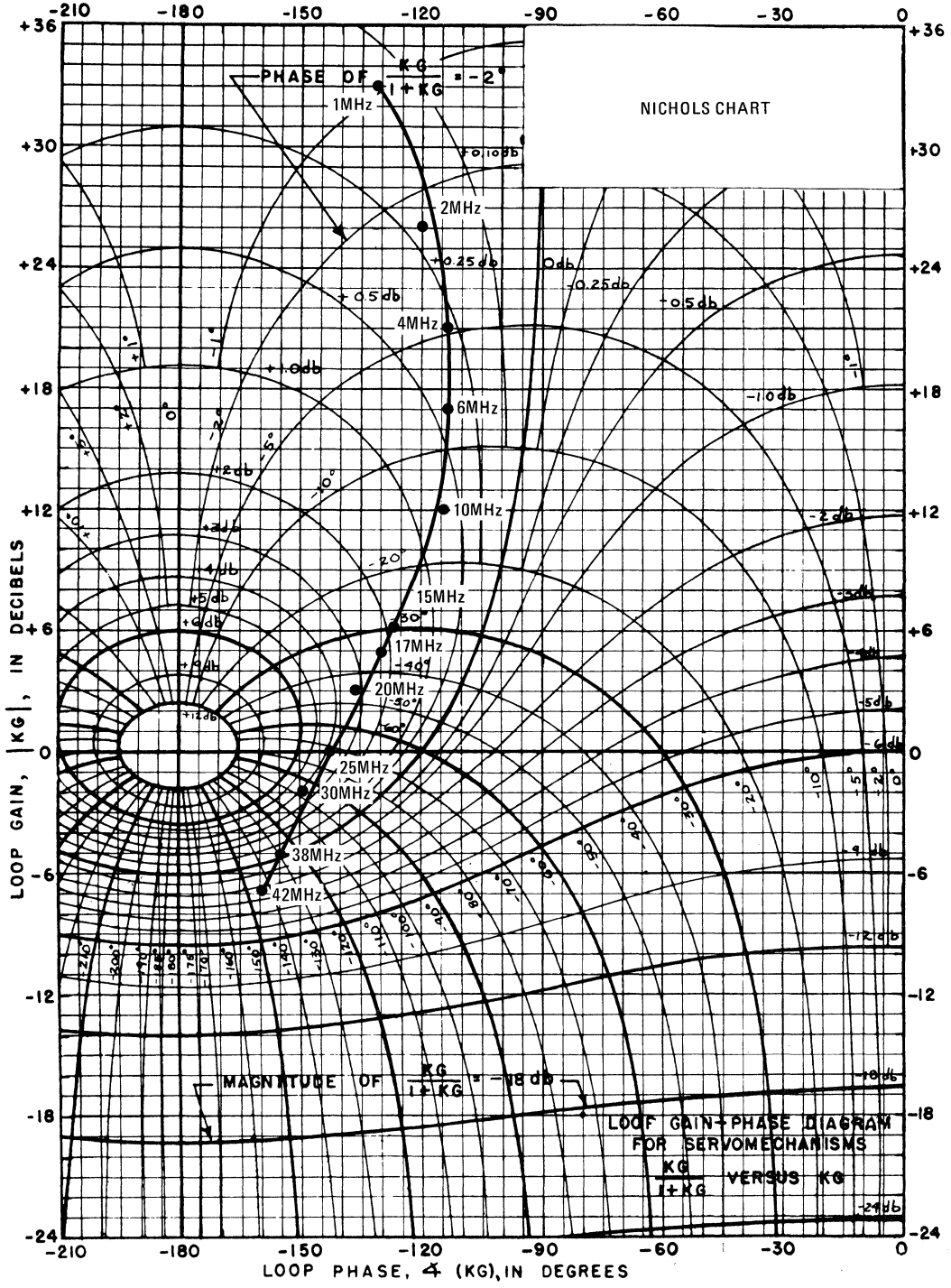

NICHOLS CHART
PHASE OF KG/(1+KG) = -2°
1MHz
2MHz
4MHz
6MHz
10MHz
15MHz
17MHz
20MHz
25MHz
30MHz
38MHz
42MHz
+0.10db
+0.25db
0db
-0.25db
-0.5db
+0.5db
+1.0db
-1.0db
-2db
-3db
-5db
-6db
-9db
-12db
MAGNITUDE OF KG/(1+KG) = -18 db
LOOP GAIN-PHASE DIAGRAM FOR SERVOMECHANISMS
KG/(1+KG) VERSUS KG
LOOP GAIN, |KG|, IN DECIBELS
LOOP PHASE, ∠ (KG), IN DEGREES
-210
-180
-150
-120
-90
-60
-30
0
+36
+30
+24
+18
+12
+6
0
-6
-12
-18
-24

Figure 7

(4) Transfer these points to semi-log paper and add the pole given by $w = \frac{1}{R_f C_f}$ (or f_p = 32MHz for this case) to obtain the calculated closed-loop response, $(\frac{E_o}{E_i})_{CALC}$ shown in Figure 8.

(5) Obtain Bandwidth, Peaking and closed-loop phase margin from the closed-loop response given in Figure 8.

Comparing the actual closed-loop response with that of our prediction, we see that favorable results were obtained. The performance specifications are:

PREDICTION OF CLOSED LOOP RESPONSE USING NICHOLS CHART

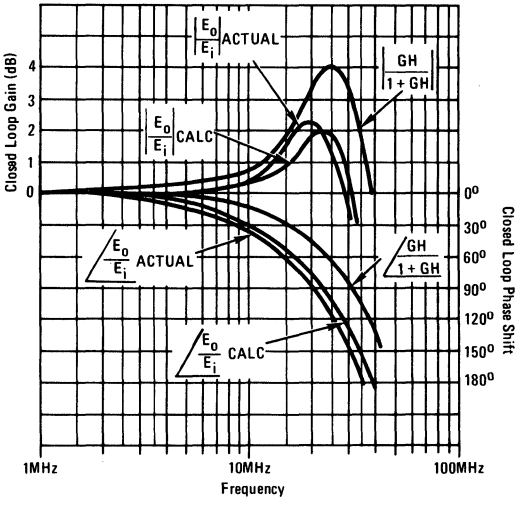


Figure 8

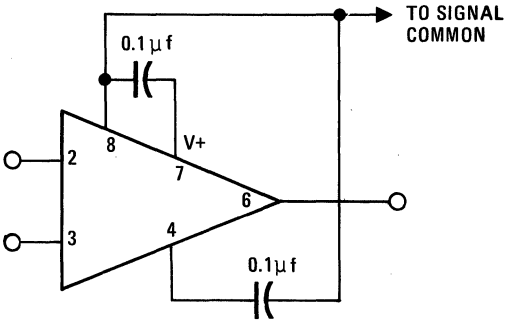
	ACTUAL	PREDICTED
Bandwidth(0dB)	29MHz	31MHz
Closed Loop Phase Margin	39°	42°
Mp (peaking)	2.3dB	2dB

SPECIAL CONSIDERATIONS FOR OPTIMUM PERFORMANCE

INTRODUCTION

Obtaining the best performance from high frequency amplifiers is not always easy. External components, deoupling, stray wiring capacitance and long lead lengths are a few of the culprits that can take a 30MHz amplifier and convert it to a 3MHz amplifier with no effort at all. However, we can avoid these shortcomings if a few simple rules are followed:

(1) Decouple as close to the amplifier pins as possible. In fact, decoupling the HA-2530 as shown below will give best results.



(2) Know your decoupling caps: At RF frequencies decoupling capacitors may look like an inductor and/or resistor. Select a good H.F. ceramic.

(3) Orient components to minimize stray capacitance.

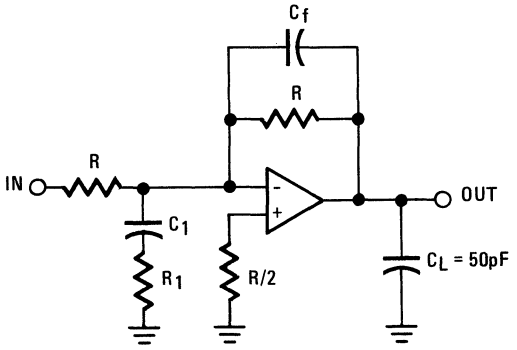
(4) Keep leads short to minimize inductance and prevent ground loop problems.

(5) Keep input and feedback resistor values as small as practical; they react with stray and input capacitance.

(6) Minimize loading capacitance; it affects settling time and stability (see how in next section).

CIRCUIT FOR OPTIMUM SETTLING TIME

Before we investigate settling time, let's take a look at phase margin with a capacitive load of $C_L = 50pF$. The effects of load capacitance can be seen by referring to the uncompensated phase response shown in Figure 9. Note the phase margin reduction from approximately 38^o (Figure 3) to only 4^o; a marginally stable condition with a long settling time. The load capacitance effectively causes a high frequency pole whose break frequency is $\frac{1}{2}\pi R_{OUT} C_L$, where R_{OUT} is the approximate output resistance of the amplifier. The additional phase shift that C_L adds will give us some hint as to the pole location. That is, at 25MHz, about 34^o is added to the unloaded response resulting in a pole frequency of about 40MHz. Using this break frequency, R_{OUT} calculates to be about 80 ohms. This bit of information may prove useful in evaluating closed-loop response against various capacitive loads. At this point, let's see how we can improve phase margin to improve settling time. Consider the circuit below consisting of the pole-zero compensating network ($R_1 - C_1$).



OPEN LOOP RESPONSE USING POLE-ZERO COMPENSATION AND C_L = 50pf

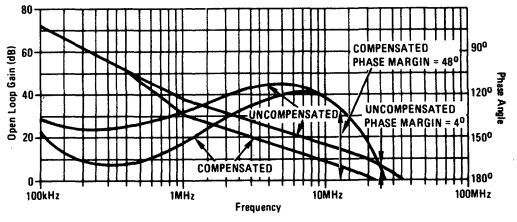


Figure 9

CIRCUIT FOR OPTIMUM SETTLING TIME (continued)

The $R_1 - C_1$ network will increase phase margin by sacrificing a small amount of bandwidth at no expense to slew rate. Slew rate is not affected as long as the voltage divider made up of the input resistor (R) and $R_1 \parallel R$ provides an instantaneous voltage at the summing point that will be sufficient to slew the amplifier. Assuming a single pole response and a bandwidth of 25MHz, this voltage to a first approximation should be greater than 1.8 volts.

The network forces an increase in phase margin by rolling-off the amplifier gain response without affecting phase response at the bandwidth frequency. The pole-zero locations are chosen at frequencies where the loop gain is large enough to buffer the error effects caused by the additional phase shift of the network in this region. Component values are chosen to satisfy the slew condition and neutralize high frequency phase shift caused by the input capacitance according to the relationship.

$$(R_1 \parallel R)C_i = RC_f \qquad \textbf{Equation (20)}$$

The following values were determined experimentally for optimum settling time and satisfy the conditions mentioned previously.

$R = 2K\Omega$ $\quad C_1 = 250pF$ $\quad C_i = 10pF$
$R_1 = 620\Omega$ $\quad C_f = 3pF$

The pole-zero locations are approximately:

$$\text{Pole: } f_{pl} = \frac{1}{2\pi(R/2 + R_1)C_1} = 400kHz$$

$$\text{Zero: } f_{zl} = \frac{1}{2\pi R_1 C_1} = 1MHz$$

The compensated open-loop response curve shown in Figure 9 shows the effects of the pole-zero additions. Note how its phase response deviates from the uncompensated at frequencies less than 10MHz but coincides

above this frequency allowing a phase margin of 48° to be achieved. From experimental data using a 10V pulse, a typical settling time to 0.1% of 550ns was achieved. Settling times to 0.1% for various compensation capacitors without the pole-zero network are shown in the table below.

	C_C	0pF	3pF	10pF	20pF	30pF
C_L = 0pF	T_S(ns)	500	540	620	760	880
C_L = 50pF	T_S(ns)	Unstable	650	740	840	940

Looking at the table, we see that the best settling time without the pole-zero compensating network is 650ns with C_C = 3pF. This will suffice for most pulse applications but optimum settling is still obtained with the pole-zero network.

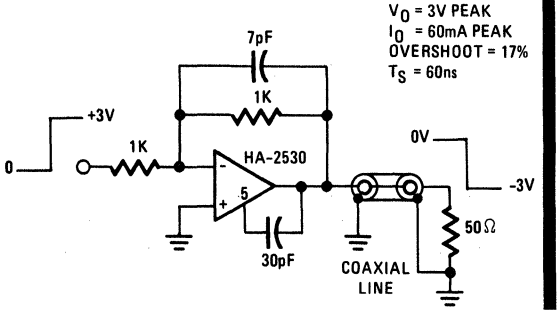
APPLICATIONS

INTRODUCTION

In all the applications to be discussed the HA-2530 is used as an inverting amplifier. Usage as a non-inverting amplifier can be used but the common mode range is limited to about ±0.5V because the inverting input is diode-clamped to signal ground. Usable bandwidth in this mode is only about 100kHz.

APPLICATION 1
FAST SETTLING COAXIAL DRIVER

The circuit below is intended for use in line driving systems requiring good settling at high output current levels; such as radar pulse drivers, video sync driver, PAM line driver, etc.

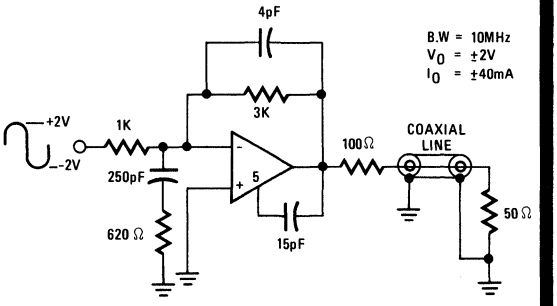


The input voltage source supplies only 3mA at 3 volts into the driver circuit which develops an output current drive of 60mA into a 50 ohm load. At these low voltage levels, the HA-2530 relies chiefly upon its excellent gain bandwidth product resulting in a 5% settling time of 60ns.

Although the HA-2530 is capable of providing high output current, special attention should be given to the input duty cycle so that the maximum power dissipation of the device is not exceeded; especially if operating at high ambient temperatures (consult data sheet for details).

APPLICATION 2
10MHz COAXIAL LINE DRIVER

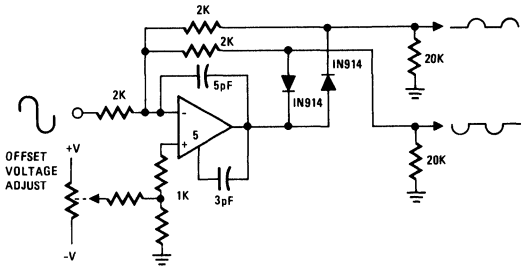
The circuit shown below will find excellent usage in high frequency line driving systems that require wide-power bandwidths at high output current levels.



The bandwidth of the circuit is limited only by the single pole response of the feedback components; namely $f_{-3dB} = \frac{1}{2}\pi R_f C_f$. As such, the response is flat with no peaking and yields minimum distortion.

APPLICATION 3
WIDE RANGE SIGNAL SEPARATOR

The high open-loop gain of the HA-2530 along with its high slew rate will allow a wide variation of input voltages and a wide frequency response as well. The circuit separates the input voltage into its positive and negative components. The diodes steer the positive and negative components to the

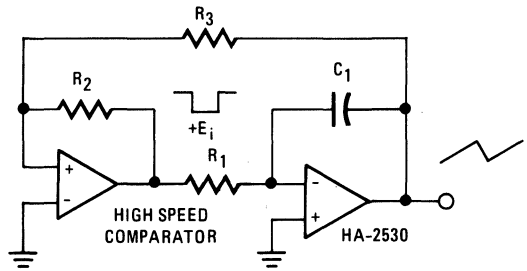


respective outputs. When placed in the feedback loop they virtually act as ideal diodes since the output error voltage is only the forward voltage drop divided by the loop gain of the amplifier. The two outputs can be driven into a differential amplifier to produce an absolute value circuit useful in many multiplier and averaging circuits.

Dynamic ranges between 60dB and 80dB can be obtained depending upon the maximum operating frequency. For example, in the circuit above a dynamic range from 5mV to 10 volts peak was easily obtained for a bandwidth of 100kHz without offset voltage adjustment. For a bandwidth of 1MHz, the range was 100mV to 10 volts peak. Dynamic ranges approaching 60dB at 1MHz can be obtained with proper offset voltage adjustment.

APPLICATION 4
HIGH FREQUENCY TRIANGULAR WAVE GENERATOR

Frequency generation well into the megahertz region can be realized with the HA-2530. Assuming circuit operation is not limited by the comparator's speed, operating frequencies between 1MHz and 5MHz can be achieved with the circuit below.



The integration time constant and circuit gain is set according to:

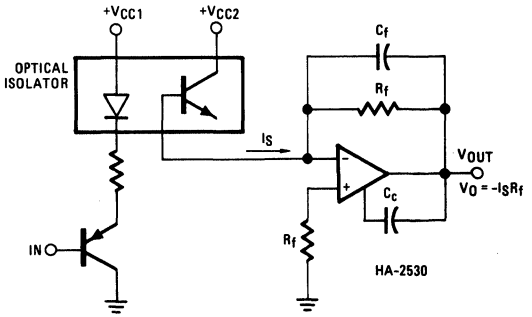
$$(a)\quad f = \frac{1}{4R_1C_1}\left(\frac{R_2}{R_3}\right)$$

$$(b)\quad \frac{E_o}{E_i} = -\frac{R_3}{R_2}$$

For accurate integration, the time constant, $\frac{R_3}{R_2}(R_1C_1)$, should be large compared to the unity gain frequency time constant and the comparator rise time. Also, the integrating capacitor, C_1, should be large in relation to the input capacitance of the amplifier while the resistors should be small to avoid reacting with stray and input capacitances. For larger output swings, another HA-2530 could be cascaded for amplification.

APPLICATION 5
CURRENT-TO-VOLTAGE CONVERTER

FET amplifiers used as current amplifiers offer the greatest resolution of current input because they have very low input bias currents. However, their input offset voltage and drift characteristics are very poor, sometimes adding to gross inaccuracies over temperature. The HA-2530 offers excellent offset voltage and drift characteristics (0.8mV, 5μV/°C) with low bias currents (17nA). The circuit below depicts the HA-2530 used to enhance the speed of an optical isolator interface. Operating the photo-transistor as a diode will increase speed at the expense of decreased current output. In this configuration the maximum current output may vary from 100μA to 400μA depending upon the LED pulse duration. At these current levels the errors of the HA-2530 are negligible and speed is limited only by the gain-bandwidth of the amplifier with attainable rise times of 20ns.



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APPLICATION NOTE 517

APPLICATIONS OF A MONOLITHIC SAMPLE-AND-HOLD/GATED OPERATIONAL AMPLIFIER

BY DON JONES

INTRODUCTION

The sample-and-hold or track-and-hold function is very widely used in linear systems. Until recently, this function was available only in modular or hybrid circuits; or perhaps most frequently the circuit was constructed by the user from an analog switch, a capacitor, and a very low bias current operational amplifier.

A high quality sample-and-hold circuit must meet certain requirements:

(1) The holding capacitor must charge up and settle to its final value as quickly as possible.

(2) When holding, the leakage current at the capacitor must be as near zero as possible to minimize voltage drift with time.

(3) Other sources of error must be minimized.

Design of a sample-and-hold, particularly the user built variety, involves a number of compromises in the above requirements. The amplifier or other device feeding the analog switch must have high current capability and be able to drive capacitive loads with stability. The analog switch must have both low ON resistance and extremely low OFF leakage currents. But, leakage currents of most analog switches (except the dielectrically isolated types) run to several hundred nanoamperes at elevated temperatures. The analog switch must have very low coupling between the digital input and analog output, because any spikes generated at the instant of turn-off will change the charge on the capacitor. The output amplifier must have extremely low bias current over the temperature range, and also must have low offset drift and sufficient slew rate; a combination satisfied by only a few available amplifiers.

THE HA-2420/2425

The HA-2420/2425 is the first complete monolithic sample-and-hold integrated circuit. A functional diagram is shown in Figure 1.

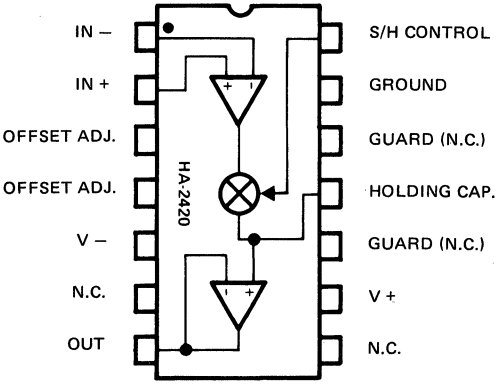


Figure 1 – HA-2420/2425 Functional Diagram

The input amplifier stage is a high performance operational amplifier with excellent slew rate, and the ability to drive high capacitance loads without instability. The switching element is a highly efficient bipolar transistor stage with extremely low leakage in the OFF condition. The output amplifier is a MOSFET input unity gain follower to achieve extremely low bias current.

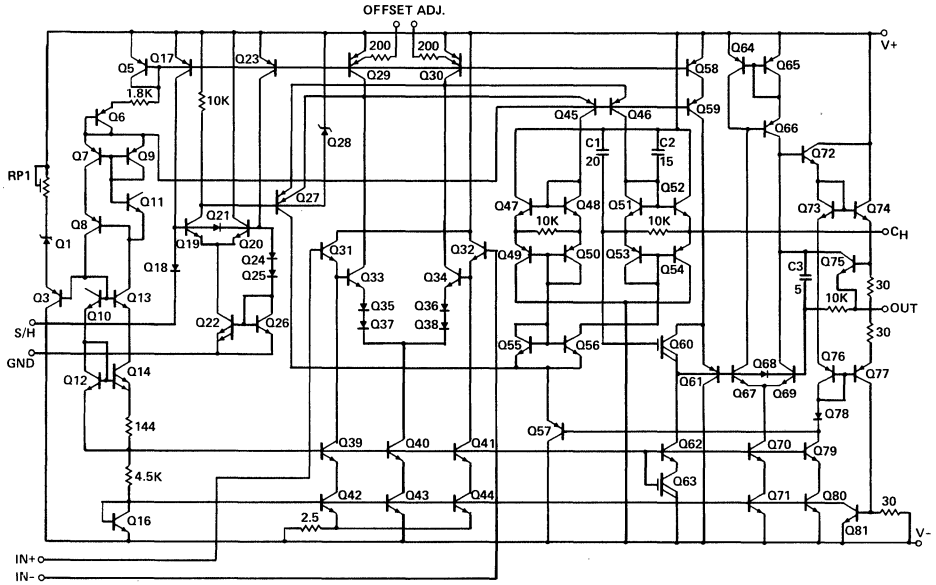
MOSFET inputs are generally not used for D.C. amplifiers because their offset voltage

7

drift is difficult to control. In this configuration, however, negative feedback is generally applied between the output and inputs of the entire device, and the effect of this offset drift at the inputs is divided by the open loop gain of the input amplifier stage.

The schematic of the HA-2420 is in Figure 2. During sampling (S/H control LOW) the signal path through the input amplifier stage starts at Q31-34, through Q45 and Q46, and then to the holding capacitor terminal through Q51-54. The output follower amplifier has its input at MOSFET Q60.

HA-2420/2425
Sample-and-Hold



NOTE: 1. Unless otherwise specified resistance values are in OHMS, capacitance values are in picofarads.

Figure 2

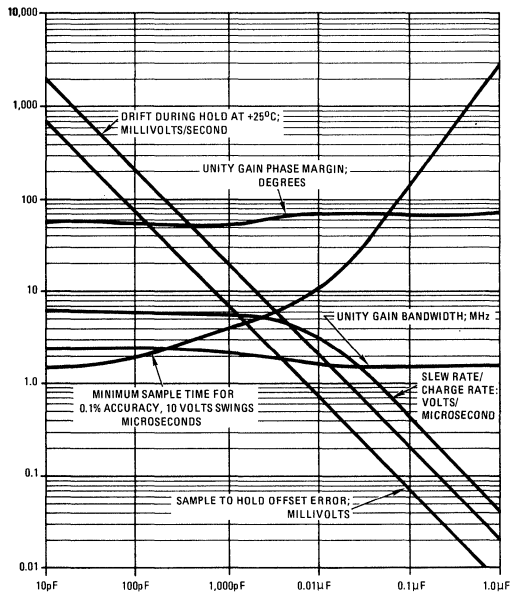


Figure 3 – Holding Capacitor, C_H

TYPICAL SAMPLE-AND-HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITANCE

In the "hold" mode, the S/H control is HIGH, so Q21 conducts, turning on Q27 which diverts the signal away from Q45 and Q46, and passes the signal to V - through Q57. Q57 also forces Q51-54 to ride up and down with the output signal, so there is virtually zero potential between these transistor bases and the voltage on C_H; completely eliminating leakage from C_H back into the input amplifier.

SAMPLE-AND-HOLD APPLICATIONS

A number of basic applications are shown on the following pages. The device is exceptionally versatile, since it can be wired into any of the hundreds of feedback configurations possible with any operational amplifier. In many applications the device will replace both an operational amplifier and a sample-and-hold module.

The larger the value of the timing capacitor, the longer time it will hold the signal without excessive drift; however, it will also reduce the

charging rate/slew rate and the amplifier bandwidth during sampling. So the capacitance value must be optimized for each particular application. The graph in Figure 3 shows these tradeoffs. Drift during holding tends to double for every 10°C rise in ambient temperature. The holding capacitor should have extremely high insulation resistance and low dielectric absorption-polystyrene (below +85°C), Teflon, or mica types are recommended.

Guard Ring Layout (Bottom View)

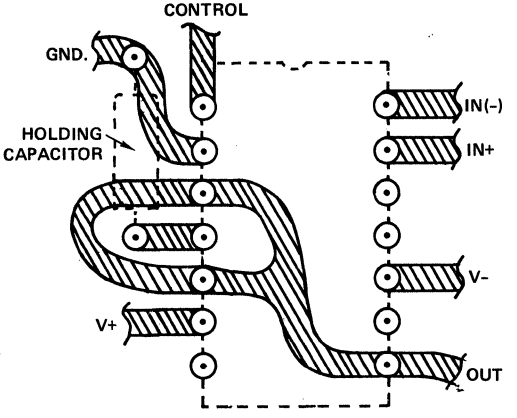


Figure 4

For least drift during holding, leakage paths on the P.C. board and on the device package surface must be minimized. Since the output voltage is nearly equal to the voltage on C_H, the output line may be used as a guard line surrounding the line to C_H. Then, since the potentials are nearly equal, very low leakage currents will flow. The two package pins surrounding the C_H pin are not internally connected, and may be used as guard pins to reduce leakage on the package surface. A suggested P.C. guard ring layout is shown in Figure 4.

GATED OPERATIONAL AMPLIFIER APPLICATIONS

An operational amplifier with a highly efficient analog switch in series with its output is a very useful building block for linear systems. The amplifier can be connected in any of the conventional op amp feedback configurations. With the switch closed, the circuit behaves as a conventional op amp with excellent bandwidth, slew rate, high output current capability, and is able to drive capacitive loads with good stability. With the switch open, the output node is an almost perfect open circuit.

The output buffer amplifier has extremely high input impedance and exceptionally low bias current, but is not particularly well suited for D.C. applications outside an overall feedback loop, since its offset voltage may be quite high.

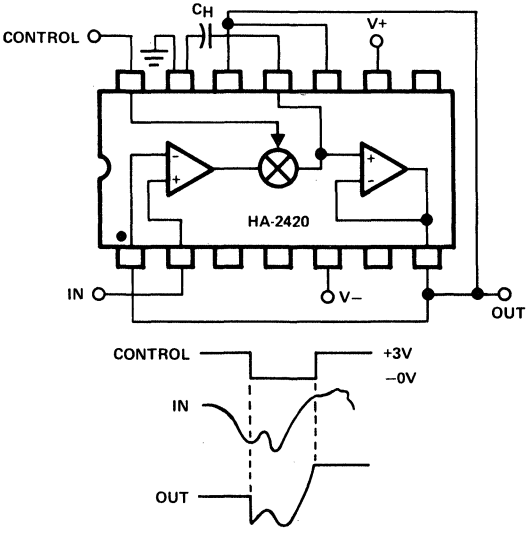
A number of possible gated amplifier applications are suggested in the following section.

APPLICATION NO. 1

Feedback is the same as a conventional op amp voltage follower which yields a unity gain, non-inverting output. This hookup also has a very high input impedance.

The only difference between a track-and-hold and a sample-and-hold is the time period during which the switch is closed. In track-and-hold operation, the switch is closed for a relatively long period during which the output signal may change appreciably; and the output will hold the level present at the instant the switch is opened. In sample-and-hold opera-

Basic Track-and-Hold/Sample-and-Hold



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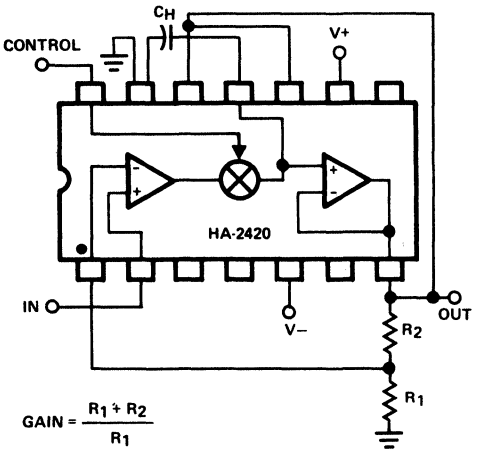
tion, the switch is closed only for the period of time necessary to fully charge the holding capacitor.

APPLICATION NO. 2

Sample-and-Hold With Gain



This is the standard non-inverting amplifier feedback circuit.

It illustrates one of the many ways in which the HA-2420 may be used to perform both op amp and sampling functions, eliminating the need for a separate scaling amplifier and sample-and-hold module.

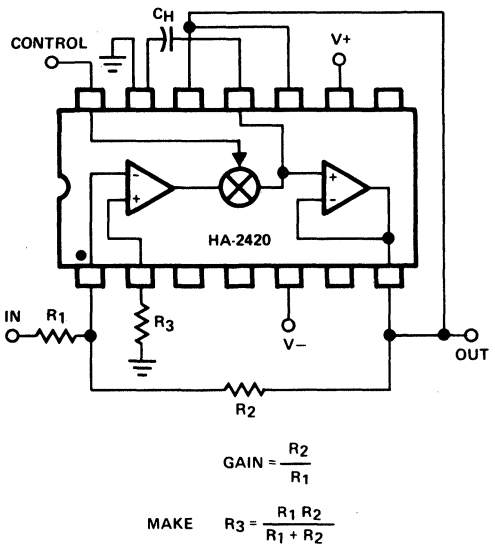
In general, it is usually best design practice to scale the gain such that the largest expected signal will give an output close to + or − 10 volts. Drift current is essentially independent of output level, and less percentage drift will occur in a given time for a larger output signal.

APPLICATION NO. 3

This illustrates another application in which the hookup versatility of the HA-2400 often eliminates the need for a separate operational amplifier and sample-and-hold module. This hookup will have somewhat higher input to output feedthrough during "hold," than the non-inverting connection, since output impedance is the open-loop value during "hold," and feedthrough will be:

$$\frac{Vin\ Ro}{R_1 + R_2 + R_0}$$

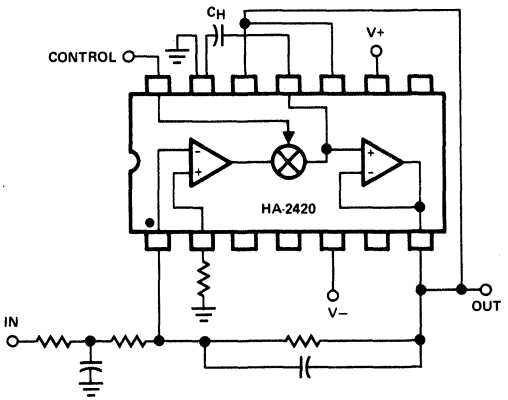
Inverting Sample-and-Hold



APPLICATION NO. 4

It is often required that a signal be filtered prior to sampling. This can be accomplished with only one device. Any of the inverting and non-inverting filters which can be built with op amps can be implemented. However, it is necessary that the sampling switch be closed for sufficient time for the filter to settle when active filter types are connected around the device.

Filtered Sample-and-Hold



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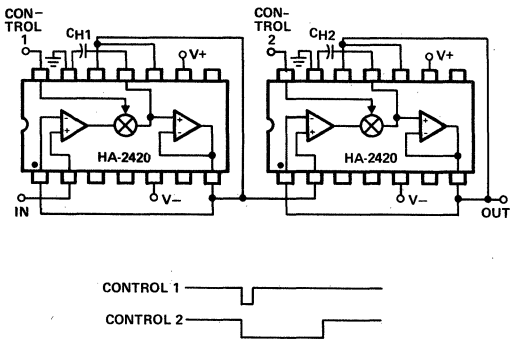
APPLICATION NO. 5

Cascaded Sample-and-Hold

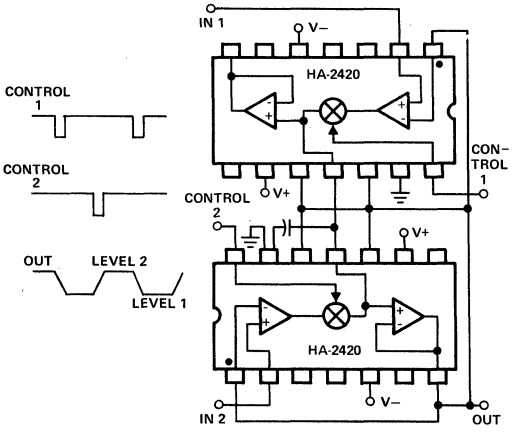


Short sample times require a low value holding capacitor; while long, accurate hold times require a high value holding capacitor. So, achieving a very long hold with a short sample appears to be contradictory. However, it can be accomplished by cascading two S/H circuits, the first with a low value capacitor, the second with a high value. Then the second S/H can sample for as long a time as the first circuit can accurately hold the signal.

APPLICATION NO. 6

Two or more S/H circuits may share a common holding capacitor and output as shown. The only limit to the number of devices to be

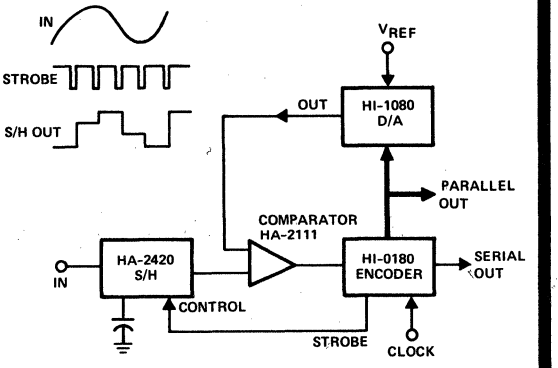
Multiplexed Sample-and-Hold



multiplexed is that the leakage currents of all devices add together, which increases drift during holding.

APPLICATION NO. 7

A/D Converter

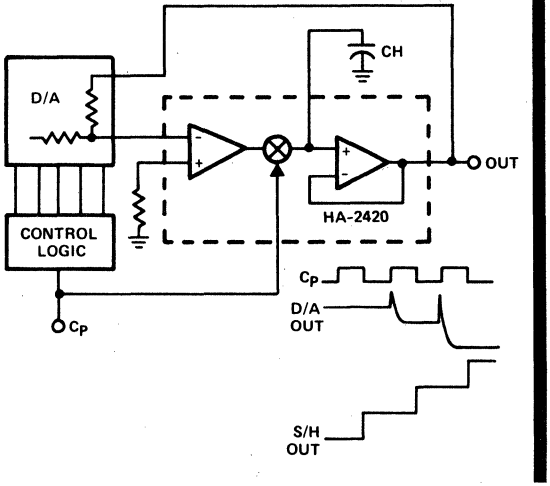


Certain analog to digital converters such as the successive approximation type require that the input signal be a steady D.C. level during the conversion cycle. The HA-2420 is ideal for holding the signal steady during conversion; and also functions as a buffer amplifier for the input signal, adding gain, inversion, etc., if required.

The system illustrated is a complete 8 bit successive approximation converter requiring only four I.C. packages and capable of up to 40,000 conversions per second. Interconnection details are shown on the HI-0180 data sheet.

APPLICATION NO. 8

De-Glitcher



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The word "glitch" has been a universal slang expression among electronics people for an unwanted transient condition. In D to A converters, the word has achieved semi-official status for an output transient which momentarily goes in the wrong direction when the digital input address is changed.

In the illustration, the HA-2420 does double duty, serving as a buffer amplifier as well as a glitch remover, delaying the output by ½ clock cycle.

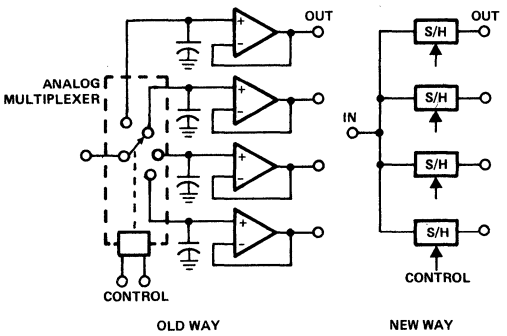
The HA-2420 may be used to remove many other types of "glitches" in a system. If a delayed sample pulse is required, this can be generated using a dual monostable multivibrator I.C.

APPLICATION NO. 9

This circuit reconstructs and separates analog signals which have been time division multiplexed.

The conventional method, shown on the left, has several restrictions, particularly when a short dwell time and a long, accurate hold time is required. The capacitors must charge from a low impedance source through the resistance and current limiting characteristics of the multiplexer. When holding, the high impedance lines are relatively long and subject

De-Multiplexer

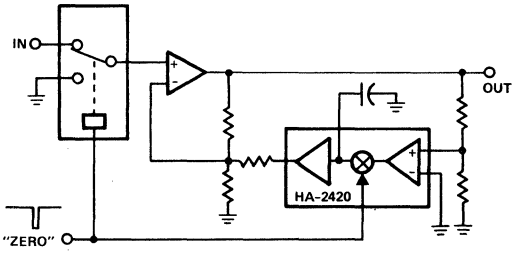


to noise pickup and leakage. When FET input buffer amplifiers are used for low leakage, severe temperature offset errors are often introduced.

Use of the HA-2420 greatly diminishes all of these problems.

APPLICATION NO. 10

Automatic Offset Zeroing



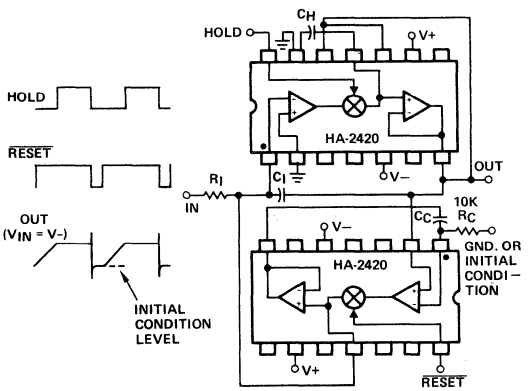
This basic circuit has widespread applications in instrumentation, A/D conversion, DVM's and DPM's to eliminate offset drift errors by periodically rezeroing the system. Basically, the input is periodically grounded, the output offset is then sampled and fed back to cancel the error.

The system illustrated automatically zeros a high gain amplifier. Care in the actual design is necessary to assure that the zeroing loop is dynamically stable. A second sample-and-hold could be added in series with the output to remove the output discontinuity.

Many variations of this scheme are possible to suit the individual system.

APPLICATION NO.11

Integrate-Hold-Reset



This circuit accurately computes the functions,

$$V_o = \int_{T_1}^{T_2} V_{in}\, dt$$

and holds the answer for further processing.

Resetting circuits for integrators have always been a practical design problem. The reset circuit must produce an extremely low leakage current across the integrating capacitor, and must produce a very low offset voltage when turned on. The circuit illustrated has excellent results since the leakage at the switch node is exceptionally low. R_C and C_C prevent oscillations during reset and their product should be at least 0.02 times R_I X C_I.

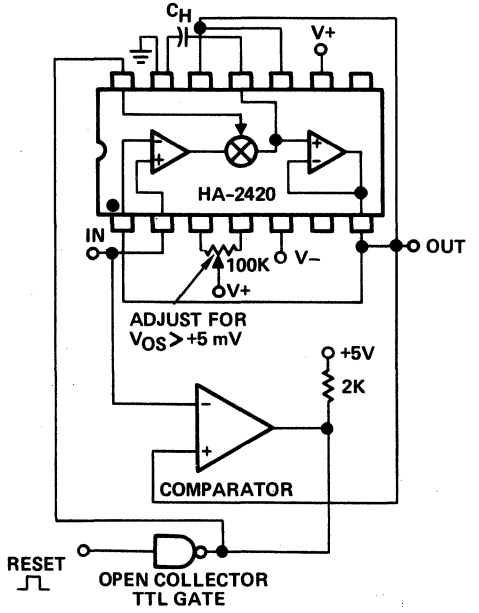
For the simpler integrate and reset function without a hold, substitute an ordinary operational amplifier for the upper device.

APPLICATION NO. 12

This accurate, low drift peak detector circuit combines the basic sample-and-hold connection with a comparator, and will detect 20V p-p signals up to 50kHz.

When the input signal level exceeds the voltage being stored in the S/H, the comparator trips, and a new sample of the input is taken. The S/H offset pot should be adjusted for a slight positive offset, so that the comparator will trip back when the new peak is acquired; otherwise the comparator would remain "on" and the S/H would follow the peak back down.

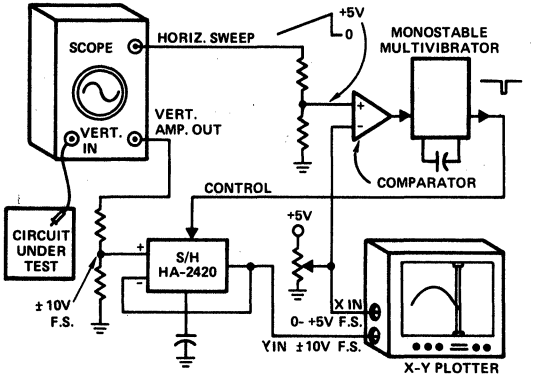
To make a negative peak detector, reverse the comparator inputs, and adjust the S/H for a negative offset.



The reset function, which is difficult to achieve in other peak detector circuits, forces a new sample at the instantaneous input level.

APPLICATION NO. 13

Plot High Speed Waveforms With Sampling Techniques



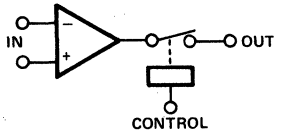
This useful application illustrates how fast repetitive waveforms can be slowed down using sampling techniques. The input signal is much too fast to be tracked directly by the X-Y recorder; but sampling allows the recorder to be driven as slow as necessary.

To operate, the waveform is first synched in on the scope. Then the potentiometer connected to the recorder X input is slowly advanced, and the waveform will be reproduced. The HA-2420 samples for a very short interval once each horizontal sweep of the scope. The sampling instant is determined by the potentiometer at the instant when the horizontal sweep waveform corresponds to the X position of the recorder.

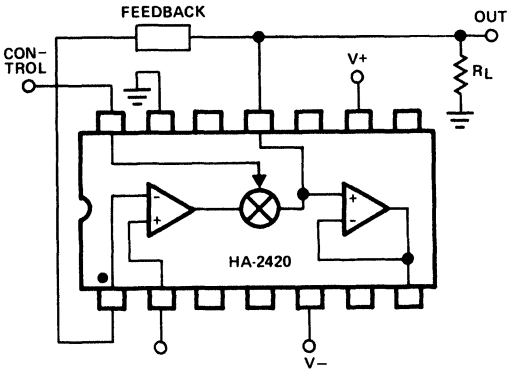
This principle can be applied to many systems for waveform analysis, etc.

APPLICATION NO. 14

Gated Operational Amplifier



EQUIVALENT CIRCUIT



The following are a few of the many applications where an operational amplifier followed by a highly efficient analog switch could be used:

Analog Multiplexer Element
Gated Oscillator
Precision Timing Circuit
Chopper Type Modulator/Demodulator
Crosspoint Switch Element
Reset or Initial Conditions Switch
Gated Comparator
Automatic Calibration Switch
Gated Voltage Regulator

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 518

THE HA-2900 MONOLITHIC CHOPPER STABILIZED AMPLIFIER

BY DON JONES and ROBERT W. WEBB

INTRODUCTION

An operational amplifier should ideally be selected so that, in a given application, performance to the required accuracy is determined only by the external networks. The amplifier should act like a pure, nearly infinite gain block; and not intrude its own personality on the overall circuit performance within the desired accuracy level.

Monolithic integrated circuit operational amplifiers have been quite successful in applications where total input inaccuracies of a few millivolts are acceptable. A new monolithic op amp, the HA-2900, is now available which allows about 100 times improvement in total accuracy.

For about thirty years, the chopper stabilized amplifier has been used when an op amp with the ultimate in DC performance was required. First it was constructed with vacuum tubes and mechanical relay choppers. More recently, it was made with discrete solid state devices in a module or hybrid package. It would be very desirable to achieve the same performance in a monolithic amplifier, with its compactness, higher reliability, and lower cost.

OFFSET VOLTAGE DRIFT

The one parameter which is probably the most troublesome to the monolithic operational amplifier design is offset voltage drift. This is also the most basic parameter for a DC amplifier – with zero volts differential input, the amplifier ought to have zero volts output. Input offset voltage (the small voltage which would be required between the input terminals to make the output actually go to zero volts) can generally be adjusted to a very low value using an external potentiometer or selected fixed resistors. The problem is that this adjustment is good only for the ambient temperature (and instant of time) at which it was made. With a few degrees of change in temperature or after a few months passage of time; the offset voltage may again become significant.

OFFSET CURRENT DRIFT

In many precision op amp specifications, there appears to be a tradeoff between offset voltage drift and offset current drift, each amplifier type being quite good in one category but only average in the other. For precision applications, both drift parameters should be low. For example, a FET input op amp with a quite respectable offset current drift of 10pA/°C, with balanced source resistances of 100K ohms, would have an additional offset voltage drift of 1.0μV/°C created by the offset current drift.

To maintain precision, the maximum practical source resistance will be determined by the offset voltage drift divided by the offset current drift. In the HA-2900, this computes to 130K ohms.

CHOPPER STABILIZATION

Stabilization of offset voltage in an amplifier can be accomplished by adding an auxiliary DC amplifier which may have very limited frequency response but which has very low offset voltage drift. In Figure 1, A1 is the main amplifier, and A2 the auxiliary. If the gain of A2 is large, the effective input offset

voltage of the entire circuit will be nearly that of A2 alone. This is because the input offset voltage of A1 is effectively divided by the gain of A2 in determining its contribution to the offset of the entire circuit. The open loop DC gain of the entire circuit is the product of the gains of A1 and A2.

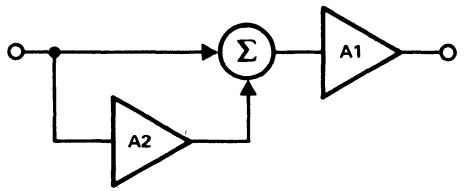


Figure 1

Figure 2 shows a classical chopper amplifier which is often used as an auxiliary DC amplifier. Chopper switch S1 functions as a modulator which changes the incoming DC level to an AC waveform with a proportional amplitude, and phase angle of either 0° or 180° depending on input polarity. The chopped signal is then amplified by an AC coupled amplifier. Ground level of the amplified signal is restored by a second chopper switch, S2, which may be regarded as a synchronous demodulator. Filtering then recreates an amplified replica of the incoming DC or low frequency signal.

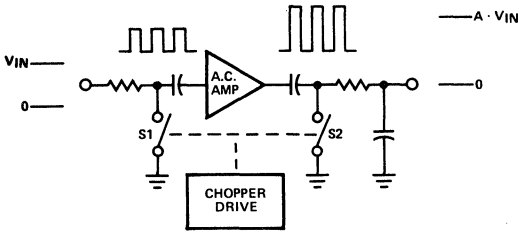


Figure 2

This circuit, properly constructed, will have extremely low offset voltage drift. The amplifier, being AC coupled, does not contribute to the DC offset. The most critical element is S1, since any coupling, DC or AC, of the drive signal to the contacts may introduce an offset error.

A different chopper amplifier concept is illustrated in Figure 3. This is a DC coupled amplifier scheme in which the amplifier periodically disconnects itself from the input signal and adjusts its offset voltage to zero. With S1 and S3 up, the circuit functions as a DC amplifier. When S1, S2, and S3 go down, the amplifier input is grounded and A2 forces the output of A1 to ground. S2, and C1 form a sample-and-hold, so that the correction signal to zero the offset of A1 is stored on C1 after S2 opens. S3, C2, and A3 form a second sample-and-hold, whose function is to store the previous output of A1, while self-zeroing is taking place, thereby removing most of the signal discontinuity.

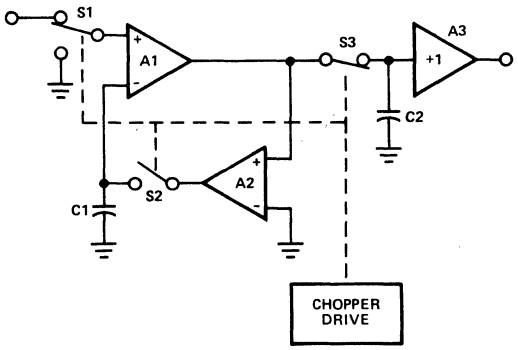


Figure 3

THE HA-2900

In choosing a candidate for monolithic integration, the second scheme (Figure 3) is more attractive, although the block diagram seems more complex. This scheme does not require large value resistors. It requires fewer external capacitors, and these have one end grounded, which allows use of a standard 8 pin can.

There are also performance advantages. The absence of coupling capacitors provides much faster recovery from overdriven conditions – a notorious problem with traditional chopper stabilized amplifiers. The response of the sample-and-hold filter is flat to one half the chopper frequency which greatly reduces settling times. Also, this scheme may be readily modified to provide a stabilized amplifier with full differential inputs; a highly desirable feature.

A diagram of the HA-2900 is shown in Figure 4. A1 is the main amplifier, and A2 is the auxiliary stabilizing amplifier. A3 is the sample-and-hold amplifier in the self-zeroing loop of A2, and A4 is the sample-and-hold amplifier which holds the previous signal during the zeroing interval.

One obvious difference between this diagram and those previously discussed is that the input circuitry is completely symmetrical with respect to the two input lines. This produces a true differential input, in contrast to most stabilized amplifiers which are designed either

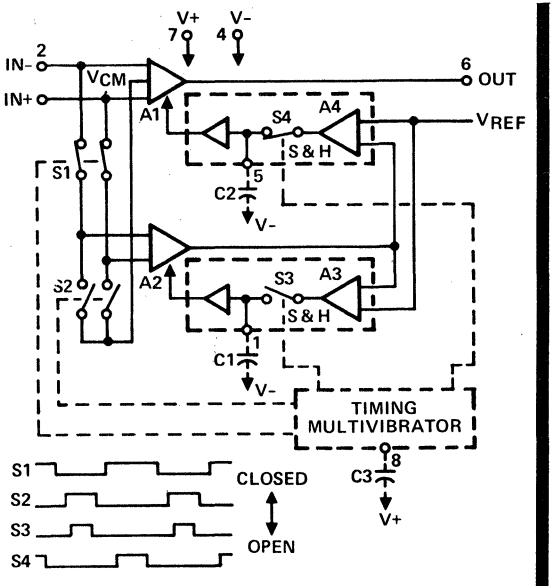


Figure 4

as inverting-only or as non-inverting amplifiers.

During the period in which A2 is stabilizing A1, S1 and S4 are closed while S2 and S3 are open. The DC and low frequency components of the input are amplified by A2 and applied as a correction signal to A1. The effective input offset voltage is nearly that of A2 alone.

To keep the offset voltage of A2 extremely low, it is periodically zeroed. S1 opens and S2 closes, disconnecting A2 from the input terminals and shorting the inputs of A2 together — not at ground level — but to a level equal to the input common mode voltage. This results in an extremely high common mode rejection ratio.

Like most other monolithic op amps, this device does not have a ground terminal; so when S3 closes, the output of A2 is forced to equal an internally generated reference voltage, rather than to ground. Since A4 is referenced to the same voltage, the result is the same. C2 charges to a level which will maintain the offset voltage of A2 at zero. In the meantime, S4 has opened, so that C1 maintains its previous level. The offset of A2 has now been zeroed and A2 then returns to its task of stabilizing A1.

Note that the opening and closing times of S1 through S4 are interleaved. This allows the transient spikes generated when a switch is opened or closed to settle out before other signal paths, which could be affected by these transients, are actuated. The timing multivibrator generates a triangular waveform (Figure 5). Different levels of this triangle are detected by four comparator circuits referenced to different points on a voltage divider to produce the four desired switch driving signals.

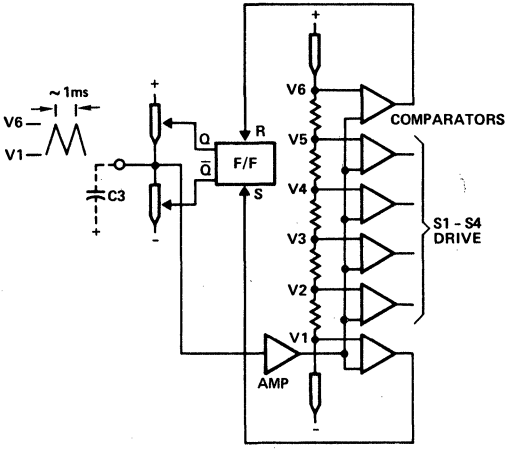


Figure 5

Switches S1 and S2 are each composed of two N-Channel MOSFET's which make excellent no-offset choppers for the low levels and low currents involved. S3 and S4 are complementary bipolar current switches, since appreciable current drive is required and offset voltage is not critical at these points (Figure 6).

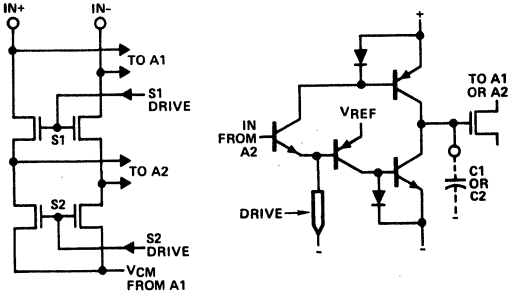


Figure 6

A1 and A2 are each N-Channel MOSFET input amplifiers, which produce the extremely low input currents (Figure 7). Normally, MOSFET's would not be suitable as DC amplifier input stages because of their high offset voltage drift; but chopper stabilization effectively removes that drift; while retaining their high input impedance advantage.

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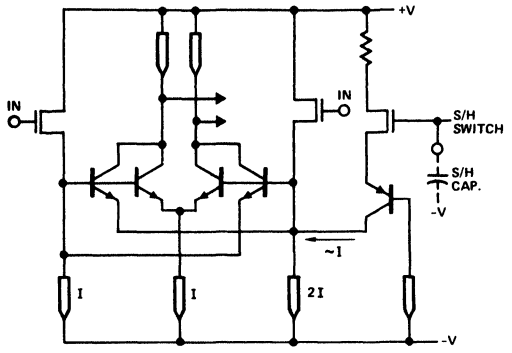

Figure 7

Single ended MOSFET input stages are used in the two sample-and-hold circuits as buffers to sense capacitor voltages. The correction signal from each sample-and-hold circuit alters a current generator which feeds one of the MOSFET sources in the inputs of A1 and A2.

The output stage of A1 is a conventional complementary bipolar follower with short circuit protection.

All of this complex circuitry boils down to the simple functional op amp block shown in Figure 8, packaged with the standard op amp pin-out in the standard TO-99 can. Three external capacitors are required for operation; one for multivibrator timing and two for the sample-and-holds.

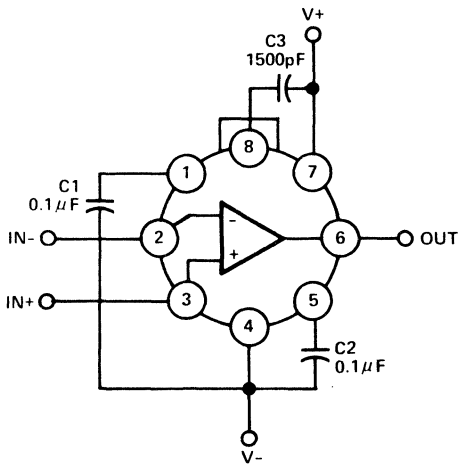

Figure 8

FABRICATION

The HA-2900 is an LSI linear device, containing 252 active elements on a chip measuring .093 X .123 inches.

The chip was designed using the dielectric isolation process, rather than the more conventional junction isolation process, for several reasons. A linear chip can usually be made smaller in dielectric isolation, both because of better packing density and because the high quality active elements can simplify the design — requiring fewer high value resistors and capacitors. The savings in chip area and the consequent higher yields mean that dielectric isolation can be used at little or no cost premium.

The factor which really makes a monolithic chopper stabilized amplifier practical is the high quality NPN, PNP, and FET elements which can be readily fabricated using dielectric isolation. The circuit designer has more freedom in the choice of transistors with desirable parameters, such as high frequency, high gain, vertical PNP transistors; and MOSFET's optimized for chopper service. The superior isolation between elements greatly reduce parasitic capacitance and prevents interaction or latchup due to unwanted four-layer devices. This also allows accurate circuit modeling — essential in a circuit of this complexity.

PERFORMANCE

Significant performance parameters of the HA-2900 are listed in Table 1. In addition to the superior DC parameters, bandwidth and slew rate are also quite respectable. The amplifier is stable, even as a unity gain follower, and exhibits a smooth, fast settling slewing waveform (Figure 9).

OFFSET VOLTAGE DRIFT:	0.2μV/°C
OFFSET CURRENT DRIFT:	1pA/°C
OPEN LOOP GAIN:	5 X 10^8
BANDWIDTH:	3MHz
SLEW RATE:	2.5V/μS
TRUE DIFFERENTIAL INPUTS	

Table I

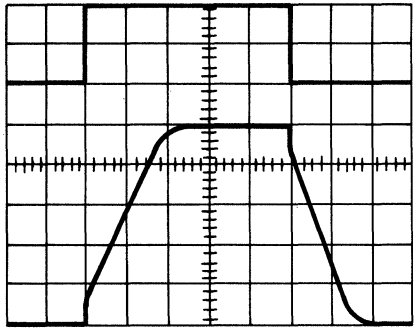

Figure 9

RANDOM NOISE CONSIDERATION

One of the more noticeable characteristics of the HA-2900, particularly when used in high gain circuits, is that the random noise level is 5 to 10 times higher than that seen with conventional bipolar input amplifiers. This is a result of a deliberate design tradeoff — offset current errors vs. noise.

Super gain bipolar input devices or JFET inputs would have lower noise, but have offset current drifts of about 10pA/°C, while the HA-2900 offset current drift is about 1pA/°C. The HA-2900, therefore, may be used with ten times higher input resistors than the other type amplifiers with the same drift errors due to offset current drift. The important applications fact in making this tradeoff is that noise can easily be averaged, allowing recovery of low level D.C. signals at the expense of response time; however, errors due to offset current drift in moderate to high impedance circuits cannot be recovered.

A curve of total equivalent input noise vs. bandwidth for the HA-2900 is shown in Figure 10. As an example of the use of this curve, suppose that we wished to resolve D.C. changes of 10 microvolts with the amplifier illustrated in Figure 11. From the curve, a maximum bandwidth of 0.6 Hz would be required, which could be achieved with C= .0027μF. Response time (10% to 90%) would be about 0.35 ÷ B.W., or about 0.6 seconds.

But suppose we need both fast response and low noise. This can be accomplished by utilizing the best characteristics of two operational amplifiers as illustrated in the applications section.

Synchronous noise generated by the choppers is primarily a common mode current noise, which can be minimized by matching the impedances at the two input terminals. With matched impedances up to 100 K ohms, the synchronous noise seen at the output is well below the random noise level; and the effect of random current noise is not discernable at this impedance level.

HA-2900 EQUIVALENT INPUT NOISE (peak-to-peak) AS A FUNCTION OF CLOSED LOOP BANDWIDTH

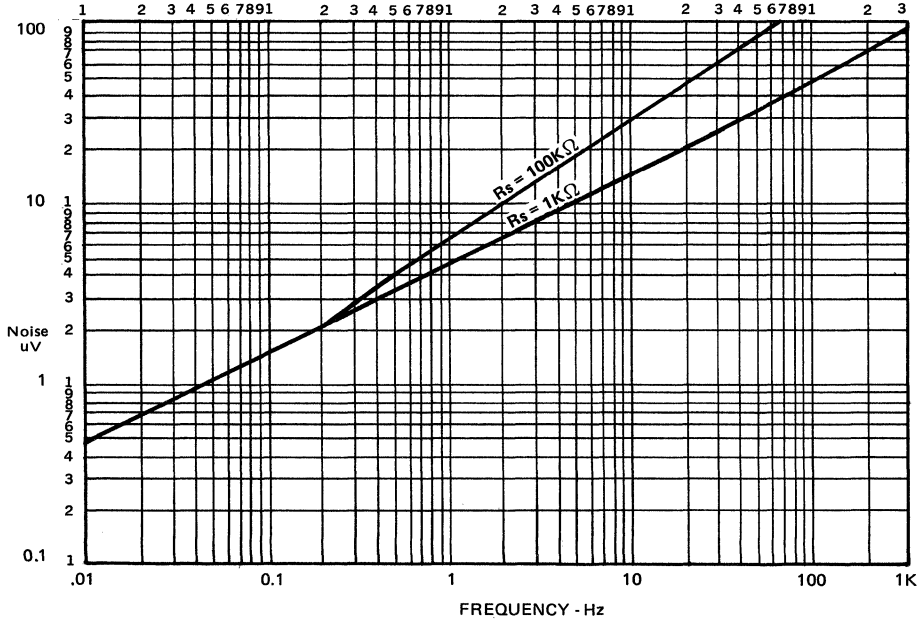

Figure 10

WHO NEEDS IT?

There are many applications, such as in precise analog computation and in precision DC instrumentation where the low drift of a chopper stabilized amplifier is obviously required.

There are many other applications where the need for this amplifier vs. the more conventional op amps is less obvious. The designer should ask himself these questions:

1. Are there assemblies which require a technician to adjust a pot or select resistors to zero an amplifier? What are the cost and reliability advantages in using an amplifier which requires no circuit adjustments? Trimmer pots are many times less reliable than a monolithic I.C.

2. Does the system require occasional recalibration because of amplifier drift with time? The chopper stabilized amplifier is actually a closed loop system – offset voltage is continuously monitored and adjusted to near zero.

3. Do assemblies ever have to be reworked because of excessive amplifier drift with temperature? In many amplifiers the drift specification may no longer be valid after zeroing. In many low drift amplifiers, the guaranteed drift specifications are not 100% measured by the manufacturer, so the burden of proof is left to the user.

4. Is the total system performance marginal because of the accumulation of errors? Would the error budget situation improve with the substitution of much more accurate op amps?

5. Is a complex analog-digital system under consideration, simply because of accuracy and drift problems associated with a simpler all analog system?

The decision on whether or not to use a chopper stabilized amplifier in these cases will depend on the analysis of the cost and performance tradeoffs in the individual situation. In any case, the knowledge that a solution is now available, should any of these problems arise, will remove some of the greatest worries of the linear systems designer.

APPLICATIONS

The HA-2900 may be used in virtually any of the hundreds of published operational amplifier applications.

Some care is required in the physical layout of the system to realize the full accuracy potential of an ultra-low drift amplifier. When mounted in a typical breadboard or P.C. card adequate for an ordinary op amp application, drifts on the order of 1μV/°C may be expected. If this is good enough, the designer need go no further. But to reach the ultimate device performance, the designer must take into account external effects. These include thermocouple and electrochemical EMF's generated at junctions of dissimilar metals (solder joints, connectors, internal junctions in resistors and capacitors), leakage across insulating materials, static charges created by moving air, and improper grounding and shielding practices. The main layout procedure is to insure that the networks going to the two amplifier inputs are identical and are at the same temperature.

Figure 11 shows a typical high gain amplifier application. Gain is 1,000; bandwidth is about 2 KHZ. Either input terminal may be grounded for inverting or non-inverting operation or the inputs may be driven differentially. The symmetrical networks at the device inputs are recommended for any of the three operating modes to eliminate chopper noise and yield the best drift characteristics. Total input noise, with C=0, is about 30μVRMS. This noise can be reduced, at the expense of bandwidth by adding capacitors as shown.

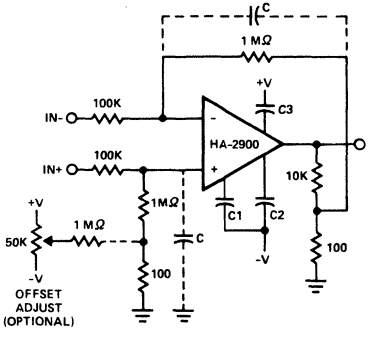

Figure 11

A high impedance differential instrumentation amplifier is shown in Figure 12. This well known configuration has excellent common mode rejection of ±10 volts common mode input signals. Protection diodes are included to prevent the device input terminals from exceeding either power supply.

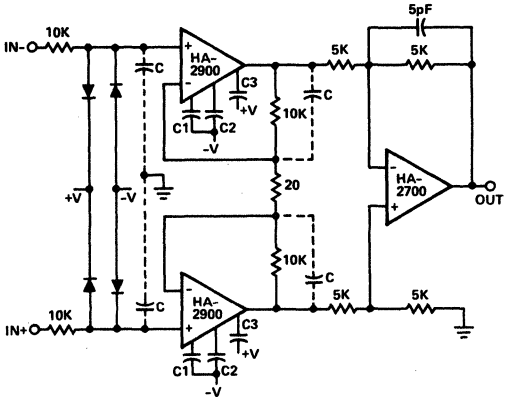

Figure 12

Integrators have been around as long as op amps, and are used in analog computation, active filters, timers, waveform generators, control systems, and A/D converters. An op amp for a precision integrator should have high gain, low offset voltage, low bias current, and wide bandwidth. So it is evident that the HA-2900 should make the best possible integrator (Figure 13). The gain of the HA-2900 allows accurate integration over eight decades of frequency. Dual slope A/D converters can now easily be made with six digit resolution.

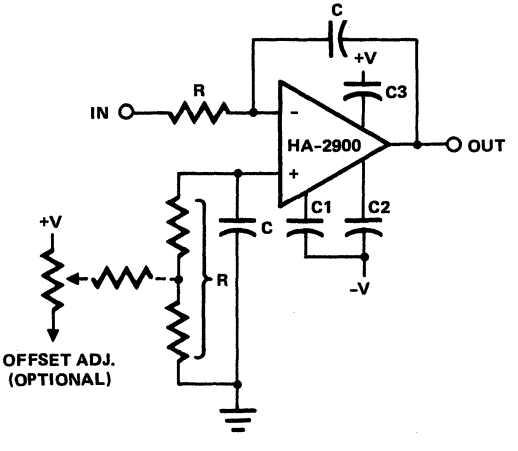

Figure 13

The composite amplifier combines the best performance of two different amplifier types. The exceptionally low drift characteristics of the HA-2900 may be added to another amplifier with wide bandwidth and high slew rate or low noise.

Figure 14 illustrates an excellent combination of characteristics for use wherever inverting amplifier applications are required. Features of the composite amplifier include: slew rate: 300V/μs, gain bandwidth product: 10-500 MHz, D.C. gain: 10^{13}, offset voltage drift: 0.3uV/°C, bias current drift: 50pA/°C, input noise (0-1 KHz): 5uV peak to peak.

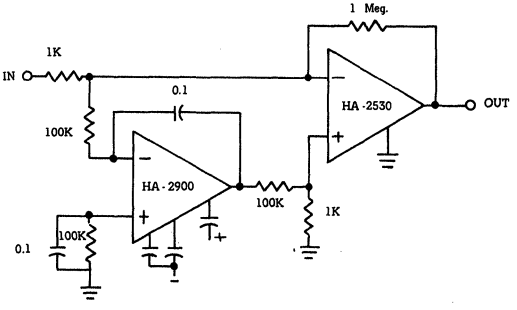

Figure 14

In most composite amplifiers, to avoid excessively long settling times or instabilities, it is preferable to match the 0 db response of the integrator to the open loop low frequency pole of the main amplifier. However, if the main amplifier has all of the characteristics, except for offset voltage drift, necessary to resolve the lowest required input change; it will be possible to operate the integrator at a much lower bandwidth, greatly reducing its noise contribution. The main amplifier must have very high gain, low bias current, low noise, and very small changes in offset voltage with output voltage changes. Then the integrator needs to remove only the essentially D.C. offset voltage of the main amplifier.

Figure 15 illustrates a hookup for non-inverting amplifier applications, which is useful from gains of unity up to several thousand. Gain — bandwidth product is 100 MHz. If the composite amplifier closed loop bandwidth exceeds the unity gain bandwidth of the HA-2900 (2.5MHz), then R and C should be added to suppress response peaks and pulse overshoot. Low frequency flicker noise is about 10μV peak to peak, caused chiefly by the HA-2620.

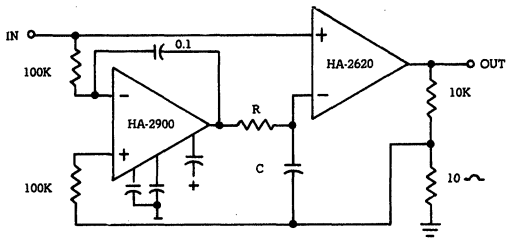

Figure 15

The circuit shown in Figure 16 where the integrator drives one of the offset adjust terminals of the main amplifier may be adapted to many amplifier types. This hookup has the advantages that the composite amplifier retains differential inputs, and may be used in any normal operational amplifier feedback configuration.

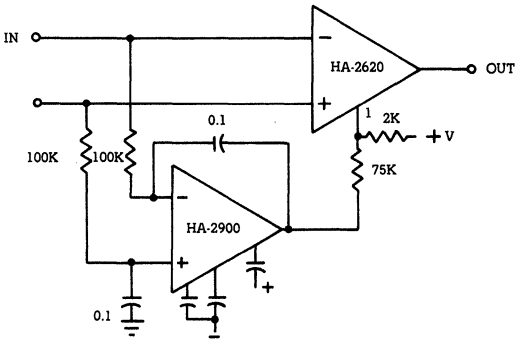

Figure 16

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 519

OPERATIONAL AMPLIFIER NOISE PREDICTION

BY RICHARD WHITEHEAD

INTRODUCTION

When working with op amp circuits an engineer is frequently required to predict the total RMS output noise in a given bandwidth for a certain feedback configuration. While op amp noise can be expressed in a number of ways, "spot noise" (RMS input voltage noise or current noise which would pass through 1Hz wide bandpass filters centered at various discrete frequencies), affords a universal method of predicting output noise in any op amp configuration.

THE NOISE MODEL

Figure 1 is a typical noise model depicting the noise voltage and noise current sources that are added together in the form of root mean square to give the total equivalent input voltage noise (RMS), therefore:

$$E_{ni} = \sqrt{e_{ni}^2 + I_{ni}^2 R_g^2 + 4KTR_g}$$ where,

E_{ni} is the total equivalent input voltage noise of the circuit.

e_{ni} is the equivalent input voltage noise of the amplifier.

$I_{ni}^2 R_g^2$ is the voltage noise generated by the current noise.

$4KTR_g$ expresses the thermal noise generated by the external resistors in the circuit where $K = 1.23 \times 10^{-23}$ joules/°K; $T = 300°K$ (27°C) and $R_g = \left(\frac{R_1 R_3}{R_1 + R_3}\right) + R_2$

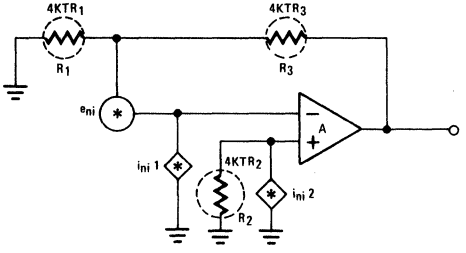

Figure 1

The total RMS output noise (E_{no}) of an amplifier stage with gain = G in the bandwidth between f_1 and f_2 is:

$$E_{no} = G\left(\int_{f1}^{f2} E_{ni}^2 df^{1/2}\right)$$

Note that in the amplifier stage shown, G is the non-inverting gain $\left(G = 1 + \frac{R_2}{R_1}\right)$ regardless of which input is normally driven.

PROCEDURE FOR COMPUTING

1. Refer to the voltage noise curves for the amplifier to be used. If the R_g value in the application is close to the R_g value in one of the curves, skip directly to step 6, using that curve for values of E_{ni}^2. If not, go to step 2.
2. Enter values of e_{ni}^2 in line (a) of the table below from the curve labeled "$R_g = 0\,\Omega$".
3. From the current noise curves for the

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amplifier, obtain the values of i_{ni}^2 for each of the frequencies in the table, and multiply each by R_g^2, entering the products in line (b) of the table.

4. Obtain the value of $4KTR_g$ from Figure 14, and enter it on line (c) of the table. This is constant for all frequencies. The $4KTR_g$ value must be adjusted for temperatures other than normal room temperature.

5. Total each column in the table on line (d). This total is E_{ni}^2.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2					
(b) $i_{ni}^2R_g^2$					
(c) $4KTR_g$					
(d) E_{ni}^2					

6. On linear scale graph paper enter each of the values for E_{ni}^2 vs. frequency. In most cases, sufficient accuracy can be obtained simply by joining the points on the graph with straight line segments.

7. For the bandwidth of interest, calculate the area under the curve by adding the areas of trapezoidal segments. This procedure assumes a perfectly square bandpass condition; to allow for the more normal -6db/octave bandpass skirts, multiply the upper (-3db) frequency by 1.57 to obtain the effective bandwidth of the circuit, before computing the area. The total area obtained is equivalent to the square of the total input noise over the given bandwidth.

8. Take the square root of the area found above and multiply by the gain (G) of the circuit to find the total Output RMS noise.

A TYPICAL EXAMPLE

It is necessary to find the output noise of the circuit shown below between 1KHz and 24KHz.

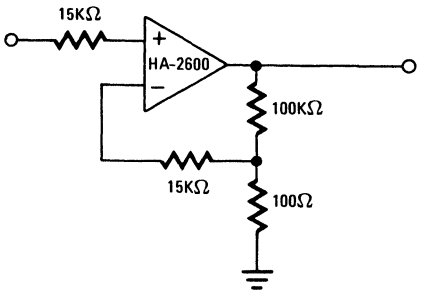
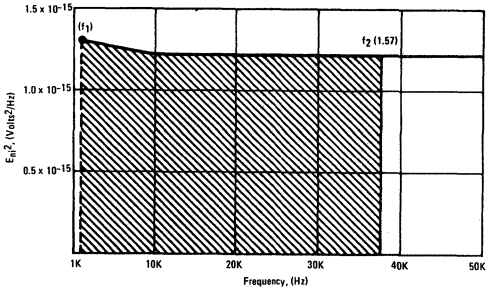


Figure 2
The HA-2600 In a Typical G = 1000 Circuit

Values are selected from Figures 5, 5a and 14 to fill in the table as shown below. An R_g of 30KΩ was selected.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2	3.6×10^{-15}	1.156×10^{-15}	7.84×10^{-16}	7.29×10^{-16}	7.29×10^{-16}
(b) $i_{ni}^2R_g^2$	9.9×10^{-16}	1.89×10^{-16}	3.15×10^{-17}	7.2×10^{-18}	7.2×10^{-18}
(c) $4KTR_g$	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}
(d) E_{ni}^2	5.09×10^{-15}	1.86×10^{-15}	1.31×10^{-15}	1.23×10^{-15}	1.23×10^{-15}

The totals of the selected values for each frequency is in the form of E_{ni}^2. This should be plotted on linear graph paper as shown below:



HA-2600 Total Equivalent Input Noise Squared

Since a noise figure is needed for the frequency of 1KHz to 24KHz, it is necessary to calculate the effective bandwidth of the circuit. With AV = 60db the upper 3db point is approximately 24KHz. The product of 1.57 (24KHz) is 37.7KHz and is the effective bandwidth of the circuit.

The shaded area under the curve is approximately 45 x 10^{-12} $Volts^2$; the total equivalent input noise is $\sqrt{E_{ni}^2}$ or 6.7 microvolts, and the total output noise for the selected bandwidth is $\sqrt{E_{ni}^2}$ x (closed loop gain) or 6.7 millivolts RMS.

ACTUAL MEASUREMENTS FOR COMPARISON

The circuit shown below was used to actually measure the broadband noise of the HA-2600 for the selected bandwidth:

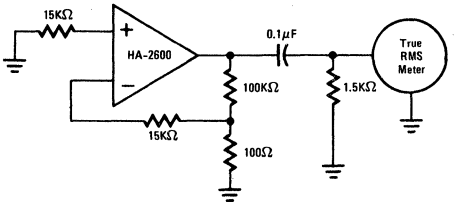


Figure 3
A Typical Test Circuit for Broadband Noise Measurements

The frequencies below the f_1 point of the bandwidth selected are filtered out by the RC network on the output of HA-2600. The measurement of the broadband noise is observed on the true RMS voltmeter. The measured output noise of the circuit is 4.7 millivolts RMS as compared to the calculated value of 6.7 microvolts RMS.

ACQUIRING THE DATA FOR CALCULATIONS

Spot noise values must be generated in order to make the output noise prediction. The effects of "Popcorn" noise have been excluded due to the type of measurement system.

The Quan-Tech Control Unit, model no. 2283 and Filter Unit, model no. 2181 were used to acquire spot noise voltage values expressed in ($V\sqrt{Hz}$). The test system performs measurements from 10Hz by orders of magnitude to 100KHz with an effective bandwidth of 1Hz at each tested frequency.

Several source resistance (R_g) values were used in the measuring system to reveal the effects of R_g on each type of Harris' op amps and to obtain proper voltage noise values essential for current noise calculations.

A DISCUSSION ON "POPCORN" NOISE

"Popcorn" noise was first discovered in early 709 type op amps. Essentially it is an abrupt step-like shift in offset voltage (or current) lasting for several milliseconds and having amplitude from less than one microvolt to several hundred microvolts. Occurance of the "pops" is quite random — an amplifier may exhibit several "pops" per second during one observation period and then remain "popless" for several minutes. Worst case conditions are usually at low temperatures with high values of R_g. Some amplifier designs and some manufacturer's products are notoriously bad in this respect. Although theories of the popcorn mechanism differ, it is known that devices with surface contamination of the semiconductor chip will be particularly bad "poppers". Advertising claims notwithstanding, the authors have never seen any manufacturer's op amp that was completely free of "popcorn". Some peak detector circuits have been developed to screen devices for low amplitude "pops", but 100% assurance is impossible because an infinite test time would be required. Some studies have shown that spot noise measurements at 10Hz and 100Hz, discarding units that are much higher than typical, is an effective screen for potentially high "popcorn" units.

The vast majority of Harris op amps will exhibit less than 3 μV peak-to-peak "popcorn". Screening can be performed, but it should be noted that the confidence level of the screen could be as low as 60%.

REFERENCES

Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design. New York: John Wiley and Sons, 1973.

Instruction Manual, Model 2173C Transistor Noise Analyzer Control Unit. Quan-Tech, Division of KMS Industries. Whippany, New Jersey.

TYPICAL SPOT NOISE CURVES

Unless Otherwise Noted:
$V_S = \pm 15V$ $T_A = +25^oC$

Figure 1

HA-901/911 INPUT NOISE VOLTAGE

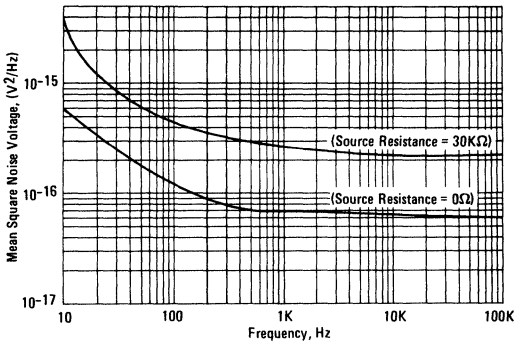


Figure 1A

HA-909/911 INPUT NOISE CURRENT

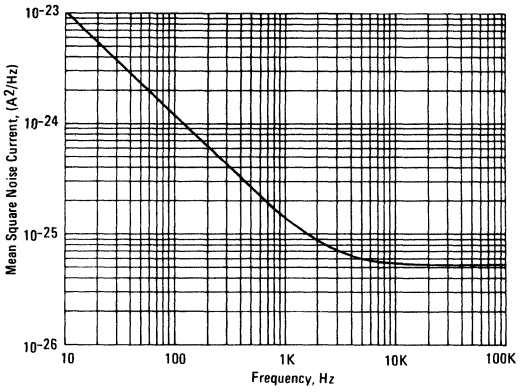


Figure 2

HA-2000/2005 INPUT NOISE VOLTAGE

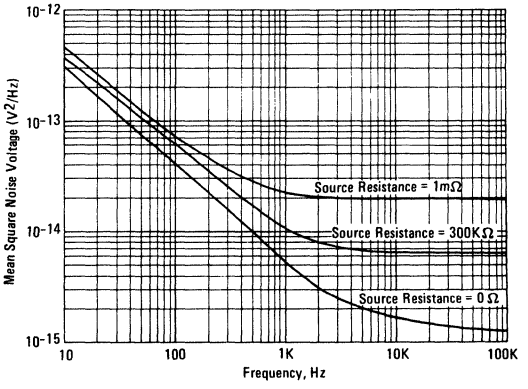


Figure 2A

HA-2000/2005 INPUT NOISE CURRENT

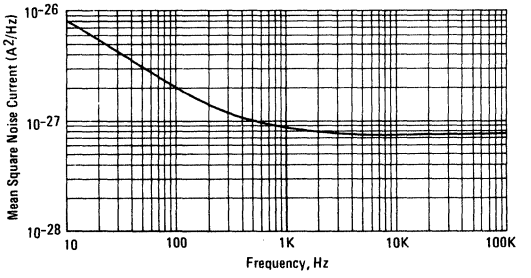


Figure 3

HA-2050/2055 INPUT NOISE VOLTAGE

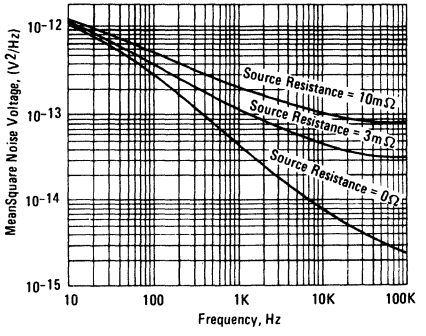


Figure 3A

HA-2050/2055 INPUT NOISE CURRENT

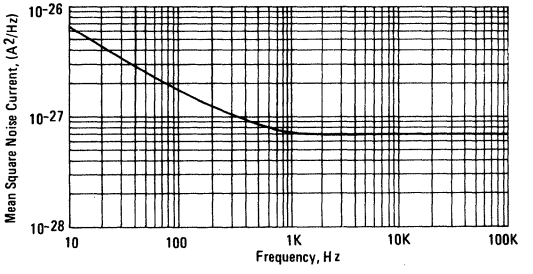


Figure 4

HA-2060/2065 INPUT NOISE VOLTAGE

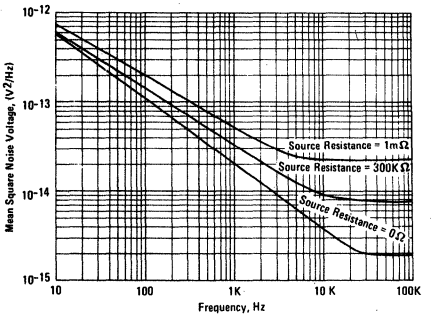


Figure 4A

HA-2060/2065 INPUT NOISE CURRENT

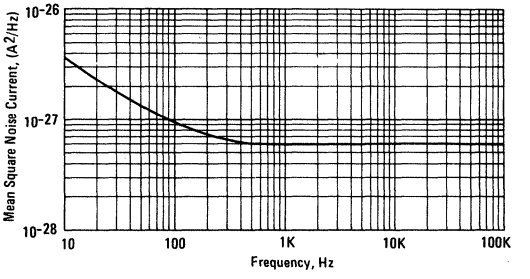


Figure 5

HA-2400 INPUT NOISE VOLTAGE

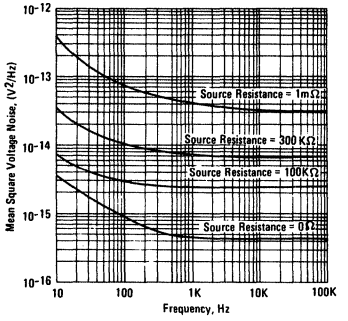


Figure 5A

HA-2400 INPUT NOISE CURRENT

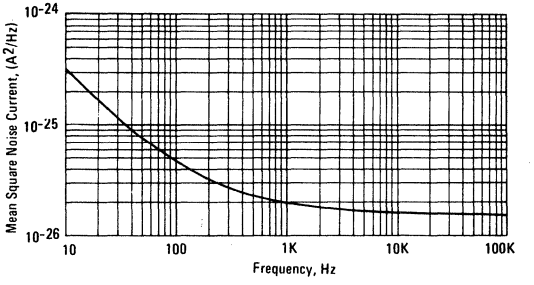


Figure 6

HA-2500/2510/2520 INPUT NOISE VOLTAGE

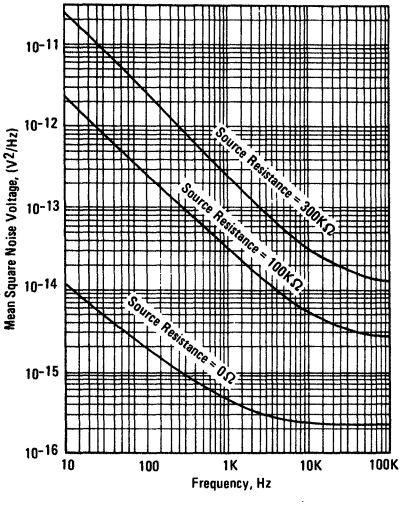


Figure 6A

HA-2500/2510/2520 INPUT NOISE CURRENT

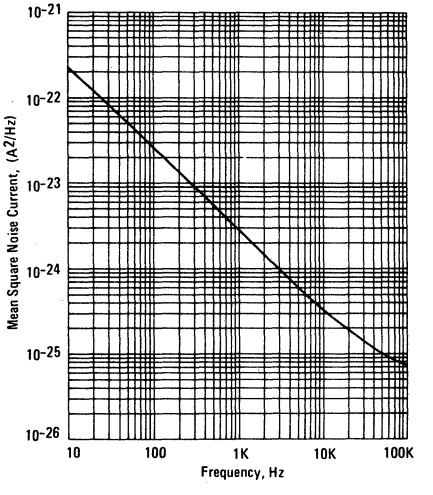


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Figure 7

HA-2530/2535 NOISE VOLTAGE

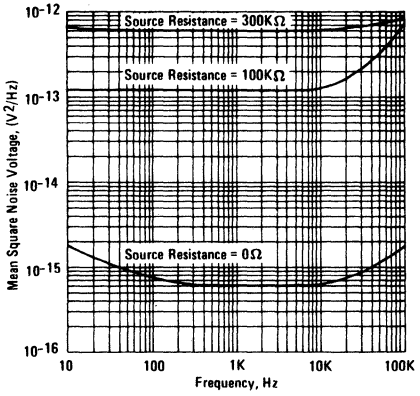

Figure 7A

HA-2530/2535 NOISE CURRENT

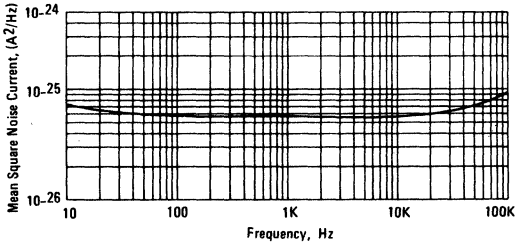

Figure 8

HA-2600/2620 INPUT NOISE VOLTAGE

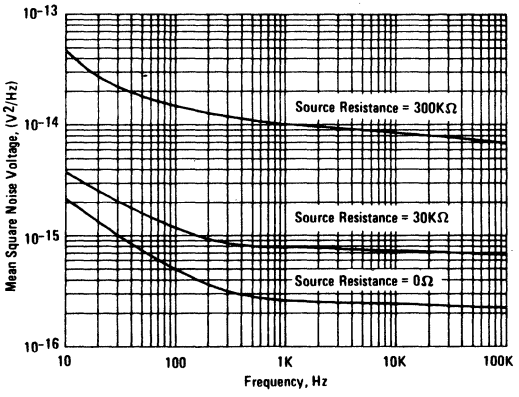

Figure 8A

HA-2600/2620 INPUT NOISE CURRENT

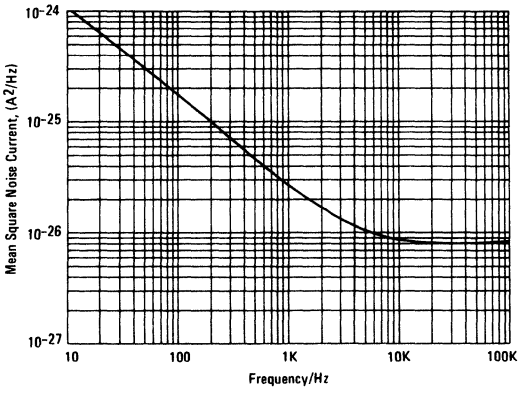

Figure 9

HA-2640/2645 INPUT VOLTAGE NOISE ($V_S = \pm 30V$)

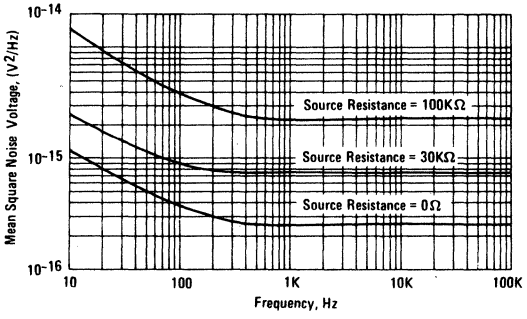

Figure 9A

HA-2640/45 INPUT NOISE CURRENT ($V_S = \pm 30V$)

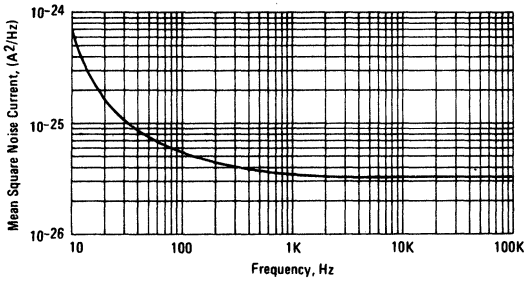

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Figure 10

HA-2700 INPUT NOISE VOLTAGE

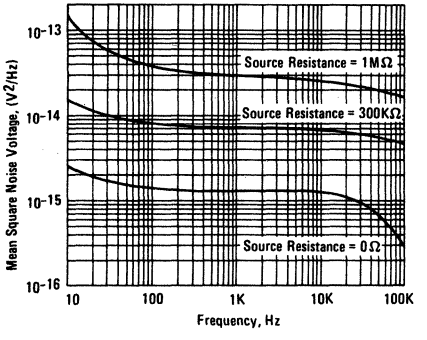

Figure 10A

HA-2700 INPUT NOISE CURRENT

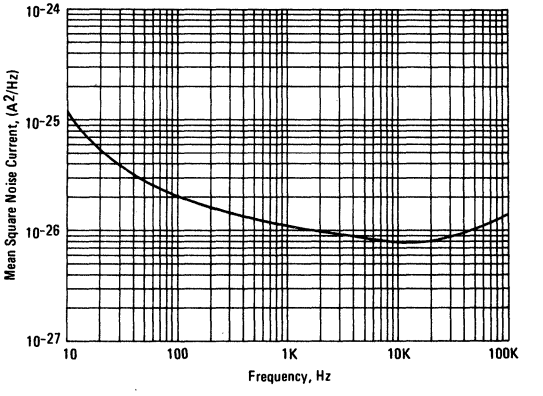

Figure 11

HA-2720/2730 INPUT NOISE VOLTAGE (I_{SET} = 1μA)

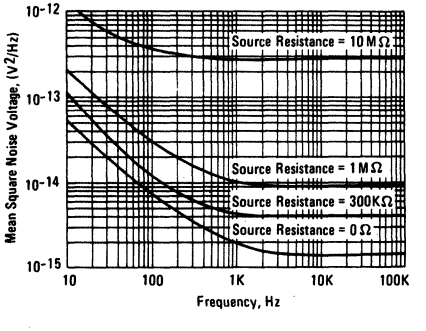

Figure 11A

HA-2720/2730 INPUT NOISE CURRENT (I_{SET} = 1μA)

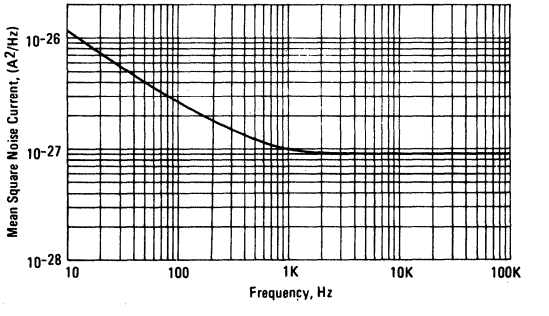

Figure 12

HA-2720/2730 INPUT NOISE VOLTAGE (I_{SET} = 10μA)

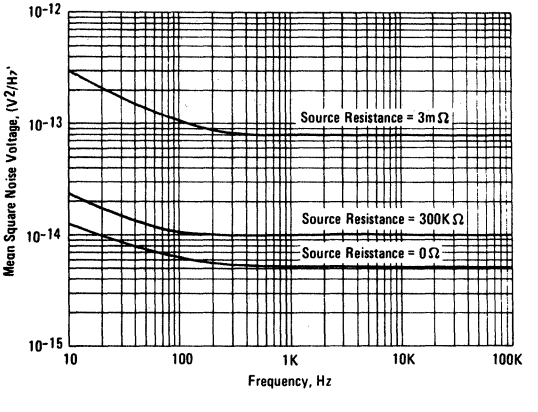

Figure 12A

HA-2720/2730 INPUT NOISE CURRENT (I_{SET} = 10μA)

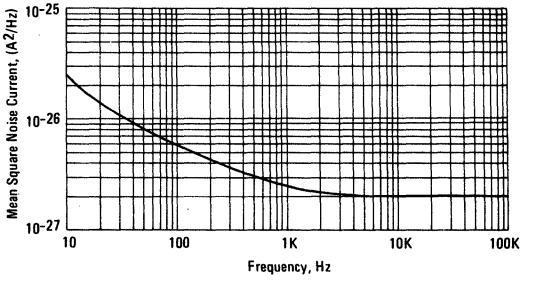

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Figure 13

HA-2720/2730 INPUT NOISE VOLTAGE (I_{SET} = 100μA)

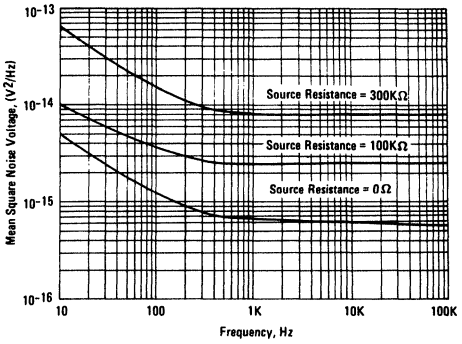

Figure 13A

HA-2720/2730 INPUT NOISE CURRENT (I_{SET} = 100μA)

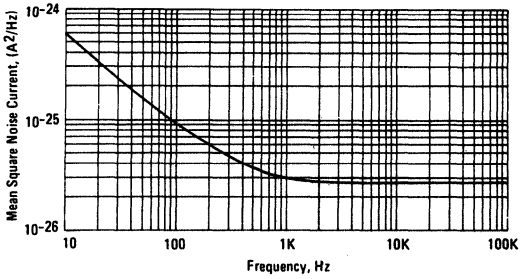

Figure 14

HA-4600/4602/4605 INPUT NOISE VOLTAGE

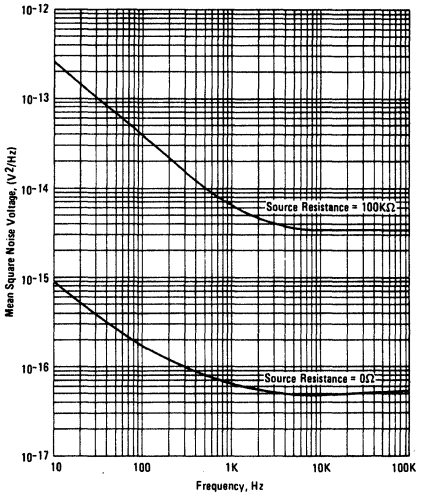

Figure 14A

HA-4600/4602/4605 INPUT NOISE CURRENT

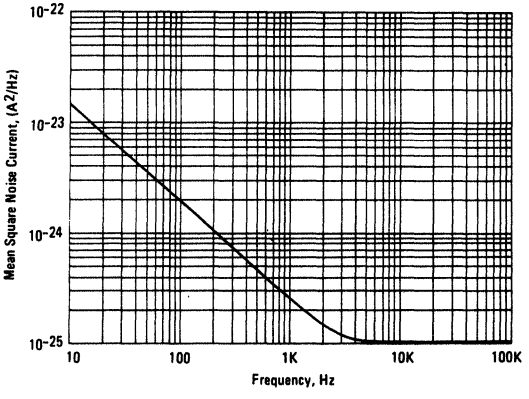

Figure 15

HA-4741 INPUT NOISE VOLTAGE

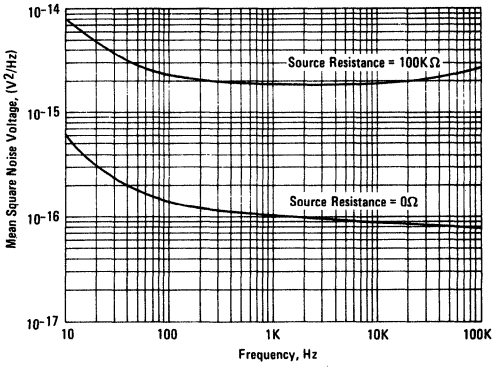

Figure 15A

HA-4741 INPUT NOISE CURRENT

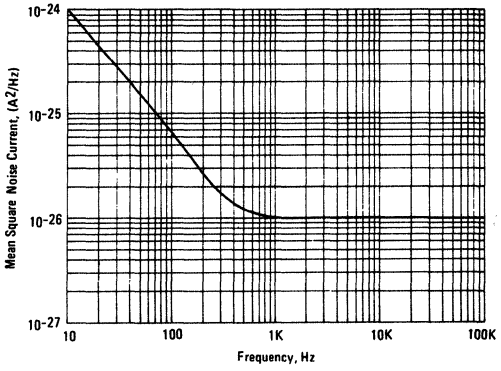

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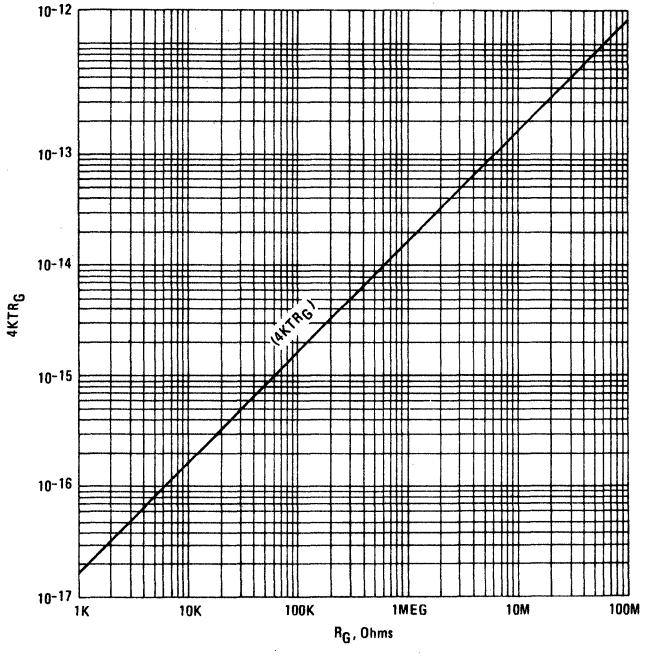
Figure 16


10-12
10-13
10-14
10-15
10-16
10-17
4KTRG
(4KTRG)
1K
10K
100K
1MEG
10M
100M
RG, Ohms

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 520

CMOS ANALOG MULTIPLEXERS AND SWITCHES; APPLICATIONS CONSIDERATIONS

BY DON JONES

INTRODUCTION

This paper is a mixed collection of answers to questions most frequently asked about CMOS analog multiplexers and switches. It covers selection criteria, parameter definitions, handling and design precautions, typical applications, and special topics such as transient considerations and R.F. switching. Some other devices which perform analog switching functions in particular applications are also discussed.

As a complement to this paper, the article, "Getting the Most Out of CMOS Devices for Analog Switching Jobs" by Ernie Thibodeaux, Electronics, December 25, 1975 is recommended reading for any analog CMOS user (reprinted in Application Note 521). This discusses the different CMOS processes used by various manufacturers, showing the performance trade-offs and particularly the different failure modes which may be encountered.

CHOOSING THE RIGHT DEVICE

A. MULTIPLEXERS: PROTECTED OR UNPROTECTED?

Harris overvoltage protected multiplexers, HI-506A/507A/508A/509A are designed for failure-proof operation in a common class of applications: any system in which the analog input signal lines originate external to the equipment. This includes most data acquisition, telemetry, and process control systems. Overvoltage protection is necessary because the signal lines are commonly subject to a number of potentially destructive situations.

1. Analog signals may be present while the MUX power supplies are off.
2. The signal lines may receive induced voltage spikes from nearby sources.
3. Static electricity may be introduced on the signal lines by personnel or equipment.
4. Grounding problems are frequent; A.C. power line voltages at high impedance can appear on the signal lines. Signal lines can be accidentally shorted to other voltage sources.

Harris protected type multiplexers will withstand a continuous voltage on any one input of ±20 Volts greater than either supply (this limitation is due only to temperature rise considerations at maximum ambient) and have withstood simulated static discharge conditions of greater than 1000 Volts.

It should be emphasized that only the HI-506A through 509A (and exact equivalents from authorized alternate suppliers) will have this kind of protection necessary for inputs from the outside world. Certain CMOS process improvements, such as "floating body" and "buried layer" do help minimize one failure mode (latchup) but will still fail under excess voltage or current conditions prevalent in this type application.

Conventional CMOS multiplexers can be protected against overvoltage destruction by external resistor-diode networks to limit input current to a safe level, but it is difficult to prevent another phenomenon with overvoltage; normally-off switching elements will tend to switch on, due to parasitic bipolar transistors in the CMOS structure, so the overvoltage spike will appear at the multiplexer output. The Harris internal protection circuits eliminate the problem by automatically shutting off the parasitic transistor during overvoltage conditions.

A simplified equivalent circuit of the Harris internal protection network is shown in Figure 1.

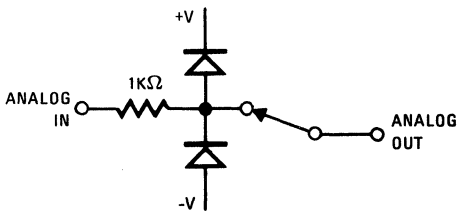


Figure 1

This will help answer the question of what happens when the supplies are turned off, but input signals are present. If the supplies are shorted to ground, then the inputs will have about 1KΩ impedance to ground. If the supplies are open circuit, then the most positive and most negative inputs will act as supplies to the multiplexer.

In normal operating parameters, internally protected multiplexers have one difference from the unprotected versions—ON resistance is necessarily higher because of the added series current limiting resistor. However, to achieve the same degree of protection with conventional devices, the same resistance must be added externally, plus external diodes which would add to the effective leakage currents.

Conventional unprotected multiplexers are suitable for systems where the MUX inputs come from sources within the equipment, such as from op amps powered by the same ±15 Volt supplies. The HI-506/507/1818A/1828A are intended for this type system. They are entirely free of any latch-up tendency, which have plagued some other types, even in these more benign applications. They are also free of the performance compromises which have accompanied some attempts to cure the latch-up problem.

B. WHICH SWITCH TO SWITCH TO?

Harris furnishes a complete line of CMOS analog switches, including replacements for most of the available CMOS and JFET switches. All types feature rugged no-latch-up construction, uniform characteristics over the analog signal range, and excellent high frequency characteristics.

The HI-200 and HI-201 replace the popular, low cost DG200 and DG201 types dual and quad switches.

The HI-1800A is a low leakage dual DPST switch with a versatile addressing scheme, allowing use of a single type for many different switching functions.

The HI-5040 through HI-5051 are low resistance types, offering one to four switches in virtually all combinations. These replace the IH-5040 series with significantly better performance, and with both 75 ohm and 30 ohm switches available in all configurations. These are also plug-in replacements for many of the DG180 and DG190 series of FET hybrid switches, offering the advantage of monolithic construction, but with slightly longer switching times.

The analog switches do not contain overvoltage protection on the analog inputs, although they will withstand inputs 2 or 4 Volts greater than the supplies. External current limiting should be provided if higher overvoltages are anticipated, such as a resistor in series with the analog input of value: R(ohms) $\geq$ (V_{IN} -V_{SUPPLY}) x 50 where V_{IN} is the maximum expected input voltage. All digital inputs do have overvoltage/static charge protection.

DATA SHEET DEFINITIONS

A. ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, these are maximum conditions which may be applied to a device (one at a time) without resulting in permanent damage. The device may, or may not, operate satisfactorily under these conditions—conditions listed under "Electrical Characteristics" are the only ones guaranteed for satisfactory operation.

B. V_S, ANALOG SIGNAL RANGE

The input analog signal range over which reasonably accurate switching will take place. For supply voltages lower than nominal, V_S will be equal to the voltage span between the supplies. Note that other parameters such as R_{ON} and leakage currents are guaranteed over a smaller input range, and would tend to degrade towards the V_S limits. All Harris devices can withstand $+V_S$ applied at an input while $-V_S$ is applied to the output (or vice-versa) without switch breakdown—this is not true for some other manufacturers' devices.

C. R_{ON}, ON RESISTANCE

The effective series on-switch resistance measured from input to output under specified conditions. Note that R_{ON} changes with temperature (highest at high temp.) and to a lesser degree with signal voltage and current.

D. $I_S(OFF)$, $I_D(OFF)$, $I_D(ON)$: LEAKAGE CURRENTS

Currents measured under conditions illustrated on data sheet. Harris prefers to guarantee only worst-case high temperature leakages, because room temperature picoampere levels are virtually impossible to measure repeatably on available automated test equipment. Even under laboratory conditions, fixture and test equipment stray leakages may frequently exceed the device leakage. Leakages tend to double every 10°C temperature rise, so it is reasonable to assume that the +25°C figure is about .001 times the +125°C measurement; however, in some cases there may be ohmic leakages, such as on the package surface, which would make the +25°C reading higher than calculated.

Each of these leakage figures is the algebraic sum of all currents at the point being measured: to each power supply, to ground, and through the switches; so the current direction cannot be predicted. In making an error analysis it should be assumed that all leakages are in the worst-case direction.

In most systems, $I_D(ON)$ has the most effect, creating a voltage offset across the closed switch equal to $I_D(ON) \times R_{ON}$.

E. V_{AL}, V_{AH}; INPUT THRESHOLDS

The lower and upper limits for the digital address input voltage at which the switching action takes place. All other parameters will be valid if all "0" address inputs are less than V_{AL} and all "1" inputs are greater than V_{AH}. Logic compatibility will be discussed in detail later in this paper.

F. I_A, INPUT LEAKAGE CURRENT

Current at a digital input, which may be in either direction. Digital inputs on Harris devices are similar to CMOS logic inputs; connection to MOS gates through resistor-diode protection networks. Unlike some other devices, there is no DC negative resistance region which could create an oscillating condition.

G. T_A, T_{ON}, T_{OFF}; ACCESS TIME

The logic delay time plus output rise time to the 90% point of a full scale analog output swing. After this time the output will continue to rise, approaching the 100% point on an exponential curve determined by $R_{ON} \times C_D(OFF)$.

H. T_{OPEN}, BREAK-BEFORE-MAKE DELAY

The time delay between one switch turning OFF and another switch turning ON; both switches being commanded simultaneously. This prevents a momentary condition of both switches being ON, generally a very minor problem.

I. $C_S(OFF)$, $C_D(OFF)$, $C_D(ON)$ INPUT/OUTPUT CAPACITANCE

Capacitance with respect to ground measured at the analog input/output terminals. $C_D(ON)$ is generally the sum of $C_S(OFF)$ and $C_D(OFF)$. $C_D(OFF)$ is usually the most important term as rise time/settling characteristics are determined by $R_{ON} \times C_D(OFF)$, as well as the high frequency transmission characteristics.

J. $C_{DS}(OFF)$, DRAIN TO SOURCE CAPACITANCE

The equivalent capacitance shunting an open switch.

K. OFF ISOLATION

The proportion of a high frequency signal applied to an open switch input appearing at the output: off isolation = 20 log $\frac{V_{IN.}}{V_{OUT}}$ This feedthrough is transmitted through $C_{DS}(OFF)$ to a load composed of $C_D(OFF)$ in parallel with the external load. The isolation generally decreases by 6dB/octave with increasing frequency.

L. C_A, DIGITAL INPUT CAPACITANCE

Capacitance to ground measured at digital input. This chiefly affects propagation delays when driven by CMOS logic.

M. P_D, POWER DISSIPATION: I+, I-

Quiescent power dissipation, $P_D = (V+ \times I+) + (V- \times I-)$. This may be specified both operating and standby ("Enable" pin ON/OFF). Note that, as with all CMOS devices, dissipation increases with switching frequency; but that Harris devices exhibit much less of this effect.

CARE AND FEEDING OF MULTIPLEXERS AND SWITCHES

Dielectrically isolated CMOS I.C.'s require no more care in handling and use than any other semiconductor—bipolar or otherwise. However, they are not indestructible, and reasonable common sense care should be taken.

In a laboratory breadboard, power should be shut off before inserting or removing any I.C.. It is especially important that supply lines have decoupling capacitors to ground permanently installed at the I.C. socket pins, as intermittent supply connections can create high voltage spikes through the inductance of a few feet of wire.

Because each of the major manufacturers of CMOS multiplexers and switches uses a radically different process, it is urged that units from all prospective suppliers be equally tested in breadboards and prototypes. It will be interesting to note which types survive best the hazards of a few weeks of breadboard testing.

Particular care of semiconductors during incoming inspection and installation is quite important, because the cost of reworking finished assemblies with even a small percentage of preventable failures can seriously erode profits. All equipment should be periodically inspected for proper grounding. With these devices, it is not usually necessary to shackle personnel to the nearest water pipe, if reasonable attention is paid to clothing and floor coverings; but be alert for periods of unusually high static electricity. If special lines are already set up for handling MOS devices, it wouldn't hurt to use them.

There are a few good rules for P.C. card layout:

1. Each card or removable subassembly should contain decoupling capacitors for each supply line to ground. This not only helps keep noise away from the analog lines, but gives good protection from static electricity damage when loose cards are handled.
2. When digital inputs come through a card connector, the pull-up resistor should be at the CMOS input. This forces current through the connector and prevents possible dry circuit conditions (see following discussion on digital interface).
3. All unused digital inputs must be tied to logic "0" (ground) or logic "1" (logic supply or

device + supply) depending on truth table and action desired. Open inputs tend to oscillate between "0" and "1". It would also be best to ground any unused analog inputs/outputs and any uncommitted device pins.

DIGITAL INTERFACE

A. REFERENCE CONNECTION

HI-5040 through HI-5051 and HI-1800A/1818A/1828A require a connection to the digital logic supply (+5V to +15V).

The HI-200/201/506A/507A have V_{REF} pins which are normally left open when driving from +5 Volt logic (DTL or TTL), but may be connected to higher logic supplies (to +15V) to raise the threshold levels when driving from CMOS or HNIL. The HI-200/201 will have significantly lower power dissipation when V_{REF} is connected to a high level supply.

The HI-506/507/508A/509A do not have V_{REF} terminals, but will operate reliably with any logic supplied from +5 to +15 Volts.

B. DTL/TTL INTERFACE

One major difference found in comparisons of similar devices from different manufacturers is the worst-case digital input high threshold (V_{AH} or V_{IH}). These range anywhere from +2V to +5V; and anything greater than +2.4V is obviously not compatible with worst-case TTL output levels. The fact is that no CMOS input is truly TTL compatible unless an external pull-up resistor is added. TTL output stages were not designed with CMOS loads in mind.

The experienced designer will always add a pull-up resistor from the CMOS input to the +5 Volt supply when driving from TTL/DTL:

1. Interchangeability: allows subsititution of similar devices from several manufacturers.
2. Noise immunity: a TTL output in the "high" condition can be quite high impedance. Even when voltage noise immunity seems satisfactory, the line is quite susceptible to induced noise. The pull-up resistor will reduce the impedance while increasing voltage noise immunity.
3. Compatibility: one manufacturer does guarantee +2.0 Volt minimum V_{AH}. However, this is accomplished with circuitry that is anything but TTL compatible: input current vs. voltage shows an abrupt positive then negative resistance region which is not the kind of load recommended for an emitter follower stage. A pull-up resistor will swamp out the negative resistance. Other CMOS inputs capacitively couple internal switching spikes to the input which could cause double-triggering without the pull-up resistor.
4. Reliability: it shouldn't happen with carefully processed I.C.'s; but any possible long term degradation of CMOS devices usually involves threshold voltage shifts. The pull-up resistor will help maintain operation if input thresholds drift out of spec. On units without adequate input protection, the resistor will also help protect the device when a loose P.C. card is handled. Where the interface goes through a P.C. connector, the resistor will force current through the connector to break down any insulating film which otherwise might build up and cause erratic dry circuit operation.

   A 2K ohm resistor connected from the CMOS input to the +5 Volt supply is adequate for any TTL type output. If power consumption is critical, open collector TTL/DTL should be used, allowing a higher value resistor—the voltage drop across the resistor is computed from the sum of specified "1" level leakage currents at the TTL output and CMOS input.

C. CMOS INTERFACE

The digital input circuitry on all Harris devices is identical to series 4000 and 54C/74C logic inputs, and is compatible with CMOS logic with supplies between +5V and +15V without external pull-up resistors.

D. ELECTROMECHANICAL INTERFACE

When driving inputs from mechanical switches or relays, either a pull-up or pull-down resistor must be connected at the CMOS input to clear the dry circuit and damp out any spikes, as illustrated in Figure 2, (b) and (c).

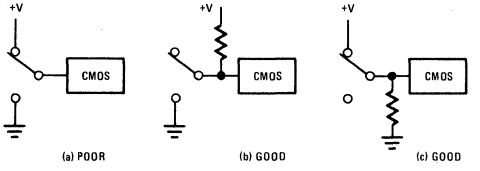


Figure 2

A PRACTICAL MULTIPLEXER APPLICATION

Figure 3 illustrates a practical data acquisition system hookup using an analog multiplexer, a monolithic sample-and-hold and an A/D converter. The HA-2420/2425 sample-and-hold is a particularly good choice for this type application because it eliminates the need for a separate high impedance, high slew rate buffer amplifier. Its acquisition time is consistent with CMOS multiplexer settling times and most available A/D conversion times. Errors, after initial

adjustment, are consistent with up to 12 bit absolute accuracy over a wide temperature range.

A. ACCURACY

D.C. error sources include:

1. Multiplexer:
   a. input offset = R source x $I_{S(OFF)}$
   b. output offset = R(ON) x ($I_{D(ON)}$ + I bias (S/H))
2. Sample-and-hold
   a. input offset voltage
   b. charge injection; sample-to-hold offset
   c. gain error during "hold"
   d. drift during hold
3. A/D converter:
   a. linearity
   b. gain drift
   c. offset drift

Item 1(a) and (b), and 2(d) become significant only at very high temperatures. 2(a) and (b) are initially adjusted out with the offset adjustment pot on the S/H. 2(c) is usually adjusted out by A/D gain adjustment, but could also be removed by a voltage divider feedback on the S/H to give a slightly greater than unity gain during "sample". After initial adjustments, typical S/H errors are less than 0.5mV over 0° to +75°C. Note that after adjustment, there may be an appreciable offset at the S/H output when switching from sample to hold. This is not a problem, since accuracy is required only during "hold", and the system is adjusted for this.

The largest system errors are usually 3(b) and (c), drifts with temperature and time. If two multiplexer channels can be dedicated for stable (+) and (-) reference voltage inputs, then the data processor can continuously calibrate the system, effectively removing all errors, except 1(a) and 3(a) which are usually negligible.

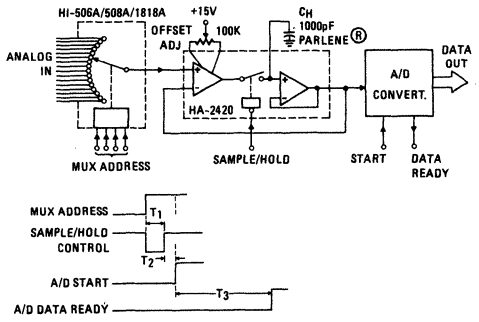


Figure 3

B. TIMING

The timing diagram in Figure 3 indicates the necessary system delays for each multiplexer address:

T_1 is the combined acquisition time for the multiplexer and S/H.

T_2 is the short interval required for the sample-to-hold transient to settle.

T_3 is the A/D conversion time.

The following table indicates minimum recommended timing for ± 10 Volt input range for acquisition/settling times to ½ L.S.B. accuracy:

	T_1	T_2
10 bit:	6μS	1μS
12 bit:	12μS	2μS

The multiplexer, by itself, requires about 2 μs and 9 μs settling to 10 bit and 12 bit accuracy, respectively; but fortunately this can be concurrent with S/H acquisition time. This is longer than would be predicted by the R_{ON} C_D time constant; probably because of internal distributed capacitance, a rather long period is required to traverse the last few millivolts towards the final value.

It should be noted that impedance conditions at the multiplexer inputs can affect the necessary acquisition time. At the instant the multiplexer switches from one channel to a new one, there is appreciable current pulled through the new channel input in order to charge C_D from its old level to its new level. This can cause ringing on signal lines, or glitches at signal conditioning amplifier outputs which require longer periods to settle. It is best for signal conditioning amplifiers to be wide band types, such as HA-2600, so that their high frequency output impedance is low and recovery from load transients is fast; even though the signal to be measured is very low bandwidth.

The T_1 and T_2 times could be eliminated by alternating two S/H circuits, acquiring a new signal on the second while A/D conversion is taking place. The two S/H circuits would have inputs connected together, and outputs alternately connected to the A/D by an analog switch. Total time, then, would be T_3 plus the analog switch settling time.

If the MUX input channels are sequentially switched, each channel will be sampled at a rate of

$$F_S = \frac{1}{N(T_1 + T_2 + T_3)}$$ samples per second, where N is the number of channels. The frequency spectra of the input signals must then be no higher than $\frac{F_S}{2}$.

In many systems, however, each channel carries a different maximum frequency of interest, and it may be desirable to depart from simple sequential scanning. Quickly varying signals, for example, could be addressed several times during a scanning period.

C. ADDING CHANNELS

For more than sixteen channels, several multiplexers may be tied together at the outputs, and addressed in parallel, but with only one "enabled" at a time. The MUX output offset will be increased, since I_D (OFF or ON) is additive. Also, output capacitance, C_D, is additive, creating increased access times.

These errors can be minimized in large systems by

having several tiered levels of multiplexing; where the outputs of a number of MUX's are individually connected to the inputs of another MUX.

D. DIFFERENTIAL MULTIPLEXING

When low level analog signals must be conducted over a distance, it is generally better, from a noise pickup standpoint, to use a balanced transmission line carrying signals which are differential with respect to ground.

A dual multiplexer is used for this purpose, as shown in Figure 4. Two sample-and-hold circuits plus an op amp form a high impedance differential sample-and-hold with gain. At gains greater than 4, the minimum sampling time (T_1 in previous example) must be increased proportionately to gain to allow for overdamped settling characteristics.

When handling low level, or high impedance signals, consideration should be given to adding signal conditioning amplifiers at the signal sources, since this can often produce less troublesome, more accurate, lower cost systems.

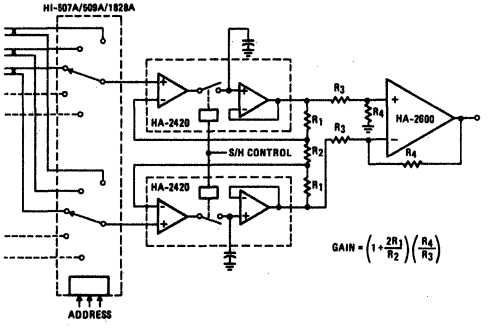


Figure 4

E. DEMULTIPLEXING

Since the switches in a CMOS MUX conduct equally well in either direction, it is perfectly feasible to use it as a single input-selected multiple output switch. Figure 5 illustrates its use as a demultiplexer, with capacitors to hold the output signal between samples. When the address lines are synchronous with the address of the original multiplexer, the output lines will recreate the original inputs, except level changes will be in steps.

Overvoltage protection is not effective with signals injected at the normal MUX output, so an external network should be added, if necessary.

A more accurate demultiplexer could be constructed using the HA-2420/2425 sample-and-hold for each channel, connecting inputs together and sampling each channel sequentially.

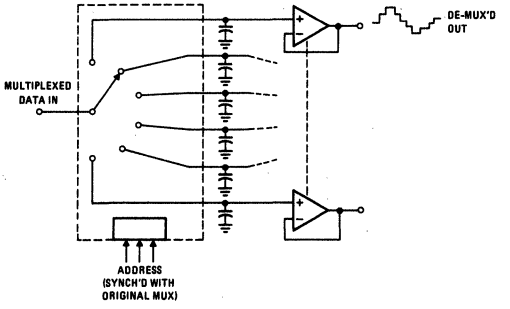


Figure 5

ANALOG SWITCH APPLICATIONS

A. HIGH CURRENT SWITCHING

Analog switches are sometimes required to conduct appreciable amounts of current, either continuous, or instantaneous—such as charging or discharging a capacitor. For best reliability, it is recommended that instantaneous current be limited to less than 80mA peak and that average power over any 100 millisecond period be limited to $I^2R_{ON} \leq$ (absolute max. derated power—quiescent power). Note that R_{ON} increases at high current levels, which is characteristic of any FET switch. Switching elements may be connected in parallel to reduce R_{ON}.

B. OP AMP SWITCHING APPLICATIONS

When analog switches are used either to select an op amp input, or to change op amp gain, minor circuit rearrangements can frequently enhance accuracy. In Figure 6 (a), R_{ON} of the input selector switch adds to R_1, reducing gain and allowing gain to change with temperature. By switching into a non-inverting amplifier (b), gain change becomes negligible. Similarly, in a gain switching circuit, R_{ON} is part of the gain determining network in (c), but has negligible effect in (d).

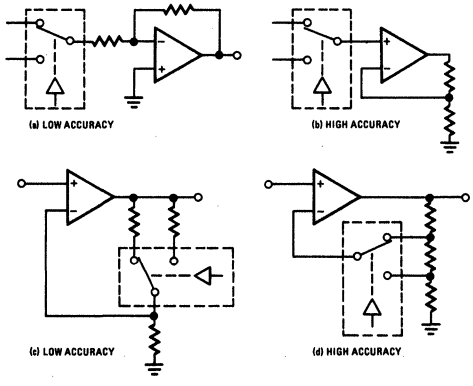


Figure 6

C. SWITCHING SPIKES AND CHARGE INJECTION

Transient effects when turning a switch off or on are of concern in certain applications. Short duration spikes are generated (Figure 7 (a)) as a result of capacitive coupling between digital signals and the analog output. These have the effect of creating an acquisition time interval during which the output level is invalid even when little or no steady state level change is involved. The total net energy (charge injection) coupled to the analog circuit is of concern when switching the voltage on a capacitor, since the injected charge will change the capacitor voltage at the instant the switch is opened (Figure 7 (b)).

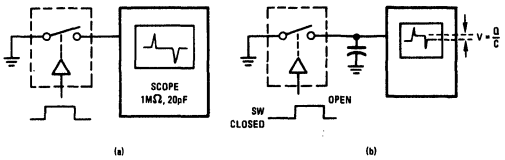


Figure 7

Charge injection is measured in pico Coulombs; the voltage transferred to the capacitor computed by

$$V = \frac{\text{Charge (pC)}}{\text{Capacitance (pF)}}$$

Both of these effects are, in general, considerably less for CMOS switches than for equivalent resistance JFET or PMOS devices, since the gate drive signals for the two switching transistors are of opposite polarity. However, complete cancellation is not possible, since the N and P channel switches do not receive gate signals quite simultaneously, and their geometrics are necessarily different to achieve the desired D.C. resistance match.

In applications where transients create a problem; it is frequently possible to minimize the effect by cancellation in a differential circuit, similar to Figure 8.

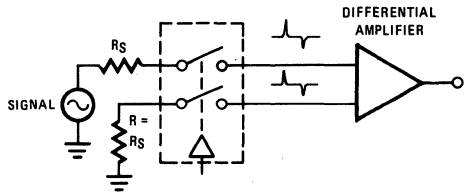


Figure 8

Among the Harris anlog switches, the HI-201 is the best from the transient standpoint, having turn-on spikes of about 100mV peak, 50ns width at the 50% point, and charge injection at turn-off of about 20 pico Coulombs. Transients of the HI-5040 series are several times higher.

D. HIGH FREQUENCY SWITCHING

When considering a switching element for R.F. or video type information, two factors must be watched: attenuation vs. frequency characteristics of an ON switch, and feedthrough vs. frequency characteristics of the OFF switch. Optimizing the first characteristic requires a low $R_{ON} \times C_D$ product, and the second a low value of C_{DS} (OFF).

The 30 ohm switch types of the HI-5040 series appear to best meet these requirements, and testing at high frequencies has verified this.

Figure 9 illustrates these circuit configurations; (a) is a simple series switch, (b) is a series-shunt configuration to reduce feedthrough, and (c) is a SPDT selector configuration with series-shunt elements. A 1K ohm load is illustrated, which might be the input impedance of a buffer amplifier stage; a lower load resistance would improve the response characteristics, but would create greater losses in the switch and would tend to distort high level signals.

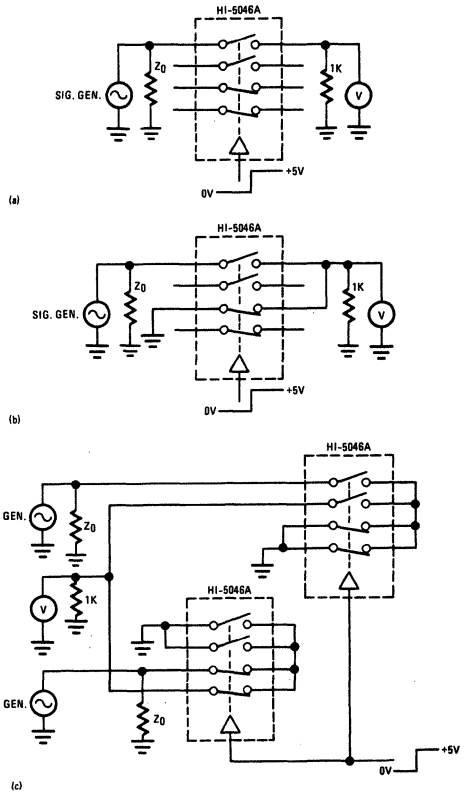


Figure 9

Figure 10 shows ON and OFF frequency response for each of the above configurations. Arbitrarily, we will define useful frequency response as the

region where ON losses are less than -3dB and OFF isolation is greater than -40dB.

The simple configuration (a) has excellent ON response, but OFF isolation limits the useful range to about 1MHz (the data sheet indicates -80dB isolation at 100kHz, but this is measured with 100 ohms load, which accounts for the 20dB difference).

The circuit in (b) shows a good improvement in isolation produced by the low impedance of the shunt switch. The useful range is about 10MHz; which could also be achieved in a simple SPDT 2-switch selector if source impedances are very low.

The selector switch in (c) has excellent characteristics, both ON and OFF curves indicating 40MHz useful response. Additional switches connected to the same point would reduce the ON response because of added shunt capacitance; but this could be eliminated by feeding separate summing amplifier inputs.

Careful layout is, of course, important for high frequency switching applications to avoid feedthrough paths or excessive load capacitance.

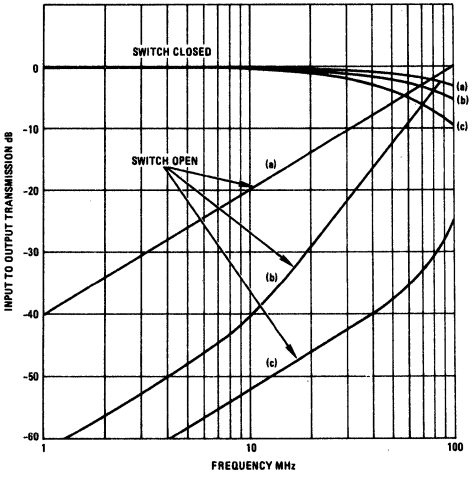


Figure 10

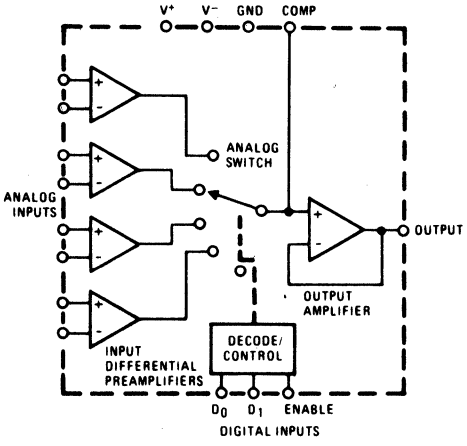
ALTERNATIVES TO CMOS SWITCHES AND MULTIPLEXERS

CMOS devices are excellent in many applications. However, there are some other devices which merit consideration in certain analog switching circuits where they may improve performance, reduce parts count, or be more economical.

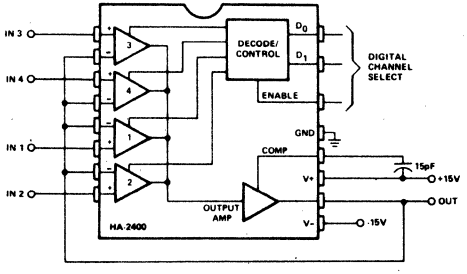
A. THE PRAM, PROGRAMMABLE AMPLIFIER

The HA-2400/2405 is a unique monolithic bipolar circuit which combines analog switching with high performance operational amplifiers. It basically consists of four op amp type input stages, any one of which is connected to a single output by bipolar switches controlled through a TTL compatible address decoder. In a single package, it contains the equivalent of 5 op amps plus a 4 channel mulitplexer. It has literally hundreds of applications in signal selection and programmable signal conditioning.

Figure 11 illustrates a four channel multiplexer. Connections from the output to each input stage are always the same as a comparable op amp circuit; the +1 gain connection is illustrated.



(a) FUNCTIONAL DIAGRAM



(b) ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

Figure 11

Advantages over a comparable CMOS multiplexer circuit are as follows:

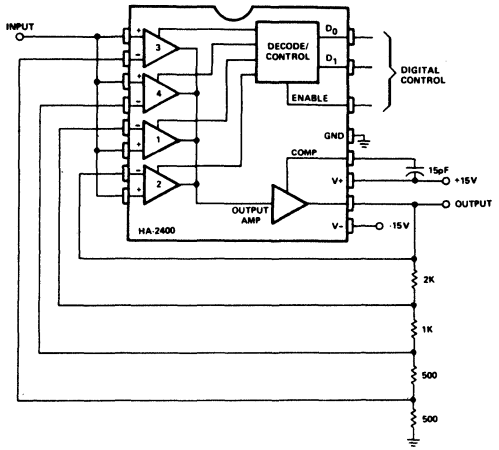
1. High input impedance (10^{12} ohms), low output impedance (< 0.1 ohm) means that ON resistance and leakage currents are no longer of concern. There is negligible transient loading of input lines.
2. Gain filtering, etc. can easily be added with feedback networks.
3. Fast acquisition (1.5μS).

4. Wide bandwidth (8 MHz).
5. Superior feedthrough characteristics (-110dB at 10kHz, -60dB at 1MHz).

Disadvantages include:

1. Less accuracy for low level D.C. signals; the offset voltages of each input stage do not necessarily match or track each other.
2. Cannot be used in reverse as a demultiplexer.
3. Disabling the device (enable pin low) does not open the output line, or drive the output to zero. Adding channels may be accomplished by tieing compensation pins together.

Figure 12 illustrates the PRAM used as a programmable gain amplifier. Any connection possible with op amps can be wired 4 ways to make programmable active filters, oscillators, etc., etc. Harris Application Note 514 shows many possibilities.



AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN

Figure 12

B. SAMPLE-AND-HOLD

The sample-and-hold function has often been accomplished with separate analog switches and op amps. These designs always involve performance tradeoffs between acquisition time, charge injection, and droop rate.

The HA-2420/2425 monolithic sample-and-hold, illustrated previously in Figure 3 has many times better tradeoffs, usually at a lower total cost than the other approaches. The switching element is a complementary bipolar circuit with feedback which allows high charging currents (30mA), low charge injection (10pC), and ultra low OFF leakage current (5pA); a combination not approached in any other electronic switch. These factors make it also superior as an integrator reset switch, or as a precision peak detector as shown in Figure 13. Harris Application Note 517 illustrates many other applications.

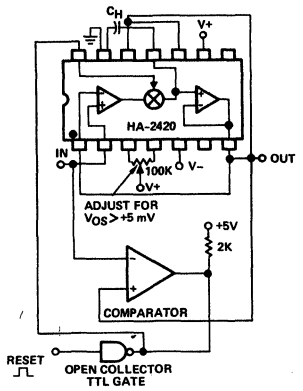


Figure 13

C. PROGRAMMABLE SUPPLY CURRENT OP AMPS

The HA-2720/2725 and HA-2730/2735 (dual amp) are op amps with an extra terminal which is used to control quiescent supply current. These are most generally used in low power systems to optimize the power dissipation vs. bandwidth and slew rate tradeoffs. They can also be used with variable set currents to make linearly variable oscillators, filters, etc. Another application is a switchable op amp as shown in Figure 14.

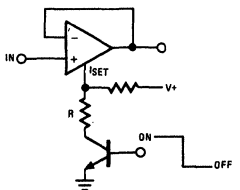


Figure 14

The illustrated transistor could be the output of high voltage open collector gate. The set resistor R is chosen so that the set current is the desired value when the transistor is ON, considering that the voltage at I_{SET} terminal when ON is about 2 forward junction drops ($\sim$ 1.5V) below V+. When the transistor is turned OFF, amplifier input, output, and supply terminals become very high impedance, so that two or more amplifier outputs could alternately be switched to the same point.

Off isolation with a 2,000 ohm load is about -80dB at 10kHz.

D. CHOPPER STABILIZED AMPLIFIER

Analog switches are sometimes used as choppers for amplifying low level D.C. signals with low offset errors. The HA-2900/2905 is a monolithic chopper stabilized amplifier in a TO-99 can. Typical offset drifts are 0.2 μV/°C and 1pA/°C with 5 x 10^8 open loop gain. Harris Application Note 518 describes this device.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 521

GETTING THE MOST OUT OF C-MOS DEVICES FOR ANALOG SWITCHING JOBS

BY ERNIE THIBODEAUX

INTRODUCTION

Although most designers appreciate the benefits of the complementary-MOS process for digital design, few realize how effective the technology can be for analog switching. C-MOS analog switches, which consume less power than bipolar devices, exhibit no dc offset voltage and can handle signals up to the supply rails. The C-MOS bilateral property furnishes input and output functions, making multiplexing and demultiplexing possible. In addition, the on-resistance of an MOS switch is as low as 30 ohms—a third as much as a bipolar device.

Unfortunately, C-MOS analog switches, which until recently were built with junction isolation, have been difficult to design into analog multiplexers and switches. The devices latched up easily, their C-MOS inputs were destroyed by electrostatic charges, and they literally went up in smoke when confronted with input overvoltage spikes and power-supply transients. To prevent destruction, costly external protective circuits were needed, and, even then, the devices latched up unless the power was turned on and off in a set sequence.

Because latch-up problems limited the use of analog switches so severely, device designers focused a great deal of attention on eliminating the condition. Recently, the success has been noteworthy. Indeed, three new technologies now offer latch-free analog switch operation: latch-proof junction isolation (JI), floating-body junction isolation, and dielectric isolation (DI).

Both JI techniques are conventional processes that have been slightly modified to alleviate the old problem of latch-up. However, both of these JI technologies still require costly external protection circuits to guard against burn-out in such applications as analog-signal multiplexing that interface them with the outside world. That is why JI devices are best suited for internal-switching applications where the electrical environment can be controlled. In contrast, the improved DI technology, by virtue of its construction, offers analog-switching devices suitable for many inside applications, as well as providing inboard analog protection for devices that interface with the other circuits. Happily, the smaller substrate area of the DI device delivers a better speed-power product than the JI technology.

THE BASIC C-MOS SWITCH

The basic C-MOS transistor (Fig. 1) has parasitic junctions that are reverse-biased during normal operation. However, certain overvoltage conditions can forward-bias these junctions to cause high currents that could possibly destroy the devices.

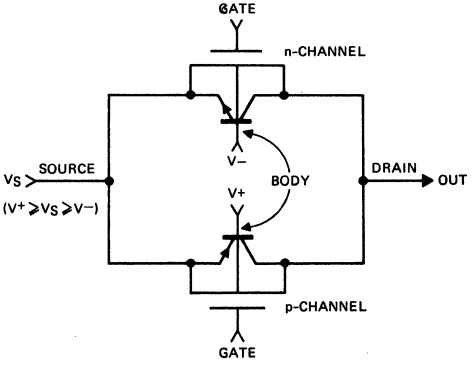


Figure 1. Bad
In the basic C-MOS analog switch, the parasitic junctions are reversed-biased during normal operation. Large overvoltages, however, make them forward-biased and draw large currents.

The parasitic junctions are actually npn and pnp transistors that are normally reverse-biased by the applied body potentials. However, because many analog switches, and especially multiplexers, are connected to their analog sources through long lines, they are highly susceptible to externally induced voltage spikes. For example, these spikes, which can often exceed the p-channel body potential, V+, can inadvertently turn on a normally off switch

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through the parasitic pnp transistor (Fig. 1).

The n-channel device is similarly affected when the parasitic npn transistor is turned on by a negative overvoltage. This action, commonly known as channel interaction, causes momentary channel-to-channel shorting, which introduces significant errors in the system. This intermittent condition, which is seldom destructive, is rarely isolated because it occurs only randomly.

One of the adverse effects of channel interaction is illustrated in Fig. 2. Channel 1 of an analog multiplexer is selected when all other channels are off. Channel 16 receives an input-noise spike that momentarily exceeds the positive supply. The sequence causes channel 1 read-out to be +16V because of interaction with channel 16 just before initiating the hold command to the sample-and-hold device. To prevent this annoyance requires additional protective circuits that clamp each channel input to a voltage below the threshold of the parasitics to ensure that the channels remain inactive under any conditions.

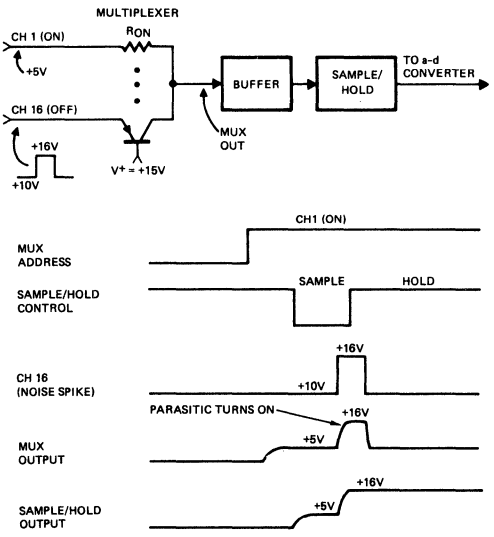

Figure 2. Worse

With CMOS devices, noise spikes can cause channel interaction. In this multiplexer, although channel 1 is only one selected, noise spikes cause cross talk in channel 16, which affects reading.

A more serious condition exists when the substrates (p- or n-) lose their respective potentials to ground (Fig. 3) —a condition that occurs when power to the device is turned off while the analog signals are still present. In this situation, the analog switch, which at that point represents a diode connected through the low impedance of the supply, draws high current from the analog source.

This current turns on the switch through its parasitics and shorts all channels to the output. These shorts can easily be catastrophic in multiplexer systems that have different power supplies for the analog source and the multiplexer switch. An error during troubleshooting or an inadvertent supply glitch can trigger this fault mode and destroy the whole system. Therefore, there is obviously much more to system reliability than having latch-proof C-MOS devices.

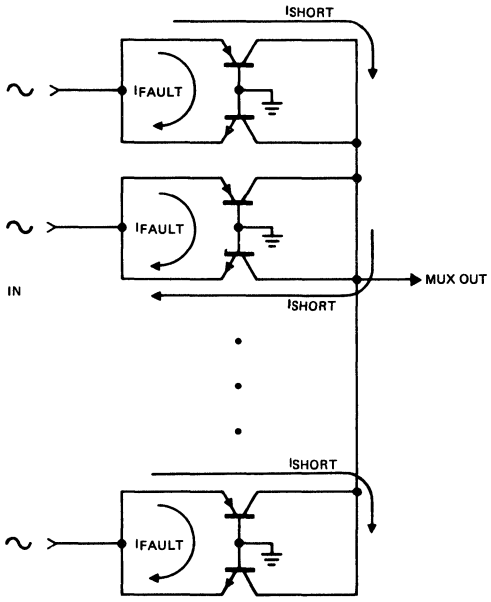

Figure 3. Still Worse

Most serious in CMOS switches is losing substrate potential to ground. This condition, which happens when power is lost and the analog signal is present, causes very high currents.

CONSIDERING LATCH-PROOF JI TECHNOLOGY

The standard JI process has been modified by what is claimed to be latch-proof construction through control of the effective betas of the parasitic transistors. A cross section in Fig. 4(a) shows the C-MOS structure along with its parasitic transistors and the equivalent circuit in Fig. 4(b) that gives rise to the silicon-controlled-rectifier latch-up problem.

Under any of the fault conditions previously mentioned, the npn and/or pnp can trigger this quasi-dual-gate SCR into a state of high conduction. If the transistor β product is 1 or greater, this configuration is sustained until either the device burns up or all sources of power are removed. By using a buried-layer configuration, as shown in the cross section, the β product is reduced to less than 1, eliminating the latch-up conditions.

Again, especially in multiplexer applications, the latch-free devices do not guarantee against destruction, and the JI multiplexer still requires costly discrete circuits around the device, as shown in Fig 5. If an overvoltage exists, the resistor/diode circuit at each analog input limits the input voltage to the

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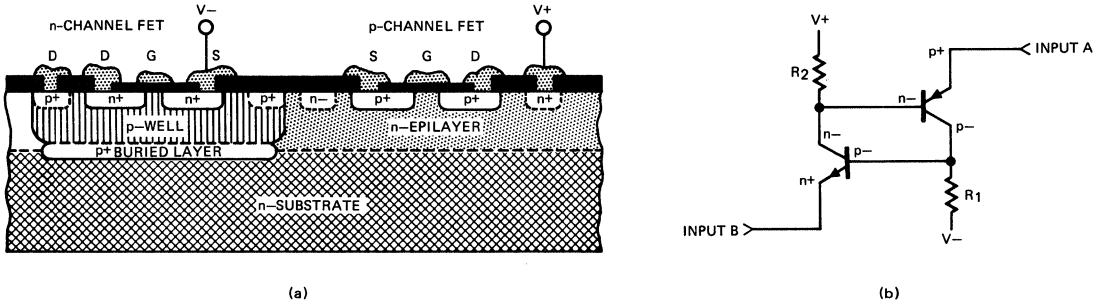

Figure 4. Latch-Proof. Junction-isolated devices are now made latch-proof with a buried-layer configuration (a), which keeps beta of parasitic transistor under unity. That kills chance for latch-up (b), which plagues devices built with older junction-isolation technology.

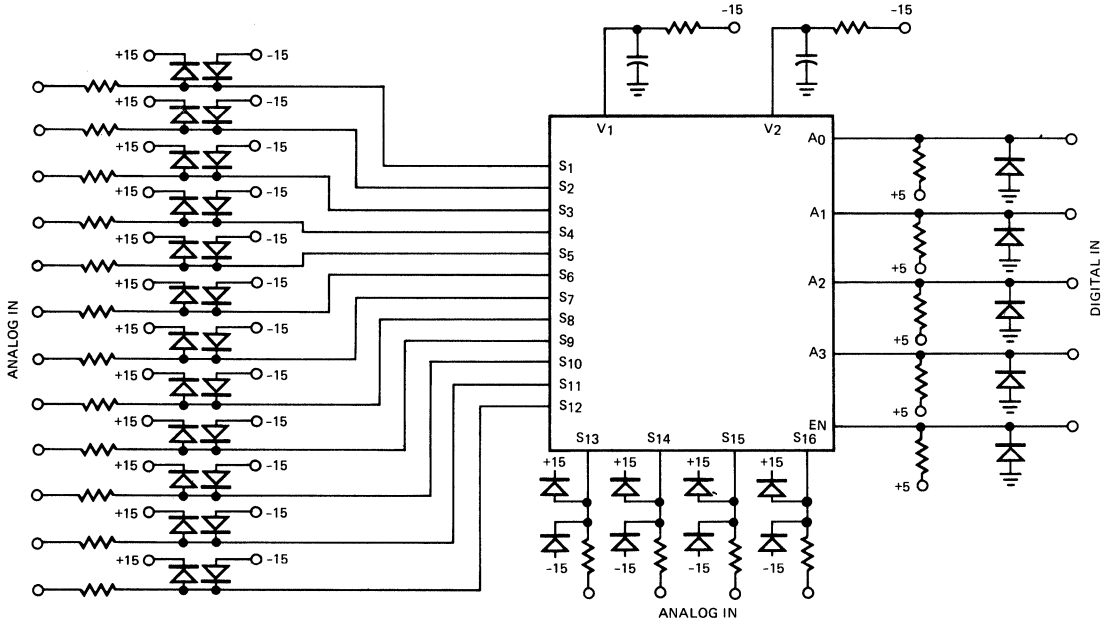

Figure 5. Protection still needed. Although new JI devices won't latch up, they still can be destroyed by large currents. That's why typical JI multiplexers, like the one shown here, still need to be surrounded by external protective components, which drive up system costs.

supply-voltage range to prevent the parasitic transistor action.

The resistors limit the overvoltage currents through the diodes. The diodes must have a low threshold voltage—much lower than the 0.6V silicon-junction threshold of the internal parasitic diodes—to ensure that the parasitics do not turn on.

A germanium diode offers a low threshold voltage, but its high leakage current makes it impractical, especially in 0.1% systems. Therefore, in most applications, more expensive low-leakage diodes are used.

For example, Schottky diodes meet the requirements, but they cost about 50 cents each in volume, and the total cost per multiplexer, including parts and labor, for the discrete protection circuit may well be double the initial purchase price of the device. Even then, its reliability will never approach that of an IC that has this protection already built in.

THE FLOATING-BODY JI TECHNOLOGY

Standard JI technology allows another approach to latch-proof device construction: a portion of the SCR continuity is broken by floating the "body" or substrate of the n-channel switching device. A cross section of this process is similar to that in Fig. 4(a), excluding the buried layer and the negative supply connection to the p- substrate, so that the dual-gate SCR is changed to a single -gate device that can only be triggered by the pnp parasitic. This, of course, reduces the latch-up probability by 50%.

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To completely eliminate latch-up, as before, the β product of the transistors is reduced to less than 1. This accomplishment, certainly a significant improvement over the conventional process, offers greater reliability, but certain trade-offs must be made when the body of a MOSFET is floated.

Nominal source-to-drain breakdown voltages are reduced which limit the peak-to-peak signal range. Over-all breakdown is limited by the collector-emitter breakdown voltage, BV_{CEO}, of the npn parasitic transistor of the floating n-channel MOSFET. The breakdown voltage increases with the degree of reverse-bias potential applied to the substrate. With a floating body, BV_{CEO} is minimum, so particular care is necessary when using these devices in configurations such as single-pole single-throw, single-pole double-throw, dpst, and dpdt, where each side of the switch connects to opposite polarities. The peak-to-peak handling capability is specified at a minimum of 22V; therefore, 30V pk-pk cannot be switched with ± 15V supplies, as it can with other C-MOS devices.

What's more, the leakage currents of floating-body JI devices are higher than other types, simply because the I_{CEO} of the floating base for the npn is much greater than the I_{CBO} of other devices having fixed reversed-biased body potentials. The increased leakage currents in spst switches may not be too significant.

However, in multiplexers that have the outputs of as many as 16 switches tied together in one IC, the total summation of currents can significantly affect system accuracy. For example, the specification for a worst-case 16-channel floating-body multiplexer is 10 microamperes, and the channel on resistance is 550 ohms . The dc-offset error would be 5.5 millivolts, representing an accuracy to 0.055%.

Other 16-channel types specify worst-case parameters of 500 nanoamperes and channel resistance between 550 ohms and 2 kilohms. Their dc-offset error is between 0.28 mV and 1 mV, respectively, allowing accuracy to 0.01% or better.

Finally, the effective off impedance of the floating-body switch is degraded by the floating-body technique. Off-isolation characteristics of a MOSFET are primarily determined by its source-to-drain capacitance. But with the base floating, the effective capacitance from emitter to collector is increased by the series combination of emitter-base and base-collector-junction capacitances (Fig. 6a). This increase degrades the over-all off-isolation characteristics. For example, the off isolation for a typical floating-body channel at 1 megahertz that has RL = 100 ohms is specified to be -54 decibels, which compares favorable with other types. However, at lower frequencies such as 1 kHz, the isolation is only -62dB, compared to more than -110dB for improved devices. Capacitances C_1 and C_2 for them are shunted by the low ac impedance of the supply voltage (Fig. 6b).

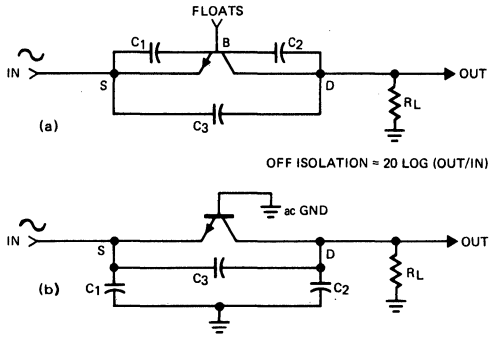

Figure 6. Floating Bodies

Floating-body switches have degraded "off" impedance because total capacitance (a) combines two junction capacitances. In DI circuit (b), capacitances are shunted out.

THE LINEAR DIELECTRIC-ISOLATION TECHNOLOGY

The linear dielectric-isolation process requires no modifications to guard against latch-up. Its basic construction ensures that the SCR configuration that causes latch-up can not exist. The functional cross section in Fig. 7 reveals the silicon-dioxide isolation barrier fabricated between all parasitic transistors. This isolation allows each active element to be self-contained and independent with no interface junctions. At most, only three-layer structures are permitted for each tub, so that four-layer strucures, or SCRs, are impossible. Also, since the DI technology requires no guard bands, junction capacitances, leakage currents, and size are minimized. The resulting increase in packing density per wafer, together with increased yields, enables these devices to be cost-competitive with other types.

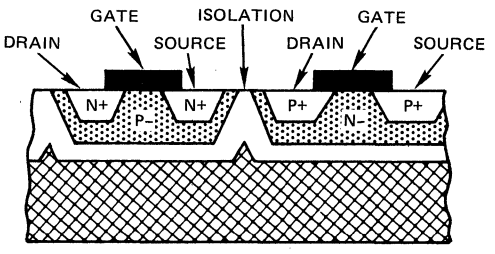

Figure 7. How DI Does It

Dielectric isolation eliminates latch-up by a silicon-dioxide isolation barrier between devices. This separates all active elements, eliminating interface junctions that cause parasitic SCR's.

In working with DI devices, the IC designer is not burdened with the fixed substrate potentials found in JI devices. He may let the substrate float, fix it to some potential, or even modulate it. Fig. 8 depicts a typical DI analog switch circuit that minimizes the variation of on resistance with the analog signal. Ordinarily, in conventional circuits, the body or

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substrate potentials of the n and p-channel devices are fixed and the source-to-body bias potentials vary with the analog input voltage. This change in body bias causes a wide variation of on resistance within the analog signal range. However, in the DI circuit, the bodies of P_1 and N_1 are connected together through N_3 during the on state. This allows the body to follow the input voltage providing a constant source-body bias and therefore a constant on resistance. During the off state, the bodies of N_1 and P_1 are at their respective supply potentials through P_2 and N_2, thereby preserving high off isolation and low leakage currents.

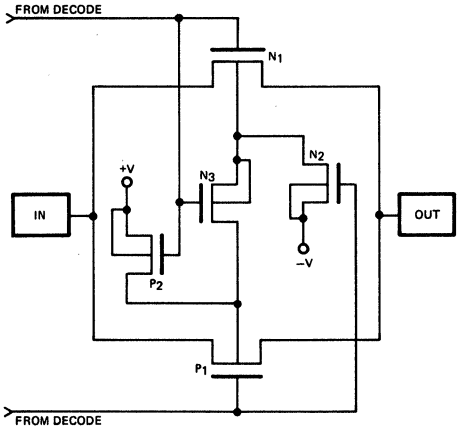

Figure 8. DI Does It

In dielectrically isolated switches, on resistance modulation by the analog input is minimized by connecting N_1 and P_1 bodies together through N_3.

DESIGNING A FOOLPROOF C-MOS ANALOG MULTIPLEXER

In dielectrically isolated multiplexer circuits, protection can be provided on the chip primarily to eliminate channel interaction. This protection prevents normally off channels from being turned on by parasitics from other channels. And because this interaction is prevented, even worst-case power-supply faults cannot destroy the device. Moreover, since DI structures have no SCR effect, protection against latch-up and power-sequencing are not necessary. In short, DI multiplexers with built-in protection can withstand virtually any conceivable fault from the outside world.

The typical protected DI multiplexer (Fig. 9) benefits from a combined bipolar/C-MOS technology. The illustrated bipolar section is used to sense an analog overvoltage condition and steer current away from the parasitic MOSFET junctions. Each of the switching devices, N_1 and P_1, has its own protection circuits. Devices P_3, D_6, D_7 and Q_6 protect P_1 while N_3, D_4, D_5, and Q_5 protect N_1. When the switch is off, the substrate of the p-channel FET, P_1, is connected to V+ through P_3 and diode D_7 for maximum isolation and low leakage currents in the off state. If the input voltage suddenly exceeds V+, the source-body junction, which would normally conduct, is instead clamped by transistor Q_6.

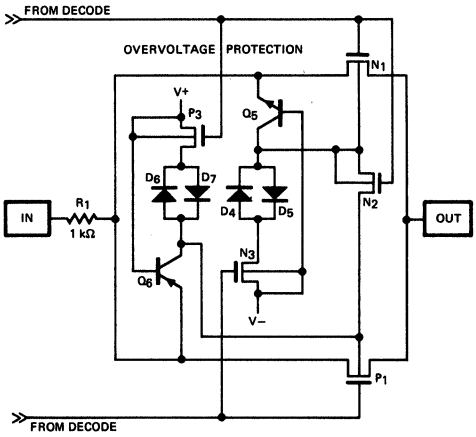

Figure 9. Winning Combination

Combining bipolar and MOS technologies in the same multiplexer gives built-in protection. This circuit is typical for each channel in multiplexers HI-506A, HI-507A, HI-508A, and HI-509A.

The base-emitter junction conducts to hold the source-body diode off with a saturation voltage $V_{CE(SAT)}$ of about 0.2V. Thus clamped, the switch is protected from the effects of overvoltage.

Clamp Q_6 always turns on before the forward-voltage drop of the source-body diode is exceeded because diode D_6 requires an additional forward-voltage drop for conduction through the parasitic junction. Moreover, resistor R_1 limits the current flowing through Q_6 when high overvoltages exist. Although R_1 adds to the total on-resistance of the channel, its associated error is insignificant, since most systems provide high-impedance buffering anyway. For negative overvoltages, N_1 is similarly protected. What's more, the protection circuit, rated at a nominal overvoltage of $\pm$33V, reveals a cross-talk current of only about 5na (Fig. 10).

When the switch is normally turned on, the substrates of N_1 and P_1 are connected together through N_2, which, as described before, results in a constant on resistance.

This condition represents an absolute error from channel interaction of only 6 microvolts (R_{ON} x 5NA)—certainly negligible in most systems. In contrast, floating-body types have guarantees only that they won't be burned up by $\pm$25V overvoltage. Their manufacturers do not make any claim against channel interaction. In fact, channel interaction occurs readily in these devices when the n- and p-channel thresholds are exceeded by an overvolt-

age. For example, the n-channel device, although floating, would be inadvertently turned on if the analog input exceeded the negative supply by its gate-to-source threshold, which is typically 1.5V.

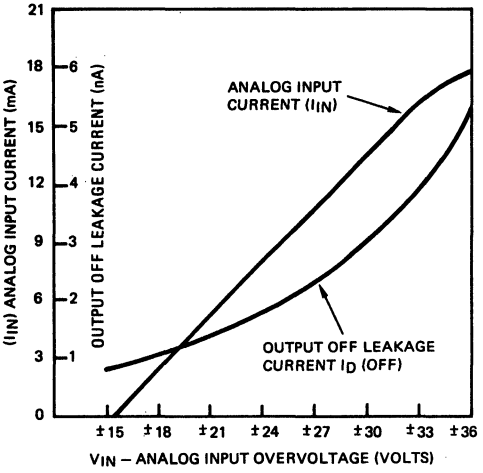

Figure 10. Blocking Cross Talk

DI switches have minimal cross-talk problems. An overvoltage of 33V produces a cross-talk current of only 5nA—an absolute error from channel interaction of only 6 μV.

ADDING BENEFITS

RESULTS OF DIGITAL-INPUT PROTECTION TESTS (20 DIELECTRICALLY ISOLATED UNITS)	
STRESS STEP/VOLTS	FAILURES
500	0
1,000	0
1,500	0
2,000	1
2,500	0
3,000	3
3,500	0
4,000	3

Additional DI benefits are passed on to the user in the design of the digital input-protection circuit shown in Fig. 11. The fabrication of all components as isolated silicon islands eliminates any possibility of latch-up. The diodes switch fast and quickly discharge any static charge that may appear at the digital MOS input gates. The table gives the results of a step-stress analysis performed on 20 units. A total of 80% survived the 3.5 kilovolt level, and only one failed below 2kV.

The DI technology enables a wide variety of active elements to be integrated on the same chip to provide maximum versatility. For example, in the transistor-transistor-logic/C-MOS reference circuit shown in

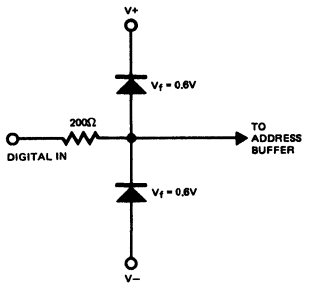

Figure 11. Digital Protection

DI devices also protect digital inputs. For example, the diodes in this circuit quickly discharge any static charge that may appear on an MOS input gate.

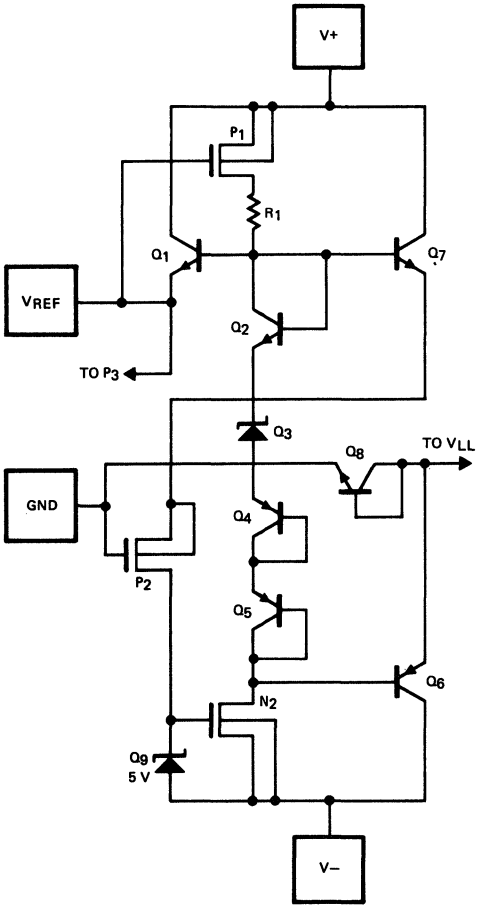

Figure 12. Packing It In

DI technology increases chip density of analog switch, allowing more circuit capability per package. For example, DI designs make possible this internal logic reference circuit in HI-200 and HI-201 switches.

Fig. 12, the bipolar technology enables realization of a simple zener reference circuit, consisting of resistor R_2 and transistors Q_1, Q_2, and Q_3.

The circuit develops a stable 5V reference for interfacing with TTL and eliminates the need for an additional 5V logic supply. Current for the zener (Q_3) is supplied through the normally on MOSFET, P_1, which can be easily turned off if not needed to minimize power consumption when interfacing with C-MOS-logic circuits. P_1 turns off when V+ or supply voltage V_{DD} is applied to the reference terminal V_{REF} to convert the IC's power-consumption from bipolar to C-MOS level. If power is not critical, V_{REF} can be left open to speed switching.

In high-speed data-acquisition systems, the designer is concerned with both quiescent power and dynamic power consumption. If JI devices are used, the capacitance or leakage currents are so high they contribute a major portion of total power consumption. That situation is caused by the large-geometry parasitic junctions formed by the n- junction.

In contrast, the smaller substrate area of the DI device provides much less power drain. Dynamic-power consumption as a function of frequency for several 16-channel analog multiplexers with ±15V supplies is shown in Fig. 13. The DI device consumes only 100mW at 1 MHz to yield the best speed-power product.

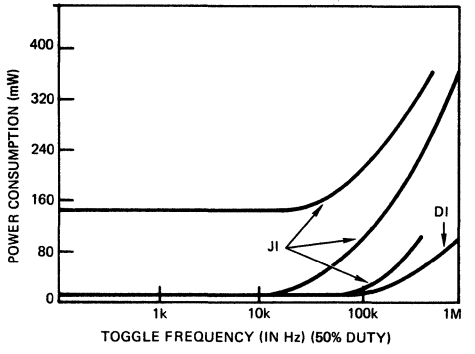

Figure 13. DI Performs
DI devices not only perform well, but do it with less power. Dynamic-power-consumption data for commercial multiplexers shows DI device consuming only 100mW at 1MHz.

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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 601

INTRODUCTION TO THE PHASE LOCKED LOOP

BY DON JONES

INTRODUCTION

In electronics, we are all concerned with the manipulation of information which is expressed as electrical quantities. This information can be expressed many ways - as a voltage, a current, a time period between two events, or as modulation information on an AC. carrier - amplitude, frequency, or phase angle.

Of these, the time related expressions - time, frequency, and phase angle have several advantages. Information can be transferred between remote points with less loss of accuracy due to noise. Extremely accurate standards are available - crystal oscillators and atomic clocks.

One reason that frequency or phase modulation has not been used more universally as an information medium, is that hardware to manipulate these signals has been more complex than that for voltage and current signals. For voltage and current signals, inexpensive building blocks such as operational amplifiers and digital circuits have greatly simplified design of complex systems. Now, there is a versatile building block for signals in the frequency domain - the monolithic phase locked loop.

You've probably heard the term. "phase locked loop", a number of times since first starting in electronics; but unless you have already had the opportunity to work with one, the concept may not be clear. The general operation of this circuit is really not difficult to understand. You will find the phase locked loop to be a very useful tool wherever A.C. signals are encountered - from subaudio to microwave frequencies.

WHAT IS A LOOP?

First, let's review what is meant by "loop"; then later we can show where "phase lock" comes in.

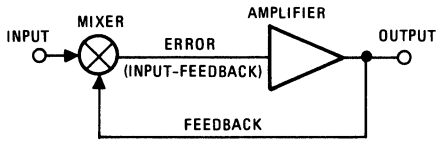


Figure 1

Figure 1 is a general diagram which fits many control systems - electronic, mechanical, or even the human body. The input signal is a function of the desired output. If the output is not presently at the desired point, an error signal is generated by the mixer- which is amplified and drives the output in a direction so as to minimize the error signal. In a moment, we will see how this negative feedback loop system applies to the phase locked loop.

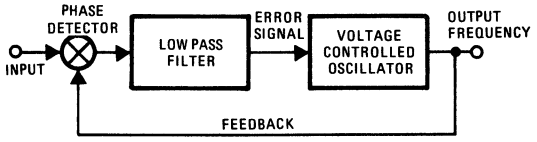


Figure 2

A simple diagram for a phase locked loop is shown in Figure 2. If we consider the phase detector and low pass filter to be a mixer, and the voltage controlled oscillator to be a type of amplifier, the diagram is identical to the negative feedback loop in Figure 1.

In many feedback control systems, the input and output information signals are expressed as voltages. In the phase locked loop, however, the input and output information signals are expressed as A.C. frequencies.

As in the general loop, the output is driven in the direction which will tend to minimize the error signal. In this case, the error signal is a frequency - so the loop tends to drive the error frequency towards zero frequency. To accomplish this, the feedback frequency must be made equal to the input frequency. Once the two frequencies are made equal, the error signal is a function of phase difference between the two signals, so that the phase difference is also controlled.

Before showing what we can do with the phase locked loop, let's examine its parts.

PHASE DETECTOR AND FILTER

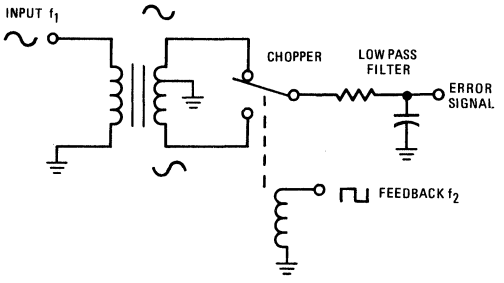


Figure 3

For simplicity, an electromechanical phase detector is illustrated in Figure 3. Of course, most systems use a solid state switching element, rather than a mechanical chopper.

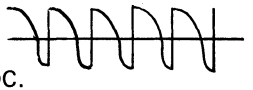
As the chopper armature is moved from one contact to the other, the input signal appears at the armature alternately at 0^o or 180^o phase. If the input and feedback frequencies, f_1 and f_2 are not equal, the circuit acts as a balanced modulator with sum and difference frequencies, $(f_1 + f_2)$ and $(f_1 - f_2)$ appearing at the chopper armature. The low pass filter will pass mainly the difference frequency with increasing amplitude as the two frequencies approach one another.

If the input and feedback frequencies are exactly equal, a D.C. component will appear at the filter output, with amplitude dependent on the phase difference between the two signals. This is illustrated in Figure 4.

a) f_1 & f_2 In Phase:

Chopper Armature:
Filter output is positive D.C.

b) f_1 & f_2 90^o Out of Phase



Chopper Armature:
Fitler output is OVDC.

c) f_1 & f_2 180^o Out of Phase:

Chopper Armature:
Filter output is negative D.C.

Figure 4

Figure 5 shows filter output D.C. voltage as a function of phase difference between f_1 and f_2.

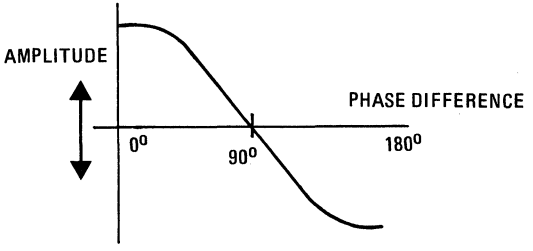


Figure 5

In this example, we can see that the output level is proportional to the input amplitude, as well as phase angle, and that zero output occurs at 90^o phase angle. This is also true of most solid state phase detectors, which actually multyply the two A.C. input signals together.

VOLTAGE CONTROLLED OSCILLATOR

The voltage controlled oscillator (V.C.O.) is usually nothing more than a free running multivibrator with a D.C. input which can vary the frequency over a certain range.

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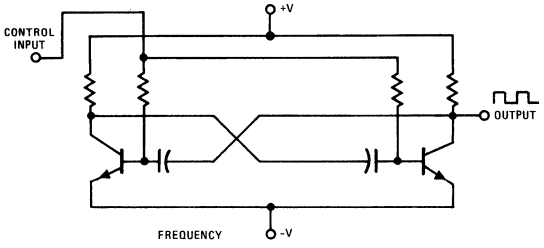


Figure 6

Figure 6 shows a simple V.C.O. If the control input were tied to +V, this would be a conventional fixed frequency multivibrator. As the control input D.C. voltage becomes more positive, the timing capacitors charge more rapidly, and the output frequency increases. Conversely, as the control input becomes less positive, the timing capacitors will charge more slowly and the output frequency will decrease. This relationship is shown in Figure 7.

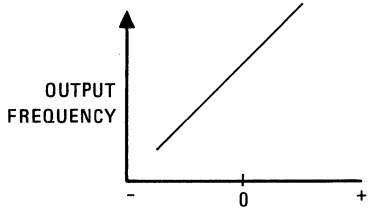


Figure 7

PHASE LOCKED LOOP OPERATION

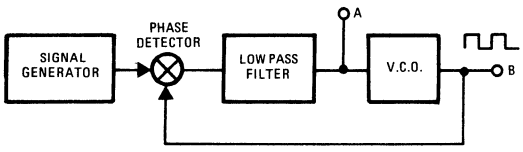


Figure 8

Suppose we connect a signal generator to the P.L.L. as shown above, and watch what happens as we vary the input frequency. First, we have chosen the timing components in the V.C.O. to produce the characteristic shown in Figure 9.

The V.C.O. can be constrained to run between 900 and 1,100 Hz by limiting the voltage swing at point A. Since the detector output characteristic (Figure 5) is bounded at both ends, the oscillator can only function between the limits determined by its input characteristic (Figure 7) and the detector output characteristic.

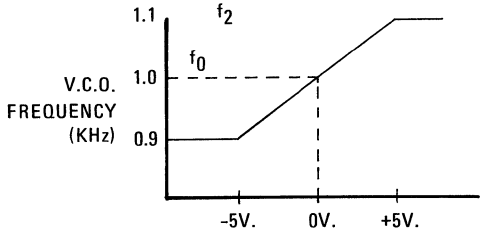


Figure 9

If the signal generator is disconnected, the V.C.O. will run at f_0, 1000 Hz, since the filter output is zero volts. If we then connect the signal generator with its frequency set to 700 Hz, the V.C.O. will still run at f_0, since the difference frequency is high and very little signal gets through the low pass filter.

Now, as we slowly increase the generator frequency, we will observe more and more "jitter" on the V.C.O. output, as the difference frequency becomes lower, and appears larger at the filter output, frequency modulating the V.C.O. about f_0.

Suddenly, say when the generator reaches about 920 Hz - the V.C.O. frequency abruptly jumps and holds steady exactly at the generator frequency. We find that the V.C.O. frequency is "locked" to the generator frequency as long as the generator remains between 900 and 1,100 Hz. If the generator frequency goes outside these limits, the V.C.O. will snap back to f_0. As the generator approaches f_0 from either direction, we find that we have to go slightly closer to f_0 to initially achieve "lock" than the 900 to 1,100 Hz limits required to hold the signal in "lock". These two sets of limits are known as Capture Range and Lock Range respectively, and can be independently adjusted by changing circuit constants in the PLL.

HOW DOES IT WORK?

Prior to lock, as the generator frequency approached f_0 from either direction, the difference frequency from the phase detector becomes smaller and its amplitude passed though the filter becomes larger. This signal modulates the V.C.O. frequency about f_0

until the V.C.O. frequency sweeps past the input frequency - then "lock" takes place.

But why do the two signals "lock"? We can examine the stability of any closed loop system, by imagining what happens if the output takes a small random drift in either direction. Let's assume for the moment that the generato and V.C.O. frequencies are identical. The low pass filter output will be the D.C. level required to maintain the V.C.O. at that frequency in accordance with Figure 9. The phase difference between the V.C.O. and the generator will not necessarily be 90° - it will be whatever phase angle is necessary to produce the proper V.C.O. D.C. input through the phase detector and filter to hold the oscillator frequency identical with the input frequency. Now suppose that the V.C.O. frequency drifts upward from the generator frequency by a fraction of a cycle. The first indication of this is that the phase difference between the two signals will change - the V.C.O. phase will become more leading. If the phase detector is connected such that a leading V.C.O. phase will make its output less positive, then the filter output will tend to pull the V.C.O. back to its original frequency. Conversely, a tendency for the V.C.O. to drift downward will also be corrected. For the same reasons, any change in the generator frequency will be tracked by the V.C.O. frequency. Since the phase detector output level as a function of phase angle is a cosine curve (Figure 5), there will be two points in 360° where the detector output is at the proper level to drive the oscillator to the input frequency - but only one of these points has positive stability, so the loop will automatically settle on the stable side of the curve.

7

APPLICATIONS

There are several properties of the phase locked loop which make it quite useful in processing signals in the frequency domain.

First we will find that the PLL is able to lock on to low level C.W. signals, even in the presence of random noise of greater amplitude than the signal.

1. The PLL can perform as an amplifier and noise filter.

Also, we know that the PLL will respond only to frequencies in the range of the V.C.O. and phase detector, so:

2. The PLL functions as a band-pass filter.

Referring back to Figure 8, suppose we rock the signal generator frequency back and forth between 900 and 1,100 Hz while observing the filter output at point A with a D.C. voltmeter. We will find that as the generator (and V.C.O.) frequency increases, the voltage will increase by a proportional amount in accordance with Figure 9: since the V.C.O. input voltage must change to track a change in generator frequency. If the generator is frequency modulated by a low frequency sine wave, that sine wave will be reproduced at point A. We can conclude:

3. The PLL will domodulate F.M. signals.

Some of the areas where the PLL may be applied include:

1. F. M. Receivers
   A PLL connected to a receiver I.F. signal with its center frequency at the I.F. frequency will replace one or more I.F. stages and the discriminator stage, eliminating the cost, bulk, and lower reliability of I.F. and discriminator transformers. In broadcast receivers, PLL's can also be used to detect the stereo pilot signal and to demodulate SCA broadcasts. In T.V. receivers, PLL's can be used in the I.F., sound discriminator, synch separator, and color discriminator sections; in each case replacing L-C tuned circuits. With modifications, the PLL can also be used in A.M. or phase modulation discriminators.

2. Data Modems
   In transmitting digital data over telephone lines, the ones and zeros are often encoded as two different audio tone frequencies. This is know as frequency shift keying, or FSK.

   The PLL may be used to decode these tones, since its filter output level will be proportional to the input frequency. Other modem systems utilize phase modulation of a single audio frequency, which can also be detected by a PLL in terms of spikes at the filter output.

3. Data Synchronizers
   In exchanging data between different systems, it is often necessary that the different system clocks be synchronized together. The V.C.O. of a PLL connected to an

incoming data stream will recreate the clock signal of the sending system. This eliminates the need for a separate data channel to send the clock signal.

4. Motor Speed Control
   Many electromechanical systems, such as magnetic tape drives, require precise speed control, particularly during start and stop operations. Figure 10 shows the incorporation of a motor control within a phase locked loop.

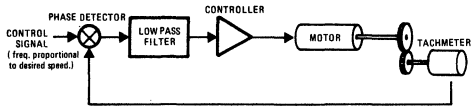


Figure 10

5. Frequency Synthesizers
   A frequency synthesizer is a programmable frequency source with high stability, used in test equipment and in transmitters. It is often desirable to derive any of the programmed frequencies from a single stable reference frequency, as illustrated in Figure 11.

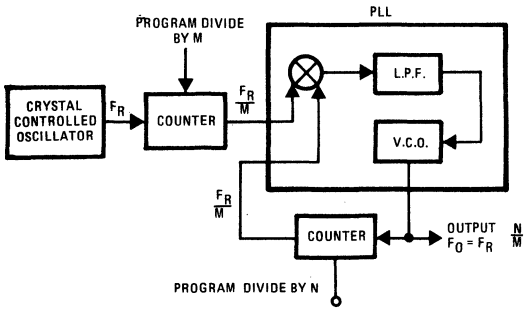


Figure 11

The counters shown may be standard digital integrated circuits which perform a programmed frequency division. The reference frequency, F_R, is first divided by an integer, M, and applied to the PLL input. In order for the loop to be locked, the identical frequency must be present at the other phase detector input. Since another counter (divide by N) is in series with the V.C.O. feedback line, the V.C.O. must be running at N times the PLL input frequency to satisfy conditions for lock. Therefore, the V.C.O. frequency is F_R times the ratio, $\frac{M}{N}$. Therefore, by programming M and N, we can produce any of a large number of frequencies, each with the stability of the single reference frequency.

HA-2820 PLL

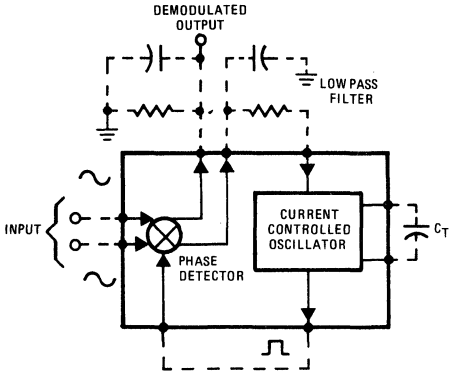


Figure 12

Harris Semiconductor has developed a monolithic PLL integrated circuit with a number of improvements over similar circuits. The HA-2820 is designed for frequencies from 0.01Hz to 3MHz.

Functions are shown in Figure 12. Significant features include:

1. No Internal Connections Between Detector and Oscillator

   This greatly enhances the device versatility. The low pass filter can be a critical element in some applications. With the loop broken at this point, complex passive or active filters may be inserted, several filters of different characteristics may be switched into the loop to aid in signal acquisition and tracking, or sweep circuits may be switched into the oscillator to scan a frequency band and acquire a signal.

   Also, with the loop broken, amplifiers may be inserted in the loop to control loop gain. This technique will be discussed in a later section.

2. Two Isolated Phase Detector Outputs
   For F.M. demodulation, the demodulated output is generally the filtered error signal

from the phase detector. However, a separate output from the phase detector has several advantages. The demodulated output gain can then be adjusted independent of the loop gain, and different filter characteristics may be chosen for the loop filter and the demodulated output filter. Separate filters are necessary to demodulate phase modulated signals - a low frequency cutoff filter in the loop so that the oscillator phase is constant and is determined by the average input phase; and a higher cutoff filter at the demodulated output to distinguish phase shifts between the input signal and oscillator.

3. Current Controlled Oscillator
   Operation of these devices is identical with those described previously containing a voltage controlled oscillator, except that error signal from the phase detector is a current, rather than a voltage. The phase detector outputs are high impedance current sources, so that the demodulated output voltage swing may be adjusted by selection of a load resistor. The oscillator input is a low impedance current sink with a fixed negative input voltage level. The impedance levels allow construction of accurate, temperature stable filters, since filter characteristics will be relatively independent of the device internal impedance characteristics.

LOOP GAIN ADJUSTMENT

In certain applications it may be desirable to increase loop gain by the addition of an amplifier in the error signal path. This has the effect of:

1. Increasing tracking range. The tracking range will then be limited only by the oscillator input range, rather than by the detector output range. Tracking ranges of greater than 3:1 are practical.

2. Tighter characteristics for small input frequency ranges. With an amplified error signal, the phase relationship between the input signal and oscillator output will stay closer to 90^{o} over a given frequency range. The demodulated output swing will be smaller, but more linear.

A simple connection for insertion of an operational amplifier is shown in Figure 13.

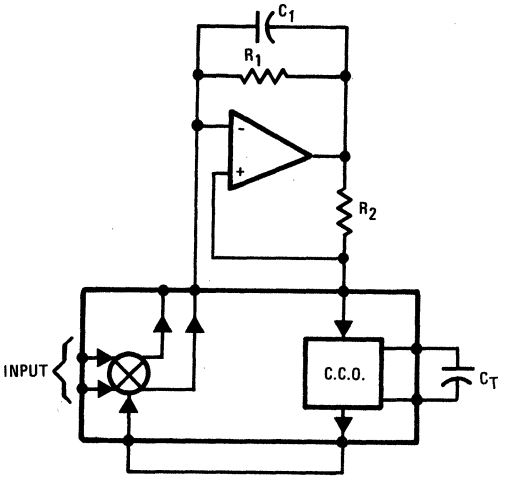


Figure 13

The current gain of the circuit is:

$$-\frac{R_1}{R_2}$$

The inversion of the error signal does not affect loop stability, since the phase detector characteristic is symmetrical about 0^{o} and lock will occur at -90^{o} rather than $+90^{o}$. The low pass filter is formed by R_1 and C_1. The connection of the amplifier (+) input to the C.C.O. input sets the amplifier output voltage swing about the C.C.O. input voltage - very little signal feedback to the (+) input occurs because of the low impedance of the C.C.O. input.

TRACKING RANGE LIMITER

This circuit may be added externally to the HA-2820/

Tracking range in a PLL is normally limited by the output signal range of the phase detector. In some applications, such as where response to a limited frequency band is desired, tighter control of the tracking range is necessary. This can be accomplished by limiting the excursions of the error signal.

The circuit in Figure 14 shows one method of limiting tracking range. The operational amplifier simply produces an isolated output voltage equal to the oscillator input voltage.

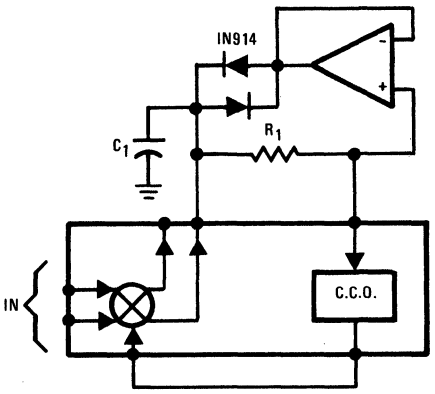


Figure 14

The voltage swing at the amplifier output is limited to approximately ±0.7 volts about the C.C.O. input voltage by the forward diode characteristics. Therefore, the oscillator input current is limited to approximately $\pm\frac{0.7}{R_1}$, and the tracking range may be calculated from the published oscillator conversion gain. The amplifier and diodes are built in to the HA-2800/2805.

GLOSSARY OF PLL TERMS

Acquisition Range(Capture Range): The range of input frequency about f_o under which a PLL, which is initially unlocked, will become locked. This range is narrower than the normal tracking range, and is a function of the loop filter characteristics and the input amplitude.

Conversion Gain: The ratio of output change to input change in a portion of the loop. In the phase detector, this is the ratio of output signal change, to a change in phase angle between the two inputs (volts/radian or μA/radian). Since the phase detector characteristic is generally a cosine curve, the gain is measured for small excursions about the 90° point. In the oscillator this is the ratio of output frequency change to an input change (% Δf/volt or % Δf/μA).

Current Controlled Oscillator (C.C.O.): A circuit which creates an A.C. output signal whose frequency is a function of the D.C. input current.

f_o: The free running frequency of the oscillator under a zero input signal condition.

Loop Gain: The product of the conversion gains of the loop elements (% Δf/radian), which is the ratio of change in input (and oscillator) frequency to the change in phase shift between input and oscillator. Therefore, loops with higher gains will hold the phase relationship closer to 90° for a given input frequency change, and conversely will have a broader tracking range.

Phase Detector (Phase Comparator): A circuit which creates an output level which is a function of the phase angle between two A.C. input signals. Most phase detectors are also amplitude sensitive.

Tracking Range (Lock-In Range): The range of input frequency about f_o under which a PLL, once locked, will remain locked. This is a function of loop gain, since the phase detector output is bounded and can drive the oscillator only over a certain frequency range. The tracking range may be controlled, if desired, by limiting the input signal to the oscillator.

Voltage Controlled Oscillator (V.C.O.): A circuit which creates an A.C. output signal whose frequency is a function of the D.C. input voltage.

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 602

A GENERAL ANALYSIS OF THE PHASE LOCKED LOOP

BY J.A. CONNELLY

INTRODUCTION

The concept of phase locked loops (PLL) was first proposed over forty years ago by de Bellescize in 1932.[1] De Bellescize investigated the subject of synchronous reception of radio signals where a receiver consisting of only a local oscillator, a mixer, and an audio amplifier was employed. The oscillator was adjusted to exactly the same frequency as the carrier frequency. With no frequency modulation of the carrier, an intermediate frequency of zero hertz was created. However, when the carrier was frequency modulated, the output from the mixer represented the desired demodulated information carried by the signal.

The principal shortcoming of the receiver system as proposed by de Bellescize was the practical limitation of achieving perfect synchronization between the carrier frequency and the frequency of the local oscillator. Any frequency mismatch hopelessly garbled the information. To achieve the desired operation, the local oscillator and transmitted signal had to be frequency and phase locked together with a degree of synchronization which was impractical at that time. Thus, the more complicated but more practical technique of the superhetrodyne receiver became the accepted approach for demodulation.

Subsequent to these early investigation by de Bellescize, numerous systems employing phase locked loops have been designed which overcame the practical constraints that plagued previous attempts. A few examples where successful phase locked loop operation has been achieved include the synchronization of horizontal and vertical scanning signals in television receivers, removal of the Doppler frequency shift in satellite tracking, stabilization of the frequency of klystron oscillators, and noise filtering in many communication systems. Virtually all of these applications of PLLs employ a variety of sophisticated circuit techniques utilizing complex, inductively tuned filters to achieve the required frequency stability. Other potential application areas of PLLs exist where the employment of this technique using discrete components remained either too complex or too expensive to be justifiable until the advent of the integrated circuit PLL.

The recent development of the integrated circuit phase locked loop (PLL) has enabled many of the practical limitations to be overcome which prevented utilization of most of the simpler and more direct instrumentation techniques.

Synchronous detection without tuned circuits is now feasible and economically advantageous. Also, PLLs can now be employed economically in a variety of related applications such as frequency multiplication and division, frequency synthesizers, tracking filters, motor speed monitoring and controls, modems, tone decoders, and FSK receivers. The purpose of this application note is to present the fundamental concepts involved with phase locked loops and to describe the operation of a typical PLL system.

PRINCIPLES OF PHASE LOCKED LOOPS

The function of a phase locked loop system is to detect and track small differences in phase and frequency existing between an incoming signal and a secondary reference signal. As shown in Figure 1, the PLL is basically an electronic servo loop consisting of a phase detector (PD), a low pass filter (LPF), and a controlled oscillator whose frequency is a linear function of either a dc voltage or current. In the following discussion, current control will be assumed to produce a current controlled oscillator (CCO).

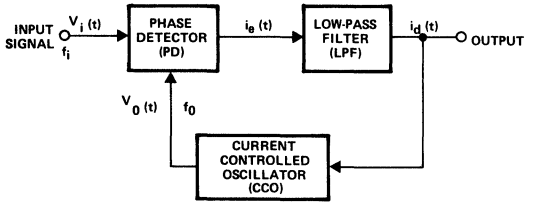


Figure 1

As the loop tracks the input signal, the PD compares the frequency of the input signal with the output from the CCO. A change in the phase of the input signal indicates that the incoming frequency is beginning to change. This change is detected by the PD, which produces and output directly proportional to the sum and difference in frequency and/or phase between the input signal and the signal from the CCO. The high frequency (sum) component of the phase detector's output is removed by the low pass filter, leaving a low frequency current signal. The output current from the LPF is an error signal whose magnitude is directly proportional to the phase difference between the two signals applied to the phase detector. This error signal is then used to adjust the frequency, and, consequently, the phase of the current controlled oscillator in such a direction as to establish phase synchronization between the two signals applied to the phase detector.

The closure of the loop and the establishment of phase lock between the PD inputs produces a configuration with negative feedback typical of those encountered in classical control systems. As such, many of the analytical techniques developed for determination of system stability, frequency response, tracking, and system optimization are directly applicable to phase locked loops. Since it is beyond the scope of the treatment intended here, the more interested reader is referred to several sources where developments of these techniques may be found.[2-4] It is hoped that the discussion which follows covering the operation of the phase detector, low pass filter, and current controlled oscillator will provide the necessary background for applying the control system techniques in the design of a particular phase locked system.

A LINEAR MODEL FOR A PLL SYSTEM

Whenever a phase lock is established between v_i (t) and v_o (t), the linear model of Figure 2 can be used to predict the performance of the PLL system. ϕ_i and ϕ_o represent the phase angles associated with the input and CCO respectively. F (s) represents a generalized current transfer function of the low pass filter in the frequency domain. K_d and K_o are the conversion gains of the phase detector and current controlled oscillator, each having units as shown.

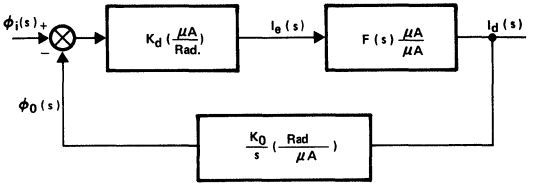


Figure 2

The representation of the phase detector as a summing network for combining ϕ_i (s) and ϕ_o (s) can be explained as follows. The phase detector is an analog multiplier which forms the product of an RF input signal v_i (t) and the output signal, v_o (t), from the current controlled oscillator. Assume that these two signals can be described by:

$$v_i(t) = V_i \sin w_i t \quad \text{and}$$

$$v_o(t) = V_o \sin(w_o t + \phi) \quad \text{where}$$

w_i, w_o, and are the frequency and phase characteristics of interest. The product of these two signals is an output current signal given by:

$$i_e(t) = K_1 V_i V_o (\sin w_i t)[\sin(w_o t + \phi)]$$

where K_1 is an appropriate dimensional constant. Note that the amplitude of i_e (t) is directly proportional to the amplitude of the input signal V_i.

The two cases of $w_i \neq w_o$ and $w_i = w_o$ are of interest and will now be considered separately.

Case I: $w_i \neq w_o$
When the two input frequencies to the phase detector are not synchronized, the loop is not locked. Furthermore, the phase angle ϕ is meaningless for this case since it can be eliminated by appropriately choosing the time origin. The phase detector's output current signal is given by:

$$i_e(t) = \frac{V_i V_o K_1}{2} [\cos (w_i - w_o)t - \cos(w_i + w_o)t]$$

When i_e (t) is passed through the low pass filter, F(s), the summed frequencies are attenuated, leaving:

$$i_d (t) = V_i V_o K \cos (w_i - w_o)t \quad \text{where}$$

K is a constant. This equation represents the signal current which is supplied to the CCO to control its output frequency. The equation shows that this signal sets up a beat frequency between w_i and w_o, causing the CCO's frequency to deviate by $\pm \Delta w$ from w_o in proportion to the signal amplitude ($V_i V_o K$) passing through the filter. If the amplitude of V_i is sufficiently large, and signal limiting or saturation does not occur, the CCO's output frequency will be shifted from the free running frequency, w_o', by some Δw until lock is established where $w_i = w_o = w_o' \pm \Delta w$. If lock cannot be established, then either (1) the input signal amplitude is too small to drive the CCO to produce the necessary $\pm \Delta w$ deviation, or (2) w_i is beyond the dynamic range of the CCO, i.e. $w_i \lesssim w_o' \pm \Delta w$. Obvious remedies for these "no lock conditions" are:

1. Increase the input signal's amplitude. This can be done either internally or externally to the loop by employing additional amplification.

2. Increase the internal loop gain by adjusting upward (larger - 3dB frequency) the response of the low pass filter.

3. Shift the free running frequency, w_o', of the CCO closer to the expected w_i frequency. Establishing frequency lock for the loop leads to the second case, namely phase lock where $w_i = w_o$.

Case II: $w_i = w_o$
When w_i and w_o are frequency synchronized, the output signal from the phase detector for $w_i = w_o = w$ and phase shift ϕ is:

$$i_e (t) = K_1 V_i V_o (\sin wt)(\sin wt + \phi)$$

$$= \frac{K_1 V_i V_o}{2} [\cos \phi - \cos (2wt + \phi)]$$

The low pass filter removes the high-frequency, ac part of $i_e(t)$ while leaving the dc component as a current signal for the CCO. Thus:

$$i_d (t) = I_d = \frac{K_2 V_i V_o}{2} \cos \phi$$

where K_2 is a dimensional constant.

Suppose w_i and w_o are perfectly synchronized to the free-running frequency w_o'. For this case I_d will be zero indicating that the ϕ must be 90°. Thus the error signal, I_d, is proportional to a phase difference between w_i and w_o centered about a reference phase angle of 90°. If w_i now changes from w_o', I_d will adjust and settle out to some non-zero value in order to correct w_o so that frequency lock is maintained with $w_i = w_o$. ϕ will be shifted by some amount, $\Delta \phi$, from the reference phase angle of 90°. This concept can be simplified by redefining ϕ as:

$$\phi = \phi_o \pm \Delta \phi \quad \text{where}$$

ϕ_o is the inherent 90° phase shift and $\Delta\phi$ represents departures from this reference value. Now the I_d becomes:

$$I_d = V_i V_o K_2 \cos(\phi_o \pm \Delta \phi) = \pm V_i V_o K_2 \sin \Delta\phi$$

Since the sine function is odd, a momentary change in $\Delta\phi$ contains information as to which way to adjust the CCO frequency to correct and maintain the locked condition. The maximum range over which Δ changes can be tracked is from -90° to +90°. This corresponds to a ϕ range from 0 to 180°.

In addition to being an error signal, I_d represents the demodulated output of an FM input applied as v_i (t) assuming a linear CCO characteristic. Thus, FM demodulation can be accomplished with the PLL without the inductively tuned circuits employed using conventional detectors.

The useful frequency range over which the PLL can track an input signal is called the Lock Range or alternatively, the Tracking Range. The lock range is determined primarily by the maximum frequency swing possible in the CCO and the maximum output current from the phase detector for the input signal level.

When the frequency of the input signal deviates from the reference frequency w_o', of the CCO by more than the tracking range, the loop becomes unlocked and the linear model of Figure 2 no longer describes the system. When this happens, the CCO runs at w_o' and the output current, I_d becomes zero.

Phase lock is reestablished when the input frequency approaches w_o'. The frequency range over which the PLL can acquire an input signal is denoted as the Capture Range which is set by the low pass filter's characteristics. The capture range is limited to a value less than the lock range.

For normal, phase lock operation, the frequency of the reference signal input, w_o', is first set under zero input signal conditions to establish the free-running frequency of the loop. A particular w_o' is normally positioned in the center of the frequency band of interest so that both positive and negative deviations of the input signal frequency about w_o' can be detected by the PLL. Next, the particular LPF configuration necessary from design considerations is determined for the system. The factors to be considered are the necessary capture range for the $\pm \Delta w$ modulations expected, high attenuation of the 2 w_i component from the phase detector, and the desired loop response to rapid changes in input frequency.

STABILITY CONSIDERATIONS OF PLL

Unexpected oscillations are always a possibility whenever feedback is employed to close a loop containing active elements. The stability, as well as the operation of the PLL of Figure 2, principally depends upon the characteristics of the low pass filter. A stability analysis using root locus techniques is given for several typical low pass filters. The purpose of the low pass filter is to surpress the summed frequencies ($w_i + w_o = 2w$) from the multiplier while preserving the dc signal represented by i_d. The selectivity, i.e. tracking and capture ranges, as well as the time response to changes in input frequency or phase angle, depend upon the frequency characteristics of this low pass filter. Any linear low pass filter will have the generalized response given by:

$$F(s) = \frac{\sum_{i=o}^{m} a_i s^i}{\sum_{j=o}^{n} b_j s^j} \qquad \text{where } m \leq n$$

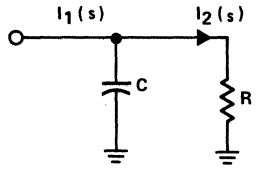
In typical filter applications, one particular pole will dominate in the F(s) expression, i.e. the lowest of the high frequency poles. As the location of this pole is moved closer to the zero frequency origin, the frequency selectivity of the PLL to the $w_i - w_o$ difference increases. This increase in frequency selectivity naturally reduces both the tracking and capture ranges.

When the PLL is tracking an input signal, the loop gain of Figure 2 is given by:

$$G(s)\,H(s) = \frac{K_d K_o F(s)}{s}$$

The simplest low pass filter is the RC network shown in Figure 3 which has a current transfer function given by:

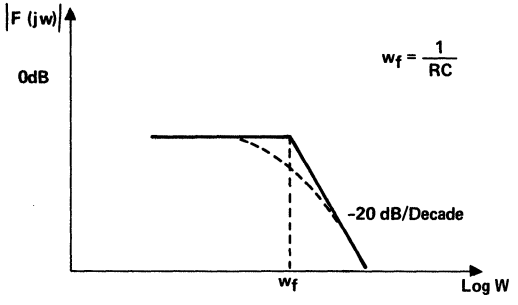
$$F(s) = \frac{I_2(s)}{I_1(s)} = \frac{1}{1 + \tau_f s} \qquad \text{where } \tau_f = RC$$



$$F(s) = \frac{I_2(s)}{I_1(s)} = \frac{1}{1 + s\tau_f}$$

where $\tau_f = RC$

(a) Circuit Configuration



(b) Frequency Characteristics

Figure 3

With this filter, the loop gain is:

$$G(s)\,H(s) = \frac{K_d K_o}{s\,(1 + \tau_f s)} = \frac{K}{s\,(1 + \tau_f s)} \quad \text{where}$$

$$K = K_d K_o$$

The root locus for the PLL with the simple RC filter is shown in Figure 4. This locus shows the behavior of the PLL when the loop is closed for all positive values of gain K. The locus begins on the poles, corresponding to K = 0 and preceeds along the real axis until the critical value of gain is reached. For K = K_{crit}, the closed loop response has the form:

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{K_{crit}/\tau_f}{s^2 + \frac{s}{\tau_f} + \frac{K_{crit}}{\tau_f}} = \frac{K_{crit}/\tau_f}{(s + \frac{1}{\tau_{crit}})^2}$$

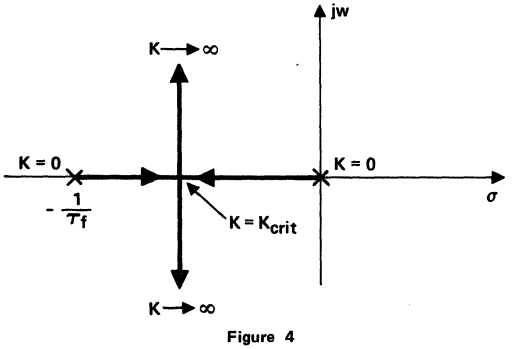


Figure 4

This equation shows that the system is critically clamped for this gain. When K > K_{crit}, the system will exhibit a damped sinusoidal response to an input phase angle step function. Since the root locus always lies in the left-half of the complex plane, the system is unconditionally stable for all K values.

In most phase lock loop systems, the conversion gains K_o and K_d are functions of parameters internal to the integrated circuit, and therefore not easily adjustable to achieve the desired system response. To overcome this shortcoming, an amplifier whose gain, A, is easily adjusted, can be inserted in the loop. When a typical amplifier with a single high frequency pole is employed, the loop gain becomes:

$$G(s)H(s) = \frac{K_o K_d A}{s(1+s\tau_f)(1+s\tau_a)} = \frac{K_1}{s(1+s\tau_f)(1+s\tau_a)}$$

where A and τ_a represent the amplifier's characteristics. The root locus describing this loop gain is shown in Figure 5. In constructing this plot, the pole due to the amplifier was arbitrarily made larger than the filter's pole. However, the general shape of the root locus is independent of the relative positions of these two poles. This locus illustrates that the system will become unstable for all values of gain K_1 greater than K_{crit}. However, stable operation can be achieved by limiting the maximum gain of the amplifier (as well as $K_o K_d$) to a value less than that which produces K_{crit}.

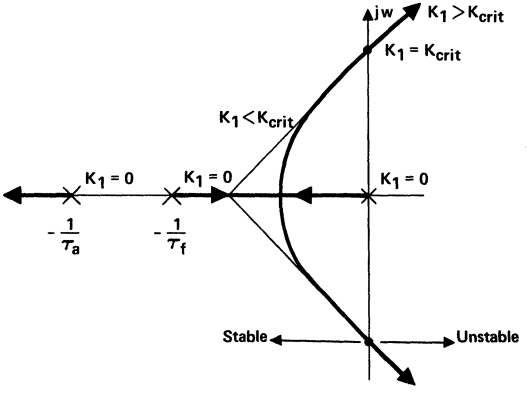
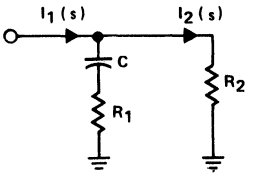


Figure 5

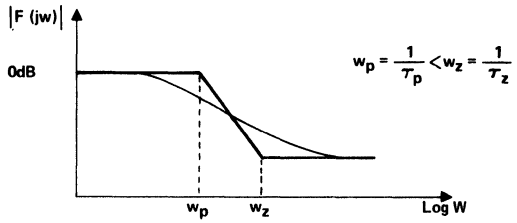
Stable PLL operation with adjustable gain can be achieved by utilizing a filter having both a pole and a zero such as that shown in Figure 6. When this filter and the previous amplifier are employed, the loop gain becomes:

$$G(s)H(s) = \frac{K_o K_d A\,(1 + s\tau_z)}{s(1 + s\tau_p)(1 + s\tau_a)}$$



$$F(s) = \frac{I_2(s)}{I_1(s)} = \frac{R_1 C s + 1}{(R_1 + R_2) C s + 1} = \frac{1 + s\tau_z}{1 + s\tau_p}$$

(a) Circuit Configuration

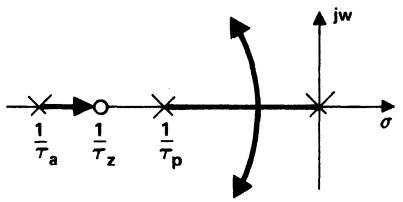


$$w_p = \frac{1}{\tau_p} < w_z = \frac{1}{\tau_z}$$

(b) Frequency Response

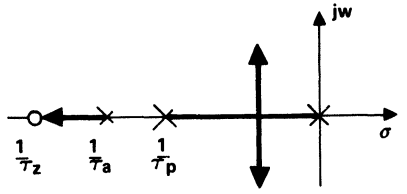
Figure 6

A number of different root loci are possible for this loop gain expression depending upon the relative locations of τ_z, τ_n, and τ_a. Figure 7 illustrates all possibilities and shows the loop is now stable for all values of gain. Introduction of the zero has the effect of pulling the root locus to the left away from the right-half plane where instability would result. The case shown in part (e) of Figure 7 is of particular interest, since it shows pole-zero cancellation between the amplifier and the low pass filter, resulting in the same root locus as previously given in Figure 3.



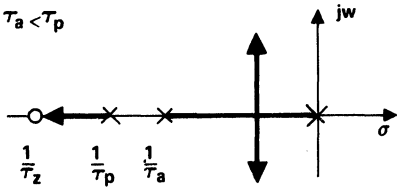
$\tau_a < \tau_z < \tau_p$

(a) Zero located between poles



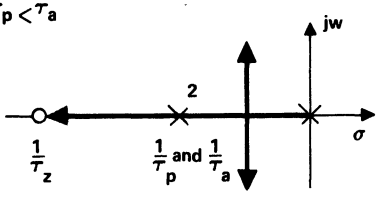
$\tau_z < \tau_a < \tau_p$

(b) Zero to the left of both poles with $\tau_a < \tau_p$



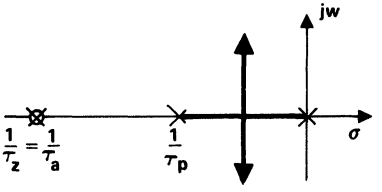
$\tau_z < \tau_p < \tau_a$

(c) Zero to the left of both poles with $\tau_p < \tau_a$



$\tau_z < \tau_p = \tau_a$

(d) Equal poles



$\tau_z = \tau_a < \tau_p$

(e) Poles - Zero cancelation

Figure 7

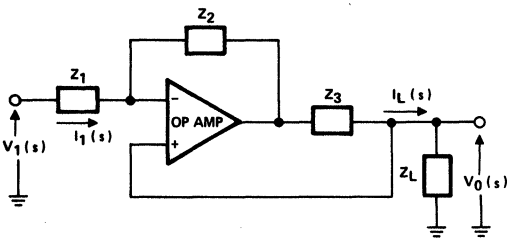
Many other filter configurations for PLL operation could be examined if space permitted. However, the utilization of active filters with PLL presents many especially interesting possibilities, one example of which follows. Figure 8 shows a typical, generalized circuit configuration for an active filter, which has the voltage and current transfer responses indicated. These transfer responses were obtained assuming an ideal operational amplifier ($A_V \rightarrow \infty$, $Z_{in} \rightarrow \infty\ \Omega$, $Z_{out} \rightarrow 0\Omega$).

The current transfer function is particularly significant since it indicates that the output current is not a function of the load impedance Z_1. Thus, in addition to being an active filter, this network can be made to supply a constant current to a varying load impedance.

As a special example of the active filter of Figure 8, assume that impedances are chosen according as:

$$Z_1 = 0 \quad Z_2 = R_2 + \frac{1}{sC_2}$$

$$Z_3 = R_3 \qquad Z_1 = R_1$$



$$\frac{V_0(s)}{V_1(s)} = \frac{Z_L Z_2}{Z_L Z_2 - Z_1 Z_3}$$ Forward Voltage Transfer Function

$$\frac{I_L(s)}{I_1(s)} = -\frac{Z_2}{Z_3}$$ Forward Current Transfer Function

Figure 8

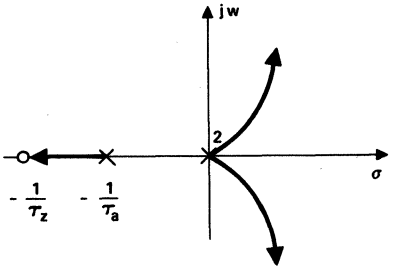
Chosen thusly, the response of the active filter is given by:

$$F(s) = \frac{I_L(s)}{I_1(s)} = -\frac{1}{R_3C_2}\left[\frac{1+s\tau_Z}{s}\right] = K_f\left[\frac{1+s\tau_Z}{s}\right]$$

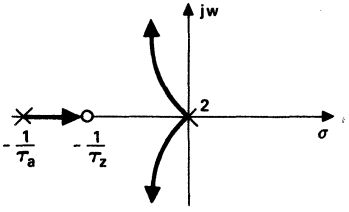
where $\tau_Z = R_2C_2$. For very small τ_Z, the low pass filter is essentially an integrator. When this filter is employed in the PLL, the loop gain becomes:

$$G(s)H(s) = \frac{K_0K_dK_fA(1+s\tau_Z)}{s^2(1+s\tau_a)} = \frac{K_2(1+s\tau_Z)}{s^2(1+s\tau_a)}$$

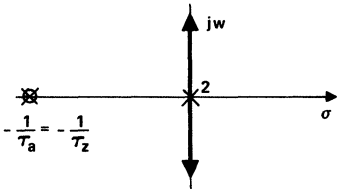
Three root loci are possible depending upon the relative locations of τ_Z to τ_a, as shown in Figure 9. As can be seen, stability is only guaranteed for part (b) where the zero of the filter lies between the poles. Part (c) where the locus coincides with the imaginary axis is considered "marginally stable". However, it is not useful practically.



(a) Zero to the left of amplifier's pole



(b) Pole to the left of active filter zero



(c) Pole-zero cancellation

Figure 9

STEADY-STATE RESPONSE OF PLL

The steady-state response of a phase locked loop system to stimulation afforded by various types of input signals is of equal importance to the system's stability. Frequently, while the employment of a certain low pass filter may guarantee stability, it may produce a system with unsatisfactory steady-state characteristics for the types of input signals expected. The development which follows will be useful for determining the particular type of low pass filter needed to enable the system to respond to step function, ramp and acceleration inputs.

With reference again to the linear model of the PLL system shown in Figure 2, the current signal $I_e(s)$ represents the phase error that exists between the incoming reference signal $\phi_i(s)$ and the feedback signal $\phi_o(s)$. The final value theorem associated with Laplace transformations, namely:

$$\lim_{t \to \infty} [I_e(t)] = \lim_{s \to 0} [s\, I_e(s)]$$

will be used to find the steady state error without transforming back to the time domain. The phase error signal is given by:

$$\theta_e(s) = \frac{K_d s}{s + K_d K_o F(s)} \theta_i(s)$$

For unit step function input,

$$\theta_i(s) = \frac{1}{s}$$

For a unit ramp input,

$$\theta_i(s) = \frac{1}{s^2}$$

For a unit acceleration input.

$$\theta_i(s) = \frac{1}{s^3}$$

The steady state responses of the error signal for these three inputs are:

$$\text{STEP: } \lim_{t \to \infty} [\theta_e(t)] = \lim_{s \to 0} \frac{K_d s}{s + K_d K_o F(s)}$$

$$\text{RAMP: } \lim_{t \to \infty} [\theta_e(t)] = \lim_{s \to 0} \left[\frac{K_d}{s + K_d K_o F(s)} \right]$$

$$\text{ACCELERATION: } \lim_{t \to \infty} [\theta_e(t)] = \lim_{s \to 0} \left\{ \frac{K_d}{s[s + K_d K_o F(s)]} \right\}$$

As long as the filter is truly low pass, namely having a general response given by:

$$F(s) = \frac{\sum_{i=0}^{m} a_i s^i}{\sum_{j=0}^{n} b_j s^j} \qquad \text{where } m \leq n$$

the following simplifications are possible:

$$\text{STEP: } \lim_{t \to \infty} [\theta_e(t)] = 0 \quad \text{for any } F(s)$$

$$\text{RAMP: } \lim_{t \to \infty} [\theta_e(t)] = \frac{1}{K_o} \lim_{s \to 0} \frac{1}{F(s)}$$

$$\text{ACCELERATION: } \lim_{t \to \infty} [\theta_e(t)] = \frac{1}{K_o} \lim_{s \to 0} \frac{1}{s F(s)}$$

Thus the PLL will track a step input with zero steady state error regardless of the low pass filter. In order to achieve zero steady state error for an acceleration input, the low pass filter must have at least two poles positioned at the origin (type 2 filter). Table I shows the expected steady state error for the different inputs when type 1, type 2, and type 3 low pass filters are employed.

INPUT	TYPE 0	TYPE 1	TYPE 2
STEP	ZERO	ZERO	ZERO
RAMP	CONSTANT	ZERO	ZERO
ACCELERATION	CONTINUALLY INCREASING	CONSTANT	ZERO

TABLE 1
STEADY-STATE ERRORS OF VARIOUS FILTER TYPES FOR THREE DIFFERENT INPUTS

CONCLUSIONS

This application note describes the basic theory of Phase Locked Loop operation and develops a linear model for predicting the performance of a typical system. The effects of several typical low pass filters upon system stability and response are described using root locus and steady state error analysis techneques.

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2. Chestnut, H. and R. W. Mayer, Servomechanisms and Regulating System Design, Wiley, New York, 1959
3. D'Azzo, J. J. and C. H. Houpis, Feedback Control System Analysis and Synthesis, McGraw - Hill, New York, 1966
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HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

APPLICATION NOTE 605

THE HA-2820/2825 LOW FREQUENCY PHASE LOCKED LOOP

BY J. A. CONNELLY

INTRODUCTION

The HA-2820/2825 are monolithic integrated circuits designed to serve a wide variety of phase locked loop applications in the broad frequency range between 0.1Hz and 3MHz. The circuit contains a phase detector, a current controlled oscillator, a level shifter, and an associated bias network. A block diagram of the HA-2820/2825 is shown in Figure 1

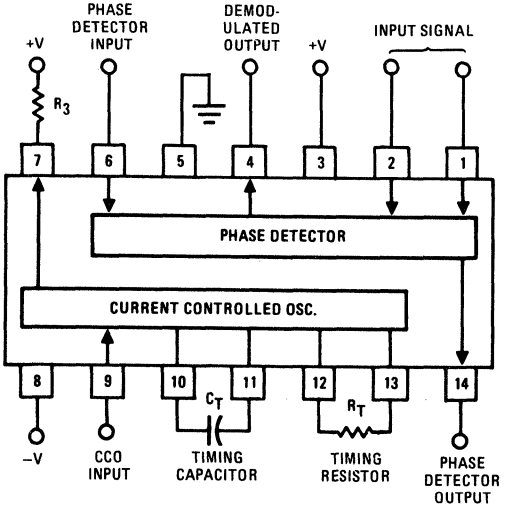


Figure 1
Block Diagram of the HA-2820/2825 PLL

illustrating the active PLL functions together with the pin-out locations. As this figure shows, all connections between the detector and oscillator are made externally which allows for maximum design flexibility in the selection of the low-pass filter, counters, etc. typically included within a phase locked loop (PLL). In this application note, we will first describe the circuit operation of the HA-2820/2825 and then discuss several points to keep in mind when making external connections to the device.

CIRCUIT OPERATION

The schematic diagram for the HA-2820/2825 is shown in Figure 2. The dashed lines partition the various functional blocks for ease of identification. We will now briefly analyze the operation of the circuitry contained within these blocks.

A. PHASE DETECTOR

The heart of the phase detector is the four-quadrant multiplier consisting of three differential pairs, i.e. Q6-Q9, Q11-Q13, and Q7-Q12. Transistors Q1, Q5, Q8, Q10, and Q14 provide a constant current bias for these differential pairs. Before considering the operation of the entire multiplier, let's examine a single stage as shown in Figure 3. Since the two transistors operate in their linear regions, we can write the following expressions for their collector currents:

$$(1)\quad I_2 = I_{se}^{\gamma V_{BE2}}$$

$$(2)\quad I_1 = I_{se}^{\gamma (V+V_{BE2})}$$

where $\gamma = \frac{q}{kT}$ and

I_S is the reverse saturation current. Let's now assume equal collector and emitter currents and recognize that:

$$(3)\quad I_0 = I_1 + I_2$$

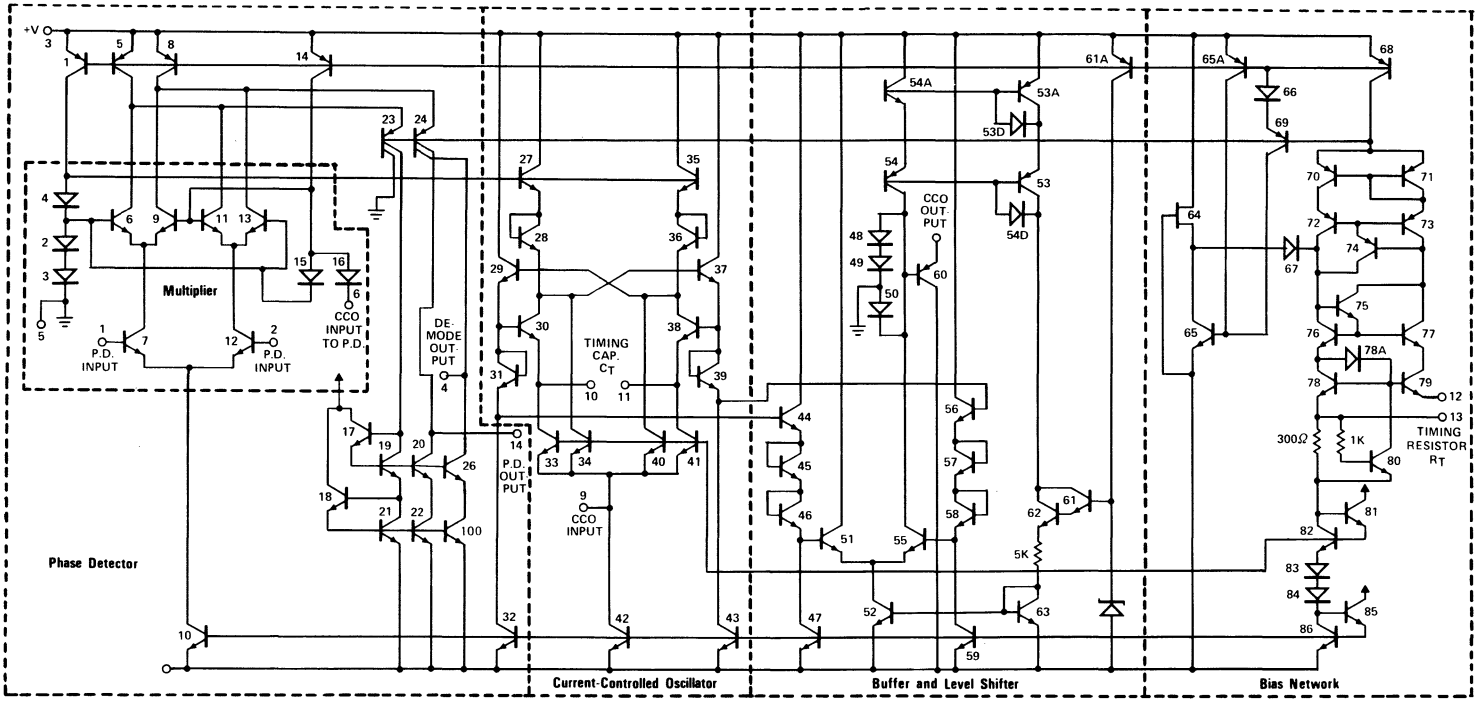


Figure 2
HA-2820/2825 Low Frequency Phase Locked Loop
Schematic Diagram

After some algebraic manipulation, we can write:

$$(4)\ I_2 = \frac{I_0}{1 + e^{\gamma V}} = I_0\, F_2\,(V)$$

and $$(5)\ I_1 = \frac{I_0\, e^{\gamma V}}{1 + e^{\gamma V}} = I_0\, F_1\,(V)$$

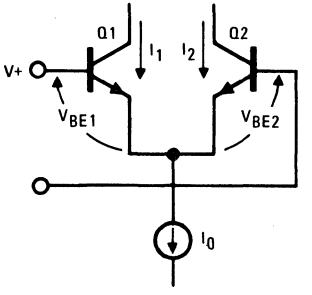


Figure 3
A Single Stage Differential Pair

Now we'll apply these basic equations to the complete multiplier shown in Figure 4 which has two separate voltages applied, namely V_A and V_B. By direct comparison of the currents in the two figures, we can write the following set of equations:

$$(6)\begin{cases} I_{1A} = \dfrac{I_{mx}\, e^{\gamma V_B}}{1 + e^{\gamma V_B}} = I_{mx}\, F_1(V_B) \\ I_{1B} = \dfrac{I_{mx}}{1 + e^{\gamma V_B}} = I_{mx}\, F_2\,(V_B) \end{cases}$$

$$(7)\begin{cases} I_{3A} = I_{1A}\, F_2\,(V_A) \\ I_{3B} = I_{1B}\, F_2\,(V_A) \end{cases}$$

$$(8)\begin{cases} I_{2A} = I_{1A}\, F_1\,(V_A) \\ I_{2B} = I_{1B}\, F_1\,(V_A) \end{cases}$$

$$(9)\begin{cases} I_{4A} = I_{2A} + I_{3B} = I_{1A}\, F_1(V_A) + I_{1B}\, F_2(V_A) \\ I_{4A} = I_{mx}[F_1(V_B)F_1(V_A) + F_2(V_B)F_2(V_A)] \end{cases}$$

$$(10)\begin{cases} I_{4B} = I_{3A} + I_{2B} = I_{1A}\, F_2(V_A) + I_{1B}\, F_1(V_A) \\ \quad = I_{mx}[F_1(V_B)F_2(V_A) + F_2(V_B)\, F_1(V_A)] \end{cases}$$

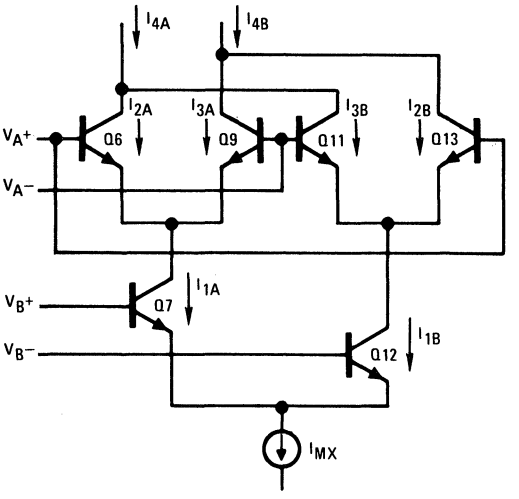


Figure 4
The Four-Quadrant Multiplier

Now by subtracting Equation 10 from 9, we have:

$$(11)\begin{cases} I_{4A} - I_{4B} = I_{mx}\,[F_1(V_B)F_1(V_A) + F_2(V_B) \\ \quad F_2(V_A) - F_1(V_B)F_2(V_A) - F_2(V_B)F_1(V_A)] \\ I_{4A} - I_{4B} = I_{mx}\left[\dfrac{e^{\gamma V_B}\, e^{\gamma V_A} + 1 - e^{\gamma V_B} - e^{\gamma V_A}}{(1 + e^{\gamma V_B})\,(1 + e^{\gamma V_A})}\right] \\ = I_{mx}\left[\dfrac{e^{\gamma V_B/2} - e^{-\gamma V_B/2}}{e^{\gamma V_B/2} + e^{-\gamma V_B/2}}\right]\left[\dfrac{e^{\gamma V_A/2} - e^{-\gamma V_A/2}}{e^{\gamma V_A/2} + e^{-\gamma V_A/2}}\right] \\ = I_{mx} \tanh\left(\dfrac{\gamma V_e}{2}\right) \tanh\left(\dfrac{\gamma V_A}{2}\right) \end{cases}$$

Now recall that the series expansion for tanh x is:

$$\tanh x = x - \frac{x^3}{3} + \frac{2\,x^5}{17} - \text{--------}$$

For small V_A and V_B, we will retain only the first term of the expansion which allows Equation 11 to be approximated as:

$$(12)\ I_{4A} - I_{4B} \approx I_{mx}\frac{\gamma^2}{4} V_A\, V_B$$

Thus, the difference between these two I_4 currents is directly proportional to the product of the voltages V_A and V_B. Transistors Q17 through Q26 convert the I_4 difference current into an output current given by:

$$(13)\ I_d = K\, V_A\, V_B$$

where K is a dimensional constant.

Two separate output currents are available from the phase detector at Pins 4 and 14. These currents are of equal magnitude and phase. Since they are buffered by Q24, two different filters may be connected at these pins with negligible interactions. In a typical application, a low-pass filter is employed inside the loop between Pin 14 and the CCO input while a second filter, external to the loop, is utilized at the demodulated output (Pin 4). Later in this paper we will discuss the filter connection to these high impedance, current-source outputs.

B. CURRENT CONTROLLED OSCILLATOR

The current controlled oscillator portion of the HA-2820/2825 is identified on the schematic diagram of Figure 2. The circuit is basically an emitter-coupled astable multivibrator with an external input provided at Pin 9 where a DC current can be applied to change the frequency of oscillation. A detailed explanation of astable operation may be found in Millman and Taub. Therefore, only a brief description of the timing and current-control modifications added to the basic circuit will be presented here.

The free-running or center frequency of oscillation, f_O, of the CCO is set by the combination of an external capacitor, C_T, connected between Pins 10 and 11 and by an external resistor, R_T, connected between Pins 12 and 13. A signal current is then applied at Pin 9 to modulate the CCO frequency around f_O.

In beginning our analysis of the CCO circuit operation, let's assume that an R_T resistor is in position and that no current signal is applied at Pin 9. The R_T resistor in the bias network establishes equal quiescent currents in the following transistor pairs: Q33 and Q41; Q34 and Q40; and Q30 and Q38. These quiescent currents vary inversely with the value of R_T. Without a timing capacitor, C_T, in the circuit, no feedback is provided around the amplifier made up of Q29, Q30, Q37, and Q38, and the multivibrator will not oscillate. The string of transistors on the left and right sides of an imaginary center line through the CCO will draw equal stand-by currents.

Connection of C_T completes the CCO feedback loop and initiates multivibrator oscillations since the amplifier gain exceeds unity. Current is switched alternatively between Q30 and Q38 through C_T. When Q30 conducts heavily, its collector voltage is lower than that of Q38. Q30 then carries the entire current for the pair. The additional current required by the constant current source, Q42, is supplied by removing charge from C_T. This action causes the emitter voltage of Q38 to fall until Q38 conducts heavily. The collector voltage of Q38 falls, turning off Q30. The collector voltage of Q30 rises turning on Q38 even more heavily. This process is repeated during the next half-cycle with the roles of Q30 and Q38 reversed. Figure 5 shows typical emitter and collector waveshapes.

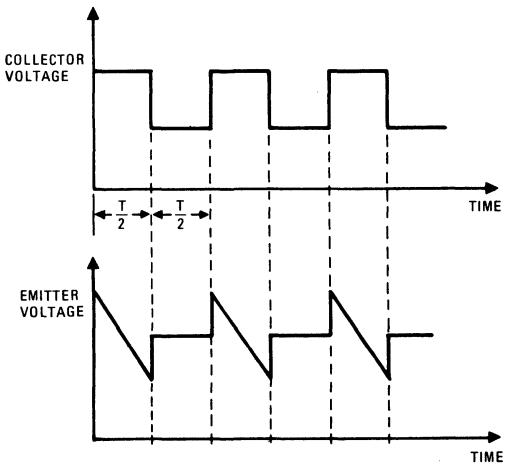


Figure 5
Typical Multivibrator Waveshapes

During the rapid transition periods at the beginning of each half-cycle, the timing capacitor appears as an AC short circuit. The capacitor discharges at a constant rate directly proportional to the current set by R_T during the ramp portion of each cycle. The timing capacitor, C_T, controls the slope of the ramp discharge. Thus, the free-running frequency of the CCO can be expressed by:

$$(14)\ f_O = \frac{K_1 I_O}{C_T} = \frac{K_2}{R_T C_T}$$

where K_1 and K_2 are dimensional constants and I_O is the discharge controlled by R_T.

Now, let's consider circuit operation when an external current signal is applied at the CCO input (Pin 9). An external current modulates I_O, thereby causing the CCO output frequency to deviate by $\pm\Delta f$ about f_O.

The extent of the deviation is linearily proportional to the applied external current. Thus, we can describe the output frequency by:

(15) $f_{CCO} = f_o + K_o I_{mod}$

where K_o is the conversion gain of the CCO.

C. BUFFER AND LEVEL SHIFTER

The differential signals from the CCO (emitters of Q31 and Q39) drive the Darlington input differential amplifier composed of transistors Q44, Q51, Q55, and Q56. The single-ended, current-signal output at the collector of Q55 is level shifted by Q54. The diode network of D48, D49, and D50 limits the voltage excursions at the collector of Q54 to the range of from −.7V to +1.4V. The emitter follower, Q60, provides a low impedance output from the CCO (Pin 7) with a typical voltage swing of +2.1V above ground. (An external pull-up resistor is normally connected to Pin 7 and +V supply. The resistance value should be chosen for a typical current of approximately 1mA through Q60). These levels of 0 and 2.1V make the CCO output directly compatible with TTL gates and counters.

D. BIAS NETWORK

The bias network establishes the appropriate quiescent voltages and currents for the other functional circuits on the monolithic chip. The network has been carefully designed so that a remarkable temperature stability of 100ppm is typical. Power supply rejection typically is an outstanding 0.1% / V.

As we saw previously in Equation 14, the external R_T resistor in the bias network controls the discharge current, I_o, in the CCO. The K_1 factor in this equation contains a term which varies inversely with temperature. To compensate the CCO frequency against temperature variations, the bias network purposely introduces a linear variation if I_o with temperature. Since the CCO frequency is a function of the product of K_1 and I_o, these effects compensate and the CCO frequency is highly stable in the presence of temperature changes.

CONNECTION TO THE HA-2820/2825

Having examined the internal circuitry of the IC, we are better equipped to discuss the external connections to the HA-2820/2825. Let's consider the connections to the PLL shown in Figure 6. This is a test circuit which is typical of many applications such as FM demodulation, modems, SCA receivers, tracking filters, etc.

The circuit configuration shown is recommended for AC coupling a differential input signal into the HA-2820/2825. The R_S resistors are chosen to match the signal line's characteristic impedance. The C_S coupling capacitors must be large enough to pass the lowest input frequency of interest. As Figure 6 shows, the input signal may be direct coupled into Pins 1 and 2 with a 0V reference level. (A DC path to ground must be provided for the base bias currents to the input transistors). If DC coupling is used, the magnitude of the input signal must be limited to not more than 0.5 VRMS to prevent nonlinear multiplier operation. Also, if direct coupling is employed, any DC drift present in the signal source will cause the CCO frequency to drift also. This occurs because the drift passes through the phase detector and low-pass filter and appears as a modulating signal to the CCO. Operation with a single-ended input to the phase detector is also possible by simply removing one of the C_S coupling capacitors and applying a signal to the other input, either directly or through the other coupling capacitor.

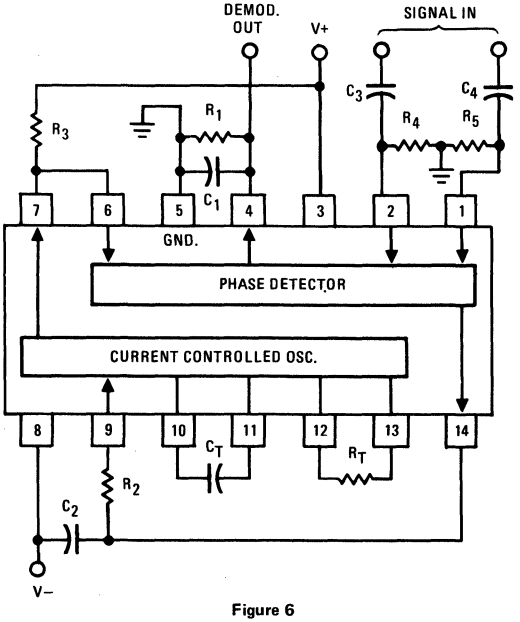


Figure 6
PLL Test Circuit Showing Typical External Connections

The second input to the phase detector is the feedback signal applied to Pin 6. This signal is available directly at the CCO output (Pin 7)

and is externally connected as shown in Figure 6 for many demodulator applications. The phase detector input at Pin 6 and the CCO output at Pin 7 are TTL compatible. Therefore, a frequency counter can easily be inserted at this point within the loop for frequency synthesis applications.

The phase detector has two identical outputs, available at Pins 4 and 14. A passive, low-pass current filter (R_1-C_1) is connected as shown in Figure 6 to obtain a demodulated output. Since this is a high impedance output, the amplitude of the demodulated voltage is controllable with R_1 adjustment as as shown in Figure 7.

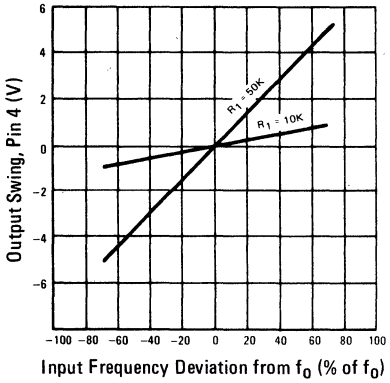
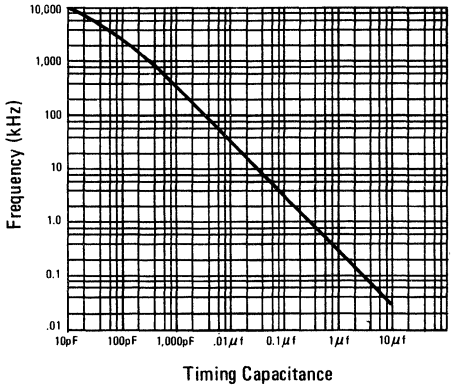


Figure 7
Demodulated Output Swing
Versus Input Frequency Deviation

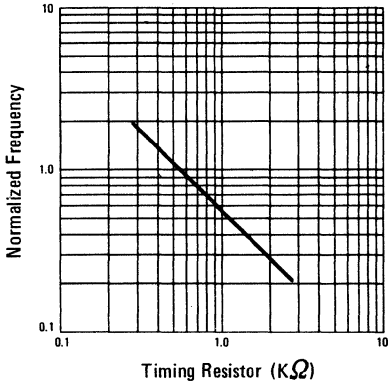
The second output from the phase detector is externally connected to the CCO input through a second, low-pass filter. A single-pole, passive filter (R_2-C_2) is shown in Figure 6. Because the filter is completely external to the PLL, the designer has the flexibility to use more complicated, multi-pole active and passive filters here. Such filters can be used to set the capture and tracking ranges as is explained in Application Note 606.

Capacitor C_T and resistor R_T set the free-running frequency, f_0, of the CCO. Figure 8 displays the f_0 variations for six decade range of C_T values and a decade range of R_T. In many typical applications, C_T is used for making a coarse setting of f_0. R_T is made a potentiometer and varied for fine control of f_0. R_T and C_T must be highly temperature stable to minimize f_0 drift. Figure 9 shows the typical and guaranteed frequency drift for f_0 versus temperature for the HA-2820/2825.

As this figure illustrates, the temperature coefficient for the PLL is a remarkable 100ppm/°C over the appropriate temperature range.



(A) Center Frequency Versus C_T



(B) Center Frequency Versus R_T

Figure 8
Setting the Center Frequency f_0

External modulation of the CCO frequency around f_0 is accomplished by applying a signal current to Pin 9. It should be remembered that the signal current is returned to an input, open-circuit voltage at Pin 9 which is about 2.5V more positive than the negative supply. The CCO input impedance here is typically 500Ω, and it may be necessary to consider this value when designing the appropriate low-pass filter. Figure 10 shows the f_0 variation versus input signal current. The conversion gain, K_0 of the CCO is obtained by multiplying the slope of this curve by f_0.

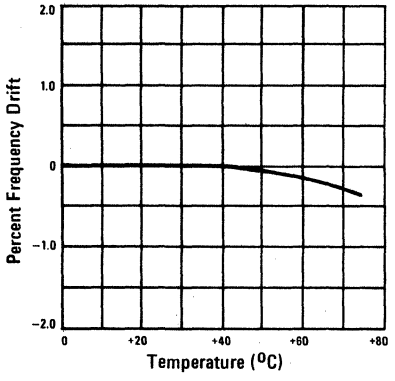


Figure 9
Frequency Drift Versus Temperature

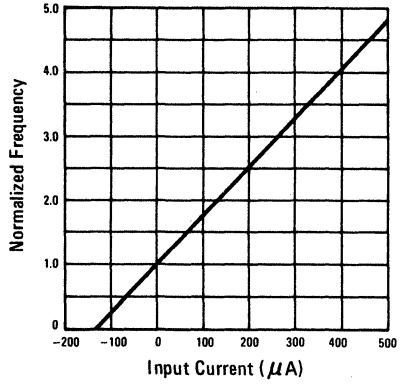


Figure 10
Oscillator Frequency Versus Input Current

Figure 11 shows the loop gain characteristic (frequency deviation versus phase angle) for the HA-2820/2825. The conversion gain of the phase detector, K_d is determined as the quotient of the slope of the loop gain characteristic divided by the slope of the CCO curve of Figure 10. As Figure 11 shows, the loop gain characteristic depends upon the input signal amplitude. Since the dependence is approximately linear, the slope of the loop gain characteristic can be scaled to correspond to the expected signal amplitude. Application Note 603 provides a further insight into parameter determination of PLL's from data available on the specification sheet.

A pull-up resistor, R_3, is typically employed at the CCO output (Pin 7) as shown in Figure 6. The resistor value is critical only to the extent that it must limit the maximum current through the output transistor to less than 5mA. For applications involving frequencies above approximately 1MHz, decreasing R_3 (while still keeping the current less than 5mA) will improve the transient performance of the CCO output.

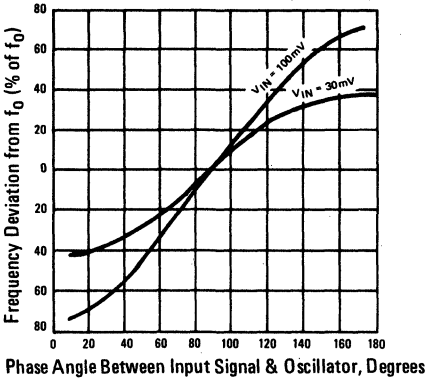


Figure 11
Loop Gain Characteristic

CONCLUSION

This application note explains the circuitry of the HA-2820/2825 Low Frequency Phase Locked Loop in order to provide a better understanding of the performance characteristics of the device. Methods are discussed for obtaining useful parameters of a linear PLL model from the device's performance curves. Considerations involved in making external connections to the device are presented and illustrated with a typical FM demodulator circuit.

Chip Information

GENERAL INFORMATION

Most of the Harris Analog standard products are available in chip form to the hybrid micro circuit designer. The standard chips are DC electrically tested at +25°C to the data sheet limits for the commercial device and are 100% visually inspected to MIL-STD-883, Method 2010, Condition B criteria. Packaging for shipment consists of waffle pack carriers plus an anti-static cushioning strip for extra protection.

The hybrid industry has rapidly become more diversified and stringent in its requirements for integrated circuits. To meet these demands Harris has several options additional to standard chip processing available upon request at extra cost. These options include; gold-backing, guaranteed DC specifications over the military temperature range. For more information consult the nearest Harris Sales Office or Representative.

CHIP ORDERING INFORMATION

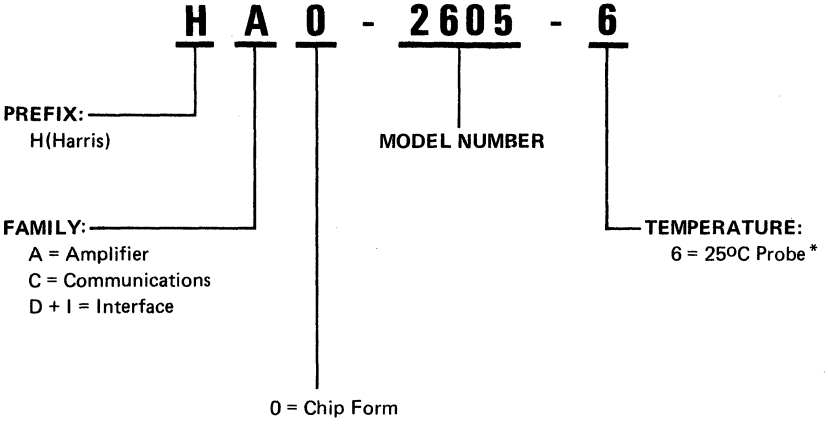
Standard and special chip sales are direct factory order only. The minimum order on all sales is $250.00 per line item. Contact the local Harris Sales Office or Representative for pricing and delivery on special chip requirements.

MECHANICAL INFORMATION

Dimensions: All chip dimensions nominal with a tolerance of ±.003".
Maximum chip thickness is .012".

Bonding Pads: Minimum bonding pad size is .004" x .004" unless otherwise specified.

PRODUCT CODE EXAMPLE



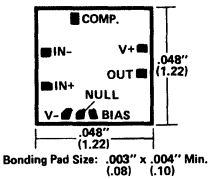
*Contact Harris for availability of -2 (-55°C to +125°C) dice.

Chip Geometries

1. All dimensions in inches, millimeters are shown in parentheses.
2. Unless otherwise specified, minimum bonding pad size for all devices is .004" x .004" (.10mm x .10mm).

OPERATIONAL AMPLIFIERS & COMPARATORS

HA0-911



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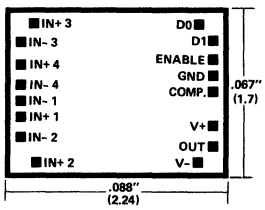

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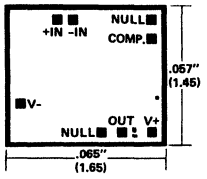

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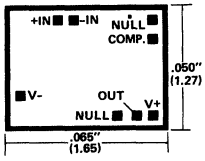

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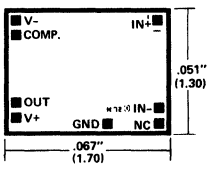

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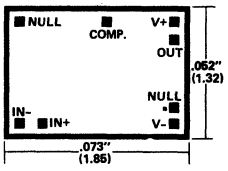

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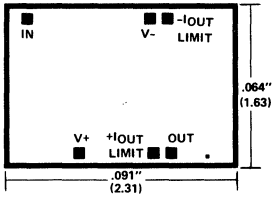

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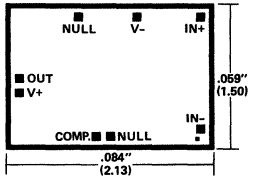

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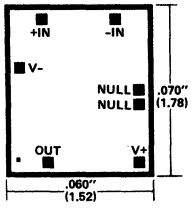

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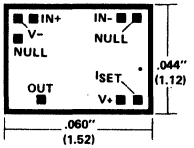

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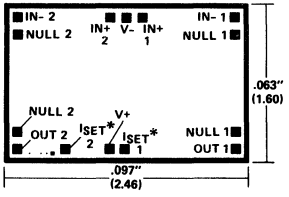

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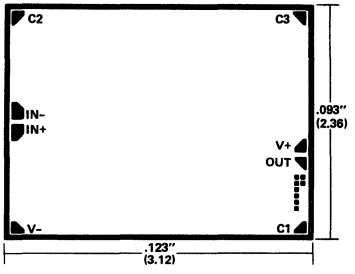

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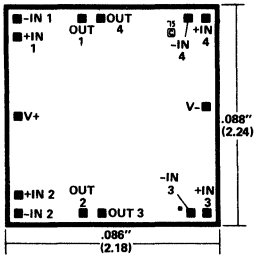

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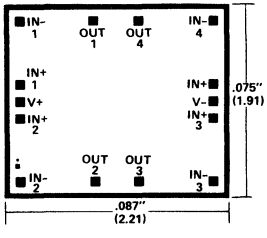

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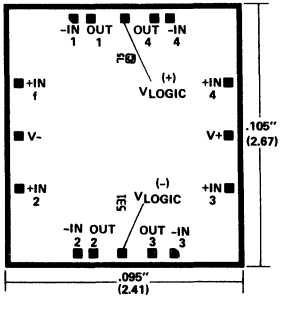

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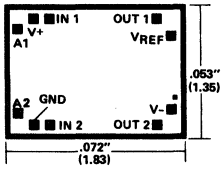

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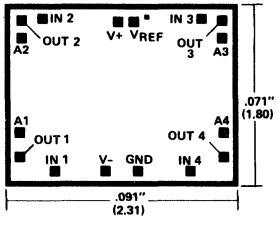

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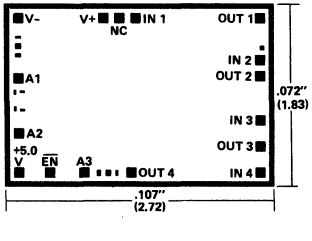

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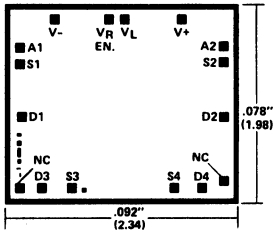

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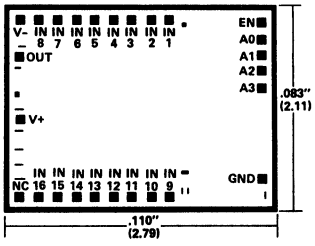

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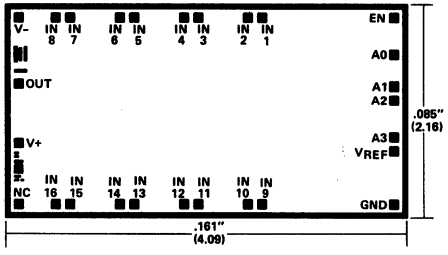

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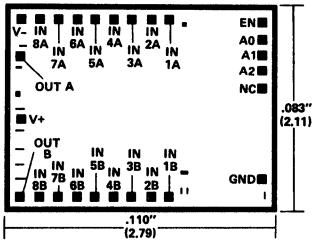

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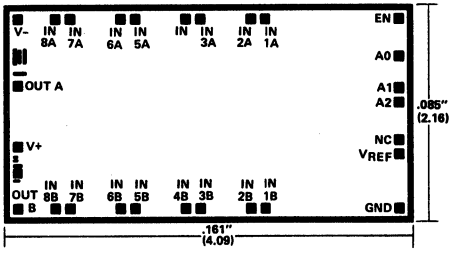

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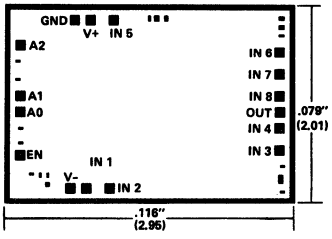

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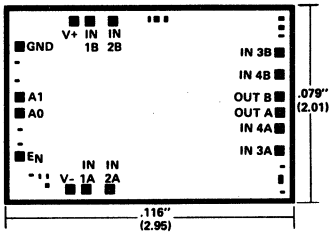

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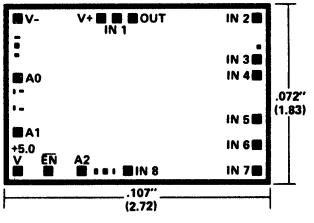

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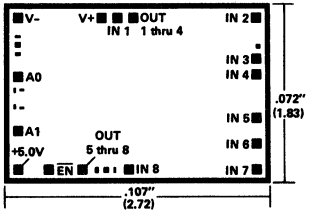

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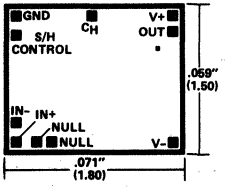

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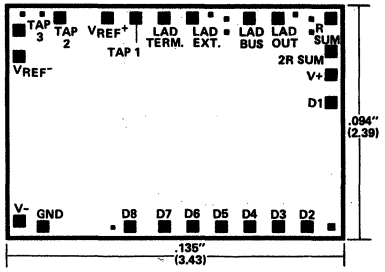

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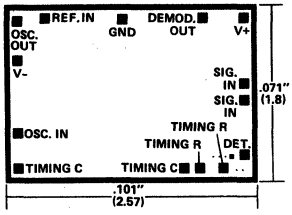

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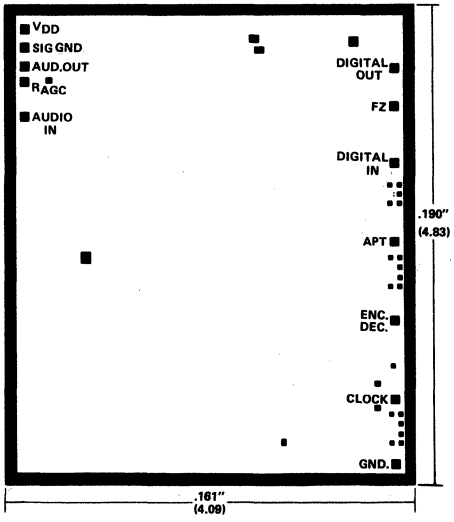

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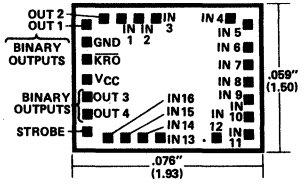


Harris
Quality and Reliability Programs

DASH 8 Program

MIL-STD-883
OFF-THE-SHELF DELIVERY

MIL-STD-883/MIL-M-38510 MIL-Q-9858A

INTRODUCTION

STATEMENT OF SCOPE

This section establishes the detail requirements for Harris' Circuits screened and tested under the Product Assurance Program.

The Harris DASH 8 Devices pass the screening requirements of the latest issue of MIL-STD-883, Method 5004, Class B, and the requirements as specified in this document. Included in this Section are the quality standards and screening methods for commercial parts which must perform reliably in the field.

APPLICABLE DOCUMENTS

The following Military documents form a part of this section to the extent referenced herein and provide the foundation for Harris Products Assurance Program.

MIL-M-38510	"General Specification of Microcircuits"
MIL-Q-9858A	"Quality Program Requirements"
MIL-STD-883	"Test Methods and Procedures for Microelectronics"
NASA Publication 200-3	"Inspection System Provisions"

Harris maintains a Product Assurance Program (PAP) using MIL-M-38510 as a guide. Harris Product Assurance Program assures compliance with the requirements and quality standards of control drawings and the requirements of this specification.

The DASH 8 Program will also be found useful by those Harris customers who must generate their own procurement specifications. Use of the enclosed Harris Standard Test Tables, Test Parameters, and Burn-In Circuits will aid in reducing specification negotiation time.

PRODUCT ASSURANCE AT HARRIS

Our Product Assurance Department strives to assure that the quality and reliability of products shipped to customers is of a high quality level and consistent with customer requirements. During product processing, there are several independent visual and electrical checks performed by Quality Assurance personnel.

Prior to shipment, a final inspection is performed at Quality Assurance Plant Clearance to insure that all requirements of the purchase order and customer specifications are met. The system and procedures used and implemented are in accordance with MIL-M-38510, MIL-Q-9858A, MIL-STD-883A, MIL-C-45662 and MIL-I-45208.

The Harris Semiconductor Reliability and Quality Manual which is available upon request, describes the total function and policies of the organization to assure product reliability and quality.

HARRIS SEMICONDUCTOR DASH 8 PRODUCT FLOW
MIL-M-38510/MIL-STD-883, METHOD 5004 CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1080 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1001 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: (A) Fine (B) Gross	1014 Cond. A or B 1014 Cond. C2, no vacuum pre-cond. Step 2.
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Subgroups A1, A2, A3, A7, Functional tests per Table I
9	External Visual	2009 Sample Inspection
10	Lot Acceptance	Table I, Group A Elect. Tests

Note:

Traceability: All devices are assigned date code identification that provides traceability back to the inspection lot.

Branding: All devices are branded with the HX-XXXX-8 and EIA date code.

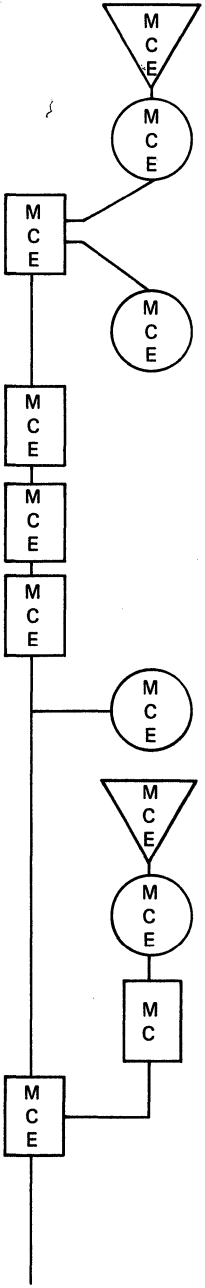
Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to group A inspection requirements.

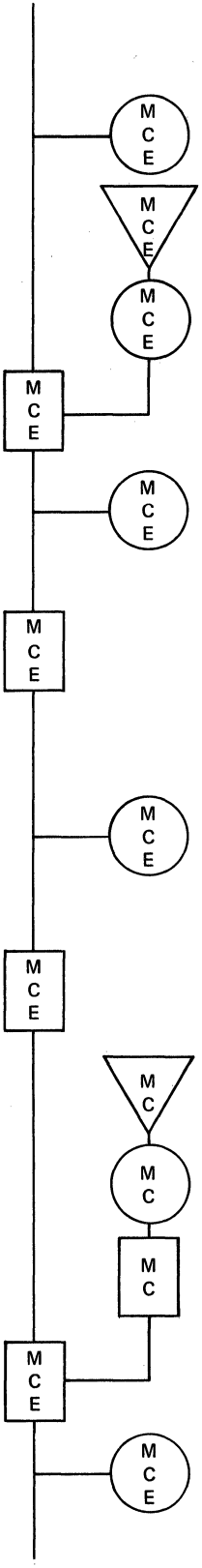
Additional Requirements: Attributes data will be supplied on Group A Lot Acceptance upon request.

Generic data from Harris' Reliability Add-On Program is available upon request. The objective of Harris Reliability Add-On Program is to provide a continuous life and environmental monitor for all products families in manufacturing. This program provides life test performance results to fullfill reliability data requirements and to verify package integrity. The Reliability Add-On Program is supplemental to customer funded Lot Qualification.

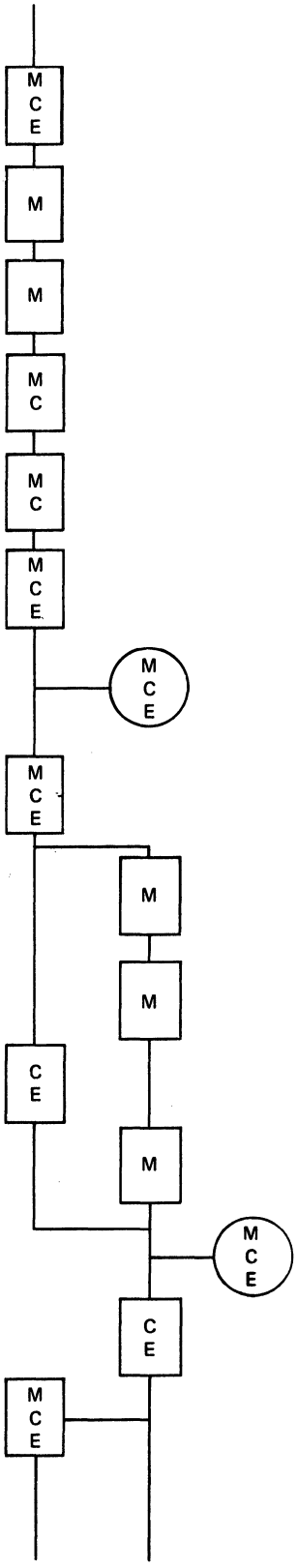
For customers desiring Lot Qualification, Harris Semiconductor will perform Group A, B, C and D inspections to MIL-STD-883, Method 5005 as defined herein for an additional charge.

Standard Products Screening and Inspection Procedure

OPER. SEQ.	OPER. DESCRIPTION	PRODUCT CATEGORIES		
		MIL (M)	COMM (C)	EPOXY (E)
	Incoming Material Silicon and Chemical Procurement.	X	X	X
	Q.C. Incoming Inspection. Materials are Inspected for Conformance to Specified Requirements.	X	X	X
	Manufacturing Wafer Fabrication	X	X	X
	QC • DIH_2O & Gas Monitor • SEM Process Control • Wafer Process Control	X	X	X
	Manufacturing, Wafer Electrical Probe (100%)	X	X	X
	Manufacturing, Wafer Scribe, Break (100%)	X	X	X
	Manufacturing Dice Screen (100%)	X	X	X
	QA Dice Inspection Control	X	X	X
	Preform Procurement	X	X	N/A
	Package Procurement	X	X	N/A
	Leadframe Procurement			X
	Epoxy Compound Procurement			X
	Q.C. Preform Inspection	X	X	N/A
	Q.C. Package Inspection	X	X	N/A
	Q.C. Leadframe Inspection			X
	Manufacturing Package Clean	X	X	N/A
	Manufacturing Die Mounting	X	X	X



QA Die Mount Control (continuous sampling) • Visual Die Inspection	X	X	X
Bond Wire Procurement	X	X	X
Q.C. Wire Inspection (receiving)	X	X	X
Manufacturing Wire Bonding	X Al	X Al	X Au
QA Bond Control (continuous sampling) • Visual Die & Bond Inspection • Wire and Pull Test	X	X	X
Manufacturing Pre-Seal Screen (100%)	MS883 Method 2010 Cond. A or B	MS883 Method 2010 HS Mod. Cond. B	MS883 Method 2010 HS Mod. Cond. B
QA Pre-Seal Inspection Lot Acceptance	MS883 Method 2010 Cond. A or B	MS883 Method 2010 HS Mod. Cond. B	MS883 Method 2010 HS Mod. Cond. B
Preseal Bake Per MS-883, Method 1008, Cond. C	8 hr.	4 hr.	4 hr.
Package Lid Procurement	X	X	N/A
Package Lid Inspection	X	X	N/A
Package Lid Clean	X	X	N/A
Package Seal/Encapsulation	X	X	X
QA Package Seal/Encapsulated Control (continuous sampling)	X	X	X



Stabilization Bake MS-883, Method 1008, Cond. C.	24 hr.	8 hr.	8 hr.
Temperature Cycle, MS-883, Method 1010, Cond. C,	X	N/A	N/A
Centrifuge, MS-883, Method 1010, (Y1) Plane 30 KG's min.	100%	N/A	N/A
Fine Leak, MS-883, Method 1014	100%	Sample	N/A
Gross Leak, MS-883, Method 1014 Omit Step 1, No Vacumm Pre-Cond. Step 3	100%	Sample	N/A
Frame Removal & Loading Units In Carriers/Sticks	X	X	X
Final QA Lot Inspection, MS-883 Method 1014 • Fine & Gross Leak • Visual/Mechanical Inspection	X	X	X
Group A Initial Tests Table I	X	X	X
Brand Device Type/Date Code Serialize, If Applicable	X	N/A	N/A
Burn-In (100%), MS-883, Method 1015	Classes A/B Products	N/A	N/A
Group A Final Test (100%)	X	N/A	N/A
QA Acceptance Elec. Testing • Visual/Mechanical Method 2009 Lot Sampling	X	X	X
Brand Devices Type/Date Code	N/A	X	X
Controlled Inventory	X	X	X

M C E	Package for Shipment	X	X	X
M C E	Quality Conformance Inspection Group B/C/D Testing, MS-883, Method 5005, Periodically or by Customer P.O. Request	X	X	X
M C E	QA Plant Clearance • Final Visual of Marking and Physical Quantity, Conformation of Product by Inspection or Sample Test	X	X	X
M C E	Ship to Customer	X	X	X

Harris Commercial Grade Products

This product is processed on the same wafer fabrication lines, to the same thorough specification and rigid controls as HI-Rel parts. At wafer electrical probe the product may be categorized for electrical performance, such as temperature range of operation or maximum output (see specific product data sheet for grading details) by utilizing multiple colored inks. Defective die are inked with red ink, but, for example, die meeting the commercial temperature range electrical specifications may be inked with green ink.

The die are then visually inspected and sorted after die separation to a modified Class B visual criteria. They are then assembled in packages on a controlled assembly line. The ink used to categorize product performance, such as the green ink, might not be removed from the commercial grade die. This ink has been chemically characterized as inert and reliability verification confirms there is no effect on performance or operating life of the parts.

Harris invites any interested customer to review our assembly flow and facilities for information, quality survey, or certification.

Table I - Group A Electrical Tests [1.]

SUBGROUP [2.]	DASH 8 & 2 LTPD * MIL-PRODUCT	LTPD* COMM. PRODUCT
Subgroup 1 Static Test at 25°C	5	7
Subgroup 2 Static Test at Maximum Rated Operating Temperature	7	N/A
Subgroup 3 Static Tests at Minimum Rated Operating Temperature	7	N/A
Subgroup 4 Dynamic Tests at 25°C	5	7
Subgroup 5 Functional Tests at 25°C	5	7
Subgroup 6 Functional Tests at Maximum and Minimum Rated Operating Temperatures	10	15
Subgroup 7 Switching Tests at 25°C	7	10

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable procurement document or specification sheet. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test to satisfy Group A requirements.
2. A single sample may be used for all subgroup testing. Where the required size exceeds the lot size, 100% inspection shall be allowed.

* Groups A, B, C and D sampling plans are based on standard LTPD tables of MIL-M-38510. Typically, the sample size chosen is based on 1 reject allowed. If necessary, the sample size will be increased once to the quantity not exceeding an acceptance number of 2.

Table II - Group B Tests (Lot Related)[1.]

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1			
Physical Dimensions	2016		2 Devices (No Failures)
Subgroup 2			
a. Resistance to Solvents	2015		3 Devices (No Failures)
b. Internal Visual and Mechanical	2014	Failure Criteria from Design and Construction Requirements of Applicable Procurement Document.	1 Device (No Failures)
c. Bond Strength[2.]			
(1) Thermocompression	2011	(1) Test Condition C or D	15
(2) Ultrasonic or Wedge		(2) Test Condition C or D	
(3) Beam Lead		(3) Test Condition H	
Subgroup 3			
Solderability[3.]	2003	Soldering Temperature of 260 ±10°C	15

NOTES:

1. Electrical reject devices from the same inspection lot may be used for all subgroups when end point measurements are not required.
2. Test samples for bond strength may, at the manufacturer's option unless otherwise specified be randomly selected immediately following internal visual (precap) inspection specified in method 5004, prior to sealing.
3. All devices submitted for solderability test must have been through the temperature/time exposure specified for burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.
4. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note — Table 1 *

Table III - Group C (Die-Related Tests)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1			
Operating Life Test	1005	Test Condition to be specified (1000 Hrs)	5
End Point Electrical Parameters		Table I — Subgroup 1	
Subgroup 2			
Temperature Cycling	1010	Test Condition C	15
Constant Acceleration	2001	Test Condition E Y_1 Axis	
Seal (a) Fine (b) Gross 2.	1014	As Applicable	
Visual Examination	1.		
End Point Electrical Parameters		Table I — Subgroup 1	

NOTES:

1. Visual examination shall be in accordance with method 1010.
2. When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.
3. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note - Table 1 *

Table IV - Group D (Package Related Tests)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2 [4.]			
Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6.]			
Subgroup 3 [1.]			
Thermal Shock	1011	Test Condition B as a Minimum, 15 Cycles Minimum.	15
Temperature Cycling	1010	Test Condition C, 10 Cycles Minimum	
Moisture Resistance	1004	Omit Initial/Conditioning and Vibration	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6.]			
Visual Examination	2.		
End Point Electrical Parameters		Table I – Subgroup 1	
Subgroup 4 [1.]			
Mechanical Shock	2002	Test Condition B	15
Vibration Variable Frequency	2007	Test Condition A	
Constant Acceleration	2001	Test Condition E (See 3)	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6.]			
Visual Examination	3.		
End Point Electrical Parameters		Table I – Subgroup 1	
Subgroup 5 [4.]			
Salt Atmosphere	1009	Test Condition A	15
Visual Examination	5.		

NOTES:

1. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".
2. Visual examination shall be in accordance with method 1010 or 1011 at a magnification of 5X to 10X.
3. Visual examination shall be performed in accordance with method 2007 for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damages shall constitute a failure.
4. Electrical reject devices from that same inspection lot may be used for samples.
5. Visual examination shall be in accordance with paragraph 3.3.1 for method 1009.
6. When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.
7. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note - Table 1 *

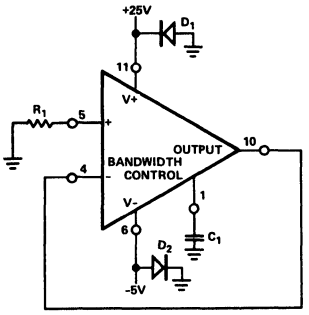
Burn-In Circuit Index

		DRAWING NO.
HA-909	Low Noise, Operational Amplifier	1, 2
HA-2050	High Slew Rate F.E.T. Input Operational Amplifier	2
HA-2050A	High Slew Rate F.E.T. Input Operational Amplifier	2
HA-2060	Wide Band F.E.T. Input Operational Amplifier	2
HA-2060A	Wide Band F.E.T. Input Operational Amplifier	2
HA-2400	PRAM Four Channel Operational Amplifiers	3
HA-2420	Sample and Hold, Gated Operational Amplifiers	4
HA-2500	High Slew Rate Operational Amplifier	2
HA-2502	High Slew Rate Operational Amplifier	2
HA-2510	High Slew Rate Operational Amplifier	2, 5
HA-2512	High Slew Rate Operational Amplifier	2, 5
HA-2520	High Slew Rate Operational Amplifier	2, 5
HA-2522	High Slew Rate Operational Amplifier	2, 5
HA-2530	Wide Band High Slew Inverting Amplifier	6
HA-2600	High Impedance Operational Amplifiers	2, 7
HA-2602	High Impedance Operational Amplifiers	2, 7
HA-2620	Wide Band, High Impedance Operational Amplifiers	7, 8
HA-2622	Wide Band, High Impedance Operational Amplifiers	7, 8
HA-2630	High Performance Current Booster	9
HA-2640	High Voltage Operational Amplifiers	2
HA-2650	Dual High Performance Operational Amplifiers	13
HA-2700	Low Power, High Performance Operational Amplifier	10, 11
HA-2720	Low Power, Current Programmable Operational Amplifiers	12
HA-2730	Low Power, Dual, Current Programmable Operational Amplifiers	13
HA-2820	Phase Locked Loop	14
HA-2900	Chopper Stabilized Operational Amplifiers	15
HA-4602	High Performance Quad Op Amp	16
HA-4741	Quad Op Amp	16
HA-4900	Quad Voltage Comparator	17
HC-55516/32	CVSD	18
HD-245	Triple-Line Transmitter	19
HD-246	Triple-Line Receiver	20
HI-200	Dual SPST Analog Switch	21, 22
HI-201	Quad SPST Analog Switch	23

HI-506	CMOS 16 Channel Analog Multiplexer	24
HI-506A	CMOS 16 Channel Analog Multiplexer	24
HI-507	Dual-8 Channel Multiplexer	24
HI-507A	Dual-8 Channel Multiplexer	24
HI-508A	8 Channel Analog Multiplexer	25
HI-509A	Dual-4 Channel Analog Multiplexer	26
HI-562	Precision 12-Bit D/A Converter	27
HI-1080	8-Bit D/A Converter	28
HI-1800A	DPDT-Low Leakage 4 Channel Analog Switch	29
HI-1818A	8 Channel Multiplexer	30
HI-1828A	Dual-4 Channel Analog Multiplexer	31
HI-1840	CMOS 16 Channel High Impedance Analog Multiplexer	24
HI-5040 thru 5051	CMOS Analog Switches	32

Burn-In Circuits

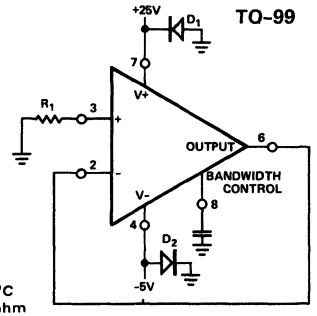
1 HA-909 TO-86 FLAT PACK



NOTES:
T_A = +125°C
R_1 = 1Megohm
C_1 = 0.01 µF, 100V

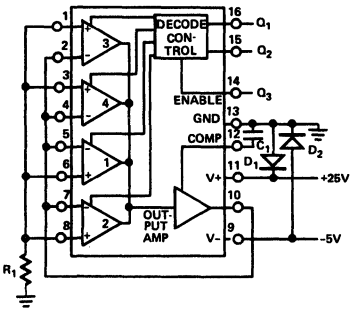
2 HA-909, HA-2500, HA-2502, HA-2510, HA-2512, HA-2520, HA-2522, HA-2600, HA-2602, HA-2620, HA-2622, HA-2050, HA-2050A, HA-2060, HA-2060A, HA-2640*

TO-99



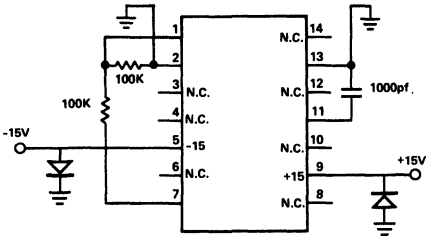
NOTES:
T_A = +125°C
R_1 = 1Megohm
C_1 = 0.01 µF, 100V
*V_{SUPPLY} = ±40V

3 HA-2400 16 LEAD CERDIP



NOTES:
T_A = +125°C
R_1 = 100KΩ
C_1 = 910pF, 50V
$D_{1,2}$ = IN4002
FREQ.: Q_1 = 100KHz; Q_2 = 50KHz; Q_3 = 25KHz

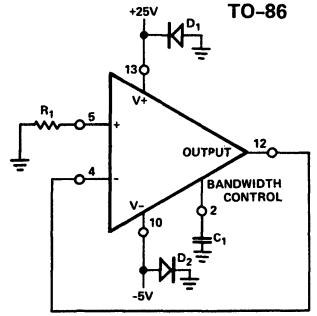
4 HA-2420 14 LEAD CERDIP



NOTE:
T_A = +125°C

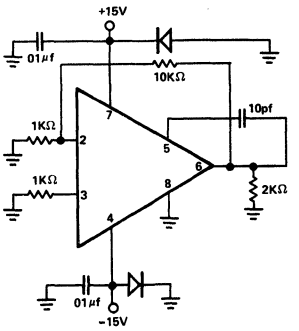
5 HA-2510, HA-2512, HA-2520, HA-2522

TO-86



NOTES:
T_A = +125°C
R_1 = 1Megohm
C_1 = 0.01 µF, 50V

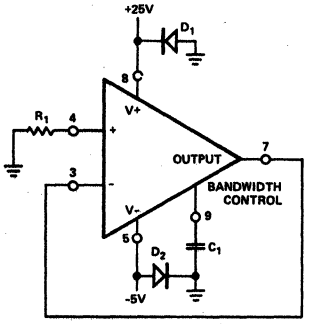
6 HA-2530 TO-99



NOTE: T_A = +125°C

7 HA-2600, HA-2602, HA-2620, HA-2622

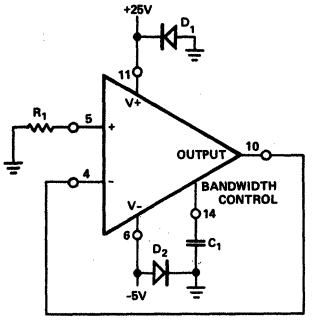
TO-91



NOTES:
T_A = +125°C
R_1 = 1Megohm
C_1 = 0.01 μF, 100V

8 HA-2620/2622

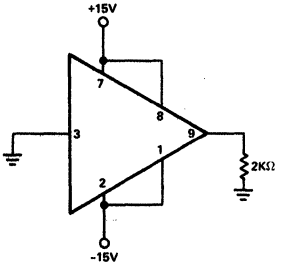
TO-116



NOTES:
T_A = +125°C
R_1 = 1 Megohm
C_1 = 0.01 μF, 100V

9 HA-2630

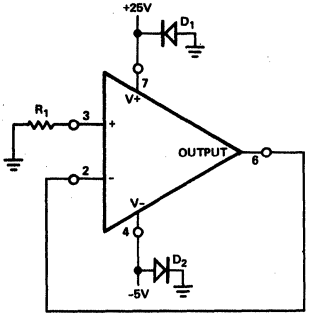
TO-8



NOTE:
T_A = +125°C

10 HA-2700

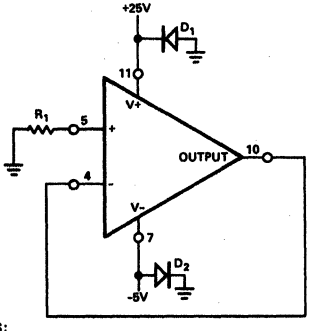
TO-99



NOTES:
TA = +125oC
R1 = 1 Megohm

11 HA-2700

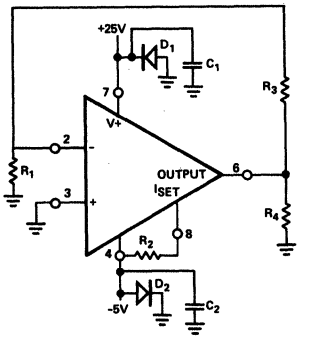
TO-116 D.I.P.



NOTES:
T_A = +125°C
R_1 = 1 Megohm

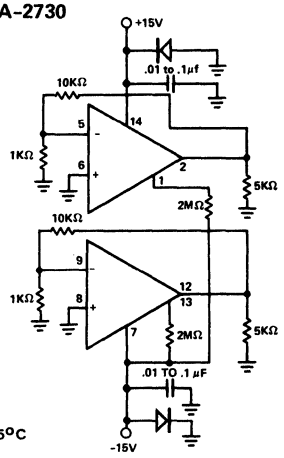
12 HA-2720

TO-99



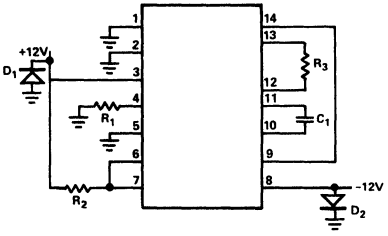
NOTES:
T_A = +125°
C_1C_2 = 0.01 to 0.1 μF
R_1 = 1KΩ
R_2 = 2MΩ
R_3 = 10KΩ
R_4 = 5KΩ

13 HA-2730 TO-116



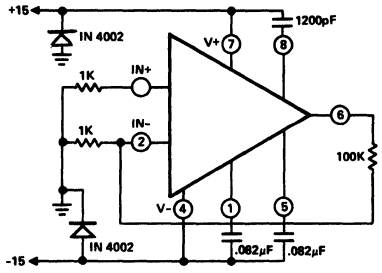
NOTE:
TA = +125°C

14 HA-2820 TO-116



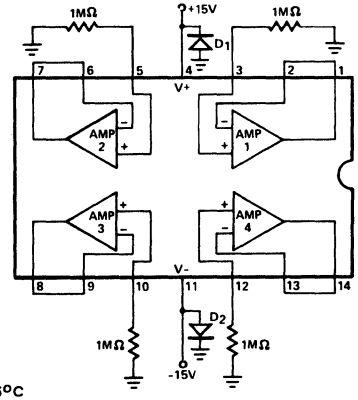
NOTES:
T_A = +125°C
R_1 = 10KΩ
R_2 = 4.7KΩ
R_3 = 560Ω
C_1 = 01 μF

15 HA-2900 TO-99



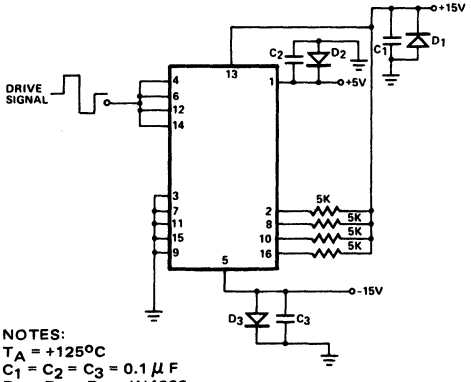
NOTE:
T_A = +125°C

16 HA-4602/4741 14 LEAD CERDIP



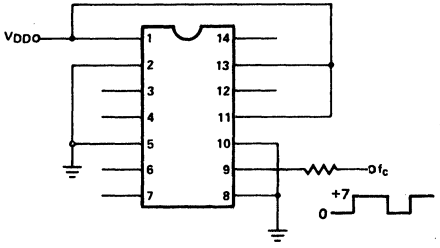
NOTES:
T_A = +125°C
D_1 = D_2 = IN4002

17 HA-4900 16 PIN CERDIP



NOTES:
T_A = +125°C
C_1 = C_2 = C_3 = 0.1 μF
D_1 = D_2 = D_3 = IN4002
DRIVE SIGNAL FREQ. = 2000Hz
DRIVE SIGNAL AMP. = ±.6VOLTS

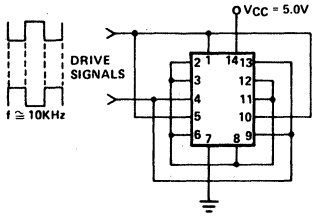
18 HC-55516/32 14 LEAD DIP/FLAT PACK



NOTES:
T_A = +125°C
V_{DD} = +7.0VOLTS
f_c = 16KHz

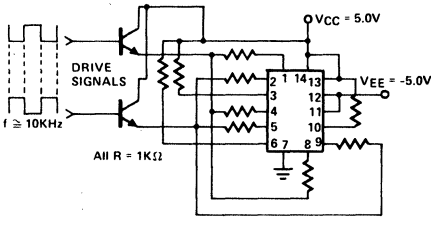
9

19 HD-245 14 PIN DIP/FLAT PACK



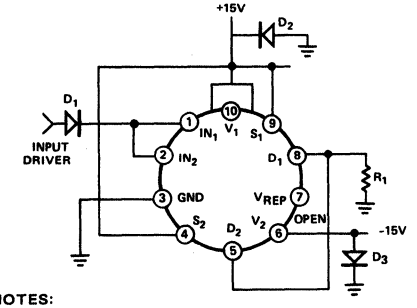
NOTE:
T_A = +125°C

20 HD-246 14 PIN DIP/FLAT PACK



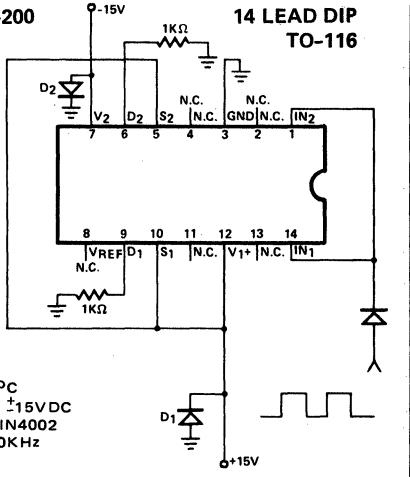
NOTE:
T_A = +125°C

21 HI-200 TO-100



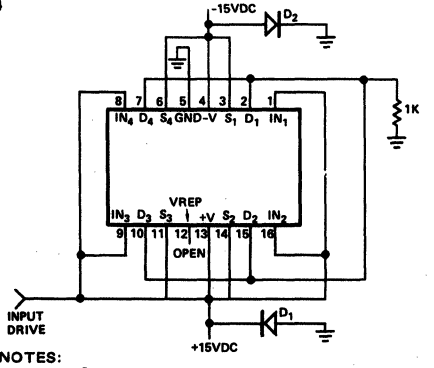
NOTES:
T_A = +125°C
R_1 = 10KΩ
$D_1D_2D_3$ = IN4002
FREQ.. = 100KHz

22 HI-200 14 LEAD DIP TO-116



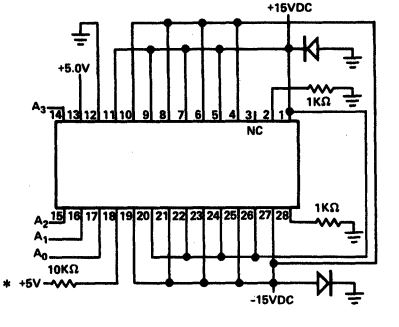
NOTES:
T_A = +125°C
SUPPLIES: ±15VDC
D_1 = D_2 = IN4002
FREQ. = 50KHz

23 HI-201 16 LEAD CERDIP



NOTES:
T_A = +125°C
D_1D_2 = IN4002
FREQ.: = 100KHz

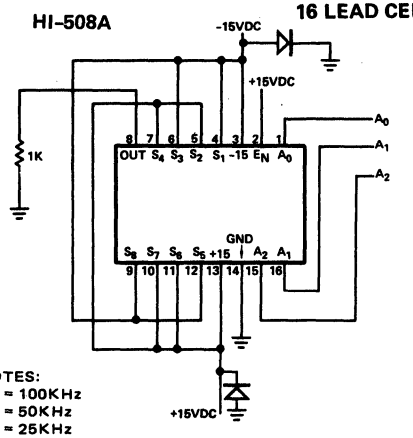
24 HI-506/507/506A/507A 28 LEAD CERDIP HI-1840



NOTES:
A_0 = 100KHz
A_1 = 50KHz
A_2 = 25KHz
A_3 = 12.5KHz

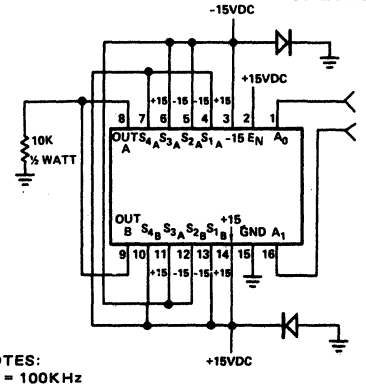
* Pin 18 grounded for HI-1840

25 HI-508A — 16 LEAD CERDIP



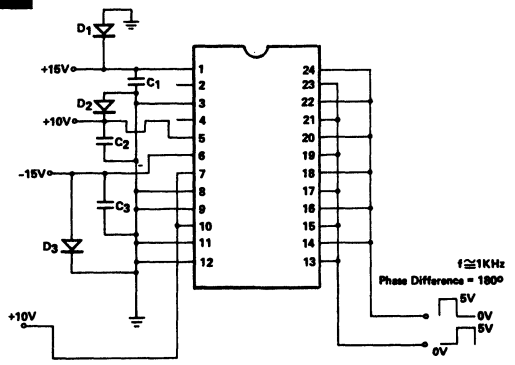
NOTES:
A_0 = 100KHz
A_1 = 50KHz
A_2 = 25KHz
TEMP: +125°C
PACKAGE: 16 PIN DIP

26 HI-509A — 16 LEAD CERDIP



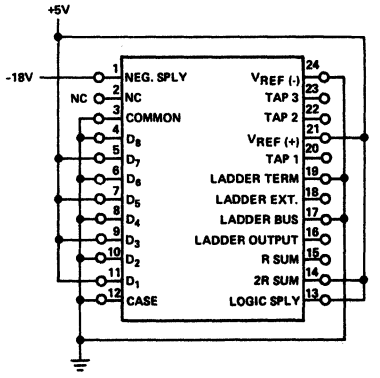
NOTES:
A_0 = 100KHz
A_1 = 50KHz
TEMP: +125°C
PACKAGE: 16 PIN DIP

27 HI-562 — 24 PIN DIP



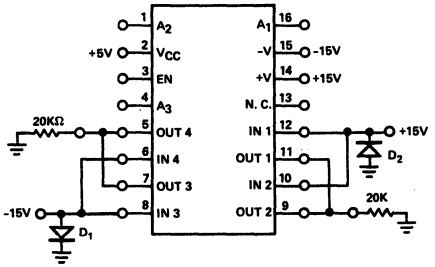
NOTES:
T_A = +125°C
D_1, D_2, D_3 = IN4002
C_1, C_2, C_3 = 0.01μF

28 HI-1080 — 24 LEAD CERDIP



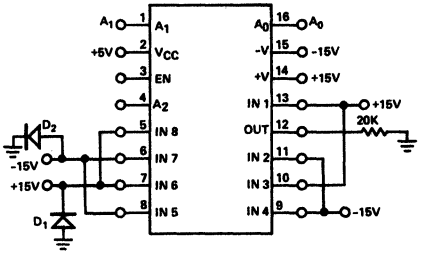
NOTE:
T_A = +125°C

29 HI-1800A — 16 LEAD CERDIP



NOTES:
T_A = +125°C
A_1 = 100KHz
A_2 = 50KHz
A_3 = 25KHz
EN = 12.5KHz

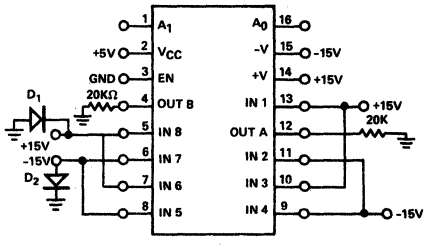
30 HI-1818A — 16 LEAD CERDIP



NOTES:
T_A = +125°C
A_0 = 100KHz
A_1 = 50KHz
A_2 = 25KHz
EN = 12.5KHz

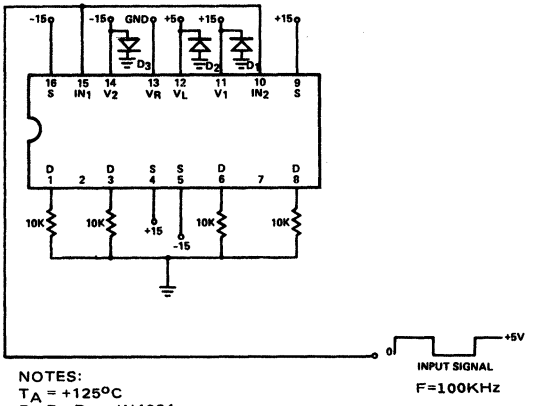
9

31 HI-1828A 16 LEAD CERDIP



NOTES:
T_A = +125°C
A_0 = 100KHz
A_1 = 50KHz
EN = 25KHz

32 HI-5040 thru HI-5051 16 LEAD CERDIP



NOTES:
T_A = +125°C
D_1, D_2, D_3 = IN4004

9

Packaging

Harris Package Selection Guide

PART NUMBER	PACKAGE CODE (See Note)		
	CAN	FLATPACK	D.I.P.
HA-909/911	2A	9V	
HA-2050/2055/2050A/2055A	2A		
HA-2060/2065/2060A/2065A	2A		
HA-2400/2404/2405			4B
HA-2420/2425			4U
HA-2500/2502/2505	2A		
HA-2510/2512/2515	2A	9V*	
HA-2520/2522/2525	2A	9V*	
HA-2530/2535	2A		
HA-2600/2602/2605	2A	9W*	
HA-2620/2622/2625	2A		4U
HA-2630/2635	2G		
HA-2640/2645	2A		
HA-2650/2655	2A		4U
HA-2700/2704/2705	2A		4U
HA-2720/2725	2A		
HA-2730/2735			4U
HA-2820/2825			4U
HA-2900/2904/2905	2E		
HA-4602/4605			4U
HA-4741			4U, 3B†
HA-4900/4905			4B
HC-55516/55532		9R	4Q
HD-0165			4K
HD-245/545		9V	1S
HD-246/546/249/549		9V	1S
HD-248/548		9V	1S
HI-200	2D		
HI-201			4B
HI-506/507/506A/507A			1M
HI-508A/509A			4B
HI-562			1H
HI-1080/1085			4K
HI-1800A			4B
HI-1818A/1828A			4B
HI-1840			1M
HI-5040 thru HI-5051			4B

NOTE: "Package Code" references drawings on the following pages. Note that these do not correspond with the general package designations to be used in constructing the part number, which is explained in Ordering Information at the front of this book.

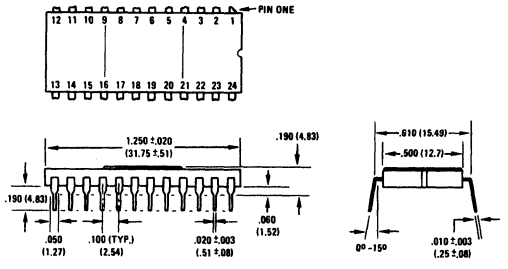
* Flatpack not available for commercial temperature range.

† 3B (Plastic D.I.P.) not available for military temperature range.

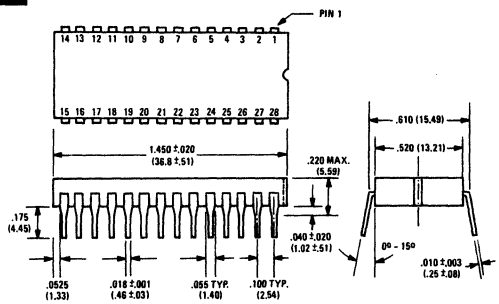
Package Dimensions

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.
3. Package codes are shown in black squares.

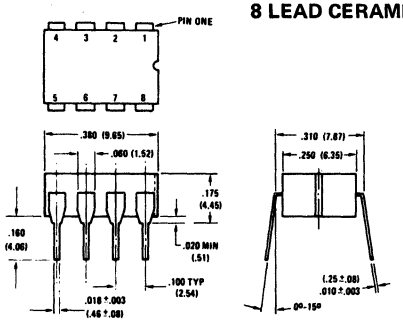
1H 24 LEAD D.I.P.



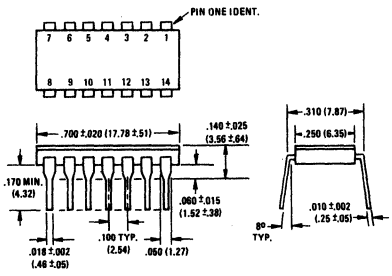
1M 28 LEAD CERAMIC D.I.P.



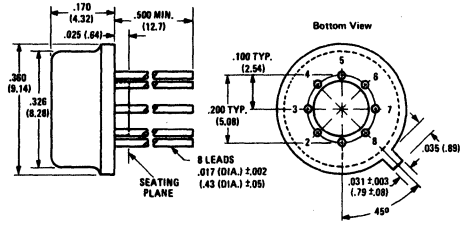
1N 8 LEAD CERAMIC D.I.P.



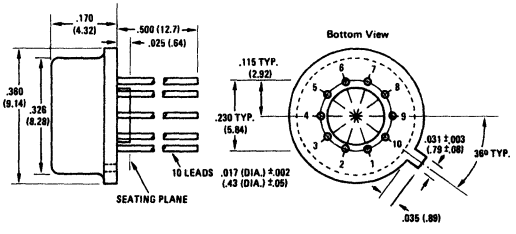
1S 14 LEAD BRAZED D.I.P.



2A TO-99 [.200 PC] (5.08 PC)

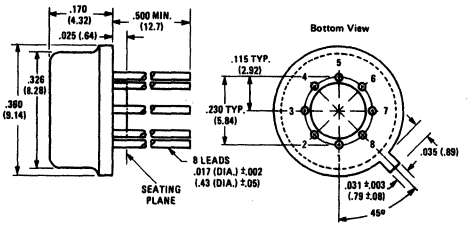


2D TO-100 (10 LEAD)

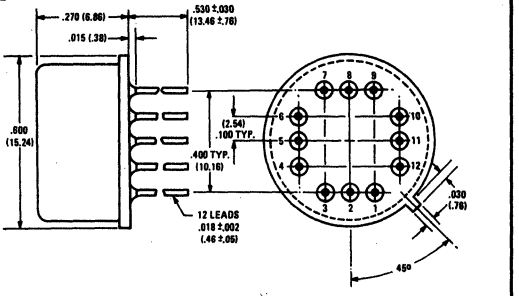


1

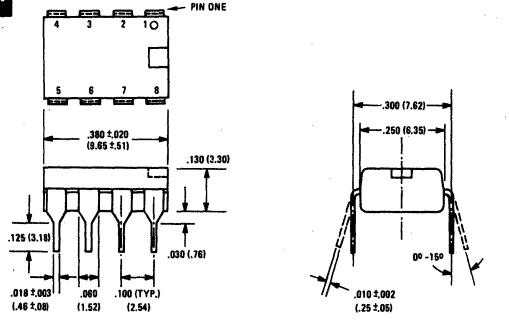
2E TO-99 [.230 PC] (5.84 PC)



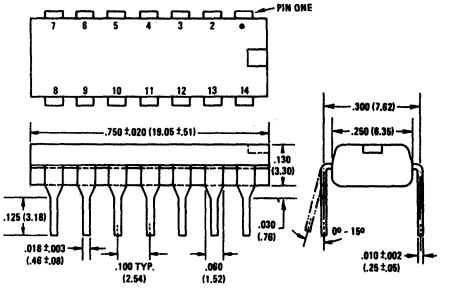
2G TO-8 (12 LEAD)



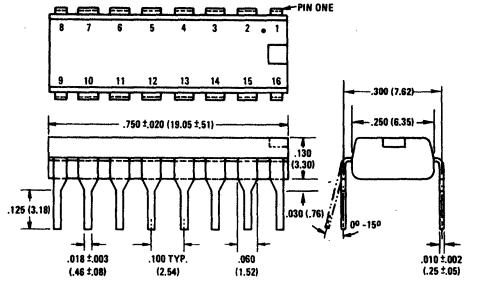
3A 8 LEAD D.I.P. EPOXY



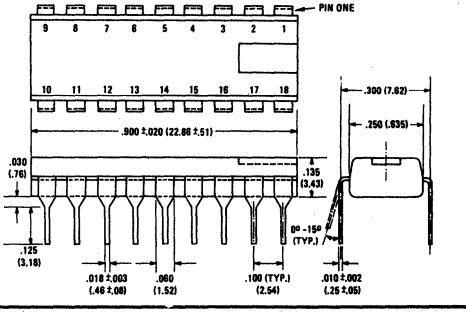
3B 14 LEAD D.I.P. EPOXY



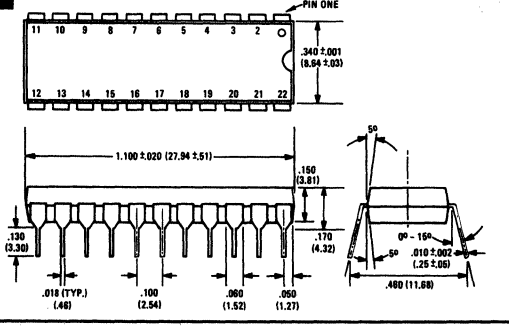
3C 16 LEAD D.I.P. EPOXY



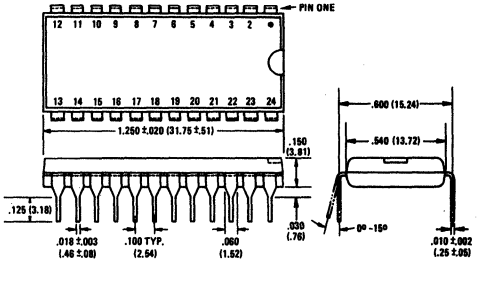
3D 18 LEAD D.I.P. EPOXY



3E 22 LEAD D.I.P. EPOXY

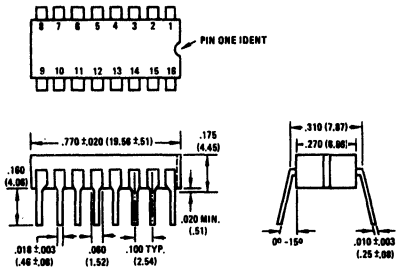


3F 24 LEAD D.I.P. EPOXY

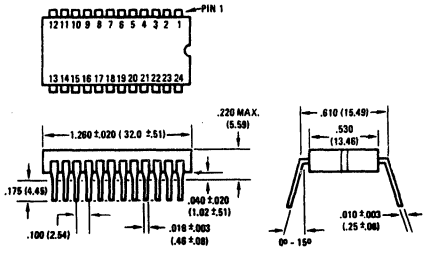


O

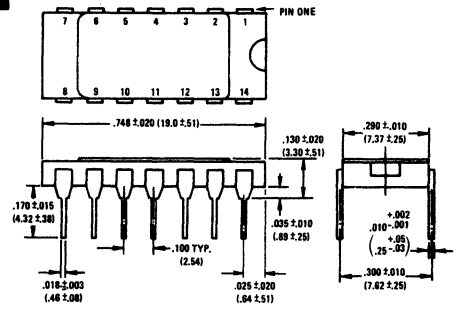
4B 16 LEAD CERAMIC D.I.P.



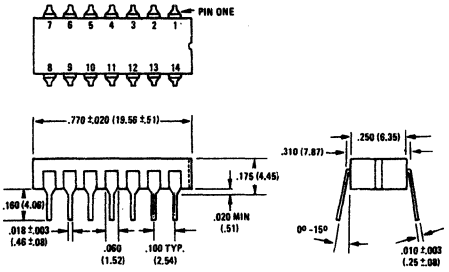
4K 24 LEAD CERAMIC D.I.P.



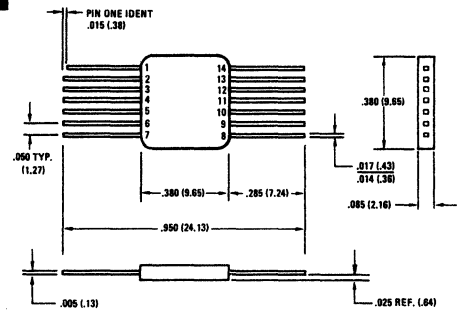
4Q 14 LEAD D.I.P. SIDE BRAZE



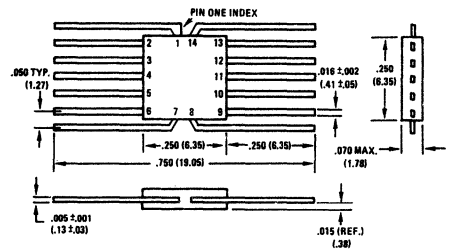
4U 14 LEAD CERAMIC D.I.P.



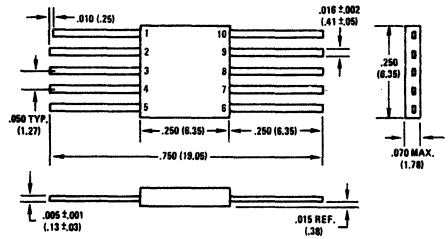
9R 14 LEAD METAL GLASS FLATPACK



9V TO-86 METAL BOTTOM



9W TO-91



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Harris Sales Locations

OEM Sales Offices

EASTERN REGION

535 Broadhollow Road
Melville, L.I., N.Y. 11746
(516) 249-4500

Suite 301
177 Worchester Street
Wellesley Hills, Mass. 02181
(617) 237-5430

Suite 325
650 E. Swedeford Road
Wayne, Penn. 19087
(215) 687-6680

Suite 115
2020 West McNab Road
Ft. Lauderdale, Fl. 33309
(305) 971-3200

CENTRAL REGION

Suite 100
4972 Northcutt Place
Dayton, Ohio 45414
(513) 226-0636

Suite 100
15 Spinning Wheel Road
Hinsdale, Ill. 60521
(312) 325-4242

Suite 132
7710 Computer Avenue
Minneapolis, Minn. 55435
(612) 835-2505

Suite 7G
777 S. Central Expressway
Richardson, Texas 75080
(214) 231-9031

WESTERN REGION

Suite 103
4014 Long Beach Blvd.
Long Beach, Calif. 90807
(213) 426-7687

Suite 230
1032 Elwell Court
Palo Alto, Calif. 94303
(415) 964-6443

HOME OFFICE

P.O. Box 883
Melbourne, Fl. 32901
(305) 724-7000
TWX-510-959-6259

International Sales Offices

Europe

OEM SALES

HARRIS SYSTEMS LTD.
Harris Semiconductor Div.
P.O. Box 27, 145 Farnham Rd.
Slough SL1 4XD, England
Tel: (Slough) 34666
TWX 848174 Harris G

HARRIS SEMICONDUCTOR, INC.
53 Bd. de Waterloo Bte 5
B-1000 Brussels, Belguim
Tel: 511 08 24
TX 26382

North Europe

DENMARK

DITZ SCHWEITZER A.S.
Vallensbaekvej 41
DK-2600 Glostrup, Denmark
Tel: (02) 453044
TX 33257

FINLAND

FINN METRIC OY
Ahertajantie 6D
SF-02101 Tapiola PI 6, Finland
Tel: 460844
TX 122018

NETHERLANDS

TECHMATION ELECTRONICS N.V.
Gebouw 106, Schiphol-Oost
1117-AA Amsterdam, Netherlands
Tel: (20) 456955
TX 13427

NORWAY

EGA A/S
Hjalamar Brantingsvei 6
N-Oslo 5, Norway
Tel: (02) 221900
TX 11265A EGA N

SWEDEN

A B ELECTROFLEX
Box 7068
S-17207 Sundbyberg, Sweden
Tel: (08) 289290
TX 17644

UNITED KINGDOM & IRELAND

CRELLON ELECTRONICS LTD.
380 Bath Road,
Slough, Bucks SLI 3UZ
England
Tel: Burnham (06286) 4434
TX 847571

MEMEC LTD
The Firs, Whitchurch
Nr. Aylesbury, Bucks,
England
Tel: (029664) 366
TX 837508

APEX COMPONENTS LTD.
396 Bath Road
Slough, Berks., England
Tel: (06286) 63741
TX 848519

Central Europe

AUSTRIA

KONTRON GMBH
Ameisgasse 49
A-1140 Vienna, Austria
Tel: 945646
TX 11699

BELGIUM

BETEA S.A.
15 Av. Geo Bernier
B-1050 Brussels, Belgium
Tel: (02) 649 99 00
TX 23188

Central Europe (continued)

GERMANY

KONTRON ELEKTRONIK GMBH
Oskar Von Miller Str. 1
D-8057 Eching Bei Munchen,
Germany
Tel: (08165) 771
TX 0526512

SWITZERLAND

STOLZ A.G.
Bellikonerstr. 218
CH-8968 Mutchellen, Switzerland
Tel: (057) 54655
TX 54070

South Europe

FRANCE

ALMEX (DISTRB.)
48, Rue de L'Aubepine
F-92160 Antony
France
Tel: 666-21-12
TX 250067

SPETELEC
Tour Europa
Belle Epine
Cidex A111
F-94532 Rungis
Tel: 686 5665
TX 25.801

IRAN

BERKEH COMPANY, LTD.
20 Salm Road
Roosevelt Avenue
Tehran, Iran
Tel: 828294
TX 212956

ITALY

ERIE ELETTRONICA SPA
Via Melchiorre Gioia 66
I-20125 Milano, Italy
Tel: (2)6884833/4/5
TX 36385

SPAIN & PORTUGAL

INSTRUMENTOS ELECTRONICOS
DE PRECISION
Alcalde Sainz de Baranda 33
Madrid 9, Spain
Tel: 2741007
TX 22961

Far East

OEM SALES

HARRIS SEMICONDUCTOR, INC.
2-3-6 Otemachi
Chiyodaku, Tokyo, Japan
Tel: (03) 279-1691
TX J 26525

AUSTRALIA

CEMA (DISTRB.) PTY. LTD.
21 Chandos Street
Crows Nest, N.S.W. 2065
Australia
Tel: 439-4655
TX A22846

JAPAN

HAKUTO COMPANY, LTD.
Foreign Division
C.P.O. Box 25
Tokyo, 100-91, Japan
Tel: (03) 503-3711
TX J 22912

KANEMATSU/HAMILTON GROUP
Kanematsu Gosho Ltd.
Electronics Dept. 2
2-5, Takara-Cho2
Chuo-Ku, Tokyo 104, Japan
TX 22333

MITSUBISHI CORPORATION
6-3, Marunouchi 2-Chome
Chiyoda-Ku
Tokyo, 100-91, Japan
Tel: (03) 210-3023
TX J 22222

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION