HARRIS

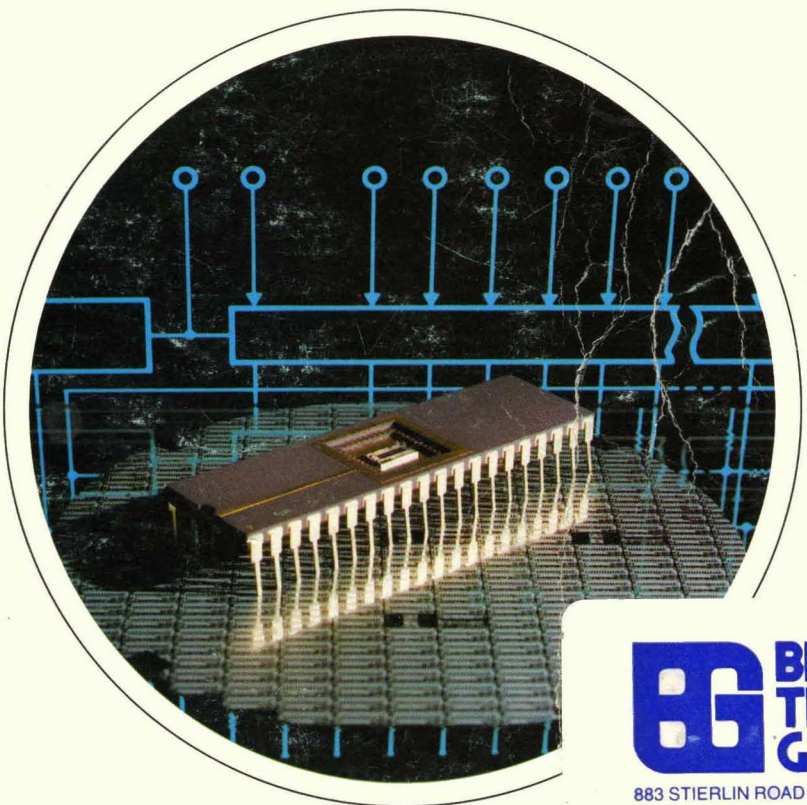
Volume 3

ANALOG

Linear·DataAcquisition·Communications·Linear·DataAcquisitio

Communications·Linear·DataAcquisition·Communications·Linea

Analog Data Book



HARRIS

Volume 3
$4.95

Harris Linear & Data Acquisition Products

Harris Semiconductor Analog Products represent the state of the art in precision and high speed performance. Capitalizing on the advanced linear processing technologies developed over the past 15 years, Harris Semiconductor Analog Products offer high quality and unmatched performance.

This data book describes Harris Semiconductor's complete line of Linear and Data Acquisition products, and includes a complete set of product specifications and data sheets, application notes and a separate section describing our quality and high reliability program.

All specifications in this data book are applicable only to packaged products. Specifications for dice are obtainable in Harris Semiconductor's Chip Data Book.

Please fill out the registration card at the back of this data book and return it to us so we may keep you informed of our latest new product developments over the next year.

If you need more information on these and other Harris products, please contact the nearest Harris sales office listed in the back of this data book.

Harris Semiconductor's products are sold by description only. Harris reserves the right to make changes in circuit design,specifications and other information at any time without prior notice. Accordingly, the reader is cautioned to verify that data sheets and other information in this publication are current before placing orders. Information contained in application notes is intended solely for general guidance; use of the information for user's specific application is at user's risk. Reference to products of other manufacturers are solely for convenience of comparison and do not imply total equivalency of design, performance, or otherwise.

Printed in USA

Contents

Alpha-Numeric Product Index

Advance

Ordering Information

Harris proprietary Analog products are designated by "Harris Product Code". These products will always begin with the letter H and specific device numbers are isolated by hyphens. "Industry standards" are identified by their standardized part numbers and product. Examples of both product codes are shown below. When ordering, please refer to products by the full code identification.

HARRIS PRODUCT CODE EXAMPLE

H A 7 - 5135 - 5

PREFIX:
H (Harris)

FAMILY:
A – Analog
C – Communications
D – Digital
I – Interface
M – Memory
V – Analog, High Voltage

PACKAGE:
1– Dual-In-Line
2– TO-5 Type
3– Epoxy Package
5– LCC Hybrid
4– Leadless Carriers
7– Mini DIP
0– Chip Form

PART NUMBER

TEMPERATURE:
1 0°C to +200°C*
2 -55°C to +125°C
2A -55°C to +125°C (Temperature Range Only – Does not Imply 883B Processing)
3 -200°C to +300°C*
4 -25°C to +85°C
5 0°C to +75°C
6 100% 25°C Probe (Dice Only)
7 Dash-7 High Reliability Commercial Product. 0°C to +75°C.
8 Dash-8 Program MIL-STD-883 Class B HA2-2700-8 (Example Only)
9 -40°C to +85°C

* Special high temperature testing available on certain product types. Consult factory for availability.

INDUSTRY STANDARDS PRODUCT CODE EXAMPLE

LM 301A H

- H – PACKAGE
- 301A – DEVICE NUMBER
- LM – DEVICE FAMILY

PACKAGE
D – Side-brazed Ceramic
H – TO-5 (TO-99, TO-100, TO-8)
J – Mini Cerdip (8-pin)
N – Plastic Dual-In-Line Package

DEVICE NUMBER*
3, 4, or 5 Digit Number Suffix Indicators:
A – Improved Electrical Specification
C – Commercial Temperature Range

DEVICE FAMILY
LF – Linear FET
LM – Linear Monolithic

* The first digit in the device number signifies the operating temperature range. A "1" denotes a Military temperature range device (-55°C to +125°C), A "3" denotes a Commercial temperature range device (0°C to +70°C).

HARRIS DASH 8 PROGRAM

As a service to users of High Rel products Harris makes readily available via the high reliability DASH 8 program many products from our product lines. Parts screened to MIL-STD-883 Method 5004 Class B are simply branded with the post-script "-8" to the appropriate Harris part numbers, in effect, offering "off the shelf" delivery. For details concerning this special Harris program for High Rel users, see Section 10 of this Data Book.

HARRIS DASH 7 PROGRAM

The Harris DASH 7 program extends the normal processing to include an added burn-in step for enhanced reliability. Details on DASH 7 are included in Section 10 of this Data Book.

HARRIS ANALOG JAN PROGRAM

In March 1980, Harris received JAN certification for the Analog Wafer Fabrication and Assembly facilities. All Harris Analog JAN products are produced on the certified line in strict compliance with all MIL-M-38510 program requirements.

Many Harris Analog high performance ICs are now available for immediate delivery in JAN Class B form. Consult your local Harris representative for an up-to-date list of all Harris JAN-qualified devices.

JAN from Harris offers the IC user high reliability, quality, and performance at a lower price and with faster delivery than similar products fabricated in accordance with non-standard source control drawings.

SPECIAL ORDERS

For best availability and price, it is urged that standard "Product Code" devices be specified, which are available worldwide from authorized distributors. Where enhanced reliability is needed, note standard "Dash 8" screening described in this Data Book. Harris application engineers may be consulted for advice about suitability of a part for a given application.

If additional electrical parameter guarantees or reliability screening are absolutely required, a Request for Quotation and Source Control Drawing should be submitted through the local Harris Sales Office or Sales Representative. Since many electrical parameters may be economically assured through design analysis, characterization, or correlation with other parameters, additionally desired parameters should be labeled, "Vendor will guarantee, but not necessarily test".

Harris reserves the right to decline to quote, or to request modification to special screening requirements.

I. C. Handling Procedures

Harris Analog I.C. processes produce circuits more rugged than similar ones. However, no semiconductor is immune from damage resulting from the sudden application of many thousands of volts of static electricity. While the phenomenon of catastrophic failure of devices containing MOS transistors or capacitors is well known, even bipolar circuits can be damaged by static discharge, with altered electrical properties and diminished reliability. None of the common I.C. internal protection networks operate quickly enough to positively prevent damage.

It is suggested that all semiconductors be handled, tested, and installed using standard "MOS handling techniques" of proper grounding of personnel and equipment. Parts and subassemblies should not be in contact with untreated plastic bags or wrapping material. High impedance I.C. inputs wired to a P.C. connector should have a path to ground on the card.

HANDLING RULES

Since the introduction of integrated circuits with MOS structures and high quality junctions, a safe and effective means of handling these devices has been of primary importance. One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existance in the industry. In addition most compensation networks in linear circuits are located at high impedance nodes, where protection networks would disturb normal circuit operation. If static discharge occurs at sufficient magnitude (2kV or more), some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10KV in a low humidity environment; thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. It is evident, therefore, that proper handling procedures or rules should be adopted.

Elimination or reduction of static charge can be accomplished as follows:

- Use conductive work stations. Conductive plastic* mats on work benches and floor, connected to ground through a 1-M ohm resistor, help eliminate static build-up and discharge. Do not use metallic surfaces.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1-M ohm to ground (the 1-M ohm resistor will prevent electroshock injury to personnel). Transient product personnel should wear grounding heel straps.
- Smocks, clothing, and especially shoes of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold, or aid, in the generation of a static change. Where they cannot be eliminated natural materials such as cotton etc. should be used to minimize charge generation capacity. Conductive smocks are also available as an alternative.
- Control relative humidity to as high a level as practical. 50% is generally considered sufficient (operations should cease if R. H. falls below 25%).
- Ionized airblowers reduce charge build-up in areas where grounding is not possible or practical.
- Devices should be in conductive carriers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam or foil.
- In automated handling equipment, the belts, chutes, or other surfaces should be of conducting non-metal material. If this is not possible, ionized air blowers or ionizing bars may be a good alternative.

*Supplier 3M Company
"Static Control Table Mat 8210/8210R"
"Static Control Floor Mat 8200/8200R"

Harris Analog I. C. Technologies

JUNCTION ISOLATION (J.I.)

This is the most common integrated circuit process. Bipolar I.C.'s generally begin with a p-type wafer into which a buried layer pattern, if used, is first diffused. Then the n-type epitaxial layer is grown, and p-type isolation walls are diffused around each area which is to be electrically isolated from the other circuitry. These isolation walls must be diffused deeply into the wafer in order to

contact the original p-substrate. In operation, the p-substrate and isolation walls are connected to the most negative circuit potential, so that each active area is surrounded on the sides and bottom by a reverse biased junction through which negligible current flows (Figure 1).

To complete the I.C., base and emitter diffusions are performed, the wafer is coated with aluminum and the conductor pattern is etched.

Representative Harris devices using this process are HA-4741, HA-5082, and HA-5084.

DIELECTRIC ISOLATION (D.I.)

A somewhat different process has been proven particularly advantageous for fabricating high performance analog I.C.'s. This is dielectric isolation (D.I.), where each active area is surrounded on the sides and bottom by an insulating layer of silicon dioxide, and for mechanical strength imbedded in polycrystalline silicon. This process for bipolar I.C.'s begins with a wafer of n-type silicon. The side of the wafer which will eventually be the bottom is deeply etched to form the sidewall pattern, then silicon dioxide and polycrystalline silicon are grown to fill the etched "moats". The opposite side of the wafer is then polished until the insulating sidewalls appear at the wafer surface (Figure 2). Conventional diffusion and metallization processes follow to complete the I.C. D.I. for analog I.C.'s has a number of advantages:

1. Almost all op amp designs require at least one PNP transistor in the signal path. Typical J.I. op amps must use a lateral PNP which inherently has very low frequency response, limiting typical compensated bandwidth to 1MHz. The D.I. process makes it practical to build a vertical PNP with much higher bandwidth making possible compensated op amp bandwidths of 12MHz or higher (Figure 3). Also, transistor collector to substrate capacitance is 2/3 less using D.I., further enhancing high frequency performance.
2. Other devices such as optimally specified MOS or JFET transistors may be fabricated on the same chip. Isolated diffused and thin film resistors are also practical.
3. The isolation removes the possibility of parasitic SCR's which might create latchup under certain sequences of power and signal application.
4. Leakage currents to the substrate under high temperature conditions are greatly reduced. While the circuits in this data book were not specifically designed for operating temperatures greater than +125°C, many have shown superior performance. For I.C.'s requiring the ultimate in radiation resistance, Harris Semiconductor Programs Division should be consulted.

DIELECTRIC ISOLATED CMOS

J.I. processed CMOS Analog I.C.'s, which are generally used in conjunction with several power supplies, are particularly prone to parasitic SCR latchup failures and failures due to input voltage spikes. The D.I. CMOS process, which is compared in detail in Harris Application Note 521, has proved to be the best solution.

Since analog multiplexers are often used at the input of a data acquisition system, particular attention must be paid to the possibility of damaging input overvoltage conditions. Harris has provided an effective answer in the HI-506A through HI-509A multiplexers with built-in overvoltage protection.

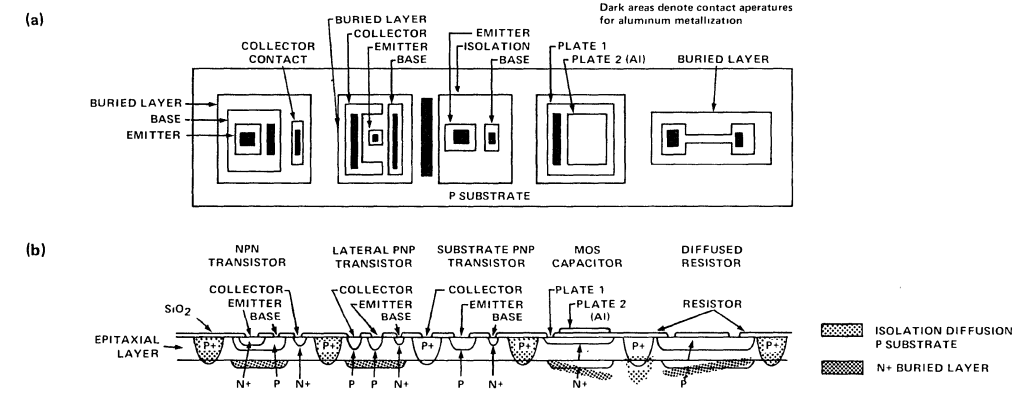


Figure 1 – Structures of various components formed in the junction-isolation process. (a) Topological view. (b) Cross-sectional view.

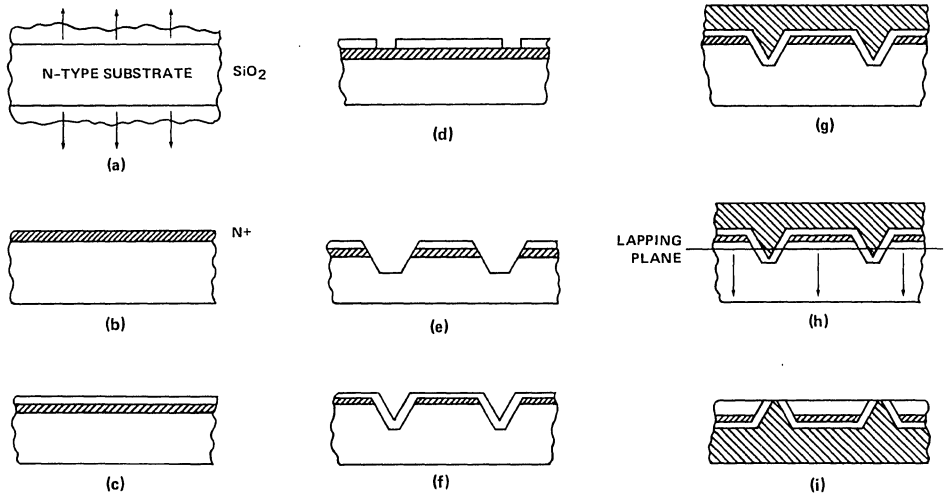


Figure 2- Process steps for dielectric isolation. (a) Surface preparation, (b) N-buried layer diffusion, (c) masking oxide, (d) isolation pattern, (e) silicon etch, (f) dielectric oxide, (g) polycrystalline deposition, (h) backlap and polish, (i) finished slice.

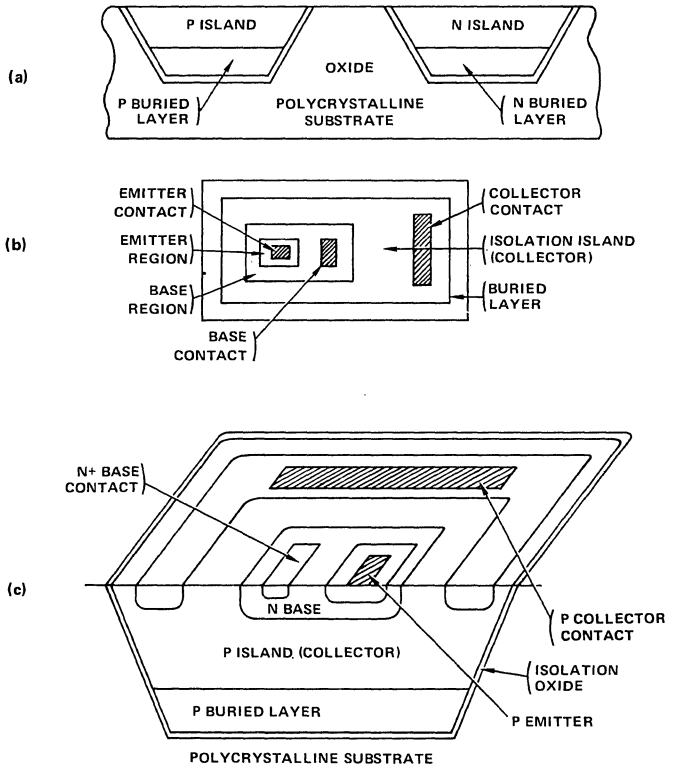


Figure 3—The high-frequency process. (a) Cross-sectional view of P and N islands for PNP and NPN transistors. (b) Topological view showing relative placement of transistor regions. (c) Cross-sectional view of high-frequency PNP device formation in the D. I. process.

MANU-FACTURER	PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	SUGGESTED FOR NEW DESIGN
AMD	AM118/318	LM118/318	LM118A/318A	LM118A/318A
	AM715			HA-2520/25
	AM1660			HA-2500/05
				HA-2600/05
	AM6012		HI-562A	HI-562A
ANALOG DEVICES	AD505		HA-2530/35	
	AD507JH*	HA2-2625-5		
	AD507SH	HA2-2620-2		
	AD509JH*	HA2-2525-5		
	AD509SH	HA2-2520-2		
	AD518	LM318	HA-2510/15	
	AD562		HI-562A	
	AD565A	HI-565A		
	AD566A		HI-5660	HI-5660
	AD574A	HI-574A		
	AD582		HA-2420/25	
	AD583KS	HA1-2425-3		
	AD7501			HI-1818A
	AD7502			HI-1828A
	AD7503			HI-1818A
	AD7506TD*	HI1-506-2		
	AD7507TD*	HI1-507-2		
	AD7510			HI-201
	AD7511			HI-201
	AD7512			HI-5043
	AD7513TH*	HI2-200-2		
	AD7541	HI-7541		
	ADDAC80	HI-5680		
BURR BROWN	3500/3510A			HA-2605
	3500/3510R			HA-2605
	3503J	HA2-2505-5		
	3506J	HA2-2605-5		
	3507J	HA2-2525-5		
	3508J	HA2-2625-5		
	3527AM		HA2-5170-5	
	3553AM			HA-2630/35
	MPC4D	HI1-509A-5		
	MPC8S	HI1-508A-5		
	MPC8D	HI1-507A-5		
	MPC16S	HI1-506A-5		
	DAC80	HI-5680		
DATEL	AM-450-2	HA2-2505-5		
	AM-452-2	HA2-2525-5		
	AM-460-2	HA2-2605-5		
	AM-462-1	HA1-2625-5		
	AM-462-2	HA2-2625-5		
	AM-464-2	HA2-2645-5		
	AM-490-2A	HA2-2905-5		
	MX-808	HI-508A-5		
	MX-1606	HI-506A-5		

*"K" equivalent is either military or selected commercial

COMPETITIVE CROSS-REFERENCE GUIDE TO LINEAR & DATA ACQUISITION PRODUCTS (continued)

MANU-FACTURER	PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	SUGGESTED FOR NEW DESIGN
DATEL (Continued)	MXD-409	HI-509A-5		
	MXD-807	HI-507A-5		
	SHM-1C-1	HA1-2425-5		
	DAC-681	HI-562A		
EXAR	XR4212		HA-4741	
FAIRCHILD	μA702			HA-2620/25
	μA709		HA-2620/2625	
	μA714		HA-5130	
	μA715			HA-2520/25
	μA727			HA-5130
	μA740			HA-5170
	μA741		HA-2620/2625	
	μA747			HA-2650/55
	μA748			HA-2620/25
	μA772		HA-2510/15	
	μA776		HA-2720/25	
	μA791			HA-2630/35
	SH3002			
	1558/1458		HA-2650/55	
INTERSIL	IH201	HI-201		
	IH200	HI-201		
	4250		HA-2720	
	4250C		HA-2725	
	IH5040MDE	HI1-5040-2		
	IH5040CDE	HI1-5040-5		
	IH5041MDE	HI1-5041-2		
	IH5041CDE	HI1-5041-5		
	IH5042MDE	HI1-5042-2		
	IH5042CDE	HI1-5042-5		
	IH5043MDE	HI1-5043-2		
	IH5043CDE	HI1-5043-5		
	IH5044MDE	HI1-5044-2		
	IH5044CDE	HI1-5044-5		
	IH5045MDE	HI1-5045-2		
	IH5045CDE	HI1-5045-5		
	IH5046MDE	HI1-5046-2		
	IH5046CDE	HI1-5046-5		
	IH5047MDE	HI1-5047-2		
	IH5047CDE	HI1-5047-5		
	IH5048MDE	HI1-5048-2		
	IH5048CDE	HI1-5048-5		
	IH5049MDE	HI1-5049-2		
	IH5049CDE	HI1-5049-5		
	IH5050MDE	HI1-5050-2		
	IH5050CDE	HI1-5050-5		
	IH5051MDE	HI1-5051-2		
	IH5051CDE	HI1-5051-5		
	8017			HA-2520/25
	8021M		HA-2720	
	8021C		HA-2725	
	8023	HA-8023		
	IH5110/5111			HA-2420/25
	AD7541	HI-7541		

COMPETITIVE CROSS-REFERENCE GUIDE TO LINEAR & DATA ACQUISITION PRODUCTS
(continued)

MANU-FACTURER	PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	SUGGESTED FOR NEW DESIGN
INTERSIL (Continued)	IH5060		HI-506A	
	IH5070		HI-507A	
	HA-2500/02/05	HA-2500/02/05		
	HA-2510/12/15	HA-2510/12/15		
	HA-2520/22/25	HA-2520/22/25		
	HA-2600/02/05	HA-2600/02/05		
	HA-2620/22/25	HA-2620/22/25		
INTRONICS	A-560	HA2-2525-5		
	A-561	HA2-2625-5		
	A-570	HA2-2535-5		
MOTOROLA	MC1520/1420			HA-2600/05
	MC1530/1531/ 1430/31			HA-2600/05
	MC1536/1436		HA-2640/45	
	MC1538/1438			HA-2620/2635
	MC1539/1439			HA-2620/25
	MC1545/1445			HA-2500/2505
	MC1554/1454			HA-2620/2635
	MC1556/1456			HA-2600/05
	MC1558/1458	LM1558/1458A	HA-2650/55	
	MC3301/3401			HA-4741
	MC3302			HA-4900
	MC3403/3505		HA-4741	
	MC3412	HI-565A		
	MX4741		HA-4741	HA-2700/05
NATIONAL	LF11508/13508		HI-508A	
	LF11509/13509		HI-509A	
	LF11201/12201/13201		HI-201	
	LF155A/156A/157A	LF155A/156A/157A	HA-5100-2	
	LF355A/356A/357A	LF355A/356A/357A	HA-5105-5	
	LF198/398			HA-2420/25
	LH0002			HA-2630
	LH0003			HA-2520
	LH0004			HA-2640
	LH0005			HA-2620
	LH0022/42/52	LF342		HA-5180
	LH0023/43			HA-2420/25
	LH0024			HA-2530/35
	LH0032		HA-2540	
	LH0033/63		HA-2540	HA-2630/35
	LH0052	HA-5180A		
	LH0062	HA-5162		
	LM102/302			HA-2600/05
	LM108/208/308	LM108/208/308		HA-2700/04/05
	LM108A/208A/308A	LM108A/208A/308A		HA-2700/04/05
	LM110/310			HA-2500/05

COMPETITIVE CROSS-REFERENCE GUIDE TO LINEAR & DATA ACQUISITION PRODUCTS
(continued)

MANU-FACTURER	PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	SUGGESTED FOR NEW DESIGN
NATIONAL (Continued)	LM112/212/312			HA-2700/04/05
	LM118/318	LM118/318	LM118A/318A	HA-2510/15
	LM124/324		HA-4741	
	LM139/339			HA-4900/05
	LM143/343	LM143/343		LM143A/343A
	LM144/344		HA-2640/45	
	LM148/248/348	LM148/248/348	HA-4741	LM148A/348A
	LM149/349			
	LM4250/4250C	LM4250/4250C		
	DAC1280	HI-5680		
PRECISION MONO.	MUX-08	HI-508/508A		
	MUX-09	HI-509/509A		
	OP-01			HA-2600/05
				HA-2500/05
	OP-07883AJ	HA2-5130-8		
	OP-07AJ	HA2-5130-2/OP-07AJ		
	OP-07883J	HA2-5135-8		
	OP-07J	HA2-5135-2/OP-07J		
	OP-07EP/CP/DP	HA3-5135-5		
	SMP 10/11	HA-2420/25		
	MUX-88	HI-508A		
	OP-15A		HA-5170-2	
	OP-15E		HA-5170-5	
	OP-15F		HA-5170-5	
	OP-17A		HA-5110-2	
	OP-17E		HA-5110-5	
	OP-17F		HA-5115-5	
	REF-01A		HA-1608-2	
	REF-01E		HA-1608-5	
	SSS1558/1458		HA-2650/55	
	DAC-12			HI-562A
	SSS562	HI1-562A-5		
RCA	CA3020			HA-2630/35
	CA3078		HA-5144	HA-2720
	CA3100			HA-2520/25
	CA6078			HA-2720
	CD4016			HI-201
RAYTHEON	RM/RC1556A			HA-2600/05
	RM/RC4131			HA-2600/05
	RM/RC4136			HA-4741
	RM4156	HA1-4156-2		
	RC4156	HA1-4156-5		
	HA1-4741-2	HA1-4741-2		LM348
	HA1-4741-5	HA1-4741-5		
	RM/RC4531			HA-2500/05
	RM/RC4558		HA-2650/55	

COMPETITIVE CROSS-REFERENCE GUIDE TO LINEAR & DATA ACQUISITION PRODUCTS (continued)

MANU-FACTURER	PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	SUGGESTED FOR NEW DESIGN
SIGNETICS	5537			HA-2420/25
	531			HA-2510/15
	5556			HA-2600/05
	5539	HA-2539		
	5558		HA-2650/55	
SILICON GENERAL	SG741S			HA-2500
	SG741SG			HA-2505
SILICONIX	DG181			HI-381, HI-5048
	DG182			HI-381, HI-5041
	DG184			HI-384, HI-5049
	DG185			HI-384, HI-5045
	DG187			HI-387, HI-5050
	DG188			HI-387, HI-5042
	DG190			HI-390, HI-5051
	DG191			HI-390, HI-5043
	DG200AA	HI2-0200-2		
	DG200BA	HI2-0200-4		
	DG200AP	HI1-0200-2		
	DG200BP	HI1-0200-4		
	DG200CJ	HI3-0200-5		
	DG201AP	HI1-0201-2		
	DG201BP	HI1-0201-4		
	DG201CJ	HI3-0201-5		HI3-0201HS-J
	DG211CK			HI3-0201-5
	DG300AA	HI2-0300-2		
	DG300BA	HI2-0300-4		
	DG300AP	HI1-0300-2		
	DG300BP	HI1-0300-4		
	DG300CJ	HI3-0300-5		
	DG301AA	HI2-0301-2		
	DG301BA	HI2-0301-4		
	DG301AP	HI1-0301-2		
	DG301BP	HI1-0301-4		
	DG301CJ	HI3-0301-5		
	DG302AP	HI1-0302-2		
	DG302BP	HI1-0302-4		
	DG302CJ	HI3-0302-5		
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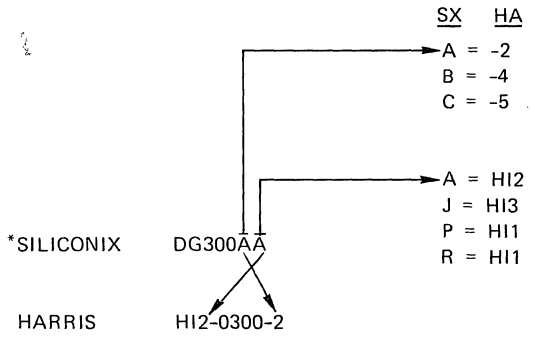
	DG303BP	HI1-0303-4		
	DG303CJ	HI3-0303-5		
	DG304AA	HI2-0304-2		
	DG304BA	HI2-0304-4		
	DG304AP	HI1-0304-2		
	DG304BP	HI1-0304-4		
	DG304CJ	HI3-0304-5		
	DG305AA	HI2-0305-2		
	DG305BA	HI2-0305-4		
	DG305AP	HI1-0305-2		
	DG305BP	HI1-0305-4		
	DG305CJ	HI3-0305-5		
	DG306AP	HI1-0306-2		
	DG306BP	HI1-0306-4		
	DG306CJ	HI3-0306-5		

COMPETITIVE CROSS-REFERENCE GUIDE TO LINEAR & DATA ACQUISITION PRODUCTS
(continued)

MANU-FACTURER	PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	SUGGESTED FOR NEW DESIGN
SILICONIX (Continued)	DG307AP	HI1-0307-2		
	DG307BP	HI1-0307-4		
	DG307CJ	HI3-0307-5		
	DG381AA	HI2-0381-2		
	DG381BA	HI2-0381-4		
	DG381AP	HI1-0381-2		
	DG381BP	HI1-0381-4		
	DG381CJ	HI3-0381-5		
	DG384AP	HI1-0384-2		
	DG384BP	HI1-0384-4		
	DG384CJ	HI3-0384-5		
	DG387AA	HI2-0387-2		
	DG387BA	HI2-0387-4		
	DG387AP	HI1-0387-2		
	DG387BP	HI1-0387-4		
	DG387CJ	HI3-0387-5		
	DG390AP	HI1-0390-2		
	DG390BP	HI1-0390-4		
	DG390CJ	HI3-0390-5		
	DG506AR	HI1-0506-2		HI1-0506A-2
	DG506BR	HI1-0506-4		HI1-0506A-4
	DG506CJ	HI3-0506-5		HI3-0506A-5
	DG507AR	HI1-0507-2		HI1-0507A-2
	DG507BR	HI1-0507-4		HI1-0507A-4
	DG507CJ	HI3-0507-5		HI3-0507A-5
	DG508AP	HI1-0508-2		HI1-0508A-2
	DG508BP	HI1-0508-4		HI1-0508A-4
	DG508CJ	HI3-0508-5		HI3-0508A-5
	DG509AP	HI1-0509-2		HI1-0509A-2
	DG509BP	HI1-0509-4		HI1-0509A-4
	DG509CJ	HI3-0509-5		HI3-0509A-5
	L140			HA-2720/25



COMPETITIVE CROSS-REFERENCE GUIDE TO LINEAR & DATA ACQUISITION PRODUCTS (continued)

MANU-FACTURER	PART NUMBER	HARRIS PIN-FOR-PIN REPLACEMENT	HARRIS CLOSEST REPLACEMENT	SUGGESTED FOR NEW DESIGN
SOLITRON	CM4016A			HI-201
	μc4000/4001C/ 4002C			HA-2605
	μc4250	LM4250	HA-2720	
	μc4250c	LM4250C	HA-2725	
SPRAGUE	ULS/ULN2139			HA-2600/05
	ULS/ULN2151			HA-2600/05
	ULS/ULN2156			HA-2600/05
	ULS/ULN2157			HA-2650/55
	ULS/ULN2158			HA-2650/55
	ULS/ULN2171			HA-2600/05
	ULS/ULN2172			HA-2620/25
	ULS/ULN2173			HA-2600/05
	ULS/ULN2174			HA-2620/25
	ULS/ULN2175			HA-2600/05
	ULS/ULN2176			HA-2600/05
TELEDYNE PHILBRICK	1321	HA2-2625-5		
	1321-01	HA2-2620-2		
	1322	HA2-2525-5		
	1322-01	HA2-2520-2		
	1332	HA2-2645-5		
	1339			HA-2625
	4551	HI1-507A-5		
	4552	HI1-506A-5		
	4856	HA1-2425-5		
	1430			HA-5195
TI	TL044			HA-4741
	TL062	HA-5062		
	TL064	HA-5064		
	TL082	HA-5082		
	TL084	HA-5084		
	MC1558/1458		HA-2650/55	
TRANSITRON	TOA7709			HA-2600
	TOA8709			HA-2605

High Temperature Electronics

To serve the growing need for electronics that will operate in severe high temperature environments, Harris will offer integrated circuits that have been characterized over elevated temperatures and that have electrical characteristics guaranteed at 200°C.

Typical applications include:

- Well Logging
- Industrial Process Control
- Engine Control and Testing
- High Temperature Data Acquisition Systems

It is the intention of Harris Semiconductor to make available in the high temperature series (identified by the -1 suffix following the device part number) all the basic elements required for the designer to build a data acquisition system that will function to specified limits at 200°C.

The devices to be offered:

- Operational Amplifiers
- Analog Switches
- Analog Multiplexers
- 12 Bit Digital to Analog Converter
- Sample & Hold Amplifiers
  A/D Converters

All parts offered in the -1 series have had their electrical performance parameters characterized up to 250°C.

Production flow of -1 parts includes screening to MIL-STD-883B, 160 hours burn-in and final electrical test at 200°C.

Devices available Now:

• HA-2420-1	Sample & Hold Amplifier
• HA-2600-1	Operational Amplifier
• HA-2620-1	Operational Amplifier
• HI-200-1	Analog Switch
• HI-201-1	Analog Switch

Consult factory for price and availability information.

Advanced Packaging Techniques

Harris Semiconductor is now offering Leadless Chip Carriers (LCC) as a packaging option on various Analog integrated circuits. An LCC is a square or rectangular package for an Integrated Circuit (IC) that is manufactured in the same manner as a conventional side-braze dual-in-line package (DIP). The LCC is essentially comprised of the cavity and seal ring section of a standard DIP. It offers the user a means of achieving high density system configurations while retaining the reliability benefits of hermetic IC packaging. Figure 1 provides a comparison of the construction of an LCC and a conventional side-braze DIP.

The LCC's two principle advantages over conventional side braze DIPs are packaging density and electrical performance. Packaging density is the number one advantage to an LCC over a side braze DIP. The size of a DIP is governed primarily by the number of leads required and not by the size of the IC. As pin count increases, more and more of the DIP package is used only to provide an electrical trace path to the external leads. The size of an LCC is dependant on the size of the die not on the number of leads. As pin count increases, overall size increases but at a much slower rate. Table 1 provides a comparison between the areas of 18, 28, and 48 lead LCCs to 18, 28, and 48 lead side braze DIPs. The chart indicates a 270% improvement in packaging area for the 18 lead LCC, and 542% improvement for the 48 lead LCC. Obviously, sizable savings in circuit board area can be achieved with this packaging option. The second major advantage of the LCC is in electrical performance. The package size and geometry also dictates trace length and uniformity. Figure 2 provides a comparison between the trace lengths for various LCCs and side braze DIPs. As pin

count goes up, trace lengths get longer, adding resistance and capacitance unequally around the package. As ICs get faster and more complex, these factors start to become a limiting factor on performance. LCCs minimize this effect by maintaining, as close as possible, uniform trace length so that the package is significantly smaller determinant of system performance.

The LCC also offers environmental advantages over "chip-and-wire" manufacturing techniques used in high density hybrid circuits. An IC can be fully tested, burned-in and processed to MIL-STD-883B in an LCC, thereby guaranteeing its performance. The IC is further protected by small hermetic package in which internal water vapor content can be carefully controlled during production.

In summary, Harris Semiconductor Leadless Chip Carriers use a proven technology to provide a reliable high density, high performance packaging option for today's systems.

A list of products available in LCC form is provided in the Packaging Section on page 11-6. Consult the factory or your Harris sales representative for pricing and availability.

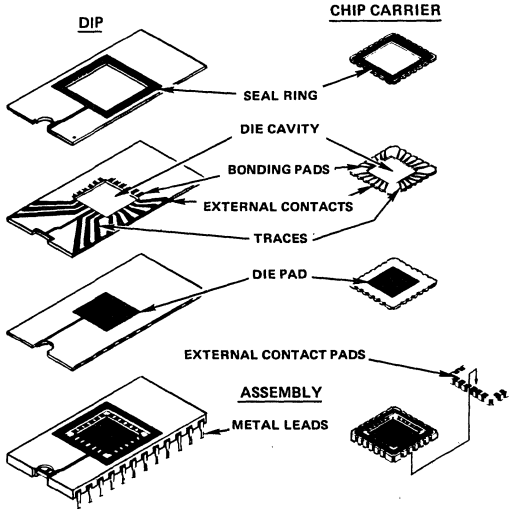
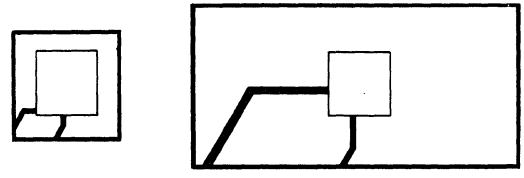


FIGURE 1. Exploded view of Chip Carrier and DIP.



LEAD COUNT	LONGEST TRACE DIP LONGEST TRACE CC	LONGEST TRACE SHORTEST TRACE	
		CC	DIP
18	2:1	1.5:1	6:1
24	4:1	1.5:1	3:1
40	5:1	1.5:1	6:1
54	6:1	1.5:1	7:1

FIGURE 2. Electrical Performance (Resistance and Speed)

TABLE I

	LCC	DIP	DIP AREA LCC AREA
18 Lead	0.10	0.22	270
28 Lead	0.20	0.84	420
48 Lead	0.31	1.68	542

(All units in square inches)

Operational Amplifiers and Comparators

As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in a permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

LINEAR PRODUCTS – PARAMETRIC CLASSIFICATION REFERENCE

	HARRIS	NATIONAL	T. I.	PMI	SIGNETICS	INTERSIL	MOTOROLA	RCA	ANALOG DEVICES	BURR BROWN	RAYTHEON	FAIRCHILD	
HIGH SLEW RATE	HA-2500 HA-2510 HA-2520 HA-2530 HA-2539 HA-2540 HA-5160 HA-5195 LM318	LH0032 LH0024C LH0062 LM318	LM318	OP-17 OP-37	SE5538 NE5539	HA2520			LH0032 AD509 AD518 AD528	3550K 3507 3551 3554	LM318	μA318	
WIDEBAND	HA-2539 HA-2540 HA-2600 HA-2620 HA-4625 HA-5115 HA-5160 HA-5190 LF347	LF357 LH0024 LH0032 LH0003 LH0005	TL702	OP-17 OP-37	NE5539	HA-2620	MC1712	CA3100	AD528 ADLH0032 AD507	3551 3554		μA702	
LOW NOISE	HA-4605 HA-5135 HA-5170 LM348/A	LM359		OP-07 OP-27 OP-37					ADOP-07 AD504 AD510 AD517	3510C			
PRECISION	OP07 HA-5135 HA-5170 HA-5180A LM308	LM11 LH0044 LM725 LM308		OP-07 OP-27 OP-25 SSS-725 OP-10					ADOP-07 AD504 AD510 AD517	3510C 3527	LM308A	μA714 μA725	
LOW POWER	HA-2725 HA-2740 HA-8023 LM346 LM4250 HA-5062 HA-5064 HA-5141 HA-5142 HA-5144	LM11 LM4250	TL061 TL062 TL064	OP-420 OP-421 OP-220 OP-20 OP-21		ICL4250 ICL8021 ICL8023 ICL76XX	MC1776 MC3476	CA3078 CA3094 CA3078A				μA776	

	HARRIS	NATIONAL	T.I.	PMI	SIGNETICS	INTERSIL	MOTOROLA	RCA	ANALOG DEVICES	BURR BROWN	RAYTHEON	FAIRCHILD	
PROGRAMMABLE	HA-2725 HA-2740 HA-8023 LM346 LM4250 LM4250C	LM4250 LM4250C LH24250C LM346	TL066			ICL4250C ICL8022C ICL8021C ICL7611C ICL7612C	MC1776C MC3476 MC3575 TCA3003	CA3078 CA3080 CA3094 CA3060			LM346	μA776 μA776C	
HIGH INPUT IMPEDANCE	HA-5062 HA-5064 HA-5082 HA-5084 HA-5100 HA-5160 HA-5170 HA-5180 LF342 LF347 LF353 LF355 LF356 LF357	LF347 LF351 LF353 LF355 LF356 LF357 LH0052 LH0042 LH0022 LF13741	TL081 TL062 TL064 TL082 TL084	PM355 PM356 PM357 OP-17 OP-16		LF355 LF356 LF357	LF355 LF356 LF357	CA3140 CA3160	AD515 AD545	3522 3523 3527 3528		μAF355 μAF356 μAF357	
HIGH VOLTAGE	HA-2645 LM343 LM343A	LH0004 LM143 LM144 LM1536				ICH8510M ICH8520M ICH8530M	MC1436			3581J 3571A 3572A 3580J			
HIGH POWER	HA-2635	LH0061 LH0041 LH0005 LH0003				ICH8510M		CA3094		3571A 3554A/B 3580J 3583 3581		μA759 μA759C	
GENERAL PURPOSE	HA-4741 HA-4156 LM348 HA-2655	LM348				ICL7632C ICL8023					RC 4156		

Operational Amplifiers Glossary

AVERAGE INPUT OFFSET CURRENT DRIFT ($\Delta I_{OS}/\Delta T$) - The ratio of the change in the offset current to the change in temperature producing it.

AVERAGE OFFSET VOLTAGE DRIFT ($\Delta V_{OS}/\Delta T$) - The ratio of the change in the offset voltage to the change in temperature producing it.

BANDWIDTH (BW) - That frequency at which the gain of the amplifier is 3dB below its low frequency value.

CHANNEL SEPARATION - The ratio of the input of a driven amplifier to the output of an adjacent undriven amplifier.

COMMON MODE INPUT VOLTAGE (V_{IC}) - The average of the two input voltages.

COMMON MODE INPUT VOLTAGE RANGE (V_{ICR}) - The range of voltage that if exceeded at either input terminal will cause the amplifer to cease operating properly.

COMMON MODE REJECTION RATIO (C_{MRR}) - The ratio of the differential voltage gain to the common mode voltage gain.

Note: This is measured by determining the ratio of the change in input common-mode voltage to the resulting change in offset voltage.

COMMON MODE RESISTANCE (r_{ic}) - The value of resistance looking into both inputs tied together.

DIFFERENTIAL INPUT RESISTANCE (r_{id}) - The value of resistance between two ungrounded inputs.

FULL POWER BANDWIDTH (FPBW) - The maximum frequency at which a full size undistorted sine wave can be obtained at the output of the amplifier.

GAIN BANDWIDTH PRODUCT - The product of the gain and bandwidth at some specified frequency.

INPUT BIAS CURRENT (I_{BIAS}) - The average of the currents flowing into the input terminals when the output is at zero voltage.

INPUT CAPACITANCE (C_{IN}) - The capacitance of either input with the other grounded.

INPUT NOISE CURRENT (i_n) - The input noise current that would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance.

INPUT OFFSET CURRENT (I_{OS}) - The difference in the currents flowing into the two input terminals when the output is at zero voltage.

INPUT OFFSET VOLTAGE (V_{OS}) - The differential D.C. voltage required to zero the output voltage with no input signal or load. Input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT NOISE VOLTAGE (e_n) - The input noise voltage that would reproduce the noise seen at the output if all the amplifier noise sources and source resistances were set to zero.

INPUT RESISTANCE (R_{IN}) - The ratio of the change in input voltage to the change in input current at either terminal with the other grounded.

LARGE SIGNAL VOLTAGE GAIN (A_V) - The ratio of the peak to peak output voltage swing (over a specified range) to the change in input voltage required to drive the output.

OUTPUT CURRENT (I_{OUT}) - The output current available from the amplifier at some specified output voltage.

OUTPUT RESISTANCE (RO) - The ratio of the change in output voltage to the change in output current.

OUTPUT SHORT CIRCUIT CURRENT (I_{SC}) - The maximum output current available from the amplifier with the output shorted to ground (or other specified potential).

OUTPUT VOLTAGE SWING (VOUT) - The peak to peak output voltage swing, referred to ground, that can be obtained without clipping under specified loading conditions.

OVERSHOOT - Peak excursion above final value of an output step response.

POWER SUPPLY REJECTION RATIO (PSRR) - The ratio of the change in input offset voltage to the change in power supply voltage producing it.

RISE TIME (t_r) - The time required for an output voltage step to change from 10% to 90% of its final value, when the input is subjected to a small voltage pulse.

SETTLING TIME - The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE (SR) - The rate of change of the output under large signal conditions. Slew rate may be specified separately for both positive and negative going changes.

SUPPLY CURRENT (I_S) - The current required from the power supply to operate the amplifier with no load and the output at zero volts.

SUPPLY VOLTAGE RANGE - The range of power supply voltage over which the amplifier may be safely operated.

UNITY GAIN BANDWIDTH - The frequency range from D.C. to that frequency where the amplifiers open loop gain is unity.

HARRIS

HA-1608

+10V Adjustable Voltage Reference

FEATURES

- MONOLITHIC CONSTRUCTION
- INITIAL ACCURACY +10V ± 0.010V
- OUTPUT VOLTAGE ERROR, TOTAL ±1/4 LSB
- LOW NOISE $20\mu V_{p-p}$
- WIDE INPUT RANGE 12V TO 30V
- LOW POWER DISSIPATION 30mW
- OUTPUT SHORT CIRCUIT PROTECTION
- ADJUSTABLE OUTPUT

APPLICATIONS

- AN ECONOMICAL EXTERNAL REFERENCE FOR: HI-5608; DAC 08; AD1408; AD559
- VOLTAGE REGULATOR REFERENCE
- PORTABLE BATTERY OPERATED EQUIPMENT
- NEGATIVE 10V REFERENCE

DESCRIPTION

HA-1608 is a monolithic +10V adjustable voltage reference featuring accuracy and temperature stability specifications detailed exclusively for 8 bit data conversion systems. A stable +10V output is provided by a reference zener and buffer amplifier coupled with laser trimmed feedback and zener bias resistors. Long term stability is ensured through integration of all reference components into a monolithic design. Flexibility of HA-1608 is provided through an external trim control which allows the user to adjust the output voltage for binary or BCD applications without affecting overall performance.

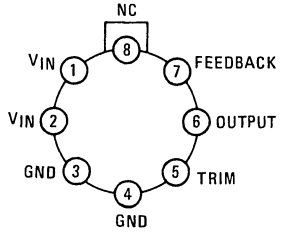
These devices provide a total output voltage error of ± 1/4 LSB for 8 bit D/A or A/D converters. Low standby power (0.3mW) makes HA-1608 a natural selection for portable battery operated equipment, comparator references, and reference stacking circuits. These devices can also be used on -10V references.

HA-1608 is packaged in 8 pin metal cans (TO-99) and the pinout is arranged for convenient replacement of other less accurate regulators in applications demanding minimal change with temperature and time. HA-1608-2 is specified for -55°C to +125°C operation while the HA-1608-5 operates from 0°C to +75°C.

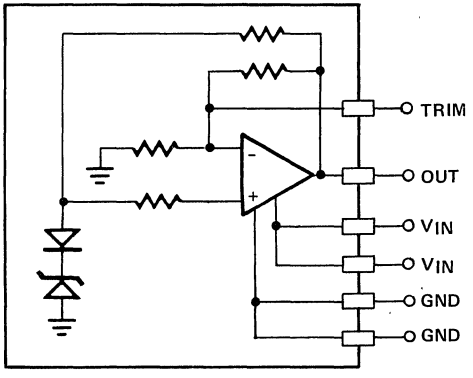
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage	40V	Operating Temperature Range	
Output Short Circuit Duration	Indefinitely	HA-1608-2	-55°C to +125°C
Power Dissipation	500mW	HA-1608-5	0°C to +75°C
Storage Temperature Range	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS (Note 2) (V_{IN} = +15V, I_L = 0mA, unless otherwise specified)

PARAMETER	TEMP	HA-1608-2 -55°C to +125°C MIN	TYP	MAX	HA-1608-5 0°C to +75°C MIN	TYP	MAX	UNITS
POWER INPUT CHARACTERISTICS								
Input Voltage Range, V_{IN}	Full	12	15	30	12	15	30	V
Quiescent Current, I_Q	25°C		1.9			1.9		mA
	Full			3.0			3.0	
REGULATED OUTPUT CHARA.'S								
Output Voltage, V_O	25°C	9.990	10.00	10.010	9.990	10.00	10.010	V
Output Load Current, I_L	Full	10	20		10	20		mA
Line Regulation (V_{IN} = 12V to 30V)	25°C		0.006			0.006		%/V
	Full			0.015			0.015	
Load Regulation (I_L = Open to 10mA)	25°C		0.006			0.006		%/mA
	Full			0.015			0.015	
Output Voltage Error Total I_L = 0mA (Relative to 8-bit accuracy, see Definition #3)	Full			±1/4 LSB			±1/4 LSB	
Output Noise Voltage, EN 0.1Hz to 10Hz	Full		35			35		μV_{p-p}
Dynamic Load Settling Time to ±0.1%	25°C		2.5			2.5		μs
to ±0.01%	25°C		5			5		
Warm-up Time (to ±0.01%)	25°C		1			1		sec
	Full		3			3		

NOTES:

1. Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

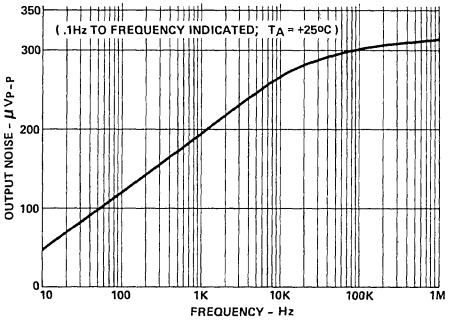
2. The specified electrical characteristics apply to suggested hook-up only.

DEFINITIONS

1. Output Noise Voltage - the output noise voltage in a specified frequency band.
2. Quiescent Current, I_Q - the current required from the supply to operate the device at no load condition after the device is warmed-up.
3. Output Voltage Error Total - Includes effects of Noise Voltage, Line Regulation, and $\Delta V_0 TC$ relative to 8-bit (10V output) resolution where: 1 LSB = one part in 256 or 39mV for a +10V output.
4. Line Regulation (%/V) - the ratio of the change in output voltage to the change in line voltage producing it; line regulation (%/V) = $[(\Delta V_0/10V) \times 100]/\Delta V_{IN}$.
5. Load Regulation (%/mA) - the ratio of the change in output voltage to the change in load current producing it; load regulation (%/mA) = $[(\Delta V_0/10V) \times 100]/\Delta mA$.
6. Dynamic Load Settling Time - the time required for the output to settle to within the specified error band for a change in the load current of 1mA.

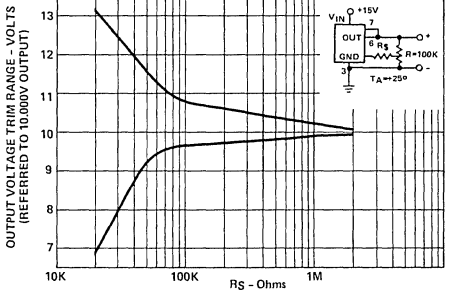
PERFORMANCE CURVES

OUTPUT WIDEBAND NOISE VS. BANDWIDTH

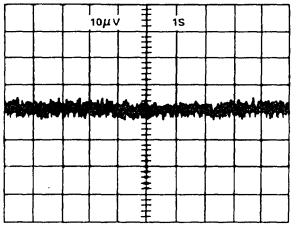


OUTPUT WIDEBAND NOISE VS. BANDWIDTH

OUTPUT VOLTAGE TRIM VS. RS



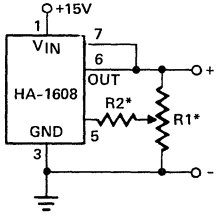
OUTPUT VOLTAGE TRIM VS. R_S



OUTPUT NOISE (0.1Hz TO 10Hz)

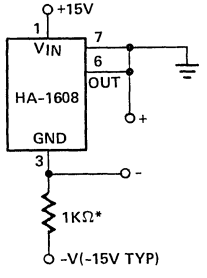
APPLICATIONS

TYPICAL HOOK-UP WITH OUTPUT TRIM



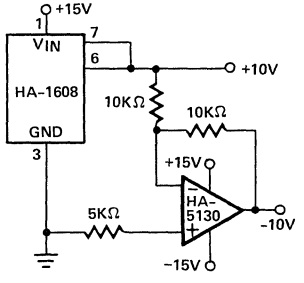
*NOTE: R_1 potentiometer value can be 10K to 100K R_2 can range from 10K to 2M

NEGATIVE 10 VOLT REFERENCE



*NOTE: The value of R may reduce the output current available to less than that specified on the data sheet.

±10V REFERENCE



HARRIS HA-2400/2404/2405

PRAM Four Channel Programmable Amplifier

2

FEATURES

- PROGRAMMABILITY
- HIGH SLEW RATE 30V/μs
- WIDE GAIN BANDWIDTH 40MHz
- HIGH GAIN 150,000
- LOW OFFSET CURRENT 5nA
- HIGH INPUT IMPEDANCE 30MΩ
- SINGLE CAPACITOR COMPENSATION
- DTL/TTL COMPATIBLE INPUTS

APPLICATIONS

- THOUSANDS OF NEW APPLICATIONS; PROGRAM
  - SIGNAL SELECTION/MULTIPLEXING
  - OP AMP GAIN
  - OSCILLATOR FREQUENCY
  - FILTER CHARACTERISTICS
  - ADD-SUBTRACT FUNCTIONS
  - INTEGRATOR CHARACTERISTICS
  - COMPARATOR LEVELS

DESCRIPTION

HA-2400/2404/2405 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

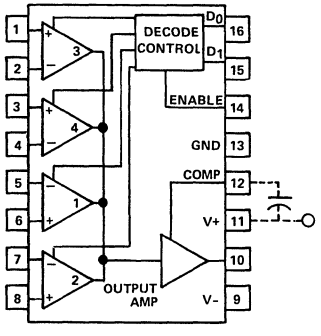
Each channel of the HA-2400/2404/2405 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing, signal selection, and mathematical function designs. With 30V/ μs slew rate, 40MHz gain bandwidth, and 30M ohms input impedance these devices are ideal building blocks for signal generators, active filters, and data acquisition designs. Programmability coupled with 2mV typical offset voltage and 5nA offset current makes these amplifiers outstanding components for signal conditioning circuits.

HA-2400/2404/2405 are available in a 16 pin dual-in-line package. HA-2400 is specified from -55°C to +125°C. HA-2404 is specified over the -25°C to +85°C range, while HA-2405 operates from 0°C to +75°C.

PINOUT

TOP VIEW

Section 11 for Packaging



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

SCHEMATIC

Condensed circuit diagram for a programmable amplifier (PRAM HA-2400)

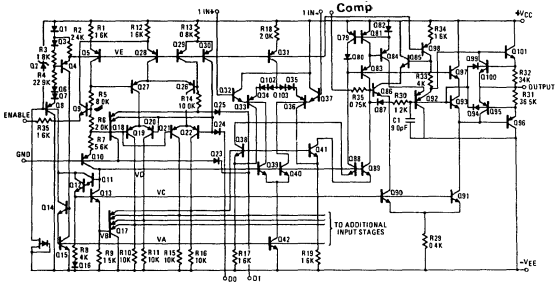


Diagram includes: ONE INPUT STAGE, DECODE CONTROL, BIAS NETWORK AND OUTPUT STAGE

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals	45.0V	Internal Power Dissipation (Note 13)	300mW
Differential Input Voltage	$\pm V_{Supply}$	Operating Temperature Range	$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2400)
Digital Input Voltage	−0.76V to +10.0V		$-25^{o}C \leq T_A \leq +85^{o}C$ (HA-2404)
Output Current	Short Circuit Protected ($I_{SC} \leq \pm 33mA$)		$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2405)
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

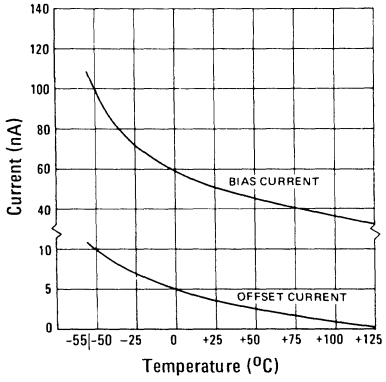
Digital inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$
Limits apply to each of the four channels, when addressed.

PARAMETER	TEMP.	HA-2400/HA-2404 LIMITS MIN.	HA-2400/HA-2404 LIMITS TYP.	HA-2400/HA-2404 LIMITS MAX.	HA-2405 LIMITS MIN.	HA-2405 LIMITS TYP.	HA-2405 LIMITS MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		4	9		4	9	mV
	Full			11			11	mV
Bias Current (Note 12)	+25°C		50	200		50	250	nA
	Full			400			500	nA
Offset Current (Note 12)	+25°C		5	50		5	50	nA
	Full			100			100	nA
Input Resistance (Note 12)	+25°C		30			30		MΩ
Common Mode Range	Full	±9.0			±9.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 1,5)	+25°C	50K	150K		50K	150K		V/V
	Full	25K			25K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		dB
Gain Bandwidth (Note 3)	+25°C	20	40		20	40		MHz
(Note 4)	+25°C	4	8		4	8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current	+25°C	10	20		10	20		mA
Full Power Bandwidth (Notes 3, 5)	+25°C	200	500		200	500		kHz
(Notes 4,5)	+25°C	100	200		100	200		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	+25°C		20	45		20	50	ns
Overshoot (Notes 4,6)	+25°C		25	40		25	40	%
Slew Rate (Notes 3,7)	+25°C	20	30		20	30		V/μs
(Notes 4,7)	+25°C	6	8		6	8		V/μs
Settling Time (Notes 4, 7, 8)	+25°C		1.5	2.5		1.5	2.5	μs
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full		1	1.5		1	1.5	mA
Digital Input Current ($V_{IN} = +5.0V$)	Full		5			5		nA
Output Delay (Note 9)	+25°C		100	250		100	250	ns
Crosstalk (Note 10)	+25°C	-80	-110		-74	-110		dB
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.8	6.0		4.8	6.0	mA
Power Supply Rejection Ratio (Note 11)	Full	74	90		74	90		dB

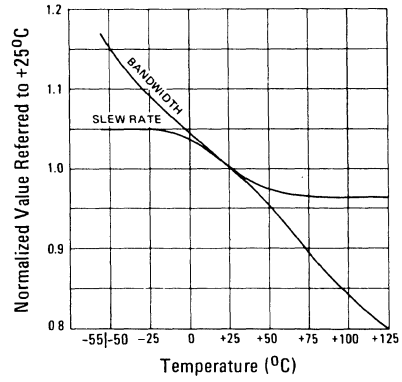
NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 5V$,D.C.
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2K\Omega$, $C_L = 50pF$
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2K\Omega$, $C_L = 50pF$
5. $V_{OUT} = 20V$ peak-to-peak
6. $V_{OUT} = 200mV$ peak-to-peak
7. $V_{OUT} = 10.0V$ peak-to-peak
8. To 0.1% of final value
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10$ V.D.C.
11. $V_{SUPP} = \pm 10V$.D.C. to $\pm 20V$.D.C.
12. Unselected channels have approximately the same input parameters.
13. Derate by 4.3mW/°C above 105°C

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.

INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE

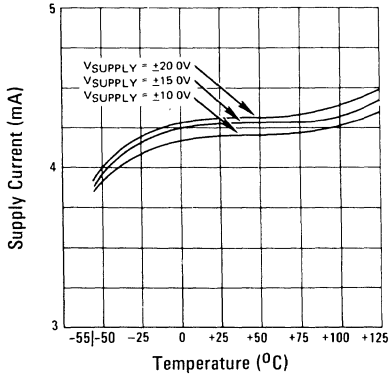


NORMALIZED A.C. PARAMETERS VS. TEMPERATURE

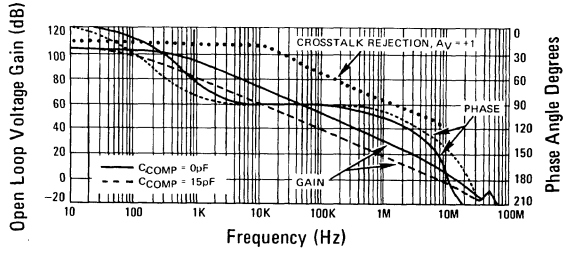


2

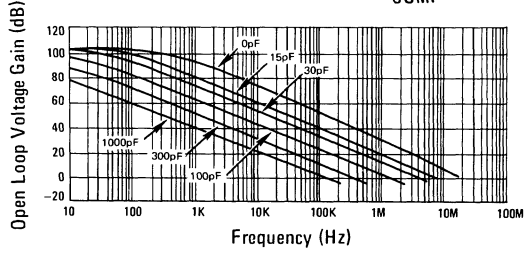
POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



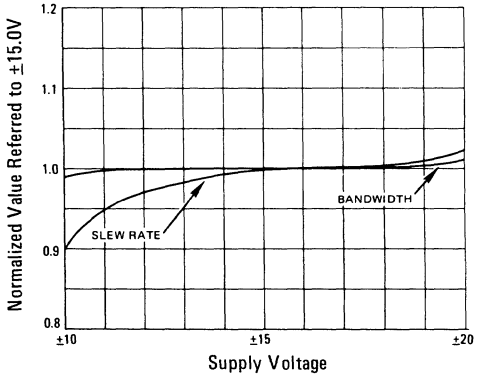
OPEN LOOP FREQUENCY AND PHASE RESPONSE



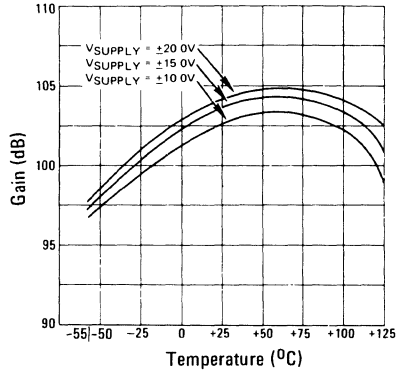
FREQUENCY RESPONSE VS. C_{COMP}



NORMALIZED A.C. PARAMETERS VS. SUPPLY VOLTAGE

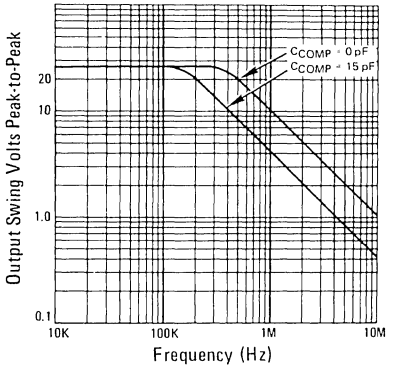


OPEN LOOP VOLTAGE GAIN VS. TEMPERATURE

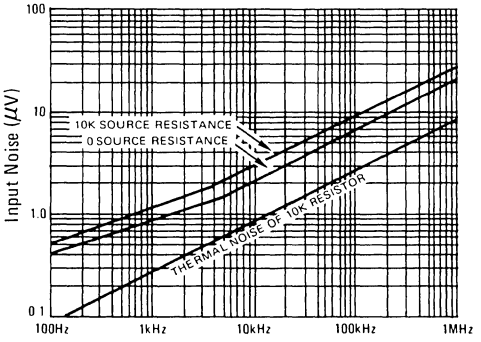


CHARACTERISTIC CURVES (continued)

OUTPUT VOLTAGE SWING VS. FREQUENCY

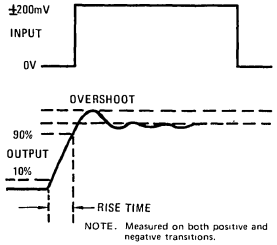


EQUIVALENT INPUT NOISE VS. BANDWIDTH

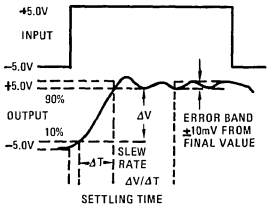


Upper 3dB Frequency
Lower 3dB Frequency - 10Hz
Broadband Noise Characteristics

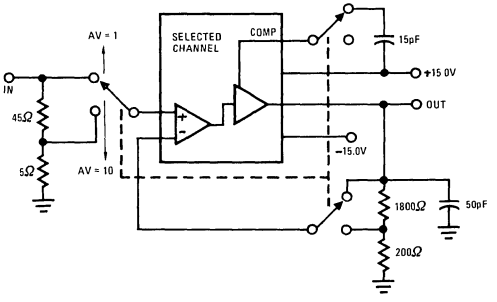
TRANSIENT RESPONSE



SLEW RATE AND SETTLING

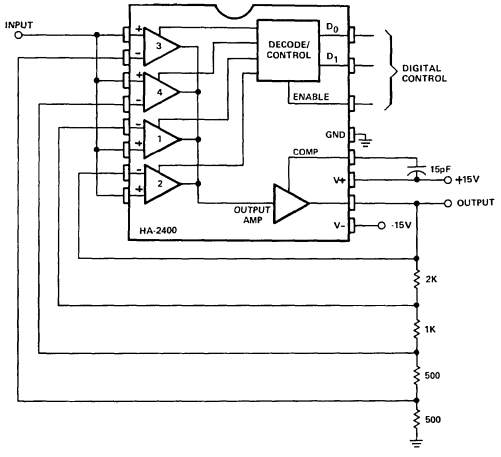


SLEW RATE AND TRANSIENT RESPONSE

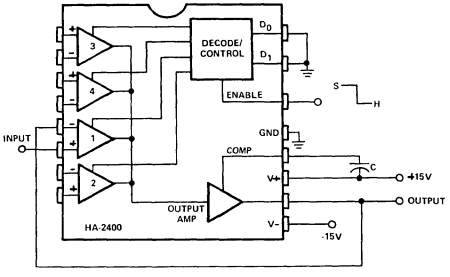


TYPICAL APPLICATIONS

AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN



SAMPLE AND HOLD



Sample charging rate = $\frac{I_1}{C}$ V/sec.

Hold drift rate = $\frac{I_2}{C}$ V/sec.

Switch pedistal error = $\frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$ A

$I_2 \approx 200 \times 10^{-9}$ A @ +25°C

$\approx 600 \times 10^{-9}$ A @ -55°C

$\approx 100 \times 10^{-9}$ A @ +125°C

$Q \approx 2 \times 10^{-12}$ Coul.

FOR MORE EXAMPLES, SEE HARRIS APPLICATION NOTE 514

2

HARRIS

HA-2500/02/05

Precision High Slew Rate Operational Amplifiers

2

FEATURES

- HIGH SLEW RATE 30V/μS
- FAST SETTLING 330ns
- WIDE POWER BANDWIDTH 500kHz
- HIGH GAIN BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 50 MΩ
- LOW OFFSET CURRENT 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISTION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

HA-2500/2502/2505 comprise a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Slew rate of ±25V/μs and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12 MHz bandwidth and 500kHz power bandwidth make these devices well suited to R.F. and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2500/2502/2505 are particularly useful components in signal conditioning designs.

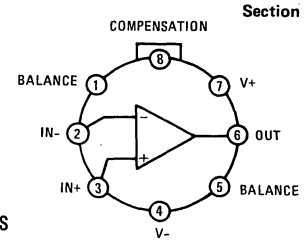
The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

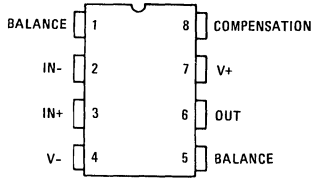
HA-2500/2502/2505 are available in metal can (TO-99) packages. HA-2500 and HA-2502 are specified over the -55°C to +125°C range. HA-2505 is specified from 0°C to +75°C.

PINOUT

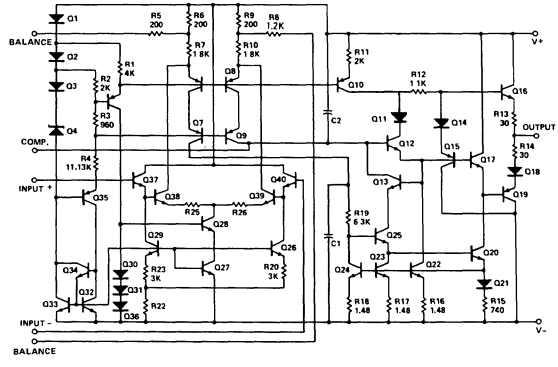
Section 11 for Packaging

TOP VIEWS





SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range –	HA-2500/HA-2502	$-55^oC \leq T_A \leq +125^oC$
Differential Input Voltage	±15.0V		HA-2505	$0^oC \leq T_A \leq +75^oC$
Peak Output Current	50mA	Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$
Internal Power Dissipation	300mW			

ELECTRICAL CHARACTERISTICS

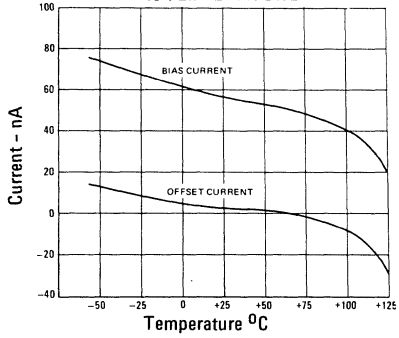
V+ = +15V D.C., V- = -15V D.C.

		HA-2500 -55°C to +125°C			HA-2502 -55°C to +125°C			HA-2505 0°C to +75°C			
		LIMITS			LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C Full		2	5 8		4	8 10		4	8 10	mV mV
Offset Voltage Average Drift	Full		20			20			20		µV/°C
Bias Current	+25°C Full		100	200 400		125	250 500		125	250 500	nA nA
Offset Current	+25°C Full		10	25 50		20	50 100		20	50 100	nA nA
Input Resistance (Note 10)	+25°C	25	50		20	50		20	50		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1,4)	+25°C Full	20K 15K	30K		15K 10K	25K		15K 10K	25K		V/V V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	350	500		300	500		300	500		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1,5,8 & 12)	+25°C	±25	±30		±20	±30		±20	±30		V/µs
Settling Time to 0.1% (Notes 1,5,8 & 12)	+25°C		0.33			0.33			0.33		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

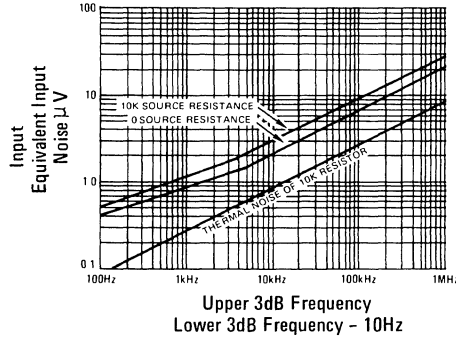
NOTES:
1. $R_L = 2K$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $V_O \pm 200mV$
8. See transient response test circuits and waveforms page four.
9. $\Delta V = \pm 5.0V$
10. This parameter value is based on design calculations.
11. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = S.R./2\pi V_{peak}$.
12. $V_{OUT} = \pm 5V$

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

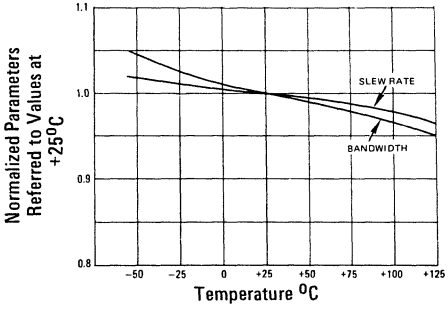
INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE



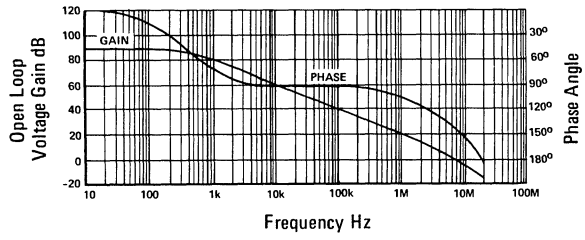
EQUIVALENT INPUT NOISE vs BANDWIDTH



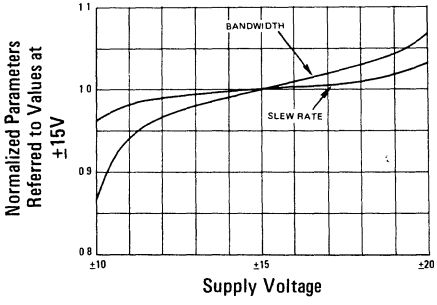
NORMALIZED AC PARAMETERS vs TEMPERATURE



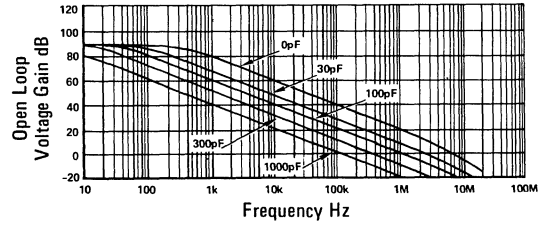
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C

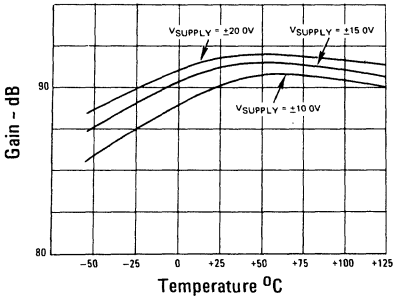


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

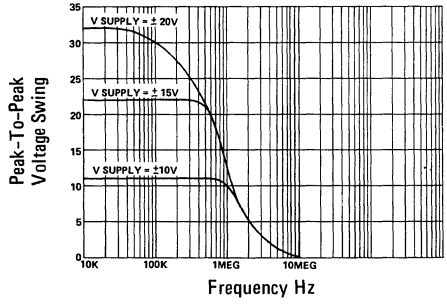


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

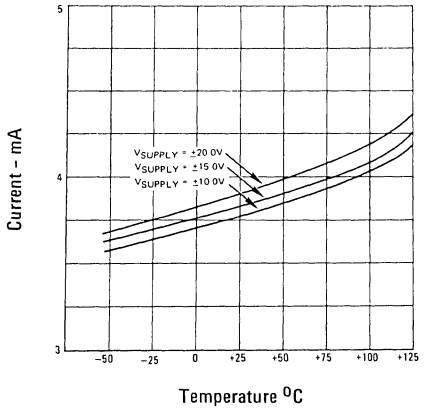
OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



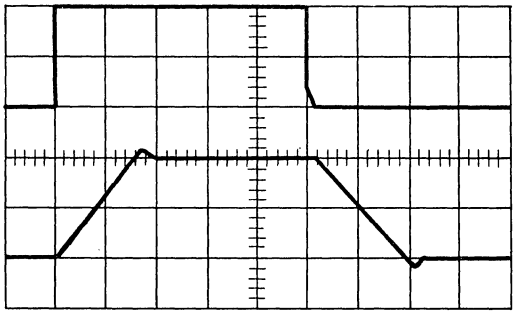
OUTPUT VOLTAGE SWING vs FREQUENCY AT +25°C



POWER SUPPLY CURRENT
vs TEMPERATURE



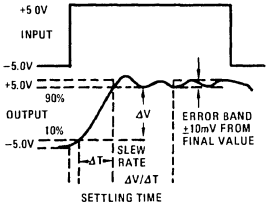
VOLTAGE FOLLOWER PULSE RESPONSE



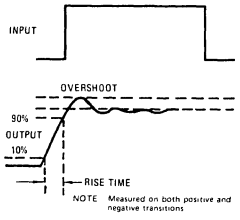
R_L = 2KΩ, C_L = 50pF
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 200ns/Div.
T_A = +25°C, V_S = ±15.0V

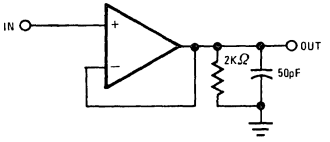
SLEW RATE AND
SETTLING TIME



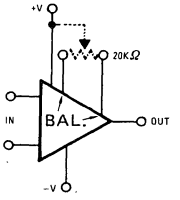
TRANSIENT RESPONSE



SLEW RATE AND
TRANSIENT RESPONSE



SUGGESTED
VOS ADJUSTMENT



2

HARRIS

HA-2510/2512/2515

High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE 60V/μs
- FAST SETTLING 250ns
- WIDE POWER BANDWIDTH 1,000kHz
- HIGH GAIN BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 100MΩ
- LOW OFFSET CURRENT 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

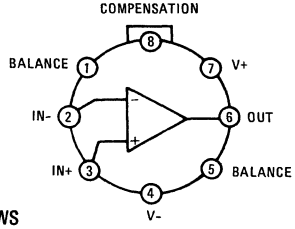
The HA-2510/2512/2515 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidth for internally compensated monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

The $\pm$60V/ μs slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/2512/2515's superior 12MHz gain bandwidth and 1000kHz power bandwidth is extremely useful in R.F. and video applications. For accurate signal conditioning these amplifiers also provide 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

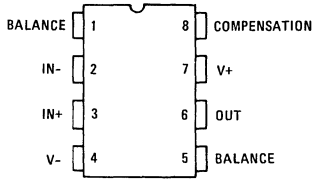
The HA-2510/2512 are available in metal can (TO-99) and 14-pin flat packages. HA-2510 and HA-2512 are specified from -55°C to +125°C. HA-2515 is specified over the 0°C to +75°C range, and is available in the TO-99 package.

PINOUT

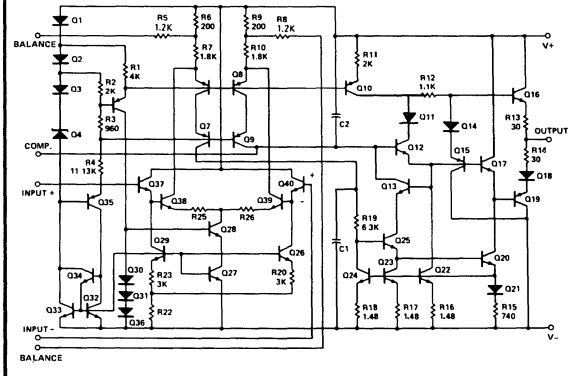
Section 11 for Packaging



TOP VIEWS



SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2510/HA-2512	$-55^oC \leq T_A \leq +125^oC$		
HA-2515	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

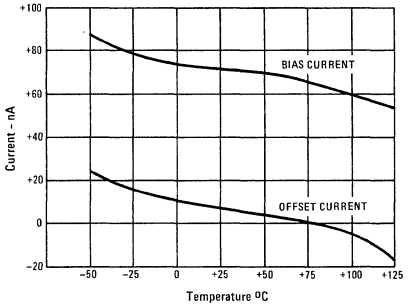
V+ = +15V D.C., V– = 15V D.C.

PARAMETER	TEMP.	HA-2510 -55°C to +125°C LIMITS MIN.	HA-2510 LIMITS TYP.	HA-2510 LIMITS MAX.	HA-2512 -55°C to +125°C LIMITS MIN.	HA-2512 LIMITS TYP.	HA-2512 LIMITS MAX.	HA-2515 0°C to +75°C LIMITS MIN.	HA-2515 LIMITS TYP.	HA-2515 LIMITS MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 10)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1,4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4, 11)	+25°C	750	1000		600	1000		600	1000		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±50	±65		±40	±60		±40	±60		V/µs
Settling Time (Notes 1, 5, 8 & 12)	+25°C		0.25			0.25			0.25		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

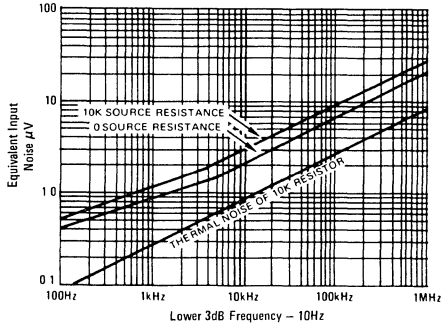
NOTES:
1. R_L = 2K
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. C_L = 50pF
6. $V_O = \pm 200mV$
7. $V_O = \pm 200mV$
8. See transient response test circuits and waveforms
9. $\Delta V = \pm 5.0V$
10. This parameter value is based upon design calculations.
11. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./2πV_{peak}.
12. $V_{OUT} = \pm 5V$

V+ = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.

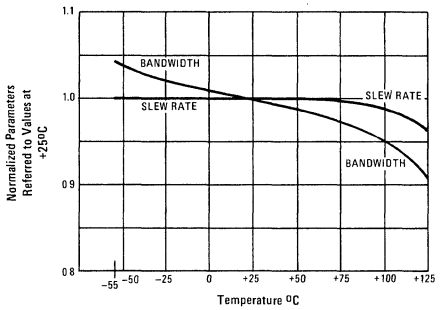
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



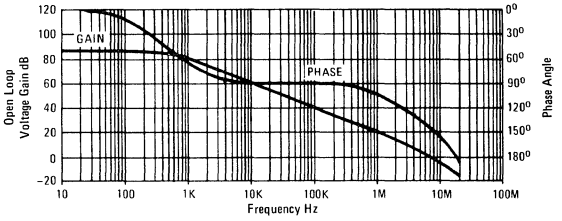
EQUIVALENT INPUT NOISE vs. BANDWIDTH



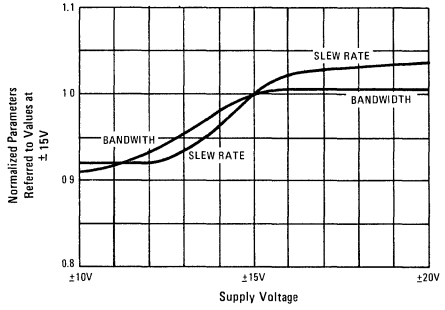
NORMALIZED AC PARAMETERS vs. TEMPERATURE



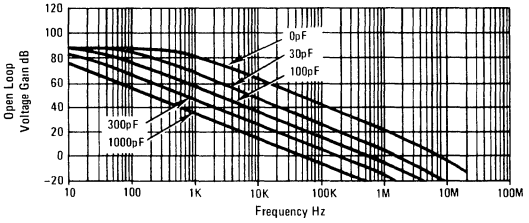
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE

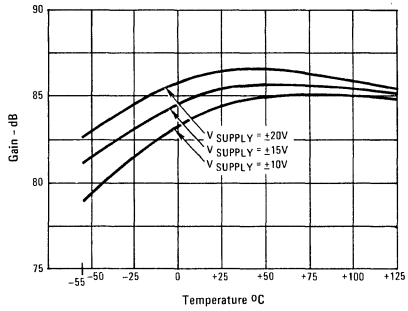


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

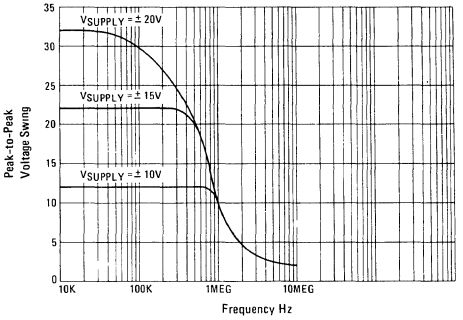


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

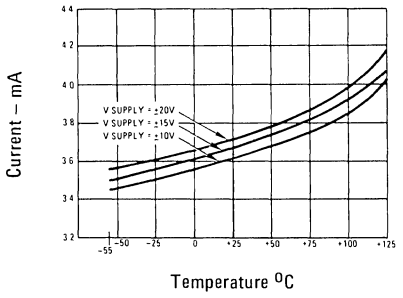
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



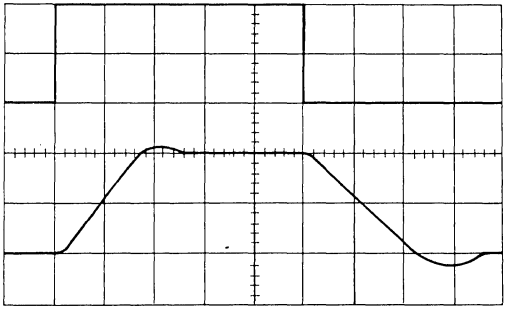
OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C



POWER SUPPLY CURRENT
VS
TEMPERATURE



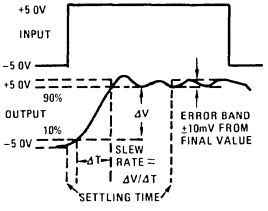
VOLTAGE FOLLOWER PULSE RESPONSE



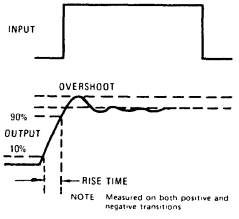
R_L = 2K Ω , C_L = 50pF
Upper Trace: Input
Lower Trace: Output

Vertical = 5V/Div.
Horizontal = 100n/Div.
T_A = +25°C, V_S = ±15.0V

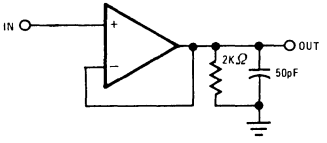
SLEW RATE AND
SETTLING TIME



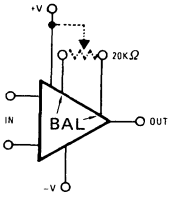
TRANSIENT RESPONSE



SLEW RATE AND
TRANSIENT RESPONSE



SUGGESTED
VOS ADJUSTMENT



2

HA-2520/22/25

Uncompensated High Slew Rate Operational Amplifiers

2

FEATURES

- HIGH SLEW RATE 120V/μs
- FAST SETTLING 200ns
- WIDE POWER BANDWIDTH 2,000kHz
- HIGH GAIN BANDWIDTH 20MHz
- HIGH INPUT IMPEDANCE 100MΩ
- LOW OFFSET CURRENT 10nA

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

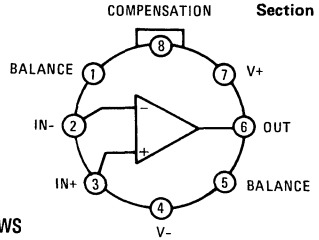
HA-2520/2522/2525 comprise a series of monolithic operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at closed loop gains greater than 3 without external compensation. In additon, these high performance components also provide low offset current and high input impedance.

120V/μs slew rate and 200ns (0.1%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for R.F. and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complimented by 10nA offset current, 100MΩ input impedance and offset trim capability.

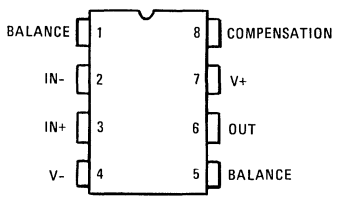
The HA-2520/2522 are available in metal can (TO-99) and 14-pin flat packages. HA-2520 and HA-2522 are specified over -55°C to +125°C range. HA-2525 is specified from 0°C to +75°C, and is available in the TO-99 package.

PINOUT

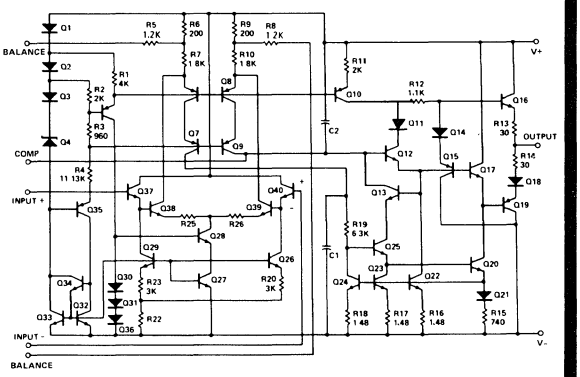
Section 11 for Packaging



TOP VIEWS



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range			
HA-2520/2522	$-55^oC \leq T_A \leq +125^oC$	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2525	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

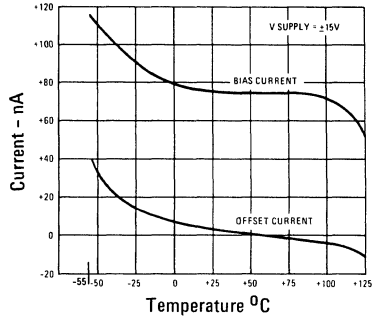
$V+ = +15V$ D.C., $V- = -15V$ D.C.

		HA-2520 -55^oC to $+125^oC$ LIMITS			HA-2522 -55^oC to $+125^oC$ LIMITS			HA-2525 0^oC to $+75^oC$ LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance (Note 9)	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1,4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C	10	20		10	20		10	20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4, 10)	+25°C	1500	2000		1200	1600		1200	1600		kHz
TRANSIENT RESPONSE ($A_V = +3$)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
Slew Rate (Notes 1, 5, 8 & 11)	+25°C	±100	±120		±80	±120		±80	±120		V/µs
Settling Time (Notes 1, 5, 8 & 11)	+25°C		0.20			0.20			0.20		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

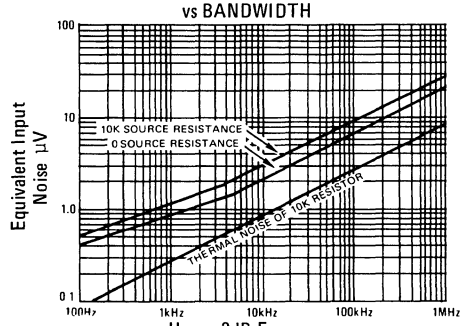
NOTES:
1. $R_L = 2K$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. See transient response test circuits and waveforms
9. This parameter value is based upon design calculations.
10. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./$2\pi V_{peak}$.
11. $V_{OUT} = \pm 5V$

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

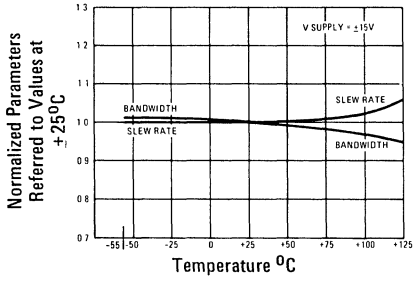
INPUT BIAS AND OFFSET CURRENT
vs TEMPERATURE



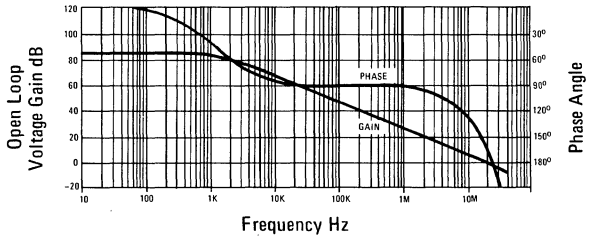
EQUIVALENT INPUT NOISE
vs BANDWIDTH



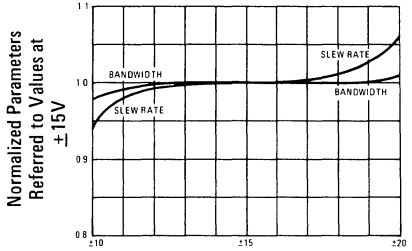
NORMALIZED AC PARAMETERS
vs TEMPERATURE



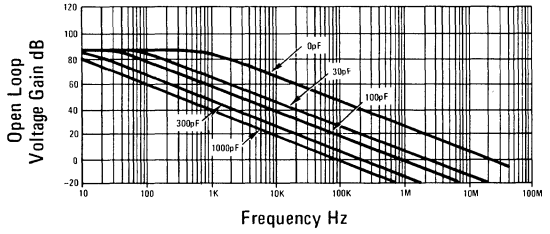
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



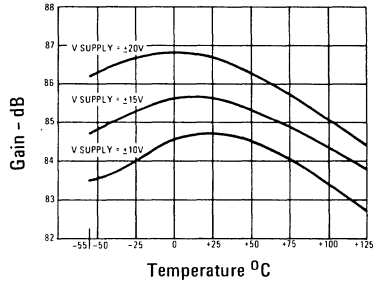
NORMALIZED AC PARAMETERS
vs SUPPLY VOLTAGE AT +25°C



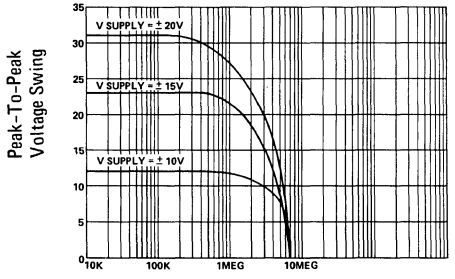
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



OPEN LOOP VOLTAGE GAIN
vs TEMPERATURE

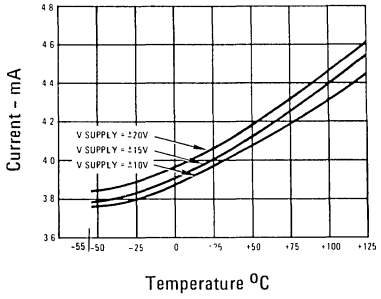


OUTPUT VOLTAGE SWING
vs FREQUENCY AT +25°C

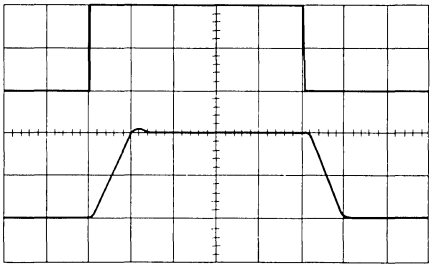


PERFORMANCE CURVES (continued)

POWER SUPPLY CURRENT
vs TEMPERATURE



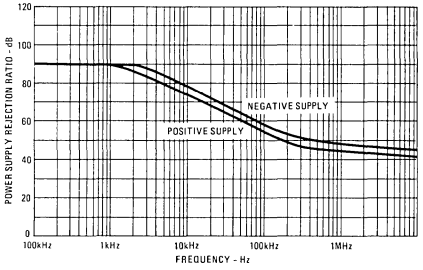
VOLTAGE FOLLOWER PULSE RESPONSE



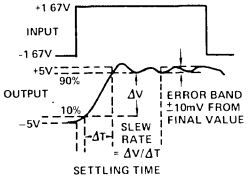
$R_L = 2K\Omega$, $C_L = 50pF$
Upper Trace: Input; 1.67V/Div.
Lower Trace: Output; 5V/Div.

Horizontal = 100ns/Div.
$T_A = +25^oC$, $V_S = \pm 15V$

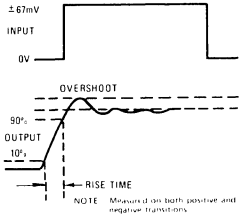
POWER SUPPLY REJECTION RATIO
VS. FREQUENCY



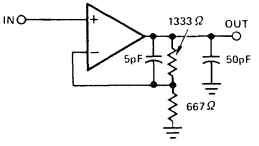
SLEW RATE AND
SETTLING TIME



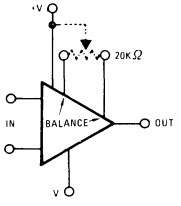
TRANSIENT
RESPONSE



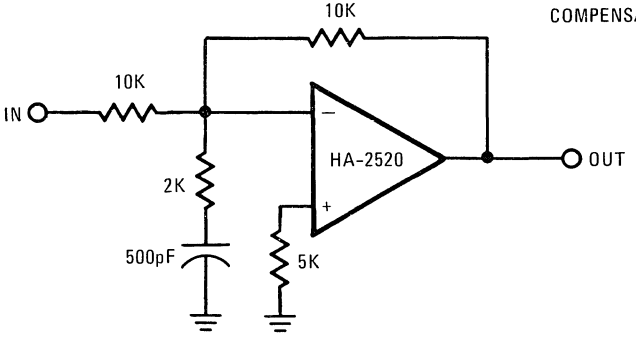
SLEW RATE AND
TRANSIENT RESPONSE



SUGGESTED
VOS ADJUSTMENT



TYPICAL APPLICATIONS



COMPENSATION CIRCUIT FOR INVERTING UNITY GAIN

Slew Rate ≈ 120V/μs
Bandwidth ≈ 10MHz
Settling Time ≈ 500ns

HARRIS HA-2530/2535

High Slew Rate, Wideband Inverting Amplifier

FEATURES

- HIGH SLEW RATE ±320V/μs
- FAST SETTLING TIME 550ns
- WIDE POWER BANDWIDTH 5MHz
- HIGH GAIN BANDWIDTH PRODUCT 70MHz
- LOW OFFSET VOLTAGE 0.8mV
- LOW POWER SUPPLY CURRENT 3.5

Product to be Discontinued. HA-2539 or HA-2540 Suggested for New Designs.

APPLICATIONS

- PULSE AMPLIFIC
- SIGNAL CONDITIO
- SIGNAL GENERATOR
- COAXIAL CABLE DRIVE
- INTEGRATORS

DESCRIPTION

HA-2530 and HA-2535 are monolithic high speed inverting amplifiers which deliver supe w rate, bandwidth, and accuracy specifications other amplifier in its class. Designs of ated amplifiers utilize the feed produce excellent d low power con- compensation at

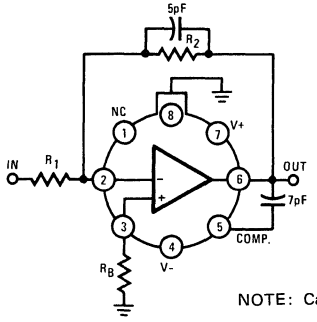
components for pulse circuits, and high speed integrators that can take ±320V/μs slew rate and 550ns (0.1%) settling Hz gain bandwidth product, 5MHz power bandwidth pled with 0.8mV offset voltage and ±50mA typical output current levels make these amplifiers ideally suited for signal conditioning, signal generation, and coaxial driver applications.

The HA-2530 and HA-2535 are available in metal can (TO-99) packages. HA-2530 is specified over the -55°C to +125°C range while HA-2535 is specified from 0°C to +75°C.

PINOUT

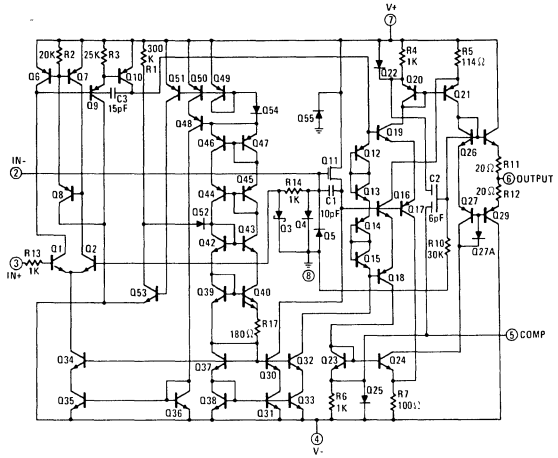
Section 11 for Packaging

TOP VIEW



NOTE: Case tied to V-

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Internal Power Dissipation (Note 1)	550mW	
		Operating Temperature Range	$-55^{o}C \leq T_A \leq +125^{o}C$	(HA-2530)
Peak Output Current	±100mA		$0^{o}C \leq T_A \leq +75^{o}C$	(HA-2535)
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$	

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ Unless Otherwise Specified.

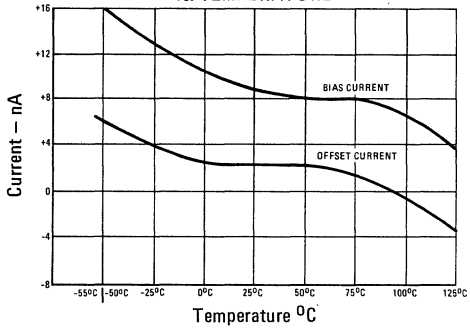
		HA-2530 -55°C to +125°C LIMITS			HA-2535 0°C to +75°C LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.8			0.8		mV
	Full			3			5	mV
Average Offset Voltage Drift	Full		5			5		µV/°C
Bias Current	+25°C		15			15		nA
	Full			100			200	nA
Offset Current	+25°C		5			5		nA
	Full			20			20	nA
Input Resistance	+25°C		2			2		MΩ
Input Capacitance	+25°C		10			10		pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 2,5)	+25°C		$2X10^6$			$2X10^6$		V/V
	Full	10^5			10^5			V/V
Common-Mode Rejection Ratio (Note 3)	Full	86	100		80	100		dB
Gain Bandwidth Product (Note 4)	+25°C		70			70		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
Output Current (Note 5)	+25°C	±25	±50		±25	±50		mA
Full Power Bandwidth (Note 5)	+25°C	4	5		4	5		MHz
TRANSIENT RESPONSE (NOTES 6&7)								
Rise Time	+25°C		20	40		20	40	ns
Overshoot	+25°C		30	45		30	50	%
Slew Rate	+25°C	±280	±320		±250	±320		V/µs
Settling Time	+25°C		500			500		ns
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.5	8		3.5	8	mA
Power Supply Rejection Ratio (Note 8)	Full	86	100		80	100		dB

NOTES:
1. Derate at 5.5mW/°C for Operation at Ambient Temperature Above 75°C.
2. $R_L = 2K$
3. $V_{CM} = \pm 5.0V$
4. $A_V > 10$
5. $V_O = \pm 10V$
6. $C_L = 50pF$
7. See Transient Response Test Circuit and Wave Forms
8. $\Delta V = \pm 5.0V$

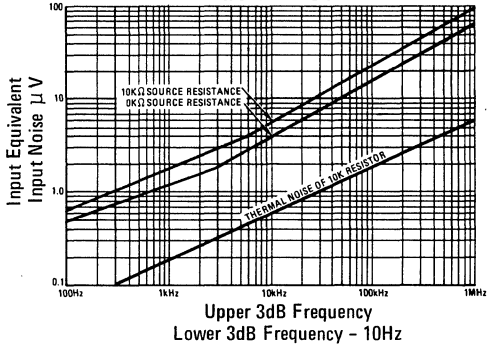
PERFORMANCE CURVES

V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

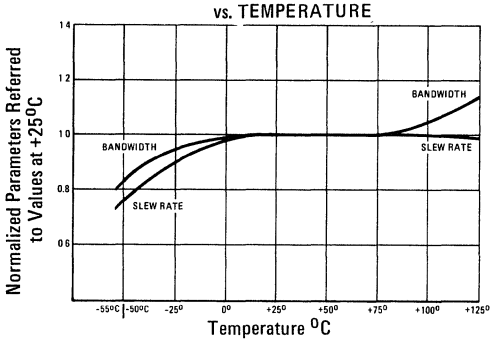
INPUT BIAS AND OFFSET CURRENT
vs. TEMPERATURE



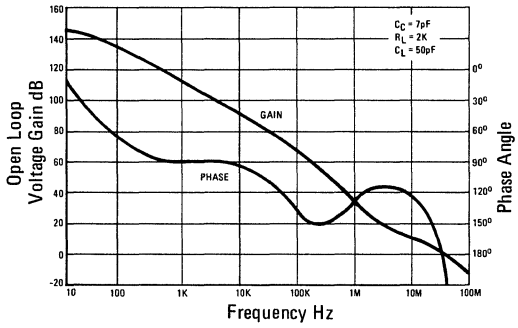
EQUIVALENT INPUT NOISE
vs. BANDWIDTH



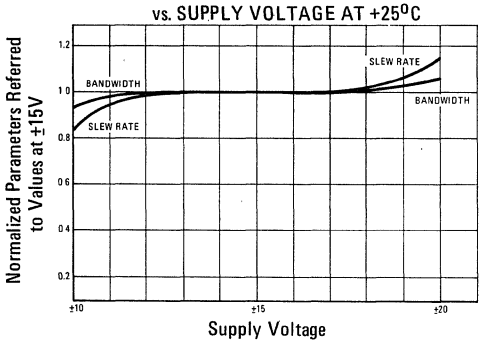
NORMALIZED AC PARAMETERS
vs. TEMPERATURE



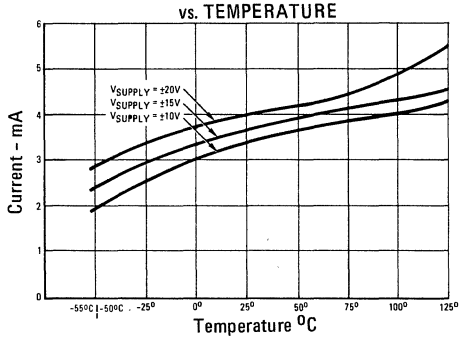
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



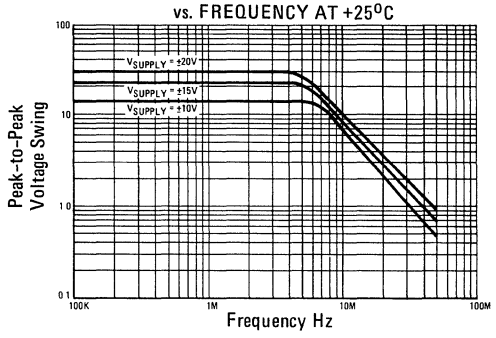
NORMALIZED AC PARAMETERS
vs. SUPPLY VOLTAGE AT +25°C



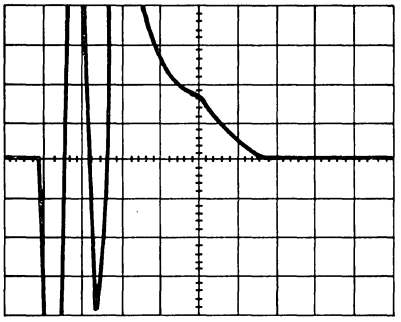
POWER SUPPLY CURRENT
vs. TEMPERATURE



OUTPUT VOLTAGE SWING
vs. FREQUENCY AT +25°C

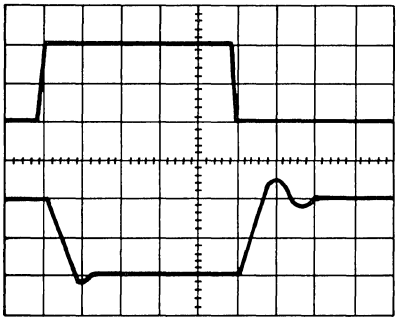


SETTLING TIME MEASUREMENT *1



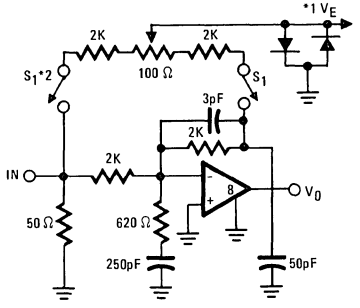
VERTICAL = 5mV/DIV.
HORIZONTAL = 100ns/DIV.
$T_A = +25^oC$, $V_S = \pm 15V$

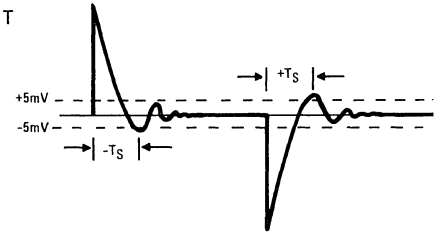
UNITY GAIN PULSE RESPONSE



UPPER TRACE: INPUT VERTICAL = 5V/DIV.
LOWER TRACE: OUTPUT HORIZONTAL = 50ns/DIV.
$T_A = +25^oC$, $V_S = \pm 15V$

SLEW RATE/SETTLING TIME/TRANSIENT RESPONSE TEST CIRCUIT

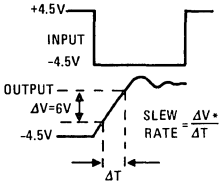




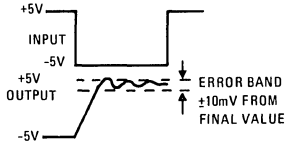
*1 Settling time (T_S) is measured using a high speed high recovery oscilloscope to display the error voltage V_E. When V_E is within ±5mV of final value the output V_O will be within ±10mV (0.1%).

*2 S_1 closed for settling time.

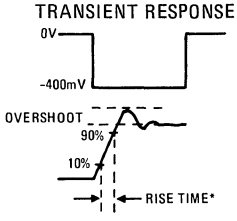
SLEW RATE



SETTLING TIME

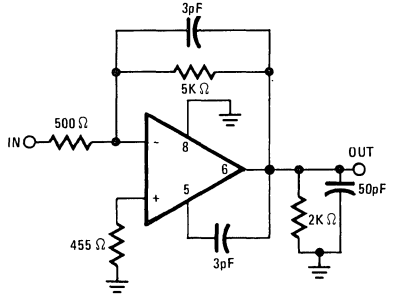


TRANSIENT RESPONSE



* MEASURED ON BOTH POSITIVE AND NEGATIVE EXCURSIONS.

5MHz VIDEO AMPLIFIER (A_V = 10)



HARRIS

HA-2539

Very High Slew Rate Wideband Operational Amplifiers

Preliminary

2

FEATURES

- VERY HIGH SLEW RATE — 600V/μs
- OPEN LOOP GAIN — 30kV/V
- WIDE GAIN-BANDWIDTH — 600MHz
- POWER BANDWIDTH — 9.5MHz
- LOW OFFSET VOLTAGE — 3mV
- INPUT VOLTAGE NOISE — 15nV/$\sqrt{\text{Hz}}$
- OUTPUT VOLTAGE SWING — $\pm$10V

APPLICATIONS

- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- RF OSCILLATORS

GENERAL DESCRIPTION

The Harris HA-2539 represents the ultimate in high slew rate wideband, monolithic, operational amplifiers. It has been designed and constructed with the Harris high frequency BIPDIP (Bipolar dielectric isolation process), and features dynamic parameters never before available from a truly differential device.

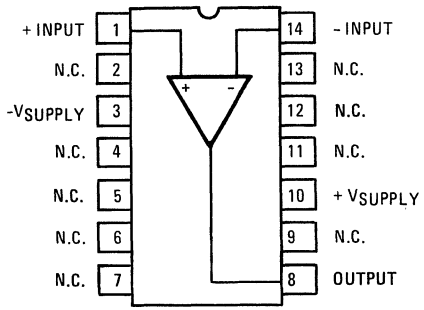
With a 600V/ μs slew rate and a 600MHz gain-bandwidth-product, the HA-2539 is ideally suited for use in video and RF amplifier designs. Full $\pm$ 10V output swing coupled with outstanding A.C. parameters and complemented by high open loop gain makes these devices useful in high speed data acquisition systems.

The HA-2539 is available in the 14 pin CERDIP. The HA-2539-2 denotes -55°C to +125°C operation while the HA-2539-5 operates over the 0°C to +75°C range.

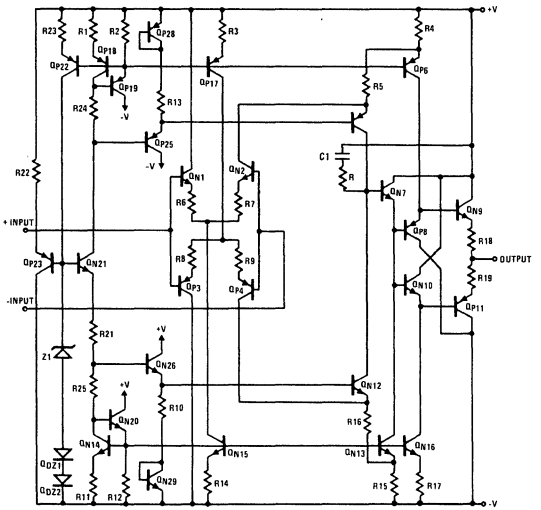
PINOUT

Section 11 for Packaging

TOP VIEW



SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip)
Operating Temperature Range: (HA-2539-2)	$-55^{o}C \leq T_A \leq +125^{o}C$
(HA-2539-5)	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; R_L = 1K ohms, unless otherwise specified.

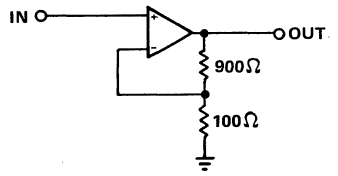
		HA-2539-2 -55°C to +125°C			HA-2539-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3	5		3	15	mV
	FULL			10			20	mV
Average Offset Voltage Drift	FULL		20			20		µV/°C
Bias Current	+25°C		5	20		5	20	µA
	FULL			25			25	µA
Offset Current	+25°C		1	6		1	6	µA
	FULL			8			8	µA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±10			±10			V
Input Voltage Noise (f = 1kHz, $R_g = 0\Omega$)	+25°C		15			15		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	60			60			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		600			600		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±10			±10			V
Output Current (Note 3)	+25°C	10			10			mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	8.7	9.5		8.7	9.5		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		7			7		ns
Overshoot	+25°C		15			8		%
Slew Rate	+25°C	550	600		550	600		V/µs
Settling Time: 10V Step to 0.1%	+25°C		350			350		ns
POWER REQUIREMENTS								
Supply Current	FULL		20	25		20	25	mA
Power Supply Rejection Ratio (Note 9)	FULL	60			60			dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 8.7mW/°C for operation at ambient temperatures above +75°C. Heat sinking required at temperatures above +75°C. T_{JA} = 115°C/W; T_{JC} = 35°C/W. Thermalloy model 6007 heat sink recommended.
3. R_L = 1KΩ, VO = ± 10V
4. V_{CM} = ± 10V
5. V_O = 90mV.
6. A_V = 10.
7. Full power bandwidth guaranteed based on slew rate measurement using FPBW = $\frac{\text{Slew Rate}}{2\pi V_{peak}}$.
8. Refer to Test Circuits section of data sheet.
9. V_{SUPPLY} = ±5 VDC to ±15 VDC

TEST CIRCUITS

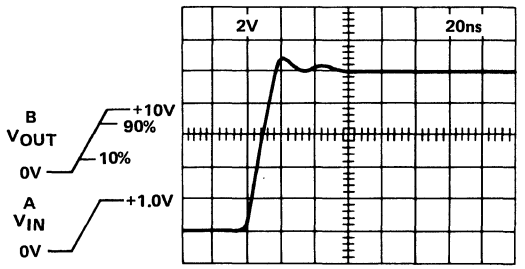
LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT *



A_V = 10
*$C_L \leq$ 10pF

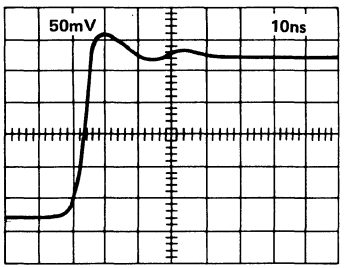
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A = 1.0V/Div., B = 2.0V/Div.)
Horizontal Scale: (Time: 20ns/Div.)

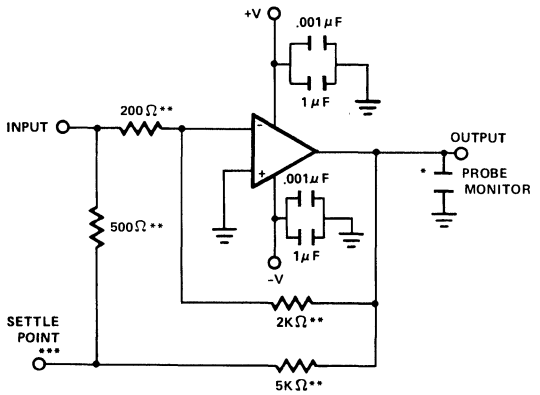


SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: 50mV/Div.)
Horizontal Scale: (Time: 10ns/Div.)



SETTLING TIME TEST CIRCUIT



* Load Capacitance should be less than 10pF.

** It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched.

*** SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

HARRIS

HA-2540

Wideband, Fast Settling Operational Amplifiers

Preliminary

FEATURES

- VERY HIGH SLEW RATE — 400V/μs
- FAST SETTLING TIME — 250ns
- WIDE GAIN-BANDWIDTH — 400MHz
- POWER BANDWIDTH — 6MHz
- LOW OFFSET VOLTAGE — 5mV
- INPUT VOLTAGE NOISE — 15nV/$\sqrt{Hz}$
- OUTPUT VOLTAGE SWING — $\pm$10V
- MONOLITHIC BIPOLAR CONSTRUCTION

APPLICATIONS

- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- FAST, PRECISE D/A CONVERTERS

GENERAL DESCRIPTION

The Harris HA-2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance. Additionally, the HA-2540 has a drive capability of $\pm$10V into a 1K ohm load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

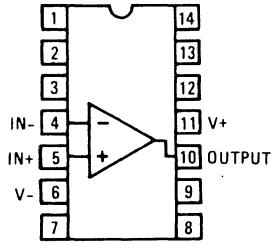
A 400V/ μs slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth-product is ideally suited for wideband signal amplification. A settling time of 250ns also makes the HA-2540 an excellent selection for high speed Data Acquisition Systems.

The HA-2540-2 is specified over the -55°C to +125°C range while the HA-2540-5 is specified from 0°C to +75°C.

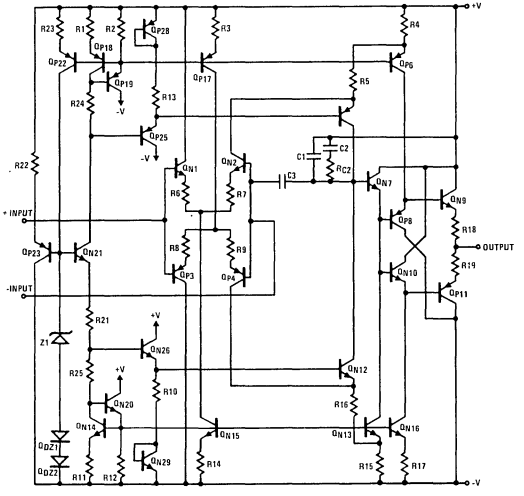
PINOUT

Section 11 for Packaging

TOP VIEW



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip)
Operating Temperature Range: (HA-2540-2)	$-55^{o}C \leq T_A \leq +125^{o}C$
(HA-2540-5)	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; R_L = 1K ohms, unless otherwise specified.

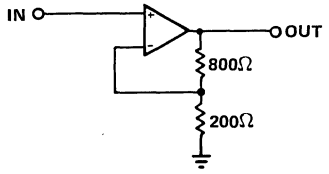
		HA-2540-2 -55°C to +125°C			HA-2540-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3	5		3	15	mV
	FULL			10			20	mV
Average Offset Voltage Drift	FULL		20			20		µV/°C
Bias Current	+25°C		5	20		5	20	µA
	FULL			25			25	µA
Offset Current	+25°C		1	6		1	6	µA
	FULL			8			8	µA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±10			±10			V
Input Noise Voltage (f = 1kHz, $R_g = 0\Omega$)	+25°C		15			15		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	60			60			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		400			400		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±10			±10			V
Output Current (Note 3)	+25°C	10			10			mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	5.5	6		5.5	6		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		14			14		ns
Overshoot	+25°C		5			5		%
Slew Rate	+25°C	350	400		350	400		V/µs
Settling Time: 10V Step to 0.1%	+25°C		250			250		ns
POWER REQUIREMENTS								
Supply Current	FULL		20	25		20	25	mA
Power Supply Rejection Ratio (Note 9)	FULL	60			60			dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 8.7mW/°C for operation at ambient temperatures above +75°c. Heat sinking required at temperatures above +75°c. T_{JA} = 115°C/W; T_{JC} = 35°C/W. Thermalloy model 6007 heat sink recommended.
3. R_L = 1KΩ, VO = ±10V
4. V_{CM} = ±10V
5. V_O = 90mV.
6. A_V = 5.
7. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$.
8. Refer to Test Circuits section of data sheet.
9. V_{SUPPLY} = ±5 VDC to ±15 VDC

TEST CIRCUITS

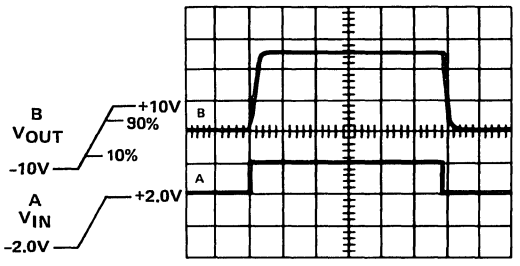
LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT*



A_V = 5
*$C_L \leq$ 10pF

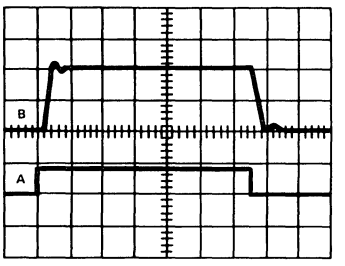
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A = 4.0V/Div., B = 8.0V/Div.)
Horizontal Scale: (Time: 100ns/Div.)

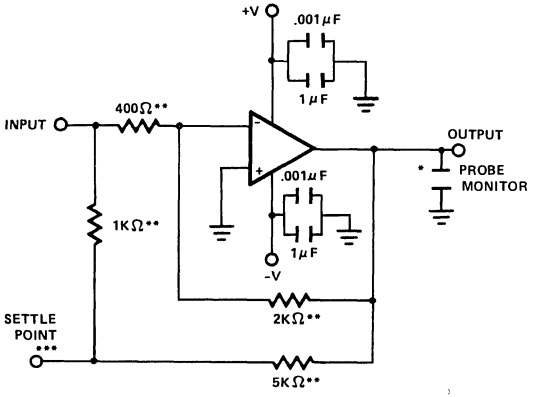


SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: A=50mV/Div., B=100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)



SETTLING TIME TEST CIRCUIT



* Load Capacitance should be less than 10pF.

** It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched.

*** SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

HARRIS HA-2600/2602/2605

WideBand, High Impedance Operational Amplifiers

2

FEATURES

- WIDE BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 0.5mV
- HIGH GAIN 150K V/V
- HIGH SLEW RATE 7V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- VIDEO AMPLIFIER
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

DESCRIPTION

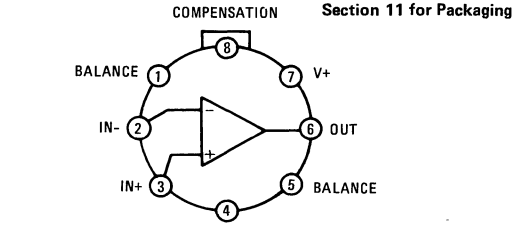
HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500 MΩ, HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth product, 7V/μs slew rate and 150,000V/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characterisitics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

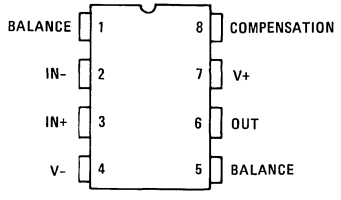
HA-2600 and HA-2602 are guaranteed over -55°C to +125°C. HA-2605 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and HA-2600/2602 are available in 10 lead flat packages.

PINOUT

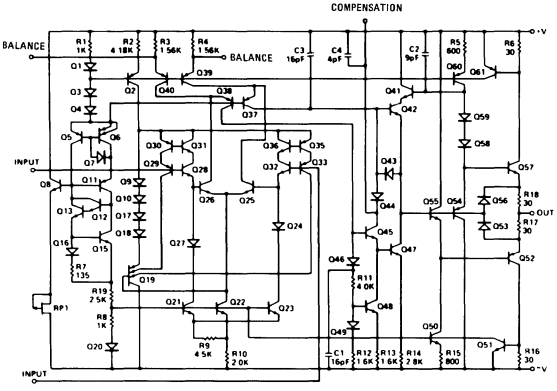
Section 11 for Packaging



Case Connected to V- TOP VIEWS



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Operating Temperature Range – HA-2600/HA-2602	$-55^oC \leq T_A \leq +125^oC$
HA-2605	$0^o \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

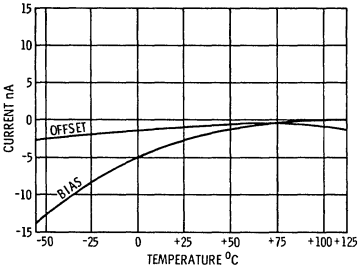
V+ = +15VDC, V- = -15VDC

		HA-2600 −55°C to +125°C LIMITS			HA-2602 −55°C to +125°C LIMITS			HA-2605 0°C to +75°C LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	4		3	5		3	5	mV
	Full		2	6			7			7	mV
Offset Voltage Average Drift	Full		5								µV/°C
Bias Current	+25°C		1	10		15	25		5	25	nA
	Full		10	30			60			40	nA
Offset Current	+25°C		1	10		5	25		5	25	nA
	Full		5	30			60			40	nA
Input Resistance (Note 10)	+25°C	100	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 1, 4)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		74	100		dB
Unity Gain Bandwidth (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Note 4 &11)	+25°C	50	75		50	75		50	75		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		30	60		30	60		30	60	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	40		25	40	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±4	±7		±4	±7		±4	±7		V/µs
Settling Time (Notes 1, 5, 8 & 12)	+25°C		1.5			1.5			1.5		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

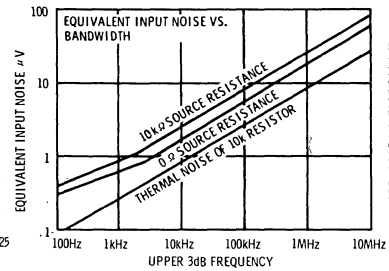
TEST CONDITIONS

NOTES:
1. $R_L = 2K$
2. $V_{CM} = \pm 10V$
3. $V_O < 90mV$
4. $V_O = \pm 10V$
5. $C_L = 100pF$
6. $V_O = \pm 200mV$
7. $V_O = \pm 200mV$
8. See Transient response test circuits and waveforms
9. $\Delta VS = \pm 5V$
10. This parameter value guaranteed by design calculations.
11. Full power bandwidth guaranteed by slew rate measurement. $FPBW = S.R./2\pi V_{peak}$.
12. $V_{OUT} = \pm 5V$

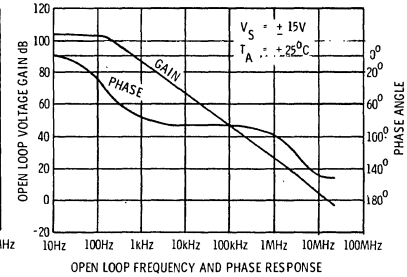
V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.

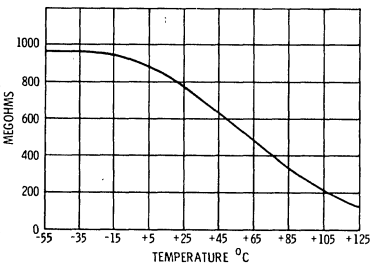


INPUT BIAS CURRENT AND OFFSET CURRENT
AS A FUNCTION OF TEMPERATURE

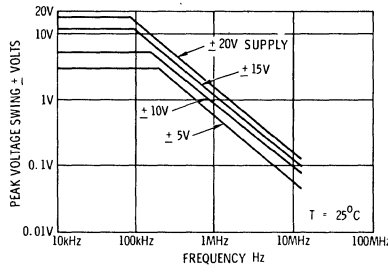


LOWER 3dB FREQUENCY - 10Hz
BROADBAND NOISE CHARACTERISTICS

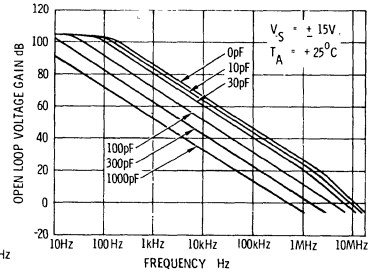




INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

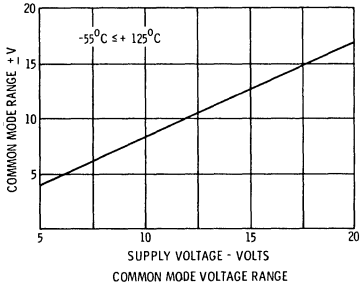


OUTPUT VOLTAGE SWING VS. FREQUENCY

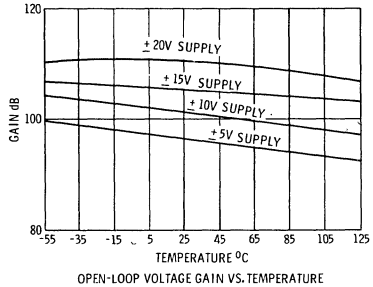


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

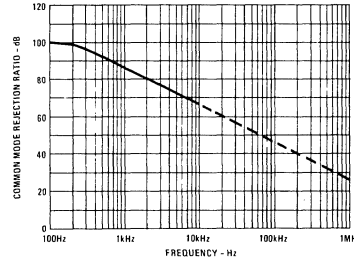
Note External Compensation Components are not Required for Stability, But May be Added to Reduce Bandwidth if Desired If External Compensation is Used, Also Connect 100pF Capacitor From Output to Ground.



COMMON MODE VOLTAGE RANGE
AS A FUNCTION OF SUPPLY VOLTAGE

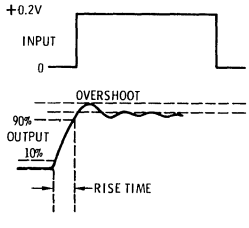


OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE



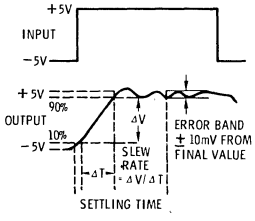
COMMON MODE REJECTION RATIO
VS FREQUENCY

TRANSIENT RESPONSE

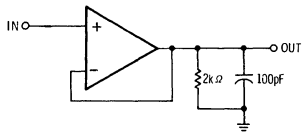


NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

SLEW RATE AND SETTLING TIME



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED VOS ADJUSTMENT

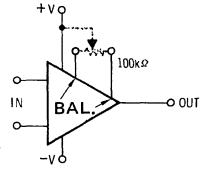
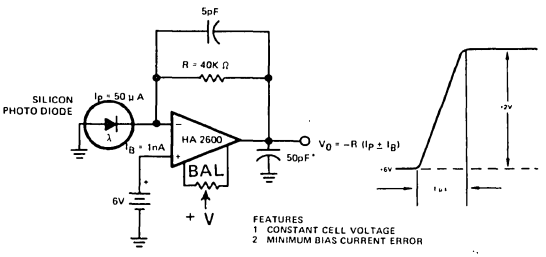
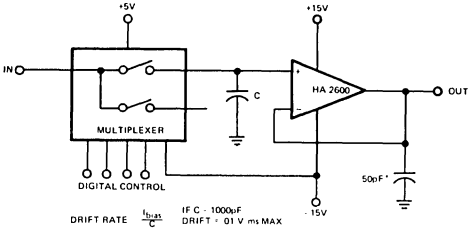


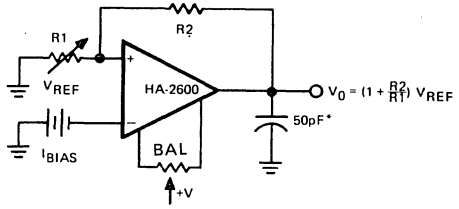
PHOTO-CURRENT TO VOLTAGE CONVERTER



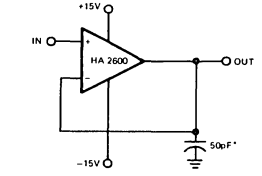
SAMPLE – AND – HOLD



REFERENCE VOLTAGE AMPLIFIER



VOLTAGE FOLLOWER



*A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

HARRIS HA-2620/2622/2625

Very Wide Band, Uncompensated Operational Amplifiers

2

FEATURES

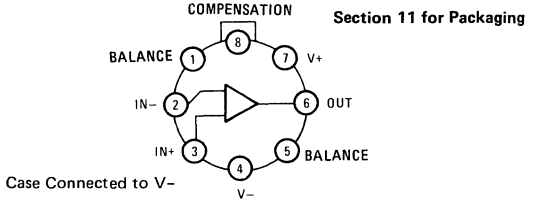
- GAIN BANDWIDTH PRODUCT(A_V = 5) 100MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 0.5mV
- HIGH GAIN 150K V/V
- HIGH SLEW RATE 35V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

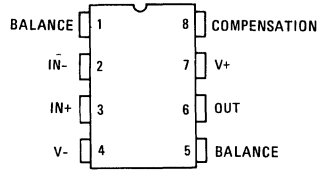
APPLICATIONS

- VIDEO AND R.F. AMPLIFIERS
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

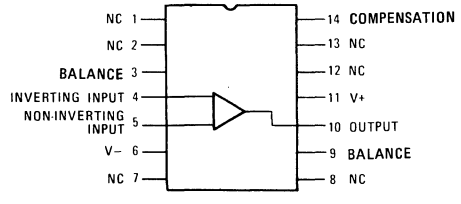
PINOUT

Section 11 for Packaging





TOP VIEWS



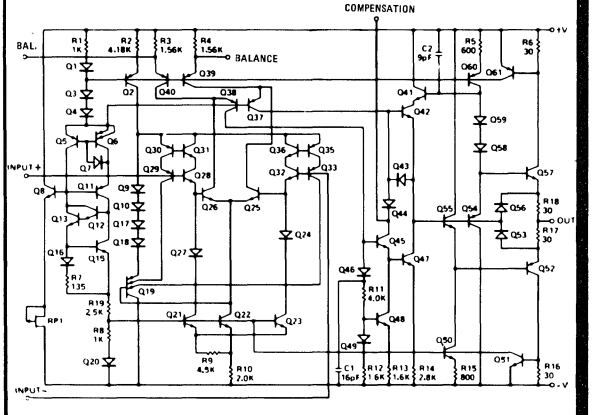
DESCRIPTION

HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 100MHz gain-bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/ μs slew rate and 150,000V/V open-loop gain enables HA-2620/2622/2625 to perform high-gain amplification of very fast, wideband signals. These dynamic characterisitcs, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

HA-2620 and HA-2622 are guaranteed over -55°C to +125°C. HA-2625 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and 14 lead D.I.P. packages.

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

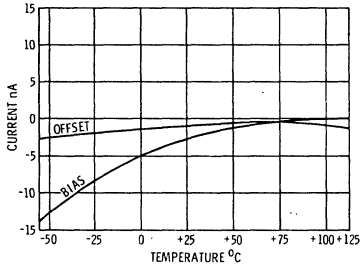
ELECTRICAL CHARACTERISTICS

$V^+ = +15$ VDC, $V^- = -15$ VDC

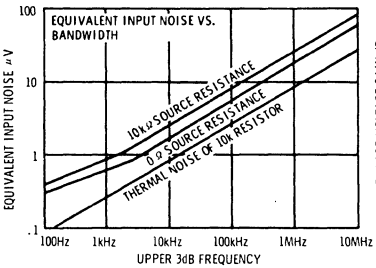
		HA-2620 −55°C to +125°C			HA-2622 −55°C to +125°C			HA-2625 0°C to +75°C			
PARAMETER	TEMPERATURE	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage (Note 1)	+25°C		0.5	4		3	5		3	5	mV
	Full			6			7			7	mV
Bias Current	+25°C		1	15		5	25		5	25	nA
	Full		10	35			60			40	nA
Offset Current	+25°C		1	15		5	25		5	25	nA
	Full		5	35			60			40	nA
Input Resistance (Note 11)	+25°C	65	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 2 & 3)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80	100		74	100		74	100		dB
Gain Bandwidth Product (Notes 2, 5, &6)	+25°C		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 3)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Notes 2, 3, 7 &12)	+25°C	400	600		320	600		320	600		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 2, 7 & 8)	+25°C		17	45		17	45		17	45	ns
Slew Rate (Notes 2, 7, 8 & 10)	+25°C	±25	±35		± 20	±35		± 20	±35		V/µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. Offset may be externally adjusted to zero.
2. $R_L = 2K\Omega$, $C_L = 50pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 10V$
5. $V_O < 90mV$
6. 40dB Gain
7. See transient response test circuits and waveforms
8. $A_V = 5$ (The HA-2620 family is not stable at unity gain without external compensation.)
9. $\Delta V_{Sup} = \pm 5V$
10. $V_{OUT} = \pm 5V$
11. This parameter value based upon design calculations.
12. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./$2\pi V_{peak}$.

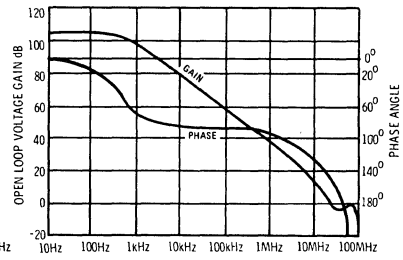
V+ = 15VDC, V- = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED.



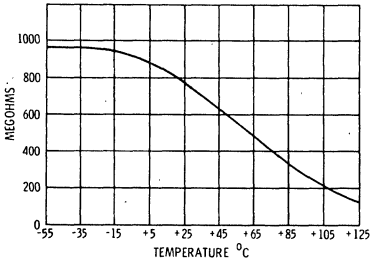
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



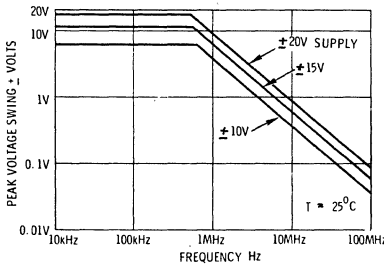
BROADBAND NOISE CHARACTERISTICS



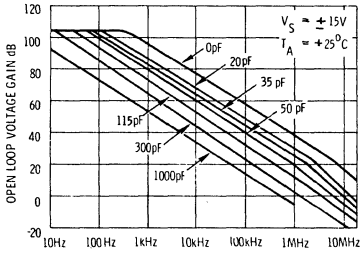
OPEN LOOP FREQUENCY AND PHASE RESPONSE



INPUT IMPEDANCE VS. TEMPERATURE, 100Hz

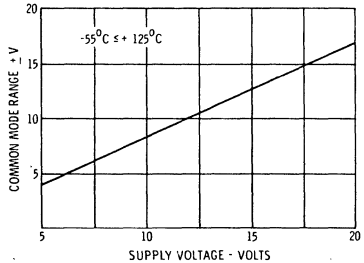


OUTPUT VOLTAGE SWING VS. FREQUENCY

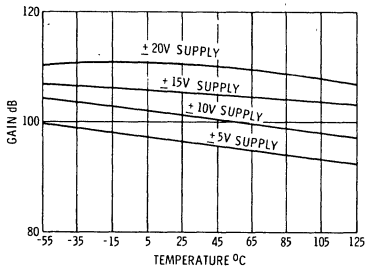


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

Note External Compensation is Required For Closed Loop Gain <5. If External Compensation is Used, Also Connect 100 pF Capacitor From Output to Ground.

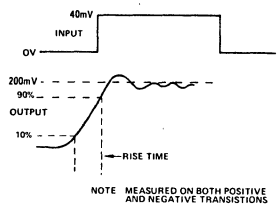


COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

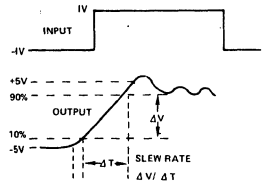


OPEN-LOOP VOLTAGE GAIN VS. TEMPERATURE

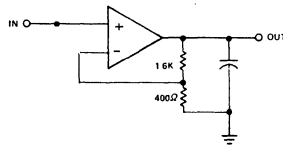
TRANSIENT RESPONSE



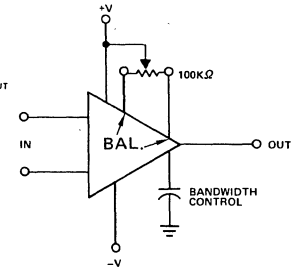
SLEW RATE



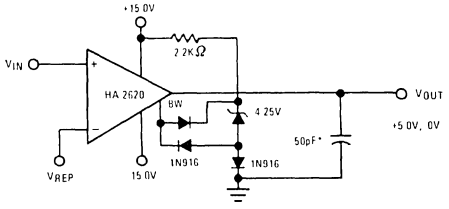
SLEW RATE AND TRANSIENT RESPONSE



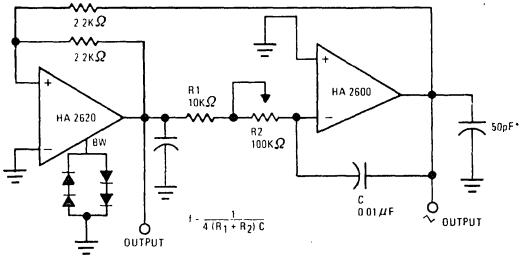
SUGGESTED VOS ADJUSTMENT AND COMPENSATION HOOK-UP



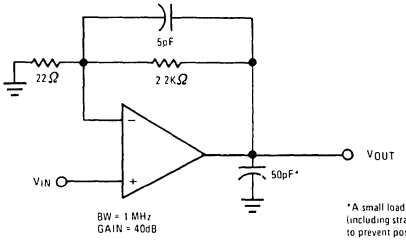
HIGH IMPEDANCE COMPARATOR



FUNCTION GENERATOR



VIDEO AMPLIFIER



*A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations

HARRIS

HA-2630/2635

High Performance Current Booster

2

FEATURES

- OUTPUT CURRENT ±400mA
- SLEW RATE 500V/μs
- BANDWIDTH 8MHz
- FULL POWER BANDWIDTH 8MHz
- INPUT RESISTANCE $2.0 \times 10^6 \Omega$
- OUTPUT RESISTANCE 2.0Ω
- POWER SUPPLY RANGE ±5V to ±20V
- PACKAGE IS ELECTRICALLY ISOLATED

APPLICATIONS

- COAXIAL CABLE DRIVERS
- AUDIO OUTPUT AMPLIFIERS
- SERVO MOTOR DRIVERS
- POWER SUPPLIES (BIPOLAR)
- PRECISION DATA RECORDING

DESCRIPTION

HA-2630 and HA-2635 are monolithic, unity voltage gain current amplifiers delivering extremely high slew rate, wide bandwidth, and full power bandwidth even under heavy output loading conditions. This dielectrically isolated current booster also offers high input impedance and low output resistance. These devices are intended to be used in series with an operational amplifier and inside the feedback loop whenever additional output current is required. Output current levels are programmable by selecting two optional external resistors.

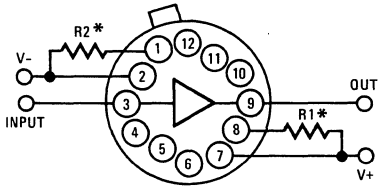
These current amplifiers offer an exceptional 500V/μs slew rate and 8MHz bandwidth which allows them to be used with many high performance op amps in precision data recording and high speed coaxial cable driver designs. 2.0M ohm input resistance and 2 ohm output resistance coupled with ±400mA output current make HA-2630 and HA-2635 ideal components in high fidelity audio output amplifier designs.

HA-2630 and HA-2635 are available in an electrically isolated TO-8 type can for ease of mounting with or without a heat sink. HA-2630 is specified over the -55°C to +125°C range. HA-2635 is specified from 0°C to +75°C.

PINOUT

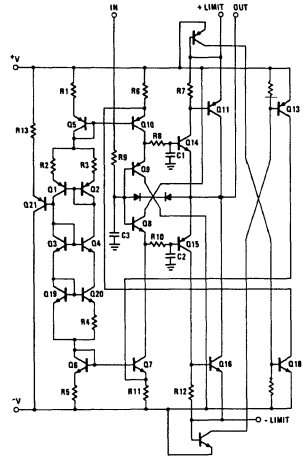
Section 11 for Packaging

TOP VIEW



* Optional Current Limiting Resistor

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V
Input Voltage Range	± V Supply
Output Current (Note 2)	±700mA
Internal Power Dissipation (Note 6) Free Air:	1W
In Heat Sink:	4W

Operating Temperature Range:
$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2630)
$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2635)

Storage Temperature Range:
$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

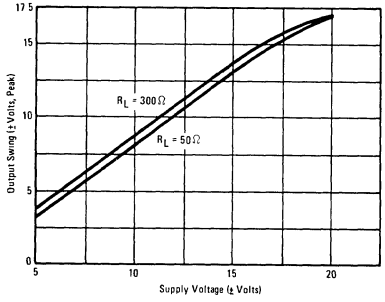
$V_{Supply} = \pm 15$ Volts $R_L = 50$ Ohms $R_1 = R_2 = 0$ Ohms Unless otherwise specified.

		HA-2630 -55°C to +125°C			HA-2635 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Bias Current	+25°C		30	150		30	150	µA
	Full			200			200	µA
Input Resistance	+25°C		2.0			2.0		MΩ
Input Capacitance	+25°C		5.0			5.0		pF
TRANSFER CHARACTERISTICS								
Voltage Gain (Note 1)	Full	.85	.95		.85	.95		V/V
Offset Voltage ($V_{OUT} - V_{IN}$)	+25°C		70	±200		70	±200	mV
	Full			±300			±300	mV
Bandwidth (-3dB)	+25°C		8.0			8.0		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10	±12		±10	±12		V
Output Current (Note 1)	Full	±300	±400		±300	±400		mA
Output Resistance	+25°C		2.0			2.0		Ω
Full Power Bandwidth (Note 1)	+25°C		8.0			8.0		MHz
TRANSIENT RESPONSE								
Rise Time (Note 3)	+25°C		30			30		ns
Slew Rate (Note 4)	+25°C	200	500		200	500		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		15	20		15	23	mA
Supply Voltage Range	Full	±5		±20	±5		±20	V
Power Supply Rejection Ratio (Note 5)	Full		66			66		dB

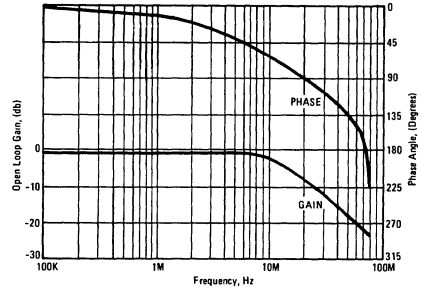
NOTES:
1. $V_O = \pm 10V$
2. Heat sink is required for continuous short circuit protection, regardless of current limit setting.
3. $V_O = 0.4V$ p-p.
4. $V_O = 10V$ p-p.
5. $\Delta V_{SUPPLY} = \pm 5V$.
6. Without heat sink, derate by 14mW/°C ambient temperature above 100°C ambient, with heat sink, derate by 67mW/°C case temperature above 115°C case.

V+ = 15VDC, V– = 15VDC, T_A = 25°C UNLESS OTHERWISE STATED

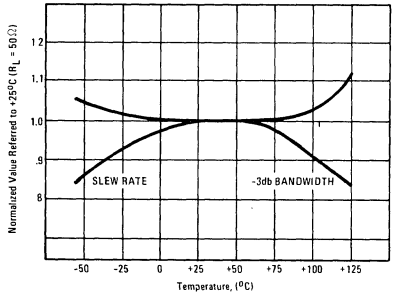
OUTPUT SWING
(R_{LIMIT} = 0Ω)



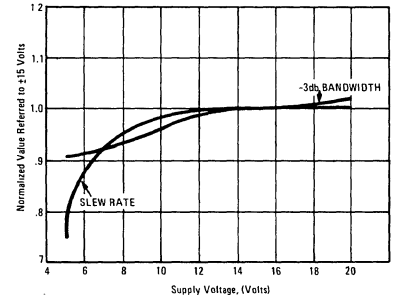
OPEN LOOP FREQUENCY AND
PHASE RESPONSE (R_L = 50Ω, C_L ≈ 10pf)



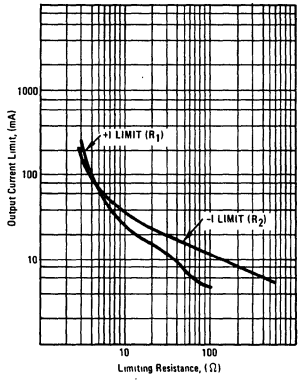
NORMALIZED AC PARAMETERS vs.
TEMPERATURE (R_L = 50Ω)



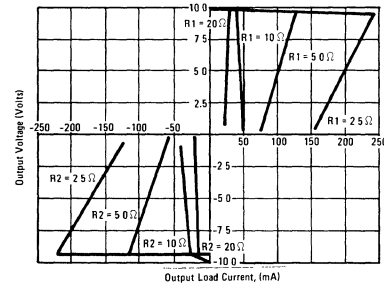
NORMALIZED AC PARAMETERS vs.
SUPPLY VOLTAGE (R_L = 50Ω)



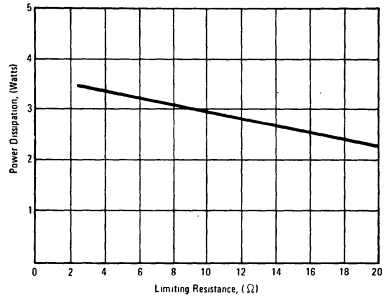
OUTPUT CURRENT LIMITING vs.
LIMITING RESISTANCE



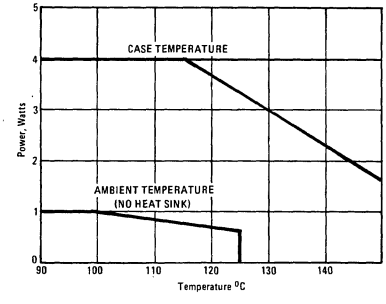
OUTPUT CURRENT CHARACTERISTIC



POWER DISSIPATION vs. LIMITING RESISTANCE
WITH OUTPUT SHORTED TO GROUND; V_{IN} = +10V

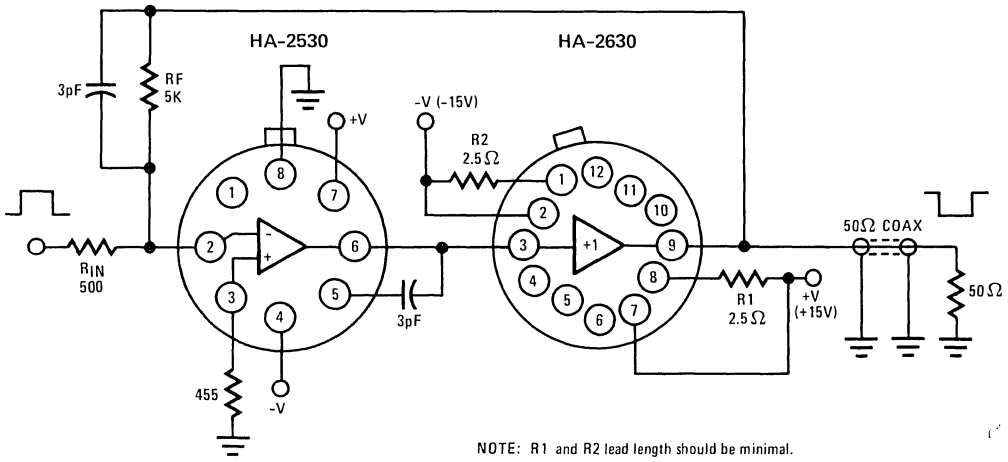


MAXIMUM ALLOWABLE INTERNAL
POWER DISSIPATION vs. TEMPERATURE



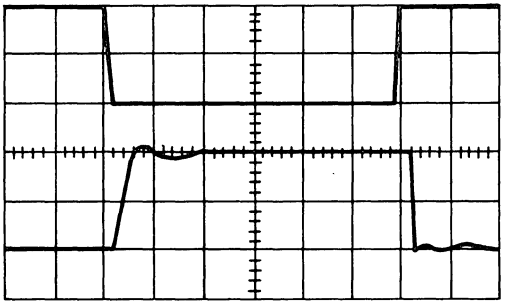
TYPICAL APPLICATION

20dB, 5MHz VIDEO COAXIAL LINE DRIVER



NOTE: R1 and R2 lead length should be minimal.

LINE DRIVER PULSE RESPONSE



Horizontal Scale = 200ns/Div.
Upper Trace: Input, 200mV/Div.
Lower Trace: Output, 2V/Div.

SOME OTHER APPLICATIONS

- BIPOLAR POWER SUPPLY
- FUNCTION GENERATOR OUTPUT
- DEFLECTION COIL DRIVE
- AUDIO OUTPUT AMPLIFIER

HARRIS

HA-2640/2645

High Voltage Operational Amplifier

2

FEATURES

- OUTPUT VOLTAGE SWING ±35V
- SUPPLY VOLTAGE ±10V TO ±40V
- OFFSET CURRENT 5nA
- BANDWIDTH 4MHz
- SLEW RATE 5V/μs
- COMMON MODE INPUT VOLTAGE SWING ±35V
- OUTPUT OVERLOAD PROTECTION

APPLICATIONS

- INDUSTRIAL CONTROL SYSTEMS
- POWER SUPPLIES
- HIGH VOLTAGE REGULATORS
- RESOLVER EXCITATION
- SIGNAL CONDITIONING

DESCRIPTION

HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

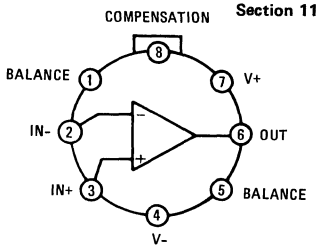
For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

These amplifers deliver ±35V common mode input voltage swing, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and 5V/μs slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excellent components for resolver excitation designs.

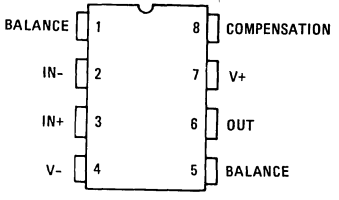
HA-2640 and HA-2645 are available in metal can (TO-99) packages and can be used as high performance pin-to-pin replacements for many general purpose op amps. HA-2640 is specified from -55°C to +125°C and HA-2645 is specified over the 0°C to +75°C range.

PINOUT

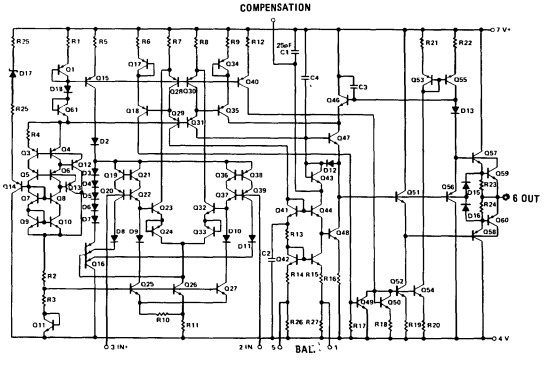
Section 11 for Packaging



TOP VIEWS



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals 100V
Input Voltage Range ±37V
Output Current/Full Short Circuit Protection
Internal Power Dissipation 680mW*

*Derate by 4.6mW/°C above +25°C

Operating Temperature Range
$-55^{\circ}C \leq T_A \leq +125^{\circ}C$ (HA-2640)
$0^{\circ}C \leq T_A \leq +75^{\circ}C$ (HA-2645)
Storage Temperature Range
$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS

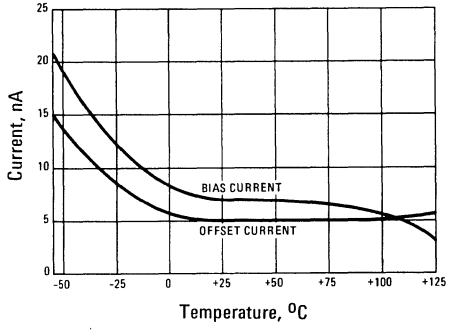
$V_{Supply} = \pm 40V$, $R_L = 5K$, Unless Otherwise Specified.

PARAMETER	TEMP.	HA-2640 -55°C to +125°C MIN.	HA-2640 -55°C to +125°C TYP.	HA-2640 -55°C to +125°C MAX.	HA-2645 0°C to +75°C MIN.	HA-2645 0°C to +75°C TYP.	HA-2645 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		2	4		2	6	mV
	Full			6			7	mV
Offset Voltage Average Drift	Full		15			15		µV/°C
Bias Current	+25°C		10	25		12	30	nA
	Full			50			50	nA
Offset Current	+25°C		5	12		15	30	nA
	Full			35			50	nA
Input Resistance **(Note 10)**	+25°C	50	250		40	200		MΩ
Common Mode Range	Full	±35			±35			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain **(Note 8)**	+25°C	100K	200K		100K	200K		V/V
	Full	75K			75K			V/V
Common Mode Rejection Ratio (Note 1)	Full	80	100		74	100		dB
Unity Gain Bandwidth (Note 2)	+25°C		4			4		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±35			±35			V
Output Current (Note 9)	+25°C	±12	±15		±10	±12		mA
Output Resistance	+25°C		500			500		Ω
Full Power Bandwidth **(Notes 3 &11)**	+25°C		23			23		kHz
TRANSIENT RESPONSE (Note 7)								
Rise Time (Notes 4, 6)	+25°C		60	**100**		60	**100**	ns
Overshoot (Notes 4, 6)	+25°C		15	**30**		15	**40**	%
Slew Rate (Note 6)	+25°C	**±3**	±5		**±2.5**	±5		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.2	3.8		3.2	4.5	mA
Supply Voltage Range	Full	±10		±40	±10		±40	V
Power Supply Rejection Ratio (Note 5)	Full	80	90		74	90		dB

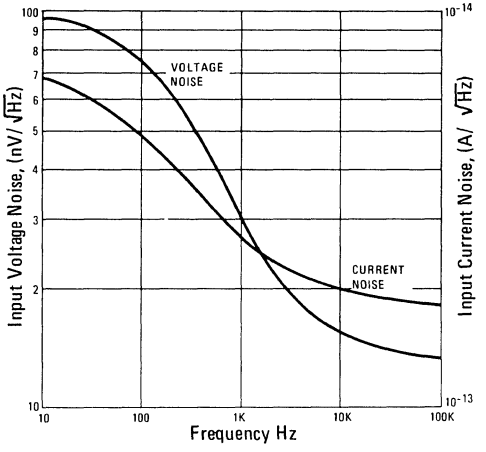
NOTES:
1. $V_{CM} = \pm 20V$
2. $V_O = 90mV$
3. $V_O = \pm 35V$
4. $V_O = \pm 200mV$
5. $V_S = \pm 10V$ to $\pm 40V$
6. $A_V = 1$
7. $C_L = 50pF$
8. $V_O = \pm 30V$
9. $R_L = 1K$
10. This parameter based upon design calculations.
11. Full power bandwidth guaranteed based upon slew rate measurement. FPBW = S.R./$2\pi V_{peak}$.

V+ = V- = 40VDC, T_A = +25°C UNLESS OTHERWISE STATED

INPUT BIAS AND OFFSET CURRENT vs TEMPERATURE

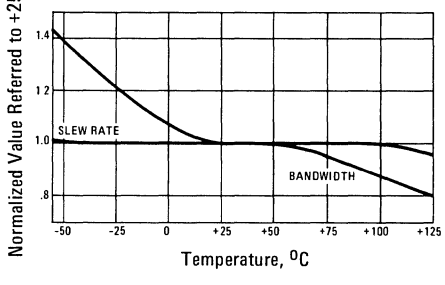


INPUT NOISE CHARACTERISTICS

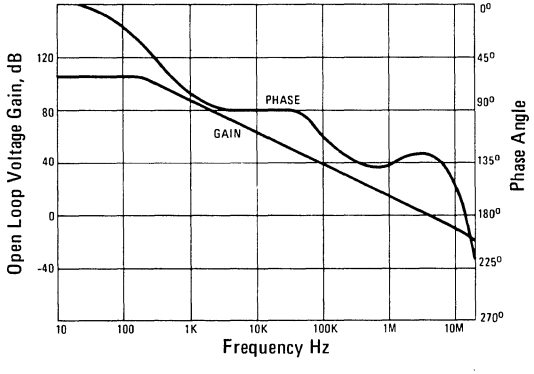


2

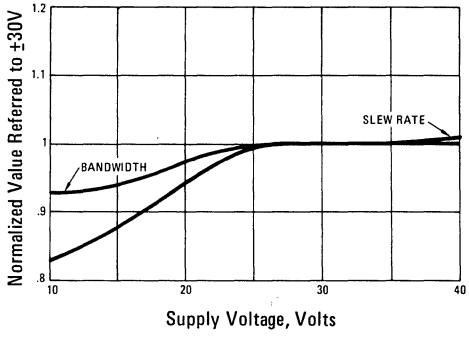
NORMALIZED AC PARAMETERS vs TEMPERATURE



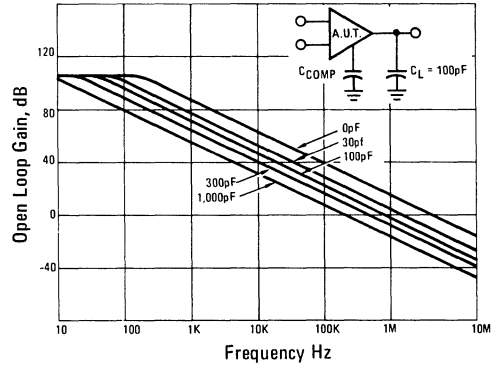
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE AT +25°C



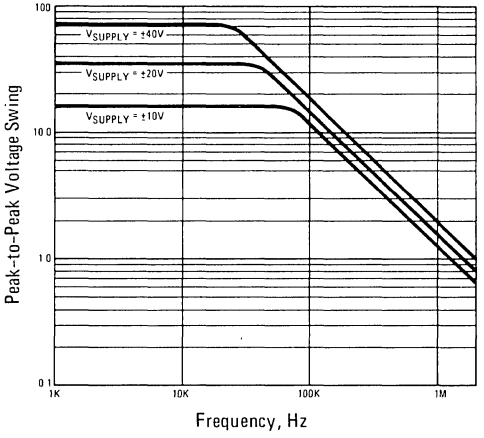
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND



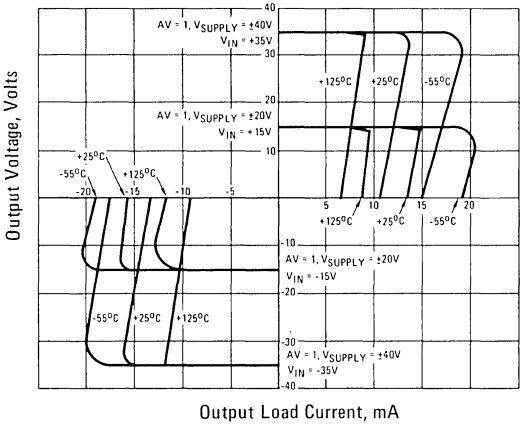
NOTE: External Compensation Components are not Required for Stability. But May be Added to Reduce Bandwidth if Desided. C_L = 100pF is Also Required for Stability Only if External Compensation Capacitor is Used.

PERFORMANCE CURVES (continued)

OUTPUT VOLTAGE SWING
vs FREQUENCY AT +25°C

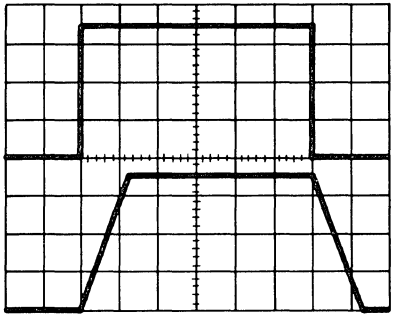


OUTPUT CURRENT CHARACTERISTIC



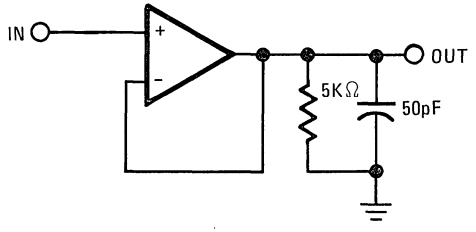
SWITCHING WAVEFORM AND TEST CIRCUIT

VOLTAGE FOLLOWER
PULSE RESPONSE

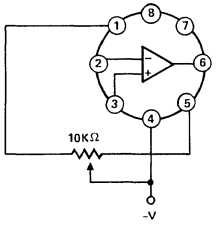


R_L = 5K, C_L = 50pF
Vertical = 10V/Div. T_A = +25°C
Horizontal = 5µs/Div. V_S = ±40V

SLEW RATE AND TRANSIENT
RESPONSE TEST CIRCUIT



SUGGESTED VOS ADJUSTMENT



HARRIS

HA-2650/2655

Dual High Performance Operational Amplifier

2

FEATURES

- SLEW RATE — 5V/μs
- BANDWIDTH — 8MHz
- BIAS CURRENT — 35nA
- AV. OFFSET VOLTAGE DRIFT — 8μV/°C
- POWER CONSUMPTION — 75mW
- SUPPLY VOLTAGE RANGE — ±2V TO ±20V

APPLICATIONS

- VIDEO AMPLIFIERS
- HIGH IMPEDANCE, WIDEBAND BUFFERS
- INTEGRATORS
- AUDIO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

HA-2650/2655 contains two internally compensated operational amplifiers offering high slew rate and high frequency performance combined with exceptional DC characteristics. 5V/μ sec slew rate and 8MHz bandwidth make these amplifiers suitable for processing fast, wideband signals extending into the video frequency spectrum. Signal processing accuracy is enhanced by front-end performance that includes 1.5mV offset voltage, 8 μ V/°C offset voltage drift and low offset and bias current (1nA and 35nA respectively). Offset voltage can be trimmed to zero on the devices offered in dual-in-line packages. Signal conditioning is further enhanced by 500MΩ input impedance.

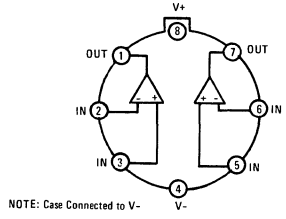
Applications for HA-2650/2655 include video circuit designs such as high impedance buffers, integrators, tone generators and filters. These amplifiers are also ideal components for active filtering of audio and voice signals.

HA-2650/2655 are offered in 14 pin D.I.P. and metal TO-99 packages and are also available in dice form. HA-2650 is specified from -55°C to +125°C. HA-2655 operates from 0°C to +75°C.

PINOUT

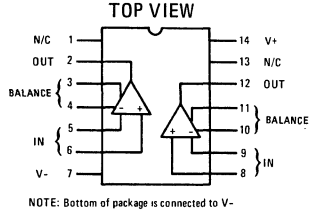
TOP VIEW

Section 11 for Packaging



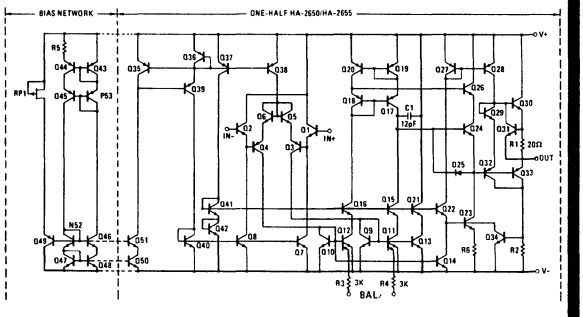
NOTE: Case Connected to V-

TOP VIEW



NOTE: Bottom of package is connected to V-

SCHEMATIC



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration	Indefinite

Power Dissipation (Note 2)	TO-99	300 mW
	TO-116	300 mW
Operating Temperature Range:		
HA-2650	-55°C ≤ T_A ≤ +125°C	
HA-2655	0°C ≤ T_A ≤ +75°C	
Storage Temperature Range	-65°C ≤ T_A ≤ +150°C	

ELECTRICAL CHARACTERISTICS

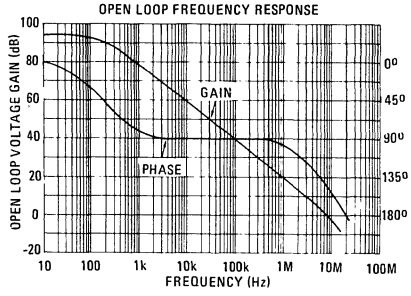
V+ = 15V V- = -15V

PARAMETER	TEMP.	HA-2650 -55°C to +125°C MIN.	HA-2650 TYP.	HA-2650 MAX.	HA-2655 0°C to +75°C MIN.	HA-2655 TYP.	HA-2655 MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		1.5	3		2	5	mV
	Full			5			7	mV
Av. Offset Voltage Drift	Full		8			8		µV/°C
Bias Current	+25°C		35	100		50	200	nA
	Full			200			300	nA
Offset Current	+25°C		1	30		2	60	nA
	Full			60			100	nA
Common Mode Range	Full	±13			±13			V
Differential Input Resistance (Note 9)	+25°C	5	20		5	20		MΩ
Common Mode Input Resistance	+25°C		500			500		MΩ
Input Capacitance	+25°C		5			5		pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3ab)	+25°C	20K	40K		15K	40K		V/V
	Full	15K			10K			V/V
Common Mode Rejection Ratio (Note 4)	+25°C	80	100		74	100		dB
	Full	80			74			dB
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 3c)	+25°C	±13	±14		±13	±14		V
	Full	±13			±13			V
Full Power Bandwidth (Notes 5 &10)	+25°C	30	80		30	80		KHz
Output Current (Note 3a)	+25°C		±20			±18		mA
Output Resistance	+25°C		100			100		Ω
TRANSIENT RESPONSE (Note 6)								
Rise Time (Note 7)	+25°C		40	80		40	90	ns
Overshoot (Note 7)	+25°C		15	30		15	40	%
Slew Rate	+25°C	±2	±5		±2	±5		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		2.5	4		3	5	mA
Power Supply Rejection Ratio (Note 8)	+25°C	80	100		74	100		dB
	Full	80			74			dB

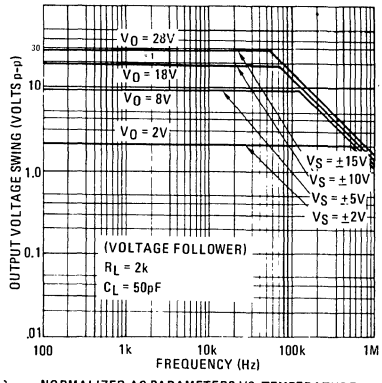
NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above +110°C.
3. (a) V_O = ±10V (b) R_L = 2K (c) R_L = 10K
4. V_{CM} = ±5.0V
5. A_V = 1, R_L = 2K, V_O = 20V_{pp}
6. See transient response/slew rate circuit.
7. V_{in} = 200mV
8. Δ V = ±5.0V
9. This parameter value based upon design calculations.
10. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./2πV_{peak}.

V+ = +15V, V- = -15V, T_A = +25°C unless otherwise stated.

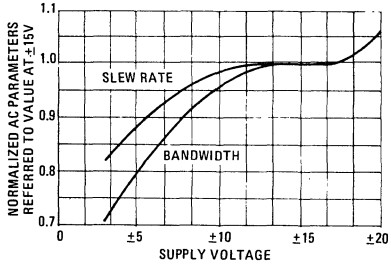
OPEN LOOP FREQUENCY RESPONSE



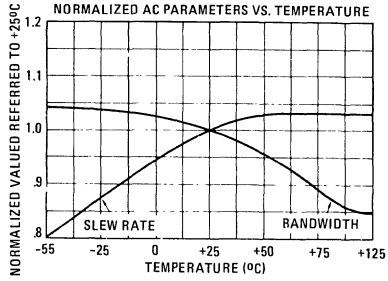
OUTPUT VOLTAGE SWING VS. FREQUENCY



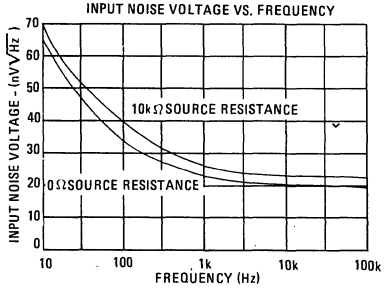
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



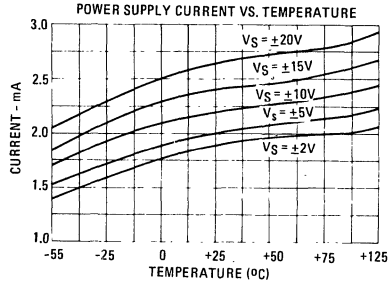
NORMALIZED AC PARAMETERS VS. TEMPERATURE



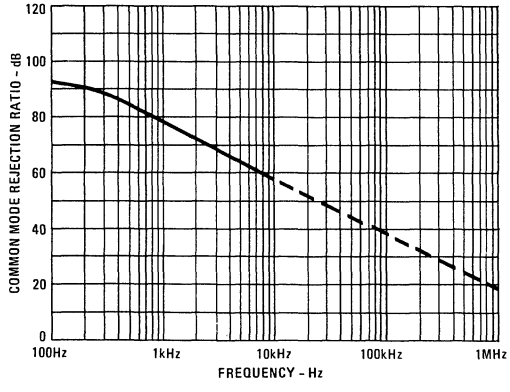
INPUT NOISE VOLTAGE VS. FREQUENCY



POWER SUPPLY CURRENT VS. TEMPERATURE

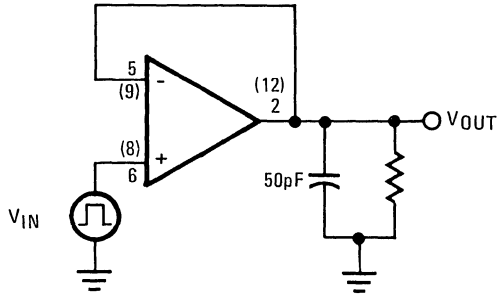


COMMON MODE REJECTION RATIO VS. FREQUENCY



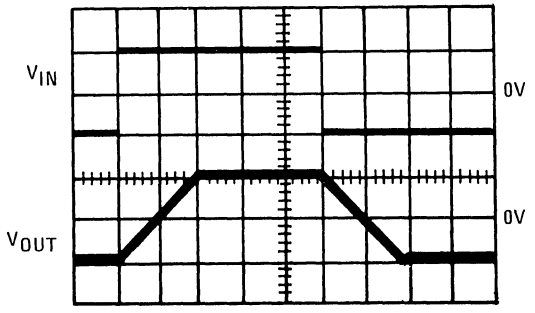
PERFORMANCE CHARACTERISTICS

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



Note: Numbers in parentheses refer to the second half of TO-116 package.

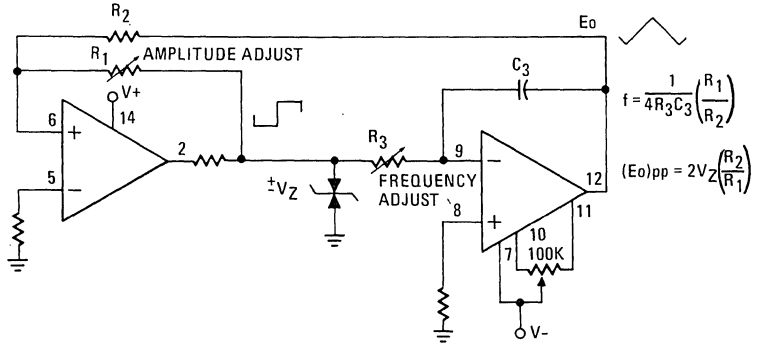
SLEWING WAVEFORM



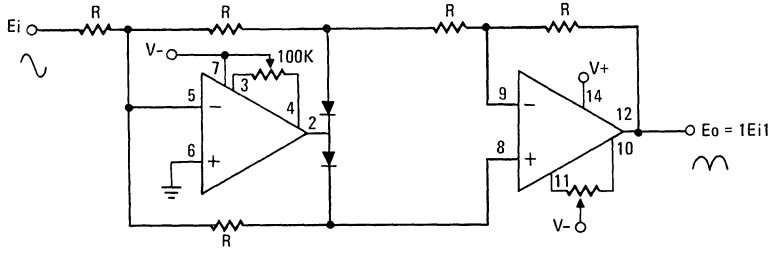
VERTICAL 5V/DIV. HORIZONTAL 1μs/DIV.

TYPICAL APPLICATIONS

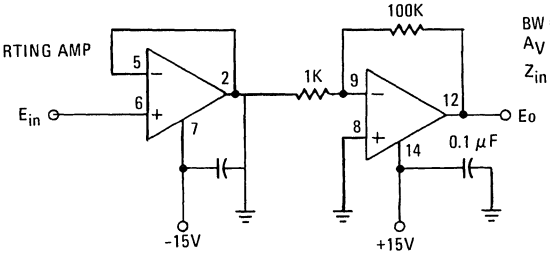
LOW COST HIGH FREQUENCY GENERATOR



ABSOLUTE-VALUE CIRCUIT



HIGH IMPEDANCE
HIGH GAIN
HIGH FREQUENCY INVERTING AMP



BW = 100KHz
A_V = 100
Z_{in} = 2 x $10^9 \Omega$

HARRIS

HA-2720/25

Wide Range Programmable Operational Amplifier

2

FEATURES

- WIDE PROGRAMMING RANGE

SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

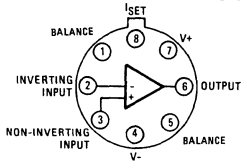
HA-2720/2725 programmable amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables HA-2720/2725 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2720 and HA-2725 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

A major advantage of HA-2720/2725 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipment. A primary application for HA-2720/2725 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2720/2725 can be used for designs such as current controlled oscillators modulators, sample and hold circuits and variable active filters.

HA-2720 is guaranteed over -55°C to +125°C. HA-2725 is specified from 0°C to +75°C. Both parts are available in TO-99 cans or dice form.

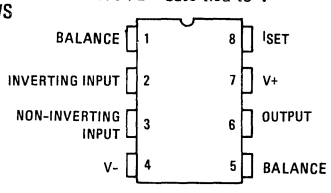
PINOUT

Section 11 for Packaging

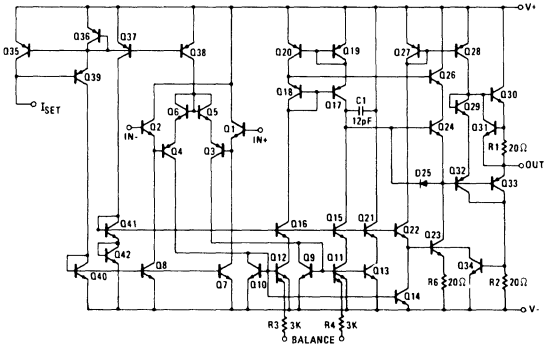


NOTE: Case tied to V⁻

TOP VIEWS



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	300mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2720	$-55^{o}C \leq T_A \leq +125^{o}C$
I_{SET} (Current at I_{SET})	500μA	HA-2725	$0^{o}C \leq T_A \leq +75^{o}C$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

V+ = +3.0V, V- = -3.0V

		HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 9)	25°C	15K	40K		15K	40K		15K	40K		15K	40K		V/V
	Full	10K			10K			10K			10K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		15			170			15			170		μA
	Full			25			250			25			250	μA
Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

ELECTRICAL CHARACTERISTICS

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	30K	100K		30K	120K		25K	100K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		20			210			20			210		μA
	Full			50			450			50			450	μA
Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

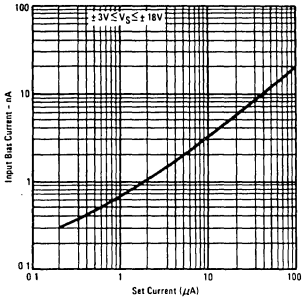
NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 6.8mW/°C for operation ambient temperatures above 75°C.

	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	R_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

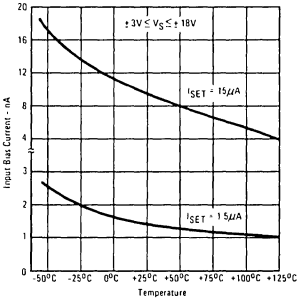
10. This parameter based upon design calculations.

UNLESS OTHERWISE NOTED: $T_A = +25^0C$, $V_S = \pm 15VDC$

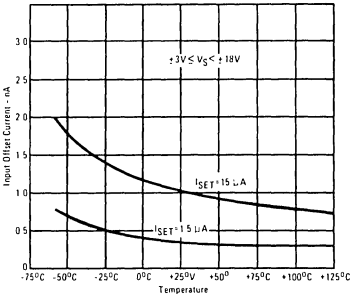
INPUT BIAS CURRENT
vs. SET CURRENT



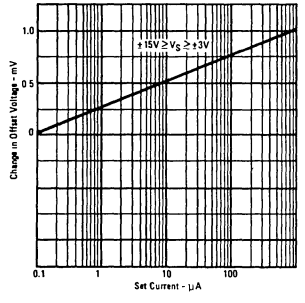
INPUT BIAS CURRENT
vs. TEMPERATURE



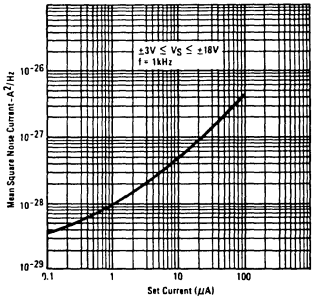
INPUT OFFSET CURRENT
vs. TEMPERATURE



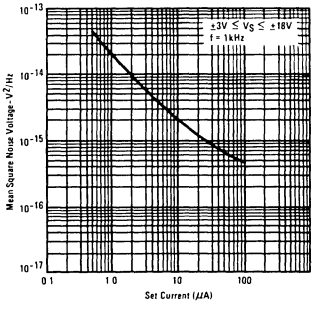
CHANGE IN OFFSET VOLTAGE
vs. I_{SET} (UNNULLED)



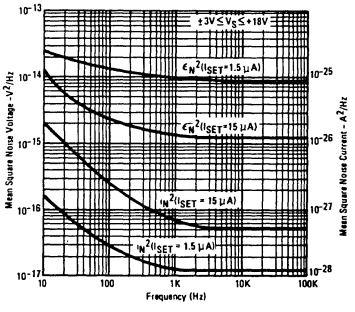
INPUT NOISE CURRENT
vs. I_{SET}



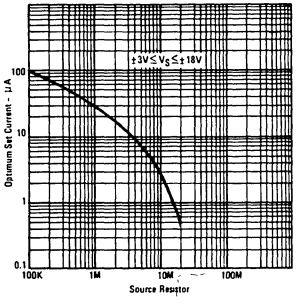
INPUT NOISE VOLTAGE
vs. I_{SET}



INPUT NOISE VOLTAGE AND CURRENT
vs. FREQUENCY



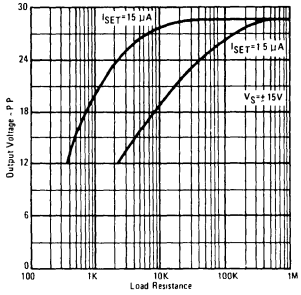
OPTIMUM SET CURRENT FOR MINIMUM
NOISE vs. SOURCE RESISTOR



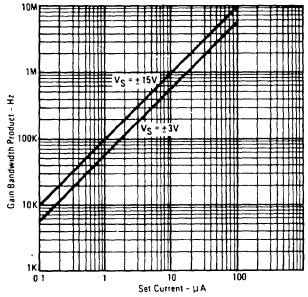
2

UNLESS OTHERWISE NOTED: $T_A = +25^0C$, $V_S = \pm 15VDC$

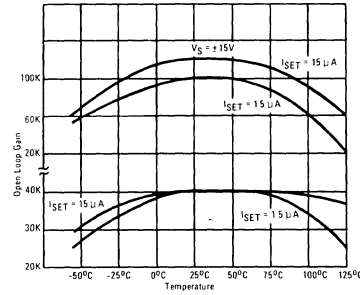
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



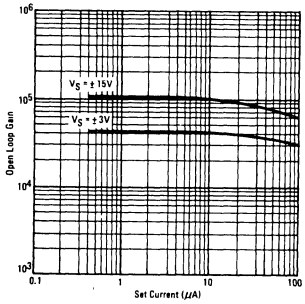
GAIN BANDWIDTH PRODUCT vs. I_{SET}



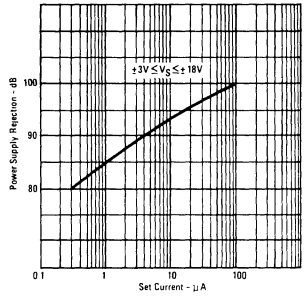
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



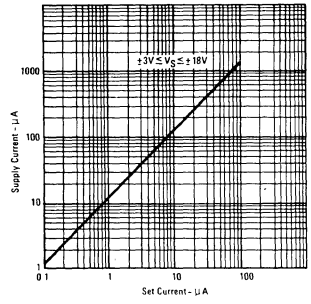
OPEN LOOP VOLTAGE GAIN vs. I_{SET}



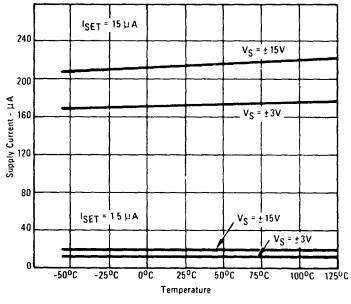
POWER SUPPLY REJECTION vs. I_{SET}



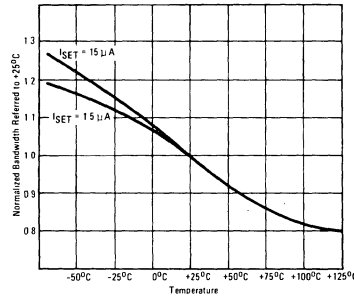
STANDBY SUPPLY CURRENT vs. I_{SET}



SUPPLY CURRENT vs. TEMPERATURE

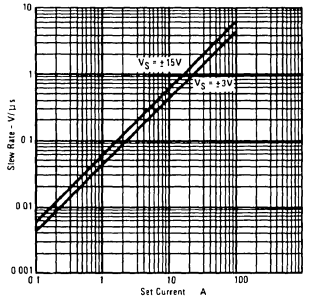


NORMALIZED BANDWIDTH vs. TEMPERATURE

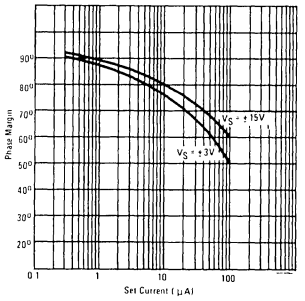


PERFORMANCE CURVES

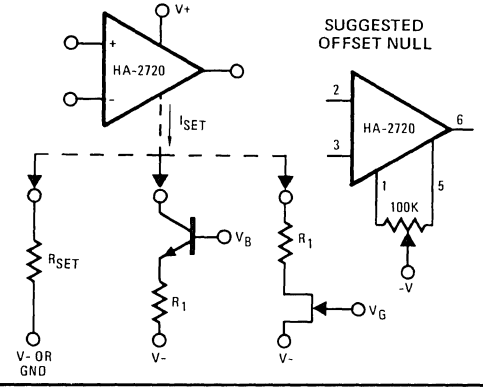
SLEW RATE vs. I_{SET}



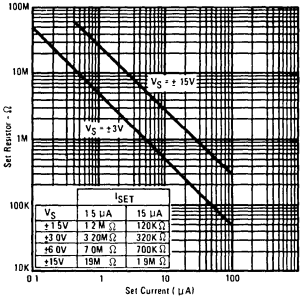
PHASE MARGIN vs. SET CURRENT



TYPICAL BIASING CIRCUITS

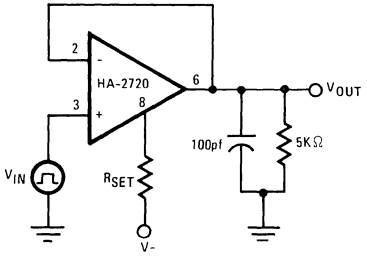


SET CURRENT VS. SET RESISTOR

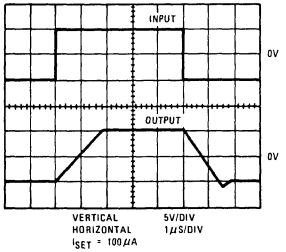


V_S	I_{SET} 1.5 µA	15 µA
±15V	12M Ω	120KΩ
±3.0V	3.20M Ω	320K Ω
±6.0V	7.0M Ω	700K Ω
+15V	19M Ω	1.9M Ω

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEWING WAVEFORM



HARRIS

HA-2730/35

Wide Range Dual Programmable Operational Amplifier

2

FEATURES

- WIDE PROGRAMMING RANGE

SET CURRENT	0.1 TO 100μA
SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2730/2735 Dual Programmable Amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. Each amplifier on the chip can be adjusted independently. This versatile adjustment capability enables HA-2730/2735 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2730/2735 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

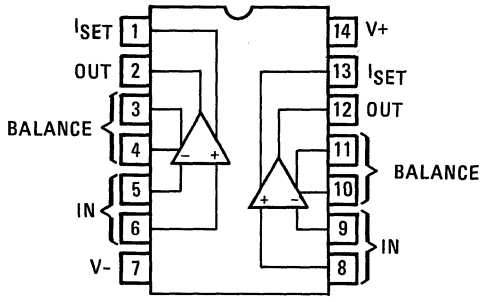
A major advantage of HA-2730/2735 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipement. A primary application for HA-2730/2735 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2730/2735 can be used for designs such as current controlled oscillators, modulators, sample and hold circuits and variable active filters.

HA-2730 is guaranteed over -55°C to +125°C. HA-2735 is specified from 0°C to +75°C. Both parts are available in 14 lead D.I.P. package or dice form.

PINOUT

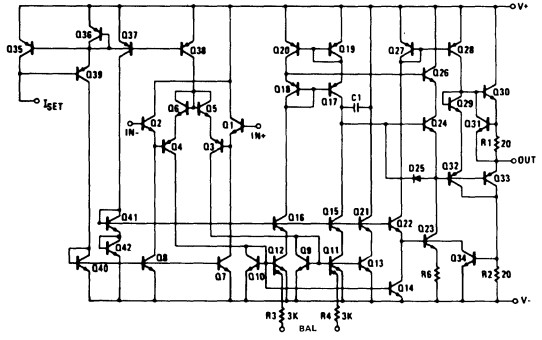
Section 11 for Packaging

TOP VIEW



NOTE: Bottom of package is connected to V-.

SCHEMATIC



(ONE HALF ONLY)
HA-2730/35

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	500mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2730	$-55^{o}C \leq T_A \leq +125^{o}C$
I_{SET} (Current at I_{SET})	500μA	HA-2735	$0^{o}C \leq T_A \leq +75^{o}C$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +3.0V, V- = -3.0V

		HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	15K	40K		15K	40K		15K	40K		15K	40K		V/V
	Full	10K			10K			10K			10K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current (Each Amp)	25°C		15			170			15			170		μA
	Full			25			250			25			250	μA
Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Notes 3 & 9)	25°C	30K	100K		30K	120K		25K	100K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current (Each Amp)	25°C		20			210			20			210		μA
	Full			50			450			50			450	μA
Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

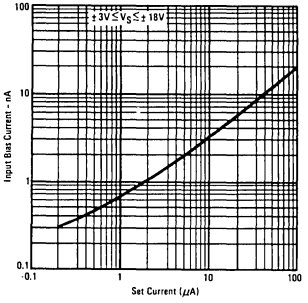
NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above 68°C.

	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	R_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

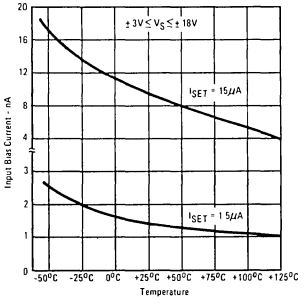
10. This parameter value based upon design calculations.

UNLESS OTHERWISE NOTED: $T_A = 25^0C$, $V_S = \pm 15VDC$

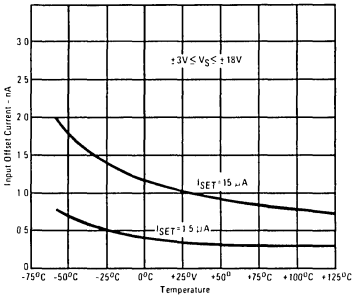
INPUT BIAS CURRENT
vs. SET CURRENT



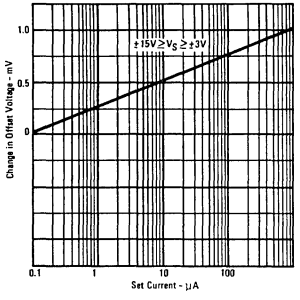
INPUT BIAS CURRENT
vs. TEMPERATURE



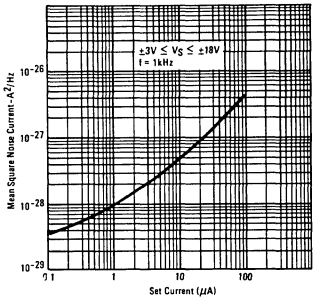
INPUT OFFSET CURRENT
vs. TEMPERATURE



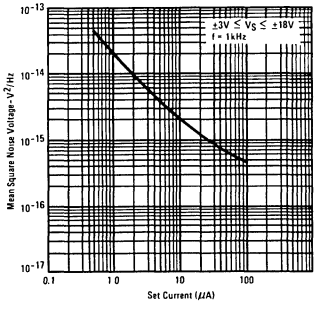
CHANGE IN OFFSET VOLTAGE
vs. I_{SET} (UNNULLED)



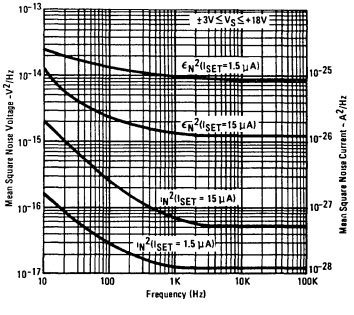
INPUT NOISE CURRENT
vs. I_{SET}



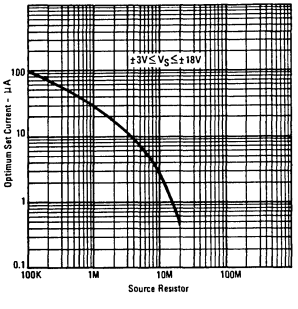
INPUT NOISE VOLTAGE
vs. I_{SET}



INPUT NOISE VOLTAGE AND CURRENT
vs. FREQUENCY



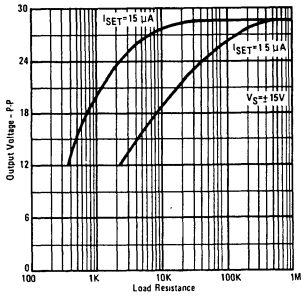
OPTIMUM SET CURRENT FOR MINIMUM
NOISE vs. SOURCE RESISTOR



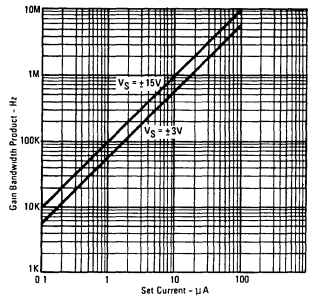
2

UNLESS OTHERWISE NOTED: $T_A = 25^0C$, $V_S = \pm 15VDC$

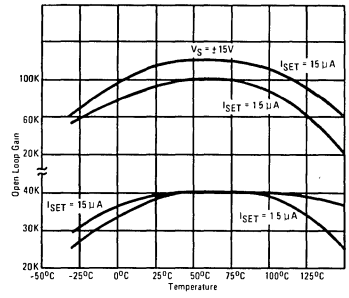
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



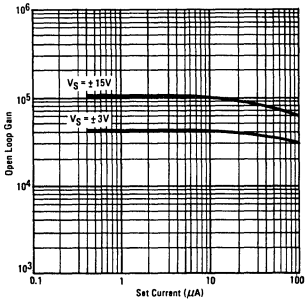
GAIN BANDWIDTH PRODUCT vs. I_{SET}



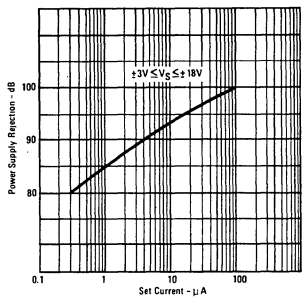
OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE



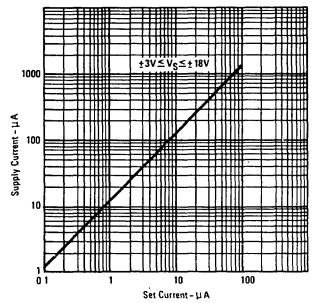
OPEN LOOP VOLTAGE GAIN vs. I_{SET}



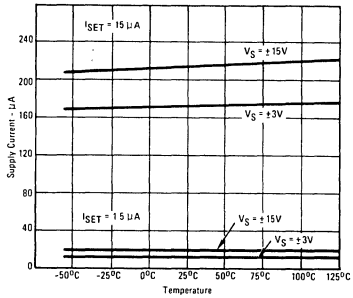
POWER SUPPLY REJECTION vs. I_{SET}



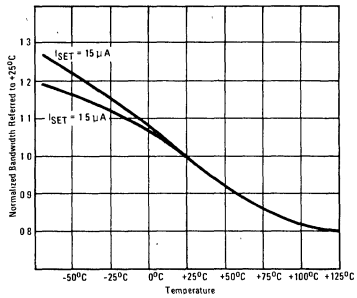
STANDBY SUPPLY CURRENT vs. I_{SET}



SUPPLY CURRENT vs. TEMPERATURE

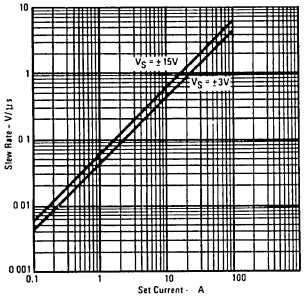


NORMALIZED BANDWIDTH vs. TEMPERATURE

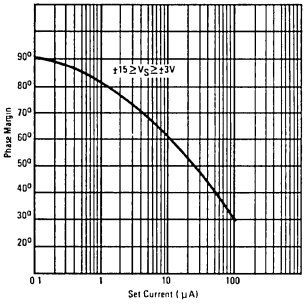


PERFORMANCE CURVES

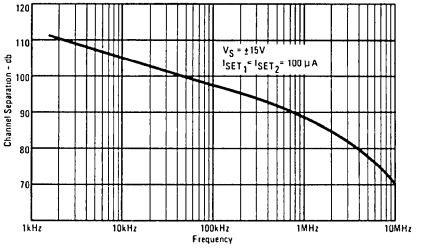
SLEW RATE vs. I_{SET}



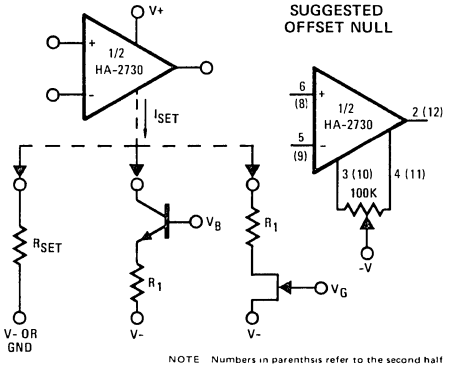
PHASE MARGIN vs. SET CURRENT



CHANNEL SEPARATION vs. FREQUENCY



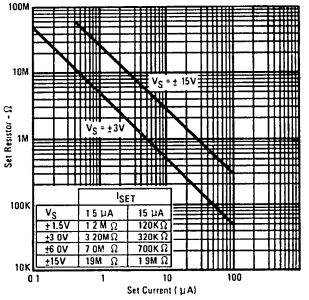
TYPICAL BIASING CIRCUITS



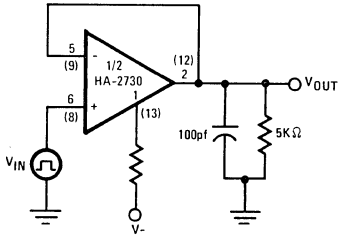
SUGGESTED OFFSET NULL

NOTE Numbers in parenthsis refer to the second half

SET CURRENT VS. SET RESISTOR

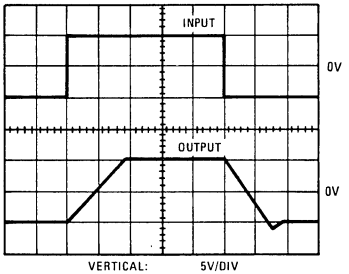


TRANSIENT RESPONSE/SLEW RATE CIRCUIT



NOTE Numbers in parenthsis refer to the second half.

SLEWING WAVEFORM



VERTICAL: 5V/DIV
HORIZONTAL: 1µS/DIV
I_{SET} = 100µA

2

HARRIS

HA-2740

Quad Programmable Operational Amplifier

2

FEATURES

- WIDE PROGRAMMING RANGE
  - ► SLEW RATE 0.8V/μs
  - ► BANDWIDTH 1MHz
  - ► BIAS CURRENT 8nA
  - ► SUPPLY CURRENT 250μA
- WIDE POWER SUPPLY RANGE
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

The Harris HA-2740 programmable amplifier is an internally compensated monolithic device offering a wide range of performance, that can be controlled by adjusting the circuit "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables the HA-2740 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. The HA-2740 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting programming current.

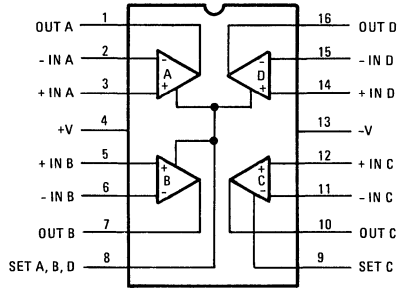
A major advantage of the HA-2740 is that operating characteristics remain virtually constant over a wide supply range ($\pm$1.2V to $\pm$18V), allowing the amplifier to offer maximum performance in almost any system including battery-operated equipment. A primary application for the HA-2740 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, the HA-2740 can be used for designs such as current controlled oscillators, modulators, sample and hold circuits and variable active filters.

The HA-2740-2 is guaranteed over -55°C to +125°C. The HA-2740-5 is specified from 0°C to +75°C. Both parts are available in a 16 pin dual-in-line package.

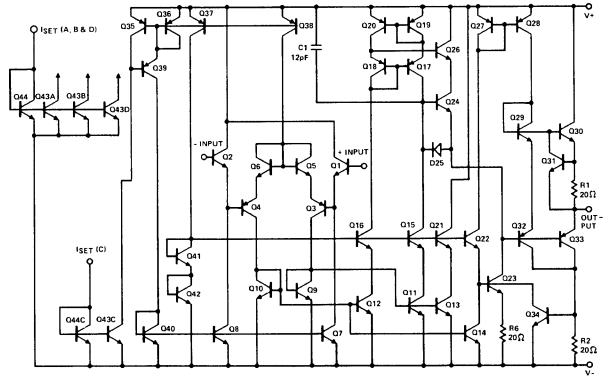
PINOUT

Section 11 for Packaging

TOP VIEW



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	45.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 2)	±15.0V
I_{SET} (Current at I_{SET})	500μA
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0 \leq V_{SET} \leq V+$
Power Dissipation	300mW
Operating Temperature Range:	
HA-2740-2	$-55^oC \leq T_A \leq +125^oC$
HA-2740-5	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS V+ = +15.0V, V⁻ = -15.0V

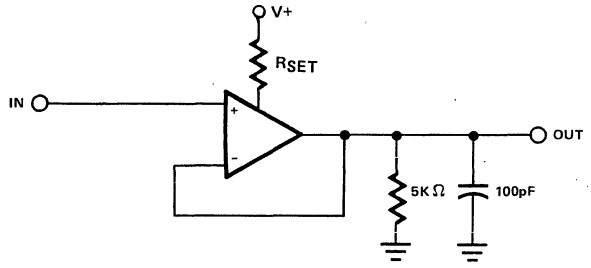
PARAMETER	TEMP	HA-2740-2 -55°C to +125°C						HA-2740-5 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS														
Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			30	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 3)	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 4)	25°C	30K	100K		30K	120K		25K	100K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio (Note 5)	25°C		100			100			100			100		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 6)	25°C	±12	±14		±12	±14		±12	±14		±12	±14		V
	Full	±10			±10			±10			±10			V
Channel Separation (Note 7)	25°C		110			110			110			110		dB
Output Current (Note 8)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short Circuit Current	25°C		3.6			16			3.6			16		mA
TRANSIENT RESPONSE														
Rise Time (Note 9)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 9)	25°C		2			10			2			10		%
Slew Rate (Note 10)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current (each amp)	25°C		25			250			25			250		μA
	Full			50			450			50			450	μA
Power Supply Rejection Ratio (Note 11)	Full	100				100		150			150			μV/V

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. This parameter based upon design calculations.
4. V_O = ±10V, R_L = 5K @ I_{SET} = 15μA
   R_L = 75K @ I_{SET} = 1.5μA
5. VCM = ±5V
6. R_L = 5kΩ @ I_{SET} = 15μA, R_L = 75K @ I_{SET} = 1.5μA
7. RS = 1kΩ, f = 100Hz.
8. V_O = ±10V
9. AV = 1, VIN = 200ı V, RL = 5k, CL = 100pF.
10. V_O = ±10V, R_L = 5K @ I_{SET} = 15μA,
    R_L = 20K @ I_{SET} = 1.5μA
11. AV = ±5V.

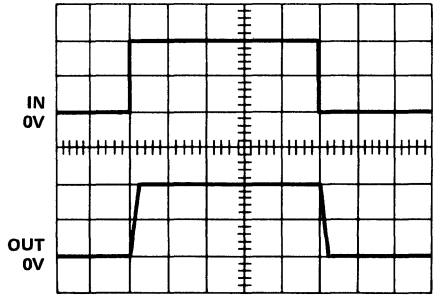
TEST CIRCUITS

LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



LARGE SIGNAL RESPONSE

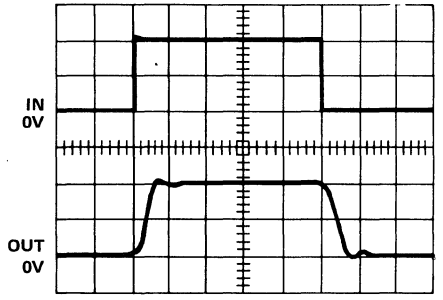
VOLTS: Input A: 5V/Div.,
Output B: 5V/Div.
TIME: 50μs/Div.



VERTICAL: 5V/Div.
HORIZONTAL: 50μs/Div.

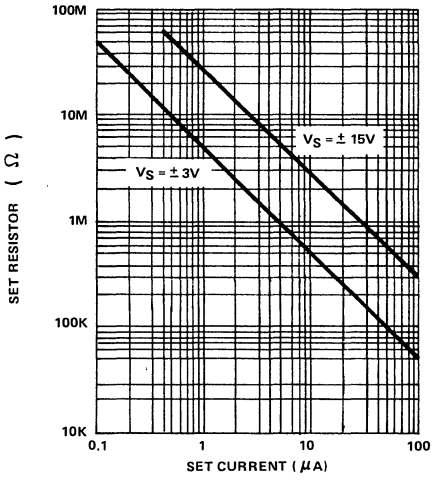
SMALL SIGNAL RESPONSE

VOLTS: Input A: 100mV/Div.,
Output B: 100mV/Div.
TIME: 1μs/Div.



VERTICAL: 100mV/Div.
HORIZONTAL: 1μs/Div.

SET CURRENT vs. SET RESISTOR



	ISET	
VS	1.5μA	15μA
±1.5V	1.2MΩ	120KΩ
±3.0V	3.20MΩ	320KΩ
±6.0V	7.0MΩ	700KΩ
±15V	19MΩ	1.9MΩ

HARRIS

HA-4156

High Performance Quad Operational Amplifier

FEATURES

- SLEW RATE — 1.6 $V/\mu S$ (TYP.)
- BANDWIDTH — 3.5 MHz (TYP.)
- INPUT VOLTAGE NOISE (f = 1KHz) — 9 $NV/\sqrt{Hz}$ (TYP.)
- INPUT OFFSET VOLTAGE — 0.5 mV (TYP.)
- INPUT BIAS CURRENT — 60 nA (TYP.)
- SUPPLY RANGE — ±2V to ±20V
- NO CROSSOVER DISTORTION
- STANDARD QUAD PIN-OUT

DESCRIPTION

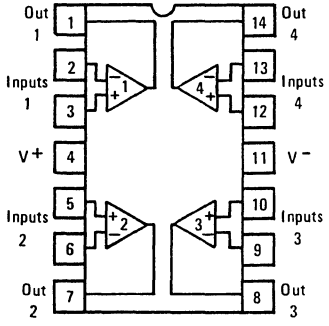
The HA-4156 contains four general purpose operational amplifiers on a monolithic chip. The performance of each amplifier is equal to or better than the 741 type amplifier in all respects. Its superior bandwidth, slew rate and noise characteristics make it an excellent choice for active filter or audio amplifier applications.

The HA-4156-5 is guaranteed over 0°C to +75°C.

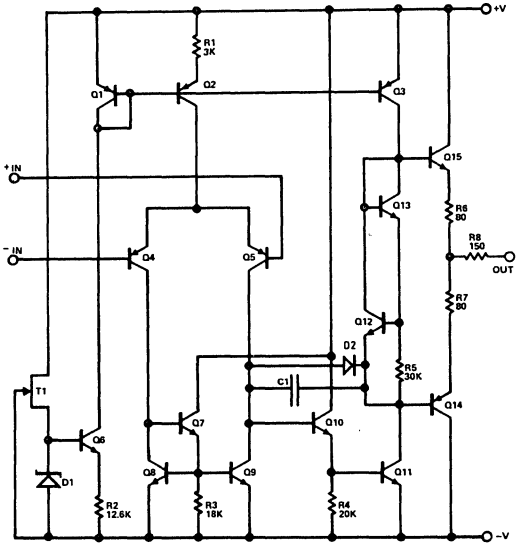
2

PINOUT

PIN OUT Section 11 for Packaging



SCHEMATIC



(¼) HA-4156

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated		Power Dissipation (Note 3)	880mW
Voltage Between V+ and V− Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±30.0V	HA-4156-5	$0°C \leq T_A \leq +75°C$
Input Voltage (Note 1)	±15.0V		
Output Short Circuit Duration (Note 2)	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS

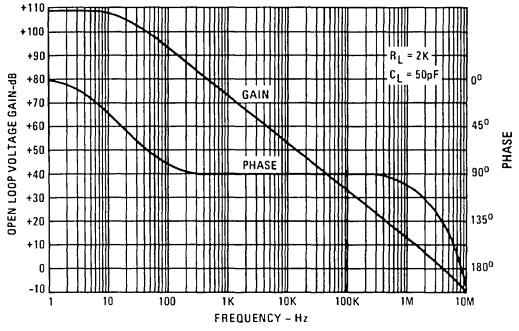
V+ = 15V, V− = −15V

PARAMETER	TEMP.	HA-4156-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	+25°C		1.0	5.0	mV
	Full		5.0	6.5	mV
Av. Offset Voltage Drift	Full		5		µV/°C
Bias Current	+25°C		60	300	nA
	Full			400	nA
Offset Current	+25°C		30	50	nA
	Full			100	nA
Common Mode Range	Full	±12			V
Differential Input Resistance	+25°C		5		MΩ
Input Noise Voltage (f = 1KHz)	+25°C		9		$nV/\sqrt{Hz}$
(f = 20Hz to 20kHz)	+25°C		1.4	2.0	µVRMS
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Note 4)	+25°C	25K	50K		V/V
	Full	15K			V/V
Common Mode Rejection Ratio (Note 8)	+25°C	80			dB
	Full	74			dB
Channel Separation (Note 5)	+25°C		−108		dB
Small Signal Bandwidth	+25°C	2.8	3.5		MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (R_L = 10K)	Full	±12	±13.7		V
(R_L = 2K)	Full	±10	±12.5		V
Full Power Bandwidth (Note 4)	+25°C	20	25		KHz
Output Current (Note 6)	Full	±5	±15		mA
Output Resistance	+25°C		300		Ω
TRANSIENT RESPONSE (Note 7)					
Rise Time	+25°C		75		ns
Overshoot	+25°C		25		%
Slew Rate	+25°C	1.3	±1.6		V/µs
POWER SUPPLY CHARACTERISTICS					
Supply Current (I^+ or I^-)	+25°C			7.0	mA
Power Supply Rejection Ratio (Note 8)	Full	80			dB

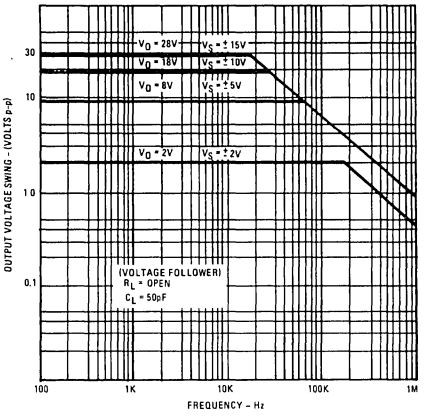
NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K
5. Referred to input; f = 10KHz, R_S = 1K
6. V_{OUT} = ±10
7. See pulse response characteristics
8. ΔV = ±5.0V

$V+ = +15V$, $V- = -15V$, $T_A = +25^oC$
Unless Otherwise Stated.

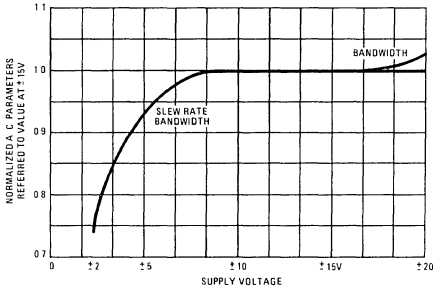
OPEN LOOP FREQUENCY RESPONSE



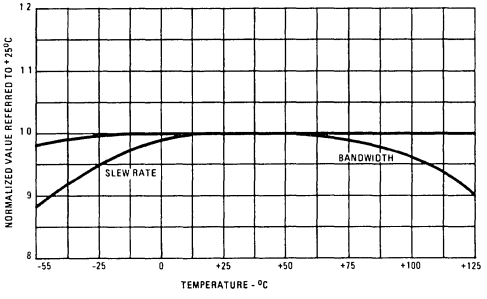
OUTPUT VOLTAGE SWING
VS. FREQUENCY



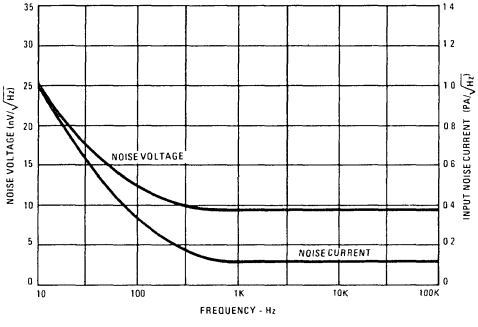
NORMALIZED AC PARAMETERS
VS. SUPPLY VOLTAGE



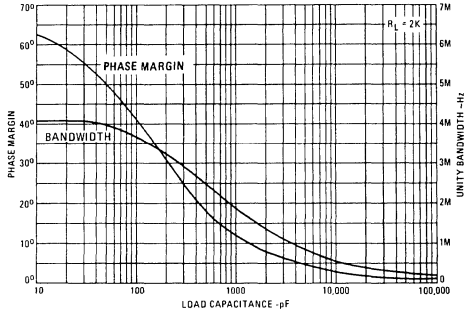
NORMALIZED AC PARAMETERS
VS. TEMPERATURE



INPUT NOISE VS. FREQUENCY



SMALL SIGNAL BANDWIDTH AND PHASE
MARGIN VS. LOAD CAPACITANCE



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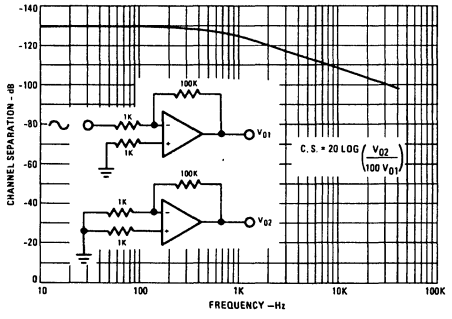
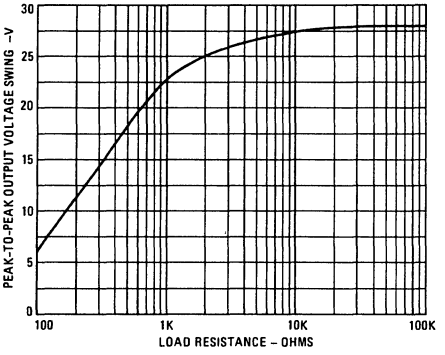
PERFORMANCE CURVES (cont'd.)

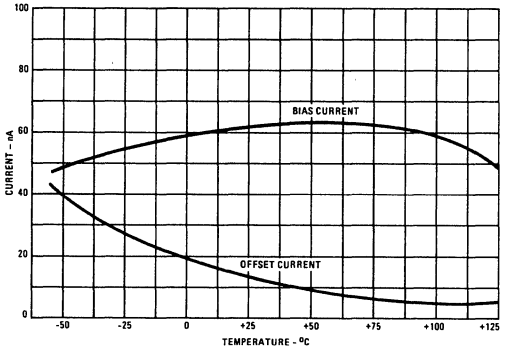
CHANNEL SEPARATION VS. FREQUENCY



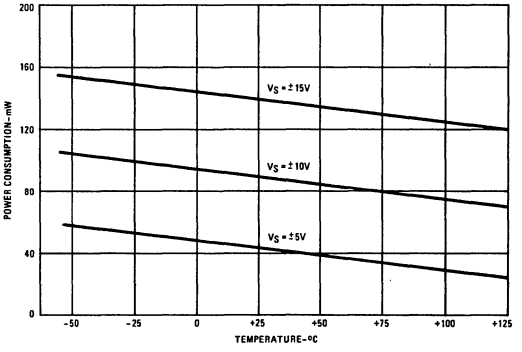
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

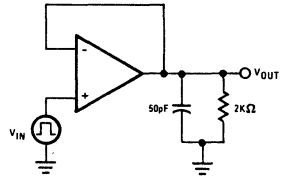


POWER CONSUMPTION VS. TEMPERATURE

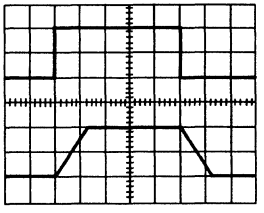


PULSE RESPONSE

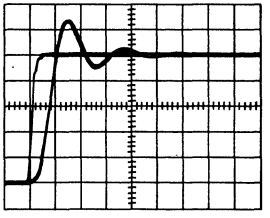
TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEW RESPONSE (Volts: 5V/Div, Time: 5 μs/Div)



TRANSIENT RESPONSE (Volts: 10mV/Div , Time: 100ns/Div)



HA-4600/02/05

High Performance Quad Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE 0.3mV
- HIGH SLEW RATE ±4V/μs
- WIDE BANDWIDTH 8MHz
- LOW DRIFT 2μV/°C
- FAST SETTLING (0.01%, 10V STEP) 4.2μs
- LOW POWER CONSUMPTION 35mW/AMP
- SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

- HIGH Q, WIDE BAND FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- DATA ACQUISITION SYSTEMS
- INTEGRATORS
- ABSOLUTE VALUE CIRCUITS
- TONE DETECTORS

DESCRIPTION

The HA-4600 series are high performance dielectrically isolated monolithic quad operational amplifiers with superior specifications not previously available in a quad amplifier. These amplifiers offer excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

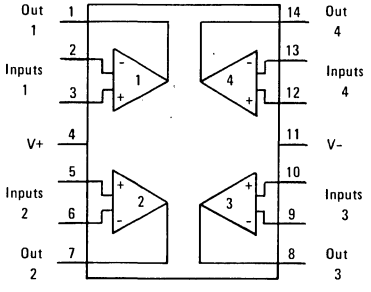
A wide range of applications can be achieved by using the features made available by the HA-4600 series. With wide bandwidth (8MHz), low power (35mW/amp), and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise (8nV/$\sqrt{Hz}$) and excellent full power bandwidth (60kHz). The HA-4602/4605 is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2μV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/μs) and fast settling time (4.2μs to 0.01%, 10V step) makes these amplifiers useful compoinents in fast, accurate data acquisition systems.

The HA-4600 series are available in 14 pin CERDIP packages which are interchangeable with most other quad op amps. HA-4600/4602-2 is specified from -55°C to +125°C and HA-4600/4605-5 is specified over 0°C to +75°C range.

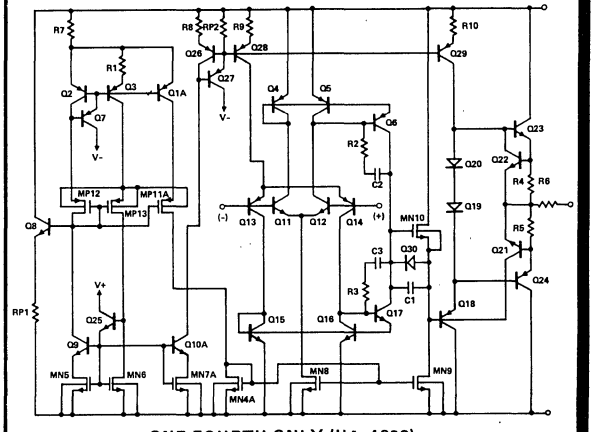
PINOUT

Section 11 for Packaging

TOP VIEW



SCHEMATIC



ONE FOURTH ONLY (HA-4600)

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated		Power Dissipation (Note 4)	880mW
Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±7V	HA-4600/4602-2	$-55°C \leq T_A \leq +125°C$
Input Voltage (Note 2)	±15.0V	HA-4600/4605-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration (Note 3)	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS V+ = +15V, V- = -15V

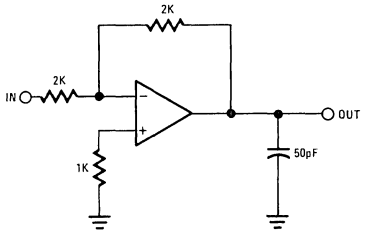
		HA-4600-2 HA-4600-5			HA-4602-2 HA-4605-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.3	2.5		3.0	9	mV
	Full			3.0			10	mV
Av. Offset Voltage Drift	Full		2			5		µV/°C
Bias Current	+25°C		130	200		200	400	nA
	Full			325			500	nA
Offset Current	+25°C		30	75		70	150	nA
	Full			125			175	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance			500			500		kΩ
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
Common Mode Rejection Ratio (Note 9)	Full	86			80			dB
Channel Separation (Note 6)	+25°C		-108			-108		dB
Small Signal Bandwidth	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60			60		kHz
Output Current (Note 7)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		50			50		ns
Overshoot	+25°C		30			30		%
Slew Rate	+25°C	1	±4			±4		V/µs
Settling Time (Note 10)			4.2			4.2		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.6	5.5		5.0	7.5	mA
Power Supply Rejection Ratio (Note 9)	Full	86			74			dB

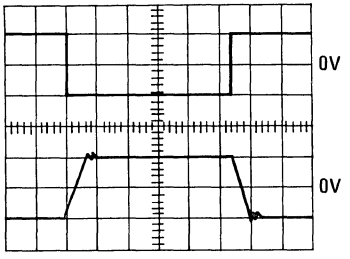
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 2K ohms.
6. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak-to-peak; R_S = 1K ohms. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
7. Output current is measured with V_{OUT} = ±5 volts.
8. For transient response test circuits and measurement conditions refer to Test Circuits section of the data sheet.
9. ΔV = ±5.0 volts.
10. Settling time is measured to 0.1% of final value for a 10 volt input step, A_V = -1.

TEST CIRCUITS

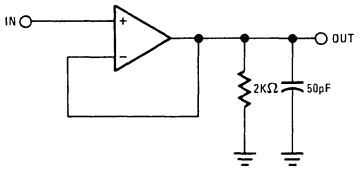
LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5μs/Div.)

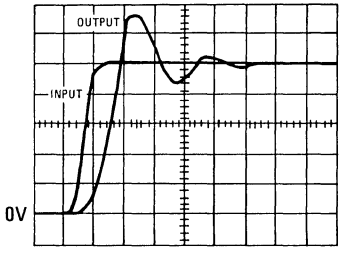




VERT. 5V/DIV.
HORZ. 5 μs/DIV.

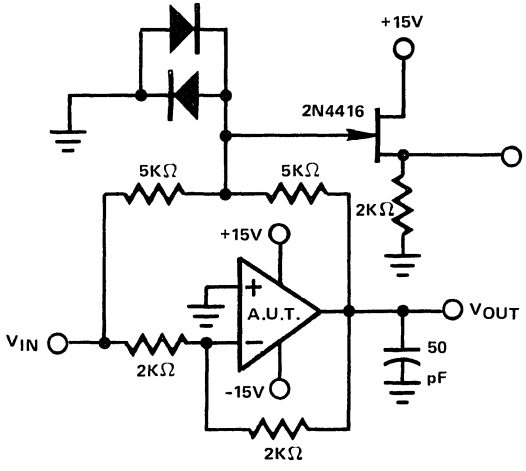
SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.)





HORIZONTAL: 50 NSEC/DIV.
VERTICAL. 10mV/DIV

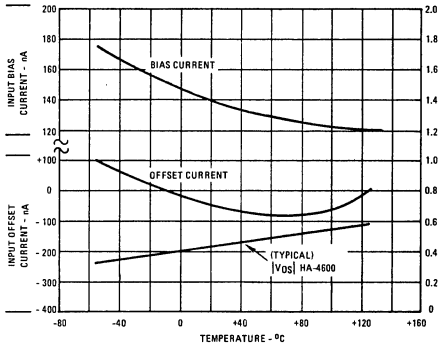
SETTLING TIME CIRCUIT



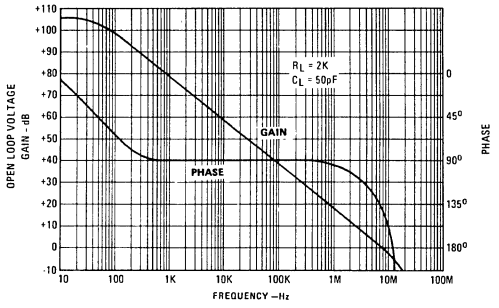
- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

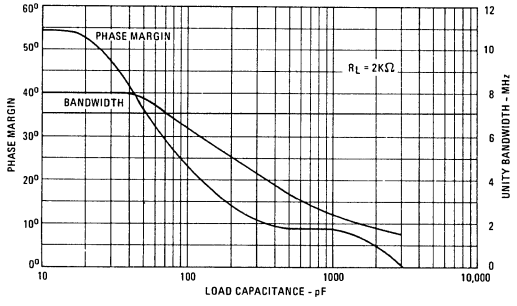
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



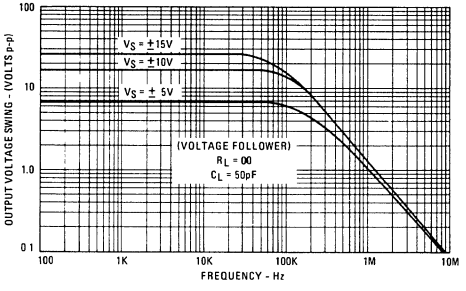
OPEN LOOP FREQUENCY RESPONSE



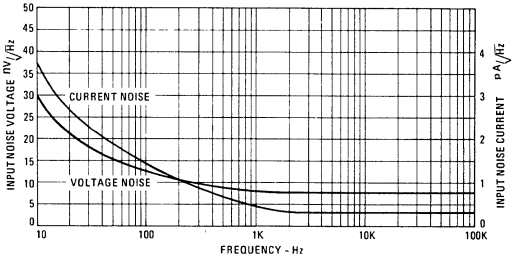
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



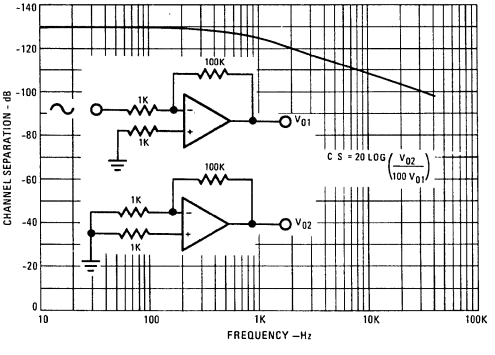
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



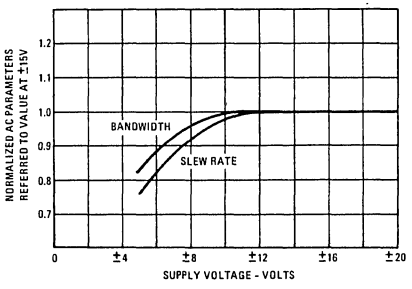
INPUT NOISE VS. FREQUENCY



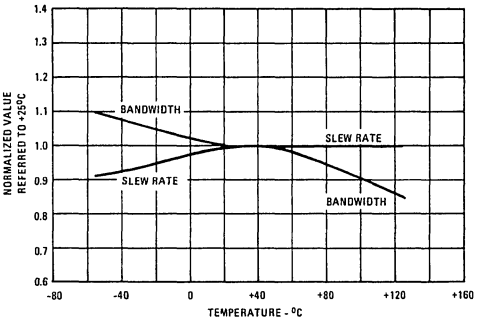
CHANNEL SEPARATION VS. FREQUENCY



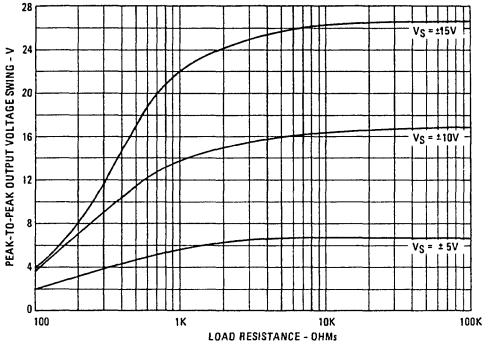
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



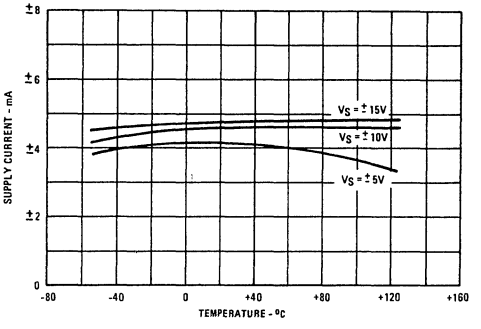
NORMALIZED AC PARAMETERS VS. TEMPERATURE



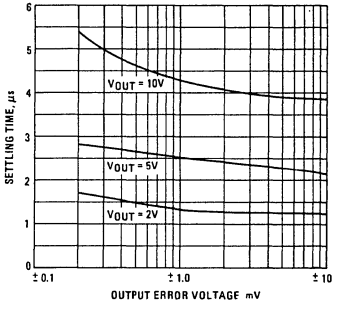
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



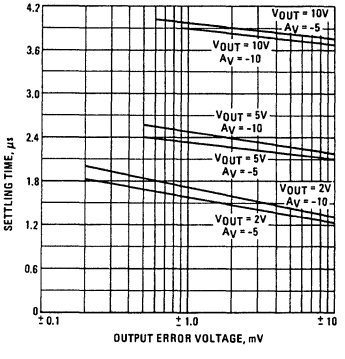
POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



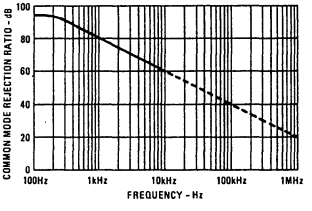
SETTLING TIME VS. OUTPUT AMPLITUDE (A_V = -1)



SETTLING TIME VS. OUTPUT AMPLITUDE AND SIGNAL GAIN (A_V = -5 AND A_V = -10)



HA-4602 - COMMON MODE REJECTION RATIO VS. FREQUENCY



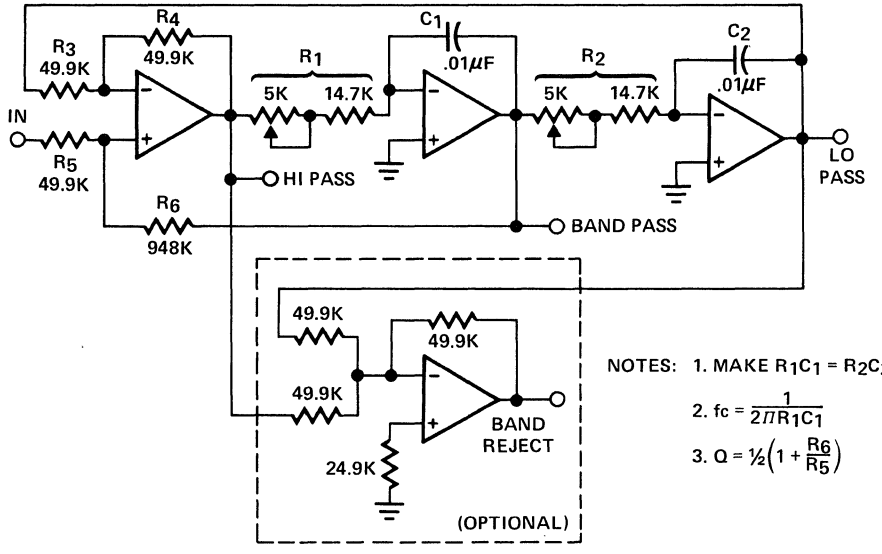
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. UNUSED OP AMPS: Unused op amp sections should be connected in a non-inverting follower configuration with the (+) input tied to ground in order to insure optimum performance of devices being used.

3. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

APPLICATIONS

2ND ORDER STATE VARIABLE FILTER (1kHz, Q = 10)



NOTES: 1. MAKE $R_1C_1 = R_2C_2$

2. $f_c = \frac{1}{2\pi R_1 C_1}$

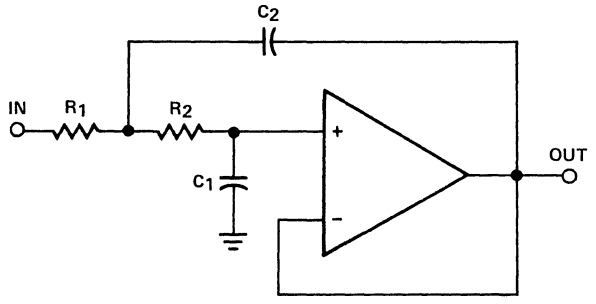
3. $Q = \frac{1}{2}\left(1 + \frac{R_6}{R_5}\right)$

The state variable filter is relatively insensitive to component changes (changes can be adjusted out with potentiometers) and also has low sensitivity to amplifier bandwidths. (Amplifier gain bandwidth product should be $\gg Q \times f_C$). The bandwidth criteria will determine whether a general purpose op amp like Harris HA-4741 or the wide band HA-4602/4605 should be used.

This filter finds wide application because multiple filtering functions are available simultaneously (High pass, Lo pass, Band pass, Band reject). In this circuit the various RC products are matched with pot adjustments allowing for non-interactive adjustment of Q and f_C. This allows capacitors (C_1, C_2) with loose tolerances to be used. To tune for f_C, apply a sine wave at f_C to the input, adjust R_1 for equal amplitudes at the Hi pass and Band pass terminals (they will be phased 90° apart) then adjust R_2 for equal amplitudes at the Band pass and Lo pass terminals.

The state variable filter is often used as building blocks in multiple pole Butterworth of Chebyshev filters. Many references contain normalized tables indicating settings for Q and f_C of each pole-pair section.

SALLEN AND KEY 2ND ORDER LO PASS FILTER



NOTES:

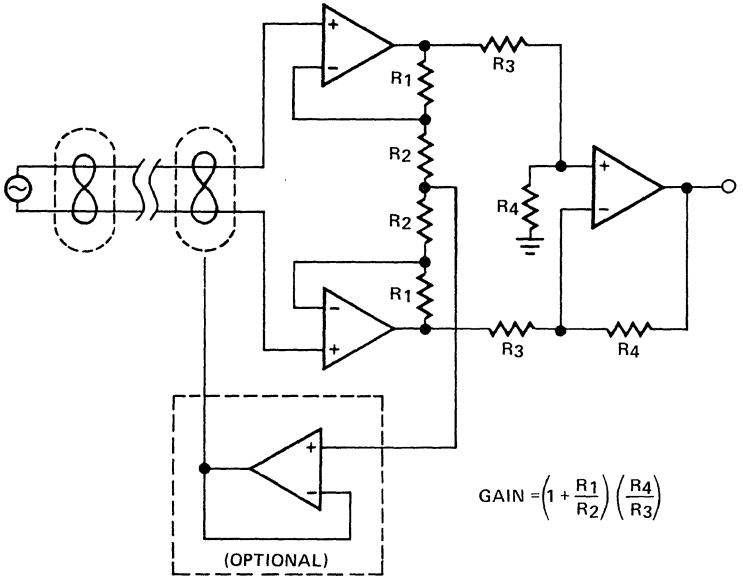
1. Make $R_1 = R_2$
2. $f_c = \frac{1}{2\pi R_1 \sqrt{C_1 C_2}}$
3. $Q = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}$

The advantage of using the Sallen and Key filter is simplicity, but in any application this must be weighed against the state-variable type filter for accuracy, practicality, and cost. Amplifier bandwidth limitations are much more apparent at moderate frequencies and Q values with this filter design. (For accuracy, amplifier gain-bandwidth product should be $\gg f_C \times Q^2$). The wide bandwidth of the HA-4602/4605 is particularly advantageous in this design even at audio frequencies.

In this filter all component values affect both Q and f_C. Precision, temperature stable resistors and capacitors must be used.

For economy, this filter could be used in the low Q stages of multiple-pole filter design, while the state variable type is used in the more critical stages.

INSTRUMENTATION AMPLIFIER



Instrumentation amplifiers (differential amplifiers) are specifically designed to extract and amplify small differential signals from much larger common mode voltages.

To serve as building blocks in instrumentation amplifiers, op amps must have very low offset voltage drift, high gain and wide bandwidth. The HA-4602/4605 is ideally suited for this application, delivering superior input and speed characteristics.

The optional circuitry makes use of the fourth amplifier section as a shield driver which enhances the AC common mode rejection by nullifying the effects of capacitance-to-ground mismatch between input conductors.

HARRIS

HA-4620/22/25

Wideband, High Performance Quad Operational Amplifier

2

FEATURES

- Wide Gain Bandwidth Product — 70MHz
- High Slew Rate — ±20V/μs
- Low Offset Voltage — 0.3mV
- Fast Settling (0.01%, 10V Step) — 2.5μs
- Total Harmonic Distortion — <.01% to 30kHz
- Low Drift — 2μV/°C
- Low Power Consumption — 35mW/Amp
- Supply Range — ±5V to ±20V

APPLICATIONS

- High Q Wide Band Filters
- Pulse Amplifiers
- Audio Amplifiers
- Data Acquisition Systems
- Absolute Value Circuits
- Video and R.F. Amplifiers

DESCRIPTION

The HA-4620 series are wide band quad operational amplifiers featuring high slew rate, wide bandwidth and fast settling time specifications complemented by low input offset voltage, low drift and input noise voltage.

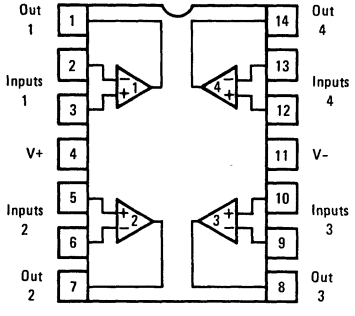
These dielectrically isolated devices are optimized to offer excellent features suitable for applications where a gain of 10 or greater is to be used. The 35mW/amp and a 70MHz gain-bandwidth-product make these monolithic amplifiers valuable components for many active filter circuits. HA-4620 series offers 0.3mW offset voltages and 2μV/°C offset voltage drift for very accurate signal conditioning designs. In high performance audio applications, these amplifiers deliver 260kHz full power bandwidth and 8nV$\sqrt{Hz}$ noise voltage. For fast accurate data acquisition systems HA-4620 series offer 20Vμs slew rate and settling time of 2.5μsecs to 0.1% 10V step.

HA-4620 series are available in 14 pin CERDIP packages and are interchangeable with most other quad op amps. HA-4625 is also available in chip form. HA-4620/4622-2 is specified from -55°C to +125°C and HA-4620/4625-5 is specified over 0°C to +75°C range.

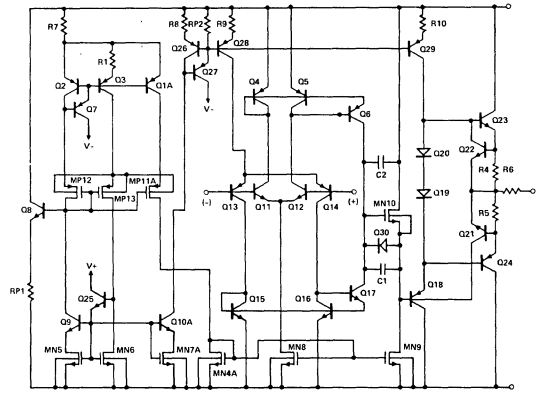
PINOUT

Section 11 for Packaging

TOP VIEW



SCHEMATIC



ONE FOURTH ONLY (HA-4620)

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated.		Power Dissipation (Note 4)	880mW
Voltage between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	±7V	HA-4620/4622-2	$-55°C \leq T_A \leq +125°C$
Input Voltage (Note 2)	±15.0V	HA-4620/4625-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration (Note 3)	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS

		HA-4620-2 HA-4620-5			HA-4622-2 HA-4625-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.3	2.5		3.0	9	mV
	Full			3.0			10	mV
Av. Offset Voltage Drift	Full		2			5		µV/°C
Bias Current	+25°C		130	200		200	400	nA
	Full			325			500	nA
Offset Current	+25°C		30	75		70	150	nA
	Full			125			175	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance	+25°C		500			500		kΩ
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
Common Mode Rejection Ratio (Note 6)	Full	86			80			dB
Channel Separation (Note 7)	+25°C		-108			-108		dB
Gain Bandwidth Products (Note 8)	+25°C		70			70		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 9)	+25°C		260			260		kHz
Output Current (Note 7)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 11)								
Rise Time	+25°C		38	60		38		ns
Overshoot	+25°C		45	60		45		%
Slew Rate	+25°C	±12	±20		±12	±20		V/µs
Settling Time (Note 10)			2.5			2.5		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		4.6	5.5		5.0	7.5	mA
Power Supply Rejection Ratio (Note 9)	Full	86			74			dB

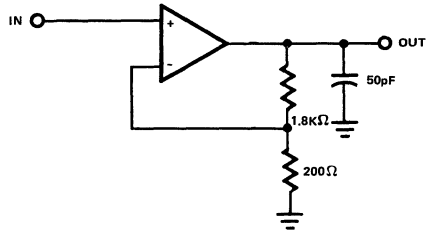
NOTES:

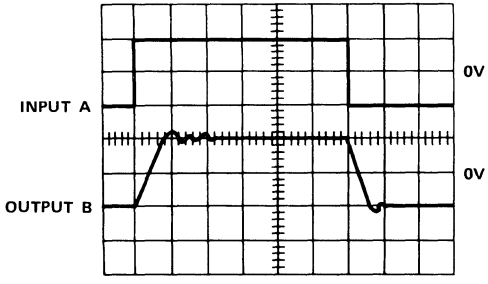
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages $< \pm$ 15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. $V_{OUT} = \pm 10V$, $R_L = 2K\Omega$
6. $\Delta V = \pm 5.0V$.
7. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak to peak; $R_S = 1k\Omega$. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
8. $A_V = 10$; $R_L = 2K$; $C_L \leq 10pF$.
9. Full power bandwidth is guaranteed by equation:
   $$\text{Full power bandwidth} = \frac{\text{Slew Rate}}{2\pi V \text{ Peak}}$$
10. Output current is measured with $V_{OUT} = \pm 5V$.
11. Refer to Test Circuits section of the data sheet.
12. Setting time is measured to 0.1% of final value for a 1 volt input step, and $A_V = -10$.

TEST CIRCUITS

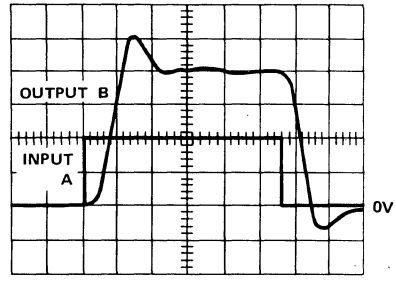
2

LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



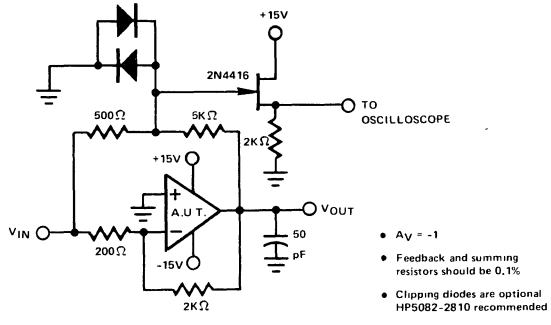


VOLTS: Input A: .5V/Div., Output B: 5V/Div.
TIME: 500ns/Div.



VOLTS: Input A: .01V/Div., Output B: 50mV/Div.
TIME: 50ns/Div.

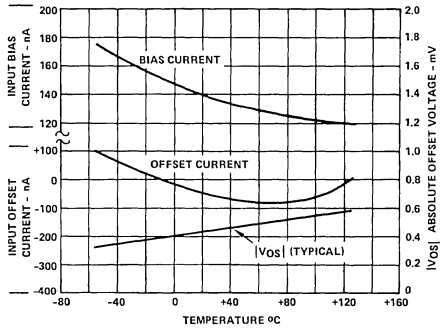
SETTLING TIME CIRCUIT



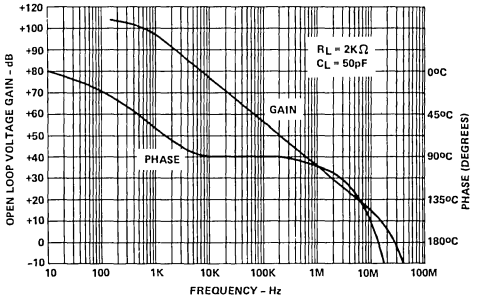
- $A_V = -1$
- Feedback and summing resistors should be 0.1%
- Clipping diodes are optional HP5082-2810 recommended

V+ = +15V, T_A = +25°C Unless otherwise stated.

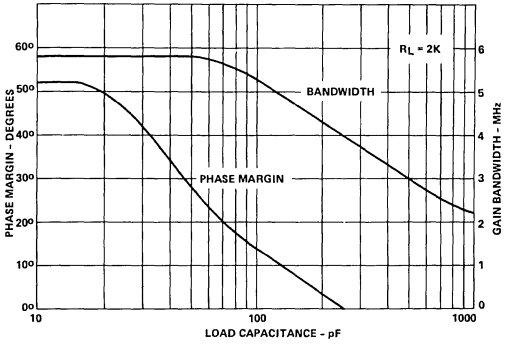
OFFSET VOLTAGE INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



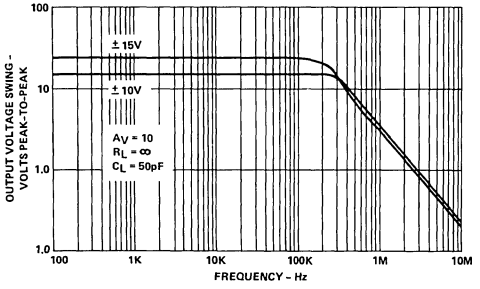
OPEN LOOP FREQUENCY RESPONSE



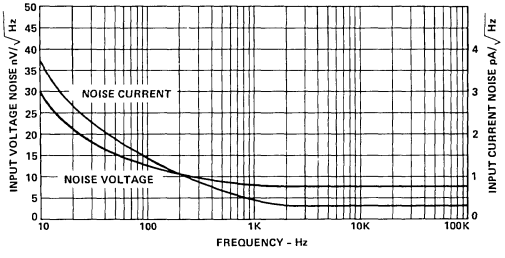
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



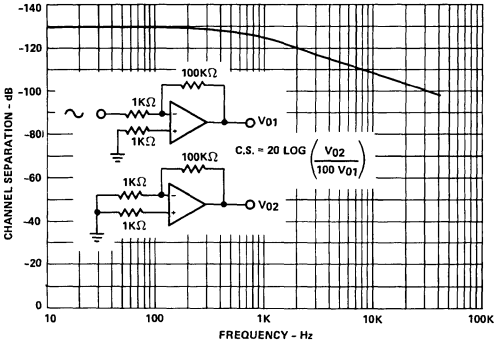
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



INPUT NOISE VS. FREQUENCY

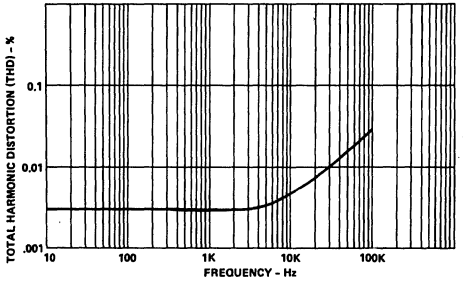


CHANNEL SEPARATION VS. FREQUENCY

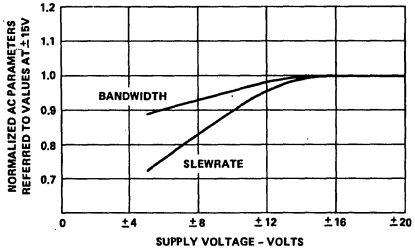


2

TOTAL HARMONIC DISTORTION VS. FREQUENCY

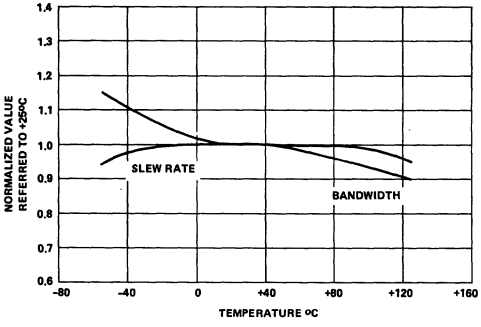


NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE

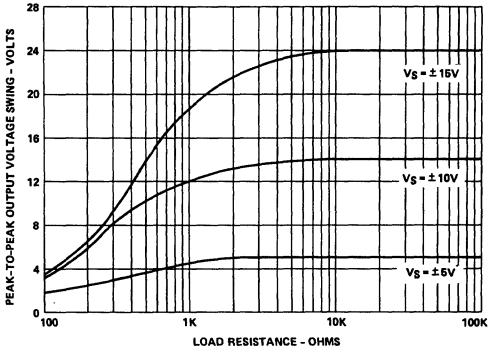


2

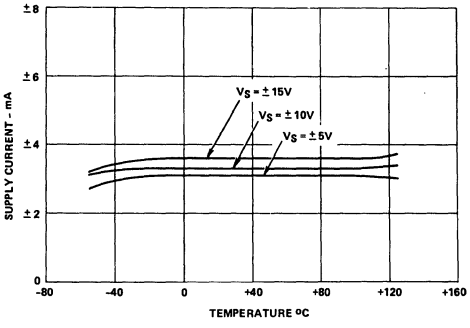
NORMALIZED AC PARAMETERS VS. TEMPERATURE



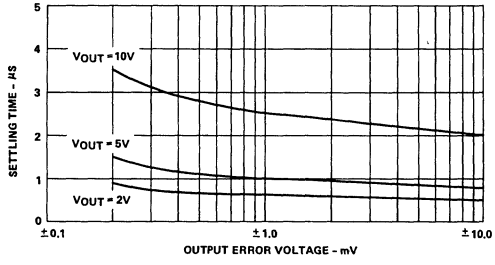
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



SETTLING TIME VS. OUTPUT AMPLITUDE (A_V = -10)



1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible. If several amplifier sections are connected in series, it is recommended that every third or fourth section be decoupled.

2. UNUSED OP AMPS: Unused op amp sections should be connected in a non-inverting A_V = 10 configuration with the (+) input tied to ground in order to optimize performance of devices being used.

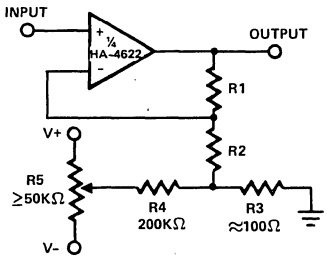
3. In high frequency applications where large value feedback resistors are used, a small capacitor (3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by input capacitance.

4. When driving heavy capacitive loads (>100pF), a small value resistor should be connected in series with the output and inside the feedback loop.

APPLICATIONS

SUGGESTED METHODS FOR OFFSET NULLING

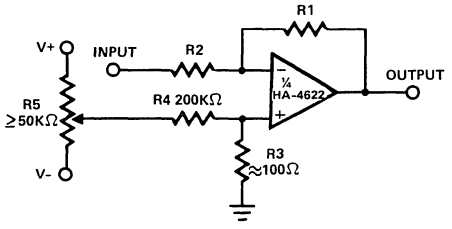
NON-INVERTING AMPLIFIER



NON-INVERTING AND INVERTING AMPLIFIERS RANGE OF ADJUSTMENT DETERMINED BY PRODUCT OF VSUPPLY AND R3/R4 RATIO

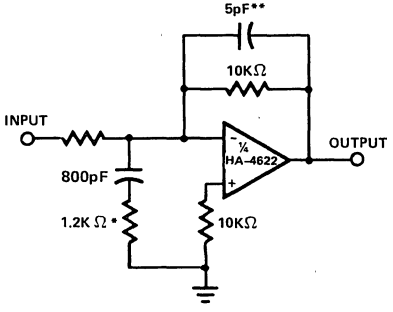
$$A_V = 1 + \frac{R1}{R2 + R3}$$

INVERTING AMPLIFIER

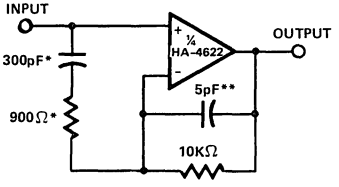


SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY

INVERTING

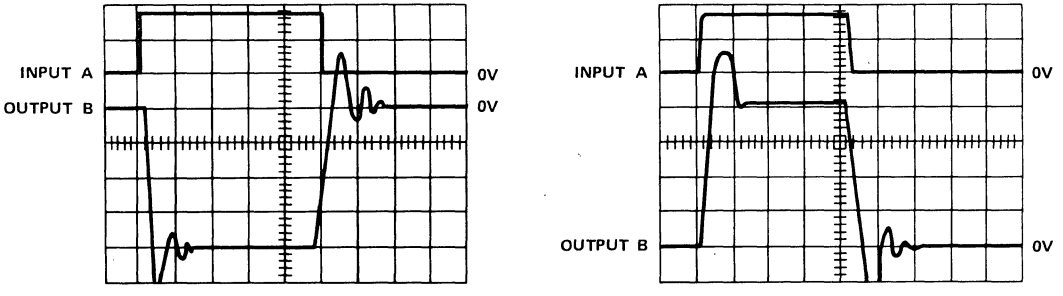


NON-INVERTING



* VALUES WERE DETERMINED EXPERIMENTALLY FOR OPTIMUM SPEED AND SETTLING TIME
** OPTIONAL

LARGE SIGNAL RESPONSE



VOLTS: Input A: 5V/Div., Output B: 2V/Div.
TIME: 1μs/Div.

HARRIS

HA-4741

Quad Operational Amplifier

2

FEATURES

- SLEW RATE — 1.6V/μs (TYP.)
- BANDWIDTH — 3.5MHz (TYP.)
- INPUT VOLTAGE NOISE — 9nV/$\sqrt{Hz}$ (TYP.)
- INPUT OFFSET VOLTAGE — 0.5mV (TYP.)
- INPUT BIAS CURRENT — 60nA (TYP.)
- SUPPLY RANGE — ±2V TO ±20V
- NO CROSSOVER DISTORTION
- STANDARD QUAD PIN-OUT

APPLICATIONS

- UNIVERSAL ACTIVE FILTERS
- D3 COMMUNICATIONS FILTERS
- AUDIO AMPLIFIERS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

The HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/ $\sqrt{Hz}$ at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion. These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (108dB at 1kHz).

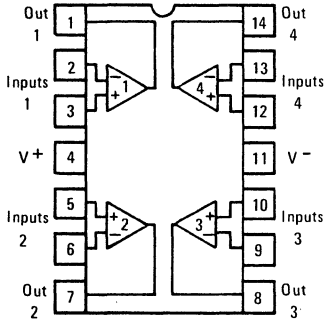
A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

The HA-4741 has guaranteed operation over -55°C to +125°C and can be furnished to meet MIL-STD-883 (HA-4741-8). The HA-4741-5 is guaranteed over 0°C to +75°C and is available in ceramic and plastic dual-in-line packages and in dice form.

PINOUT

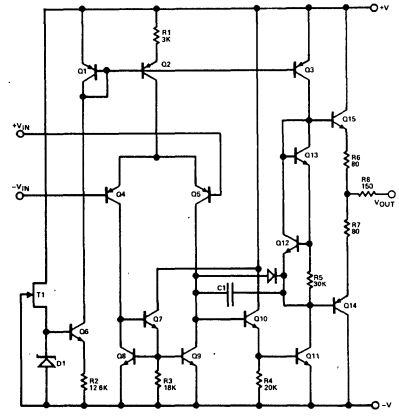
Section 11 for Packaging

TOP VIEW



QUAD OP AMP

SCHEMATIC



(¼) HA-4741

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration (Note 2)	Indefinite
Power Dissipation For Epoxy Package. (Note 3)	880mW
Operating Temperature Range	
HA-4741-2	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-4741-5	$0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range	$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS

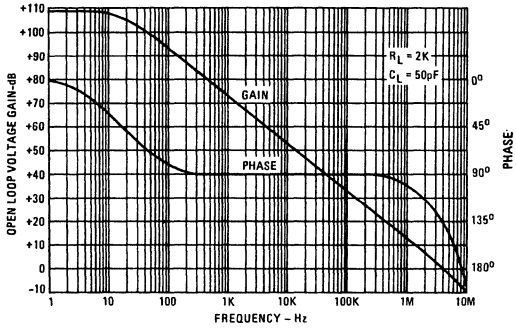
V+ = 15V, V- = -15V

PARAMETER	TEMP.	HA-4741-2 -55°C to +125°C MIN.	TYP.	MAX.	HA-4741-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.5	3.0		1.0	5.0	mV
	Full		4.0	5.0		5.0	6.5	mV
Av. Offset Voltage Drift	Full		5			5		µV/°C
Bias Current	+25°C		60	200		60	300	nA
	Full			325			400	nA
Offset Current	+25°C		15	30		30	50	nA
	Full			75			100	nA
Common Mode Range	Full	±12			±12			V
Differential Input Resistance	+25°C		5			5		MΩ
Input Noise Voltage (f = 1KHz)	+25°C		9			9		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	50K	100K		25K	50K		V/V
	Full	25K			15K			V/V
Common Mode Rejection Ratio (Note 8)	+25°C	80			80			dB
	Full	74			74			dB
Channel Separation (Note 5)	+25°C	90	-108		90	-108		dB
Small Signal Bandwidth	+25°C	2.5	3.5		2.5	3.5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (R_L = 10K)	Full	±12	±13.7		±12	±13.7		V
(R_L = 2K)	Full	±10	±12.5		±10	±12.5		V
Full Power Bandwidth (Notes 4 & 9)	+25°C	14	25		14	25		kHz
Output Current (Note 6)	Full	±5	±15		±5	±15		mA
Output Resistance	+25°C		300			300		Ω
TRANSIENT RESPONSE (Notes 7 &10)								
Rise Time (Note 11)	+25°C		75	140		75	140	ns
Overshoot (Note 11)	+25°C		25	40		25	40	%
Slew Rate (Note 12)	+25°C		±1.6			±1.6		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C			5.0			7.0	mA
Power Supply Rejection Ratio (Note 8)	Full	80			80			dB

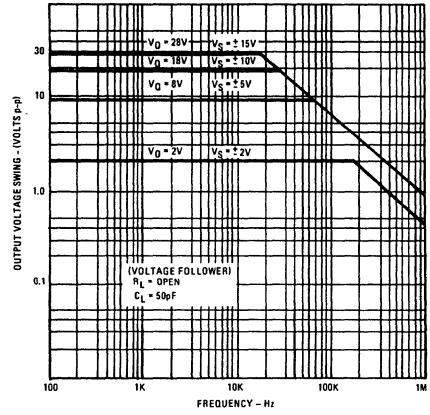
NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K
5. Referred to input; f = 10KHz, R_S = 1K
6. V_{OUT} = ±10
7. See pulse response characteristics
8. ΔV = ±5.0V
9. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./2πVpeak
10. R_L = 2K, C_L = 50pf.
11. V_{OUT} = ±200mV
12. V_{OUT} = ±5V

$V+ = +15V$, $V^- = -15V$, $T_A = +25^oC$
Unless Otherwise Stated.

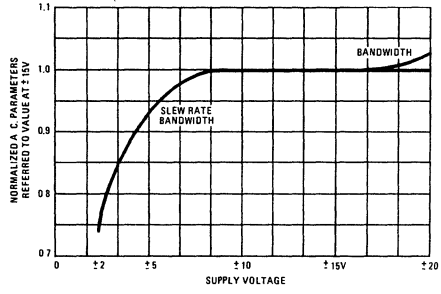
OPEN LOOP FREQUENCY RESPONSE



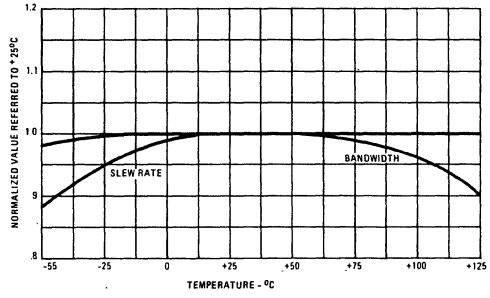
OUTPUT VOLTAGE SWING
VS. FREQUENCY



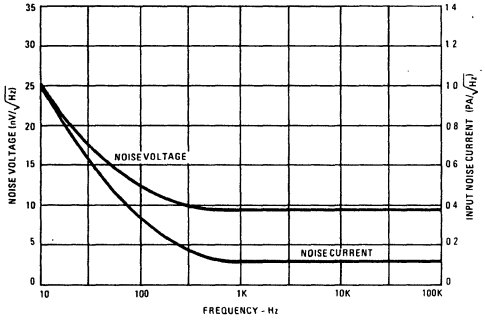
NORMALIZED AC PARAMETERS
VS. SUPPLY VOLTAGE



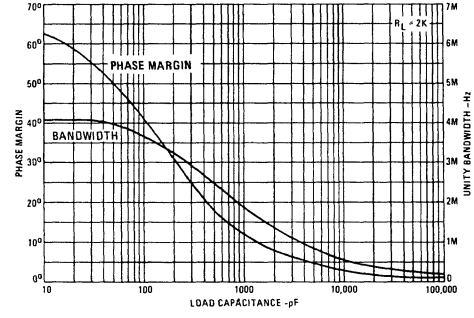
NORMALIZED AC PARAMETERS
VS. TEMPERATURE



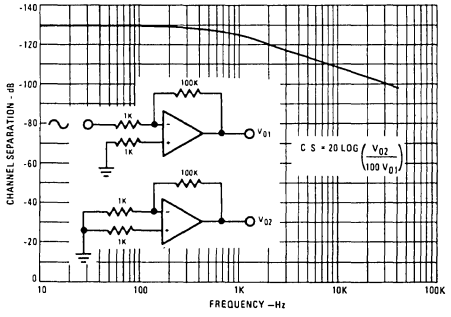
INPUT NOISE VS. FREQUENCY



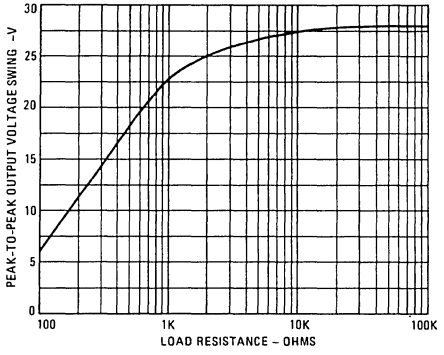
SMALL SIGNAL BANDWIDTH AND PHASE
MARGIN VS. LOAD CAPACITANCE



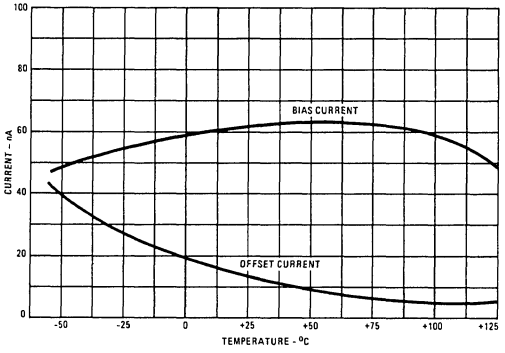
CHANNEL SEPARATION VS. FREQUENCY



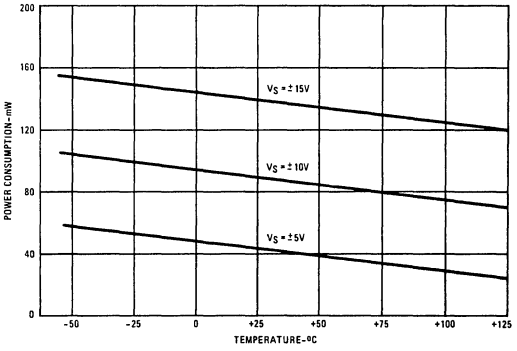
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

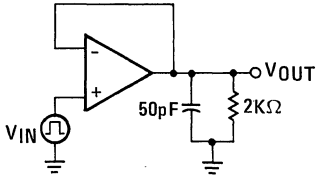


POWER CONSUMPTION VS. TEMPERATURE

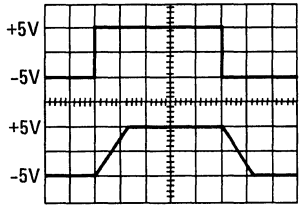


PULSE RESPONSE

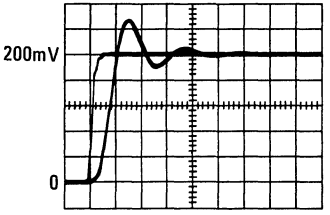
TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEW RESPONSE (Volts: 5V/Div, Time: 5 μs/Div)



TRANSIENT RESPONSE (Volts: 40mV/Div., Time: 100ns/Div.)



2

HARRIS

HA-4900/02/05

Precision Quad Comparator

2

FEATURES

- FAST RESPONSE TIME 130ns
- LOW OFFSET VOLTAGE 2.0mV
- LOW OFFSET CURRENT 10nA
- SINGLE OR DUAL-VOLTAGE SUPPLY OPERATION
- SELECTABLE OUTPUT LOGIC LEVELS
- ACTIVE PULL-UP/PULL-DOWN OUTPUT CIRCUIT - NO EXTERNAL RESISTORS REQUIRED

APPLICATIONS

- THRESHOLD DETECTOR
- ZERO-CROSSING DETECTOR
- WINDOW DETECTOR
- ANALOG INTERFACES FOR MICROPROCESSORS
- HIGH STABILITY OSCILLATORS
- LOGIC SYSTEM INTERFACES

DESCRIPTION

The HA-4900 series are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current, and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5 volt supply (digital systems) or from dual supplies (analog networks) up to ±15 volts. The HA-4900 series contains a unique current driven output stage which can be connected to logic system supplies (V_{Logic}+ and V_{Logic}-) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900 series input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

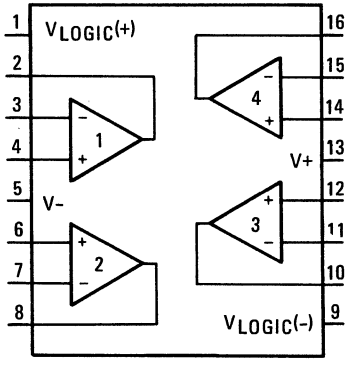
These comparators' combination of features makes them ideal components for signal detection and processing in data acquisition systems, test equipment, and microprocessor/analog signal interface networks.

All devices are available in 16 pin dual-in-line ceramic packages. The HA-4900/4902-2 operates from -55°C to +125°C and the HA-4905-5 operates over a 0°C to +75°C temperature range.

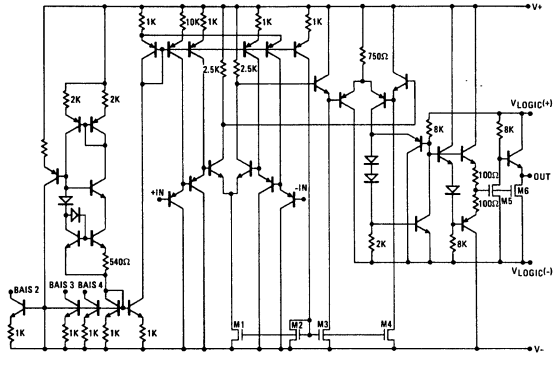
PINOUT

Section 11 for Packaging

Top View



SCHEMATIC



ONE FOURTH ONLY (HA-4900 SERIES)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	33V
Voltage Between $V_{Logic}(+)$ and $V_{Logic}(-)$	18V
Differential Input Voltage	±15V
Peak Output Current	±50mA
Internal Power Dissipation (Note 7, 8)	880mW
Storage Temperature Range	$-65^oC \leq T_A \leq 150^oC$

ELECTRICAL CHARACTERISTICS $V+ = +15.0V, V- = -15.0V, V_{Logic}(+) = 5.0V, V_{Logic}(-) = GND.$

PARAMETER	TEMP	HA-4900-2 -55°C to +125°C MIN	HA-4900-2 -55°C to +125°C TYP	HA-4900-2 -55°C to +125°C MAX	HA-4902-2 -55°C to +125°C MIN	HA-4902-2 -55°C to +125°C TYP	HA-4902-2 -55°C to +125°C MAX	HA-4905-5 0°C to +75°C MIN	HA-4905-5 0°C to +75°C TYP	HA-4905-5 0°C to +75°C MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage (Note 2)	25°C		2	3		2	5		4	7.5	mV
	Full			4			8			10	mV
Offset Current	25°C		10	25		10	35		25	50	nA
	Full			35			35			70	nA
Bias Current (Note 3)	25°C		50	75		50	150		100	150	nA
	Full			150			200			300	nA
Input Sensitivity (Note 4)	25°C			Vio +.3			Vio +.5			Vio +.5	mV
	Full			Vio +.4			Vio +.6			Vio +.7	mV
Common Mode Range	Full	V-		V+ -2.4	V-		V+ +2.4	V-		V+ +2.4	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	25°C		400K			400K			400K		V/V
Response Time ($T_{pd}0$) (Note 5)	25°C		130	200		130	200		130	200	ns
Response Time ($T_{pd}1$) (Note 5)	25°C		180	215		180	215		180	215	ns
OUTPUT CHARACTERISITICS											
Output Voltage Level											
Logic "Low State" (V_{OL}) (Note 6)	Full		0.2	0.4		0.2	0.4		0.2	0.4	V
Logic "High State" (V_{OH}) (Note 6)	Full	3.5	4.2		3.5	4.2		3.5	4.2		V
Output Current											
I_{Sink}	Full	3.0			3.0			3.0			mA
I_{Source}	Full	3.0			3.0			3.0			mA
POWER SUPPLY CHARACTERISTICS											
Supply Current, I_{ps} (+)	25°C		6.5	20		6.5	20		7	20	mA
Supply Current , I_{ps} (-)	25°C		4	8		4	8		5	8	mA
Supply Current, I_{ps} (Logic)	25°C		2.0	4		2.0	4		2.0	4	mA
Supply Voltage Range											
V_{Logic} (+) (Note 7)	Full	0		+15.0	0		+15.0	0		+15.0	V
V_{Logic} (-) (Note 7)	Full	-15.0		0	-15.0		0	-15.0		0	V

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

2. Minimum differential input voltage required to ensure a defined output state.

3. Input bias currents are essentially constant with differential input voltages up to ±9 volts. With differential input voltages from ±9 to ±15 volts, bias current on the more negative input can rise to approximately 500 μA.

4. $R_S \leq 200$ ohms; $V_{IN} \leq$ Common Mode Range. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state. This parameter inludes the effects of offset voltage, offset current, common mode rejection, and voltage gain.

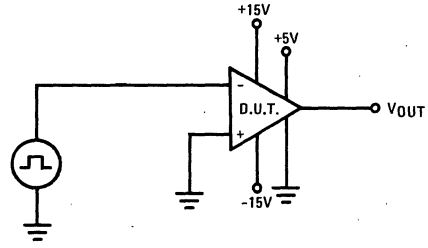
5. For $T_{pd}(1)$; 100mV input step, -5mV overdrive. For $T_{pd}(0)$; -100mV input step, 5mV overdrive. Frequency $\approx$ 100Hz; Duty Cycle $\approx$ 50%; Inverting input driven. See Test Circuit below.

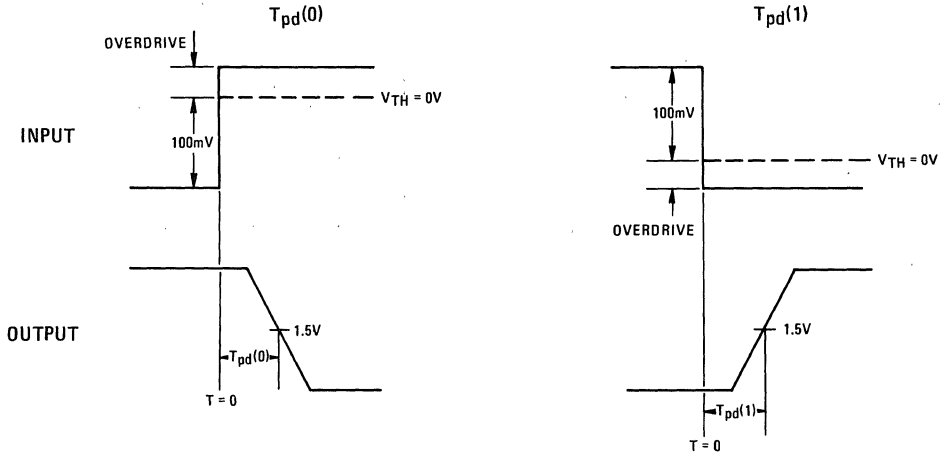
6. For V_{OH} and V_{OL}: $I_{Sink} = I_{Source} = 3.0$mA. For other values of V_{Logic}; V_{OH} (min.) = V_{Logic} + -1.5V.

7. Total Power Dissipation (T.P.D.) is the sum of individual dissipation contributions of V+, V- and V_{Logic} shown in curves of Power Dissipation vs. Supply Voltages (see Performance Curves). The calculated T.P.D. is then located on the graph of Maximum Allowable Package Dissipation vs. Ambient Temperature to determine ambient temperature operating limits imposed by the calculated T.P.D. (See Performance Curves). For instance, the combination of +15V, -15V, +5V, 0V (V+, V-, V_{Logic}+, V_{Logic}-) gives a T.P.D. of 350mW which allows operation to +125°C; the combination +15V, -15V, 0V gives a T.P.D. of 450mW and an operating limit of T_A = +95°C.

8. Derate by 5.8mW/°C above T_A = +75°C.

RESPONSE TIME TEST CIRCUITS

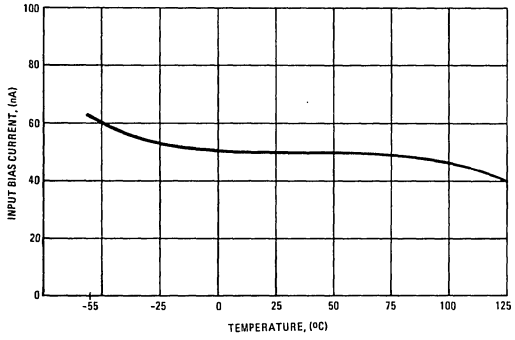




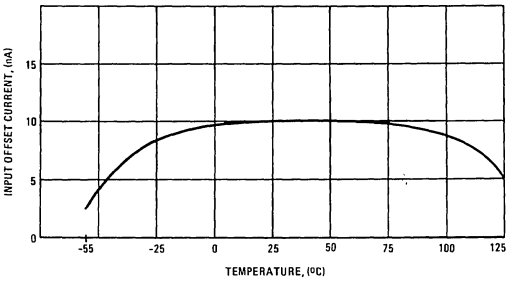
For input and output voltage waveforms for various input overdrives see Performance Curves.

V+ = 15V, V- = -15V, $V_{Logic}(+)$ = 5.0V, $V_{Logic}(-)$ = 0V, T_A = +25°C, Unless Otherwise Stated.

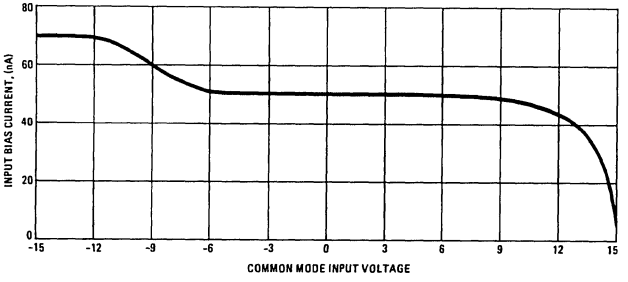
INPUT BIAS CURRENT vs. TEMPERATURE



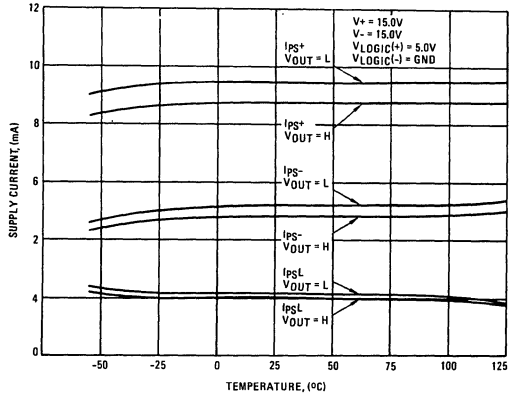
INPUT OFFSET CURRENT vs. TEMPERATURE



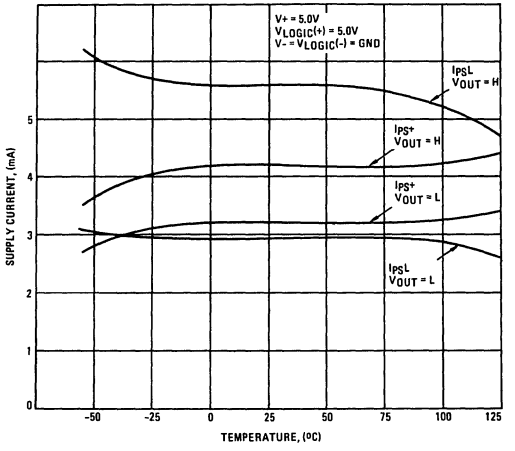
INPUT BIAS CURRENT vs. COMMON MODE INPUT VOLTAGE
($V_{DIFF.}$ = 0V)



SUPPLY CURRENT vs. TEMPERATURE
FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY

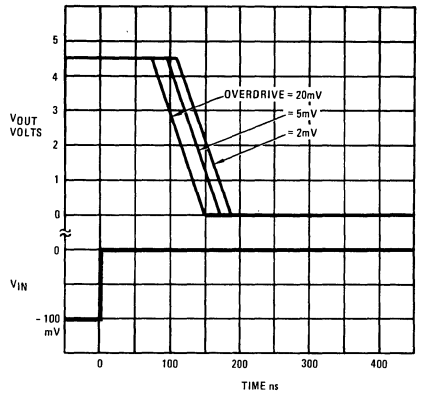


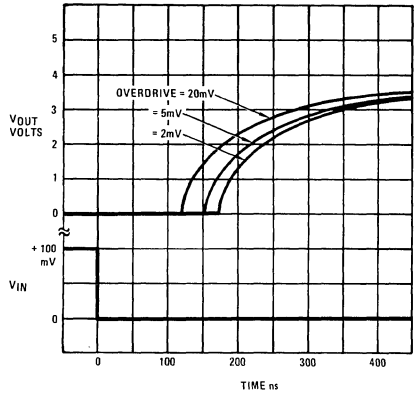
SUPPLY CURRENT vs. TEMPERATURE
FOR SINGLE +5V OPERATION



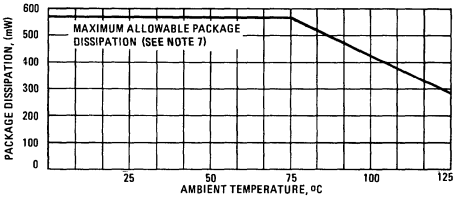
2

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

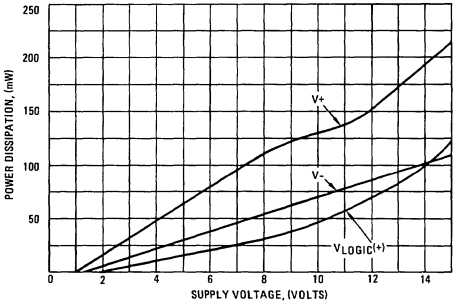




MAXIMUM PACKAGE DISSIPATION vs. $T_{AMBIENT}$



MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE (NO LOAD CONDITION)



APPLYING THE HA-4900 SERIES COMPARATORS

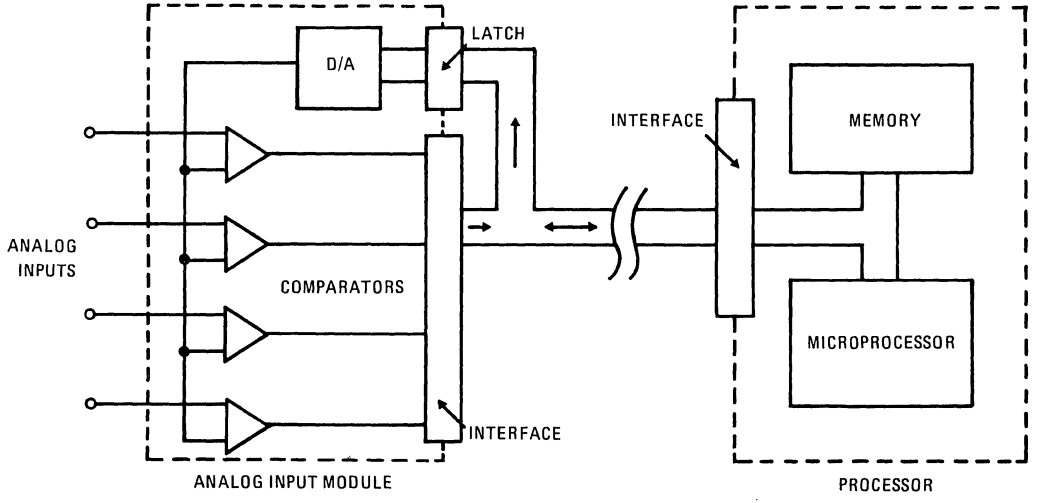
1. SUPPLY CONNECTIONS: This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to V_{Logic}+ and V_{Logic}-. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings (15V P-P, max.) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to +15V), V+ and V_{Logic}+ may be connected together to the positive supply while V- and V_{Logic}- are grounded. If an input signal could swing negative with respect the V- terminal, a resistor should be connected in series with the input to limit input current to $<$ 5mA since the C-B junction of the input transistor would be forward biased.

2. UNUSED INPUTS: Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter".

3. CROSSTALK: Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{OS}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

4. POWER SUPPLY DECOUPLING: Decouple all power supply lines with .01 μ F ceramic capacitors to a ground line located near the package to reduce coupling between channnels or from external sources.

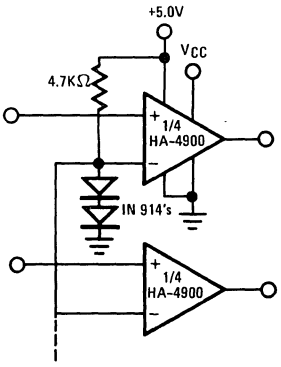
5. RESPONSE TIME: Fast rise time ($<$ 200ns) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.



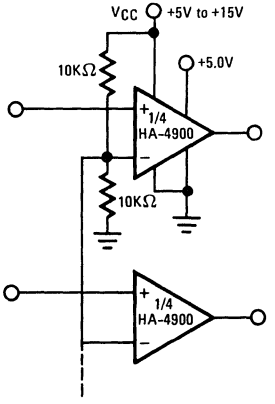
DATA ACQUISITION SYSTEM

In this circuit the HA-4900 series is used in conjunction with a D to A converter to form a simple, versatile, multi-channel analog input for a data acquisition system. In operation the processor first sends an address to the D to A, then the processor reads the digital word generated by the comparator outputs.

To perform a simple comparison, the processor sets the D to A to a given reference level, then examines one or more comparator outputs to determine if their inputs are above or below the reference. A window comparison consists of two such cycles with 2 reference levels set by the D to A. One way to digitize the inputs would be for the processor to increment the D to A in steps. The D to A address, as each comparator switches, is the digitized level of the input. While stairstepping the D to A is slower than successive approximation, all channels are digitized during one staircase ramp.



TTL TO CMOS

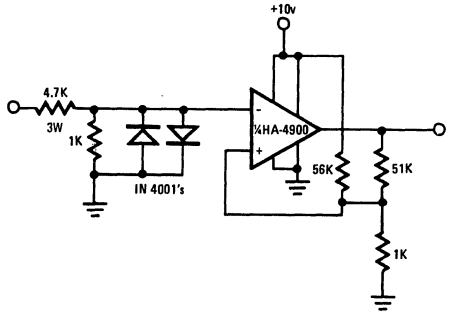


CMOS TO TTL

LOGIC LEVEL TRANSLATORS

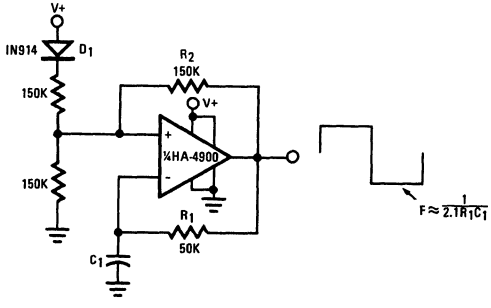
The HA-4900 series comparators can be used as versatile logic interface devices as shown in the circuits above. Negative logic devices may also be interfaced with appropriate supply connections.

If separate supplies are used for V- and V_{Logic-}, these logic level translators will tolerate several volts of ground line differential noise.



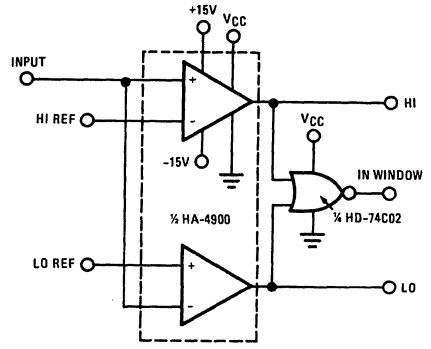
RS-232 TO CMOS LINE RECEIVER

This RS-232 type line receiver to drive CMOS logic uses a Schmitt trigger feedback network to give about 1 volt input hysteresis for added noise immunity. A possible problem in an interface which connects two equipments, each plugged into a different AC receptacle, is that the power line voltage may appear at the receiver input when the interface connection is made or broken. The two diodes and a 3 watt input resistor will protect the inputs under these conditions.



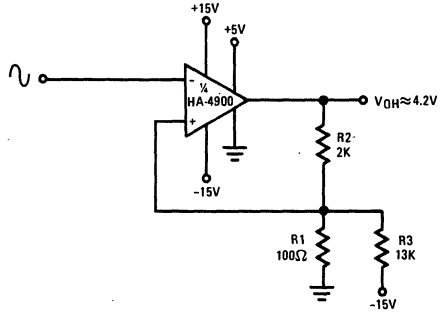
OSCILLATOR/CLOCK GENERATOR

This self-starting fixed frequency oscillator circuit gives excellent frequency stability. R_1 and C_1 comprise the frequency determining network while R_2 provides the regenerative feedback. Diode D_1 enhances the stability by compensating for the difference between V_{OH} and V_{Supply}. In applications where a precision clock generator up to 100kHz is required, such as in automatic test equipment, C_1 may be replaced by a crystal.



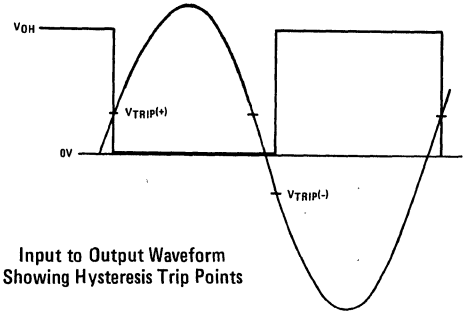
WINDOW DETECTOR

The high switching speed, low offset current and low offset voltage of the HA-4900 series makes this window detector circuit extremely well suited to applications requiring fast, accurate, decision-making. The circuit above is ideal for industrial process system feedback controllers, or "out-of-limit" alarm indicators.



SCHMITT TRIGGER (ZERO CROSSING DETECTOR WITH HYSTERESIS)

This circuit has a 100mV hysteresis which can be used in applications where very fast transition times are required at the output even though the signal input is very slow. The hysteresis loop also reduces false triggering due to noise on the input. The waveforms below show the trip points developed by the hysteresis loop.



Input to Output Waveform
Showing Hysteresis Trip Points

HARRIS

HA-5062 Series

Low Power JFET Input Dual Operational Amplifiers

Preliminary

FEATURES

- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- LOW INPUT BIAS CURRENT 200pA
- LOW INPUT OFFSET CURRENT 100pA
- VERY LOW POWER CONSUMPTION
  TYPICAL SUPPLY CURRENT 200μA
- INTERNAL FREQUENCY COMPENSATION
- HIGH SLEW RATE 4V/μs
- PIN COMPATIBLE WITH LM1458
- DIRECT REPLACEMENT FOR TL062

APPLICATIONS

- ACTIVE FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- BATTERY OPERATED EQUIPMENT
- SIGNAL CONDITIONING

DESCRIPTION

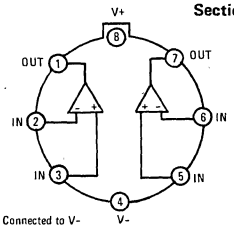
The HARRIS HA-5062 operational amplifiers are a series of dual monolithic JFET-input amplifiers featuring low input bias and offset currents, high input impedence and very low power operation. In addition to being a direct replacement for the TL062 series, the HA-5062 series offers improved performance with a minimum open loop gain 20K V/V and a slew rate of 4v/μs.

This improved performance is a result of the HARRIS FET/Bipolar technology and makes the HA-5062 series of amplifiers ideally suited for applications in industrial control, communication, and battery powered instrumentation equipment.

The HA-5062-2 is characterized for operation over the full military temperature range of -55°C to +125°C. The HA-5062A-5, HA-5062B-5 and HA-5062-5 are all characterized over the commercial temperature range of 0°C to +75°C.

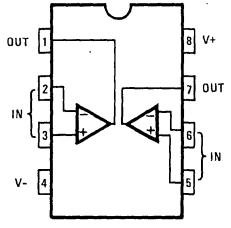
PINOUT

Section 11 for Packaging

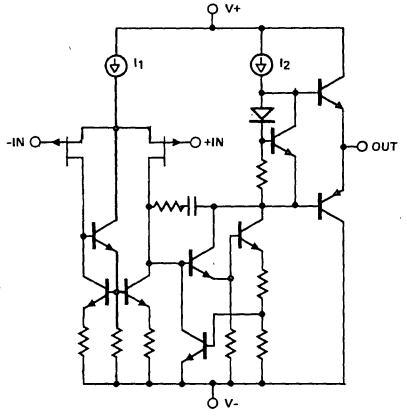


NOTE: Case Connected to V-

TOP VIEWS



SIMPLIFIED SCHEMATIC



(ONE HALF ONLY)

2

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	± 20V	Power Dissipation	600mW*
Differential Input Voltage	± 40V	Operating Temperature Range:	
Input Voltage (Note 2)	±15.0V	HA-5062-2	$-55^{o}C \leq T_A \leq +125^{o}C$
Output Short Circuit Duration	Indefinite	HA-5062-5	$0^{o}C \leq T_A \leq +75^{o}C$
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

* To-99 Derate by 6.75mW/°C above +85°C
Dip Derate by 5.57mW/°C above +65°C

ELECTRICAL CHARACTERISTICS

V+ = 15V V- = 15V

Parameters are guaranteed at indicated ambient temperature after warm-up.

		HA-5062-2 -55°C to +125°C			HA-5062A-5 0°C to 75°C			HA-5062B-5 0°C to 75°C			HA-5062-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage (Note 3)	+25°C		3	6		3	6		2	3		3	15	mV
	Full			9			7.5			5			20	mV
Av. Offset Voltage Drift	Full		10			10			10			10		µV/°C
Bias Current	+25°C		30	200		30	200		30	200		30	400	pA
	Full			50			7			7			10	nA
Offset Current	+25°C		5	100		5	100		5	100		5	200	pA
	Full			20			3			3			5	nA
Common Mode Range	Full	±10	±12		±10	±12		±10	±12		±10	±12		V
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}			10^{12}		MΩ
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 4)	+25°C	20K	25K		20K	25K		20K	25K		10K	25K		V/V
	Full	10K			15K			15K			5K			V/V
Common Mode Rejection Ratio (Note 5)	Full	80	86		80	86		80	86		70	76		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		±10	±12		±10	±12		V
	Full	±10			±10			±10			±10			V
Unity Gain Bandwidth (Note 6)	+25°C		1			1			1			1		MHz
Full Power Bandwidth (Note 7)	+25°C		63			63			63			63		KHz
TRANSIENT RESPONSE														
Rise Time (Note 8)	+25°C		80			80			80			80		nsec
Overshoot (Note 8)	+25°C		10			10			10			10		%
Slew Rate (Note 9)	+25°C		4			4			4			4		V/µs
Settling Time (Note 10)	+25°C		3.5			3.5			3.5			3.5		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current (Note 11)	+25°C			0.4			0.4			0.4			0.5	mA
Power Supply Rejection Ratio (Note 12)	Full	80	95		80	95		80	95		70	95		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. $R_S = 50\Omega$.
4. $R_L \geq 10K\Omega$, $V0 = \pm 10V$.
5. $\Delta V_{IN} = \pm 10V$.
6. $R_L = 10K\Omega$.
7. $R_L = 10K$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. $V_{IN} = 50mV$, $C_L = 50pF$, $R_L = 10K\Omega$.
9. $V_{IN} = 10V$, $C_L = 50pF$, $R_L = 10K\Omega$.
10. Settling time is measured to 0.1% of final value for a 10 volt output step and $A_V = -1$.
11. No load, No signal.
12. $V_{SUPP} = \pm 5V.D.C.$ to ± 15 V.D.C.

HARRIS

HA-5064 Series

Low Power, JFET Input Quad Operational Amplifiers

Preliminary

FEATURES

- LOW INPUT BIAS CURRENT 100pA
- LOW POWER DISSIPATION 24mW/Pkg.
- FAST SLEWING 4V/μs
- LOW VIO DRIFT 10μV/^{o}C
- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- GOOD CHANNEL SEPARATION 120dB
- POWER SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

WHERE DENSITY AND POWER REQUIREMENTS ARE DEMANDING:

- ACTIVE FILTERS
- SIGNAL CONDITIONING
- SIGNAL GENERATION
- INSTRUMENTATION AMPLIFIERS

DESCRIPTION

The HARRIS HA-5064 series JFET input monolithic, quad operational amplifiers feature very low power requirements coupled with excellent AC and DC characteristics. Maximum power dissipation of 24 mW/package is achieved by using complementary design, process, and layout techniques.

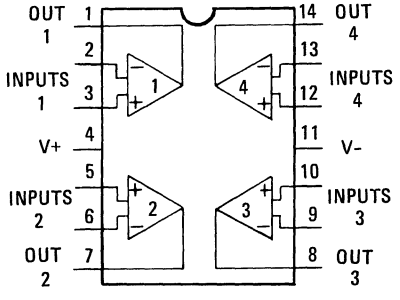
A 4V/μs slew rate coupled with 1MHz gain-bandwidth makes these devices most suitable for active filter and signal conditioning designs. The HA-5064 series is ideally suited for those applications demanding low power and high density without compromising other performance characteristics. High input impedance and low drift also makes the HA-5064 series useful as instrumentation amplifiers.

The HA-5064 is packaged in a 14-pin DIP and is pin compatible with most other quad operational amplifiers. The HA-5064-2 is specified for -55^{o}C to +125^{o}C operation while the HA-5064 A-5/HA-5064B-5/HA-5064-5 are specified over the 0^{o}C to +75^{o}C range.

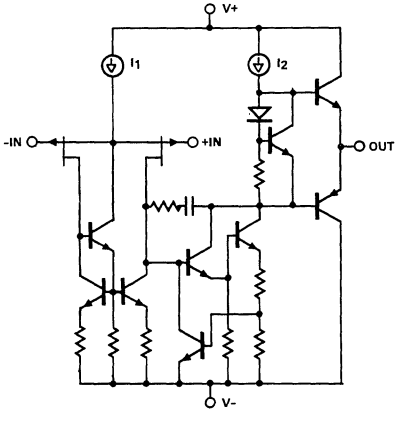
PINOUT

Section 11 for Packaging

TOP VIEW



SIMPLIFIED SCHEMATIC



ONE-FOURTH ONLY

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	40V
Differential Input Voltage (Note 2)	±30V
Output Current (Note 3)	Continuous
Internal Power Dissipation (Note 4)	500mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

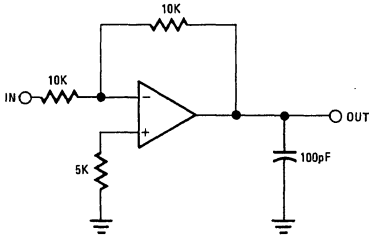
V+ = 15VDC; V- = -15VDC

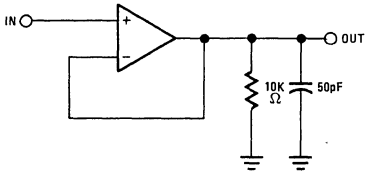
		HA-5064-2 -55°C to +125°C			HA-5064A-5 0°C to +75°C			HA-5064B-5 0°C to +75°C			HA-5064-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	+25°C		2	6		2	6		2	3			15	mV
	Full			9			7.5			5			20	mV
Offset Voltage Average Drift	Full		10			10			10			20		µV/°C
Bias Current	+25°C			200			200			200			400	pA
	Full			50			7			7			10	nA
Offset Current	+25°C			100			100			100			200	pA
	Full			20			3			3			5	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10			±10			±10			±10			V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 5)	+25°C	20K	25K		20K	25K		20K	25K		10K	25K		V/V
	Full	10K			15K			15K			5K			V/V
Common Mode Rejection Ratio (Note 6)	Full	80			80			80			70			dB
Gain Bandwidth	+25°C		1			1			1			1		MHz
Channel Separation (Note 7)	+25°C		120			120			120			120		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 8)	+25°C	±10	±12		±10	±12		±10	±12		±10	±12		V
	Full	±10			±10			±10			±10			V
Output Current (Note 9)	Full	±1			±1			±1			±1			mA
Full Power Bandwidth (Note 10)	+25°C		63			63			63			63		kHz
Output Resistance (Note 11)	+25°C		300			300			300			300		Ω
TRANSIENT RESPONSE (Note 12)														
Rise Time (10% TO 90%)	+25°C		80			80			80			80		nsec
Slew Rate	+25°C	2	4		2	4		2	4		2	4		V/µsec
Settling Time (Note 13)	+25°C		3.5			3.5			3.5			3.5		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current	+25°C			.8			.8			.8			1	mA
P. S. R. R. (Note 14)	Full	80			80			80			70			dB

NOTES

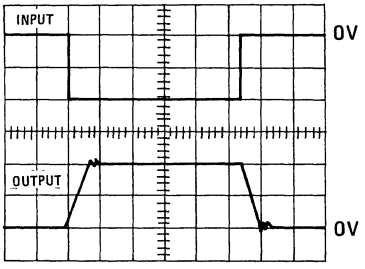
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 10KΩ
6. ΔV_{IN} = ±10V
7. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak-to-peak; R_S = 10KΩ
8. R_L = 2K ohms.
9. Output current is measured with V_{OUT} = 10 volts.
10. R_L = 10K; Full power bandwidth guaranteed, based on slew rate measurement using FPBW = $\frac{\text{SLEW RATE}}{2\pi V_{PEAK}}$
11. Output resistance measured under open loop conditions.
12. Refer to Test Circuits section of the data sheet.
13. Settling Time is measured to 0.1% of final value for a 10 volt output step and A_V = -1.
14. V_{SUPP} = +5VDC to +15VDC.

TEST CIRCUITS

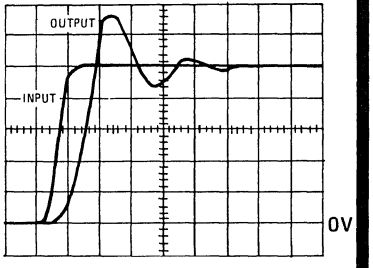




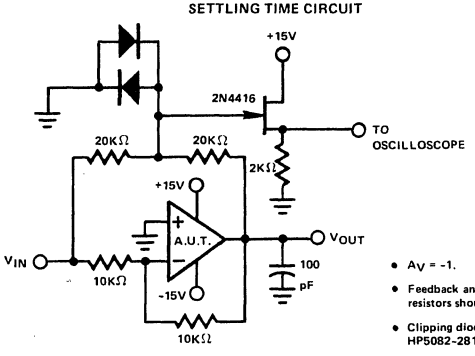
LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5μs/Div.)



SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.)



SETTLING TIME CIRCUIT



- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

HARRIS

HA-5082 Series

JFET Input Dual Operational Amplifiers

Preliminary

2

FEATURES

- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- LOW INPUT BIAS CURRENT 200pA
- LOW INPUT OFFSET CURRENT 100pA
- LOW POWER CONSUMPTION TYPICAL SUPPLY CURRENT 3.5mA
- HIGH SLEW RATE 15V/μs
- PIN COMPATIBLE WITH LM1458
- DIRECT REPLACEMENT FOR TL082

APPLICATIONS

- ACTIVE FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- SIGNAL CONDITIONING

DESCRIPTION

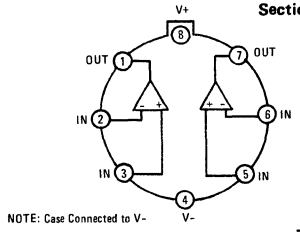
The HARRIS HA-5082 operational amplifiers are a series of dual monolithic JFET-input amplifiers featuring low input bias and offset currents, high input impedance and, high slew rate. In addition to being a direct replacement for the TL082 series, the HA-5082 series offers improved performance with an input offset voltage of 2mV, a slew rate of 15V/μs, and bandwidths of 4MHz.

This improved performance is a result of the HARRIS FET/Bipolar technology and makes the HA-5082 series of amplifiers ideally suited for applications in industrial control, communication, and computer peripheral equipment.

The HA-5082-2 is characterized for operation over the full military temperature range of -55°C to +125°C. The HA-5082A-5, HA-5082B-5 and HA-5082-5 are all characterized over the commercial temperature range of 0°C to +75°C.

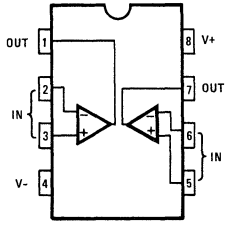
PINOUT

Section 11 for Packaging

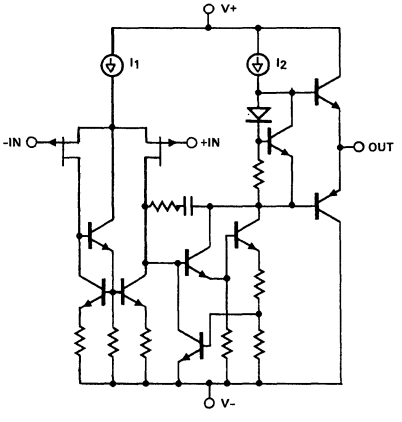


NOTE: Case Connected to V-

TOP VIEWS



SIMPLIFIED SCHEMATIC



(ONE HALF ONLY)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals	±20V	Power Dissipation	600mW*
Differential Input Voltage	±40V	Operating Temperature Range:	
Input Voltage (Note 2)	±15.0V	HA-5082-2	$-55^oC \leq T_A \leq +125^oC$
Output Short Circuit Duration	Indefinite	HA-5082-5	$0^oC \leq T_A \leq +75^oC$
		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

* To-99 Derate by 6.75mW/°C above +85°C
Dip Derate by 5.57mW/°C above +65°C

ELECTRICAL CHARACTERISTICS

V+ = 15V V- = -15V
Parameters are guaranteed at indicated ambient temperature after warm-up.

		HA-5082-2 -55°C to +125°C			HA-5082A-5 0°C to 75°C			HA-5082B-5 0°C to 75°C			HA-5082-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage (Note 3)	+25°C		3	5		3	5			2		5	15	mV
	Full			8			7			4			20	mV
Av. Offset Voltage Drift	Full		10			10			10			10		µV/°C
Bias Current	+25°C		30	200		30	200		30	200		30	400	pA
	Full			50			8			4			10	nA
Offset Current	+25°C		5	100		5	100		5	100		5	200	pA
	Full			20			4			2			5	nA
Common Mode Range	Full	±10	±12		±10	±12		±10	±12		±10	±12		V
Input Resistance	+25°C		10^{12}			10^{12}				10^{12}		10^{12}		MΩ
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 4)	+25°C	50K	200K		50K	200K		50K	200K		25K	200K		V/V
	Full	15K			25K			25K			15K			V/V
Common Mode Rejection Ratio (Note 5)	+25°C	80	86		80	86		80	86		70	76		dB
Unity Gain Bandwidth	+25°C		4			4			4			4		MHz
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		±10	±12		±10	±12		V
	Full	±10			±10			±10			±10			V
Output Current (Note 7)	Full	±5			±5			±5			±5			mA
Full Power Bandwidth (Note 8)	+25°C		240			240			240			240		KHz
TRANSIENT RESPONSE														
Rise Time (Note 9)	+25°C		60			60			60			60		nsec
Overshoot (Note 9)	+25°C		10			10			10			10		%
Slew Rate (Note 10)	+25°C		15			15			15			15		V/µs
Settling Time (Note 11)	+25°C		2			2			2			2		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current (Note 12)	+25°C		3.5	5.6		3.5	5.6		3.5	5.6		3.5	5.6	mA
Power Supply Rejection Ratio (Note 13)	+25°C	80	86		80	86		80	86		70	76		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. $R_S = 50\Omega$.
4. $R_L \geq 10K\Omega$, $V0 = \pm 10V$.
5. $\Delta V_{IN} = \pm 10V$.
6. $R_L = 2K\Omega$.
7. $V_{OUT} = \pm 10V$
8. $R_L = 2K$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$.
9. $V_{IN} = 50mV$, $C_L = 100pF$, $R_L = 2K\Omega$.
10. $V_{IN} = 10V$, $C_L = 100pF$, $R_L = 2K\Omega$.
11. Settling time is measured to 0.1% of final value for a 10 volt output step and $A_V = -1$.
12. No load, No signal.
13. $V_{SUPP} = \pm 5V$.D.C. to ±15 V.D.C.

HARRIS

HA-5084 Series

JFET Input Quad Operational Amplifiers

Preliminary

2

FEATURES

- LOW INPUT BIAS CURRENT 200pA
- HIGH SLEW RATE 15V/μs
- WIDE BANDWIDTH 4MHz
- LOW DRIFT 10μV/^{o}C
- HIGH INPUT IMPEDANCE $10^{12}\Omega$
- LOW SUPPLY CURRENT 7.2mA
- SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

- HIGH Q, WIDEBAND FILTERS
- INTEGRATORS
- TONE DETECTORS
- SAMPLE/HOLD CIRCUITS
- DATA ACQUISITION SYSTEMS
- ABSOLUTE VALUE CIRCUITS

DESCRIPTION

The Harris HA-5084 is a JFET input, monolithic, quad operational amplifier featuring low input bias and offset currents, high input impedance, and high slew rate. Manufactured using FET/Bipolar technology coupled with advanced layout considerations, these devices also feature excellent channel separation and offset voltage drift specifications.

High slew rate (15V/μs) coupled with excellent input bias (30pA) and offset current (3pA) make the HA-5084 ideally suited for high speed analog designs such as integrators, fast D/A converters, and sample-and-hold circuits.

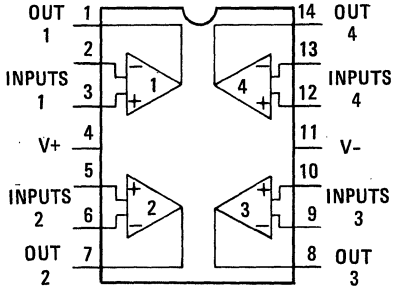
The HA-5084 is available in ceramic and plastic 14 pin DIP's and is pin compatible with the LM324, LM348, and MC3403 quad operational amplifier pinout.

The HA-5084-2 is specified from -55^{o}C to +125^{o}C while the HA-5084-5 operates from 0^{o}C to +75^{o}C.

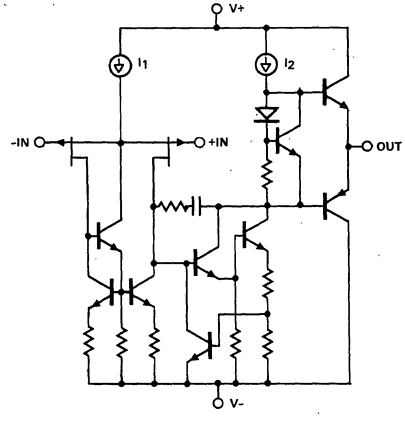
PINOUT

Section 11 for Packaging

TOP VIEW



SIMPLIFIED SCHEMATIC



(ONE FOURTH ONLY)

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	40V
Differential Input Voltage (Note 2)	±40V
Output Current (Note 3)	Full Short Circuit Protection
Internal Power Dissipation (Note 4)	500mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

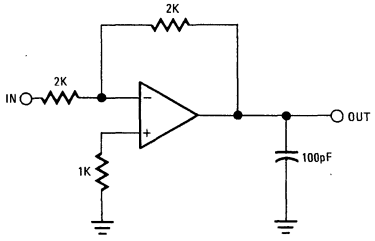
V+ = 15VDC; V- = -15VDC

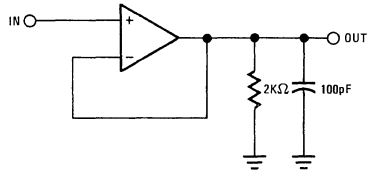
		HA-5084-2 -55°C to +125°C			HA-5084A-5 0°C to +75°C			HA-5084B-5 0°C to +75°C			HA-5084-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	+25°C			5			5			2			15	mV
	Full			8			7			4			20	mV
Offset Voltage Average Drift	Full		8.3			8.3			8.3			8.3		µV/°C
Bias Current	+25°C			200			200			200			400	pA
	Full			50			8			4			10	nA
Offset Current	+25°C			100			100			100			200	pA
	Full			20			4			2			5	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10			±10			±10			±10			V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 5)	+25°C	25K			50K			50K			25K			V/V
	Full	15K			25K			25K			15K			V/V
Common Mode Rejection Ration (Note 6)	Full	70			80			80			70			dB
Unity Gain Bandwidth	+25°C		4			4			4			4		MHz
Channel Separation (Note 7)			-120			-120			-120			-120		dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note8)	+25oC	10			10			10			10			V
	Full	10			10			10			10			V
Output Current (Note 9)	Full	±5			±5			±5			±5			mA
Full Power Bandwidth (Note 10)	+25°C		240			240			240			240		kHz
Output Resistance (Note 11)	+25°C		300			300			300			300		Ω
TRANSIENT RESPONSE (Note 12)														
Rise Time	+25oC		60			60			60			60		nsec
Slew Rate	+25°C		15			15			15			15		V/µsec
Settling Time (Note 13)	+25°C		2			2			2			2		µsec
POWER SUPPLY CHARACTERISTICS														
Supply Current	+25°C		7.2	11		7.2	11		7.2	11		7.2	12	mA
P. S. R. R. (Note 14)	Full	80			80			80			70			dB

NOTES

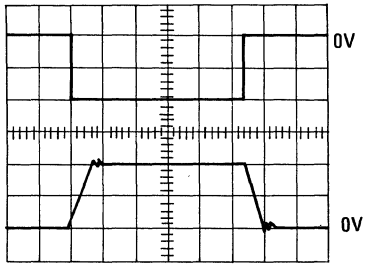
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V; R_L = 10KΩ.
6. ΔV_{IN} = ±10V
7. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak-to-peak; R_S = 1K ohms.
8. R_L = 2K ohms.
9. Output current is measured with V_{OUT} = 10 volts.
10. R_L = 2K; Full power bandwidth guaranteed, based on slew rate measurement using FPBW = $\frac{\text{SLEW RATE}}{2\pi V_{PEAK}}$
11. Output resistance measured under open loop conditions.
12. Refer to Test Circuits section of the data sheet.
13. Settling Time is measured to 0.1% of final value for a 10 volt output step and A_V = -1.
14. V_{SUPP} = ±5V.D.C. to ±15V.D.C.

TEST CIRCUITS



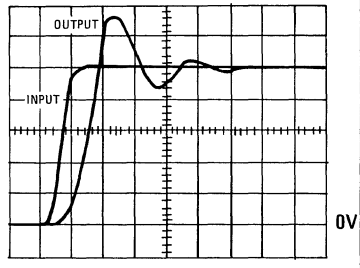


LARGE SIGNAL RESPONSE CIRCUIT (Volts: 5V/Div., Time: 5μs/Div.)



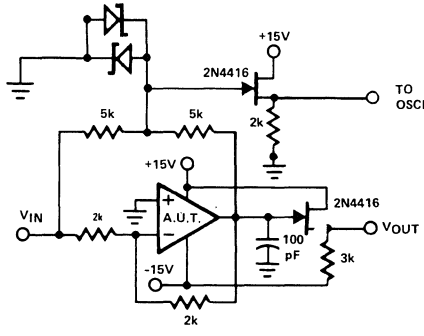
VERT. 5V/DIV.
HORZ. 5 μs/DIV.

SMALL SIGNAL RESPONSE CIRCUIT (Volts: 10mV/Div., Time: 50ns/Div.)



HORIZONTAL: 50 NSEC/DIV.
VERTICAL: 10mV/DIV

SETTLING TIME CIRCUIT



- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

HA-5100/5105

Wideband, JFET Input Operational Amplifier

FEATURES

- LOW INPUT OFFSET VOLTAGE 0.5mV
- LOW OFFSET DRIFT . . . . . 5μV/^{o}C
- LOW INPUT BIAS CURRENT 50pA
- LARGE VOLTAGE GAIN . . . . . 150K V/V
- WIDE BANDWIDTH 18MHz
- HIGH SLEW RATE 8V/μsec
- FAST LARGE SIGNAL SETTLING TIME: 1.7μsec

APPLICATIONS

- PRECISION, HIGH SPEED, DATA ACQUISITION SYSTEMS
- PRECISION SIGNAL GENERATION
- PULSE AMPLIFICATION

GENERAL DESCRIPTION

The HA-5100/5105 are monolithic wideband operational amplifiers manufactured with FET/Bipolar technologies and dielectric isolation. Precision laser trimming of the input stage complements the amplifier high frequency capabilities with excellent input characteristics.

The HA-5100/5105 offer a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics the Harris devices have quite constant slew rate, bandwidth, and settling characteristics over the operating range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. The slewing waveform is symmetrical to provide reduced distortion. Note also that Harris specifies all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

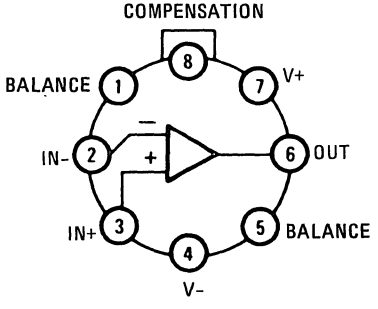
Complementing HA-5100/5105's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and extremely high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications.*

* -2 denotes a range of -55^{o}C to +125^{o}C and -5 denotes a 0^{o}C to +75^{o}C range.

PINOUT

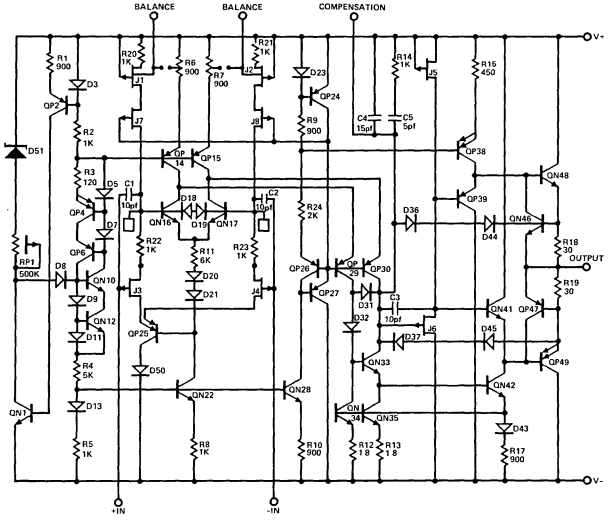
Section 11 for Packaging

TOP VIEW



CASE CONNECTED TO V-

SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	40V
Differential Input Voltage	±40V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	510mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

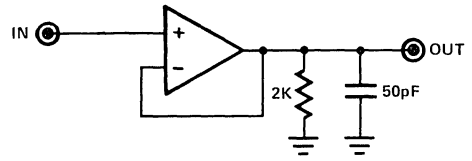
		HA-5100-2 -55°C to +125°C			HA-5100-5 0°C to +75°C			HA-5105-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	1.0		0.5	1.0		0.5	1.5	mV
	Full		0.50	2.0		0.50	2.0		0.75	3.5	mV
Offset Voltage Average Drift	Full		5			10			15		µV/°C
Bias Current	+25°C		20	50		20	50		50	100	pA
	Full		5	10			10		10	20	nA
Offset Current	+25°C		2	10		2	10		5	50	pA
	Full		2	5		2	5		5	10	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±10.5		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		50K	100K		V/V
	Full	60K	100K		60K	100K		40K	80K		V/V
Common Mode Rejection Ratio (Note 4)	Full	80	86		80	86		80	86		dB
Gain Bandwidth Product at A_V = 10	Full		18			18			18		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±12	±13		±12	±13		±11	±12		V
	Full	±12	±13		±12	±13		±11	±12		V
Short Circuit Output Current (Note 6)	Full	±10	±15		±10	±15		±8	±15		mA
Full Power Bandwidth (Note 7)	+25°C	90	150		90	150		75	125		kHz
Output Resistance (Note 8)	+25°C		30			30			40		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time	+25°C		15	35		15	35		20		nsec
Slew Rate	+25°C	6	8		6	8		5	8		V/µsec
Settling Time (Note 10)	+25°C		1.7			1.7			2.0		µsec
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full		5	7		5	7		6	8	mA
P.S.R.R. (Note 11)	Full	80	86		80	86		80	86		dB

NOTES:

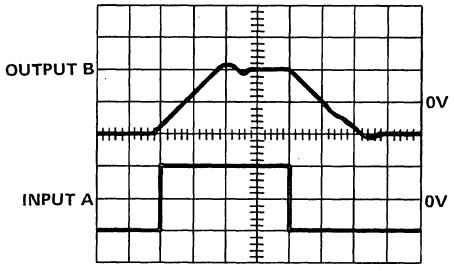
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8 mW/°C for operation at ambient temperatures above +75°C.
3. $V_{OUT} = \pm 10V$; $R_L = 2K$.
4. $V_{CM} = \pm 10V$ D.C.
5. $R_L = 10K$.
6. $V_{OUT} = 0V$.
7. $R_L = 2K$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$.
8. Output resistance measured under open loop conditions.
9. Refer to test circuits section of the data sheet.
10. Settling time is measured to 0.1% of final value for a 10 volt output step and $A_V = -1$.
11. $V_{SUPP} = \pm 10V$ D.C. to $\mp 20V$ D.C.

TEST CIRCUITS

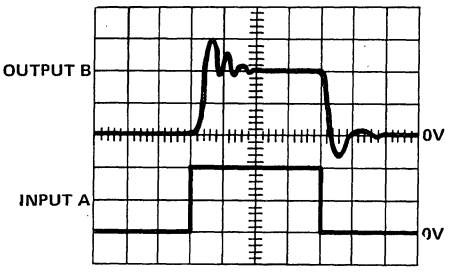
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



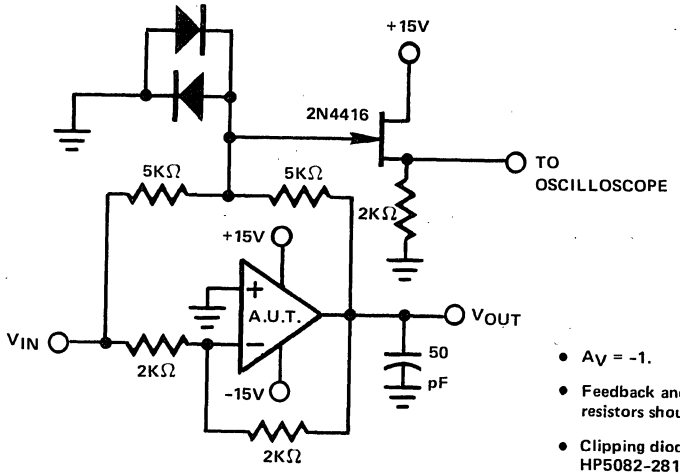
LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: 5V/Div.)
Horizonal Scale: (Time: 500ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: 100mV/Div.)
Horizonal Scale: (Time: 100ns/Div.)



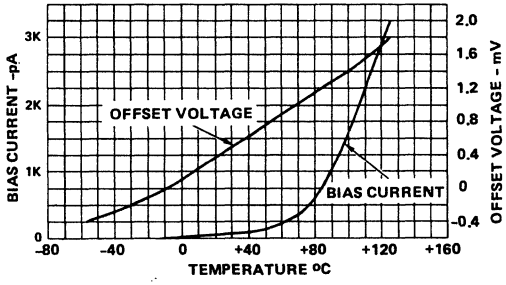
SETTLING TIME CIRCUIT



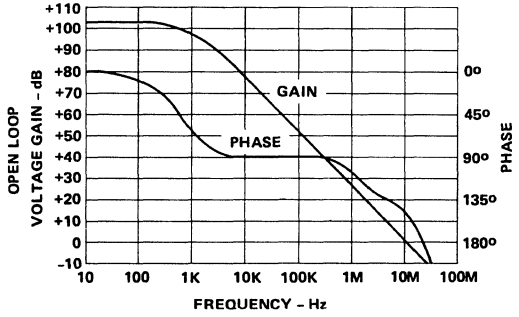
- $A_V = -1$.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

$V+ = +15V$, $V- = -15V$, $T_A = +25^oC$ UNLESS OTHERWISE STATED.

INPUT OFFSET VOLTAGE AND BIAS CURRENT VS TEMPERATURE

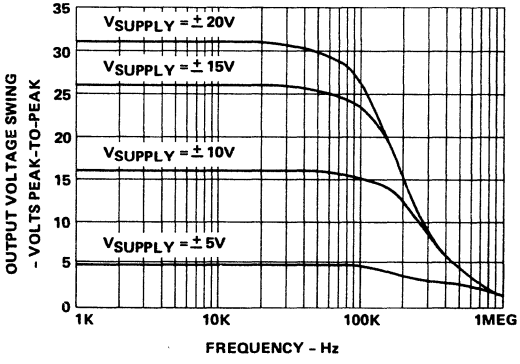


OPEN LOOP FREQUENCY RESPONSE

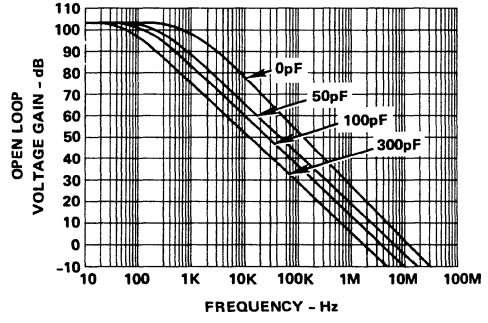


2

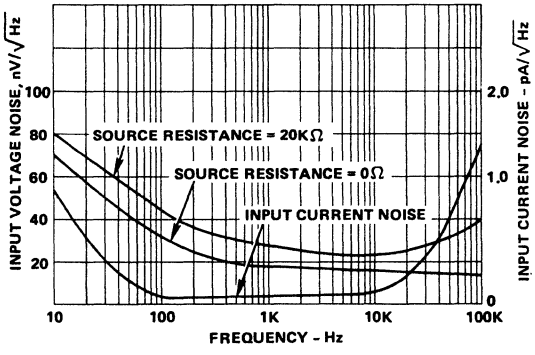
OUTPUT VOLTAGE SWING VS FREQUENCY



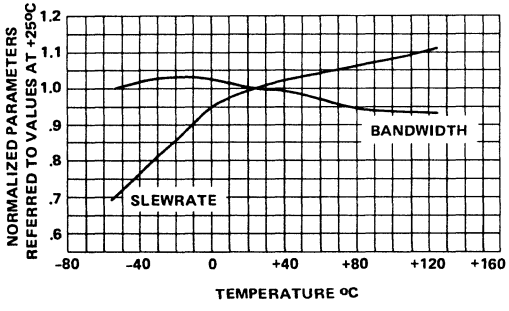
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS COMPENSATION CAPACITORS



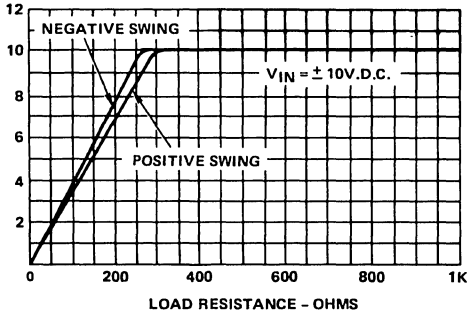
INPUT VOLTAGE AND CURRENT NOISE VS FREQUENCY



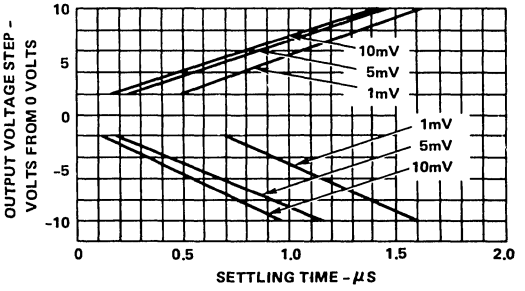
NORMALIZED AC PARAMETERS VS TEMPERATURE



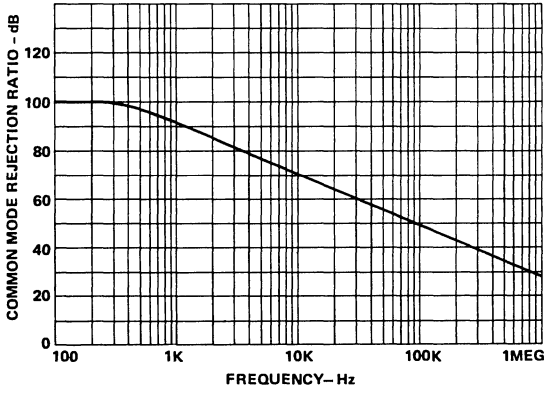
OUTPUT VOLTAGE SWING
VS LOAD RESISTANCE



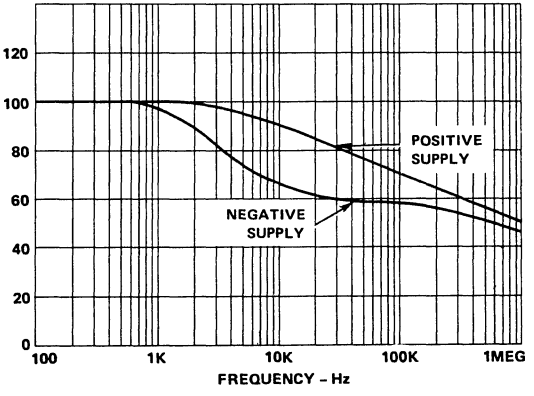
SETTLING TIME FOR VARIOUS
OUTPUT STEP VOLTAGES



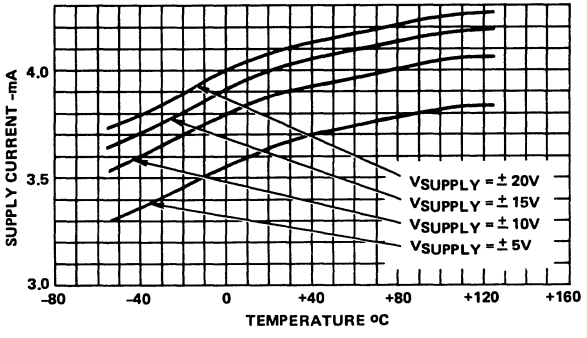
COMMON MODE REJECTION
RATIO VS FREQUENCY



POWER SUPPLY REJECTION
RATIO VS FREQUENCY



POWER SUPPLY CURRENT
VS TEMPERATURE

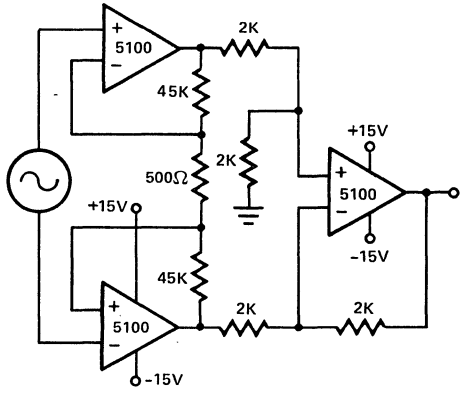


2

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. STABILITY CONSIDERATIONS: In applications where large value feedback resistors are used, a small capacitor ($\approx$ 3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by the input capacitance.
3. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads ($\geq$ 100pF) a small resistor ($\approx$100Ω) should be connected in series with the output and inside the feedback loop.
4. OFFSET VOLTAGE NULLING: Offset nulling, if required, is accomplished with a 100KΩ pot between pins 1 and 5; wiper to V+. Alteration of initial offset voltage may affect the temperature coefficient of the offset voltage.

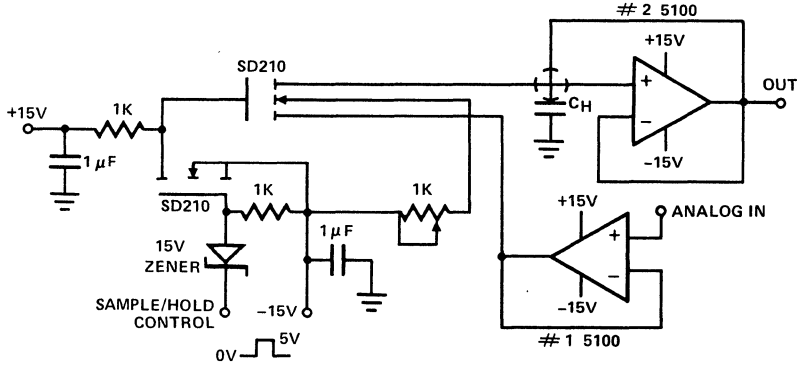
APPLICATIONS

PRECISION INSTRUMENTATION AMPLIFIER (A_V = 100)



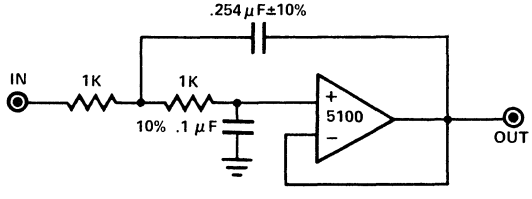
Experimental Results
Yielded 80dB CMRR.
V_{IO} drift < 20μV/°C.

PRECISION/FAST SAMPLE/HOLD CIRCUIT



Experimental Results:
V_{IN} = 10 volt step
C_H = 1000pF
Acquisition Time = 0.4μs (0.1%)
Charge Injection = 30pC
Drift Current = 320pA
Switching Spikes $\approx$ 200mV

1kHz SALLEN AND KEY FILTER



Experimental Results:
F_C = 1KHz
Q = 20
-3dB $\approx$ 1.1KHz
-20dB $\approx$ 3.4KHz

HARRIS

HA-5110/5115

Wideband, JFET Input, Uncompensated, Operational Amplifier

FEATURES

- WIDE GAIN BANDWIDTH 60MHz
- HIGH SLEW RATE 50V/μs
- SETTLING TIME 850ns
- POWER BANDWIDTH 800KHz
- OFFSET VOLTAGE 0.5mV
- BIAS CURRENT 50pA

APPLICATIONS

- VIDEO AND RF AMPLIFIERS
- DATA ACQUISITION
- PULSE AMPLIFIERS
- PRECISION SIGNAL GENERATION

DESCRIPTION

HA-5110/5115 are wideband, uncompensated, operational amplifiers manufactured with FET/Bipolar technologies and dielectric isolation. These monolithic amplifiers feature superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. These devices are controlled at closed loop gains greater than 10 without compensation.

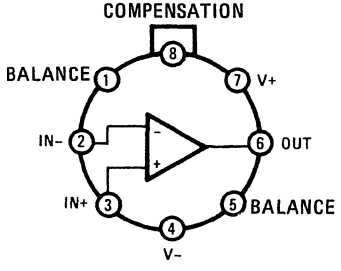
With excellent dynamic and input characteristics, HA-5110/5115 are well suited for many wideband, pulse, and video applications. These amplifiers are ideal components for video and RF circuitry requiring up to 60MHz gain-bandwidth-product and 800KHz power bandwidth. 50V/μs slew rate and 850ns settling time make these devices useful in pulse amplification and data acquisition designs. HA-5110/5115's 0.5mV offset voltage, 10pA offset current, and extremely high impedance coupled with excellent AC parameters make these amplifiers ideal selections for accurate signal conditioning designs. For applications requiring less critical input characteristics, HA-5115 is available in untrimmed form.

HA-5110/5115 are available in metal can (TO-99) packages. Suffix -2 denotes a range to -55°C to +125°C and -5 denotes a 0°C to +75°C range.

PINOUT

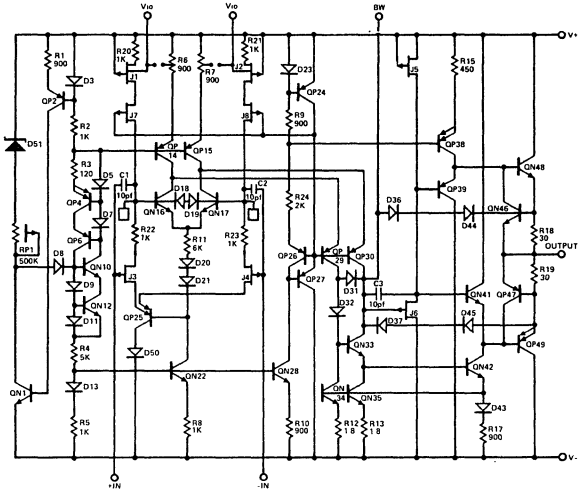
Section 11 for Packaging

TOP VIEW



CASE CONNECTED TO V-

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^-	40V	Internal Power Dissipation (Note 2)	510mW
Differential Input Voltage	±40V	Storage Temperature Range	-65°C to +150°C
Peak Output Current	Full Short Circuit Protection		

ELECTRICAL CHARACTERISTICS

V+ = 15VDC; V- = -15VDC
Parameters are guaranteed at indicated ambient temperature after warm-up.

		HA-5110-2 -55°C to +125°C			HA-5110-5 0°C to +75°C			HA-5115-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	1.0		0.5	1.0		0.5	1.5	mV
	Full		0.50	2.0		0.50	2.0		0.75	3.5	mV
Offset Voltage Average Drift	Full		5			10			15		µV/°C
Bias Current	+25°C		20	50		20	50		50	100	pA
	Full		5	10			10		10	20	nA
Offset Current	+25°C		2	10		2	10		5	50	pA
	Full		2	5		2	5		5	10	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±10.5		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		50K	100K		V/V
	Full	60K	100K		60K	100K		40K	80K		V/V
Common Mode Rejection Ratio (Note 4)	Full	80	86		80	86		80	86		dB
Gain Bandwidth Product (A_V = 10)	Full		60			60			50		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±12	±13		±12	±13		±11	±12		V
	Full	±12	±13		±12	±13		±11	±12		V
Output Current (Note 6)	+25°C	±10	±15		±10	±15		±8	±15		mA
Full Power Bandwidth (Note 7)	+25°C	550	625		550	625		550	625		kHz
Output Resistance (Note 8)	+25°C		30			30			40		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time (A_V = 10)	+25°C		20			20			20		nsec
Slew Rate (A_V = 10)	+25°C	35	50		35	50		35	40		V/µsec
Settling Time (Note 10)	+25°C		.85			.85			1.0		µsec
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full		5	7		5	7		6	8	mA
Power Supply Rejection Ratio (Note 11)	+25°C	80	94		80	94		80	94		dB

NOTES:

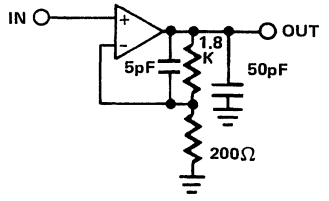
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. V_{OUT} = ±10V. R_L = 2K
4. V_{CM} = ±10 V.D.C.
5. R_L = 10K
6. V_{OUT} = 0V
7. R_L = 2K; Full power bandwidth guaranteed, based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. Output resistance measured under open loop conditions.
9. Refer to Test Circuits section of the data sheet.
10. Settling Time is measured to 0.1% of final value for a 10 volt output step and A_V = -10.
11. V_{SUPP} = ±10 V.D.C. to ±20 V.D.C.

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. $V_{OUT} = \pm 10V$. $R_L = 2K$
4. $V_{CM} = \pm 10$ V.D.C.
5. $R_L = 10K$
6. $V_{OUT} = 0V$
7. $R_L = 2K$; Full power bandwidth guaranteed, based on slew rate measurement using $FPBW = \frac{\text{SLEW RATE}}{2\pi V_{PEAK}}$
8. Output resistance measured under open loop conditions.
9. Refer to Test Circuits section of the data sheet.
10. Settling Time is measured to 0.1% of final value for a 10 volt output step and $A_V = -10$.
11. $V_{SUPP} = \pm 10$ V.D.C. to ∓ 20 V.D.C.

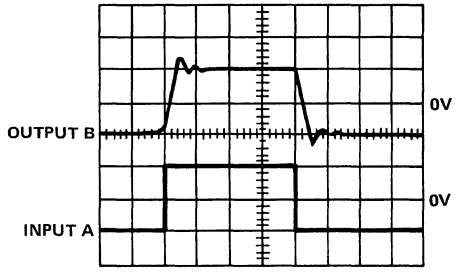
TEST CIRCUITS

LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



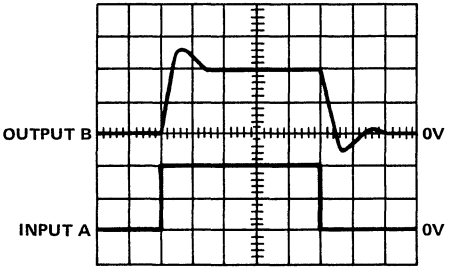
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A=.5V/Div,B=5V/Div.)
Horizontal Scale: (Time: 500ns/Div.)

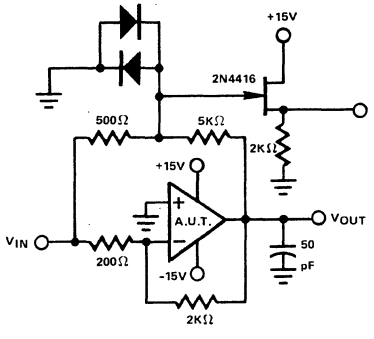


SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: A=10mV/Div., B=100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)



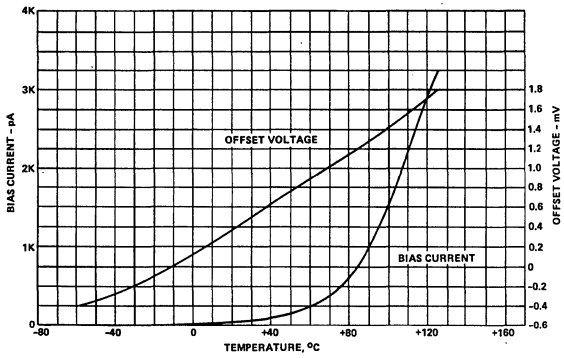
SETTLING TIME CIRCUIT



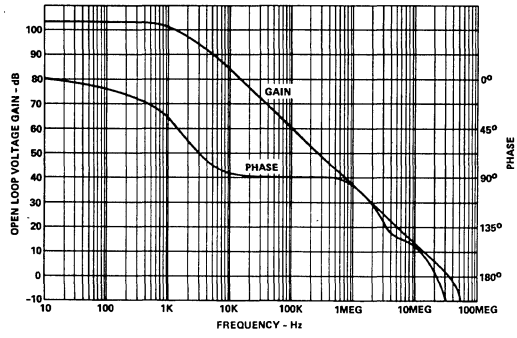
- $A_V = -1$.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

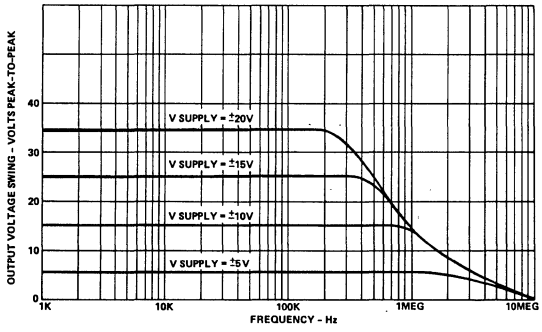
INPUT OFFSET VOLTAGE AND BIAS CURRENT VS TEMPERATURE



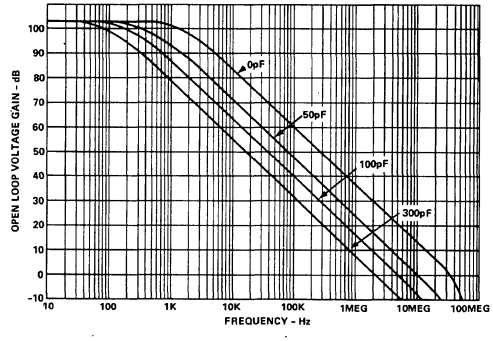
OPEN LOOP FREQUENCY RESPONSE



OUTPUT VOLTAGE SWING VS FREQUENCY

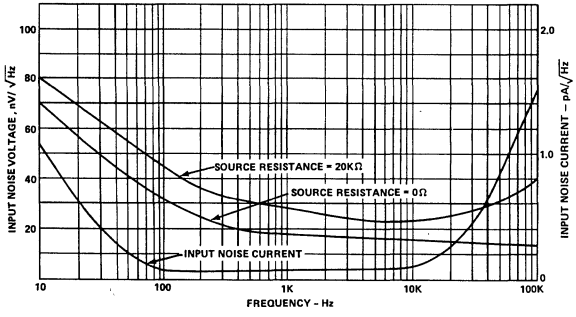


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS COMPENSATION CAPACITORS

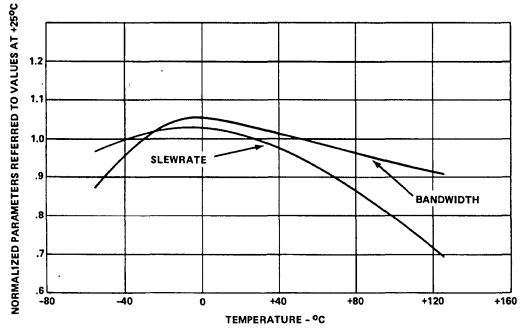


NOTE: External compensation components are not required for closed loop gains > 10, but may be added to reduce bandwidth if desired.

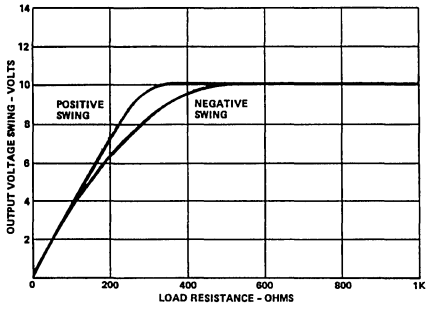
INPUT NOISE VOLTAGE AND NOISE CURRENT VS FREQUENCY



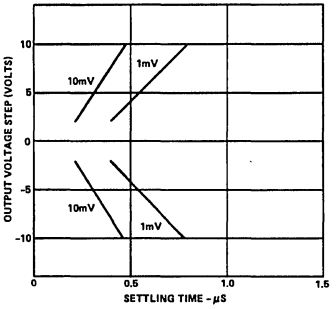
NORMALIZED AC PARAMETERS VS TEMPERATURE



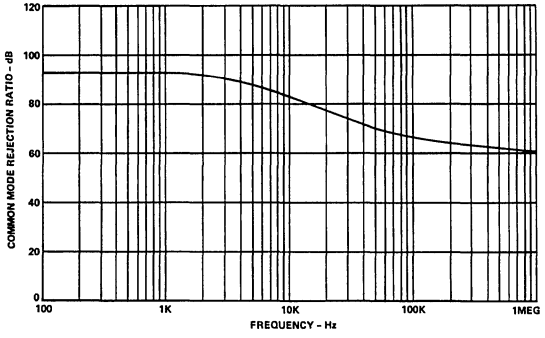
OUTPUT VOLTAGE SWING VS LOAD RESISTANCE



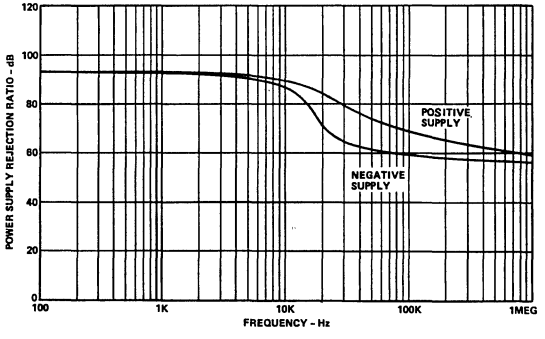
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



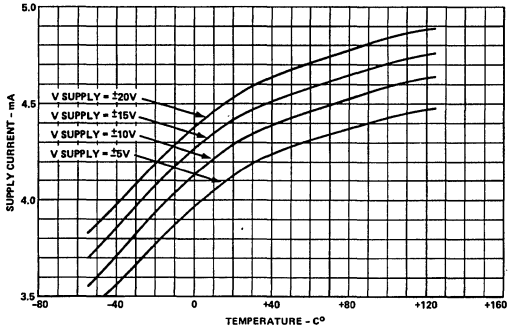
COMMON MODE REJECTION RATIO VS FREQUENCY



POWER SUPPLY REJECTION RATIO VS FREQUENCY



POWER SUPPLY CURRENT VS TEMPERATURE



2

APPLYING THE HA-5110/5115

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01 μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. STABILITY CONSIDERATIONS: In applications where large value feedback resistors are used, a small compacitor ($\approx$ 3pF) may be needed in parallel with the feedback resistor to neutralize the pole introduced by the input capacitance.

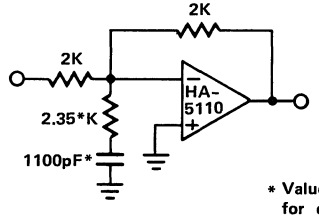
3. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads ($\geq$ 100pF) a small capacitor ($\approx$ 10pF) should be connected in parallel with the feedback resistor.

4. OFFSET VOLTAGE NULLING: Offset nulling, if required, is accomplished with a 100KΩ pot between pins 1 and 5; wiper to V+. Alteration of initial offset voltage may affect the temperature coefficient of the offset voltage.

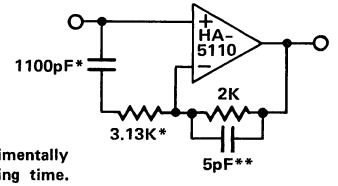
APPLICATIONS

SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY

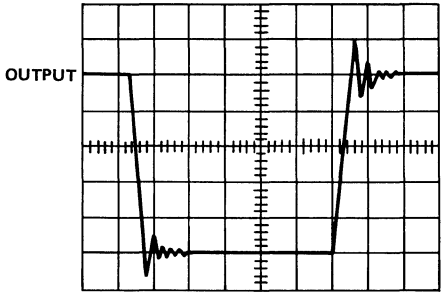
INVERTING

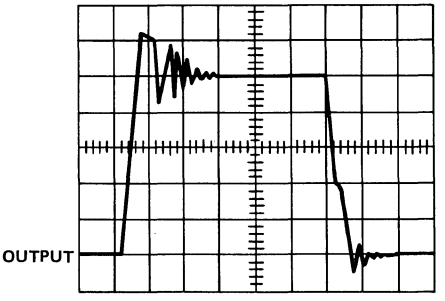


NON-INVERTING



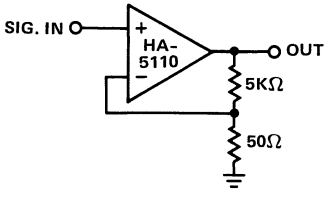
* Values were determined experimentally for optimum speed and settling time.
** Optional



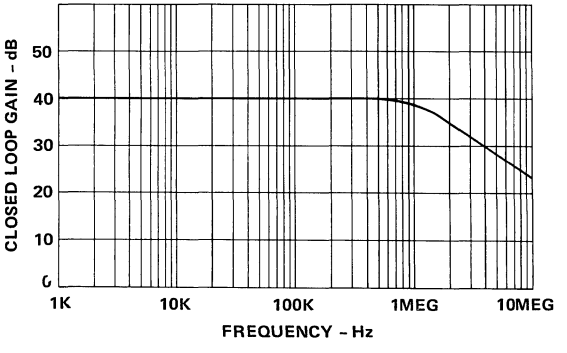


Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 500ns/Div.)

40dB, 1MHz BANDWIDTH AMPLIFIER



CLOSED LOOP FREQUENCY RESPONSE (A_V = 100)



HARRIS

HA-5130/5135

Precision Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE — 25μV
- LOW OFFSET VOLTAGE DRIFT — 0.4μV/^{o}C
- LOW NOISE — 9nV/$\sqrt{Hz}$
- OPEN LOOP GAIN — 10^7
- BANDWIDTH (UNITY GAIN) — 2.5MHz
- ALL BIPOLAR CONSTRUCTION

APPLICATIONS

- HIGH GAIN INSTRUMENTATION
- PRECISION DATA ACQUISITION
- PRECISION INTEGRATORS
- BIOMEDICAL AMPLIFIERS
- PRECISION THRESHOLD DETECTORS

DESCRIPTION

HA-5130/5135 are precision operational amplifiers manufactured using a combination of key technological advancements to provide outstanding input characteristics.

A Super Beta input stage is combined with laser trimming, dielectric isolation, and matching techniques to produce 25μV (Max.) input offset voltage and 0.4μV/^{o}C input offset voltage average drift. Other features enhanced by this process include 9nV (Typ.) Input Noise Voltage, 1nA Input Bias Current, and 140dB Open Loop Gain.

These features coupled with 120dB CMRR and PSRR make HA-5130/5135 an ideal device for precision DC instrumentation amplifiers. Excellent input characteristics in conjunction with 2.5MHz bandwidth and 0.8V/μs slew rate, makes this amplifier extremely useful for precision integrator and biomedical amplifier designs. These amplifiers are also well suited for precision data acquisition and for accurate threshold detector applications.

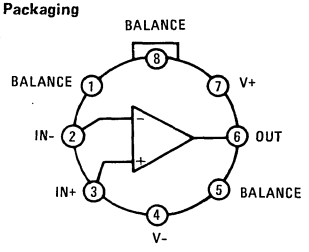
HA-5130/35 is packaged in an 8 pin (TO-99) can and an 8 lead Cerdip and is pin compatible with many existing op amp configurations.

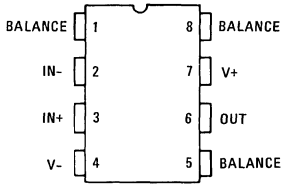
HA-5130/5135-2 is specified for -55^{o}C to +125^{o}C operation while HA-5130/5135-5 operate from 0^{o}C to +75^{o}C.

PINOUT

Section 11 for Packaging

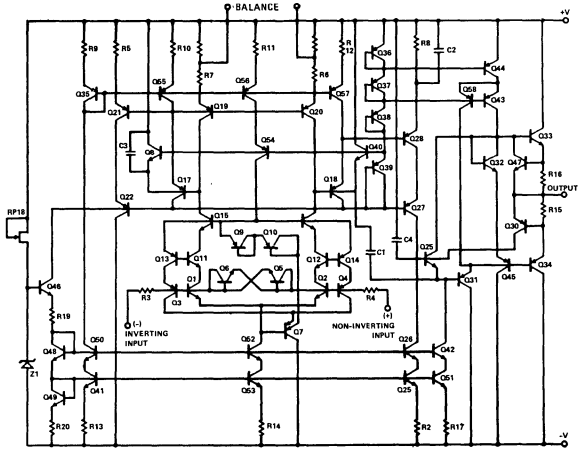
TOP VIEW





* Pins 5 and 8 are internally connected

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated		Power Dissipation (Note 2)	300mW
Voltage Between V+ and V- Terminals	40.0V	Operating Temperature Range	
Differential Input Voltage	± 15.0V	HA-5130/5135-2	$-55°C \leq T_A \leq +125°C$
		HA-5130/5135-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

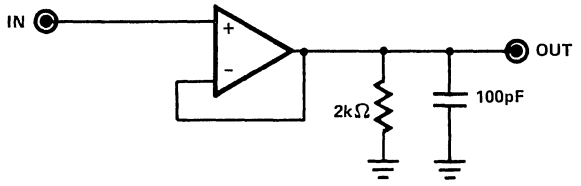
ELECTRICAL CHARACTERISTICS V+ = 15V, V- = -15V

PARAMETER	TEMP.	HA-5130-2/-5 MIN.	HA-5130-2/-5 TYP.	HA-5130-2/-5 MAX.	HA-5135-2/-5 MIN.	HA-5135-2/-5 TYP.	HA-5135-2/-5 MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		10	25		10	75	µV
	Full		50	60		50	130	µV
Average Offset Voltage Drift	Full		0.4	0.6		0.4	1.3	µV/°C
Bias Current	+25°C		± 1	± 2		± 1	± 4	nA
	Full			± 4			± 6	nA
Bias Current Average Drift	Full		0.02	0.04		0.02	0.04	nA/°C
Offset Current	+25°C			2			4	nA
	Full			4			5.5	nA
Offset Current Average Drift	Full		0.02	0.04		0.02	0.04	nA/°C
Common Mode Range	Full	± 12			± 12			V
Differential Input Resistance	+25°C	20	30		20	30		MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 3)	+25°C			0.6			0.6	μV_{p-p}
Input Noise Voltage Density (Note 3)	+25°C							$nV/\sqrt{Hz}$
f_O = 10Hz			13.0	18.0		13.0	18.0	
f_O = 100Hz			10.0	13.0		10.0	13.0	
f_O = 1000Hz			9.0	11.0		9.0	11.0	
Input Noise Current (Note 3) 0.1Hz to 10Hz	+25°C		15	30		15	30	pA_{p-p}
Input Noise Current Density (Note 3)	+25°C							$pA/\sqrt{Hz}$
f_O = 10Hz			0.4	0.8		0.4	0.8	
f_O = 100Hz			0.17	0.23		0.17	0.23	
f_O = 1000Hz			0.14	0.17		0.14	0.17	
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	120	140		120	140		dB
	Full	120			120			dB
Common Mode Rejection Ratio (Note 5)	Full	110	120		106	120		dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	0.6	2.5		0.6	2.5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	± 10	± 12		± 10	± 12		V
	Full	± 10			± 10			V
Full Power Bandwidth (Note 7)	+25°C	8	10		8	10		kHz
Output Current (Note 8)	+25°C	± 25	± 30		± 25	± 30		mA
Output Resistance (Note 9)	+25°C		45			45		Ω
TRANSIENT RESPONSE (Note 10)								
Rise Time	+25°C		340			340		ns
Slew Rate	+25°C	0.5	0.8		0.5	0.8		V/µs
Settling Time (Note 11)	+25°C		11			11		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		1.0	1.3		1.0	1.7	mA
Power Supply Rejection Ratio (Note 12)	Full	100	130		94	130		dB

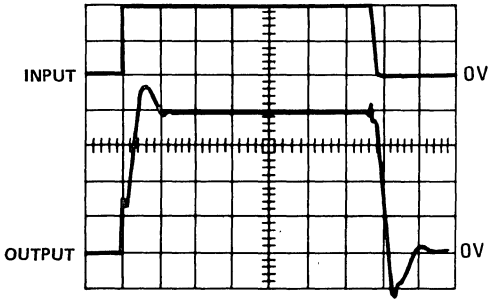
NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temp.'s above +75°C.
3. Not tested. 90% of units meet or exceed these specifications.
4. $V_{OUT} = \pm 10V$; $R_L = 2k$. Gain dB = 20 $\log_{10}$ Average
   ∴ 120dB = 1000V/mV
   140dB = 10,000V/mV
5. $V_{CM} = \pm 10V$ DC
6. $R_L = 600\Omega$
7. R_L = 2k; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. V_{OUT} = 10V
9. Output resistance measured under open loop conditions (f = 100Hz)
10. Refer to test circuits section of the data sheet.
11. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
12. $V_{SUPP} = \pm 5V$ DC to $\pm 20V$ DC.

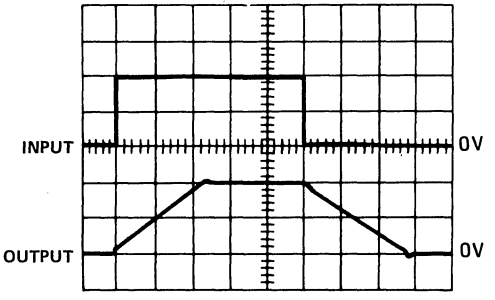
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



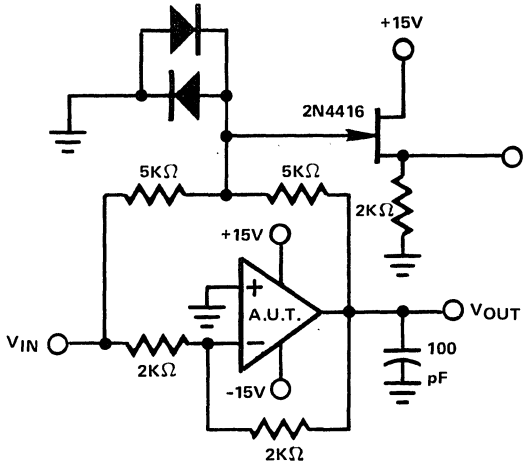
SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: 50mV/Div. Output)
(Volts: 100mV/Div. Input)
Horizontal Scale: (Time: 1μs/Div.)



LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: 5V/Div.)
Horizontal Scale: (Time: 5μs/Div.)

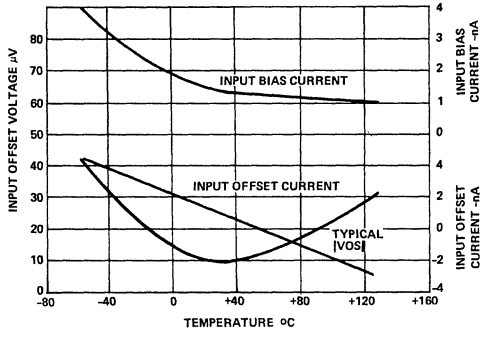


SETTLING TIME CIRCUIT

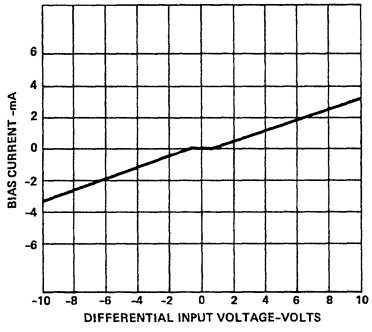


- A_V = -1.
- Feedback and summing resistors should be 0.1%.
- Clipping diodes are optional. HP5082-2810 recommended.

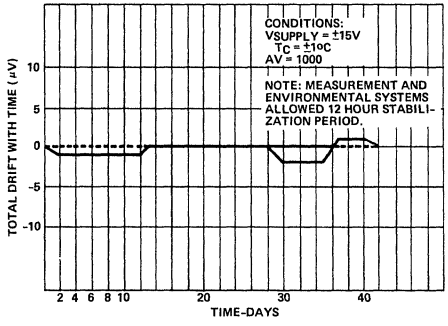
INPUT OFFSET VOLTAGE, INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE



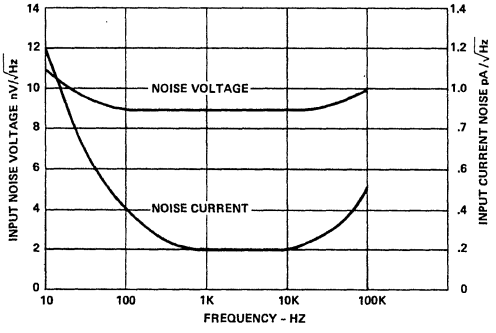
INPUT BIAS CURRENT VS. DIFFERENTIAL INPUT VOLTAGE



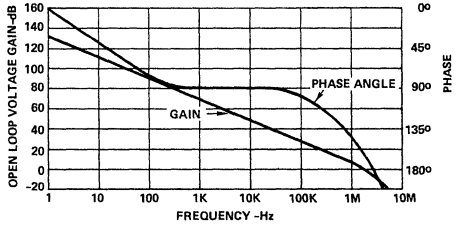
HA-5130 OFFSET VOLTAGE STABILITY VS. TIME



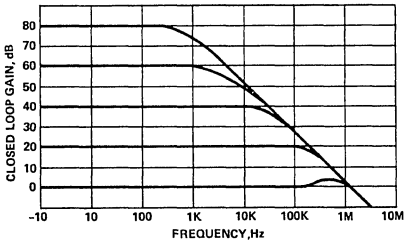
INPUT - NOISE VS. FREQUENCY



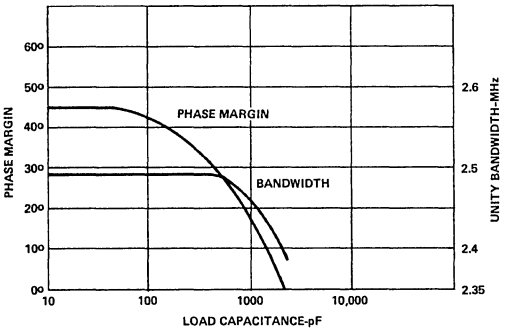
OPEN LOOP FREQUENCY RESPONSE



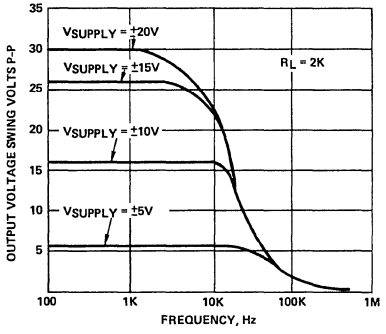
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



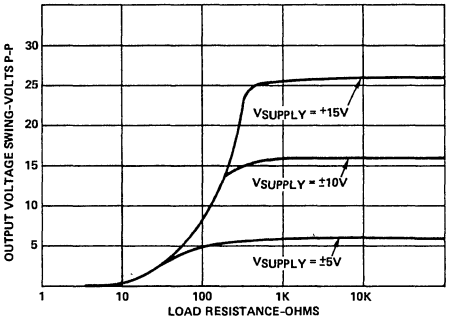
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN VS. LOAD CAPACITANCE



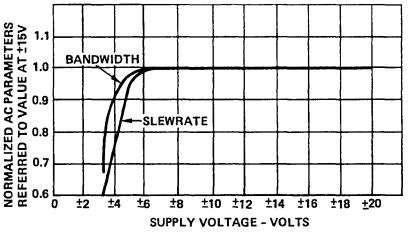
OUTPUT VOLTAGE SWING VS. FREQUENCY AND SUPPLY VOLTAGE



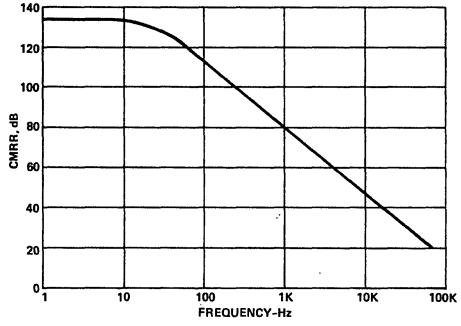
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE AND SUPPLY VOLTAGE



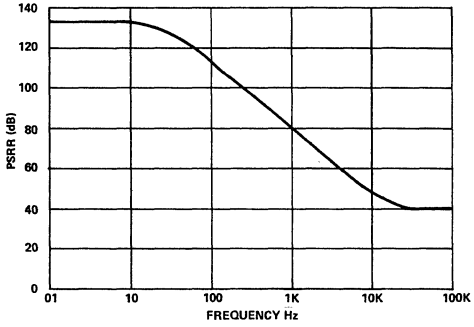
NORMALIZED AC PARAMETERS VS. SUPPLY VOLTAGE



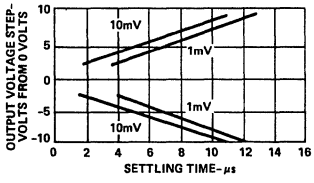
CMRR VS. FREQUENCY



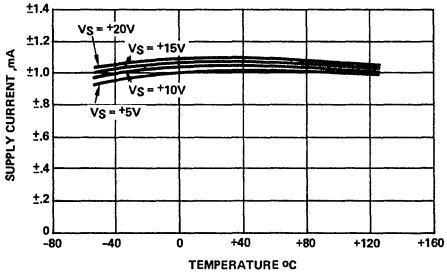
PSRR VS. FREQUENCY



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



POWER SUPPLY CURRENT VS. TEMPERATURE AND SUPPLY VOLTAGE



APPLYING THE HA-5130/5135 OPERATIONAL AMPLIFIERS

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01μ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. CONSIDERATIONS FOR PROTOTYPING: The following list of recommendations are suggested for prototyping.
   - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces, and implementation of moisture barriers when required is suggested.
   - Error voltages generated by theromocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuitry from heat generating components is recommended.
   - Shielded cable input leads, guard rings, and shield drivers are recommended for the most critical applications.

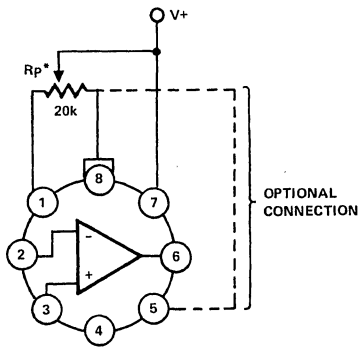
3. When driving large capacitive loads (> 500pF), as small value resistor (≈50Ω) should be connected in series with the output and inside the feedback loop.

4. OFFSET VOLTAGE ADJUSTMENT: A 20 KΩ balance potentiometer is recommended if offset nulling is required. However, other potentiometer values such as 10KΩ, 50KΩ, and 100KΩ may be used. The minimum adjustment range for given values is ±2mV.

5. SATURATION RECOVERY: Input and output saturation recovery time is negligible in most applications. However, care should be exercised to avoid exceeding the absolute maximum ratings of the device.

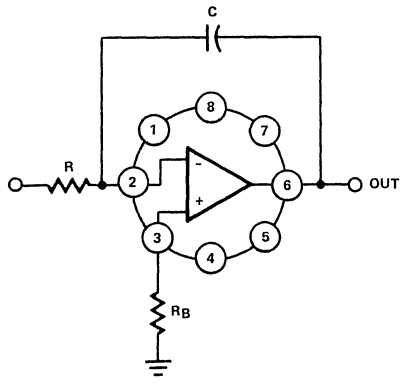
6. DIFFERENTIAL INPUT VOLTAGES: Inputs are shunted with back-to-back diodes for overvoltage protection. In applications where differential input voltages in excess of IV are applied between the inputs, the use of limiting resistors at the inputs is recommended.

OFFSET NULLING CONNECTIONS



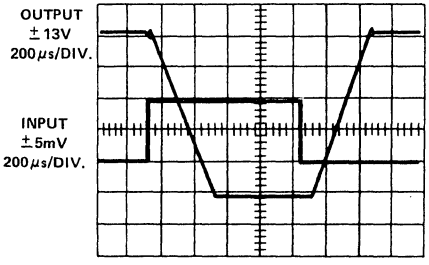
*Although Rp is shown equal to 20k, other values such as 50k, 100k, and 1M may be used. Range of adjustment is approximately ±2.5mV. V_{OS} TC of the amplifier is optimized at minimal V_{OS}.

PRECISION INTEGRATOR

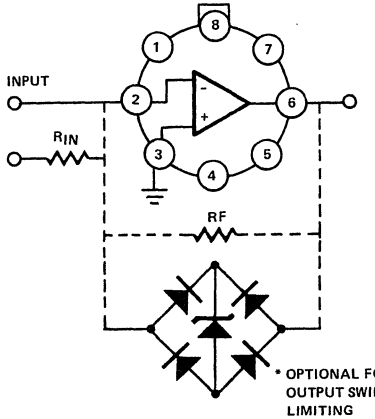


The excellent input and gain characteristics of HA-5130 are well suited for precision integrator applications. Accurate integration over seven decades of frequency using HA-5130, virtually nullifies the need for more expensive chopper-type amplifiers.

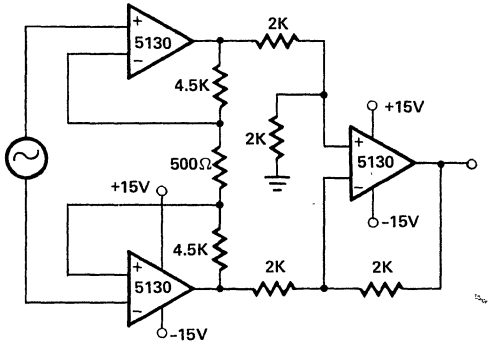
ZERO CROSSING DETECTOR



Low V_{OS} coupled with high open loop Gain, high CMRR, and high PSRR make HA-5130 ideally suited for precision detector applications.



PRECISION INSTRUMENTATION AMPLIFIER (A_V = 100)



HA-5160/5162

Wideband, JFET Input, High Slew Rate, Uncompensated, Operational Amplifier

2

FEATURES

- WIDE GAIN BANDWIDTH 100MHz
- HIGH SLEW RATE 120V/μs
- SETTLING TIME (0.2%) 280ns
- POWER BANDWIDTH 1000kHz
- OFFSET VOLTAGE 1.0mV
- BIAS CURRENT 20pA

APPLICATIONS

- VIDEO AND RF AMPLIFIERS
- DATA ACQUISITION
- PULSE AMPLIFIERS
- PRECISION SIGNAL GENERATION

DESCRIPTION

The HA-5160/5162 is a wideband, uncompensated, operational amplifier manufactured with FET/Bipolar technologies and dielectric isolation. This monolithic amplifier features superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. This device has excellent phase margin at a closed loop gain of 10 without external compensation.

The HA-5160/5162 offers a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics, the HARRIS devices have nearly constant slew rate, bandwidth, and settling characteristics over the operating temperature range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. Note also that HARRIS specified all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

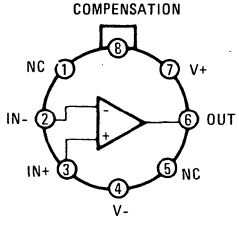
Complementing the HA-5160/5162's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and extremely high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications.* The HA-5160 provides excellent performance for applications which require both precision and high speed perfornance. The HA-5162 meets or exceeds the performance specifications of National's hybrid op amp, the LH0062.

* -2 denotes a range of -55°C to +125°C and -5 denotes a 0°C to +75°C range.

PINOUT

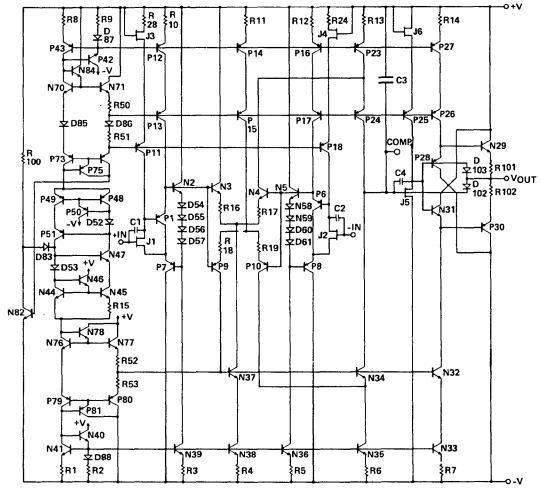
Section 11 for Packaging

TOP VIEW



Case connected to V-

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	40V
Differential Input Voltage	±40V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	675mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS V+ = +15V, V- = -15V

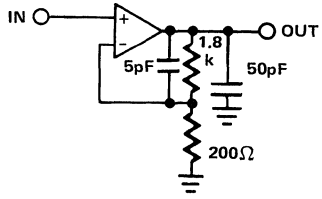
		HA-5160-2 -55°C to +125°C			HA-5160-5 0°C to +75°C			HA-5162-5 0°C to 75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	TYP	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		1.0	3.0		1.0	3.0		3	15	mV
	Full		3.0	5.0		3.0	5.0		5	20	mV
Offset Voltage Average Drift	Full		10			20			20	35	μV/°C
Bias Current	+25°C		20	50		20	50		20	65	pA
	Full		5	10			10			10	nA
Offset Current	+25°C		2	10		2	10		2	10	pA
	Full		2	5		2	5		2	5	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±11		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75K	150K		75K	150K		25K	100K		V/V
	Full	60K	100K		60K	100K		25K	75K		V/V
Common Mode Rejection Ratio (Note 4)	Full	74	80		74	80		70	80		dB
Gain Bandwidth Product (A_V = 10)	Full		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 5)	+25°C	±10	±11		±10	±11		±10	±11		V
	Full	±10	±11		±10	±11		±10	±11		V
Output Current (Note 6)	+25°C	±15	±20		±15	±20		±15	±20		mA
Full Power Bandwidth (Note 7)	+25°C		1000			1000			1000		kHz
Output Resistance (Note 8)	+25°C		50			50			50		Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time (A_V = 10)	+25°C		20			20			20		ns
Slew Rate (A_V = 10)	+25°C	100	120		100	120		50	70		V/μs
Settling Time (Note 10)	+25°C		280			280			400		ns
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full		8.0	10		8.0	10		8.0	12	mA
Power Supply Rejection Ratio (Note 11)	+25°C	74	86		74	86		70	86		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. $V_{OUT} = \pm 10V$. $R_L = 2k$
4. $V_{CM} = \pm 10V$ DC.
5. $R_L = 2k$
6. $V_{OUT} = 0V$
7. $R_L = 2k$; Full power bandwidth guaranteed, based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. Output resistance measured under open loop conditions.
9. Refer to Test Circuits section of the data sheet.
10. Settling Time is measured to 0.2% of final value for a 10 volt output step and $A_V = 10$.
11. $V_{SUPP} = \pm 10$ V.D.C. to ± 20V DC.

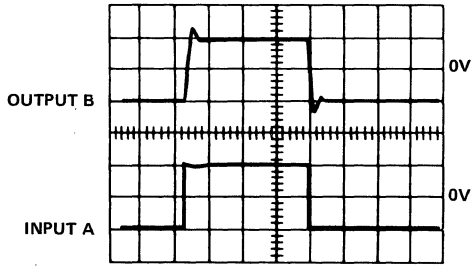
TEST CIRCUITS

LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



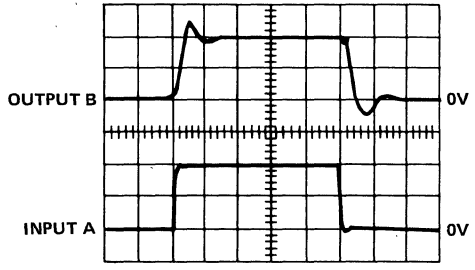
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A = 0.5V/Div., B = 5V/Div.)
Horizontal Scale: (Time: 500ns/Div.)

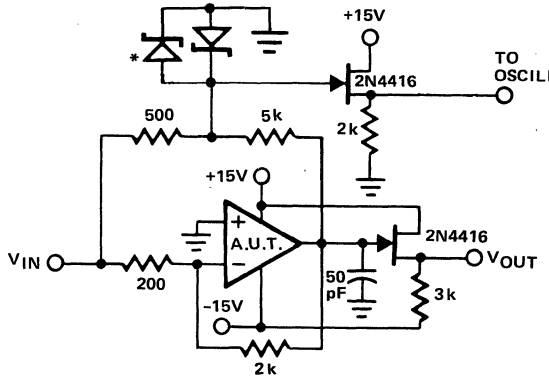


SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: A = 10mV/Div., B = 100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)

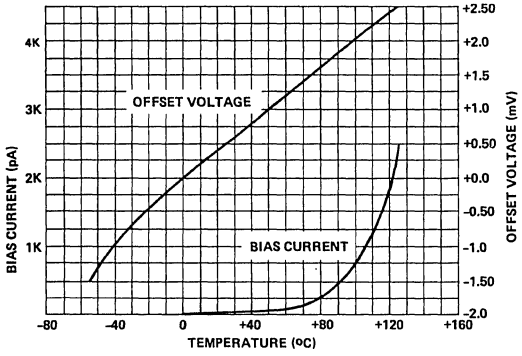


SETTLING TIME CIRCUIT

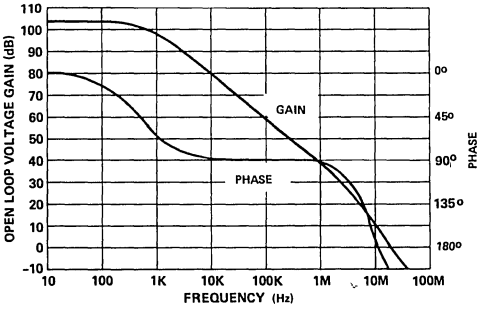


- $A_V = -10$
- Feedback and summing resistors should be 0.1%.
- * Clipping Diodes are optional. HP5082-2810 recommended.

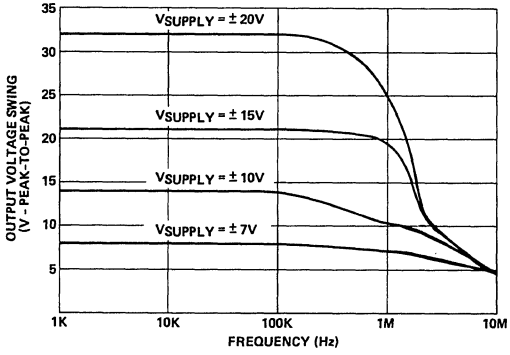
INPUT OFFSET VOLTAGE AND BIAS CURRENT VS. TEMPERATURE



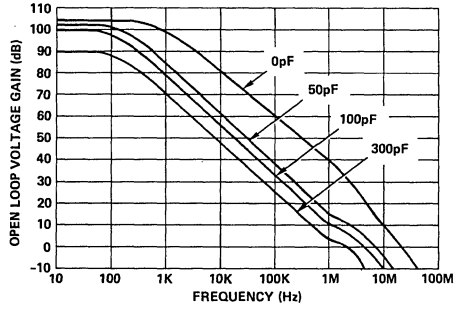
OPEN LOOP FREQUENCY RESPONSE



OUTPUT VOLTAGE SWING VS. FREQUENCY

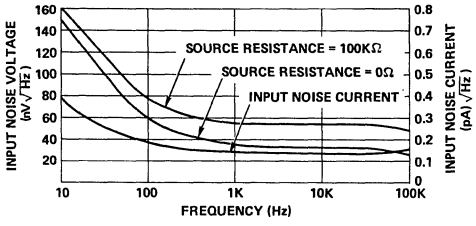


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS BANDWIDTH CONTROL CAPACITANCES

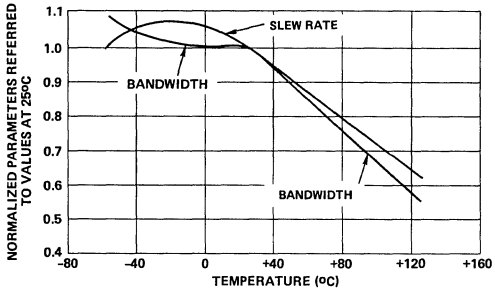


2

INPUT NOISE VOLTAGE AND NOISE CURRENT VS. FREQUENCY

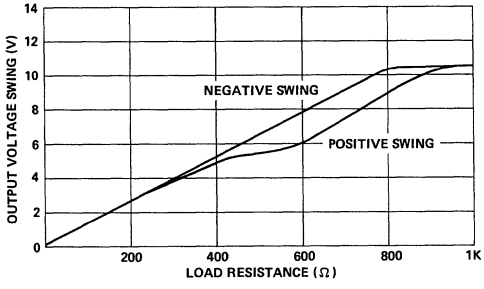


NORMALIZED AC PARAMETERS VS. TEMPERATURE

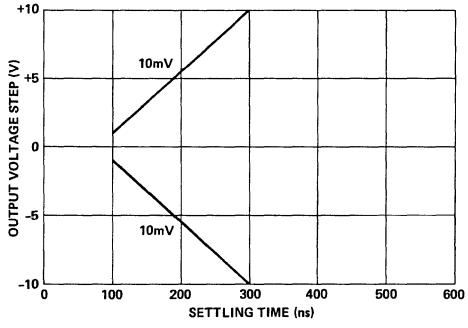


2

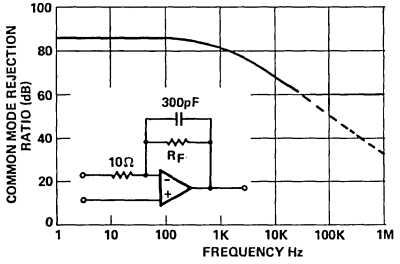
OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



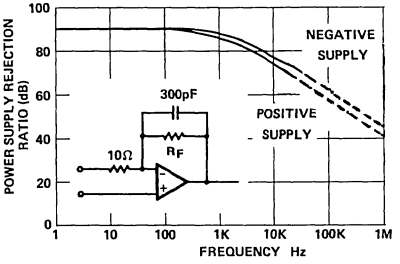
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



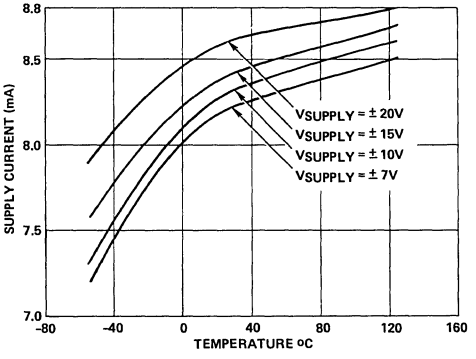
COMMON MODE REJECTION RATIO VS. FREQUENCY



POWER SUPPLY REJECTION RATIO VS. FREQUENCY



POWER SUPPLY CURRENT VS. TEMPERATURE

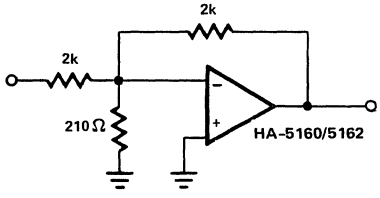


1. POWER SUPPLY DECOUPLING: Although not absolutely necessasry, it is recommended that all power supply lines be decoupled with 0.01 μF ceramic capacitors to ground decoupling capacitors should be located as near to the amplifier terminals as possible.
2. STABILITY: The phase margin of the HA-5160/5162 will be improved by connecting a small capacitor (>10pF) between the output and the inverting input of the device. This small capacitor compensates for the input capacitance of the FET.
3. CAPACITIVE LOADS: When driving large capacitive loads (>100pF), it is suggested that a small resistor ($\approx$100Ω) be connected in series with the output of the device and inside the feedback loop.

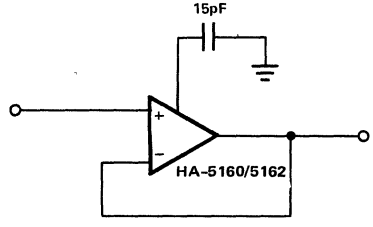
APPLICATIONS

SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY *

INVERTING

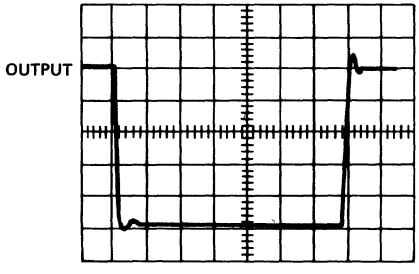


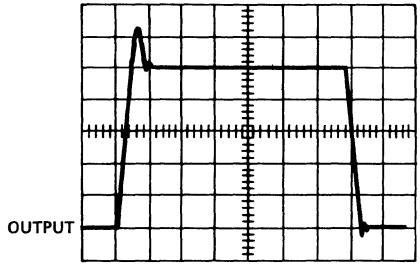
NONINVERTING



*VALUES WERE DETERMINED EXPERIMENTALLY FOR OPTIMUM SPEED AND SETTLING TIME

VERTICAL SCALE: (VOLTS: 2V/DIV.)
HORIZONTAL SCALE: (TIME: 500ns/DIV.)





HARRIS

HA-5170

Precision JFET Input Operational Amplifier

Preliminary

FEATURES

- LOW OFFSET VOLTAGE — 100μV
- LOW OFFSET VOLTAGE DRIFT — 3μV/°C
- LOW NOISE — 12nV/√Hz
- OPEN LOOP GAIN — 100K
- BANDWIDTH (UNITY GAIN) — 5MHz

APPLICATIONS

- HIGH GAIN INSTRUMENTATION
- PRECISION DATA ACQUISITION
- PRECISION INTEGRATORS
- PRECISION THRESHOLD DETECTORS

DESCRIPTION

The Harris HA-5170 is a precision, JFET input, operational amplifier which features low noise, low offset voltage and low offset voltage drift. Constructed using FET/Bipolar technology, the Harris Dielectric Isolation (DI) process, and laser trimming this amplifier offers low input bias and offset currents. This operational amplifier design also completely eliminates the troublesome errors due to warm-up drift.

Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An 8V/μs slew rate and 5MHz bandwidth allow the designer to extend precision instrumentation applications in both speed and bandwidth. These characteristics make the HA-5170 well suited for precision integrator amplifier designs.

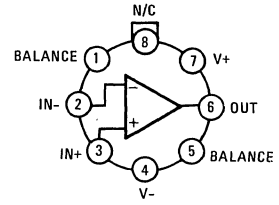
The superior input characteristics also make the HA-5170 ideally suited for transducer signal amplifiers, precision voltage followers and precision data acquisition systems.

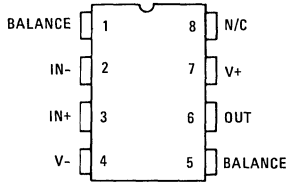
Packaged in an 8-pin (TO-99) can or an 8 lead Minidip, the HA-5170 is pin compatible with most existing op amp configurations.

PINOUT

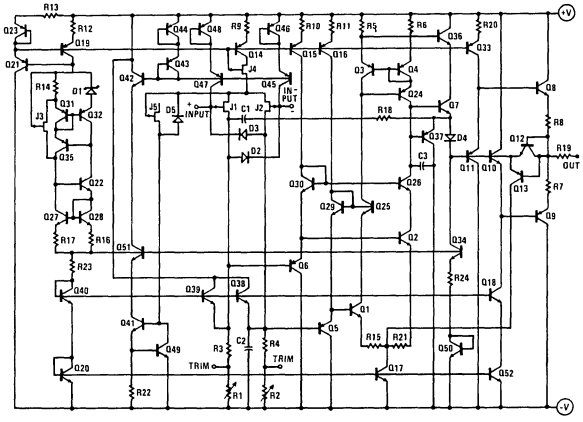
Section 11 for Packaging

TOP VIEW





SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless otherwise stated		Power Dissipation (Note 2)	675mW
Voltage Between V+ and V-Terminals	44.0V	Operating Temperature Range	
Differential Input Voltage	±30.0V	HA-5170-2	$-55°C \leq T_A \leq +125°C$
		HA-5170-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL CHARACTERISTICS V+ = 15V, V- = -15V

PARAMETER	TEMP.	HA-5170-2 MIN	HA-5170-2 TYP	HA-5170-2 MAX	HA-5170-5 MIN	HA-5170-5 TYP	HA-5170-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.1	0.5		0.1	0.5	mV
	Full			1			0.75	mV
Average Offset Voltage Drift	Full		3	5		3	5	µV/°C
Bias Current	+25°C		20	30		20	60	pA
	Full		3	10		0.04	0.1	nA
Bias Current Average Drift	Full						3	pA/°C
Offset Current	+25°C			30			60	pA
	Full			5			0.1	nA
Offset Current Average Drift	Full						1	pA/°C
Common Mode Range	Full	±10			±10			V
Differential Input Resistance	+25°C		6×10^{10}			6×10^{10}		MΩ
Input Noise Voltage (f = 1kHz)	+25°C		12			12		nV/√Hz
Input Noise Current (f = 1kHz)	+25°C		0.01			0.01		pA/√Hz
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	100K			80K			V/V
	Full	80K			50K			V/V
Common Mode Rejection Ratio (Note 4)	Full	100			90			dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C		5			5		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 5)	+25°C	±10			±10			V
Full Power Bandwidth (Note 6)	+25°C		110			110		kHz
Output Current (Note 7)	+25°C	±10			±10			mA
Output Resistance (Note 8)	+25°C		45			45		Ω
TRANSIENT RESPONSE								
Rise Time	+25°C		45	100		45	100	ns
Slew Rate	+25°C	5	8		5	8		V/µs
Settling Time (Note 9)	+25°C		1			1		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		1.9	2.1		1.9	2.1	mA
Power Supply Rejection Ratio (Note 10)	Full	100			90			dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8 mW/°C for operation at ambient temperatures above +75°C.
3. V_{OUT} = ±10V; R_L = 2k.
4. V_{CM} = ±10V D. C.
5. R_L = 2kΩ.
6. R_L = 2k; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
7. V_{OUT} = 10V.
8. Output resistance measured under open loop conditions (f = 100Hz).
9. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
10. V_{SUPP} = ±5V D. C. to ±20V D. C.

HARRIS

HA-5190/5195

Wideband, Fast Settling Operational Amplifier

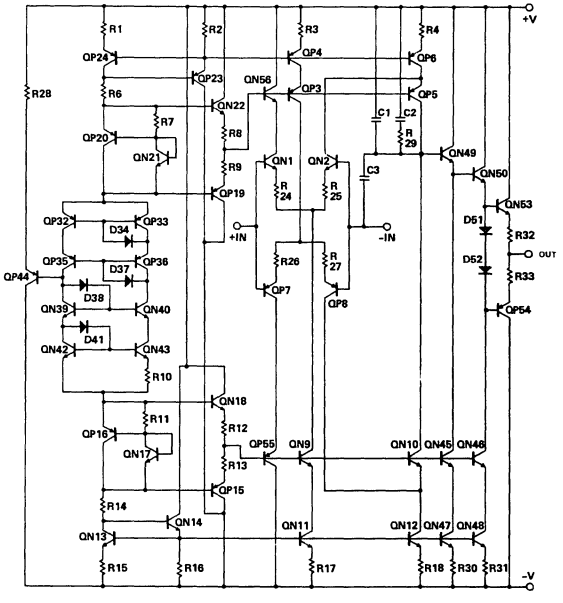
FEATURES

- FAST SETTLING TIME — 70ns
- VERY HIGH SLEW RATE — 200V/μs
- WIDE GAIN-BANDWIDTH — 150MHz
- POWER BANDWIDTH — 6.5MHz
- LOW OFFSET VOLTAGE — 5mV
- INPUT VOLTAGE NOISE — 15nV/$\sqrt{Hz}$
- MONOLITHIC BIPOLAR CONSTRUCTION

APPLICATIONS

- FAST, PRECISE D/A CONVERTERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- PULSE AND VIDEO AMPLIFIERS
- WIDEBAND AMPLIFIERS
- REPLACE COSTLY HYBRIDS

SCHEMATIC



GENERAL DESCRIPTION

HA-5190/5195 are monolithic operational amplifiers featuring an ultimate combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with dielectric isolation, these devices are capable of delivering an unparalleled 200V/μs slew rate with a settling time of 70ns (0.1%, 5V output step). These truly differential amplifiers are designed to operate at gains ≥ 5 without the need for external compensation. Other outstanding HA-5190/5195 features are 150MHz gain-bandwidth-product and 6.5MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 5mV offset voltage and 15nV input voltage noise (at 1kHz).

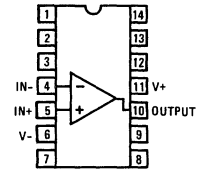
With 200V/μs slew rate and 70ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. 150MHz gain-bandwidth-product, 6.5MHz power bandwidth, and 5mV offset voltage make HA-5190/5195 ideally suited for a variety of pulse and wideband video amplifier applications.

At temperatures above +75°C, a heat sink is required for HA-5190. (See note 2). HA-5190 is specified over the -55°C to +125°C range while HA-5195 is specified from 0°C to +75°C.

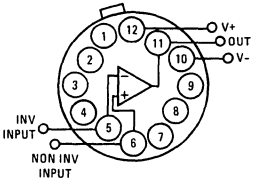
PINOUTS

Section 11 for Packaging

TOP VIEW



TOP VIEW



CASE TIED TO V-

LH0032 PINOUT

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation (Note 2)	870mW (Cerdip); 1W (TO-8) Free Air
Operating Temperature Range: (HA-5190)	$-55^{o}C \leq T_A \leq +125^{o}C$
(HA-5195)	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS $V_{SUPPLY} = \pm 15$ Volts; R_L = 1K ohms, unless otherwise specified.

		HA-5190 -55°C to +125°C			HA-5195 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		3.0	5.0		3.0	6	mV
	FULL			10.0			10.0	mV
Average Offset Voltage Drift	FULL		20			20		µV/°C
Bias Current	+25°C		5	15		5	15	µA
	FULL			20			20	µA
Offset Current	+25°C		1	4		1	4	µA
	FULL			6			6	µA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±5			±5			V
Input Noise Voltage (f = 1kHz, $R_g = 0\Omega$)	+25°C		15			15		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	15K	30K		10K	30K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 4)	FULL	74			74			dB
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C		150			150		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	FULL	±5	±8		±5	±8		V
Output Current (Note 3)	+25°C	25	30		25	30		mA
Output Resistance	+25°C		30			30		Ohms
Full Power Bandwidth (Note 3 & 7)	+25°C	5	6.5		5	6.5		MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		13	18		13	18	ns
Overshoot	+25°C		8			8		%
Slew Rate	+25°C	160	200		160	200		V/µs
Settling Time:								
5V Step to 0.1%	+25°C		70			70		ns
5V Step to 0.01%	+25°C		100			100		ns
2.5V Step to 0.1%	+25°C		50			50		ns
2.5V Step to 0.01%	+25°C		80			80		ns
POWER REQUIREMENTS								
Supply Current	FULL		19	28		19	28	mA
Power Supply Rejection Ratio (Note 9)	FULL	70	90		70	90		dB

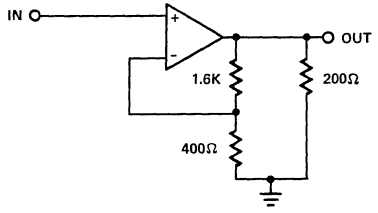
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 8.7mW/°C for operation at ambient temperatures above +75°c. Heat sinking required at temperatures above +75°c. T_{JA} = 115°C/W; T_{JC} = 35°C/W. Thermalloy model 6007 heat sink recommended.
3. $R_L = 200\Omega, C_L < 10pF$, $V0 = \pm 5V$
4. $V_{CM} = \pm 5V$.
5. $V_0 = 90mV$.
6. $A_V = 10$.
7. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$.
8. Refer to Test Circuits section of data sheet.
9. $V_{SUPPLY} = \pm 5$ VDC to ± 15 VDC

TEST CIRCUITS

LARGE AND SMALL SIGNAL RESPONSE

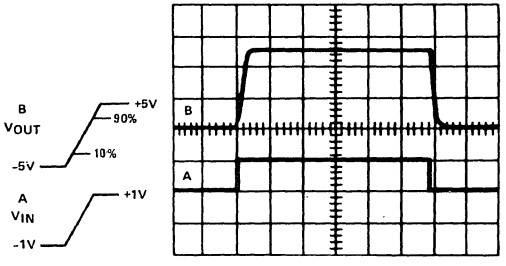
TEST CIRCUIT*



AV = 5
*$C_L \leq 10pF$

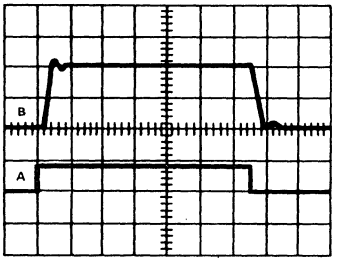
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A = 0.5V/Div., B = 4.0V/Div.)
Horizontal Scale: (Time: 100ns/Div.)

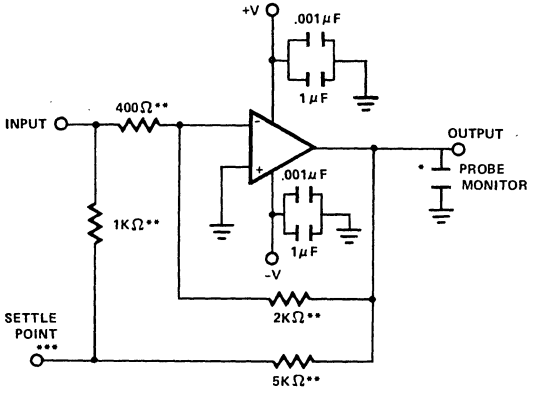


SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: A=50mV/Div., B=100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)



SETTLING TIME TEST CIRCUIT



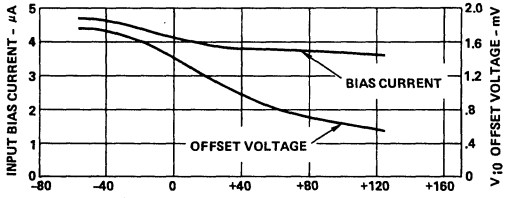
* Load Capacitance should be less than 10pF.

** It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched.

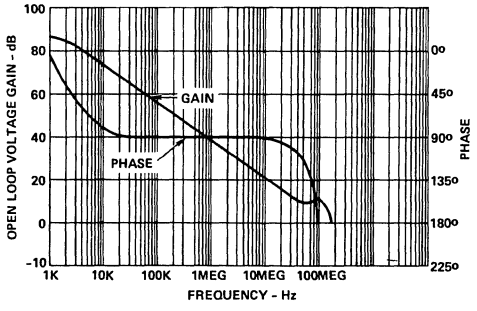
*** SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

V+ = +15V, V- = -15V, T_A = +25°C unless otherwise stated.

INPUT OFFSET VOLTAGE AND BIAS CURRENT VS. TEMPERATURE

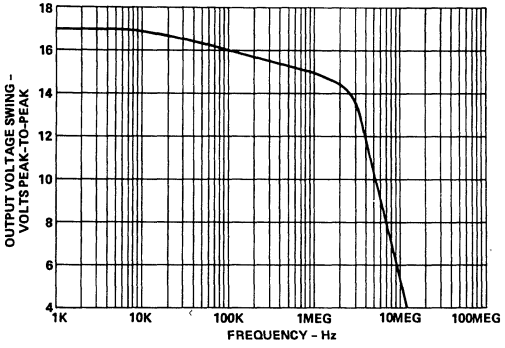


OPEN LOOP FREQUENCY RESPONSE

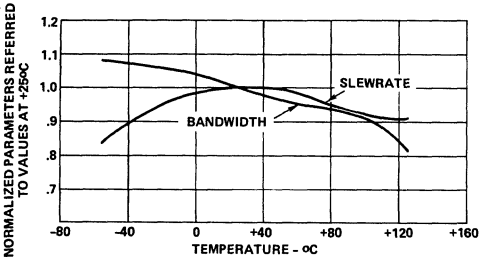


2

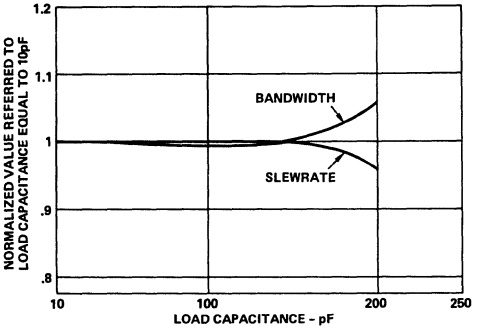
OUTPUT VOLTAGE SWING VS. FREQUENCY



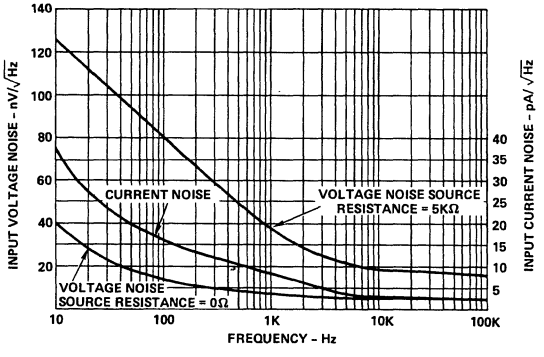
NORMALIZED AC PARAMETERS VS. TEMPERATURE



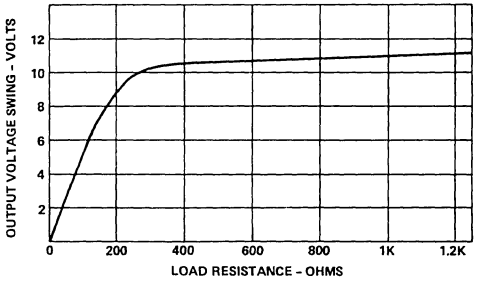
NORMALIZED AC PARAMETERS VS. LOAD CAPACITANCE



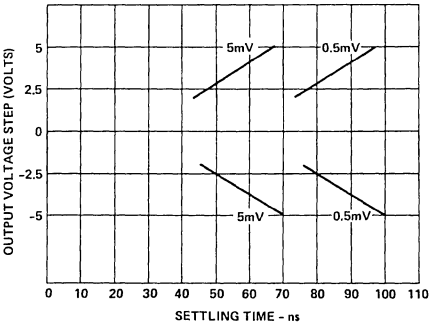
INPUT NOISE VOLTAGE AND NOISE CURRENT VS. FREQUENCY



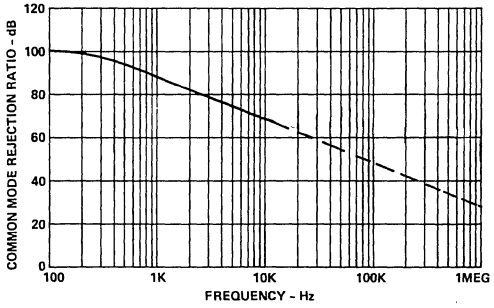
OUTPUT VOLTAGE SWING
VS. LOAD RESISTANCE



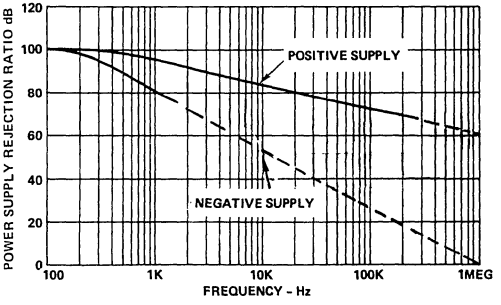
SETTLING TIME FOR VARIOUS
OUTPUT STEP VOLTAGES



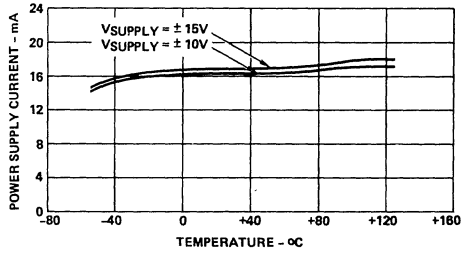
COMMON MODE REJECTION RATIO
VS. FREQUENCY



POWER SUPPLY REJECTION
RATIO VS. FREQUENCY



POWER SUPPLY CURRENT
VS. TEMPERATURE



2

APPLYING THE HA-5190/5195

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with .01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.

2. STABILITY CONSIDERATIONS: HA-5190/5195 is stable at gains ≥ 5. Gains < 5 are covered elsewhere in this data sheet. Feedback resistors should be of carbon composition located as near to the input terminals as possible.

3. WIRING CONSIDERATIONS: Video pulse circuits should be built on a ground plane. Minimum point to point connections directly to the amplifier terminals should be used. When ground planes cannot be used, good single point grounding techniques should be applied.

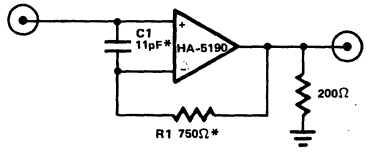
4. OUTPUT SHORT CIRCUIT: HA-5190/5195 does not have output short circuit protection. Short circuits to ground can be tolerated for approximately 10 seconds. Short circuits to either supply will result in immediate destruction of the device. In applications where short circuiting is possible, current limiting resistors in the supply lines are recommended.

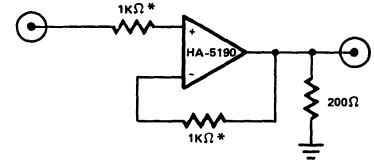
5. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads ($\geq$100pF) a small resistor ($\approx$100Ω) should be connected in series with the output and inside the feedback loop.

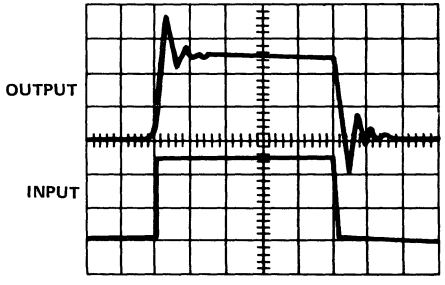
APPLICATIONS

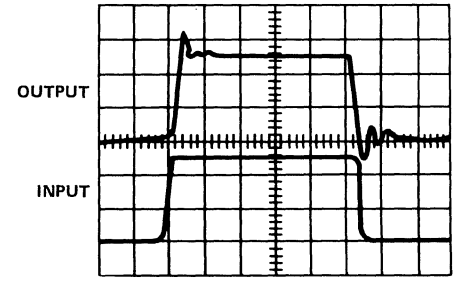
SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY

NONINVERTING







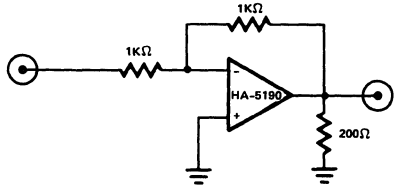


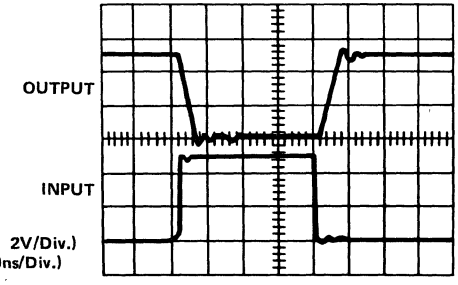
Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 100ns/Div.)

* Values were determined experimentally for optimum speed and settling time.

R1 and C1 should be optimized for each particular application to ensure best overall frequency response.

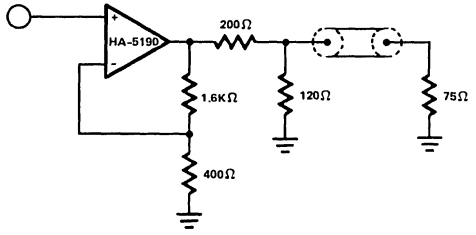
INVERTING



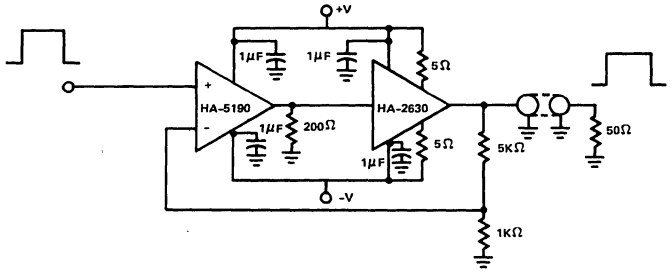


Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (50ns/Div.)

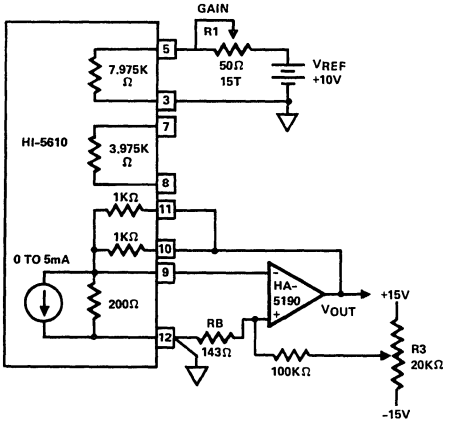
VIDEO PULSE AMPLIFIER/75Ω COAXIAL DRIVER

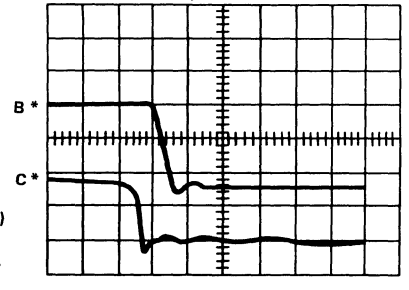


VIDEO PULSE AMPLIFIER COAXIAL LINE DRIVER



FAST DAC OUTPUT BUFFER





Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 50ns/Div.)

B = V_{OUT} C = DIGITAL INPUT

* Time delay between B and C represents total time delay for 0V to +5V full scale coded change.

HARRIS

HA-8023

Triple Low Power Programmable Operational Amplifier

Preliminary

2

FEATURES

- LOW INPUT OFFSET VOLTAGE (MAX) 3mV
- LOW INPUT BIAS CURRENT (MAX) 30nA
- WIDE POWER SUPPLY RANGE ±2V TO ±18V
- INTERNALLY COMPENSATED

APPLICATIONS

- BATTERY-POWERED EQUIPMENT
- CURRENT CONTROLLED OSCILLATORS
- ACTIVE FILTERS
- VARIABLE ACTIVE FILTERS

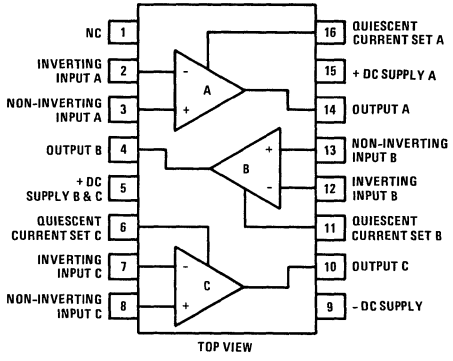
DESCRIPTION

The HA-8023 triple programmable amplifiers are internally compensated, monolithic devices which offer a wide range of performance characteristics that can be controlled by adjusting the circuits' "SET" current. Each amplifier on the chip can be adjusted independently, and by adjusting an external resistor or current source, the electrical characteristics can be programmed to the desired levels. This versatile adjustment capability enables the HA-8023 to provide optimum design solutions by delivering the required level of performance with minimum power dissipation.

The HA-8023-2 performance specifications are guaranteed over the -55°C to +125°C temperature range and the HA-8023-5 over the 0°C to +75°C temperature range.

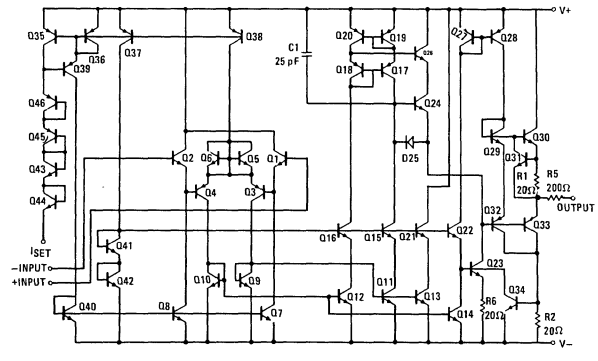
PINOUT

Section 11 for Packaging



TOP VIEW

SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	±22V
Differential Input Voltage	±15V
Input Voltage (Note 2)	±15V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS $V_S = \pm 6V$, $I_Q = 30\mu A$, unless otherwise specified I_Q = Quiescent Supply Current

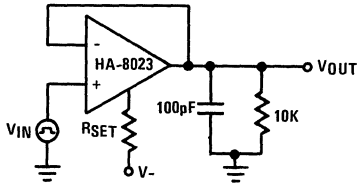
		HA-8023-2 -55°C to +125°C			HA-8023-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage (Note 3)	+25°C		2	3.0		2	6	mV
	Full		2	4		2	7.5	mV
Offset Voltage Average Drift	Full		5			5		µV/°C
Bias Current	+25°C		3	30		3	30	nA
	Full		5	50		5	50	nA
Offset Current	+25°C		3	10		3	10	nA
	Full		1	15		1	15	nA
Input Resistance	+25°C	3	10		3	10		MΩ
Input Voltage Range (Note 4)	+25°C	±12	±13		±12	±13		V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 5)	Full	5K	10K		5K	10K		V/V
Channel Separation (Note 6)	+25°C		105			105		dB
Common Mode Rejection Ratio (Note 7)	+25°C	70	100		70	100		dB
Unity Gain Bandwidth (Note 8)	+25°C		270			270		kHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 9)	+25°C	±11	±13		±11	±13		V
	Full	±10	±13		±10	±13		V
Output Voltage Swing (Note 10)	+25°C	±12	±14		±12	±14		V
Output Voltage Swing (Note 11)	+25°C	±4	±5		±4	±5		V
	Full	±4	±5		±4	±5		V
Output Short Circuit Current	+25°C		±4			±4		mA
Full Power Bandwidth (Note 12)	+25°C		3.5			3.5		kHz
Output Resistance	+25°C		2			2		KΩ
TRANSIENT RESPONSE (Note 13)								
Rise Time	+25°C		700			700		ns
Slew Rate	+25°C		.1			.1		V/µs
Overshoot	+25°C		12			12		%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		30	40		30	50	µA
Power Consumption (Note 14)	+25°C		360	480		360	600	µW
Power Supply Rejection Ratio (Note 15)	+25°C	76	100		76	100		dB

NOTES

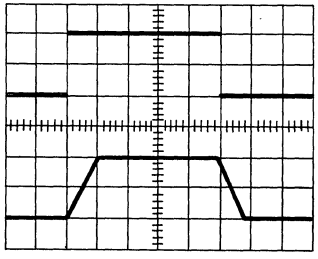
1. Absolute Maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages Less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. $R_S \leq 100K\Omega$
4. $V_S = \pm 15V$
5. $R_L = 10K\Omega$
6. $R_S = 1K\Omega$, f = 10kHz
7. $R_S \leq 10K\Omega$, $V_{CM} = \pm 5V$ DC
8. $R_L = 20K\Omega$, $V_{IN} = 20mV$
9. $R_L \geq 10K\Omega$, $V_S = \pm 15V$
10. $R_L \geq 20K\Omega$, $V_S = \pm 15V$
11. $R_L \geq 10K\Omega$, $V_S = \pm 6V$
12. $R_L = 20K\Omega$
13. $R_L = 10K\Omega$, $C_L = 100pF$
14. $V_{OUT} = 0V$, $R_{SET} = 2.7m\Omega$,
15. $V_{SUPP} = \pm 1V$ DC to $\pm 11V$ DC

TEST CIRCUITS

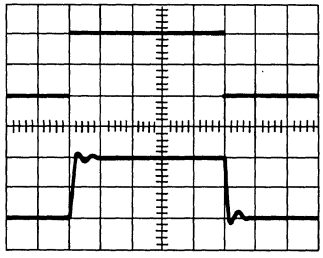
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: A = 2V/ Div., B = 2V/Div.)
Horizontal Scale (Time: 50 μs/Div.)



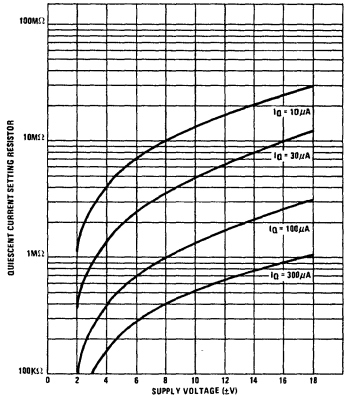
SMALL SIGNAL RESPONSE
Vertical Scale; (Volts: A = 20mV/Div., B = 20mV/Div.)
Horizontal Scale : (Time: 5 μs/Div.)



QUIESCENT CURRENT ADJUSTMENT
QUIESCENT CURRENT TO V-

IQ / VS	10μA	30μA	100μA	300μA
± 2.0V	1MΩ	275KΩ	100KΩ	30KΩ
± 3.0V	2.7MΩ	1MΩ	270KΩ	100KΩ
± 6.0V	7.5MΩ	2.7MΩ	750KΩ	270KΩ
± 9.0V	18MΩ	6.3MΩ	1.8MΩ	620KΩ
± 12.0V	26MΩ	9MΩ	2.7MΩ	900KΩ
± 15.0V	32MΩ	12MΩ	3.7MΩ	1.2MΩ

QUIESCENT CURRENT SETTING RESISTOR TO V-



LF155 Series Monolithic JFET Input Operational Amplifiers

LF155, LF155A, LF355, LF355A, LF355B low supply current

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

Common Features

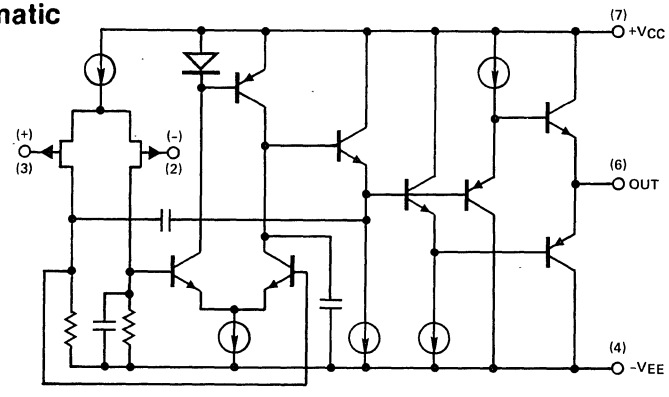
(LF155A)

Low input bias current	30 pA
Low Input Offset Current	3 pA
High input impedance	$10^{12}\Omega$
Low input offset voltage	1 mV
Low input offset voltage temperature drift	$3\mu V/°C$
Low input noise current	0.01 $pA/\sqrt{Hz}$
High common-mode rejection ratio	100 dB
Large dc voltage gain	106 dB

Uncommon Features

	LF155A	UNITS
Extremely fast settling time to 0.01%	4	μs
Fast slew rate	5	$V/\mu s$
Wide gain bandwidth	2.5	MHz
Low input noise voltage	20	$nV/\sqrt{Hz}$

Simplified Schematic



Absolute Maximum Ratings

	LF155A	LF155	LF355B	LF355A LF355
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}) (Note 1)				
T_{jMAX}				
(H and J Package)	150°C	150°C	115°C	115°C
(N Package)			100°C	100°C
(H Package) P_d	670 mW	670 mW	570 mW	570 mW
θ_{jA}	150°C/W	150°C/W	150°C/W	150°C/W
(J Package) P_d	670 mW	670 mW	570 mW	570 mW
θ_{jA}	140°C/W	140°C/W	140°C/W	140°C/W
(N Package) P_d			500 mW	500 mW
θ_{jA}			155°C/W	155°C/W
Differential Input Voltage	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155A			LF355A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		1	2		1	2	mV
		Over Temperature			2.5			2.3	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5		3	5	µV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		µV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5)		3	10		3	10	pA
		$T_j \leq T_{HIGH}$			10			1	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	50		30	50	pA
		$T_J \leq T_{HIGH}$			25			5	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = ±15V$, $T_A = 25°C$ $V_O = ±10V$, $R_L = 2k$	50	200		50	200		V/mV
		Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	$V_S = ±15V$, $R_L = 10k$	±12	±13		±12	±13		V
		$V_S = ±15V$, $R_L = 2k$	±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = ±15V$	±11	+15.1 −12		±11	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = 25°C$, $V_S = ±15V$

SYMBOL	PARAMETER	CONDITIONS	LF155A/355A			UNITS
			MIN	TYP	MAX	
SR	Slew Rate	$A_V = 1$	3	5		V/µs
						V/µs
GBW	Gain Bandwidth Product			2.5		MHz
t_s	Settling Time to 0.01%	(Note 7)		4		µs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz		25		$nV/\sqrt{Hz}$
		f = 1000 Hz		25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 100 Hz		0.01		$pA/\sqrt{Hz}$
		f = 1000 Hz		0.01		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3		pF

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155			LF355B			LF355			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu V/°C$ per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5)		3	20		3	20		3	50	pA
		$T_j \leq T_{HIGH}$			20			1			2	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$ $V_O = \pm10V$, $R_L = 2k$	50	200		50	200		25	200		V/mV
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		±12	±13		±12	±13		V
		$V_S = \pm15V$, $R_L = 2k$	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1		±11	+15.1		±10	+15.1		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

PARAMETER	LF155A/155, LF355A/355B		LF355		UNITS
	TYP	MAX	TYP	MAX	
Supply Current	2	4	2	4	mA

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF155 355/355B TYP	UNITS
SR	Slew Rate	$A_V = 1$	5	V/μs
				V/μs
GBW	Gain Bandwidth Product		2.5	MHz
t_s	Settling Time to 0.01%	(Note 7)	4	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz	25	$nV/\sqrt{Hz}$
		f = 1000 Hz	20	$nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f = 100 Hz	0.01	$pA/\sqrt{Hz}$
		f = 1000 Hz	0.01	$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance		3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

	LF155A LF155	LF355A	LF355B	LF355
Supply Voltage, V_S	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 18V$	$\pm 15V \le V_S \pm 20V$	$V_S = \pm 15V$
T_A	$-55°C \le T_A \le +125°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$	$0°C \le T_A \le +70°C$
T_{HIGH}	+125°C	+70°C	+70°C	+70°C

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA}$ Pd where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

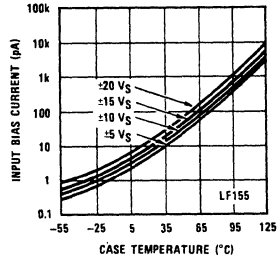
Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter.

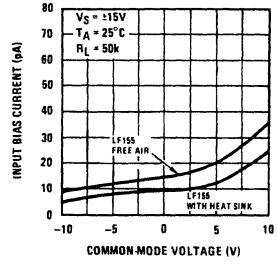
Typical DC Performance Characteristics

Curves are for LF155

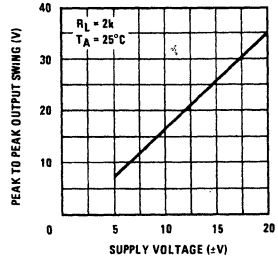
Input Bias Current



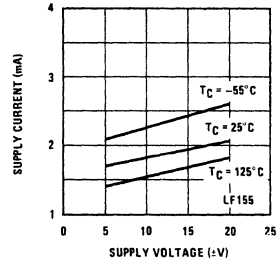
Input Bias Current



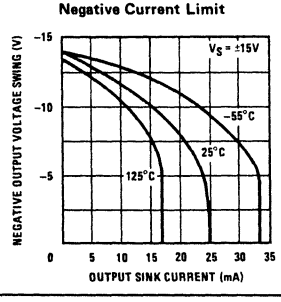
Voltage Swing



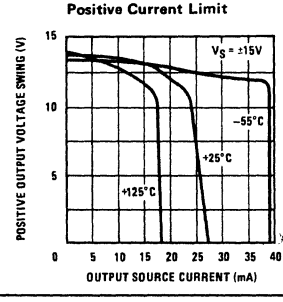
Supply Current



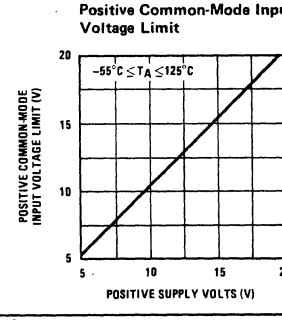
Negative Current Limit



Positive Current Limit

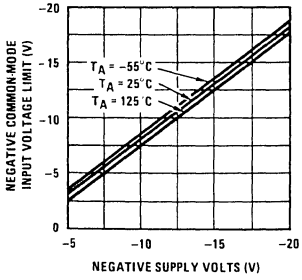


Positive Common-Mode Input Voltage Limit

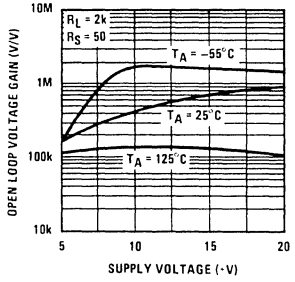


Typical DC Performance Characteristics (Continued)

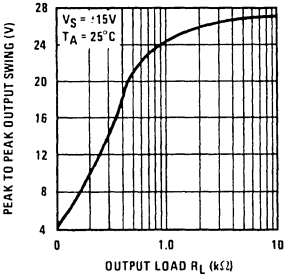
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain

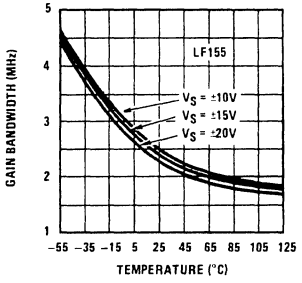


Output Voltage Swing

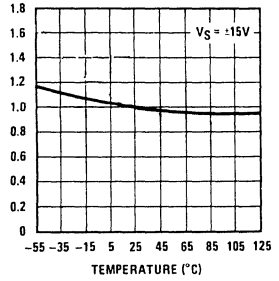


Typical AC Performance Characteristics

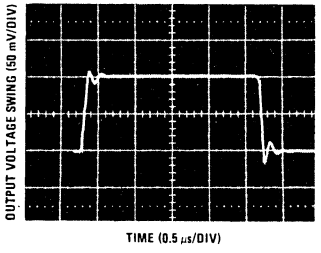
Gain Bandwidth



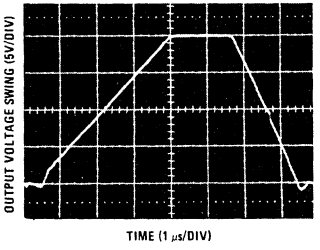
Normalized Slew Rate



LF155 Small Signal Pulse Response, $A_V = +1$

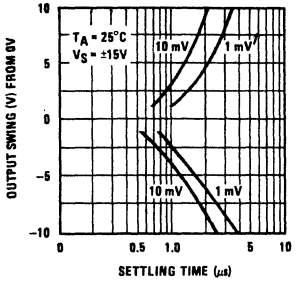


LF155 Large Signal Pulse Response, $A_V = +1$

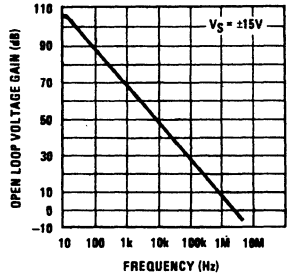


Typical AC Performance Characteristics (Continued)

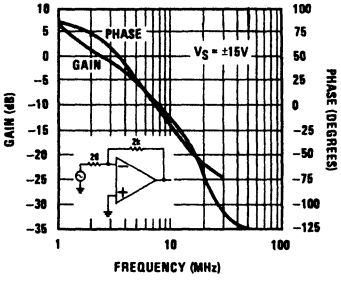
Inverter Settling Time



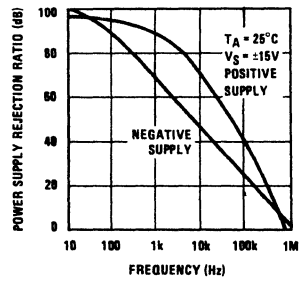
Open Loop Frequency Response



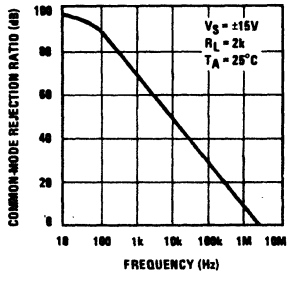
Bode Plot



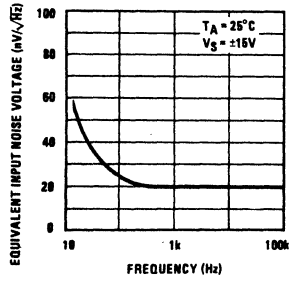
Power Supply Rejection Ratio



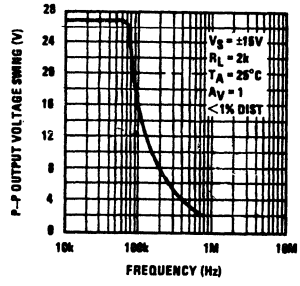
Common-Mode Rejection Ratio



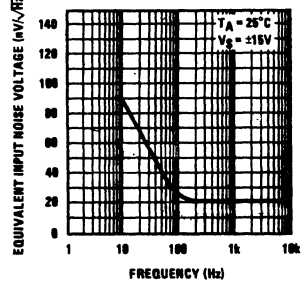
Equivalent Input Noise Voltage (Expanded Scale)



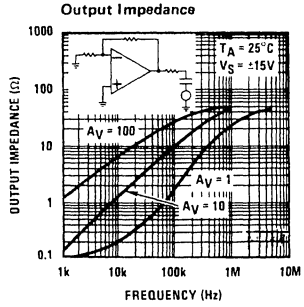
Undistorted Output Voltage Swing



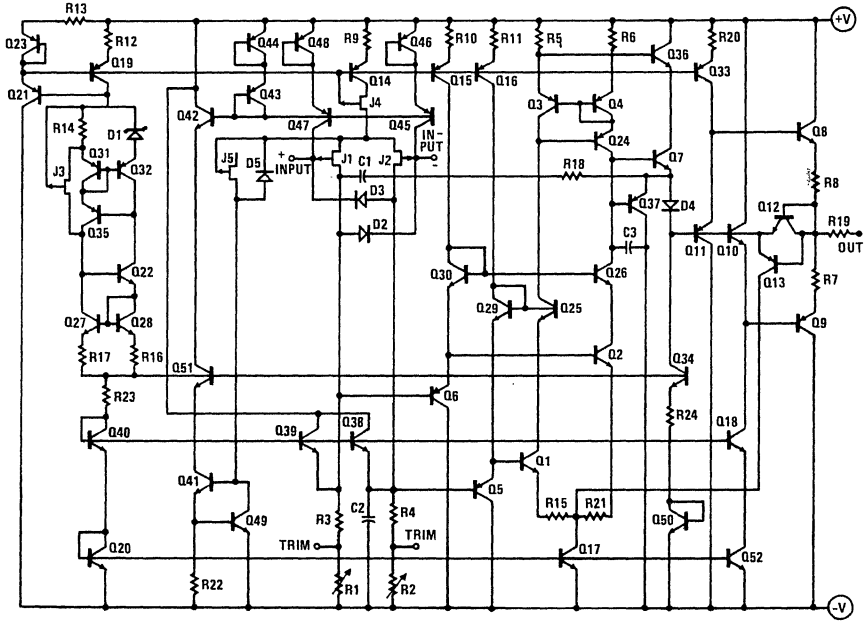
Equivalent Input Noise Voltage



Typical AC Performance Characteristics (Continued)



Detailed Schematic

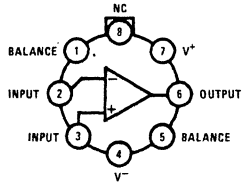


Connection Diagrams (Top Views) Section 11 for Packaging

Order Number
LF155AH
LF155H

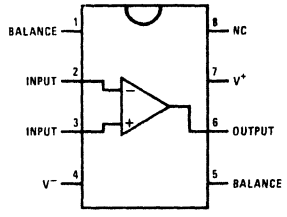
LF355AH
LF355H

Metal Can Package (H)



Note 4: Pin 4 connected to case.

Dual-In-Line Package (N or J)



Order Number LF355N
OR LM355J-8

Application Hints

The LF155 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

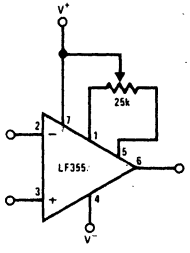
Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

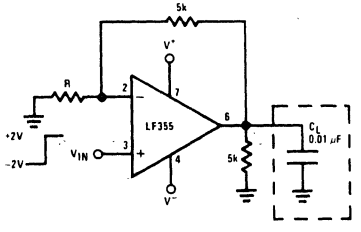
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C (0.5 μV/°C/mV of adj.)

Driving Capacitive Loads



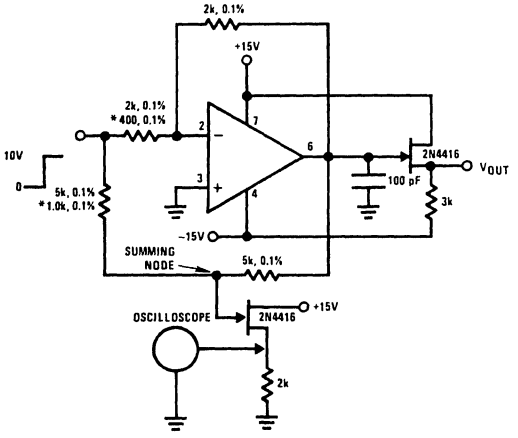
Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \sim 0.01\ \mu F$.

Overshoot ≤ 20%

Settling time (t_s) 5 μs

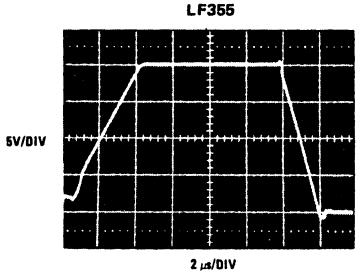
Typical Applications

Settling Time Test Circuit

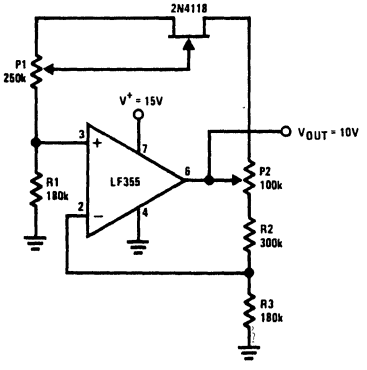


- Settling time is tested with the LF155 connected as unity gain inverter
- FET used to isolate the probe capacitance
- Output = 10V step

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)



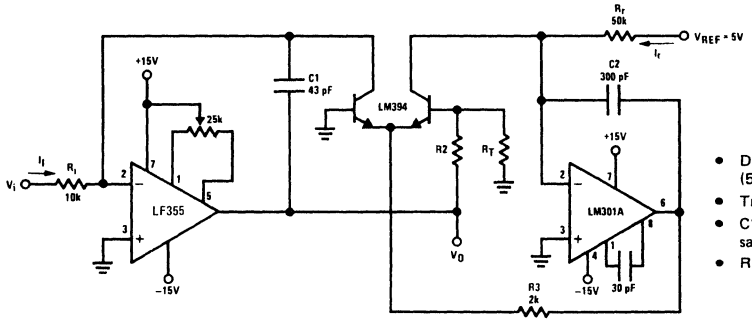
Low Drift Adjustable Voltage Reference



- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/^{\circ}C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - Low I_B
  - Low drift
  - Low supply current

Typical Applications (Continued)

Fast Logarithmic Converter

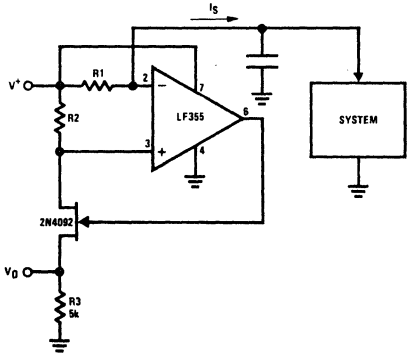


- Dynamic range: 100 $\mu A \leq I_i \leq 1$ mA (5 decades), $|V_O| = 1V$/decade
- Transient response: 3 μs for $\Delta I_i = 1$ decade
- C1, C2, R2, R3: added dynamic compensation
- R_T: Tel Labs type Q81 + 0.3%/°C

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \ln V_i \left[\frac{R_r}{V_{REF}\, R_i}\right] = \log V_i \frac{1}{R_i\, I_r}$$

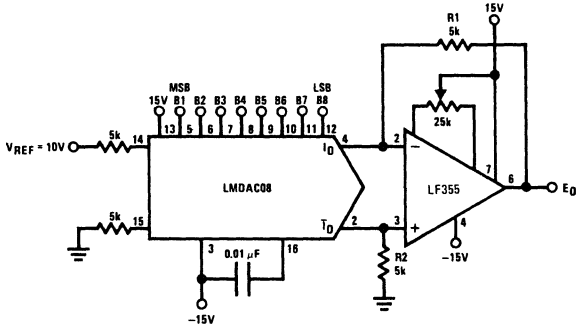
R2 = 15.7k, R_T = 1k, 0.3%/°C (for temperature compensation)

Precision Current Monitor



- V_O = 5 R1/R2 (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common-mode range to supply range
  - Low I_B
  - Low V_{OS}
  - Low supply current

8-Bit D/A Converter with Symmetrical Offset Binary Operation

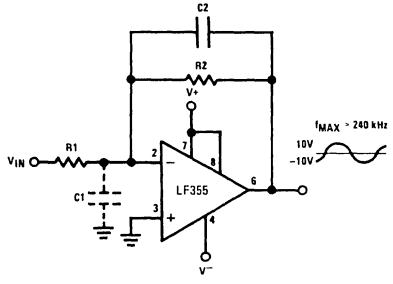


- R1, R2 should be matched within ±0.05%
- Full-scale response time: 3 μs

E_O	B1	B2	B3	B4	B5	B6	B7	B8	COMMENTS
+9.920	1	1	1	1	1	1	1	1	Positive Full-Scale
+0.040	1	0	0	0	0	0	0	0	(+) Zero-Scale
−0.040	0	1	1	1	1	1	1	1	(−) Zero-Scale
−9.920	0	0	0	0	0	0	0	0	Negative Full-Scale

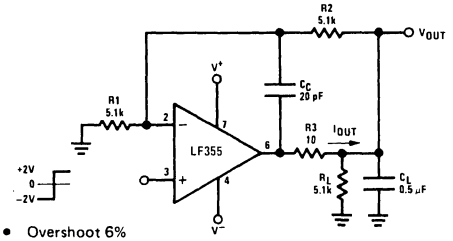
Typical Applications (Continued)

Wide BW Low Noise, Low Drift Amplifier



- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 240$ kHz
- Parasitic input capacitance C1 ≅ (3 pF for LF155 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

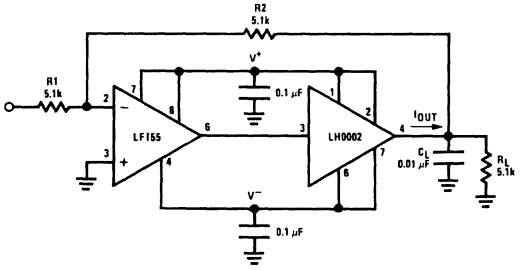
Isolating Large Capacitive Loads



- Overshoot 6%
- t_s 10 µs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

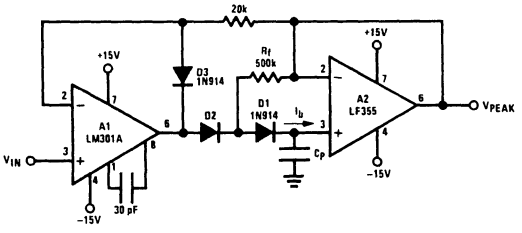
$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5} \text{ V/µs} = 0.04 \text{ V/µs (with } C_L \text{ shown)}$$

Boosting the LF155 with a Current Amplifier



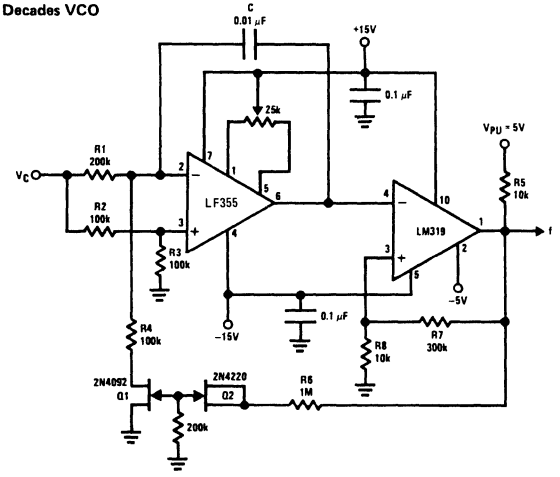
- $I_{OUT(MAX)} \cong 150$ mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}$ V/µs (with C_L shown)
- No additional phase shift added by the current amplifier

Low Drift Peak Detector



- By adding D1 and R_f, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through R_f
- Leakage of circuit is essentially I_b plus capacitor leakage of C_P.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be $<< 1/2\pi R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.

3 Decades VCO

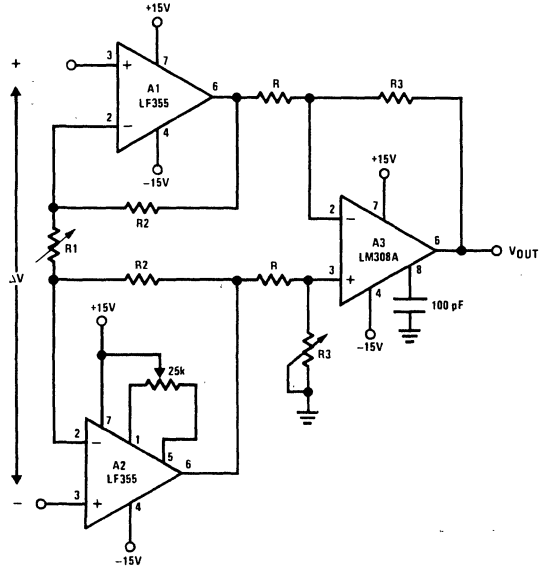


$$f = \frac{V_C (R8+R7)}{[8\, V_{PU}\, R8\, R1]\, C} \quad 0 \leq V_C \leq 30\text{V},\ 10\text{ Hz} \leq f \leq 10\text{ kHz}$$

R1, R4 matched. Linearity 0.1% over 2 decades.

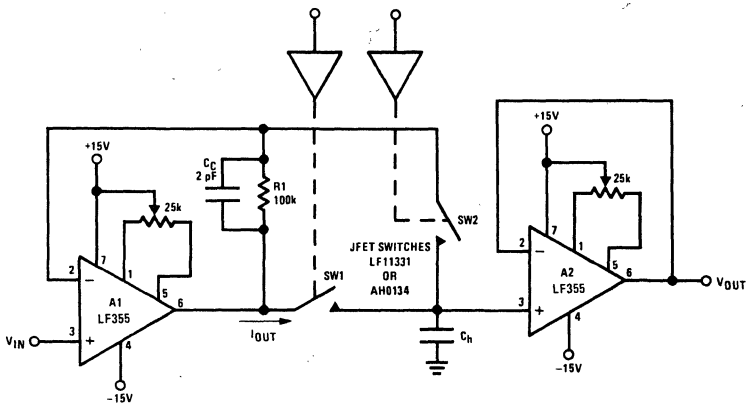
Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier



- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right] \Delta V, V^- + 2V \leq V_{IN}$ common-mode $\leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier Resistor array RA201 (National Semiconductor) recommended

Fast Sample and Hold



- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

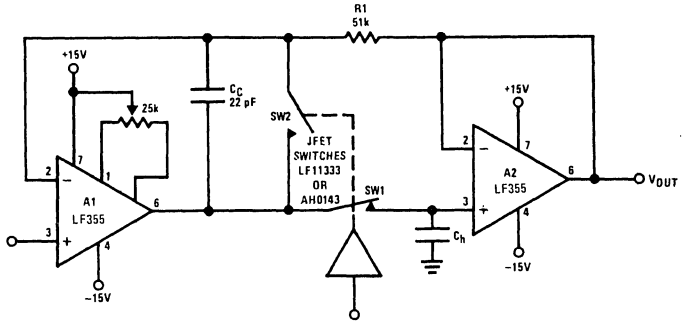
  $T_A \cong \left[\frac{2R_{ON} \cdot V_{IN} \cdot C_h}{S_r}\right]^{1/2}$ provided that:

  $V_{IN} < 2\pi S_r R_{ON} C_h$ and $T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}$, R_{ON} is of SW1

  If inequality not satisfied: $T_A \cong \frac{V_{IN} C_h}{20\ mA}$
- LF155 developes full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

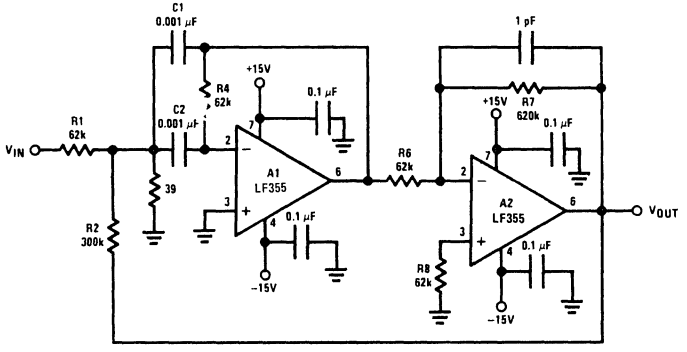
Typical Applications (Continued)

High Accuracy Sample and Hold



- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF155 for
  - ▲ Low V_{OS}

High Q Band Pass Filter

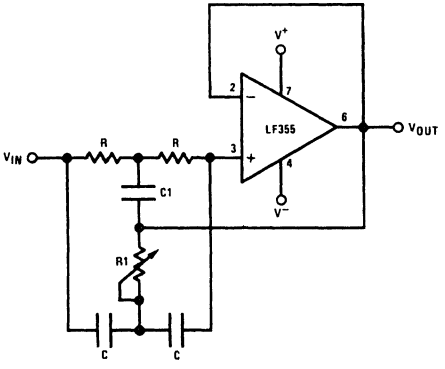


- By adding positive feedback (R2) Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 µs

High Q Notch Filter



- 2R1 = R = 10 MΩ
  2C = C1 = 300 pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - ▲ Low I_B
  - ▲ Low supply current

HARRIS

LF156 Monolithic JFET Input Operational Amplifiers LF156, LF156A, LF356,LF356A Wide Band

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

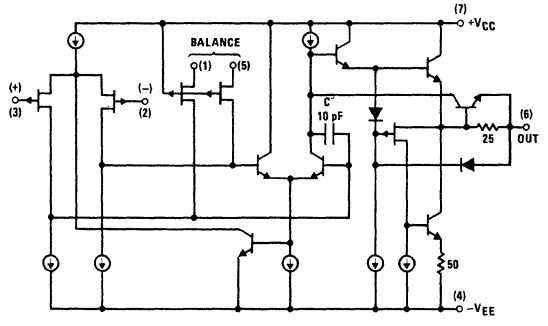
Features

LF156A

■ Low input bias current	30 pA
■ Low Input Offset Current	3 pA
■ High input impedance	$10^{12}\Omega$
■ Low input offset voltage	1 mV
■ Low input offset voltage temperature drift	$3\mu V/^{\circ}C$
■ Low input noise current	0.01 pA/$\sqrt{Hz}$
■ High common-mode rejection ratio	100 dB
■ Large dc voltage gain	106 dB

	LF156A	UNITS
■ Extremely fast settling time to 0.01%	1.5	μs
■ Fast slew rate	10	$V/\mu s$
■ Wide gain bandwidth	5	MHz
■ Low input noise voltage	18	nV/$\sqrt{Hz}$

Simplified Schematic



Absolute Maximum Ratings

	LM156/6A	LF356/6A
Supply Voltage	±22V	±18V
Power Dissipation (Note 1)	670 mW	500 mW
TO-99 (H package)		
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
$T_{j(MAX)}$	150°C	100°C
Differential Input Voltage	±40V	±30V
Input Voltage Range (Note 2)	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF156A			LF356A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{os}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		1	2		1	2	mV
		Over Temperature			2.5			2.5	mV
$\Delta V_{os}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3			5		μV/°C
$\Delta TC/\Delta V_{os}$	Change in Average TC with V_{os} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		μV/°C per mV
I_{os}	Input Offset Current	$T_j = 25°C$, (Notes 3, 6)		3	10		3	10	pA
		$T_j \leq T_{HIGH}$			10			1	nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 5)		30	50		30	50	pA
		$T_j \leq T_{HIGH}$			25			5	nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25°C$	50	200		50	200		V/mV
		$V_O = \pm 10V$, $R_L = 2k$							
		Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$	±12	±13		±12	±13		V
		$V_S = \pm 15V$, $R_L = 2k$	±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	±11	±12		±11	±12		V
CMRR	Common-mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm 15V$

SYMBOL	PARAMETER	CONDITIONS	LF156A/356A			UNITS
			MIN	TYP	MAX	
SR	Slew Rate		8	10		V/μs
GBW	Gain-Bandwidth Product		4	4.5		MHz
t_s	Settling Time to 0.01%	(Note 7)		1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$				
		f = 100 Hz		32		$nV/\sqrt{Hz}$
		f = 1000 Hz		18		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 100 Hz		0.01		$pA/\sqrt{Hz}$
		f = 1000 Hz		0.01		$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3		pF

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF156			LF356			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{os}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25^oC$ Over Temperature		3	5 7		3	10 13	mV mV
$\Delta V_{os}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5		$\mu V/^oC$
$\Delta TC/\Delta V_{os}$	Change in Average TC with V_{os} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		$\mu V/^oC$ per mV
I_{os}	Input Offset Current	$T_j = 25^oC$, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	20 20		3	50 2	pA nA
I_B	Input Bias Current	$T_j = 25^oC$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	100 50		30	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25^oC$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15V$, $T_A = 25^oC$ $V_O = \pm 10V$, $R_L = 2k$ Over Temperature	50 25	200		25 15	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k$ $V_S = \pm 15V$, $R_L = 10k$	± 12 ± 10	± 13 ± 12		± 12 ± 10	± 13 ± 12		V V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm 15V$	± 11	± 12		± 10	± 12		V
CMRR	Common-Mode Rejection Ratio		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		80	100		dB

DC Electrical Characteristics $T_A = 25^oC$, $V_S = \pm 15V$

PARAMETER	LF156A/156		LF356A/LF356		UNITS
	TYP	MAX	TYP	MAX	
Supply Current	5	7	5	10	mA

AC Electrical Characteristics $T_A = 25^oC$, $V_S = \pm 15V$

SYMBOL	PARAMETER	CONDITIONS	LF156	LF156/LF356	UNITS
			MIN	TYP	
SR	Slew Rate	LF156 $A_V = 1$	7.5	10	$V/\mu s$
GBW	Gain-Bandwidth Product			5	MHz
t_s	Settling Time to 0.01%	(Note 7)		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz f = 1000 Hz		 32 18	 $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f = 100 Hz f = 1000 Hz		0.01 0.01	$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3	pF

Notes for Electrical Characteristics

Note 1: The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case; for the DIP package, the device must be derated based on thermal resistance of 175°C/W junction to ambient.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ unless otherwise stated for the LF156/6A. For the LF356/6A these specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5 $\mu V/°C$ typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

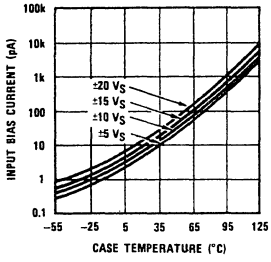
Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature. T_j temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta_{jA}$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

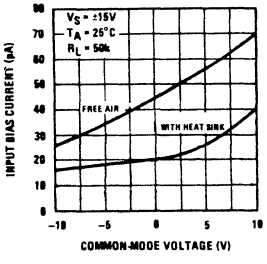
Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF156. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.0% of its final value from the time a 10V step input is applied.

Typical DC Performance Characteristics

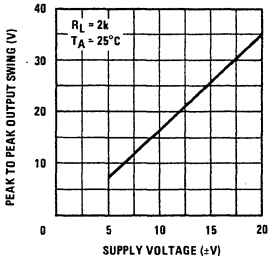
Input Bias Current



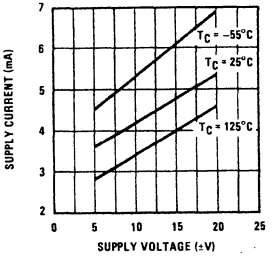
Input Bias Current



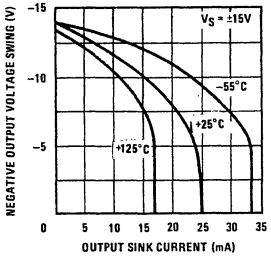
Voltage Swing



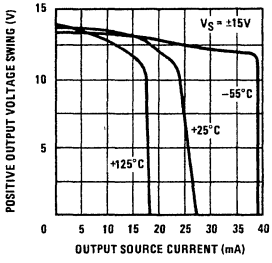
Supply Current



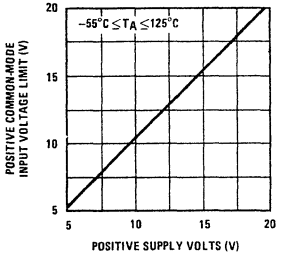
Negative Current Limit



Positive Current Limit

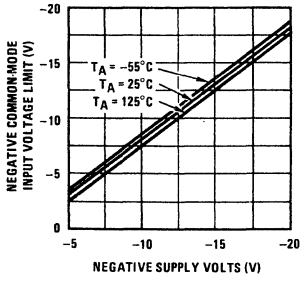


Positive Common-Mode Input Voltage Limit

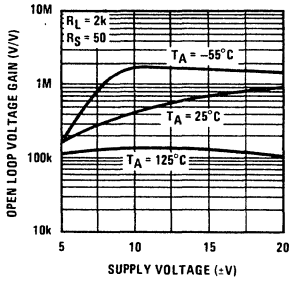


Typical DC Performance Characteristics (Continued)

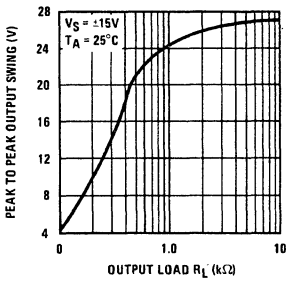
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain

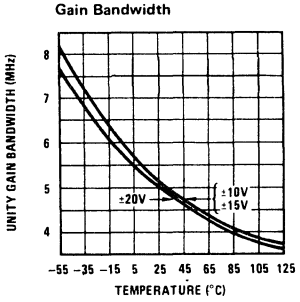


Output Voltage Swing

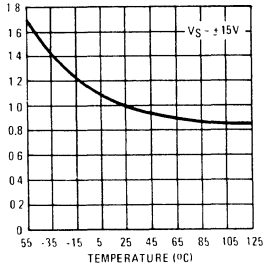


Typical AC Performance Characteristics

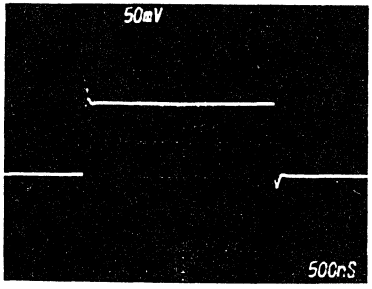
Gain Bandwidth



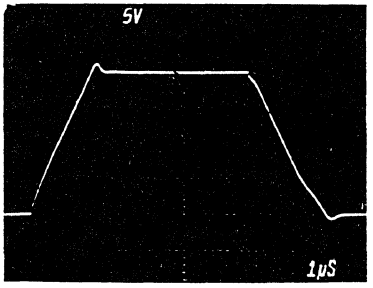
Normalized Slew Rate



LF156 Small Signal Pulse Response, A_V = +1

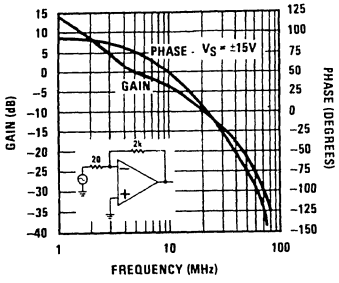


LF156 Large Signal Pulse Response, A_V = +1

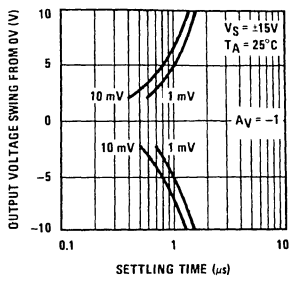


Typical AC Performance Characteristics (Continued)

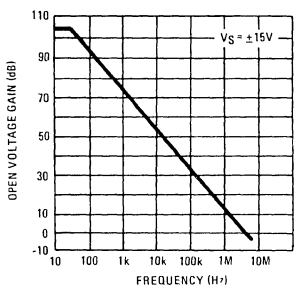
Bode Plot



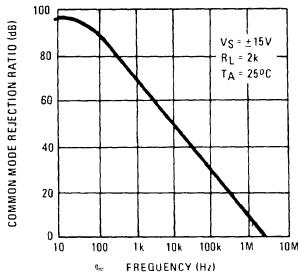
Inverter Settling Time



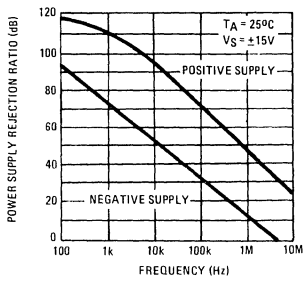
Open Loop Frequency Response



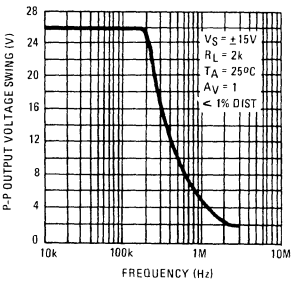
Common-Mode Rejection Ratio



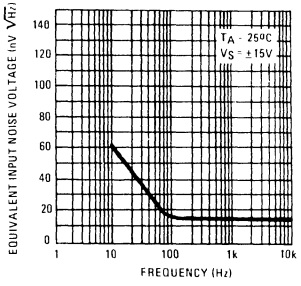
Supply Voltage Rejection Ratio



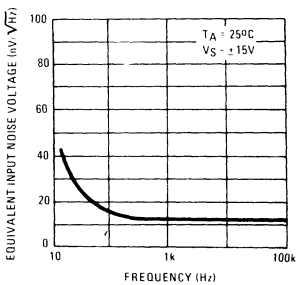
Undistorted Output Voltage Swing



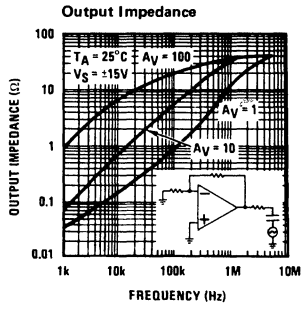
Equivalent Input Noise Voltage



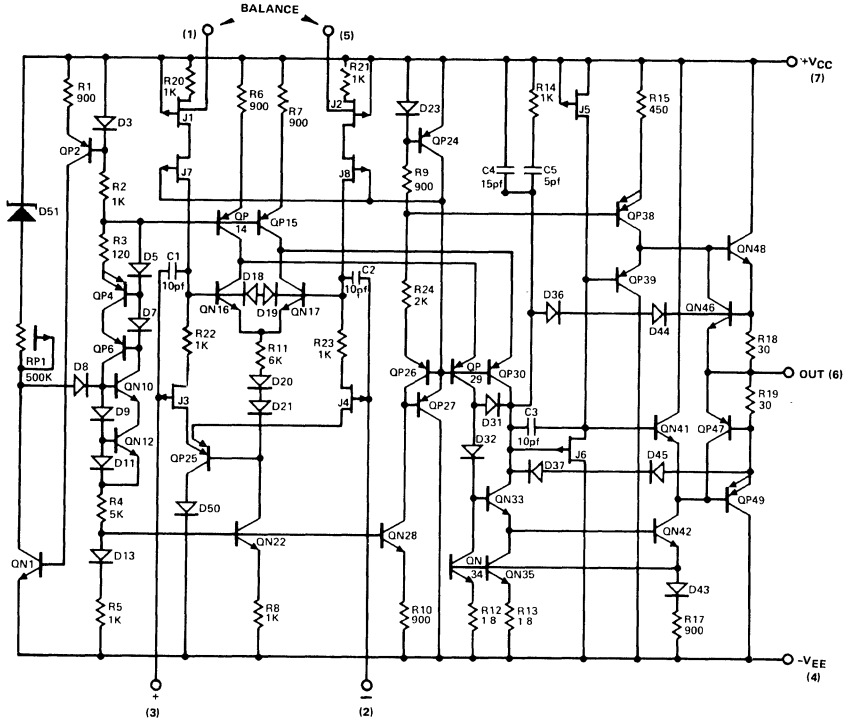
Equivalent Input Noise Voltage (Expanded Scale)



Typical AC Performance Characteristics (Continued)



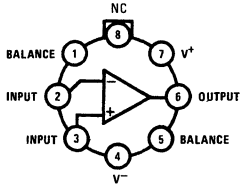
Detailed Schematic



Connection Diagrams (Top Views) Section 11 for Packaging

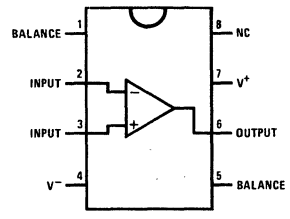
Order Number
LF156AH
LF156H
LF356AH
LF356H

Metal Can Package



Note 4: Pin 4 connected to case.

Dual-In-Line Package



Order Number LF356N, LF356J-8

Application Hints

The LF156/6A series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

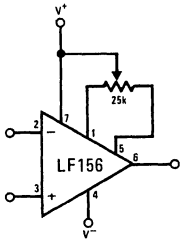
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels if greater than or equal to the original feedback pole time constant.

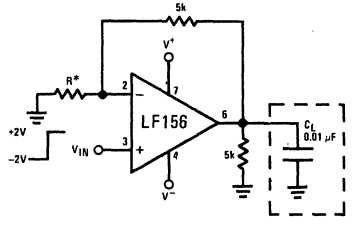
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ±(0.5 μV/°C/mV of adj.)

Driving Capacitive Loads



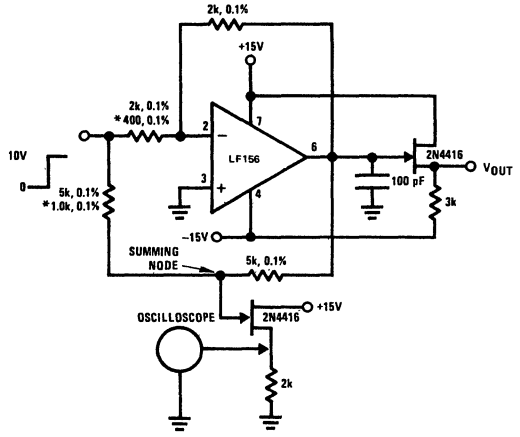
Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L(MAX)} \cong 0.01\ \mu F$.

Overshoot $\leq$ 20%

Settling time (t_s) ≅ 5 μs

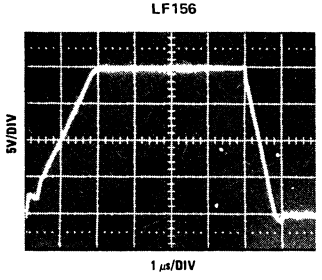
Typical Applications

Settling Time Test Circuit

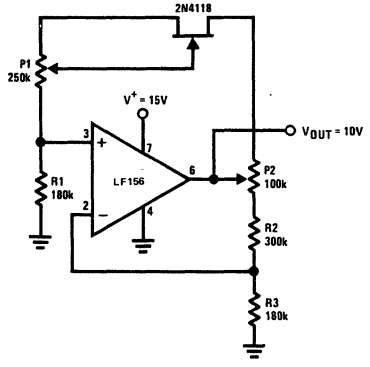


- Settling time is tested with the LF156 connected as unity gain inverter
- FET used to isolate the probe capacitance
- Output = 10V step

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)



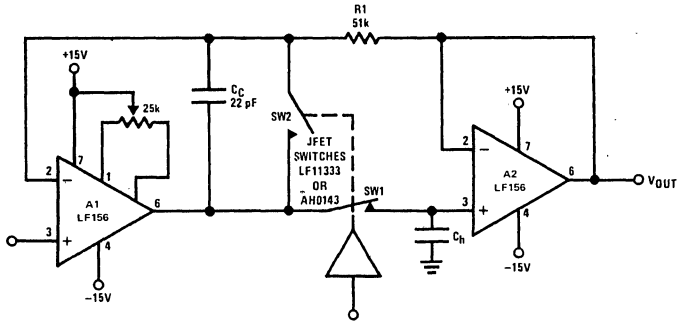
Low Drift Adjustable Voltage Reference



- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/^{o}C$
- All resistors and potentiometers should be wire-bound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF156 for
  - Low I_B
  - Low drift

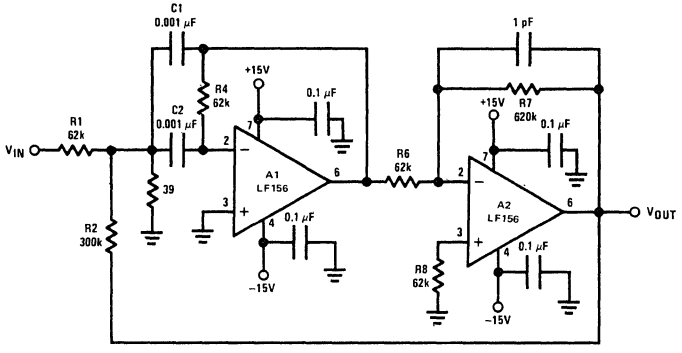
Typical Applications (Continued)

High Accuracy Sample and Hold



- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - Fast settling time
  - Low V_{OS}

High Q Band Pass Filter

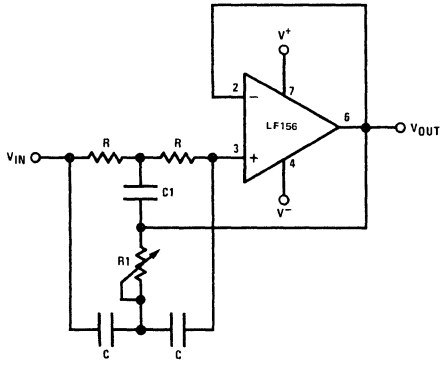


- By adding positive feedback (R2) Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 μs

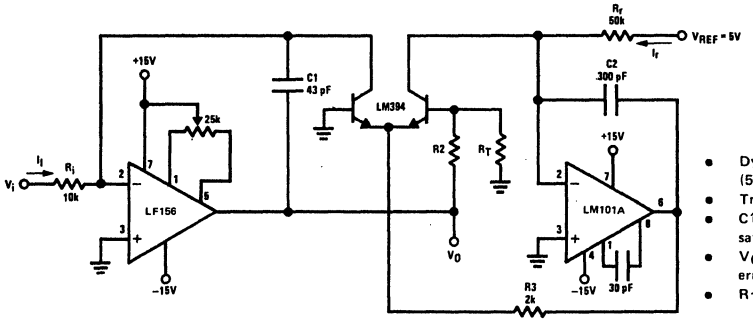
High Q Notch Filter



- 2R1 = R = 10 MΩ
  2C = C1 = 300 pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100

Typical Applications (Continued)

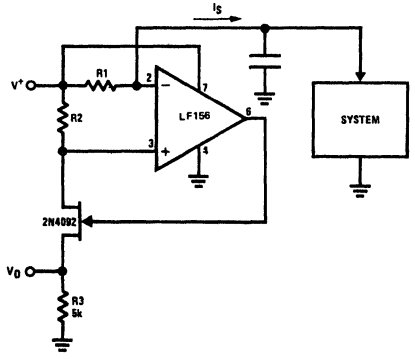
Fast Logarithmic Converter



- Dynamic range: 100 $\mu A \leq I_i \leq 1mA$ (5 decades), V_O = 1V/decade
- Transient response : 3 μs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type 081 + 0.3%/°C

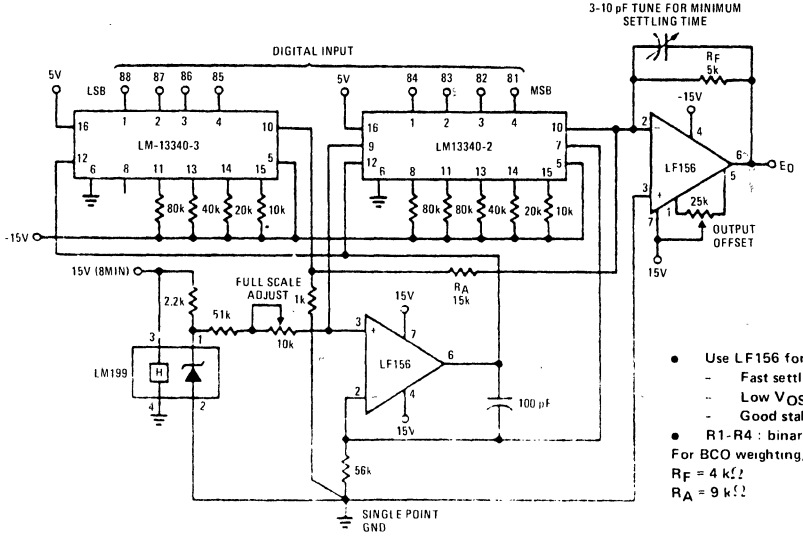
$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right] \frac{kT}{q} \ln V_i \left[\frac{R_r}{V_{REF}\, R_i}\right] = \log V_i \frac{1}{R_i I_r}$$ R2 = 15.7k, R_T = 1k, 0.3%/°C (for temperature compensation)

Precision Current Monitor



- $V_O = 5 \frac{R1}{R2}$ (V/mA of I_S)
- R1, R2, R+: 0.1% resistors
- Use LF156 for
  - Common-mode range to supply voltage
  - Low I_B
  - Low V_{OS}

Temperature Compensated 8-Bit D/A Converter

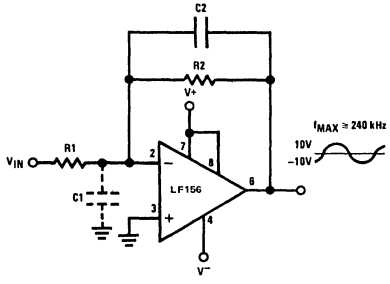


- Use LF156 for
  - Fast settling time
  - Low V_{OS} drift
  - Good stability
- R1-R4 : binary ladder

For BCO weighting,
R_F = 4 kΩ
R_A = 9 kΩ

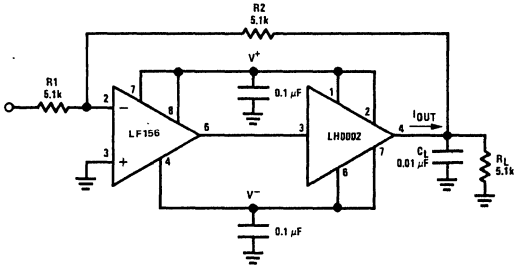
Typical Applications (Continued)

Wide BW Low Noise, Low Drift Amplifier



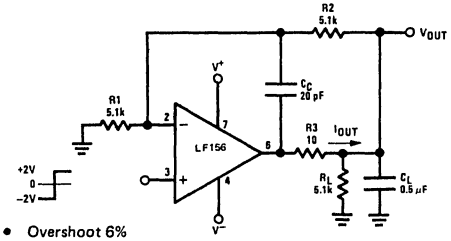
- Power BW: $f_{MAX} = \frac{S_r}{2\pi V_P} \cong 240$ kHz
- Parasitic input capacitance C1 ≅ (3 pF for LF156 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that : R2C2 ≅ R1C1.

Boosting the LF156 with a Current Amplifier



- $I_{OUT(MAX)} \cong 150$ mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}}$ V/μs (with C_L shown)
- No additional phase shift added by the current amplifier

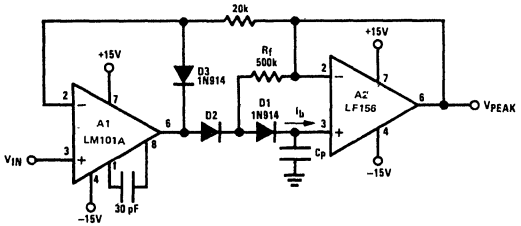
Isolating Large Capacitive Loads



- Overshoot 6%
- t_s 10 μs
- When driving large C_L, the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5} \text{ V/μs} = 0.04 \text{ V/μs (with } C_L \text{ shown)}$$

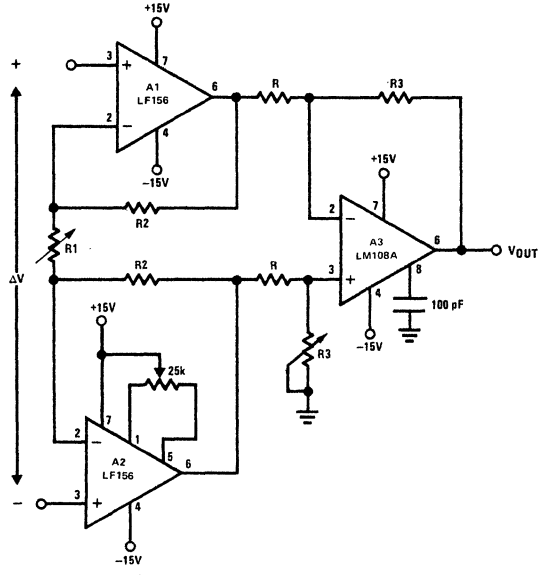
Low Drift Peak Detector



- By adding D1 and R_f, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b (ILF156) plus capacitor leakage of C_P.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be $<< 1/2\pi R_f C_{D2}$ where C_{D2} is the shunt capacitance of D2.

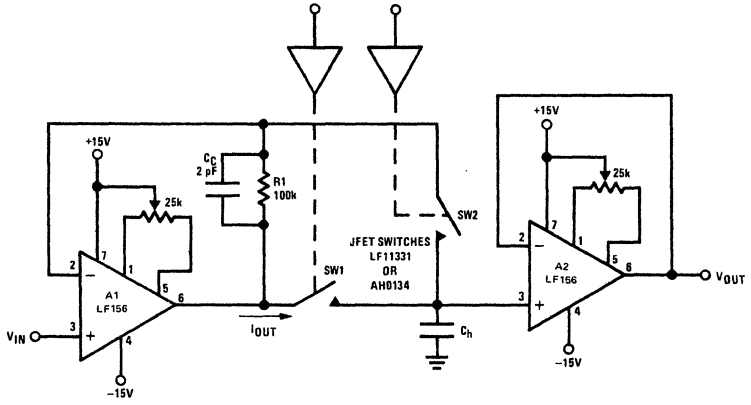
Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier



- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right] \Delta V, V^- + 2V \leq V_{IN}$ common-mode $\leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier Resistor array RA201 (National Semiconductor) recommended

Fast Sample and Hold



- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A, estimated by:

  $T_A \cong \left[\frac{2R_{ON} \cdot V_{IN} \cdot C_h}{S_r}\right]^{1/2}$ provided that:

  $V_{IN} < 2\pi S_r R_{ON} C_h$ and $T_A > \frac{V_{IN} C_h}{I_{OUT(MAX)}}$, R_{ON} is of SW1

  If inequality not satisfied: $T_A \cong \frac{V_{IN} C_h}{20\ mA}$
- LF156 developes full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

LF157 Monolithic JFET Input Operational Amplifiers

LF157, LF157A, LF357, LF357A

Wide Band Decompensated ($A_{V_{MIN}}$ = 10)

General Description

These are among the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and low 1/f noise corner.

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

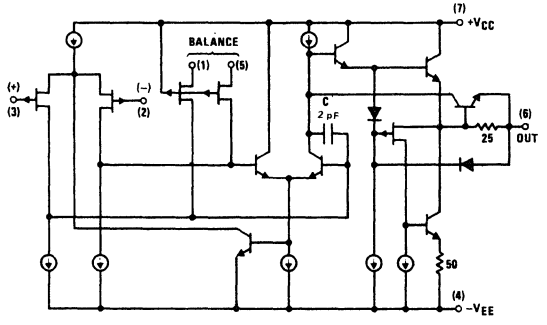
Features

LF157A

Low input bias current	30 pA
Low Input Offset Current	3 pA
High input impedance	$10^{12}\Omega$
Low input offset voltage	1 mV
Low input offset voltage temperature drift	3μV/°C
Low input noise current	0.01 pA/$\sqrt{Hz}$
High common-mode rejection ratio	100 dB
Large dc voltage gain	106 dB

	LF157A (A_V = 10)	UNITS
Extremely fast settling time to 0.01%	1.5	μs
Fast slew rate	50	V/μs
Wide gain bandwidth	20	MHz
Low input noise voltage	18	nV/$\sqrt{Hz}$

Simplified Schematic



Absolute Maximum Ratings

	LF157A	LF157	LF357A/LF357
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 1)	670 mW	670 mW	500 mW
TO-99)H package)			
Operating Temperature Range	-55°C to +125°C	-55°C to +125°C	0°C to +70°C
T_j(MAX)	150°C	150°C	100°C
Differential Input Voltage	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF157A			LF357A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{os}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ Over Temperature		1	2 2.5		1	2 2.3	mV mV
$\Delta V_{os}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3			3		µV/°C
$\Delta TC/\Delta V_{os}$	Change in Average TC with V_{os} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		µV/°C per mV
I_{os}	Input Offset Current	$T_j = 25°C$, (Notes 3, 6) $T_j \leq T_{HIGH}$		3	10 10		3	10 1	pA nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	50 25		30	50 5	pA nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$ $V_O = \pm10V$, $R_L = 2k$ Over Temperature	50	200		50 25	200		V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$ $V_S = \pm15V$, $R_L = 2k$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11 	 ±12		±11 	 ±12		V V
CMRR	Common-mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF157A/357A			UNITS
			MIN	TYP	MAX	
SR	Slew Rate	LF157A: $A_V = 5$	40	50		V/µs
GBW	Gain-Bandwidth Product		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		1.5		µs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz f = 1000 Hz		 32 18		 nV/√Hz nV/√Hz
i_n	Equivalent Input Noise Current	f = 100 Hz f = 1000 Hz		0.01 0.01		pA/√Hz pA/√Hz
C_{IN}	Input Capacitance			3		pF

DC Electrical Characteristics (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF157			LF357			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{os}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25^oC$ Over Temperature		3	5 7		3	10 13	mV mV
$\Delta V_{os}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5		$\mu V/^oC$
$\Delta TC/\Delta V_{os}$	Change in Average TC with V_{os} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		$\mu V/^oC$ per mV
I_{os}	Input Offset Current	$T_j = 25^oC$, (Notes 3, 5) $T_j \leq T_{HIGH}$		3	20 20		3	50 2	pA nA
I_B	Input Bias Current	$T_j = 25^oC$, (Notes 3, 5) $T_j \leq T_{HIGH}$		30	100 50		30	200 8	pA nA
R_{IN}	Input Resistance	$T_j = 25^oC$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25^oC$ $V_O = \pm10V$, $R_L = 2k$ Over Temperature	50 25	200		50 15	200		V/mV V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$ $V_S = \pm15V$, $R_L = 10k$	±12 ±10	±13 ±12		±12 ±10	±13 ±12		V V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	±12		±10	±12		V V
CMRR	Common-Mode Rejection Ratio		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		80	100		dB

DC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

PARAMETER	LF157A/LF157		LF357A/LF357		UNITS
	TYP	MAX	TYP	MAX	
Supply Current	5	7	5	10	mA

AC Electrical Characteristics $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF157	LF157/357	UNITS
			MIN	TYP	
SR	Slew Rate	LF157: $A_V = 10$	30	50	$V/\mu s$
GBW	Gain-Bandwidth Product			20	MHz
t_s	Settling Time to 0.01%	(Note 7)		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$ f = 100 Hz f = 1000 Hz		 32 18	 $nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f = 100 Hz f = 1000 Hz		0.01 0.01	$pA/\sqrt{Hz}$ $pA/\sqrt{Hz}$
C_{IN}	Input Capacitance			3	pF

Notes for Electrical Characteristics

Note 1: The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case; for the DIP package, the device must be derated based on thermal resistance of 175°C/W junction to ambient.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for $\pm 15V \leq V_S < \pm 20V$, $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ unless otherwise stated for the LF157A and the LF157. For the LF357/LF357A these specifications apply for $\pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS} I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The temperature coefficient of the adjusted input offset voltage changes only a small amount (0.5 $\mu V/°C$ typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \theta_{jA} Pd$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

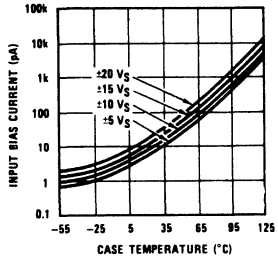
Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time as defined here, is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -10$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit, page 9).

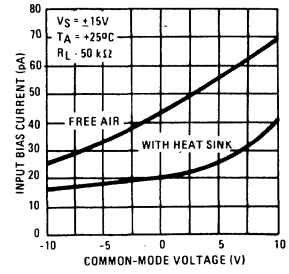
2

Typical DC Performance Characteristics Curves are for LF157 unless otherwise specified.

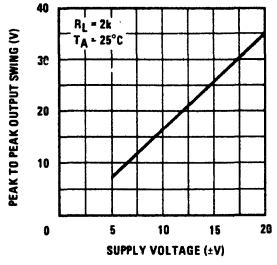
Input Bias Current



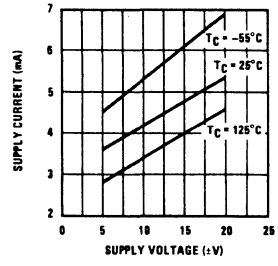
Input Bias Current



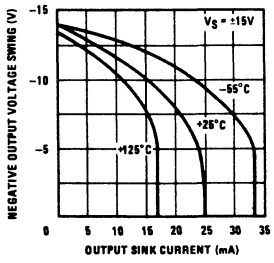
Voltage Swing



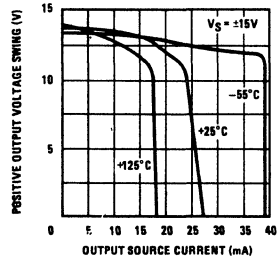
Supply Current



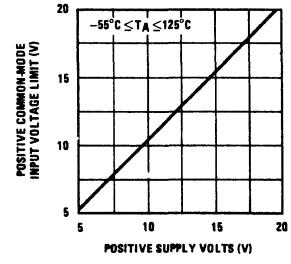
Negative Current Limit



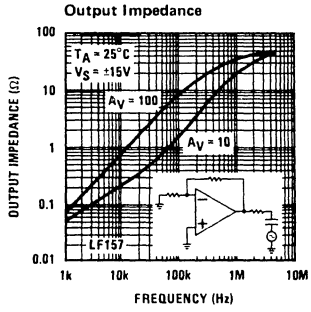
Positive Current Limit



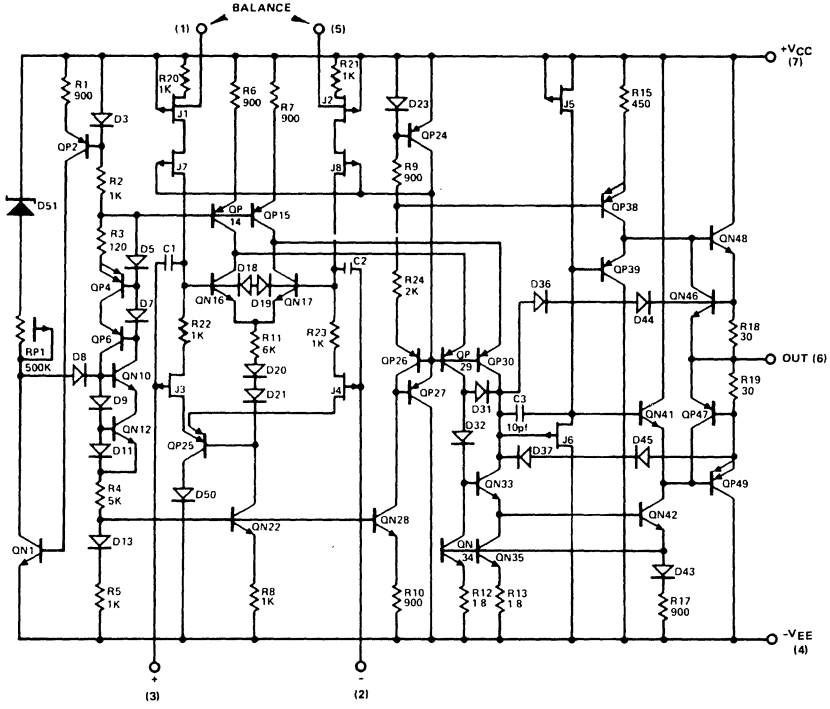
Positive Common-Mode Input Voltage Limit



Typical AC Performance Characteristics (Continued)



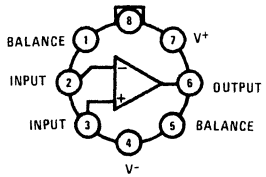
Detailed Schematic



Connection Diagrams Section 11 for Packaging

Order Number
LF157AH
LF157H
LF357AH
LF357H

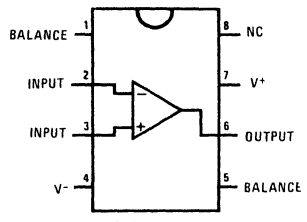
Metal Can Package



Note 4: Pin 4 connected to case.

TOP VIEW

Dual-In-Line Package



Order Number
LF357J-8, LF357N

TOP VIEW

Application Hints

The LF157 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accomodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

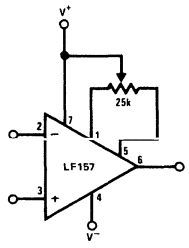
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant

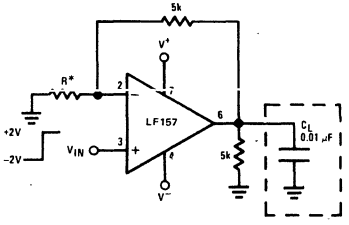
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5 μV/°C/mV of adjustment
- Typical overall drift: 5 μV/°C ±(0.5 μV/°C/mV of adj.)

Driving Capacitive Loads



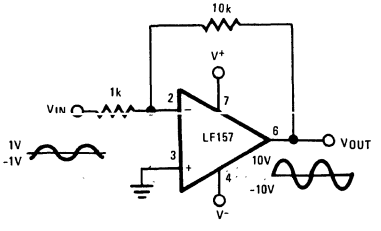
Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability.

$C_{L(MAX)} \cong 0.01\ \mu F$

Overshoot $\leq 20\%$

Settling time (t_s) $\cong 5\ \mu s$

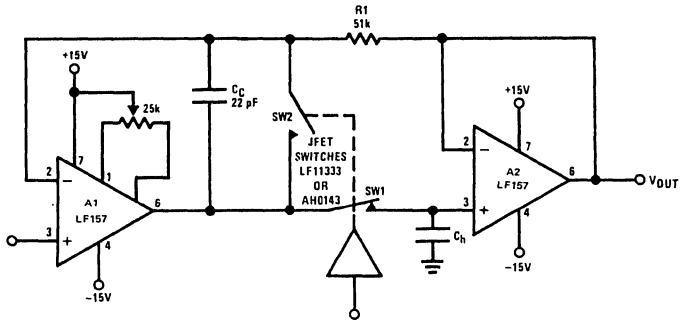
LF157. A Large Power BW Amplifier



For distortion < 1% and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500 kHz

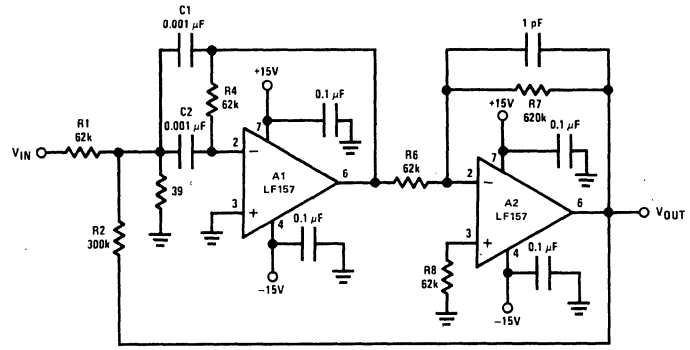
Typical Applications (Continued)

High Accuracy Sample and Hold



- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation

High Q Band Pass Filter



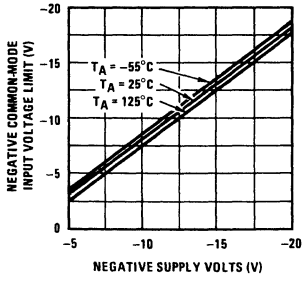
- By adding positive feedback (R2) Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

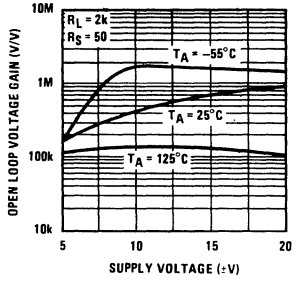
- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300 μs

Typical DC Performance Characteristics (Continued)

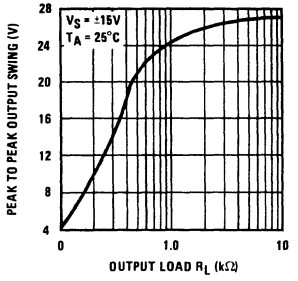
Negative Common-Mode Input Voltage Limit



Open Loop Voltage Gain

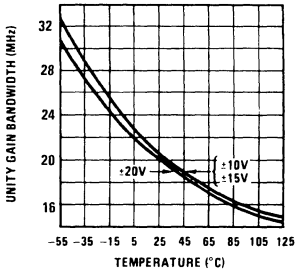


Output Voltage Swing

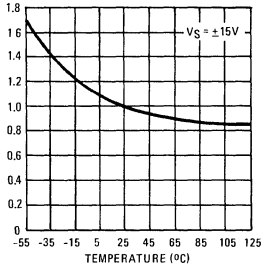


Typical AC Performance Characteristics

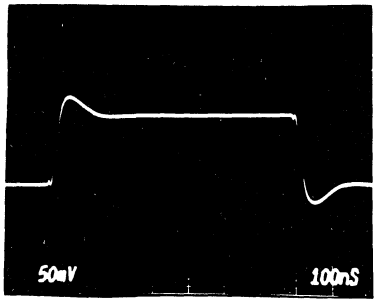
Gain Bandwidth



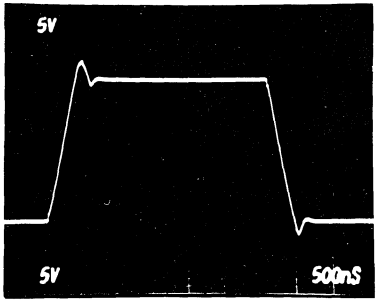
Normalized Slew Rate



LF157 Small Signal Pulse Response, A_V = +10

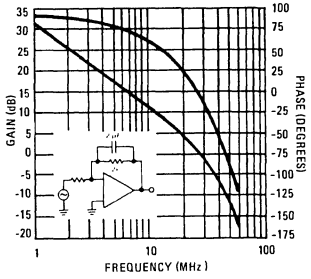


LF157 Large Signal Pulse Response, A_V = +10

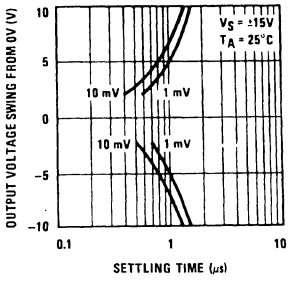


Typical AC Performance Characteristics (Continued)

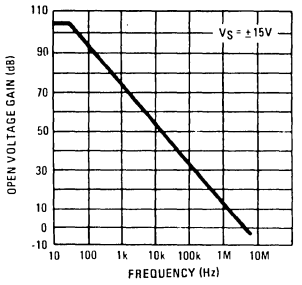
Bode Plot



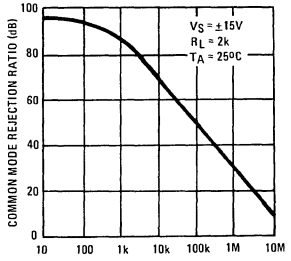
Inverter Settling Time



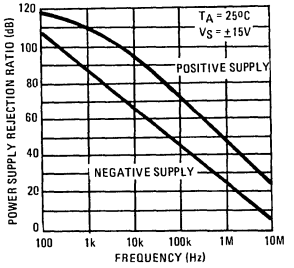
Open Loop Frequency Response



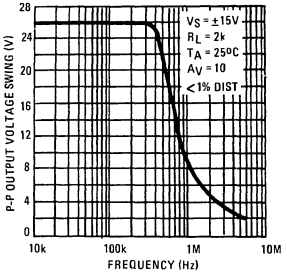
Common-Mode Rejection Ratio



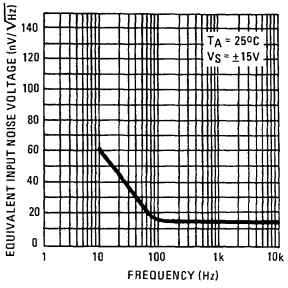
Power Supply Rejection Ratio



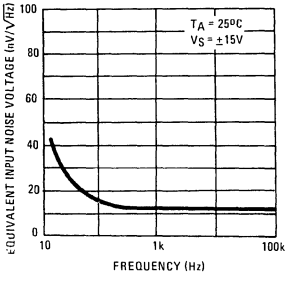
Undistorted Output Voltage Swing



Equivalent Input Noise Voltage

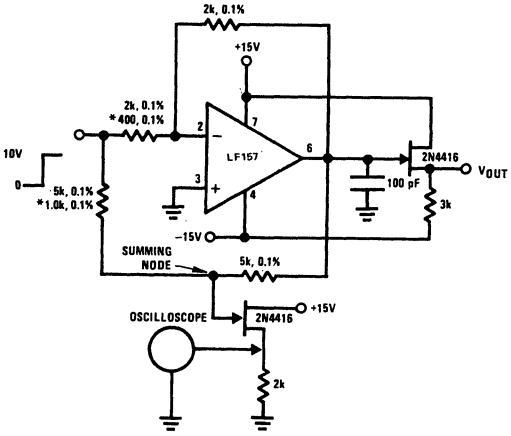


Equivalent Input Noise Voltage (Expanded Scale)



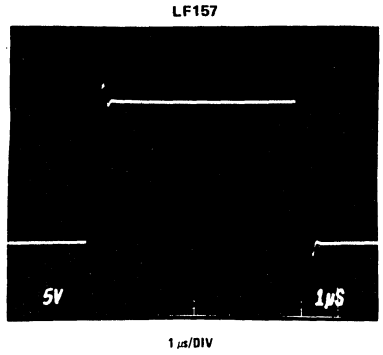
Typical Applications

Settling Time Test Circuit



- Settling time is tested with the LF157 connected for $A_V = -10$
- FET used to isolate the probe capacitance
- Output = 10V step

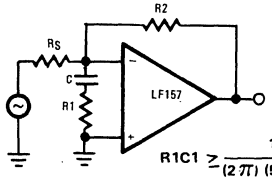
Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)



1 μs/DIV

Low Drift Adjustable Voltage Reference

Non-Inverting Unity Gain Operation for LF157



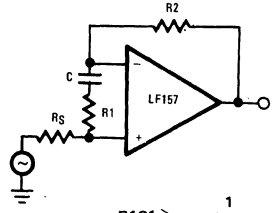
$$R1C1 \geq \frac{1}{(2\pi)\,(5\ \text{MHz})}$$

$$R1 = \frac{R2 + R_S}{4}$$

$A_{V(DC)} = 1$

$f_{-3dB} \approx 5\text{MHz}$

Inverting Unity Gain for LF157



$$R1C1 \geq \frac{1}{(2\pi)\,(5\ \text{MHz})}$$

$$R1 = \frac{R2}{4}$$

$A_{V(DC)} = -1$

$f_{-3dB} \approx 5\text{MHz}$

LF347 Wide Bandwidth Quad JFET Input Operational Amplifier

General Description

The Harris LF347 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage. The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF347 is pin compatible with the standard LM348. This feature allows designers to immediately upgrade the overall performance of existing LM348 and LM324 designs.

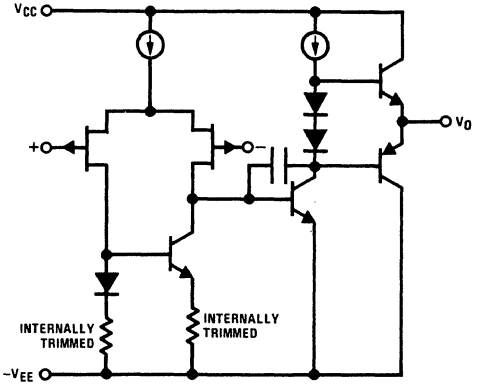
The LF347 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

- Internally trimmed offset voltage — 2 mV
- Low input bias current — 50 pA
- Low input noise voltage — 16 nV/$\sqrt{Hz}$
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 7.2 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

Simplified Schematic

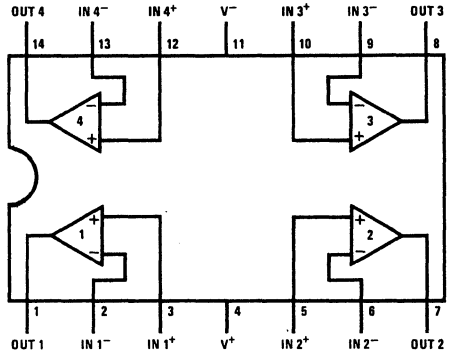
1/4 Quad



Connection Diagram

Section 11 for Packaging

Dual-In-Line Package



TOP VIEW

Order Number LF347N, LF347AN or LF347BN

Order Number LF347J, LF347AJ or LF347BJ

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF347A			LF347B			LF347			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		1	2		3	5		5	10	mV
		Over Temperature			4			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10			10			10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 4, 5)		25	100		25	100		25	100	pA
		$T_j \leq 70°C$			2			4			4	nA
I_B	Input Bias Current	T_j = 25°C, (Notes 4, 5)		50	200		50	200		50	200	pA
		$T_j \leq 70°C$			4			8			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C	50	100		50	100		25	100		V/mV
		V_O = ±10V, R_L = 2 kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq 10$ kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF347A			LF347B			LF347			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1 Hz–20 kHz (Input Referred)		−120			−120			−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C		13			13			13		V/µs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C		4			4			4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		16			16			16		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 125°C/W junction to ambient or 95°C/W junction to case.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: P_D max rating cannot be exceeded.

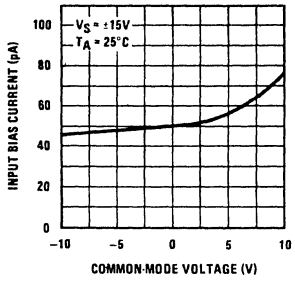
Note 4: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

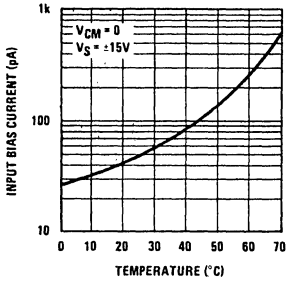
Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

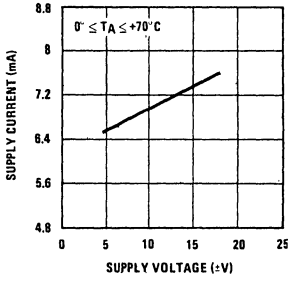
Input Bias Current



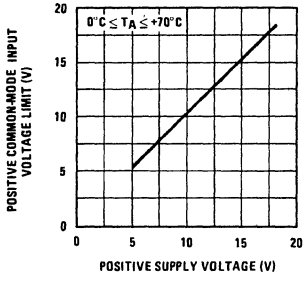
Input Bias Current



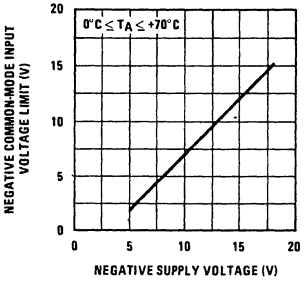
Supply Current



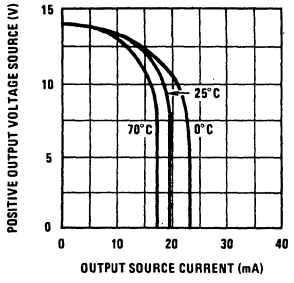
Positive Common-Mode Input Voltage Limit



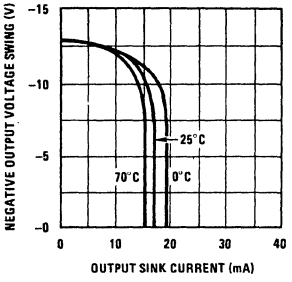
Negative Common-Mode Input Voltage Limit



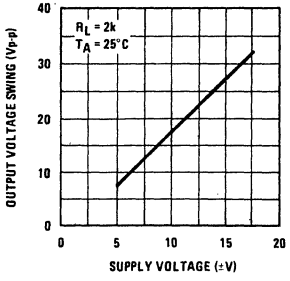
Positive Current Limit



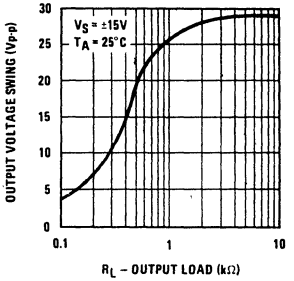
Negative Current Limit



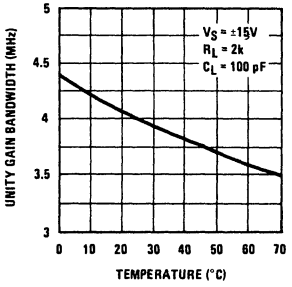
Voltage Swing



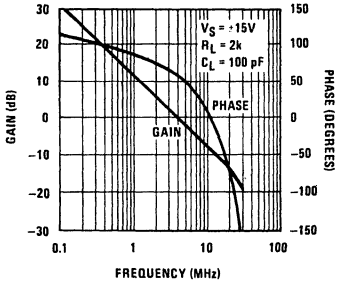
Output Voltage Swing



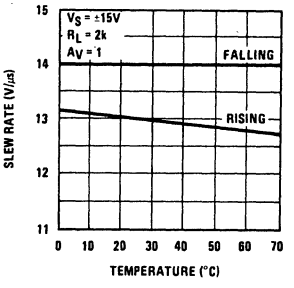
Gain Bandwidth



Bode Plot

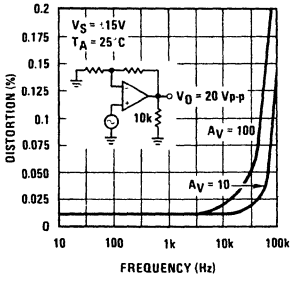


Slew Rate

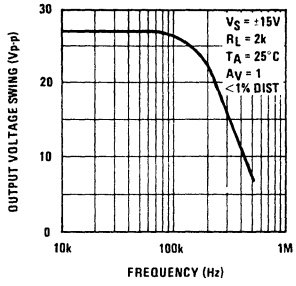


Typical Performance Characteristics (Continued)

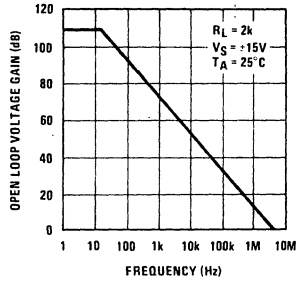
Distortion vs Frequency



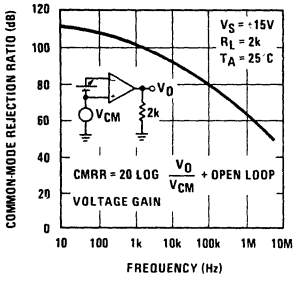
Undistorted Output Voltage Swing



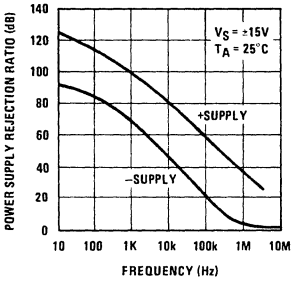
Open Loop Frequency Response



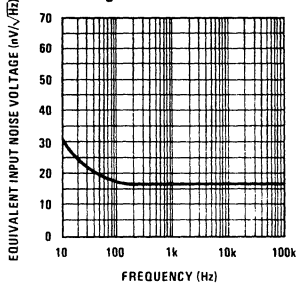
Common-Mode Rejection Ratio



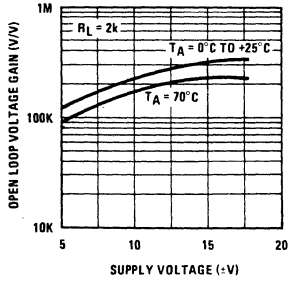
Power Supply Rejection Ratio



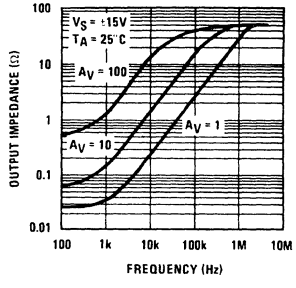
Equivalent Input Noise Voltage



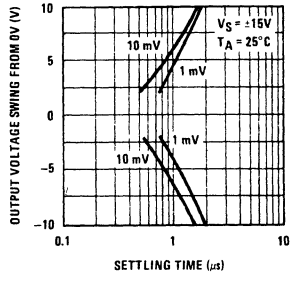
Open Loop Voltage Gain (V/V)



Output Impedance

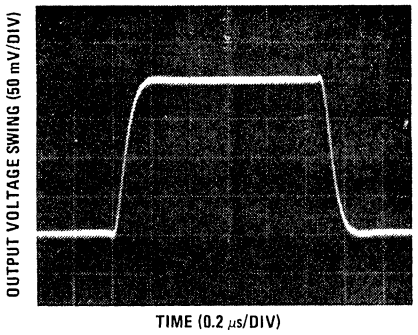


Inverter Settling Time

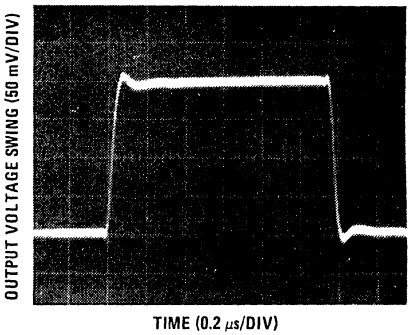


Pulse Response

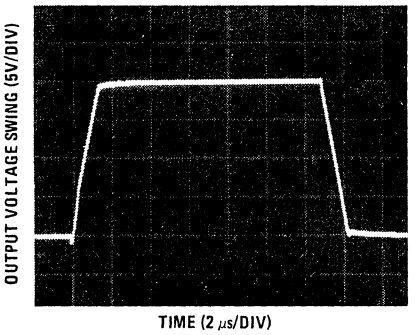
Small Signal Inverting



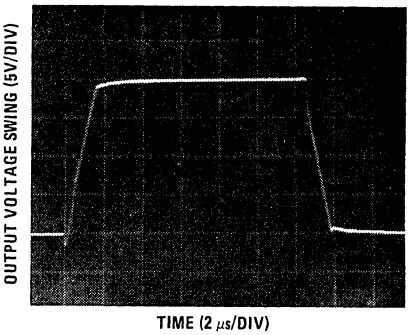
Small Signal Non-Inverting



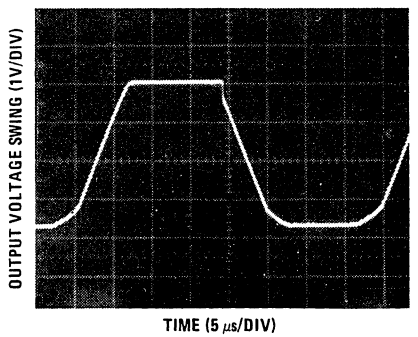
Large Signal Inverting



Large Signal Non-Inverting



Current Limit (R_L = 100Ω)



Application Hints

The LF347 is an op amp with an internally trimmed input offset voltage and JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF347 will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

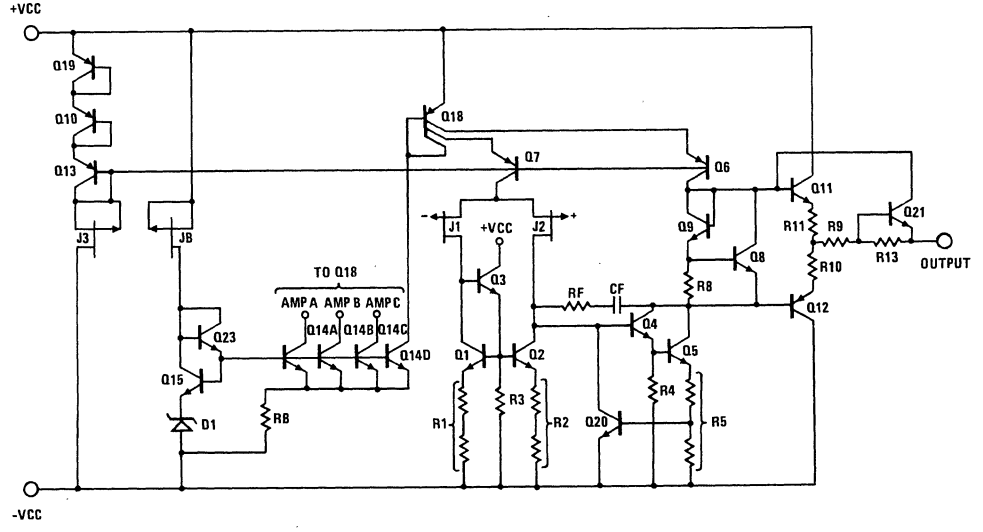
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

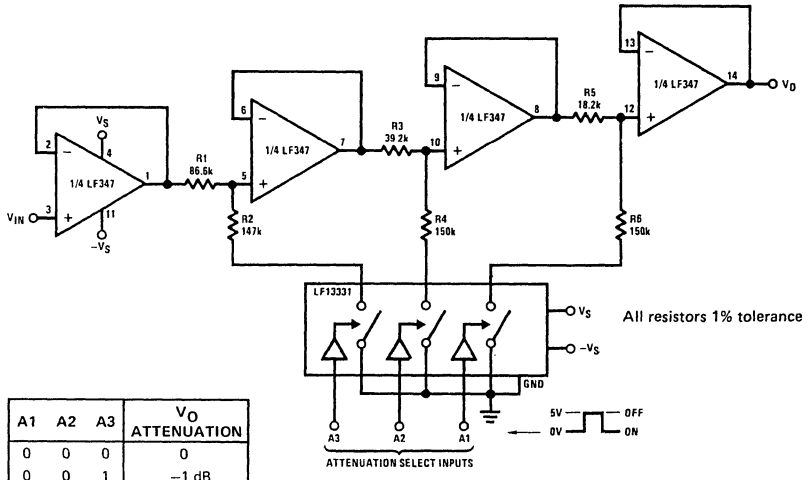
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



Typical Applications

Digitally Selectable Precision Attenuator

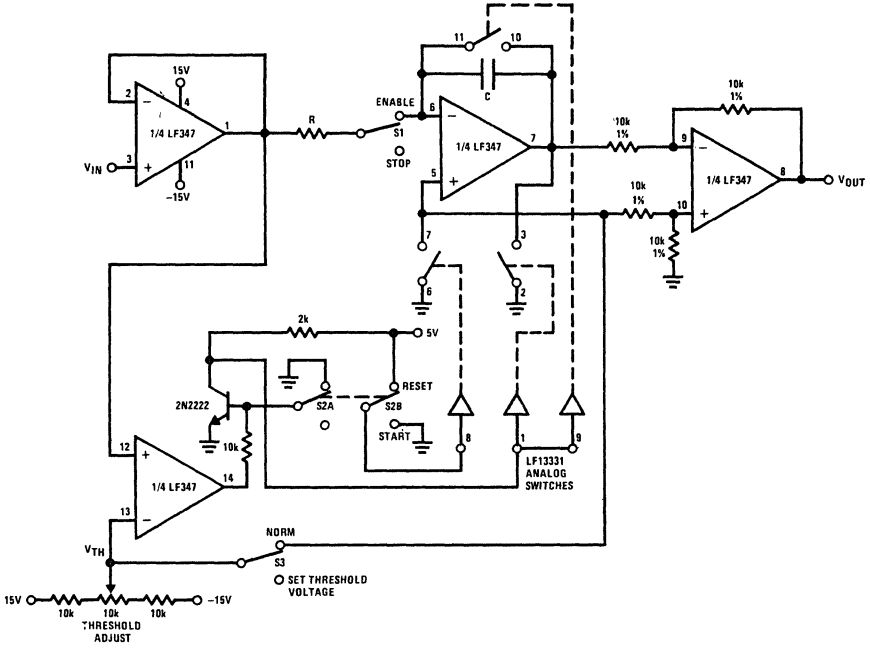


All resistors 1% tolerance

A1	A2	A3	V_O ATTENUATION
0	0	0	0
0	0	1	−1 dB
0	1	0	−2 dB
0	1	1	−3 dB
1	0	0	−4 dB
1	0	1	−5 dB
1	1	0	−6 dB
1	1	1	−7 dB

- Accuracy of better than 0.4% with standard 1% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



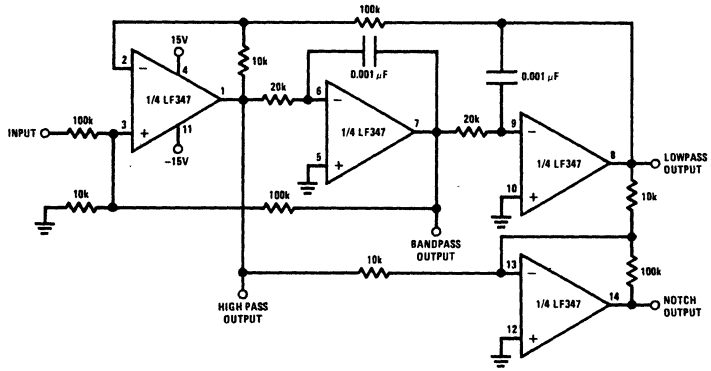
- V_{OUT} starts from zero and is equal.to the integral of the input voltage with respect to the threshold voltage:

$$V_{OUT} = \frac{1}{RC}\int_0^t (V_{IN} - V_{TH})dt$$

- Output starts when $V_{IN} \geq V_{TH}$
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

Typical Applications (Continued)

Universal State Variable Filter



For circuit shown:
f_o = 3 kHz, f_{NOTCH} = 9.5 kHz
Q = 3.4
Passband gain:
Highpass — 0.1
Bandpass — 1
Lowpass — 1
Notch — 10

- $f_o \times Q \leq 200$ kHz
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM348 data sheet for design equations

HARRIS

Operational Amplifiers/Buffers
LF353 Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

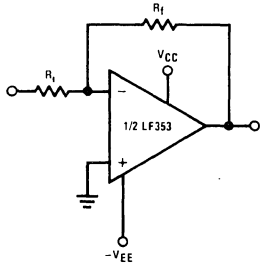
These devices are low cost, high speed, dual JFET input operational amplifiers. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

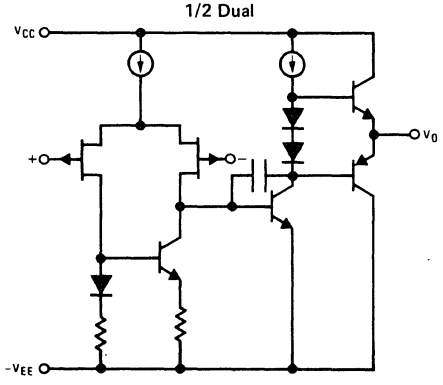
Features

- Typical offset voltage — 2 mV
- Low input bias current — 50 pA
- Low input noise voltage — 16 nV/√Hz
- Low input noise current — 0.01 pA/√Hz
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 3.6 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to .1% — 2 μs

Typical Connection



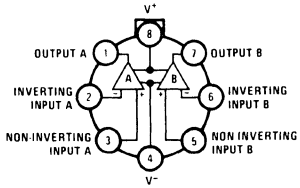
Simplified Schematic



Connection Diagrams

Section 11 for Packaging

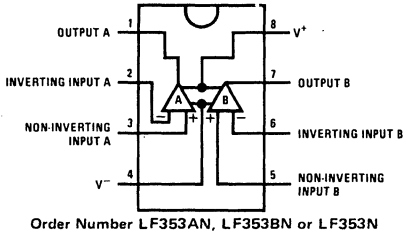
LF353H Metal Can Package (Top View)



Order Number LF353AH or LF353BH

Section 11 for Packaging

LF353N Dual-In-Line Package (Top View)



Order Number LF353AN, LF353BN or LF353N

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Operating Temperature Range	0°C to +70°C
T_j(MAX)	115°C
Differential Input Voltage	±30V
Input Voltage Range (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF353A			LF353B			LF353			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		1	2		3	5		5	10	mV
		Over Temperature			4			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10	20		10	30		10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 4, 5)		25	100		25	100		25	100	pA
		$T_j \leq$ 70°C			2			4			4	nA
I_B	Input Bias Current	T_j = 25°C, (Notes 4, 5)		50			50	200		50	200	pA
		$T_j \leq$ 70°C			4			8			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C	50	100		50	100		25	100		V/mV
		V_O = ±10V, R_L = 10kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15		±11	+15		±11	+15		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	80	100		80	100		70	100		dB
I_S	Supply Current			3.6	5.6		3.6	5.6		3.6	6.5	mA

AC Electrical Characteristics (Note 4)

SYMBOL	PARAMETER	CONDITIONS	LF353A			LF353B			LF353			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1 Hz–20 kHz (Input Referred)		−120			−120			120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C	10	13			13			13		V/µs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C	3	4			4			4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		16			16			16		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01			0.01			0.01		pA/$\sqrt{Hz}$

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of 160°C/W junction to ambient for the N package, and 150°C/W junction to ambient for the H package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: The power dissipation limit, however, cannot be exceeded.

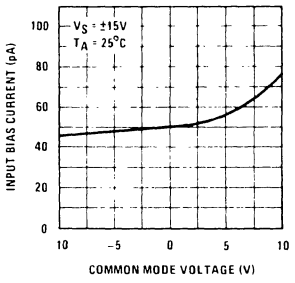
Note 4: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

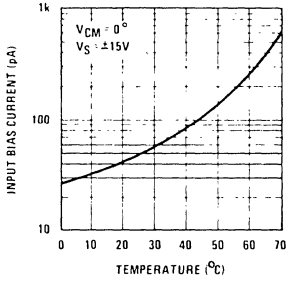
Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

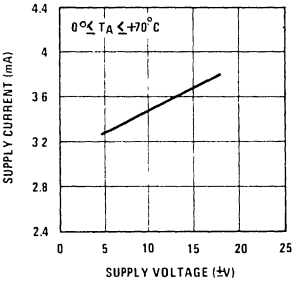
Input Bias Current



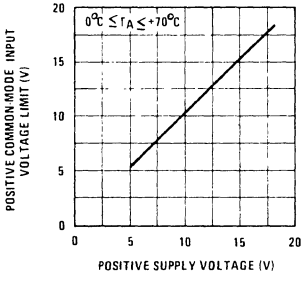
Input Bias Current



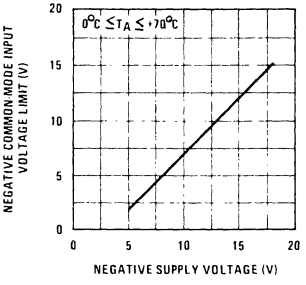
Supply Current



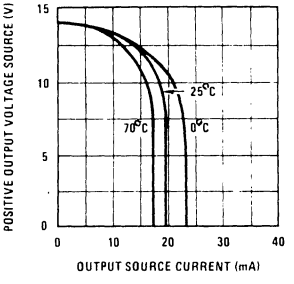
Positive Common-Mode Input Voltage Limit



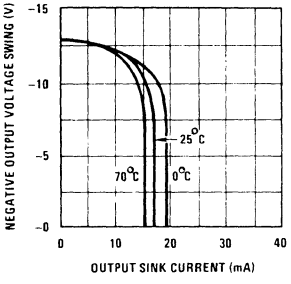
Negative Common-Mode Input Voltage Limit



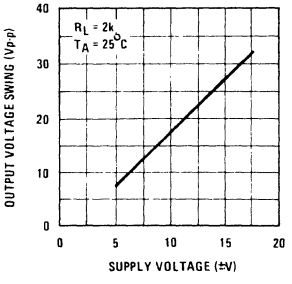
Positive Current Limit



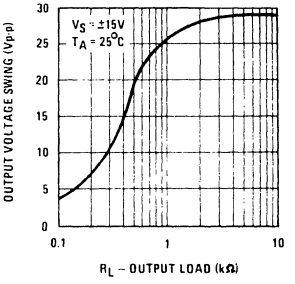
Negative Current Limit



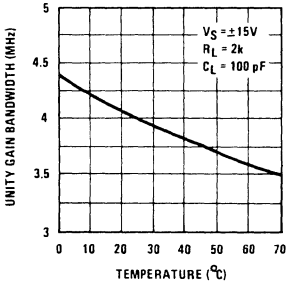
Voltage Swing



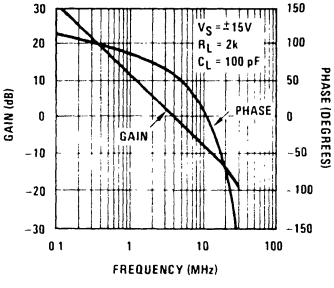
Output Voltage Swing



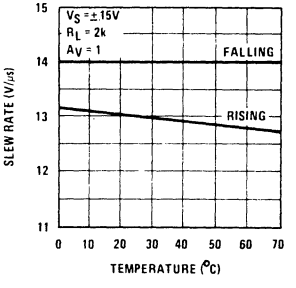
Gain Bandwidth



Bode Plot

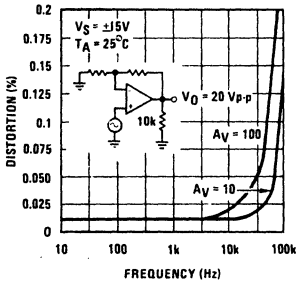


Slew Rate

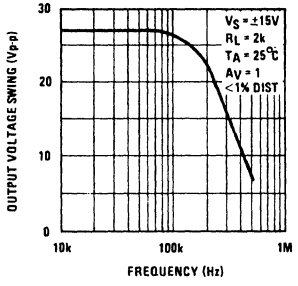


Typical Performance Characteristics (Continued)

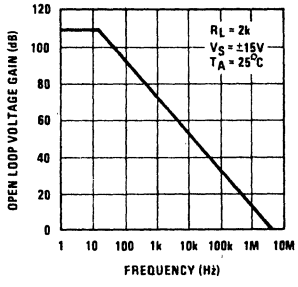
Distortion vs Frequency



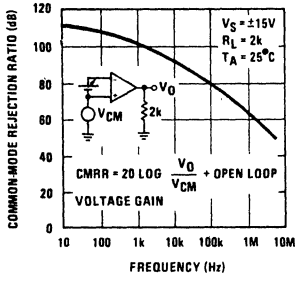
Undistorted Output Voltage Swing



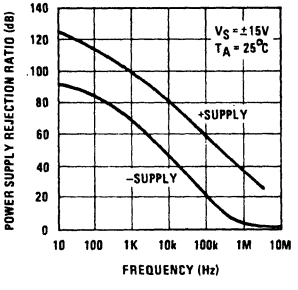
Open Loop Frequency Response



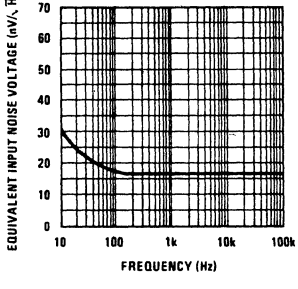
Common-Mode Rejection Ratio



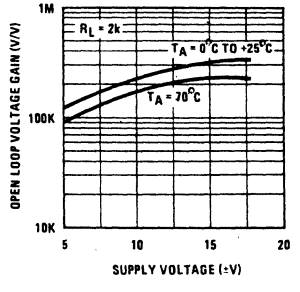
Power Supply Rejection Ratio



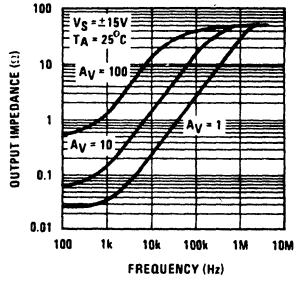
Equivalent Input Noise Voltage



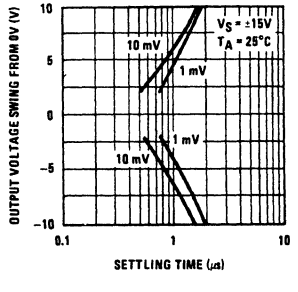
Open Loop Voltage Gain (V/V)



Output Impedance

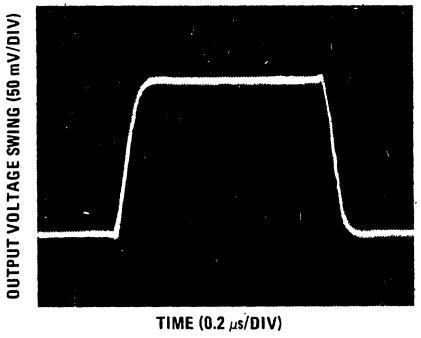


Inverter Settling Time

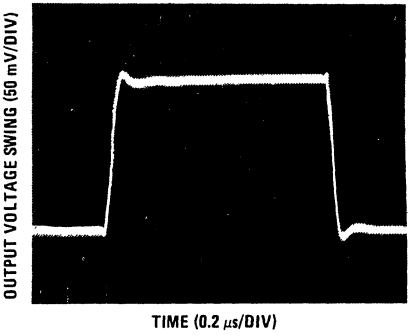


Pulse Response

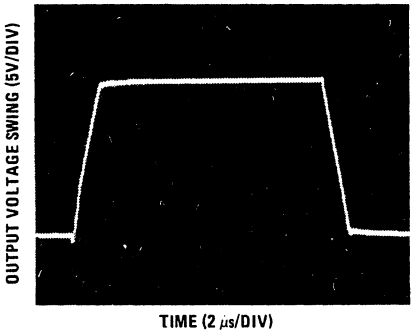
Small Signal Inverting



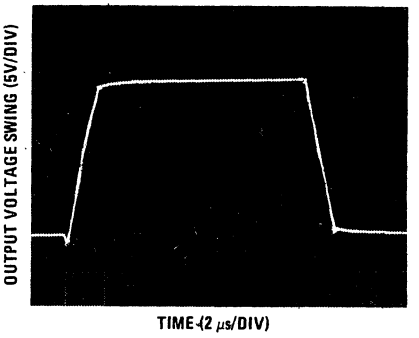
Small Signal Non-Inverting



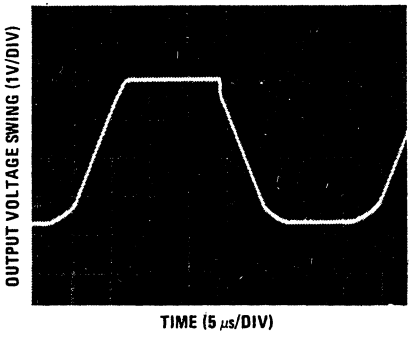
Large Signal Inverting



Large Signal Non-Inverting



Current Limit ($R_L = 100\Omega$)



Application Hints

These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a

Application Hints (Continued)

high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur

The amplifier is biased by a zener reference which allows normal circuit operation on ±4V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

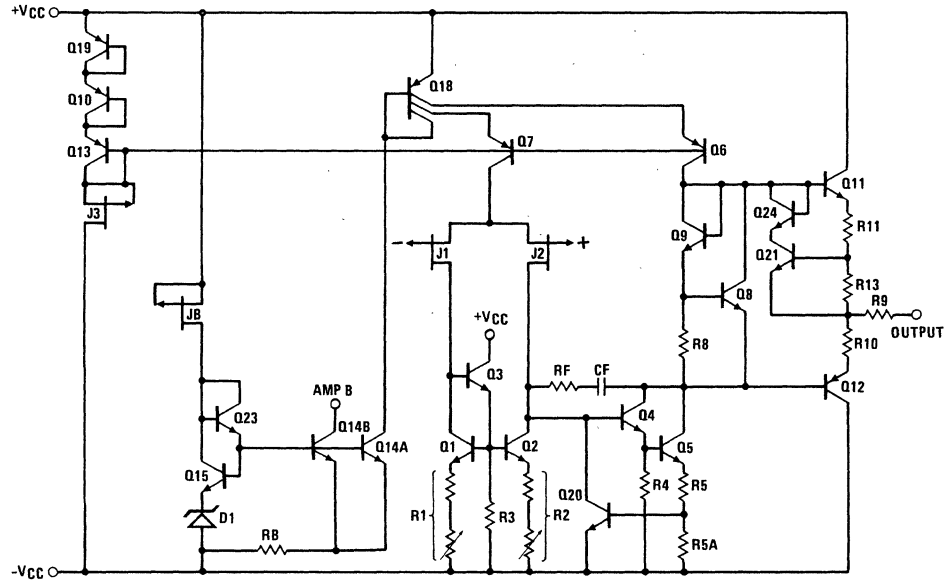
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

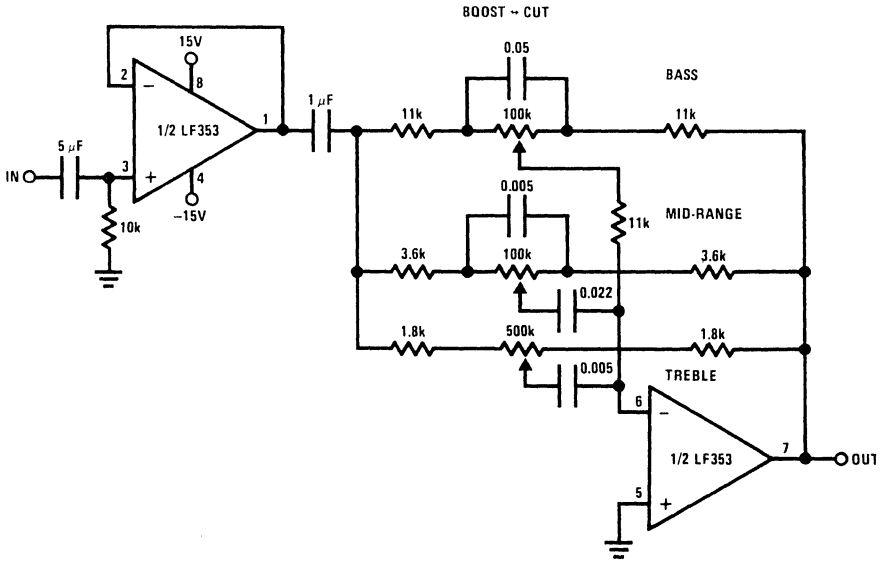
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

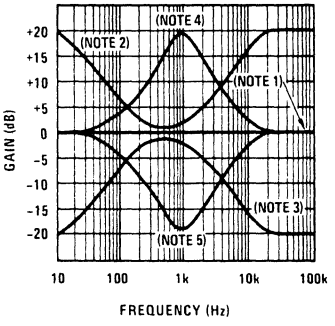
Detailed Schematic



Typical Applications

Three-Band Active Tone Control



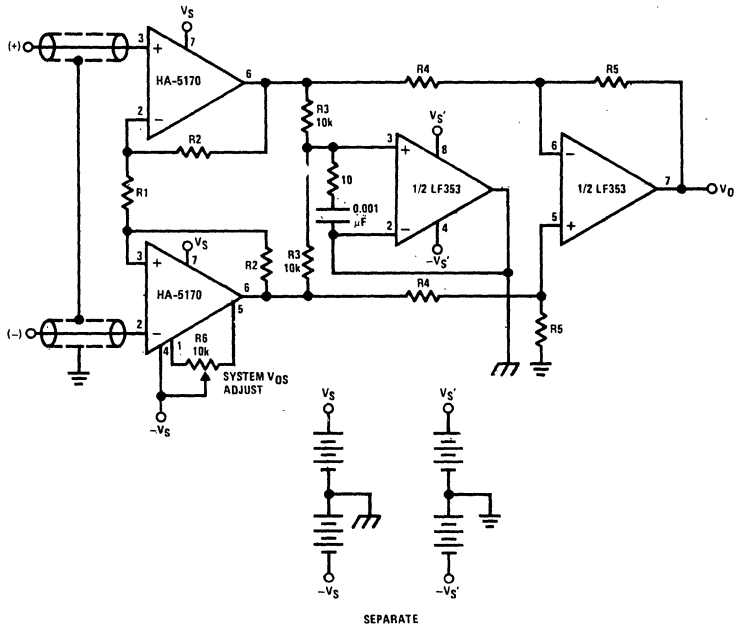


Note 1: All controls flat.
Note 2: Bass and treble boost, mid flat.
Note 3: Bass and treble cut, mid flat.
Note 4: Mid boost, bass and treble flat.
Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier



$$A_V = \left(\frac{2R2}{R1} + 1\right) \frac{R5}{R4}$$

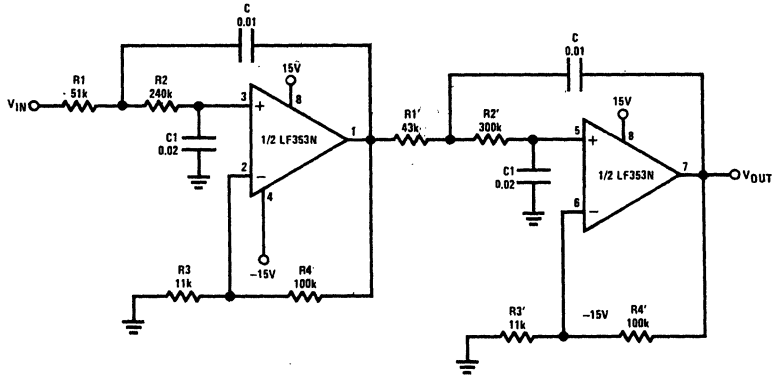
and are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With A_{V_T} = 1400, resistor matching ≈ 0.01%: CMRR ≈ 136 dB

- Very high input impedance
- Super high CMRR

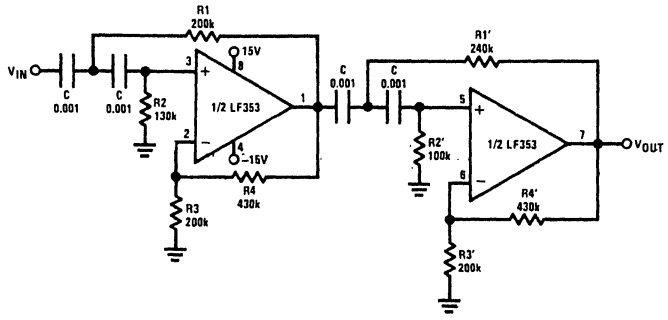
Fourth Order Low Pass Butterworth Filter



- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2CC1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'CC1}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3) (1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

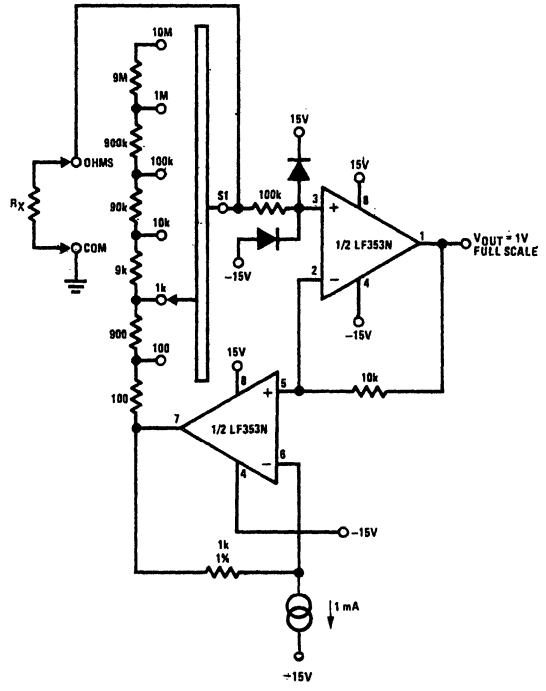
Typical Applications (Continued)

Fourth Order High Pass Butterworth Filter



- Corner frequency (f_c) = $\sqrt{\frac{1}{R1R2C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R1'R2'C^2}} \cdot \frac{1}{2\pi}$
- Passband gain (H_O) = (1 + R4/R3)(1 + R4'/R3')
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

Ohms to Volts Converter



$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

HARRIS

LM108/LM308 Operational Amplifiers

General Description

The LM108 series are precision operational amplifiers having specifications a factor of ten better than FET amplifiers over a -55°C to +125°C temperature range. It is possible to eliminate offset adjustments, in most cases, and obtain performance approaching chopper stabilized amplifiers.

The devices operate with supply voltages from ±3 to ±20V and have sufficient supply rejection to use unregulated supplies. They are fabricated using the Harris dielectric isolation process which coupled with our unique design, makes external compensation unnecessary. Outstanding characteristics include:

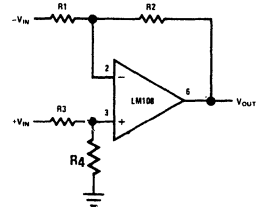
- Maximum input bias current of 6.0 nA over temperature
- Offset current less than 5.5 nA over temperature
- Supply current of only 1.0 mA
- Guaranteed drift characteristics
- External compensation components not required

The low current error of the LM108 series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from 10 MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μV/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

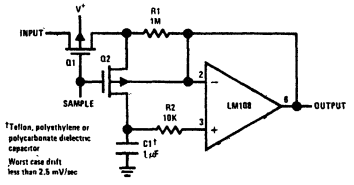
The LM108 is guaranteed from -55°C to +125°C, and the LM308 from 0°C to +70°C.

Typical Applications

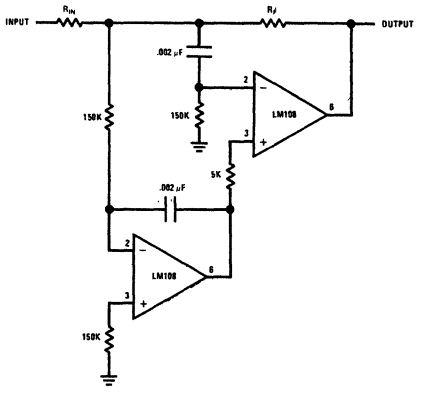
Standard Differential Amplifier



Sample and Hold



High Speed Amplifier with Low Drift and Low Input Current



Absolute Maximum Ratings

	LM108	LM308
Supply Voltage	±20V	±18V
Power Dissipation (Note 1)	500 mW	500 mW
Differential Input Current (Note 2)	±10 mA	±10 mA
Input Voltage (Note 3)	±15V	±15V
Output Short-Circuit Duration	Indefinite	Indefinite
Operating Temperature Range (LM108)	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics (Note 4)

PARAMETER	CONDITIONS	LM108			LM308			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_S = \pm 15V$, $T_A = 25°C$		0.7	2.0		2.0	7.5	mV
Input Offset Current			0.05	4.0		0.2	4.0	nA
Input Bias Current			0.8	4.0		1.5	7	nA
Input Resistance		10	30		10	30		MΩ
Supply Current			1.0	1.7		1.0	1.7	mA
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	50	300		25	300		V/mV
Input Offset Voltage	$V_S = \pm 15V$			3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage	$0°C \leq T_A \leq 70°C$ (LM308)		3.0	15		6.0	30	μV/°C
Input Offset Current	$-55°C \leq T_A \leq 125°C$ (LM108)			5.5			5.5	nA
Average Temperature Coefficient of Input Offset Current			0.04	0.06		0.04	0.06	nA/°C
Input Bias Current				6.0			10	nA
Supply Current			1.0	1.7				mA
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	25			15			V/mV
Output Voltage Swing	$R_L = 10\ k\Omega$	±10	±12		±10	±12		V
Input Voltage Range		±12			±12			V
Common-Mode Rejection Ratio		85	100		80	100		dB
Supply Voltage Rejection Ratio		80	96		80	96		dB

Note 1: The maximum junction temperature of the LM108 is 150°C and 85°C for the LM308. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, function to ambient.

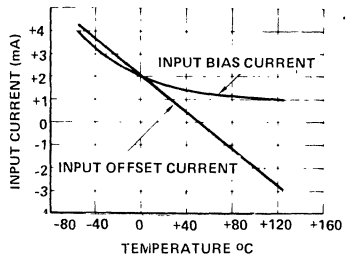
Note 2: If a differential input voltage in excess of the operating supply is applied between the inputs, excessive current will flow unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

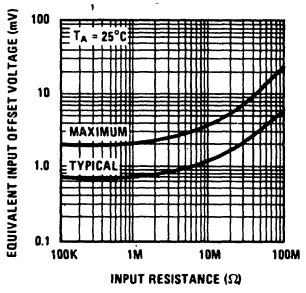
Note 4: The device operating supply voltage range is $\pm 3V \leq V_S \leq \pm 18V$.

Typical Performance Characteristics LM108

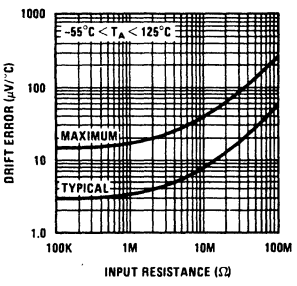
Input Currents



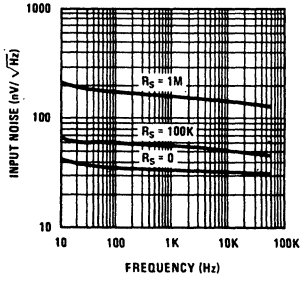
Offset Error



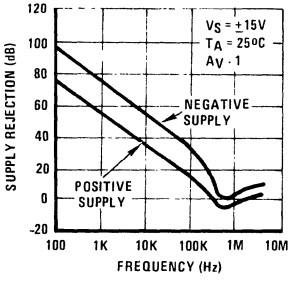
Drift Error



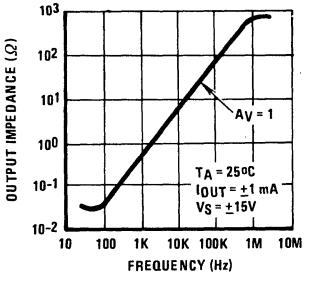
Input Noise Voltage



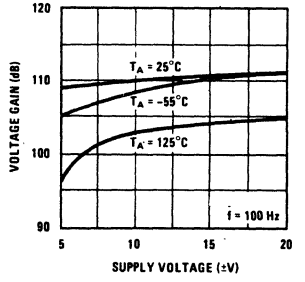
Power Supply Rejection



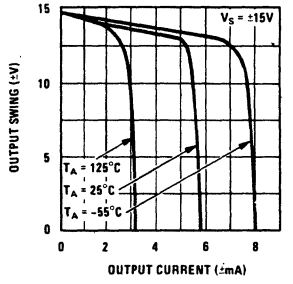
Closed Loop Output Impedance



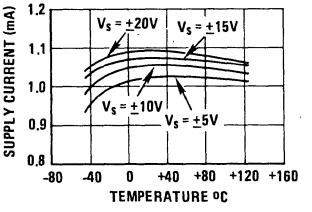
Voltage Gain



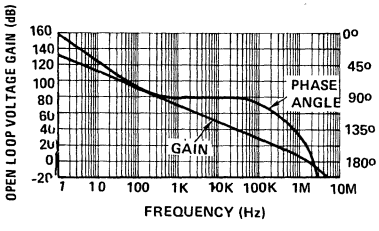
Output Swing



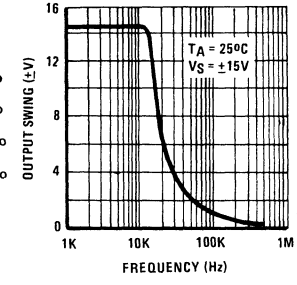
Power Supply Current Vs. Temperature and Supply Voltage



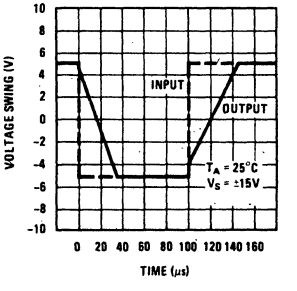
Open Loop Frequency Response



Large Signal Frequency Response

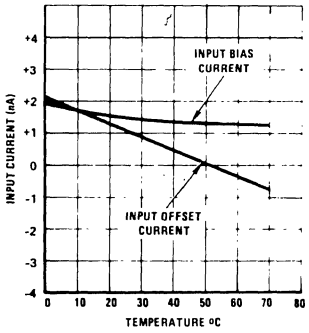


Voltage Follower Pulse Response

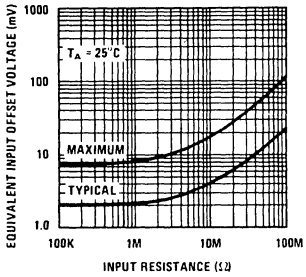


Typical Performance Characteristics LM308

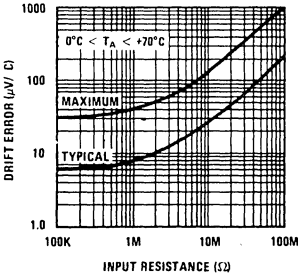
Input Currents



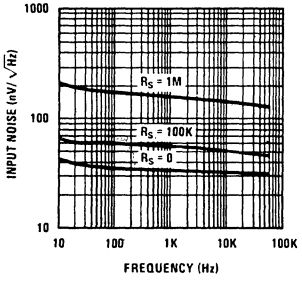
Offset Error



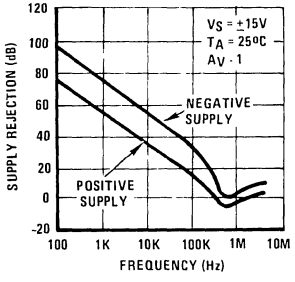
Drift Error



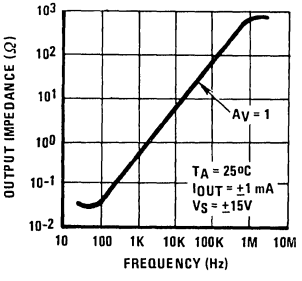
Input Noise Voltage



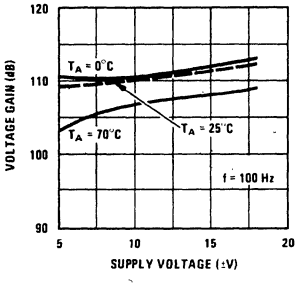
Power Supply Rejection



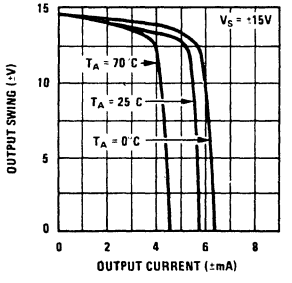
Closed Loop Output Impedance



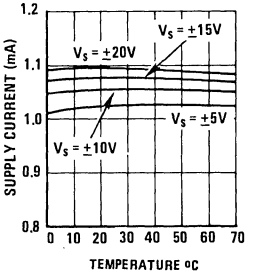
Voltage Gain



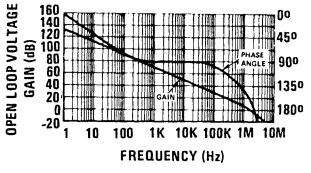
Output Swing



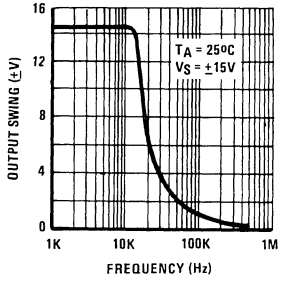
Power Supply Current Vs. Temperature and Supply Voltage



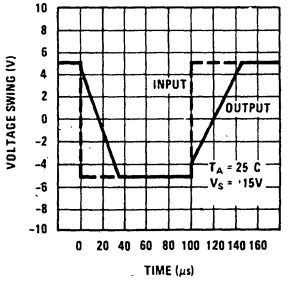
Open Loop Frequency Response



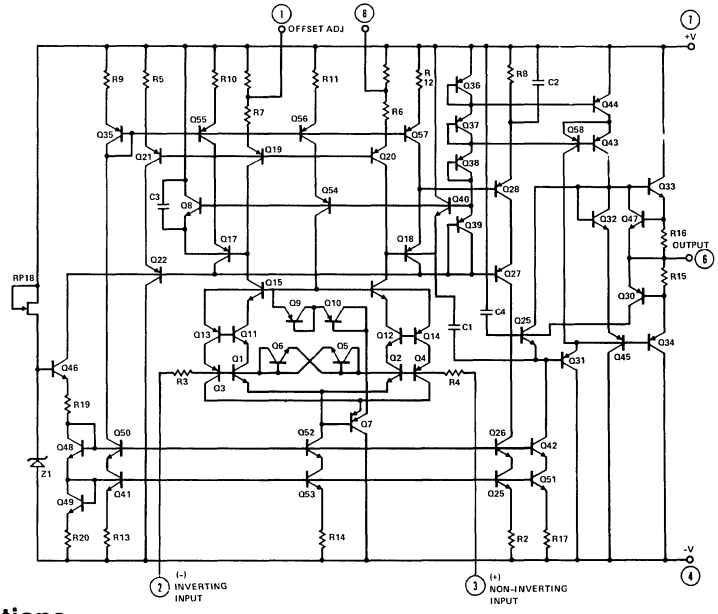
Large Signal Frequency Response



Voltage Follower Pulse Response

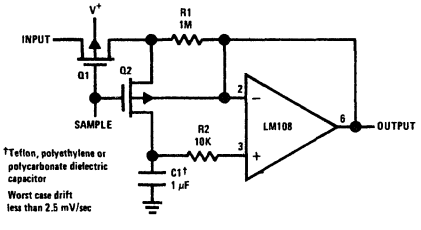


Schematic Diagram

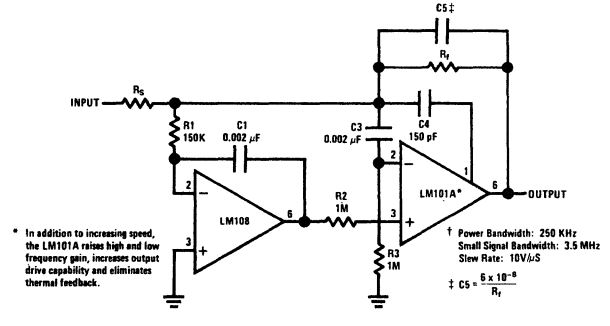


Typical Applications (Continued)

Sample and Hold

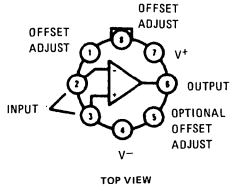


Fast† Summing Amplifier



Connection Diagrams Section 11 for Packaging

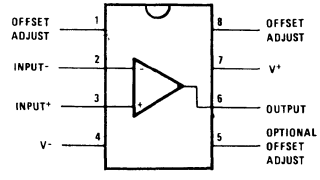
Metal Can Package



TOP VIEW

Order Number LM108H
LM308H

Dual-In-Line Package

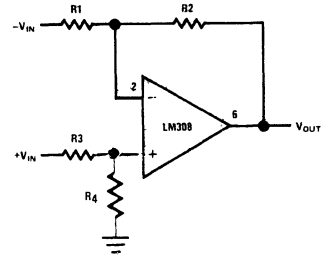


TOP VIEW

Order Number LM108J-8,
LM308J-8

Order Number LM308N

Standard Differential Amplifier



*Pin connections shown on schematic diagram are for TO-5 and Dual-In-Line Package

LM108A/LM308A Operational Amplifiers

General Description

The LM108A/308A series are precision operational amplifiers having specifications about a factor of ten better than FET amplifiers over their operating temperature range. In addition ro low input currents, these devices have extremely low offset voltage, making it possible to eliminate offset adjustments, in most cases, and obtain performance approaching chopper stabilized amplifiers.

The devices operate with supply voltages from ±3V to ±18V and have sufficient supply rejection to use unregulated supplies. They are fabricated using the Harris dielectric isolation process which coupled with our unique design makes external compensation unnecessary. Outstanding characteristics include:

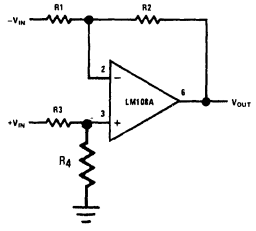
- Offset voltage guaranteed less than 0.25mV
- Maximum input bias current of 4.0 nA over temperature
- Offset current less than 4.0 nA over temperature
- Supply current of only 1 mA
- Guaranteed .6 μV/°C drift
- External compensation components not required

The low current error of the LM108A series makes possible many designs that are not practical with comventional amplifiers. In fact, it operated from 10MΩ source resistances, introducing less error than devices like the 709 with 10 kΩ sources. Integrators with drifts less than 500 μ V/sec and analog time delays in excess of one hour can be made using capacitors no larger than 1 μF.

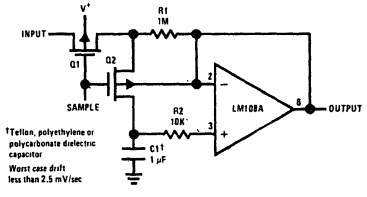
The LM308A devices have slightly relaced specifications and performance guaranteed over a 0°C to 70°C temperature range.

Typical Characteristics

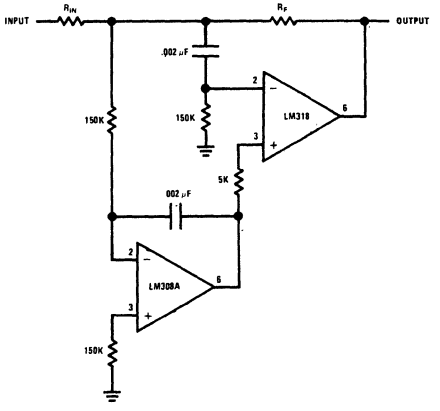
Standard Differential Amplifier



Sample and Hold



High Speed Amplifier with Low Drift and Low Input Current



LM108A
Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range LM108A	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$V_S = \pm 15V$, $T_A = 25°C$		.01	.025	mV
Input Offset Current			0.05	2.0	nA
Input Bias Current			0.8	2.0	nA
Input Resistance		10	30		MΩ
Supply Current			1.0	1.7	mA
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	120	140		dB
Input Offset Voltage	$V_S = \pm 15V$			.06	mV
Average Temperature Coefficient of Input Offset Voltage	$-55°C \leq T_A \leq +125°C$		.4	.6	μV/°C
Input Offset Current				4.0	nA
Average Temperature Coefficient of Input Offset Current				.04	nA/°C
Input Bias Current				4.0	nA
Supply Current			1.0	1.7	mA
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	120			dB
Output Voltage Swing	$R_L = 10\ k\Omega$	±10	± 12		V
Input Voltage Range		±12			V
Common Mode Rejection Ratio		106	120		dB
Supply Voltage Rejection Ratio		100	130		dB

Note 1: The maximum junction temperature of the LM108A is 150°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
Note 2: If a differential input voltage in excess of the oerating supply is applied between the inputs, excessive current will flow unless some limiting resistance is used.
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 4: The device operating supply voltage range is $\pm 3V \leq Vs \leq \pm 18V$.

LM308A

Absolute Maximum Ratings

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$V_S = \pm 15V$, $T_A = 25^oC$		.01	.025	mV
Input Offset Current			0.2	2.0	nA
Input Bias Current			1.5	2.0	nA
Input Resistance			30		MΩ
Supply Current			1.0	1.7	mA
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 10\ k\Omega$	120	140		dB
Input Offset Voltage LM308A	$V_S = \pm 15V$ $0^oC \leq T_A \leq +70^oC$			.06	mV
Average Temperature Coefficient of Input Offset Voltage LM308A			.4	.6	μV/°C
Supply Current			1.0	1.7	mA
Input Offset Current				4.0	nA
Average Temperature Coefficient of Input Offset Current				0.04	nA/°C
Input Bias Current				4	nA
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$ $R_L \geq 10\ k\Omega$	120			dB V
Output Voltage Swing	$R_L = 10\ k\Omega$	±10	±12		V
Input Voltage Range		±12			dB
Common-Mode Rejection Ratio		106	120		
Supply Voltage Rejection Ratio		100	130		dB

Note 1: The maximum junction termperature of the LM308A, LM308-1, and LM308-2 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: If a differential input voltage in excess of the operating supply is applied between the inputs, excessive current will flow unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: The device operating supply voltage range is $\pm 3V \leq Vs \leq \pm 18V$.

Application Hints

A very low drift amplifier poses some uncommon application and testing problems. Many sources of error can cause the apparent circuit drift to be much higher than would be predicted.

Thermocouple effects caused by temperature gradient across dissimilar metals are perhaps the worst offenders. Only a few degrees gradient can cause hundreds of microvolts of error. The two places this shows up, generally, are the package-to printed circuit board interface and temperature gradients across resistors. Keeping package leads short and the two input leads close together help greatly.

Resistor choice as well as physical placement is important for minimizing thermocouple effects. Carbon, oxide film and some metal film resistors can cause large thermocouple errors. Wirewound resistors of evenohm or manganin are best since they only generate about 2 $\mu V/^{\circ}C$ referenced to copper. Of course, keeping the resistor ends at the same temperature is important. Generally, shielding a low drift stage electrically and thermally will yield good results.

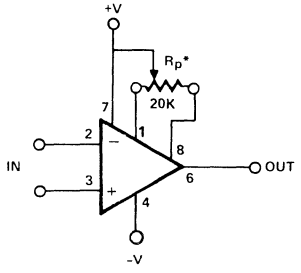
Resistors can cause other errors besides gradient generated voltages. If the gain setting resistors do not track with temperature a gain error will result. For example a gain of 1000 amplifier with a constant 10 mV input will have a 10V output. If the resistors mistrack by 0.5% over the operating temperature range, the error at the output is 50 mV. Referred to input, this is a 50 μV error. All of the gain fixing resistor should be the same material.

Offset balancing the LM308A is not a problem since there is an easy offset adjustment incorporated into the circuit. This adjustment can be accomplished by simply using the circuit given below.

In addition to the suggested offset nulling method, this adjustment can also be done at the input by employing one of the three commonly used circuits shown.

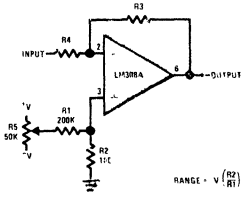
Testing low drift amplifiers is also difficult. Standard drift testing technique such as heating the device in an oven and having the leads available through a connector, thermoprobe, or the soldering iron method – do not work. Thermal gradients cause much greater errors than the amplifier drift. Coupling microvolt signal through connectors is especially bad since the temperature difference across the connector can be 50°C or more. The device under test along with the gain setting resistor should be isothermal. The following circuit will yield good results if well constructed.

Suggested Connections for Offset Nulling

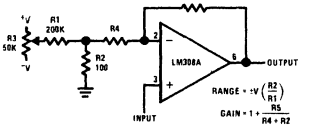


* Although R_P is shown equal to 20k, other values such as 50k, 100k, and 1M may be used. Range of adjustment is approximately ±2.5mV. $V_{OS}TC$ of the amplifier is not compromised.

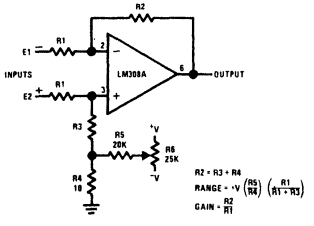
For Inverting Amplifiers



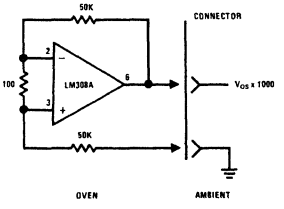
For Non-Inverting Amplifiers



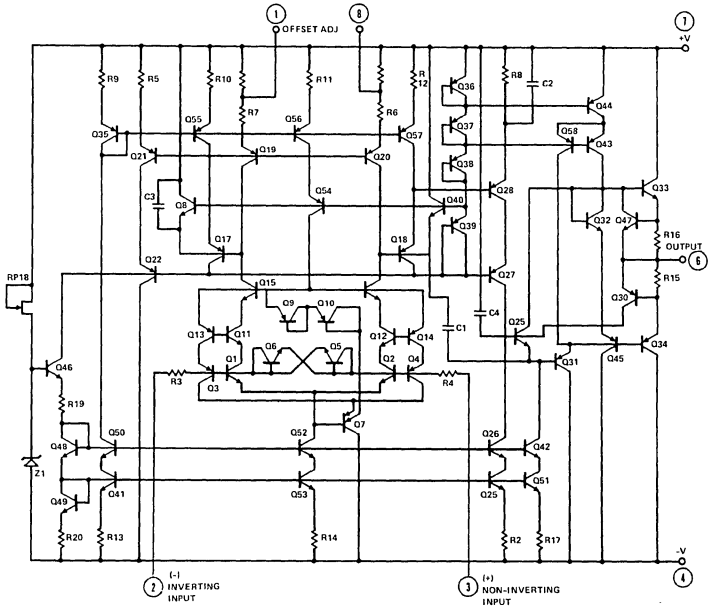
Offset Adjustment for Differential Amplifiers



Drift Measurement Circuit



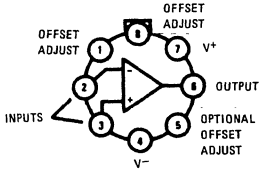
Schematic Diagram*



*Pin connections shown on schematic diagram refer to TO-5 and Dual-In-Line Package

Connection Diagrams **Section 11 for Packaging**

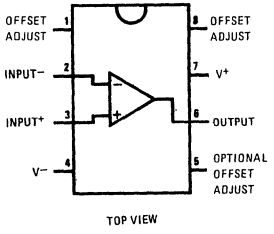
Metal Can Package



TOP VIEW

Order Number LM108AH,
LM308AH

Dual-In-Line-Package



TOP VIEW

Order Number LM108AJ-8
LM308AJ-8

Order Number LM308AN

HARRIS

LM118/LM318 Operational Amplifiers

General Description

The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

Fabricated using the Harris process which, coupled with our unique design, affords a more predictable dynamic performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. Howerver, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 300ns if required.

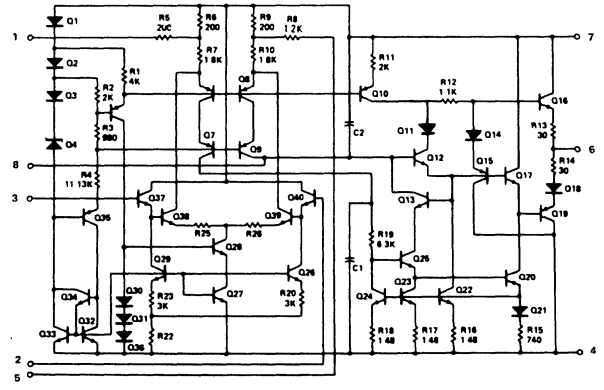
The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

The LM318 is identical to the LM118 except that the LM318 has its performance specified over a 0°C to +70°C temperature range.

Features

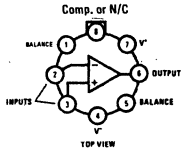
- 15 MHz small signal bandwidth
- Guaranteed 50V/ μ s slew rate
- Maximum bias current of 250 nA
- Operates from supplies of $\pm$5V to $\pm$20V
- Internal frequency compensation
- Pin compatible with general purpose op amps

Schematic and Connection Diagrams



Section 11 for Packaging

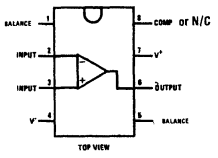
Metal Can Package*



*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Order Number LM118H,
or LM318H

Dual-In-Line Package



Order Number LM118J-8,
or LM318J-8

Order Number LM318N

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Diffentntial Input Current (Note 2)	±15V
Output Short-Circuit Duration (Note 4)	Indefinite
Operating Temperature Range	
LM118	-55°C to +125°C
LM318	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (Note 5)

PARAMETER	CONDITIONS	LM118			LM318			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	Unless Otherwise Specified: $V_S = \pm 15V$, $T_A = +25°C$		2	4		5	10	mV
Input Offset Current			6	50		30	200	nA
Input Bias Current			120	250		150	500	nA
Input Resistance		1	3		0.5	3		M
Supply Current			5	8		5	10	mA
Large Signal Voltage Gain (Note 6)	$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	12	15		10	15		V/mV
Slew Rate	$A_V = 1$	50	70		50	70		V/μs
Small Signal Bandwidth			15			15		MHz
Input Offset Voltage	Unless Otherwise Specified: $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM118), $0°C \leq T_A \leq +70°C$ (LM318)			6			15	mV
Input Offset Current				100			300	nA
Input Bias Current				500			750	nA
Supply Current	$T_A = +125°C$		4.5	6		4.5	6	mA
Large Signal Voltage Gain (Note 6)	$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	8			8			V/mV
Output Voltage Swing	$R_L = 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range								V
Common-Mode Rejection Ratio		80	100		70	100		dB
Supply Voltage Rejection Ratio		70	80		65	80		dB

Note 1: The maximum junction temperature of the LM118 is 150°C and the LM318 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: If a differential input voltage in excess of the operating supply voltage is applied between the input, excessive current will flow unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

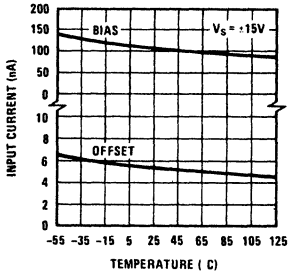
Note 4: LM118/LM318 can withstand continuous shorts to ground or either supply rail. However, good practice is to avoid exceeding the maximum junction temperature rating of the device, which could cause the circuit to be damaged.

Note 5: These specifications apply for $\pm 15V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$, (LM118), and $0°C \leq T_A \leq +70°C$ (LM318). Also, power supplies must be bypassed with 0.1 μF disc capacitors.

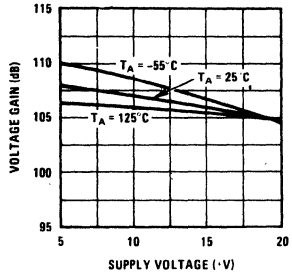
Note 6: In practically all applications the specified open loop voltage gain will be sufficient. In unusual applications requiring minimized loop gain errors, external adjustments may be necessary.

Typical Performance Characteristics LM118

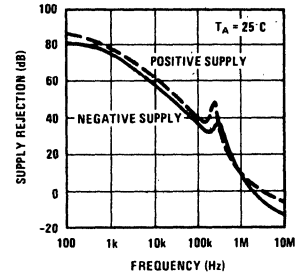
Input Current



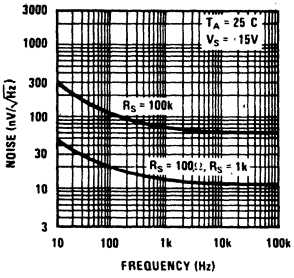
Voltage Gain



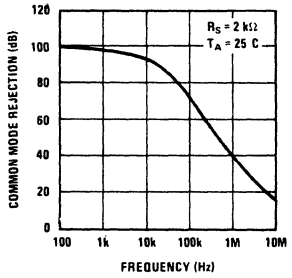
Power Supply Rejection



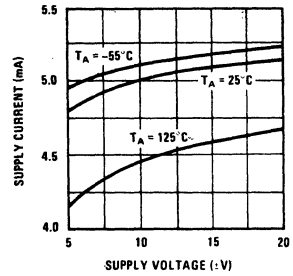
Input Noise Voltage



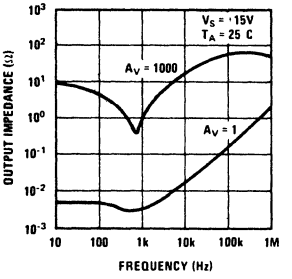
Common Mode Rejection



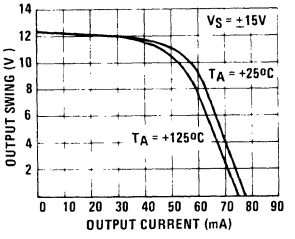
Supply Current



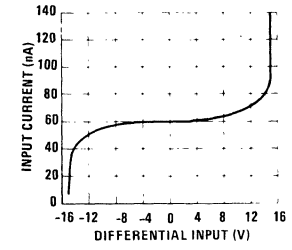
Closed Loop Output Impedance



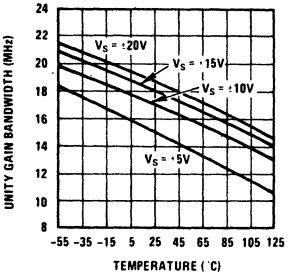
Output Current



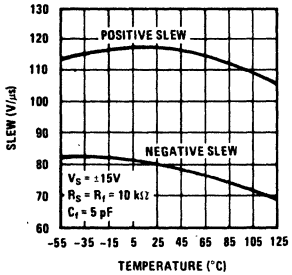
Input Current



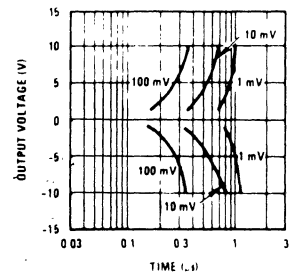
Unity Gain Bandwidth



Voltage Follower Slew Rate

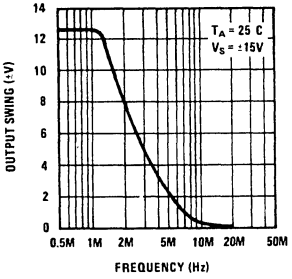


Inverter Settling Time

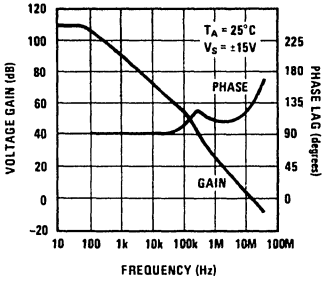


Typical Performance Characteristics LM118, (Continued)

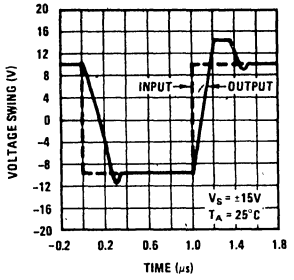
Large Signal Frequency Response



Open Loop Frequency Response

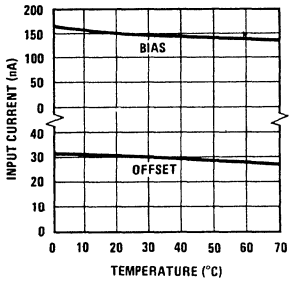


Voltage Follower Pulse Response

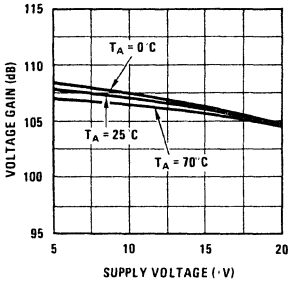


Typical Performance Characteristics LM318

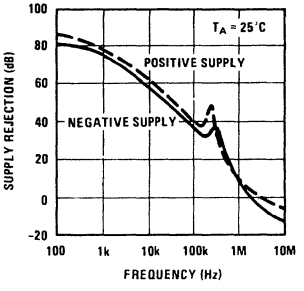
Input Current



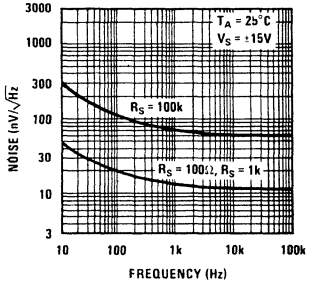
Voltage Gain



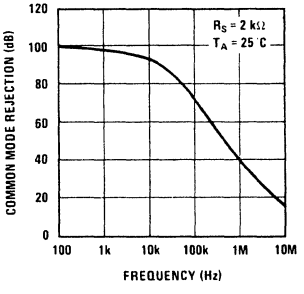
Power Supply Rejection



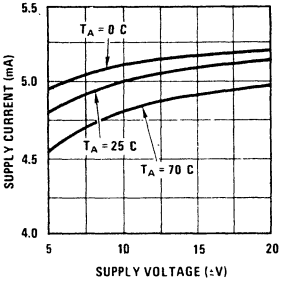
Input Noise Voltage



Common Mode Rejection

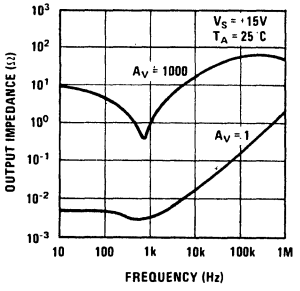


Supply Current

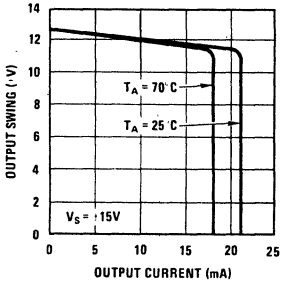


Typical Performance Characteristics LM318 (Continued)

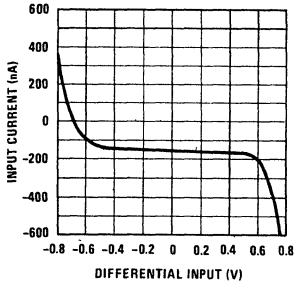
Closed Loop Output Impedance



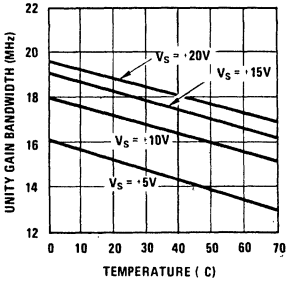
Current Limiting



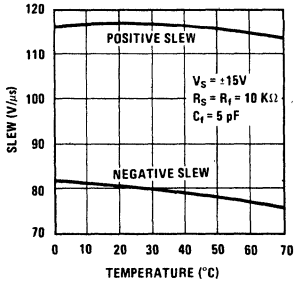
Input Current



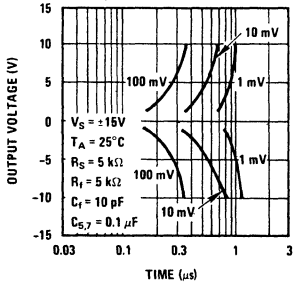
Unit Gain Bandwidth



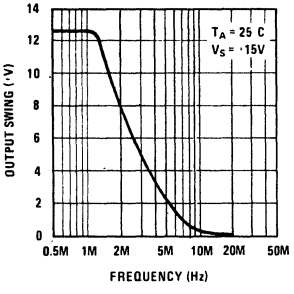
Voltage Follower Slew Rate



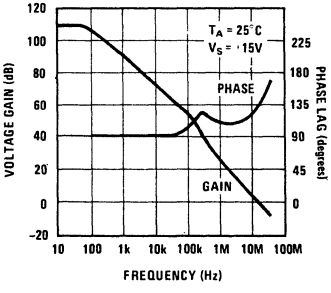
Inverter Settling Time



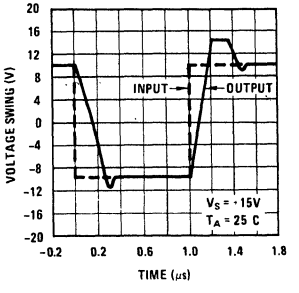
Large Signal Frequency Response



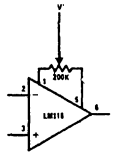
Open Loop Frequency Response



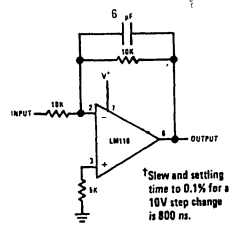
Voltage Follower Pulse Response



Auxiliary Circuits

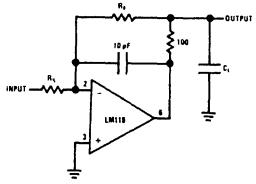


Offset Balancing

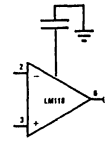


†Slew and settling time to 0.1% for a 10V step change is 800 ns.

Compensation for Minimum Settling† Time

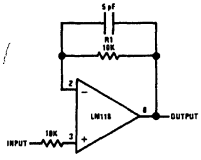


Isolating Large Capacitive Loads

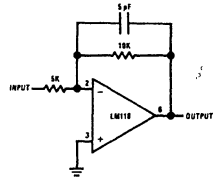


Overcompensation

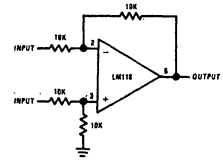
Typical Applications



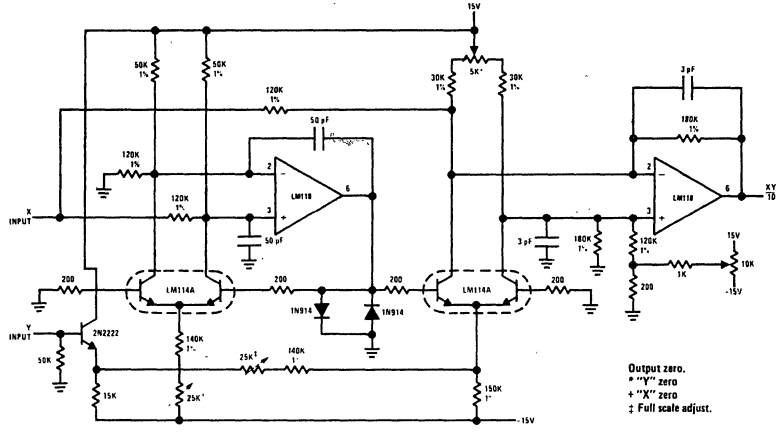
Fast Voltage Follower



Fast Summing Amplifier



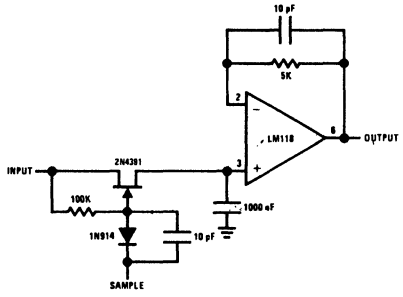
Differential Amplifier



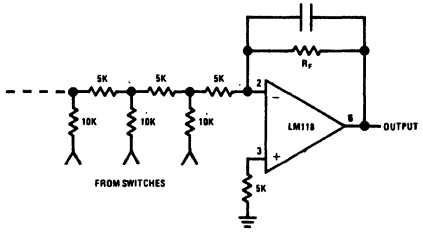
Output zero.
* "Y" zero
+ "X" zero
‡ Full scale adjust.

Four Quadrant Multiplier

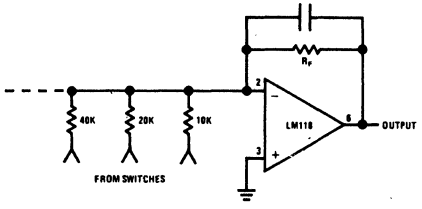
Typical Applications (Continued)



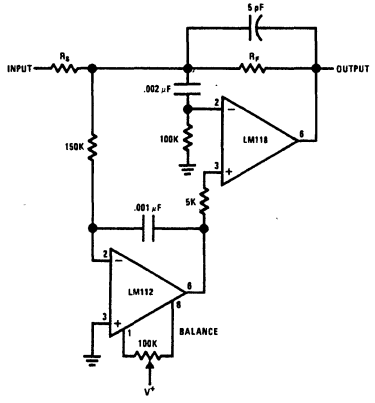
Fast Sample and Hold



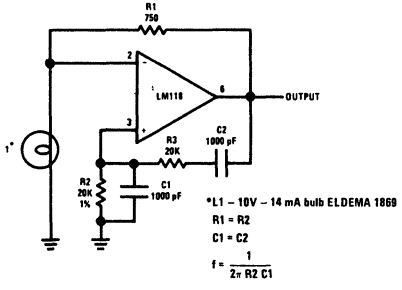
D/A Converter Using Ladder Network



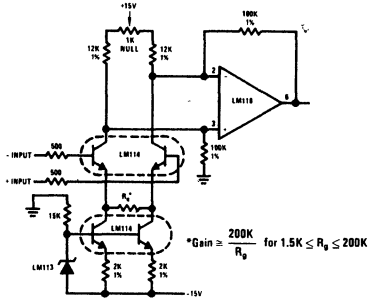
D/A Converter Using Binary Weighted Network



Fast Summing Amplifier
with Low Input Current



Wein Bridge Sine Wave Oscillator



Instrumentation Amplifier

LM118A/LM318A Operational Amplifiers

General Description

The LM118A series are precision high speed operational amplifiers designed for applications requiring predictable wide bandwidth and high slew rate. They feature similar performance criteria to the LM118 while offering lower power requirements.

The LM118A series provides internal unity gain frequency compensation. This coupled with the Harris DI process and a unique design, simplifies LM118's application since no external compensation components are necessary. However, compensation may be added for applications where greater stability is required. Further, a single capacitor can be added to reduce the 0.1% settling time to under 300 ns if required.

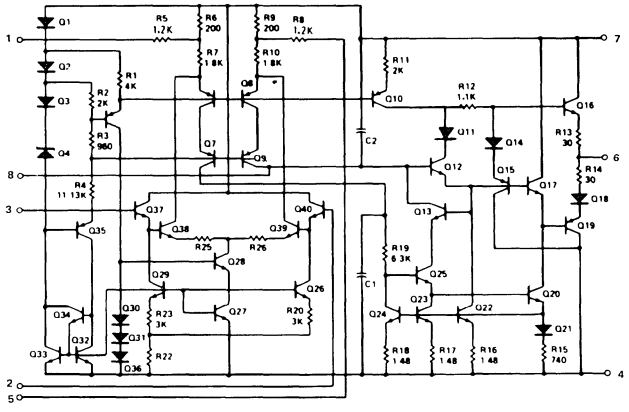
LM118A's high speed, fast settling time, and ease of use is ideally suited for A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices offer a superior predictable AC performance to industry standards such as LM709.

LM318A is identical to the LM118A except that the LM318A has its performance specified over a 0°C to +70°C temperature range.

Features

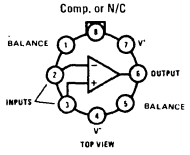
- 15 MHz small signal bandwidth
- Guaranteed 50V/μs slew rate
- Maximum bias current of 250 nA
- Operates from supplies of $\pm$5V to $\pm$20V
- Internal frequency compensation
- Pin compatible with general purpose op amps
- Need better process term

Schematic and Connection Diagrams



Section 11 for Packaging

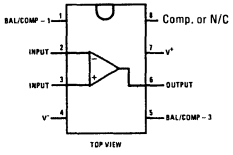
Metal Can Package*



*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Order Number LM118H
or LM318H

Dual-In-Line Package



Order Number LM118J-8
Or LM318J-8

Order Number 318N

Absolute Maximum Ratings

Supply Voltage	±20V
Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration (Note 4)	Indefinite
Operating Temperature Range	
LM118A	-55°C to +125°C
LM318A	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

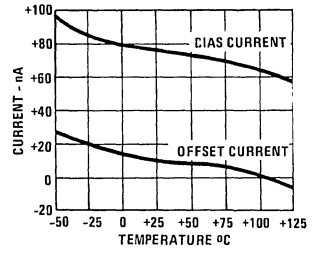
Electrical Characteristics (Note 5)

PARAMETER	CONDITIONS	LM118A			LM318A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	Unless Otherwise Specified. $V_S = \pm 15V$, $T_A = +25°C$		1	3		5	8	mV
Input Offset Current			10	25		20	50	nA
Input Bias Current			100	200		125	250	nA
Input Resistance		50	100		40	100		MΩ
Supply Current			4	6		4	6	mA
Large Signal Voltage Gain (Note 6)	$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	15	20		12	15		V/mV
Slew Rate	$A_V = 1$	65	70		65	70		V/μs
Small Signal Bandwidth			12			12		MHz
Input Offset Voltage	Unless Otherwise Specified. $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM118), $0°C \leq T_A \leq +70°C$ (LM318)			5			12	mV
Input Offset Current				50			100	nA
Input Bias Current				400			500	nA
Supply Current	$T_A = +125°C$		4	6		4	6	mA
Large Signal Voltage Gain (Note 6)	$V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	10			10			V/mV
Output Voltage Swing	$R_L = 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range		±10			±10			V
Common-Mode Rejection Ratio		80	90		74	90		dB
Supply Voltage Rejection Ratio		80	90		74	90		dB

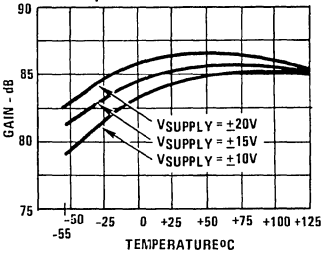
Note 1: The maximum junction temperature of the LM118A is 150°C, and the LM318A is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide,, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
Note 2: If a differential input voltage in excess of the operating supply voltage is applied between the inputs, excessive current will flow unless some limiting resistance is used.
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 4: LM118A/LM318A can withstand continuous shorts to the ground or either supply rail. However, good practice is to avoid exceeding the maximum junction temperature rating of the device, which could cause the circuit to be damaged.
Note 5: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55°C \leq T_A \leq +125°C$, (LM118A) and $0°C \leq T_A \leq +70°C$ (LM318A). Also, power supplies must be bypassed with 0.1μF disc capacitors.
Note 6: In practically all applications the specified open loop voltage gain will be sufficient. In unusual applications requiring minimized loop gain errors, external adjustments may be necessary.

Typical Performance Characteristics LM118A

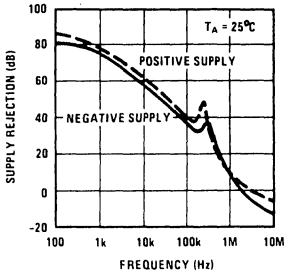
Input Bias and Offset Current vs Temperature



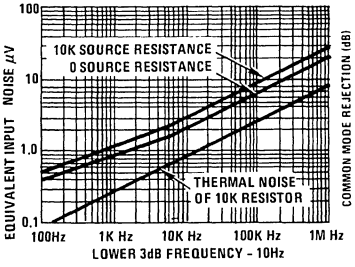
Open Loop Voltage Gain vs Temperature



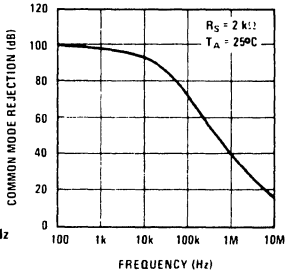
Power Supply Rejection



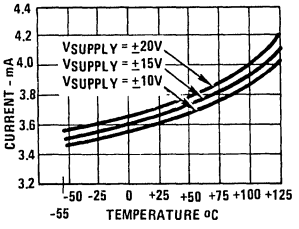
Equivalent Input Noise vs Bandwidth



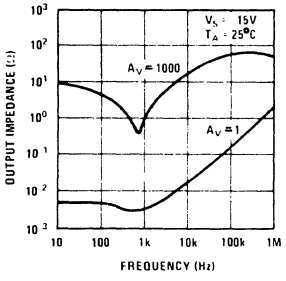
Common Mode Rejection



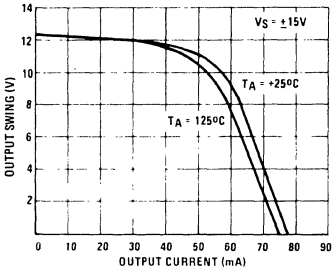
Power Supply Current vs Temperature



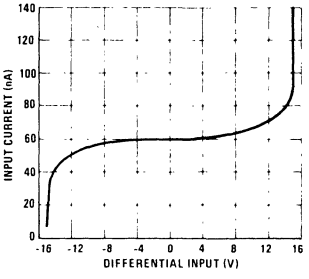
Closed Loop Output Impedance



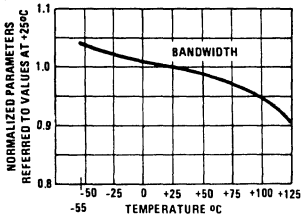
Output Current



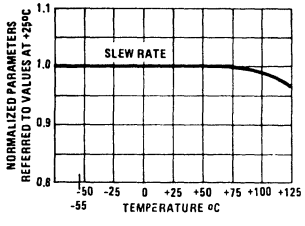
Input Current



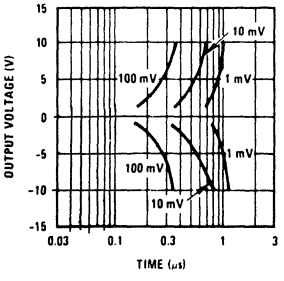
Normalized AC Parameters vs Temperature



Normalized AC Parameters vs Temperature



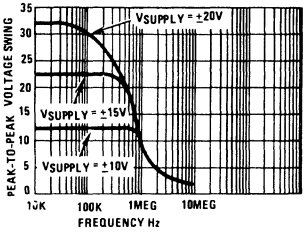
Inverter Settling Time



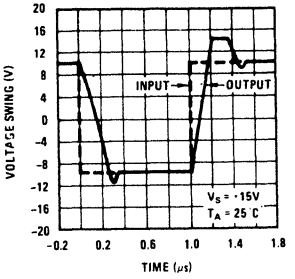
2

Typical Performance Characteristics LM318A (Continued)

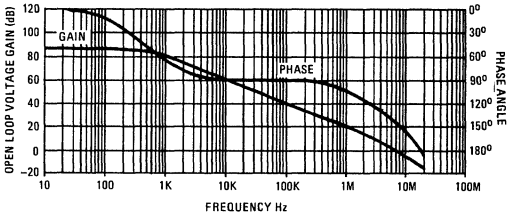
Output Voltage Swing vs Frequency at +25°C



Voltage Follower Pulse Response

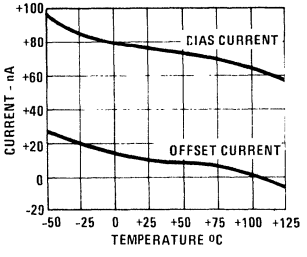


Open Loop Frequency and Phase Response

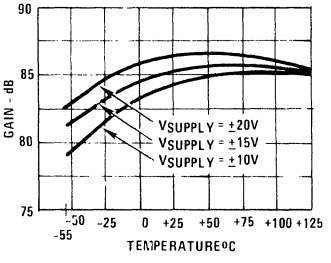


Typical Performance Characteristics LM318A

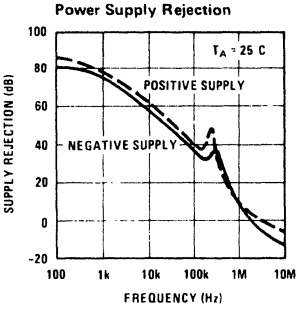
Input Bias and Offset Current vs Temperature



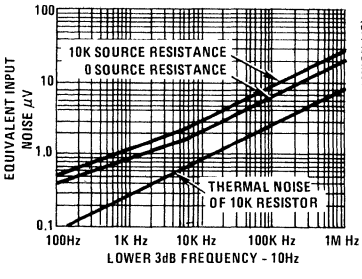
Open Loop Voltage Gain vs Temperature



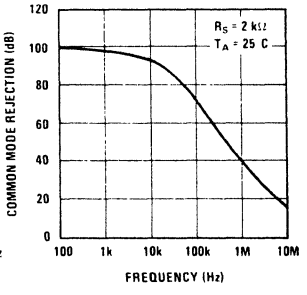
Power Supply Rejection



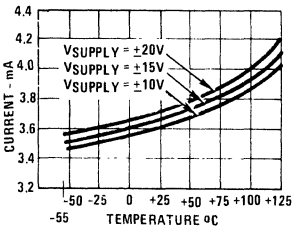
Equivalent Input Noise vs Bandwidth



Common Mode Rejection

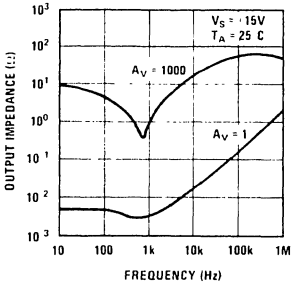


Power Supply Current vs Temperature

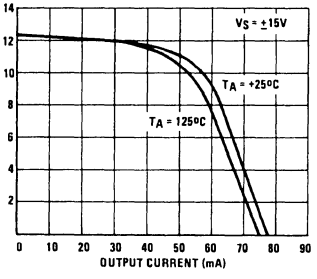


Typical Performance Characteristics LM318A (Continued)

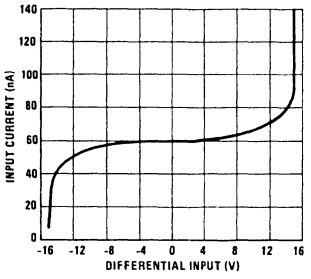
Closed Loop Output Impedance



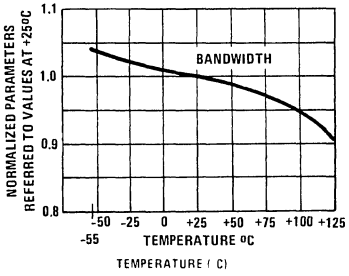
Output Current



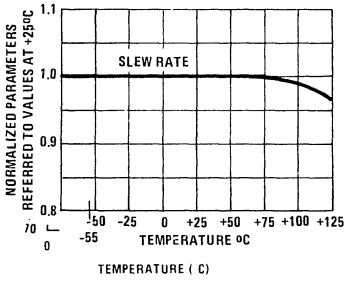
Input Current



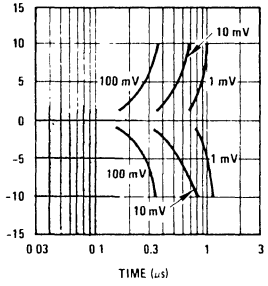
Normalized AC Parameters vs Temperature



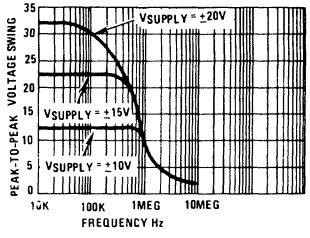
Normalized AC Parameters vs Temperature



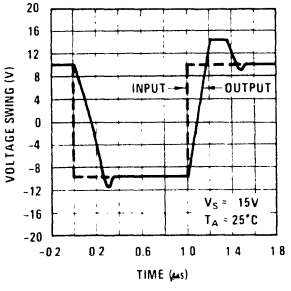
Inverter Settling Time



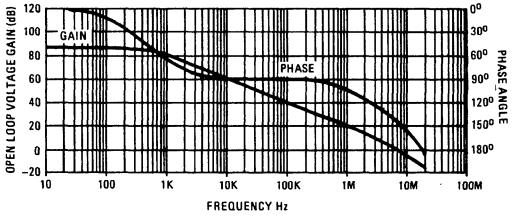
Output Voltage Swing vs Frequency at +25°C



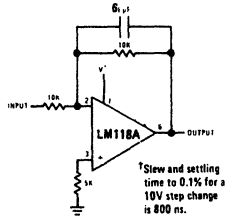
Voltage Follower Pulse Response



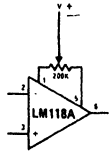
Open Loop Frequency and Phase Response



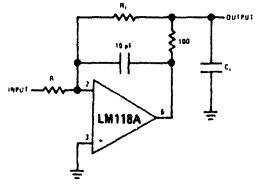
Auxiliary Circuits



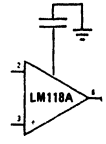
Compensation for Minimum Settling† Time



Offset Balancing

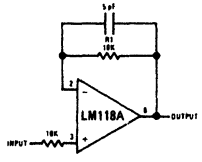


Isolating Large Capacitive Loads

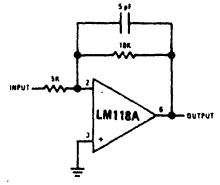


Overcompensation

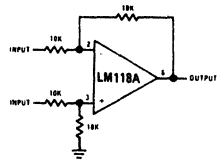
Typical Applications



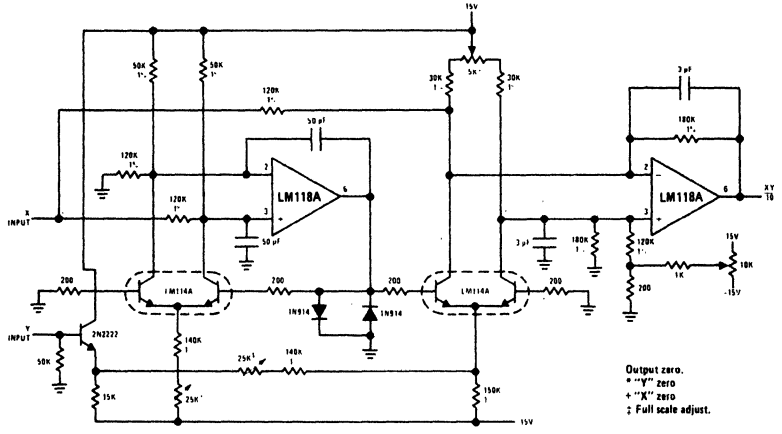
Fast Voltage Follower *



Fast Summing Amplifier

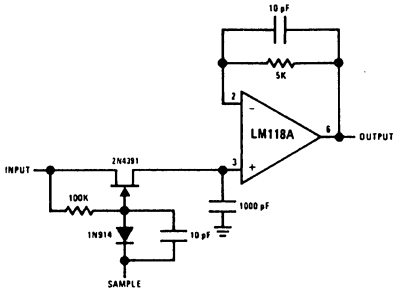


Differential Amplifier

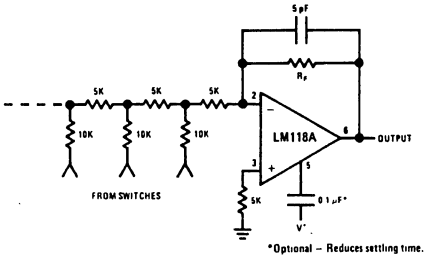


Four Quadrant Multiplier

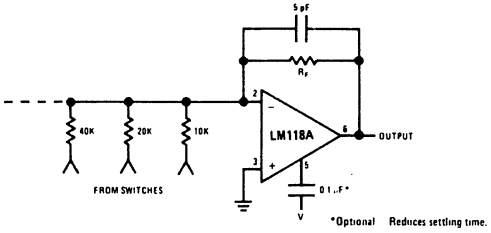
Typical Applications (Continued)



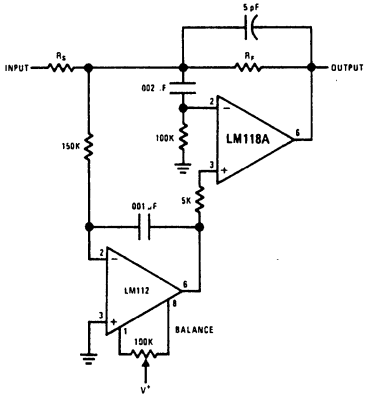
Fast Sample and Hold



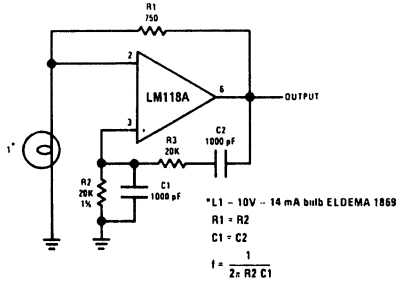
D/A Converter Using Ladder Network



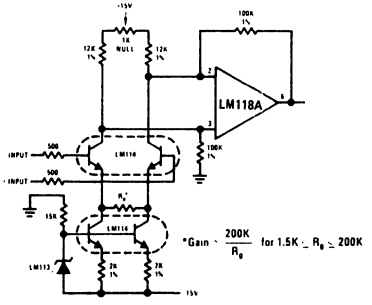
D/A Converter Using Binary Weighted Network



Fast Summing Amplifier
with Low Input Current



Wein Bridge Sine Wave Oscillator



Instrumentation Amplifier

HARRIS

LM143/LM343 High Voltage Operational Amplifier

General Description

The LM143 is a general purpose high voltage operational amplifier featuring operation to ±40V, complete input overvoltage protection up to ±40V and input currents comparable to those of other super-β op amps. Increased slew rate, together with higher common-mode and supply rejection, insure improved performance at high supply voltages. Operating characteristics, in particular supply current, slew rate and gain, are virtually independent of supply voltage and temperature. Furthermore, gain is unaffected by output loading at high supply voltages due to thermal symmetry on the die. The LM143 is pin compatible with general purpose op amps and has offset null capability.

Application areas include those of general purpose op amps, but can be extended to higher voltages and higher output power when externally boosted. For example, when used in audio power applications, the LM143 provides a power bandwidth that covers the entire audio spectrum. In addition, the LM143 can be reliably operated in environments with large overvoltage spikes on the power supplies, where other internally-compensated op amps would suffer catastrophic failure.

The LM343 is similar to the LM143 for applications in less severe supply voltage and temperature environments.

Features

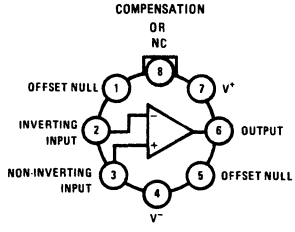
- Wide supply voltage range ±4.0V to ±40V
- Large output voltage swing ±37V
- Wide input common-mode range ±38V
- Input overvoltage protection Full ±40V
- Supply current is virtually independent of supply voltage and temperature

Unique Characteristics

- Low input bias current 10.0 nA
- Low input offset current 3.0 nA
- High slew rate—essentially independent of temperature and supply voltage 2.5V/μs
- High voltage gain—virtually independent of resistive loading, temperature, and supply voltage 100k min
- Internally compensated for unity gain
- Output short circuit protection
- Pin compatible with general purpose op amps

Connection Diagrams Section 11 for Packaging

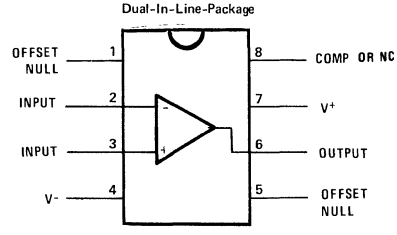
Metal Can Package



TOP VIEW

Order Number LM143H
or LM343H

Dual-In-Line-Package



TOP VIEW

Order Number LM143J
or LM343J, LM343N

Absolute Maximum Ratings (Note 1)

	LM143	LM343
Supply Voltage	±40V	±34V
Power Dissipation (Note 1)	680 mW	680 mW
Differential Input Voltage (Note 2)	80V	68V
Input Voltage (Note 2)	±40V	±34V
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Output Short Circuit Duration	5 seconds	5 seconds
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics

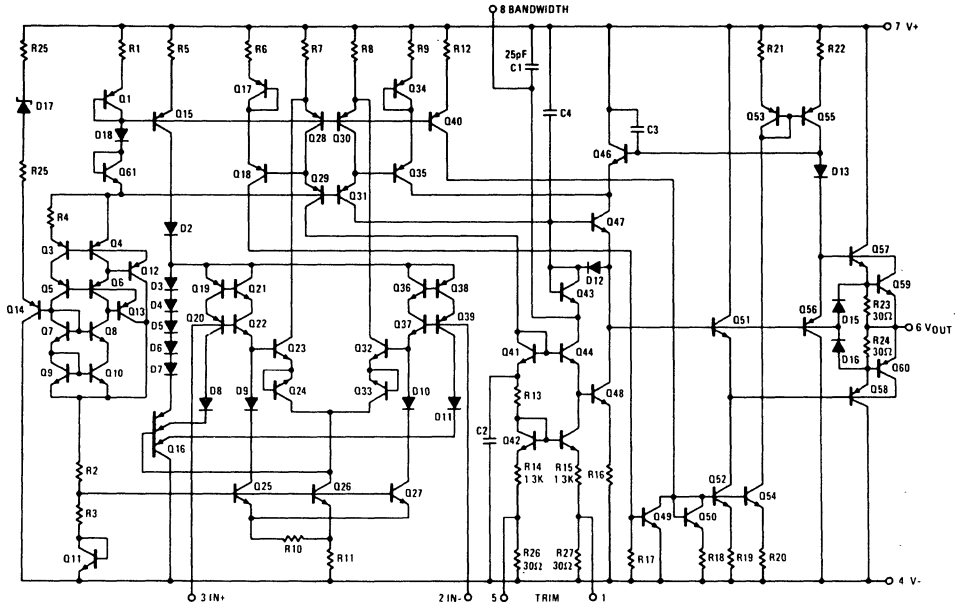
PARAMETER	CONDITIONS	LM143			LM343			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_S = \pm 28V$, $T_A = 25°C$, UNLESS OTHERWISE SPECIFIED		2.0	5.0		2.0	8.0	mV
Input Offset Current			3.0	12.0		3.0	30.0	nA
Input Bias Current			10.0	25.0		12.0	40	nA
Supply Voltage Rejection Ratio			10	100		10	200	μV/V
Output Voltage Swing	$R_L \geq 5$ k	22	25		20	25		V
Large Signal Voltage Gain	$V_{OUT} = 10V$, $R_L \geq 100$ k	100k	180k		70k	180k		V/V
Common-Mode Rejection Ratio		80	90		70	90		dB
Input Voltage Range		24	26		22	26		V
Supply Current			2.8	4.0		2.8	5.0	mA
Short Circuit Current			20			20		mA
Slew Rate	$A_V = 1$		2.5			2.5		V/μs
Power Bandwidth	$V_{OUT} = 40\ V_{p\text{-}p}$, $R_L = 5$ k THD ≥ 1%		20k			20k		Hz
Unity Gain Frequency	$T_A = 25°C$		1.0M			1.0M		Hz
Input Offset Voltage	T_A = Max (Note 3)			6.0			10	mV
	T_A = Min			6.0			10	mV
Input Offset Current	T_A = Max		0.8	4.5		0.8	14	nA
	T_A = Min		4.0	35.0		4.0	50.0	nA
Input Bias Current	T_A = Max		5.0	35		5.0	55	nA
	T_A = Min		16	50.0		16	55	nA
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$	50k	150k		50k	150k		V/V
	$R_L \geq 100\ k\Omega$	50k	220k		50k	220k		V/V
Output Voltage Swing	$R_L \geq 5.0\ k\Omega$	22	26		20	26		V
	$R_L \geq 5.0\ k\Omega$	22	25		20	25		V

Note 1: Absolute maximum ratings are not necessarily concurrent, and care must be taken not to exceed the maximum junction temperature of the LM143 (150°C) or the LM343 (100°C). For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltage less than ±40V for the LM143 and less than ±34V for the LM343, the absolute maximum input voltage is equal to the supply voltage.

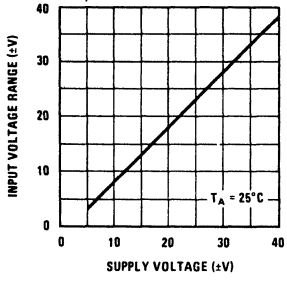
Note 3: For the LM143, $-55°C \leq T_A \leq +125°C$ and for the LM343, $0°C \leq T_A \leq 70°C$.

Schematic Diagram

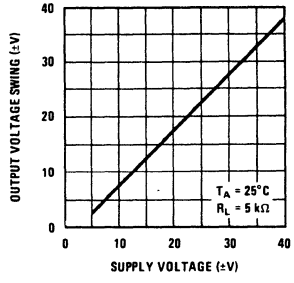


Typical Performance Characteristics

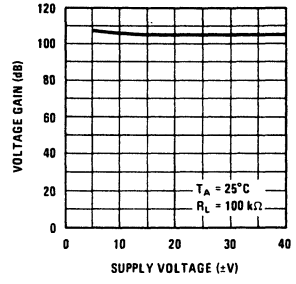
Input Voltage Range



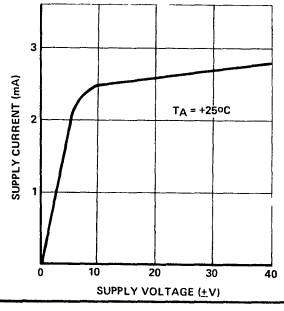
Output Voltage Swing



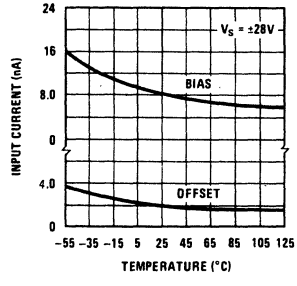
Voltage Gain



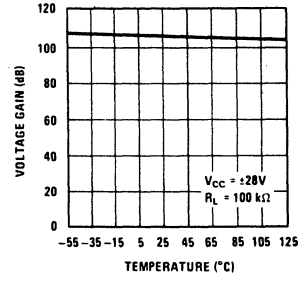
Supply Current



Input Current

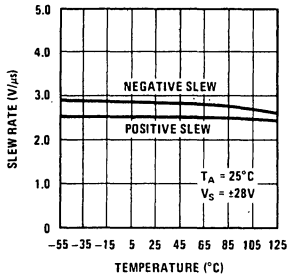


Voltage Gain

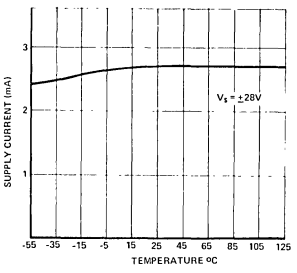


Typical Performance Characteristics (Continued)

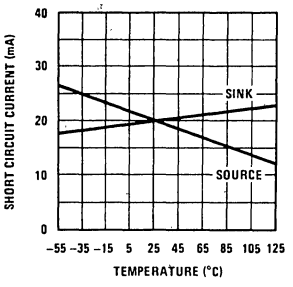
Voltage Follower Slew Rate



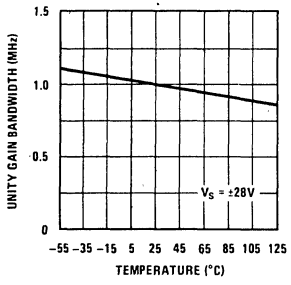
Supply Current



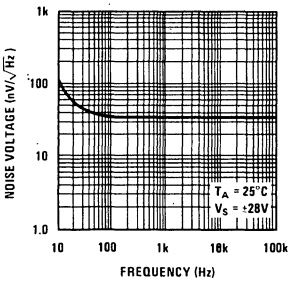
Short Circuit Current



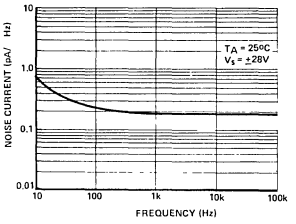
Unity Gain Bandwidth



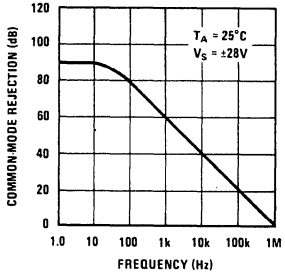
Input Noise Voltage



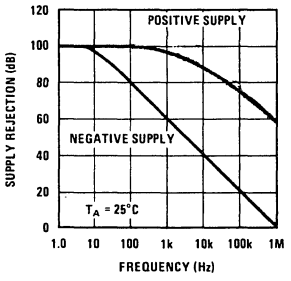
Input Noise Current



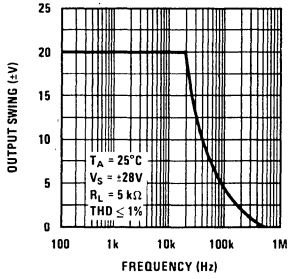
Common-Mode Rejection



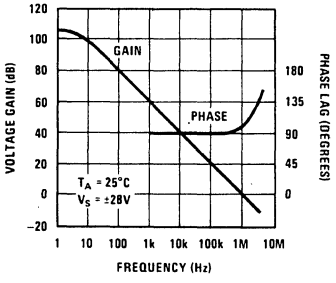
Power Supply Rejection



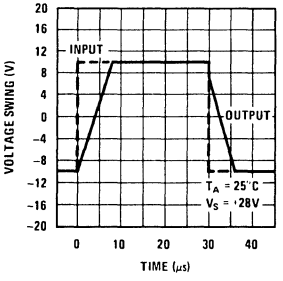
Large Signal Frequency Response



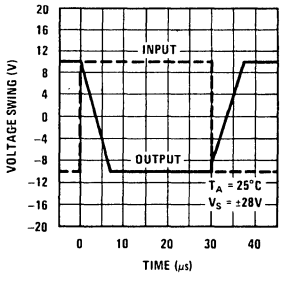
Open Loop Frequency Response



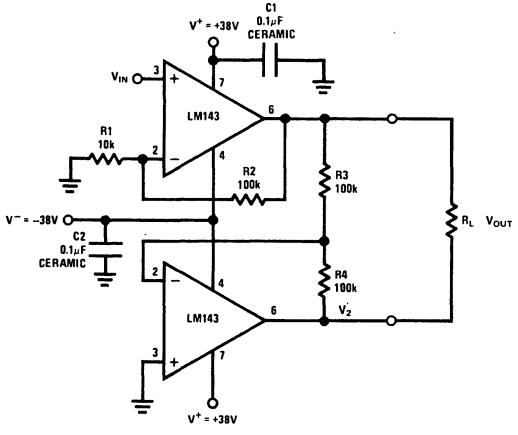
Voltage Follower Pulse Response



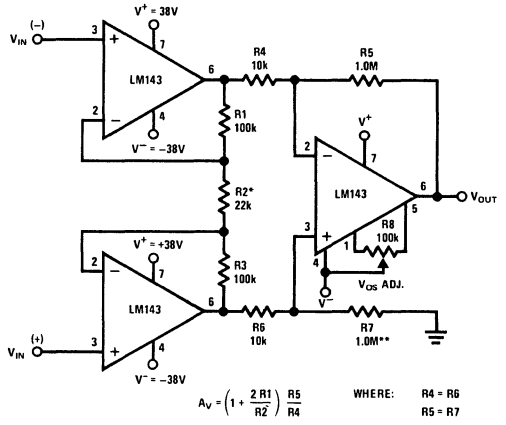
Inverter Pulse Response



Typical Applications ‡



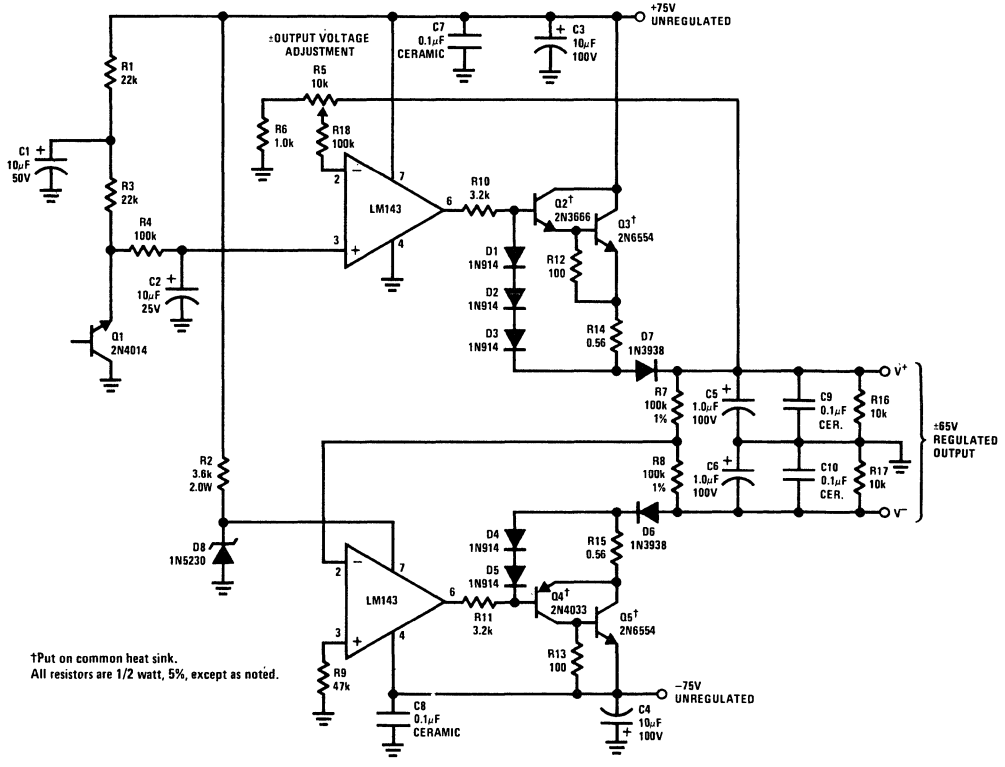
130 V_{P-P} Drive Across a Floating Load



*R2 may be adjustable to trim the gain.

**R7 may be adjusted to compensate for the resistance tolerance of R4 – R7 for best CMR.

±34V Common-Mode Instrumentation Amplifier

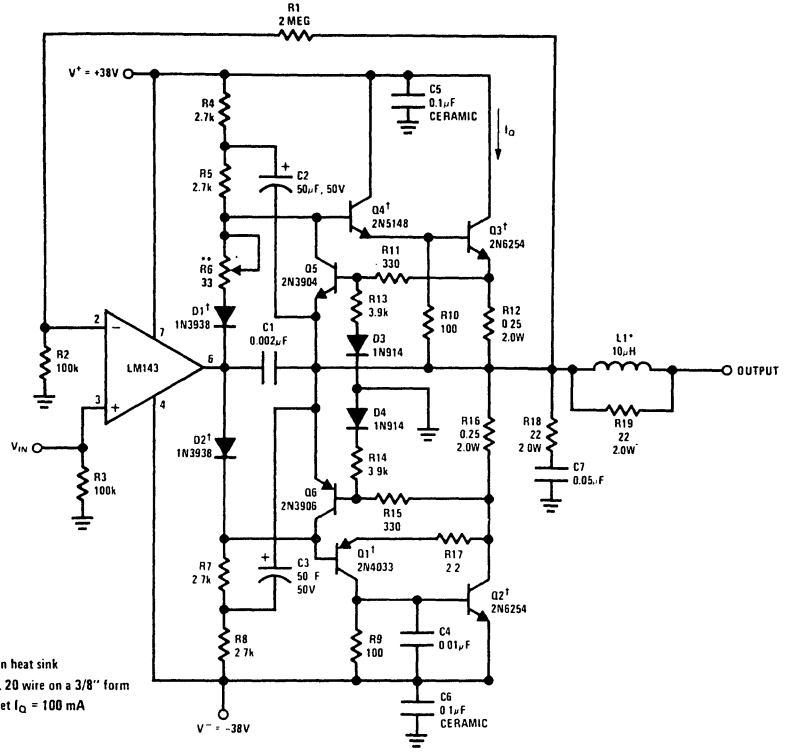


†Put on common heat sink.
All resistors are 1/2 watt, 5%, except as noted.

Tracking ±65V, 1 Amp Power Supply with Short Circuit Protection

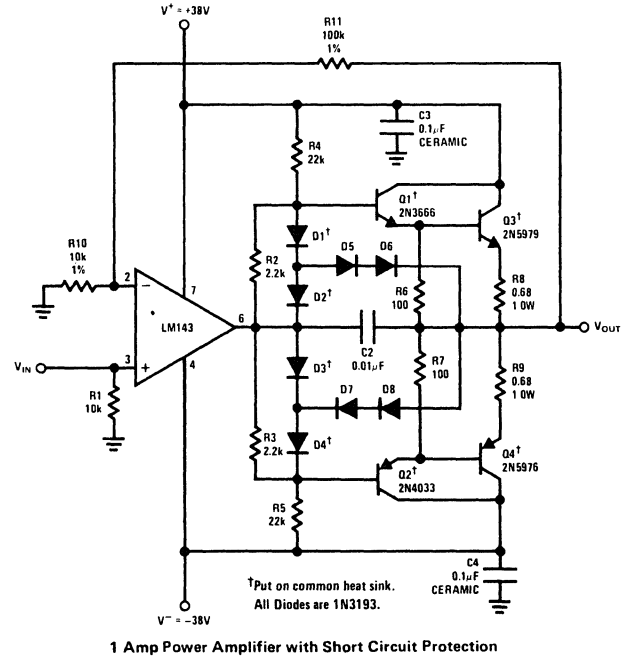
‡The 38V supplies allow for a 5% voltage tolerance. All resistors are 1/2 watt, except as noted.

Typical Applications (Continued)



†Put on common heat sink
*34 turns of no. 20 wire on a 3/8" form
**Adjust R6 to set I_Q = 100 mA

90W Audio Power Amplifier with Safe Area Protection



†Put on common heat sink.
All Diodes are 1N3193.

1 Amp Power Amplifier with Short Circuit Protection

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are 1/2 watt, except as noted.

Application Hints

The LM143 is designed for trouble free operation at any supply voltage up to and including the guaranteed maximum of ±40V. Input overvoltage protection, both common-mode and differential, is 100% tested and guaranteed at the maximum supply voltage. Furthermore, all possible high voltage destructive modes during supply voltage turn-on have been eliminated by design. As with most IC op amps, however, certain precautions should be observed to insure that the LM143 remains virtually blow-out proof.

Although output short circuits to ground or either supply can be sustained indefinitely at lower supply voltages, these short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM143 can drive most general purpose op amps outside of the maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. Voltage reversal between the power supplies will almost always result in a destroyed unit.

In high voltage applications which are sensitive to very low input currents, special precautions should be exercised. For example, with high source resistances, care should be taken to prevent the magnitude of the PC board leakage currents, although quite small, from approaching those of the op amp input currents. These leakage currents become larger at 125°C and are made worse by high supply voltages. To prevent this, PC boards should be properly cleaned and coated to prevent contamination and to provide protection from condensed water vapor when operating below 0°C. A guard ring is also recommended to significantly reduce leakage currents from the op amp input pins to the adjacent high voltage pins in the standard op amp pin connection as shown in *Figure 1. Figures 2, 3 and 4* show how the guard ring is connected for the three most common op amp configurations.

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present.

The LM143 can be used as a plug-in replacement in most general purpose op amp applications. The circuits presented in the following section emphasize those applications which take advantage of unique high voltage capabilities of the LM143.

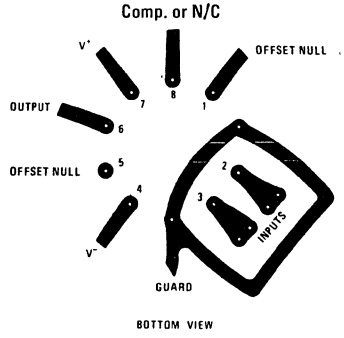


FIGURE 1. Printed Circuit Layout for Input Guarding with TO-5 Package

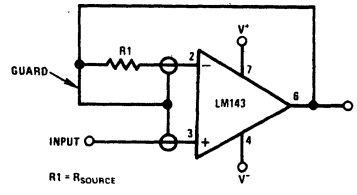


FIGURE 2. Guarded Voltage Follower

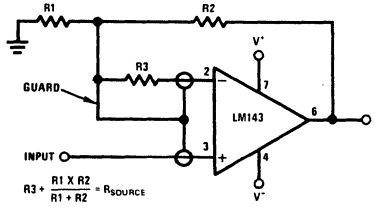


FIGURE 3. Guarded Non-Inverting Amplifier

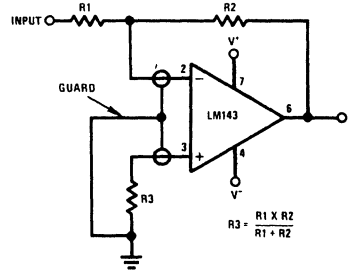


FIGURE 4. Guarded Inverting Amplifier

LM143A/LM343A High Voltage Operational Amplifier

General Description

The LM143A is a general purpose high voltage operational amplifier featuring operation to ±50V, complete input overvoltage protection up to ±50V and input currents comparable to those of other super-β op amps. Increased slew rate, together with higher common-mode and supply rejection, insure improved performance at high supply voltages. Operating characteristics, in particular supply current, slew rate and gain, are virtually independent of supply voltage and temperature, furthermore, gain is unaffected by output loading at high supply voltages due to thermal symmetry on the die. The LM143A is pin compatible with general purpose op amps and has offset null capability.

Application areas include those of general purpose op amps, but can be extended to higher voltages and higher output power when externally boosted. For example, when used in audio power applications, the LM143A provides a power bandwidth that covers the entire audio spectrum. In addition, the LM143A can be reliably operated in environments with large overvoltage spikes on the power supplies, where other internally compensated op amps would suffer catastrophic failure.

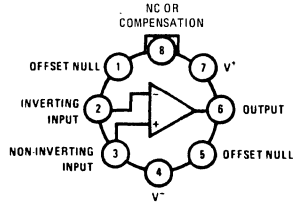
The LM343A is similar to the LM143A for applications in less severe supply voltage and temperature environments.

Features

- Wide supply voltage range ±4.0V to ±50V
- Large output voltage swing ±47V
- Wide Input common-mode range ±48V
- Input overvoltage protection Full ±50V
- Supply current is virtually independent of supply voltage and temperature
- Low input bias current 10.0 nA
- Low input offset current 3.0 nA
- High slew rate-essentially independent of temperature and supply voltage 5.0V/μs
- High voltage gain-virtually independent of resistive loading, temperature, and supply voltage 100k min
- Internally compensated for unity gain
- Pin compatible with general purpose op amps

Connection Diagrams Section 11 for Packaging

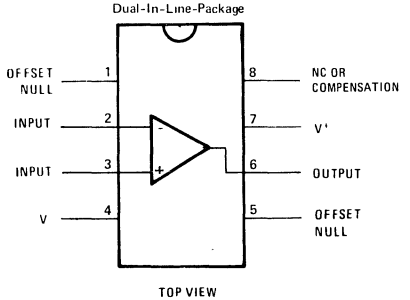
Metal Can Package



TOP VIEW

Order Number LM143AH
or LM343AH

Dual-In-Line-Package



TOP VIEW

Order Number LM143AJ-8
or LM343AJ-8, LM343AN

Absolute Maximum Ratings (Note 1)

	LM143A	LM343A
Supply Voltage	±55V	±55V
Power Dissipation (Note 1)	680 mW	680 mW
Differential Input Voltage (Note 2)	100V	80V
Input Voltage (Note 2)	±50V	±45V
Operating Temperature Range	-55°C to 125°C	0°C to 70°C
Storage Temperature Range	-65°C to 150°C	-65°C to 150°C
Output Short Circuit Duration	Indefinite	Indefinite
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics

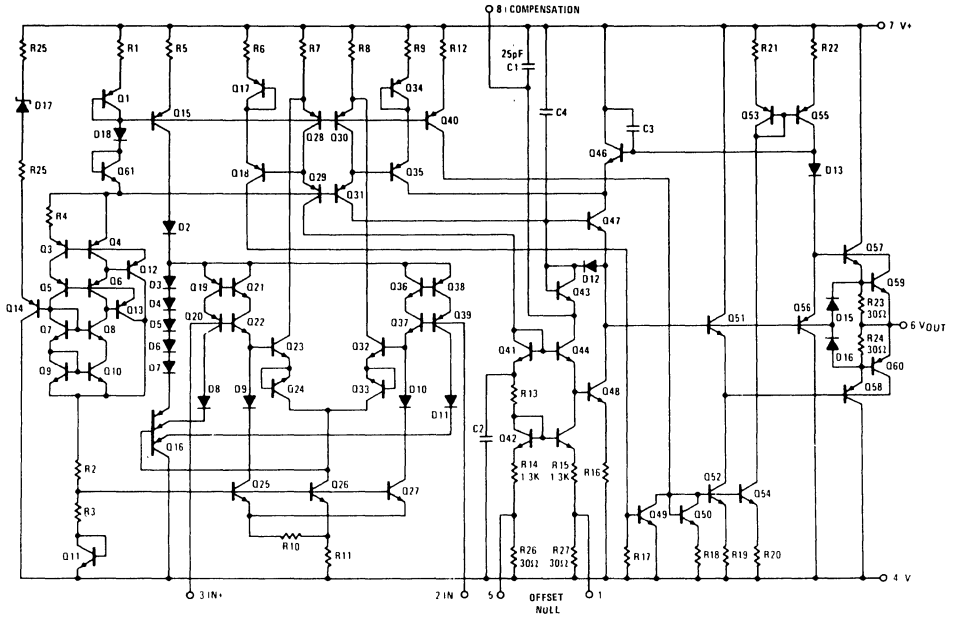
PARAMETER	CONDITIONS	LM143A			LM343A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_S = \pm 50V$, $T_A = 25°C$		2.0	4.0		2.0	6.0	mV
Input Offset Current			3.0	12.0		15.0	30.0	nA
Input Bias Current			10.0	25.0		12.0	30.0	nA
Supply Voltage Rejection Ratio			10	100		10	200	μV/V
Output Voltage Swing	$R_L \geq 5$ k	± 35			± 35			V
Large Signal Voltage Gain	$V_{OUT} = \pm 30V$, $R_L \geq 10$ k	100k	200k		100k	200k		V/V
Common-Mode Rejection Ratio		80	100		74	100		dB
Input Voltage Range		± 35			± 35			V
Supply Current			3.2	3.8		3.2	4.5	mA
Short Circuit Current			20			20		mA
Slew Rate	$A_V = 1$		5			5		V/μs
Power Bandwidth	$V_{OUT} = 70V_{p-p}$, $R_L = 5\ k\Omega$, THD ≤1%		20k			20k		Hz
Unity Gain Frequency			4.0			4.0		MHz
Input Offset Voltage	T_A = Max (Note 3)			6.0			7.0	mV
	T_A = Min			6.0			7.0	mV
Input Offset Current	T_A = Max		0.8	4.5		0.8	14	nA
	T_A = Min		4.0	35.0		1.8	50.0	nA
Input Bias Current	T_A = Max		5.0	35		5.0	55	nA
	T_A = Min		16	50.0		16	55	nA
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$, T_A = Max	75k	150k		75k	150k		V/V
	$R_L \geq 100\ k\Omega$, T_A = Min	75k	220k		75k	220k		V/V
Output Voltage Swing	$R_L \geq 5.0\ k\Omega$, T_A = Max	± 35			± 35			V
	$R_L \geq 5.0\ k\Omega$, T_A = Min	± 35			± 35			V

Note 1: Absolute maximum ratings are not necessarily concurrent, and care must be taken not to exceed the maximum junction temperature of the LM143A (150°C) or the LM343A (100°C). For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltage less than ±50V for the LM143A and less than ±45V for the LM343A the absolute maximum input voltage is equal to the supply voltage.

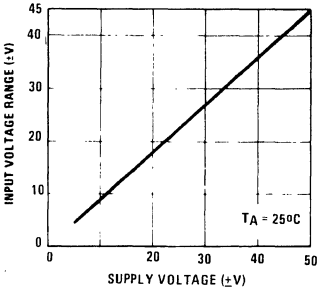
Note 3: For the LM143A, $-55°C \leq T_A \leq +125°C$ and for the LM343A, $0°C \leq T_A \leq +70°C$.

Schematic Diagram

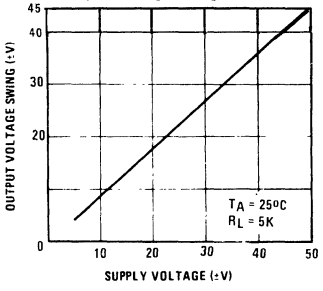


Typical Performance Characteristics

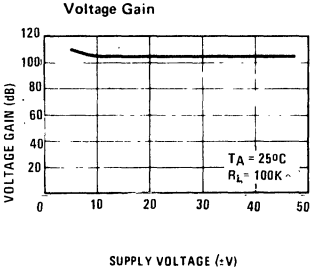
Input Voltage Range



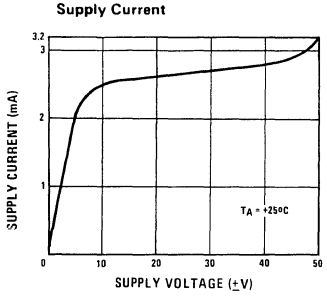
Output Voltage Swing



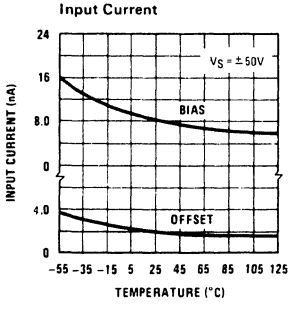
Voltage Gain



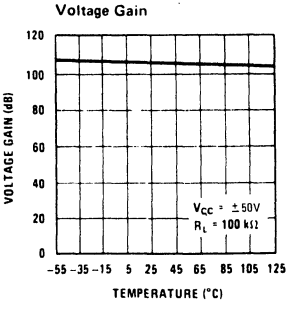
Supply Current



Input Current

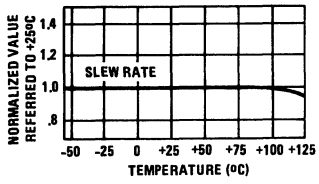


Voltage Gain

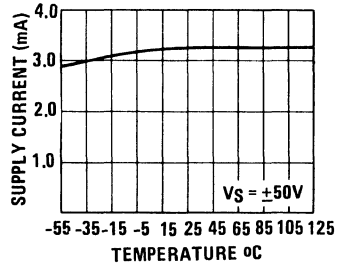


Typical Performance Characteristics (Continued)

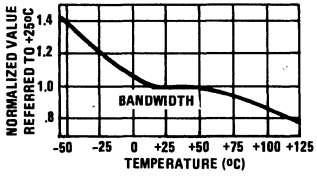
Normalized Slew Rate vs. Temperature



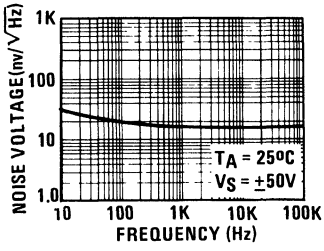
Supply Current



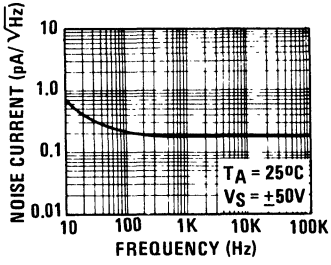
Normalized Gain Bandwidth vs. Temperature



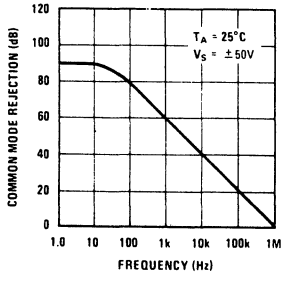
Input Noise Voltage



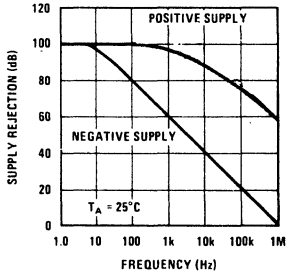
Input Noise Current



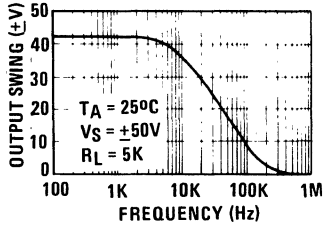
Common-Mode Rejection



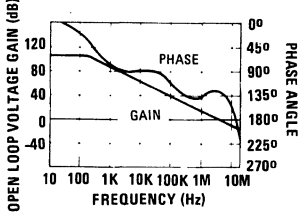
Power Supply Rejection



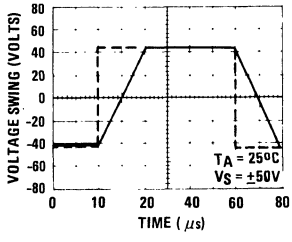
Large Signal Frequency Response



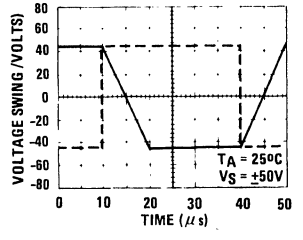
Open Loop Frequency Response



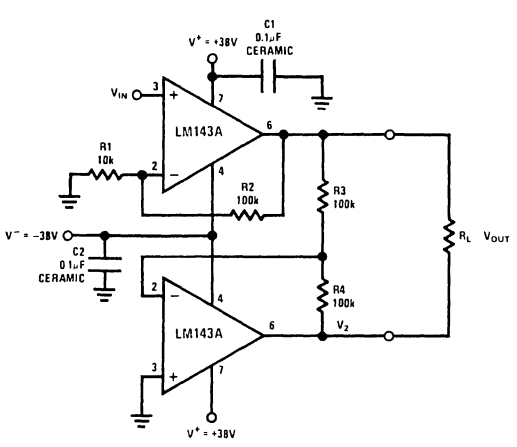
Voltage Follower Pulse Response



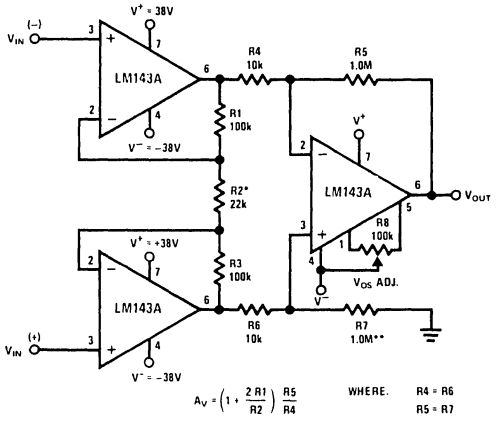
Inverter Pulse Response



Typical Applications ‡



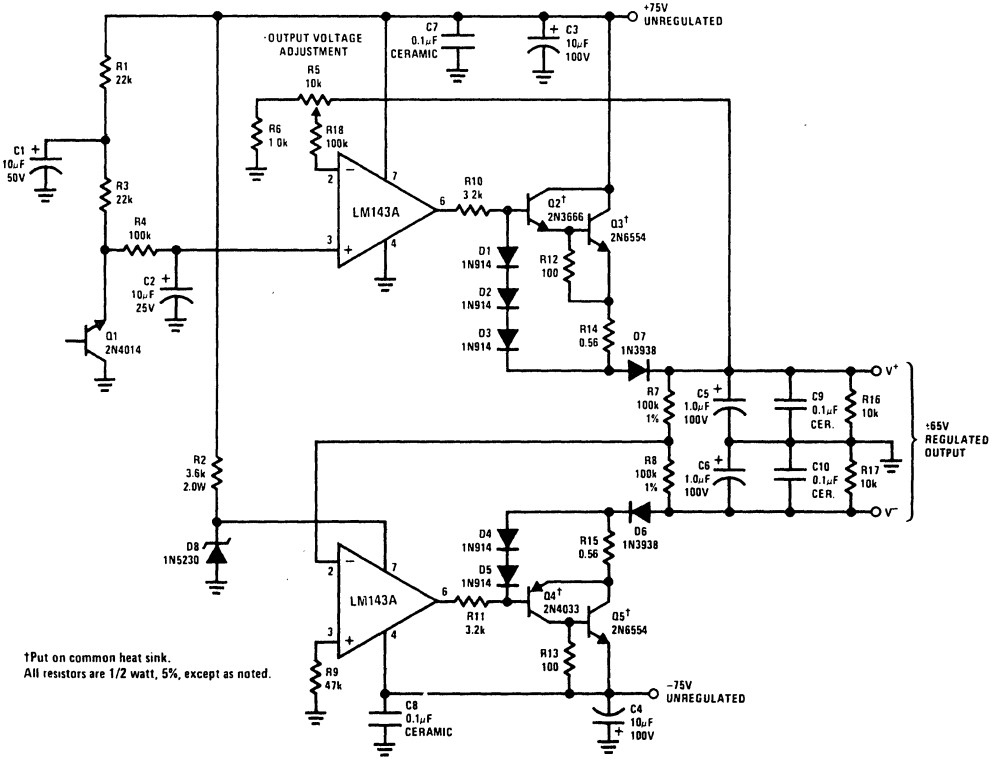
130 Vp-p Drive Across a Floating Load



*R2 may be adjustable to trim the gain.

**R7 may be adjusted to compensate for the resistance tolerance of R4 – R7 for best CMR.

±34V Common-Mode Instrumentation Amplifier



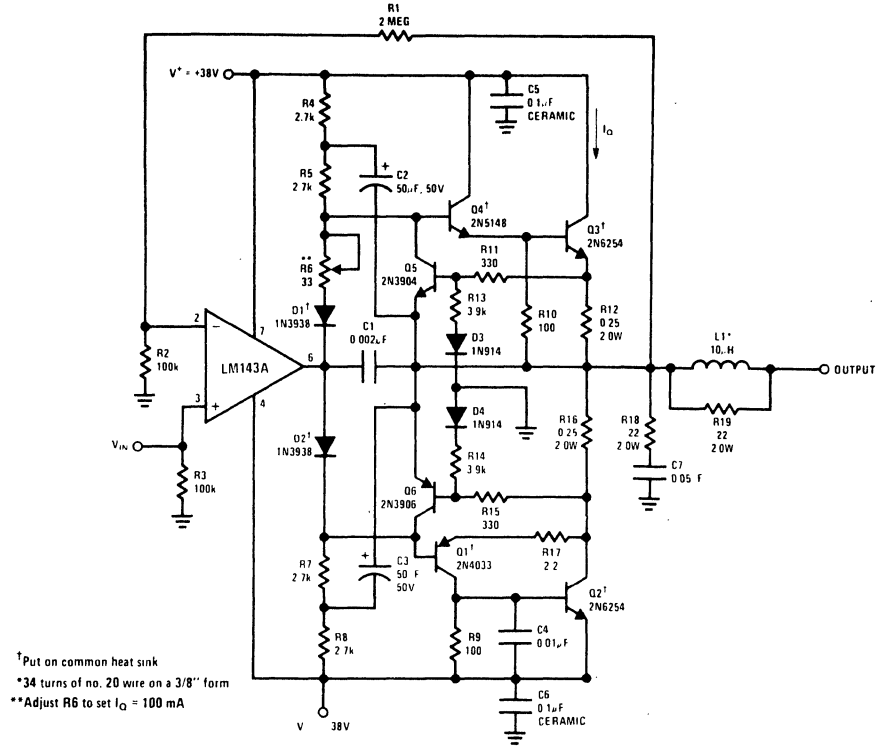
†Put on common heat sink.
All resistors are 1/2 watt, 5%, except as noted.

Tracking ±65V, 1 Amp Power Supply with Short Circuit Protection

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are 1/2 watt, except as noted.

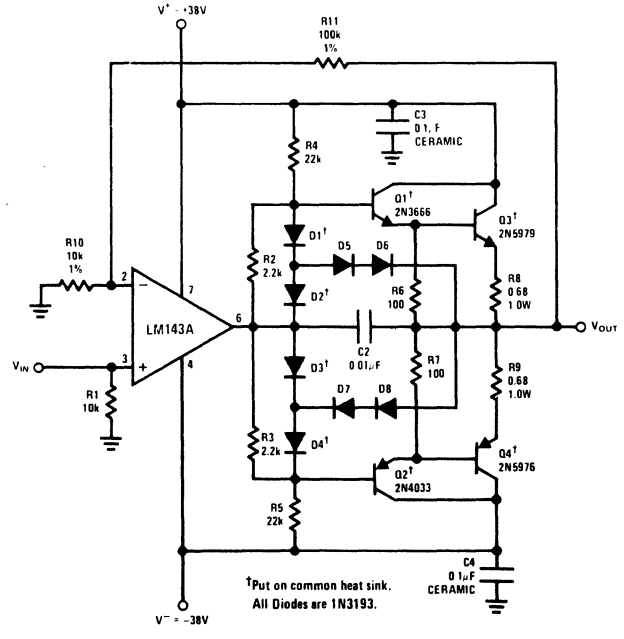
2

Typical Applications (Continued)



†Put on common heat sink
*34 turns of no. 20 wire on a 3/8" form
**Adjust R6 to set I_O = 100 mA

90W Audio Power Amplifier with Safe Area Protection



†Put on common heat sink.
All Diodes are 1N3193.

1 Amp Power Amplifier with Short Circuit Protection

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are 1/2 watt, except as noted.

Application Hints

The LM143A is designed for trouble free operation at any supply voltage up to and including the guaranteed maximum of ±55V. Input overvoltage protection, both common-mode and differential, is 100% tested and guaranteed at the maximum supply voltage. Furthermore, all possible high voltage destructive modes during supply voltage turn-on have been eliminated by design. As with most IC op amps, however, certain precautions should be observed to insure that the LM143A remains virtually blow out proof.

Although output short circuits to ground or either supply can be sustained indefinitely at lower supply voltages, these short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM143A can drive most general purpose op amps outside of the maximum input voltage range, causing heavy current to flow and possible destroying both devices.

Precautions should be taken to insure that the power supplies never become reversed in polarity-even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. Voltage reversal between the power supplies will almost always result in a destroyed unit.

In high voltage applications which are sensitive to very low input currents, special precautions should be exercised. For example, with high source resistances, care should be taken to prevent the magnitude of the PC Board leakage currents, although quite small, from approaching those of the op amp input currents. These leakage currents become larger at 125°C and are made worse by high supply voltages. To prevent this, PC boards should be properly cleaned and coated to prevent contamination and to provide protection from condensed water vapor when operating below 0°C. A guard ring is also recommended to significantly reduce leakage currents from the op amp input pins to the adjacent high voltage pins in the standard op amp pin connection as shown in Figure 1. Figures 2, 3 and 4 show how the guard ring is connected for the three most common op amp configurations.

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present.

The LM143A can be used as a plug-in replacement in most general purpose op amp applications. The circuits presented in the following section emphasize those applications which take advantage of the unique high voltage capabilities of the LM143A.

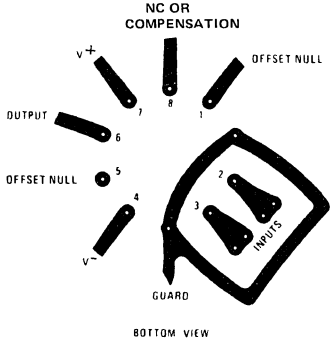


FIGURE 1. Printed Circuit Layout for Input Guarding with TO-5 Package

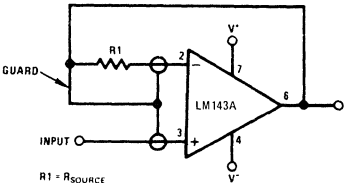


FIGURE 2. Guarded Voltage Follower

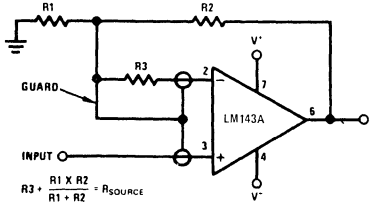


FIGURE 3. Guarded Non-Inverting Amplifier

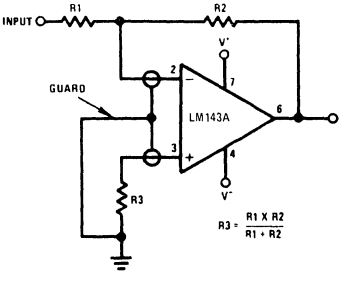


FIGURE 4. Guarded Inverting Amplifier

HARRIS

LM146/LM346 Programmable Quad Operational Amplifiers

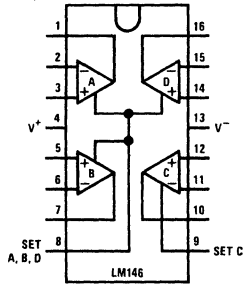
General Description

The LM146 series of quad op amps consists of four independent, high gain, internally compensated, low power, programmable amplifiers. Two external resistors (R_{SET}) allow the user to program the gain bandwidth product, slew rate, supply current, input bias current, input offset current and input noise. For example, the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way, other amplifier characteristics can be tailored to the application. Except for the two programming pins at the end of the package, the LM146 pin-out is the same as the LM124 and LM148.

Features (I_{SET} = 10 μA)

- Programmable electrical characteristics
- Battery-powered operation
- Low supply current — 350 μA amplifier
- Guaranteed gain bandwidth product — 0.8 MHz min
- Large DC voltage gain — 105 dB
- Low noise voltage — 28 nV/√Hz
- Wide power supply range — ±1.5V to ±22V
- Class AB output stage—no crossover distortion
- Ideal pin out for Biquad active filters

Connection Diagrams (Dual-In-Line Packages, Top Views) **Section 11 for Packaging**



Order Number LM146J or LM346J

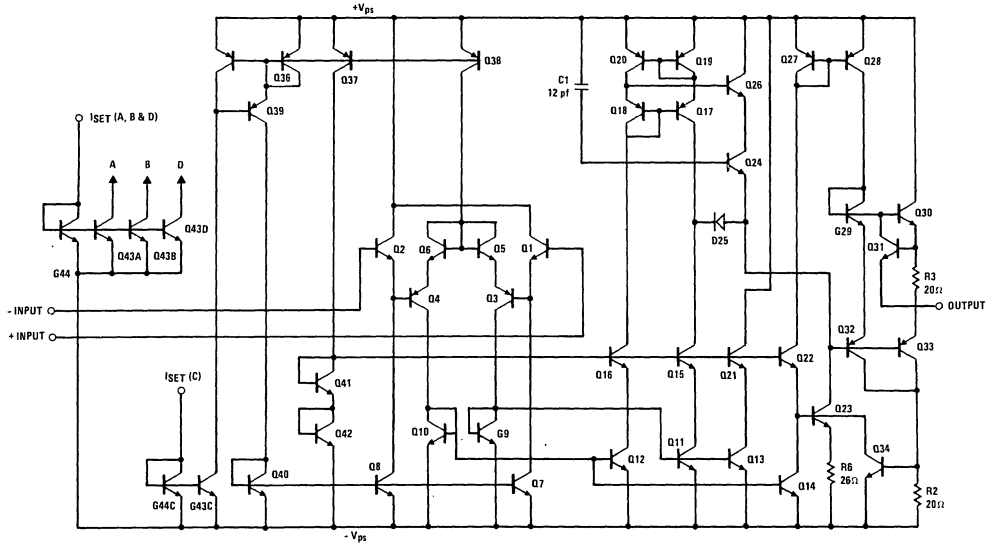
Order Number LM346N

PROGRAMMING EQUATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)
Gain Bandwidth Product = 1 MHz (I_{SET}/10 μA)
Slew Rate = 0.4V/μs (I_{SET}/10 μA)
Input Bias Current ≈ 50 nA (I_{SET}/10 μA)
I_{SET} = Current into pin 8, pin 9 (see schematic-diagram)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

Schematic Diagram



Absolute Maximum Ratings (Note 1)

	LM146	LM346
Supply Voltage	±22V	±18V
Differential Input Voltage (Note 1)	±30V	±30V
CM Input Voltage (Note 1)	±15V	±15V
Power Dissipation (Note 2)	900 mW	500 mW
Output Short-Circuit Duration (Note 3)	Indefinite	Indefinite
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
Maximum Junction Temperature	150°C	100°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C
Thermal Resistance (θ_{jA}), (Note 2)		
Cavity DIP (D) (J) P_d	900 mW	900 mW
θ_{jA}	90°C/W	90°C/W
Molded DIP (N) P_d		500 mW
θ_{jA}		140°C/W

DC Electrical Characteristics (V_S = ±15V, I_{SET} = 10 μA, Note 4)

PARAMETER	CONDITIONS	LM146			LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{CM} = 0V, $R_S \leq 50\ \Omega$, T_A = 25°C		0.5	5		0.5	6	mV
Input Offset Current	V_{CM} = 0V, T_A = 25°C		2	20		2	100	nA
Input Bias Current	V_{CM} = 0V, T_A = 25°C		50	100		50	250	nA
Supply Current (4 Op Amps)	T_A = 25°C		1.4	2.0		1.4	2.5	mA
Large Signal Voltage Gain	R_L = 10 kΩ, ΔV_{OUT} = ±10V, T_A = 25°C	30	120		50	120		V/mV
Input CM Range	T_A = 25°C	±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq$ 10 kΩ, T_A = 25°C	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq$ 10 kΩ, T_A = 25°C	80	100		74	100		dB
Output Voltage Swing	$R_L \geq$ 10 kΩ, T_A = 25°C	±12	±14		±12	±14		V
Short-Circuit Current	T_A = 25°C	5	20	30	5	20	30	mA
Gain Bandwidth Product	T_A = 25°C	0.8	1.2		0.5	1.2		MHz
Phase Margin	T_A = 25°C		60			60		Deg
Slew Rate	T_A = 25°C		0.4			0.4		V/μs
Input Noise Voltage	f = 1 kHz, T_A = 25°C		28			28		$nV/\sqrt{Hz}$
Channel Separation	R_L = 10 kΩ, ΔV_{OUT} = 0V to ±12V, T_A = 25°C		120			120		dB
Input Resistance	T_A = 25°C		1.0			1.0		MΩ
Input Capacitance	T_A = 25°C		2.0			2.0		pF
Input Offset Voltage	V_{CM} = 0V, $R_S \leq 50\ \Omega$		0.5	6		0.5	7.5	mV
Input Offset Current	V_{CM} = 0V		2	25		2	100	nA
Input Bias Current	V_{CM} = 0V		50	100		50	250	nA
Supply Current (4 Op Amps)			1.5	2.0		1.5	2.5	mA
Large Signal Voltage Gain	R_L = 10 kΩ, ΔV_{OUT} = ±10V	20	120		25	120		V/mV
Input CM Range		±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 50\ \Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 50\ \Omega$	76	100		74	100		dB
Output Voltage Swing	$R_L \geq$ 10 kΩ	±12	±14		±12	±14		V

DC Electrical Characteristics ($V_S = \pm 15V$, $I_{SET} = 1\ \mu A$)

PARAMETER	CONDITIONS	LM146			LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\ \Omega$, $T_A = 25°C$		0.5	5		0.5	7	mV
Input Bias Current	$V_{CM} = 0V$, $T_A = 25°C$		7.5	20		7.5	100	nA
Supply Current (4 Op Amps)	$T_A = 25°C$		140	250		140	300	μA
Gain Bandwidth Product	$T_A = 25°C$	80	100		50	100		kHz

DC Electrical Characteristics ($V_S = \pm 1.5V$, $I_{SET} = 10\ \mu A$)

PARAMETER	CONDITIONS	LM146			LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{CM} = 0V$, $R_S \leq 50\ \Omega$, $T_A = 25°C$		0.5	5		0.5	7	mV
Input CM Range	$T_A = 25°C$	±0.7			±0.7			V
CM Rejection Ratio	$R_S \leq 50\ \Omega$, $T_A = 25°C$		80			80		dB
Output Voltage Swing	$R_L \geq 10\ k\Omega$, $T_A = 25°C$	±0.6			±0.6			V

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

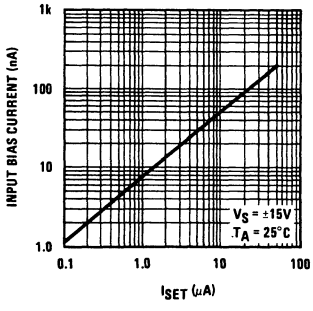
Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

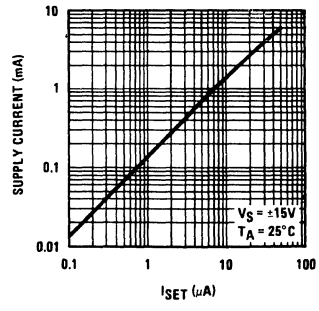
Note 4: These specifications apply over the absolute maximum operating temperature range unless otherwise noted.

Typical Performance Characteristics

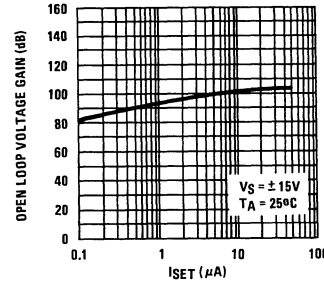
Input Bias Current vs I_{SET}



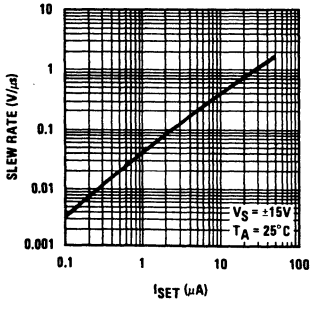
Supply Current vs I_{SET}



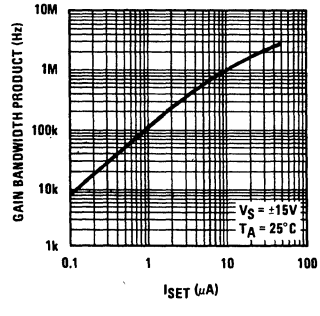
Open Loop Voltage Gain vs I_{SET}



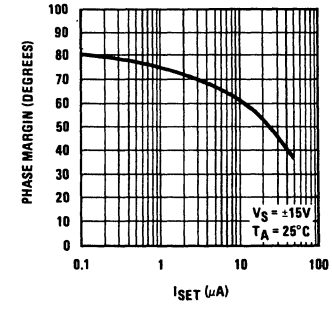
Slew Rate vs I_{SET}



Gain Bandwidth Product vs I_{SET}

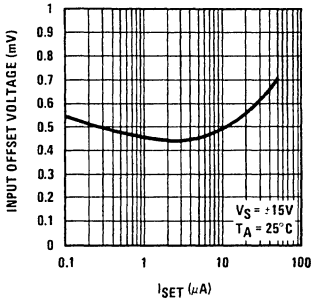


Phase Margin vs I_{SET}

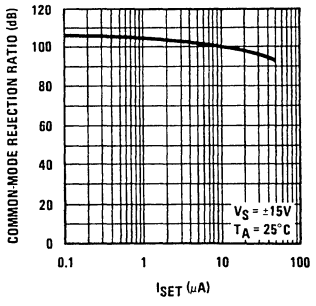


Typical Performance Characteristics (Continued)

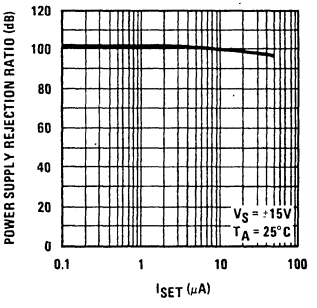
Input Offset Voltage vs I_{SET}



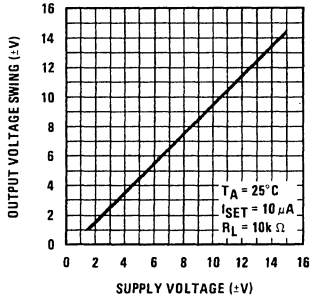
Common-Mode Rejection Ratio vs I_{SET}



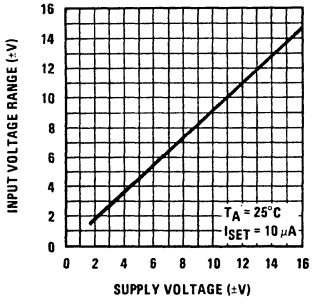
Power Supply Rejection Ratio vs I_{SET}



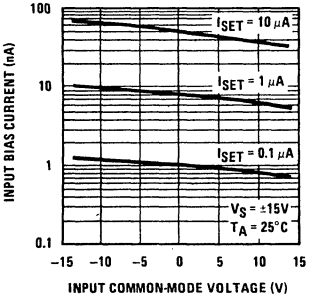
Output Voltage Swing vs Supply Voltage



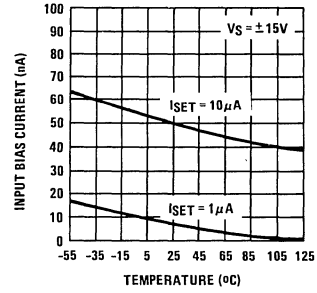
Input Voltage Range vs Supply Voltage



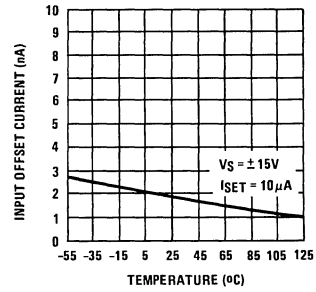
Input Bias Current vs Input Common-Mode Voltage



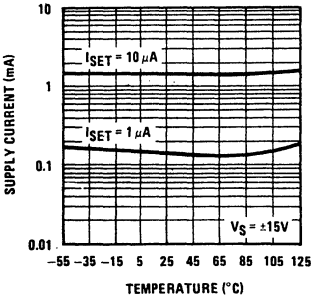
Input Bias Current vs Temperature



Input Offset Current vs Temperature

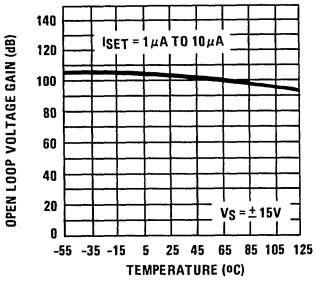


Supply Current vs Temperature

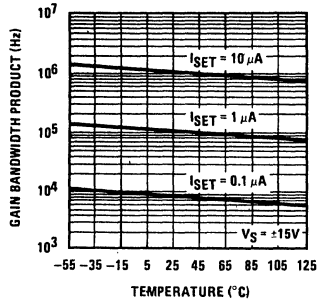


Typical Performance Characteristics (Continued)

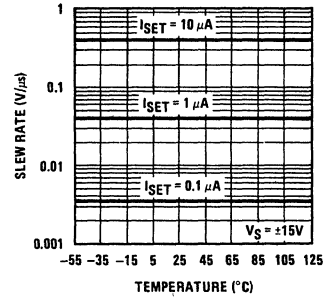
Open Loop Voltage Gain vs Temperature



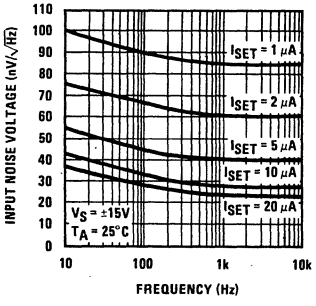
Gain Bandwidth Product vs Temperature



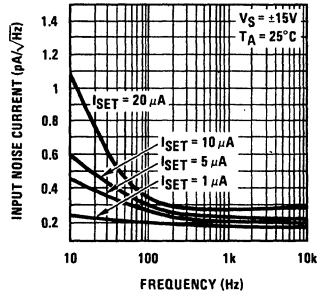
Slew Rate vs Temperature



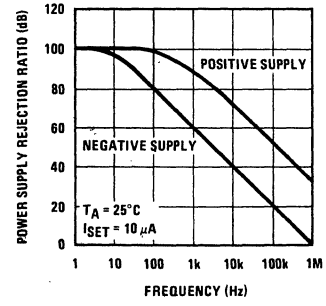
Input Noise Voltage vs Frequency



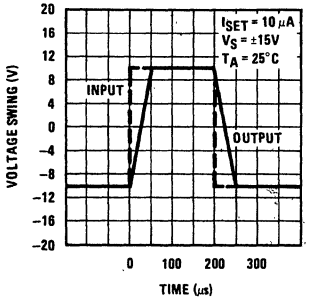
Input Noise Current vs Frequency



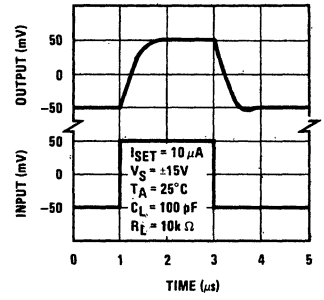
Power Supply Rejection Ratio vs Frequency



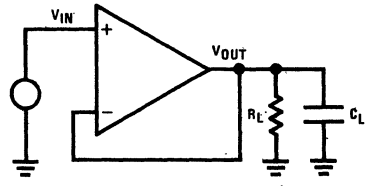
Voltage Follower Pulse Response



Voltage Follower Transient Response



Transient Response Test Circuit



Application Hints

Avoid reversing the power supply polarity, the device will fail.

Common-Mode Input Voltage: The negative common-mode voltage limit is one diode drop above the negative supply voltage. Exceeding this limit on either input will result in an output phase reversal. The positive common-mode limit is typically 1V below the positive supply voltage. No output phase reversal will occur if this limit is exceeded by either input.

Output Voltage Swing vs I_{SET}: For a desired output voltage swing the value of the minimum load depends on the positive and negative output curent capability of the op amp. The maximum available positive output current, (I_{CL+}), of the device increases with I_{SET} whereas the **negative output current (I_{CL}) also increases with I_{SET}.** *Figure 1* illustrates the above.

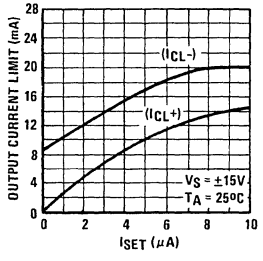


FIGURE 1. Output Current Limit vs I_{SET}

Input Capacitance: The input capacitance, C_{IN}, of the LM146 is approximately 2 pF; any stray capacitance, C_S, (due to external circuit circuit layout) will add to C_{IN}. When resistive or active feedback is applied, an additional pole is added to the open loop frequency response of the device. For instance with resistive feedback *(Figure 2)*, this pole occurs at $1/2\pi$ (R1||R2) (C_{IN} + C_S). Make sure that this pole occurs at least 2 octaves beyond the expected −3 dB frequency corner of the closed loop gain of the amplifier; if not, place a lead capacitor in the feedback such that the time constant of this capacitor and the resistance it parallels is equal to the $R_I(C_S + C_{IN})$, where R_I is the input resistance of the circuit.

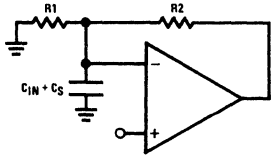


FIGURE 2

Temperature Effect on the GBW: The GBW (gain bandwidth product), of the LM146 is directly proportional to I_{SET} and inversely proportional to the absolute temperature. When using resistors to set the bias current, I_{SET}, of the device, the GBW product will decrease with increasing temperature.

Isolation Between Amplifiers: The LM146 die is isothermally layed out such that crosstalk between *all 4* amplifiers is in excess of −105 dB (DC). Optimum isolation (better than −110 dB) occurs between amplifiers A and D, B and C; that is, if amplifier A dissipates power on its output stage, amplifier D is the one which will be affected the least, and vice versa. Same argument holds for amplifiers B and C.

LM146 Typical Performance Summary: The LM146 typical behavior is shown in *Figure 3*. The device is fully predictable. As the set current, I_{SET}, increases, the speed, the bias current, and the supply current increase while the noise power decreases proportionally and the V_{OS} remains constant. The usable GBW range of the op amp is 10 kHz to 3.5–4 MHz.

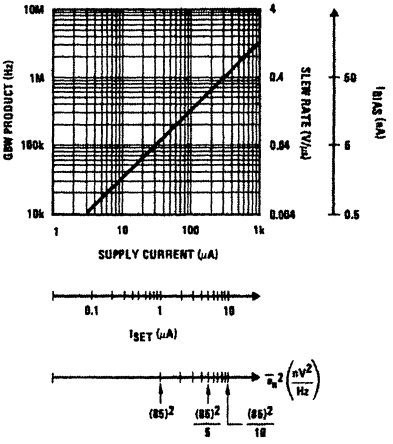


FIGURE 3. LM146 Typical Characteristics

Low Power Supply Operation: The quad op amp operates down to ±1.3V supply. Also, since the internal circuitry is biased through programmable current sources, no degradation of the device speed will occur.

Speed vs Power Consumption: LM146 vs LM4250 (single programmable). Through *Figure 4*, we observe that the LM146's power consumption has been optimized for GBW products above 200 kHz, whereas the LM4250 will reach a GBW of no more than 300 kHz, for GBW products below 200 kHz, the LM4250 will consume less.

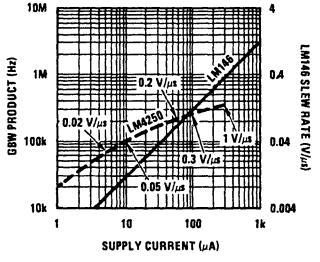
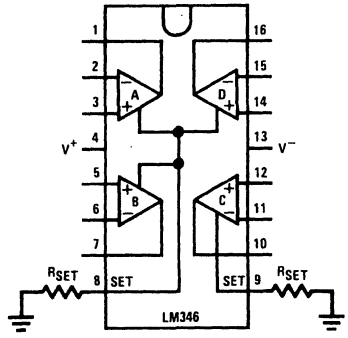


FIGURE 4. LM146 vs LM4250

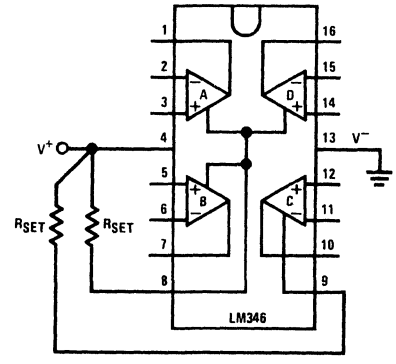
Typical Applications

Dual Supply or Negative Supply Biasing



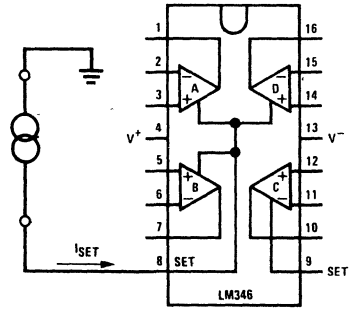
$$I_{SET} \simeq \frac{|V^-| - 0.6V}{R_{SET}}$$

Single (Positive) Supply Biasing

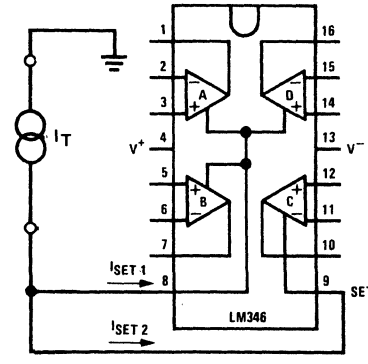


$$I_{SET} \simeq \frac{V^+ - 0.6V}{R_{SET}}$$

Current Source Biasing



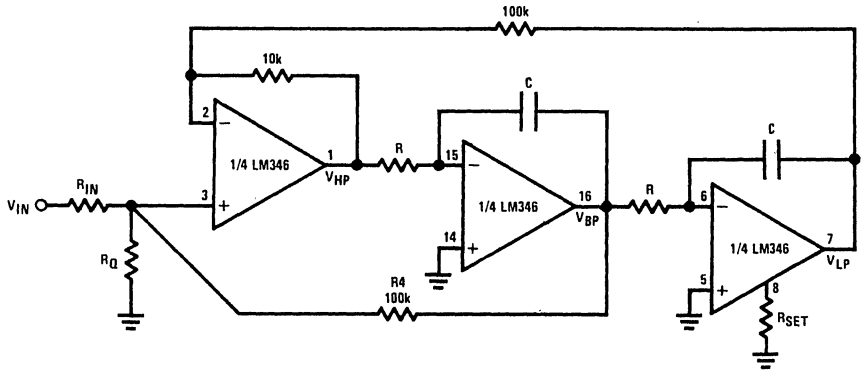
Biasing all 4 Amplifiers with Single Current Source



$$I_T = I_{SET\,1} + I_{SET\,2}$$

Active Filters Applications

Basic (Non-Inverting "State Variable") Active Filter Building Block



- The LM146 quad programmable op amp is especially suited for active filters because of their adequate GBW product and low power consumption.

Need to know desired: f_o = center frequency measured at the BP output
Q_o = quality factor measured at the BP output
H_o = gain at the output of interest (BP or HP or LP or all of them)

▲ Relation between different gains: $H_{o(BP)} = 0.316 \times Q_o \times H_{o(LP)}$; $H_{o(LP)} = 10 \times H_{o(HP)}$

▲ $R \times C = \dfrac{5.033 \times 10^{-2}}{f_o}$ (sec)

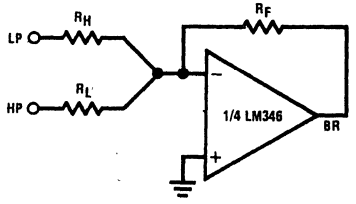
▲ For BP output: $R_Q = \left(\dfrac{3.478\,Q_o - H_{o(BP)}}{10^5} - \dfrac{H_{o(BP)}}{10^5 \times 3.478 \times Q_o}\right)^{-1}$; $R_{IN} = \dfrac{\left(\dfrac{3.478\,Q_o}{H_{o(BP)}} - 1\right)}{\dfrac{1}{R_Q} + 10^{-5}}$

▲ For HP output: $R_Q = \dfrac{1.1 \times 10^5}{3.478\,Q_o\,(1.1 - H_{o(HP)}) - H_{o(HP)}}$; $R_{IN} = \dfrac{\dfrac{1.1}{H_{o(HP)}} - 1}{\dfrac{1}{R_Q} + 10^{-5}}$

Note. All resistor values are given in ohms.

▲ For LP output: $R_Q = \dfrac{11 \times 10^5}{3.478\,Q_o\,(11 - H_{o(LP)}) - H_{o(LP)}}$; $R_{IN} = \dfrac{\dfrac{11}{H_{o(LP)}} - 1}{\dfrac{1}{R_Q} + 10^{-5}}$

▲ For BR (notch) output: Use the 4th amplifier of the LM146 to sum the LP and HP outputs of the basic filter.



$$\sqrt{\frac{R_H}{R_L}} = 0.316\ \frac{f_{notch}}{f_o}$$

Determine R_F according to the desired gains: $H_{o(BR)}\big|_{f << f_{notch}} = \dfrac{R_F}{R_L} H_{o(LP)}$, $H_{o(BR)}\big|_{f >> f_{notch}} = \dfrac{R_F}{R_H} H_{o(HP)}$

- **Where to use amplifier C:** Examine the above gain relations and determine the dynamics of the filter. Do not allow slew rate limiting in any output (V_{HP}, V_{BP}, V_{LP}), that is:

$$V_{IN(peak)} < 63.66 \times 10^3 \times \frac{I_{SET}}{10\,\mu A} \times \frac{1}{f_o \times H_o}\ \text{(Volts)}$$

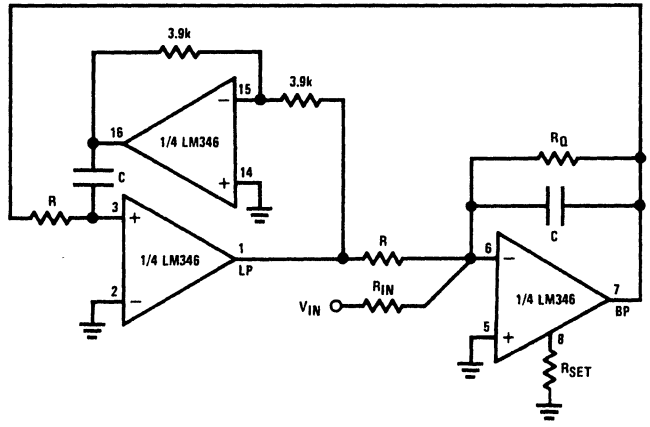
If necessary, use amplifier C, biased at higher I_{SET}, where you get the largest output swing.

Deviation from Theoretical Predictions: Due to the finite GBW products of the op amps the f_o, Q_o will be slightly different from the theoretical predictions.

$$f_{real} \simeq \frac{f_o}{1 + \dfrac{2\,f_o}{GBW}}\ ,\ Q_{real} \simeq \frac{Q_o}{1 - \dfrac{3.2\,f_o \times Q_o}{GBW}}$$

Active Filters Applications (Continued)

A Simple-to-Design BP, LP Filter Building Block



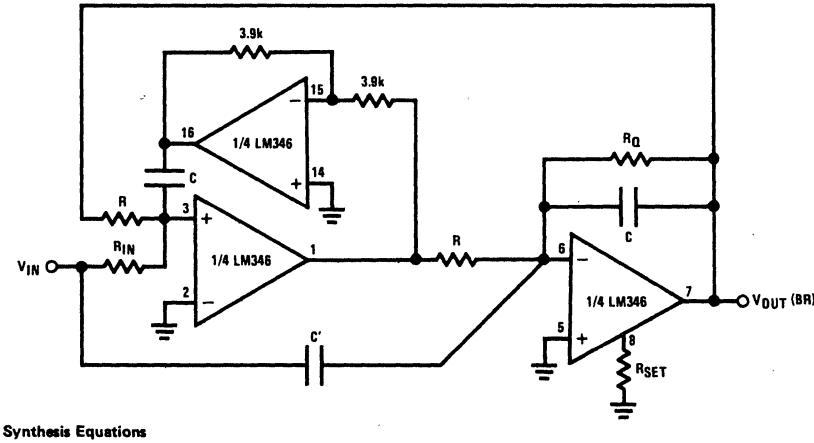
- If resistive biasing is used to set the LM346 performance, the Q_o of this filter building block is nearly insensitive to the op amp's GBW product temperature drift; it has also better noise performance than the state variable filter.

Circuit Synthesis Equations

$$H_{o(BP)} = Q_o H_{o(LP)}; R \times C = \frac{0.159}{f_o}; R_Q = Q_o \times R; R_{IN} = \frac{R_Q}{H_{o(BP)}} = \frac{R}{H_{o(LP)}}$$

- For the eventual use of amplifier C, see comments on the previous page.

A 3-Amplifier Notch Filter (or Elliptic Filter Building Block)



Circuit Synthesis Equations

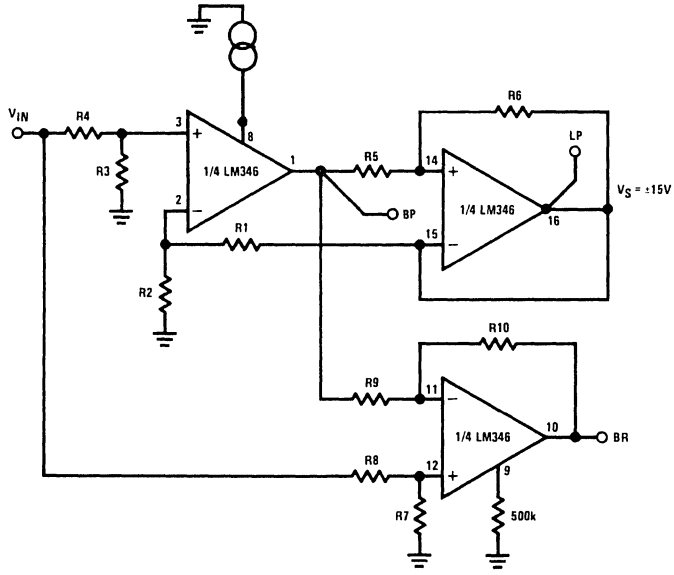
$$R \times C = \frac{0.159}{f_o}; R_Q = Q_o \times R; R_{IN} = \frac{0.159 \times f_o}{C' \times f^2_{notch}}$$

$$H_{o(BR)}\Big|_{f << f_{notch}} = \frac{R}{R_{IN}} \quad H_{o(BR)}\Big|_{f >> f_{notch}} = \frac{C'}{C}$$

- For nothing but a notch output: $R_{IN} = R$, $C' = C$.

Active Filters Applications (Continued)

Capacitorless Active Filters (Basic Circuit)

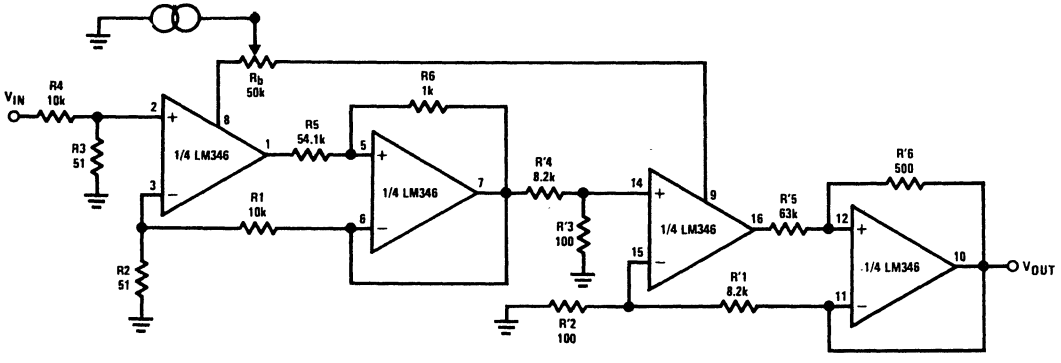


- This is a BP, LP, BR filter. The filter characteristics are created by using the tunable frequency response of the LM346.
- **Limitations:** $Q_o < 10$, $f_o \times Q_o < 1.5$ MHz, output voltage should not exceed $V_{peak(out)} \leq \frac{63.66 \times 10^3}{f_o} \times \frac{I_{SET}\ (\mu A)}{10\ \mu A}$ (V)
- *Design equations:* $a = \frac{R6 + R5}{R6}$, $b = \frac{R2}{R1 + R2}$, $c = \frac{R3}{R3 + R4}$, $d = \frac{R7}{R8 + R7}$, $e = \frac{R10}{R9 + R10}$, $f_{o(BP)} = f_u \sqrt{\frac{b}{a}}$, $H_{o(BP)} = a \times c$,

  $H_{o(LP)} = \frac{c}{b}$, $Q_o = \sqrt{a \times b}$

  $f_{o(BR)} = f_{o(BP)} \left(1 - \frac{c}{b}\right) \simeq f_{o(BP)}$ ($C << 1$) provided that $d = H_{o(BP)} \times e$, $H_{o(BR)} = \frac{R10}{R9}$.
- Advantage: f_o, Q_o, H_o can be independently adjusted; that is, the filter is extremely easy to tune.
- Tuning procedure (ex. BP tuning)
  1. Pick up a convenient value for b; ($b < 1$)
  2. Adjust Q_o through R5
  3. Adjust $H_{o(BP)}$ through R4
  4. Adjust f_o through R_{SET}

A 4th Order Butterworth Low Pass Capacitorless Filter

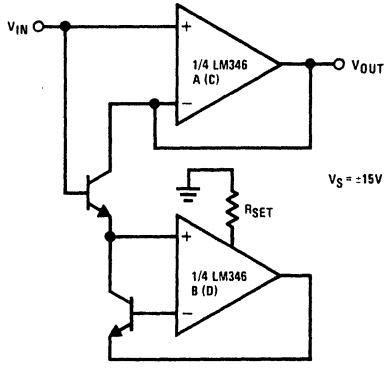


Ex: $f_c = 20$ kHz, H_o (gain of the filter) = 1, $Q_{o1} = 0.541$, $Q_{o2} = 1.306$.

- Since for this filter the GBW product of all 4 amplifiers has been designed to be the same (~1 MHz) only one current source can be used to bias the circuit. Fine tuning can be further accomplished through R_b.

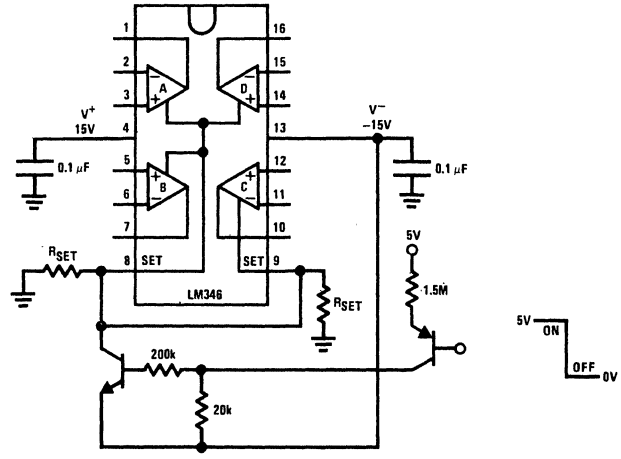
Miscellaneous Applications

A Unity Gain Follower with Bias Current Reduction



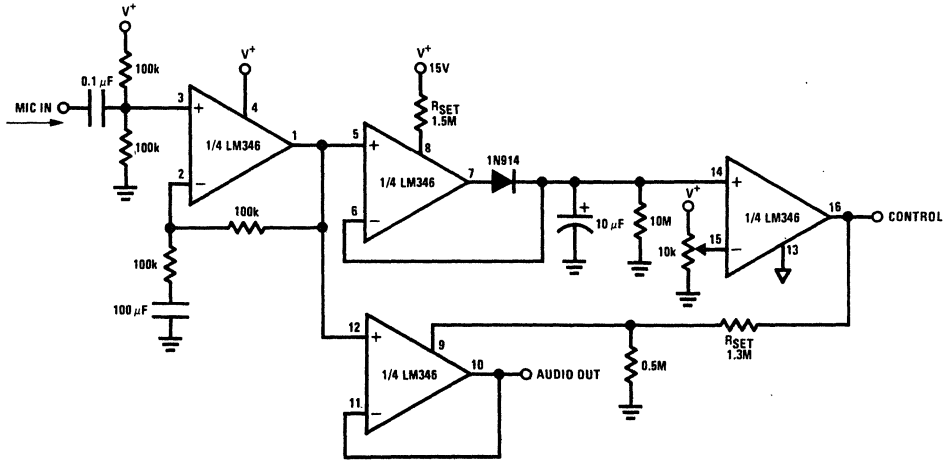
- For better performance, use a matched NPN pair.

Circuit Shutdown



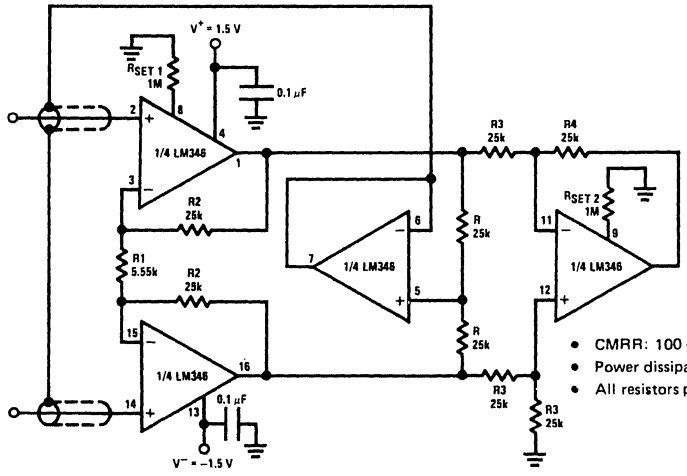
- By pulling the SET pin(s) to V⁻ the op amp(s) shuts down and its output goes to a high impedance state. According to this property, the LM346 can be used as a very low speed analog switch.

Voice Activated Switch and Amplifier



Miscellaneous Applications (Continued)

X10 Micropower Instrumentation Amplifier with Buffered Input Guarding



- CMRR: 100 dB (typ)
- Power dissipation: 0.4 mW
- All resistors part of RA201 array

HARRIS

LM148 Series Quad 741 Op Amps

LM148/LM348 quad 741 op amps

General Description

The LM148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

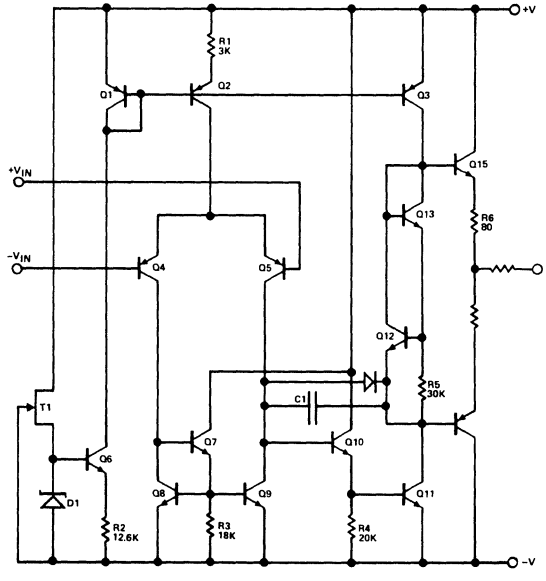
The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Features

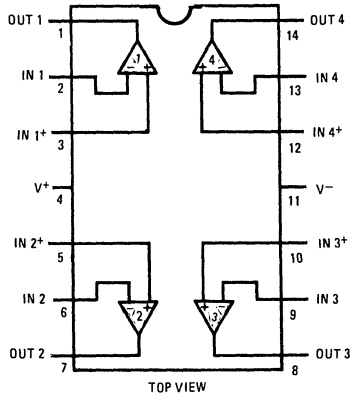
- 741 op amp operating characteristics
- Low cupply current drain — 4.5 mA/Package
- Class AB output stage-no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage — 1 mV
- Low input offset current — 15 nA
- Low input bias current — 60 nA
- Gain bandwidth product LM148 (unity gain) — 3.5 MHz
- High degree of isolation between amplifiers — 120 dB
- Overload protection on all outputs

Schematic and Connection Diagrams

Section 11 for Packaging



Dual-In-Line Package



Order Number LM148J, LM348J

Order Number LM348N

Absolute Maximum Ratings

	LM148	LM348
Supply Voltage	±22V	±18V
Differential Input Voltage	$\pm V_S$	$\pm V_S$
Input Voltage	$\pm V_S$	$\pm V_S$
Output Short Circuit Duration (Note 1)	Continuous	Continuous
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}), (Note 2)		
Molded DIP (N) P_d	—	500 mW
θ_{jA}	—	150°C/W
Cavity DIP (J) P_d	900 mW	900 mW
θ_{jA}	100°C/W	100°C/W
Maximum Junction Temperature (T_{jMAX})	150°C	100°C
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$	$0°C \leq T_A \leq +70°C$
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C	300°C

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LM148			LM348			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage ($R_S \leq 10$ kΩ)	Unless Otherwise Specified: $V_S = \pm 15V$, $T_A = +25°C$		1.0	5.0		1.0	6.0	mV
Input Offset Current			4	25		4	50	nA
Input Bias Current			30	100		30	200	nA
Input Resistance		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers			2.4	3.6		2.4	4.5	mA
Large Signal Voltage Gain	V_{OUT} 0 ±10V, $R_L \geq 2$ kΩ	50	160		25	160		V/mV
Amplifier to Amplifier Coupling	f = 1 Hz to 20 kHz (Input Referred) See Crosstalk Test Circuit		−120			−120		dB
Small Signal Bandwidth			1.0			1.0		MHz
			4.0			4.0		MHz
Phase Margin			60			60		degrees
			60			60		degrees
Slew Rate			0.5			0.5		V/μs
			2.0			2.0		V/μs
Output Short Circuit Current			25			25		mA
Input Offset Voltage ($R_S \leq 10$ kΩ)	Unless Otherwise Specified: $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM148), $0°C \leq T_A \leq +70°C$ (LM348), $V_{OUT} = \pm 10V$, $R_L > 2$ kΩ, $R_L > 2$ kΩ			6.0			7.5	mV
Input Offset Current				75			100	nA
Input Bias Current				325			400	nA
Large Signal Voltage Gain		25			15			V/mV
Output Voltage Swing	$R_L = 10$ kΩ	±12	±13		±12	±13		V
	$R_L = 2$ kΩ	±10	±12		±10	±12		V
Input Voltage Range		±12			±12			V
Common-Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection	$R_S \leq 10$ kΩ	77	96		77	96		dB

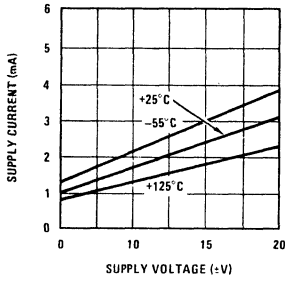
Note 1: Any of the amplifier outputs can be shorted to ground indefinitely; however more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

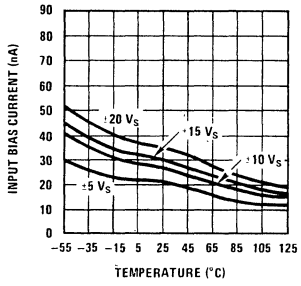
Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.

Typical Performance Characteristics

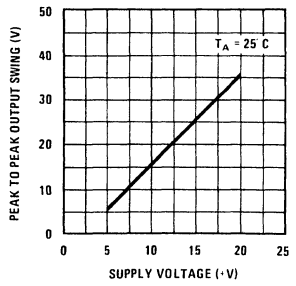
Supply Current



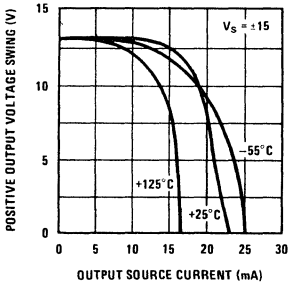
Input Bias Current



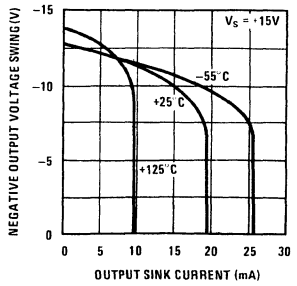
Voltage Swing



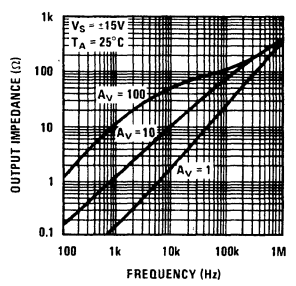
Positive Current Limit



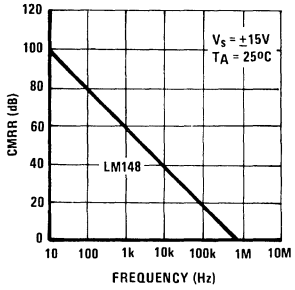
Negative Current Limit



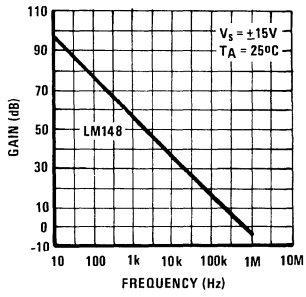
Output Impedance



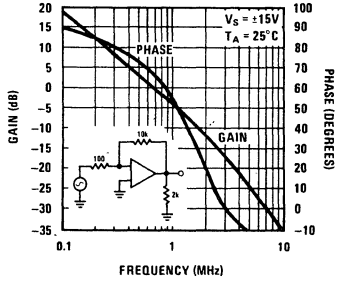
Common-Mode Rejection Ratio



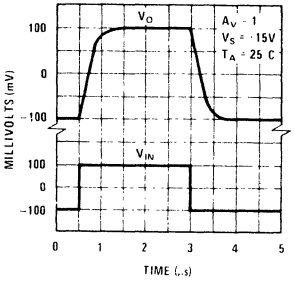
Open Loop Frequency Response



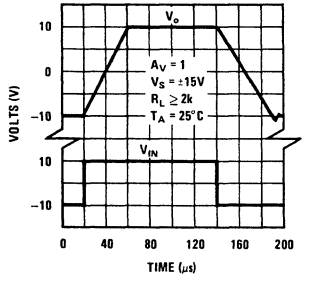
Bode Plot LM148



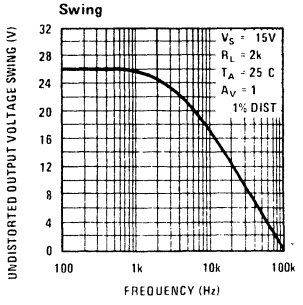
Small Signal Pulse Response (LM148)



Large Signal Pulse Response (LM148)

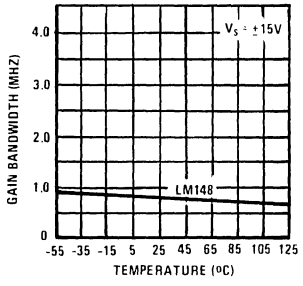


Undistorted Output Voltage Swing

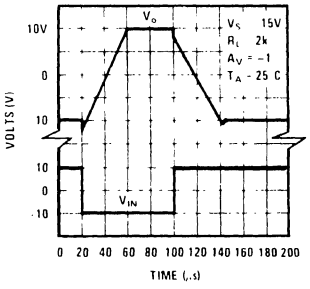


Typical Performance Characteristics (continued)

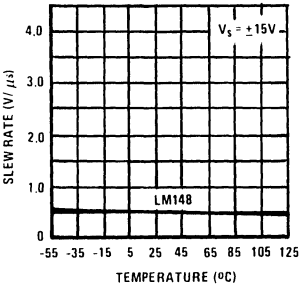
Gain Bandwidth



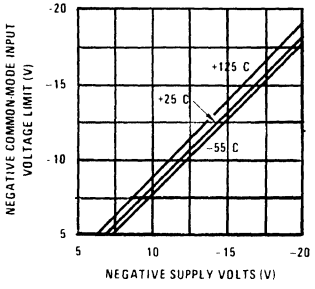
Inverting Large Signal Pulse Response (LM148)



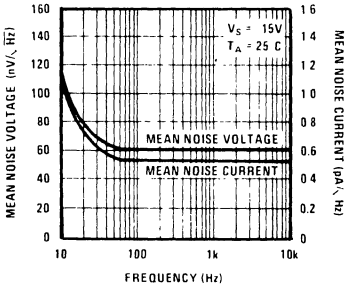
Slew Rate



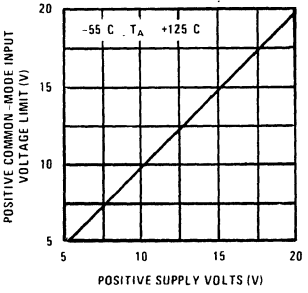
Negative Common-Mode Input Voltage Limit



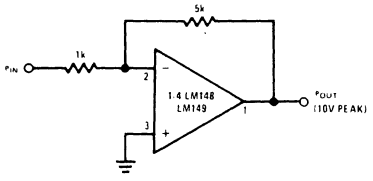
Input Noise Voltage and Noise Current

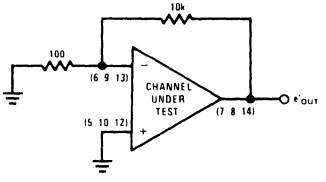


Positive Common-Mode Input Voltage Limit



Cross Talk Test Circuits



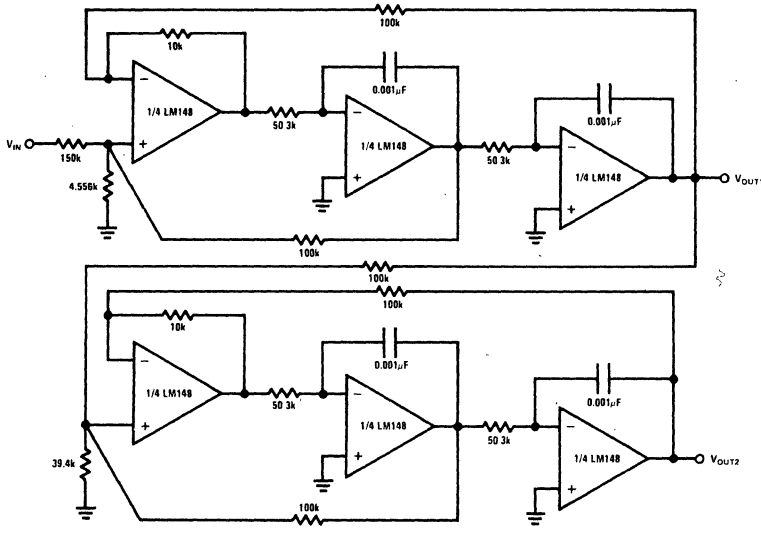


$$\text{Crosstalk} = -20 \log \frac{e'_{OUT}}{101 \times e_{OUT}} \text{ (dB)}$$

$V_S = \pm 15V$

Typical Applications — LM148 (Continued)

A 1 kHz 4 Pole Butterworth

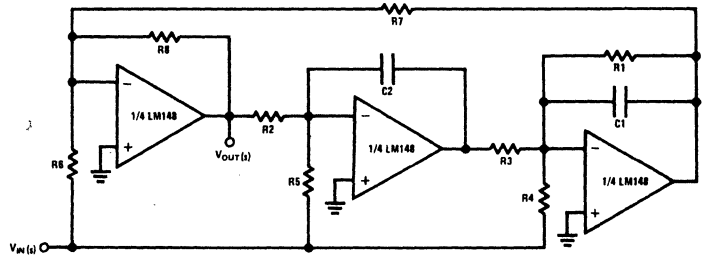


Use general equations, and tune each section separately

$Q_{1stSECTION} = 0.541$, $Q_{2ndSECTION} = 1.306$

The response should have 0 dB peaking

A 3 Amplifier Bi-Quad Notch Filter



$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}}, \quad f_o = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}}, \quad f_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

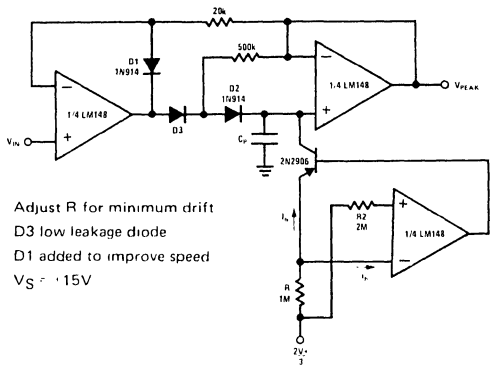
Necessary condition for notch: $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex: $f_{NOTCH} = 3$ kHz, $Q = 5$, R1 = 270k, R2 = R3 = 20k, R4 = 27k, R5 = 20k, R6 = R8 = 10k, R7 = 100k, C1 = C2 = 0.001μF

Better noise performance than the state-space approach

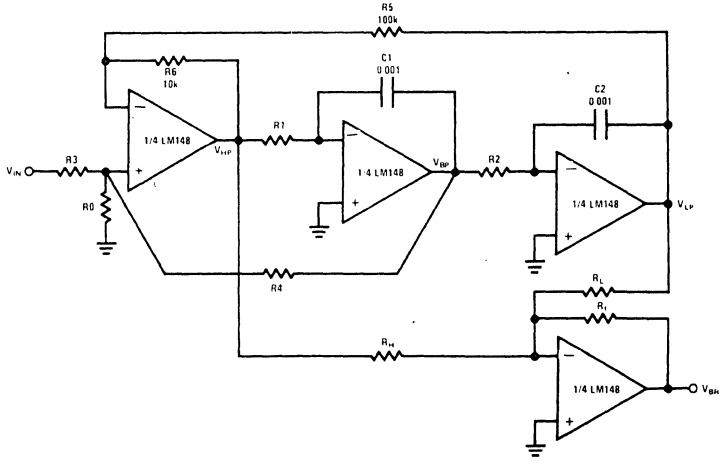
Typical Applications — LM148 (Continued)

Low Drift Peak Detector with Bias Current Compensation



Adjust R for minimum drift
D3 low leakage diode
D1 added to improve speed
$V_S = \pm 15V$

Universal State-Space Filter



Tune Q through R0,
For predictable results: $f_O\ Q \leq 4 \times 10^4$
Use Band Pass output to tune for Q

$$\frac{V_{(s)}}{V_{IN(s)}} = \frac{N(s)}{D(s)},\quad D(s) = S^2 + \frac{S\omega_o}{Q} + \omega_o{}^2$$

$$N_{HP(s)} = S^2 H_{OHP},\ N_{BP(s)} = \frac{-S\omega_O H_{OBP}}{Q} \qquad N_{LP} = \omega_o{}^2 H_{OLP}$$

$$f_o = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\quad\sqrt{\frac{1}{t1\,t2}},\quad t_1 = R_1C_1,\quad Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right)\left(\frac{R6}{R5}\ \frac{t_1}{t_2}\right)^{1/2}$$

$$f_{NOTCH} = \frac{1}{2\pi}\left(\frac{R_H}{R_L t_1 t_2}\right)^{1/2},\quad H_{OHP} = \frac{1 + R6|R5}{1 + R3|R0 + R3|R4},\quad H_{OBP} = \frac{1 + R4|R3 + R4|R0}{1 + R3|R0 + R3|R4}$$

$$H_{OLP} = \frac{1 + R5|R6}{1 + R3|R0 + R3|R4}$$

Application Hints

The LM148 series are quad low power 741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the 741 op amp. In those applications where 741 op amps have been employed, the LM148 series op amps can be employed directly with no change in circuit performance.

The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

For input voltages which greatly exceed the operating supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current.

Like the LM741, these amplifiers can easily drive a 100 pF capacitive load throughout the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier, a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

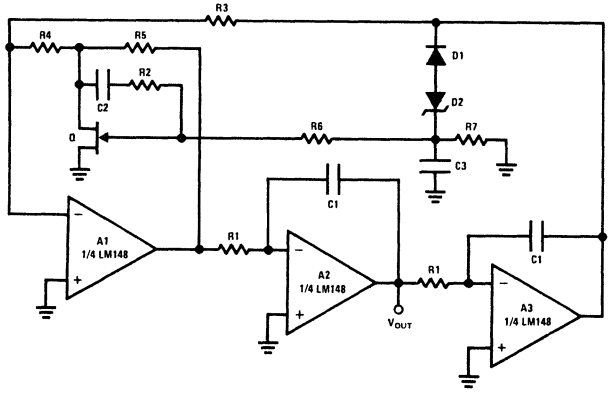
The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor shoud be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications — LM148

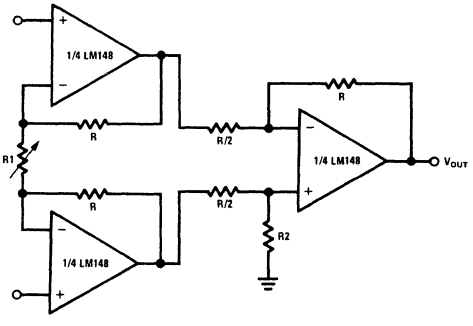
One Decade Low Distortion Sinewave Generator



$$f = \frac{1}{2\pi R1C1} \times \sqrt{K}\ ,\ K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right),\ r_{DS} \cong \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

f_{MAX} = 5 kHz, THD ≤ 0.03%
R1 = 100k pot., C1 = 0.0047μF, C2 = 0.01μF, C3 = 0.1μF, R2 = R6 = R7 = 1M, R3 = 5.1k, R4 = 12Ω, R5 = 240Ω, Q = NS5102, D1 = 1N914, D2 = 3.6V avalanche diode (ex. LM103), V_S = ±15V
A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

Low Cost Instrumentation Amplifier

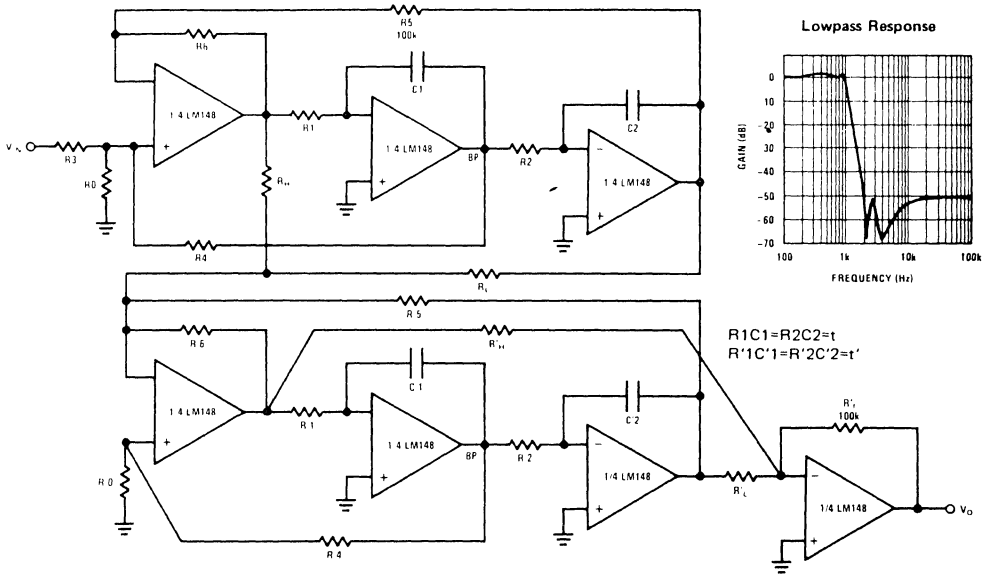


$$V_{OUT} = 2\left(\frac{2R}{R1} + 1\right),\ V_S^- - 3V \le V_{IN\ CM} \le V_S^+ - 3V,$$

V_S = ±15V
R = R2, trim R2 to boost CMRR

Typical Applications — LM148 (Continued)

A 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)



Lowpass Response

f_C = 1 kHz, f_S = 2 kHz, f_P = 0.543, f_Z = 2.14, Q = 0.841, f'_P = 0.987, f'_Z = 4.92, Q' = 4.403, normalized to ripple BW

$$f_P = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}} \times \frac{1}{t}, f_Z = \frac{1}{2\pi}\sqrt{\frac{R_H}{R_L}} \times \frac{1}{t}, Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right) \times \sqrt{\frac{R6}{R5}}, Q' = \sqrt{\frac{R'6}{R'5}} \frac{1 + R'4|R'0}{1 + R'6|R'5 + R'6|R_P}$$

$$R_P = \frac{R_H R_L}{R_H + R_L}$$

Use the BP outputs to tune Q, Q', tune the 2 sections separately

R1 = R2 = 92.6k, R3 = R4 = R5 = 100k, R6 = 10k, R0 = 107.8k, R_L = 100k, R_H = 155.1k,

R'1 = R'2 = 50.9k, R'4 = R'5 = 100k, R'6 = 10k, R'0 = 5.78k, R'_L = 100k, R'_H = 248.12k, R'f = 100k. All capacitors are 0.001μF.

HARRIS

LM148A Series Quad 741 Type Op Amps

LM148A/LM348A Quad 741 Type Op Amps

General Description

The LM148A series is a quad 741 type operational amplifier. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide DC and AC performance superior to the familiar 741 and LM148 operational amplifiers. While maintaining low supply current, these devices offer speed and bandwidth specifications comparable to high performance type op amps. Excellent isolation between amplifiers has been ensured by employing the Harris DI process coupled with layout techniques which minimize thermal coupling.

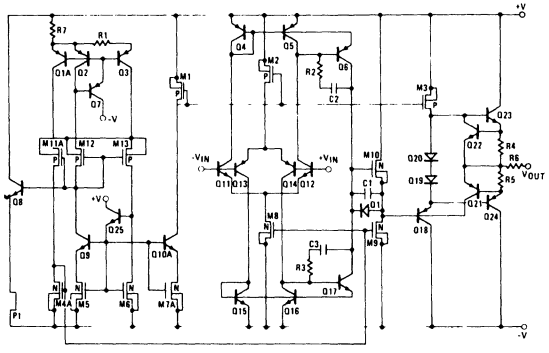
The LM148A can be used in virtually all LM148 or LM149 applications. Where amplifier matching or high packing density is required, these devices can be used in place of multiple single or dual type op amps.

Features

- High performance operating characteristics
- Low supply current → P_{DISS} 140 mW/Package
- Class AB output stage-no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage 0.3 mV
- Low input offset current 30 nA
- Low input bias current 130 nA
- Gain bandwidth product LM148A (unity gain) 8 MHz
- High degree of isolation between amplifiers 120 dB
- Overload protection on all outputs

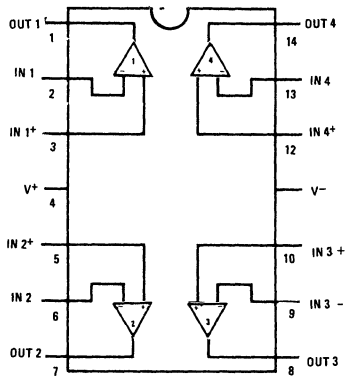
Schematic and Connection Diagrams

Section 11 for Packaging



Dual-In-Line Package

TOP VIEW



Order Number LM148AJ, LM348AJ

Order Number LM348AN

Absolute Maximum Ratings (Note 1)

	LM148A	LM348A
Supply Voltage	±20V	±20V
Differential Input Voltage	$\pm V_s$	$\pm V_s$
Input Voltage	$\pm V_s$	$\pm V_s$
Output Short Circuit Duration (Note 1)	Continuous	Continuous
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}), (Note 2)		
Molded DIP (N) P_d	—	500 mW
θ_{jA}	—	150°C/W
Cavity DIP (D) (J) P_d	900 mW	900 mW
θ_{jA}	100°C/W	100°C/W
Maximum Junction Temperature (T_{jMAX})	150°C	100°C
Operating Temperature Range	$-55°C \leq T_A \leq +125°C$	$0°C \leq T_A \leq +70°C$
Storage Temperature Range	-65° to +150°C	-65°C to 150°C
Lead Temperature (Soldering, 60 seconds)	200°C	300°C

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LM148A			LM348A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage ($R_s \leq 10$ kΩ)	Unless Otherwise Specified: $V_s = \pm 15V$		.3	3.0		.5	4.0	mV
Input Offset Current	T_A = +25°C		15	25		30	50	nA
Input Bias Current			75	100		130	300	nA
Input Resistances			.5			.5		MΩ
Supply Current All Amplifiers				7.5			7.5	mA
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 2$ kΩ	100	250		75	250		V/mV
Amplifier to Amplifier Coupling	f = 1 Hz to 20 kHz (Input Referred) See Crosstalk Test Circuit		-108			-108		dB
Small Signal Bandwidth			8			8		MHz
Phase Margin			40			40		degrees
Slew Rate		±1	±4		±1	±4		V/μs
Output Short Circuit Current			25			25		mA
Input Offset Voltage ($R_s \leq 10$ kΩ)	Unless Otherwise Specified: $V_s = \pm 15V$			3.5			4.5	mV
Input Offset Current	$-55°C \leq T_A \leq +125°C$ (LM148A)			75			100	nA
Input Bias Current	$0°C \leq T_A \leq +70°C$ (LM348A)			325			400	nA
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$	100			75			V/mV
Output Voltage Swing	R_L = 10 kΩ	±12	±13		±12	±13		V
	R_L = 2 kΩ	±10	±12		±10	±12		V
Input Voltage Range		±12			±12			V
Common-Mode Rejection Ratio	$R_s \leq 10$ kΩ	80	90		80	90		dB
Supply Voltage Rejection	$R_s \leq 10$ kΩ	80	90		80	90		dB

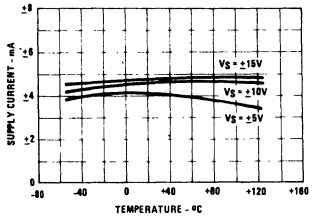
Note 1: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

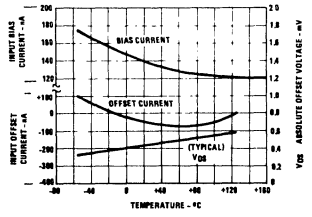
Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.

Typical Performance Characteristics

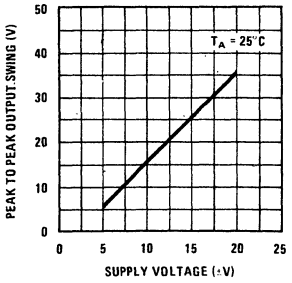
Power Supply Current vs Temperature and Supply Voltage



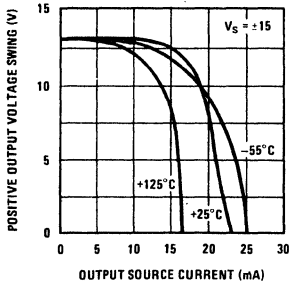
Offset Voltage Input Bias and Offset Current vs Temperature



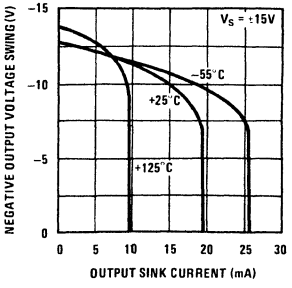
Voltage Swing



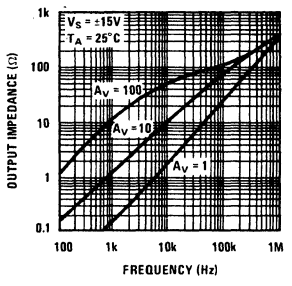
Positive Current Limit



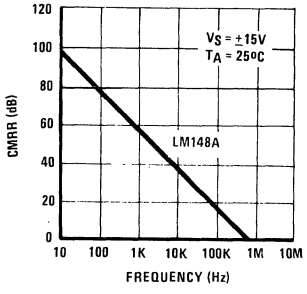
Negative Current Limit



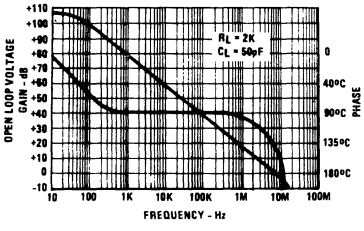
Output Impedance



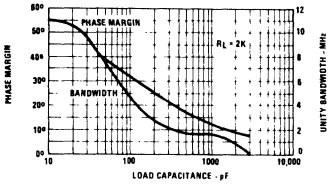
Common-Mode Rejection Ratio



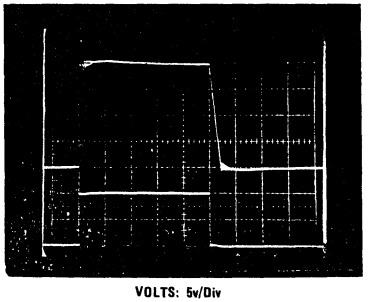
Open Loop Frequency Response



Small Signal Bandwidth and Phase Margin vs Load Capacitance



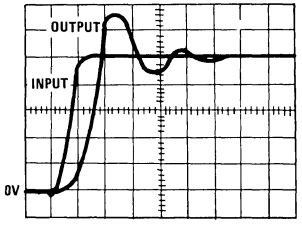
Large Signal Pulse Response (LM148A)



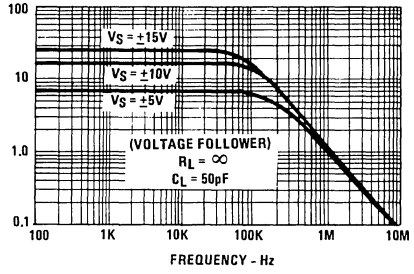
VOLTS: 5v/Div
TIME: 20 μs/Div

Typical Performance Characteristics (Continued)

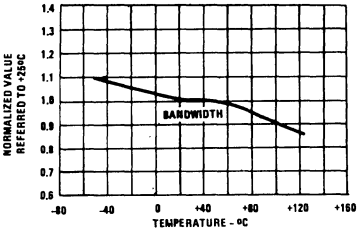
Small Signal Response Circuit
(Volts: 10mV/Div., Time: 50ns/Div.)



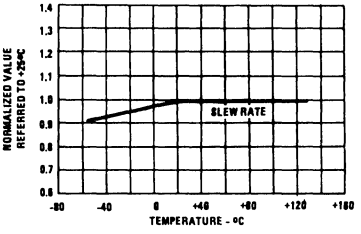
Undistorted Output Voltage Swing



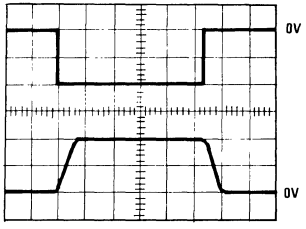
Normalized Gain Bandwith VS. Temperature



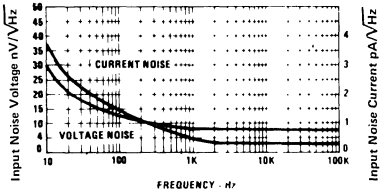
Normalized Gain Bandwidth VS. Temperature



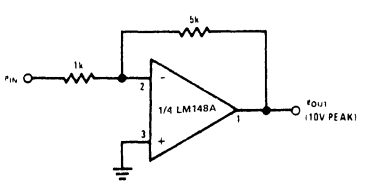
Inverting Large Signal Pulse Response (LM148A)
(Volts: 5V/Div., Time: 5 μs/Div.)

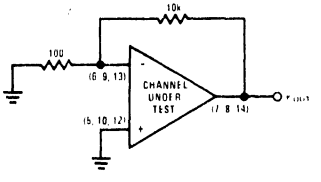


Input Noise Voltage and Noise Current



Cross Talk Test Circuits





$$\text{Crosstalk} = -20 \log \frac{e'_{OUT}}{101 \times e_{OUT}} \text{ (dB)}$$

$V_S = \pm 15V$

Application Hints

The LM148A series are quad low power 741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familar, easy to use operating characteristics of the 741 op amp. In those applications where 741 op amps have been employed, the LM148A series op amps can be employed directly with no change in circuit performance.

The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

For input voltages which greatly exceed the operating supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current.

Like the LM741, these amplifiers can easily drive a 100 pF capacitive load throughout the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier, a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

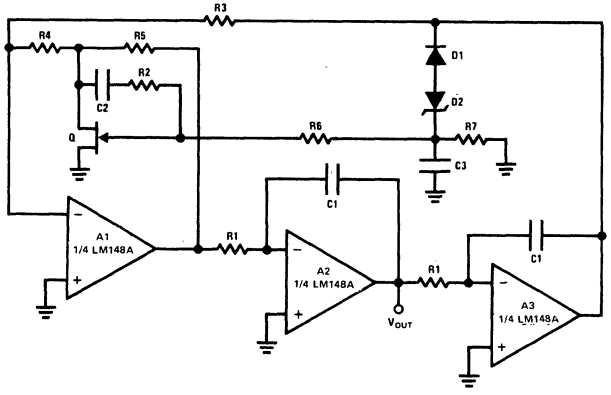
The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications — LM148A/LM348A

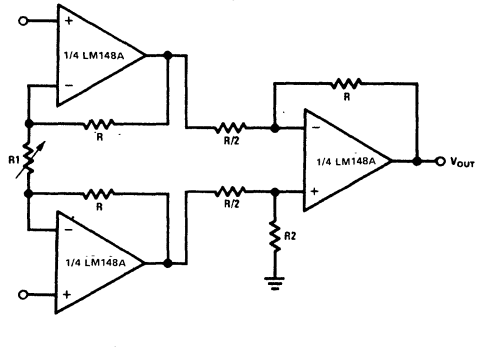
One Decade Low Distortion Sinewave Generator



$$f = \frac{1}{2\pi R1C1} \times \sqrt{K}\ ,\ K = \frac{R4R5}{R3}\left(\frac{1}{r_{DS}} + \frac{1}{R4} + \frac{1}{R5}\right),\ r_{DS} \cong \frac{R_{ON}}{\left(1 - \frac{V_{GS}}{V_P}\right)^{1/2}}$$

f_{MAX} = 5 kHz, THD ≤ 0.03%
R1 = 100k pot., C1 = 0.0047μF, C2 = 0.01μF, C3 = 0.1μF, R2 = R6 = R7 = 1M, R3 = 5.1k, R4 = 12Ω, R5 = 240Ω, Q = NS5102, D1 = 1N914, D2 = 3.6V avalanche diode (ex. LM103), V_S = ±15V
A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in the feedback loop of A3.

Low Cost Instrumentation Amplifier

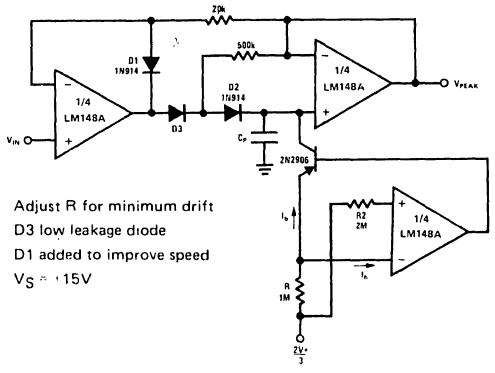


$$V_{OUT} = 2\left(\frac{2R}{R1} + 1\right),\ V_S^- - 3V \leq V_{IN\ CM} \leq V_S^+ - 3V,$$

V_S = ±15V
R = R2, trim R2 to boost CMRR

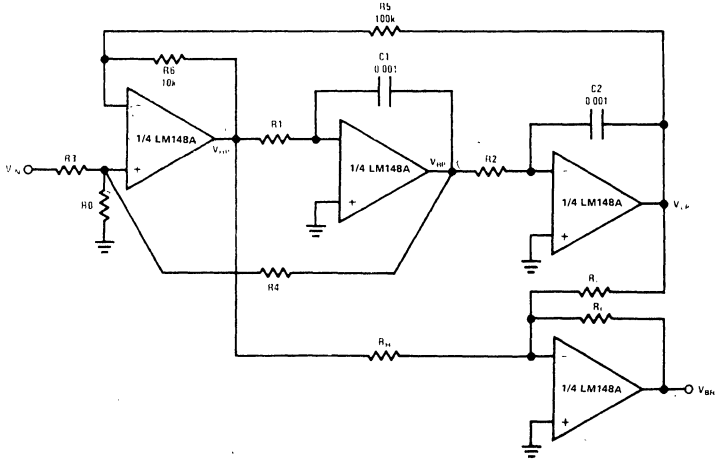
Typical Applications — LM148A/LM348A (Continued)

Low Drift Peak Detector with Bias Current Compensation



Adjust R for minimum drift
D3 low leakage diode
D1 added to improve speed
$V_S = \pm 15V$

Universal State-Space Filter



Tune Q through R0,
For predictable results. $f_O\, Q \leq 4 \times 10^4$
Use Band Pass output to tune for Q

$$\frac{V(s)}{V_{IN}(s)} = \frac{N(s)}{D(s)},\quad D(s) = S^2 + \frac{S\omega_o}{Q} + \omega_o{}^2$$

$$N_{HP(s)} = S^2 H_{OHP},\ N_{BP(s)} = \frac{S\omega_O H_{OBP}}{Q} \quad N_{LP} = \omega_o{}^2 H_{OLP}$$

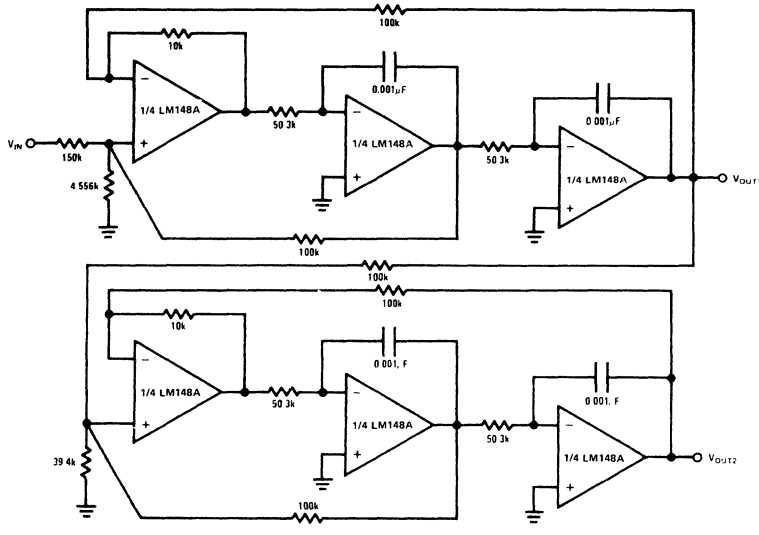
$$f_o = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}}\quad\sqrt{\frac{1}{t1t2}},\ t_i = R_iC_i,\ Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right)\left(\frac{R6}{R5}\frac{t_1}{t_2}\right)^{1/2}$$

$$f_{NOTCH} = \frac{1}{2\pi}\left(\frac{R_H}{R_L t_1 t_2}\right)^{1/2},\ H_{OHP} = \frac{1 + R6|R5}{1 + R3|R0 + R3|R4},\ H_{OBP} = \frac{1 + R4|R3 + R4|R0}{1 + R3|R0 + R3|R4}$$

$$H_{OLP} = \frac{1 + R5|R6}{1 + R3|R0 + R3|R4}$$

Typical Applications — LM148A/LM348A (Continued)

A 1 kHz 4 Pole Butterworth

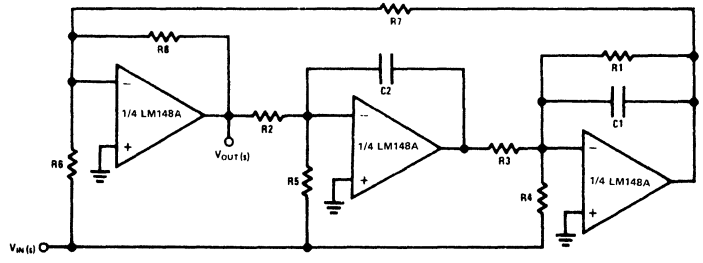


Use general equations, and tune each section separately

$Q_{1st\,SECTION} = 0.541$, $Q_{2nd\,SECTION} = 1.306$

The response should have 0 dB peaking

A 3 Amplifier Bi-Quad Notch Filter



$$Q = \sqrt{\frac{R8}{R7}} \times \frac{R1C1}{\sqrt{R3C2R2C1}}, \quad f_o = \frac{1}{2\pi}\sqrt{\frac{R8}{R7}} \times \frac{1}{\sqrt{R2R3C1C2}}, \quad f_{NOTCH} = \frac{1}{2\pi}\sqrt{\frac{R6}{R3R5R7C1C2}}$$

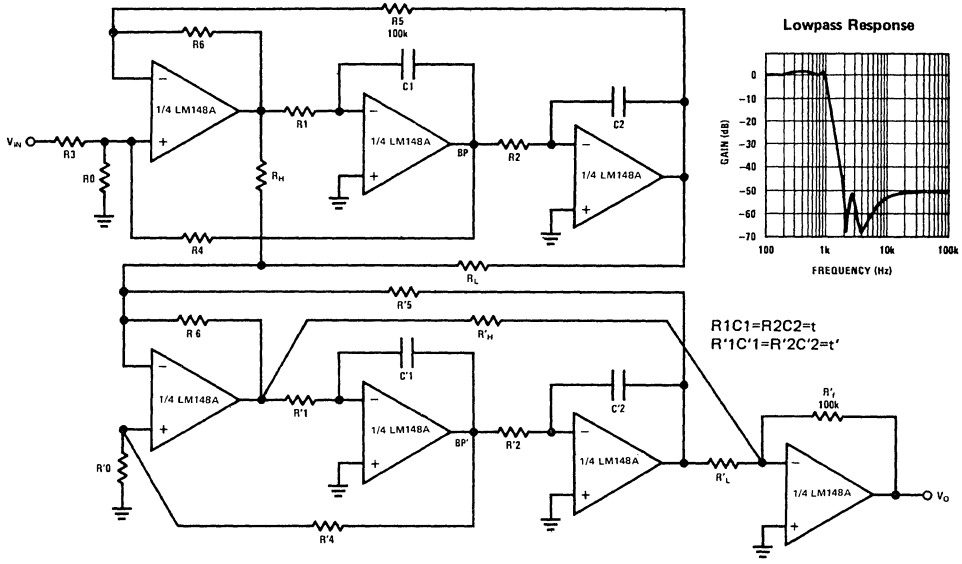
Necessary condition for notch: $\frac{1}{R6} = \frac{R1}{R4R7}$

Ex: $f_{NOTCH} = 3$ kHz, $Q = 5$, R1 = 270k, R2 = R3 = 20k, R4 = 27k, R5 = 20k, R6 = R8 = 10k, R7 = 100k, C1 = C2 = 0.001μF

Better noise performance than the state-space approach

Typical Applications — LM148A/LM348A (Continued)

A 4th Order 1 kHz Elliptic Filter (4 Poles, 4 Zeros)



Lowpass Response

f_C = 1 kHz, f_S = 2 kHz, f_P = 0.543, f_Z = 2.14, Q = 0.841, f'_P = 0.987, f'_Z = 4.92, Q' = 4.403, normalized to ripple BW

$$f_P = \frac{1}{2\pi}\sqrt{\frac{R6}{R5}} \times \frac{1}{t},\ f_Z = \frac{1}{2\pi}\sqrt{\frac{R_H}{R_L}} \times \frac{1}{t},\ Q = \left(\frac{1 + R4|R3 + R4|R0}{1 + R6|R5}\right) \times \sqrt{\frac{R6}{R5}},\ Q' = \sqrt{\frac{R'6}{R'5}}\ \frac{1 + R'4|R'0}{1 + R'6|R'5 + R'6|R_P}$$

$$R_P = \frac{R_H R_L}{R_H + R_L}$$

Use the BP outputs to tune Q, Q', tune the 2 sections separately

R1 = R2 = 92.6k, R3 = R4 = R5 = 100k, R6 = 10k, R0 = 107.8k, R_L = 100k, R_H = 155.1k,

R'1 = R'2 = 50.9k, R'4 = R'5 = 100k, R'6 = 10k, R'0 = 5.78k, R'_L = 100k, R'_H = 248.12k, R'f = 100k. All capacitors are 0.001μF.

HARRIS

LM1558A/LM1458A Dual Operational Amplifier

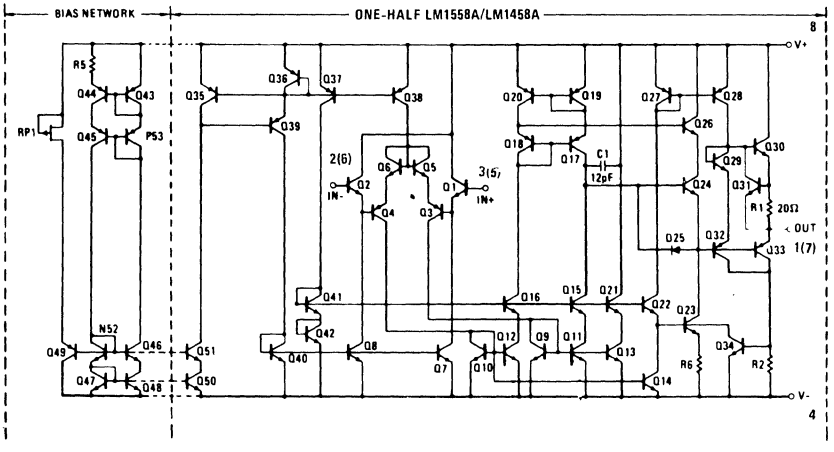
General Description

The LM1558A and the LM1458A are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, the operation is completely independent. Features include:

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Bandwidth 8 MHz
- Slew rate 5V/ μs typ
- Low-power consumption
- 8-lead TO-5 and 8-lead mini DIP
- No latch up when input common mode range is exceeded

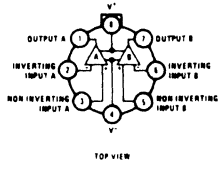
The LM1458A is identical to the LM1558A except that the LM1458A has its specifications guaranteed over the temperature range from 0°C to 70°C instead of -55°C to +125°C.

Schematic and Connection Diagrams



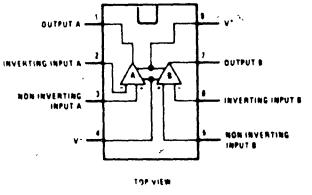
Note Numbers in parentheses are pin numbers for amplifier B

Metal Can Package



Order Number LM1558AH
or LM1458AH

Dual-In-Line Package



Order Number LM1558AJ-8 Order Number LM1458AN
or LM1458AJ-8

Absolute Maximum Ratings

Supply Voltage	LM1558A	±22V	Output Short-Circuit Duration		Indefinite
	LM1458A	±18V	Operating Temperature Range	LM1558A	-55°C to +125°C
Power Dissipation (Note 1)	LM1558AH/1458AH	500mW		LM1458A	0°C to 70°C
	LM1458AN	400mW	Storage Temperature Range		-65°C to 150°C
Differential Input Voltage		±30V	Lead Temperature (Soldering, 10 sec)		300°C
Input Voltage (Note 2)		±15V			

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LM1558A			LM1458A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, $R_S < 10\ k\Omega$		1.0	3.0		1.0	5.0	mV
Input Offset Current	$T_A = 25°C$		1.0	30		2.0	60	nA
Input Bias Current	$T_A = 25°C$		35	100		50	200	nA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Supply Current Both Amplifiers	$T_A = 25°C$, $V_S = \pm 15V$		2.5	3.0		3.0	4.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	20	40		20	40		V/mV
Input Offset Voltage	$R_S \leq 10\ k\Omega$			5.0			7.0	mV
Input Offset Current				60			100	nA
Input Bias Current				200			300	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	15			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±13	±14		±13	±14		V
	$R_L = 2\ k\Omega$	±12	±13		±12	±13		V
Input Voltage Range	$V_S = \pm 15V$	±13			±13			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	80	100		74	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	80	96		74	96		dB

Note 1: The maximum junction temperature of the LM1558A is 150°C, while that of the LM1458A is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the DIP the devices must be derated based on a thermal resistance of 187°C/W junction to ambient.

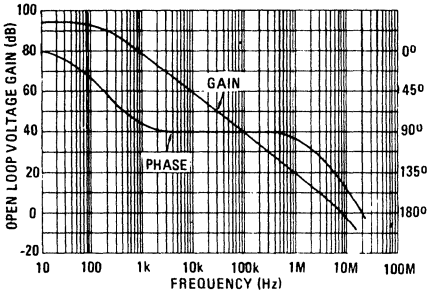
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. With the LM1458A, however, all specifications are limited to $0°C \leq T_A \leq 70°C$ and $V_S = \pm 15V$.

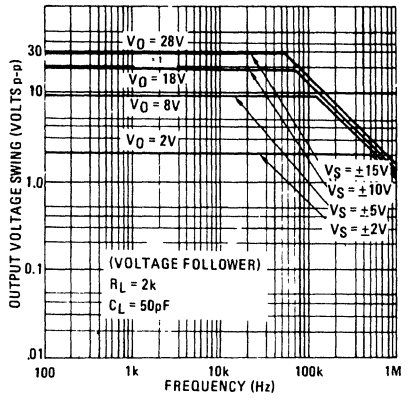
Performance Curves

V+ = +15V, V- = -15V, T_A = +25°C Unless Otherwise Stated.

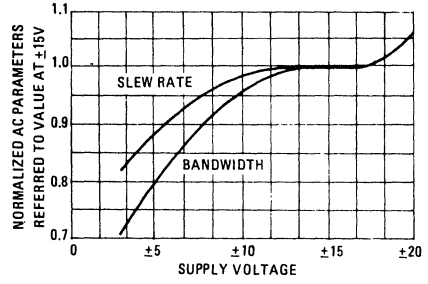
Open Loop Frequency Response



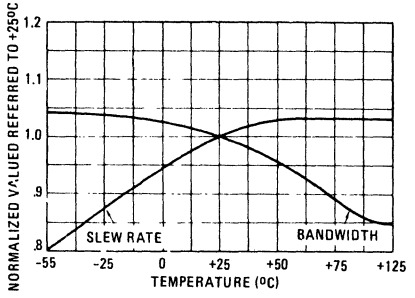
Output Voltage Swing vs Frequency



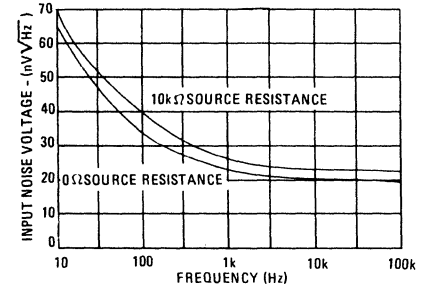
Normalized AC Parameters vs Supply Voltage



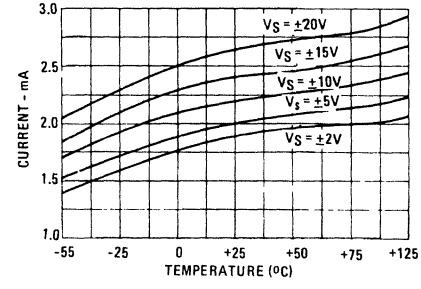
Normalized AC Parameters vs Temperature



Input Noise Voltage vs Frequency



Power Supply Current vs Temperature



LM2908 Quad Op Amps

General Description

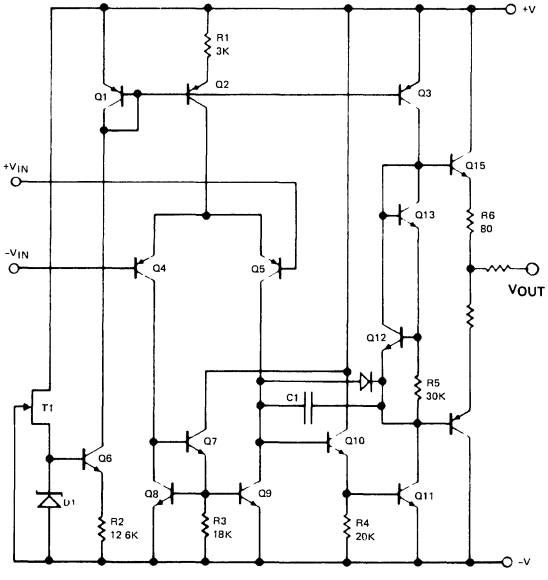
The LM2908 consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics similar to those of the familiar 741 operational amplifier. In addition, the total supply current of all four amplifiers is comparable to the supply current of a single 741 type op amp. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

The LM2908 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Features

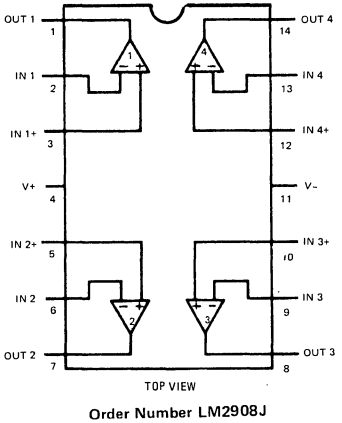
- 741 op amp operating characteristics
- Low supply current drain — 4.0mA/Package
- Class AB output stage-no crossover distortion
- Pin compatible with the LM348
- Low input offset voltage — 10mV
- Low input offset current — 200nA
- Low input bias current — 250nA
- Gain bandwidth product (unity gain) — 3.5 MHz
- High degree of isolation between amplifiers — 120 dB
- Overload protection on all outputs

Schematic and Connection Diagrams



Section 11 for Packaging

Dual-In-Line Package



Order Number LM2908J

Order Number LM2908N

Absolute Maximum Ratings

Supply Voltage	±18V	Maximum Junction Temperature (T_{jMAX})	150°C
Differential Input Voltage	$\pm V_S$	Operating Temperature Range	$0^oC \leq T_A \leq +70^oC$
Input Voltage	$\pm V_S$	Storage Temperature Range	−65°C to +150°C
Output Short Circuit Duration (Note 1)	Continuous	Lead Temperature (Soldering, 60 seconds)	300°C
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}), (Note 2)			
Molded DIP (N) P_d	900mW		
θ_{jA}	108°C/W		
Cavity DIP (J) P_d	900 mW		
θ_{jA}	100°C/W		

Electrical Characteristics (Note 3)

PARAMETER	CONDITIONS	LM2908 MIN	LM2908 TYP	LM2908 MAX	UNITS
Input Offset Voltage ($R_S \leq 10$ kΩ)	Unless Otherwise Specified: $V_S = \pm 15V$, $T_A = +25^oC$		6	10	mV
Input Offset Current			100	200	nA
Input Bias Current			250	500	nA
Input Resistance		0.8	2.5		MΩ
Supply Current All Amplifiers			4	7	mA
Large Signal Voltage Gain	$V_{OUT} = \pm 10V$, $R_L \geq 2$ kΩ	25	160		V/mV
Amplifier to Amplifier Coupling	f = 1 Hz to 20 kHz Input Referred		−120		dB
Small Signal Bandwidth			1.0		MHz
Phase Margin			60		degrees
Slew Rate			0.5		V/μs
Output Short Circuit Current			25		mA
Input Offset Voltage ($R_S \leq 10$ kΩ)	Unless Otherwise Specified: $V_S = \pm 15V$			14	mV
Input Offset Current	$0^oC \leq T_A \leq +70^oC$ (LM2908)			250	nA
Input Bias Current	$V_{OUT} = \pm 10V$, $R_L > 2$ kΩ			600	nA
Large Signal Voltage Gain	$R_L > 2$ kΩ	15			V/mV
Output Voltage Swing	$R_L = 10$ kΩ	±12	±13		V
	$R_L = 2$ kΩ	±10	±12		V
Input Voltage Range		±12			V
Common-Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection	$R_S \leq 10$ kΩ	77	96		dB

Note 1. Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.

LM4250/LM4250C Programmable Operational Amplifier

General Description

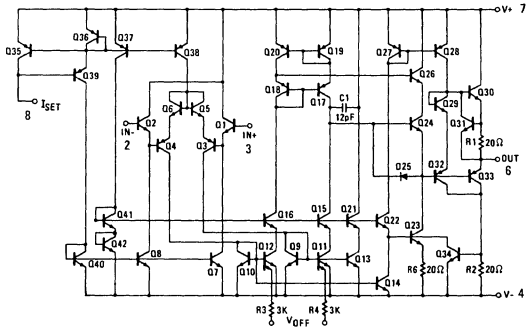
The LM4250 and LM4250C are extremely versatile programmable monolithic operational amplifiers. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product. The device is a truly general purpose operational amplifier.

Features

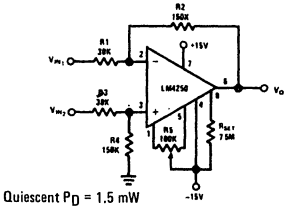
- ±1V to ±18V power supply operation
- 3 nA input offset current
- Standby power consumption as low as 500 nW
- No frequency compensation required
- Programmable electrical characteristics
- Offset Voltage nulling capability
- Can be powered by two flashlight batteries
- Short circuit protection

The LM4250C is identical to the LM4250 except that the LM4250C has its performance guaranteed over a 0°C to 70°C temperature range instead of the −55°C to +125°C temperature range of the LM4250.

Schematic Diagrams

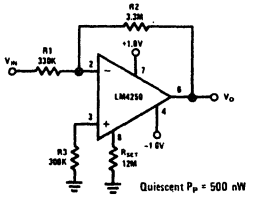


Typical Applications



Quiescent P_D = 1.5 mW

X5 Difference Amplifier



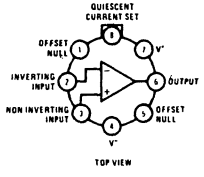
Quiescent P_D = 500 nW

500 Nano-Watt X10 Amplifier

Connection Diagrams

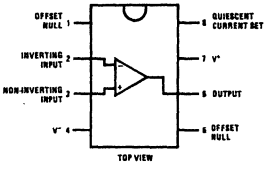
Section 11 for Packaging

Metal Can Package



Order Number LM4250H or LM4250CH

Dual-In-Line Package



Order Number LM4250CN

Order Number LM4250J or LM4250CJ

absolute maximum ratings

Supply Voltage	±18V	Output Short-Circuit Duration		Indefinite
Power Dissipation (Note 1)	500 mW	Operating Temperature Range	LM4250	$-55°C \leq T_A \leq 125°C$
Differential Input Voltage	±30V		LM4250C	$0°C \leq T_A \leq 70°C$
Input Voltage (Note 2)	±15V	Storage Temperature Range		−65°C to 150°C
I_{SET} Current	150 μA	Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics LM4250 ($-55°C \leq T_A \leq 125°C$ unless otherwise specified)

PARAMETERS	CONDITIONS	$V_S = \pm 1.5V$			
		I_{SET} = 1 μA		I_{SET} = 10 μA	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25°$ $R_S \leq 100$ kΩ		3 mV		5 mV
I_{OS}	$T_A = 25°$		3 nA		10 nA
I_{bias}	$T_A = 25°$		7.5 nA		50 nA
Large Signal Voltage Gain	$T_A = 25°$ $R_L = 100$ kΩ	20KV/V			
	$V_O = \pm 0.6$, $R_L = 10$ kΩ			20KV/V	
Supply Current	$T_A = 25°C$		20 μA		120 μA
Power Consumption	$T_A = 25°C$		60 μW		360 μW
V_{OS}	$R_S \leq 100$ kΩ		4 mV		6 mV
I_{OS}	$T_A = 125°C$		5 nA		10 nA
	$T_A = -55°C$		3 nA		10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±0.7V		±0.7V	
Large Signal Voltage Gain	$V_O = \pm 0.6V$ $R_L = 100$ kΩ	10KV/V			
	$R_L = 10$ kΩ			10KV/V	
Output Voltage Swing	$R_L = 100$ kΩ	±0.6V			
	$R_L = 10$ kΩ			±0.6V	
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ	76 dB		76 dB	
Supply Current			20 μA		200 μA
Power Consumption			60 μW		600 μW

PARAMETERS	CONDITIONS	$V_S = \pm 15V$			
		I_{SET} = 1 μA		I_{SET} = 10 μA	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25°C$ $R_S \leq 100$ kΩ		3 mV		5 mV
I_{OS}	$T_A = 25°C$		3 nA		10 nA
I_{bias}	$T_A = 25°C$		7.5 nA		50 nA
Large Signal Voltage Gain	$T_A = 25°C$ $R_L = 100$ kΩ	30KV/V			
	$V_O = \pm 10V$ $R_L = 10$ kΩ			30KV/V	
Supply Current	$T_A = 25°C$		25 μA		210 μA
Power Consumption	$T_A = 25°C$		300 μW		2.7 mW
V_{OS}	$R_S \leq 100$ kΩ		4 mV		6 mV
I_{OS}	$T_A = 125°C$		25 nA		25 nA
	$T_A = -55°C$		3 nA		10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 100$ kΩ	20KV/V			
	$R_L = 10$ kΩ			20KV/V	
Output Voltage Swing	$R_L = 100$ kΩ	±12V			
	$R_L = 10$ kΩ			±12V	
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ	76 dB		76 dB	
Supply Current			25 μA		250 μA
Power Consumption			750 μW		7.5 mW

Note 1: The maximum junction temperature of the LM4250 is 150°C, while that of the LM4250C is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W junction to ambient, or 45°C/W junction to case. The thermal resistance of the dual-in-line package is 125°C/W.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

electrical characteristics LM4250C ($0°C \leq T_A \leq 70°C$ unless otherwise specified)

PARAMETERS	CONDITIONS	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25°C$ $R_S \leq 100\ k\Omega$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$T_A = 25°C$ $R_L = 100\ k\Omega$	25kV/V			
	$V_O = \pm 0.6V$ $R_L = 10\ k\Omega$			25kV/V	
Supply Current	$T_A = 25°C$		20 μA		120 μA
Power Consumption	$T_A = 25°C$		60 μW		270 μW
V_{OS}	$R_S \leq 10\ k\Omega$		6.5 mV		360 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	$V_O = \pm 0.6V$ $R_L = 100\ k\Omega$	25kV/V			
	$R_L = 10\ k\Omega$			25kV/V	
Output Voltage Swing	$R_L = 100\ k\Omega$	±0.6V			
	$R_L = 10\ k\Omega$			±0.6V	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	74 dB		74 dB	
Supply Current			20 μA		120 uA
Power Consumption			60 μW		600 uW

PARAMETERS	CONDITIONS	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25°C$ $R_S \leq 100\ k\Omega$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$T_A = 25°C$ $R_L = 100\ k\Omega$	25 KV/V			
	$V_O = \pm 10V$ $R_L = 10\ k\Omega$			25 KV/V	
Supply Current	$T_A = 25°C$		25 μA		210 μA
Power Consumption	$T_A = 25°C$		330 μW		3 mW
V_{OS}	$R_S \leq 10\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 100\ k\Omega$	20KV/V			
	$R_L = 10\ k\Omega$			20KV/V	
Output Voltage Swing	$R_L = 100\ k\Omega$	±12V			
	$R_L = 10\ k\Omega$			±12V	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	74 dB		74 dB	
Supply Current			25 uA		250 uA
Power Consumption			750 uW		7.5 mW

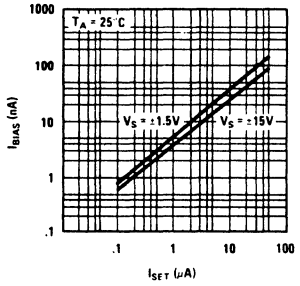
resistor biasing

Set Current Setting Resistor to V^-

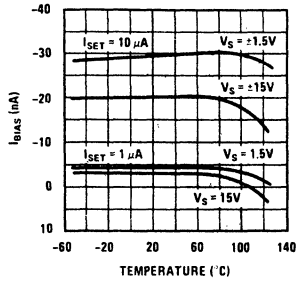
	I_{SET}				
V_S	0.1 μA	0.5 μA	1.0 μA	5 μA	10 μA
±1.5V	25.6 MΩ	5.04 MΩ	2.5 MΩ	492 kΩ	244 kΩ
±3.0V	55.6 MΩ	11.0 MΩ	5.5 MΩ	1.09 MΩ	544 kΩ
±6.0V	116 MΩ	23.0 MΩ	11.5 MΩ	2.29 MΩ	1.14 MΩ
±9.0V	176 MΩ	35.0 MΩ	17.5 MΩ	3.49 MΩ	1.74 MΩ
±12.0V	236 MΩ	47.0 MΩ	23.5 MΩ	4.69 MΩ	2.34 MΩ
±15.0V	296 MΩ	59.0 MΩ	29.5 MΩ	5.89 MΩ	2.94 MΩ

Typical Performance Characteristics

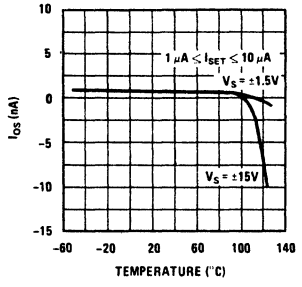
Input Bias Current vs I_{SET}



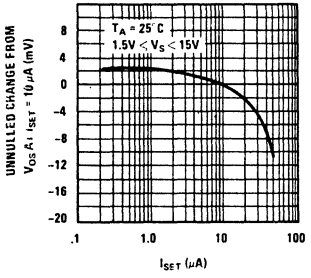
Input Bias Current vs Temperature



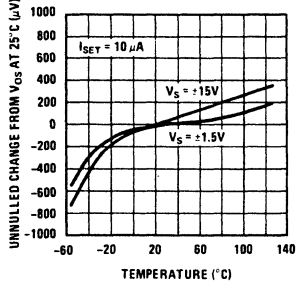
Input Offset Current vs Temperature



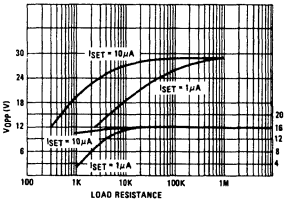
Unnulled Input Offset Voltage Change vs I_{SET}



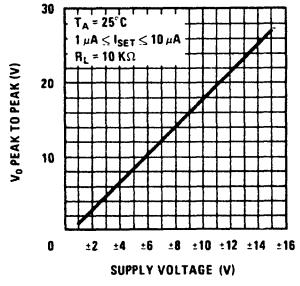
Unnulled Input Offset Voltage Change vs Temperature



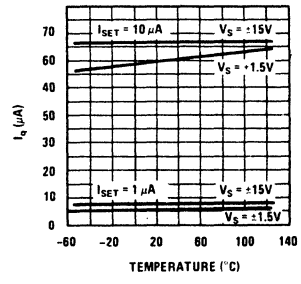
Peak to Peak Output Voltage Swing vs Load Resistance



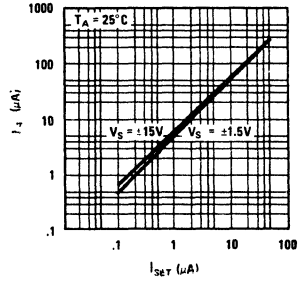
Peak to Peak Output Voltage Swing vs Supply Voltage



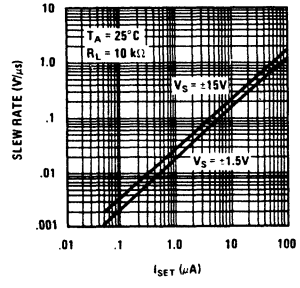
Quiescent Current (I_Q) vs Temperature



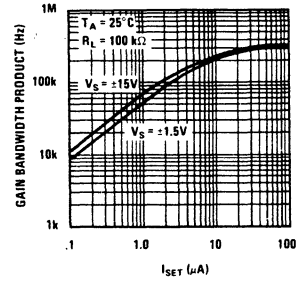
Quiescent Current (I_Q) vs I_{SET}



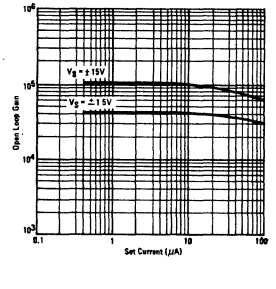
Slew Rate vs I_{SET}



Gain Bandwidth Product vs I_{SET}

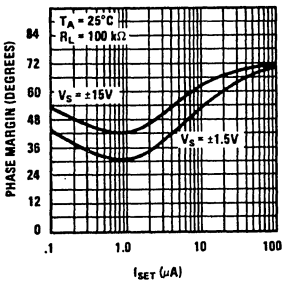


Open Loop Voltage Gain vs I_{SET}

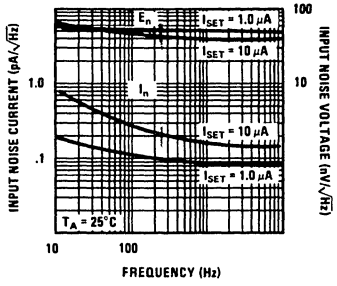


typical performance characteristics (con't)

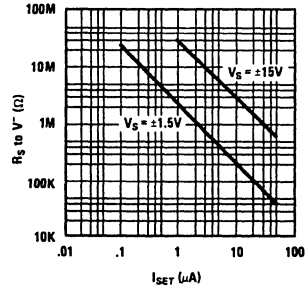
Phase Margin vs I_{SET}



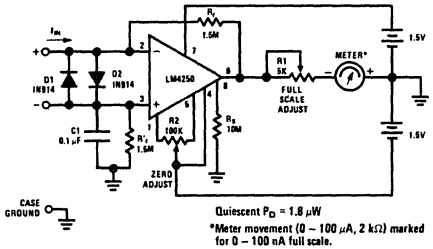
Input Noise Current (I_n) and Voltage (E_n) vs Frequency



R_{SET} vs I_{SET}



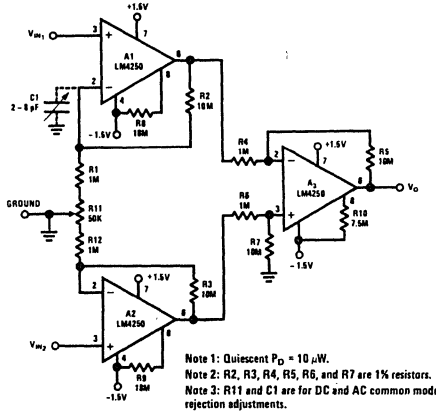
typical applications (con't)



Quiescent P_D = 1.8 μW

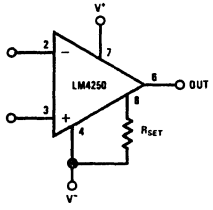
*Meter movement (0 – 100 μA, 2 kΩ) marked for 0 – 100 nA full scale.

Floating Input Meter Amplifier
100 Nano-Ampere Full Scale

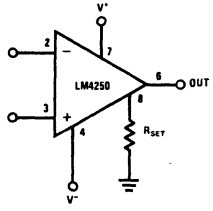


Note 1: Quiescent P_D = 10 μW.
Note 2: R2, R3, R4, R5, R6, and R7 are 1% resistors.
Note 3: R11 and C1 are for DC and AC common mode rejection adjustments.

X100 Instrumentation Amplifier 10 μW



R_{SET} Connected to V⁻

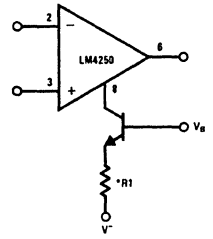


R_{SET} Connected to Ground

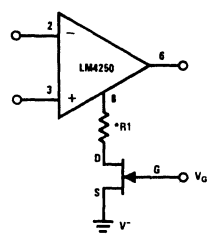
I_{SET} EQUATIONS:

$$I_{SET} \approx \frac{V^+ + |V^-| - 0.5}{R_{SET}}$$ where R_{SET} is connected to V⁻.

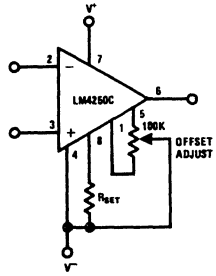
$$I_{SET} \approx \frac{V^+ - 0.5}{R_{SET}}$$ where R_{SET} is connected to ground.



Transistor Current Source Biasing



FET Current Source Biasing



Offset Null Circuit

*R1 limits I_{SET} maximum

HARRIS

OP-07

ULTRA-LOW OFFSET VOLTAGE OP AMP

GENERAL DESCRIPTION

The OP-07 Series represents a breakthrough in monolithic operational amplifier performance—Vos of 10 μV, TC Vos of 0.4 μV/°C and long term stability of 0.2 μV/month are achieved by a low noise, chopper-less bipolar input transistor amplifier circuit. Complete elimination of external components for offset nulling, frequency compensation and device protection permits extreme miniaturization and optimization of system Mean-Time-Between-Failure Rates in high performance aerospace/defense and industrial applications. Excellent device interchangeability provides reduced system assembly time and eliminates field recalibrations.

2

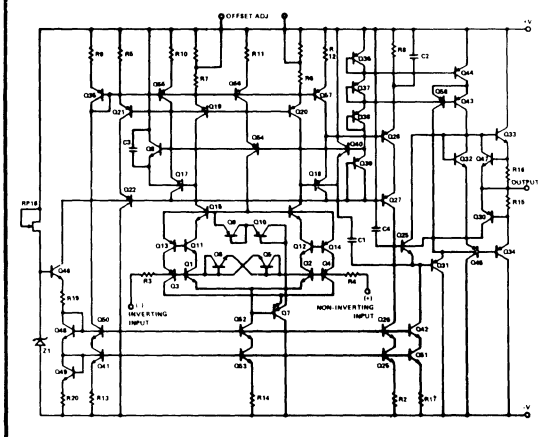
True differential inputs with wide input voltage range and outstanding common mode rejection provide maximum flexibility and performance in high noise environments and non-inverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.

Low cost, high volume production of OP-07 is achieved by laser trimming of an on-chip offset trimming network during initial factory testing. The OP-07 provides unparalleled performance for low noise, high accuracy amplification of very low level signals in transducer applications. Other applications include use in stable integrators, precision summing amplifiers for analog computation and test equipment and in ultra-precise voltage threshold detectors and comparators. The OP-07 is recommended as a replacement for modular and monolithic chopper-stabilized amplifiers where reductions in cost, noise, size and power consumption are required. Devices are available in chip form for use in hybrid circuitry. The OP-07 is a direct replacement for 725, 108A/308A, and OP-05 amplifiers: 741-types may be directly replaced by removing the 741's nulling potentiometer.

FEATURES

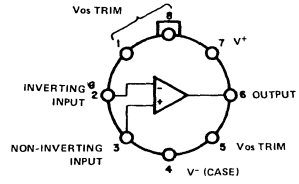
- Ultra-Low Vos . . . . . 10 μV
- Ultra-Low Vos Drift . . . . . 0.4 μV/°C
- Ultra-stable vs Time . . . . . 0.2 μV/Month
- Ultra-Low Noise . . . . . 0.35 μVp-p
- No External Components required
- Replaces Chopper amps at Lower Cost
- Single Chip Monolithic Construction
- Large Input Voltage Range. . . . . ±14.0V
- Wide Supply Voltage Range . . . . . ±5V to ±18V
- Fits 725, 108A/308A, 741, AD510 Sockets

SCHEMATIC



PIN CONNECTIONS AND ORDERING INFORMATION

Section 11 for Packaging



TO-99 (J-Suffix)
ORDER: OP-07AJ
OP-07J

ELECTRICAL CHARACTERISTICS			OP-07A			OP-07			
These specifications apply for V_S = ±15V, T_A = 25°C, unless otherwise noted.									
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
Input Offset Voltage	V_{os}	(Note 1)		10	25		30	75	µV
Long Term Input Offset Voltage Stability	V_{os}/Time	(Note 2)		0.2	1.0	-	0.2	1.0	µV/Mo
Input Offset Current	I_{os}		-	0.3	2.0	-	0.4	4.0	nA
Input Bias Current	I_B		-	±.7	±2.0		±1.0	±4.0	nA
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz (Note 3)	--	0.35	0.6	--	0.35	0.6	µV p-p
Input Noise Voltage Density	e_n	f_o = 10Hz (Note 3) f_o = 100Hz (Note 3) f_o = 1000Hz (Note 3)	--- -- --	10.3 10.0 9.6	18.0 13.0 11.0	-- --- --	10.3 10.0 9.6	18.0 13.0 11.0	nV/√Hz
Input Noise Current	i_{np-p}	0.1Hz to 10Hz (Note 3)	--	14	30	--	14	30	pA p-p
Input Noise Current Density	i_n	f_o = 10Hz (Note 3) f_o = 100Hz (Note 3) f_o = 1000Hz (Note 3)	-- -- --	0.32 0.14 0.12	0.80 0.23 0.17	-- -- -	0.32 0.14 0.12	0.80 0.23 0.17	pA/√Hz
Input Resistance - Differential Mode	R_{in}		30	80	--	20	60	-	MΩ
Input Resistance - Common Mode	R_{inCM}		--	200	--	-	200	--	GΩ
Input Voltage Range	IVR		±12	±14.0	--	±12	±14.0	--	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±10	110	126	--	110	126	--	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	100	110	--	100	110	--	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, V_O = ±10V $R_L \geq 500\Omega$, V_O = ± 5V V_S = ±3V	300 150	500 500	-- --	200 150	500 500	-- --	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $R_L \geq 1k\Omega$	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	--	±12.5 ±12.0 ±10.5	±13.0 ±12.8 ±12.0	-- -- --	V
Slewing Rate	SR	R_L = ≥ 2kΩ (Note 3)	0.1	0.17	-	0.1	0.17	--	V/µsec
Closed Loop Bandwidth	BW	A_{VCL} = +1.0 (Note 3)	0.4	0.6	--	0.4	0.6	--	MHz
Open Loop Output Resistance	R_o	V_O = 0, I_O = 0	-	45	-	--	45	--	Ω
Power Consumption	Pd	V_S = ±3V		300	390	-- --	300	390	mW
Offset Adjustment Range		R_p = 20kΩ	--	±2	--	--	±2	--	mV
The following specifications apply for V_S = ±15V, -55°C ≤ T_A ≤ +125°C, unless otherwise noted.									
Input Offset Voltage	V_{os}	(Note 1)	--	25	60	--	60	200	µV
Average Input Offset Voltage Drift Without External Trim With External Trim	 TCV_{os} TCV_{osn}	 R_p 20kΩ	 -- --	 0.4 0.4	 0.6 0.6	 -- --	 0.4 0.4	 1.3 1.3	 µV/°C µV/°C
Input Offset Current	I_{os}		--	0.8	4.0	--	1.2	5.6	nA
Average Input Offset Current Drift	TCI_{os}		--	5	25	--	8	50	pA/°C
Input Bias Current	I_B		--	±1.0	±4.0	--	±2.0	±6.0	nA
Average Input Bias Current Drift	TCI_B		--	8	25	--	13	50	pA/°C
Input Voltage Range	IVR		±13.0	±13.5	--	±13.0	±13.5	--	V
Common Mode Rejection Ratio	CMRR	V_{CM} = ±13V	106	123	--	106	123	--	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	94	106	--	94	106	--	dB
Large Signal Voltage Gain	A_{vo}	$R_L \geq 2k\Omega$, V_O = ±10V	200	400	--	150	400	--	V/mV
Maximum Output Voltage Swing	V_{oM}	$R_L \geq 2k\Omega$	±12.0	±12.6	--	±12.0	±12.6	--	V

NOTE 1: Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, OP-07A offset voltage is measured five minutes after power supply application at 25°C, -55°C and +125°C.

NOTE 2: Long Term Input Offset Voltage Stability refers to the averaged trend line of Vos vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in Vos during the first 30 operating days are typically 2.5µV — refer to typical performance curve on Page 5. Parameter is not 100% tested; 90% of units meet this specification.

NOTE 3: Parameter is not 100% tested; 90% of units meet this specification.

ABSOLUTE MAXIMUM RATINGS

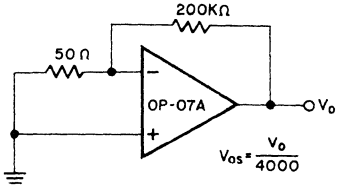
Supply Voltage	±22V	Storage Temperature	-65°C to 150°C
Internal Power Dissipation (Note 1)	500mW	Operating Temperature Range	
Differential Input Voltage	±30V	OP-07A, OP-07	-55°C to +125°C
Input Voltage (Note 2)	±22V	Lead Temperature Range	300°C
Output Short Circuit Duration	Indefinite	(Soldering, 60 sec)	

NOTES:

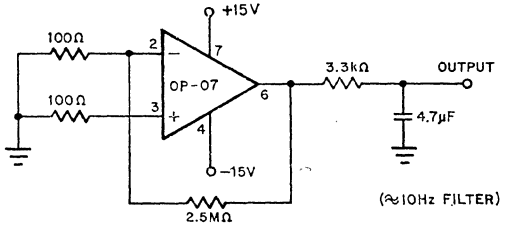
Note 1: Maximum package power dissipation vs. ambient temperature.

Note 2: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

TYPICAL OFFSET VOLTAGE TEST CIRCUIT

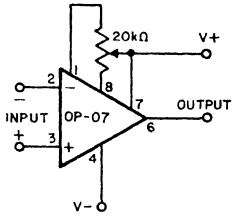


TYPICAL LOW FREQUENCY NOISE TEST CIRCUIT

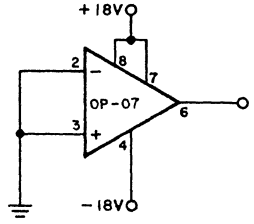


INPUT REFERRED NOISE = $\frac{V_o}{25,000} = \frac{5mV/cm}{25,000} = 200nV/cm$

OPTIONAL OFFSET NULLING CIRCUIT



BURN-IN CIRCUIT



APPLICATIONS INFORMATION

OP-07 Series units may be fitted directly to 725, 108A/308A* and OP-05 sockets with or without removal of external compensation or nulling components. Additionally, OP-07 may be fitted to unnulled 741-type sockets; however if conventional 741 nulling circuitry is in use, it should be modified or removed to enable proper OP-07 operation. OP-07 offset voltage may be nulled to zero (or other desired setting) through use of a potentiometer (see diagram above).

*"J" Package Only.

The OP-07 provides stable operation with load capacitances up to 500pF and ±10V swings; larger capacitances should be decoupled with a 50Ω decoupling resistor. The designer is cautioned that stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

HARRIS

ADVANCE

HA-5141/42/44

Ultra-Low Power Operational Amplifier

FEATURES

- LOW SUPPLY CURRENT 60μA
- WIDE OPERATING VOLTAGE RANGE 2V to 30V
- SINGLE SUPPLY OPERATION
- HIGH SLEW RATE 1.5V/μs
- HIGH GAIN 100K V/V
- AVAILABLE IN SINGLES, DUALS AND QUADS

APPLICATIONS

- PORTABLE INSTRUMENTS
- METER AMPLIFIERS
- TELEPHONE HEADSETS
- MICROPHONE AMPLIFIERS
- INSTRUMENTATION

DESCRIPTION

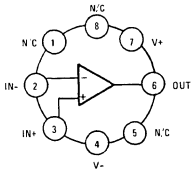
The HA-5141/42/44 ultra-low power operational amplifiers provide AC and DC performance characteristics similar to or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. These amplifiers are well suited to applications which require low power dissipation and good electrical characteristics.

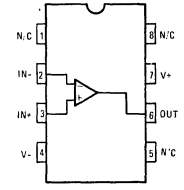
The HA-5141/42/44 provides accurate signal processing by virtue of its low input offset voltage (0.5mV), low input bias current (50nA), high open loop gain (100KV/V) and low noise, for low power operational amplifiers (20nV/$\sqrt{Hz}$). These characteristics coupled with 1.5V/μs slew rate and 400KHz bandwidth make the HA-5141/42/44 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (2V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment.

These amplifiers are available in singles (HA-5141, can or minidip), duals (HA-5142, can or minidip) or quads (HA-5144, 14 pin dip) with industry standard pinouts which allow the HA-5141/42/44's to be interchangeable with most other operational amplifiers.

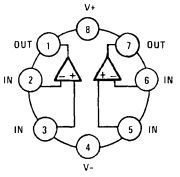
PINOUTS

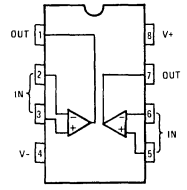
TOP VIEW



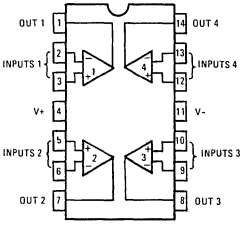


TOP VIEW

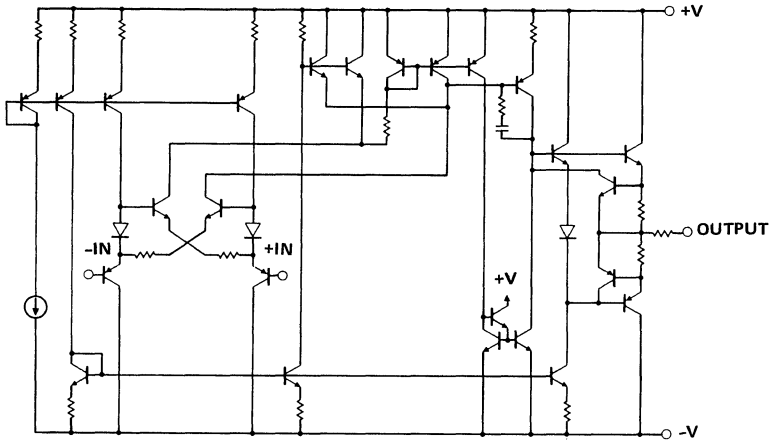




TOP VIEW



SCHEMATIC



2

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Operating Temperature Range	$0^{o}C \leq T_A \leq +75^{o}C$
Differential Input Voltage	±7V		$-55^{o}C \leq T_A \leq +125^{o}C$
Output Current	S/C Protected	Storage Temperature Range	$-65^{o} \leq T_A \leq +150^{o}C$
Internal Power Dissipation	500mW		

ELECTRICAL CHARACTERISTICS V+ = +5V

		HA-5141/42/44A			HA-5141/42/44			
PARAMETER	TEMP.	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.5	6		0.7	7	mV
	Full			8			9	mV
Bias Current	+25°C		45	75		45	100	nA
	Full			100			125	nA
Offset Current	+25°C		0.3	10		0.3	10	nA
	Full			15			20	nA
Common Mode Range	Full	0 to 4			0 to 3			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain	+25°C	50	100		20	100		KV/V
(Note 1)	Full	30			15			KV/V
Common Mode Rejection	Full	80	105		77	105		dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	0 to 4			0 to 3			V
TRANSIENT RESPONSE								
Slew Rate (Notes 1,2,3)	+25°C	1	1.5		0.5	1		V/μs
POWER SUPPLY CHARACTERISTICS								
Supply Current (per Amplifier)	+25°C		45	65		50	80	μA
	Full			75			100	μA
Power Supply Rejection Ratio	Full	80	105		77	105		dB

NOTES:
1. RL = 50K
2. CL = 50pf
3. VIN = +3V Pulse

HARRIS

ADVANCE

HA-5180/5180A

Low Bias Current, Low Power JFET Input Operational Amplifier

FEATURES

• ULTRA LOW BIAS CURRENT	250fA
• LOW POWER SUPPLY CURRENT	0.8mA
• LOW OFFSET VOLTAGE	0.5mV (max.)
• BANDWIDTH	2 MHz
• SLEW RATE	7V/ μs

APPLICATIONS

- ELECTROMETER AMPLIFIER DESIGNS
- PHOTO CURRENT DETECTORS
- PRECISION, LONG-TERM INTEGRATORS
- LOW DRIFT SAMPLE & HOLD CIRCUITS
- VERY HIGH IMPEDANCE BUFFERS
- HIGH IMPEDANCE BIOLOGICAL MICRO PROBES

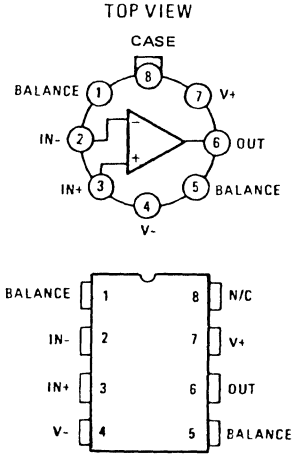
DESCRIPTION

The HARRIS HA-5180/5180A is an ultra low input bias current, JFET input, monolithic operational amplifier which also features low power, low offset voltage and excellent AC characteristics. Employing FET/Bipolar construction coupled with dielectric isolation this operational amplifier offers the lowest input bias currents (250fA typ.) available in any monolithic operational amplifier. The HA-5180/5180A has another unique feature in which the offset bias current may be nulled by externally adjusting the offset voltage. For applications which require precision performance the HA-5180A offers an input offset voltage of 0.5 mV (max) while the HA-5180 offers 3 mV (max.)

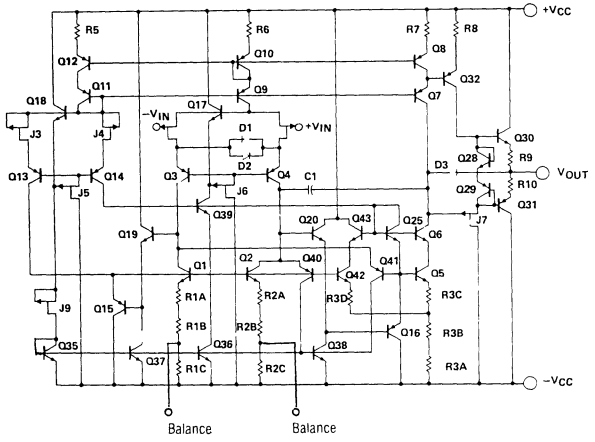
The HA-5180/5180A also offers excellent AC performance not previously available in similar hybrid or monolithic op amp designs. The 2 MHz bandwidth and 7V/μs slew rate of the HA-5180/5180A extends the bandwidth and speed for applications such as very low drift sample and hold amplifiers and photo-current detectors. Other applications include use in electrometer designs, pH/Ion sensitive electrodes, low current oxygen sensors, long term precision integrators and very high impedance buffer measurement designs.

The HA-5180/5180A is packaged in an 8-pin (TO-99) can and an 8-lead cerdip and is pin compatible with most existing op amp configurations. The case of the TO-99 package is internally connected to pin 8 so that it may be connected to the same potential as the input. This feature helps minimize stray leakage to the case, helps shield the amplifier from external noise and reduces common mode input capacitance.

PINOUT



SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 1)

$T_A = +25°C$ Unless otherwise stated

Voltage Between V+ and V− Terminals	40.0V	Power Dissipation (Note 2)	300mW
Differential Input Voltage	±40V	Operating Temperature Range	
		HA-5180/5180A-2	$-55°C \leq T_A \leq +125°C$
		HA-5180/5180A-5	$0°C \leq T_A \leq +75°C$
Output Short Circuit Duration	Indefinite	Storage Temperature Range	$-65°C \leq T_A \leq +150°C$

ELECTRICAL RATINGS V+ = 15V, V− = −15V

PARAMETER	TEMP.	5180A-2 MIN	5180A-2 TYP	5180A-2 MAX	5180A-5 MIN	5180A-5 TYP	5180A-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		0.1	0.5		0.1	0.5	mV
	Full			1			1	mV
Average Offset Voltage Drift	Full		5			5		µV/°C
Bias Current (Note 3)	+25°C		250	1000		250	1000	fA
	Full		100	500		6	30	pA
Offset Current (Note 3)	+25°C		30	200		30	200	fA
	Full		6	30		1	5	pA
Common Mode Range	Full	±10	±12		±10	±12		V
Differential Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Noise Voltage (f = 1kHz)	+25°C		70			70		$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C		0.01			0.01		$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	200k	1M		200k	1M		V/V
	Full	150k			150k			V/V
Common Mode Rejection Ratio (Note 5)	Full	90	110		90	110		dB
Closed Loop Bandwidth ($A_{VCL} = +1$)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
	Full	±10			±10			V
Full Power Bandwidth (Note 7)	+25°C		110			110		kHz
Output Current (Note 8)	+25°C	±10	±15		±10	±15		mA
Output Resistance (Note 9)	+25°C		25			25		Ω
TRANSIENT RESPONSE								
Rise Time	+25°C		75			75		ns
Slew Rate	+25°C	4	7		4	7		V/µs
Settling Time (Note 10)	+25°C		2			2		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		0 7	1		0 8	1	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105		85	105		dB

ELECTRICAL RATINGS

V+ = 15V, V− = −15V

PARAMETER	TEMP.	5180A-2 MIN	5180A-2 TYP	5180A-2 MAX	5180A-5 MIN	5180A-5 TYP	5180A-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		1	3		1	3	mV
	Full			4			4	mV
								mV
								mV
Average Offset Voltage Drift	Full		5			5		µV/°C
Bias Current (Note 3)	+25°C		250	1000		250	1000	fA
	Full		100	500		6	**30**	pA
Offset Current (Note 3)	+25°C		30	200		30	200	fA
	Full		6	30		1	5	pA
Common Mode Range	Full	±10	±12		±10	±12		V
Differential Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Noise Voltage (f = 1kHz)	+25°C		70			70		nV/√Hz
Input Noise Current (f = 1kHz)	+25°C		0.01			0.01		pA/√Hz
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	200k	1M		200k	1M		V/V
	Full	150k			**150k**			V/V
Common Mode Rejection Ratio (Note 5)	Full	90	110		90	110		dB
Closed Loop Bandwidth ($A_{VCL} = +1$)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12		±10	±12		V
	Full	±10			±10			V
Full Power Bandwidth (Note 7)	+25°C		110			110		kHz
Output Current (Note 8)	+25°C	±10	±15		±10	±15		mA
Output Resistance (Note 9)	+25°C		25			25		Ω
TRANSIENT RESPONSE								
Rise Time	+25°C		75			75		ns
Slew Rate	+25°C	4	7		4	7		V/µs
Settling Time (Note 10)	+25°C		2			2		µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full		0.7	1		0.8	1	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105		85	105		dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.9 mW/°C for operation at ambient temperatures above +75°C.
3. This parameter is guaranteed by design and is not 100% tested.
4. $V_{OUT} = \pm 10V$; $R_L = 2k$. Gain dB = 20 $\log_{10} Av$.
5. $V_{CM} = \pm 10V$ D.C.
6. $R_L = 2k$
7. $R_L = 2k$; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. $V_{OUT} = \pm 10V$.
9. Output resistance measured under open loop conditions (f = 100Hz)
10. Settling time is measured to 0.1% of final value for a 10V output step and $A_V = -1$.
11. V_{SUPP} = + 5V D.C. to ±20V D.C.

APPLICATION HINTS

The HA-5180/5180A offers one of the lowest input bias currents of any monolithic operational amplifier and is ideal for use in applications for measuring signals from very high impedance or very low current sources. To fully utilize the capabilities of the HA-5180/5180A care should be taken to minimize noise pickup and current leakage paths with the use of shielding and guarding techniques and by placing the device as close as possible to the signal source. The small size and low quiesent current (possible battery operation) of the HA-5180/5180A allows easy installation at the signal source or inside a probe. The HA-5180/5180A is internally compensated and is capable of driving long signal cables which have several hundred pF capacitive loading.

Guarding is achieved by applying a low impedance bootstrap potential to a shield which surrounds the high impedance signal line. This bootstrap potential should be held at the same potential as the signal source to eliminate any voltage drop (therefore, zero leakage currents) across the insulation (Ref to Fig 1 & 2). For lowest leakage at the device either use a teflon IC socket or connect the high impedance signal line to the HA-5180/5180A inputs using teflon standoffs. If neither of these options are feasible, a guard ring, as shown in Fig. 3, applied to both sides of the pc board and bootstrapped to the same potential as the input signal will minimize leakage paths across the pc board. Pin 8 of the TO-99 can, which is internally tied to the case, should also be tied to the bootstrap potential to help minimize noise pickup and leakage currents accross the package insulation. This technique will also reduce common mode input capacitance.

Cleanliness of circuit boards and components is also important for achieving low leakage currents. Printed circuit boards and components should be thoroughly cleaned by using a low residue solvent such as TMC Freon, rinsed by deionized water and dried with nitrogen. The circuit board should be protected from high contamination and high humidity environments.

Input protection is generally not necessary when designing with the HA-5180/5180A. Many electrometer type devices, especially CMOS, require elaborate zener protection schemes which may compromise overall performance. The Harris dielectric isolation process and JFET input design enables the HA-5180/5180A to withstand input signals several volts beyond either supply and large differential signals equal to the rail-to-rail supply voltage without damage or degredation of performance.

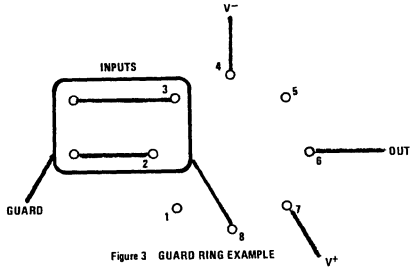


Figure 3 GUARD RING EXAMPLE

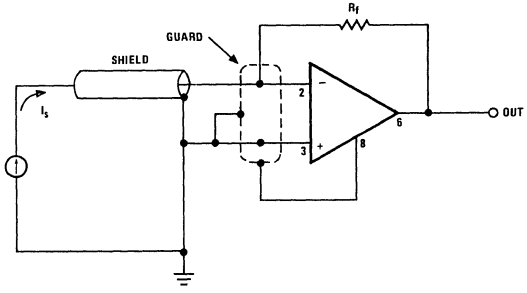


Figure 1 CURRENT TO VOLTAGE CONVERTER

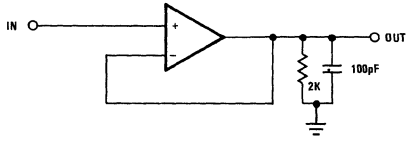


Figure 4 SLEW RATE AND TRANSIENT RESPONSE

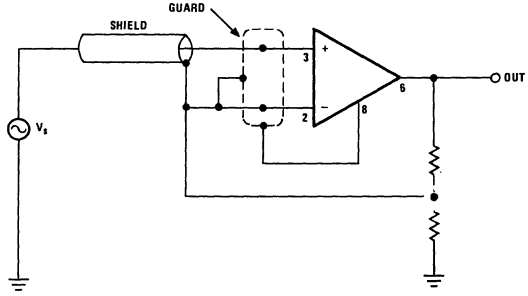


Figure 2 VERY HIGH IMPEDANCE NON-INVERTING AMPLIFIER

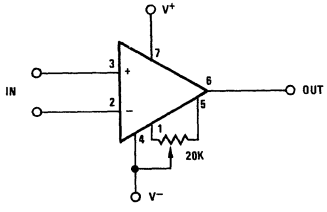


Figure 5 SUGGESTED OFFSET ADJUSTMENT CIRCUIT

CMOS
Analog Switches

3

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

Analog Switches Glossary

ANALOG SIGNAL RANGE (± Vs) - The maximum safe input voltage range.

BREAK-BEFORE-MAKE-DELAY (tOPEN) - The elapsed time between the turn-off of one switch and the corresponding turn-on of another switch for a common change in logic state. This delay is measured between the 50% points of the output transitions.

CHANNEL INPUT CAPACITANCE (C_{SOFF}) The capacitance between the analog input and ground with the channel "OFF." This capacitance consists primarily of the source-body capacitance.

CHANNEL OUTPUT CAPACITANCE (C_{DOFF}) The capacitance between the analog output and ground with the channel "OFF". This capacitance consists of the sum of the drain-body capacitances.

CHANNEL OUTPUT CAPACITANCE (C_{DON}) - The capacitance between the analog output and ground with the channel "ON".

CHARGE INJECTION - The amount of charge transferred to a specified load capacitance due to the switch changing state.

CROSSTALK - The amount of cross coupling from an "OFF" analog input to the output of another "ON" channel output.

DIGITAL INPUT CAPACITANCE - The capacitance between a digital input and ground.

INPUT LOW LEAKAGE CURRENT (I_{AL}) - The current measured at the digital input with a logic low applied.

INPUT LOW THRESHOLD (V_{AL}) - The maximum allowable voltage that can be applied to the digital inputs and still be recognized by the device as a low input.

INPUT HIGH LEAKAGE CURRENT (I_{AH}) - The current measured at the digital input with a logic high applied.

INPUT HIGH THRESHOLD (V_{AH}) - The minimum voltage that can be applied to the digital inputs and still be recognized by the device as a high input.

INPUT TO OUTPUT CAPACITANCE (CD_{SOFF}) - The capacitance between the analog input and output when the channel is "OFF".

"OFF" INPUT LEAKAGE CURRENT (I_{SOFF}) - The current measured at the input of an "OFF" channel with a specified voltage applied to both input and output. This current consists largely of the diode leakage current of the source- body junctions.

OFF ISOLATION - The feedthrough of an applied signal through an "OFF" switch to the output. This feedthrough occurs through the source-body and drain-body capacitances and has a greater effect at high frequencies.

"OFF" OUTPUT LEAKAGE CURRENT (I_{DOFF}) - The current measured at the output of an "OFF" channel with a specified voltage applied to both input and output. This current is due largely to the diode leakages of the drain-body junctions.

"ON" CHANNEL LEAKAGE CURRENT (I_{DON}) - The current flowing through the source-body and drain body junctions of the "ON" channel. This current is measured with a specified voltage applied to both the input and output.

"ON" RESISTANCE (R_{ON}) - The series "ON" channel resistance measured between the input and output terminals under a specified range of input voltages.

SUPPLY CURRENT (I_S) - The current required from the power supply to operate the switch in a no load condition.

SWITCH TURN "OFF" TIME (t_{OFF}) - The time required to deactivate an "ON" switch to an "OFF" state. This time is measured from the 50% point of the logic input change to the time the output reaches 10% of the initial value.

SWITCH TURN "ON" TIME (t_{ON}) - The time required to activate an "OFF" switch to an "ON" state. This time is measured for the 50% point of the logic input to the time the output reaches 90% of the final value.

CMOS Switches Selection Guide

FUNCTION	DEVICE	R_{ON} (Ω) (TYP)	$I_{D(OFF)}$ (NA) (TYP)	$t_{(ON)}$ (NS) (TYP)	$t_{(OFF)}$ (NS) (TYP)	P_D (mW) (TYP)
SPST	HI-5040	50	0.5	370	280	1.5
2 x SPST	HI-200	55	1	240	180	15
	HI-300	35	0.04	210	160	1
	HI-304	35	0.04	210	160	0.3
	HI-381	35	0.04	210	160	1
	HI-5048	25	0.5	370	280	1.5
	HI-5041	50	0.5	370	280	1.5
4 x SPST	HI-201	55	1	180	155	15
	HI-201HS	30	0.3	30	40	120
SPDT	HI-301	35	0.04	210	160	1
	HI-305	35	0.04	210	160	0.3
	HI-387	35	0.04	210	160	1
	HI-5050	25	0.5	370	280	1.5
	HI-5042	50	0.5	370	280	1.5
2 x SPDT	HI-303	35	0.04	210	160	1
	HI-307	35	0.04	210	160	0.3
	HI-390	35	0.04	210	160	1
	HI-5051	25	0.5	370	280	1.5
	HI-5043	50	0.5	370	280	1.5
DPST	HI-5044	50	0.5	370	280	1.5
2 x DPST	HI-302	35	0.04	210	160	1
	HI-306	35	0.04	210	160	0.3
	HI-384	35	0.04	210	160	1
	HI-5049	25	0.5	370	280	1.5
	HI-5045	50	0.5	370	280	1.5
DPDT	HI-5046A	25	0.5	370	280	1.5
	HI-5046	50	0.5	370	280	1.5
4PST	HI-5047A	25	0.5	370	280	1.5
	HI-5047	50	0.5	370	280	1.5

NOTE: All data represents typical room temperature specifications at ±15V supplies. For guaranteed and tested specifications, consult the device data sheet.

HARRIS

HI-200

Dual SPST CMOS Analog Switch

3

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 240ns
- LOW R_{ON} 55Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

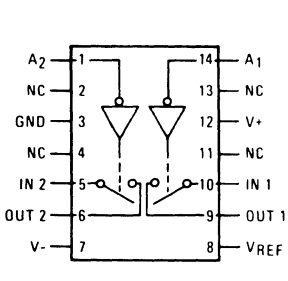
HI-200 is a monolithic device comprising two independently selectable SPST switches which feature fast switching speeds (290ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-200 operates without any applications problems induced by latch-up or SCR mode phenomena.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters,and op amp gain switching networks.

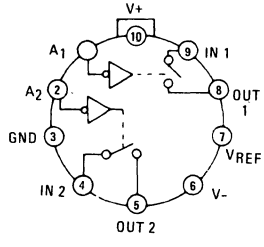
HI-200 is available in DIP and metal (TO-100) cans. HI-200-2 is specified from -55°C to +125°C while HI-200-5 operates from 0°C to +75°C. HI-200 is functionally and pin compatible with other available "200 series" switches.

PINOUT

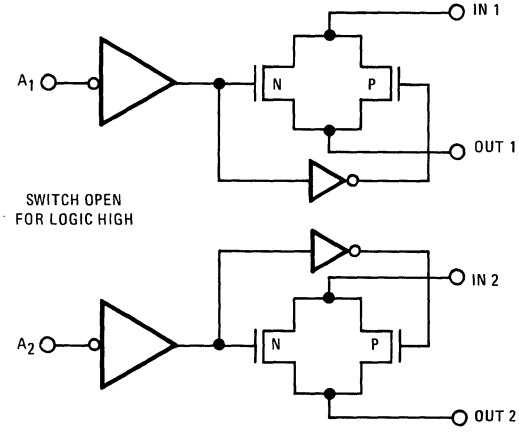
Section 11 for Packaging



Top View



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	44V (±22)	Total Power Dissipation*	450mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	$+V_{Supply}$ +4V	HI-200-2	-55°C to +125°C
	$-V_{Supply}$ -4V	HI-200-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-200-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 6mW/°C Above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH}(Logic Level High) = 2.4V V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

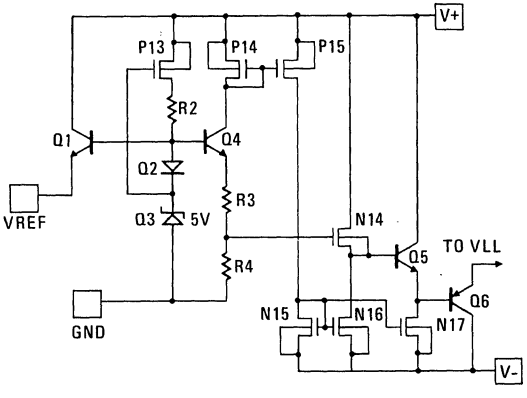
		HI-200-2 -55°C to +125°C			HI-200-5 ** 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		72	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current	+25°C		1			1		nA
(Note 6)	Full		100	500		10	500	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C		1			1		nA
(Note 6)	Full		100	500		10	500	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		.02			.02		nA
	Full		6	500		6	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	2.4			2.4			V
I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		60			60		ns
t_{on}, Switch on Time	+25°C		240	500		240		ns
t_{off}, Switch off Time	+25°C		330	500		500		ns
"Off Isolation" (Note 4)	+25°C		70			70		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
I^+, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
I^-, Current	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = +5V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f = 100kHz
5. V_A = +3V or V_A = OV For Both Switches
6. Refer to leakage current measurement diagram on page (3-8)

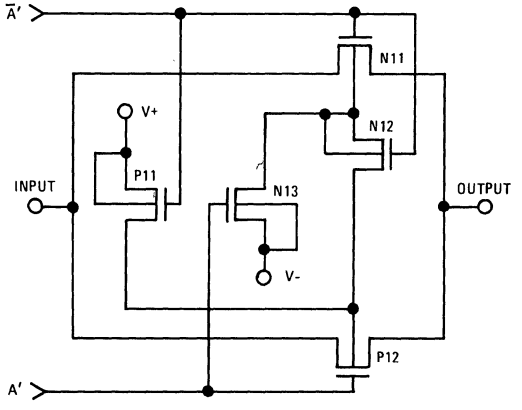
** Note: HI-200-4 has same specifications as HI-200-5 over the temperature range -20°C to +85°C.

TTL/CMOS
REFERENCE CIRCUIT

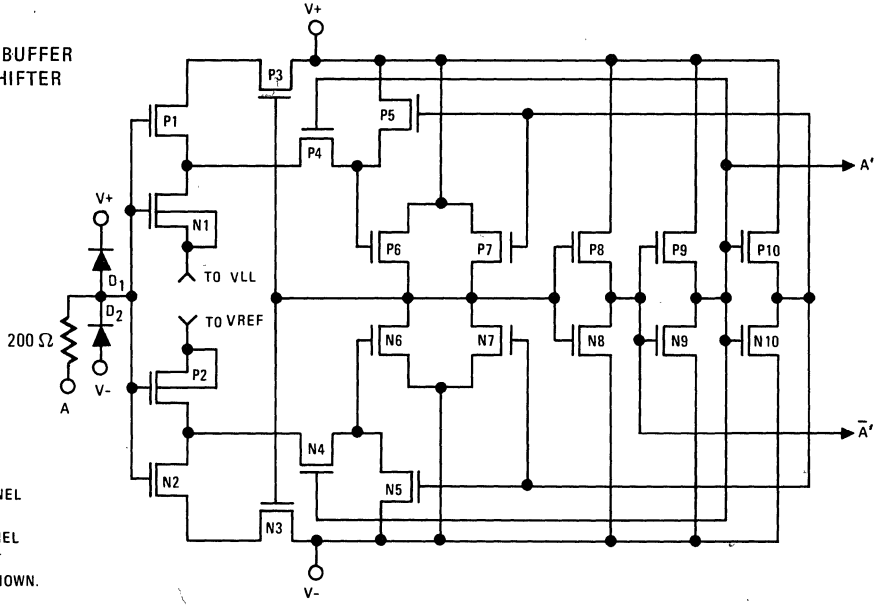
V-REF CELL



SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER



ALL N-CHANNEL
BODIES TO V-

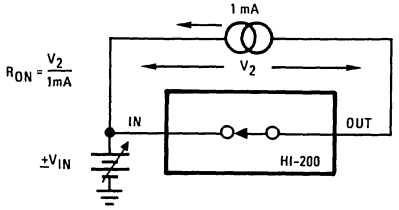
ALL P-CHANNEL
BODIES TO V+

EXCEPT AS SHOWN.

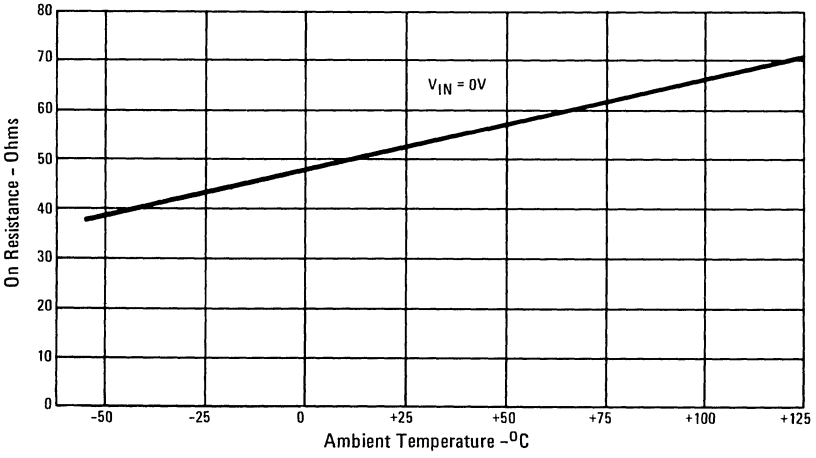
3

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 2.4V$ $V_{AL} = 0.8V$ AND V_{REF} = OPEN).

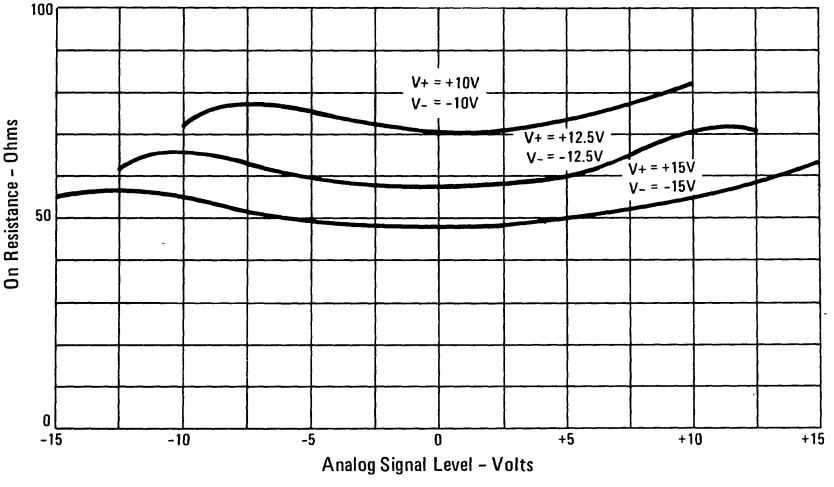
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



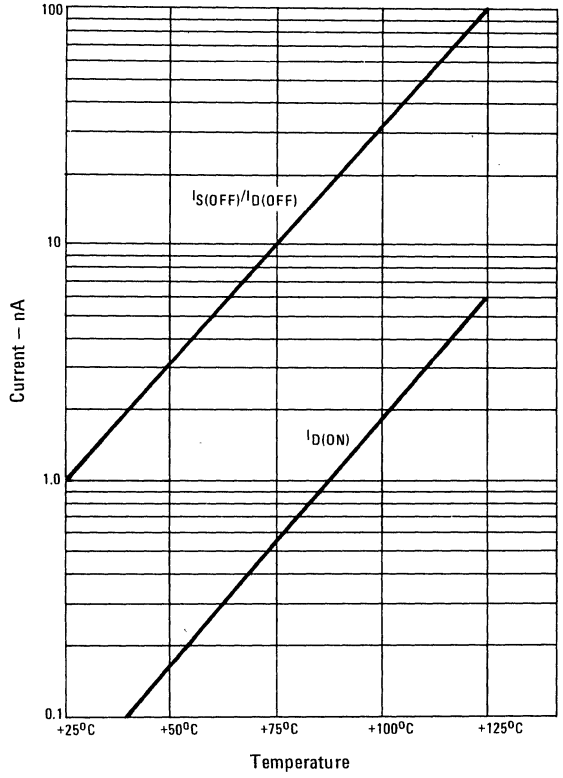
ON RESISTANCE vs. TEMPERATURE



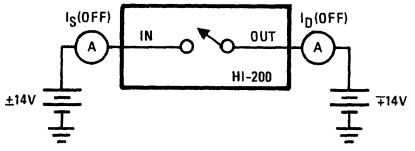
(HI-200)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE



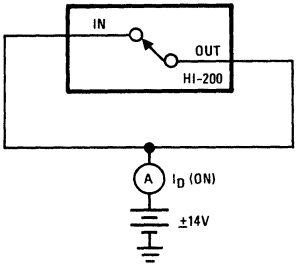
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-200)



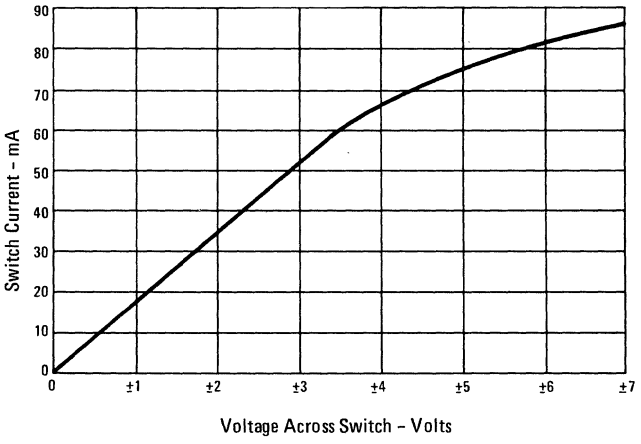
OFF LEAKAGE CURRENT vs. TEMPERATURE



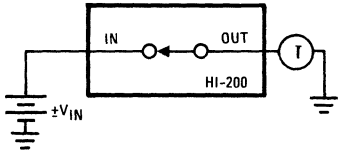
ON LEAKAGE CURRENT vs. TEMPERATURE



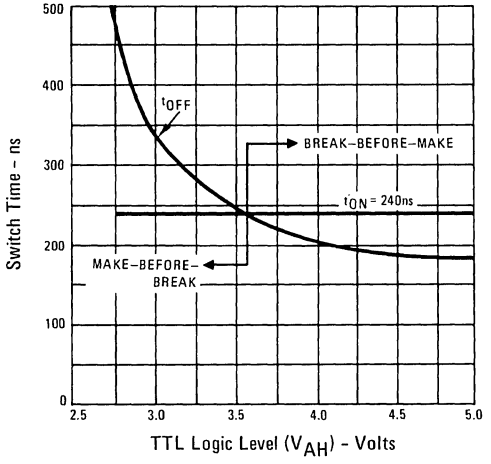
SWITCH CURRENT vs. VOLTAGE



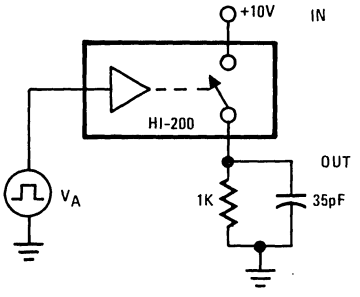
SWITCH CURRENT vs. VOLTAGE



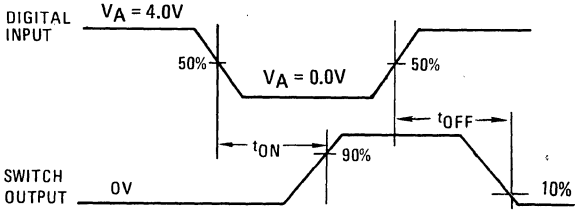
(HI-200)
SWITCH TIME vs. TTL LOGIC LEVEL



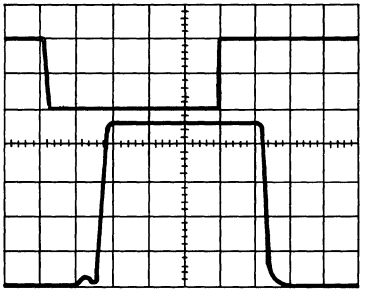
ON/OFF SWITCH TIME vs.
LOGIC LEVEL



SWITCHING WAVEFORMS

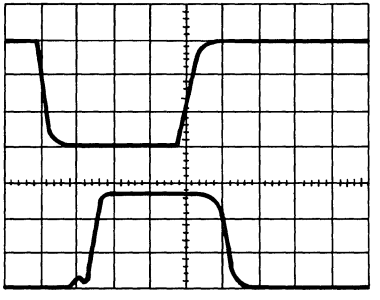


tON, tOFF (TTL INPUT)
VAH = +4.0V



Top: TTL Input Vertical: 2V/Div.
Bottom: Output Horizontal: 200ns/Div.

tON, tOFF(CMOS INPUT)
VREF = OPEN, VAH = +15V



Top: CMOS Input Vertical: 5V/Div.
Bottom: Output Horizontal: 200ns/Div.

HARRIS

HI-201

Quad SPST CMOS Analog Switch

3

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 185ns
- LOW R_{ON} 55 Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

HI-201 is a monolithic device comprising four independently selectable SPST switches which feature fast switching speeds (185ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-201 operates without any applications problems induced by latch-up or SCR-mode phenomena.

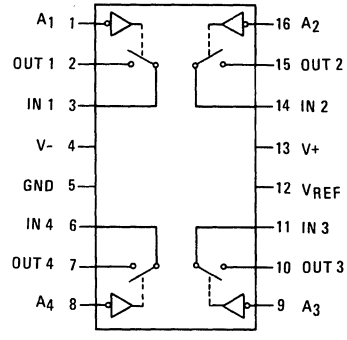
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-201 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and op amp gain switching networks.

HI-201 is available in a 16 lead dual-in-line package. HI-201-2 is specified from -55°C to +125°C while HI-201-5 operates from 0°C to +75°C. HI-201 is functionally and pin compatible with other available "200 series" switches.

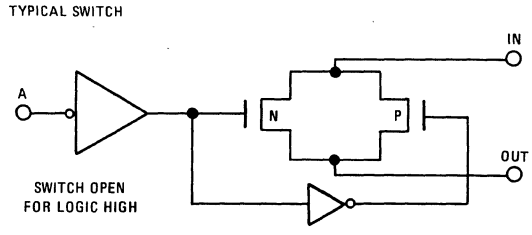
PIN OUT

Section 11 for Packaging

Top View



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 4 and 13	44V (±22)	Total Power Dissipation*	750mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	V_{Supply}(+) +4V	HI-201-2	-55°C to +125°C
	V_{Supply}(-) -4V	HI-201-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-201-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

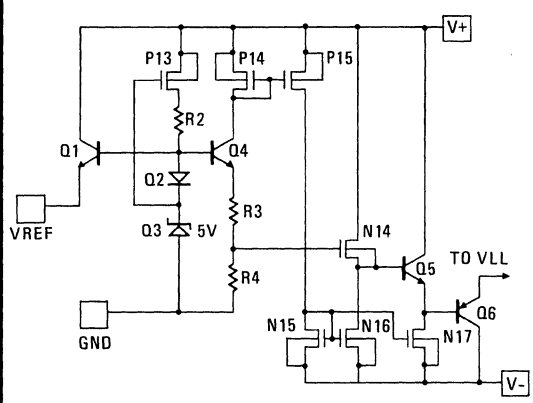
		HI-201-2 -55°C to +125°C			HI-201-5 ** 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		75	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current	+25°C		2			2		nA
(Note 6)	Full			500			250	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C		2			2		nA
(Note 6)	Full			500			250	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C		2			2		nA
	Full			500			250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	2.4			2.4			V
I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		30			30		ns
t_{on}, Switch ON Time	+25°C		185	500		185		ns
t_{off}, Switch OFF Time	+25°C		220	500		220		ns
"Off Isolation" (Note 4)	+25°C		80			80		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
I+, Current (Pin 13)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
I- Current (Pin 4)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = 5V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f = 100KHz
5. V_A = +3V or V_A = 0V For all Switches
6. Refer to leakage current measurement diagram on page (3-14)

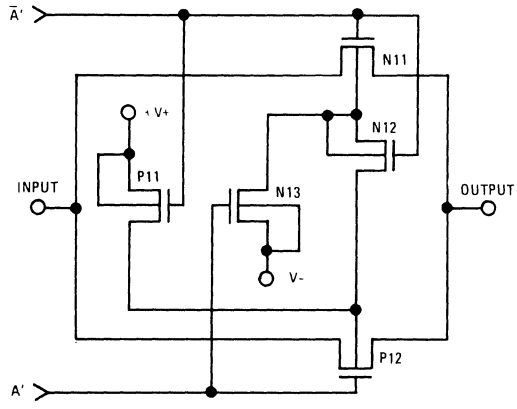
** Note: HI-201-4 has same specifications as HI-201-5 over the temperature range -20°C to +85°C.

TTL/CMOS
REFERENCE CIRCUIT

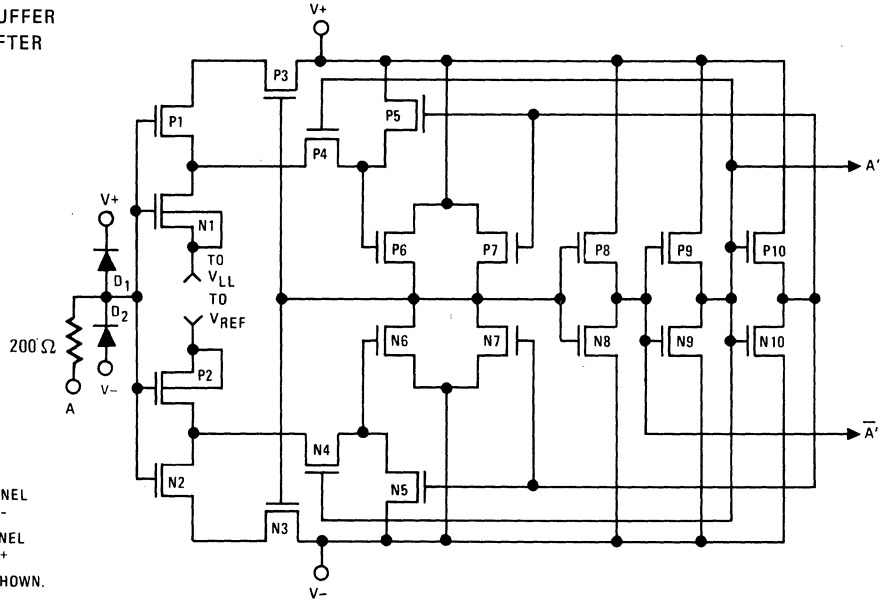
V-REF CELL



SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER



ALL N-CHANNEL
BODIES TO V-

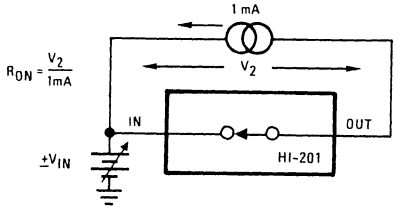
ALL P-CHANNEL
BODIES TO V+

EXCEPT AS SHOWN.

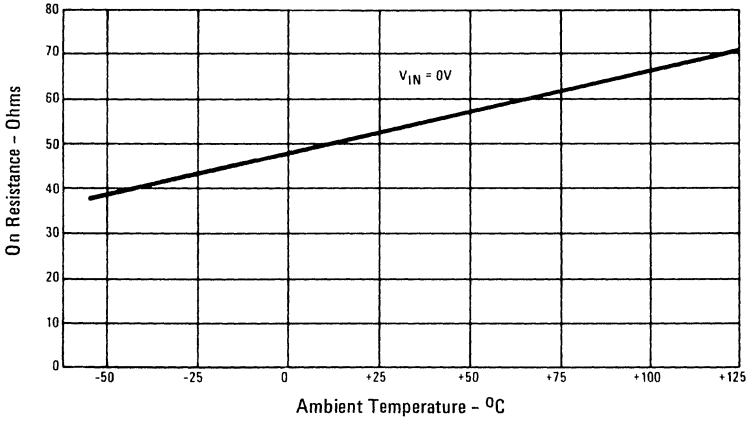
3

(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = 2.4\ V$ $V_{AL} = 0.8V$ AND V_{REF} = OPEN).

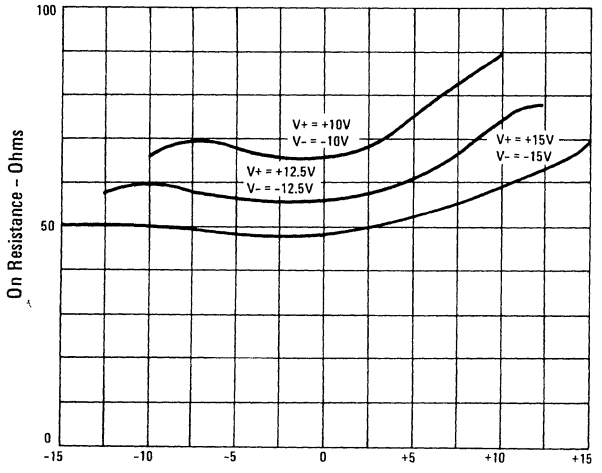
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE



ON RESISTANCE vs. TEMPERATURE

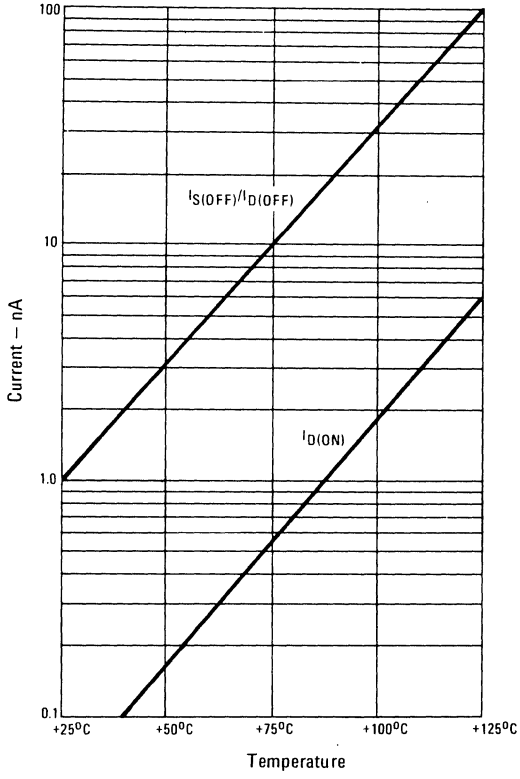


(HI-201)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE

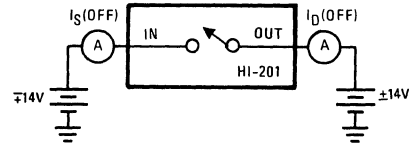


3

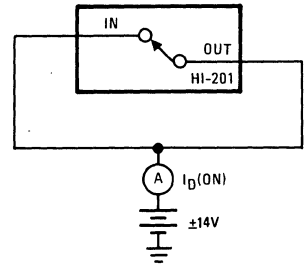
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-201)



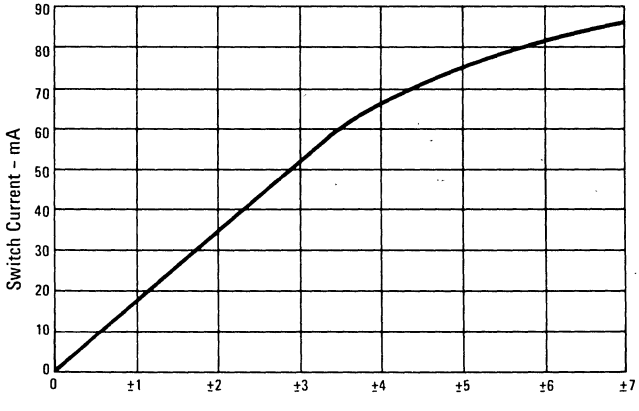
OFF LEAKAGE CURRENT vs. TEMPERATURE



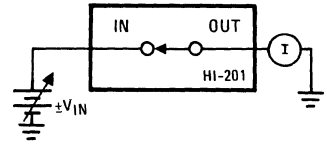
ON LEAKAGE CURRENT vs. TEMPERATURE

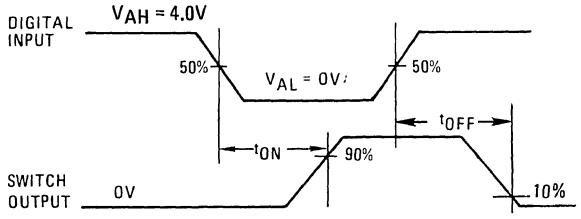


SWITCH CURRENT vs. VOLTAGE

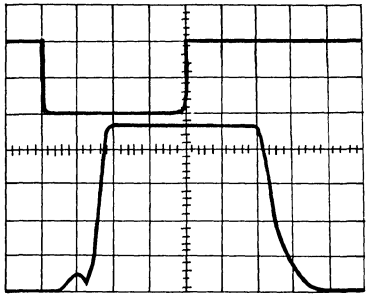


SWITCH CURRENT vs. VOLTAGE





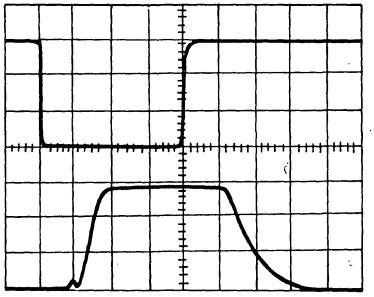
t_{ON}, t_{OFF}(TTL INPUT)
V_{IN} = 4.0V



Top: TTL Input
Bottom: Output

Horizontal: 100ns/Div.
Vertical: 2V/Div.

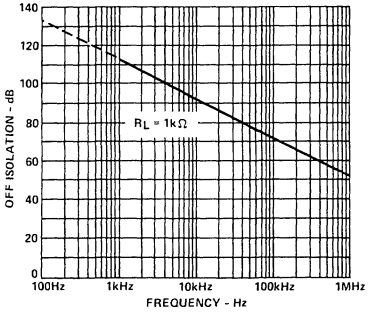
t_{ON}, t_{OFF}(CMOS INPUT)
V_{REF} = OPEN, V_{IN} = +15V



Top: CMOS Input
Bottom: Output

Vertical: 5V/Div.
Horizontal: 100ns/Div.

OFF ISOLATION VS. FREQUENCY



HARRIS

HI-201HS

High Speed Quad SPST CMOS Analog Switch

Preliminary

3

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 30ns
- LOW R_{ON} 30Ω
- LOW POWER DISSIPATION 120mW
- TTL COMPATIBLE
- LOW CHARGE INJECTION 10pC

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

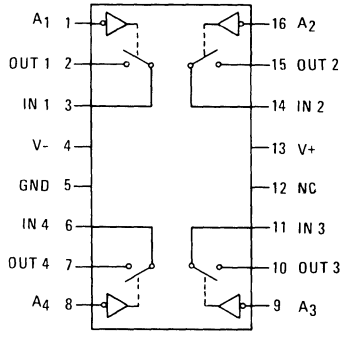
The Harris HI-201HS is a monolithic CMOS analog switch featuring very fast switching speeds and low ON resistance. The device consists of four independently selectable SPST switches and is identical in pinout to the HI-201 quad switch.

Fabricated using the Harris dielectric isolation technology, this TTL compatible device offers improved performance over previously available CMOS analog switches. Featuring switching speeds of 50ns max., low ON resistance of 50Ω max., and wide analog signal range of ±15V, the HI-201HS is designed for any application where improved switching performance, particularly switching speed, is required.

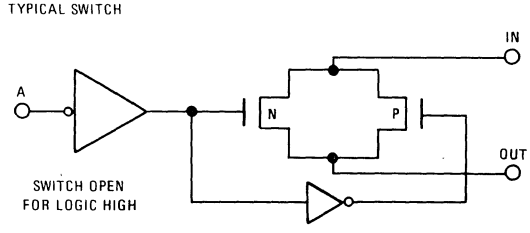
The HI-201HS is available in a 16 lead dual-in-line package. The HI-201HS-2 is specified for the temperature range of -55°C to +125°C and the HI-201HS-5 operates from 0°C to +75°C.

PIN OUT

Top View



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage Between Pins 4 and 13	+36V	Total Power Dissipation*	750mW
		Operating Temperature	
Digital Input Voltage:	V_{Supply}(+) +4V	HI-201HS-2	-55°C to +125°C
	V_{Supply}(-) -4V	HI-201HS-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-201HS-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified, Supplies = +15V, -15V; V_{AH} (Logic Level High) = 5.0V; V_{AL} (Logic Level Low) = +0.8V

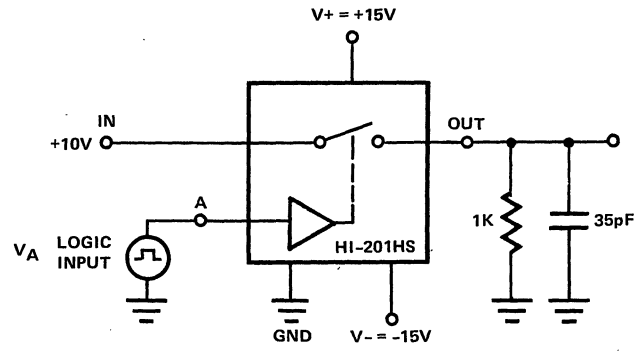
PARAMETER	TEMP.	HI-201HS-2 HI-201HS-5 MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS					
V_S, Analog Signal Range	Full	-15		+15	V
R_{ON}, On Resistance (Note 2)	+25°C		30	50	Ω
	Full			75	Ω
$I_{S(OFF)}$, Off Input Leakage Current	+25°C		.3	10	nA
	Full			100	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C		.3	10	nA
	Full			100	nA
$I_{D(ON)}$, On Leakage Current	+25°C		.1	10	nA
	Full			100	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold	Full			0.8	V
V_{AH}, Input High Threshold	+25°C	2.0			V
	Full	2.4			V
I_{AL}, Input Leakage Current (Low)	Full			500	μA
I_{AH}, Input Leakage Current (High)	Full			40	μA
SWITCHING CHARACTERISTICS					
t_{ON}, Switch ON Time (Note 3)	+25°C		30	50	ns
t_{OFF}, Switch OFF Time (Note 3)	+25°C		40	50	ns
"Off Isolation" (Note 4)	+25°C		72		dB
Crosstalk (Note 5)	+25°C		86		dB
Charge Injection (Note 6)	+25°C		10		pC
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		10		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		10		pF
$C_{D(ON)}$,	+25°C		30		pF
C_A, Digital Input Capacitance	+25°C		18		pF
$C_{DS(OFF)}$, Drain-to-Source Capacitance	+25°C		.5		pF
POWER REQUIREMENTS (Note 7)					
P_D, Power Dissipation	+25°C		120		mW
	Full			240	mW
I^+, Current (Pin 13)	+25°C		4.5		mA
	Full			10.0	mA
I^-, Current (Pin 4)	+25°C		3.5		mA
	Full			6	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $V_{OUT} = \pm 10V$, $I_{OUT} = 1mA$
3. $R_L = 1k\Omega$, $C_L = 35pF$, $V_{IN} = +10V$, $V_A = +5V$
4. $V_A = 5V$, $R_L = 1K\Omega$, $C_L = 10pF$, $V_S = 3$ VRMS, f = 100kHz
5. $V_A = 5V$, $R_L = 1k\Omega$, f = 100kHz, $V_{IN} = 2V_{p-p}$
6. $C_L = 1000pF$, $V_{IN} = 0V$, $R_{IN} = 0\Omega$ $\Delta Q = C_L \times \Delta V_O$
7. $V_A = 5V$ or $V_A = 0$ for all switches.

TEST CIRCUIT

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})



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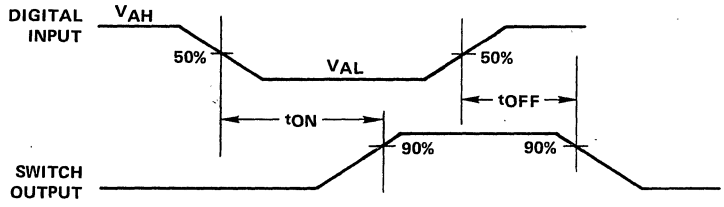
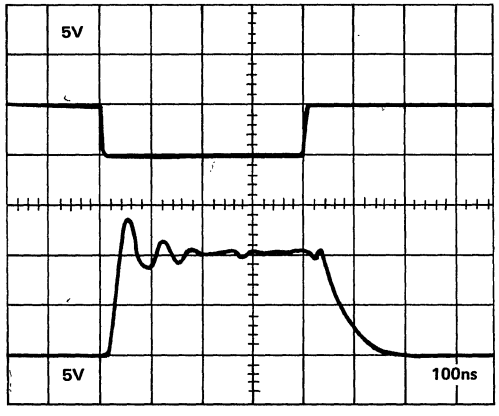
SWITCHING WAVEFORMS



t_{ON}, t_{OFF} (TTL INPUT)
V_{AH} = +5.0V



Top: TTL Input
Bottom: Output

Vertical: 5V/Div.
Horizontal: 100ns/Div.

HARRIS

HI-300 thru HI-307

CMOS Analog Switches

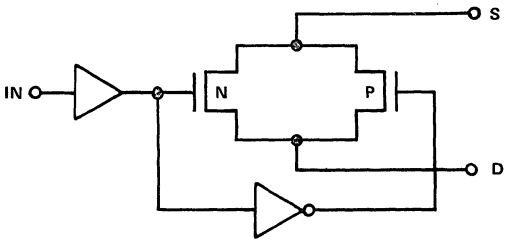
FEATURES

- ANALOG SIGNAL RANGE (±15V SUPPLIES) ±15V
- LOW LEAKAGE (TYP. @ 25°C) 40pA
- LOW LEAKAGE (TYP. @ 125°C) 1nA
- LOW ON RESISTANCE (TYP. @ 25°C) 35Ω
- BREAK-BEFORE-MAKE DELAY (TYP.) 60ns
- CHARGE INJECTION 30pC
- TTL, CMOS COMPATIBLE
- SYMETRICAL SWITCH ELEMENTS
- LOW OPERATING POWER 1.0mW
  (TYP. FOR HI-300 - 303)

APPLICATIONS

- SAMPLE AND HOLD i.e. LOW LEAKAGE SWITCHING
- OP AMP GAIN SWITCHING i.e. LOW ON RESISTANCE
- PORTABLE, BATTERY OPERATED CIRCUITS
- LOW LEVEL SWITCHING CIRCUITS
- DUAL OR SINGLE SUPPLY SYSTEMS

FUNCTIONAL DIAGRAM



TYPICAL SWITCH 300 SERIES

DESCRIPTION

The HI-300 through HI-307 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These switches feature break-before-make switching, (HI-301, 303, 305 & 307 only) , low and nearly constant ON resistance over the full analog signal range, and low power dissipation, (a few milliwatts for the HI-300-303, a few hundred microwatts for the HI-304-307).

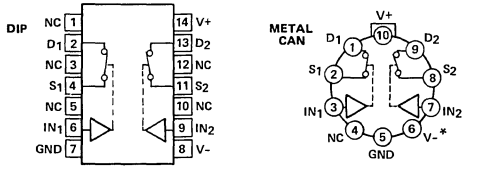
The HI-300-303 are TTL compatible and have a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4.0V. The HI-304-307 switches are CMOS compatible and have a low state with an input less than 3.5V and a high state with an input greater than 11V. (See pinouts for switch conditions with a logic "1" input.)

All the devices are available in a 14 pin epoxy or ceramic DIP. The HI-300, 301, 304 and 305 are also available in a 10 pin metal can. Each of the switch types are available in either the -55°C to +125°C or 0°C to +75°C operating ranges.

PINOUTS (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

Section 11 for Packaging

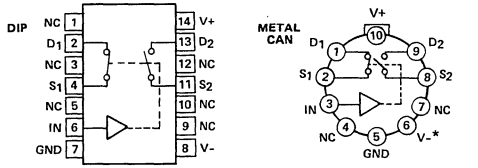
DUAL SPST HI-300 & HI-304
(TOP VIEWS)



LOGIC	SWITCH
0	OFF
1	ON

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

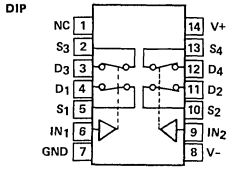
SPDT HI-301 & HI-305
(TOP VIEWS)



LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

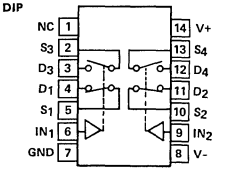
*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-302 & HI-306
(TOP VIEW)



LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT HI-303 & HI-307
(TOP VIEW)



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between Supplies	44V (±22V)
Digital Input Voltage	V^+ +4.0V V^- -4.0V
Analog Input Voltage	V^+ 1.5V V^- 1.5V

Total Power Dissipation

14 Pin Epoxy DIP	526mW
14 Pin Ceramic DIP	588mW
10 Pin Metal Can*	435mW

*Derate 6.9mW/0°C Above T_A = 70°C

Operating Temperature	HI-3XX-2	-55°C to +125°C
	HI-3XX-5	0°C to +75°C
Storage Temperature		-65°C to +150°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified; Supplies = +15V, -15V; V_{IN} = Logic Input.
HI-300-303 : V_{IN} - for Logic "1" = 4V, for Logic "0" = 0.8V
HI-304-307 : V_{IN} - for Logic "1" = 11V, for Logic "0" = 3.5V

PARAMETER	TEMP	-55°C to +125°C MIN	-55°C to +125°C TYP	-55°C to +125°C MAX	0°C to +75°C MIN	0°C to +75°C TYP	0°C to +75°C MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON} ON Resistance (Note 2)	+25°C		35	50		35	50	Ω
	Full		40	75		40	75	Ω
IS_{OFF} OFF Input Leakage Current (Note 3)	+25°C		0.04	1		0.04	5	nA
	Full		1	100		0.2	100	nA
ID_{OFF} OFF Output Leakage Current (Note 3)	+25°C		0.04	1		0.04	5	nA
	Full		1	100		0.2	100	nA
ID_{ON} ON Leakage Current (Note 4)	+25°C		0.03	1		0.03	5	nA
	Full		0.5	100		0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL} Input Low Level *	Full			0.8			0.8	V
V_{INH} Input High Level *	Full	4			4			V
V_{INL} Input Low Level **	Full			3.5			3.5	V
V_{INH} Input High Level **	Full	11			11			V
I_{INL} Input Leakage Current (Low) (Note 5)	Full			1			1	μA
I_{INH} Input Leakage Current (High) (Note 5)	Full			1			1	μA
SWITCHING CHARACTERISTICS								
t_{OPEN} Break-Before-Make Delay ***	+25°C		60			60		ns
t_{ON} Switch On Time *	+25°C		210	300		210	300	ns
t_{OFF} Switch Off Time *	+25°C		160	250		160	250	ns
t_{ON} Switch On Time **	+25°C		160	250		160	250	ns
t_{OFF} Switch Off Time **	+25°C		100	150		100	150	ns
Off Isolation (Note 6)	+25°C		60			60		dB
Charge Injection (Note 7)	+25°C		3			3		mV
CS_{OFF} Input Switch Capacitance	+25°C		16			16		pF
CD_{OFF} Output Switch Capacitance	+25°C		14			14		pF
CD_{ON} Output Switch Capacitance	+25°C		35			35		pF
C_{IN} (High) Digital Input Capacitance	+25°C		5			5		pF
C_{IN} (Low) Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
I+ Current * (Note 8)	+25°C		0.09	0.5		0.09	0.5	mA
	Full			1			1	mA
I- Current * (Note 8)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current * (Note 9)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current * (Note 9)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current ** (Note 10)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current ** (Note 10)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I+ Current ** (Note 11)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA
I- Current ** (Note 11)	+25°C		0.01	10		0.01	100	μA
	Full			100				μA

* HI-300 thru HI-303 Only; ** HI-304 thru HI-307 Only; *** HI-301, HI-303, HI-305, HI-307 Only

ELECTRICAL CHARACTERISTICS NOTES:

1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.
2. $V_S = \pm$ 10V, I_{OUT} = -10mA On resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V, V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1k. $C_L = C_{FIXTURE} + C_{PROBE}$, "Off Isolation" = 20logV_S/V_D.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. (HI-300 -303) Switches are symmetrical; S and D may be interchanged. Logic Drive = 15V (HI-304-307)
8. V_{IN} = 4V (one input) (all other inputs = 0V)
9. V_{IN} = 0.8V (all inputs).
10. V_{IN} = 15V (all inputs).
11. V_{IN} = 0V (all inputs).
12. To drive from DTL/TTL circuits, pull-up resistors to +5V supply are recommended.

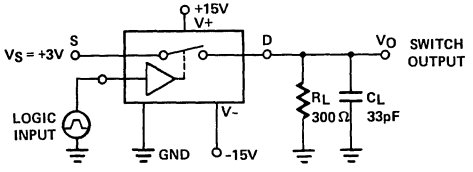
TEST CIRCUITS

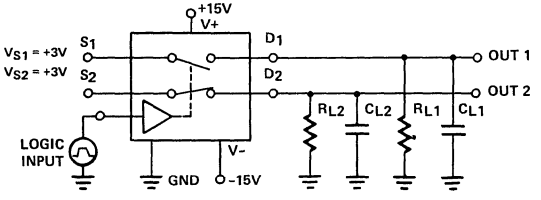
SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

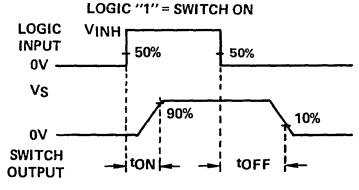
SWITCH TYPE	V_{INH}
HI-300 thru HI-303	4V
HI-304 thru HI-307	15V

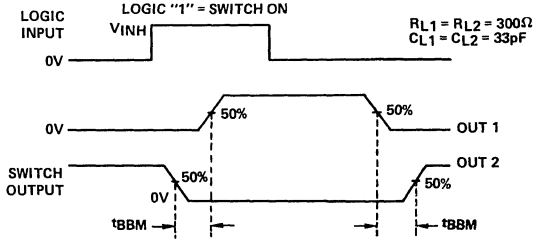
BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

SWITCH TYPE	V_{INH}
HI-301, HI-303	5V
HI-305, HI-307	15V



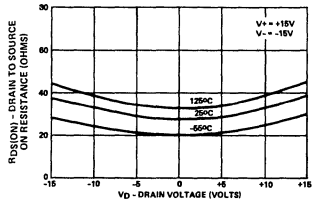




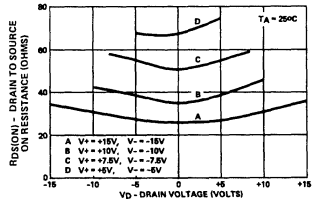


TYPICAL PERFORMANCE CURVES

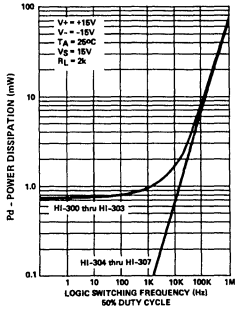
$R_{DS(ON)}$ VS. V_D AND TEMPERATURE



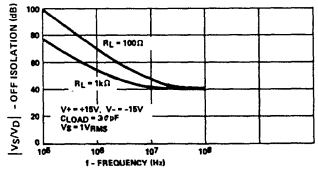
$R_{DS(ON)}$ VS. V_D AND POWER SUPPLY VOLTAGE



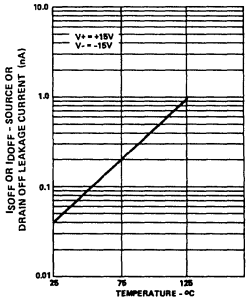
DEVICE POWER DISSIPATION VS. SWITCHING FREQUENCY SINGLE LOGIC INPUT



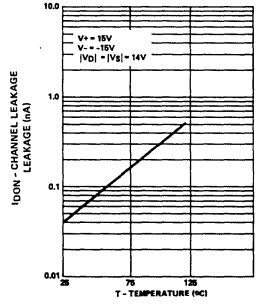
OFF ISOLATION VS. FREQUENCY



$I_{S(OFF)}$ OR $I_{D(OFF)}$ VS. TEMPERATURE *

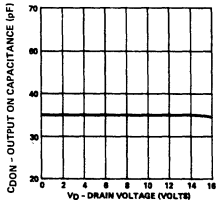


$I_{D(ON)}$ VS. TEMPERATURE *

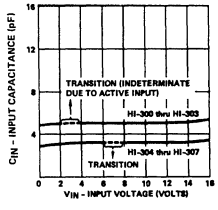


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

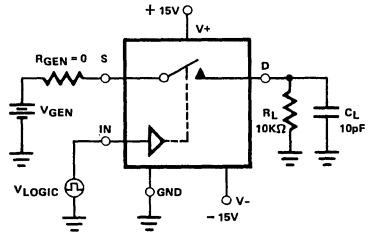
OUTPUT ON CAPACITANCE VS. DRAIN VOLTAGE



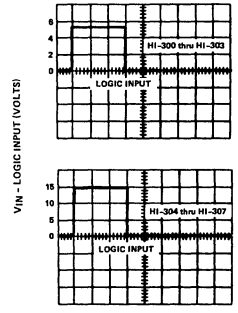
DIGITAL INPUT CAPACITANCE VS. INPUT VOLTAGE

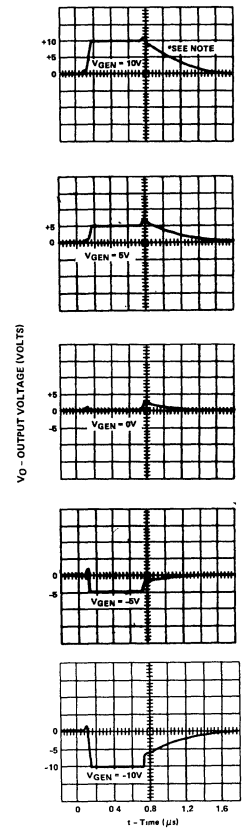


Typical delay, rise, fall, settling times, and switching transients in this circuit.

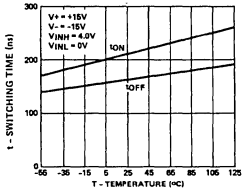


If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

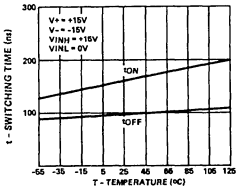




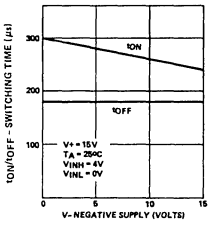
SWITCHING TIME VS. TEMPERATURE HI-300 thru HI-303



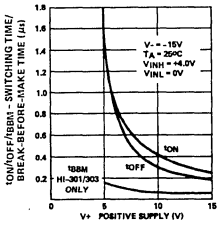
SWITCHING TIME VS. TEMPERATURE HI-304 thru HI-307



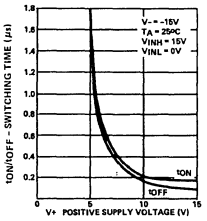
SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-300 thru HI-303



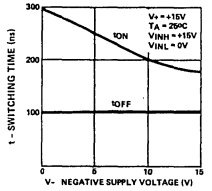
SWITCHING TIME AND BREAK BEFORE MAKE TIME VS. POSITIVE SUPPLY VOLTAGE HI-300 thru HI-303



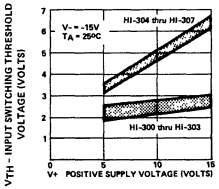
SWITCHING TIME VS. POSITIVE SUPPLY VOLTAGE HI-304 thru HI-307



SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-304 thru HI-307



INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-300 thru HI-307



3

HARRIS

HI-381/384/ 387/390

CMOS Analog Switches

FEATURES

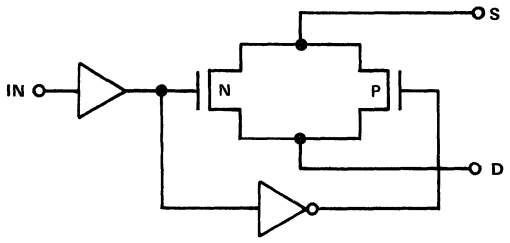
- ANALOG SIGNAL RANGE (±15V SUPPLIES) ±15V
- LOW LEAKAGE (TYP. @ 25°C) 40pA
- LOW LEAKAGE (TYP @ 125°C) 1nA
- LOW ON RESISTANCE (TYP. @ 25°C) 35Ω
- BREAK-BEFORE-MAKE DELAY (TYP.) 60ns
- CHARGE INJECTION 30pC
- TTL COMPATIBLE
- SYMMETRICAL SWITCH ELEMENTS
- LOW OPERATING POWER (TYP.) 1.0mW

APPLICATIONS

- SAMPLE AND HOLD i.e. LOW LEAKAGE SWITCHING
- OP AMP GAIN SWITCHING i.e. LOW ON RESISTANCE
- PORTABLE BATTERY OPERATED CIRCUITS
- LOW LEVEL SWITCHING CIRCUITS
- DUAL OR SINGLE SUPPLY SYSTEMS

3

FUNCTIONAL DIAGRAM



TYPICAL SWITCH - 300 SERIES

DESCRIPTION

The HI-381 through HI-390 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These devices are TTL compatible and are available in four switching configurations. (See device pinout for particular switching function with a logic "1" input.)

These switches feature low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

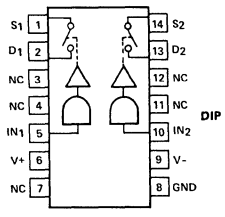
The HI-381 and HI-387 switches are available in a 14 pin epoxy or ceramic DIP or10 pin metal can. The HI-384 and HI-390 are available in a 16 pin epoxy or ceramic DIP. Each of the individual switch types are available in the -55°C to +125°C and 0°C to +75°C operating ranges.

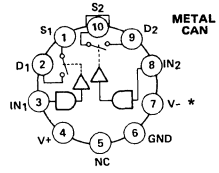
PINOUTS (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

Section 11 for Packaging

DUAL SPST HI-381

(TOP VIEWS)



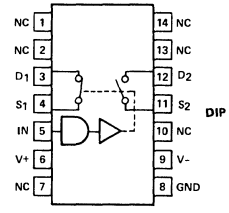


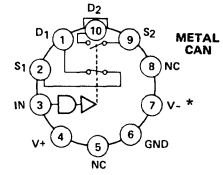
LOGIC	SW 1 SW 2
0	ON
1	OFF

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

SPDT HI-387

(TOP VIEWS)



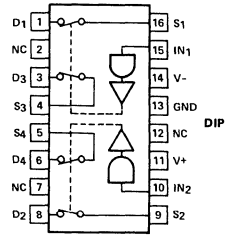


LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-384

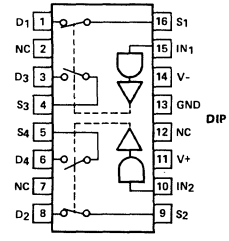
(TOP VIEW)



LOGIC	SW 1 - 4
0	OFF
1	ON

DUAL SPDT HI-390

(TOP VIEW)



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between Supplies 44V (±22)

Digital Input Voltage
V^++4.0V
V^- -4.0V

Analog Input Voltage
V^++1.5V
V^- -1.5V

Storage Temperature Range -65°C to +150°C

Total Power Dissipation

14 Pin Epoxy DIP	526mW
14 Pin Ceramic DIP	588mW
16 Pin Epoxy DIP	625mW
16 Pin Ceramic DIP	685mW
10 Pin Metal Can*	435mW

*Derate 6.9mW/°C above T_A = 70°C

Operating Temperature

HI-3XX-2	-55°C to +125°C
HI-3XX-5	0°C to +75°C

ELECTRICAL CHARACTERISITICS

Unless otherwise specified; Supplies = +15V, -15V; VIN = Logic Input, VIN for logic "1" = 4V, for logic 0 = .8V

		-55°C to +125°C			0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	FULL	-15		+15	-15		+15	V
R_{ON} ON Resistance (Note 2)	+25°C		35	50		35	50	Ω
	FULL		40	75		40	75	Ω
IS_{OFF} OFF Input Leakage Current (Note 3)	+25°C		.04	1		.04	5	nA
	FULL		1	100		0.2	100	nA
ID_{OFF} OFF Output Leakage Current	+25°C		.04	1		.04	5	nA
(Note 3)	FULL		1	100		0.2	100	nA
ID_{ON} ON Leakage Current (Note 4)	+25°C		.03	1		.03	5	nA
	FULL		0.5	100		0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL} Input Low Level	FULL			.8			.8	V
V_{INH} Input High Level	FULL	4			4			V
I_{INH} Input Leak. Current (High) (Note 5)	FULL			1			1	μA
I_{INL} Input Leak. Current (Low) (Note 5)	FULL			1			1	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay (HI-387/390 only)	+25°C		60			60		ns
t_{ON}, Switch ON Time	+25°C		210	300		210	300	ns
t_{OFF}, Switch OFF Time	+25°C		160	250		160	250	ns
OFF Isolation (Note 6)	+25°C		60			60		dB
Charge Injection (Note 7)	+25°C		3			3		mV
CS_{OFF} Input Switch Capacitance	+25°C		16			16		pF
CD_{OFF} Output Switch Capacitance	+25°C		14			14		pF
CD_{ON} Output Switch Capacitance	+25°C		35			35		pF
C_{IN} (High) Digital Input Capacitance	+25°C		5			5		pF
C_{IN} (Low) Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
I+ Current (Note 8)	+25°C		.09	.5		.09	.5	mA
	FULL			1			1	mA
I- Current (Note 8)	+25°C		.01	10		.01	100	μA
	FULL			100				μA
I+ Current (Note 9)	+25°C		.01	10		.01	100	μA
	FULL			100				μA
I- Current (Note 9)	+25°C		.01	10		.01	100	μA
	FULL			100				μA

3

ELECTRICAL CHARACTERISTICS NOTES :

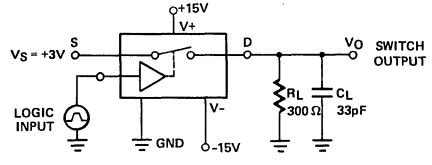
1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.
2. $V_S = \pm 10V$, $I_{OUT} = -10mA$ on resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V$, $V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, $C_L = 15pF$, $R_L = 1k$, $C_L = C_{FIXTURE} + C_{PROBE}$, "off isolation" = $20\log V_S/V_D$.
7. $V_S = 0V$, $C_L = 10{,}000pF$, Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged.
8. $V_{IN} = 4V$. (one input) (all other inputs = 0)
9. $V_{IN} = 0.8V$. (all inputs)
10. To drive from DTL/TTL circuits, pull-up resistors to +5V Supply are recommended.

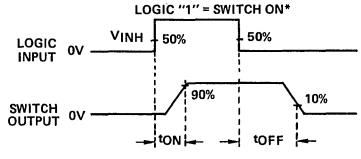
TEST CIRCUITS

3

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

SWITCH TYPE	V_{INH}
HI-381 thru HI-390	5V

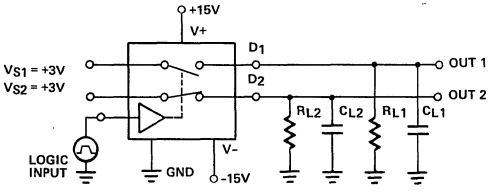


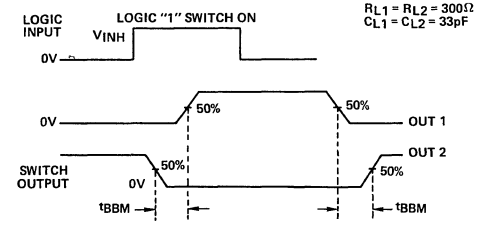


*Inverted logic for HI-381

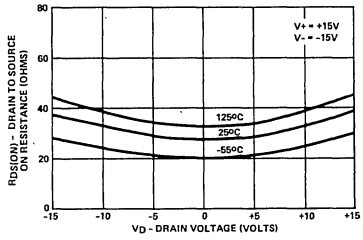
BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

SWITCH TYPE	V_{INH}
HI-387 and HI-390	5V

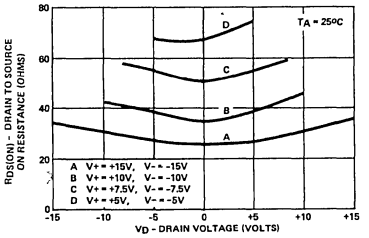




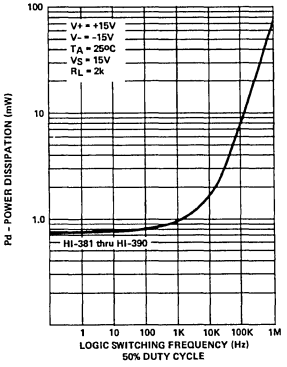
$R_{DS(ON)}$ VS. V_D AND TEMPERATURE



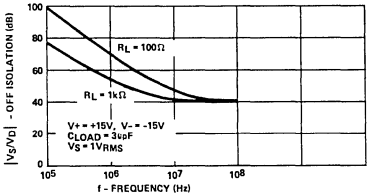
$R_{DS(ON)}$ VS. V_D AND POWER SUPPLY VOLTAGE



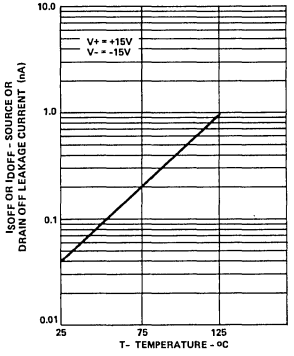
DEVICE POWER DISSIPATION VS. SWITCHING FREQUENCY SINGLE LOGIC INPUT



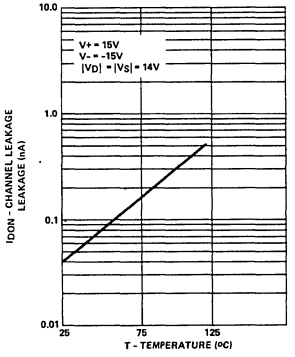
OFF ISOLATION VS. FREQUENCY



I_{SOFF} OR I_{DOFF} VS. TEMPERATURE*

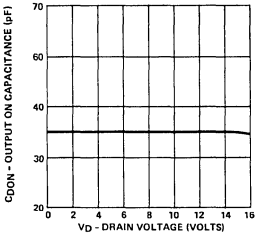


I_{DON} VS. TEMPERATURE*

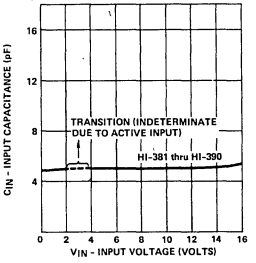


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

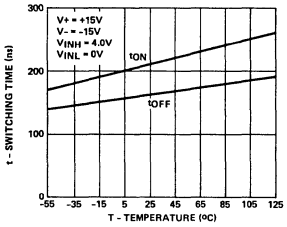
OUTPUT ON CAPACITANCE VS. DRAIN VOLTAGE



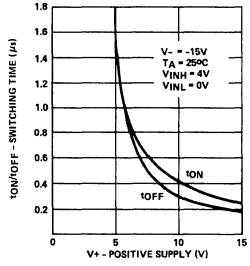
DIGITAL INPUT CAPACITANCE VS. INPUT VOLTAGE



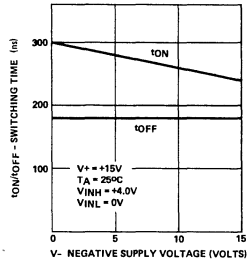
SWITCHING TIME VS. TEMPERATURE HI-381 thru HI-390



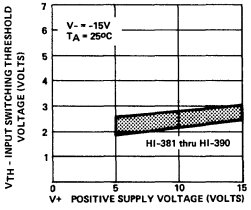
SWITCHING TIME VS. POSITIVE SUPPLY VOLTAGE HI-381 thru HI-390



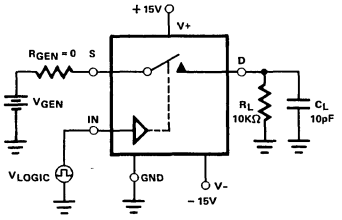
SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-381 thru HI-390



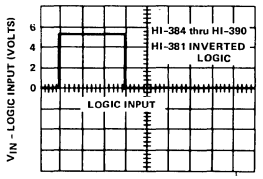
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-381 thru HI-390

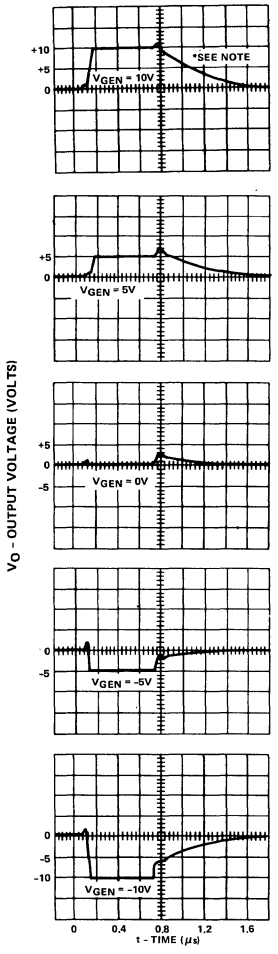


Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.





* NOTE: The turn-off time is primarily limited here by the RC time constant (100ns) of the load.

HI-5040 thru HI-5051
HI-5046A and
HI-5047A

CMOS Analog Switches

FEATURES

- WIDE ANALOG SIGNAL RANGE ±15V
- LOW "ON" RESISTANCE (TYP) 25Ω
- HIGH CURRENT CAPABILITY (TYP) 80mA
- BREAK-BEFORE-MAKE SWITCHING
  - TURN-ON TIME (TYP) 370ns
  - TURN-OFF TIME (TYP) 280ns
- NO LATCH-UP
- INPUT MOS GATES ARE PROTECTED FROM ELECTROSTATIC DISCHARGE
- DTL, TTL, CMOS, PMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY SWITCHING
- SAMPLE AND HOLD
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING

DESCRIPTION

This family of CMOS analog switches offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25 ohms for HI-5048 through HI-5051 and HI-5046A/5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at 25°C). This family of switches also features very low power operation (1.5mW at 25°C).

There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional diagram). All devices are available in 16 pin D.I.P. packages. The HI-5040/5050 switches can directly replace IH-5040 series devices and are functionally compatible with the DG 180/190 family. Each switch type is available in the -55°C to +125°C and 0°C to +75°C performance grades.

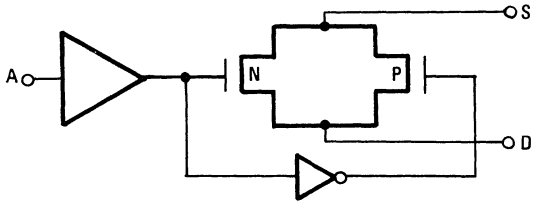
FUNCTIONAL DESCRIPTION

Section 11 for Packaging

PART NUMBER	TYPE	R_{ON}
HI-5040	SPST	75Ω
HI-5041	DUAL SPST	75Ω
HI-5042	SPDT	75Ω
HI-5043	DUAL SPDT	75Ω
HI-5044	DPST	75Ω
HI-5045	DUAL DPST	75Ω
HI-5046	DPDT	75Ω
HI-5046A	DPDT	30Ω
HI-5047	4PST	75Ω
HI-5047A	4PST	30Ω
HI-5048	DUAL SPST	30Ω
HI-5049	DUAL DPST	30Ω
HI-5050	SPDT	30Ω
HI-5051	DUAL SPDT	30Ω

FUNCTIONAL DIAGRAM

TYPICAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$)	36V	Analog Current (S to D)	80mA
V_R to Ground	V^+, V^-	Total Power Dissipation*	450mW
Digital and Analog	$V^+ + 4V$	Operating Temperature	
Input Voltage	$V^- - 4V$	HI-50XX-2	-55^oC to $+125^oC$
		HI-50XX-5	0^oC to $+75^oC$
		Storage Temperature	-65^oC to $+150^oC$

*Derate 6mW/^{o}C above $T_A = 75^oC$

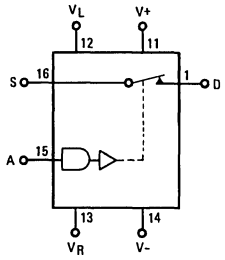
ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 3.0V; V_{AL} (Logic Level Low) = +0.8V, V_L = +5V
For Test Conditions, consult Performance Characteristics

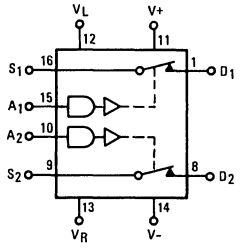
		-55°C to +125°C			0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15		+15	-15		+15	V
Ron, "ON" Resistance (Note 1a)	+25°C		50			50		Ω
	Full			75			75	Ω
Ron, "ON" Resistance (Note 1b)	+25°C		25			25		Ω
	Full			50			50	Ω
Ron, Channel-to-Channel Match (Note 1a)	+25°C		2	10		2	10	Ω
Ron, Channel-to-Channel Match (Note 1b)	+25°C		1	5		1	5	Ω
$I_{S(OFF)} = I_{D(OFF)}$, Off Input or Output	+25°C		0.8			0.8		nA
Leakage Current	Full		100	500		100	500	nA
$I_{D(ON)}$, On Leakage Current	+25°C		0.01			0.01		nA
	Full		2	500		2	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
I_A, Input Leakage Current (High or Low)	Full		.01	1.0		.01	1.0	μA
SWITCHING CHARACTERISTICS								
t_{on}, Switch "ON" Time	+25°C		370	1000		370	1000	ns
t_{off}, Switch "OFF" Time	+25°C		280	500		280	500	ns
Charge Injection (Note 2)	+25°C		5	20		5		mV
"OFF Isolation" (Note 3)	+25°C	75	80			80		dB
"Crosstalk" (Note 3)	+25°C	80	88			88		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		11			11		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		11			11		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS								
P_D, Quiescent Power Dissipation	+25°C		1.5			1.5		mW
I^+, +15V Quiescent Current	Full			0.3			0.5	mA
I^-, -15V Quiescent Current	Full			0.3			0.5	mA
I_L, +5V Quiescent Current	Full			0.3			0.5	mA
I_R, Gnd Quiescent Current	Full			0.3			0.5	mA

NOTES: 1. $V_{OUT} = \pm 10V$, $I_{OUT} = 1mA$
a) For HI-5040 thru HI-5047
b) For HI-5048 thru HI-5051, HI-5046A/5047A
2. $V_{IN} = 0V$, $C_L = 10{,}000pF$
3. $R_L = 100\Omega$, f= 100 KHz, $V_{IN} = 2\ V_{PP}$, $C_L = 5pF$

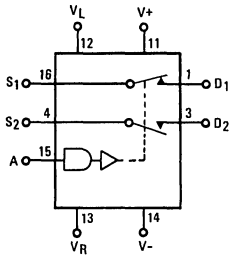
SPST
HI-5040 (75Ω)



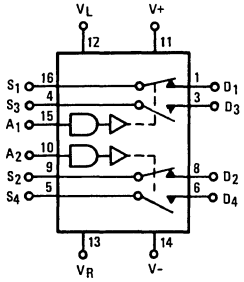
DUAL SPST
HI-5041 (75Ω)



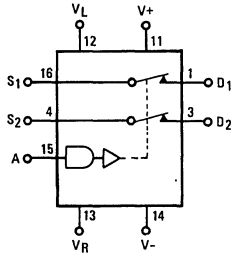
SPDT
HI-5042 (75Ω)



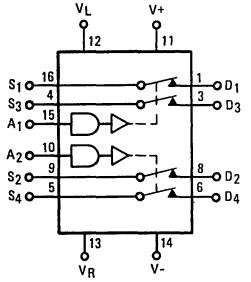
DUAL SPDT
HI-5043 (75Ω)



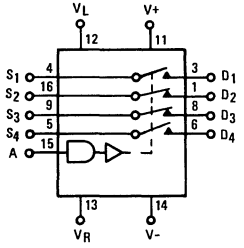
DPST
HI-5044 (75Ω)



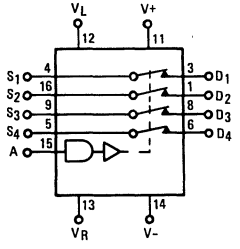
DUAL DPST
HI-5045 (75Ω)



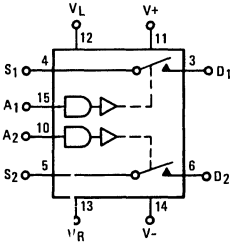
DPDT
HI-5046 (75Ω)
HI-5046A (30Ω)



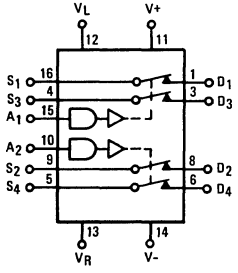
4PST
HI-5047 (75Ω)
HI-5047A (30Ω)



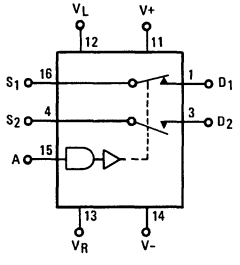
DUAL SPST
HI-5048 (30Ω)



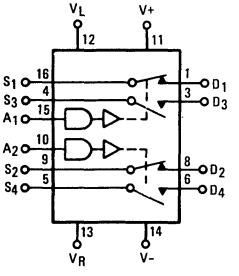
DUAL DPST
HI-5049 (30Ω)



SPDT
HI-5050 (30Ω)



DUAL SPDT
HI-5051 (30Ω)



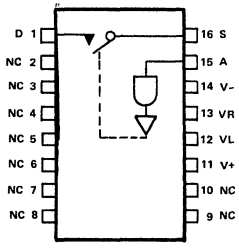
3

PIN CONFIGURATIONS

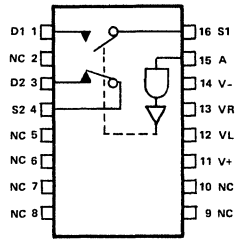
SWITCH STATES ARE FOR LOGIC "0" INPUT

SINGLE CONTROL

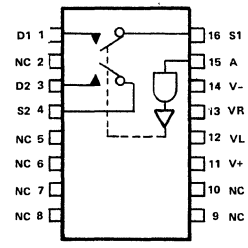
SPST
HI-5040 (75Ω)



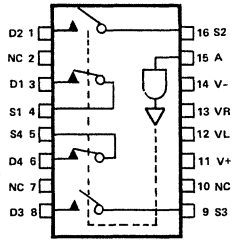
SPDT
HI-5042 (75Ω)
HI-5050 (25Ω)



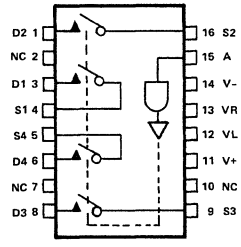
DPST
HI-5044 (75Ω)



DPDT
HI-5046 (75Ω)
HI-5046A (25Ω)

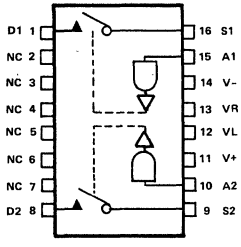


4 SPST
HI-5047 (75Ω)
HI-5047A (25Ω)

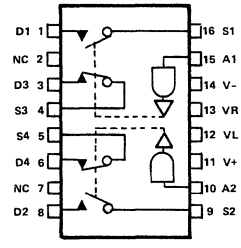


DUAL CONTROL

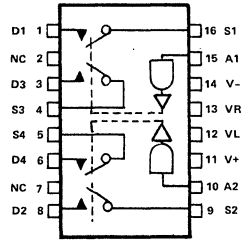
DUAL SPST
HI-5041 (75Ω)



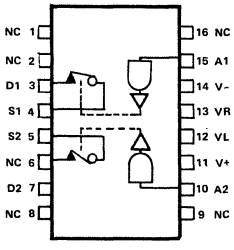
DUAL SPDT
HI-5043 (75Ω)
HI-5051 (25Ω)



DUAL DPST
HI-5045 (75Ω)
HI-5049 (25Ω)

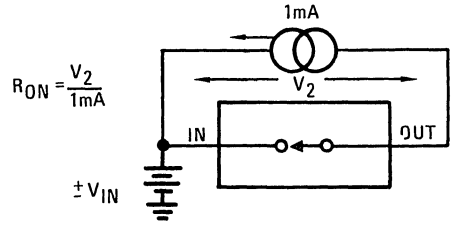


DUAL SPST
HI-5048 (25Ω)

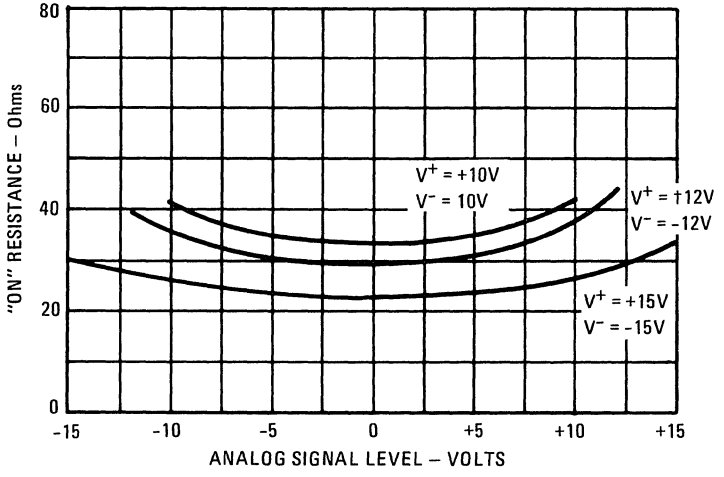


(UNLESS OTHERWISE SPECIFIED $T_A = 25^oC$, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$, $V_R = 0V$, $V_{AH} = 3.0V$ and $V_{AL} = 0.8V$

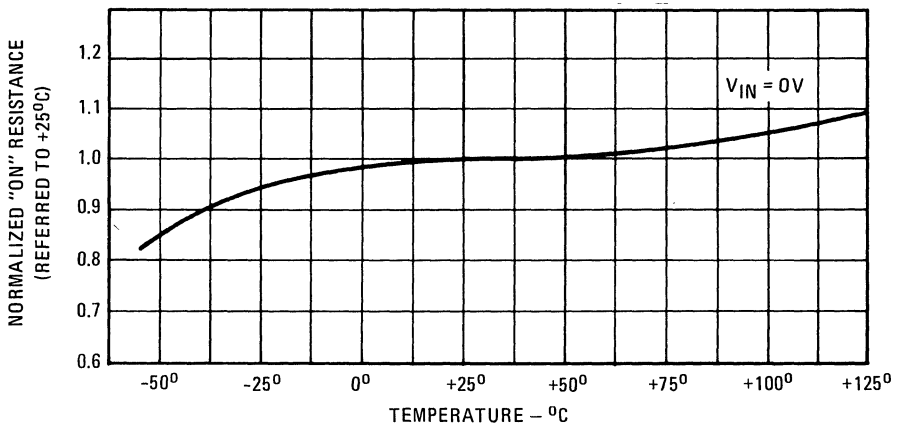
ON RESISTANCE vs. ANALOG SIGNAL LEVEL,
SUPPLY VOLTAGE AND TEMPERATURE

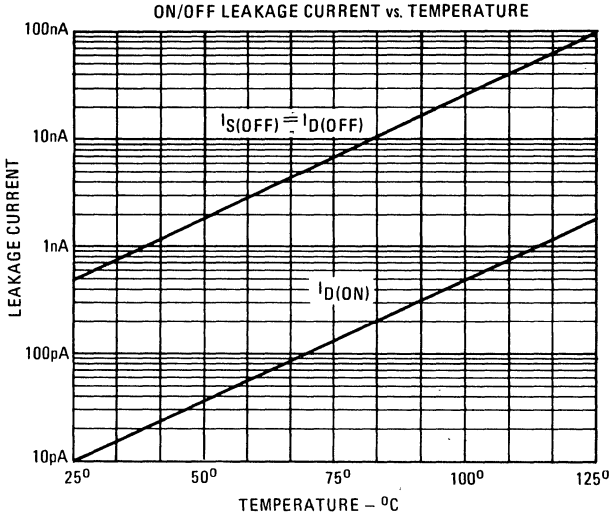


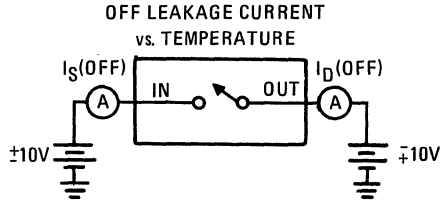
"ON"' RESISTANCE vs. ANALOG SIGNAL LEVEL
AND POWER SUPPLY VOLTAGE

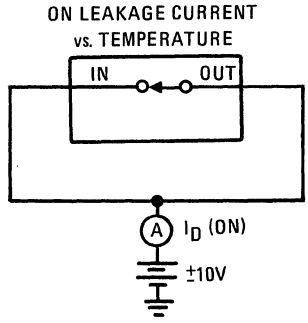


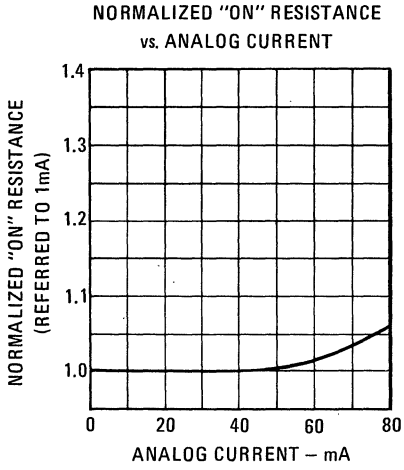
NORMALIZED "ON" RESISTANCE vs. TEMPERATURE

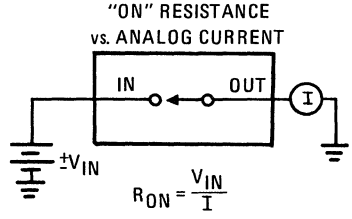



ON/OFF LEAKAGE CURRENT vs. TEMPERATURE
100nA
10nA
1nA
100pA
10pA
LEAKAGE CURRENT
$I_{S(OFF)} = I_{D(OFF)}$
$I_{D(ON)}$
25°
50°
75°
100°
125°
TEMPERATURE – °C

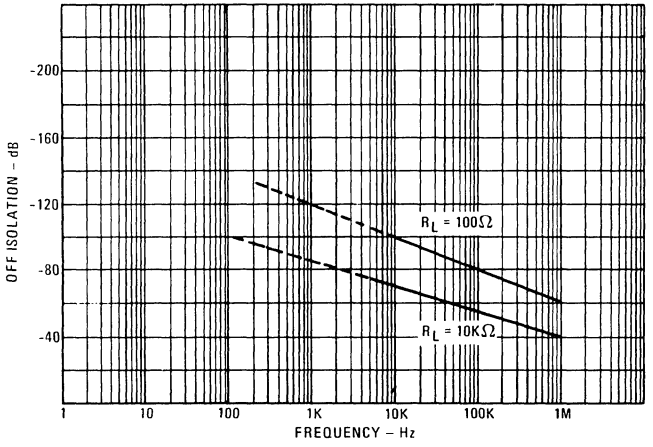

OFF LEAKAGE CURRENT
vs. TEMPERATURE
$I_{S(OFF)}$
$I_{D(OFF)}$
IN
OUT
A
±10V
±10V

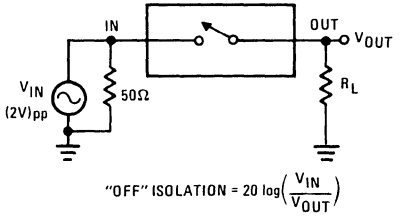

ON LEAKAGE CURRENT
vs. TEMPERATURE
IN
OUT
A
I_D (ON)
±10V


NORMALIZED "ON" RESISTANCE
vs. ANALOG CURRENT
NORMALIZED "ON" RESISTANCE
(REFERRED TO 1mA)
1.4
1.3
1.2
1.1
1.0
0
20
40
60
80
ANALOG CURRENT – mA


"ON" RESISTANCE
vs. ANALOG CURRENT
IN
OUT
I
±V_{IN}
$R_{ON} = \frac{V_{IN}}{I}$

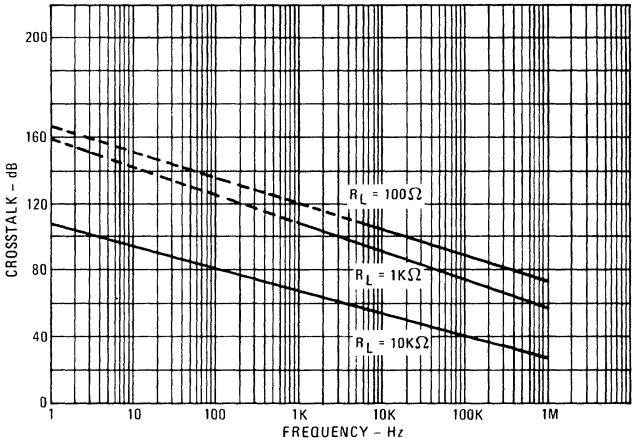
"OFF" ISOLATION vs. FREQUENCY

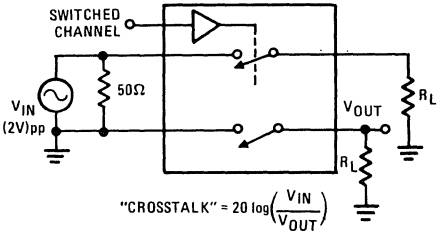




"OFF" ISOLATION = $20 \log\left(\frac{V_{IN}}{V_{OUT}}\right)$

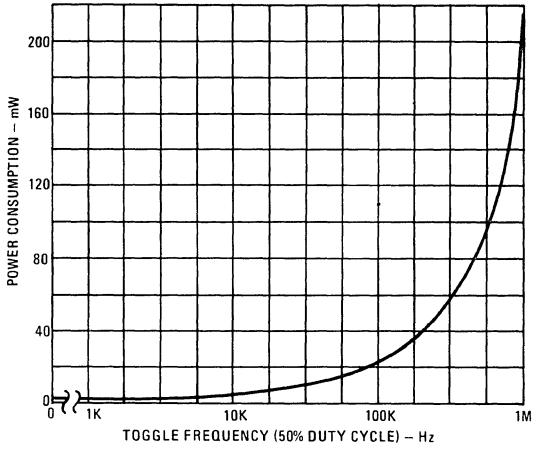
CROSSTALK vs. FREQUENCY

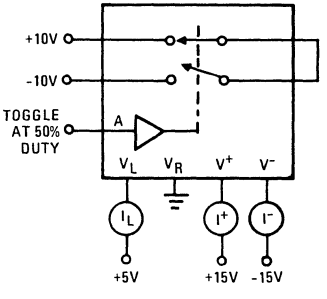




"CROSSTALK" = $20 \log\left(\frac{V_{IN}}{V_{OUT}}\right)$

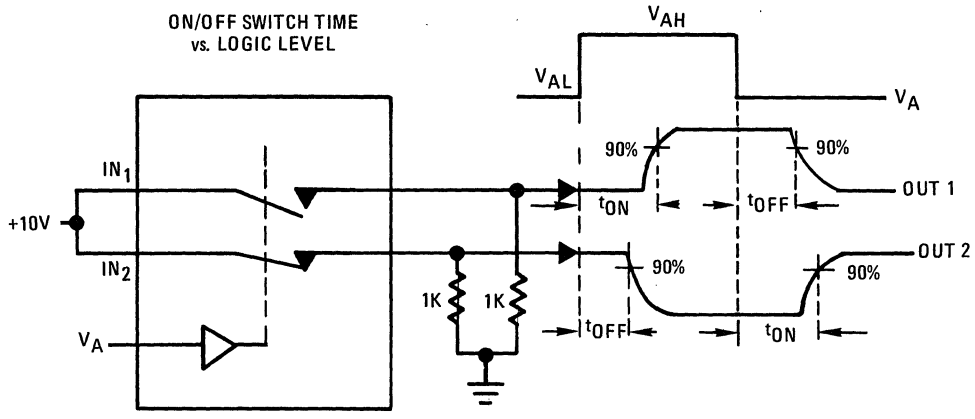
POWER CONSUMPTION vs. FREQUENCY

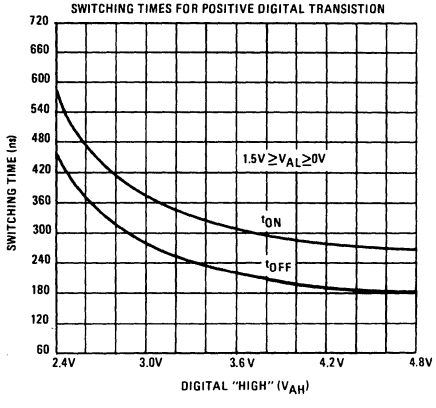


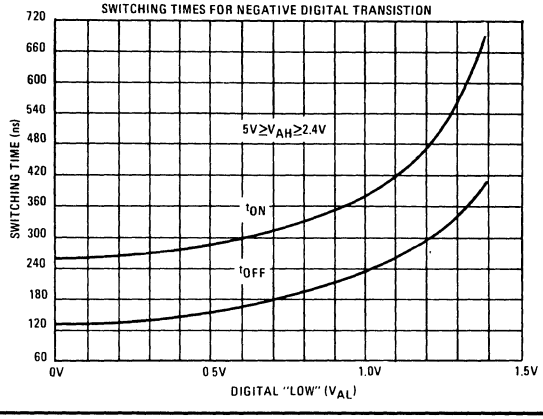


SWITCHING CHARACTERISTICS

ON/OFF SWITCH TIME
vs. LOGIC LEVEL

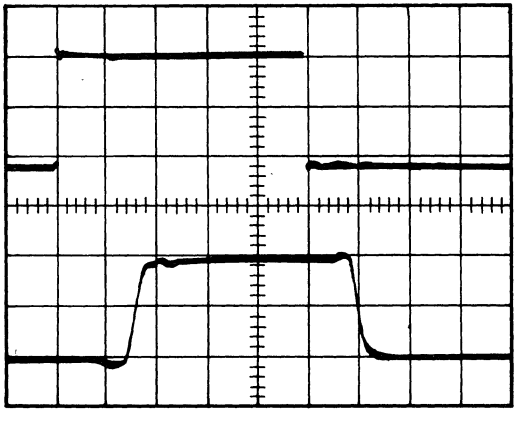






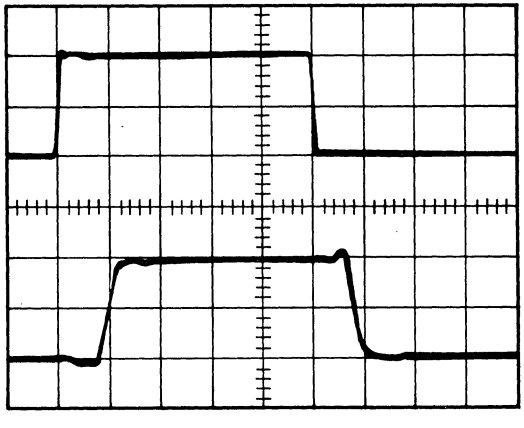
SWITCHING WAVEFORMS

TOP: TTL INPUT (1V/DIV)
V_{AH} = 3V, V_{AL} = 0.8V
BOTTOM: OUTPUT (5V/DIV)



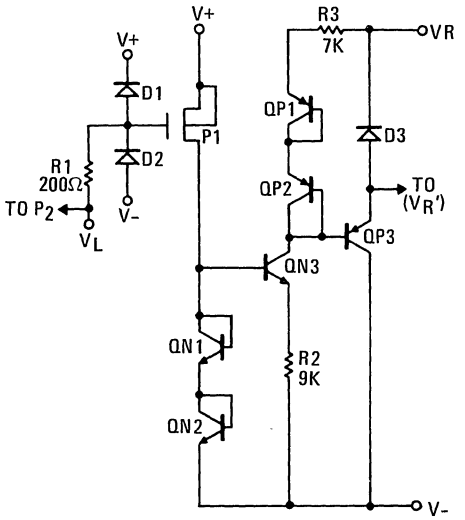
200ns/DIV

TOP: CMOS INPUT (5V/DIV)
V_{AH} = 10V, V_{AL} = 0V
BOTTOM: OUTPUT (5V/DIV



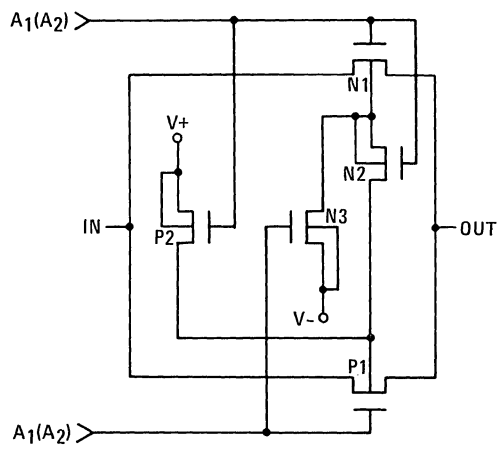
200ns/DIV

TTL/CMOS
REFERENCE CIRCUIT*

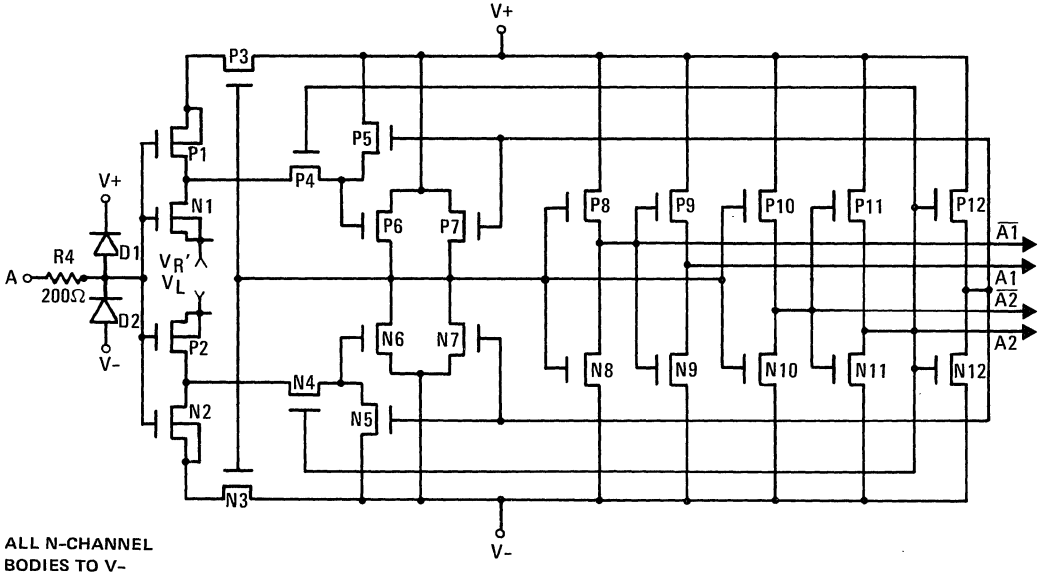


*Connect V^+ to V_L for minimizing power consumption when driving from CMOS circuits

SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER



ALL N-CHANNEL BODIES TO V-

ALL P-CHANNEL BODIES TO V+

EXCEPT AS SHOWN

3

3

CMOS
Analog Multiplexers

4

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

CMOS Multiplexers Selection Guide

FUNCTION	DEVICE	FEATURE	TTL "HIGH" MIN(V)	$R_{ON}(\Omega)$ (TYP)	$I_{D(OFF)}$ (nA) (TYP)	$t_{(ON)}$ (ns) (TYP)	$t_{(OFF)}$ (ns) (TYP)	P_D(mW) (TYP)	PAGE
4-CHANNEL DIFFERENTIAL	HI-1828A	LOW R_{ON} LOW LEAKAGE	4.0	250	0.05	350	250	5	48
	HI-509A	ANALOG INPUT OVERVOLTAGE PROTECTION	4.0	1200	1.0	300	300	7.5	22
8-CHANNEL	HI-1818A	LOW R_{ON} LOW LEAKAGE	4.0	250	0.1	350	250	5	48
	HI-508A	ANALOG OVERVOLTAGE PROTECTION	4.0	1200	1.0	300	300	7.5	22
8-CHANNEL DIFFERENTIAL	HI-507	LOW R_{ON}	2.4	170	1.0	300	300	30	3
	HI-507A	ANALOG OVERVOLTAGE PROTECTION	4.0	1200	1.0	300	300	7.5	9
16-CHANNEL	HI-506	LOW R_{ON}	2.4	170	1.0	300	300	30	3
	HI-506A	ANALOG OVERVOLTAGE PROTECTION	4.0	1200	1.0	300	300	7.5	34
8-CHANNEL/ 4 DIFFERENTIAL	HI-518	HIGH SPEED LOW LEAKAGE	2.4	620	0.035	100	80	525	31
16-CHANNEL/ 8 DIFFERENTIAL	HI-516	HIGH SPEED LOW LEAKAGE	2.4	480	0.1	80	60	360	28
4-CHANNEL	HI-524	VIDEO BANDWIDTH	2.4	700	0.2	180	180	540	34
4-CHANNEL/ DIFFERENTIAL	HI-539	LOW LEVEL SIGNALS	4.0	650 ΔR_{ON} = 5.5 Ω	0.1 $\Delta I_{D(OFF)}$ = 10pA	250	160	2.5	39

NOTE: All data typical room temperature specifications at $\pm$15V supplies. For guaranteed and tested specifications consult the device data sheet.

HARRIS

HI-506/HI-507

Single 16/Differential 8 Channel CMOS Analog Multiplexers

FEATURES

- LOW ON RESISTANCE (TYP.) 170Ω
- WIDE ANALOG SIGNAL RANGE ±15V
- DIRECTLY TTL/CMOS COMPATIBLE 2.4V (LOGIC "1")
- ACCESS TIME (TYP.) 300ns
- HIGH CURRENT CAPABILITY (TYP.) 50mA
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several mulitplexers are present.

The Dielectic Isolation (DI) process used in fabrication of these devices eliminates the problem of latchup. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction - isolated CMOS (See Application Note 521). With the low ON resistance (180Ω typical), this allows low static error, fast channel switching rates, and fast settling.

Switches are guaranteed to break-before-make, so two channels are never shorted together.

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for "1" and maximum 0.8V for "0". This allows direct interface without pullup resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

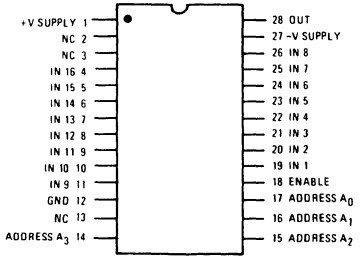
The HI-506 is a sixteen channel single-ended multiplexer, and the HI-507 is an eight channel differential version. The recommended supply voltage is ± 15V; however, reasonable performance is available down to ± 7V. Each device is packaged in a 16 pin DIP.

The HI-506/507 are specified for operation from 0°C to 70°C. The "-2" versions are specified from -55°C to +125°C. "Dash 8" (-8) designates -2 parts which have been screened per Mil-Std-883/ Method 5004/Class B.

PINOUT

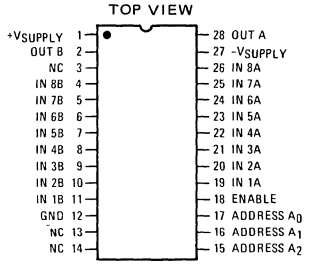
HI-506 — Section 11 for Packaging

TOP VIEW



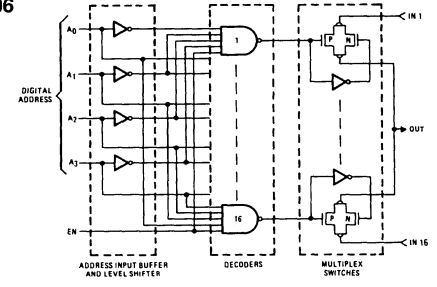
HI-507 — Section 11 for Packaging

TOP VIEW

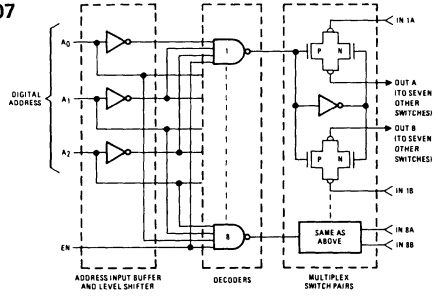


FUNCTIONAL DIAGRAM

HI-506



HI-507



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 40V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { V_{Supply} (+) +4V; V_{Supply} (-) -4V

Analog Input Overvoltage: (Note 6)

V_D or V_S { V_{Supply} (+) +2V; V_{Supply} (-) -2V

Total Power Dissipation* 1200 mW

Operating Temperature:

HI-506/HI-507-2 -55°C to +125°C

HI-506/HI-507-5 0°C to +75°C

Storage Temperature -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: Supplies = +15V, -15V; V_{AH}(Logic Level High) = +2.4V, V_{AL}(Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics section.

		HI-506/HI-507-2 -55°C to +125°C			HI-506/HI-507-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
* V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		170	300		270	400	Ω
	Full			400			500	Ω
* ΔR_{ON}, (Between Channels)	+25°C		6			6		%
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		0.3			1.0		nA
HI-506	Full			±500			±500	nA
HI-507	Full			±250			±250	nA
* $I_{D(ON)}$, On Channel Leakage Current	+25°C		0.3			1.0		nA
HI-506	Full			±500			±500	nA
HI-507	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			+0.8			+0.8	V
V_{AH}, Input High Threshold	Full	+2.4			+2.4			V
* I_A, Input Leakage Current (High or Low)(Note 2)	Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		300	1000		300		ns
t_{OPEN}, Break-Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300	1000		300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300	1000		300		ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.025%)	+25°C		2.4			2.4		μs
"Off Isolation" (Note 3)	+25°C		75			75		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		4			4		pF
$C_{D(OFF)}$, Channel Output Capacitance								
HI-506	+25°C		44			44		pF
HI-507	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		2.2			2.2		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.08			0.08		pF
POWER REQUIREMENTS								
* I+, Current Pin 1 (Note 4)	Full		1.7	3.0		3.4	5.0	mA
* I-, Current Pin 27 (Note 4)	Full		0.4	1.0		0.8	2.0	mA
* I+, Standby (Note 5)	Full		1.7	3.0		3.4	5.0	mA
* I-, Standby (Note 5)	Full		0.4	1.0		0.8	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -1mA
2. Digital Inputs are Mos Gates. Typical Leakage Less Than 1nA.
3. V_{EN} = 0.8V, R_L = 1K, C_L = 28pF, V_S = 7VRMS, f = 500kHz.
4. V_{EN} = 4.0V, All V_A = 4.0V
5. V_{EN} = 0V, All V_A = 0V
6. If Analog Input Overvoltage Conditions are Anticipated, Use of HI-506A/507A Protected Multiplexers is Recommended. See HI-506A/507A Data Sheet.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

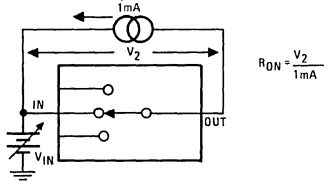
HI-507

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

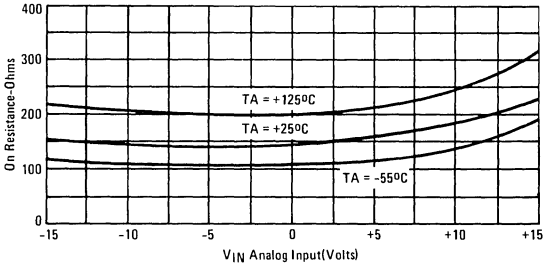
Unless Otherwise Specified; $T_A = 25^oC$, $V_{Supply} = \pm 15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$.

TEST CIRCUIT NO. 1

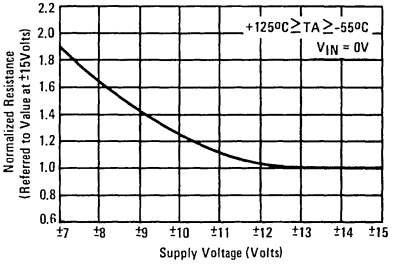
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE



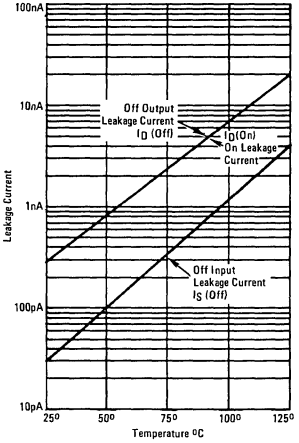
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



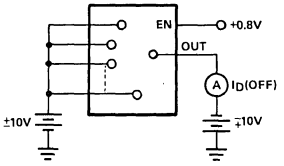
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



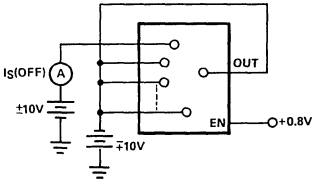
LEAKAGE CURRENT VS. TEMPERATURE



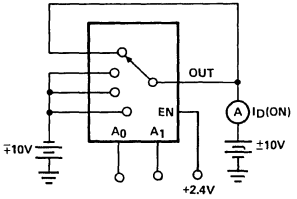
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

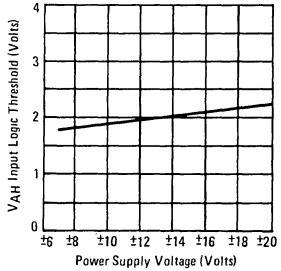


TEST CIRCUIT NO. 4*

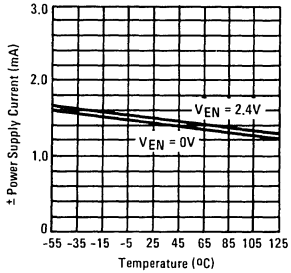


***Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V.)**

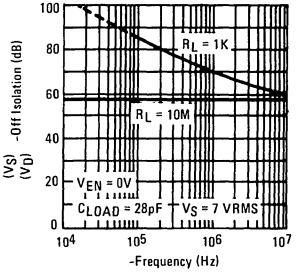
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



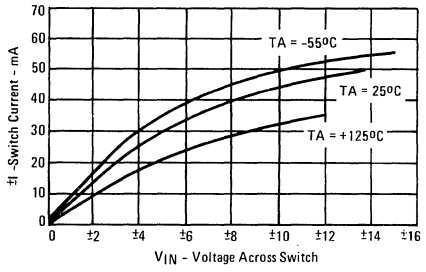
POWER SUPPLY CURRENT vs. TEMPERATURE



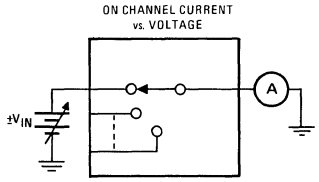
OFF ISOLATION vs. FREQUENCY



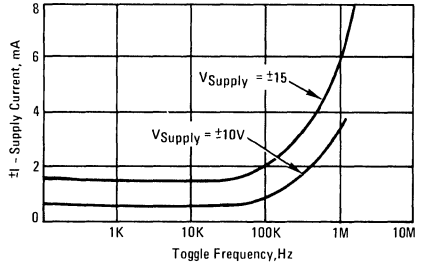
ON CHANNEL CURRENT vs. VOLTAGE



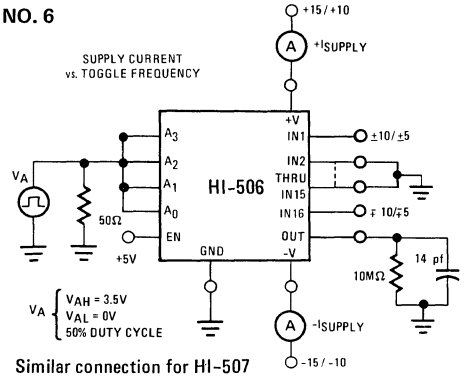
TEST CIRCUIT NO. 5



SUPPLY CURRENT vs. TOGGLE FREQUENCY

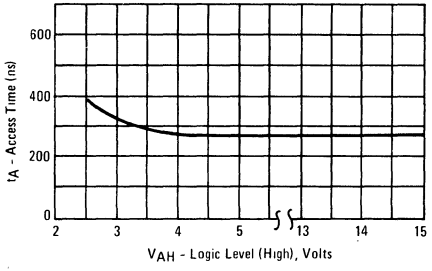


TEST CIRCUIT NO. 6

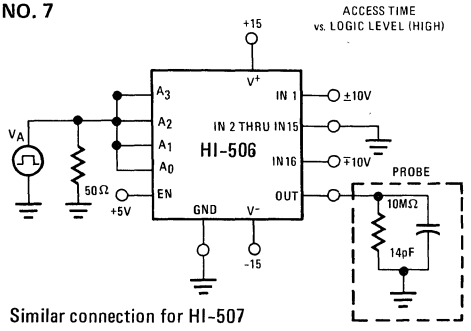


Similar connection for HI-507

ACCESS TIME vs. LOGIC LEVEL (HIGH)

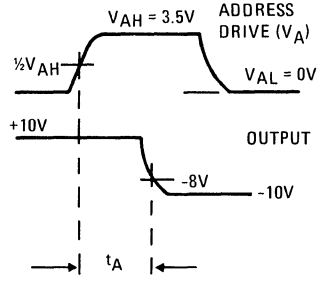


TEST CIRCUIT NO. 7

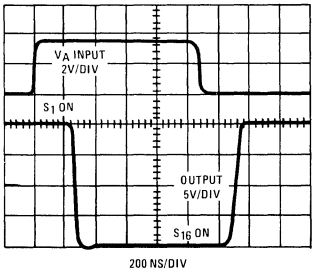


Similar connection for HI-507

SWITCHING WAVEFORMS

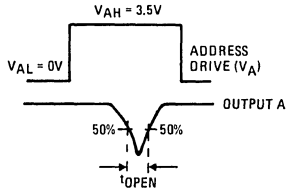


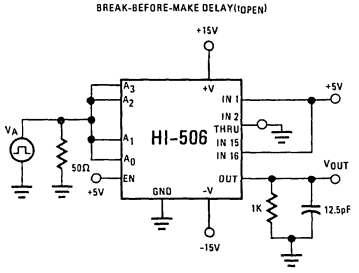
ACCESS TIME



SWITCHING WAVEFORMS (continued)

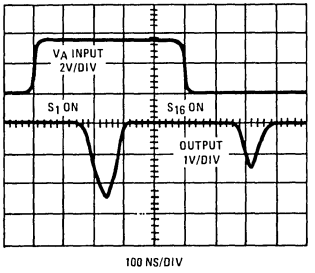
TEST CIRCUIT NO. 8



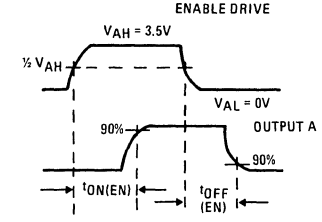


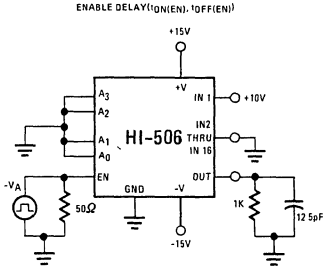
Similar connection for HI-507

BREAK-BEFORE-MAKE DELAY (t_{OPEN})



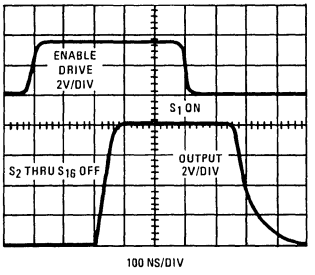
TEST CIRCUIT NO. 9





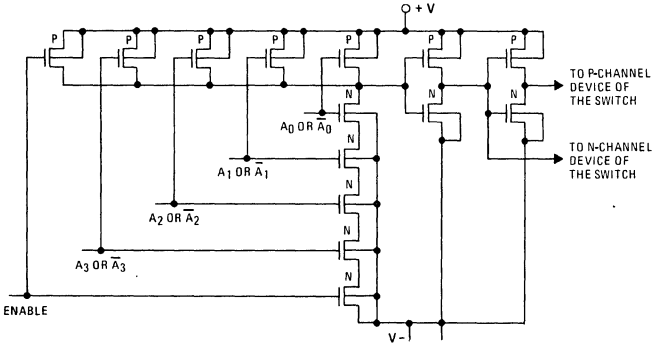
Similar connection for HI-507

ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



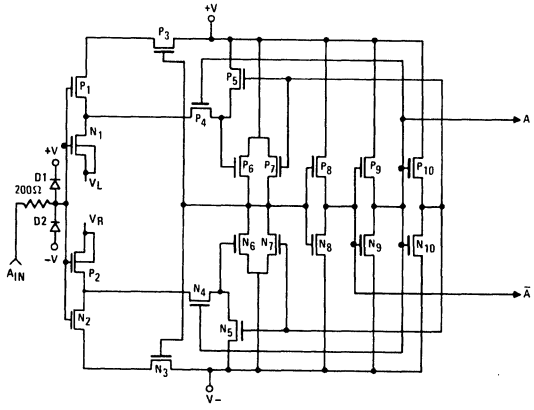
SCHEMATIC DIAGRAMS

ADDRESS DECODER



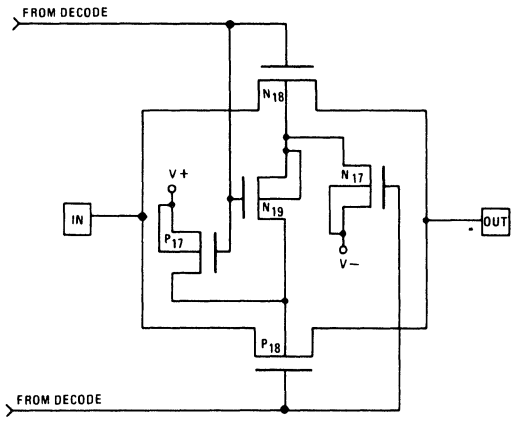
Delete A_3 or $\overline{A_3}$ Input for HI-507

ADDRESS INPUT BUFFER
LEVER SHIFTER

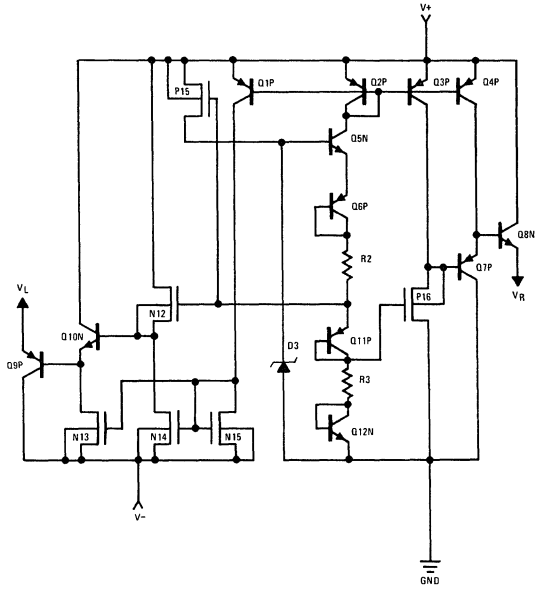


All N-Channel Bodies to V-
All P-Channel Bodies to V+ Unless Otherwise Indicated.

MULTIPLEX SWITCH



TTL REFERENCE CIRCUIT



HARRIS

HI-506A/HI-507A

16 Channel CMOS Analog Multiplexer with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

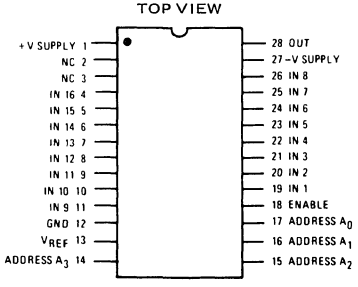
The HI-506A and HI-507A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

The HI-506A-2 and HI-507A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

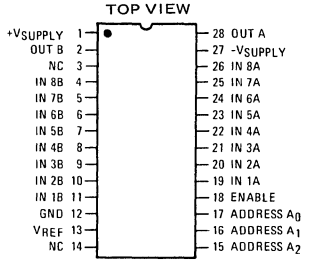
4

PINOUT

HI-506A — **Section 11 for Packaging**

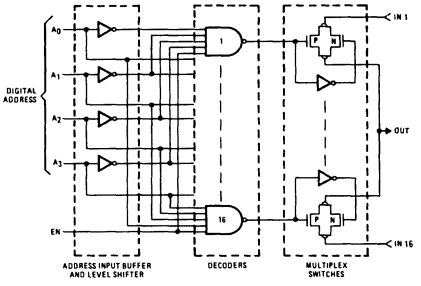


HI-507A — **Section 11 for Packaging**

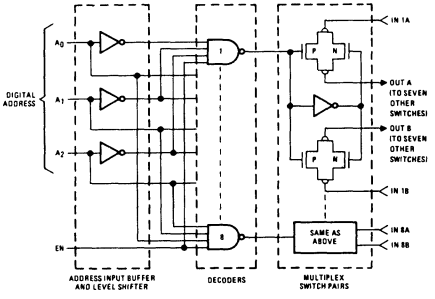


FUNCTIONAL DIAGRAM

HI-506A



HI-507A



ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27	40V	Total Power Dissipation*	1200mW
V_{REF} to Ground V+ to Ground	+20V	Operating Temperature	
V_{EN}, V_A, Digital Input Overvoltage:		HI-506A/507A-2	-55°C to +125°C
V_A (V_{Supply} (+))	+4V	HI-506A/507A-5	0°C to +75°C
V_A (V_{Supply} (–))	-4V	Storage Temperature	-65°C to +150°C
Analog Overvoltage:			
V_S (V_{Supply} (+))	+20V		
V_S (V_{Supply} (–))	-20V	*Derate 8mW/°C above T_A = +75°C	

ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	HI-506A/507A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-506A/507A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	2.0		1.8	2.0	KΩ
*I_S (OFF), Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
*I_D (OFF), Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-506A	Full			±500			±500	nA
HI-507A	Full			±250			±250	nA
*I_D (OFF) with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				μA
*I_D (ON), On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-506A	Full			±500			±500	nA
HI-507A	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold | TTL Drive	Full			0.8			0.8	V
V_{AH}, Input High Threshold | (Note 7)	Full	4.0			4.0			V
V_{AL} | MOS Drive (Note 3)	+25°C			0.8			0.8	V
V_{AH} |	+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break-Before Make Delay	+25°C		80			80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		300			300		ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		300			300		ns
Settling Time (0.1%)	+25°C		1.3			1.3		μs
(0.025%)	+25°C		4.4			4.4		μs
"Off Isolation" (Note 4)	+25°C		65			65		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-506A	+25°C		50			50		pF
HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current Pin 1 (Note 5)	Full		0.5	2.0		0.5	5.0	mA
*I-, Current Pin 27 (Note 5)	Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 6)	Full		0.5	2.0		0.5	5.0	mA
*I-, Standby (Note 6)	Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100 μA.
2. Analog Overvoltage = ±33V.
3. V_{REF} = +10V.
4. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500KHz.
5. V_{EN} = +4.0V.
6. V_{EN} = 0.8V.
7. To drive from DTL/TTL circuits, 1KΩ pull-up resistors to +5.0V supply are recommended.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

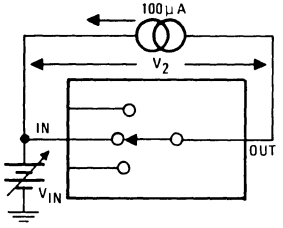
A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

(UNLESS OTHERWISE SPECIFIED $T_A = 25^0C$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$ AND V_{REF} = OPEN.)

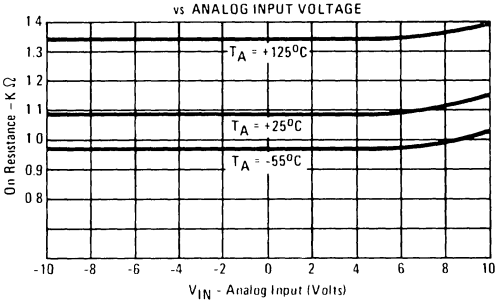
TEST CIRCUIT NO. 1

$$R_{ON} = \frac{V_2}{100\mu A}$$

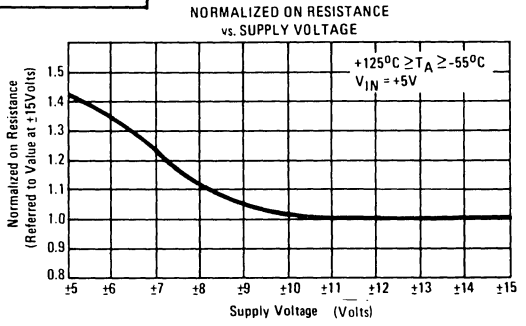
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE



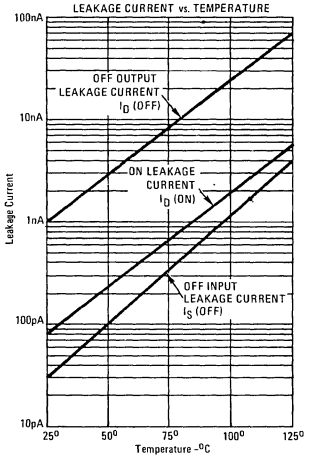
ON RESISTANCE vs ANALOG INPUT VOLTAGE



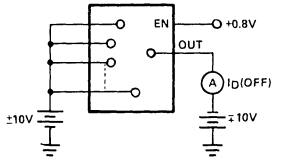
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



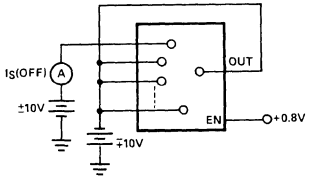
LEAKAGE CURRENT vs. TEMPERATURE



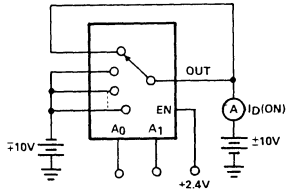
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

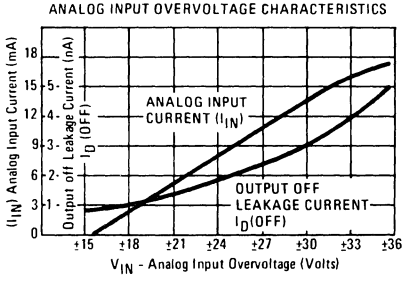


TEST CIRCUIT NO. 4*



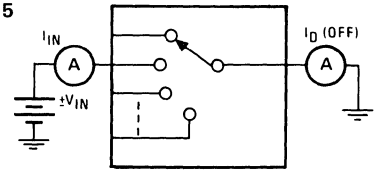
***Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for ID(OFF): +10V/-10V and -10V/+10V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

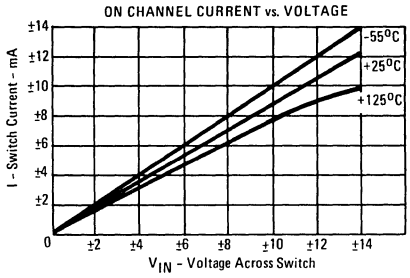


TEST CIRCUIT NO. 5

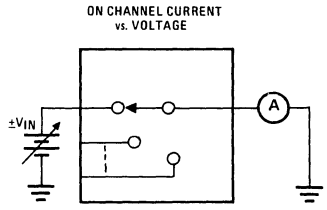
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

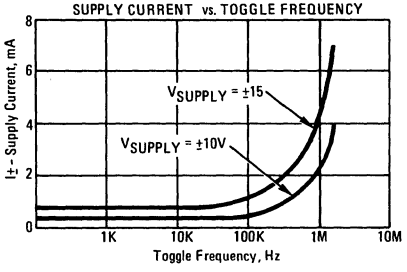


PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

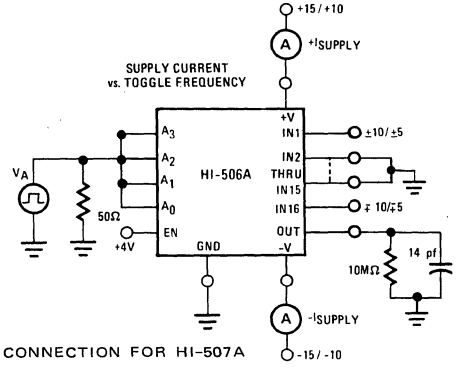


TEST CIRCUIT NO. 6

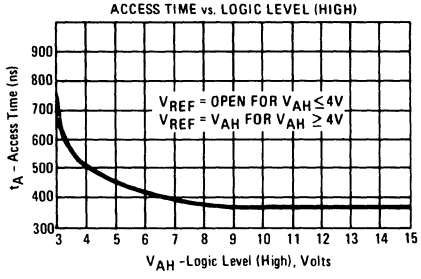




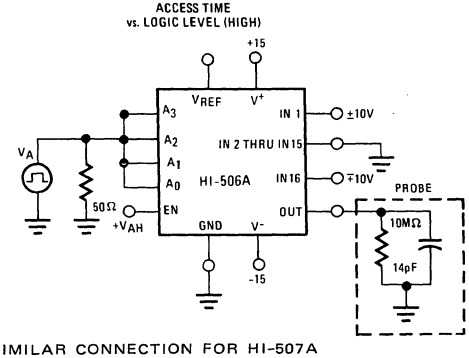
TEST CIRCUIT NO. 7



SIMILAR CONNECTION FOR HI-507A

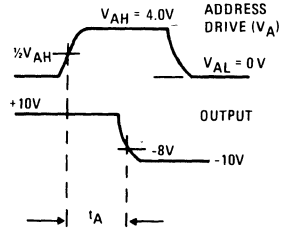


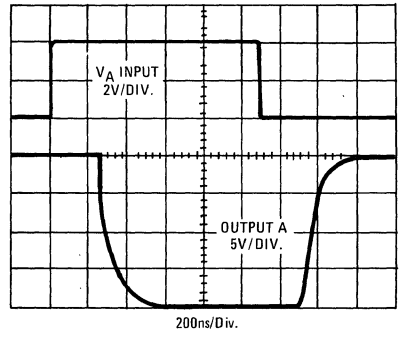
TEST CIRCUIT NO. 8



SIMILAR CONNECTION FOR HI-507A

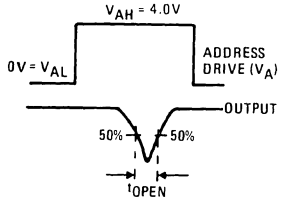
SWITCHING WAVEFORMS



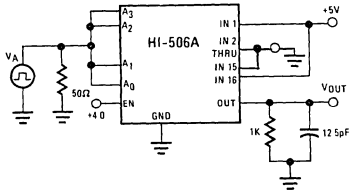


SWITCHING WAVEFORMS (continued)

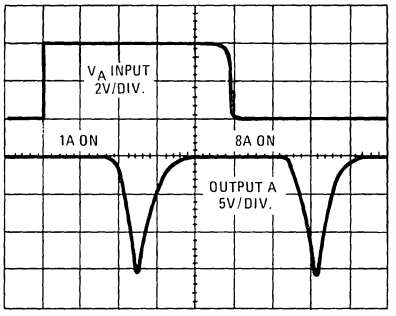
TEST CIRCUIT NO. 9



BREAK BEFORE MAKE DELAY (t_{OPEN})



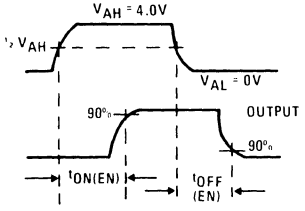
BREAK BEFORE MAKE DELAY (t_{OPEN})



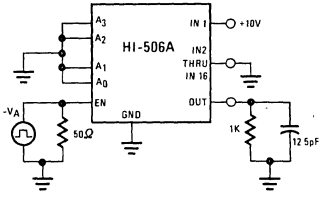
SIMILAR CONNECTION FOR HI-507A

TEST CIRCUIT NO. 10

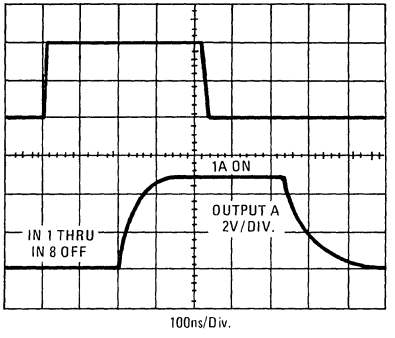
ENABLE DRIVE



ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

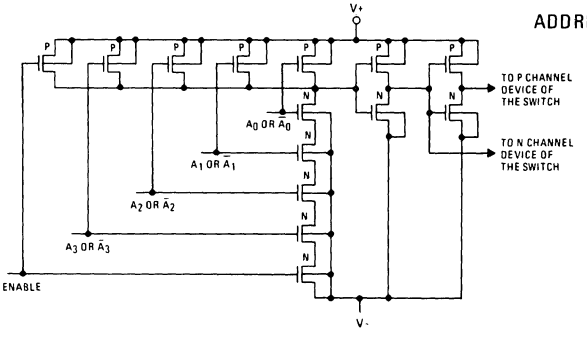


SIMILAR CONNECTION FOR HI-507A

SCHEMATIC DIAGRAMS

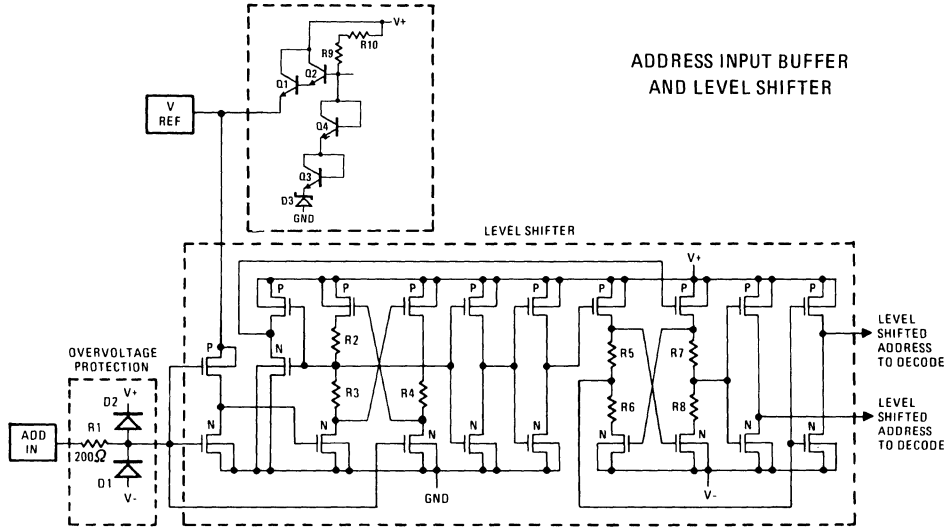
DELETE A_3 or $\overline{A}_3$ INPUT FOR HI-507A

ADDRESS DECODER

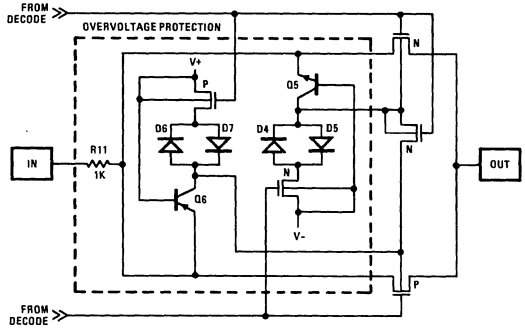


4

ADDRESS INPUT BUFFER
AND LEVEL SHIFTER



MULTIPLEX SWITCH



HI-508/HI-509

Single 8/Differential 4 Channel CMOS Analog Multiplexer

FEATURES

- FAST ACCESS 220ns
- FAST SETTLING (0.01%) 600ns
- LOW R_{ON} 180 Ω
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP
- TTL/CMOS COMPATIBLE 2.4V (LOGIC "1")

APPLICATIONS

- PRECISION INSTRUMENTS
- DATA ACQUISITION SYSTEMS
- TELEMETRY

DESCRIPTION

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (see Application Note 521). Combined with the low ON resistance (180Ω typical), these benefits allow low static error, fast channel switching rates, and fast settling.

Switches are guaranteed to break-before-make, so two channels are never shorted together.

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed min. 2.4V for "1" and max. 0.8V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL, and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

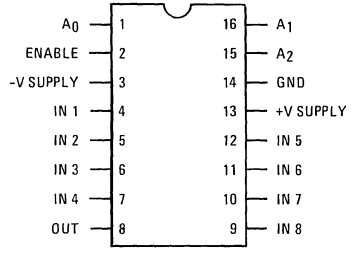
The HI-508 is an eight channel single-ended multiplexer, and the HI-509 is a four channel differential version. The recommended supply voltage is ±15V; however, reasonable performance is available down to ±7V. Each device is packaged in a 16 pin DIP.

The HI-508/509-5 are specified for operation from 0°C to 70°C. The "-2" versions are specified from -55°C to ±125°C. "Dash 8" (-8) designates -2 parts which have been screened per MIL-STD-883/Method 5004/Class B.

PINOUTS

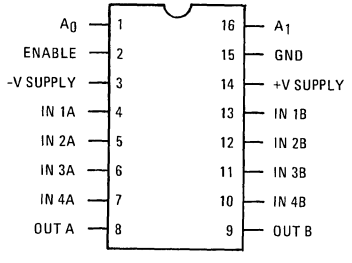
HI-508 — Section 11 for Packaging

TOP VIEW



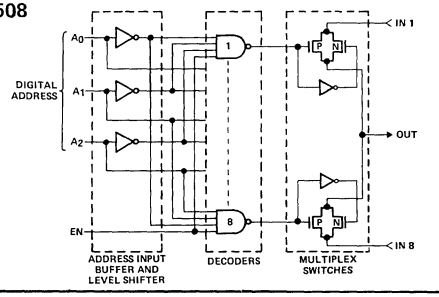
HI-509 — Section 11 for Packaging

TOP VIEW

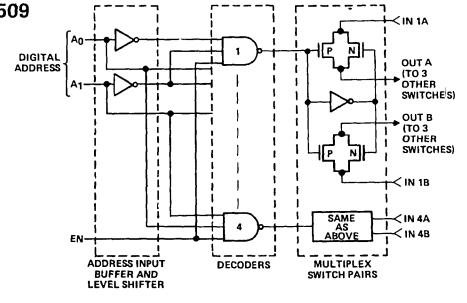


FUNCTIONAL DIAGRAMS

HI-508



HI-509



4

ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{Supply}^{(+)}$ to $V_{Supply}^{(-)}$ 40V

$V_{Supply}^{(+)}$ to GND 20V

$V_{Supply}^{(-)}$ to GND 20V

Digital Input Overvoltage:

V_{EN}, V_A $\begin{cases} V_{Supply}^{(+)} & +4V \\ V_{Supply}^{(-)} & -4V \end{cases}$

Analog Input Overvoltage (Note 6):

V_D, V_S $\begin{cases} V_{Supply}^{(+)} & +2V \\ V_{Supply}^{(-)} & -2V \end{cases}$

Power Dissipation * 750mW
(Derate 8mW/°C above T_A = +75°C)

Operating Temperature Ranges:

HI-508/509-2, -8	-55°C to +125°C
HI-508/509-5, -6	0°C to 70°C
HI-508/509-1	-55°C to +200°C

Storage Temperature Range -65°C to +150°C

* Package Limitation

ELECTRICAL CHARACTERISTICS Unless otherwise specified: Supplies = ± 15V, GND = 0V

		HI-508/HI-509-2 -55°C to +125°C			HI-508/HI-509-5 0°C to +70°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance	+25°C		180	300		180	400	Ω
	Full		230	400		230	500	Ω
ΔR_{ON}, Any Two Channels	+25°C		5			5		%
$I_{S(OFF)}$, Off Input Leakage Current (Note 2)	+25°C			10			10	nA
	Full			50			50	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C							
HI-508	Full		10	200		10	200	nA
HI-509	Full		10	100		10	100	nA
$I_{D(ON)}$, On Channel Leakage Current	+25°C							
HI-508	Full		10	200		10	200	nA
HI-509	Full		10	100		10	100	nA
I_{DIFF}, Differential Off Output Leakage Current	+25°C		1	5		1	5	nA
(HI-509 Only)	Full		5	50		5	50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AH}, High Threshold	Full	2.4			2.4			V
V_{AL}, Low Threshold	Full			0.8			0.8	V
I_A, Input Leakage Current (High or Low) (Note 3)	Full			1			1	μA
SWITCHING CHARACTERISTICS								
t_A, Access (Transition) Time	+25°C		220	500		220	1000	ns
	Full			1000				ns
t_{OPEN}, Break-Before-Make Interval	+25°C		70			70		ns
$t_{ON(EN)}$, Enable Turn-On	+25°C		210			210		ns
$t_{OFF(EN)}$, Enable Turn-Off	+25°C		180			180		ns
t_S, Settling Tme to 0.1%	+25°C		360			360		ns
to 0.01%	+25°C		600			600		ns
Off Isolation (Note 4)	+25°C		68			68		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D(OFF)}$, Channel Output Capacitance	+25°C		21			21		pF
C_A, Digital Input Capacitance	+25°C		3			3		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		.08			.08		pF
POWER REQUIREMENTS								
I+, Positive Supply Current (Note 5)	Full			2			2	mA
I-, Negative Supply Current (Note 5)	Full			1			1	mA
P_D, Power Dissipation	Full			45			45	mW

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Ten nanoamps is the practical limit for high speed measurement in the production test environment. Actually, I_S (off) is below 100pA for most devices, at 25°C.
3. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
4. V_{EN} = 0.8V, R_1 = 1K, C_1 = 15pF, V_S = 7V_{RMS}, f = 500kHz. Worst case isolation occurs on channel 4 (HI-508) and channels 4, 8 (HI-509), due to proximity of the output pins.
5. V_{EN} = 0V or 5V. All V_A = 0.
6. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the HARRIS HI-508A/509A multiplexers are recommended.

TRUTH TABLES

HI-508

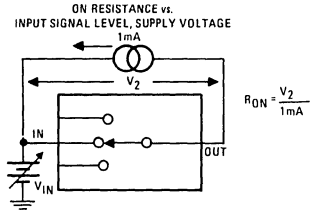
A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509

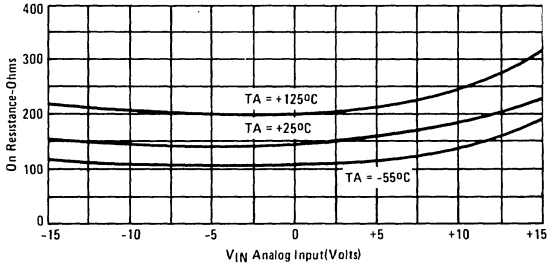
A_1	A_0	EN	"ON" CHANNEL
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Unless Otherwise Specified; T_A = 25°C, V_{Supply} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V.

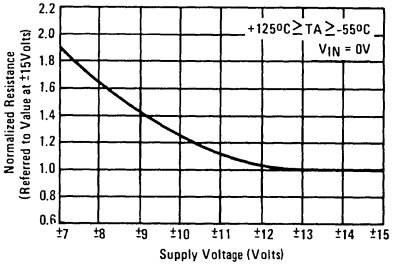
TEST CIRCUIT NO. 1



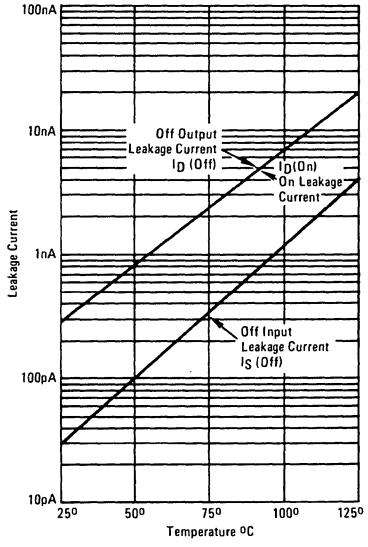
ON RESISTANCE
vs. ANALOG INPUT VOLTAGE, TEMPERATURE



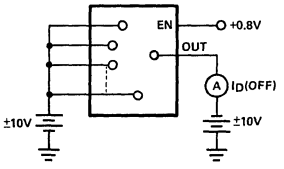
NORMALIZED ON RESISTANCE
vs. SUPPLY VOLTAGE



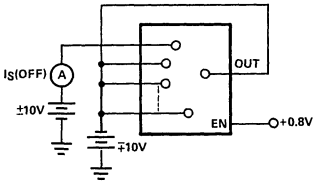
LEAKAGE CURRENT vs. TEMPERATURE



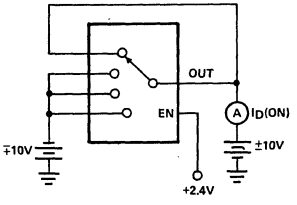
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

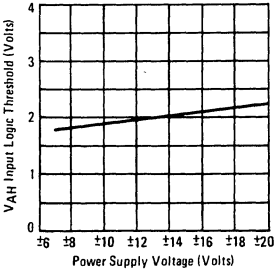


TEST CIRCUIT NO. 4*

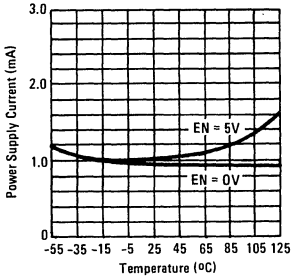


***Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V.)**

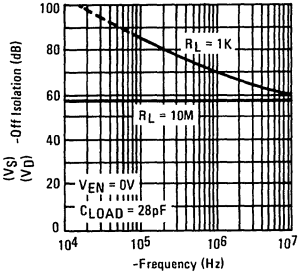
LOGIC THRESHOLD
vs. POWER SUPPLY VOLTAGE



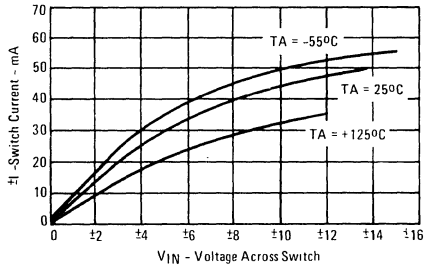
POWER SUPPLY CURRENT
vs. TEMPERATURE



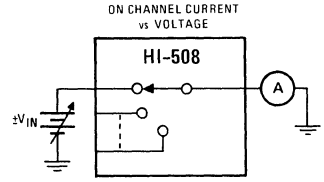
OFF ISOLATION vs.
FREQUENCY



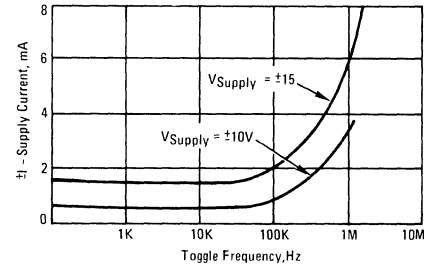
ON CHANNEL CURRENT vs. VOLTAGE



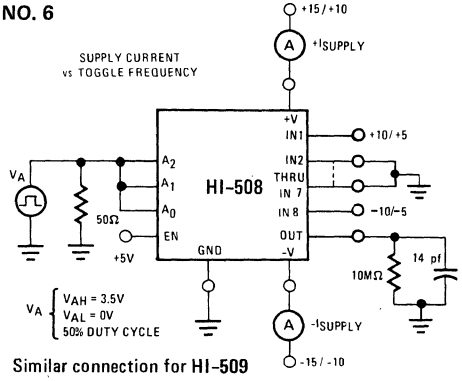
TEST CIRCUIT NO. 5



SUPPLY CURRENT vs. TOGGLE FREQUENCY

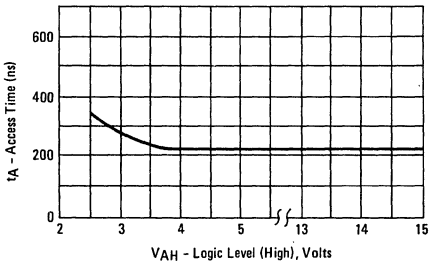


TEST CIRCUIT NO. 6

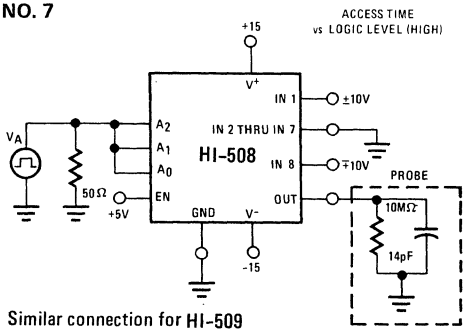


Similar connection for HI-509

ACCESS TIME vs. LOGIC LEVEL (HIGH)

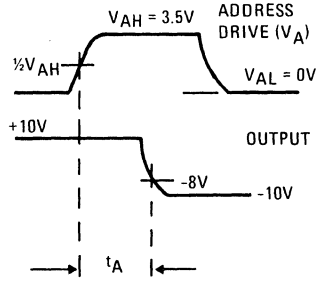


TEST CIRCUIT NO. 7

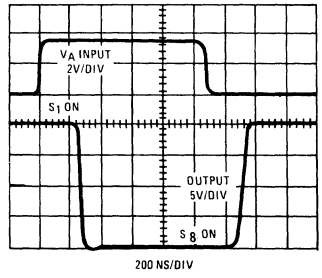


Similar connection for HI-509

SWITCHING WAVEFORMS



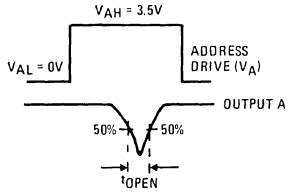
ACCESS TIME



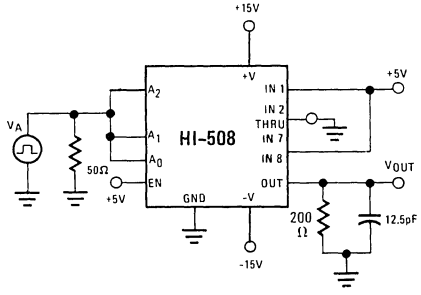
SWITCHING WAVEFORMS (continued)

TEST CIRCUIT NO. 8

ENABLE DRIVE

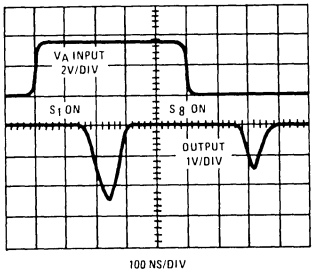


BREAK-BEFORE MAKE DELAY(t_{OPEN})



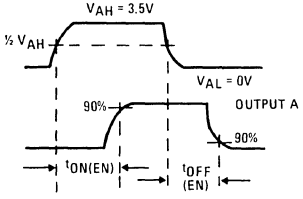
Similar connection for HI-509

BREAK-BEFORE-MAKE DELAY (t_{OPEN})

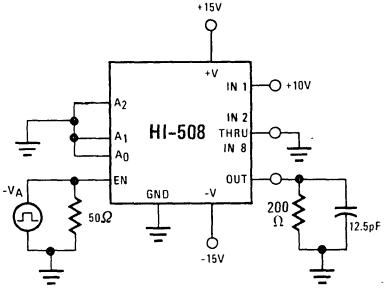


TEST CIRCUIT NO. 9

ENABLE DRIVE

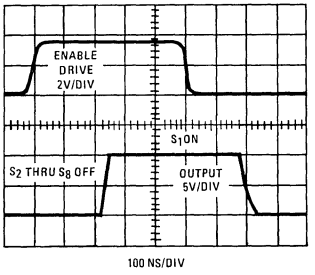


ENABLE DELAY($t_{ON(EN)}$, $t_{OFF(EN)}$)



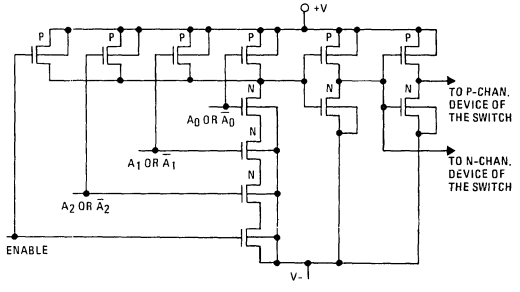
Similar connection for HI-509

ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



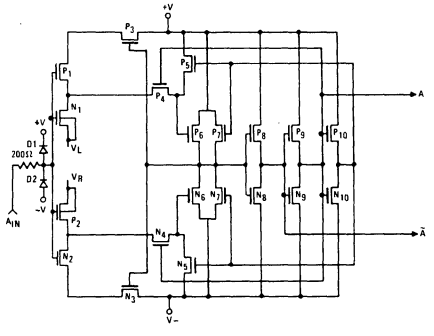
SCHEMATIC DIAGRAMS

ADDRESS DECODER



DELETE (A_2 OR $\bar{A}_2$) INPUT FOR HI-509

ADDRESS INPUT BUFFER LEVER SHIFTER

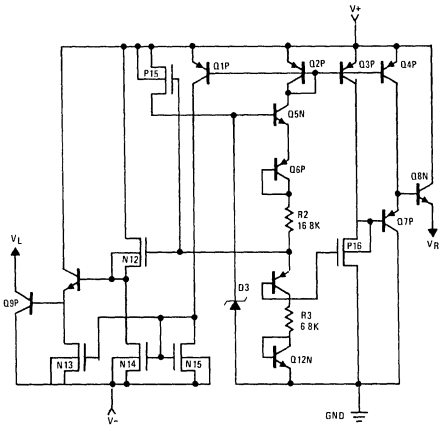


All N-Channel Bodies to V-
All P-Channel Bodies to V+ Unless Otherwise Indicated.

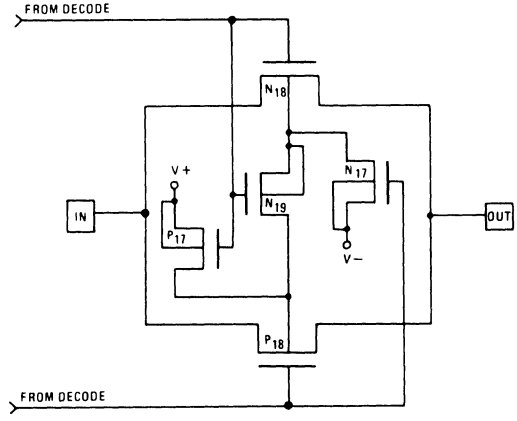
4

SCHEMATIC DIAGRAMS (continued)

TTL REFERENCE CIRCUIT

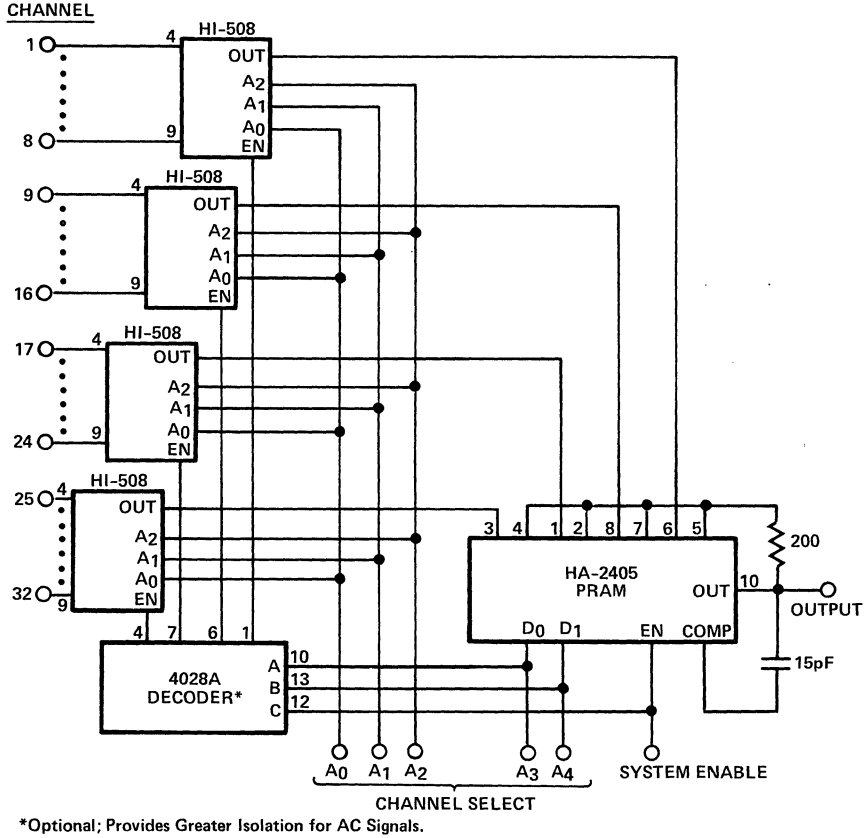


MULTIPLEX SWITCH



APPLICATIONS

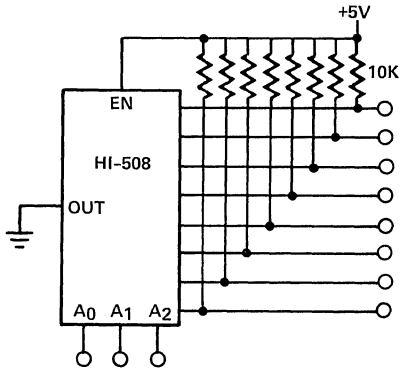
32 CHANNEL BUFFERED MULTIPLEXER



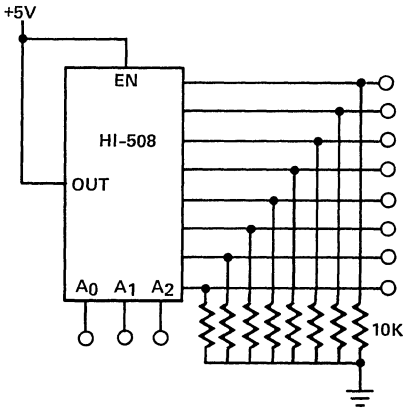
*Optional; Provides Greater Isolation for AC Signals.

ONE OF 8 DECODER

ACTIVE LOW



ACTIVE HIGH



4

HI-508A/509A

8 Channel CMOS Analog Multiplexers with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

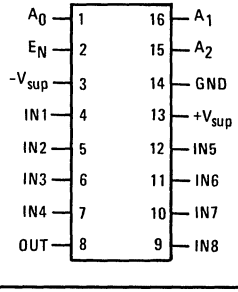
The HI-508A and HI-509A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

The HI-508A-2 and HI-509A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

PINOUT

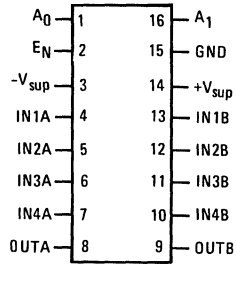
HI-508A — **Section 11 for Packaging**

TOP VIEW



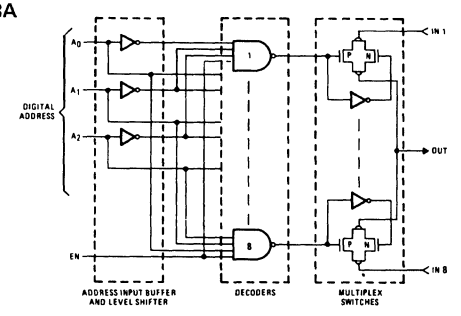
HI-509A — **Section 11 for Packaging**

TOP VIEW

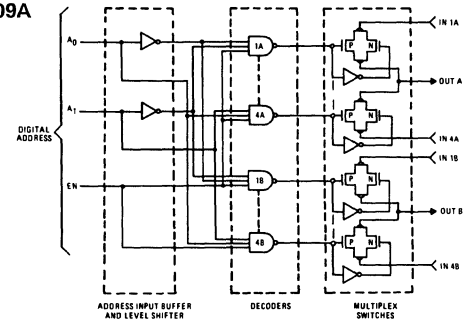


FUNCTIONAL DIAGRAM

HI-508A



HI-509A



4

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins 40V

V+ to Ground 20V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { V_{Supply}(+) +4V; V_{Supply} (-) -4V

Analog Input Overvoltage:

V_S { V_{Supply} (+) +20V; V_{Supply} (-) -20V

Total Power Dissipation* 725 mW

Operating Temperature:

HI-508A/HI-509A-2 -55°C to +125°C

HI-508A/HI-509A-5 0°C to +75°C

Storage Temperature -65°C to +150°C

*Derate 8mW/°C above t_A = 75°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characterisitcs section.

PARAMETER	TEMP.	HI-508A/509A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-508A/509A-5 0°C to +75°C MIN.	TYP	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-508A	Full			±250			±250	nA
HI-509A	Full			±125			±125	nA
* $I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				μA
* $I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-508A	Full			±250			±250	nA
HI-509A				±125			±125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold (Note 6)	Full			0.8			0.8	V
V_{AH}, Input High Threshold (Note 6)	Full	4.0			4.0			V
* I_A, Input Leakage Current (High or Low)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break - Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300			300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300			300		ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.025%)	+25°C		3.5			3.5		μs
"OFF Isolation" (Note 3)	+25°C		65			65		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D(OFF)}$, Channel Output Capacitance								
HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current (Note 4)	Full		0.5	2.0		0.5	5.0	mA
*I-, Current (Note 4)	Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 5)	Full		0.5	2.0		0.5	5.0	mA
*I-, Standby (Note 5)	Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100μA
2. Analog Overvoltage = ±33V
3. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3V RMS, f = 500KHz
4. V_{EN} = +4.0V
5. V_{EN} = 0.8V
6. To drive from DTL/TTL Circuits, 1KΩ pull-up resistors to +5.0V supply are recommended

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-508A

A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

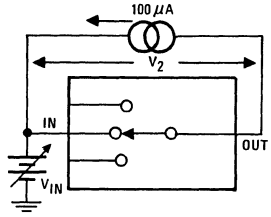
A_1	A_0	EN	ON SWITCH PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

4

UNLESS OTHERWISE SPECIFIED: $T_A = 25^oC$, $V_{SUPPLY} = +15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$

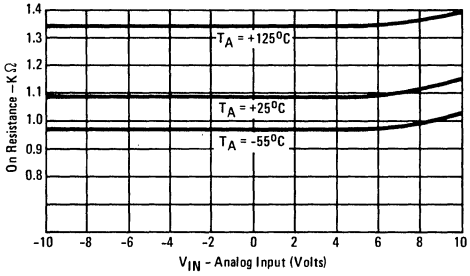
TEST CIRCUIT NO. 1

$R_{ON} = \frac{V_2}{100\mu A}$

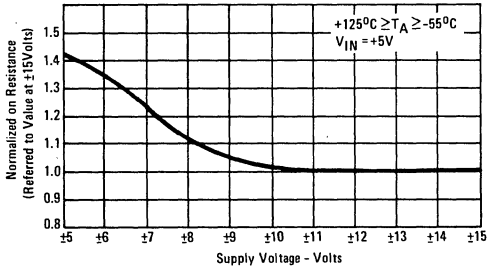


ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

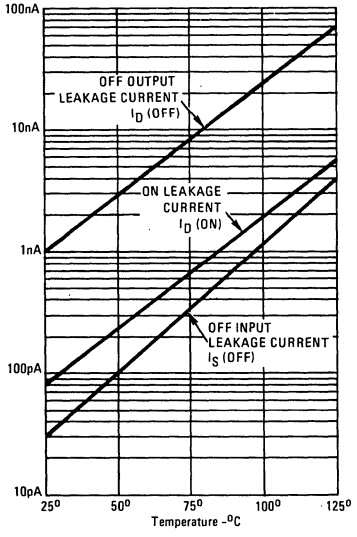
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



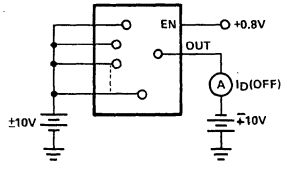
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



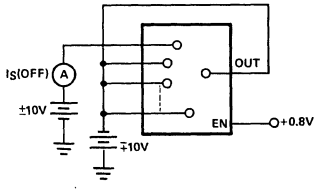
LEAKAGE CURRENT vs. TEMPERATURE



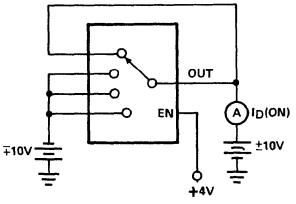
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

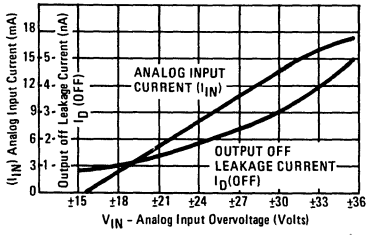


TEST CIRCUIT NO. 4*



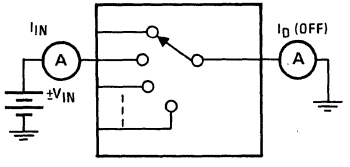
***Two measurements per channel: +10V/–10V and –10V/+10V. (Two measurements per device for $I_{D(OFF)}$: +10V/–10V and –10V/+10V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



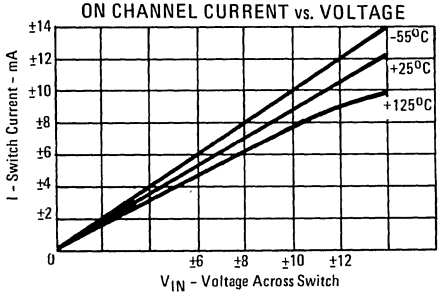
TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



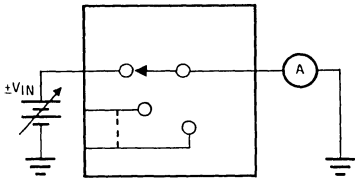
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (continued)

ON CHANNEL CURRENT vs. VOLTAGE

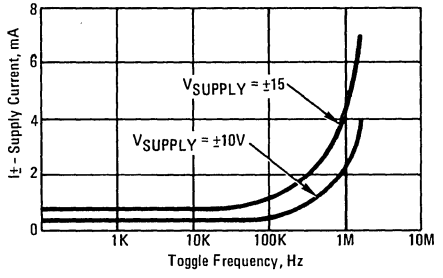


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

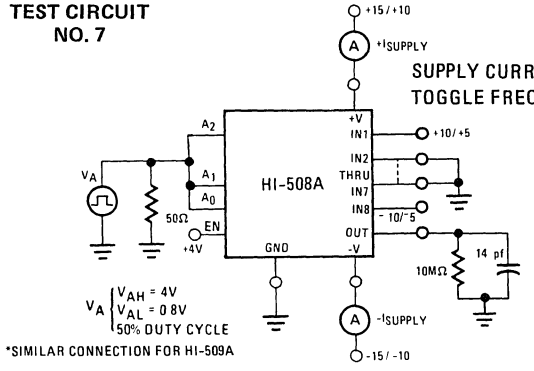


SUPPLY CURRENT vs. TOGGLE FREQUENCY



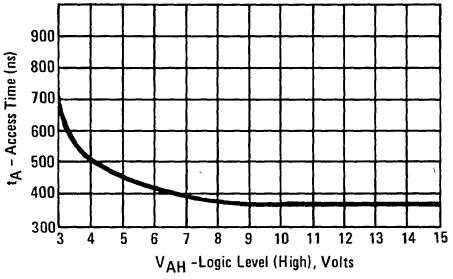
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY



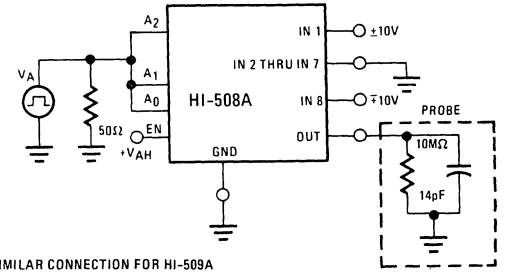
*SIMILAR CONNECTION FOR HI-509A

ACCESS TIME vs. LOGIC LEVEL (HIGH)



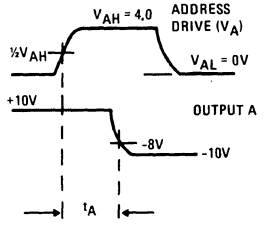
TEST CIRCUIT NO. 8

ACCESS TIME vs. LOGIC LEVEL(HIGH)

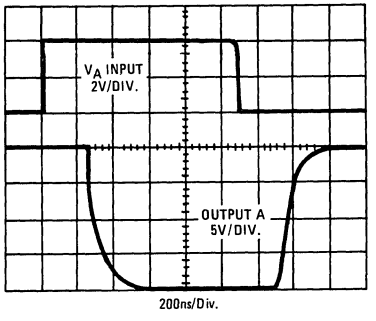


* SIMILAR CONNECTION FOR HI-509A

SWITCHING WAVEFORMS



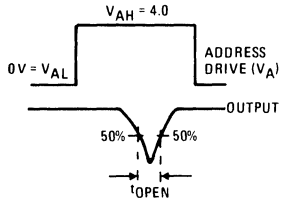
ACCESS TIME

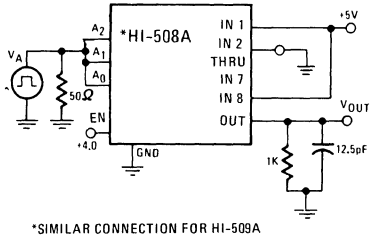


4

SWITCHING WAVEFORMS (continued)

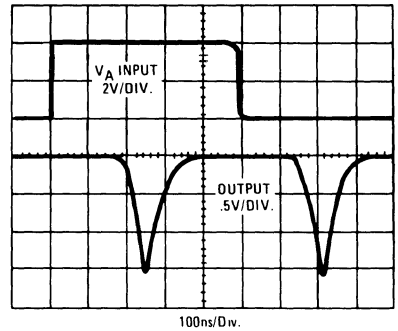
TEST CIRCUIT
NO. 9
BREAK BEFORE MAKE DELAY (t_{OPEN})



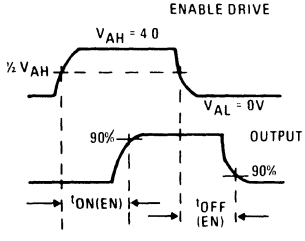


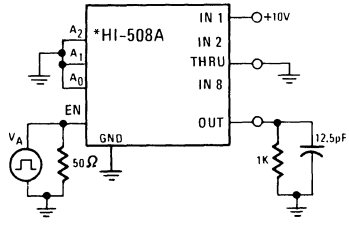
*SIMILAR CONNECTION FOR HI-509A

BREAK BEFORE MAKE DELAY (t_{OPEN})



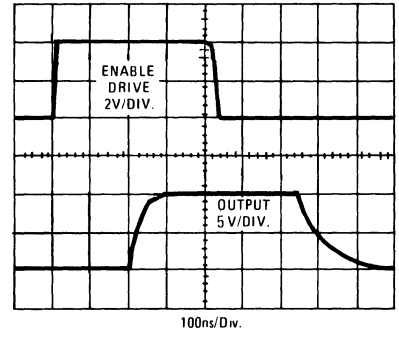
TEST CIRCUIT
NO. 10
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



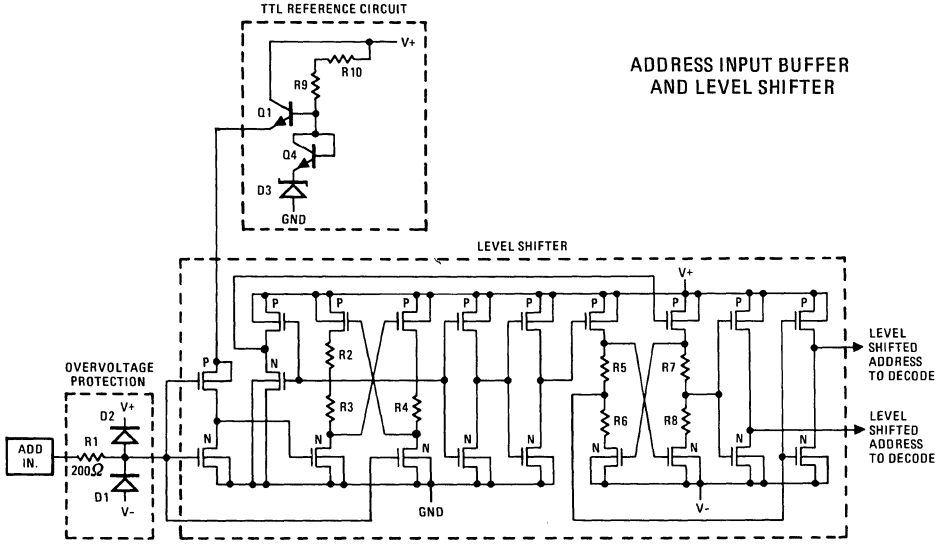


* SIMILAR CONNECTION FOR HI-509A

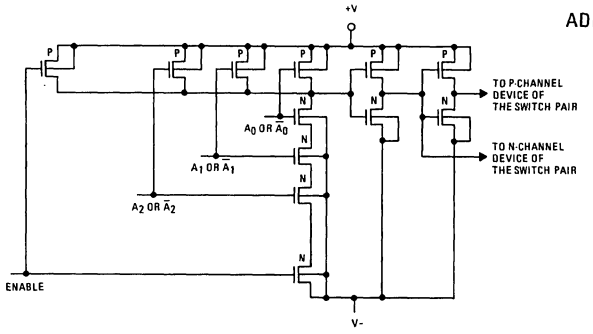
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



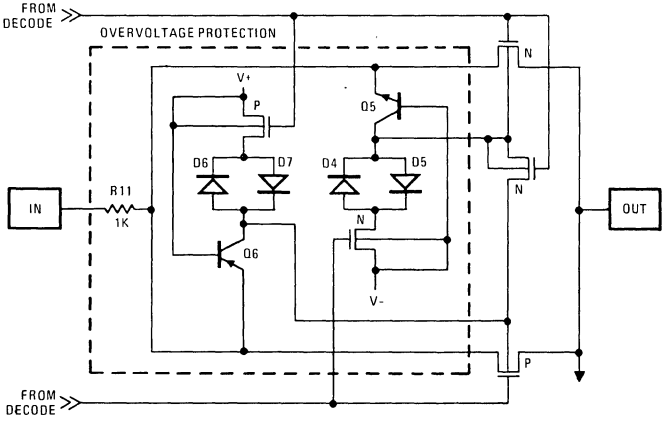
SCHEMATIC DIAGRAMS



ADDRESS DECODER



MULTIPLEX SWITCH



HARRIS

HI-516

16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer

FEATURES

- ACCESS TIME (TYP) 100ns
- SETTLING TIME (TYP TO 0.01%) 800ns
- LOW LEAKAGE I_S OFF 10pA
  I_D OFF 35pA
- LOW CAPACITANCE C_S OFF 2.5pF
  C_D OFF 18pF
- HIGH OFF ISOLATION AT 1MHz 80dB
- LOW CHARGE INJECTION 0.3pC
- SINGLE ENDED TO DIFFERENTIAL SELECTABLE (SDS)
- LOGIC LEVEL SELECTABLE (LLS)

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- INDUSTRIAL CONTROL

DESCRIPTION

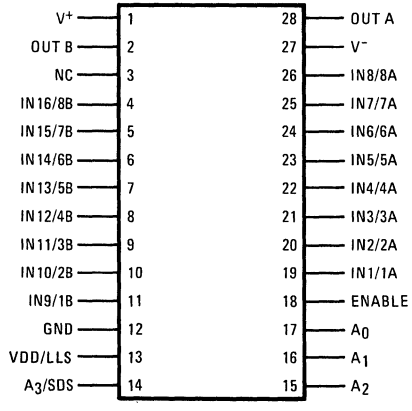
The HI-516 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_3 enables the HI-516 to be user programmed either as a single ended 16-channel multiplexer by connecting 'out A' to 'out B' and using A_3 as a digital address input, or as an 8-channel differential multiplexer by connecting A_3 to the V^- supply. The substrate leakages and parasitic capacitances are reduced substantially using the Harris dielectric isolation process to achieve optimum performances in both high and low level signal applications. The low output leakage current (I_D Off < 100pA @ 25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process controls.

The HI-516 is available in a 28 lead dual-in-line package. HI-516-5 is specified for operation over 0°C to +75°C, and the HI-516-2 over -55°C to +125°C. Processing to MIL-STD-883A, Class B screening is available by selecting the HI-516-8.

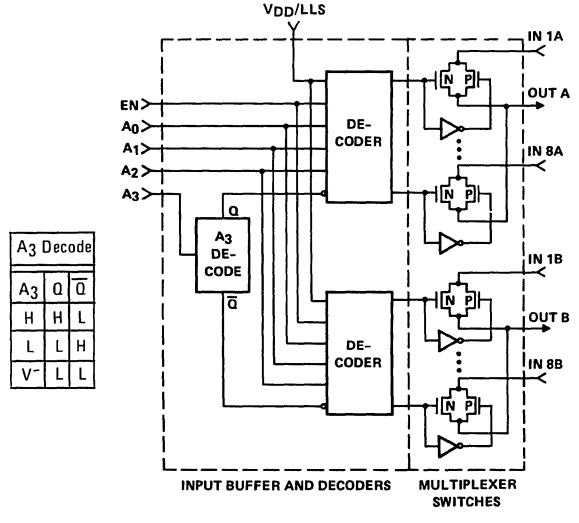
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL DIAGRAM



A3 Decode

A3	Q	Q̄
H	H	L
L	L	H
V-	L	L

ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:

- TTL: $-6V < V_{AH} < +6V$
- TTL: A2 V_{SUPPLY} (-) -2V
- CMOS: V_{SUPPLY}(+) +2V
- CMOS: GND -2V

Analog Input Voltage:

- V_S: V_{SUPPLY}(+) +2V
- V_S: V_{SUPPLY}(-) -2V

Voltage Between Supply Pins 33V

Total Power Dissipation* 1200mW

Operating Temperature Ranges:

- HI-516-2 -55°C to +125°C
- HI-516-5 0°C to 75°C

Storage Temperature Range -65°C to 150°C

*Derate 8mW/°C above t_A 75°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = Open (Note 6)

PARAMETER	TEMP	-55°C to +125°C MIN	TYP	MAX	0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 1)	+25°C		620	750		620	750	Ω
	Full		770	1,000		700	1,000	Ω
I_S (OFF), Off Input Leakage Current	+25°C		0.01			0.01		nA
	Full		0.38	50		0.38	50	nA
I_D(OFF), Off Output Leakage Current	+25°C		0.035			0.035		nA
	Full		0.48	100		0.48	100	nA
I_D(ON), On Channel Leakage Current	+25°C		0.04			0.04		nA
	Full		0.56	100		0.56	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AH} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AL} Current (Low)	Full		4	25		4	25	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		100	150		100	150	ns
	Full		120	200		120	200	ns
t_{OPEN}, Break before make delay	+25°C		20			20		ns
t_{ON}(EN), Enable Delay (IN)	+25°C		100	150		100		ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		80	125		80		ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		ns
Charge Injection (Note 2)	+25°C		0.33			0.33		pC
Off Isolation (Note 3)	+25°C		90			90		dB
C_S(OFF), Channel Input Capacitance	+25°C		2.5			2.5		pF
C_D(OFF), Channel Output Capacitance	+25°C		18			18		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS}(OFF), Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
PD, Power Dissipation	Full		525			525		mW
I^+, Current (Note 4)	Full		17.5	25		17.5	30	mA
I^-, Current (Note 4)	Full		17.5	25		17.5	30	mA
I^+, Standby (Note 5)	Full		17.0	25		17.0	30	mA
I^-, Standby (Note 5)	Full		17.0	25		17.0	30	mA

NOTES:

1. $V_{IN} = \pm 10V$, $I_{OUT} = -100\mu A$
2. V_{IN} = 0V, C_L = 100pF, Enable input pulse = 3V, f = 500kHz
3. V_{EN} = 0.8V, V_S = $3V_{RMS}$, f = 500kHz, C_L = 40pF, R_L = 1k, Pin 3 grounded
4. V_{EN} = +2.4V
5. V_{EN} = 0.8V
6. V_{DD}/LLS Pin = Open or Grounded for TTL Compatibility
   V_{DD}/LLS Pin = V_{DD} for CMOS Compatibility

HI-516 USED AS A 16-CHANNEL MULTIPLEXER OR 8 CHANNEL DIFFERENTIAL MULTIPLEXER *

USE A_3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	NONE	NONE
H	L	L	L	L	1A	NONE
H	L	L	L	H	2A	NONE
H	L	L	H	L	3A	NONE
H	L	L	H	H	4A	NONE
H	L	H	L	L	5A	NONE
H	L	H	L	H	6A	NONE
H	L	H	H	L	7A	NONE
H	L	H	H	H	8A	NONE
H	H	L	L	L	NONE	1B
H	H	L	L	H	NONE	2B
H	H	L	H	L	NONE	3B
H	H	L	H	H	NONE	4B
H	H	H	L	L	NONE	5B
H	H	H	L	H	NONE	6B
H	H	H	H	L	NONE	7B
H	H	H	H	H	NONE	8B

* For 16-Channel single-ended function, tie 'out A' to 'out B', for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

HI-516 USED AS A DIFFERENTIAL 8-CHANNEL MULTIPLEXER

A_3 CONNECT TO V^- SUPPLY				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

HARRIS

HI-518

8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer

FEATURES

- ACCESS TIME (TYP) 80ns
- SETTLING TIME (0.1%) 250ns
- LOW LEAKAGE I_S (OFF) 50pA
  I_D (OFF) 100pA
- LOW CAPACITANCE (TYP) C_S (OFF) 2pF
  C_D (OFF) 10pF
- HIGH OFF ISOLATION @ (1MHz) 75dB
- SINGLE ENDED TO DIFFERENTIAL MODE SELECTABLE (SDS)
- LOGIC LEVEL SELECTABLE (LLS)
- LOW CHARGE INJECTION 0.3pC

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

The HI-518 is a monolithic, high performance, high speed Analog Multiplexer, constructed utilizing the Harris Dielectrically isolated CMOS process.

This device has the added feature that it can be user programmed either as a single ended 8-channel multiplexer by connecting 'out A' to 'out B' and using A2 as a digital address input, or as a 4-channel differential multiplexer by connecting A2 to the V^- supply.

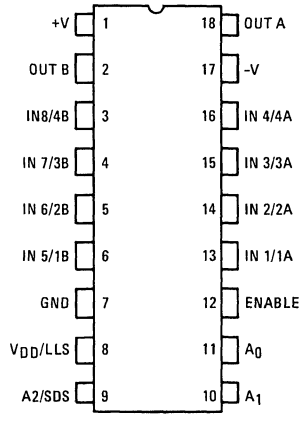
TTL or CMOS compatibility is also selectable. Low leakage current, I_D off < 100pA @ 25°C, and fast settling, 250ns to 0.1%, characteristics of this device make it an ideal choice for high speed data acquisition systems, precision instrumentation and industrial process controls.

The HI-518 is available in an 18 lead Dual-in-Line Package. The HI-518-5 is specified for operation over 0°C to +75°C, and the HI-518-2 over -55°C to +125°C. Processing to MIL-STD-883A Class B screening is available by selecting the HI-518-8.

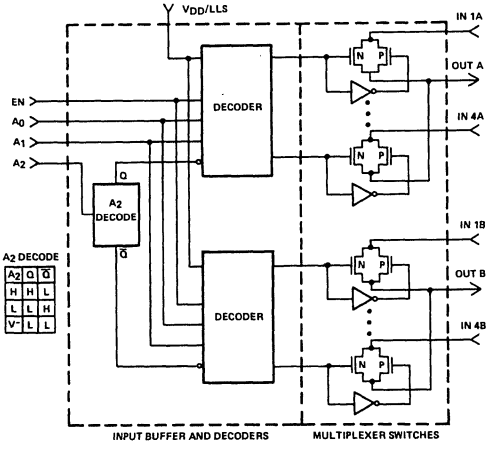
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL DIAGRAM



4

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:

TTL	$-6V < V_{AH} < +6V$	
	A2 V_{SUPPLY} (-)	-2V
CMOS	V_{SUPPLY}(+)	+2V
	GND	-2V

Analog Input Voltage:

V_S	V_{SUPPLY}(+)	+2V
	V_{SUPPLY}(-)	-2V

Voltage Between Supply Pins	33V
Total Power Dissipation*	725mW
Operating Temperature Ranges:	
HI-518-2	-55°C to +125°C
HI-518-5	0°C to 75°C
Storage Temperature Range	-65°C to 150°C
*Derate 8mW/°C above t_A	75°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = Open (Note 6).

PARAMETER	TEMP	-55°C to +125°C MIN	TYP	MAX	0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON} On Resistance (Note 1)	+25°C		480	750		480	750	Ω
	Full		700	1000		700	1000	Ω
I_S (OFF) Off Input	+25°C		0.05			0.05		nA
Leakage Current	Full		0.60	50		0.60	50	nA
I_D (OFF) Off Output	+25°C		0.10			0.10		nA
Leakage Current	Full		0.30	50		0.30	50	nA
I_D (ON) On Channel	+25°C		0.10			0.10		nA
Leakage Current	Full		0.30	50		0.30	50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AL} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AH} Input Leakage Current (Low)	Full		4	20		4	20	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		80	125		80	125	
	Full		110	150		110	150	ns
t_{OPEN}, Break before make Delay	+25°C		20			20		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		80	150		80	150	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		60	125		60	125	ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		
Charge Injection (Note 2)	+25°C		0.3			0.3		pC
Off Isolation (Note 3)	+25°C		86			86		dB
C_S (OFF) Channel Input Capacitance	+25°C		1.9			1.9		pF
C_D (OFF) Channel Output Capacitance	+25°C		10			10		pF
C_A, Digital Input Capacitance	+25°C		3			3		pF
CDS (OFF) Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		360	450		360	540	mW
I+, Current (Note 4)	Full		12	15		12	18	mA
I⁻, Current (Note 4)	Full		12	15		12	18	mA
I+, Standby (Note 5)	Full		11.5	15		11.5	18	mA
I⁻, Standby (Note 5)	Full		11.5	15		11.5	18	mA

NOTES:

1. $V_{IN} = \pm 10V$, $I_{OUT} = -100\mu A$
2. $V_{IN} = 0V$, $C_L = 100pF$, Enable Input pulse = 3V, f = 500kHz.
3. $V_{EN} = 0.8V$, $V_S = 3V_{RMS}$, f = 500kHz, $C_L = 40pF$, $R_L = 1k$. Due to the pin to pin capacitance between IN 8/4B (Pin 3) and Out B (Pin 2) channel 8/4B exhibits 60dB of Off Isolation under the above test conditions.
4. $V_{EN} = +2.4V$.
5. $V_{EN} = 0.8V$.
6. V_{DD}/LLS Pin = Open or grounded for TTL compatibility. V_{DD}/LLS Pin = V_{DD} for CMOS compatibility.

HI-518 USED AS 8 CHANNEL MULTIPLEXER OR
4 CHANNEL DIFFERENTIAL MULTIPLEXER

USE A_2 AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	NONE
H	L	L	H	2A	NONE
H	L	H	L	3A	NONE
H	L	H	H	4A	NONE
H	H	L	L	NONE	1B
H	H	L	H	NONE	2B
H	H	H	L	NONE	3B
H	H	H	H	NONE	4B

HI-518 USED AS DIFFERENTIAL
4 CHANNEL MULTIPLEXER

A_2 CONNECT TO V^- SUPPLY			ON CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	NONE	NONE
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

HARRIS

HI-524

4 Channel Video Multiplexer

FEATURES

- CROSSTALK (10MHz) > 60dB
- FAST ACCESS TIME 150ns
- FAST SETTLING TIME (0.01%) 600ns
- TTL COMPATIBLE

APPLICATIONS

WIDEBAND SWITCHING

- RADAR
- TV VIDEO
- ECM

DESCRIPTION

The HI-524 is a four channel CMOS analog multiplexer designed to process single-ended video signals with bandwidths up to 10MHz. The chip includes a 1 of 4 decoder for channel selection and an Enable input to inhibit all channels (chip select).

Three CMOS transmission gates are used in each channel, as compared to the single gate in more conventional CMOS multiplexers. This provides a double barrier to the unwanted coupling of signals from each input to the output. In addition, Dielectric Isolation (DI) processing helps to insure that Crosstalk exceeds 60dB at 10MHz.

The HI-524 is designed to operate into a wideband buffer amplifier such as the HARRIS HA-5190. The multiplexer chip includes two "on" switches in series, for use as a feedback element with the amplifier. This feedback resistance matches and tracks the channel R_{ON} resistance, to minimize the amplifier V_{OS} and its variation with temperature.

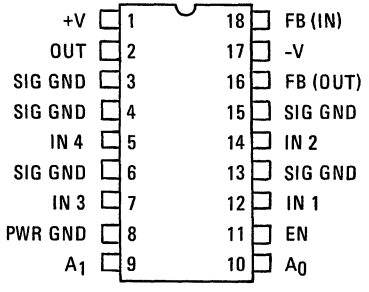
The HI-524 is well suited to the rapid switching of video signals in telemetry, instrumentation, radar and video systems. It is packaged in an 18 pin ceramic DIP and operates on ±15V supplies.

The performance levels available are: HI1-524-2, -55°C to +125°C operating range; HI1-524-5, 0°C to +75°C operating range and HI1-524-8, -55°C to+125°C operating range plus 100% screening per MIL-STD-883/Method 5004/Class B. Chips for hybrid applications are designated HI0-524-6.

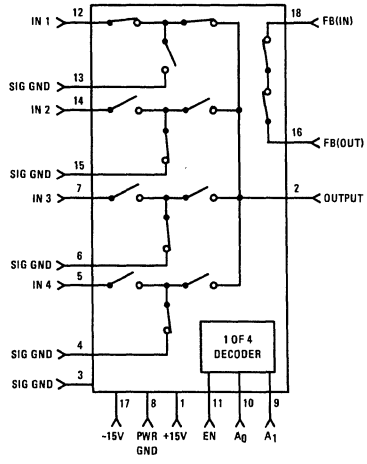
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL DIAGRAM



TRUTH TABLE

A_1	A_0	EN	ON CHANNEL
X	X	L	NONE
L	L	H	1*
L	H	H	2
H	L	H	3
H	H	H	4

* CHANNEL 1 IS SHOWN SELECTED IN THE DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Digital Input Overvoltage:
$-6V < V_{AH} < +6V$

Analog Input (V_S) or Output (V_O)
$+V_{SUPPLY}$ +2V
$-V_{SUPPLY}$ -2V

Voltage Between Supply Pins	33V
Either Supply to Ground	16.5V
Total Power Dissipation	750mW
Operating Temperature Range:	
HI-524-2, -8	-55°C to +125°C
HI-524-5	0°C to 75°C
Storage Temperature Range	-65°C to 150°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} = (Logic Level Low) = +0.8V; V_{EN} = +2.4V

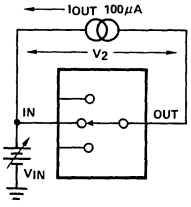
PARAMETER	TEMP	HI-524-2, -8 -55°C to +125°C MIN	TYP	MAX	HI-524-5 0°C to +75°C MIN	TYP	MAX	UNITS
Analog Channel Characteristics								
V_S, Analog Signal Range	Full	-10		+10	-10		+10	V
R_{ON}, On Resistance (Note 1)	+25°C		700			700		Ω
	Full			1.5K			1.5K	Ω
I_S (OFF), Off Input Leakage Current (Note 2)	+25°C		0.2			0.2		nA
	Full			50			50	nA
I_D (OFF), Off Output Leakage Current (Note 2)	+25°C		0.2			0.2		nA
	Full			50			50	nA
I_D (ON), On Channel Leakage Current (Note 2)	+25°C		0.7			0.7		nA
	Full			50			50	nA
3dB Bandwidth: (Note 3)	Full		20			20		MHz
Digital Input Characteristics								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
I_{AL} Current (Low)	Full		4	25		4	25	μA
Switching Characteristics								
t_A, Access Time (Note 4)	+25°C		150	300		150	300	ns
	Full							ns
t_{OPEN}, Break before make delay (Note 4)	+25°C		20			20		ns
t_{ON} (EN), Enable Delay (ON), R_L = 500Ω	+25°C		180	300		180		ns
t_{OFF} (EN), Enable Delay (OFF), R_L = 500Ω	+25°C		180	250		180		ns
Settling Time (0.1%) (Note 4)	+25°C		200			200		ns
(0.01%)	+25°C		600			600		ns
Crosstalk (Note 5)	+25°C		-65			-65		dB
C_S (OFF), Channel Input Capacitance	+25°C			6		6		pF
C_D (OFF), Channel Output Capacitance	+25°C			4		4		pF
C_A, Digital Input Capacitance	+25°C			5		5		pF
Power Requirements								
P_D, Power Dissipation	Full		540			540		mW
I^+, Current (V_{EN} = 2.4V) (Note 6)	Full		18	25		18	25	mA
I^-, Current (V_{EN} = 2.4V) (Note 6)	Full		18	25		18	25	mA
I^+, Standby (V_{EN} = 0.8V) (Note 6)	Full		18	25		18	25	mA
I^-, Standby (V_{EN} = 0.8V) (Note 6)	Full		18	25		18	25	mA

1. V_{IN} = 0V; I_{OUT} = 100 A (See Test Circuit # 1)
2. $V_O = \pm 10V$; $V_S = \mp 10V$ (See Test Circuits # 2, 3, 4)
3. MUX output is buffered with HA-5190 as shown in Applications section.
4. (See Test Circuit # 5)
5. V_{IN} = 10MHz, $3V_{p-p}$ on one channel, with any other channel selected. (Worst case is channel 3 selected with input on channel 4.) MUX output is buffered with HA-5190 as shown in Applications section. Terminate all channels with 75Ω .
6. Supply currents vary less than 0.5mA for switching rates from DC to 2MHz.

(UNLESS OTHERWISE SPECIFIED T_A = 25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V)

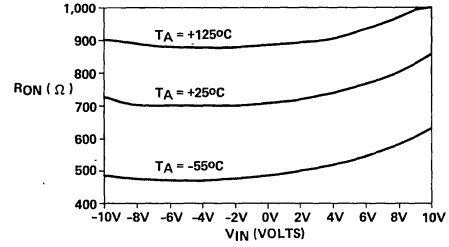
ON RESISTANCE

TEST CIRCUIT NO. 1

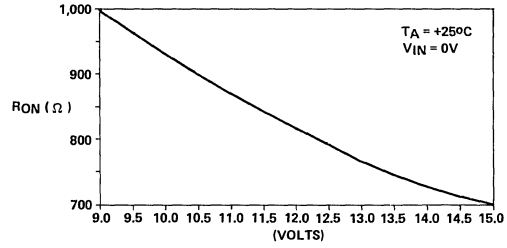


$$R_{ON} = \frac{V_2}{100\mu A}$$

ON RESISTANCE VS. ANALOG INPUT VOLTAGE



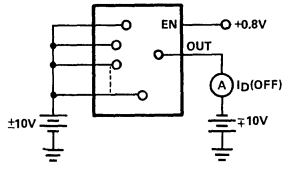
ON RESISTANCE VS. SUPPLY VOLTAGE



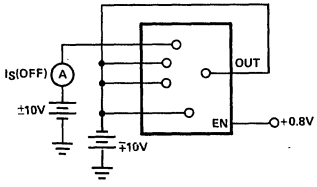
4

LEAKAGE CURRENT

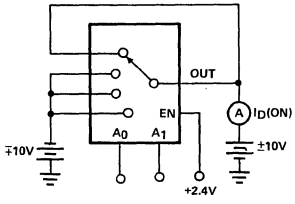
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

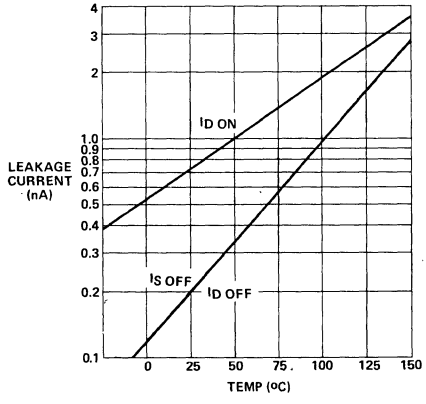


TEST CIRCUIT NO. 4*



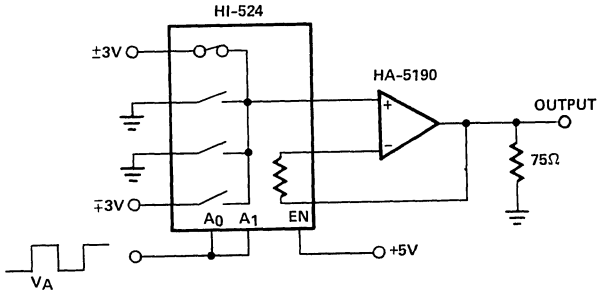
*Two measurements per channel:
+10V/-10V and -10V/+10V.
(Two measurements per device for $I_{D(OFF)}$:
+10V/-10V and -10V/+10V.)

LEAKAGE CURRENT VS. TEMPERATURE

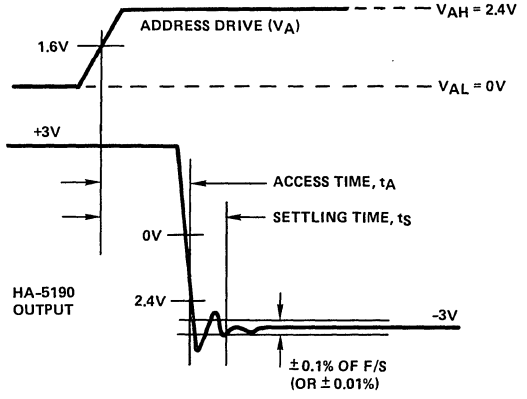


TEST CIRCUIT NO. 5

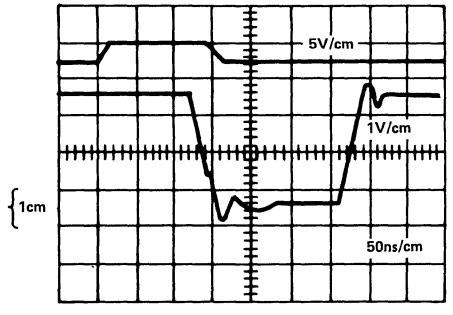
SETTLING TIME
ACCESS TIME
BREAK-BEFORE-MAKE DELAY



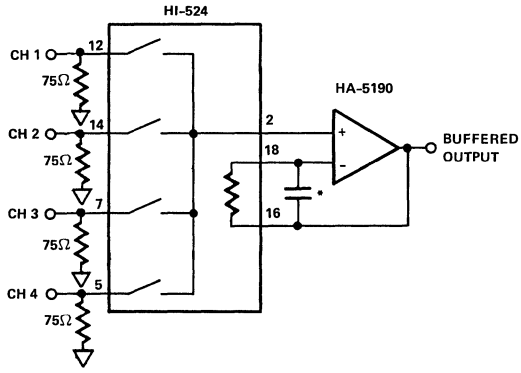
(USE DIFFERENTIAL COMPARATOR PLUG-IN ON SCOPE FOR SETTLING TIME MEASUREMENT.)



ACCESS TIME



- Often it is desirable to buffer the HI-524 output, to avoid loading errors due to the channel "ON" resistance:



* APPROXIMATELY 10pF SHOULD REMOVE ANY LOW LEVEL INSTABILITY AT THE OUTPUT.

- The main requirement for the buffer amplifier is a full power bandwidth high enough to avoid attenuation of the video signal. The HARRIS HA-5190 is well suited for this purpose; in fact the HI-524 was designed to be compatible with the 5190. This 524/5190 combination offers a 3dB bandwidth of at least 20MHz for a 3V peak-to-peak input. As mentioned earlier, the 524 includes a feedback element for the amplifier which matches and tracks the channel "ON" resistance.

- Note that the on-chip feedback element between pins 16 and 18 includes two switches in series, to simulate a channel resistance. These switches open for V_{EN} = Low. This allows two or more HI-524's to operate into one HA-5190, with their feedback elements connected in parallel. Thus, only the selected multiplexer provides feedback, and the amplifier remains stable.

- All HI-524 package pins labeled 'SIG GND' (pins 3, 4, 6, 13, 15) should be externally connected to signal ground for best Crosstalk performance.

- Bypass capacitors (0.1 to 1.0μF) are recommended from each HI-524 supply pin to power ground (pins 1 and 17 to pin 8). Locate the buffer amplifier near the HI-524 so the two capacitors may bypass both devices.

- If an analog input 1V or greater is present when supplies are off, a low resistance is seen from that input to a supply line. (For example, the resistance is approximately 160Ω for an input of -3V.) Current flow may be blocked by a diode in each supply line, or limited by a resistor in series with each channel. The best solution, of course, is to arrange that no digital or analog inputs are present when the power supplies are off.

HARRIS

HI-539

Monolithic, Four Channel, Low Level, Differential Multiplexer

FEATURES

- DIFFERENTIAL PERFORMANCE, TYP.:
  - LOW ΔR_{ON}, +125°C — 5.5Ω
  - LOW $\Delta I_{D(ON)}$, +125°C — 0.6nA
  - LOW Δ(CHARGE INJECTION) — 0.1pC
  - LOW CROSSTALK — -120dB
- SETTLING TIME, ±0.01% — 900ns
- WIDE SUPPLY RANGE — ±5V TO ±18V
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- LOW LEVEL DATA ACQUISITION
- PRECISION INSTRUMENTATION
- TEST SYSTEMS

DESCRIPTION

The Harris HI-539 is a monolithic, four channel, differential multiplexer. Two digital inputs are provided for channel selection, plus an Enable input to disconnect all channels.

Performance is guaranteed for each channel over the range ± 10V, but is optimized for low level differential signals. Leakage current, for example, which varies slightly with input voltage, has its distribution centered at zero for zero input volts.

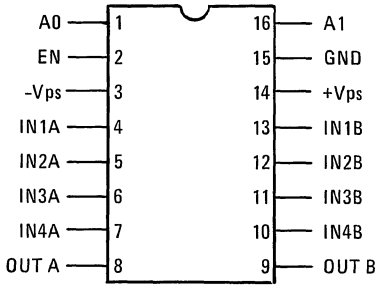
In most monolithic multiplexers, the net differential offset due to thermal effects becomes significant for low level signals. This problem is minimized in the HI-539 by symmetrical placement of critical circuitry with respect to the few heat producing devices.

The HI-539 will be offered in both commercial and military temperature ranges, with screening available for MIL-STD-883, Class B. Supply voltages are ± 15V and power consumption is only 2.5mW. The package is a 16 pin ceramic DIP.

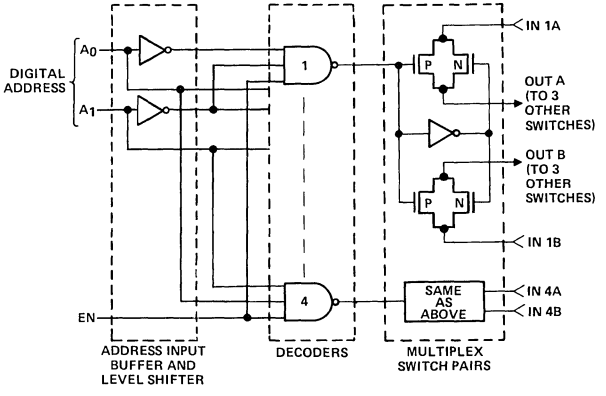
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL DIAGRAM



4

ABSOLUTE MAXIMUM RATINGS

Voltage Between Supply Pins (V_{ps+}, V_{ps-}) 40V

Voltage from either Supply to Ground 20V

Analog Input Voltage, V_S $V_{ps-} \leq V_S \leq V_{ps+}$

Digital Input Voltage, V_A $V_{ps-} \leq V_A \leq V_{ps+}$

Storage Temperature Range -65°C to +150°C

Internal Power Dissipation (Derate 8mW/°C above +75°C ambient) 725mW

Operating Temperature Range

HI-539-2, -8 -55°C to +125°C

HI-539-4 -25°C to +85°C

HI-539-5 0°C to +75°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified) Supplies = ±15V, V_{EN} = +4.0V, V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V. See the Performance Characteristics Section for test circuits and conditions. Selected parameters are defined in the Definitions Section.

PARAMETER	TEMP	HI-539-2, -8 TYP	HI-539-2, -8 MAX (MIN)	HI-539-4, -5 TYP	HI-539-4, -5 MAX (MIN)	UNITS
ANALOG CHANNEL CHARA'S						
V_S, Analog Signal Range	Full		(-10)/+10		(-10)/+10	V
R_{ON}, On Resistance V_{IN} = 0V	+25°C	650	850	650	850	Ω
V_{IN} = ± 10V	+25°C	700	900	700	900	Ω
V_{IN} = 0V	Full	950	1.3K	800	1K	Ω
V_{IN} = ± 10V	Full	1.1k	1.4k	900	1.1k	Ω
ΔR_{ON} [Side A - Side B]						
V_{IN} = 0V	+25°C	4.0	24	4.0	24	Ω
V_{IN} = ± 10V	+25°C	4.5	27	4.5	27	Ω
V_{IN} = 0V	Full	4.75	28	4.0	24	Ω
V_{IN} = ± 10V	Full	5.5	33	4.5	27	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 1)						
Condition 0V	+25°C	30	200	30	200	pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{S(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3	100	3	100	pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 1)						
Condition 0V	+25°C	30	200	30	200	pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{D(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3	100	3	100	pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(ON)}$, On Channel Leakage Current (Note 1)						
Condition 0V	+25°C	50	200	50	200	pA
Condition ± 10V	+25°C	150		150		pA
Condition 0V	Full	5	25	0.5	2.5	nA
Condition ± 10V	Full	6	40	0.8	4.0	nA
$\Delta I_{D(ON)}$ [Side A - Side B]						
Condition 0V	+25°C	10	100	10	100	pA
Condition ± 10V	+25°C	30		30		pA
Condition 0V	Full	0.5	5	0.05	0.5	nA
Condition ± 10V	Full	0.6	6	0.08	0.8	nA
ΔV_{OS}, Differential Offset Voltage	+25°C	0.02	0.04	0.02	0.04	μV
	Full	0.70	10	0.08	1.0	μV

PARAMETER	TEMP	HI-539-2, -8 TYP	HI-539-2, -8 MAX (MIN)	HI-539-4, -5 TYP	HI-539-4, -5 MAX (MIN)	UNITS
DIGITAL INPUT CHARACTERISTICS						
V_{AL}, Input Low Threshold	Full		0.8		0.8	V
V_{AH}, Input High Threshold	Full		(4.0)		(4.0)	V
I_{AH}, Input Leakage Current (High)	Full		1		1	μA
I_{AL}, Input Leakage Current (Low)	Full		1		1	μA
SWITCHING CHARACTERISTICS						
T_A, Access Time	+25°C	250	750	250	750	ns
	Full	450	1,000	450	1,000	ns
T_{open}, Break-Before-Make Delay	+25°C	85	(30)	85	(30)	ns
	Full		(30)		(30)	ns
$T_{ON(EN)}$, Enable Delay On	+25°C	250	750	250	750	ns
	Full		1,000		1,000	ns
$T_{OFF(EN)}$, Enable Delay Off	+25°C	160	650	160	650	ns
	Full		900		900	ns
Settling Time, to ±0.01%	+25°C	0.9		0.9		μs
Charge Injection (Output)	Full	3		3		pC
Δ Charge Injection (Output)	Full	0.1		0.1		pC
Charge Injection (Input)	Full	10		10		pC
Differential Crosstalk (Note 3)	+25°C	124		124		dB
Single Ended Crostalk (Note 3)	+25°C	100		100		dB
$C_{S(OFF)}$, Channel Input Capacitance	Full	5		5		pF
$C_{D(OFF)}$, Channel Output Capacitance	Full	7		7		pF
$C_{D(ON)}$, Channel On Output Capacitance	Full	17		17		pF
C_{DS}, Input to Output Capacitance (Note 4)	Full	0.08		0.08		pF
C_A, Digital Input Capacitance	Full	3		3		pF
POWER REQUIREMENTS						
P_D, Power Dissipation	+25°C	2.5		2.5		mW
	Full		45		45	mW
I+ Current	+25°C	0.150		0.150		mA
	Full		2.0		2.0	mA
I- Current	+25°C	0.001		0.001		mA
	Full		1.0		1.0	mA
±V, Supply Voltage Range	Full	±15	(±5)/ ±18	±15	(±5)/ ±18	V

NOTES

1. See Test Circuits #2, 3, 4. The condition ±10V means:

   $I_{S(OFF)}$ and $I_{D(OFF)}$: (V_S = +10V, V_D = -10V), then (V_S = -10V, V_D = +10V)

   $I_{D(ON)}$: (+10V, then -10V)

2. ΔV_{OS} (Exclusive of thermocouple effects) = $R_{ON}\ \Delta I_{D(ON)} + I_{D(ON)}\ \Delta R_{ON}$.

   See Applications section for discussion of additional V_{OS} error.

3. V_{IN} = 1kHz, $15V_{p-p}$ on all but the selected channel. See Test Circuit #9.

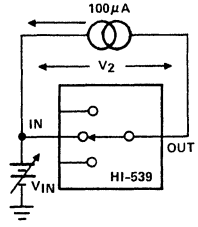
4. Calculated from typical Single-Ended Crosstalk performance.

(UNLESS OTHERWISE SPECIFIED T_A = 25°C, V_{SUPPLY} = ± 15V, V_{AH} = +4V AND V_{AL} = +0.8V)

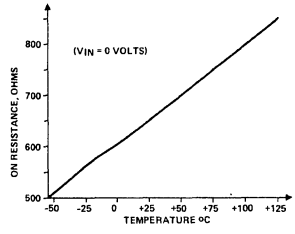
ON RESISTANCE MEASUREMENT

TEST CIRCUIT NO. 1

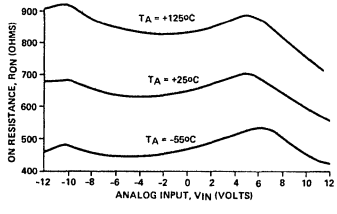
$R_{ON} = \frac{V_2}{100\mu A}$



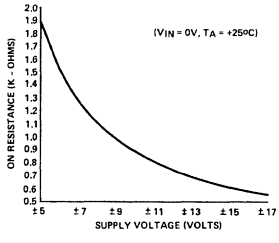
ON RESISTANCE vs. TEMPERATURE



ON RESISTANCE vs. ANALOG INPUT VOLTAGE



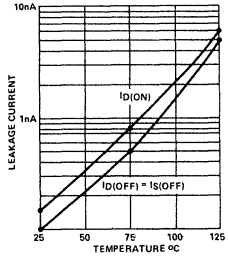
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



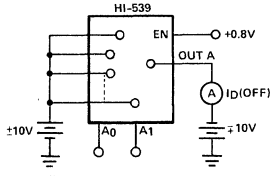
4

LEAKAGE CURRENT

LEAKAGE CURRENT vs. TEMPERATURE

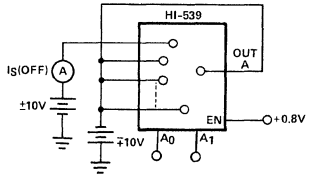


TEST CIRCUIT NO. 2*



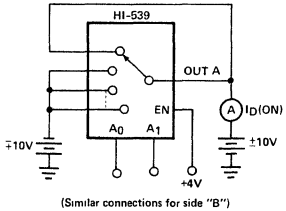
(Similar connections for side "B")

TEST CIRCUIT NO. 3*



(Similar connections for side "B")

TEST CIRCUIT NO. 4*

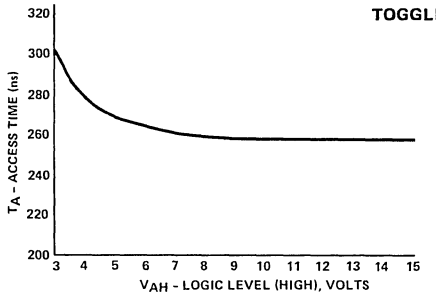


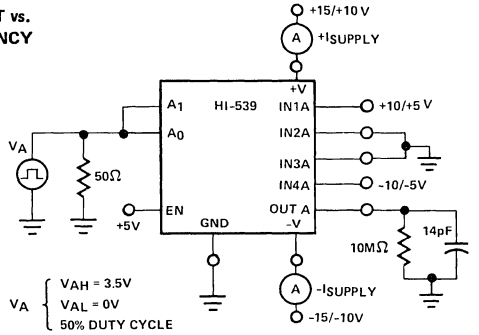
(Similar connections for side "B")

*Three measurements = +10V/-10V, -10V/+10V, and 0V

TEST CIRCUIT NO. 5

SUPPLY CURRENT vs. TOGGLE FREQUENCY

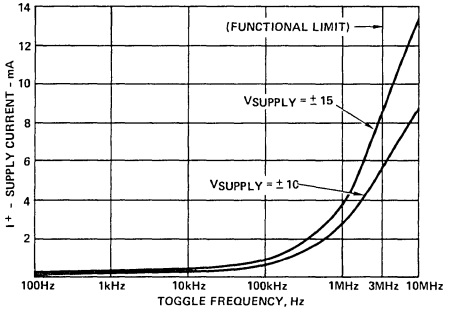


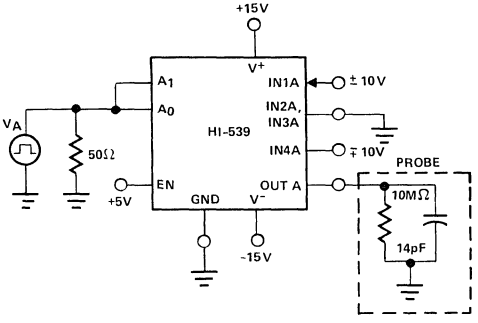


(SIMILAR CONNECTIONS FOR "B" SIDE)

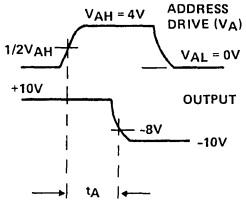
TEST CIRCUIT NO. 6

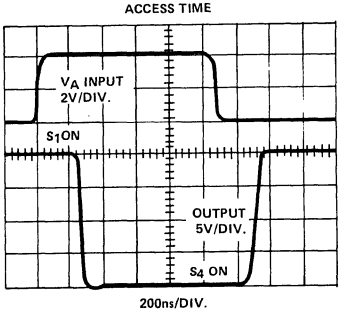
ACCESS TIME vs. LOGIC LEVEL (HIGH)





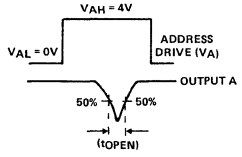
(SIMILAR CONNECTIONS FOR "B" SIDE)



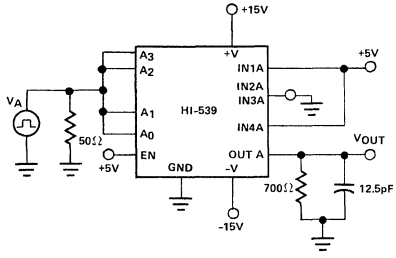


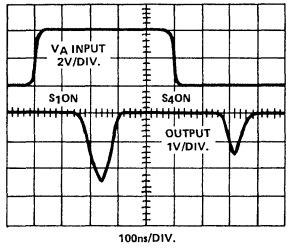
TEST CIRCUIT NO. 7

ENABLE DRIVE



BREAK-BEFORE-MAKE DELAY (t_{OPEN})

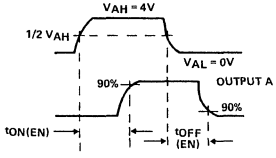




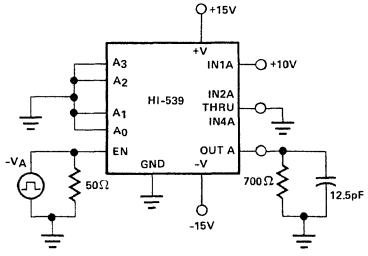
(SIMILAR CONNECTION FOR "B" SIDE)

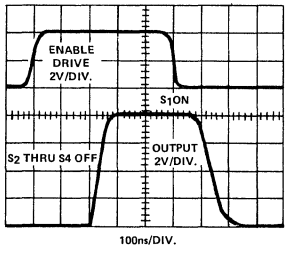
TEST CIRCUIT NO. 8

ENABLE DRIVE



ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

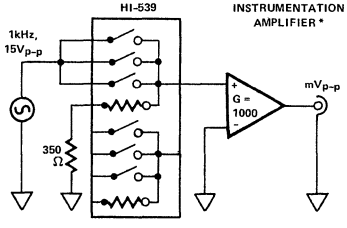




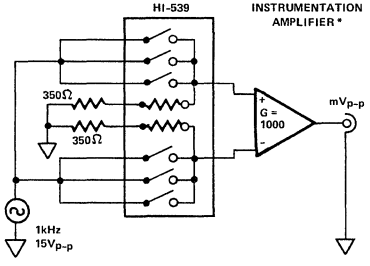
(SIMILAR CONNECTION FOR "B" SIDE)

TEST CIRCUIT NO. 9

SINGLE-ENDED CROSSTALK



DIFFERENTIAL CROSSTALK



* AD606 OR BB3630, FOR EXAMPLE

DEFINITIONS

CHARGE INJECTION – Charge (in pC) transferred, during a transition between channels, through the internal gate-to-channel capacitance. The resulting voltage error varies inversely with the output (or input) capacitance.

CROSSTALK – Signal at the multiplexer output, coupling though the C_{DS} capacitance of an OFF channel. Amplitude is proportional to source resistance for the ON channel. See Test Circuit # 9 for single-ended and differential versions of crosstalk.

DIFFERENTIAL LEAKAGE CURRENT ($\Delta I_{S(OFF)}$, $\Delta I_{D(OFF)}$, $\Delta I_{D(ON)}$) – The absolute difference in leakage for the two sides of a channel.

DIFFERENTIAL OFFSET VOLTAGE (ΔV_{OS}) – Voltage between the multiplexer output terminals with both channel input terminals shorted to ground.

DIFFERENTIAL ON RESISTANCE (ΔR_{ON}) – The absolute difference in On Resistance for the two sides of a channel.

INPUT TO OUTPUT CAPACITANCE (C_{DS}) – Capacitance from one input terminal of a channel to the corresponding output of the multiplexer. This parameter is responsible for Crosstalk.

APPLICATIONS

GENERAL

The HI-539 accepts inputs in the range -15V to +15V, with performance guaranteed over the ±10V range. At these higher levels of analog input voltage it is comparable to the HI-509, and is plug-in compatible with that device (as well as the HI-509A). However, as mentioned earlier, the HI-539 was designed to introduce minimum error when switching low level inputs.

Special care is required in working with these low level signals. The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded, differential signal path is essential, especially to maintain a noise level below 50 μVrms.

LOW LEVEL SIGNAL TRANSMISSION

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area, to guard against pickup of electromagnetic interference, and the twisted pair should be shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only one tenth as much leakage capacitance to ground per foot. A key requirement for the transmission cable is that it presents a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled in phase to both conductors, and may be rejected as common mode voltage by a differential amplifier connected to the multiplexer output.

Coaxial cable is not suitable for low-level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

Table 1

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 oz. Cu.)	D.C. RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT	
				AT 60Hz	AT 10kHz
18	0.47"	0.0064Ω	0.36μH	0.0064Ω	0.0235Ω
20	0.30"	0.0102Ω	0.37μH	0.0102Ω	0.0254Ω
22	0.19"	0.0161Ω	0.37μH	0.0161Ω	0.0288Ω
24	0.12"	0.0257Ω	0.40μH	0.0257Ω	0.0345Ω
26	0.075"	0.041Ω	0.42μH	0.041Ω	0.0488Ω
28	0.047"	0.066Ω	0.45μH	0.066Ω	0.0718Ω
30	0.029"	0.105Ω	0.49μH	0.105Ω	0.110Ω
32	0.018"	0.168Ω	0.53μH	0.168Ω	0.171Ω

WATCH SMALL ΔV ERRORS

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few milliohms must be considered, especially to meet an accuracy requirement of 12 bits or more.

Table 1 is a useful collection of data for calculating the effect of these short connections. (Proximity to a ground plane will lower the values of inductance.)

As an example, suppose the HI-539 is feeding a 12 bit converter system with an allowable error of ±1/2 LSB (±1.22mV). If the interface logic draws 100mA from the 5V supply, this current will produce 1.28mV across 6 inches of #24 wire; more than the error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

PROVIDE PATH FOR I_{BIAS}

The input bias current for any DC-coupled amplifier must have an external path back to the amplifier's power supply. No such path exists in Figure 1A, and consequently the amplifer output will remain in saturation.

A single large resistor (1MΩ to 10MΩ) from either signal line to power supply common will provide the required path, but a resistor on each line is necessary to preserve accuracy. A single pair of these bias current resistors on the HI-539 output may be used if their loading effect can be tolerated (each forms a voltage divider with R_{ON}). Otherwise, a resistor pair on each input channel of the multiplexer is required.

The use of bias current resistors is acceptable only if one is confident that the sum of signal plus common-mode voltage will remain within the input range of the multiplexer/amplifier combination.

Another solution is to simply run a third wire from the low side of the signal source, as in Figure 1B. This wire assures a low common-mode voltage as well as providing the path for bias currents. Making the connection near the multiplexer will save wire, but it will also unbalance the line and reduce the amplifier's common-mode rejection.

DIFFERENTIAL OFFSET, ΔV_{OS}

There are two major sources of ΔV_{OS}. That part, due to the expression ($R_{ON}\,\Delta I_D(ON) + I_D(ON)\,\Delta R_{ON}$) becomes significant with increasing temperature, as shown in the Electrical Characteristics section. The other source of offset is the thermocouple effects due to dissimilar materials in the signal path. These include silicon, aluminum, tin, nickel-iron and (often) gold, just to exit the package.

For the thermocouple effects in the package alone, the constraint on ΔV_{OS} may be stated in terms of a limit on the difference in temperature for package pins leading to any channel of the HI-539. For example, a difference of 0.13°C produces a 5μV offset. Obviously, this ΔT effect can dominate the ΔV_{OS} parameter at any temperature unless care is taken in mounting the HI-539 package.

Temperature gradients across the HI-539 package should be held to a minimum in critical applications. Locate the HI-539 far from heat producing components, with any air currents flowing lengthwise across the package.

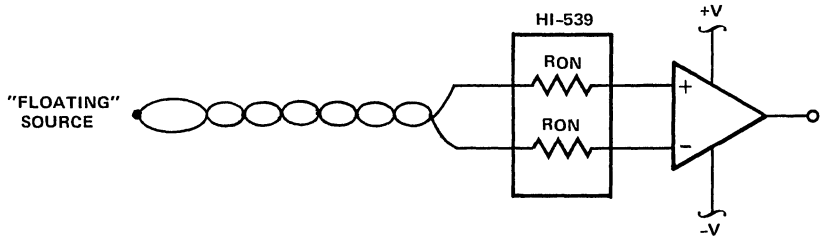


Figure 1A

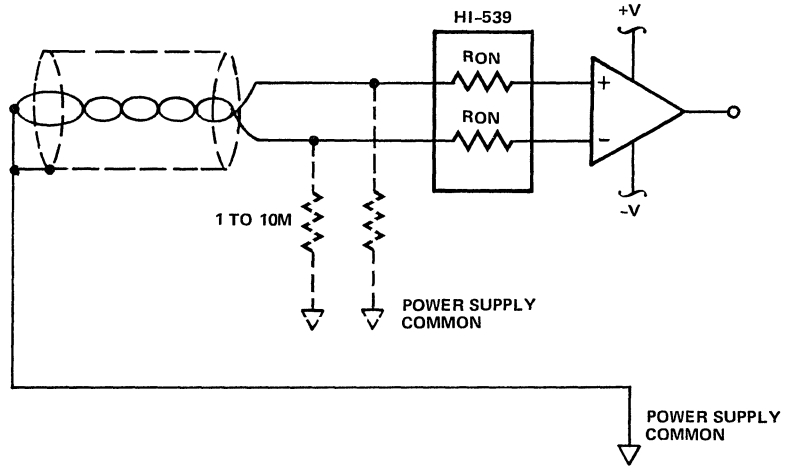


Figure 1B

The amplifier in Figure 1A is unusable because its bias currents cannot return to the power supply. Figure 1B shows two alternative paths for these bias currents: either a pair of resistors, or (better) a third wire from the low side of the signal source.

HARRIS

HI-1818A/1828A

Low Resistance
8 Channel CMOS Analog Multiplexers

FEATURES

- SIGNAL RANGE ±15V
- "ON" RESISTANCE (TYP.) 250Ω
- INPUT LEAKAGE AT +125°C (TYP.) 20nA
- ACCESS TIME (TYP.) 350ns
- POWER CONSUMPTION (TYP.) 5mW
- DTL/TTL COMPATIBLE ADDRESS
- -55°C to +125°C OPERATION

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

The HI-1818A/1828A are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250 Ω) assure optimum performance in low level or current mode applications.

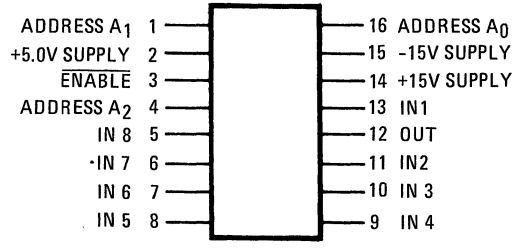
The 1818A is a single-ended 8 channel multiplexer, while the HI-1828A is a differential 4 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

The HI-1818A-2 and HI-1828A are specified over -55°C to +125°C, while the -5 versions are specified over 0°C to +75°C.

PINOUT

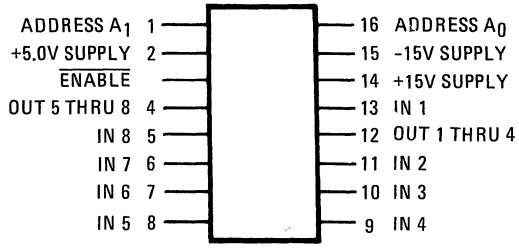
HI-1818A — Section 11 for Packaging

Top View



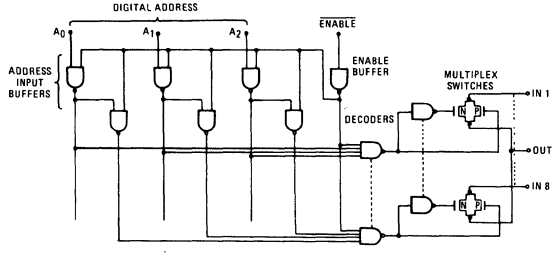
HI-1828A — Section 11 for Packaging

Top View

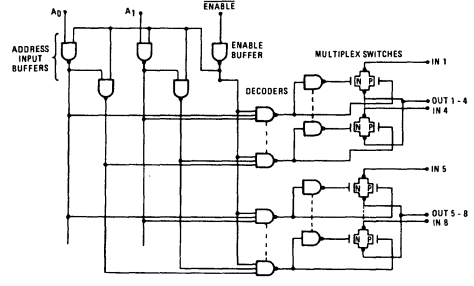


FUNCTIONAL DIAGRAM

HI-1818A



HI-1828A



4

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	V-Supply to V+ Supply
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation (Note 2)	780mW
Analog Input Voltage: V^+_{Supply} +2V		Storage Temperature Range	-65°C to +150°C
V^-_{Supply} -2V			

ELECTRICAL CHARACTERISTICS

Supplies = +15V, -15V, +5V

PARAMETER	TEMP.	HI-1818A-2/1828A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-1818A-5/1828A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_{IN}, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, ON Resistance (Note 3)	+25°C		250	400		250	400	Ω
	Full		300	500		300	500	Ω
*I_S(OFF), Input Leakage Current	Full		20	50		20	50	nA
*I_D(ON), On Channel Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
*I_D(OFF) Output Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.4			0.4	V
V_{AH}, Input High Threshold (Note 4)	Full	4.0			4.0			V
$I_{A,}$, Input Leakage Current	Full		.01	1		.01	1	μA
SWITCHING CHARACTERISTICS								
T_S, Access Time (Note 5)	+25°C		350			350		ns
Break-Before-Make Delay	+25°C		100			100		ns
Settling Time (0.1%)	+25°C		1.08			1.08		μs
(0.025%)	+25°C		2.8			2.8		μs
C_{IN}, Channel Input Capacitance	+25°C		4			4		pF
C_{OUT}, Channel Output Capacitance								
(HI-1818A)	+25°C		20			20		pF
(HI-1828A)	+25°C		10			10		pF
C_{DS}(OFF), Drain-To-Source Capacitance	+25°C		0.6			0.6		pF
$C_{D,}$ Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		5			5		mW
P_{DS}, Standby Power (Note 6)	Full		5			5		mW
* I_+, Current Pin 14	Full		0.1	0.5		0.1	1	mA
* I_-, Current Pin 15	Full		0.3	1		0.3	2	mA
* I_L, Current Pin 2	Full		0.3	1		0.3	2	mA

NOTES:
1. Voltage ratings apply when voltages at all other pins are within their normal operating ranges.
2. Derate 9.25 mW/°C above 75°C.
3. V_{OUT} = ± 10V I_{OUT} = - 1mA.
4. To drive from DTL/TTL circuits, 1K pull-up resistors to + 5.0V supply are recommended.
5. Time measured to 90% of final output level; V_{OUT} = - 5.0V to +5.0V, Digital Inputs = 0V to + 4.0V.
6. Voltage at Pin 3, $\overline{ENABLE}$ = + 4.0V.

* 100% Tested for Dash 8 at +25°C and +125°C Only.

TRUTH TABLES

HI-1818A

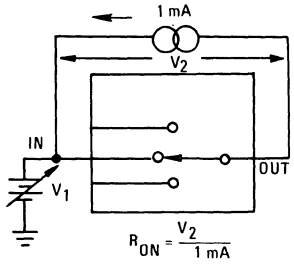
ADDRESS A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	NONE

HI-1828A

ADDRESS A_1	A_0	$\overline{EN}$	"ON" CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	NONE

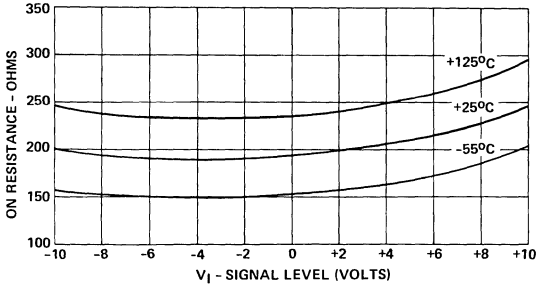
4

ON RESISTANCE vs ANALOG SIGNAL LEVEL

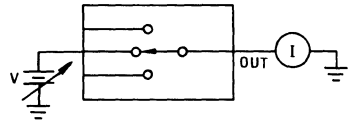


$$R_{ON} = \frac{V_2}{1\ mA}$$

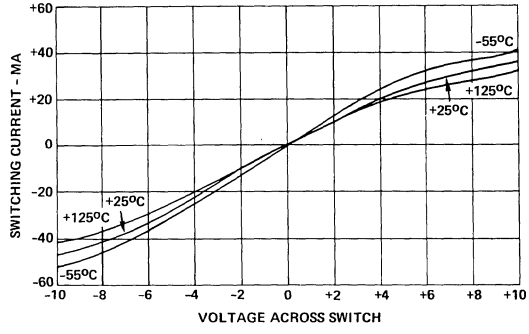
Test Circuit



ON CHANNEL CURRENT vs VOLTAGE

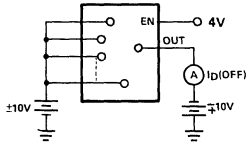


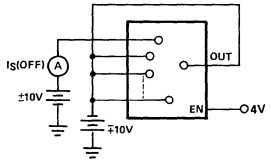
Test Circuit



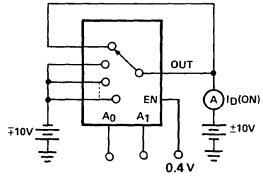
LEAKAGE CURRENTS vs TEMPERATURE

OFF LEAKAGE

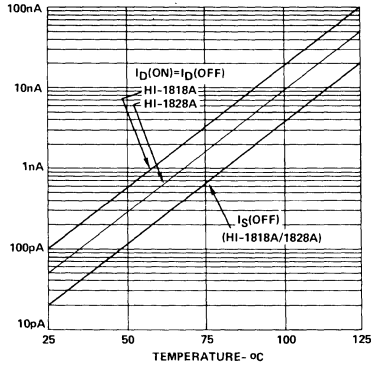




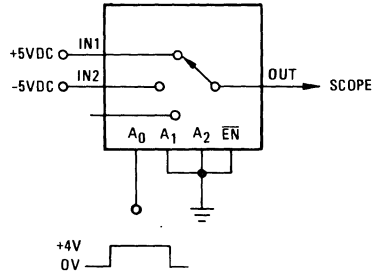
ON LEAKAGE

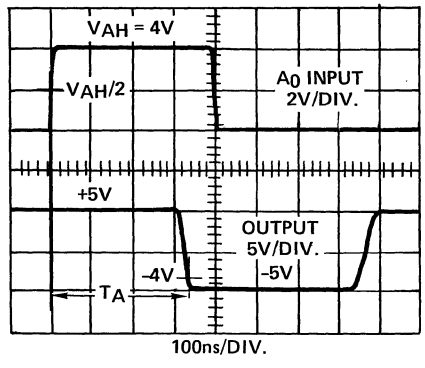


*Two measurements per channel:
+10V/-10V and -10V/+10V
(Two measurements per device for ID(OFF)
+10V/-10V and -10V/+10V.)

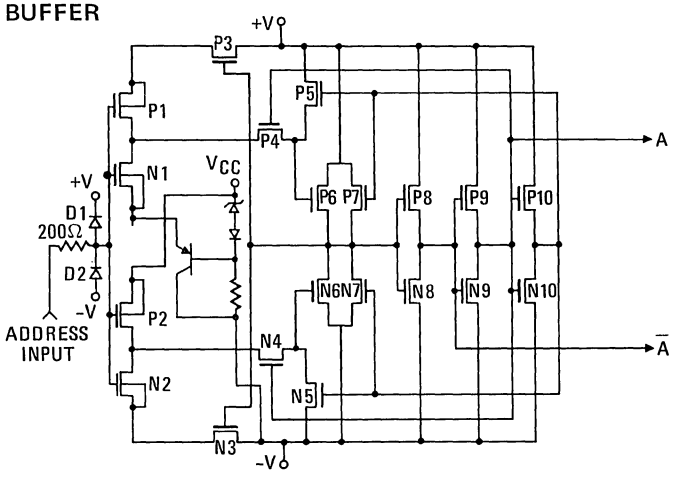


ACCESS TIME





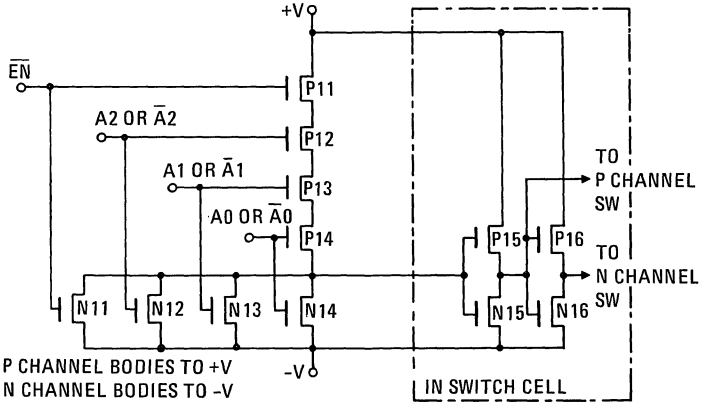
ADDRESS INPUT BUFFER



ALL N-CHANNEL BODIES TO V-

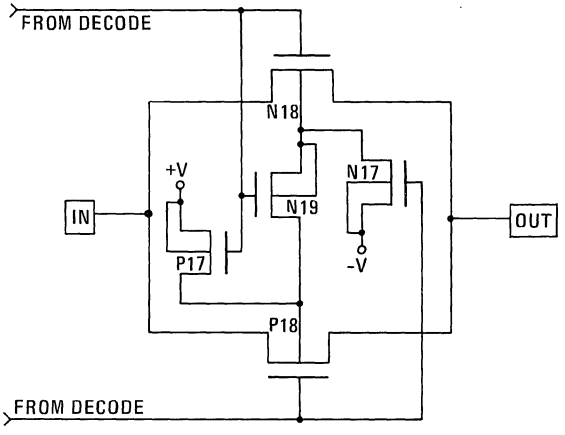
ALL P-CHANNEL BODIES TO V+ UNLESS OTHERWISE INDICATED.

DECODER GATE



A2 OR Ā2 NOT USED FOR HI-1828A

MULTIPLEX SWITCH



4

5

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

HARRIS

HA-2420/2425

Fast Sample and Hold

FEATURES

- LOW DROOP RATE (C_H = 1000pF) 5μV/ms
- LOW CHARGE TRANSFER 5pC
- FAST ACQUISITION TIME (10V STEP TO .01%) 5μs
- HIGH SLEW RATE 7V/μs
- BANDWIDTH 2.5MHz
- LOW APERTURE TIME 30ns
- TTL COMPATIBLE CONTROL INPUT

APPLICATIONS

- A TO D CONVERSION SYSTEMS
- D TO A DEGLITCHER
- AUTO ZERO SYSTEMS
- PEAK DETECTOR
- GATED OP AMP

DESCRIPTION

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier.

With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

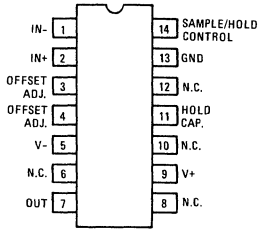
Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

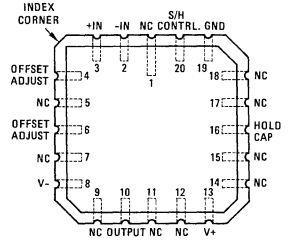
PINOUT

Section 11 for Packaging

TOP VIEW

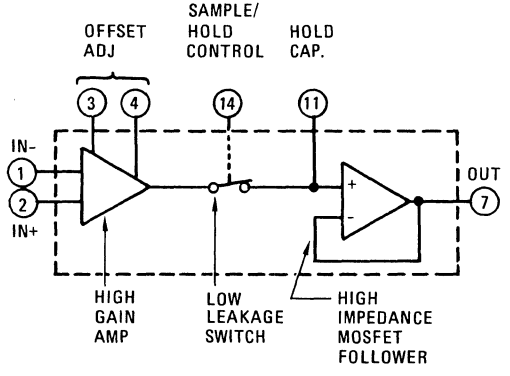


14 PIN DIP



LEADLESS CHIP CARRIER (LCC) PACKAGE

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Operating Temperature Range	
Differential Input Voltage	±24V	HA-2420-2/8	$-55^{o}C \leq T_A \leq +125^{o}C$
Digital Input Voltage (Pin 14)	+8V, -15V	HA-2425-5	$0^{o}C \leq T_A \leq +75^{o}C$
Output Current	Short Circuit Protected	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$
Internal Power Dissipation	300mW (Note 7)		

ELECTRICAL CHARACTERISTICS

Test Conditions (Unless otherwise specified) $V_{SUPPLY} = \pm 15.0V$; $C_H = 1000pF$; Digital Input (Pin 14), $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold)

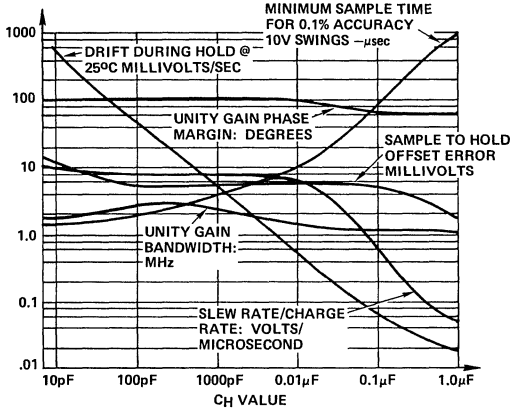
PARAMETER	TEMP	HA-2420-2 MIN	HA-2420-2 TYP	HA-2420-2 MAX	HA-2425-5 MIN	HA-2425-5 TYP	HA-2425-5 MAX	UNITS
INPUT CHARACTERISTICS								
*Offset Voltage	+25°C		2	4		3	6	mV
	Full		3	6		4	8	mV
*Bias Current	+25°C		40	200		40	200	nA
	Full			400			400	nA
*Offset Current	+25°C		10	50		10	50	nA
	Full			100			100	nA
Input Resistance	+25°C	5	10		5	10		MΩ
Common Mode Range	Full	±10			±10			V
TRANSFER CHARACTERISTICS								
*Large Signal Voltage Gain (Note 1, 4)	Full	25K	50K		25K	50K		V/V
*Common Mode Rejection (Note 2)	Full	80	90		74	90		dB
Hold Mode Feedthrough Attenuation (Note 9)	Full		-76			-76		dB
Gain Bandwidth Product (Note 3)	+25°C		2.5			2.5		MHz
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 1)	Full	±10			±10			V
Output Current	+25°C	±15			±15			mA
Full Power Bandwidth (Note 3, 4)	+25°C		100			100		kHz
Output Resistance (D.C.)	+25°C		.15			.15		Ω
TRANSIENT RESPONSE								
Rise Time (Note 3, 5)	+25°C		50			50		ns
Overshoot (Note 3, 5)	+25°C		25			25		%
Slew Rate (Note 3, 6)	+25°C		7			7		V/μs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current (V_{IN} = 0V)	Full			0.8			0.8	mA
Digital Input Current (V_{IN} = +5.0V)	Full			20			20	μA
Digital Input Voltage (Low)	Full			0.8			0.8	V
Digital Input Voltage (High)	Full	2.0			2.0			V
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time to .1% 10V Step (Note 3)	+25°C		4			4		μs
Acquisition Time to .01% 10V Step (Note 3)	+25°C		5			5		μs
Aperture Time	+25°C		30			30		ns
Aperture Delay Time	+25°C		50			50		ns
Aperture Uncertainty Time	+25°C		5			5		ns
*Drift Current (Note 3, 8)	+25°C		5	50		5	50	pA
	Full		0.5	4.0		0.5	1.0	nA
*Charge Transfer (Note 8)	+25°C		5	10		5	10	pC
POWER SUPPLY CHARACTERISTICS								
*Supply Current (+)	+25°C		3.5	5.5		3.5	5.5	mA
*Supply Current (-)	+25°C		2.5	3.5		2.5	3.5	mA
*Power Supply Rejection	Full	80	90		74	90		dB

NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10VDC$
3. $A_V = +1$, $R_L = 2k\Omega$, $C_L = 50pF$
4. $V_{OUT} = 20V$ peak-to-peak
5. $V_{OUT} = 400mV$ peak-to-peak
6. $V_{OUT} = 10.0V$ peak-to-peak
7. Derate Power Dissipation by 4.3mW/°C above +105°C Ambient Temperature
8. $V_{IN} = 0V$
9. $f_{IN} \leq 100kHz$

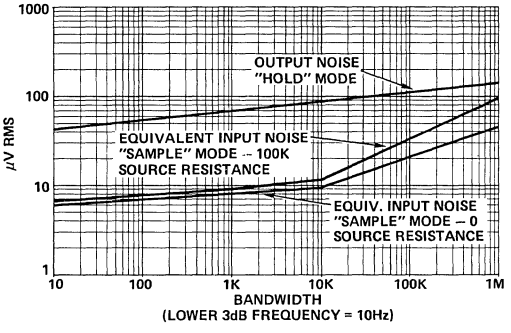
*100% Tested for DASH 8

V_{SUPPLY} = ±15VDC, T_A = +25°C, C_H = 1,000pF Unless Otherwise Specified

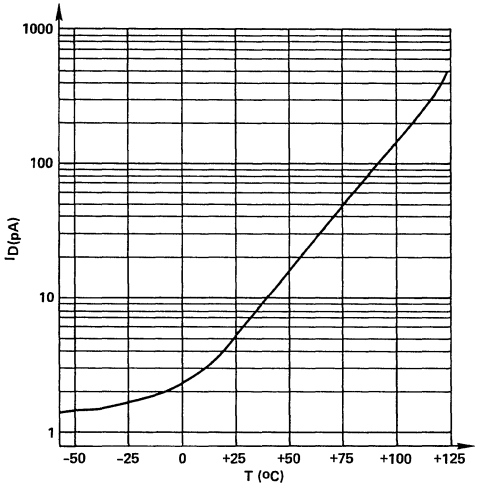
TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR



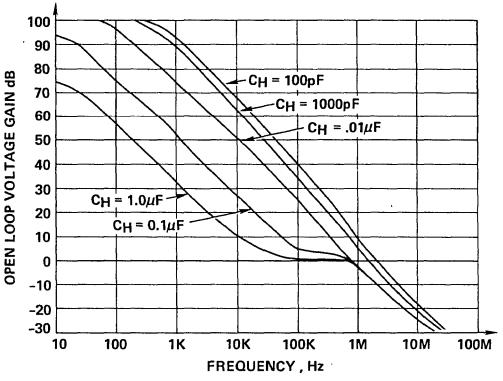
BROADBAND NOISE CHARACTERISTICS



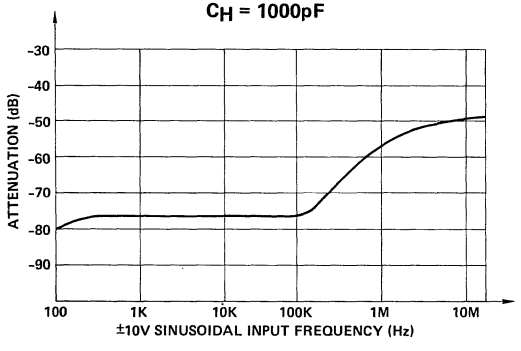
DRIFT CURRENT VS. TEMPERATURE



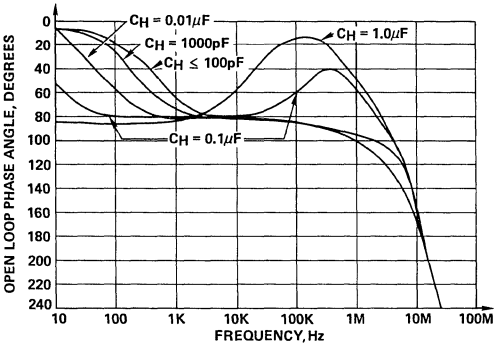
OPEN LOOP FREQUENCY RESPONSE



HOLD MODE FEED THROUGH ATTENUATION C_H = 1000pF



OPEN LOOP PHASE RESPONSE



5

PEDESTAL VS. INPUT VOLTAGE

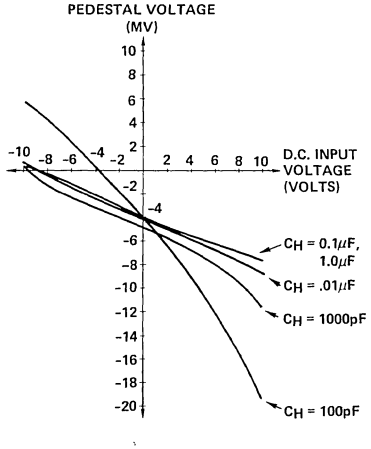


Figure 1

OFFSET ADJUSTMENT

The offset voltage of the HA-2420/2425 may be adjusted using a 100kΩ trim pot, as shown in Figure 6. The recommended adjustment procedure is:

1. Apply zero volts to the sample-and-hold input, and a square wave to the S/H control.
2. Adjust the trim pot for zero volts output in the hold mode.

This procedure will alter the input V_{OS} value so that it cancels the pedestal voltage.

GAIN ADJUSTMENT

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (C_H = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage ($V_{-10\ NOMINAL}$). Adjust the trim pot for an output hold voltage of

$$\frac{(V_{-10\ NOMINAL})+(-10V)}{2}$$

INVERTING CONFIGURATION

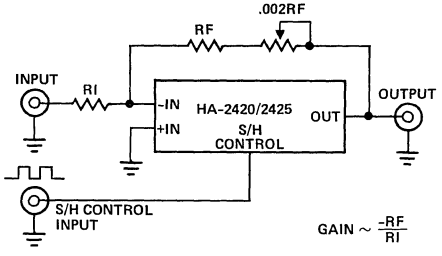


Figure 2

NONINVERTING CONFIGURATION

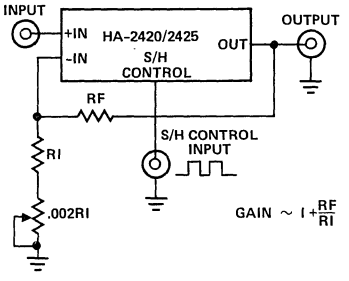


Figure 3

CHARGE TRANSFER AND DRIFT CURRENT

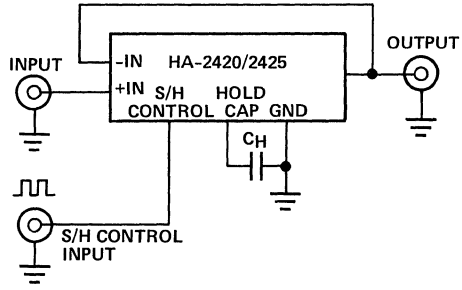
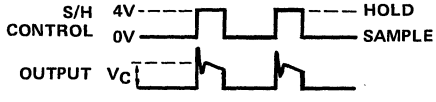


Figure 4

CHARGE TRANSFER TEST

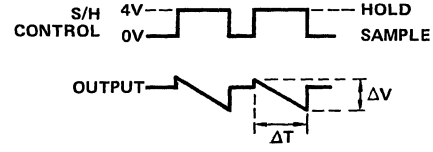
1. With a D.C. input voltage, observe the following waveforms:



2. Compute charge transfer from: $Q = V_C C_H$

DRIFT CURRENT TEST

1. With a D.C. input voltage, observe the following waveforms:



2. Measure the slope of the output during hold, $\Delta V/\Delta t$, and compute drift current from: $I_D = C_H \Delta V/\Delta t$

HOLD MODE FEEDTHROUGH ATTENUATION

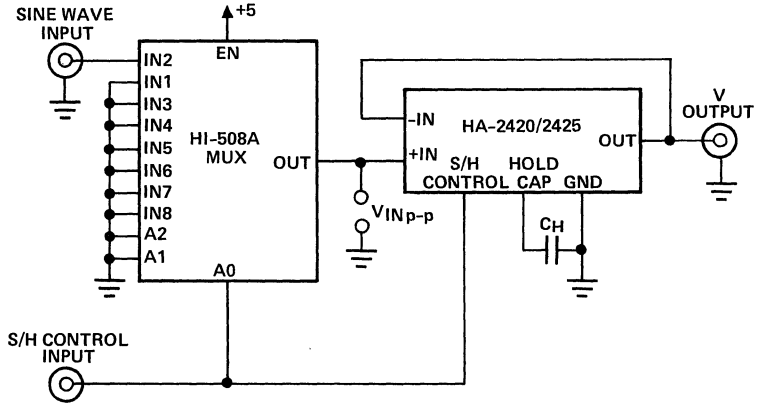


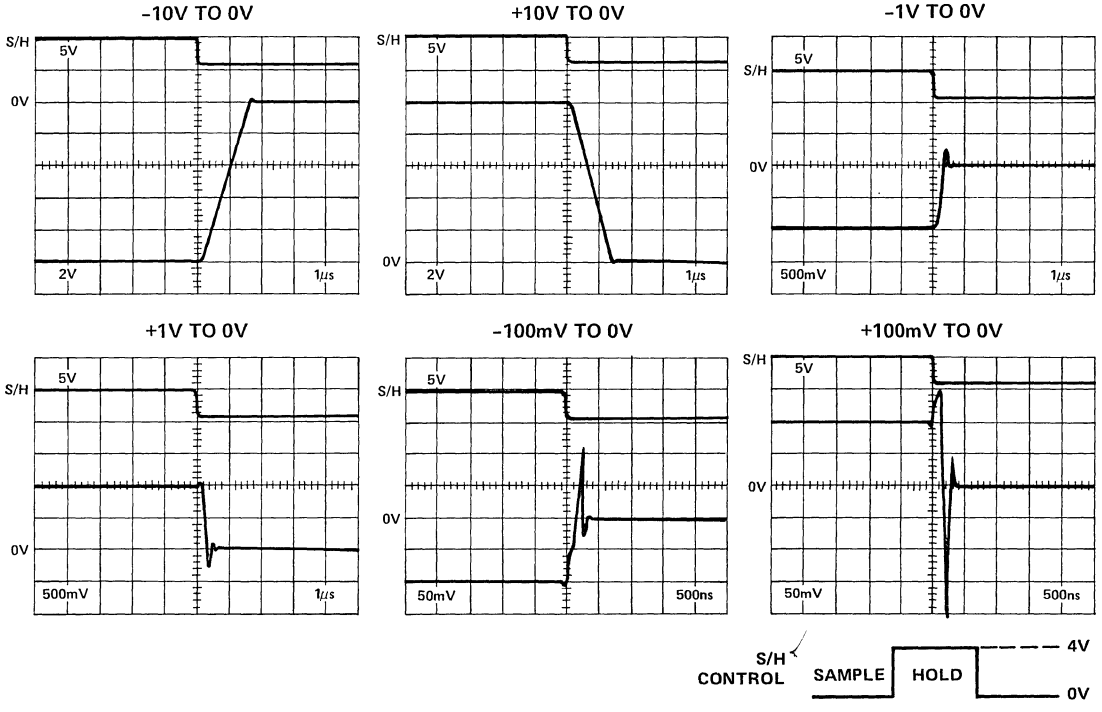
Figure 5

NOTE: Compute hold mode feedthrough attenuation from the formula:

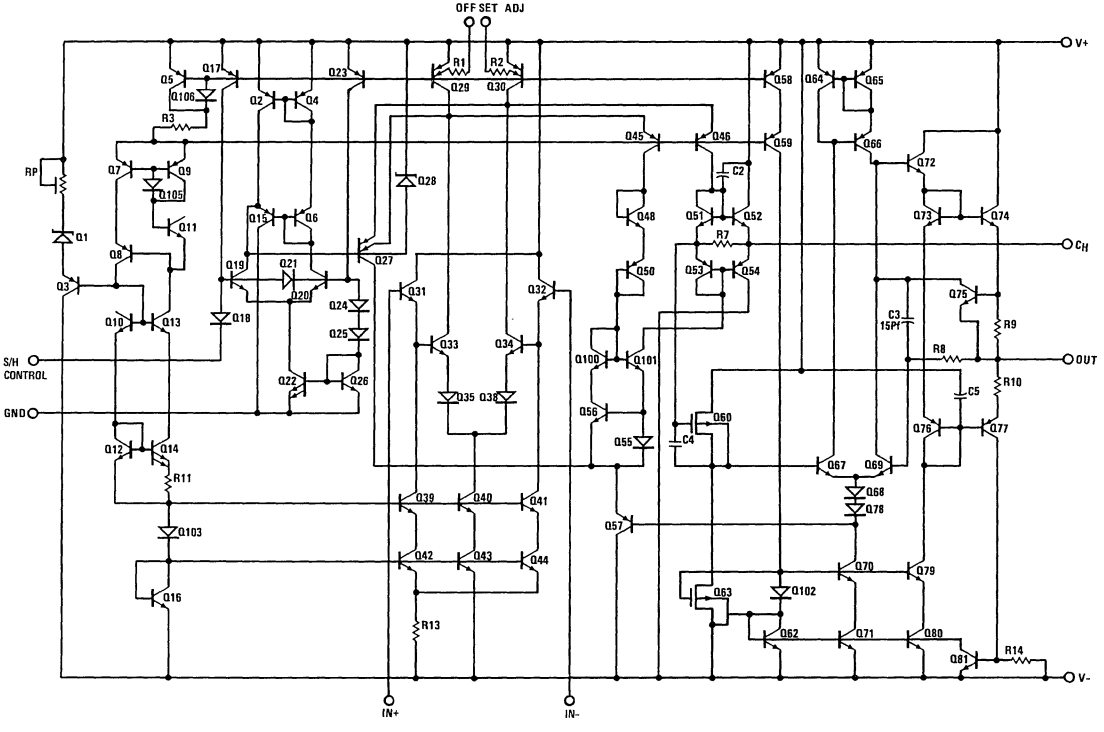
$$\text{Feedthrough Attenuation} = 20 \text{ Log } \frac{V_{OUT\ HOLD}}{V_{IN\ HOLD}}$$

Where $V_{OUT\ HOLD}$ = Peak-Peak value of output sinewave during the hold mode.

ACQUISITION TIMES (C_H = 1000pF)



SCHEMATIC



5

APPLICATIONS

BASIC SAMPLE-AND-HOLD
(TOP VIEW)

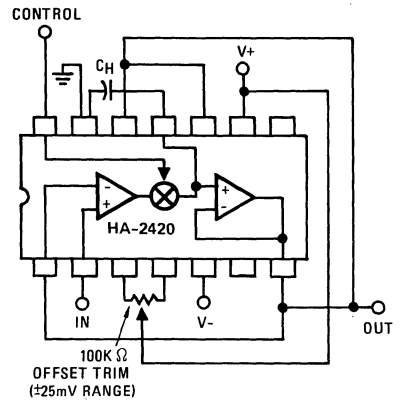


Figure 6

GUARD RING LAYOUT
(BOTTOM VIEW)

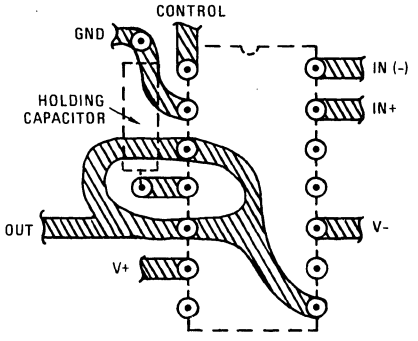


Figure 7

NOTES:

1. Figure 6 shows a typical unity gain circuit, with Offset Zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420/2425. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.

2. The method used to reduce leakage paths on the P.C. board and the device package is shown in Figure 7. This guard ring is recommended to minimize the drift during hold mode.

3. The holding capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), Teflon, or Parlene types are recommended.

For more applications, consult Harris Application Note 517, or factory applications group.

GLOSSARY OF TERMS

ACQUISITION TIME:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

CHARGE TRANSFER:

The small charge transferred to the hold capacitor from the inter-electrode capacitance of the switch, during the transition from Sample to Hold. Charge transfer contributes a portion (E) of the sample-to-hold offset (pedestal) error, according to:

$$E(V) = \frac{\text{Charge Transfer (pC)}}{\text{Hold Capacitance (pF)}}$$

Other mechanisms contribute additional pedestal error during the Sample to Hold transition.

APERTURE TIME:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

APERTURE DELAY:

The time interval between the sample-to-hold command (50% level) and the instant at which the switch is 10% open.

DRIFT CURRENT:

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D(pA) = C_H\,(pF) \times \frac{\Delta V}{\Delta T}\,(Volts/sec)$$

HARRIS

HD-0165

Keyboard Encoder

FEATURES

- STROBE OUTPUT
- KEY ROLLOVER OUTPUT
- EXPANDABLE: 2 PACKAGES REQUIRED FOR FULL TELETYPEWRITER, EIGHT-BIT ENCODING
- SINGLE +5.0V SUPPLY REQUIRED
- DTL/TTL OUTPUTS
- MONOLITHIC RELIABILITY

APPLICATIONS

- MICROPROCESSOR DATA ENTRY (16 KEY TO HEX CODE)
- BCD DATA ENTRY
- TYPEWRITER TYPE KEYBOARDS
- CONTROL PANELS

DESCRIPTION

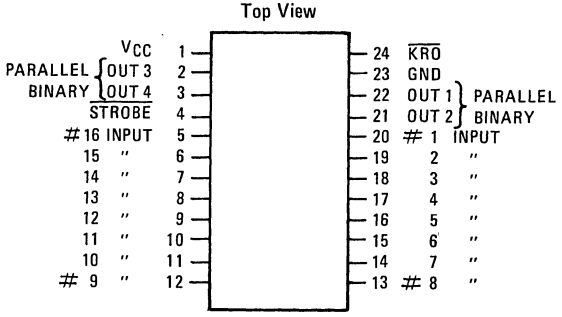
The HD-0165 Keyboard Encoder is a 16 line to four-bit parallel encoder intended for use with manual data entry devices such as calculator or typewriter keyboards. In addition to the encoding function, there is a Strobe output and a Key Rollover output which energizes whenever two or more inputs are energized simultaneously. Any four-bit code can be implemented by proper wiring of the input lines. Inputs are normally wired through the key switches to the +5.0V power supply. Full typewriter keyboard encoding up to eight bits can be accomplished with two Encoder circuits by the use of double pole key switches or single pole switches with two isolation diodes per key. Outputs will interface with all popular DTL and TTL logic families. The circuit is packaged in a hermetic 24-pin dual-in-line package and operates over the temperature range of 0°C to +75°C.

5

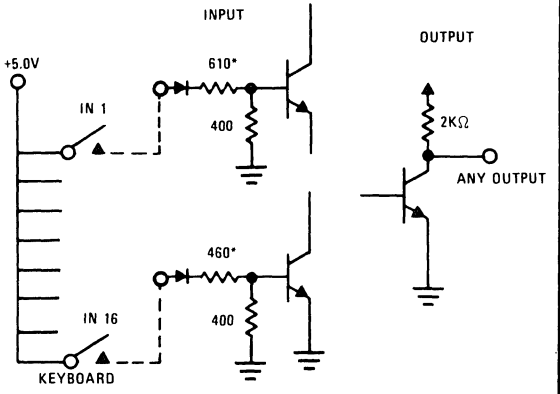
PINOUT

Section 11 for Packaging

Top View



EQUIVALENT CIRCUITS



* EQUIVALENT RESISTORS FOR OTHER INPUTS ARE BETWEEN THESE TWO VALUES

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V	Output Current	30mA
Input Voltage	+5.5V	Storage Temperature	-65^{0} to $+150^{0}$C
Output Voltage	+5.5V	Operating Temperature (Case)	0^{0}C to $+75^{0}$C

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5.0V ± 5%
T_{Case} = 0^{0}C to $+75^{0}$C
Unless otherwise specified

	PARAMETER	SYM.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
D.C.	Input Current "1"	I_{IH}			17	mA	V_{IN} = +5.0V
D.C.	Output Voltage "0"	V_{OL}		+0.2	+0.4	V	V_{IH} = +4.5V I_{OL} = 10mA
D.C.	Output Voltage "0"	V_{OL}			+0.4	V	V_{IH} = +3.5V I_{OL} = 3.2mA
D.C.	Output Voltage "1"	V_{OH}	+2.4	+4.0		V	V_{IL} = Open Circuit, I_{OH} = −240µA
D.C.	Power Supply Current Operating	I_{CC}			52	mA	One Input at +5.25V
D.C.	Power Supply Current Maximum	I_{CCM}			88	mA	All Inputs at +5.25V
A.C.	Skew Time (Note 1)	T_{SK}		80	200	ns	T_{Case} = 25^{0}C V_{CC} = V_{IN} = +5.0V C_L < 50pF

NOTE: (1) Skew time is the maximum time differential between propagation delay times of any outputs including strobe and K_{RO}.

TRUTH TABLE

INPUTS 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	OUTPUTS 1	2	3	4	$\overline{St.}$	$\overline{K_{RO}}$
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H
L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	H
L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H
L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H	L	H
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	H	L	H
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	H
L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	H	L	L	H
L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	H	L	L	H
L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	H	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	H	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
ANY TWO OR MORE HIGH																X	X	X	X	L	L

INPUTS: L = Open Circuit or < +1.0V H = > +4.5V Current Source
OUTPUTS: L = < +0.4V H = > +2.4V X = Erroneous Data

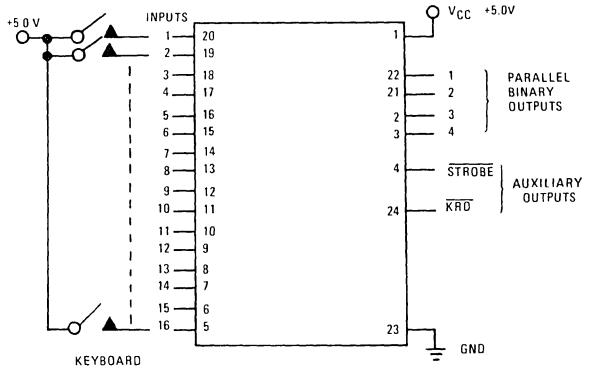


Figure 1. GENERAL CONFIGURATION FOR ENCODING TWO TO SIXTEEN KEYS

The Truth Table is used to determine wiring from the key switches to Encoder inputs to produce desired output codes.

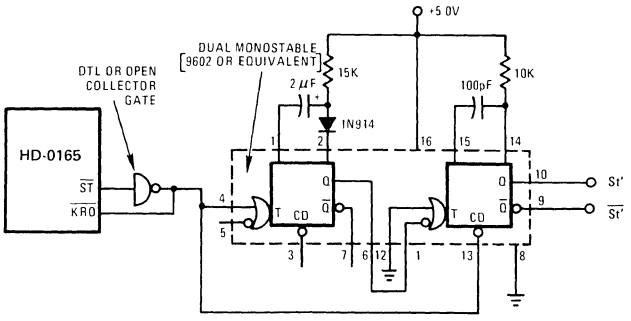


Figure 2. SWITCH BOUNCE ELIMINATION

This circuit generates a delayed Strobe pulse (ST'). Delay time is determined by first monostable and should be about 10ms. Pulse width is determined by second monostable and should be set according to system requirements. Effect of switch bounce or arcing on make or break is positively eliminated and proper encoding will take place under two key rollover conditions

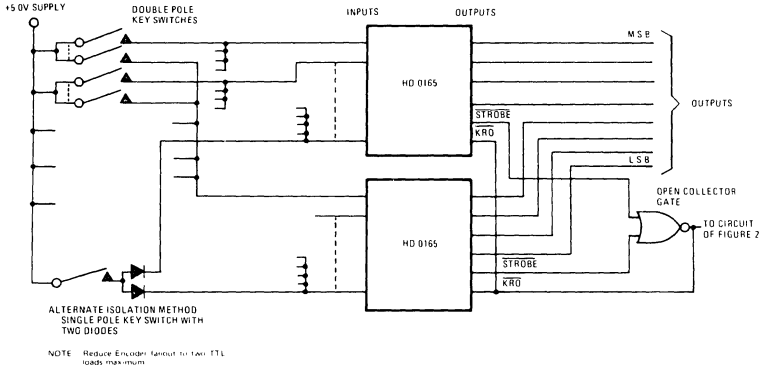


Figure 3. ENCODING UP TO 256 KEYS

Use upper Encoder to produce the four most significant output bits; the lower to produce the least significant bits. Use Truth Table and required output codes to determine wiring from each key to the two Encoders.

SHIFT and CONTROL functions can be implemented by logic gates in series with the output lines.

HARRIS

HI-562A

12 Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- OUTPUT CURRENT 2mA, F.S.
- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING 300ns TO 0.01% (TYP.)
- LOW GAIN DRIFT ±10ppm/°C (MAX.)
- EXCELLENT LINEARITY ±1/2 LSB (MAX.)
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE
- NOTE: HI-562A IS RECOMMENDED FOR NEW DESIGNS

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH-REL APPLICATIONS
- PRECISION INSTRUMENTS

DESCRIPTION

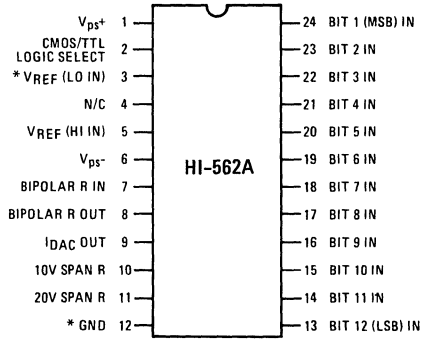
The Harris HI-562A is the first monolithic digital-to-analog converter to combine both ultra-high speed performance and 12-bit accuracy on the same chip. The HI-562A's fast output current settling of 300ns to 0.01% is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-562A by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-ON and turn-OFF switching times. This creates within the chip a very uniform constant thermal distribution for excellent linearity and also completely eliminates thermal transients during switching. High stability thin film resistor processing together with laser trimming provide the HI-562A with guaranteed true 12-bit linearity to within ±1/2 LSB maximum at +25°C for -4 and -5 parts, and to within ±1/4 LSB maximum at +25°C for -2 and -8 parts. The HI-562A is recommended as a replacement for higher cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data acquisition systems requiring throughput rates as a high as 3.3 MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-562A is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-562A-5 is specified for operation over 0°C to +75°C, the HI-562A-4 over -25°C to +85°C and the HI-562A-2 and HI-562A-8 over -55°C to +125°C. Processing MIL-STD-883A Class B screening is available by selecting the HI-562A-8. All are available in a hermetically sealed 24-lead dual-in-line package.

PINOUT

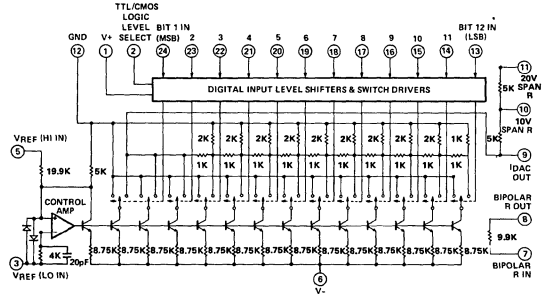
Section 11 for Packaging

TOP VIEW



*Pin 3 connected to bottom case for high frequency shielding.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	V_{ps+}	+20V
	V_{ps-}	-20V
Reference Inputs	VREF (Hi)	$\pm V_{ps}$
Digital Inputs	Bits 1-12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	$\pm V_{ps}$
	Pin 9	$+V_{ps}$, -5V

Power Dissipation P_d, Package	1000mW
Operating Temperature Range	
HI-562A-2	-55°C to +125°C
HI-562A-4	-25°C to +85°C
HI-562A-5	0°C to +75°C
HI-562A-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, V_{ps+} = +5V, V_{ps-} = -15V, V_{REF} = +10V, pin 2 tied to pin 12 unless otherwise noted)

PARAMETER	CONDITIONS	HI-562A-2/HI-562A-8 MIN	HI-562A-2/HI-562A-8 TYP	HI-562A-2/HI-562A-8 MAX	HI-562A-4/HI-562A-5 MIN	HI-562A-4/HI-562A-5 TYP	HI-562A-4/HI-562A-5 MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (3)	Bit ON "Logic 1" Bit OFF "Logic 0"							
TTL Input Voltage (2) Logic "1"	Over full temp. range Pin 2 tied to Pin 12	2.0			2.0			V
TTL Logic "0"				0.8			0.8	V
TTL Input Current (2) Logic "1"			20	100		20	100	nA
TTL Logic "0"			-50	-100		-50	-100	μA
CMOS Input Voltage Logic "1"	Connect pin 2 to pin 1 for $V_{ps+} \geq$ 9.5V. Otherwise (for CMOS levels below 8V), connect pin 2 to pin 12.	$0.7V_{ps+}$			$0.7V_{ps+}$			V
CMOS Logic "0"				$0.3V_{ps+}$			$0.3V_{ps+}$	V
CMOS Input Current Logic "1"			20	100		20	100	nA
CMOS Logic "0"			-50	-100		-50	-100	μA
Reference Input								
Input Resistance			20K			20K		Ω
Input Voltage			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Over full temp. range			12			12	Bits
Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range		±1/2	±1			±1	
Differential Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range			MONOTONICITY GUARANTEED				
Relative Accuracy (6)	With 50 Ω(1%) Trim Resistors							
Gain Error	All Bits ON		±.024	±0.25		±.024	±0.25	
Bipolar Offset Error	All Bits OFF		±.024	±0.25		±.024	±0.25	% FSR (4)
Unipolar Offset Error			±.012	±0.05		±.012	±0.05	
Adjustment Range	See Operating Instructions							
Gain	With 100 ΩTrim		±0.25			±0.25		% FSR
Bipolar Offset	Potentiometers		±0.5			±0.5		
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (3)	Over full		±6	±10			±10	ppm of
Offset Drift (3)	temp. range							FSR/°C
Unipolar Offset	All Bits OFF			±2			±2	
Bipolar Offset				±4			±4	
Differential Nonlinearity	Over full temp. range		±1	±2		±2	±2	
Settling Time (3) to ±1/2 LSB	All Bits ON-to-OFF or OFF-to-ON		300	400		300	400	ns

5

PARAMETER	CONDITIONS	HI-562A-2/HI-562A-8 MIN	HI-562A-2/HI-562A-8 TYP	HI-562A-2/HI-562A-8 MAX	HI-562A-4/HI-562A-5 MIN	HI-562A-4/HI-562A-5 TYP	HI-562A-4/HI-562A-5 MAX	UNITS
Major Carry Transient								
Peak Amplitude	From 011...1 to 100...0		0.7			0.7		mA
Settling Time to	or 100...0 to 011...1							
90% Complete			35			35		ns
Power Supply Sensitivity (3)								
Unipolar Offset	All Bits OFF							ppm of FSR/% V_{ps}
V_{ps}+ @ +5V			±0.5			±0.5		
V_{ps}- @ -15V			±0.5			±0.5		
Bipolar Offset	All Bits OFF, Bipolar mode							
V_{ps}+ @ 5V			±1.5			±1.5		
V_{ps}- @ -15V			±1.5			±1.5		
Gain	All Bits ON							
V_{ps}+ @ +5V				±3.5			±3.5	
V_{ps}- @ -15V				±7.5			±7.5	

OUTPUT CHARACTERISTICS

Output Current								
Unipolar			-2.0			-2.0		mA
Bipolar			±1.0			±1.0		
Resistance			2K			2K		ohms
Capacitance			20			20		pF
Output Voltage Ranges								
Unipolar	Using external op amp		0 to +5			0 to +5		
	and internal scaling		0 to +10			0 to +10		
Bipolar	resistors. See Figure 1		±2.5			±2.5		V
	and Table 1 for connections		±5			±5		
			±10			±10		
Compliance Limit (3)		-3		+10	-3		+10	V
Compliance Voltage (3)	Over full temp. range		±1.0			±1.0		V
Output Noise	0.1 to 10Hz (All Bits ON)		30			30		µV (p-p)
	0.1 to 5MHz (All Bits ON)		100			100		

POWER REQUIREMENTS

V_{ps}+ (7)	Over full	4.5	5	16.5	4.75	5	16.5	V
V_{ps}-	temp. range	-13.5	-15	-16.5	-13.5	-15	-16.5	
I_{ps}+ (5)	All Bits ON or OFF in		8	15		8	15	mA
I_{ps}- (5)	either TTL or CMOS mode (25°C)		16	23		16	23	
I_{ps}+ (5)	Same as above except		11	20		11	20	mA
I_{ps}- (5)	over full temp. range		20	30		20	30	
Power Dissipation	+25°C		280	420				mW
	V_{ps}+ = +5V							
	V_{ps}- = -15V							

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

2. $V_{ps}+$ tolerance is ±10% for HI-562A-2, -8. and ±5% for HI-562A-4,-5.

3. See Definitions.

4. FSR is "full scale range" = 20V for ± 10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.

5. After 30 seconds warm-up.

6. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Operating Instructions Figure 2.)

7. The HI-562A is designed for $V_{ps}+ = 5V$, but $+4.5V \leq V_{ps}+ \leq +16V$ may be connected if convenient. (For $V_{ps}+$ above +5V, there is an increase in power dissipation but little change in performance.)

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-562A accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement, or Offset Binary, (See Operating Instructions).

	ANALOG OUTPUT		
DIGITAL INPUT	Straight Binary	Offset Binary	Two's Complement*
MSB LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	Zero –1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB
*Invert MSB with external inverter to obtain Two's Complement Coding			

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonictiy; i.e., the output always increases and never decreases for an increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the converter resulting from a change in the -15V or +5V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-562A **(preferably** to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

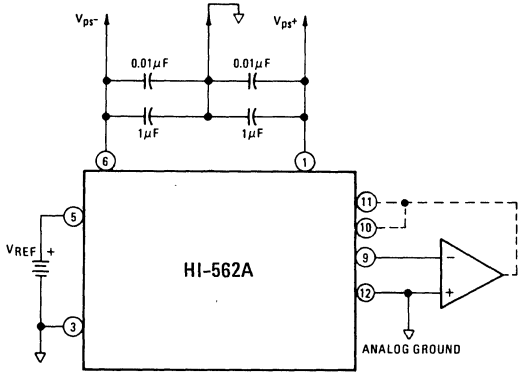
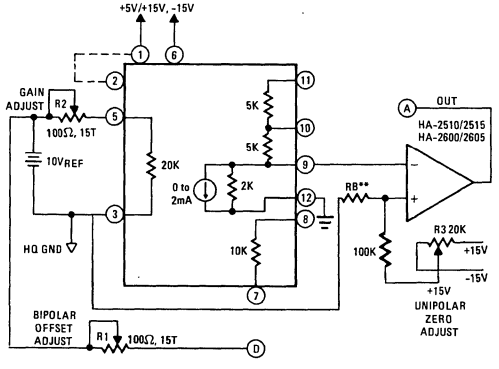


Figure 1

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

CONNECTIONS – Using an external resistive load, the output **voltage should not** exceed ±1V to maintain specified accuracy. For higher output voltages, accuracy can be maintained by using an external op amp and the internal span resistors as shown in Figure 2 and defined in Table 1 for unipolar and bipolar modes.



* For TTL and DTL compatibility, connect +5V to pin 1 and tie pin 2 to pin 12. For CMOS compatibility, connect digital power supply ($+4.85V \leq V_{DD} \leq +12V$) to pin 1 and short pin 2 to pin 1.

** Bias resistor, RB, should be chosen to equalize op amp offset voltage due to bias current. Its value is calculated from the parallel combination of the current source output resistance (2K) and the op amp feedback resistor. See Table 1 for values of RB.

Figure 2

Table 1

	OUTPUT RANGE	CONNECTIONS Pin 7 to	Pin 8 to	Pin 10 to	Pin 11 to	BIAS (R_B) RESISTOR
Unipolar Mode	0 to +10V	N.C.	N.C.	A	N.C.	1.43K
	0 to +5V	N.C.	N.C.	A	9	1.11K
Bipolar Mode	±10V	D	9	N.C.	A	1.43K
	±5V	D	9	A	N.C.	1.25K
	±2.5V	D	9	A	9	1.0K

EXTERNAL GAIN AND ZERO CALIBRATION (See Figure 2)

The input reference resistor (20K nominal) and bipolar offset resistors shown in Figure 2 are both intentionally set low by 50 Ω to all the user to externally trim-out initial errors to a very high degree of precision. The adjustments are made in the voltage output mode using an external op amp as current-to-voltage converter and the HI-562A internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. For best accuracy over temperature, select an op amp that has good front-end temperature coefficients such as the HA-2600/2605 with offset voltage and offset current tempco's of 5 μ V/°C in 1nA/°C, respectively. For high speed voltage mode applications where fast settling is required, the HA-2510/2515 is recommended for better than 1.5 μs settling to 0.01%. Using either one, potentiometer R_3 conveniently nulls unipolar offset plus op amp offset in one operation (for HA-2510/2515 and HA-2600/2605 use R_3 = 20K and 100K, respectively). For bipolar mode operation, R_3 should be used to null op amp offset to optimize its tempco (i.e., short 9 to A and adjust R_3 for zero before calibrating in bipolar mode). The gain and bipolar offset adjustment range using 100Ω potentiometers is ±12LSB and ±25 LSB respectivelv. If desired, the potentiometers can be replaced with fixed 50Ω(1%) resistors resulting in an initial gain and bipolar offset accuracy of typically ±1/2LSB.

UNIPOLAR CALIBRATION

Step 1: Unipolar Offset
- Turn all bits OFF
- Adjust R3 for zero volts output

Step 2: Gain
- Turn all bits ON
- Adjust R2 for an output of FS -1 LSB
  That is, adjust for:
  9.9976V for 0V to +10V range
  4.9988V for 0V to +5V range

BIPOLAR CALIBRATION

Step 1: Bipolar Offset
- Turn all bits OFF
- Adjust R1 for an output of:
  -10V for ±10V range
  -5V for ±5V range
  -2.5V for ±2.5V range

Step 2: Gain
- Turn bit 1 (MSB) ON; all other bits OFF
- Adjust R2 for zero volts output

HARRIS

HI-5610

10 Bit High Speed Monolithic Digital-to-Analog Converter

Preliminary

FEATURES

- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING. . . . . 85ns TO ½LSB TYP.
- LOW GAIN DRIFT. . . . . ±5ppm/°C TYP.
- EXCELLENT LINEARITY OVER TEMPERATURE . . . . . ± ½LSB MAX.
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH RELIABILITY APPLICATIONS
- PRECISION INSTRUMENTS

DESCRIPTION

The HI-5610 is an ultra-high speed 10 bit monolithic current output digital-to-analog converter. The fast output current settling of 85ns to ½LSB of its final value is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-5610 by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-on and turn-off switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also eliminates thermal transients during switching. High stability thin film resistor processing, together with laser trimming provide the HI-5610 with true 10 bit linearity to within ± ½LSB maximum over operating temperature range. The HI-5610's low offset and gain drift over the operating temperature range assures that its absolute accuracy when referred to a fixed 10V reference will not deviate more than ±1LSB for both unipolar and bipolar operation.

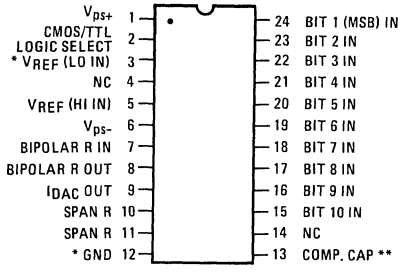
The HI-5610 is recommended as a replacement for high cost hybrid and modular units for increased reliability and accuracy in applications such as CRT Displays, precision instruments and data acquisition system requiring through-put rates as high as 12mHz for full range transitions. Its small size makes it an ideal choice as the essential part of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-5610 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-5610-5 is specified for operation over 0°C to +75°C, the HI-5610-2 and HI-5610-8 over -55°C to +125°C. Processing to MIL-STD-883A class B screening is available by selecting the HI-5610-8. All are available in a hermetically sealed 24 lead dual-in-line package.

PINOUT

Section 11 for Packaging

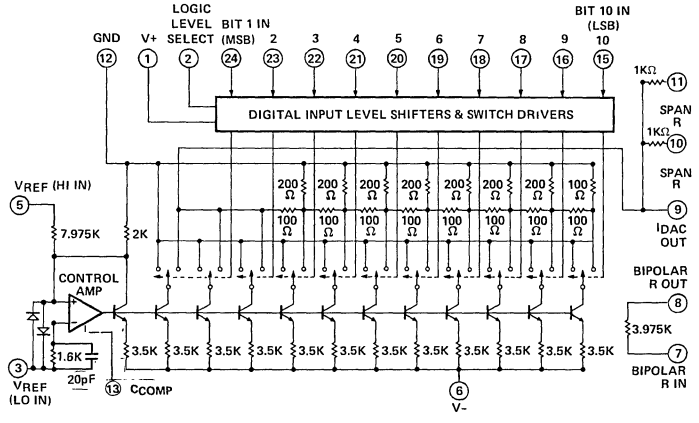
TOP VIEW



* Pin 3 connected to bottom case for high frequency shielding.

** For high speed operation, connect 0.01 µF between Pin 13 and GND. Otherwise, leave Pin 13 open.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{ps}+$	+20V
	$V_{ps}-$	-20V
Reference Inputs	VREF (Hi)	$\pm V_{ps}$
	VREF(Lo)	0V
Digital Inputs	Bits 1 - 12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	$\pm V_{ps}$
	Pin 9	$+V_{ps}$, -5V

Power Dissipation Pd, Package	1000mW
Operating Temperature Range	
HI-5610-2	-55°C to +125°C
HI-5610-5	0°C to +75°C
HI-5610-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{ps}+$, = +5V, $V_{ps}-$ = -15V, V_{REF} = +10V, pin 2 ground unless otherwise noted)

		HI-5610-2 HI-5610-8			HI-5610-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (2)								
TTL Logic Input Voltage (3)								
Logic "1"	Full	2.0			2.0			V
Logic "0"	Full			0.8			0.8	V
Input Current								
Logic "1"	Full		20	100		20	100	nA
Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4)								
Logic "1"	Full	$0.7V_{ps}+$			$0.7V_{ps}+$			V
Logic "0"	Full			$0.3V_{ps}+$			$0.3V_{ps}+$	V
Input Current								
Logic "1"	Full		20	100		20	100	nA
Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input								
Input Resistance			8K			8K		Ω
Input Voltage (I_{OUT} = 5mA + 20%)			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Full			10			10	Bits
Nonlinearity (5)	25°C			±½			±½	LSB
Differential Nonlinearity (5)	25°C			±½			±½	LSB
Relative Accuracy (6)								
Gain Error								(9)
(Input Code 11....1)			±0.05			±0.05		% FSR
Unipolar Offset Error								
(Input Code 00....0)			±0.05			±0.05		% FSR
Bipolar Offset Error								
(Input Code 00....0)			±0.05			±0.05		% FSR
(Adjustable to zero, see Figure 4, 5)								
Adjustment Range								
Gain			±0.25			±0.25		% FSR
Bipolar Offset			±0.25			±0.25		% FSR
Temperature Stability								
Gain Drift	Full		±5			±5		ppm/°C
Unipolar Offset Drift	Full		±3			±3		ppm/°C
Bipolar Offset Drift	Full		±3			±3		ppm/°C
Differential Nonlinearity	Full		±2			±2		ppm/°C
MONOTONICITY - GUARANTEED OVER FULL OPERATING TEMPERATURE RANGE								
Settling Time to ½LSB (5)								
From all 0's to all 1's						85		ns
From all 1's to all 0's						85		ns
Major Carry Switching to 90% Complete			40			40		ns

PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Power Supply Sensitivity (5)								
$V_{ps}+$ = +5V, $V_{ps}-$ = -13.5V to -16.5V								
Gain								
(Input Code 11....1)				±2			±2	
Unipolar Offset								
(Input Code 00....0)			±0.5			±0.5		
Bipolar Offset								ppm of
(Input Code 00....0)			±1.5			±1.5		FSR/%V_{ps}
$V_{ps}-$ = -15V, $V_{ps}+$ = 4.5V to 5.5V								
Gain								
(Input Code 11....1)				±1			±1	
Unipolar Offset								
(Input Code 00....0)			±0.5			±0.5		
Bipolar Offset								
(Input Code 00....0)			±1.5			±1.5		
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar			-5.0			-5.0		mA
Bipolar			±2.5			±2.5		mA
Output Resistance			200			200		Ω
Output Capacitance			20			20		pF
Output Voltage Range (7)								
Unipolar			+5			+5		V
			+2.5			+2.5		V
Bipolar			±2.5			±2.5		V
			±1.25			±1.25		V
Output Compliance Limit (5)		-3		+10	-3		+10	V
Output Compliance Voltage (5)	Full		±1.5			±1.5		V
Output Noise Voltage (8)								
0.1Hz to 100Hz			10			10		μVp-p
0.1Hz to 1MHz			100			100		μVp-p
POWER REQUIREMENTS								
$V_{ps}+$ (4)	Full	4.5	5	16.5	4.75	5	16.5	V
$V_{ps}-$	Full	-13.5	-15	-16.5	-13.5	-15	-16.5	V
$I_{ps}+$ (All 1's or all 0's in	25°C		9			9		mA
(10) either TTL or CMOS Mode)	Full		20			20		mA
$I_{ps}-$ (Same as above)	25°C		25			25		mA
(10)	Full		30			30		mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5610 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions).
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The $V_{ps}+$ tolerance is ±10% for HI-5610-2,-8. And ±5% for HI-5610-5.
4. For CMOS compatibility based on $V_{ps}+ \geq +8V$, (switching thresholds equal $V_{ps}+/2$), connect pins 1 and 2. For CMOS levels below +8V, connect pin 2 to ground only (this provides a threshold of approximately +1.4V).
5. See definitions.
6. Using an external op amp with internal span resistors and 24.9Ω ±1% external trim resistors in place of potentiometers R1 and R2. These errors are adjustable to zero using R1 and R2. (See operating instructions.)
7. Using an external op amp and internal span resistors. (See operating instructions for connections.)
8. Specified for digital input in all '1's or all '0's.
9. FSR is "Full Scale Range" and is 5V for ±2.5V range, 2.5V for ±1.25V range, etc., or 5mA (±20%) for current output.
10. After 30 seconds warm-up.

DEFINITIONS OF SPECIFICATIONS

ACCURACY

NONLINEARITY - Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY - For a D/A converter, it is the difference between the actual output voltage change and the ideal (1LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ± 1LSB or less guarantees monotonicitiy; i.e., the output always increases and never decreases for and increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition (01.....1 to 10.....0 or vice versa)

DRIFT

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C - T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011.....1 to 100.....0 or vice versa. For example, if turn ON is greater than turn OFF for 011.....1 to 100.....0, an intermediate state of 000.....0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

OPERATING INSTRUCTIONS

DECOUPLING AND GROUNDING

For best accuracy and high speed performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5610 (preferrably to the device pin) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

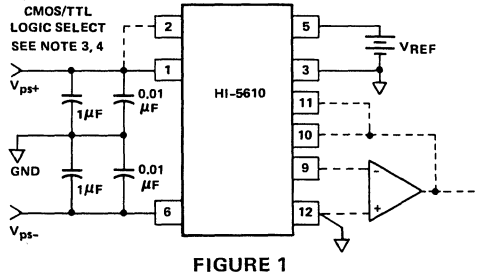


FIGURE 1

HIGH PERCISION PERFORMANCE

The output accuracy of the HI-5610 depends mainly on the accuracy of the voltage applied to the VREF input of HI-5610 and it can be described roughly as VREF/8KΩ = ¼ full scale output current. This means the output of HI-5610 will change whenever VREF varies. For high precision performance a precision +10V voltage reference with reasonably low temperature coefficient such as HA-1600 is highly recommended. For voltage output operation use an external op amp as current-to-voltage converter and the HI-5610 internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. The selected op amp should have a good front-end temperature coefficient such as HA-2600/2605 with offset voltage and offset current tempco's of 5 μV/°C and 1nA/°C, respectively. The input reference resistor (7.975K Ω) and bipolar offset resistor (3.975K Ω) are both intentionally set low by 25 Ω to allow the user to externally trim-out initial errors to a very high degree of precision. For high speed voltage output applications where fast settling is required, the HA-2510/2515 is recommended for better than 1 μs settling to ½LSB.

UNIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for unipolar +5V and +2.5V voltage output using an external op amp and the internal span resistors are shown in Figure 2 and Figure 3, respectively.

CALIBRATION - UNIPOLAR

Step 1 Offset
- Turn all bits off (all 0's)
- Adjust R3 for zero volts output

Step 2 Gain
- Turn all bits on (all 1's)
- Adjust R1 for an output of FS-1LSB
  That is, adjust for:
  4.99512V for 0V to +5V range
  2.49756V for 0V to +2.5V range

UNIPOLAR - STRAIGHT BINARY
0V TO +5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1LSB	= 4.99512V
10 0	½FS	= 2.50000V
01 1	½FS -1LSB	= 2.49512V
00 0	Zero	= 0.00000V

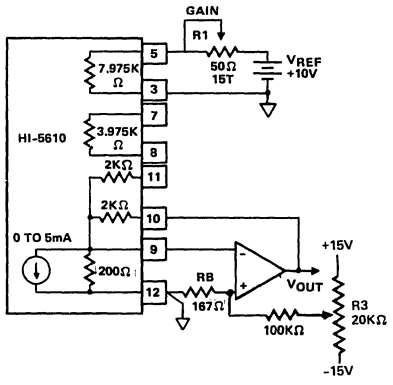


FIGURE 2

UNIPOLAR - STRAIGHT BINARY
0V TO +2.5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1LSB	= 2.49756V
10 0	½FS	= 1.25000V
01 1	½FS -1LSB	= 1.24756V
00 0	Zero	= 0.00000V

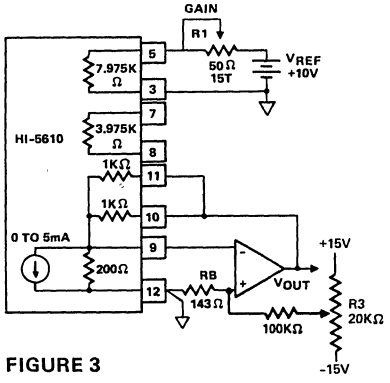


FIGURE 3

BIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for Bipolar ± 2.5V and ± 1.25V voltage output using an external op amp and the internal span resistors are shown in Figure 4 and Figure 5, respectively.

CALIBRATION - BIPOLAR

Step 1 Op Amp Null
- Short op amp output to op amp -input
- Adjust R3 for zero volts output

Step 2 Gain
- Turn all bits on (all 1's) record output voltage
- Turn all bits off (all 0's) record output voltage
- Adjust R1 till the difference between the readings is equal to:
  4.99512V for ± 2.5V range
  2.49756V for ±1.25V range.

Step 3 Offset
- Turn bit 1 (MSB) on, all other bits off (10....0)
- Adjust R2 for zero volts output

BIPOLAR - OFFSET BINARY
±2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS - 1 LSB	= +2.49512V
10 0	ZERO	= +0.00000V
01 1	Zero - 1 LSB	= -0.00488V
00 0	-FS	= -2.50000V

BIPOLAR TWO'S COMPLEMENT **
±2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1LSB	= +2.49512V
00 0	Zero	= +0.00000V
11 1	Zero - 1LSB	= -0.00488V
10 0	-FS	= -2.50000V

** Invert MSB with external inverter
to obtain two's complement coding.

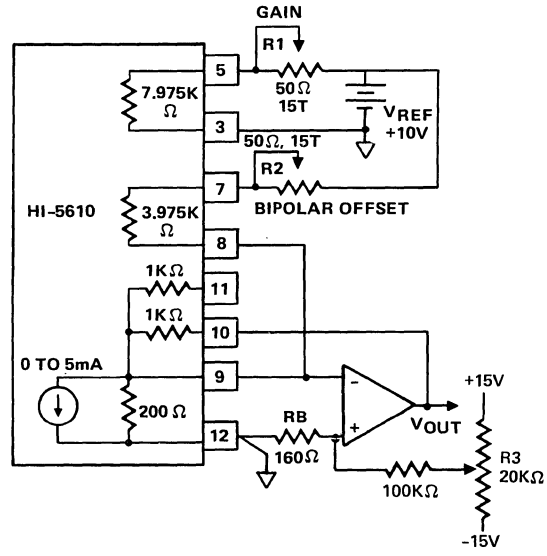


FIGURE 4

BIPOLAR - OFFSET BINARY
±1.25V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS - 1LSB	= +1.24756V
10 0	Zero	= +0.00000V
01 1	Zero - 1LSB	= -0.00244V
00 0	-FS	= -1.25000V

BIPOLAR - TWO'S COMPLEMENT **
±1.25V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1LSB	= +1.24756V
00 0	Zero	= +0.00000V
11 1	Zero - 1LSB	= -0.00244V
10	-FS	= -1.25000V

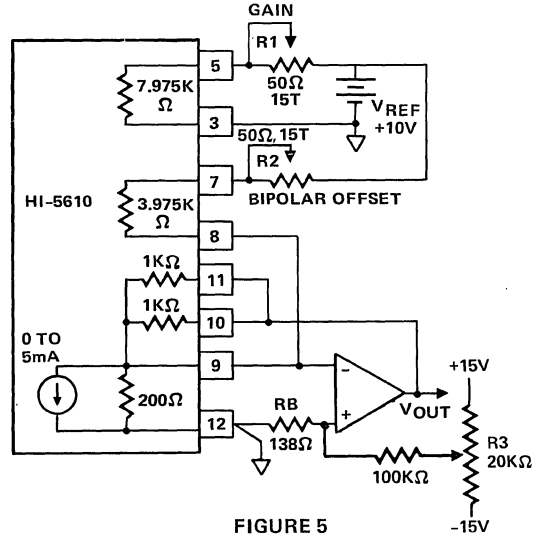


FIGURE 5

HARRIS

HI-5618A/5618B

8 Bit High Speed Digital-to-Analog Converters

FEATURES

- VERY FAST SETTLING CURRENT OUTPUT 65ns
- MINIMUM NONLINEARITY ERROR
  - HI-5618A ±1/4 LSB MAX
  - HI-5618B ±1/2 LSB MAX
- LOW POWER OPERATION 340mW TYP
- ON-CHIP RESISTORS FOR GAIN AND BIPOLAR OFFSET
- GUARANTEED MONOTONIC OVER TEMPERATURE
- CMOS, TTL, OR DTL COMPATIBLE

APPLICATIONS

- HIGH SPEED PROCESS CONTROL
- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERSION
- WAVEFORM SYNTHESIS
- HIGH RELIABILITY APPLICATIONS
- VIDEO SIGNAL RECONSTRUCTION

DESCRIPTION

The HI-5618A/B are very high speed 8 bit current output D/A converters. These monolithic devices are fabricated with dielectrically isolated bipolar processing, which reduces internal parasitic capacitance to allow fast rise and fall times. This achieves a typical full scale settling time of 65ns to ±1/2 LSB. Output glitches are minimized by incorporation of equally weighted current sources, switched to either an R-2R ladder network or ground for symmetrical turn ON and turn OFF times. High stability thin film resistors provide excellent accuracy without trimming. For example, the HI-5618A has ±1/4 LSB maximum nonlinearity error at +25°C, with ±3/8 LSB guaranteed over the full operating temperature range.

The HI-5618A/B are recommended for any application requiring high speed and accurate conversions. They can be used in CRT displays and systems requiring throughput rates as high as 20MHz for full scale transitions. Other applications include high speed process control, defense systems, avionics, and space instrumentation.

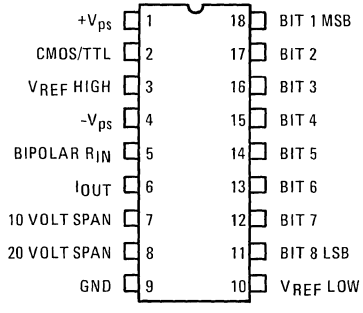
The HI-5618A-5 and HI-5618B-5 are specified for operation from 0°C to +75°C. The "-2" versions are specified from -55°C to +125°C. "Dash 8" (-8) designates parts which have been screened per MIL-STD-883, Method 5004/Class B.

Power requirements are +5V and -15V. Package is an 18 pin DIP, in plastic or ceramic.

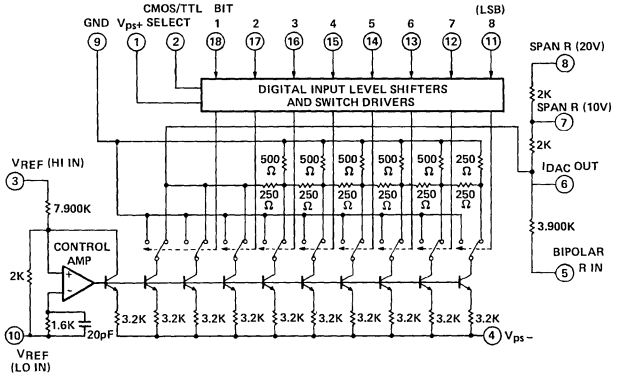
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Referred to Ground) (1)

Power Supply Inputs	$V_{PS}+$	+20V
	$V_{PS}-$	-20V
Reference Inputs	V_{REF} (Hi)	$\pm V_{PS}$
	V_{REF} (Lo)	0V
Digital Inputs	Bits 1 - 8	-1V, +12V
CMOS/TTL Logic Select		-1V, +12V
Outputs	Pins 5, 7, 8	$\pm V_{PS}$
	Pin 6	$+V_{PS}$, -2.5V

Power Dissipation Pd, Package	700mW
Operating Temperature Range	
HI-5618A/B-2	-55°C to +125°C
HI-5618A/B-5	0°C to +75°C
HI-5618A/B-8	-55°C to +125°C
Storage Temperature Range	-65°C to 150°C

ELECTRICAL CHARACTERISTICS ($V_{PS}+ = +5V$; $V_{PS}- = -15V$; $V_{REF} = +10V$; Pin 2 to GND, unless otherwise noted)

PARAMETER		TEMP	HI-5618A/B-2 HI-5618A/B-8 MIN	TYP	MAX	HI-5618A/B-5 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS									
Digital Inputs (2)									
TTL Logic Input Current (3)	Logic "1"	Full	2.0			2.0			V
	Logic "0"	Full			0.8			0.8	V
Input Current	Logic "1"	Full		20	100		20	100	nA
	Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4)	Logic "1"	Full	$0.7V_{PS}+$			$0.7V_{PS}+$			V
	Logic "0"	Full			$0.3V_{PS}+$			$0.3V_{PS}+$	V
CMOS Logic Input Current	Logic "1"	Full		20	100		20	100	nA
	Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input									
Input Resistance		+25°C		8k			8k		Ω
Input Voltage (I_{OUT} = 5mA ± 20%)		+25°C		+10			+10		V
TRANSFER CHARACTERISTICS									
Resolution		Full		8			8		Bits
Nonlinearity, Integral and Differential	HI-6518A	25°C			±1/4			±1/4	LSB
		Full			±3/8			±3/8	LSB
	HI-5618B	25°C			±1/2			±1/2	LSB
		Full			±5/8			±5/8	LSB
Initial Accuracy (6) (Relative to External +10V Reference)									
Gain		25°C			±2			±2	LSB
Unipolar Zero		25°C			±1/8			±1/8	LSB
Bipolar Offset (Neg. Full Scale)		25°C			±2			±2	LSB
Temperature Stability									
Gain Drift		Full			±1/4			±1/4	LSB
Unipolar Zero Drift		Full			±1/16			±1/16	LSB
Bipolar Zero Drift		Full			±1/4			±1/4	LSB
Settling Time (5) to 1/2 LSB									
High Impedance (11)	(from all 0's to all 1's)	+25°C		65	75		65	75	ns
or	(from all 1's to all 0's)								

5

PARAMETER	TEMP	HI-5618A/B-2 HI-5618A/B-8 MIN	HI-5618A/B-2 HI-5618A/B-8 TYP	HI-5618A/B-2 HI-5618A/B-8 MAX	HI-5618A/B-5 MIN	HI-5618A/B-5 TYP	HI-5618A/B-5 MAX	UNITS
TRANSFER CHARACTERISTICS (Continued)								
Glitch (5) - Major Carry Transition								
Duration	+25°C		20			20		ns
Amplitude (See Fig. 4)	+25°C		350			350		mV
Area	+25°C		3500			3500		mV–ns
Power Supply Sensitivity (5)								
V_{ps+} = +5V, V_{ps-} = -13V to -16.5V								
Gain (Input Code 11 . . . 1)	+25°C			±5			±5	
Unipolar Zero (Input Code 00 . . . 0)	+25°C		±0.5			±0.5		ppm of
Bipolar Offset (Input Code 00 . . . 0)	+25°C		±1.5			±1.5		FSR/% Vps (9)
V_{ps-} = -15V, V_{ps+} = 4.5V to 5.5V								
Gain (Input Code 11 . . . 1)	+25°C			±5			±5	
Unipolar Zero (Input Code 00 . . . 0)	+25°C		±0.5			±0.5		
Bipolar Offset (Input Code 00 . . . 0)	+25°C		±1.5			±1.5		
OUTPUT CHARACTERISTICS								
Output Current Unipolar	+25°C		-5			-5		mA
Bipolar	+25°C		±2.5			±2.5		mA
Output Resistance	+25°C		500			500		Ω
Output Capacitance	+25°C		20			20		pF
Output Voltage Range (7) Unipolar	+25°C		+10			+10		V
	+25°C		+5			+5		V
Bipolar	+25°C		±10			±10		V
	+25°C		±5			±5		V
	+25°C		±2.5			±2.5		V
Output Compliance Voltage (5)	+25°C		±1.5			±1.5		V
Output Noise Voltage (8) 0.1Hz to 100Hz	+25°C		30			30		μV_{p-p}
0.1Hz to 1Mhz	+25°C		100			100		μV_{p-p}
POWER REQUIREMENTS (4)								
V_{ps+}	Full	4.5	5	15	4.75	5	15	V
V_{ps-}	Full	-13.5	-15	-16.5	-14.25	-15	-15.75	V
I_{ps+} (10) (All 1's or all 0's in either	+25°C		9			9		mA
TTL or CMOS mode) (3, 4)	Full			12			12	mA
I_{ps-} (10) (All 1's or all 0's in either	+25°C		19			19		mA
TTL or CMOS mode) (3, 4)	Full			26			26	mA

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5618 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions)
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The V_{ps+} tolerance is ± 10% for HI-5618A/B -2, -8; and ± 5% for HI-5618A/B-5.
4. For CMOS compatibility connect digital power supply ($+4.5V \leq V_{DD} \leq +10V$) to pin 1 and short pin 2 to pin 1.
5. See definitions.
6. These errors may be adjusted to zero using external potentiometers R_1, R_2, R_3. R_1 and R_2 each provide more than ± 3 LSB's adjustment. (See Operating Instructions). The specifications listed under initial accuracy are based on use of an external op amp, internal span and offset resistors, and 100Ω ± 1% resistors, in place of R_1 and R_2.
7. Using an external op amp with the internal span and offset resistors. See Operating Instructions.
8. Specified for all "1's" or all "0's" digital input.
9. FSR is "Full Scale Range", i.e., 20V for ± 10V range; 10V for ± 5V range, etc. Nominal full scale output current is 5mA.
10. After 30 seconds warm-up.
11. See Test Circuit, Figure 3.
12. See Test Circuit , Figure 4.

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY - Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straightline transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY - For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for any two adjacent codes. A Differential Nonlinearity of $\pm$ 1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in fractional LSB's, or parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Gain error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25^{o}C) and low ranges (+25^{o}C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

ZERO DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Zero error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Zero Drift is calculated for both high (T_H - 25^{o}C) and low (+25^{o}C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst case drift.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale transition. D/A settling time may vary depending upon the impedance level being driven. A comparator presents a high impedance, while an op amp connected for current to voltage conversion presents a low impedance. Figure 3a shows the test circuit used for testing the HI-5618A/B for T_S (OFF) into a high impedance.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011 . . . 1 to 100 . . . 0 or vice versa. For example, if turn ON is greater than turn OFF for 100 . . . 1 to 100 . . . 0, an intermediate state of 000 . . . 0 exists, such that, the output momentarily glitches toward zero output. In general, when a D/A is driven by a set of external logic gates, the unmatched turn on - turn off times at the gates will add to the glitch problem. See Figure 4.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in the +5V or -15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE VOLTAGE

When the D/A converter is used without an op amp, it may be configured for various ranges of voltage at its output. However, Compliance Voltage is the maximum full scale voltage for which the converter will comply with its specifications.

5

OPERATING INSTRUCTIONS

DECOUPLING AND GROUNDING

For best accuracy and high speed performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5618A/B; preferably to the device pin. A solid tantalum or electrolytic capacitor in parallel with a smaller ceramic type is recommended.

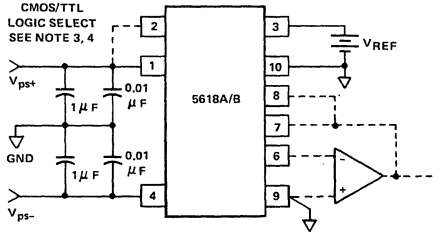


FIGURE 1

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

Make connections as shown in the table and Figure 2, for five standard output ranges:

	OUTPUT RANGE	CONNECTIONS PIN 5 TO	CONNECTIONS PIN 7 TO	CONNECTIONS PIN 8 TO	BIAS RESISTOR R_B
Unipolar Mode	0 to +10V	NC	A	NC	390Ω
	0 to +5V	NC	A	6	330Ω
Bipolar Mode	± 10V	D	NC	A	400Ω
	± 5V	D	A	NC	360Ω
	± 2.5V	D	A	6	390Ω

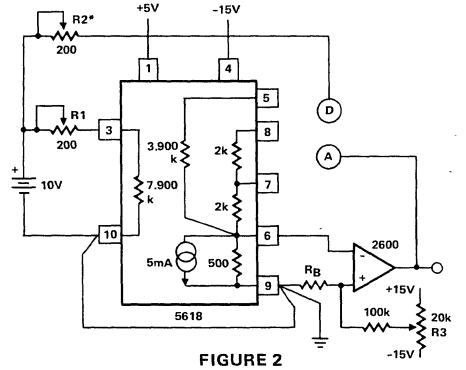


FIGURE 2

*Used in Bipolar Mode only.

The HI-5618A/B accepts an 8 bit digital word in Straight Binary code. In the bipolar mode this code becomes Offset Binary. Also in bipolar mode, the MSB may be complemented using an external inverter to obtain 2's complement code. Here are the correct outputs for some key input codes:

UNIPOLAR - STRAIGHT BINARY
0V TO +10V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1 LSB	= 9.96094V
10 0	½FS	= 5.00000V
01 1	½FS - 1 LSB	= 4.96094V
00 0	Zero	= 0.00000V

UNIPOLAR - STRAIGHT BINARY
0V TO +5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1 LSB	= 4.98047V
10 0	½FS	= 2.50000V
01 1	½FS - 1 LSB	= 2.48047V
00 0	Zero	= 0.00000V

BIPOLAR - OFFSET BINARY
± 10V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS -1 LSB	= +9.92188V
10 0	Zero	= +0.00000V
01 1	Zero -1 LSB	= -0.07813V
00 0	-FS	= -10.0000V

BIPOLAR - TWO'S COMPLEMENT **
± 10V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1 LSB	= +9.92188V
00 0	Zero	= +0.00000V
11 1	Zero - 1 LSB	= -0.07813V
10 0	-FS	= -10.0000V

** Invert MSB with external inverter to obtain two's complement coding.

5

Output Accuracy of the HI-5618A/B is affected directly by the reference voltage, since $I_O(F/S) \simeq 4\ (V_{REF}/8k\Omega)$. For precision performance, a stable +10V reference with low temperature coefficient is recommended, such as HARRIS HA-1610.

The output current may be converted to voltage using an external op amp with the internal span and offset resistors, as shown above in the table. The op amp should have good front end temperature coefficients. For example, the HA-2600/2605 is well suited to this application, with offset voltage and offset current tempco's of 5 μV/°C and 1nA/°C, respectively. The input reference resistor (7.9kΩ) and bipolar offset resistor (3.9kΩ) are both intentionally set low by 100Ω to allow the user to externally trim out initial errors to a high degree of precision.

For high speed voltage output applications where fast settling is required, the HA-2510/25 is recommended for settling times better than 250ns to 1/2 LSB. The HA-5190/95 is recommended for applications requiring settling times less than 150ns. (See Applications).

CALIBRATION

UNIPOLAR MODE -

1. Apply zero (all 0's) input, and adjust R_3 for 0V output.
2. Apply full scale (all 1's) input, and adjust R_1 for:
   +9.96094 Volts, +10 Volt range
   +4.98047 Volts, +5 Volt range

BIPOLAR MODE -

1. Short the op amp output to its inverting input, then adjust R_3 for 0V output. Remove the short.

2. Apply negative full scale (also called bipolar offset): All 0's for offset binary; 1000 . . . . for 2's complement. Adjust R_2 for output voltages as follows:
   -10 Volts, ±10 Volt Range
   -5 Volts, ± 5 Volt Range
   -2.5 Volts, ±2.5 Volt Range

3. Apply positive full scale (all 1's for offset Binary; 0111. . . . for 2's complement) Adjust R_1 for output voltages as follows:
   +9.92188 Volts, ± 10 Volt Range
   +4.96094 Volts, ±5 Volt Range
   +2.48047 Volts, ±2.5 Volt Range

4. Apply zero input (1000. . . . for offset Binary; 0000. . . . for 2's complement). Output should be zero volts. Any error is due to nonlinearity in the DAC, and cannot be nulled without disrupting the calibration in steps 2 and 3.

SETTLING TIME

Turn-off settling time ($T_{S(OFF)}$) is somewhat longer than $T_{S(ON)}$ for the HI-5618. Typical $T_{S(OFF)}$ performance is shown in Figure 3C, using the circuit of Figure 3A.

Refer to Figure 3B; Settling time following turn-off equals T_X plus T_D. The comparator delay T_D may be measured at 1mV/cm, using a Tektronix 7A13 differential comparator or equivalent. Then, T_X is easily measured in a short procedure:

- Adjust delay on generator # 2 for T_X approximately 1μs
- Switch the LSB to +5V (ON).
- Adjust the V_{LSB} supply for 50 percent triggering at COMP. OUT (equal brightness).
- DVM reads -1 LSB. Adjust V_{LSB} supply so DVM reads -1/2 LSB.
- Switch the LSB to P (pulse); COMP. OUT pulse disappears.
- Reduce generator # 2 delay until COMP. OUT pulse reappears; adjust delay for "equal brightness".
- Measure T_X from scope. (Any overshoot will be less than 1/2 LSB, so it is not necessary to examine the other side of the envelope, i.e. final value plus 1/2 LSB.)

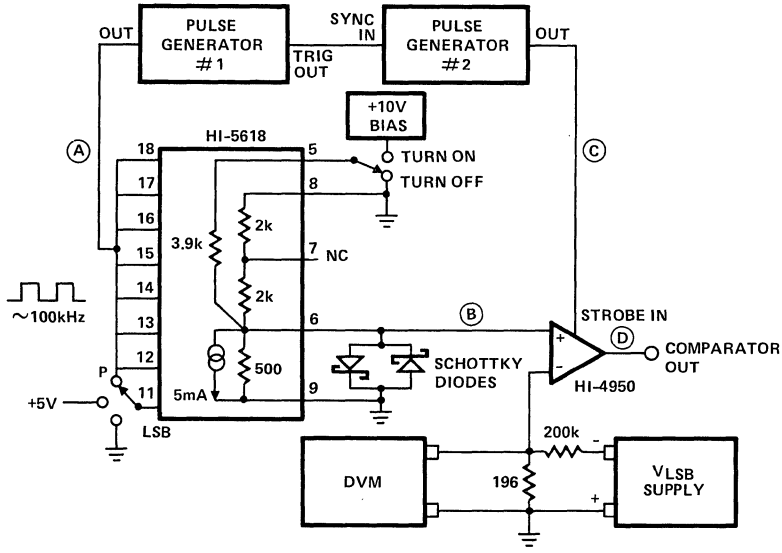


Figure 3A

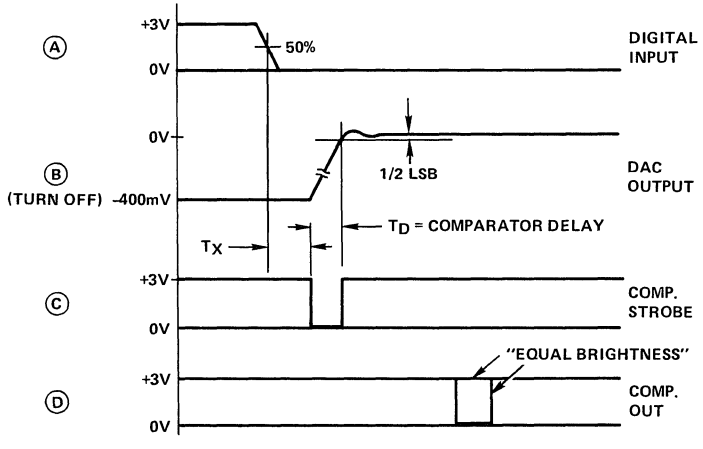


Figure 3B

TEST CIRCUIT (Continued)

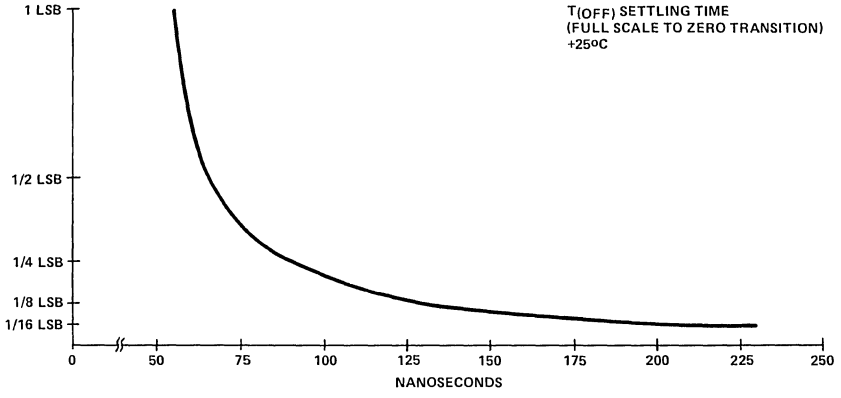
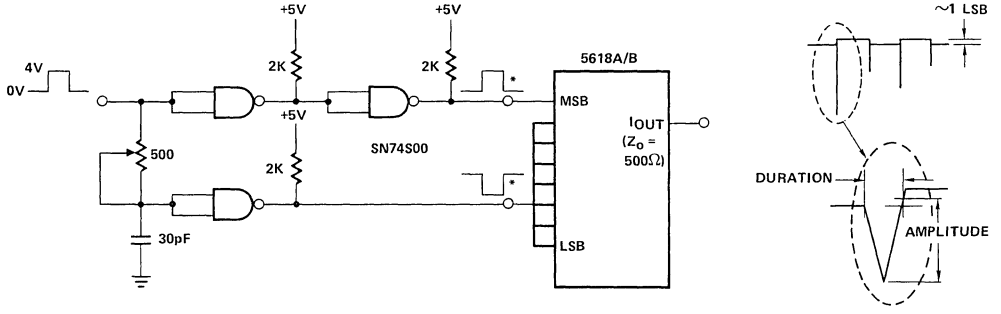


Figure 3C

OUTPUT GLITCH MEASUREMENT

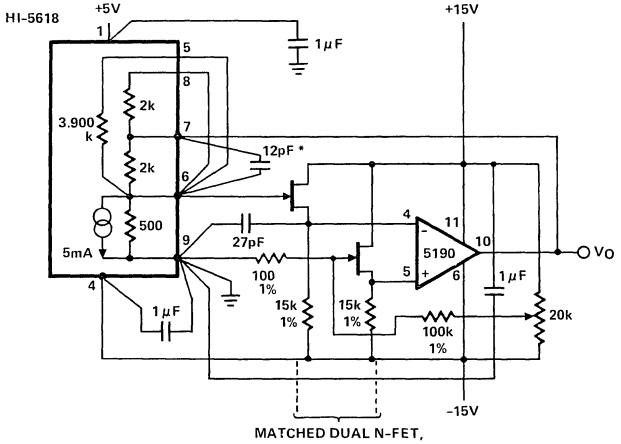


* ADJUST 500Ω TRIMMER SO THAT INPUT SIGNALS CROSS THEIR RESPECTIVE SWITCHING THRESHOLDS AT THE SAME TIME.

Figure 4

APPLICATIONS

HIGH SPEED VOLTAGE OUTPUT



* NOMINAL VALUE, SELECTED FOR OPTIMUM STEP RESPONSE.

HI-5712/5712A

High Performance 12 Bit Analog to Digital Converter

FEATURES

- MICROPROCESSOR COMPATIBLE
- CONVERSION TIME 10μsec MAX OVER TEMP.
- NO MISSING CODES OVER TEMPERATURE
- INTERNAL +10V REFERENCE
- INTERNAL CLOCK WITH EXTERNAL OVERRIDE CAPABILITY
- SERIAL OUTPUT
- TTL/CMOS COMPATIBLE
- TRISTATE PARALLEL OUTPUTS
- 40 PIN DIP
- MIL-STD-883 PROCESSING AVAILABLE

APPLICATIONS

- MULTI-CHANNEL DATA ACQUISITION SYSTEMS
- STATUS MONITORING SYSTEMS
- PROCESS CONTROL SYSTEMS
- INSTRUMENTATION
- HIGH RELIABILITY DAS's

DESCRIPTION

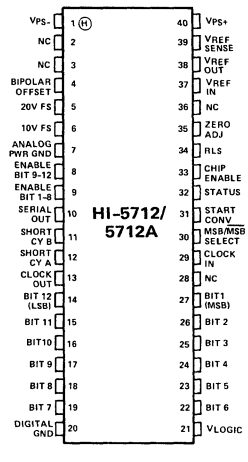
The HI-5712/5712A is a 12-bit successive approximation analog-to-digital converter (ADC) intended for high-speed, high-performance data conversion applications. An 8μs conversion time for an accurate 12 bit conversion with low gain and offset temperature coefficients are among its many features. Numerous functions can be software controlled to meet a variety of ADC requirements.

The highly flexible input design accepts user programmed unipolar and bipolar inputs of: 0 to +10V, 0 to +20V, ±5V and ±10V full scale signal levels. The internal precision +10V reference delivers up to 10mA of output current with ultra high temperature stability. This reference is intended for biasing the ADC reference input, although other configurations can be implemented. A remote sense line is provided for applications requiring usage of the precision reference elsewhere in the system.

The output code select line and the short cycle control inputs are latched internally for microprocessor compatibility and provide selection of either binary or 2's complement output code, and resolution of 6, 8, 10 or 12 bits, respectively. A flexible interface is provided for 8, 12 and 16 bit systems via the chip select line and the word length control pins. The latter allows independent tri-state enabling of parallel output bits 1-8 and 9-12. A serial data output line is provided for applications requiring remote data transmission.

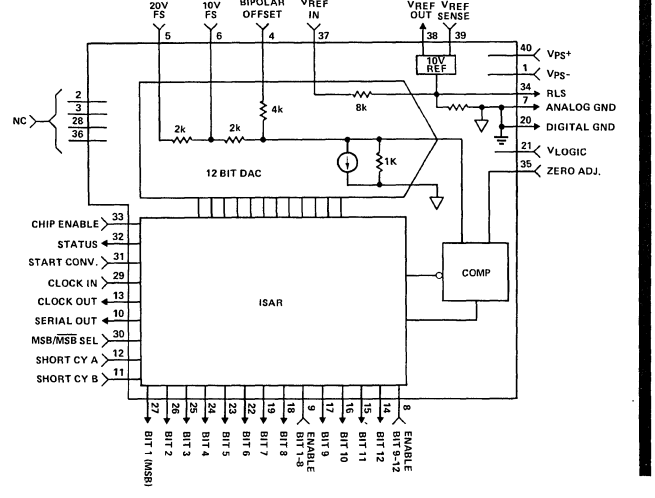
The HI-5712/5712A is manufactured with hermetically sealed leadless chip carriers (LCC's) mounted to both sides of a multi-layer ceramic substrate which results in a compact 40 pin dual-in-line package. The HI-5712A is intended for military, industrial and instrumentation applications. MIL-STD-883 class B and high reliability commercial grades are both available as standard products.

PINOUT



Section 11 for Packaging

FUNCTIONAL DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Power Supply Inputs		Power Dissipation (Pd) 2 Watts	
V_{PS}^+	+20V	Operating Temperature Range	
V_{PS}^-	-20V	HI-5712-2, HI-5712A-2	55°C to +125°C
V_{LOGIC}	+10V	HI-5712-5, HI-5712A-5	0°C to +75°C
V_{REF} IN (Pin 37)	0V, V_{PS}^+	HI-5712-7, HI-5712A-7	0°C to +75°C (Hi Rel)
V_{REF} SENSE (Pin 39)	0V, V_{PS}^+	HI-5712-8, HI-5712A-8	-55°C to +125°C (Hi Rel)
Digital Inputs	-1V, V_{LOGIC}	Storage Temperature Range	
			65°C to +150°C

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{PS} = +15V, V_{PS}^- = -15V, V_{LOGIC} = +5V, V_{REF} In = Internal V_{REF}, Full Scale = +10V, Conversion Speed = 9 µs TYP (Internal Clock), 12-BIT Conversion, Unless otherwise noted.)

			HI-5712A-2 HI-5712A-8 HI-5712-2 HI-5712-8			HI-5712A-5 HI-5712A-7 HI-5712-5 HI-5712-7			
PARAMETER		TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
RESOLUTION		Full			12			12	BITS
NONLINEARITY	HI-5712A	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/4	±1/2		±1/4	±1/2	LSB
	HI-5712	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/2	±1		±1/2	±1	LSB
DIFFERENTIAL NONLINEARITY	HI-5712A	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/4	±1/2		±1/4	±1/2	LSB
	HI-5712	+25°C		±1/4	±1/2		±1/4	±1/2	LSB
		Full		±1/2	±1		±1/2	±1	LSB
		NO MISSING CODES GUARANTEED OVER TEMPERATURE							
INHERENT QUANTIZATION ERROR		Full			±1/2			±1/2	LSB
UNIPOLAR OFFSET ERROR (Note 2) (Adjustable to Zero)		+25°C		.3	.6		.3	.6	%FSR
BIPOLAR OFFSET ERROR (Note 2) (Adjustable to Zero)		+25°C		.3	.6		.3	.6	%FSR
GAIN ERROR (note 2) (Adjustable to Zero)		+25°C		.1	.3		.1	.3	%FSR
ADJUSTMENT RANGE									
UNIPOLAR OFFSET		+25°C	±1	±2		±1	±2		%FSR
BIPOLAR OFFSET		+25°C	±1	±2		±1	±2		%FSR
GAIN		+25°C			.3			.3	%FSR
TEMPERATURE STABILITY (With Internal V_{REF})									
UNIPOLAR OFFSET	HI-5712A	Full		±2	±5		±2	±5	ppm FSR/°C
DRIFT	HI-5712	Full		±4	±15		±4	±15	ppm FSR/°C
BIPOLAR OFFSET	HI-5712A	Full		±4	±10		±4	±10	ppm FSR/°C
DRIFT	HI-5712	Full		±8	±25		±8	±25	ppm FSR/°C
GAIN DRIFT	HI-5712A	Full		±5	±10		±5	±10	ppm FSR/°C
	HI-5712	Full		±10	±20		±10	±20	ppm FSR/°C
		NO MISSING CODES GUARANTEED OVER TEMPERATURE							

5

PARAMETER	TEMP	HI-5712A-2/-8 HI-5712-2/-8 MIN	TYP	MAX	HI-5712A-5/-7 HI-5712-5/-7 MIN	TYP	MAX	UNITS
CONVERSION SPEED (Internal Clock)								
12 BIT	+25°C		9.0	10.0		9.0	10.0	μs
10 BIT	"		6.8	8.5		6.8	8.5	μs
8 BIT	"		5.6	7.0		5.6	7.0	μs
6 BIT	"		4.4	5.4		4.4	5.4	μs
MAXIMUM CONVERSION SPEED AT 12 BITS WITH EXTERNAL CLOCK (Note 3)	Full		6.5			6.5		μs
ANALOG INPUT CHARACTERISTICS								
INPUT VOLTAGE RANGE								
UNIPOLAR	Full	10			10			V
	Full	20			20			V
BIPOLAR	Full	±5	±5		±5	±5		V
	Full	±10	±10		±10	±10		V
INPUT IMPEDANCE								
10V FS (PIN 6)	Full	1.6	2	2.4	1.6	2	2.4	KΩ
20V FS (PIN 5)	Full	3.2	4	4.8	3.2	4	4.8	KΩ
V_{REF} IN (PIN 37)	Full	6.4	8	9.6	6.4	8	9.6	KΩ
ANALOG OUTPUT CHARACTERISTICS								
V_{REF} OUTPUT VOLTAGE	+25°C	9.970	10.000	10.030	9.970	10.000	10.030	V
V_{REF} OUTPUT CURRENT	Full	10			10			mA
VREF OUTPUT TC HI-5712A	Full		±10	±15		±10	±15	ppm FSR/°C
VREF OUTPUT TC HI-5712	Full		±10	±15		±10	±15	ppm FSR/°C
DIGITAL INPUT CHARACTERISTICS								
INPUT VOLTAGE (Note 8)								
LOGIC 1	Full	3.3	2.7		3.3	2.7		V
LOGIC 0	Full		1.2	.8		1.2	.8	V
INPUT CURRENT (Note 8)								
LOGIC 1 (VCC)	Full	-25	0	+25	-25	0	+25	μA
LOGIC 0 (GND)	Full		-200	-400		-200	-400	μA
ETERNAL CLOCK (Note 3)	Full			2.5			2.5	MHz
DIGITAL OUTPUT CHARACTERISTICS								
OUTPUT VOLTAGE								
LOGIC 1 I_{OH} = -800 A	Full	3.5	4.0		3.5	4.0		V
LOGIC 0 I_{OL} = +3.2mA	Full	.2	.4			.2	.4	V
OUTPUT CURRENT								
LOGIC 1 VO = 3.5V	Full	-800	-1000		-800	-1000		μA
LOGIC 0 VO = .4V	Full	3.2	4.0		3.2	4.0		mA
DIGITAL INPUT TIMING CHARACTERISTICS								
CHIP ENABLE TO START CONVERT t_{cd}	Full	50			50			nsec
START CONVERT PULSE LOW t_{scl}	Full	100			100			nsec
START CONVERT PULSE HIGH t_{sch}	Full	50			50			nsec
CONTROL SETUP TIME t_s	Full	100			100			nsec
CONTROL HOLD TIME t_h	Full	100			100			nsec
CLOCK INPUT LOW t_{pwl}	Full	125			125			nsec
CLOCK INPUT HIGH t_{pwh}	Full	150			150			nsec
CLOCK INPUT PERIOD t_{cl}	Full	400			400			nsec
ENABLE 1-8, 9-12 PULSE WIDTH t_{em}	Full	100			100			nsec

5

PARAMETER	TEMP	HI-5712A-2/-8 HI-5712-2/-8 MIN	TYP	MAX	HI-5712A-5/-7 HI-5712-5/-7 MIN	TYP	MAX	UNITS
DIGITAL OUTPUT TIMING CHARACTERISTICS (See Figure 6)								
THREE STATE ENABLE DELAY t_{oe}	Full		40	50		40	50	nsec
THREE STATE DISABLE DELAY t_{od}	Full		60	100		60	100	nsec
START CONVERT TO STATUS DELAY t_{sd}	Full		70	100		70	100	nsec
START CONVERT TO CLOCK OUT DELAY t_{scd}			200	500		200	500	nsec
CLOCK TO SERIAL OUT DELAY t_{psd}	Full	100	150	200	100	150	200	nsec
LAST CLOCK TO STATUS DELAY t_{scdt}	Full	50	75	100	50	75	100	nsec
PARALLEL DATA TO STATUS DELAY t_{ds}	Full	50	75		50	75		nsec
LAST SERIAL BIT TO STATUS DELAY t_{da}	Full	50	75		50	75		nsec
CLOCK INPUT TO CLOCK OUT DELAY t_{dcl}	Full		25	50		25	50	nsec
PARALLEL DATA OUTPUT CODES								
UNIPOLAR (Note 4)	Positive True Binary							
BIPOLAR (Note 4)	Positive True Offset Binary							
	Positive True Two's Complement Binary							
SERIAL DATA OUTPUT CODE	Positive True NRZ Code							
POWER SUPPLY REQUIREMENTS (Note 5)								
$V_{PS}+$	Full	+13.5	+15	+16.5	+13.5	+15	+16.5	V
$V_{PS}-$	Full	-13.5	-15	-16.5	-13.5	-15	-16.5	V
V_{LOGIC}	Full	+4.5	+5	+5.5	+4.75	+5	+5.25	V
$I_{PS}+$	Full		27	35		27	35	mA
$I_{PS}-$	Full		42	50		42	50	mA
I_{LOGIC}	Full		4.5	15		4.5	15	mA
POWER SUPPLY SENSITIVITY (Note 6)								
$V_{PS}+$ = +13.5V to +16.5V, $V_{PS}-$ = -15V, V_{LOGIC} = +5V								
UNIPOLAR OFFSET			2	5		2	5	ppm of FSR/ %ΔP.S.
BIPOLAR OFFSET			2	4		2	4	
GAIN			1	3		1	3	
$V_{PS}-$ = -13.5V to -16.5V, $V_{PS}+$ = +15V, V_{LOGIC} = +5V								
UNIPOLAR OFFSET			2	5		2	5	
BIPOLAR OFFSET			2	4		2	4	
GAIN			1	3		1	3	
V_{LOGIC} = +4.5V to +5.5V, $V_{PS}+$ = +15V, $V_{PS}-$ = -15V CONVERSION SPEED (12 Bit with Internal Clock)			±5	±10		±5	±10	%

5

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. See Figure 2 for connections. The initial errors are adjustable to zero by using external trim potentiometers as shown in Figure 3, and 4.
3. The HI-5712A will operate at these speeds (for 12 bit conversion), but parametric performance is not guaranteed.
4. See operating instructions for details.
5. After 60 seconds warm-up.
6. See definitions.
7. These terminals will be used in the future for additional functions. Do not make connections to these pins in your system.
8. TTL compatibility guaranteed.

PIN FUNCTIONS AND DESCRIPTIONS

PIN	SYMBOL	DESCRIPTION
1	V_{ps}-	-15V Power Supply Terminal
2	NC	No Connection See Note 7
3	NC	No Connection See Note 7
4	BIPOLAR OFFSET	Connect to V_{REF} for Bipolar Input Mode. See Operating Instructions for Details.
5	20V FS	20V Full Scale Analog Input
6	10V FS	10V Full Scale Analog Input
7	ANALOG GND	Analog Power Supply Return
8	ENABLE BIT 9-12	Output "Three State" Control. An Input "0" Enables Bits 9 through 12, whereas a "1" Switches these Bits to a High Impedance State.
9	ENABLE BIT 1-8	Output "Three State" Control. An Input "0" Enables Bits 1 through 8, whereas a "1" Switches these Bits to a High Impedance State.
10	SERIAL OUT	NRZ Serial Data Output. To be used in Conjunction with Clock Out for Remote Data Transmission
11	SHORT CY B	See Description for Pin 12
12	SHORT CY A	Digital Inputs Applied to short cycle A and B selects a conversion of 6, 8, 10, or 12-bits:

BITS	SHORT CY A	SHORT CY B
6	0	0
8	0	1
10	1	0
12	1	1

PIN	SYMBOL	DESCRIPTION
13	CLOCK OUT	SAR Clock Output. Used for Decoding Serial Out Data
14	BIT 12	Output Data Bit (LSB)
15	BIT 11	Output Data Bit
16	BIT 10	Output Data Bit
17	BIT 9	Output Data Bit
18	BIT 8	Output Data Bit
19	BIT 7	Output Data Bit
20	DIGITAL GND	Digital Power Supply Return
21	V_{LOGIC}	+5V Power Supply Terminal
22	BIT 6	Output Data Bit
23	BIT 5	Output Data Bit
24	BIT 4	Output Data Bit
25	BIT 3	Output Data Bit
26	BIT 2	Output Data Bit
27	BIT 1	Output Data Bit (MSB)
28	NC	No Connection. See Note 7.
29	CLOCK IN	An External Clock Signal Applied to this Input Overrides the Internal Clock.
30	MSB/$\overline{\text{MSB}}$ SEL	Digital Input Pin. A "1" Applied to this Terminal Selects a Straight Binary or Offset Binary Output Code. A "0" Inverts the MSB to Yield a 2's Complement Binary Output Code.
31	START CONV	Digital Input Pin. A High to Low Transition Initiates the ADC Conversion Cycle.
32	STATUS	Digital Output Pin. A "1" Indicates that the ADC is Busy, While a "0" Denotes that Conversion is Completed and Data is Ready for Retrieval.

PIN FUNCTIONS AND DESCRIPTIONS

PIN	SYMBOL	DESCRIPTION
33	CHIP ENABLE	Digital Input Pin. A "1" Forces the Output Data, Serial Out and Status Terminals to a High Impedance State and the ADC is Disabled. A "0" Enables these ADC Functions.
34	RLS	Reference Low Sense.
35	ZERO ADJ	External Zero Adjustment Pin, See Operating Instructions for Details.
36	NC	No Connection. See Note 7.
37	V_{REF} IN	+10V Reference Input to ADC.
38	V_{REF} OUT	Internal +10V Reference Output, Normally Connected to V_{REF} IN (Pin 37).
39	V_{REF} SENSE	Internal +10V Reference Sensing Terminal, Normally connected to V_{REF} Out (Pin 38). See Operating Instructions for Details.
40	V_{ps+}	+15V Power Supply Terminal.

APPLYING THE HI-5712/5712A

OPERATING INSTRUCTIONS

Conventional ADC systems provide maximum performance when the analog and digital ground lines are tied together at the ADC terminals. This minimizes analog interference due to digital switching noise. For optimum performance, this external grounding procedure should be followed in HI-5712/5712A installations to reinforce the unit's internal analog-to-digital ground connections. Under no circumstances should the Reference Low Sense (RLS) terminal (Pin 34) be connected to system ground.

In practice, the Reference Low Sense (RLS) terminal (Pin 34) normally is connected to zero adjust (or error amplifier) input terminal (Pin 35), either directly or through an appropriate resistor network. See figures 3 and 4.

On the HI-5712/5712A substrate, the power supply lines to each active component are bypassed to ground with 0.01 μF chip capacitors for high frequency noise rejection. For best accuracy, the grounding and decoupling schemes shown in Figures 3 and 4 are recommended. The 10 μF bypass capacitors shown should be connected as close as possible to the HI-5712/5712A, preferably at the device pin.

For applications where usage of potentiometers is highly undesirable, the trim pots shown in Figures 3 and 4 can either be deleted or replaced by precision fixed resistors. (Delete R_3 and R_4; replace R_1 with 25 ohms). When precision fixed resistors are used, the initial offset error and gain error contributions are as specified in page 2.

NOTE: The HI-5712/5712A may latch up if the device is enabled before applying power. Disabling the device following power turn on will remedy this situation. Care supplies do not excessively overshoot their final value during turn on.

CONTROL AND INTERFACE

The HI-5712/5712A features a versatile set of controlling functions which allows a wide variety of applications, including microprocessor bus interfacing.

When the chip enable is set to low, the internal registers are enabled, and the output data lines can be enabled via the output enable control lines. The conversion cycle is initiated at the falling edge of the start conversion pulse. At this time, the MSB/MSB Select, Short Cycle A, and Short Cycle B control information is latched into the internal registers. The status line is also forced into an active high state indicating that a conversion is taking place. At the end of the conversion cycle the status line will be set to low to signify that the data is ready at the tri-state buffers. The various timing relationships are shown in Figure 1.

There are two distinct modes of operation, namely, continuous conversion and single step conversion. Continuous conversion can be easily achieved by connecting the Status line to the Start Convert pin. In this application, an indecision state may occur during the initial power-on conditions. Normal operation is restored by pulsing the chip enable pin to logic high for a period greater than 100 ns.

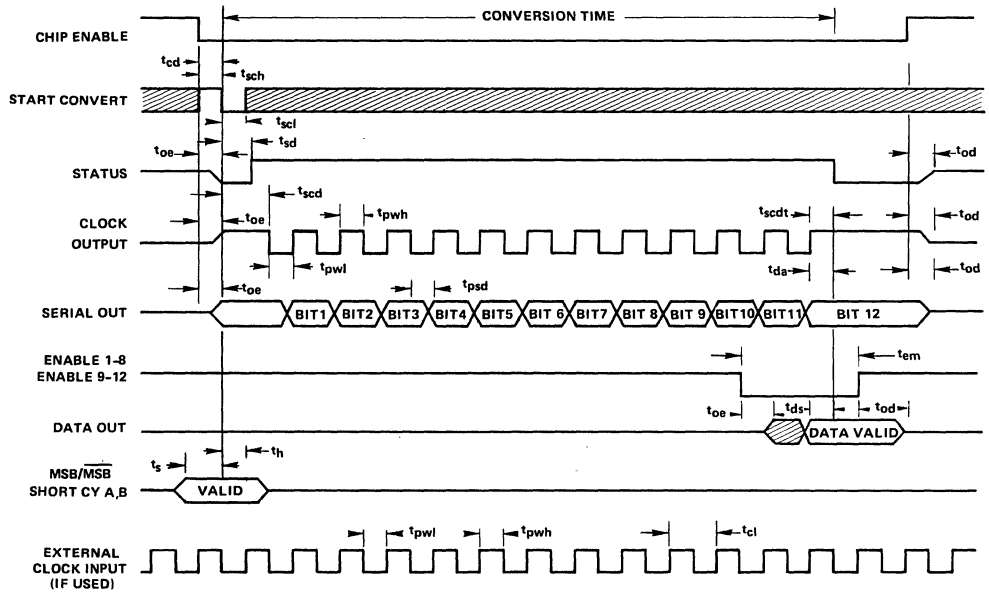


FIGURE 1. HI-5712/5712A TIMING DIAGRAM

5

REMOTE DATA TRANSMISSION

The Serial Data Out is mainly used for remote data transmission, where only a limited number of wires are available.

Serial Output is bit by bit (MSB first, LSB last) in a NRZ (nonreturn-to-zero) format. It changes state only at the positive going edges of the Clock Out, and remains valid during the whole clock period. Parallel data can be constructed by clocking the serial data into a receiving shift register.

In order to minimize transmission error, the negative-going edge of the clock should be used to clock data into the remote shift register. The parallel data will be valid once the status line returns to low. The clocking scheme is shown in Figure 1.

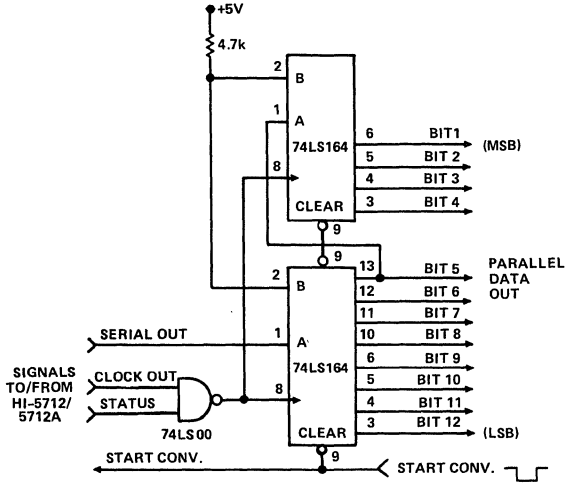


FIGURE 2. DECODING SERIAL DATA OUT

HI-5712/5712A CALIBRATION CHART

OPERATING MODE	ANALOG INPUT CONNECTION	R2 BIAS RESISTOR	MSB/MSB SELECT PIN 30	OFFSET ADJUST ANALOG INPUT VOLTAGE	ADJUST R3 FOR DITHER BETWEEN CODES	GAIN ADJUST ANALOG INPUT VOLTAGE	ADJUST R1 FOR DITHER BETWEEN CODES	LSB WEIGHT
UNIPOLAR STRAIGHT BINARY 0V to +10V	10VFS PIN 6	667Ω	HIGH	+1.22mV	0000 0000 0000 0000 0000 0001	+9.9963V	1111 1111 1110 1111 1111 1111	2.44mV
UNIPOLAR STRAIGHT BINARY 0V to +20V	20VFS PIN 5	800Ω	HIGH	+2.44mV	0000 0000 0000 0000 0000 0001	+19.9927V	1111 1111 1110 1111 1111 1111	4.88mV
BIPOLAR OFFSET BINARY -5V to +5V	10VFS PIN 6	580Ω	HIGH	-4.9988V	0000 0000 0000 0000 0000 0001	+4.9963V	1111 1111 1110 0111 1111 1111	2.44mV
BIPOLAR OFFSET BINARY -10V to +10V	20V FS PIN 5	667Ω	HIGH	-9.9976V	0000 0000 0000 0000 0000 0001	+9.9927V	1111 1111 1110 1111 1111 1111	4.88mV
BIPOLAR 2's COMPLEMENT -5V to +5V	10V FS PIN 5	580Ω	LOW	-4.9988V	1000 0000 0000 1000 0000 0001	+4.9963V	0111 1111 1110 0111 1111 1111	2.44mV
BIPOLAR 2's COMPLEMENT 10V to +10V	20V FS PIN 6	667Ω	LOW	-9.9976V	1000 0000 0000 1000 0000 0001	+9.9927V	0111 1111 1110 0111 1111 1111	4.88mV

CALIBRATION PROCEDURE- Refer to Calibration Chart and to Figures 3 and 4 for appropriate analog input connections, value of bias resistor, and MSB/MSB select.

STEP 1 OFFSET ADJUSTMENT

- Set analog input to the appropriate value for offset adjustment.
- Adjust R3 for dither between codes shown in calibration chart.

STEP 2 GAIN ADJUSTMENT

- Set analog input to the appropriate value for gain adjustment.
- Adjust R1 for dither between codes shown in calibration chart.

NOTE: This calibration procedure insures that the transfer characteristic produced by connecting the midpoints of all quantization intervals passes through the origin.

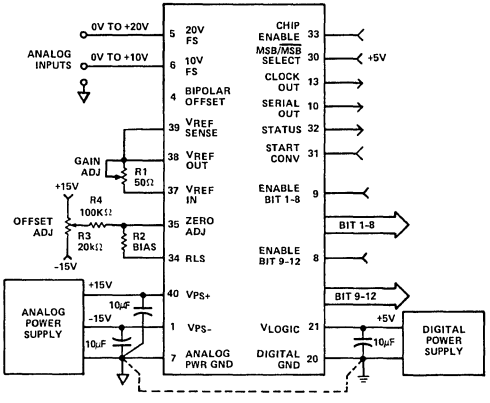


FIGURE 3. UNIPOLAR INPUT CONNECTIONS - STRAIGHT BINARY OUTPUT CODE

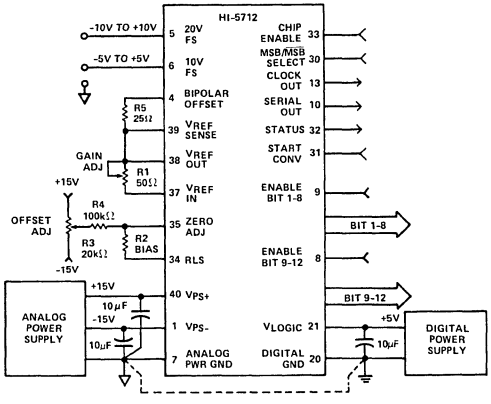


FIGURE 4. BIPOLAR INPUT CONNECTIONS

DEFINITIONS

Least Significant Bit (LSB) - The LSB of an Analog-to-Digital Converter (ADC) is defined to be the digital output bit carrying the lowest numerical weight ($\frac{1}{2}^n$); or the Analog input shift associated with this bit (FSR/2^n) which is the smallest possible Analog input step that can be resolved.

Most Significant Bit (MSB) - The Digital output bit carrying the highest numerical weight (½); or the Analog input shift associated with this bit. In a Binary ADC the MSB indicates the Analog input reaches its ½ FSR.

Resolution - An indication of the number of possible analog input levels an ADC will resolve. Usually it is expressed as the number of output bits. For example, a 12 bit Binary ADC can have $2^{12} = 4096$ possible output codes and it has a resolution of 12 bits.

Nonlinearity (Linearity Error) - A measure of the deviation of each individual code from an ideal straight line transfer curve drawn between zero and full scale. The deviation of a code from the ideal straight line is measured from the middle of each particular code.

Code Width - A fundamental quantity for ADC specifications, it is defined as the range of Analog input values which produce a given digital output code. The ideal value of a code width is equivalent to FSR/2^n, where n is the number of bits.

Differential Nonlinearity - A measure of the deviation between the actual code width of an ADC from the ideal code width. A specification which guarantees no missing codes requires that every code must have a non-zero width.

Quantizing Error (or uncertainty) - The uncertainty introduced by partitioning the Analog continuum into 2^n discrete ranges for n-BIT conversion. The Analog values within a given quantum are normally assigned to the nominal midrange value, represented by the same digital code and therefore, a quantization uncertainty of $\pm$½ LSB is inherently associated with a given resolution.

Unipolar Offset Error - A measure of the difference between the ideal (+½LSB) and the actual analog input level required to produce the first output digital code transition (00- - -0 to 00- - -01). It is usually expressed in percent of full scale range (%FSR).

Bipolar Offset Error - A measure of the difference between the ideal (½FSR -½LSB) and the actual analog input level required to produce the major carry output digital code transition (from 011- - -0 to100- - -0). It is usually expressed in percent of full scale range (%FSR).

5

Gain Error - The gain of an ADC is defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation between the actual gain from the ideal gain of FS-2LSB. It is usually expressed in percent of full scale range (%FSR).

Unipolar Offset Drift - A measure of the change in unipolar offset over the specified temperature range expressed in parts per million of full scale range per ^oC (PPM of FSR/^oC).

Gain Drift - A measure of the change in gain (with offset error removed) over the specified termperature range expressed in parts per million of full scale range per ^oC (PPM of FSR/^oC).

Bipolar Offset Drift - A measure of the change in bipolar offset over the specified temperature range expressed in parts per million of full scale range per ^oC (PPM of FSR/^oC).

Power Supply Sensitivity - A measure of the change in gain, offset, and conversion speed of the ADC resulting from a change in supply voltages. It is expressed in parts per million of full scale range per percent of change in power supply voltages (PPM of FSR/%).

Conversion Speed - The measure of how long it takes an ADC to arrive at the proper output code. It is the time between the edge of the digital command that starts conversion and the edge of the status line signal which signifies that the conversion is completed.

Throughput Rate - For SAR-Types, ADC's throughput rate is defined as the total number of conversions in a given time period. Usually, it is expressed in conversions per second although, the term Hertz is generally accepted.

HARRIS

HI-5900

Analog Data Acquisition Signal Processor

FEATURES

- INPUT OVERVOLTAGE PROTECTION
- 50kHz THROUGHPUT
- 12-BIT ACCURACY
- OUTPUT TRACK/HOLD AMPLIFIER
- ZERO OFFSET ADJUSTMENT
- DIFFERENTIAL INPUT CHANNELS
- SOFTWARE CONTROLLED GAIN AND CHANNEL SELECT
- 85dB CMRR
- COMPACT 32 PIN DIP
- MIL-STD-883 SCREENING AVAILABLE

APPLICATIONS

- HIGH PERFORMANCE DATA ACQUISITION
- MILITARY SYSTEMS

DESCRIPTION

The HI-5900 comprises "front end" components of a data acquisition system including an eight channel differential multiplexer, programmable gain instrumentation amplifier (PGA), and Track and Hold amplifier. Adding a timing circuit and one A to D converter yields a complete data acquisition system. A 50kHz channel-to-channel throughput rate is achieved when the HI-5900 is used with a fast 12 bit A to D converter such as HARRIS HI-5712.

Each output line of the input multiplexer is buffered by a high-quality non-inverting amplifier. This isolates each line from source resistances external to the 5900, preserving the high CMRR of the instrumentation amplifier block. Also, the buffers provide a high input impedance for each channel.

The PGA, which includes an op amp, a monolithic resistor network and a four channel differential multiplexer, offers precision gain values of 1,2,4, and 8. The voltage gain is selected by a two bit digital word. The output of the PGA drives the Track and Hold amplifier, and the ground side of the PGA is isolated by a buffer amplifier to maintain a high CMRR.

The output Track/Hold amplifier is a monolithic device, internally connected for non-inverting unity gain. In the sample mode is operates as a high performance buffer amplifier. With an external holding capacitor, it may be switched to HOLD with an aperture delay of 50ns and 10pC of charge transfer.

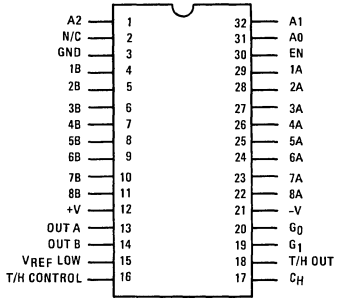
The packaging technique involves monolithic chips mounted in leadless chip carriers (LCC's) and soldered to both sides of a multilayer ceramic substrate. Each LCC may undergo reliability screening such as MIL-STD-883, Method 5004/Class B, before assembly on the substrate. The resulting package is a compact 32 pin DIP.

The HI-5900 is offered as a high performance front-end section for military and industrial data acquisition systems. It is designed for interface with computers and is well suited for high-rel applications.

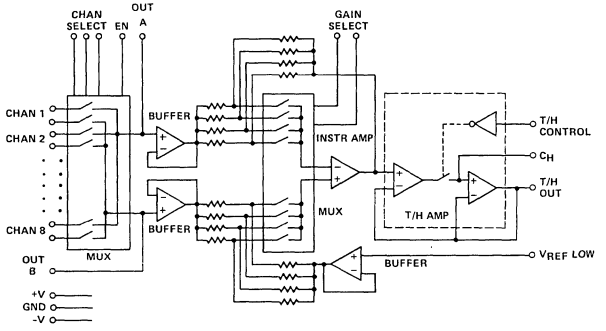
PINOUT

Section 11 for Packaging

TOP VIEW



FUNCTIONAL DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals 40V

Digital Input Overvoltage (Multiplexers)

V_{Supply} (+) +4V

V_{Supply} (-) -4V

Analog Input Overvoltage

V_{Supply} (+) +20V

V_{Supply} (-) -20V

Output Current Short Circuit Protected

Operating Temperature Range

HA-5900-5 $0^oC \leq T_A \leq +75^oC$

HA-5900-2 $-55^oC \leq T_A \leq +125^oC$

Storage Temperature Range $-65^oC \leq T_A \leq +150^oC$

Internal Power Dissipation 650mW

T/H Control Input +8, -15V

ELECTRICAL CHARACTERISTICS Unless otherwise specified: $V_S = \pm 15V$; $C_H = 1000pF$; $V_{IH} = 4.0V$; $V_{IL} = 0.8V$

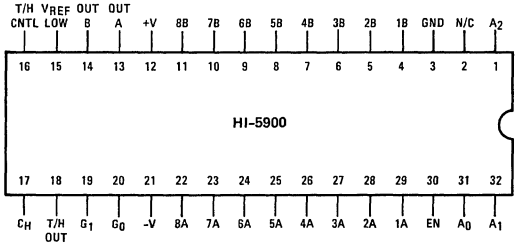
		HI-5900-2 -55°C to +125°C			HI-5900-5 0°C to +70°C			
PARAMETER	TEMP	MIN	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG INPUT CHAR., EACH CHANNEL								
Offset Voltage	+25°C		2	7		3	10	mV
	Full			9			12	mV
Bias Current	+25°C		80	300		80	300	nA
	Full		90	600		80	600	nA
Offset Current	+25°C		15	150		20	150	nA
	Full		30	300		30	300	nA
Common Mode Range	Full	±10			±10			V
Common Mode Rejection Ratio ($V_{CM} = \pm 10V$) Any Gain	Full	80	85		74	85		dB
DIGITAL INPUT CHAR.								
Multiplexer Digital Input Current (High or Low)	Full		0.5	1		0.5	1	μA
Track/Hold Digital Input Current								
$V_{IN} \leq 0.8V$	Full			0.8			0.8	mA
$V_{IN} \geq 4.0V$	Full			20			20	μA
TRANSFER CHARACTERISTICS								
Small Signal Bandwidth (Gain = 1)	+25°C		2			2		MHz
Full Power Bandwidth (Gain = 1, $V_O = \pm 10V$)	+25°C		70			70		kHz
Crosstalk (Sample Mode, Gain = 8, 1kHz 20VP -P Input on all but Selected Channel)	+25°C	-80	-90		-80	-90		dB
"Off Isolation (Hold Mode, Gain = 1, 1kHz 20V P-P Input)	+25°C		-76			-76		dB
Acquisition Time (Note 2), to 0.01%	+25°C		9			9		μs
Gain - Absolute Error								
Gain Of 1, 2,	Full		0.01	0.1		0.01	0.2	%
Gain Of 4, & 8	Full		0.01	0.2		0.01	0.2	%
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10			±10			V
Output Current	+25°C	±10			±10			mA
Output Resistance	+25°C		5			5		Ω
DYNAMIC CHARACTERISTICS								
t_{ON}, Enable (MUX)	+25°C		300			300		ns
t_{OFF}, Enable (MUX)	+25°C		300			300		ns
Slew Rate	+25°C		±4			±4		V/μs
Droop Rate (T/H)	+25°C		5			5		nV/μs
	Full			20			5	μV/μs
Charge Transfer (T/H)	25°C		10			10		pC
Aperture Delay (T/H)	+25°C		50			50		ns
Aperture Uncertainty (T/H)	+25°C		5			5		ns
POWER SUPPLY CHARACTERISTICS								
I_+	+25°C			13			13	mA
	Full		8.5	15		8.0	15	mA
I_-	+25°C			13			13	mA
	Full		6.5	15		6.0	15	mA
Power Supply Rejection Ratio, V+	Full	76	90		70	90		dB
Power Supply Rejection Ratio, V-	Full	80	100		80	100		dB

NOTES:
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Acquisition Time is defined for a change of channel (+10V on chan. 1 to 0V on chan. 8) with simultaneous change from HOLD to TRACK mode. Gain = 1.

PIN	SYMBOL	DESCRIPTION
4	1B	Non-Inverting Side of the Eight Differential Input Channels
5	2B	
6	3B	
7	4B	
8	5B	
9	6B	
10	7B	
11	8B	
29	1A	Inverting Side of the Eight Differential Input Channels
28	2A	
26	4A	
25	5A	
24	6A	
23	7A	
22	8A	
31	A_0	Digital Channel Select Inputs*
32	A_1	
1	A_2	
20	G_0	Digital Gain Select Inputs*
19	G_1	

PIN	SYMBOL	DESCRIPTION
16	T/H CONTROL	Track/Hold Mode Select*
2	NC	No Connection
3	GND	Signal and Power Ground
12	+V	Positive Supply (+15V)
21	-V	Negative Supply (-15V)
18	T/H OUT	Output of the HI-5900
17	C_H	Hold Capacitor Connection
15	V_{REF} LOW	Reference for the Output on Pin 18
13	OUT A	"A" Output of the Input Multiplexer (Inverting Side of each Channel)
14	OUT B	"B" Output of the Input Multiplexer (Non-Inverting Side of each Channel)
30	EN	Enable Strobe for the Input Multiplexer; Normally Forced High. EN may be used in Conjunction with OUT A and OUT B, to Poll Additional Channels through an External Multiplexer.

* See Programmable Functions



PROGRAMMABLE FUNCTIONS

Input Codes are as follows:

X = DON'T CARE
0 = $V_{IN} \leq +0.8V$;
1 = $V_{IN} \geq +4.0V$, where V_{IN} is the digital input voltage.

1. T/H Control (PIN 16)

0	Track
1	Hold

2. Gain Select

G_1 (PIN 19)	G_0 (PIN 20)	GAIN
0	0	1
0	1	2
1	0	4
1	1	8

3. Channel Select

A_2 (PIN 1)	A_1 (PIN 32)	A_0 (PIN 31)	EN (PIN 30)	CHANNEL
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

PERFORMANCE CURVES

ACQUISITION TIME vs. OUTPUT STEP CHANGE

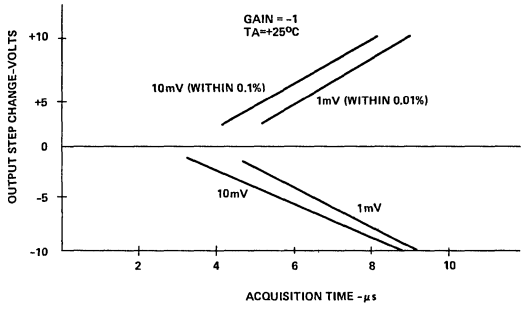


FIGURE 1

INPUT NOISE VOLTAGE vs. FREQUENCY

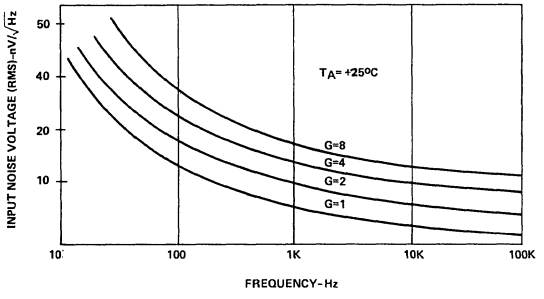


FIGURE 2

TYPICAL T/H AMPLIFIER PERFORMANCE vs. HOLD CAPACITANCE Ch

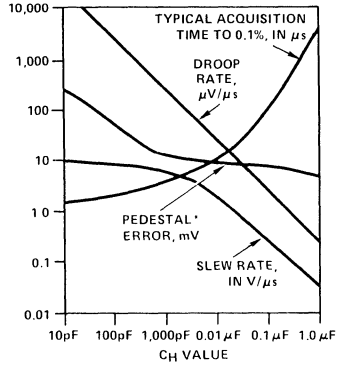


FIGURE 3

INPUT LEAKAGE, BIAS & OFFSET CURRENT vs. TEMPERATURE

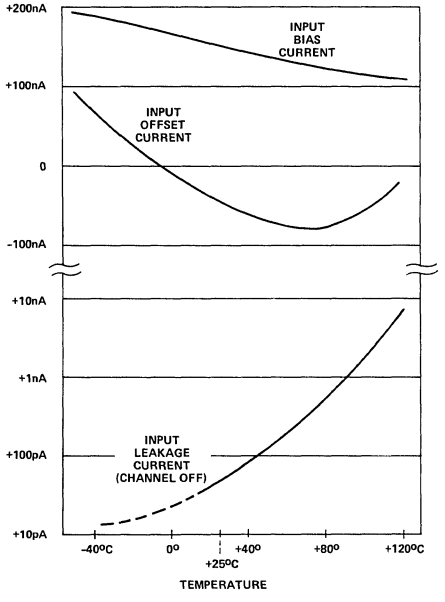


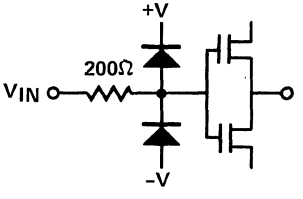
FIGURE 4

APPLYING THE HI-5900

GENERAL CONSIDERATIONS

The HI-5900 was designed to provide a versatile front-end section for a data acquisition system. Both hardwired and computer-controlled systems may be implemented in a variety of configurations. The following general considerations and precautions should be observed.

1. HANDLING – Each digital input is protected by a resistor-diode network, to minimize failures due to static discharge through the MOS gate:



For additional protection, it is wise to observe all of the proper shipping and handling procedures customary for CMOS devices.

2. POWER SUPPLY CONNECTIONS – Each of the four active chips in the HI-5900 are bypassed to ground by internal .01 μF capacitors. These eight nonpolarized capacitors prevent high frequency variations in the supply voltage.

   To bypass lower frequencies, connect a polarized capacitor from the ground pin to each supply pin, with value from 10μF to 50μF.

3. LAYOUT

   A. Distributed capacitance between signal paths external to the HI-5900 is a major source of crosstalk. Within the HI-5900, careful substrate design and packaging have ensured that "static" crosstalk will not exceed -80dB. ("Static") refers to the absence of channel-to-channel switching. Thus, a maximum of 2mV p-p can feed into a selected channel, from 20V p-p applied to one or more OFF channels.)

   When a multiplexer is continuously cycled from channel to channel, two other forms of crosstalk arise. These are dynamic crosstalk and adjacent* channel crosstalk, which are both minimized along with static crosstalk by careful attention to circuit board layout. A strip of ground plane should separate conductors for adjacent channels on a printed circuit board. See Fig. 5. Make these traces (and the conductors) short, and as narrow as practical for maximum separation.

   *Adjacent in time – for example, channels 1 and 8 may occupy adjacent time slots during time – division multiplexing.

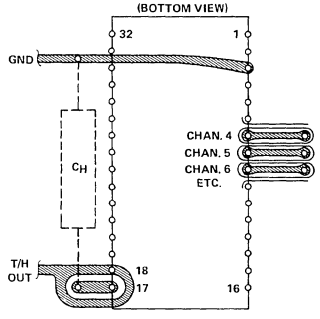


FIGURE 5
HI-5900 GUARD RING LAYOUT

   B. The holding capacitor C_H is the only essential external component required for operation of the HI-5900. The value selected determines droop rate, offset error and acquisition time according to curves shown in Fig. 3. Board layout should include a guard ring to prevent voltage-driven leakage at the capacitor terminal. See Fig. 5.

   For minimum droop error in the HOLD mode, choose a capacitor with high insulation resistance and low dielectric absorption. Since type of dielectric is the best performance indicator for hold capacitor applications, consider these guidelines: Teflon is best (especially at high temperature) but the most expensive. In descending order of choice, polystyrene, polypropylene, and polycarbonate are all acceptable. Least acceptable are ceramic and mica, which can allow several percent of change in the held voltage due to dielectric absorption (vs. .01% for the other types).

OFFSET ADJUSTMENT

The V_{REF} LOW input (pin 15) is a convenient point for nulling any DC offset voltage in an HI-5900 system. This can be done with a simple manual trim:

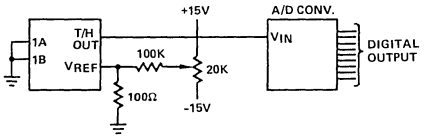


FIGURE 6

With zero volts on the selected input channel, the HI-5900 output (T/H OUT) may be adjusted to zero. If the system includes an A to D converter, net DC offset may be nulled by adjusting the converter's digital output to zero. In either case, readjustment is required after a change in temperature or a change in the HI-5900 gain. The need for readjustment may be eliminated by using an auto-zero circuit as shown in Fig. 7.

The offset at V_O is driven to zero by application of a voltage at V_{REF} LOW, opposite in sign and with magnitude (G + 1) V_O, where G is the digitally selected gain. This voltage is updated each time channel 8 is addressed. Since channel 8 is chosen for the zero (ground) reference input, the SN7420 decoder output is wired to go low only when channel 8 is addressed. The HA-2420 track/hold amplifier acquires a new sample of the offset at V_O during this interval. This sample is of opposite sign to V_O and approximately 100X (G + 1) in magnitude, due to the 10K/100Ω attenuator. Storing 100X the actual correction value minimizes the percent droop error during hold. Finally, OFFSET TRIM is used to remove any residual offset at V_O, introduced by the HA-2420.

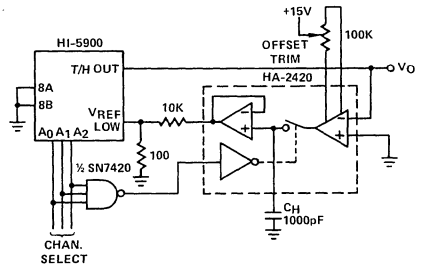


FIGURE 7

HARRIS

HI-5901

Analog Data Acquisition Signal Processor

FEATURES

- INPUT OVERVOLTAGE PROTECTION
- SOFTWARE CONTROLLED GAIN AND INPUT CHANNEL SELECTION
- 16 PSEUDO-DIFFERENTIAL/SINGLE ENDED INPUT CHANNELS
- GAINS OF 1, 2, 4 AND 8
- -90dB CROSSTALK
- 0.01% GAIN ERROR
- 9μs ACQUISITION TIME
- DROOP RATE: 5nV/μsec
- LOW POWER DISSIPATION 250mW
- COMPACT 32 PIN DIP
- MIL-STD-883 SCREENING AVAILABLE

APPLICATIONS

- MULTI-CHANNEL DATA ACQUISITION SYSTEMS
- STATUS MONITORING SYSTEMS
- PROCESS CONTROL SYSTEMS
- INSTRUMENTATION
- HIGH RELIABILITY DAS's

DESCRIPTION

The HI-5901 is a data acquisiton front end subsystem intended for multisensor based high-level applications, requiring conversion of analog input data to digital form for computer processing. It provides sixteen single-ended or pseudo-differential channels of fault-protected multiplexed inputs, programmable gains of 1, 2, 4, 8 and a buffered track and hold output block compatible with any commercially available A/D converter. All these functions are digitally selectable through appropriate coding of seven control terminals. Input channel expansion can be easily implemented through addition of external multiplexers and proper utilization of the enable-command pin.

Being self-contained units except for the holding capacitor, they facilitate user applications and eliminate the need for selection of high-priced precision resistors or labor intensive adjustments to achieve the accuracy levels specified.

This product provides channel to channel throughput rates of 50kHz at ±10 volt signal range when used in connection with a fast 12 bit A/D converter such as the HI-5712. In addition, it offers excellent input characteristics such as low input offset voltage with offset nulling capability, low input currents, very high input impedance, and very low crosstalk. Typical acquisition time and gain error are 9 microseconds and ±0.01%, respectively. The internal track and hold amplifier features aperture delay of 50ns, 10pC of charge transfer error, and a droop rate of 5nV/μsec. Total power dissipation is only 250mW.

A complete high-speed and high precision data acquisition system with 15 bits of dynamic range can be easily implemented with only three components: the HI-5901, the HI-5712, and an offset nulling DAC. Board space required is 3 square inches and total weight is less than 25 grams.

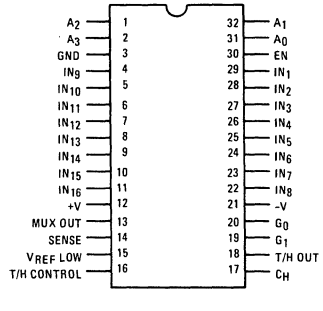
The manufacturing technique adopted for the HI-5901 involves monolithic dice packaged in leadless chip carriers (LCC's) and soldered to both sides of a multilayer ceramic substrate. The resulting product is a compact and easy-to-use 32 pin DIP.

The HI-5901 is intended for military, aerospace, industrial and instrumentation applications. MIL-STD-883 Class B and high reliability commercial grades are both available as standard products.

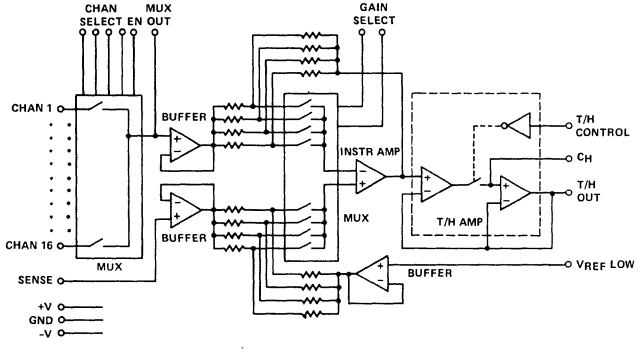
PINOUT

TOP VIEW

Section 11 for Packaging



FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V- Terminals 40V

Digital Input Overvoltage (Multiplexers)

V_{Supply} (+) +4V

V_{Supply} (-) -4V

Analog Input Overvoltage

V_{Supply} (+) +20V

V_{Supply} (-) -20V

Output Current Short Circuit Protected

Operating Temperature Range

HA-5901-5, -7 $0^oC \leq T_A \leq +75^oC$

HA-5901-2, -8 $-55^oC \leq T_A \leq +125^oC$

Storage Temperature Range $-65^oC \leq T_A \leq +150^oC$

Internal Power Dissipation 650mW

T/H Control Input +8, -15V

ELECTRICAL CHARACTERISTICS Unless otherwise specified: $V_S = \pm 15V$; $C_H = 1000pF$; $V_{IH} = 4.0V$; $V_{IL} = 0.8V$

		HI-5901-2, -8 -55°C to +125°C			HI-5901-5, -7 0°C to +70°C			
PARAMETER	TEMP	MIN	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG INPUT CHAR., EACH CHANNEL								
Offset Voltage	+25°C		2	7.5		3	10.5	mV
	Full			9.5			13	mV
Bias Current	+25°C		80	300		80	300	nA
	Full		90	600		80	600	nA
Offset Current	+25°C		15	150		20	150	nA
	Full		30	300		30	300	nA
Common Mode Range	Full	±10			±10			V
Common Mode Rejection Ratio ($V_{CM} = \pm 10V$) Any Gain	Full	80	85		74	85		dB
DIGITAL INPUT CHAR.								
Multiplexer Digital Input Current (High or Low)	Full		0.5	1		0.5	1	μA
Track/Hold Digital Input Current								
$V_{IN} \leq 0.8V$	Full			0.8			0.8	mA
$V_{IN} \geq 4.0V$	Full			20			20	μA
TRANSFER CHARACTERISTICS								
Small Signal Bandwidth (Gain = 1)	+25°C		2			2		MHz
Full Power Bandwidth (Gain = 1, $V_O = \pm 10V$)	+25°C		70			70		kHz
Crosstalk (Sample Mode, Gain = 8, 1kHz 20VP -P Input on all but Selected Channel)	+25°C	-80	-90		-80	-90		dB
"Off Isolation (Hold Mode, Gain = 1, 1kHz 20V P-P Input)	+25°C		-76			-76		dB
Acquisition Time (Note 2), to 0.01%	+25°C		9			9		μs
Gain - Absolute Error								
Gain Of 1, 2,	Full		0.01	0.1		0.01	0.2	%
4, 8			0.01	0.2		0.01	0.2	%
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10			±10			V
Output Current	+25°C	±10			±10			mA
Output Resistance	+25°C		5			5		Ω
DYNAMIC CHARACTERISTICS								
t_{ON}, Enable (MUX)	+25°C		300			300		ns
t_{OFF}, Enable (MUX)	+25°C		300			300		ns
Slew Rate	+25°C		±4			±4		V/μs
Droop Rate (T/H)	+25°C		5			5		nV/μs
	Full			20			5	μV/μs
Charge Transfer (T/H)	25°C		10			10		pC
Aperture Delay (T/H)	+25°C		50			50		ns
Aperture Uncertainty (T/H)	+25°C		5			5		ns
POWER SUPPLY CHARACTERISTICS								
I_+	+25°C			13			13	mA
	Full		8.5	15		8.0	15	mA
I_-	+25°C			13			13	mA
	Full		6.5	15		6.0	15	mA
Power Supply Rejection Ratio, V+	Full	76	90		70	90		dB
Power Supply Rejection Ratio, V-	Full	80	100		80	100		dB

NOTES. 1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

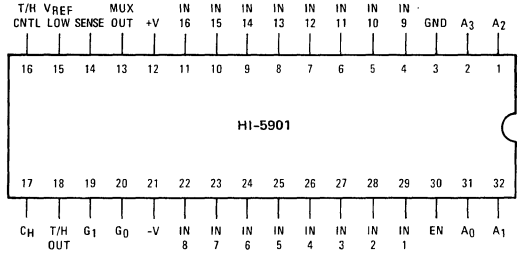
2. Acquisition Time is defined for a change of channel (+10V on chan. 1 to 0V on chan.16) with simultaneous change from HOLD to TRACK mode. Gain = 1.

PIN FUNCTIONS AND DESCRIPTION

PIN	SYMBOL	DESCRIPTION
4	IN_9	16 Single Ended Input Channels. The Signals Applied to these Input Channels are Inverted at the Output of HI-5901
5	IN_{10}	
6	IN_{11}	
7	IN_{12}	
8	IN_{13}	
9	IN_{14}	
10	IN_{15}	
11	IN_{16}	
29	IN_1	
28	IN_2	
27	IN_3	
26	IN_4	
25	IN_5	
24	IN_6	
23	IN_7	
22	IN_8	
31	A_0	Digital Channel Select Inputs*
32	A_1	
1	A_2	
2	A_3	

PIN	SYMBOL	DESCRIPTION
20	G_0	Digital Gain Select Inputs*
19	G_1	
16	T/H CONTROL	Track/Hold Mode Select*
3	GND	Signal and Power Ground
12	+V	Positive Supply (+15V)
21	-V	Negative Supply (-15V)
18	T/H OUT	Output of the HI-5901
17	C_H	Hold Capacitor Connection
15	$V_{REF}LOW$	Reference for the Output on Pin 18
13	MUX OUT	Input Multiplexer Output
14	SENSE	Analog Signal Return
30	EN	Enable Strobe for the Input Multiplexer; Normally Forced High. EN may be used in Conjunction with MUX OUT and SENSE, to Poll Additional Channels through an External Multiplexer

*See Programmable Functions



PROGRAMMABLE FUNCTIONS

Input Codes are as follows:

X = DON'T CARE
0 = $V_{IN} \leq +0.8V$
1 = $V_{IN} \geq +4.0V$, where V_{IN} is the digital input voltage

1. T/H CONTROL (Pin 16)

0	TRACK
1	HOLD

2. GAIN SELECT

G_1 (Pin 19)	G_0 (Pin 20)	GAIN
0	0	1
0	1	2
1	0	4
1	1	8

3. CHANNEL SELECT

A_3 (Pin 2)	A_2 (Pin 1)	A_1 (Pin 32)	A_0 (Pin 31)	EN (Pin 30)	CHANNEL
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

PERFORMANCE CURVES

ACQUISITION TIME vs. OUTPUT STEP CHANGE

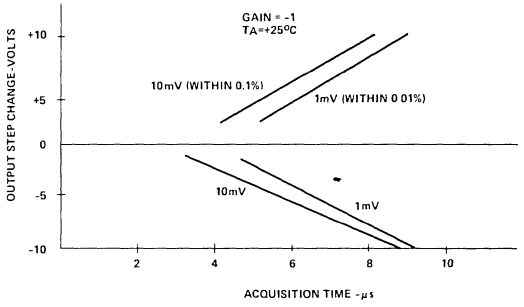


FIGURE 1

INPUT NOISE VOLTAGE vs. FREQUENCY

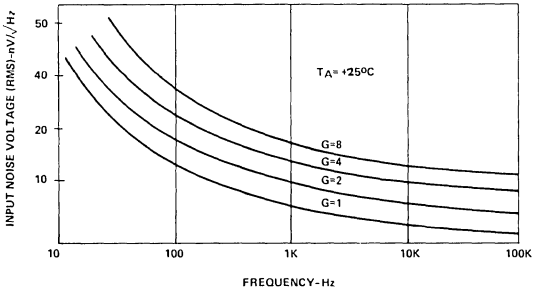


FIGURE 2

TYPICAL T/H AMPLIFIER PERFORMANCE vs. HOLD CAPACITANCE Ch

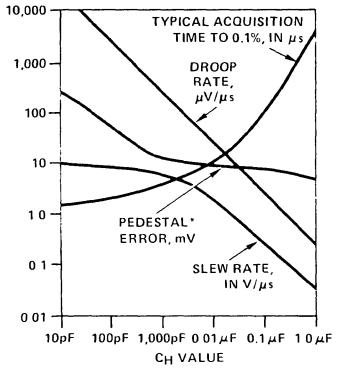


FIGURE 3

INPUT LEAKAGE, BIAS & OFFSET CURRENT vs. TEMPERATURE

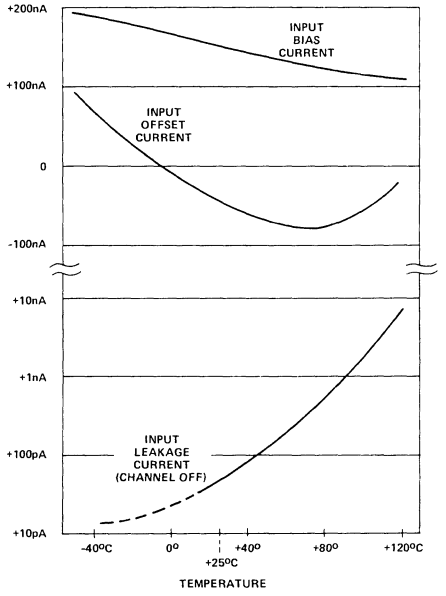


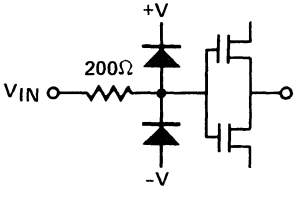
FIGURE 4

APPLYING THE HI-5901

GENERAL CONSIDERATIONS

The HI-5901 was designed to provide a versatile front-end section for a data acquisition system. Both hardwired and computer-controlled systems may be implemented in a variety of configurations. The following general considerations and precautions should be observed.

1. HANDLING – Each digital input is protected by a resistor-diode network, to minimize failures due to static discharge through the MOS gate:



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For additional protection, it is wise to observe all of the proper shipping and handling procedures customary for CMOS devices.

2. POWER SUPPLY CONNECTIONS – Each of the four active chips in the HI-5901 are bypassed to ground by internal .01 μF capacitors. These eight nonpolarized capacitors prevent high frequency variations in the supply voltage.

   To bypass lower frequencies, connect a polarized capacitor from the ground pin to each supply pin, with value from 10μF to 50μF.

3. LAYOUT

   A. Distributed capacitance between signal paths external to the HI-5901 is a major source of crosstalk. Within the HI-5901, careful substrate design and packaging have ensured that "static" crosstalk will not exceed -80dB. ("Static") refers to the absence of channel-to-channel switching. Thus, a maximum of 2mV p-p can feed into a selected channel, from 20V p-p applied to one or more OFF channels.)

   When a multiplexer is continuously cycled from channel to channel, two other forms of crosstalk arise. These are dynamic crosstalk and adjacent* channel crosstalk, which are both minimized along with static crosstalk by careful attention to circuit board layout. A strip of ground plane should separate conductors for adjacent channels on a printed circuit board. See Fig. 5. Make these traces (and the conductors) short, and as narrow as practical for maximum separation.

   *Adjacent in time – for example, channels 1 and 16 may occupy adjacent time slots during time – division multiplexing.

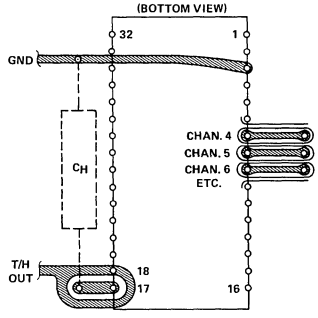


FIGURE 5
HI-5901 GUARD RING LAYOUT

   B. The holding capacitor C_H is the only essential external component required for operation of the HI-5901. The value selected determines droop rate, offset error and acquisition time according to curves shown in Fig. 3. Board layout should include a guard ring to prevent voltage-driven leakage at the capacitor terminal. See Fig. 5.

   For minimum droop error in the HOLD mode, choose a capacitor with high insulation resistance and low dielectric absorption. Since type of dielectric is the best performance indicator for hold capacitor applications, consider these guidelines: Teflon is best (especially at high temperature) but the most expensive. In descending order of choice, polystyrene, polypropylene, and polycarbonate are all acceptable. Least acceptable are ceramic and mica, which can allow several percent of change in the held voltage due to dielectric absorption (vs. .01% for the other types).

OFFSET ADJUSTMENT

The V_{REF} LOW input (pin 15) is a convenient point for nulling any DC offset voltage in an HI-5901 system. This can be done with a simple manual trim:

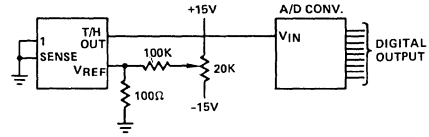


FIGURE 6

With zero volts on the selected input channel, the HI-5901 output (T/H OUT) may be adjusted to zero. If the system includes an A to D converter, net DC offset may be nulled by adjusting the converter's digital output to zero. In either case, readjustment is required after a change in temperature or a change in the HI-5901 gain. The need for readjustment may be eliminated by using an auto-zero circuit as shown in Fig. 7.

The offset at V_O is driven to zero by application of a voltage at V_{REF} LOW, opposite in sign and with magnitude (G + 1) V_O, where G is the digitally selected gain. This voltage is updated each time channel 16 is addressed. Since channel 16 is chosen for the zero (ground) reference input, the SN7420 decoder output is wired to go low only when channel 16 is addressed. The HA-2420 track/hold amplifier acquires a new sample of the offset at V_O during this interval. This sample is of opposite sign to V_O and approximately 100X (G + 1) in magnitude, due to the 10K/100Ω attenuator. Storing 100X the actual correction value minimizes the percent droop error during hold. Finally, OFFSET TRIM is used to remove any residual offset at V_O, introduced by the HA-2420.

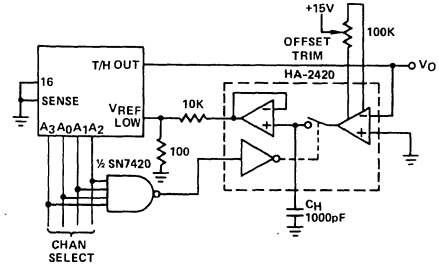


FIGURE 7

TIMING AND CONTROL

The HI-5901 is intended to operate with a fast A to D converter such as HARRIS' 12 bit HI-5712. A single monostable (one-shot) multivibrator such as half of the dual SN74123 provides the necessary timing and control:

The pulse rate at $\overline{Q}$ is equal to the conversion rate of the A to D converter, since the one-shot is driven by the converter's STATUS output. Polarity of the Q output is correct for initiating a conversion each time the HI-5901 returns to the HOLD mode. For maximum channel-to-channel throughput rate, the $\overline{Q}$ pulse duration (determined by R and C) may be set equal to the HI-5901 acquisition time.

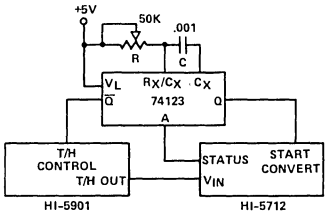


FIGURE 8

HI-7541

12 Bit Multiplying Monolithic Digital-to-Analog Converter

FEATURES

- FULL FOUR QUADRANT MULTIPLICATION
- .01% RELATIVE ACCURACY OVER TEMPERATURE
- LOW OUTPUT CAPACITANCE 100pF MAX
- TTL/CMOS COMPATIBLE
- MONOLITHIC CONSTRUCTION
- VERY LOW OUTPUT LEAKAGE CURRENT ±100nA MAX
- LOW GAIN ERROR 0.1%

APPLICATIONS

- PROGRAMMABLE GAIN AMPLIFIERS
- PROGRAMMABLE FUNCTION GENERATION

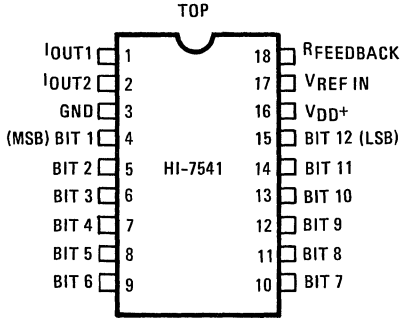
DESCRIPTION

The Harris HI-7541 is a 12-Bit Monolithic Digital to Analog converter, offering full four quadrant multiplying capability. The chip features dielectrically isolated CMOS technology to assure fast settling time and freedom from latch-up. Included are thin film ladder and applications resistors, laser trimmed for accuracy over the full operating temperature range.

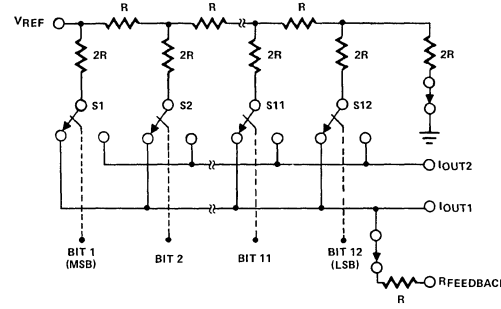
The HI-7541 is recommended as a high performance direct replacement for the AD7541 device. It operates on a single +15V supply and is available in an 18-pin ceramic package as well as in dice form. Screening to MIL-STD-883 method 5004 class B is available.

PINOUT

Section 11 for Packaging



FUNCTIONAL DIAGRAM



DIGITAL INPUTS (DTL, TTL, CMOS COMPATIBLE)
LOGIC: A SWITCH IS CLOSED TO I_{OUT1} FOR ITS DIGITAL INPUT IN A HIGH (LOGIC 1) STATE.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)1

Power Supply Inputs V_{DD}	+17V
Reference Inputs VREF (Hi)	±25V
Digital Input Range Bits 1-12	V_{DD} to GND
Output Voltage (Pins 1 and 2)	-100mV to V_{DD}

Power Dissipation (Package) up to +75°C Derate above +75°C by 6mW/°C.	450mW
Operating Temperature Range	
HI-7541SD/TD/SO	-55°C to +125°C
HI-7541AD/BD	-25°C to +85°C
HI-7541JN/KN/JO	0°C to +75°C
HI-7541SD/883 AND TD/883.	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@25°C, V_{DD} = +15V, V_{REF} = +10V Unless otherwise noted)

PARAMETER	CONDITIONS	HI-7541KN/BD/TD MIN	HI-7541KN/BD/TD TYP	HI-7541KN/BD/TD MAX	HI-7541JN/AD/SD/JO/SO MIN	HI-7541JN/AD/SD/JO/SO TYP	HI-7541JN/AD/SD/JO/SO MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs	Bit ON = "Logic 1" Bit OFF = " Logic 0"							
Input Voltage								
Logic 1, V_{AH}		2.4			2.4			V
Logic 0, V_{AL}				0.8			0.8	V
Input Current								
Logic 1	V_{IN}=15V			1			1	µA
Logic 0	V_{IN}=0V			-1			-1	µA
Reference Input								
Input Resistance		7	9	12	7	9	12	KΩ
Input Voltage		-10		+10	-10		+10	V
TRANSFER CHARACTERISTICS								
Resolution	Over Full Temp. Range	12			12			Bits
Integral (2) Nonlinearity	@+25°C			±.01			±.02	%FSR
	Over Full Temp Range							
Differential (2) Nonlinearity	@ +25°C			±.01			±.02	%FSR
	Over Full Temp Range							
Gain Error (2)	@ +25°C			±0.1			±0.2	
	Over Full Temp. Range			±0.15			±0.25	%FSR
Gain Tempco (2)(5)	Over Full Temp. Range			±5			±5	PPM/°C
Settling Time (2) (5) to +1/2 LSB				1			1	µs
PSRR (2)	14.5V≤V_{DD}≤15.5V;25°C			±.01			±.01	%FSR/
	Over Full Temp. Range			±.02			±.02	%ΔV_{DD}
OUTPUT CHARACTERISTICS								
Output (2) Leakage Current	V_{REF} = ±10V @ +25°C			±50			±50	nA
	Over Full Temp. Range			±100			±100	nA
Capacitance (2) (5)				100			100	pF
Feed Through (2)(5)	V_{REF} = 20 V_{pp} @ 10kHz			±1			±1	mVpp
POWER REQUIREMENTS								
V_{DD}	(See Fig. 6, 8, & 9)	+5	+15	+16	+5	+15	+16	V
I_{DD} (3)				2			2	mA

5

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. See Definitions.
3. After 30 seconds warm-up.
4. Specification's subject to change without notice.
5. Guaranteed by design, not tested.

DEFINITIONS OF SPECIFICATIONS

ACCURACY

INTEGRAL NONLINEARITY-Integral Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line drawn between zero (all bit OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY-For a D/A converter, it is the difference between the actual output change and the ideal (1LSB) change for a one bit change in code. A Differential Nonlinearity of +1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

FEEDTHROUGH ERROR

Variation in V_{OUT} due to variation in V_{REF}, for the condition all bits OFF (zero output current).

GAIN

The gain is defined only when the MDAC is used with an output operational amplifier in which case it is V_{OUT}/V_{REF}.

POWER SUPPLY REJECTION RATIO (PSRR)

Variation in V_{OUT} due to variation in V_{DD} expressed in %FSR/% V_{ps}.

OUTPUT CAPACITANCE

Measured capacity from I_{OUT1} or I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT

Current leakage to ground from I_{OUT1} (all bits low) or I_{OUT2} (all bits high) with no connection to the span resistor (Pin 18).

OPERATING INSTRUCTIONS

BYPASSING AND GROUNDING

For best accuracy and high frequency performance the grounding and bypass scheme shown in Figure 1 should be used. Bypass capacitors should be connected close to the HI-7541 (preferably to the device pins) and should be tantalum in parallel with a smaller ceramic type for best high frequency noise rejection.

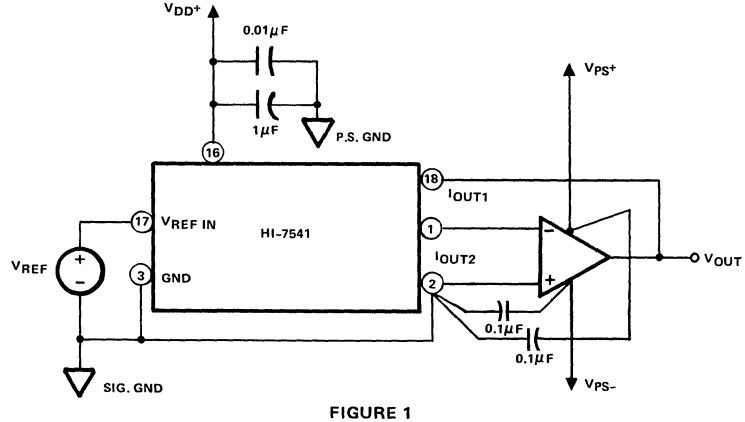


FIGURE 1

UNIPOLAR BINARY OPERATION

For most applications the HI-7541 requires an output operational amplifier, since both I_{OUT1} and I_{OUT2} should remain at ground potential to avoid linearity errors. Figure 2 shows the connections for unipolar straight binary operation. A schottky diode limits the negative excursions of voltage on I_{OUT}.

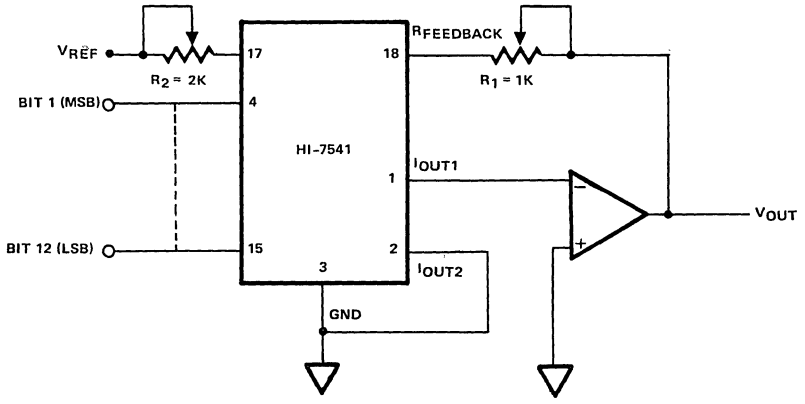


FIGURE 2

CODE TABLE- UNIPOLAR OPERATION

DIGITAL INPUT												NOMINAL ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1	$-V_{REF}(1-2^{-12})$
1	0	0	0	0	0	0	0	0	0	0	1	$-V_{REF}(1/2+2^{-12})$
1	0	0	0	0	0	0	0	0	0	0	0	$-V_{REF}/2$
0	1	1	1	1	1	1	1	1	1	1	1	$-V_{REF}(1/2-2^{-12})$
0	0	0	0	0	0	0	0	0	0	0	1	$-V_{REF}(2^{-12})$
0	0	0	0	0	0	0	0	0	0	0	0	0

CODE TABLE - BIPOLAR (OFFSET) OPERATION

DIGITAL INPUT												NOMINAL ANALOG OUTPUT
1	1	1	1	1	1	1	1	1	1	1	1	$-V_{REF}(1-2^{-11})$
1	0	0	0	0	0	0	0	0	0	0	1	$-V_{REF}(2^{-11})$
1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	1	1	1	1	$V_{REF}(2^{-11})$
0	0	0	0	0	0	0	0	0	0	0	1	$V_{REF}(1-2^{-11})$
0	0	0	0	0	0	0	0	0	0	0	0	V_{REF}

BIPOLAR (4-QUADRANT) BINARY OPERATION

Figure 3 shows the configuration for bipolar offset binary coded operation. The analog output will be the product of V_{REF} and the values given above.

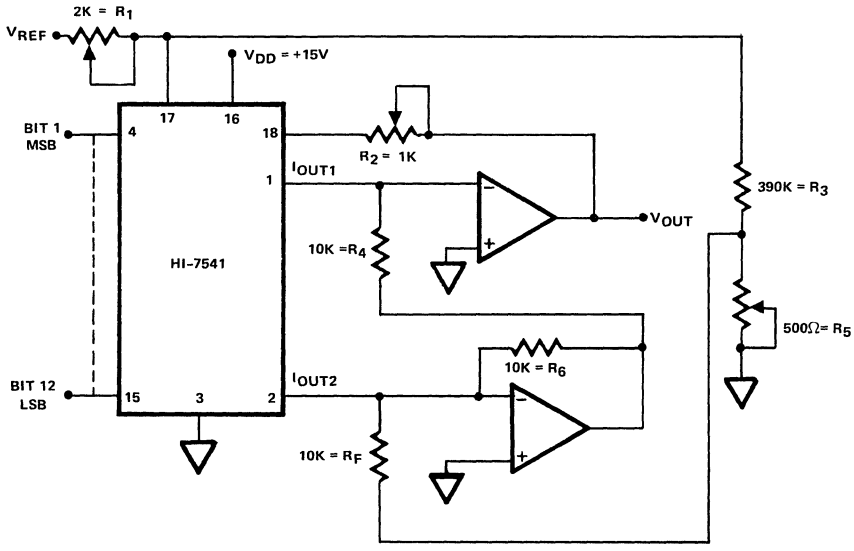


FIGURE 3

OFFSET AND GAIN CALIBRATION

UNIPOLAR CALIBRATION	
Step 1:	Unipolar Zero Offset Adjustment • Turn all bits OFF (00...00) • Adjust offset trimpot on the output operational amplifier to 0V ± 1mV at V_{OUT}
Step 2:	Unipolar Gain Adjustment • Turn all bits ON (11...11) • Adjust R_1 and R_2 for an output of $V_{OUT} = -V_{REF}(1-2^{-12})$
BIPOLAR CALIBRATION	
Step 1:	Bipolar Offset Adjustment • Set $V_{REF} = +10V$ • Turn MSB ON, all other bits OFF (1000...00) • Adjust R_4 so that $V_{OUT} = 0V$
Step 2:	Bipolar Gain Adjustment • Set $V_{REF} = +10V$ • Turn all bits off (00...00) • Adjust R_1 and R_2 so that $V_{OUT} = V_{REF}$

SELECTING AN OPERATIONAL AMPLIFIER

The outputs I_{OUT1} and I_{OUT2} must remain very close to ground potential for the HI-7541 to maintain its accuracy. Because of this constraint, most applications require selection of a suitable output op-amp. Harris Analog Products Division offers a wide range of high performance op-amps which are well suited to a variety of applications.

COMPENSATION

In the standard configurations of Figures 1 and 2 the output capacitance of the MDAC along with the feedback resistance introduces a pole in the open loop response of the system. This pole may cause undesirable phase shift leading to excessive ringing or even oscillation. The phase shift may be compensated by placing a capacitor in the feedback loop. Figure 3 shows this scheme. The compensation is exact for $R_oC_o = R_{FB}C_{FB}$. This is a special case, however, since both Ro and Co are dependent on the digital code for a CMOS MDAC.

A practical approach is to turn all bits of the MDAC ON while applying a square wave of appropriate magnitude to the reference input. Then select a feedback capacitor which gives approximately 20% of overshoot, which is equal to a 45° Phase Margin. This form of compensation reduces the overall bandwidth of the system, which is dependent on the op amp selected.

MDAC EQUIVALENT CIRCUIT WITH COMPENSATION

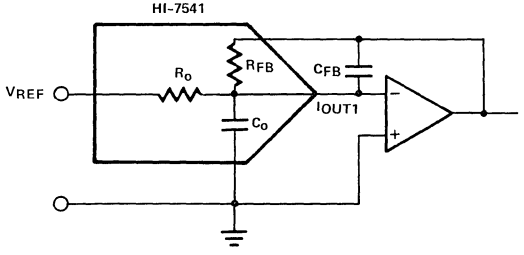


FIGURE 4

OP AMP PARAMETERS

The addition of the output amplifier has a direct effect on many of the MDAC parameters, including bandwidth, settling time, accuracy and tempco. Settling time is difficult to measure for the HI-7541 since the current outputs have almost no voltage compliance. The output settling time of the MDAC-OP AMP system can be measured; and if the settling time of the Op Amp itself is known, that of the MDAC can be estimated by the Root-Sum of Squares method;

$$T_{MDAC}\sqrt{T^2\,(MDAC + AMP) - T^2\,AMP}$$

The bandwidth of the MDAC itself can be approximated by modeling it as a voltage source (V_{ref}) followed by a series resistance Ro) and capacitance (Co) as in figure 3. The half-power frequency then is;

$$f = \frac{1}{2\pi RoCo}$$

If R_0 = 10KΩ and C_0 = 50pf then f = 318KHz. However, an output amplifier virtually eliminates C_0 by maintaining zero volts across it, thus extending the DAC/amplifier bandwidth almost to that of the amplifier alone.

TABLE 1 HARRIS OP AMPS (TYPICAL AT T_A = +25°C)

Op Amp HA-	Full Power B.W.	Offset Voltage	Offset Voltage Drift	Bias Current	C_{FB}* Compensation for 45° P.M.	Settling Time**
2600	75KHz	500μV	5μV/oC	1nA	20pf	1.5μs
2525	1.6MHz	5mV	30μV/°C	125nA	12pf	200ns
5100	150KHz	500μV	5μV/°C	20pA	18pf	1.7μs
5130	600KHz	100μV	1μV/°C	1nA	30pf	11μs
5190	6.5MHz	3mV	20μV/°C	5μA	2pf	70ns

* For standard configuration such as Figure 3. Vref equals 1KHz 10V peak to peak square wave.

** For the Op Amp alone. A_{VCL} = -1, 10V step to 0.1%.

OFFSET

The offset of the Op Amp can be adjusted to zero using either the op amp offset terminals or the scheme of Figure 4. A more important parameter is offset drift over temperature. For instance a 30 V/°C offset drift spec will lead to an error over a 75°C temperature span (0°C to +75°C) of almost 1 LSB for a 10V Full Scale output.

EXTERNAL OFFSET ADJUST AND SCHOTTKY PROTECTION

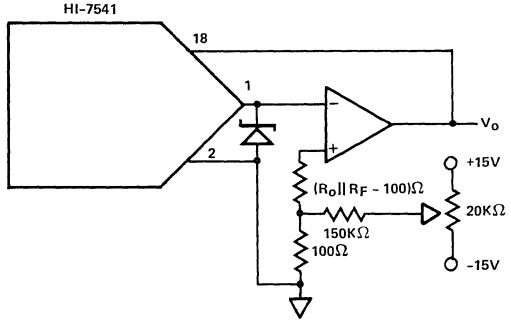


FIGURE 5

BIAS CURRENTS

Bias currents can also introduce errors but there are many Op Amps on the market which require negligible bias current. Examples of these are the HA-2600 and HA-5100.

DIODE PROTECTION

Some high speed Op Amps present a low impedance between the inverting input and the negative supply terminal during power up. In these instances a schottky diode should be placed as in Figure 4.

PERFORMANCE CURVES

LINEARITY ERROR VS. SUPPLY VOLTAGE

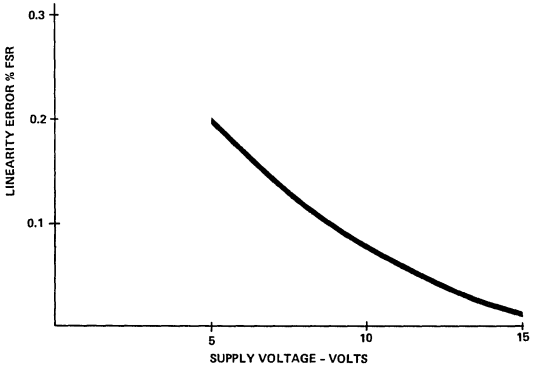


FIGURE 6

FEEDTHROUGH ERROR VS. FREQUENCY

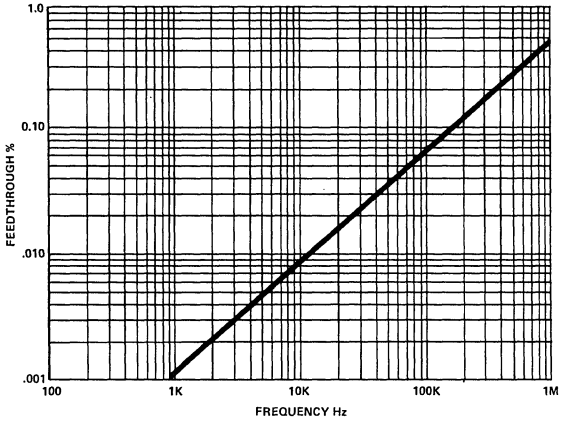


FIGURE 7

GAIN ERROR VS. SUPPLY VOLTAGE

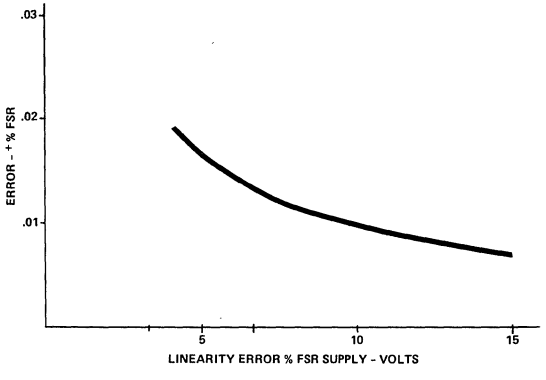


FIGURE 8

SUPPLY CURRENT VS. SUPPLY VOLTAGE

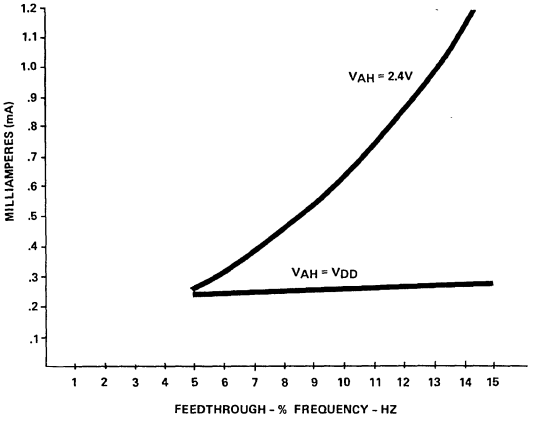


FIGURE 9

HARRIS

HI-DAC 80I

12-Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- DAC 80 CONFIGURATION
- MONOLITHIC CONSTRUCTION
- FAST SETTLING 260ns (TYP) TO 0.01%
- GUARANTEED MONOTONIC 0°C TO 75°C
- WAFER LASER TRIMMED
- APPLICATION RESISTORS ON CHIP
- ACCEPTS 6.2V OR 10.24V REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING

APPLICATIONS

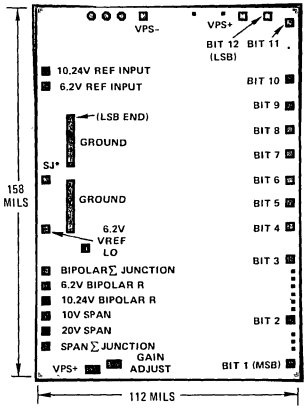
- HYBRID DAC 80 BY ADDING REFERENCE
- HIGH SPEED, SUCCESSIVE APPROXIMATION TYPE ADC'S
- HYBRID DATA ACQUISITION SYSTEMS

DESCRIPTION

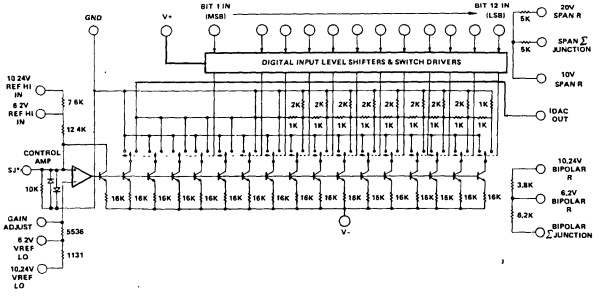
The Harris HI-DAC 80I is a 12-bit, monolithic digital to analog converter. Available in dice form, it is suitable as a component in hybrid or compound monolithic circuits. The HI-DAC 80I is a current output device, and the addition of a precision voltage reference makes it the functional equivalent of the popular DAC 80CBI-I. Two versions are available–DAC 80I-A, laser trimmed to accept a +6.2V reference; and DAC 80I-B, laser trimmed to accept a +10.24V reference. Both versions are guaranteed monotonic over the 0°C to 75°C temperature range. Digital input code may be complementary binary, complementary offset binary, or complementary two's complement binary logic.

Fast output current settling of 260ns is achieved using Dielectric Isolation (DI) processing to reduce internal parasitics. The speed of the HI-DAC 80I combined with its guaranteed monotonicity and maximum 1/2 LSB linearity error (@+25°C) make it an ideal choice for high speed successive approximation analog-to-digital converters. Laser trimmed application resistors are provided on-chip for use with an external output amplifier. They allow bipolar operation as well as +5V, +10V and +20V output ranges.

PAD CONFIGURATION/CHIP



FUNCTIONAL DIAGRAM



* A Summing Junction (normally an inverting input) is formed at the control amplifier's noninverting input, since the amplifier's feedback is inverted by an external transistor.

5

ABSOLUTE MAXIMUM RATINGS (Referred to Ground) (Note 1).

Power Supply Inputs	V_{ps+}	+18V	Operating Temperature Range	-55°C to +125°C
	V_{ps-}	-18V		
Reference Inputs	V_{REF} (Hi)	$+V_{ps}$	Storage Temperature Range	-65°C to +150°C
Digital Inputs	Bits 1-12	0V TO +10V		

ELECTRICAL CHARACTERISTICS (Note 5)

(@ +25°C, V_{ps+} = +15V, V_{ps-} = -15V, V_{REF} = 6.2V, Unless otherwise noted)

PARAMETER	CONDITION	HI-DAC 80I MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Digital Inputs (TTL Compatible)					
Input Voltage	Bit ON = "Logic 0"				
Logic "1"	Bit OFF = "Logic 1"	2.0			V
Logic "0"				0.8	V
Input Current					
Logic "1"				10	μA
Logic "0"	Guaranteed, not tested			-100	μA
Reference Inputs (Note 2)					
Input Voltage					
HI-DAC 80I-A			6.2		V
HI-DAC 80I-B			10.24		V
Input Resistance					
HI-DAC 80I-A			12.4K		Ω
HI-DAC 80I-B			20K		Ω
TRANSFER CHARACTERISTICS					
Resolution				12	Bits
Linearity (Note 2)					
Integral				±½	LSB
Differential				±½	LSB
Monotonicity	0°C to +75°C GUARANTEED				
Offset (Note 5)	All bits OFF				
Unipolar			0.005	0.01	% FSR
Bipolar				0.1	% FSR
Gain Error	All bits OFF		0.05	0.1	% FSR
Temperature Stability					
Offset Drift (Note 2)	All bits OFF				
Unipolar			0.2		ppm FSR/°C
Bipolar			2		
Differential Nonlinearity (Note 2)			0.5		
Gain Drift (Note 2)	All bits ON		2		
Settling Time (Note 2), ± 1/2 LSB	All bits ON to OFF or OFF to ON		260	400	ns

PARAMETER	CONDITION	HI-DAC 80I			
		MIN	TYP	MAX	UNITS
Power Supply Sensitivity (Note 2)					
Offset					
Unipolar					
$+V_{ps}$	$-V_{ps}$ = -15V			0.05	% FSR/
$-V_{ps}$	$+V_{ps}$ = +15V			0.05	$\%\Delta V_{ps}$
Bipolar					
$+V_{ps}$	$-V_{ps}$ = -15V			0.05	
$-V_{ps}$	$+V_{ps}$ = +15V			0.05	
Gain					
$+V_{ps}$	$-V_{ps}$ = -15V			10	
$-V_{ps}$	$+V_{ps}$ = +15V			10	
OUTPUT CHARACTERISTICS					
Output Current					
Unipolar		1.6	2	2.4	mA
Bipolar		±0.8	± 1	± 1.2	mA
Output Resistance	Not including	1.6	2	2.4	KΩ
Output Capacitance	Feedback Resistor			10	pF
Compliance Limit (Note 2)		-3		+10	V
Glitch (Note 2)			1600		mV-ns
POWER SUPPLY REQUIREMENTS					
$V_{ps}+$		4.5	15	16.5	V
$V_{ps}-$		-16.5	-15	-11.4	V
$I_{ps}+$ (Note 4)			5		mA
$I_{ps}-$ (Note 4)			-10		mA

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. See Definitions.
3. FSR is "full scale range" and is 2mA (±20%) for current output.
4. After 30 seconds warm-up.
5. Parameters may vary according to die bonding scheme used. See recommended bonding diagram.

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-DAC 80I accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	Complementary Binary	Complementary Offset Binary	Complementary Two's Complement*
MSB LSB			
000...000	+Full Scale	+Full Scale	-LSB
100...000	Mid Scale-1LSB	-1LSB	+Full Scale
111...111	Zero	-Full Scale	Zero
011...111	+½ Full Scale	Zero	-Full Scale

*Invert MSB with external inverter to obtain CTC Coding

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

DEFINITIONS OF SPECIFICATIONS (Continued)

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H-25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of fullscale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

OPERATING INSTRUCTIONS

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BONDING AND GROUNDING

In order to ensure proper operation of the HI-DAC 80I, care must be taken to bond it correctly. Primary in these considerations is the selection of a grounding scheme. The best approach is to distinguish between a general power ground and a reference, or precision ground. Figure 1 shows the recommended connections in a system using an operational amplifier (such as the Harris HA-2600) to achieve voltage output. Notice that a ground plane extends along the chip, and all currents on the device flow through this plane. Any errors which arise along this plane are most significant at the MSB end. It is best then to choose this end as the reference point for the output. The opposite, or LSB end of the plane, is bonded to the general system or power ground. Varying currents through this point will give rise to voltages above those defined as reference; however, the only current flowing into precision ground is the constant current drawn by the reference plus the negligible bias current of the op-amp. Remember that the magnitude of the reference current changes when switching from unipolar to bipolar operation and requires readjustment of offset and gain. The finite resistance of the bond wires themselves introduce an error at both ends of the ground plane, and this effect is reduced by double bonding of the ground pads. For effective bypassing tie the bypass capacitors close to the pads of the chip.

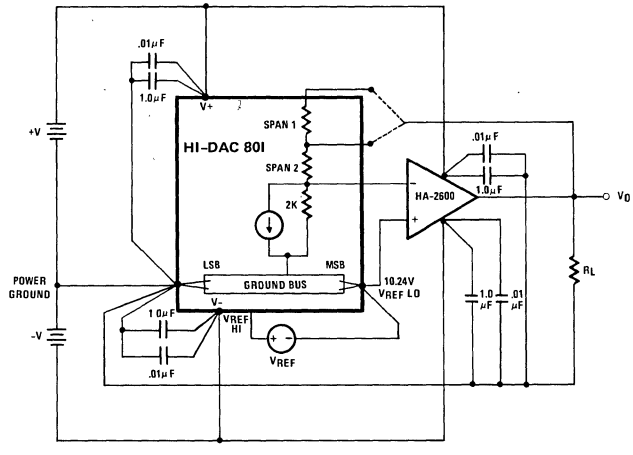
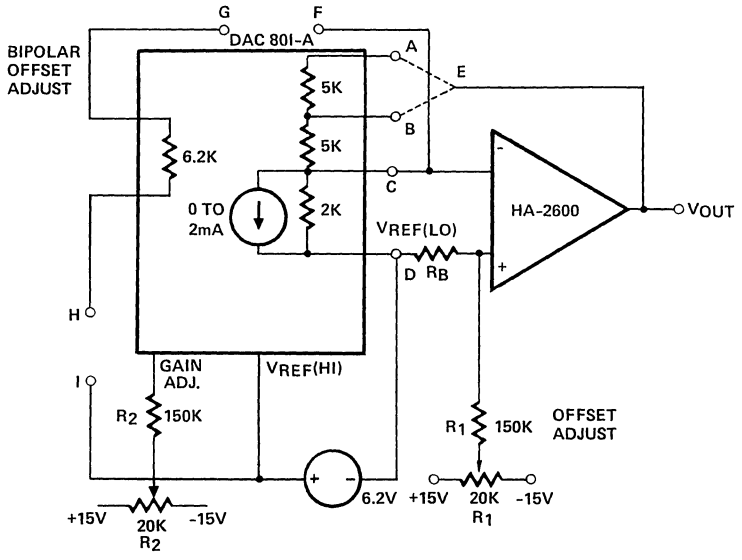


FIGURE 1. SYSTEM GROUNDING AND SUPPLY BYPASSING

OFFSET GAIN ADJUSTMENT

The offset and gain of the HI-DAC 80I may be externally adjusted via potentiometers. With the device mounted in a suitable package (see Packaging the HI-DAC 80I) connect the potentiometers as indicated in Figure 2.



	OUTPUT RANGE	CONNECTIONS	BIAS RESISTOR (R_B)
UNIPOLAR MODE	0 TO +10V 0 TO +5V	B TO E ; B TO E ; A TO C	1.43KΩ 1.11KΩ
BIPOLAR MODE	±10V ±5V 2.5V	F TO G ; H TO I ; A TO E F TO G ; H TO I ; B TO E F TO G ; H TO I ; B TO E A TO C	1.31K Ω 1.16KΩ .94KΩ

FIGURE 2. OFFSET GAIN ADJUSTMENT

UNIPOLAR CALIBRATION

Step 1: Unipolar Offset
- Turn all bits OFF
- Adjust R_1 for zero volts output

Step 2: Gain
- Turn all Bits ON
- Adjust R2 for an output of FS-1 LSB
- That is, adjust for:
- 9.9976V for 0V to +10V Range
- 4.9988V for 0V to +5V Range

BIPOLAR CALIBRATION

Step 1: Bipolar Offset
- Turn all bits OFF
- Adjust R1 for an output of:
- -10V for ±10V Range
- -5V for ±5V Range
- -2.5V for ±2.5V Range

Step 2: Gain
- Turn Bit 1 (MSB) ON; all other bits OFF
- Adjust R2 for zero volts output

HARRIS

HA-5320

High Speed Precision Monolithic Sample and Hold Amplifier

ADVANCE

FEATURES

- ACQUISITION TIME — 1.5μs (0.01%)
- DROOP RATE — 0.1μV/μs (25°C); 100μV/μs (FULL TEMP)
- APERTURE TIME — 25ns
- PEDESTAL ERROR — 2.5 mV (ADJUSTABLE TO ZERO)
- INTERNAL HOLD CAPACITOR
- FULLY DIFFERENTIAL INPUT
- TTL COMPATIBLE

APPLICATIONS

- PRECISION DATA ACQUISITION SYSTEMS
- D/A CONVERTER DEGLITCHING
- AUTO-ZERO CIRCUITS
- PEAK DETECTORS

DESCRIPTION

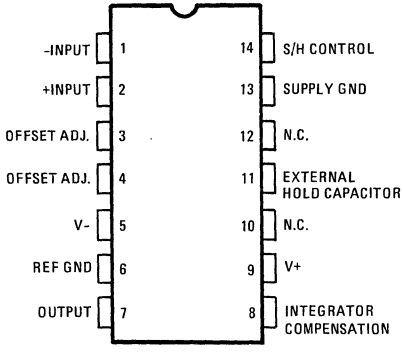
The HA-5320 was designed for use in data acquisition systems whose sample-and-hold acquisition time is the primary speed limiting specification. The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier.

The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

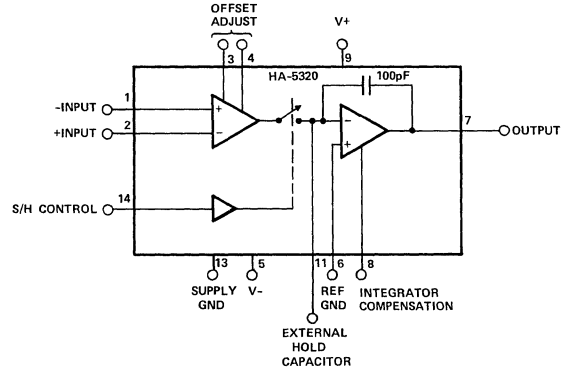
This monlithic device is manufactured using the Harris dielectric isolation process, minimizing stray capacitance and eliminating SCR's. This allows higher speed and latch-free operation. The HA-5320 requires ±15V, and is available in a ceramic or plastic 14-pin DIP.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



5

HARRIS

HI-565A

ADVANCE

High Speed Monolithic Digital to Analog Converter with Reference

FEATURES

- DAC AND REFERENCE ON A SINGLE CHIP
- VERY HIGH SPEED: SETTLES TO 1/2 LSB IN 350ns TYP
  FULL SCALE SWITCHING TIME 30ns (TYP)
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- 1/2 LSB MAX NONLINEARITY GUARANTEED OVER TEMPERATURE
- LOW GAIN DRIFT (MAX, DAC PLUS REFERENCE) 15ppm/°C
- LOW POWER DISSIPATION, MAX. 345mW

APPLICATIONS

- CRT DISPLAYS
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIS

DESCRIPTION

The HI-565A is a fast, 12 bit digital to analog converter with a precision voltage reference on a single chip.

Twelve high speed bipolar switches route the current from each bit cell either to ground or to the laser trimmed thinfilm R-2R ladder network, depending on the logic level of the bit input.

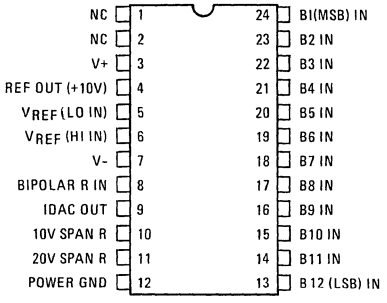
The Harris dielectric isolation process is used to fabricate the HI-565A, providing minimal stray capacitance and latch-free operation. The chips are laser tirmmed at the wafer level to a maximum linearity error of 1/4 LSB at +25°C, making the HI-565A an ideal choice when both high speed and high accuracy are essential.

The low noise, highly stable reference voltage is brought out to a package pin, and may be used elsewhere in the system. Laser trimming sets the absolute value and temperature coefficient of the reference. The HI-565A is thus well suited for a wide temperature range with a maximum linearity error of 1/2 LSB.

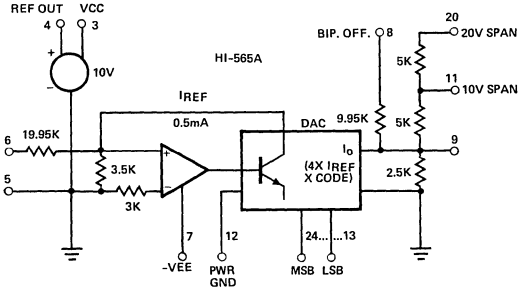
The HI-565A is available in both commercial and military temperature grades, and is packaged in a ceramic 24 pin DIP. Power requirement is +5V, -15V.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



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HARRIS

HI-574A

ADVANCE

Fast, Complete 12-Bit Analog to Digital Converter with Microprocessor Interface

FEATURES

- AD574A SECOND SOURCE
- LOW POWER 360mW
- COMPLETE 12-BIT A/D CONVERTER WITH REFERENCE AND CLOCK
- FULL 8 OR 16-BIT μP INTERFACE
- FAST SUCCESSIVE APPROXIMATION CONVERSION 25 μs
- COMPOUND MONOLITHIC CONSTRUCTION
- NO MISSING CODES OVER TEMPERATURE
- LOW GAIN T.C. 10ppm/°C
- LOW COST

APPLICATIONS

- HIGH PERFORMANCE DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- MILITARY AND INDUSTRIAL SYSTEMS

DESCRIPTION

The Harris HI-574A is a complete 12-bit analog-to-digital converter. Successive approximation conversion is performed by two monolithic chips housed in a 28-pin dual-in-line package. This compound monolithic circuit combines Harris' CMOS and Bipolar processes.

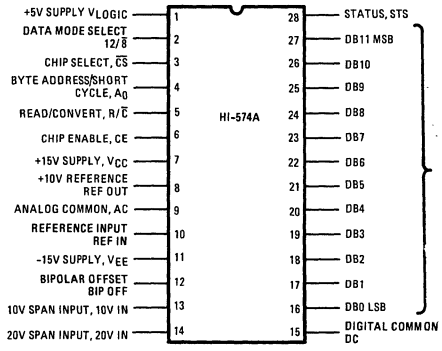
Designed as a direct replacement for the AD574A, the device offers full microprocessor compatibility by both 8 and 16-bit systems via "Three State" output buffer circuitry. Wafer level laser trimming techniques provide close match of ladder resistors, ensuring high accuracy plus a guarantee of no missing codes over temperature. Included in the A/D converter are a 12-bit, high performance digital-to-analog converter, a very stable voltage reference, and an accurate comparator.

In systems where power consumption must be minimized, Harris offers a significant improvement over other manufacturers units. The HI-574A dissipates typically 400mW.

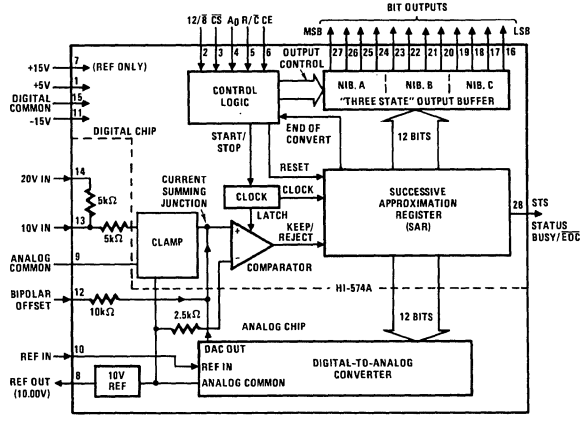
The HI-574A is available in versions which have guaranteed performance over both military and commercial temperature ranges. Screening to MIL-STD-883A, Class B is also available.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



HARRIS

HI-5660

ADVANCE

High Speed Monolithic Digital-to-Analog Converter

FEATURES

- VERY HIGH SPEED: SETTLES TO 1/2 LSB IN 350ns
  FULL SCALE SWITCHING TIME 30ns
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- 1/2 LSB MAX NONLINEARITY GUARANTEED OVER TEMPERATURE
- LOW GAIN DRIFT 10ppm/°C
- LOW POWER DISSIPATION 230mW
- LOW COST
- LOW PSF 1ppm/%PS

APPLICATIONS

- CRT DISPLAYS
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIS

DESCRIPTION

The HI-5660 12-bit digital-to-analog converter is a similar second source to the AD566, yet offers improved power dissipation performance.

Twelve high speed bipolar switches route the current from each bit cell either to ground or to the laser trimmed thin film R-2R ladder network, depending on the logic level of the bit input.

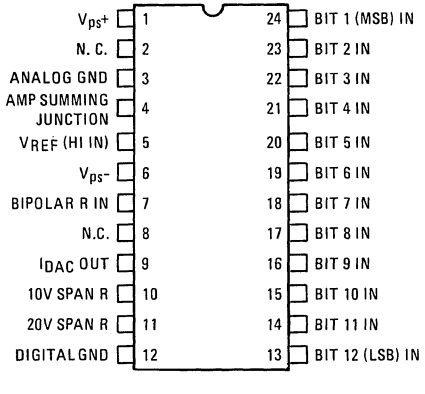
The Harris dielectric isolation process is used to fabricate the HI-5660, providing minimal stray capacitance and latch-free operation. The chips are trimmed at the wafer level to a maximum linearity error of 1/4 LSB at 25°C, making the HI-5660 an ideal choice when both high speed and high accuracy are essential.

For a +10V reference, Harris recommends using the HA-1610. This highly stable precision reference is laser trimmed to an absolute accuracy of ± 0.05% and a temperature coefficient of ± 3ppm/°C. For designs where an external reference is impractical, the HI-565A DAC is recommended.

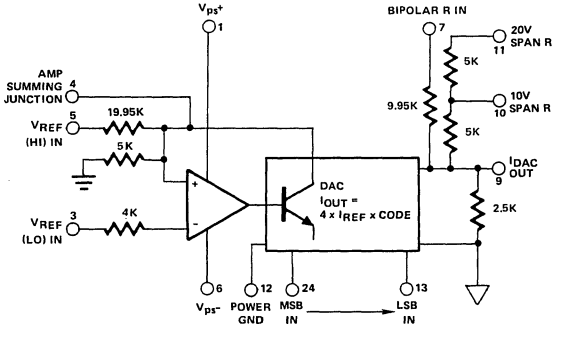
The HI-5660 is available in both commercial and military temperature grades, and is packaged in a ceramic 24 pin DIP. Power requirement is +5V, -15V.

PINOUT

TOP VIEW
24 LEAD DIP



FUNCTIONAL DIAGRAM



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HARRIS

ADVANCE

HI-5680

12 Bit Low Cost Monolithic Digital-to-Analog Converter

FEATURES

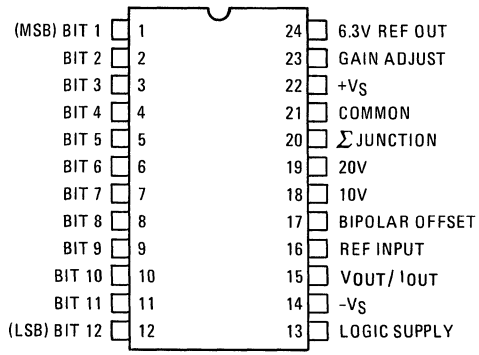
- DAC 80 ALTERNATE SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED MONOTONIC 0°C TO 75°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

PINOUT

TOP VIEW



DESCRIPTION

The HI-5680 is a monolithic direct replacement for the popular DAC 80 12-bit digital to analog converter. Single chip construction makes the HI-5680 the optimum choice for low cost, high reliability applications. Additionally, Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching time and minimum glitch. Wafer-level laser trimming of ladder and span resistors ensures high accuracy and exceptional tracking over temperature.

The HI-5680 is available in both current and voltage output models which are guaranteed over the 0°C to 75°C temperature range.

MODEL	INPUT CODE	OUTPUT MODE
HI-5680 V	Complementary Binary	Voltage
HI-5680 I	Complementary Binary	Current

All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier.

Power requirements consist of a +5V logic supply and ±Vs which has a range of ±(11.4V to 16.5V). The package is a 24 pin DIP.

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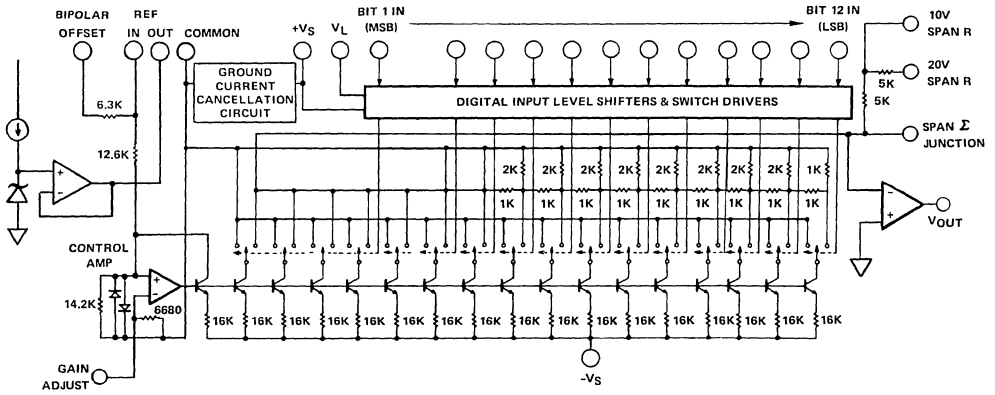
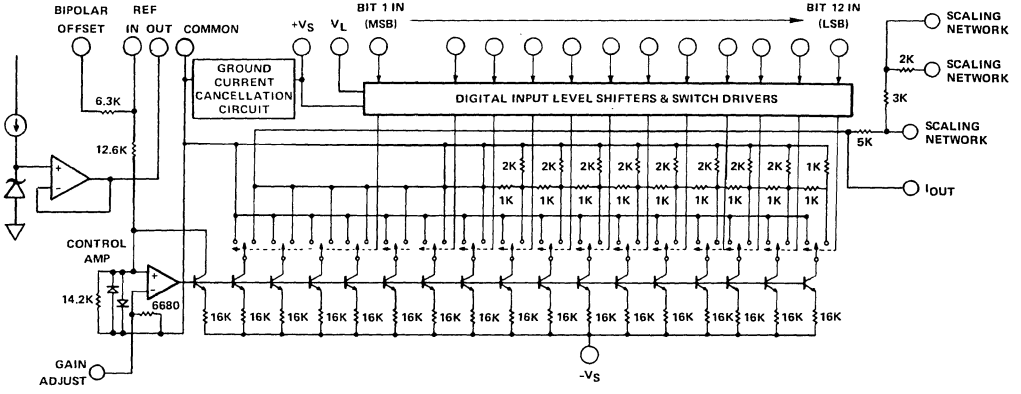
FUNCTIONAL DIAGRAM VOLTAGE OUTPUT



HI-5680 V

FUNCTIONAL DIAGRAM CURRENT OUTPUT



HI-5680 I

HARRIS

ADVANCE

HI-5685

High Performance Monolithic 12 Bit Digital-to-Analog Converter

FEATURES

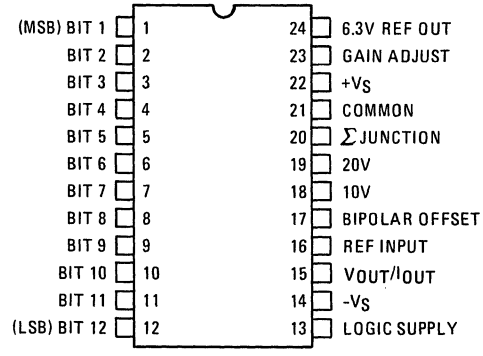
- DAC 85 SECOND SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED MONOTONIC -25°C TO +85°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

PINOUT

TOP VIEW



DESCRIPTION

The HI-5685 is a monolithic direct replacement for the popular DAC 85 12-bit digital to analog converter. Single chip construction makes the HI-5685 the optimum choice for low cost, high reliability applications. Additionally, Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching time and minimum glitch. Wafer-level laser trimming of ladder and span resistors ensures high accuracy and exceptional tracking over temperature.

The HI-5685 is available in both current and voltage output models which are guaranteed over the specified temperature range.

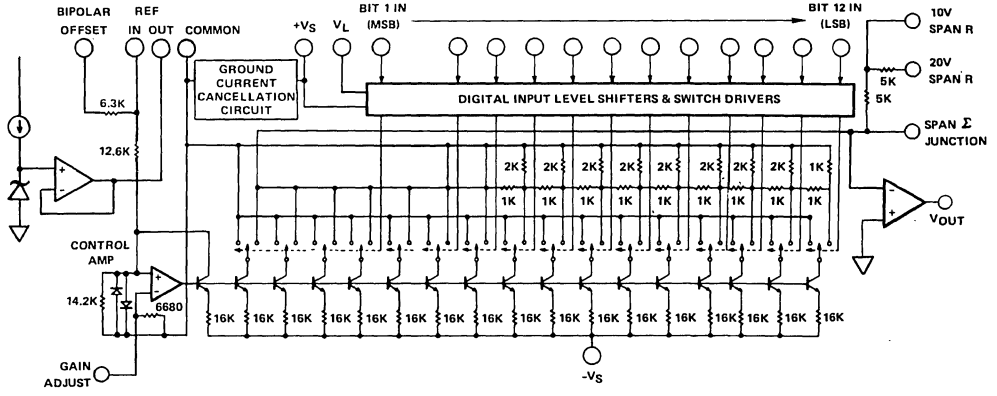
MODEL	INPUT CODE	OUTPUT MODE	TEMPERATURE RANGE
HI-5685 V	Complementary Binary	Voltage	-25°C to +85°C
HI-5685 I	Complementary Binary	Current	-25°C to +85°C
HI-5685 V	Complementary Binary	Voltage	-25°C to +85°C
HI-5685 I	Complementary Binary	Current	-25°C to +85°C

All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier.

Power requirements consist of a +5V logic supply and ±Vs which has a range of ±(11.4V to 16.5V). The package is a 24 pin DIP.

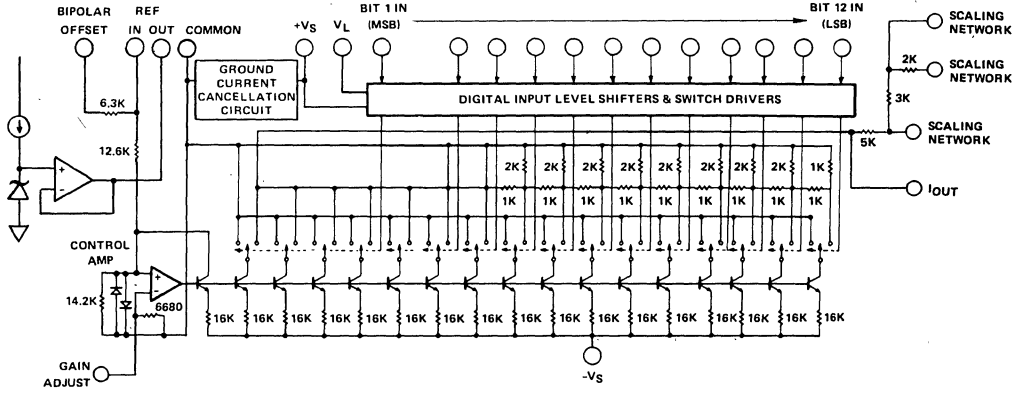
5

FUNCTIONAL DIAGRAM VOLTAGE OUTPUT



HI-5685 V

FUNCTIONAL DIAGRAM CURRENT OUTPUT



HI-5685 I

5

HARRIS

ADVANCE

HI-5687

Wide Temperature Range Monolithic 12 Bit Digital-to-Analog Converter

FEATURES

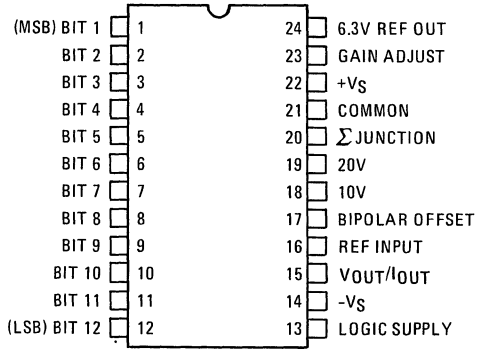
- DAC 87 SECOND SOURCE
- MONOLITHIC CONSTRUCTION (SINGLE CHIP)
- FAST SETTLING
- GUARANTEED SPECIFICATIONS -55°C to 125°C
- WAFER LASER TRIMMED
- APPLICATIONS RESISTORS ON-CHIP
- ON-BOARD REFERENCE
- DIELECTRIC ISOLATION (DI) PROCESSING
- ±12V POWER SUPPLY OPERATION

APPLICATIONS

- HIGH SPEED A/D CONVERTERS
- PRECISION INSTRUMENTATION
- CRT DISPLAY GENERATION

PINOUT

TOP VIEW



DESCRIPTION

The HI-5687 is a monolithic direct replacement for the popular DAC 87 12-bit digital to analog converter. Single chip construction makes the HI-5687 the optimum choice for low cost, high reliability applications. Additionally, Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching time and minimum glitch. Wafer-level laser trimming of ladder and span resistors ensures high accuracy and exceptional tracking over temperature.

The HI-5687 is available in both current and voltage output models which are 100% tested over the -55°C to +125°C temperature range.

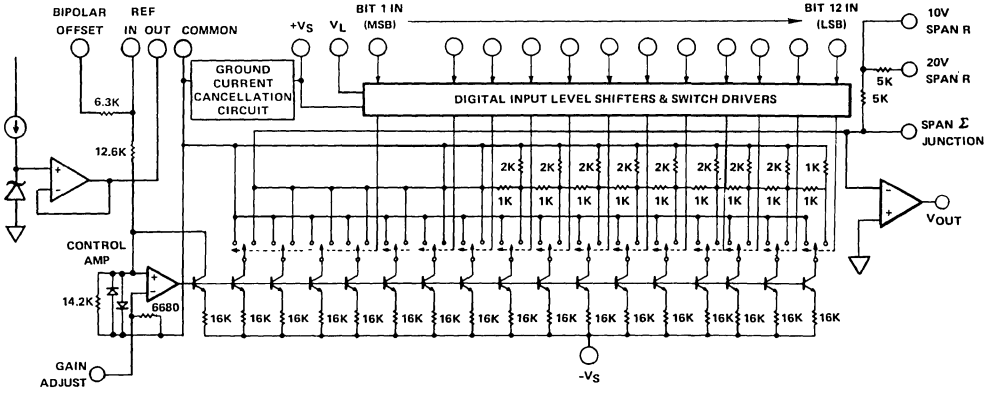
MODEL	INPUT CODE	OUTPUT MODE
HI-5687 V	Complementary Binary	Voltage
HI-5687 I	Complementary Binary	Current

All models include a buried zener reference featuring low temperature coefficient. In addition, the voltage output models include an on-board output amplifier.

Power requirements consist of a +5V logic supply and ±Vs which has a range of ±(11.4V to 16.5V). The package is a 24 pin DIP.

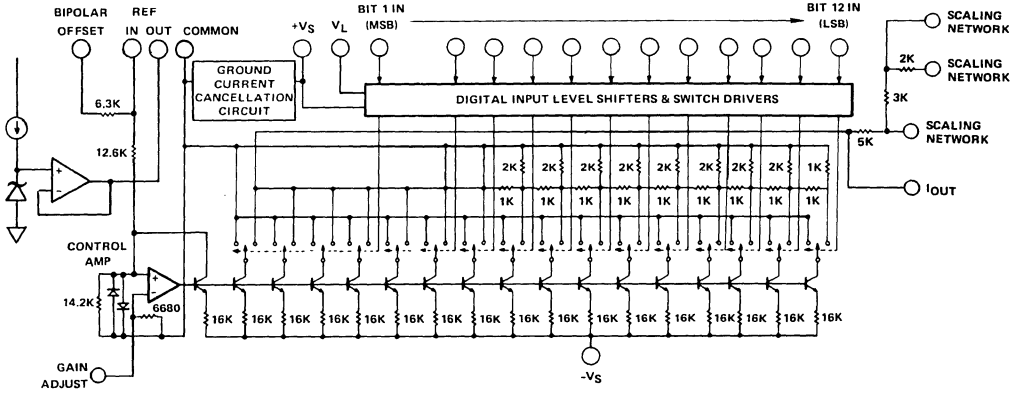
5

FUNCTIONAL DIAGRAM VOLTAGE OUTPUT



HI-5687 V

FUNCTIONAL DIAGRAM CURRENT OUTPUT



HI-5687 I

5

HARRIS

ADVANCE

HI-DAC16B/C

16-Bit D to A Converter

FEATURES

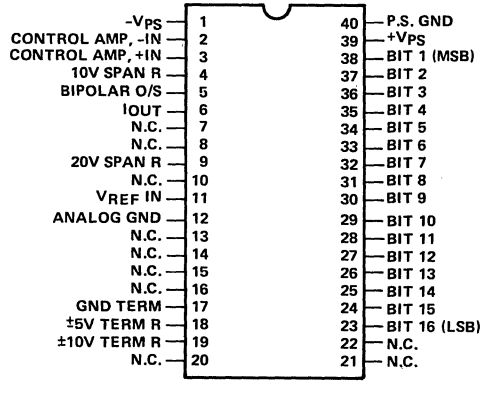
- 16 BIT RESOLUTION
- MONOLITHIC DI BIPOLAR CONSTRUCTION
- FAST SETTLING TIME — 1 μs TO .003%FS
- LOW DIFF. NONLIN. DRIFT — ± 0.3ppm/°C
- LOW GAIN DRIFT — ± 1ppm/°C
- ON-CHIP SPAN & OFFSET RESISTORS
- TTL/5V-CMOS COMPATIBLE
- LOW UNIPOLAR OFFSET — ≤ 1/2LSB@ +25°C
- LOW UNIPOLAR OFFSET T.C. — ± 0.2ppm/°C
- EXCELLENT STABILITY

APPLICATIONS

- HIGH RESOLUTION CONTROL SYSTEMS
- HIGH FIDELITY AUDIO RECONSTRUCTION
- PRECISION FUNCTION GENERATION AND INSTRUMENTATION

PINOUT

TOP VIEW



DESCRIPTION

The HARRIS HI-DAC16 is a 16-bit, current output D/A converter. Single chip construction includes thin-film application resistors for use with an external op amp. These permit standard output voltage ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V and ±10V.

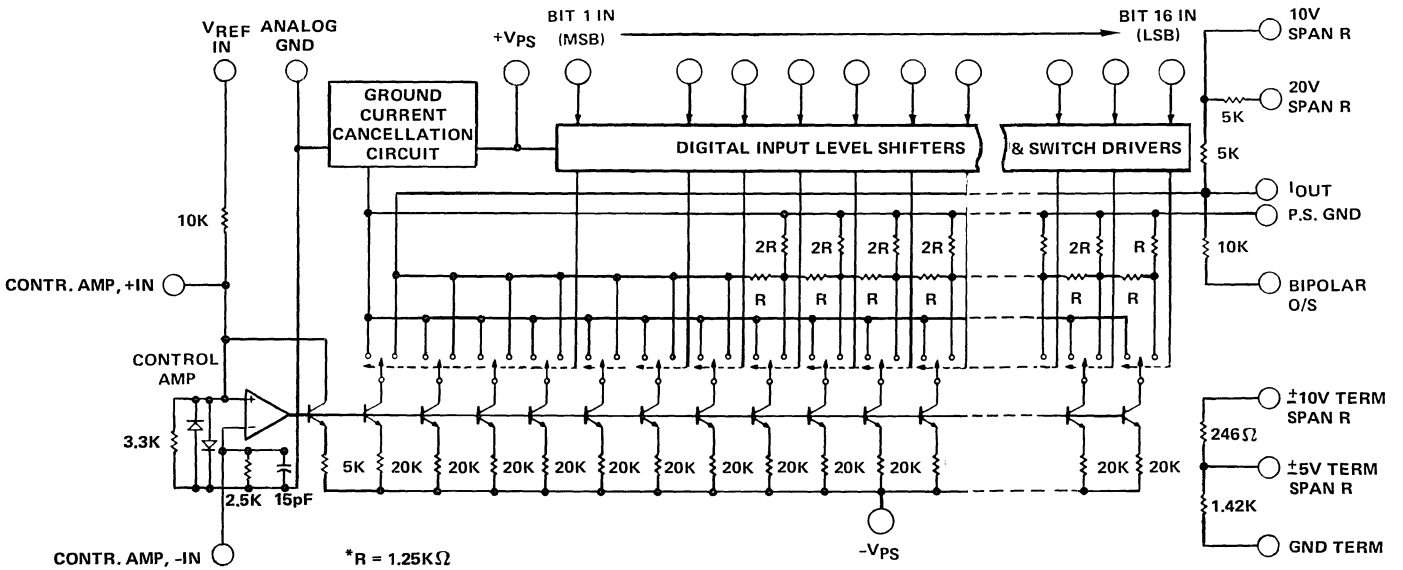
Reference and span resistors have adjacent placement on the chip for optimum match and thermal tracking. Futhermore, this layout feature helps minimize the superposition error caused by self-heating of the span resistor, reducing it to less than 1/10LSB. This and other design innovations have produced exceptionally stable operation over temperature. Typical temperature coefficients are ± 1ppm/°C for gain error and 0.3ppm/°C for differential non-linearity error.

The internal architecture is an extension of the earlier HI-562 with several major improvements. All code dependent ground currents are steered to a separate non-critical path, namely, power supply ground. This feature allows the precision ground of the converter to be sensed with virtually zero voltage drop referred to system ground. The result is the complete elimination of non-linearities due to code dependent ground currents while yielding an extremely low unipolar offset of less than 1/2LSB. Because of this separation, the user may route the precision ground some distance to the system ground without degrading converter accuracy.

The HARRIS HI-DAC16 delivers a stable, accurate output without sacrifice in speed. Settling time to within ±0.003% is one microsecond. Overall performance of this monolithic device should be attractive for applications such as high fidelity audio and high-resolution control systems.

Typical power requirement is 450 MW, from the +15V and -15V supplies combined. The package is a 40 pin ceramic DIP. Two accuracy grades are offered.

5


VREF IN
ANALOG GND
+VPS
BIT 1 IN (MSB)
BIT 16 IN (LSB)
10V SPAN R
20V SPAN R
5K
GROUND CURRENT CANCELLATION CIRCUIT
DIGITAL INPUT LEVEL SHIFTERS
& SWITCH DRIVERS
5K
IOUT
P.S. GND
10K
2R
R
10K
BIPOLAR O/S
CONTR. AMP, +IN
CONTROL AMP
3.3K
5K
20K
±10V TERM SPAN R
246Ω
±5V TERM SPAN R
1.42K
GND TERM
2.5K
15pF
CONTR. AMP, -IN
*R = 1.25KΩ
-VPS

5

Communications

6

ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Characteristics" are the only conditions recommended for satisfactory operation.

HARRIS

HC-55516

All-Digital Continuously Variable Slope Delta Modulator (CVSD)

FEATURES

- REQUIRES FEWER EXTERNAL PARTS
- LOW POWER DRAIN: 6mW FROM SINGLE 5V-7V SUPPLY
- TIME CONSTANTS DETERMINED BY CLOCK FREQUENCY; NO CALIBRATION OR DRIFT PROBLEMS; AUTOMATIC OFFSET ADJUSTMENT
- HALF DUPLEX OPERATION BY DIGITAL CONTROL
- FILTER RESET BY DIGITAL CONTROL
- AUTOMATIC OVERLOAD RECOVERY
- AUTOMATIC "QUIET" PATTERN GENERATION
- AGC CONTROL SIGNAL AVAILABLE

APPLICATIONS

- VOICE TRANSMISSION OVER DATA CHANNELS
- VOICE ENCRYPTION/SCRAMBLING
- VOICE I/O FOR DIGITAL SYSTEMS AND SPEECH SYNTHESIS
- AUDIO MANIPULATIONS: DELAY LINES, TIME COMPRESSION, ECHO GENERATION/ SUPPRESSION, SPECIAL EFFECTS, ETC.

The HC-55516 is a half duplex modulator/demodulator CMOS integrated circuit used to convert voice signals into serial NRZ digital data, and to reconvert that data into voice. The conversion is by delta modulation, using the continuously variable slope (CVSD) method of companding.

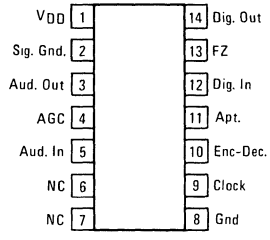
While signals are compatible with other CVSD circuits, internal design is unique. The analog loop filters have been replaced by digital filters, using very low power, and requiring no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The HC-55516 has internal time constants optimized for a 16K bits/sec data rate and is usable from 9K bits/sec to above 64K bits/sec. The unit is available in 14 pin DIP (HC1) packages in two temperature ranges: -55°C to +125°C (-2 or -8), and -40°C to +85°C (-9). It is also available in chip form.

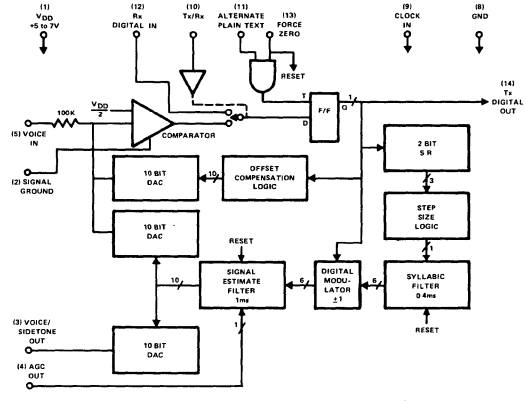
PINOUT

Section 11 for Packaging

Top View



FUNCTIONAL DIAGRAM



PIN # 14-LEAD D.I.P.	SYMBOL	ACTIVE* LEVEL	DESCRIPTION
1	V_{DD}		Positive supply voltage.
2	Sig. Gnd.		Ground connection to D/A ladders and comparator; i.e. audio ground.
3	Aud. Out		Recovered audio out. May be used as side tone at the transmitter. Presents approximately 100 kilohm source. Zero signal reference is $V_{DD}/2$.
4	AGC		A logic "Low" level will appear at this output when the recovered signal excursion reaches one-half of full scale value.
5	Aud. In		Audio input. Should be externally AC coupled. Presents approximately 100 kilohms in series with $V_{DD}/2$.
6,7			No internal connection is made to these pins.
8	Gnd.		Logic ground. Negative supply voltage.
9	Clock		Receiver clock must be phased with digital input such that data must be present at the positive clock transition.
10	Encode (Decode)	Low (High)	A single CVSD can provide half-duplex operation. The encode and decode functions are selected by the logic level applied to this input. A low level selects the encode mode, a high level, the decode mode.
11	APT.	Low	Activating this input causes an "alternate plain text" (quieting pattern) to be transmitted without affecting the internal operation of the CVSD.
12	Dig. In		Input for the received digital data.
13	FZ	Low	Activating this input forces the transmitted output, the internal logic, and the recovered audio output into the "quieting" condition.
14	Dig. Out		Output for transmitted digital data.

*Note: No active input should be left in a "floating condition".

ABSOLUTE MAXIMUM RATINGS

Voltage At Any Pin	-3.0V to V_{DD} +0.3V	Operating Temperature (-9)	-40°C to +85°C
Maximum V_{DD} Voltage	+7.0V	(-2)	-55°C to +125°C
		(-8)	-55°C to +125°C
Operating V_{DD} Range	+5.0V to +7.0V	Storage Temperature	-65°C to +150°C

ELECTRICAL CHARACTERISTICS @ T_A = 25°C

Test Conditions V_{DD} = 6.0V, Bit Rate = 16Kb/s

PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Bit Rate		16/32	64	Kb/s	(1)
Clock Duty Cycle	30		70	%	
Supply Voltage	+5.0		+7.0	V	
Supply Current		1.0		mA	
Digital "1" Input		4.5		V	(2)
Digital "0" Input		1.5		V	(2)
Digital "1" Output		5.5		V	(3)
Digital "0" Output		0.5		V	(3)
Audio Input Voltage		0.5	1.4	Vrms	(4)
Audio Output Voltage		0.5	1.4	Vrms	(5)
Audio Input Impedance		100		KΩ	(6)
Audio Output Impedance		100		KΩ	(7)
Transfer Gain	-0.5		+0.5	dB	(8)
Syllabic Time Constant		4.0		mS	(9)
L.P. Filter Time Constant (55516)		0.94		mS	(9)
Step Size Ratio (55516)		24		dB	(10)
Resolution (55516)		0.1		%	(11)
Min. Step Size (55516)		0.2		%	(12)
Slope Overload		Fig. 1			(13)
Signal/Noise Ratio			Tab. 1		(14)
Quieting Pattern Amplitude (55516)		12		mV P-P	(15)
AGC Threshold		0.5		F.S.	(16)
Clamping Threshold		0.75		F.S.	(17)

NOTES

1. There is one NRZ (Non-Return Zero) data bit per clock period. Clock must be phased with digital data such that data must be present at the positive clock transition.

2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.

3. Logic outputs are CMOS compatible at supply voltage and withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions.

4. Recommended voice input range for best voice performance.

5. May be used for side-tone in encode mode.

6. Should be externally AC coupled. Presents 100 Kilohms in series with $V_{DD}/2$.

7. Presents 100 Kilohms in series with recovered audio voltage. Zero-signal references is $V_{DD}/2$.

8. Unloaded, for linear signals.

9. Note that filter time constants are inversely proportional to clock rate.

10. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.

11. Minimum quantization voltage level expressed as a percentage of supply voltage.

12. The minimum step size between levels is twice the resolution.

13. For large signal amplitudes or high frequencies, the encoder may become slope-overloaded. Figure 1 shows the frequency response at various signal levels,measured with a 3kHz low-pass filter having a 130dB/octave roll-off to -50dB. See Table II.

14. Table I shows the SNR under various conditions, using the output filter described in 13 (above) at a bit rate of 16Kb/s. See Table II.

15. The "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.

16. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative).

17. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

TABLE I

INPUT FREQUENCY Hz	INPUT AMPLITUDE mV RMS	OUTPUT SNR dB MIN.
300	1400	20
300	45	15
1000	500	14
1000	16	9

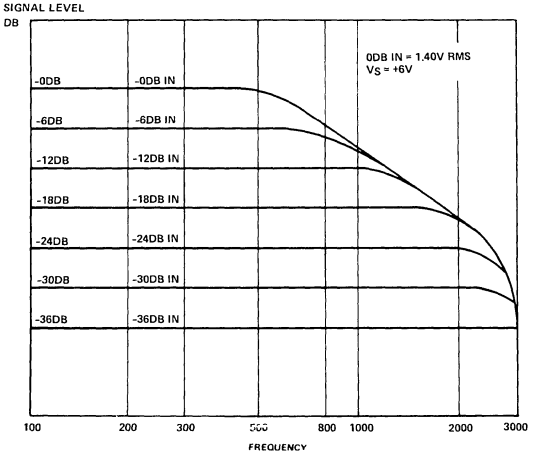


Figure 1 — Transfer Function for CVSD at 16KB

NOTES (Continued)

TABLE II

INPUT FILTER FREQUENCY RESPONSE		OUTPUT FILTER FREQUENCY RESPONSE	
FREQUENCY	RELATIVE OUTPUT	FREQUENCY	RELATIVE OUTPUT
100Hz	0±0.5dB	100Hz to 1500Hz	0±1.5dB
200Hz	0±0.1dB	1500Hz to 3000Hz	0±2.5dB
1000Hz	0±0.1dB	3800Hz to 100KHz	Less Than -45dB
3000Hz	-3±0.5dB		
9000Hz	-20±2.0dB		

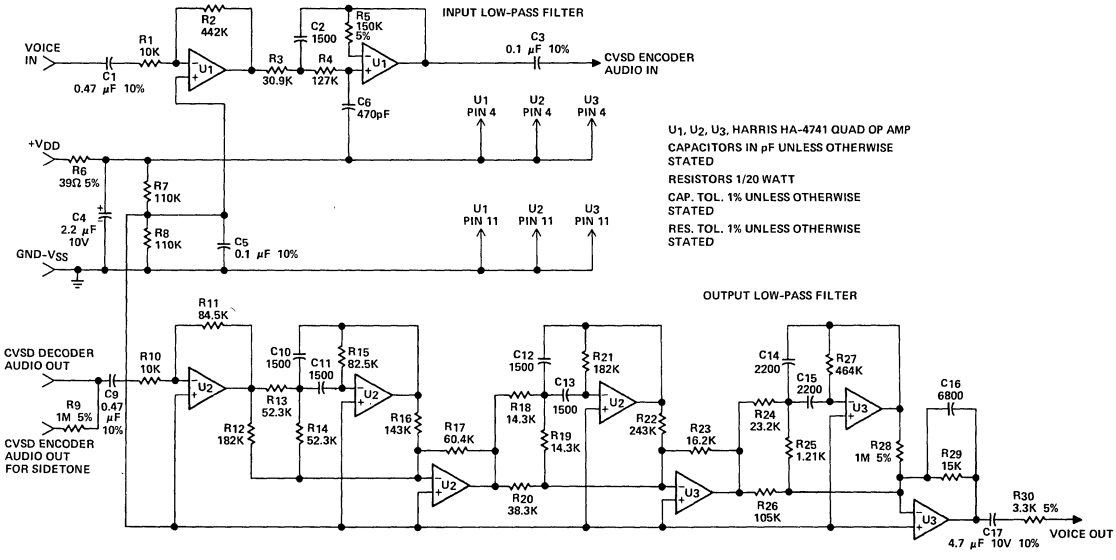


Figure 2 – Suggested Input/Output Audio Filters for SNR Measurement

NOTE: An output filter similar to the input filter section above will generally suffice for good voice intelligibility.

HARRIS

HC-5502

SLIC-LC Subscriber Line Interface Circuit

Preliminary

FEATURES

- MONOLITHIC INTEGRATED DEVICE
- UNIQUE DI HIGH VOLTAGE PROCESS
- COMPATIBLE WITH WORLDWIDE PABX PERFORMANCE REQUIREMENTS
- CONTROLLED SUPPLY OF BATTERY FEED CURRENT FOR SHORT LOOPS
- INTERNAL RING RELAY DRIVER
- LOW POWER CONSUMPTION DURING STANDBY
- SWITCH HOOK, GROUND KEY AND RING TRIP DETECTION FUNCTIONS
- SELECTIVE DENIAL OF POWER TO SUBSCRIBER LOOPS

APPLICATIONS

- SOLID STATE LINE INTERFACE CIRCUIT FOR DIGITAL PBX SYSTEMS

DESCRIPTION

The HARRIS SLIC-LC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. Using the unique HARRIS dielectric isolation process, the SLIC-LC can operate directly with a wide range of station battery voltagees.

The SLIC-LC also provides selective denial of power. If the PABX system becomes overloaded during an emergency, the SLIC-LC will provide system protection by denying power to selected subscriber loops.

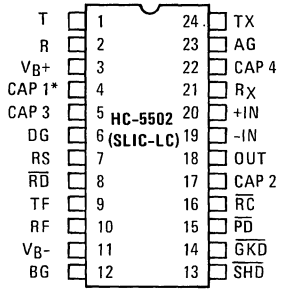
The HARRIS SLIC-LC is ideally suited in the design of new digital PABX systems, by eliminating bulky, expensive hybrid transformers.

SLIC-LC is available in either a 24 pin dual-in-line plastic or ceramic package.

PINOUT

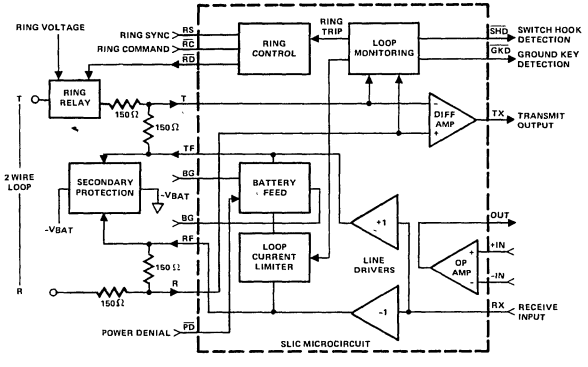
Section 11 for Packaging

TOP VIEW



*Optional

FUNCTIONAL DIAGRAM



6

ABSOLUTE MAXIMUM RATINGS

Maximum Continuous Supply Voltages	(V_{B-})	-60 to +.5 Volts
	(V_{B+})	-.5 to +15 Volts
	($V_{B+} - V_{B-}$)	75 Volts
Operating Ambient Temperaure Range	(T_A)	0°C to +75°C
Storage Temperature Range (R_{SRG})		-40°C to +85°C
Power Package Dissipation @ 25°C (P_D)		TBD
Power Dissipation Derating		TBD

RECOMMENDED OPERATING CONDITIONS

Positive Supply Voltage (V_{B+})	10.8 to 13.2 Volts
Negative Supply Voltage (V_{B-})	-42 to -58 Volts
Minimum High Level Logic Input Voltage	2.4 Volts
Maximum Low Level Logic Input Voltage	0.8 Volts
Loop Resistance (R_L)	200 to 1200 Ohms
Ambient Operating Temperature Range (T_A)	0°C to +70°C

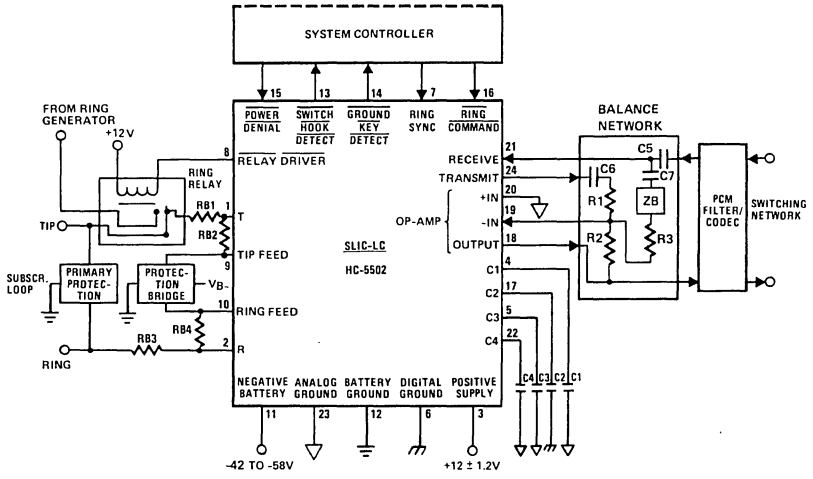
ELECTRICAL CHARACTERISTICS

(V_{B-} = -48V, V_{B+} = +12V, AG = BG = DG at = 0V, T_A = 25°C Unless Otherwise Stated)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook Power Dissipation			110		mW
Off Hook Loop Current	R_{LOOP} = 1200 Ohms		21		mA
Off Hook Loop Current	R_{LOOP} = 200 Ohms		27		mA
Fault Currents					
TIP to V_{B+} Ground			13.3		mA
RING to V_{B+} Ground			54		mA
TIP to RING			27		mA
TIP and RING to V_{B+} Ground			67		mA
Ring Relay Driver Current	0.2 Volts		62		mA
Ring Trip Detection Period	R_{LOOP} = 600 Ohms		2		Ring Cycles
Switch Hook Detection Threshold		5	7.5	10	mA
Ground Key Detection Threshold			12.5	20	mA
Dial Pulse Distortion			0.1		ms
Receive Input Impedance			90		k Ohms
Transmit Output Impedance			1		Ohm
Two Wire Return Loss	(Return Loss Referenced				
SRL LO	to 600Ω+2.16μF)		15.5		dB
ERL			24		dB
SRL HI			31		dB
Longitudinal Balance	1V Peak-Peak				
2 Wire Off Hook	200Hz – 3400Hz		72		dB
2 Wire On Hook			63		dB
4 Wire Off Hook			64		dB
Low Frequency Longitudinal Balance	R.E.A. Method			23	dBrnC

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Insertion Loss	@ 1kHz, 0dBm Input Level				
2 Wire – 4 Wire			±.05	±.15	dB
4 Wire – 2 Wire			±.05	±.15	dB
Frequency Response	200 – 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level		±.02		dB
Idle Channel Noise					
2 Wire – 4 Wire				5	dBrnC
4 Wire – 2 Wire				5	dBrnC
Absolute Delay					
2 Wire – 4 Wire				30	μs
4 Wire – 2 Wire				30	μs
Envelope Delay					
2 Wire – 4 Wire				90	μs
4 Wire – 2 Wire				90	μs
Trans Hybrid Loss	Balance Network Set Up for 600 Ohm Termination	36	40		dB
Overload Level					
2 Wire – 4 Wire		+4			dBm
4 Wire – 2 Wire		+4			dBm
Level Linearity					
2 Wire – 4 Wire	+3 to -40dBm			±.05	dB
	-40 to -50dBm			±.1	dB
	-50 to -55dBm			±.3	dB
4 Wire – 2 Wire	+3 to -40dBm			±.05	dB
	-40 to -50dBm			±.1	dB
	-50 to -55dBm			±.3	dB
Power Supply Rejection Ratio					
V_{B+} to 2 Wire	10 – 60Hz, $R_{LOOP} = 600\Omega$	15			dB
V_{B+} to Transmit		15			dB
V_{B-} to 2 Wire		15			dB
V_{B-} to Transmit		15			dB
V_{B+} to 2 Wire	200 – 16kHz	30			dB
V_{B+} to Transmit	$R_{LOOP} = 600\Omega$	30			dB
V_{B-} to 2 Wire		30			dB
V_{B-} to Transmit		30			dB
Logic Inputs					
Logic '0' V_{IL}				0.8	Volts
Logic '1' V_{IH}		2.4		5.5	Volts
Logic Outputs	Max Two TTL Loads				
Logic '0' V_{OL}			0.1	0.8	Volts
Logic '1' V_{OH}		3.0	6.1	6.3	Volts

PIN NUMBER	SYMBOL	DESCRIPTION
1	T	An analog input connected to the TIP (more positive) side of the subscriber loop through the ring relay. Used with the ring lead to receive voice signals from the telephone and for loop monitoring purposes.
2	R	An analog input connected to the RING (more negative) side of the subscriber loop. Used with the tip lead to receive voice signals from the telephone and for loop monitoring purposes.
3	V_{B+}	Positive Voltage Source – Most positive supply. V_{B+} is typically 12 volts with an operational range of 10.8 to 13.2 volts.
4	CAP 1	Capacitor #1 – Optional Capacitor used to improve +12 V supply rejection. This pin should be left open if unused.
5	CAP 3	Capacitor #3 – An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering -48V supply. Typical value is 0.3μF, 30V.
6	DG	Digital Ground – To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.
7	RS	Ring Synchronization Input – A TTL-compatible clock input. The clock is arranged such that a positive transition occurs on the negative going zero crossing of the ring voltage source. Ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero.
8	$\overline{RD}$	Relay Driver – A low active open collector logic output. When enabled, the external ring relay is energized.
9	TF	Tip Feed – A low impedance analog output connected to the tip lead through a 300 Ohm ±1% feed resistance. Used with the ring feed lead to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.
10	RF	Ring Feed – A low impedance analog output connected to the ring lead through a 300 Ohm ±1% feed resistance. Used with the tip feed lead to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.
11	V_{B-}	Negative Voltage Source – Most negative supply. V_{B-} is typically -48 volts with an operational range of -42 to -58 volts. Frequently referred to as "battery".
12	BG	Battery Ground – To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.
13	$\overline{SHD}$	Switch Hook Detection – A low active TTL-compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.
14	$\overline{GKD}$	Ground Key Detection – A low active TTL-compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 17.5mA, and disabled if this current difference is less than 10mA.
15	$\overline{PD}$	Power Denial – A low active TTL-compatible logic input. When enabled, the loop current is limited to a maximum 2mA, the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.
16	$\overline{RC}$	Ring Command – A low active TTL-compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next rising edge of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off-hook ($\overline{SHD}$ = 0).
17	CAP 2	Capacitor #2 – An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15μF, 10V. This capacitor is not used if ground key function is not required.
18	OUT	The analog output of the spare operational amplifier.
19	-IN	The inverting analog input of the spare operational amplifier.
20	+IN	The non-inverting analog input of the spare operational amplifier.
21	RX	Receive Input, Four Wire Side – A high impedance (90kΩ) analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the tip feed and ring feed terminals, which in turn drive tip and ring through the 300 Ohm feed resistance.
22	CAP 4	Capacitor #4 – An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced into the subscriber loop from near proximity power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5μF, 20V.
23	AG	Analog Ground – To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.
24	TX	Transmit Output, Four Wire Side – A low impedance (10Ωmax) analog output which represents the differential voltage across tip and ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.



TYPICAL COMPONENT VALUES

C1 = .5μF C4 = .5μF
C2 = .15μF C5 = .5μF
C3 = .3μF C6 = C7 = .1μF (1% Match Required) Note 2

R1 → R3 = 100kΩ (.1% Match Required) ,ZB = 0 for 600ΩTerminations Note 2
RB1 = RB2 = RB3 = RB4 = 150Ω (0.1% Match Required)

NOTE 1: C1 is an optional capacitor used to improve +12V supply rejection. This pin must be left open if unused.

NOTE 2: To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 are 1μF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -12 volt step when the loop is closed and that too large a value for C6 may produce an excessively long transient at the op-amp output to the pcm Filter/CODEC. A 1μF capacitor at C6 and C7 would typically produce a 300 millisecond transient.

HARRIS

HC-5510/HC-5511

Monolithic CODECs

Preliminary

FEATURES

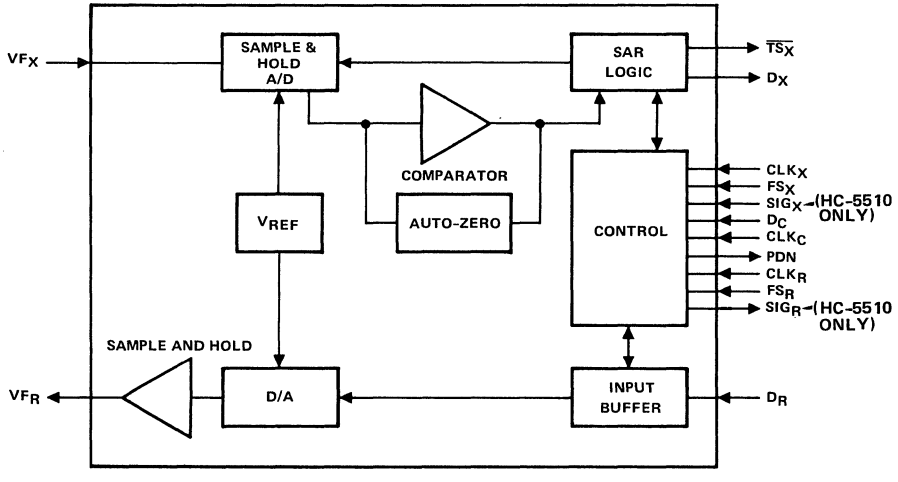
- LOW OPERATION POWER 45mW TYPICAL
- LOW STANDBY POWER 1mW TYPICAL
- ±5V OPERATION
- TTL COMPATIBLE DIGITAL INTERFACE
- TIME SLOT ASSIGNMENT OR ALTERNATE FIXED TIME SLOT MODES
- INTERNAL PRECISION REFERENCE
- INTERNAL SAMPLE AND HOLD CAPACITORS
- INTERNAL AUTO-ZERO CIRCUIT
- HC-5510 – μ-LAW CODING WITH SIGNALING CAPABILITIES
- HC-5511 – A-LAW CODING
- SYNCHRONOUS OR ASYNCHRONOUS OPERATION

DESCRIPTION

The HC-5510 and HC-5511 are monolithic PCM CODECs implemented with double-poly CMOS technology. The HC-5510 is intended for μ-law applications and contains logic for μ-law signaling insertion and extraction. The HC-5511 is intended for A-law applications.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the HC-5510/HC-5511 may be operated in a fixed time slot mode. Both devices are intended to be used with the HC-5512 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smoothes the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Operating Temperature	-25°C to +125°C
Storage Temperature	-65°C to +150°C
V_{CC} with Respect to GNDD	7V
V_{CC} with Respect to V_{BB}	14V
V_{BB} with Respect to GNDD	-7V
Voltage at Any Input or Output	V_{BB} -0.3V to V_{CC} +0.3V
Lead Temperature (Soldering, 10 seconds)	300°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%, V_{BB} = -5.0V ±5%. Typical characteristics are specified at V_{CC} = 5.0V and T_A = 25°C. All digital signals are referenced to GNDD. All analog signals are referenced to GNDA.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
DIGITAL INTERFACE						
I_I	Input Current	-10		10	µA	$0 < V_{IN} < V_{CC}$
V_{IL}	Input Low Voltage			0.6	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output Low Voltage			0.4 0.4 0.4 0.4	V V V V	D_X, I_{OL} = 4.0mA SIG_R, I_{OL} = 0.5mA $\overline{TS}_X$, I_{OL} = 3.2mA, Open Drain PDN, I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4 2.4			V V	D_X, I_{OH} = 6mA SIG_R, I_{OH} = 0.6mA
ANALOG INTERFACE						
Z_I	VF_X Input Impedance when Sampling	2.0			kΩ	Resistance in Series with Approximately 70pF
Z_O	Output Impedance at VF_R			10		-3.1V < VF_R < 3.1V
V_{OS}	Output Offset Voltage at VF_R	-25		25	mV	D_R = PCM Zero Code, HC-5510 or Alternating ±1 Code, HC-5511
I_{IN}	Analog Input Bias Current	-0.1		0.1	µA	V_{IN} = 0V
R1 x C1	DC Blocking Time Constant	4.0			ms	
C1	DC Blocking Capacitor	0.1			µF	
R1	Input Bias Resistor			50	kΩ	
POWER DISSIPATION						
I_{CC0}	Standby Current, V_{CC}		0.1	0.4	mA	
I_{BB0}	Standby Current, V_{BB}		0.0	0.1	mA	
I_{CC1}	Operating Current, V_{CC}		4.5	8.0	mA	
I_{BB1}	Operating Current, V_{BB}		4.5	8.0	mA	

AC ELECTRICAL CHARACTERISTICS Unless otherwise noted, the analog input is a 0dBm0, 1.02kHz sine wave. The digital input is a PCM bit stream generated by passing a 0dBm0, 1.02kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

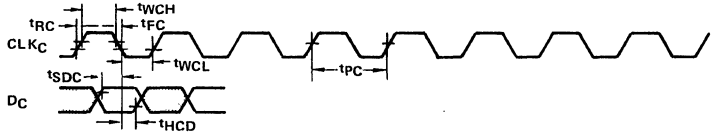
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
	Absolute Level					The nominal 0dBm0 levels for the HC-5510 and HC-5511 are 1.520 Vrms and 1.525 Vrms respectively. The resulting nominal overload level is 3.096V peak for both devices. All gain measurements for the encode and decode portions of the HC-5510/ HC-5511 are based on these nominal levels after the necessary sin x/x corrections are made.
G_{RA}	Receive Gain, Absolute	-0.1		0.1	dB	T = 25°C, V_{CC} =+5V,V_{BB} = -5V
G_{RAT}	Absolute Receive Gain Variation with Temperature	-0.05		0.05	dB	T = 0°C to 70°C
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	-0.07		0.07	dB	V_{CC} = 5V ±5%, V_{BB} =-5V±5%
G_{XA}	Transmit Gain, Absolute	-0.1		0.1	dB	T = 25°C, V_{CC} = 5V, V_{BB} = -5V
G_{XAT}	Absolute Transmit Gain Variation with Temperature	-0.05		0.05	dB	T = 0°C to 70°C
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	-0.07		0.07	dB	V_{CC} = 5V ±5%, V_{BB} = -5V ±5%
G_{RAL}	Absolute Receive Gain Variation with Level					CCITT Method 2 Relative to -10dBm0
		-0.3		0.3	dB	0dBm0 to 3dBm0
		-0.2		0.2	dB	-40dBm0 to 0dBm0
		-0.4		0.4	dB	-50dBm0 to -40dBm0
		-1.0		1.0	dB	-55dBm0 to -50dBm0
G_{XAL}	Absolute Transmit Gain Variation with Level					CCITT Method 2 Relative to -10dBm0
		-0.3		0.3	dB	0dBm0 to 3dBm0
		-0.2		0.2	dB	-40dBm0 to 0dBm0
		-0.4		0.4	dB	-50dBm0 to -40dBm0
		-1.0		1.0	dB	-55dBm0 to -50dBm0
S/D_R	Receive Signal to Distortion Ratio					Sinusoidal Test Method Input Level
		35			dBc	-30dBm0 to 0dBm0
		29			dBc	-40dBm0
		25			dBc	-45dBm0
S/D_X	Transmit Signal to Distortion Ratio					Sinusoidal Test Method Input Level
		35			dBc	-30dBm0 to 0dBm0
		29			dBc	-40dBm0
		25			dBc	-45dBm0
N_R	Receive Idle Channel Noise			0	dBnrc0	D_R = Steady State PCM Code
N_X	Transmit Idle Channel Noise			13	dBrnc0	HC-5510, VF_X = 0V (no signalling)
				-67	dBm0p	HC-5511, VF_X = 0V
HD_R	Receive Harmonic Distortion			-47	dB	2nd or 3rd Harmonic
HD_X	Transmit Harmonic Distortion			-47	dB	2nd or 3rd Harmonic
$PPSR_R$	Positive Power Supply Rejection, Receive	40			dB	D_R = Steady PCM Code, V_{CC} = 5.0V_{DC} +20mVrms, f = 1.02kHz
$PPSR_X$	Positive Power Supply Rejection, Transmit	50			dB	Input Level = 0V, V_{CC} = 5.0V_{DC} +20mVrms, f = 1.02kHz
$NPSR_R$	Negative Power Supply Rejection, Receive	45			dB	D_R = Steady PCM Code, V_{BB} = -5.0V_{DC} +20mVrms, f = 1.02kHz
$NPSR_X$	Negative Power Supply Rejection Transmit	50			dB	Input Level = 0, V_{BB} = -5.0V_{DC} +20mVrms, f = 1.02kHz
CT_{XR}	Transmit to Receive Crosstalk			-75	dB	D_R = Steady PCM Code
CT_{RX}	Receive to Transmit Crosstalk			-70	dB	Transmit Input Level = 0V

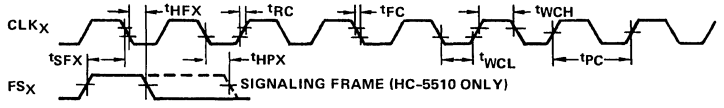
TIMING SPECIFICATIONS

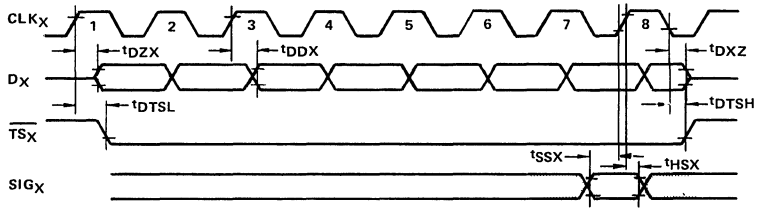
Unless otherwise noted, T_A = 0°C to 70°C, V_{CC} = 5.0 ±5%, V_{BB} = -5.0 ±5%. All digital signals are referenced to GNDD and measured at V_{IL} and V_{IH} levels as indicated in the timing waveforms.

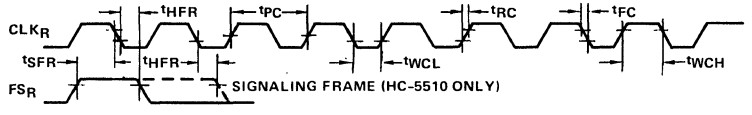
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
t_{PC}	Period of Clock	488			ns	CLK_C, CLK_R, CLK_X
t_{RC}, t_{FC}	Rise and Fall Time of Clock			30	ns	CLK_C, CLK_R, CLK_X
t_{WCH}	Width of Clock High	165			ns	CLK_C, CLK_R, CLK_X
t_{WCL}	Width of Clock Low	165			ns	CLK_C, CLK_R, CLK_X
$t_{A/D}$	A/D Conversion Time			16	Time Slots	From End of Encoder Time Slot to Completion of Conversion
$t_{D/A}$	D/A Conversion Time			2	Time Slots	From End of Decoder Time Slot to Transition of VF_R
t_{SDC}	Set-Up Time, D_C to CLK_C	100			ns	
t_{HDC}	Hold Time, CLK_C to D_C	100			ns	
t_{SFC}	Set-Up Time FS_X or CLK_X	100			ns	
t_{HFX}	Hold Time, CLK_X to FS_X	100			ns	
t_{DZX}	Delay Time to Enable D_X on TS Entry			125	ns	C_L = 150pF
t_{DDX}	Delay Time, CLK_X to D_X			125	ns	C_L = 150pF
t_{DXZ}	Delay Time, D_X to High Impedance State on TS Exit	50		165	ns	C_L = 0pF
t_{DTSL}	Delay to $\overline{TS}_X$ Low	30		185	ns	$0 \leq C_L \leq 150pF$
t_{DTSH}	Delay to $\overline{TS}_X$ Off	30		185	ns	C_L = 0pF
t_{SSX}	Set-Up Time, SIG_X to CLK_X	100			ns	
t_{HSX}	Hold Time, CLK_X to SIG_X	100			ns	
t_{SFR}	Set-Up Time, FS_R to CLK_R	100			ns	
t_{HFR}	Hold Time, CLK_R to FS_R	100			ns	
t_{SDR}	Set-Up Time, D_R to CLK_R	40			ns	
t_{HDR}	Hold Time, CLK_R to D_R	30			ns	
t_{DSR}	Delay Time, CLK_R to SIG_R			300	ns	C_L = 100pF

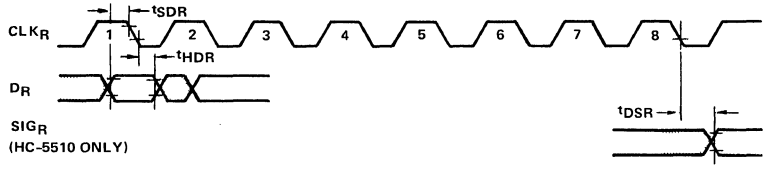
TIMING WAVEFORMS





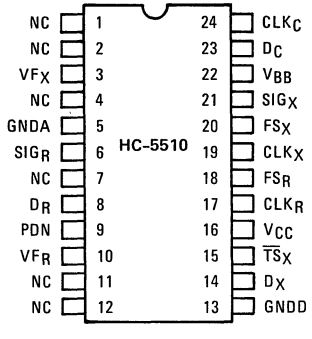




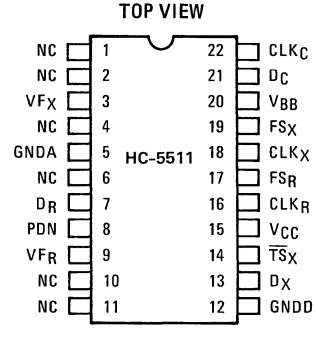


PINOUTS

TOP VIEW



TOP VIEW



HC-5510

PIN NO.	SYMBOL	DESCRIPTION
1	NC	Unused
2	NC	Unused
3	VR_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin.
6	SIG_R	Receive signaling bit output. During receive signaling frames the least significant (last) bit shifted into D_R is internally latched and appears at this output-SIG_R will then remain valid until changed during a subsequent receive signaling frame or reset by a power-down command.
7	NC	Unused
8	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
9	PDN	TTL output level which goes high when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
10	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15μs after the end of the decode time slot.
11	NC	Unused
12	NC	Unused
13	GNDD	Digital ground. All digital levels are referenced to this pin.
14	D_X	Serial PCM "Three-State" output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
15	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external "Three-State" bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
16	V_{CC}	5V (±5%) input.
17	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_X or CLK_C.
18	FS_R	Decoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.
19	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_R or CLK_C.
20	FS_X	Encoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_X to two or more cycles of CLK_X signifies a transmit signaling frame.
21	SIG_X	Transmit signaling input. During a transmit signaling frame, the signal at SIG_X is shifted out of D_X in place of the least significant (last) bit of PCM data.
22	V_{BB}	-5V (±5%) input.
23	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
24	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlay a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the HC-5510/HC-5511 into the fixed time slot mode.

HC-5511

PIN NO.	SYMBOL	DESCRIPTION
1	NC	Unused
2	NC	Unused
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	GNDA	Analog ground. All analog signals are referenced to this pin.
6	NC	Unused
7	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into DR, most significant bit first, on the falling edge of CLK_R.
8	PDN	Open drain output which turns off when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
9	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15μs after the end of the decode time slot.
10	NC	Unused
11	NC	Unused
12	GNDD	Digital ground. All digital levels are referenced to this pin.
13	D_X	Serial PCM "Three-State" output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most signficant bit first, on the rising edge of CLK_X.
14	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external "Three-State" bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
15	V_{CC}	5V (±5%) input.
16	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_X or CLK_C.
17	FS_R	Decoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_R cycle wide.
18	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536MHz, 1.544MHz, or 2.048MHz. May be asynchronous with CLK_R or CLK_C.
19	FS_X	Encoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_X cycle wide.
20	V_{BB}	-5V (±5%) input.
21	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
22	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the HC-5510/HC-5511 into the fixed time slot mode.

Power-Up

Upon application of power, internal circuitry initializes the CODEC and places it into the power-down mode. No sequencing of 5V or -5V is required. In the power-down mode, all non-essential circuits are deactivated, the Three-State PCM data output D_X is placed in the high impedance state and the receive signaling output of the HC-5510, SIG_R, is reset to logical zero. Once in the power-down mode, the method of activating the HC-5510/5511 depends on the chosen mode of operation, time slot assignment or fixed time slot.

Time Slot Assignment Mode

The time slot assignment mode of operation is selected by maintaining CLK_C in a normally low state. The state of the CODEC is updated by pulsing CLK_C eight times within a period of 125 μs or less. The falling edge of each clock pulse shifts the data on the D_C input into the CODEC. The first two control bits determine if the subsequential control bits B3-B8 are to specify the time slot for the encoder (B1 = 0), the decoder (B2 = 0) or both (B1 and B2 = 0) or if the CODEC is to be placed into the power-down mode (B1 and B2 = 1). The desired action will take place upon the occurrence of the second frame sync pulse following the first pulse of CLK_C. Assigning a time slot to either the encoder or decoder will automatically power-up the entire CODEC circuit. The D_X output and D_R input, however, will be inhibited for one additional frame to allow the analog circuitry time to stabilize. If separate time slots are to be assigned to the encoder and the decoder, the encoder time slot should be assigned first. This is necessary because up to four frames are required to assign both time slots separately, but only three frames are necessary to activate the D_X output. If the encode time slot has not been updated the PCM data will be outputed during the previously assigned time slot which may now be assigned to another CODEC.

Fixed Time Slot Mode

There are several ways in which the HC-5510/5511 may operate in the fixed time slot mode. The first and easiest method is to leave CLK_C disconnected or to connect CLK_C to V_{CC}. In this situation, D_C behaves as a power-down input. When D_C goes low, both encode and decode time slots are set to one on the second subsequent frame sync pulse. Time slot one corresponds to the eight CLK_X or CLK_R cycles starting one cycle from the nominal leading edge of FS_X or FS_R respectively. As in the time slot assignment mode, the D_X output is inhibited for one additional frame after the circuit is powered up. A logical "1" on D_C powers the CODEC down on the second subsequent FS_X pulse.

A second fixed time slot method is to operate CLK_C continuously. Placing a "1" on D_C will then cause the serial control register to fill up with ones. With B1 and B2 equal to "1" the CODEC will power-down. Placing a "0" on D_C will cause the serial control register to fill up with zeroes, assigning time slot one to both the encoder and decoder and powering up the device. One important restriction with this method of operation is that the rising transition of D_C must occur at least 8 cycles of CLK_C prior to FS_X. If this restriction is not followed, it is possible that on the frame prior to power-down, the encoder could be assigned to an incorrect time slot (e.g., 1, 3, 7, 15 or 31), resulting in a possible PCM bus conflict.

Serial Control Port

When the HC-5510/HC-5511 is operated in the time slot assignment mode or the fixed time slot mode with continuous clock, the data on D_C is shifted into the serial control register, bit 1 first. In the time slot assignment mode, depending on B1 and B2, the data in the RCV or XMT time slot registers is updated at the second FS_R or FS_X pulse after the first CLK_C pulse, or the CODEC is powered down. In the continuous clock fixed time slot mode, the CODEC is powered up or down at every second FS_R or FS_X pulse. The control register data is interpreted as follows:

B1	B2	ACTION
0	0	Assign Time Slot to Encoder and Decoder
0	1	Assign Time Slot to Encoder
1	0	Assign Time Slot to Decoder
1	1	Power-Down CODEC

B3	B4	B5	B6	B7	B8	TIME SLOT
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	63
1	1	1	1	1	1	64

During the power-down command, bits 3 through 8 are ignored. Note that with 64 possible time slot assignments it is frequently possible to assign a time slot which does not exist. This can be useful to disable an encoder or decoder without powering down the CODEC.

Signaling

The HC-5510 μ-law CODEC contains circuitry to insert and extract signaling information for the PCM data. The transmit signaling frame is signified by widening the FS_X pulse from one cycle of CLK_X to two or more cycles.

When this occurs, the data present on the SIG_X input at the eighth clock pulse of the encode time slot is inserted into the last bit of the PCM data stream. A receive signaling frame is indicated in a similar fashion by widening the FS_R pulse to two or more cycles of CLK_R.

During a receive signaling frame, the last PCM bit shifted in is latched into a flip-flop and appears at the SIG_R output. This output will remain unchanged until the next signaling frame, until a power-down is executed or until power is removed from the device. Since the least significant bit of the PCM data is lost during a signaling frame, the decoder interprets the bit as a "1/2" (i.e., half way between a "0" and a "1"). This minimizes the noise and distortion due to the signaling.

FUNCTIONAL DESCRIPTION (Continued)

Encoding Delay

The encoding process begins immediately at the end of the encode time slot and is concluded no later than 17 time slots later. In normal applications, this PCM data is not shifted out until the next time slot 125 μs later, resulting in an encoding delay of 125μs. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048MHz clock, the FS rate could be increased to 15kHz reducing the delay from 125μs to 67μs.

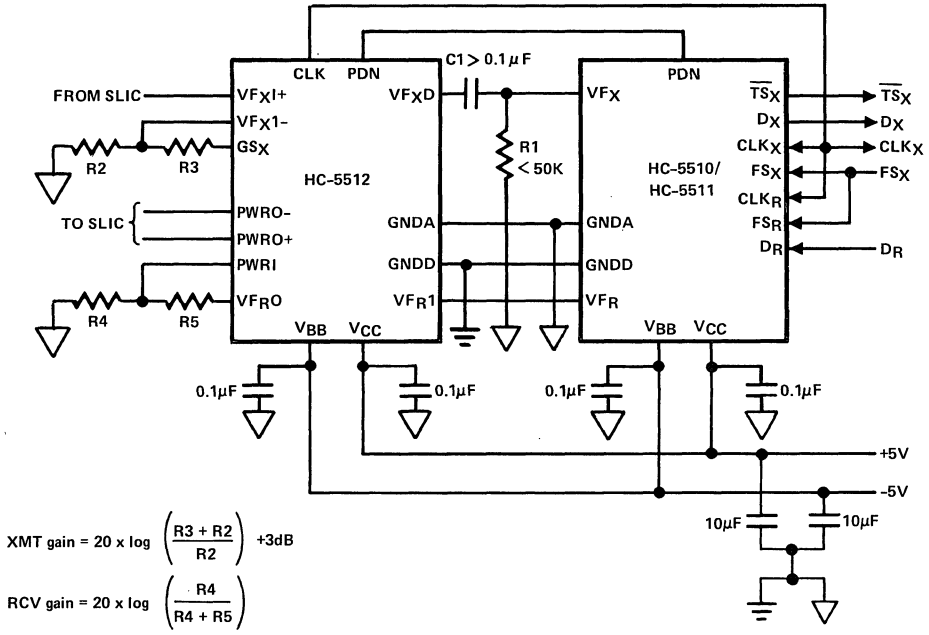
Decoding Delay

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 CLK_R cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or 81μs for a 1.544MHz system with an 8kHz frame rate or 76μs for a 2.048MHz system with an 8kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

Typical Application

A typical application of the HC-5510/HC-5511 used in conjunction with the HC-5512 PCM filter is shown. The values of resistor R1 and D_C blocking capacitor C1, are noncritical. The capacitor value should exceed 0.1μF, R1 should be less than 50kΩ , and the product R1 x C1 should exceed 4ms.

TYPICAL APPLICATION



The power supply decoupling capacitors should be 0.1μF. In order to take advantage of the excellent noise performance of the HC-5510/HC5511/HC-5512, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines.

HARRIS

HC-5512/5512A

PCM Monolithic Filter

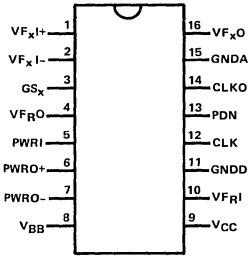
FEATURES

- EXCEEDS ALL D3/D4 AND CCITT SPECIFICATIONS
- +5V, -5V POWER SUPPLIES
- LOW POWER CONSUMPTION:
  - 45mW (600Ω 0dBm LOAD)
  - 30mW (POWER AMPS DISABLED)
- POWER DOWN MODE: 0.5mW
- 20dB GAIN ADJUST RANGE
- NO EXTERNAL ANTI-ALIASING COMPONENTS
- SIN x/x CORRECTION IN RECEIVE FILTER
- 50/60Hz REJECTION IN TRANSMIT FILTER
- TTL AND CMOS COMPATIBLE LOGIC
- ALL INPUT PROTECTED AGAINST STATIC DISCHARGE DUE TO HANDLING

PINOUT

DUAL-IN-LINE PACKAGE
TOP VIEW

Section 11 for Packaging



DESCRIPTION

The HC-5512/HC-5512A filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8kHz sampled systems.

The filter is manufactured using double-poly silicon gate CMOS technology. Switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200Hz and above 3.4kHz.

RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

FUNCTIONAL DIAGRAM

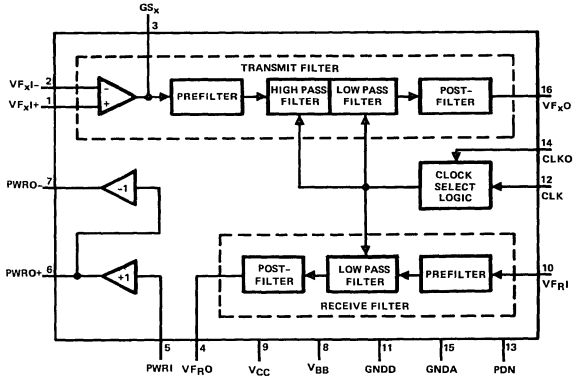


FIGURE 1

6

ABSOLUTE MAXIMUM RATINGS

Supply Voltages	±7V
Power Dissipation	1W/Package
Input Voltage	±7V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	-25°C to +125°C
Storage Temperature	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A = 0°C to 70°C, V_{CC} = 5.0V±5%, V_{BB} = 5.0V±5%, clock frequency is 2.048 MHz. Typical parameters are specified at T_A = 25°C, V_{CC} = 5.0V, V_{BB} = -5.0V. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	µA
I_{BB0}	V_{BB} Standby Current	PDN = V_{DD}, Power Down Mode		50	100	µA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	4.0	mA
I_{CC2}	V_{CC} Operating Current	Note 1		4.6	6.4	mA
I_{BB2}	V_{BB} Operating Current	Note 1		4.6	6.4	mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	$V_{BB} \le V_{IN} \le V_{CC}$	-10		10	µA
I_{INP}	Input Current, PDN	$V_{BB} \le V_{IN} \le V_{CC}$	-100			µA
I_{IN0}	Input Current, CLK0	$V_{BB} \le V_{IN} \le V_{CC} - 2V$	-10		-0.1	µA
V_{IL}	Input Low Voltage, CLK, PDN		0		0.8	V
V_{IH}	Input High Voltage, CLK, PDN		2.2		V_{CC}	V
V_{IL0}	Input Low Voltage, CLK0		V_{BB}		V_{BB}+0.5	V
V_{II0}	Input Intermediate Voltage, CLK0		-0.8		0.8	V
V_{IH0}	Input High Voltage, CLK0		V_{CC}-0.5		V_{CC}	V
TRANSMIT INPUT OP AMP						
$IB_x I$	Input Leakage Current, $VF_x I$	$V_{BB} \le VF_x I \le V_{CC}$	-100		100	nA
$RI_x I$	Input Resistance, $VF_x I$	$V_{BB} \le VF_x I \le V_{CC}$	10			MΩ
$VOS_x I$	Input Offset Voltage, $VF_x I$	$-2.5V \le V_{IN} \le +2.5V$	-20		20	mV
V_{CM}	Common-Mode Range, $VF_x I$		-2.5		2.5	V
CMRR	Common-Mode Rejection Ratio	$-2.5V \le V_{IN} \le 2.5V$	60			dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}		60			dB
R_{OL}	Open Loop Output Resistance, GS_x			1		kΩ
R_L	Minimum Load Resistance, GS_x		10			kΩ
C_L	Maximum Load Capacitance, GS_x				25	pF
$VO_x I$	Output Voltage Swing, GS_x	$R_L \ge 10k$	±2.5			V
A_{VOL}	Open Loop Voltage Gain, GS_x	$R_L \ge 10k$	5,000			V/V
F_c	Open Loop Unity Gain Bandwidth, GS_x			2		MHz

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_A = 25°C. All parameters are specified for a signal level of 0 dBm0 at 1KHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT FILTER (Transmit filter input op amp set to the non-inverting unity gain mode, with VF_xI = 1.1 Vrms unless otherwise noted.)						
RL_x	Minimum Load Resistance, VF_xO		10			kΩ
CL_x	Load Capacitance, VF_xO				25	pF
RO_x	Output Resistance, VF_xO			1	3	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_xO	f = 1 kHz, VF_xI+ = 0 Vrms	30			dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO	Same as Above	35			dB
GA_x	Absolute Gain	f = 1 kHz (HC-5512A)	2.9	3.0	3.1	dB
		f = 1 kHz (HC-5512)	2.875	3.0	3.125	dB
GR_x	Gain Relative to GA_x	Below 50 Hz			−35	dB
		50 Hz		−41	−35	dB
		60 Hz		−35	−30	dB
		200 Hz (HC-5512A)	−1.5		0	dB
		200 Hz (HC-5512)	−1.5		0.05	dB
		300 Hz to 3 kHz (HC-5512A)	−0.125		0.125	dB
		300 Hz to 3 kHz (HC-5512)	−0.15		0.15	dB
		3.3 kHz	−0.35		0.03	dB
		3.4 kHz	−0.70		−0.1	dB
		4.0 kHz		−15	−14	dB
		4.6 kHz and Above			−32	dB
DA_x	Absolute Delay at 1 kHz				230	μs
DD_x	Differential Envelope Delay from 1 kHz to 2.6 kHz				60	μs
DP_x1	Single Frequency Distortion Products				−48	dB
DP_x2	Distortion at Maximum Signal Level	0.16 Vrms, 1 kHz Signal Applied to VF_xI+, Gain = 20 dB, R_L = 10k			−45	dB
NC_x1	Total C Message Noise at VF_xO			2	5	dBrnc0
NC_x2	Total C Message Noise at VF_xO	Gain Setting Op Amp at 20 dB, Non-Inverting, Note 3 T_A = 0°C to 70°C		3	6	dBrnc0
GA_xT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain	V_{CC} = 5.0V ± 5% V_{BB} = −5.0V ± 5%		0.01		dB/V
CT_{RX}	Crosstalk, Receive to Transmit $20 \log \frac{VF_xO}{VF_RO}$	Receive Filter Output = 2.2 Vrms VF_xI+ = 0 Vrms, f = 0.2 kHz to 3.4 kHz Measure VF_xO			−70	dB
GR_xL	Gaintracking Relative to GA_x	Output Level = +3 dBm0	−0.1		0.1	dB
		+2 dBm0 to −40 dBm0	−0.05		0.05	dB
		−40 dBm0 to −55 dBm0	−0.1		0.1	dB

ELECTRICAL CHARACTERISTICS (Continued)

Unless otherwise specified, T_A = 25°C. All parameters are specified for a signal level of 0 dBm0 at 1KHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.6 Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-3.2V \le V_{IN} \le 3.2V$	−100		100	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	3	Ω
CL_R	Load Capacitance, VF_RO				25	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1 kHz	35			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	−200		200	mV
GA_R	Absolute Gain	f = 1 kHz (HC-5512A) f = 1 kHz (HC-5512)	−0.1 −0.125	0 0	0.1 0.125	dB dB
GR_R	Gain Relative to Gain at 1 kHz	Below 300 Hz 300 Hz to 3.0 kHz (HC-5512A) 300 Hz to 3.0 kHz (HC-5512) 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	 −0.125 −0.15 −0.35 −0.7		0.125 0.125 0.15 0.03 −0.1 −14 −32	dB dB dB dB dB dB dB
DA_R	Absolute Delay at 1 kHz				100	μs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz				100	μs
DP_R1	Single Frequency Distortion Products	f = 1 kHz			−48	dB
DP_R2	Distortion at Maximum Signal Level	2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, R_L = 10k			−45	dB
NC_R	Total C-Message Noise at VF_RO			3	5	dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_xO}$	Transmit Filter Output = 2.2 Vrms VF_RI = 0 Vrms, f = 0.3 kHz to 3.4 kHz Measure VF_RO			−70	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0 Note 5	−0.1 −0.05 −0.1		0.1 0.05 0.1	dB dB dB

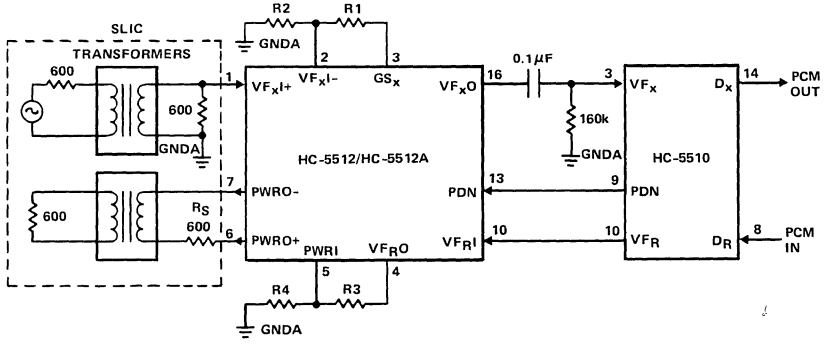
AC Electrical Characteristics (Continued)

Unless otherwise specified, T_A =25°C. All parameters are specified for a signal level of 0 dBm0 at 1kHz. The 0dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	$-3.2V \le V_{IN} \le 3.2V$	0.1		3	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO +, PWRO –	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO +, PWRO –				500	pF
GA_P+	Gain, PWRI to PWRO +	R_L = 600Ω Connected Between		1		V/V
GA_P-	Gain, PWRI to PWRO –	PWRO + and PWRO –, Input Level = 0 dBm0 (Note 4)		–1		V/V
GR_PL	Gaintracking Relative to 0 dBm0 Output Level	V = 2.05 Vrms, R_L = 600Ω (Notes 4, 5)	– 0.1		0.1	dB
		V = 1.75 Vrms, R_L = 300Ω	– 0.1		0.1	dB
S/D_P	Signal/Distortion	V = 2.05 Vrms, R_L = 600Ω (Notes 4, 5)			– 45	dB
		V = 1.75 Vrms, R_L = 300Ω			– 45	dB
VOSP	Output DC Offset, PWRO +, PWRO –	PWRI Connected to GNDA	– 50		50	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	45			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power amplifier. The specification listed assumes 0 dBm is delivered to 600Ωconnected from PWRO+ to PWRO–.
Note 2: Voltage input to receive filter at 0V VF_RO connected to PWRI, 600Ω from PWRO+ to PWRO–. Output measured from PWRO+ to PWRO–.
Note 3: The 0dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.
Note 4: The odBm0 level for the power amplifiers is load dependent. For R_L = 600 to GNDA the 0dBm0 level is 1.43 Vrms measured at the amplifier output for R_L = 3000 the 0dBm0 level is 1.22Vrms.
Note 5: VF_RO connected to PWRI, input signal applied to VF_RI.

INTERFACE CIRCUIT FOR HC-5510 CODEC



Note 1 Transmit voltage gain = $\frac{R1 + R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3dB gain) (R1 +R2 ≥ 10k).

Note 2. Receive gain = $\frac{R4}{R3 + R4}$
(R3 +R4 ≥ 10k)

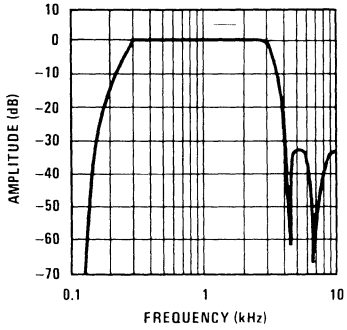
Note 3 In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a signal level of 8.5dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1dBm across a 600Ω termination impedance.

DESCRIPTION OF PIN FUNCTIONS

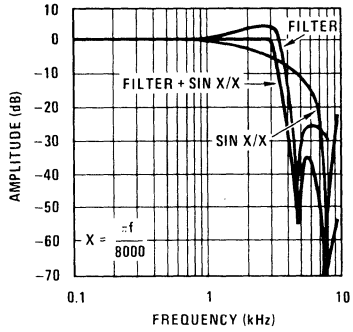
Pin No.	Name	Function
1	VF_xI+	The non-inverting input to the transmit filter stage.
2	VF_xI-	The inverting input to the transmit filter stage.
3	GS_x	The output used for gain adjustments of the transmit filter.
4	VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
5	PWRI	The input to the receive filter differential power amplifier.
6	PWRO+	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
7	PWRO–	The inverting output of the receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
8	V_{BB}	The negative power supply pin. Recommended input is –5V.
9	V_{CC}	The positive power supply pin. The recommended input is 5V.
10	VF_RI	The input pin for the receive filter stage.
11	GNDD	Digital ground input pin. All digital signals are referenced to this pin.
12	CLK	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
13	PDN	The input pin used to power down the HC-5512 during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
14	CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency: **CLK** **Connect CLK0 to:** 2048 kHz V_{CC} 1544 kHz GNDD 1536 kHz V_{BB} An internal pull-up is provided.
15	GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
16	VF_xO	The output of the transmit filter stage.

TYPICAL PERFORMANCE CHARACTERISTICS

Transmit Filter Stage



Receive Filter Stage



FUNCTIONAL DESCRIPTION

The HC-5512 monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/ Select Logic *(Figure 1)*. A brief description of the operation for each section is provided below.

Transmit Filter

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10MΩ , a voltage gain of greater than 10,000, low power consumption (less than 3mW), high power supply rejection, and is capable of driving a 10kΩ load in parallel with up to 25pF. The inputs and output of the amplifier are accessible for added flexibility. Noninverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40dB. The output of the transmit filter is capable of driving a ±3.2V peak to peak signal into a 10kΩ load in parallel with up to 25pF.

Receive Filter

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband reejction and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

Receive Filter Power Amplifiers

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain settling resistors, R3, R4 *(Figure 2)*. The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10mW-20mW depending on output signal amplitude.

Power Down Control

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1mW and clamp the power amplifier output to V_{BB}. Connect PDN to GNDD for normal operation.

Frequency Divider and Select Logic Circuit

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048MHz, 1.544MHz or 1.536MHz clock frequencies. By connecting the frequency select pin CLK0 (pin 14) to V_{CC}, a 2.048MHz clock input frequency is selected. Digital ground selects 1.544MHz and V_{BB} selects 1.536MHz.

APPLICATIONS INFORMATION

Gain Adjust

Figure 2 shows the signal path interconnections between the HC-5512 and HC-5510 single channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

Optimum noise and distortion performance will be obtained for the HC-5512/HC-5512A filter when operated with system peak overload voltages of +2.5V to +3.2V at VF_XO and VF_RO. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

For example, the HC-5512 filter can be used with the HC-5510/5511 series CODEC which has a 5.5V peak overload voltage. A gain stage following the transmit filter output and an attenuation stage following the CODEC output are required.

Board Layout

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between GNDA and GNDD and between the GNDA traces of adjacent filters and CODECs.

HARRIS

ADVANCE

HC-5531

Automatic Line Balance Network

FEATURES

- MONOLITHIC LSI DEVICE
- NO EXTERNAL COMPONENTS REQUIRED
- AUTOMATIC SELECTION OF BALANCE NETWORK FOR LOADED AND NON-LOADED LOOPS
- SOFTWARE CONTROLLED LOSS IN .1dB STEPS
- SOFTWARE CONTROLLED GAIN/LOSS IN .1 dB STEPS
- LOW POWER CONSUMPTION CMOS PROCESS
- COMPATIBLE WITH EXISTING MONOLITHIC PCM CHANNEL FILTERS
- COMPATIBLE WITH TRANSFORMER-COUPLED OR SOLID-STATE SLIC's

APPLICATION

- DIGITAL TELEPHONE SWITCHES
- 2-4 WIRE JUNCTIONS

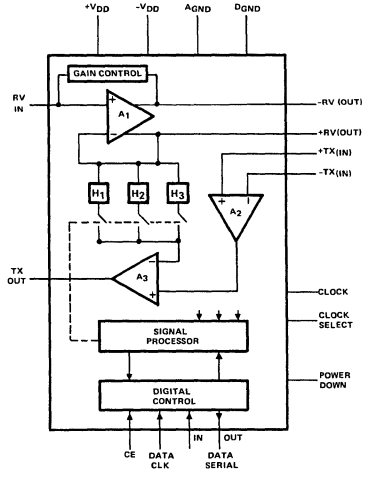
DESCRIPTION

The HARRIS HC-5531 Automatic Line Balance Network (ALBN) is a monolithic LSI device for application in digital telephone switches.

The device incorporates the elements required to perform the automatic balancing of the loop using samples of the receive and transmit signals. A signal processor selects the appropriate balance network which provides maximum transhybrid loss for either loaded or non-loaded subscriber loops. This type of compensation is essential to maintain necessary singing margin in a zero dB loss digital switch. A digitally controlled attenuator in the receive path with 1dB steps allows loss insertion to be performed in the line card. Gain/loss control in .1dB steps for fine adjustment is also available.

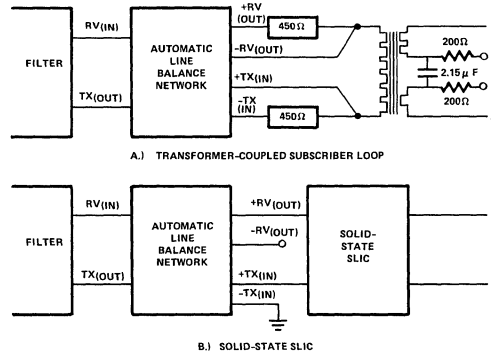
The HARRIS ALBN enhances the transmission performance of digital telephone switches by minimizing the singing margin of a connection through automatic selection of balance networks.

PIN ASSIGNMENTS



FUNCTIONAL DIAGRAM SHOWING PIN ASSIGNMENTS (HC-5531)

INSTALLATION DIAGRAM



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PARAMETER	TYPICAL VALUE	UNIT	NOTE
Supply Voltage	+5, -5	Volts	
Return Loss Cable: 1650Ω/ /0,005μF (loaded) 800Ω/ /.05μF (Nonloaded) 900Ω+2.15μF (standard)	 35 35 35	 dB dB dB	
Insertion Loss Error 0,1,2,3 or 6 dB Setting	±.01	dB	
Fine Gain/Loss Error .1 dB to .5dB in .1 dB Steps	±.01	dB	
Input Impedance (All Analog Inputs)	100	kΩ	
Output Amplifier Maximum Signal Capability	+10	dBm	1
Idle Channel Noise	5	dBrnCo	
Distortion	.1	%	
Power Dissipation Operation: Power Down:	 75 1	 mW mW	 2

NOTES:

1. Receive output driving 450Ω+ 450Ω(Balanced)
2. Same as Note 1 with 0 dBm signal level.

6

HARRIS HV-1000/1005/1010

Induction Motor Energy Saver

Preliminary

FEATURES

- OPERATES DIRECTLY OFF 110/220V AC LINE – NO POWER SUPPLY REQUIRED
- PRODUCES POWER SAVINGS OFF FROM 10% TO 50% FOR MOTORS WITH LIGHT OR VARIABLE LOADS
- SCR OUTPUT STAGE TRIGGERS TRIAC DIRECTLY
- LOAD ANTICIPATOR SENSES SHOCK LOADS AND RESPONDS INSTANTLY WITH FULL POWER
- WITHSTANDS LINE SURGES TO 2000V
- CAUSES MOTOR TO RUN QUIETER, COOLER
- CAN BE MOUNTED INSIDE MOTOR
- NEEDS ONLY 3 RESISTORS, 2 CAPACITORS AND A TRIAC TO ASSEMBLE COMPLETE CONTROLLER

DESCRIPTION

The HV-1000/1005/1010 are energy saving induction motor controller circuits specifically designed for use with 110/220 volt AC single phase induction motors to reduce power consumption.

The controller circuit senses the load on the motor and then controls a TRIAC to apply reduced voltage to lightly loaded motors, full voltage to heavily loaded motors.

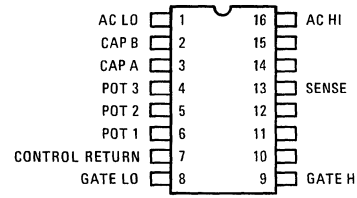
The HV-1000/1005/1010 is available in a 16 lead DIP. Ideal for mounting inside induction motors, it can also be mounted in a heat sunk circuit box for external, after market application.

APPLICATIONS

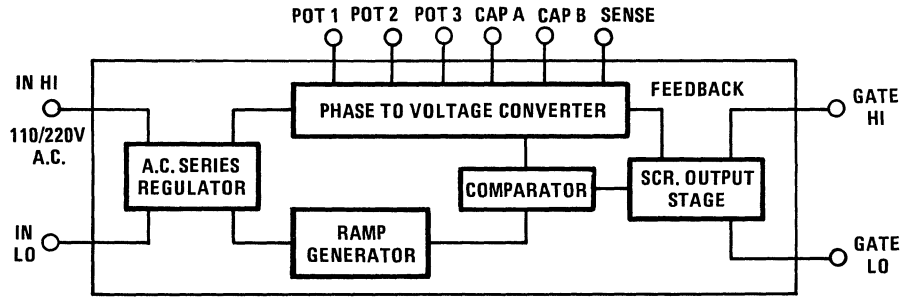
- POWER TOOLS
- WATER PUMPS
- HEAT PUMPS
- PRESSES
- CONVEYORS
- COMPRESSORS
  - ► ANY APPLICATION WHERE FOR SOME OF THE TIME THE MOTOR IS DRIVING LESS THAN ITS RATED LOAD

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Input Voltage (With Input Resistor)	±2000V
Input Voltage (Without Input Resistor)	±600V
Power Dissipation	500mW
Operating Temperature Range	-25°C to +85°C
Storage Temperature	-40°C to +100°C
Lead Temperature (Soldering, 10 seconds)	300°C
Output Current (10 microsecond pulse)	500mA

ELECTRICAL CHARACTERISTICS

These characteristics apply to the HV-1000/1005/1010 operating off 60Hz AC line power. HV-1000/1005/1010 respectively should be selected so that the full load power factor of the controller approximately matches that of the motor. The motor power factor $= \frac{\text{Watts}}{\text{Volt Amperes}}$ at full load, which should be measured experimentally.

FULL LOAD POWER FACTOR		
HV-1000	HV-1005	HV-1010
.86	.78	.68

PARAMETER	MINIMUM	MAXIMUM	UNITS
Difference Between Positive and Negative Triggering Times, Measured from Line Voltage Zero Crossing		75	μsec
Output Stage Breakover Voltage	±600		V

NOTES:

1. Selection of HV-1000/1005/1010 by matching the full load power factor of the motor to that of the controller ensures that the controller will apply full voltage to the motor at its full rated load. At reduced loads, the controller will then apply appropriately reduced voltage to the motor so that its power consumption is reduced.

2. No guarantee of power savings can be given since the savings achievable depend entirely on the motor and its application. For a motor driving only a flywheel (e.g. a circular saw or a bench grinder) a power reduction of 50% may often be observed when the tool is switched on but not in use. For typical variable load applications, an overall power reduction of 10% is likely to be observed.

TYPICAL APPLICATION CIRCUIT

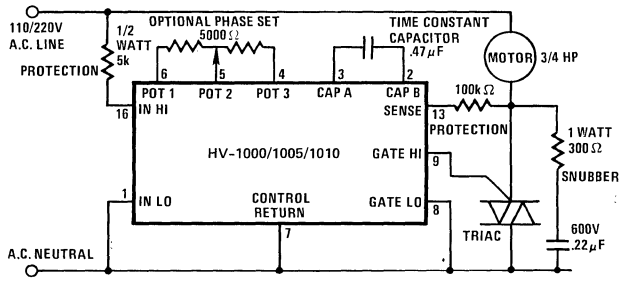


FIGURE 1

NOTES:

1. An optional potentiometer may be attached as shown to any of the three versions of the circuit and used to set the full load power factor. If the potentiometer is omitted, the full load power factor will be as defined in the electrical characteristics. With the potentiometer connected power factor may be adjusted from 0.5 to 0.9 for all three circuits.

2. A small number of motor designs exist which cannot be controlled in a stable fashion by HV-1000/1005/1010. The symptoms of instability are irregular vibration and jerky rotation of the shaft. This instability is seldom observed with motors driving a pulley, flywheel or equivalent inertial load. It may be helped by increasing the inertia in the load driven by the motor. Sometimes the use of either larger or smaller time constant capacitors will also help. Occasionally examination of the waveform across the time constant capacitor with an oscilloscope will show the presence of a low level instability which is usually insignificant. (1) Normally this voltage should be steady when the motor and controller are in equilibrium.

3. The HV-1000/1005/1010 contains a circuit which allows it to respond within one cycle of the power line to a shock load. In this circumstance full power is applied to the motor immediately.

4. The TRIAC should be chosen to have a continuous current rating equal to the current drawn by the motor. In most applications heat sinking will be required to remove the heat produced by the power dissipation of the TRIAC.

5. The snubber circuit is required to prevent the SCR output stage being triggered inadvertently by the voltage transient which would otherwise appear across the TRIAC at the moment of current zero crossing.

6. In the event of a line voltage surge in excess of 600V, a protection SCR between pins 1 and 16 breaks over and latches down to approximately 2V, dropping the surge voltage across the 5K protection resistor. The SCR can withstand 0.4A for 1 millisecond, allowing 2000V surges to be tolerated. The output stage is self protecting since it consists of SCRs which break over and turn on the TRIAC so that the surge voltage is dropped across the motor.

THEORY OF OPERATION

Induction motors run at a speed which depends primarily on the supply frequency, little on voltage. They draw almost a constant current regardless of the load – the motor responds to load with a change in power factor. Thus, a lightly loaded motor wastes energy by heating its windings with inductive current. The HV-1000/1005/1010 measures the load using the current phase angle and then saves power by applying to the motor only sufficient voltage to drive the load. (2) Since the voltage is adjusted by TRIAC phase control a side benefit of the controller is power factor correction.

The controller chip triggers a TRIAC which is in series with the motor. This varies the RMS voltage across the motor. The resulting voltage waveform across the motor is shown at the top of Figure 2. A motor can be characterized by the relation between the two parameters ⊖c and ⊖t, shown in Figure 2 for a typical motor. At point A, the motor is running fully loaded with full voltage applied, as it was designed. At point B, the motor is running lightly loaded with voltage reduced to the point of stalling. The function of the controller is to force the motor to operate along the load line AB, rather than AC which it does naturally. Figure 3 shows an example of the typical power savings which results when the controller chip is incorporated in a motor.

(1) For safety it is recommmended not to connect the ground clip on the scope probe when performing this measurement.
(2) This circuit principle was first described by F. J. Nola in U.S. Pat. 4052648.

The key features of the circuit are firstly that all the analog processing is carried out with the circuitry running entirely on 60Hz alternating current. Direct current is not used at all. Secondly it is integrated using dielectric isolation, with junction breakdowns of 400V. Junctions are stacked in both the input regulator and the SCR output stage so that the composite breakdown voltage of these stages is ±600V.

The analog processing which achieves the control function is explained conceptually in Figure 4. At any given load condition the controller tries to force the motor current phase ⊖c to a pre-programmed set phase. The phase to voltage converter measures the difference between the set phase and ⊖c, and increments a pedestal voltage at a rate proportional to the difference, delaying the trigger point ⊖t where a reference ramp intersects the pedestal. The delayed triggering reduces the voltage applied to the motor, decreasing the motor winding current so that ⊖c is forced to the set phase by the modulation of ⊖t. The set phase is itself a slow function of ⊖t, which produces the sloping controller characteristic of Figure 2. This is achieved via the feedback path from the output stage to the phase to voltage converter.

An additional feature of the phase to voltage converter is the load anticipator. If ⊖c is ever more than 0.5msec less than the set phase, which means the motor has received a sudden heavy load, the full line voltage is immediately applied to the motor. This allows the motor to respond at once to a step function load. If the load is abruptly removed, the controller cuts back the voltage applied to the motor over a time period of typically one second, set by the external time constant capacitor.

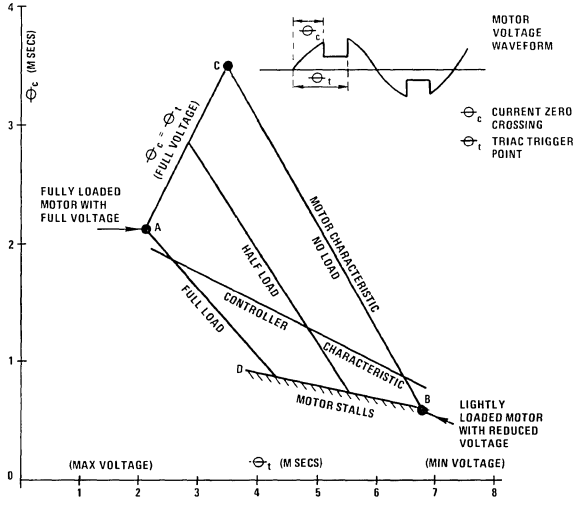


FIGURE 2 – Voltage Waveform Characteristics of a TRIAC Controlled Induction Motor

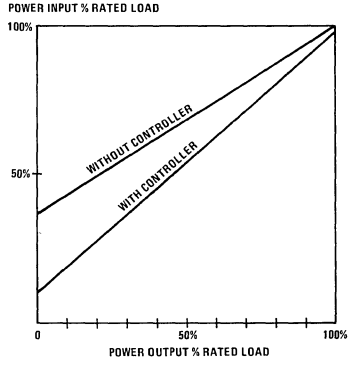


FIGURE 3 – Power Savings as a Function of Load for a 1/3 HP Motor

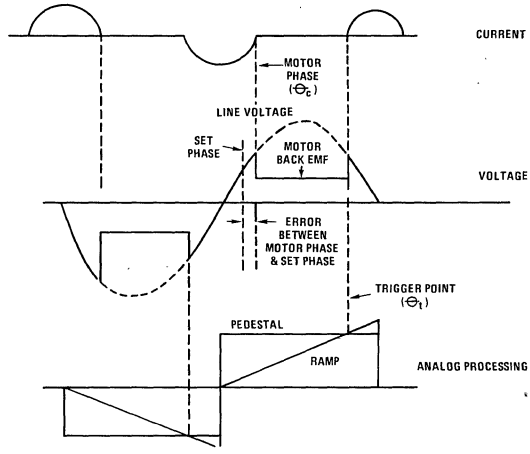


FIGURE 4 – Relation of the Voltage and Current Waveforms to the Analog Processing Function

APPLICATIONS INFORMATION

Improvement of the efficiency of single phase induction motors may be achieved in two ways. For motors which drive a steady load equal to their rated capacity, the best method is to use a run capacitor with an auxiliary winding. This causes the internal field structure of the motor to resemble that of a three phase motor, an inherently more efficient arrangement. However, if a capacitor run motor is used to drive less than its rated load, its power consumption will usually be greater than a motor without a run capacitor, so if this is the case for a significant fraction of the time a run capacitor is not effective for improving efficiency. By contrast an electronic energy saving motor controller produces significant improvements in efficiency for lightly loaded motors and is therefore the best choice for motors which spend a significant part of their time lightly loaded. Electronic energy saving controllers are useful for power tools, water pumps, heat pumps, presses, conveyors, compressors and commercial washing machines, in other words for any application where the load on the motor is either variable or ill defined. Run capacitors are useful for refrigerators, air conditioners, and ventilation fans – all applications where the load on the motor is steady and well defined. An electronic energy saving controller should not be applied in a circumstance where a motor is driving a constant, steady load equal to its rated load. In this circumstance the power dissipated in the TRIACs may actually increase the total power usage. However it sometimes happens that induction motors are relatively conservatively designed, and the real power capability of the motor is greater than that stated. This may come about, for instance, because the motor may have been designed to operate with worst case low line voltage, say, 100V for a nominal 115V motor. In such a circumstance an electronic energy saving controller can produce useful savings because in reality the conservative design of the motor is causing it to be operating at less than its full capability. This circumstance can be tested experimentally by connecting a power meter to the motor and then adjusting the set power factor with a potentiometer on the controller circuit to test whether reduced power consumption can be obtained. Once set up in this way, the controller will continue to give the motor just sufficient voltage to drive the load in hand, even if the line voltage drifts high. In other words, the energy saving controller also acts as a line voltage regulator. This is especially beneficial in areas where the line voltage fluctuates, since high line voltage can cause an induction motor to consume excessive amounts of power.

Harris takes the Total Approach to Hi-Rel

High-Reliability does not occur by accident in microcircuit manufacturing. It can be achieved only as a result of informed planning, precise design, careful manufacturing methods, scrupulously controlled production processes, accurate screening, and exhaustive testing.

In short, reliability must be totally designed and manufactured into the product. It is not a characteristic that can be added after manufacture. It must be part and parcel of the flow from original design through final assembly and test.

The major steps affecting microcircuit reliability are:

- Initial circuit selection and design
- Die layout and geometry
- Raw material inspection and QC
- Wafer/die production process and controls
- Die/package assembly and controls
- Burn-in techniques
- Screening and test procedures

Harris Hi-Rel Flows

Harris recognized early that a single grade of Hi-Rel devices would be inadequate for such varied customer requirements as critical commercial equipment, manned space missions, sensitive industrial systems, exacting avionic instruments and demanding military applications. Realizing, further, that custom-tailoring each product manufacturing flow to meet individual order specfications would result in prohibitive costs, Harris developed and now offers devices in four different standard Hi-Rel grades which, together, will accommodate the requirements of virtually all users.

Not all devices are available in all grades, of course. For up-to-date availability information, refer to the applicable data sheets or contact either the factory or the local Harris Semiconductor representative.

Produced in accordance with different manufacturing flows, the standard Harris Hi-Rel grades and their indicated areas of application are as follows:

7

- **DASH-2 (MIL-STD-883 Class C)** is designed for general use in a military temperature range environment. Performance is guaranteed over a temperature range of $-55°C$ to $+125°C$.

- **DASH-8 (MIL-STD-883 Class B)** provides the same basic screening flow as DASH-2 with the addition of a 160-hour burn-in. The burn-in cycle results in accelerated failure of marginal devices or those which may be subject to infant mortality. DASH-8 is intended to be used in general-purpose Hi-Rel applications.

Note the DASH-2 and DASH-8 product are not fully defined by goverment specifications as is JAN Class B. DASH-2 and DASH-8 are tested electrically per the criteria defined in the applicable Harris data sheet.

- **DASH-7** is a DASH-8 equivalent for commerical applications. DASH-7 receives a 96-hour burn-in and is tested over the $0°C$ to $+75°C$ operating range. DASH-7 screening is available on Harris Linear Circuits only.

- **JAN Class B** - Most military weapons systems and certain other military hardware use JAN Class B microcircuits. JAN Class B devices receive essentially the same environmental/mechanical screening as Harris DASH-8 products. JAN Class B circuits, in addition, are purchased to a MIL-M-38510 Slash Sheet, which calls out stringent electrical screening and an extensive system of manufacturing controls, reliability and Quality Assurance procedures.

Advantages of Standard Flows

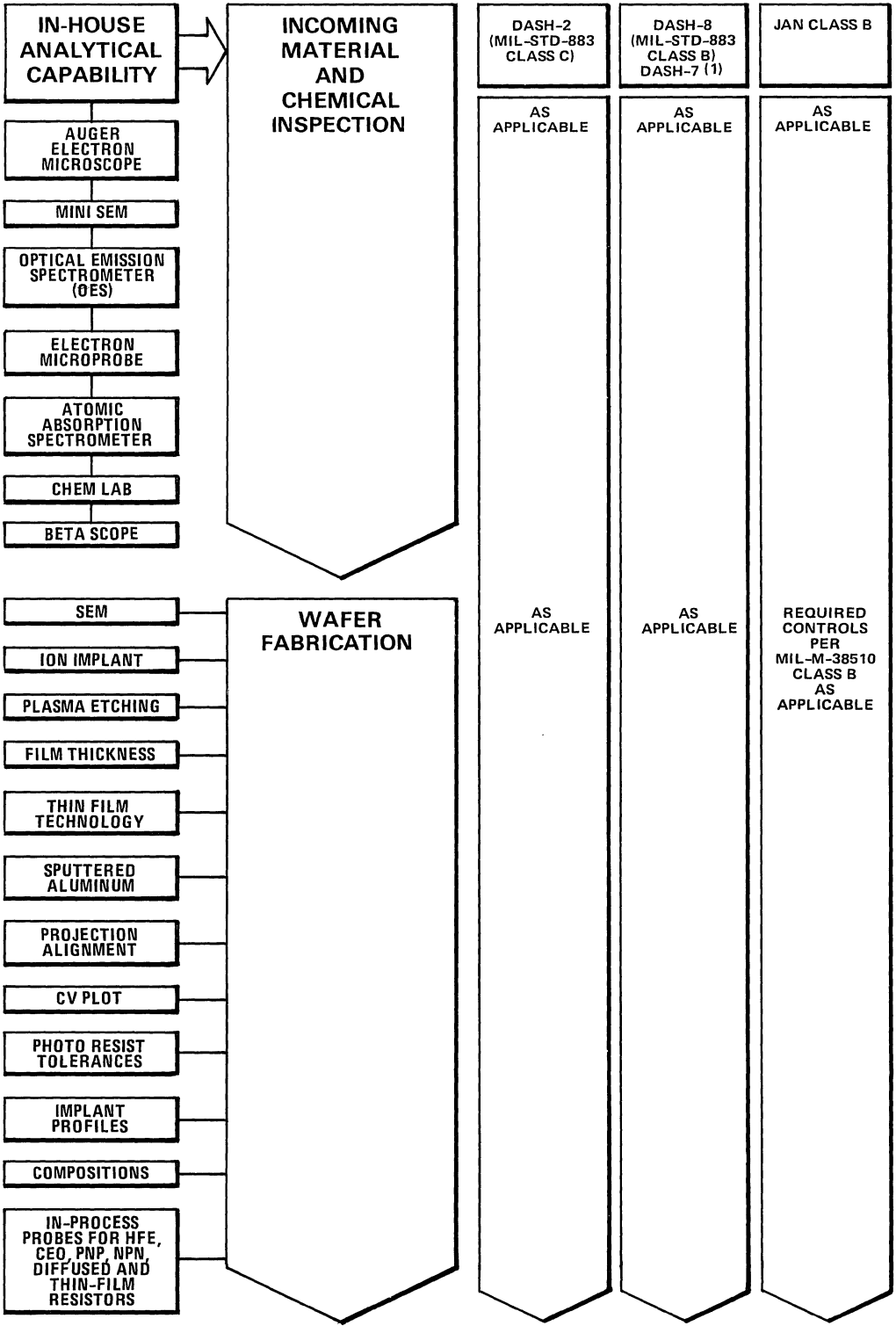
Wherever feasible, and in accordance with good value engineering practice, the IC user should specify Hi-Rel device grades based on one of the four standard Harris manufacturing flows. These are more than adequate for the overwhelming majority of applications and may be utilized quite easily if the user engineer bases his designs on the standard data book or slash sheet (as applicable) electrical limits.

Some of the more important advantages gained by using standard as opposed to custom flows are as follows:

- **Lower cost** than the same or an equivalent flow executed on a custom basis. This results from the higher efficiency achieved with a constant product flow and the elimination of such extra cost items as special fixturing, test programs, additional handling, and added documentation.
- **Faster delivery** since the manufacturer often can supply many items from inventory and, in any case, can establish and maintain a better product flow when there is no need to restructure process and/or test procedures.
- **Increased confidence** in the Hi-Rel devices, for a continuing flow of a given Hi-Rel product permits the manufacturer to monitor trends which may bear on end-product performance or reliability and to effect necessary corrective action.
- **Reduction of risk,** since each product is processed independent of specific customer orders, permitting lot failures to be absorbed within the scheduling framework without impacting on the customer's needs. In the case of a custom Hi-Rel flow, a lot failure late in the production cycle can result in significant delays in delivery due to the required re-cycling time.

Despite the advantages of using standard Hi-Rel flows, there are cases where a special or custom flow is mandatory to meet design or other requirements. In such cases, the Harris Analog and Digital Marketing groups stand ready to discuss individual customer needs and, where indicated, to develop appropriate custom flows.

HARRIS SEMICONDUCTOR
STANDARD HI-REL PROCESSING FLOWS



(1) T_A = -55°C to +125°C for all grades except DASH-7 (DASH-7 T_A = 0°C to +75°C)

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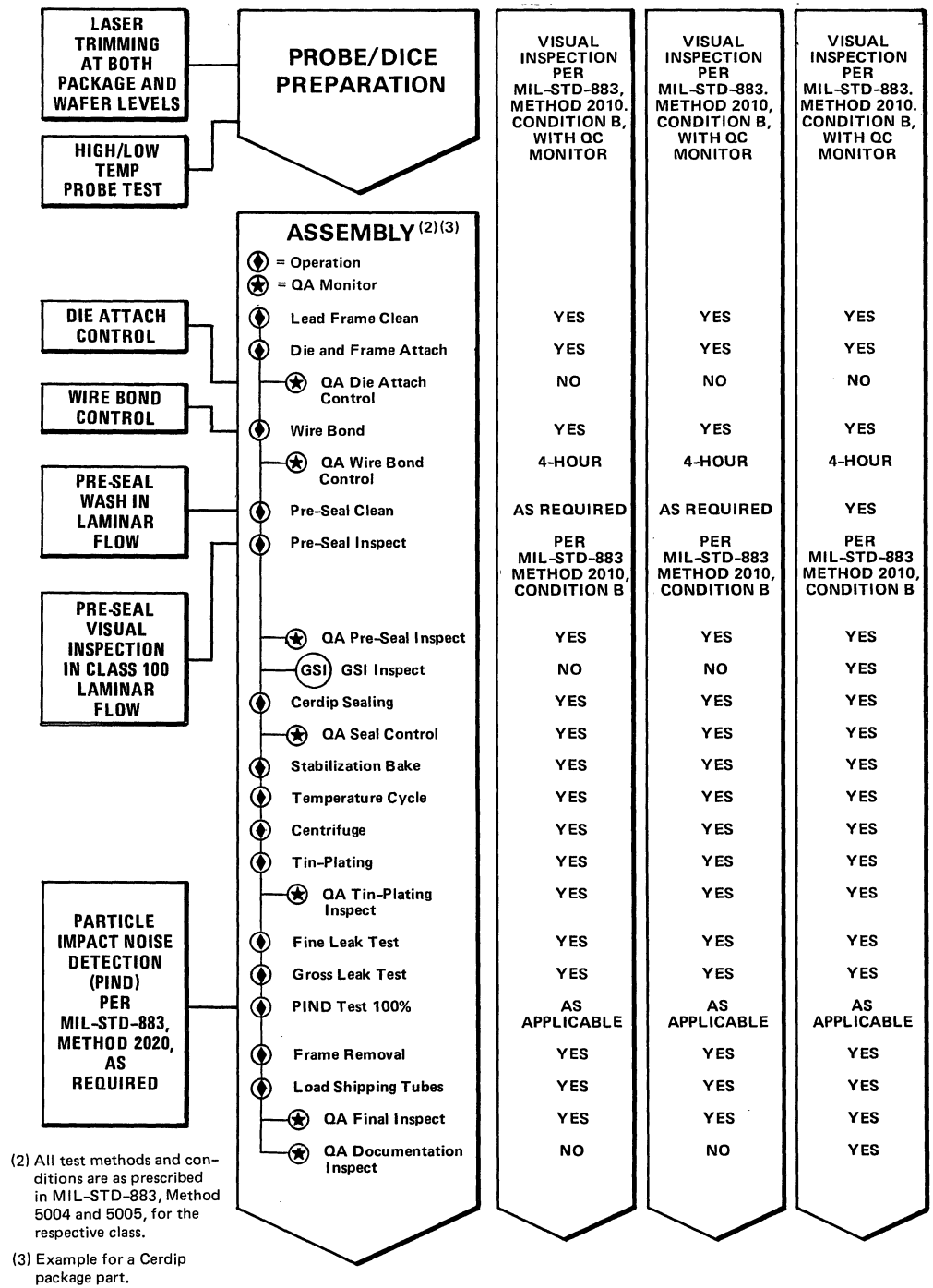
HARRIS SEMICONDUCTOR
STANDARD HI-REL PROCESSING FLOWS
(continued)



(2) All test methods and conditions are as prescribed in MIL-STD-883, Method 5004 and 5005, for the respective class.

(3) Example for a Cerdip package part.

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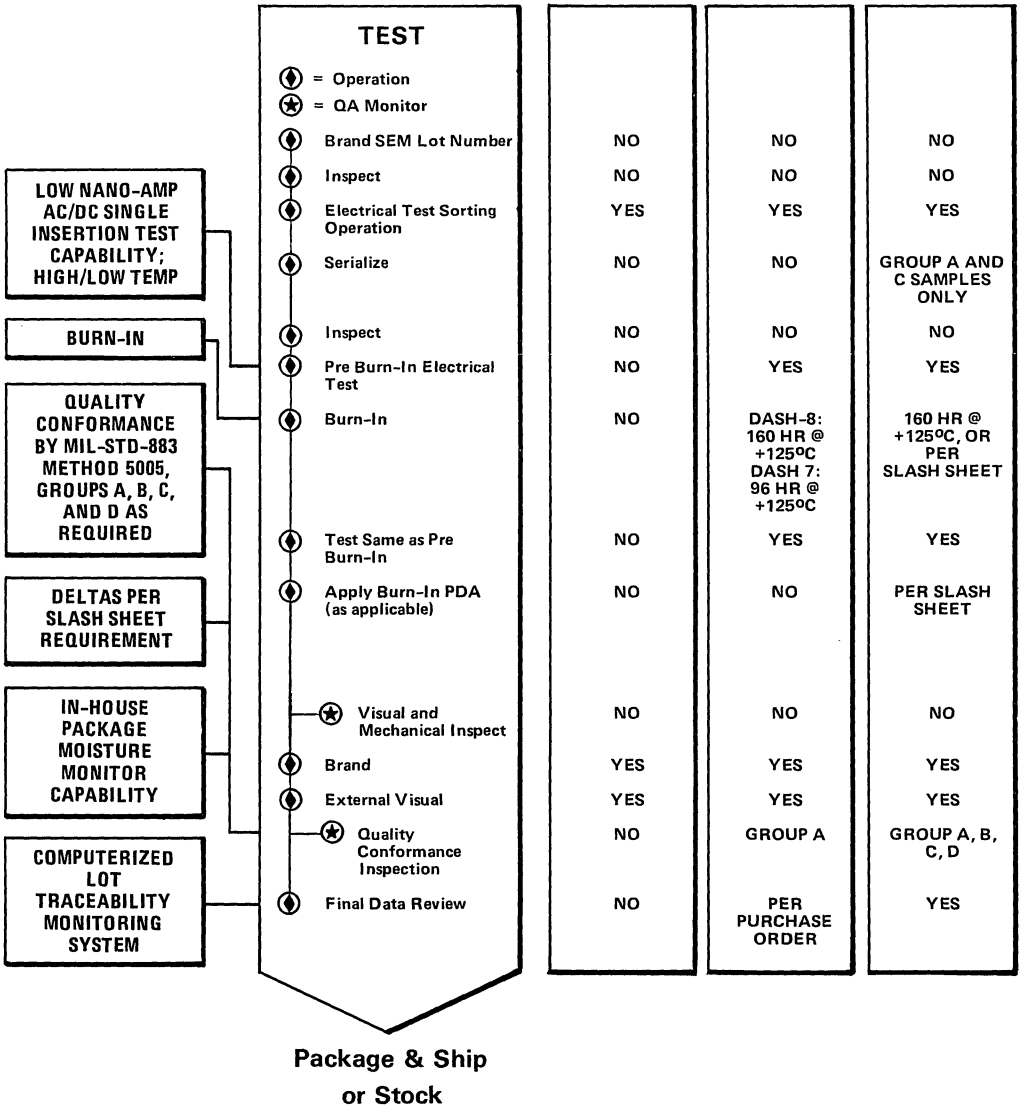
HARRIS SEMICONDUCTOR
STANDARD HI-REL PROCESSING FLOWS

(continued)



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Initial Circuit Selection and Design

There are, of course, many different circuit configurations capable of handling any given task, once operational characteristics and parameter limits have been established. Harris designers choose those which are capable of meeting the required performance specifications with maximum reliability.

Powerful computer aided design (CAD) techniques are applied in developing the original circuits, with computer modeled circuit simulation used to corroborate projected product performance. Monte Carlo methods, ISPICE programs, and other simulation techniques are used, as appropriate to the specific design.

Regardless of the circuit approach selected, high reliability, top performance, and maximum potential yield are the governing criteria.

Individual active device types and component values are selected to provide optimum circuit performance and to minimize sensitivity to parametric changes which may occur with aging or as a result of application environmental conditions.

Die Layout and Geometry

IC die conformance with good layout practice is a must, for consistently reliable devices cannot be assembled from poorly designed dice. Therefore, the IC die layout phase at Harris is controlled by ground rules which establish the "do's" and "don'ts" for each manufacturing process. These rules define dimensions and tolerances for ensuring product immunity to process variations, while maximizing product reliability under worst-case stress conditions. Computerized ground rule program packages are used by the chip designers to assure dimensional adherence of diffusion windows as well as interconnect width and spacing. Automatic checkout procedures confirm that the product conforms to the established ground rules.

Raw Material Inspection and QC

Acknowledging that Hi-Rel, high performance devices can be manufactured only by using top quality materials, Harris subjects incoming materials, piece parts and supplies to rigorously documented tests and inspections. The techniques used are selected for optimum evaluation of the materials checked to ensure full compliance not only with Harris internal specifications, but with applicable standards, including MIL-STD-883 and MIL-M-38510.

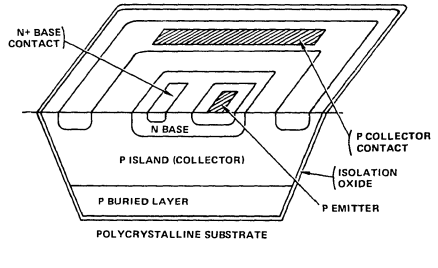
Wafer Die Production Process and Controls

Harris has a wide range of state-of-the-art wafer and die processing capabilities, permitting the chip designer to choose the optimum production technique for each type of device.

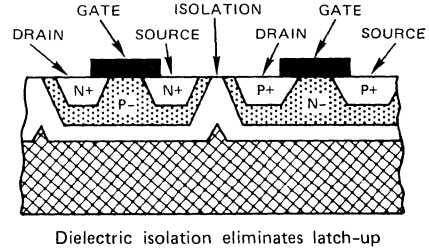
Depending on specific design and performance specifications, devices may be fabricated using either conventional or complementary bipolar, CMOS, combined bipolar and CMOS, NMOS or PMOS construction. Two different complementary *vertical* bipolar processes are available, offering frequency responses two orders of magnitude higher than conventional designs.

Regardless of the fabrication technique used, extensive controls and checks are incorporated within each process technology to ensure high yields, close adherence to target specifications, and full conformance with all standards applicable to the specific Hi-Rel class.

With high reliability an integral part of its manufacturing philosophy, Harris Semiconductor does not have separate production lines for standard and Hi-Rel devices. Rather, all Harris devices of a given type are manufactured on the same line. Hi-Rel devices are selected by the application of screening tests and control procedures including



Cross-sectional view of high-frequency PNP device formation in the DI process.



Dielectric isolation eliminates latch-up by placing a silicon-dioxide isolation barrier between devices. This separates all active elements, eliminating interface junctions that cause parasitic SCRs.

a comprehensive burn-in program. Compliance with overall quality assurance goals is proven by lot acceptance in accordance with applicable quality conformance test standards.

Die/Package Assembly and Controls

Many mechanical and environmental compliance tests are implemented during the die/package assembly stage. The specific controls and tests utilized at each step are in strict compliance with the applicable standards for the device reliability class designation.

Burn-In

An essential part of Harris Hi-Rel flows, 100% burn-in is a screening procedure used to detect devices subject to infant mortality failure modes. Biases are applied to simulate worst-case operational conditions, permitting the identification and elimination of marginal units.

The applied voltage levels, operational state, temperature and test period vary with the type of device and reliability class, as governed by the applicable standards. Electrical test of the device is performed both prior to and after the burn-in period.

Screening and Test Procedures

While many factors are critical in the production of Hi-Rel devices, the screening and test procedures, considered as a group, are critical to establishing reliability grade levels. In addition to the test procedures required by the purchase specification, all Harris devices must undergo an exhaustive battery of internal QA and QC tests to assure compliance with the rigorous Harris production standards.

Harris internal QA and QC tests are in full compliance with Appendix A of MIL-M-38510 for all JAN Class B devices. For DASH-2, DASH-7, and DASH-8 devices, Harris imposes a QA and QC program derived from and comparable to the same standard.

Reliability Assessment and Enhancement

At Harris, reliability assurance is a dynamic program with the primary and ultimate goal of securing full product adherence to all applicable standards and specifications. Each phase of the manufacturing operation from original design to final packaging is subject to continuous review, analysis, and evaluation, with modifications introduced when needed to improve product performance and reliability.

The Design Phase

The initial design is not only the first step in producing a new device, but can be one of the most important in determining product reliability, for without sound design practice, neither extensive process controls nor intensive down line testing can positively assure product reliability.

At Harris, all new products are developed using a proven set of design rules. Derived from composite inputs supplied by the Product Design, Manufacturing, Sustaining Product Engineering, Quality Assurance and Reliability Departments, the design rule package is subject to a continuing review. These procedures ensure that all designs conform to state-of-the-art engineering practice.

Process Control and Evaluation

Harris is extremely conscious of process-related problems which may contribute to degradation of reliability. All fabrication processes are accurately documented, with process and other program specifications under configuration control and subject to change only through formal ECN. Among other measures, critical parameters are monitored constantly by the Process Engineering, QC, QA, Sustaining Product Engineering and Reliability Departments, which then investigate and suggest methods to enhance reliability and improve yields.

The Harris Reliability Department

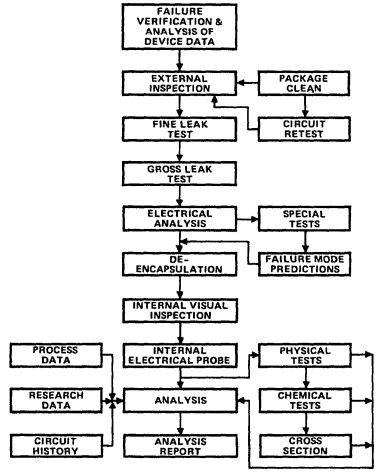
Charged with overall responsibility for the reliability of Harris Semiconductor products, the Reliability Department is involved, as needed, in all phases of the production cycle from original concept and design through final packaging and test. Among its major accomplishments, the Reliability Department has implemented a comprehensive multi-faceted program to assure a continuing high level of product and new technology reliability prove-in. The program comprises several major activities, as follows:

- **Add-On** - One of the overall activities is the maintenance of an active operating life test program called **"Add-On."** This program provides an ongoing data base and determines life trends. Package integrity is verified, as is qualification in accordance with MIL-STD-883, including residual moisture monitoring inside the package cavity. In practice, the latter is accomplished through the use of a Harris-designed in-situ moisture monitor cell. The development and practical implementation of this revolutionary moisture-monitoring technique culminated in DESC Certification of Harris to supply moisture data.

  Another facet of the **Add-On** Program is the periodic release of product and package Reliability Bulletins. Representing the results of long-term operating life testing, this information is routinely updated. The current Reliability Bulletins and an applicable updated index are available on request.

- **Failure Rate Prediction** - Another important facet of the comprehensive reliability program, *failure rate prediction* is used to extrapolate meaningful long-term operating performance under end-use conditions. Using the Arrhenius relationship, derated failure rates can be projected using an activation energy for the applicable process technology.
- **Failure Analysis** - An exhaustive analysis of device failures is another significant feature of the Harris reliability program. Before the Reliability Department proceeds with an analysis program, the reported failure mode must be confirmed by electrical tests. After failure confirmation, the device is processed through a standard failure analysis procedure.

Failure Analysis Flow



- **Package Type/Vendor Qualification** Since the integrity of packages and associated piece-parts are critical to the reliability of assembled products, the Reliability Department is charged with qualifying all vendor-supplied package types, both initially and, on a continuing basis, through ongoing monitoring programs. The qualification tests are in accordance with the rigorous MIL-STD-883 procedures and ensure full compliance with all thermal, mechanical and environmental specifications.
- **New Product/Process/Module Qualification** - In addition to the direct responsibilty of assuring product reliability, the Reliability Department performs qualification of all new products and processes. The reliability qualification must be completed *before* a new product can be transferred officially into production or offered for sale.

Harris and the JAN Program

Harris Semiconductor became an active participant in the JAN program as the *first* microcircuit manufacturer to JAN-qualify a PROM, receiving a QPL-2 qualification in 1972 and the higher level QPL-1 qualification in 1974 for the military version of the HPROM-0512, as defined by MIL-M-38510, Slash Sheet 201. Since this initial effort, Harris has received JAN line certification for the generic HM-76XX PROM family. In early 1980, Harris received JAN certification for three additional production lines supplying Dielectrically Isolated (DI) operational amplifiers, analog switches, analog multiplexers, and Junction Isolated op amps.

Harris will continue to pursue further line certification and part qualification efforts, offering users an ever-expanding line of JAN-qualified devices.

Full JAN-qualified products can be supplied only in packaged form. However, Harris stands ready to supply individual dice on special order which have been processed through probe/dice preparation in accordance with indicated JAN flows and controls.

TYPE	FUNCTION	MIL-M-38510/	QPL-2
HA2-2600	High Performance Operational Amplifier	12202BGC	Now Qualified
HA2-2620	Very Wide Band, Uncompensated Op Amp	12203BGC	Now Qualified
HA2-2500	Precision High Slew Rate Op Amp	12204BGC	Now Qualified
HA2-2510	High Slew Rate Op Amp	12205BGC	Now Qualified
HA2-2520	High Slew Rate Uncompensated Op Amp	12206BGC	Now Qualified
HA1-4741	Quad Operational Amp	11003BCA	Now Qualified

7

Typical Harris Hi-Rel Government Program Participation

NEARTIP (Torpedo)
CRUISE MISSILE (ALCM)
(TLCM)
(GLCM)
CAPTOR (Mine)
IUS (Shuttle Inertial Upper Stage)
F15 (Aircraft)
F14 (Aircraft)
F16 (Aircraft)
F18 (Aircraft)
HARPOON (Missile)
SPACE SHUTTLE
VIKING (Mars Lander)
GPS (Global Position Satellite System)
ROLAND (Close in Air Defense)
AMRAAM (Advanced Medium Range Air-to-Air Missile)
HELLFIRE (Anti-Tank Missile)
757 (Commercial Aircraft)
767 (Commercial Aircraft)
SEASPARROW (Missile System)
WILD WEASLE (F-14)
MARK 48 TORPEDO
HARM (Hi-velocity Anti-Radiation Missile)
AWACS (Airborne Warning and Control System)
TACFIRE (Tactical Display and Control System)

Analog Application Notes

HARRIS

APPLICATION NOTE 509

A SIMPLE COMPARATOR USING THE HA-2620

BY G. G. MILER

The input current and impedance of a comparator circuit frequently loads the source and reference signals enough to cause significant errors. This problem is frequently eliminated by using a high impedance operational amplifier between the signal and the comparator. Figure 1 shows a simple circuit in which the operational amplifier is used as a comparator which is capable of driving approximately ten logic gates. The input impedance of the HA-2620 is typically 500 MΩ. The input current is typically 1 nA. The minimum output current of 15 mA is obtainable with an output swing of up to ±10 volts.

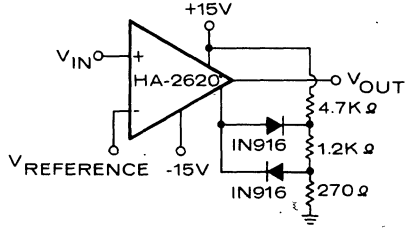


FIGURE 1 - HIGH IMPEDANCE COMPARATOR

The bandwidth control point is a very high impedance point having the same voltage as the amplifier output. The output swing can be conveniently limited by clamping the swing of the bandwidth control point. The maximum current through the clamp diodes is approximately 300 μA. The switching time is dependent on the output voltage swing and the stray capacitance at the bandwidth control point.

Figure 2 shows the waveforms for the comparator. The stray capacitance at the bandwidth control point can be reduced considerably below that of the breadboard circuit; this would improve the switching time. The switching time begins to increase more rapidly as the overdrive is reduced below 10 mV and is approximately 1μs for an overdrive of 5 mV. Dependable switching can be obtained with an overdrive as small as 1 mV. However, the switching time increases to almost 12 μs.

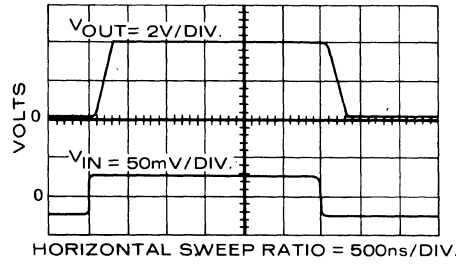


FIGURE 2 - WAVEFORMS FOR HA-2620 COMPARATOR

A common mode range of ±11 volts and a differential input range of ±12 volts makes the HA-2620 a very versatile comparator. The HA-2620 can sink or supply a minimum of 15 mA. The ability to externally clamp the output to any desired range makes the HA-2620 a very flexible comparator which is capable of driving unusual loads.

HARRIS

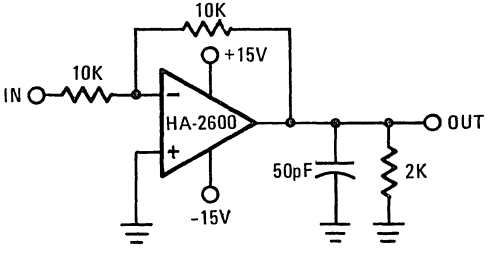
APPLICATION NOTE 515

OPERATIONAL AMPLIFIER STABILITY: INPUT CAPACITANCE CONSIDERATIONS

BY DON JONES

This is the first in a series of notes dealing with stabilization and optimization of A.C. response in operational amplifiers. One of the more common difficulties in applying operational amplifiers will be discussed.

Let's consider the unity gain inverting amplifier circuit shown below:



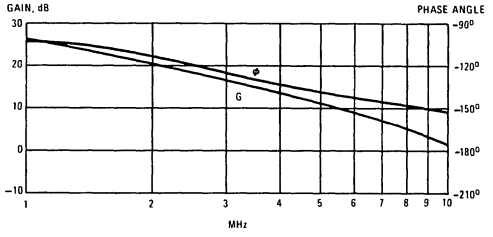
This appears to be a straightforward application with reasonable component values.

But, with the input grounded, the circuit output shows an oscillation at about 5 MHz.

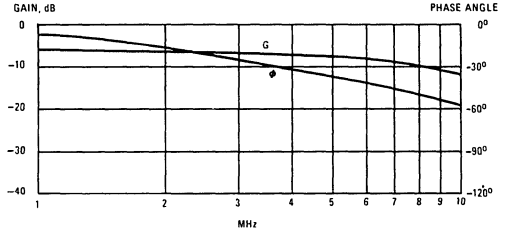
Even more surprising, if the same device is connected as a voltage follower with the same load, it is perfectly stable. Since the inverting amplifier has 6 dB less feedback than the voltage follower, shouldn't it be more stable?

The culprit here is capacitance at the amplifier inverting input. The HA-2600 in the TO-99 can has an input capacitance of about 2 or 3 pF. When soldered on a P.C. card, or inserted in a socket, wiring capacitance might add another 3 to 6 pF. With only 5K effective resistance at this point, 5 to 10 pF seems pretty negligible, doesn't it? But let's find out.

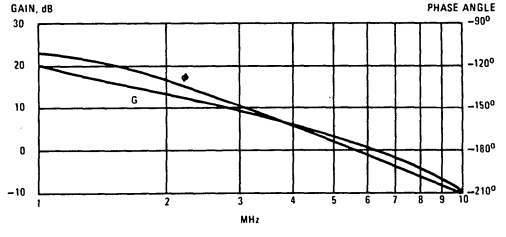
The open loop amplitude and phase response characteristics of the amplifier between 1 and 10 MHz looks like this:



The characteristics of the feedback network alone with 5 pF capacitance to ground looks like this:



Combining these two graphs by algebraically adding the dB gains together and adding the phase shifts together gives us the open loop response at the summing point:



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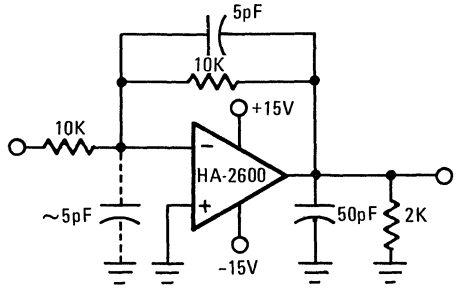
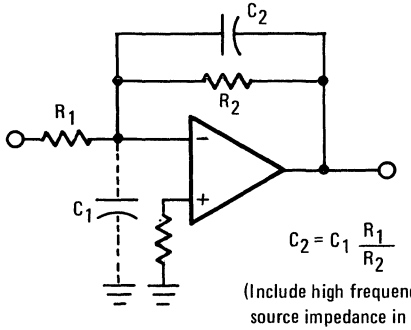
We can see that on the composite response curves, the phase shift crosses 180° at 5.5 MHz, and that there is still about +2 dB of gain at this frequency. Therefore, closing the loop automatically creates an oscillator.

How can we overcome this effect? If we add a capacitor across the feedback resistor, we can cancel the effects of the input capacitance:

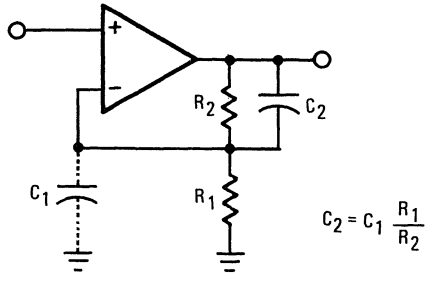


If the feedback capacitance matches the input capacitance, the response curves of the feedback network alone will be a flat -6 dB and 0° across the frequency band. The composite curves will then show a bandwidth of 7.5 MHz and a positive phase margin of 33°. So the circuit will now be quite stable. It's amazing how much difference that small capacitance can make.

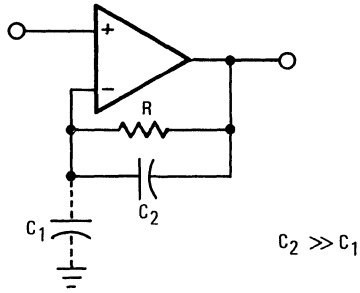
The general scheme for compensation of various circuit types is shown below:



INVERTING AMPLIFIER



NON-INVERTING AMPLIFIER



FOLLOWER WITH FEEDBACK RESISTOR

It's not really necessary to know the exact value of stray capacitance, C_1 - for most layouts, about 5 to 10 pF is a good guess. Unless you are trying to squeeze out the last Hz of frequency response, it doesn't hurt to guess on the high side. At higher gains, where C_2 calculates out to less than 1 or 2 pF, it isn't necessary to use C_2 - but it won't disturb anything if you do use it.

If you are uncertain about whether compensation is necessary, check the pulse response or frequency response of the closed loop stage. Hook a pulse generator to the input, and adjust the amplitude for about a 200 millivolt step at the output - if the output overshoot is less than 40% of the step, the circuit will be stable. Alternately, check the small signal frequency response of the stage - if the high frequency peaking is less than +6 dB, more than the low frequency gain, the circuit is stable. Of course, you can increase the compensation capacitor if you need even smoother response.

The phenomena we have described are not peculiar to any one amplifier type. Wideband amplifiers require a little more care in the design of feedback networks; but the same type oscillations will show up on 741 type amplifiers with higher feedback resistor values.

HARRIS

APPLICATION NOTE 517

APPLICATIONS OF A MONOLITHIC SAMPLE-AND-HOLD/GATED OPERATIONAL AMPLIFIER

BY DON JONES

INTRODUCTION

The sample-and-hold or track-and-hold function is very widely used in linear systems. Until recently, this function was available only in modular or hybrid circuits; or perhaps most frequently the circuit was constructed by the user from an analog switch, a capacitor, and a very low bias current operational amplifier.

A high quality sample-and-hold circuit must meet certain requirements:

(1) The holding capacitor must charge up and settle to its final value as quickly as possible.

(2) When holding, the leakage current at the capacitor must be as near zero as possible to minimize voltage drift with time.

(3) Other sources of error must be minimized.

Design of a sample-and-hold, particularly the user built variety, involves a number of compromises in the above requirements. The amplifier or other device feeding the analog switch must have high current capability and be able to drive capacitive loads with stability. The analog switch must have both low ON resistance and extremely low OFF leakage currents. But, leakage currents of most analog switches (except the dielectrically isolated types) run to several hundred nanoamperes at elevated temperatures. The analog switch must have very low coupling between the digital input and analog output, because any spikes generated at the instant of turn-off will change the charge on the capacitor. The output amplifier must have extremely low bias current over the temperature range, and also must have low offset drift and sufficient slew rate; a combination satisfied by only a few available amplifiers.

THE HA-2420/2425

The HA-2420/2425 is the first complete monolithic sample-and-hold integrated circuit. A functional diagram is shown in Figure 1.

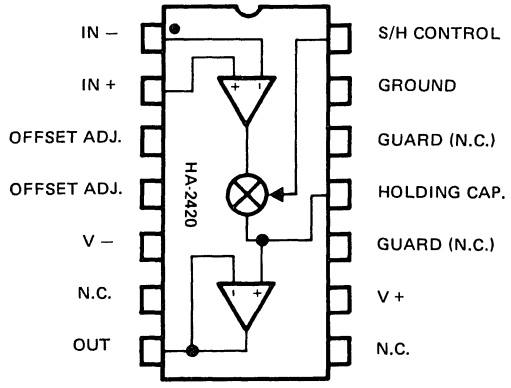


Figure 1 – HA-2420/2425 Functional Diagram

The input amplifier stage is a high performance operational amplifier with excellent slew rate, and the ability to drive high capacitance loads without instability. The switching element is a highly efficient bipolar transistor stage with extremely low leakage in the OFF condition. The output amplifier is a MOSFET input unity gain follower to achieve extremely low bias current.

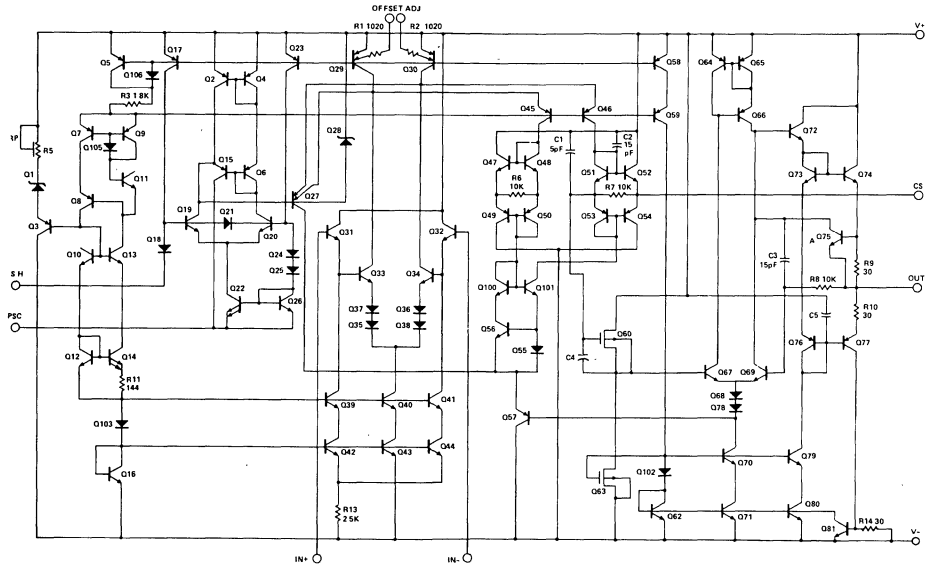
MOSFET inputs are generally not used for D.C. amplifiers because their offset voltage

8

drift is difficult to control. In this configuration, however, negative feedback is generally applied between the output and inputs of the entire device, and the effect of this offset drift at the inputs is divided by the open loop gain of the input amplifier stage.

The schematic of the HA-2420 is in Figure 2. During sampling (S/H control LOW) the signal path through the input amplifier stage starts at Q31-34, through Q45 and Q46, and then to the holding capacitor terminal through Q51-54. The output follower amplifier has its input at MOSFET Q60.

HA-2420/2425
Sample-and-Hold



NOTE: 1. Unless otherwise specified resistance values are in OHMS, capacitance values are in picofarads.

Figure 2

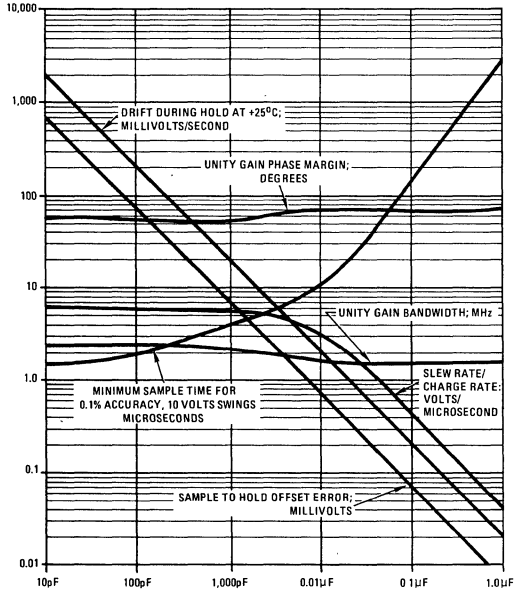


Figure 3 – Holding Capacitor, C_H
TYPICAL SAMPLE-AND-HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITANCE

In the "hold" mode, the S/H control is HIGH, so Q21 conducts, turning on Q27 which diverts the signal away from Q45 and Q46, and passes the signal to V - through Q57. Q57 also forces Q51-54 to ride up and down with the output signal, so there is virtually zero potential between these transistor bases and the voltage on C_H; completely eliminating leakage from C_H back into the input amplifier.

SAMPLE-AND-HOLD APPLICATIONS

A number of basic applications are shown on the following pages. The device is exceptionally versatile, since it can be wired into any of the hundreds of feedback configurations possible with any operational amplifier. In many applications the device will replace both an operational amplifier and a sample-and-hold module.

The larger the value of the timing capacitor, the longer time it will hold the signal without excessive drift; however, it will also reduce the

charging rate/slew rate and the amplifier bandwidth during sampling. So the capacitance value must be optimized for each particular application. The graph in Figure 3 shows these tradeoffs. Drift during holding tends to double for every 10°C rise in ambient temperature. The holding capacitor should have extremely high insulation resistance and low dielectric absorption-polystyrene (below +85°C), Teflon, or mica types are recommended.

Guard Ring Layout (Bottom View)

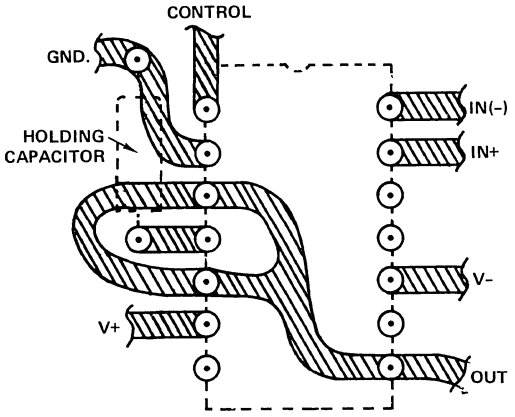


Figure 4

For least drift during holding, leakage paths on the P.C. board and on the device package surface must be minimized. Since the output voltage is nearly equal to the voltage on C_H, the output line may be used as a guard line surrounding the line to C_H. Then, since the potentials are nearly equal, very low leakage currents will flow. The two package pins surrounding the C_H pin are not internally connected, and may be used as guard pins to reduce leakage on the package surface. A suggested P.C. guard ring layout is shown in Figure 4.

GATED OPERATIONAL AMPLIFIER APPLICATIONS

An operational amplifier with a highly efficient analog switch in series with its output is a very useful building block for linear systems. The amplifier can be connected in any of the conventional op amp feedback configurations.

With the switch closed, the circuit behaves as a conventional op amp with excellent bandwidth, slew rate, high output current capability, and is able to drive capacitive loads with good stability. With the switch open, the output node is an almost perfect open circuit.

The output buffer amplifier has extremely high input impedance and exceptionally low bias current, but is not particularly well suited for D.C. applications outside an overall feedback loop, since its offset voltage may be quite high.

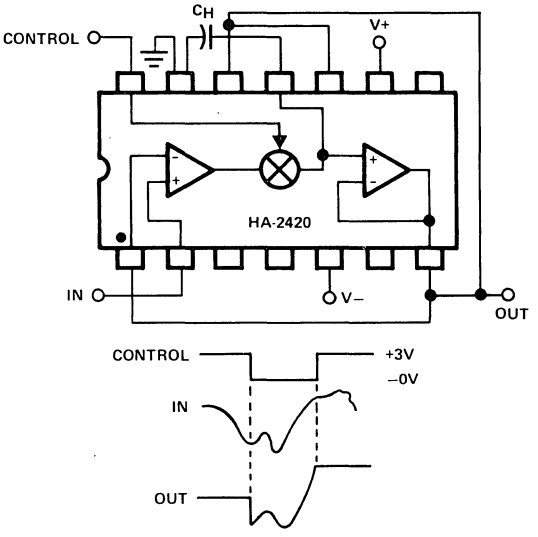
A number of possible gated amplifier applications are suggested in the following section.

APPLICATION NO. 1

Feedback is the same as a conventional op amp voltage follower which yields a unity gain, non-inverting output. This hookup also has a very high input impedance.

The only difference between a track-and-hold and a sample-and-hold is the time period during which the switch is closed. In track-and-hold operation, the switch is closed for a relatively long period during which the output signal may change appreciably; and the output will hold the level present at the instant the switch is opened. In sample-and-hold opera-

Basic Track-and-Hold/Sample-and-Hold



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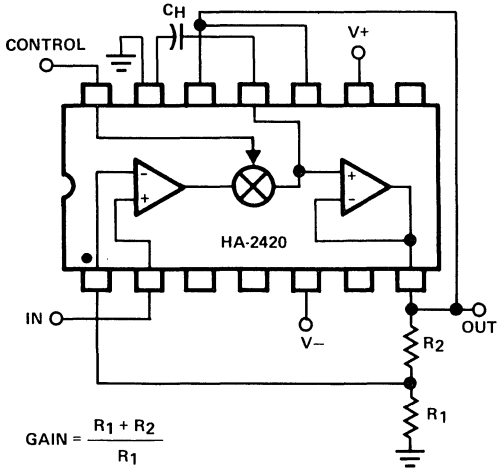
tion, the switch is closed only for the period of time necessary to fully charge the holding capacitor.

APPLICATION NO. 2

Sample-and-Hold With Gain



$$\text{GAIN} = \frac{R_1 + R_2}{R_1}$$

This is the standard non-inverting amplifier feedback circuit.

It illustrates one of the many ways in which the HA-2420 may be used to perform both op amp and sampling functions, eliminating the need for a separate scaling amplifier and sample-and-hold module.

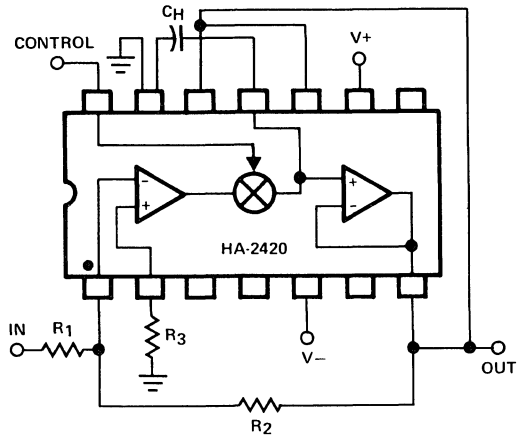
In general, it is usually best design practice to scale the gain such that the largest expected signal will give an output close to + or − 10 volts. Drift current is essentially independent of output level, and less percentage drift will occur in a given time for a larger output signal.

APPLICATION NO. 3

This illustrates another application in which the hookup versatility of the HA-2400 often eliminates the need for a separate operational amplifier and sample-and-hold module. This hookup will have somewhat higher input to output feedthrough during "hold," than the non-inverting connection, since output impedance is the open-loop value during "hold," and feedthrough will be:

$$\frac{\text{Vin Ro}}{R_1 + R_2 + R_O}$$

Inverting Sample-and-Hold



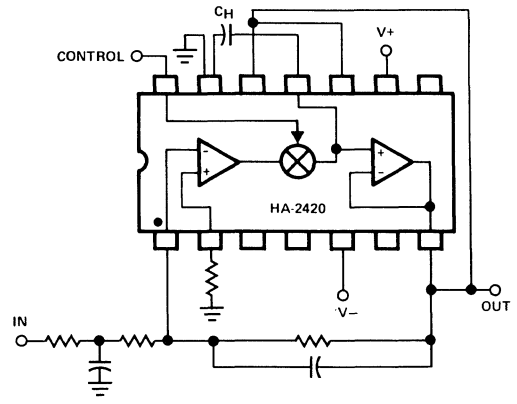
$$\text{GAIN} = -\frac{R_2}{R_1}$$

$$\text{MAKE} \quad R_3 = \frac{R_1 R_2}{R_1 + R_2}$$

APPLICATION NO. 4

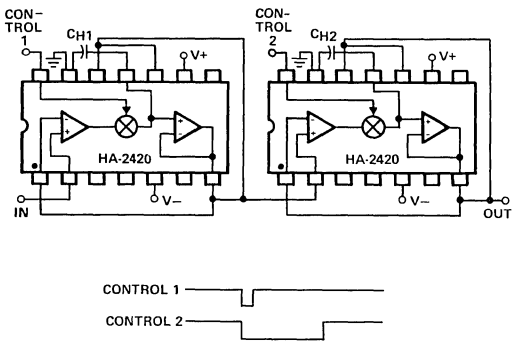
It is often required that a signal be filtered prior to sampling. This can be accomplished with only one device. Any of the inverting and non-inverting filters which can be built with op amps can be implemented. However, it is necessary that the sampling switch be closed for sufficient time for the filter to settle when active filter types are connected around the device.

Filtered Sample-and-Hold



APPLICATION NO. 5

Cascaded Sample-and-Hold

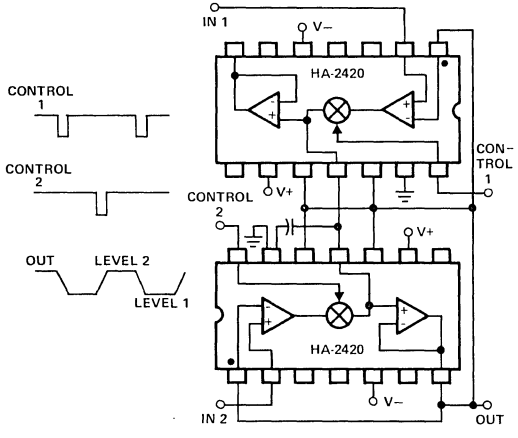


Short sample times require a low value holding capacitor; while long, accurate hold times require a high value holding capacitor. So, achieving a very long hold with a short sample appears to be contradictory. However, it can be accomplished by cascading two S/H circuits, the first with a low value capacitor, the second with a high value. Then the second S/H can sample for as long a time as the first circuit can accurately hold the signal.

APPLICATION NO. 6

Two or more S/H circuits may share a common holding capacitor and output as shown. The only limit to the number of devices to be

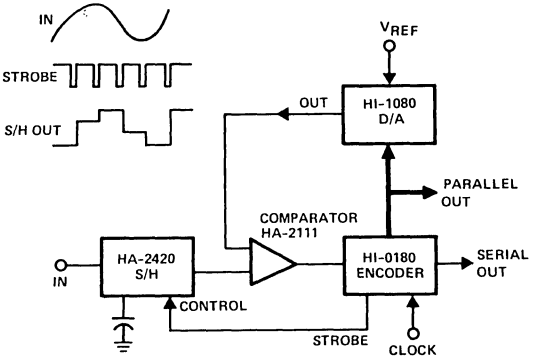
Multiplexed Sample-and-Hold



multiplexed is that the leakage currents of all devices add together, which increases drift during holding.

APPLICATION NO. 7

A/D Converter

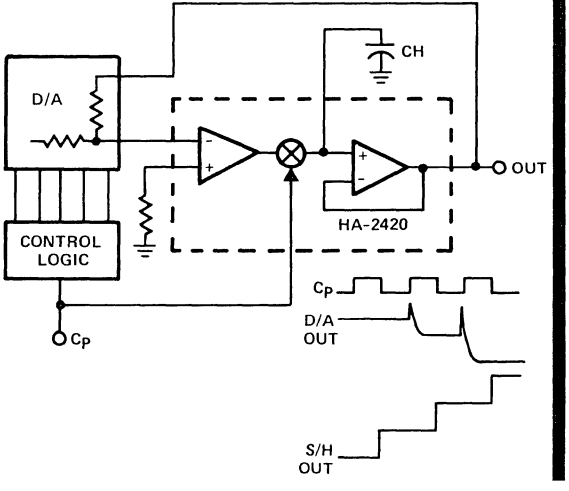


Certain analog to digital converters such as the successive approximation type require that the input signal be a steady D.C. level during the conversion cycle. The HA-2420 is ideal for holding the signal steady during conversion; and also functions as a buffer amplifier for the input signal, adding gain, inversion, etc., if required.

The system illustrated is a complete 8 bit successive approximation converter requiring only four I.C. packages and capable of up to 40,000 conversions per second. Interconnection details are shown on the HI-0180 data sheet.

APPLICATION NO. 8

De-Glitcher



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The word "glitch" has been a universal slang expression among electronics people for an unwanted transient condition. In D to A converters, the word has achieved semi-official status for an output transient which momentarily goes in the wrong direction when the digital input address is changed.

In the illustration, the HA-2420 does double duty, serving as a buffer amplifier as well as a glitch remover, delaying the output by ½ clock cycle.

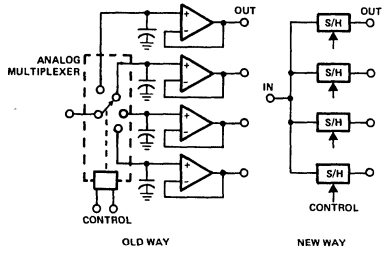
The HA-2420 may be used to remove many other types of "glitches" in a system. If a delayed sample pulse is required, this can be generated using a dual monostable multivibrator I.C.

APPLICATION NO. 9

This circuit reconstructs and separates analog signals which have been time division multiplexed.

The conventional method, shown on the left, has several restrictions, particularly when a short dwell time and a long, accurate hold time is required. The capacitors must charge from a low impedance source through the resistance and current limiting characteristics of the multiplexer. When holding, the high impedance lines are relatively long and subject

De-Multiplexer

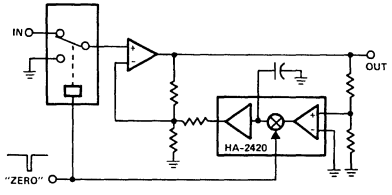


to noise pickup and leakage. When FET input buffer amplifiers are used for low leakage, severe temperature offset errors are often introduced.

Use of the HA-2420 greatly diminishes all of these problems.

APPLICATION NO. 10

Automatic Offset Zeroing



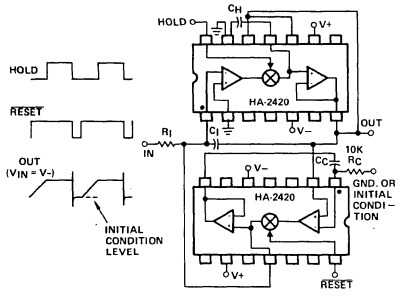
This basic circuit has widespread applications in instrumentation, A/D conversion, DVM's and DPM's to eliminate offset drift errors by periodically rezeroing the system. Basically, the input is periodically grounded, the output offset is then sampled and fed back to cancel the error.

The system illustrated automatically zeros a high gain amplifier. Care in the actual design is necessary to assure that the zeroing loop is dynamically stable. A second sample-and-hold could be added in series with the output to remove the output discontinuity.

Many variations of this scheme are possible to suit the individual system.

APPLICATION NO.11

Integrate-Hold-Reset



This circuit accurately computes the functions,

$$V_o = \int_{T_1}^{T_2} V_{in}\, dt$$

and holds the answer for further processing.

Resetting circuits for integrators have always been a practical design problem. The reset circuit must produce an extremely low leakage current across the integrating capacitor, and must produce a very low offset voltage when turned on. The circuit illustrated has excellent results since the leakage at the switch node is exceptionally low. R_C and C_C prevent oscillations during reset and their product should be at least 0.02 times R_I X C_I.

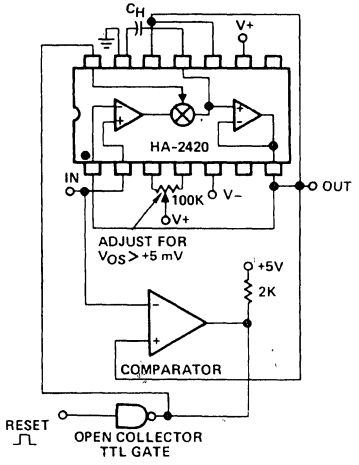
For the simpler integrate and reset function without a hold, substitute an ordinary operational amplifier for the upper device.

APPLICATION NO. 12

This accurate, low drift peak detector circuit combines the basic sample-and-hold connection with a comparator, and will detect 20V p-p signals up to 50kHz.

When the input signal level exceeds the voltage being stored in the S/H, the comparator trips, and a new sample of the input is taken. The S/H offset pot should be adjusted for a slight positive offset, so that the comparator will trip back when the new peak is acquired; otherwise the comparator would remain "on" and the S/H would follow the peak back down.

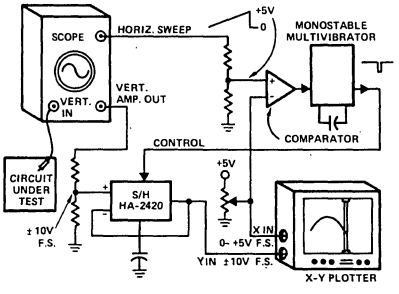
To make a negative peak detector, reverse the comparator inputs, and adjust the S/H for a negative offset.



The reset function, which is difficult to achieve in other peak detector circuits, forces a new sample at the instantaneous input level.

APPLICATION NO. 13

Plot High Speed Waveforms With Sampling Techniques



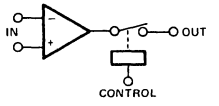
This useful application illustrates how fast repetitive waveforms can be slowed down using sampling techniques. The input signal is much too fast to be tracked directly by the X-Y recorder; but sampling allows the recorder to be driven as slow as necessary.

To operate, the waveform is first synched in on the scope. Then the potentiometer connected to the recorder X input is slowly advanced, and the waveform will be reproduced. The HA-2420 samples for a very short interval once each horizontal sweep of the scope. The sampling instant is determined by the potentiometer at the instant when the horizontal sweep waveform corresponds to the X position of the recorder.

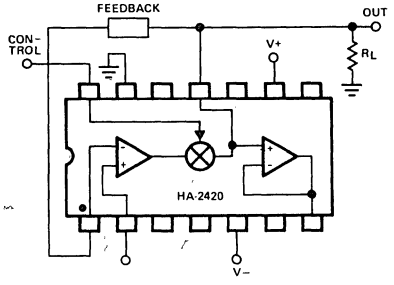
This principle can be applied to many systems for waveform analysis, etc.

APPLICATION NO. 14

Gated Operational Amplifier



EQUIVALENT CIRCUIT



The following are a few of the many applications where an operational amplifier followed by a highly efficient analog switch could be used:

- Analog Multiplexer Element
- Gated Oscillator
- Precision Timing Circuit
- Chopper Type Modulator/Demodulator
- Crosspoint Switch Element
- Reset or Initial Conditions Switch
- Gated Comparator
- Automatic Calibration Switch
- Gated Voltage Regulator

8

HARRIS

APPLICATION NOTE 519

OPERATIONAL AMPLIFIER NOISE PREDICTION

BY RICHARD WHITEHEAD

INTRODUCTION

When working with op amp circuits an engineer is frequently required to predict the total RMS output noise in a given bandwidth for a certain feedback configuration. While op amp noise can be expressed in a number of ways, "spot noise" (RMS input voltage noise or current noise which would pass through 1Hz wide bandpass filters centered at various discrete frequencies), affords a universal method of predicting output noise in any op amp configuration.

THE NOISE MODEL

Figure 1 is a typical noise model depicting the noise voltage and noise current sources that are added together in the form of root mean square to give the total equivalent input voltage noise (RMS), therefore:

$$E_{ni} = \sqrt{e_{ni}^2 + I_{ni}^2 R_g^2 + 4KTR_g}$$ where,

E_{ni} is the total equivalent input voltage noise of the circuit.

e_{ni} is the equivalent input voltage noise of the amplifier.

$I_{ni}^2 R_g^2$ is the voltage noise generated by the current noise.

$4KTR_g$ expresses the thermal noise generated by the external resistors in the circuit where $K = 1.23 \times 10^{-23}$ joules/°K; $T = 300$°K (27°C) and $R_g = \left(\frac{R_1 R_3}{R_1 + R_3}\right) + R_2$

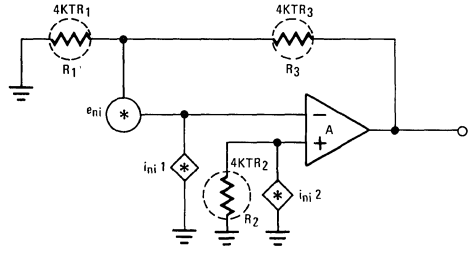


Figure 1

The total RMS output noise (E_{no}) of an amplifier stage with gain = G in the bandwidth between f_1 and f_2 is:

$$E_{no} = G\left(\int_{f_1}^{f_2} E_{ni}^2 df^{1/2}\right)$$

Note that in the amplifier stage shown, G is the non-inverting gain $\left(G = 1 + \frac{R_2}{R_1}\right)$ regardless of which input is normally driven.

PROCEDURE FOR COMPUTING TOTAL OUTPUT NOISE

1. Refer to the voltage noise curves for the amplifier to be used. If the R_g value in the application is close to the R_g value in one of the curves, skip directly to step 6, using that curve for values of E_{ni}^2. If not, go to step 2.

2. Enter values of e_{ni}^2 in line (a) of the table below from the curve labeled "$R_g = 0\,\Omega$".

3. From the current noise curves for the

8

amplifier, obtain the values of i_{ni}^2 for each of the frequencies in the table, and multiply each by R_g^2, entering the products in line (b) of the table.

4. Obtain the value of $4KTR_g$ from Figure 14, and enter it on line (c) of the table. This is constant for all frequencies. The $4KTR_g$ value must be adjusted for temperatures other than normal room temperature.

5. Total each column in the table on line (d). This total is E_{ni}^2.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2					
(b) $I_{ni}^2R_g^2$					
(c) $4KTR_g$					
(d) E_{ni}^2					

6. On linear scale graph paper enter each of the values for E_{ni}^2 vs.. frequency. In most cases, sufficient accuracy can be obtained simply by joining the points on the graph with straight line segments.

7. For the bandwidth of interest, calculate the area under the curve by adding the areas of trapezoidal segments. This procedure assumes a perfectly square bandpass condition; to allow for the more normal -6db/octave bandpass skirts, multiply the upper (-3db) frequency by 1.57 to obtain the effective bandwidth of the circuit, before computing the area. The total area obtained is equivalent to the square of the total input noise over the given bandwidth.

8. Take the square root of the area found above and multiply by the gain (G) of the circuit to find the total Output RMS noise.

A TYPICAL EXAMPLE

It is necessary to find the output noise of the circuit shown below between 1KHz and 24KHz.

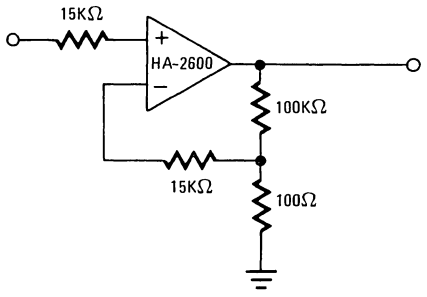
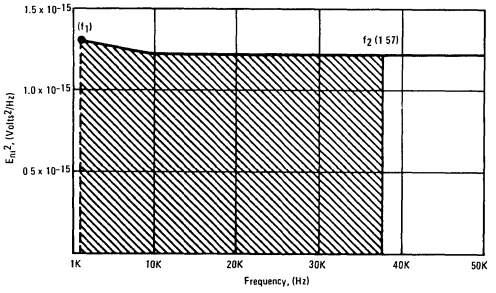


Figure 2
The HA-2600 In a Typical G = 1000 Circuit

Values are selected from Figures 5, 5a and 14 to fill in the table as shown below. An R_g of 30KΩ was selected.

	10Hz	100Hz	1KHz	10KHz	100KHz
(a) e_{ni}^2	3.6×10^{-15}	1.156×10^{-15}	7.84×10^{-16}	7.29×10^{-16}	7.29×10^{-16}
(b) $I_{ni}^2R_g^2$	9.9×10^{-16}	1.89×10^{-16}	3.15×10^{-17}	7.2×10^{-18}	7.2×10^{-18}
(c) $4KTR_g$	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}	4.968×10^{-16}
(d) E_{ni}^2	5.09×10^{-15}	1.86×10^{-15}	1.31×10^{-15}	1.23×10^{-15}	1.23×10^{-15}

The totals of the selected values for each frequency is in the form of E_{ni}^2. This should be plotted on linear graph paper as shown below:



HA-2600 Total Equivalent Input Noise Squared

Since a noise figure is needed for the frequency of 1KHz to 24KHz, it is necessary to calculate the effective bandwidth of the circuit. With AV = 60db the upper 3db point is approximately 24KHz. The product of 1.57 (24KHz) is 37.7KHz and is the effective bandwidth of the circuit.

The shaded area under the curve is approximately 45 x 10^{-12} $Volts^2$; the total equivalent input noise is $\sqrt{E_{ni}^2}$ or 6.7 microvolts, and the total output noise for the selected bandwidth is $\sqrt{E_{ni}^2}$ x (closed loop gain) or 6.7 millivolts RMS.

ACTUAL MEASUREMENTS FOR COMPARISON

The circuit shown below was used to actually measure the broadband noise of the HA-2600 for the selected bandwidth:

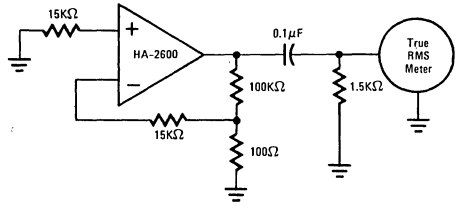


Figure 3
A Typical Test Circuit for Broadband Noise Measurements

The frequencies below the f_1 point of the bandwidth selected are filtered out by the RC network on the output of HA-2600. The measurement of the broadband noise is observed on the true RMS voltmeter. The measured output noise of the circuit is 4.7 microvolts RMS as compared to the calculated value of 6.7 microvolts RMS.

ACQUIRING THE DATA FOR CALCULATIONS

Spot noise values must be generated in order to make the output noise prediction. The effects of "Popcorn" noise have been excluded due to the type of measurement system.

The Quan-Tech Control Unit, model no. 2283 and Filter Unit, model no. 2181 were used to acquire spot noise voltage values expressed in ($V\sqrt{Hz}$). The test system performs measurements from 10Hz by orders of magnitude to 100KHz with an effective bandwidth of 1Hz at each tested frequency.

Several source resistance (R_g) values were used in the measuring system to reveal the effects of R_g on each type of Harris' op amps and to obtain proper voltage noise values essential for current noise calculations.

A DISCUSSION ON "POPCORN" NOISE

"Popcorn" noise was first discovered in early 709 type op amps. Essentially it is an abrupt step-like shift in offset voltage (or current) lasting for several milliseconds and having amplitude from less than one microvolt to several hundred microvolts. Occurance of the "pops" is quite random — an amplifier may exhibit several "pops" per second during one observation period and then remain "popless" for several minutes. Worst case conditions are usually at low temperatures with high values of R_g. Some amplifier designs and some manufacturer's products are notoriously bad in this respect. Although theories of the popcorn mechanism differ, it is known that devices with surface contamination of the semiconductor chip will be particularly bad "poppers". Advertising claims notwithstanding, the authors have never seen any manufacturer's op amp that was completely free of "popcorn". Some peak detector circuits have been developed to screen devices for low amplitude "pops", but 100% assurance is impossible because an infinite test time would be required. Some studies have shown that spot noise measurements at 10Hz and 100Hz, discarding units that are much higher than typical, is an effective screen for potentially high "popcorn" units.

The vast majority of Harris op amps will exhibit less than 3 μV peak-to-peak "popcorn". Screening can be performed, but it should be noted that the confidence level of the screen could be as low as 60%.

REFERENCES

Fitchen, F.C. and Motchenbacker, C.D. Low Noise Electronic Design. New York: John Wiley and Sons, 1973.

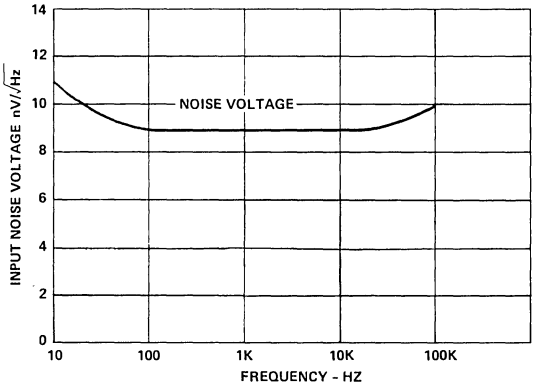
Instruction Manual, Model 2173C Transistor Noise Analyzer Control Unit. Quan-Tech, Division of KMS Industries. Whippany, New Jersey.

TYPICAL SPOT NOISE CURVES

Unless Otherwise Noted:
$V_S = \pm 15V$ $T_A = +25^oC$

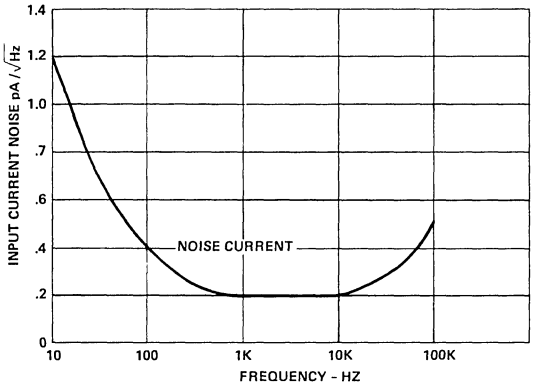
Curve 1

HA-5130/35 INPUT NOISE VOLTAGE



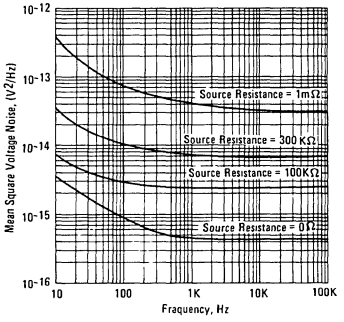
Curve 1A

HA-5130/35 INPUT NOISE CURRENT



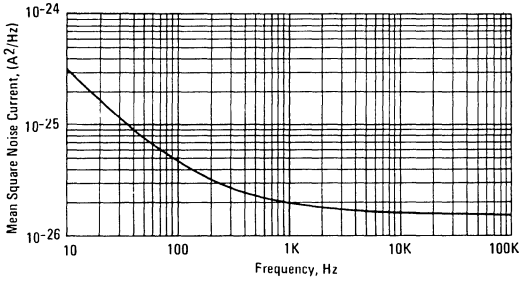
Curve 2

HA-2400 INPUT NOISE VOLTAGE



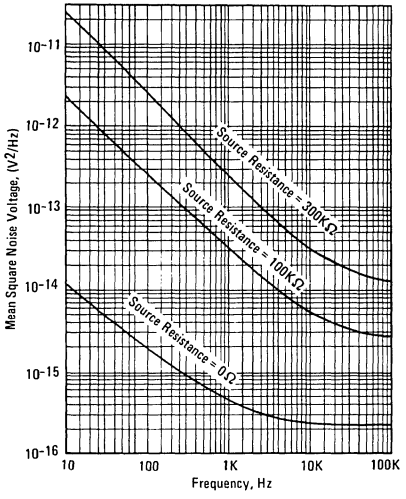
Curve 2A

HA-2400 INPUT NOISE CURRENT



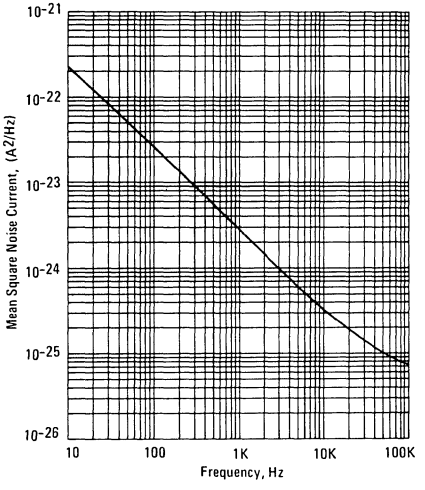
Curve 3

HA-2500/2510/2520 INPUT NOISE VOLTAGE



Curve 3A

HA-2500/2510/2520 INPUT NOISE CURRENT



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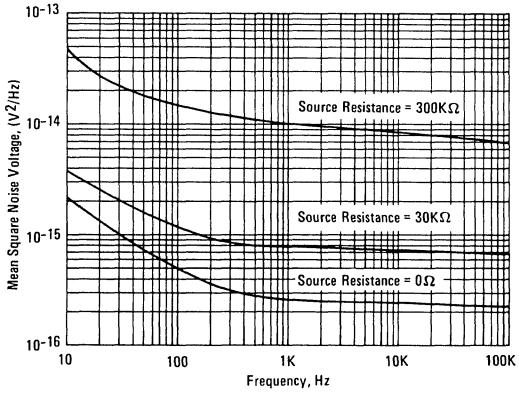
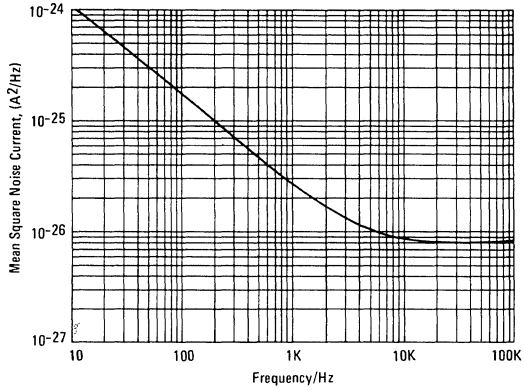
Curve 4

HA-2600/2620 INPUT NOISE VOLTAGE



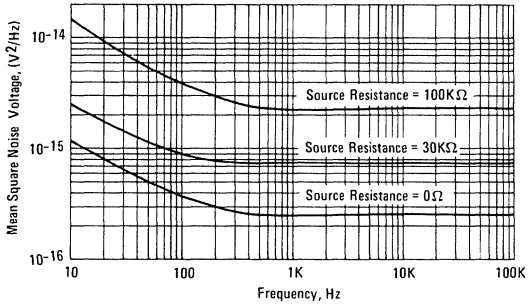
Curve 4A

HA-2600/2620 INPUT NOISE CURRENT



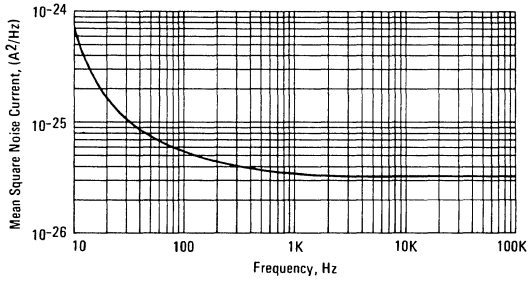
Curve 5

HA-2640/2645 INPUT VOLTAGE NOISE ($V_S = \pm 30V$)



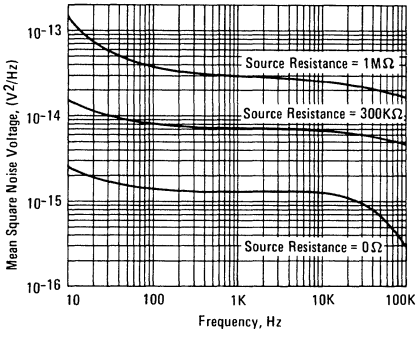
Curve 5A

HA-2640/45 INPUT NOISE CURRENT ($V_S = \pm 30V$)



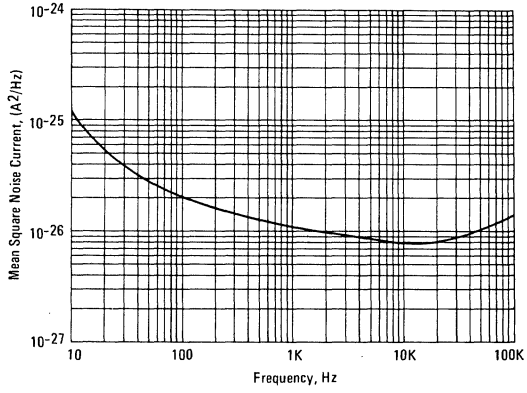
Curve 6

HA-2700 INPUT NOISE VOLTAGE



Curve 6A

HA-2700 INPUT NOISE CURRENT



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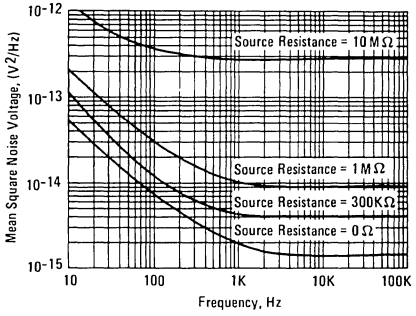
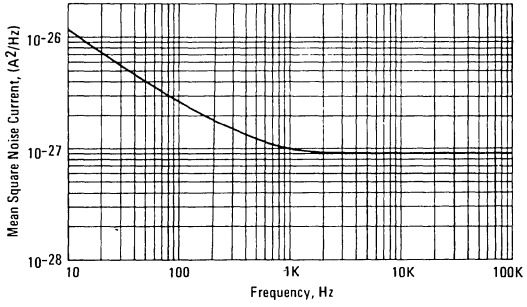
Curve 7

HA-2720/2730 INPUT NOISE VOLTAGE (I_{SET} = 1μA)



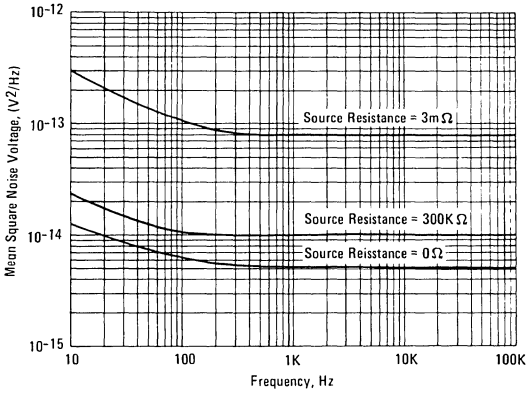
Curve 7A

HA-2720/2730 INPUT NOISE CURRENT (I_{SET} = 1μA)



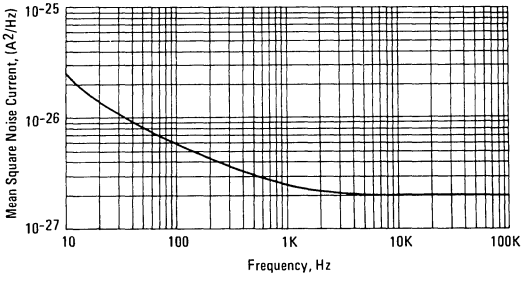
Curve 8

HA-2720/2730 INPUT NOISE VOLTAGE (I_{SET} = 10μA)



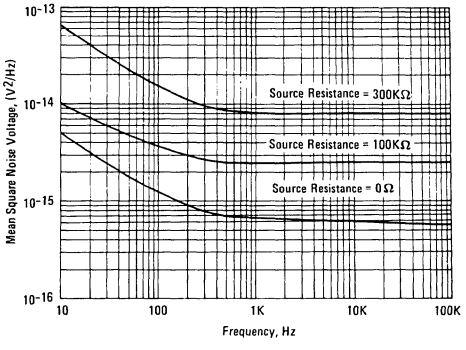
Curve 8A

HA-2720/2730 INPUT NOISE CURRENT (I_{SET} = 10μA)



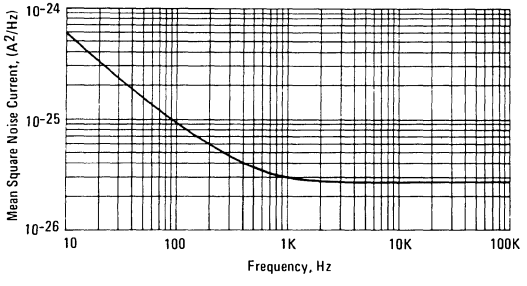
Curve 9

HA-2720/2730 INPUT NOISE VOLTAGE (I_{SET} = 100μA)



Curve 9A

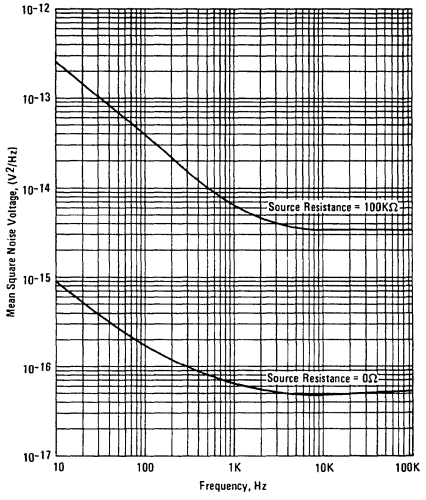
HA-2720/2730 INPUT NOISE CURRENT (I_{SET} = 100μA)



8.

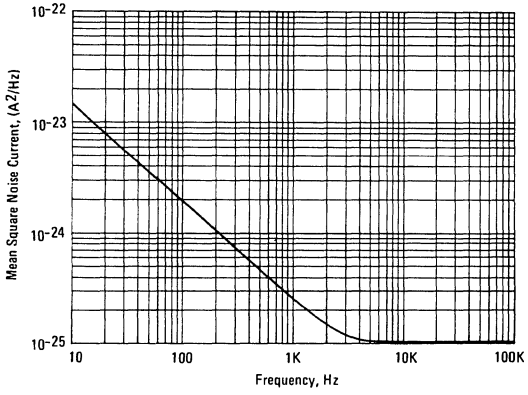
Curve 10

HA-4602/4605 INPUT NOISE VOLTAGE



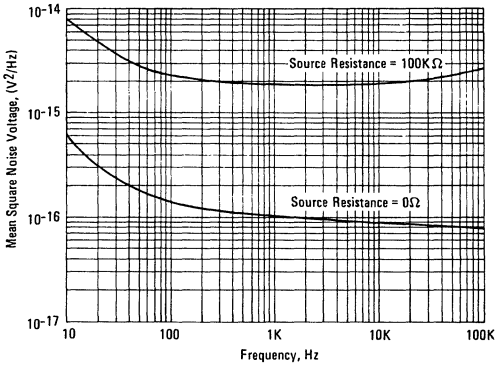
Curve 10A

HA-4602/4605 INPUT NOISE CURRENT



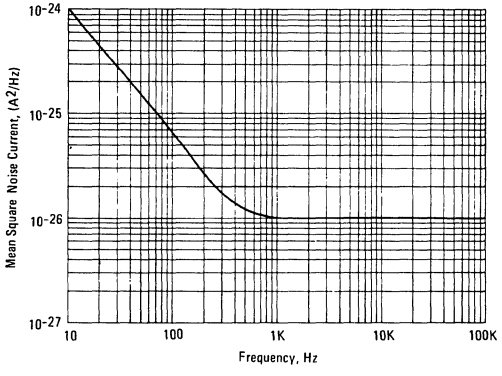
Curve 11

HA-4741 INPUT NOISE VOLTAGE

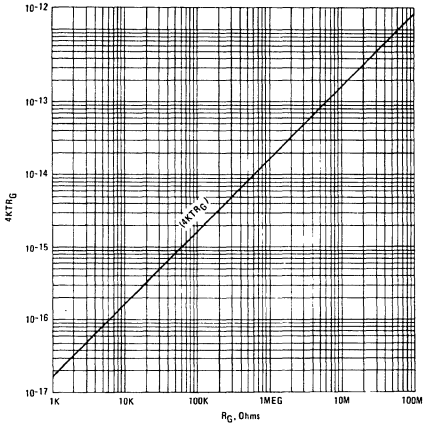


Curve 11A

HA-4741 INPUT NOISE CURRENT



Curve 12



8

HARRIS

APPLICATION NOTE 520

CMOS ANALOG MULTIPLEXERS AND SWITCHES; APPLICATIONS CONSIDERATIONS

BY DON JONES

INTRODUCTION

This paper is a mixed collection of answers to questions most frequently asked about CMOS analog multiplexers and switches. It covers selection criteria, parameter definitions, handling and design precautions, typical applications, and special topics such as transient considerations and R.F. switching. Some other devices which perform analog switching functions in particular applications are also discussed.

As a complement to this paper, the article, "Getting the Most Out of CMOS Devices for Analog Switching Jobs" by Ernie Thibodeaux, Electronics, December 25, 1975 is recommended reading for any analog CMOS user (reprinted in Application Note 521). This discusses the different CMOS processes used by various manufacturers, showing the performance trade-offs and particularly the different failure modes which may be encountered.

CHOOSING THE RIGHT DEVICE

A. MULTIPLEXERS: PROTECTED OR UNPROTECTED?

Harris overvoltage protected multiplexers, HI-506A/507A/508A/509A are designed for failure-proof operation in a common class of applications: any system in which the analog input signal lines originate external to the equipment. This includes most data acquisition, telemetry, and process control systems. Overvoltage protection is necessary because the signal lines are commonly subject to a number of potentially destructive situations.

1. Analog signals may be present while the MUX power supplies are off.
2. The signal lines may receive induced voltage spikes from nearby sources.
3. Static electricity may be introduced on the signal lines by personnel or equipment.
4. Grounding problems are frequent; A.C. power line voltages at high impedance can appear on the signal lines. Signal lines can be accidentally shorted to other voltage sources.

Harris protected type multiplexers will withstand a continuous voltage on any one input of ±20 Volts greater than either supply (this limitation is due only to temperature rise considerations at maximum ambient) and have withstood simulated static discharge conditions of greater than 1000 Volts.

It should be emphasized that only the HI-506A through 509A (and exact equivalents from authorized alternate suppliers) will have this kind of protection necessary for inputs from the outside world. Certain CMOS process improvements, such as "floating body" and "buried layer" do help minimize one failure mode (latchup) but will still fail under excess voltage or current conditions prevalent in this type application.

Conventional CMOS multiplexers can be protected against overvoltage destruction by external resistor-diode networks to limit input current to a safe level, but it is difficult to prevent another phenomenon with overvoltage; normally-off switching elements will tend to switch on, due to parasitic bipolar transistors in the CMOS structure, so the overvoltage spike will appear at the multiplexer output. The Harris internal protection circuits eliminate the problem by automatically shutting off the parasitic transistor during overvoltage conditions.

A simplified equivalent circuit of the Harris internal protection network is shown in Figure 1.

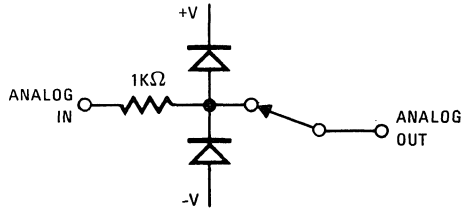


Figure 1

This will help answer the question of what happens when the supplies are turned off, but input signals are present. If the supplies are shorted to ground, then the inputs will have about 1KΩ impedance to ground. If the supplies are open circuit, then the most positive and most negative inputs will act as supplies to the multiplexer.

In normal operating parameters, internally protected multiplexers have one difference from the unprotected versions—ON resistance is necessarily higher because of the added series current limiting resistor. However, to achieve the same degree of protection with conventional devices, the same resistance must be added externally, plus external diodes which would add to the effective leakage currents.

Conventional unprotected multiplexers are suitable for systems where the MUX inputs come from sources within the equipment, such as from op amps powered by the same ±15 Volt supplies. The HI-506/507/1818A/1828A are intended for this type system. They are entirely free of any latch-up tendency, which have plagued some other types, even in these more benign applications. They are also free of the performance compromises which have accompanied some attempts to cure the latch-up problem.

B. WHICH SWITCH TO SWITCH TO?

Harris furnishes a complete line of CMOS analog switches, including replacements for most of the available CMOS and JFET switches. All types feature rugged no-latch-up construction, uniform characteristics over the analog signal range, and excellent high frequency characteristics.

The HI-200 and HI-201 replace the popular, low cost DG200 and DG201 types dual and quad switches.

The HI-1800A is a low leakage dual DPST switch with a versatile addressing scheme, allowing use of a single type for many different switching functions.

The HI-5040 through HI-5051 are low resistance types, offering one to four switches in virtually all combinations. These replace the IH-5040 series with significantly better performance, and with both 75 ohm and 30 ohm switches available in all configurations. These are also plug-in replacements for many of the DG180 and DG190 series of FET hybrid switches, offering the advantage of monolithic construction, but with slightly longer switching times.

The analog switches do not contain overvoltage protection on the analog inputs, although they will withstand inputs 2 or 4 Volts greater than the supplies. External current limiting should be provided if higher overvoltages are anticipated, such as a resistor in series with the analog input of value: R(ohms) $\geq$ (V_{IN} -V_{SUPPLY}) x 50 where V_{IN} is the maximum expected input voltage. All digital inputs do have overvoltage/static charge protection.

DATA SHEET DEFINITIONS

A. ABSOLUTE MAXIMUM RATINGS

As with all semiconductors, these are maximum conditions which may be applied to a device (one at a time) without resulting in permanent damage. The device may, or may not, operate satisfactorily under these conditions—conditions listed under "Electrical Characteristics" are the only ones guaranteed for satisfactory operation.

B. V_S, ANALOG SIGNAL RANGE

The input analog signal range over which reasonable accurate switching will take place. For supply voltages lower than nominal, V_S will be equal to the voltage span between the supplies. Note that other parameters such as R_{ON} and leakage currents are guaranteed over a smaller input range, and would tend to degrade towards the V_S limits. All Harris devices can withstand +V_S applied at an input while -V_S is applied to the output (or vice-versa) without switch breakdown—this is not true for some other manufacturers' devices.

C. R_{ON}, ON RESISTANCE

The effective series on-switch resistance measured from input to output under specified conditions. Note that R_{ON} changes with temperature (highest at high temp.) and to a lesser degree with signal voltage and current.

D. I_S(OFF), I_D(OFF), I_D(ON): LEAKAGE CURRENTS

Currents measured under conditions illustrated on data sheet. Harris prefers to guarantee only worst-case high temperature leakages, because room temperature picoampere levels are virtually impossible to measure repeatably on available automated test equipment. Even under laboratory conditions, fixture and test equipment stray leakages may frequently exceed the device leakage. Leakages tend to double every 10°C temperature rise, so it is reasonable to assume that the +25°C figure is about .001 times the +125°C measurement; however, in some cases there may be ohmic leakages, such as on the package surface, which would make the +25°C reading higher than calculated.

Each of these leakage figures is the algebraic sum of all currents at the point being measured: to each power supply, to ground, and through the switches; so the current direction cannot be predicted. In making an error analysis it should be assumed that all leakages are in the worst-case direction.

In most systems, I_D(ON) has the most effect, creating a voltage offset across the closed switch equal to I_D(ON) x R_{ON}.

E. V_{AL}, V_{AH}; INPUT THRESHOLDS

The lower and upper limits for the digital address input voltage at which the switching action takes place. All other parameters will be valid if all "0" address inputs are less than V_{AL} and all "1" inputs are greater than V_{AH}. Logic compatibility will be discussed in detail later in this paper.

F. I_A, INPUT LEAKAGE CURRENT

Current at a digital input, which may be in either direction. Digital inputs on Harris devices are similar to CMOS logic inputs; connection to MOS gates through resistor-diode protection networks. Unlike some other devices, there is no DC negative resistance region which could create an oscillating condition.

G. T_A, T_{ON}, T_{OFF}; ACCESS TIME

The logic delay time plus output rise time to the 90% point of a full scale analog output swing. After this time the output will continue to rise, approaching the 100% point on an exponential curve determined by $R_{ON} \times C_D(OFF)$.

H. T_{OPEN}, BREAK-BEFORE-MAKE DELAY

The time delay between one switch turning OFF and another switch turning ON; both switches being commanded simultaneously. This prevents a momentary condition of both switches being ON, generally a very minor problem.

I. $C_S(OFF)$, $C_D(OFF$, $C_D(ON)$ INPUT/OUTPUT CAPACITANCE

Capacitance with respect to ground measured at the analog input/output terminals. $C_D(ON)$ is generally the sum of $C_S(OFF)$ and $C_D(OFF)$. $C_D(OFF)$ is usually the most important term as rise time/settling characteristics are determined by $R_{ON} \times C_D(OFF)$, as well as the high frequency transmission characteristics.

J. $C_{DS}(OFF)$, DRAIN TO SOURCE CAPACITANCE

The equivalent capacitance shunting an open switch.

K. OFF ISOLATION

The proportion of a high frequency signal applied to an open switch input appearing at the output: off isolation = 20 log $\frac{V_{IN.}}{V_{OUT}}$ This feedthrough is transmitted through $C_{DS}(OFF)$ to a load composed of $C_D(OFF)$ in parallel with the external load. The isolation generally decreases by 6dB/octave with increasing frequency.

L. C_A, DIGITAL INPUT CAPACITANCE

Capacitance to ground measured at digital input. This chiefly affects propagation delays when driven by CMOS logic.

M. P_D, POWER DISSIPATION: I+, I-

Quiescent power dissipation, $P_D = (V+ \times I+) + (V- \times I-)$. This may be specified both operating and standby ("Enable" pin ON/OFF). Note that, as with all CMOS devices, dissipation increases with switching frequency; but that Harris devices exhibit much less of this effect.

CARE AND FEEDING OF MULTIPLEXERS AND SWITCHES

Dielectrically isolated CMOS I.C.'s require no more care in handling and use than any other semiconductor—bipolar or otherwise. However, they are not indestructible, and reasonable common sense care should be taken.

In a laboratory breadboard, power should be shut off before inserting or removing any I.C.. It is especially important that supply lines have decoupling capacitors to ground permanently installed at the I.C. socket pins, as intermittent supply connections can create high voltage spikes through the inductance of a few feet of wire.

Because each of the major manufacturers of CMOS multiplexers and switches uses a radically different process, it is urged that units from all prospective suppliers be equally tested in breadboards and prototypes. It will be interesting to note which types survive best the hazards of a few weeks of breadboard testing.

Particular care of semiconductors during incoming inspection and installation is quite important, because the cost of reworking finished assemblies with even a small percentage of preventable failures can seriously erode profits. All equipment should be periodically inspected for proper grounding. With these devices, it is not usually necessary to shackle personnel to the nearest water pipe, if reasonable attention is paid to clothing and floor coverings; but be alert for periods of unusually high static electricity. If special lines are already set up for handling MOS devices, it wouldn't hurt to use them.

There are a few good rules for P.C. card layout:

1. Each card or removable subassembly should contain decoupling capacitors for each supply line to ground. This not only helps keep noise away from the analog lines, but gives good protection from static electricity damage when loose cards are handled.
2. When digital inputs come through a card connector, the pull-up resistor should be at the CMOS input. This forces current through the connector and prevents possible dry circuit conditions (see following discussion on digital interface).
3. All unused digital inputs must be tied to logic "0" (ground) or logic "1" (logic supply or

device + supply) depending on truth table and action desired. Open inputs tend to oscillate between "0" and "1". It would also be best to ground any unused analog inputs/outputs and any uncommitted device pins.

DIGITAL INTERFACE

A. REFERENCE CONNECTION

HI-5040 through HI-5051 and HI-1800A/1818A/1828A require a connection to the digital logic supply (+5V to +15V)..

The HI-200/201/506A/507A have V_{REF} pins which are normally left open when driving from +5 Volt logic (DTL or TTL), but may be connected to higher logic supplies (to +15V) to raise the threshold levels when driving from CMOS or HNIL. The HI-200/201 will have significantly lower power dissipation when V_{REF} is connected to a high level supply.

The HI-506/507/508A/509A do not have V_{REF} terminals, but will operate reliably with any logic supplied from +5 to +15 Volts.

B. DTL/TTL INTERFACE

One major difference found in comparisons of similar devices from different manufacturers is the worst-case digital input high threshold (V_{AH} or V_{IH}). These range anywhere from +2V to +5V; and anything greater than +2.4V is obviously not compatible with worst-case TTL output levels. The fact is that no CMOS input is truly TTL compatible unless an external pull-up resistor is added. TTL output stages were not designed with CMOS loads in mind.

The experienced designer will always add a pull-up resistor from the CMOS input to the +5 Volt supply when driving from TTL/DTL:

1. Interchangeability: allows subsititution of similar devices from several manufacturers.
2. Noise immunity: a TTL output in the "high" condition can be quite high impedance. Even when voltage noise immunity seems satisfactory, the line is quite susceptible to induced noise. The pull-up resistor will reduce the impedance while increasing voltage noise immunity.
3. Compatibility: one manufacturer does guarantee +2.0 Volt minimum V_{AH}. However, this is accomplished with circuitry that is anything but TTL compatible: input current vs. voltage shows an abrupt positive then negative resistance region which is not the kind of load recommended for an emitter follower stage. A pull-up resistor will swamp out the negative resistance. Other CMOS inputs capacitively couple internal switching spikes to the input which could cause double-triggering without the pull-up resistor.
4. Reliability: it shouldn't happen with carefully processed I.C.'s; but any possible long term degradation of CMOS devices usually involves threshold voltage shifts. The pull-up resistor will help maintain operation if input thresholds drift out of spec. On units without adequate input protection, the resistor will also help protect the device when a loose P.C. card is handled. Where the interface goes through a P.C. connector, the resistor will force current through the connector to break down any insulating film which otherwise might build up and cause erratic dry circuit operation.

   A 2K ohm resistor connected from the CMOS input to the +5 Volt supply is adequate for any TTL type output. If power consumption is critical, open collector TTL/DTL should be used, allowing a higher value resistor—the voltage drop across the resistor is computed from the sum of specified "1" level leakage currents at the TTL output and CMOS input.

C. CMOS INTERFACE

The digital input circuitry on all Harris devices is identical to series 4000 and 54C/74C logic inputs, and is compatible with CMOS logic with supplies between +5V and +15V without external pull-up resistors.

D. ELECTROMECHANICAL INTERFACE

When driving inputs from mechanical switches or relays, either a pull-up or pull-down resistor must be connected at the CMOS input to clear the dry circuit and damp out any spikes, as illustrated in Figure 2, (b) and (c).

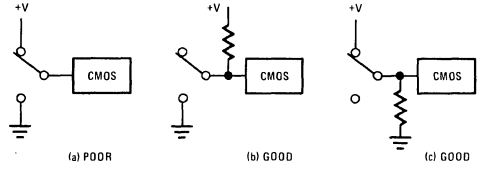


Figure 2

A PRACTICAL MULTIPLEXER APPLICATION

Figure 3 illustrates a practical data acquisition system hookup using an analog multiplexer, a monolithic sample-and-hold and an A/D converter. The HA-2420/2425 sample-and-hold is a particularly good choice for this type application because it eliminates the need for a separate high impedance, high slew rate buffer amplifier. Its acquisition time is consistent with CMOS multiplexer settling times and most available A/D conversion times. Errors, after initial

adjustment, are consistent with up to 12 bit absolute accuracy over a wide temperature range.

A. ACCURACY

D.C. error sources include:

1. Multiplexer:
   a. input offset = R source x I_S(OFF)
   b. output offset = R(ON) x (I_D(ON) + I bias (S/H))
2. Sample-and-hold
   a. input offset voltage
   b. charge injection; sample-to-hold offset
   c. gain error during "hold"
   d. drift during hold
3. A/D converter:
   a. linearity
   b. gain drift
   c. offset drift

Item 1(a) and (b), and 2(d) become significant only at very high temperatures. 2(a) and (b) are initially adjusted out with the offset adjustment pot on the S/H. 2(c) is usually adjusted out by A/D gain adjustment, but could also be removed by a voltage divider feedback on the S/H to give a slightly greater than unity gain during "sample". After initial adjustments, typical S/H errors are less than 0.5mV over 0° to +75°C. Note that after adjustment, there may be an appreciable offset at the S/H output when switching from sample to hold. This is not a problem, since accuracy is required only during "hold", and the system is adjusted for this.

The largest system errors are usually 3(b) and (c), drifts with temperature and time. If two multiplexer channels can be dedicated for stable (+) and (-) reference voltage inputs, then the data processor can continuously calibrate the system, effectively removing all errors, except 1(a) and 3(a) which are usually negligible.

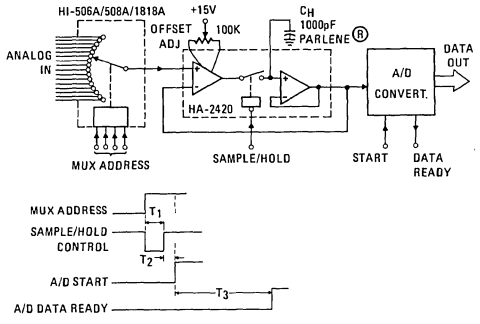


Figure 3

B. TIMING

The timing diagram in Figure 3 indicates the necessary system delays for each multiplexer address:

T_1 is the combined acquisition time for the multiplexer and S/H.

T_2 is the short interval required for the sample-to-hold transient to settle.

T_3 is the A/D conversion time.

The following table indicates minimum recommended timing for ± 10 Volt input range for acquisition/settling times to ½ L.S.B. accuracy:

	T_1	T_2
10 bit:	6μS	1μS
12 bit:	12μS	2μS

The multiplexer, by itself, requires about 2 μs and 9 μs settling to 10 bit and 12 bit accuracy, respectively; but fortunately this can be concurrent with S/H acquisition time. This is longer than would be predicted by the R_{ON} C_D time constant; probably because of internal distributed capacitance, a rather long period is required to traverse the last few millivolts towards the final value.

It should be noted that impedance conditions at the multiplexer inputs can affect the necessary acquisition time. At the instant the multiplexer switches from one channel to a new one, there is appreciable current pulled through the new channel input in order to charge C_D from its old level to its new level. This can cause ringing on signal lines, or glitches at signal conditioning amplifier outputs which require longer periods to settle. It is best for signal conditioning amplifiers to be wide band types, such as HA-2600, so that their high frequency output impedance is low and recovery from load transients is fast; even though the signal to be measured is very low bandwidth.

The T_1 and T_2 times could be eliminated by alternating two S/H circuits, acquiring a new signal on the second while A/D conversion is taking place. The two S/H circuits would have inputs connected together, and outputs alternately connected to the A/D by an analog switch. Total time, then, would be T_3 plus the analog switch settling time.

If the MUX input channels are sequentially switched, each channel will be sampled at a rate of

$$F_S = \frac{1}{N(T_1 + T_2 + T_3)}$$ samples per second, where N is the number of channels. The frequency spectra of the input signals must then be no higher than $\frac{F_S}{2}$.

In many systems, however, each channel carries a different maximum frequency of interest, and it may be desirable to depart from simple sequential scanning. Quickly varying signals, for example, could be addressed several times during a scanning period.

C. ADDING CHANNELS

For more than sixteen channels, several multiplexers may be tied together at the outputs, and addressed in parallel, but with only one "enabled" at a time. The MUX output offset will be increased, since I_D (OFF or ON) is additive. Also, output capacitance, C_D, is additive, creating increased access times.

These errors can be minimized in large systems by

having several tiered levels of multiplexing; where the outputs of a number of MUX's are individually connected to the inputs of another MUX.

D. DIFFERENTIAL MULTIPLEXING

When low level analog signals must be conducted over a distance, it is generally better, from a noise pickup standpoint, to use a balanced transmission line carrying signals which are differential with respect to ground.

A dual multiplexer is used for this purpose, as shown in Figure 4. Two sample-and-hold circuits plus an op amp form a high impedance differential sample-and-hold with gain. At gains greater than 4, the minimum sampling time (T_1 in previous example) must be increased proportionately to gain to allow for overdamped settling characteristics.

When handling low level, or high impedance signals, consideration should be given to adding signal conditioning amplifiers at the signal sources, since this can often produce less troublesome, more accurate, lower cost systems.

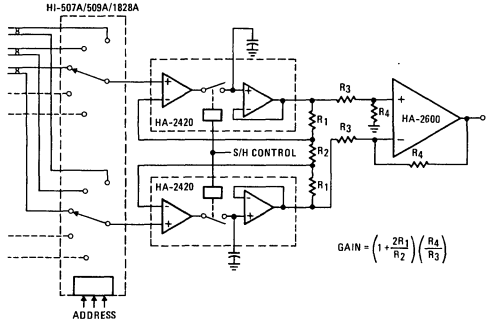


Figure 4

E. DEMULTIPLEXING

Since the switches in a CMOS MUX conduct equally well in either direction, it is perfectly feasible to use it as a single input-selected multiple output switch. Figure 5 illustrates its use as a demultiplexer, with capacitors to hold the output signal between samples. When the address lines are synchronous with the address of the original multiplexer, the output lines will recreate the original inputs, except level changes will be in steps.

Overvoltage protection is not effective with signals injected at the normal MUX output, so an external network should be added, if necessary.

A more accurate demultiplexer could be constructed using the HA-2420/2425 sample-and-hold for each channel, connecting inputs together and sampling each channel sequentially.

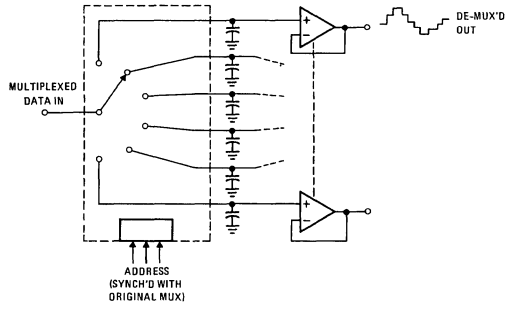


Figure 5

ANALOG SWITCH APPLICATIONS

A. HIGH CURRENT SWITCHING

Analog switches are sometimes required to conduct appreciable amounts of current, either continuous, or instantaneous—such as charging or discharging a capacitor. For best reliability, it is recommended that instantaneous current be limited to less than 80mA peak and that average power over any 100 millisecond period be limited to $I^2R_{ON} \leq$ (absolute max. derated power—quiescent power). Note that R_{ON} increases at high current levels, which is characteristic of any FET switch. Switching elements may be connected in parallel to reduce R_{ON}.

B. OP AMP SWITCHING APPLICATIONS

When analog switches are used either to select an op amp input, or to change op amp gain, minor circuit rearrangements can frequently enhance accuracy. In Figure 6 (a), R_{ON} of the input selector switch adds to R_1, reducing gain and allowing gain to change with temperature. By switching into a non-inverting amplifier (b), gain change becomes negligible. Similarly, in a gain switching circuit, R_{ON} is part of the gain determining network in (c), but has negligible effect in (d).

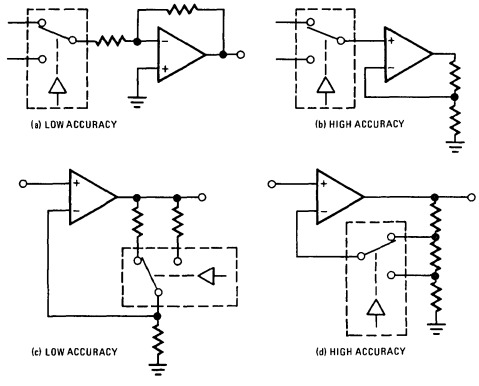


Figure 6

C. SWITCHING SPIKES AND CHARGE INJECTION

Transient effects when turning a switch off or on are of concern in certain applications. Short duration spikes are generated (Figure 7 (a)) as a result of capacitive coupling between digital signals and the analog output. These have the effect of creating an acquisition time interval during which the output level is invalid even when little or no steady state level change is involved. The total net energy (charge injection) coupled to the analog circuit is of concern when switching the voltage on a capacitor, since the injected charge will change the capacitor voltage at the instant the switch is opened (Figure 7 (b)).

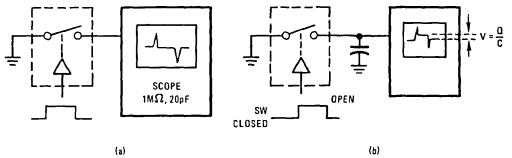


Figure 7

Charge injection is measured in pico Coulombs; the voltage transferred to the capacitor computed by

$$V = \frac{\text{Charge (pC)}}{\text{Capacitance (pF)}}$$

Both of these effects are, in general, considerably less for CMOS switches than for equivalent resistance JFET or PMOS devices, since the gate drive signals for the two switching transistors are of opposite polarity. However, complete cancellation is not possible, since the N and P channel switches do not receive gate signals quite simultaneously, and their geometrics are necessarily different to achieve the desired D.C. resistance match.

In applications where transients create a problem, it is frequently possible to minimize the effect by cancellation in a differential circuit, similar to Figure 8.

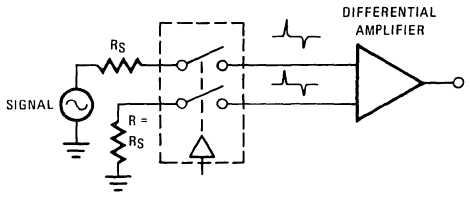


Figure 8

Among the Harris anlog switches, the HI-201 is the best from the transient standpoint, having turn-on spikes of about 100mV peak, 50ns width at the 50% point, and charge injection at turn-off of about 20 pico Coulombs. Transients of the HI-5040 series are several times higher.

D. HIGH FREQUENCY SWITCHING

When considering a switching element for R.F. or video type information, two factors must be watched: attenuation vs. frequency characteristics of an ON switch, and feedthrough vs. frequency characteristics of the OFF switch. Optimizing the first characteristic requires a low $R_{ON} \times C_D$ product, and the second a low value of C_{DS} (OFF).

The 30 ohm switch types of the HI-5040 series appear to best meet these requirements, and testing at high frequencies has verified this.

Figure 9 illustrates these circuit configurations; (a) is a simple series switch, (b) is a series-shunt configuration to reduce feedthrough, and (c) is a SPDT selector configuration with series-shunt elements. A 1K ohm load is illustrated, which might be the input impedance of a buffer amplifier stage; a lower load resistance would improve the response characteristics, but would create greater losses in the switch and would tend to distort high level signals.

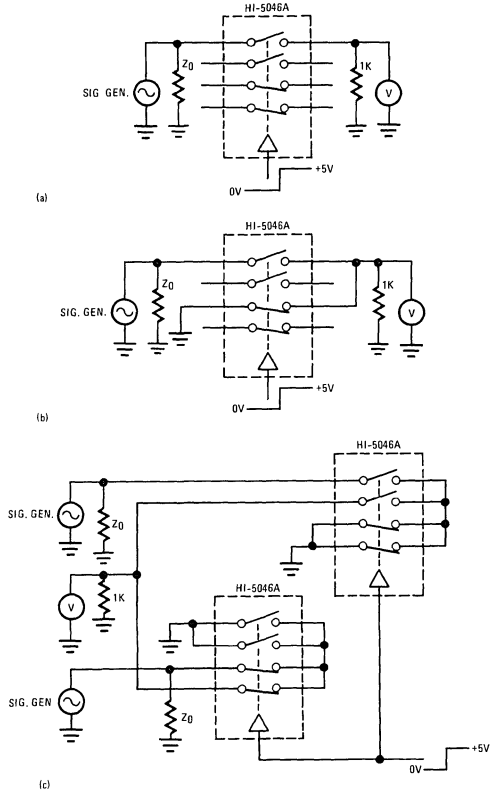


Figure 9

Figure 10 shows ON and OFF frequency response for each of the above configurations. Arbitrarily, we will define useful frequency response as the

region where ON losses are less than -3dB and OFF isolation is greater than -40dB.

The simple configuration (a) has excellent ON response, but OFF isolation limits the useful range to about 1MHz (the data sheet indicates -80dB isolation at 100kHz, but this is measured with 100 ohms load, which accounts for the 20dB difference).

The circuit in (b) shows a good improvement in isolation produced by the low impedance of the shunt switch. The useful range is about 10MHz; which could also be achieved in a simple SPDT 2-switch selector if source impedances are very low.

The selector switch in (c) has excellent characteristics, both ON and OFF curves indicating 40MHz useful response. Additional switches connected to the same point would reduce the ON response because of added shunt capacitance; but this could be eliminated by feeding separate summing amplifier inputs.

Careful layout is, of course, important for high frequency switching applications to avoid feedthrough paths or excessive load capacitance.

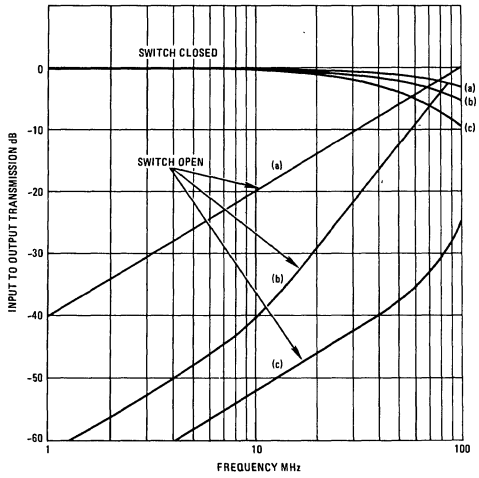


Figure 10

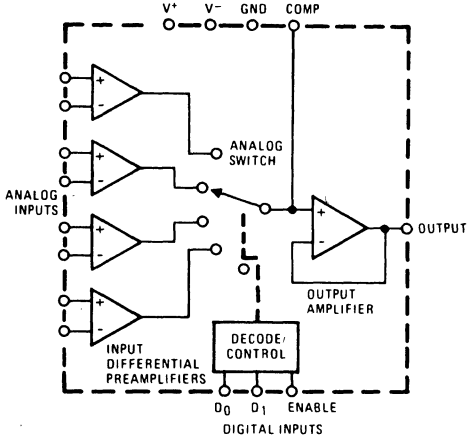
ALTERNATIVES TO CMOS SWITCHES AND MULTIPLEXERS

CMOS devices are excellent in many applications. However, there are some other devices which merit consideration in certain analog switching circuits where they may improve performance, reduce parts count, or be more economical.

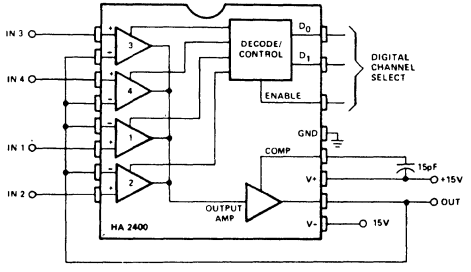
A. THE PRAM, PROGRAMMABLE AMPLIFIER

The HA-2400/2405 is a unique monolithic bipolar circuit which combines analog switching with high performance operational amplifiers. It basically consists of four op amp type input stages, any one of which is connected to a single output by bipolar switches controlled through a TTL compatible address decoder. In a single package, it contains the equivalent of 5 op amps plus a 4 channel mulitplexer. It has literally hundreds of applications in signal selection and programmable signal conditioning.

Figure 11 illustrates a four channel multiplexer. Connections from the output to each input stage are always the same as a comparable op amp circuit; the +1 gain connection is illustrated.



(a) FUNCTIONAL DIAGRAM



(b) ANALOG MULTIPLEXER WITH BUFFERED INPUT AND OUTPUT

Figure 11

Advantages over a comparable CMOS multiplexer circuit are as follows:

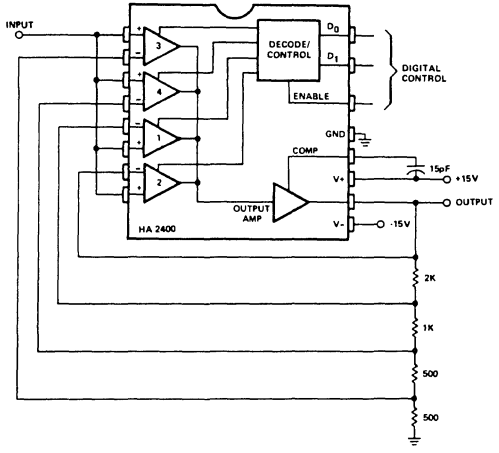
1. High input impedance (10^{12} ohms), low output impedance (< 0.1 ohm) means that ON resistance and leakage currents are no longer of concern. There is negligible transient loading of input lines.
2. Gain filtering, etc. can easily be added with feedback networks.
3. Fast acquisition (1.5μS).

4. Wide bandwidth (8 MHz).
5. Superior feedthrough characteristics (-110dB at 10kHz, -60dB at 1MHz).

Disadvantages include:

1. Less accuracy for low level D.C. signals; the offset voltages of each input stage do not necessarily match or track each other.
2. Cannot be used in reverse as a demultiplexer.
3. Disabling the device (enable pin low) does not open the output line, or drive the output to zero. Adding channels may be accomplished by tieing compensation pins together.

Figure 12 illustrates the PRAM used as a programmable gain amplifier. Any connection possible with op amps can be wired 4 ways to make programmable active filters, oscillators, etc., etc. Harris Application Note 514 shows many possibilities.



AMPLIFIER, NON-INVERTING PROGRAMMABLE GAIN

Figure 12

B. SAMPLE-AND-HOLD

The sample-and-hold function has often been accomplished with separate analog switches and op amps. These designs always involve performance tradeoffs between acquisition time, charge injection, and droop rate.

The HA-2420/2425 monolithic sample-and-hold, illustrated previously in Figure 3 has many times better tradeoffs, usually at a lower total cost than the other approaches. The switching element is a complementary bipolar circuit with feedback which allows high charging currents (30mA), low charge injection (10pC), and ultra low OFF leakage current (5pA); a combination not approached in any other electronic switch. These factors make it also superior as an integrator reset switch, or as a precision peak detector as shown in Figure 13. Harris Application Note 517 illustrates many other applications.

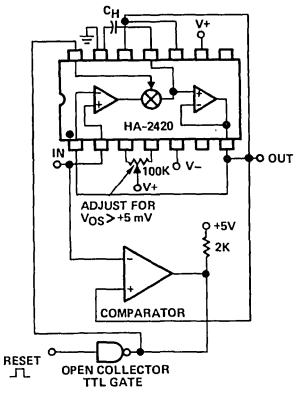


Figure 13

C. PROGRAMMABLE SUPPLY CURRENT OP AMPS

The HA-2720/2725 and HA-2730/2735 (dual amp) are op amps with an extra terminal which is used to control quiescent supply current. These are most generally used in low power systems to optimize the power dissipation vs. bandwidth and slew rate tradeoffs. They can also be used with variable set currents to make linearly variable oscillators, filters, etc. Another application is a switchable op amp as shown in Figure 14.

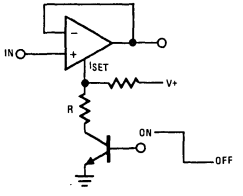


Figure 14

The illustrated transistor could be the output of high voltage open collector gate. The set resistor R is chosen so that the set current is the desired value when the transistor is ON, considering that the voltage at I_{SET} terminal when ON is about 2 forward junction drops ($\sim$ 1.5V) below V+. When the transistor is turned OFF, amplifier input, output, and supply terminals become very high impedance, so that two or more amplifier outputs could alternately be switched to the same point.

Off isolation with a 2,000 ohm load is about -80dB at 10kHz.

D. CHOPPER STABILIZED AMPLIFIER

Analog switches are sometimes used as choppers for amplifying low level D.C. signals with low offset errors. The HA-2900/2905 is a monolithic chopper stabilized amplifier in a TO-99 can. Typical offset drifts are 0.2 μV/^{o}C and 1pA/^{o}C with 5 x 10^8 open loop gain. Harris Application Note 518 describes this device.

HARRIS

APPLICATION NOTE
521

GETTING THE MOST OUT OF C-MOS DEVICES FOR ANALOG SWITCHING JOBS

BY ERNIE THIBODEAUX

INTRODUCTION

Although most designers appreciate the benefits of the complementary-MOS process for digital design, few realize how effective the technology can be for analog switching. C-MOS analog switches, which consume less power than bipolar devices, exhibit no dc offset voltage and can handle signals up to the supply rails. The C-MOS bilateral property furnishes input and output functions, making multiplexing and demultiplexing possible. In addition, the on-resistance of an MOS switch is as low as 30 ohms—a third as much as a bipolar device.

Unfortunately, C-MOS analog switches, which until recently were built with junction isolation, have been difficult to design into analog multiplexers and switches. The devices latched up easily, their C-MOS inputs were destroyed by electrostatic charges, and they literally went up in smoke when confronted with input overvoltage spikes and power-supply transients. To prevent destruction, costly external protective circuits were needed, and, even then, the devices latched up unless the power was turned on and off in a set sequence.

Because latch-up problems limited the use of analog switches so severely, device designers focused a great deal of attention on eliminating the condition. Recently, the success has been noteworthy. Indeed, three new technologies now offer latch-free analog switch operation: latch-proof junction isolation (JI), floating-body junction isolation, and dielectric isolation (DI).

Both JI techniques are conventional processes that have been slightly modified to alleviate the old problem of latch-up. However, both of these JI technologies still require costly external protection circuits to guard against burn-out in such applications as analog-signal multiplexing that interface them with the outside world. That is why JI devices are best suited for internal-switching applications where the electrical environment can be controlled. In contrast, the improved DI technology, by virtue of its construction, offers analog-switching devices suitable for many inside applications, as well as providing inboard analog protection for devices that interface with the other circuits. Happily, the smaller substrate area of the DI device delivers a better speed-power product than the JI technology.

THE BASIC C-MOS SWITCH

The basic C-MOS transistor (Fig. 1) has parasitic junctions that are reverse-biased during normal operation. However, certain overvoltage conditions can forward-bias these junctions to cause high currents that could possibly destroy the devices.

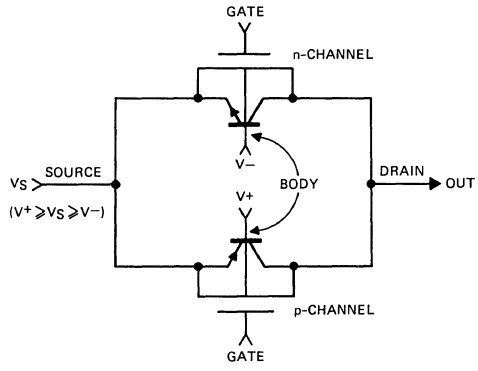


Figure 1. Bad

In the basic C-MOS analog switch, the parasitic junctions are reversed-biased during normal operation. Large overvoltages, however, make them forward-biased and draw large currents.

The parasitic junctions are actually npn and pnp transistors that are normally reverse-biased by the applied body potentials. However, because many analog switches, and especially multiplexers, are connected to their analog sources through long lines, they are highly susceptible to externally induced voltage spikes. For example, these spikes, which can often exceed the p-channel body potential, V+, can inadvertently turn on a normally off switch

8

through the parasitic pnp transistor (Fig. 1).

The n-channel device is similarly affected when the parasitic npn transistor is turned on by a negative overvoltage. This action, commonly known as channel interaction, causes momentary channel-to-channel shorting, which introduces significant errors in the system. This intermittent condition, which is seldom destructive, is rarely isolated because it occurs only randomly.

One of the adverse effects of channel interaction is illustrated in Fig. 2. Channel 1 of an analog multiplexer is selected when all other channels are off. Channel 16 receives an input-noise spike that momentarily exceeds the positive supply. The sequence causes channel 1 read-out to be +16V because of interaction with channel 16 just before initiating the hold command to the sample-and-hold device. To prevent this annoyance requires additional protective circuits that clamp each channel input to a voltage below the threshold of the parasitics to ensure that the channels remain inactive under any conditions.

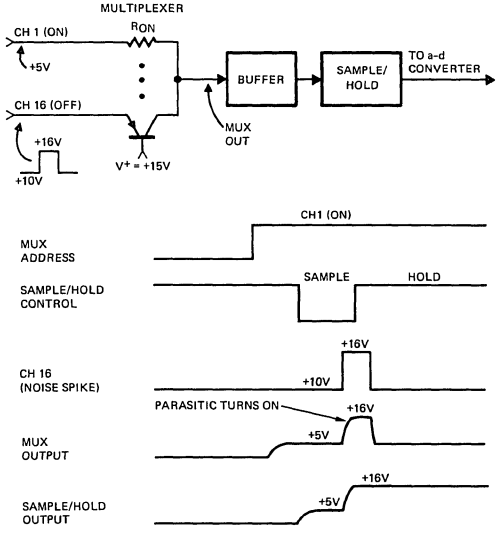


Figure 2. Worse

With CMOS devices, noise spikes can cause channel interaction. In this multiplexer, although channel 1 is only one selected, noise spikes cause cross talk in channel 16, which affects reading.

A more serious condition exists when the substrates (p- or n-) lose their respective potentials to ground (Fig. 3) —a condition that occurs when power to the device is turned off while the analog signals are still present. In this situation, the analog switch, which at that point represents a diode connected through the low impedance of the supply, draws high current from the analog source.

This current turns on the switch through its parasitics and shorts all channels to the output. These shorts can easily be catastrophic in multiplexer systems that have different power supplies for the analog source and the multiplexer switch. An error during troubleshooting or an inadvertent supply glitch can trigger this fault mode and destroy the whole system. Therefore, there is obviously much more to system reliability than having latch-proof C-MOS devices.

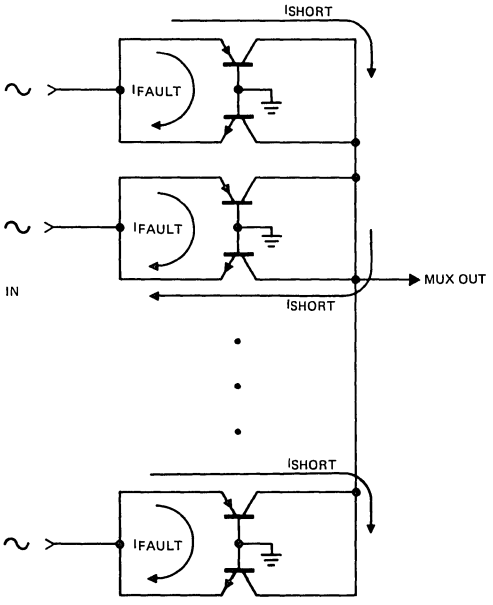


Figure 3. Still Worse

Most serious in CMOS switches is losing substrate potential to ground. This condition, which happens when power is lost and the analog signal is present, causes very high currents.

CONSIDERING LATCH-PROOF JI TECHNOLOGY

The standard JI process has been modified by what is claimed to be latch-proof construction through control of the effective betas of the parasitic transistors. A cross section in Fig. 4(a) shows the C-MOS structure along with its parasitic transistors and the equivalent circuit in Fig. 4(b) that gives rise to the silicon-controlled-rectifier latch-up problem.

Under any of the fault conditions previously mentioned, the npn and/or pnp can trigger this quasi-dual-gate SCR into a state of high conduction. If the transistor β product is 1 or greater, this configuration is sustained until either the device burns up or all sources of power are removed. By using a buried-layer configuration, as shown in the cross section, the β product is reduced to less than 1, eliminating the latch-up conditions.

Again, especially in multiplexer applications, the latch-free devices do not guarantee against destruction, and the JI multiplexer still requires costly discrete circuits around the device, as shown in Fig 5. If an overvoltage exists, the resistor/diode circuit at each analog input limits the input voltage to the

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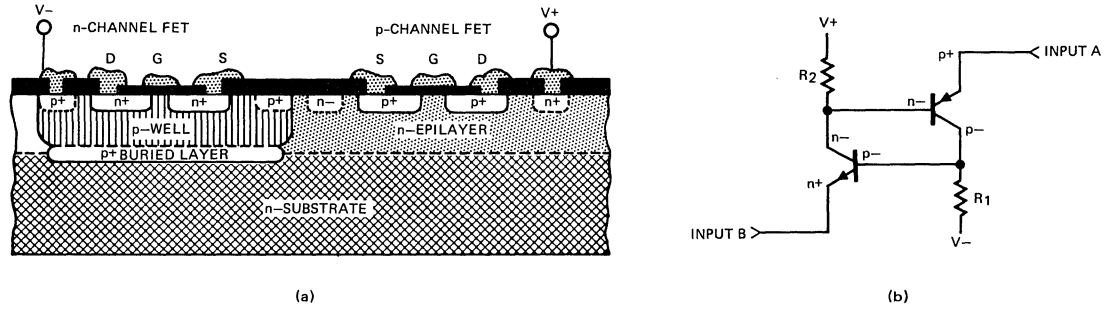

Figure 4. Latch-Proof. Junction-isolated devices are now made latch-proof with a buried-layer configuration (a), which keeps beta of parasitic transistor under unity. That kills chance for latch-up (b), which plagues devices built with older junction-isolation technology.

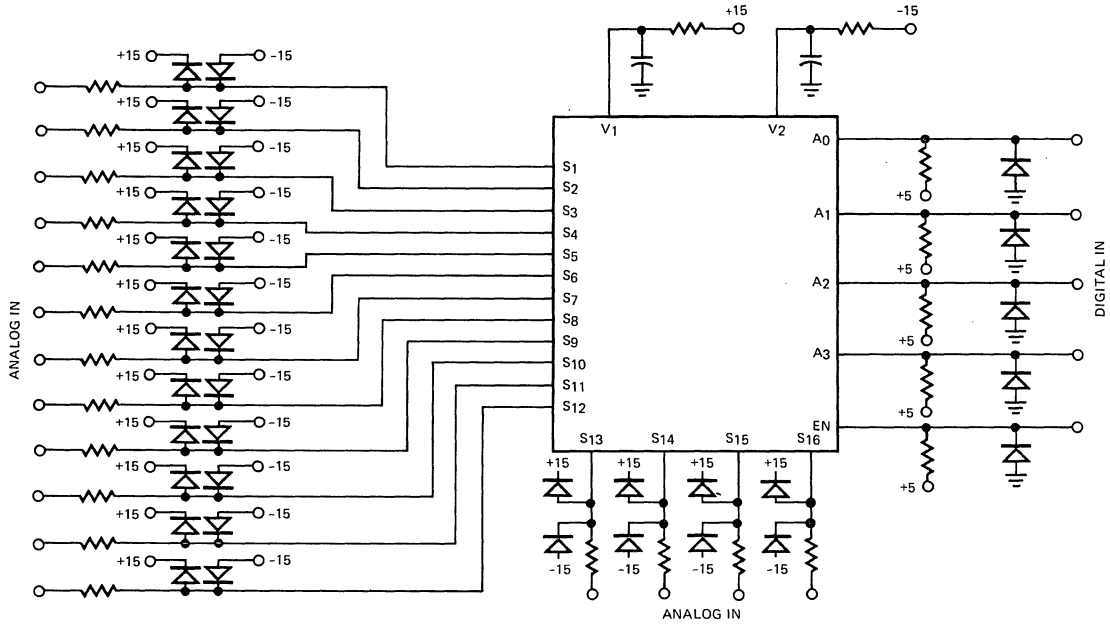

Figure 5. Protection still needed. Although new JI devices won't latch up, they still can be destroyed by large currents. That's why typical JI multiplexers, like the one shown here, still need to be surrounded by external protective components, which drive up system costs.

supply-voltage range to prevent the parasitic transistor action.

The resistors limit the overvoltage currents through the diodes. The diodes must have a low threshold voltage—much lower than the 0.6V silicon-junction threshold of the internal parasitic diodes—to ensure that the parasitics do not turn on.

A germanium diode offers a low threshold voltage, but its high leakage current makes it impractical, especially in 0.1% systems. Therefore, in most applications, more expensive low-leakage diodes are used.

For example, Schottky diodes meet the requirements, but they cost about 50 cents each in volume, and the total cost per multiplexer, including parts and labor, for the discrete protection circuit may well be double the initial purchase price of the device. Even then, its reliability will never approach that of an IC that has this protection already built in.

THE FLOATING-BODY JI TECHNOLOGY

Standard JI technology allows another approach to latch-proof device construction: a portion of the SCR continuity is broken by floating the "body" or substrate of the n-channel switching device. A cross section of this process is similar to that in Fig. 4(a), excluding the buried layer and the negative supply connection to the p- substrate, so that the dual-gate SCR is changed to a single -gate device that can only be triggered by the pnp parasitic. This, of course, reduces the latch-up probability by 50%.

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To completely eliminate latch-up, as before, the β product of the transistors is reduced to less than 1. This accomplishment, certainly a significant improvement over the conventional process, offers greater reliability, but certain trade-offs must be made when the body of a MOSFET is floated.

Nominal source-to-drain breakdown voltages are reduced which limit the peak-to-peak signal range. Over-all breakdown is limited by the collector-emitter breakdown voltage, BV_{CEO}, of the npn parasitic transistor of the floating n-channel MOSFET. The breakdown voltage increases with the degree of reverse-bias potential applied to the substrate. With a floating body, BV_{CEO} is minimum, so particular care is necessary when using these devices in configurations such as single-pole single-throw, single-pole double-throw, dpst, and dpdt, where each side of the switch connects to opposite polarities. The peak-to-peak handling capability is specified at a minimum of 22V; therefore, 30V pk-pk cannot be switched with ± 15V supplies, as it can with other C-MOS devices.

What's more, the leakage currents of floating-body JI devices are higher than other types, simply because the I_{CEO} of the floating base for the npn is much greater than the I_{CBO} of other devices having fixed reversed-biased body potentials. The increased leakage currents in spst switches may not be too significant.

However, in multiplexers that have the outputs of as many as 16 switches tied together in one IC, the total summation of currents can significantly affect system accuracy. For example, the specification for a worst-case 16-channel floating-body multiplexer is 10 microamperes, and the channel on resistance is 550 ohms . The dc-offset error would be 5.5 millivolts, representing an accuracy to 0.055%.

Other 16-channel types specify worst-case parameters of 500 nanoamperes and channel resistance between 550 ohms and 2 kilohms. Their dc-offset error is between 0.28 mV and 1 mV, respectively, allowing accuracy to 0.01% or better.

Finally, the effective off impedance of the floating-body switch is degraded by the floating-body technique. Off-isolation characteristics of a MOSFET are primarily determined by its source-to-drain capacitance. But with the base floating, the effective capacitance from emitter to collector is increased by the series combination of emitter-base and base-collector-junction capacitances (Fig. 6a). This increase degrades the over-all off-isolation characteristics. For example, the off isolation for a typical floating-body channel at 1 megahertz that has RL = 100 ohms is specified to be -54 decibels, which compares favorable with other types. However, at lower frequencies such as 1 kHz, the isolation is only -62dB, compared to more than -110dB for improved devices. Capacitances C_1 and C_2 for them are shunted by the low ac impedance of the supply voltage (Fig. 6b).

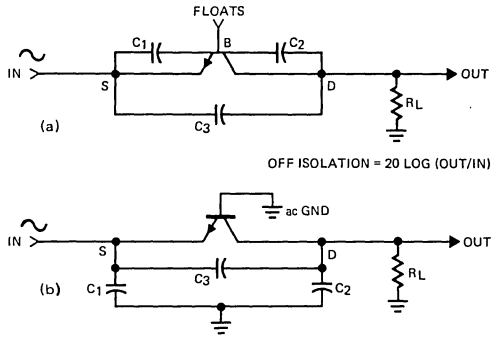

Figure 6. Floating Bodies
Floating-body switches have degraded "off" impedance because total capacitance (a) combines two junction capacitances. In DI circuit (b), capacitances are shunted out.

THE LINEAR DIELECTRIC-ISOLATION TECHNOLOGY

The linear dielectric-isolation process requires no modifications to guard against latch-up. Its basic construction ensures that the SCR configuration that causes latch-up can not exist. The functional cross section in Fig. 7 reveals the silicon-dioxide isolation barrier fabricated between all parasitic transistors. This isolation allows each active element to be self-contained and independent with no interface junctions. At most, only three-layer structures are permitted for each tub, so that four-layer strucures, or SCRs, are impossible. Also, since the DI technology requires no guard bands, junction capacitances, leakage currents, and size are minimized. The resulting increase in packing density per wafer, together with increased yields, enables these devices to be cost-competitive with other types.

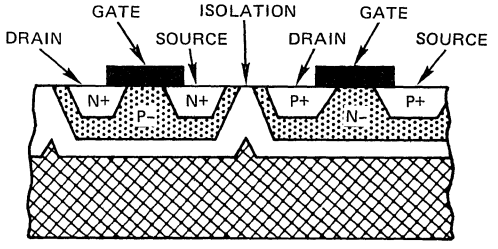

Figure 7. How DI Does It
Dielectric isolation eliminates latch-up by a silicon-dioxide isolation barrier between devices. This separates all active elements, eliminating interface junctions that cause parasitic SCR's.

In working with DI devices, the IC designer is not burdened with the fixed substrate potentials found in JI devices. He may let the substrate float, fix it to some potential, or even modulate it. Fig. 8 depicts a typical DI analog switch circuit that minimizes the variation of on resistance with the analog signal. Ordinarily, in conventional circuits, the body or

substrate potentials of the n and p-channel devices are fixed and the source-to-body bias potentials vary with the analog input voltage. This change in body bias causes a wide variation of on resistance within the analog signal range. However, in the DI circuit, the bodies of P_1 and N_1 are connected together through N_3 during the on state. This allows the body to follow the input voltage providing a constant source-body bias and therefore a constant on resistance. During the off state, the bodies of N_1 and P_1 are at their respective supply potentials through P_2 and N_2, thereby preserving high off isolation and low leakage currents.

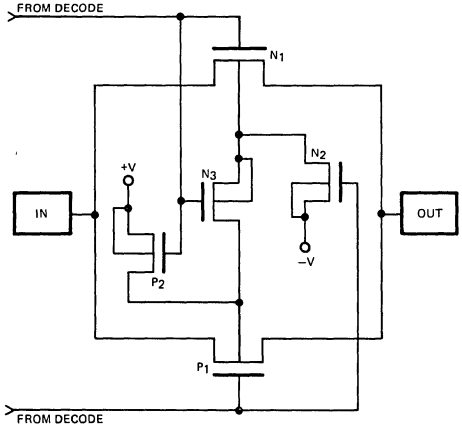

Figure 8. DI Does It

In dielectrically isolated switches, on resistance modulation by the analog input is minimized by connecting N_1 and P_1 bodies together through N_3.

DESIGNING A FOOLPROOF C-MOS ANALOG MULTIPLEXER

In dielectrically isolated multiplexer circuits, protection can be provided on the chip primarily to eliminate channel interaction. This protection prevents normally off channels from being turned on by parasitics from other channels. And because this interaction is prevented, even worst-case power-supply faults cannot destroy the device. Moreover, since DI structures have no SCR effect, protection against latch-up and power-sequencing are not necessary. In short, DI multiplexers with built-in protection can withstand virtually any conceivable fault from the outside world.

The typical protected DI multiplexer (Fig. 9) benefits from a combined bipolar/C-MOS technology. The illustrated bipolar section is used to sense an analog overvoltage condition and steer current away from the parasitic MOSFET junctions. Each of the switching devices, N_1 and P_1, has its own protection circuits. Devices P_3, D_6, D_7 and Q_6 protect P_1 while N_3, D_4, D_5, and Q_5 protect N_1. When the switch is off, the substrate of the p-channel FET, P_1, is connected to V+ through P_3 and diode D_7 for maximum isolation and low leakage currents in the off state. If the input voltage suddenly exceeds V+, the source-body junction, which would normally conduct, is instead clamped by transistor Q_6.

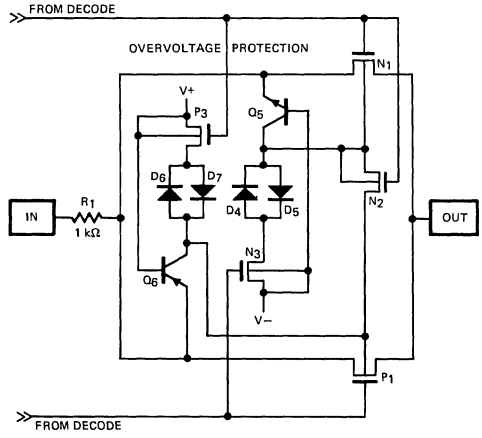

Figure 9. Winning Combination

Combining bipolar and MOS technologies in the same multiplexer gives built-in protection. This circuit is typical for each channel in multiplexers HI-506A, HI-507A, HI-508A, and HI-509A.

The base-emitter junction conducts to hold the source-body diode off with a saturation voltage $V_{CE(SAT)}$ of about 0.2V. Thus clamped, the switch is protected from the effects of overvoltage.

Clamp Q_6 always turns on before the forward-voltage drop of the source-body diode is exceeded because diode D_6 requires an additional forward-voltage drop for conduction through the parasitic junction. Moreover, resistor R_1 limits the current flowing through Q_6 when high overvoltages exist. Although R_1 adds to the total on-resistance of the channel, its associated error is insignificant, since most systems provide high-impedance buffering anyway. For negative overvoltages, N_1 is similarly protected. What's more, the protection circuit, rated at a nominal overvoltage of ±33V, reveals a cross-talk current of only about 5na (Fig. 10).

When the switch is normally turned on, the substrates of N_1 and P_1 are connected together through N_2, which, as described before, results in a constant on resistance.

This condition represents an absolute error from channel interaction of only 6 microvolts (R_{ON} x 5_{NA})—certainly negligible in most systems. In contrast, floating-body types have guarantees only that they won't be burned up by ±25V overvoltage. Their manufacturers do not make any claim against channel interaction. In fact, channel interaction occurs readily in these devices when the n- and p-channel thresholds are exceeded by an overvolt-

age. For example, the n-channel device, although floating, would be inadvertently turned on if the analog input exceeded the negative supply by its gate-to-source threshold, which is typically 1.5V.

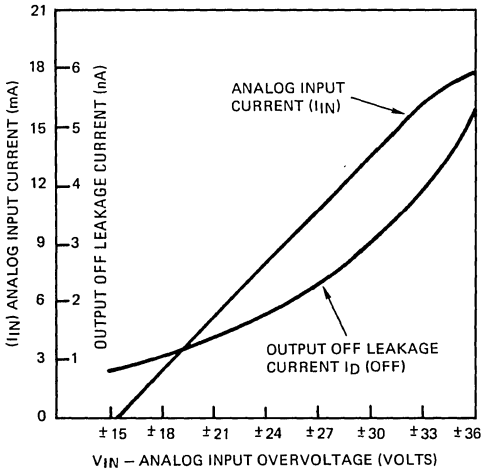

Figure 10. Blocking Cross Talk

DI switches have minimal cross-talk problems. An overvoltage of 33V produces a cross-talk current of only 5nA—an absolute error from channel interaction of only 6 μV.

ADDING BENEFITS

RESULTS OF DIGITAL-INPUT PROTECTION TESTS (20 DIELECTRICALLY ISOLATED UNITS)	
STRESS STEP/VOLTS	FAILURES
500	0
1,000	0
1,500	0
2,000	1
2,500	0
3,000	3
3,500	0
4,000	3

Additional DI benefits are passed on to the user in the design of the digital input-protection circuit shown in Fig. 11. The fabrication of all components as isolated silicon islands eliminates any possibility of latch-up. The diodes switch fast and quickly discharge any static charge that may appear at the digital MOS input gates. The table gives the results of a step-stress analysis performed on 20 units. A total of 80% survived the 3.5 kilovolt level, and only one failed below 2kV.

The DI technology enables a wide variety of active elements to be integrated on the same chip to provide maximum versatility. For example, in the transistor-transistor-logic/C-MOS reference circuit shown in

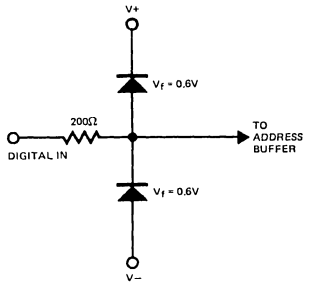

Figure 11. Digital Protection

DI devices also protect digital inputs. For example, the diodes in this circuit quickly discharge any static charge that may appear on an MOS input gate.

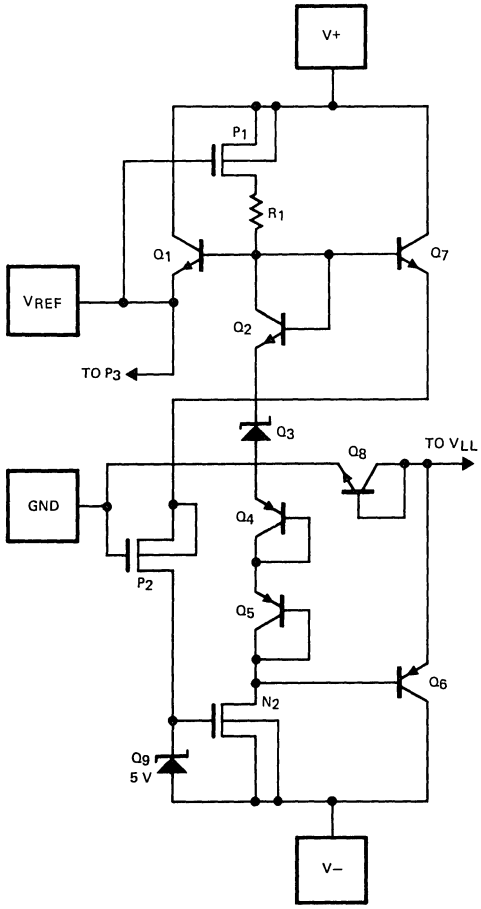

Figure 12. Packing It In

DI technology increases chip density of analog switch, allowing more circuit capability per package. For example, DI designs make possible this internal logic reference circuit in HI-200 and HI-201 switches.

Fig. 12, the bipolar technology enables realization of a simple zener reference circuit, consisting of resistor R_2 and transistors Q_1, Q_2, and Q_3.

Reprinted from **Electronics**, December 25, 1975.

The circuit develops a stable 5V reference for interfacing with TTL and eliminates the need for an additional 5V logic supply. Current for the zener (Q_3) is supplied through the normally on MOSFET, P_1, which can be easily turned off if not needed to minimize power consumption when interfacing with C-MOS-logic circuits. P_1 turns off when V+ or supply voltage V_{DD} is applied to the reference terminal V_{REF} to convert the IC's power-consumption from bipolar to C-MOS level. If power is not critical, V_{REF} can be left open to speed switching.

In high-speed data-acquisition systems, the designer is concerned with both quiescent power and dynamic power consumption. If JI devices are used, the capacitance or leakage currents are so high they contribute a major portion of total power consumption. That situation is caused by the large-geometry parasitic junctions formed by the n- junction.

In contrast, the smaller substrate area of the DI device provides much less power drain. Dynamic-power consumption as a function of frequency for several 16-channel analog multiplexers with ±15V supplies is shown in Fig. 13. The DI device consumes only 100mW at 1 MHz to yield the best speed-power product.

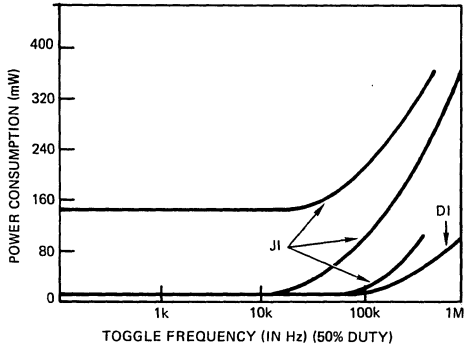

Figure 13. DI Performs
DI devices not only perform well, but do it with less power. Dynamic-power-consumption data for commercial multiplexers shows DI device consuming only 100mW at 1MHz.

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APPLICATION NOTE 522

DIGITAL TO ANALOG CONVERTER TERMINOLOGY

BY DICK TI TUNG

INTRODUCTION

In recent years the development and rapid reduction in cost of digital integrated circuits have resulted in an explosion in the applications of digital processing systems in the area of data acquisition and automatic process control. The need for a building block, such as the digital-to-analog converter (DAC), which interfaces the digital system with the analog world, is evident.

The purpose of digital-to-analog conversion is to produce a unique but consistent analog quantity, voltage or current, for a given digital input code. The most commonly used input digital code to a DAC is the natural binary number. A natural binary number is represented as

$$N = A_n2^n + A_{n-1}2^{n-1} + \ldots + A_12^1 + A_02^0 + A_{-1}2^{-1} + \ldots + A_{-n}2^{-n}$$

where the coefficients A_i (for $n \geq i \geq -n$) assume the values of "0" or "1" and is called a "bit". The left half portion of the binary number N

$$A_n2^n + A_{n-1}2^{n-1} + \ldots + A_12^1 + A_02^0$$

constitutes the integer part of the number N, whereas the right portion

$$A_{-1}2^{-1} + A_{-2}2^{-2} + \ldots + A_{-n}2^{-n}$$

constitutes the fractional part of the number N. The bit that carries the greatest weight (left most bit) is called the most significant bit, or MSB. Similarly, the bit with the smallest weight (right most bit) is called the least significant bit, or LSB.

The analog output of a n-bit binary DAC is related to its binary number in the following manner:

$$E_o = FS(A_{-1}2^{-1} + A_{-2}2^{-2} + \ldots + A_{-n}2^{-n})$$

where the term FS is defined as the nominal Full-Scale output of the DAC and it is known as the unreachable Full-Scale. It is easy to see that the actual Full-Scale output of the DAC, E_{FS}, with all the input bits "1" is

$$E_{FS} = FS(2^{-1} + 2^{-2} + \ldots + 2^{-n}) = FS(1-2^{-n}).$$

The term $FS(1/2^n)$ is the smallest output level that the DAC can resolve and it is known as the 1 LSB output level change. It is universal practice that the input code of a DAC is written in the form of binary integer with the fractional nature of the corresponding number understood.

As an example, the transfer function of an ideal 3-bit binary DAC is plotted as shown in Figure 1. Since a 3-bit DAC has only 8 discrete input codes which correspond to 8 different output levels (ranging from zero to 7/8 FS), no other output levels can exist and it is plotted as a bar graph. The line that connects the Zero and FS is called the Gain Curve.

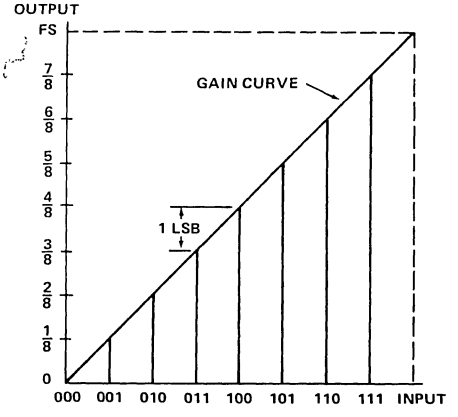

Figure 1 – Ideal Transfer Function Straight Binary (Unipolar)

There are two other input codings associated with binary DACs known as Bipolar codes, which are offset binary and two's complement binary codes. The offset binary code is obtained by offsetting the binary code such that the half-scale code, 10 . . . 0, becomes zero. And the two's complement code is achieved by inverting the MSB of the offset binary

8

code such that it is mathematically consistent with computer arithmetic. The transfer functions for the 3-bit DAC with offset binary input code and two's complement input code are plotted as shown in Figure 2 and Figure 3, respectively. (The +FS and -FS limits are used for easy interpretation of Bipolar operations. They are not confined by the previous definition of FS.)

In practical DACs, the zero output level may not be exactly zero (offset error), the range from zero to FS may not be exactly as specified (gain error), the differences in output levels may not be changing uniformly (nonlinearity), and so on. In selecting a DAC for a given application, some characteristics may have to be weighted more than the others. An understanding of some of the terms and characteristics involved in D/A conversion is helpful in choosing the correct part.

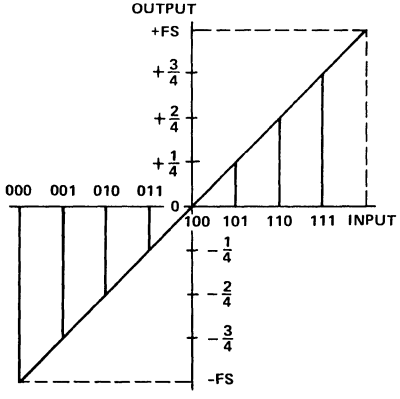

Figure 2 – Ideal Transfer Function Offset Binary (Bipolar)

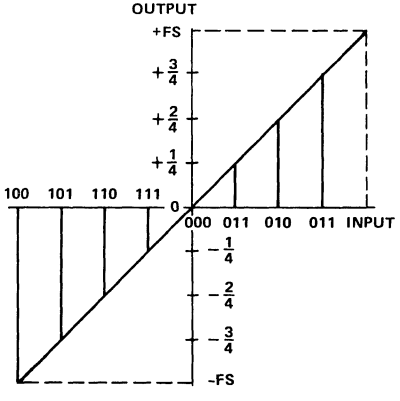

Figure 3 – Ideal Transfer Function Two's Complement (Bipolar)

TERMINOLOGY

Least Significant Bit (LSB) – The digital input bit carrying the lowest numerical weight ($1/2^n$); or the analog output level shift associated with this bit ($FSR/2^n$) which is the smallest possible analog output step.

Most Significant Bit (MSB) – The digital input bit carrying the highest numerical weight (1/2); or the analog output level shift associated with this bit. In a binary DAC the MSB creates a 1/2 FSR output level shift.

Resolution – An indication of the number of possible analog output levels a DAC will produce. Usually, it is expressed as the number of input bits. For example, a 12-bit binary DAC will have $2^{12} = 4096$ possible output levels (including zero) and it has a resolution of 12 bits.

Absolute Accuracy – A measure of the deviation of the analog output level from the ideal value under any input combination. Accuracy can be expressed as a percentage of full scale range, a number of bits (n bits accuracy means a magnitude of $1/2^n$ FSR possible error may exist), or a fraction of the LSB (if a DAC with n-bit resolution has 1/2 LSB accuracy the magnitude of the possible error is $1/2(1/2^n FSR)$). Accuracy may be of the same, higher, or lower order of magnitude as the resolution. Possible error in individual bit weight may be cumulative with combination of bits and may change due to temperature variations. Usually, the accuracy of a DAC is expressed in terms of nonlinearity, differential nonlinearity, and zero and gain drift due to temperature variations.

Nonlinearity (linearity error) – A measure of the deviation of the analog output level from an ideal straight line transfer curve drawn between zero and full scale (commonly referred as endpoint linearity).

Differential Nonlinearity – A measure of the deviation between the actual output level change from the ideal (1 LSB) output level change for a one bit change in input code. A differential nonlinearity of ± 1 LSB or less guarantees monotonicity; that is the output always increases for an increasing input.

Gain Drift – A measure of the change in full scale analog output, with all bits 1's, over the specified temperature range expressed in parts per million of full scale range per °C (PPM of FSR/°C). It is measured with respect to +25°C at high (T_H) and low (T_L) temperature, and it is specified the larger of the two representing worst case drift.

Offset Drift (Unipolar or Bipolar) – A measure of the change in analog output, with all bits 0's, over the specified temperature range expressed in parts per million of full scale range per °C (PPM of FSR/°C). It is measured with respect to +25°C at high (T_H) and low (T_L) temperature, and it is specified the larger of the two representing worst case drift.

Settling Time – The total time measured from a digital input change to the time the analog output reaches its new value within a specified error band. Usually, the settling time is specified for a DAC to settle for a Full-Scale code change (00 . . . 0 to 11 . . . 1 or 11 . . . 1 to 00 . . .0) to within $^{+}1/2$ LSB of its final value.

Compliance – Compliance voltage is the maximum output voltage range that can be tolerated and still maintain the specified accuracy.

The effects of gain error, offset error, nonlinearity, and differential nonlinearity on the transfer functions are plotted, respectively, as shown in Figure 4, 5, 6, & 7. A conversion chart which shows the number of bits and its resolution is given in Table 1.

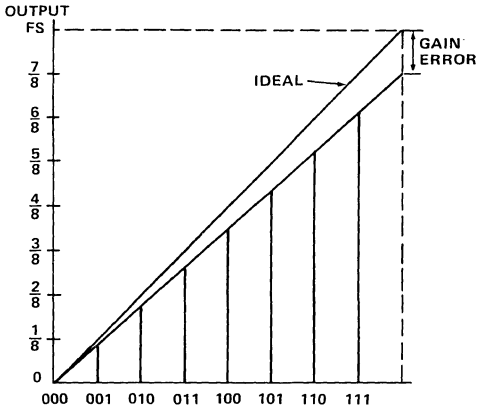

Figure 4 – Gain Error

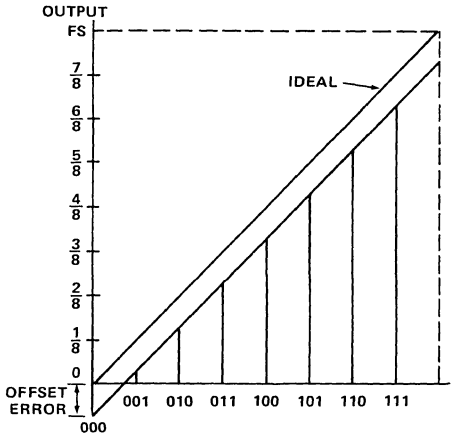

Figure 5 – Offset Error

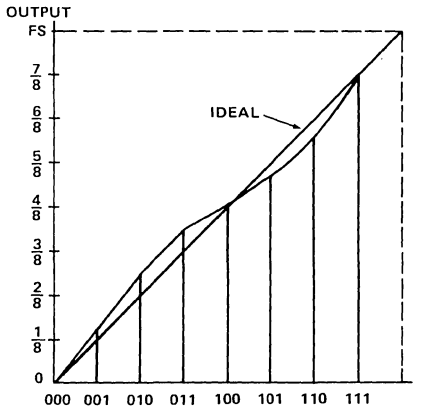

Figure 6 – Linearity Error

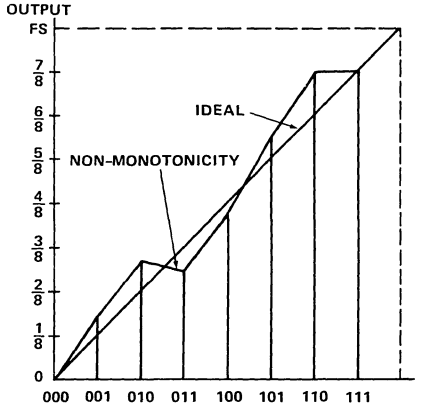

Figure 7 – Differential Linearity Error (Non-Monotonicity)

Table 1 – Conversion Chart

# OF BITS	LSB	RESOLUTION		TEMPCO PPM/°C – 1 LSB DRIFT OVER	
		%	PPM	0°C ≤ TA ≤ 75°C	-55°C ≤ TA ≤ 125°C
6	$FS/64$	1.5620	15,625	208.3	86.8
7	$FS/128$	0.7812	7.812	104.2	43.4
8	$FS/256$	0.3906	3,906	52.1	21.7
9	$FS/512$	0.1953	1,953	26 0	10.9
10	$FS/1024$	0.0977	977	13.0	5.4
11	$FS/2048$	0.0488	488	6.5	2.7
12	$FS/4096$	0.0244	244	3.3	1.4
13	$FS/8192$	0.0122	122	1.6	0 68
14	$FS/16384$	0.00610	61	0.8	0.34
15	$FS/32768$	0.00305	31	0.4	0.17
16	$FS/65536$	0.00153	15	0 2	0.08

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APPLICATION NOTE 524

DIGITAL TO ANALOG CONVERTER HIGH SPEED ADC APPLICATIONS

BY DICK TI TUNG

ANALOG-TO-DIGITAL CONVERTER (ADC)

The uses of high speed DACs in CRT display, industrial process control, signal regeneration, etc., are well established. Perhaps one of the most important applications is to use the DAC in high speed ADC design. There are two types of ADC design where high speed and high resolution DACs are essential.

TRACKING ADC OR SERVO TYPE ADC

The tracking ADC is very efficient in monitoring one analog signal continuously, converting it into a sequence of digital codes representing the analog signal in real time.

Functionally, the analog input is compared with the output of a DAC, with the digital input of the DAC being driven by a counter. After the ADC is turned on, the counter increments until the DAC output crosses the analog input value. The counter will then, running up or down, drive the DAC 1 LSB at a time to track the input signal. The counter state represents the digital equivalent of the input signal.

In Figure 1, the analog input is fed into the span resistor of a DAC. The analog input voltage range is selectable in the same way as the output voltage range of the DAC. The net current flow through the ladder termination resistance, i.e. 2kΩ for HI-562A, produces an error voltage at the DAC output. This error voltage is compared with 1/2 LSB by a comparator. When the error voltage is within ± 1/2 LSB range, the Q output of the comparators are both low, which stops the counter and gives a data ready signal to indicate that the digital output is correct. If the error exceeds the ±1/2 LSB range, the counter is enabled and driven in an up or down direction depending on the polarity of the error voltage.

Since the digital output changes state only when there is a significant change in the analog input, the data ready signal is then very useful in adaptive systems or computer systems for efficient data transfer. When monitoring a slowly varying input, it is necessary to read the digital output only after a change has taken place. The data ready signal could be used to trigger a flip-flop to indicate the condition and reset it after read-out.

The main disadvantage of the tracking ADC is that the time required to initially acquire a signal, for a 12 bit ADC, could be up to 4096 clock periods. The input signal usually must be filtered so that its rate of change does not exceed the tracking range of the ADC (1 LSB per clock period).

SUCCESSIVE-APPROXIMATION ADC

Perhaps the most widely used technique for a high speed analog-to-digital converter design is the successive approximation method. Ideal for interfacing with computers, this type is capable of both high speed and high resolution, and the conversion time is fixed and independent of the magnitude of the input voltage.

Figure 2 shows a block diagram of a successive-approximation ADC. When a negative going start conversion pulse is applied to the ADC, the internal registers of the successive approximation register (SAR) are set to low except for the MSB, which is set to high. This turns on the MSB of the DAC. The FS output current of the DAC is compared with the current fed through the span resistor by the analog input. The net current flow through the ladder termination resistance produces an error voltage at the DAC output. This error voltage is then compared with a fixed reference by a comparator to determine whether the analog input is greater or less than the present state of the DAC. The result of the comparison is clocked into the SAR at the rising edge of the clock. The MSB of the SAR will be set to high if the analog input is greater; otherwise, it will be set to low. At the same time, the second bit of the SAR is set to high with the remaining bits at their previous states. During the second clock period, the sum of the result of the first choice and the weight of the second bit is compared with the analog input. The second bit is set to high or low in the same manner as the MSB, and so on, until the LSB is updated.

During this conversion time, the output of a status flip-flop is set to high, indicating that a conversion is taking place. It will return to low at the end of conversion to signify that the output state of the SAR represents the digital equivalent of the input analog voltage.

It is easy to see that in any successive-approximation ADC application, the analog input should remain reasonably constant during the conversion to avoid erroneous results. This is usually accomplished by using a sample-and-hold circuit in the analog line.

DATA ACQUISITION SYSTEM

The functional diagram of a 16-channel data acquisition system is shown in Figure 3. Functionally, the outputs of the binary counter are fed to the 16-channel analog multiplexer to serve as the channel select signals, and it is also fed to the 4 line to 16 line digital decoder as address inputs. At the rising edge of the clock pulse, an analog input channel is selected, and the sample and hold circuit (S/H) is set to sample. The duration of the "1" state of the clock pulse should be adjusted such that the output of the S/H would settle to its required accuracy. At the falling edge of the clock pulse, the S/H holds the signal level acquired during the clock "1" state, and with one gate delay time, the ADC commences its conversion. Once the conversion is completed, the $\overline{CC}$ signal from the ADC will enable the decoder to send out a decoded signal to strobe the ADC output into the proper storage register. The duration of the "0" state of the clock pulse should be adjusted to allow the proper data entry to the storage register. The next analog input channel will be acquired for the next clock period, and so on. If a 50kHz clock pulse is used, the data will be refreshed every 320μs.

This 16-channel data acquisition system is applicable to industrial process control, and multi-channel panel display. It can also interface with an intelligent terminal, such as a micro-computer system, to provide multi-channel data conversion function. The offset error and gain error of the data acquisition system over the operating temperature range can be easily compensated by proper programming.

By the same token, a 15-channel data acquisition system with offset correction could be easily incorporated as shown in Figure 4. Consider the case that one of the analog input channels is dedicated to sense the ground level, and its binary equivalent is stored in latch register B in its complementary form to establish a ground reference in real time. All the other analog input channels will then be converted and stored in register A, one at a time. The binary adder will perform the binary subtraction in less than 1μs for the given pair of A and B. This, in fact, eliminates the offset error of the ADC, offset error of the S/H circuit, and excess droop of the S/H due to temperature variation.

This circuit is easy to implement and is especially useful when an intelligent terminal is not available. To expand this concept one step further, the gain error of the system due to temperature variations could also be eliminated if a binary multiplier is used to correct the gain facter in real time.

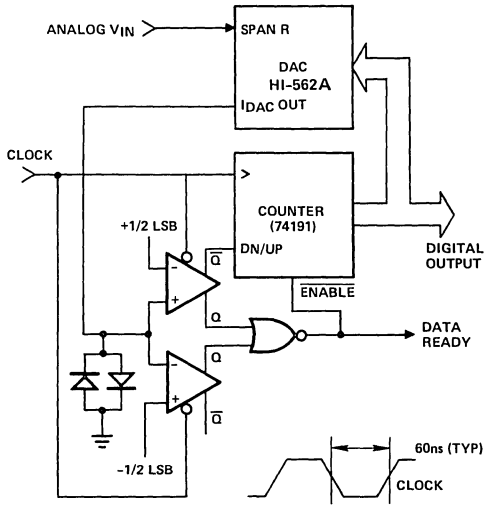


Figure 1. Tracking ADC

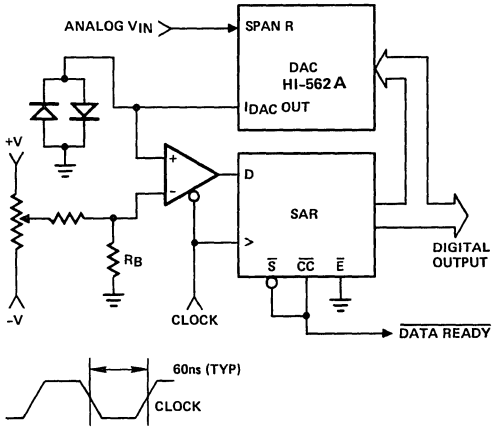


Figure 2. Successive-Approximation ADC

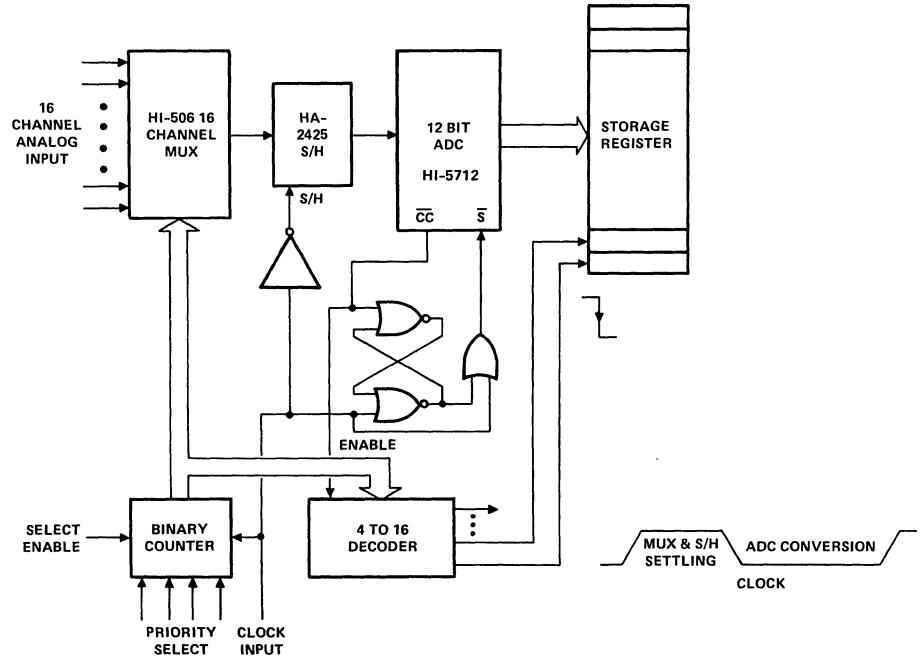


Figure 3. 16 Channel Data Acquisition System

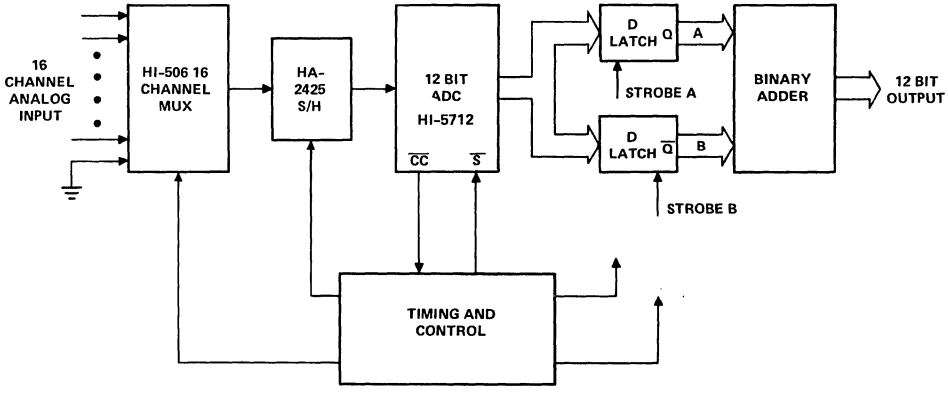


Figure 4. 15 Channel Data Acquisition System
with Offset Correction

HARRIS

APPLICATION NOTE
525

HA-5190/5195 FAST SETTLING OPERATIONAL AMPLIFIER

G. COTREAU, D. JONES,
R. WHITEHEAD

INTRODUCTION

The military temperature range HA-5190 and its commercial temperature equivalent, HA-5195, are monolithic operational amplifiers featuring ±200V/μs slew rate, 150mHz gain-bandwidth-product, and 70ns settling time. Similar performance has previously been available only in more costly modular and hybrid amplifiers, which require much higher bandwidth and slew rate to achieve the same settling time as HA-5190/5195. Since it exhibits a classical -6dB/octave rolloff over most of its frequency range, remarkably smooth output wave forms are generated by HA-5190 when reasonable care is employed.

Applications for this op amp include pulse, RF, and video amplifiers, wave form generators, high speed data acquisition and instrumentation circuits.

INSIDE THE HA-5190/5195

Figure 1 shows the schematic of the HA-5190/5195 design. The schematic can be simplified to show the AC signal path as shown in Figure 2.

The input stage consists of two symmetrical differential transistor pairs. The signal path for positive going signals is Q_1, Q_2, and Q_3, while negative going signals pass through Q_4, Q_5, and Q_6. The signal then goes through the output stage (represented by the voltage follower symbol) consisting of one PNP and two NPN emitter followers.

In Figure 2, the compensation network is C_1, C_2, C_3, and R_{29}. This network makes the amplifier system appear as second-order critically damped. The scheme produces the dominant pole plus two zeros. The zeros are positioned to cancel the effects of undesired poles developed by the F_t of the transistors.

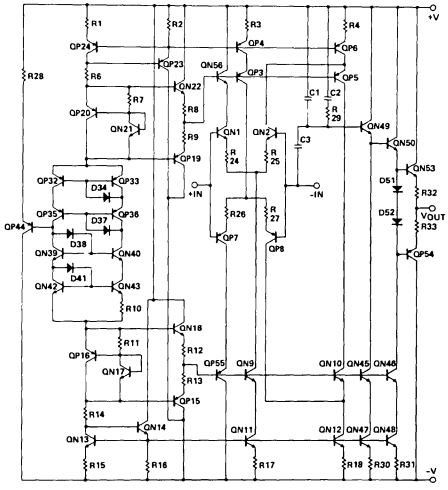


Figure 1. HA-5190/5195 Schematic.

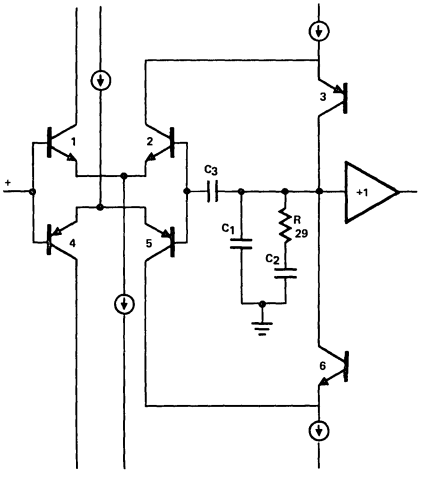


Figure 2. Simplified HA-5190 Schematic.

8

CONSIDERATIONS FOR PROTOTYPING

When using the HA-5190, high frequency layout techniques are recommended for bread-boarding. The device should be mounted through a ground plane. If an IC socket is to be used, Teflon types are recommended. Feedback components should be mounted between Teflon insulated standoffs located as close as possible to the device pins.

The input impedance characteristic of the HA-5190 is such that the closed loop performance (DC and AC) will depend on both the feedback component ratio and the actual impedance presented to each amplifier input. For best high frequency performance, resistor values for feedback networks should be limited to a maximum of 5K ohms (preferably less than 1K ohm). Film type resistors are recommended. Power supply decoupling with ceramic capacitors from the device supply pins to ground is essential.

It is recommended that optimum circuit values for a particular application be developed through experimentation using amplifiers from several production runs. The PC artwork in the vicinity of the HA-5190 should be prototyped early to determine any sensitivites to layout.

OPERATION AT ELEVATED TEMPERATURES

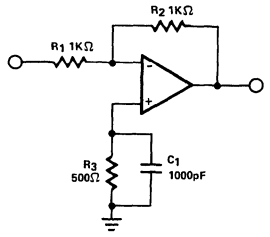
HA-5190/5195 may be used without a heat sink up to +75°C ambient. Above this temperature the power derating is 8.7mW/°C and a heat sink should be used. THERMALLOY model 6007 heat sink is recommended. For temperatures up to +125°C, the thermal resistance of the heat sink should be 30.6°C/W maximum.

FREQUENCY COMPENSATION

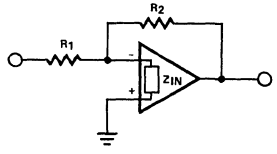
HA-5190/5195 is stable in standard DC amplifier configurations with closed loop gains exceeding +5 or -4. At these or higher gains, optimum AC performance can be achieved by keeping network resistor values as low as is practical.

Quite simple circuitry, as illustrated in Figure 3, gives excellent performance for lower closed loop gains. The compensation schemes use the amplifier's differential input impedance to reduce both the input and feedback signals thereby raising the effective noise gain approximately 14dB to a stable point on the frequency response curve.

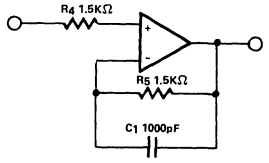
Inverting and non-inverting unity gain connections for HA-5190 are shown in Figure 3 (a) and (c). R_3 and R_5 serve only to balance DC voltage offsets due to input bias current, and may be replaced with a short for AC applications. C_1 is not neccessary for stability, but helps reduce overshoot and smooth the frequency response. Settling time or frequency response can be optimized (about 30mHz small signal bandwidth is practical) by fine tuning component values.



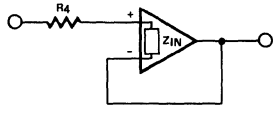
(a) Gain = -1



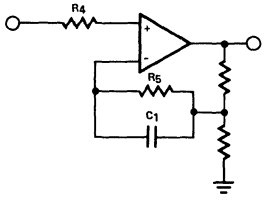
(b) Stabilization using Z_{IN}.



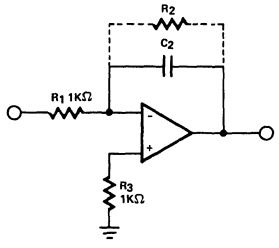
(c) Gain = +1



(d) Stabilization using Z_{IN}.



(e) Non-inverting gain stage.



(f) Integrator

Figure 3. Compensation recommended when $1 + \frac{R2}{R1} < 5$.

For closed loop gains between 1 and 5, reducing R_1 in Figure 3 (a) and (e) will raise the gain with minimum effect on bandwidth. However, in the inverting configuration, R_1 determines the input impedance, and it may be more practical to raise R_2 at the expense of bandwidth. In Figure 3 (e), R_4 and R_5 may be reduced as gain is increased and removed entirely at gains greater than +4.

For applications requiring 100% feedback at high frequencies, such as integrators and low pass filters, HA-5190/5195's compensation scheme should be thoroughly evaluated through experimentation. The circuit in Figure 3 (f) is quite stable, using the two 1K ohm resistors.

SUGGESTED METHODS FOR PERFORMANCE ENHANCEMENT

To avoid compromising AC performance, the HA-5190 design does not include provisions for internal offset adjustment.

The circuits in Figure 4 (a) and (b) show two possible schemes for offset voltage adjustment.

Figure 5 (a) and (b) uses the inherent qualities of the FET to reduce input bias currents by several orders of magnitude and raise input impedance to thousands of megohms. Both circuits are shown in the unity gain follower mode. Circuit gain can be implemented using normal feedback techniques. To optimize for speed, care should be taken in layout. Experimental results yielded slew rates of approximately 130V/μs.

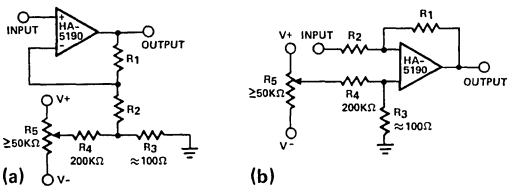
Figure 5 (c) illustrates a composite inverting amplifier which greatly reduces DC errors due to the HA-5190 input bias current and gain, while retaining superior settling time. The 0 dB frequency of the integrator section approximates the open loop low frequency pole (~2.5kHz) of the HA-5190. This circuit might also be connected as a current-to-voltage amplifier for use with a high accuracy, high speed DAC.

Figure 6 shows a composite amplifier scheme for boosting output current drive of the HA-5190/5195. The circuit gain (shown $A_V = 5$) can be adjusted using normal feedback systems. HA-5190 used in conjunction with HA-2630 can drive 50 ohm coaxial cable with 10 volt peak-to-peak signals at speeds up to 200V/μs.

APPLICATIONS

INTRODUCTION

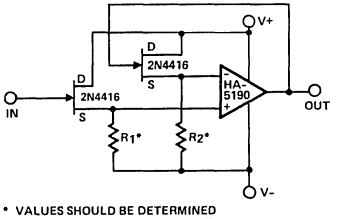
HA-5190/5195 represents an ideal building block for high speed, precision data acquisition systems and for video pulse amplification. Although this amplifier can be used in a wide variety of other applications, the ones to be discussed show where it can be used most advantageously.



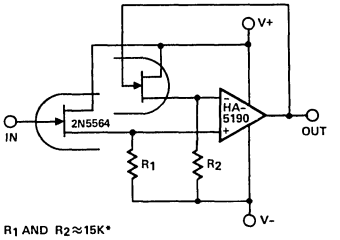
RANGE OF ADJUSTMENT FOR BOTH NON-INVERTING (LEFT) AND INVERTING AMPLIFIERS (RIGHT) DETERMINED BY PRODUCT OF V_{SUPPLY} AND R_3/R_4 RATIO.

$$A_V = 1 + \frac{R_1}{R_2 + R_3}$$

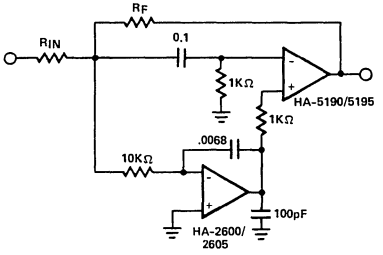
Figure 4. Offset Nulling.



(a) * VALUES SHOULD BE DETERMINED EXPERIMENTALLY FOR OPTIMIZED PERFORMANCE.



(b) R_1 AND $R_2 \approx 15K^*$
INPUT FETS ARE MATCHED PAIR 2N5564



(c)

Figure 5. Reducing Input Bias Currents.

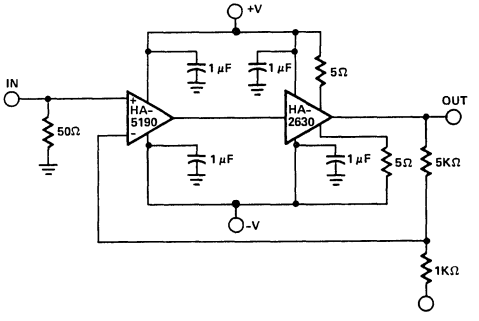


Figure 6. Boosting Output Current.

Application 1 Fast DAC Output Buffer

The circuit at right illustrates the HA-5190's usefulness as a high speed DAC buffer.

The amplifier operates as a current-to-voltage converter/output buffer to the HI-5610 which is a precision 10 bit DAC with output current settling time less than 100ns. The voltage divider on the non-inverting input serves to null any DC errors introduced into the system. The amplifier maximizes speed of the system since its dynamic performance exceeds that of the DAC.

Application 2 High Speed Sample/Hold

Sample/Hold circuits are used in many areas of data acquisition systems such as de-glitchers for D/A converters and input stages for successive approximation A/D converters.

The circuit at right uses the speed and drive capability of the HA-5190 coupled with two high speed DMOS FET switches.

The input amplifier is allowed to operate at a gain of -5 although the overall circuit gain is unity. Acquisition times of less than 100ns to 0.1% of a 1 volt input step are possible. Drift current can be appreciably reduced by using FET input buffers on the output stage of the Sample/Hold.

Application 3 Video Pulse Amplifier/75 ohm Coaxial Driver

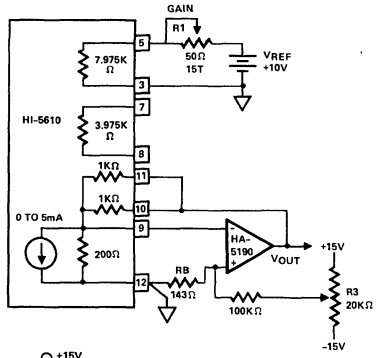
HA-5190/5195 is also well suited for video pulse applications. The circuit at right could be found in various types of video broadcasting equipment where 75 ohm systems are commonly employed.

HA-5190 can drive the 75 ohm coaxial cable with signals up to 2.5 volts peak-to-peak without the need for current boosting. In this circuit the overall gain of the circuit is approximately unity because of the impedance matching network.

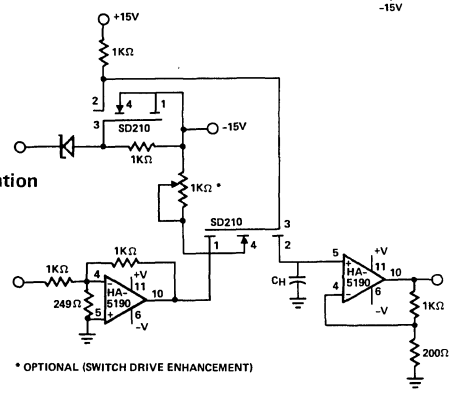
Application 4 Output Limiter

HA-5190 is rated for ± 5 volt output swing, and saturates at ± 7 volts. As with most op amps, recovery from output saturation is slow compared to the amplifier's normal response time; so some form of limiting, either of the input signal or in the feedback path, is desirable if saturation might occur. The circuit above illustrates a feedback limiter, where gain is reduced if the output exceeds ± (Vz + 2Vf). A 5 volt zener with a sharp knee characteristic is recommended.

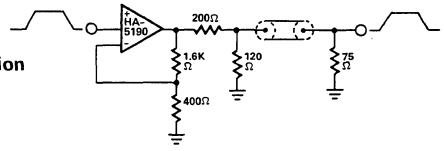
Application 1



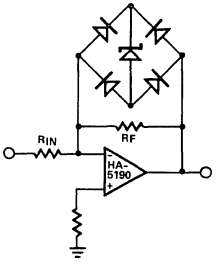
Application 2



Application 3



Application 4



8

HARRIS

APPLICATION NOTE 526

VIDEO APPLICATIONS HA-5190/5195

L. E. GARNER

INTRODUCTION

Offering superior performance in video and RF circuits, the HA-5190/5195 family can be used effectively in the design of television broadcast studio equipment, test instruments, and monitoring or surveillance TV systems. A very high 200V/μs slew rate, a full power bandwidth of 6.5MHz, and a fast settling time of only 70ns (typ) are but three of the unique characteristics which make these devices ideal for critical wideband video and RF applications. Other features include true differential operation, excellent stability with gains ≥ 5, and complete freedom from latch up, the latter a result of the exclusive HARRIS dielectric isolation process combined with optimized chip design and layout.

The op amp family can be used, typically, as studio tape head, test instrument, and video camera preamplifiers, as buffers, as broadcast relay link repeaters, as coaxial line drivers, and as cable or industrial system video repeater and bridging amplifiers. Extremely versatile, the devices can be operated effectively in AGC and dc gain controlled configurations as well as in fixed gain designs, and are fully capable of driving low impedance loads.

When used in standard video amplifier configurations, the HA-5190/5195 devices easily meet or exceed the performance tolerance specifications of applicable current FCC (NTSC) composite TV signal standards as well as the requirements of EIA Tentative Standard RS-170A.

VIDEO PERFORMANCE

The overall color video performance of the HA 5190/5195 family was confirmed by checking a number of standard devices. Tests were made to determine both video response and signal/noise ratio under typical operating conditions. The basic video amplifier circuit illustrated in Figure 1 was used for the tests, with the actual procedures abstracted from those described in EIA Standard RS-250-B. The general test setup is shown in Figure 2.

VIDEO RESPONSE TESTS

Referring to Figure 1, the test video amplifier comprised an HA5190/5195 op amp, BNC coaxial input jack J1, input level control R1 shunted by impedance matching resistor R2, input series stabilization resistor R3, gain control network R4-Rgain, series output limiting resistor Rs, and BNC coaxial output jack J2. Operational power was supplied by a well regulated and filtered dual line operated power supply.

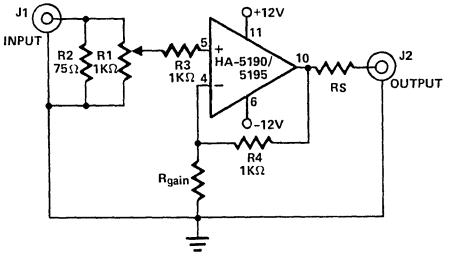


Figure 1–Test Video Amplifier

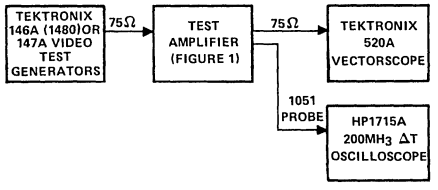


Figure 2–Video Response Test Setup

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Initially, standard NTSC and EIA ramp and timing test signals were applied using the Tektronix Models 146A (1480) and 147A video test generators. Amplifier performance was observed and measured at various levels with a Tektronix 520A Vectorscope and HP Model 1715A 200 MHz delta time Oscilloscope. Three of the RS-250-B specified test waveforms used are illustrated in Figure 3, including the (a) ramp linearity, (b) 12.5T and 2T sine-squared pulse and bar, and (c) multiburst signals. With the test signal level maintained at 1.0V p-p, level control R1 was adjusted as needed to establish a 1.0V p-p output signal (at J2) for each gain value. The Vectorscope was used to measure color differential phase and gain, with the Oscilloscope used to check for distortion of the 2T, 12.5T, multiburst and color bar signals. The average test results are summarized in Table A. All measured values were well within applicable specifications.

Table A - Summary of Test Results

NOMINAL GAIN	R_{gain}	R_s	DIFF ϕ	DIFF GAIN	2T	12.5T	MULTI	COLOR BARS
1	∞	0	-0.2°	-0.5%	UNM*	UNM*	FLAT	UNM*
2	1k	75Ω	-0.15°	≈0	UNM*	UNM*	FLAT	UNM*
5	251Ω	200Ω	-0.2°	≈0	UNM*	UNM*	FLAT	UNM*
10	110Ω	200Ω	-0.4°	-0.5%	UNM*	UNM*	FLAT	UNM*

*UNM : UNMEASURABLE DISTORTION

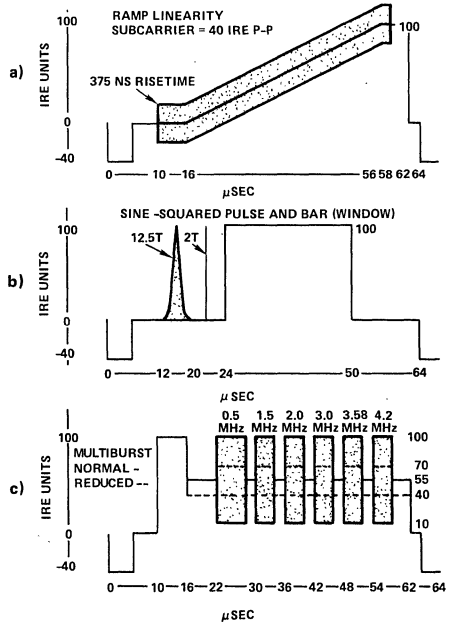


Figure 3—Video Test Signal Waveforms

S/N RATIO

Signal/noise (S/N) ratio measurements were made using the same basic amplifier configuration, but with Rgain fixed at 251Ω, ±1%, and Rs at 200Ω ±5%. The dc power supply terminals were bypassed with a 100 μF tantalum capacitor. A Tektronix 147A NTSC Test Signal Generator was used as a signal source, with output measurements made using a Rhode & Schwartz Video Noise Meter, as diagrammed in Figure 4. The Tektronix 147A was set to deliver a flat field signal at 50 IRE units, with the R&S Video Noise Meter adjusted as follows: (a) 10kHz High pass, (b) Video Bandpass, (c) Subcarrier Trap OFF, (d) Internal Sync, (e) Tilt & Sag Comp OFF.

Under the specified conditions and with level control R1 adjusted to deliver a 1.0V p-p signal at J2, the measured p-p signal/RMS noise ratio averaged 68dB, or well over the minimum value required by applicable standards.

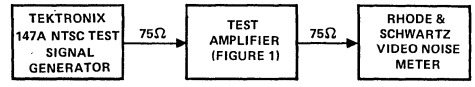


Figure 4—S/N Ratio Test Setup

GENERAL CONSIDERATIONS

Since the HA-5190/5195 devices do not require special treatment, optimum video performance can be achieved by observing standard high frequency design and wiring practices. However, the following suggestions, abstracted in part from HARRIS Application Note 525, should prove helpful when developing practical designs.

POWER SUPPLY REQUIREMENTS

A well-regulated, well-filtered dual dc power source is required for best operation, for the op amps draw moderate currents during normal operation. Although not essential in all applications, it is recommended that the power supply lines be decoupled using 0.01 μF ceramic capacitors to circuit ground, with the capacitors located as near to the amplifier terminals as possible to minimize lead inductances. For optimum performance and operation at specified parameters, the dc power supply should furnish not less than ±10V dc, with higher source voltages (±15V, typically) preferred.

TEMPERATURE CONSIDERATIONS

The HA-5190/5195 devices can be used without heat sinks at ambient temperatures up to 75°C. Under these conditions, the internally generated heat stabilizes device operation and ensures relative immunity

to external temperature variations. At ambients above 75°C, however, the devices should be derated at 8.7mW/°C, with a suitable heat sink, such as a THERMALLOY Model 6007, used to provide adequate heat dissipation. At temperatures up to +125°C, the thermal resistance of the heat sink should be no greater than 30.6°C/W.

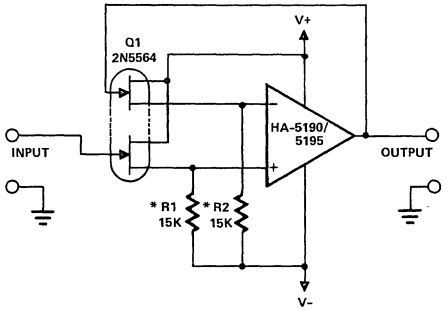
Under some conditions, the internally generated heat can affect other components. Therefore, avoid mounting temperature sensitive devices or components near or directly adjacent to the op amps.

DESIGN HINTS

Except for their exceptional performance specifications, the HA-5190/5195 devices are essentially standard op amps and may be treated as such by the video equipment or system designer. Thus, conventional design techniques may be used when developing specific circuit configurations, as long as maximum ratings are observed and adequate compensation is made for device operational characteristics. For example, the closed loop performance (dc and ac) at gains ≥ 5 depends on both the feedback component ratio and the actual impedance at each amplifier input. Since the devices offer a comparatively low input impedance, feedback network resistor values should be 5k or less (preferably, less than 1k) for optimum high frequency performance.

If the intended video application requires a high input impedance, a FET preamp stage may be added ahead of the HA-5190/5195 op amp, as shown in Figure 5. Full details and an additional FET input circuit are provided in HARRIS Semiconductor Application Note 525.

Where used, a FET preamp not only raises the effective input impedance from (approximately) 10k to thousands of megohms, but also reduces the input bias current requirement by several orders of magnitude. There is, of course, a trade-off in frequency response, with a FET input stage reducing the effective overall slew rate from 200V/μs to 130V/μs (typically). However, the full power bandwidth with a FET input is more than adequate for all low to mid level video applications.



*Approximate Values

Figure 5– FET Input Circuit

Some video applications may require output currents which exceed the maximum capabilities of the HA-5190/5195 devices. In these cases, the HA-5190/5195 op amps can be teamed with high performance current boosters such as, for example, the HA-2630/2635 devices. A typical cascaded op amp/booster circuit is illustrated in Figure 6. Since the current booster, a unity gain device, has a typical slew rate and bandwidth (Slew rate 500V/μs, BW 8.0MHz) far greater than that of the op amp, the overall frequency performance of the composite amplifier is essentially that of the op amp alone.

To compensate for manufacturing tolerances and ensure optimum performance, the fixed component values used in specific designs should be finalized empirically, using active devices from several production runs.

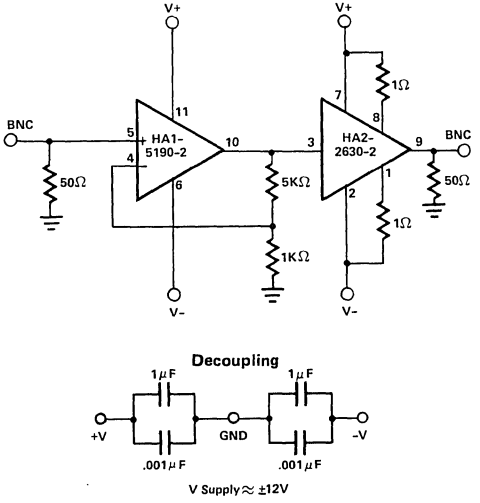


Figure 6–Boosting Output Current

PROTOTYPING TIPS

In accordance with standard engineering practice, new circuit designs should be breadboarded to verify overall operation. Afterwards, a number of preproduction prototypes identical to the planned production design should be assembled and tested using active devices from several production runs. These prototype tests permit optimization of component values and determination of circuit sensitivities to layout and component positioning. Preliminary environmental tests, if required, also may be made using the prototypes.

If IC sockets are used, Teflon types are preferred to minimize distributed capacitances. For the same reason, feedback components should be mounted between Teflon insulated standoffs located as close as practicable to the device pins or socket terminals. For maximum stability, film type resistors are recommended for the feedback networks.

Signal carrying leads should be kept short and direct, of course, to minimize both lead inductances and distributed capacitances. The devices should be mounted through a ground plane cr, if this is impracticable, single point grounding should be used to avoid ground loops.

TYPICAL APPLICATIONS

The test circuit given in Figure 1 may be used as a general purpose video amplifier, although minor changes in component values may be needed to optimize operation for specific requirements. Additional practical circuits are illustrated in Figures 7 and 8.

RF AGC AMPLIFIER

Designed and checked as a buffer for the head preamp of a studio video tape recorder, the circuit shown in Figure 7 functions as a wide band adjustable AGC amplifier. With an effective bandwidth of approximately 10 MHz, it is capable of handling RF input signal frequencies from 3.2 to 10MHz at levels ranging from 40mV up to 3V p-p.

AGC action is achieved by using opto coupler/isolator OCI as part of the gain control feedback loop. In operation, the positive peaks of the amplified output signal drive the OCI LED into a conducting state. Since the resistance of the OCI photosensitive element is inversely proportional to light intensity, the higher the signal level, the lower the feedback resistance to the op amp inverting input and hence the greater the negative feedback, thereby lowering stage gain. Any changes in gain occur smoothly because the inherent memory characteristic of the photoresistor acts to integrate the peak signal inputs. In practice, the stage gain is adjusted automatically to a point where the output signal positive peaks are approximately one diode drop above ground.

GAIN SET control R5 applies a fixed dc bias to the op amp non-inverting input, thus establishing the steady-state zero input signal current through the OCI LED and determining the signal level at which AGC action begins. In experimental tests under large signal conditions (i.e., E_{IN} = 3V p-p), a GAIN SET value of -0.26V provided unity gain, while a value of -1.55V yielded on A_V of 2.7 , with a flat response to 5.0MHz at both levels. Under small signal conditions (i.e., E_{IN} = 40mV), gains from 8 to 50 could be achieved as the GAIN SET value was adjusted from 0.65V to -80mV. At A_V = 8, the frequency response was flat to 5MHz, while at A_V = 80, the response was limited to that of the HA-5190/5195.

The effective AGC range depends on a number of factors, including individual device characteristics, the nature of the RF drive signal, the initial setting for R5, et al. Theoretically, however, the AGC range can be as high as 4000:1 for a perfect op amp, for the OCI photoresistor can vary in value from 1 Megohm with the LED dark to 250Ω with the LED full on.

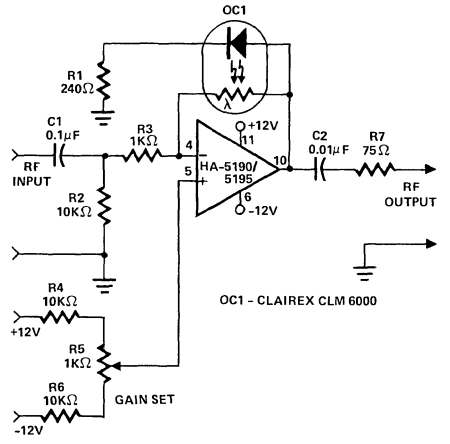


Figure 7–RF AGC Amplifier

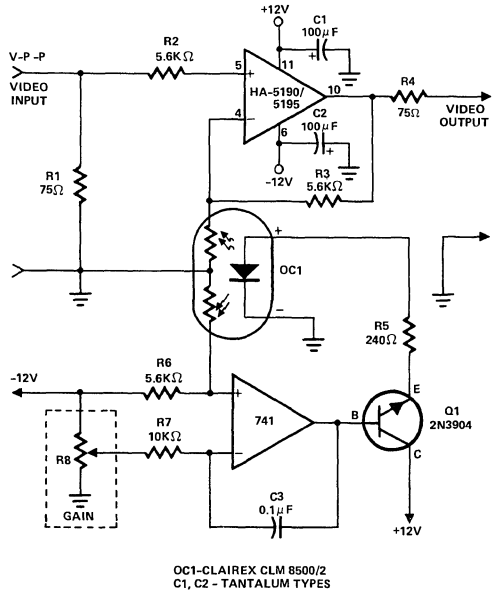


Figure 8–DC Gain Controlled Video Amplifier (Analog Multiplier)

DC GAIN CONTROLLED VIDEO AMPLIFIER

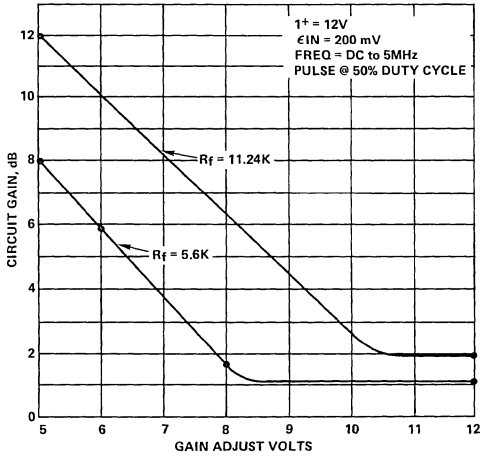
Suitable for use in virtually any application requiring a variable gain wideband or video amplifier, the circuit illustrated in Figure 8 employs a cascaded op amp integrator and transistor buffer (Q1) to drive the amplifier gain control element. Except for a simple modification, the HA-5190/5195 stage is connected as a conventional non-inverting operational amplifier, and includes input and output impedance matching resistors R1 and R4, respectively, series stabilization resistor R2, and power supply bypass capacitors C1 and C2. The circuit differs from standard designs in that the gain control network includes a photoresistor, part of OCI.

Referring to the schematic diagram, opto coupler/isolator OCI contains two matched photoresistors, both activated by a common LED. The effective resistances offered by these devices is inversely proportional to the light emitted by the LED. The greater the current through the LED, then, the more intense its light emission, and the lower the effective values of the photoresistors. One photoresistor is part (with R3) of the HA-5190/5195 gain network, while the other forms a voltage-divider with R6 to control the bias applied to the integrator non-inverting terminal.

In operation, the dc voltage supplied by GAIN control R8 is applied to the integrator inverting input terminal through input resistor R7. Depending on the relative magnitude of the control voltage, the integrator output will either charge or discharge C3. This change in output, amplified by Q1, controls the current supplied to the OCI LED through series limiting resistor R5. This action continues until the voltage applied to the integrator non-inverting input by the R6-photoresistor voltage divider matches the control voltage applied by R8 to the inverting input. At the same time, of course, the ratio of the R3-photoresistor gain network is changing, adjusting the op amp stage gain. As the control (R8) voltage is readjusted, the OCI photo-resistances track these changes, automatically readjusting the op amp gain in accordances with the new control voltage setting.

In experimental tests with typical devices, the amplifier gain could be varied from 12dB to 2dB as the dc control voltage was changed from 5.0 to 10.5Volts. Typical plots of stage gain (A_V) versus control voltage (V) are shown in Figure 9.

Since all temperature sensitive components are inside the integrator feedback loop, the circuit is quite stable with respect to changes in the ambient temperature.



ACKNOWLEDGEMENTS

A. J. Carl Cooper of HARRIS CVS (Consolidated Video Systems), 1255 E. Arques Ave., Sunnyvale, CA. 94086, developed the basic circuits described herein and, in addition, devised and executed the initial evaluation and performance tests.

B. Richard Whitehead and Robert Junkins of HARRIS SEMICONDUCTOR, P.O. Box 883, Melbourne, Fla. 32901, carried out additional confirmation tests of circuit performance and made other significant contributions to this publication.

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1. HA-5190/5195 Wideband, Fast Settling Operational Amplifiers (Harris data brochure)

2. Application Note 525 - HA-5190/5195 Fast Settling Operational Amplifier. May 1979.

3. EIA STANDARD RS-170A - Color Television Studio Picture Line Amplifier Output.

4. EIA STANDARD RS5-250-B - Electrical Performance Standards for Television Relay Facilities.

HARRIS

APPLICATION NOTE 527

APPLYING THE HI-5900 ANALOG DATA ACQUISITION SIGNAL PROCESSOR

BY JOHN E. SULLIVAN

JULY 1981

INTRODUCTION

The HI-5900 Analog Data Acquisition Signal Processor is a powerful building block for use in a Data Acquisition Subsystem (DAS), or in stand-alone operation. Incorporating a differential analog multiplexer, a programmable gain instrumentation amplifier and track and hold amplifier, the HI-5900 is an ideal signal conditioning element for a wide range of commercial, industrial and military applications.

FUNCTIONAL OPERATION OF THE HI-5900

As illustrated in Figure 1, the HI-5900 incorporates three primary components. An input multiplexer controls selection of the signal to be processed, the programmable gain instrumentation amplifier provides common mode signal rejection and gain while the track and hold amplifier stores the instantaneous signal level for final signal processing. Signal acquisition, including multiplexer, amplifier, and track and hold settling times, is less than 10 μs to 0.01% accuracy.

The multiplexer selects one of eight possible differential analog input signals to be processed, or it can be disabled to the high impedance state. All analog input lines have full overvoltage protection and can tolerate inputs up to 20 volts in excess of the power supply voltages for extended periods and transient spikes up to several hundred volts.

Expansion lines, MUX OUT A and MUX OUT B, can be used either to expand the number of input channels or as monitor outputs. The multiplexer exhibits a nominal 2 kilohm ON resistance; therefore, when using MUX OUT A or MUX OUT B as monitor points, a high impedance monitor (> 1 megohm) should be used to minimize loading affects.

Select lines A_0, A_1 and A_2 operate in binary mode (000 selects channel 1 and 111 selects Channel 8). The enable line, when LOW, DISABLES the multiplexer and forces its output to the high impedance state. Both the select and enable lines have an operating range of V- to +0.8 volts for a logic 0 input and 4 volts to V+ for a logic 1 input. When driving these inputs with TTL logic, a 1K ohm pullup resistor is recommended to ensure proper switching. All unused inputs (both signal and control) can be hardwired to either V- or ground for a logic 0 and +5 volts (V_{CC}) or V+ for a logic 1.

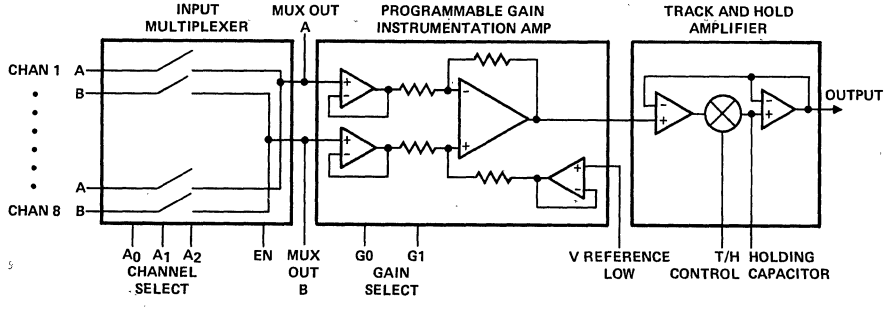


FIGURE 1 – FUNCTIONAL BLOCK DIAGRAM

PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

The programmable gain instrumentation amplifier (PGA) operates in the true differential mode with A input signals being inverted and B input signals being noninverted. Some applications will have true differential input signals with an infinite impedance to ground. These applications should incorporate a 5 megohm resistor to ground from both the MUX OUT A and MUX OUT B outputs to allow amplifier bias currents to flow to ground.

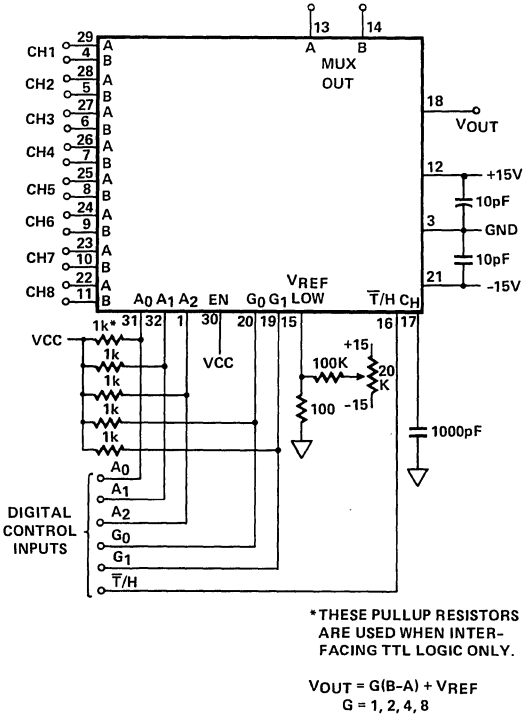
The PGA has digitally selectable gains of 1, 2, 4 and 8 in binary format (00, G = 1; 11, G = 8). The digital control levels are identical to those of the input multiplexer, and as such require 1k ohm pullup resistors when driven from TTL logic.

The V_{REF} LOW line can be tied to ground or used for offset nulling as illustrated in Figure 2. Other configurations such as level shifting or quasi-differential outputs can also be implemented as shown in Figure 5.

TRACK AND HOLD AMPLIFIER

The track and hold amplifier stores and holds the instantaneous signal level applied to its input when the T/H line goes to a logic 1. The T/H mode control is fully TTL compatible and requires no pullup resistor, with the track mode defined as -5 to +0.8V and the hold mode defined as +2 to +7 volts.

An external holding capacitor (typically 1000pF to minimize pedestal errors and droop rate) is used to store the signal level while in the hold mode. This capacitor should be selected for minimum dielectric absorption and leakage as found in Teflon or polystyrene types. As shown in Figure 3, the acquisition time vs. accuracy vs. droop rate is a function of the value of the holding capacitor, and can be chosen to optimize any one parameter for a given application.



*THESE PULLUP RESISTORS ARE USED WHEN INTERFACING TTL LOGIC ONLY.

$V_{OUT} = G(B-A) + V_{REF}$
G = 1, 2, 4, 8

FIGURE 2 – TYPICAL CONFIGURATION

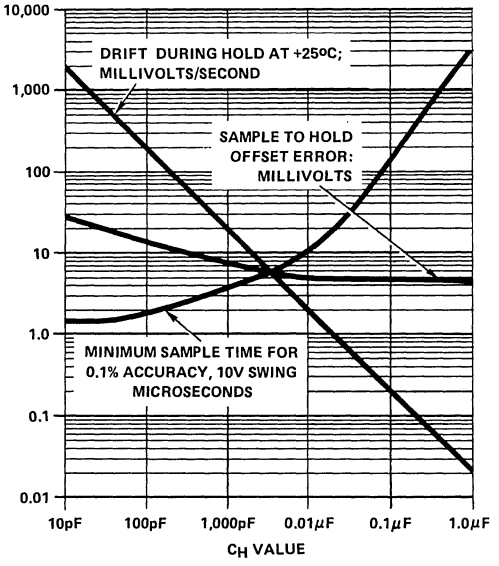


FIGURE 3 – TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITANCE.

APPLICATION HINTS

1. Expanding the Channel Capacity of the HI-5900

Figure 4 illustrates a typical HI-5900 with its channel capacity increased from 8 to 16 channels. Further expansion can easily be implemented by adding more address lines (each additional address line doubles the channel capacity) and the required control logic to enable each multiplexer.

2. The HI-5900 in a Two-Chip DAS

The HI-5900, when teamed with the HI-5712 A/D converter as illustrated in Figure 5, will provide a two-package DAS with 12-bit accuracy and a 50kHz throughput rate. The gain selection of the HI-5900 gives this system a dynamic range of 15 bits.

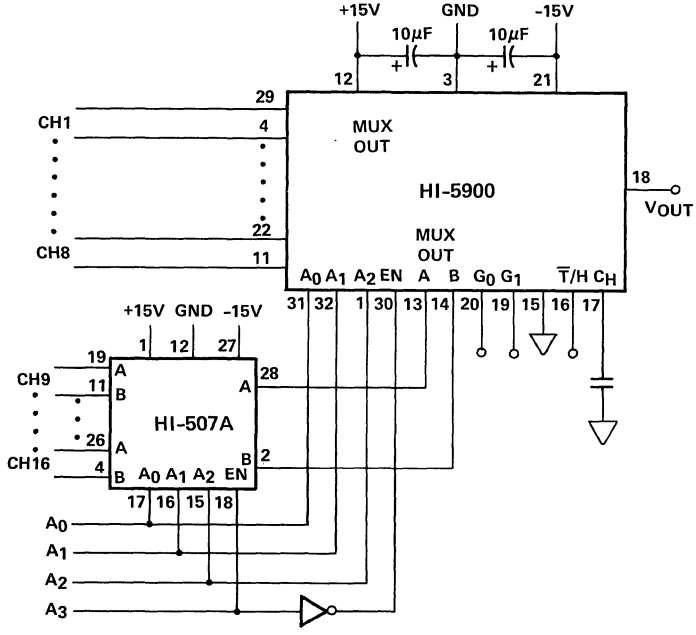


FIGURE 4 – EXPANDING THE HI-5900 TO 16 INPUT CHANNELS.

SELECTED CHANNEL	A_3	A_2	A_1	A_0
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1
11	1	0	1	0
12	1	0	1	1
13	1	1	0	0
14	1	1	0	1
15	1	1	1	0
16	1	1	1	1

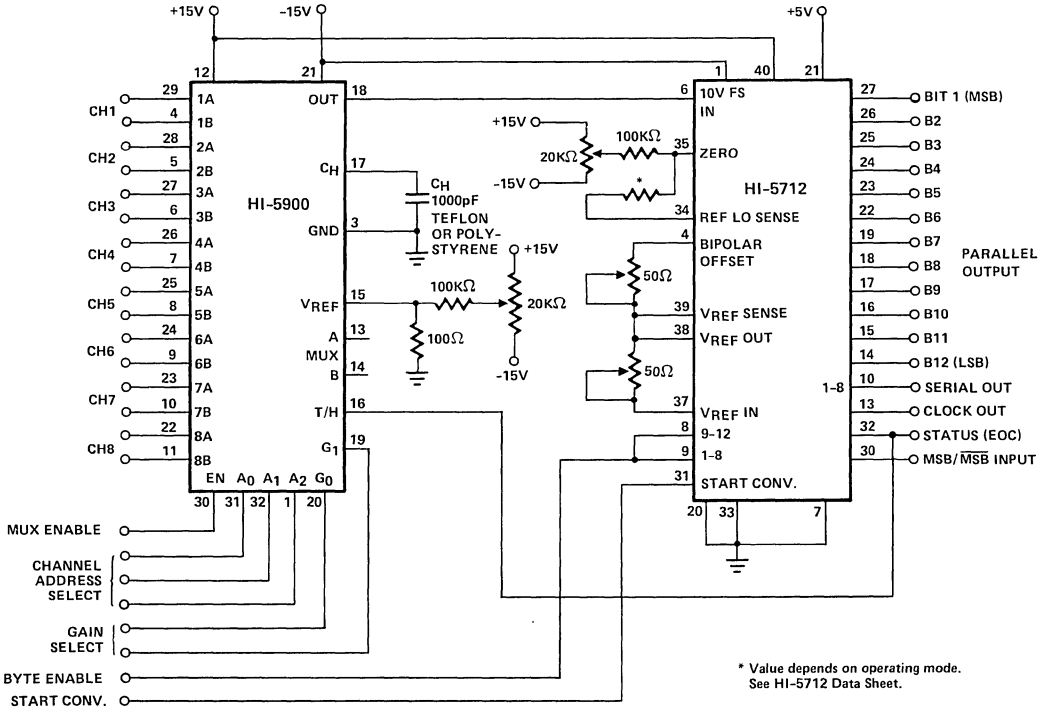


FIGURE 5 – DATA ACQUISITION SYSTEM (USING ONLY TWO PACKAGES).

HARRIS

APPLICATION NOTE 528

INTERFACING MICROPROCESSORS AND MICROCOMPUTERS WITH HI-5712 HIGH PERFORMANCE 12-BIT ANALOG-TO-DIGITAL CONVERTER

BY JOHN E. SULLIVAN

INTRODUCTION

The microprocessor, with its inherent ease of use, flexibility, and numerical computing capability, has become a powerful tool for control and processing in a host of commercial, industrial and military applications. This tool, however, has had limited success in those applications interfacing the real world of analog signals. Until recently the Analog to Digital Converter (ADC), which is the analog input interface to the microprocessor, has only fulfilled part of this function. Various devices are available to easily interface the input analog signal, but require massive support to interface with the microprocessor. This "extra" interface support not only increases the overall system cost and complexity, but also reduces flexibility. The development of the HI-5712, 12 bit high performance analog to digital converter solves these and other problems by providing both an analog and microprocessor interface in a compact dual-in-line package. An LSI circuit performs all logic and interface functions while the balance of the device performs analog processing. Packaged in the unique Leadless Chip Carrier (LCC) - Hybrid form, the HI-5712 provides all the functions required to interface an analog signal to a microprocessor.

DIGITAL INTERFACE

The successive approximation conversion technique is used in the HI-5712, as illustrated in Figure 1. The Successive Approximation Register (SAR) contains all of the digital interface and control logic for conversion and interface control. Constructed using a modified CMOS process (SAJI), the SAR combines the best features of CMOS and TTL logic. All input or output lines are fully TTL/CMOS/NMOS compatible, with inputs having low loading, and outputs providing 3.2mA of sink current in the active mode and less than 25μA loading in the three state mode. All outputs are of a three state design. Data output lines are enabled with a combination of chip enable and three state enable lines, while all other outputs are enabled using only the chip enable line.

The output is structured in byte format with the most significant eight bits enabled by the enable bit EN 1-8 control line, and the least significant four bits enabled by the enable bit EN 9-12 control line. For 8-bit bus applications, the SAR 8-bit output bus can be hardwired in parallel with the SAR 4-bit output bus, eliminating the need for external drivers (see Figures 2 and 3). The fast enable/disable time (typically 60ns) of the output drivers, and their low loading characteristics minimize system integration problems for applications using unbuffered microprocessor buses (Figure 3).

The input architecture of the SAR, provides for real-time program control of analog signal conversion. Two control lines, SHORT CYCLE A and SHORT CYCLE B, control the conversion process. Conversion of 6, 8, 10 or 12-bit analog signals can be configured as per Table 1. The output format, either binary or twos complement is controlled with the MSB/MSB select line. These control lines are all internally latched into the SAR command register on the falling edge of the START CONVERT signal. These input lines can be hardwired to V_{CC}, ground or directly connected to the microprocessor for dynamic program control as illustrated in Figure 3.

TABLE 1

SHORT CYCLE A	SHORT CYCLE B	CONVERSION RESOLUTION
0	0	6 Bits
1	0	8 Bits
0	1	10 Bits
1	1	12 Bits

8

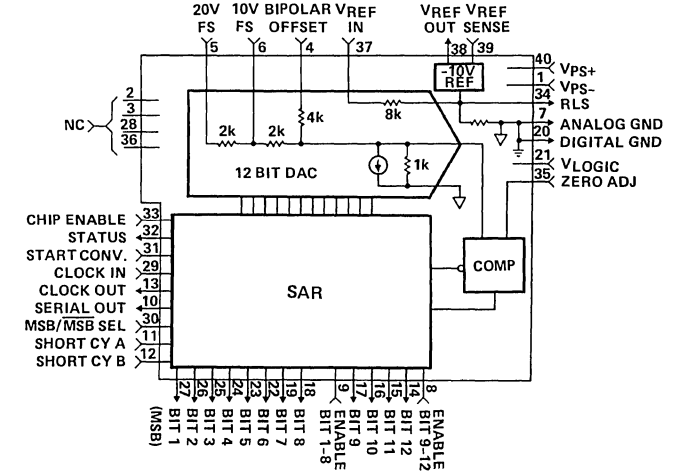


FIGURE 1 – HI-5712 FUNCTIONAL BLOCK DIAGRAM

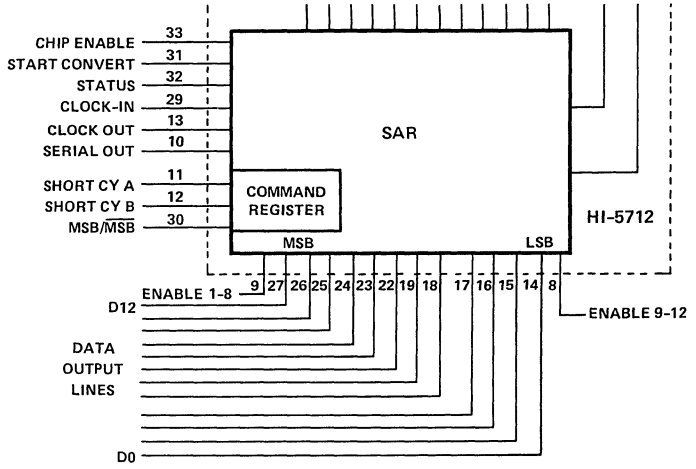


FIGURE 2 – HI-5712 DIGITAL INTERFACE

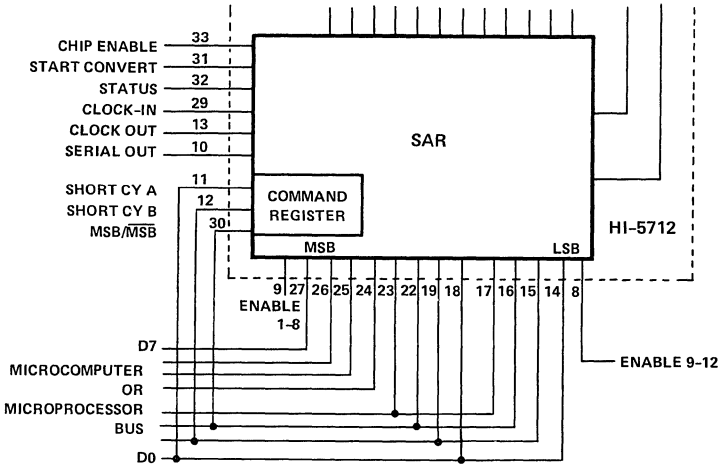


FIGURE 3

Systems requiring serial data transfer can use the serial output data port and clock output to transfer error-free data over twisted pair lines. The SAR also contains an external clock input for those applications requiring external clock synchronization. The balance of the HI-5712 contains analog processing and conditioning circuits for conversion of the input signal.

MICROCOMPUTER INTERFACE

Microcomputer systems using the HI-5712 ADC, unlike other converters, usually require no additional parts for optimum performance. Figures 4 and 5 show interfaces with the Intel 8748 and Motorola 6801 microcomputers. These examples are also applicable to most currently available microcomputers.

Four microcomputer control lines along with the microcomputer bus satisfy all of the interface requirements. Two of the control lines control the flow of data onto the microcomputer bus. The remaining two control lines start ADC conversion and interrupt the microcomputer when data is available. As discussed previously, the command register lines, the four least significant ADC data lines, and the eight most significant ADC data lines are wired in parallel to the microcomputer bus or port. This configuration typically utilizes less than 10% of the bus or port drive capability, allowing connection of additional peripheral support chips, and eliminating the need for buffer or driver devices.

The simplicity of the hardware interface correlates directly with minimal software requirements. The software flowchart in Figure 6 illustrates typical operation. The control word to the HI-5712 need only be applied during the falling edge of the START CONVERT line.

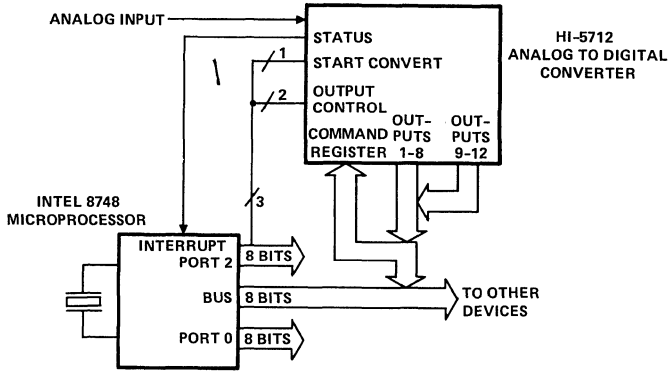


FIGURE 4 – INTEL 8748 MICROCOMPUTER INTERFACE WITH HI-5712 ADC

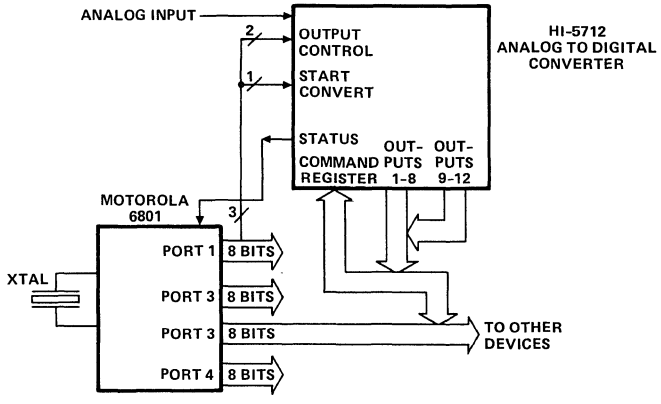


FIGURE 5 – MOTOROLA 6801 MICROCOMPUTER INTERFACE WITH HI-5712 ADC

After meeting the minimum required set-up and hold timing, the data can be removed, freeing the bus for other functions. When the microcomputer receives the interrupt signal, signaling data available, data is then read in two bytes. Since reading of the data is nondestructive, the order of reading can be configured to minimize software requirements.

These microcomputer interfaces, although deceivingly simple, will operate at up to 100kHz throughput rates. At these speeds, high performance complex analog signal processing, for speech, process control and signal analysis applications can be easily implemented.

MICROPROCESSOR INTERFACE

Microprocessor systems are available in two types: the minimum or unbuffered system, and the maximum or fully buffered system. The minimum system is usually found in dedicated or control process applications, while the maximum system is more common in the general purpose application. The HI-5712 ADC is equally well suited for both applications with only a bus driver added to the minimum system configurations discussed here to support the very high drive requirements to the larger maximum system.

As with any peripheral device, the HI-5712 ADC requires address decoding as illustrated in Figure 7 and 8 (Intel 8085 and Motorola 6800 interfaces). The interrupt flip-flop provides stable interrupt generation to notify the microprocessor of data availability when conversion is completed. In a manner similar to the microcomputer, the command register lines and output data lines can be wired in parallel. The minimum system application requires no buffering as the HI-5712 simultaneoulsy exhibits minimum loading with high current drive capability, and can therefore be treated as any other high impedance NMOS peripheral support device.

The software requirement is the same as a microprocessor interface. Command register data can be loaded during a Write cycle with the converter automatically initiating conversion of the rising edge of the Write signal. Data is inputted to the microprocessor in the same two byte format.

The high speed nature of the HI-5712 ADC provides all of the necessary capabilities for use with advanced signal analysis techniques. It should be noted, however, that a 12-bit conversion is completed in 8 microseconds. To fully utilize these high speed throughput rates, microprocessor systems will require operation with a high speed Direct Memory Access (DMA) as most microprocessors cannot keep pace with a 10 microsecond or faster ADC. Systems not incorporating a DMA or other high speed transfer device will be throughput-limited by the microprocessor and not the ADC.

CONCLUSION

High performance analog processing systems using microprocessors can now be easily designed using a minimum of hardware and software support. By careful utilization of the versatile I/O features of the HI-5712, many applications can be implemented with no digital interface hardware and far less software than with other conventional devices. New horizons in signal processing are now realizable. The HI-5712, with its advanced I/O and superior analog characteristics, is an ideal solution for microprocessor/microcomputer systems with analog input interfaces.

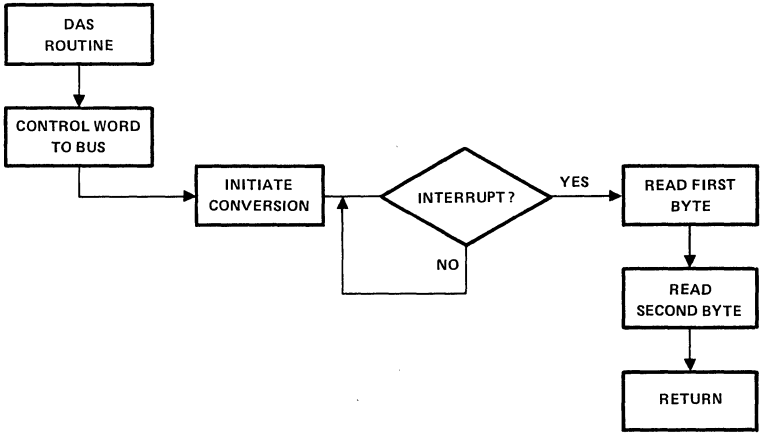


FIGURE 6 – SOFTWARE FLOW CHART FOR MICROCOMPUTER OR MICROPROCESSOR CONTROL OF ADC

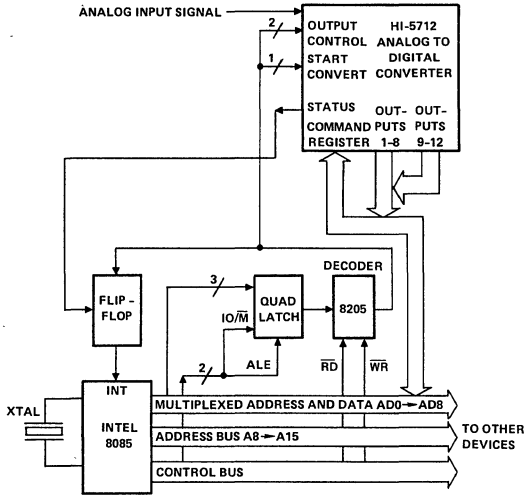


FIGURE 7 – INTEL 8085 MICROPROCESSOR

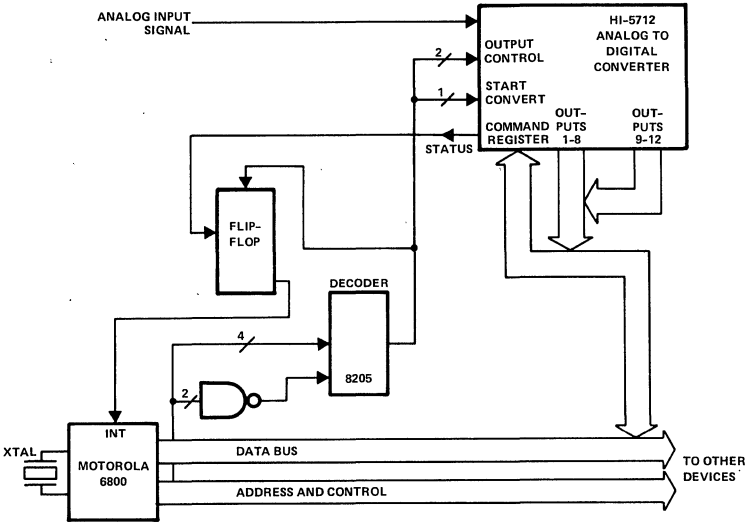


FIGURE 8 – MOTOROLA 6800 MICROPROCESSOR WITH HI-5712 ADC

HARRIS

APPLICATION NOTE 529

MICROPROCESSOR INTERFACE METHODS FOR HIGH-SPEED DATA ACQUISITION SYSTEMS

BY L. E. ENRIQUEZ, J. E. SULLIVAN, D. T. TUNG

Since their introduction in the early 1970's microprocessors have dramatically displaced random logic for system design. This explosive growth of microprocessor applications has greatly influenced the increased use of peripheral interface integrated circuits (IC's). These special IC's were developed to support CRT's, printers, floppy disks and other peripheral devices, but virtually none were offered for analog input signal conditioning and conversion. Typical systems using a single microprocessor board and multiple analog interface boards became commonplace due to the lack of suitable analog interface IC's. Today, new units are available which provide microprocessor compatibility with analog input signal conditioning and processing within compact hybrid devices comparable in size to individual IC's. These new products permit the assembly of a complete analog interface and microprocessor system on a single board no larger than those used in the past for the microprocessor alone. The HI-5900 and the HI-5901 analog signal processors and the HI-5712 Analog to Digital Converter (ADC) are state-of-the-art versions of these new hybrid devices.

A typical analog to microprocessor interface (data acquisition subsystem) consists of five functional blocks. (See Figure 1). Multiple input signals are accepted and selected by the input multiplexer, with the programmable gain instrumentation amplifier providing both common mode signal rejection and signal amplification. Additional signal processing is required between the output of the instrumentation amplifier and the ADC, for the latter cannot convert a continuously changing analog signal into digital form. The additional processing is provided by the track-and-hold stage, which samples the instantaneous value of the analog signal on command and holds this level as a steady input to the ADC until the conversion cycle is completed. The ADC supplies a series of digital output words, which correspond to the individually sampled analog levels. Finally, digital logic circuitry is required to interface the function control signals from the microprocessor to the individual circuit elements.

As shown by the dotted lines in Figure 1, two hybrid devices, the HI-5900 (or the HI-5901), and the HI-5712 contain all of the necessary analog and digital building blocks needed, for a complete two package, multi-channel data acquisition subsystem. The HI-5900 includes an eight-channel differential input multiplexer, a precision gain programmable instrumentation amplifier and a unity gain track-and-hold stage. Designed for 16-channel pseudo-differential or single-ended applications, the HI-5901 features a 16-channel multiplexer, a precision gain programmable instrumentation amplifier and a unity gain track-and-hold amplifier. All input control lines are microprocessor compatible and well suited for NMOS, CMOS, and TTL logic.

The HI-5712 is a 12-bit, high speed ADC which features a microprocessor compatible tri-state output bus and software programmable output code and word length controls permitting its application in 8, 12, and 16-bit systems. Accepting either unipolar or bipolar inputs, the device incorporates input latches on all digital control lines, assuring full compatibility with TTL, CMOS, and NMOS logic. The unit also features an on-board, overridable, precision +10 volt reference with sufficient output current capability for external applications.

Unlike conventional hybrid technology, these products are fabricated using leadless chip carrier (LCC) techniques, which employ IC dice packaged in LCC's mounted to both sides of a multilayer ceramic substrate. The final product comprises hermetically-sealed building blocks, each visually inspected and mechanically and electrically tested to the highest standards of commercial, industrial, or military specifications prior to assembly. Subsequently, additional visual and electrical tests are made to the completed hybrid device at nominal and rated temperature extremes to ensure maximum reliability and optimum performance.

When used in combination, the HI-5900 (or 5901) and the HI-5712 form a high performance, extremely accurate two-package data acquisition subsystem with a 50 kHz (600 kbs) throughput rate. The system is compatible with all standard microprocessor systems although the interface peripherals required will vary from one system to another, depending on individual system complexity. An example of a two chip, high performance data acquisition subsystem using a microcomputer is illustrated in Figure 2. This example, using the Intel 8748 series microcomputer, is applicable to any of the

currently available chip microcomputers. Both hardware and software requirements have been minimized to reduce costs and provide maximum flexibility.

Four microcomputer control lines along with the microcomputer bus satisfy all of the interface requirements. Two of the lines are used to initiate data conversion and to interrupt the microcomputer when data is available The remaining two lines enable data onto the bus under microcomputer control. The bus is structured so that channel selection, amplifier gain and ADC modes of operation are controlled by simply outputting data to the bus. Input data is in the form of two bytes: the first byte contains the most significant eight bits with the second byte containing the least significant four bits. Due to the high impedance nature of the Harris parts, other devices can be added to the bus without exceeding bus load limitations.

The complete DAS operates under software control for maximum flexibility. A microcomputer internal software timing loop establishes the necessary hardware timing signals. The software flowchart in Figure 3 illustrates typical system operation.

The system as depicted operates at a 50 kHz throughput rate, while maintaining true 12-bit accuracy throughout the temperature range. Similar high performance DAS's can be implemented for a variety of applications and offering compatibility with most microcomputers.

Interfacing a DAS to a microprocessor system bus is similar to interfacing any other peripheral device. Figure 4 illustrates an interface for a typical microprocessor bus and is applicable to all popular microprocessors.

As with any peripheral, a bus driver and address decoder is required. The octal latch provides stable control information during signal acquisition while the one-shot generates a start convert pulse after the required 10 μsec delay. Two I/O locations are used for the interface: one location is used for both Read and Write and the other is a Read only. A Write to the first location loads multiplexer gain and ADC control information and 10 μsec after the Write initiates a conversion cycle. At the end of conversion an interrupt is generated informing the microprocessor that data is available. Data can then be read in the same two byte format as previously discussed for the microcomputer. Software control for this application is merely a driver routine to support the two I/O locations and the interrupt routine, with all timing functions being generated in the hardware.

Further enhancement of system performance can be achieved with Direct Memory Access (DMA), FIFO's and other circuits to alleviate the high speed data handling requirements that a 50 kHz throughput DAS places on the microprocessor.

In conclusion, a single board microprocessor DAS can now be easily implemented using newly available hybrid analog interface devices. These devices not only support the requirements of microprocessor system buses but provide superior performance compared to discrete designs, while using far less printed circuit (PC) board real estate. The versatile HI-5900, HI-5901 and HI-5712 devices offer ideal solutions for these and other applications requiring high performance, and cost-effective microprocessor interface capability.

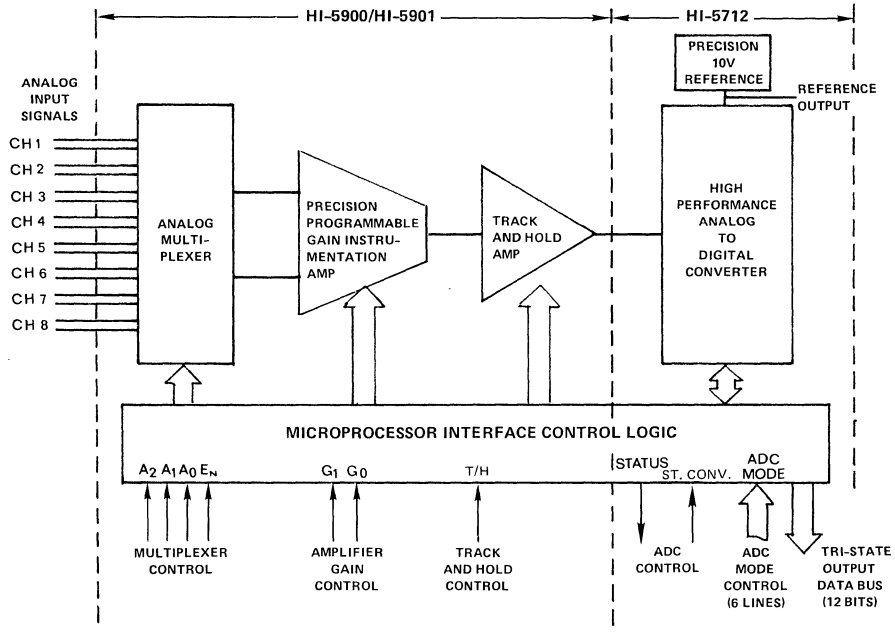


Figure 1 Data Acquisition Subsystem

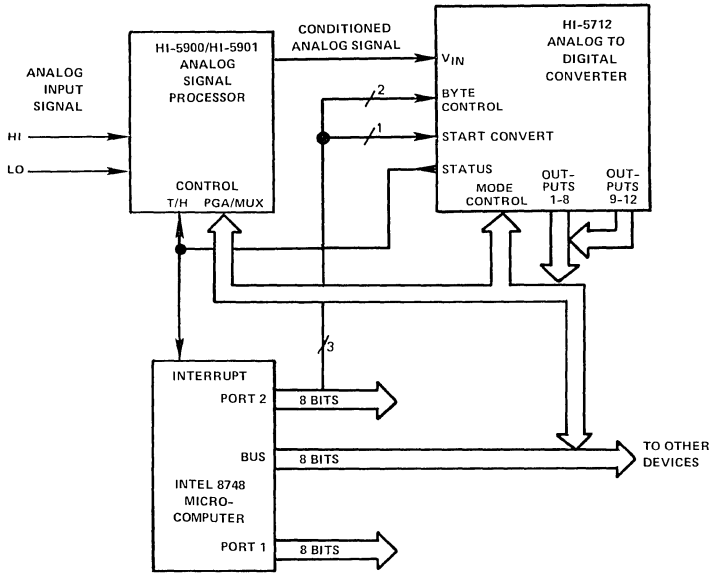


Figure 2. Microcomputer with High Performance Data Acquisition Subsystem

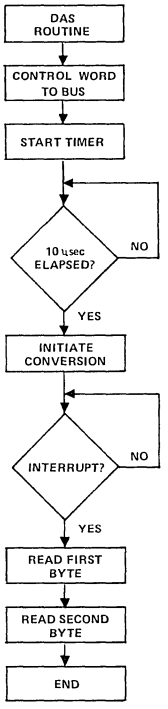


Figure 3 Software Flowchart

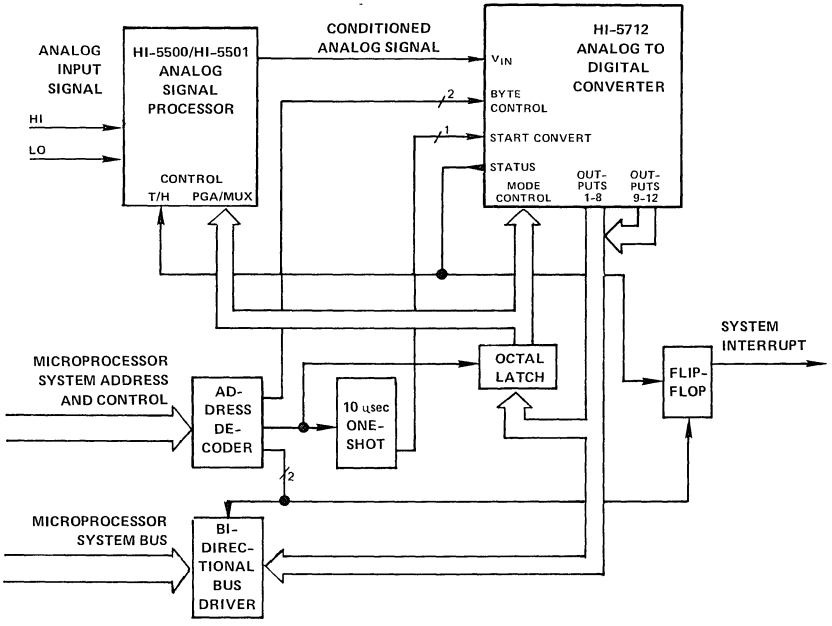


Figure 4. Microprocessor DAS and Interface

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APPLICATION NOTE 530

A DATA ACQUISITION AND CONVERSION SYSTEM WITH LESS THAN ±1 LSB OFFSET ERROR

BY JOHN E. SULLIVAN

The continuing pressure for higher resolution and higher accuracy Data Acquisition Systems requires smaller overall system offset errors. Historically, with eight-bit systems, offsets of up to 30 or 40 millivolts were acceptable, and the use of trimpots or fixed resistors for adjustment was more than adequate. State-of-the-art systems with 12 to 16-bit resolution, however, require total system offset over temperature to be less than 5 millivolts. Offset voltages of this magnitude are difficult to achieve using trimpots, and extremely difficult to stabilize in uncontrolled thermal environments.

Ideally, a DAS system should have less than ±1 LSB of offset error regardless of the number of bits incorporated in the system. This goal is extremely difficult to achieve using linear design techniques. Digital design techniques, however, can be used to null offsets, typically to ±1/2 LSB over the complete temperature operating range.

A typical Data Acquisition System is illustrated in Figure 1. System offset correction can be accomplished at any stage even though each stage contributes to the overall offset. The first step to offset correction is to have the analog to digital converter (A/D) calculate the digital code representing total system offset when the input is grounded. This code, when converted back to analog form, inverted and added to the input circuitry at a convenient point, will null all offsets.

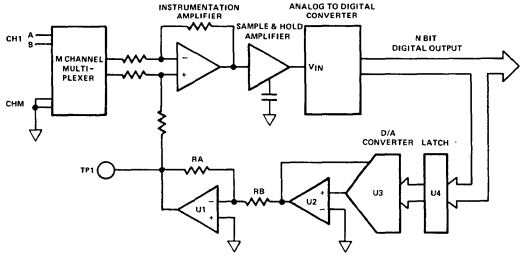

Figure 1 – Typical Data Acquisition Block Diagram

Figure 2 shows a simple digital offset correction scheme. The additional digital to analog converter (D/A) U3 and op amp U2 convert the calculated digital offset code back to analog form. Op amp U1 inverts this signal and adds it to the input differential amplifier. The inverted signal is scaled by resistors RA and RB such that a 1LSB step of the A/D is equal but opposite in sign to a 1LSB step of the D/A at TP1. This scaling can be calculated by Equation 1.

Equation 1

$$\frac{VP_1}{2^{n1}} = \frac{RA}{RB} \quad \frac{VP_2}{2^{n2}}$$

Where: VP_1 = Dynamic range of Linear A/D in volts

n_1 = Number of Bits of A/D

VP_2 = Dynamic Range of Linear D/A in volts

n_2 = Number of Bits of D/A

RA = Feedback Resistor

RB = Input Resistor

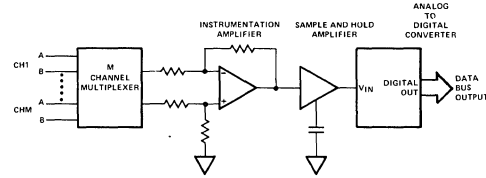

Figure 2 – Digital Error Correction Block Diagram

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Measurement of the system offset is made with all digital input bits to the D/A set at logic 0. Further, the D/A is configured for bipolar operation so that a digital input bits to the D/A set at logic 0. Further, the D/A is configured for bipolar operation so that a digital zero input results in a positive half full scale output voltage at TP1. This ensures that the A/D need only measure positive offset voltages and not negative voltages, allowing for systems operating both in uinpolar and bipolar modes.

The size of the D/A converter is determined by the maximum amount of offset that must be corrected by the system:

Equation 2

$$\text{D/A Size (Bits)} \geq \frac{\ln\left(\frac{\text{Max offset}}{VP_1}\ 2^{n1}\right)}{\ln(2)}$$

In operation, a spare input channel is grounded and the input to the D/A is forced to digital zero. The resulting compound offset, Voffset, is then equal to the voltage at TP1 plus all component offsets. The A/D then calculates a digital code representing V_{offset} which is latched into the D/A. Due to the inversion and scaling of the Op Amp U2, this is equivalent to subtracting Voffset from the half full scale output of the D/A. Obviously the result is the nulling of V_{offset}.

The most critical parameter in this circuit is the ratio of the resistors RA and RB. This ratio will determine the overall accuracy of the correction, and 1% resistors are sufficiently accurate to null all offsets. Normally for 12 and 14-bit systems, a 6-bit DAC will correct all possible offsets.

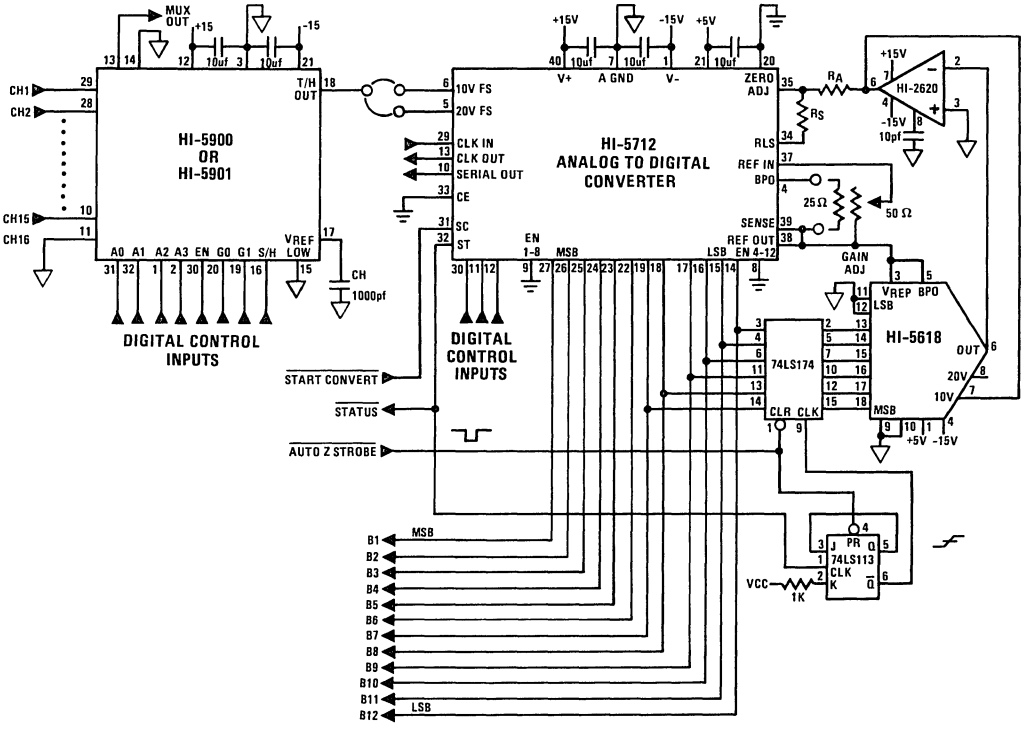

Figure 3 – Auto-Zero Analog to Digital Converter

Various configurations can be employed to minimize parts count. Fully automatic offset correction is added to the HI-5900/HI-5712 DAS component set using only four additional I.C.'s as shown in Figure 3. External digital logic or a microprocessor selects a spare input channel which has been previously grounded. Receipt of the Auto-Z strobe initializes the auto-zero function by clearing the latch to all zeroes, resulting in a D/A output of 32 LSB's of positive offset. The microprocessor then initiates an analog to digital conversion sequence. The Conversion Complete status line of the A/D causes the latch to strobe and store the digital offset correction term to the D/A converter. The analog correction term is then injected into the zero adjust pin of the A/D converter. Care must be taken when injecting the correction term to this point on the A/D since the ratio of RA/RB is affected by the impedance of the summing junction.

Table 1 lists the accuracy of correction for various full scale input ranges. The offset after correction listed in the Table is the maximum observed offset when 10 different 5900's and 5712's were tested at all temperature ranges between -55°C, and +125°C ambient. In no case did the offset after correction ever exceed 1LSB of the analog to digital converter.

HI-5712 INPUT CONFIGURATION	R_S	R_A	OFFSET AFTER CORRECTION
0 TO +10V	681Ω	147kΩ	0.5mV
0 TO +20V	825Ω	147kΩ	1.0mV
-5V TO +5V	580Ω	147kΩ	1.0mV
-10V TO +10V	681Ω	147kΩ	2.0mV

Table 1 – Offset Correction Accuracy

Along with the straight forward benefit of greatly improved offset performance, this correction technique eliminates the requirement for any offset adjustments, either initially or during the operating life of the DAS. In practice, the auto-zero function need only to be used after system power is applied or after a significant change in ambient temperature. Therefore, high performance microprocessor-based DAS systems requiring maximum performance can employ this technique to improve accuracy with minimal impact on throughput rate.

HARRIS

APPLICATION NOTE 531

ANALOG SWITCH APPLICATIONS IN A/D DATA CONVERSION SYSTEMS

BY RICHARD WHITEHEAD

INTRODUCTION

A choice of three approaches is available when implementing a data conversion system: 1). "build-from-scratch", 2) buy sub-systems and configure a system, or 3) purchase a pre-engineered system which meets the requirements. Also, as a matter of economics, the users of sensor-based data acquisition systems make it common practice to ensure a maximum number of elements are shared in the system. An invaluable tool used in this process is the analog switch or multiplexer. The purpose of this article is to focus attention on those parts of the system which require analog switches and to emphasize the importance of relative operating parameters.

BASIC SYSTEM CONFIGURATIONS

A/D data conversion systems can be categorized into two general groups: 1) low level signal conversion (analog signals below 1 volt) and 2) high level signal conversion (analog signals above 1 volt). Within these categories, four basic data conversion configurations are illustrated to point out the advantages of using analog switches.

Conditioning the analog signals prior to multiplexing (Figure 1A) is the most popular system arrangement and is both efficient and capable of high performance This configuration, which shares the level signals. Figure 1B represents a more austere approach resulting in lower cost and decreased performance. This type is useful in less demanding applications such as processing high level signals. To process multichannel, single event information such as wind tunnel or seismographic measurements the arrangement shown in Figure 1C is most likely to be used. This configuration represents a more expensive, less efficient approach due to the decreased number of shared elements. Figure 1D shows the elimination of the analog multiplexer and sample and hold circuits. By moving the multiplexing task to the digital domain, slower and lower cost A/D converters can be used.

TYPES OF ANALOG SWITCHES

The most commonly used types of analog switches found in today's data conversion systems are: reed relay, JFET, and CMOS. Reed relays offer low ON and high OFF resistance and are capable of handling very high voltages, but have slow speeds. JFET switches have lower OFF leakage current and are capable of very high speeds. CMOS switches, which are the most popular and widely used in multiplexer applications, have low OFF leakage currents, good speed, and stable ON resistance under varying input signal conditions.

SELECTING THE PROPER CMOS ANALOG SWITCH

The data conversion system error budget should be used to narrow the field of CMOS analog switches suitable for the application. Primarily, the speed of the switch must be consistent with the systems's sample rate requirements without introducing unacceptable transfer error. Significant dynamic errors inherent to CMOS analog switches are OFF channel leakage current and a settling time value dictated by the device's ON resistance and its inherent capacitance. Figure 2 shows the equivalent of a CMOS analog switch giving all of the inherent and distributed properties which may become the source of unwanted system errors.

Other system restrictions may further narrow the field of candidates suitable to performing the switching task. These restrictions could include, low power budget, hostile environment, cost, alternate sourcing, and package density. It's possible that all of

these restrictions could occur, and this situation may influence the user to seek a compromise solution to his problem.

Fortunately, CMOS analog switches consume very little power and only the most demanding power budget would feel the strain of their power requirements. If the operating environment of the device includes high voltage spikes, excessive noise pickup, and/or power supply interruptions, the selection should be narrowed to the internally protected analog devices such as the HARRIS HI-506A/507A. These multiplexers come with guaranteed overvoltage specifications which enhance the reliability of the data conversion system. Usually, package density, cost restrictions, and alternate source requirements are simultaneously applied, and with present CMOS analog switch availability from several vending sources, these problems should be minimal. It should also be ensured that the CMOS analog switch selected does not exhibit any inherent latch-up tendencies. The Harris dielectrically isolated CMOS analog switches offer latch free operation.

To some users the proper CMOS analog switch selection may become complicated leading to possible alternate solutions. An example of such a situation could be in high speed data conversion system where the settling time constraint placed on the multiplexer results in an unacceptable time penalty (Figure 3A). Figure 3B shows an alternate and practical solution to this problem. The two tiered multiplexing scheme may reduce the errors caused by leakage currents and settling time by an order of magnitude. Another practical solution would be to select an analog signal processor such as the HARRIS HI-5900/5901 shown in Figures 4A and 4B. These devices facilitate user application and reduce engineering time thereby reducing overall cost.

OTHER USES FOR CMOS ANALOG SWITCHES

Attention has been focused on the selection of CMOS analog multiplexers used to increase efficiency of data conversion systems through shared elements. But the versatile CMOS switch is not limited to only that function. Obviously they can be used in sample and hold circuits, with important parameters being switching speed, OFF leakage current, and charge transfer. Analog switches such as the HARRIS HI-200/201 and HI-300 series may be used in sample and hold circuits and also in auto-zeroing circuits for integrating type data converters (Figure 5).

Figure 6 shows the CMOS analog switch used to program the gain of an instrumentation amplifier.

HIGHLIGHTS

In A/D data conversion systems analog switches are mainly used as multi-channel multiplexers to increase system efficiency through shared elements.

CMOS analog switches are the most widely used in data conversion systems.

When selecting the proper CMOS analog switch, look for low OFF leakage current, good settling time, latch free operation, and stable ON resistance under varying analog signal input conditions.

If the environment is hostile, select from the internally protected CMOS analog switches.

Where an alternate solution is required, attempt to ensure your solution is the most practical with respect to your error budget.

References:

Garrett, Patrick H. Analog Systems for Microprocessors and Minicomputers. Virginia: Reston Publishing Company, Inc., 1978.

Kaufman, Milton and Seidman, Arthur H. Handbook of Electronic Calculations. New York: McGraw-Hill Book Company, 1979.

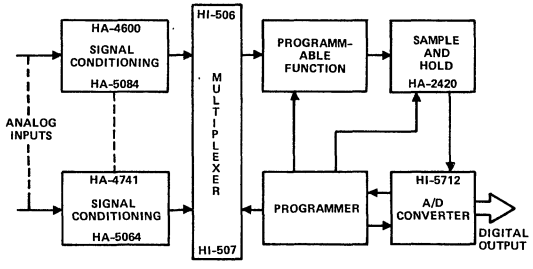

Figure 1A – Multiplexed. Signal Conditioning for Low Level Inputs

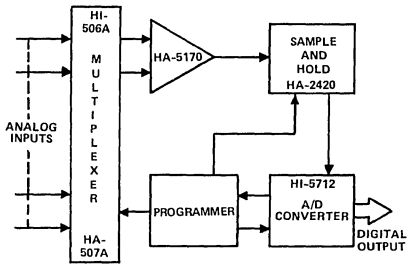

Figure 1B – Multiplexed, High Level Inputs

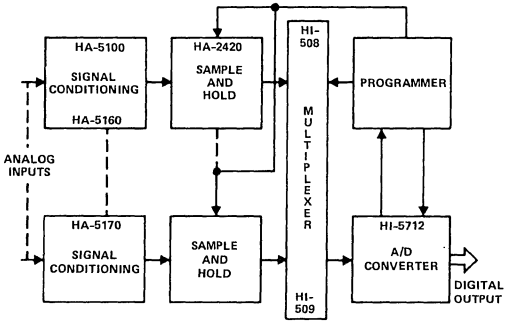

Figure 1C – Multiplexed, Sample / Hold Outputs

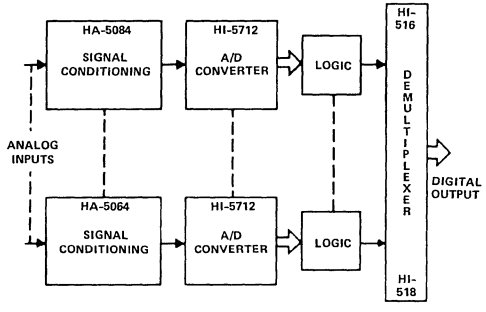

Figure 1D – Multiplexed, Demultiplexer
A/D Outputs

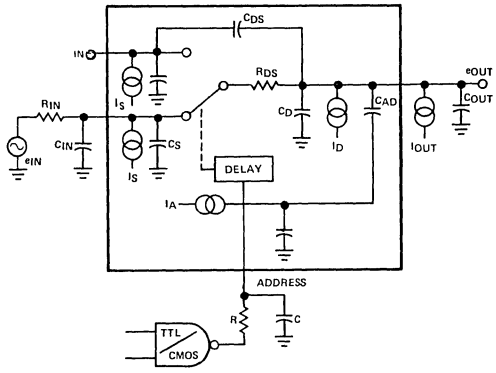

Figure 2 – Equivalent CMOS ANALOG SWITCH
DC Offset Error = $R_{DS} \times I_D$
Setting Time Determined by $R_{DS} \times C_D$

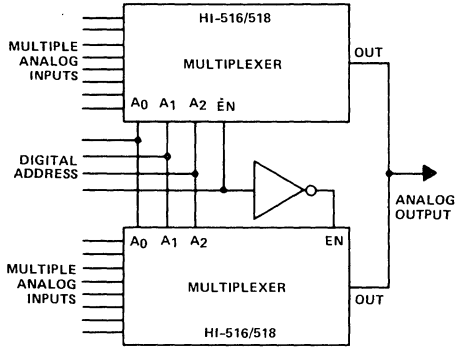

Figure 3A – Cascaded Multiplexers: Output Leakage Currents and Output Capacitance Increase Errors

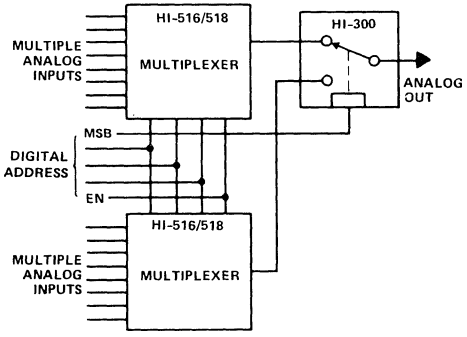

Figure 3B – Cascaded Multiplexers Two - Tiered Method : Errors Reduced Through Shared Switch

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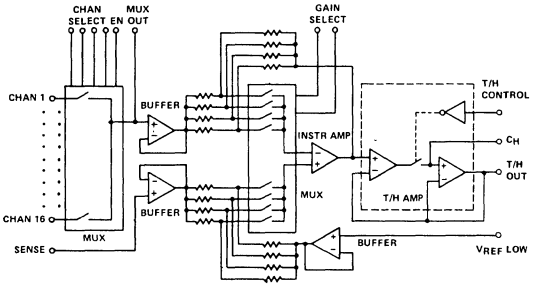

Figure 4A – HI-5900 Analog Signal Processor

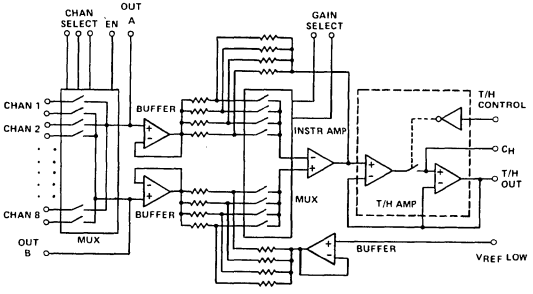

Figure 4B – HI-5901 Analog Signal Processor

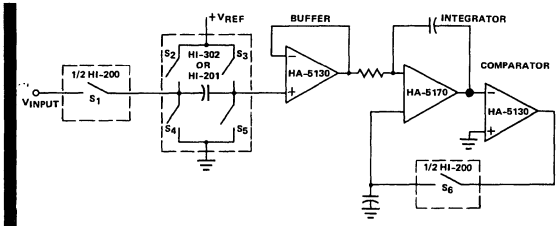

Figure 5. This autozero integrating converter uses six analog switches – S_1 through S_6. Zero correction occurs when S_3, S_4 and S_6 are "on". Integration occurs with S_1 closed. Integrate-reference takes place when S_2 or S_5 is "on".

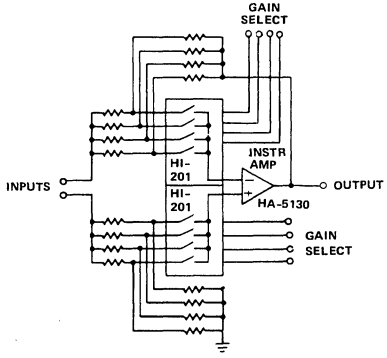

Figure 6 – Programmable Gain Instrumentation Amplifier

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APPLICATION NOTE 532

COMMON QUESTIONS CONCERNING CMOS ANALOG SWITCHES

BY CARL WOLFE

INTRODUCTION

The following information is a direct result of a significant amount of time spent in response to questions from users of HARRIS analog switches. Among the variety of questions are a few which seem to be asked more frequently than others. Over the next few pages, these questions are discussed with the hope that the answers will be helpful to the users and potential users of HARRIS analog switches. Some questions are technical in nature while others are simply questions on interpretation of the HARRIS Analog Data Book.

POWER SUPPLY CONSIDERATIONS

The first two questions are similar questions and the explanation will apply to both:

QUESTION #1: If the power supplies are off, will the switch be open? (Present a high impedance to the input signal)

QUESTION #2: If the power supplies are off, can an input signal be applied?

Both of these questions refer to an overvoltage condition when the supplies are off and an input signal is applied. A common misunderstanding is that the switch will be open and block the signal when actually the opposite occurs.

What is meant by the power supplies being off? Does it refer to the supplies being shorted to ground or does it imply they are open circuited?

If the power supplies go to ground, the input signal will pass through the switch and appear at the output. The explanation for this can be seen in Figure 1, which is a simplified CMOS switch cell. This switch cell consists of two enhancement type field effect transistors, one N-channel and one P-channel. An enhancement type of device is a FET which is normally off without some potential (gate voltage) to turn it on. A P-channel FET requires a negative potential (gate to source voltage) to turn it on and an N-channel FET requires a positive potential (gate to source). Contained in the physical structure of the FETS are parasitic transitors which are shown in Figure 1 as diodes from the source and drain to the body potentials of the devices. These diodes or parasitic junctions are normally reversed biased. If those junctions are forward biased, a fault condition exists where the signal is passed through the parasitic transitor. This is what occurs if the power supplies go to ground. Depending on the polarity of the input signal, either the N or P channel FET parasitics will be forward biased and the signal passed through the switch.

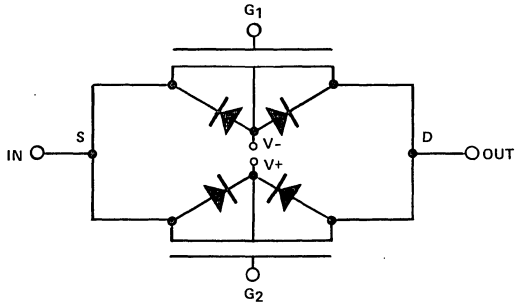


Figure 1. Basic CMOS Transmission Gate

Having the signal pass through the switch may be acceptable in some applications, but most likely it is not. An example would be user who was switching various voltages (transducers) as shown in Figure 2. If the supplies go to ground and these signals pass through the switch, the input voltage sources could easily be shorted.

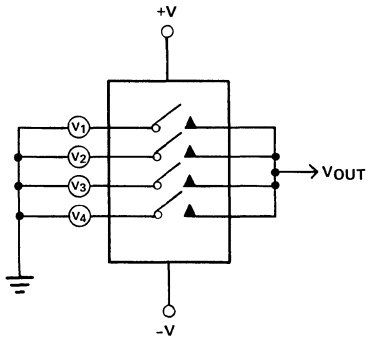


Figure 2. Switching Multiple Inputs

Another situation occurs if the power supplies are open circuited where the most positive and negative input signals will provide power to the switch. In this case, the signals being used for power will be passed to the output, but the remaining switches with inputs less than those used for supply will operate properly.

INPUT OVERVOLTAGE PROTECTION

There is a possibilty the switch will be damaged if exposed to excessive current levels during an overvoltage condition. A second overvoltage condition is the case where the input signals exceed the existing power supply levels. Neither of these situations are recommended and the following questions are similar to those frequently asked.

QUESTION #3: Can an input greater than the supplies be applied?

QUESTION #4: In my application, there is a possibility that the switch will lose power and the input signal will still be applied. Is there a way to protect the switch if this situation occurs?

Referring to Figure 1 once again, if the input signal exceeds the supply by an amount greater than the breakdown voltage of the parasitic junction, the normally reversed biased junction will come forward biased. These forward biased junctions will pass the input signals to the output and possibly short out the input voltage sources.

The most common form of protection circuit for these types of overvoltage conditions is the resistor-diode network at the input of the switch as shown in Figure 3.

This circuit protects the device if the supplies go to ground or if the input exceeds the supply. If either of these situations occur the diodes will be forward biased and current path to ground will exist. This will protect the switch from excessive current levels. The primary purpose of the resistor is to limit the current through the diode.

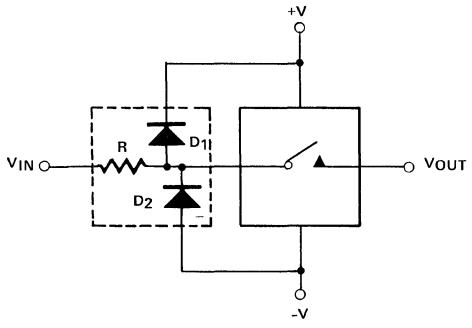


Figure 3. Protection for Each Analog Input

Another advantage of using diode protection is that it prevents the input signal from passing to the output. This is a result of the input being clamped to the breakdown voltage of the protection diodes. If this breakdown voltage is less than the threshold voltage (turn on voltage) of the parasitic diodes, the parasitic transistor will remain reverse biased and the signal will not pass through the switch.

There are some disadvantages to the user with this type of protection. One would be the economics involved with using external protection for each analog input. This could present a cost problem if a large number of channels were involved. Another concern would be the current limiting resistors which adds to the on resistance of the switch contributing to the overall system error. A further possible source of error is current leakage in the diodes. It is recommended that low leakage diodes, such as schottkey diodes be used.

The protection circuit just discussed is not used to protect the switch from latch up. The HARRIS switches are constructed using the dielectric isolation process and the four layer SCR found in JI technology does not exist. This circuit is intended to protect the device from high current levels which result from the forward biasing of the parasitic transistors which are inherent in all FET structures.

If for some reason the resistor-diode protection circuit cannot be used there are other possibilities. The following method may help to avoid the extra cost of protecting each input. In this method, since the supplies are open circuited, the most positive and most negative signal will power-up the chip and any input with signals less than those being used for power will operate properly. However, this method can only be used if the outputs are not common and a user can afford to have at least two signals pass to the output.

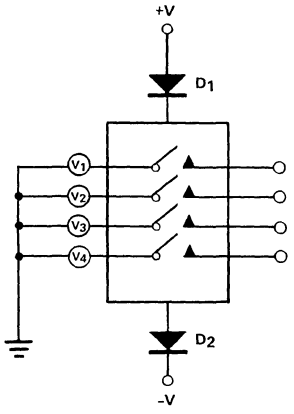


Figure 4. Powering the Switch With the Input Signals

Another alternative does not involve protection circuitry, but instead takes advantage of CMOS technology. An example would be a user who has ±15V supplies and needs to switch a +18V signal as shown in Figure 5. This appears to be an overvoltage condition since the input exceeds the supply. But rather than protect the device, the user can shift the supplies to +20V, -10V. Now the input signal is within the supply level and the switch should work properly. In certain applications the supply voltages can be adjusted in order to pass a larger range of input signals.

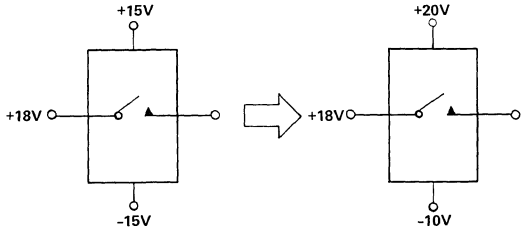


Figure 5. Varying the Supplies to Meet the V_{IN} < V Supply Requirements

SINGLE SUPPLY OPERATION

Single supply operation is a topic which is discussed frequently and the following are examples of typical questions.

QUESTION #5: Can the switch be operated at a single power supply?

QUESTION #6: What is the minimum power supply possible?

Usually engineers with critical power requirements request single supply operation. An example would be battery operated applications such as portable equipment. In these cases the designer is limited to single supply, low supply or both.

Trade-offs exist with single supply operation that should be pointed out to the user. An example is the HI-300 series of switches which has the capability of operating with a single +5 volt supply. The performance of the switch will vary, however, as the supply voltage varies. So, for the HI-300 series, as supply voltage decreases, the on resistance and the switching times increase. A 300 series switch with a single +5 volt supply will have higher on resistance and slower switching speeds than the same device at ±15 volts or even a single +15 volt supply. This represents a change in both DC and AC performance. Even though the switch may now meet the users power requirements at single supply, the question is whether it will still meet the performance requirements.

The explanation for these variations can be found in the FET devices composing the switch cell itself. The variation in on resistance is due to the fact that the channel impedance of FET is dependent on the gate - source bias. Since the gate voltage is determined by the supply voltage, it can be concluded that the on resistance is a function of the supply voltage.

The fact that the on resistance varies with supply voltage directly relates to the slower switching times, since the higher on resistance will reduce the available current needed to charge the internal capacitance of the switch. Lower changing current relates directly to slower switching times.

QUESTIONS ABOUT HARRIS SWITCHES

Many of the questions asked about switches could apply to any CMOS switch manufacturer's products. But some questions are unique to both the Harris product line and data catalog. The following are examples of some of the more common questions concerning the Harris Analog Data Catalog.

QUESTION #7: What is the difference between the VL and VR pins on the HI-5043 and V_{REF} pins on the HI-201 ?

The device pins mentioned above have their own individual functions even though they are all associated wth the logic reference circuits of their respective designs. For the HI-201, the V_{REF} pin is the terminal which establishes the logic threshold levels for which the switch will change state. Although it is normally left open when driving from +5V logic (DTL or TTL), it can be connected to a higher supply in order to raise the switching threshold levels when driving from CMOS Logic greater than 5 volts. The V_{REF} pin enables the user to change from TTL to CMOS Logic.

The reference circuit of the HI-50XX series of switches is different from the HI-201, which accounts for the V_R and V_L pins. Even though the V_R terminal is brought out on the package, it is recommended that this pin be grounded. This terminal establishes the ground for the internal ref-

erence circuit. The V_L pin performs a similar function to the V_{REF} pin on the HI-201. It is normally connected to 5 volts for TTL logic but can be tied to a higher supply for CMOS levels. This effectively raises the switching thresholds to accomodate the higher CMOS level.

The next question is easily the most frequently asked question about HARRIS HI-50XX series of switches.

QUESTION #8: Are the switch functions shown on the data sheet a result of the logic address being HIGH or LOW ?

Actually, the answer to the question is printed at the top of the data sheet page,depicting switch functions "switch states are for a logic 1 input". Therefore, the address is in the HIGH state for the switch functions shown on that page.

Some other areas which are often questioned on the data sheets are the maximum ratings and performance between channels of the switches. The following questions are typical:

QUESTION #9: Will the switch operate at the absolute maximum ratings?

The topic of absolute maximum ratings does create some confusion. Basically, the contents of the Electrical characteristic table are the guaranteed parameters. The switch may operate with conditions other than those recommended, but are not guaranteed parameters. Anything above absolute maximum ratings may permanently damage the device.

Problems sometime arise when a customer tests some parts at conditions other than those which are guaranteed. If the parts work, the user may go ahead and design around these conditions. But there is a good possibility the next batch of switches may not perform in the same manner. The user must be aware that anything outside the guaranteed limits is a user's risk and susceptable to variations in manufacturing.

QUESTION #10: What is the variation in "on" resistance between channels on the switch?

There are two causes for these variation. One cause is process variation which is due to variables in manufacturing. This can create variation between channels on the same unit. The second reason is lot variation which can cause differences in performance from unit to unit. After all variations are taken into account, a good "rule of thumb" is ±10% tolerance on typical parameter values. So if a device has a typical on resistance of 50Ω , a user could expect a ±5Ω variation.

HARRIS

APPLICATION NOTE 533

A MONOLITHIC SUBSCRIBER LINE INTERFACE CIRCUIT

BY DAVID P. LAUDE

INTRODUCTION

This application note describes the HC-5501 and HC-5502 SLICs. These are monolithic low current (LC) SLICs for use in PABX or Central Office (CO) applications which are fabricated with 80 volt Dielectric Isolation technology. The HC-5502 has enhanced surge voltage capability, and requires two extra external resistors as shown in the application circuit. The SLIC-LC provides battery feed with power denial control and loop current limiting, overvoltage protection (with some external devices), ringing relay control, line supervision with off-hook, ring trip and ground key detection and 2/4 wire conversion. In addition, an uncommited op amp is included in the SLIC-LC either for external connection of a balance network or for any other application.

FUNCTIONAL DESCRIPTION

Shown in Fig. 1 is a typical line circuit configuration using the SLIC-LC (HC-5501).

Balanced DC Battery Feed with Loop Current Limiting and Power Denial

The SLIC-LC provides DC loop current to the two wire side to provide power to the end instrument in the off-hook state and for loop monitoring purposes. Furthermore, this battery feed is balanced so that the tip to ground impedance is the same as the ring to ground impedance. To minimize power dissipation, the SLIC-LC provides a maximum of 30mA loop current under worst case conditions (V_{B-} = -58 volts, R_{Loop} = 200Ω). This is accomplished by a loop current limiting circuit within the SLIC-LC device. The tip feed (TF) and the ring feed (RF) outputs are low impedance and require two external series 300Ω ±1% resistors (HC-5501) or four external 150Ω±1% resistors (HC-5502) that limit current to the secondary protection bridge during overvoltage surges and present a 600Ω impedance to the loop. Both these resistors are to be matched within 0.1% for specified longitudinal balance.

If ILoop is less than 30mA, the $R_{Loop} = \frac{40V}{I_{Loop}}$ -600Ω. In this case, voltage at RF = -44V for a typical -48V operation. If R_{Loop} is less than 733 Ω and the supply voltage is -48V, then voltage at RF will move towards ground to maintain the maximum loop current at 30mA.

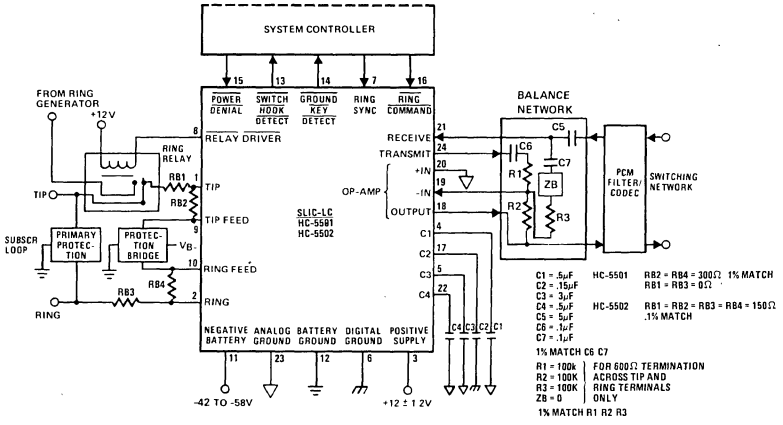


Figure 1 – Typical Line Circuit Application with the Monolithic SLIC

8

SLIC-LC offers selective denial of power to subscriber loops. When a logic level 0 is applied to the power denial ($\overline{PD}$) Terminal, the following events occur:

- Metallic loop current is limited to a maximum of 2mA.
- The loop monitoring functions described later are not necessarily valid.
- It is not possible to apply ringing voltage to the loop (across tip and ring).

Overvoltage Protection and Longitudinal Current Rejection

The SLIC-LC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

Table 1

PARAMETER	TEST CONDITION	PERFORMANCE (MIN)	UNITS
Longitudinal Surge	10μs Rise/ 1000μs Fall	± 1000 (Plastic) ± 800 (Ceramic)	V Peak V Peak
Metallic Surge	10μs Rise/ 1000μs Fall	± 1000 (Plastic) ± 800 (Ceramic)	V Peak V Peak
T/GND, R/GND	10μs Rise/ 1000μs Fall	± 1000 (Plastic) ± 800 (Ceramic)	V Peak V Peak
60Hz Current			
T/GND, R/GND	700V rms Limited to 10A rms	11	Cycles

The SLIC-LC will withstand longitudinal currents up to a maximum of 30mA rms without any performance degradation.

Ring Injection and Ring Trip Detection with Hardware Interlock

Ring Injection is accomplished by a ring relay external to the SLIC-LC device. The SLIC-LC device has an open collector relay driver output ($\overline{RD}$) capable of sinking 62mA current for control of this ring relay. Furthermore, the device has a low active ring command ($\overline{RC}$) input (TTL compatible) which activates the ring relay unless the subscriber is off hook ($I_{Loop} > 10mA$) or the SLIC-LC is in the power denial state ($\overline{PD}$) < 0.8 volts. This hardware interlock feature, prevents inadvertent ringing of the phone in the off-hook or power denial conditions.

In order to preserve the ring relay contacts and minimize RFI, the ($\overline{RD}$) output is only permitted to change state at or near the zero voltage crossings of the ring voltage signal. A TTL compatible ring sync (RS) input synchronized with ring voltage is applied to implement this feature.

Ring trip detection is also performed by the SLIC-LC device. If the subscriber goes off-hook during ringing, the $\overline{RD}$ output becomes inactive within 3 ring voltage cycles after this event occurs.

Loop Monitoring (Switch Hook and Ground Key Detection)

The SLIC-LC is able to monitor DC conditions associated with the loop (i.e. tip and ring) in order to determine end instrument status, transmit dialing pulses, and detect line fault conditions.

The SLIC-LC device provides the following low active TTL compatible logic outputs which indicate loop status:

- Switch Hook Detection ($\overline{SHD}$) – This output becomes active for loop currents exceeding 10mA and becomes inactive for loop currents less than 5mA.
- Ground Key Detection ($\overline{GKD}$) – This output becomes active when the DC current flowing into the ring lead (I_{RING}) exceeds the current flowing out of the tip lead ($-I_{TIP}$) by more than 17.5mA, and becomes inactive when this current difference is less than 10mA. This function can be used for monitoring calibrated ground key signals or sustained unbalanced output shorts.

Hybrid Function

Conversion of bidirectional signals from 2 wire telephone lines to separate receive and transmit signals is accomplished with this SLIC-LC device. Key features are:

- With extend resistors as specified, a balanced DC and AC impedance of 600Ω appears across tip and ring terminals.
- Longitudinal balance (2 wire) in excess of 60dB. A measure of degree of matching of tip to ground and ring to ground impedance.
- Longitudinal balance (4 wire) in excess of 50dB. A measure of common mode rejection capability of the device.
- Low frequency longitudinal current suppression – operational capability in presence of large common mode current at power line frequencies.
- Low idle channel noise.
- Level linearity over 60dB dynamic range.
- Overload level to accommodate maximum speech power level.
- Good transhybrid loss (i.e. rejection of receive signals leaking through to transmit side) capability in conjunction with appropriate balancing network. As shown in Fig. 1, external passive components and internal uncommitted op amp make up the balance network.

The impedance Z_B can be made to balance any loop impedance. Parameters of the balance impedance can be calculated by knowing the loop termination Z_L and from the following equation: $Z_B = \frac{K}{2} Z_L$

(K is a scale factor and this function allows the user to scale the balance impedance components to practical values. K = 100 is recommended for most applications.)

Values of other components in balance network are: C5 = 0.5μF, C6 = 0.1μF, C7 = 0.1μF, $R_1 = R_2 = K \times 600$ ohms, $R_3 = K \times 300$ ohms.

- Minimum delay in transmitting signals through the device.
- Capacitors C1 through C4 help provide filtering and time delay functions.

BLOCK DIAGRAM DESCRIPTION

In the SLIC-LC block diagram Fig. 2, the Receive (RCV) signal and -4V are summed and buffered to TF, they are negatively summed with VB- and buffered to RF, providing an open circuit DC feed of -4V and -44V for a VB- of -48V. Since the RCV signal appears in opposite phase between TF and RF, the 4/2 wire insertion loss is 0dB if Z_L = RBF1 + RBF2.

The transversal loop currents appear in voltage form at the output of summer 3 (VTRAN) which is also the transmit (Tx) output. The VTRAN signal is sensed by the switch hook detection circuit which signals the logic when transversal loop currents exceed 7.5mA. In addition, the VTRAN signal is monitored by the ITRAN limit circuit, which can modify the DC component of RF through summer 2 by adjustment of I1 through R. This limits the DC transversal current to a maximum value of 30mA, which also limits maximum power dissipation.

Longitudinal loop currents appear in voltage form at the output of summer 4 (VLONG) which provides input for the ring trip and ground key detection circuit. Undesirable power line induced longitudinal currents of up to 30mA rms are suppressed by an external capacitor (C4) which may delay ring trip detection by up to 3 ring cycles.

Power Denial is accomplished by setting I1 so that the voltage at RF is -4V. Power dissipation during line shorts to ground is limited by the thermal limiting circuit, which supplies I2 to force the voltage at RF positive. This limits die temperature by reduction of the short circuit current.

SLIC-LC (HC-5501) PIN DESCRIPTIONS (Refer to Fig. 3)

Pin 1 – T

This is an analog input which is connected to the TIP (more positive) side of the subscriber loop through the ring relay. It is used in conjunction with the ring lead to receive voice signals from the telephone and for loop monitoring purposes.

Pin 2 – R

This is an analog input which is connected to the RING (more negative) side of the subscriber loop. It is used in conjunction with the tip lead to receive voice signals from the telephone and for loop monitoring purposes.

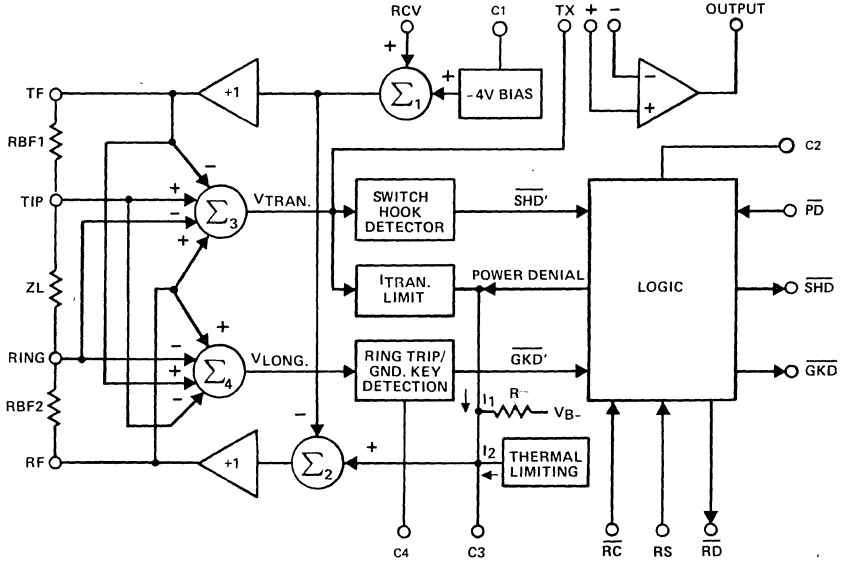


Figure 2 – SLIC-LC (HC-5501) Block Diagram

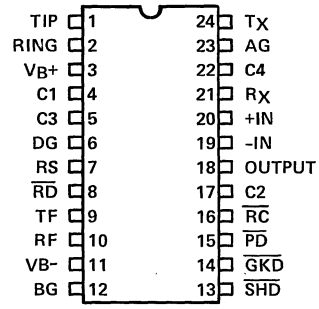


Figure 3 – Pin Configuration

Pin 3 – V_B+ (Positive Voltage Source)

Most positive supply. V_B+ is typically 12 volts with an operational range of 10.8 to 13.2 volts.

Pin 4 – C1 (Capacitor #1)

An optional external capacitor can be connected between this terminal and analog ground to further suppress noise appearing on the +12V supply. Typical value of this capacitor is 0.5 μF, 5V. If this pin is unused it should be left open.

Pin 5 – C3 (Capacitor #3)

An external capacitor is to be connected between this terminal and analog ground. This capacitor is required for proper operation of the loop current limiting function, and for filtering the -48V supply. Typical value of this capacitor is 0.3μF, 30V.

Pin 6 – DG (Digital Ground)

This is to be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC device.

Pin 7 – RS (Ring Synchronization Input)

This is a TTL compatible clock input. The clock is arranged such that a positive transition occurs on the negative going zero crossing of the ring voltage source. This ensures that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If this feature is not required, then this pin may be left open or tied to +5V.

Pin 8 – $\overline{RD}$ ($\overline{Relay\ Driver}$)

This a low active open collector logic output. When enabled, the external ring relay is energized.

Pin 9 – TF (Tip Feed)

A low impedance analog output which is connected to the tip lead through a 300 ohm ±1% feed resistor. It is used in conjunction with the ring feed lead to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.

Pin 10 – RF (Ring Feed)

A low impedance analog output which is connected to the ring lead through a 300 ohm ±1% feed resistor. It is used in conjunction with the tip feed lead to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.

Pin 11 – V_B- (Negative Voltage Source)

Most negative supply. V_B- is typically -48 volts with an operational range of -42 to -58 volts. This supply is frequently referred to as "battery".

Pin 12 – BG (Battery Ground)

To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.

Pin 13 – $\overline{SHD}$ ($\overline{Switch\ Hook\ Detection}$)

A low active TTL compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop current less than 5mA.

Pin 14 – $\overline{GKD}$ ($\overline{Ground\ Key\ Detection}$)

A low active TTL compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 17.5mA, and disabled if this current difference is less than 10mA.

Pin 15 – $\overline{PD}$ ($\overline{Power\ Denial}$)

A low active TTL compatible logic input. When enabled the metallic loop current is limited to a maximum 2mA, the switch hook detect ($\overline{SHD}$) and ground key detect ($\overline{GKD}$) are not necessarily valid, and the relay driver ($\overline{RD}$) output is disabled.

Pin 16 – $\overline{RC}$ ($\overline{Ring\ Command}$)

A low active TTL compatible logic input. When enabled, the relay driver ($\overline{RD}$) output goes low on the next rising edge of the ring sync (RS) input, as long as the SLIC is not in the power denial state ($\overline{PD}$ = 0) or the subscriber is not already off-hook ($\overline{SHD}$ = 0).

Pin 17 – C2 (Capacitor #2)

An external capacitor can be connected between this terminal and digital ground. This capacitor prevents false ground key indications from occurring during ring trip detection and may be omitted if $\overline{GKD}$ is not used. Typical value of this capacitor is 0.15 μF, 10V.

Pin 18 – OUTPUT

The analog output of the spare operational amplifier.

Pin 19 – -IN

The inverting analog input of the spare operational amplifier.

Pin 20 – +IN

The noninverting analog input of the spare operational amplifier.

Pin 21 – Rx (Receive Input, Four wire side)

A high impedance (90kohm) analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the tip feed and ring feed terminals, which in turn drive tip and ring through the 300 ohm feed resistors.

Pin 22 – C4 (Capacitor #4)

An external capacitor is to be connected between this terminal and analog ground. This capacitor prevents false ground key indications from occurring when large longitudinal currents are induced into the subscriber loop form near proximity power lines and other noise sources. Typical value of this capacitor is 0.5μF, 20V).

Pin 23 – AG (Analog Ground)

To be connected to zero potential and serves as a reference for the transmit output (Tx) and receive input (Rx) terminals.

Pin 24 – Tx (Transmit Output, Four wire side)

This is a low impedance (10Ω max) analog output which represents the differential voltage across tip and ring. Transhybrid balancing must be performed (using the spare op amp of the SLIC device) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.

HARRIS

APPLICATION NOTE

534

ADDITIONAL INFORMATION ON THE HI-300 SERIES SWITCH

BY CARL WOLFE

INTRODUCTION

The introduction of the HI-300 series of CMOS analog switches is the latest addition to the HARRIS switch family and gives the designer a viable second source to the Siliconix DG 300 series analog switch.

This family of monolithic, dielectrically isolated, CMOS analog switches consists of twelve products, the HI-300 thru HI-307 and the HI-381 thru HI-390 are designed for TTL level compatibility (logic "0" = .8V, logic "1" = 4.0V). The HI-304 thru HI-307 are CMOS compatible (logic "0" = 3.5V, logic "1" =11V).

The HI-300 series features low and nearly constant on resistance over analog signal range, low leakage and minimal power dissipation.

IMPROVED PERFORMANCE

An understanding of what a designer would consider important in an analog switch is useful in order to illustrate the advantage of the HI-300 series. Although any parameter could be considered important for a particular application, there are certain parameters considered to be most critical for the majority of applications. These parameters are:

"on" Resistance (Ron)
leakage current (I_{SOFF}, I_{DOFF}, I_{DON})
switching speed (ton, toff)
power supply current (I+, I-)

These parameters are important because the majority of designs require either high accuracy, speed, or low power dissipation.

ON RESISTANCE

In high accuracy systems, such as data acquisition systems, the designer would be concerned with minimizing errors caused by "on" resistance and leakage currents. An inverting programmable gain amplifier shown in Figure 1 will help illustrate the need for low on resistance and leakage current in high accuracy systems.

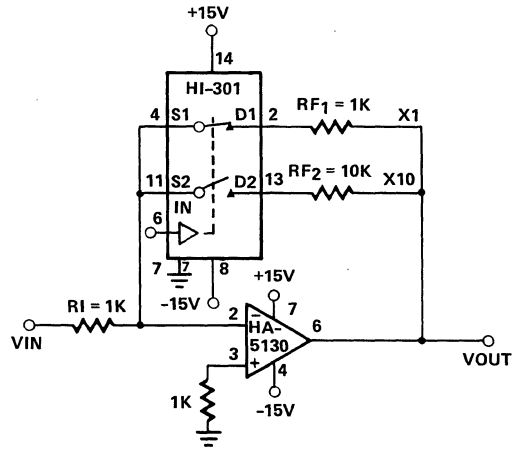


Figure 1 — Inverting Programmable Gain Amplifier

Ideally, the voltage gain of this inverting amplifier would be, $A_V = -(R_F/R_I)$. But when using a switch to program the gain, its characteristics must be taken into account and the amplifier gain equation must be modified to $A_V = -(R_F + R_{ON}/R_I)$. The higher the on resistance of the switch, the greater the gain error. Variations in the on resistance of the switch will also effect the gain error.

LEAKAGE CURRENT

Another source of error occurs in the switch "off" state, where leakage current causes offset voltage errors. In Figure 1 , leakage current flowing through the feedback resistor creates an output voltage error equivalent to the expression, $V_O = R_F \times I_{DOFF}$.

SWITCHING SPEED

A designer concerned with switching times would

8

obviously be sensitive to the ton and toff specifications. A low value of "on" resistance is also important, since this resistance increases the RC time constants and can slow the circuits overall performance.

POWER SUPPLY REQUIREMENTS

The last critical parameter would be power consumption. There are certain applications where power supply currents are the primary concern of the designer. Examples would be portable or battery operated equipment.

The majority of switch applications require critical performance in one or more of the areas just discussed. The HI-300 series offers improved performance in each of these areas. The following tables compare the HI-300 series with existing HARRIS switches. Table 1 contains maximum specifications for T = 125°C and Table 2 consists of typical values at T = 25°C.

+125°C Maximum Specifications

SWITCH TYPE	RON	I LEAKAGE	I SUPPLY	tON	tOFF
HI-200	125Ω	500nA	2mA	500ns	500ns
HI-5040	75Ω	500nA	.3mA	1000ns	500ns
HI-300	75Ω	100nA	.1mA	300ns	250ns

Table 1 — Switch Comparisons at T=125°C

+25°C Typical Specifications

SWITCH TYPE	RON	I LEAKAGE	I SUPPLY	tON	tOFF
HI-200	55Ω	1nA	.5mA	240ns	330ns
HI-5040	25Ω	.8nA	.3mA	370ns	280ns
HI-300	30Ω	.1nA	.23μA	210ns	160ns

Table 2 — Switch Comparisons at T=25°C

From these tables it should be clear that the HI-300 series offers improved performance to the designer.

INSIDE THE HI-300

Figure 2 shows the schematic of the digital input and driver stages of the HI-300. The purpose of this stage is to take the logic level signals and condition them to drive the gates of the FET switch cells.

The HI-300 series has a digital input protection circuit consisting of a 200Ω series resistor and clamping diodes, D1 and D2, to the supplies.

These diodes will quickly discharge any static charge which might appear at the digital inputs.

The F. E. T. Devices N1 thru N5 and P1 thru P5 form the input buffer and level shifter which establishes the proper voltages to drive the switch cell. N6, N7, P6, and P7 form the output buffers which isolate the level shifter from the capacitive load of the switch cell.

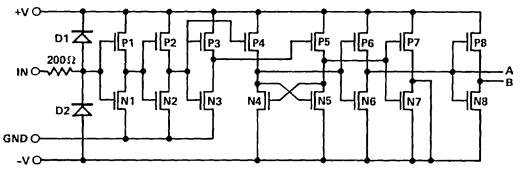


Figure 2 — Partial Schematic

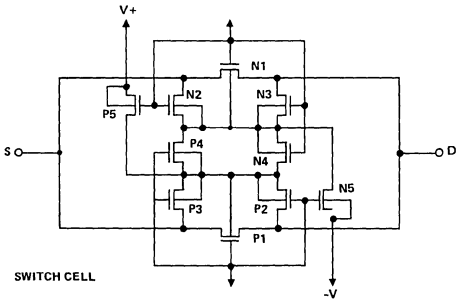


Figure 3 — Schematic

The switch cell shown in Figure 3 is based on the FET devices N1 and P1. The remaining devices, N2 thru P5 serve various functions, such as reducing leakage current, minimizing on resistance variations and minimizing charge injection.

ADDITIONAL PERFORMANCE CHARACTERISTICS

(A) SINGLE SUPPLY OPERATION

The HI-300 series has the capability of single supply operation. These switches can operate to a minimum supply of +5 volts, although designers must be aware of the trade off which exists at these levels. The trade off is the performance of the switch will vary as the supply level varies. Examples of these performance variations are increased on resistance and slower switching times. So, a HI-300 series switch with a single five volt supply will have higher on resistance and slower switching speeds then the same device at ±15 volts or even a single +15 volt supply.

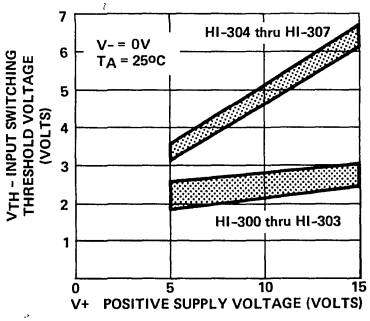
The explanation for these variations can be found in the F.E.T. devices composing the switch cell itself. The variation in on resistance is due to the fact that the channel impedance of the FET is dependent on the gate-source bias. Since the gate voltage is determined by the supply voltage, it can be concluded that the on resistance is a function of the supply voltage.

The fact that the on resistance varies with supply voltage directly relates to the slower switching times. The higher resistance reduces the available current

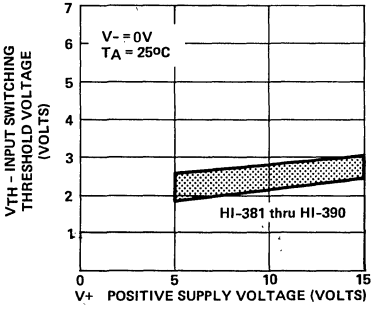
needed to charge the internal capacitances of the switch. Lower charging current directly relates to the slower switching times.

The explanations, just given, along with the following typical curves of the HI-300 single supply operation, should aid the designer in applying the HI-300 series in single supply applications.

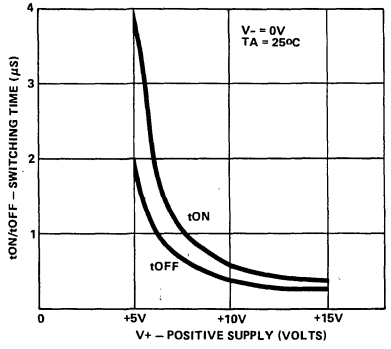
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-300 THRU HI-307



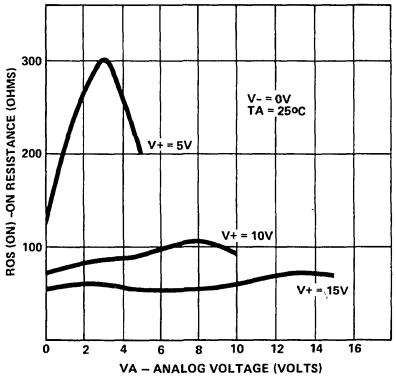
INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-381 THRU HI-390



SWITCHING TIME VS. V+ - POSITIVE SUPPLY VOLTAGE



RDS(ON) VS. ANALOG AND POSITIVE SUPPLY VOLTAGE WITH V- = 0V



B) CHARGE INJECTION

The charge injection of a switch is a critical parameter for certain applications, such as small signal switching or sample and hold circuits.

For the case of small signal switching, unwanted switching spikes result from this transferred charge causing system errors. These spikes are created when the transitions of the gate voltage are capacitively coupled to the output through the gate to source and gate to drain capacitances, as shown in Figure 4. The magnitude of these switching spikes will depend on the values of the load and source impedances, the value of the gate voltage and the size of the internal capacitances of the switch.

For the sample and hold circuit, shown in Figure 5, a common problem is sample to hold offset error. It is caused by the same mechanisms discussed for the small signal application, but in this case the charge is transferred to the hold capacitor and an offset voltage is created. The voltage is determined by the following relationship. $V = Q/CH$.

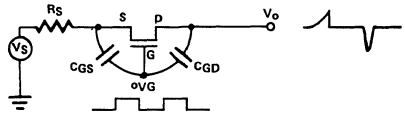


Figure 4 — Charge Transfer

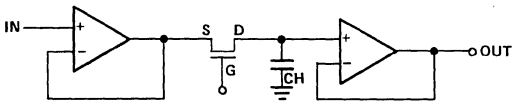


Figure 5 — Sample and Hold

Charge injection can create problems in the type of applications just described. A typical curve of the HI-300 series charge injection performance is shown in Figure 6 as an aid to designing in these type of circuits.

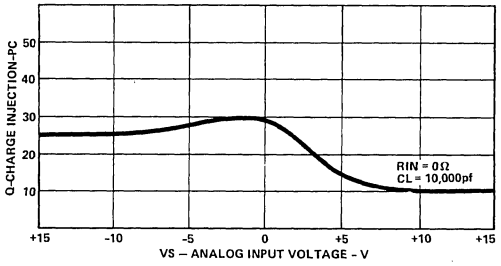


Figure 6 — Charge Injection vs. Input Voltage

APPLICATION HINTS

A\ POWER SUPPLY CONSIDERATIONS

The HI-300 series analog inputs do not feature overvoltage protection. External protection circuitry would be necessary if the switches were subjected to possibly destructive situations.

An example could be an overvoltage condition where the power supplies to the switch go down while an analog input signal is still present. A common misunderstanding is that the switch will be open and block the input signal, when actually the opposite occurs.

If the power supplies go to ground, the input signal will pass through the switch and appear at the output. The explanation for this can be seen in Figure 7, which is a simplified CMOS switch cell. This switch cell consists of two enhancement type field effect transistors, one N-channel and one P-channel. An enhancement type of device is a FET which is normally off without some potential (gate voltage) to turn it on. A P-channel FET requires a negative potential (gate to source voltage) to turn it on an N-channel FET requires a positive potential (gate to source). Contained in the physical structure of the FETS are parasitic transistors which are shown in Figure 7 as diodes from the source and drain to the body potentials of the devices. These diodes or parasitic junctions are normally reversed biased. If those junctions are forward biased, a fault condition exists where the signal is passed through the parasitic transistor. This is what occurs if the power supplies go to ground. Depending on the polarity of the input signal, either the N or P channel FET parasitics will be forward biased and the signal passed through the switch.

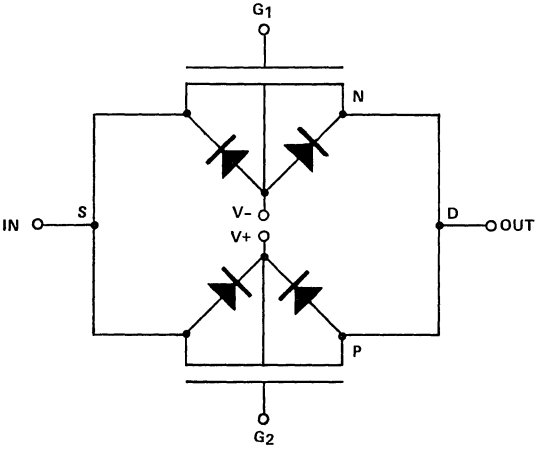


Figure 7 — Basic CMOS Transmission Gate

Another situation occurs if the power supplies are open circuited, the most positive and negative input signals will provide power to the switch. In this case, the signals being used for power will be passed to the output, but the remaining switches with input signals less than those used for supply will operate properly.

A second overvoltage condition is the case where the input signals exceed the existing power supply levels. Referring to Figure 7, if the input signal exceeds the supply by an amount greater than the breakdown voltage of the parasitic junction, the normally reversed biased junction will become forward biased. These forward biased junctions will pass the input signals to the output and possibly short out the input voltage sources.

The most common form of protection circuit for these types of overvoltage conditions is the resistor-diode network at the input of the switch as shown in Figure 8. This circuit protects the device if the supplies go to ground or if the input exceeds the supply. If either of these situations occur, the diodes will be forward biased and a current path to ground will exist. This protects the switch from excessive current levels. The primary purpose of the resistor is to limit the current through the diodes.

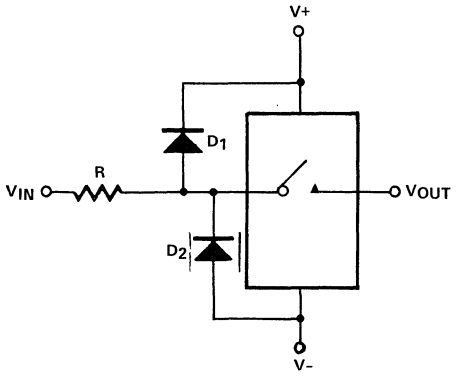


Figure 8 – Protection for Each Analog Input

Another advantage of using diode protection is that it prevents the signal from passing to the output. This is a result of the input being clamped to the breakdown voltage of the protection diodes. If this breakdown voltage is less than the threshold voltage (turn on voltage) of the parasitic diodes, the parasitic transistor will remain reversed biased and the signal will not pass through the switch.

The protection network may introduce unwanted error into the circuit in the form of leakage current and increased on resistance. It is recommended that low leakage diodes be used, such as Schottkey diodes. If the switch is looking into a high impedance, such as the input operational amplifier, the error introduces by the increased on resistance will be negligible.

The protection circuit just discussed is not used to prevent the switch from latch up. The HI-300 series switch is constructed using the HARRIS dielectric isolation process and the four layer SCR found in JI technology does not exist. This circuit is intended to protect the device from high current levels which result from the forward biasing of the parasitic transistors which are inherent in all FETS.

An alternative to protection circuits takes advantage of CMOS technology. Assume an overvoltage condition exists where the input exceeds supply. Rather than use external components to protect the device, it may be possible to shift the supplies in order to accomodate the input signal. An example would be an application with ±15 volt supplies, but attempting to switch a +18 volt input signal. A possible solution would be to shift the supplies to V+ = +20V and V- = -10V and now the input signal is within the existing supplies. In some applications the supply voltage can be adjusted in order to pass larger input signals.

ACKNOWLEDGEMENT

A. Engineering staff of Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901, particularly Frank Cooper, whose useful comments contributed to this publication.

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(2) Don Jones, "CMOS Analog Multiplexers and Switches' Applications Considerations" Harris Application Note 520.

(3) Ernie Thibodeax, "Getting the most out of C-MOS devices for analog switching jobs", Harris Application Note 521.

(4) Hunter, Bill, CMOS DATA BOOK: Tab Books, 1978.

HARRIS

APPLICATION NOTE 535

DESIGN CONSIDERATIONS FOR A DATA ACQUISITION SYSTEM (DAS)

BY TARLTON FLEMING

INTRODUCTION

This is a collection of guidelines for the design of a data acquisition system. Its purpose is to supplement the more methodical block-by-block discussions available in numerous other papers and application notes. Emphasis in this note is on the less easily quantifiable happenings "between the blocks", rather than a description of the block components and their error contributions. This latter information may be found in the Bibilography under "General".

A data acquisition system is defined to include all the components needed to generate the electrical analogs of various physical variables, transmit these signals to a central location and digitize the information for entry into a digital computer. Among these components are transducers, amplifiers, filters, multiplexers, sample/holds and analog-to-digital converters. The system also includes all signal paths tying these functions together.

Several system architectures will be considered, followed by a general discussion aimed at the designer who must choose hardware for a given application. Topics include:

- Data Acquisition System Architecture
- Signal Conditioning
- Transducers
- Single-Ended vs. Differential Signal Paths
- Low-Level Signals
- Filters
- Programmable Gain Amplifier
- Sampling Rate
- Computer Interface

DATA ACQUISITION SYSTEM ARCHITECTURE

At present the most widely used DAS configuration is that shown in Fig. 1. It handles a moderate number of analog channels, feeding into a common multiplexer, programmable gain amplifier (if required), track/hold amplifier and A-D converter.

A more specialized and expensive variation is to place a Track/Hold in each channel as shown in Fig. 2. Switching all channels to HOLD simultaneously produces a "snapshot" view which preserves the phase relation of signals in all channels. This information is important in seismic studies and vibration analyses.

The DAS system of Fig. 3 offers many advantages, but is not yet practical except for slowly changing channel data. Low frequency signals allow dedication of a slow but accurate integrating type A-D converter for each channel. The channel filters often included to reduce aliasing errors and noise are not necessary, since aliasing is not a problem with low bandwidth signals. The integrating converter suppresses wideband noise by averaging it about the instantaneous signal level. Also, the converter's integration period may be chosen to provide almost complete rejection of a specific interference frequency such as 60 Hz. Digital outputs from the converters are then digitally multiplexed.

The system shown in Fig. 3 has an inherent advantage over the other two systems, having eliminated both the track/hold and the analog multiplexer with their many error contributions. The disadvantage, of course, is cost. Fig. 3 would become the system of choice in many more applications, if a significant reduction should occur in the price of successive - approximation A-D converters.

A small RAM may be added at the converter's output in any of these systems, to buffer the computer and offload its involvement with individual conversions. Timing and control may be arranged to scan all channels repeatedly, and continuously update a RAM location for each channel. The computer is then free to look at a recent reading for any channel, at any time.

Further discussion will center on Fig. 1, both in the single-ended version shown, and in the differential version.

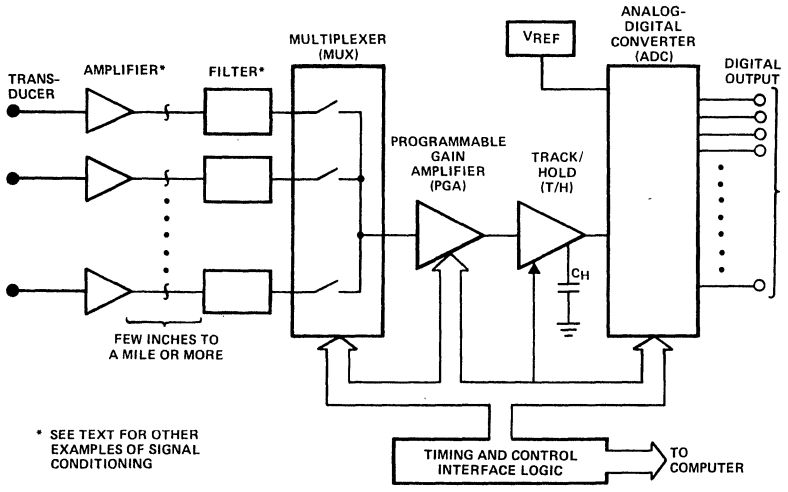


FIGURE 1. Typical Data Acquisition System

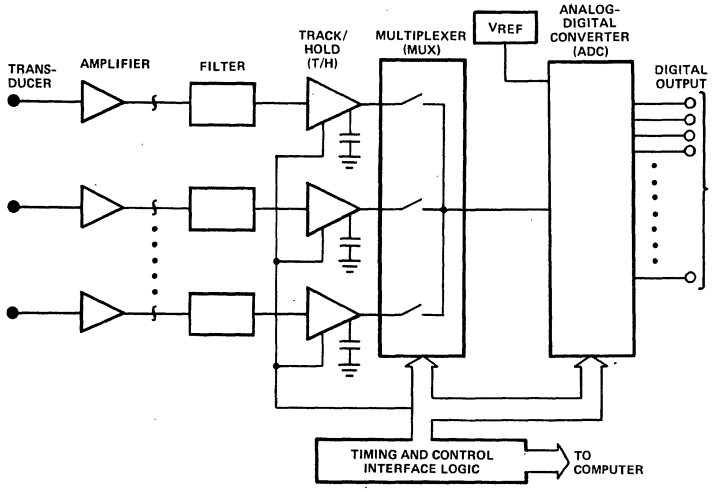


FIGURE 2. DAS System For Simultaneous Sampling Of All Channels

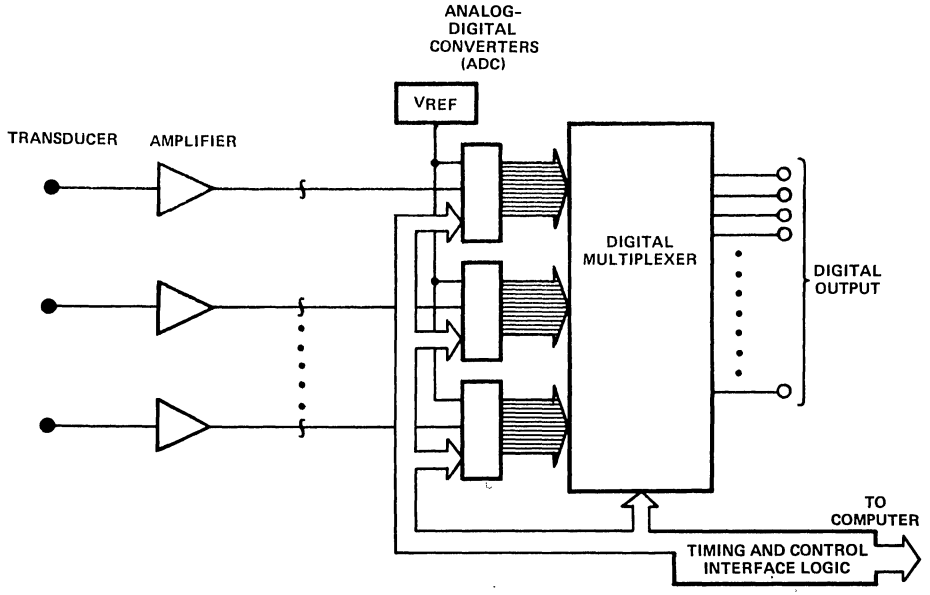


FIGURE 3. High Accuracy, Multi-Converter DAS System

SIGNAL CONDITIONING

Signal conditioning refers to all the operations performed on a transducer signal up to (and including) digitization by the A-D converter. Standard among these operations are multiplexing, programmable gain, and Track/Hold. Others may be added as required:

- Transducer excitation
- Amplification
- Filtering
- Calibration
- Linearization
- Voltage to current conversion (4 to 20 mA; 10 to 50 mA)
- rms to dc conversion
- Logarithmic signal compression
- Common mode rejection

For highest signal-to-noise ratio all signal conditioning should be performed near the transducer, with the exception of common mode rejection and filtering. Filters should be located near the multiplexer input. Besides minimizing alias errors originating in the high end of the transducer's output spectrum, filters suppress wideband noise picked up on signal lines to the transducer.

TRANSDUCERS

The first item in the signal path of a DAS is the transducer. This device usually transforms energy from one form to another, producing an electrical analog of the physical variables to be monitored or measured. Transducers are based on a variety of physical principles but most produce a voltage as output. Some yield an intermediate variable such as resistance or capacitance, which is transformed to voltage by an applied electrical excitation (carrier frequency, dc voltage, current source).

Often, several types of transducers are available to sense a given quantity. When selecting a voltage output transducer, remember that a low source resistance is desirable, both to minimize noise and to reduce loading by the next "block" in the signal path. Provision on the transducer for a convenient method of signal calibration will be welcome, once a system is in operation. Also, a center tap on the transducer allows better interface to a balanced line if low level signals are to be transmitted.

Several questions arise at this point:

- Should the signal path be single-ended or differential?
- Should the signal be transmitted at low level (100 mV) or high level?
- What type of conductor should be used for signal transmission?

Answers to these and other questions are covered in the following Sections.

SINGLE-ENDED VS. DIFFERENTIAL SIGNAL PATHS

Consider the transducer output. A high level signal (100 mV to 10 V) is easier to handle than low level. Is a common mode signal present? If not, is it likely to be acquired as "pickup" during transmission? This is likely if the cable is routed near fluorescent lights, motors or other electrical machinery. If common mode voltage is not expected, then an economical single-ended connection is possible, with a single wire per channel and a common return. (see Fig. 4). High level signals, short distance and controlled conditions will ensure good performance with this arrangement.

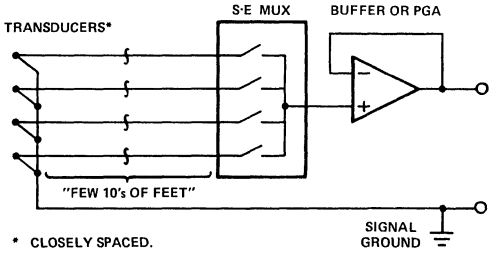


FIGURE 4. Single-ended Data Paths

Low level signals require special treatment. Whether high or low level, the presence of common mode voltage calls for a differential signal path. The most widely used solution is an unshielded, twisted pair of wires, good for 1000 feet or so with a bandwidth of 100 KHz. As a minimum then, two wires per channel feed into a differential amplifier or multiplexer, buffered by a full or pseudo-differential amplifier to reject the unwanted common mode voltage (see Fig. 5).

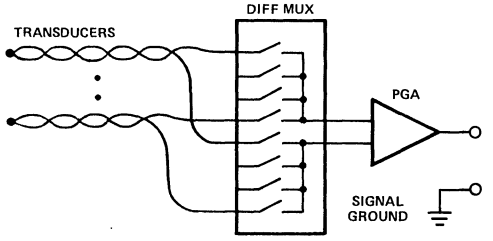


FIGURE 5. Differential Data Paths

For the case in which the transducer output is a low level voltage, the choice is whether to transmit it as is, or to boost the level by adding an amplifier. The amplifier will provide low source impedance as well as gain; two valuable forms of signal conditioning. However, providing power to a remote amplifier can be difficult. Even if a supply is available at the remote site, the voltage between two widely separated commons presents a problem. If the sum of signal plus common mode voltage does not exceed the input range of either the multiplexer or buffer amplifier, Fig. 5 can be used.

A more expensive approach is required for higher common mode voltages. One reliable technique is the "flying capacitor" multiplexer of Fig. 6, using reed relay switches. This works well for thermocouples bonded to machinery and riding on hundreds of volts relative to DAS ground, but in some applications the reed relay's 1 ms response time can be a limitation.

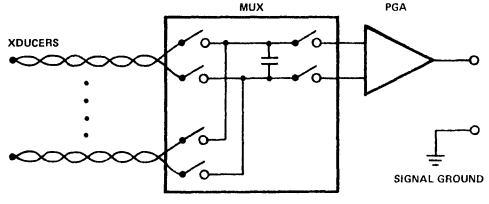


FIGURE 6. "Flying Capacitor" multiplexer using reed relay switches for high CMV signals.

Isolation amplifiers can handle higher voltages and higher bandwidths than the system of Fig. 6. For example, magnetically isolated amplifiers are rated at 2KV and up with a small signal bandwidth of approximately 2 KHz. One of these per channel is expensive, but in addition to common mode rejection it can solve the problem of supplying power at the remote transducer. Isolation amplifier models are available which include ±15V terminals, referenced to the floating front-end of the amplifier. This power can provide transducer excitation and supply an amplifier or other signal conditioning circuitry.

For higher bandwidth data, optically isolated isolation amplifiers are available with $f_{-3dB} = 15KHz$ and 2KV isolation. These amplifiers do not provide the external supply terminals to power transducer circuitry.

LOW LEVEL SIGNALS

The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded, differential signal path is essential for transmitting these signals, especially to maintain a noise level below 50μV rms.

Most transducer outputs are low level and low bandwidth as well. Since shielding precautions to be described are intended to produce an acceptable signal to noise ratio, filters may not be necessary. Otherwise, active filters with their relatively large dc errors should not be used for low level signals. Passive filters on the other hand, are restricted to two or three poles as a practical limit, which in turn restricts the allowable signal bandwidth for a given accuracy (see the Section titled Filters).

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area, to guard against pickup of electromagnetic interference, and the twisted pair should be shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only one tenth as much leakage capacitance to ground per foot.

A key requirement for the transmission cable is that it present a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled in-phase to both conductors and rejected as common mode voltage. Again, any such noise will be directly proportional to the source impedance driving the line. An isolation or instrumentation amplifier may be used to terminate the line, providing high input impedance, common-mode rejection, conversion from a differential to single-ended signal path, and a buffer for the ON resistance of the following multiplexer.

Coaxial cable is not suitable for low-level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few milliohms must be considered, especially to meet an accuracy requirement of 12-bits or more.

The table of Fig. 7 is a useful collection of data for calculating the effect of these short connections. (Proximity to a ground plane will lower the values for inductance.)

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 OZ. Cu.)	DC RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT AT 60Hz	IMPEDANCE PER FOOT AT 10KHz
18	0.47"	0.0064Ω	0.36μH	0.0064Ω	0.0235Ω
20	0.30"	0.0102Ω	0.37μH	0.0102Ω	0.0254Ω
22	0.19"	0.0161Ω	0.38μH	0.0161Ω	0.0288Ω
24	0.12"	0.0257Ω	0.40μH	0.0257Ω	0.0345Ω
26	0.075"	0.041Ω	0.42μH	0.041Ω	0.0488Ω
28	0.047"	0.066Ω	0.45μH	0.066Ω	0.0718Ω
30	0.029"	0.105Ω	0.49μH	0.105Ω	0.110Ω
32	0.018"	0.168Ω	0.53μH	0.168Ω	0.171Ω

FIGURE 7. Impedance of Electrical Connections, +20° C

As an example, suppose the ADC in Fig. 1 has 12-bit resolution, and the system accuracy is to be ± ½ LSB (± 1.2mV). The interface logic might draw 100 mA from the + 5V supply. Flowing through six inches of #24 wire, this current produces a drop of 1.28mV; more than the entire error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

FILTERS

The presampling or anti-aliasing filters shown in Fig. 1 are normally required with high-level signals of significant bandwidth, especially if the signal is to be reconstructed by a digital-to-analog converter after processing. If low level signals require a passive filter, the differential configuration of Fig. 8 preserves some degree of impedance balance on the line.

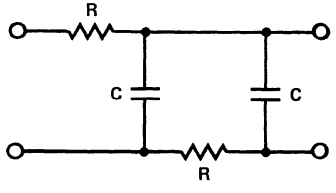
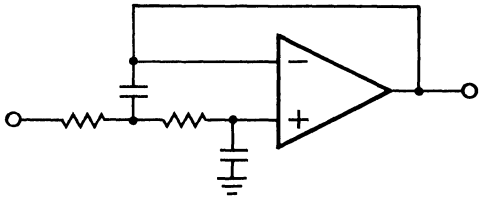


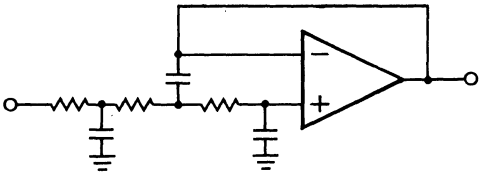
FIGURE 8. A Passive, Two Pole, Low Pass, Differential Input Filter

A low-pass Butterworth response is best for the channel bandlimiting filter in most data acquisition systems. The Butterworth filter output decreases monotonically with frequency, though this attenuation is very slight within the passband. Other filter types produce ripple in the passband, whose amplitude degrades accuracy unless expensive, high tolerance components are used.

Butterworth is not the most linear phase response, and if signal group delay is critical an elliptic (Bessel) filter should be chosen. Again, however, Butterworth fits most applications. A given number of poles may be had by cascading the two and three pole sections shown in Fig. 9. Either reference under "Filters" in the Bibliography gives a systematic procedure for calculating R and C values in terms of a given cutoff frequency. See the Section on "Sampling Rate" for the poles vs. accuracy requirement.



a. TWO POLE SECTION



b. THREE POLE SECTION

FIGURE 9. Butterworth Low-Pass Filters

PROGRAMMABLE GAIN AMPLIFIER (PGA)

Unless the ratio of highest to lowest signals anticipated on any channel is ≤ 2, some form of programmable gain amplification is desirable between the multiplexer and A-D converter. Without this variable gain block, the MSB's are idled one after another as input level decreases. Although the resolution of an n-bit converter remains a constant $FS/2^n$ by definition, resolution referred to the input level is decreasing (FS = Full Scale).

Considering resolution as referred to the input level, a 12-bit converter digitizes an input of .06FS to only 8 bits. The full 12-bit resolution applies only for $V_{IN} \geq FS/2$. Therefore to fully utilize the converter, gain should be added as necessary before each conversion, to meet the condition $FS/2 \leq V_{IN} \leq FS$. Then the amount of gain introduced by the PGA is noted by the computer to keep track of the actual input value.

Three other services are performed by the PGA:

1. Buffering: Prevents a loading effect due to the multiplexer's ON resistance.

2. Differential to Single-Ended Conversion: Necessary for the majority of Track (or Sample) /Holds and A-D converters.

3. Common Mode Rejection (CMR). When connected to the output of a differential multiplexer, the PGA's differential input rejects the common mode voltage accumulated by a signal transmission cable. Fig. 10 shows a subtractor or "pseudo-differential" PGA suitable for wideband signals with low common mode content. In this circuit, CMR is limited by precision of the "K" ratio and variations in the channel source impedance.

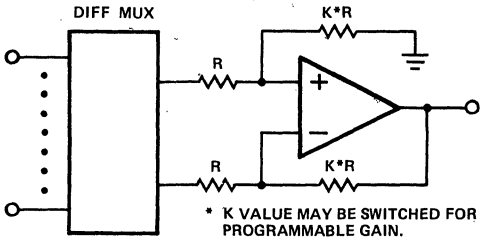


FIGURE 10. Subtractor or Pseudo-Differential PGA

Fig. 11 is the full differential PGA, necessary for low-level, high common mode signals. This version offers the highest gain accuracy and for high gain, the best CMR.

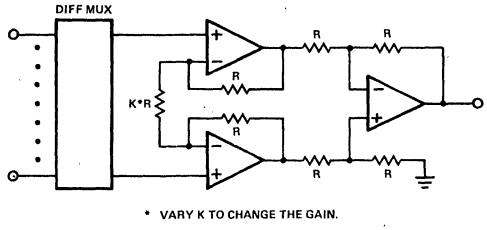


FIGURE 11. Full Differential PGA

The PGA normally precedes the Track/Hold, since the PGA would amplify any error introduced by that device. This order must be reversed to implement an auto-range capability, because the signal voltage must be held at the PGA input for the duration of an auto-range subroutine by the computer. Such an algorithm consists of:

- Set PGA gain
- Trigger a conversion
- Note RESULT
- Iterate until (FS/2 ≤ RESULT ≤ FS)

SAMPLING RATE

Throughput rate for a DAS may be defined as the maximum number of digital samples per second that it can produce without exceeding its specified limit for accuracy. The system may run at a lower speed to avoid generating redundant and useless data; but if a waveform of significant bandwidth is to be reconstructed from the digital samples, then "the higher the better" is generally the rule for sampling rate.

The required rate is often higher than one would suppose. For example, using the criteria of data bandwidth alone, a very low sample rate is required for the slowly changing voltage outputs from a solar panel. Once per minute for each channel might be enough. With 60 channels though, the rate required is once per second. In addition, one might require a maximum of one second for notice of failure on any channel, boosting the required sample rate to 60 samples per second. In this manner low bandwidth channels may require a high speed DAS, according to the relationship:

System Sample Rate = (Highest Channel Rate) X (Number of Channels)

Also, a very high sample rate is required to preserve the high frequency content of a transient event on a single channel. The most commonly encountered requirement though, is a multichannel DAS (see Fig. 1) with a modest bandwidth on each channel. For example, each data source might be an accelerometer with an output ranging through several hundred Hertz.

Notice that the low and high bandwidth signals just described cannot be handled efficiently with the same system. A sample rate high enough for the highest bandwidth channel will oversample the lower bandwidth channels, generating unnecessary data. High and low bandwidth data are best handled by separate multiplexer/converter systems.

Presampling filters are essential to ensure accuracy in the sequence of digital samples representing a given channel. Since the multiplexer is a sampler (as is the Sample/Hold and A-D Converter) this means a separate filter dedicated to each channel preceding the multiplexer. A single filter following the multiplexer would do the job, but its modest response time would form a bottleneck restricting the sample rate. Guidelines are needed then, to relate a given level of accuracy to data bandwidth, filter cutoff frequency, and number of filter poles.

As mentioned earlier, a filter limits the error due to alias frequencies by restricting the bandwidth of both signal and noise. Either acting alone or in concert may cause error, since alias frequencies arise in several ways:

1. Overlap of the signal spectrum and the lower sideband associated with the sampling frequency f_S.
2. Overlap of the upper and lower sidebands associated with any two consecutive harmonics of f_S.
3. Overlap of any sideband with wideband noise from the data channel.

A band-reject filter would control case 1, but a low-pass type is needed to handle cases 2 and 3 as well. Again, the Butterworth response is preferred in most applications, but it does offer increasing phase shift and gain error for frequencies approaching the cutoff (-3dB) frequency. This cutoff should be set no higher than necessary for acceptable gain error in the highest signal components. A higher cutoff will only include unnecessary noise bandwidth.

Finally, for a given accuracy specification such as ± ½ LSB, a tradeoff may be made between the sample rate and number of poles. These poles usually come from the filter, but the number may include any pole(s) inherent in the transducer, provided they occur at an acceptable location relative to the cutoff frequency.

Fig. 12 shows aliasing error due to the signal spectrum alone vs sampling rate for different numbers of poles. The horizontal axis is normalized to Sampling Frequency/Cutoff Frequency. Notice that a 2-pole filter requires a sampling frequency 30 times the filter cutoff frequency, just to obtain 1% accuracy. For ± ½ LSB error in a 12-bit system (± .01%), a 5-pole filter requires sampling at 11 times the cutoff frequency. Remember, Fig. 12 applies only to the signal spectrum. Noise will cause some additional aliasing error.

Clearly, Nyquist's Sampling Theorem is not a practical guide for sampling rate in real applications. Actual (as opposed to hypothetical) filters cannot bandlimit a signal sufficiently to permit the theoretical minimum of two samples per cycle of highest signal frequency.

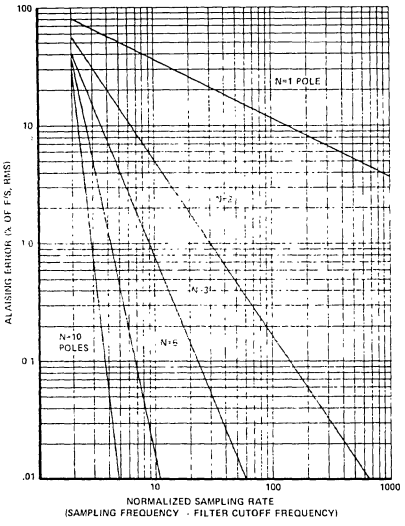


FIGURE 12. Effect of Filter Poles on Aliasing Error

COMPUTER INTERFACE

The typical DAS we have described (Fig. 1) requires several control signals:

- Mulitplexer Channel Address
- PGA Gain Address
- Track/Hold Control
- A-D Converter
  - Start Convert
  - MSB Invert
  - Short cycle
  - Unipolar/Bipolar
  - Output Byte Enable
  - Conversion Interrupt etc.

This control can be provided directly by the computer, but some portion of these signals is usually supplied by an intermediate block of control logic. For monitoring predictable channel data, the DAS can repeatedly scan through its channels, trigger the converter, and notify the computer when each data sample is ready. This independent operation can be accomplished by a clock and counter arrangement to supply channel and gain addresses, plus a dual "one shot" multivibrator (74123) to gate the Start Convert and Track/Hold functions.

To handle a sudden change in data level or other unexpected event, the computer must be able to random access any channel or PGA gain. Provision is made to write this information to the DAS via the computer's data or address bus, using appropriate address decoders and latches.

When processing higher bandwidth signals, one error source to be minimized is the Track/Hold's aperture delay uncertainty, or jitter. The logic which generates the T/H control signal needs close attention, since jitter in this waveform adds to that specified for the device itself.

Finally, the DAS output consists of a serial stream of parallel digital words from the converter, synchronized with the converter's status signal indicating when the data is valid. Techniques for passing this data to the computer include direct memory access (DMA), memory mapping, and mapping via a dedicated I/0 port, all with or without an external interrupt of the processor.

DMA is most efficient for the high speed transfer of large volumes of data. This can proceed by program request, resulting in the movement of a block of data to a designated sequence of memory locations, at a speed limited only by the memory cycle time. As an alternative, hardware can be configured to allow transfer of a data word during every non-memory machine cycle. This allows an almost continuous output of data from the DAS. The transfers are asynchronous and unsolicited by the program with only a slight increase in software execution time.

For less demanding data rates the choice is between an I/0 or memory mapped interface. The former is best for small systems. For example, the 8085 microprocessor can control up to eight I/0 devices without external address decoding. Addition of decoders expands the field from 8 to 256 peripherals.

There is a range of applications for which the choice of I/0 or memory mapping is not clear, but memory mapping becomes attractive with increasing system complexity. The memory reference instructions available with this approach simplify programming and speed execution. A further increase in throughput is obtained by use of the processor's interrupt system, allowing the main program to proceed while an analog-to-digital conversion is in progress.

Memory mapping plus interrupt is very effective; however, the software overhead associated with service of an interrupt-driven I/0 interface results in a diminishing advantage as the required throughput rate increases. Again, DMA offers the advantage for high data rates.

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HARRIS

APPLICATION NOTE 607

DELTA MODULATION FOR VOICE TRANSMISSION

BY DON JONES

INTRODUCTION TO DELTAMOD

Delta modulation has evolved into a simple, efficient method of digitizing voice for secure, reliable communications and for voice I/O in data processing.

To illustrate basic principles, a very simple delta modulator and demodulator are illustrated in Figure 1. The modulator is a sampled data system employing a negative feedback loop. A comparator senses whether or not the instantaneous level of the analog voice input is greater or less than the feedback signal. The comparator output is clocked by a flip-flop to form a continuous NRZ digital data stream. This digital data is also integrated and fed back to the comparator. The feedback system is such that the integrator ramps up and down to produce a rough approximation of the input waveform. An identical integrator in the demodulator produces the same waveform, which when filtered, reproduces the voice.

We can see that the digital data 0's and 1's are commands to the integrators to "go up" or "go down" respectively. Another way of looking at it is that the digital data stream also has analog significance; it approximates the differential of the voice, since analog integration of the data reproduces the voice.

Note that the integrator output never stands still; it always travels either up or down by a fixed amount in any clock period. Because of its fixed integrator output slope, the simple delta modulator is less than ideal for encoding human voice which may have a wide dynamic amplitude range.

The integrator cannot track large, high frequency signals with its fixed slope. Fortunately, human speech has statistically smaller amplitudes at higher frequencies, and an integrator time constant of about 1 millisecond will satisfactorily reproduce voice in a 3kHz bandwidth.

A more serious limitation is that voice amplitude changes which are less than the heighth of the integrator ramp during one clock period cannot be resolved. So dynamic range is proportional to clock frequency, and satisfactory range cannot be obtained at desirable low clock rates.

A means of effectively increasing dynamic range is called "companding" (compressing-expanding); where at the modulator, small signals are given higher relative gain, and an inverse characteristic is produced at the demodulator.

The CVSD: A popular effective scheme for companded delta modulation is known as CVSD (continuously variable slope deltamod) shown in Figure 2. Additional digital logic, a second integrator, and an analog multiplier are added to the simple modulator.

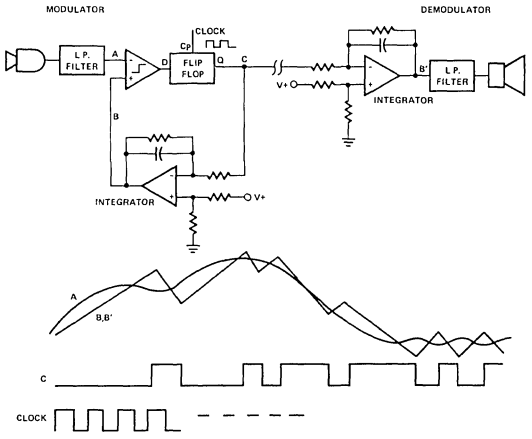
Under small input signal conditions, the second integrator (known as the syllabic filter) has no input, and circuit function is identical to the simple modulator, except that the multiplier is biased to output quite small ramp amplitudes giving good resolution to the small signals.

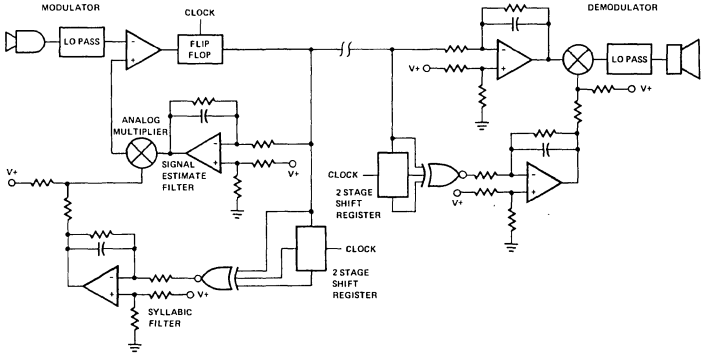
A larger signal input is characterized by consecutive strings of 1's or 0's in the data as the integrator attempts to track the input. The logic input to the syllabic filter actuates whenever 3 or more consecutive 0's or 1's are present in the data. When this happens, the syllabic filter output starts to build up, increasing the multiplier gain, passing larger amplitude ramps to the comparator, enabling the system to track the larger signal. Up to a limit, the more consecutive 1's or 0's generated, the larger the ramp amplitude. Since the larger signals increase the negative feedback of the modulator and the forward gain of the demodulator, companding takes place. By listening tests, the syllabic filter time constant of 4 to 10 milliseconds is generally considered optimum.

An outstanding characteristic of CVSD is its ability, with fairly simple circuitry, to transmit intelligible voice at relatively low data rates. Companded PCM, for telephone quality transmission, requires about 64K bits/sec data rate per channel. CVSD produces equal quality at 32K bits/sec. (However, at this rate it does not handle tone signals or phase encoded modern transmissions as well.)

CVSD is useful at even lower data rates. At 16K bits/sec the reconstructed voice is remarkably natural, but has a slightly "Fuzzy Edge". At 9.6K bits/sec intelligibility is still excellent, although the sound

is reminiscent of a damaged loudspeaker. Of course, very sophisticated speech compression techniques have been used to transmit speech at even lower data rates; but CVSD is an excellent compromise between circuit simplicity and bandwidth economy.





THE DIGITAL CVSD

Delta modulated data is in a form which can be digitally filtered with fairly simple circuitry. A compatible CVSD can be made using digital integrators and multipliers driving a digital-to-analog converter. The block diagram of the Harris HC-55516/55532 monolithic CVSD is shown in Figure 3.

The CMOS digital circuit functions of Figure 3 closely parallel the equivalent analog function in Figure 2. The filters are single pole recursive types using shift registers with feedback. A digital multiplier feeds a 10 bit R-2R DAC which reconstructs the voice waveform. The DAC output is in steps, rather than ramps.

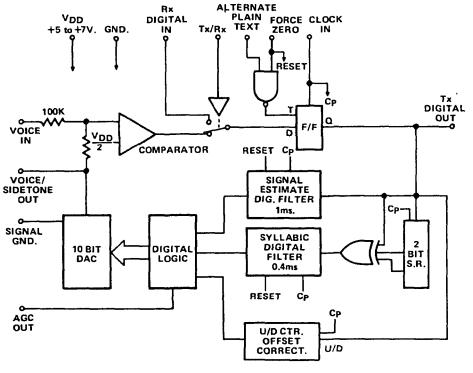


Figure 3 – HC-55516/55532 CVSD Functional Diagram

8

The digital CVSD has a number of advantages over its analog counterpart, and has desirable features which would otherwise require additional circuitry:

1) The all CMOS device requires only 1mA current from a single +4.5V to +7V supply.

2) No bulky external precision resistors or capacitors are required for the integrators; time constants of the digital filters are set by the clock frequency and do not drift with time or temperature.

3) For best intelligibility and freedom from listener fatigue, it is important that the recovered audio is quiet during the pauses between spoken words. During quiet periods, an alternate "1", "0" pattern should be encoded, which when decoded and filtered will be inaudible. Achieving this in the analog CVSD requires that up and down ramp slopes are precisely equal and that offsets in the comparator and amplifiers are adjusted to zero. Improper adjustment or excessive component drift can result in noisy oscillations. In the digital design, comparator offset and drift are adjusted by a long up-down counter summed to the DAC to insure that over a period of time equal numbers of 1's and 0's are generated.

   An added feature is automatic quieting, where if the DAC input would be less than 2 LSB's the quieting pattern is generated instead. This has proven to aid intelligibility.

4) To prevent momentary overload when beginning to encode or decode, it is desirable to initialize the integrators. In the analog CVSD, external analog switches would be required to discharge the capacitors.

   In the digital CVSD, the filters are reset by momentarily putting the "Force Zero" pin low. At the same time, a quieting pattern is generated without affecting internal encoding by putting the "Alternate Plain Text" pin low.

5) In some analog CVSD designs, transient noise will be generated during recovery from a low frequency overdriven input condition. The digital CVSD has a clipped output with instant recovery, when overdriven.

6) Half-duplex operation (using the same device, switching between the encode and decode functions) requires external circuits with the analog CVSD, while the digital type is switched internally by a logic input.

A possible drawback to the digital CVSD is that, since its filter time constants are proportional to the clock period, a single device will not be optimum for all clock frequencies. For this reason, Harris has two devices, the HC-55516 for clock rates below 24K bits/sec, and the HC-55532 for higher clock rates.

APPLICATIONS OF DELTA MODULATION

1) **Telecommunications:** Digitized signals are easily routed and multiplexed with low cost digital gates. Voice channels may be easily added to existing multiplexed digital data transmission systems. The digital signals are much more immune to crosstalk and noise when transmitted over long distances by wire, R.F., or optical paths. CVSD has better intelligibility than PCM when random bit errors are introduced during transmission.

2) **Secure Communications:** Digital data can be quite securely encrypted using fairly simple standard hardware (Figure 4a). Scrambled speech for audio channels may also be accomplished by encoding into a shift register, then selecting different segments of the shifted data in pseudo-random fashion and decoding it (Figure 4b).

3) **Audio Delay Lines:** Although charge-coupled deviced (CCD) will perform this function, they are still expensive and choice of configurations is quite limited. Also, there is a practical limit to the number of CCD stages, since each introduces a slight degradation to the signal.

   As shown in Figure 5, the delay line consists of a CVSD modulator, a shift register and a demodulator. Delay is proportional to the number of register stages divided by the clock frequency. This can be used in speech scrambling, as explained above, echo supression in PA systems; special echo effects; music enhancement or synthesis; and recursive or nonrecursive filtering.

4) **Voice I/O:** Digitized speech can be entered into a computer for storage, voice identification, or word recognition. Words stored in ROM's, disc memory, etc. can be used for voice output. CVSD, since it can operate at low data rates, is more efficient in storage requirements than PCM or other A to D conversions. Also, the data is in a useful form for filtering or other processing.

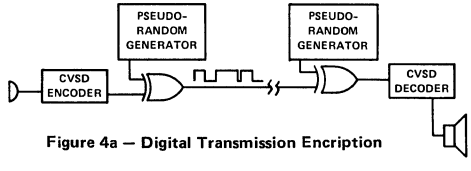


Figure 4a – Digital Transmission Encription

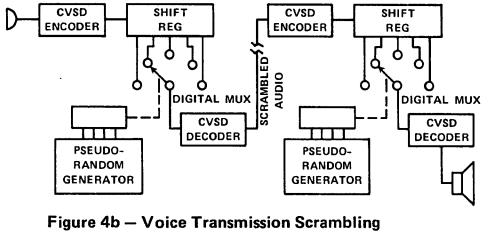


Figure 4b – Voice Transmission Scrambling

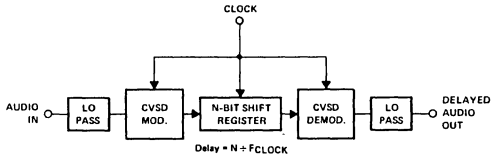


Figure 5 – Audio Delay Line

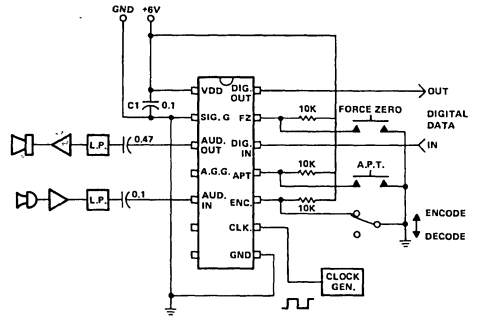


Figure 6 – CVSD Hookup for Evaluation

Figure 6 illustrates a simple evaluation breadboard circuit for the HC-55516/55532. A single device is sufficient to evaluate sound quality, etc. since, when encoding, the feedback signal at pin 3 is identical to the decoded signal from a receiver. The following are some pointers for using the devices:

1) Power supply decoupling is essential with the capacitor (C1 in Figure 6) located close to the I.C.

2) Power to the I.C. must be present before the audio input, the clock, or other digital inputs are applied. Failure to observe this may result in a latchup condition, which is usually not destructive and may be removed by cycling the supply off, then on.

3) Signal ground (pin 2) should be externally connected to pin 8 and power ground. It is recommended for noise-free operation that the audio input and output ground returns connect directly to pin 2 and to no other grounds in the system. Pins 6 and 7 must be open circuited.

4) Digital inputs and outputs are similar to and compatible with standard CMOS logic circuits using the same supply voltage. The illustrated 10K pullup resistors are necessary only with mechanical switches, and are not necessary when driving these pins with CMOS. Unused digital inputs should be tied to the appropriate supply rail for the desired operation. TTL output, however, will require pullup resistors (about 1K) to obtain the required CMOS input levels. Pins 4 and 14 will drive CMOS logic, or each can drive one low power TTL input.

5) Capacitor coupling is recommended for the audio in and out (pins 3 and 5) as each pin is internally biased to about 1/2 the supply voltage.

6) The AGC output (pin 4) is a digital output, whose duty cycle is dependent on the average audio level. This may be externally integrated to drive an AGC preamplifier; or it could be used (through a buffer gate) to drive an LED indicator to indicate proper speaking volume.

7) To prevent generation of alias frequencies, the input filter should reduce the audio amplitude at frequencies greater than half the clock rate to less than 12 millivolts peak-to-peak.

8) The complex output filter shown on the data sheet is necessary only when measuring signal to noise ratios where all frequencies above 3kHz must be removed. Generally a 2 or 3 pole filter is sufficient for acceptable voice quality.

9) A suggested receiver clock circuit is a free running multivibrator, synchronized at each transition of the incoming data. Any synch errors occurring during reception of long strings of zeros or ones will have negligible effect on the decoded voice.

Figures 7 though 11 illustrate some typical audio output (before filtering) and digital output waveforms. To make the scope picture stationary, the audio input generator was synchronized with a submultiple of the clock frequency.

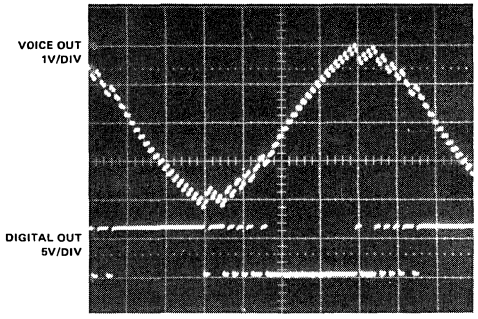
Figure 7 shows the results of a large low frequency sine wave. The somewhat jagged peaks are typical of all CVSD systems. Note that the digital output is continuous "ones" while the waveform is slewing down and continuous "zeros" while slewing up.

Figure 8 shows the excellent recovery from overdriven conditions at low frequency. Some analog type CVSD's have trouble recovering from this condition.

As mentioned previously, CVSD's cannot handle large signals at high frequencies (but these are not generally present in the human voice). Figure 9 shows this limitation where the voice output is slewing at its maximum rate, but cannot catch up with the input. At reduced amplitudes, however, the same signal can be reproduced, as shown in Figure 10.

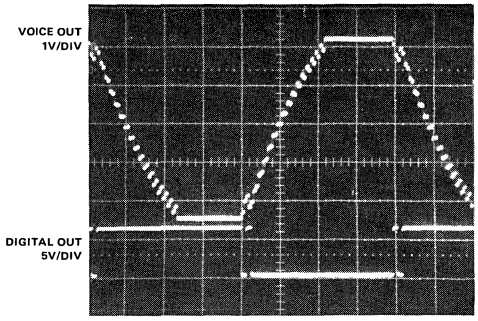
The transfer function curve on the data sheet shows that at 16kHz clock rate, a 1.4V RMS signal can be tracked up to 500Hz. With a 32kHz clock, the same curves may be used, but with each of the indicated frequencies doubled. Likewise, each of the SNR figures shown on the data sheet will be 6dB better with a 32kHz clock.

Figure 11 shows the 12 millivolt voice output waveform at 1/2 the clock rate, when there is no audio input. After filtering, this signal is inaudible.



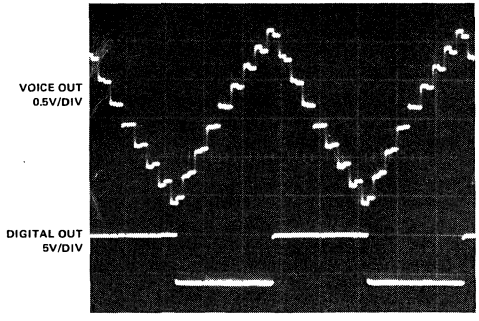
0.5ms/DIV.
VOICE IN = 250Hz, 4V P-P SINE WAVE
CLOCK = 16kHz

Figure 7 — CVSD Large Signal Sine Wave Reconstruction



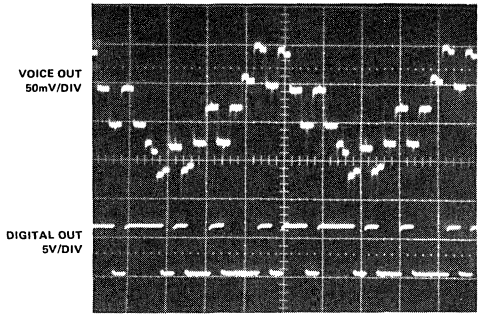
0.5ms/DIV.
VOICE IN = 250Hz, 6V P-P SINE WAVE
CLOCK = 16kHz

Figure 8 — CVSD Large Signal, Low Frequency Clipped Waveform



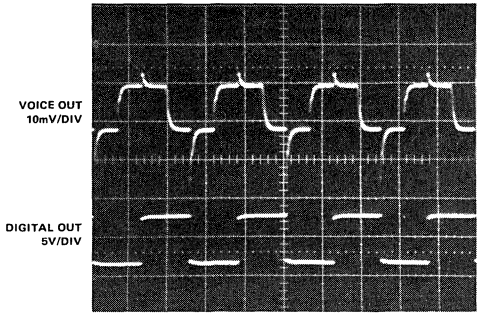
0.2ms/DIV.
VOICE IN = 1kHz, 6V P-P SINE WAVE
CLOCK = 16kHz

Figure 9 — CVSD Large Signal, High Frequency Slew Limiting



0.2ms/DIV.
VOICE IN = 1kHz, 0.15V P-P SINE WAVE
CLOCK = 16kHz

Figure 10 — CVSD Small Signal Sine Wave Reconstruction



50 μs/DIV.
VOICE IN = 0
CLOCK = 16kHz

Figure 11 — CVSD Zero Signal Idle Pattern

Chip Information

Most Harris Semiconductor Analog products are available in dice form. Orders can be placed directly with Harris salesmen and representatives or with either of our authorized chip distributors listed below:

HCI – Hybrid Components, Inc.
140 Elliott St.
Beverly, MA 01915
Tel. 617 (927-5820)
TWX 710-347-1660

Elmo Semiconductor Corp.
915 North Citrus Avenue
Los Angeles, CA 90038-2479
Tel. 213 (465-2163)
TWX 910-321-2943
Telex 69-8181

Consult your local Harris salesman, representative or chip distributor for chip data sheets and brochures as well as price and delivery information.

Harris
Quality and Reliability Programs

INTRODUCTION

The Product Assurance Department at Harris Semiconductor Analog Products Division is responsible for assuring that the quality and reliability of all products shipped to customers meet their requirements. During all phases of product fabrication there are many independent visual and electrical tests performed by Product Assurance personnel.

Prior to shipment a final inspection is performed to assure product quality, and that all requirements of the purchase order and customer specifications are met.

The following military documents provide the foundation for the Harris Analog Product Assurance Program.

MIL-M-38510	"General Specification of Microcircuits"
MIL-Q-9858A	"Quality Program Requirements"
MIL-STD-883B	"Test Methods and Procedures for Microcircuits"
NASA Publication 200-3	"Inspection System Provisions"
MIL-C-45662A	"Calibration System Requirements"
MIL-I-4508A	"Inspection Systems Requirements"

The Harris Semiconductor Reliability and Quality Manual which is available upon request, describes this total function and policies of the organization to assure product reliability and quality.

QUALITY CONTROL

All processing of Analog Products is subjected to rigid manufacturing and quality controls. Total quality committment initiates at raw material procurement, continues throughout product manufacture and final inspection and culminates in successful product performance.

Ion implantation and diffusion processes are subjected to oxide thickness controls, penetration evaluations, resistivity measurements, and inspection gates for visual defects. Diffusion furnaces, metallization and passivation equipment are subjected to frequent qualifications via C-V plotting techniques to insure product stability.

Thin film controls insure specified interconnect and passivation thicknesses. Nichrome and silicon chromium resistor processing is very carefully monitored via resistivity, film composition and geometry controls.

Other in-line process controls include:

- Critical controls on all raw materials used in device processing and assembly
- In-line SEM inspections
- Specified consistent compositions of thin film source materials
- Continual environmental monitoring for humidity, particle counts and temperature
- Controls on oxide and metallization thicknesses
- Doping concentrations and profiles
- Pre and post etch inspections
- Gates to control defect densities at mask production
- Ion penetrations
- Prescribed calibration intervals and preventive maintenance of all processing equipment
- Total specification documentation and rigid change control procedures

RELIABILITY

The primary purpose of the Reliability Department is to establish and maintain the controls and procedures which will assure, with a high level of confidence, that all manufactured product will perform as required under specific environments and under specified stress conditions for a period of time consistent with final end-use.

The Reliability approach at Harris Semiconductor is based on designing in reliability rather than only testing for reliability. Testing is utilized to confirm that sound design with quality and reliability based ground rules are observed and correctly executed in a new product design.

Reliability engineering becomes involved as early as concept review of new products and continues to remain involved through design and layout review. At all those points basic reliability guidelines are involved. At the circuit process technology and package levels, first run product evaluations and reliability qualifications are mandatory. Tests at both maximum rated and accelerated stress levels are performed. Process changes require the approval of the Reliability Manager prior to implementation.

JAN Program

The Harris Analog Wafer Fabrication and Assembly facilities have received JAN Class B certification. All Harris Analog JAN products are produced on the certified line in strict compliance with all MIL-M-38510 program requirements. Use of JAN products therefore guarantees:

- Use of Certified Lines Only
- Full MIL-M-38510 Compliance
- Strict Baseline Compliance
- Government Source Inspection
- Quality Conformance Program for Qualification Maintenance

JAN certified production lines and JAN qualified products further enhance the quality and reliability posture of Harris and emphasize its dedication to serving the needs of Hi-Rel applications.

Harris Hi-Rel processing flows and capabilities brochures are available through your local Harris representative to help you decide if your applications requirements can be met by JAN or one of the other standard production flows from Harris.

HARRIS DASH 8 devices pass the screening requirements of the latest issue of MIL-STD-883, Method 5004, Class B and the requirements specified in this document. Off-the-shelf availability of DASH 8 product meets the needs of customers seeking enhanced quality and reliability.

HARRIS SEMICONDUCTOR DASH 8 PRODUCT FLOW
MIL-STD-883, METHOD 5004, CLASS B

100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	2010 Cond. B.
2	Stabilization Bake	1008 Cond. C (24 hrs. minimum)
3	Temperature Cycling	1010 Cond. C
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: (A) Fine (B) Gross	1014 Cond. A or B 1014 Cond. C
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, 160 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at Worst Case Operating Conditions
9	External Visual	2009 Sample Inspection
10	Lot Acceptance	Table I, Group A Elect. Tests

NOTE:

Traceability: All devices are assigned date code identification that provides traceability.

Branding: All devices are branded with the HX-XXXX-8 and date code.

Aged Products: Product that has been held for more than 24 months will be reinspected prior to shipment to Group A inspection requirements.

Additional Requirements: Attributes data will be supplied on Group A Lot Acceptance upon request.

Generic data from Harris' Reliability Add-On Program is available upon request. The objective of the Harris Reliability Add-On Program is to provide a continuous life and environmental monitor for all products families in manufacturing. This program provides life test performance results to fullfill reliability data requirements and to verify package integrity. The Reliability Add-On Program is supplemental to customer funded Lot Qualification.

For customers desiring Lot Qualification, Harris Semiconductor will perform Group A, B, C and D inspections to MIL-STD-883, Method 5005 as defined herein for an additional charge.

DASH 7 Program

HIGH RELIABILITY COMMERCIAL PRODUCTS OFF-THE-SHELF DELIVERY

INTRODUCTION

The HARRIS DASH 7 program extends the normal processing to include an added burn-in step to provide extra reliability.

DASH 7 (and all other HARRIS commercial grades of product) utilizes procedures and documents that, with minor modifications, resemble those used for mil-std products as described under DASH 8. This flow includes environmental tests such as temperature cycling and seal tests, and is outlined below.

DASH 7, by adding an extra burn-in to eliminate potential early failures, will reduce incoming test requirements and service costs.

Information on availability and cost of DASH 7 processing can be obtained through the HARRIS sales representatives.

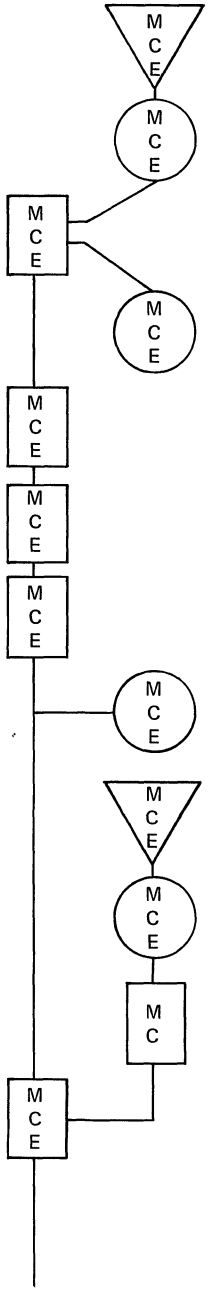
HARRIS SEMICONDUCTOR DASH 7 PRODUCT FLOW

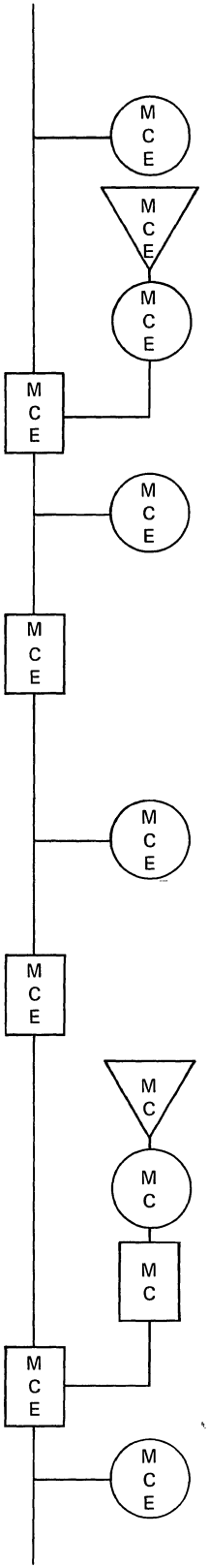
100% SCREENING PROCEDURE

	SCREEN	MIL-STD-883 METHOD/COND.
1	Internal Visual	Harris Standard in-house Level IV procedures.
2	Stabilization Bake	1008 Condition C (24 hr. min.)
3	Temperature Cycling	1010 Cond. (10 Cycles)
4	Constant Acceleration	2001 Cond. E; Y1 plane
5	Seal: Ⓐ Fine Ⓑ Gross	1014 Cond. A or B 1014 Cond. C2, no vacuum pre-cond. Step 2.
6	Initial Electrical	Harris Specifications
7	Burn-In Test	1015, min. 96 hrs. @ 125°C (or equivalent) (Burn-In circuits enclosed)
8	Final Electrical 100% go-no-go	Tested at worst case operating condition Functional tests per Table 1
9	External Visual	2009 Sample Inspection
10	Lot Acceptance	Table 1, Group A Elect. Tests.

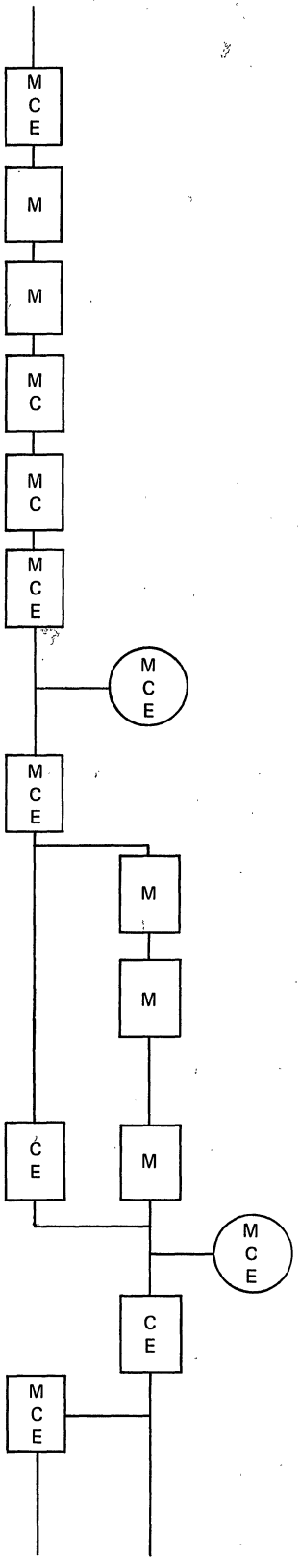
Branding: All devices are branded with the HX-XXXX-7 and date code.

Standard Products Screening and Inspection Procedure

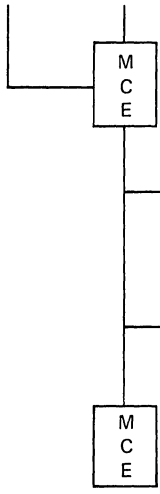
OPER. SEQ.	OPER. DESCRIPTION	PRODUCT CATEGORIES		
		MIL (M)	COMM (C)	EPOXY (E)
	Incoming Material Silicon and Chemical Procurement.	X	X	X
	Q.C. Incoming Inspection. Materials are Inspected for Conformance to Specified Requirements.	X	X	X
	Manufacturing Wafer Fabrication	X	X	X
	QC • DIH_2O & Gas Monitor • SEM Process Control • Wafer Process Control	X	X	X
	Manufacturing, Wafer Electrical Probe (100%)	X	X	X
	Manufacturing, Wafer Scribe, Break (100%)	X	X	X
	Manufacturing Dice Screen (100%)	X	X	X
	QA Dice Inspection Control	X	X	X
	Preform Procurement	X	X	N/A
	Package Procurement	X	X	N/A
	Leadframe Procurement			X
	Epoxy Compound Procurement			X
	Q.C. Preform Inspection	X	X	N/A
	Q.C. Package Inspection	X	X	N/A
	Q.C. Leadframe Inspection			X
	Manufacturing Package Clean	X	X	N/A
	Manufacturing Die Mounting	X	X	X



QA Die Mount Control (continuous sampling) • Visual Die Inspection	X	X	X
Bond Wire Procurement	X	X	X
Q.C. Wire Inspection	X	X	X
Manufacturing Wire Bonding	X Al	X Al	X Au
QA Bond Control (continuous sampling) • Visual Die & Bond Inspection • Wire and Pull Test	X	X	X
Manufacturing Pre-Seal Screen (100%)	MS883 Method 2010 Cond. A or B	MS883 Method 2010 HS Mod. Cond. B	MS883 Method 2010 HS Mod. Cond. B
QA Pre-Seal Inspection Lot Acceptance	MS883 Method 2010 Cond. A or B	MS883 Method 2010 HS Mod. Cond. B	MS883 Method 2010 HS Mod. Cond. B
Preseal Bake Per MS-883, Method 1008, Cond. C (for TO-5 Type Cans Only)	8 hr.	4 hr.	N/A
Package Lid Procurement	X	X	N/A
Package Lid Inspection	X	X	N/A
Package Lid Clean	X	X	N/A
Package Seal/Encapsulation	X	X	X
QA Package Seal/Encapsulated Control (continuous sampling)	X	X	X



Stabilization Bake MS-883, Method 1008, Cond. C.	24 hr.	24	24
Temperature Cycle, MS-883, Method 1010, Cond. C,(10 Cycles)	X	X	X
Centrifuge, MS-883, Method 1010, (Y1) Plane 30 KG's min.	X	X	X
Fine Leak, MS-883, Method 1014	X	X	N/A
Gross Leak, MS-883, Method 1014 (1) Except Pre-Conditioning not Performed	100%	100% (1)	N/A
Frame Removal & Loading Units In Carriers/Sticks	X	X	X
Final QA Lot Inspection, MS-883 Method 1014 • Fine & Gross Leak • Visual/Mechanical Inspection	X	X	X
100% Initial Tests	X	X	X
Brand Device Type/Date Code Serialize, If Applicable	X	N/A	N/A
Burn-In (100%), MS-883, Method 1015 (for Jan B, –8 military product and -7 commercial product only)	X	X	X
Group A Final Test (100%)	X	X	X
QA acceptance • Electrical Testing • Visual/Mechanical Method 2009 Lot Sampling	X	X	X
Brand Devices Type/Date Code	N/A	X	X
Controlled Inventory	X	X	X



Package for Shipment	X	X	X
Quality Conformance Inspection Group A/B/C/D Testing, MS-883, Method 5005, Periodically or by Customer P.O. Request	X	N/A	N/A
QA Plant Clearance • Final Visual of Marking and Physical Quantity, Conformation of Product by Inspection or Sample Test	X	X	X
Ship to Customer	X	X	X

HARRIS Commercial Grade Products

This product is processed on the same wafer fabrication lines, to the same thorough specification and rigid controls as HI-Rel parts. At wafer electrical probe the product may be categorized for electrical performance, such as temperature range of operation or maximum output (see specific product data sheet for grading details) by utilizing multiple colored inks. Defective die are inked with red ink, but, for example, die meeting the commercial temperature range electrical specifications may be inked with green ink.

The die are then visually inspected and sorted after die separation to a modified Class B visual criteria. They are then assembled in packages on a controlled assembly line. The ink used to categorize product performance, such as the green ink, might not be removed from the commercial grade die. This ink has been chemically characterized as inert and reliability verification confirms there is no effect on performance or operating life of the parts.

Harris invites any interested customer to review our assembly flow and facilities for information, quality survey, or certification.

Table I — Group A Electrical Tests[1]

SUBGROUP[2]	CLASSES S AND B LTPD	CLASS C LTPD
Subgroup 1 Static Test at 25°C	5	5
Subgroup 2 Static Tests at Maximum Rated Operating Temperature	7	10
Subgroup 3 Static Tests at Minimum Rated Operating Temperature	7	10
Subgroup 4 Dynamic Tests at 25°C	5	5
Subgroup 5 Dynamic Tests at Maximum Rated Operating Temperature	7	10
Subgroup 6 Dynamic Tests at Minimum Rated Operating Temperature	7	10
Subgroup 7 Functional Tests at 25°C	5	5
Subgroup 8 Functional Tests at Maximum and Minimum Rated Operating Temp.	10	15
Subgroup 9 Switching Tests at 25°C	7	10
Subgroup 10 Switching Tests at Maximum Rated Operating Temperature	10	15
Subgroup 11 Switching Tests at Minimum Rated Operating Temperature	10	15

1. The specific parameters to be included for tests in each subgroup shall be as specified in the applicable procurement document or specification sheet. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test to satisfy Group A requirements.
2. A single sample may be used for all subgroup testing. Where the required size exceeds the lot size, 100% inspection shall be allowed.

Table II — Group B Tests (Lot Related)[1]

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1 Physical Dimensions	2016		2 Devices (No Failures)
Subgroup 2 Resistance to Solvents	2015		4 Devices (No Failures)
Subgroup 3 Solderability [3]	2003	Soldering Temperature of 260 ± 10°C	15
Subgroup 4 Internal Visual and Mechanical	2014	Failure Criteria from Design and Construction Requirements of Applicable Procurement Document.	1 Device (No Failures)
Subgroup 5 Bond Strength[2] (1) Thermocompression (2) Ultrasonic or Wedge (3) Beam Lead	2011	(1) Test Condition C or D (2) Test Condition C or D (3) Test Condition H	15
Subgroup 6	—	Not Applicable	—
Subgroup 7 Seal (a) Fine (b) Gross	1014	As Applicable	5

NOTES:

1. Electrical reject devices from the same inspection lot may be used for all subgroups when end point measurements are not required.
2. Test samples for bond strength may, at the manufacturer's option unless otherwise specified be randomly selected immediately following internal visual (precap) inspection specified in method 5004, prior to sealing.
3. All devices submitted for solderability test must have been through the temperature/time exposure specified for burn-in. The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of leads required.
4. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note — Table 1*

Table III — Group C (Die Related Tests)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LTPD*
Subgroup 1			
Operating Life Test	1005	Test Condition to be specified (1000 Hrs)	5
End Point Electrical Parameters		Table I — Subgroup 1	
Subgroup 2			
Temperature Cycling	1010	Test Condition C	15
Constant Acceleration	2001	Test Condition E Y_1 Axis	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [2]			
Visual Examination	1.		
End Point Electrical Parameters		Table I — Subgroup 1	

NOTES:

1. Visual examination shall be in accordance with method 1010.
2. When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.
3. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.

* Reference Note - Table 1 *

Table IV — Group D (Package Related Tests)

TEST	MIL-STD-883 METHOD	MIL-STD-883 CONDITION	LPTD*
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2[4]			
Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6]			
Lid Torque [8]	2024	As Applicable	
Subgroup 3 [1]			
Thermal Shock	1011	Test Condition B as a Minimum, 15 Cycles Minimum.	15
Temperature Cycling	1010	Test Condition C, 100 Cycles Minimum	
Moisture Resistance	1004	Omit Initial/Conditioning and Vibration	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6]			
Visual Examination	2.		
End Point Electrical Parameters		Table 1 — Subgroup 1	
Subgroup 4 [1]			
Mechanical Shock	2002	Test Condition B	15
Vibration Variable Frequency	2007	Test Condition A	
Constant Acceleration	2001	Test Condition E	
Seal	1014	As Applicable	
(a) Fine			
(b) Gross [6]			
Visual Examination	3.		
End Point Electrical Parameters		Table 1 — Subgroup 1	
Subgroup 5 [4]			
Salt Atmosphere	1009	Test Condition A	15
Seal			
(a) Fine			
(b) Gross			
Visual Examination			
Subgroup 6			
Internal Water Vapor Content	1018	5,000 ppm Maximum Water Content at 100°C	3 Devices (0) Failures or 5 Devices (1 Failure)
Subgroup 7 [4]			
Adhesion of Lead Finish	2025		15
Lid Torque [10]	2023		

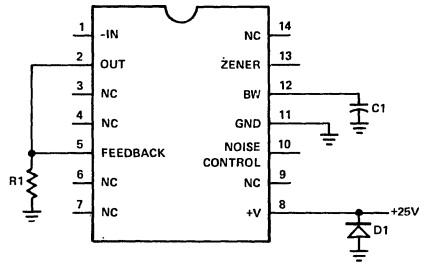
NOTES:
1. Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical"
2. Visual examination shall be in accordance with method 1004.
3. Visual examination shall be performed in accordance with method 2007 for evidence of defects or damage to case, leads, or seals resulting from testing (not fixturing). Such damages shall constitute a failure.
4. Electrical reject devices from that same inspection lot may be used for sample.
5. Visual examination shall be in accordance with paragraph 3.3.1 for method 1009.
6. When fluorocarbon gross leak testing is utilized, test condition C_2 shall apply as minimum.
7. Generic data from Harris Reliability Add-On Program in the form of Reliability Bulletins are available upon request.
8. Required for packages which use glass frit seal.
9. If initial sample (3 or 5) fails, additional sampling may be tested at another facility and all data presented.
10. Applicable only to package which use glass frit seal.

* Reference Note — Table 1*

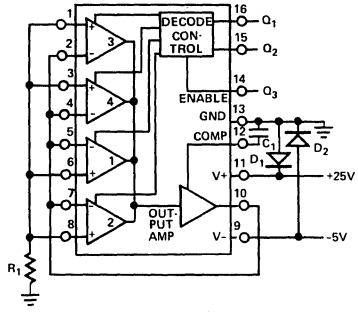
Burn-In Circuit Index

		DRAWING NO.
HA-1608	+10V Adjustable Voltage Reference	1
HA-2400/04/05	PRAM, Four Channel Operational Amplifiers	2
HA-2420/25	Fast Sample and Hold Operational Amplifiers	3, 4
HA-2500/02/05	Precision High Slew Rate Operational Amplifiers	5
HA-2510/12/15	High Slew Rate Operational Amplifers	5
HA-2520/22/25	Uncompensated High Slew Rate Operational Amplifiers	5
HA-2530/35	High Slew Rate Wideband Inverting Operational Amplifiers	6
HA-2539	Very High Slew Rate Wideband Operational Amplifiers	7
HA-2540	Wideband, Fast Settling Operational Amplifiers	8
HA-2600/02/05	Wideband, High Impedance Operational Amplifiers	5
HA-2620/22/25	Very Wideband, Uncompensated Operational Amplifiers	5
HA-2630/35	High Performance Current Booster	9
HA-2640/45	High Voltage Operational Amplifiers	5
HA-2650/55	Dual High Performance Operational Amplifiers	10, 11
HA-2720/25	Wide Range Programmable Operational Amplifiers	12
HA-2730/35	Wide Range Dual Programmable Operational Amplifiers	13
HA-2740	Quad Programmable Operational Amplifiers	14
HA-4156	High Performance Quad Operational Amplifiers	15
HA-4600/02/05	High Performance Quad Operational Amplifiers	16
HA-4620/22/25	Wideband, High Performance Quad Operational Amplifiers	16
HA-4741	Quad Operational Amplifier	15
HA-4900/02/05	Precision Quad Comparators	17
HA-5062	Low Power, JFET Input Operational Amplifier	18
HA-5064	Low Power, JFET Input Quad Operational Amplifier	15
HA-5082	JFET Input Operational Amplifier	18
HA-5084	JFET Input Quad Operational Amplifier	15
HA-5100/05	Wideband, JFET Input Operational Amplifiers	19
HA-5110/15	Wideband, JFET Input, Uncompensated Operational Amplifiers	19
HA-5130/35	Precision Operational Amplifiers	20
HA-5160/62	Wideband, JFET Input, High Slew Rate, Uncompensated Operational Amplifiers	21
HA-5170	Precision JFET Input Operational Amplifier	20
HA-5190/95	Wideband, Fast Settling Operational Amplifiers	8, 22
HA-8023	Triple Low Power Programmable Operational Amplifier	23
HC-5502	SLIC-LC Subscriber Line Interface Circuit	24
HC-5512	PCM Monolithic Filter	25
HC-55516	All Digital Continuously Variable Slope Delta Modulator (CVSD)	26
HI-200	Dual SPST CMOS Analog Switch	27, 28
HI-201	Quad SPST CMOS Analog Switch	29
HI-201HS	High Speed Quad SPST CMOS Analog Switch	29
HI-300	Dual SPST CMOS Analog Switch	30
HI-301	SPDT CMOS Analog Switch	30
HI-302	Dual DPST CMOS Analog Switch	30
HI-303	Dual SPDT CMOS Analog Switch	31
HI-304	Dual SPST CMOS Analog Switch	31
HI-305	SPDT CMOS Analog Switch	31
HI-306	Dual DPST CMOS Analog Switch	31
HI-307	Dual SPDT CMOS Analog Switch	31
HI-381	Dual SPST CMOS Analog Switch	32
HI-384	Dual DPST CMOS Analog Switch	33
HI-387	SPDT CMOS Analog Switch	32
HI-390	Dual SPDT CMOS Analog Switch	33
HI-506/507	Single 16/Differential 8 Channel CMOS Analog Multiplexers	34
HI-506A/507A	16 Channel CMOS Analog Multiplexers with Overvoltage Protection	34
HI-508/509	Single 8/Differential 4 Channel CMOS Analog Multiplexers	35, 36, 37, 38
HI-508A/509A	8 Channel CMOS Analog Multiplexers with Overvoltage Protection	35, 36, 37, 38
HI-516	16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer	39
HI-518	8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer	40
HI-524	4 Channel Video Multiplexer	41
HI-539	Monolithic, Four Channel, Low Level, Differential Multiplexer	42
HI-562A	12 Bit High Speed Monolithic Digital-to-Analog Converter	43
HI-1818A	Low Resistance 8 Channel CMOS Analog Multiplexer	44, 45
HI-1828A	Low Resistance 8 Channel CMOS Analog Multiplexer	46, 47

1 HA-1608

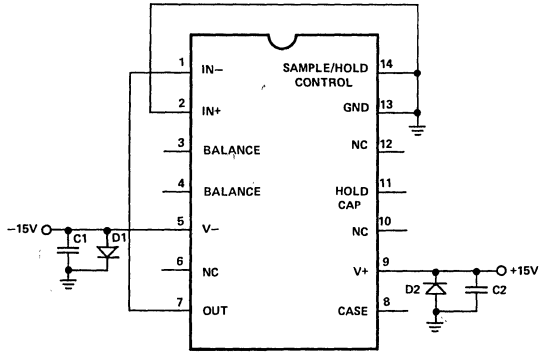


2 HA-2400/04/05



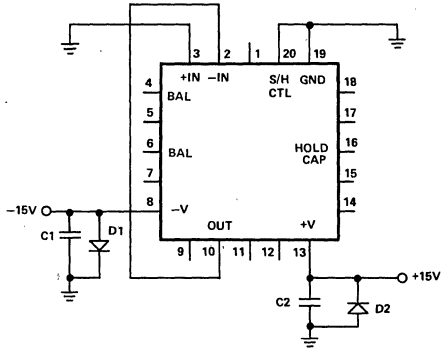
NOTES:
TA = +125°C
R1 = 100kΩ
C1 = 910pF, 50V
D1, D2 = IN4002
Freq., Q1 = 100kHz, Q2 = 50kHz, Q3 = 25kHz

3 HA-2420/25



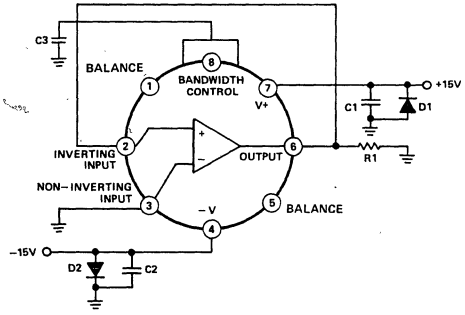
NOTES:
C1, C2 = .01μF
D1, D2 = IN4002

4 HA-2420/25



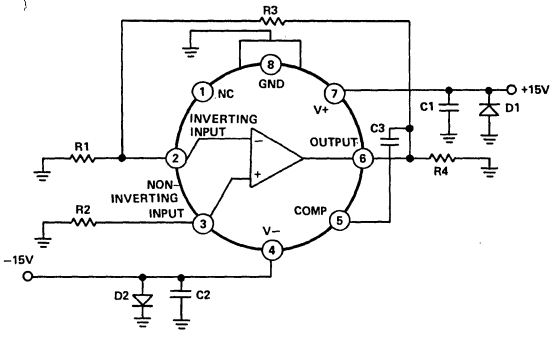
NOTES:
C1, C2 = .01μF
D1, D2 = IN4002

5 HA-2500/02/05, HA-2510/12/15, HA-2520/22/25 HA-2600/02/05, HA-2620/22/25, HA-2640/45 LM118/318, LM118A/318A, LM143/343, LM143A/343A



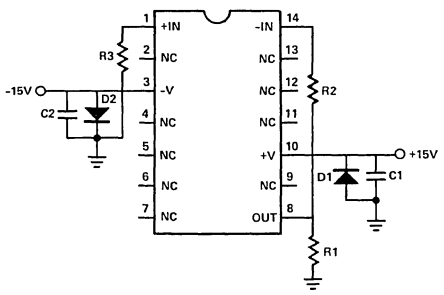
NOTES:
R1 = 2kΩ, ±5%, 1/4 or 1/2 Watt
C1 = C2 = C3 = 0.01μF
D1 = D2 = IN4002

6 HA-2530/35



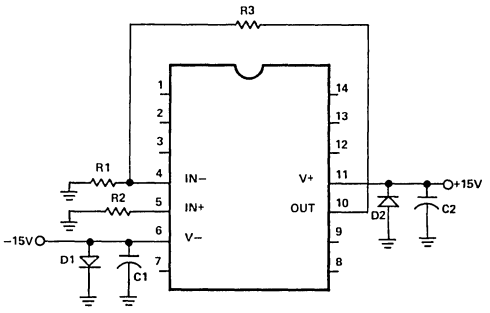
NOTES:
C1 = C2 = 0.01μF; C3 = 10pF
R1 = R2 = 1kΩ, ±5%, 1/2 or 1/4 Watt
R3 = 10kΩ, ±5%, 1/4 or 1/2 Watt
R4 = 2kΩ, ±5%, 1/4 or 1/2 Watt
D1 = D2 = IN4002

7 HA-2539



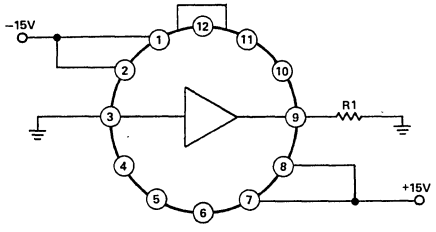
NOTES:
R1 = R3 = 1kΩ, ±5%
R2 = 10kΩ, ±5%
C1 = C2 = 0.01μF (One Per Socket)
D1 = D2 = IN4002 (One Per Board)

8 HA-2420/25, HA-5190/95



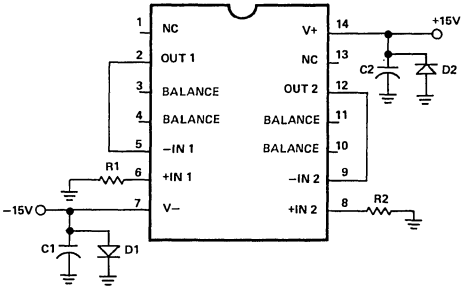
NOTES:
R1, R2: 1KΩ, 1/4 or 1/2 Watt, 5%
R3: 10kΩ, 1/4 or 1/2 Watt, 5%
C1, C2: 0.1μF
D1, D2: IN4002

9 HA-2630/35



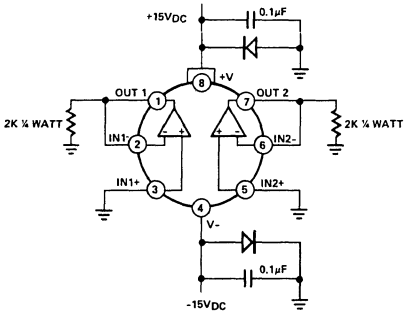
NOTE:
R1 = 2kΩ

10 HA-2650/55, LM1458A/1558A, LM4250/4250C



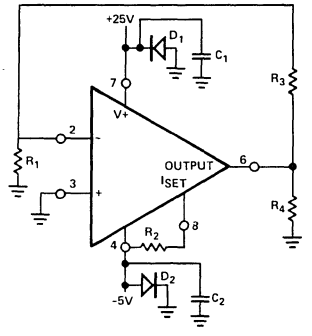
NOTES:
R1, R2: 1MΩ, 1/4 or 1/2 Watt, 5%
C1, C2: 0.1μF
D1, D2: IN4002

11 HA-2650/55, LM4250/4250C



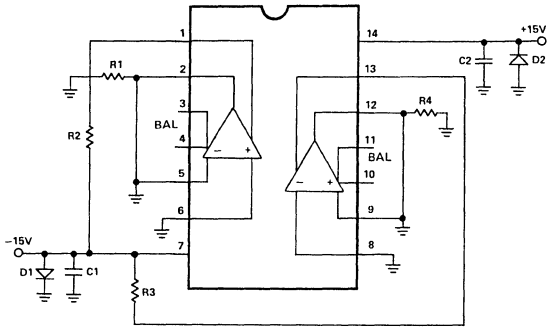
NOTES:
TA = +125°C, Supplies = ±15VDC
Resistors = 2kΩ, ±10%, 1/4 Watt
Capacitors = 0.01 to 0.1μF, Nonelectrolytic

12 HA-2720/25



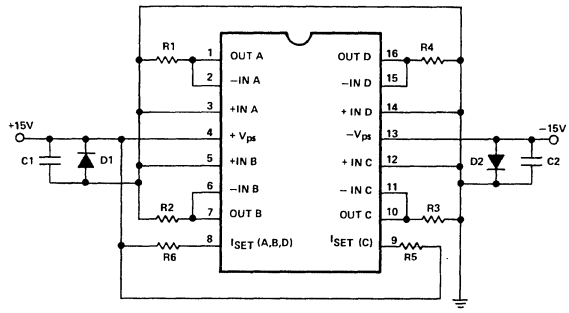
NOTES:
TA = +125°C
C1, C2 = 0.01 to 0.1μF
R1 = 1kΩ, R2 = 2MΩ, R3 = 10kΩ, R4 = 5kΩ

13 HA-2730/35



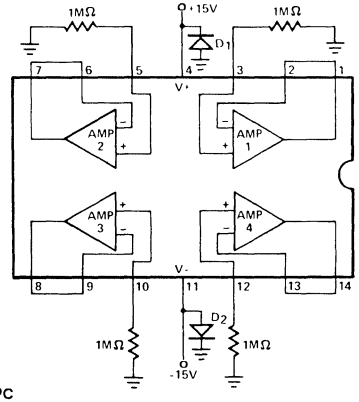
NOTES:
R1, + R4 = 2kΩ
R2, + R3 = 2MΩ
C1, + C2 = .01 to .1μF
D1, + D2 = IN4002 or Similar

14 HA-2740, LM146/346



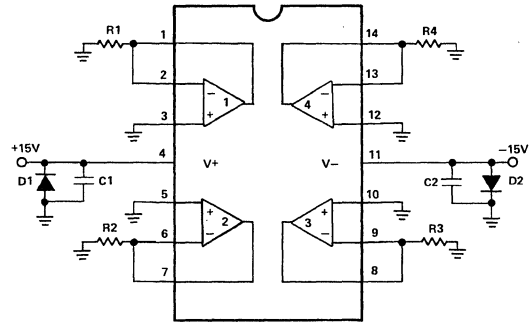
NOTES:
C1, C2 = 0.01μF
D1, D2 = IN4002
R1, R2, R3, R4 = 2kΩ, 1/2 or 1/4 Watt, 5%
R5, R6 = 3MΩ, 1/2 or 1/4 Watt, 5%

15 HA-4156, HA-4741, HA-5064, HA-5084, LF374, LM148/348, LM2908



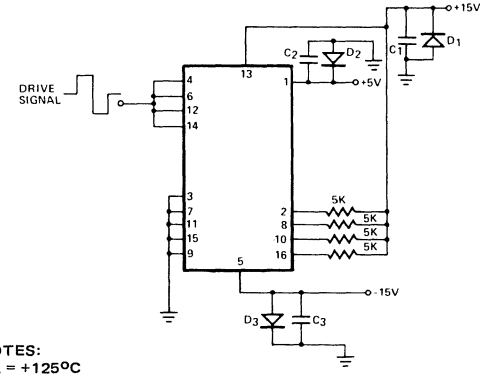
NOTES:
TA = +125°C
D1, D2 = IN4002

16 HA-4600/02/05, HA-4620/22/25



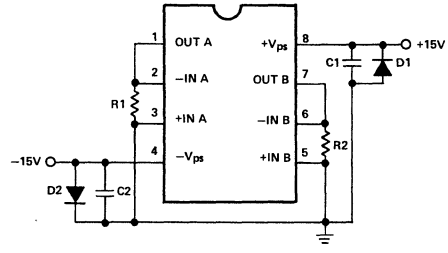
NOTES:
C1 = C2 = 0.01μF
D1 = D2 = IN4002
R1 = R2 = R3 = R4 = 2kΩ, ±5%, 1/4 or 1/2 Watt

17 HA-4900/02/05



NOTES:
TA = +125°C
C1, C2, C3 = 0.1μF
D1, D2, D3 = IN4002
Drive Signal Freq. = 2000Hz
Drive Signal Amp. = ±0.6V

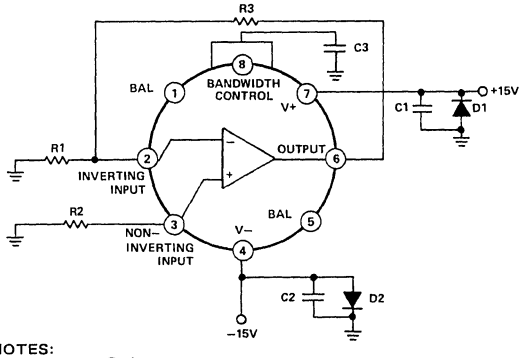
18 HA-5062, HA-5082, LF353



NOTES:
C1, C2 = 0.01μF
D1, D2 = IN4002
R1, R2 = 2kΩ, 1/2 or 1/4 Watt, 5%

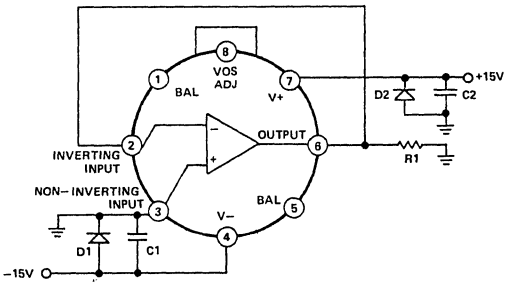
10

19 HA-5100/05, HA-5110/15, LF156 Series, LF157 Series



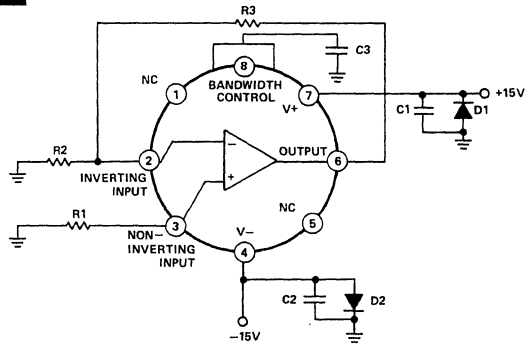
NOTES:
R1 = R2 = 10kΩ, ±5%, 1/4 or 1/2 Watt
R3 = 100kΩ, ±5%, 1/4 or 1/2 Watt
C3 = 0.01μF
C1 = C2 = 0.1μF
D1 = D2 = IN4002

20 HA-5130/35, HA-5170, LF155 Series, LM108/308, LM108A/308A, OP-07



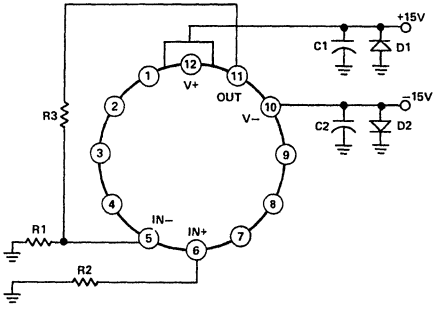
NOTES:
R1 = 2kΩ, 5%, 1/4 or 1/2 Watt
C1, C2 = .01μF
D1, D2 = IN4002

21 HA-5160/62



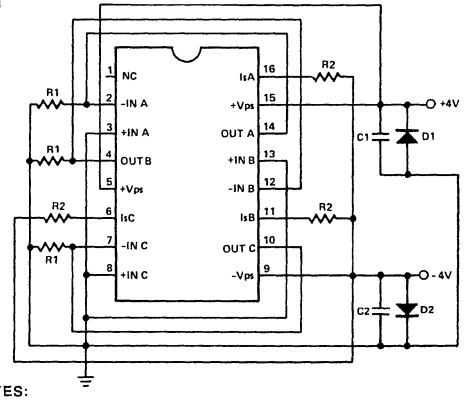
NOTES:
R1 = R2 = 1kΩ, ±5%, 1/4 or 1/2 Watt
R3 = 10kΩ, ±5%, 1/4 or 1/2 Watt
C1 = C2 = 0.01μF
C3 = 0.1μF
D1 = D2 = IN4002

22 HA-5190/95



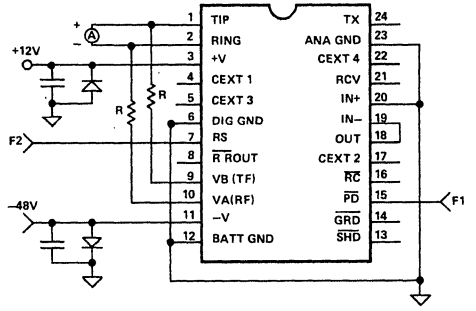
NOTES:
R1, R2: 1kΩ, 1/4 or 1/2 Watt, 5%
R3: 10kΩ, 1/4 or 1/2 Watt, 5%
C1, C2: 0.1μF
D1, D2: IN4002

23 HA-8023



NOTES:
R1 = 2kΩ, 5%, 1/4 or 1/2 Watt (One Each Per Socket)
R2 = 150kΩ, 5%, 1/4 or 1/2 Watt (One Each Per Socket)
C1, C2 = 0.01μF (One Each Per Socket)
D1, D2 = IN4002 (One Each Per Board)

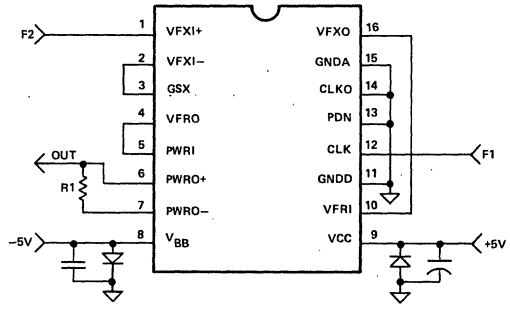
24 HC-5502



NOTES:
R = 300Ω, ±10%, 1/4 Watt
f1 = 15Hz, 0-5V Square Wave
f2 = 60Hz, 0-5V Square Wave
f1 and f2 must be synchronized

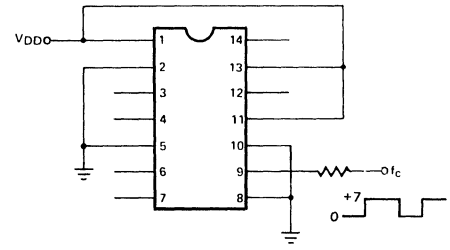
10

25 HC-5512/5512A



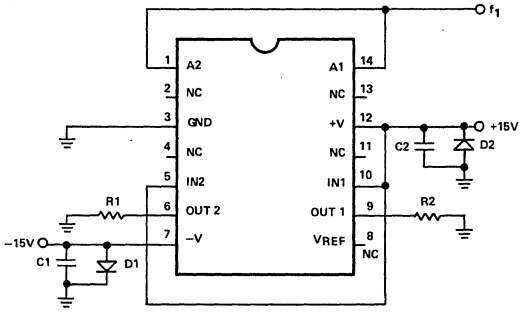
NOTES:
R1 = 600Ω
f1 = 800kHz, TTL ±10%
f2 = 2.0Vp-p, 1kHz

26 HC-55516



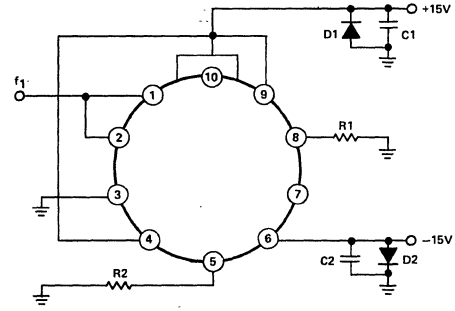
NOTES:
TA = +125°C
VDD = +7.0V
fc = 16kHz

27 HI-200



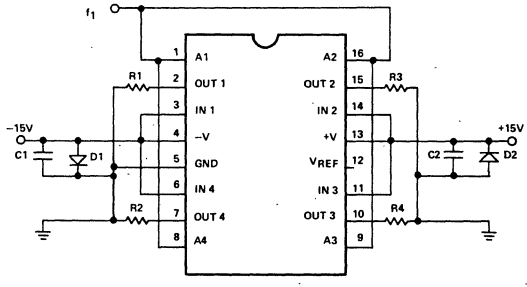
NOTES:
f1 = 50kHz
R1, R2 = 1kΩ
C1, C2 = .01μF
D1, D2 = IN4002
(For Static Configuration Tie A1, A2 to Ground)

28 HI-200



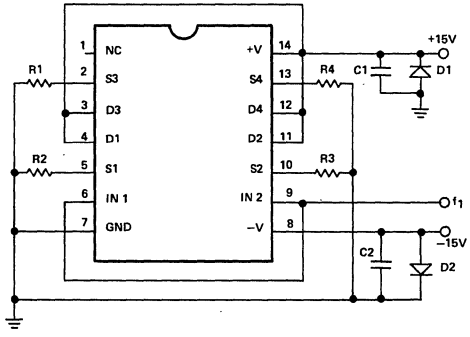
NOTES:
C1 = C2 = 0.1μF
R1 = R2 = 1kΩ, ±5%, 1/4 or 1/2 Watt
D1 = D2 = IN4002
f1 = 50kHz
(For Static Burn-In Tie f1 to Ground)

29 HI-201, HI-201HS



NOTES:
R1, R2, R3, R4 = 10kΩ, 5%, 1/4 or 1/2 Watt
C1, C2 = .01μF
D1, D2 = IN4002
f = 100kHz, TTL Levels (50% Duty Cycle)

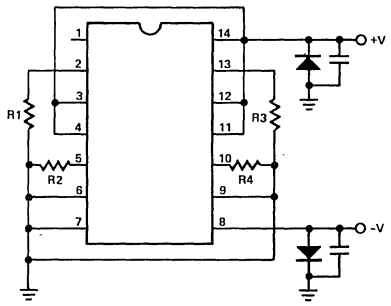
30 HI-300, HI-301, HI-302



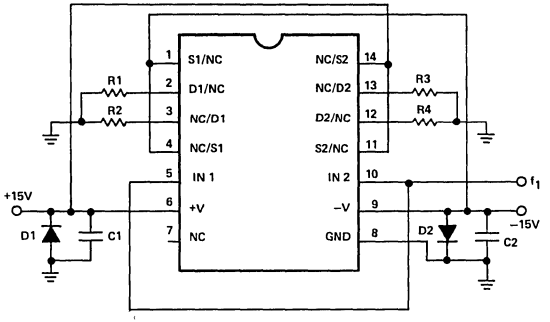
NOTES:
R1, R2, R3, R4 = 10kΩ, 5%, 1/4 or 1/2 Watt
C1, C2 = .01μF
D1, D2 = IN4002
F1 = 100kHz, TTL Levels, (50% Duty Cycle 0-5V)

10

31 HI-303, HI-304, HI-305, HI-306, HI-307

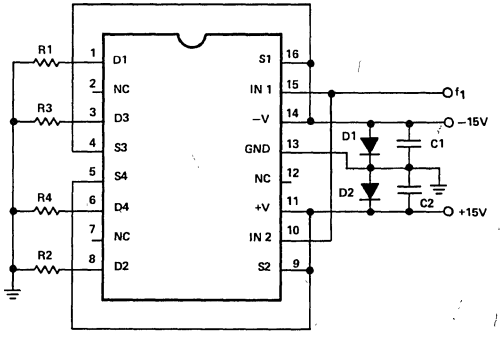


32 HI-381, HI-387



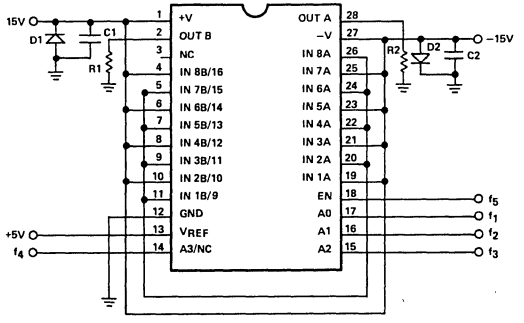
NOTES:
R1 – R4 = 10kΩ, ±5%, 1/4 or 1/2 Watt
C1 – C2 = .01μF
D1 – D2 = IN4002
f1 = 100kHz TTL Levels, 5% Duty Cycle
(For Static Configuration Tie Input (f1) to Ground)

33 HI-384. HI-390



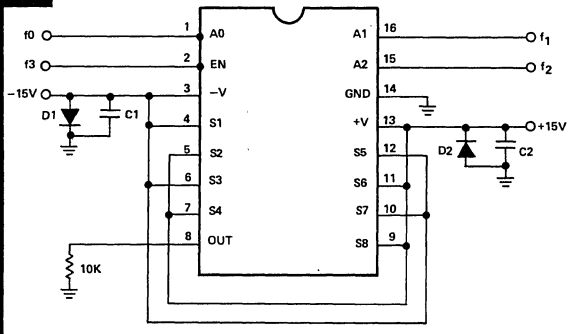
NOTES:
R1 – R4 = 10kΩ, ±5%, 1/4 or 1/2 Watt
C1 – C2 = .01μF
D1 – D2 = IN4002
f1 = 100kHz, TTL Levels (0–5V), 50% Duty Cycle
(For Static Configuration Tie Inputs (f1) to +5V)

34 HI-506/507, HI-506A/507A



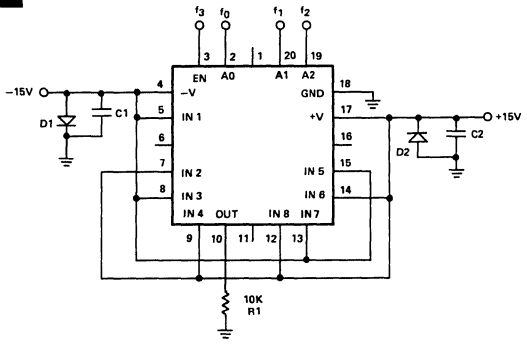
NOTES:
R1, R2 = 1KΩ, 5%, 1/2 or 1/4 Watt
C1, C2 = 0.1μF
D1, D2 = IN4002
f1 = 100kHz, f2 = 50kHz, f3 = 25kHz, f4 = 12.5kHz, f5 = 6.25kHz
(For Static Configuration Tie A0, A1, A2, A3 & EN to Ground)

35 HI-508, HI-508A



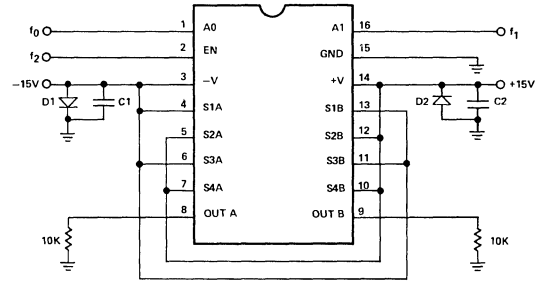
NOTES:
R1 =10kΩ, 5%, 1/4 or 1/2 Watt
C1, C2 = 0.1μF
D1, D2 = IN4002
f0 = 100kHz, f1 = 50kHz, f2 = 25kHz, f3 = 12.5kHz,
50% Duty Cycle (0–5V)
(For Static Configuration Tie A0, A1 & A2 to +5V,
Tie EN to Ground)

36 HI-508, HI-508A



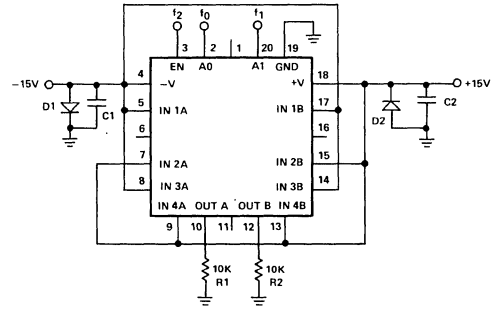
NOTES:
R1 = 10kΩ, ±5%, 1/4 or 1/2 Watt
C1, C2 = .01μF
D1, D2 = IN4002
f0 = 100kHz, f1 = 50kHz, f2 = 25kHz, f3 = 12.5kHz, EN = 6.25kHz,
50% Duty Cycle 0–5V
(For Static Configuration Tie A0, A1, A2 to +5V, EN to Ground)

37 HI-509, HI-509A



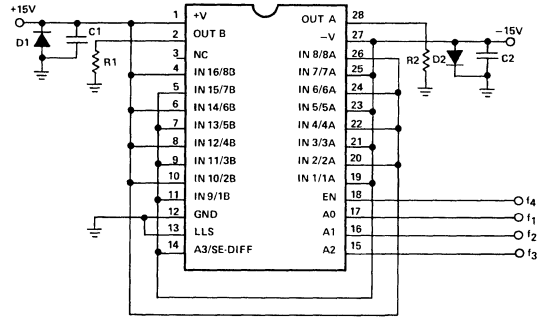
NOTES:
R1, R2 = 10kΩ, ±5%, 1/2 or 1/4 Watt
C1, C2 = .01μF
D1, D2 = IN4002
f0 = 100kHz, f1 = 50kHz, f2 = 25kHz, 50% Duty Cycle (0–5V)
(For Static Configuration Tie A0, A1 to +5V, Tie EN to Ground)

38 HI-509, HI-509A



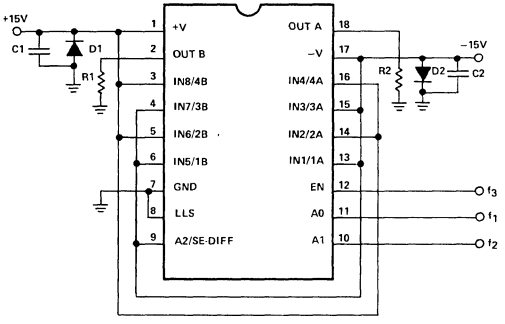
NOTES:
R1, R2 = 10kΩ, ±5%, 1/2 or 1/4 Watt
C1, C2 = .01μF
D1, D2 = IN4002
f0 = 100kHz, f1 = 50kHz, f2 = 25kHz, EN = 12.5kHz,
50% Duty Cycle (0–5V)
(For Static Configuration Tie A0, A1, & A2 to +5V, EN to GND)

39 HI-516



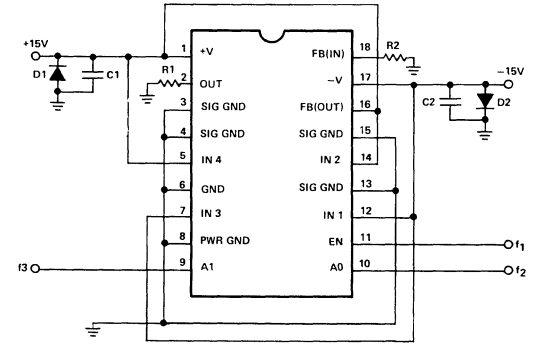
NOTES:
R1, R2 = 10kΩ, ±5%, 1/4 or 1/2 Watt
D1, D2 = IN4002
C1, C2 = .01μF
f1 = 100kHz, f2 = 50kHz, f3 = 25kHz, f4 = 12.5kHz,
50% Duty Cycle (0–5V)
(For Static Configuration Tie A0 — A2 to +5V, Tie EN to GND)

40 HI-518



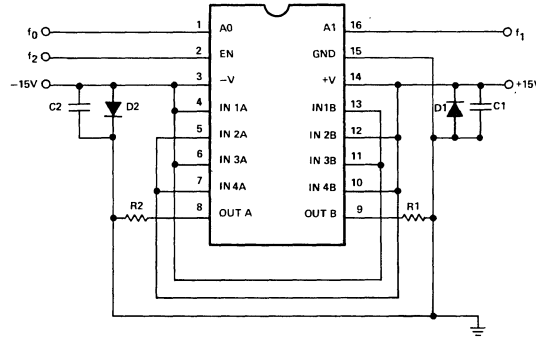
NOTES:
R1, R2 = 10kΩ, ±5%, 1/4 or 1/2 Watt
C1, C2 = .01μF
D1, D2 = IN4002
f1 = 100kHz, f2 = 50kHz, f3 = 25kHz, 50% Duty Cycle (0–5V)
(For Static Configuration Tie A0, A1 to +5V, Tie EN to GND)

41 HI-524



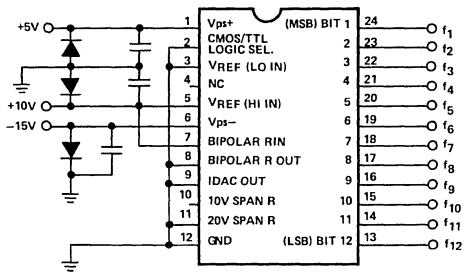
NOTES:
R1, R2 = 10kΩ, ±5%, 1/4 or 1/2 Watt
C1, C2 = .01μF
D1, D2 = IN4002
f1 = 500kHz, f2 = 250kHz, f3 = 125kHz, TTL Levels,
50% Duty Cycle

42 HI-539



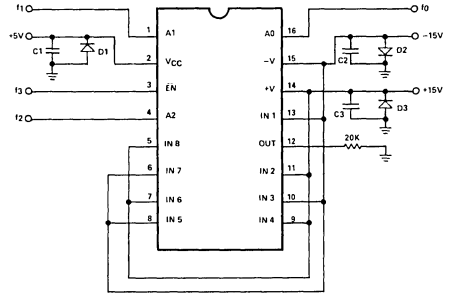
NOTES:
C1, C2 = .01μF
D1, D2 = IN4002
R1, R2 = 10kΩ, 5%, 1/2 or 1/4 Watt
f0 = 100kHz, f1 = 50kHz, f2 = 25kHz, TTL Logic Levels

43 HI-562A



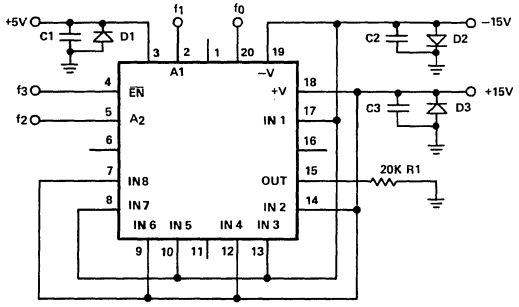
NOTES:
C1 — C3 = .01μF; D1 — D3 = IN4002
f1 = 100kHz, f2 = 50kHz, f3 = 25kHz, f4 = 12.5kHz, f5 = 6.25kHz, f6 = 3.125kHz, f7 = 1.56kHz, f8 = .78kHz, f9 = .390kHz, f10 = .195kHz, f11 = .098kHz, f12 = .049kHz
(For Static Configuration Tie f1 — f12 to +Vps, +5V)

44 HI-1818A



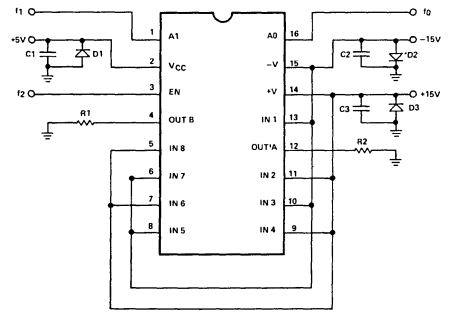
NOTES:
C1, C2, C3 = .01μF
D1, D2, D3 = IN4002
A0 = 100kHz, A1 = 50kHz, A2 = 25kHz, EN = 12.5kHz, 50% Duty Cycle (0–5V)
(For Static Configuration Tie EN, A0, A1, A2 to +5V)

45 HI-1818A



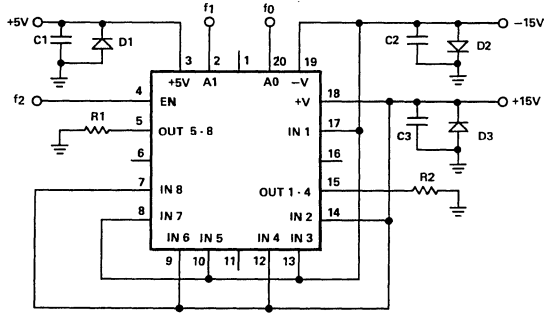
NOTES:
R1 = 20kΩ, ±5%, 1/2 or 1/4 Watt
C1, C2, C3 = .01μF
D1, D2, D3 = IN4002
A0 = 100kHz, A1 = 50kHz, A2 = 25kHz, EN = 12.5kHz, 50% Duty Cycle (0–5V)
(For Static Configuration Tie EN, A0, A1, A2 to +5V)

46 HI-1828A



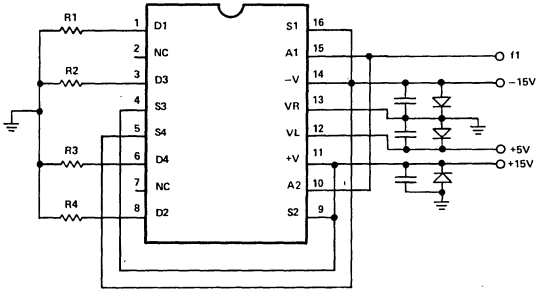
NOTES:
R1, R2 = 20kΩ, 5%, 1/4 or 1/2 Watt
C1, C2, C3 = .01μF
D1, D2, D3 = IN4002
A0 = 100kHz, A1 = 50kHz, EN = 25kHz, 50% Duty Cycle (0–5V)
(For Static Configuration Tie A0, A1, EN to +5V)

47 HI-1828A



NOTES:
R1, R2 = 20kΩ, 5%, 1/4 or 1/2 Watt
C1, C2, C3 = .01μF
D1, D2, D3 = IN4002
A0 = 100kHz, A1 = 50kHz, EN = 25kHz, 50% Duty Cycle (0–5V)
(For Static Configuration Tie A0, A1, EN to +5V)

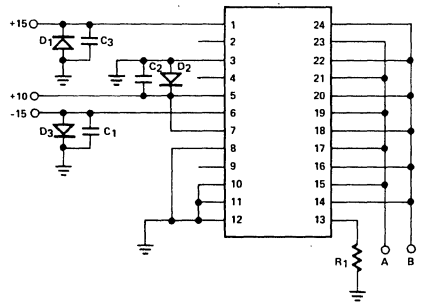
48 HI-5040 Thru HI-5051



NOTES:
R1 — R4 = 10kΩ, 5%, 1/4 or 1/2 Watt
C1, C2, C3 = .01μF
D1, D2, D3 = IN4002
f1 = 100kHz, 50% Duty Cycle
(For Static Configuration Tie Inputs (Pins 10, 15) to +5V)

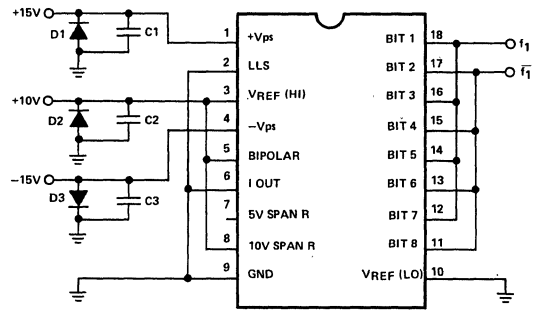
10

49 HI-5610



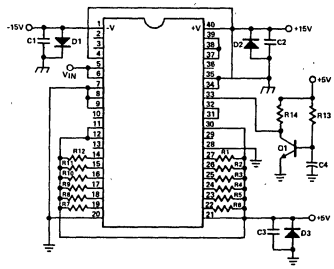
NOTES:
R1 = 50kΩ
D2, D3, D11 = IN4002
C2, C3, C11 = 0.01μF

50 HI-5618A/18B



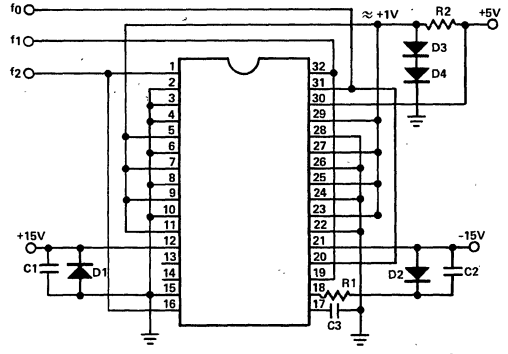
NOTES:
D1 — D3 = IN4002 or Similar
C1 — C3 = .1μF
f1 = 1MHz, TTL Level, 50% Duty Cycle

51 HI-5712/12A

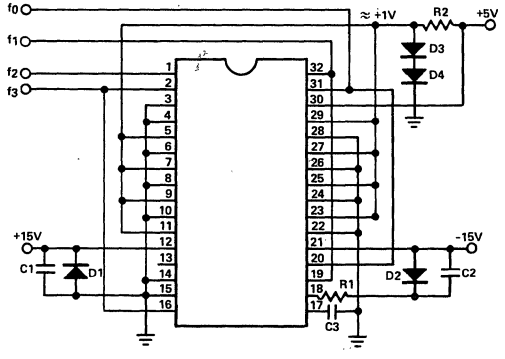


NOTES:
R1 — R12 = 4kΩ, 1/4 or 1/2 Watt, 5%
R13 = 10kΩ, 1/4 or 1/2 Watt, 5% (One Each Per Board)
R14 = 1kΩ, 1/4 or 1/2 Watt, 5% (One Each Per Board)
C1, C2, C3 = .01μF (One Each Per Socket)
C4 = 100μF (One Each Per Board)
D1, D2, D3 = IN4002 (One Each Per Board)
VIN = 1kHz Triangular Wave, ±5V
Q1 = 2N2222 (One Each Per Board)
(Short Boards, PC Layout Only. Do Not Hand Wire)

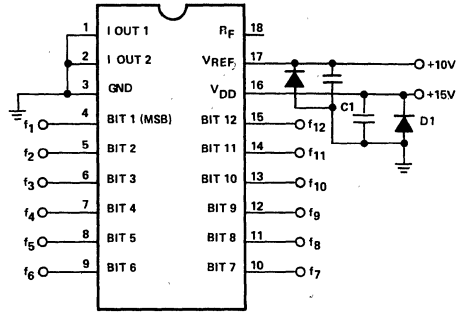
52 HI-5900



53 HI-5901



54 HI-7541



NOTES:
C1 = .01μF, D1 = IN4002
f1 = 100kHz, f2 = 50kHz, f3 = 25kHz, f4 = 12.5kHz, f5 = 6.25kHz, f6 = 3.125kHz, f7 = 1.56kHz, f8 = .78kHz, f9 = .390kHz, f10 = .195kHz, f11 = .098kHz, f12 = .049kHz, 50% Duty Cycle, Square Wave, TTL Level (0-5V), (For Static Configuration Tie f1 — f12 to +5V)

Packaging

Harris Analog Package Selection Guide

PART NO.	PACKAGE CONFIGURATION (See Note)				
	CAN	PLASTIC	CERDIP	SIDE BRAZE	LEADLESS CHIP CARRIER
HA-1608	R	G	L		
HA-2400/04/05				B	
HA-2420/25		H	D		X
HA-2500/02/05	R	G	L		
HA-2510/12/15	R	G	L		
HA-2520/22/25	R	G	L		
HA-2530/35	R				
HA-2539		H	D		X
HA-2540		H	D		
HA-2600/02/05	R	G	L		
HA-2620/22/25	R	G	L		
HA-2630/35	V				
HA-2640/45	R		L		
HA-2650/55	R	G	L		
HA-2720/25	R		L		
HA-2730/35			D		
HA-2740		J	E		
HA-4156		H	D		
HA-4600/02/05		H	D		
HA-4620/22/25		H	D		
HA-4741		H	D		X
HA-4900/02/05			E		X
HA-5062	R	G	L		
HA-5064		H	D		
HA-5082	R	G	L		
HA-5084		H	D		
HA-5100/05	R	G	L		
HA-5110/15	R	G	L		
HA-5130/35	R	G	L		X
HA-5160/62	R				
HA-5170	R	G	L		X
HA-5190/95	V		D		
HA-8023		J	E		
HC-5502			M		
HC-5510			M		
HC-5511		*			
HC-5512/5512A			E		
HC-55516				A	
HD-0165			M		
HI-200	T	H	D		
HI-201		J	E		X
HI-201HS		J	E		
HI-300/301/304/305	T	H	D		

NOTE: "Package Configuration" references drawings on the following pages. Package designations to be used in constructing the part number are explained in the Ordering Information in the Part number guide.

Plastic DIP packages are not available for military temperature range.

Consult factory for information on ordering and availability of products with package configurations other than those indicated in the chart.

Solder-dipped parts add +0.003 inches to "dimension B" in plastic DIP and "dimension G" in metal cans.

* Contact factory for packaging.

Harris Analog Package Selection Guide (continued)

PART NO.	PACKAGE CONFIGURATION (See Note)				
	CAN	PLASTIC	CERDIP	SIDE BRAZE	LEADLESS CHIP CARRIER
HI-302/303/306/307		H	D		
HI-381/384/387/390					
381/387	T	J	E		
384/390		J	E		
HI-506/507		P	N		Y
HI-506A/507A		P	N		Y
HI-508/509		J	E		X
HI-508A/509A		J	E		X
HI-516		P	N		Y
HI-518		K	F		
HI-524		K	F		
HI-539		J	E		
HI-562A				C	Y
HI-1818A/1828A		J	E		
HI-5040 thru 5051		J	E		
HI-5043/5045			E		X
HI-5610				C	
HI-5618A/18B		K	F		
HI-5712/12A	(MC) LCC's on Ceramic Substrate				
HI-5900	(MB) LCCs on Ceramic Substrate				
HI-5901	(MB) LCCs on Ceramic Substrate				
HI-7541		K		Z	X
HV-1000/05/10		J			
LF353	R	G	L		
LF155/155A/355/355A/355B	R	G	L		
LF156/156A/356/356A/356B	R	G	L		
LF157/157A/357/357A/357B	R	G	L		
LF347		D	H		
LM108/308	R	G	L		
LM108A/308A	R	G	L		
LM118/318	R	G	L		
LM118A/318A	R	G	L		
LM143/343	R	G	L		
LM143A/343A	R	G	L		
LM146/346		J	E		
LM148/348		H	D		
LM148A/348A		H	D		
LM1458/1558A	R	G	L		
LM2908		H	D		
LM4250/4250C	R	G	L		
OP-07	R	G	L		

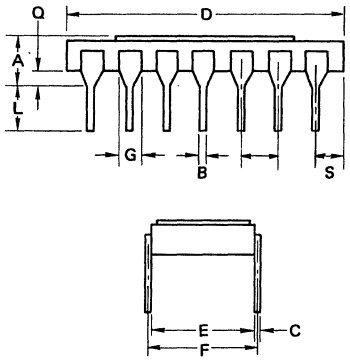
NOTE: "Package Configuration" references drawings on the following pages. Package designations to be used in constructing the part number are explained in the Ordering Information in the Part number guide.

Plastic DIP packages are not available for military temperature range.

Consult factory for information on ordering and availability of products with package configurations other than those indicated in the chart.

Solder-dipped parts add +0.003 inches to "dimension B" in plastic DIP and "dimension G" in metal cans.

A B Z D TYPE SIDE BRAZED CERAMIC

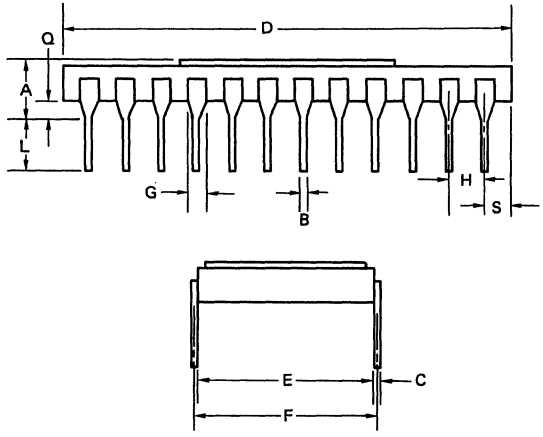


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S
A	14	– / .200	.014 / .023	.008 / .015	– / .785	.220 / .310	.290 / .320	.030 / .070	.100 / BSC	.125 / .200	.015 / .060	– / .098
B	16	– / .200	.014 / .023	.008 / .015	– / .840	.220 / .310	.290 / .320	.030 / .070	.100 / BSC	.125 / .200	.015 / .060	– / .098
Z	18	– / .200	.014 / .023	.008 / .015	– / .950	.220 / .310	.290 / .320	.030 / .070	.100 / BSC	.125 / .200	.015 / .060	– / .098

NOTE: MIN. / MAX.

DIMENSIONS IN INCHES

C D TYPE SIDE BRAZED CERAMIC



PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S
C	24	– / .225	.014 / .023	.008 / .015	– / 1.290	.500 / .610	.590 / .620	.030 / .070	.100 / BSC	.120 / .200	.015 / .075	– / .098

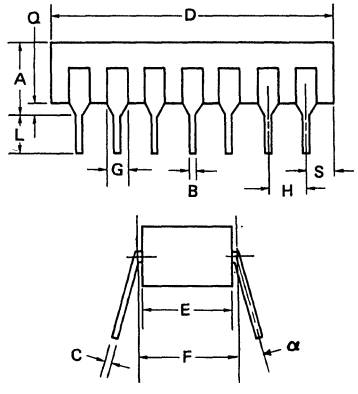
NOTE: MIN. / MAX.

DIMENSIONS IN INCHES

D E F J TYPE CERDIP DUAL-IN-LINE

G H J K N TYPE PLASTIC DUAL-IN-LINE

L J-8 TYPE 8 PIN MINI-CERDIP



PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
G, L	8	– / .200	.014 / .023	.008 / .015	– / .395	.220 / .310	.290 / .320	.030 / .070	.100 / BSC	.125 / .200	.015 / .060	– / .060	0° / 15°
D, H	14	– / .200	.014 / .023	.008 / .015	– / .790	.220 / .310	.290 / .320	.030 / .070	.100 / BSC	.125 / .200	.015 / .060	– / .098	0° / 15°
E, J	16	– / .200	.014 / .023	.008 / .015	– / .790	.220 / .310	.290 / .320	.030 / .070	.100 / BSC	.125 / .200	.015 / .060	– / .060	0° / 15°
F, K	18	– / .200	.014 / .023	.008 / .015	– / .950	.220 / .310	.290 / .320	.030 / .070	.100 / BSC	.125 / .200	.015 / .060	– / .060	0° / 15°

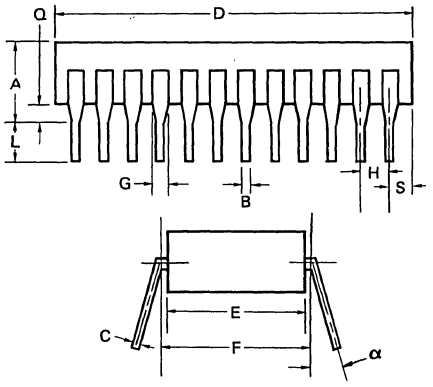
NOTE: MIN. / MAX.

DIMENSIONS IN INCHES

11

M N J TYPE CERDIP DUAL-IN-LINE

P N TYPE PLASTIC DUAL-IN-LINE

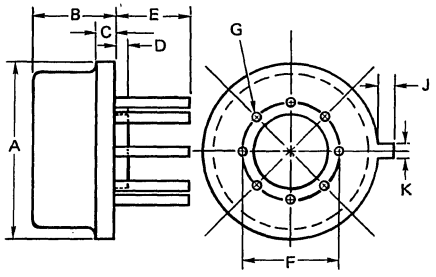


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H	DIM. L	DIM. Q	DIM. S	DIM. α
M	24	– / .225	.014 / .023	.008 / .015	– / 1.290	.500 / .610	.590 / .620	.030 / .070	.100 / BSC	.120 / .200	.015 / .075	– / .098	0° / 15°
N, P	28	– / .225	.014 / .023	.008 / .015	– / 1.490	.500 / .610	.590 / .620	.030 / .070	.100 / BSC	.120 / .200	.015 / .075	– / .098	0° / 15°

NOTES: MIN. / MAX.

DIMENSIONS IN INCHES

R T H TYPE METAL CAN, TO-99 (8 PIN) OR TO-100 (10 PIN)

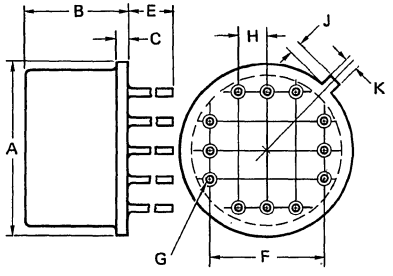


PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. J	DIM. K
R	8	.335 / .370	.165 / .185	– / .040	.010 / .045	.500 / .550	.200 / BSC	.016 / .021	.027 / .045	.027 / .034
T	10	.335 / .370	.165 / .185	– / .040	.010 / .045	.500 / .550	.230 / BSC	.016 / .021	.027 / .045	.027 / .034

NOTE: MIN. / MAX.

DIMENSIONS IN INCHES

V H TYPE METAL CAN, TO-8
(HA-5190/95 AND HA-2630/35 ONLY)



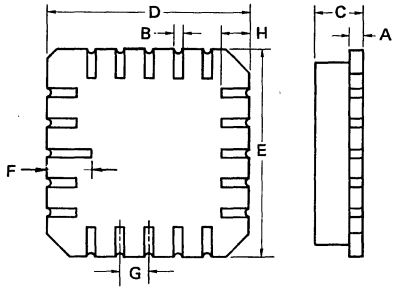
PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. E	DIM. F	DIM. G	DIM. H	DIM. J	DIM. K
V	12	.585 / .615	.130 / .150	– / .040	.500 / .550	.400 / BSC	.016 / .021	.100 / BSC	.027 / .045	.027 / .034

NOTES: MIN. / MAX.

DIMENSIONS IN INCHES

11

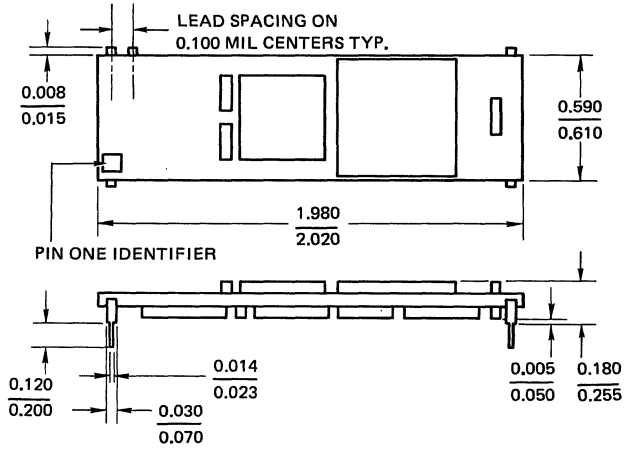
X | Y LEADLESS CARRIER



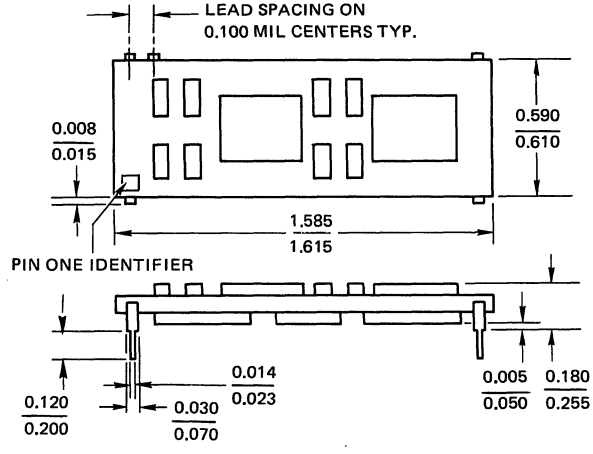
PKG. TYPE	LEAD COUNT	DIM. A	DIM. B	DIM. C	DIM. D	DIM. E	DIM. F	DIM. G	DIM. H
X	20	.017/.066	.020/.034	.064/.100	.342/.358	.342/.358	.060/0.090	.050/BSC	.040/.055
Y	28	.017/.066	.020/.034	.064/.100	.442/.458	.442/.458	.060/0.090	.050/BSC	.040/.055

NOTE: MIN./MAX. DIMENSIONS IN INCHES

MC HI-5712/12A MODULE



MB HI-5900/5901 MODULE



11

Harris Sales Locations

OEM Sales

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1 Burlington Woods Drive
Burlington, MA 01803
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Melville, L.I., N.Y. 11747
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Suite 1101
996 Old Eagle School Road
Wayne, PA 19087
(215) 687-6680

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Dallas, TX 75248
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Dayton, OH 45429
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P.O. Box 1649
Beaverton, OR 97075
(503) 297-7621

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P.O. Box 3796
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Suite 205
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Scottsdale, AZ 85261
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Europe

HEADQUARTERS

Harris GmbH
Semiconductor Group
Einsteinstrasse 127
D-8000 Munich 80
West Germany
Tel. 49-89-473047
TWX: 524126

SALES OFFICES

ENGLAND

Harris Systems Ltd.
Harris Semiconductor Div.
P.O. Box 27, 145 Farnham Rd.
Slough SLI 4XD
Tel: (Slough) 34666
TWX: 848174 HARRIS G

ITALY

Harris Italiana Inc.
20092 Cinisello Balsamo (Milano)
Via Fratelli Cracchi 48
Tel: 39-2-6187249 or
6188282
TWX: 311164 Ageris 1

WEST GERMANY

Matra-Harris Semiconducteurs
Deutschland GmbH
Erfurterstrasse 29
8057 Eching
Tel: 49-89-319-1035
TWX: 5-213-866

Harris-Matra-Harris GmbH
Walsroderstrasse 71
D-3012 Langenhagen 1
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