HD64570/HD64572

SCA Series (SCA-I SCA-II)

HITACHI

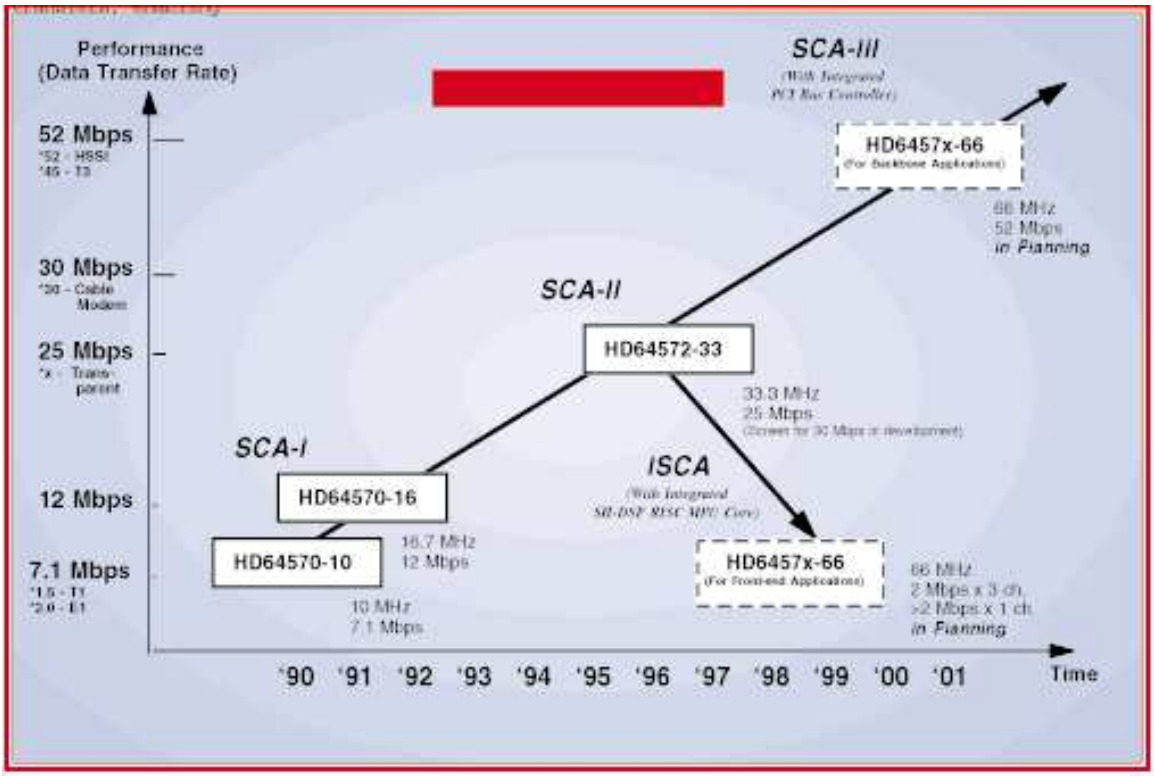
Description

The SCA Series of devices converts parallel data to serial data, and serial data to parallel data for communication with other devices. The HD64570 and HD64572 Serial Communications Adapter (SCA-I and SCA-II, respectively) peripheral chips enable a host microprocessor to perform asynchronous, byte synchronous, or bit synchronous serial communication. The SCA-II can also perform transparent communication.

Both chips have two independent full-duplex, multiprotocol serial channels that support a wide variety of communications protocols such as frame relay, HDLC, SDLC[a], X.25, LAPB, LAPD, mono sync, bisync, X.21, DDCMP, asynch, etc. Both chips also include a built-in direct memory access controller (DMAC) with deep FIFOs that can execute chained-block transfers, enabling high-speed transfers of data between an SCA device and memory. Due to the on-chip DMAC, the SCA Series can support very high data rates without monopolizing the bus, even in full-duplex communication. Other on-chip features of the SCA Series include direct MPU interfaces, a bus arbiter, timers, and an interrupt controller.

Highly optimized, the SCA Series of devices are used in a large number of datacommunication and networking applications such as bridges, routers, multiplexers, switches, frame relay exchanges, broad band and Internet access products, LAN/WAN interface cards, T1/E1 applications, fractional T3 applications, protocol converters, repeaters, frame relay over ATM applications, remote access LAN products, etc.

SDLC[a] is a trademark of International Business Machines (IBM).



SCA-I (HD64570) Features:

Data Transfer Rate:

- 50 bits/sec to 7.1 Mbits/sec (f = 10 MHz)
- 50 bits/sec to 12 Mbits/sec (f = 16.7 MHz, the high speed version)

Data and Address Bus Widths:

- Data bus: 8/16-bit
- Address bus: 24-bit

Protocol Support:

- Asynchronous (ASYNC): 5 to 8 bits + parity (odd, even, or none)
- Byte Synchronous (COP): mono synch, bisync, X.21, DDCMP, external sync modes, etc.
- Bit Synchronous (BOP): frame relay, HDLC, SDLC[a], X.25 link level (LAPB), LAPD, BOP loop, etc.

Highly Efficient Data Transfer:

- Two 32-byte FIFOs (transmit/receive) per channel

Transmission Error Detection:

- Parity (asynchronous), CRC-16, CRC-CCITT (byte and bit synchronous)

Transmission Codes:

- NRZ, NRZI, FM0, FM1, Manchester

Operating Modes:

- Normal operating mode (full-duplex), auto echo, local loop back

DMA Transfer:

- On-chip DMAC with four channels and single/chained-block transfer capability
- DMA transfer rate (max.) at 10 MHz: 11.1 MBytes/sec
- DMA transfer rate (max.) at 16.7 MHz:
  18.4 MBytes/sec

Address Space:

- 16 MBytes

MPU Bus Interface:

- Connects to 64180, 80x86, and 680x0 systems;
  8/16-bit MPU systems

Timers:

- On-chip timers with four 16-bit channels
- Time-out detection, etc.

Power Supply:

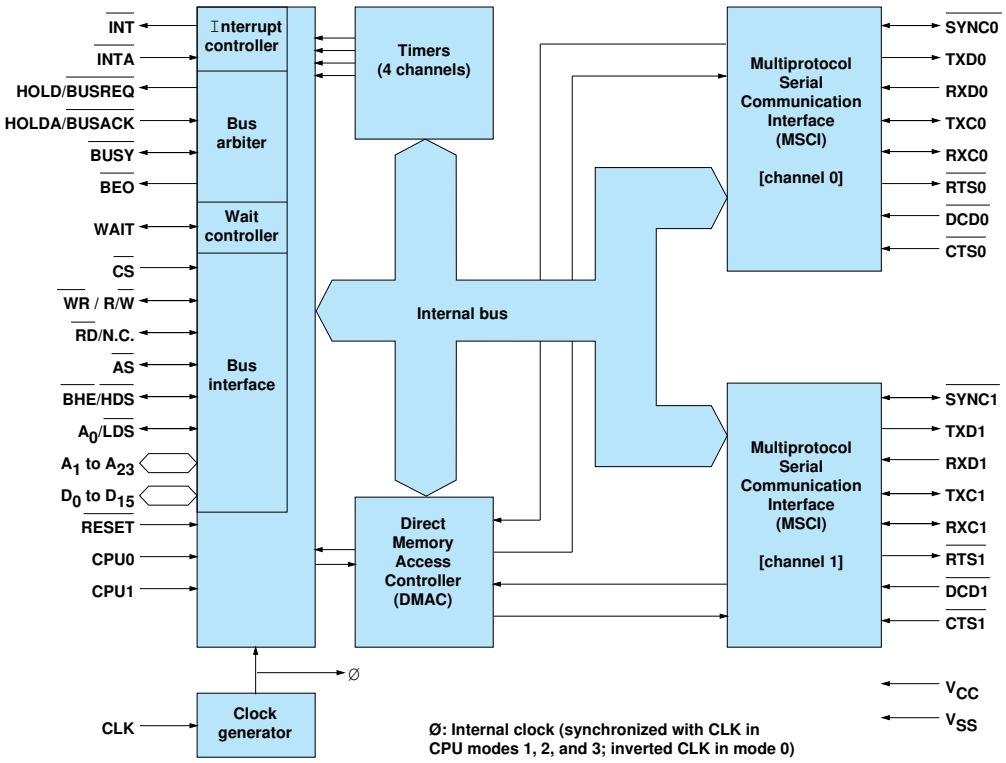
- 5V +/- 10% (-20ûC to +75ûC) for the 10 MHz chip
- 5V +/- 5% (0 to +70ûC) for the 16.7 MHz chip

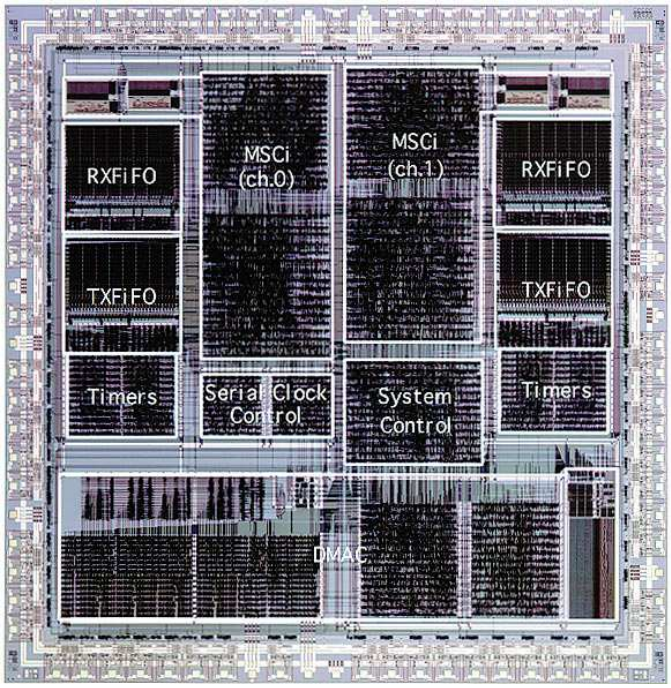
Process Technology:

- 1.0µm CMOS

Packaging:

- 84-pin PLCC (CP-84)
- 88-pin QFP (FP-88)





SCA-II (HD64572) Features:

Data Transfer Rate:

- 50 bits/sec to 25 Mbits/sec (f = 33.3 MHz)
- 50 bits/sec to 30 Mbits/sec (f = 33.3 MHz, the high-speed version)

Data and Address Bus Widths:

- Data bus: 32-bit
- Address bus: 32-bit

Protocol Support:

- Asynchronous (ASYNC): 5 to 8 bits + parity (odd, even, or none)
- Byte Synchronous (COP): mono synch, bisync, X.21, DDCMP, external sync modes, etc.
- Bit Synchronous (BOP): frame relay, HDLC, SDLC[a], X.25 link level (LAPB), LAPD, BOP loop, etc.
- Transparent: T-1 multiplexer, ATM

Highly Efficient Data Transfer:

- Two 64-byte FIFOs (transmit/receive) per channel

Transmission Error Detection:

- Parity (asynchronous), CRC-16, CRC-CCITT, CRC-32 (byte and bit synchronous)

Transmission Codes:

- NRZ, NRZI, NRZI (IEEE), FM0, FM1, Manchester

Operating Modes:

- Normal operating mode (full-duplex), auto echo, local loop back (two types)

DMA Transfer:

- On-chip DMAC with four channels and single/chained-block transfer capability
- DMA transfer rate (max.) at 33.3 MHz: 66.6 MBytes/sec

Address Space:

- 4 GBytes

MPU Bus Interface:

- Connects to 80x86 (two types*), 680x0, and RISC systems; 32-bit MPU systems

* Note: The SCA-IIÕs 8086 bus interface control signals correspond to those of the 8086 CPU, but both the address bus and the data bus are 32-bits wide.

Timers/Counters:

- On-chip timers with four 16-bit channels
- Time-out detection, etc.
- Count occurrences of various kinds of MSCI status (interrupt sources)
- Count EOMs and transmission errors detected (underrun frames, overrun frames, CRC error frames, etc.)

Power Supply:

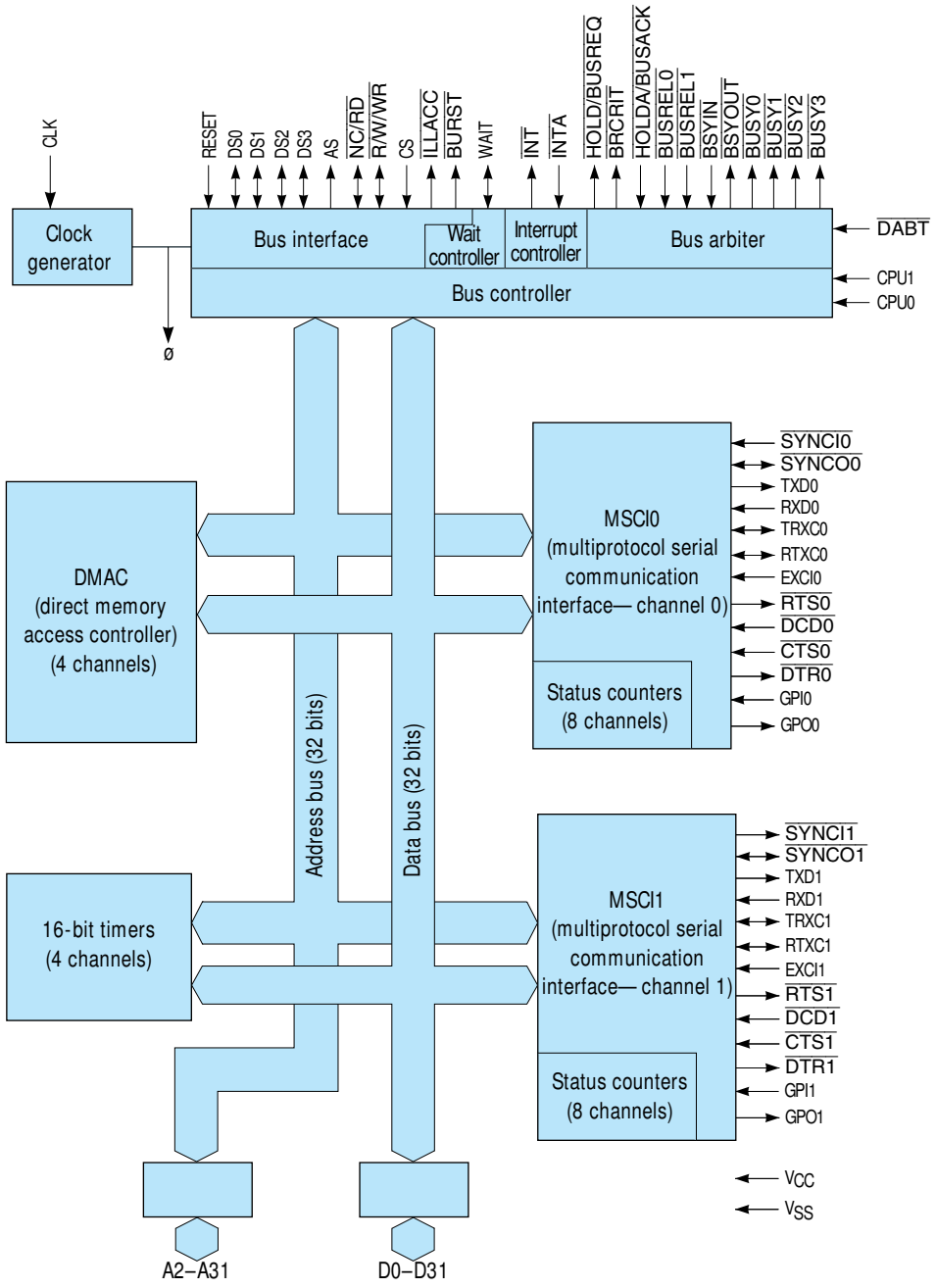
- 5V +/- 5% (-20ûC to +75ûC)

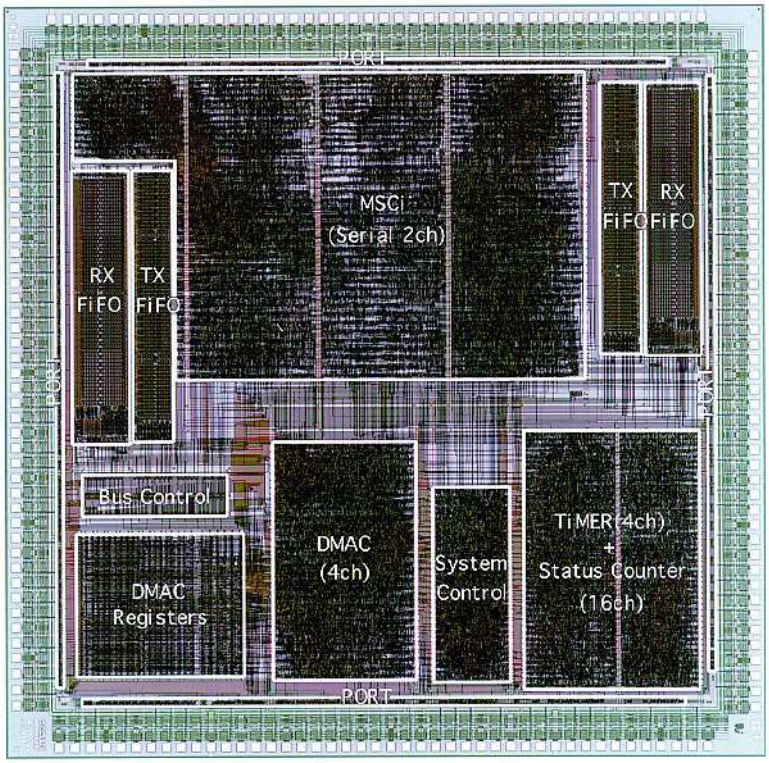
Process Technology:

- 0.6µm CMOS

Packaging:

- 176-pin LQFP (FP-176)


CLK
RESET
DS0
DS1
DS2
DS3
AS
NC/RD
R/W/WR
CS
ILLACC
BURST
WAIT
INT
INTA
HOLD/BUSREQ
BRCRIT
HOLDA/BUSACK
BUSREL0
BUSREL1
BSYIN
BSYOUT
BUSY0
BUSY1
BUSY2
BUSY3
Clock generator
Bus interface
Wait controller
Interrupt controller
Bus arbiter
Bus controller
DABT
CPU1
CPU0
ø
DMAC (direct memory access controller) (4 channels)
16-bit timers (4 channels)
Address bus (32 bits)
Data bus (32 bits)
MSCI0 (multiprotocol serial communication interface— channel 0)
Status counters (8 channels)
SYNCI0
SYNCO0
TXD0
RXD0
TRXC0
RTXC0
EXCI0
RTS0
DCD0
CTS0
DTR0
GPI0
GPO0
MSCI1 (multiprotocol serial communication interface— channel 1)
Status counters (8 channels)
SYNCI1
SYNCO1
TXD1
RXD1
TRXC1
RTXC1
EXCI1
RTS1
DCD1
CTS1
DTR1
GPI1
GPO1
VCC
VSS
A2–A31
D0–D31



Literature

SCA-I (HD64570) UserÕs Manual: PMHKSTH001D2

- Includes User's Manual, Application Note and Technical Q&A

SCA-II Evaluation/Demo Board Support

SCA-II Engineering Design Kit (EDK)

Please contact Marketing for availability!

- Hitachi SCA-II (HD64572)
- V3 Semiconductor PCI Bus Controller (V292PBC)
- Gcom demonstration software with drivers
- Windows¨ 95 and Windows¨ NT support

Software Support

Gcom, Inc.
1800 Woodfield Drive
Savoy, IL 61874
Phone: (217) 351-4241
Web Site Address:
www.gcom.com

SDL Communications
46 Eastman Street
Easton, MA 02334
Phone: (508) 238-4490
Web Site Address:
www.sdlcomm.com

Ordering Information SCA Series (HD64570 and HD64572)

Series	Part Number	Maximum Operating Frequency	Maximum Data Transfer	Operating Voltage	Package Type* PLCC	QFP	LQFP
SCA-I	HD64570CP HD64570F	10 MHz	7.1 Mbits/sec	+5V +/- 10% (-20ûC to +75ûC)	84	88	
High Speed SCA-I	HD64570CP16 HD64570F16	16.7 MHz	12 Mbits/sec	+5V +/- 5% (0 to +70ûC)	84	88	
SCA-II	HD64572FL33	33.3 MHz	25 Mbits/sec	+5V +/- 5%(-20ûC to +75ûC)			176
High-Speed	HD64572AFL33	33.3 MHz	30 Mbits/sec	+5V +/- 5%			176

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