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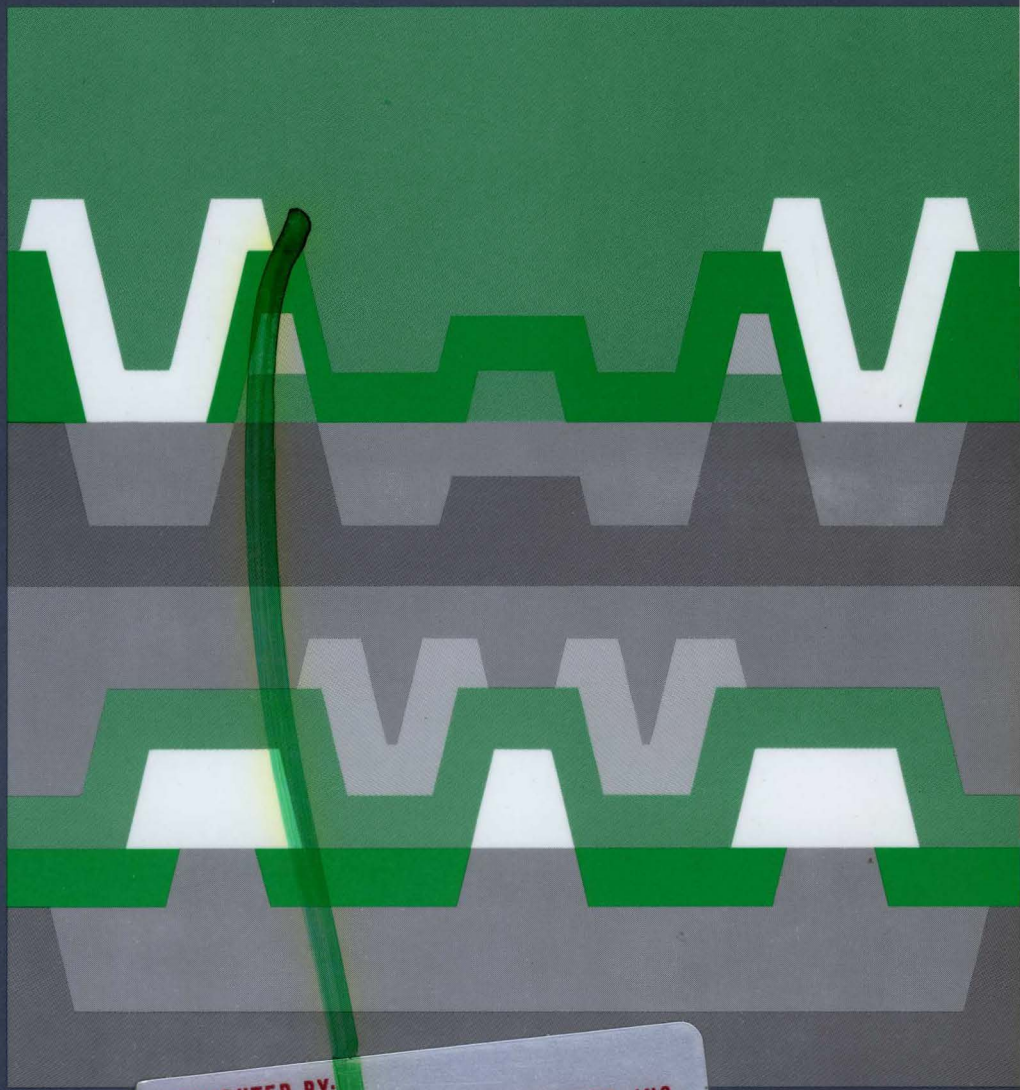
SRAM DATA BOOK



#M18

SRAM
DATA BOOK

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March 1990

Printed in U.S.A.

SRAM DATA BOOK
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Introduction

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- Reliability of Hitachi I.C. Memories
- Quality Assurance of I.C. Memory
- Outline of Testing Method
- Application

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QUICK REFERENCE GUIDE TO HITACHI MEMORIES

■ MOS RAM

Mode	Total	Type No.	Process	Organization (word × bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static	16k-b	HM6116-2*2	CMOS	2048 × 8	120	120	+5	0.1m/0.2	24		●	●							64
		HM6116-3*2			150	150		0.1m/0.175			●	●							64
		HM6116-4*2			200	200					●	●							64
		HM6116L-2*2			120	120		10μ/0.175			●	●							64
		HM6116L-3*2			150	150		10μ/0.15			●	●							64
		HM6116L-4*2			200	200					●	●							64
		HM6116A-12*2			120	120		0.1m/15m			●		●						69
		HM6116L-15*2			150	150					●		●						69
		HM6116A-20*2			200	200					●		●						69
		HM6116AL-12*2			120	120		5μ/10m			●		●						69
		HM6116AL-15*2			150	150					●		●						69
		HM6116AL-20*2			200	200					●		●						69
		HM6716-25	Bi-CMOS	2048 × 8 (with OE)	25	25		0.28					●						74
		HM6716-30			30	30							●						74
		HM6719-25			25	25							●						74
		HM6719-30			30	30							●						74
		HM6268-25	CMOS	4096 × 4	25	25		0.1μ/0.25	20		●								80
		HM6268-35			35	35					●								80
		HM6268-45			45	45					●								80
		HM6268L-25			25	25		5μ/0.25			●								80
		HM6268L-35			35	35					●								80
		HM6268L-45			45	45					●								80
		HM6267-35		16384 × 1	35	35		0.1m/0.2			●								87
		HM6267-45			45	45					●								87
		HM6267-55			55	55					●								87
		HM6267L-35			35	35		5μ/0.2			●								87
		HM6267L-45			45	45					●								87
		HM6267L-55			55	55					●								87
	18k-b	HM6719-25	Bi-CMOS	2048 × 9	25	25		0.28	24				●						74
		HM6719-30			30	30							●						74
	16k-b	HM6264-10*2	CMOS	8192 × 8	100	100		0.1m/0.2	28		●	●							94
		HM6264-12*2			120	120					●	●							94
		HM6264A-10			100	100		0.1m/15m			●	●	●						94
		HM6264A-12			120	120					●	●	●						94
		HM6264A-15			150	150					●	●	●						94
		HM6264AL-10			100	100		10μ/15m			●	●	●						94
		HM6264AL-12			120	120					●	●	●						94
		HM6264AL-15			150	150					●	●	●						94
		HM6264AL-10L			100	100		10μ/15m			●	●	●						94
		HM6264AL-12L			120	120					●	●	●						94
		HM6264AL-15L			150	150					●	●	●						94
		HM6288-25		16384 × 4	25	25		0.1m/0.3	22 24 (SOJ)				●				●		103
		HM6288-35			35	35							●				●		103
		HM6288L-25			25	25							●				●		103
		HM6288L-35			35	35							●				●		103
		HM6788-25	Bi-CMOS		25	25		10m/0.23	22				●						111
		HM6788-35			35	35							●						111
		HM6788H-20			20	20		0.28					●						115
		HM6788HA-12			12	12		.3					●						119
		HM6788HA-15			15	15							●						119
		HM6788HA-20			20	20							●						119
	64k-b	HM6289-25	CMOS	16384 × 4 (with OE)	25	25		0.1m/0.3	24								●		124
		HM6289-35			35	35											●		124
		HM6289L-25			25	25											●		124
		HM6289L-35			35	35											●		124

(continued)

■ MOS RAM

Mode	Total	Type No.	Process	Organization (word × bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static	256k-b	HM6789-25	Bi-CMOS	16384 × 4 (with $\overline{OE}$)	25	25	+5	10μ/0.23	24				●				●		135
		HM6789-30			30	30							●				●		135
		HM6789H-15			15	15		0.28					●				●		142
		HM6789H-20			20	20							●				●		142
		HM6789HA-12			12	12							●				●		149
		HM6789HA-15			15	15							●				●		149
		HM6789HA-20			20	20							●				●		149
		HM6287-45	CMOS	65536 × 1	45	45		0.1m/0.3	22				●						157
		HM6287-55			55	55							●						157
		HM6287-70			70	70							●						157
		HM6287L-45			45	45		10μ/0.3					●						157
		HM6287L-55			55	55							●						157
		HM6287L-70			70	70							●						157
		HM6287H-25			25	25		0.1m/0.3	22 24 (SOJ)				●				●		164
		HM6287H-35			35	35							●				●		164
		HM6287HL-25			25	25		10μ/0.3					●				●		164
		HM6287HL-35			35	35							●				●		164
		HM6787-25	Bi-CMOS		25	25		38m/0.18					●						173
		HM6787-35			35	35							●						173
		HM6787H-15			15	15		0.21					●				●		178
		HM6787H-20			20	20							●				●		178
		HM6787HAJP-12			12	12		.3					●				●		178
		HM6787HAJP-15			15	15							●				●		183
		HM6787HAJP-20			20	20							●				●		183
		HM62256-8	CMOS	32768 × 8	85	85		0.2m/40m	28		●	●							189
		HM62256-10			100	100					●	●							189
		HM62256-12			120	120					●	●							189
		HM62256-15			150	150					●	●							189
		HM62256L-8			85	85		10μ/40m			●	●							189
		HM62256L-10			100	100					●	●							189
		HM62256L-12			120	120					●	●							189
		HM62256L-15			150	150					●	●							189
		HM62256L-10SL			100	100		10μ/40m			●	●							189
		HM62256L-12SL			120	120					●	●							189
		HM62256L-15SL			150	150					●	●							189
		HM62832-35			35	35		75m/.3					●				●		197
		HM62832-45			45	45							●				●		197
		HM62832L-35			35	35		10m/.3					●				●		197
		HM62832L-45			45	45							●				●		197
		HM62832H-25			25	25		.1m/.3					●				●		197
		HM62832H-35			35	35							●				●		197
		HM62832H-45			45	45							●				●		197
		HM62832HL-25			25	25		30m/.3					●				●		197
		HM62832HL-35			35	35							●				●		197
		HM62832HL-45			45	45							●				●		197
		HM6208-35	CMOS	65536 × 4	35	35		0.1m/0.3	24		●								203
		HM6208-45			45	45					●								203
		HM6208L-35			35	35		10μ/0.3			●								203
		HM6208L-45			45	45					●								203
		HM6208H-25			25	25		0.1m/0.3					●				●		203
		HM6208H-35			35	35							●				●		203
		HM6208HL-25			25	25		10μ/0.3					●				●		203
		HM6208HL-35			35	35							●				●		203
		HM6708-20*3	Bi-CMOS		20	20		0.35					●				●		211
		HM6708-25*3			25	25							●				●		211
		HM6708A-15			15	15		.4				●				●			217
		HM6708A-20			20	20						●				●			217
		HM6708A-25			25	25						●				●			217
		HM6709-20			20	20		.35	28								●		222
		HM6709-25			25	25											●		222
		HM6709A-15			15	15		.4					●				●		229
		HM6709A-20			20	15							●				●		229
		HM6709A-25			25	25							●				●		229

(continued)

■ MOS RAM

Mode	Total	Type No.	Process	Organization (word × bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1 Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	Page
Static	256k-b	HM6207-35	CMOS	262144 × 1	35	35	+5	0.1m/0.3	24				●						236
		HM6207-45			45	45							●						236
		HM6207L-35			35	35		10μ/0.3					●						236
		HM6207L-45			45	45							●						236
		HM6207H-25			25	25		0.1m/0.3					●				●		243
		HM6207H-35			35	35							●				●		243
		HM6207HL-25			25	25		10μ/0.3					●				●		243
		HM6207HL-35			35	35							●				●		243
		HM6707-20*3	Bi-CMOS		20	20		0.35					●				●		250
		HM6707-25*3			25	25							●				●		250
		HM6707A-15			15	15		.4					●				●		255
		HM6707A-20			20	20							●				●		255
		HM6707A-25			25	25							●				●		255
	1M-b	HM628128-7*3	CMOS	131072 × 8	70	70		0.1m/75m	32		●	●							261
		HM628128-8*3			85	85					●	●							261
		HM628128-10*3			100	100					●	●							261
		HM628128-12*3			120	120					●	●							261
		HM628128L-7*7			70	70		10μ/75m			●	●							261
		HM628128L-8*7			85	85					●	●							261
		HM628128L-10*7			100	100					●	●							261
		HM628128L-12*7			120	120					●	●							261
		HM624256-35*3		Z62144 × 4	35	35		0.1m/0.35	28				●				●		269
		HM624256-45*3			45	45							●				●		269
		HM624256L-35*3			35	35		.1m/.35					●				●		269
		HM624256L-45*3			45	45							●				●		269
		HM624257-35*4			35	35		0.1m/0.35	32								●		275
		HM624257-45*4			45	45											●		275
		HM624257L-35*4			35	35											●		275
		HM624257L-45*4			45	45											●		275
Static RAM Module		HM66204-12*4		131072 × 8 (with decoder)	120	120		0.8m/50m										●	283
		HM66204-15*4			150	150												●	283
		HM66204L-12*4			120	120		40μ/50m										●	283
		HM66204L-15*4			150	150												●	283
FIFO	18k-b	HM63921-20		2k × 9	20	30		1.0W max.	28		●								289
		HM63921-25			25	35					●								289
		HM63921-35			35	45					●								289
	36k-b	HM63941-25		4k × 9	25	35					●								289
		HM63941-35			35	45					●								289
		HM63941-45			45	60					●								289
Cache Static RAMs	120k-b	HM62A168-25		8k × 16 (2 way)	25	25		1.1 (max.)	52							●			311
		HM62A168-35			35	35										●			311
		HM62A168-45			45	45										●			311
	128k-b	HM62A188-25		8k × 18 (2 way)	25	25										●			311
		HM62A188-35			35	35										●			311
		HM62A188-45			45	45										●			311
	256k-b	HM67C932-20	Bi-CMOS	32k × 9 (4 way)	20	20		TBD	44							●			319
		HM67C932-25			25	25										●			319
		HM67B932-20			20	20										●			†
		HM67B932-25			25	25										●			†
Fast SRAM Module	1M-b	HB66B1616A-25	CMOS	16k × 16 (module)	25	25		.4m/1.2	36									●	333
		HB66B1616A-35			35	35												●	333
	2M-b	HB66A2568A-25		256k × 8 (module)	25	25		.8m/2.4	60									●	343
		HB66A2568A-35			35	35												●	343
TAG RAM	32k-b	HM644332-25		2k × 20 (tag ram)	25	25		1.0 max.	64										351
		HM644332-30			30	30													351

†Data sheet not included in this manual. Request data sheet for HM67B932.

(continued)

■ MOS RAM

Mode	Total	Type No.	Process	Organization (word × bit)	Access Time (ns) Max	Cycle Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1										Page
									Pin No.	G	P	FP	SP	ZP	CG	CP	JP	M	
Pseudo Static	256k-b	HM65256B-10		32768 × 8	100	100		2m/0.175	28		●	●	●						369
		HM65256B-12			120	190					●	●	●						369
		HM65256B-15			150	235					●	●	●						369
		HM65256B-20			200	310					●	●	●						369
		HM65256BL-10			100	180					●	●	●						369
		HM65256BL-12			120	190					●	●	●						369
		HM65256BL-15			150	235					●	●	●						369
		HM65256BL-20			200	310					●	●	●						369
		HM658128D-10		131072 × 8	100	180		5m/0.2	32		●	●							376
		HM658128D-12			120	210					●	●							376
		HM658128D-15			150	250					●	●							376
		HM658128L-10			100	180		0.5m/0.2			●	●							376
		HM658128L-12			120	210					●	●							376
		HM658128L-15			150	250					●	●							376

■ ECL RAM

Level	Total Bit	Type No.	Organization (word × bit)	Output	Access Time (ns) Max	Supply Voltage (V)	Power Dissipation (W)	Package *1					Page
								Pin No.	G	F	CG	JP	
ECL 10K	64k-bit	HM10494-10	16384 × 4	Open	10	-5.2	0.8	28	●	●			388
		HM10494-12			12				●	●			388
		HM10490-10	65536-1		10		.57	22	●	●			393
		HM10490-12			12				●	●			393
	256k-bit	HM10504-10	65536 × 4		10		.50	28		●			397
		HM10504-12			12					●			397
		HM10500-15*3	262144 × 1	Emitter	15		0.52	24	●				399
ECL100K	64k-bit	HM100494-10*4	16384 × 4		10	-4.5	0.65	28	●	●		●	403
		HM100494-12*4			12				●	●		●	403
		HM100490-10	65536 × 1		15		0.57	22	●	●		●	407
		HM100490-12			20				●	●		●	407
		HM100490-15							●	●		●	407
	256k-bit	HM100504F-10	65536 × 4		10		.50	28		●			411
		HM100504F-12			12					●			411
		HM100500-18*3	262144 × 1		18		0.5	24/28	●	●	●		412
	64k-bit	HM101494-10	16384 × 4		10	5.2	.75	28	●	●			415
		HM101494-12			12				●	●			415
		HM101490-10	65536 × 1		10		.57	22	●	●			419
		HM101490-12			12				●	●			419
		HM101504-10			10					●			423
		HM10504-12			12					●			423
		HM101500-15*3					.50	24		●			425

Notes) *1. The package codes of G, F and CG and applied to the package material as follows.
G; cerdip, F; Flat Package, CG; Ceramic Leadless Chip Carrier
*2. Maintenance Only. This device is not available for new application.
*3. Preliminary
*4. Under Development

Package Information

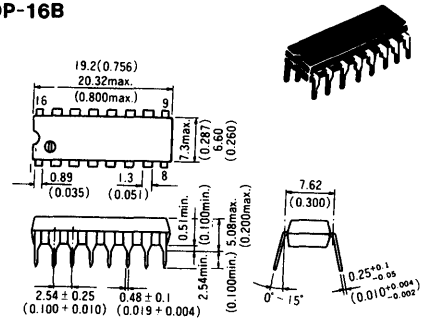
HITACHI®

■ PACKAGE INFORMATION

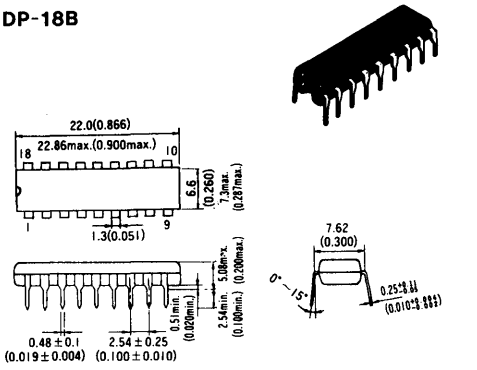
● Dual-in-line Plastic

Unit: mm (inch) Scale 1/1

●DP-16B



●DP-18B



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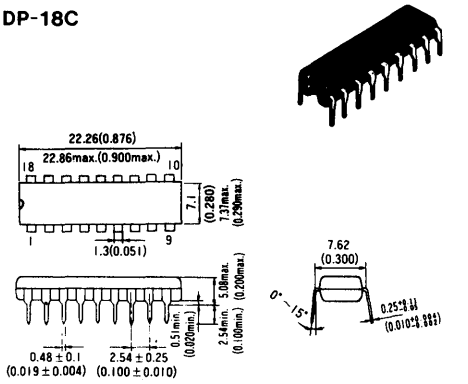

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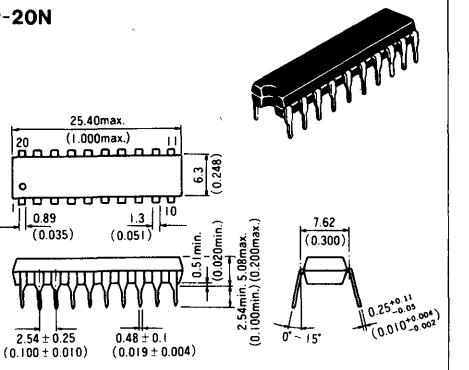

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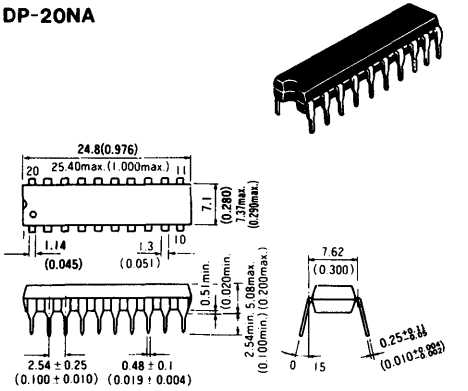

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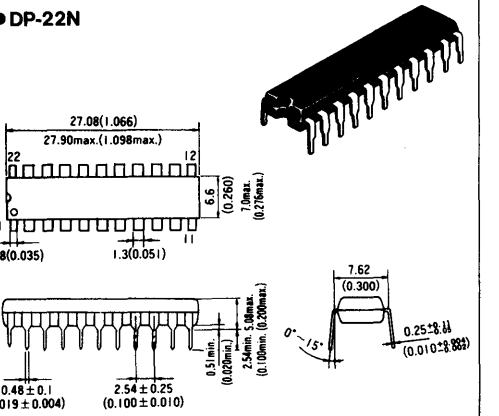
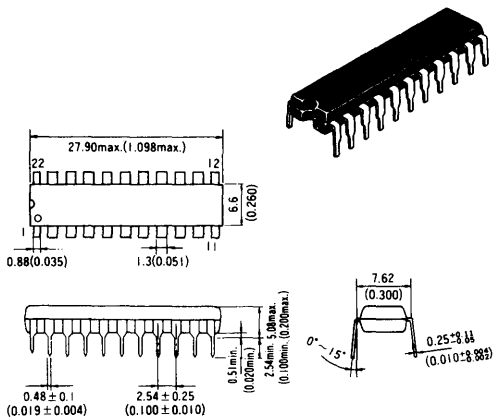


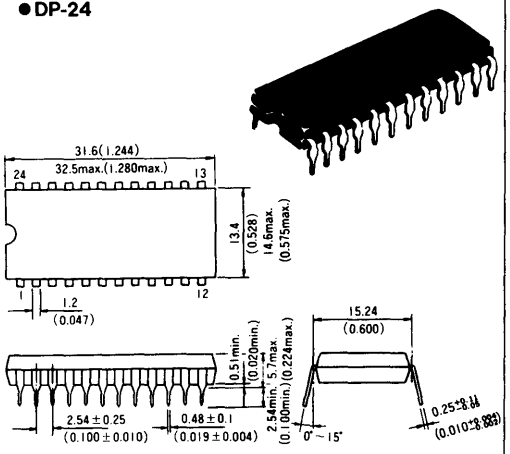
● Dual-in-line Plastic

Unit: mm (inch) Scale 1/1

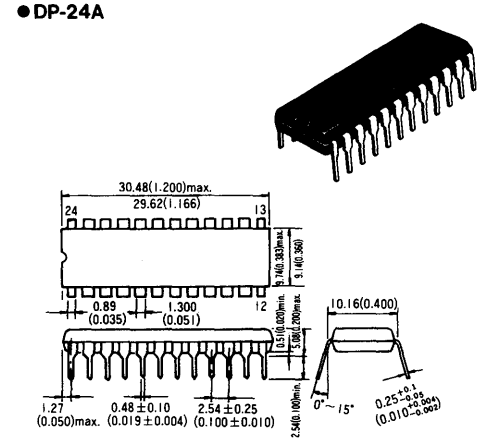
● DP-22NB



● DP-24



● DP-24A



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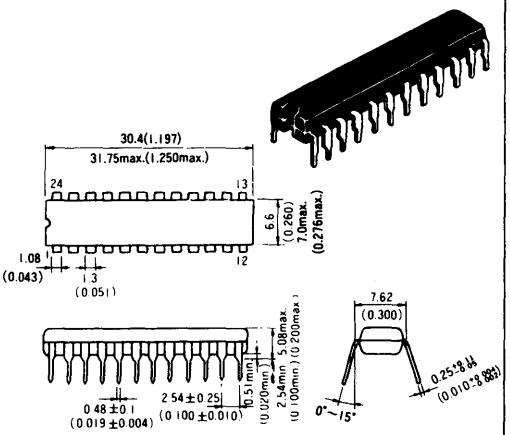

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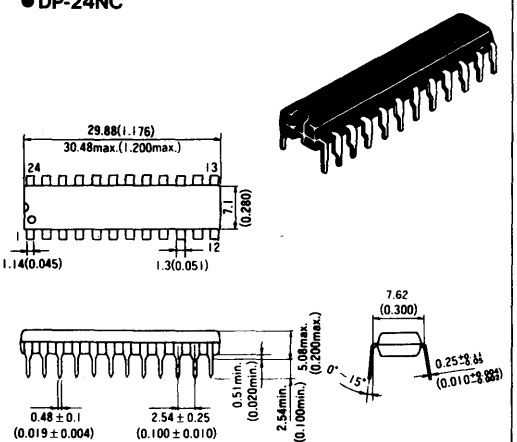
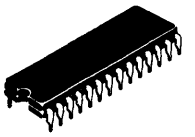
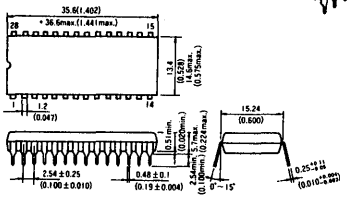


● Dual-in-line Plastic

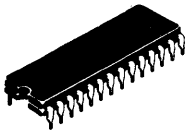
Unit: mm (inch) Scale 1/1

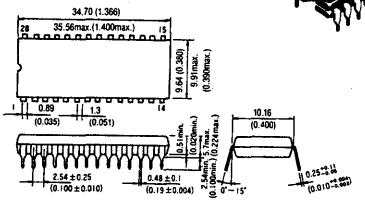
● DP-28



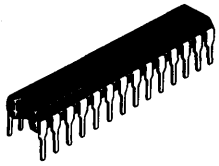


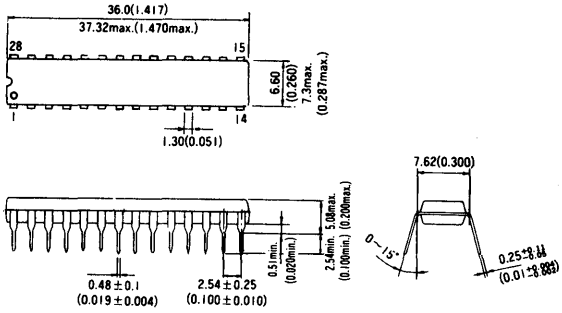
● DP-28C



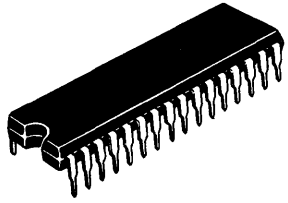


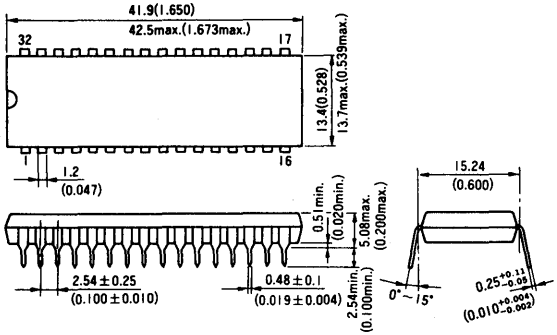
● DP-28N



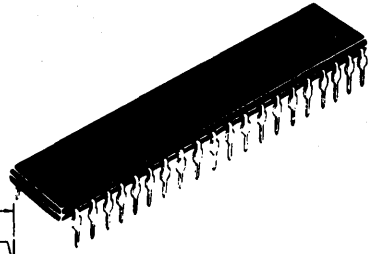


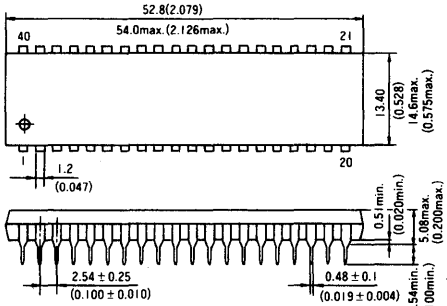
● DP-32





● DP-40

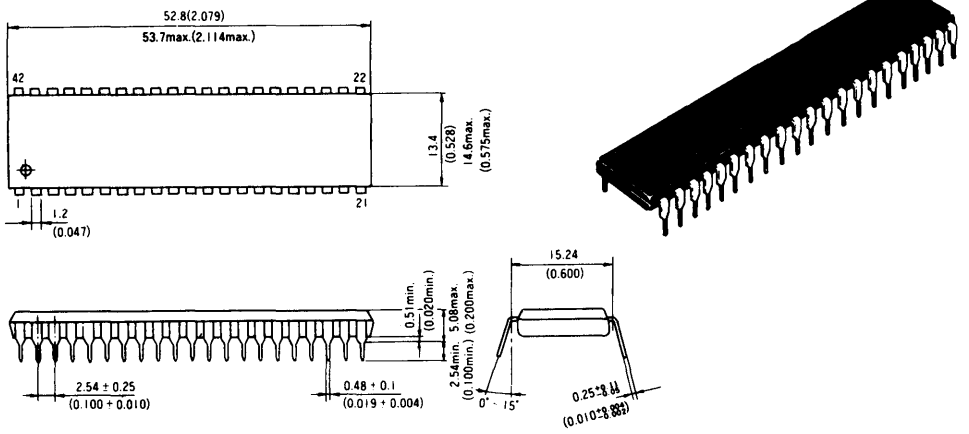




● Dual-in-line Plastic

Unit: mm (inch) Scale 1/1

●DP-42



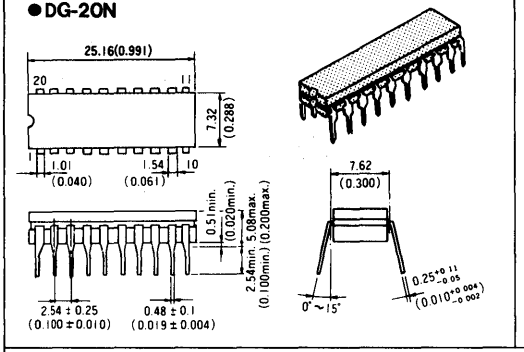
Applicable ICs

DP-16B	HM50256P Series, HM50257P Series, HM51256P Series, HM51256LP Series, HM51258P Series
DP-18B	HM50464P Series, HM50465P Series
DP-18C	HM53051P, HM511000AP Series, HM511000SP Series, HM511000HP Series, HM511001AP Series, HM511001SP Series, HM511002AP Series, HM511002SP Series
DP-20N	HM6168HP Series, HM6168HLP Series, HM6268P Series, HM6268LP Series, HM6167P Series, HM6167LP Series, HM6167HP Series, HM6167HLP Series, HM6267P Series, HM6267LP Series
DP-20NA	HM514256P Series, HM514256AP Series, HM514256SP Series, HM514256HP Series, HM514258HLP Series, HM514258SP Series
DP-22N	HM6287P Series, HM6287LP Series
DP-22NB	HM6288P Series, HM6288LP Series, HM6788P Series, HM6788HP Series, HM6287HP Series, HM6287HLP Series, HM6787P Series, HM6787HP Series
DP-24	HM6116P Series, HM6116LP Series, HM6116AP Series, HM6116ALP Series
DP-24A	HM53461P Series, HM53462P Series
DP-24N	HM6116ASP Series, HM6116ALSP Series
DP-24NC	HM6716P Series, HM6719P Series, HM6789P Series, HM6789HP Series, HM6208P Series, HM6208LP Series, HM6208HP Series, HM6208HLP Series, HM6708P Series, HM6207P Series, HM6207LP Series, HM6207HP Series, HM6207HLP Series, HM6707P Series
DP-28	HM6264P Series, HM6264LP Series, HM6264LP-L Series, HM6264AP Series, HM6264ALP Series, HM6264ALP-L Series, HM62256P Series, HM62256LP Series, HM62256LP-L Series, HM65256AP Series, HM65256BP Series, HM65256BLP Series, HN623257P, HN623258P, HN62321P, HN62321BP, HN62331P, HN62321EP, HN62331EP, HN62321AP, HN62331AP, HN58064P, HN58C66P, HN58C256P, HN27128AP, HN27256P, HN27512P
DP-28N	HM6264ASP Series, HM6264ALSP Series, HM6264ALSP-L Series, HM65256ASP Series, HM65256BSP Series, HM65256BLSP Series, HM63021P Series
DP-32	HM628128P Series, HM628128LP Series, HM658128DP Series, HM65256ASP Series, HM65256BSP Series, HN27C101P Series, HN27C301P Series
DP-40	HN62412P, HN62422P, HN62404P, HN62424P
DP-42	HN62408P, HN624016P

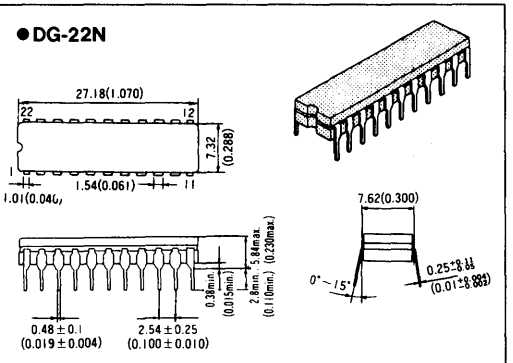
● CERDIP

Unit: mm (inch) Scale 1/1

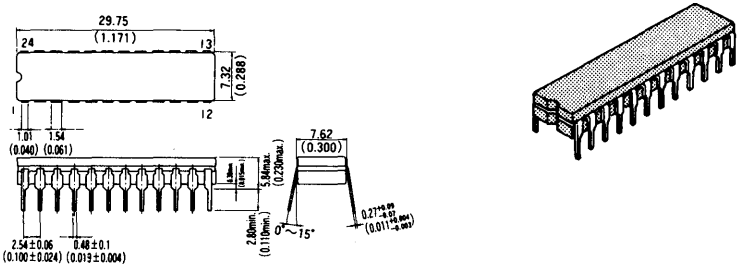
●DG-20N



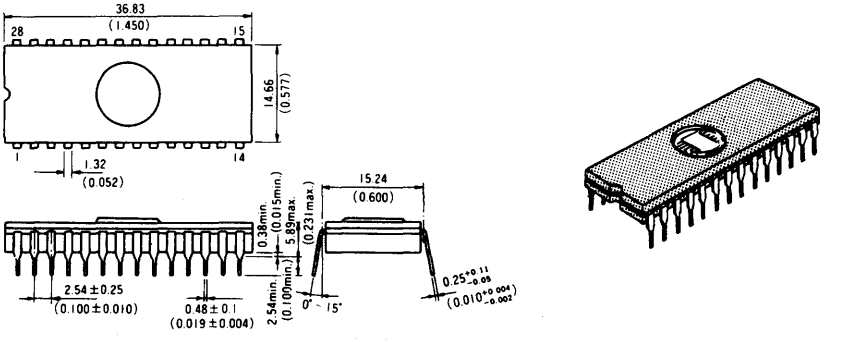
●DG-22N



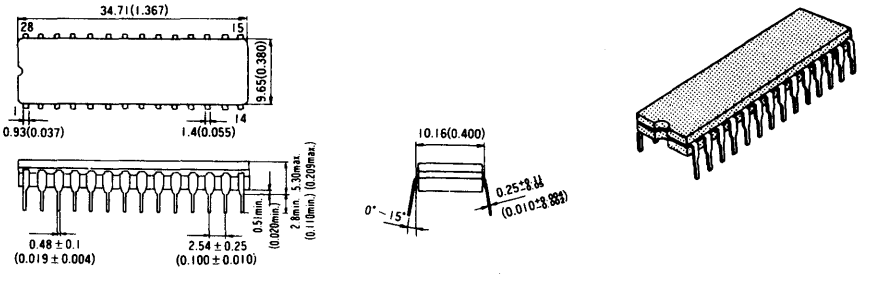
●DG-24V



●DG-28



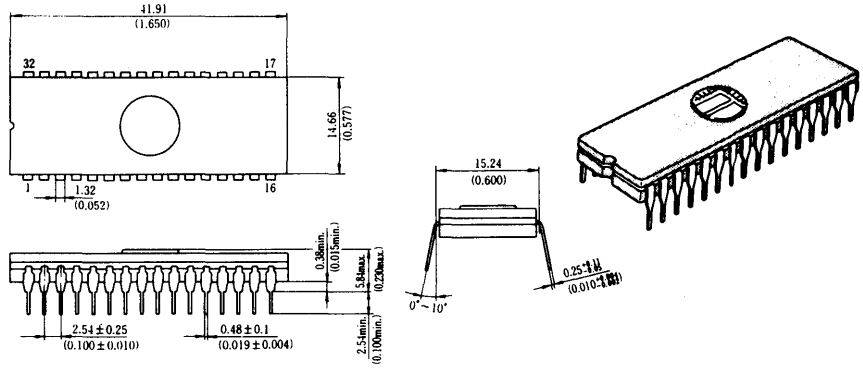
●DG-28N



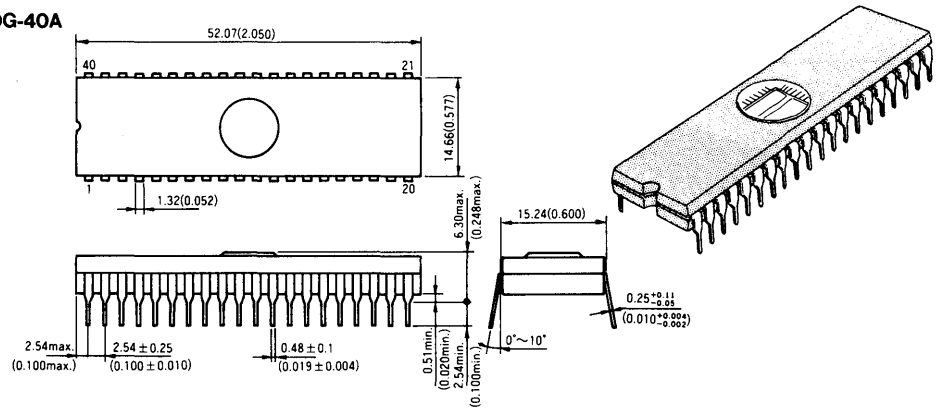
● CERDIP

Unit: mm (inch) Scale 1/1

●DG-32



●DG-40A



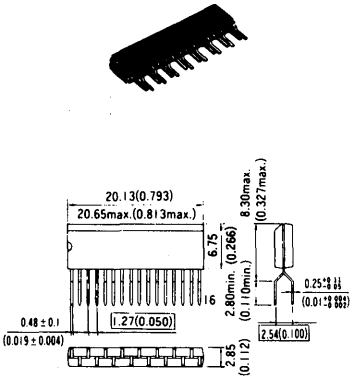
Applicable ICs

DG-20N	HM10480-15, HM100480-15
DG-22N	HM10490-15, HM100490 Series
DG-24V	HM10500-15
DG-28	HN27128AG Series, HN27256G Series, HN27C256G Series, HN27C256AG Series, HN27C256HG Series, HN27512G Series
DG-28N	HM10494 Series, HM100494 Series
DG-32	HN27C101G Series, HN27C301G Series
DG-40A	HN27C1024HG Series

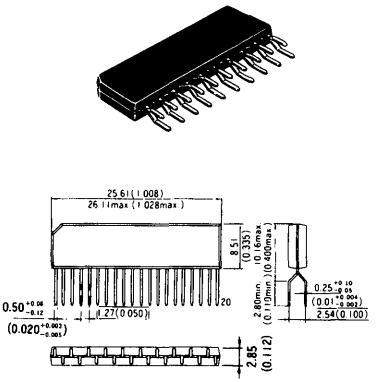
● Zigzag-in-line Plastic

Unit: mm (inch) Scale 1/1

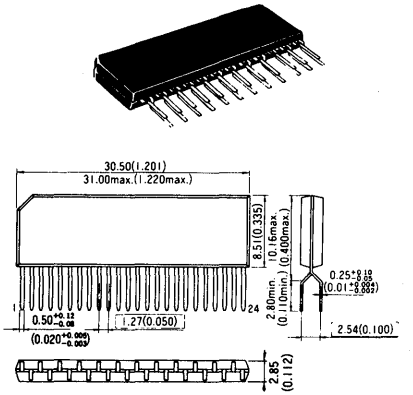
● ZP-16



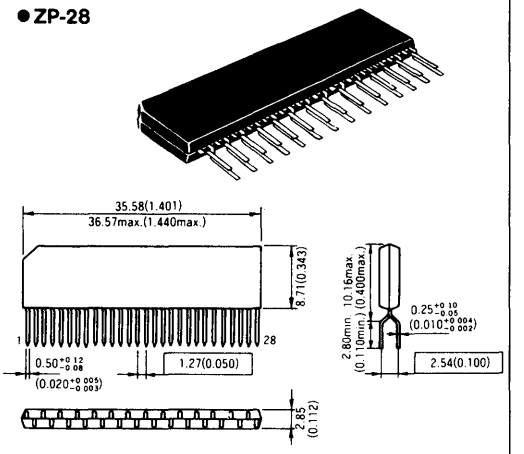
● ZP-20



● ZP-24



● ZP-28



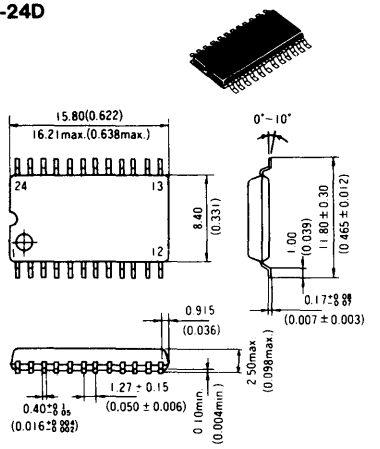
Applicable ICs

ZP-16	HM50256ZP Series, HM50257ZP Series, HM51256ZP Series, HM51256LZP Series
ZP-20	HM514256ZP Series, HM514256AZP Series, HM514256SZP Series, HM514256HZP Series, HM514258AZP Series HM514258SZP Series, HM511000AZP Series, HM511000SZP Series, HM511000HZP Series, HM511001AZP Series, HM511001SZP Series, HM511002AZP Series, HM511002SZP Series
ZP-24	HM53461ZP Series, HM53462ZP Series
ZP-28	HM534251ZP Series, HM534252ZP Series, HM534253ZP Series

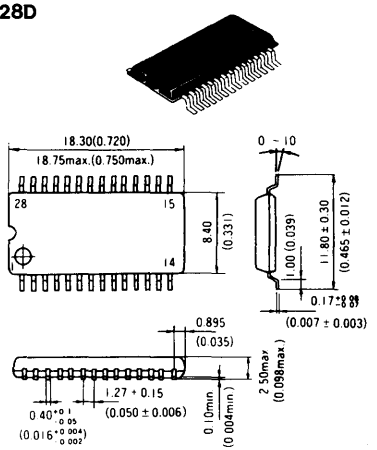
● Flat Package

Unit mm (inch) Scale 1½

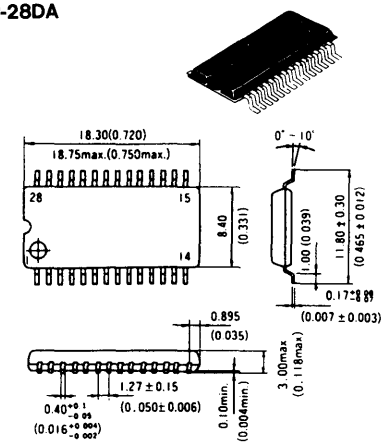
● FP-24D



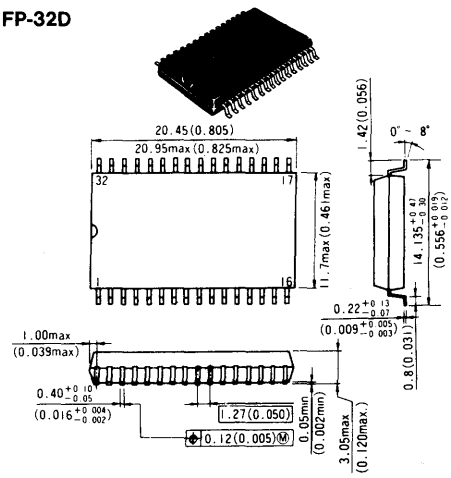
● FP-28D



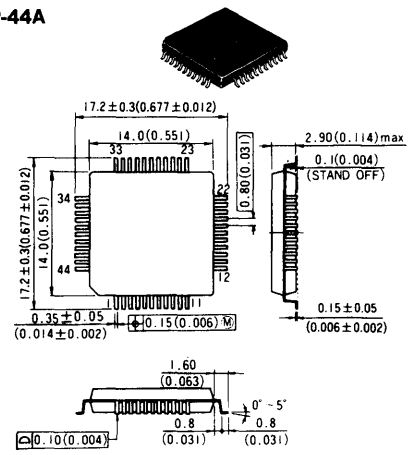
● FP-28DA



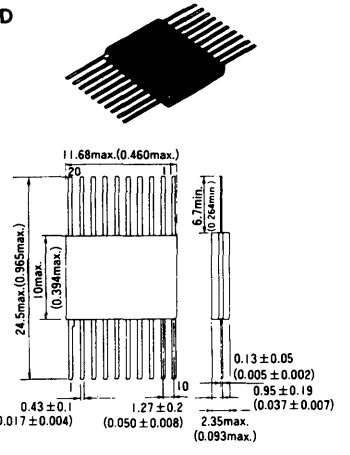
● FP-32D



● FP-44A

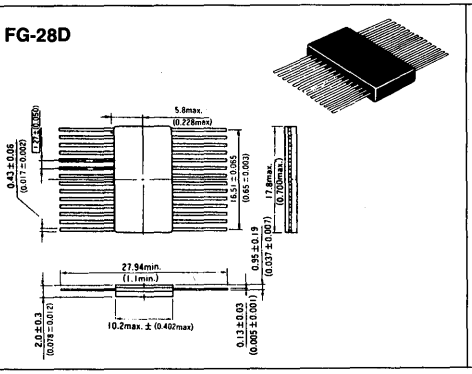


● FG-20D

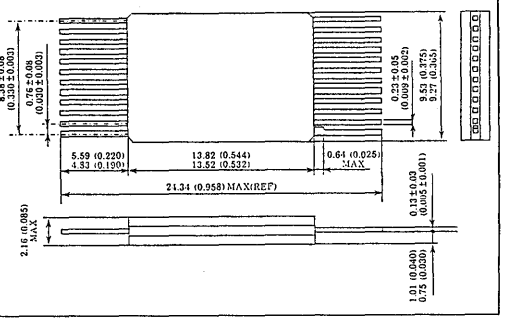


● Flat Packages (continued)

● FG-28D



● FG-24A

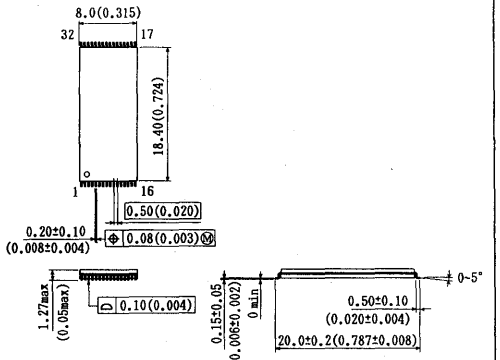


Applicable ICs

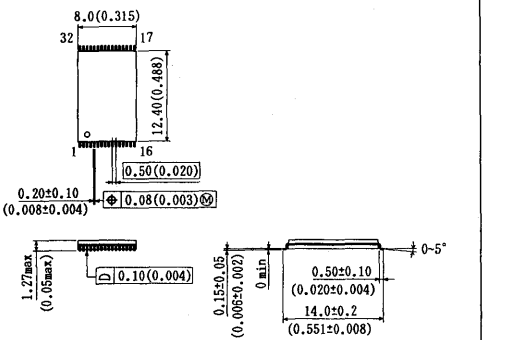
FP-24D	HM6116FP Series, HM6116LFP Series
FP-28D	HM6264FP Series, HM6264LFP Series, HM6264LFP-L Series, HM6264AFP Series, HM6264ALFP Series HM6264ALFP-L Series, HN58C65FP Series, HN58C66FP Series, HN58C256FP Series
FP-28DA	HM6264FP Series, HM6264LFP Series, HM6264LFP-L Series, HM6264AFP Series, HM6264ALFP Series HM6264ALFP-L Series, HM62256FP Series, HM62256LFP Series, HM62256SLFP Series, HM65256BFP Series, HM65256BLFP Series, HN623257F, HN623258F, HN62321F, HN62321BF, HN62331F, HN62321EF, HN62331EF, HN58C65FP, HN58C66FP, HN58C256FP, HN27C256FP
FP-32D	HM628128FP Series, HM628128LFP Series, HM658128DFP Series, HM658128LFP Series, HN62321AF, HN62331AF, HN62304BF, HN62324BF, HN27C101FP, HN27C301FP
FP-44A	HN62412FP, HN62422FP, HN62404FP, HN62424FP, HN62408FP
FG-20D	HM101500F-15
FG-24A	HM1015WF-15
FG-28D	HM10049F Series

● TSOP Packages

● TFP-32D

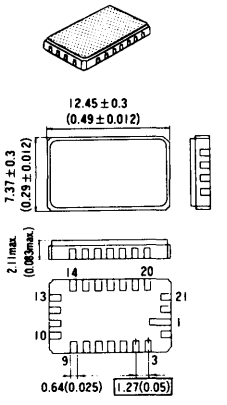


● TFP-32DA

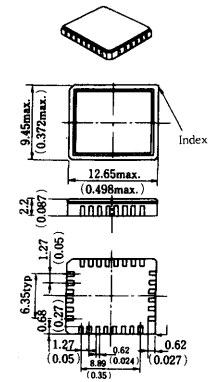


● Leadless Chip Carrier

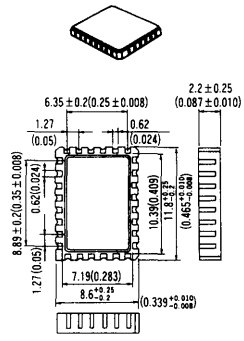
● CG-22A



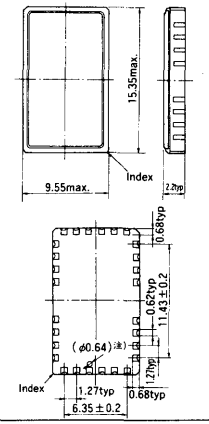
● CG-28



● CG-28A

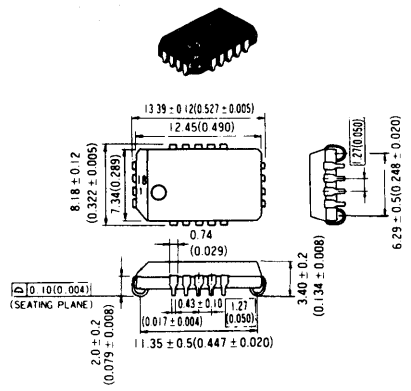


● CG-28B

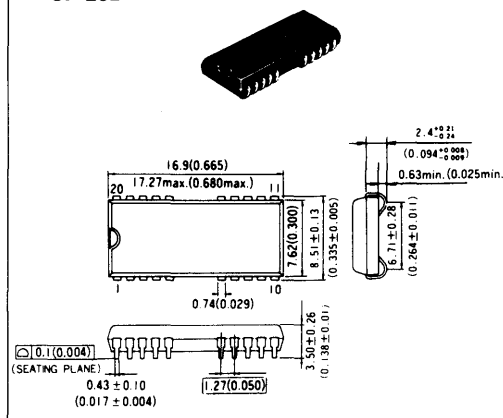


● Flat Package (J-bend Leads)

● CP-18



● CP-20D



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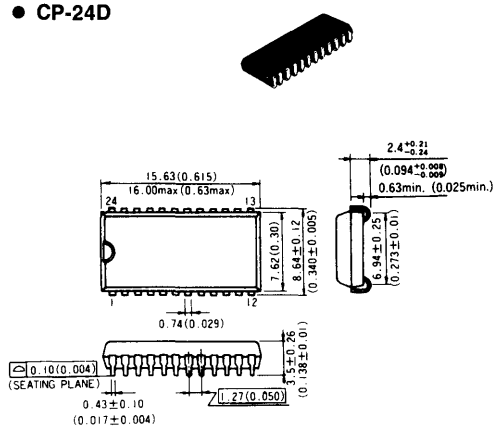
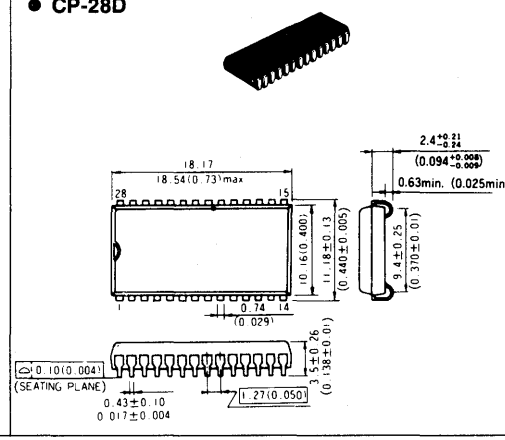


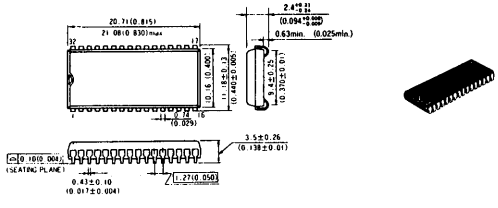
● CP-28D



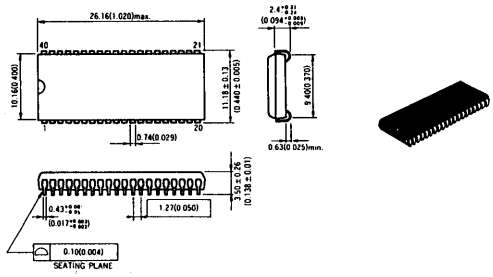
● Flat Packages (J-Bend Leads) (continued)

Unit: mm (inch) Scale 1½

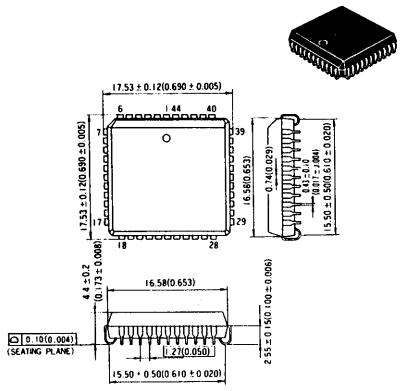
● CP-32D



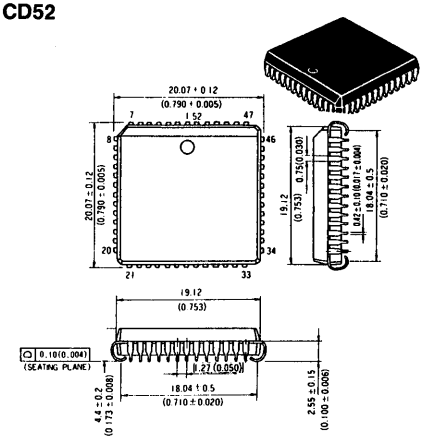
● CP-40D



● CP-44



● CD52



Applicable ICs

CG-22A	HM6787CG Series, HM100490CG Series
CG-28	HM10490CG-15
CG-28A	HM2144CG Series, HM10480CG-13 HM1015WCG-15
CG-28B	HM100500CG-18
CP-18	HM50464CP Series, HM50256CP Series, HM50257CP Series, HM51256CP Series, HM51256LCP Series
CP-20D	HM514256JP Series, HM514256AJP, HM514256SJP Series, HM514256HJP Series, HM514258AJP Series, HM514258SJP Series, HM511000AJP Series, HM511000SJP Series, HM511000HJP Series, HM511001AJP Series, HM511001SJP Series, HM511002AJP Series, HM511002SJP Series
CP-24D	HM6288JP Series, HM6288LJP Series, HM6289JP Series, HM6289LJP Series, HM6789JP Series, HM6789HJP Series, HM6287HJP Series, HM6287HLJP Series, HM6787HJP Series, HM6208HJP Series, HM6208HLJP Series, HM6708JP Series, HM6207HJP Series, HM6207HLJP Series, HM6707JP Series,
CP-28D	HM624256JP Series, HM534251JP Series, HM534252JP Series, HM534253JP Series
CP-32D	HM624257JP Series, HM624257LJP Series
CP-40D	HM538121JP Series, HM538122JP Series, HM538123JP Series
CP-44	HM67C932 Series
CP-52	HM62A168 Series, HM62A188 Series

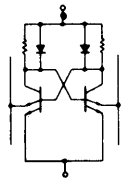
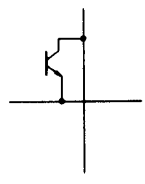
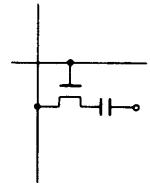
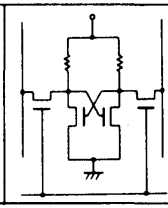
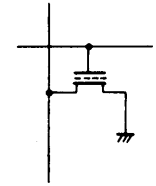
■ RELIABILITY OF HITACHI IC MEMORIES

1. STRUCTURE

IC memories are basically classified into bipolar type and MOS type and utilized effectively by their characteristics. The characteristic of bipolar memories is high speed but small capacity, instead, MOS memories have large capacity. There are also differences in circuit design, layout pattern, degree of integration, and manufacturing process. These memories have been produced with the standardized concept of design and inspection all through the processes of designing, manufacturing and inspection.

IC memories are constituted by the unit patterns called cells, which are integrated in high density. The knowhows based on our experience have been applied in every production stage. In addition, reliability has been ensured using TEG (Test Element Group) evaluation. Examples of cell circuits of bipolar and MOS memories are shown in Table 1.

● **Table 1 Basic Cell Circuit of IC Memories**

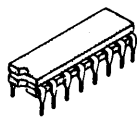
Classification	Bipolar memory (RAM)	Bipolar memory (PROM)	NMOS memory (Dynamic RAM)	NMOS, CMOS memories (Static RAM)	NMOS memory (PROM)
Application	Buffer memory, control memory of high-speed computer	Microcomputer control use	Main memory of computer, microcomputer memory		For microcomputer control
Example of basic cell circuit					

Dies of IC memories are produced in various packages. In this process of packaging, Hitachi has also innovated new techniques and ensured to high level. As packages for IC memories, cerdip (glass-sealed) packages and plastic packages are currently used. Also such packages as LCC (Leadless Chip Carrier) or SOP (Small Outline Package) have been developed for high density packaging. Cerdip packages sealed hermetically are suitable for equipment requiring high reliability. Plastic packages are widely applied to many kinds of equipment. Hitachi plastic packages have been improved the reliability level as highly as that of the hermetically sealed packages. Table 2 shows the outlines of the Hitachi packages.

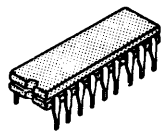
● **Table 2 IC Memory Package Outline**

■ Cerdip

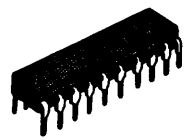
● 16 pin



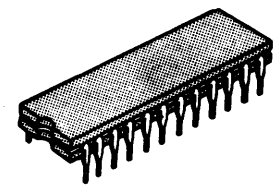
● 18 Pin



● 20 Pin

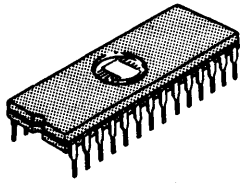


● 24 Pin

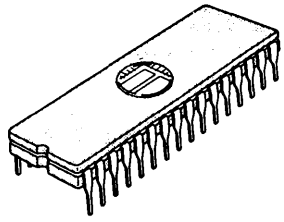


■ Cerdip (continued)

• 28 Pin with Lid

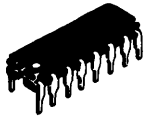


• 32 Pin with Lid



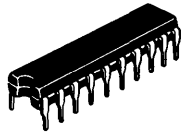
■ Plastic DIP

• 16 Pin

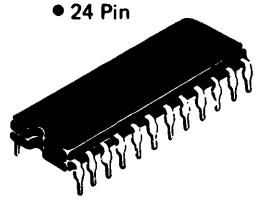


• 18 Pin

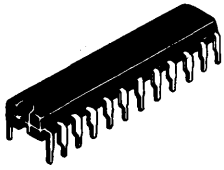
• 20 Pin



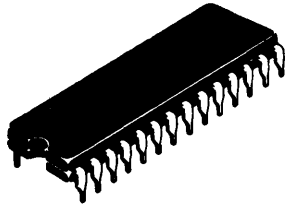
• 24 Pin



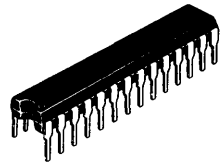
• 24 Pin



• 28 Pin



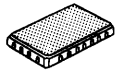
• 28 Pin



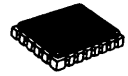
■ Leadless Chip Carrier

• 20 Pin

• 22 Pin

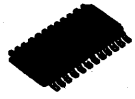


• 24 Pin

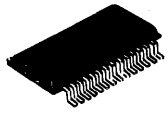


■ SOP

• 24 Pin



• 28/32 Pin

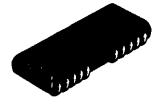


■ PLCC

• 18 Pin

■ SOJ

• 20/26/28/32 Pin



2. RELIABILITY

Results of reliability tests are listed below.

2.1 Reliability Test Data on Bipolar Memories

The reliability test data on the bipolar memories are shown in Table 3 and 4. Since they are manufactured under the standardized design rules and quality control, there is no difference in reliability among the various types. And the larger the capacity is, the higher the reliability per bit becomes.

• Table 3 Results on Bipolar Memory Reliability Test (1)

Test item	HM10480-15					HM2144CG				
	Test condition	Samples	Total component hours	Failures	Failure rate* (1/hr)	Test condition	Samples	Total component hours	Failures	Failure rate* (1/hr)
High-temperature (Operating)	T_a=125°C VEE=-5.2V	340	C.H. 3.4×10^5	0	1/h 2.7×10^{-6}	T_a=125°C VEE=-5.2V	120	C.H. 1.2×10^5	0	1/h 7.7×10^{-6}
High-temp storage	T_a=200°C	351	3.51×10^5	0	2.6×10^{-5}	T_a=200°C	120	1.2×10^5	0	7.7×10^{-6}

* Confidence level 60%

• Table 4 Results on Bipolar Memory Reliability Test (2)

Test item	Test condition	HM10480-15		HM2144CG	
		Samples	Failure	Samples	Failures
Temperature cycling	-55°C to +150°C, 10 cycle	160	0	180	0
Soldering heat	260°C, 10 seconds	35	0	22	0
Thermal shock	0°C to +100°C, 10 cycles	50	0	50	0
Mechanical shock	1500G, 0.5ms, Three times each for X, Y and Z	30	0	22	0
Variable frequency	100 to 200 Hz, 20G, Three times each for X, Y and Z	40	0	22	0
Constant-acceleration	20000G, 1 minute, each for X, Y and Z	40	0	22	0

2.2 Reliability test data on Hi-BiCMOS memory

Hi-BiCMOS memory is newly designed based on the latest fine machining technologies (2m ~ 1m), which features low electric consumption / high integrity by CMOS and high speed / high drivability by bipolar. This device also attains high speed close to ECL and low electric consumption as CMOS. Input and output level supports both ECL and TTL. Reliability test data of HM100490-15 (64k-words x 1-bit) and HM6788P-25 (16k-words x 4-bits) are listed in table 5 and table 6.

The above shows the sufficient reliability of high speed Hi-BiCMOS in the normal use with some limitations considered from its own circuit composition. For further information, see each data sheet. Besides the caution points with CMOS and bipolar device, avoid abnormal use as in deformed or slow wave form which causes malfunction and latch up.

Table 5 Results on Hi-BiCMOS Memory Reliability Test (1)

Test item	HM100490-15 (Cerdip)					Test item	HM6788P-25 (Plastic)					Remarks
	Test condition	Samples	Total test time	Failures	Failure rate		Test condition	Samples	Test test time	Failures	Failure rate	
High-temperature pulse operation	Ta = 125°C VEE=-4.5V	380	C.H. 3.8×10^5	0	1/h 2.4×10^{-6}	High-temperature pulse operation	Ta = 125°C VCC = 5.0V	420	C.H. 4.2×10^5	1*1	1/h 4.8×10^{-6}	*1 foreign matter
						Moisture endurance	85°C 85%RH 5V	210	2.1×10^5	0	4.8×10^{-6}	
High-temp. storage	Ta=200°C	330	3.3×10^5	0	3.0×10^{-6}	Pressure cooker	121°C100%RH	80	0.16×10^5	0	6.3×10^{-5}	

Table 6 Results on Hi-BiCMOS Memory Reliability Test (2)

Test item	Test condition	HM100490-15 (Cerdip)		HM6788P-25 (Plastic)	
		Samples	Failure	Samples	Failure
Temperature cycling	−55°C ~ −150°C 100 cycles	180	0	180	0
Soldering heat	250°C 10 seconds	22	0	22	0
Thermal shock	0°C ~ 100°C 10 cycles	50	0	50	0
Mechanical shock	1500G, 0.5ms Three times each for X, Y and Z	22	0	–	–
Variable frequency	100 ~ 200Hz, 20G Three times each for X, Y and Z	22	0	–	–
Constant acceleration	20000G, 1 minute, each for X, Y and Z	22	0	–	–

2.3 Reliability test data on MOS memories

2.3.1 Reliability test data on MOS DRAM and SRAM

Table 7 and table 8 shows the reliability test data on the representative types of 1M DRAM (HM511000/HM514256), 256k SRAM (HM62256) 1M SRAM (HM628128FP).

The life test is performed at high temperature and high voltage to evaluate the reliability of products using fewer samples. All failures are caused in manufacturing process, so we feedback the data into manufacturing process to improve the quality and reliability.

• Table 7 Reliability Data on 1M DRAM

Test item	Test condition	HM511000P/HM514256P Series (DIP)				HM511000JP/HM514256JP Series (SOP)				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total total time	Failures	Failure rate* (1/hr)	
High-temperature pulse operation	125°C/5.5V	300	6.00×10^{5}	0	1.53×10^{-6}	200	4.00×10^{5}	0	2.30×10^{-6}	*1 Oxide film Failure x1
	125°C/7V	1252	4.50×10^{5}	1*	4.48×10^{-6}	3186	9.34×10^{5}	0	9.85×10^{-7}	
	150°C/7V	200	4.00×10^{5}	0	2.30×10^{-6}	200	4.00×10^{5}	0	2.30×10^{-6}	
Moisture endurance	85°C 85% RH 5.5V	420	8.40×10^{5}	0	1.10×10^{-6}	682	1.36×10^{6}	0	6.74×10^{-7}	
Pressure cooker	121°C/100% RH	150	4.50×10^{4}	0	2.04×10^{-5}	200	6.00×10^{4}	0	1.53×10^{-5}	

* Confidence level 60%

• Table 8. Reliability Data on 256K and 1M SRAM

Test item	Test condition	HM62256FP (SOP)				HM628128FP (SOP)				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total total time	Failures	Failure rate* (1/hr)	
High-temperature pulse operation	125°C/5.5V	3088	3.11×10^{6}	0	8.88×10^{-7}	1038	1.04×10^{6}	0	8.86×10^{-7}	*1 Foreign x 2 *2 Leak x 1
	125°C/7V	455	4.55×10^{5}	0	2.02×10^{-6}	951	5.33×10^{5}	1*1	3.79×10^{-6}	
	150°C/7V	103	1.00×10^{5}	1*1	2.02×10^{-5}	80	1.60×10^{5}	0	5.75×10^{-6}	
Moisture endurance	85°C/85% RH 7V	680	6.80×10^{5}	0	1.35×10^{-6}	127	2.54×10^{5}	0	3.62×10^{-6}	
Pressure cooker	121°C/100% RH	320	6.40×10^{4}	1*2	3.16×10^{-5}	90	2.70×10^{4}	0	3.41×10^{-5}	

* Confidence level 60%

2.3.2 Reliability Test Data on EPROM

EPROM has two types; conventional EPROM with transparent window and one time programmable ROM (OTPROM) packaged in plastic package. Table 9 shows reliability test data on the representative EPROM types 512k EPROM (HN27512, HN27512P), 1M EPROM (HN27C101, HN27C301).

• Table 9. Reliability Data on 512K and 1M EPROM

Test item	Test condition	HN27512 (Cerdip/Plastic)				HN27C101/HN27C301				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total total time	Failures	Failure rate* (1/hr)	
High-temperature operation	125°C/5.5V	200	3.72×10^{5}	0	2.47×10^{-6}	180	3.24×10^{5}	0	2.84×10^{-6}	*1 Data dissipation x 49
	125°C/7V	530	7.95×10^{5}	0	1.16×10^{-6}	327	6.54×10^{5}	0	1.41×10^{-6}	
High-temperature bake	175°C	260	4.91×10^{5}	0	1.87×10^{-6}	150	7.5×10^{5}	0	1.23×10^{-6}	
	200°C	240	3.72×10^{5}	1*1	5.43×10^{-6}	130	6.49×10^{5}	1*1	3.11×10^{-6}	
	250°C	180	1.89×10^{5}	7*1	4.44×10^{-5}	110	3.07×10^{5}	40*1	1.30×40^{-4}	
Moisture endurance	85°C/85% RH 5.5V	290	5.22×10^{5}	0	1.76×10^{-6}	–	–	–	–	Data of 512K OTPROM
Pressure cooker	121°C/100% RH	50	0.10×10^{5}	0	9.20×10^{-5}	–	–	–	–	

* Confidence level 60%.

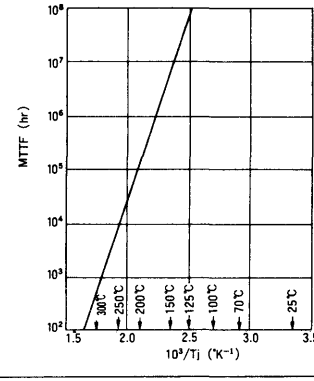
The failure shown in table 9 is due to the data dissipation in memory cells. Getting thermal energy, electrons in memory cells are activated and go through the floating gate. In actual usage, however, it has no problem because this phenomenon dependes on temperature (about 1.0eV of activated energy) greatly. The moisture resistance of OTPROM is also satisfactory.

Table 10 shows the example of PROM derating. When derating, the parameter is generally only the temperature because other operating conditions are specified. Especially to lower the junction temperature during mounting is important for stabilizing the operation relative to access time, refresh time and other characteristics.

• Table 10 Example of HN27C101/HN27C301 Derating

Factor	Temperature
Failure criteria	Electrical Characteristics, Function Test
Failure mechanism	Increase of leak current and others

Results:
The result from high temperature baking of PROM is shown in the right figure.



Note: Decreasing junction temperature shown in the figure will promise the higher reliability. The junction temperature can be calculated by a formula : $T_j = T_a + \theta_{ja} \cdot P_d$ θ_{ja} in about 100°C/W with no air flow and about 60 to 70°C/W with 2.5 m/s air flow.

2.3.3 Reliability Data on MASK ROM

Table 9 shows the reliability test data on 2M and 4M bit MASK ROM. MASK ROM is patterned according to ROM information in manufacturing process, so data dissipation isn't occurred in high temperature like EPROM and EEPROM.

• Table 11. Reliability Data on 2M and 4M MASK ROM

Test item	Test condition	HN62412P (Plastic)				HN62404P (Plastic)				Remarks
		Samples	Total test time	Failures	Failure rate* (1/hr)	Samples	Total test time	Failures	Failure rate* (1/hr)	
High-temp. pulse operaton	125°C/5.5V	–	–	–	–	200	4.0×10^{5}	0	2.3×10^{-6}	
	125°C/7V	120	1.2×10^{5}	0	7.67×10^{-6}	300	3.0×10^{5}	0	3.0×10^{-6}	
Moisture endurance	85°C/85% RH 5.5V	120	1.2×10^{5}	0	7.67×10^{-6}	120	1.20×10^{5}	0	7.67×10^{-6}	
Pressure cooker	121°C/ 100% RH	45	2.3×10^{4}	0	4.1×10^{-5}	45	2.3×10^{4}	0	4.1×10^{-5}	

* Confidence level 60%.

2.3.4 Reliability Data on MOS Memory (The result of environment test)

Table 12 shows examples of each environment test data. They show good results without any failure even in severe environment.

V_{TH} of MOS transistor is one of the basic process parameters in MOS memory, which has almost no change using surface stabilization technology and clean process. Figure 4 shows the examples of time changes for 1M DRAM; V_{DD} min. (V_{min}) and access time (t_{RAC}) in high temperature pulse test.

• Table 12 Reliability Data on MOS Memories

Test item	Test condition	HM511000P (DIP)		HM511000JP (SOJ)		HM62256FP (SOP)		HM628128FP (SOP)		EPROM (Cerdip)		Remarks
		Samples	Failure	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	
Temperature cycling	–55°C to 150°C 10 cycle	3755	0	2786	0	3328	0	710	0	2790	0	
Temperature cycling	–55°C to 150°C 500 cycle	150	0	200	0	482	0	105	0	450	0	
Thermal shock	–65°C to 150°C 15 cycle	77	0	100	0	76	0	77	0	80	0	
Soldering heat	260°C, 10 seconds	22	0	22	0	22	0	22	0	22	0	
Mechanical shock	1,500G, 0.5ms	–	–	–	–	–	–	–	–	38	0	
Variable frequency	100 to 2,000Hz 20G	–	–	–	–	–	–	–	–	38	0	
Constant-acceleration	6000G	–	–	–	–	–	–	–	–	38	0	*6,000G

2.4 Change of Electrical Characteristics on IC Memory

The degradation of I_{CBO} and h_{FE} are the main factors of degradation in inner cell transistor of bipolar memory. In actual element designing, however, it is designed to operate in the range at which no degradation happen. Therefore no change of characteristics including access time are observed. Time dependence in access time for HM10470 are shown in Fig. 1.

Figure 1 Time change in access time for bipolar memory

Example	
Device name	HM10480-15
Test condition	Ta = 125°C, V_{EE} = –5.2V
Failure criteria	t_{AA} = 15ns
Failure mechanism	Surface degration
Results: Access time is stabilized.	

Example of time change in access time for Bipolar memory

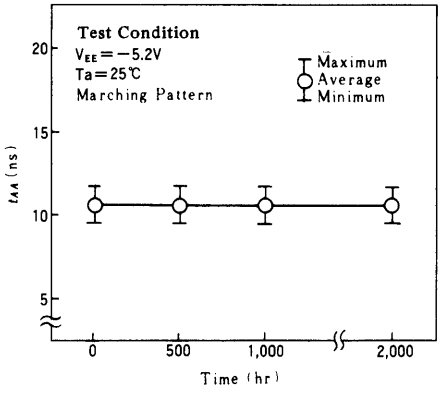


Figure 2 Time change in access time for Hi-BiCMOS memory

Example	
Device name	HM100490
Test condition	Ta = 125°C, V_{EE} = –4.5V all bit scanning
Failure criteria	t_{AA} = 15ns
Failure mechanism	Surface degradation
Results: Access time is stabilized.	

Example of time change in access time for Hi-Bi CMOS memory

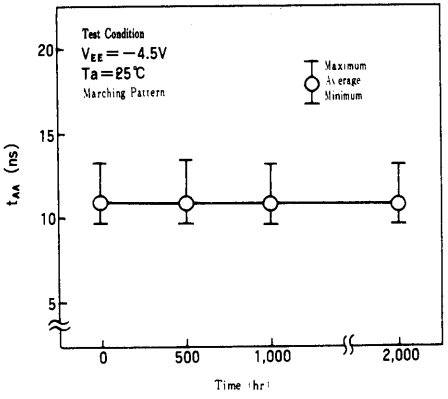


Figure 3 Time change in V_{CC} min and t_{AA} for Hi-BiCMOS memory

Example	
Device name	HM6788P-25
Test condition	Ta = 125°C, V_{CC} = 5.0V all bit scanning
Failure criteria	V_{CC} = 4.5V, t_{AA} = 25ns
Failure mechanism	Surface degradation

Results:
Both of V_{CC} (min) and t_{AA} are stabilized.

Examples of time change in V_{CC} min and t_{AA} for Hi-Bi CMOS memory

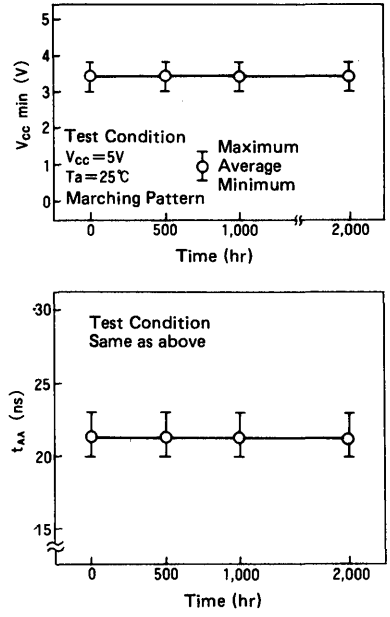


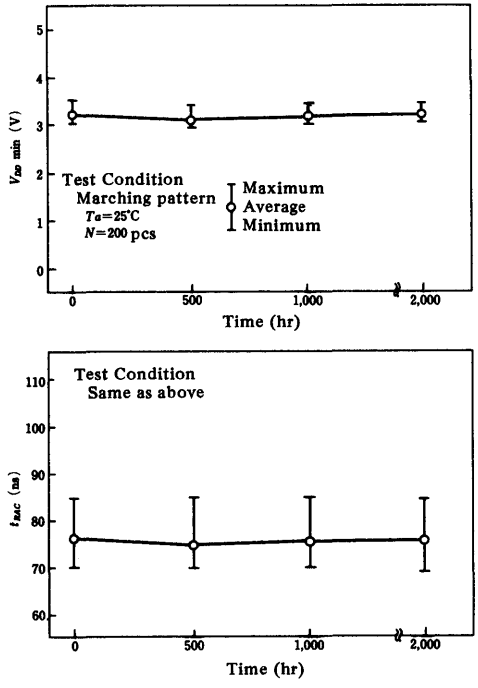
Figure 4 Time change in V_{DD} min and t_{RAC} for MOS memory

Example	
Device name	HM511000P
Test condition	Ta =125°C, V_{CC} = 7V all bit scanning
Failure criteria	V_{DD} = 4.5V, ΔV_{DD} = 1.0V
Failure mechanism	Surface degradation

Results:
Access time (t_{AA}) is stabilized and is within the failure criteria.

Note: Test accuracy is 0.2V, 2ns.

Example of time change in V_{DD} min and t_{RAC} for MOS memory



2.5 Failure Mode Rate

Figure 5 and 6 show examples of failure mode happened in users' application. Since IC memories require the finest pattern process technology, the percentage of failures, such as pinholes, defects on photoresist and foreign materials, tends to increase. To eliminate the defects in the manufacturing process, Hitachi has improved the process and performed 100% burn in screening under high temperature. Hitachi has been collecting and checking customers' process-data and marketing data for higher reliability of our products. To analyze them is very helpful for the improvement of designing and manufacturing.

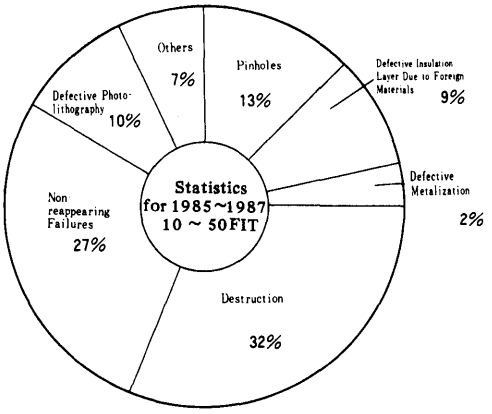


Figure 5 Failure Mode Rate of Bipolar Memory

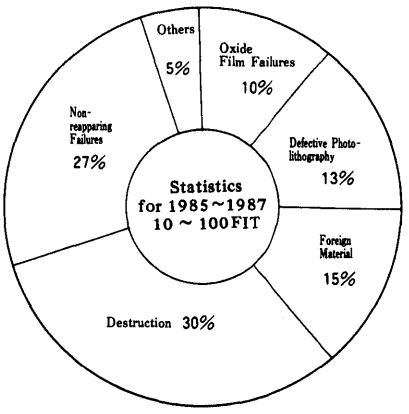


Figure 6 Failure Mode Rate of MOS Memory

3. Reliability of Semiconductor Devices

3.1. Reliability Characteristics for Semiconductor Devices

Hitachi semiconductor devices are designed, manufactured and inspected so as to achieve a high level of reliability. Accordingly, system reliability can be improved by combining highly reliable components along proper environmental conditions. This section describes reliability characteristics, failure types and their mechanisms in terms of devices. First, semiconductor device characteristics are examined in light of their reliability.

(1) Semiconductor devices are essentially structure sensitive as seen in surface phenomenon. Fabricating the device requires precise control of a large number of process steps.

(2) Device reliability is partly governed by electrode materials and package materials, as well as by the coordination of these materials with the device materials.

(3) Devices employ thin-film and fine-processing techniques for metallization and bonding. Fine materials and thin film surfaces sometimes exhibit physically different characteristics from the bulks.

(4) Semiconductor device technology advances drastically: Many new devices have been developed using new processes over a short period of time. Thus, conventional device reliability data cannot be used in some cases.

(5) Semiconductor devices are characterized by volume production. Therefore, variations should be an important consideration.

(6) Initial and accidental failures are only considered to be semiconductor device failures based on the fact that semiconductor devices are essentially operable semipermanently. However, wear failures caused by worn materials and migration should be also reviewed when electrode and package materials are not suited for particular environmental conditions.

(7) Component reliability may depend on device mounting, conditions for use, and environment. Device reliability is affected by such factors as voltage, electric field strength, current density, temperature, humidity, gas, dust, mechanical stress, vibration, mechanical shock, and radiation magnetic field strength.

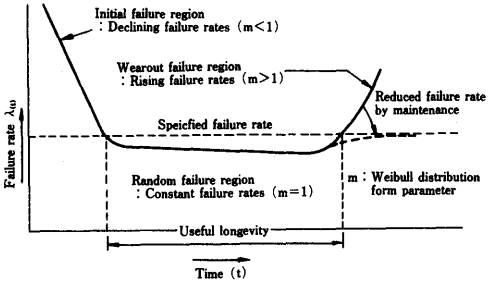


Figure 7 Typical failure rate curve

Device reliability is generally represented by the failure rate. 'Failure' means that a device loses its function, including intermittent degradation as well as complete destruction.

Generally, the failure rate of electric components and equipment is represented by the bathtub curve shown in Fig. 7. For semiconductor devices, the configuration parameter of the Weibull distribution is smaller than 1, which means an initial failure type. Such devices ensure a long lifetime unless extreme environmental stress is applied. Therefore, initial and accidental failures can become a problem for semiconductor devices. Semiconductor device reliability can be physically represented as well as statistically. Both aspects of failures have been thoroughly analyzed to establish a high level of reliability.

3.2 Failure Types and Their Mechanisms

3.2.1 Failure physics

Failure physics is, in a broad sense, a basic technology of "physics + engineering". It is used to examine the physical mechanism of failures in terms of atoms and molecules to improve device reliability. This physical approach was introduced to the reliability field with the demand for minimized development cost and period, as technology rapidly developed and system performance increased, requiring more complex and higher levels of reliability. These conditions derived from the development of solid state physics (semiconductor physics) after World War II and associated device development.

Failure physics have been employed to:

1) Detect failed devices as soon as possible
2) Establish models and equation used for failure prediction
3) Evaluate reliability in short periods by accelerated life test

The purpose of the failure physics approach is to contribute to reliability related fields such as product design, prediction, test, storage and usage by adding physics as a basic technology to conventional experimental and statistical approaches.

3.2.2 Failure types and their mechanism

Device failures are physically discussed in this section. Semiconductor device failures are basically categorized as disconnection, short-circuit, deterioration and miscellaneous failures. These failures and their causes are summarized in Table 11. Typical failure mechanisms are reviewed next.

(1) Surface Deterioration

The pn junction has a charge density of 10^{14} – 10^{20}/cm^3. If charges exceeding the above density are accumulated on the pn junction surface, particularly adjacent to a depletion layer, electric characteristics of the junction tend to be easily varied. Although the surface of such devices as planar transistors is generally covered with a SiO_2 film and is in an inactive state, the possibility of deterioration caused by surface channels still exists. Surface deterioration depends heavily on applied temperature and voltage and is often handled by the reaction model.

One example of recent failures is surface deterioration caused by hot carriers. Hot carriers are generated when such devices as MOS dynamic RAMs are operated at a voltage near the minimum breakdown voltage BV_{DS} by raising internal voltage and when a strong electric field is established near the MOS device's drain resulting from reduced device geometry from 2 μm to 0.8 μm. Generated hot carriers may affect surface boundary characteristics on a part of the gate oxide film, resulting in degradation of threshold voltage (V_{TH}) and counter conductance (gm). Hitachi devices have employed improved design and process techniques to prevent these problems. However, as process becomes finer, surface deterioration may possibly become a serious problem.

(2) Electrode-related Failures

Electrode-related failures have become increasingly important as multi-layer wiring has become more complicated. Noticeable failures include electromigration and Al wiring corrosion in plastic sealed packages.

① Electromigration

This is a phenomenon in which metal atoms are moved by a large current of about 10^6 A/cm^2 supplied to the metal. When ionized atoms collide with current of about scattering electrons, an 'electron wind' is produced. This wind moves the

metal atoms in the opposite direction from the current flow, which generates voids at a negative electrode, and hillock and whiskers at an opposite one. The generated voids increase wiring resistance and cause excessive currents to flow in some areas, leading to disconnection. The generated whiskers may cause shortcircuits in multi-metal line.

② Multi-metal line related failures

Major failures associated with multi-metal line include increased leak currents, shortcircuits caused by a failed dielectric interlayer, and increased contact metal resistance and disconnection between metal wirings.

③ Al line corrosion and disconnection

When Plastic encapsulated devices are subjected to high-temperatures, high-humidity or a bias-applied condition, Al electrodes in devices can cause corrosion or disconnection (Fig. 8). Under high-temperature and high-humidity, corrosions are randomly

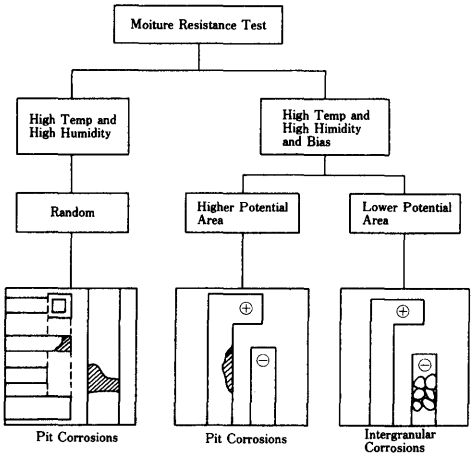


Figure 8 Categorized Al corrosion mode

generated over the element surface. However, after an extended period of time, the corrosions have not significantly increased. Accordingly, this failure is possibly due to an initial failure associated with manufacturing. It is also verified that this type of failure can be generated when the adhesion surface between an element and resin is separated or when foreign materials are attached to the element with human saliva. Under a bias-appllied, high-temperature, high-humidity condition, on the other hand, corrosions are generated in higher potential areas while in lower potential areas, grain corrosion occurs. Once this failure occurs in part of a device, the device can become worn out in a relatively short time. This failure proves to depend on the hydroscopic volume resistivity of sealed resin. The Al line corrosion mechanism described above is summarized in Fig. 9.

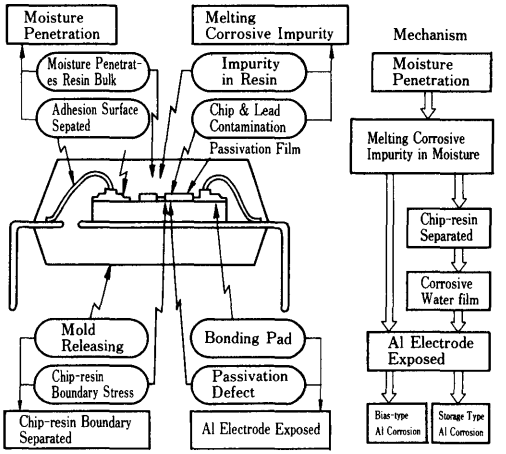


Figure 9 Plastic package cross section and Al corrosion mechanism

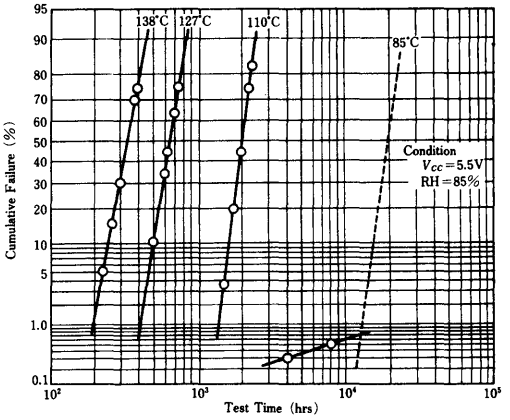


Figure 10 An Example of Moisture Resistance by High temp. and High humidity and bias

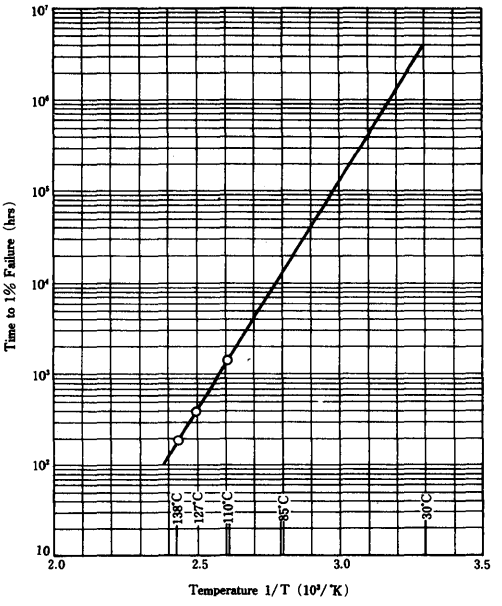


Figure 11 Relationship between temperature and Time to 1% failure (RH = 85%)

(3) Bonding related failures

① Degradation caused by intermetallic formation

Bonding strength degradation and contact resistance increase are caused by compounds formed in connections between Au wire and Al film or between Au film and Al wire. These are the most serious problems in terms of reliability. The compounds are formed rapidly during bonding and are increased through thermal treatment. Consequently, Hitachi products are subjected to a lower-temperature, shorter-period bonding whenever possible.

② Wire creep

Wire creep is wire neck destruction in an Au ball along an intergranular system occurring when a plastic sealed device is subjected to a long-term thermal cycling test. This failure results from increased crystal grains due to heat application when forming a ball at the top of an Au wire, or from an impurity introducing to the intergranular system. Bonding under usual conditions with no loop configuration failures does not cause this failure unless a severe long-term thermal cycling test is applied. Accordingly, wire creep is not a problem in actual usage.

③ Chip crack

With the increase in chip size associated with the increased number of incorporated functions, more problems have been occurring during assembly, such as chip cracks during bonding. Bonding methods include Au-silicon eutectic, soldering and Ag-paste. Soldering and Ag-paste exhibit few chip crack problems. For Au-silicon eutectic, in contrast, large stress is applied to a pellet due to its strength and high temperature resistance for attachment, which may result in critical chip defects. Today, the chip destruction limit can be determined by finite-element analysis and by distortion measurement using a fine accuracy gauge. Ideally, Au-silicon eutectic should be evenly applied over the entire surface. However, this is difficult due to the existence of a silicon oxide film on the silicon back surface. Therefore, specifications for Au-silicon eutectic have been established based on stress analysis and thermal cycling test results.

④ Reduced maximum power dissipations

For power devices, heat fatigue due to thermal expansion coefficient mismatch among different materials deteriorates thermal resistance. This results in decreased maximum power dissipations.

(4) Sealing related failures

Hermetic sealing packages, including metal, glass, ceramic, and all other types, have the possibility of the following failures.

1. Al line corrosion on the chip surface due to slight moisture and reaction between the different ionized materials.
2. Intermittent moving foreign metals short
3. Al line corrosion due to extraneous H_2O caused by hermetic failure

Moving foreign matter, even if it is a non-active solid, can be charged up within a cavity during movement, thereby inducing parastic effects and metal shorts. The foreign matter detection method is specified by MIL-STD-883C, PIND (Particle Impact Noise Detection) Test. The PIND test consists of filtering a particle impact waveform (ultrasonic waveform), detecting it with a microphone, and then amplifying.

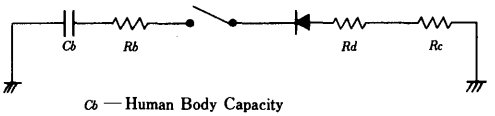
(5) Disturbance

①Electrostatic discharge destruction

Destruction caused by electrostatic discharge is a problem common to semiconductor devices. A recent report introduced three modes of this failure; the human body model, charged device model and field induced model.

The human body is easily charged. A person just walking across a carpet can be charged up to 15000 V. This voltage is high enough to destroy a device. An equivalent circuit of the human body model is shown in Fig. 10. The human body's capacitance Cb and resistance Rb are 100 to 200 pF and 1000 to 2000Ω, respectively. Assuming a body is charged

with 2000V, the dissipated energy is obtained as follows: With a time constant of 10^{-7} sec, the dissipated energy is 2 KW, which is enough to destroy a small area of a chip.



Cb — Human Body Capacity
Rb — Human Body Resistance
Rd — Device Resistance
Rc — Resistance Between Device and Ground

$$E = \frac{1}{2} CbV^2 = 0.2 \times 10^{-3} J$$

Figure 12 Equivalent circuit of human body model

In the charged device model, charges are accumulated in a device, not a human body, and discharged through contact resistance during a short time. The equivalent circuit of this model is shown in Fig. 13. Device size and device position relative to GND are important parameters in this model since the model depends on device capacity.

In the field induced model a device is left under a strong electric field or is affected by neighboring high voltage material. Since the capacitor of device or lead of device acts like an antenna, the following cases will possibly cause destruction. 1) a device is incorporated into a high electric field such as a CRT, 2) a device is left under a high-frequency electric field and 3) a device is moved with a container charged at high voltage, such as a tube.

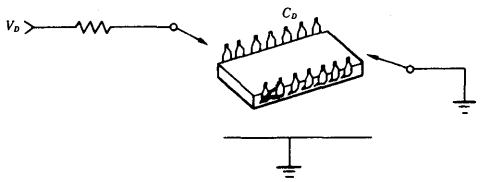


Figure 13 Equivalent circuit of charging model

② Latch up

Latch up is a problem unique to CMOS devices. This problem is a thyristor phenomenon caused by a parasitic PNP or NPN transistor formed in the CMOS configuration. Latch up occurs when an accidental surge voltage exceeding a maximum rating, a power supply ripple, an unregulated power supply and noise is applied, or when a device is operated from two sources having different set-up voltages. These cases can cause input or output current to flow in the opposite direction from usual flow, which triggers parasitic thyristors. This results in excessive current flowing between a power supply and ground. This phenomenon continues until the power is off or the flowing current is forced to be reduced to a certain level. Once latch up occurs in an operating device, the device will be destroyed.

Much effort should be made in designing circuits to prevent latch up. Latch up triggering input or output currents start to flow under the following conditions.

Vin <Vcc or Vin < GND for input level

Vout > Vcc or Vout < GND for input level

Therefore, circuits should be designed so that no forward current flows through the input protection diodes or output parasitic diodes.

③ Soft errors

When α particles are generated from uranium or thorium in a package the silicon surface of an LSI chip, electron-hole pairs are formed which act as noise to data lines and other floating nodes, causing temporary soft errors. This phenomenon is shown in Fig. 14. Only electrons from among the electron-hole pairs are only collected to a memory cell. As a result, the cell changes from a state of 1 to 0, which is a soft error.

Hitachi devices have been subjected to simulation and irradiation tests to prevent soft errors. In some cases, organic material, PIQ, is applied to the surface of the device.

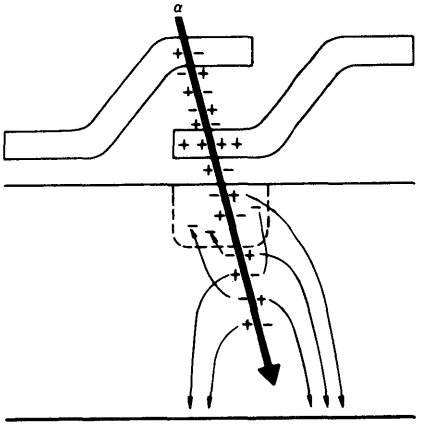


Figure 14 Soft error caused by α particles in dynamic memory

Table 13. Failure causes and mechanism

Failure related causes		Failure mechanisms	Failure modes
Passivation	Surface oxide film, Insulating film between wires	Pin hole, Crack, Uneven thickness, Contamination, Surface inversion, Hot carrier injected	Withstanding voltage reduced, Short, Leak current increased, h_{FE} degraded, Threshold voltage variation, Noise
Metallization	Interconnection, Contact, Through hole	Flaw, Void, Mechanical damage, Break due to uneven surface, Non-ohmic contact, Insufficient adhesion strength, Improper thickness, Electromigration, Corrosion	Open, Short, Resistance increased
Connection	Wire bonding, Ball bonding	Bonding runout, Compounds between metals, Bonding position mismatch, Bonding damaged	Open, Short Resistance increased
Wire lead	Internal connection	Disconnection, Sagging, Short	Open, Short
Diffusion, Junction	Junction diffusion, Isolation	Crystal defect, Crystallized impurity, Photo resist mismatching	Withstanding voltage reduced, Short
Die bonding	Connection between die and package	Peeling chip, Crack	Open, Short, Unstable operation, Thermal resistance increased
Package sealing	Packaging, Hermetic Seal, Lead plating, Hermetic pakage & plastic package, Filler gas	Integrity, moisture ingress, Impurity gas, High temperature, Surface contamination, Lead rust, Lead bend, break	Short, Leak current Increased, Open, Corrosion disconnection, Soldering failure
Foreign matter	Foreign matter in package	Dirt, Conducting foreign matter, Organic carbide	Short, Leak current increased
Input/output pin	Electrostatistics, Excessive Voltage, Surge	Electron destroyed	Short, Open, Fusing
Disturbance	α particle	Electron hole generated	Soft error
	High electric field	Surface inversion	Leak current increased

(6) Fine geometry related problems

In response to higher integration requirements for memories and microcomputers, LSI geometry has been reduced in the way of 3 μm → 2 μm → 1.3 μm → 0.8 μm.

However power supply has not been scaled down used for 5V, only line dimensions have been fined increasingly. Problems associated with finer geometry are shown in Table 14.

Table 14. Finer geometry related problems

Item	Problems	Countermeasure
5V single supply voltage	• Breakdown voltage of gate oxide films • SiO_2 defects	Oxide film formation process improved • Cleaning • Gettering • Screening
Horizontal dimension reduction	• Soft errors by α particles • Al reliability reduced • CMOS latch up • Mask alignment margin reduced • Hot carriers	Surface passivation film improved • Metallization improved • Design/layout improved • Process improved
Vertical & horizontal dimension reduction	• Higher breakdown voltage not permitted • Electrostatic discharge resistance reduced	Use of low voltage examined • Configuration improved • Protection circuits enhanced

1. VIEWS ON QUALITY AND RELIABILITY

Hitachi basic views on quality are to meet individual users' purpose and their required quality level and also to maintain the satisfied level for general application. Hitachi has made efforts to assure the standardized reliability of our IC memories in actual usage. To meet users' requests and to cover expanding application, Hitachi performs the followings;

(1) Establish the reliability in design at the stage of new product development.
(2) Establish the quality at all steps in manufacturing process.
(3) Intensify the inspection and the assurance of reliability of products.
(4) Improve the product quality based on marketing data.

Furthermore, to get higher quality and reliability, we cooperate with our research laboratories.
With the views and methods mentioned above, Hitachi makes the best efforts to meet the users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Target

Establishment of reliability target is important in manufacturing and marketing as well as function and price. It is not practical to determine the reliability target based on the failure rate under single common test condition. So, the reliability target is determined based on many factors such as each characteristics of equipment, reliability target of system, derating applied in design, operating condition and maintenance.

2.2 Reliability Design

Timely study and execution are essential to achieve the reliability based on reliability targets. The main items are the design standardization, device design including process and structural design, design review and reliability test.

(1) Design Standardization
Design standardization needs establishing design rules and standardizing parts, material, and process. When design rules are established on circuit, cell, and layout design, critical items about quality and reliability should be examined. Therefore, in using standardized process or material, even newly developed products would have high reliability, with the exception of special requirement on function.

(2) Device Design
It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in case of applying new process or new material, we study the technology prior to development of the device in detail.

(3) Reliability Test by Test Site
Test site is sometimes called Test Pattern. It is useful method for evaluating reliability of designing and processing ICs with complicated functions.

1. Purposes of Test Site are as follows;
   - Making clear about fundamental failure mode;
   - Analysis of relation between failure mode and manufacturing process condition.
   - Analysis of failure mechanism.
   - Establishment of QC point in manufacturing.
2. Effects of evaluation by Test Site are as follows;
   - Common fundamental failure mode and failure mechanism in devices can be evaluated.
   - Factors dominating failure mode can be picked up, and compared with the process having been experienced in field.
   - Able to analyze relation between failure causes and manufacturing factors.
   - Easy to run tests.

2.3 Design Review

Design review is a method to confirm systematically whether or not design satisfies the performance required including by users, follows the specified ways, and whether or not the technical items accumulated in test data and application data are effectively applied.
In addition, from the standpoint of competition with other products, the major purpose of design review is to insure quality and reliability of the product. In Hitachi, design review is performed in designing new products and also in changing products.
The followings are the items to consider at design review.

(1) Describe the products based on specified design documents.
(2) Considering the documents from the standpoint of each participant, plan and execute the subprogram such as calculation, experiments and

investigation if unclear matter is found.

(3) Determine the contents and methods of reliability test based on design document and drawing.

(4) Check process ability of manufacturing line to achieve design goal.

(5) Arrange the preparation for production.

(6) Plan and execute the sub-programs of design changes proposed by individual specialists, for tests, experiments and calculation to confirm the design change.

(7) Refer to the past failure experiences with similar devices, confirm the prevention against them, and plan and execute the test program for confirmation of them.

In Hitachi, these study and decision at design review are made using the individual check lists according to its objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

The following items are the general views of overall quality assurance in Hitachi;

(1) Problems is solved in each process so that even the potential failure factors will be removed at final stage of production.

(2) Feedback of information is made to insure satisfied level of process ability.

As the result, we assure the reliability.

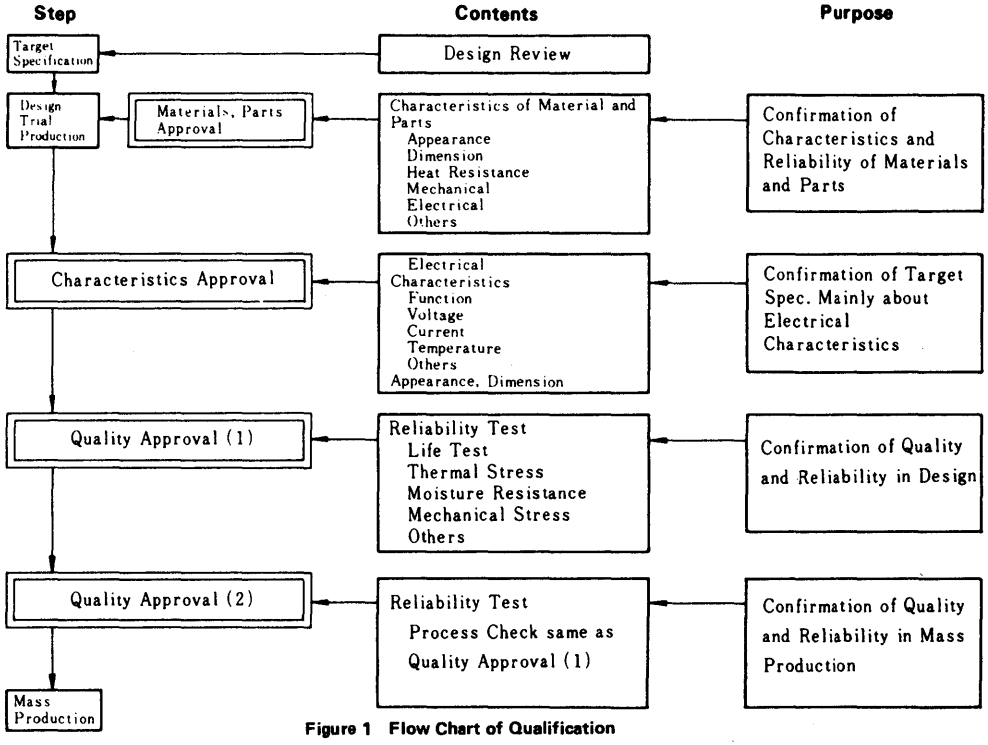


Figure 1 Flow Chart of Qualification

3.2 Qualification

To assure the quality and reliability, the qualification tests are done at each stage of trial production and mass production based on the reliability design described in section 2.

The followings are the views on qualification in Hitachi:

(1) From the standpoint of customers, qualify the products objectively by a third party.
(2) Consider the failure experiences and data from customers.
(3) Qualify every change in design and work.
(4) Qualify intensively on parts and materials and process.
(5) Considering the process ability and factor of manufacturing fluctuation, establish the control points in mass production.

Considering the views mentioned above, qualification shown in Fig. 1 is done.

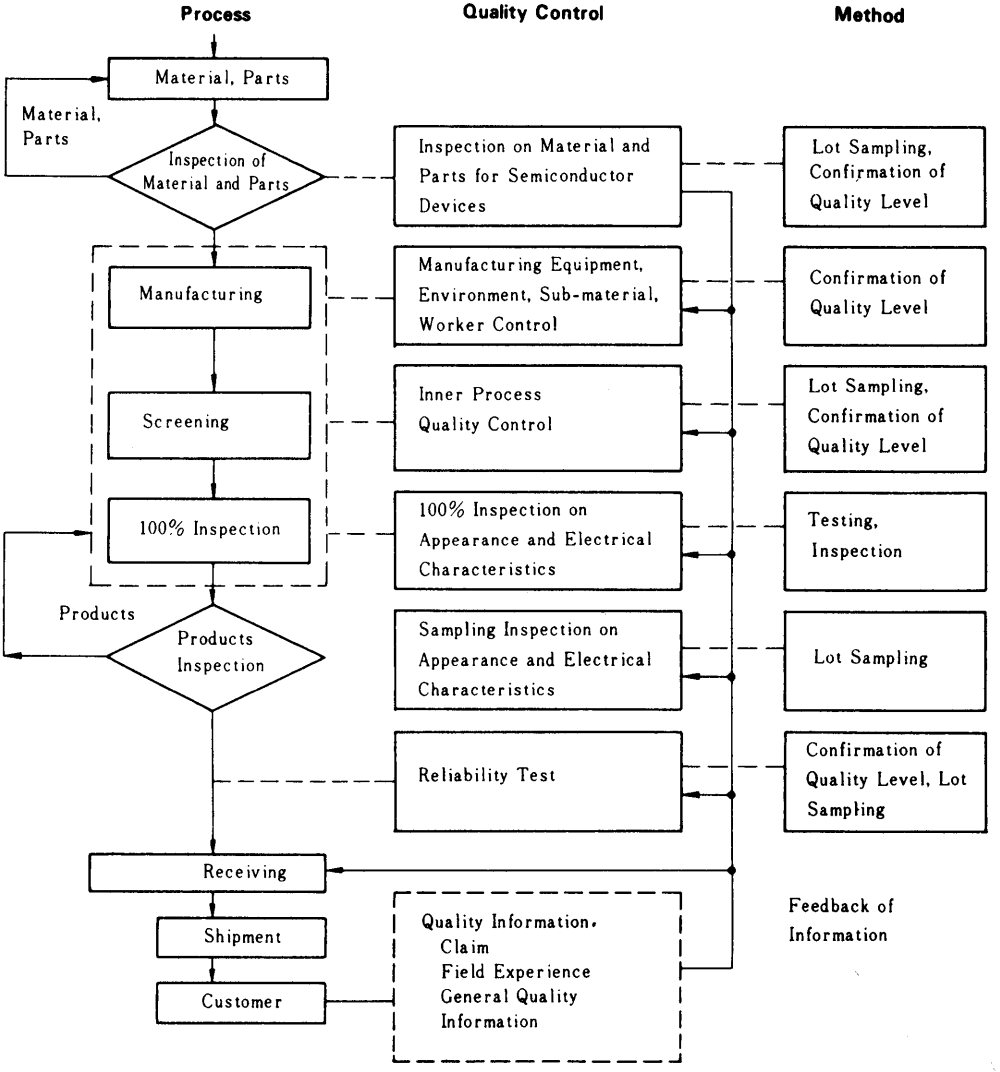


Figure 2 Flow Chart of Quality Control in Manufacturing Process

3.3 Quality and Reliability Control in Mass Production

To assure quality in mass production, quality is controlled functionally by each department, mainly by manufacturing department and quality assurance department. The total function flow is shown in Fig. 2.

3.3.1 Quality Control on Parts and Materials

With the tendency toward higher performance and higher reliability of devices, quality control of parts and materials becomes more important. The items such as crystal, lead frame, fine wire for wire bonding, package and materials required in manufacturing process like mask pattern and chemicals, are all subject to inspection and control.

Besides qualification of parts and materials stated in 3.2, quality control of parts and materials is defined in incoming inspection. Incoming inspection is performed based on its purchase specification, drawing and mainly sampling test based on MIL-STD-105D. The other activities for quality assurance are as follows.

- **Table 1. Quality Control Check Points of Parts and Material (example)**

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension	Flatness
	Sheet Resistance	Resistance
	Defect Density	Defect Numbers
	Crystal Axis	
Mask	Appearance	Defect Numbers, Scratch
	Dimension	Dimension Level
	Resistoration	
	Gradation	Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension	
	Purity	Purity Level
	Elongation Ratio	Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Processing Accuracy	
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension	Dimension Level
	Leak Resistance	Airtightness
	Plating	Bondability, Solderability
	Mounting Characteristics	Heat Resistance
	Electrical Characteristics	
	Mechanical Strength	Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics	
	Thermal Characteristics	
	Molding Performance	Molding Performance
	Mounting Characteristics	Mounting Characteristics

(1) Technology Meeting with Vendors
(2) Approval and Guidance of Vendors
(3) Analysis and tests of physical chemistry.

The typical check points of parts and materials are shown in Table 1.

3.3.2 Inner Process Quality Control

To control inner process quality is very significant for quality assurance of devices. The quality control of products in every stage of production is explained below. Fig. 3 shows inner process quality control.

(1) Quality Control of Products in Every Stage of Production

Potential failure factors of devices should be removed in manufacturing process. Therefore, check points are set up in each process so as not to move the products with failure factors to the next process. Especially, for high reliability devices, manufacturing lines are rigidly selected in order to control the quality in process. Additionally we perform rigid check per process or per lot, 100% inspection in proper processes so as to remove failure factors caused by manufacturing fluctuation, and screenings depending on high temperature aging or temperature cycling. Contents of controlling quality under processing are as follows:

- Control of conditions of equipment and workers and sampling test of uncompleted produsts.
- Proposal and execution of working improvement.
- Education of workers
- Maintenance and improvement of yield
- Picking up of quality problems and execution of countermeasures toward them.
- Communication of quality information.

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing facilities have been developed with the need of higher devices in performance and the automated production. It is also important to determine quality and reliability.

In Hitachi, automated manufacturing is promoted to avoid manufacturing fluctuation, and the operation of high performance equipment is controlled to function properly.

As for maintenance inspection for quality control, daily and periodically inspections are performed based on specification on every check point.

As for adjustment and maintenance of measuring equipment, the past data and specifications are clearly checked to keep and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-material.

Quality and reliability of devices are affected especially by manufacturing process. Therefore, we thoroughly control the manufacturing circumstances such as temperature, humidity, dust, and the sub-materials like gas or pure water used in manufacturing process.

Dust control is essential to realize higher integration and higher reliability of devices. To maintain and improve the clearness of manufacturing site, we take care buildings, facilities, air-conditioning system, materials, clothes and works. Moreover, we periodically check on floating dust in the air, fallen dust or dirtiness on floor.

Process	Control Point		Purpose of Control
▽ Purchase of Material			
Wafer	Wafer	Characteristics, Appearance	Scratch, Removal of Crystal Defect Wafer
○ Surface Oxidation	Oxidation		Assurance of Resistance
○ Inspection on Surface Oxidation		Appearance, Thickness of Oxide Film	Pinhole, Scratch
○ Photo Resist	Photo Resist		
○ Inspection on Photo Resist		Dimension, Appearance	Dimension Level
◇ PQC Level Check			Check of Photo Resist
○ Diffusion	Diffusion	Diffusion Depth, Sheet Resistance	Diffusion Status
○ Inspection on Diffusion		Gate Width	Control of Basic Parameters (V_{TH}, etc) Cleaness of surface, Prior Check of V_{IH} Breakdown Voltage Check
◇ PQC Level Check		Characteristics of Oxide Film Breakdown Voltage	
○ Evaporation	Evaporation	Thickness of Vapor Film, Scratch, Contamination	Assurance of Standard Thickness
○ Inspection on Evaporation			
◇ PQC Level Check			
○ Wafer Inspection	Wafer	Thickness, V_{TH} Characteristics	Prevention of Crack, Quality Assurance of Scribe
○ Inspection on Chip Electrical Characteristics	Chip	Electrical Characteristics	
○ Chip Scribe		Appearance of Chip	
○ Inspection on Chip Appearance			
◇ PQC Lot Judgement			
Frame			
○ Assembling	Assembling	Appearance after Chip Bonding	Quality Check of Chip Bonding
		Appearance after Wire Bonding	Quality Check of Wire Bonding
◇ PQC Level Check		Pull Strength, Compresion Width, Shear Strength	Prevention of Open and Short
○ Inspection after Assembling		Appearance after Assembling	
◇ PQC Lot Judgement			
Package			
○ Sealing	Sealing	Appearance after Sealing Outline, Dimension	Guarantee of Appearance and Dimension
◇ PQC Level Check	Marking	Marking Strength	
○ Final Electrical Inspection			
◇ Failure Analysis		Analysis of Failures, Failure Mode, Mechanism	Feedback of Analysis Information
○ Appearance Inspection			
△ Sampling Inspection on Products			
○ Receiving			
Shipment			

Figure 3 Example of Inner Process Quality Control

3.3.3 Final Tests and Reliability Assurance

(1) Final Tests

Lot inspection is done by quality assurance department for the product passed in 100% test in final manufacturing process. Though 100% of passed products is expected, sampling inspection is subjected to prevent mixture of failed products by mistake. The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Our lot inspection is based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability, the reliability tests are performed periodically, and performed on each manufacturing lot if user requires.

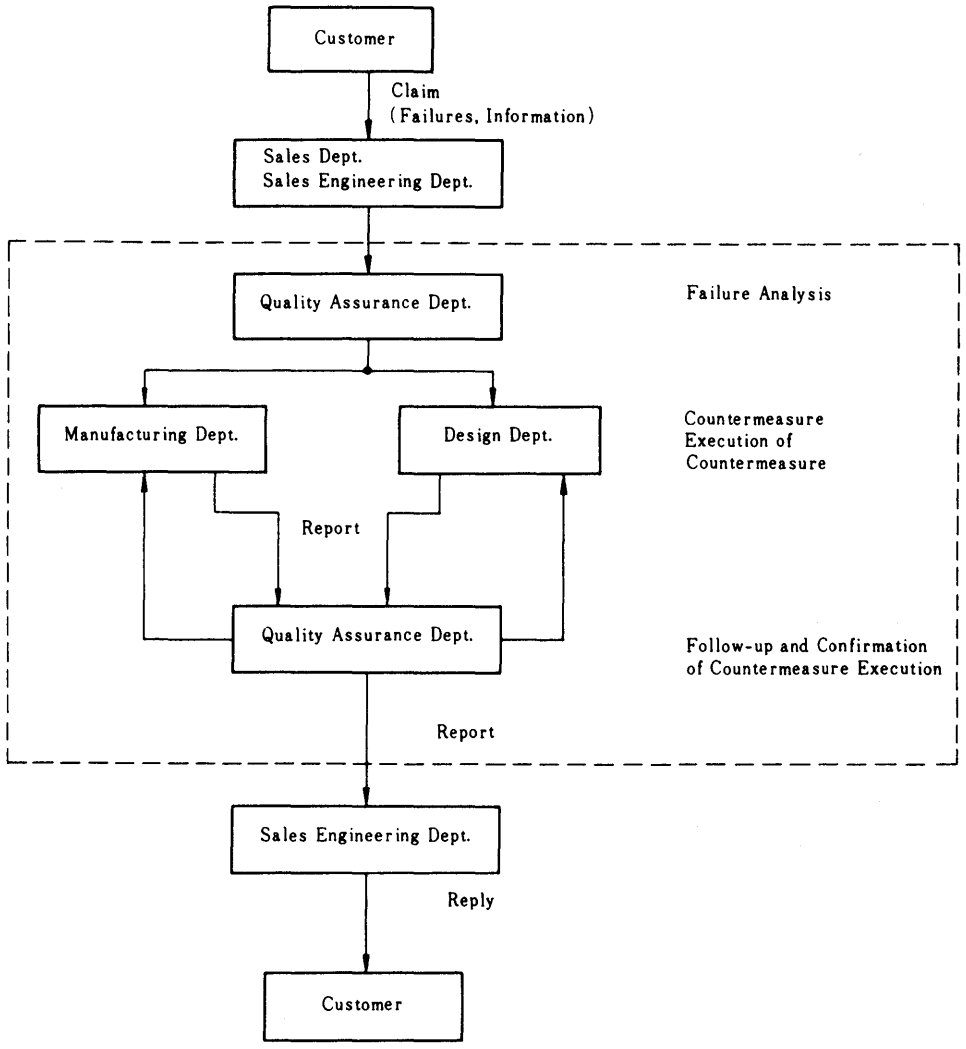


Figure 4 Process Flow Chart of Coping with Failure to a Customer

■ OUTLINE OF TESTING METHOD

1. INSPECTION METHOD

Compared to conventional core memories, IC memories contain all peripheral circuits, such as the decoder circuit, write circuit and read circuit. As a result, assembly and electrical inspection of ICs are all performed by IC manufacturers. Consequently, as the electrical inspection of IC memories are becoming more systematic, conventional IC inspection facilities are becoming useless. This has led to the development and introduction of a memory tester with pattern generator to generate the inspection pattern of the memory IC at high speed. A function test for such as TTL gates can be performed even by a simple DC parameter facility. However, when the address input becomes multiplexed as in 16K, 64K and 256K memory, even the generation of the function test pattern becomes a serious problem.

In the memory IC inspection, its quality cannot be judged by DC test on external pins only, because the number of the element such as transistor which can be judged in the DC test is only 1/1000 of all elements. The followings are the address patterns proposed to inspect whether the internal circuits are functioning correctly.

(1) All "Low", All "High"
(2) Checker Flag
(3) Stripe Pattern
(4) Marching Pattern
(5) Galloping
(6) Waling
(7) Ping-Pong

Those are not all, but only representative ones. There are the pattern to check the mutual interference of bits and the pattern for the maximum power dissipation. Among the above mentioned patterns, those of (1) to (4) are called N pattern, which can check one sequence of N bit IC memory with the several times of N patterns at most. Those of (5) to (7) are called N^2 pattern, which need several times of N^2 patterns to check one sequence of N bit IC memory. Serious problem arises in using N^2 pattern in a large-capacity memory. For example, inspection of 16K memory with galloping pattern takes a lot of time – about 30 minutes. (1), (2) and (3) are rather simple and good methods, however, they are not perfect to find any failure in decoder circuits. Marching is the most simple and necessary pattern to check the function of IC memories.

2. MARCHING PATTERN

The marching pattern, as its name indicates, is a pattern in which "1"s march into all bits of "0"s. For example, a simple addressing of 16 bit memory is described below.

(1) Clear all bits . . . . . See Fig. 1 (a)
(2) Read "0" from 0th address and check that the read data is "0". Hereafter, "Read" means "checking and judging data"
(3) Write "1" on 0th address. . . . . See Fig. 1(b)
(4) Read "0" from 1st address.
(5) Write "1" on 1st address.
(6) Read "0" from nth address.
(7) Write "1" on nth address . . . . . See Fig. 1(c)
(8) Repeat (6) to (7) to the last address. Finally, all data will be "1".
(9) After all data become "1", repeat from (2) to (8) replacing "0" and "1".

In this method, 5N address patterns are necessary for the N-bit memory.

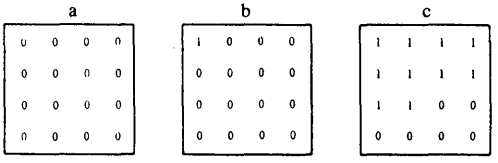


Figure 1 Addressing method of for 16 bit memory in the Marching pattern

1. Static RAM

1.1. Static RAM Memory Cell

The static RAM memory cell consists of flip-flops organized as 4 NMOS transistors and 2 load resistors as shown in figure 1-1. The data in the cell can be retained as long as power is supplied, and read out without being destroyed.

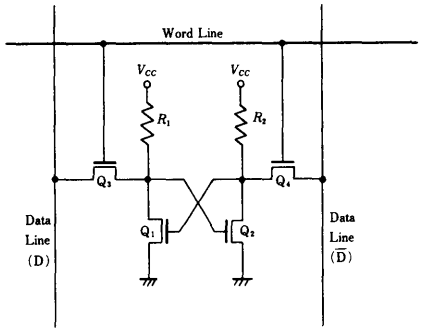


Figure 1-1. Static RAM Memory Cell

1.2. Data Retention Mode and Battery Back-up System

The data in RAM is destroyed at power off. However, CMOS static RAM has a data retention mode. In this mode, power consumption at standby is extremely low and supply voltage can be reduced to 2 V. So, it enables a battery back-up system to retain data during power failure.

Data Retention Mode: The important point in designing a battery back-up system is the timing relation between the memory power supply during the change (ordinal source → battery) and the chip select signal. If the timing for the change is missed, the data in memory might be destroyed.

Figure 1-2. shows the timing for switching the power supply. The following explains the technical terms related to the data retention mode.

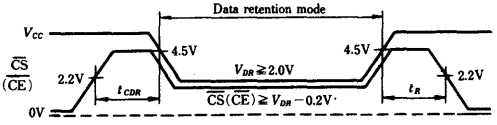


Figure 1-2. Timing for Battery Back-up Application

Data retention mode: The period that the power supply voltage is lower than the specified operation voltage. During this period, memory must be kept in non-select condition (e.g. $\overline{CS} = V_{DR} - 0.2V$).

t_{CDR} (time for chip select to data retention): The minimum time needed to change from operating mode to data retention mode. Normally 0 ns.

t_R (Operation recovery time): The minimum time needed to change from data retention mode to operating mode. Normally, it is the same as the cycle time of the memory.

V_{DR} (data retention voltage): The voltage applied in data retention mode. Normally, the minimum supply voltage needed to retain memory data is 2 V.

I_{CCDR} (data retention current): The current consumption in data retention mode. It depends on memory power supply voltage and ambient temperature. It is specified at supply voltage (V_{DR}) = 3.0 V.

Battery Back-up System: battery back-up sequence is described in the following:

1. External circuit detects failure of system power supply.
2. External circuit changes RAM to standby mode.
3. External circuit separates RAM from system power supply.
4. External circuit switches to Back-up power supply.

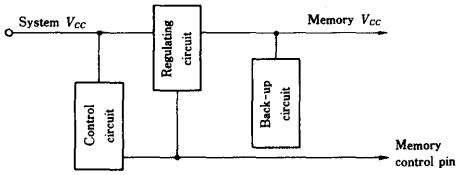


Figure 1-3. Example of Battery Back-up System

The control circuit detects the power failure and cuts off the power after switching memories to standby mode. On recovery, it confirms power supply and after some delay, returns memories to operating mode. The memory control signals depend on the types of memories used in the system.

* Using memory with only one $\overline{CS}$. NAND signal between the control signal and chip select signal should be connected to $\overline{CS}$. As the level of $\overline{CS}$ in data retention mode must be higher than V_{DR} − 0.2V, the power supply for this NAND gate must either be shared with the memory power supply, or be pulled up to the memory power supply.
* Using memory with two $\overline{CS}$. Basically, the signals are the same as mentioned above. In general use, two pins should be used for the control signal and the chip select signal respec-

tively. $\overline{CS}$, which can intercept current path of other pins in the input buffers, is for control signal input of data retention mode.

* Using memory with $\overline{CS}$ and CS. As CS selects the chips at high level, it is better to use CS than $\overline{CS}$ as control signal input for data retention mode. As soon as power down is detected, signals should be brought to low level. So a pull-up to the memory power supply level is not needed and circuit organization is simplified.

Figure 1-4 shows an example of a battery back-up system circuit. Hitachi recommends using CMOS logic for gate G_1 in control circuit and memory V_{CC}. The low V_{CE} transistor Q_1 is required to switch regulating circuit from system power supply to back-up power supply.

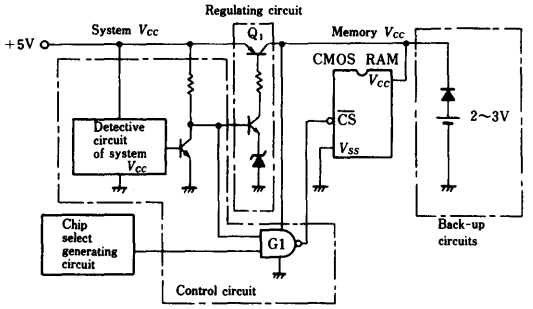


Figure 1-4. Example of Battery Back-up System Circuit

2. Pseudo-Static RAM

2.1 Pseudo-Static RAM Features

A new type of memory, pseudo-static RAM has been developed providing the advantages of dynamic RAM (low cost, high density), and static RAM (easy usage). IC memory consists of memory cells for data storage, and input/output circuits for interfacing to the external circuits. PSRAM provides the memory cell and peripheral circuits of DRAM and the external control circuits, which includes a part of the refresh control circuits not provided by dynamic RAM, and interface circuits similar to that of static RAM, on a chip, as shown in table 2-1. Address input is not multiplexed and data input/output is byte-wide like standard static RAM. With PSRAM x 8 organization, medium density memory system can be designed easily. PSRAM provides address refresh, automatic refresh and self refresh.

Figure 2-1 shows examples of system design using PSRAM and DRAM. Using PSRAM, the circuits interfacing CPU to DRAM can be drastically reduced.

Figure 2-2 shows block diagram of pseudo static RAM.

Table 2-1. PSRAM Features

	SRAM	PSRAM	DRAM
Memory Cell	4 Tr + 2 R	1 Tr + 1 C	
Organization	x1, x4, x8	x8	x1, x4
Address	Single Address		Multiplexed Address
Refresh	Nor Necessary	Necessary	
External Circuits	Simple ⟺ Complexed		

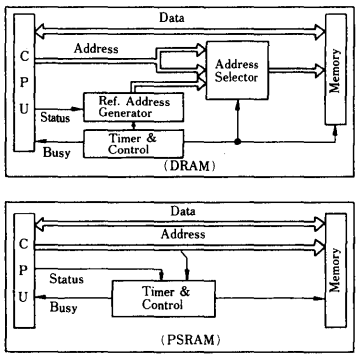


Figure 2-1. System Organization

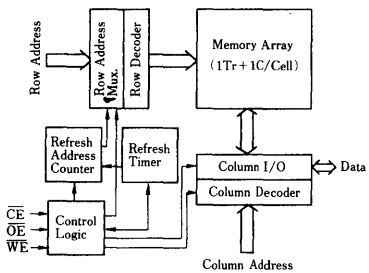


Figure 2-2. Block Diagram (PSRAM)

2.2. 1 Mbit Pseudo-Static RAM Function

Read/Write Cycle: Figure 2-3 and figure 2-4 show the timing chart for the read/write cycle of 1 Mbit pseudo-static RAM HM658128. The HM658128 can perform 2 types of access in a read cycle, $\overline{CE}$ access (Figure 2-3 (a)) and $\overline{OE}$ access figure 2-3 (b)). It writes the data at the rising edge of $\overline{WE}$ (figure 2-4 (a)) or at the rising edge of $\overline{CE}$ (figure 2-4 (b)). The $\overline{CS}$ pin should be brought high when the address is latched at the falling edge of $\overline{CE}$ in the read/write cycle. The HM658128 has no $\overline{OE}$ specification at the falling edge of $\overline{CE}$ as it provides both $\overline{OE}$ pin and $\overline{RFSH}$ pin.

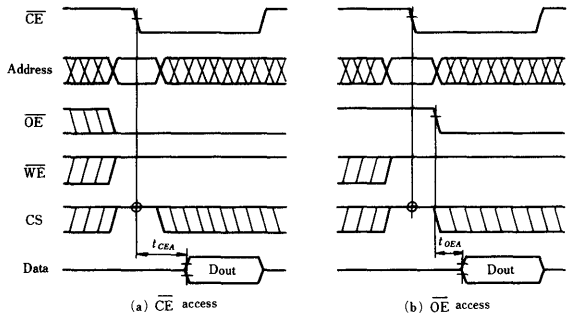


Figure 2-3. Read Cycle

CS Standby Mode: The HM658128 enters CS standby mode for one cycle if CS turns to low at the falling edge of $\overline{CE}$ (figure 2-5).

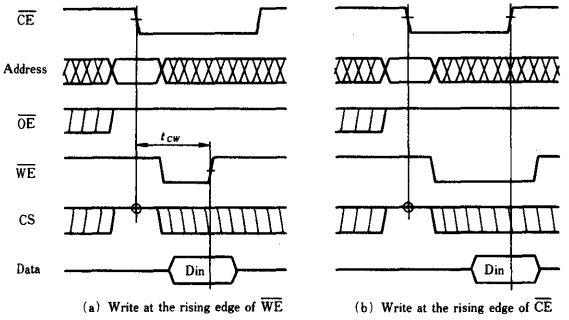


Figure 2-4. Write Cycle

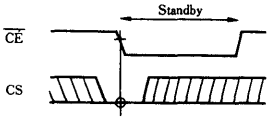


Figure 2-5. CS Standby Mode

Address Refresh: Address refresh mode performs refresh by access to row address (A0 – A8) 0 – 511 sequentially within 8 ms, as shown in figure 2-6 (in distributed mode). In this mode, CS should be high at falling edge of $\overline{CE}$.

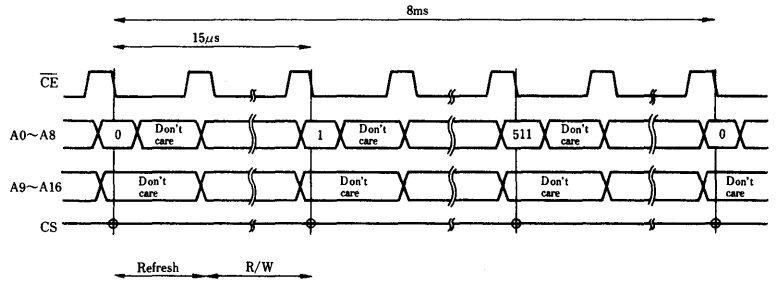


Figure 2-6. Address Refresh

Automatic Refresh: The HM658128 goes to automatic refresh mode if $\overline{RFSH}$ falls while $\overline{CE}$ is high and it is kept low for more than 180 ns.
It is not required to input the refresh address from address pins A0 – A8, as it is generated internally. Figure 2-7 shows the timing chart for distributed refresh. In automatic refresh mode, the timing for only $\overline{CE}$ and $\overline{RFSH}$ are specified.

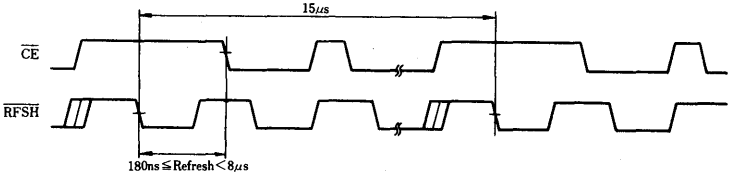


Figure 2-7. Automatic Refresh

Self Refresh: Self refresh mode performs refresh at the internally determined interval. The HM658128 enters the mode when the internal refresh timer is enabled by keeping $\overline{CE}$ high and $\overline{RFSH}$ low for more than 8 μs (figure 2-8).

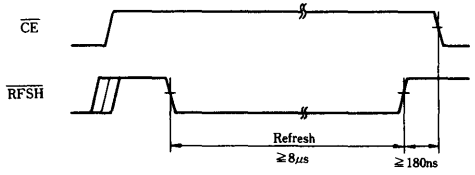


Figure 2-8. Self Refresh

Considerations on Using HM658128: The following should be considered when using the HM658128.

- Data retention. The HM658128 can retain the data with a battery (but not for long time). The HM658128L, low power version, offers typical self-refresh or standby current of 100μA.
  A 1-Mbyte system (using eight HM658128Ls) can retain the data for about 1.5 months with battery of 100 mAh current. V_{CC} = 5 V ± 10% must be maintained for data retention.
- Power on. Start HM658128 operation by executing more than eight initial cycles (dummy cycles) more than 100 μs after power voltage reaches 4.5 V – 5.5 V after power on.
- Bypass capacitor. Hitachi recommends inserting 1 bypass capacitor per RAM.

2.3 Pseudo-Static RAM Data Retention

PSRAM with self refresh retains data $\overline{CE}$ and $\overline{OE}$ are fixed for more than defined period. The following explains considerations for PSRAM data retention.

First, PSRAM cannot retain the data at low supply voltage.

They employ 1 MOS type memory cell as shown in figure 2-9. The charge is stored on the capacitor C as memory data. The data 1, written at low supply

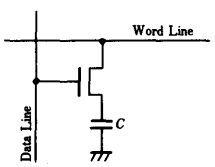


Figure 2-9. Memory Cell of PSRAM

voltage, cannot be read as 1 at high supply voltage.

Figure 2-10 indicates the operation voltage for self refresh and subsequent read of PSRAM. If the data is read out at more than 5 V of V_{CC}, for example, after self refresh is performed at V_{CC} = 3.7 V, it is destroyed.

PSRAM must be used at supply voltage from 4.5V to 5.5V.

Second self refresh current increases at low supply voltage.

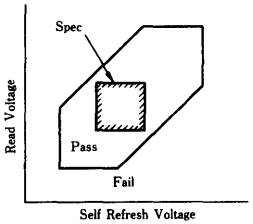


Figure 2-10. PSRAM Operating Voltage

PSRAM provides the voltage level detector circuit to reduce self refresh current. However, it should be noted that the circuit increases the current with low supply voltage in self refresh (figure 2-11). Self refresh current also increases at low temperature (figure 2-12).

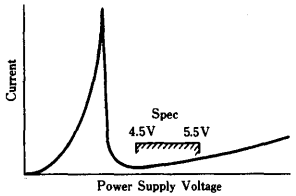


Figure 2-11. Self Refresh Current vs. Voltage

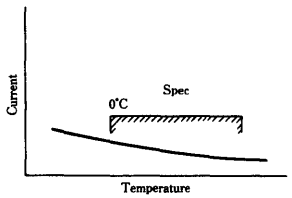


Figure 2-12. Self-Refresh Current vs Temperature

Please use PSRAM within the recommended operation range (V_{CC} more than 4.5 V, temperature more than 0°C) for data retention, especially using a battery.

3. Video RAM

3.1. Multiport Video RAM

Figure 3-1 shows general idea of video RAM. Multiport video RAM provides an internal data register (SAM) with the memory (RAM). Both of them can be accessed asynchronously. Effective graphic display memory is realized by using the random port of the RAM part for graphic processor drawing and the serial port of the SAM part for CRT display.

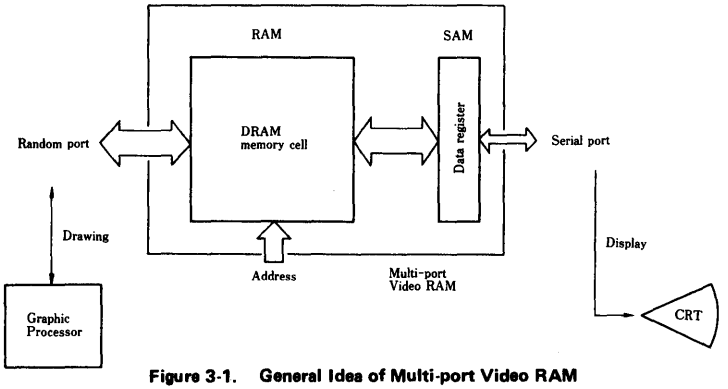


Figure 3-1. General Idea of Multi-port Video RAM

Figure 3-2 shows the block diagram of the 256-kbit multiport video RAM HM53461, and table 3-1 shows the operation modes of the HM53461.

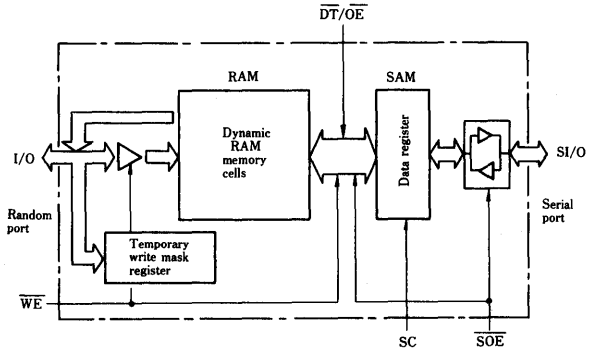


Figure 3-2. Block Diagram of HM53461

The operation modes shown in table 3-1 are described as follows.

Table 3-1. Operation Modes of HM53461

At the falling edge of RAS				RAM modes	SAM modes	
CAS	DT/OE	WE	SOE		SI/O direction	Notes
H	H	H	X	Read/write	Sin/Sout	1, 2, 3
H	H	L	X	Temporary write mask data program	Sin/Sout	1, 2, 3
H	L	H	X	Read transfer	Sout	2
H	L	L	L	Write transfer	Sin	
H	L	L	H	Pseudo transfer	Sin	
L	X	X	X	CBR refresh	Sin/Sout	1,2

H: High
L: Low
X: Don't Care

Notes: 1. Transfer cycle executed previously defines SI/O direction.
2. SI/O is in high impedance state with SOE high, even if the direction is Sout.
3. The HM53461 starts write operation if WE is low at the falling edge of CAS or become low between the falling edge of CAS and the rising edge of RAS.

Read/Write Operation: Read/write is performed on the random port in the same sequence as for a dynamic RAM (figure 3-3). The HM53461 starts the read operation with $\overline{WE}$ high and the write operation at the falling edge of $\overline{WE}$.

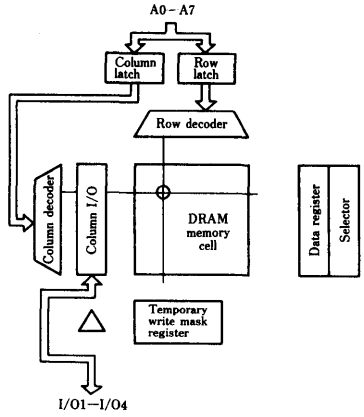


Figure 3-3. Read/Write Operation

Temporary Write Mask Set and Temporary Masked Write Operation: The HM53461 provides temporary masked write operation which inhibits to write data bit-by-bit (write mask) during one $\overline{RAS}$ cycle. Temporary write mask set function defines the bits to be inhibited (figure 3-4). This operation puts the data on I/O1 – I/O4 into the internal temporary write mask register. When 0 is programmed to the register, writing to the corresponding bit is inhibited.

The temporary write mask register is reset at the rising edge of $\overline{RAS}$.

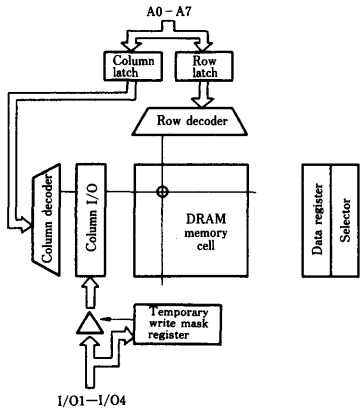


Figure 3-4. Temporary Masked Write Operation

Read Transfer Operation: In this cycle, the HM53461 transfers the data of one row in RAM (1024 bits), which address is specified at the falling edge of $\overline{RAS}$, to SAM (figure 3-5). The start address in SAM can be programmed at the falling edge of $\overline{CAS}$ in this cycle. After data transfer, the serial port turns to serial read mode at the rising edge of $\overline{DT/OE}$.

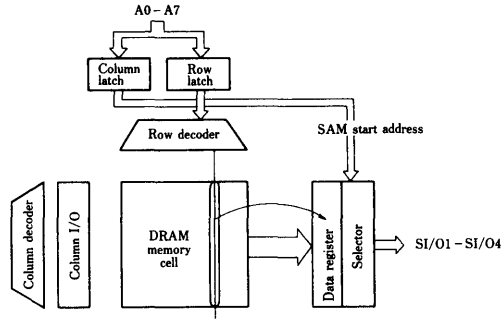


Figure 3-5. Read Transfer Operation

Write Transfer Operation: In this cycle, the HM53461 transfers the data in the SAM data register (1024 bits) to one row in RAM, which address is specified at the falling edge of $\overline{RAS}$ (figure 3-6). The start address in SAM can be programmed in this cycle. After data transfer, serial port turns to serial write mode.

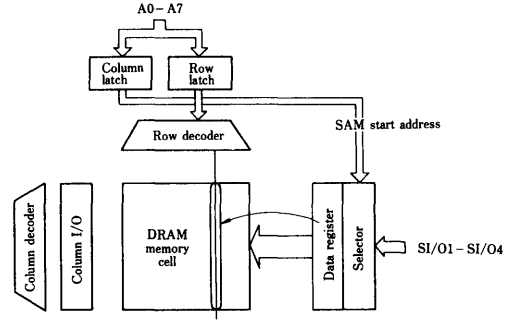


Figure 3-6. Write Transfer Operation

Pseudo Transfer Operation: This operation switches the serial port to serial write mode (figure 3-7). It does not perform data transfer between RAM and SAM. SAM start address can be programmed in this cycle.

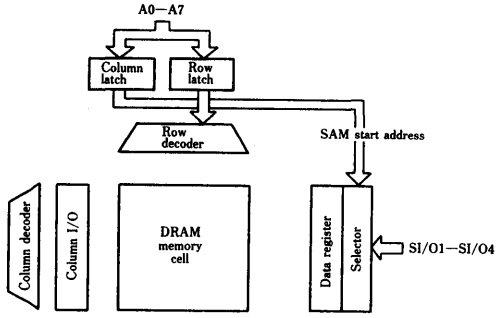


Figure 3-7. Pseudo Transfer Operation

$\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Operation: The HM53461 performs refresh by using the internal address counter in this operation (figure 3-8).

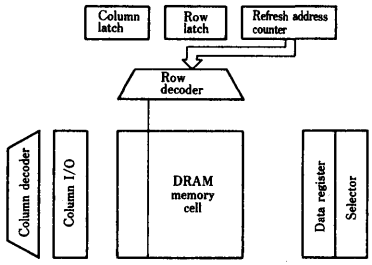


Figure 3-8. $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh

Serial Read/Write Operation: The HM53461 reads/writes the contents of the SAM data register in serial at the rising edge of SC (serial clock input) (figure 3-9). The address for serial access is generated by the internal address pointer, independently of random port operation. It should be considered that serial access is restricted in transfer cycles. The SAM, employing static-type data registers, requires no refresh.

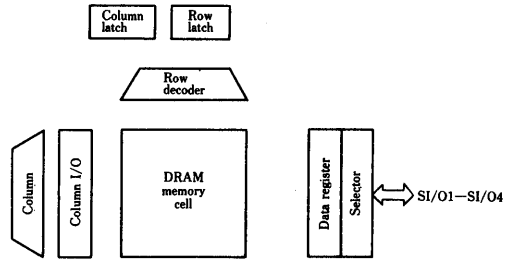


Figure 3-9. Serial Read/Write Operation

The HM53462 is a multiport video RAM, adding logic operation capability to the advantages of HM53461.

Figure 3-10 shows the block diagram. Table 3-2 describes the operation modes.

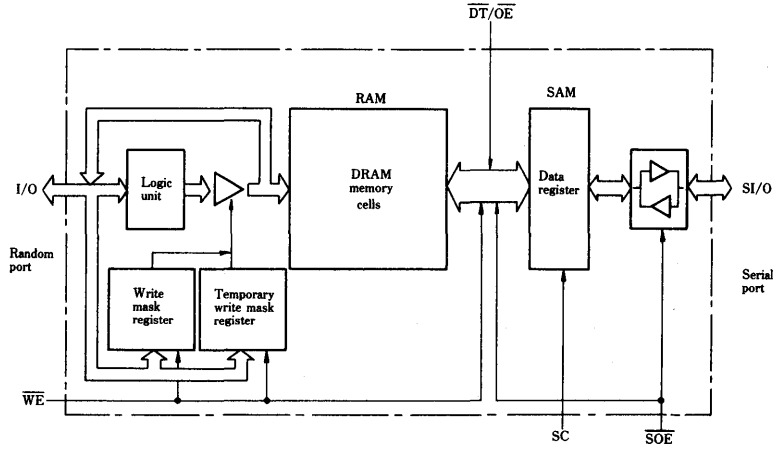


Figure 3-10. Block Diagram of HM53462

Table 3-2. Operation Modes of HM53462

At the falling edge of $\overline{RAS}$				RAM modes	SAM modes	
$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WE}$	$\overline{SOE}$		SI/O direction	Notes
H	H	H	X	Read/write	Sin/Sout	1, 2, 3
H	H	L	X	Temporary masked write	Sin/Sout	1, 2, 3
H	L	H	X	Read transfer	Sout	2
H	L	L	L	Write transfer	Sin	
H	L	L	H	Pseudo transfer	Sin	
L	X	X	X	$\overline{CAS}$-before-$\overline{RAS}$ refresh	Sin/Sout	1,2
L	X	L	X	Logic operation program (CBR Refresh)	Sin/Sout	1,2

H: High L: Low X: Don't Care

Notes: 1. Transfer cycle previously executed defines SI/O direction.
2. SI/O is in high impedance with $\overline{SOE}$ high, even if SI/O direction is Sout.
3. HM53462 writes if $\overline{WE}$ is low at the falling edge of $\overline{CAS}$ or becomes low between the falling edge of $\overline{CAS}$ and the rising edge of RAS.

Logic Operation Programming: This function programs a logic operation (figure 3-11). The logic operation is available until re-programmed or reset. In logic operation mode, HM53462 performs read-modify-write internally when data is written into random port. The result of the logic operation between memory data and written data is put into the address from which the memory data is transferred.

In the logic operation programming cycle, the mask register, which differs from the temporary mask register, is also programmed. It is available until re-programmed.

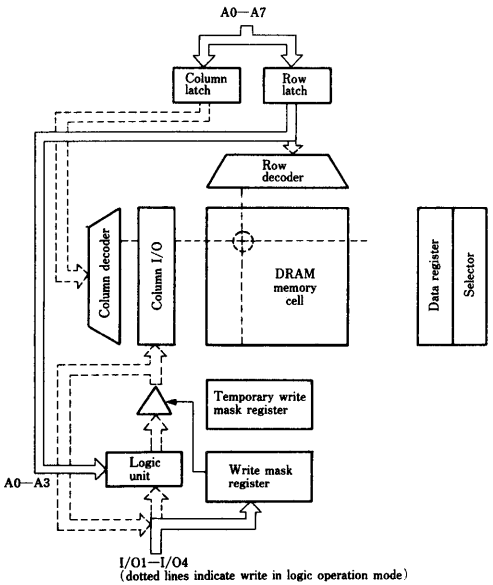


Figure 3-11. Logic Operation Programming

Notes: Notes on using HM53461/HM53462 are as follows.

- Dummy $\overline{RAS}$ cycle. Devices should be initialized by 8 dummy $\overline{RAS}$ cycles (minimum) before access to random port. Refresh cycle can be inserted for initialization. It is recommended that the system be initialized by dummy $\overline{RAS}$ cycle in the automatic reset time of the processor.
- Bypass capacitor. One bypass capacitor should be inserted between V_{CC} and V_{SS} to each device. The V_{CC} pin should be connected to the capacitor by the shortest path. A capacitor of several μF is suitable.
- Negative voltage input. Negative polarity input level to input pin or I/O pin should be under −1 V. In this range, it has no effect on device characteristics or RAM/SAM data retention.
- Initialization of logic operation mode (HM53462). The logic operation programming cycle should be executed before access to the random port to initialize logic operation mode after power on. At this time, the operation codes (0101) and all 1 write mask data are recommended.

3.2. Line Memory

Hitachi has produced a line memory for line buffers with simple circuits, providing specific functions as described below.

The line buffer can improve picture quality by storing 1 horizontal line data. It has following features.

- Capacity to store 1 horizontal line data
- High-speed operation matching the sampling speed of PAL TV signal (4 fsc/8 fsc) or NTSC TV signal (4 fsc/8 fsc).

- Separate data inputs/outputs and capability of serial data inputs and outputs.

The conventional line buffer composed of high speed static RAMs requires separate input/output for double buffer organization. It also requires interleaving for high speed operation, matching 4 fsc/8 fsc, where fsc is the subcarrier frequency. In addition, external circuits are needed for serial address scan.

The line memory provides all of these functions. Figure 3-12 shows the standard organization of a conventional memory buffer and figure 3-13 shows the block diagram of line memory.

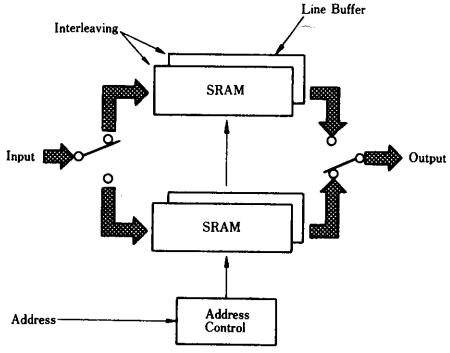


Figure 3-12. Standard Organization of Conventional Line Buffer

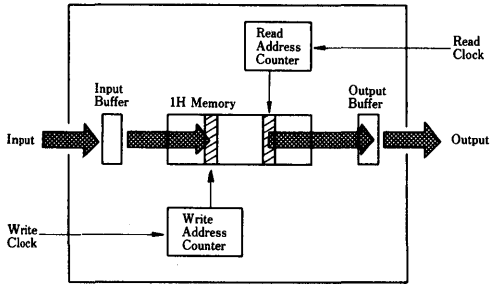


Figure 3-13. Block Diagram of Line Memory

The Hitachi HM63021 is a 2048-word x 8-bit line memory storing 2 horizontal lines of data.

It has five different modes for various video graphic system applications. It realizes high speed operations for PAL and NTSC TV signals, and dissipates little power employing 1.3 μm CMOS technology and static-type memory cells.

The features of the HM63021 are described as follows:

- Five modes for various video graphic system applications
  - Delay line mode
  - Alternate 1H/2H delay mode
  - TBC (Time-Base Corrector) mode
  - Double speed conversion mode
  - Time-base compression/expansion mode
- High speed cycle time
  - HM63021-34: 34 ns min (corresponds to 8 fsc of NTSC TV signal)
  - HM63021-28: 28 ns min (corresponds to 8 fsc of PAL TV signal).

Line memory in the system using digital signal processing technologies offers following applications:

1. comb filter
2. double-speed conversion (non-interlace)
3. compression/expansion of graphics (picture-in-picture)
4. dropout canceller
5. time-base corrector
6. noise reducer

4. Dynamic RAM

4.1. Dynamic RAM Memory Cell

The dynamic RAM memory cell consists of 1 MOS transistor and 1 capacitor, as shown in figure 4-1. It detects the data in the cell (1 or 0) by the charge stored in capacitor. Dynamic RAM offers higher density than that of static RAM because of fewer components per chip.

However, Dynamic RAM must rewrite data, called refresh, in a defined cycle because the charge stored in the capacitor leaks.

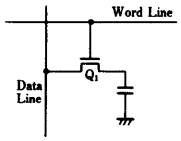


Figure 4-1. Memory Cell of Dynamic RAM

4.2. Power On Procedure

After turning on power, to set the internal memory circuitry, hold for more than 100 μs, then apply eight or more dummy cycles before operation. The dummy cycle may be either a normal read/write cycle or a refresh cycle. When using an internal refresh counter, eight or more $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required as dummy cycles.

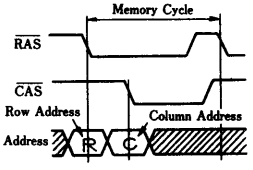
4.3 Address Multiplexing

Dynamic RAMs are used to increase capacity because of their smaller cell area. In using dynamic RAMs in systems, however, it is desirable to increase the memory density by using smaller packages. To reduce the number of pins and the package size, address multiplexing is used.

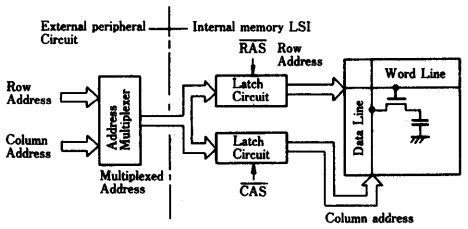
Using a 1-Mbit dynamic RAM, 20-address signals are necessary to select one of 1,048,576 memory cells. Address multiplexing allows address signals to be applied to each address pin. Thus only 10-address input pins are required to select one of 1048,576 addresses. Multiplexed address inputs are latched as follows: $\overline{RAS}$ (Row Address Strobe) selects one of word lines according to the row address signal, and one of column decoders is selected by $\overline{CAS}$ (column address strobe) following column address signal. Although two extra signals, $\overline{RAS}$ and $\overline{CAS}$, are required, the number of address pins is reduced to half. Figure 4-2 shows the pin arrangement, address latch waveform, and the block diagram of address-multiplexed 1-Mbit dynamic RAM. Systems need an address multiplexer in order to latch the multiplexed address signals into the device.

A0 – A9	Address Inputs
$\overline{CAS}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
A0 – A8	Refresh Address Inputs

(a) Pin Arrangement



(b) Address Latch

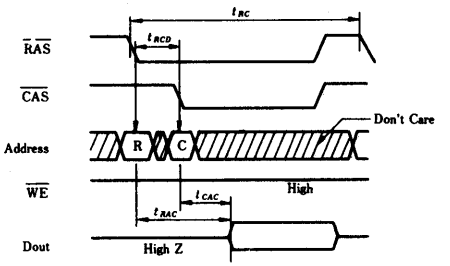


(c) Block diagram of Address Multiplexing

Figure 4-2 Address Multiplexing of Dynamic RAMs

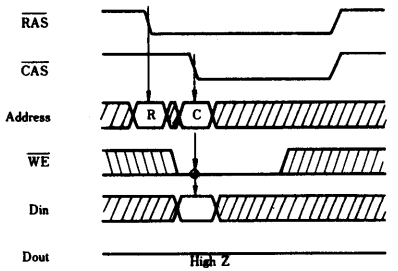
4.4. Dynamic RAM Function

Figure 4-3 shows the normal function of Dynamic RAM.

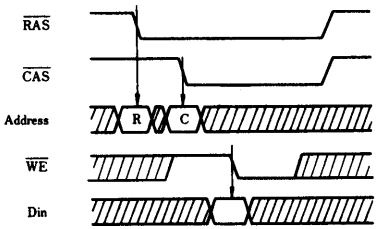


(a) Read Cycle

t_{RC}: Random Read or Write Cycle Time
t_{RCD}: RAS to CAS Delay Time
t_{RAC}: Access Time from RAS
t_{CAC}: Access Time from CAS
R: Row Address
C: Column Address

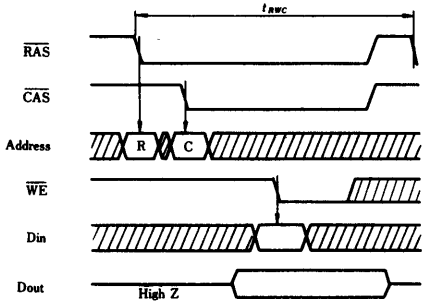


(Early Write)



(Delayed Write)

(b) Write Cycle



(c) Read-Modify-Write Cycle

t_{RWC}: Read-Write Cycle Time

Figure 4-3 Normal Function of Dynamic RAM

Read Cycle: In the read cycle, a row address is latched at the falling edge of RAS, and a column address is latched at the falling edge of CAS after the RAS falling edge. If WE is high, the data is read out from Dout with the access time of t_{CAC} (Access time from CAS) or t_{RAC} (Access time from RAS).

The t_{RCD} maximum (RAS to CAS delay time) is specified only to guarantee the specified minimum values of other timings such as the cycle time, RAS/CAS pulse width. Therefore, when using these timings with more than the specified minimum value, there is no need to limit the t_{RCD} to the specified maximum value.

Write Cycle: Dynamic RAM provides two write cycle modes: early write cycle and delayed write cycle. In the early write cycle, when WE is low, data is written into Din at the falling edge of CAS. In delayed write cycle, when WE is high, data is written into Din at the falling edge of WE after CAS falling.

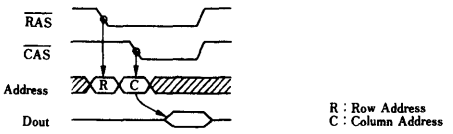
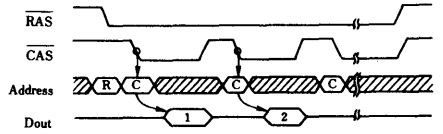
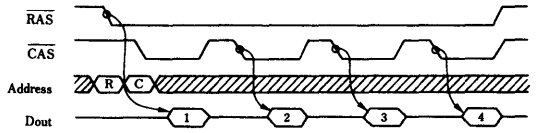
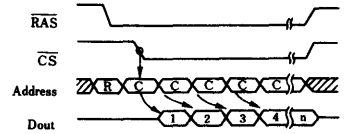
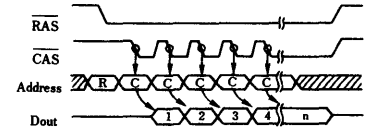
Read-Modify-Write Cycle: The read-modify-write

cycle is initiated by taking $\overline{WE}$ high. Data is read out from Dout at the falling edge of $\overline{CAS}$ with $\overline{WE}$ high. Then, when $\overline{WE}$ goes low, data is written into the same address from Din in the same cycle.
The cycle time in the read-modify-write mode (t_{RWC}) is longer than the cycle time in read/write mode (t_{RC}).

4.5 High Speed Access Mode

Dynamic RAM access time is typically longer than that of static RAMs. To realize higher speed operation, they have high speed access modes.
The read operation in dynamic RAM is performed as follows:
When a word line is selected by row address, all data in the memory cells connected to the selected word line is transferred to sense amplifiers. One of these sense amplifiers is selected by the column address, and its contents are output.
The output of data from other sense amplifiers is controlled only by the column address.
Access controlled only by column address with the row address fixed is called high speed access mode.
Table 4-1 compares each mode.
Page Mode: This is the most typical access mode in dynamic RAM. The column address is switched synchronized with $\overline{CAS}$ falling.
Nibble Mode: In a nibble mode dynamic RAM,

Table 4-1. Comparison of Dynamic RAM High Speed Access Modes

Normal Mode	
Page Mode	
Nibble Mode	
Static Column Mode	
High-Speed Page Mode	

data from 4 sequential addresses is stored in the 4-bit output latch circuits. Output is provided by the $\overline{CAS}$ signal, which controls the latch circuits.
When 4 addresses are accessed sequentially, the row addresses on and after second bit need not be selected. Therefore, it facilitates the timing design. In nibble mode, the operation is limited to 4 addresses, however, it enables faster access (t_{NAC}) than that in page mode.

Static Column Mode: In static column mode, the column address is switched without the synchronized signal by high-speed static RAM technology in the peripheral circuits.

High Speed Page Mode: This mode is the advanced mode of static column mode, with $\overline{CAS}$ providing the address latch function.

4.6 Refresh

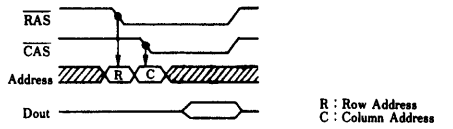
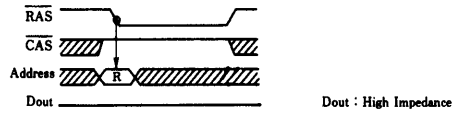
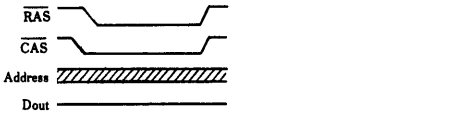
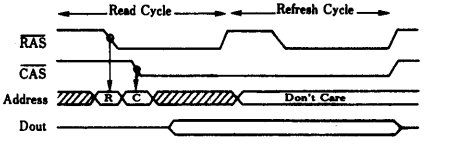
Refresh operation is performed by accessing every word line within the specified time (refresh cycle). Table 4-2 compares the following refresh modes in dynamic RAM.

$\overline{RAS}$ Only Refresh: In $\overline{RAS}$ only refresh mode, refresh can be completed by selecting only row addresses synchronized with $\overline{RAS}$.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh: This mode refreshes by the $\overline{CAS}$ falling edge before $\overline{RAS}$ in the period defined by the internal refresh address generator. This mode simplifies the external address multiplexer.

Hidden Refresh: In hidden refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh is performed while output data is valid.

Table 4-2. Comparison of Dynamic RAM Refresh Modes

Read	
$\overline{RAS}$ Only Refresh	
$\overline{CAS}$ before $\overline{RAS}$ Refresh	
Hidden Refresh	

▨: Don't care

5. EEPROM

5.1. EEPROM Memory Cell

EEPROM is electrically erasable and programmable ROM, which can be erased or written remotely while the system is in operation.

The Hitachi EEPROM memory cell is MNOS (Metal Nitride Oxide Semiconductor) type, as shown in figure 5-1.

An MNOS memory cell consists of two layers of oxide film and nitride film. The thickness of oxide film is about 20 Å and that of nitride film is 300 to 500 Å. There are traps in the boundary of the oxide and nitride films to catch electrons. Electrons move by the tunneling phenomenon between the substrate and traps.

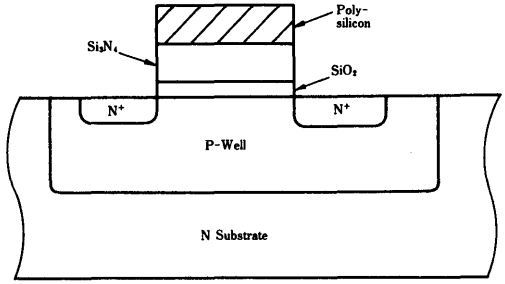


Figure 5-1. MNOS Type Memory Transistor

5.2. 64-kbit CMOS EEPROM Function

Page Write Function: The 64-kbit HN58C65 can latch 32 bytes (max) and write them in one write cycle. Writer cycle time is specified as 10 ms (max.). The effective byte write speed of HN58C65 in page write mode is:

10 ms/32 bytes = 0.31 ms/byte

Thus it takes only 2.56 seconds to write the whole HN58C65. Figure 5.2 shows internal operation. The following describes operation sequence:

1. 32-byte memory cell data at the row address selected by address pins A5 – A12 is latched.
2. Latched data at the column address specified by address pins A0 – A4 is altered with write data, which is put into Din buffer from I/O pins I/O0 – I/O7.
   The 32 bytes (max) of latched data are altered by repeating this operation 32 times.
3. 32-bytes memory cell data in the selected row (1) are erased (All 1).
4. Latched data is written into the selected row (3).
5. CPU acknowledges the completion of write cycle by the internal timer. The HN58C65 provides RDY/$\overline{\text{BUSY}}$ and $\overline{\text{Data}}$ polling to indicate the write completion.

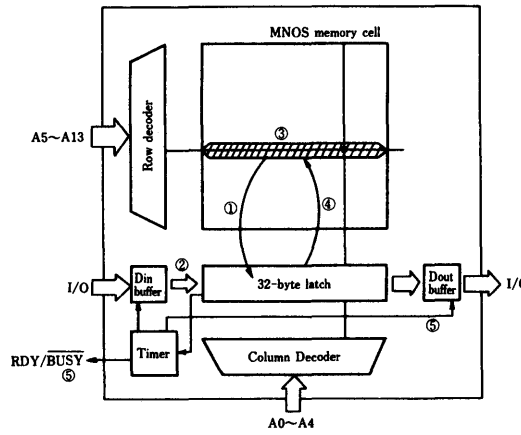


Figure 5-2. HN58C65 Page Write

Internal Timer: The HN58C65 indicates the completion of data write to the CPU by using the internal timer. The HN58C65 enters next cycle as soon as detecting the completion of write. This function offers high system throughput as the CPU can access other devices during write cycle. The HN58C65 has two functions, RDY/$\overline{\text{Busy}}$ and $\overline{\text{Data}}$ polling, to indicate the completion of data write.

The RDY/$\overline{\text{Busy}}$ approach indicates the completion of data write by using pin 1. It is low when the HN58C65 is in data write operation ($\overline{\text{Busy}}$) and turns to high impedance state at the end of data write (RDY). RDY/$\overline{\text{Busy}}$ pin should be pulled up as it uses open drain output. The RDY/$\overline{\text{Busy}}$ pins can be wired-OR when using several HN58C65s.

The $\overline{\text{Data}}$ polling approach, implemented by software, indicates the completion of data write through pin 19 (I/O7). While the data write is not completed, I/O7 shows the inverted data of what was written in the last cycle. In using this approach, RDY/$\overline{\text{Busy}}$ pin should be opened or grounded. The $\overline{\text{Data}}$ polling approach can acknowledge the completion of data write in an individual HN58C65, even if several HN58C65s are used in the system.

Data Protection: EEPROM performs data write with a higher voltage (V_{PP}) than power supply voltage (V_{CC}). The HN58C65 internally generates V_{PP} by a high voltage generator with the combination of control pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$). It supports the following functions to avoid accidental data write (data protection).

1. Data protection against the noise on the control pins ($\overline{\text{CE}}$, $\overline{\text{OE}}$, $\overline{\text{WE}}$) during operation.
2. Data protection against the noise at power-on/power-off.

6. EPROM/OTPROM

6.1. EPROM Programming

Figure 6-1 shows the sectional structure of an EPROM memory cell. The upper gate, one of the gates made of two-layered polycrystalline silicon, is called the control gate and is connected to a word line. The lower layer is called the floating gate and is not connected. This memory cell is programmed as follows: With substrate and source grounded, apply high voltage between drain and control gate. Then, an electric potential incline occurs between source and drain so that intensity of the electric field becomes high near the drain. Because of this electric field, electrons are accelerated and so-called hot electrons are generated, which jump over the energy barrier of SiO_2 film. Hot electrons are pulled by the electric potential of the control gate and pour into the floating gate. Electrons stored in the floating gate remain stable, as they fall into a well surrounded by an energy barrier of SiO_2 film. Therefore, it is evident that the quality of SiO_2 film surrounding the floating gate is essential for good data retention characteristics. To keep data retention in the 5- or 10-year range, high quality SiO_2 film is needed.

Figure 6-2. shows the fundamental characteristics of the EPROM transistor. While I_D in a non-programmed transistor begins to flow with V_G of about 1V, the current in a programmed transistor does not flow until V_G rises to 7 V – 10 V. Therefore, if the voltage of word line applied to the control gate is about 5 V in readout, the non-programmed memory transistor will be on, and the programmed one will be off. This means that the data can be read out by means of the same structure as NOR-type mask ROM.

6.2. Erasing EPROM

When shipped, all bits of the EPROM are at logic 1 with all electrons in the floating gate released (erase). Changing the logic 1 to logic 0 through the application of the specified waveform and voltage, programs the necessary information. The higher the V_{PP} voltage and the longer the program pulse width t_{PW}, the more electrons can be programmed in, as shown in Figure 6-3. If V_{PP} exceeds the rated value, such as by overshoot, the p-n junction of the memory may yield to permanent breakdown. To avoid this, check V_{PP} overshoot of the PROM programmer. Also, check negative-voltage-induced noise at other terminals, which can create a parasitic transistor effect and reduce the yield voltage.

Hitachi's EPROMs can usually be written and erased more than 100 times.

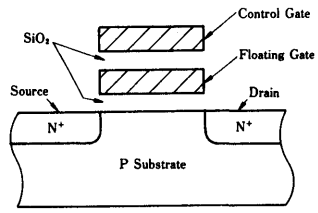


Figure 6-1. Cross Section of EPROM Memory Cell

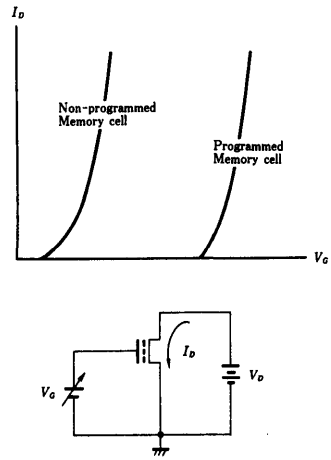


Figure 6-2. Fundamental Characteristic of EPROM Memory Cell

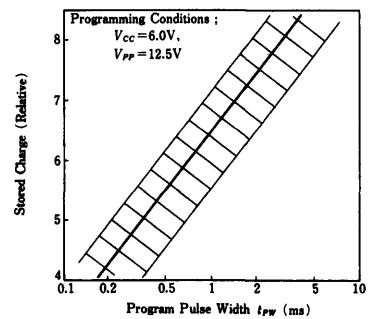


Figure 6-3. Standard Programming Characteristics of EPROMs

EPROMs are erased by ultraviolet light exposure through a transparent window on the package. Electrons in the floating gate get energy from photons and become hot electrons again with enough energy to go over the energy barrier of SiO_2

film. The hot electrons go through to the control gate or the substrate and erasure is completed. Therefore, light with enough energy to get the electrons over the energy barrier of SiO_2 film is needed for erasure. Light energy is proportional to its frequency, and described as $E = h\nu$. E means the energy of light, h is Planck's constant, ν is light frequency. Erasure isn't caused by light over certain wavelengths, and under certain wavelengths, erasure does occur. However, erasure time depends upon the quantity of photons, therefore erasure time cannot be shortened by shorter wavelength. Figure 6-4 shows the relation between wavelength and erasure effectiveness. Erasure starts at about 4000 Å, and is saturated at about 3000Å.

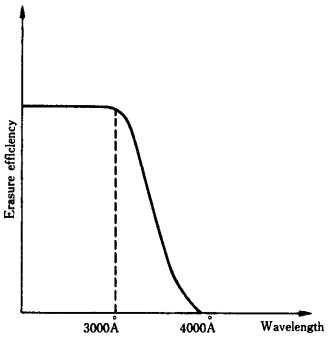


Figure 6-4. Erasure Efficiency of EPROM

For erasure, the wavelength and minimum irradiation rate of ultraviolet light must be 2,537Å and 15 $W \cdot s/cm^2$ respectively. These conditions can be met by placing the device 2 – 3 cm below a 12,000 W/cm^2 UV lamp for about 20 minutes.

The UV transmittance of the transparent lid materials is about 70%. However, it is influenced by contamination or foreign materials on the lid surface. Contamination or foreign materials should be removed with a solvent such as alcohol that does not damage the package.

Figure 6-5 shows EPROM standard erasure characteristics.

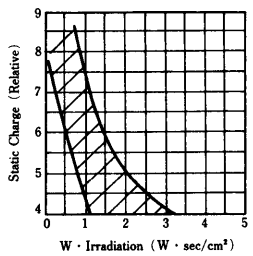


Figure 6-5. Standard Erasure Characteristics

6.3. EPROM Data Retention Characteristic

About 2 to 20×10^{-14} coulomb of electrons are accumulated in the floating gate when programmed. However, these electrons dissipate with time. Then the data may be inverted. The mechanism of electron dissipation is generally explained as follows.

Data Dissipation by Heat: The electrons at the floating gate are in a non-equilibrium state, so the dissipation of electrons by thermal energy is unavoidable. Therefore, the data retention time depends on temperature. Figure 6-6 shows typical data retention characteristics. The data retention time is proportional to the reciprocal of absolute temperature.

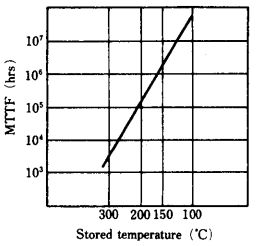


Figure 6-6. EPROM's Data Rentention Characteristic

Data Dissipation by Ultraviolet Light: Ultraviolet rays at a wavelength of not greater than 3,000 – 4000Å is capable of releasing the electric charge at

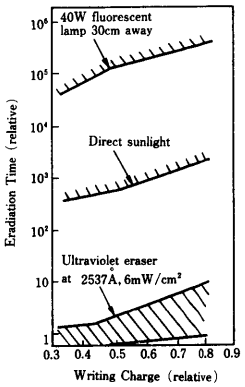


Figure 6-7. EPROM's Data Retention Time

floating gate of the EPROM with varying efficiencies. Fluorescent light and sunlight contain some ultraviolet light, and so prolonged exposure to these lights can cause data corruption as a result of electric charge dissipation. Figure 6-7 shows the standard, data retention time under an ultraviolet eraser, sunlight and fluorescent lighting.

6.4 Optimized High-Speed Programming

With the increase of EPROM density, the time for programming becomes more important. The method for high speed programming has been developed and put into practical use according to each EPROM generation.

Following explains three methods for High-Speed programming.

(1) First generation ... conventional programming.

This method is employed in the 3 μm and 5 μm process products. Programming is performed with a uniform pulse of 50 ms per byte. Although it is the advantage that it applies enough pulse to all bits, it takes much time to program high density devices.

(2) Second generation ... High performance programming

This method is employed in 2 μm process product. "High Performance programming (figure 6-8) is performed with a base pulse of 1 ms width. It repeats programming and reading (verifying) until the data is programmed enough. There are two good points in this programming.

First, the programming itself is performed with optimum program time depending on the capability of each memory cell.

Second, after verification, the data is programmed using three times as long a pulse and assures high-reliability data retention.

(3) Third generation ... Fast High Reliability Programming

This method is employed in the 1.3 μm process products. "Fast High-Reliability Programming" (figure 6-9) is performed with a base pulse of 0.2 ms. It also shortenes a supplement pulse width to one-third of that of "High Performance Programming". As a result, this method realizes short programming time, reduced to one-tenth theoretically.

1M bit EPROM series employ "Page Programming", which programs 32-bit at once (figure 6-10), reducing programming time to a quarter of "Fast High-Reliability Programming" for 128k x 8 organization and a half for 64k x 16 organization.

Figure 6-11 shows the programming time of above methods.

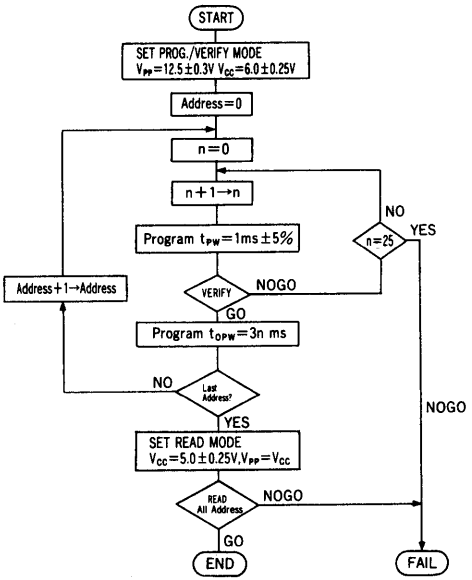


Figure 6-8. High-Speed Programming (High Performance Programming)

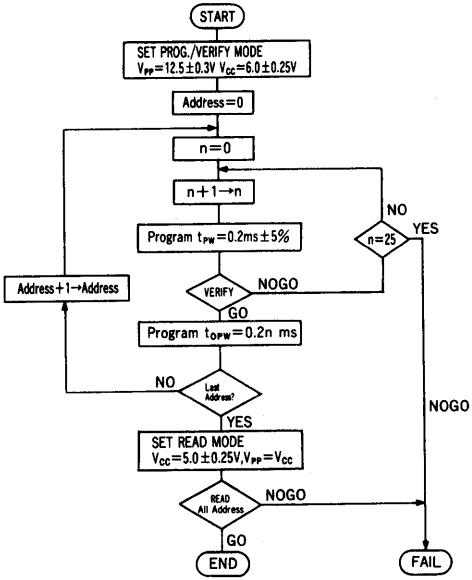


Figure 6-9. 0.2ms High-Speed Programming (Fast High-Reliability Programming)

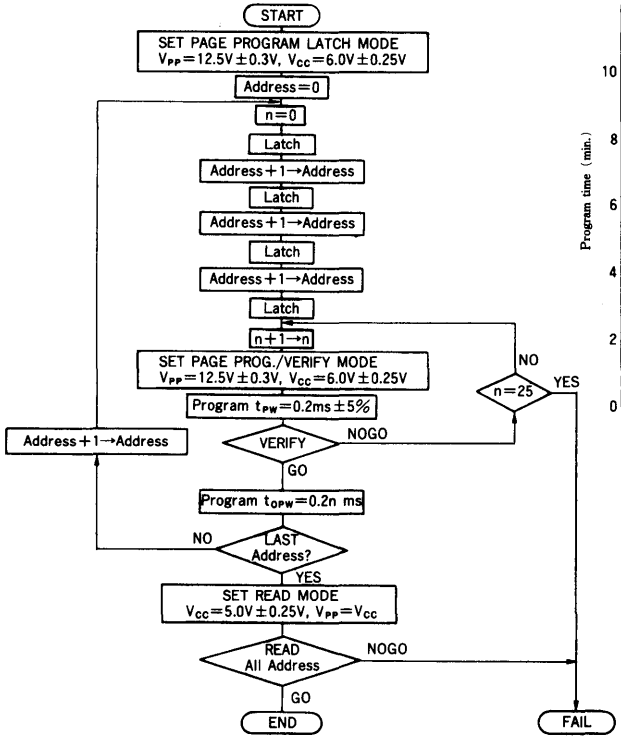
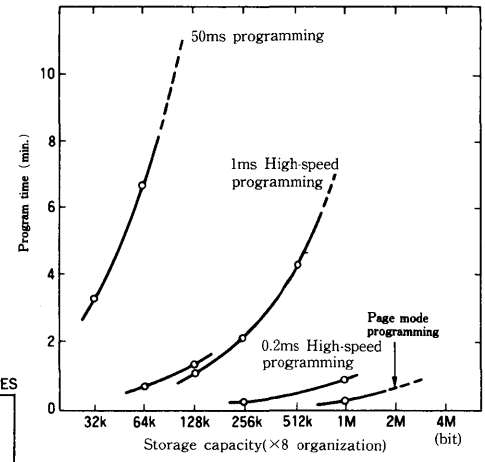


Figure 6-10. Page-Mode Programming (Page Programming)



(Note) Actual program time differs according to the programmer.

Figure 6-11. Shortened Program Time by High-Speed Programming.

6.5 Device Indentifier Code

EPROM programming conditions depend on EPROM manufacturers and device types, confusion may cause miss operation. As a countermeasure some EPROMs provide device identifier code including such information as manufacture and device type. Some newly developed commercial EPROM programmers can set write conditions automatically by recognizing this code.

Different programming conditions are as follows: (1) program voltage, (2) program timing, (3) high-performance programming algorithm, (4) pin configuration. The Hitachi EPROM has a device identifier code area besides the memory access area, as shown in figure 6-12.

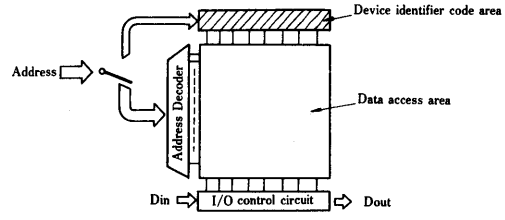


Figure 6-12. Device Identifier Code

Table 6-1 describes how to use the device identifier code. Setting A9 at 12 V and A1 – A8, A10 – A13 at V_{IL} access the device identifier code area and I/O0 – I/O7 output the programming condition code with V_{IL} or V_{IH} of A0.

Tablel 6-1. Hitachi EPROM Device Identifier Code

		A_0	I/O8–I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Hex Data
Manufacturer Code	Hitachi	V_{IL}	–	0	0	0	0	0	1	1	1	07
ROM code	HN27128A	V_{IH}	–	0	0	0	0	1	1	1	1	0D
	HN27256		–	0	0	0	1	0	0	0	0	10
	HN27C256		–	1	0	1	1	0	0	0	0	B0
	HN27C256H		–	0	0	1	1	0	0	0	1	31
	HN27C256A		–	0	0	1	1	0	0	0	1	31
	HN27512		–	1	0	0	1	0	1	0	0	94
	HN27C1024H		–	1	0	1	1	1	0	1	0	BA

A9: 12V
A1 -A8, A10 -A13: V_{IL}
A14, A15: Don't care

6.6 Shielding Label

When using an EPROM in an environment where it can be exposed to ultraviolet light, Hitachi recommends putting a shielding label on its transparent lid to absorb ultraviolet light. In choosing a shielding label, the following points should be carefully checked.

★ Adhesiveness (mechanical strength). Avoid repeated attaching or exposure to dust that may reduce the adhesive strength. Ultraviolet erasing and reprogramming are recommended after stripping off an attached label. (When the need arises to change a label, it is advisable to put a new one on over the old one since peeling may create a static charge.)

★ Allowable temperature range. Use the shielding label in an environment whose temperature falls within the specified allowable temperature range. Beyond the specified temperature range, the paste on the label may harden or stick too fast. When it hardens, the label may come off easily. When it sticks too fast, the paste may remain on the window glass after the label has been removed.

★ Moisture resistance. Use the shielding label in an environment whose humidity falls within the specified allowable humidity range.

6.7 EPROM Programmer

The EPROM programmer stores the user's program in its internal RAM and writes the program in the EPROM. For this programming, 3 functions at least are necessary: blank check function prior to programming, programming function, and the verify function after programming. Figure 6-13 shows the programming flow chart. Some programmers check for pin contact failure or the reverse insertion before the blank check.

The outline of each block is as follows.

1. Pin contact check
   In the ROM pin and socket connection test, checking is normally performed by detecting the forward current at each EPROM pin. Care is necessary as this forward biased resistance differs in products of each company.
2. Reverse insertion check
   This check detects the reverse insertion of the device, places the equipment in reset mode and protects the device and equipment.
3. Blank check
   This check is performed before programming. It checks whether the device is an erased EPROM, or it preventing EPROM reprogramming. Since the output data in the erased condition are 1 (high level), check whether or not data in EPROM are all 1. It will fail-stop even when one bit is 0 (low level). Normally, it is designed to provide warning with a lamp or buzzer.
4. Programming
   The function of programming the data in the internal RAM of the programmer into EPROM will fail-stop when programming cannot be done. The normal flow is as shown in figure 6-14. The EPROM data will be read out prior to programming and compared with programming data. If they coincide, programming will be skipped and if they differ, programming will be performed. Then, the data will be read out again and compared with the programming data, and if they coincide, the programmer will progress to the next address.
5. Verify
   This function checks after programming completion whether or not the programming is correct when comparing with the data in the internal RAM of the programmer. It performs fail-stop when they do not coincide. Normally, when it fails, it lights the fail lamp and displays

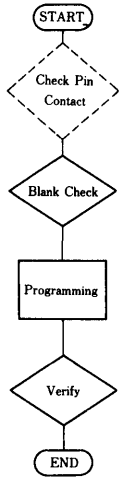


Figure 6-13. Programming Flow Chart of EPROM Programmer (1)

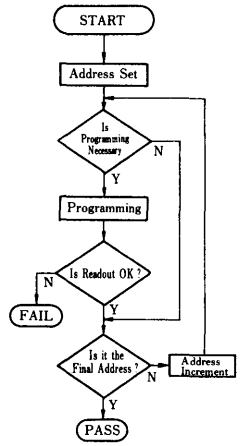


Figure 6-14. Programming Flow Chart of EPROM Programmer (2)

the address and data.

6. How to input the program
   Table 6-2 shows several methods for inputting the program data to the internal RAM of the programmer. Normally, paper tape input and teletypewriter input are prefered options.

Table 6-2. EPROM Data Input

Method	Content
Copy input	Input by copying the master ROM.
Manual input	Input by the keyswitch on the front panel. Used for correction or revision of program
Paper tape input	Read the paper tape furnished from the host system with the tape reader
Teletypewriter input	Input with the teletypewriter. Preparation, correction, and list preparation of the program can be made.

6.8 Handling EPROMs

Touched with a charged human body or rubbed with plastics or dry cloth, the glass window of an EPROM generates static electricity which causes device malfunctions. Typical malfunctions are faulty blanking and write margin setting that give the false impression that information has been correctly written in. As already reported at the international conferences concerning the reliability of LSI chips, this is due to the prolonged retention of electric charge (resulting from the static electricity) on the glass window. Such malfunctions can be eliminated by neutralizing the charges by irradiating with ultraviolet rays for a short time. The EPROM should be reprogrammed after this irradiation since it reduces the electric charges in the floating gate, too. The basic countermeasure is to prevent the charging of the window, which can be achieved by the following methods as in the prevention of common static breakdown of ICs.

1. Ground operators who handle the EPROM. Avoid using things such as gloves that may generate static electricity.
2. Refrain from rubbing the glass window with plastic or other materials that may generate static electricity.
3. Avoid the use of coolant sprays which contain some ions.
4. Use shielding labels (especially those containing conductive substances) that can evenly distribute established charge.

6.9 Ensuring OTPROM Reliability

One time electrically programmable ROM (OTPROM) has two kinds of packages: standard dual in-line package (DIP) and small outline package (SOP). It is one time only programmable because it has no window for ultraviolet light exposure; testing by programming and erasure cannot be performed after it is assembled.

So, Hitachi performs screening test for programming, access time, and data retention on wafers at proving test.

However, rare defects may occur in the assembly process cannot be completely removed in final test screening which is only a reading test.

Therefore, Hitachi recommends that users perform high temperature baking after programming devices to ensure high reliability.

Detailed conditions and procedures for screening are shown in figure 6-15. First, program and verify devices. Then, leave them without bias at 125 to 150°C for 24 to 48 hours.

After that, check read-out function and remove the chips with data retention failures.

From the results of devices in which the recommended screening test is properly performed, we confirm that the data retention characteristics of OTPROMs are equal to general EPROMs.

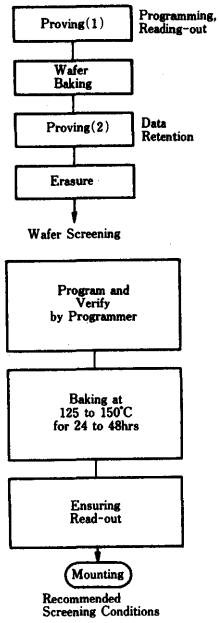


Figure 6-15. Screening Flow Chart of OTPROM

S0 indicates the head of the file and S9 indicates the end of the file. The actual data starts following S1. This means that the data starts from the address (hexadecimal) indicated in the address size. The address of the address size of the data recorder is compared with the next data recorder address by counting in increments of 1 byte of the data and checking whether it is sequential or not. The printed example of the HMCS6800 load module mode is as shown in figure 7-3.

```
Header Record  →S00B000058204558414D504CB5
Data Record    →S113F0007EF5587EF7897EFAA77EF9C07EF9C47E24
Data Record    →S112F010FA657EFA8B7EFAA07EF9DC7EFA247E06
End of
File Record    →S9030000FC
```

Figure 7-3. HMCS6800 Load Module Example

If an address is skipped, enter the skipped address into the "ROM Specification Identification Sheet" and the data (00 or FF) entered into the skipped address.

5. BNPF mode

   One word is symbolized by the word start mark B, the bit content represented by 8 characters of P and N, and the BNPF slice composed of successive 10 characters of the work end mark F.

   The contents from F of one BNPF slice up to B of the next BNPF slice are ignored.

   (Example) The code of AA (hexadecimal) is symbolized as shown in figure 7-4.

   It is necessary to designate the bit pattern (BNPF slice) on all ROM addresses. Therefore, the term of the ROM head address of "ROM Specification Identification Sheet" always becomes 0.

   B . . . . . Indicates start of 1 word.
   N . . . . . Indicates 1 bit data.
   P . . . . . Indicates 1 bit of 1 data.
   F . . . . . Indicates end of 1 word.

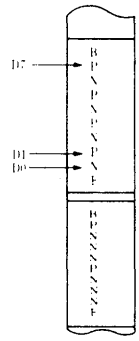


Figure 7-4. BNPF Mode Example

7.3 Specification of Floppy Disk

1. Use the following type of floppy disk (figure 7-5):

   Type. . . . 8 Inch Single Sided and Single Density
   Number of Sectors 26
   Number of Tracks 77

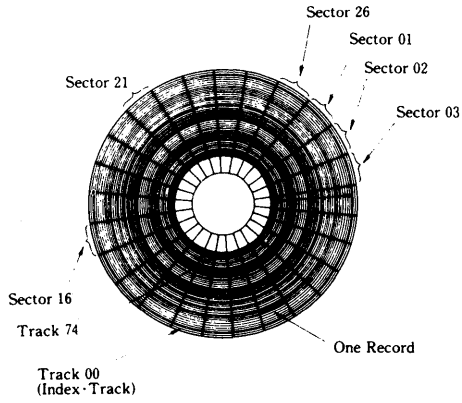


Figure 7-5. Floppy Disk Format

2. Use EBCDIC as the use code.
3. Format the floppy disk as described below. Composition is described in table 7-1.

   Record size . . . . . 80 byte/1 record

Table 7-1. Floppy Disk Composition

No.	Item	Location	
		Track	Sector
1	Standard Volume Label	00	07
2	Standard Head Label	00	08 – 26
3	Data Area	01 – 73	01 – 26
4	Alternal Track	75, 76	01 – 26
5	Spare Track	00 74	01 – 06 01 – 26

7. MASK ROM PROGRAMMING INSTRUCTION

The writing of the custom program code into mask ROMs is performed by the CAD system on a large-sized computer. ROM code data should conform to specifications given below, using either paper tape, EPROM, or magnetic tape. Additional instructions, such as chip select and customers' part number, should be given in the "ROM Specification Identification Sheet"

7.1 Specification of EPROM

1. Submit the three sets of the EPROM-stored data. Specify the address of the EPROM in the case of two or four EPROMs.
2. The ROM code data is input from the start address to Final Address in the EPROM.
3. Type of EPROM
   HN482764 (8-kword x 8-bit, 2764 Compatible)
   HN4827128 (16-kword x 8-bit, 27128 Compatible)
   HN27256 (32-kword x 8-bit, 27256 Compatible)
   HN27C256 (32-kword x 8-bit, 27C256 Compatible)

7.2 Specification of Magnetic Tape

1. Use the following type of magnetic tape which can be used by a magnetic tape device compatible with the IBM magnetic tape device.
   Length . . . . . 2,400 feet, 1,200 feet or 600 feet
   Width . . . . . 1/2 inch
   Channel . . . . . 9 channels
   Bit density . . . . 800 BPI or 1,600 BPI (Clearly state which it is in the "ROM Specification Indetification Sheet".)
2. Use EBCDIC as the use code.
3. Follow the format of the magnetic tape as described below
   No leading tape mark
   No label
   Record size . . . . . 80 byte/1 record
   Block size . . . . . 10 records/1 block
   The end of the file should be indicated by 2 successive tape marks (TM) (figure 7-1).
4. HMCS6800 load module data mode. This mode is the object mode output from the assembler HMCS6800.
   Divide the 8-bit code into the upper and lower 4-bit codes, and convert each into hexadecimal notation.
   Example: The code 1100 0110 is as follows under binary notation.

(Upper 4-bits)	(Low 4-bits)	Bit weight
D7 D6 D5 D4	D3 D2 D1 D0	(ROM output
1 1 0 0	0 1 1 0	equivalence)

   The actual load module mode is shown in figure 7-2.

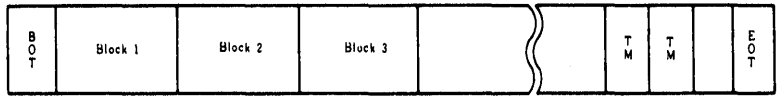


Figure 7-1. Magnetic Tape Format

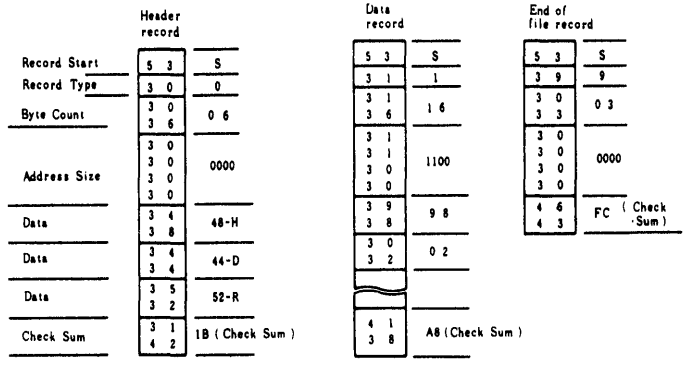


Figure 7-2. HMCS68000 Load Module Data Format

Use the sectors as in figure 7-6. Use one sector for one record, that is, 80 bytes out of 128 bytes used for one record.

4. Data Mode. See data mode for magnetic tape.

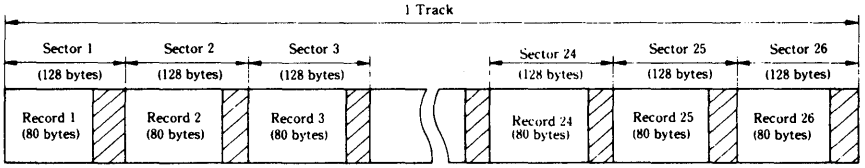


Figure 7-6. Floppy Disk Sector Format

: unused

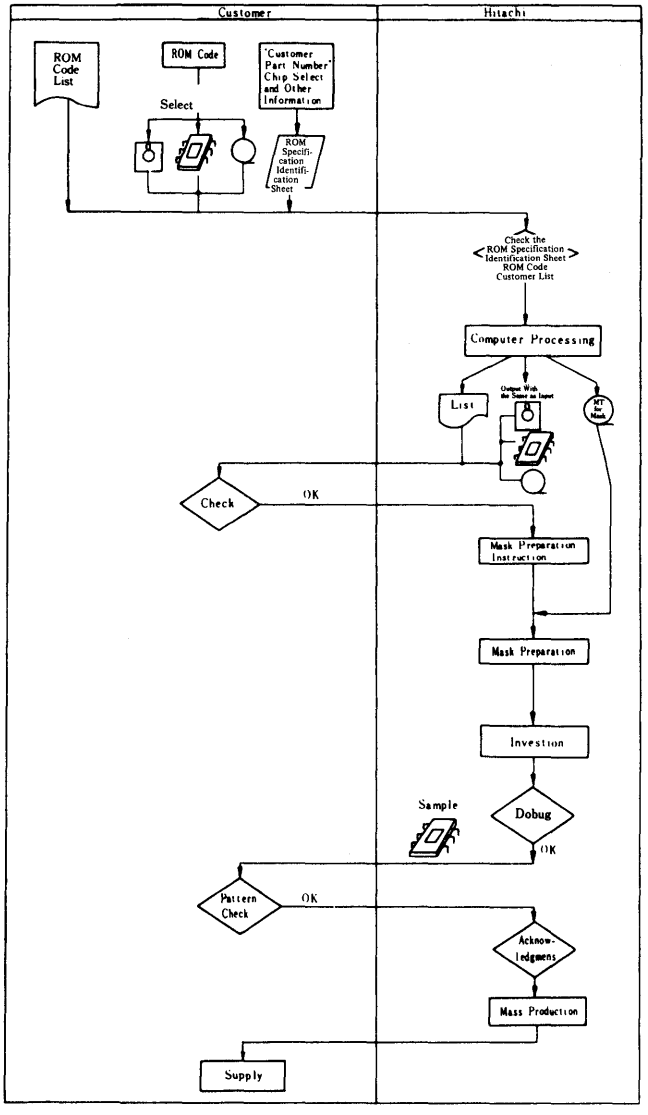


Figure 7-7. Mask ROM Development Flowchart

8. INSTRUCTIONS FOR USING MEMORY DEVICES

8.1 Prevention of Electrostatic Discharge

As semiconductor memory designs are based on a very fine pattern, they can be subject to malfunction or defects caused by static electricity. Though the built-in protection circuits assure unaffected reliability in normal use, devices should be handled according to the following instructions:

1. In transporting and storing memory devices, put them in conductive magazine or put all pins of each device into a conductive mat so that they are kept at the same potential. Manufacturers should give enough consideration to packing when shipping their products.
2. When devices touch a human body in mounting or inspection, the handler must be grounded. Do not forget to insert a resistor (1MΩ approx is desirable) in series to protect the handles from electrical shock.
3. Keep the relative ambient humidity at about 50% in process.
4. For working clothes, cotton is preferrable to synthetic fabrics.
5. Use a soldering iron operating at low voltage (12 V or 24 V, if possible) with its tip grounded.
6. In transporting the board with memory devices mounted on it, cover it with conductive sheets.
7. Use conductive sheets of high resistance (about 10^9 ohm/□) to protect devices from electrostatic discharge. For, if dropped onto conductive materials like a metal sheet, devices may deteriorate or even breakdown owing to sudden discharge of the charge stored on the surface.
8. Never set the system to which memory devices are applied near anything that generates high voltage (e.g. CRT Anode electrode, etc.).

8.2 Using CMOS Memories

As shown in figure 8-1, the input of a CMOS memory is connected to the gate of an inverter consisting of PMOS and NMOS transistors. Figure 8-2 shows the relationship between the input voltage and current in this inverter. The top and bottom transistors turn ON and make current flown when the input voltage becomes intermediate level. Therefore, it is necessary to keep the input voltage below 0.2 V or above V_{CC} − 0.2 V in order to minimize power consumption. The data sheet specifies the stand-by current for both the cases of input level with minimum V_{IH} and maximum V_{IL} and that with 0.2 V or V_{CC} − 0.2 V, and the difference in value is remarkably great. Some memory devices are designed to cut off such current flow in standby mode by the control of input signals, but it depends on device type. This should be confirmed in data sheets for each device type.

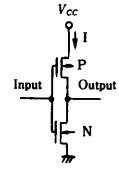


Figure 8-1. CMOS Inverter

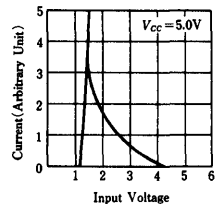


Figure 8-2. Relationship between Input Voltage & Current In CMOS Inverter

Another problem particular to CMOS devices is latch-up. Figure 8-3 shows the cross section of a CMOS inverter and the structure of a parasitic bipolar transistor. The equivalent circuit of the parasitic thyristor is shown in figure 8-4. When positive DC current or pulse noise is applied (figure 8-4 (a)), TR3 is turned on owing to the bias voltage generated between base and emitter. And trigger current flows into GND through R_P, the base resistance of TR2. As a result, TR2 becomes conductive and current flows from power supply (V_{CC}) through the base resistance of TR1 (R_N), which puts TR1 into conduction, too. Then, as the base of TR2 is rebiased by collector current from TR1, the closed loop consisting of TR1 and TR2 reacts. Thus current flows constantly between power supply (V_{CC}) and GND even without trigger current caused by outside noise.

Latch-up can be caused by a negative pulse, too (figure 8-4 (bb)). Most of semiconductor memory manufacturers are trying to improve latch-up immunity of their products. Hitachi provides enough guard band by applying diffusion layer around inputs and outputs, taking care not to connect input to p^+ diffusion layer. Input voltage for 64 kbit

static RAM HM6264A, for example, is specified as follows:

V_{IH} max 6.0 V (not depending on V_{CC})
V_{IL} min 3.0 V (pulse width = 50 ns)
−0.3 V (DC level)

Thus almost no consideration for latch-up is required in system design.

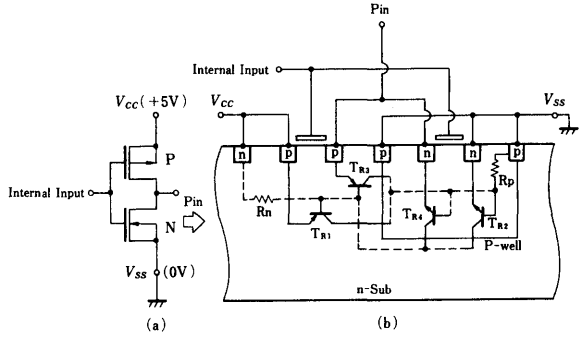


Figure 8-3. Cross Section Structure of CMOS Inverter

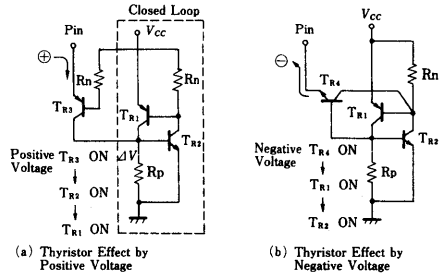


Figure 8-4. Equivalent Circuit of Parasitic Thyristor

8.3 Noise Prevention

Noise in semiconductor memories is roughly classified into input signal noise and power supply noise.

8.3.1 Input Signal Noise

Input signal noise is caused by overshoot and undershoot. If either of them is out of recommended DC operating conditions, normal operation is hindered, and voltage over absolute maximum rating will break the device. In operating high speed systems, special care is required to prevent input signal noise.

The noise can be prevented by inserting a serial resistance of less than 50 ohm into each input or a terminating resistance into the input line. Actually, however, input signal noise can be simply reduced by a stable power supply line, because it is often caused by unstable reference voltage (GND level).

8.3.2 Power Supply Noise

The power source noise can be classed as low-frequency noise and high-frequency noise as shown in figure 8-5. To assure stable memory operation, the peak-to-peak power supply voltage in the presence of low-or high-frequency noise should be held below 10 percent of its standard level.

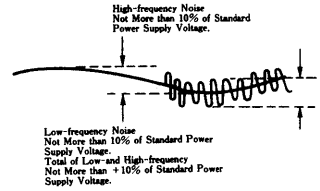


Figure 8-5. Power Source Noise

Devices like dynamic RAMs, which operate from clock signals, or high speed CMOS static RAMs, through which current flows during transition of signals, consume high peak current. When a power supply does not have enough capacity for the peak current, voltage drops. And if the recovery rate of the power supply synchronizes with its time constant, it may start oscillating. To reduce the influence of the peak current, a bypass capacitor of 0.1 – 0.01 μF should be inserted near the device. The following points must be considered in designing pattern of the board:

★ For bypass capacitors, use titanium, ceramic, or tantalum capacitors which have better high-frequency characteristics.

★ Bypass capacitors must be applied as near to the power supply pin of memory devices as possible, and inductance in the path from V_{CC} pin to V_{SS} pin through the bypass capacitor must be as little as possible.

★ The line connected to the power supply on the board should be as wide as possible.

★ It is preferrable for the power supply line to be at right angles to devices selected at the same time, lest too much peak current should flow through one power supply line at a time.

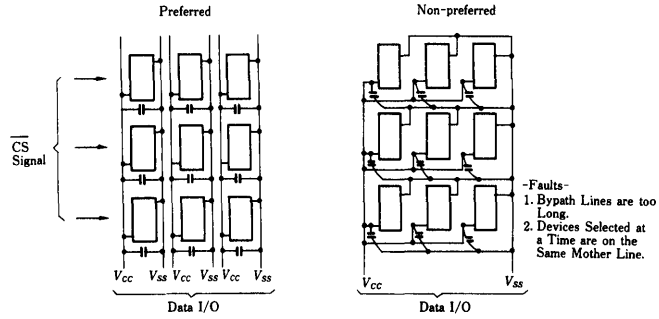


Figure 8-6. Examples of Power Supply Board Pattern

8.4 Address Input Waveform of Hi-BiCMOS Memory

Data stored in memory might be destructed in case that Address Input of the HM6716, HM6719, HM6787, HM6788 and HM6789 series becomes floating and sticks at and around threshold voltage. (e.g. CPU does Address Bus to off state in Figure 1.) Consequently, the following three methods are recommended so as to preserve malfunction of memory device.

A: Insert latch as shown in Figure 8-7 lest Address Input should become floating.

B: Put $\overline{CS}$ into High while Address Input becomes floating.
(Dotted line in Figure 8-8)

C: Insert Pull-up Resistor (R) to hold time constant of Rising Edge wave form of Address Input pin (tr = R x C) below 150 ns.

Stable operation can be assured if you have already adopted the above three method (A, B, C), while if you have any problem, please contact our sales offices.

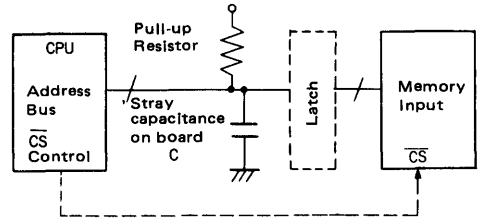


Figure 8-7

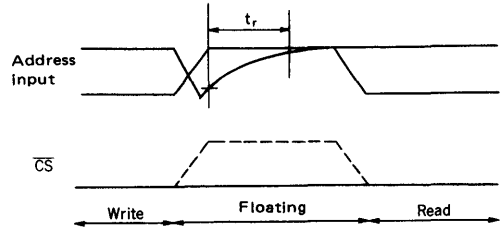


Figure 8-8

2

Section 2
MOS Static RAM

HITACHI®

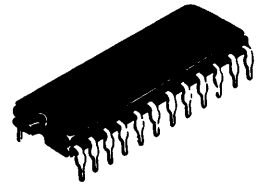
HM6116 Series — Maintenance Only

2048-word x 8-bit High Speed CMOS Static RAM

■FEATURES

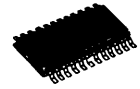
- Single 5V Supply
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation
  - Standby: 100μW (typ.)
    10μW (typ.) (L-version)
  - Operation: 200mW (typ.)
    175mW (typ.) (L-version)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back Up Operation (L-version)

HM6116P Series



(DP-24)

HM6116FP Series

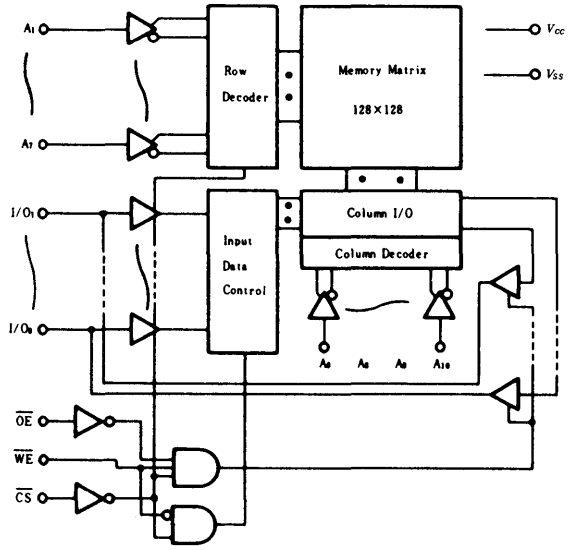


(FP-24D)

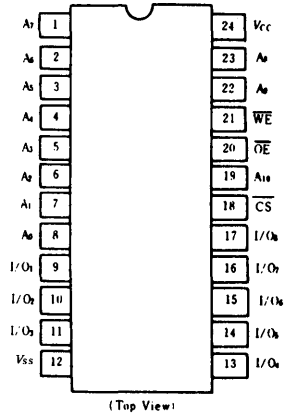
■ORDERING INFORMATION

Type No.	Access Time	Package
HM6116P-2 HM6116P-3 HM6116P-4	120ns 150ns 200ns	600mil 24pin Plastic DIP
HM6116LP-2 HM6116LP-3 HM6116LP-4	120ns 150ns 200ns	
HM6116FP-2 HM6116FP-3 HM6114FP-4	120ns 150ns 200ns	24pin Plastic SOP
HM6116LFP-2 HM6116LFP-3 HM6116LFP-4	120ns 150ns 200ns	

■FUNCTIONAL BLOCK DIAGRAM



■PIN ARRANGEMENT



(Top View)

Note) This device is not available for new application.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

Note) *1. −3.5V for pulse width≦50ns

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta=0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−0.3*1	—	0.8	V

Note) *1. −3.0V for pulse width≦50ns.

■DC AND OPERATING CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, Ta=0 to +70°C)

Item	Symbol	Test Conditions	HM6116-2			HM6116-3/-4			Unit
			min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}= V_{SS} to V_{CC}	—	—	10	—	—	10	μA
			—	—	2*3	—	—	2*3	
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$= V_{IH} or $\overline{OE}$= V_{IH}, $V_{I/O}$= V_{SS} to V_{CC}	—	—	10	—	—	10	μA
			—	—	2*3	—	—	2*3	
Operating Power Supply Current	I_{CC}	$\overline{CS}$= V_{IL}, $I_{I/O}$=0mA	—	40	80	—	35	70	mA
			—	35*3	70*3	—	30*3	60*3	
	I_{CC1}*2	V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	35	—	—	30	—	mA
			—	30*3	—	—	25*3	—	
Average Operating Current	I_{CC2}	Min. cycle, duty=100% $I_{I/O}$=0mA	—	40	80	—	35	70	mA
			—	35*3	70*3	—	30*3	60*3	
Standby Power Supply Current	I_{SB}	$\overline{CS}$= V_{IH}	—	5	15	—	5	15	mA
			—	4*3	12*3	—	4*3	12*3	
	I_{SB1}	$\overline{CS}$≧ V_{CC}−0.2V, 0V≦ V_{IN}≦ 0.2V or V_{CC}−0.2V≦ V_{IN}	—	0.02	2	—	0.02	2	μA
			—	2*3	50*3	—	2*3	50*3	
Output Voltage	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

Notes) *1. V_{CC}=5V, Ta=25°C
*2. Reference Only
*3. This characteristics are guaranteed only for L-version.

■CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L (100pF) (including scope and jig)

●READ CYCLE

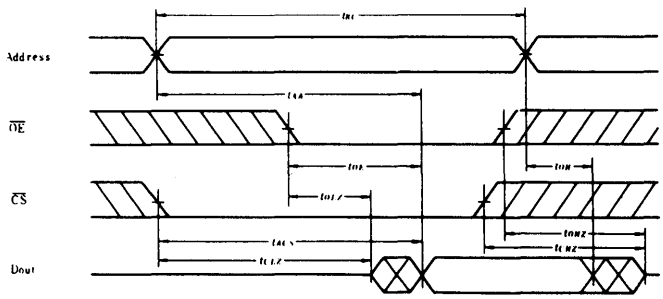
Item	Symbol	HM6116-2		HM6116-3		HM6116-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

●WRITE CYCLE

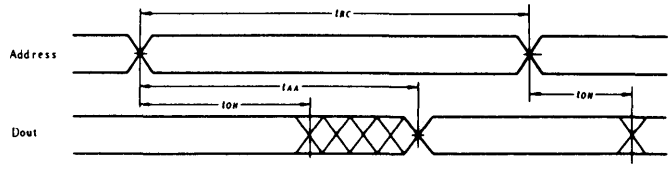
Item	Symbol	HM6116-2		HM6116-3		HM6116-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

■TIMING WAVEFORM

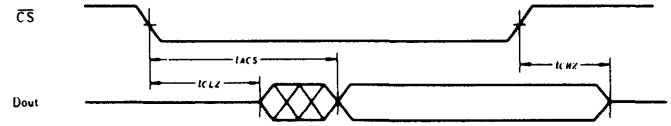
●READ CYCLE (1)[1]



● READ CYCLE (2)[1][2][4]

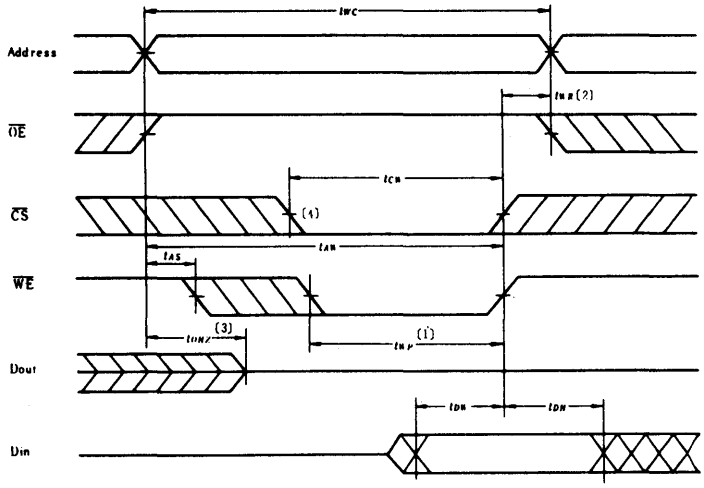


● READ CYCLE (3)[1][3][4]

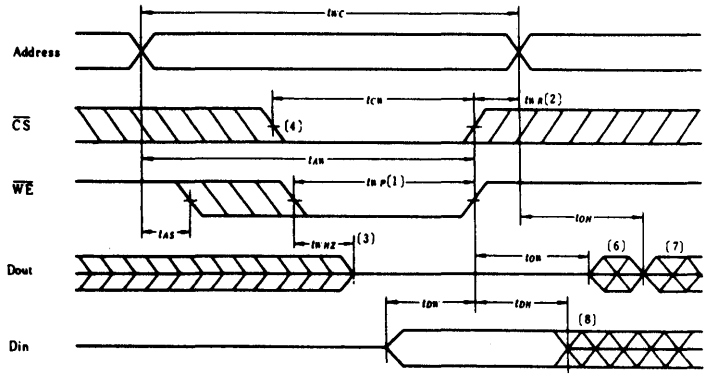


NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

● WRITE CYCLE (1)



● WRITE CYCLE (2)[5]



NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

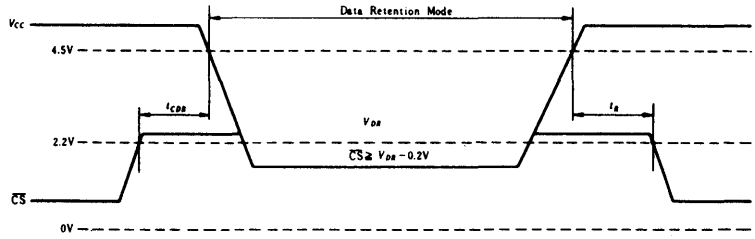
■ LOW Vcc DATA RETENTION CHARACTERISTICS ($Ta = 0$ to $+70°C$)

This characteristics are guaranteed only for L-version.

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$, $V_{in} \geq V_{CC} - 0.2V$ or $V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR} *1	$V_{CC} = 3.0V$, $\overline{CS} \geq 2.8V$, $V_{IH} \geq 2.8V$ or $0V \leq V_{IN} \leq 0.2V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *2	—	—	ns

Notes) *1. 10μA max at $Ta = 0°C$ to $+40°C$, V_{IL} min $= -0.3V$
*2. t_{RC} = Read Cycle Time.

● Low Vcc Data Retention Waveform



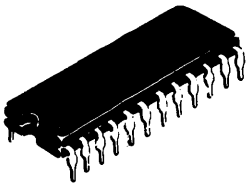
HM6116A Series——Maintenance Only

2048-word×8-bit High Speed Static CMOS RAM

■ FURTURES

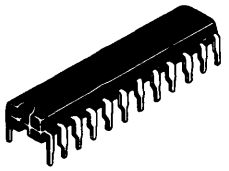
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Low Power Operation
  - Standby: 100μW (typ.)
    5μW (typ.) (L-version)
  - Operation: 15mW (typ.) (f = 1 MHz)
    10 mW (typ.) (L-version)
- Single 5V Supply and High Density 24 Pin Package
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back Up Operation (L-version)

HM6116AP Series



(DP-24)

HM6116ASP Series

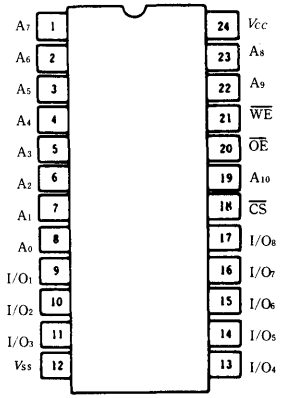


(DP-24N)

■ORDERING INFORMATION

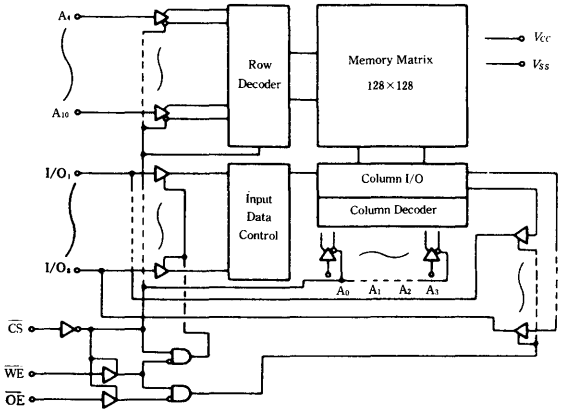
Type No.	Access Time	Package
HM6116AP-12 HM6116AP-15 HM6116AP-20	120ns 150ns 200ns	600mil 24pin Plastic DIP
HM6116ALP-12 HM6116ALP-15 HM6116ALP-20	120ns 150ns 200ns	
HM6116ASP-12 HM6116ASP-15 HM6116ASP-20	120ns 150ns 200ns	300mil 24pin Plastic DIP
HM6116ALSP-12 HM6116ALSP-15 HM6116ALSP-20	120ns 150ns 200ns	

■PIN ARRANGEMENT



(Top View)

■FUNCTIONAL BLOCK DIAGRAM



Note) This device is not available for new application.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C
Power Dissipation	P_T	1.0	W

Note) *1. −3.5V for pulse width≦50ns.

■TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

■RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−0.3*1	—	0.8	V

Note) *1. −3.0V for pulse width≦50ns.

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	HM6116A-12			HM6116A-15			HM6116A-20			Unit
			min	typ*1	max	min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{in}=V_{SS} to V_{CC}	—	—	2	—	—	2	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=V_{SS} to V_{CC}	—	—	2	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	—	5	15	—	5	15	—	5	15	mA
		V_{in}=V_{IH} or V_{IL}	—	4*2	12*2	—	4*2	12*2	—	4*2	12*2	
	I_{CC1}	V_{IH}=V_{CC}, V_{IL}=0V, $\overline{CS}$=V_{IL},	—	3	6	—	3	6	—	3	6	mA
		$I_{I/O}$=0mA, f=1MHz	—	2*2	5*2	—	2*2	5*2	—	2*2	5*2	
Average Operating Current	I_{CC2}	min. cycle, $I_{I/O}$=0mA	—	35	60	—	25	45	—	20	35	mA
		duty = 100%	—	30*2	50*2	—	20*2	40*2	—	15*2	30*2	
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	—	1	4	—	1	4	—	1	4	mA
			—	0.5*2	3*2	—	0.5*2	3*2	—	0.5*2	3*2	
	I_{SB1}	$\overline{CS}$ ≧ V_{CC} − 0.2V	—	0.02	2	—	0.02	2	—	0.02	2	mA
		0V ≦ Vin	—	1*2	50*2	—	1*2	50*2	—	1*2	50*2	μA
Output Voltage	V_{OL}	I_{OL} = 4mA	—	—	0.4	—	—	0.4	—	—	0.4	V
	V_{OH}	I_{OH} = −1.0mA	2.4	—	—	2.4	—	—	2.4	—	—	V

Notes) *1. V_{CC}=5V, T_a=25°C
*2. This characteristics is guaranteed only for L-version.

■CAPACITANCE (f=1MHz, Ta=25°C)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	V_{in}=0V	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

Note) This parameter is sampled and not 100% tested.

■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70°C)

●AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V
Input Rise and Fall Times: 10 ns
Input and Output Timing Reference Levels: 1.5V
Output Load: 1TTL Gate and C_L = 100pF (including scope and jig)

● READ CYCLE

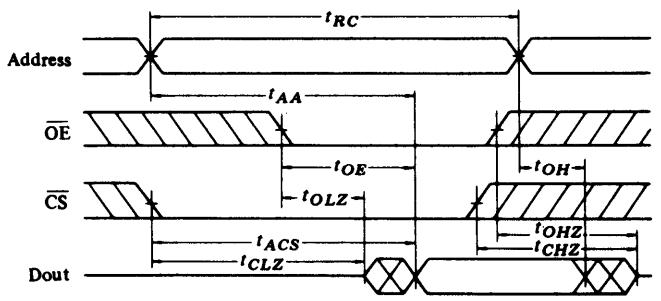
Item	Symbol	HM6116A-12		HM6116A-15		HM6116A-20		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	–	150	–	200	–	ns
Address Access Time	t_{AA}	–	120	–	150	–	200	ns
Chip Select Access Time	t_{ACS}	–	120	–	150	–	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	ns
Output Enable to Output Valid	t_{OE}	–	55	–	60	–	70	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	10	–	10	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	–	15	–	20	–	ns

● WRITE CYCLE

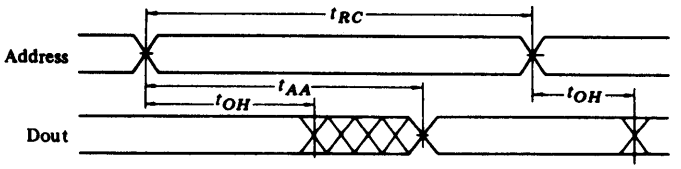
Item	Symbol	HM6116A-12		HM6116A-15		HM6116A-20		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	–	150	–	200	–	ns
Chip Selection to End of Write	t_{CW}	70	–	90	–	120	–	ns
Address Valid to End of Write	t_{AW}	105	–	120	–	140	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	70	–	80	–	100	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	35	–	40	–	50	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	10	–	10	–	10	–	ns

■TIMING WAVEFORM

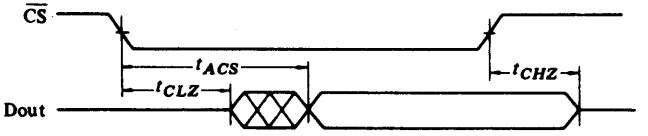
●READ CYCLE (1)[1]



● READ CYCLE (2)[1][2][4]

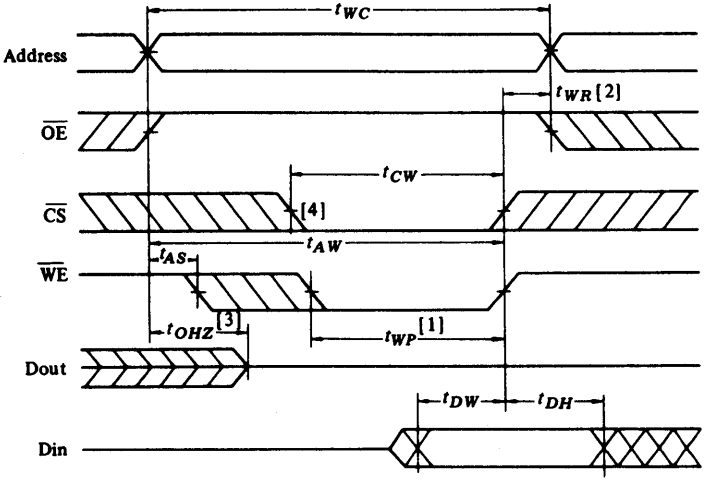


● READ CYCLE (3)[1][3][4]

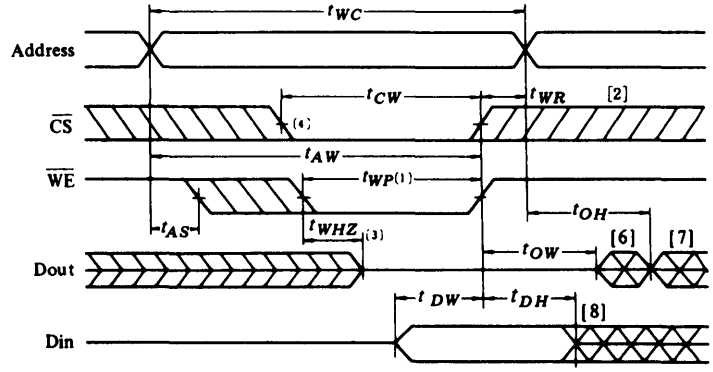


NOTES: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE} = V_{IL}$.

● WRITE CYCLE(1)



● **WRITE CYCLE (2)**[5]



NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

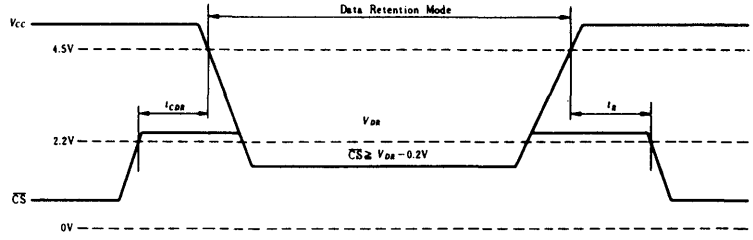
■ LOW Vcc DATA RETENTION CHARACTERISTICS ($Ta = 0$ to $+70°C$)

This characteristics is guaranteed only for L-version.

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}*1	$V_{CC} = 3.0V$, $\overline{CS} \geq 2.8V$, $0V \leqq V_{IN}$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}*2	—	—	ns

Notes) * 1. 10μA max at $Ta = 0°C$ to $+40°C$, V_{IL} min $= -0.3V$
* 2. t_{RC} = Read Cycle Time.

● **Low Vcc Data Retention Waveform**

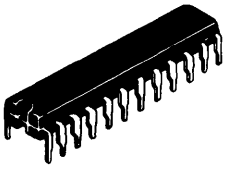


HM6716 Series
HM6719 Series

Maintenance Only

2048-word × 8-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)
2048-word × 9-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)

- **Features**
- Fast Access Time: 25/30ns (max)
- Low Power Dissipation (DC): 280mW (typ.)
- +5V Single Supply
- Completely Static Memory No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

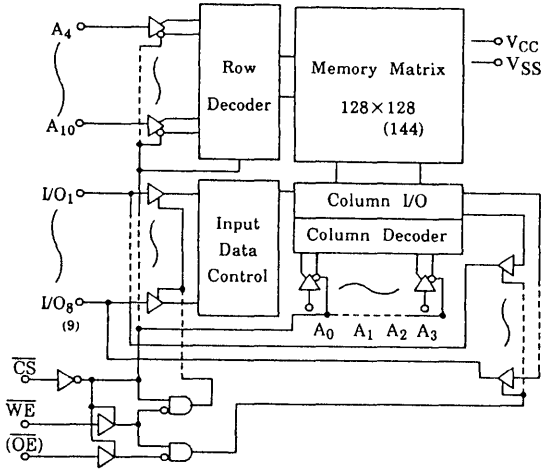


(DP-24NC)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6716P-25	25ns	300 mil 24 Pin Plastic DIP
HM6716P-30	30ns	
HM6719P-25	25ns	
HM6719P-30	30ns	

■ Block Diagram

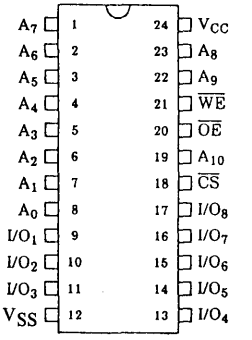


■ Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

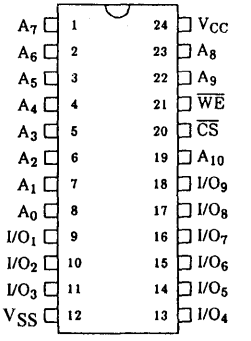
■ PIN ARRANGEMENT

- **HM6716**



(Top View)

- **HM6719**



(Top View)

■ Truth Table

● HM6716

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (2)
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–

● HM6719

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (2) (3)
L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (2)

■ Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}*)	−3.0	–	0.8	V

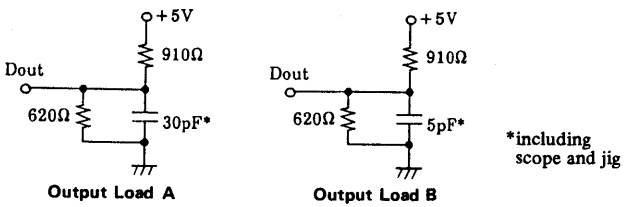
*) Pulse Width: 20ns, DC: −0.5V

■ DC and Operating Characteristics (V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}= V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, $V_{I/O}$= V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	–	120	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100% $I_{I/O}$=0mA	–	–	130	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}	–	–	30	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$ $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	–	–	10	mA
Output Low Voltage	V_{OL}	I_{OL}=4mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH}=−1mA	2.4	–	–	V

■ AC Test Conditions

Input pulse levels: V_{SS} to 3.0V
Input and Output reference levels: 1.5V
Input rise and fall time: 4ns
Output Load: See Figure



(t_{CHZ}, t_{WHZ}, t_{CLZ}, t_{OW}, t_{OLZ}, t_{OHZ})

■ **Capacitance** (T_a = 25°C, f = 1.0 MHz)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	–	–	6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	–	8	pF

Note) This parameter is sampled and not 100%, tested.

■ **AC Characteristics** (V_{CC} 5V ± 10%, T_a = 0 to +70°C, unless otherwise noted.)

● **Read Cycle**

Item	Symbol	HM6716-25 HM6719-25		HM6716-30 HM6719-30		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	25	–	30	–	ns	–
Address Access Time	t_{AA}	–	25	–	30	ns	–
Chip Select Access Time	t_{ACS}	–	25	–	30	ns	–
Chip Selection to Output in Low Z	t_{CLZ}	0	–	0	–	ns	*2
Output Enable to Output Valid	t_{OE}	0	20	0	20	ns	*1
Output Enable to Output in Low Z	t_{OLZ}	0	–	0	–	ns	*1, *2
Chip Deselection to Output in High Z	t_{CHZ}	0	10	0	12	ns	*2
Chip Disable to Output in High Z	t_{OHZ}	0	10	0	10	ns	*1, *2
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	–
Input Voltage Rise/Fall Time	t_T	–	150	–	150	ns	*3

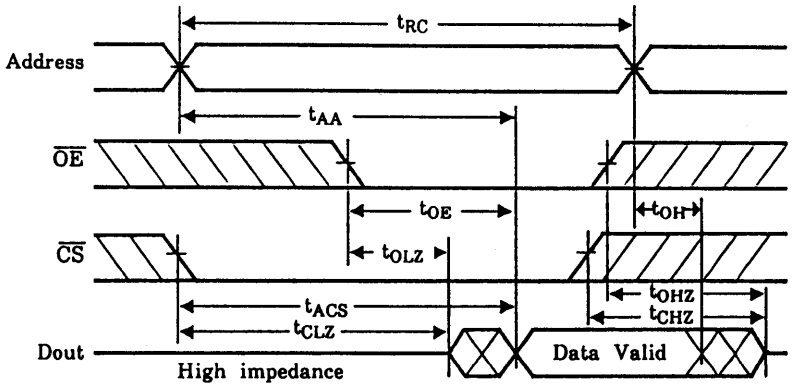
● **Write Cycle**

Item	Symbol	HM6716-25 HM6719-25		HM6716-30 HM6719-30		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	25	–	30	–	ns	–
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns	–
Address Setup Time	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AW}	20	–	25	–	ns	–
Write Pulse Width	t_{WP}	20	–	25	–	ns	–
Write Recovery Time	t_{WR}	0	–	0	–	ns	–
Output Disable to Output in High Z	t_{OHZ}	0	10	0	10	ns	*1, *2
Write to Output in High Z	t_{WHZ}	0	10	0	12	ns	*2
Data Valid to End of Write	t_{DW}	15	–	15	–	ns	–
Data Hold Time	t_{DH}	5	–	5	–	ns	–
Output Active from End of Write	t_{OW}	0	–	0	–	ns	*2

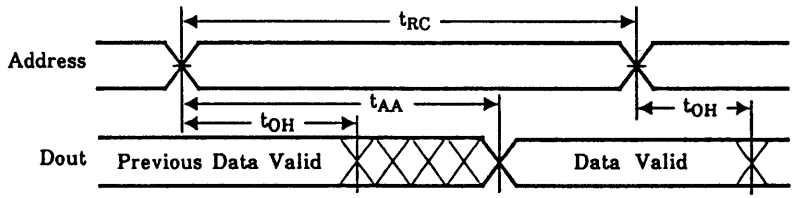
Notes) *1. These parameters are for HM6716.
*2. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
*3. If t_T becomes more than 150ns, there is possibility of function fail. Please contact your nearest Hitachi's Sale Dept. regarding specification.

■ Timing Waveforms

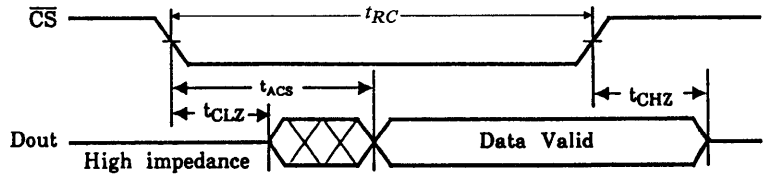
● Read Cycle (1)*1



● Read Cycle (2)*1,*2,*4

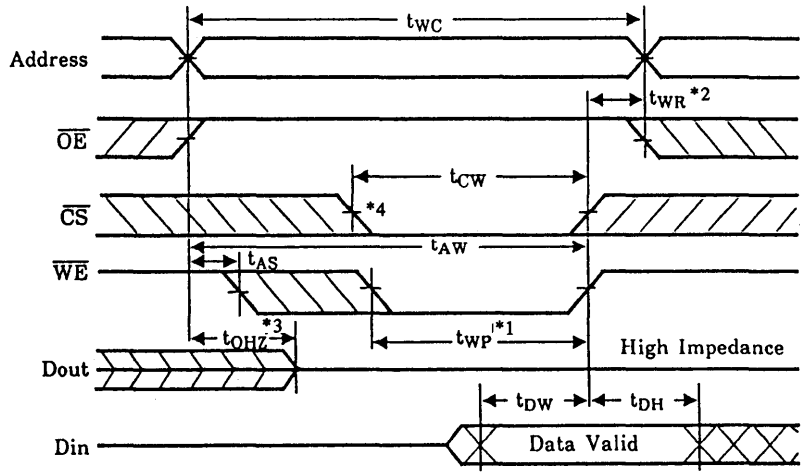


● Read Cycle (3)*1,*3,*4

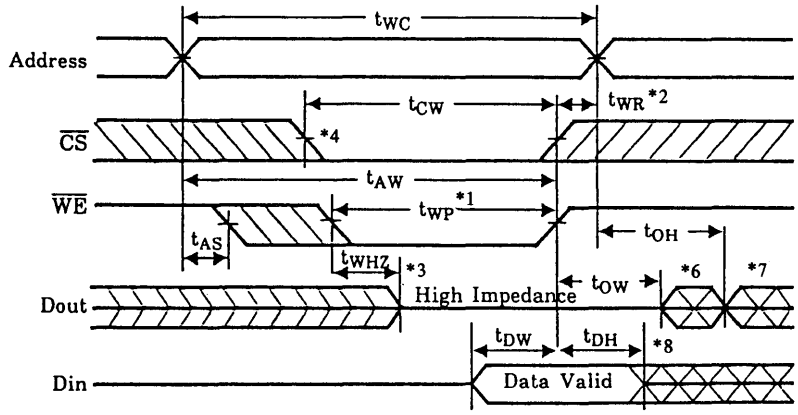


Notes) *1. $\overline{WE}$ is High for Read Cycle.
*2. Device is continuously selected, $\overline{CS}=V_{IL}$.
*3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
*4. $\overline{OE}=V_{IL}$.

- **Write Cycle (1)**



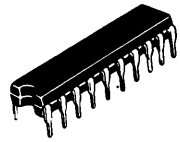
- **Write Cycle (2)**[*5]



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
*5. $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL}).
*6. Dout is the same phase of write data of this write cycle.
*7. Dout is the read data of next address.
*8. If $\overline{CS}$ is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

HM6268 Series

4096-word x 4-bit High Speed CMOS Static RAM



(DP-20N)

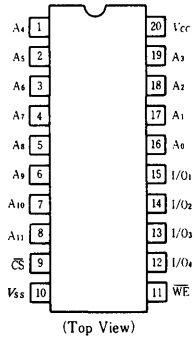
■FEATURES

- Single 5V Supply and High Density 20 Pin Package.
- High Speed: Fast Access Time 25/35/45ns (max.)
- Low Power Standby: 100μW typ, 5μW typ (L-version)
  Active: 250mW typ.
- Completely Static Memory: No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible – All Inputs and Outputs
- Capability of Battery Back Up Operation (L-version)

■ORDERING INFORMATION

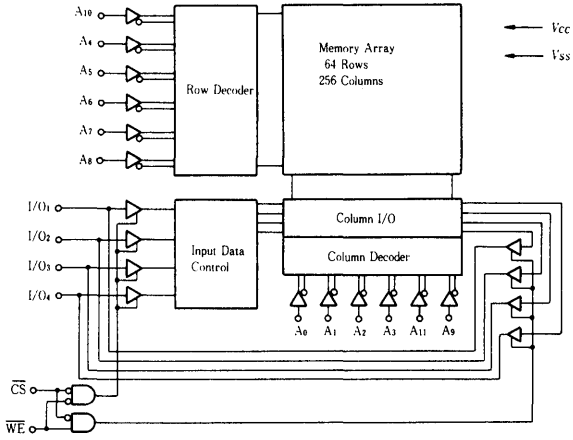
Type No.	Access Time	Package
HM6268P-25 HM6268P-35 HM6268P-45	25ns 35ns 45ns	300mil 20pin Plastic DIP
HM6268LP-25 HM6268LP-35 HM6268LP-45	25ns 35ns 45ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width≤10ns.

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	Din	Write Cycle

■RECOMMENDED OPERATING CONDITIONS (Ta=0 to +70℃)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width≦10ns.

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C

Parameter	Symbol	Test Condition	Min.	Typ.*1	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	—	—	2.0	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	—	—	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA, min. cycle	—	50*3	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, min. cycle	—	15	25	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}$ ≥ V_{CC} −0.2V,	—	0.02	2.0	mA
		0V ≤ V_{IN} ≤ 0.2V or V_{CC} − 0.2V ≤ V_{IN}	—	1*2	50*2	μA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −0.4mA	2.4	—	—	V

Notes) *1. Typical limits are at V_{CC}=5.0V, Ta= +25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. 40mA typ. for 45ns version.

■CAPACITANCE (Ta=25°C, f=1.0MHz)

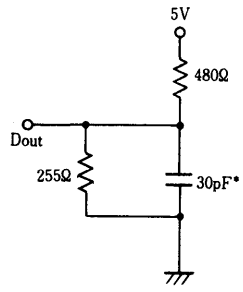
Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	9	pF

Note: This parameter is sampled and not 100% tested.

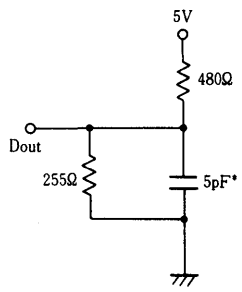
■AC CHARACTERISTICS (V_{CC}=5V±10%, Ta=0 to +70℃, unless otherwise noted.)

- **AC Test Conditions**
  Input pulse levels: V_{SS} to 3.0V
  Input rise and fall times: 5ns
  Input and Output timing reference levels: 1.5V
  Output load: See Figure

Output Load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



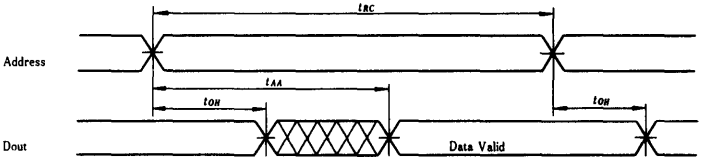
*Including scope and jig.

● READ CYCLE

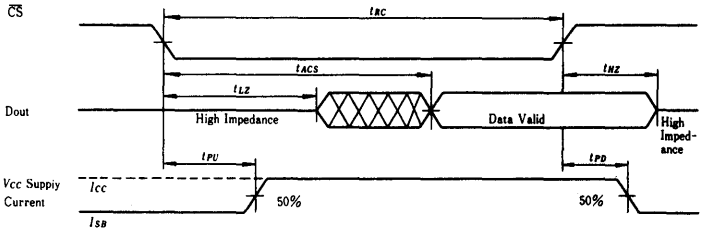
Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	—	45	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}*1	10	—	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}*1	0	15	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	25	—	25	—	30	ns

Note) * 1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No. 1 (1),(2)



● Timing Waveform of Read Cycle No. 2 (1),(3)



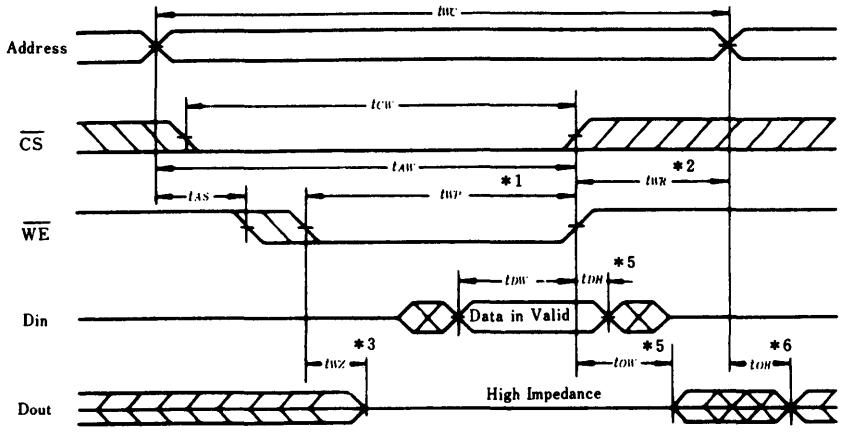
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

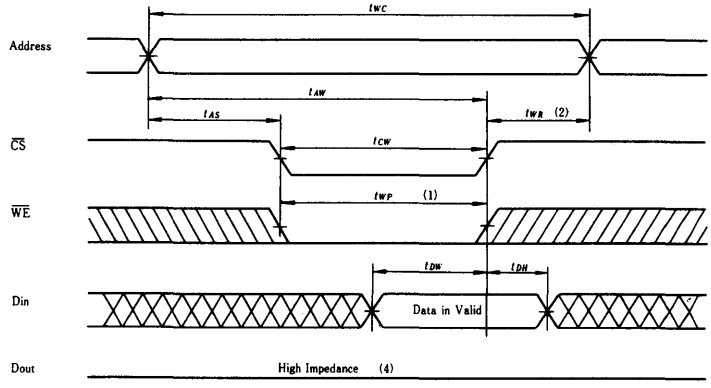
Parameter	Symbol	HM6268-25		HM6268-35		HM6268-45		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	35	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	12	—	20	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High Z	t_{WZ}*1	0	8	0	10	0	15	ns
Output Active from End of Write	t_{OW}*1	0	—	0	—	0	—	ns

Note) * 1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

- Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



- Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes:
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

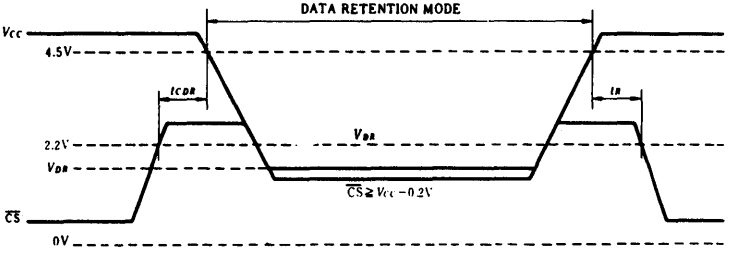
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leq Ta \leq 70°C$)

This characteristics guaranteed only for L-version.

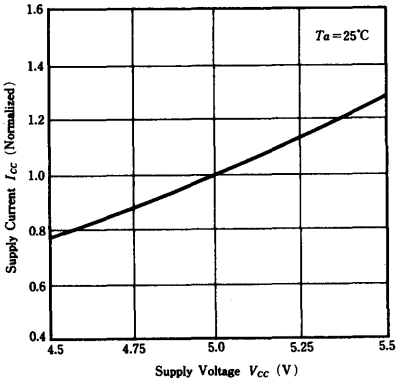
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$ $V_{in} \geq V_{CC}-0.2V$ or $0V \leq V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30 *2 20 *3	μA
Chip Deselect to Data Retention Time	t_{CDR}	See retention waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

Notes) *1. t_{RC} = Read Cycle Time. *2. V_{CC} = 3.0V *3. V_{CC} = 2.0V

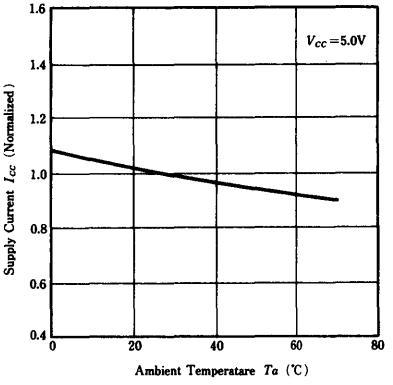
●LOW V_{CC} DATA RETENTION WAVEFORM



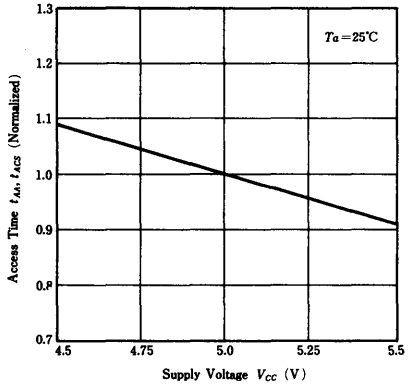
SUPPLY CURRENT VS. SUPPLY VOLTAGE



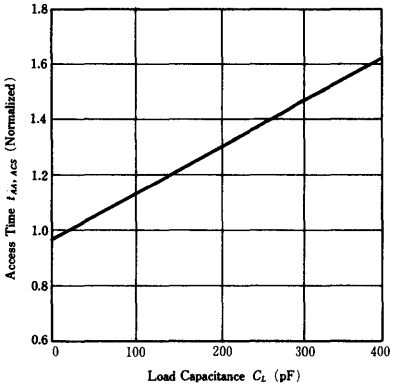
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



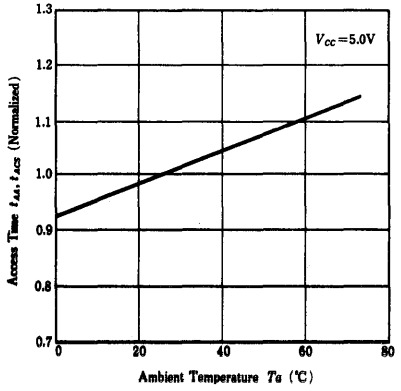
ACCESS TIME VS. SUPPLY VOLTAGE



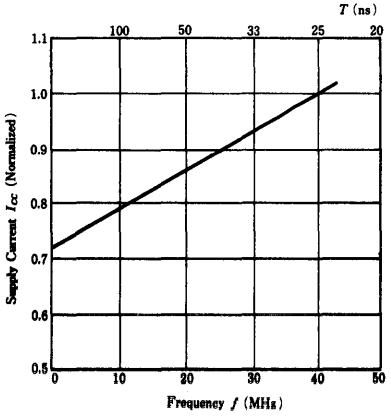
ACCESS TIME VS. LOAD CAPACITANCE



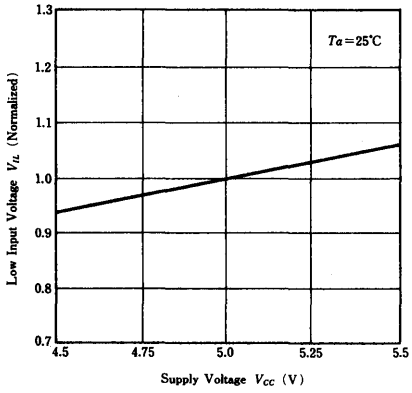
ACCESS TIME VS. AMBIENT TEMPERATURE



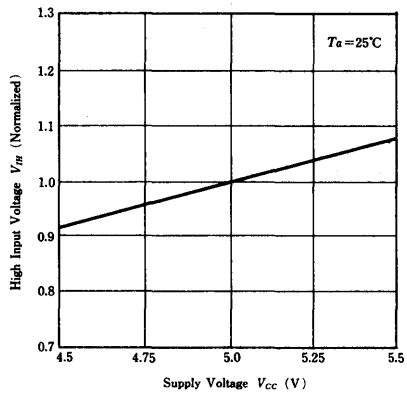
SUPPLY CURRENT VS. FREQUENCY



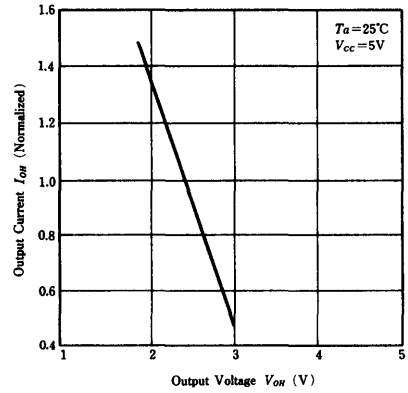
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



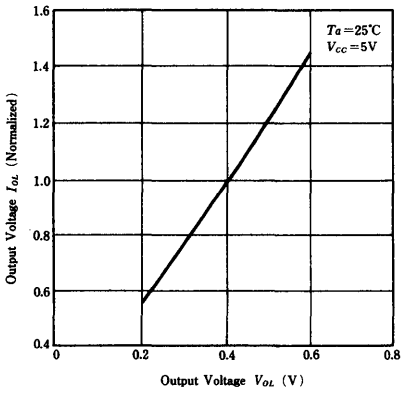
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



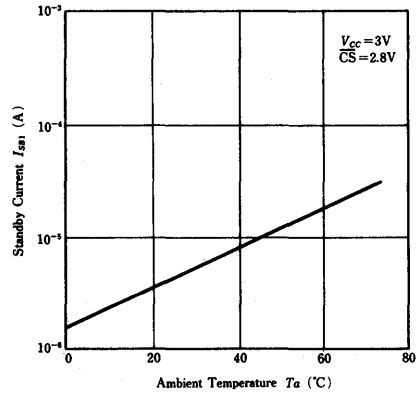
OUTPUT CURRENT VS. OUTPUT VOLTAGE



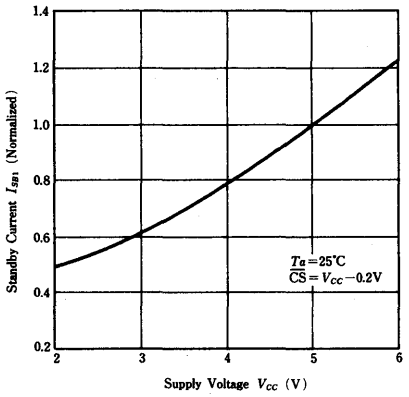
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE

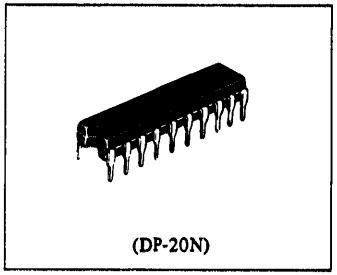


HM6267 Series

16384-word x 1-bit High Speed CMOS Static RAM

■ FEATURES

- High Speed: Fast Access Time 35/45/55ns (max.)
- Low Power Standby and Low Power Operation
  Standby: 0.1mW (typ.)/5μW (typ.) (L-version),
  Operation: 200mW (typ.)
- Single 5V Supply and High Density 20 Pin Package
- Completely Static Memory ..... No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-version)

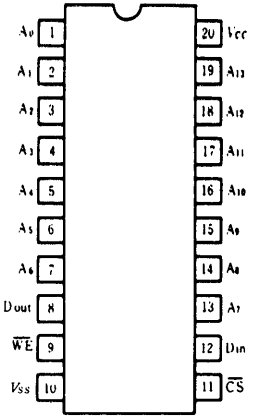


(DP-20N)

■ ORDERING INFORMATION

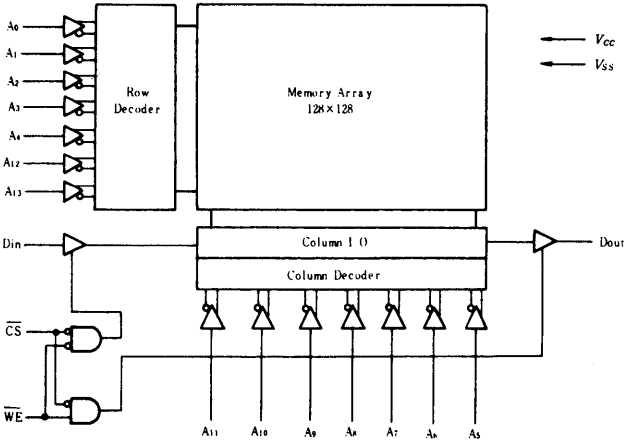
Type No.	Access Time	Package
HM6267P-35	35ns	300 mil 20 pin Plactic DIP
HM6267P-45	45ns	
HM6267P-55	55ns	
HM6267LP-35	35ns	
HM6267LP-45	45ns	
HM6267LP-55	55ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*1	V_T	-0.5*2 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

Notes) *1. With respect ot V_{SS}.
*2. -3.5V for pulse width ≦ 20ns.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-0.5*1	–	0.8	V

Note) *1. -3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	HM6267-35			HM6267-45/55			Unit
			min	typ*1	max	min	typ*1	max	
Input Leakage Current	$\|I_{LI}\|$	V_{CC}=5.5V, V_{IN}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$=V_{IH}, V_{OUT}=V_{SS} to V_{CC}	–	–	10	–	–	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, I_{OUT}=0mA, min. cycle	–	40	100	–	40	80	mA
Stand by Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, min cycle	–	10	20	–	10	20	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC} – 0.2V, 0V ≦ V_{IN} ≦ 0.2V or V_{CC} – 0.2V ≦ V_{IN}	–	0.02	2	–	0.02	2	mA
			–	1*2	50*2	–	1*2	50*2	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = -4mA	2.4	–	–	2.4	–	–	V

Notes) *1. Typical limts are at V_{CC} = 5V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	—	5	pF	V_{IN}=0V
Output Capacitance	C_{OUT}	—	7	pF	V_{OUT}=0V

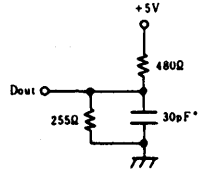
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

● AC TEST CONDITIONS

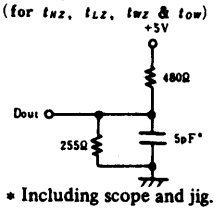
Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure

Output Load A



* Including scope and jig.

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

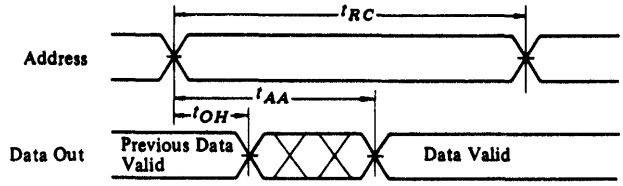


* Including scope and jig.

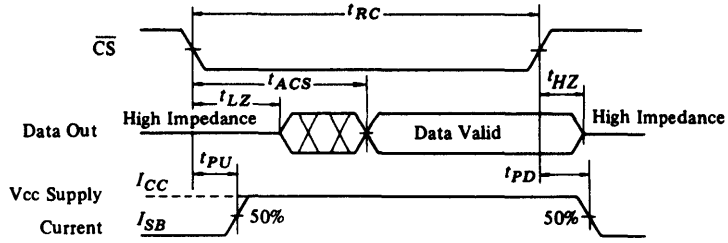
• Read Cycle

Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	35	-	45	–	55	–	ns	1
Address Access Time	t_{AA}	–	35	–	45	-	55	ns	
Chip Select Access Time	t_{ACS}	–	35	–	45	–	55	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	5	–	ns	2,3,7
Chip Deselectio to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2,3,7
Chip Selectio to Power Up Time	t_{PU}	0	–	0	–	0	–	ns	
Chip Deselection to Power Down Time	t_{PD}	–	20	–	30	–	30	ns	

• TIMING WAVEFORM OF READ CYCLE NO. 1 [4) 5)]



• TIMING WAVEFORM OF READ CYCLE NO. 2 [4) 6)]

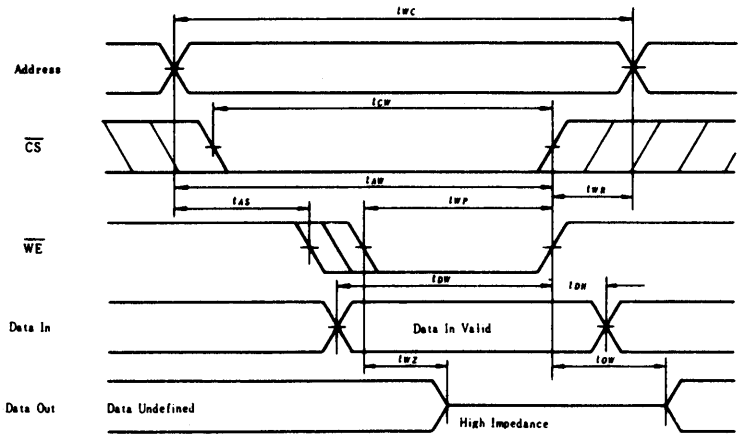


Notes) 1. All Read Cylce timing are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is High for READ cycle.
5. Device is continuously selected, $\overline{CS}$ = V_{IL}.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

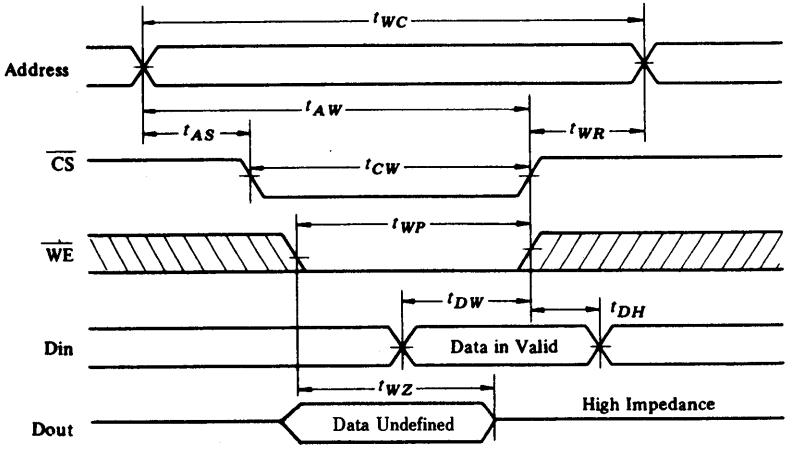
• Write Cycle

Item	Symbol	HM6267-35		HM6267-45		HM6267-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	35	–	45	–	55	–	ns	2
Chip Selection to End of Write	t_{CW}	30	–	40	–	50	–	ns	
Address Valid to End of Write	t_{AW}	30	–	40	–	50	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	35	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	0	25	ns	3,4
Output Active from End of Write	t_{OW}	0	–	0	–	0	–	ns	3,4

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ Controlled)



Notes) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

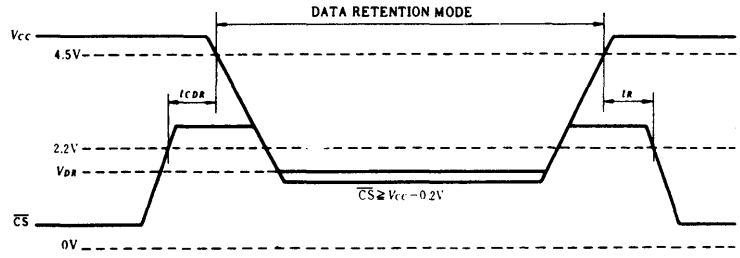
■LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0°C \leqq Ta \leqq 70°C$)

This characteristics is guaranteed only for L-version.

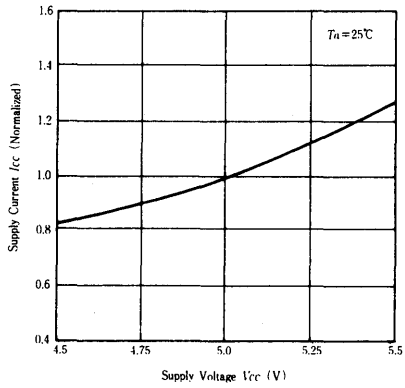
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC}-0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}	$V_{in} \geqq V_{CC}-0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	—	—	30*2 20*3	μA
Chip Deselect to Data Retention Time	t_{CDR}	see retention waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC} *1	—	—	ns

Notes) *1. t_{RC} = Read Cycle Time. *2. V_{CC} = 3.0V *3. V_{CC} = 2.0V

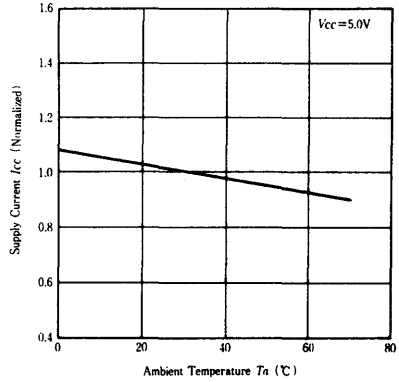
●LOW V_{CC} DATA RETENTION WAVEFORM



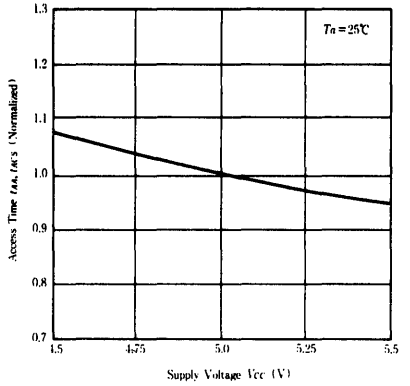
SUPPLY CURRENT VS. SUPPLY VOLTAGE



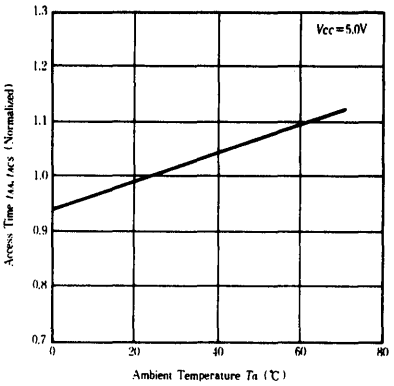
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



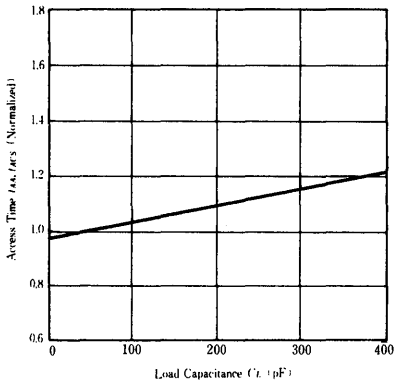
ACCESS TIME VS. SUPPLY VOLTAGE



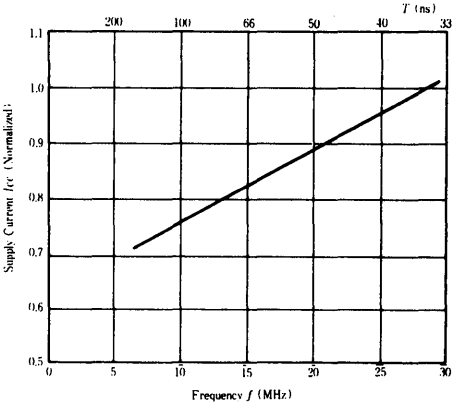
ACCESS TIME VS. AMBIENT TEMPERATURE



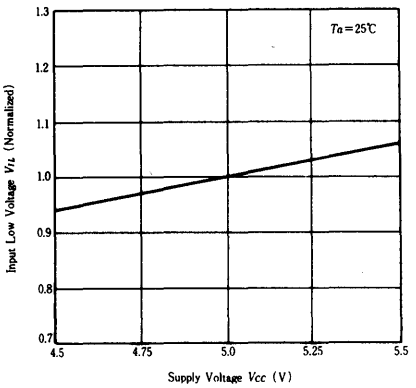
ACCESS TIME VS. LOAD CAPACITANCE



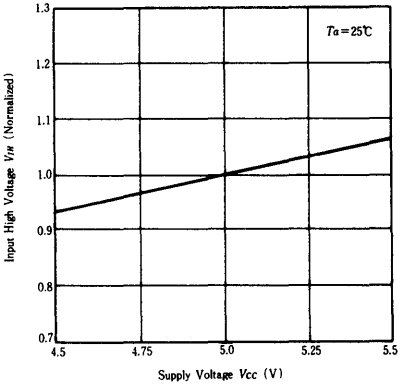
SUPPLY CURRENT VS. FREQUENCY



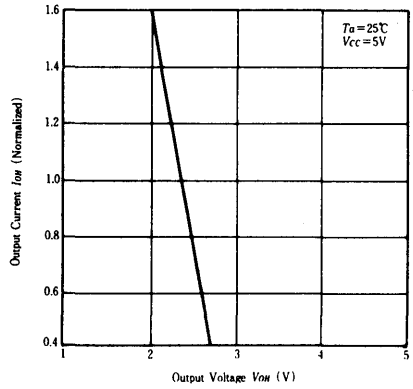
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



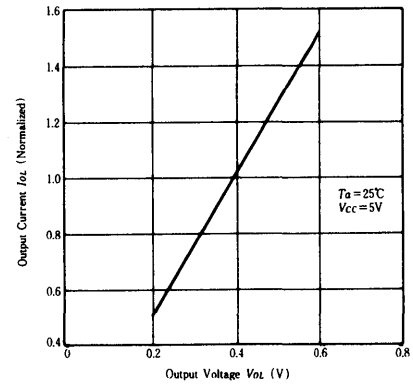
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



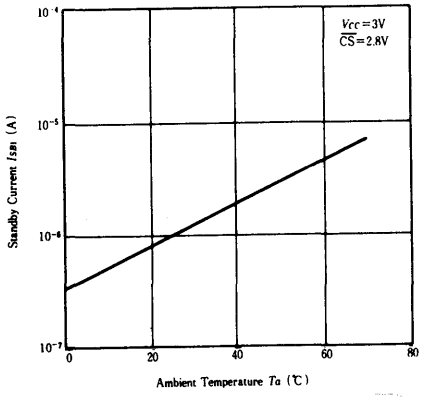
OUTPUT CURRENT VS. OUTPUT VOLTAGE



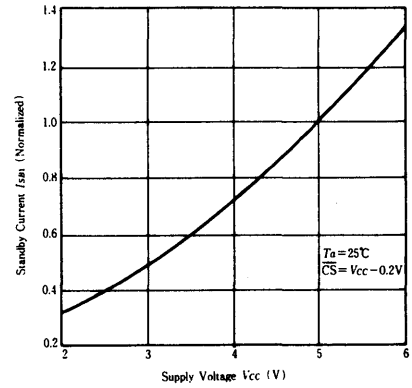
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



HM6264A Series — Maintenance Only

8192-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

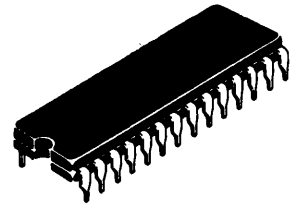
- Low Power Standby — Standby: 0.1mW (typ.) 10μW (typ.) L-/LL-version
  Low Power Operation — Operating: 15mW/MHz (typ.)
- Fast access Time — 100ns/120ns/150ns (max.)
- Single +5V Supply
- Completely Static Memory. . . . . No clock or Timing Strobe Required
- . Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-/LL-version)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6264AP-10	100ns	600 mil 28 pin Plastic DIP
HM6264AP-12	120ns	
HM6264AP-15	150ns	
HM6264ALP-10	100ns	
HM6264ALP-12	120ns	
HM6264ALP-15	150ns	
HM6264ALP-10L	100ns	
HM6264ALP-12L	120ns	
HM6264ALP-15L	150ns	
HM6264ASP-10	100ns	300 mil 28 pin Plastic DIP
HM6264ASP-12	120ns	
HM6264ASP-15	150ns	
HM6264ALSP-10	100ns	
HM6264ALSP-12	120ns	
HM6264ALSP-15	150ns	
HM6264ALSP-10L	100ns	
HM6264ALSP-12L	120ns	
HM6264ALSP-15L	150ns	
HM6264AFP-10	100ns	28 pin Plastic SOP (Note)
HM6264AFP-12	120ns	
HM6264AFP-15	150ns	
HM6264ALFP-10	100ns	
HM6264ALFP-12	120ns	
HM6264ALFP-15	150ns	
HM6264ALFP-10L	100ns	
HM6264ALFP-12L	120ns	
HM6264ALFP-15L	150ns	

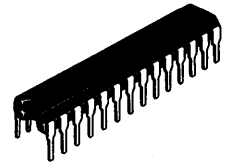
Note) T is added to the end of the type no. for a SOP of 3.00 mm (max.) thickness.

HA6264AP Series



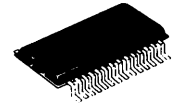
(DP-28)

HM6264ASP Series



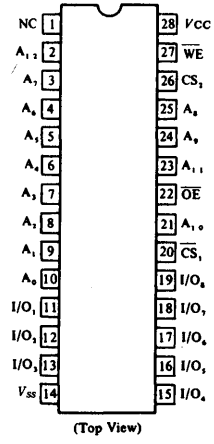
(DP-28N)

HM6264AFP Series



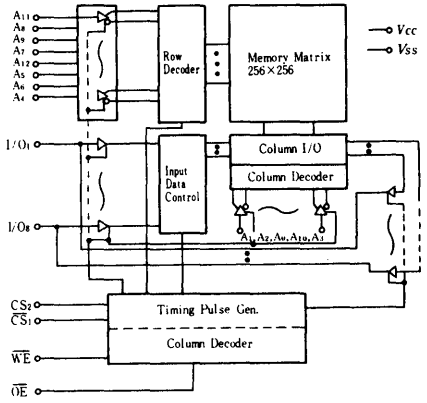
(FP-28D/DA)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage*1	V_T	−0.5*2 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	−10 to +85	°C

Notes) *1. With respect to V_{SS}.
*2. −3.0V for pulse width ≦ 50ns

■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB},I_{SB1}	
X	X	L	X		High Z	I_{SB},I_{SB1}	
H	L	H	H	Output Disabled	High Z	I_{CC}	
H	L	H	L	Read	Dout	I_{CC}	Read Cycle
L	L	H	H	Write	Din	I_{CC}	Write Cycle (1)
L	L	H	L		Din	I_{CC}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	--	6.0	V
	V_{IL}	−0.3*1	--	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{in}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS1}=V_{IH}$ or CS2=V_{IL} or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CCDC}	$\overline{CS1}=V_{IL}$, CS2=V_{IH}, $I_{I/O}$=0mA	–	7	15	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $\overline{CS1}=V_{IL}$, CS2=V_{IH} $I_{I/O}$=0mA	–	30	45*5	mA
				30	55*6	
	I_{CC2}	Cycle time = 1μs, duty = 100%, $I_{I/O}$ = 0mA, $\overline{CS1} \leqq 0.2V$, CS2 $\geqq V_{CC}-0.2V$ $V_{IH} \geqq V_{CC}-0.2V$, $V_{IL} \leqq 0.2V$	–	3	5	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}=V_{IH}$ or CS2=V_{IL}	–	1	3	mA
	I_{SB1}*2	$\overline{CS1} \geqq V_{CC}-0.2V$, CS2 $\geqq V_{CC}-0.2V$ or $0V \leqq OS2 \leqq 0.2V$, $0V \leqq V_{in}$	–	0.02	2	mA
			–	2*3	100*3	μA
			–	2*4	50*4	
Output Voltage	V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
	V_{OH}	I_{OH}=–1.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC}=5.0V, T_a=25°C and specified loading.
*2. V_{IL} min=–0.3V
*3. This characteristics is guaranteed only for L-version.
*4. This characteristics is guaranteed only for LL-version.
*5. For 120ns/150ns version.
*6. For 100ns version.

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, Ta = 0 to +70°C)

• AC TEST CONDITIONS

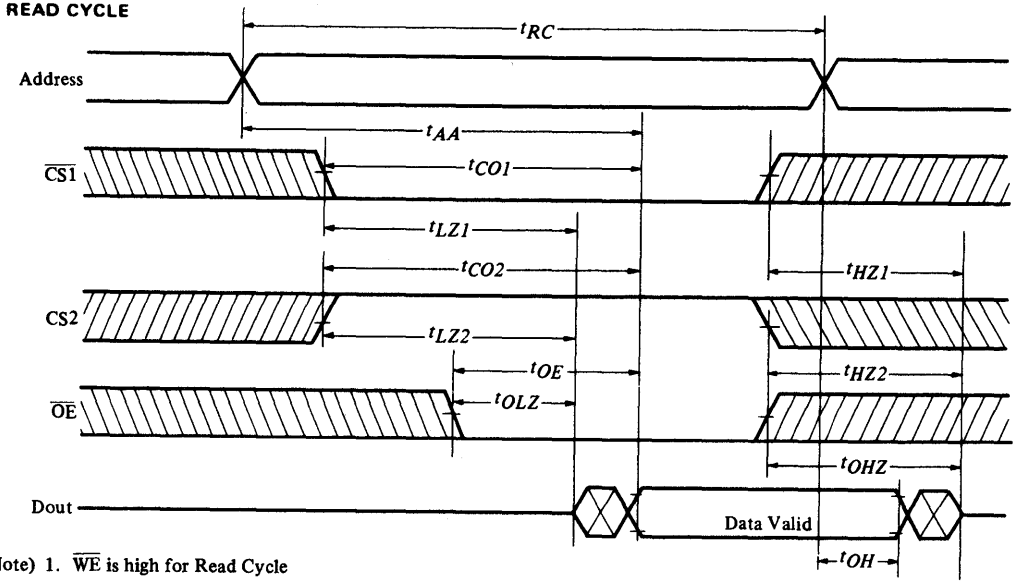
Input Pulse Levels: 0.8V/2.4V
Input Rise and Fall Time: 10ns
Input Timing Reference Level: 1.5V
Output Timing Reference Level: 0.8V/2.0V
Output Timing Reference Level: HM6264A-10 1.5V
HM6264A-12/15 0.8V/2.0V
Output Load: 1TTL Gate and C_L (100pF) (including scope and jig)

• READ CYCLE

Item		Symbol	HM6264A-10		HM6264A-12		HM6264A-15		Unit
			min	max	min	max	min	max	
Read Cycle Time		t_{RC}	100	–	120	–	150	–	ns
Address Access Time		t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	10	–	ns

Notes) 1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from d device to device.

• READ CYCLE

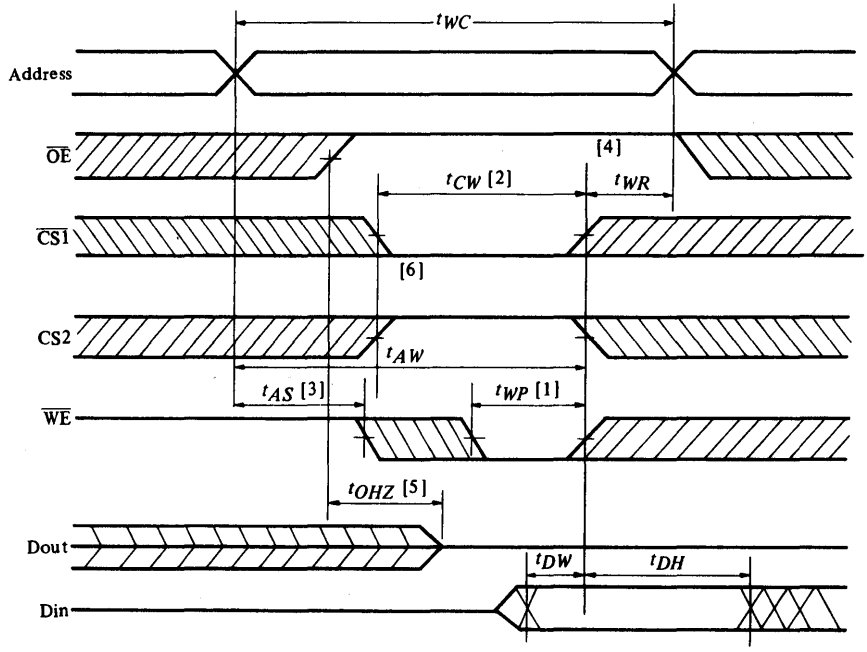


Note) 1. $\overline{WE}$ is high for Read Cycle

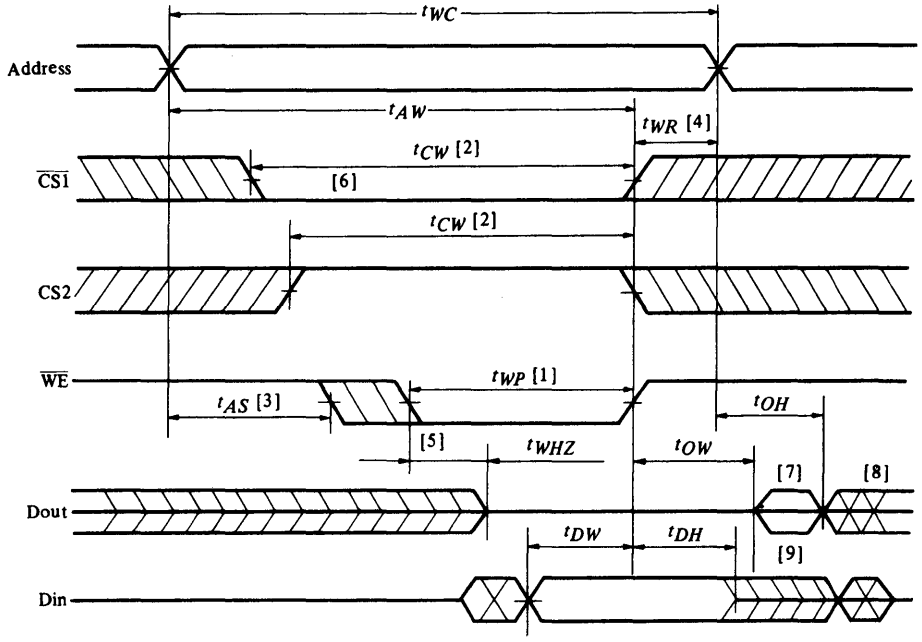
• WRITE CYCLE

Item	Symbol	HM6264A-10		HM6264A-12		HM6264A-15		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	80	–	85	–	100	–	ns
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	80	–	85	–	100	–	ns
Write Pulse Width	t_{WP}	60	–	70	–	90	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	40	–	50	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	ns
Output Enable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns

• WRITE CYCLE (1) ($\overline{OE}$ clock)



• WRITE CYCLE (2) ($\overline{OE}$ Low Fix)



NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.

2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

3) t_{AS} is measured from the address valid to the beginning of write.

4) t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

6) If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

7) Dout is the same phase of the latest written data in this write cycle.

8) Dout is the read data of next address.

9) If $\overline{CS1}$ is low and $\overline{CS2}$ is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

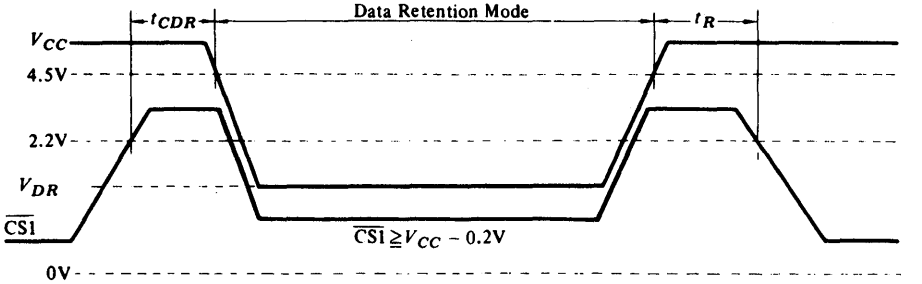
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L/LL-version.

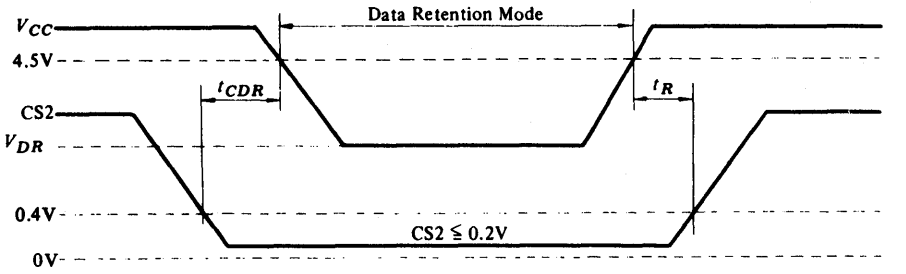
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \geq V_{CC}-0.2V$ or $CS2 \leq 0.2V$	2.0	–	–	V
Data RetentionCurrent	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS1} \geq V_{CC}-0.2V$, $CS2 \geq V_{CC}-0.2V$ or $0V \leq CS2 \leq 0.2V, 0V \leq V_{in}$	–	1*1	50*1	μA
			–	1*2	25*2	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*3	–	–	ns

Notes) *1. V_{IL} min = −0.3V, 20μA max at T_a=0 to 40°C, This characteristics is guaranteed only for L-version.
*2. V_{IL} min = −0.3V, 10μA max at T_a = 0 to 40°C, This characteristics is guarnteed only for LL-version.
*3. t_{RC} = Read Cycle Time

• LOW Vcc DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)

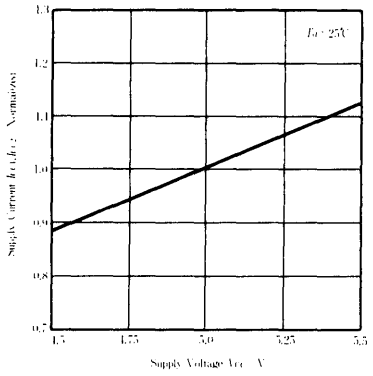


• LOW Vcc DATA RETENTION WAVEFORM (2) (CS2 Controlled)

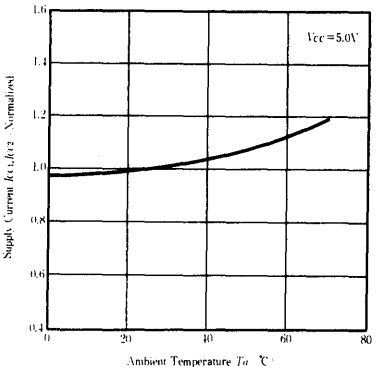


Note) In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and Din buffer. If CS2 controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either $CS2 \geq V_{CC}-0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

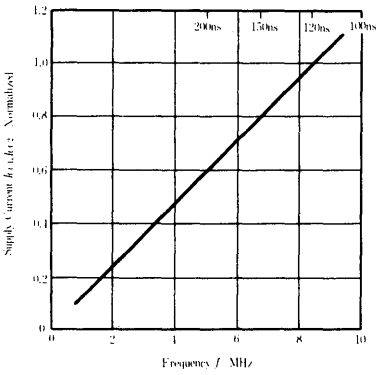
SUPPLY CURRENT VS. SUPPLY VOLTAGE



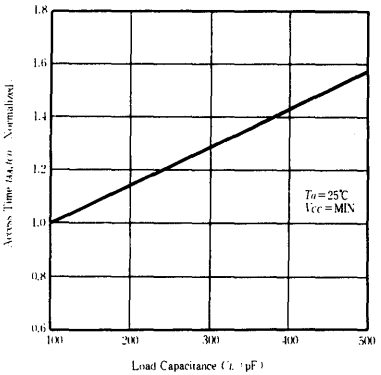
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



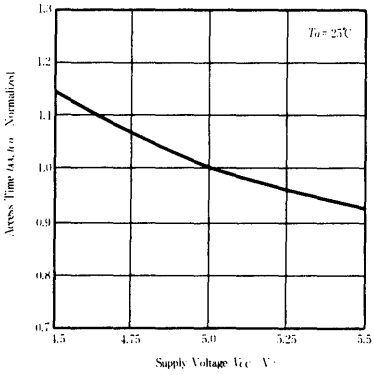
SUPPLY CURRENT VS. FREQUENCY



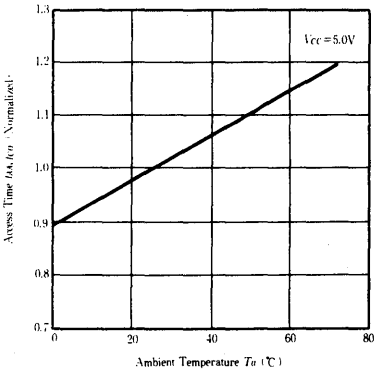
ACCESS TIME VS. LOAD CAPACITANCE



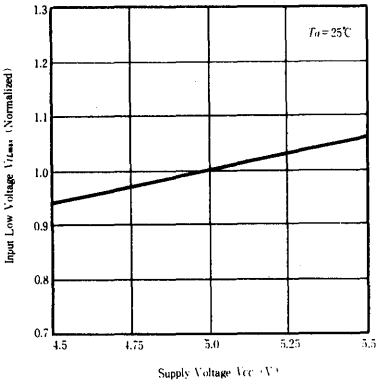
ACCESS TIME VS. SUPPLY VOLTAGE



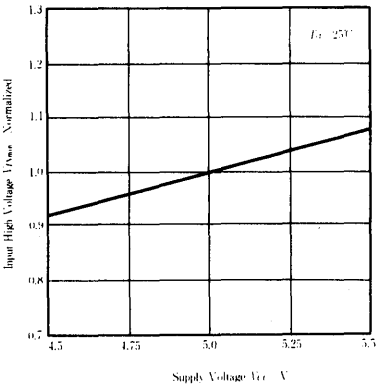
ACCESS TIME VS. AMBIENT TEMPERATURE



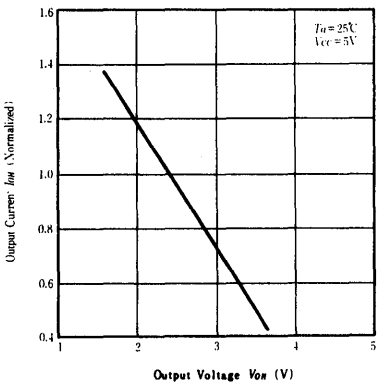
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



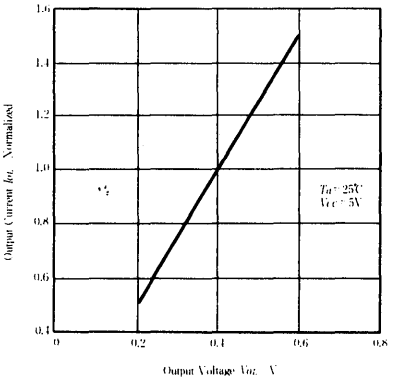
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



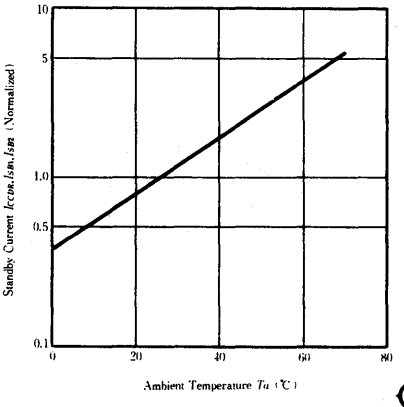
OUTPUT CURRENT VS. OUTPUT VOLTAGE



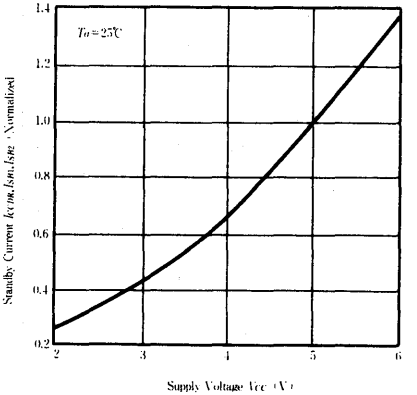
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



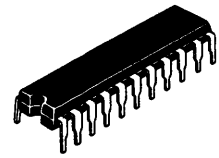
HM6288 Series

16384-word×4-bit High Speed CMOS Static RAM

The Hitachi HM6288 is a high speed 64k static RAM organized as 16-kword x 4-bit. It realizes high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6288, packaged in a 300 mil plastic DIP and SOJ, is available for high density mounting. Low power version retains the data with battery back up.



(DP-22NB)

(CP-24D)

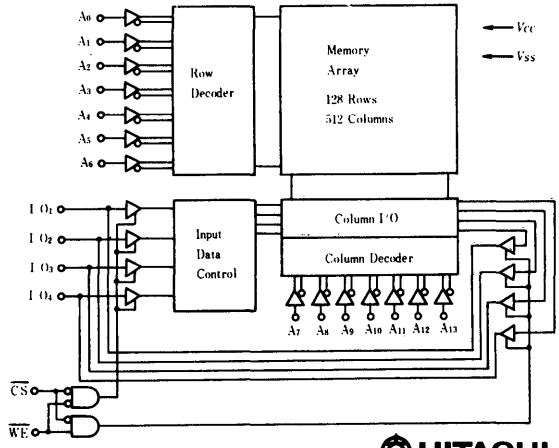
■FEATURES

- Single 5V Supply and High Density Plastic Package.
- High Speed: Fast Access Time 25/35/45 ns (max.)
- Low Power dissipation
  - Active mode 300mW (typ.)
  - Standby mode 100μW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required.
- Equal Access and Cycle Times.
- Directly TTL Compatible – All Inputs and Outputs.

■ ORDERING INFORMATION

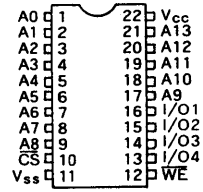
Type No.	Access Time	Package
HM6288P-25 HM6288P-35	25ns 35ns	300 mil 22-pin Plastic DIP (DP-22NB)
HM6288LP-25 HM6288LP-35	25ns 35ns	
HM6288JP-25 HM6288JP-35	25ns 35ns	300 mil 24-pin SOJ (CP-24D)
HM6288LJP-25 HM6288LJP-35	25ns 35ns	

■BLOCK DIAGRAM



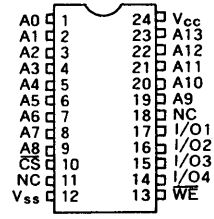
■PIN ARRANGEMENT

- HM6288P Series



(Top View)

- HM6288JP Series



(Top View)

■Pin Description

Pin Name	Function
A0 - A13	Address
I/O1–I/O4	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

HITACHI

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5^{*1} to $+7.0$	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Note: *1. V_T min. = −2.0V for pulse width ≦ 10ns

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■ RECOMMENDED DC OPERATING CONDITIONS (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-0.5^{*1}	–	0.8	V

Note: *1. V_{IL} min. = −2.0V for pulse width ≦ 10ns

■ DC AND OPERATING CHARACTERISTICS (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC} = MAX. $V_{IN} = V_{SS}$ to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS} = V_{IH}$, $V_{I/O} = V_{SS}$ to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_{I/O}$ = 0mA, min. cycle	–	60	120	mA
Standby V_{CC} Current	I_{SB}	$\overline{CS} = V_{IH}$, min. cycle	–	15	30	mA
Standby V_{CC} Current 1	I_{SB1}*2	$\overline{CS} \geqq V_{CC} - 0.2V$	–	0.02	2.0	mA
	I_{SB1}*3	$0V \leqq V_{IN} \leqq 0.2V$ or $V_{CC} - 0.2V \leqq V_{IN}$	–	0.02	0.1	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4.0mA	2.4	–	–	V

Notes: *1. Typical limits are at V_{CC} = 5.0V, Ta = +25°C and specified loading.
*2. P version
*3. LP version

■ CAPACITANCE (Ta = 25°C, f = 1.0MHz)

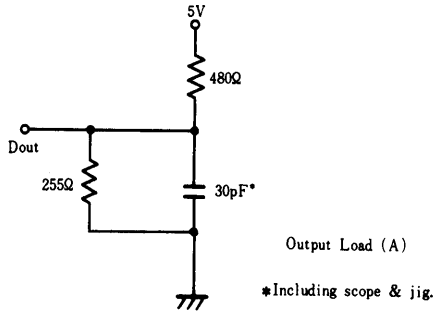
Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	8	pF

Note: This parameter is sampled and not 100% tested

■AC CHARACTERISTICS

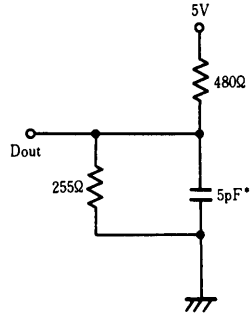
- **AC Test Conditions**

Input pulse levels: 0V to 3.0V
Input rise and fall times: 5ns
Input and Output timing reference levels: 1.5V
Output load: See Figure



Output Load (A)

*Including scope & jig.



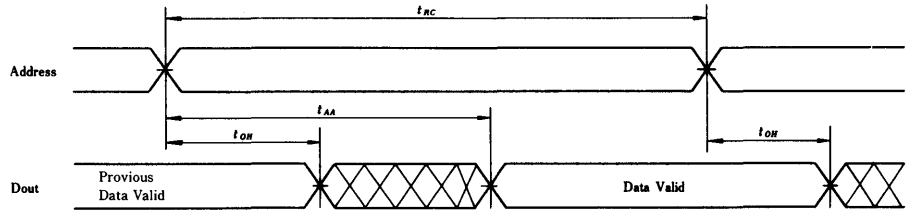
Output Load (B)
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

■ READ CYCLE

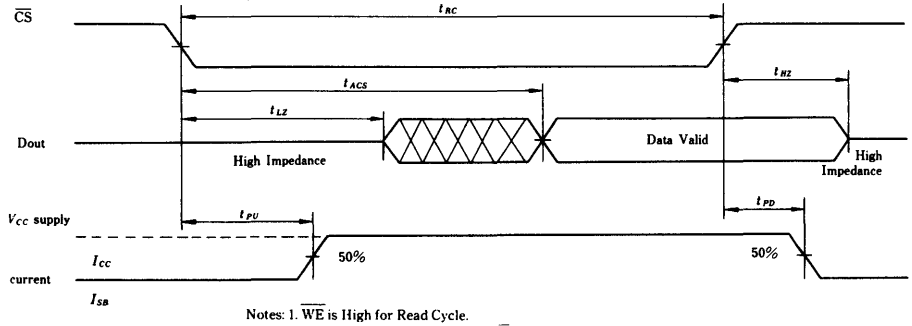
Parameter	Symbol	HM6288-25		HM6288-35		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	–	35	–	ns
Address Access Time	t_{AA}	–	25	–	35	ns
Chip Select Access Time	t_{ACS}	–	25	–	35	ns
Output Hold from Address Change	t_{OH}	3	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ}*	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{HZ}*	0	12	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Seselection to Power Down Time	t_{PD}	–	25	–	30	ns

* Transition is measured ±200mV from steady state voltage with Load(B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No.1 [1] [2]



● Timing Waveform of Read Cycle No.2 [1] [3]



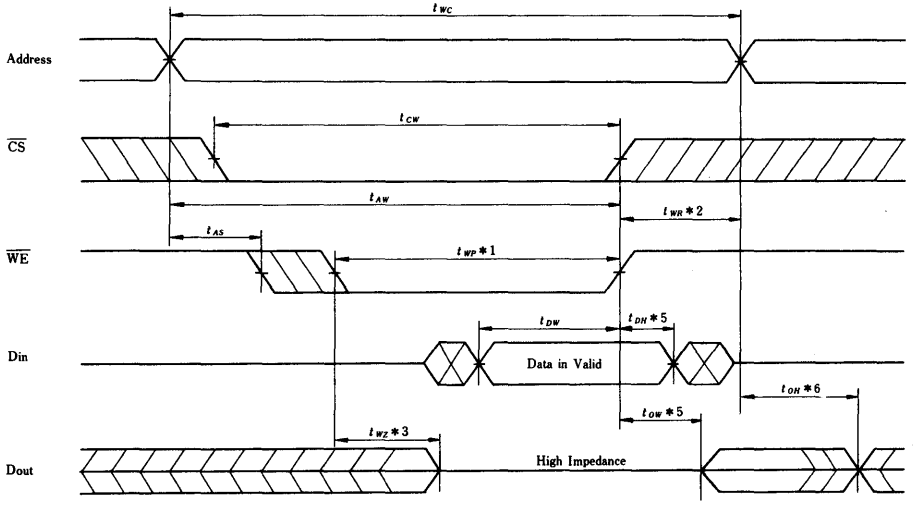
Notes: 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.

■ WRITE CYCLE

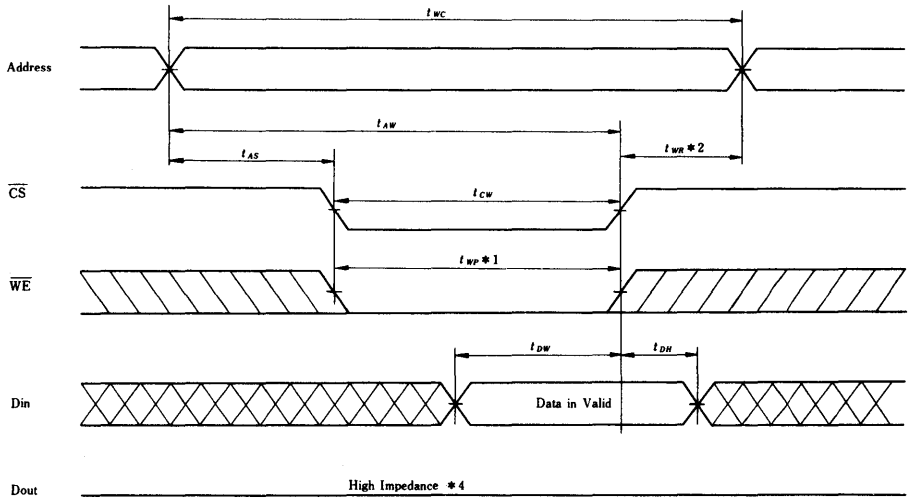
Parameter	Symbol	HM6288-25		HM6288-35		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	–	35	–	ns
Chip Selection to End of Write	t_{CW}	20	–	30	–	ns
Address Valid to End of Write	t_{AW}	20	–	30	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Write Pulse Width	t_{WP}	20	–	30	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Date Valid to End of Write	t_{DW}	12	–	20	–	ns
Data Hold Time	t_{DH}	0	–	0	–	ns
Write Enabled to Output in High Z	t_{WZ}*	0	8	0	10	ns
Output Active from End of Write	t_{OW}*	5	–	5	–	ns

* Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Write Cycle No.1 ($\overline{WE}$ Controlled)



● Timing Waveform of Write Cycle No.2 ($\overline{CS}$ Controlled)



Notes) 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tow. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

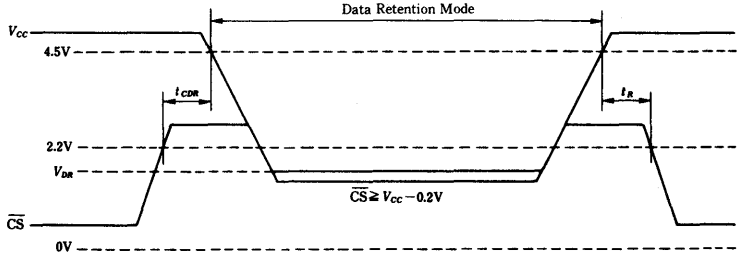
● Low *Vcc* Data Retention Characteristics (Ta=0 to +70°C)

(This Characteristics is guaranteed only for L-version.)

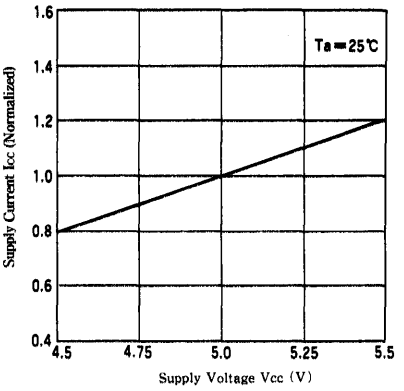
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geq V_{CC}-0.2V$
Data retention current	I_{CCDR}	–	–	50[2] 35[3]	μA	$V_{in} \geq V_{CC}-0.2V$ or $0V \leq V_{in} \leq 0.2V$
Chip deselect to data retention time	t_{CDR}	0	–	–	ns	See retention waveform
Operation recovery time	t_R	t_{RC}[1]	–	–	ns	

NOTE : 1. t_{RC} = Read cycle time
2. V_{CC} = 3.0V
3. V_{CC} = 2.0V

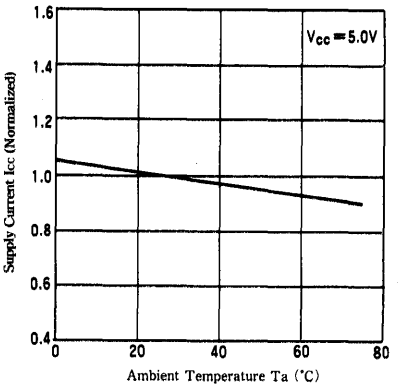
Low *Vcc* Data Retention Waveform



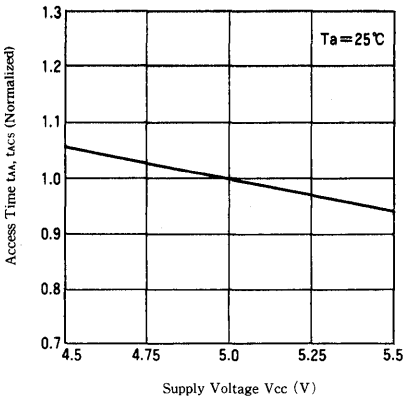
SUPPLY CURRENT VS. SUPPLY VOLTAGE



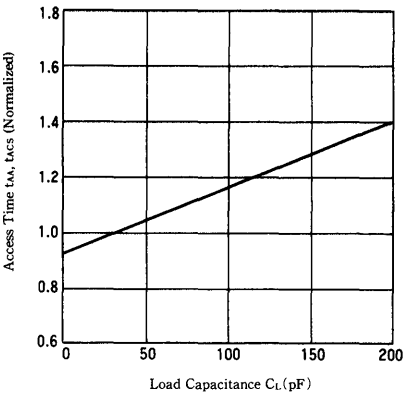
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



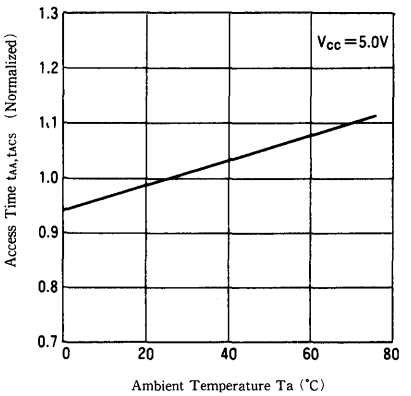
ACCESS TIME VS. SUPPLY VOLTAGE



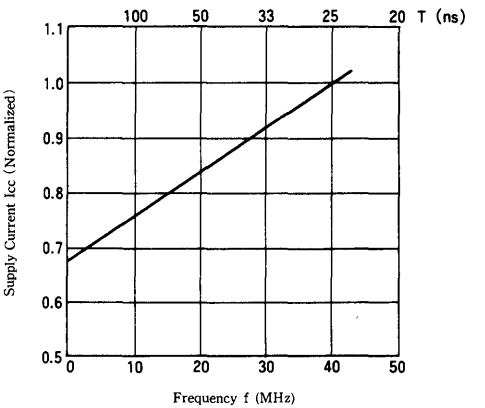
ACCESS TIME VS. LOAD CAPACITANCE



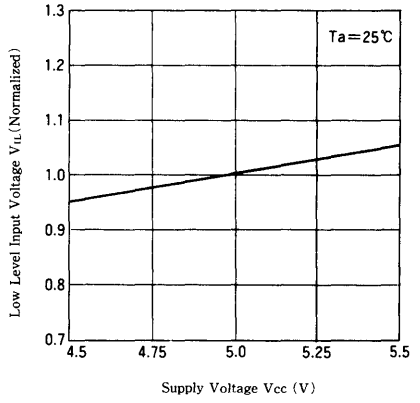
ACCESS TIME VS. AMBIENT TEMPERATURE



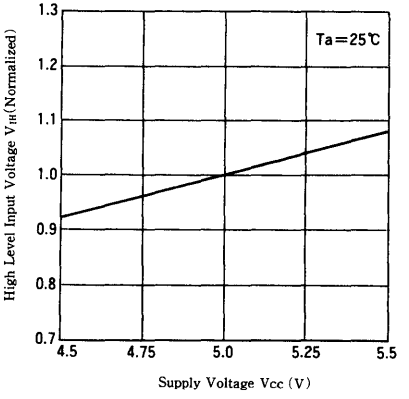
SUPPLY CURRENT VS. FREQUENCY



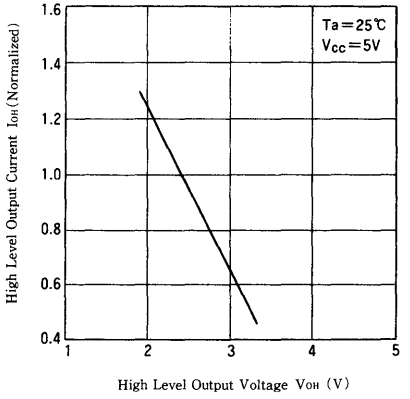
LOW LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



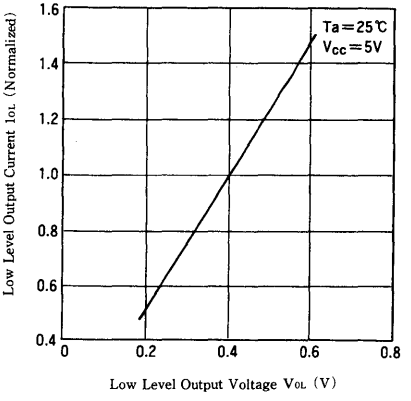
HIGH LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



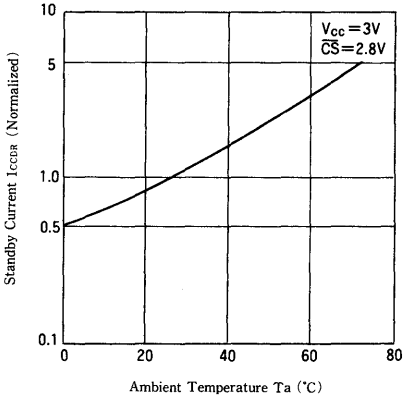
OUTPUT CURRENT VS. OUTPUT VOLTAGE(1)



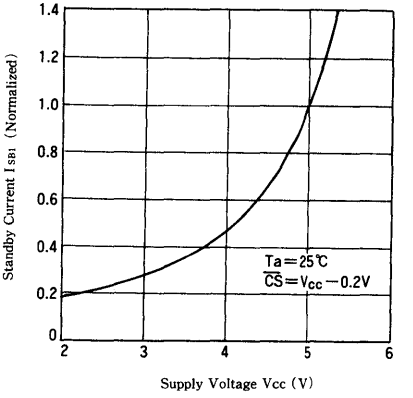
OUTPUT CURRENT VS. OUTPUT VOLTAGE(2)



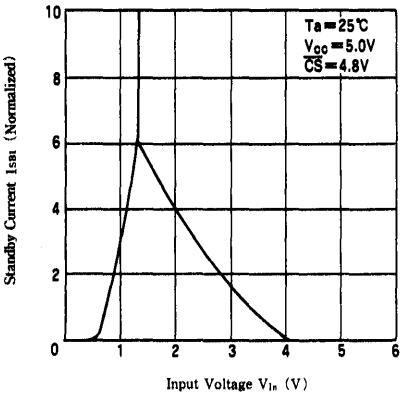
STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



STANDBY CURRENT VS. INPUT VOLTAGE

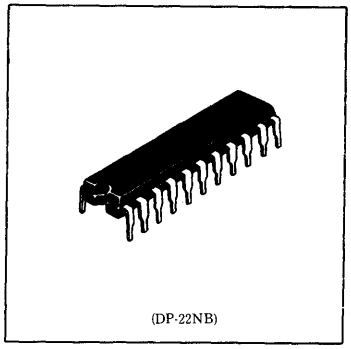


HM6788 Series — Maintenance Only

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM

■FEATURES

- Super Fast Access Time : 25/30ns (max.)
- Low power Operation
  Operating: 230mW (typ), Standby: 10mW (typ)
- +5V Single Supply
- Completely Static Memory –
  No Clock or Timing Strobe required
- Balanced Read and Write Cycle Time
- Fully TTL compatible Input and Output

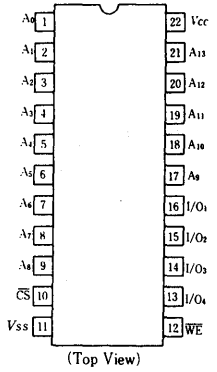


(DP-22NB)

■ ORDERING INFORMATION

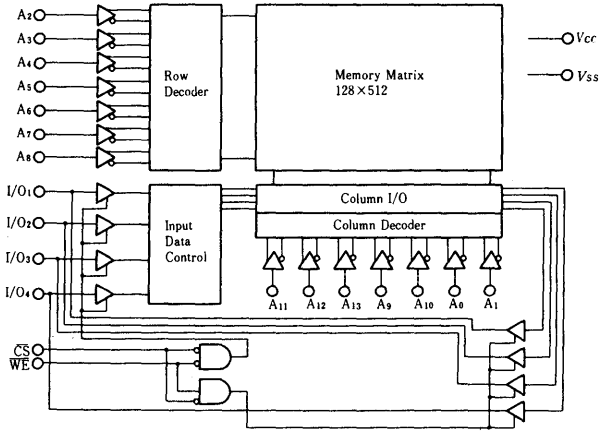
Type No.	Access Time	Package
HM6788P-25	25ns	300 mil 22 pin Plastic DIP
HM6788P-30	30ns	

■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (with bias)	T_{stg}(bias)	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

■TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2)
L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1) (2)

×: H or L

■RECOMMENDED DC OPERATING CONDITIONS ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V with 20ns pulse width.

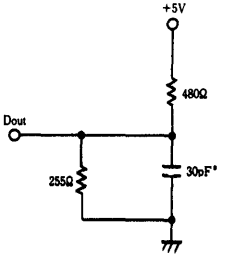
■DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $Ta=0°C$ to $+70°C$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	$V_{CC}=5.5V$, $V_{IN}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	2	μA
Opearating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0mA$	–	–	80	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%	–	–	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	–	–	30	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC}-0.2V$, $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$	–	–	10	mA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	–	–	0.5	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	–	–	V

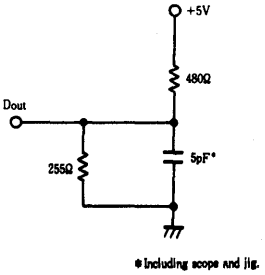
■AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

- **AC Test Conditions**

Input pulse levels: V_{SS} to 3.0V
Input rise and fall time: 4ns
Input and Output reference levels: 1.5V
Output Load: See Figure



Output Load A



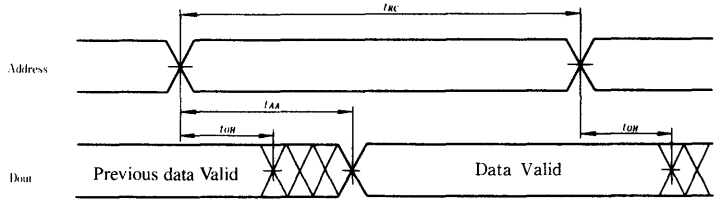
Output Load B
(t_{CHZ}, t_{WHZ}, t_{CLZ}, t_{OW})

● READ CYCLE

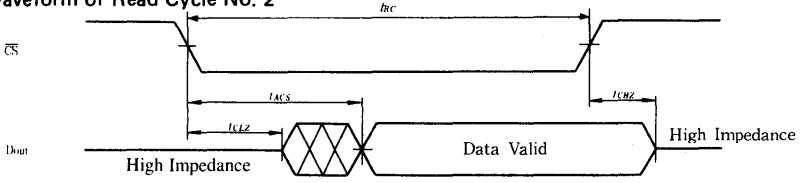
Item	Symbol	HM6788-25		HM6788-30		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	—	30	—	ns
Address Access Time	t_{AA}	—	25	—	30	ns
Chip Select Access Time	t_{ACS}	—	25	—	30	ns
Chip Selection to Output in Low Z	t_{CLZ} *2	0	—	0	—	ns
Chip Deselection to Output in High Z	t_{CHZ} *2	0	10	0	12	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Power Up Time*1	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time*1	t_{PD}	—	20	—	30	ns
Input Voltage Rise/Fall Time*3	t_T	—	150	—	150	ns

Notes) *1. This parameter is sampled and not 100% tested.
*2. Transition is measured ±200mV form steady state voltage with Load (B). This parameter is sampled and not 100% tested
*3. If t_T becomes more than 150ns, there is possibility of function fail.
please contact your nearest Hitachi Sales Dept. regarding specification.

● Timing waveform of Read Cycle No. 1 *1,*2



● Timing waveform of Read Cycle No. 2 *1,*3



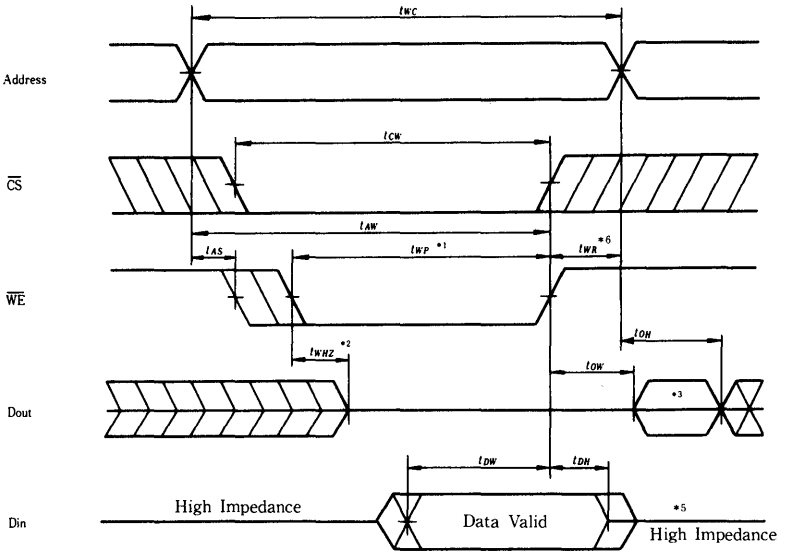
Note) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

● WRITE CYCLE

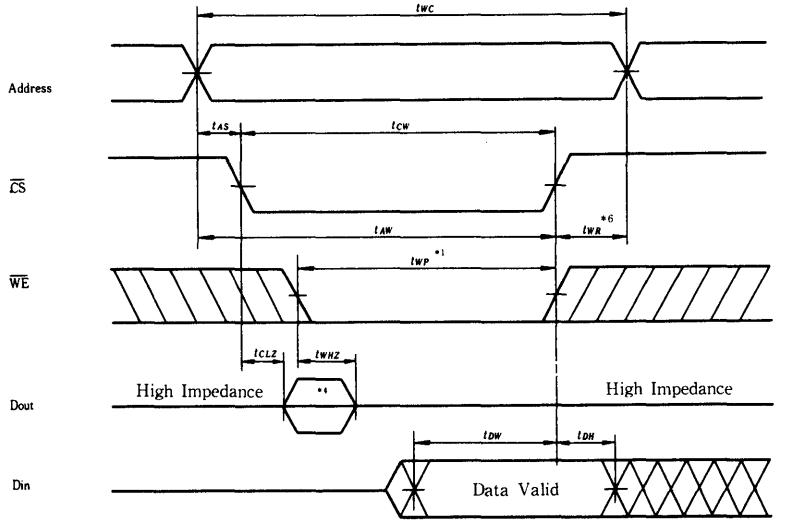
Item	Symbol	HM6788-25		HM6788-30		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	—	30	—	ns
Chip Selection to End of Write	t_{CW}	20	—	25	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	20	—	25	—	ns
Write Pulse Width	t_{WP}	20	—	25	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Write to Output in High Z	t_{WHZ} *1	0	10	0	12	ns
Data Valid to End of Write	t_{DW}	15	—	15	—	ns
Data Hold Time	t_{DH}	5	—	5	—	ns
Output Active from End of Write	t_{OW} *1	0	—	0	—	ns

*1. Transition is measured ±200mV from steady state voltage with Lood(B).
This parameter is sampled and not 100% tested.

- Timing waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



- Timing waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3. Dout is the same phase of write data of this write cycle.
*4. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
*6. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

■CAPACITANCE (Ta=25°C, f=1.0MHz)

Item	Symbol	min	typ	max	Conditions
Input Capacitance	C_{IN}	–	–	6.0	V_{IN}=0V
Input/Output Capacitance	$C_{I/O}$	–	–	8.0	V_{OUT}=0V

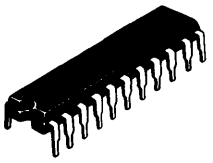
Note) This parameter is sampled and not 100% tested.

HM6788H Series

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM

Features

- Super Fast Access Time : 15/20ns (max.)
- Low power Operation
  Operating: 280mW (typ)
- +5V Single Supply
- Completely Static Memory –
  No Clock or Timing Strobe required
- Equal Access and Cycle Times
- Fully TTL compatible Input and Output

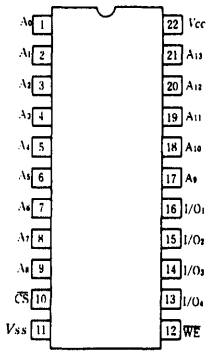


(DP-22NB)

Ordering Information

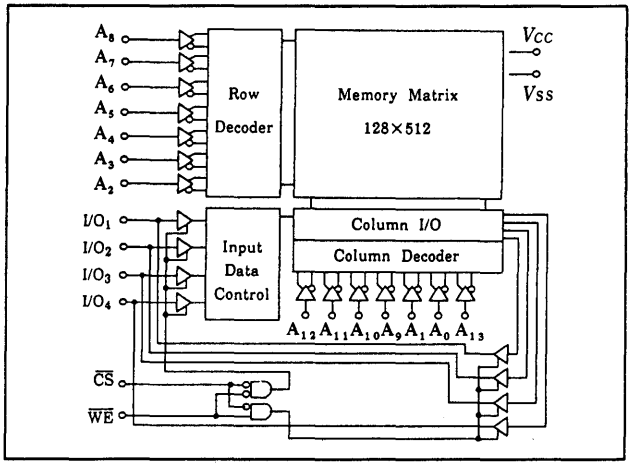
Type No.	Access Time	Package
HM6788HP-15	15ns	300 mil 22 pin Plastic DIP
HM6788HP-20	20ns	

Pin Arrangement



(Top View)

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to *Vss* pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (with bias)	T_{stg}(bias)	−10 to +85	°C
Storage Temperature	T_{stg}	−55 to +125	°C

Note) The specifications of this device are subject to change without notice.
Please contact Hitachi's Sales Dept. regarding specifications.

Truth Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1), (2)
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1), (2)

×: H or L

Recommended DC Operating Conditions ($0°C \leq Ta \leq 70°C$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V with 10ns pulse width.

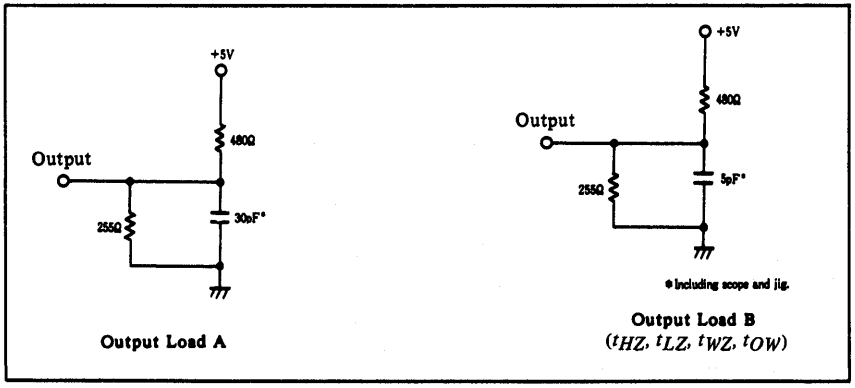
DC and Operating Characteristics ($V_{CC}=5V \pm 10\%$, $Ta=0°C$ to $+70°C$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	$V_{CC}=5.5V$, $V_{IN}=V_{SS}$ to V_{CC}	–	–	2	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}=V_{IH}$, $V_{I/O}=V_{SS}$ to V_{CC}	–	–	10	μA
Opearating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0mA$	–	–	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100% $I_{I/O}=0mA$	–	–	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	–	–	30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	–	–	10	mA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	–	–	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	–	–	V

AC Characteristics (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

- **AC Test Conditions**

  Input pulse levels: V_{SS} to 3.0V
  Input rise and fall time: 4ns
  Input and Output reference levels: 1.5V
  Output Load: See Figure

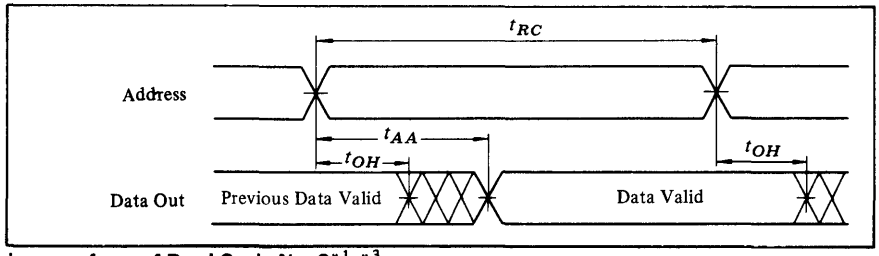


Read Cycle

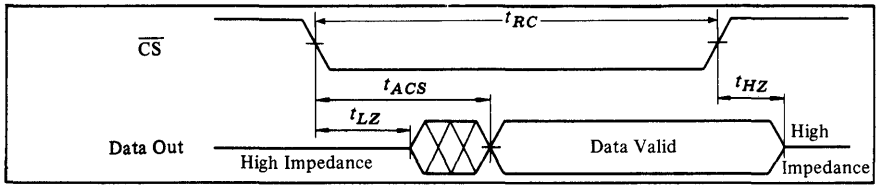
Item	Symbol	HM6788H-15		HM6788H-20		Unit	Note
		min	max	min	max		
Read Cycle Time	t_{RC}	15	–	20	–	ns	
Address Access Time	t_{AA}	–	15	–	20	ns	
Chip Select Access Time	t_{ACS}	–	15	–	20	ns	
Chip Selection to Output in Low Z	t_{LZ}	3	–	3	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	ns	1, 2
Output Hold from Address Change	t_{OH}	3	–	3	–	ns	

Note) *1. This parameter is sampled and not 100% tested.
*2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

- **Timing waveform of Read Cycle No. 1*1,*2**



- **Timing waveform of Read Cycle No. 2*1,*3**



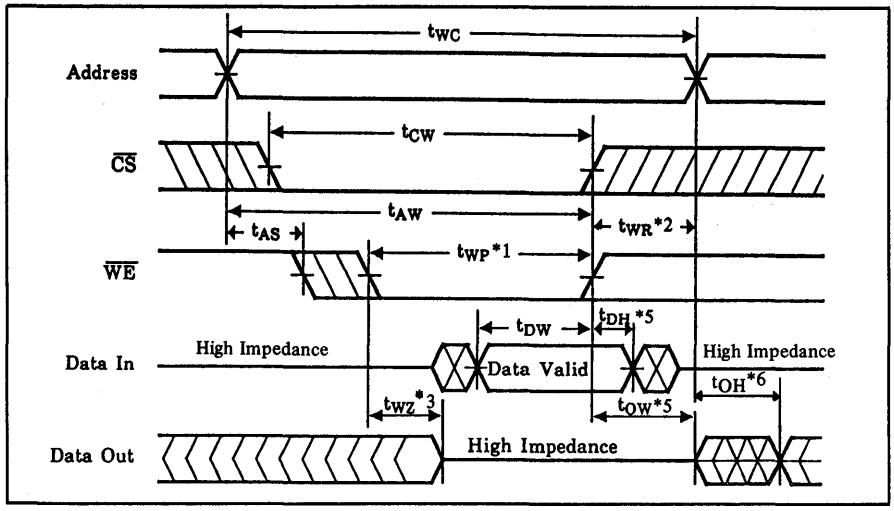
Note) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. Address valid prior to or coincident with $\overline{CS}$ transition Low.

Write Cycle

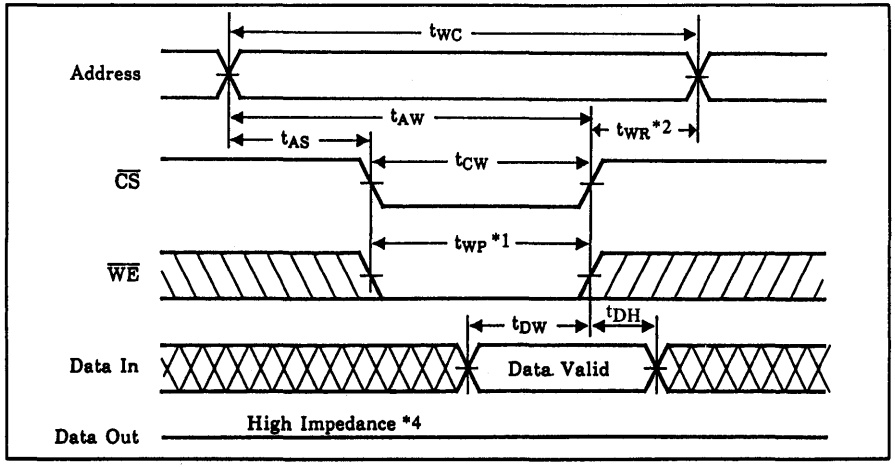
Item	Symbol	HM6788H-15		HM6788H-20		Unit	Note
		min	max	min	max		
Write Cycle Time	t_{WC}	15	–	20	–	ns	2
Chip Selection to End of Write	t_{CW}	10	–	15	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AW}	10	–	15	–	ns	
Write Pulse Width	t_{WP}	10	–	15	–	ns	
Write Recovery Time	t_{WR}	1	–	1	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	ns	3, 4
Data Valid to End of Write	t_{DW}	9	–	10	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

- **Timing waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)**



- **Timing waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)**



Note)*1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})

*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.

*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

*6. Data Out is the same phase of write data of this write cycle.

Capacitance (Ta=25°C, f=1.0MHz)

Item	Symbol	min	typ	max	Conditions
Input Capacitance	C_{IN}	–	–	6.0	V_{IN}=0V
Input/Output Capacitance	$C_{I/O}$	–	–	10	$V_{I/O}$=0V

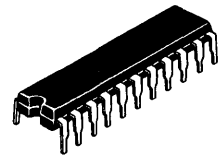
Note) This parameter is sampled and not 100% tested.

HM6788HA Series — Preliminary

16384-Word × 4-Bit High Speed Static RAM

■ FEATURES

- Super Fast
  Access Time. . . . . .12/15/20ns (max.)
- +5V Single Supply
- Low Power Dissipation
  (DC) Operating . . . . . .300mW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Fully TTL Compatible—All Inputs and Outputs

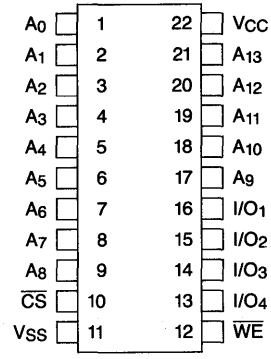


(DP-22NB)

■ ORDERING INFORMATION

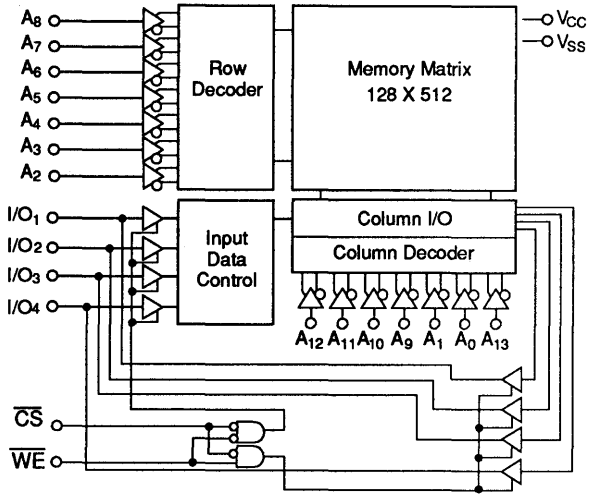
Type No.	Access Time	Package
HM6788HAP-12	12ns	300 mil 22 pin
HM6788HAP-15	15ns	Plastic DIP
HM6788HAP-20	20ns	(DP-22NB)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{bias}	-10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_a \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	-3.0*	—	0.8	V

*Pulse width ≤ 10ns, DC: -0.5V

■ TRUTH TABLE

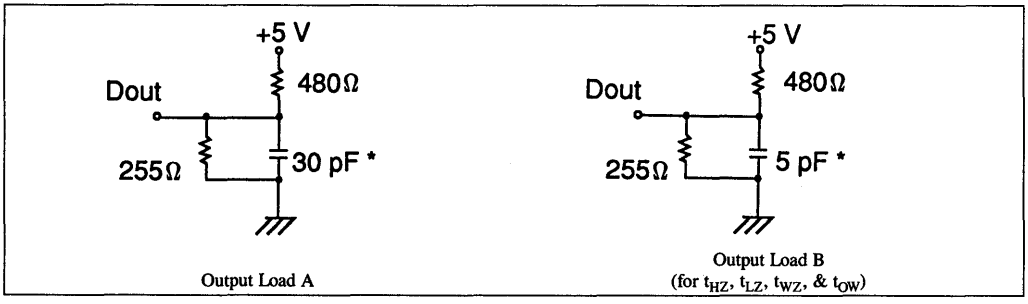
$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1), (2)
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1), (2)

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, V_{SS} = 0V)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$, = 0mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle Duty: 100% $I_{I/O}$ = 0mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	—	—	30	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}$ ≥ V_{CC} - 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} - 0.2V	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input Timing Reference Levels: 1.5V
- Output Load: See Figure
- Input Rise and Fall Times: 4ns
- Output Reference Levels: 1.5V



Output Load A

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ}, & t_{OW})

*Including scope and jig capacitance.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Max.	Unit	Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	10.0	pF	$V_{I/O}$ = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6788HA-12		HM6788HA-15		HM6788HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	12	—	15	—	20	—	ns	—
Address Access Time	t_{AA}	—	12	—	15	—	20	ns	—
Chip Select Access Time	t_{ACS}	—	12	—	15	—	20	ns	—
Output Hold from Address Change	t_{OH}	4	—	4	—	4	—	ns	—
Chip Selection to Output in Low Z	t_{LZ}	3	—	5	—	5	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	6	0	8	ns	1, 2

NOTES: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• Write Cycle

Item	Symbol	HM6788HA-12		HM6788HA-15		HM6788HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	12	—	15	—	20	—	ns	2
Chip Selection to End of Write	t_{CW}	8	—	10	—	15	—	ns	—
Address Valid to End of Write	t_{AW}	8	—	10	—	15	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Write Pulse Width	t_{WP}	8	—	10	—	15	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Data Valid to End of Write	t_{DW}	6	—	7	—	10	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Write Enable to Output in High Z	t_{WZ}	0	6	0	6	0	8	ns	3, 4
Output Active from End of Write	t_{OW}	3	—	3	—	3	—	ns	3, 4

NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

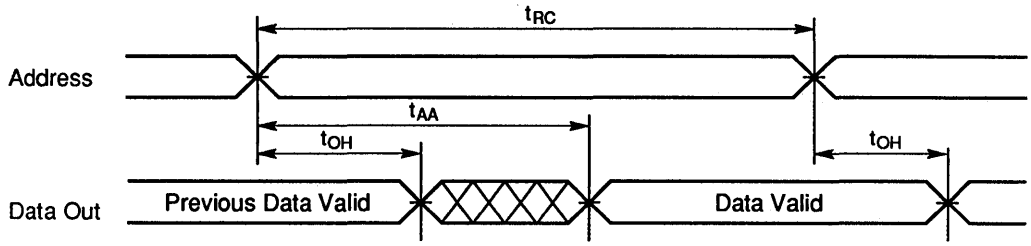
2. All write cycle timings are referenced from the last valid address to the first transitioning address.

3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

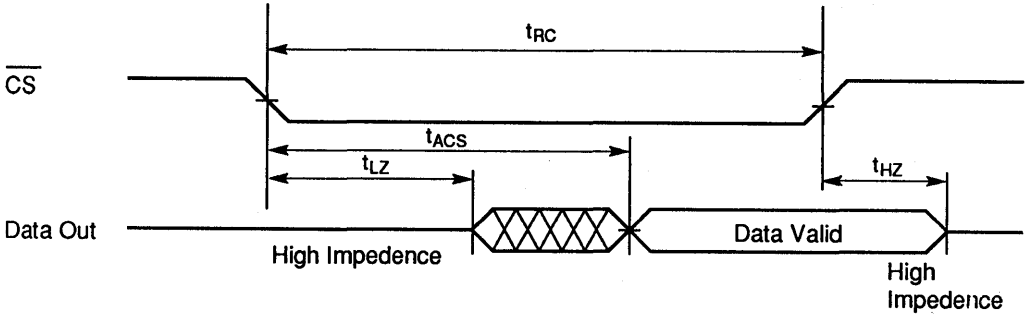
4. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

• Read Cycle (1) (1) (2)

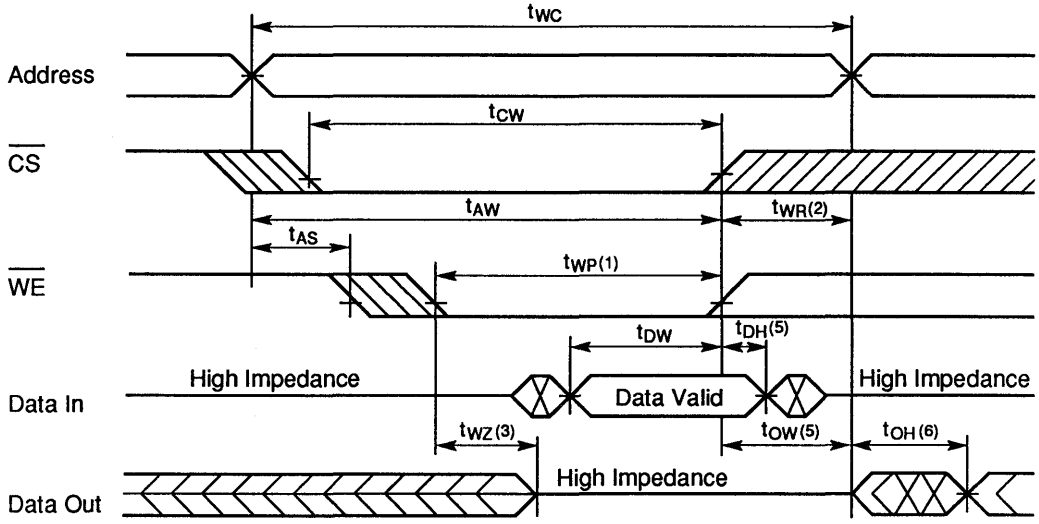


• Read Cycle (2) (1) (3)

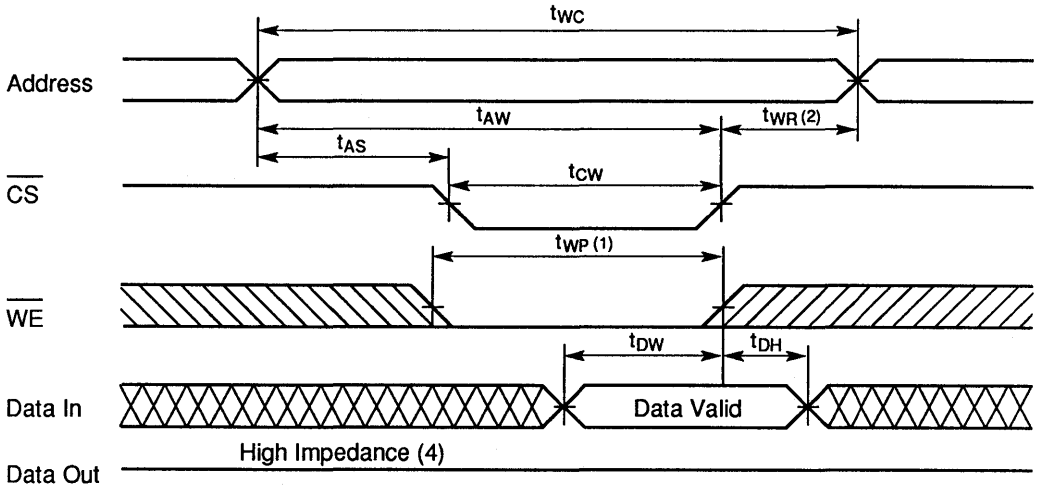


NOTES: 1. $\overline{WE}$ is High for READ cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

• **Write Cycle (1)** ($\overline{WE}$ Controlled)



• **Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTES:

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. D_{out} is the same phase of write data of this write cycle.

HM6289 Series

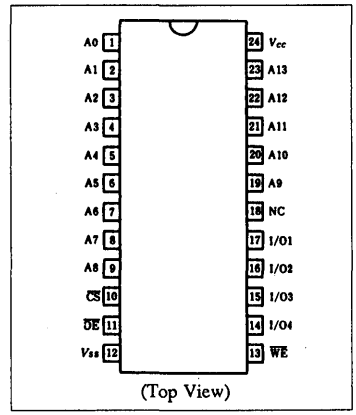
16384-Word × 4-Bit High Speed CMOS Static RAM (with $\overline{OE}$)

The Hitachi HM6289 is a high speed 64k static RAM organized as 16-kword x 4-bit. It realizes high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology.

It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6289, packaged in a 300-mil SOJ, is available for high density mounting. Low power version retains the data with battery back up.

Pin Arrangement



(Top View)

Features

- High speed
  - Access time: 25/35 ns (max)
- High density 24-pin SOJ package
- Low power
  - Active mode: 300 mW (typ)
  - Standby mode: 100 μW (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs

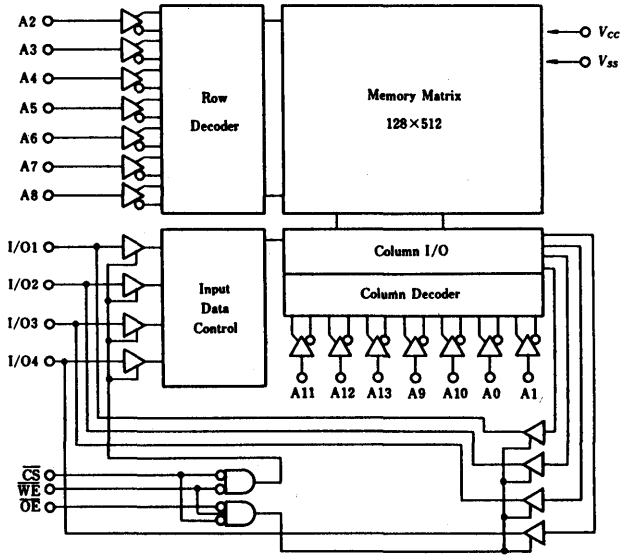
Ordering Information

Type No.	Access Time	Package
HM6289JP-25	25 ns	300-mil
HM6289JP-35	35 ns	24-pin
HM6289LJP-25	25 ns	SOJ
HM6289LJP-35	35 ns	(CP-24D)

Pin Description

Pin Name	Function
A0–A13	Address
I/O1–I/O4	Input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Vcc Current	I/O pin	Ref. Cycle
H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	Icc	Dout	Read cycle (1)–(3)
L	H	L	Write	Icc	Din	Write cycle (1)–(2)
L	L	L	Write	Icc	Din	Write cycle (3)–(6)

Note: ×; H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{in}	–0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	T_{stg}	–55 to +125	°C
Storage temperature range under bias	T_{bias}	–10 to +85	°C

Note: *1. Vin min = –2.0 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
	Vss	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

DC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, Vss = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	Vcc = Max Vin = 0V to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = 0 V to Vcc
Operating Vcc current	Icc	—	60	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. cycle
Standby Vcc current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, Min. cycle
Standby Vcc current (1)	I_{SB1}*2	—	0.02	2.0	mA	$\overline{CS}$ ≥ Vcc – 0.2 V 0V ≤ Vin ≤ 0.2 V or Vcc – 0.2 V ≤ Vin
	I_{SB1}*3	—	0.02	0.1	mA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: *1. Typical limits are at Vcc = 5.0 V, Ta = +25°C and specified loading.
*2. P-version
*3. LP-version

Capacitance (Ta = 25°C, f = 1MHz)

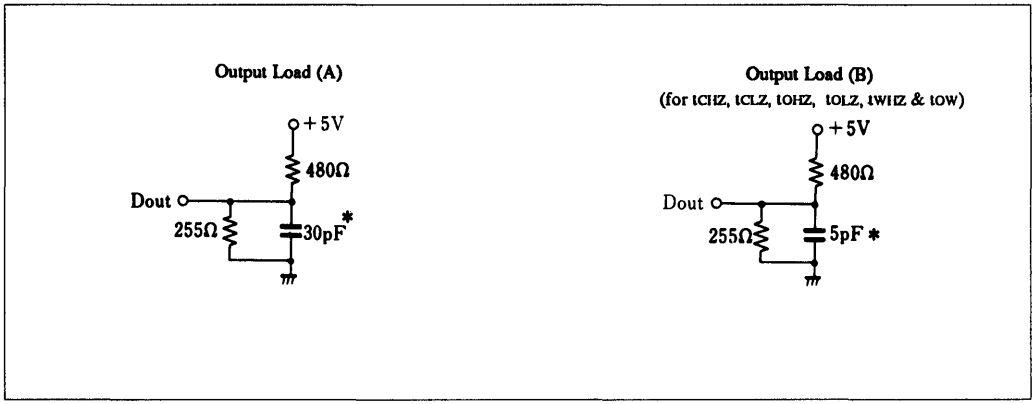
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Input/output capacitance	$C_{I/O}$	—	—	8	pF	V I/O = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

Input pulse levels:	Vss to 3.0 V
Input rise and fall times:	5 ns
Input and output timing reference levels:	1.5 V
Output load:	See figures



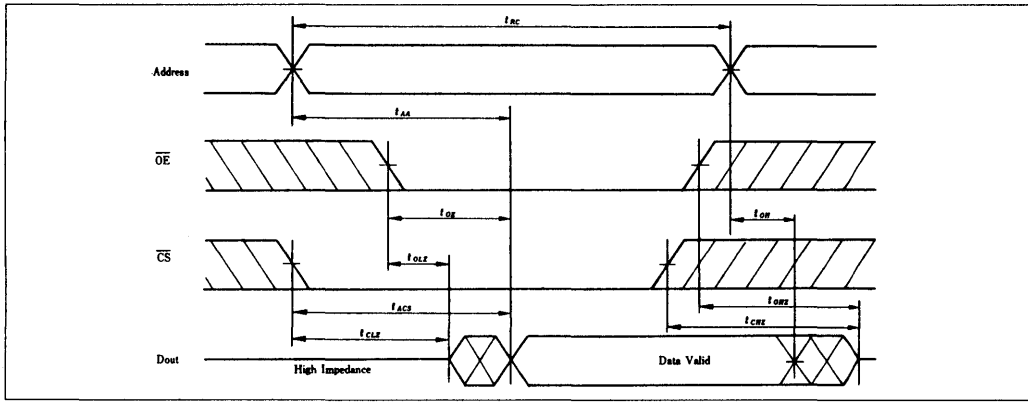
Note: * Including scope & jig.

Read Cycle

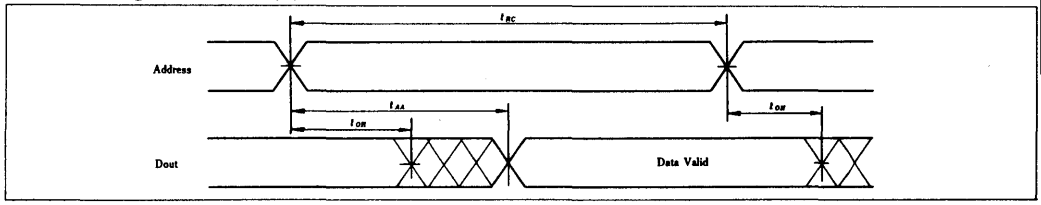
Item	Symbol	HM6289-25		HM6289-35		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Chip selection to output in low-Z	t_{CLZ}*1	5	—	5	—	ns
Output enable to output valid	t_{OE}	—	12	—	15	ns
Output enable to output in low-Z	t_{OLZ}*1	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}*1	0	12	0	20	ns
Chis disable to output in high-Z	t_{OHZ}*1	0	10	0	10	ns
Output hold from address change	t_{OH}	3	—	5	—	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	25	—	30	ns

Note: *1. Output transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

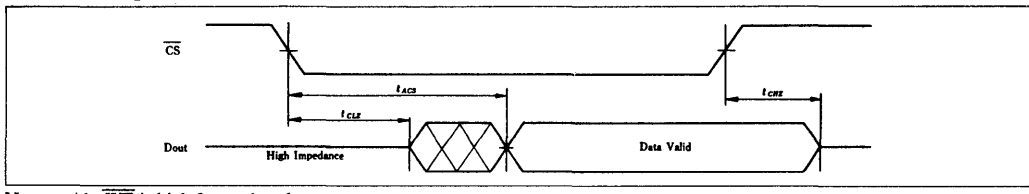
Read Timing Waveform (1) *1



Read Timing Waveform (2) *1,*2,*4



Read Timing Waveform (3) *1,*3,*4



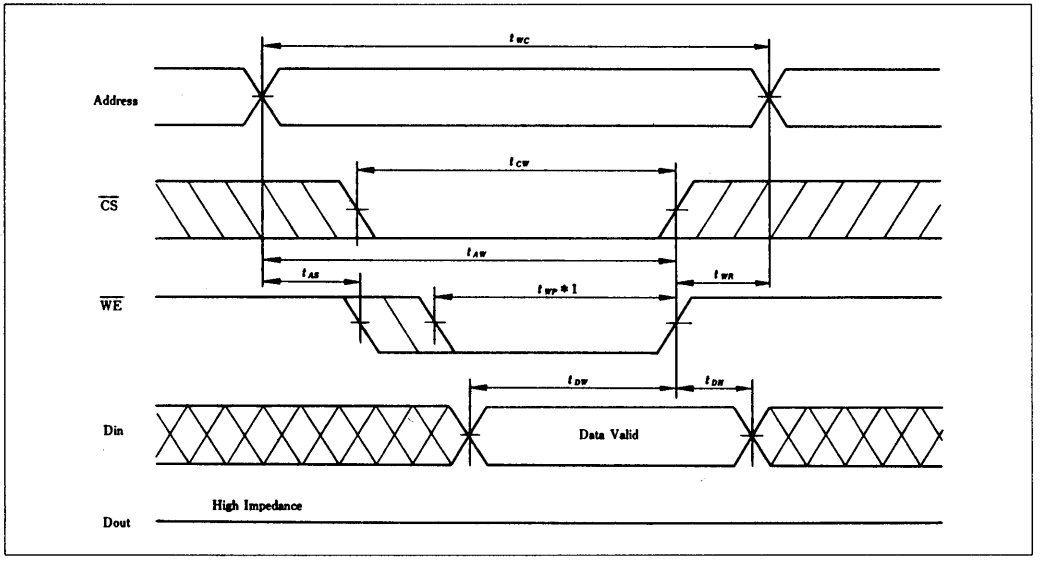
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

Write Cycle

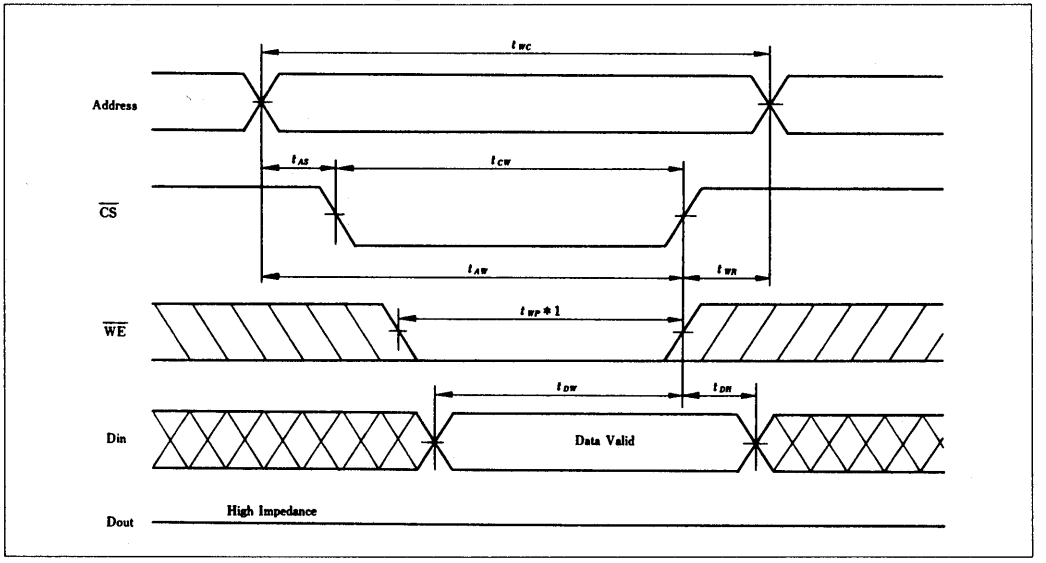
Item	Symbol	HM6289-25		HM6289-35		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	30	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Output disable to output in high-Z*1	t_{OHZ}	0	10	0	10	ns
Write to output in high-Z*1	t_{WHZ}	0	8	0	10	ns
Data to write time overlap	t_{DW}	12	—	20	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Output active from end of write*1	t_{OW}	5	—	5	—	ns

Note: *1. Output transition is measured ± 200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

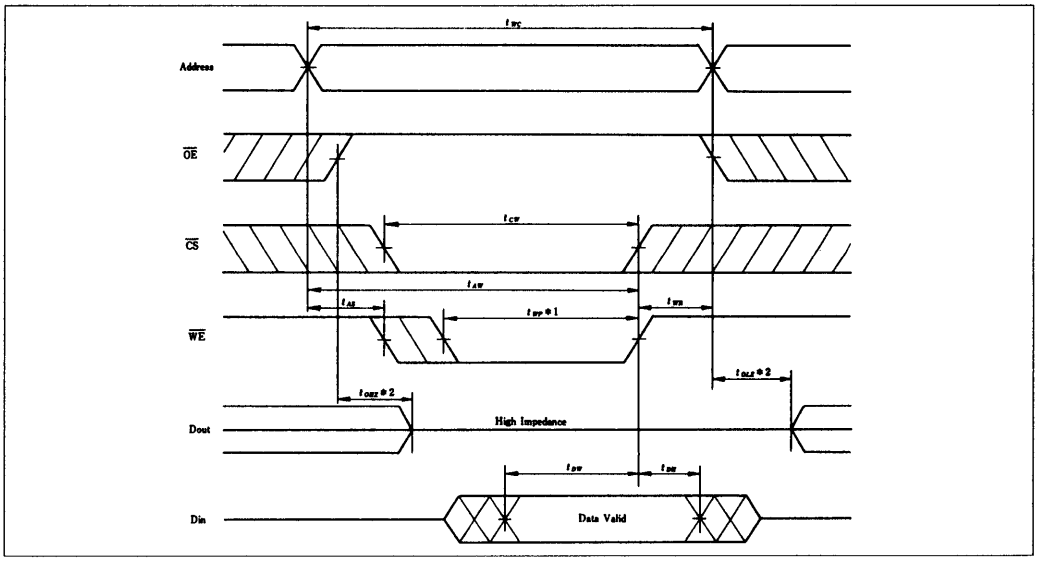
Write Timing Waveform (1) ($\overline{OE}$ = High, $\overline{WE}$ = Controlled)



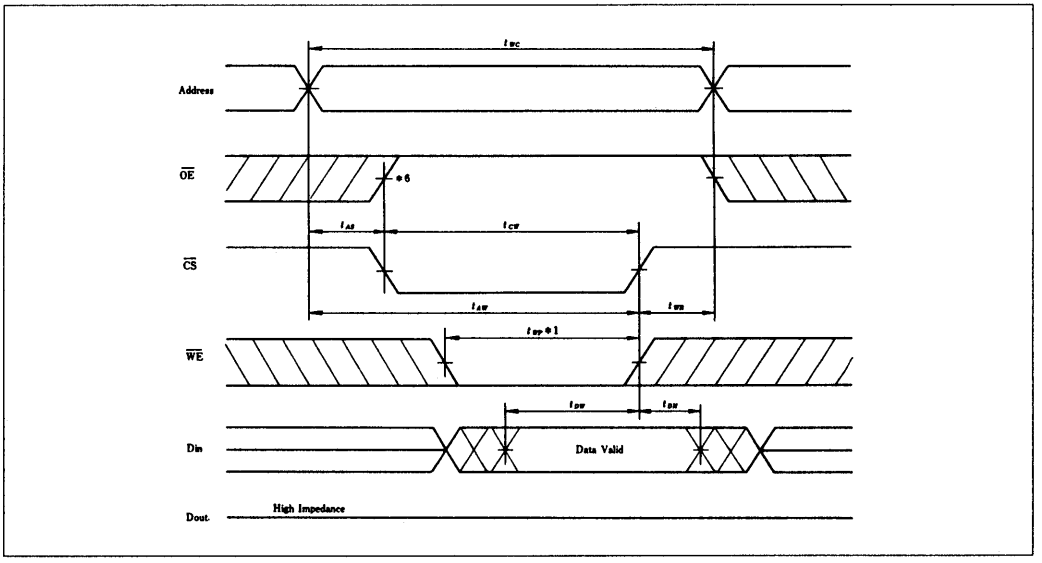
Write Timing Waveform (2) ($\overline{OE}$ = High, $\overline{CS}$ = Controlled)



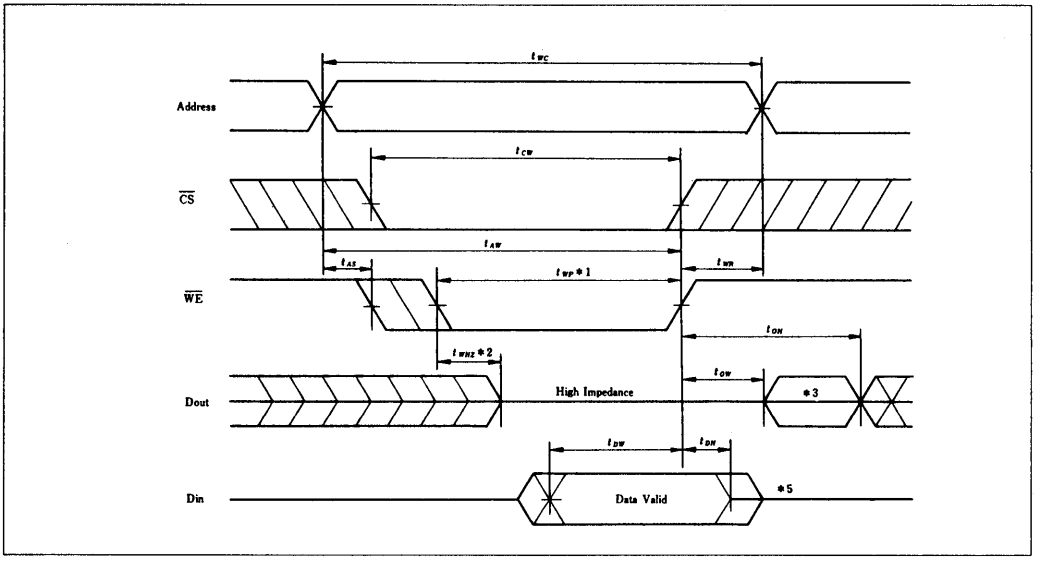
Write Timing Waveform (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ = Controlled)



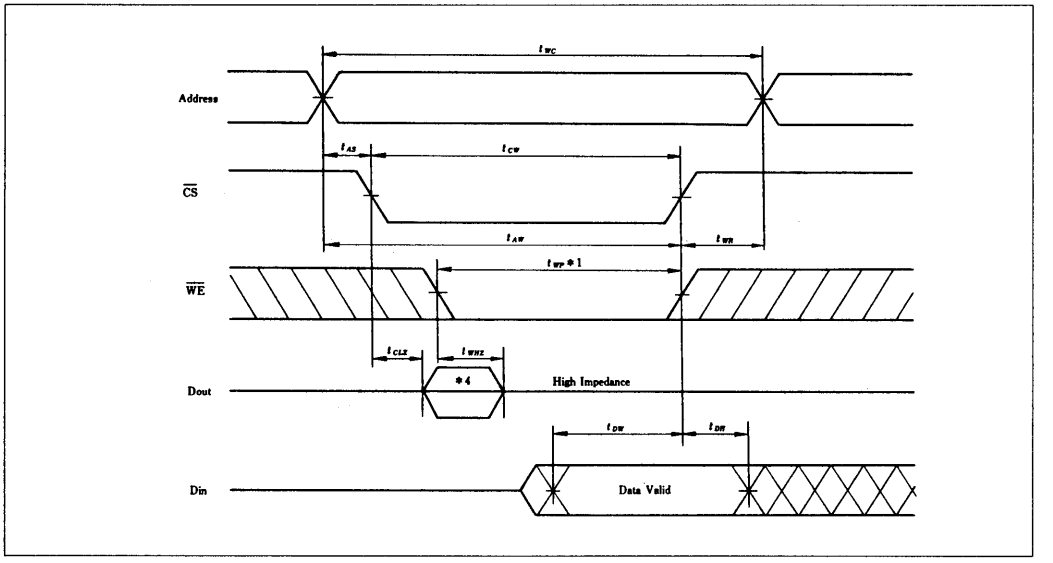
Write Timing Waveform (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ = Controlled)



Write Timing Waveform (5) ($\overline{OE}$ = Low, $\overline{WE}$ = Controlled)



Write Timing Waveform (6) ($\overline{OE}$ = Low, $\overline{CS}$ = Controlled)



Notes: *1 A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (tWP)
*2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after tOW. Then the data input signals of opposite phase to the outputs must not be applied to them.
*6. Dout is the same phase of write data of this write cycle, if tWR is long enough.
*7. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

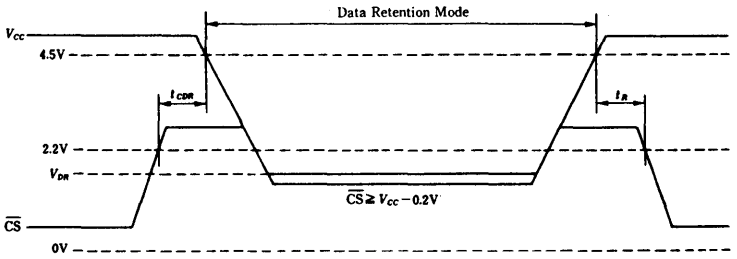
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

This characteristics is guaranteed only for L-version.

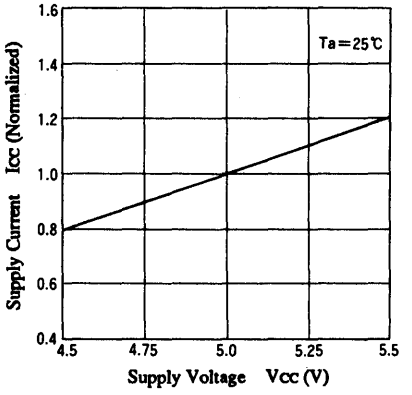
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V,
Data retention current	I_{CCDR}	—	—	50*2	µA	Vin ≥ Vcc – 0.2 V or
				35*3		0 V ≤ Vin ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

Note: *1. t_{RC} = Read cycle time
*2. Vcc = 3.0 V
*3. Vcc = 2.0 V

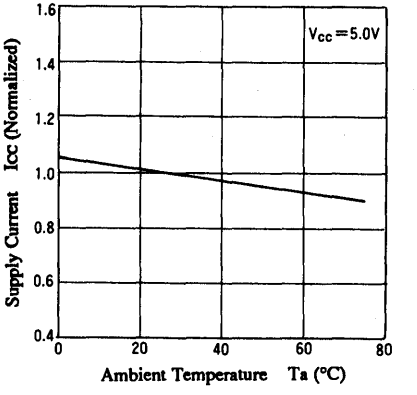
Low Vcc Data Retention Waveform



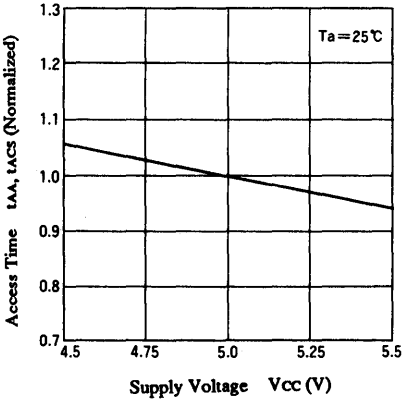
Supply Current vs. Supply Voltage



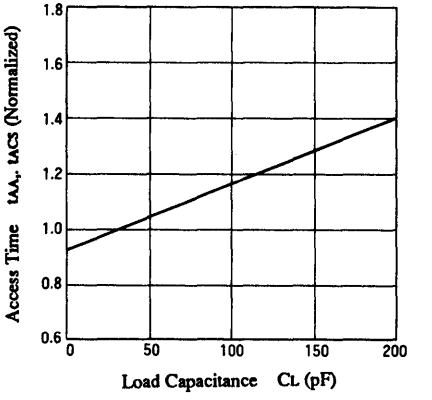
Supply Current vs. Ambient Temperature



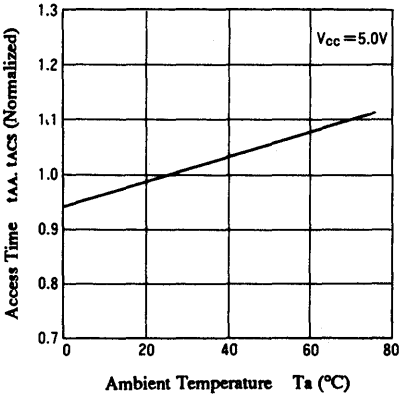
Access Time vs. Supply Voltage



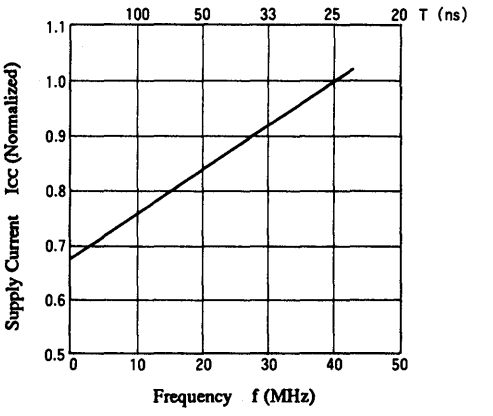
Access Time vs. Load Capacitance



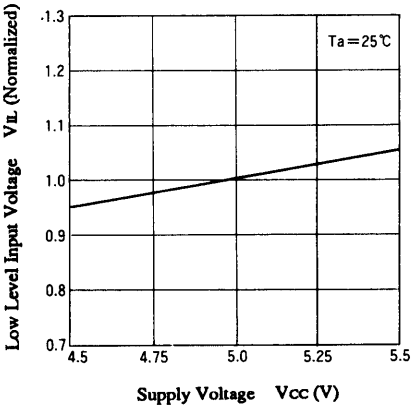
Access Time vs. Ambient Temperature



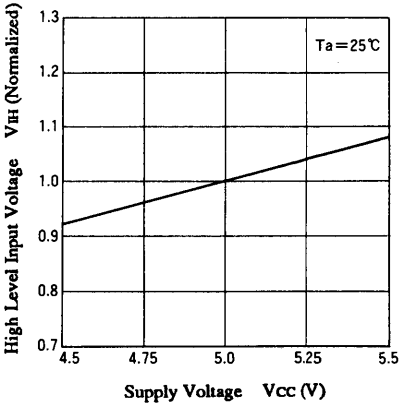
Supply Current vs. Frequency



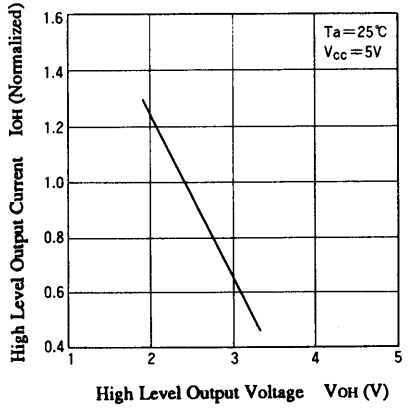
Low Level Input Voltage vs. Supply Voltage



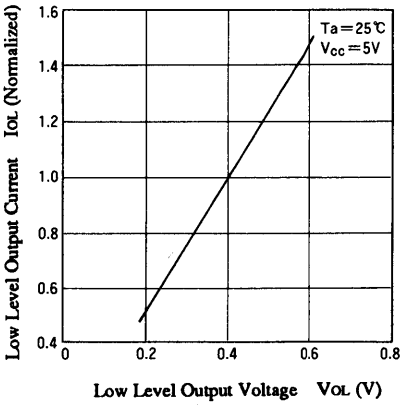
High Level Input Voltage vs. Supply Voltage



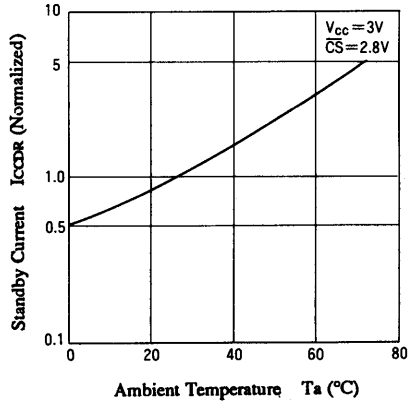
Output Current vs. Output Voltage (1)



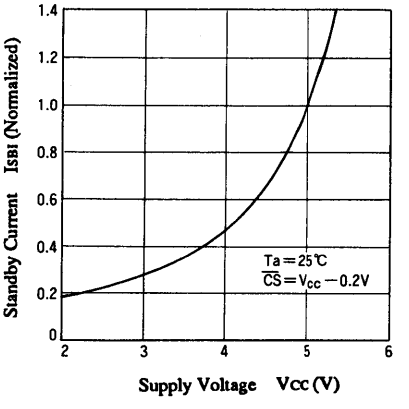
Output Current vs. Output Voltage (2)



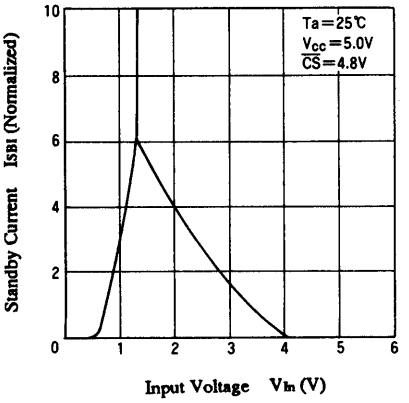
Standby Current vs. Ambient Temperature



Standby Current vs. Supply Voltage



Standby Current vs. Input Voltage



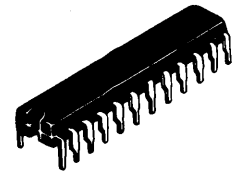
HM6789 Series — Maintenance Only

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)

Features

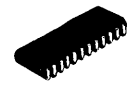
- Super Fast Access Time: . . . . . 25/30 ns (max)
- Low Power Dissipation (DC) Operating . . . . . 230 mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6789P Series



(DP-24NC)

HM6789JP Series

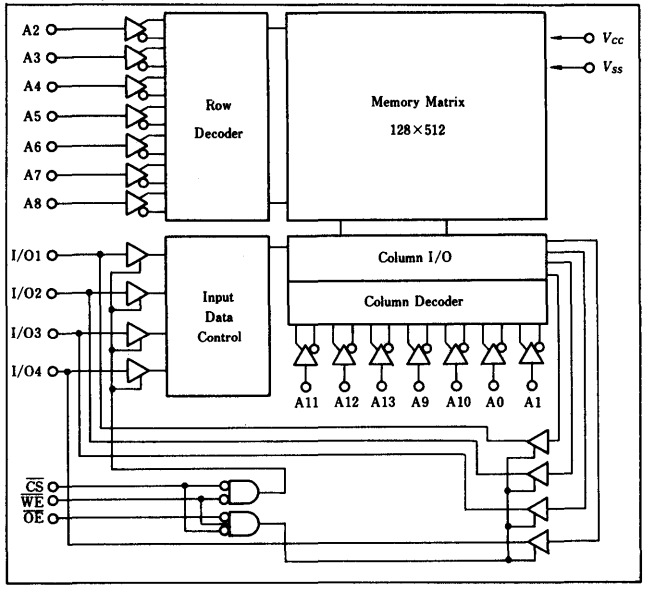


(CP-24D)

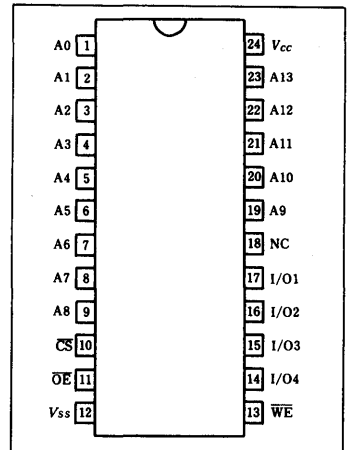
Ordering Information

Type No.	Access Time	Package
HM6789P-25	25ns	300 mil 24 pin
HM6789P-30	30ns	plastic DIP
HM6789JP-25	25ns	300 mil 24 pin
HM6789JP-30	30ns	Plastic SOJ

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range under bias	T_{stg}(bias)	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	–0.5*1	–	0.8	V

Note) *1. –3.0V for pulse width ≦ 20ns.

Function Table

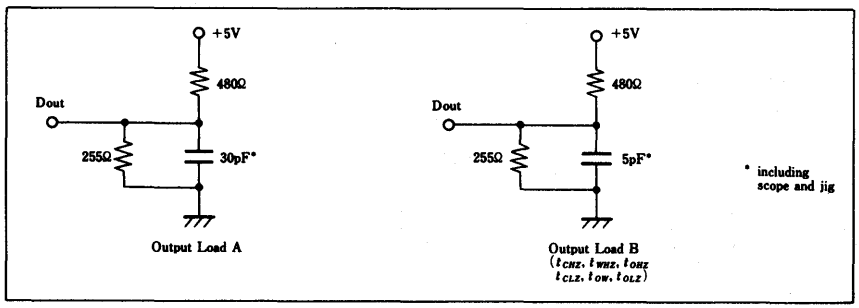
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Din	Write Cycle (5) (6)

DC and Operating Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C)

Item	Symbol	min	typ	max	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min.Cycle, Duty: 100%, $I_{I/O}$=0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	–	–	10	mA	$\overline{CS}$ ≧ V_{CC} – 0.2V V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} – 0.2V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = –4mA

AC Test Conditions

- Input pulse levels ..... V_{SS} to 3.0V
- Input and Output reference levels ..... 1.5 V
- Input rise and fall time ..... 4 ns
- Output Load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	min	typ	max	Unit	Test Conditions
Imput Capacitance	C_{IN}	–	–	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	–	–	8	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C, unless otherwise noted.)

Read Cycle

Item	Symbol	HM6789-25		HM6789-30		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	–	30	–	ns
Address Access Time	t_{AA}	–	25	–	30	ns
Chip Select Access Time	t_{ACS}	–	25	–	30	ns
Chip Selection to Output in Low Z	t_{CLZ}*1	0	–	0	–	ns
Output Enable to Output Valid	t_{OE}	0	15	0	15	ns
Output Enable to Output in Low Z	t_{OLZ}*1	0	–	0	–	ns
Chip Deselection to Output in High Z	t_{CHZ}*1	0	10	0	12	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	ns
Input Voltage Rise/Fall Time	t_T*2	–	150	–	150	ns

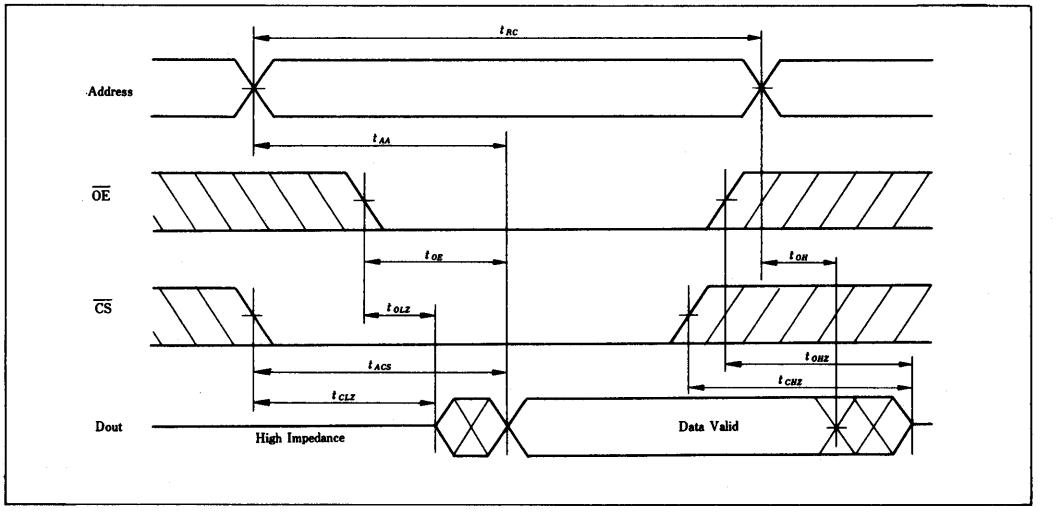
Write Cycle

Item	Symbol	HM6789-25		HM6789-30		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	–	30	–	ns
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	20	–	25	–	ns
Write Pulse Width	t_{WP}	20	–	25	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}*1	0	10	0	12	ns
Data Valid to End of Write	t_{DW}	15	–	20	–	ns
Data Hold Time	t_{DH}	5	–	5	–	ns
Output Disable to Output in Hihg Z	t_{OHZ}*1	0	10	0	10	ns
Output Active from End of Write	t_{OW}*1	0	–	0	–	ns

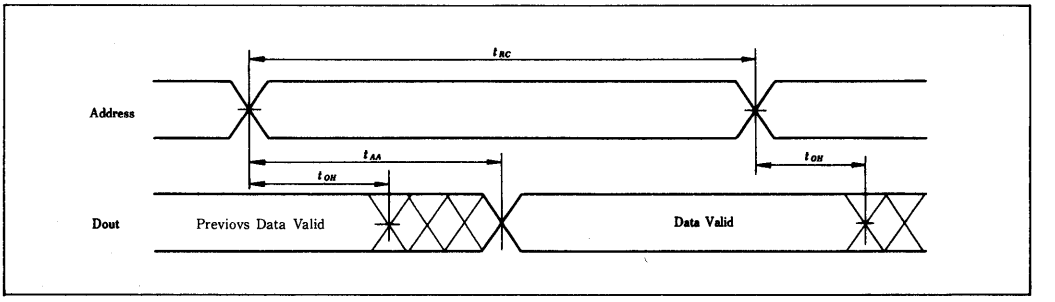
Notes) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.
*2. If t_T becomes more than 150ns, there is possibility of function fail.
Please contact your nearest Hitachi Sales Dept. regarding specification.

Timing Waveform

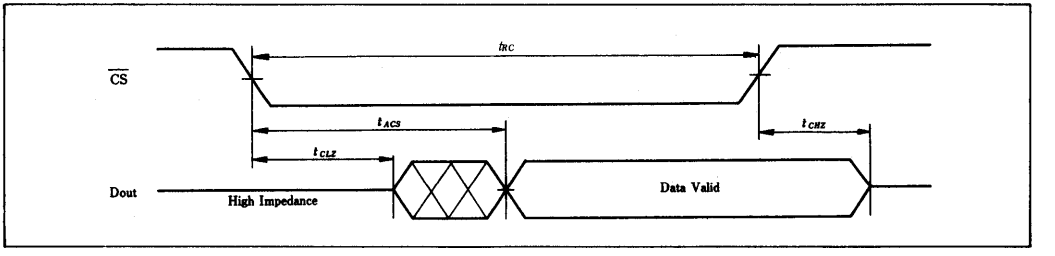
Read Cycle (1) *1



Read Cycle (2) *1, *2, *3

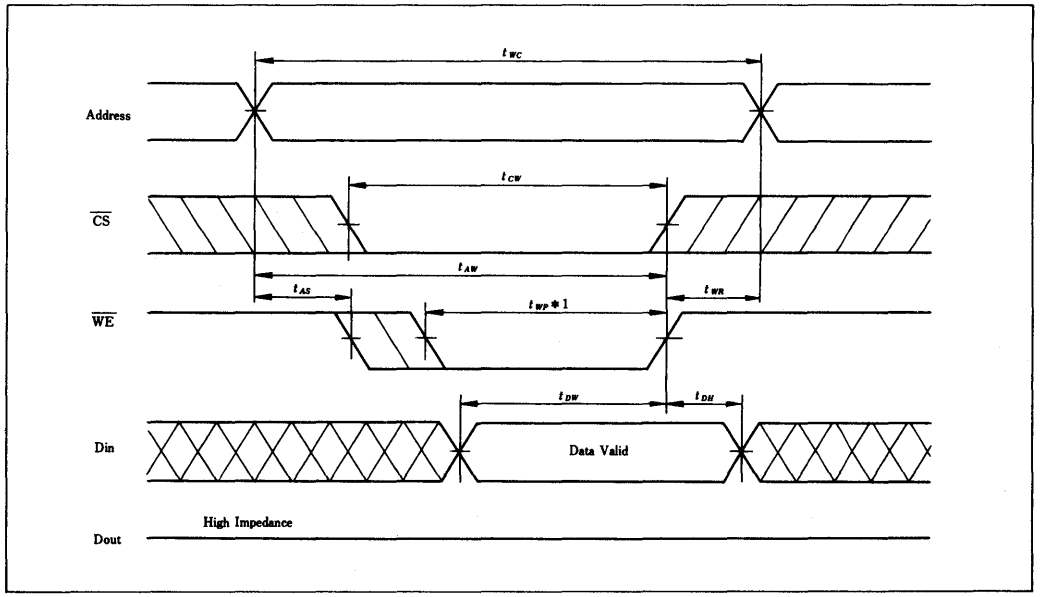


Read Cycle (3) *1, *3, *4

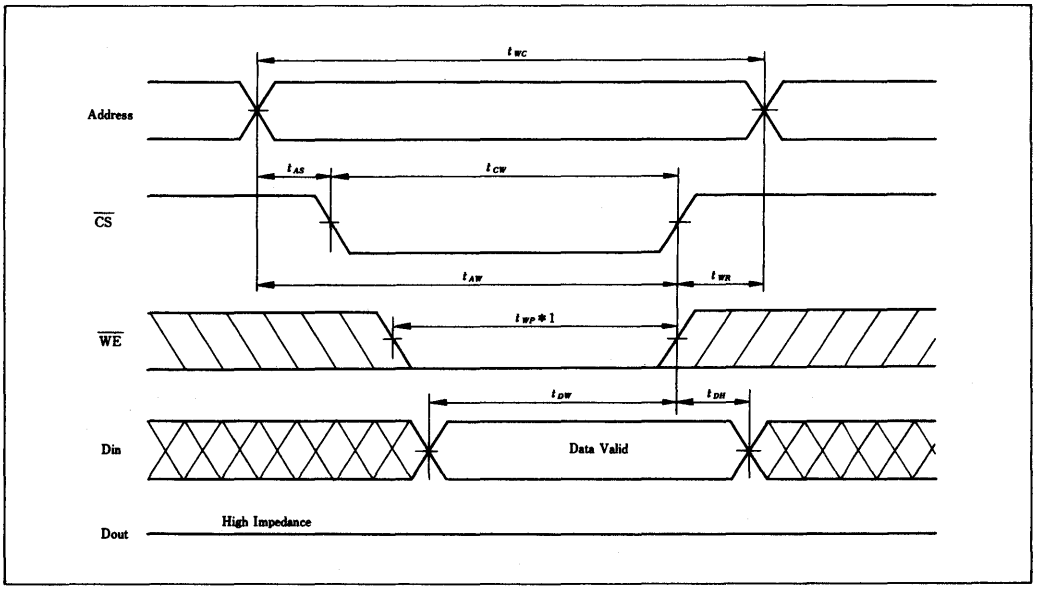


Notes) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. $\overline{OE} = V_{IL}$
*4. Address valid prior to or coincident with $\overline{CS}$ transition Low.

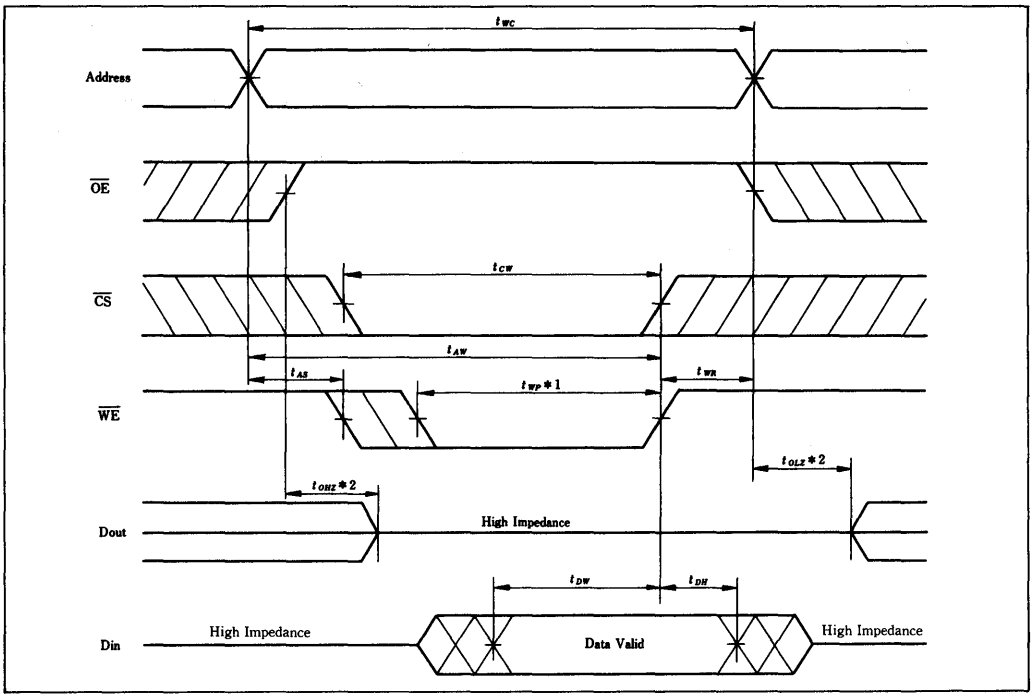
Write Cycle (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



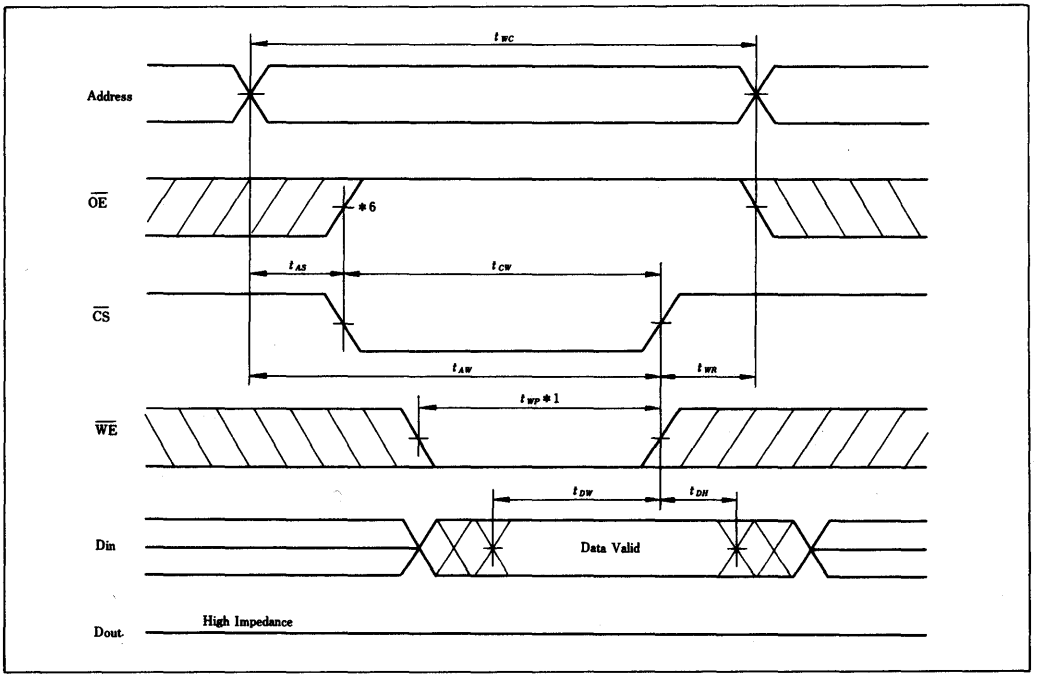
Write Cycle (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



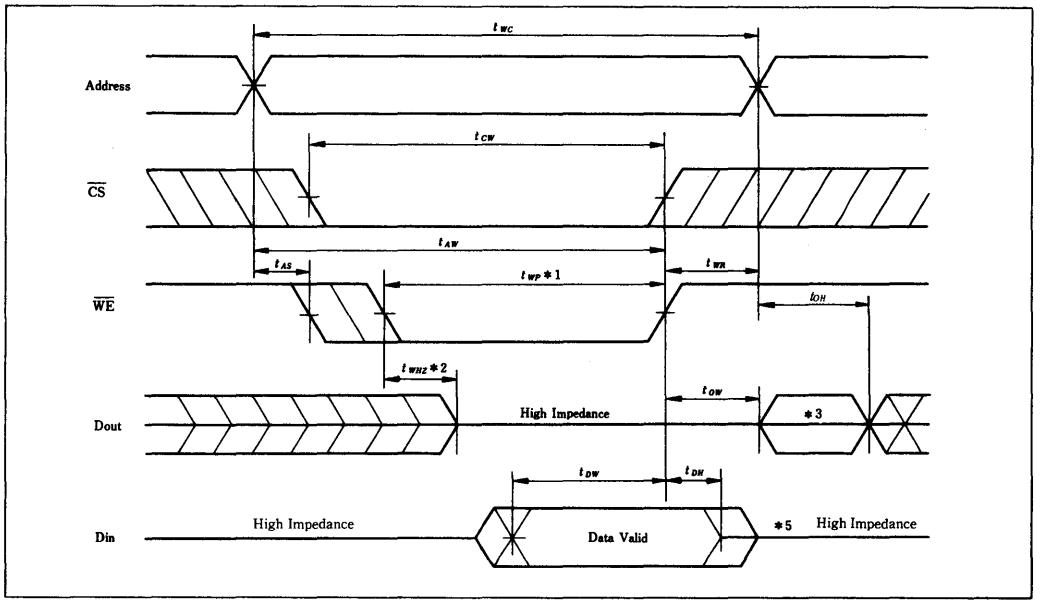
Write Cycle (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



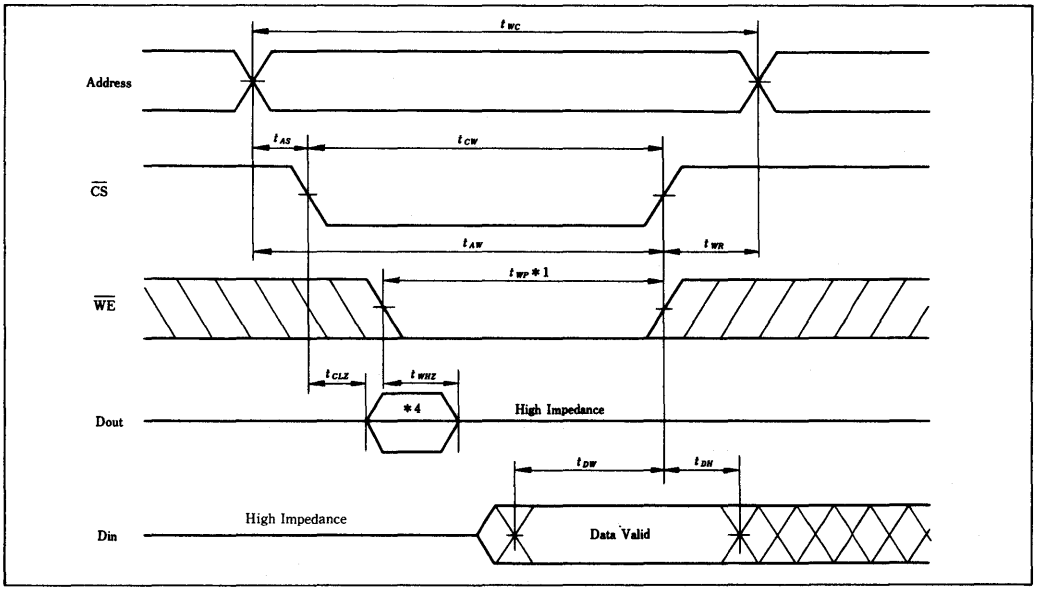
Write Cycle (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



Write Cycle (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Write Cycle (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*3. Dout is the same phase of write data of this write cycle.

*4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.

*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

*6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

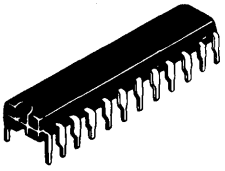
HM6789H Series

16384-word x 4-bit High Speed Hi-BiCMOS Static RAM (with $\overline{OE}$)

Features

- Super Fast Access Time: . . . . . 15/20 ns (max)
- Low Power Dissipation (DC) Operating . . . . . 280 mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6789HP Series



(DP-24NC)

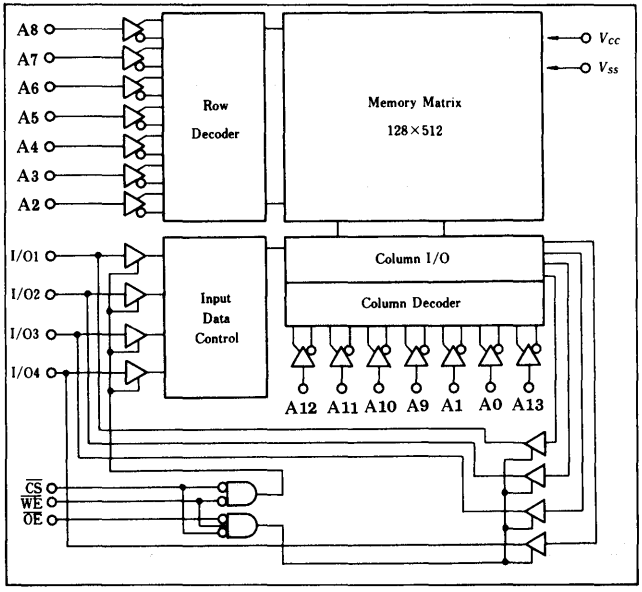
HM6789HJP Series

(CP-24D)

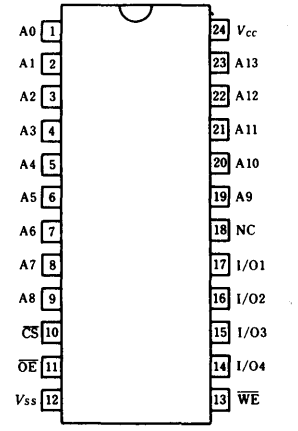
Ordering Information

Type No.	Access Time	Package
HM6789HP-15	15ns	300 mil 24 pin
HM6789HP-20	20ns	plastic DIP
HM6789HJP-15	15ns	300 mil
HM6789HJP-20	20ns	24 pin plastic SOJ

Block Diagram



Pin Arrangement



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range under bias	T_{stg}(bias)	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Note) The specifications of this device are subject to change without notice.
Please contact Hitachi's Sales Dept. regarding specifications.

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 10ns.

Function Table

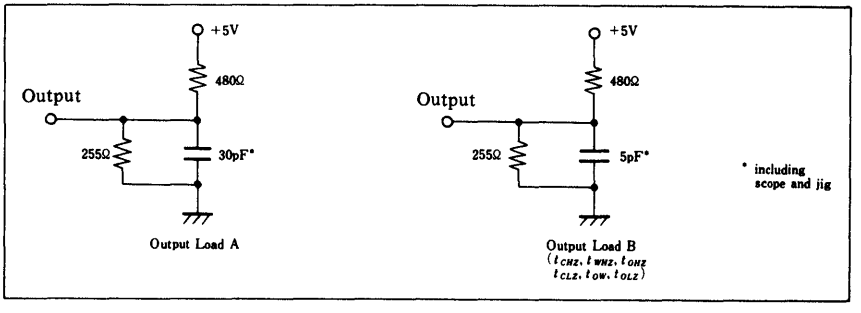
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	–
L	L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data Out	Write Cycle (5) (6)

DC and Operating Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C)

Item	Symbol	min	typ	max	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min.Cycle, Duty: 100%, $I_{I/O}$=0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}
	I_{SB1}	–	–	10	mA	$\overline{CS}$ ≧ V_{CC} − 0.2V, V_{IN} ≦ 0.2V or V_{IN} ≧ V_{CC} − 0.2V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4mA

AC Test Conditions

- Input pulse levels ..... V_{SS} to 3.0V
- Input and Output reference levels ..... 1.5 V
- Input rise and fall time ..... 4 ns
- Output Load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	min	typ	max	Unit	Test Conditions
Imput Capacitance	C_{IN}	–	–	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$	–	–	10	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC}=5V±10%, T_a=0 to +70°C, unless otherwise noted.)

Read Cycle

Item	Symbol	HM6789H-15		HM6789H-20		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	15	–	20	–	ns
Address Access Time	t_{AA}	–	15	–	20	ns
Chip Select Access Time	t_{ACS}	–	15	–	20	ns
Chip Selection to Output in Low Z	t_{CLZ}*1	3	–	3	–	ns
Output Enable to Output Valid	t_{OE}	0	12	0	12	ns
Output Enable to Output in Low Z	t_{OLZ}*1	3	–	3	–	ns
Chip Deselection to Output in High Z	t_{CHZ}*1	0	6	0	8	ns
Output Hold from Address Change	t_{OH}	3	–	3	–	ns

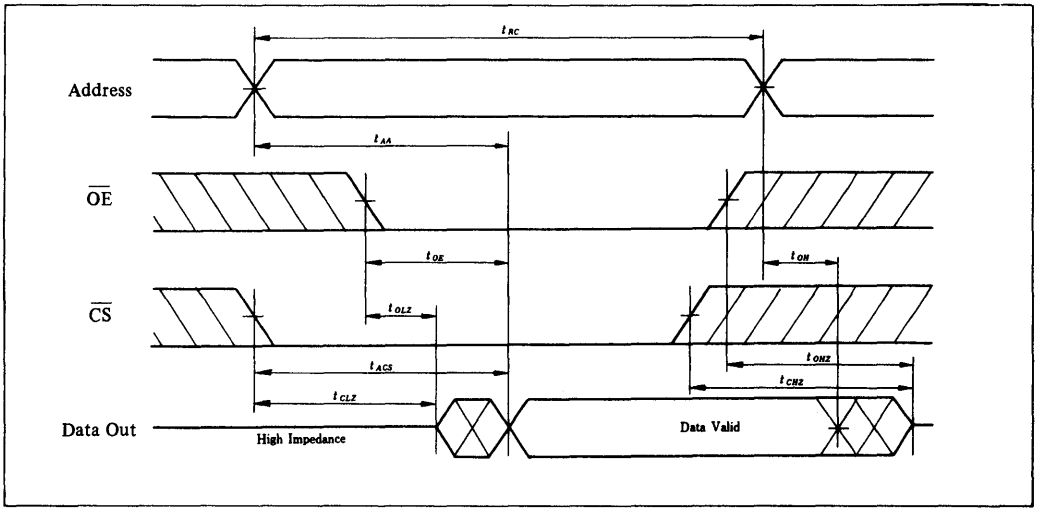
Write Cycle

Item	Symbol	HM6789H-15		HM6789H-20		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	15	–	20	–	ns
Chip Selection to End of Write	t_{CW}	10	–	15	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Address Valid to End of Write	t_{AW}	10	–	15	–	ns
Write Pulse Width	t_{WP}	10	–	15	–	ns
Write Recovery Time	t_{WR}	1	–	1	–	ns
Write to Output in High Z	t_{WHZ}*1	0	6	0	8	ns
Data Valid to End of Write	t_{DW}	9	–	10	–	ns
Data Hold Time	t_{DH}	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}*1	0	6	0	8	ns
Output Active from End of Write	t_{OW}*1	0	–	0	–	ns

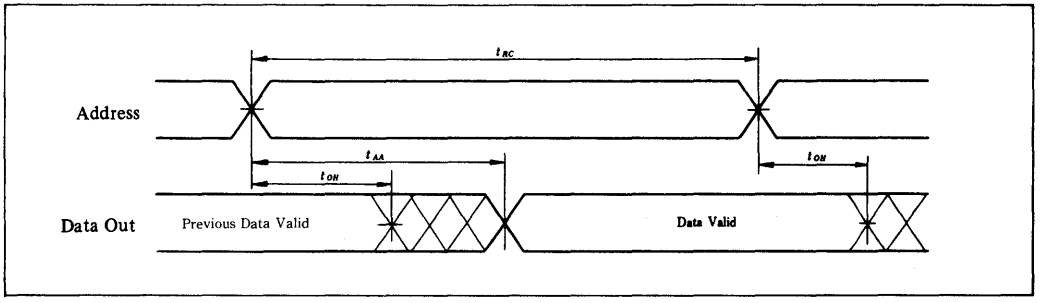
Note) *1. Transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Timing Waveform

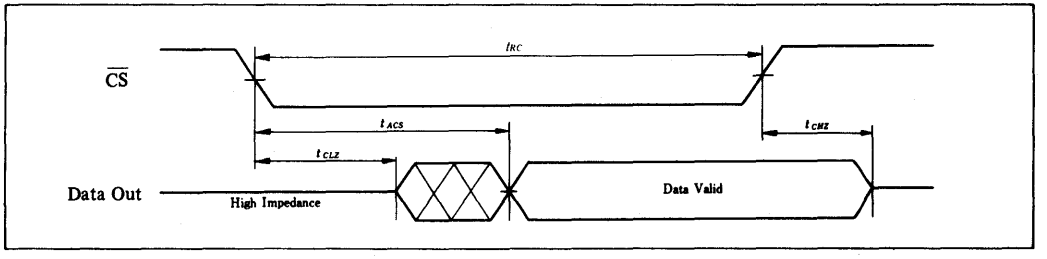
Read Cycle (1) *1



Read Cycle (2) *1, *2, *3

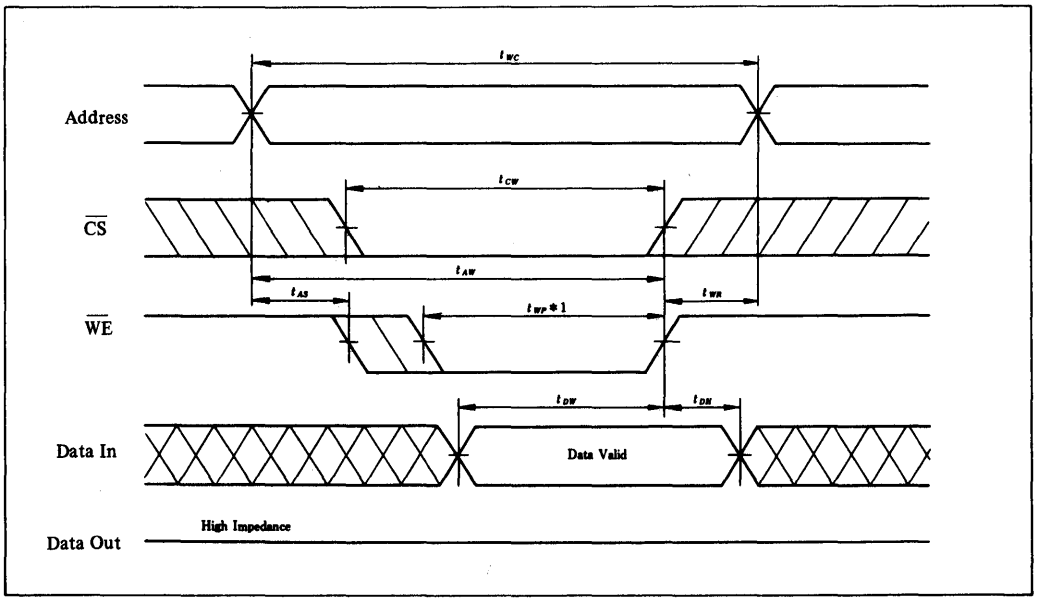


Read Cycle (3) *1, *3, *4

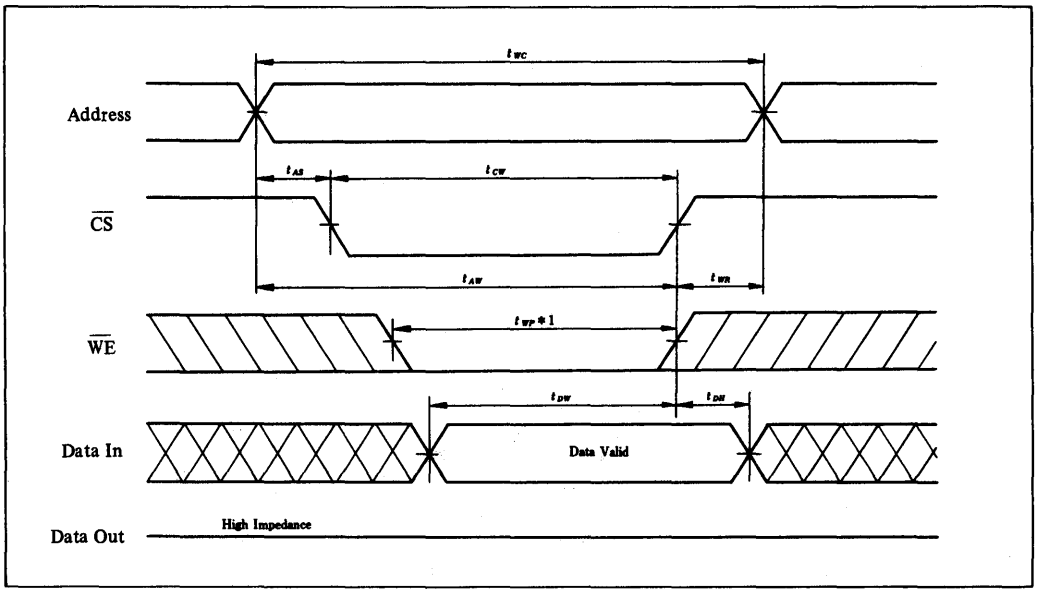


Notes) *1. $\overline{WE} = V_{IH}$
*2. $\overline{CS} = V_{IL}$
*3. $\overline{OE} = V_{IL}$
*4. Address valid prior to or coincident with $\overline{CS}$ transition Low.

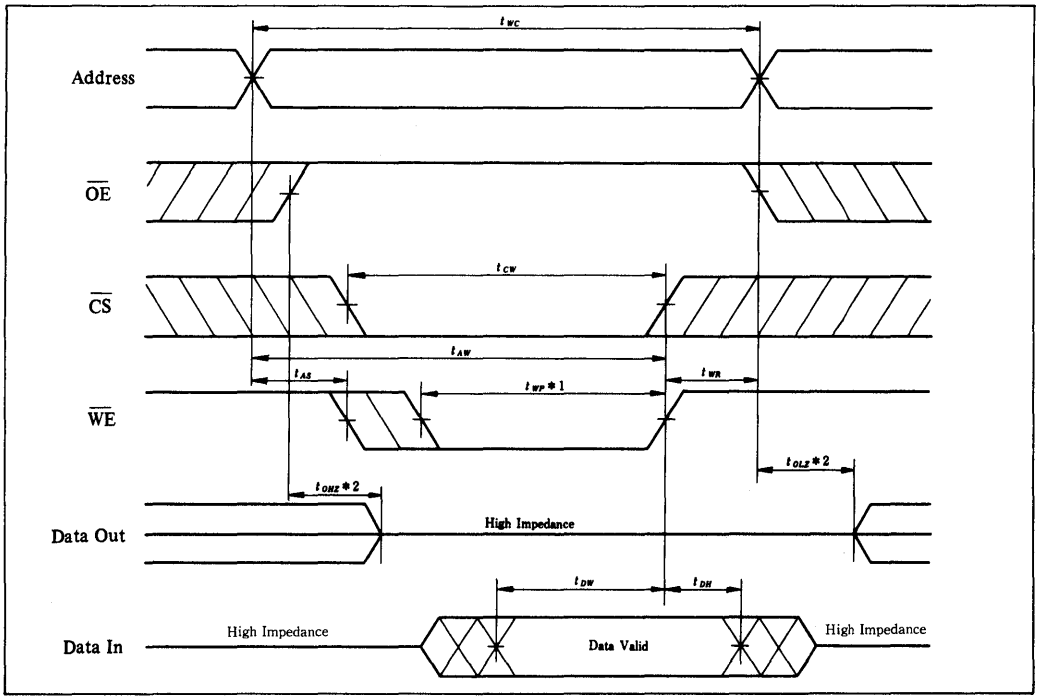
Write Cycle (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



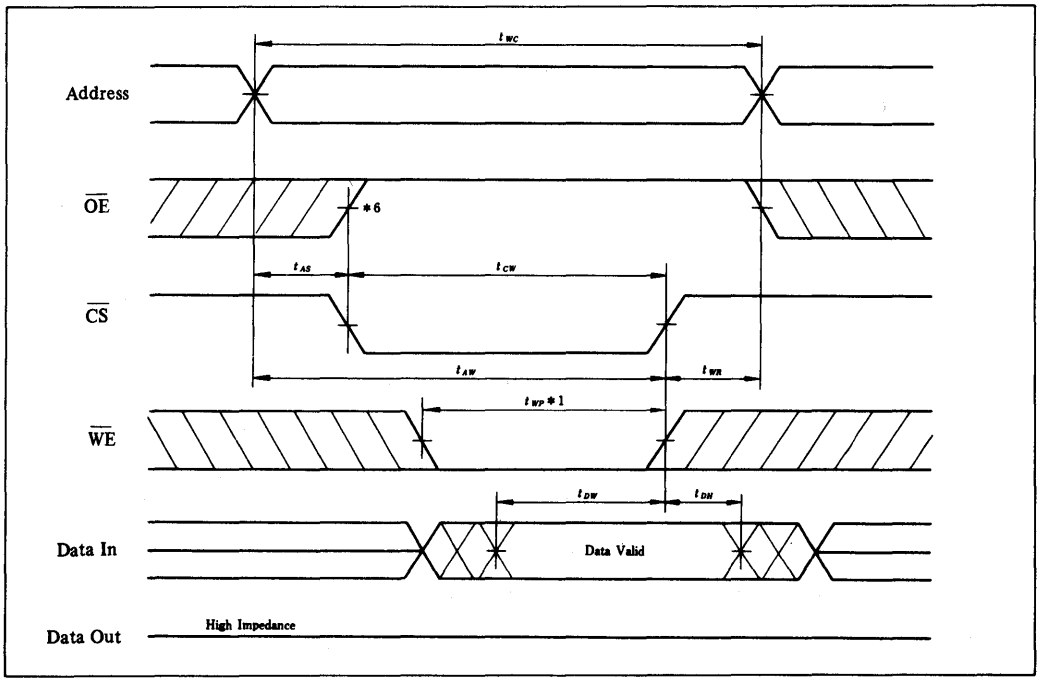
Write Cycle (2) ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



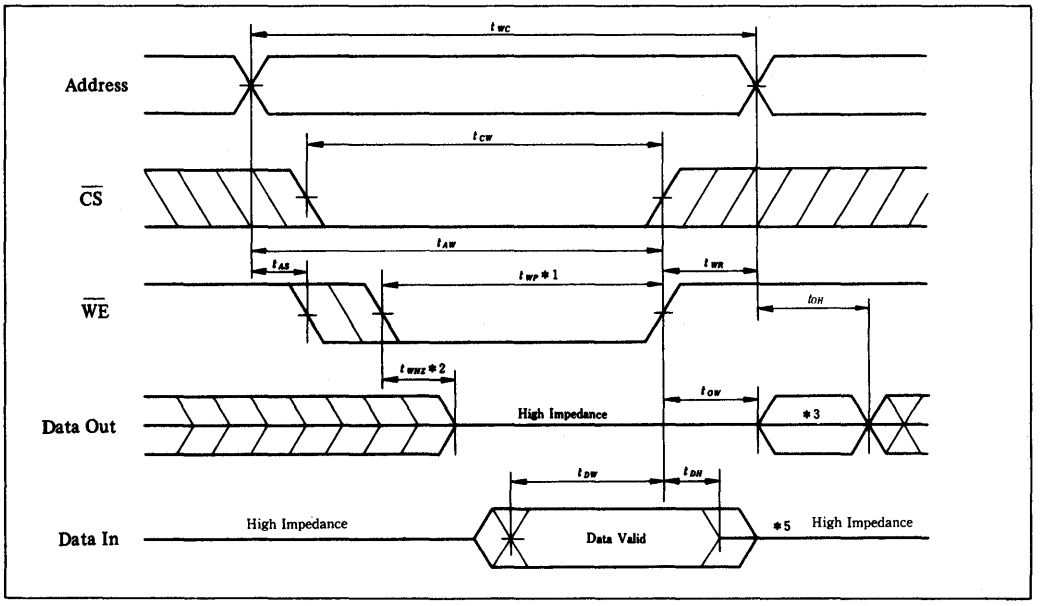
Write Cycle (3) ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



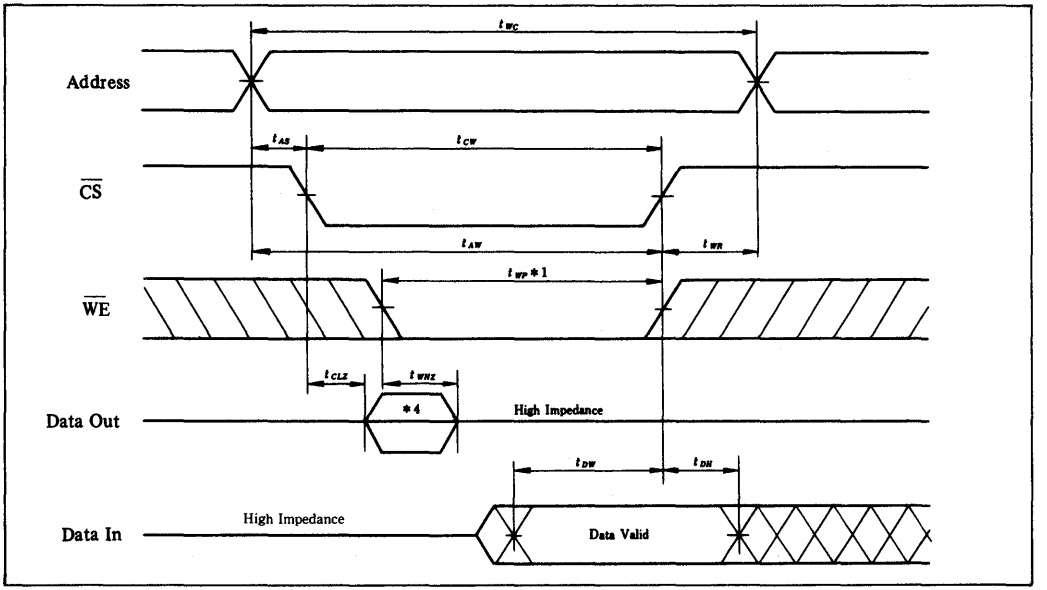
Write Cycle (4) ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



Write Cycle (5) ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Write Cycle (6) ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*3. Data Out is the same phase of write data of this write cycle.
*4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
*6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

HM6789HA Series — Preliminary

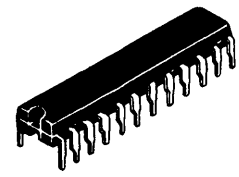
16384-Word × 4-Bit High Speed Static RAM (with $\overline{OE}$)

■ FEATURES

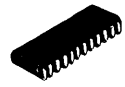
- Super Fast
  Access Time .....Add. 12/15/20ns (max.)
  $\overline{OE}$ 6/7/8ns (max.)
- Low Power Dissipation
  (DC) Operating .....300mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6789HAP-12	12ns	300 mil 24 pin
HM6789HAP-15	15ns	Plastic DIP
HM6789HAP-20	20ns	(DP-24NC)
HM6789HAJP-12	12ns	300 mil 24 pin
HM6789HAJP-15	15ns	Plastic SOJ
HM6789HAJP-20	20ns	(CP-24D)

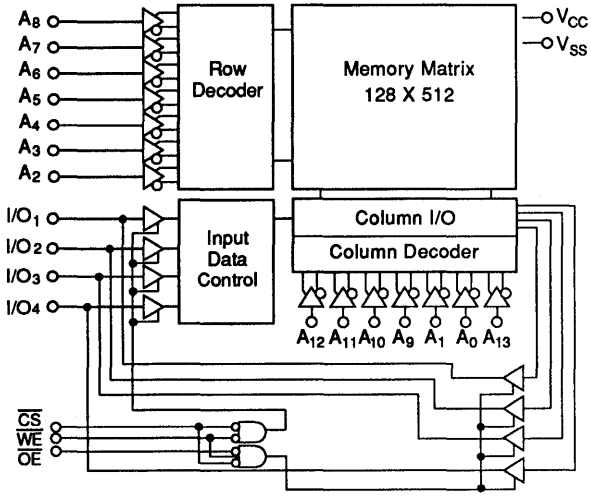


(DP-24NC)

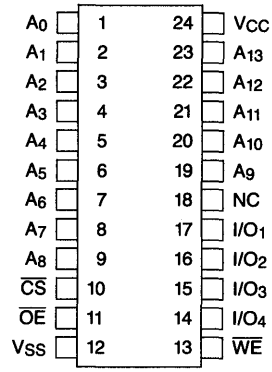


(CP-24D)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_a \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}*	−3.0	—	0.8	V

*Pulse width ≤ 10ns, DC: −0.5V

■ TRUTH TABLE

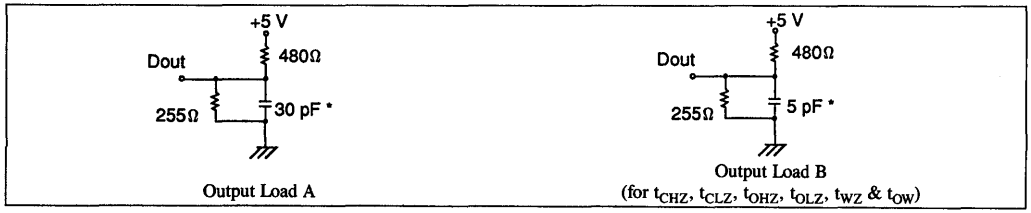
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	—
L	L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data In	Write Cycle (5) (6)

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, V_{SS} = 0V)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL} $V_{I/O}$ = V_{SS} to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$, = 0mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O}$ = 0mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	—	—	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} − 0.2V	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Reference Levels: 1.5V ± 200mV from steady level (Output Load B)
- Input Rise and Fall Time: 4ns
- Output Load: See Figure



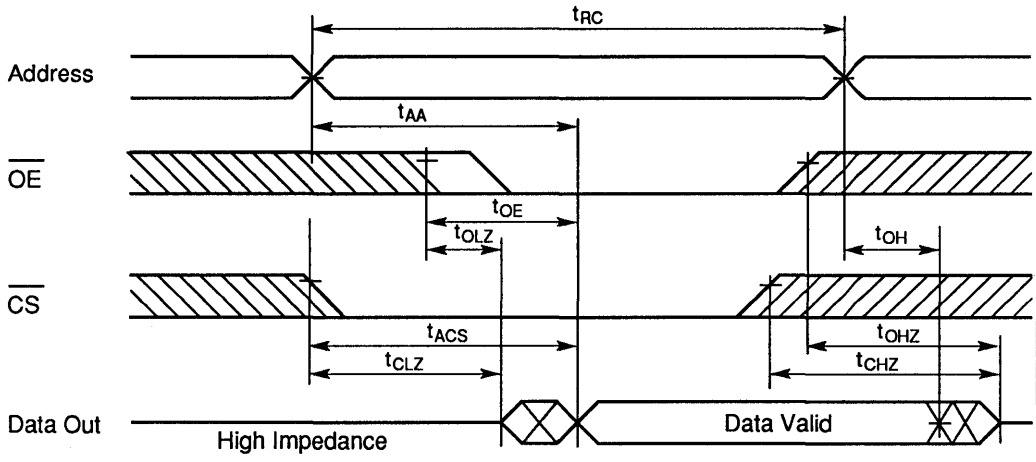
Output Load A

Output Load B
(for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WZ} & t_{OW})

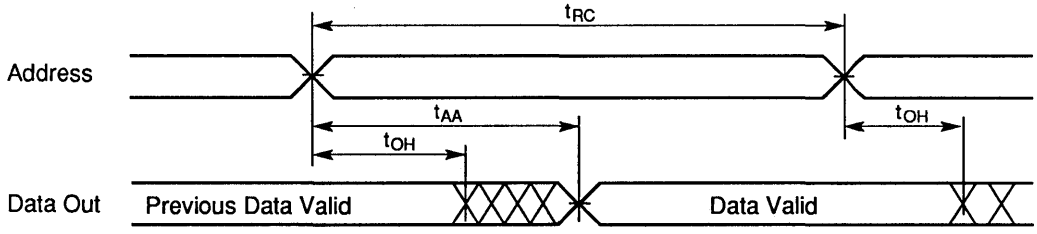
*Including scope and jig capacitance.

■ TIMING WAVEFORM

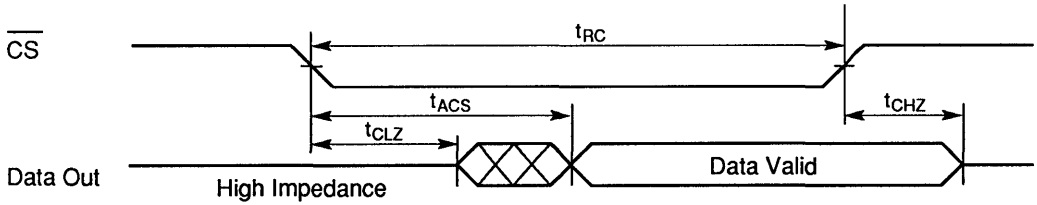
• **Read Cycle (1)** (1)



• **Read Cycle (2)** (1) (2) (3)



• **Read Cycle (3)** (1) (3) (4)



NOTES: 1. $\overline{WE}$ = V_{IH}
2. $\overline{CS}$ = V_{IL}
3. $\overline{OE}$ = V_{IL}
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

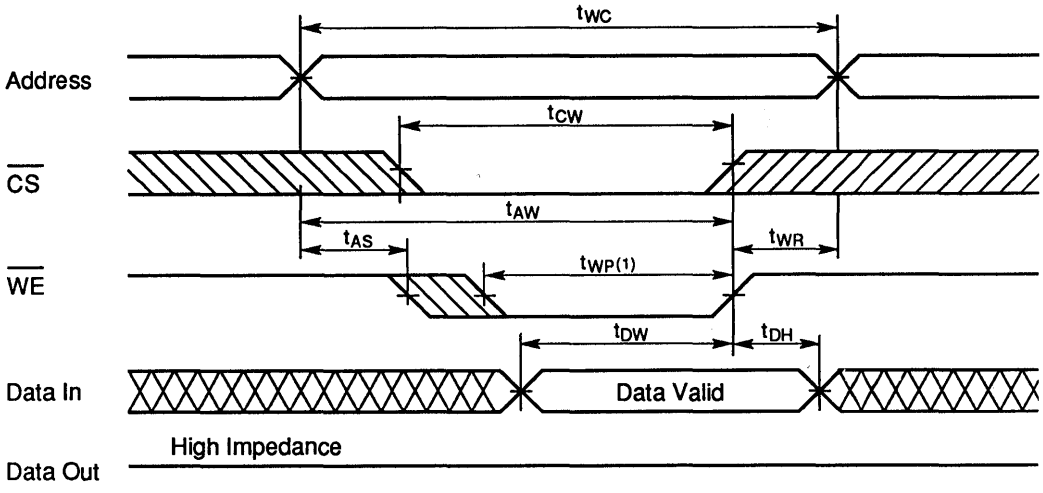
Item	Symbol	HM6789HA-12		HM6789HA-15		HM6789HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	12	—	15	—	20	—	ns	—
Address Access Time	t_{AA}	—	12	—	15	—	20	ns	—
Chip Select Access Time	t_{ACS}	—	12	—	15	—	20	ns	—
Chip Selection to Output in Low Z	t_{CLZ}	3	—	5	—	5	—	ns	1, 2
Output Enable to Output Valid	t_{OE}	0	6	0	7	0	8	ns	1
Output Enable to Output in Low Z	t_{OLZ}	2	—	2	—	2	—	ns	1, 2
Chip Deselection to Output in High Z	t_{CHZ}	0	6	0	6	0	8	ns	1, 2
Output Hold from Address Change	t_{OH}	4	—	4	—	4	—	ns	—

• Write Cycle

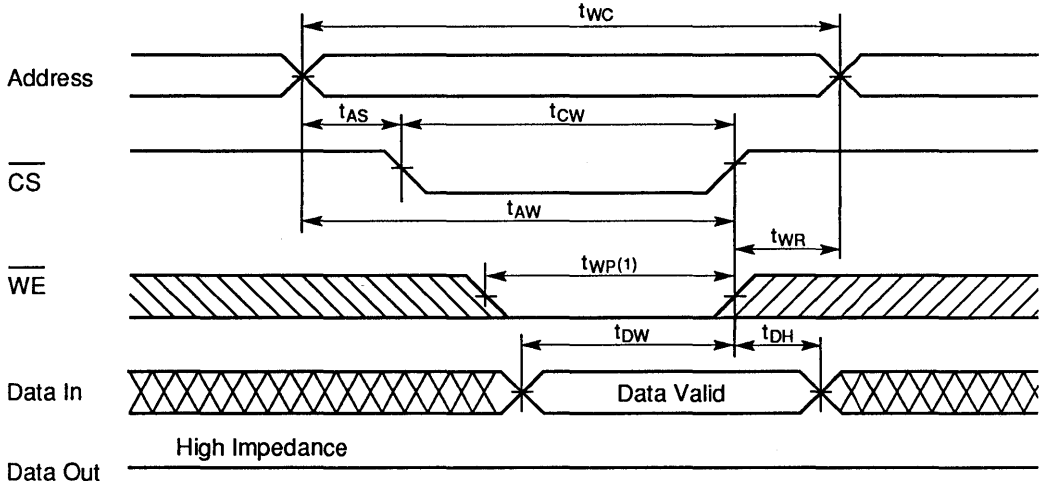
Item	Symbol	HM6789HA-12		HM6789HA-15		HM6789HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	12	—	15	—	20	—	ns	—
Chip Selection to End of Write	t_{CW}	8	—	10	—	15	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Address Valid to End of Write	t_{AW}	8	—	10	—	15	—	ns	—
Write Pulse Width	t_{WP}	8	—	10	—	15	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Write to Output in High Z	t_{WHZ}	0	6	0	6	0	8	ns	1, 2
Data Valid to End of Write	t_{DW}	6	—	7	—	10	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Output Disable to Output in High Z	t_{OHZ}	1	6	1	6	1	8	ns	1, 2
Output Active from End of Write	t_{OW}	3	—	3	—	3	—	ns	1, 2

NOTES: 1. Transition is measured ±200mV from steady state voltage with Load B.
2. This parameter is sampled and not 100% tested.

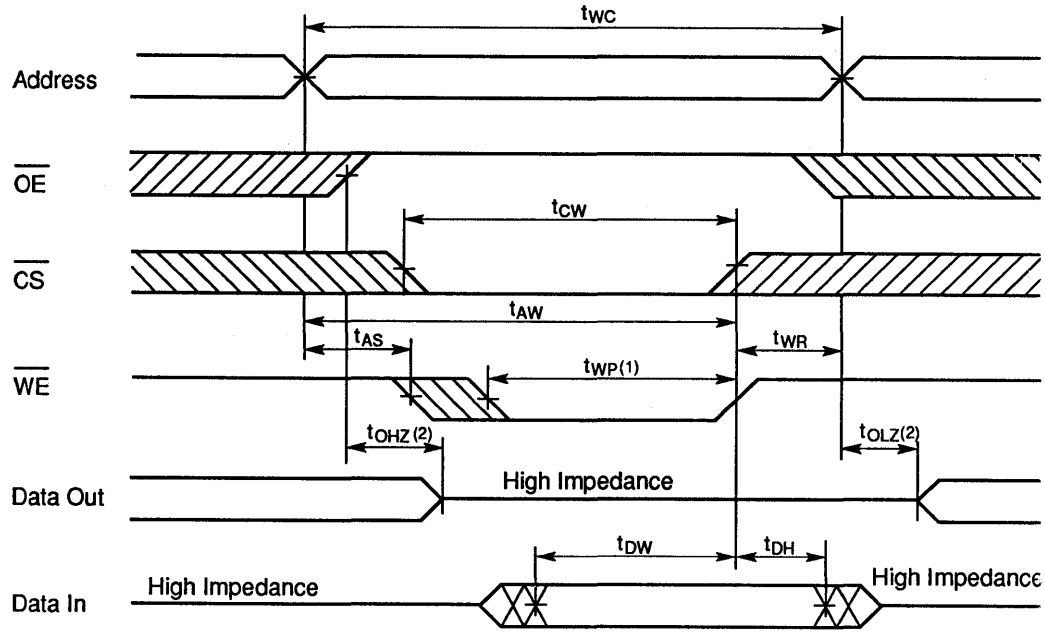
• **Write Cycle (1)** ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



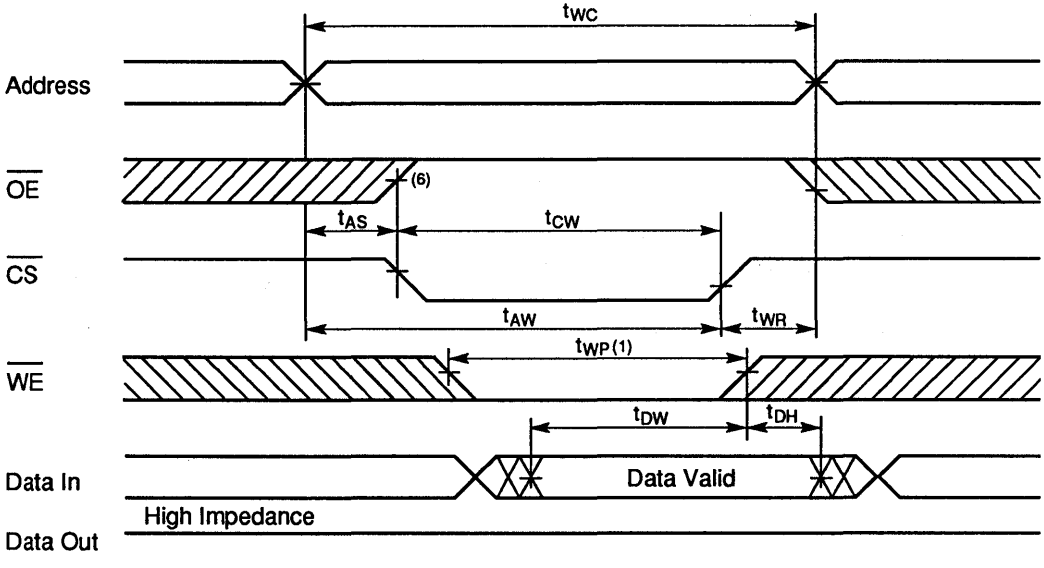
• **Write Cycle (2)** ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



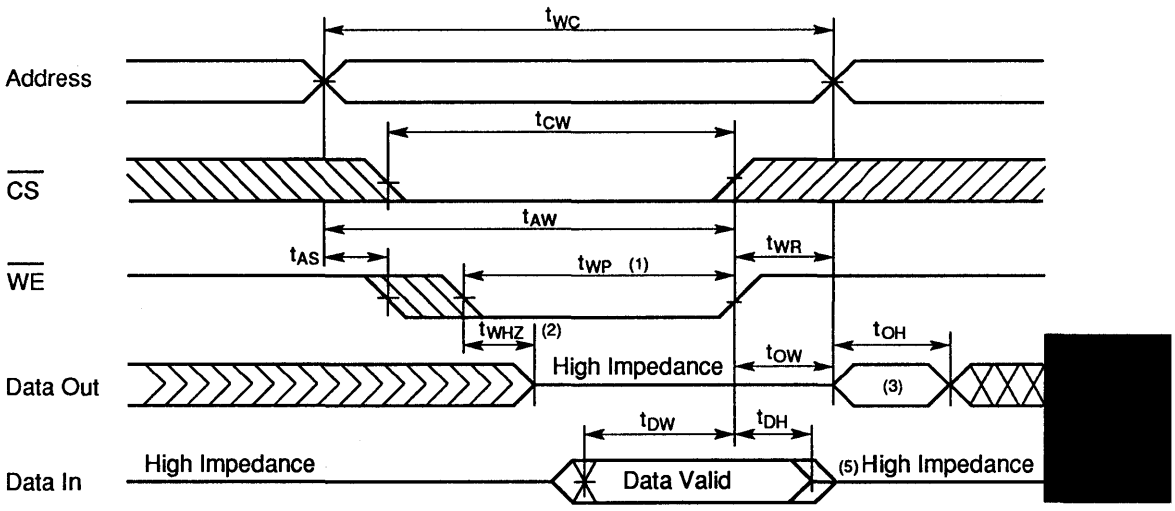
• **Write Cycle (3)** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



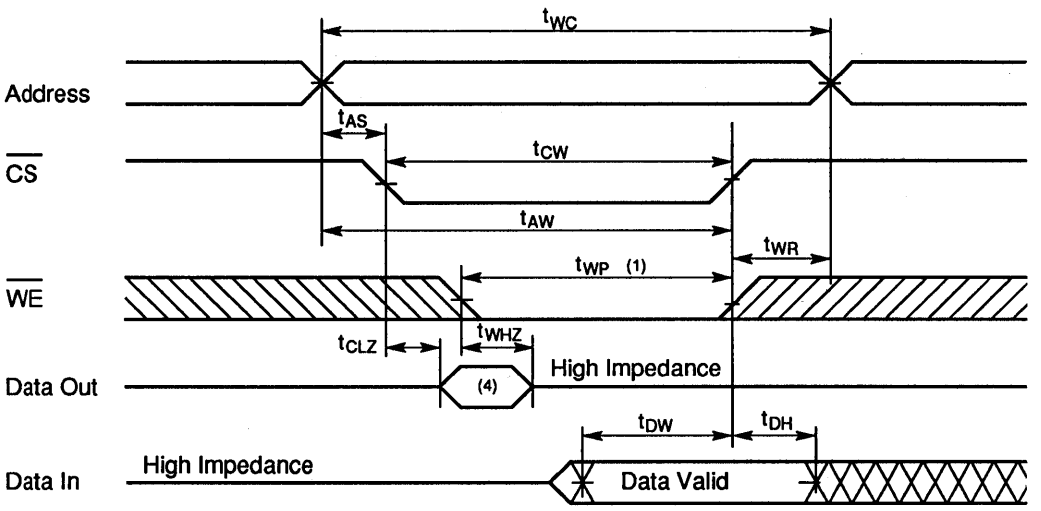
• **Write Cycle (4)** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



• **Write Cycle (5)** ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



• **Write Cycle (6)** ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



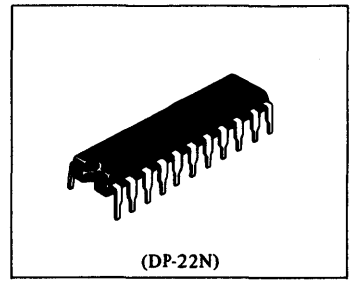
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. D_{out} is the same phase of write data of this write cycle.
4. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

HM6287 Series — Maintenance Only

65536-word x 1-bit High Speed CMOS Static RAM

■ FEATURES

- High Speed: Fast Access Time 45/55/70ns (max.)
- Single 5V Supply and High Density 22 Pin Package
- Low Power Standby and Low Power Operation
  Standby: 100μW (typ.)/10μW (typ.) (L-version)
  Operation: 300mW (typ.)
- Completely Static Memory
  No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible: All Inputs and Output
- Capability of Battery Back Up Operation (L-version)

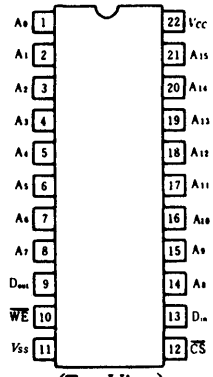


(DP-22N)

■ ORDERING INFORMATION

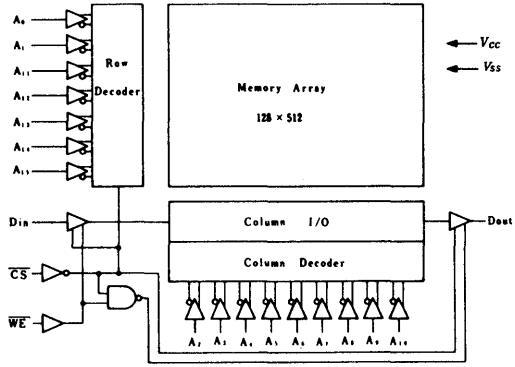
Type No.	Access Time	Package
HM6287P-45	45ns	300 mil 22 pin Plastic DIP
HM6287P-55	55ns	
HM6287P-70	70ns	
HM6287LP-45	45ns	
HM6287LP-55	55ns	
HM6287LP-70	70ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



NOTE: Not for new designs.

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High Z	Write Cycle

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.5V for pulse width ≦ 20ns

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 20ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item	Symbol	Test Conditions	min	typ*1	max	Unit
Input Leakage Current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5V, V_{in} = V_{SS} to V_{CC}	–	–	2.0	μA
Output Leakage Current	$\lvert I_{LO} \rvert$	$\overline{CS}$ = V_{IH}, V_{out} = V_{SS} to V_{CC}	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{out} = 0mA, min. cycle	–	60	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, min. cycle	–	10	30	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V,	–	0.02	2.0	mA
		0V ≦ V_{in} ≦ 0.2V or V_{CC} − 0.2V ≦ V_{in}	–	2*2	100*2	μA
Output Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	V
	V_{OH}	I_{OH} = −4.0mA	2.4	–	–	V

Notes) *1. Typical limits are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (f = 1MHz, T_a = 25°C)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	–	5	pF
Output Capacitance	C_{out}	V_{out} = 0V	–	–	7.5	pF

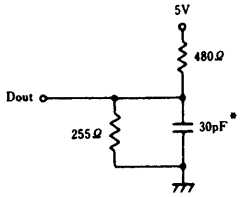
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ±10%, T_a = 0 to +70°C, unless otherwise noted)

• AC TEST CONDITIONS

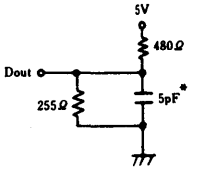
Input Pulse Levels: V_{SS} to 3.0V
Input Rise and Fall Times: 5ns
Input and Output Timing Reference Levels: 1.5V
Output Load: See Figure

Output Load A



*Including scope & jig capacitance

Output Load B

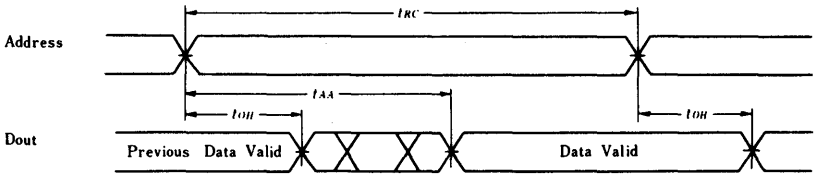


*Including scope & jig capacitance

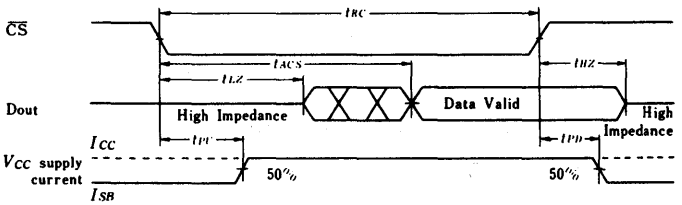
• READ CYCLE

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	45	–	55	–	70	–	ns	1
Address Access Time	t_{AA}	–	45	–	55	–	70	ns	
Chip Select Access Time	t_{ACS}	–	45	–	55	–	70	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	5	–	ns	2, 3, 7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	0	–	ns	7
Chip Deselection to Power Down Time	t_{PD}	–	40	–	40	–	40	ns	7

• Timing Waveform of Read Cycle No. 1[4][5]



• Timing Waveform of Read Cycle No. 2[4][6]

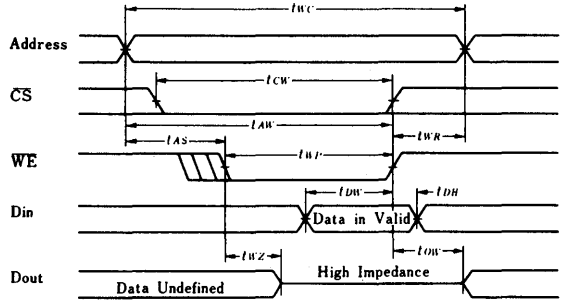


Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Load B.
4. $\overline{WE}$ is high for READ Cycle.
5. Device is continuously selected, while $\overline{CS} = V_{IL}$.
6. Address valid prior to or coincident with $\overline{CS}$ transition low.
7. This parameter is sampled and not 100% tested.

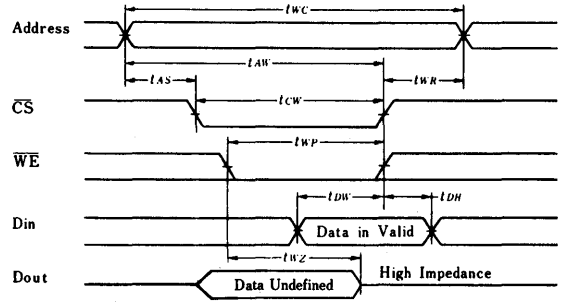
• WRITE CYCLE

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	45	–	55	–	70	–	ns	2
Chip Selection to End of Write	t_{CW}	40	–	50	–	55	–	ns	
Address Valid to End of Write	t_{AW}	40	–	50	–	55	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	35	–	40	–	ns	
Write Recovery Time	t_{WR}	0	–	0	–	0	–	ns	
Data Valid to End of Write	t_{DW}	25	–	25	–	30	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	0	–	ns	
Write Enabled to Output in High Z	t_{WZ}	0	25	0	25	0	30	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	0	–	ns	3, 4

• Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



• Timing Waveform of Write Cycle No. 1 ($\overline{CS}$ Controlled)



Notes) 1. If $\overline{CS}$ goes high Simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

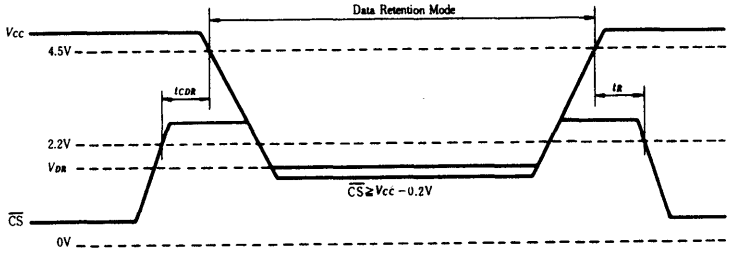
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

This characteristics is guaranteed only for L-version.

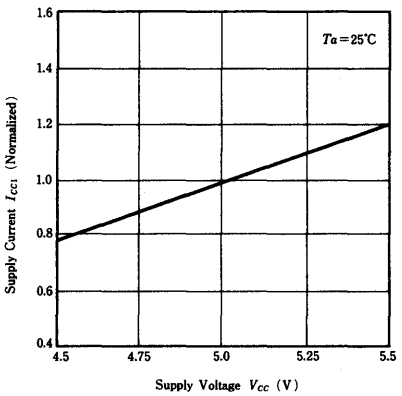
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geqq V_{CC} - 0.2V$, $V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$	2.0	–	–	V
Data Retention Current	I_{CCDR}		–	1	50*2	μA
Chip Deselect to Data Retention Time	t_{CDR}	See retention waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*1	–	–	ns

Note) *1. t_{RC} = Read Cycle Time
*2. V_{CC} = 3.0V

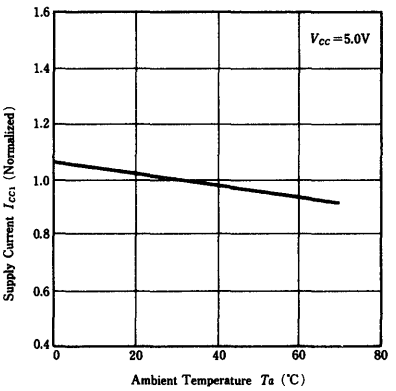
● LOW V_{CC} DATA RETENTION WAVEFORM



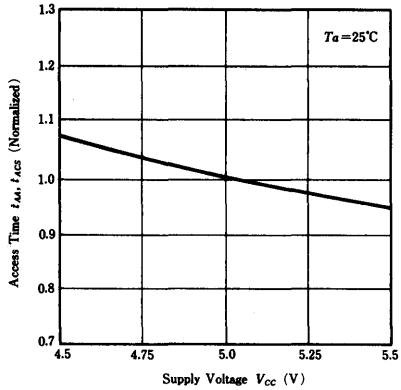
SUPPLY CURRENT vs. SUPPLY VOLTAGE



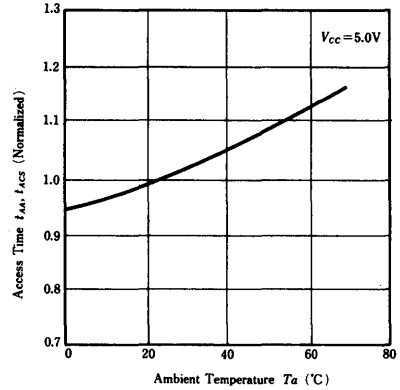
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



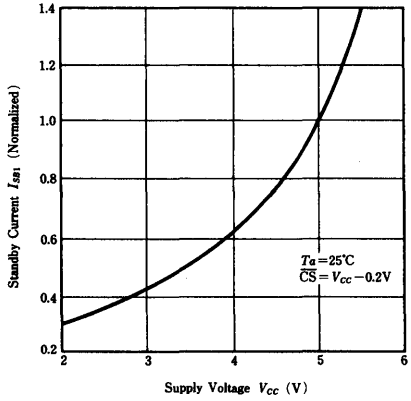
ACCESS TIME vs. SUPPLY VOLTAGE



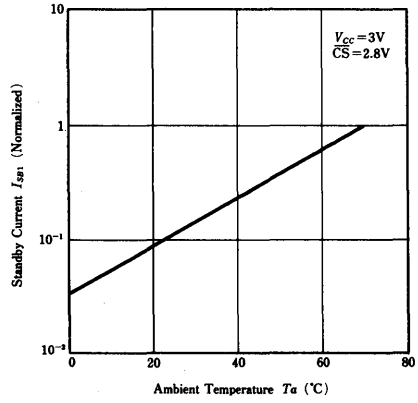
ACCESS TIME vs. AMBIENT TEMPERATURE



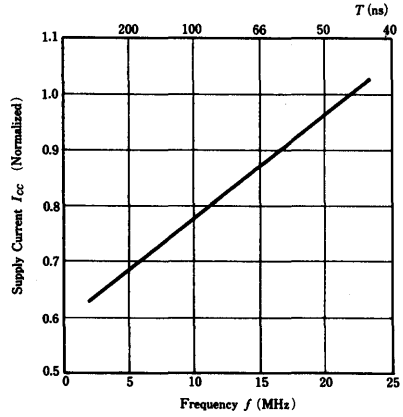
STANDBY CURRENT vs. SUPPLY VOLTAGE



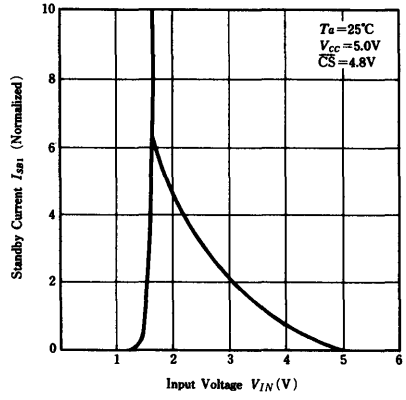
STANDBY CURRENT vs. AMBIENT TEMPERATURE



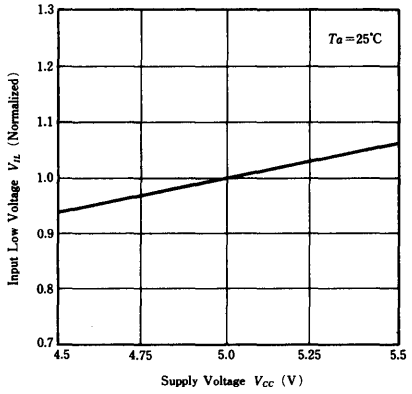
SUPPLY CURRENT vs. FREQUENCY



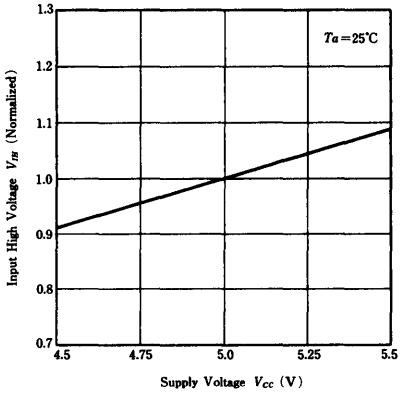
STANDBY CURRENT vs. INPUT VOLTAGE



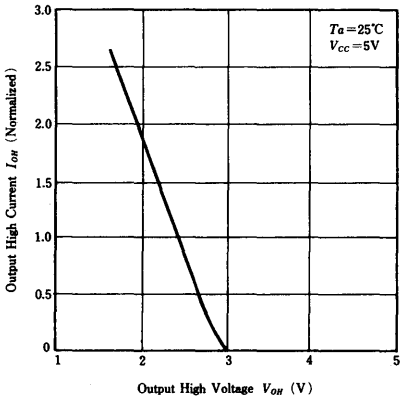
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



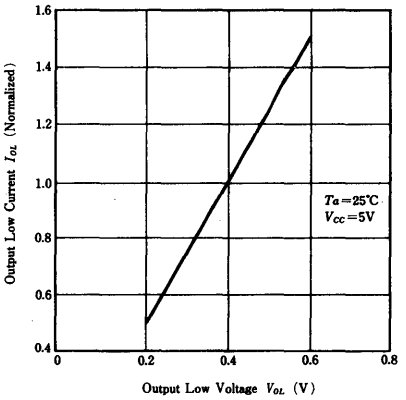
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



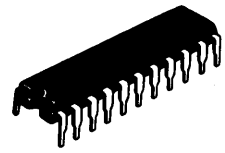
HM6287H Series

65536-Word × 1-Bit High Speed CMOS Static RAM

The Hitachi HM6287H is a high speed 64K static RAM organized as 64-kword × 1-bit. It realizes high speed access time (25/35 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU. The HM6287H packaged in a 300-mil plastic DIP and SOJ, is available for high density mounting.

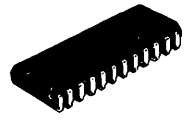
Low power version retains the data with battery back up.

HM6287HP Series



(DP-22NB)

HM6287HJP Series



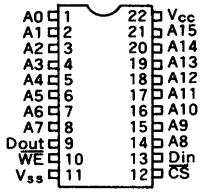
(CP-24D)

Features

- Single 5 V supply and high density 22-pin DIP and 24-pin SOJ
- High speed: Fast access time 25/35 ns (max)
- Low power
  - Operation: 300 mW (typ)
  - Standby: 100 µW (typ)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Directly TTL compatible: All inputs and outputs

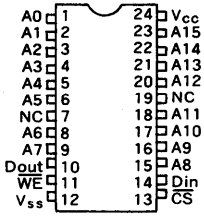
Pin Arrangement

HM6287HP Series



(Top View)

HM6287HJP Series



(Top View)

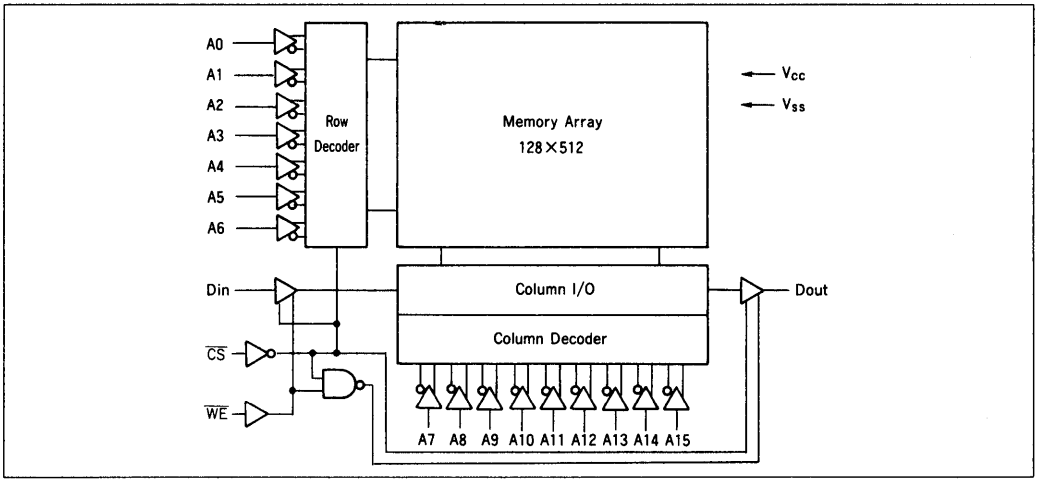
Pin Description

Pin Name	Function
A0 – A15	Address
Din	Input
Dout	Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Ordering Information

Type No.	Access Time	Package
HM6287HP-25	25 ns	300-mil 22-pin plastic DIP (DP-22NB)
HM6287HP-35	35 ns	
HM6287HLP-25	25 ns	
HM6287HLP-35	35 ns	
HM6287HJP-25	25 ns	300-mil 24-pin SOJ (CP-24D)
HM6287HJP-35	35 ns	
HM6287HLJP-25	25 ns	
HM6287HLJP-35	35 ns	

Block diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	Dout Pin	Ref. Cycle
H	×	Standby	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle 1, 2
L	L	Write	Icc	High-Z	Write cycle 1, 2

Note: ×: H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Note: *1. V_T min = −2.0 V for pulse width ≤ 10 ns

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
	Vss	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	−0.5*1	—	0.8	V

Note: *1. V_{IL} min = −2.0 V for pulse width ≤ 10 ns

DC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, Vss = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2.0	µA	Vcc = Max Vin = Vss to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2.0	µA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = Vss to Vcc
Operating Vcc current	Icc	—	60	120	mA	$\overline{CS}$ = V_{IL} Iout = 0 mA, min cycle
Standby Vcc current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, min cycle
Standby Vcc current (1)	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ Vcc – 0.2 V 0 V ≤ Vin ≤ 0.2V or Vcc – 0.2 V ≤ Vin
		—	0.02*2	0.1*2	mA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Notes: *1. Typical limits are at Vcc = 5.0 V, Ta = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)*1

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	8	pF	Vout = 0 V

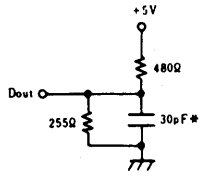
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, unless otherwise noted.)

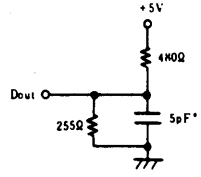
Test Conditions

- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 5 ns
- Input and Output timing reference levels: 1.5 V
- Output load: See figures

Output Load (A)



Output Load (B) (for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

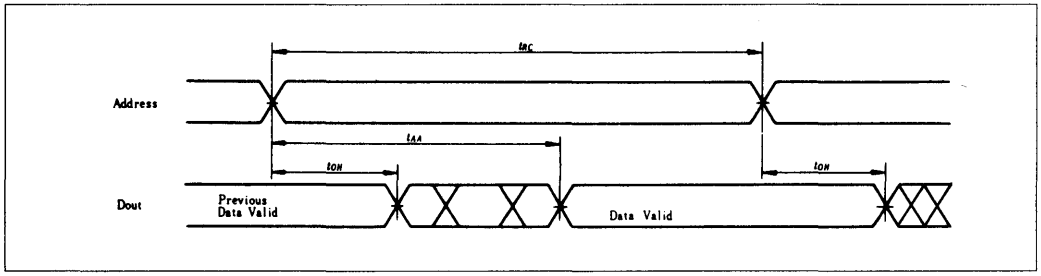


Note: Including scope & jig

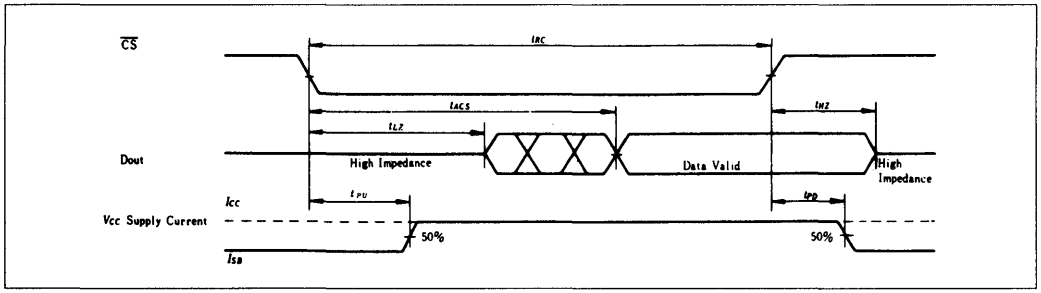
Read Cycle

Item	Symbol	HM6287H-25		HM6287H-35		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	25	—	35	—	ns
Address access time	t_{AA}	—	25	—	35	ns
Chip select access time	t_{ACS}	—	25	—	35	ns
Output hold from address change	t_{OH}	3	—	5	—	ns
Chip selection to output in low-Z	t_{LZ}*1	5	—	5	—	ns
Chip deselection to output in high-Z	t_{HZ}*1	0	12	0	20	ns
Chip selection to power up time	t_{PU}	0	—	0	—	ns
Chip deselection to power down time	t_{PD}	—	25	—	30	ns

Read Timing Waveform (1) *2, *3, *5



Read Timing Waveform (2) *2, *4

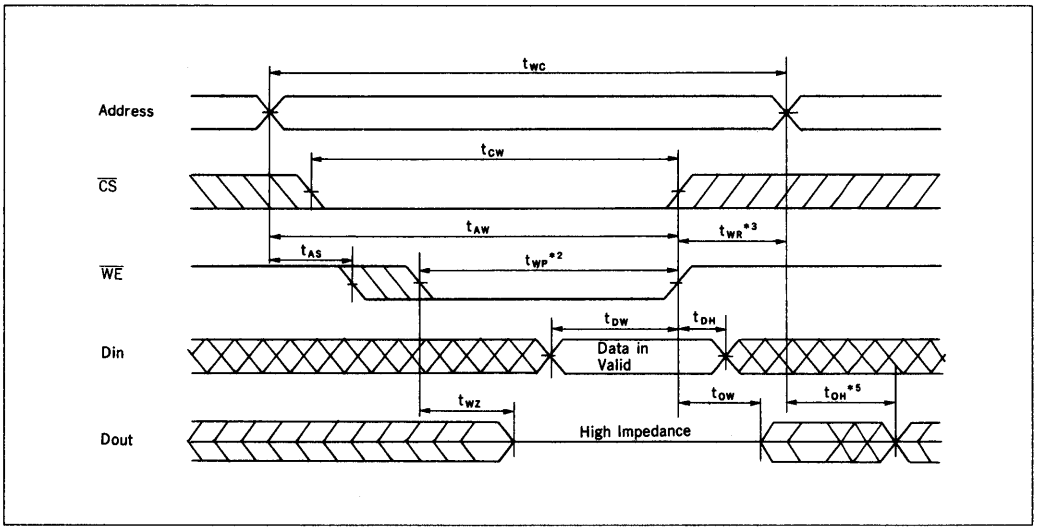


Notes: *1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100 % tested.
*2. $\overline{WE}$ is high for read cycle.
*3. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*4. Address valid prior to or coincident with $\overline{CS}$ transition low.
*5. All read cycle timing are referenced from last valid address to the first transitioning address.

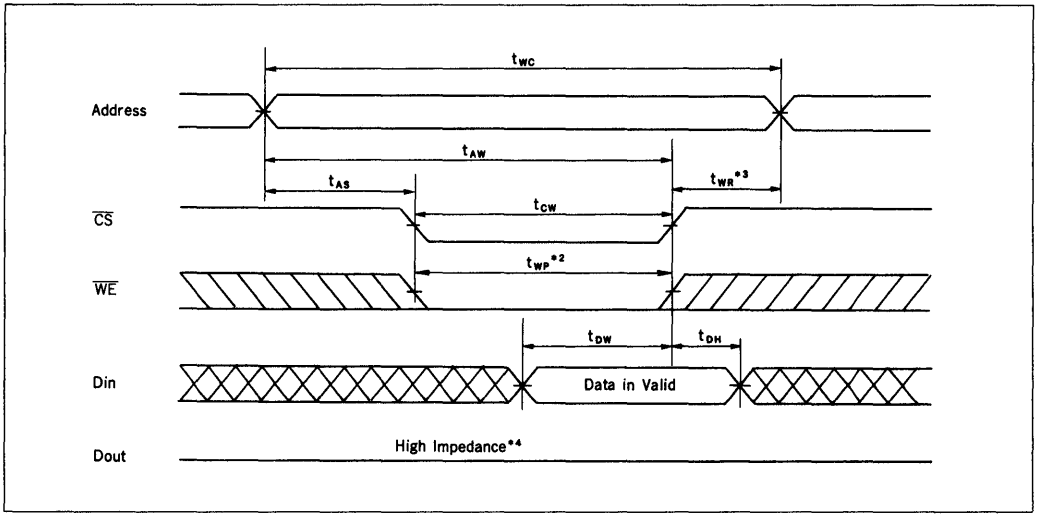
Write Cycle

Item	Symbol	HM6287H-25		HM6287H-35		Unit
		Min	Max	Min	Max	
Write cycle time	t_{WC}	25	—	35	—	ns
Chip selection to end of write	t_{CW}	20	—	30	—	ns
Address valid to end of write	t_{AW}	20	—	30	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	30	—	ns
Write recovery time	t_{WR}	0	—	0	—	ns
Data valid to end of write	t_{DW}	15	—	20	—	ns
Data hold time	t_{DH}	0	—	0	—	ns
Write enabled to output in high-Z	t_{WZ}*1	0	8	0	10	ns
Output active from end of write	t_{OW}*1	5	—	5	—	ns

Write Timing Waveform (1) ($\overline{WE}$ controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
*2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
*3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

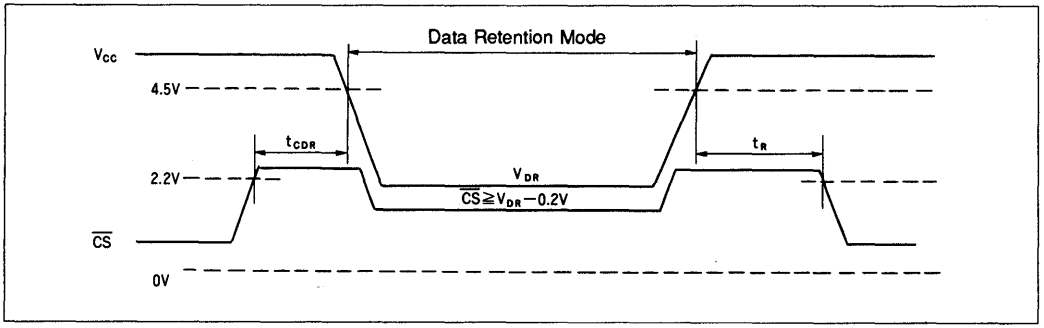
Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

(This specification is guaranteed only for L-version.)

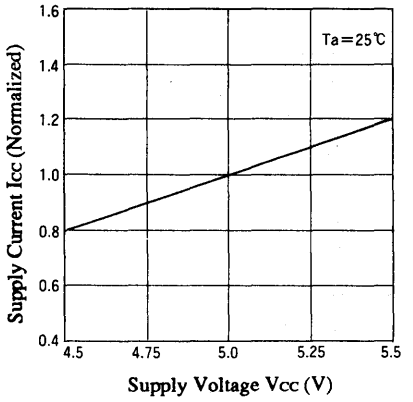
Item	Symbol	Min	Typ	Max	Unit	Test Condition
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V
Data retention current	I_{CCDR}	—	—	50*2	µA	Vin ≥ Vcc – 0.2 V or
				35*3		0 V ≤ Vin ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

Notes: *1. t_{RC} = Read cycle time
*2. Vcc = 3.0 V
*3. Vcc = 2.0 V

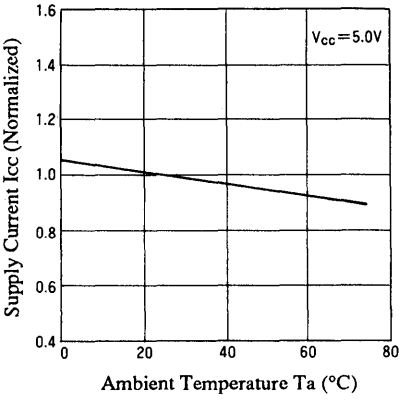
Low Vcc Data Retention Timing Waveform



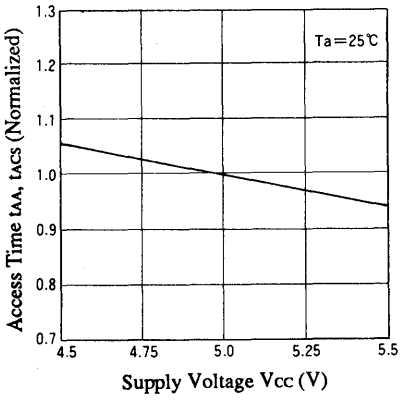
Supply Current vs. Supply Voltage



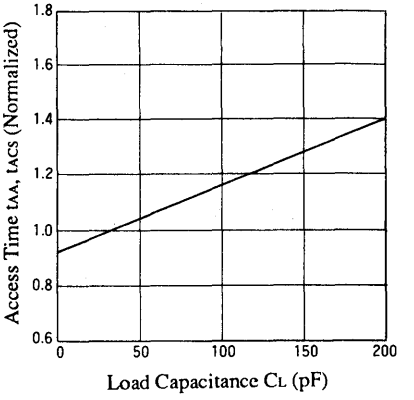
Supply Current vs. Ambient Temperature



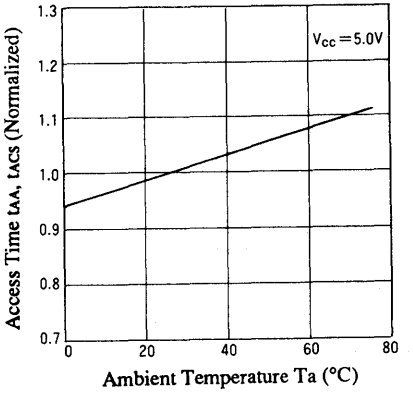
Access Time vs. Supply Voltage



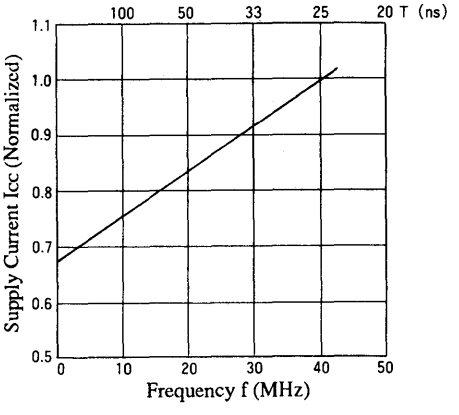
Access Time vs. Load Capacitance



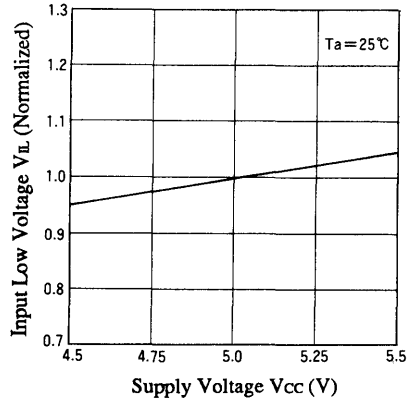
Access Time vs. Ambient Temperature



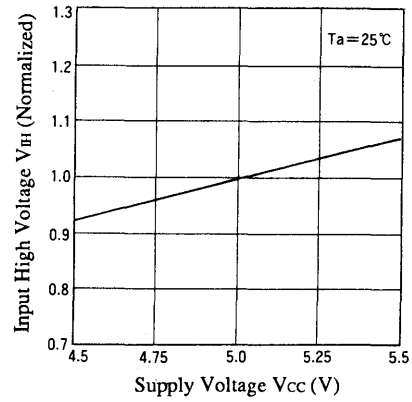
Supply Current vs. Frequency



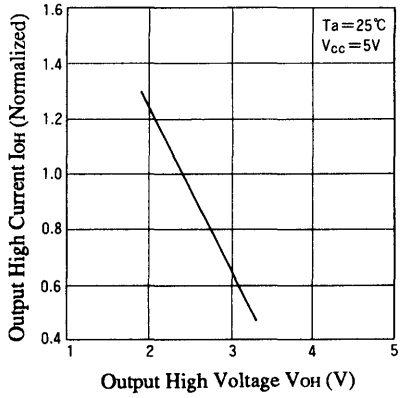
Input Low Voltage vs. Supply Voltage



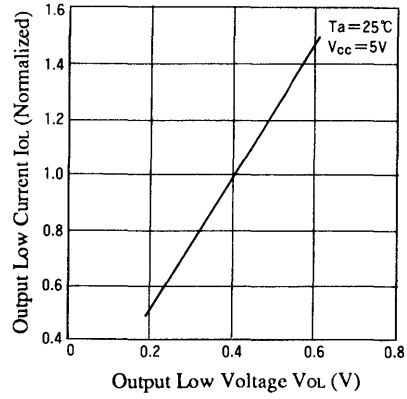
Input High Voltage vs. Supply Voltage



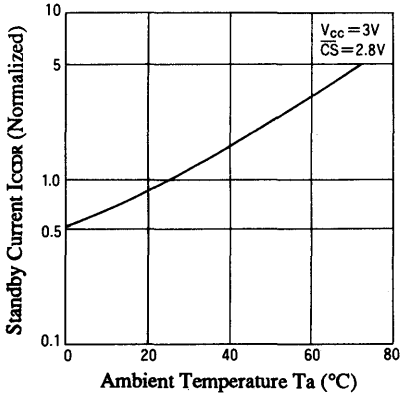
Output Current vs. Output Voltage (1)



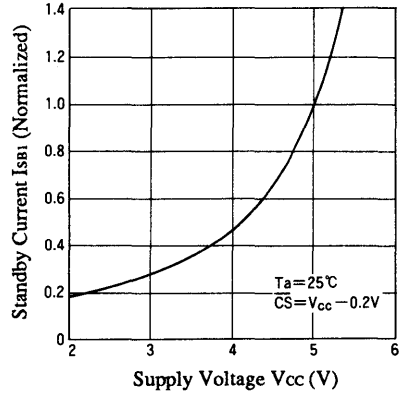
Output Current vs. Output Voltage (2)



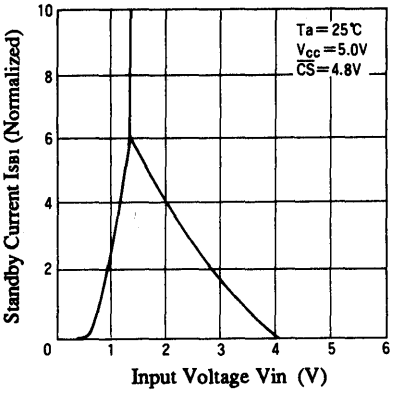
Standby Current vs. Ambient Temperature



Standby Current vs. Supply Voltage

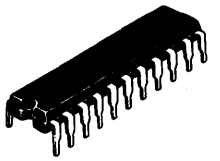


Standby Current vs. Input Voltage



65536-word x 1-bit High Speed Hi-BiCMOS Static RAM

HM6787P Series



(DP-22NB)

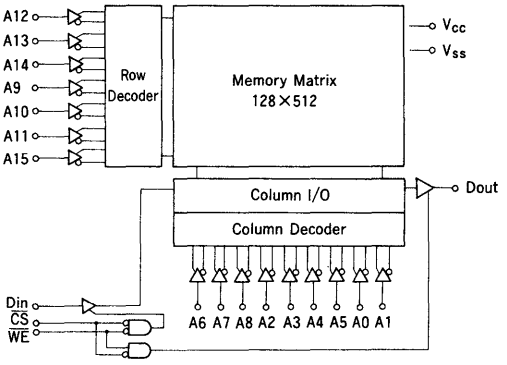
■ FEATURES

- Super Fast Access Time: 25ns/30ns (max.)
- Low Power Dissipation (DC):
  Operating 180mW (typ)
- High Driving Capability: I_{OL} 16mA
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output
- Skinny 22-pin Plastic Dip (300 mil) and 22-pin Chip Carrier

■ ORDERING INFORMATION

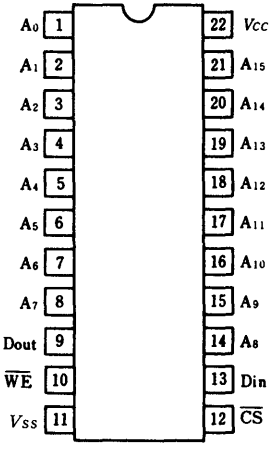
Type No.	Access Time	Package
HM6787P-25	25ns	300 mil 22 pin
HM6787P-30	30ns	Plastic DIP

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT

- HM6787P Series



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}	Dout
L	L	Write	I_{CC}	High Z

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	–0.5*1	–	0.8	V

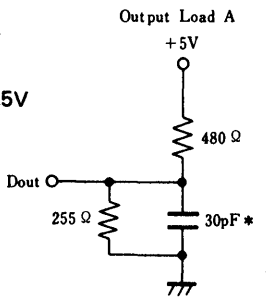
Note) *1. –3.0V for pulse width ≦ 20ns.

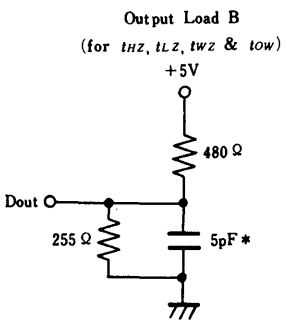
■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0°C to +70°C)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{OUT}=0mA	–	–	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	–	–	40	mA
	I_{SB1}	$\overline{CS} \geqq V_{CC} - 0.2V$ $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC} - 0.2V$	–	–	20	mA
Output Low Voltage	V_{OL}	I_{OL} = 16mA	–	–	0.5	V
Output High Voltage	V_{OH}	I_{OH} = –4mA	2.4	–	–	V

■ AC TEST CONDITIONS

Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 4ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure





* Including scope and jig.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	7.0	pF	V_{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V±10%, T_a = 0°C to 70°C, unless otherwise noted.)

• READ CYCLE

Item	Symbol	HM6787-25		HM6787-30		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	25	–	30	–	ns	
Address Access Time	t_{AA}	–	25	–	30	ns	
Chip Select Access Time	t_{ACS}	–	25	–	30	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	15	0	15	ns	1, 2
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	2
Chip Deselection to Power Down Time	t_{PD}	–	25	–	30	ns	2
Input Voltage Rise/Fall Time	t_T	–	150	–	150	ns	3

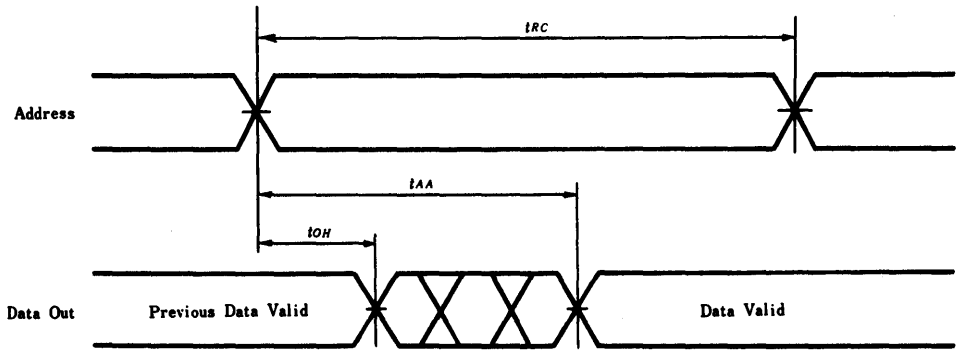
Notes) 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
2. This parameter is sampled and not 100% tested.
3. If tT becomes more than 150ns, there is possibility of function fail.
Please contact your nearest Hitachi's Sale Dept. regarding specification.

• WRITE CYCLE

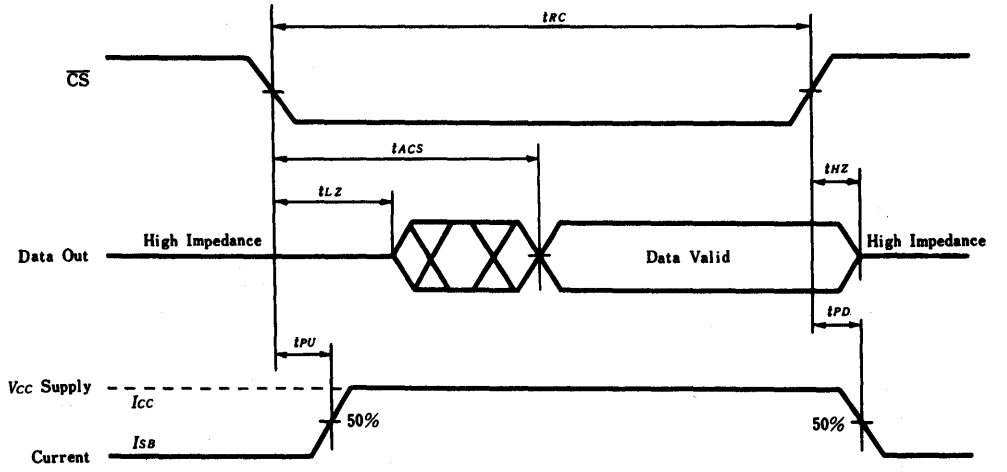
Item	Symbol	HM6787-25		HM6787-30		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	25	–	30	–	ns	2
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns	
Address Valid to End of Write	t_{AW}	20	–	25	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	ns	
Write Recovery Time	t_{WR}	5	–	5	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	15	0	15	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

• TIMING WAVEFORM OF READ CYCLE NO. 1[1), 2)]

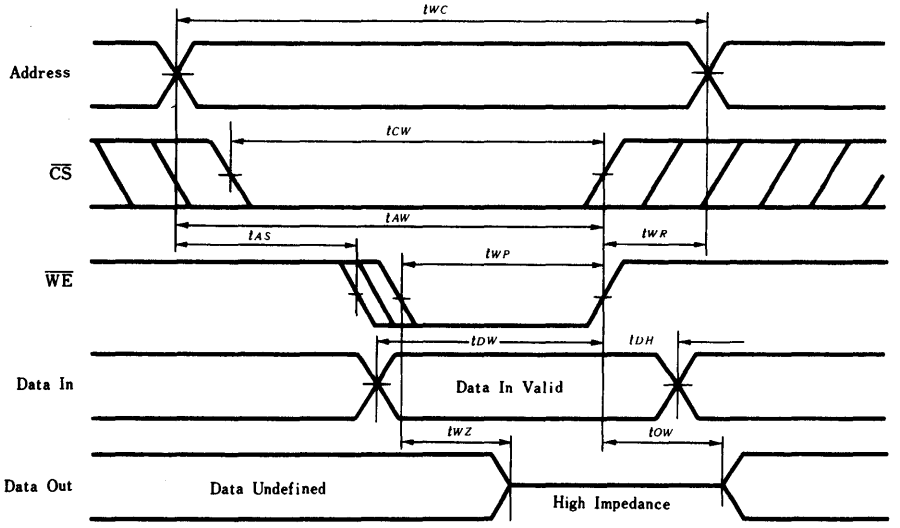


• TIMING WAVEFORM OF READ CYCLE NO. 2[1), 3)]



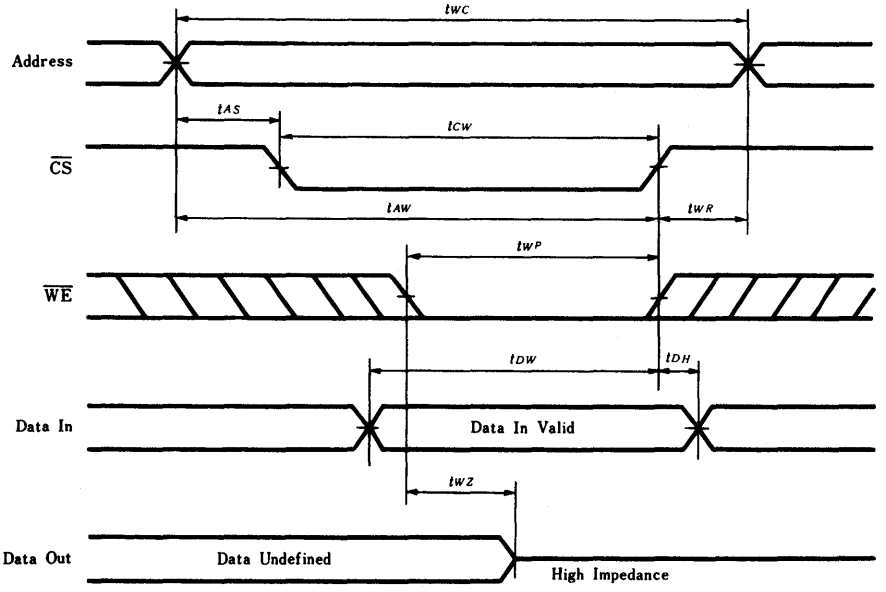
Note: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

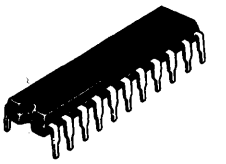
HM6787H Series

65536-word x 1-bit High Speed Hi-BiCMOS Static RAM

Features

- Super Fast Access Time: 15ns/20ns (max.)
- Low Power Dissipation (DC):
  Operating 210mW (typ)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6787HP Series



(DP-22NB)

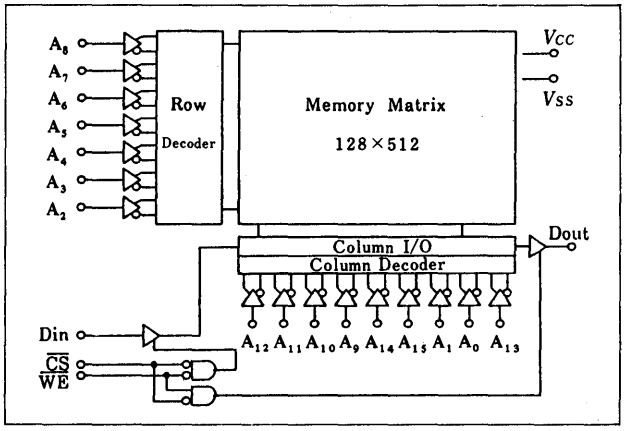
HM6787HJP Series

(CP-24D)

Ordering Information

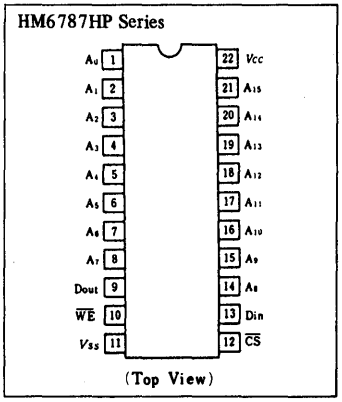
Type No.	Access Time	Package
HM6787HP-15	15ns	300 mil 22 pin
HM6787HP-20	20ns	Plastic DIP
HM6787HJP-15	15ns	300 mil 24 pin
HM6787HJP-20	20ns	Plastic SOJ

Block Diagram

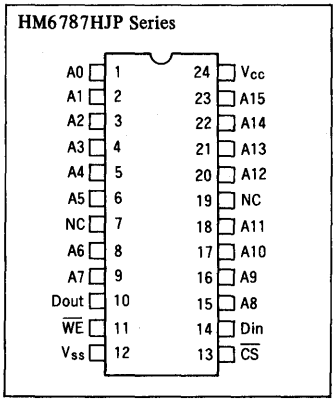


Pin Arrangement

HM6787HP Series



HM6787HJP Series



Note) The specifications of this device are subject to change without notice.
Please contact Hitachi's Sales Dept. regarding specifications.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Temperature under Bias	T_{bias}	−10 to +85	°C

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}, I_{CC1}	Dout
L	L	Write	I_{CC}, I_{CC1}	High Z

Recommended DC Operating Conditions ($0°C \leqq Ta \leqq 70°C$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	–	6.0	V
Input Low Voltage	V_{IL}	−0.5*1	–	0.8	V

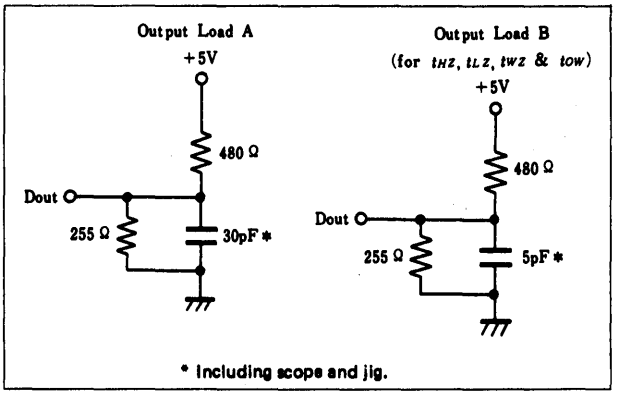
Note) *1. −3.0V for pulse width ≦ 10ns.

DC and Operating Characteristics ($V_{CC} = 5V \pm 10\%$, $T_a = 0°C$ to $+70°C$)

Item	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	$V_{CC} = 5.5V$, $V_{IN} = V_{SS}$ to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{CS} = V_{IH}$, $V_{OUT} = V_{SS}$ to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS} = V_{IL}$, I_{OUT}=0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min. Cycle, Duty: 100% I_{OUT}=0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS} = V_{IH}$
	I_{SB1}	–	–	10	mA	$\overline{CS} \geqq V_{CC} - 0.2V$ $V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC} - 0.2V$
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4mA

AC Test Conditions

Input pulse levels: V_{SS} to 3.0V
Input rise and fall times: 4ns
Input timing reference levels: 1.5V
Output reference levels: 1.5V
Output load: See Figure



Capacitance (T_a = 25°C, f = 1.0MHz)

Item	Symbol	max.	Unit	Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	10.0	pF	V_{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5V±10%, T_a = 0°C to 70°C, unless otherwise noted.)

Read Cycle

Item	Symbol	HM6787H-15		HM6787H-20		Unit	Notes
		min.	max.	min.	max.		
Read Cycle Time	t_{RC}	15	–	20	–	ns	
Address Access Time	t_{AA}	–	15	–	20	ns	
Chip Select Access Time	t_{ACS}	–	15	–	20	ns	
Output Hold from Address Change	t_{OH}	3	–	3	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	3	–	3	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	ns	1, 2

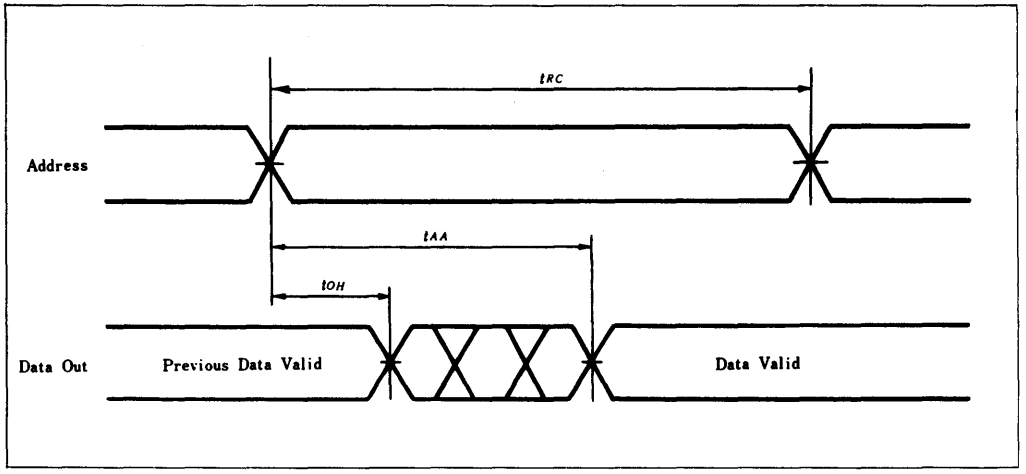
Note: 1. This parameter is sampled and 100% tested.
2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

Write Cycle

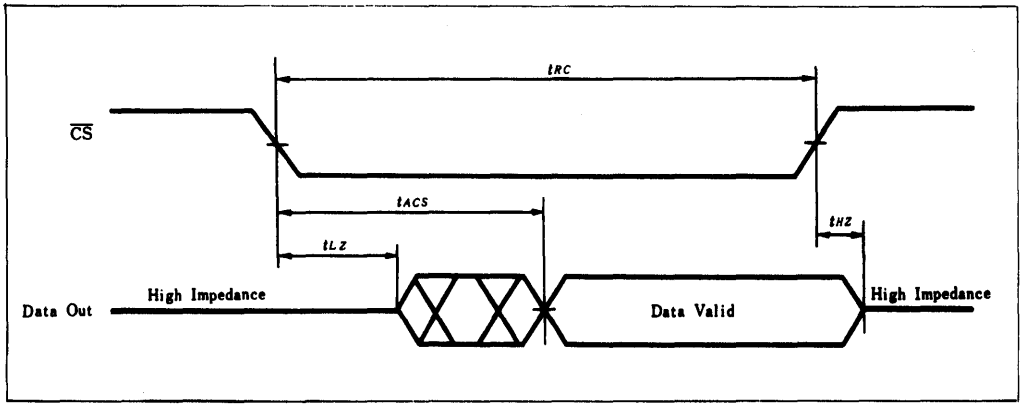
Item	Symbol	HM6787H-15		HM6787H-20		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	15	–	20	–	ns	2
Chip Selection to End of Write	t_{CW}	10	–	15	–	ns	
Address Valid to End of Write	t_{AW}	10	–	15	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	10	–	15	–	ns	
Write Recovery Time	t_{WR}	3	–	3	–	ns	
Data Valid to End of Write	t_{DW}	12	–	15	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

Timing Waveform of Read Cycle No. 1[1), 2)]

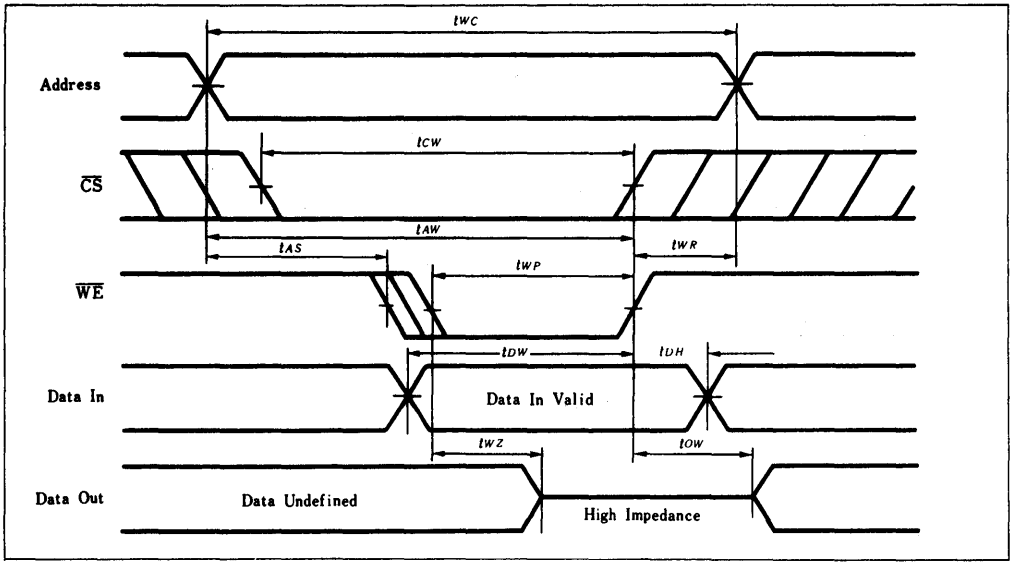


Timing Waveform of Read Cycle No. 2[1), 3)]



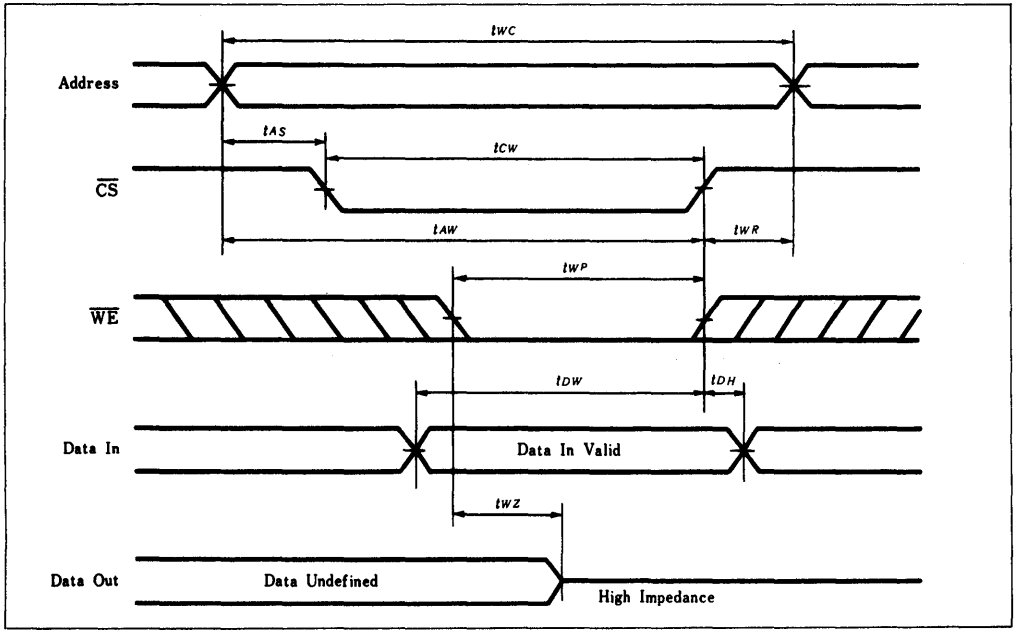
Note: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



Note: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

HM6787HA Series — Preliminary

65536-Word × 1-Bit High Speed Static RAM

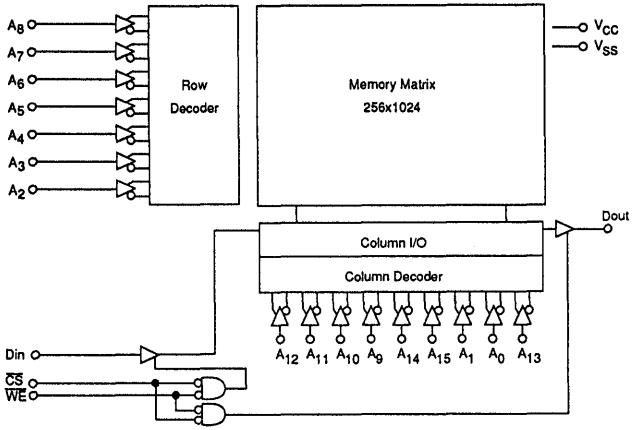
■ FEATURES

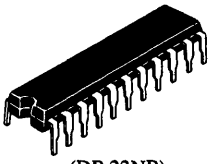
- Super Fast
  Access Time . . . . . 12/15/20ns (max.)
- Low Power Dissipation
  (DC) Operating . . . . . 300mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6787HAP-12 HM6787HAP-15 HM6787HAP-20	12ns 15ns 20ns	300 mil 22 pin Plastic DIP (DP-22NB)
HM6787HAJP-12 HM6787HAJP-15 HM6787HAJP-20	12ns 15ns 20ns	300 mil 24 pin Plastic SOJ (CP-24D)

■ BLOCK DIAGRAM



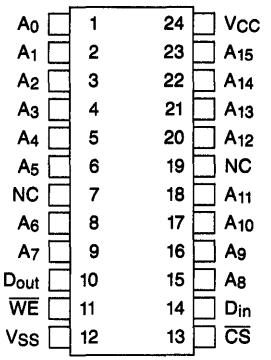


(DP-22NB)

(CP-24D)

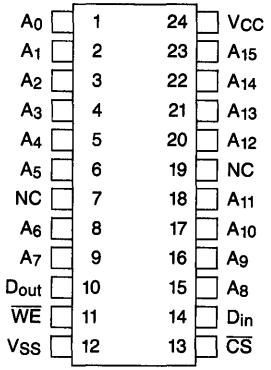
■ PIN ARRANGEMENT

HM6787HAP Series



(Top View)

HM6787HAJP Series



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_a \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	−3.0*	—	0.8	V

*Pulse width ≤ 10ns, DC: −0.5V

■ TRUTH TABLE

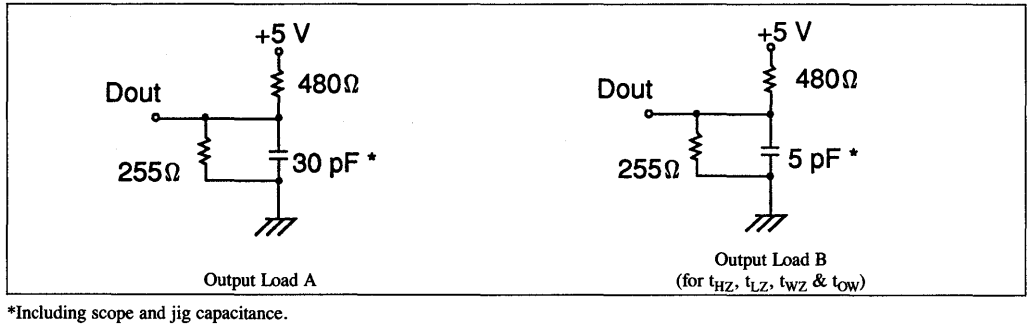
$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}, I_{CC1}	Data Out
L	L	Write	I_{CC}, I_{CC1}	High Z

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0°C$ to $70°C$, $V_{SS} = 0V$)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC} = 5.5V$, $V_{IN} = V_{SS}$ to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS} = V_{IH}$, $V_{OUT} = V_{SS}$ to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_{OUT} = 0mA$	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle Duty: 100%, $I_{OUT} = 0mA$	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$	—	—	30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	—	—	10	mA
Output Low Voltage	V_{OL}	$I_{OL} = 8mA$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4mA$	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input Timing Reference Levels: 1.5V
- Output Load: See Figure
- Input Rise and Fall Times: 4ns
- Output Reference Levels: 1.5V



*Including scope and jig capacitance.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Max.	Unit	Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	10.0	pF	V_{OUT} = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a to 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6787HA-12		HM6787HA-15		HM6787HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	12	—	15	—	20	—	ns	—
Address Access Time	t_{AA}	—	12	—	15	—	20	ns	—
Chip Select Access Time	t_{ACS}	—	12	—	15	—	20	ns	—
Output Hold from Address Change	t_{OH}	4	—	4	—	4	—	ns	—
Chip Selection to Output in Low Z	t_{LZ}	3	—	5	—	5	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	6	0	8	ns	1, 2

NOTES: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• Write Cycle

Item	Symbol	HM6787HA-12		HM6787HA-15		HM6787HA-20		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	12	—	15	—	20	—	ns	2
Chip Selection to End of Write	t_{CW}	8	—	10	—	15	—	ns	—
Address Valid to End of Write	t_{AW}	8	—	10	—	15	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Write Pulse Width	t_{WP}	8	—	10	—	15	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Data Valid to End of Write	t_{DW}	7	—	8	—	10	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Write Enable to Output in High Z	t_{WZ}	0	6	0	6	0	8	ns	3, 4
Output Active from End of Write	t_{OW}	3	—	3	—	3	—	ns	3, 4

NOTES: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

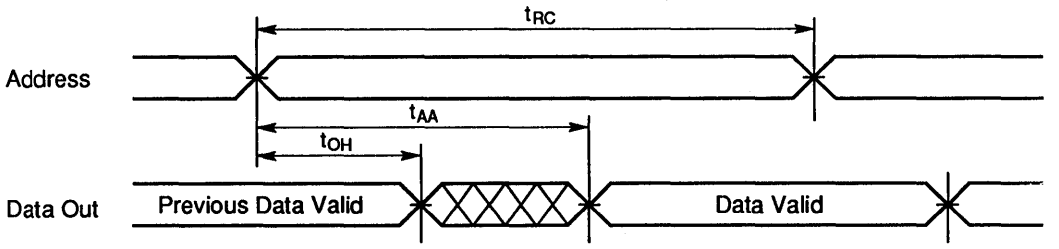
2. All write cycle timings are referenced from the last valid address to the first transitioning address.

3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

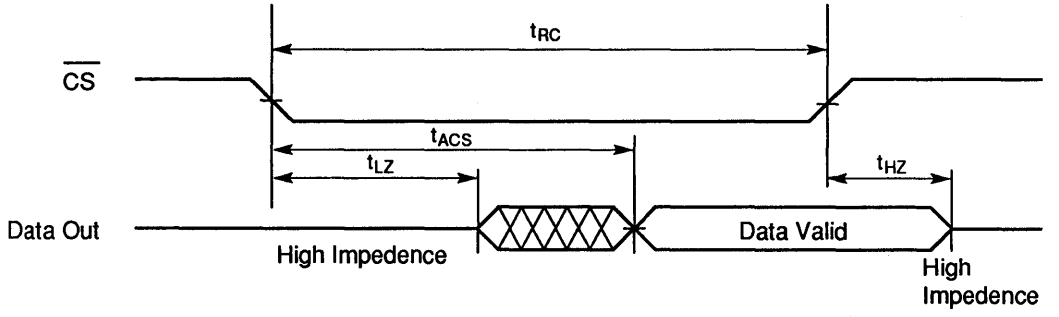
4. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

• Read Cycle (1) (1) (2)

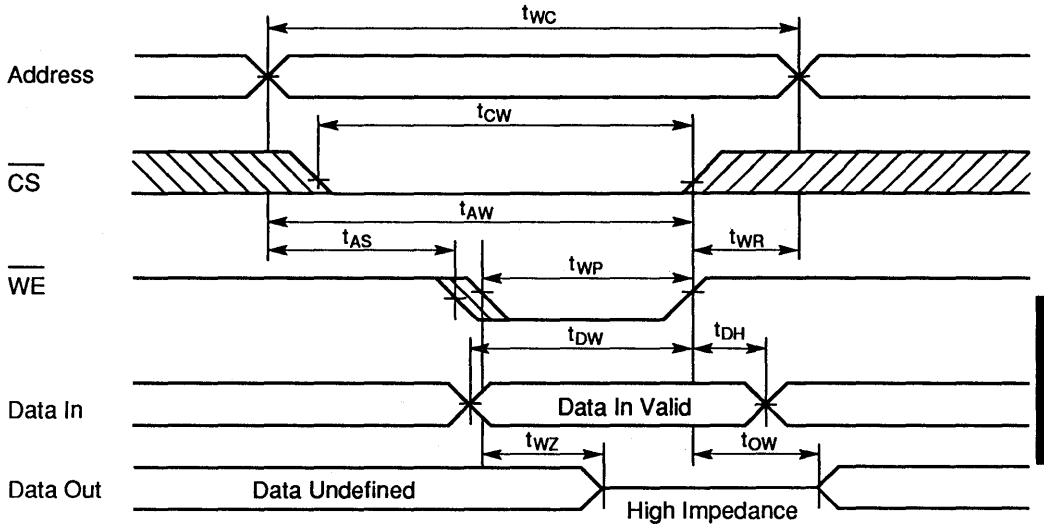


• Read Cycle (2) (1) (3)



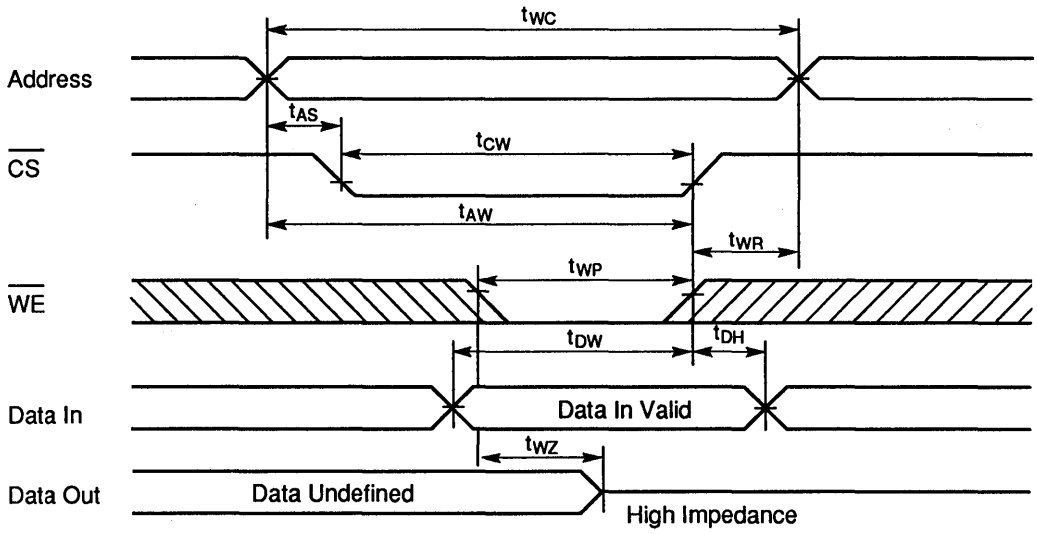
NOTES: 1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• **Write Cycle (1)** ($\overline{WE}$ Controlled)



NOTE: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• **Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTE: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

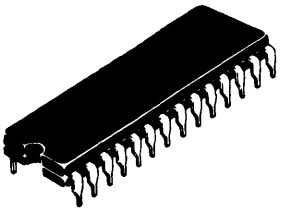
HM62256 Series

32768-word x 8-bit High Speed CMOS Static RAM

■ FEATURES

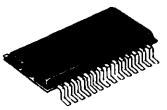
- High Speed: Fast Access Time 85/100/120/150ns (max.)
- Low Power Standby and Low Power Operation;
  Standby: 200μW (typ)/10μW (typ) (L-version),
  Operation: 40mW (typ.) (f = 1MHz)
- Single 5V Supply
- Completely Static RAM: No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three-state Output
- Directly TTL Compatible: All Input and Output
- Capability of Battery Back Up Operation (L-/L-SL version)

HM62256P Series



(DP-28)

HM62256FP Series

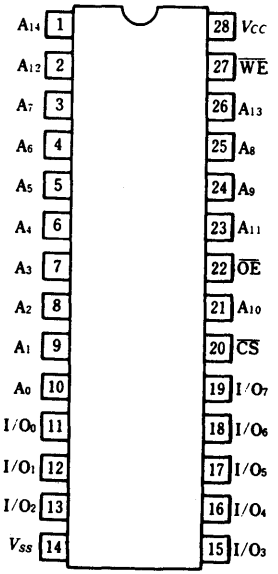


(FP-28DA)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM62256P-8	85ns	600 mil 28 pin Plastic DIP
HM62256P-10	100ns	
HM62256P-12	120ns	
HM62256P-15	150ns	
HM62256LP-8	85ns	
HM62256LP-10	100ns	
HM62256LP-12	120ns	
HM62256LP-15	150ns	
HM62256LP-10SL	100ns	
HM62256LP-12SL	120ns	
HM62256LP-15SL	150ns	
HM62256FP-8T	85ns	28 pin Plastic SOP
HM62256FP-10T	100ns	
HM62256FP-12T	120ns	
HM62256FP-15T	150ns	
HM62256LFP-8T	85ns	
HM62256LFP-10T	100ns	
HM62256LFP-12T	120ns	
HM62256LFP-15T	150ns	
HM62256LFP-10SLT	100ns	
HM62256LFP-12SLT	120ns	
HM62256LFP-15SLT	150ns	

■ PIN ARRANGEMENT



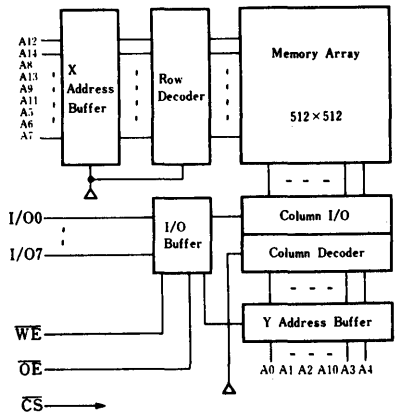
(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin with relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Temperature Under Bias	T_{bias}	−10 to +85	°C

Note) *1. −3.0V for pulse width ≦ 50ns

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	L	H	Read	I_{CC}	Dout	Read Cycle No. 1~3
L	H	L	Write	I_{CC}	Din	Write Cycle No. 1
L	L	L	Write	I_{CC}	Din	Write Cycle No. 2

X means H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0V for pulse width ≦ 50ns

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, T_a = 0 to +70°C)

Item		Symbol	Test Condition	min	typ*1	max	Unit
Input Leakage Current		$\|I_{LI}\|$	V_{IN} = V_{SS} to V_{CC}	–	–	2	μA
Output Leakage Current		$\|I_{LO}\|$	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, $V_{I/O}$=V_{SS} to V_{CC}	–	–	2	μA
Operating Power Supply Current		I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	8	15	mA
Average Operating Power Supply Current	HM62256-8	I_{CC1}	Min. Cycle, duty=100%, $\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	–	50	70	mA
	HM62256-10			–	40	70	
	HM62256-12			–	35	70	
	HM62256-15			–	33	70	
		I_{CC2}	$\overline{CS}$=V_{IL}, V_{IH}=V_{CC}, V_{IL}=0V, $I_{I/O}$=0mA, f=1MHz	–	8	15	mA
Standby Power Supply Current		I_{SB}	$\overline{CS}$=V_{IH}	–	0.5	3	mA
		I_{SB1}	$\overline{CS}$ ≧ V_{CC}−0.2V, 0V ≦ V_{IN}	–	0.04	2	mA
				–	2*2	100*2	μA
				–	2*3	50*3	
Output Voltage		V_{OL}	I_{OL}=2.1mA	–	–	0.4	V
		V_{OH}	I_{OH}=−1.0mA	2.4	–	–	V

Notes) *1. Typical values are at V_{CC}=5.0V, T_a=25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.
*3. This characteristics is guaranteed only for L-SL version.

■ CAPACITANCE (T_a=25°C, f=1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in}=0V	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	–	8	pF

Note) This parameter is sampled and not 100% tested.

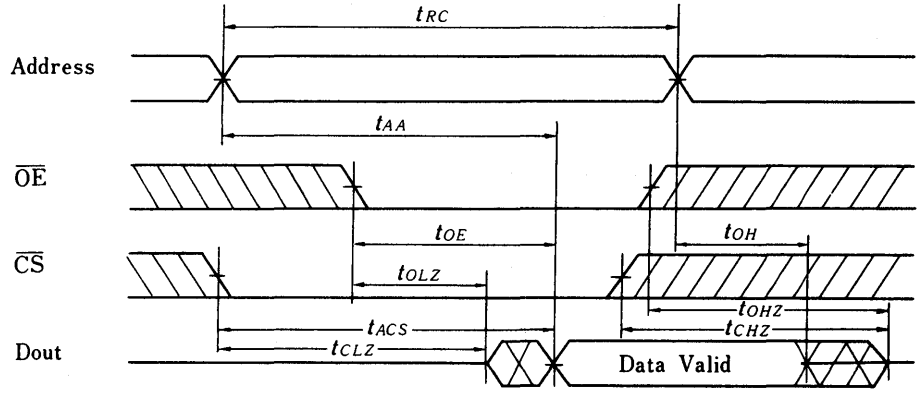
■ AC CHARACTERISTICS (V_{CC}=5V± 10%, T_a=0 to +70°C unless otherwise noted)

- **AC Test Conditions**
  - ○ Input pulse levels: 0.8V to 2.4V
  - ○ Input rise and fall times: 5ns
  - ○ Input and Output timing reference levels: 1.5V
  - ○ Output load: 1TTL Gate and C_L (100pF) (Including scope and jig)

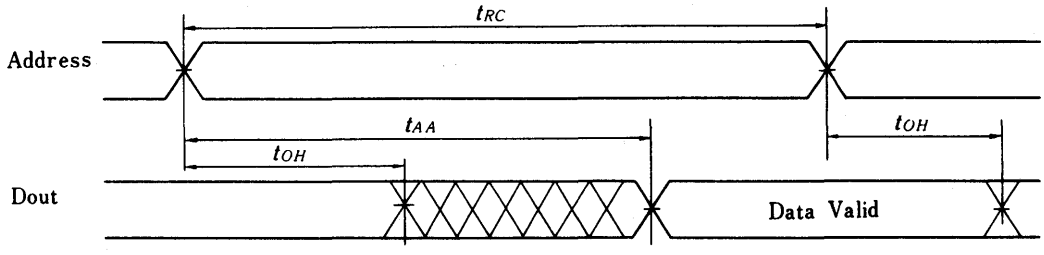
- **Read Cycle**

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	85	–	100	–	120	–	150	–	ns
Address Access Time	t_{AA}	–	85	–	100	–	120	–	150	ns
Chip Select Access Time	t_{ACS}	–	85	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	45	–	50	–	60	–	70	ns
Output Hold from Address Change	t_{OH}	5	–	10	–	10	–	10	–	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	–	10	–	10	–	10	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns

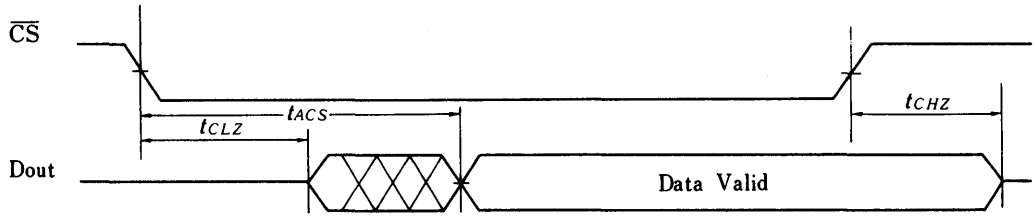
- **Timing Waveform of Read Cycle No. 1[1]**



- **Timing Waveform of Read Cycle No. 2[1][2][4]**



- **Timing Waveform of Read Cycle No. 3[1][3][4]**

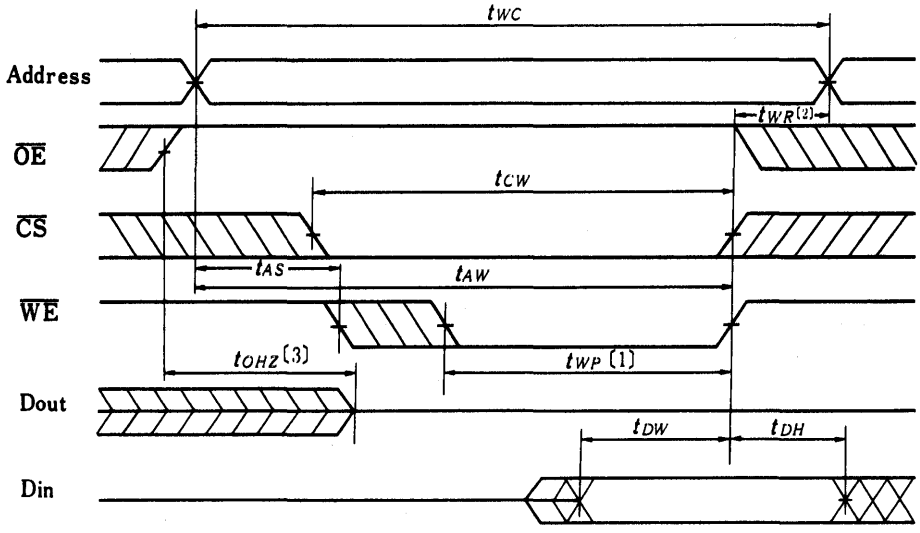


Notes) 1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address Valid prior to or coincident with $\overline{CS}$ transition Low.
4. $\overline{OE}$ = V_{IL}.

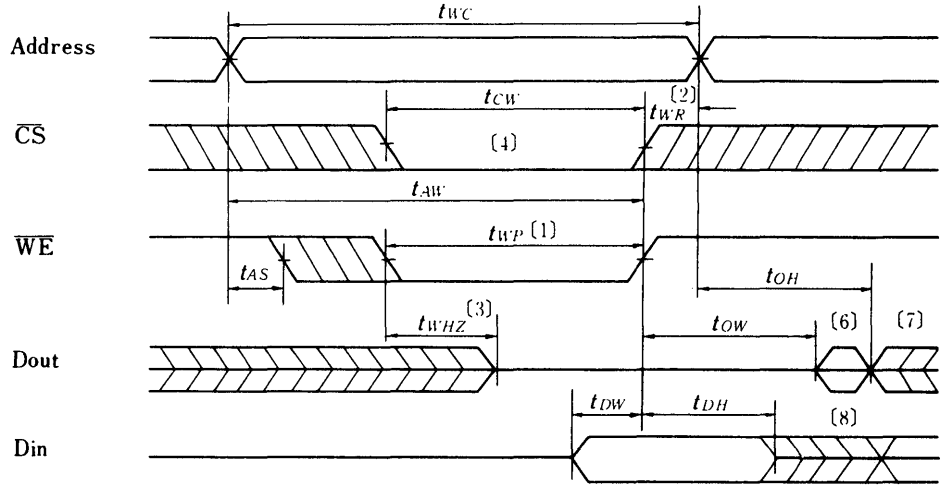
- **Write Cycle**

Item	Symbol	HM62256-8		HM62256-10		HM62256-12		HM62256-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	85	–	100	–	120	–	150	–	ns
Chip Selection to End of Write	t_{CW}	75	–	80	–	85	–	100	–	ns
Address Valid to End of Write	t_{AW}	75	–	80	–	85	–	100	–	ns
Address Set Up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Write Pulse Width	t_{WP}	60	–	60	–	70	–	90	–	ns
Write Recovery Time	t_{WR}	10	–	0	–	0	–	0	–	ns
Write to Output in High Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	–	40	–	50	–	60	–	ns
Data Hold from Write Time	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns

- **Timing Waveform of Write Cycle No. 1 ($\overline{OE}$ Clock)**



- **Timing Waveform of Write Cycle No. 2[5] ($\overline{OE}$ Low Fixed)**



Notes: 1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$)
6. Dout is in the same phase of written data of this write cycle.
7. Dout is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O Pins.

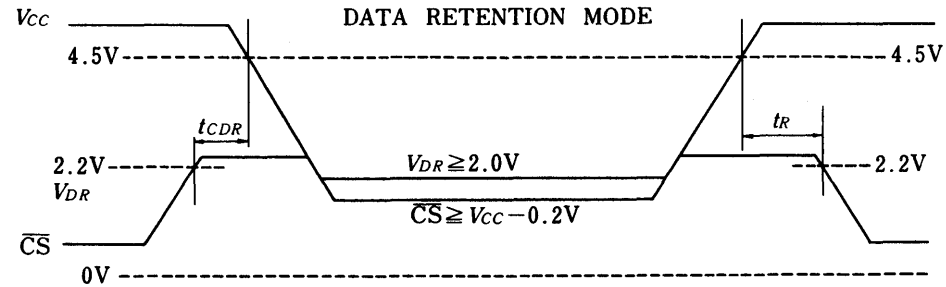
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_a = 0 to +70°C)

(This characteristics is guaranteed only for L-and L-SL version)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
V_{CC} for Date Retention	V_{DR}	$\overline{CS} \geqq V_{CC}$ -0.2V	2.0	–	–	V
Data Retention Current	I_{CCDR}	V_{CC} = 3.0V, $\overline{CS} \geqq$ 2.8V 0V $\leqq V_{in}$	–	–	50*2	μA
			–	–	10*3	
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	–	–	ns
Operation Recovery Time	t_R		t_{RC}*1	–	–	ns

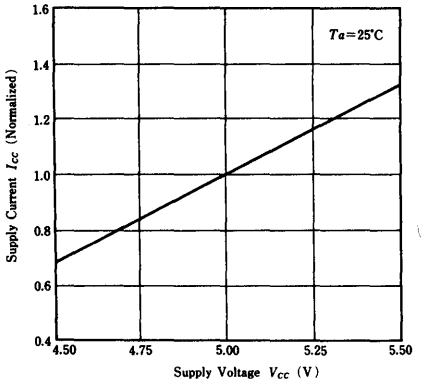
Note) *1. t_{RC} = Read Cycle Time
*2. This characteristic is guaranteed only for L-version, 20μA max. at T_a = 0 to 40°C.
*3. This characteristic is guaranteed only for L-SL version, 3μA max. at T_a = 0 to 40°C.

- **Low V_{CC} Data Retention Waveform**

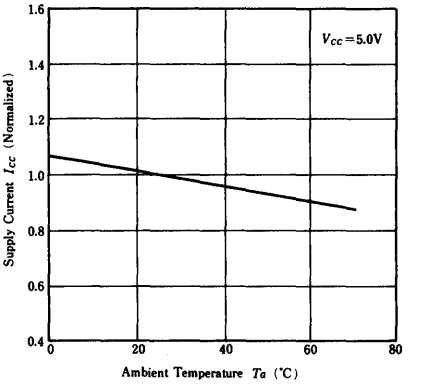


Note) In Data Retention Mode, $\overline{CS}$ controls the Address, $\overline{WE}$, $\overline{OE}$, and Din Buffers. *Vin* for these inputs can be in high impedance state in data retention mode.

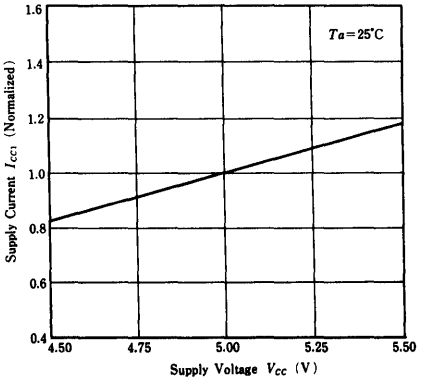
SUPPLY CURRENT vs. SUPPLY VOLTAGE (1)



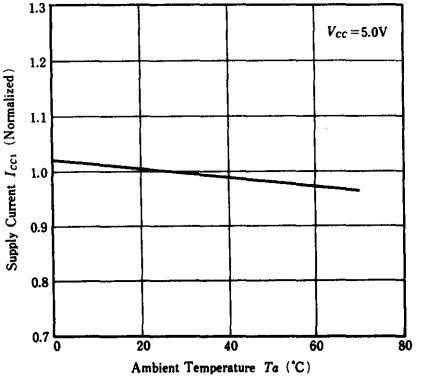
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (1)



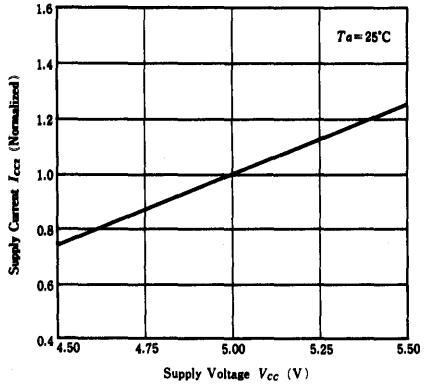
SUPPLY CURRENT vs. SUPPLY VOLTAGE (2)



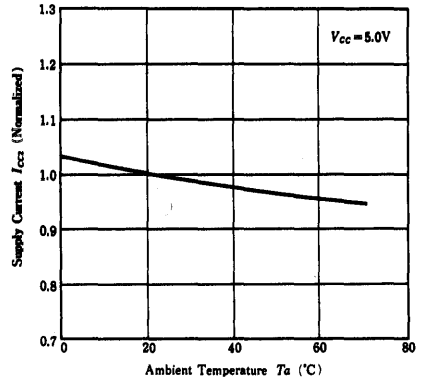
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (2)



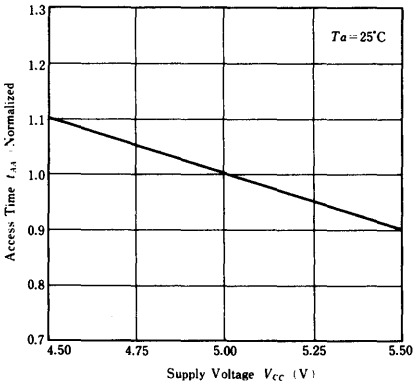
SUPPLY CURRENT vs. SUPPLY VOLTAGE (3)



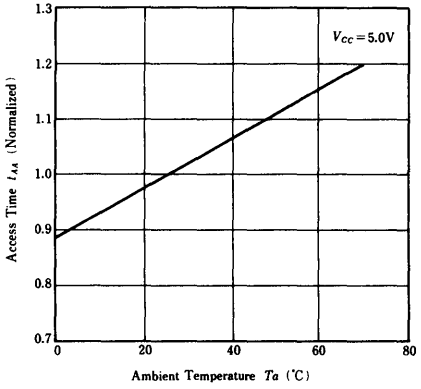
SUPPLY CURRENT vs. AMBIENT TEMPERATURE (3)



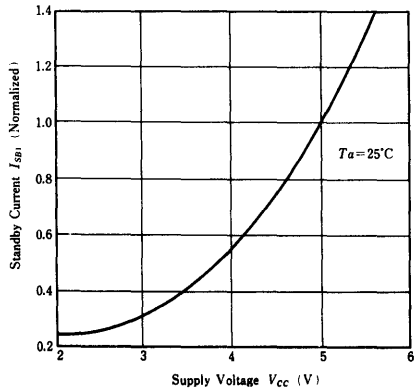
ACCESS TIME vs. SUPPLY VOLTAGE



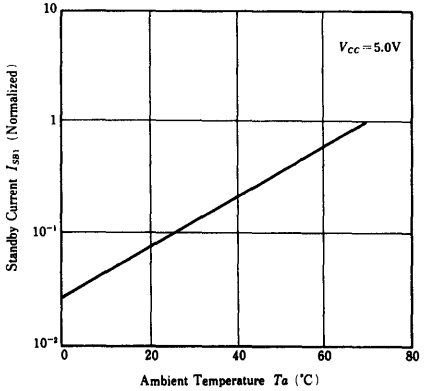
ACCESS TIME vs. AMBIENT TEMPERATURE



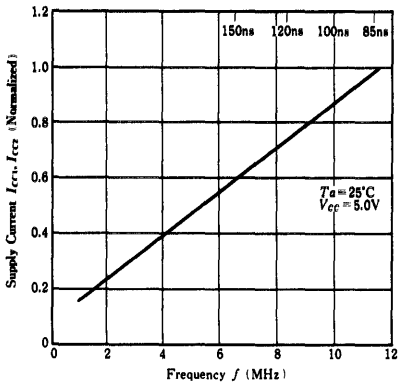
STANDBY CURRENT vs. SUPPLY VOLTAGE



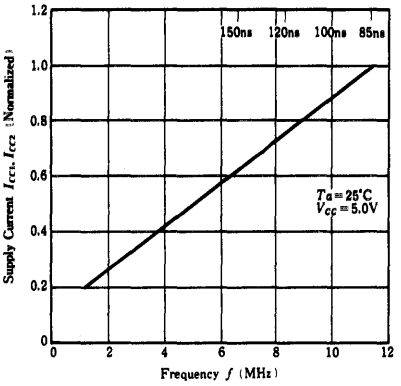
STANDBY CURRENT vs. AMBIENT TEMPERATURE



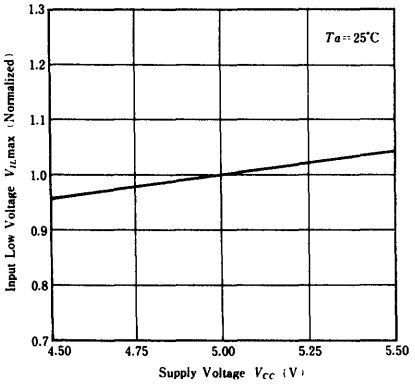
SUPPLY CURRENT vs. FREQUENCY (READ)



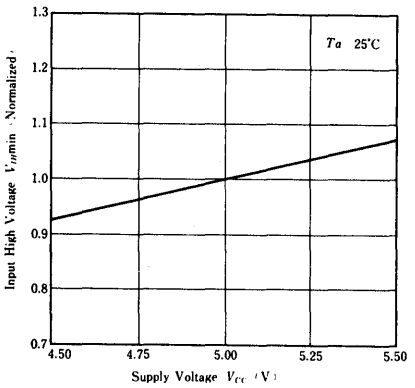
SUPPLY CURRENT vs. FREQUENCY (WRITE)



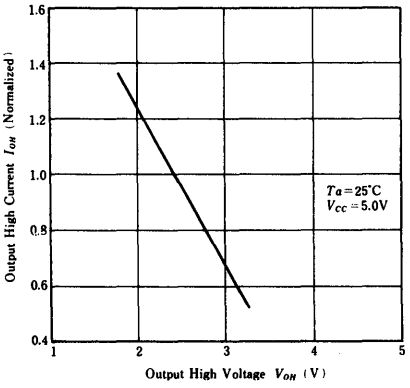
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



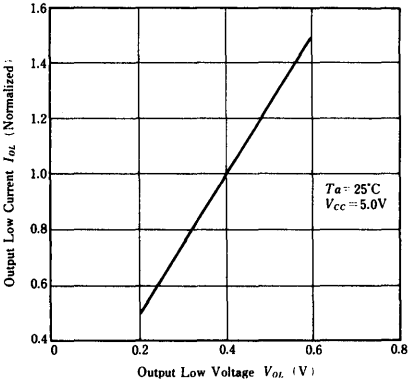
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



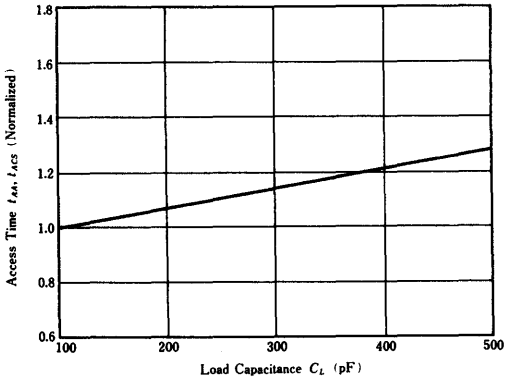
OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE



ACCESS TIME vs. LOAD CAPACITANCE



HM62832/HM62832H
8-Bit CMOS Static RAM

32768-WORD × 8-BIT HIGH SPEED CMOS STATIC RAM

■ FEATURES

- High speed: Fast Access time 25/35/45 ns (max.)

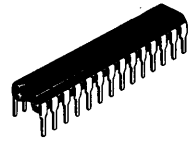
HM62832—Low power
Standby: 10 μW (typical) (L-version)
Active: 300 mW (typical)

HM62832H—Low power
Standby: 300 mW (typical)
Active: 30 μW (typical) (L-version)

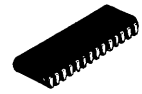
- Single 5V supply
- Completely static memory
  No clock or timing strobe required
- Equal access and cycle times
- Common data input and output—Three stage output
- Directly TTL compatible—All inputs and outputs

■ ORDERING INFORMATION

Part No.	Access	Package
HM62832P-35	35 ns	300 mil 28-pin Plastic DIP
HM62832P-45	45 ns	
HM62832LP-35	35 ns	
HM62832LP-45	45 ns	
HM62832JP-35	35 ns	300 mil 28-pin Plastic SOJ
HM62832JP-45	45 ns	
HM62832LJP-35	35 ns	
HM62832LJP-45	45 ns	
HM62832HP-25	25 ns	300 mil 28-pin Plastic DIP (DP-28NA)
HM62832HP-35	35 ns	
HM62832HP-45	45 ns	
HM62832HJP-25	25 ns	300 mil 28-pin Plastic SOJ (CP-28DN)
HM62832HJP-35	35 ns	
HM62832HJP-45	45 ns	



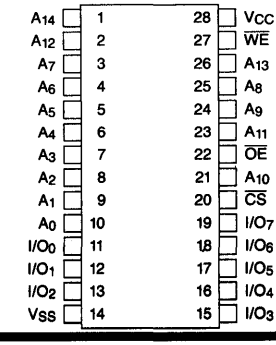
(DP-28NA)



(CP-28DN)

PIN ARRANGEMENT

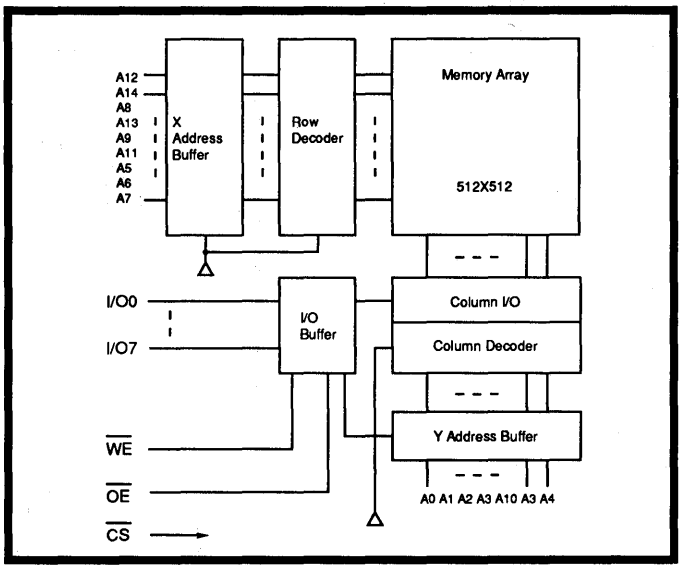
Top View



■ PIN DESCRIPTION

Pin Name	Function
A_0-A_{14}	Address
I/O_0-I/O_7	Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	-0.5*1 to + 7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

NOTE: 1. -2.5 V for pulse width ≤ 10 ns

■ FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	*Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	D_{out}	Read Cycle(1) to (3)
L	H	L	Write	I_{CC}	D_{in}	Write Cycle(1)
L	L	L		I_{CC}	D_{in}	Write Cycle(2)

NOTE: 1. X : H or L

■ DC CHARACTERISTICS for HM62832 (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions	Note
Input Leakage Current	$\|I_{LI}\|$	—	—	10	μA	V_{in} = V_{SS} to V_{CC}	
Output Leakage Current	$\|I_{LO}\|$	—	—	10	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Average Operating Power Supply Current	I_{CC}	—	60	120	mA	Min. cycle, duty = 100%, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	
Standby V_{CC} Current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}	
	I_{SB1}	—	2	100	μA	$\overline{CS}$ ≥ V_{CC} - 0.2V, 0 V ≤ V_{in} ≤ 0.2 V, or V_{in}, ≥ V_{cc} - 0.2 V	L-version
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = -4 mA	

NOTE: 1. Typical values are at V_{CC} = 5.0 V, T_A = +25°C and specified loading.

■ DC CHARACTERISTICS for HM62832H (T_A = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions	Note
Input Leakage Current	$\|I_{LI}\|$	—	—	2	μA	V_{in} = V_{SS} to V_{CC}	
Output Leakage Current	$\|I_{LO}\|$	—	—	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	
Operating Power Supply Current	I_{CC}	—	60	120	mA	Min. cycle, duty = 100%, $\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA	
Standby Power Supply Current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}	
Standby Power Supply Current	I_{SB1}	—	0.02	2	mA	$\overline{CS}$ ≥ V_{CC} - 0.2V, 0 V ≤ V_{in} ≤ 0.2 V, or V_{in}, ≥ V_{cc} - 0.2 V	
		—	0.006	0.1	mA		L-version
Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA	
	V_{OH}	2.4	—	—	V	I_{OH} = -4 mA	

NOTE: 1. Typical values are at V_{CC} = 5.0 V, T_A = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

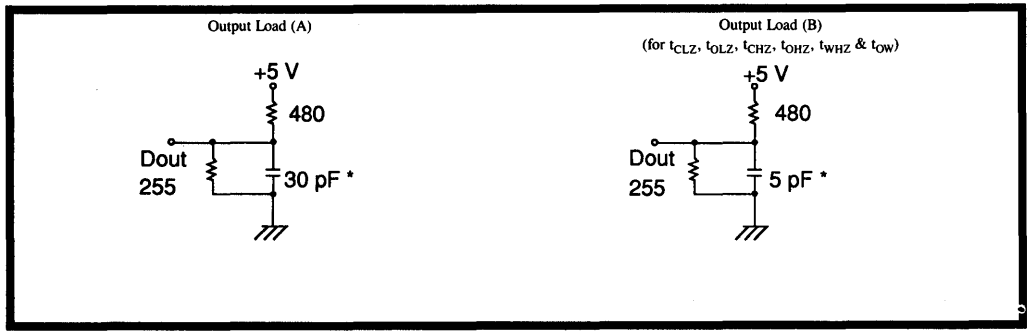
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	—	6	pF	V_{in} = 0 V
Input/Output Capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ = 0 V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.0 V to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See Figures

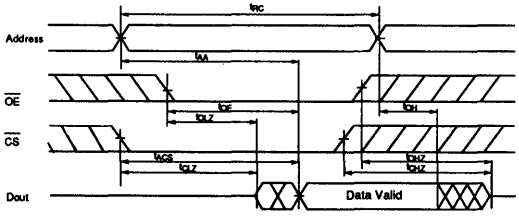


NOTE: *Including scope & jig.

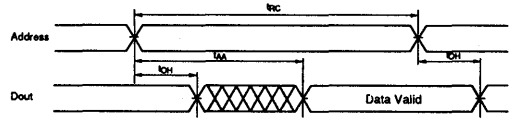
■ Read Cycle

Parameter	Symbol	HM62832H-25		HM62832-35 HM62832H-35		HM62832-45 HM62832H-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	—	45	ns
Output Enable to Output Valid	t_{OE}	—	12	—	15	—	20	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{CLZ}	5	—	5	—	5	—	ns
Output Enable to Output in Low-Z	t_{OLZ}	0	—	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}	0	12	0	15	0	15	ns
Output Disable to Output in High-Z	t_{OHZ}	0	12	0	15	0	15	ns

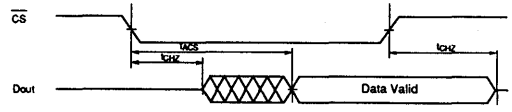
Read Cycle Timing (1) *1



Read Cycle Timing (2) *1, *2, *4



Read Cycle Timing (3) *1, *3, *4



NOTES: *1. $\overline{WE}$ is high for read cycle.

*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.

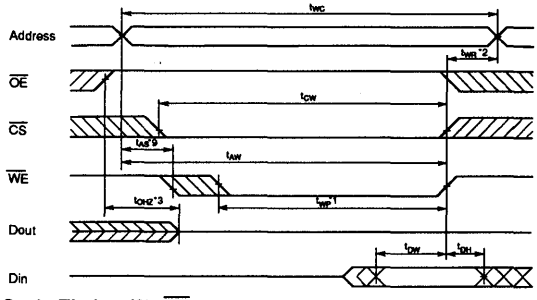
*3. Address should be valid prior to or coincident with $\overline{CS}$ transition low.

*4. $\overline{OE}$ = V_{IL}.

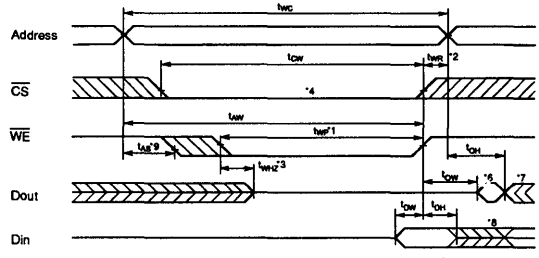
■ Write Cycle

Item	Symbol	HM62832H-25		HM62832-35 HM62832H-35		HM62832-45 HM62832H-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	15	—	20	—	25	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Write to Output in High-Z	t_{WHZ}	0	15	0	15	0	20	ns
Data to Write Time Overlap	t_{DW}	12	—	15	—	20	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns
Output Disable to Output in High-Z	t_{OHZ}	0	12	0	15	0	20	ns
Output Active From End of Write	t_{OW}	5	—	5	—	5	—	ns

Write Cycle Timing (1) ($\overline{OE}$ Clock)



Write Cycle Timing (2) ($\overline{OE}$ Low Fixed)



NOTES:

*1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.

*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

*5. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL}).

*6. D_{out} is in the same phase of written data of this write cycle.

*7. D_{out} is the read data of next address.

*8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O pins.

*9. $\overline{WE}$ must be high during all address transitions except when device is deselected with $\overline{CS}$.

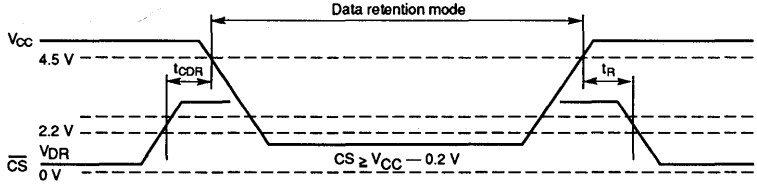
■ Low V_{CC} Data Retention Characteristics (T_A = 0 to +70°C)

This characteristics is guaranteed only for L-version

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{in} \geq V_{CC} - 0.2$ V or 0 V ≤ V_{in} ≤ 0.2 V
Data Retention Current	I_{CCDR}	—	1	50*2	μA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	t_{RC}*1	—	—	ns	

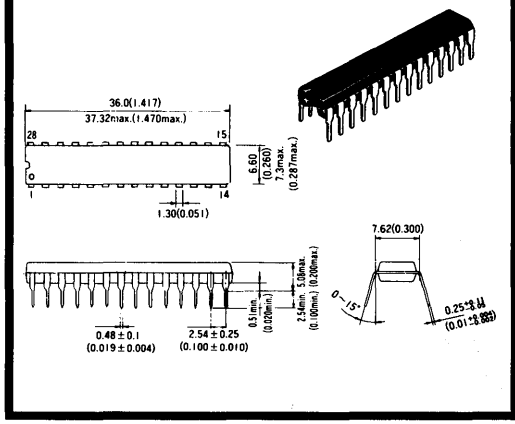
NOTES: *1. t_{RC} = read cycle time.
*2. V_{CC} = 3.0 V.

Low V_{CC} Data Retention Timing Waveform

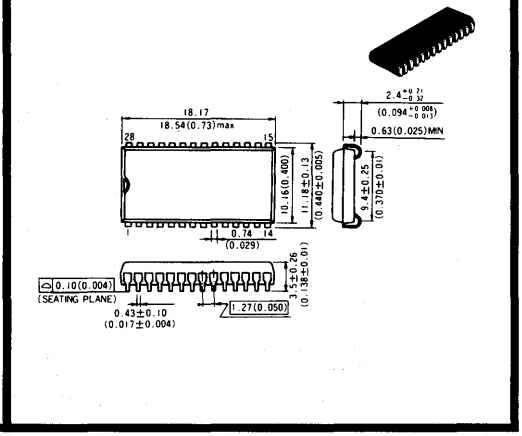


■ PACKAGE DIMENSIONS Unit: mm (inch)

HM62832HP Series
(DP-28NA)
HM62832P/HP



HM62832HJP Series
(CP-28DN)
HM62832JP/HJP

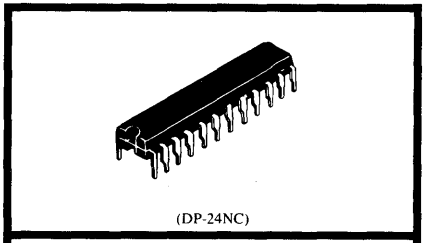


HM6208/HM6208H Series
4-Bit CMOS Static RAM

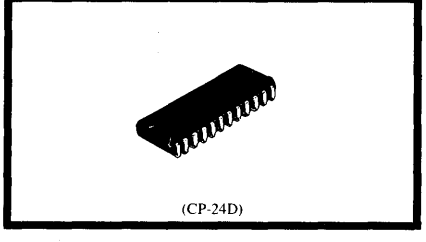
65536-Word × 4-Bit High Speed CMOS Static RAM

The Hitachi HM6208 and HM6208H are high speed 256k static RAMS organized as 64k-word × 4 bit. They realize high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous wherever high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6208 and HM6208H are packaged in the industry standard 300-mil, 24 pin, plastic DIP. The HM6208H is also available in a 300-mil, 24 pin, plastic SOJ package for high density mounting. The low power versions are ideal for battery backed systems.



(DP-24NC)



(CP-24D)

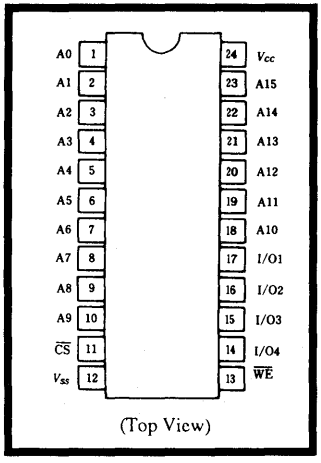
Features

- Single 5 V supply and high density 24-pin package
- High speed: Access time 25/35/45 ns (max.)
- Low power
  - Active: 300 mW (typ.)
  - Standby: 100 μW (typ.)
  - 30 μW (typ.) (L-version)
- Completely static operation requires No clock or timing strobe
- Access and cycle times are equivalent
- All inputs and outputs TTL compatible
- Capability of battery back up operation (L-version)

Ordering Information

Type No.	Access Time	Package
HM6208P-35	35 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6208P-45	45 ns	
HM6208LP-35	35 ns	
HM6208LP-45	45 ns	
HM6208HP-25	25 ns	
HM6208HP-35	35 ns	
HM6208HLP-25	25 ns	
HM6208HLP-35	35 ns	
HM6208HJP-25	25 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6208HJP-35	35 ns	
HM6208HLJP-25	25 ns	
HM6208HLJP-35	35 ns	

Pin Arrangement

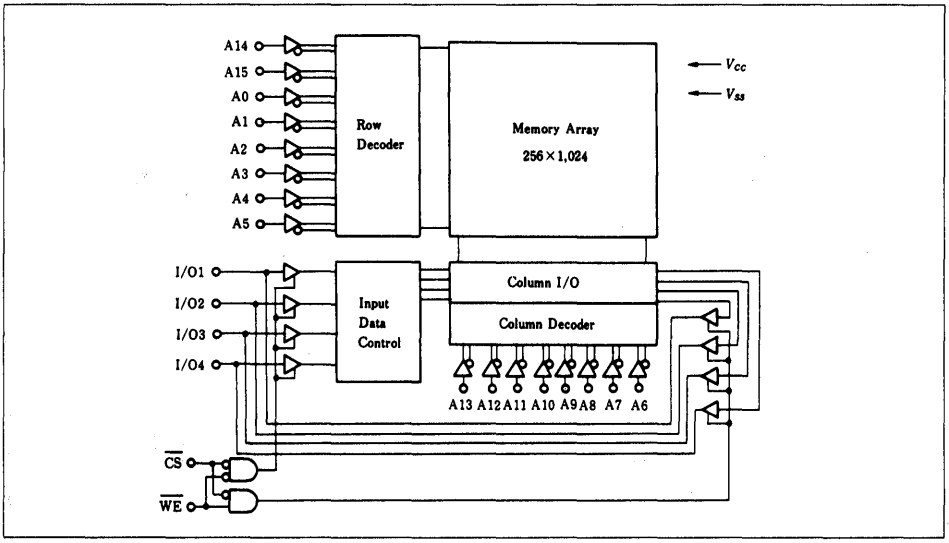


(Top View)

Pin Description

Pin Name	Function
A0 – A15	Address
I/O1 – I/O4	Input/Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle
L	L	Write	Icc	Din	Write cycle

Note: × means don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: *1. Vin min = −2.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	−0.5*1	—	0.8	V

Note: *1. V_{IL} min = −2.0 V for pulse width ≤ 10 ns.

■ DC Characteristics (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	—	2.0	μA	V_{CC} = Max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current	I_{LO}	—	—	10.0	μA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	—	60	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. Cycle, Duty = 100%
Standby Power Supply Current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, Min. Cycle
Standby Power Supply Current "H" Version	I_{SB}	—	20	40	mA	
Standby Power Supply Current	I_{SB1}	—	20	2000	μA	$\overline{CS}$ ≥ V_{CC} − 0.2 V 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} − 0.2V
Standby Power Supply Current L-Version	I_{SB1}	—	6	100	μA	
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = −4.0 mA

Note: *1. Typical limits are at V_{CC} = 5.0 V, T_a = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1MHz)*1

Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Input/output capacitance	C$_{I/O}$	—	10	pF	V$_{I/O}$ = 0 V

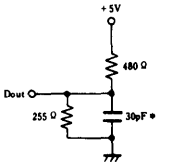
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

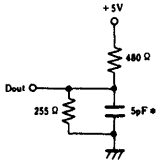
Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels : 1.5 V
- Output load: See Figures

Output Load (A)



Output Load (B)
(for tHZ, tLZ, twz & tow)



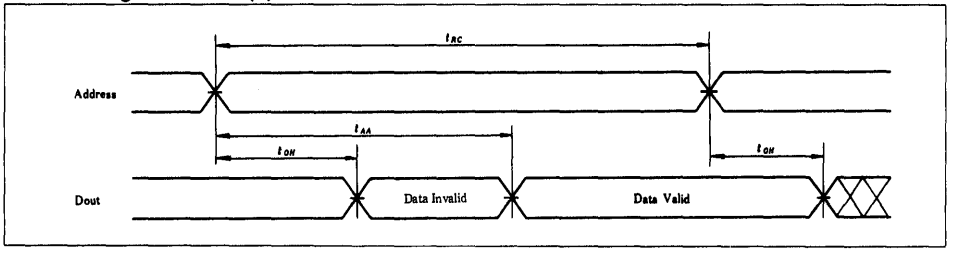
Note: * Including scope & jig.

Read Cycle

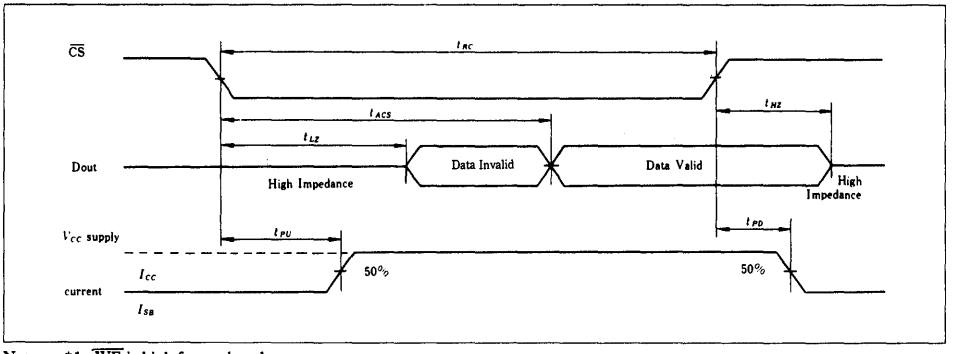
Item	Symbol	HM6208H-25		HM6208-35 HM6208H-35		HM6208-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	—	45	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}*1	5	—	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}*1	0	12	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	15	—	25	—	30	ns

Note: *1 Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



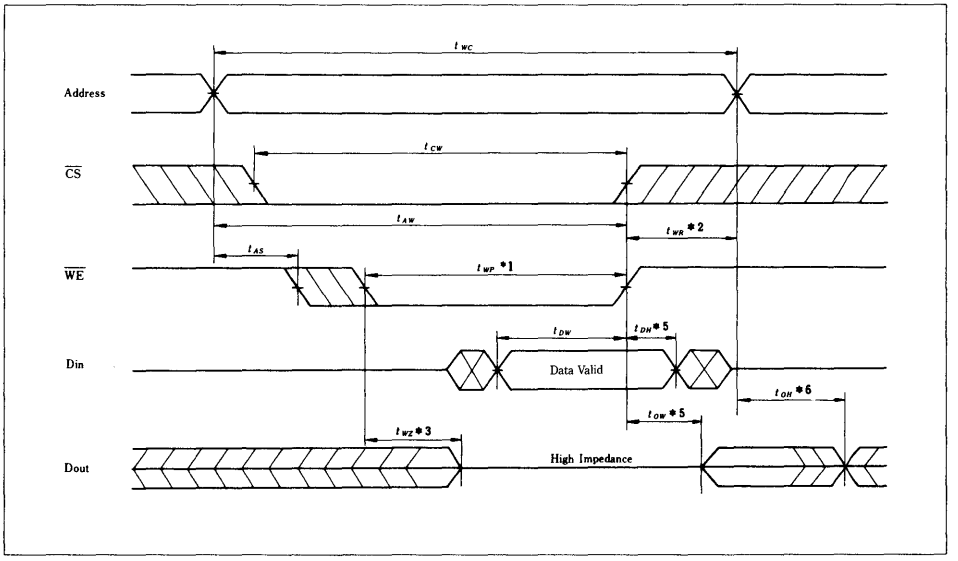
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

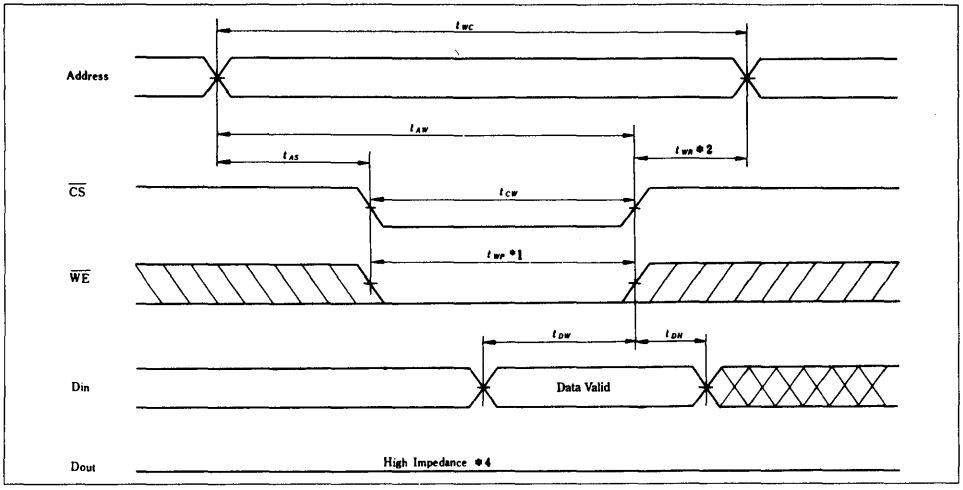
Item		Symbol	HM6208H-25		HM6208-35 HM6208H-35		HM6208-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time		t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write		t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write		t_{AW}	20	—	30	—	40	—	ns
Address Setup Time		t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width		t_{WP}	20	—	30	—	35	—	ns
	"H" Version				25				
Write Recovery Time		t_{WR}	3	—	3	—	3	—	ns
Data Valid to End of Write		t_{DW}	15	—	20	—	20	—	ns
Data Hold Time		t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High-Z		t_{WZ}*1	0	8	0	10	0	15	ns
Output Active From End of Write		t_{OW}*1	0	—	0	—	0	—	ns

Note: *1 Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



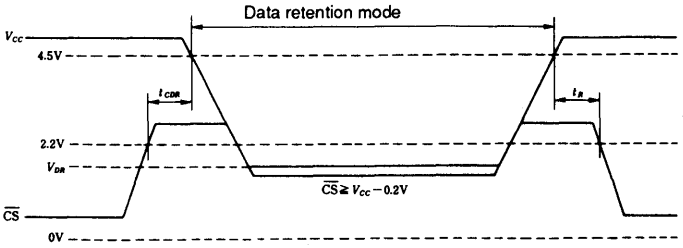
Low V_{CC} Data Retention Characteristics (T_a = 0 to +70°C)

These characteristics are guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, Vin ≥ Vcc – 0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	1	50 *2	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	t_{RC} *1	—	—	ns	

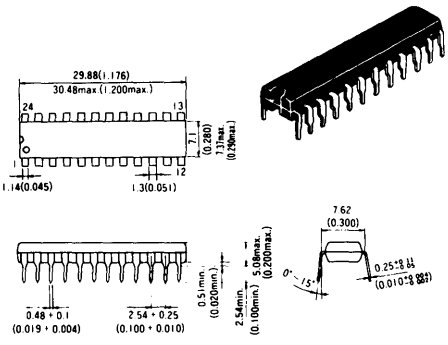
Notes: *1. t_{RC} = read cycle time.
*2. V_{CC} = 3.0 V.

Low Vcc Data Retention Timing Waveform

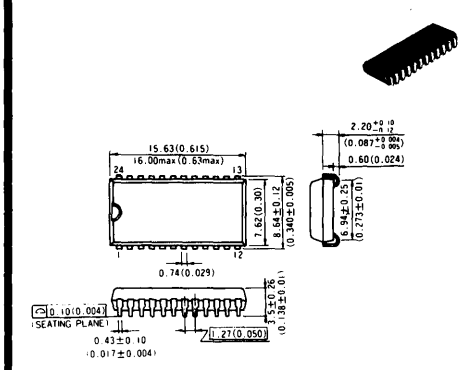


■ PACKAGE DIMENSIONS Unit: mm (inch)

HM6208/HM6208HP Series
(DP-24NC)



HM6208HJP Series
(CP-24D)



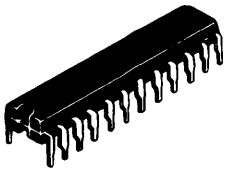
HM6708 Series

65536-word x 4-bit High Speed Hi-BiCMOS Static RAM

Features

- Super Fast Access Time : 20/25ns (max.)
- Low Power Dissipation
  Operating: 350mW (typ.) (f = 50MHz)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6708P



(DP-24NC)

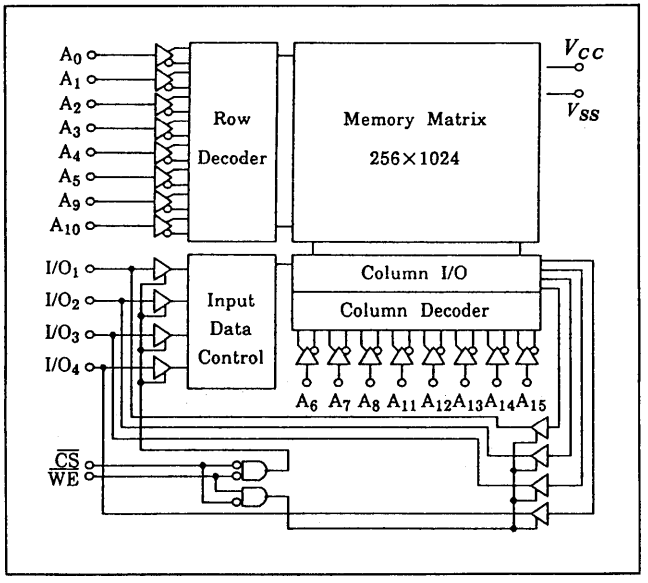
HM6708JP

(CP-24D)

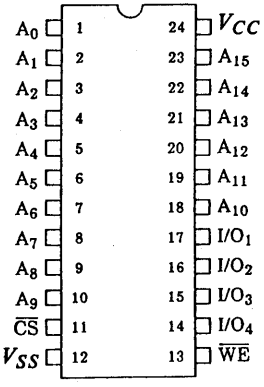
Ordering Information

Type No.	Access Time	Package
HM6708P-20	20ns	300mil 24 pin
HM6708P-25	25ns	Plastic DIP
HM6708JP-20	20ns	300 mil
HM6708JP-25	25ns	24 pin SOJ

Block Diagram



Pin Arrangement



(Top View)

Note) The specifications of this device are subject to change without notice.
Please contact Hitachi's Sales Dept. regarding specifications.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −3.0 V for pulse width 20ns.

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle

DC and Operating Characteristics (V_{CC} = 5 V ±10%, T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	µA	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	µA	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min. Cycle, Duty: 100%, $I_{I/O}$ = 0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}
	I_{SB1}	–	–	10	mA	$\overline{CS} \geqq V_{CC}-0.2$ V $V_{IN} \leqq 0.2$ V or $V_{IN} \geqq V_{CC}-0.2$V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4 mA

Capacitance (T_a = 25°C, f = 1 MHz)

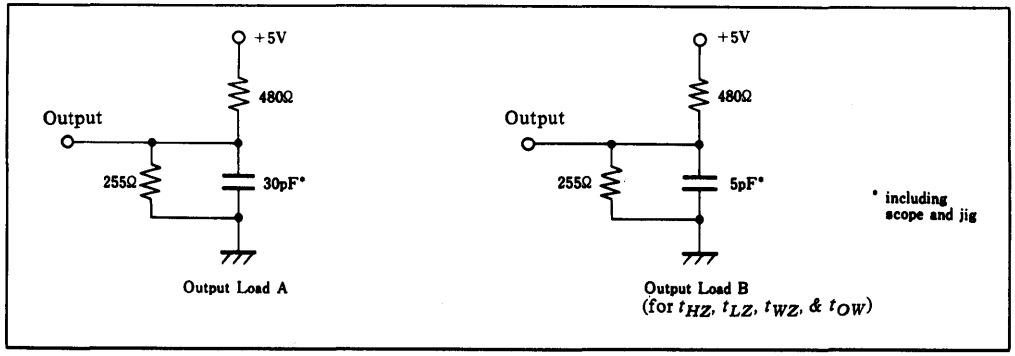
Item	Symbol	max.	Unit	Test Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0 V
Input/Output Capacitance	$C_{I/O}$	10.0	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ±10%, T_a = 0 to +70°C, unless otherwise noted)

AC Test Conditions

- Input pulse levels : V_{SS} to 3.0 V
- Input timing reference levels : 1.5 V
- Output Load : See Figure
- Input rise and fall times : 4 ns
- Output reference levels : 1.5 V

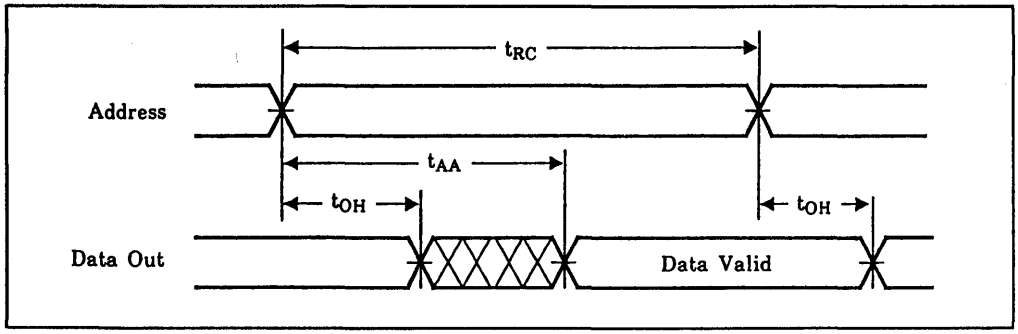


Read Cycle

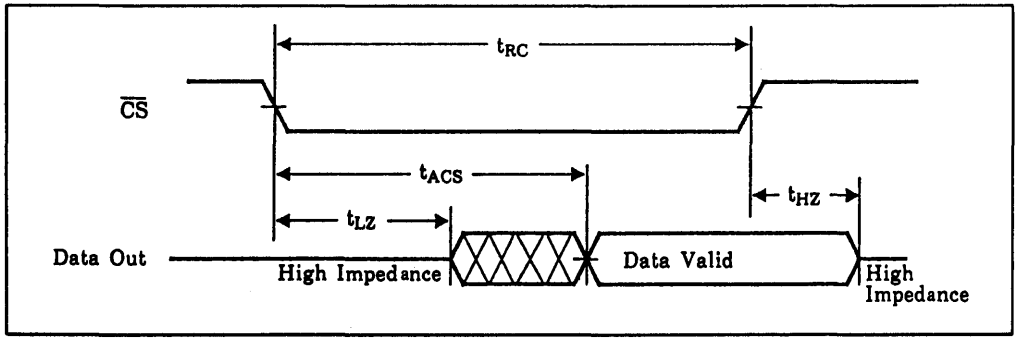
Item	Symbol	HM6708-20		HM6708-25		Unit	Notes
		min.	max.	min.	max.		
Read Cycle Time	t_{RC}	20	–	25	–	ns	–
Address Access Time	t_{AA}	–	20	–	25	ns	–
Chip Select Access Time	t_{ACS}	–	20	–	25	ns	–
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	–
Chip Selection to Output in Low Z	t_{LZ}	0	–	0	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	8	0	10	ns	1, 2

Note) 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.

Read Cycle-1*1,*2



Read Cycle-2*1,*3



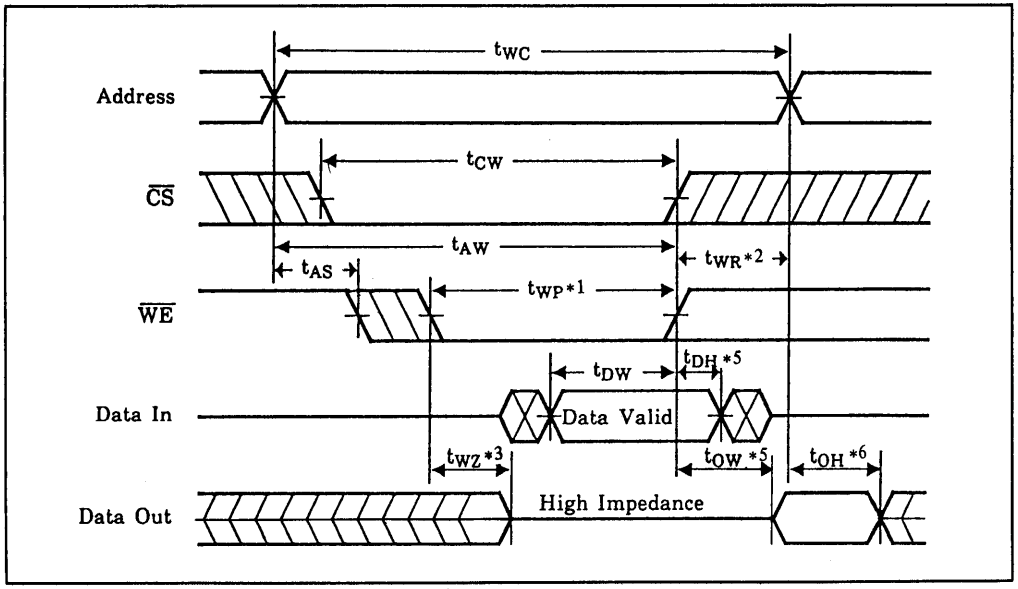
Notes) *1. $\overline{WE}$ is High for Read cycle.
*2. Device is continuously selected, $\overline{CS} = V_{IL}$.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

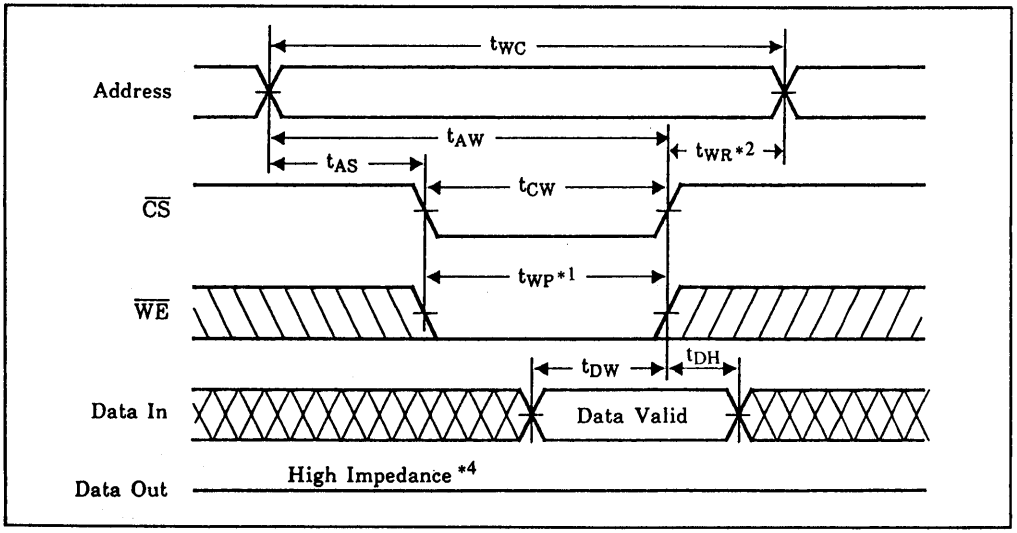
Item	Symbol	HM6708-20		HM6708-25		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	20	–	25	–	ns	2
Chip Selection to End of Write	t_{CW}	15	–	20	–	ns	–
Address Valid to End of Write	t_{AW}	15	–	20	–	ns	–
Address Setup Time	t_{AS}	0	–	0	–	ns	–
Write Pulse Width	t_{WP}	15	–	20	–	ns	–
Write Recovery Time	t_{WR}	3	–	3	–	ns	–
Data Valid to End of Write	t_{DW}	12	–	15	–	ns	–
Data Hold Time	t_{DH}	0	–	0	–	ns	–
Write Enable to Output in High Z	t_{WZ}	0	8	0	10	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

Note) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

Write Cycle-1 ($\overline{WE}$ Controlled)



Write Cycle-2 ($\overline{CS}$ Controlled)



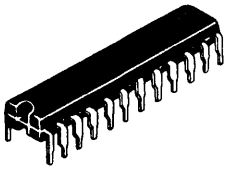
Note) *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. (t_{WP})
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
*6. Output is the same phase of write data of this write cycle.

HM6708A Series — Product Preview

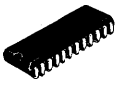
65536-Word × 4-Bit High Speed Static RAM

■ FEATURES

- Super Fast
  Access Time . . . . . .15/20/25ns (max.)
- Low Power Dissipation . . . . . .400mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output



(DP-24NC)

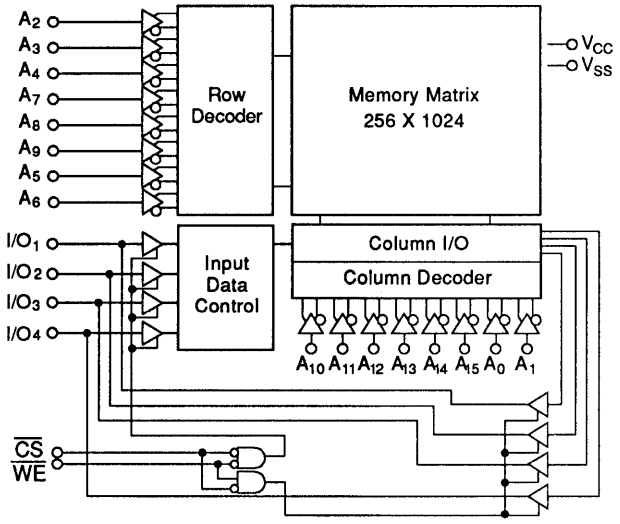


(CP-24D)

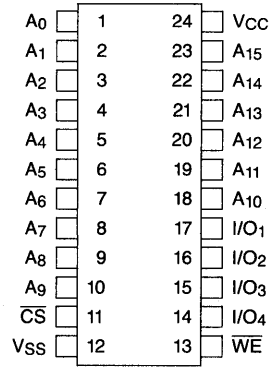
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6708AP-15	15ns	300 mil 24 pin
HM6708AP-20	20ns	Plastic DIP
HM6708AP-25	25ns	(DP-24NC)
HM6708AJP-15	15ns	300 mil 24 pin
HM6708AJP-20	20ns	Plastic SOJ
HM6708AJP-25	25ns	(CP-24D)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_a \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low (Logic 0) Voltage	V_{IL}	−3.0*	—	0.8	V

*Pulse width ≤ 15ns, DC: −0.5V

■ TRUTH TABLE

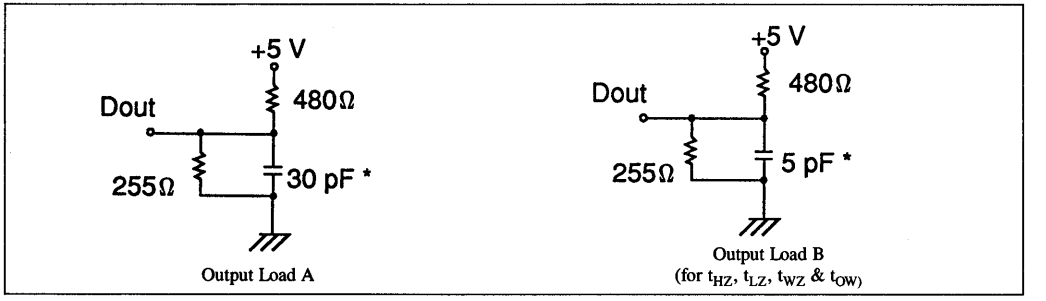
$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2)
L	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2)

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, V_{SS} = 0V)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O}$ = 0mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}	—	—	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} − 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} − 0.2V	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input Timing Reference Levels: 1.5V
- Output Reference Levels: 1.5V
- Input Rise and Fall Times: 4ns
- Output Load: See Figure



Output Load A

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

*Including scope and jig capacitance.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	6.0	pF
Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	10.0	pF

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6708A-15		HM6708A-20		HM6708A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	15	—	20	—	25	—	ns	—
Address Access Time	t_{AA}	—	15	—	20	—	25	ns	—
Chip Select Access Time	t_{ACS}	—	15	—	20	—	25	ns	—
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	ns	—
Chip Selection to Output in Low Z	t_{LZ}	3	—	3	—	3	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	0	10	ns	1, 2

NOTES: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• Write Cycle

Item	Symbol	HM6708A-15		HM6708A-20		HM6708A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	15	—	20	—	25	—	ns	1
Chip Selection to End of Write	t_{CW}	10	—	15	—	20	—	ns	—
Address Valid to End of Write	t_{AW}	10	—	15	—	20	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Write Pulse Width	t_{WP}	10	—	15	—	20	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Data Valid to End of Write	t_{DW}	9	—	12	—	15	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	0	10	ns	2, 3
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	2, 3

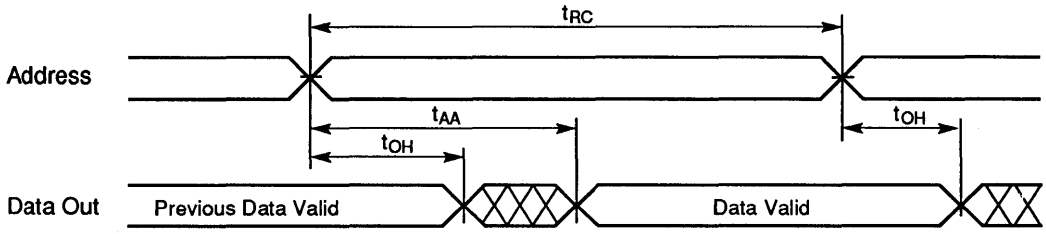
NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.

2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

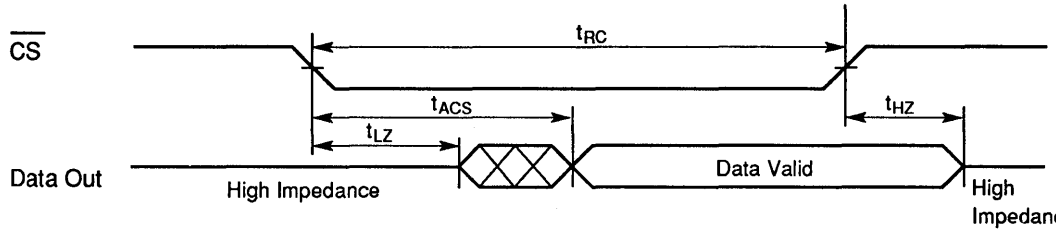
3. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

• **Read Cycle (1)** (1) (2)

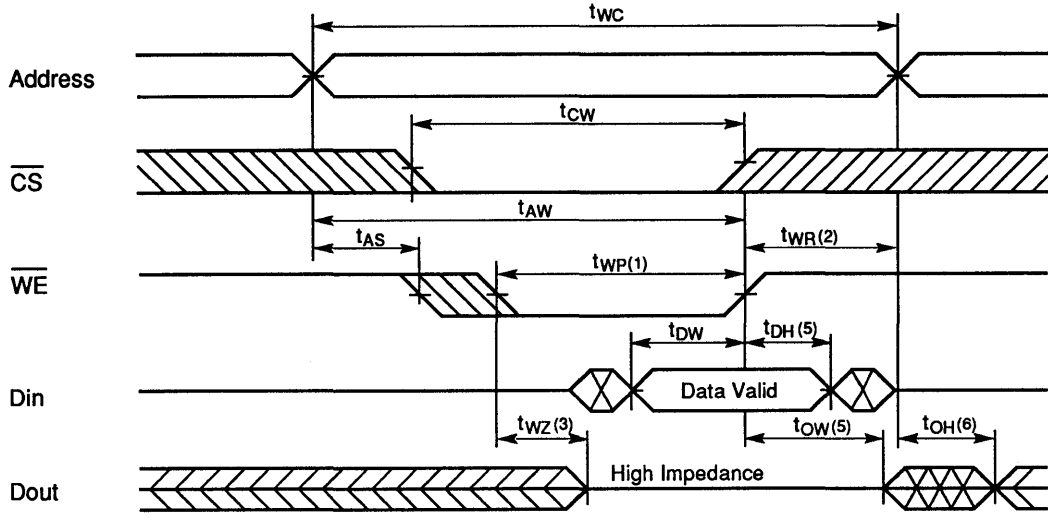


• **Read Cycle (2)** (1) (3)

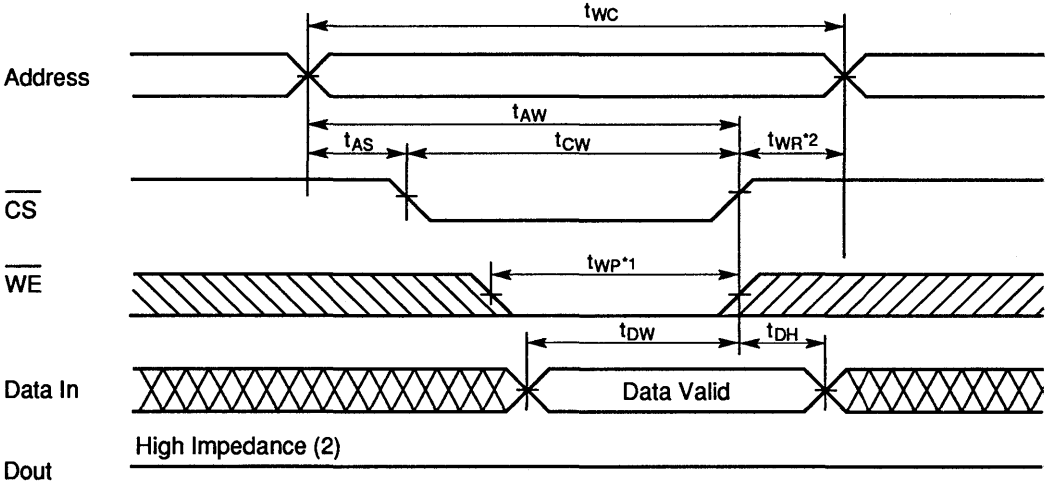


NOTES: 1. $\overline{WE}$ is High for READ cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

• **Write Cycle (1)** ($\overline{WE}$ Controlled)



• **Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTES:

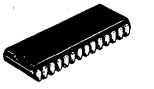
1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. Output data is the same phase of write data of this write cycle.

HM6709 Series — Preliminary

65536-Word × 4-Bit High Speed Static RAM (with $\overline{OE}$)

■ FEATURES

- Super Fast
  Access Time . . . . . .20/25ns (max.)
- Fast $\overline{OE}$
  Access Time . . . . . .10ns (max.)
- Low Power Dissipation . . . . . .350mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output
- 300 mil 28 pin SOJ

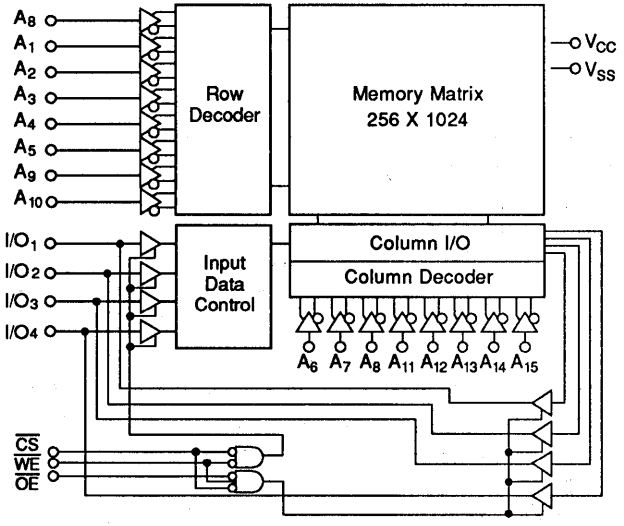


(CP-28DN)

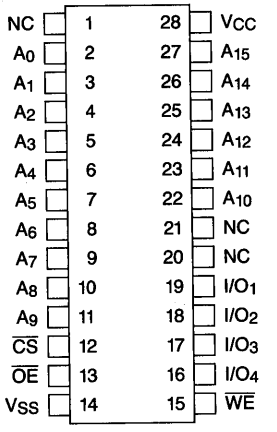
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6709JP-20 HM6709JP-25	20ns 25ns	300 mil 28 pin Plastic SOJ (CP-28DN)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	-10 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_a \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}*	-3.0	—	0.8	V

*Pulse width: 20ns, DC: -0.5V

■ TRUTH TABLE

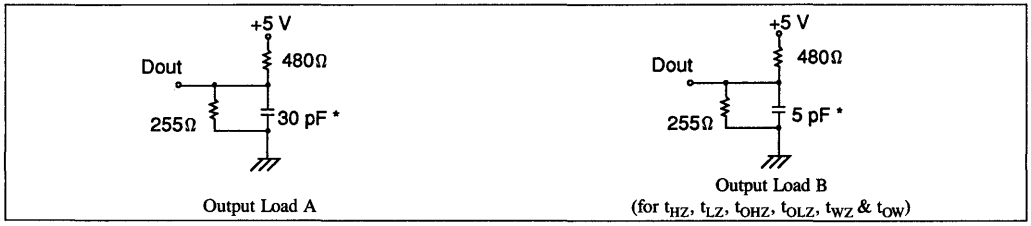
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	—
L	L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data In	Write Cycle (5) (6)

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0°C$ to $70°C$)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	$V_{CC} = 5.5V$, $V_{IN} = V_{SS}$ to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$, $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, $I_{I/O} = 0mA$	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O} = 0mA$	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$, $V_{IN} = V_{IH}$ or V_{IL}	—	—	30	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	—	—	10	mA
Output Low Voltage	V_{OL}	$I_{OL} = 8mA$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4mA$	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Reference Levels: 1.5V
- Input Rise and Fall Time: 4ns
- Output Load: See Figure



Output Load A

Output Load B
(for t_{HZ}, t_{LZ}, t_{OHZ}, t_{OLZ}, t_{WZ} & t_{OW})

*Including scope and jig capacitance.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6709JP-20		HM6709JP-25		Unit	Notes
		Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	20	—	25	—	ns	—
Address Access Time	t_{AA}	—	20	—	25	ns	—
Chip Select Access Time	t_{ACS}	—	20	—	25	ns	—
Chip Selection to Output in Low Z	t_{LZ}	0	—	0	—	ns	1, 2
Output Enable to Output Valid	t_{OE}	0	10	0	10	ns	—
Output Enable to Output in Low Z	t_{OLZ}	0	—	0	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	8	0	10	ns	1, 2
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	—

NOTES: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ±200mV from steady state voltage with specified loading is Load B.

• Write Cycle

Item	Symbol	HM6709JP-20		HM6709JP-25		Unit	Notes
		Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	20	—	25	—	ns	1
Chip Selection to End of Write	t_{CW}	15	—	20	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	ns	—
Address Valid to End of Write	t_{AW}	15	—	20	—	ns	—
Write Pulse Width	t_{WP}	15	—	20	—	ns	—
Write Recovery Time	t_{WR}	3	—	3	—	ns	—
Write to Output in High Z	t_{WZ}	0	8	0	10	ns	2, 3
Data Valid to End of Write	t_{DW}	12	—	15	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	ns	—
Output Disable to Output in High Z	t_{OHZ}	0	8	0	10	ns	2, 3
Output Active from End of Write	t_{OW}	0	—	0	—	ns	2, 3

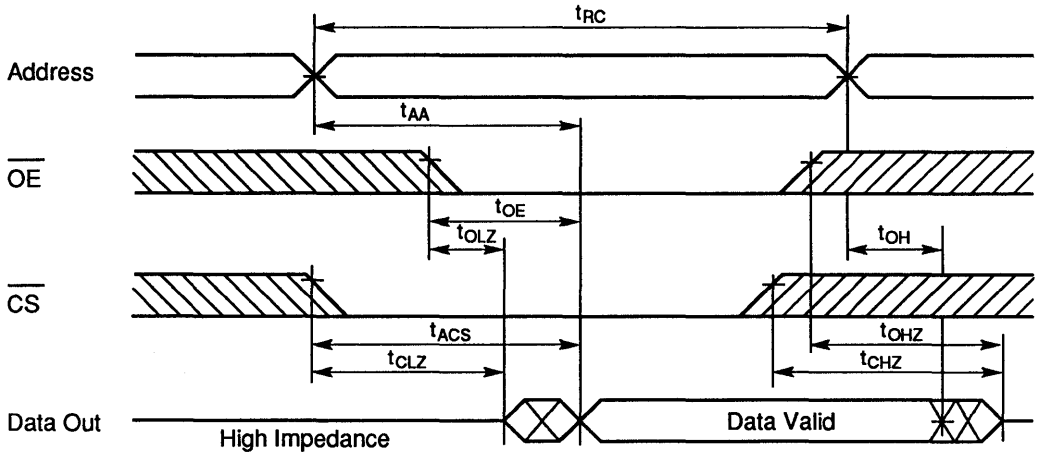
NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.

2. This parameter is sampled and not 100% tested.

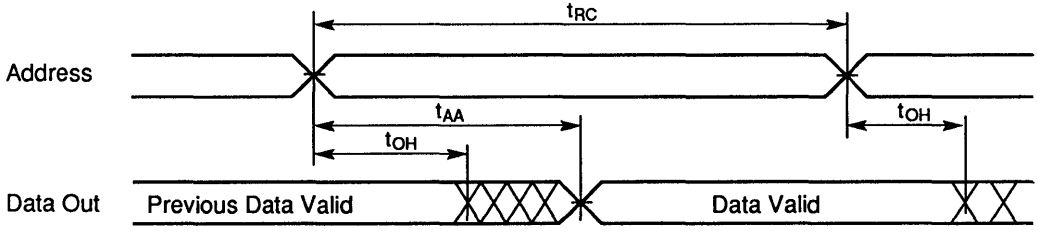
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

■ TIMING WAVEFORM

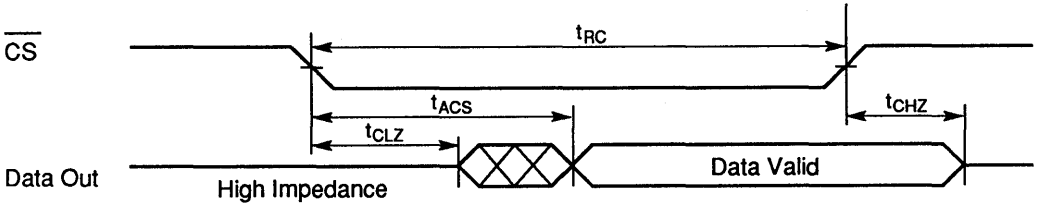
• **Read Cycle (1)** (1)



• **Read Cycle (2)** (1) (2) (3)

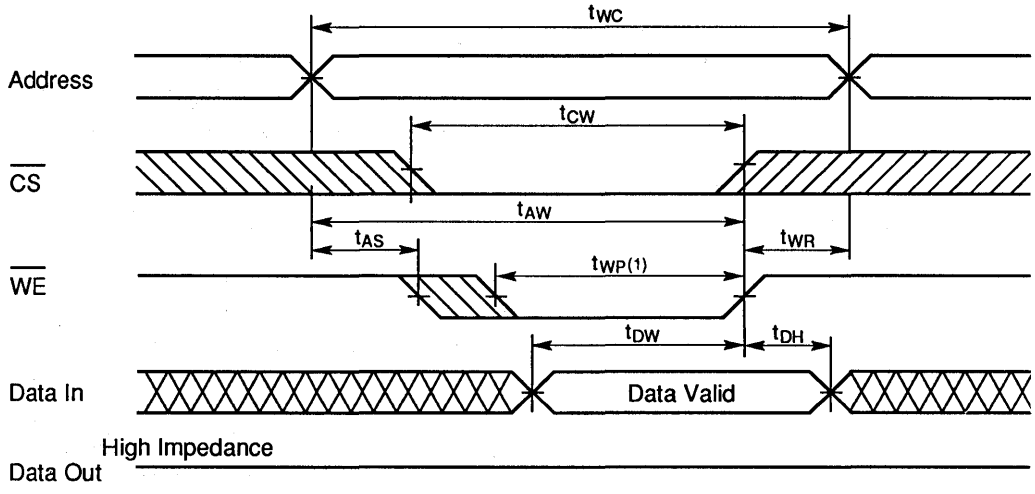


• **Read Cycle (3)** (1) (3) (4)

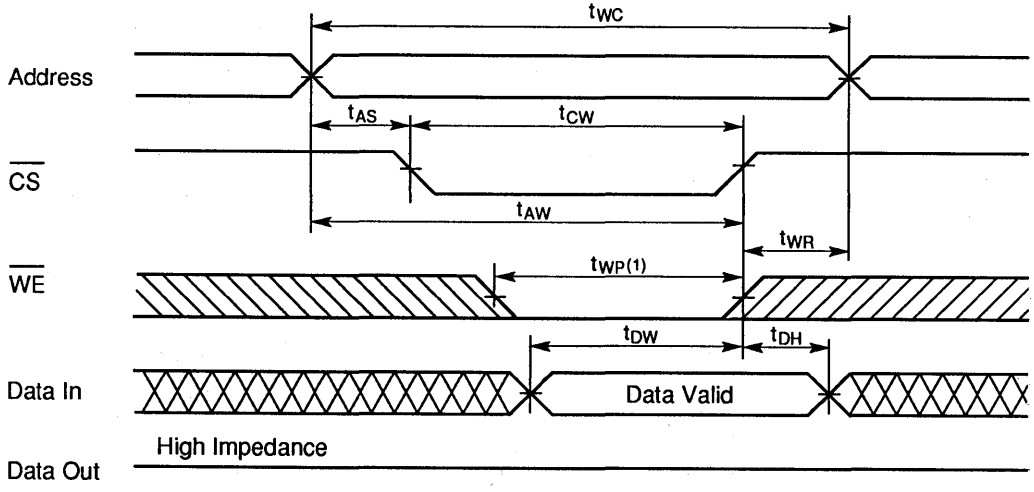


NOTES: 1. $\overline{WE}$ = V_{IH}
2. $\overline{CS}$ = V_{IL}
3. $\overline{OE}$ = V_{IL}
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

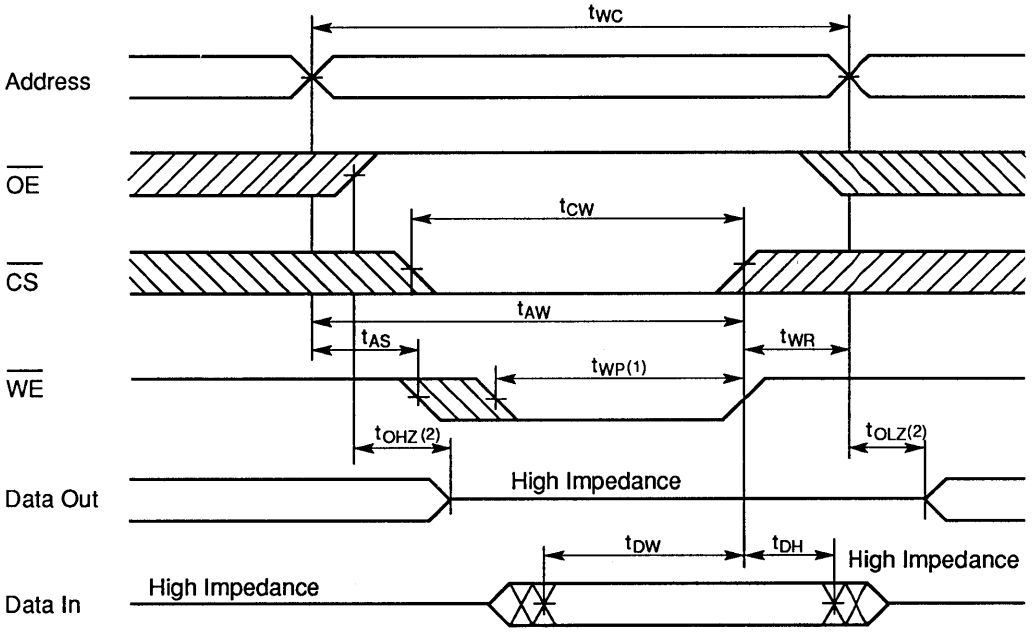
• **Write Cycle (1)** ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



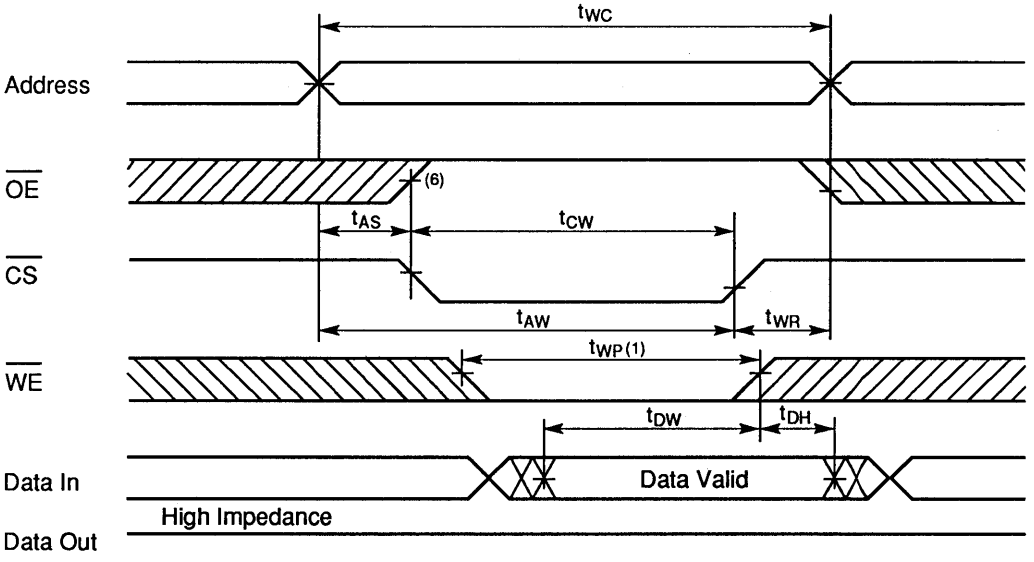
• **Write Cycle (2)** ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



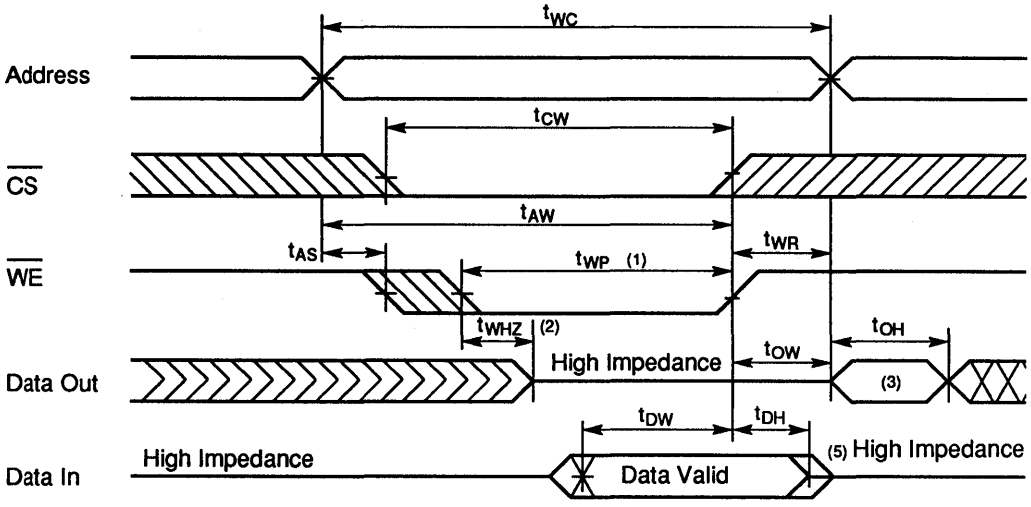
• **Write Cycle (3)** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



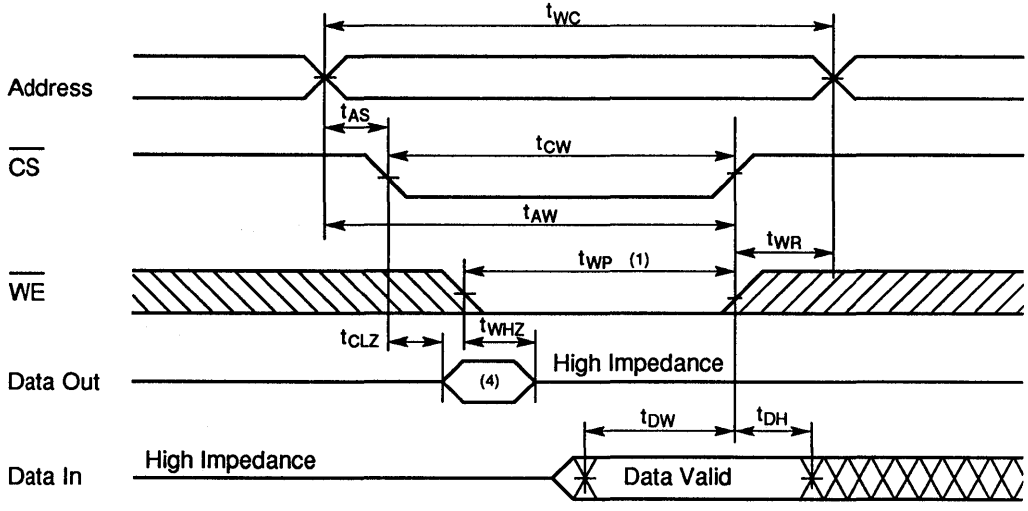
• **Write Cycle (4)** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



• **Write Cycle (5)** ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



• **Write Cycle (6)** ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



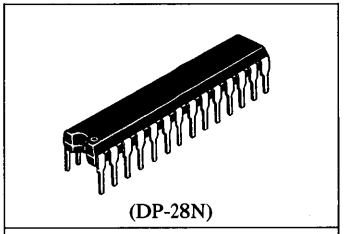
NOTES:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

HM6709A Series — Product Preview

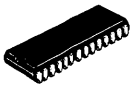
65536-Word × 4-Bit High Speed Static RAM (with $\overline{OE}$)

■ FEATURES

- Super Fast
  Access Time ..... 15/20/25ns (max.)
- Fast $\overline{OE}$
  Access Time..... 8/10/10ns (max.)
- Low Power Dissipation ..... 400mW (typ.)
- + 5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output



(DP-28N)

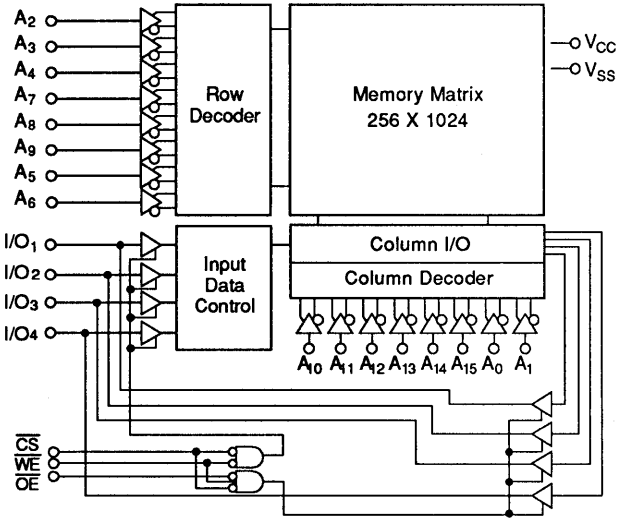


(CP-28DN)

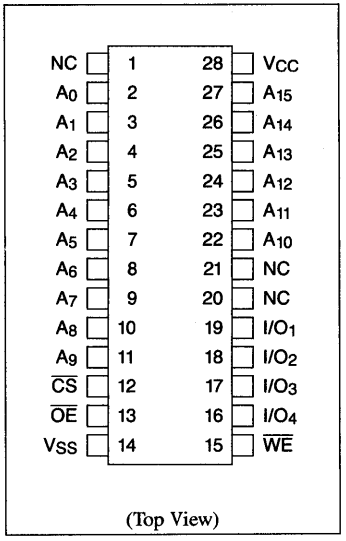
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6709AP-15	15ns	300 mil 28 pin
HM6709AP-20	20ns	Plastic DIP
HM6709AP-25	25ns	(DP-28N)
HM6709AJP-15	15ns	300 mil 28 pin
HM6709AJP-20	20ns	Plastic SOJ
HM6709AJP-25	25ns	(CP-28DN)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_a \le 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}*	−3.0	—	0.8	V

*Pulse width: 15ns, DC: −0.5V

■ TRUTH TABLE

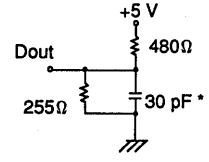
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	H or L	H or L	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	H	Output Disabled	I_{CC}, I_{CC1}	High Z	—
L	L	H	Read	I_{CC}, I_{CC1}	Data Out	Read Cycle (1) (2) (3)
L	H	L	Write	I_{CC}, I_{CC1}	Data In	Write Cycle (1) (2) (3) (4)
L	L	L		I_{CC}, I_{CC1}	Data In	Write Cycle (5) (6)

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

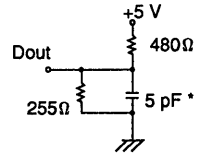
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = V_{SS} to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O}$ = 0mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}	—	—	30	mA
	I_{SB1}	$\overline{CS} \ge V_{CC} - 0.2V$ $V_{IN} \le 0.2V$ or $V_{IN} \ge V_{CC} - 0.2V$	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −4mA	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Reference Levels: 1.5V
- Input Rise and Fall Time: 4ns
- Output Load: See Figure



Output Load A



Output Load B
(for t_{HZ}, t_{LZ}, t_{OHZ}, t_{OLZ}, t_{WZ} & t_{OW})

*Including scope and jig capacitance.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	—	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6709A-15		HM6709A-20		HM6709A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	15	—	20	—	25	—	ns	—
Address Access Time	t_{AA}	—	15	—	20	—	25	ns	—
Chip Select Access Time	t_{ACS}	—	15	—	20	—	25	ns	—
Chip Selection to Output in Low Z	t_{LZ}	3	—	3	—	3	—	ns	1, 2
Output Enable to Output Valid	t_{OE}	0	8	0	10	0	10	ns	—
Output Enable to Output in Low Z	t_{OLZ}	3	—	3	—	3	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	0	10	ns	1, 2
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	ns	—

NOTES: 1. This parameter is sampled and not 100% tested.

2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• Write Cycle

Item	Symbol	HM6709A-15		HM6709A-20		HM6709A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	15	—	20	—	25	—	ns	1
Chip Selection to End of Write	t_{CW}	10	—	15	—	20	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Address Valid to End of Write	t_{AW}	10	—	15	—	20	—	ns	—
Write Pulse Width	t_{WP}	10	—	15	—	20	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Write to Output in High Z	t_{WZ}	0	6	0	8	0	10	ns	2, 3
Data Valid to End of Write	t_{DW}	9	—	12	—	15	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Output Disable to Output in High Z	t_{OHZ}	0	6	0	8	0	10	ns	2, 3
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	2, 3

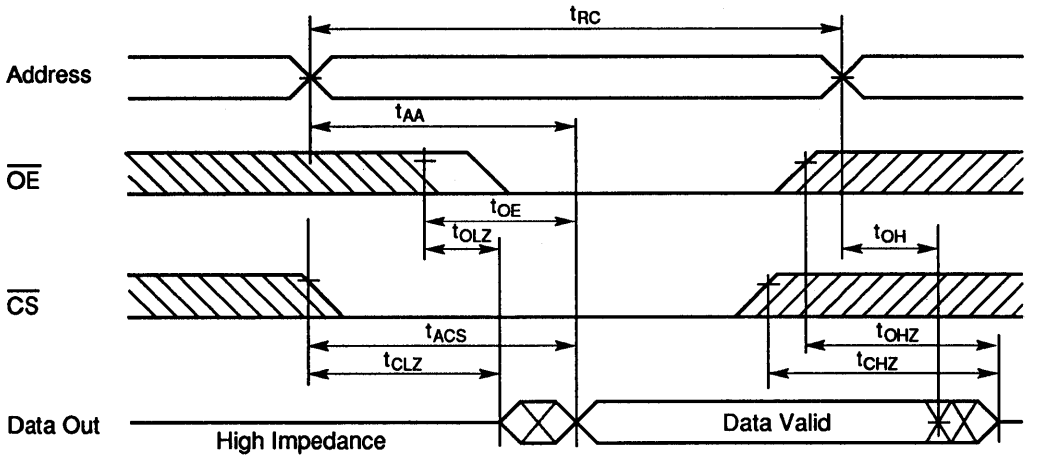
NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.

2. This parameter is sampled and not 100% tested.

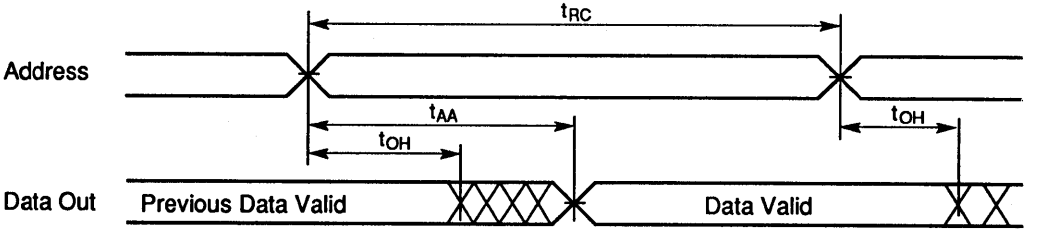
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

■ TIMING WAVEFORM

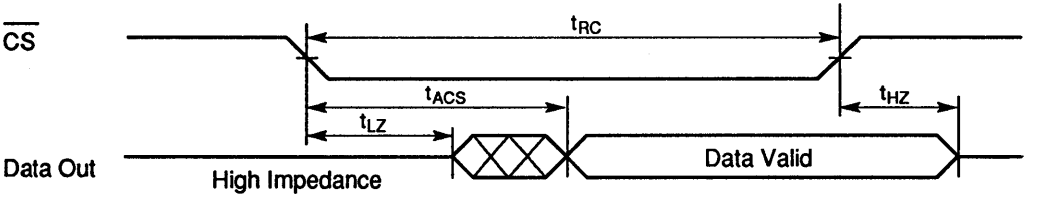
• **Read Cycle (1)** (1)



• **Read Cycle (2)** (1) (2) (3)

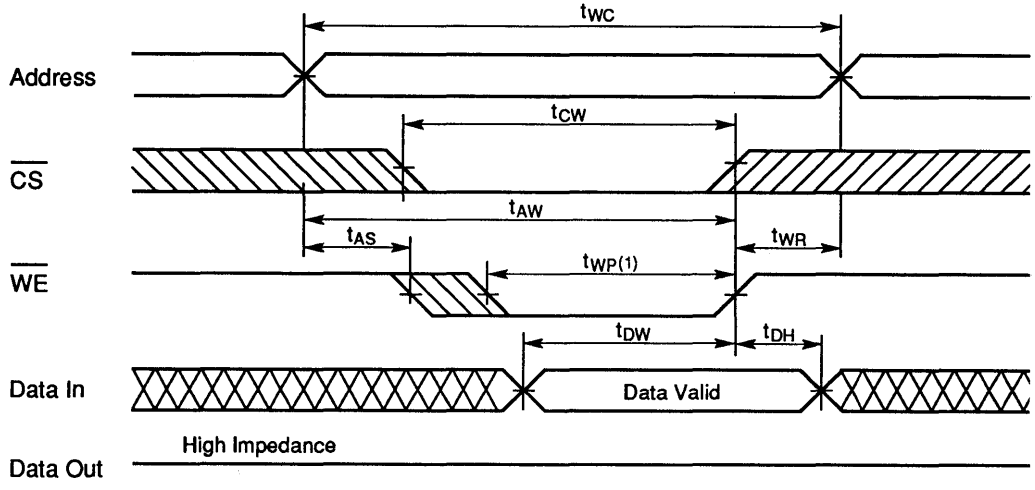


• **Read Cycle (3)** (1) (3) (4)

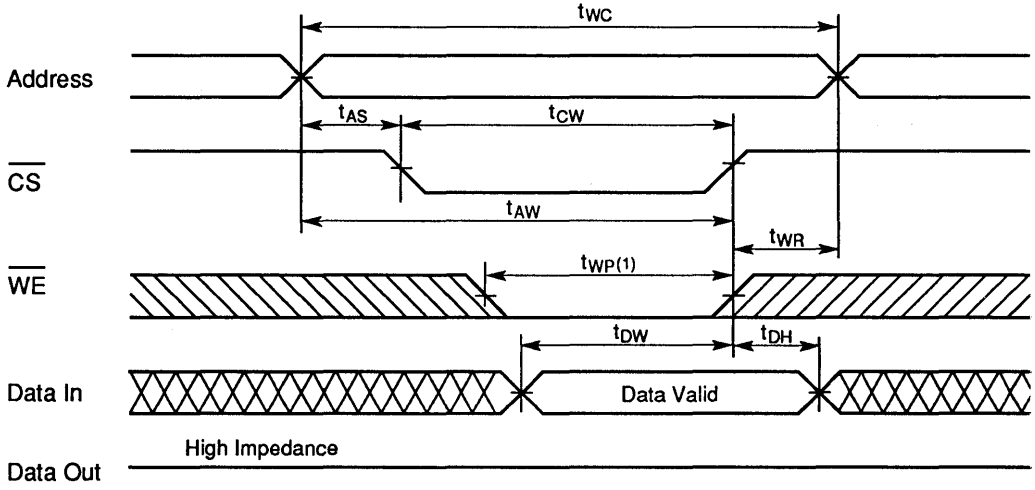


NOTES: 1. $\overline{WE}$ = V_{IH}
2. $\overline{CS}$ = V_{IL}.
3. $\overline{OE}$ = V_{IL}.
4. Address valid prior to or coincident with $\overline{CS}$ transition low.

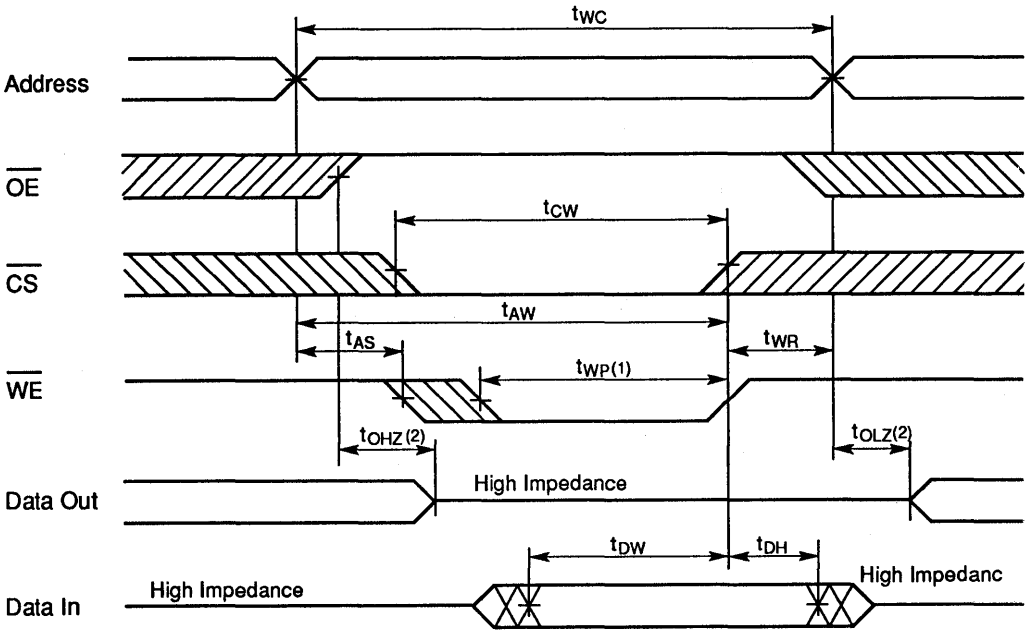
• **Write Cycle (1)** ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



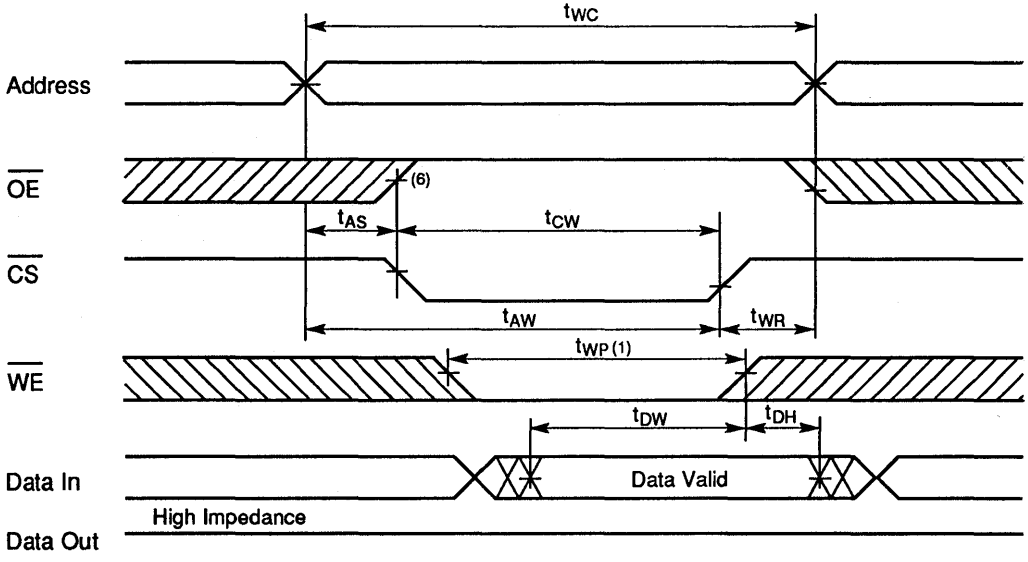
• **Write Cycle (2)** ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



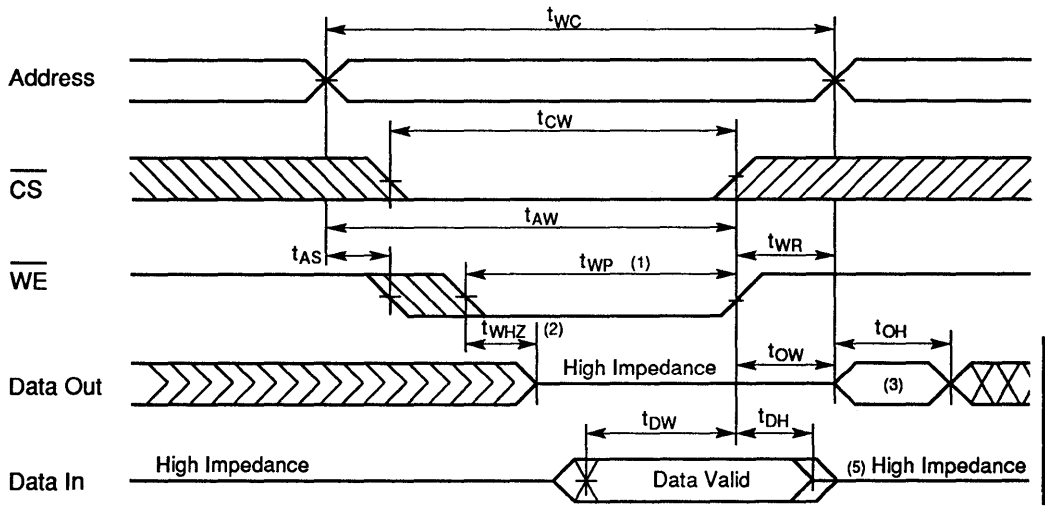
• **Write Cycle (3)** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



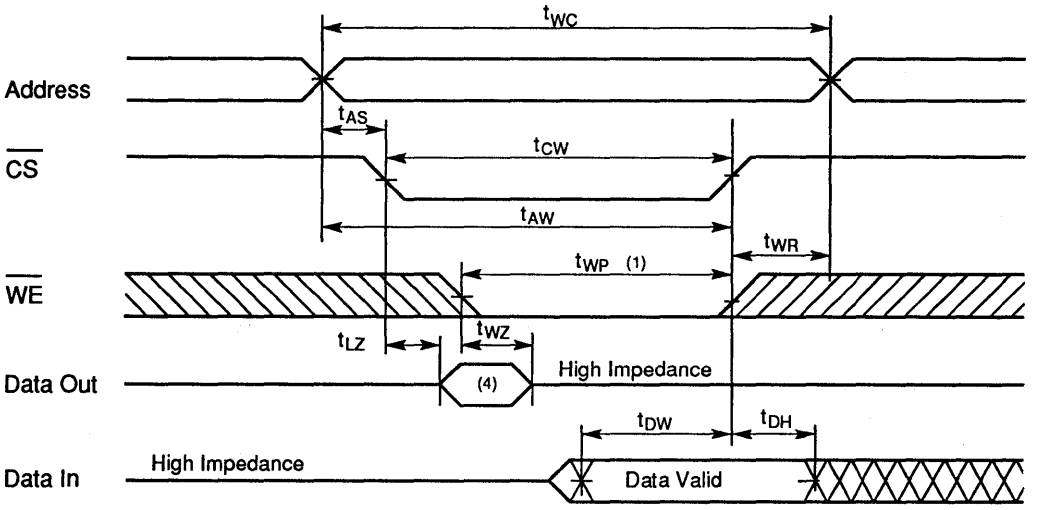
• **Write Cycle (4)** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



• **Write Cycle (5)** ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



• **Write Cycle (6)** ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



NOTES:

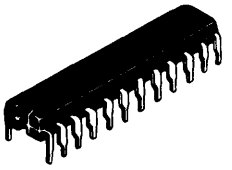
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If the $\overline{CS}$ is low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remain in high impedance state.

HM6207 Series

262144-word x 1-bit High Speed CMOS Static RAM

The Hitachi HM6207 is a high speed 256k static RAM organized as 256-kword x 1-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU. The HM6207, packaged in a 300 mil plastic DIP, is available for high density mounting.

Low power version retains the data with battery back up.



(DP-24NC)

Features

- High Speed: Fast Access Time 35/45 ns (max.)
- Low Power
  - Standby: 100 μW (typ.)/30 μW (typ.) (L-version)
  - Operation: 300 mW (typ.)
- Single 5V Supply and High Density 24 Pin Package
- Completely Static Memory:
  - No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Outputs
- Capability of Battery Back Up Operation (L-version)

Ordering Information

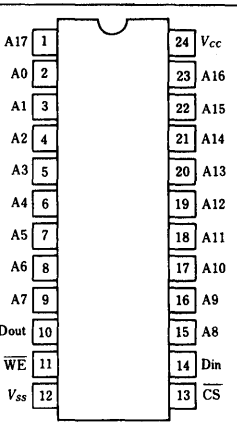
Type No.	Access Time	Package
HM6207P-35	35 ns	300-mil 24-pin Plastic DIP
HM6207P-45	45 ns	
HM6207LP-35	35 ns	
HM6207LP-45	45 ns	

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	−0.5 *1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	Topr	0 to +70	°C
Storage Temperature	Tstg	−55 to +125	°C
Storage Temperature under bias	Tbias	−10 to +85	°C

Note) *1. −2.5V for pulse width ≦ 10ns.

Pin Arrangement

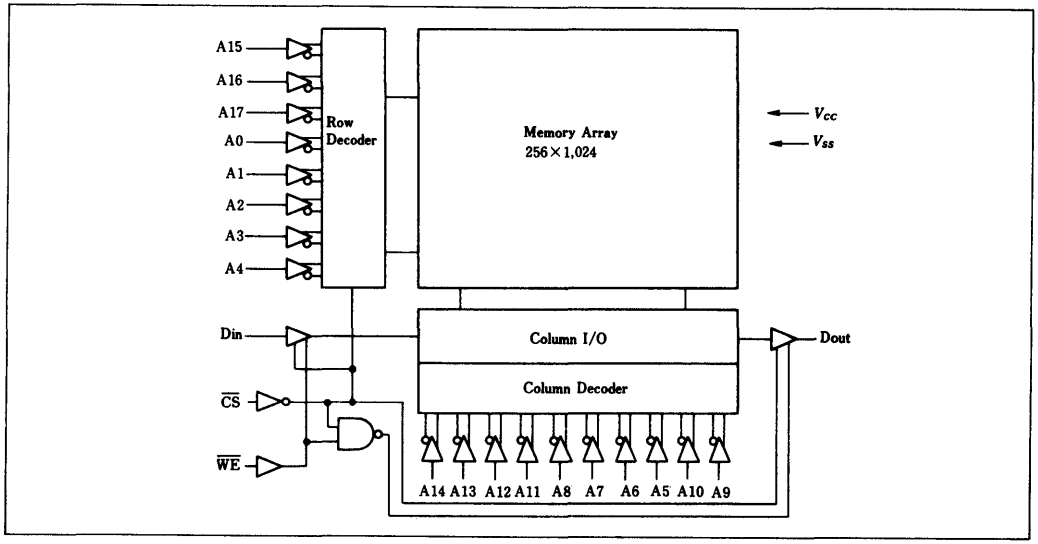


(Top View)

Pin Description

Pin Name	Function
A0 - A17	Address
Din	Data Input
Dout	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	X	NOT SELECTED	I_{SB}, I_{SB1}	HIGH-Z	---
L	H	READ	I_{CC}	Dout	READ CYCLE
L	L	WRITE	I_{CC}	HIGH-Z	WRITE CYCLE

Note) X means don't care.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	–	6.0	V
Input Low (logic 0) Voltage	V_{IL}	−0.5*1	–	0.8	V

Note) *1. −2.0V for pulse width ≦ 10 ns

DC and Operating Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	min	typ*1	max	Unit	Test Condition
Input Leakage Current	$\|I_{LI}\|$	–	–	2.0	μA	V_{CC} = MAX. V_{IN} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10.0	μA	$\overline{CS}$ = V_{IH} Vout = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	60	100	mA	$\overline{CS}$ = V_{IL} Iout = 0mA, min. cycle
Standby Power Supply Current	I_{SB}	–	15	30	mA	$\overline{CS}$ = V_{IH}, min. cycle
Standby Power Supply Current (1)	I_{SB1}	–	0.02	2.0	mA	$\overline{CS} \geqq V_{CC}-0.2V$, $0V \leqq V_{IN} \leqq 0.2V$ or $V_{IN} \geqq V_{CC}-0.2V$
		–	0.006*2	0.1*2		
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = −4.0mA

Note) *1. Typical limits are at V_{CC} = 5.0V, T_a = 25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0MHz)

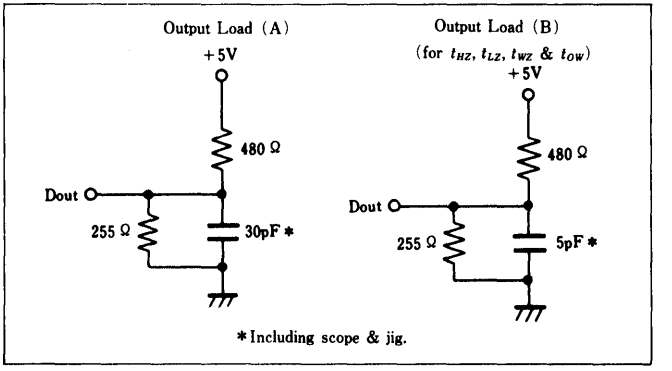
Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Capacitance	Cin	–	–	6.0	pF	Vin = 0V
Output Capacitance	Cout	–	–	10	pF	Vout = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

AC Test Conditions

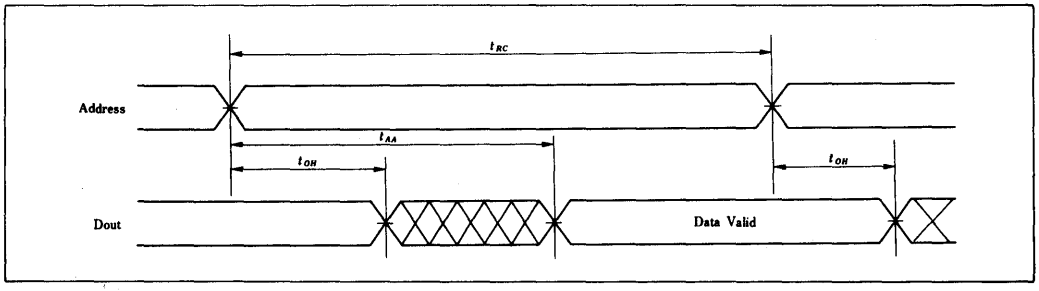
- Input pulse levels: V_{SS} to 3.0V
- Input rise and fall times: 5ns
- Input and Output timing reference levels: 1.5V
- Output load: See Figures.



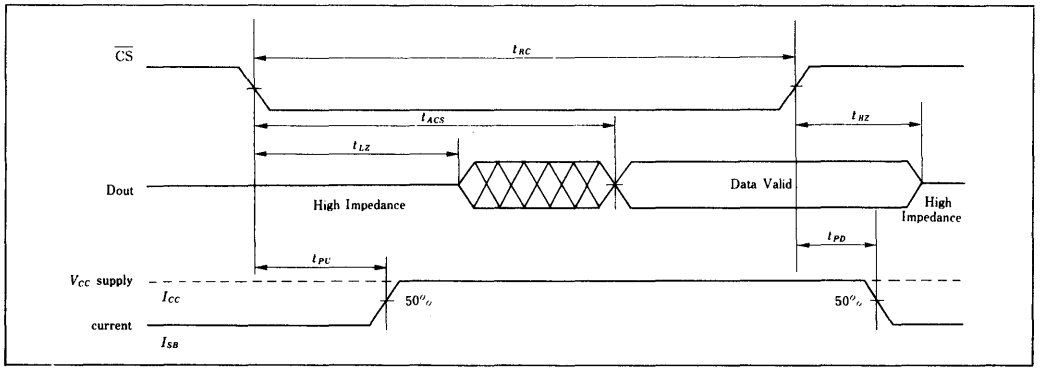
Read Cycle

Parameter	Symbol	HM6207-35		HM6207-45		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	35	–	45	–	ns	*1
Address Access Time	t_{AA}	–	35	–	45	ns	
Chip Select Access Time	t_{ACS}	–	35	–	45	ns	
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	*2, *3, *7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	*2, *3, *7
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns	*7
Chip Deselection to Power Down Time	t_{PD}	–	30	–	40	ns	*7

Timing Waveform of Read Cycle No. 1 *4, *5



Timing Waveform of Read Cycle No. 2 *4, *6

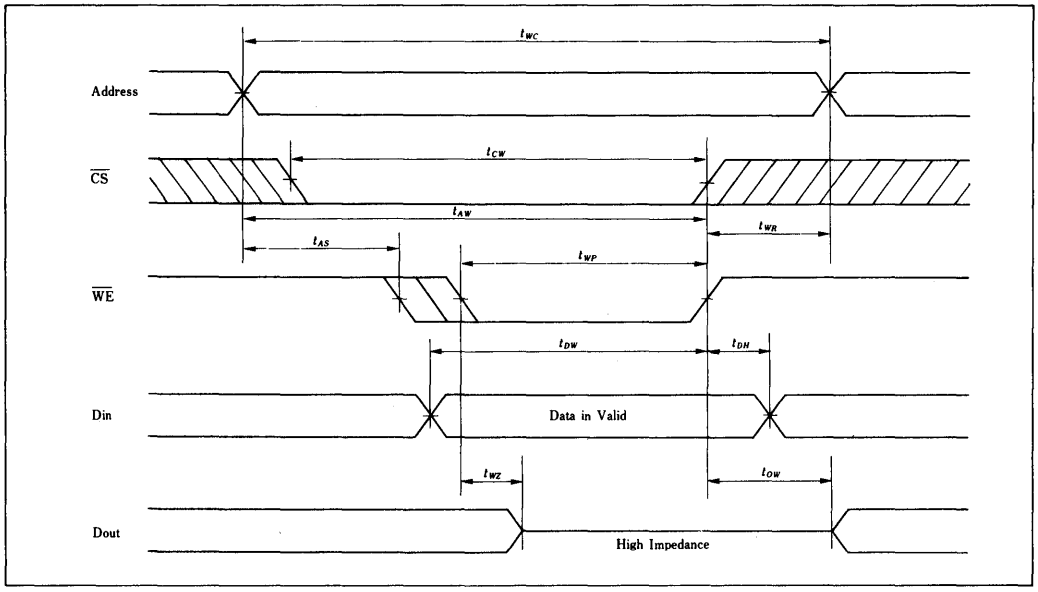


Notes) *1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
*2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
*3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
*4. $\overline{WE}$ is high for READ Cycle.
*5. Device is continuously selected, while $\overline{CS}$ = V_{IL}.
*6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
*7. This parameter is sampled and not 100% tested.

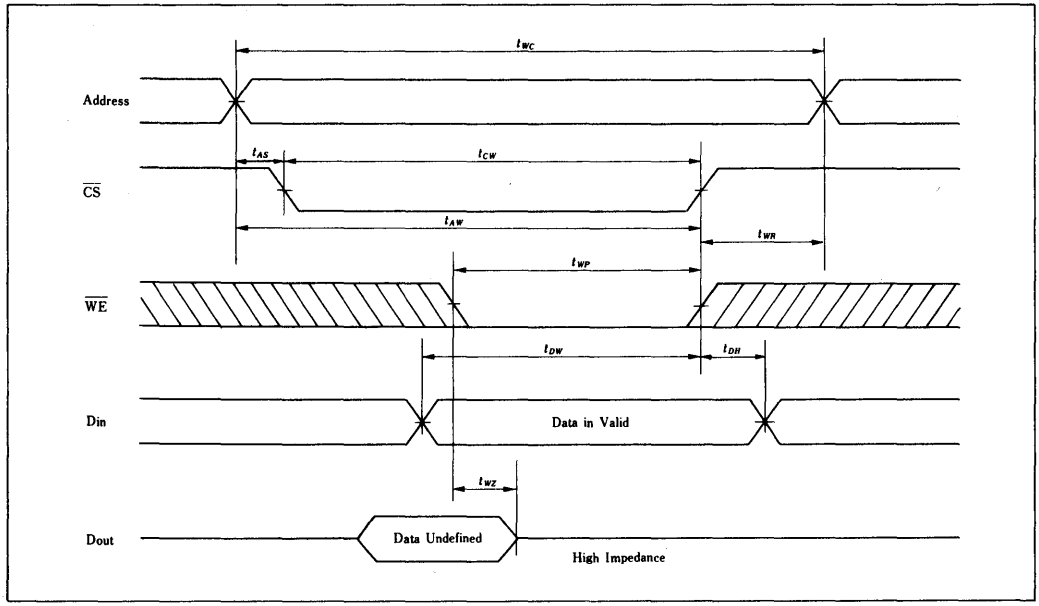
Write Cycle

Parameter	Symbol	HM6207-35		HM6207-45		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	35	–	45	–	ns	*2
Chip Selection to End of Write	t_{CW}	30	–	40	–	ns	
Address Valid to End of Write	t_{AW}	30	–	40	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	25	–	25	–	ns	
Write Recovery Time	t_{WR}	3	–	3	–	ns	
Data Valid to End of Write	t_{DW}	20	–	20	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	20	0	25	ns	*3, *4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	*3, *4

Timing Waveform of Write Cycle No. 1 ($\overline{WE}$ Controlled)



Timing Waveform of Write Cycle No. 2 ($\overline{CS}$ Controlled)



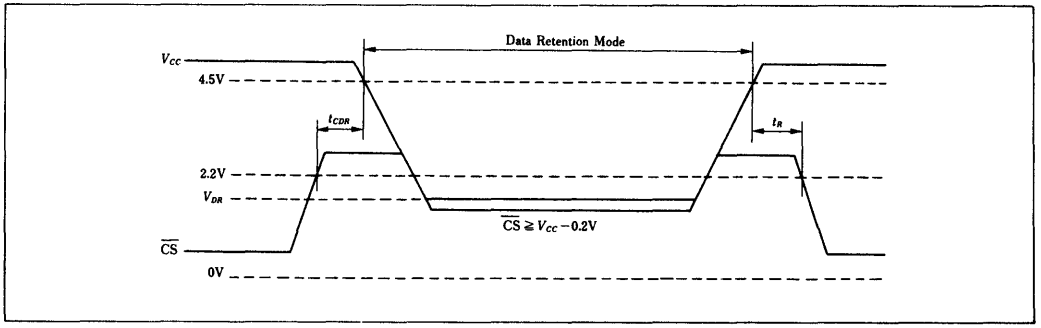
Notes) *1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance states.
*2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
*3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
*4. This parameter is sampled and not 100% tested.

Low V_{CC} Data Retention Characteristics (Ta = 0 to +70°C)
(This characteristics is guaranteed only for L-version)

Parameter	Symbol	min	typ.	max.	Unit	Test Condition
V_{CC} for Data Retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geqq V_{CC} - 0.2V$, $V_{in} \geqq V_{CC} - 0.2V$ or $0V \leqq V_{in} \leqq 0.2V$
Data Retention Current	I_{CCDR}	–	2	50*2	μA	
Chip Deselect to Data Retention Time	t_{CDR}	0	–	–	ns	See retention waveform
Operation Recovery Time	t_R	t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time *2. V_{CC} = 3.0V

Low V_{CC} Data Retention Waveform

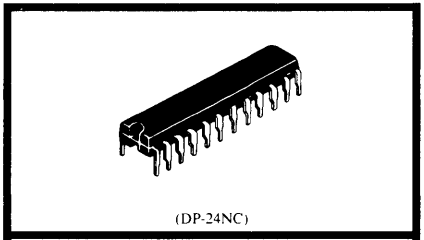


HM6207/HM6207H Series
1-Bit CMOS Static RAM

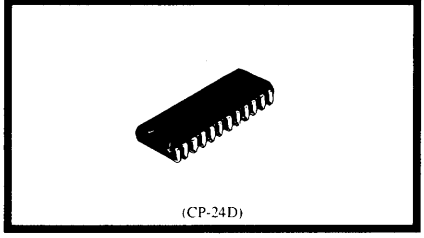
262144-Word × 1-Bit High Speed CMOS Static RAM

The Hitachi HM6207 and HM6207H are high speed 256k static RAMs organized as 256-kword × 1-bit. They realize high speed access time (25/35/45ns) and low power consumption, employing CMOS process technology and high speed circuit design technology. It is most advantageous wherever high speed and high density memory is required.

The HM6207 and HM6207H are packaged in the industry standard 300-mil, 24-pin plastic DIP. The HM6207H is also available in a 300-mil, 25-pin plastic SOJ package for high density mounting. The low power versions are ideal for battery backed systems.



(DP-24NC)



(CP-24D)

Features

- Single 5 V supply and high density 24-pin package
- High speed
  Access time: 25/35/45 ns (max.)
- Low power
  Active: 300 mW (typ.)
  Standby: 100 μW (typ.)
  30 μW (typ.) (L-version)
- Completely static memory requires
  No clock or timing strobe requires
- Equal access and cycle time
- All inputs and outputs TTL compatible
- Capability of battery back up operation (L-version)

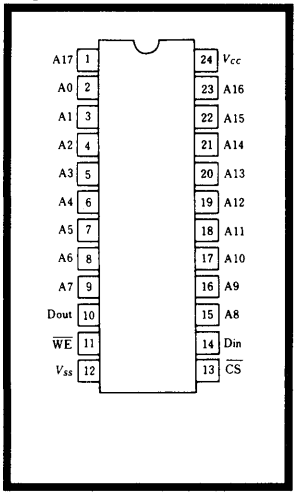
Ordering Information

Type No.	Access Time	Package
HM6207P-35	35 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6207P-45	45 ns	
HM6207HP-25	25 ns	
HM6207HP-35	35 ns	
HM6207HLP-25	25 ns	
HM6207HLP-35	35 ns	
HM6207HJP-25	25 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6207HJP-35	35 ns	
HM6207HLJP-25	25 ns	
HM6207HLJP-35	35 ns	

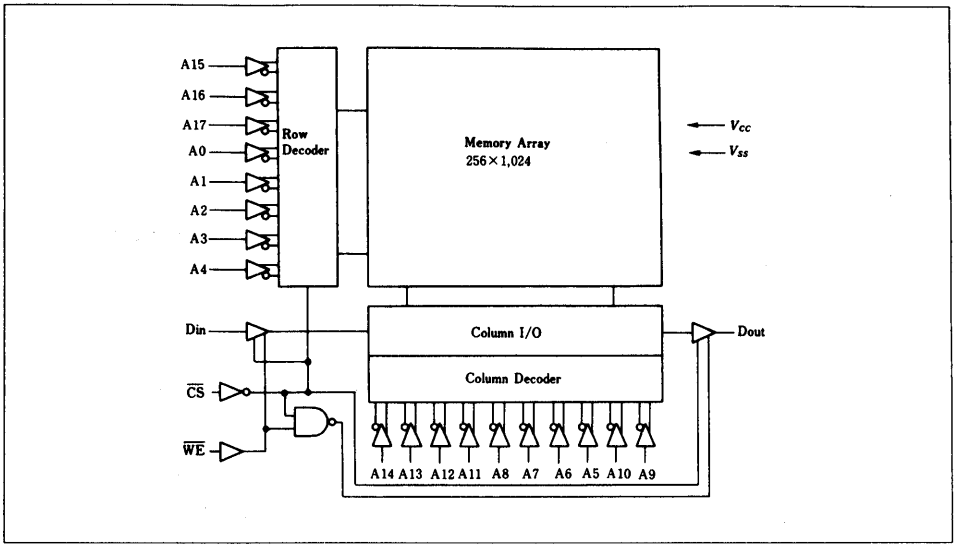
Pin Description

Pin Name	Function
A0 – A17	Address
Din	Data input
Dout	Data output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Pin Arrangement



Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle
L	L	Write	Icc	High-Z	Write cycle

Note: × means don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: *1. Vin min = −2.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	–0.5*1	—	0.8	V

Note: *1. V_{IL} min = –2.0 V for pulse width ≤ 10 ns.

■ DC Characteristics (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item		Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current		$\|I_{LI}\|$	—	—	2.0	μA	V_{CC} = Max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current		$\|I_{LO}\|$	—	—	10.0	μA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current		I_{CC}	—	60	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. Cycle, Duty = 100%
Standby Power Supply Current		I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, Min. Cycle
Standby Power Supply Current	"H" Version	I_{SB}	—	20	40	mA	
Standby Power Supply Current (1)		I_{SB1}	—	20	2000	μA	$\overline{CS}$ ≥ V_{CC} – 0.2 V 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} – 0.2V
Standby Power Supply Current (1)	L-Version	I_{SB1}	—	6	100	μA	
Output Low Voltage		V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage		V_{OH}	2.4	—	—	V	I_{OH} = –4.0 mA

Note: *1. Typical limits are at V_{CC} = 5.0 V, T_a = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1MHz)*1

Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	10	pF	V_{out} = 0 V

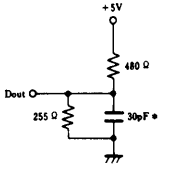
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, unless otherwise noted.)

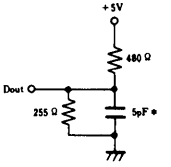
Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels : 1.5 V
- Output load: See Figures

Output Load (A)



Output Load (B)
(for tHZ, tLZ, twz & tow)



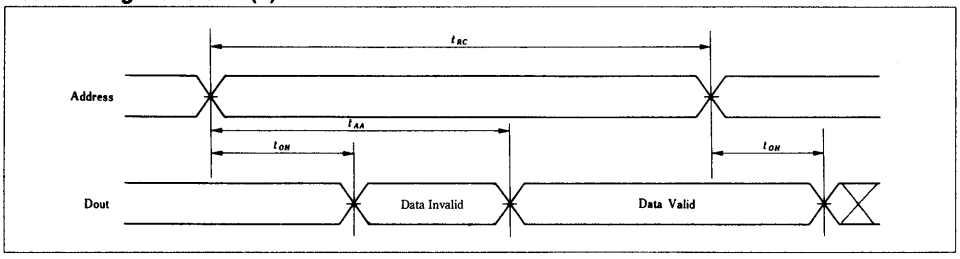
Note: * Including scope & jig.

Read Cycle

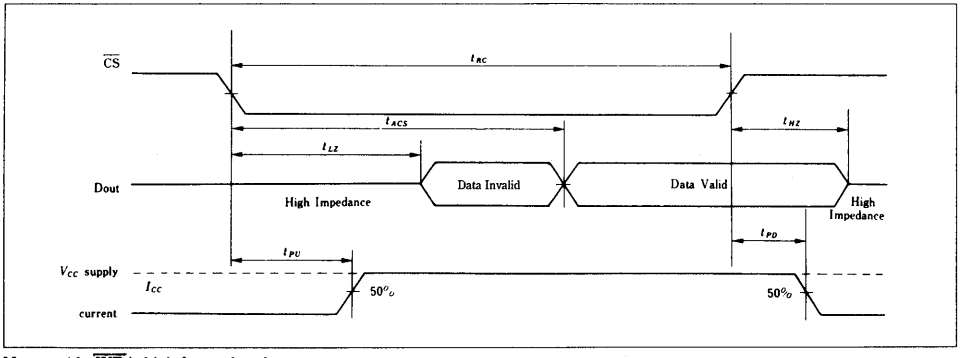
Item	Symbol	HM6207H-25		HM6207-35 HM6207H-35		HM6207-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	—	45	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}*1	5	—	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}*1	0	12	0	20	0	30	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	15	—	25	—	40	ns

Note: *1 Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



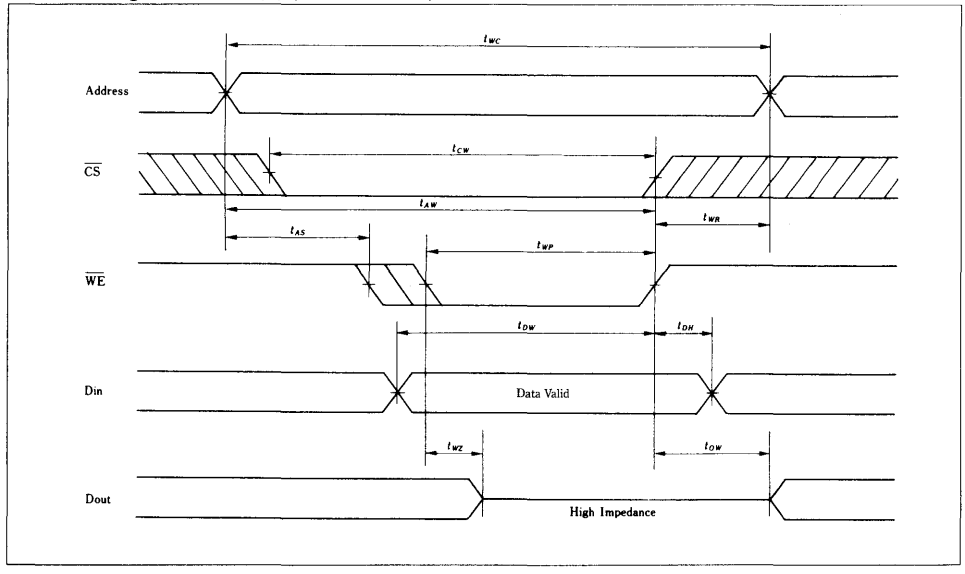
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

■ Write Cycle

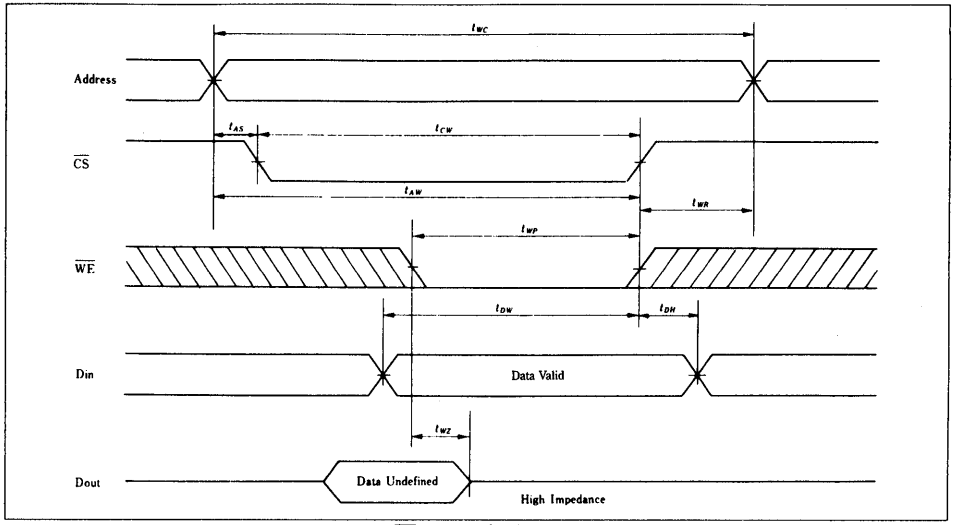
Item		Symbol	HM6207H-25		HM6207-35 HM6207H-35		HM6207-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time		t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write		t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write		t_{AW}	20	—	30	—	40	—	ns
Address Setup Time		t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width		t_{WP}	20	—	30	—	35	—	ns
	"H" Version				25				
Write Recovery Time		t_{WR}	3	—	3	—	3	—	ns
Data Valid to End of Write		t_{DW}	15	—	20	—	20	—	ns
Data Hold Time		t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High-Z		t_{WZ}*1	0	8	0	10	0	15	ns
Output Active From End of Write		t_{OW}*1	0	—	0	—	0	—	ns

Note: *1 Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



Notes: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
*4. Dout is the same phase of write data of this write cycle, if t_{WR} is long enough.

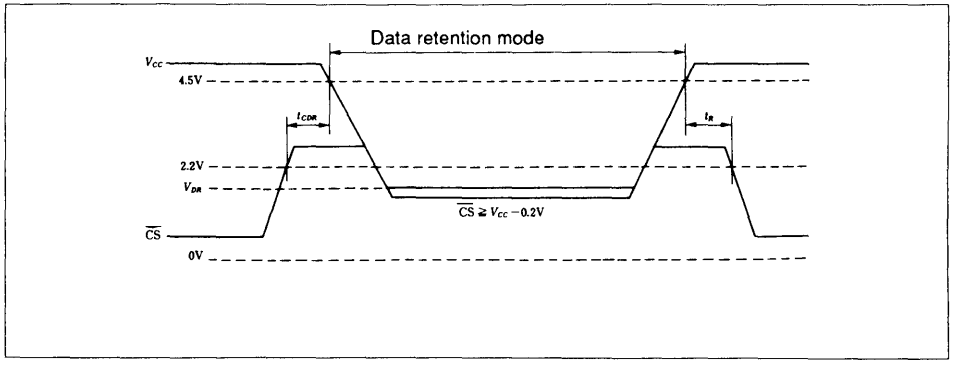
Low V_{CC} Data Retention Characteristics (T_a = 0 to +70°C)

These characteristics are guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS} \geq Vcc - 0.2$ V, Vin ≥ Vcc − 0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	1	50*2	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

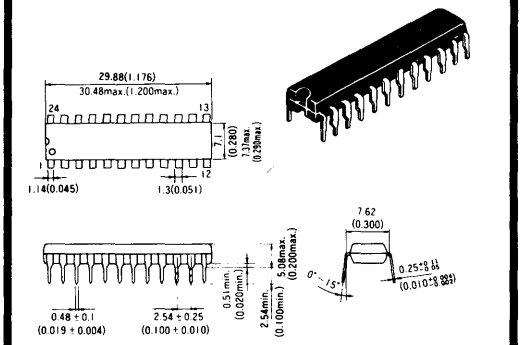
Notes: *1. t_{RC} = read cycle time.
*2. Vcc = 3.0 V.

Low Vcc Data Retention Timing Waveform

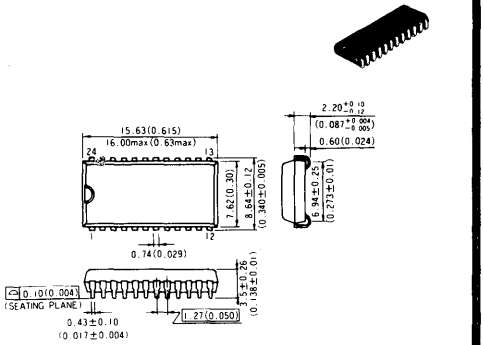


■ PACKAGE DIMENSIONS Unit: mm (inch)

HM6207P/HM6207HP Series
(DP-24NC)



HM6207HJP Series
(CP-24D)



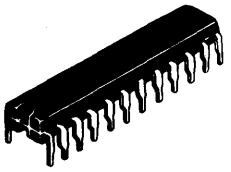
HM6707 Series

262144-word x 1-bit High Speed Hi-BiCMOS Static RAM

Features

- Super Fast Access Time : 20/25ns (max.)
- Low Power Dissipation
  Operating: 350mW (typ.) (f = 50MHz)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output

HM6707P



(DP-24NC)

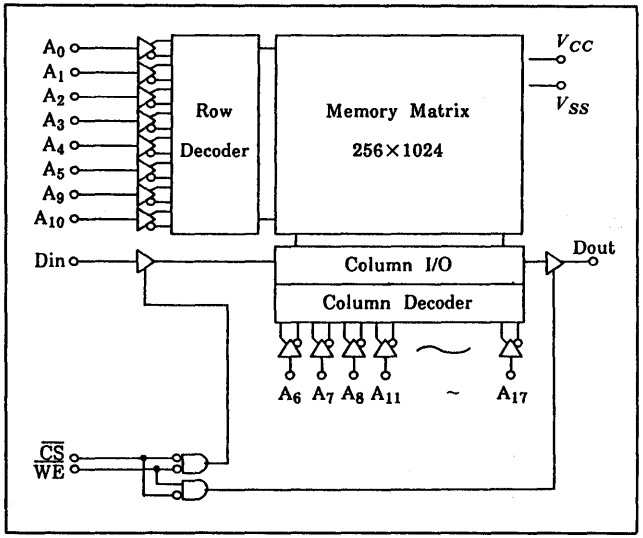
HM6707JP

(CP-24D)

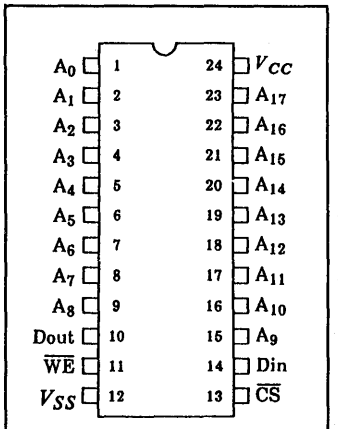
Ordering Information

Type No.	Access Time	Package
HM6707P-20	20ns	300mil 24 pin Plastic DIP
HM6707P-25	25ns	
HM6707JP-20	20ns	300 mil 24 pin SOJ
HM6707JP-25	25ns	

Block Diagram



Pin Arrangement



(Top View)

Note) The specifications of this device are subject to change without notice.
Please contact Hitachi's Sales Dept. regarding specifications.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	−0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	−10 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-0.5*1	–	0.8	V

Note) *1 : -3.0 V for pulse width 20ns.

Function Table

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}, I_{CC1}	D_{out}
L	L	Write	I_{CC}, I_{CC1}	High Z

DC and Operating Characteristics (V_{CC} = 5 V ±10%, T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	–	–	2	μA	V_{CC}=5.5 V, V_{IN}=V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	–	–	10	μA	$\overline{CS}$ = V_{IH}, V_{OUT}=V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	–	–	100	mA	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA
Average Operating Current	I_{CC1}	–	–	120	mA	Min. Cycle, Duty : 100%, I_{OUT} = 0mA
Standby Power Supply Current	I_{SB}	–	–	30	mA	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}
	I_{SB1}	–	–	10	mA	$\overline{CS} \geqq V_{CC}-0.2$ V $V_{IN} \leqq 0.2$ V or $V_{IN} \geqq V_{CC}-0.2$V
Output Low Voltage	V_{OL}	–	–	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	–	–	V	I_{OH} = -4 mA

Capacitance (T_a = 25°C, f = 1 MHz)

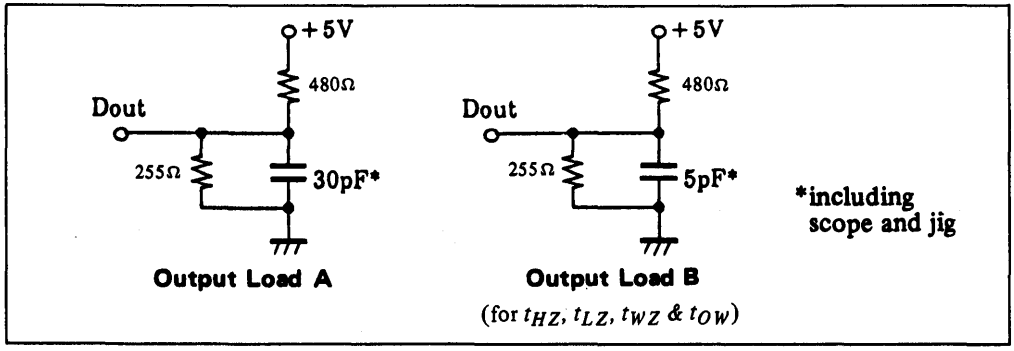
Item	Symbol	max.	Unit	Test Conditions
Input Capacitance	C_{IN}	6.0	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	10.0	pF	V_{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5V±10%, T_a = 0 to +70°C, unless otherwise noted)

AC Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input timing reference levels : 1.5 V
- Output Load : See Figure
- Input rise and fall times : 4 ns
- Output reference levels : 1.5 V

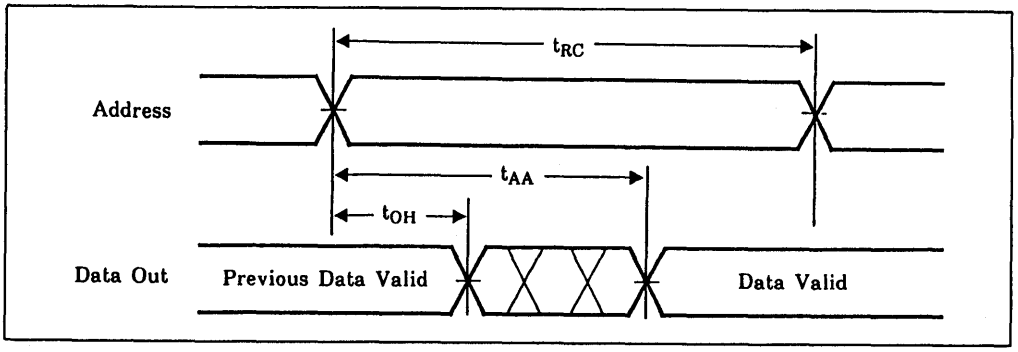


Read Cycle

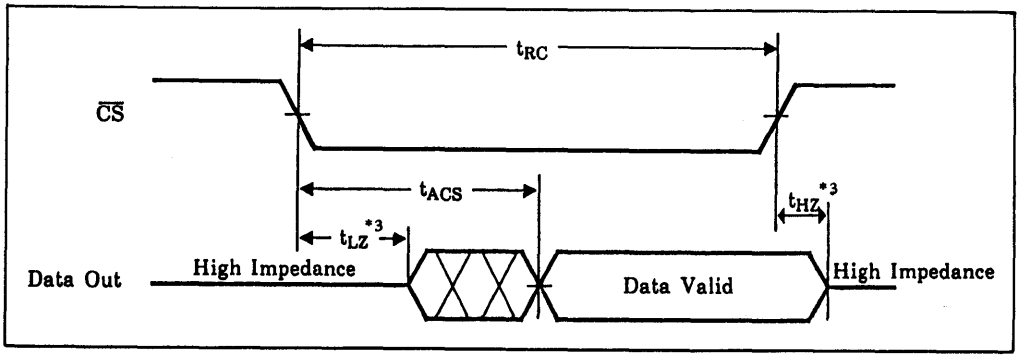
Item	Symbol	HM6707-20		HM6707-25		Unit	Notes
		min.	max.	min.	max.		
Read Cycle Time	t_{RC}	20	–	25	–	ns	–
Address Access Time	t_{AA}	–	20	–	25	ns	–
Chip Select Access Time	t_{ACS}	–	20	–	25	ns	–
Output Hold from Address Change	t_{OH}	5	–	5	–	ns	–
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	15	0	15	ns	1, 2

Note) 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.

Read Cycle-1*1



Read Cycle-2*2



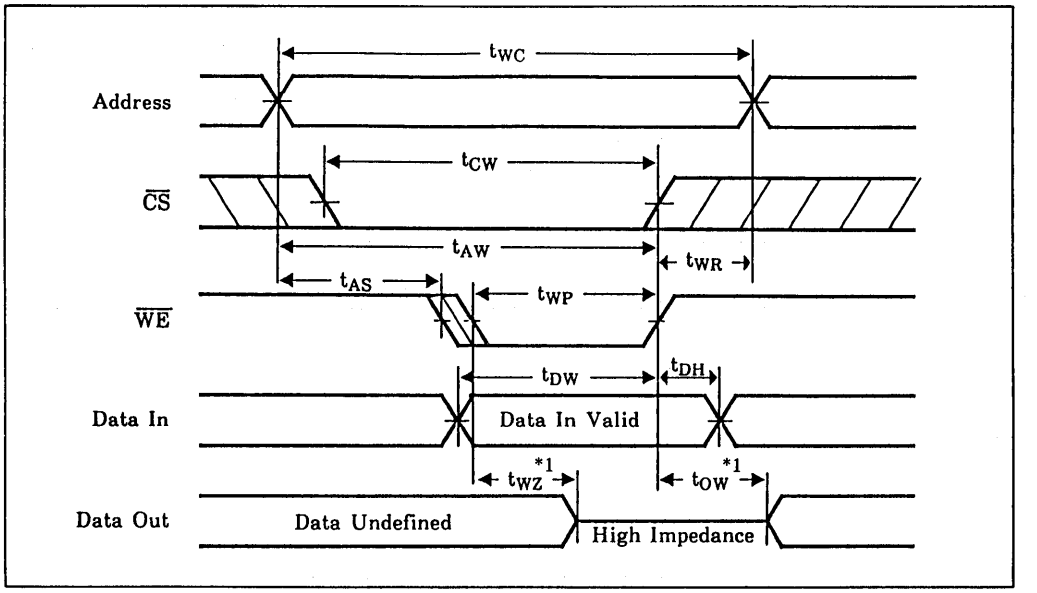
Notes) *1. $\overline{WE}$ is high and $\overline{CS}$ is low for Read cycle.
*2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
*3. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.

Write Cycle

Item	Symbol	HM6707-20		HM6707-25		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	20	–	25	–	ns	2
Chip Selection to End of Write	t_{CW}	15	–	20	–	ns	–
Address Valid to End of Write	t_{AW}	15	–	20	–	ns	–
Address Setup Time	t_{AS}	0	–	0	–	ns	–
Write Pulse Width	t_{WP}	15	–	20	–	ns	–
Write Recovery Time	t_{WR}	3	–	3	–	ns	–
Data Valid to End of Write	t_{DW}	15	–	20	–	ns	–
Data Hold Time	t_{DH}	0	–	0	–	ns	–
Write Enable to Output in High Z	t_{WZ}	0	15	0	15	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

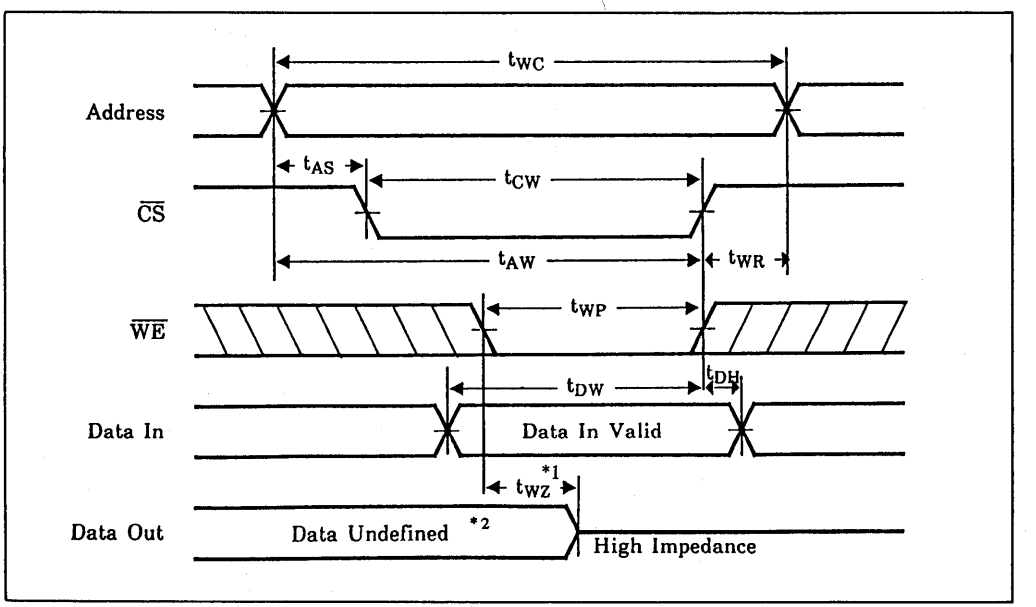
Note) 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.
4. This parameter is sampled and not 100% tested.

Write Cycle-1 ($\overline{WE}$ Controlled)



Note) *1. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.

Write Cycle-2 ($\overline{CS}$ Controlled)



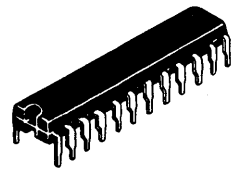
Note) *1. Transition is measured ±200 mV from steady state voltage with specified loading in Load B.
*2. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffer remains in a high impedance state.

HM6707A Series — Product Preview

262144-Word × 1-Bit High Speed Static RAM

■ FEATURES

- Super Fast
  Access Time .....15/20/25ns (max.)
- Low Power Dissipation .....400mW (typ.)
- +5V Single Supply
- Completely Static Memory
  No Clock or Timing Strobe Required
- Fully TTL Compatible Input and Output



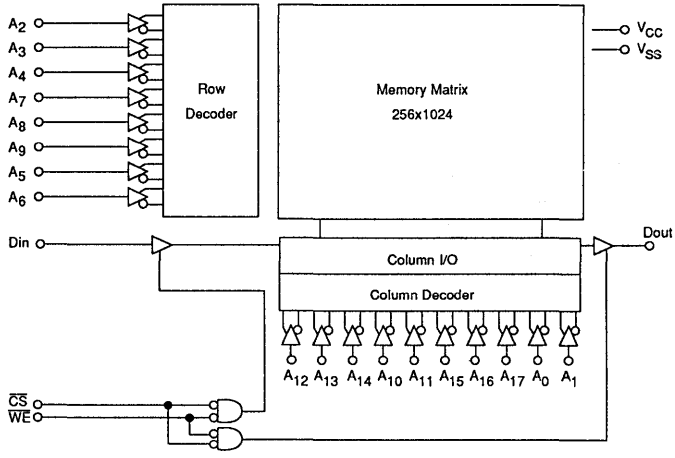
(DP-24NC)

(CP-24D)

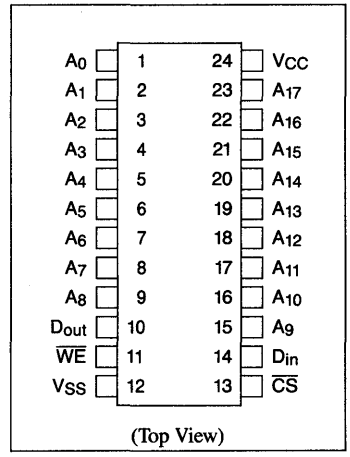
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM6707AP-15	15ns	300 mil 24 pin
HM6707AP-20	20ns	Plastic DIP
HM6707AP-25	25ns	(DP-24NC)
HM6707AJP-15	15ns	300 mil 24 pin
HM6707AJP-20	20ns	Plastic SOJ
HM6707AJP-25	25ns	(CP-24D)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to V_{SS} Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (with bias)	$T_{stg(bias)}$	-10 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \leq T_a \leq 70°C$)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-3.0*	—	0.8	V

*Pulse width: 15ns, DC: -0.5V

■ TRUTH TABLE

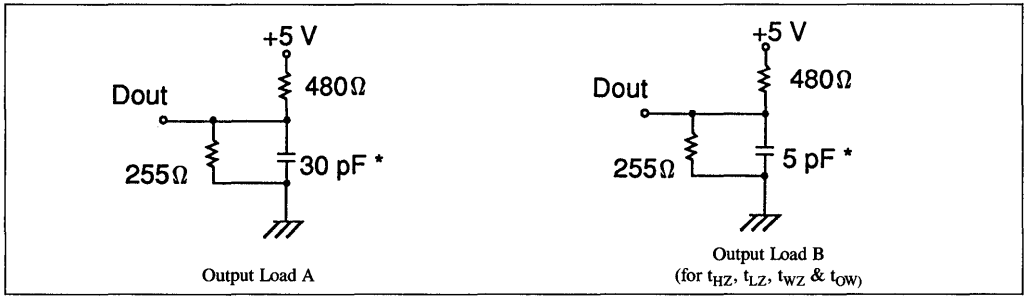
$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}, I_{CC1}	Data Out
L	L	Write	I_{CC}, I_{CC1}	High Z

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, V_{SS} = 0V)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, I_{OUT} = 0mA	—	—	100	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, I_{OUT} = 0mA	—	—	120	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} = V_{IH} or V_{IL}	—	—	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} - 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} - 0.2V	—	—	10	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	—	—	V

■ AC TEST CONDITIONS

- Input Pulse Levels: V_{SS} to 3.0V
- Input Timing Reference Levels: 1.5V
- Output Reference Levels: 1.5V
- Input Rise and Fall Times: 4ns
- Output Load: See Figure



Output Load A

Output Load B
(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})

*Including scope and jig capacitance.

■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	6.0	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	10.0	pF

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0°C to 70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	HM6707A-15		HM6707A-20		HM6707A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	15	—	20	—	25	—	ns	—
Address Access Time	t_{AA}	—	15	—	20	—	25	ns	—
Chip Select Access Time	t_{ACS}	—	15	—	20	—	25	ns	—
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	ns	—
Chip Selection to Output in Low Z	t_{LZ}	3	—	3	—	3	—	ns	1, 2
Chip Deselection to Output in High Z	t_{HZ}	0	6	0	8	0	10	ns	1, 2

NOTES: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

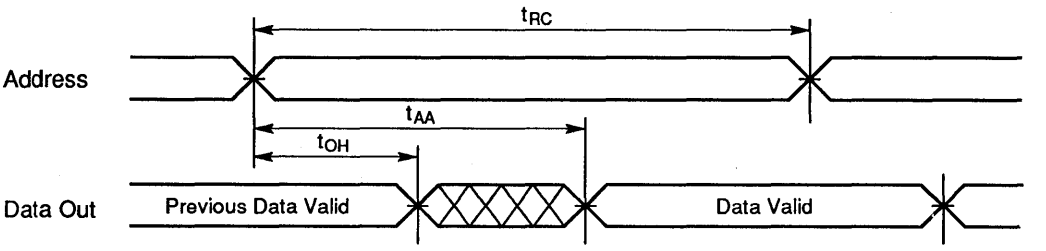
• Write Cycle

Item	Symbol	HM6707A-15		HM6707A-20		HM6707A-25		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	15	—	20	—	25	—	ns	1
Chip Selection to End of Write	t_{CW}	10	—	15	—	20	—	ns	—
Address Valid to End of Write	t_{AW}	10	—	15	—	20	—	ns	—
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	—
Write Pulse Width	t_{WP}	10	—	15	—	20	—	ns	—
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	—
Data Valid to End of Write	t_{DW}	9	—	12	—	15	—	ns	—
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	—
Write Enable to Output in High Z	t_{WZ}	0	6	0	8	0	10	ns	2, 3
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	2, 3

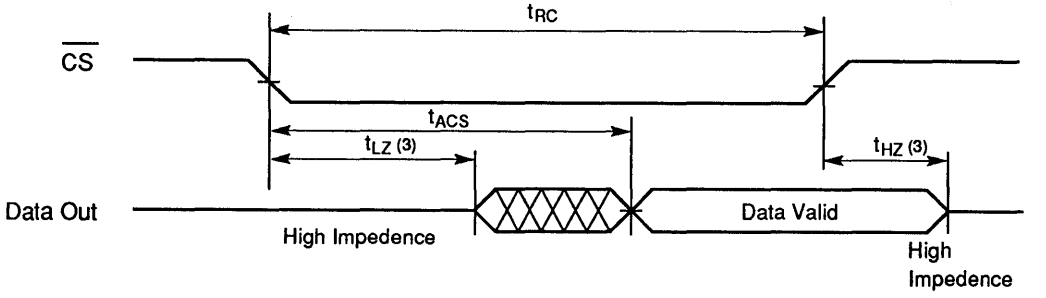
NOTES: 1. All write cycle timings are referenced from the last valid address to the first transitioning address.
2. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
3. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

• Read Cycle (1) (1)

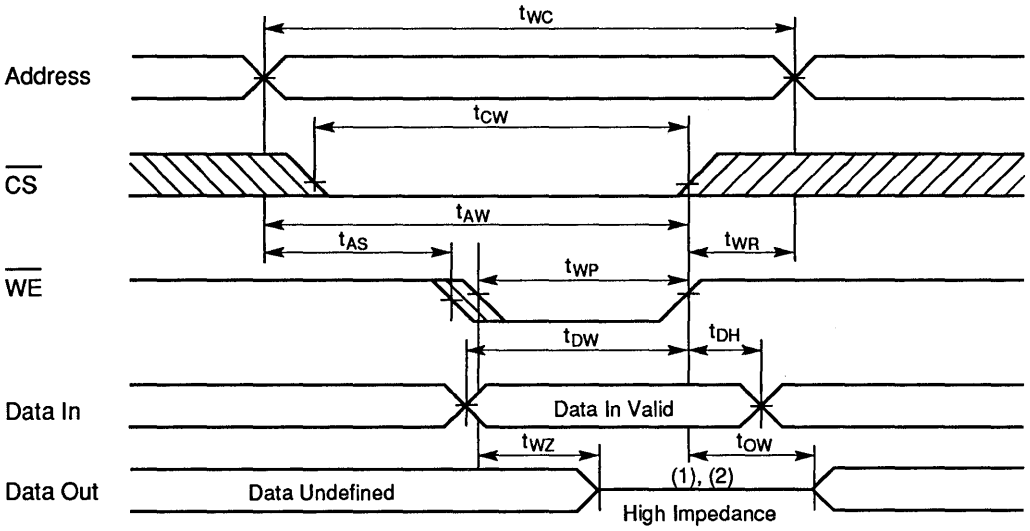


• Read Cycle (2) (2)



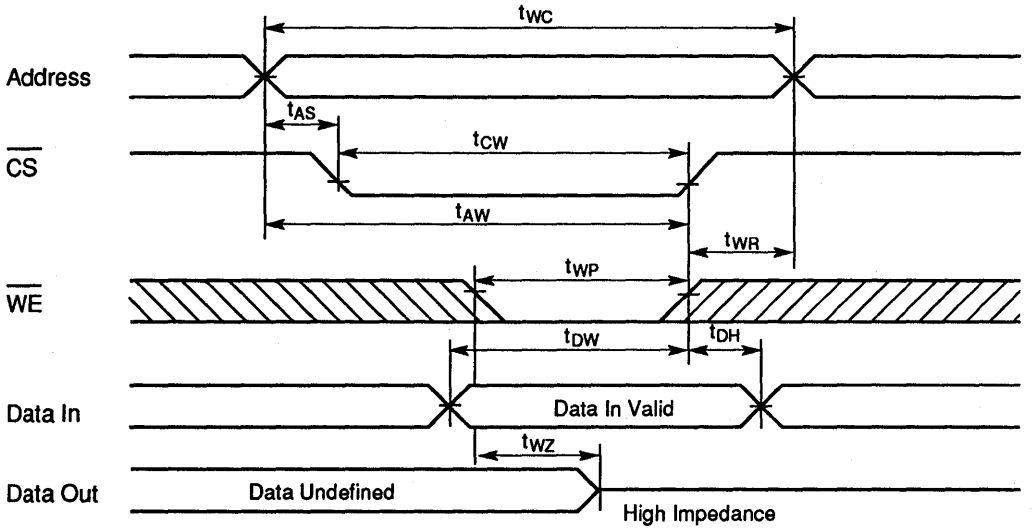
NOTES:
1. $\overline{WE}$ is high and $\overline{CS}$ is low for READ cycle.
2. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

• **Write Cycle (1)** ($\overline{WE}$ Controlled)



NOTES: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

• **Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTES: 1. Transition is measured ±200mV from steady state voltage with specified loading in Load B.

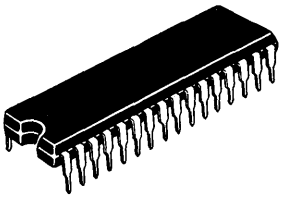
HM628128 Series

131072-Word × 8-Bit High Speed CMOS Static RAM

The Hitachi HM628128 is a CMOS static RAM organized 128-kword x 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.8 μm Hi-CMOS process technology.

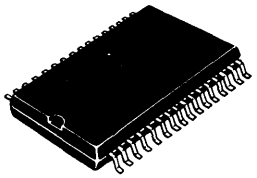
It offers low power standby power dissipation; therefore, it is suitable for battery back-up systems. The device, packaged in a 525 mil SOP (460-mil body SOP) or a 600-mil plastic DIP, is available for high density mounting.

HM628128P Series



(DP-32)

HM628128FP Series



(FP-32D)

Features

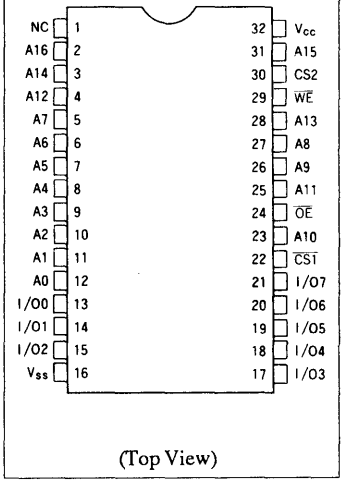
- High speed: Fast access time 70/85/100/120 ns (max.)
- Low power
  - Standby: 10 μW (typ) (L-version)
  - Operation: 75 mW (typ)
- Single 5 V supply
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Capability of battery back up operation (L-version)
  - 2 chip selection for battery back up

Ordering Information

Type No.	Access Time	Package
HM628128P-7	70 ns	600 mil 32-pin plastic DIP (DP-32)
HM628128P-8	85 ns	
HM628128P-10	100 ns	
HM628128P-12	120 ns	
HM628128LP-7	70 ns	
HM628128LP-8	85 ns	
HM628128LP-10	100 ns	
HM628128LP-12	120 ns	
HM628128FP-7	70 ns	525 mil 32-pin plastic SOP (FP-32D)
HM628128FP-8	85 ns	
HM628128FP-10	100 ns	
HM628128FP-12	120 ns	
HM628128LFP-7	70 ns	
HM628128LFP-8	85 ns	
HM628128LFP-10	100 ns	
HM628128LFP-12	120 ns	

Note: The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

Pin Arrangement

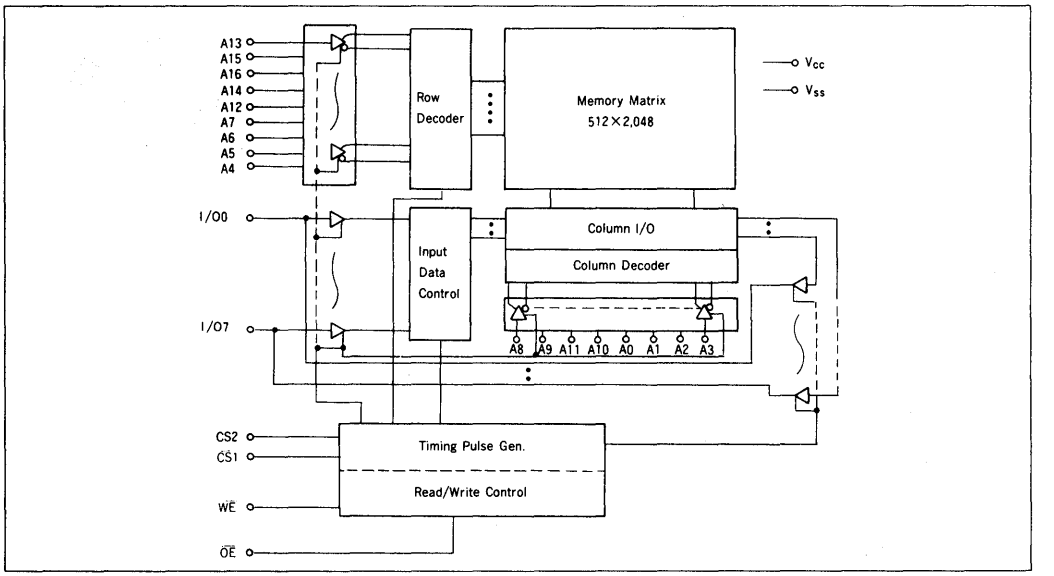


(Top View)

Pin Description

Pin Name	Function
A0 – A16	Address
I/O0 – I/O7	Input/output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
NC	No connection
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	Mode	Vcc Current	Dout Pin	Ref. Cycle
×	H	×	×	Not selected	I_{SB}, I_{SB1}	High-Z	
×	×	L	×		I_{SB}, I_{SB1}	High-Z	
H	L	H	H	Output disable	Icc	High-Z	
H	L	H	L	Read	Icc	Dout	Read cycle
L	L	H	H	Write	Icc	Din	Write cycle (1)
L	L	H	L		Icc	Din	Write cycle (2)

Note: × : H or L

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_T	–0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Storage temperature under bias	Tbias	–10 to +85	°C

Note: *1. –3.0 V for pulse half-width ≤ 30 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V	
Input low (logic 0) voltage	V_{IL}	–0.3*1	—	0.8	V	

Note: *1. –3.0 V for pulse half-width ≤ 30 ns

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min	Typ*1	Max	Unit	Test Conditions
Input leakage current	$\|I_{LI}\|$	—	—	2	µA	Vin = Vss to Vcc
Output leakage current	$\|I_{LO}\|$	—	—	2	µA	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$= Vss to Vcc
Operating power supply current: DC	I_{CC}	—	15	30	mA	$\overline{CS1}$= V_{IL}, CS2 = V_{IH}, others = V_{IH}/V_{IL} $I_{I/O}$= 0 mA
Operating power supply current	I_{CC1}	—	45	70	mA	Min cycle, duty = 100%, $\overline{CS1}$ = V_{IL}, CS2 = V_{IH}, others = V_{IH}/V_{IL} $I_{I/O}$ = 0 mA
	I_{CC2}	—	15	30	mA	Cycle time = 1 µs, duty = 100%, $I_{I/O}$ = 0 mA $\overline{CS1}$ ≤ 0.2 V, CS2 ≥Vcc – 0.2 V V_{IH} ≥ Vcc – 0.2V, V_{IL} ≤ 0.2V
Standby power supply current: DC	I_{SB}	—	1	3	mA	$\overline{CS1}$ = V_{IH}, CS2 = V_{IH} or CS2 = V_{IL}
Standby power supply current (1): DC	I_{SB1}	—	0.02	2	mA	Vin ≥ 0 V $\overline{CS1}$ ≥ Vcc – 0.2 V, CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V
		—	2*2	100*2	µA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –1.0 mA

Notes: *1. Typical values are at Vcc = 5.0 V, Ta = +25°C and specified loading.
*2. This characteristics is guaranteed only for L-version.

Capacitance (Ta = 25°C, f = 1.0 MHz)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	—	—	8	pF	Vin = 0 V
Input/output capacitance	C$_{I/O}$	—	—	10	pF	V$_{I/O}$ = 0 V

Note: This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, unless otherwise noted)

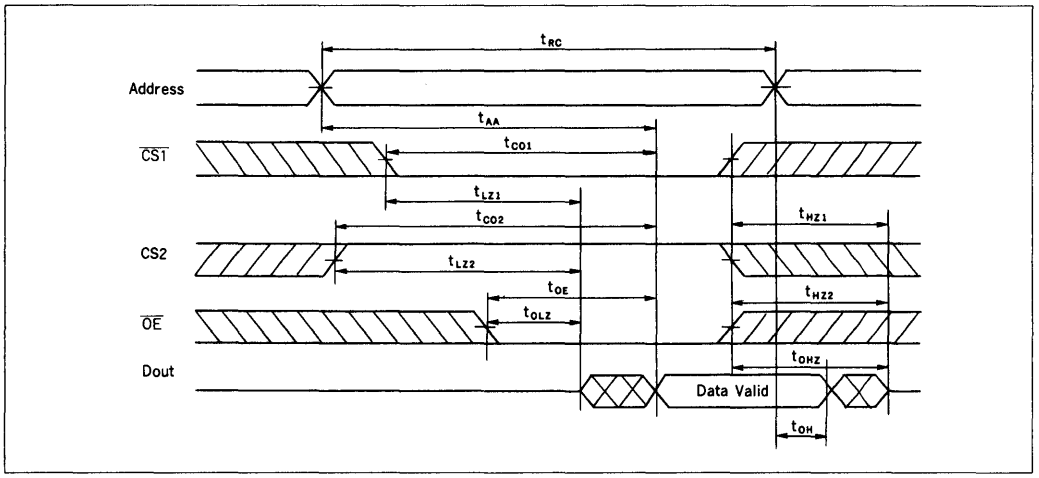
Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall times : 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate and CL (100pF) (Including scope & jig)

Read Cycle

Item	Symbol	HM628128-7		HM628128-8		HM628128-10		HM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	70	—	85	—	100	—	120	—	ns	
Address access time	t_{AA}	—	70	—	85	—	100	—	120	ns	
Chip selection ($\overline{CS1}$) to output valid	t_{CO1}	—	70	—	85	—	100	—	120	ns	
Chip selection (CS2) to output valid	t_{CO2}	—	70	—	85	—	100	—	120	ns	
Output enable ($\overline{OE}$) to output valid	t_{OE}	—	35	—	45	—	50	—	60	ns	
Chip selection ($\overline{CS1}$) to output in low-Z	t_{LZ1}	10	—	10	—	10	—	10	—	ns	*1, *2, *3
Chip selection (CS2) to output in low-Z	t_{LZ2}	10	—	10	—	10	—	10	—	ns	*1, *2, *3
Output enable ($\overline{OE}$) to output in low-Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns	*1, *2, *3
Chip deselection ($\overline{CS1}$) to output in high-Z	t_{HZ1}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Chip deselection (CS2) to output in high-Z	t_{HZ2}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Output disable ($\overline{OE}$) to output in high-Z	t_{OHZ}	0	25	0	30	0	35	0	45	ns	*1, *2, *3
Output hold from address change	t_{OH}	10	—	10	—	10	—	10	—	ns	

Read Timing Waveform*4

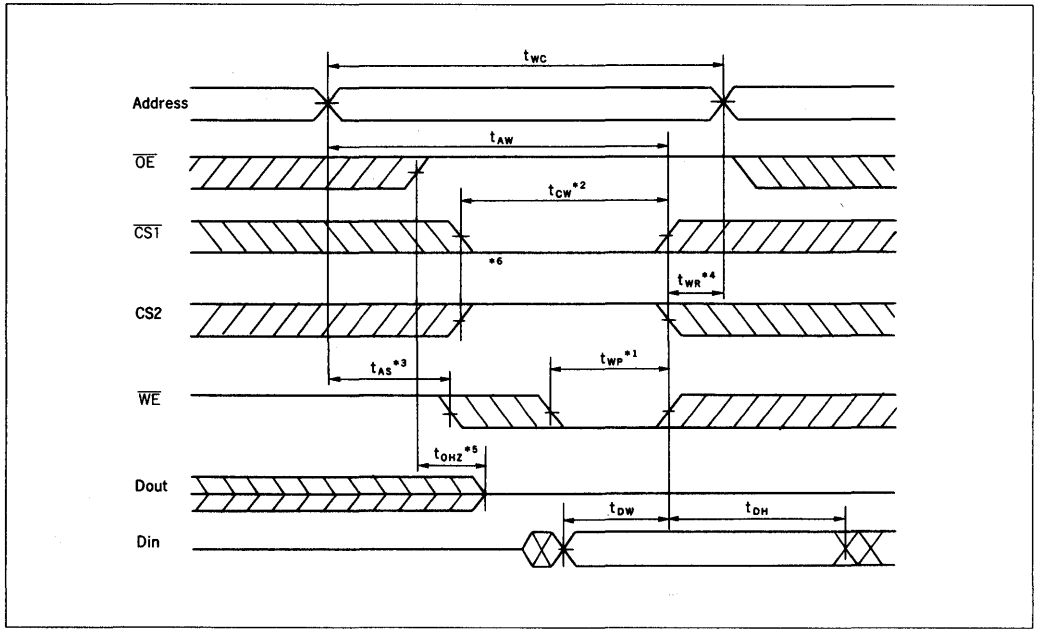


Notes: *1. tHZ and tOHZ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
*2. At any given temperature and voltage condition, tHZ max is less than tLZ min both for a given device and from device to device.
*3. This parameter is sampled and not 100% tested.
*4. $\overline{WE}$ is high for read cycle.

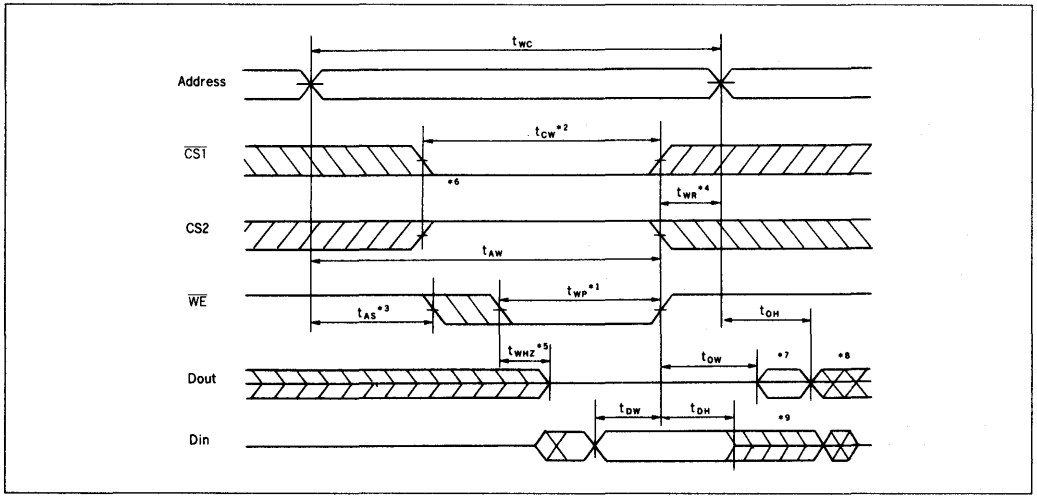
Write Cycle

Item	Symbol	HM628128-7		HM628128-8		HM628128-10		HM628128-12		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	tWC	70	—	85	—	100	—	120	—	ns	
Chip selection to end of write	tCW	60	—	75	—	90	—	100	—	ns	
Address setup time	tAS	0	—	0	—	0	—	0	—	ns	
Address valid to end of write	tAW	60	—	75	—	90	—	100	—	ns	
Write pulse width	tWP	55	—	65	—	75	—	85	—	ns	
Write recovery time	tWR	5	—	5	—	5	—	10	—	ns	
		10	—	10	—	10	—	15	—	ns	*11
Write to output in high-Z	tWHZ	0	25	0	30	0	35	0	40	ns	*10
Data to write time overlap	tDW	30	—	35	—	40	—	45	—	ns	
Write hold from write time	tDH	0	—	0	—	0	—	0	—	ns	
Output active from end of write	tOW	5	—	5	—	5	—	5	—	ns	*10

Write Timing Waveform (1) ($\overline{OE}$ Clock)



Write Timing Waveform (2) ($\overline{OE}$ Low Fix)



Notes: *1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

*2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.

*3. t_{AS} is measured from the address valid to the beginning of write.

*4. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

*5. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.

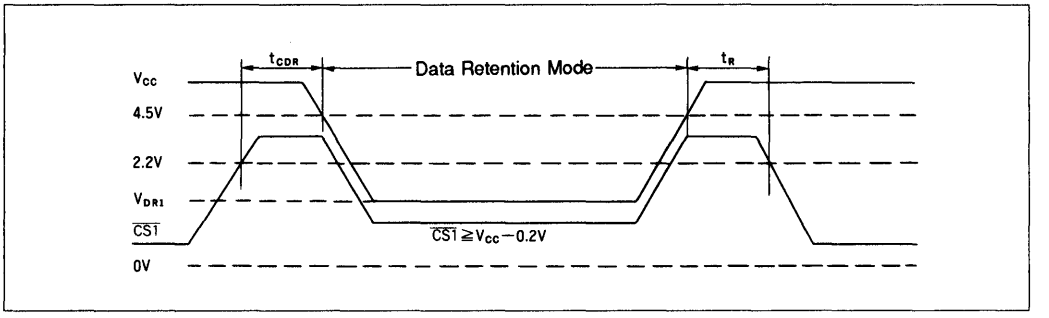
*6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
*7. Dout is the same phase of the latest written data in this write cycle.
*8. Dout is the read data of next address.
*9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
*10. This parameter is sampled and not 100% tested.
*11. This value is measured from CS2 going low to the end of write cycle.

Low Vcc Data Retention Characteristics (Ta = 0 to +70°C)

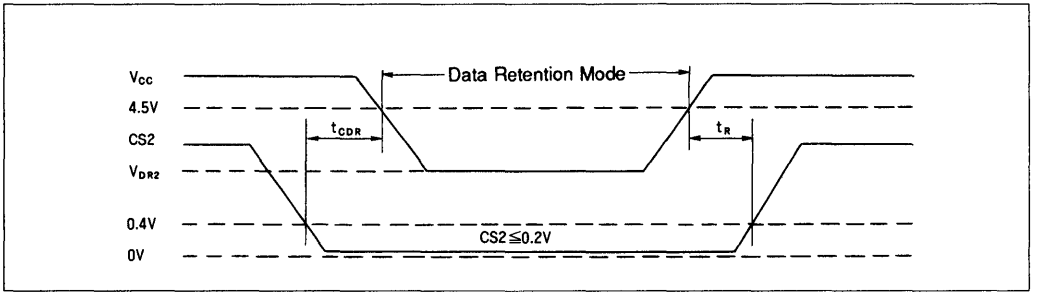
(This characteristics is guaranteed only for L-version.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions*2
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS1} \geq Vcc - 0.2$ V, CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V Vin ≥ 0 V
Data retention current	I_{CCDR}	—	1	50*1	µA	Vcc = 3.0 V, Vin ≥ 0 V $\overline{CS1} \geq Vcc - 0.2$ V, CS2 ≥ Vcc – 0.2 V or 0 V ≤ CS2 ≤ 0.2 V
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See Retention Waveform
Operation recovery time	t_R	5	—	—	ms	

Low Vcc Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



Low Vcc Data Retention Timing Waveform (2) (CS2 Controlled)



Notes: *1. 20 μA max at Ta=0 to 40°C.

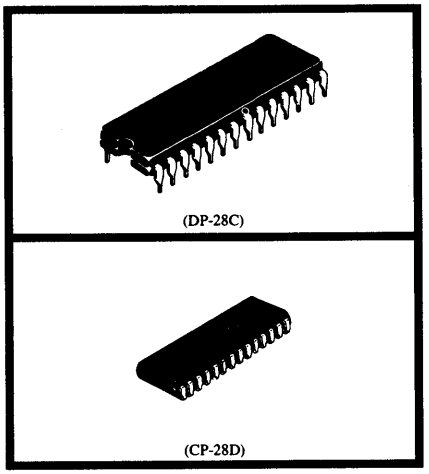
*2. CS2 controls address buffer, $\overline{WE}$ buffer, $\overline{CS1}$ buffer and $\overline{OE}$ buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CS1}$ controls data retention mode, CS2 must be CS2 ≥ Vcc − 0.2 V or 0 V ≤ CS2 ≤ 0.2 V. The other input levels (address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

HM624256 Series
4-Bit CMOS Static RAM

HM624256 SERIES
262144-WORD × 4-BIT HIGH SPEED CMOS STATIC RAM

The Hitachi HM624256 is a high speed 1M static RAM organized as 256-kword × 4-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624256, packaged in a 400-mil plastic SOJ is available for high density mounting.



■ FEATURES

- Single 5 V supply and high density 28-pin package (DIP and SOJ)
- High speed: Fast access time 35/45 ns (max.)
- Low power
  Operation: 350 mW (typ.)
  Standby: 100 μW (typ.)
- Completely static memory:
  No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs

■ ORDERING INFORMATION

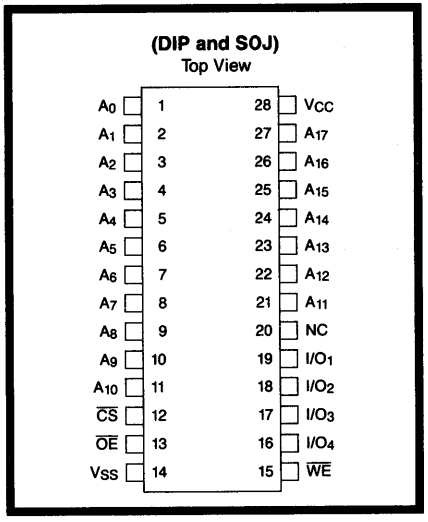
Type No.	Access Time	Package
HM624256P-35	35 ns	400 mil
HM624256P-45	45 ns	28-pin
HM624256LP-35	35 ns	Plastic DIP
HM624256LP-45	45 ns	(DP28C)
HM624256JP-35	35 ns	400 mil
HM624256JP-45	45 ns	28-pin
HM624256LJP-35	35 ns	Plastic SOJ
HM624256LJP-45	45 ns	(CP-28D)

■ PIN DESCRIPTION

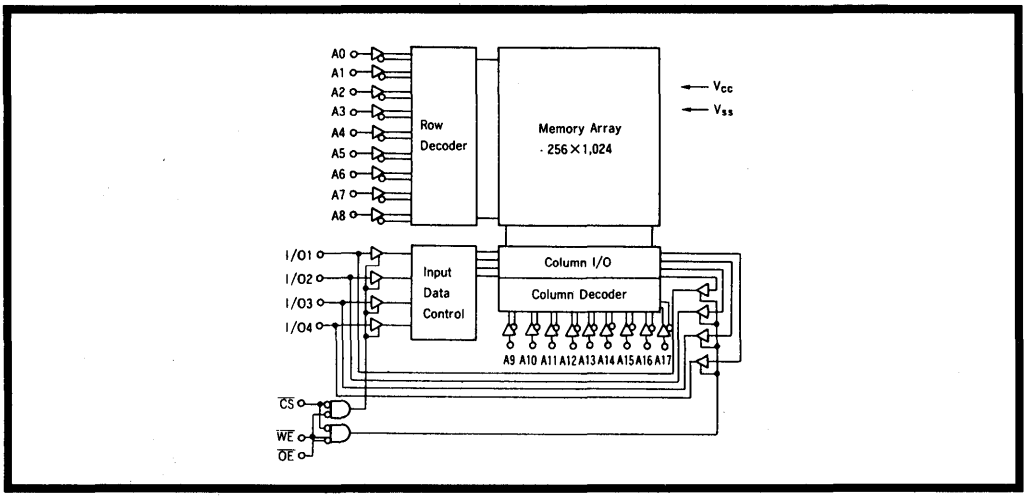
Pin Name	Function
A_0-A_{17}	Address
I/O_1-I/O_4	Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

Note: The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

PIN ARRANGEMENT



■ BLOCK DIAGRAM



■ FUNCTION TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	D_{out}	Read Cycle(1)-(3)
L	H	L	Write	I_{CC}	D_{in}	Write Cycle(1)
L	L	L	Write	I_{CC}	D_{in}	Write Cycle(2)

NOTE: X : H or L

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_T	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

NOTE: *1. V_T min. = −2.0 V for pulse width ≤ 10 ns.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	-0.5*1	—	0.8	V

NOTE: *1. V_{IL} min. = -2.0 V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	μA	V_{CC} = max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	2.0	μA	$\overline{CS}$ = V_{IH} V_{out} = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	—	70	120	mA	$\overline{CS}$ = V_{IL}, I_{out} = 0 mA, min. cycle
Standby Power Supply Current	I_{SB}	—	30	60	mA	$\overline{CS}$ = V_{IH}, min. cycle
Standby Power Supply Current (1)	I_{SB1}*2 I_{SB1}*3	— —	0.02 —	2.0 0.2	mA mA	$\overline{CS}$ ≥ V_{CC} - 0.2 V 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} - 0.2V
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = -4.0 mA

NOTES: *1. Typical limits are at V_{CC} = 5.0 V, T_a = 25°C amd specified loading.
*2. JP-version
*3. LJP-version

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

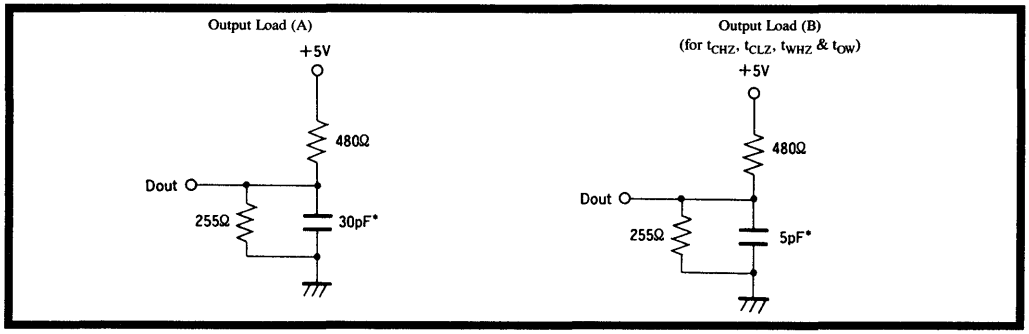
Item	Symbol	Min.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	6	pF	V_{in} = 0 V
Input/Output Capacitance	$C_{I/O}$	—	11	pF	$V_{I/O}$ = 0 V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See Figures

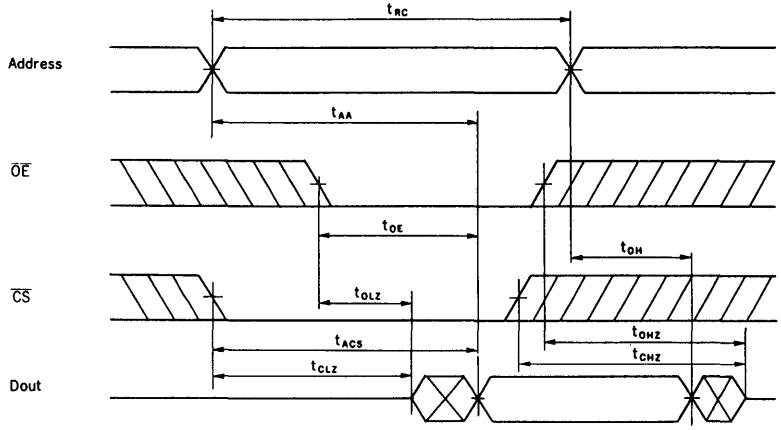


NOTE: *Including scope & jig.

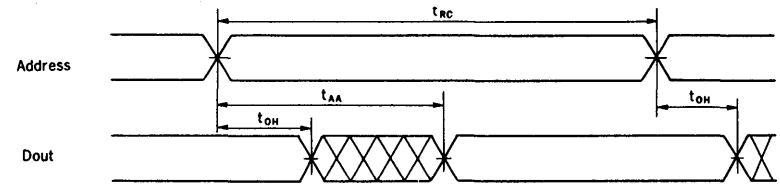
■ Read Cycle

Item	Symbol	HM624256-35		HM624256-45		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	35	—	45	—	ns
Address Access Time	t_{AA}	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	35	—	45	ns
Chip Selection to Output in Low-Z	t_{CLZ}*1	10	—	10	—	ns
Output Enable to Output Valid	t_{OE}	—	18	—	23	ns
Output Enable to Output in Low-Z	t_{OLZ}*1	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}*1	0	20	0	20	ns
Chip Disable to Output in High-Z	t_{OHZ}*1	0	10	0	15	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns

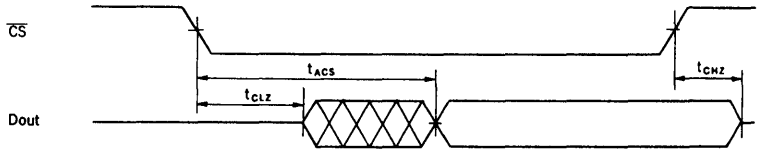
Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *2, *3, *5



Read Timing Waveform (3) *1, *2, *4, *5



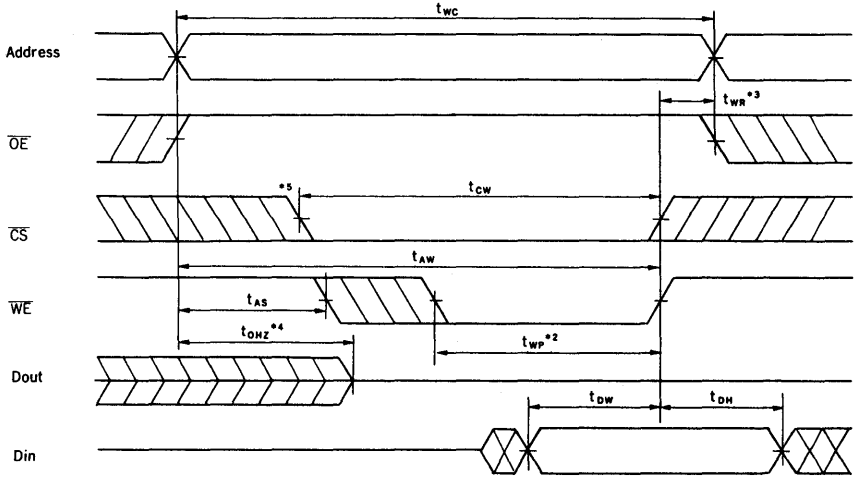
NOTES: *1. Transition is measured ±200 mv from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
*2. $\overline{WE}$ is high for read cycle.
*3. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*4. Address valid prior to or coincident with $\overline{CS}$ transition low.
*5. $\overline{OE}$ = V_{IL}.

■ Write Cycle

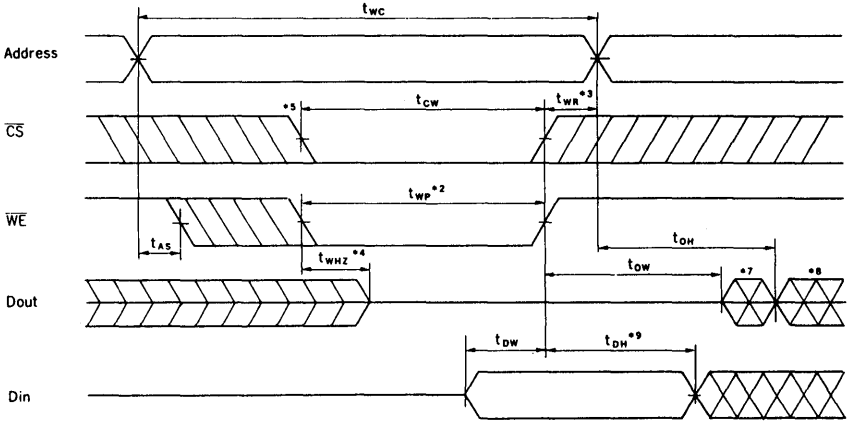
Item	Symbol	HM624256-35		HM624256-45		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	30	—	35	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Output Disable to Output in High-Z*1	t_{OHZ}	0	10	0	15	ns
Write to Output in High-Z*1	t_{WHZ}	0	10	0	15	ns
Data to Write Time Overlap	t_{DW}	20	—	25	—	ns
Data Hold From Write Time	t_{DH}	0	—	0	—	ns
Output Active From End of Write*1	t_{OW}	0	—	0	—	ns

NOTE: 1. Transition is measured ± 200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Write Timing Waveform (1)



Write Timing Waveform (2) *6



NOTES: *1. Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

*2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

*3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*4. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.

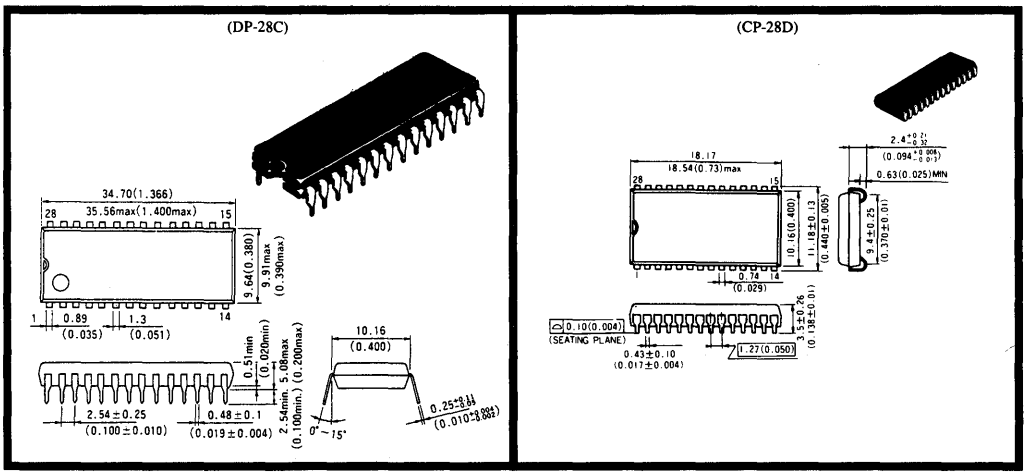
*5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.

*6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})

*7. D_{OUT} is the same phase of write data of this write cycle.

*8. D_{OUT} is the read data of next address.

*9. If $\overline{CS}$ is low during this period, I/O pins are the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.



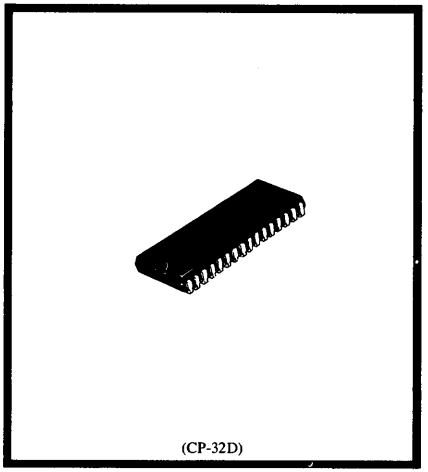
HM624257 Series
4-Bit CMOS Static RAM

Under Development

HM624257 SERIES
262144-WORD × 4-BIT HIGH SPEED CMOS STATIC RAM

The Hitachi HM624257 is a high speed 1M static RAM organized as 256-kword × 4-bit. It realizes high speed access time (35/45 ns) and low power consumption, employing the advanced CMOS process technology and high speed circuit designing technology. It is most advantageous for the field where high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM624257, packaged in a 400-mil plastic SOJ is available for high density mounting.



(CP-32D)

■ FEATURES

- Single 5 V supply and high density 32-pin package (SOJ)
- High speed: Access time 35/45 ns (max.)
- Low power dissipation
  Active mode: 350 mW (typ.)
  Standby: 100 μW (typ.)
- Completely static memory:
  No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible: All inputs and outputs

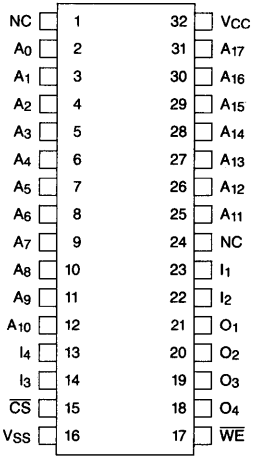
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM624257JP-35	35 ns	400 mil 32-pin Plastic SOJ (CP-32D)
HM624257JP-45	45 ns	
HM624257LJP-35	35 ns	
HM624257LJP-45	45 ns	

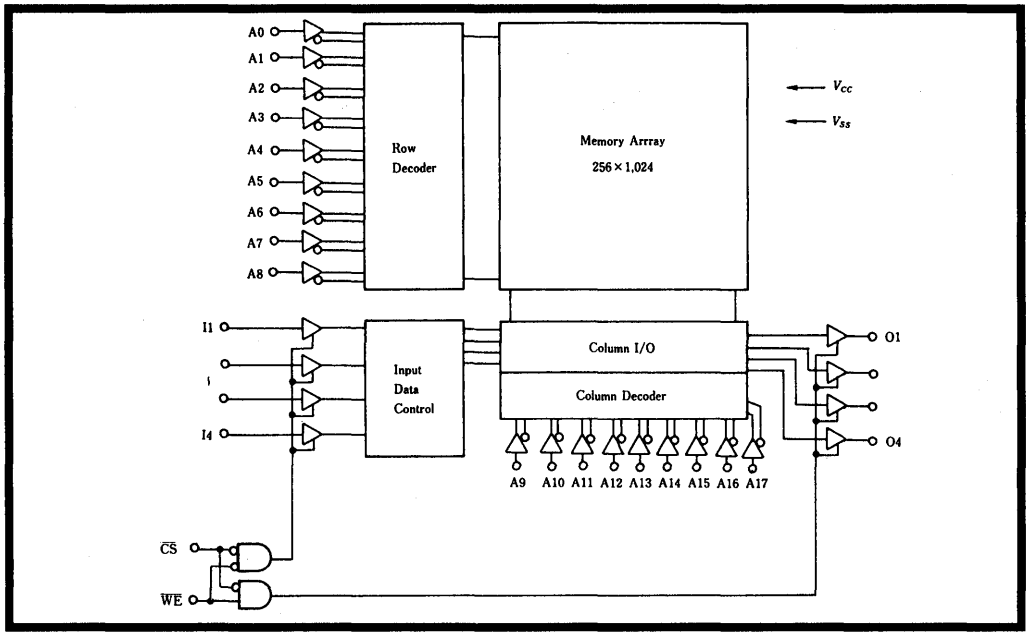
■ PIN DESCRIPTION

Pin Name	Function
A_0-A_{17}	Address
I_1-I_4	Data Input
I_1-O_4	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground

PIN ARRANGEMENT
Top View



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on any Pin Relative to V_{SS}	V_{in}	−0.5*1 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

NOTE: *1. V_{in} min. = −2.0 V for pulse width ≤ 10 ns.

■ FUNCTION TABLE

$\overline{CS}$	$\overline{WE}$	Mode	V_{CC} Current	D_{out} Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle(1)-(2)
L	L	Write	I_{CC}	High-Z	Write Cycle(1)-(2)

NOTE: X : H or L

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	-0.5*1	—	0.8	V

NOTE: *1. V_{IL} min. = -2.0 V for pulse width ≤ 10 ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current	$\|I_{LI}\|$	—	—	2.0	μA	V_{CC} = max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current	$\|I_{LO}\|$	—	—	10.0	μA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	—	70	120	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, min. cycle
Standby Power Supply Current	I_{SB}	—	30	60	mA	$\overline{CS}$ = V_{IH}, min. cycle
Standby Power Supply Current (1)	I_{SB1}	—	0.02	2.0	mA	$\overline{CS}$ ≥ V_{CC} - 0.2 V 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} - 0.2V
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = -4.0 mA

NOTE: 1. Typical limits are at V_{CC} = 5.0 V, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

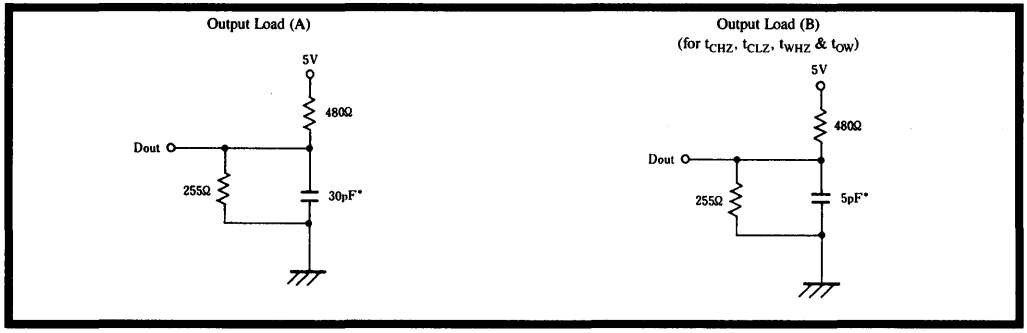
Item	Symbol	Min.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	6	pF	V_{in} = 0 V
Output Capacitance	C_{out}	—	11	pF	V_{out} = 0 V

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: See Figures



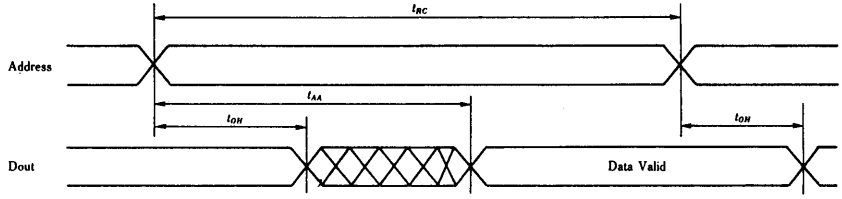
NOTE: *Including scope & jig.

■ Read Cycle

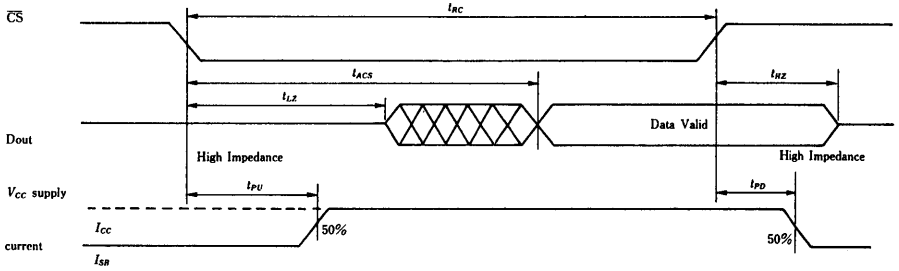
Item	Symbol	HM624257-35		HM624257-45		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	35	—	45	—	ns
Address Access Time	t_{AA}	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	35	—	45	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}*1	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}*1	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—		—	30	ns

NOTE: 1. Transition is measured ±200 mV from steady voltage with Load (B).
This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



NOTES: *1. $\overline{WE}$ is high for read cycle.

*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.

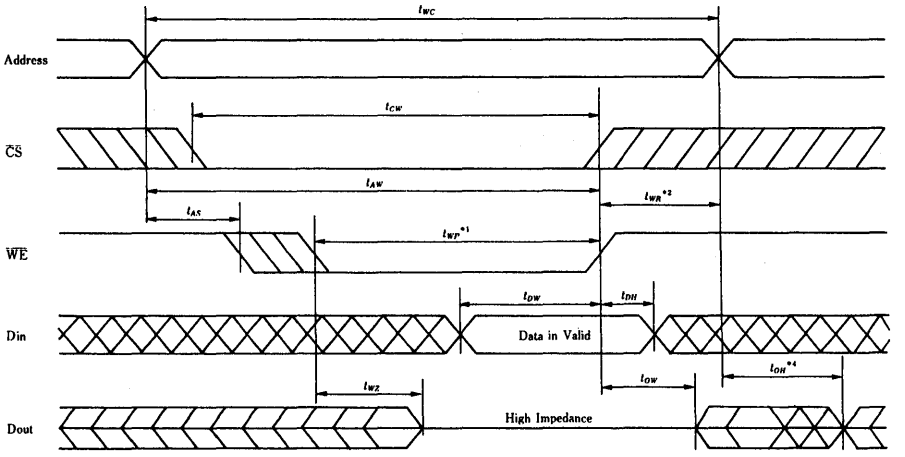
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

■ Write Cycle

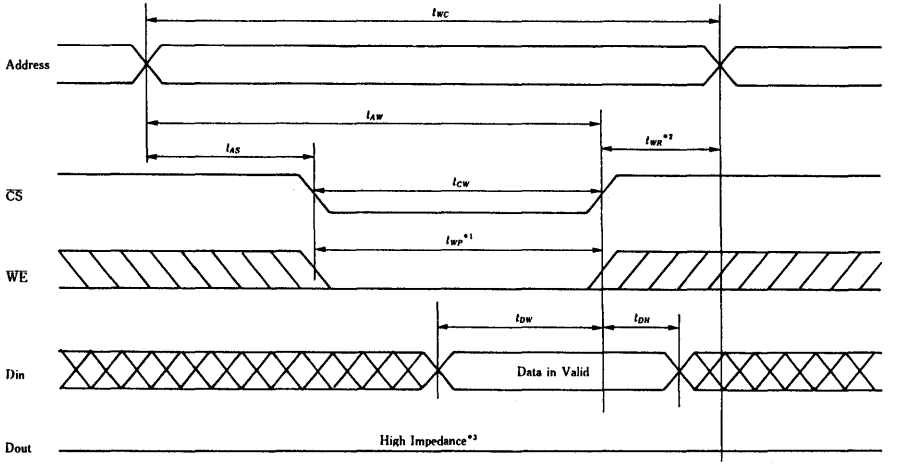
Item	Symbol	HM624257-35		HM624257-45		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	35	—	45	—	ns
Chip Selection to End of Write	t_{CW}	30	—	40	—	ns
Address Valid to End of Write	t_{AW}	30	—	40	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	30	—	35	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Data Valid to End of Write	t_{DW}	20	—		—	ns
Data Hold Time	t_{DH}	3	—	3	—	ns
Write Enabled to Output in High-Z	t_{WZ}*1	0	15	0	20	ns
Output Active From End of Write	t_{OW}*1	5	—	5	—	ns

NOTE: 1. Transition is measured ±200 mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



NOTES: *1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

*3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output buffers remain in a high impedance state.

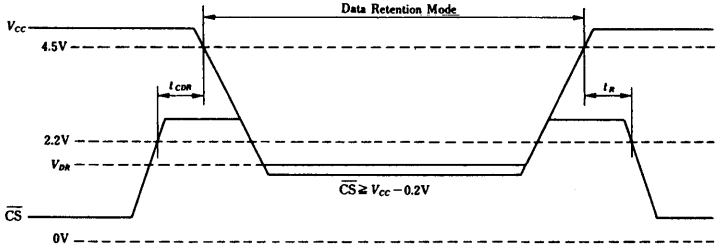
*4. D_{OUT} is the same phase of write data of this write cycle.

■ Low V_{CC} Data Retention Characteristics (T_a = 0 to +70°C)

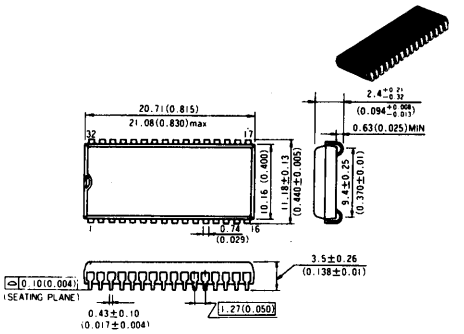
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
V_{CC} for Data Retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2$ V, $V_{in} \geq V_{CC} - 0.2$ V or 0 V ≤ V_{in} ≤ 0.2 V
Data Retention Current	I_{CCDR}	—	2	100*1	μA	
Chip Deselect to Data Retention Time	t_{CDR}	0	—	—	ns	
Operation Recovery Time	t_R	5	—	—	ms	

NOTE: *1. V_{CC} = 3.0 V.

Low V_{CC} Data Retention Timing Waveform



(CP-32D)


20.71(0.815)
21.08(0.830)max
32
17
1
16
10.16 (0.400)
11.18±0.13
(0.440±0.005)
0.74
(0.029)
2.4 +0.21 −0.32
(0.094 +0.008 −0.013)
0.63(0.025)MIN
9.4±0.25
(0.370±0.01)
3.5±0.26
(0.138±0.01)
0.10(0.004)
(SEATING PLANE)
0.43±0.10
(0.017±0.004)
1.27(0.050)

HM66204 Series — Maintenance Only

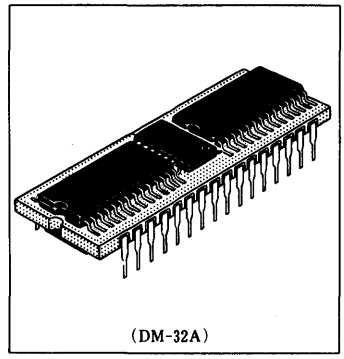
131072-word x 8-bit High Density CMOS Static RAM Module

The HM66204 is a high density 1 M-bit static RAM module consisted of 4 pieces of HM62256FP/LFP products (SOP type 256k static RAM) and a HD74HC138FP equivalent product (SOP type CMOS decoder logic).

An outline of the HM66204 is the standard 600 mil width 32 pin dual-in-line package. Its pin arrangement is completely compatible with 1 M-bit monolithic static RAM.

The HM66204 offers the features of low power and high speed by using high speed CMOS devices. And, the HM66204 makes high density mounting possible with no surface mount technology.

These features make the HM66204 ideally suited for high density compacted memory systems.

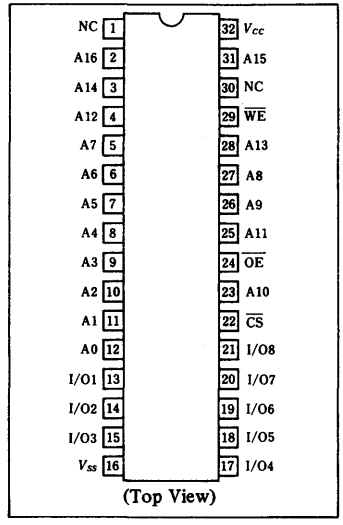


(DM-32A)

Features

- High density 32 pin DIP
  - Mounting 4 pcs. of 256k static RAM (SOP; HM62256FP/LFP) and CMOS decoder logic (SOP; HD74HC138FP equivalent)
- Pin compatible with 1M monolithic static RAM
- High speed
  - Fast access time 120 ns/150 ns (maximum)
- Equal access and cycle time
- Completely static RAM
  - No clock or timing strobe required
- Low power standby and low power operation
  - Standby 40 μW (typical) (L-version)
  - Operation 50 mW(typical) (f = 1 MHz)
- Common data input and output, three state outputs
- Capable of battery backup operation (L-version)

Pin Arrangement



(Top View)

Ordering Information

Part No.	Access Time	Package
HM66204-12	120 ns	600-mil 32-pin DIP
HM66204-15	150 ns	
HM66204L-12	120 ns	
HM66204L-15	150 ns	

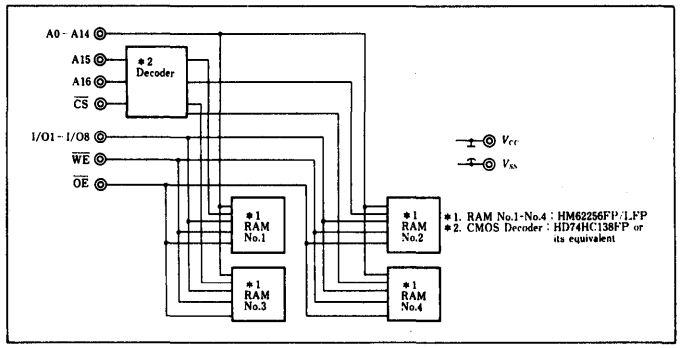
Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	−0.5 to +7.0	V
Operating temperature range	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C
Power dissipation	P_T	1.0	W

Pin Description

Pin Name	Function
A0 - A16	Address
I/O1 - I/O8	Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connection

Block Diagram



Mode Selection

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Current	Note
Not selected (Power down)	H	X	X	High-Z	I_{SB}, I_{SB1}	
Read	L	H	L	Dout	I_{CC}	Read cycle (1) – (3)
Write	L	L	H	Din	I_{CC}	Write cycle (1)
	L	L	L	Din	I_{CC}	Write cycle (2)

Note) X = Don't care (H or L)

Electrical Characteristics

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high (logic 1) Voltage	V_{IH}	3.85*1	–	6.0	V	A15, A16, $\overline{CS}$
		2.2	–	6.0	V	Others except A15, A16, $\overline{CS}$
Input low (logic 0) Voltage	V_{IL}	–0.5	–	0.8	V	

Note) *1. V_{IH} min is determined by V_{CC} x 0.7.

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Min	Typ*1	Max	Unit	Test Conditions	Notes
Input leakage current	$\|I_{LI}\|$	–	–	8	μA	V_{in} = V_{SS} to V_{CC}	
		–	–	2	μA	V_{in} = V_{SS} to 3.5V	
Output leakage current	$\|I_{LO}\|$	–	–	8	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	
		–	–	2	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to 3.5V	
Operating power supply current: DC	I_{CC}	–	10	25	mA	$\overline{CS}$ = V_{IL} $I_{I/O}$ = 0mA	
Average operating power supply current (1)	I_{CC1}	–	37	80	mA	MIN. cycle duty = 100%	–12
		–	35	80		$I_{I/O}$ = 0mA	–15
Average operating power supply current (2)	I_{CC2}	–	10	15	mA	$\overline{CS}$ = V_{IL}, V_{IH} = V_{CC} V_{IL} = 0V, $I_{I/O}$ = 0mA f = 1MHz	
Standby power supply current: DC	I_{SB}	–	2	12	mA	$\overline{CS}$ = V_{IH}	
Standby power supply current (1): DC	I_{SB1}	–	8	400	μA	$\overline{CS}$ ≥ V_{CC}–0.2V A15·A16 ≥ V_{CC} – 0.2V	HM66204L Series
		–	0.16	8	mA	or 0V ≦ A15·A16 ≦ 0.2V	
Output low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 2.1 mA	
Output high voltage	V_{OH}	2.4	–	–	V	I_{OH} = –1.0 mA	

Note) *1. Typical values are at V_{CC} = 5.0V, Ta = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	Cin	–	–	45	pF	Vin = 0V
Input/output capacitance	$C_{I/O}$	–	–	50	pF	$V_{I/O}$ = 0V

Note) This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

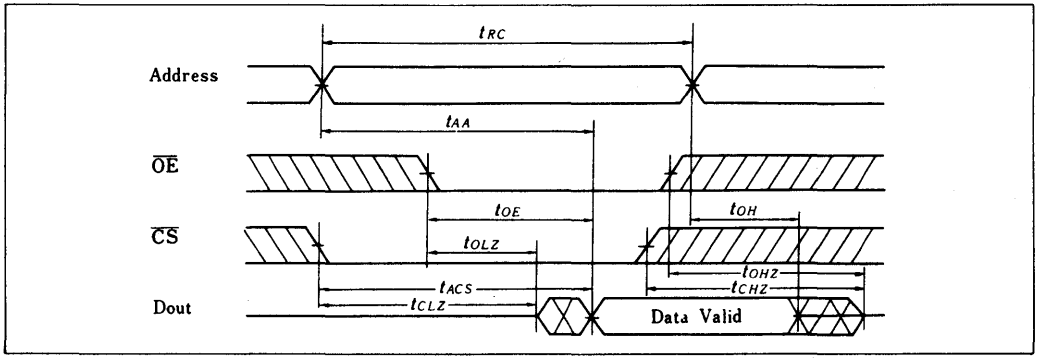
AC Test Conditions

- Input pulse levels:
  0.8V to 4.0V... $\overline{CS}$, A15, A16
  0.8V to 2.4V... Other pin except $\overline{CS}$, A15, A16
- Input rise and fall times: 5 ns
- Input and output timing reference level: 1.5V
- Output load: 1 TTL Gate and C_L (100pF) (Including scope & jig)

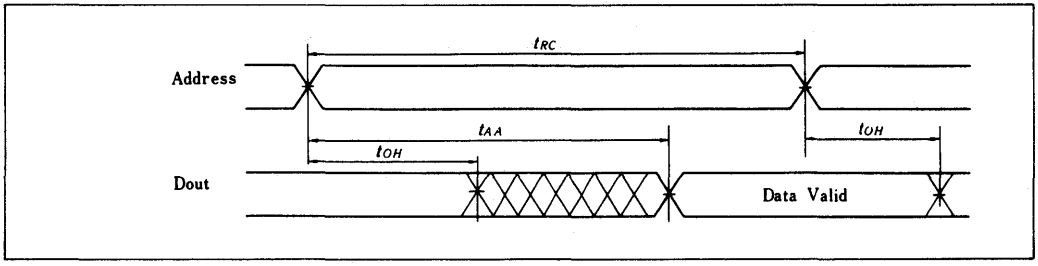
Read Cycle

Parameter	Symbol	HM66204-12		HM66204-15		Unit
		min	max	min	max	
Read cycle time	t_{RC}	120	–	150	–	ns
Address access time	t_{AA}	–	120	–	150	ns
Chip select access time	t_{ACS}	–	120	–	150	ns
Output enable to output valid	t_{OE}	–	60	–	70	ns
Output hold from address change	t_{OH}	10	–	10	–	ns
Chip selection to output in low Z	t_{CLZ}	10	–	10	–	ns
Output enable to output in low Z	t_{OLZ}	5	–	5	–	ns
Chip deselection to output in high Z	t_{CHZ}	0	40	0	50	ns
Output disable to output in high Z	t_{OHZ}	0	40	0	50	ns

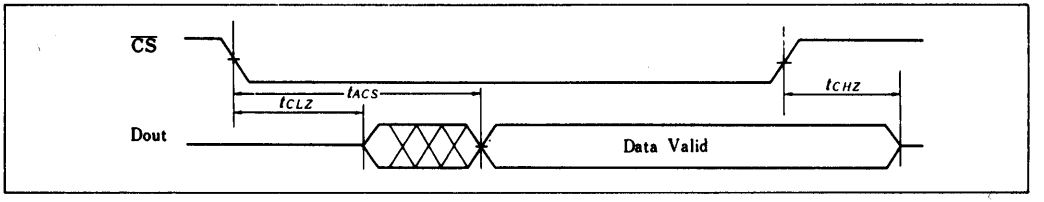
Read Cycle Timing No. 1 *1



Read Cycle Timing No. 2 *1,*2,*4



Read Cycle Timing No. 3 *1, *3, *4

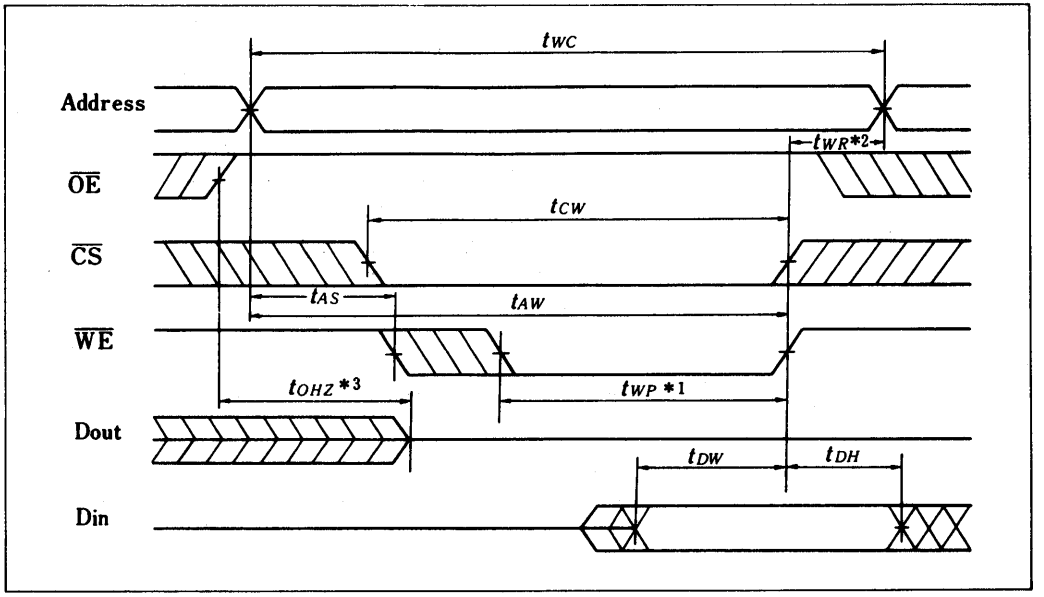


Notes) *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address should be valid prior to or coincident with $\overline{CS}$ transition low.
*4. $\overline{OE}$ = V_{IL}.

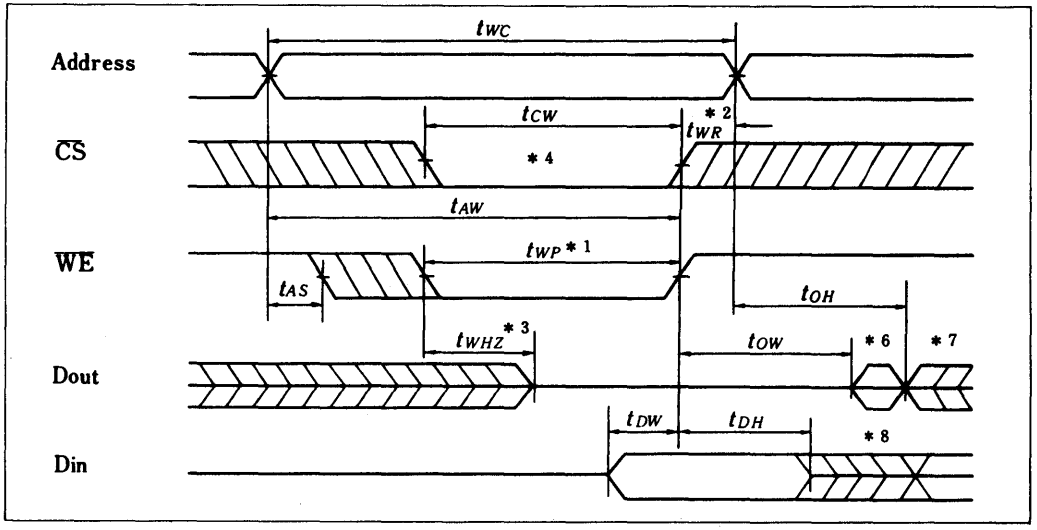
Write Cycle

Parameter	Symbol	HM66204-12		HM66204-15		Unit
		min	max	min	max	
Write cycle time	t_{WC}	120	–	150	–	ns
Chip selection to end of write	t_{CW}	100	–	120	–	ns
Address valid to end of write	t_{AW}	100	–	120	–	ns
Address setup time	t_{AS}	0	–	0	–	ns
Write pulse width	t_{WP}	90	–	110	–	ns
Write recovery time	t_{WR}	5	–	5	–	ns
Write to output in high Z	t_{WHZ}	0	40	0	50	ns
Data to write time overlap	t_{DW}	50	–	60	–	ns
Data hold from write time	t_{DH}	0	–	0	–	ns
Output disable to output in high Z	t_{OHZ}	0	40	0	50	ns
Output active from end of write	t_{OW}	5	–	5	–	ns

Write Cycle Timing No. 1 ($\overline{OE}$ Clock)



Write Cycle Timing No. 2*5 ($\overline{OE}$ Low Fixed)



Notes) *1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
*2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
*3. During this period, I/O pins are in the output state.
The input signals of opposite phase to the outputs must not be applied.
*4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
*5. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
*6. D_{out} should be held in phase of the written data during this write cycle.
*7. D_{out} is the read data of next address.
*8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. The input signals which are opposite to the output level should not be applied to I/O pins.

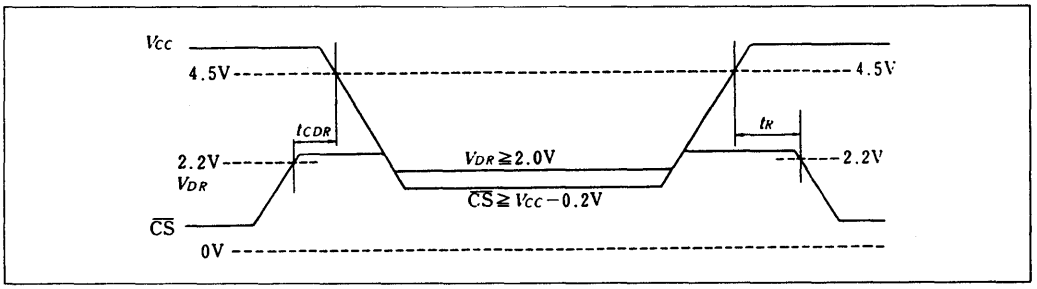
Low V_{CC} Data Retention Characteristics (Ta = 0°C to +70°C)

Data retention characteristics is guaranteed only for L version.

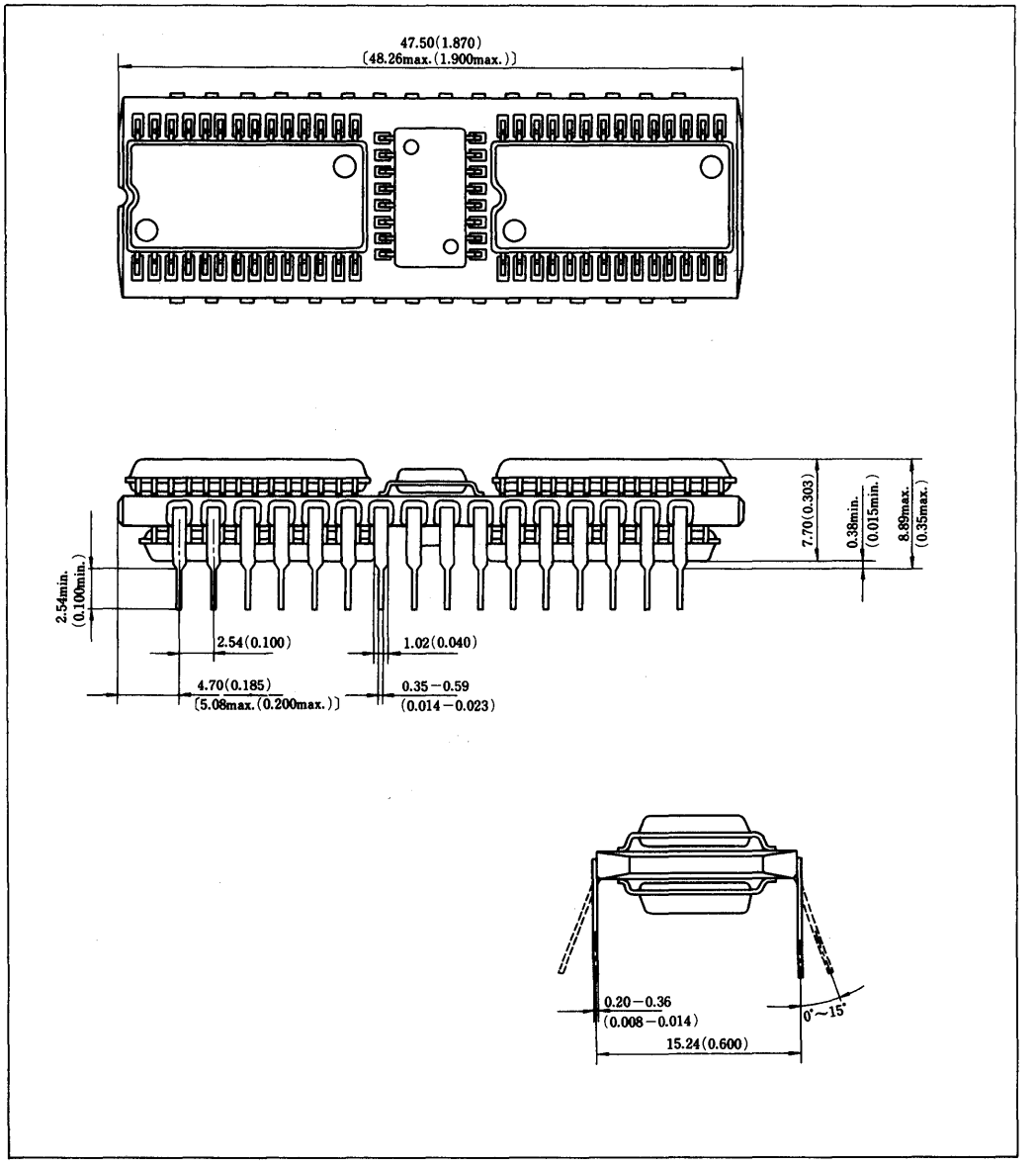
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2.0	–	–	V	$\overline{CS} \geq V_{CC}$ -0.2V A15, A16 $\geq V_{CC}$ -0.2V or A15, A16 $\leq$ 0.2V
Data retention current	I_{CCDR}	–	–	200	µA	V_{CC} = 3.0V, $\overline{CS} \geq$ 2.8V A15·A16 $\geq$ 2.8V or 0V $\leqq$ A15·A16 $\leqq$ 0.2V
Chip deselect to data retention time	t_{CDR}	0	–	–	ns	See retention waveform
Operation recovery time	t_R	t_{RC}*1	–	–	ns	

Note) *1. t_{RC} = Read Cycle Time.

Low V_{CC} Data Retention Waveform



Package Dimensions; Unit: mm (inch)



HM63921-20/25/35 — Product Preview

2K × 9-Bit CMOS Parallel In-Out FIFO Memory

■ DESCRIPTION

The HM63921 is a First-In, First-Out memory that utilizes a high performance static RAM array with internal algorithm that controls, monitors and declares status of the memory by empty flag, full flag and half-full flag, to prevent data overflow or underflow.

Expansion logic warrants unlimited expansion capability in width and depth. Both read and write are independent from each other and their corresponding pointers are designed to select the proper locations out of the entire array serially without address information to load or unload data.

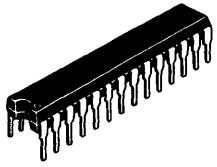
Data is toggled in and out of the device through the use of the write enable ($\overline{W}$) and read enable ($\overline{R}$) pins. The device has a read/write cycle time of 30/35/45ns. Organization of HM63921 provides a 9-bit data bus. the ninth bit could be used for control or parity for error checking at the option of the user. The HM63941 is fabricated using the Hitachi CMOS 1.3micron technology. The device is available in DIP.

■ FEATURES

- First-In, First-Out Dual Port Memory
- 2k × 9 Organization
- Low-Power CMOS 1.3micron Technology
- Asynchronous and Simultaneous Read and Write
- Fully Expandable in Depth and/or Width
- Single 5V (±10%) Power Supply
- Empty and Full Warning Flags
- Half-Full Flag
- Access Time 20/25/35ns
- Package . . . . . .300-mil 28-pin Plastic DIP Package

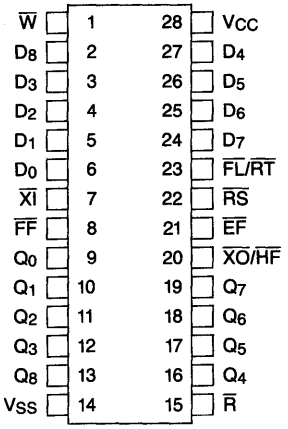
■ ORDERING INFORMATION

Type Name	Access Time	Package
HM63921P-20	20ns	300-mil 28-pin
HM63921P-25	25ns	Plastic DIP
HM63921P-35	35ns	(DP-28NA)



(DP-28NA)

■ PIN ARRANGEMENT

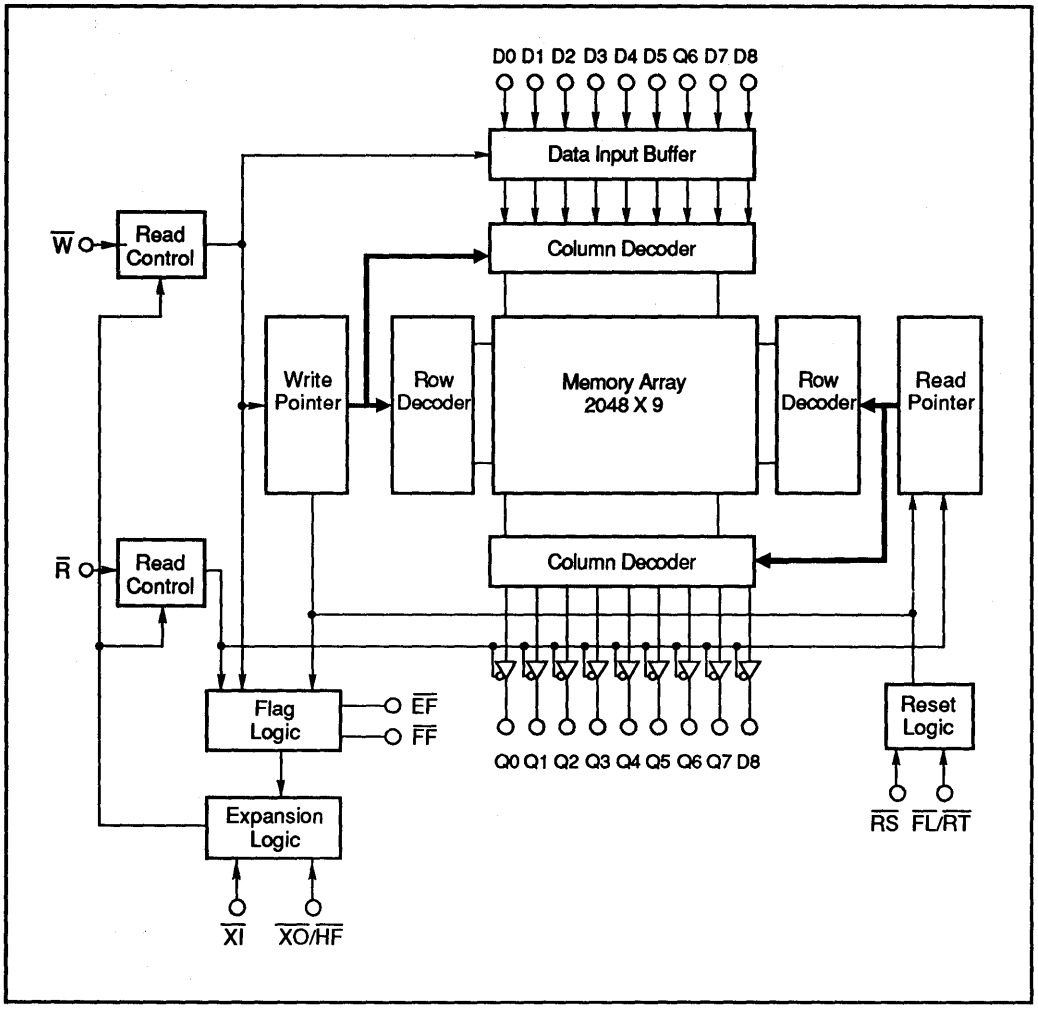


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
D_0–D_8	Data Inputs
$\overline{RS}$	Reset
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{FL}$	First Load
$\overline{RT}$	Retransmit
$\overline{XI}$	Expansion-In
$\overline{XO}$	Expansion-Out
$\overline{HF}$	Half-Full Flag
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
Q_0–Q_8	Data Outputs

■ BLOCK DIAGRAM



HITACHI

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■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage(1)	V_T	-0.5(2) to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

NOTES: 1. Relative to V_{SS}.
2. -3.5V for pulse width ≤ 10ns.

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-0.5(1)	—	0.8	V

NOTE: 1. -3.0V for pulse width ≤ 10ns.

■ DC CHARACTERISTICS (T_a = 0°C to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = 0V - V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{R}$ = V_{IH}, V_{out} = 0V - V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC1}	Average Operating Current	-20	—	120	mA
			-25	—	110	mA
			-35	—	100	mA
Standby Power Supply Current	I_{SB1}	$\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}	—	—	10	mA
	I_{SB2}	All inputs ≥ V_{CC} - 0.2V or ≤ V_{CC}	—	—	1	mA
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

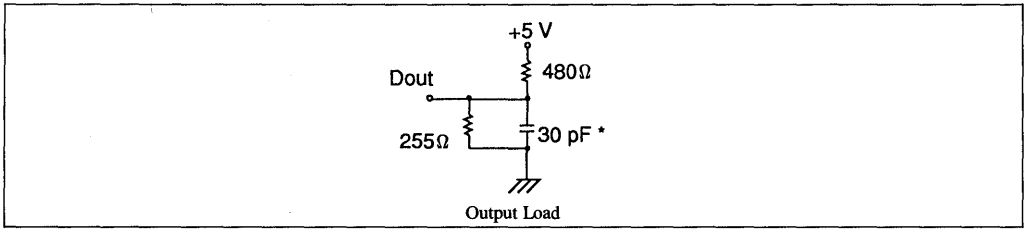
Parameter	Symbol	Test Conditions	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	—	6	pF
Output Capacitance	C_{out}	V_{out} = 0V	—	10	pF

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5 ± 10%)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Timing Reference Level: 1.5V
- Input Rise and Fall Times: 5ns
- Output Load: See Figure



*Including scope and jig.

• **Read Cycle**

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	30	—	35	—	45	—	ns
Access Time	t_A	—	20	—	25	—	35	ns
Read Recovery Time	t_{RR}	10	—	10	—	10	—	ns
Read Pulse Width	t_{RPW}	20	—	25	—	35	—	ns
Read Low to DB Low Z	t_{RLZ}(1)	5	—	5	—	5	—	ns
Read High to DB High Z	t_{RHZ}(1)	—	15	—	15	—	20	ns
Data Valid from Read High	t_{OH}	3	—	3	—	3	—	ns
Read Pulse Width After Empty Flag High	t_{RPE}	20	—	25	—	35	—	ns
Write High to DB Low Z (Read Data Flow Through Mode)	t_{WLZ}(1)	3	—	3	—	3	—	ns

NOTE: 1. t_{RLZ}, t_{RHZ} and t_{WLZ} are sampled and not 100% tested.

• **Write Cycle**

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	30	—	35	—	45	—	ns
Write Recovery Time	t_{WR}	10	—	10	—	10	—	ns
Write Pulse Width	t_{WPW}	20	—	25	—	35	—	ns
Data Setup Time	t_{DS}	10	—	15	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	5	—	ns
Effective Write Pulse Width After Full Flag High	t_{WPF}	20	—	25	—	35	—	ns

• **Reset Cycle**

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset Cycle Time	t_{RSC}	30	—	35	—	45	—	ns
Reset Pulse Width	t_{RS}	20	—	25	—	35	—	ns
Reset Setup Time	t_{RSS}	0	—	0	—	0	—	ns
Reset Recovery Time	t_{RSR}	10	—	10	—	10	—	ns

• **Retransmit Cycle**

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Retransmit Cycle Time	t_{RTC}	30	—	35	—	45	—	ns
Retransmit Pulse Width	t_{RT}	20	—	20	—	35	—	ns
Retransmit Setup Time	t_{RTS}	0	—	0	—	0	—	ns
Retransmit Recovery Time	t_{RTR}	10	—	10	—	10	—	ns

• Flag Timing

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset to Empty Flag Low	t_{EFL}	—	20	—	25	—	35	ns
Reset to Full Flag High	t_{FFH}	—	20	—	25	—	35	ns
Reset to Half-Full Flag High	t_{HFH}	—	30	—	35	—	45	ns
Read Low to Empty Flag Low	t_{REF}	—	20	—	25	—	35	ns
Read High to Full Flag High	t_{RFF}	—	20	—	25	—	35	ns
Write High to Empty Flag High	t_{WEF}	—	20	—	25	—	35	ns
Write Low to Full Flag Low	t_{WFF}	—	20	—	25	—	35	ns
Write Low to Half-Full Flag Low	t_{WHF}	—	30	—	35	—	45	ns
Read High to Half-Full Flag High	t_{RHF}	—	30	—	35	—	45	ns

• Expansion Timing

Parameter	Symbol	HM63921-20		HM63921-25		HM63921-35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Expansion in Setup to Write or Read	t_{EFL}	—	15	—	20	—	30	ns
Expansion in Recovery Time	t_{RFF}	—	15	—	20	—	30	ns
Expansion in Pulse Width	t_{WHF}	10	—	10	—	10	—	ns
Expansion Out High Delay From Clock	t_{REF}	10	—	10	—	10	—	ns
Expansion Out Low Delay From Clock	t_{RFF}	10	—	10	—	15	—	ns

SIGNAL DESCRIPTIONS

Inputs

- Reset ($\overline{RS}$)
  The device is reset whenever $\overline{RS}$ input is taken to low state, for minimum reset pulse width. When device is reset, both read and write pointers are set to the first location. A reset cycle is required after power on. Both read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must be in the high state during reset. Empty flag ($\overline{EF}$) will go low and full flag ($\overline{FF}$) and half-full ($\overline{HF}$) will go high during reset cycle.
- Write enable ($\overline{W}$)
  Write cycle is initiated at the falling edge of $\overline{W}$, if the full flag ($\overline{FF}$) is not set, provided that data set-up and hold time requirements relative to the rising edge of ($\overline{W}$) are met. Data is stored in the device sequentially and independently of any simultaneous read operation. To inhibit further write operations and prevent internal data overflow full flag ($\overline{FF}$) will go low.
- Read enable ($\overline{R}$)
  Read cycle is initiated at the falling edge of $\overline{R}$, if the empty flag ($\overline{EF}$) is not set. Data is accessed on a first-in, first-out basis independently of simultaneous write operation. As read enable ($\overline{R}$) goes high, all outputs will return to high impedance state, till next read operation. After the last data has been read from the FIFO, the empty flag ($\overline{EF}$) will go low, preventing further read operations with output kept in high impedance state. Empty flag ($\overline{EF}$) will go high during a valid write cycle (t_{WEF}), thereafter a valid read can start.
- First load/retransmit ($\overline{FL}/\overline{RT}$)
  For depth expansion mode, this pin is grounded to indicate that it is the first device, while this pin of the rest of devices should connect to V_{CC} for correct operation. In single device mode, this pin resets the read pointer to the beginning of the FIFO memory, therefore data can be reread from the beginning. Both $\overline{R}$ and $\overline{W}$ should be kept high while $\overline{RT}$ is taken low.
- Expansion-in ($\overline{XI}$)
  For single device mode expansion-in ($\overline{XI}$) is grounded. For depth expansion mode, expansion-in ($\overline{XI}$) should be connected to expansion-out ($\overline{XO}$) of previous device.
- Data In (D_0 to D_8)
  Data inputs for 9-bit wide data.

Outputs

- Full Flag ($\overline{FF}$)
  The full flag ($\overline{FF}$) will go low when FIFO is full, inhibiting further write operations until one or more read operations are completed or the FIFO is reset.
- Empty flag ($\overline{EF}$)
  The empty flag ($\overline{EF}$) will go low when the FIFO becomes empty, inhibiting further read operations, until one or more write operations are completed, or FIFO is set to retransmit.
- Expansion-out ($\overline{XO}$)/Half-full flag ($\overline{HF}$)
  This output has dual functionality depending how it is used. In depth expansion configuration expansion-out ($\overline{XO}$) is connected to next expansion-in ($\overline{XI}$). The expansion-out ($\overline{XO}$) of the last FIFO is connected to the expansion-in ($\overline{XI}$) of the first FIFO. In this way the first FIFO indicates the next FIFO that it will receive the next data. In like manner, any FIFO which becomes full will indicate the next FIFO that it will receive the next data. The second function of this output is in stand alone and/or parallel expansion configurations to indicate the system user that the FIFO is almost full.
- Data outputs (Q_0 to Q_8)
  Data outputs for 9-bit wide data. These outputs are in high impedance state when $\overline{R}$ is in high state.

VARIOUS OPERATIONS MODE

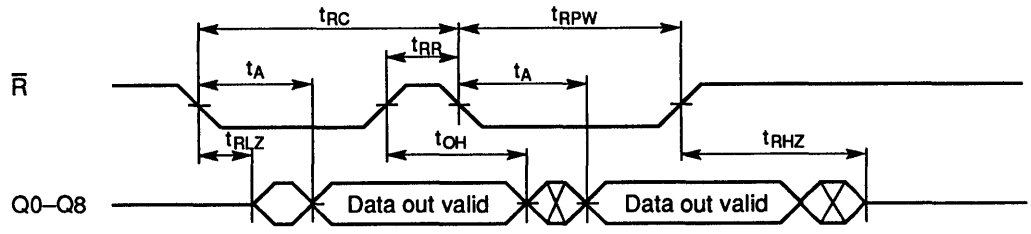
- Single device mode
  If only one FIFO is used, the expansion-in ($\overline{XI}$) pin should be grounded.
- Width expansion mode
  Width expansion by 9-bit increments may be achieved when separately paralleling the data inputs and the data outputs. In this configuration any flags of any device may be used. To avoid output contention of the flags for short periods of time, the flag outputs should not be wired together.
- Depth expansion mode
  Multiple of FIFOs could provide multiple of 2k × 9 as (N) × (2k) by 9-bits wide, where N is the number of FIFOs connected in depth expansion mode.

  The following arrangement must be provided.

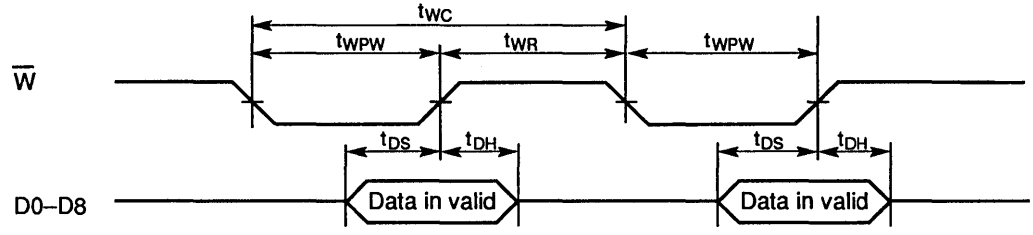
  1. First load ($\overline{FL}$) of the first FIFO should be connected to ground.
  2. All other ($\overline{FL}$) should be connected to V_{CC}.
  3. Connect the expansion-out ($\overline{XO}$) of each FIFO to expansion-in ($\overline{XI}$) of the next FIFO serially and $\overline{XO}$ of the last FIFO to $\overline{XI}$ of the first FIFO.
  4. Connect all the empty flag ($\overline{EF}$) together to OR gate and connect all the full flag ($\overline{FF}$) together to OR gate to obtain two separate valid empty flag ($\overline{EF}$) and full flag ($\overline{FF}$) outputs.
  5. ($\overline{RT}$) and ($\overline{AF}$) will not be available in this mode.
- Compound expansion mode
  Combination of width and depth expansion modes will provide larger FIFO arrays.

■ TIMING WAVEFORM

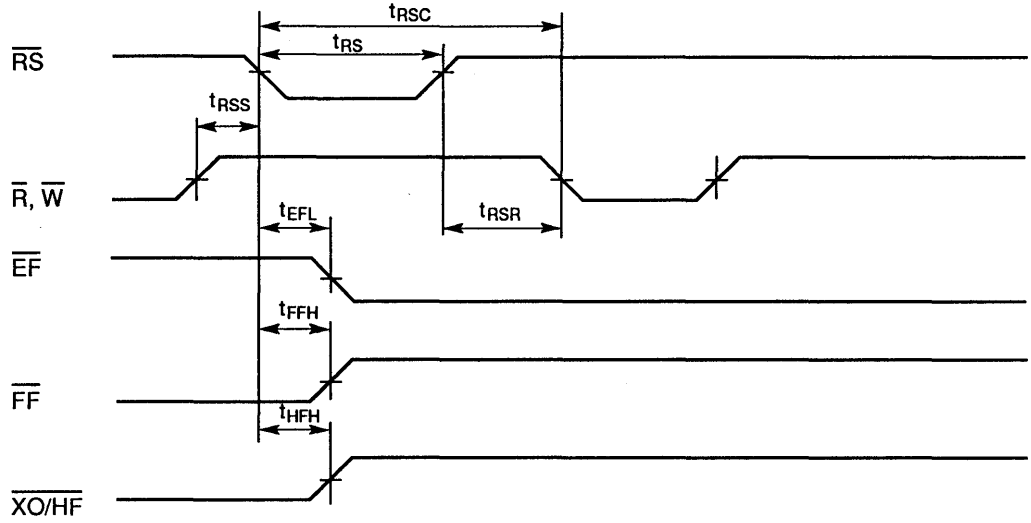
• Read Cycle



• Write Cycle



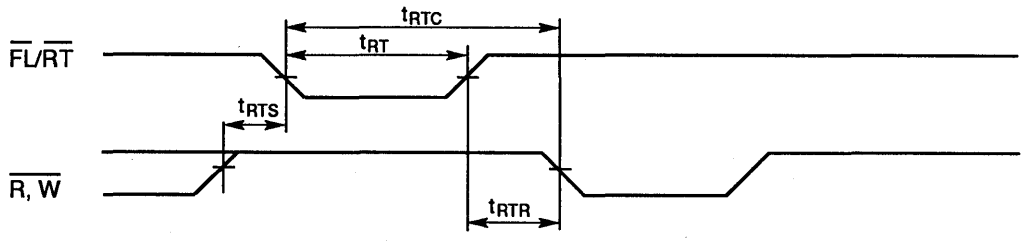
• Reset Cycle



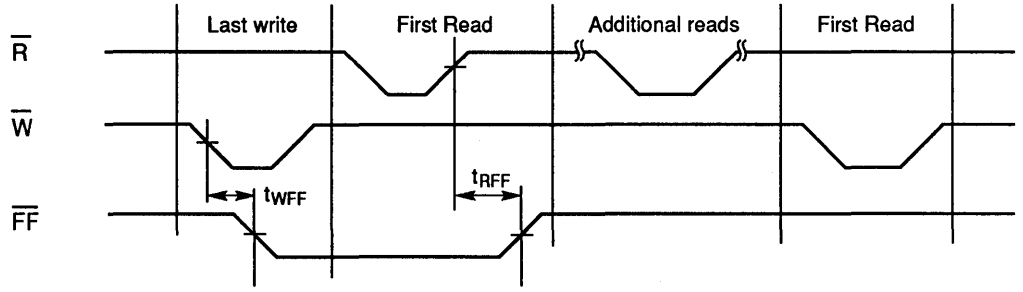
NOTES: 1. $\overline{W} = \overline{R} = V_{IH}$ during reset.

2. $t_{RSC} = t_{RST}, t_{RSR}$.

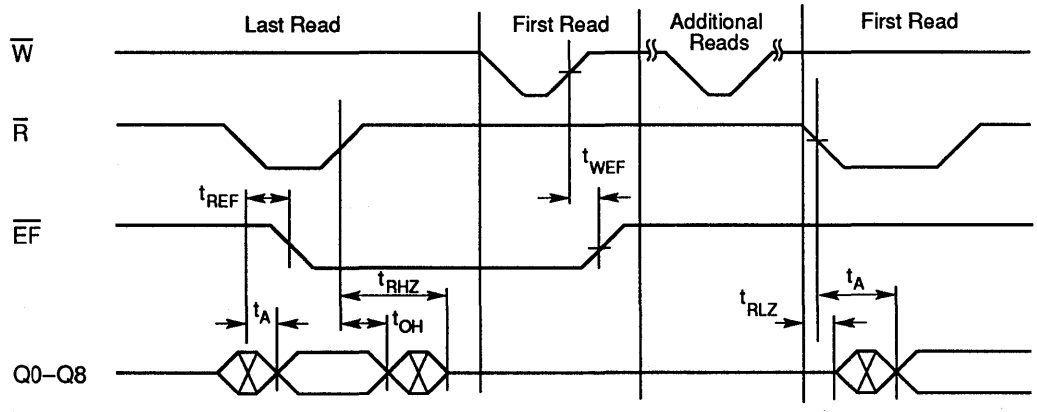
• **Retransmit Cycle**



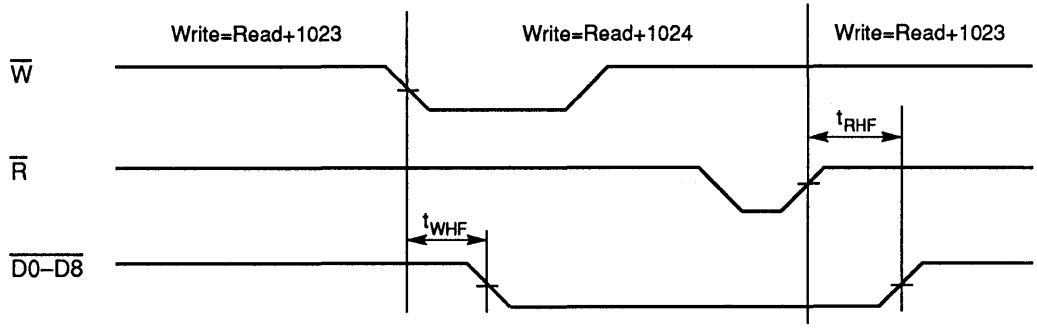
• **Full-Flag Cycle** (From Last Write to First Read)



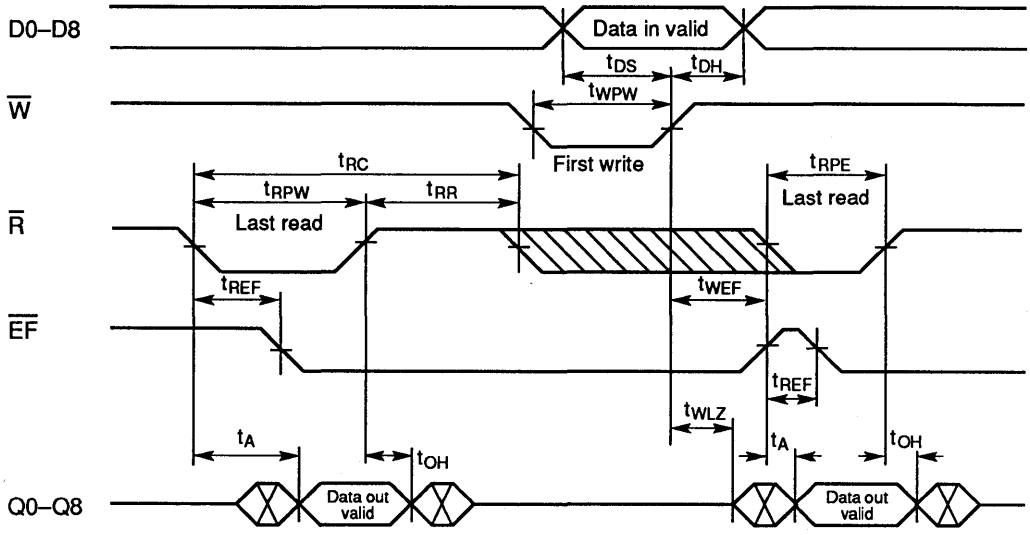
• **Empty-Flag Cycle** (From Last Read to First Write)



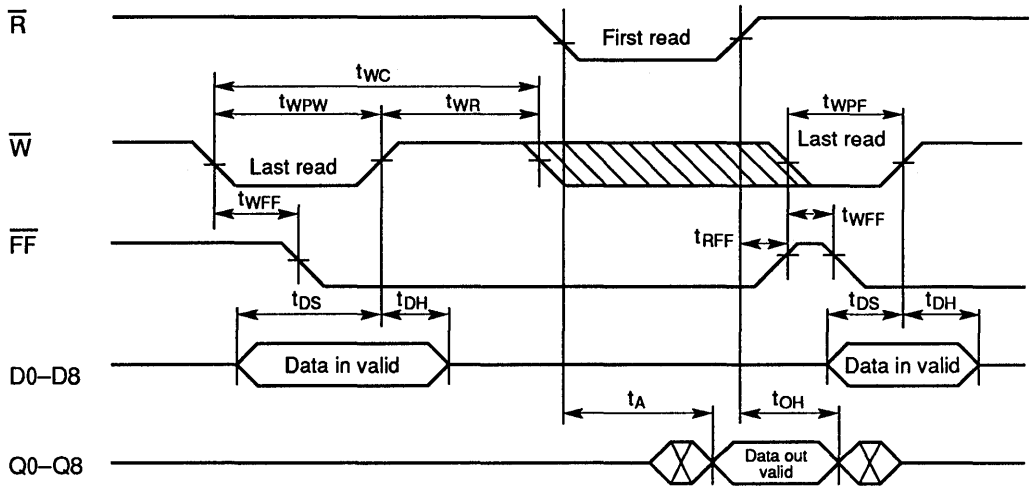
• **Half-Full Flag Cycle**



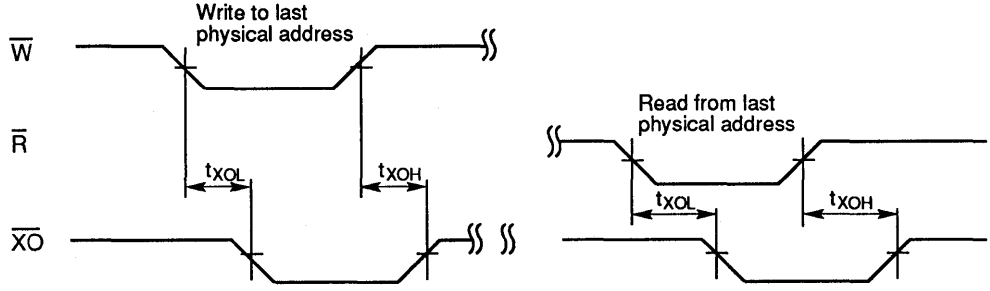
• **Read Data Flow Through Mode**



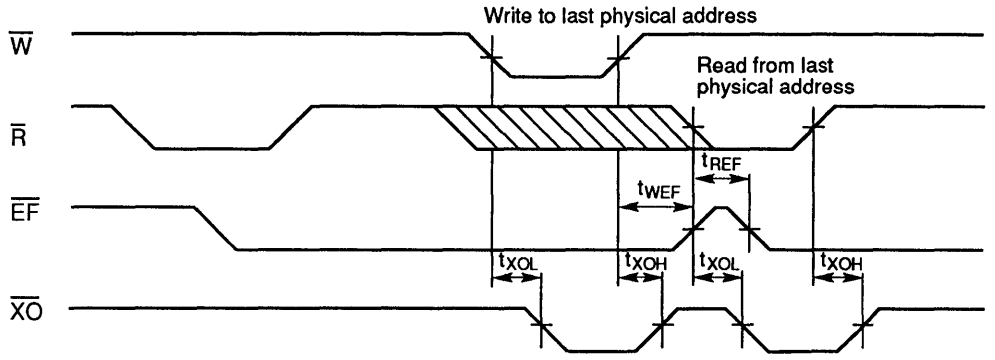
• **Write Data Flow Through Mode**



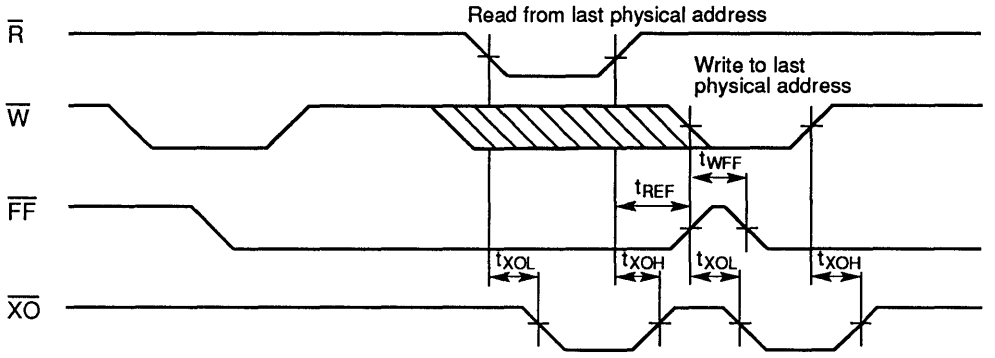
• **Expansion Out Cycle 1**



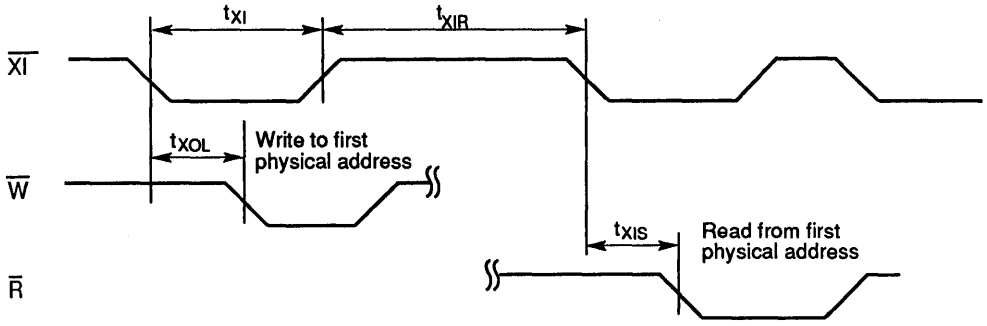
• **Expansion Out Cycle 2** (Read Data Flow Through Mode)



• **Expansion Out Cycle 3** (Write Data Flow Through Mode)



• **Expansion In Cycle**



HM63941-25/35/45 — Preliminary

4K × 9-Bit CMOS Parallel In-Out FIFO Memory

■ DESCRIPTION

The HM63941 is a First-In, First-Out memory that utilizes a high performance static RAM array with internal algorithm that controls, monitors and declares status of the memory by empty flag, full flag and almost-full flag, to prevent data overflow or underflow.

Expansion logic warrants unlimited expansion capability in width and depth. Both read and write are independent from each other and their corresponding pointers are designed to select the proper locations out of the entire array serially without address information to load or unload data.

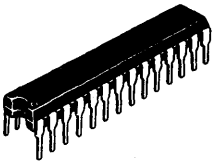
Data is toggled in and out of the device through the use of the write enable ($\overline{W}$) and read enable ($\overline{R}$) pins. The device has a read/write cycle time of 35/45/60ns. Organization of HM63941 provides a 9-bit data bus. the ninth bit could be used for control or parity for error checking at the option of the user. The HM63941 is fabricated using the Hitachi CMOS 1.3micron technology. The device is available in DIP.

■ FEATURES

- First-In, First-Out Dual Port Memory
- 4k × 9 Organization
- Low-Power CMOS 1.3micron Technology
- Asynchronous and Simultaneous Read and Write
- Fully Expandable in Depth and/or Width
- Single 5V (±10%) Power Supply
- Empty and Full Warning Flags
- Almost-Full Flag
- Access Time 25/35/45ns
- Package.....28-pin DIP Package

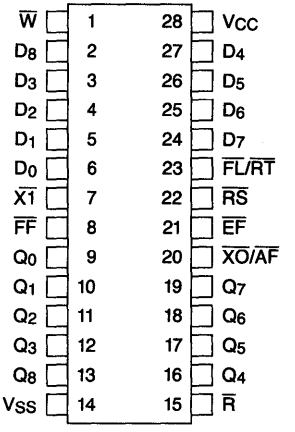
■ ORDERING INFORMATION

Type Name	Access Time	Package
HM63941P-25	25ns	28-pin Plastic DIP
HM63941P-35	35ns	
HM63941P-45	45ns	



(DP-28NA)

■ PIN ARRANGEMENT



(Top View)

■ PIN DESCRIPTION

Pin Name	Function
D_0–D_8	Data inputs
$\overline{RS}$	Reset
$\overline{W}$	Write enable
$\overline{R}$	Read enable
$\overline{FL}$	First load
$\overline{RT}$	Retransmit
$\overline{XI}$	Expansion-in
$\overline{XO}$	Expansion-out
$\overline{AF}$	Almost-full flag
$\overline{FF}$	Full flag
$\overline{EF}$	Empty flag
Q_0–Q_8	Data outputs

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage(1)	V_T	-0.5(2) to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

NOTES: 1. Relative to V_{SS}.
2. -3.5V for pulse width ≤ 10ns.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.0	—	6.0	V
	V_{IL}	-0.5(1)	—	0.8	V

NOTE: 1. -3.0V for pulse width ≤ 10ns.

■ DC CHARACTERISTICS (T_a = 0°C to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	$\|I_{LI}\|$	V_{CC} = 5.5V, V_{in} = 0V - V_{CC}	—	—	2	μA
Output Leakage Current	$\|I_{LO}\|$	$\overline{R}$ = V_{IH}, V_{out} = 0V - V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC1}	Average Operating Current	—	—	80	mA
	I_{CC2}	$\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}	—	—	10	mA
Standby Power Supply Current	I_{SB}	All Inputs ≥ V_{CC} - 0.2V or ≤ V_{CC}	—	—	1	mA
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

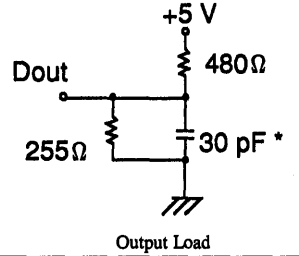
■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Conditions	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	—	TBD	pF
Output Capacitance	C_{out}	V_{out} = 0V	—	TBD	pF

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5 ± 10%)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Timing Reference Level: 1.5V
- Input Rise and Fall Times: 5ns
- Output Load: See Figure



Output Load

*Including scope and jig.

• Read Cycle

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	35	—	45	—	60	—	ns
Access Time	t_A	—	25	—	35	—	45	ns
Read Recovery Time	t_{RR}	10	—	10	—	15	—	ns
Read Pulse Width	t_{RPW}	25	—	35	—	45	—	ns
Read Low to DB Low Z	t_{RLZ}	5	—	5	—	10	—	ns
Read High to DB High Z	t_{RHZ}	—	15	—	20	—	25	ns
Data Valid from Read High	t_{OH}	5	—	5	—	5	—	ns

• Write Cycle

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	35	—	45	—	60	—	ns
Write Recovery Time	t_{WR}	10	—	10	—	15	—	ns
Write Pulse Width	t_{WPW}	20	—	35	—	45	—	ns
Data Setup Time	t_{DS}	15	—	20	—	25	—	ns
Data Hold Time	t_{DH}	0	—	0	—	5	—	ns

• Reset Cycle

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset Cycle Time	t_{RSC}	35	—	45	—	60	—	ns
Reset Pulse Width	t_{RS}	25	—	35	—	45	—	ns
Reset Recovery Time	t_{RSR}	10	—	10	—	15	—	ns

• Retransmit Cycle

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Retransmit Cycle Time	t_{RTC}	35	—	45	—	60	—	ns
Retransmit Pulse Width	t_{RT}	20	—	35	—	45	—	ns
Retransmit Recovery Time	t_{RTR}	10	—	10	—	15	—	ns

• Flag Timing

Parameter	Symbol	HM63941-25		HM63941-35		HM63941-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset to Empty Flag Low	t_{EFL}	—	30	—	45	—	60	ns
Read Low to Empty Flag Low	t_{REF}	—	25	—	35	—	45	ns
Read High to Full Flag High	t_{RFF}	—	25	—	35	—	45	ns
Write High to Empty Flag High	t_{WEF}	—	25	—	35	—	45	ns
Write Low to Full Flag Low	t_{WFF}	—	25	—	35	—	45	ns
Write Low to Almost-Full Low	t_{WAF}	—	30	—	40	—	55	ns
Read High to Almost-Full High	t_{RAF}	—	30	—	40	—	55	ns

SIGNAL DESCRIPTIONS

Inputs

- Reset ($\overline{RS}$)
  The device is reset whenever $\overline{RS}$ input is taken to low state, for minimum reset pulse width. When device is reset, both read and write pointers are set to the first location. A reset cycle is required after power on. Both read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must be in the high state during reset. Empty flag ($\overline{EF}$) will go low and full flag ($\overline{FF}$) and almost-full ($\overline{AF}$) will go high during reset cycle.
- Write enable ($\overline{W}$)
  Write cycle is initiated at the falling edge of $\overline{W}$, if the full flag ($\overline{FF}$) is not set, provided that data set-up and hold time requirements relative to the rising edge of ($\overline{W}$) are met. Data is stored in the device sequentially and independently of any simultaneous read operation. To inhibit further write operations and prevent internal data overflow full flag ($\overline{FF}$) will go low.
- Read enable ($\overline{R}$)
  Read cycle is initiated at the falling edge of $\overline{R}$, if the empty flag ($\overline{EF}$) is not set. Data is accessed on a first-in, first-out basis independently of simultaneous write operation. As read enable ($\overline{R}$) goes high, all outputs will return to high impedance state, till next read operation. After the last data has been read from the FIFO, the empty flag ($\overline{EF}$) will go low, preventing further read operations with output kept in high impedance state. Empty flag ($\overline{EF}$) will go high during a valid write cycle (t_{WEF}), thereafter a valid read can start.
- First load/retransmit ($\overline{FL}/\overline{RT}$)
  For depth expansion mode, this pin is grounded to indicate that it is the first device, while this pin of the rest of devices should connect to V_{CC} for correct operation. In single device mode, this pin resets the read pointer to the beginning of the FIFO memory, therefore data can be reread from the beginning. Both $\overline{R}$ and $\overline{W}$ should be kept high while $\overline{RT}$ is taken low.
- Expansion-in ($\overline{XI}$)
  For single device mode expansion-in ($\overline{XI}$) is grounded. For depth expansion mode, expansion-in ($\overline{XI}$) should be connected to expansion-out ($\overline{XO}$) of previous device.
- Data In (D_0 to D_8)
  Data inputs for 9-bit wide data.

Outputs

- Full Flag ($\overline{FF}$)
  The full flag ($\overline{FF}$) will go low when FIFO is full, inhibiting further write operations until one or more read operations are completed or the FIFO is reset.
- Empty flag ($\overline{EF}$)
  The empty flag ($\overline{EF}$) will go low when the FIFO becomes empty, inhibiting further read operations, until one or more write operations are completed, or FIFO is set to retransmit.
- Expansion-out ($\overline{XO}$)/Almost-full flag ($\overline{AF}$)
  This output has dual functionality depending how it is used. In depth expansion configuration expansion-out ($\overline{XO}$) is connected to next expansion-in ($\overline{XI}$). The expansion-out ($\overline{XO}$) of the last FIFO is connected to the expansion-in ($\overline{XI}$) of the first FIFO. In this way the first FIFO indicates the next FIFO that it will receive the next data. In like manner, any FIFO which becomes full will indicate the next FIFO that it will receive the next data. The second function of this output is in stand alone and/or parallel expansion configurations to indicate the system user that the FIFO is almost full.
- Data outputs (Q_0 to Q_8)
  Data outputs for 9-bit wide data. These outputs are in high impedance state when $\overline{R}$ is in high state.

VARIOUS OPERATIONS MODE

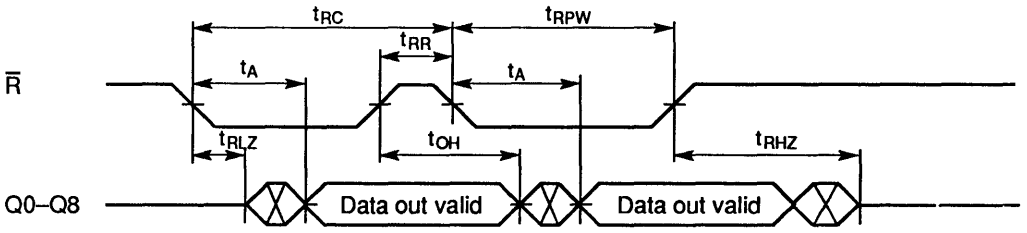
- Single device mode
  If only one FIFO is used, the expansion-in ($\overline{XI}$) pin should be grounded.
- Width expansion mode
  Width expansion by 9-bit increments may be achieved when separately paralleling the data inputs and the data outputs. In this configuration any flags of any device may be used. To avoid output contention of the flags for short periods of time, the flag outputs should not be wired together.
- Depth expansion mode
  Multiple of FIFOs could provide multiple of 4k × 9 as (N) × (4k) by 9-bits wide, where N is the number of FIFOs connected in depth expansion mode.

  The following arrangement must be provided.

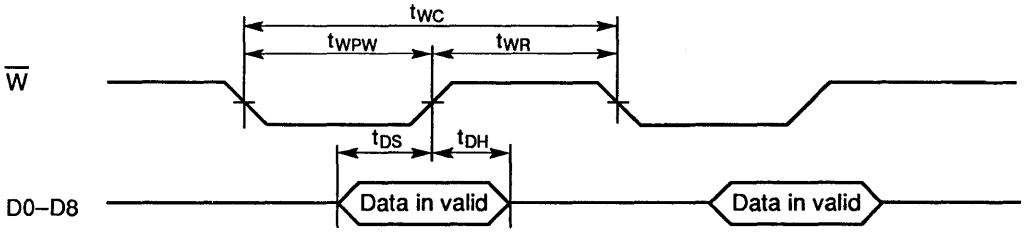
  1. First load ($\overline{FL}$) of the first FIFO should be connected to ground.
  2. All other ($\overline{FL}$) should be connected to V_{CC}.
  3. Connect the expansion-out ($\overline{XO}$) of each FIFO to expansion-in ($\overline{XI}$) of the next FIFO serially and $\overline{XO}$ of the last FIFO to $\overline{XI}$ of the first FIFO.
  4. Connect all the empty flag ($\overline{EF}$) together to OR gate and connect all the full flag ($\overline{FF}$) together to OR gate to obtain two separate valid empty flag ($\overline{EF}$) and full flag ($\overline{FF}$) outputs.
  5. ($\overline{RT}$) and ($\overline{AF}$) will not be available in this mode.
- Compound expansion mode
  Combination of width and depth expansion modes will provide larger FIFO arrays.

■ TIMING WAVEFORM

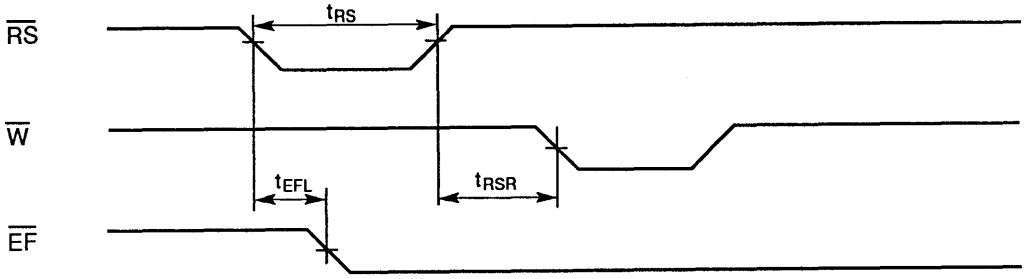
• Read Cycle



• Write Cycle



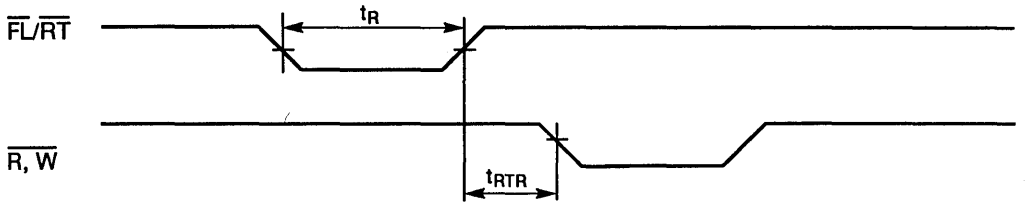
• Reset Cycle



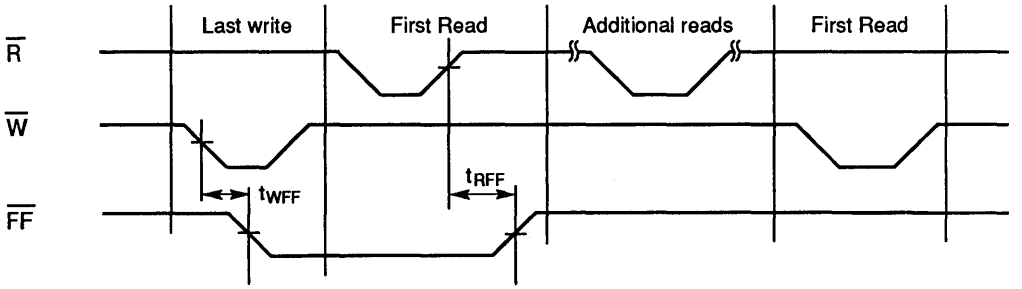
NOTES: 1. $\overline{W} = \overline{R} = V_{IH}$ during reset.

2. $t_{RSC} = t_{RST}, t_{RSR}$.

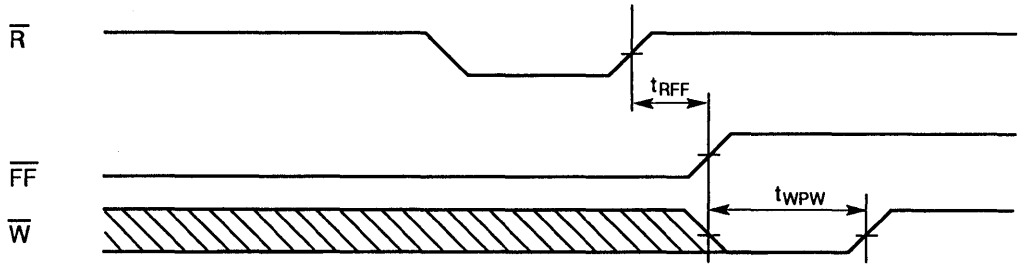
• **Retransmit Cycle**



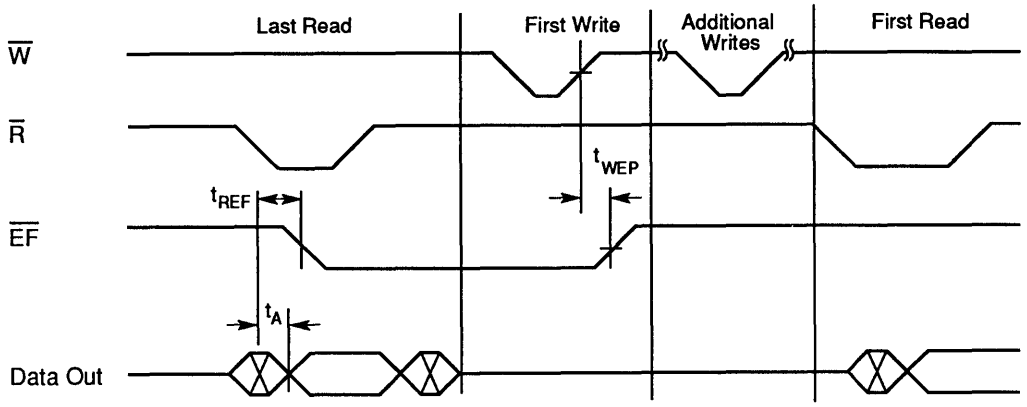
• **Full-Flag Cycle** (From Last Write to First Read)



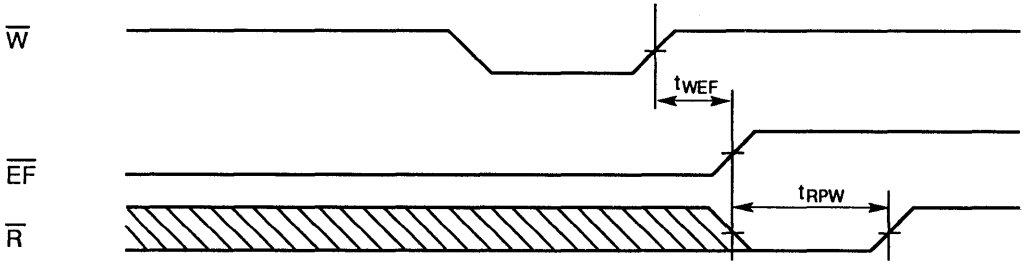
• **Full-Flag Cycle** (Effective Write Pulse Width After $\overline{FF}$ High)



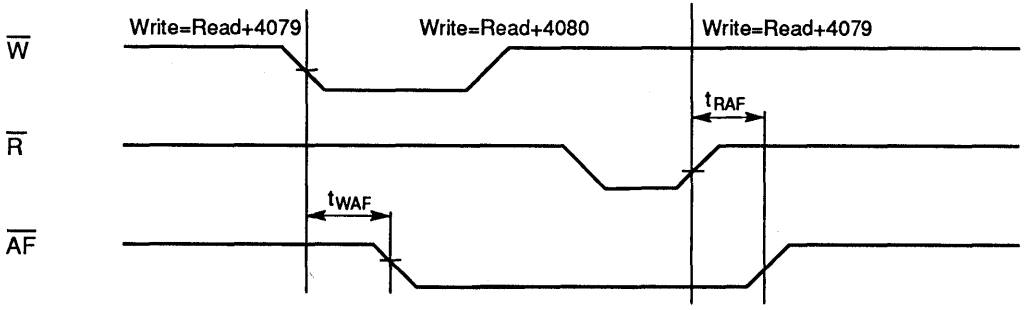
• **Empty-Flag Cycle** (From Last Write to First Read)



• **Empty-Flag Cycle** (Effective Read Pulse Width After $\overline{EF}$ High)



• **Almost-Full Flag Cycle**



Section 3
Cache Static RAM and Fast SRAM Modules

3

HITACHI®

HM62A168/HM62A188 Series — Preliminary

Direct Mapped 8,192-Word × 16/18-Bit
2-Way 4,096-Word × 16/18-Bit Static Cache RAM

■ DESCRIPTION

The Hitachi HM62A168/HM62A188 is a high speed 128/144-kbit static cache RAM organized as 2-way set associative 4k × 16/18 or direct mapped 8k × 16/18. By using two HM62A168/HM62A188 with Intel's 82385 cache controller a high performance 80386 system can be achieved.

The HM62A168/HM62A188, packaged in a 52-pin PLCC is available for high density mounting.

■ FEATURES

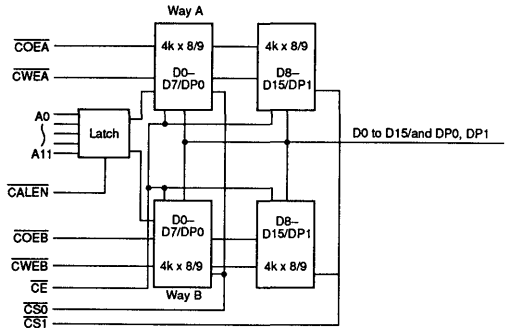
- Meets INTEL 82385 cache memory controller
- High Speed
  Access Time .....25/35/45ns (max.)
- Address Latch
- Pin Programmable for 8k × 16/18 or 2-Way 4k × 16/18

■ ORDERING INFORMATION

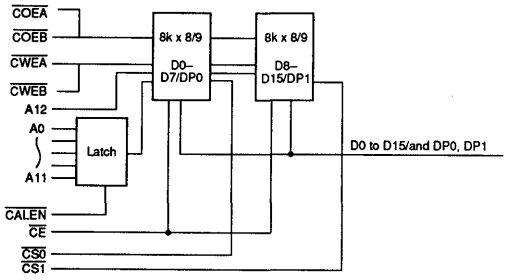
Type No.	Access	Package
HM62168CP-25	25ns	52-pin PLCC
HM62168CP-35	35ns	
HM62168CP-45	45ns	
HM62188CP-25	25ns	52-pin PLCC
HM62188CP-35	35ns	
HM62188CP-45	45ns	

■ BLOCK DIAGRAM

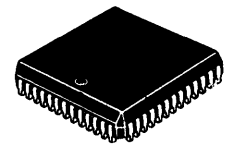
Topology Two-Way Set Associative (MODE = Logic Low)



Topology Direct Map (MODE = Logic Low)



■ PIN-OUT

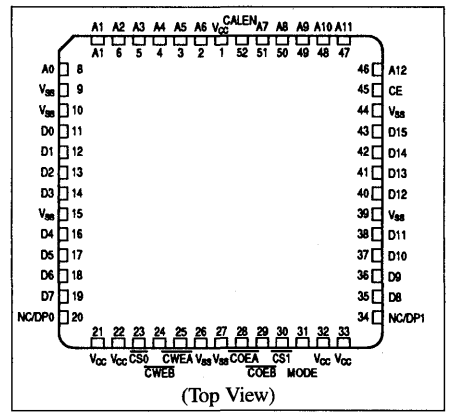


(CP-52)

■ PIN DESCRIPTION

Pin Name	Function
CALEN	Cache Address Latch Enable
MODE	Mode Select
A_0 to A_{12}	Address
$\overline{CS_0}$, $\overline{CS_1}$	Cache Chip Select
$\overline{COEA}$, $\overline{COEB}$	Cache Output Enable
$\overline{CWEA}$, $\overline{CWEB}$	Cache Write Enable
D_0 to D_{15}	Data Input/Output
$\overline{CE}$	Cache Chip Enable
NC/DP_0, DP_1	No connection Parity Input/Output

■ PIN ARRANGEMENT



(Top View)

■ FUNCTION TABLE

• Two-Way Mode (Mode = High) 2-4K × 16/18

Input Signal							I/O Pin		Function
$\overline{CE}$	$\overline{CS_0}$	$\overline{CS_1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	D_0–D_7/DP_0	D_8–D_{15}/DP_1	
H	X	X	X	X	X	X	High-Z	High-Z	Disabled
X	H	H	X	X	X	X	High-Z	High-Z	Disabled
L	L	H	L	H	H	H	Output	High-Z	Read Way A
L	L	H	H	L	H	H	Output	High-Z	Read Way B
L	H	L	L	H	H	H	High-Z	Output	Read Way A
L	H	L	H	L	H	H	High-Z	Output	Read Way B
L	L	L	L	H	H	H	Output	Output	Read Way A
L	L	L	H	L	H	H	Output	Output	Read Way B
L	L	H	X	X	L	H	Input	High-Z	Write Way A
L	L	H	X	X	H	L	Input	High-Z	Write Way B
L	H	L	X	X	L	H	High-Z	Input	Write Way A
L	H	L	X	X	H	L	High-Z	Input	Write Way B
L	L	L	X	X	L	H	Input	Input	Write Way A
L	L	L	X	X	H	L	Input	Input	Write Way B
L	L	H	X	X	L	L	Input	High-Z	Write Way A & B
L	H	L	X	X	L	L	High-Z	Input	Write Way A & B
L	L	L	X	X	L	L	Input	Input	Write Way A & B

• Direct Mode (Mode = Low) 8K × 16/18

Input Signal							I/O Pin		Function
$\overline{CE}$	$\overline{CS_0}$	$\overline{CS_1}$	$\overline{COEA}$	$\overline{COEB}$	$\overline{CWEA}$	$\overline{CWEB}$	D_0–D_7/DP_0	D_8–D_{15}/DP_1	
H	X	X	X	X	X	X	High-Z	High-Z	Disabled
X	H	H	X	X	X	X	High-Z	High-Z	Disabled
X	X	X	H	H	X	X	High-Z	High-Z	Disabled
L	L	H	L	L	H	H	Output	High-Z	Read D_0 to D_7
L	H	L	L	L	H	H	High-Z	Output	Read D_8 to D_{15}
L	L	L	L	L	H	H	Output	Output	Read D_0 to D_{15}
L	L	H	X	X	L	L	Input	High-Z	Write D_0 to D_7
L	H	L	X	X	L	L	High-Z	Input	Write D_8 to D_{15}
L	L	L	X	X	L	L	Input	Input	Write D_0 to D_{15}

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}	−0.5[1] to +7.0	V
Power Dissipation	P_T	1.2	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	−10 to +85	°C

NOTE: 1. V_{in} min. = −2.5V for pulse width ≤ 10ns.

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low (Logic 0) Voltage	V_{IL}	−0.3(1)	—	0.8	V

NOTE: 1. V_{IL} min. = −2.0V for pulse width ≤ 10ns.

■ DC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min.	Typ.(1)	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}	—	—	2.0	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	—	—	10.0	μA
Operating Power Supply Current	I_{CC}	V_{in} = 0V/V_{CC}, $I_{I/O}$ = 0mA Min. Cycle, Duty = 100%	—	—	220	mA
Output Low Voltage	V_{OL}	I_{OL} = 4mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −1.0mA	2.4	—	—	V

NOTE: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)(1)

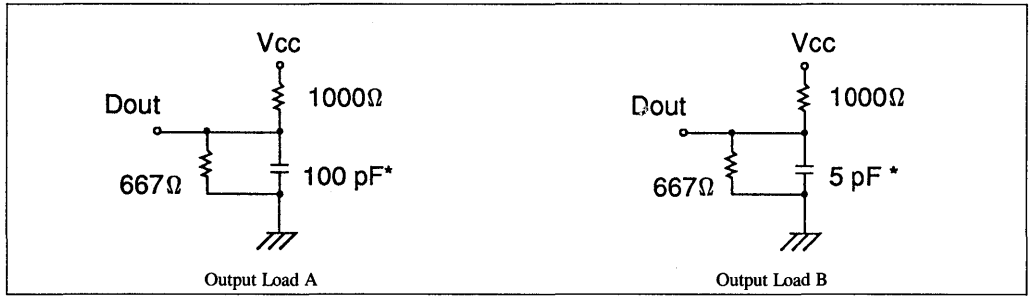
Parameter	Symbol	Max.	Max.	Unit	Test Conditions
Input Capacitance	C_{in}	—	6	pF	V_{in} = 0V
Input/Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

NOTE: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Timing Reference Levels: 1.5V
- Input Rise and Fall Times: 3ns
- Output Load: See Figures



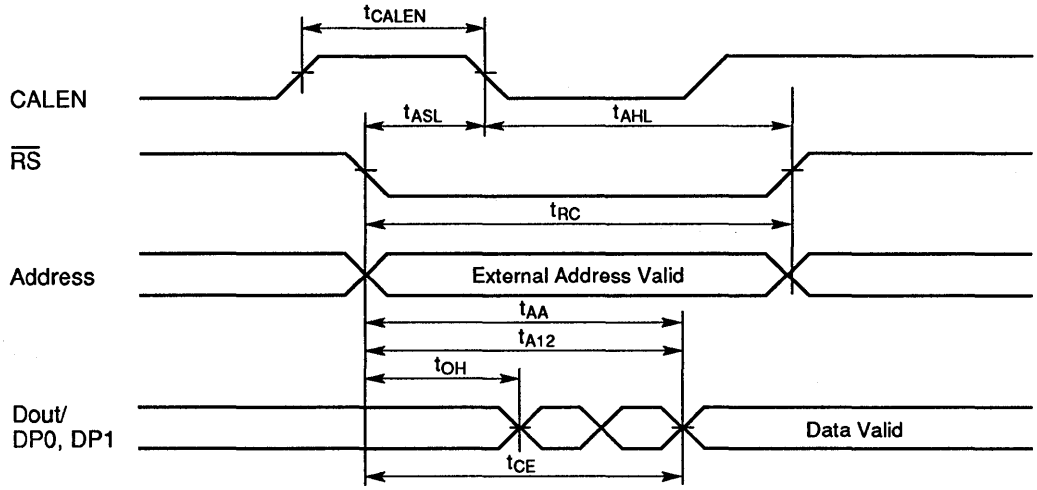
Output Load A　　Output Load B

*Including scope and jig.

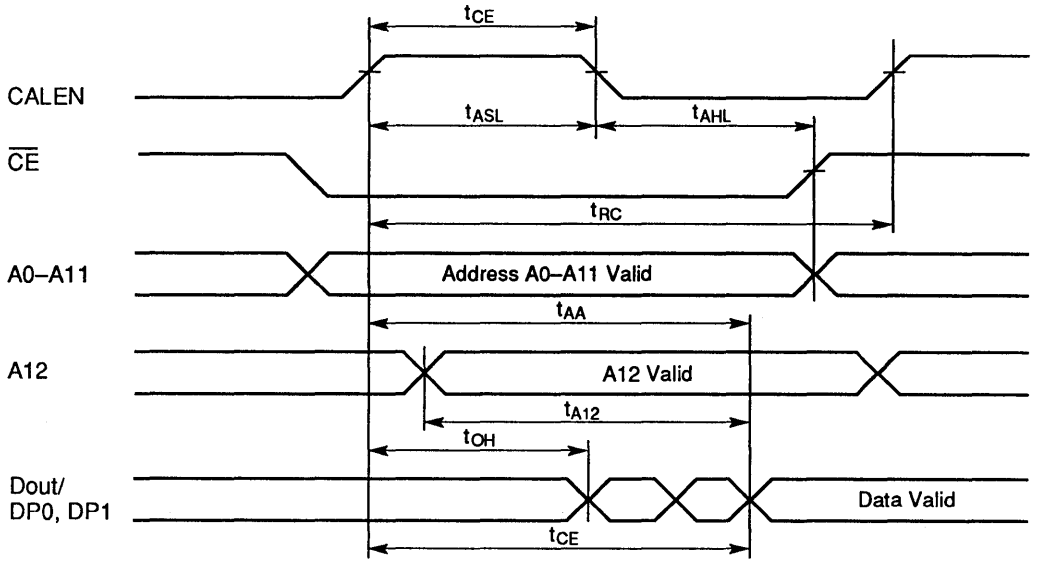
• **Read Cycle**

Parameter	Symbol	HM62168-25 HM62188-25		HM62168-35 HM62188-35		HM62168-45 HM62188-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
A_{12} Address Access Time	t_{A12}	—	17	—	25	—	30	ns
Chip Select Access Time	t_{CS}, t_{CE}	—	20	—	25	—	30	ns
Output Enable to Output Valid	t_{OE}	—	10	—	13	—	16	ns
Output Hold from Address Change	t_{OH}	3	—	3	—	3	—	ns
Chip Select to Output Low-Z	t_{LZ}	3	—	3	—	3	—	ns
Output Enable to Output Low-Z	t_{OLZ}	2	—	2	—	2	—	ns
Chip Deselect to Output in High-Z	t_{HZ}	—	15	—	25	—	30	ns
Output Disable to Output High-Z	t_{OHZ}	—	10	—	14	—	14	ns
Address Latch Enable Pulse Width	t_{CALEN}	8	—	10	—	15	—	ns
Address Setup to Latch Low	t_{ASL}	4	—	6	—	10	—	ns
Address Hold to Latch Low	t_{AHL}	5	—	5	—	5	—	ns

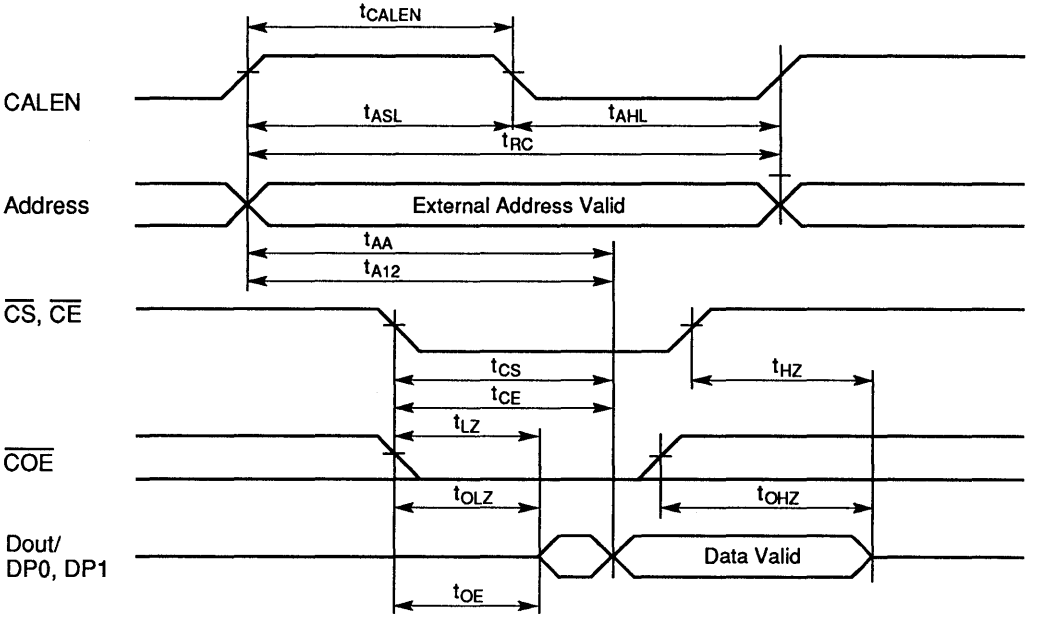
• **Read Timing Waveform (1)** ($\overline{CWE}$ = High, $\overline{COE}$ = Low, $\overline{CS}$ = Low)



• **Read Timing Waveform (2)** ($\overline{CWE}$ = High, $\overline{COE}$ = Low, $\overline{CS}$ = Low)



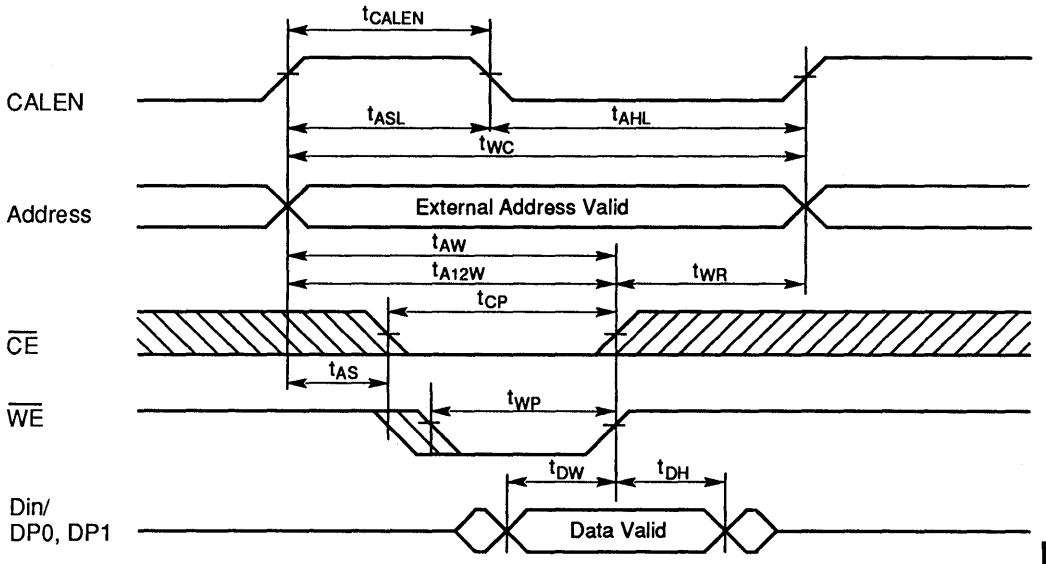
• **Read Timing Waveform (3)** ($\overline{CWE}$ = High)



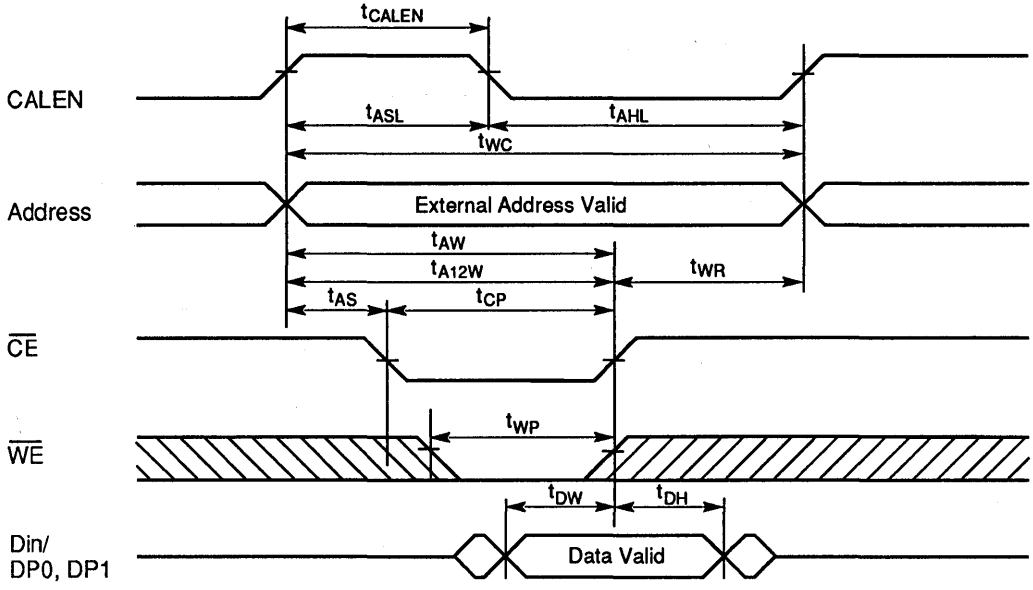
• **Write Cycle**

Parameter	Symbol	HM62168-25 HM62188-25		HM62168-35 HM62188-35		HM62168-45 HM62188-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	45	—	ns
Address Valid to End of Write	t_{AW}	18	—	25	—	40	—	ns
A_{12} Valid to End of Write	t_{A12W}	18	—	25	—	40	—	ns
Chip Select to End of Write	t_{CW}	18	—	25	—	30	—	ns
Data Valid to End of Write	t_{DW}	10	—	10	—	15	—	ns
Data Hold from End of Write	t_{DH}	0	—	0	—	0	—	ns
Write Enable Active to High-Z	t_{WHZ}	—	15	—	15	—	20	ns
Write Enable Inactive to Low-Z	t_{WLZ}	3	—	3	—	3	—	ns
Write Pulse Width	t_{WP}	18	—	25	—	30	—	ns
$\overline{CE}$ Pulse Width During Chip Enable Controlled Write	t_{CP}	18	—	25	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	2	—	ns
Address Latch Enable Pulse Width	t_{CALEN}	8	—	10	—	15	—	ns
Address Setup to Latch Low	t_{ASL}	4	—	6	—	10	—	ns
Address Hold to Latch Low	t_{AHL}	5	—	5	—	5	—	ns

• **Write Timing Waveform (1)** ($\overline{COE}$ = High, $\overline{WE}$ Controlled)



• **Write Timing Waveform (2)** ($\overline{COE}$ = High, $\overline{CE}$ Controlled)



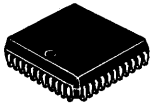
HM67C932 Series — Preliminary

8,192-Word × 9-Bit × 4-Row Static Cache RAM

■ DESCRIPTION

The Hitachi HM67C932 is a high speed 288-kbit static cache RAM organized as 4-way set associative 8k × 9 or direct mapped 32k × 9 with 4-row selector for burst mode. By using HM67C932 with high speed standard microprocessors a high performance computer system can be achieved.

The HM67C932, packaged in a 44-pin PLCC is available for high density mounting.



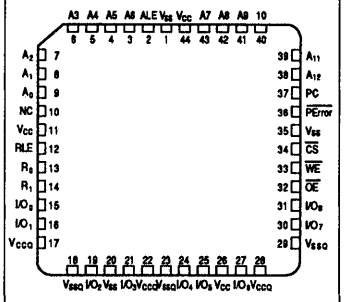
(CP-44)

■ FEATURES

- For High Speed Standard Microprocessors
- High Speed Access Capability with Lower 2-address by Selector
- Pipeline Access Capability with On Chip Address and Row Latches (Edge Trigger Type Row Latch)*
- On Chip Parity Generator and Checker
- Organization . . . . . .288-kbit (8-kw × 9 bit × 4 row)
- Drivability for Heavy Load (C_L = 100 pF) ⚠
- PLCC 44-pin
- TTL I/O

*For cache RAM with transparent row latch, request data sheet HM67B932.

■ PIN ARRANGEMENT



(Top View)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM67C932CP-20 HM67C932CP-25	20ns 25ns	44-pin PLCC

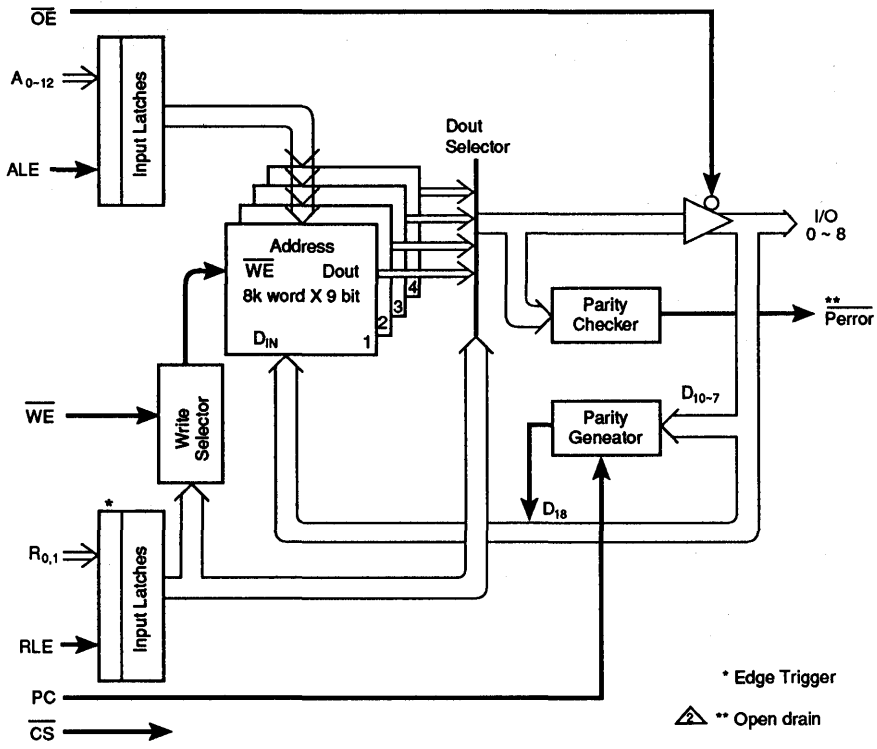
■ MAIN CHARACTERISTICS

Item		Spec.	Remarks
Access Time	Address Access Time (max.)	20/25ns	C_L = 100pF ⚠
	Row Select Access Time (max.)	10/13ns	
	$\overline{OE}$ Access Time (max.)	10/13ns	
Cycle Time (min.)		25/30ns	Clock Frequency 33 ~ 40 MHz
Power Dissipation (typ.)		0.8W	V_{CC} = 5.0V t_{CYC} = 60ns

■ PIN DESCRIPTION

Pin Name	Function
ALE	Address Latch Enable
A_0–A_{12}	Address
RLE	Row Latch Enable (Edge Trigger)
R_0–R_1	Row
I/O_0–I/O_7	Data Input/Output
I/O_8	Data Input/Output (Even Parity)
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PC	Parity Control
$\overline{PError}$	Parity Error Output (Open Drain)
V_{CC}	Power
V_{SS}	Ground
V_{CCQ}	Power (For Output Transistors)
V_{SSQ}	Ground (For Output Transistors)

■ BLOCK DIAGRAM



■ FUNCTION TABLE

• Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	PC	Mode	V_{CC} Current	I/O Pin	$\overline{PError}$ Pin	Ref. Cycle
H	X	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	High Z	
L	H	H	X	Output Disabled	I_{CC}, I_{CC1}	High Z	High Z	
L	L	H	X	Read	I_{CC}, I_{CC1}	D_{out}	High Z or L (Error)	Read Cycle No. 1, 2
L	H	L	L	Write	I_{CC}, I_{CC1}	D_{in}	High Z	Write Cycle No. 1-5
L	L	L	L	Write	I_{CC}, I_{CC1}	D_{in}	High Z	Write Cycle No. 6, 7
L	H	L	H	Write (Parity Generate)	I_{CC}, I_{CC1}	D_{in}(1)	High Z	Write Cycle No. 1
L	L	L	H	Write (Parity Generate)	I_{CC}, I_{CC1}	D_{in}(1)	High Z	

NOTE: 1. D_{I8} input is ignored and generated as parity bit from D_{I0} to D_{I7}.

• Input Latch Table

• Address Latch

ALE	Mode	Latch Output
H	Load	Address Input
L	Hold	Previous Address

• Row Latch

RLE	Mode	Latch Output
↑	Load	Row Input
H or L	Hold	Previous Row

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_T	-0.5 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range (With Bias)	$T_{stg(bias)}$	-10 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
	V_{IL}	-0.5(1)	—	0.8	V

NOTE: 1. -3.0V for pulse width ≤ 20ns.

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 to +70°C, V_{SS} = 0V)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5V, V_{IN} = V_{SS} to V_{CC}	—	—	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = V_{SS} to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	—	TBD	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%, $I_{I/O}$ = 0mA	—	—	TBD	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}	—	—	TBD	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} - 0.2V V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC} - 0.2V	—	—	TBD	mA
Output Low Voltage	V_{OL}(1)	I_{OL} = 16mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -8mA	2.4	—	—	V
		I_{OH} = -100μA	2.7	—	—	V

NOTE: 1. Including $\overline{PError}$ Output.

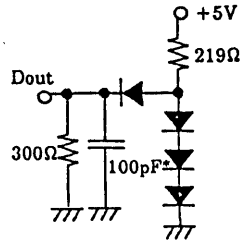
■ CAPACITANCE (T_a = 25°C, f = 1.0MHz)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	—	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF
Output Capacitance ($\overline{PError}$)	C_{out}	V_{out} = 0V	—	—	10	pF

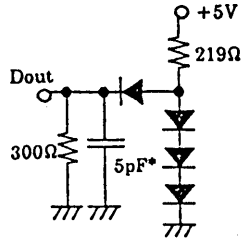
■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 to +70°C)

• AC Test Conditions

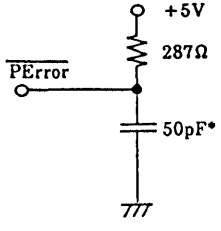
- Input Pulse Levels: 0.4V to 2.4V
- Input Timing Reference Levels: 0.8V, 2.0V
- Output Timing Reference Levels: V_{OL} = 0.8V, V_{OH} = 2.0V
- Input Rise and Fall Times: 4ns
- Output Load: See Figure



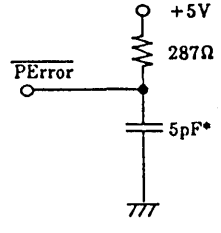
Output Load A



Output Load B
(for t_{CHZ}, t_{WHZ}, t_{OHZ}, t_{CLZ}, t_{OW} & t_{OLZ})



Output Load C



Output Load D
(for t_{APH}, t_{LEPH}, t_{RPH}, t_{CPH} & t_{OPH})

*Including scope and jig.

• Read Cycle

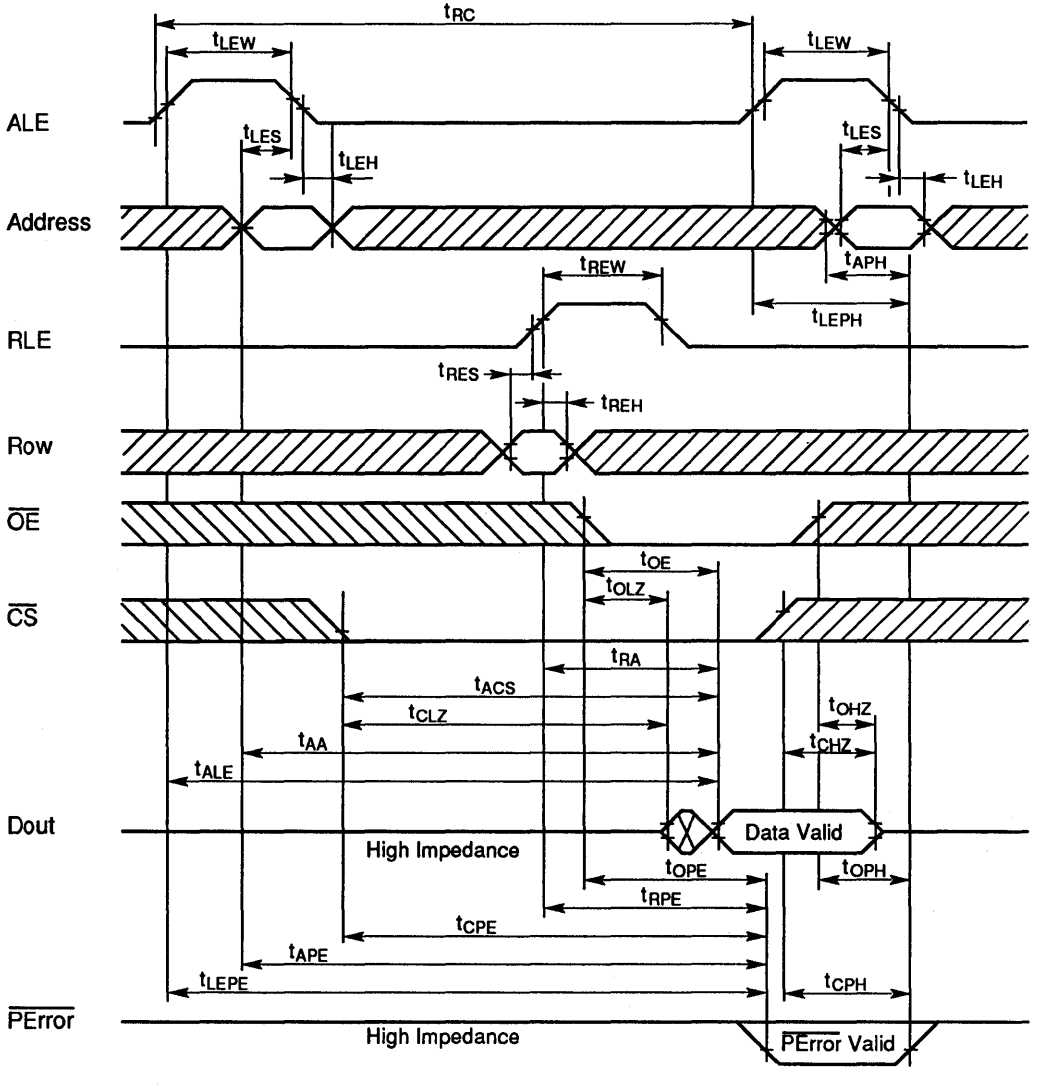
Item	Symbol	HM67C932-20 ⚠		HM67C932-25		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	30	—	ns
Row Selector Read Cycle Time	t_{RCR}	15	—	⚠18	—	ns
Address Latch Enable Pulse Width	t_{LEW}	5	—	7	—	ns
Address Latch Enable Setup Time	t_{LES}	3	—	5	—	ns
Address Latch Enable Hold Time	t_{LEH}	3	—	3	—	ns
Row Latch Enable Pulse Width	t_{REW}	5	—	7	—	ns
Row Latch Enable Setup Time	t_{RES}	3	—	5	—	ns
Row Latch Enable Hold Time	t_{REH}	3	—	3	—	ns
Address Access Time	t_{AA}	—	20	—	25	ns
Output Hold from Address Change	t_{OH}	5	—	5	0	—
Address Latch Enable Access Time	t_{ALE}	—	20	—	25	ns
Output Hold from End of Address Latch Hold	t_{OLEH}	5	—	5	—	ns
Row Selector Access Time	t_{RA}	—	10	—	13	ns
Output Hold from Row Selector Change	t_{ORH}	0	—	0	—	ns
Chip Select Access Time	t_{ACS}	—	20	—	25	ns
Chip Selection to Output in Low Z	$t_{CLZ}^{(1),(3)}$	0	—	0	—	ns
Chip Deselection to Output in High Z	$t_{CHZ}^{(1),(3)}$	0	8	0	10	ns
Output Enable to Output Valid	t_{OE}	0	10	0	13	ns
Output Enable to Output in Low Z	$t_{OLZ}^{(1),(3)}$	0	—	0	—	ns
Output Disable to Output in High Z	$t_{OHZ}^{(1),(3)}$	0	8	0	10	ns
Address to Parity Error Valid	t_{APE}	—	25	—	30	ns
Address Change to Parity Error in High Z	$t_{APH}^{(2),(3)}$	5	—	5	—	ns
Address Latch Enable to Parity Error Valid	t_{LEPE}	—	25	—	30	ns
End of Address Latch Hold to Parity Error in High Z	$t_{LEPH}^{(2),(3)}$	5	—	5	—	ns
Row Selector to Parity Error Valid	t_{RPE}	—	15	—	18	ns
Row Selector Change to Parity Error in High Z	$t_{RPH}^{(2),(3)}$	3	—	⚠3	—	ns
Chip Selection to Parity Error Valid	t_{CPE}	—	25	—	30	ns
Chip Deselection to Parity Error in High Z	$t_{CPH}^{(2),(3)}$	0	—	0	—	ns
Output Enable to Parity Error Valid	t_{OPE}	—	15	—	18	ns
Output Disable to Parity Error in High Z	$t_{OPH}^{(2),(3)}$	0	—	0	—	ns

NOTES: 1. Transition is measured ± 200mV from steady state voltage with Load B.

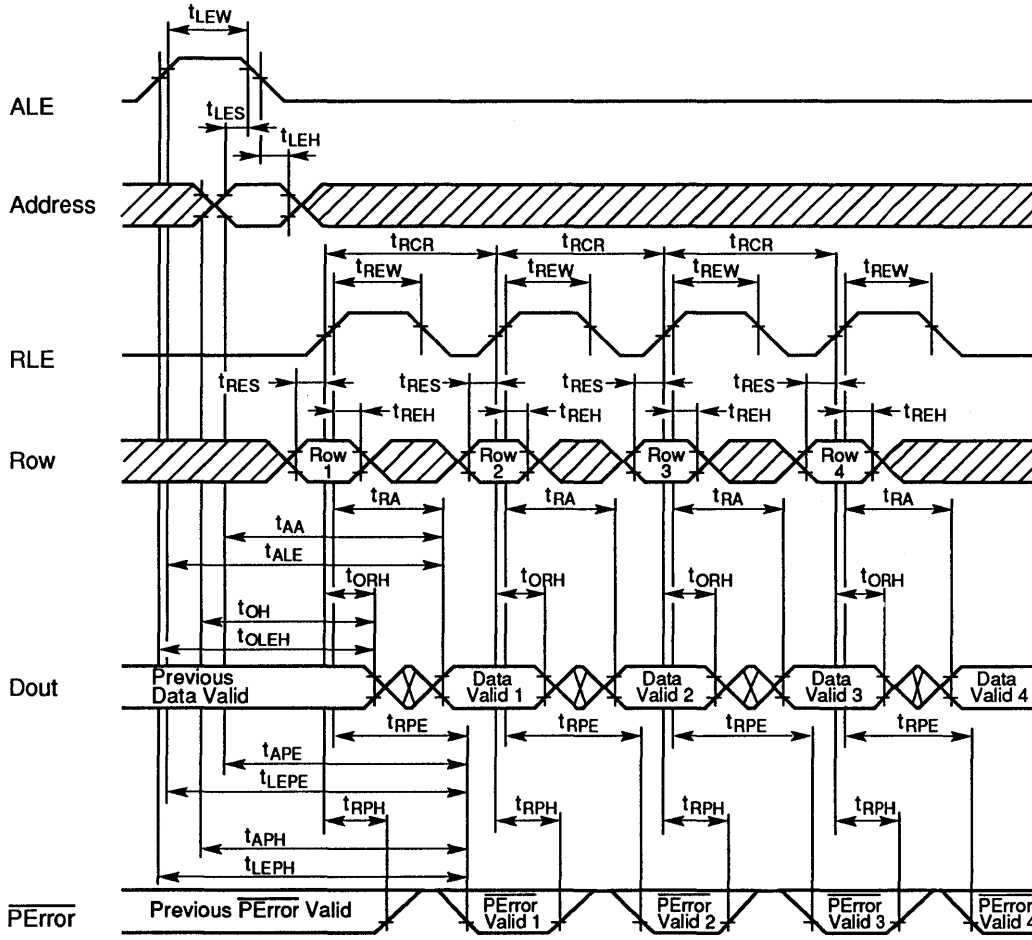
2. Transition is measured ± 200mV from steady state voltage with Load D.

3. This parameter is sampled and not 100% tested.

• **Timing Waveform of Read Cycle No. 1** (Cache Read Cycle) (1)



• **Timing Waveform of Read Cycle No. 2** (Serial Read Cycle With Row Selector) (1), (2)



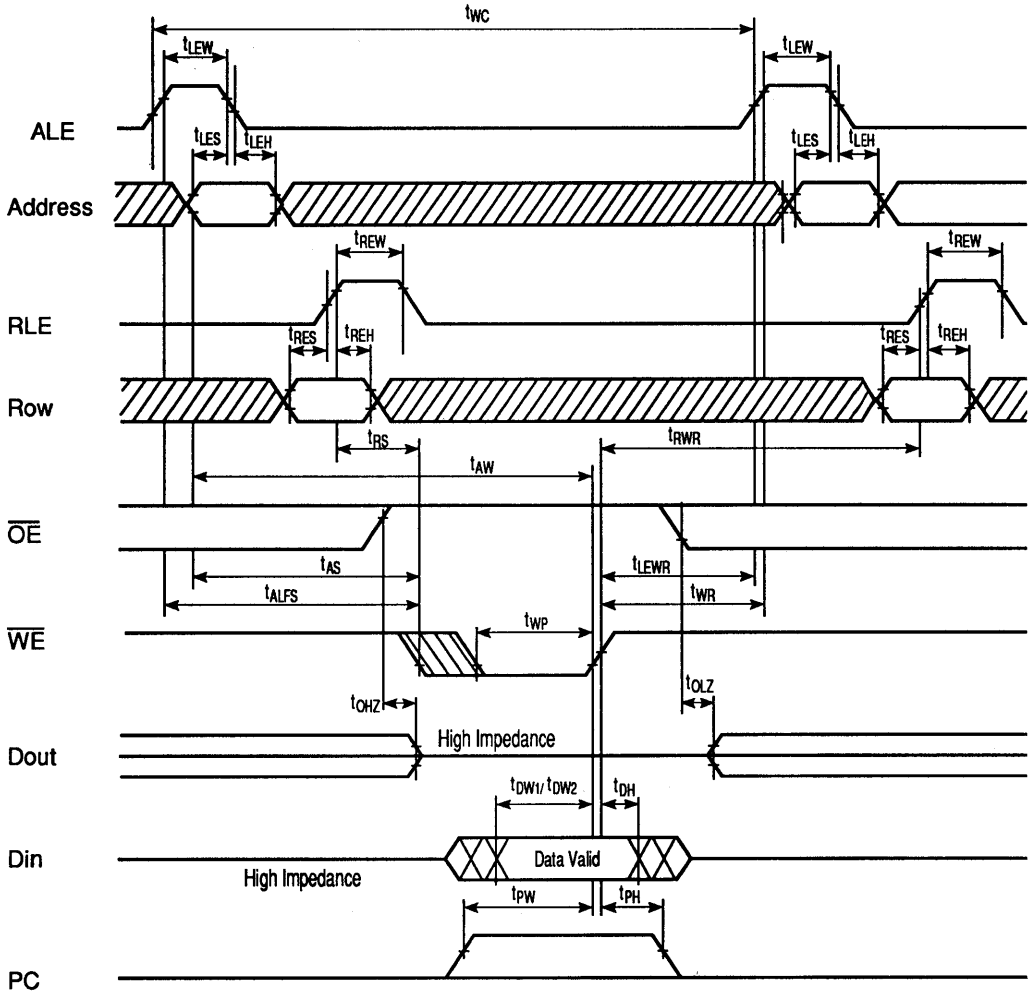
NOTES: 1. $\overline{WE}$ = V_{IH}, PC: Do not care
2. $\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IL}

• **Write Cycle**

Item	Symbol	HM67C932-20		HM67C932-25		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	30	—	ns
Chip Selection to End of Write	t_{CW}	15	—	20	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Latch Enable Setup Time	t_{ALES}	0	—	0	—	ns
Row Selector Setup Time	t_{RS}	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	15	—	20	—	ns
Write Pulse Width	t_{WP}	12	—	15	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Write Recovery to End of Address Latch Hold	t_{LEWR}	3	—	3	—	ns
Write Recovery to Row Selector Change	t_{RWR}	5	—	5	—	ns
Write to Output in High Z	t_{WHZ}(1), (2)	0	8	0	10	ns
Data Valid to End of Write	t_{DW}	8	—	10	—	ns
Data Valid to End of Write (Parity Generate Mode)	t_{DW2}	12	—	15	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Output Active from End of Write	t_{OW}(1), (2)	0	—	0	—	ns
Parity Control Setup Time	t_{PW}	12	—	15	—	ns
Parity Control Hold Time	t_{PH}	0	—	0	—	ns

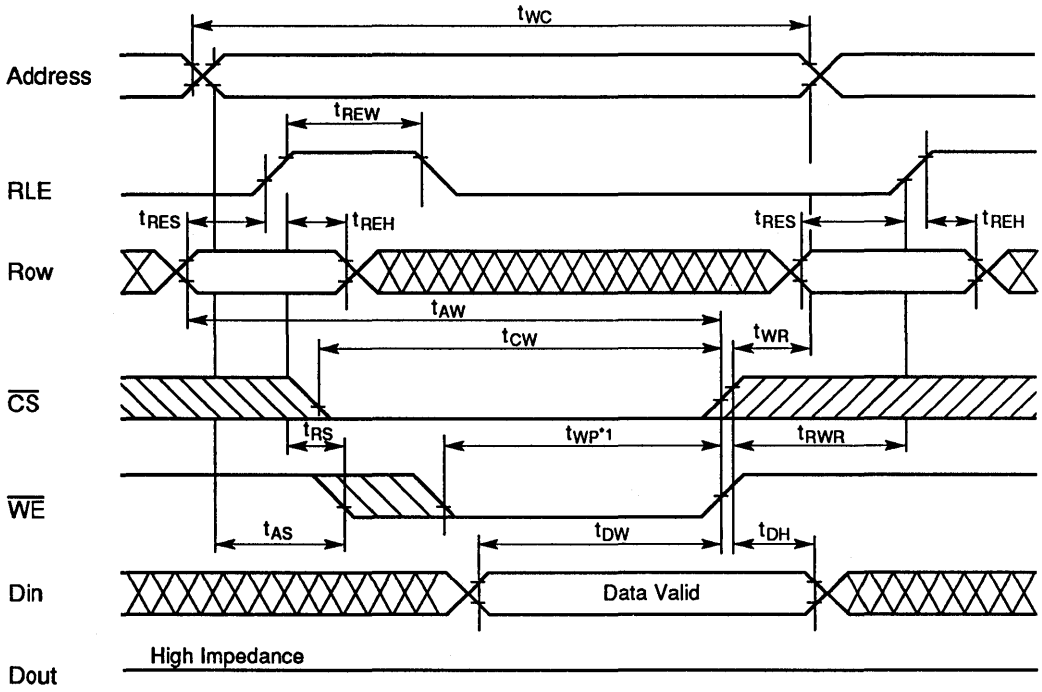
NOTES: 1. Transition is measured ±200mV from steady state voltage with Load B.
2. This parameter is sampled and not 100% tested.

• **Timing Waveform of Write Cycle No. 1** (Cache Write Cycle) (1), (2)

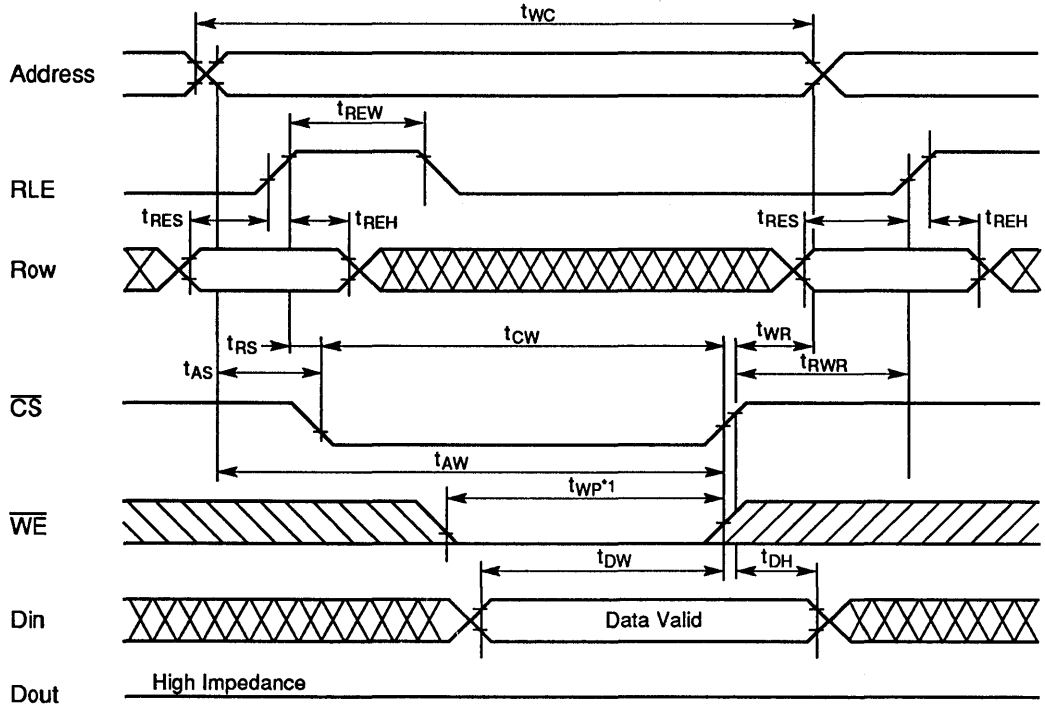


NOTES: 1. $\overline{CS}$ = V_{IL}, $\overline{PError}$: Do not care.
2. D_{I8} input is not cared with parity generate mode. Parity of written data is not checked.

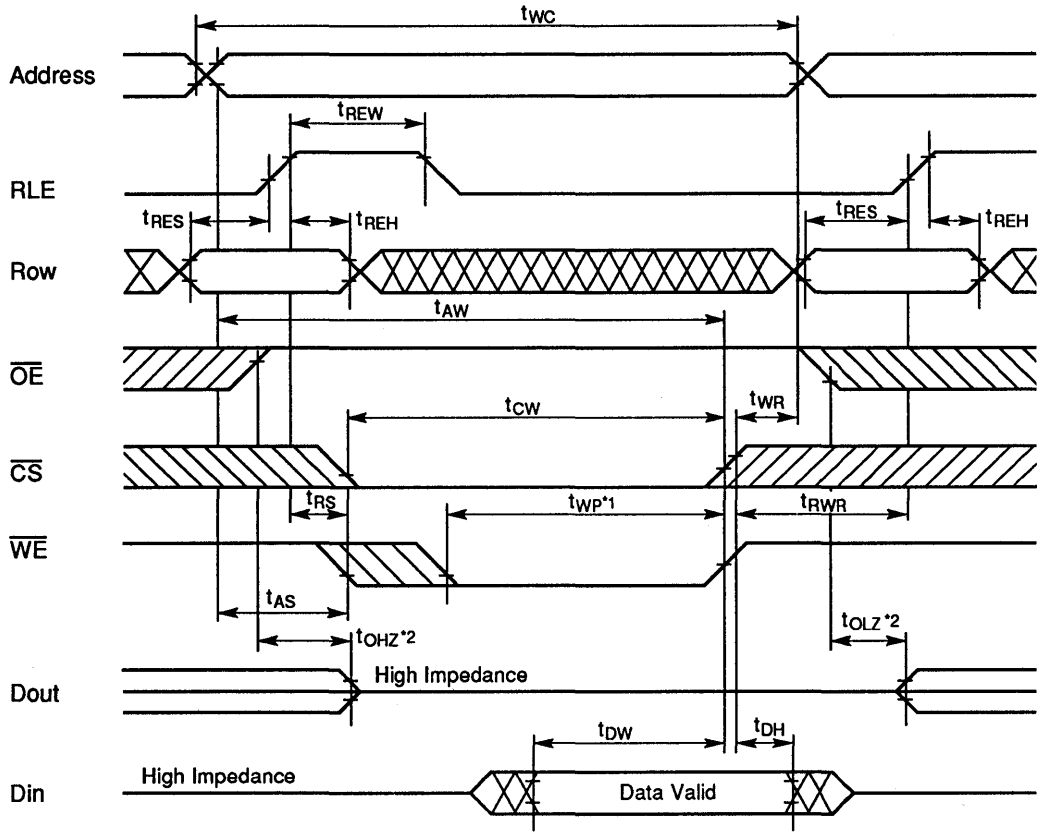
• **Timing Waveform of Write Cycle No. 2** ($\overline{OE}$ = H, $\overline{WE}$ Controlled) (7)



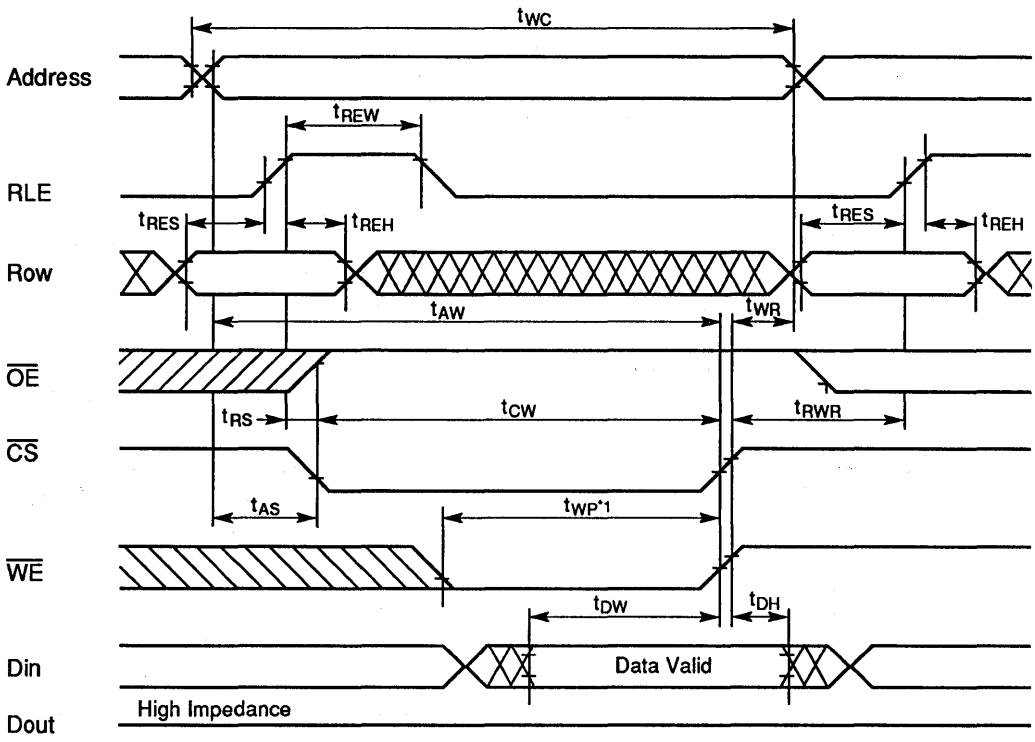
• **Timing Waveform of Write Cycle No. 3** ($\overline{OE}$ = H, $\overline{CS}$ Controlled) (7)



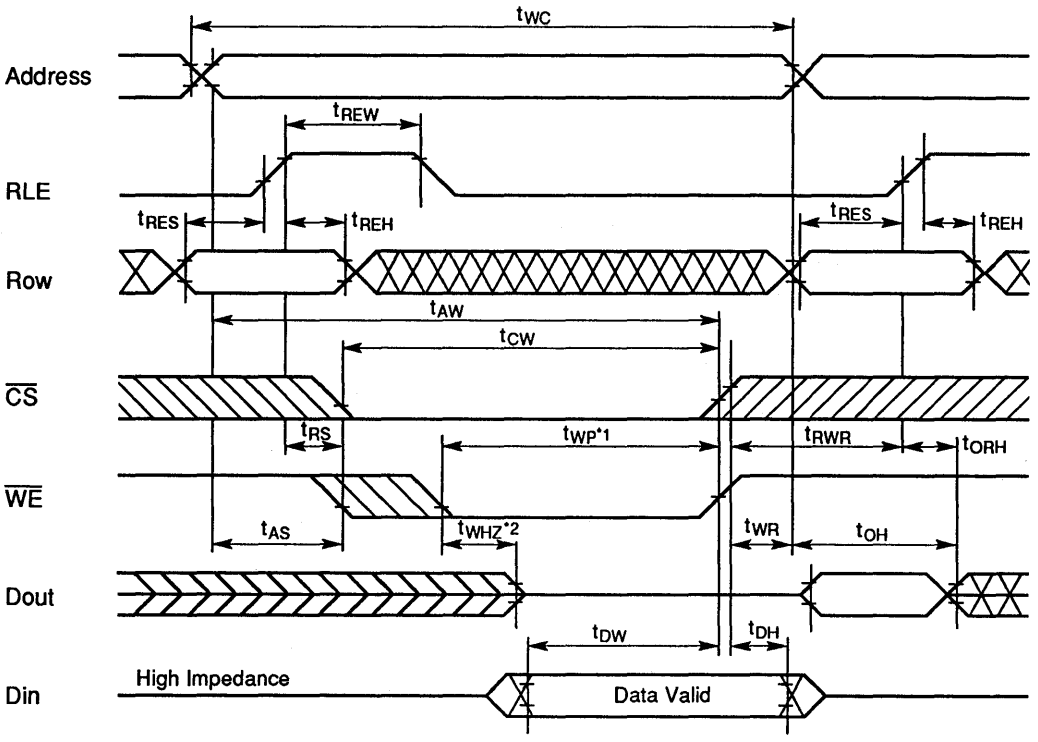
• **Timing Waveform of Write Cycle No. 4** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled) (7)



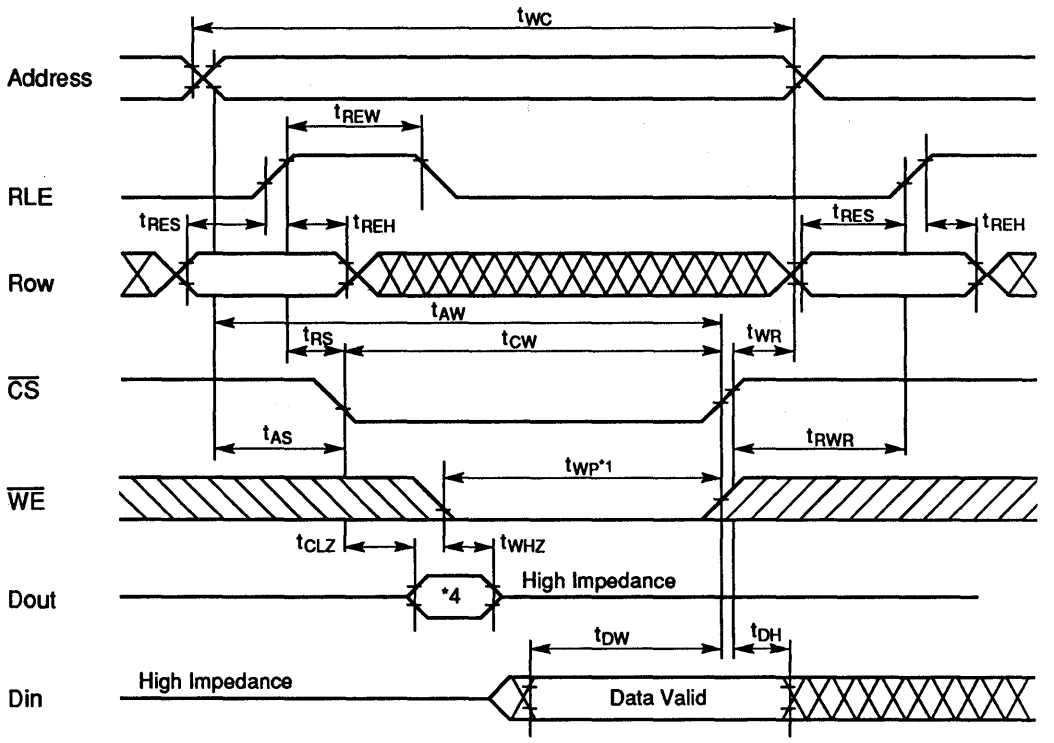
• **Timing Waveform of Write Cycle No. 5** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled) (7)



• **Timing Waveform of Write Cycle No. 6** ($\overline{OE}$ = L, $\overline{WE}$ Controlled) (7)



• Timing Waveform of Write Cycle No. 7 ($\overline{OE}$ = L, $\overline{CS}$ Controlled) (7)



NOTES:

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remains in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.
6. If $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, output remains in high impedance state.
7. ALE = V_{IH}, PC = V_{IL}, $\overline{PError}$: Do not care.

HB66B1616A-25/35

16,384-Word × 16-Bit High Speed Static RAM Module

■ DESCRIPTION

The HB66B1616A is a high speed 16K × 16 Static RAM module, mounted 4 pieces of 64K bit SRAM (HM6289JP) sealed in SOJ package. An outline of the HB66B1616A is 36-pin dual in-line package. Therefore, the HB66B1616A makes high density mounting possible without surface mount technology. The HB66B1616A provides common data inputs and outputs. Its module board has decoupling capacitors to reduce noise.

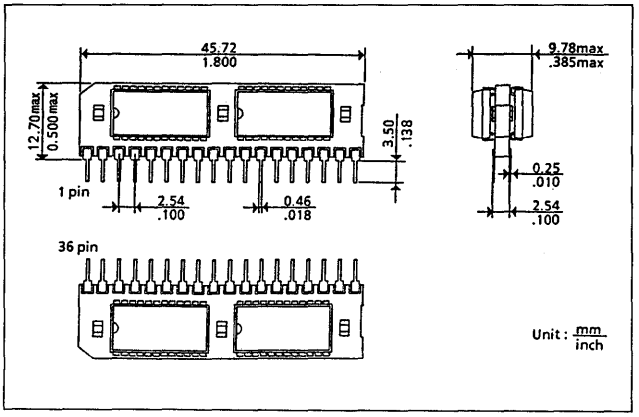
■ FEATURES

- Single 5V (± 5%) Supply
- High Speed
  - Access Time . . . . . .25/35ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .1200mW typ.
  - Standby Mode . . . . . .300mW typ. (TTL level)
  - 0.4mW typ. (CMOS level)
- Equal Access and Cycle Time
- Completely Static RAM
  - No Clock or Timing Strobe Required
- Directly TTL Compatible: All Inputs and Outputs

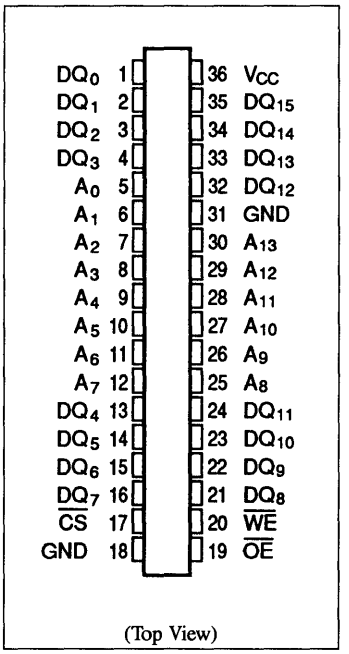
■ ORDERING INFORMATION

Part No.	Access	Package
HB66B1616A-25	25ns	36-pin dual in-line leaded type
HB66B1616A-35	35ns	

■ PHYSICAL OUTLINE



■ PIN ASSIGNMENT

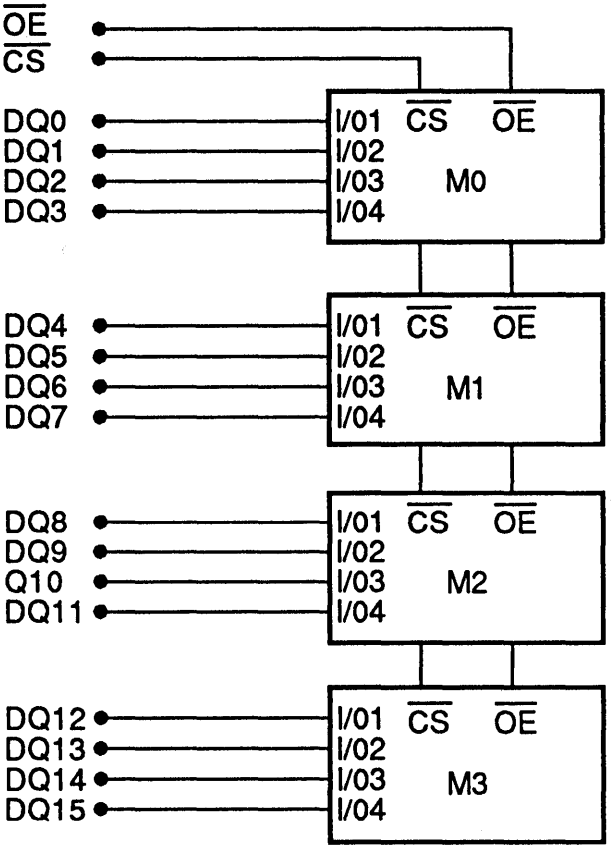


(Top View)

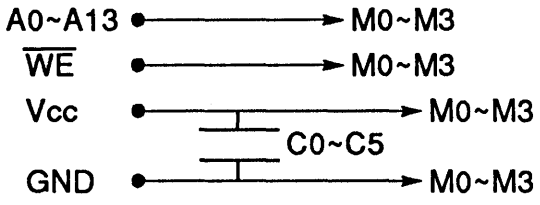
■ PIN DESCRIPTION

Pin Name	Function
A_0 ~ A_{13}	Address Input
DQ_0 ~ DQ_{15}	Data-in, Data-out
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power Supply (+5V)
GND	Ground

■ BLOCK DIAGRAM



* M0~M3 : HM6289JP



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}	-0.5(1) to +7.0	V
Power Dissipation	P_T	4.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +85	°C

NOTE: 1. V_{in} min. = -2.0V for pulse width ≤ 10ns.

■ TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	L	H	Read	I_{CC}	D_{out}	Read Cycle (1-3)
L	H	L	Write	I_{CC}	D_{in}	Write Cycle (1) (2)
L	L	L	Write	I_{CC}	D_{in}	Write Cycle (3-6)

NOTE: X means don't care.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	-0.5(1)	—	0.8	V

NOTE: 1. V_{IL} min. = -2.0V for pulse width ≤ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min.	Typ.(1)	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}	-10	—	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	-2	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA Min. Cycle	—	240	480	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH} Min. Cycle	—	60	120	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}$ = ≥ V_{CC} -0.2V 0V ≤ V_{in} ≤ 0.2V or V_{in} ≥ V_{CC} -0.2V	—	0.08	8	mA
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

NOTE: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)(1)

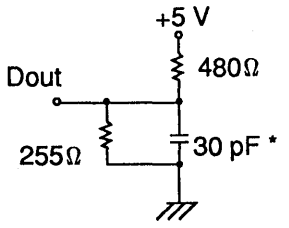
Parameter	Symbol	Test Conditions	Min.	Max.	Unit
Input Capacitance (Address, $\overline{CS}$, $\overline{OE}$, $\overline{WE}$)	C_{in}	V_{in} = 0V	—	35	pF
Input/Output Capacitance (DQ)	$C_{I/O}$	$V_{I/O}$ = 0V	—	15	pF

NOTE: 1. This parameter is sampled and not 100% tested.

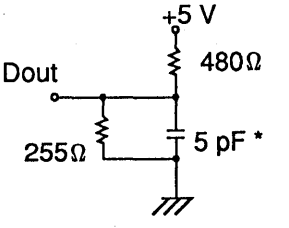
■ AC CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 5%, unless otherwise noted.)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input and Output Timing Reference Levels: 1.5V
- Input Rise and Fall Times: 5ns
- Output Load: See Figures



Output Load A



Output Load B
(for t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} & t_{OW})

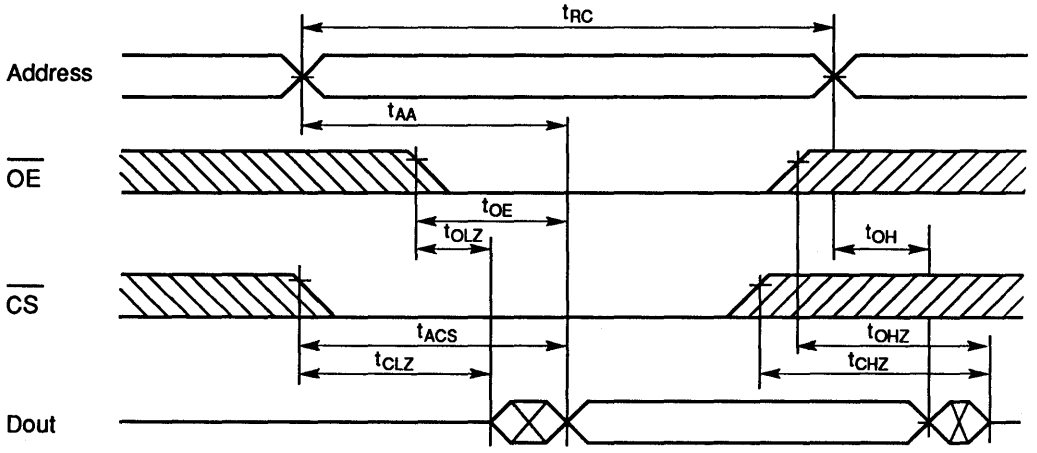
*Including scope and jig capacitance.

• Read Cycle

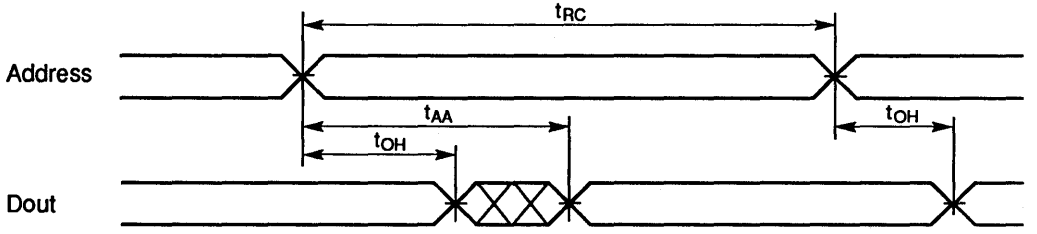
Parameter	Symbol	HB66B1616A-25		HB66B1616A-35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Chip Selection to Output in Low-Z	t_{CLZ}(1)	5	—	5	—	ns
Output Enable to Output Valid	t_{OE}	—	12	—	15	ns
Output Enable to Output in Low-Z	t_{OLZ}(1)	0	—	0	—	ns
Chip Deselection to Output in High-Z	t_{CHZ}(1)	0	12	0	20	ns
Chip Disable to Output in High-Z	t_{OHZ}(1)	0	10	0	10	ns
Output Hold from Address Change	t_{OH}	3	—	5	—	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	25	—	30	ns

NOTE: 1. Output transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

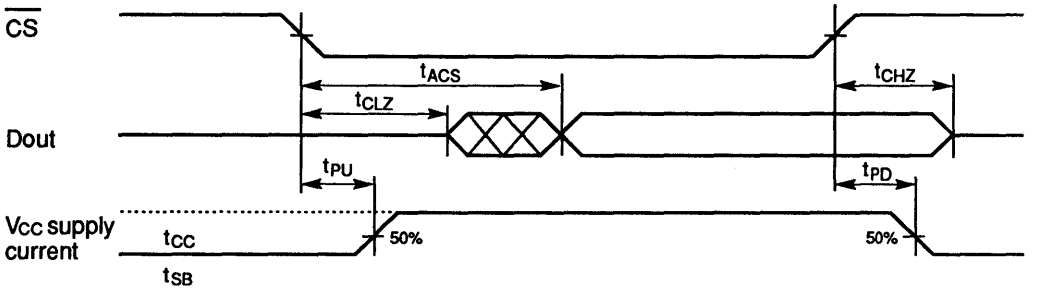
• **Read Timing Waveform (1)** (1)



• **Read Timing Waveform (2)** (1) (2) (4)



• **Read Timing Waveform (3)** (1) (3) (4)



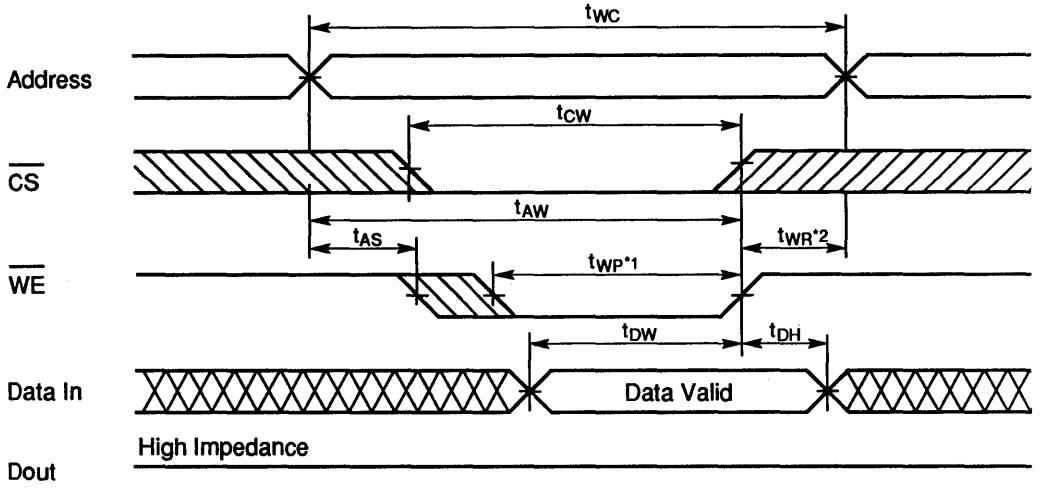
NOTES: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.

• Write Cycle

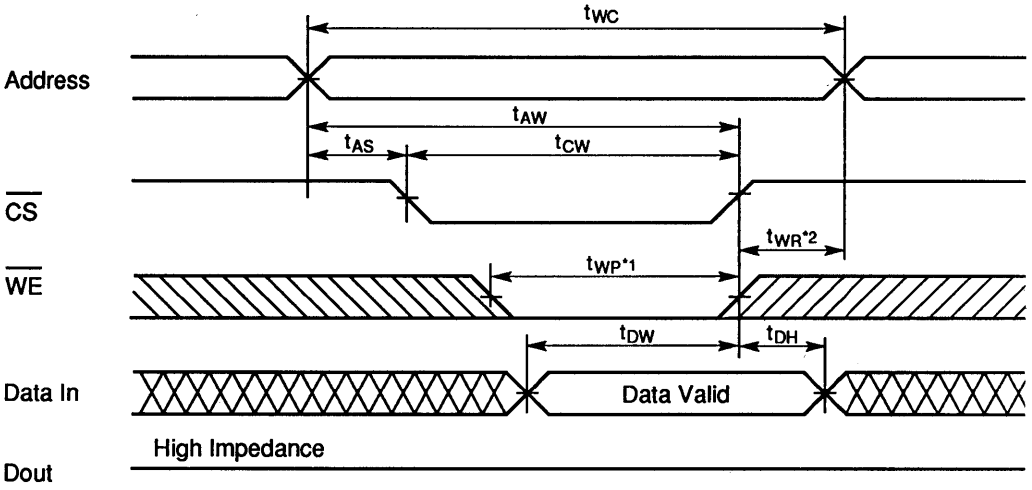
Parameter	Symbol	HB66B1616A-25		HB66B1616A-35		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Output Disable to Output in High-Z	t_{OHZ}(1)	0	10	0	10	ns
Write to Output in High-Z	t_{WHZ}(1)	0	8	0	10	ns
Data to Write Time Overlap	t_{DW}	12	—	20	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns
Output Active from End of Write	t_{OW}(1)	5	—	5	—	ns

NOTE: 1. Output transition is measured ±200mV from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

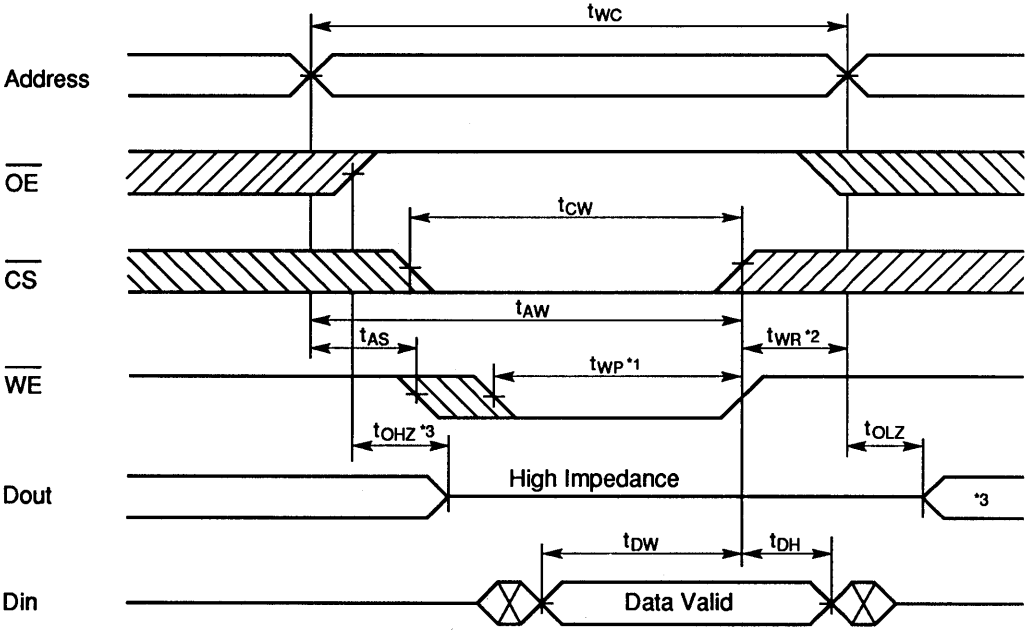
• Write Timing Waveform (1) ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



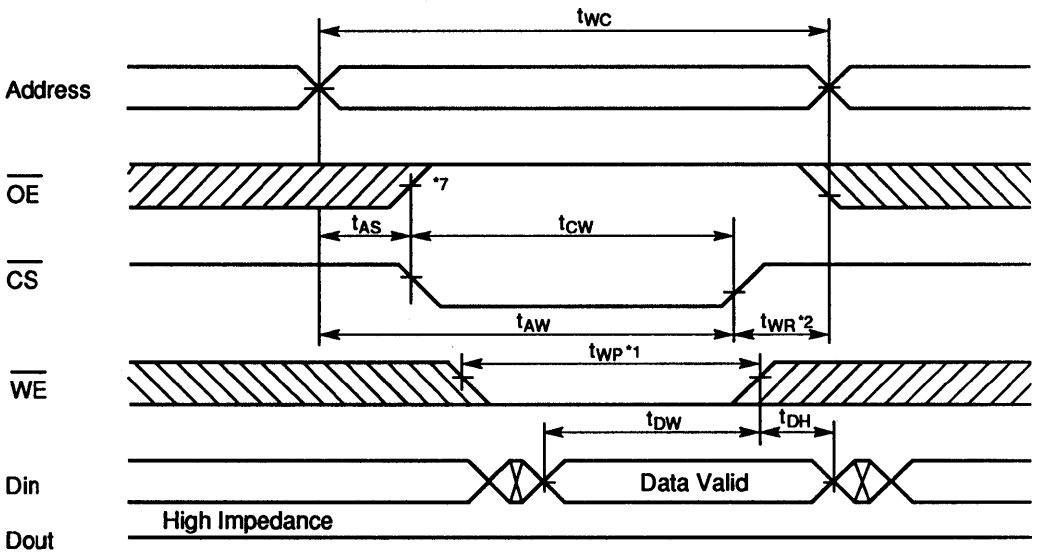
• **Write Timing Waveform (2)** ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



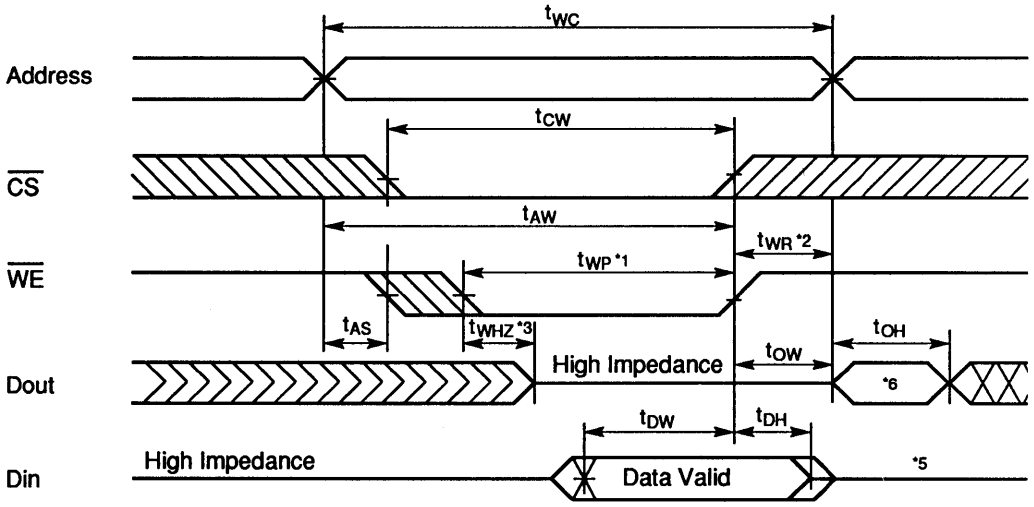
• **Write Timing Waveform (3)** ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



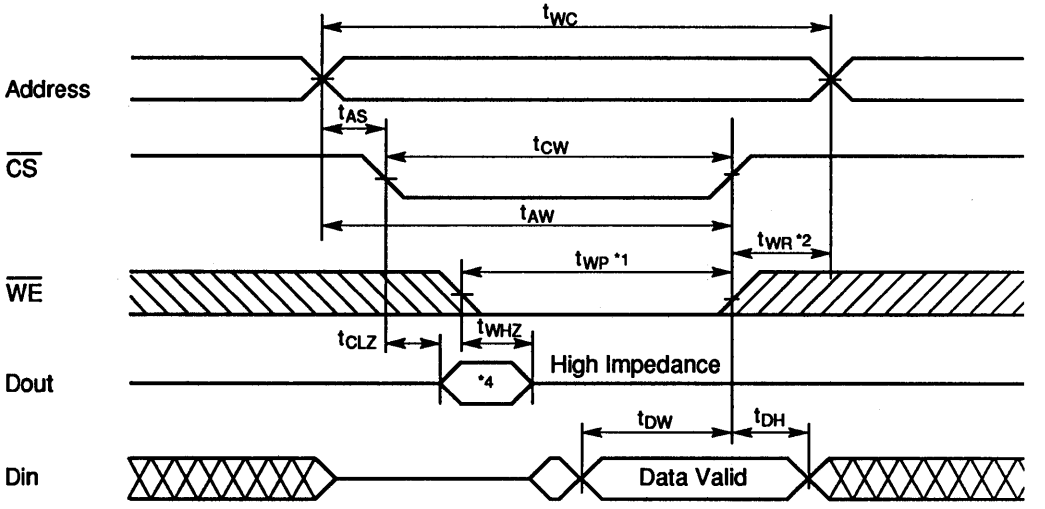
• **Write Timing Waveform (4)** ($\overline{OE}$ = Clocked, $\overline{CS}$ Controlled)



• **Write Timing Waveform (5)** ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



• **Write Timing Waveform (6)** ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



NOTES:

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (t_{WP}).
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.
5. If $\overline{CS}$ is low during this period, I/O pins are in the output state after t_{OW}. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. D_{out} is the same phase of write data of this write cycle, if t_{WR} is long enough.
7. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{OE}$ high transition or after the $\overline{OE}$ transition, the output buffers remain in a high impedance state.

HB66A2568A-25/35

262,144-Word × 8-Bit High Speed Static RAM Module

■ DESCRIPTION

The HB66A2568A is a high speed 256K × 8 Static RAM module, mounted 8 pieces of 256K bit SRAM (HM6207HJP) sealed in SOJ package. An outline of the HB66A2568A is 60-pin zigzag in-line package. Therefore, the HB66A2568A makes high density mounting possible without surface mount technology. The HB66A2568A provides separate data inputs and output. Its module board has decoupling capacitors to reduce noise.

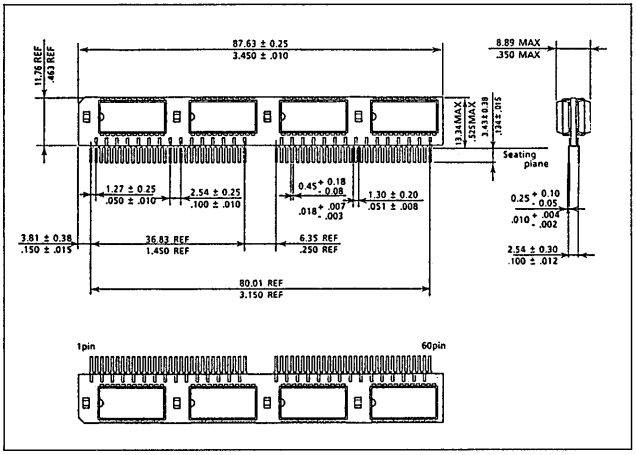
■ FEATURES

- Single 5V (± 10%) Supply
- High Speed
  - Access Time . . . . . .25/35ns (max.)
- Low Power Dissipation
  - Active Mode . . . . . .2400mW typ.
  - Standby Mode . . . . . .800mW typ. (TTL level)
    0.8mW typ. (CMOS level)
- Equal Access and Cycle Time
- Completely Static RAM
  - No Clock or Timing Strobe Required
- Directly TTL Compatible: All Inputs and Outputs

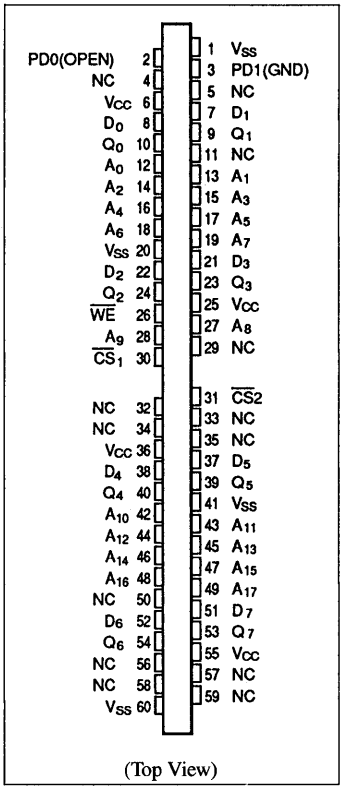
■ ORDERING INFORMATION

Part No.	Access	Package
HB66A2568A-25 HB66A2568A-35	25ns 35ns	60-pin zigzag in-line leaded type

■ PHYSICAL OUTLINE



■ PIN ASSIGNMENT

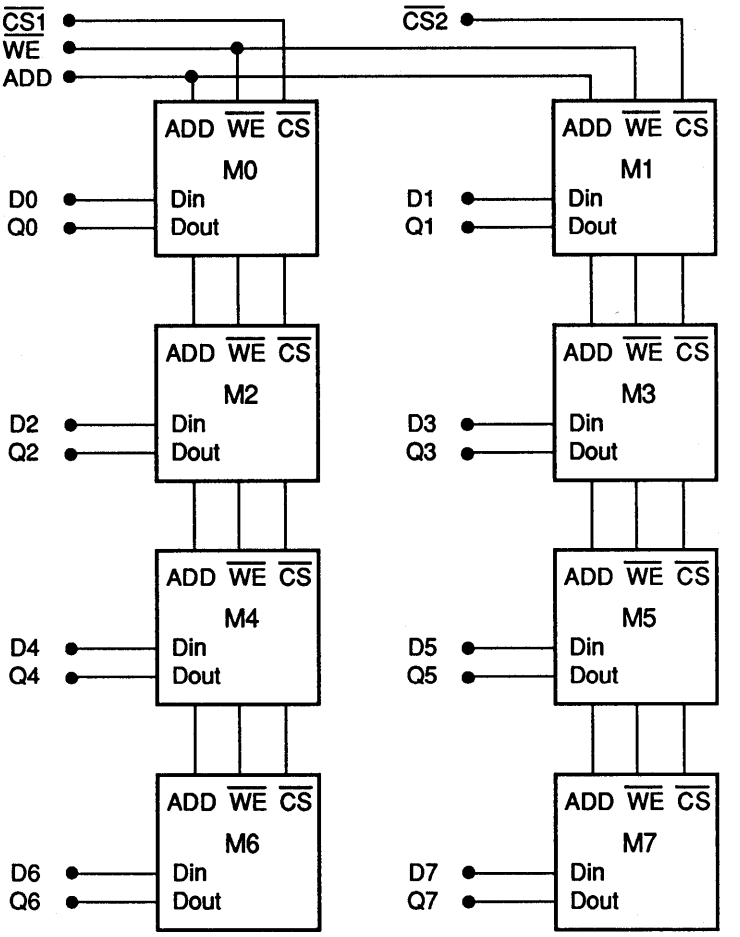


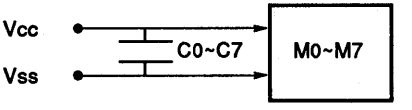
(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A_0 ~ A_{17}	Address Input
D_0 ~ D_7	Data-in
Q_0 ~ Q_7	Data-out
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	Non-connection

■ BLOCK DIAGRAM





C=0.22μF

* M0~M7 : HM6207HJP

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS}	V_{in}	-0.5(1) to +7.0	V
Power Dissipation	P_T	8.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +85	°C

NOTE: 1. V_{in} min. = -2.5V for pulse width ≤ 10ns.

■ TRUTH TABLE

$\overline{CS}_1$, $\overline{CS}_2$	$\overline{WE}$	Mode	V_{CC} Current	D_{out} Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

NOTE: X means don't care.

■ ELECTRICAL CHARACTERISTICS

• Recommended DC Operating Conditions (T_a = 0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High (Logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (Logic 0) Voltage	V_{IL}	-0.5(1)	—	0.8	V

NOTE: 1. V_{IL} min. = -2.0V for pulse width ≤ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V)

Parameter	Symbol	Test Condition	Min.	Typ.(1)	Max.	Unit
Input Leakage Current	I_{LI}	V_{CC} = Max., V_{in} = V_{SS} to V_{CC}	-10	—	10	μA
Output Leakage Current	I_{LO}	$\overline{CS}_1$, $\overline{CS}_2$ = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}	-10	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}_1$, $\overline{CS}_2$ = V_{IL}, $I_{I/O}$ = 0mA Min. Cycle, Duty = 100%	—	480	960	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}_1$, $\overline{CS}_2$ = V_{IH} Min. Cycle	—	160	320	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS}_1$, $\overline{CS}_2$ = ≥ V_{CC} -0.2V 0V ≤ V_{in} ≤ 0.2V or V_{in} ≥ V_{CC} -0.2V	—	0.16	16	mA
Output High Voltage	V_{OH}	I_{OH} = -4mA	2.4	—	—	V
Output Low Voltage	V_{OL}	I_{OL} = 8mA	—	—	0.4	V

NOTE: 1. Typical limits are at V_{CC} = 5.0V, T_a = +25°C and specified loading.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)(1)

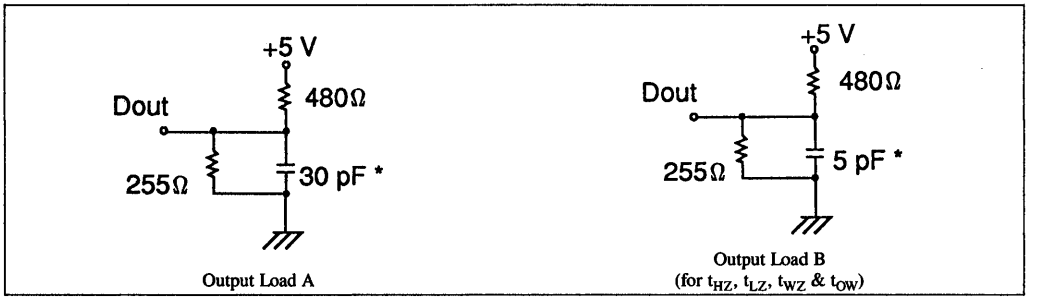
Parameter	Symbol	Test Conditions	Min.	Max.	Unit
Input Capacitance (Address, $\overline{WE}$)	C_{I1}	V_{in} = 0V	—	70	pF
Input Capacitance ($\overline{CS}$)	C_{I2}	V_{in} = 0V	—	45	pF
Input Capacitance (Data in)	C_{I3}	V_{in} = 0V	—	12	pF
Output Capacitance (Data out)	C_O	V_{out} = 0V	—	16	pF

NOTE: 1. This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0°C to 70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

• Test Conditions

- Input Pulse Levels: V_{SS} to 3.0V
- Input Rise and Fall Times: 5ns
- Input and Output Timing Reference Levels: 1.5V
- Output Load: See Figures



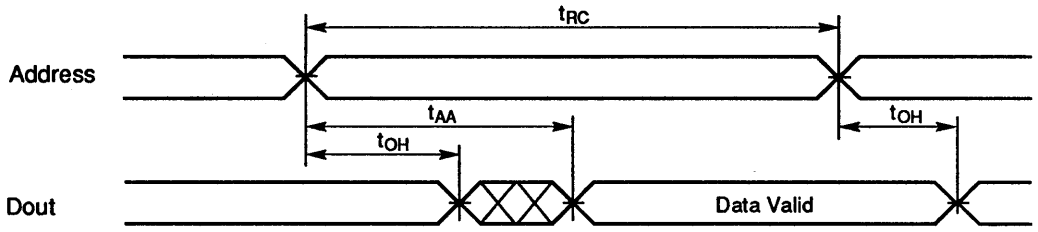
*Including scope and jig capacitance.

• Read Cycle

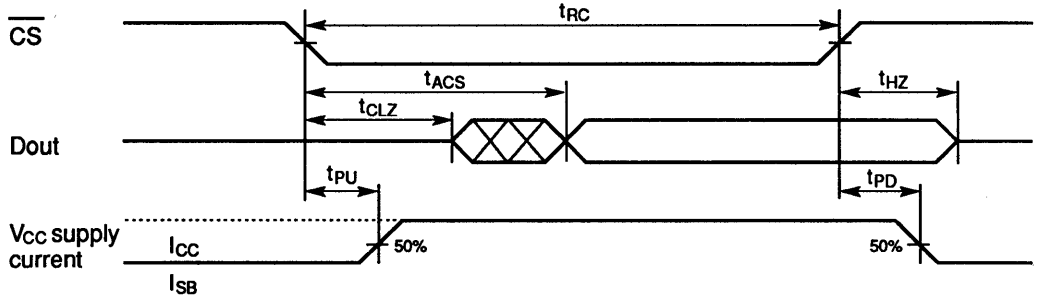
Parameter	Symbol	HB66A2568A-25		HB66A2568A-35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}(1)	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}(1)	0	12	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	15	—	25	ns

NOTE: 1. Transition is measured ±200mV from steady state voltage with Load (B)
This parameter is sampled and not 100% tested.

• **Timing Waveform of Read Cycle (1)** (1) (2)



• **Timing Waveform of Read Cycle (2)** (1) (3)



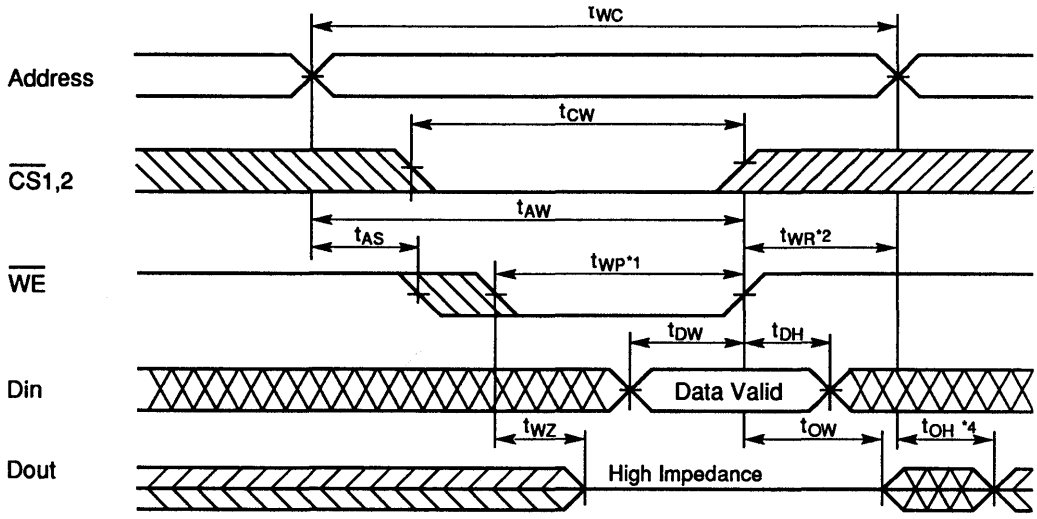
NOTES: 1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

• Write Cycle

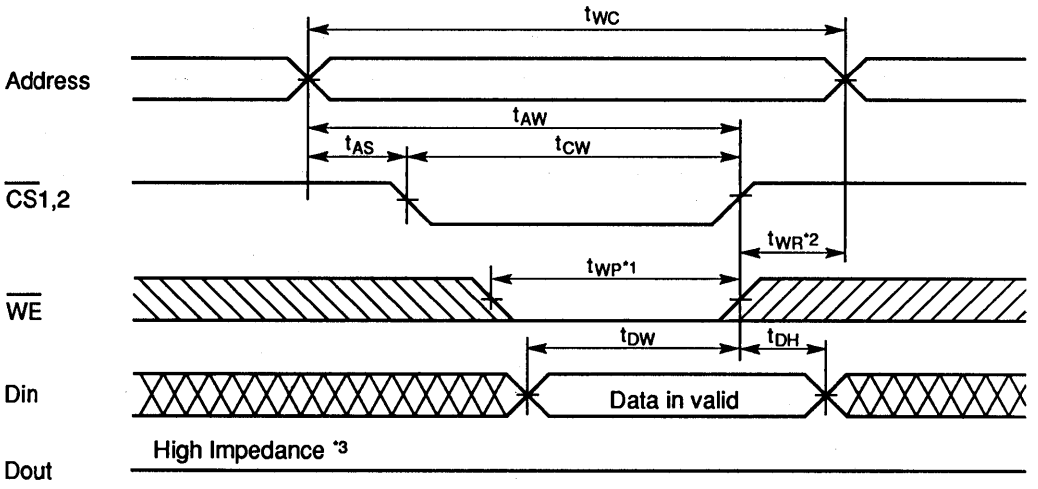
Parameter	Symbol	HB66A2568A-25		HB66A2568A-35		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	ns
Write Recovery Time	t_{WR}	3	—	3	—	ns
Data Valid to End of Write	t_{DW}	15	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enabled to Output in High-Z	t_{WZ}(1)	0	8	0	10	ns
Output Active from End of Write	t_{OW}(2)	0	—	0	—	ns

NOTE: 1. Transition is measured ±200mV from high impedance voltage with Load (B).
This parameter is sampled and not 100% tested.

• **Timing Waveform of Write Cycle (1)** ($\overline{WE}$ Controlled)



• **Timing Waveform of Write Cycle (2)** ($\overline{CS}$ Controlled)



NOTES: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.

2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

3. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the output buffers remain in a high impedance state.

4. D_{out} is the same phase of write data of this write cycle, if t_{WR} is long enough.

HM644332

2K Entry TAG Memory for Cache Sub System

The HM644332 TAGM is a 2048-entry tag memory fabricated with CMOS technology. It supports compact cache systems with 2-way or 4-way set associativity and a high level of performance for 32-bit microprocessor systems, when used together with fast static RAMs as data RAMs.

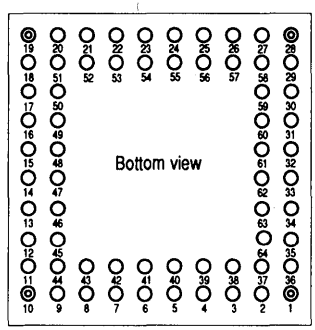
Features

- Programmable organization: 512-entry × 4-way or 1024-entry × 2-way
- Memory organization: 512 words × 98 bits
  98 bits = (20 tag bits + 1 parity bit + 2 validity bits) × 4 ways + 6 LRU bits
- Fast access time: 25/30 ns max from address inputs, 18 ns max from tag data inputs
- Single + 5 V supply
- TTL-compatible inputs and outputs
- LRU (least recently used) replacement algorithm
- Purge functions (all purge and partial purge)
- Internal parity generator/checker
- 64-pin pin-grid-array

Ordering Information

	Access Time		
Part No.	**From Address**	**From Tag Data**	**Package**
HM644332G-25	25 ns	18 ns	64-pin PGA
HM644332G-30	30 ns	18 ns	

Pin Arrangement

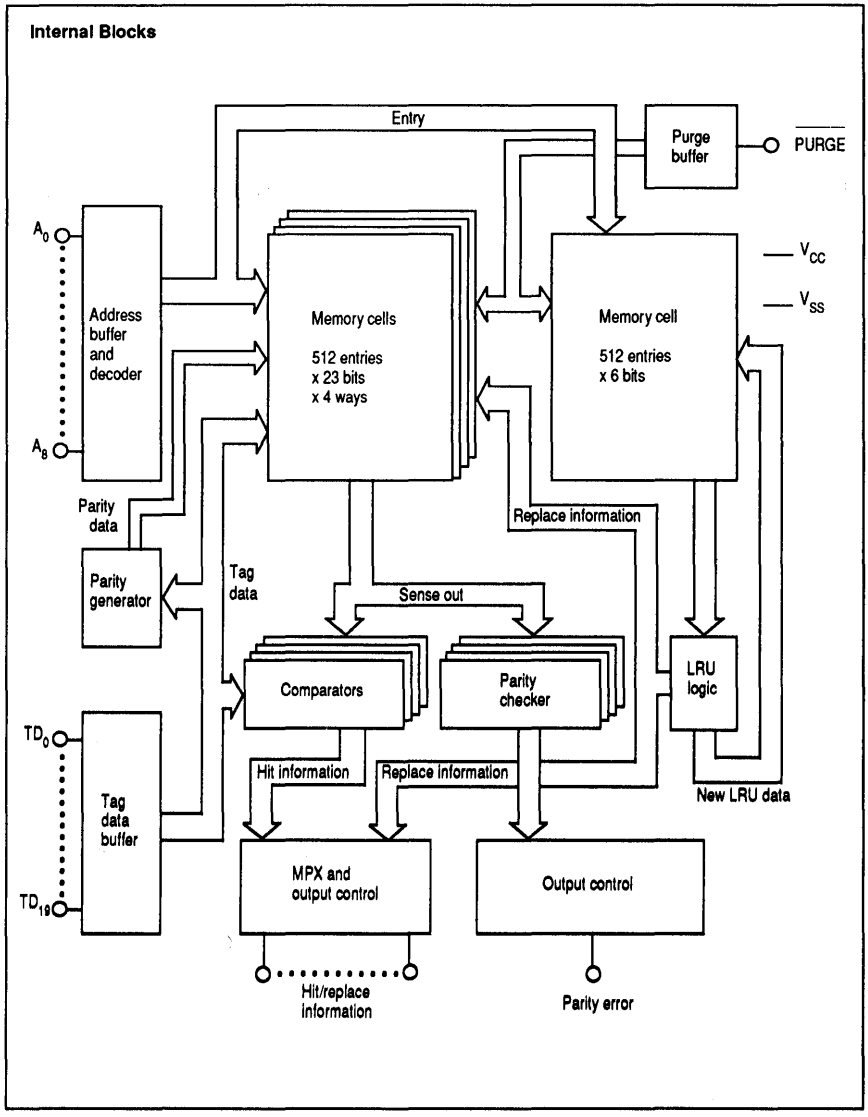


Pin No.	Function	Pin No.	Function	Pin No.	Function
1	N.C.	23	A_4	45	TD_6
2	$\overline{MHIT}$	24	A_5	46	TD_9
3	HIT_0/REP_0	25	A_7	47	V_{CC}
4	HIT_2/REP_2	26	A_9	48	TD_{13}
5	HIT_3/REP_3	27	N.C.	49	TD_{15}
6	TD_0	28	N.C.	50	TD_{17}
7	TD_2	29	$\overline{PINV}$	51	TD_{19}
8	EXTH	30	SBLK	52	A_0
9	MHENBL	31	SB_1	53	A_2
10	N.C.	32	$\overline{INH}$	54	V_{SS}
11	TD_7	33	$\overline{INVL}$	55	A_6
12	TD_8	34	$\overline{SET}$	56	A_8
13	TD_{10}	35	H/R	57	$\overline{PURGE}$
14	TD_{11}	36	$\overline{HIT}$	58	MODE
15	TD_{12}	37	HC_0/RC_0	59	$\overline{VINV}$
16	TD_{14}	38	HC_1/RC_1	60	SB_0
17	TD_{16}	39	HIT_1/REP_1	61	V_{CC}
18	TD_{18}	40	V_{SS}	62	$\overline{WRITE}$
19	N.C.	41	TD_1	63	RLATCH
20	N.C.	42	TD_3	64	$\overline{PERR}$
21	A_1	43	TD_4		
22	A_3	44	TD_5		

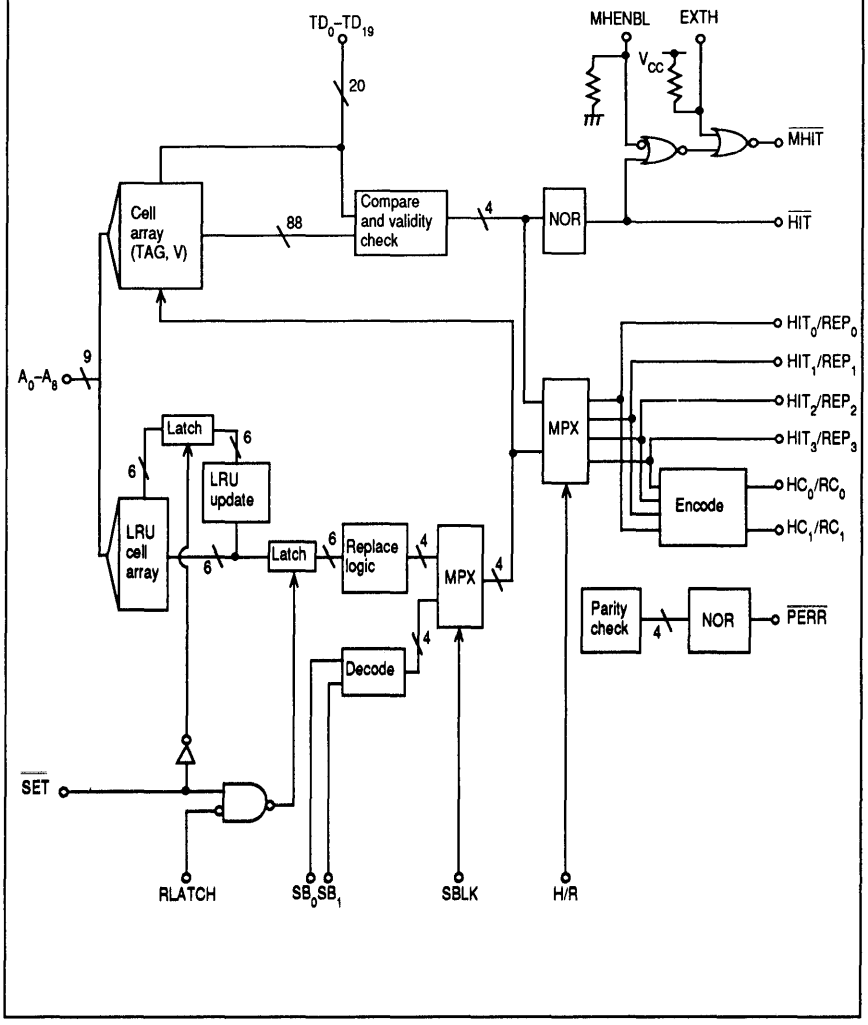
Pin Description

Symbol	Pin Name	Pin No.	I/O	Function
MODE	Mode	58	I	Mode selection MODE = H: 512-entry x 4-way MODE = L: 1024-entry x 2-way
A_0–A_9	Address	52, 21, 53, 22, 23, 24, 55, 25, 56, 26	I	Address inputs: A_9 is not used for 4-way; fix it to H or L
TD_0–TD_{19}	Tag Data	6, 41, 7, 42–45, 11, 12, 46, 13, 14, 15, 48, 16, 49, 17, 50, 18, 51	I	Tag information
$\overline{PURGE}$	Purge	57	I	All purge is done when $\overline{PURGE}$ = L
$\overline{INVL}$	Invalidate	33	I	Partial purge: V bit of specified address is forced to 0 (L)
SBLK	Way Select Enable	30	I	Enables external way selection in replacement and invalidation cycles
SB_0, SB_1	External Way Address	60, 31	I	External way address input: Enabled when SBLK = H
$\overline{WRITE}$	Write	62	I	Enables write
$\overline{SET}$	Set	34	I	Timing pulse Read cycle: Updates LRU Write cycle: Stores tag, sets V bits to H, and updates LRU Partial purge cycle: Shifts LRU and sets V bits to L
$\overline{INH}$	Inhibit	32	I	Inhibits all functions except all purge
H/R	Hit/Replace Selection	35	I	Output selection H/R = H: Hit information H/R = L: Replace information
RLATCH	Replace Latch	63	I	Latch control for replace information
$\overline{PINV}$	Parity Inversion	29	I	Used for testing only
$\overline{VINV}$	Validity Inversion	59	I	Used for testing only
MHENBL	$\overline{MHIT}$ Enable	9	I	Enables $\overline{MHIT}$ output
EXTH	External Hit Control	8	I	Forces $\overline{MHIT}$ output to L
$\overline{HIT}$	Hit	36	O	Hit output: NOR of HIT_0 to HIT_3
HC_0/RC_0 HC_1/RC_1	Hit/Replace Code	37, 38	O	Coded output of hit or replace information
HIT_0/REP_0– HIT_3/REP_3	Hit/Replace	3, 39, 4, 5	O	Uncoded output of hit or replace information
$\overline{PERR}$	Parity Error	64	O	Indicates parity error
$\overline{MHIT}$	Modified Hit	2	O	Hit output modified by MHENBL and EXTH
V_{CC}	Power	47, 61	I	Connects to + 5V power supply
V_{SS}	Ground	40, 54	I	Connects to ground

Block Diagrams



Output Control Block



Function Tables

1. Basic Functions (all combinations not listed below are inhibited)

Input					Tag Info.	Control Info.		LRU	
$\overline{INH}$	$\overline{PURGE}$	$\overline{SET}$	$\overline{WRITE}$	$\overline{INVL}$	Tag Bits	P Bit (Parity)	V Bits (Validity)	LRU Bits	Function Mode
L	H	×	×	×	No change	No change	No change	No change	Inhibit*3
H	H	H	×	×	No change	No change	No change	No change	Tag read
H	H	⊓	H	H	No change	No change	No change	No change*1 or updated	Tag read
H	H	⊓	L	H	TD_0–TD_{19}	Set	H	Updated	Tag write
×	L	H	×	×	Undefined	Undefined	L (All)	Initialized	All purge
H	H	⊓	H	L	No change	No change	No change L*2	No change*1 or shifted*4	Partial purge

×: H or L

Notes: *1 When SBLK = L and there is no hit, LRU is not changed.
*2 When SBLK = L and there is no hit, the V bits are not changed.
*3 In inhibit mode, HIT and PERR outputs are H but all other outputs are L.
*4 Shifted means that the partially-purged way becomes the least recently used way.

2. Hit or Replace Information Output

Input		Internal Information*1, *2				Output							
MODE	A_9	hit_0/ rep_0	hit_1/ rep_1	hit_2/ rep_2	hit_3/ rep_3	HIT_0/ REP_0	HIT_1/ REP_1	HIT_2/ REP_2	HIT_3/ REP_3	HC_0/ RC_0	HC_1/ RC_1	$\overline{HIT}$*3	Mode
H	×	L	L	L	L	L	L	L	L	L	L	H	4-way
H	×	H	L	L	L	H	L	L	L	L	L	L	
H	×	L	H	L	L	L	H	L	L	H	L	L	
H	×	L	L	H	L	L	L	H	L	L	H	L	
H	×	L	L	L	H	L	L	L	H	H	H	L	
L	L	L	×	L	×	L	L	L	L	L	L	H	2-way
L	L	H	×	L	×	H	L	L	L	L	L	L	
L	L	L	×	H	×	L	L	H	L	L	H	L	
L	H	×	L	×	L	L	L	L	L	L	L	H	
L	H	×	H	×	L	L	H	L	L	H	L	L	
L	H	×	L	×	H	L	L	L	H	H	H	L	

×: H or L

Notes: *1 Internal information rep_0 to rep_3 is determined by on-chip LRU logic when SBLK = L.
When SBLK = H, the internal information is determined by external signals SB_0 and SB_1.
*2 Correct operation is not guaranteed if 2 or more ways are hit at the same time.
*3 $\overline{HIT}$ output is valid when H/R = H.

3. Partial Purge ($\overline{INVL}$ = L)

Input					Internal Info.				Purged Way				$\overline{SET}$	
MODE	A_9	SBLK	SB_0	SB_1	hit_0	hit_1	hit_2	hit_3	0	1	2	3	LRU	Mode
H	×	L	×	×	L	L	L	L	—	—	—	—	No change	4-way
H	×	L	×	×	H	L	L	L	Q	—	—	—	Shifted	
H	×	L	×	×	L	H	L	L	—	Q	—	—	Shifted	
H	×	L	×	×	L	L	H	L	—	—	Q	—	Shifted	
H	×	L	×	×	L	L	L	H	—	—	—	Q	Shifted	
H	×	H	L	L	×	×	×	×	Q	—	—	—	Shifted	
H	×	H	H	L	×	×	×	×	—	Q	—	—	Shifted	
H	×	H	L	H	×	×	×	×	—	—	Q	—	Shifted	
H	×	H	H	H	×	×	×	×	—	—	—	Q	Shifted	
L	L	L	×	×	L	×	L	×	—	—	—	—	No change	2-way
L	L	L	×	×	H	×	L	×	Q	—	—	—	Shifted	
L	L	L	×	×	L	×	H	×	—	—	Q	—	Shifted	
L	L	H	L	L	×	×	×	×	Q	—	—	—	Shifted	
L	L	H	L	H	×	×	×	×	—	—	Q	—	Shifted	
L	H	L	×	×	×	L	×	L	—	—	—	—	No change	
L	H	L	×	×	×	H	×	L	—	Q	—	—	Shifted	
L	H	L	×	×	×	L	×	H	—	—	—	Q	Shifted	
L	H	H	H	L	×	×	×	×	—	Q	—	—	Shifted	
L	H	H	H	H	×	×	×	×	—	—	—	Q	Shifted	

Note: Correct operation is not guaranteed if 2 or more ways are hit at the same time.

4. Parity Error and V Bits*1

(n: 0 to 3)

pen	vn_0	vn_1	PEn	Hit Info.*2
L	L	L	L	—
L	L	H	H	Hit
L	H	L	H	Hit
L	H	H	L	Hit
H	L	L	L	—
H	L	H	H	Hit
H	H	L	H	Hit
H	H	H	H	Hit

pen: Internal parity error in way n
vn_0/vn_1: Duplicate validity bits.
PEn: Determined by the following equation:

$$PEn = (vn_0 + vn_1) \cdot pen + (vn_0 \oplus vn_1)$$

Notes: *1 $\overline{PERR}$ is the NOR of PE0 to PE3.
*2 Output information when internal hit is valid.

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V
Input Voltage at Any Pin Relative to V_{SS}	V_{in}	–3.0 to +7.0	V
Output Voltage at Any Pin Relative to V_{SS}	V_{out}	–0.5 to +7.0	V
Output Current	I_{out}	±20	mA
Power Dissipation	P_T	1.5	W
Operating Temperature	T_{opr}	–10 to +85	°C
Storage Temperature	T_{stg}	–65 to +125	°C

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_a = 0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC} *1	4.5	5.0	5.5	V
Input Low Voltage	V_{IL} *1	–0.5 *2	—	0.8	V
Input High Voltage	V_{IH} *1	2.2	—	6.0	V

Notes: *1 All voltages are relative to V_{SS}.

*2 –3.0 V for pulse width of 20 ns or less.

DC and Operating Characteristics (T_a = 0 to +70°C, V_{CC} = 5 V ±10%, V_{SS} = 0 V)

Item	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating Power Supply Current	I_{CC}	Min. cycle, I_{out} = 0 mA	—	—	200	mA
		Cycle = 100 ns, I_{out} = 0 mA	—	—	180	mA
Input Leakage Current	I_{IL}	V_{in} = V_{SS} to V_{CC}	–10	—	10	µA
Output Voltage	V_{OL}	I_{OL} = 8 mA	—	—	0.4	V
	V_{OH}	I_{OH} = –4 mA	2.4	—	—	V

Capacitances (T_a = 25°C, f = 1 MHz)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}	V_{in} = 0 V	—	—	10	pF
Output Capacitance	C_{out}	V_{out} = 0 V	—	—	TBD	pF

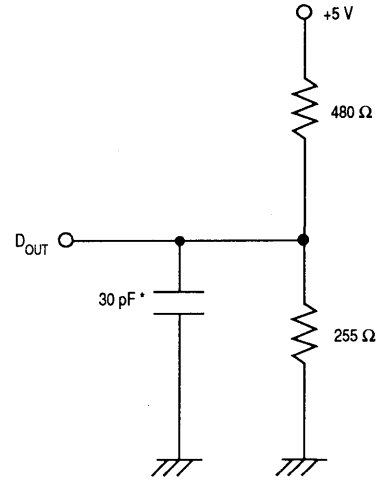
Note: These parameters are sampled, not 100% tested.

AC Characteristics (T_a = 0 to +70°C, V_{CC}= 5 V ±10%, V_{SS}=0V, unless otherwise noted)

AC Test Conditions

- Input pulse levels: 0 V to 3.0 V
- Input pulse rise and fall times: 0 ns to 5 ns (time between 0.8 V and 2.2 V)
- Input and output timing reference levels: 1.5 V
- Output load: See figure.

Output Load



*Including scope and jig

1. **Tag Read Cycle (MODE = H or L, $\overline{\text{PURGE}}$ = H, $\overline{\text{WRITE}}$ = H, $\overline{\text{INVL}}$ = H, $\overline{\text{PINV}}$ = H or L, $\overline{\text{VINV}}$ = H or L, $\overline{\text{INH}}$ = H)**

		HM644332G-25		HM644332G-30		
Item	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
Read Cycle Time	t_{RC}	50	—	50	—	ns
Address Valid to $\overline{\text{HIT}}$, HC_n, HIT_n	t_{AH}	—	25	—	30	ns
Address Valid to $\overline{\text{MHIT}}$	t_{AMH}	—	27	—	32	ns
Tag Data Valid to $\overline{\text{HIT}}$, HC_n, HIT_n	t_{TH}	—	18	—	18	ns
Tag Data Valid to $\overline{\text{MHIT}}$	t_{TMH}	—	20	—	20	ns
$\overline{\text{HIT}}$, HC_n, HIT_n Hold Time	t_{HH}	0	—	0	—	ns
Address Valid to RC_n, REP_n	t_{AR}	—	35	—	40	ns
Address Valid to $\overline{\text{PERR}}$	t_{AP}	—	35	—	40	ns
Address Setup Time for $\overline{\text{SET}}$	t_{AS}	25	—	25	—	ns
Tag Data Setup Time for $\overline{\text{SET}}$	t_{TS}	25	—	25	—	ns
$\overline{\text{SET}}$ Pulse Width	t_{SW}	20	—	20	—	ns
$\overline{\text{SET}}$ Recovery Time	t_{SR}	5	—	5	—	ns
RLATCH Setup Time	t_{RLS}	10	—	10	—	ns
RC_n, REP_n Hold Time for RLATCH	t_{RH}	0	—	0	—	ns
SBLK, SB_0, SB_1 Setup Time for RC_n, REP_n	t_{SBR}	—	25	—	25	ns
SBLK, SB_0, SB_1 Hold Time	t_{SBH}	5	—	5	—	ns
RC_n, REP_n Hold Time for SBLK, SB_0, SB_1	t_{SH}	0	—	0	—	ns
SBLK, SB_0, SB_1 Setup Time for $\overline{\text{SET}}$	t_{SBS}	25	—	25	—	ns
$\overline{\text{PERR}}$ Hold Time	t_{PH}	0	—	0	—	ns
H/R to Multiplex Output Change	t_{HR}	—	10	—	12	ns
MHENBL, EXTH to $\overline{\text{MHIT}}$ Output	t_{MMH}	—	10	—	12	ns

2. Tag Write Cycle (MODE = H or L, $\overline{PURGE}$ = H, $\overline{WRITE}$ = L, $\overline{INVL}$ = H, H/R = L, $\overline{INH}$ = H)

		HM644332G-25		HM644332G-30		
Item	Symbol	Min.	Max.	Min.	Max.	Unit
Write Cycle Time	t_{WC}	50	—	50	—	ns
Address Valid to RC_n, REP_n	t_{AR}	—	35	—	40	ns
Address Setup Time for $\overline{SET}$	t_{AS}	25	—	25	—	ns
Tag Data Setup Time for $\overline{SET}$	t_{TS}	25	—	25	—	ns
$\overline{SET}$ Pulse Width	t_{SW}	20	—	20	—	ns
$\overline{SET}$ Recovery Time	t_{SR}	5	—	5	—	ns
RLATCH Setup Time	t_{RLS}	10	—	10	—	ns
SBLK, SB_0, SB_1 Setup Time for $\overline{SET}$	t_{SBS}	25	—	25	—	ns
SBLK, SB_0, SB_1 Setup Time for RC_n, REP_n	t_{SBR}	—	25	—	25	ns
RC_n, REP_n Hold Time for SBLK, SB_0, SB_1	t_{SH}	0	—	0	—	ns
SBLK Hold Time	t_{SBH}	5	—	5	—	ns
$\overline{PINV}$, $\overline{VINV}$ Setup Time for $\overline{SET}$	t_{IS}	25	—	25	—	ns
$\overline{PINV}$, $\overline{VINV}$ Recovery Time for $\overline{SET}$	t_{IR}	5	—	5	—	ns

3. Partial Purge (MODE = H or L, $\overline{PURGE}$ = H, $\overline{WRITE}$ = H, $\overline{INVL}$ = L, H/R = H or L, $\overline{INH}$ = H, RLATCH = L, $\overline{PINV}$ = H or L, $\overline{VINV}$ = H or L)

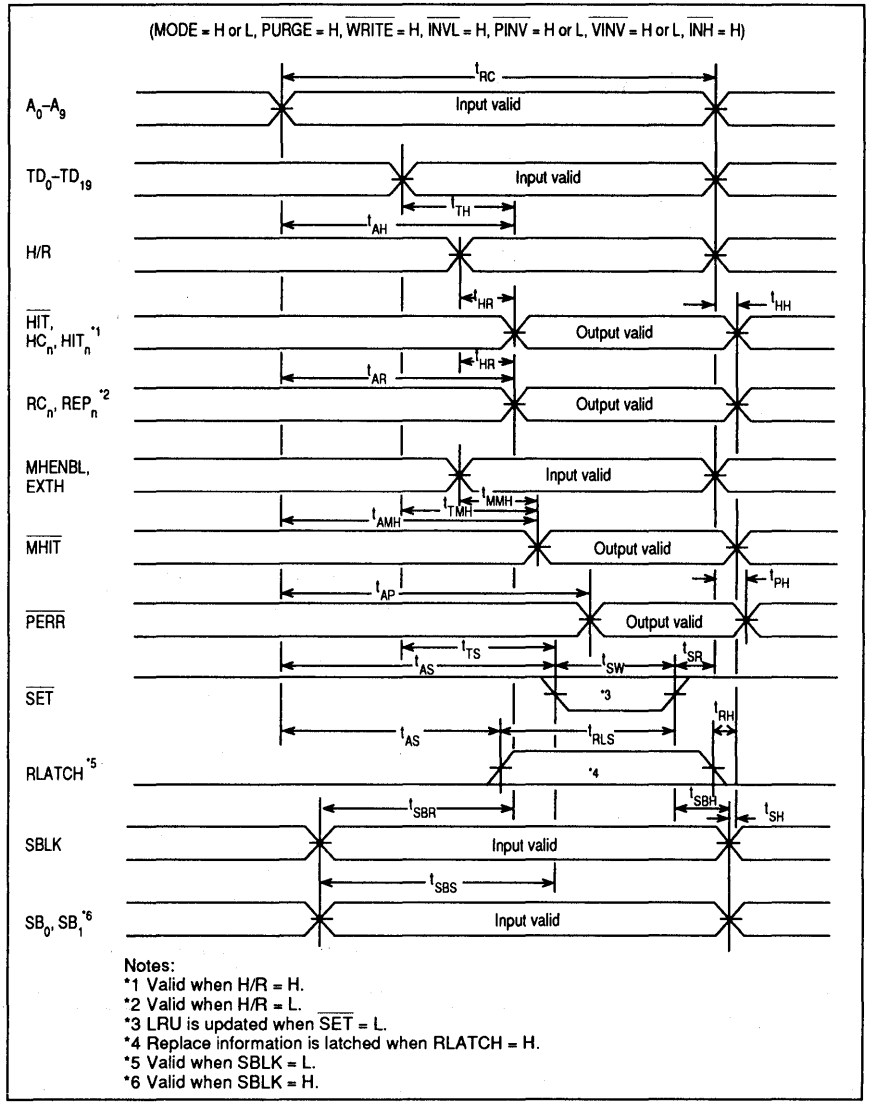
		HM644332G-25		HM644332G-30		
Item	Symbol	Min.	Max.	Min.	Max.	Unit
Partial Purge Cycle	t_{PPC}	50	—	50	—	ns
Address Setup Time for $\overline{SET}$	t_{AS}	25	—	25	—	ns
Tag Data Setup Time for $\overline{SET}$	t_{TS}	25	—	25	—	ns
$\overline{SET}$ Pulse Width	t_{SW}	20	—	20	—	ns
$\overline{SET}$ Recovery Time	t_{SR}	5	—	5	—	ns
SBLK, SB_0, SB_1 Setup Time for $\overline{SET}$	t_{SBS}	25	—	25	—	ns
SBLK, SB_0, SB_1 Hold Time	t_{SBH}	5	—	5	—	ns

4. All Purge ($\overline{SET}$ = H, other control inputs are H or L)

		HM644332G-25		HM644332G-30		
Item	Symbol	Min.	Max.	Min.	Max.	Unit
All Purge Cycle Time	t_{APC}	100	—	100	—	ns
Purge Pulse Width	t_{PPW}	50	—	50	—	ns
Purge Recovery Time	t_{PR}	50	—	50	—	ns

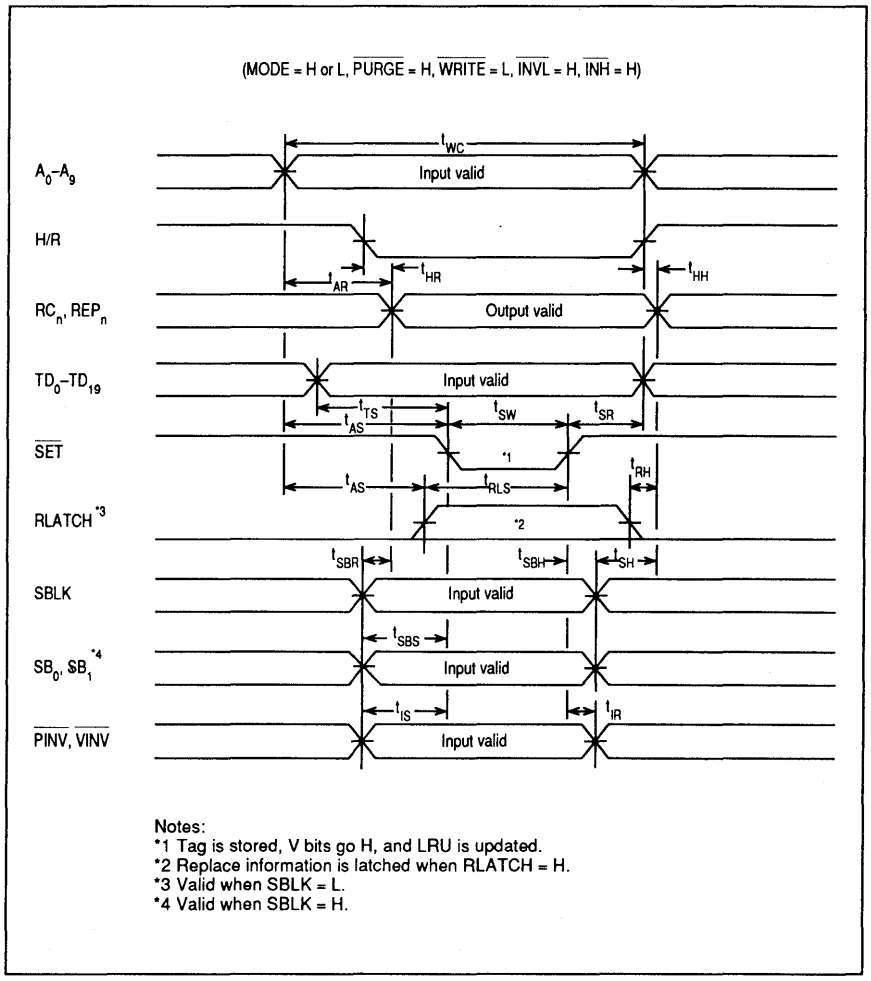
Timing Charts

1. Tag Read Cycle



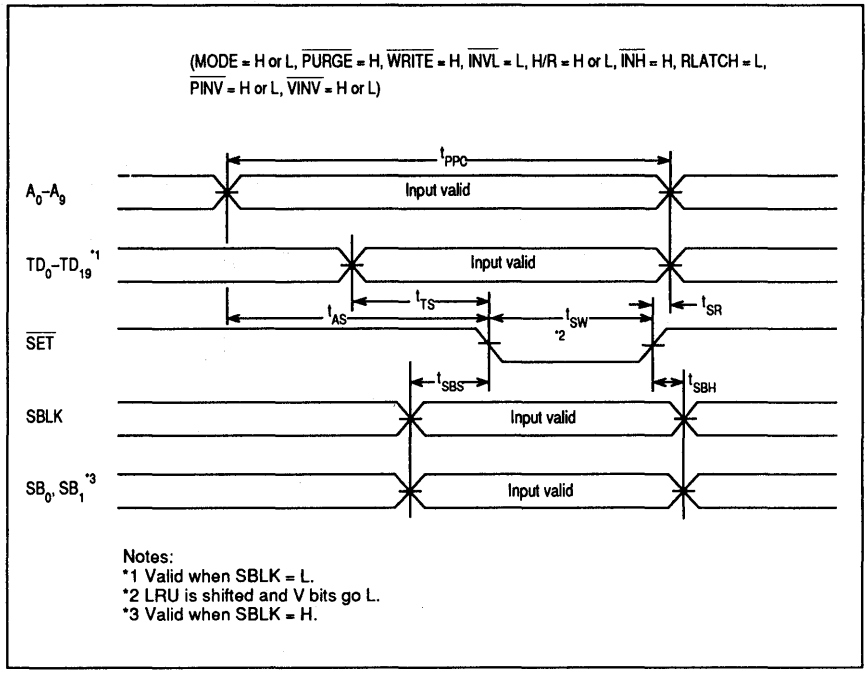
Notes:
*1 Valid when H/R = H.
*2 Valid when H/R = L.
*3 LRU is updated when SET = L.
*4 Replace information is latched when RLATCH = H.
*5 Valid when SBLK = L.
*6 Valid when SBLK = H.

2. Tag Write Cycle



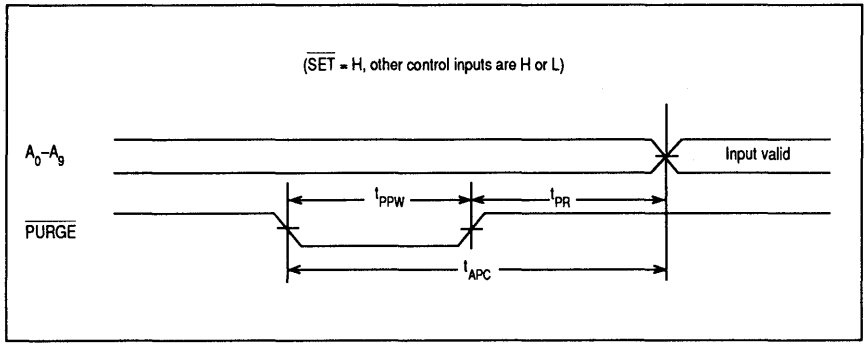
Notes:
*1 Tag is stored, V bits go H, and LRU is updated.
*2 Replace information is latched when RLATCH = H.
*3 Valid when SBLK = L.
*4 Valid when SBLK = H.

3. Partial Purge Cycle



Notes:
*1 Valid when SBLK = L.
*2 LRU is shifted and V bits go L.
*3 Valid when SBLK = H.

4. All Purge Cycle



Function Description

Tag Read

The TAG input data (TD_0-TD_{19}) and the contents of the addressed location are compared. If they are the same, a hit is assumed. $\overline{HIT}$ goes low and the HCn and HITn outputs indicate the hit way associatively. If there is no hit, the LRU logic of the tag RAM automatically specifies which way is to be replaced.

The replacement information is presented at the RCn and REPn outputs by forcing the H/R input low. These signals will be latched and used for writing data into data memory.

Tag Write

If there is no hit, the tag RAM must be updated. A write operation is performed by setting $\overline{WRITE}$ low and inputting a $\overline{SET}$ pulse. The tag data will be written into the appropriate way by the internal LRU logic.

The way can be also specified externally by using SBLK, SB_0, and SB_1 inputs. In tag write mode, the V bits (validity bits) and the parity bit are set, and the LRU is updated.

All Purge

By asserting the $\overline{PURGE}$ input low, all the V bits are reset and LRU is initialized.

In this operation, the contents of each tag and its parity will not be identified.

Partial Purge

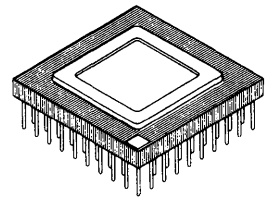
A partial purge operation is performed by setting $\overline{INVL}$ low and inputting a $\overline{SET}$ pulse.

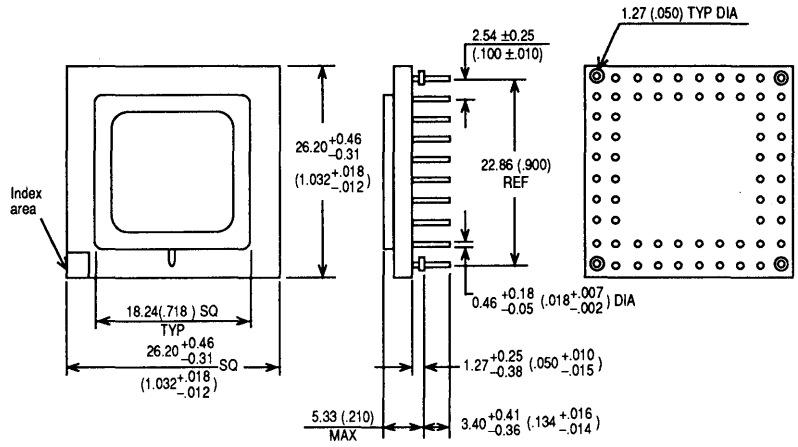
The V bit specified by the address input is reset and the LRU is shifted so that the partially-purged way becomes the least recently used way.

Package Dimensions

Unit: mm (inches)

64-Pin Ceramic PGA





Section 4
MOS Pseudo Static RAM

4

HITACHI®

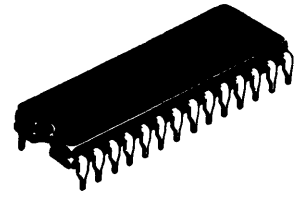
HM65256B Series

32768-word X 8-bit High Speed Pseudo Static RAM

■ FEATURES

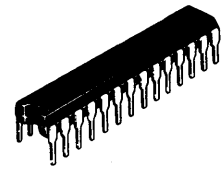
- Single 5V (±10%)
- High Speed
  Access Time
  $\overline{CE}$ Access Time 100/120/150/200ns
  Address Access Time 50/60/75/100ns
  (in Static Column Mode)
  Cycle Time
  Random Read/Write Cycle Time 160/190/235/310ns
  Static Column Mode Cycle Time 55/65/80/105ns
- Low Power
  175mW typ. Active.
- All inputs and outputs TTL compatible
- Static Column Mode Capability
- Non Multiplexed Address
- 256 Refresh Cycles (4ms)
- Refresh Functions
  Address Refresh
  Automatic Refresh
  Self Refresh

HM65256BP Series



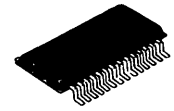
(DP-28)

HM65256BSP Series



(DP-28N)

HM65256BFP Series

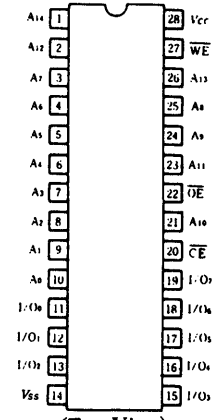


(FP-28DA)

■ ORDERING INFORMATION

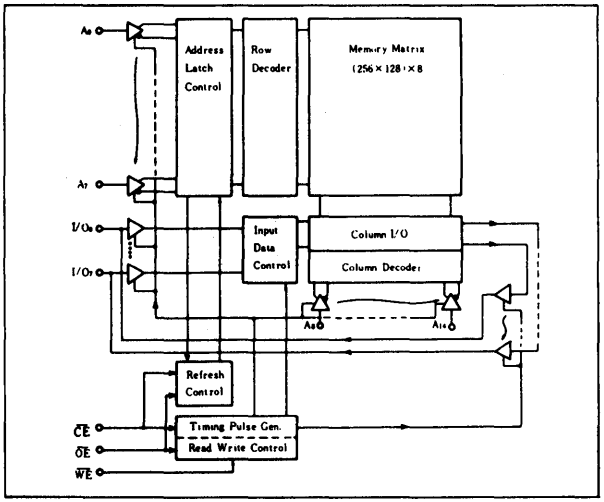
Type No.	Access Time	Package
HM65256BP-10	100ns	600 mil 28 pin Plastic DIP
HM65256BP-12	120ns	
HM65256BP-15	150ns	
HM65256BP-20	200ns	
HM65256BLP-10	100ns	
HM65256BLP-12	120ns	
HM65256BLP-15	150ns	
HM65256BLP-20	200ns	
HM65256BSP-10	100ns	300 mil 28 pin Plastic DIP
HM65256BSP-12	120ns	
HM65256BSP-15	150ns	
HM65256BSP-20	200ns	
HM65256BLSP-10	100ns	
HM65256BLSP-12	120ns	
HM65256BLSP-15	150ns	
HM65256BLSP-20	200ns	
HM65256BFP-10T	100ns	28 pin Plastic SOP
HM65256BFP-12T	120ns	
HM65256BFP-15T	150ns	
HM65256BFP-20T	200ns	
HM65256BLFP-10T	100ns	
HM65256BLFP-12T	120ns	
HM65256BLFP-15T	150ns	
HM65256BLFP-20T	200ns	

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	mode
L	L	H	Low Z	Read
L	×	L	High Z	Write
L	H	H	High Z	–
H	L	×	High Z	Refresh
H	H	×	High Z	Standby

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. V_{IL} min = −3.0V for pulse width ≦ 10ns.

■ DC ELECTRICAL CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

Parameter	Symbol	Test Conditions	HM65256B Series			HM65256BL Series			Unit
			min.	typ.	max.	min.	typ.	max.	
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0mA t_{cyc} = min.	–	35	65	–	35	65	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$	–	1	2	–	1	2	mA
	I_{SB2}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \geq V_{CC}-0.2V$	–	–	–	–	0.05	0.1	mA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$	–	1	2	–	0.6	1	mA
	I_{CC3}	$\overline{CE} \geq V_{CC}-0.2V$, $\overline{OE} \leq 0.2V$	–	–	–	–	50	100	µA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V $Vin = V_{SS}$ to V_{CC}	–10	–	10	–10	–	10	µA
Output Leakage Current	I_{LO}	$\overline{OE} = V_{IH}$ $V_{I/O} = V_{SS}$ to V_{CC}	–10	–	10	–10	–	10	µA
Output Voltage	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	–	–	0.4	V
	V_{OH}	I_{OH} = –1 mA	2.4	–	–	2.4	–	–	V

■ CAPACITANCE

Item	Symbol	Test Conditions	typ.	max.	Unit
Input Capacitance	Cin	Vin = 0V	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	7	pF

Note) This Parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ±10%)

- AC Test Conditions

Input Pulse Levels 2.4V, 0.4V
Input Rise and Fall Times 5ns
Timing Measurement Level 2.2V, 0.8V
Reference Level . . . . . V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load . . . . . 1 TTL and 100pF (including scope and jig)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Random Read or Write Cycle Time	t_{RC}	160	–	190	–	235	–	310	–	ns
Static Column Mode Read or Write Cycle	t_{RSC}	55	–	65	–	80	–	105	–	ns
Chip Enable Access Time	t_{CEA}	–	100	–	120	–	150	–	200	ns
Address Access Time	t_{AA}	–	50	–	60	–	75	–	100	ns
Output Enable Access Time	t_{OEA}	–	40	–	50	–	60	–	75	ns
Chip Disable to Output in High Z	t_{CHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	–	30	–	35	–	40	–	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	10	–	10	–	10	–	ns
Output Disable to Output in High Z	t_{OHZ}	–	25	–	25	–	30	–	35	ns
Chip Enable Pulse Width	t_{CE}	100n	4m	120n	4m	150n	4m	200n	4m	s
Chip Enable Precharge Time	t_P	50	–	60	–	75	–	100	–	ns
Address Set-up Time	t_{AS}	0	–	0	–	0	–	0	–	ns
Row Address Hold Time	t_{RAH}	20	–	20	–	25	–	30	–	ns
Column Address Hold Time	t_{CAH}	100	–	120	–	150	–	200	–	ns
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns
Output Enable Hold Time	t_{OHC}	0	–	0	–	0	–	0	–	ns
Output Enable to Chip Enable Delay Time	t_{OCD}	0	–	0	–	0	–	0	–	ns
Output Hold Time from Column Address	t_{OH}	5	–	5	–	5	–	10	–	ns
Write Command Pulse Width	t_{WP}	25	–	25	–	30	–	35	–	ns
Chip Enable to End of Write	t_{CW}	100	–	120	–	150	–	200	–	ns
Column Address Set-up Time	t_{ASW}	0	–	0	–	0	–	0	–	ns

(to be continued)

Item	Symbol	HM65256B-10		HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Column Address Hold Time after Write	t_{AHW}	0	–	0	–	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	20	–	20	–	25	–	30	–	ns
Data In Hold Time for Write	t_{DH}	0	–	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	5	–	ns
Write to Output in High Z	t_{WHZ}	–	25	–	25	–	30	–	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	50	–	60	–	75	–	100	–	ns
Refresh Precharge Time	t_{FP}	30	–	30	–	30	–	30	–	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80	10000	80	10000	80	10000	80	10000	ns
Automatic Refresh Cycle Time	t_{FC}	160	–	190	–	235	–	310	–	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}	10000	–	10000	–	10000	–	10000	–	ns
Refresh Reset Time for Self Refresh	t_{FRS}	160	–	190	–	235	–	310	–	ns
Refresh Period	t_{REF}	–	4	–	4	–	4	–	4	ms

Notes:

(1) t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions.

(2) t_{CLZ}, t_{OLZ} and t_{OW} are sampled under the condition of t_T=5ns, and not 100% tested.

(3) A write occurs during the overlap of a low $\overline{CE}$ and low $\overline{WE}$.

(4) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

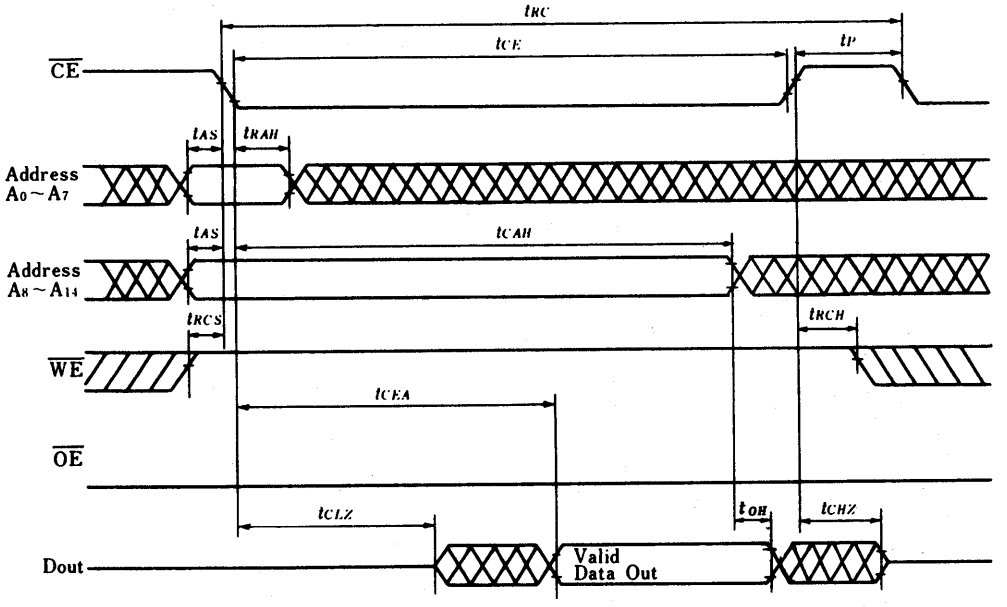
(5) If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.

(6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

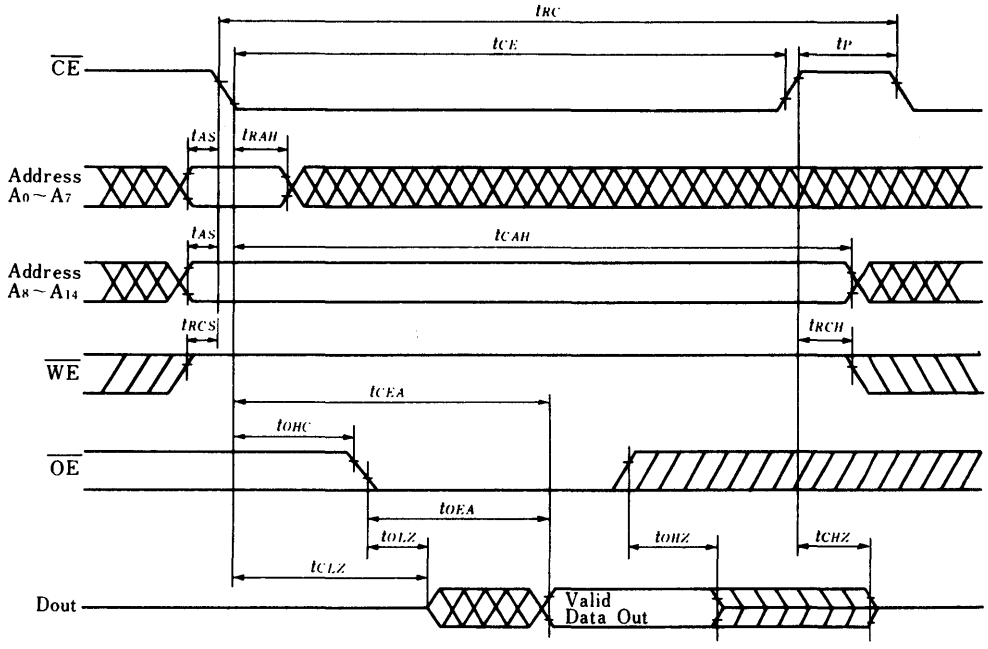
(7) An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

■ TIMING WAVEFORMS

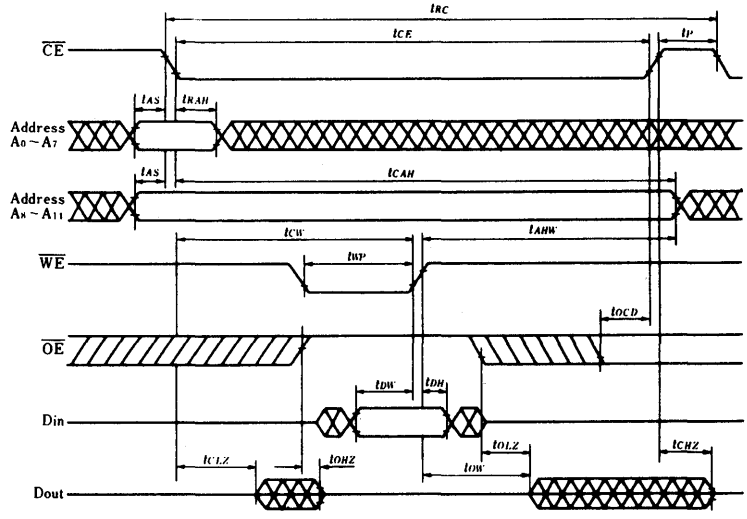
• Read Cycle No. 1 ($\overline{CE}$ controlled)



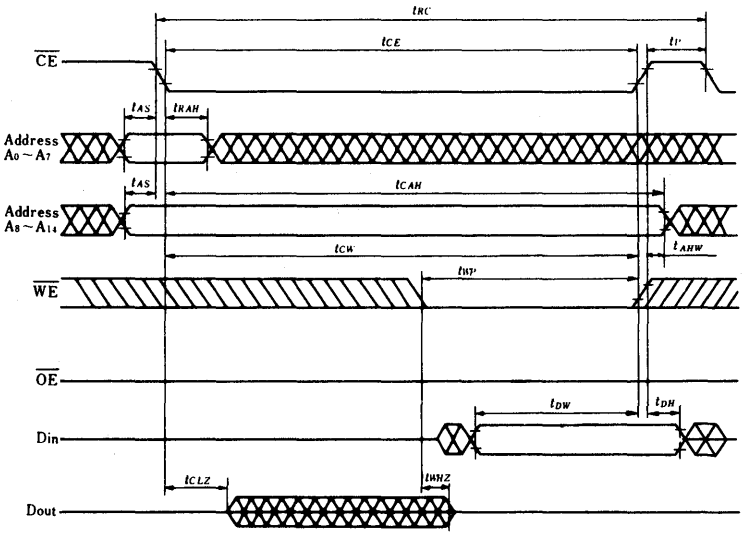
- **Read Cycle No. 2 ($\overline{OE}$ controlled)**



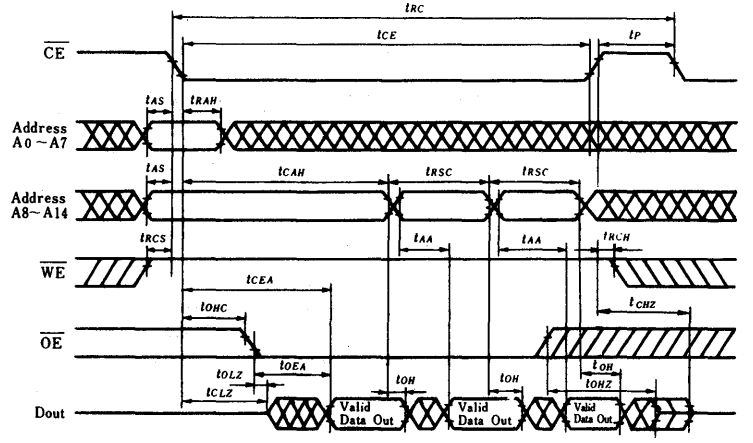
- **Write Cycle No. 1 ($\overline{OE}$ Clock)**



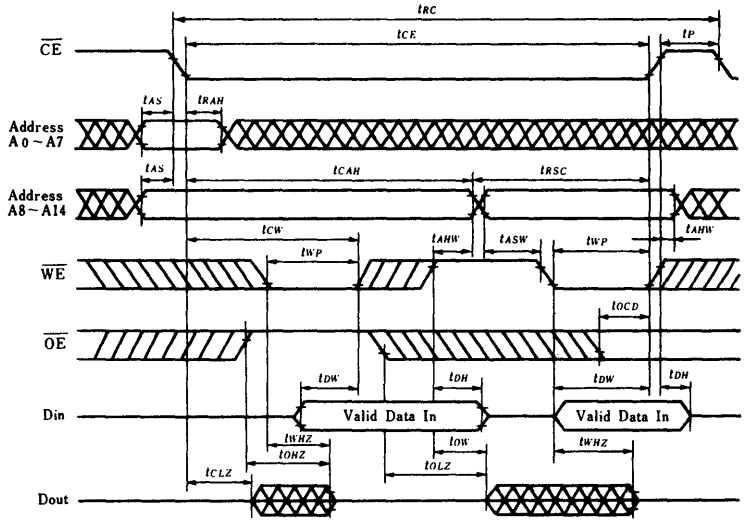
- **Write Cycle No. 2 ($\overline{OE}$ low fix)**



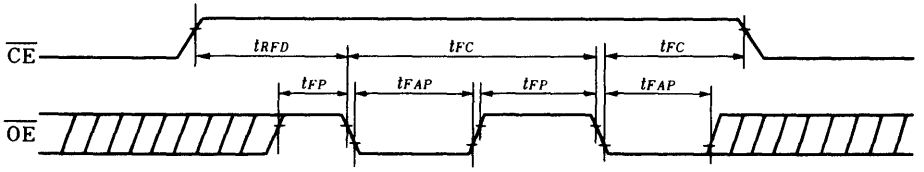
- **Static Column Mode Read Cycle**



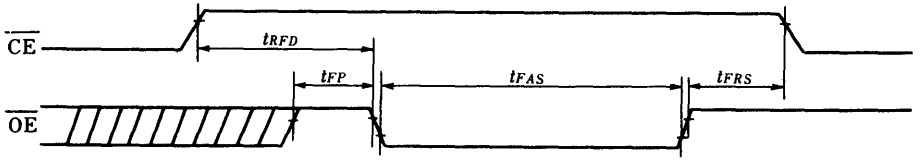
- **Static Column Mode Write Cycle**



- **Automatic Refresh Cycle**



- **Self Refresh Cycle**



HM658128 Series

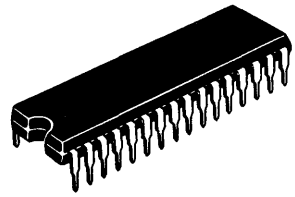
131072-word x 8-bit High Speed CMOS Pseudo Static RAM

The Hitachi HM658128 is a pseudo-static RAM organized as 131,072-word x 8-bit. HM658128 realizes low power consumption and high speed access time by employing 1.3μm CMOS process technology.

The HM658128 supports 3 refresh functions: Address Refresh, Auto Refresh and Self Refresh. Low power version dissipates only 0.5mW (typ.) in Self Refresh Mode and retains the data with battery backup for short time. Self Refresh Mode is guaranteed only for L-version.

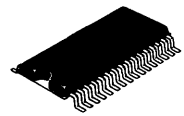
The HM658128 is pin-compatible with 256k-bit PSRAM and static RAM.

HM658128P Series



(DP-32)

HM658128FP Series



(FP-32D)

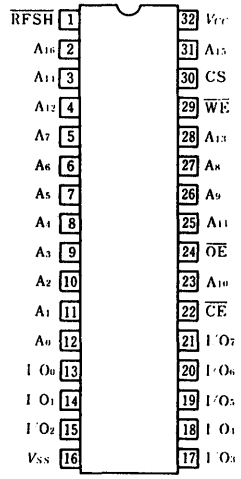
■ FEATURES

- Single 5V (±10%)
- High Speed
  - ○ Access Time
    - $\overline{CE}$ Access Time . . . 100/120/150ns
  - ○ Cycle Time
    - Random Read/Write Cycle Time . . . 180/210/250ns
- Low Power . . . 200mW typ. (Active)
  - 0.5mW (standby)
- All inputs and outputs TTL compatible
- Non Multiplexed Address
- 512 Refresh Cycles (8ms)
- Refresh Functions
  - Address Refresh
  - Automatic Refresh
  - Self Refresh (Only for L-version)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM658128DP-10	100ns	600 mil 32 pin Plastic DIP
HM658128DP-12	120ns	
HM658128DP-15	150ns	
HM658128LP-10	100ns	
HM658128LP-12	120ns	
HM658128LP-15	150ns	
HM658128DFP-10	100ns	32 pin Plastic SOP
HM658128DFP-12	120ns	
HM658128DFP-15	150ns	
HM658128LFP-10	100ns	
HM658128LFP-12	120ns	
HM658128LFP-15	150ns	

■ PIN ARRANGEMENT

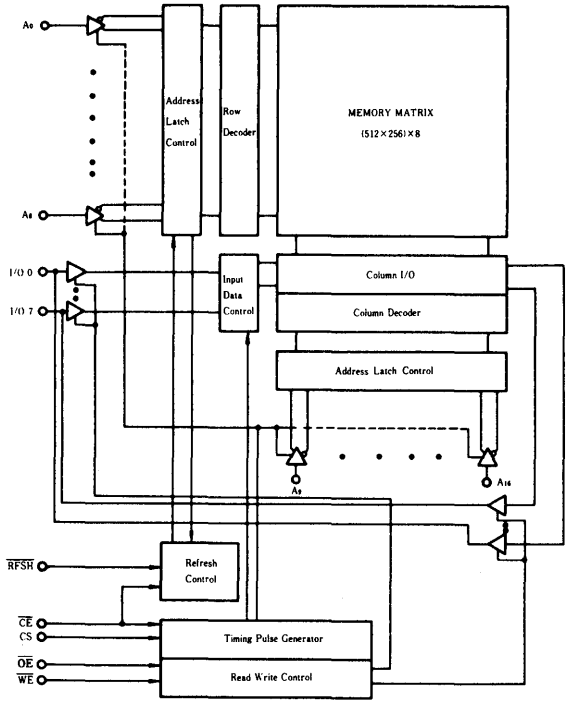


(Top View)

■ PIN DESCRIPTION

Symbol	Pin Name
A0 – A16	Address Inputs
I/O – I/O7	Data Input/Output
$\overline{RFSH}$	Refresh
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
CS	Chip Select
V_{CC}	Power Supply
V_{SS}	Ground

■ BLOCK DIAGRAM



■ TRUTH TABLE

$\overline{CE}$	CS at $\overline{CE}$ going Low	$\overline{RFSH}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode
L	H	X	L	H	Low Z	Read
L	H	X	X	L	High Z	Write
L	H	X	H	H	High Z	–
L	L	X	X	X	High Z	CS Standby
H	X	L	X	X	High Z	Refresh*1
H	X	H	X	X	High Z	Standby

Note) *1. Self refresh is guaranteed only for L-version.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	−1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C
Storage Temperature Under Bias	T_{bias}	−10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS (T_a = 0 to +70°C)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	−0.5*1	–	0.8	V

Note) *1. V_{IL} min = −3.0V for pulse width ≦ 10ns.

■ DC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Operating Power Supply Current	I_{CC1}	$I_{I/O}$ = 0 t_{cyc} = min.	–	40	75	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IH}	–	1	2	mA
Standby Power Supply Current	I_{SB2}	$\overline{CE}$ ≥ V_{CC} –0.2V $\overline{RFSH}$ ≥ V_{CC} –0.2V	–	100	200	μA
Operating Power Supply Current in Self Refresh Mode*1	I_{CC2}	$\overline{CE}$ = V_{IH} $\overline{RFSH}$ = V_{IL}	–	1	2	mA
	I_{CC3}	$\overline{CE}$ ≧ V_{CC} –0.2V $\overline{RFSH}$ ≦ 0.2V	–	100	200	μA
Input Leakage Current	I_{LI}	V_{CC} = 5.5V V_{in} = V_{SS} to V_{CC}	–10	–	10	μA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}	–10	–	10	μA
Output Voltage	V_{OL}	I_{OL} = 2.1mA	–	–	0.4	V
	V_{OH}	I_{OH} = –1mA	2.4	–	–	V

Note) *1. This characteristics is guaranteed only for L-version.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	V_{in} = 0V	–	8	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	–	10	pF

Note) This Parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (T_a = 0 to +70°C, V_{CC} = 5V ± 10%)

• AC Test Conditions

Input Pulse Levels 2.4V, 0.4V
Input Rise and Fall Times 5ns
Timing Measurement Level 2.2V, 0.8V
Reference Level ..... V_{OH} = 2.0V, V_{OL} = 0.8V
Output Load ..... 1 TTL and 100pF (including scope and jig)

Item	Symbol	HM658128-10		HM658128-12		HM658128-15		Unit
		min.	max.	min.	max.	min.	max.	
Random Read or Write Cycle Time	t_{RC}	180	–	210	–	250	–	ns
Random Read Modify Write Cycle Time	t_{RWC}	240	–	280	–	330	–	ns
Chip Enable Access Time	t_{CEA}	–	100	–	120	–	150	ns
Output Enable Access Time	t_{OEA}	–	30	–	40	–	50	ns
Chip Disable to Output in High Z	t_{CHZ}	–	30	–	35	–	40	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	–	35	–	40	–	ns
Output Disable to Output in HighZ	t_{OHZ}	–	25	–	30	–	35	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip Enable Pulse Width	t_{CE}	100n	1μ	120n	1μ	150n	1μ	s
Chip Enable Precharge Time	t_P	70	–	80	–	90	–	ns
Address Set-up Time	t_{AS}	0	–	0	–	0	–	ns
Address Hold Time	t_{AH}	30	–	35	–	40	–	ns
Read Command Set-up Time	t_{RCS}	0	–	0	–	0	–	ns
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns
$\overline{RFSH}$ Hold Time	t_{RHC}	15	–	15	–	15	–	ns
Refresh Command Delay Time (Standby Mode)	t_{RCD}	–	5	–	5	–	5	ns

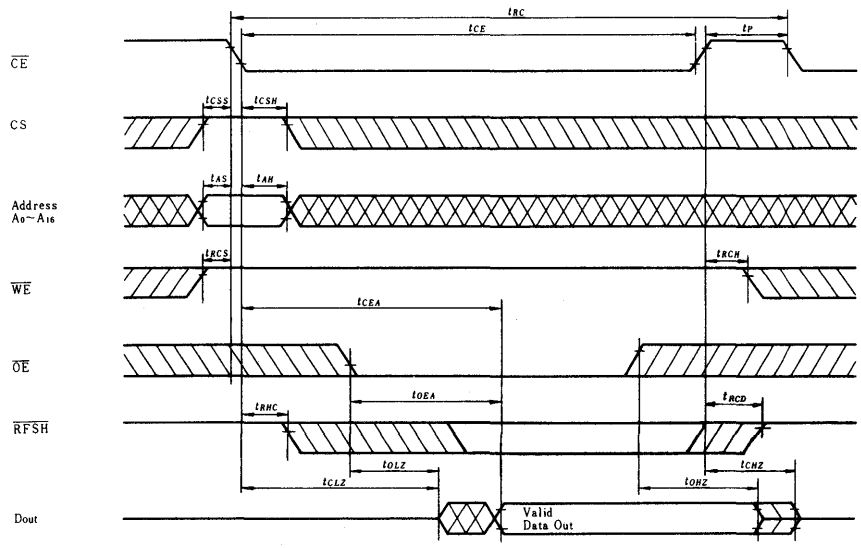
(to be continued)

Item	Symbol	HM658128-10		HM658128-12		HM658128-15		Unit
		min.	max.	min.	max.	min.	max.	
Chip Select Set-up Time	t_{CSS}	0	–	0	–	0	–	ns
Chip Select Hold Time	t_{CSH}	30	–	35	–	40	–	ns
Write Command Pulse Width	t_{WP}	30	–	35	–	40	–	ns
Chip Enable to End of Write	t_{CW}	100	–	120	–	150	–	ns
Data In to End of Write	t_{DW}	25	–	30	–	35	–	ns
Data In Hold Time for Write	t_{DH}	0	–	0	–	0	–	ns
Output Active from End of Write	t_{OW}	5	–	5	–	5	–	ns
Write to Output in High Z	t_{WHZ}	–	25	–	30	–	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	70	–	80	–	90	–	ns
Refresh Precharge Time	t_{FP}	40	–	40	–	40	–	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80n	8μ	80n	8μ	80n	8μ	s
Automatic Refresh Cycle Time	t_{FC}	180	–	210	–	250	–	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}*9	8	–	8	–	8	–	μs
Refresh Reset Time for Self Refresh	t_{RFS}*9	180	–	210	–	250	–	ns
Refresh Reset Time for Automatic Refresh	t_{RFA}	0	–	0	–	0	–	ns
Refresh Period (512 cycles)	t_{REF}	–	8	–	8	–	8	ns

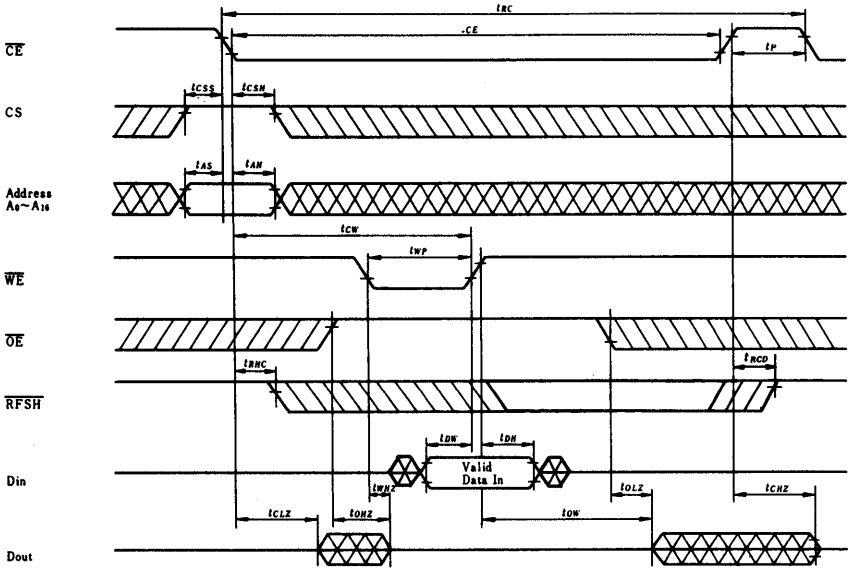
Notes:
(1) t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the output achieves the open circuit conditions under the condition of t_T = 5ns and not 100% tested.
(2) t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ} and t_{OW} are sampled under the condition of t_T = 5ns and not 100% tested.
(3) A write occurs during the overlap of a low $\overline{CE}$ and a low $\overline{WE}$. Write end is defined at the earlier of $\overline{WE}$ going high or $\overline{CE}$ going high.
(4) If $\overline{CE}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.
(5) If input signals of opposite phase to the outputs are applied in write cycle, $\overline{OE}$ or $\overline{WE}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{OE}$ or $\overline{WE}$ turning on output buffers.
(6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
(7) An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.
(8) After Self Refresh, Auto Refresh should be started within 15μs. (only for L-version)
(9) This characteristics is guaranteed only for L-version.

■ TIMING WAVEFORMS

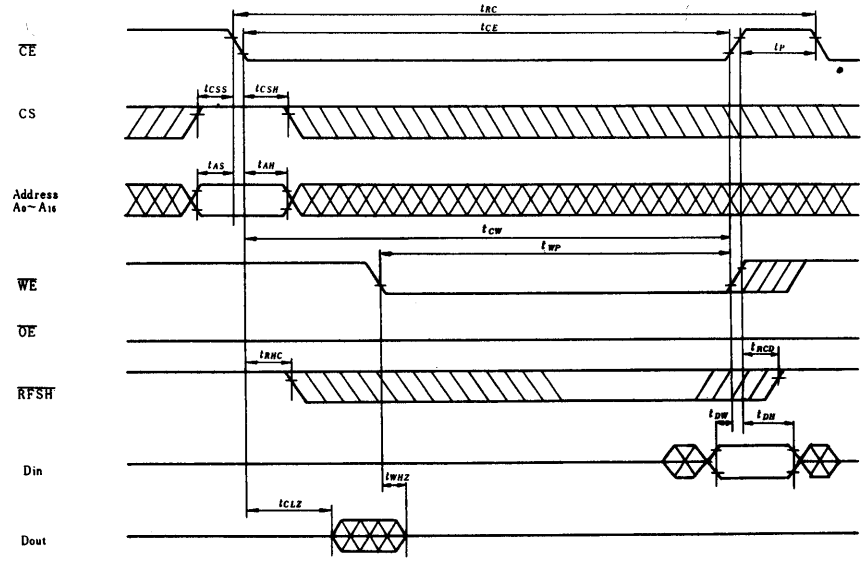
● Read Cycle



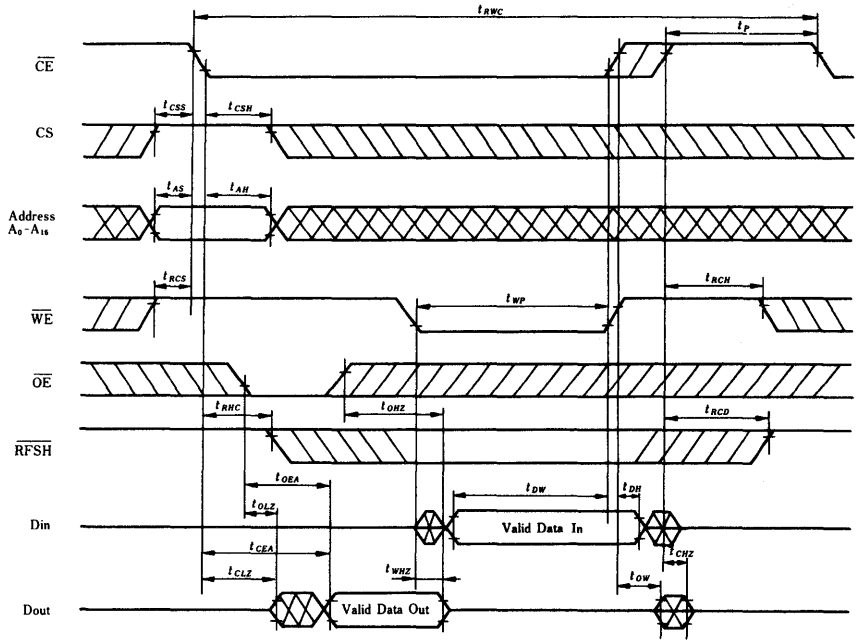
- **Write Cycle-1 ($\overline{OE}$ Clock)**



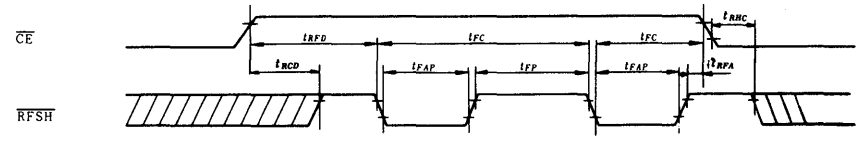
Write Cycle-2 ($\overline{OE}$ Low Fix)



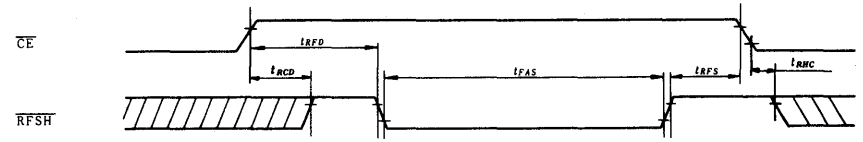
- **Read Modify Write Cycle**



- **Automatic Refresh Cycle**

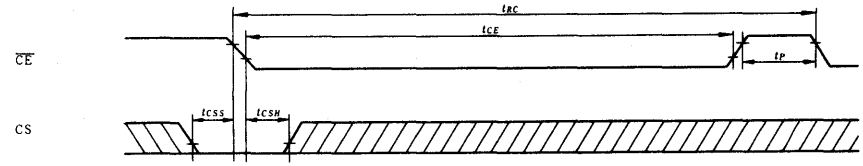


- **Self Refresh Cycle**

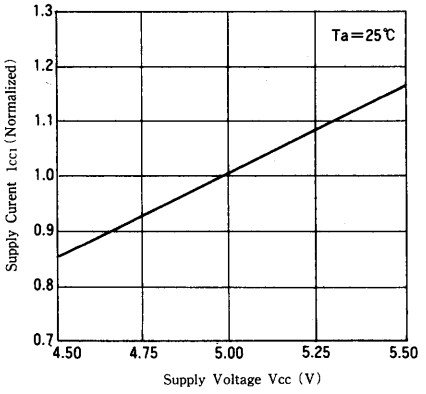


Note) Self refresh is guaranteed only for L-version.

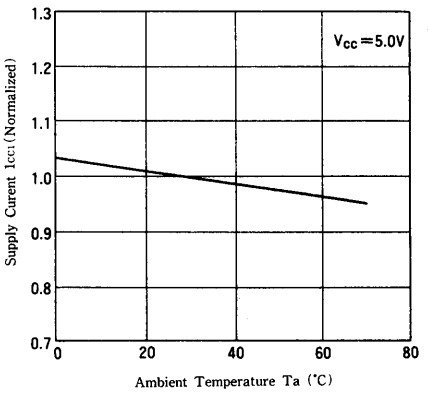
- **CS Standby Mode**



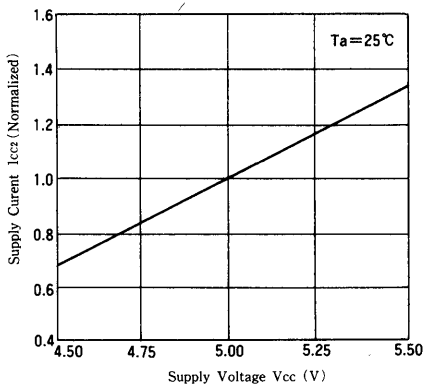
SUPPLY CURRENT VS. SUPPLY VOLTAGE(1)



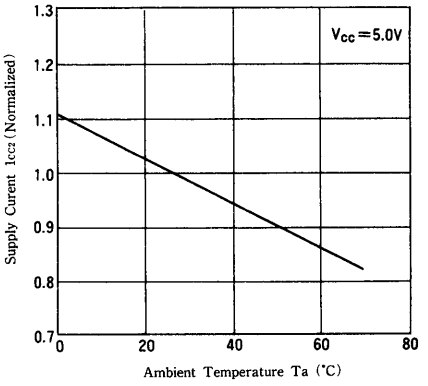
SUPPLY CURRENT VS. AMBIENT TEMPERATURE(1)



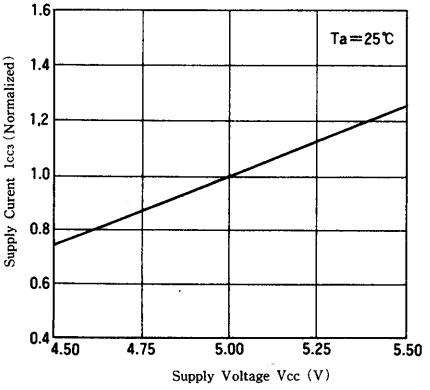
SUPPLY CURRENT VS. SUPPLY VOLTAGE(2)



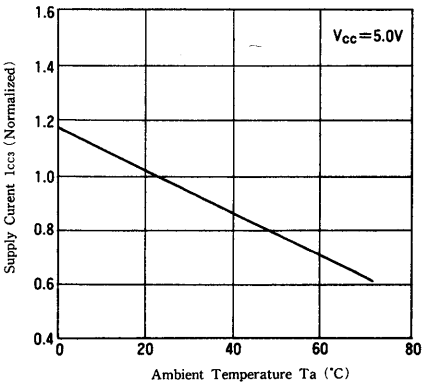
SUPPLY CURRENT VS. AMBIENT TEMPERATURE(2)



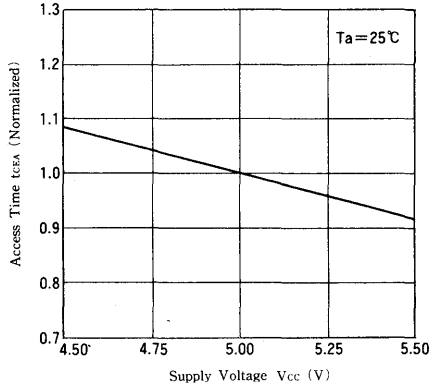
SUPPLY CURRENT VS. SUPPLY VOLTAGE(3)



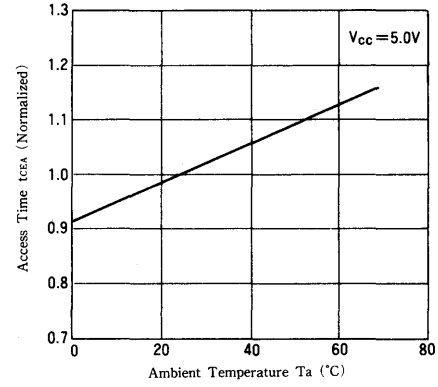
SUPPLY CURRENT VS. AMBIENT TEMPERATURE (3)



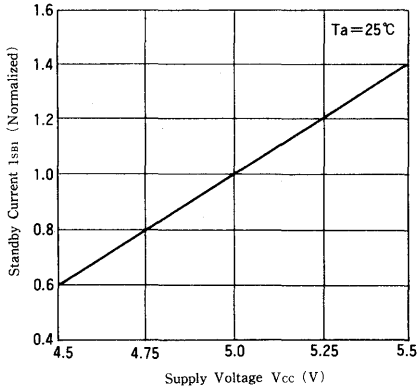
ACCESS TIME VS. SUPPLY VOLTAGE



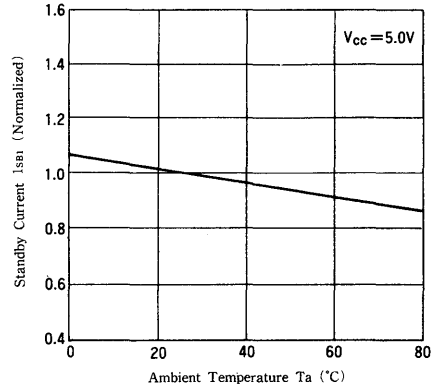
ACCESS TIME VS. AMBIENT TEMPERATURE



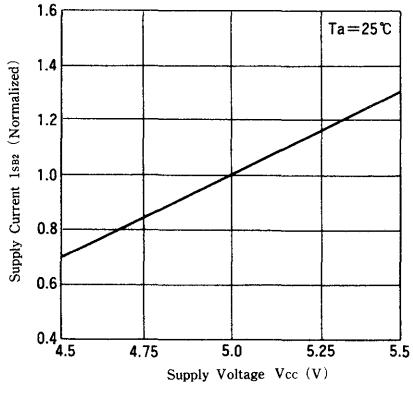
STANDBY CURRENT VS. SUPPLY VOLTAGE(1)



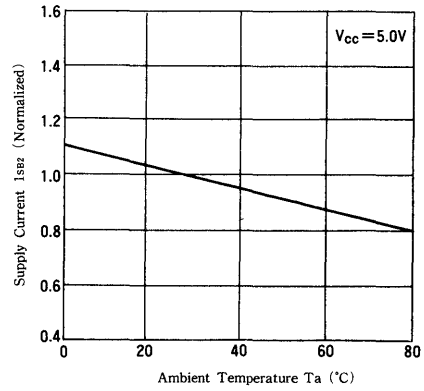
STANDBY CURRENT VS. AMBIENT TEMPERATURE (1)



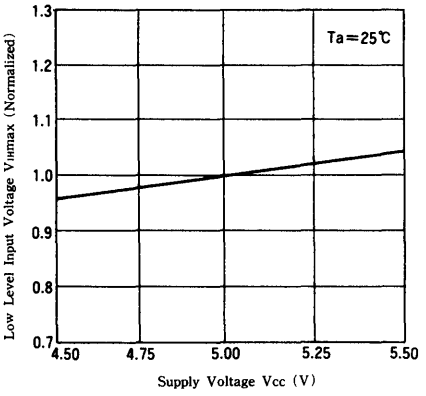
STANDBY CURRENT VS. SUPPLY VOLTAGE(2)



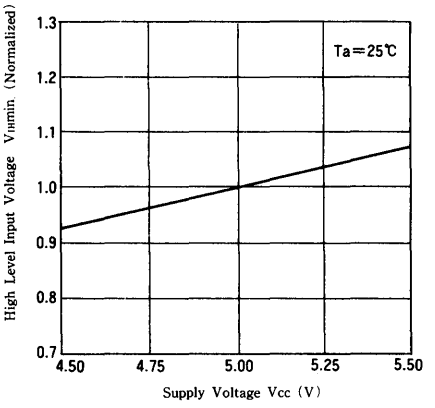
STANDBY CURRENT VS. AMBIENT TEMPERATURE(2)



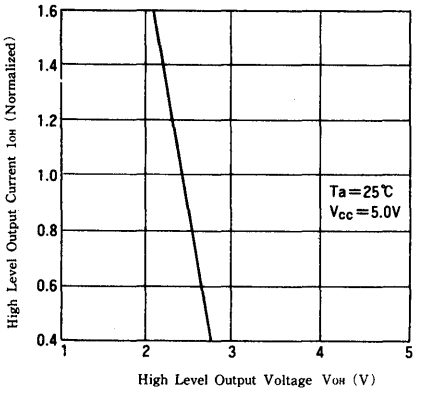
LOW LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



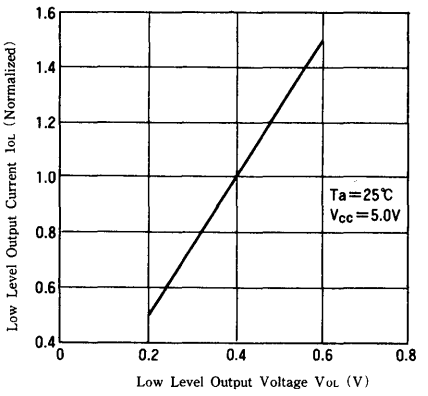
HIGH LEVEL INPUT VOLTAGE VS. SUPPLY VOLTAGE



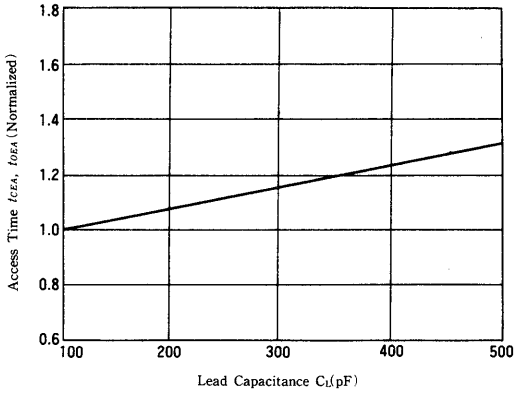
HIGH LEVEL OUTPUT CURRENT VS. OUTPUT VOLTAGE



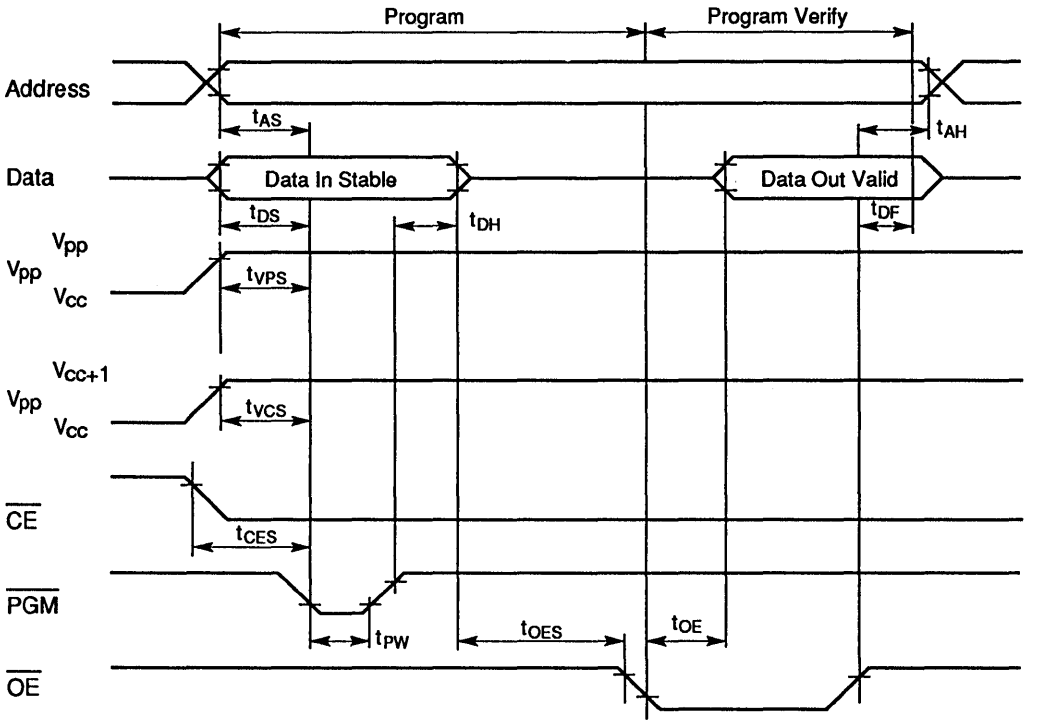
LOW LEVEL OUTPUT CURRENT VS. OUTPUT VOLTAGE



ACCESS TIME VS. LOAD CAPACITANCE



• **Fast High-Reliability Programming Timing Waveform**



Erase

Erasure of HN27C4096G/C is performed by exposure to ultraviolet light of 2537 A and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e., UV intensity × exposure time) for erasure is 15 sec/cm^2.

Mode Description

Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

• **HN27C4096 Identifier Code**

Identifier		A_0	I/O_8–I/O_{15}	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0	Hex Data
	CC-44	(24)	(11)-(4)	(14)	(15)	(16)	(17)	(18)	(19)	(20)	(21)	
	DG-40A	(21)	(10)-(3)	(12)	(13)	(14)	(15)	(16)	(17)	(18)	(19)	
Manufacture Code		V_{IL}	X	0	0	0	0	0	1	1	1	07
Device Code		V_{IH}	X	1	0	1	0	0	0	1	0	A2

NOTES: 1. X = Don't Care.
2. V_H = 12.0V ± 0.5V

Section 5
ECL RAM

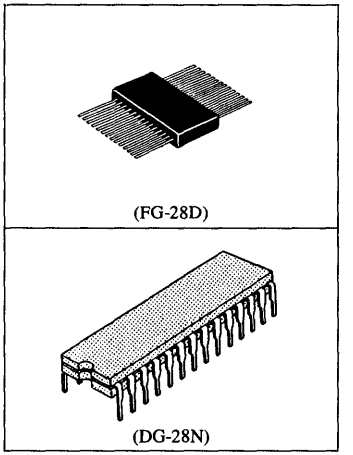
5

HITACHI®

HM10494 Series — Preliminary

16384-word × 4-bit Fully Decoded Random Access Memory

The HM10494 is ECL 10K compatible, 16384-word by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.



Features

- 16384-word × 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: 10/12 ns (max)
- Write pulse width: 6 ns (min)
- Low power dissipation: 800 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

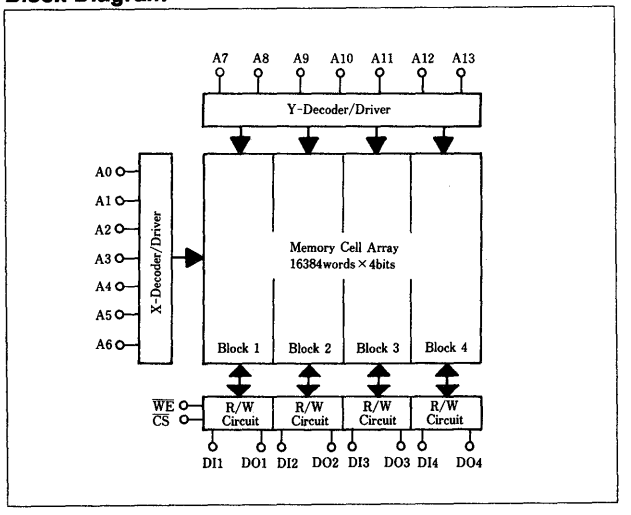
Type No.	Access Time	Package
HM10494-10	10 ns	400 mil 28 pin Cerdip
HM10494-12	12 ns	(DG-28N)
HM10494F-10	10 ns	28 pin Ceramic Flat
HM10494F-12	12 ns	(FG-28D)

Function Table

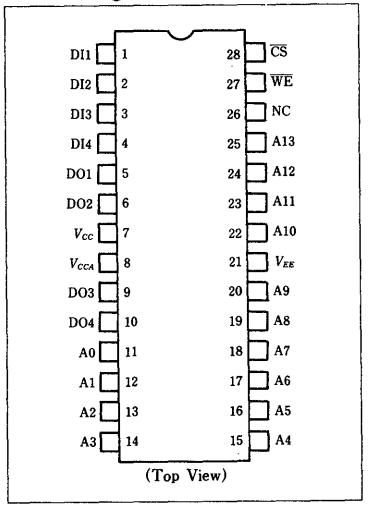
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*1	Read

Notes: ×; Irrelevant *1; Read Out Noninvert

Block Diagram



Pin Arrangement



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to Vcc	+0.5 to −7.0	V
Input Voltage	Vin	+0.5 to V_{EE}	V
Output Current	Iout	−30	mA
Storage Temperature	Tstg	−65 to +150	°C
Storage Temperature	Tstg (Bias)*1	−55 to +125	°C

Note: *1; UnderBias

Electrical Characteristics

DC Characteristics (V_{EE} = −5.2V, R_L = 50Ω to −2.0 V, Ta = 0 to +75°C, air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Conditions	
Output Voltage	V_{OH}	−1000	—	−840	mV	Vin = V_{IHA} or V_{ILB}	0°C
		−960	—	−810			+25°C
		−900	—	−720			+75°C
	V_{OL}	−1870	—	−1665			0°C
		−1850	—	−1650			+25°C
		−1830	—	−1625			+75°C
Output Threshold Voltage	V_{OHC}	−1020	—	—	mV	Vin = V_{IHB} or V_{ILA}	0°C
		−980	—	—			+25°C
		−920	—	—			+75°C
	V_{OLC}	—	—	−1645			0°C
		—	—	−1630			+25°C
		—	—	−1605			+75°C
Input Voltage	V_{IH}	−1145	—	−840	mV	Guaranteed Input Voltage High for All Inputs	0°C
		−1105	—	−810			+25°C
		−1045	—	−720			+75°C
	V_{IL}	−1870	—	−1490		Guaranteed Input Voltage Low for All Inputs	0°C
		−1850	—	−1475			+25°C
		−1830	—	−1450			+75°C
Input Current	I_{IH}	—	—	220	μA	Vin = V_{IHA}	0 to +75°C
	I_{IL}	0.5	—	170		Vin = V_{ILB} $\frac{\overline{CS}}{\text{Others}}$	0 to +75°C
		−50	—	—			
Supply Current	I_{EE}	−180	—	—	mA	All Inputs and Outputs Open	Ta = 0°C
		−180	—	—			Ta = 75°C

AC Characteristics (V_{EE} = −5.2 V ± 5%, Ta = 0 to +75°C, air flow exceeding 2 m/sec)

Read Mode

Item	Symbol	HM10494-10			HM10494-12			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Chip Select Access Time	t_{ACS}	—	—	6	—	—	8	ns	
Chip Select Recovery Time	t_{RCS}	—	—	6	—	—	8	ns	
Address Access Time	t_{AA}	—	—	10	—	—	12	ns	

Write Mode

Item	Symbol	HM10494-10			HM10494-12			Unit	Test Conditions
		Min	Typ	Max	Min	Typ	Max		
Write Pulse Width	t_W	6	—	—	8	—	—	ns	$t_{WSA} = t_{WSA}$ min
Data Setup Time	t_{WSD}	2	—	—	2	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	2	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	2	—	—	ns	$t_W = t_W$ min
Address Hold Time	t_{WHA}	2	—	—	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	—	—	8	ns	
Write Recovery Time	t_{WR}	—	—	12	—	—	14	ns	

Rise/Fall Time

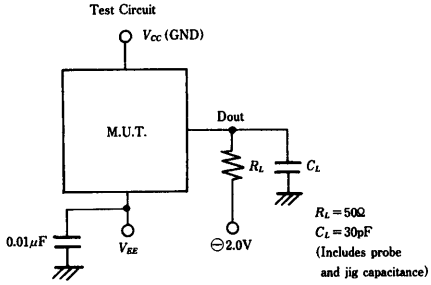
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Rise Time	tr	—	2	—	ns	
Output Fall Time	tf	—	2	—	ns	

Capacitance

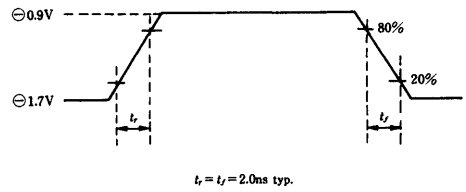
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

Loading Condition

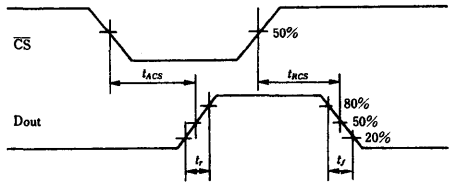


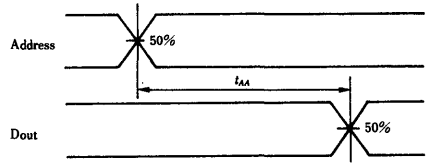
Input Pulse



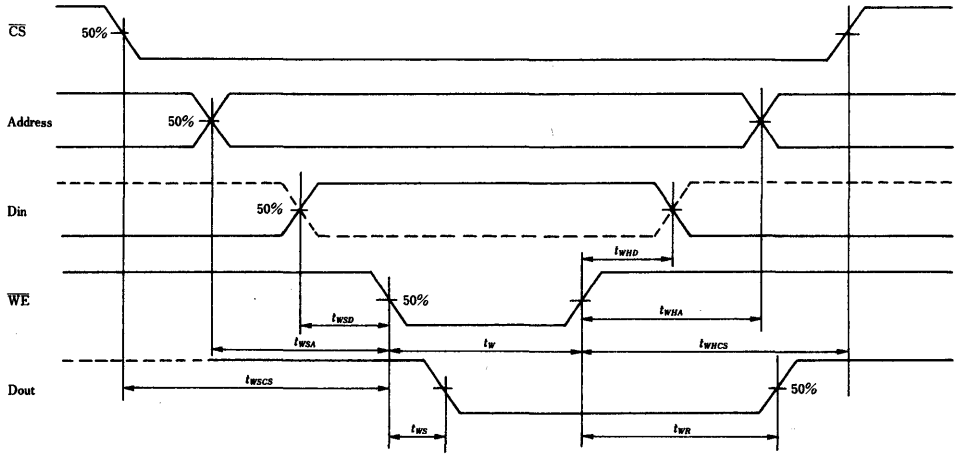
$t_r = t_f = 2.0$ns typ.

Read Mode





Write Mode



HM10490 Series — Preliminary

65536-Words × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

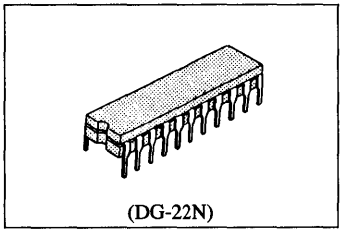
The HM10490 is ECL 10K compatible, 65536-words by 1-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

■ FEATURES

- 65536 × 1 Bit Organization
- Fully Compatible with 10K ECL Level
- Address Access Time .....10/12ns (max.)
- Write Pulse Width .....6/8ns (min.)
- Low Power Dissipation .....570mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

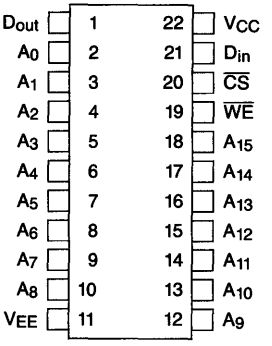
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM10490-10 HM10490-12	10ns 12ns	300 mil 22 pin Cerdip (DG-22N)



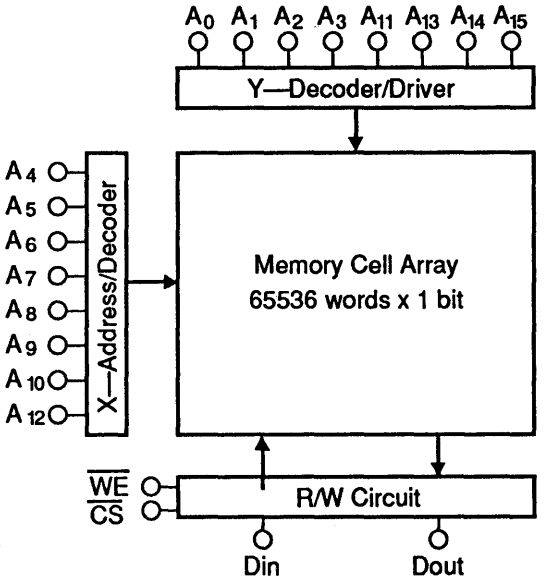
(DG-22N)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(bias)}$*	Θ55 to +125	°C

NOTE: * = Under bias.

■ DC CHARACTERISTICS (V_{EE} = Θ5.2V, R_L = 50Ω to Θ2.0V, T_a = 0 to +75°C, air flow exceeding 2m/sec.)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}	0°C	Θ1000	—	Θ840	mV
			+25°C	Θ960	—	Θ810	
			+75°C	Θ900	—	Θ720	
	V_{OL}		0°C	Θ1870	—	Θ1665	
			+25°C	Θ1850	—	Θ1650	
			+75°C	Θ1830	—	Θ1625	
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}	0°C	Θ1020	—	—	mV
			+25°C	Θ980	—	—	
			+75°C	Θ920	—	—	
	V_{OLC}		0°C	—	—	Θ1645	
			+25°C	—	—	Θ1630	
			+75°C	—	—	Θ1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	Θ1145	—	Θ840	mV
			+25°C	Θ1105	—	Θ810	
			+75°C	Θ1045	—	Θ720	
	V_{IL}	Guaranteed Input Voltage Low for All Inputs	0°C	Θ1870	—	Θ1490	
			+25°C	Θ1850	—	Θ1475	
			+75°C	Θ1830	—	Θ1450	
Input Current	I_{IH}	V_{in} = V_{IHA}	0 to +75°C	—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0 to +75°C	0.5	—	170
			Others		Θ50	—	—
Supply Current	I_{EE}	All Inputs and Outputs Open	0°C, 75°C	Θ140	—	—	mA

■ AC CHARACTERISTICS (V_{EE} = Θ5.2V ± 5%, T_a = 0 to +75°C, air flow exceeding 2m/sec.)

1. Read Mode

Item	Symbol	Test Condition	HM10490-10			HM10490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	8	ns
Address Access Time	t_{AA}		—	—	10	—	—	12	ns

2. Write Mode

Item	Symbol	Test Condition	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
Write Pulse Width	t_W	$t_{WSA} = t_{WSA}$ min.	6	—	—	8	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_W = t_W$ min.	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	12	—	—	14	ns

3. Rise/Fall Time

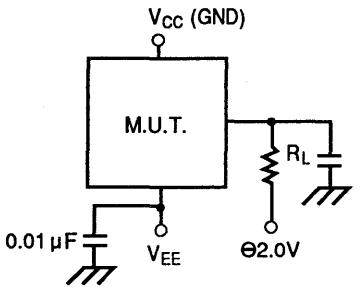
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

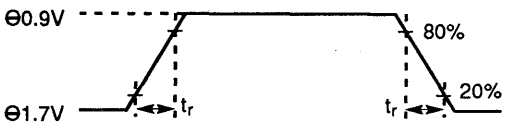
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

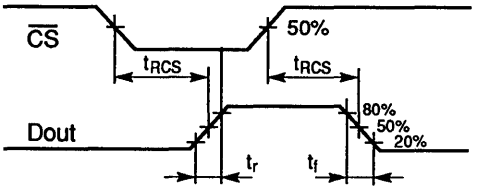
1. Loading Condition

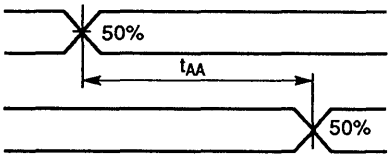


2. Input Pulse

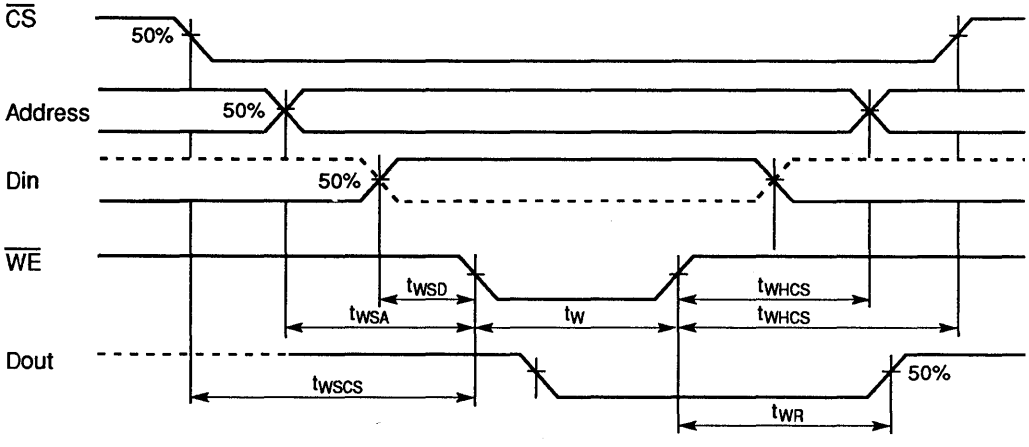


3. Read Mode





4. Write Mode



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HM10504-10/12 — Preliminary

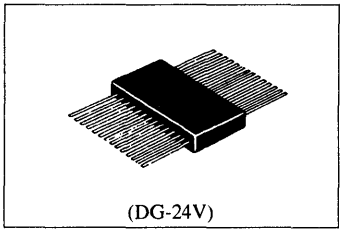
65536-Words × 4-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

The HM10504 is ECL 10K compatible, 65536-words by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

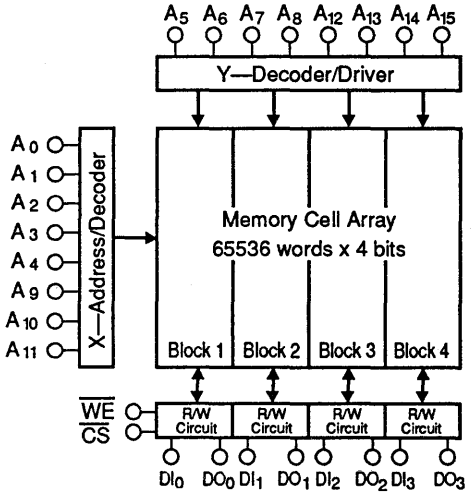
■ FEATURES

- 65536 × 4 Bit Organization
- Fully Compatible with 10K ECL Level
- Address Access Time . . . . . .10/12ns (max.)
- Write Pulse Width . . . . . .8ns (min.)
- Low Power Dissipation . . . . . .620mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

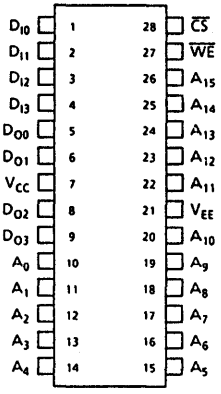


(DG-24V)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM10504-10 HM10504-12	10 ns 12 ns	300 mil 28 pin Cerdip (DG-24V)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

■ PIN DESCRIPTION

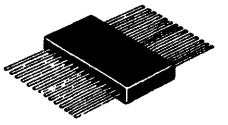
Pin Name	Function
A_0-A_{15}	Address Input
D_{I0}-D_{I3}	Data Input
D_{O0}-D_{O3}	Data Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
V_{CC}	Ground
V_{EE}	Supply Voltage

HM10500-15 — Preliminary

262,144 Words × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

HM10500-15 is ECL 10K compatible, 262,144-words × 1-bit, read/write random access memory developed for high speed systems such as main memories for super computers.



(DG-24V)

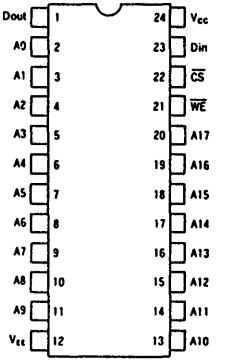
■ FEATURES

- 262,144-words × 1-bit Organization
- Fully Compatible with 10K ECL Level
- Address Access Time. . . . . .15ns (max.)
- Write Pulse Width . . . . . .10ns (min.)
- Low Power Dissipation . . . . . .520mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM10500-15	15ns	300 mil 24 pin Cerdip (DG-24V)

■ PIN ARRANGEMENT



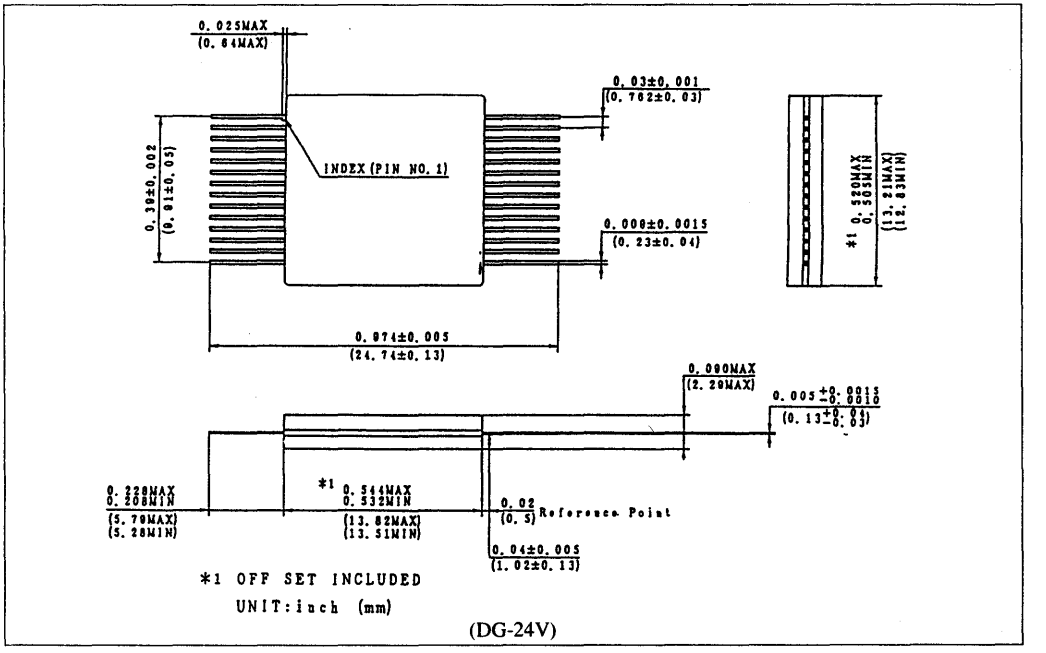
(Top View)

■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*1	Read

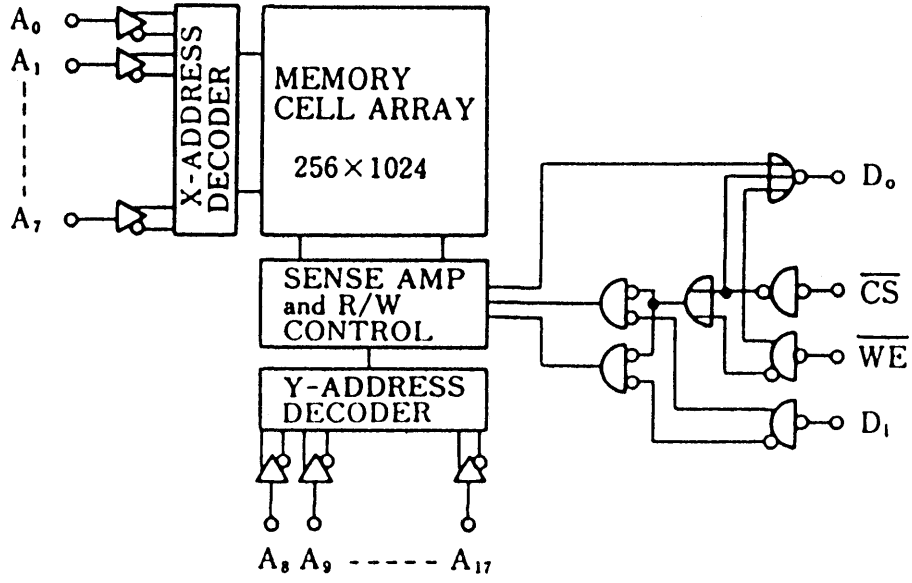
NOTES: X = Irrelevant

*1 = Read Out Noninvert



(DG-24V)

■ BLOCK DIAGRAM



Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg} (Bias)*	−55 to +125	°C

* Under Bias

Electrical Characteristics

DC Characteristics (V_{EE}=−5.2V, R_L=50Ω to −2.0V, Ta=0 to +75°C, air flow exceeding 2m/sec)

Item	Symbol	min (B)	typ	max (A)	Unit	Test Condition	
Output Voltage	V_{OH}	−1000	–	−840	mV	V_{in}=V_{IHA} or V_{ILB}	0°C
		−960	–	−810			+25°C
		−900	–	−720			+75°C
	V_{OL}	−1870	–	−1665			0°C
		−1850	–	−1650			+25°C
		−1830	–	−1625			+75°C
Output Threshold Voltage	V_{OHC}	−1020	–	–	mV	V_{in}=V_{IHB} or V_{ILA}	0°C
		−980	–	–			+25°C
		−920	–	–			+75°C
	V_{OLC}	–	–	−1645			0°C
		–	–	−1630			+25°C
		–	–	−1605			+75°C
Input Voltage	V_{IH}	−1145	–	−840	mV	Guaranteed Input Voltage High for All Inputs	0°C
		−1105	–	−810			+25°C
		−1045	–	−720			+75°C
	V_{IL}	−1870	–	−1490		Guaranteed Input Voltage Low for All Inputs	0°C
		−1850	–	−1475			+25°C
		−1830	–	−1450			+75°C
Input Current	I_{IH}	–	–	220	μA	V_{in}=V_{IHA}	0 to +75°C
	I_{IL}	0.5	–	170		$\overline{CS}$ V_{in}=V_{ILB}	0 to +75°C
		−50	–	–		Others	
Supply Current	I_{EE}	−180	–	–	mA	All Inputs and Outputs Open, Test Pin 12	Ta=0°C
		−180	–	–			Ta=75°C

AC Characteristics (V_{EE}=−5.2V±5%, Ta=0 to +75°C, air flow exceeding 2m/sec)

Read Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	–	–	15	ns	
Chip Select Recovery Time	t_{RCS}	–	–	10	ns	
Address Access Time	t_{AA}	–	–	15	ns	

Write Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Write Pulse Width	t_W	10	–	–	ns	t_{WSA}=2ns
Data Setup Time	t_{WSD}	2	–	–	ns	
Data Hold Time	t_{WHD}	3	–	–	ns	
Address Setup Time	t_{WSA}	2	–	–	ns	t_W=10ns
Address Hold Time	t_{WHA}	3	–	–	ns	
Chip Select Setup Time	t_{WSCS}	2	–	–	ns	
Chip Select Hold Time	t_{WHCS}	3	–	–	ns	
Write Disable Time	t_{WS}	–	–	10	ns	
Write Recovery Time	t_{WR}	–	–	18	ns	

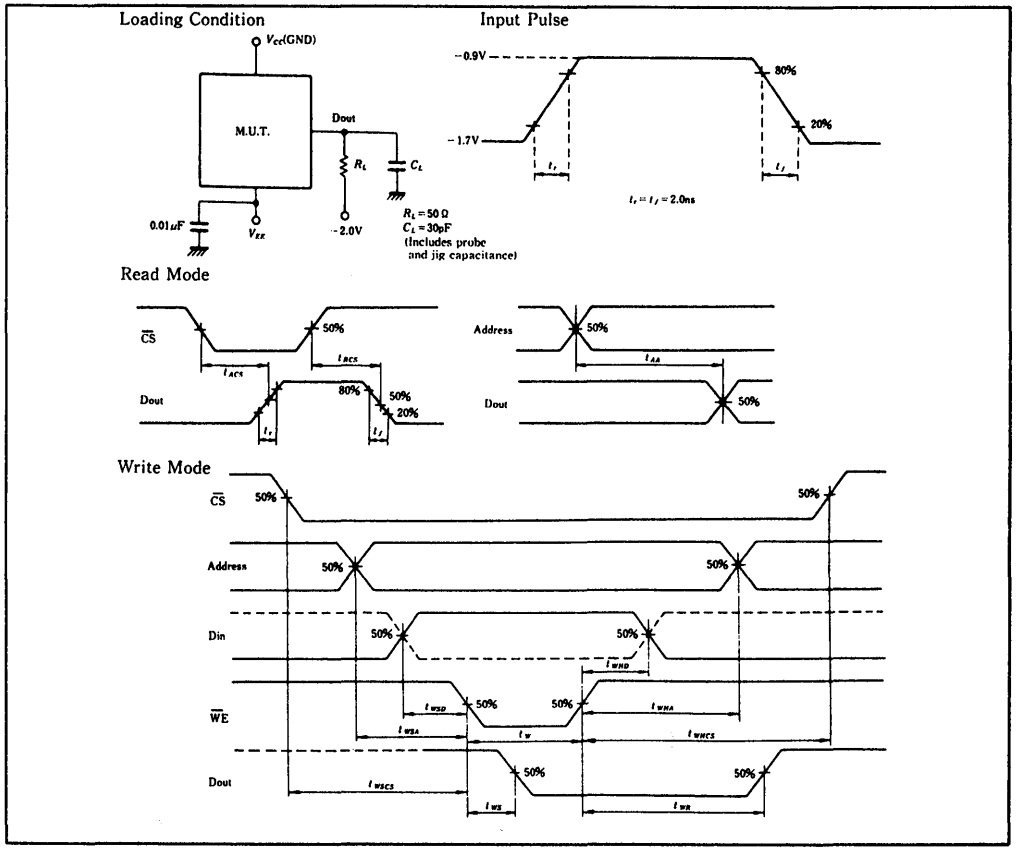
Rise/Fall Time

Item	Symbol	min	typ	max	Unit	Test Condition
Output Rise Time	t_r	–	2	–	ns	
Output Fall Time	t_f	–	2	–	ns	

Capacitance

Item	Symbol	min	typ	max	Unit	Test Condition
Input Capacitance	C_{in}	–	3	–	pF	
Output Capacitance	C_{out}	–	5	–	pF	

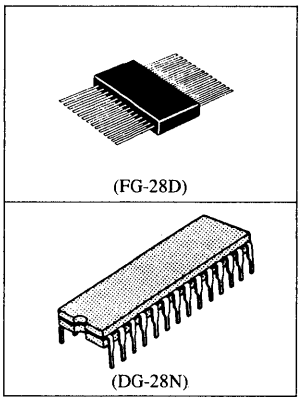
Test Circuit and Waveforms



HM100494 Series — Preliminary

16384-word × 4-bit Fully Decoded Random Access Memory

The HM100494 is ECL 100K compatible, 16384-word by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.



Features

- 16384-word × 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10/12 ns (max)
- Write pulse width: 6 ns (min)
- Low power dissipation: 650 mW (typ)
- Output obtainable by wired-OR (open emitter)

Ordering Information

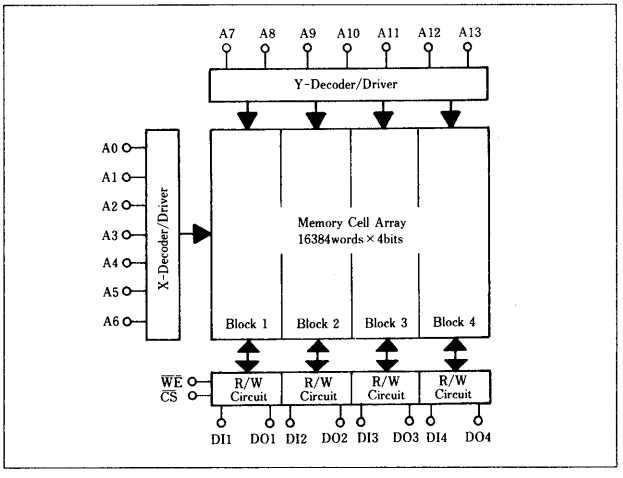
Type No.	Access Time	Package
HM100494-10	10 ns	400 mil 28-pin Cerdip
HM100494-12	12 ns	(DG-28N)
HM100494F-10	10 ns	28-pin Ceramic Flat
HM100494F-12	12 ns	(FG-28D)

Function Table

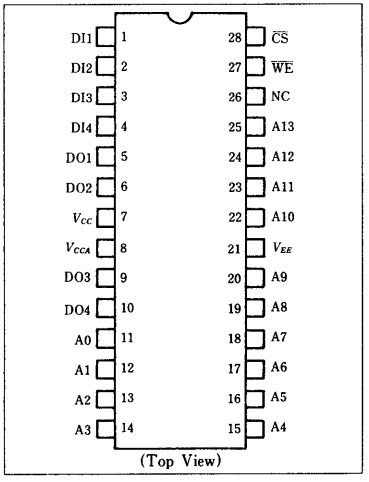
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*1	Read

Notes: ×; Irrelevant *1; Read Out Noninvert

Block Diagram



Pin Arrangement



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to Vcc	+0.5 to –7.0	V
Input Voltage	Vin	+0.5 to V_{EE}	V
Output Current	Iout	–30	mA
Storage Temperature	Tstg	–65 to +150	°C
Storage Temperature	Tstg (Bias)[1]*	–55 to +125	°C

Note: *1: UnderBias

Electrical Characteristics

DC Characteristics (V_{EE} = –4.5 V, R_L = 50Ω to –2.0 V, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Condition
Output Voltage	V_{OH}	–1025	–955	–880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	–1810	–1715	–1620	mV	
Output Threshold Voltage	V_{OHC}	–1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	–1610	mV	
Input Voltage	V_{IH}	–1165	—	–880	mV	Guaranteed Input Voltage
	V_{IL}	–1810	—	–1475	mV	High/Low for All Inputs
Input Current	I_{IH}	—	—	220	µA	Vin = V_{IHA}
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB} $\overline{CS}$
		–50	—	—		Others
Supply Current	I_{EE}	–180	—	—	mA	All Inputs and Outputs Open

AC Characteristics (V_{EE} = –4.5 V ± 5%, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Read Mode

Item	Symbol	HM100494-10			HM100494-12			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Chip Select Access Time	t_{ACS}	—	—	6	—	—	8	ns	
Chip Select Recovery Time	t_{RCS}	—	—	6	—	—	8	ns	
Address Access Time	t_{AA}	—	—	10	—	—	12	ns	

Write Mode

Item	Symbol	HM100494-10			HM100494-12			Unit	Test Condition
		Min	Typ	Max	Min	Typ	Max		
Write Pulse Width	t_W	6	—	—	8	—	—	ns	t_{WSA} = t_{WSA} min
Data Setup Time	t_{WSD}	2	—	—	2	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	2	—	—	ns	
Address Setup Time	t_{WSA}	2	—	—	2	—	—	ns	tw = tw min
Address Hold Time	t_{WHA}	2	—	—	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	2	—	—	2	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	—	—	8	ns	
Write Recovery Time	t_{WR}	—	—	12	—	—	14	ns	

Rise/Fall Time

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Output Rise Time	tr	—	2	—	ns	
Output Fall Time	tf	—	2	—	ns	

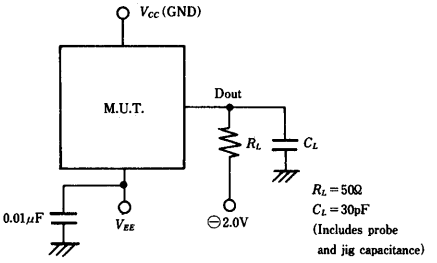
Capacitance

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

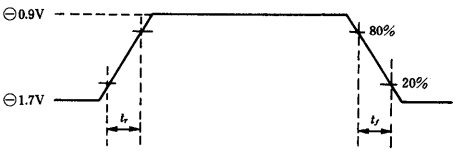
Loading Condition

Test Circuit



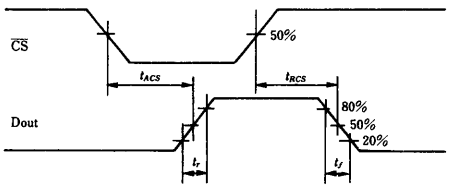
$R_L = 50\Omega$
$C_L = 30pF$
(Includes probe and jig capacitance)

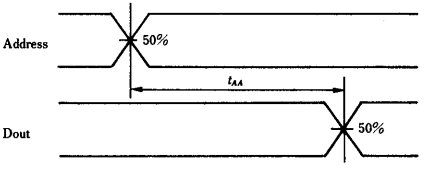
Input Pulse



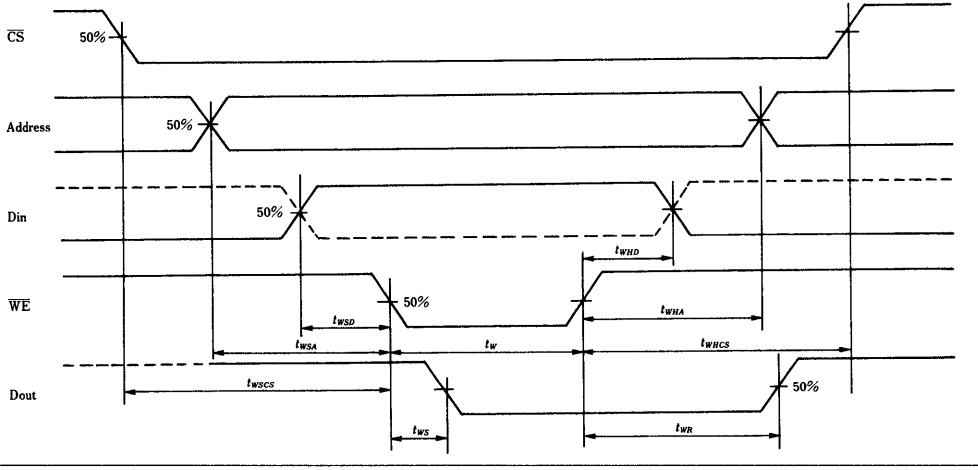
$t_r = t_f = 2.0$ns typ.

Read Mode





Write Mode



HITACHI
Hitachi America, Ltd. • Hitachi Plaza • 2000 Sierra Point Pkwy. • Brisbane, CA 94005-1819 • (415) 589-8300

HM100490 Series — Preliminary

65536-Words × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

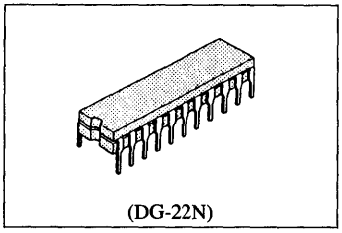
The HM100490 is ECL 100K compatible, 65536-words by 1-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

■ FEATURES

- 65536 × 1 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time .....10/12ns (max.)
- Write Pulse Width .....6/8ns (min.)
- Low Power Dissipation .....500mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

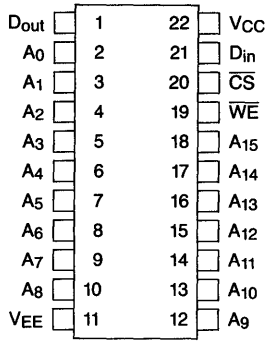
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM100490-10 HM100490-12	10ns 12ns	300 mil 22 pin Cerdip (DG-22N)



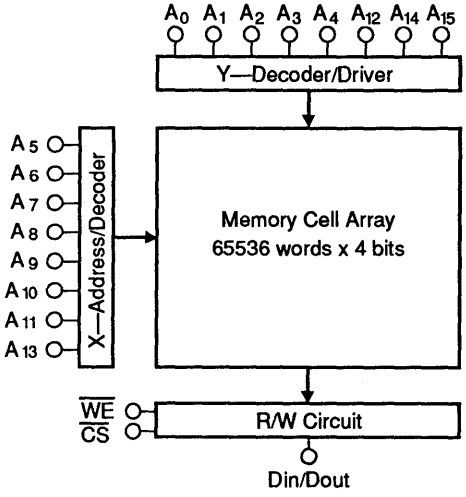
(DG-22N)

■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to Θ3.0	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(under\ bias)}$	Θ55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• DC Characteristics (V_{EE} = -4.5V, R_L = 50Ω to -2.0V, T_a = 0 to +85°C, air flow exceeding 2m/sec.)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		Θ1025	Θ955	Θ880	mV
	V_{OL}			Θ1810	Θ1715	Θ1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		Θ1035	—	—	mV
	V_{OLC}			—	—	Θ1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		Θ1165	—	Θ880	mV
	V_{IL}			Θ1810	—	Θ1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	Θ50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		Θ140	—	—	mA

• AC Characteristics (V_{EE} = -4.5V ± 5%, T_a = 0 to +85°C, air flow exceeding 2m/sec.)

1. Read Mode

Item	Symbol	Test Condition	HM100490-10			HM100490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	8	ns
Address Access Time	t_{AA}		—	—	10	—	—	12	ns

2. Write Mode

Item	Symbol	Test Condition	HM100490-10			HM100490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Write Pulse Width	t_W	t_{WSA} = t_{WSA} min.	6	—	—	8	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = t_W min.	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	12	—	—	14	ns

3. Rise/Fall Time

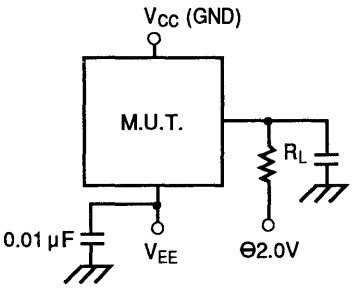
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

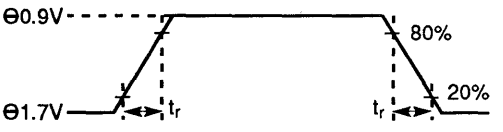
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

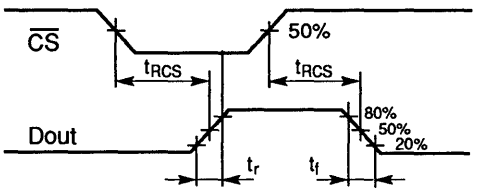
1. Loading Condition

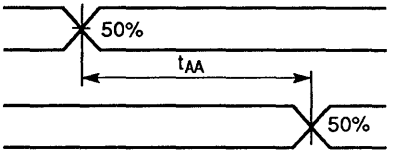


2. Input Pulse

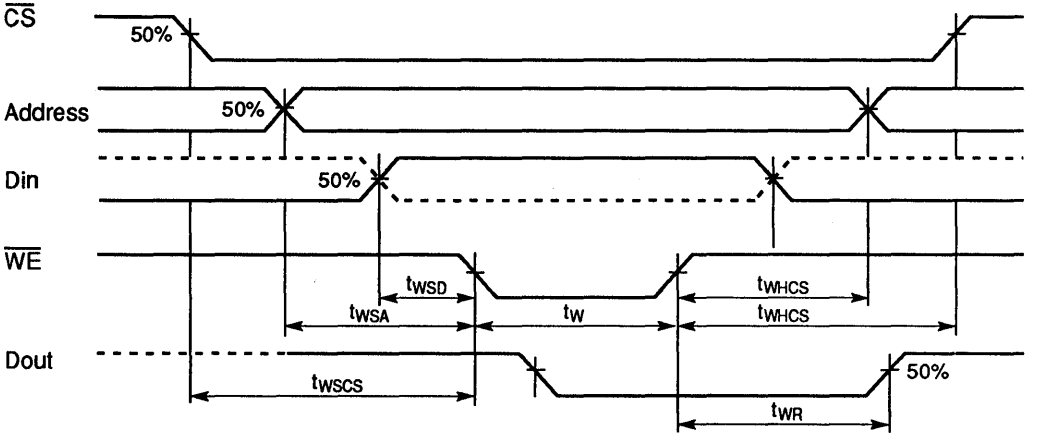


3. Read Mode





4. Write Mode


CS
Address
Din
WE
Dout
50%
50%
50%
50%
tWSD
tWSA
tW
tWHCS
tWHCS
tWSCS
tWR

HM100504F-10/12 — Preliminary

65536-Words × 4-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

The HM100504 is ECL 100K compatible, 65536-words by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

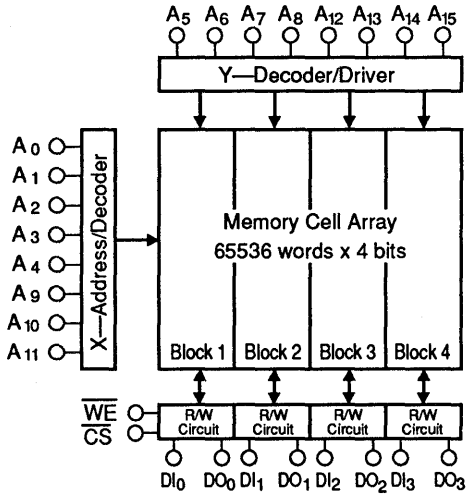
■ FEATURES

- 65536 × 4 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time . . . . . .10/12ns (max.)
- Write Pulse Width . . . . . .8ns (min.)
- Low Power Dissipation . . . . . .500mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

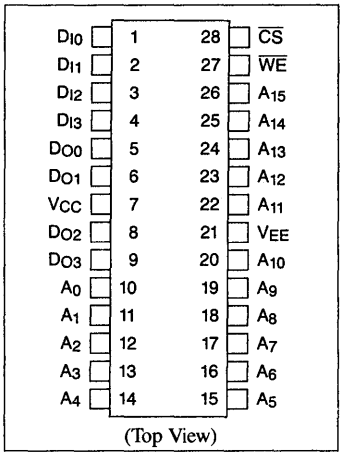
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM100504F-10	10 ns	28 pin Ceramic Flat Package
HM100504F-12	12 ns	(30 mil lead Pitch)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

HM100500CG-18 — Preliminary

262,144-Word × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

The HM100500CG-18 is ECL 100K compatible, 262,144-word × 1-bit, read/write random access memory developed for high speed systems such as main memories for super computers.

■ FEATURES

- 262,144-Word × 1-Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time. . . . . .18ns (max.)
- Write Pulse Width . . . . . .10ns (min.)
- Low Power Dissipation . . . . . .500mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ ORDERING INFORMATION

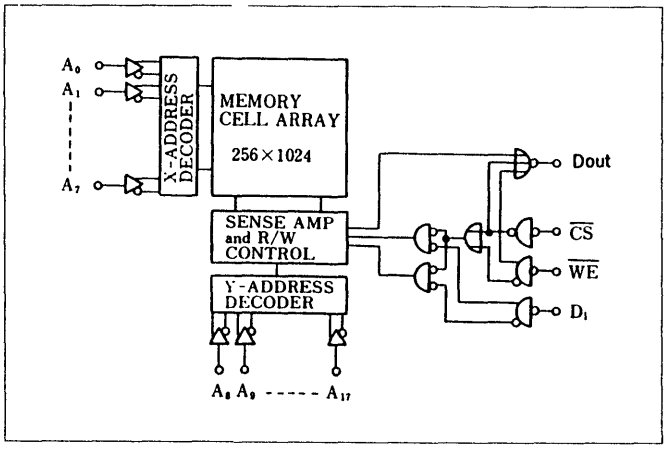
Type No.	Access Time	Package
HM100500-18	18ns	24 pin CERDIP (DG-24V)
HM100500CG-18	18ns	28 pin LCC (CG-28B)
HM100500F-18	18ns	24 pin Ceramic Flat (FG-24A)

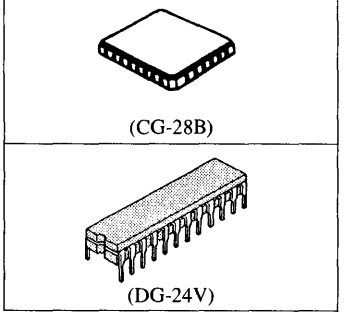
■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*1	Read

NOTES: X = Irrelevant
*1 = Read Out Noninvert

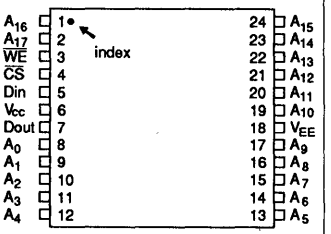
■ BLOCK DIAGRAM





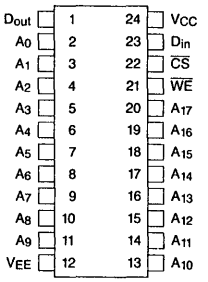
■ PIN ARRANGEMENT

(FG-24A)



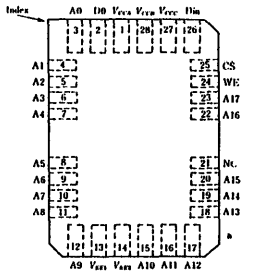
(Top View)

(DG-24V)



(Top View)

(CG-28B)



(Top View)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to Vcc	+0.5 to −7.0	V
Input Voltage	Vin	+0.5 to V_{EE}	V
Output Current	Iout	−30	mA
Storage Temperature	Tstg	−65 to +150	°C
Storage Temperature	Tstg (Bias)*1	−55 to +125	°C

Note: *1; Under Bias

Electrical Characteristics

DC Characteristics (V_{EE} = −4.5 V, R_L = 50Ω to −2.0 V, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Item	Symbol	Min (B)	Typ	Max (A)	Unit	Test Conditions
Output Voltage	V_{OH}	−1025	−955	−880	mV	Vin = V_{IHA} or V_{ILB}
	V_{OL}	−1810	−1715	−1620	mV	
Output Threshold Voltage	V_{OHC}	−1035	—	—	mV	Vin = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	−1610	mV	
Input Voltage	V_{IH}	−1165	—	−880	mV	Guaranteed Input Voltage
	V_{IL}	−1810	—	−1475	mV	High/Low for All Inputs
Input Current	I_{IH}	—	—	220	µA	Vin = V_{IHA}
	I_{IL}	0.5	—	170	µA	Vin = V_{ILB} $\overline{CS}$
		−50	—	—		Others
Supply Current	I_{EE}	−160	—	—	mA	All Inputs and Outputs Open

AC Characteristics (V_{EE} = −4.5 V ± 5%, Ta = 0 to +85°C, air flow exceeding 2 m/sec)

Read Mode

Item	Symbol	Min	Typ	CG-18 Max	F-18 Max	Unit	Test Conditions
Chip Select Access Time	t_{ACS}	—	—	18	15	ns	
Chip Select Recovery Time	t_{RCS}	—	—	18	10	ns	
Address Access Time	t_{AA}	—	—	18	18	ns	

Write Mode

Item	Symbol	Min	Typ	CG-18 Max	F-18 Max	Unit	Test Conditions
Write Pulse Width	t_W	10	—	—		ns	t_{WSA} = 2 ns
Data Setup Time	t_{WSD}	2	—	—			
Data Hold Time	t_{WHD}	3	—	—		ns	
Address Setup Time	t_{WSA}	2	—	—		ns	t_W = 10 ns
Address Hold Time	t_{WHA}	3	—	—		ns	
Chip Select Setup Time	t_{WSCS}	2	—	—		ns	
Chip Select Hold Time	t_{WHCS}	3	—	—		ns	
Write Disable Time	t_{WS}	—	—	15	10	ns	
Write Recovery Time	t_{WR}	—	—	21	21	ns	

Rise/Fall Time

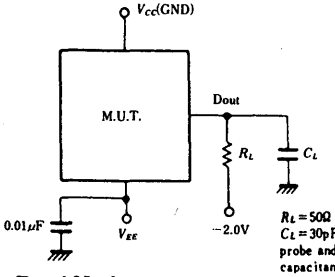
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output Rise Time	tr	—	2	—	ns	
Output Fall Time	tf	—	2	—	ns	

Capacitance

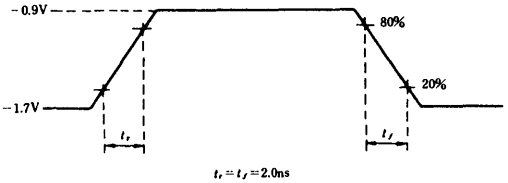
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

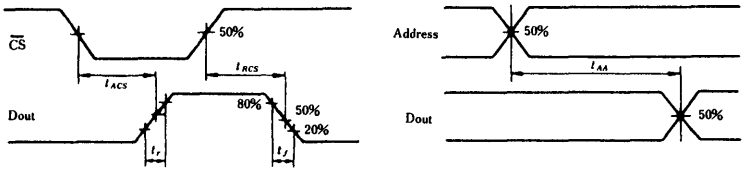
Loading Condition



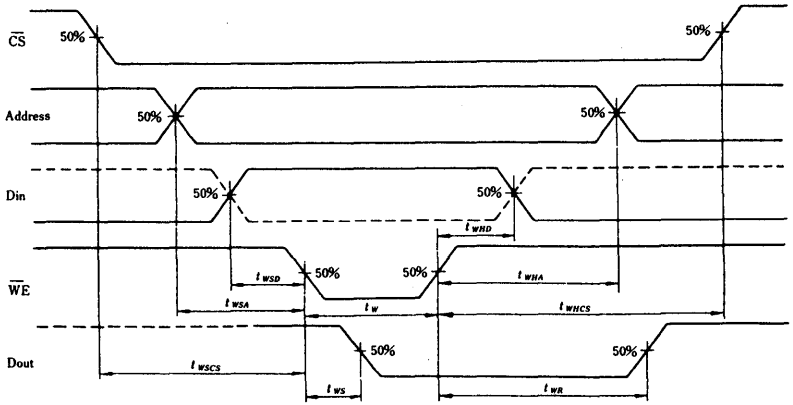
Input Pulse



Read Mode



Write Mode



HM101494 Series — Preliminary

16384-Words × 4-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

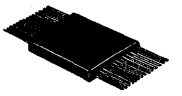
The HM101494 is ECL 100K compatible, 16384-words by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

■ FEATURES

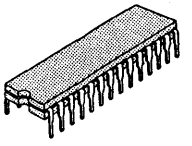
- 16384 × 4 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time .....10/12ns (max.)
- Write Pulse Width .....6/8ns (min.)
- Low Power Dissipation .....750mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM101494-10 HM101494-12	10ns 12ns	400 mil 28 pin Cerdip (DG-28N)
HM101494F-10 HM101494F-12	10ns 12ns	28 pin Ceramic Flat (FG-28D)

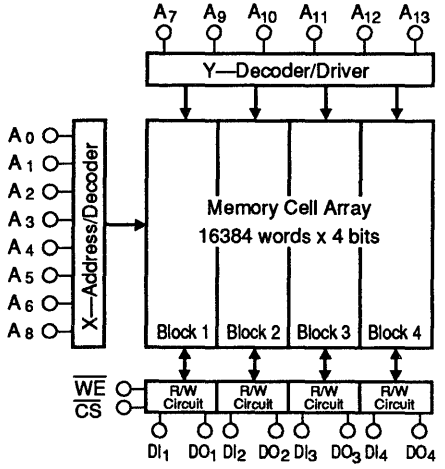


(FG-28D)

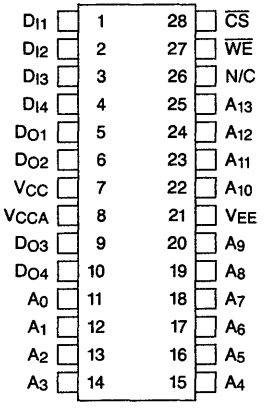


(DG-28N)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(bias)}$(1)	Θ55 to +125	°C

NOTES: 1. Under bias.
2. Ceramic flat . . . T_C, Cerdip . . . T_a.

■ ELECTRICAL CHARACTERISTICS

• **DC Characteristics** (V_{EE} = -5.2V, R_L = 50Ω to -2.0V(2), T_a = 0 to +85°C, air flow exceeding 2m/sec.(2), T_C = 0 to +85°C)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		Θ1025	Θ955	Θ880	mV
	V_{OL}			Θ1810	Θ1715	Θ1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		Θ1035	—	—	mV
	V_{OLC}			—	—	Θ1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		Θ1165	—	Θ880	mV
	V_{IL}			Θ1810	—	Θ1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	Θ50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		Θ180	—	—	mA

• **AC Characteristics** (V_{EE} = -5.2V ± 5%(2), T_a = 0 to +85°C, air flow exceeding 2m/sec.(2), T_C = 0 to +85°C)

1. Read Mode

Item	Symbol	Test Condition	HM101494-10			HM101494-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	8	ns
Address Access Time	t_{AA}		—	—	10	—	—	12	ns

2. Write Mode

Item	Symbol	Test Condition	HM101494-10			HM101494-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Write Pulse Width	t_W	t_{WSA} = t_{WSA} min.	6	—	—	8	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = t_W min.	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	12	—	—	14	ns

3. Rise/Fall Time

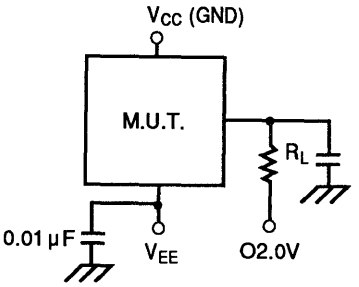
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

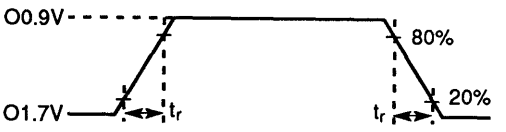
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}	$\overline{WE}$, $\overline{CS}$, D_{I1}, D_{I2}	—	5	—	pF
		Others	—	3	—	pF
Output Capacitance	C_{out}		—	3	—	pF

■ TEST CIRCUIT AND WAVEFORMS

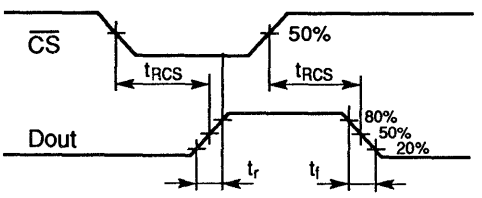
1. Loading Condition

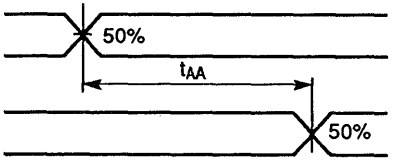


2. Input Pulse

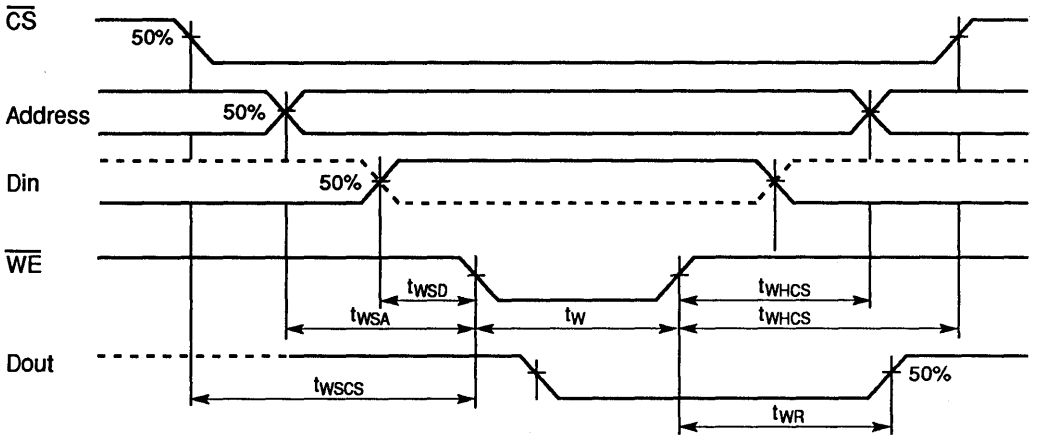


3. Read Mode





4. Write Mode


CS
Address
Din
WE
Dout
50%
50%
50%
50%
tWSD
tWSA
tW
tWHCS
tWHCS
tWSCS
tWR

HM101490 Series — Preliminary

65536-Words × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

The HM101490 is ECL 100K compatible, 65536-words by 1-bit read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

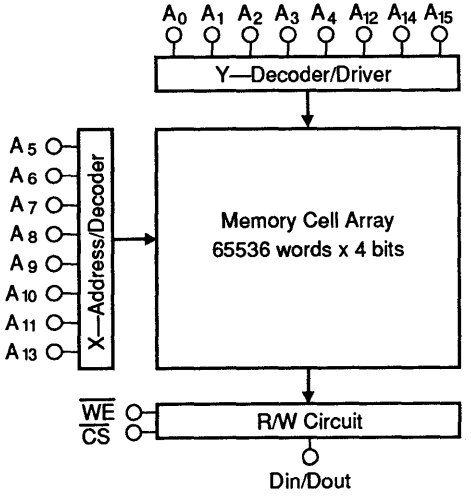
■ FEATURES

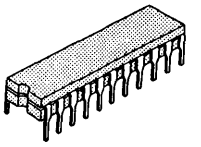
- 65536 × 1 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time .....10/12ns (max.)
- Write Pulse Width .....6/8ns (min.)
- Low Power Dissipation .....570mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HM101490-10 HM101490-12	10ns 12ns	300 mil 22 pin Cerdip (DG-22N)

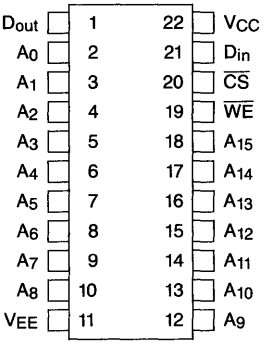
■ BLOCK DIAGRAM





(DG-22N)

■ PIN ARRANGEMENT



(Top View)

■ FUNCTION TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to Θ3.0	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(under\ bias)}$	Θ55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• **DC Characteristics** (V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_a = 0 to +85°C, air flow exceeding 2m/sec.)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		Θ1025	Θ955	Θ880	mV
	V_{OL}			Θ1810	Θ1715	Θ1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		Θ1035	—	—	mV
	V_{OLC}			—	—	Θ1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		Θ1165	—	Θ880	mV
	V_{IL}			Θ1810	—	Θ1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	Θ50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		Θ140	—	—	mA

• **AC Characteristics** (V_{EE} = -5.2V ± 5%, T_a = 0 to +85°C, air flow exceeding 2m/sec.)

1. Read Mode

Item	Symbol	Test Condition	HM101490-10			HM101490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	8	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	8	ns
Address Access Time	t_{AA}		—	—	10	—	—	12	ns

2. Write Mode

Item	Symbol	Test Condition	HM101490-10			HM101490-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Write Pulse Width	t_W	t_{WSA} = t_{WSA} min.	6	—	—	8	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	t_W = t_W min.	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	8	ns
Write Recovery Time	t_{WR}		—	—	12	—	—	14	ns

3. Rise/Fall Time

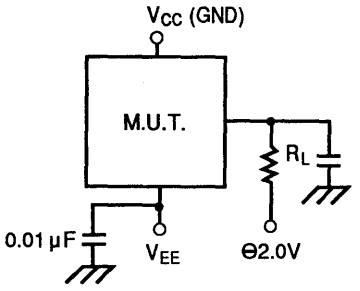
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

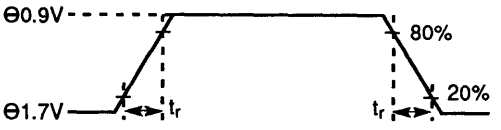
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

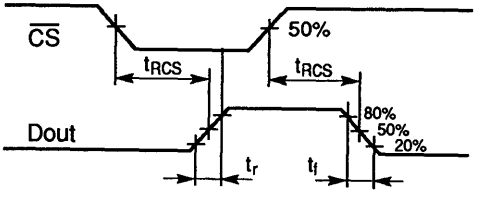
1. Loading Condition

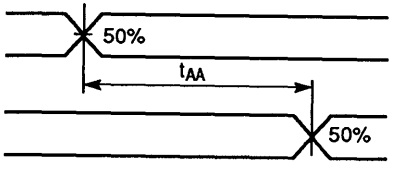


2. Input Pulse

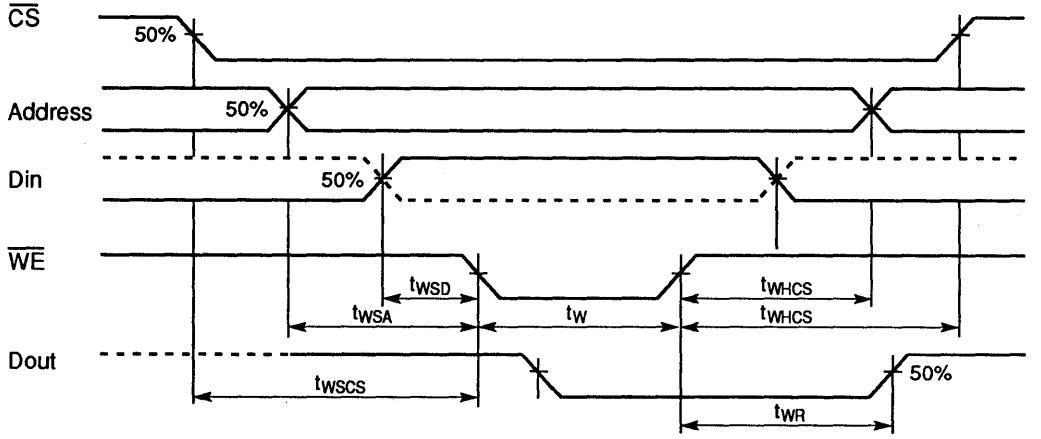


3. Read Mode





4. Write Mode


CS
Address
Din
WE
Dout
50%
50%
50%
50%
tWSD
tWSA
tW
tWHCS
tWHCS
tWSCS
tWR

HM101504F-10/12 — Preliminary

65536-Words × 4-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

The HM101504 is ECL 100K compatible, 65536-words by 4-bits read/write random access memory developed for high speed systems such as scratch pads and control/buffer storage.

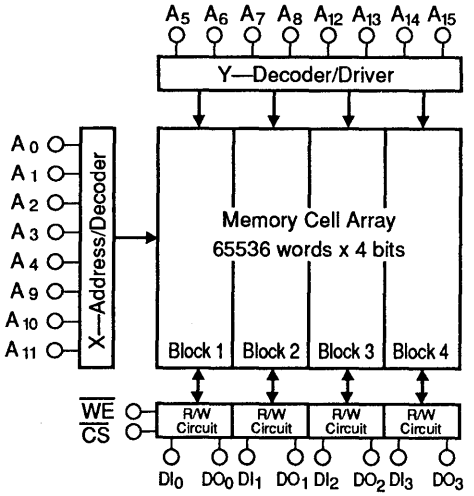
■ FEATURES

- 65536 × 4 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time . . . . . .10/12ns (max.)
- Write Pulse Width . . . . . .8ns (min.)
- Low Power Dissipation . . . . . .500mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

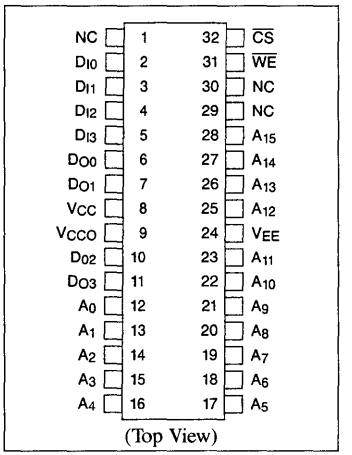
■ ORDERING INFORMATION

Type No.	Access Time	Package
HM101504F-10	10 ns	(TBD)
HM101504F-12	12 ns	

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ TRUTH TABLE

Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

NOTES: X = Irrelevant;
* = Read out noninvert

HM101500F-15 — Preliminary

262144-Words × 1-Bit Fully Decoded Random Access Memory

■ DESCRIPTION

HM101500F-15 is ECL 100K compatible, 262144-words by 1-bit, read/write random access memory developed for high speed systems such as main memories for super computers.

■ FEATURES

- 262,144-Words × 1 Bit Organization
- Fully Compatible with 100K ECL Level
- Address Access Time. . . . . .15ns (max.)
- Write Pulse Width . . . . . .10ns (min.)
- Low Power Dissipation . . . . . .500mW (typ.)
- Output Obtainable by Wired-OR (Open Emitter)

■ TRUTH TABLE

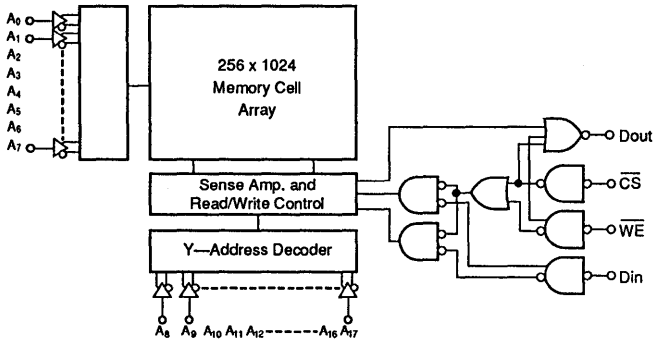
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{in}		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{out}*	Read

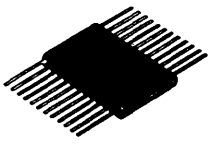
NOTES: X = Irrelevant;
* = Read out noninvert

■ ORDERING INFORMATION

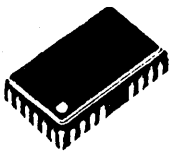
Type No.	Access Time	Package
HM101500F-15	15 ns	24 pin Ceramic Flat
HM101500CG-15	15 ns	28 pin Ceramic LCC

■ BLOCK DIAGRAM



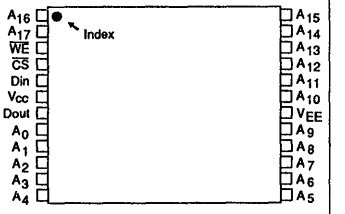


(FG-24A)

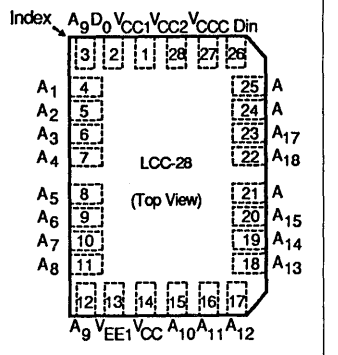


(CG-28B)

■ PIN ARRANGEMENT



(Top View)



(Top View)

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■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to Θ7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	Θ30	mA
Storage Temperature	T_{stg}	Θ65 to +150	°C
Storage Temperature	$T_{stg(bias)}$*	Θ55 to +125	°C

■ ELECTRICAL CHARACTERISTICS

• **DC Characteristics** (V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_C = 0 to +85°C)

Item	Symbol	Test Condition		Min.(B)	Typ.	Max.(A)	Unit
Output Voltage	V_{OH}	V_{in} = V_{IHA} or V_{ILB}		Θ1025	Θ955	Θ880	mV
	V_{OL}			Θ1810	Θ1715	Θ1620	mV
Output Threshold Voltage	V_{OHC}	V_{in} = V_{IHB} or V_{ILA}		Θ1035	—	—	mV
	V_{OLC}			—	—	Θ1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs		Θ1165	—	Θ880	mV
	V_{IL}			Θ1810	—	Θ1475	mV
Input Current	I_{IH}	V_{in} = V_{IHA}		—	—	220	μA
	I_{IL}	V_{in} = V_{ILB}	$\overline{CS}$	0.5	—	170	μA
			Others	Θ50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open		Θ200	—	—	mA

• **AC Characteristics** (V_{EE} = -5.2V ± 5%, T_C = 0 to +85°C)

1. Read Mode

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Chip Select Access Time	t_{ACS}		—	—	15	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	—	15	ns

2. Write Mode

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Write Pulse Width	t_W	t_{WSA} = 2ns	10	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		3	—	—	ns
Address Setup Time	t_{WSA}	t_W = 10ns	2	—	—	ns
Address Hold Time	t_{WHA}		3	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		3	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	18	

3. Rise/Fall Time

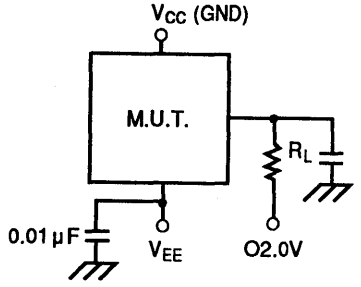
Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. Capacitance

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

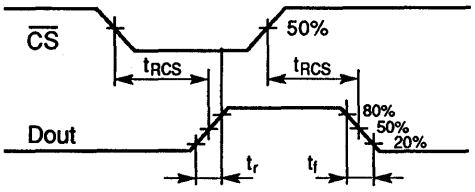
■ TEST CIRCUIT AND WAVEFORMS

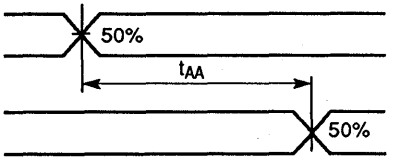
1. Loading Condition



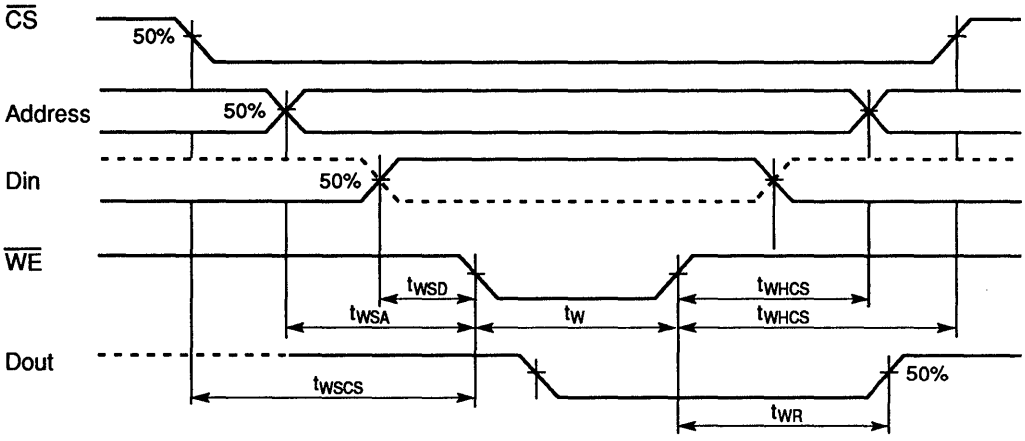
2. Input Pulse

3. Read Mode





4. Write Mode


CS
Address
Din
WE
Dout
50%
50%
50%
50%
tWSD
tWSA
tW
tWHCS
tWHCS
tWSCS
tWR

NOTES

NOTES

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10M March, 1990 Printed in U.S.A.