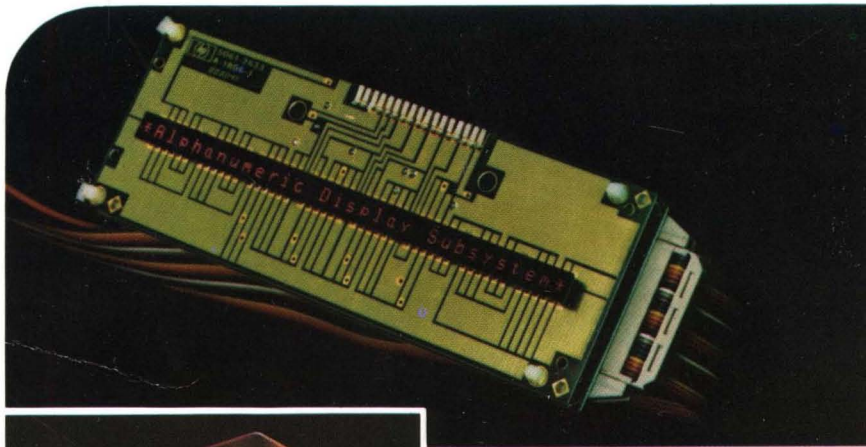
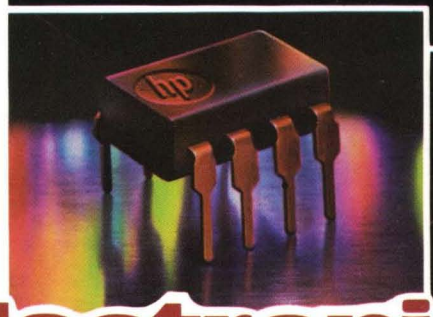
HEWLETT hp PACKARD

COMPONENTS





Optoelectronics Designer's Catalog 1979

Intensive solid state research, the development of advanced manufacturing techniques and continued expansion has enabled Hewlett-Packard to become a high volume supplier of quality, competitively priced LED displays, LED lamps, optocouplers, fiber optics, and emitters/detectors.

In addition to our broad product line, Hewlett-Packard also offers the following services: immediate delivery from any of our authorized stocking distributors, applications support, special QA testing, and a one year guarantee on all of our optoelectronic products.

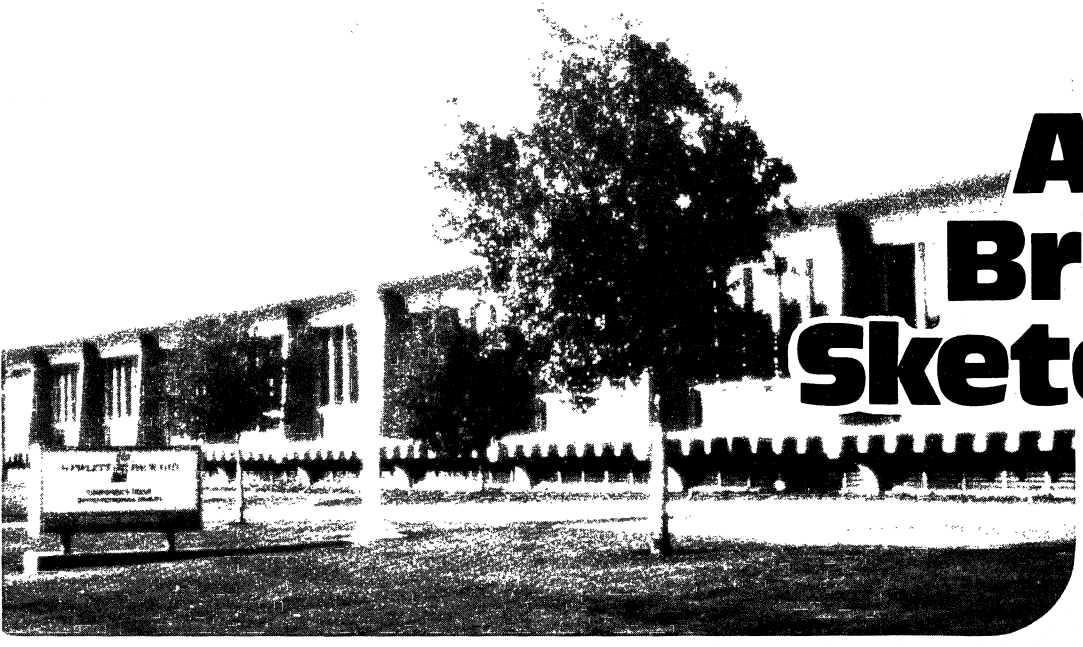
This package of products and services has enabled Hewlett-Packard to become a recognized leader in the optoelectronic industry.

Optoelectronics Designer's Catalog 1979

Hewlett-Packard is one of the world's leading designers and manufacturers of electronic, medical, analytical, and computing instruments and systems, diodes, transistors, and optoelectronic products. Since its founding in Palo Alto, California, in 1939, HP has done its best to offer only products that represent significant technological advancements.

To maintain its leadership in instrument and component technology, Hewlett-Packard invests heavily in new product development. Research and development expenditures traditionally average about 10 percent of sales revenue, and over 1,500 engineers and scientists are assigned the responsibilities of carrying out the company's various R and D projects.

HP produces more than 4,000 products at 32 domestic divisions in California, Colorado, Oregon, Idaho, Massachusetts, New Jersey and Pennsylvania and at overseas plants located in the German Federal Republic, Scotland, France, Japan, Singapore, Malaysia and Brazil.



A Brief Sketch

However, for the customer, Hewlett-Packard is no further away than the nearest telephone. Hewlett-Packard currently has sales and service offices located around the world.

These field offices are staffed by trained engineers, each of whom has the primary responsibility of providing technical assistance and data to customers. A vast communications network has been established to link each field office with the factories and with corporate offices. No matter what the product or the request, a customer can be accommodated by a single contact with the company.

Hewlett-Packard is guided by a set of written objectives. One of these is "to provide products and services of the greatest possible value to our customers". Through application of advanced technology, efficient manufacturing, and imaginative marketing, it is the customer that the more than 43,000 Hewlett-Packard people strive to serve. Every effort is made to anticipate the customer's needs, to provide the customer with products that will enable more efficient operation, to offer the kind of service and reliability that will merit the customer's highest confidence, and to provide all of this at a reasonable price.

To better serve its many customers' broad spectrum of technological needs, Hewlett-Packard publishes several catalogs. Among these are:

- Electronic Instruments and Systems for Measurement/Computation (General Catalog)
- DC Power Supply Catalog
- Medical Instrumentation Catalog
- Analytical Instruments for Chemistry Catalog
- Coax, and W/G Measurement Accessories Catalog
- Diode and Transistor Catalog

All catalogs are available at no charge from your local HP sales office.

Where Reputation and Quality Count

When quality represents a competitive edge, or when the reputation and dependability of your products is on the line, you can count on Hewlett-Packard Optoelectronic components for excellent product consistency.

The optoelectronic products available include a complete line of GaAsP and GaP discrete light emitting diodes (LED's), numeric, hexadecimal, and alphanumeric displays, optocouplers, fiber optics, and emitters/detectors. For a general overview of the products available, the next seven pages will include highlights of the discrete product family groups. There is complete technical data included in this designer's catalog for each of the Hewlett-Packard Optoelectronic products.

Fiber Optics!

Fiber Optics (Page 2)

The Data Link of the Future is Available from HP Today!

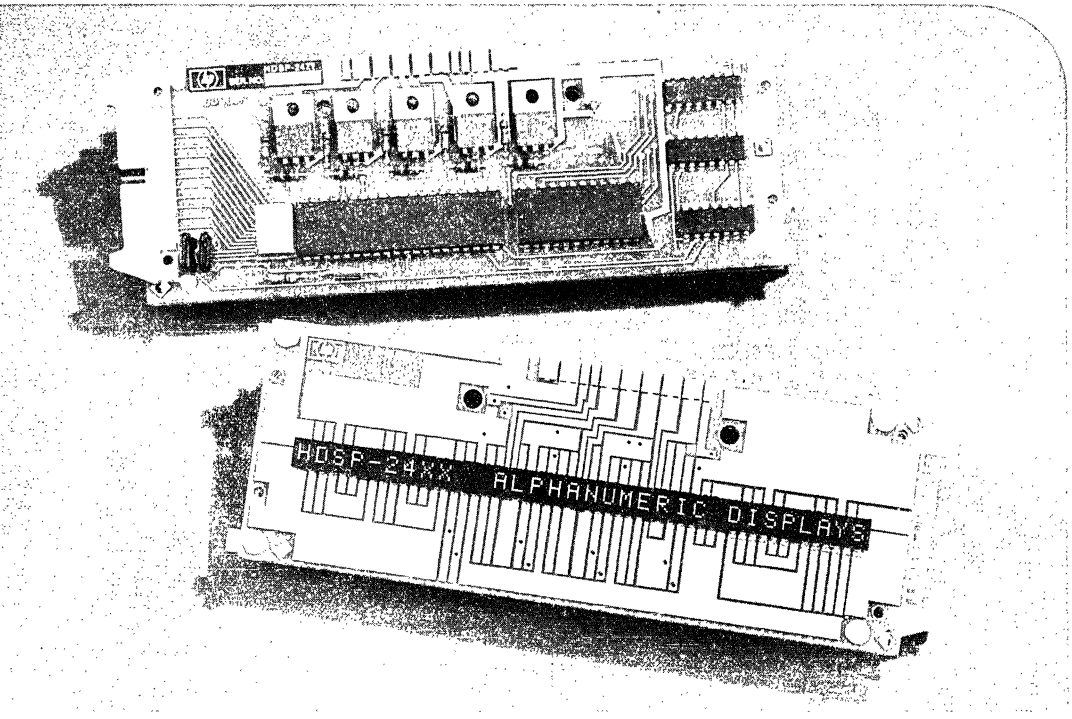
In 1978, Hewlett-Packard introduced its first complete fiber optic system. Fiber optics is one of the most exciting and fastest growing technologies in data transmission. With fiber optics, pulses of light travel down hair-thin fibers replacing electrical signals transmitted over copper wire. The light signals are impervious to electrical or magnetic interference and therefore generate no electrical or magnetic noise. This makes them ideal for linking computers or control devices and their peripherals in different environments such as those found in factories, aircraft, hospitals and large power plants.

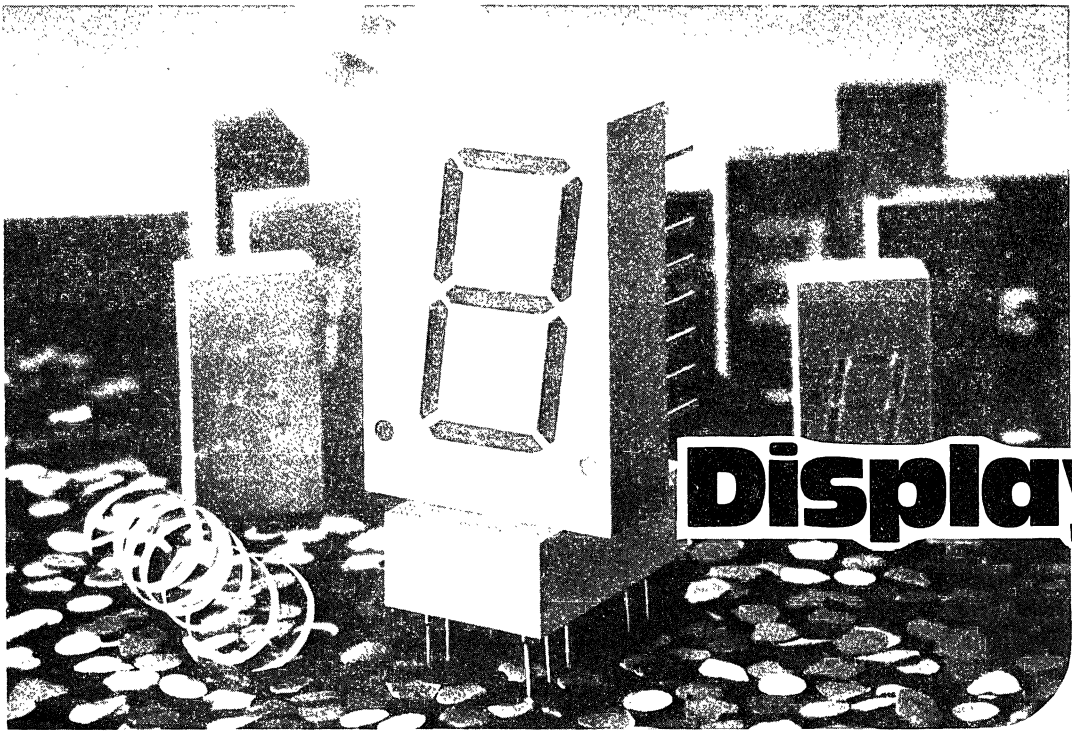
As shown in the photograph on the left, a fiber optic system consists of a transmitter, a receiver, and a length of cable encasing the hair-thin glass or plastic fiber that carries optical signals.

Currently, Hewlett-Packard's fiber optic system is capable of receiving signals from distances up to 100 metres, and in the near future will be able to include distances as far as one kilometer.

The design of cost effective fiber optic systems requires the understanding and analysis of several complex technologies — optical fibers, precision connectors, LED/laser emitters, photodetectors, circuit design, packaging, and optics. Hewlett-Packard's approach to the design of fiber optic hardware is systems oriented, drawing on the broad base of technologies available within our computer, instrumentation, semiconductor components, and corporate research and development activities. State-of-the-art LED, photodetector, and integrated circuit capability are at the heart of HP's fiber optic systems. Beginning on page 2 of this catalog, you will find further details on Hewlett-Packard's fiber optic systems.

Alphanumeric Display Subsystem (Page 102)





Displays!

20mm (0.8") Display (page 21)

HP's First Stand-Alone Alphanumeric Display System is Here!

Hewlett-Packard has expanded its selection of both alphanumeric and seven-segment numeric displays to satisfy an even broader base of applications.

Hewlett-Packard's completely supported alphanumeric display system, shown in photograph on the left, allows freedom from costly display maintenance, requires very low operating power, and minimizes the interaction normally required for alphanumeric displays. The display system is TTL compatible, requires a single 5V supply, and easily interfaces to a keyboard or microprocessor. It is ideally suited for word processing equipment, instrumentation, desktop calculators, and automatic banking terminal applications.

Hewlett-Packard's new yellow alphanumeric display is the answer to applications that require small size and prohibit the use of red displays. Both red and yellow alphanumeric displays feature four 5 x 7 dot matrix characters and on-board shift registers for data storage. They are contained in 16-pin DIPs which are end-stackable for unlimited possibilities in alphanumeric display formatting.

Available in four- and eight-character end-stackable modules are Hewlett-Packard's 18-segment solid state LED alphanumeric displays. Magnification of the LED by an integral lens results in a character size of 3.8mm (0.15 in.) making these displays ideal for use in computer peripheral products, automotive instrument panels, calculators, and electronic instruments and systems requiring low power consumption.

Low cost numeric displays, packaged single or clustered, are available in character heights from .11" to .8". Low power small character displays have been designed for portable instrumentation and calculator applications. Other seven-segment display units are available in red, yellow, and green colors for use in instrumentation, point of sale terminals, and TV indicator applications. High power, sun-light viewable, large character displays are readily adapted to outdoor terminals, gas pumps and agricultural instrumentation. For these displays, Hewlett-Packard has successfully integrated a gray package design with untinted segments. This results in excellent bright ambient contrast enhancement.

Integrated numeric and hexadecimal displays (with on-board IC's), available in plastic and hermetic packages, solve the designer's decoding/driving problem. These displays have been designed for low cost and ease of application in a wide range of environments.

Brighten-Up Your Message with Light Bars!

Light Bar Modules are Hewlett-Packard's answer to the problem of how to effectively backlight legends. The Light Bar's large, uniformly illuminated surface provides a bright light source available in either high efficiency red, yellow, or green. The universal pinout arrangement allows connecting in parallel, series, or series/parallel configurations. Hewlett-Packard's Light Bar Modules come in two sizes, are X-Y stackable, and flush mounting is easy and convenient.

Besides the new Light Bar Modules, Hewlett-Packard LED lamps are available in a wide variety of plastic and hermetic packages to satisfy almost any application. Many styles can be mounted on a front panel using clips and all are suitable for P.C. board mounting. Hewlett-Packard military screened hermetic lamps are very popular in applications demanding hi-reliability.

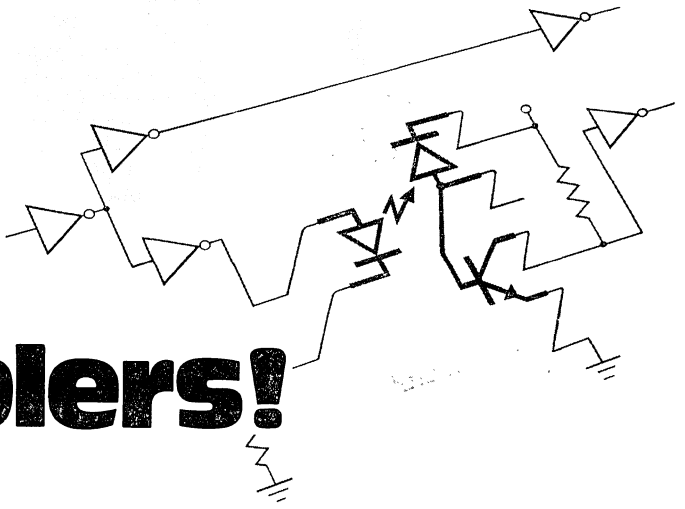
Products with wide or narrow viewing angles, and a range of brightnesses, are available in red, high efficiency red, yellow and green. Package styles include the traditional T-1-3/4, T-1, and TO-18 packages, as well as our own subminiature (stackable on 2.54mm [0.100 in.] centers), rectangular, and panel mountable hermetic packages.

Lamps!

Light Bar Modules (Page 131)

☑ High Speed
☑ Low Input Current/High Gain
☑ High Reliability

Hewlett-Packard's family of optocouplers provide economical, high performance solutions to problems caused by ground loops and induced common mode noise for both analog and digital applications in commercial, industrial, and military products. Hewlett-Packard's original approach toward integrated output detectors provides performance not found in conventional phototransistor output optocouplers. With 3000 VDC isolation, the types of optocouplers available include high speed devices capable of 10M bits and high gain devices which are specified at 400% CTR at input currents as low as 0.5mA. In addition, highly linear optocouplers are useful in analog applications, and a Hewlett-Packard integrated input optically coupled line receiver can be connected directly to twisted pair wires without additional circuitry. Most of these devices are available in dual versions, as well as in hermetic DIP packages. For military users, Hewlett-Packard's established hi-rel capability facilitates economical, hi-rel purchases.



Optocouplers!

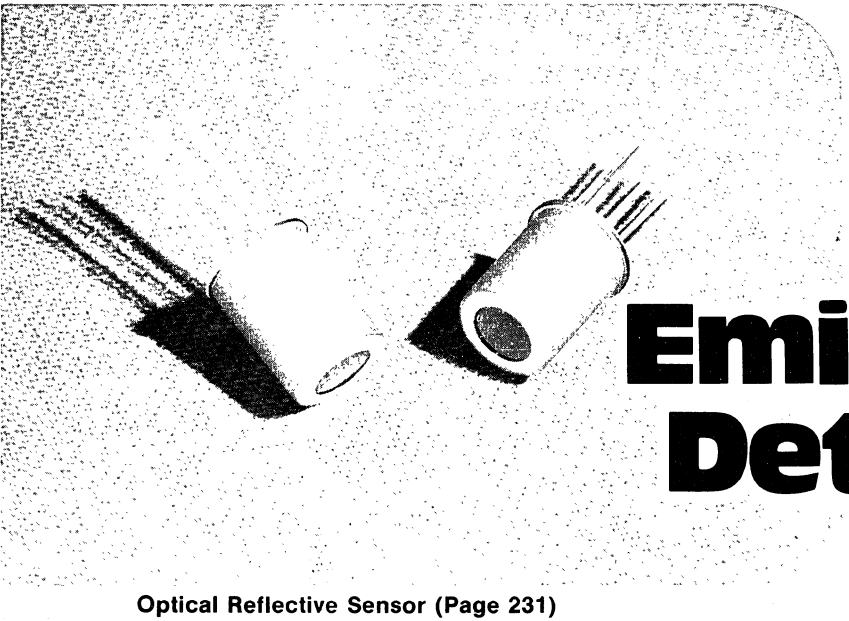
High-Speed Optocoupler (Page 194)

High Resolution Sensing!

As the growing trend continues for microprocessor systems capable of high-resolution-mechanical to electronic-interfaces, Hewlett-Packard addresses a genuine unfulfilled need with their new optical sensor. This small, self-contained optical reflective sensor (shown in photo below) combines a light source and detector with focused optics in a single package. This unique component can detect an object as fine as a human hair as well as the precise edge of large objects such as paper or printed lines and marks. It therefore becomes ideally suited in such applications as pattern recognition, optical limit switching, tachometry, defect detection, and bar code scanning.

In addition to the complete emitter/detector system described in the optical scanner, Hewlett-Packard also offers the designer the choice of discrete emitter and detector components. High radiant intensity emitters near infrared in both floodlight and spotlight configurations are ideally suited for use in optical transducers and encoders, smoke detectors, and fiber optic drivers.

Hewlett-Packard PIN photodiodes are excellent light detectors with an exceptionally fast response of 1ns, wide spectral response from near infrared to ultra-violet, and wide range linearity (constant efficiency over 6 decades of amplitude). With dark current as low as 250pA at 10V, these detectors are especially well-suited for operation at low light levels. The device construction allows high speed operation at reverse voltages of 5 volts. Some applications include fiber optic receivers, laser scanners, range finders, and medical diagnostic equipment. High reliability test programs are also available.



Emitters/ Detectors

Optical Reflective Sensor (Page 231)

This Optoelectronics Designer's Catalog contains detailed, up-to-date specifications on our complete optoelectronic product line. It is divided into five major product sections: Fiber Optics, Displays, Lamps, Optocouplers, and Emitters/Detectors. A special section which includes all of the latest application notes in full-length version follows the Emitters/Detectors product section. Hewlett-Packard Sales and Service Offices are listed on pages 363-366 and the Hewlett-Packard Components Franchised Distributors and Representatives Directory can be found on pages 360-362.

How To Use This Catalog

Three methods are incorporated for locating components:

- a Table of Contents with tabs that allows you to locate components by their general description.
- a Numeric Index that lists all components by part number, and
- a Selection Guide for each product group giving a brief overview of the product line.

How To Order

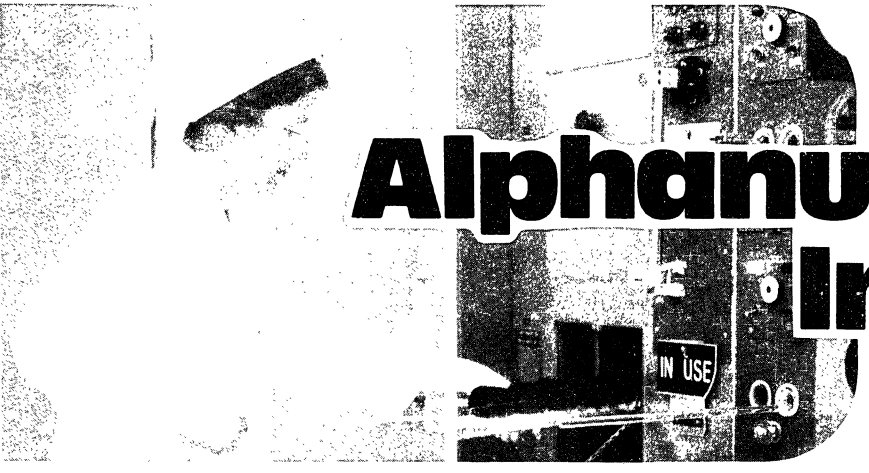
All Hewlett-Packard components may be ordered through any of the Sales and Service Offices listed on pages 363-366. In addition, for immediate delivery of Hewlett-Packard optoelectronic components, contact any of the world-wide stocking distributors and representatives listed on pages 360-362.

Warranty

HP's Components are warranted against defects in material and workmanship for a period of one year from the date of shipment. HP will repair or, at its option, replace Components that prove to be defective in material or workmanship under proper use during the warranty period. This warranty extends only to HP customers.

No other warranties are expressed or implied, including but not limited to, the implied warranties or merchantability and fitness for a particular purpose. HP is not liable for consequential damages.

Table of Contents



Alphanumeric Index

Alphanumeric Index (Continued)

NOTES:
1. EIA Registered. (Part no. changed)
2. Part no. changed.
*New product.

Fiber Optics

Optoelectronics Designer's Catalog 1979

Fiber Optics!

Fiber optics is emerging as a practical, cost-effective technology for data communications. Pulses of light traveling down hair-thin fibers are replacing electrical signals transmitted over copper wires. The transmission of information over optical cables offers many features, advantages, and benefits, some not available with any other technology:

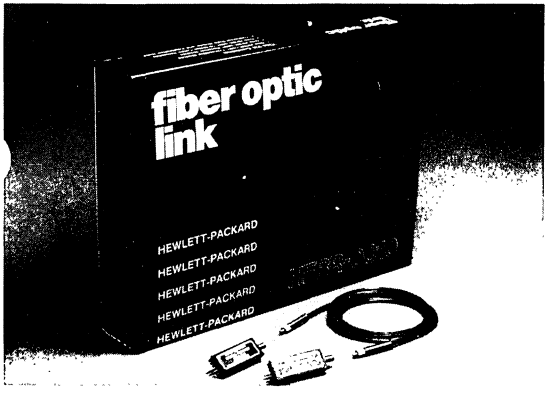
• Features	• Advantages	• Benefits
Optical transmission path	Complete input-output electrical isolation	Freedom from ground loops. Lightning safe.
Light pulse "carrier" signals	No EMI susceptibility or radiation	Freedom from induced noise. Freedom from crosstalk. Secure communications.
	Very high distance/bandwidth products achievable	Greater data rates at longer distances than wire/coax.
Bandwidth independent of cable size	Light weight, small diameter cables possible	Lower cost installation and maintenance. More bandwidth (channels) per unit area or unit weight.

Versatile

HP's new fiber optic systems are point-to-point links intended for short to intermediate distance processor-to-processor or processor-to-peripheral interconnection in commercial, industrial, or military applications. Some of these are:

- **Large computer installations**
- **Distributed processing (minicomputer) systems**
- **Hospital computer systems**
- **Power plant communications/control**
- **Industrial/process control**
- **Industrial or military secure communications**
- **Aircraft/shipboard data links**
- **High voltage or electromagnetic field research**
- **Remote instrumentation systems**
- **Factory data collection**

In many of these applications induced noise, ground potential differences, high voltage, or extended distance, make twisted wire or coaxial data links difficult or impossible to use. Fiber optics can offer an alternative to expensive shielding, conduit, isolation transformers, or data error checking and retransmission circuitry.



System Specifications*

DATA RATE:	DC to 10Mb/s NRZ
DATA FORMAT:	No restrictions
LINK DISTANCE:	0 to 100 metres
BIT ERROR RATE:	10^{-9} max. at 10Mb/s NRZ
DATA INPUT:	TTL compatible (1 LSTTL load)
DATA OUTPUT:	TTL compatible (up to 20 LSTTL loads)
CABLE CONSTRUCTION:	Reinforced, polyurethane jacketed, single fiber, glass core and cladding.
POWER SUPPLY REQUIREMENTS	
TRANSMITTER:	5V±5% at 125mA
RECEIVER:	5V±5% at 100mA
OPERATING TEMPERATURE RANGE:	0°C to 70°C

*Detailed electrical and mechanical specifications are contained in the following data sheets: HFBR-1001, HFBR-2001, HFBR-3001 to -3005.

Easy-To-Use

The HP Fiber Optic Link is a versatile, easy-to-use system. It does not require optical design expertise, calibration or adjustment.

To make it easy to get started, HP offers the HFBR-0010, a complete 10 metre simplex link consisting of a transmitter, a receiver, a 10 metre connector/cable assembly, and technical literature. Also available are separate components: the HFBR-1001 100 metre digital transmitter, the HFBR-2001 digital receiver, and the HFBR-3001 through -3005 connector/cable assemblies in five standard lengths: 10, 25, 50, 75, and 100 metres.

HP systems feature:

- **Compatible plug-together transmitters, receivers, and cable assemblies**
- **Miniature PC board mountable packages**
- **TTL electrical interfaces**
- **Single 5 volt power supply requirement**
- **Accepts any data format from DC to 10 Mbits NRZ**
- **Accommodates cable lengths up to 100 metres**
- **Integral fiber optic connectors**
- **Built-in "link monitor"**

Systems and Components

HP Part No.	Description	Page No.
HFBR-0010	Complete 10 Metre Simplex System (Contains one each HFBR-1001, -2001, -3001)	(Contact HP Sales Office)
HFBR-1001	100 Metre Digital Transmitter	4
HFBR-2001	Digital Receiver	8
	Connector/Cable Assemblies:	
HFBR-3001	10 Metre	
HFBR-3002	25 Metre	
HFBR-3003	50 Metre	12
HFBR-3004	75 Metre	
HFBR-3005	100 Metre	

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COMPONENTS

NEW PRODUCT

FIBER OPTIC 100 METRE DIGITAL TRANSMITTER

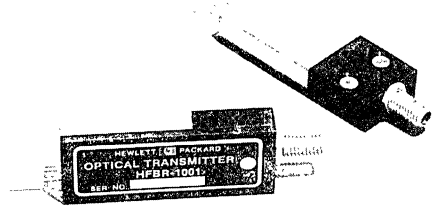
HFBR-1001

TECHNICAL DATA APRIL 1979

Features

- **HIGH SPEED: dc to 10MB/S NRZ***
- **LONG DISTANCE: 100 metres***
- **LOW PROFILE: Fits 12.7mm (0.5″) spaced card rack**
- **NO HEAT SINK REQUIRED**
- **ARBITRARY DATA FORMAT***
- **TTL INPUT LEVELS**
- **SCHMITT DATA INPUT**
- **OPTICAL PORT CONNECTOR**
- **SINGLE 5V SUPPLY**

*When used with HFBR-2001 Receiver Module and HFBR-3001 to -3005 Cable/Connector Assemblies.

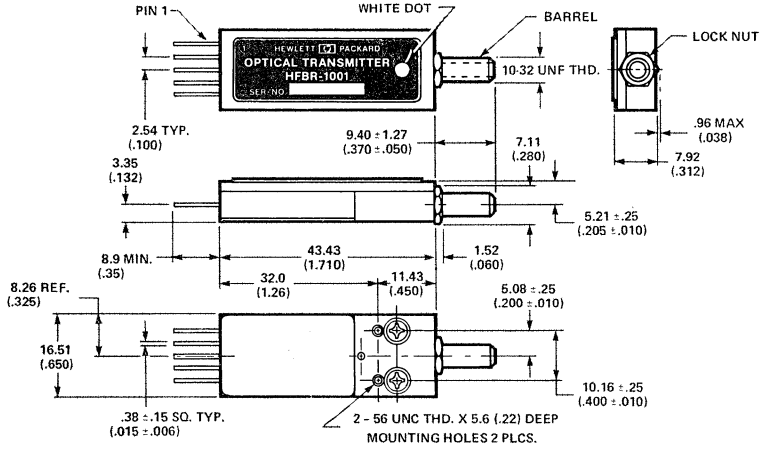


Description

The HFBR-1001 fiber optic transmitter is an integrated electrical to optical transducer designed for digital data transmission over single fiber channels. A bipolar integrated circuit and a GaAsP LED convert TTL level inputs to optical pulses at data rates from dc to 10Mb/s NRZ. An integral optical connector on the module allows easy interfacing without problems of source/fiber alignment. The low profile package is designed for direct printed circuit board mounting without additional heat sinking.

The HFBR-1001 is intended for use with HFBR-3001 to-3005 fiber optic cable/connector assemblies, and the HFBR-2001 fiber optic receiver for transmission distances up to 100 metres. The HFBR-1001 generates optical signals in either of two externally selectable modes. The internally-coded mode produces a 3-level coded optical signal for reception and decoding by the HFBR-2001 receiver. This feature provides data format independence over the data rate range of dc to 10Mb/s NRZ while allowing for wide dynamic range and high sensitivity at the receiver. The externally-coded mode produces a 2-level optical signal which is a digital replica of the data input waveform. Used in this mode with the HFBR-2001 receiver, the user must provide proper data formatting (explained in the HFBR-2001 data sheet) to insure proper receiver operation. In either mode, the radiant output is radiologically safe (per ANSI Z136.1-1976).

Package Dimensions



CAUTION:

1. LOCK NUT AND BARREL SHOULD NOT BE DISTURBED.
2. SCREWS ENTERING THE 2-56 THREADED MOUNTING HOLES MUST NOT TOUCH BOTTOM.
3. THE HFBR-3001 TO -3005 CONNECTOR SHOULD NOT BE TIGHTENED BEYOND THE LIMITS SPECIFIED IN THE HFBR-3001 TO -3005 DATA SHEET.

PIN	FUNCTION
1	MODE SELECT
2	N.C.
3	GROUND
4	V_{CC}
5	DATA INPUT

NOTES:

1. DIMENSIONS IN mm (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38mm (±.015″)

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units	Note
Storage Temperature		T_S	-55	+85	°C	
Operating Temperature		T_A	0	70	°C	
Lead Soldering	Temperature			260	°C	3
	Time			10	s	
Supply Voltage		V_{CC}	-0.5	6	V	
Mode Select or Data Input Voltage		V_I	-0.5	5.5	V	

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units	Note
Ambient Temperature	T_A	0	70	°C	
Supply Voltage	V_{CC}	4.75	5.25	V	4
High Level Input Voltage, Mode Select or Data Input	V_{IH}	2.0	V_{CC}	V	
Low Level Input Voltage, Mode Select or Data Input	V_{IL}	0	0.8	V	
Data Input Voltage Pulse Duration (high or low)	t_H, t_L	100		ns	

Electrical/Optical Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter		Symbol	Min	Typ(6)	Max	Units	Conditions		Fig.	Note
High Level Input Current	Mode Select	I_{IH}			100	μA	V_{CC} = 5.25V, V_I = 2.4V		2	
	Data Input				20					
Low Level Input Current	Mode Select	I_{IL}			-1.6	mA	V_{CC} = 5.25V, V_I = 0.4V			
	Data Input				-0.6					
Supply Current	Externally-Coded Mode	I_{CC}			170	mA	Mode Select High	Data Input High, V_{CC} = 5.25V	1, 2	5
			40					Data Input Low, V_{CC} = 4.75V		
	Internally-Coded Mode		68	95	125		Mode Select Low	Data Input High or Low, V_{CC} = 5.25V		
Optical Flux	High Level	ϕ_H		67		μW	Mode Select High	Data Input High	1, 2, 3	
	Low Level	ϕ_L		3				Data Input Low		
	Mid Level (average)	ϕ_M		35			Mode Select Low	Data Input Square Wave at 500 kHz		
	Excursion $\left(\frac{\text{peak-to-peak}}{2}\right)$	$\Delta\phi$	22	32			Mode Select High			9
Amplitude Symmetry, Flux Excursion Ratio		k	0.8		1.2	—	Mode Select Low		1	7
Exit Numerical Aperture		N.A.		0.5		—			3	
Optical Port (fiber optic core) Diam.		D_C		200		μm				
Coupling Loss	from area mismatch	α_A		6.0		dB	with HFBR-3001 to -3005 Cable and Connector Assembly			
	from numerical aperture mismatch	$\alpha_{N.A.}$		4.0						
Peak Emission Wavelength		λ_P		700		nm			4	

Dynamic Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter		Symbol	Min	Typ(6)	Max	Units	Conditions	Fig.	Note
Propagation Delay	High-to-Low Data Input Voltage Step	t_{PHL}		31	45	ns	V_{CC} = 4.75 V	1	8
	Low-to-High Data Input Voltage Step	t_{PLH}		35	50	ns			
Refresh Pulse Internally-Coded Mode	Duration	t_p		60		ns	V_{CC} = 5.00 V, Mode Select Low	1	8
	Repetition Rate	f_R		300		kHz			

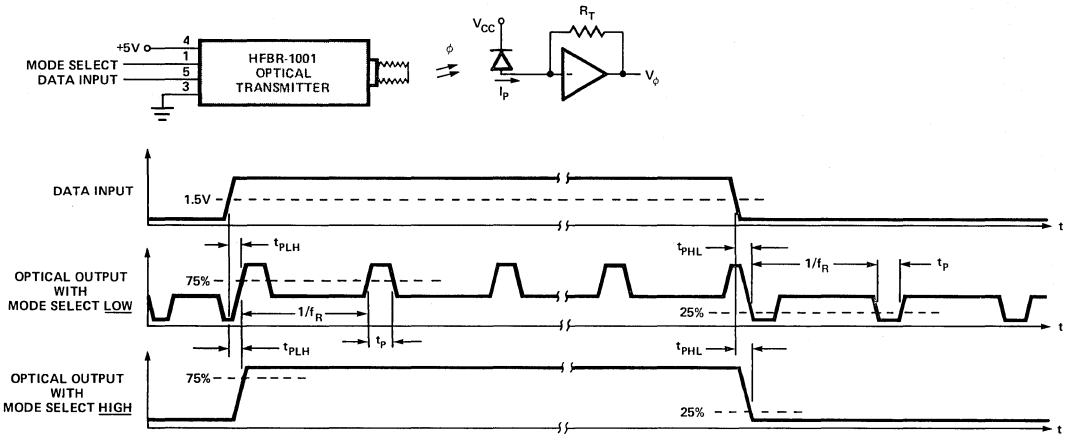


Figure 1. Flux Coding and Timing Diagram.

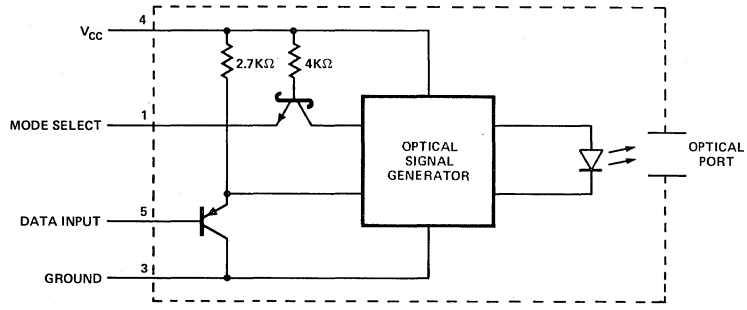


Figure 2. Schematic Diagram.

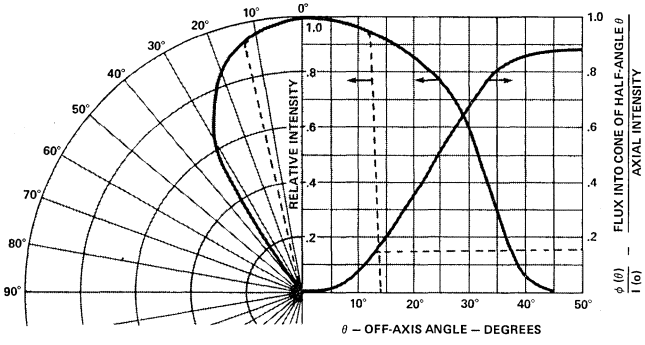


Figure 3. Radiation Pattern.*

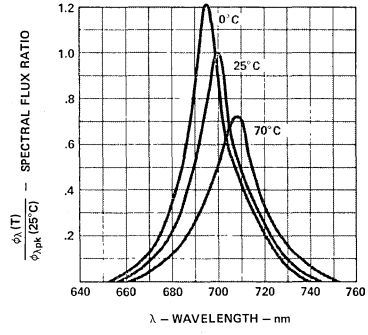


Figure 4. Emission Spectrum.

*The optical fiber is recessed within the barrel at a distance of approximately 7mm. Solid line represents radiation pattern from fiber stub without obscuration by connector barrel. Dashed line represents radiation pattern as seen from outside of connector.

Notes (cont'd):

3. Measured at a point 2mm (.079 in.) from where lead enters package.
4. A supply decoupling network of 2.2μH with 60μF is recommended.
5. Average currents for steady-state conditions at Data Input.
6. For typical values, V_{CC} = 5.00V and T_A = 25°C.
7. Flux excursion ratio, k, is the ratio of flux excursion above mid level to flux excursion below mid level. $k = \frac{\phi_H - \phi_M}{\phi_M - \phi_L}$.
8. The refresh pulse is interrupted (abbreviated) if Data Input changes state during the refresh pulse. MAX propagation delay is for Data Input changing state during the maximum excursion of the refresh pulse.
9. Flux excursion
   $\Delta\phi = 0.5\ (\phi_H - \phi_L)$, or $\Delta\phi = 0.5\ (\phi_M - \phi_L) \bullet (1+k)$.

   Notice that under the conditions specified for $\Delta\phi$, the **average** flux is $(\Delta\phi + \phi_L)$.

Electrical Description

The HFBR-1001 has two modes of operation: Internally-Coded mode and Externally-Coded mode. These are selected by making the Mode Select input "low" for Internally-Coded mode and "high" for Externally-Coded mode. With Mode Select "low," the optical signal generator in the HFBR-1001 produces a "mid-level" flux which has positive or negative excursions, depending on whether Data Input is "high" or "low." In this Internally-Coded mode, a train of positive excursions is initiated when Data Input goes "high;" when Data Input goes "low," a train of negative excursions is initiated. These excursions are pulses of approximately 60ns duration with a 300kHz repetition rate. Each initiation of a pulse train starts with a full-duration pulse, but when Data Input changes state, the train is terminated—even at mid-pulse—as a new train of opposite-polarity pulses is initiated. With this coding scheme and the low duty factor, the average flux is always near the mid-level, regardless of the data rate or duration in either state. This coding scheme is designed to operate the HFBR-2001 Fiber Optic Receiver most effectively; the mid-level flux operates the Receiver's dc-restorer and the "refresh" pulses of either polarity keep the Receiver's ALC voltage at the proper level, allowing low propagation delay for any change of state at Data Input. Since propagation delay is always the same, the Internally-Coded mode permits transmission of analog information, e.g., by means of Pulse Width Modulation. Another advantage of the 3-level Internally-Coded mode is that supply current is nearly the same for either logic state, thus reducing transients on the power supply line.

With Mode Select "high," the optical signal is at full maximum (~2 X mid level) when Data Input is "high," and nearly zero when Data Input is "low." This mode provides for these three applications:

1. Steady state turn-on of the photo-emitter at maximum flux level (e.g., for system diagnosis).
2. Stand-by mode (e.g., when the system is not in use).
3. Transmission of 2-level optical signals from externally generated code (e.g., Manchester) for receivers not configured for the 3-level code. With Mode Select "high," the output is either ϕ_H, or ϕ_L. Direct analog operation is not possible due to hysteresis in the response of the optical signal to the Data Input signal.

Mechanical and Thermal Considerations

Typical power consumption is less than 500mW so the transmitter can be mounted without consideration for external heat sinking. The optical port is an optical fiber stub centered in a metallic ferrule. This ferrule supports a split-wall cylindrical spring sleeve which aligns the ferrule in the Transmitter with the ferrule in the HFBR-3001 to-3005 Fiber Optic Connector/Cable. The connection procedure is to FIRST start the Connector ferrule into the sleeve; THEN screw the coupling ring on the barrel. The barrel performs no alignment function; its purpose is to hold the ferrule faces together when the coupling ring is tightened as specified in the HFBR-3001 to-3005 Fiber Optic Connector/Cable data sheet.

The HFBR-1001 should be mounted so that the lock nut at the optical port is not disturbed. Moving the lock nut can cause misalignment of the optical fiber stub inside the module resulting in a reduction of power output. Mounting at the edge of a printed circuit board with the lock nut overhanging the edge is recommended.

HEWLETT hp PACKARD

COMPONENTS

NEW PRODUCT

FIBER OPTIC DIGITAL RECEIVER

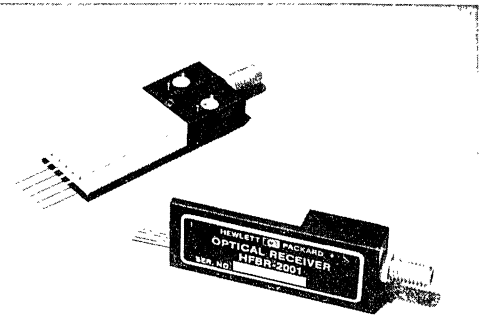
HFBR-2001

TECHNICAL DATA APRIL 1979

Features

- **HIGH SPEED: dc to 10Mb/s NRZ***
- **LOW NOISE: 10^{-9} BER with 0.8μW Input***
- **LOW PROFILE: Fits 12.7mm (0.5") spaced card rack**
- **SINGLE SUPPLY VOLTAGE**
- **WIDE OPTICAL DYNAMIC RANGE: 23dB**
- **OPTICAL PORT CONNECTOR**
- **ARBITRARY DATA FORMAT***
- **TTL OUTPUT LEVELS**
- **LINK MONITOR: Shows Satisfactory Input Signal***

*When used with HFBR-1001 Transmitter and HFBR-3001 to -3005 Cable/Connector Assemblies.



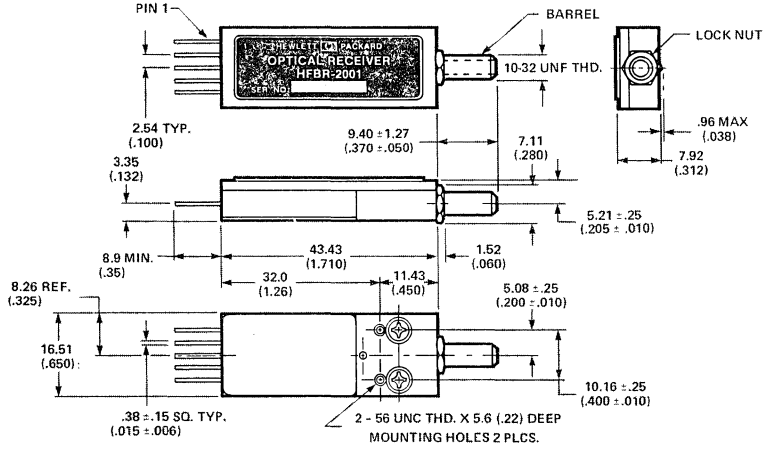
Description

HFBR-2001 fiber optic receiver is an integrated optical to electrical transducer designed for reception of digital data over single fiber channels. A silicon PIN photodetector and a bipolar integrated circuit convert optical pulses to TTL level outputs with an optical sensitivity of .8μW, a dynamic range of 23 dB, and data rates to 10 Mb/s NRZ. An integral optical connector on the module allows easy interfacing without problems of fiber/detector alignment. The low profile package is designed for direct printed circuit board mounting without additional heat sinking.

The HFBR-2001 is intended for use with HFBR-3001 to -3005 fiber optic cable/connector assemblies and the HFBR-1001 fiber optic transmitter. In order to provide wide dynamic range, dc response, and high sensitivity, the receiver must periodically extract information from the optical waveform. When operating with the HFBR-1001 transmitter in the internally-coded mode, this information is automatically provided by the transmitter. When operating in the externally-coded mode, or with another transmission source, the user must provide proper data formatting to insure proper receiver operation.

An additional TTL output called Link Monitor (LM), provides a digital indication of link continuity independent of the presence of data. Link continuity is indicated by a logical high output state.

Package Dimensions



CAUTION:

1. LOCK NUT AND BARREL SHOULD NOT BE DISTURBED.
2. SCREWS ENTERING THE 2-56 THREADED MOUNTING HOLES MUST NOT TOUCH BOTTOM.
3. THE HFBR-3001 TO -3005 CONNECTOR SHOULD NOT BE TIGHTENED BEYOND THE LIMITS SPECIFIED IN THE HFBR-3001 TO -3005 DATA SHEET.

PIN	FUNCTION
1	TEST POINT
2	LINK MONITOR
3	GROUND
4	V_{CC}
5	DATA OUTPUT

NOTES:

1. DIMENSIONS IN mm (INCHES)
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38mm (±.015")

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units	Note
Storage Temperature		T_S	-55	85	°C	
Operating Temperature		T_A	0	70	°C	
Lead Soldering Cycle	Temperature			260	°C	3
	Time			10	s	
Supply Voltage		V_{CC}	-0.5	6.0	V	
Output Voltage (High State)		V_{OH}		6.0	V	

Recommended Operating Conditions

Parameter			Symbol	Min	Max	Units	Note
Ambient Temperature			T_A	0	70	°C	
Supply Voltage			V_{CC}	4.75	5.25	V	
Supply Ripple (Peak-to-Peak)			ΔV_{CC}		250	mV	4
High Level Output Current	Link Monitor		I_{OH}		-100	µA	
	Data Output				-400		
Low Level Output Current			I_{OL}		8	mA	
Average Input Flux			ϕ_M	0.8	100	µW	6
Peak-to-Peak Input Flux			ϕ_H-ϕ_L	1.6	200	µW	
Optical Input Pulse Duration and Timing	2-Level Code	High Level	t_H	100	5000	ns	
		Low Level	t_L				
	Flux Excursion Ratio		k	0.75	1.25		7
	3-Level Code	High Level	t_H	50		ns	8
		Low Level	t_L				
		Mid Level	t_M	0.05	6.7	µs	
	Refresh Repetition Rate		f_R	150		kHz	
	Refresh Duty Factor		$f_R t_H, f_R t_L$		0.04		

Electrical/Optical Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter			Symbol	Min	Typ[5]	Max	Units	Conditions		Fig.	Note
Output Voltage	High State	Data Output	V_{OH}	2.4	2.85		V	$\phi = (\phi_M + 0.8\ \mu W)$, $I_o = -400\ \mu A$	V_{CC} = 4.75 V	1, 2	7, 9
		Link Monitor						$\Delta\phi = 0.8\ \mu W$, $I_o = -100\ \mu A$			
	Low State	Data Output	V_{OL}		0.35	0.5	V	$\phi = (\phi_M - 0.8\ \mu W)$	I_o = 8 mA		
		Link Monitor			0.2	0.4		$\Delta\phi = 0$	V_{CC} = 4.75 V		
Test Point Voltage			V_T		0		V	$\phi_M = 100\ \mu W$			10
					1.3			$\phi_M = 0$			
Supply Current			I_{CC}		77	100	mA	V_{CC} = 5.25 V			
				60	77			V_{CC} = 4.75 V			
Optical Port (fiber optic core) Diameter			D_c		200		µm				
Numerical Aperture			N.A.		0.5					3	
Peak Responsivity Wavelength			λ_p		770		nm			4	

Dynamic Characteristics 0°C to 70°C Unless Otherwise Specified

Parameter			Symbol	Min	Typ[5]	Max	Units	Conditions	Fig.	Note
Propagation Delay	High to Low	3-Level Code	t_{PHL}		29	37	ns	V_{CC} = 4.75 V, k = 1, Link Monitor High	1	11
		2-Level Code			37	45				
	Low to High	3-Level Code	t_{PLH}		37	52	ns			12
		2-Level Code			45	60				
Link Monitor Response Time	Low-to-High		t_{MH}		20		ms	V_{CC} = 4.75 V $\Delta\phi = 0.8\ \mu W$		13
	High-to-Low		t_{ML}		1000			I_{OL} = 8 mA Peak-to-Peak		14
Bit Error Rate at 10 M baud			BER			10^{-9}		k = 1, $\Delta\phi \geq 0.8\ \mu W$		15

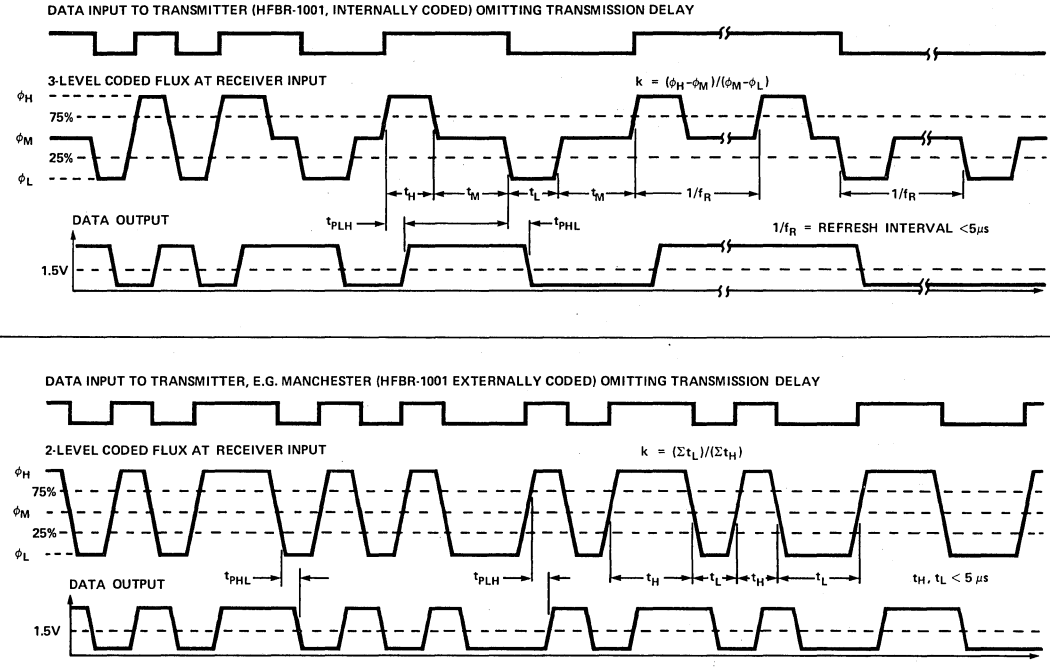


Figure 1. Optical Input Timing Requirements.

Notes (cont'd):

3. Measured at a point 2mm (.079") from where the lead enters the package.
4. If ripple exceeds the specified limit, the regulator shown in Figure 5 should be used. The LC filter shown in Figure 5 is recommended whether the regulator is used or not.
5. For typical values, V_{CC} = 5.00V and T_A = 25°C.
6. Flux is averaged over an interval of at least 50μs. Flux values specified are for the equivalent of a monochromatic source between 700nm and 820nm.
7. For either 2-level or 3-level code, k= $(\phi_H-\phi_M)/(\phi_M-\phi_L)$.
8. For the HFBR-2001, a *3-Level Code* is defined as having a mid-level, with equal-amplitude and pulse width excursions to high-level or to low-level.
9. Link Monitor provides a check of link continuity. A low Link Monitor output indicates that the optical signal path has been interrupted. For example, it might indicate a broken cable or a loose, dirty, or damaged connector. The link may still be operational with Link Monitor low, but it should be checked to determine the cause of the low indication. When the source of flux is an Internally-Coded HFBR-1001 Fiber Optic Transmitter, Link Monitor high will be a valid indication of link continuity whether or not data is being transmitted. An optical input with excursions ($\Delta\phi$) greater than or equal to 0.8μW is sufficient to hold Link Monitor high.
10. When observing V_T, use a voltmeter with at least 10MΩ input resistance. With zero input flux, V_T is at its maximum value, $V_{T,MAX}$. Then when flux is being received, whether modulated or not:

$$(V_{T,MAX} - V_T) = (25k\Omega)(I_P) = (25k\Omega)(R_\phi\phi_M)$$

where I_P = average photodiode photocurrent
$R_\phi \approx 0.4A/W$ = photodiode responsivity
ϕ_M = average flux being received

11. Measured from the time at which optical input crosses the 25% level until DATA OUTPUT = 1.5V in HL transition.
12. Measured from the time at which optical input crosses the 75% level until DATA OUTPUT = 1.5V in LH transition.

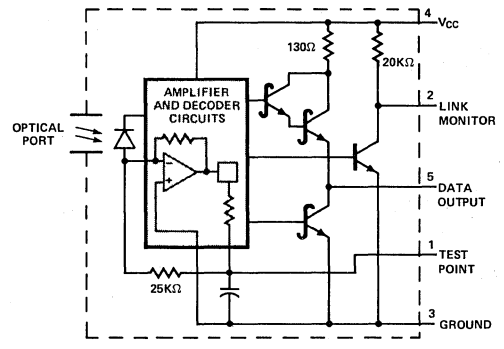


Figure 2. Schematic Diagram.

13. Measured from the time at which optical input fluctuation begins until LINK MONITOR rises to 1.5V.
14. Measured from the time at which optical input fluctuation ceases until LINK MONITOR falls to 1.5V.
15. With NRZ data, 10Mbaud corresponds to a data rate of 10Mb/s. With other codes, the data rate is the baud rate divided by the number of code intervals per bit interval—self-clocking code (e.g., Manchester) usually has two code intervals per bit interval giving 5Mb/s at 10Mbaud.

Electrical Description

Flux enters the HFBR-2001 via an optical fiber stub where a PIN photodiode converts it to a photocurrent. This photocurrent goes to an I-V (current-to-voltage) amplifier which utilizes both dc feedback and ALC (automatic level control).

The function of dc feedback is to keep the average value of the signal centered in the linear range of the amplifier. The dc feedback amplifier has a high impedance output to establish a long time constant on a capacitor at its output. (The voltage on the capacitor is observable at the test point). As seen in the schematic diagram, the voltage on this capacitor extracts the *average* component of photocurrent from the input of the I-V amplifier so its *average* output is at a *fixed level.* Optical flux excursions above and below the average cause voltage excursion above and below the fixed level at the output of the I-V amplifier.

The voltage excursions operate a flip-flop whose output drives the Data Output amplifier; an excursion above the average level sets the data output high, where it remains until an excursion below the average level resets the flip-flop.

To prevent overdrive, an ALC circuit, responding to excursions *either above or below* the average level, controls the gain of the I-V amplifier. Gain is then determined by *whichever polarity* of excursion is the *greater*. If these excursions are too far from being balanced, the gain limitation imposed by the larger excursion may cause the smaller (opposite polarity) excursion to be too small to operate the flip-flop.

The Link Monitor output is driven by an amplifier which responds to the ALC voltage. The Link Monitor is high when the flux excursions are greater than or equal to 0.8μW.

Mechanical and Thermal Considerations

Typical power consumption is less than 500mW so the Receiver can be mounted without consideration for additional heat sinking. The optical port is an optical fiber stub centered in a metallic ferrule. This ferrule supports a split-wall cylindrical spring sleeve which aligns the ferrule in the Receiver with the ferrule in the HFBR-3001 to -3005 Fiber Optic Connector/Cable. The connection procedure is to FIRST start the Connector ferrule into the sleeve, THEN screw the coupling ring on the barrel. The barrel performs no alignment function; its purpose is to hold the ferrule faces together when the coupling ring is tightened as specified in the HFBR-3001 to -3005 Fiber Optic Connector/Cable data sheet.

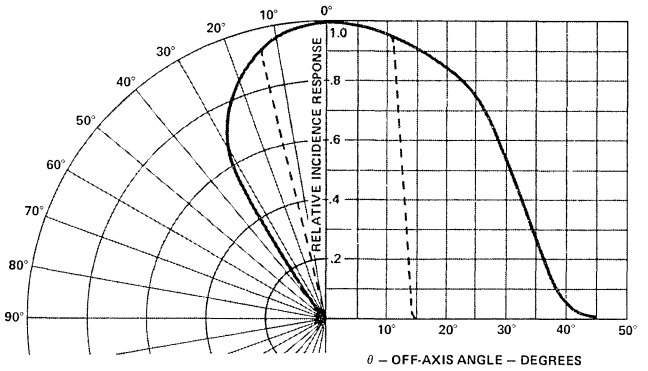


Figure 3. Reception Pattern.*

*The optical fiber is recessed within the barrel at a distance of approximately 7mm. Solid line represents reception pattern at fiber stub without obscuration by connector barrel. Dashed line represents reception pattern as seen from outside of connector.

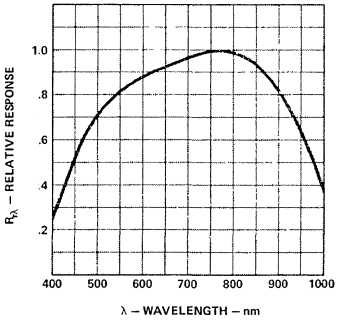


Figure 4. Spectral Response.

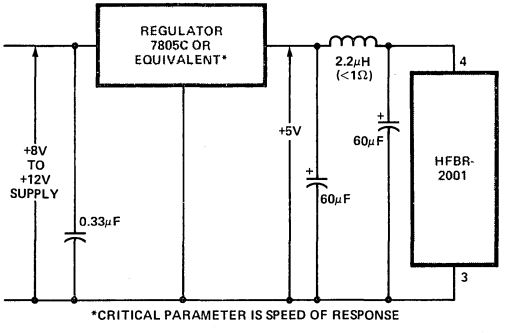


Figure 5. Power Supply Transient Filter Recommendation.

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COMPONENTS

NEW PRODUCT

FIBER OPTIC CONNECTOR/CABLE ASSEMBLIES

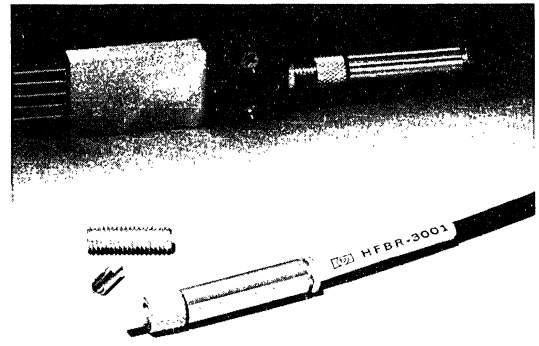
HFBR-3001 to-3005

HFBR-3099 ADAPTER

TECHNICAL DATA APRIL 1979

Features

- **CONNECTORS FACTORY INSTALLED AND TESTED**
- **LOW CONNECTOR LOSS**
- **LARGE NUMERICAL APERTURE**
- **LOW TRANSMISSION LOSS**
- **LOW DISPERSION**
- **HIGH STRENGTH**
- **LIGHT WEIGHT**
- **SINGLE-FIBER CONSTRUCTION**



Description

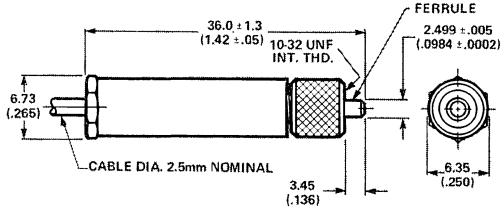
The HFBR-3001 to -3005 Fiber Optic Connector/Cable Assemblies are intended for use with the HFBR-1001 Transmitter and HFBR-2001 Receiver for digital data transmission at rates up to 10Mb/s NRZ over distances up to 100 metres. The Connectors mate directly with the optical ports on the Transmitter and Receiver. The cable uses a fused silica, step-index, glass-clad fiber surrounded by silicone coating, buffer jacket, and tensile strength members. This combination is then covered by a scuff-resistant outer jacket. The light weight and high strength of these assemblies allows them to be drawn through most electrical conduits. However, their resistance to mechanical abuses, safety in flammable environments, and inherent absence of electromagnetic interference effects may make the use of conduit unnecessary. The HFBR-3099 Adapter, for interconnecting cables, consists of two parts: a sleeve to align the ferrules and a barrel to join the connector couplings.

Selection Guide

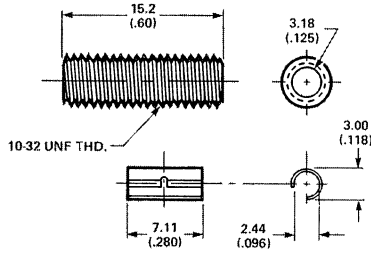
LENGTH IN METRES $\left(\frac{+1.0}{-0.0}\right)$	HFBR- SINGLE CHANNEL
10	3001
25	3002
50	3003
75	3004
100	3005

Mechanical Dimensions

CONNECTOR



HFBR-3099 ADAPTER



CAUTION:
COUPLING SHOULD NOT BE OVERTIGHTENED. SEE OPTICAL/MECHANICAL CHARACTERISTICS AND NOTE 4.

NOTES:
1. DIMENSIONS ARE IN mm (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCES ARE:
   .X ± .51mm (.XX ± .02 in.)
   .XX ± .13mm (.XXX ± .005 in.)
3. POLISHED FIBER END IS LOCKED FLUSH WITH FERRULE FACE.

Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Relative Humidity at T_A = 70°C				95	%
Storage Temperature		T_S	-40	+85	°C
Operating Temperature		T_A	0	+70	°C
Tensile Force	on Cable (Note 11)	F_T		300	N
	on Connector/Cable			50	N

Parameter	Symbol	Min	Max	Units	Note
Bend Radius	r	7		mm	11
Flexing			50,000	cycles	4
Crush Load	F_C		200	N	5
Impact	m		1	kg	6
	h		0.3	m	6

Mechanical/Optical Characteristics 0°C to +70°C Unless Otherwise Specified

Parameter	Symbol	Min	Typ(9)	Max	Units	Conditions	Fig	Note
Exit Numerical Aperture	N.A.		0.3		—	λ = 820nm ℓ = 100m	1	7
Transmission Loss per Unit Length	α_o		16	20	dB/km	λ = 700nm ℓ = 100m	2	
			10			λ = 820nm ℓ = 100m		
Rise Time Dispersion Constant	$\Delta t/\ell$		28		ns/km	700 < λ < 820nm	3	
Cable 3dB Bandwidth Constant	$\Delta f \cdot \ell$		12		MHz•km	700 < λ < 820nm		8
Fiber Optic Core Diameter	D_C		100		μm			
Cladding Outside Diameter	D_{CL}		140		μm			
Core Index of Refraction	η_C		1.49		—	700 < λ < 820nm		
Elongation Under Tensile Force	$\Delta\ell/\ell$		0.5		%	F = 300N		
Mass per Unit Length	m/ℓ		7.7		kg/km			
Eccentricity of Fiber in Ferrule	½TIR		4		μm	Coupling Ring "Finger Tight"	4	10
Insertion Loss (Connector-to-Connector)	$\alpha_{C\text{-}C}$		2.0		dB	Torque 0.05 < L < 0.1 N • m		

Notes (cont'd):

4. 180° bending at minimum bend radius.
5. On 2.5 mm diameter mandrel laid across the cable on a flat surface.
6. For mass m dropped from height h on 25 mm diameter mandrel laid across the cable on a flat surface.
7. Exit N.A. is defined as the sine of the angle at which the off-axis radiant intensity is 10% of the axial radiant intensity.
8. Cable 3dB Bandwidth is defined as 0.35/Rise Time Dispersion.
9. Typical values are at T_A = 25°C.
10. Overtightening may cause excessive fiber misalignment or permanent damage.
11. This applies for short term testing ≤ one hour.

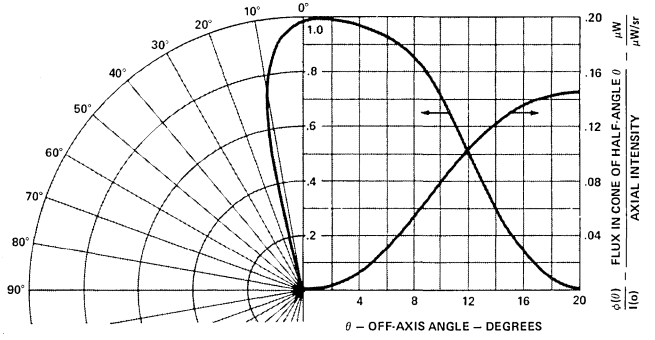


Figure 1. Optical Fiber Output Radiation Pattern.

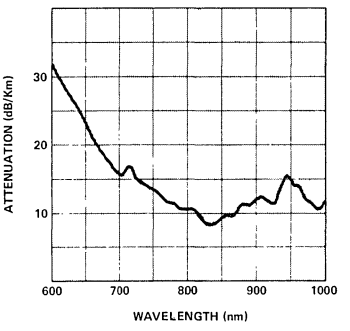


Figure 2. Spectral Transmission.

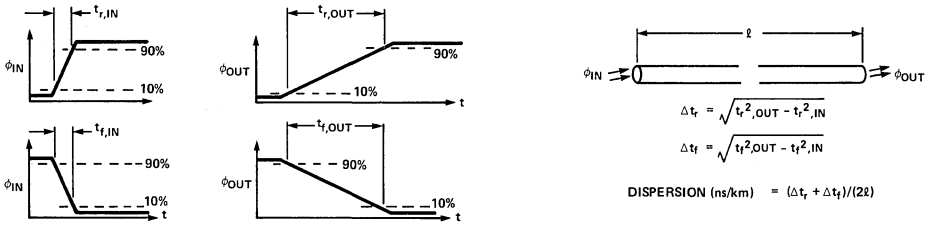


Figure 3. Definition of Dispersion.

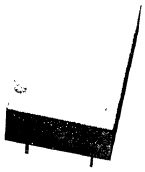
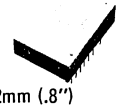
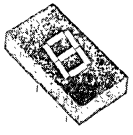
Solid State Displays

Optoelectronics Designer's Catalog 1979

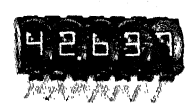
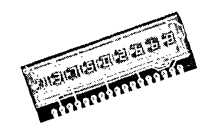
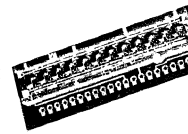
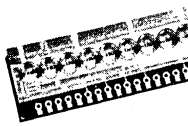
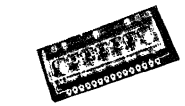
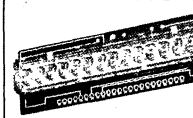
Red, High Efficiency Red, Yellow and Green Seven Segment LED Displays

Package	Device	Description	Application	Page No.
 7.62mm (.3") Dual-In-Line .75"H x .4"W x .18"D	5082-7610	High Efficiency Red, Common Anode, LHDP (14 Pin Epoxy)	General Purpose Market • Test Equipment • Digital Clocks • Clock Radios • TV Channel Indicators • Business Machines • Digital Instruments • Automobiles For further information see Application Notes 941 and 964 beginning on page 255.	31
	5082-7611	High Efficiency Red, Common Anode, RHDP (14 Pin Epoxy)		
	5082-7613	High Efficiency Red, Common Cathode, RHDP (10 Pin Epoxy)		
	5082-7616	7.11mm (.29") High Efficiency Red, Universal Polarity Overflow Indicator RHDP (14 Pin Epoxy)		
	5082-7620	Yellow, Common Anode LHDP (14 Pin Epoxy)		
	5082-7621	Yellow, Common Anode RHDP (14 Pin Epoxy)		
	5082-7623	Yellow, Common Cathode, RHDP (10 Pin Epoxy)		
	5082-7626	7.11mm (.29") Yellow, Universal Polarity and Overflow Indicator RHDP (14 Pin Epoxy)		
	5082-7630	Green, Common Anode LHDP (14 Pin Epoxy)		
	5082-7631	Green, Common Anode RHDP (14 Pin Epoxy)		
	5082-7633	Green, Common Cathode RHDP (10 Pin Epoxy)		
	5082-7636	7.11mm (.29") Green, Universal Polarity and Overflow Indicator RHDP (14 Pin Epoxy)		
 7.62mm (.3") Dual-In-Line .75"H x .4"W x .18"D	HDSP-3530	High Efficiency Red, Common Anode, LHDP (14 Pin Epoxy)		25
	HDSP-3531	High Efficiency Red, Common Anode, RHDP (14 Pin Epoxy)		
	HDSP-3533	High Efficiency Red, Common Cathode RHDP (10 Pin Epoxy)		
	HDSP-3536	7.11mm (.29") High Efficiency Red, Universal Polarity Overflow Indicator RHDP (14 Pin Epoxy)		
	HDSP-4030	Yellow , Common Anode, LHDP (14 Pin Epoxy)		
	HDSP-4031	Yellow, Common Anode, RHDP		
	HDSP-4033	Yellow, Common Cathode, RHDP (10 Pin Epoxy)		
	HDSP-4036	7.11mm (.29") Yellow, Universal Polarity Overflow Indicator RHDP (14 Pin Epoxy)		
 10.92mm (.43") Dual-In-Line .75"H x .5"W x .25"D (14 Pin Epoxy)	5082-7650	High Efficiency Red, Common Anode, LHDP		36
	5082-7651	High Efficiency Red, Common Anode, RHDP		
	5082-7653	High Efficiency Red, Common Cathode RHDP		
	5082-7656	10.36 (.4") High Efficiency Red Universal Polarity and Overflow Indicator RHDP		
	5082-7660	Yellow Common Anode LHDP		
	5082-7661	Yellow Common Anode RHDP		
	5082-7663	Yellow Common Cathode RHDP		
	5082-7666	10.36 (.4") Yellow Universal Polarity and Overflow Indicator RHDP		
	5082-7670	Green Common Anode LHDP		
	5082-7671	Green Common Anode RHDP		
	5082-7673	Green Common Cathode RHDP		
	5082-7676	10.36 (.4") Green Universal Polarity and Overflow Indicator RHDP		

Red, High Efficiency Red, Yellow and Green Seven Segment LED Displays (Cont.)

Package	Device	Description	Application	Page No.
 10.92mm (.43") Dual-In-Line .75"H x .5"W x .25"D (14 Pin Epoxy)	HDSP-3730	High Efficiency Red, Common Anode, LHDP	General Purpose Market • Test Equipment • Digital Clocks • Clock Radios • TV Channel Indicators • Business Machines • Digital Instruments • Automobiles For further information see Application Notes 941 and 964 beginning on page 255.	25
	HDSP-3731	High Efficiency Red, Common Anode, RHDP		
	HDSP-3733	High Efficiency Red, Common Cathode, RHDP		
	HDSP-3736	10.36mm (.4") High Efficiency Red, Universal Polarity Overflow Indicator RHDP		
	HDSP-4130	Yellow, Common Anode LHDP		
	HDSP-4131	Yellow, Common Anode RHDP		
	HDSP-4133	Yellow, Common Cathode RHDP		
	HDSP-4136	10.36mm (.4") Yellow, Universal Polarity Overflow Indicator RHDP		
 20.32mm (.8") Dual-In-Line 1.09"H x .78"W x .33"D (18 Pin Epoxy)	HDSP-3400	Red, Common Anode LHDP		21
	HDSP-3401	Red, Common Anode RHDP		
	HDSP-3403	Red, Common Cathode RHDP		
	HDSP-3405	Red, Common Cathode LHDP		
	HDSP-3406	18.87mm (.74") Red, Universal Polarity Overflow Indicator RHDP		
 7.62mm (.3") Dual-In-Line .75"H x .4"W x .18"D	5082-7730	Red, Common Anode, LHDP (14 Pin Epoxy)		41
	5082-7731	Red, Common Anode, RHDP (14 Pin Epoxy)		
	5082-7736	7.11mm (.29") Red, Common Anode, Polarity and Overflow Indicator (14 Pin Epoxy)		
	5082-7740	Red, Common Cathode, RHDP (10 Pin Epoxy)		
 10.92mm (.43") Dual-In-Line .75"H x .5"W x .25"D (14 Pin Epoxy)	5082-7750	Red, Common Anode, LHDP		45
	5082-7751	Red, Common Anode, RHDP		
	5082-7756	10.36mm (.4") Red, Universal Polarity and Overflow Indicator, RHDP		
	5082-7760	Red, Common Cathode, RHDP		

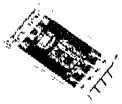
Red Seven Segment LED Displays

Device		Description	Package	Application	Page No.
	5082-7402	2.79mm(.11") Red, 3 Digits Right,[1] Centered D.P.	12 Pin Epoxy, 7.62mm (.3") DIP	Small Display Market • Portable/Battery Power Instruments • Portable Calculators • Digital Counters • Digital Thermometers • Digital Micrometers • Stopwatches • Cameras • Copiers • Digital Telephone Peripherals • Data Entry Terminals • Taxi Meters For further information ask for Application Note 937.	49
	5082-7403	2.79mm(.11") Red, 3 Digits Left,[1] Centered D.P.			
	5082-7404	2.79mm(.11") Red, 4 Digits Centered D.P.			
	5082-7405	2.79mm(.11") Red, 5 Digits, Centered D.P.	14 Pin Epoxy, 7.62mm (.3") DIP		
	5082-7412	2.79mm (.11") Red, 3 Digits Right,[1] RHDP	12 Pin Epoxy, 7.62mm (.3") DIP		
	5082-7413	2.79mm (.11") Red, 3 Digits Left,[1] RHDP			
	5082-7414	2.79mm(.11") Red, 4 Digit, RHDP			
	5082-7415	2.79mm(.11") Red, 5 Digit, RHDP	14 Pin Epoxy, 7.62mm (.3") DIP		
	5082-7432	2.79mm(.11") Red, 2 Digits Right,[2] RHDP	12 Pin Epoxy, 7.62mm (.3") DIP		53
	5082-7433	2.79mm(.11") Red, 3 Digits, RHDP			
	5082-7440	2.67mm(.105") Red, 8 Digits, Mounted on P.C. Board	50.8mm(2") P.C. Bd., 17 Term. Edge Con.		57
	5082-7448	2.67mm(.105") Red, 8 Digits, Mounted on P.C. Board	60.3mm(2.375")PC Bd., 17 Term. Edge Con.		
	5082-7441	2.67mm(.105") Red, 9 Digits, Mounted on P.C. Board	50.8mm(2") PC Bd., 17 Term. Edge Con.		
	5082-7449	2.67mm(.105") Red, 9 Digits, Mounted on P.C. Board	60.3mm(2.375")PC Bd., 17 Term. Edge Con.		
	5082-7442	2.54mm(.100") Red, 12 Digits, Mounted on P.C. Board	60.3mm(2.375")PC Bd., 20 Term. Edge Con.		
	5082-7445	2.54mm(.100") Red, 12 Digits, Mounted on P.C. Board	59.6mm(2.345")PC Bd., 20 Term. Edge Con.		
	5082-7444	2.54mm(.100") Red, 14 Digits, Mounted on P.C. Board	60.3mm(2.375") PC Bd., 22 Term. Edge Con.		
	5082-7446	2.92mm(.115") Red, 16 Digits, Mounted on P.C. Board	69.85mm(2.750")PC Bd., 24 Term. Edge Con.		
	5082-7447	2.85mm(.112") Red, 14 Digits, Mounted on P.C. Board	60.3mm(2.375") PC Bd., 22 Term. Edge Con.		
	5082-7240	2.59mm(.102") Red, 8 Digits, Mounted on P.C. Board	50.8mm (2") PC Bd., 17 Term. Edge Con.		65
	5082-7241	2.59mm(.102") Red, 9 Digits, Mounted on P.C. Board.			
	5082-7265	4.45mm(.175") Red, 5 Digits, Mounted on P.C. Board. Centered D.P.	50.8mm(2") PC Bd., 15 Term. Edge Con.		
	5082-7285	4.45mm(.175") Red, 5 Digits Mounted on P.C. Board. RHDP			
	5082-7275	4.45mm(.175") Red, 15 Digits, Mounted on P.C. Board. Centered D.P.	91.2mm(3.59") PC Bd., 23 Term. Edge Con.		
	5082-7295	4.45mm(.175") Red, 15 Digits, Mounted on P.C. Board. RHDP			

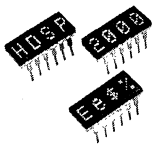
Integrated LED Displays

Device		Description	Package	Application	Page No.
	5082-7300	7.4mm (.29") 4x7 Single Digit Numeric, RHDP, Built-In Decover/Driver/Memory	8 Pin Epoxy, 15.2mm (.6") DIP	General Purpose Market • Test Equipment • Business Machines • Computer Peripherals • Avionics For further information ask for Application Note 934 on LED Display Installation Techniques	73
	5082-7302	7.4mm (.29") 4x7 Single Digit Numeric, LHDP, Built-In Decover/Driver/Memory			
	5082-7340	7.4mm (.29") 4x7 Single Digit Hexadecimal, Built-In Decoder/Driver/Memory			
	5082-7304	7.4mm (.29") Overrange Character Plus/Minus Sign			
	5082-7356	7.4mm (.29") 4x7 Single Digit Numeric, RHDP, Built-In Decoder/Driver/Memory	8 Pin Glass Ceramic 15.2mm (.6") DIP	• Medical Equipment • Industrial and Process Control Equipment • Computers • Where Ceramic Package IC's are required.	77
	5082-7357	7.4mm(.29") 4x7 Single Digit Numeric, LHDP, Built-In Decoder/Driver/Memory			
	5082-7359	7.4mm (.29") 4x7 Single Digit Hexadecimal, Built-In Decoder/Driver/Memory			
	5082-7358	7.4mm(.29") Overrange Character Plus/Minus Sign			

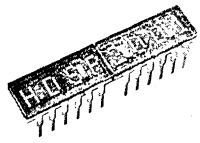
Hermetically Sealed Integrated LED Displays

Device		Description	Package	Application	Page No.
	5082-7010	6.8mm (.27") 5x7 Single Digit Numeric, LHDP, Built-In Decoder/Driver	8 Pin Hermetic 2.54mm (.100") Pin Centers	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems	82
	5082-7011	6.8mm (.27") Plus/Minus Sign			
	5082-7391	7.4mm (.29") 4x7 Single Digit Numeric, RHDP, Built-In Decoder/Driver/Memory	8 Pin Hermetic 15.2mm (.6") DIP with Gold Plated Leads	• Ground, Airborne, Shipboard Equipment • Fire Control Systems • Space Flight Systems • Other High Reliability Applications (TX Programs available, see page 88)	88
	5082-7392	7.4mm(.29") 4x7 Single Digit Numeric, LHDP, Built-In Decoder/Driver/Memory			
	5082-7395	7.4mm(.29") 4x7 Single Digit Hexadecimal, Built-In Decoder/Driver/Memory			
	5082-7393	7.4mm(.29") Overrange Character Plus/Minus Sign			

Alphanumeric LED Displays

Device		Description	Package	Application	Page No.
	HDSP-2000	3.7mm (.15") 5x7 Four Character Alphanumeric Built-In Shift Register, Drivers	12 Pin Ceramic 7.62mm (.3") DIP. Redglass Contrast Filter	• Programmable Calculators • Computer Terminals • Business Machines • Medical Instruments • Portable, Hand-held or mobile data entry, read-out or communications For further information see Application Notes 966 and 1001, starting on page 295.	94

Alphanumeric LED Displays (Cont.)

Device		Description	Package	Application	Page No.
	HDSP-2001	3.7mm (.15") 5x7 Four Character Alphanumeric Built-In Shift Register, Drivers	12 Pin Ceramic 7.62mm (.3") DIP. Integral Untinted Glass Lens	• Programmable Calculators • Computer Terminals • Business Machines • Medical Instruments • Portable, Hand-held or mobile data entry, read-out or communication For further information see Application Notes 966 and 1001, starting on page 295.	98
 	HDSP-2416	Single-Line 16 Character Display Panel Utilizing the HDSP-2000 Display	162.56mm (6.4") L x 58.42mm (2.3") H x 7.11mm (.28") D	• Data Entry Terminals • Instrumentation • Electronic Typewriters For further information see Application Note 1001 beginning on page 325.	102
	HDSP-2424	Single-Line 24 Character Display Panel Utilizing the HDSP-2000 Display.			
	HDSP-2432	Single-Line 32 Character Display Panel Utilizing the HDSP-2000 Display			
	HDSP-2440	Single-Line 40 Character Display Panel Utilizing the HDSP-2000 Display	177.80mm (7.0") L x 58.42mm (2.3") H x 7.11mm (.28") D		
	HDSP-2470	HDSP-2000 Display Interface Incorporating a 64 Character ASCII Decoder	171.22mm (6.74") L x 58.42mm (2.3") H x 16.51mm (.65") D		
	HDSP-2471	HDSP-2000 Display Interface Incorporating a 128 Character ASCII Decoder			
	HDSP-2472	HDSP-2000 Display Interface without ASCII Decoder. Instead, a 24 Pin Socket is Provided to Accept a Custom 128 Character Set from a User Programmed 1K x 8 PROM			
 	HDSP-6504	3.8mm (.15") Sixteen Segment Four Character Alphanumeric	26 Pin 15.2mm (.6") DIP	• Computer Peripherals and Terminals • Computer Base Emergency Mobile Units • Automotive Instrument Panels • Desk Top Calculators • Hand-held Instruments For further information ask for Application Note 931.	114
	HDSP-6508	3.8mm (.15") Sixteen Segment Eight Character Alphanumeric	22 Pin 15.2mm (.6") DIP		
	5082-7100	7.4mm (.29") 5x7 Three Digit Alphanumeric	22 Pin Hermetic 15.2mm (.6") DIP	General Purpose Market • Business Machines • Calculators • Solid State CRT • High Reliability Applications For further information ask for Application Note 931 on Alphanumeric Displays.	120
	5082-7101	7.4mm (.29") 5x7 Four Digit Alphanumeric	28 Pin Hermetic 15.2mm (.6") DIP		
	5082-7102	7.4mm (.29") 5x7 Five Digit Alphanumeric	36 Pin Hermetic 15.2mm (.6") DIP		

HEWLETT hp PACKARD
COMPONENTS

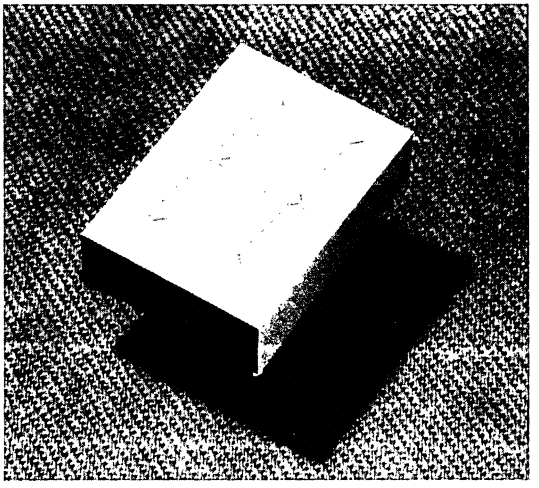
20mm (0.8") RED SEVEN SEGMENT DISPLAY

HDSP-3400 SERIES

TECHNICAL DATA APRIL 1979

Features

- **20mm (0.8") DIGIT HEIGHT**
  Viewing Up to 10 Metres (33 Feet)
- **EXCELLENT CHARACTER APPEARANCE**
  Excellent Readability in Bright Ambients Through Superior Contrast Enhancement
  — Gray Body Color
  — Untinted Segments
  Wide Viewing Angle
  Evenly Lighted Segments
  Mitered Corners on Segments
- **LOW POWER REQUIREMENTS**
  Single GaAsP Chip per Segment
- **EASY MOUNTING ON PC BOARD OR SOCKETS**
  Industry Standard 15.24mm (0.6") DIP with Lead Spacing on 2.54mm (0.1") Centers
  Industry Standard Package Dimensions and Pinouts
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit Within a Single Category
- **IC COMPATIBLE**
- **MECHANICALLY RUGGED**



Description

The HDSP-3400 Series are very large 20.32mm (0.8 in.) GaAsP LED seven segment displays. Designed for viewing distances up to 10 metres (33 feet), these single digit displays provide excellent readability in bright ambients.

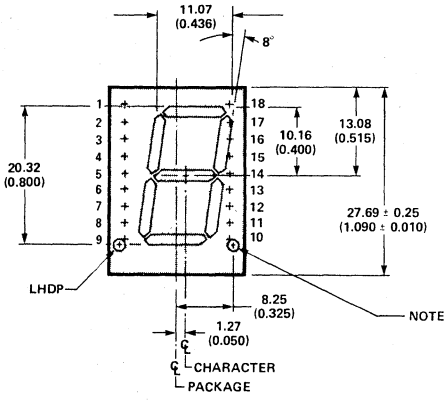
These devices utilize a standard 15.24mm (0.6 in.) dual in line package configuration that permits mounting on PC boards or in standard IC sockets. Requiring a low forward voltage, these displays are inherently IC compatible, allowing for easy integration into electronic instrumentation, point-of-sale terminals, TVs, weighing scales, and digital clocks.

Devices

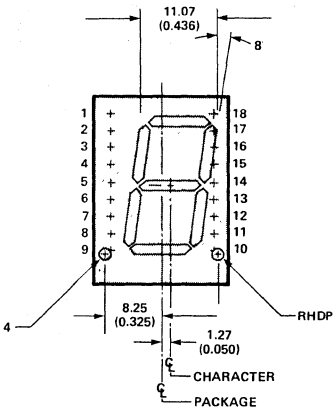
Part No. HDSP	Description	Package Drawing
-3400	Common Anode Left Hand Decimal	A
-3401	Common Anode Right Hand Decimal	B
-3403	Common Cathode Right Hand Decimal	C
-3405	Common Cathode Left Hand Decimal	D
-3406	Universal Overflow ±1 Right Hand Decimal	E

Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram E.

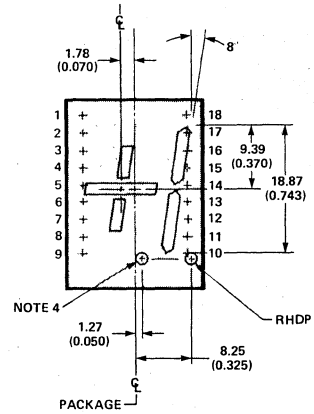
Package Dimensions



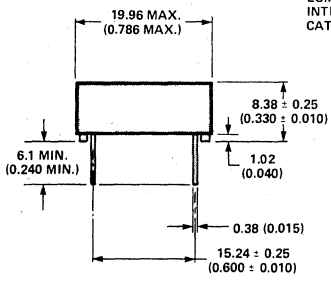
FRONT VIEW A,D



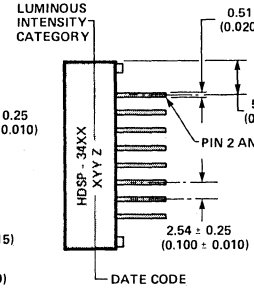
FRONT VIEW B,C



FRONT VIEW E



END VIEW

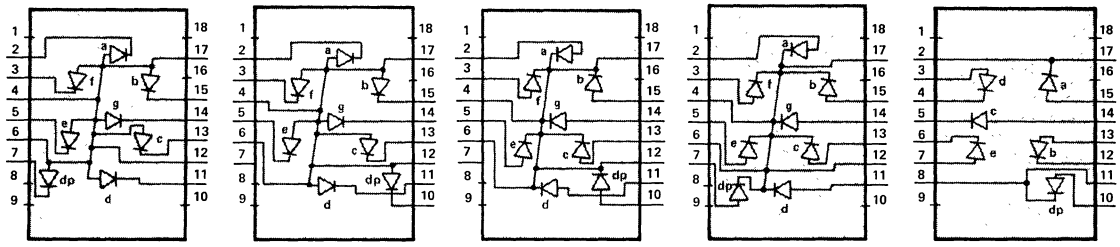


SIDE VIEW

Pin	Function A -3400	B -3401	C -3403	D -3405	E -3406
1	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
2	CATHODE a	CATHODE a	ANODE a	ANODE a	CATHODE a
3	CATHODE f	CATHODE f	ANODE f	ANODE f	ANODE d
4	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE d
5	CATHODE e	CATHODE e	ANODE e	ANODE e	CATHODE c
6	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE e
7	CATHODE dp	NO. CONNEC.	NO. CONNEC.	ANODE dp	ANODE e
8	NO PIN	NO PIN	NO PIN	NO PIN	CATHODE dp
9	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
10	NO PIN	CATHODE dp	ANODE dp	NO PIN	ANODE dp
11	CATHODE d	CATHODE d	ANODE d	ANODE d	CATHODE dp
12	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE b
13	CATHODE c	CATHODE c	ANODE c	ANODE c	ANODE b
14	CATHODE g	CATHODE g	ANODE g	ANODE g	ANODE c
15	CATHODE b	CATHODE b	ANODE b	ANODE b	ANODE a
16	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN
17	ANODE[3]	ANODE[3]	CATHODE[6]	CATHODE[6]	CATHODE a
18	NO PIN	NO PIN	NO PIN	NO PIN	NO PIN

NOTES:
1. Dimensions in millimetres and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathodes.

Internal Circuit Diagram



Absolute Maximum Ratings

Average Power Dissipation per Segment or DP (T_A = 50° C)[1] 100mW
Operating Temperature Range ..... -20° C to +85° C
Storage Temperature Range ..... -20° C to +85° C
Peak Forward Current per Segment or DP (T_A = 50° C, Pulse Width = 1.2ms)[2] 200mA
DC Forward Current per Segment or DP (T_A = 50° C)[1] 50mA
Reverse Voltage per Segment or DP 6.0V
Lead Soldering Temperature (1.6mm [1/16 inch] Below Seating Plane) ..... 260° C for 3 sec.

Notes:
1. Derate maximum DC current above T_A = 50° C at 1mA/° C per segment, see Figure 2.
2. See Figure 1 to establish pulsed operating conditions.

Electrical/Optical Characteristics at T_A=25°C

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment (Digit Average)[1]	I_V	I_F = 20mA	500	900		μcd
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength[2]	λ_d			640		nm
Forward Voltage, any Segment or DP	V_F	I_F = 20mA		1.6	2.0	V
Reverse Current, any Segment or DP	I_R	V_R = 5V		10	100	μA
Rise and Fall Time[3]	t_r, t_f			10		ns
Temperature Coefficient of Forward Voltage	ΔV_F/°C	I_F = 20mA		-1.5		mV/°C

Notes:
1. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
3. Time for a 10% - 90% change of light intensity for step change in current.

Operational Considerations

Electrical

The HDSP-3400 series of display devices are composed of eight light emitting diodes, with the light from each LED optically stretched to form individual segments and a decimal point. The LEDs have the P-N junction diffused into a GaAsP epitaxial layer on a GaAs substrate.

These display devices are designed for strobed operation at high peak currents. The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design may be calculated using the following V_F model:

$V_F = 1.78V + I_{PEAK}(3.7\Omega)$
For: 30mA $\leq I_{PEAK} \leq$200mA

Temperature derated strobed operating conditions are obtained from Figures 1 and 2. Figure 1 relates pulse duration (t_P), refresh rate (f), and ratio of maximum peak current to maximum dc current (I_{PEAK} MAX/I_{dc} MAX). Figure 2 presents the maximum allowed dc current vs. ambient temperature. To most effectively use Figures 1 and 2, perform the following steps:

1. Determine desired duty factor, DF.
   Example: Four digits, DF = 1/4
2. Determine desired refresh rate, f. Use duty factor to calculate pulse duration, t_p. Note: DF = f·t_p.
   Example: f = 1kHz, t_p = 250μs
3. Enter Figure 1 at the calculated t_p. Move vertically to the refresh rate line and record the corresponding value of I_{PEAK} MAX/I_{dc} MAX.
   Example: At t_p = 250μs and f = 1kHz,
   I_{PEAK} MAX/I_{dc} MAX = 3.2
4. From Figure 2, determine I_{dc} MAX. Note: I_{dc} MAX is derated above T_A = 50°C.
   Example: At T_A = 70°C, I_{dc} MAX = 30mA
5. Calculate I_{PEAK} MAX from I_{PEAK} MAX/I_{dc} MAX ratio and calculate I_{AVG} from I_{PEAK} MAX and DF.
   Example: I_{PEAK} MAX = (3.2) (30mA) = 96mA peak.
   I_{AVG} = (1/4) (96mA) = 24mA average.

The above calculations determine the maximum allowed strobing conditions. Operation at a reduced peak current and/or pulse width may be desirable to adjust display light output to match ambient light level or to reduce power dissipation to insure even more reliable operation.

Refresh rates of 1kHz or faster provide the most efficient operation resulting in the maximum possible time average luminous intensity.

The time average luminous intensity may be calculated using the relative efficiency characteristic of Figure 3, $\eta_{I\ PEAK}$, and adjusted for operating ambient temperature. The time average luminous intensity at T_A = 25°C is calculated as follows:

$$I_{V\ TIME\ AVG} = \left[\frac{I_{AVG}}{20mA}\right]\left[\eta_{I\ PEAK}\right]\left[I_{V\ DATA\ SHEET}\right]$$

Example: At I_{AVG} = 24mA and I_{PEAK} = 96mA

$$I_{V\ TIME\ AVG} = \left[\frac{24mA}{20mA}\right][1.19][900] = 1285\ \mu cd/Segment$$

This time average luminous intensity may be adjusted for ambient temperature by the following exponential equation:

$$I_V(T_A) = I_V(25°C)e^{[(-.0188/°C)(T_A - 25°C)]}$$

Example: T_A = 50°C

$$I_V(T_A) = (1285\ \mu cd)\ e^{[(-.0188/°C)(50-25°C)]} = 803\ \mu cd/Segment$$

Optical and Contrast Enhancement

The color of the display emitted light is red. The light radiation pattern from each segment is essentially Lambertian.

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to have the OFF-segments blend into the display background and to have the ON-segments stand out vividly against this same background. To achieve this goal the HDSP-3400 displays use a gray package and untinted segments to maximize readability in bright ambients.

Additional contrast enhancement is achieved by using a filter to reduce the luminous sterance of the display

background to a very low level, compared to the luminous sterance of the illuminated segments. These displays may be effectively filtered by using one of the following filter products: SGL Homalite H100-1605 RED or H100-1804 PURPLE: Panelgraphic RUBY RED 60, DARK RED 63 or PURPLE 90; Plexiglass 2423; 3M Light Control Film (louvered filters) in 80% Neutral Density, RED 655, VIOLET or PURPLE colors.

Mechanical

The HDSP-3400 series devices are constructed utilizing a lead frame in a standard DIP package. The LED dice are die attached directly to the lead frame. Therefore, the cathode leads are the direct thermal and mechanical stress paths to the LED dice. The absolute maximum allowed junction temperature, T_J MAX, is 100°C. The maximum power ratings have been established so that the worst case V_F device does not exceed this limit. For most reliable operation, it is recommended that the device pin-to-ambient thermal resistance through the PC board be less than 125°C/W segment. This will then establish a maximum thermal resistance LED junction-to-ambient to 500°C/W per segment.

These devices may be close-packed on 20mm (0.786 inch) centers on a PC board. Also, the large character height allows wider spacing options when desired. The package has a small tab at each corner to establish a 1.02mm (0.040 inch) seating plane.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°C) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

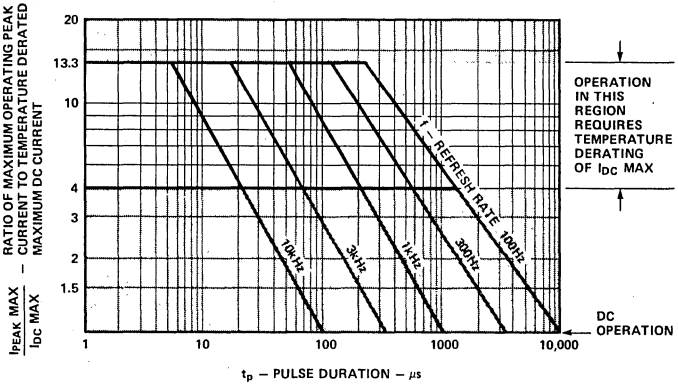


Figure 1. Maximum Allowable Peak Current vs. Pulse Duration.

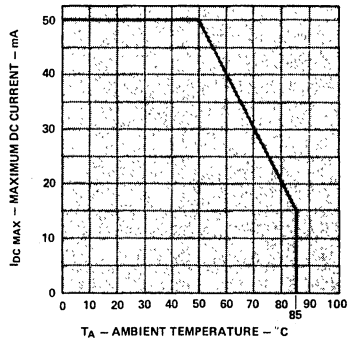


Figure 2. Maximum Allowable DC Current per Segment vs. Ambient Temperature.

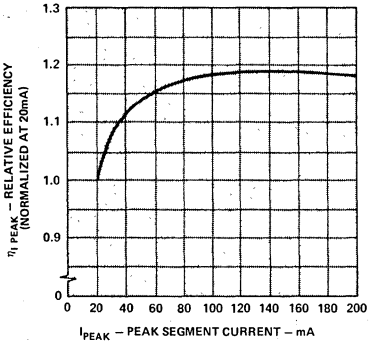


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current.

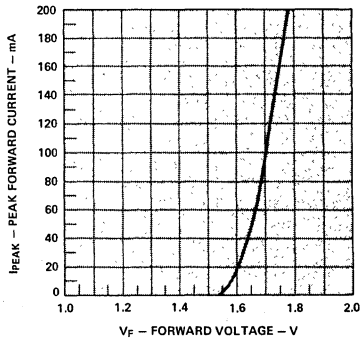


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage.

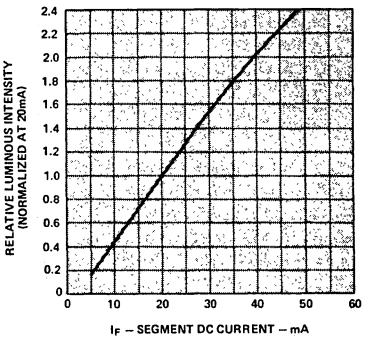


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

HEWLETT hp PACKARD

COMPONENTS

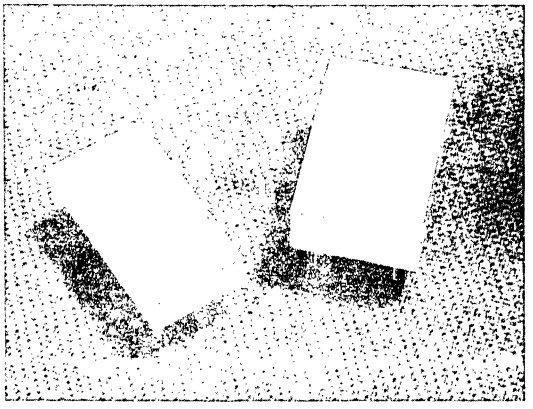
7.6/10.9mm (0.3/0.43 INCH) SEVEN SEGMENT DISPLAYS FOR HIGH LIGHT AMBIENT CONDITIONS

HIGH EFFICIENCY RED · HDSP-3530/3730 SERIES
YELLOW · HDSP-4030/4130 SERIES

TECHNICAL DATA APRIL 1979

Features

- **HIGH LIGHT OUTPUT**
  Typically 2300 μcd/Segment at 100mA Peak, 20mA Average
  Designed for Multiplex Operation
- **CHOICE OF TWO COLORS**
  High Efficiency Red
  Yellow
- **EXCELLENT CHARACTER APPEARANCE**
  Evenly Lighted Segments
  Wide Viewing Angle
  Gray Body Color for Optimum Contrast
- **EASY MOUNTING ON PC BOARD OR SOCKETS**
  Industry Standard 7.62mm (0.3 in.) DIP Leads on 2.54mm (0.1 in.) Centers
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Use of Like Categories Yields a Uniform Display
- **IC COMPATIBLE**
- **MECHANICALLY RUGGED**



Description

The HDSP-3530/4030 and -3730/4130 series are 7.62/10.92mm (0.3/0.43 in.) high efficiency red and yellow displays designed for use in high light ambient conditions. These displays are designed for use in instruments, airplane cockpits, weighing scales, and point of sale terminals.

The HDSP-3530/4030 and -3730/4130 series devices utilize high efficiency LED chips, which are made from GaAsP on a transparent GaP substrate. The active junction area is larger than that used in the 5082-7610/7620/7650/7660 series to permit higher peak currents.

Devices

Part No. HDSP-	Color	Description	Package Drawing
3530	High Efficiency Red	7.6mm Common Anode Left Hand Decimal	A
3531	High Efficiency Red	7.6mm Common Anode Right Hand Decimal	B
3533	High Efficiency Red	7.6mm Common Cathode Right Hand Decimal	C
3536	High Efficiency Red	7.6mm Universal Overflow ±1 Right Hand Decimal	D
4030	Yellow	7.6mm Common Anode Left Hand Decimal	A
4031	Yellow	7.6mm Common Anode Right Hand Decimal	B
4033	Yellow	7.6mm Common Cathode Right Hand Decimal	C
4036	Yellow	7.6mm Universal Overflow ±1 Right Hand Decimal	D
3730	High Efficiency Red	10.9mm Common Anode Left Hand Decimal	E
3731	High Efficiency Red	10.9mm Common Anode Right Hand Decimal	F
3733	High Efficiency Red	10.9mm Common Cathode Right Hand Decimal	G
3736	High Efficiency Red	10.9mm Universal Overflow ±1 Right Hand Decimal	H
4130	Yellow	10.9mm Common Anode Left Hand Decimal	E
4131	Yellow	10.9mm Common Anode Right Hand Decimal	F
4133	Yellow	10.9mm Common Cathode Right Hand Decimal	G
4136	Yellow	10.9mm Universal Overflow ±1 Right Hand Decimal	H

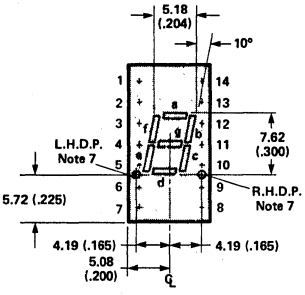
Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagrams D and H.

Absolute Maximum Ratings (All Products)

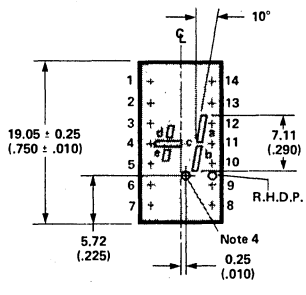
Average Power Dissipation Per Segment or DP (T_A=50° C) 83mW
Operating Temperature Range ..... -40° C to +85° C
Storage Temperature Range ..... -40° C to +85° C
Peak Forward Current Per Segment or DP (T_A = 50° C)[2] 120mA
(Pulse Width = 1.25ms)
DC Forward Current Per Segment or DP (T_A=50° C)[1] 30mA
Reverse Voltage Per Segment or DP 6.0V
Lead Soldering Temperature (1.6mm [1/16 inch]
below seating plane) ..... 260° C for 3 Seconds

Notes: 1. Derate maximum DC current above T_A=50° C at 0.51 mA/° C per segment, see Figure 2. 2. See Figure 1 to establish pulsed operating conditions.

Package Dimensions (HDSP-3530/4030 Series)

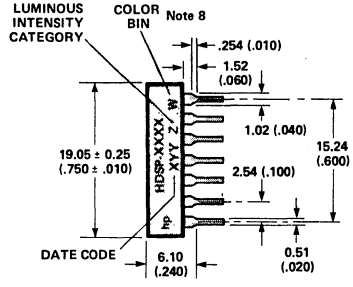


A,B,C

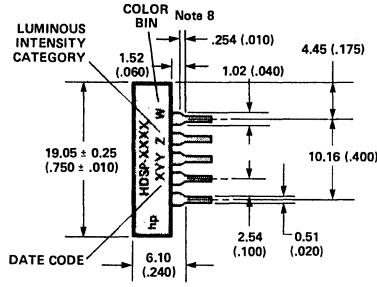


D

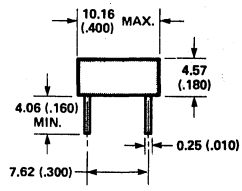
PIN	FUNCTION A -3530/-4030	B -3531/-4031	C -3533/-4033	D -3536/-4036
1	CATHODE-a	CATHODE-a	CATHODE[6]	ANODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	NO PIN
3	ANODE[3]	ANODE[3]	ANODE-g	CATHODE-d
4	NO PIN	NO PIN	ANODE-e	CATHODE-c
5	NO PIN	NO PIN	ANODE-d	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	CATHODE[6]	ANODE-a
7	CATHODE-e	CATHODE-e	ANODE-dp	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-c	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	ANODE-b	NO PIN
10	CATHODE-c	CATHODE-c	ANODE-a	CATHODE-dp
11	CATHODE-g	CATHODE-g		CATHODE-b
12	NO PIN	NO PIN		CATHODE-a
13	CATHODE-b	CATHODE-b		ANODE-a
14	ANODE[3]	ANODE[3]		ANODE-b



A,B,D SIDE



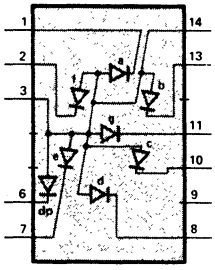
C SIDE



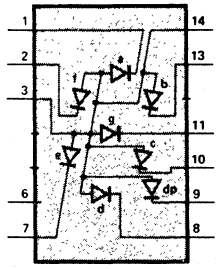
A,B,C,D END

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathode.
7. See part number table for L.H.D.P. and R.H.D.P. designation.
8. For HDSP-4030 series product only.

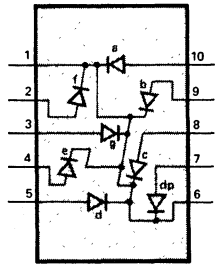
Internal Circuit Diagram (HDSP-3530/4030 Series)



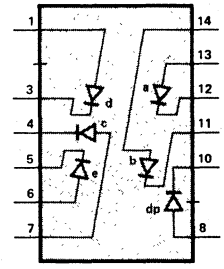
A



B

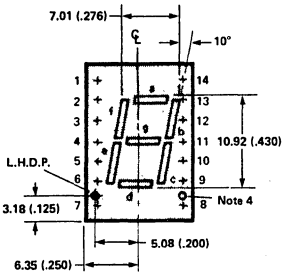


C

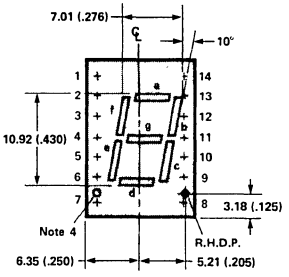


D

Package Dimensions (HDSP-3730/4130 Series)

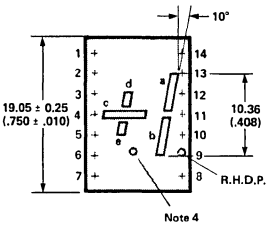


E

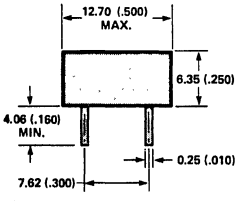


F,G

FRONT VIEW

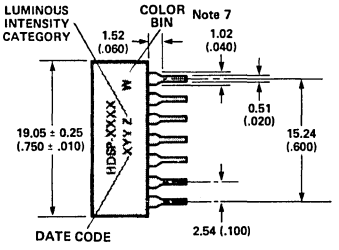


H



E, F, G, H

END VIEW



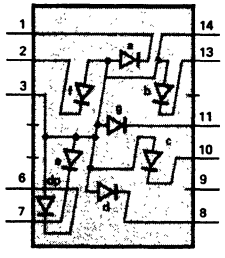
E, F, G, H

SIDE VIEW

PIN	FUNCTION			
	E 3730/-4130	F -3731/-4131	G -3733/-4133	H -3736/-4136
1	CATHODE-a	CATHODE-a	ANODE-a	CATHODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	ANODE-d
3	ANODE[3]	ANODE[3]	CATHODE[6]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE-c
5	NO PIN	NO PIN	NO PIN	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	NO CONN.[5]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-e	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-d	ANODE-dp
9	NO CONN.[6]	CATHODE-dp	ANODE-dp	CATHODE-dp
10	CATHODE-c	CATHODE-c	ANODE-c	CATHODE-b
11	CATHODE-g	CATHODE-g	ANODE-g	CATHODE-a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-b	ANODE-a
14	ANODE[3]	ANODE[3]	CATHODE[6]	ANODE-b

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram
6. Redundant cathode.
7. For HDSP-4130 series product only.

Internal Circuit Diagram (HDSP-3730/4130 Series)



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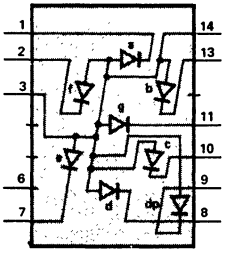

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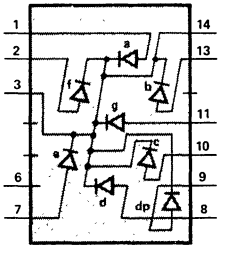

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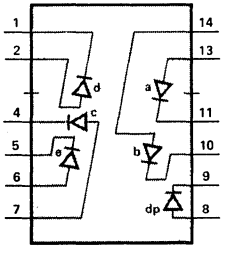


H

Electrical/Optical Characteristics at T_A=25°C

HIGH EFFICIENCY RED HDSP-3530/-3531/-3533/-3536/-3730/-3731/-3733/-3736

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[3]	I_V	100mA Pk: 1 of 5 Duty Factor	1000	2300		μcd
(Digit Average)		20mA DC		1800		μcd
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[4]	λ_d			626		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 100mA		2.55	3.1	V
Reverse Current/Segment or D.P.	I_R	V_R = 6V		10		μA
Response Time, Rise and Fall[6]	t_r, t_f			300		ns
Temperature Coefficient of V_F/Segment or D.P.	ΔV_F/°C	I_F = 100mA		-1.1		mV/°C

YELLOW HDSP-4030/-4031/-4033/-4036/-4130/-4131/-4133/-4136

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[3]	I_V	100mA Pk: 1 of 5 Duty Factor	1000	2700		μcd
(Digit Average)		20mA DC		2100		μcd
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[4,5]	λ_d			585		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 100mA		2.6	3.1	V
Reverse Current/Segment or D.P.	I_R	V_R = 6V		10		μA
Response Time, Rise and Fall[6]	t_r, t_f			200		ns
Temperature Coefficient of V_F/Segment or D.P.	ΔV_F/°C	I_F = 100mA		-1.1		mV/°C

NOTES:
3. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
4. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.
5. The HDSP-4030/-4130 series yellow displays are categorized as to dominant wavelength with the category designated by a number adjacent to the intensity category letter.
6. The rise and fall times are for a 10%-90% change of light intensity to a step change in current.

Operational Considerations

ELECTRICAL

The HDSP-3530/3730/4030/4130 series of display devices are composed of eight light emitting diodes, with the light from each LED optically stretched to form individual segments and a decimal point. The LEDs have a large area P-N junction diffused into a GaAsP epitaxial layer on a GaP transparent substrate.

These display devices are designed for strobed operation at high peak currents. The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design and maximum power dissipation may be calculated using the following V_F models:

$V_F = 2.0V + I_{PEAK}\ (11\Omega)$

For $I_{PEAK} \geq 30mA$

$V_F = 1.9V + I_{DC}\ (14\Omega)$

For $10mA \leq I_{DC} \leq 30mA$

Temperature derated strobed operating conditions are obtained from Figures 1 and 2. Figure 1 relates pulse duration (t_p), refresh rate (f), and the ratio of maximum peak current to maximum dc current (I_{PEAK} MAX/I_{DC} MAX). Figure 2 presents the maximum allowed dc current vs. ambient temperature. To most effectively use Figures 1 and 2, perform the following steps:

1. Determine desired duty factor, DF.
   Example: Five digits, DF = 1/5
2. Determine desired refresh rate, f. Use duty factor to calculate pulse duration, t_p. Note: DF = f·t_p.
   Example: f = 1 kHz, t_p = 200 μs
3. Enter Figure 1 at the calculated t_p. Move vertically to the refresh rate line and record the corresponding value of I_{PEAK} MAX/I_{DC} MAX.
   Example: At t_p = 200μs and f = 1 kHz, I_{PEAK} MAX/I_{DC} MAX = 4.0
4. From Figure 2, determine I_{DC} MAX. Note: I_{DC} MAX is derated above T_A = 50°C.
   Example: At T_A = 60°C, I_{DC} MAX = 25mA
5. Calculate I_{PEAK} MAX from I_{PEAK} MAX/I_{DC} MAX ratio and calculate I_{AVG} from I_{PEAK} MAX and DF.
   Example: I_{PEAK} MAX = (4.0) (25mA) = 100mA peak. I_{AVG} = (1/5) (100mA) = 20mA average.

The above calculations determine the maximum allowed strobing conditions. Operation at a reduced peak current and/or pulse width may be desirable to adjust display light output to match ambient light level or to reduce power dissipation to insure even more reliable operation.

Refresh rates of 1 kHz or faster provide the most efficient operation resulting in the maximum possible time average luminous intensity.

The time average luminous intensity may be calculated using the relative efficiency characteristic of Figure 3, η_{IPEAK}, and adjusted for operating ambient temperature. The time average luminous intensity at T_A=25°C is calculated as follows:

$$I_{V\ TIME\ AVG} = \left[\frac{I_{AVG}}{20mA}\right]\left[\eta_{IPEAK}\right]\left[I_{V\ DATA\ SHEET}\right]$$

Example: For HDSP-4030 series

η_{IPEAK} = 1.00 at I_{PEAK} = 100mA

$$I_{V\ TIME\ AVG} = \left[\frac{20mA}{20mA}\right]\left[1.00\right]\left[2.7mcd\right] = 2.7mcd/segment$$

The time average luminous intensity may be adjusted for operating ambient temperature by the following exponential equation:

$$I_V(T_A) = I_V(25°C)\, e^{[K\,(T_A - 25°C)]}$$

Device	K
-3530/3730 Series	-0.0131/°C
-4030/4130 Series	-0.0112/°C

Example: I_V (70°C) = (2.7mcd) $e^{[-0.0112\,(70-25)]}$ = 1.63mcd/segment

CONTRAST ENHANCEMENT

The objective of contrast enhancement is to provide good display readability in the end use ambient light. The concept is to employ chrominance contrast techniques to enhance readability by having the off-segments blend into the display background and have the on-segments stand out vividly against this same background. Therefore, these display devices are assembled with a gray package and untinted encapsulating epoxy in the segments.

Contrast enhancement in bright ambients may be achieved by using a neutral density gray filter such as Panelgraphic Chromafilter Gray 10. Additional contrast enhancement may be achieved by using the neutral density 3M Light Control Film (louvered filter).

MECHANICAL

These devices are constructed utilizing a lead frame in a standard DIP package. The LED dice are attached directly to the lead frame. Therefore, the cathode leads are the direct thermal and mechanical stress paths to the LED dice. The absolute maximum allowed junction temperature, T_J MAX, is 100°C. The maximum power ratings have been established so that the worst case V_F device does not exceed this limit. For most reliable operation, it is recommended that the device pin-to-ambient thermal resistance through the PC board be less than 320°C/W per segment. This will then establish a maximum thermal resistance LED junction-to-ambient of 602°C/W per segment.

These display devices may be operated in ambient temperatures above +50°C without derating when installed in a PC board configuration that provides a thermal resistance to ambient value less than 602°C/W/Segment. See Figure 6 to determine the maximum allowed thermal resistance for the PC board, $R\theta_{PC-A}$, which will permit nonderated operation in a given ambient temperature.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

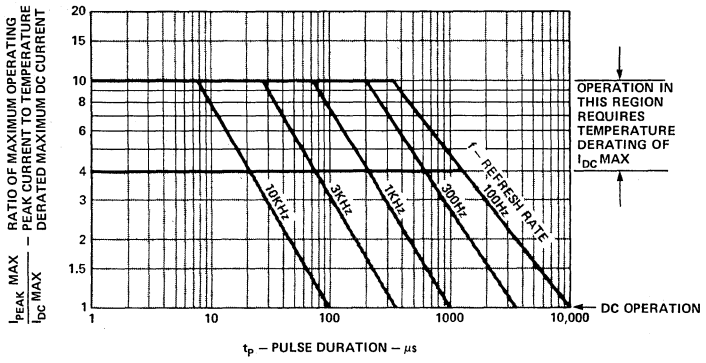


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration.

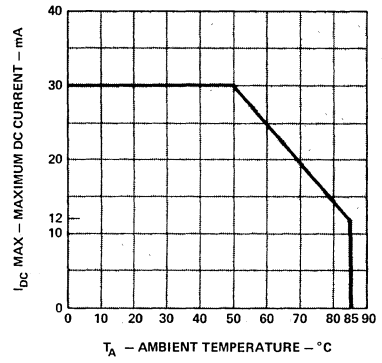


Figure 2. Maximum Allowable DC Current per Segment vs. Ambient Temperature.

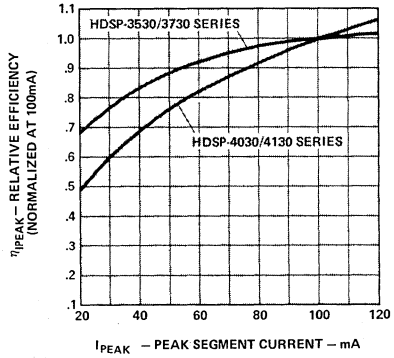


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current.

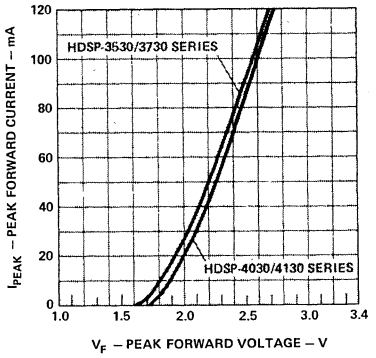


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage.

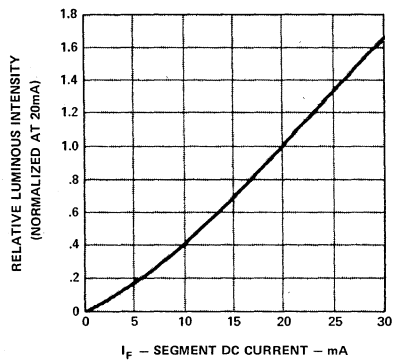


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

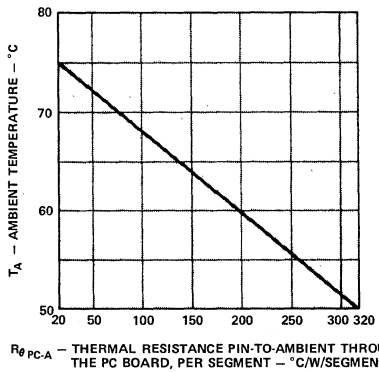


Figure 6. Maximum Operating Ambient Temperature vs. Thermal Resistance to Ambient Through the PC Board, for Device Operation Without Derating Forward Current.

HEWLETT hp PACKARD

COMPONENTS

.3 INCH SEVEN SEGMENT DISPLAYS

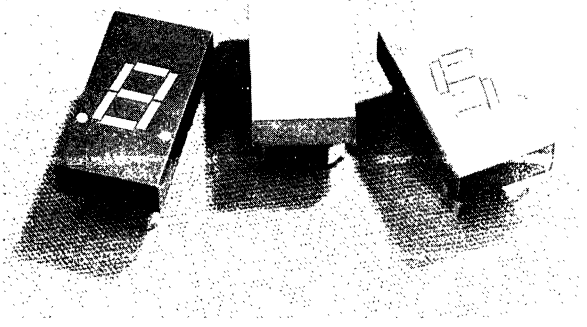
HIGH EFFICIENCY RED • 5082-7610 SERIES
YELLOW • 5082-7620 SERIES
GREEN • 5082-7630 SERIES

TECHNICAL DATA APRIL 1979

SOLID STATE DISPLAYS

Features

- **COMPACT SIZE**
- **CHOICE OF 3 BRIGHT COLORS**
  - **High Efficiency Red**
  - **Yellow**
  - **Green**
- **LOW CURRENT OPERATION**
  - **As Low as 3mA per Segment**
  - **Designed for Multiplex Operation**
- **EXCELLENT CHARACTER APPEARANCE**
  - **Evenly Lighted Segments**
  - **Wide Viewing Angle**
  - **Body Color Improves "Off" Segment Contrast**
- **EASY MOUNTING ON PC BOARD OR SOCKETS**
  - **Industry Standard 7.62mm (.3 in.) DIP Leads on 2.54mm (.1 in.) Centers**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  - **Use of Like Categories Yields a Uniform Display**
- **IC COMPATIBLE**
- **MECHANICALLY RUGGED**



Description

The 5082-7610, -7620, and -7630 series are 7.62mm (.3 in.) High Efficiency Red, Yellow, and Green seven segment displays. These displays are designed for use in instruments, point of sale terminals, clocks, and appliances.

The -7610, and -7620 series devices utilize high efficiency LED chips which are made from GaAsP on a transparent GaP substrate.

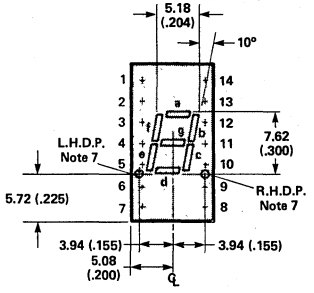
The -7630 series devices utilize chips made from GaP on a transparent GaP substrate.

Devices

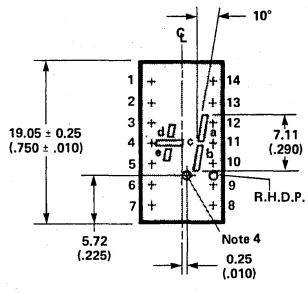
Part No. 5082-	Color	Description	Package Drawing
-7610	High Efficiency Red	Common Anode Left Hand Decimal	A
-7611	High Efficiency Red	Common Anode Right Hand Decimal	B
-7613	High Efficiency Red	Common Cathode Right Hand Decimal	C
-7616	High Efficiency Red	Universal Overflow ±1 Right Hand Decimal	D
-7620	Yellow	Common Anode Left Hand Decimal	A
-7621	Yellow	Common Anode Right Hand Decimal	B
-7623	Yellow	Common Cathode Right Hand Decimal	C
-7626	Yellow	Universal Overflow ±1 Right Hand Decimal	D
-7630	Green	Common Anode Left Hand Decimal	A
-7631	Green	Common Anode Right Hand Decimal	B
-7633	Green	Common Cathode Right Hand Decimal	C
-7636	Green	Universal Overflow ±1 Right Hand Decimal	D

NOTE: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram D.

Package Dimensions

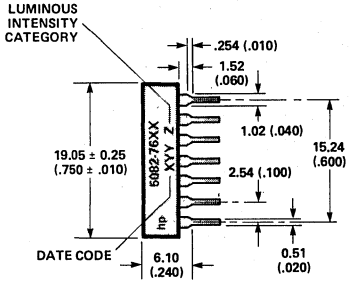


A,B,C

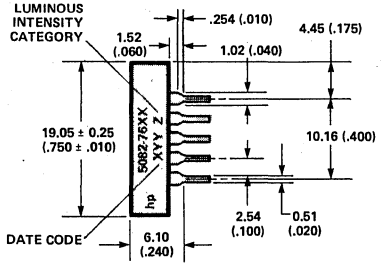


D

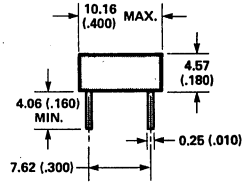
PIN	FUNCTION A -7610/-7620/ -7630	B -7611/-7621/ -7631	C -7613/-7623/ -7633	D -7616/-7626/ -7636
1	CATHODE-a	CATHODE-a	CATHODE[6]	ANODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	NO PIN
3	ANODE[3]	ANODE[3]	ANODE-g	CATHODE-d
4	NO PIN	NO PIN	ANODE-e	CATHODE-c
5	NO PIN	NO PIN	ANODE-d	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	CATHODE[6]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-dp	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-c	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	ANODE-b	NO PIN
10	CATHODE-c	CATHODE-c	ANODE-a	CATHODE-dp
11	CATHODE-g	CATHODE-g		CATHODE-b
12	NO PIN	NO PIN		CATHODE-a
13	CATHODE-b	CATHODE-b		ANODE-a
14	ANODE[3]	ANODE[3]		ANODE-b



A,B,D
SIDE



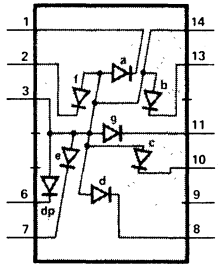
C
SIDE



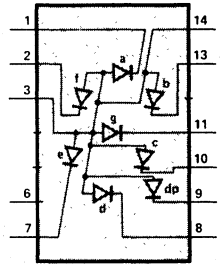
A,B,C,D
END

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathode.
7. See part number table for L.H.D.P. and R.H.D.P. designation.

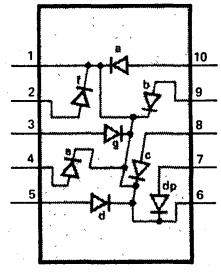
Internal Circuit Diagram



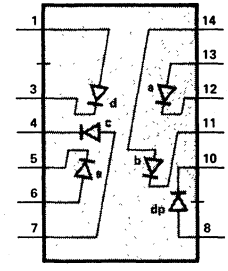
A



B



C



D

Absolute Maximum Ratings

DC Power Dissipation Per Segment or D.P.[1] (T_A=25°C) 50mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -40°C to +85°C
Peak Forward Current Per Segment or D.P.[3] (T_A=25°C) 60mA
Average Forward Current Per Segment or D.P.[1,2] (T_A=25°C) 20mA
Reverse Voltage Per Segment or D.P. 6.0V
Lead Soldering Temperature ..... 260°C for 3 Sec
[1.59mm (1/16 inch) below seating plane[4]]

Notes: 1. See power derating curve (Fig. 2). 2. Derate DC current from 50°C at 0.4mA/°C per segment. 3. See Fig. 1 to establish pulsed operating conditions. 4. Clean only in water, isopropanol, ethanol, Freon TF or TE (or equivalent) and Genesolv DI-15 or DE-15 (or equivalent).

Electrical/Optical Characteristics at T_A=25°C

HIGH EFFICIENCY RED 5082-7610/-7611/-7613/-7616

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment [5,8] (Digit Average)	I_v	5mA D.C.	70	250		μcd
		20mA D.C.		1430		μcd
		60mA Pk: 1 of 6 Duty Factor		810		μcd
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength [6]	λ_d			626		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 5mA		1.7		V
		I_F = 20mA		2.0	2.5	
		I_F = 60mA		2.8		
Reverse Current/Segment or D.P.	I_R	V_R = 6V		10		μA
Response Time [7]	t_r, t_f			90		ns
Temperature Coefficient of V_F/Segment or D.P.	ΔV_F/°C			−2.0		mV/°C

YELLOW 5082-7620/-7621/-7623/-7626

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment [5,8] (Digit Average)	I_v	5mA D.C.	90	200		μcd
		20mA D.C.		1200		μcd
		60mA Pk: 1 of 6 Duty Factor		740		μcd
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength [6]	λ_d			585		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 5mA		1.8		V
		I_F = 20mA		2.2	2.5	
		I_F = 60mA		3.1		
Reverse Current/Segment or D.P.	I_R	V_R = 6V		10		μA
Response Time [7]	t_r, t_f			90		ns
Temperature Coefficient of V_F/Segment or D.P.	V_F/°C			−2.0		mV/°C

GREEN 5082-7630/-7631/-7633/-7636

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment [5,8] (Digit Average)	I_v	10mA D.C.	150	300		μcd
		20mA D.C.		765		μcd
		60mA Pk: 1 of 6 Duty Factor		540		μcd
Peak Wavelength	λ_{PEAK}			565		nm
Dominant Wavelength [6]	λ_d			572		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 5mA		1.9		V
		I_F = 20mA		2.2	2.5	
		I_F = 60mA		2.9		
Reverse Current/Segment or D.P.	I_R	V_R = 6V		10		μA
Response Time [7]	t_r, t_f			90		ns
Temperature Coefficient of V_F/Segment or D.P.	ΔV_F/°C			−2.0		mV/°C

NOTES: 5. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
6. The dominant wavelength, λ_d, is derived from the C.I.E. Chromaticity Diagram and is that single wavelength which defines the color of the device.
7. Time for a 10% – 90% change of light intensity for step change in current.
8. Temperature coefficient of luminous intensity I_v/°C is determined by the formula:

$$I_{V_{T_A}} = I_{V_{25°C}} e^{[K (T_A - 25°C)]}.$$

Device	K
-7610 series	-.0131/°C
-7620 series	-.0112/°C
-7630 series	-.0104/°C

Operational Considerations

ELECTRICAL

The 5082-7600 series of display products are arrays of eight light emitting diodes which are optically magnified to form seven individual segments plus a decimal point.

The diodes in these displays utilize a Gallium Arsenide Phosphide junction on a Gallium Phosphide substrate to produce high efficiency red and yellow emission spectra and a Gallium Phosphide junction for the green. In the case of the red displays, efficiency is improved by at least a factor of 4 over the standard Gallium Arsenide Phosphide based technology. The use of Gallium Phosphide as the substrate does result in an internal dynamic resistance in the range of 12-48Ω. It is this resistance which causes the substantially higher forward voltage specifications in the new devices.

The user should be careful to scale the appropriate forward voltage from the V_F versus I_F curve, Figure 4, when designing for a particular forward current. Another way to obtain V_F would be to use the following formula:

$$V_F = V_{5mA} + R_S (I_F - 5mA)$$

where V_{5mA} and R_S are found in the following table:

Device	V_{5mA}	R_S
-7610 Series	1.65V	21Ω
-7620 Series	1.75V	25Ω
-7630 Series	1.85V	19Ω

Figure 1 relates refresh rate, f, and pulse duration, t_P, to a ratio which defines the maximum desirable operating peak current as a function of derated dc current, $I_{P\ MAX}/I_{DC\ MAX}$. To most effectively utilize Figure 1, perform the following steps:

1. Determine desired duty factor.
   Example: Four digit display, duty factor = 1/4
2. Determine desired refresh rate, f. Use duty factor to calculate pulse duration, t_P.
   Note: ft_P = Duty Factor
   Example: f=1 kHz; t_P=250 μsec
3. Enter Figure 1 at the calculated t_P. Move vertically to the refresh rate line and then record the corresponding value of $I_{P\ MAX}/I_{DC\ MAX}$.
   Example: At t_P=250 μsec and f=1 kHz,
   $I_{P\ MAX}/I_{DC\ MAX}$ = 4.0
4. From Figure 2, determine the value for $I_{DC\ MAX}$.
   Note: $I_{DC\ MAX}$ is derated above T_A=50°C
   Example: At T_A=70°C, $I_{DC\ MAX}$=12mA
5. Calculate $I_{P\ MAX}$ from $I_{P\ MAX}/I_{DC\ MAX}$ ratio and calculate I_{AVG} from I_P and duty factor.
   Example: I_P = (4.0) (12mA) = 48mA peak
   I_{AVG}=(1/4) (48mA) = 12mA average.

   The above calculations determine the maximum tolerable strobing conditions. Operation at a reduced peak current or duty factor is suggested to help insure even more reliable operation.

Refresh rates of 1kHz or faster provide the most efficient operation resulting in the maximum possible time average luminous intensity.

These displays may be operated in the strobed mode at currents up to 60mA peak. When operating at peak currents above 5mA for red and yellow or 10mA for green, there will be an improvement in the relative efficiency of the display (see Figure 3). Light output at higher currents can be calculated using the following relationship:

$$I_{V\ TIME\ AVG} = \left[\frac{I_{AVG}}{I_{AVG\ SPEC}}\right]\left[\frac{\eta I_{PEAK}}{\eta I_{PEAK\ SPEC}}\right]\left[I_{V\ SPEC}\right]$$

I_{AVG} = Operating point average current

$I_{AVG\ SPEC}$ = Average current for data sheet luminous intensity value, $I_{V\ SPEC}$

ηI_{PEAK} = Relative efficiency at operating peak current.

$\eta I_{PEAK\ SPEC}$ = Relative efficiency at data sheet peak current where luminous intensity $I_{V\ SPEC}$ is specified.

$I_{V\ SPEC}$ = Data sheet luminous intensity, specified at $I_{AVG\ SPEC}$ and $I_{PEAK\ SPEC}$.

Example: I_P = 40mA and I_{AVG} = 10mA:

$$I_{V\ TIME\ AVG} = \left(\frac{10mA}{5mA}\right)\left(\frac{1.58}{1}\right)(300\mu d) = 948\mu cd/seg.$$

CONTRAST ENHANCEMENT

The 5082-7600 series devices have been optimized for use in actual display systems. In order to maximum "ON-OFF" contrast, the bodies of the displays have been painted to match the appearance of an unilluminated segment. The emission wavelength of the red displays has been shifted from the standard GaAsP – 655nm to 635nm in order to provide an easier to read device.

All of the colored display products should be used in conjunction with contrast enhancing filters. Some suggested contrast filters: for red displays, Panelgraphic Scarlet Red 65 or Homalite 1670; for yellow displays, Panelgraphic Yellow 27 or Homalite (100-1720, 100-1726); for green, Panelgraphic Green 48 or Homalite (100-1440, 100-1425). Another excellent contrast enhancement material for all colors is the 3M light control film.

MECHANICAL

The 5082-7600 series devices are constructed utilizing a lead frame in a standard DIP package. The individual packages may be close-packed on 10.16mm (.4 in.) centers on a PC board. Also, the larger character height allows other character spacing options when desired. The leadframe has an integral seating plane which will hold the package approximately 1.52mm (.060 in.) above the PC board during standard soldering and flux removal operation. To optimize device performance, new materials are used that are limited to certain solvent materials for flux removal. It is recommended that only mixtures of Freon and alcohol be used for post solder vapor cleaning processes, with an immersion time in the vapors up to two minutes maximum. Suggested products are Freon TF, Freon TE, Genesolv DI-15 and Genesolv DE-15. Isoproponal, Ethanol or water may also be used for cleaning operations.

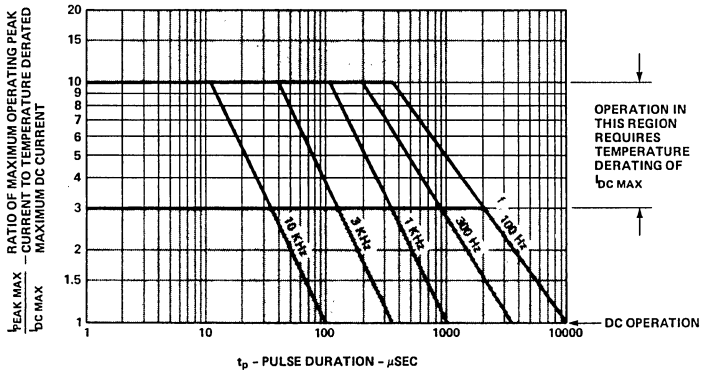


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration.

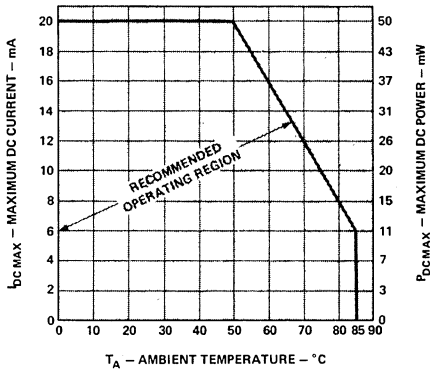


Figure 2. Maximum Allowable DC Current and DC Power Dissipation Per Segment as a Function of Ambient Temperature.

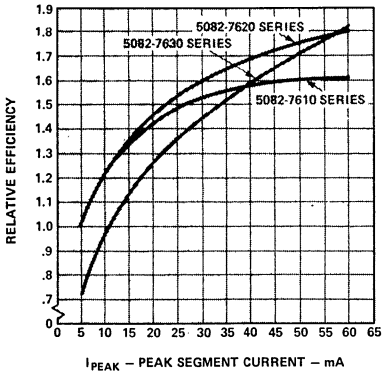


Figure 3. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current.

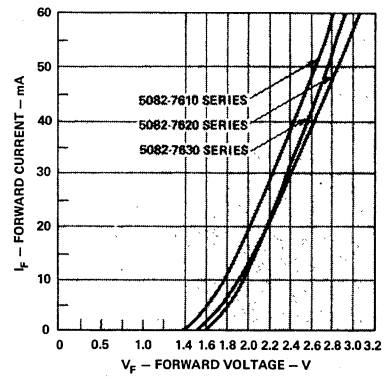


Figure 4. Forward Current vs. Forward Voltage Characteristic.

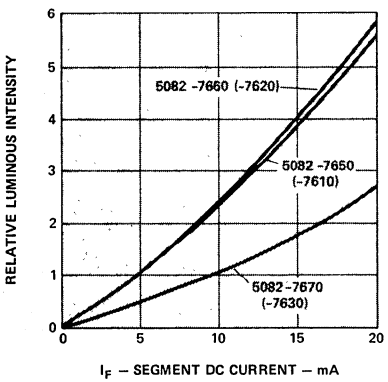


Figure 5. Relative Luminous Intensity vs. DC Forward Current

HEWLETT hp PACKARD

COMPONENTS

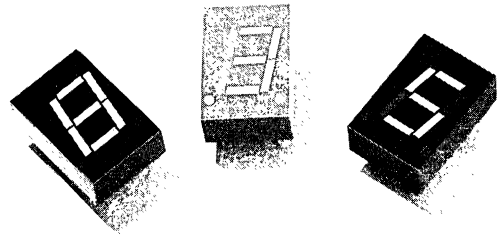
.43 INCH SEVEN SEGMENT DISPLAYS

HIGH EFFICIENCY RED • 5082-7650 SERIES
YELLOW • 5082-7660 SERIES
GREEN • 5082-7670 SERIES

TECHNICAL DATA APRIL 1979

Features

- **LARGE DIGIT**
  Viewing up to 6 meters (19.7 feet)
- **CHOICE OF 3 BRIGHT COLORS**
  High Efficiency Red
  Yellow
  Green
- **LOW CURRENT OPERATION**
  As Low as 3mA per Segment
  Designed for Multiplex Operation
- **EXCELLENT CHARACTER APPEARANCE**
  Evenly Lighted Segments
  Wide Viewing Angle
  Body Color Improves "Off" Segment Contrast
- **EASY MOUNTING ON PC BOARD OR SOCKETS**
  Industry Standard 7.62mm (.3") DIP Leads on 2.54mm (.1") Centers
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit within a Single Category
- **IC COMPATIBLE**
- **MECHANICALLY RUGGED**



Description

The 5082-7650, -7660, and -7670 series are large 10.92mm (.43 in.) Red, Yellow, and Green seven segment displays. These displays are designed for use in instruments, point of sale terminals, clocks, and appliances.

The -7650 and -7660 series devices utilize high efficiency LED chips which are made from GaAsP on a transparent GaP substrate.

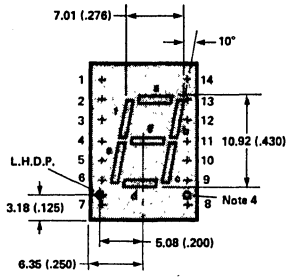
The -7670 series devices utilize chips made from GaP on a transparent GaP substrate.

Devices

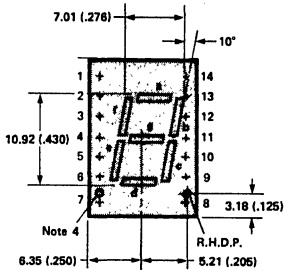
Part No. 5082-	Color	Description	Package Drawing
-7650	High Efficiency Red	Common Anode Left Hand Decimal	A
-7651	High Efficiency Red	Common Anode Right Hand Decimal	B
-7653	High Efficiency Red	Common Cathode Right Hand Decimal	C
-7656	High Efficiency Red	Universal Overflow ±1 Right Hand Decimal	D
-7660	Yellow	Common Anode Left Hand Decimal	A
-7661	Yellow	Comon Anode Right Hand Decimal	B
-7663	Yellow	Common Cathode Right Hand Decimal	C
-7666	Yellow	Universal Overflow ±1 Right Hand Decimal	D
-7670	Green	Common Anode Left Hand Decimal	A
-7671	Green	Common Anode Right Hand Decimal	B
-7673	Green	Common Cathode Right Hand Decimal	C
-7676	Green	Universal Overflow ±1 Right Hand Decimal	D

Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins, see internal diagram D.

Package Dimensions

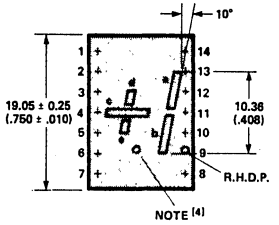


A

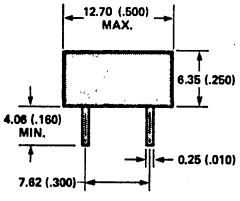


B,C

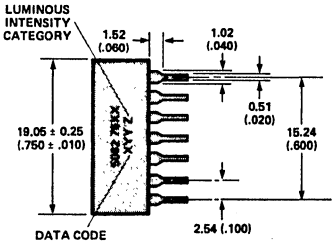
FRONT VIEW



D



END VIEW

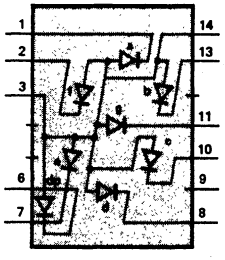


SIDE VIEW

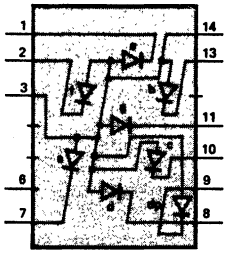
PIN	FUNCTION A -7650/-7660/-7670	B -7651/-7661/-7671	C -7653/-7663/-7673	D -7656/-7666/-7676
1	CATHODE-a	CATHODE-a	ANODE-a	CATHODE-d
2	CATHODE-f	CATHODE-f	ANODE-f	ANODE-d
3	ANODE[3]	ANODE[3]	CATHODE[6]	NO PIN
4	NO PIN	NO PIN	NO PIN	CATHODE-c
5	NO PIN	NO PIN	NO PIN	CATHODE-e
6	CATHODE-dp	NO CONN.[5]	NO CONN.[5]	ANODE-e
7	CATHODE-e	CATHODE-e	ANODE-e	ANODE-c
8	CATHODE-d	CATHODE-d	ANODE-d	ANODE-dp
9	NO CONN.[5]	CATHODE-dp	ANODE-dp	CATHODE-dp
10	CATHODE-c	CATHODE-c	ANODE-c	CATHODE-b
11	CATHODE-g	CATHODE-g	ANODE-g	CATHODE-a
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-b	ANODE-a
14	ANODE[3]	ANODE[3]	CATHODE[6]	ANODE-b

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathode.

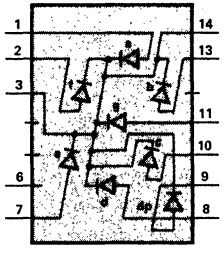
Internal Circuit Diagram



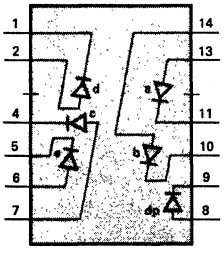
A



B



C



D

Absolute Maximum Ratings

DC Power Dissipation Per Segment or D.P.[1] (T_A=25°C) 50mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -40°C to +85°C
Peak Forward Current Per Segment or D.P[3] (T_A=25°C) 60mA
DC Forward Current Per Segment or D.P.[1,2] (T_A=25°C) 20mA
Reverse Voltage Per Segment or D.P. 6.0V
Lead Soldering Temperature ..... 260°C for 3 Sec
[1.59mm (1/16 inch) below seating plane[4]]

Notes: 1. See power derating curve (Fig.2). 2. Derate average current from 50°C at 0.4mA/°C per segment. 3. See Maximum Tolerable Segment Peak Current vs. Pulse Duration curve, (Fig. 1). 4. Clean only in water, isopropanol, ethanol, Freon TF or TE (or equivalent) and Genesolv DI-15 or DE-15 (or equivalent).

Electrical/Optical Characteristics at T_A=25°C

HIGH EFFICIENCY RED 5082-7650/-7651/-7653/-7656

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[5,8] (Digit Average)	I_v	5mA D.C.	135	300		µcd
		20mA D.C.		1720		µcd
		60mA Pk: 1 of 6 Duty Factor		970		µcd
Peak Wavelength	λ_{PEAK}			635		nm
Dominant Wavelength[6]	λ_d			626		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 5mA		1.7		V
		I_F = 20mA		2.0	2.5	
		I_F = 60mA		2.8		
Reverse Current/Segment or D.P.	I_R	V_R = 6V		10		µA
Response Time[7]	t_r, t_f			90		ns
Temperature Coefficient of V_F/Segment or D.P.	ΔV_F/°C			-2.0		mV/°C

YELLOW 5082-7660/-7661/-7663/-7666

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[5,8] (Digit Average)	I_v	5mA D.C.	100	250		µcd
		20mA D.C.		1500		µcd
		60mA Pk: 1 of 6 Duty Factor		925		µcd
Peak Wavelength	λ_{PEAK}			583		nm
Dominant Wavelength[6]	λ_d			585		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 5mA		1.8		V
		I_F = 20mA		2.2	2.5	
		I_F = 60mA		3.1		
Reverse Current/Segment or D.P.	I_R	V_R = 6V				µA
Response Time[7]	t_r, t_f			90		ns
Temperature Coefficient of V_F/Segment or D.P.	V_F/°C			-2.0		mV/°C

GREEN 5082-7670/-7671/-7673/-7676

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment[5,8] (Digit Average)	I_v	10mA D.C.	125	250		µcd
		20mA D.C.		640		µcd
		60mA Pk: 1 of 6 Duty Factor		450		µcd
Peak Wavelength	λ_{PEAK}			565		nm
Dominant Wavelength[6]	λ_d			572		nm
Forward Voltage/Segment or D.P.	V_F	I_F = 10mA		1.9		V
		I_F = 20mA		2.2	2.5	
		I_F = 60mA		2.9		
Reverse Current/Segment or D.P.	I_F	V_R = 6V		10		µA
Response Time[7]	t_r, t_f			90		ns
Temperature Coefficient of V_F/Segment or D.P.	ΔV_F/°C			-2.0		mV/°C

NOTES:

5. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
6. The dominant wavelength, λ_d, is derived from the C.I.E. Chromaticity Diagram and is that single wavelength which defines the color of the device.
7. Time for a 10% – 90% change of light intensity for step change in current.
8. Temperature coefficient of luminous intensity I_v/°C is determined by the formula: $I_{V_{T_A}} = I_{V_{25°C}} e^{[K (T_A - 25°C)]}$.

DEVICE	K
-7650 Series	-.0131/°C
-7660 Series	-.0112/°C
-7670 Series	-.0104/°C

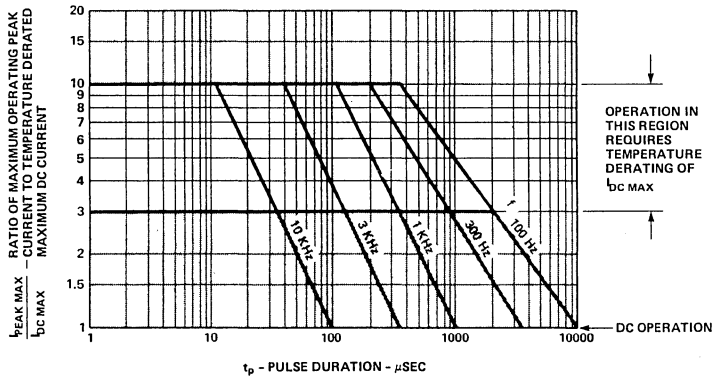


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration.

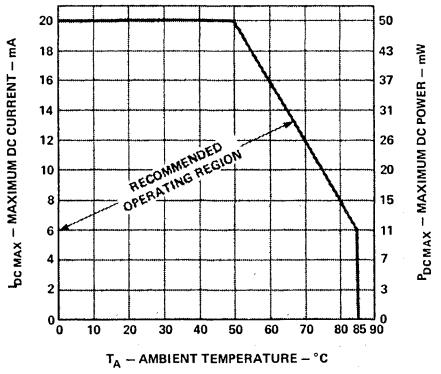


Figure 2. Maximum Allowable DC Current and DC Power Dissipation Per Segment as a Function of Ambient Temperature.

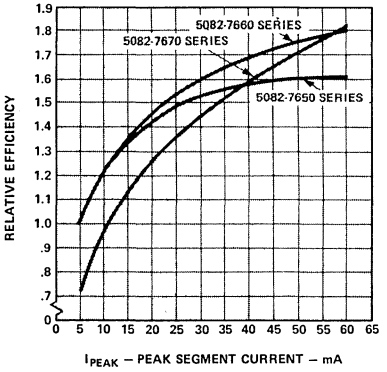


Figure 3. Relative Luminous Efficiency (Luminous Intensity per Unit Current) vs. Peak Segment Current.

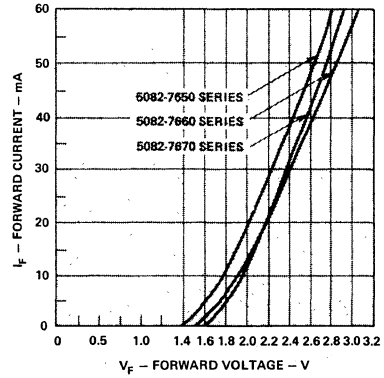


Figure 4. Forward Current vs. Forward Voltage Characteristic.

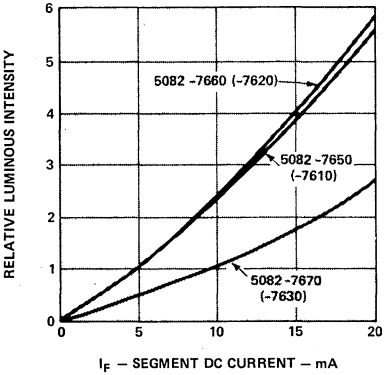


Figure 5. Relative Luminous Intensity vs. DC Forward Current

Operational Considerations

ELECTRICAL

The 5082-7600 series of display products are arrays of eight light emitting diodes which are optically magnified to form seven individual segments plus a decimal point.

The diodes in these displays utilize a Gallium Arsenide Phosphide junction on a Gallium Phosphide substrate to produce high efficiency red and yellow emission spectra and a Gallium Phosphide junction for the green. In the case of the red displays, efficiency is improved by at least a factor of 4 over the standard Gallium Arsenide Phosphide based technology. The use of Gallium Phosphide as the substrate does result in an internal dynamic resistance in the range of 12-48Ω. It is this resistance which causes the substantially higher forward voltage specifications in the new devices.

The user should be careful to scale the appropriate forward voltage from the V_F versus I_F curve, Figure 4, when designing for a particular forward current. Another way to obtain V_F would be to use the following formula:

$$V_F = V_{5mA} + R_S (I_F - 5mA)$$

where V_{5mA} and R_S are found in the following table:

Device	V_{5mA}	R_S
-7650 Series	1.65V	21Ω
-7660 Series	1.75V	25Ω
-7670 Series	1.85V	19Ω

Figure 1 relates refresh rate, f, and pulse duration, t_P, to a ratio which defines the maximum desirable operating peak current as a function of derated dc current, $I_{P\ MAX}/I_{DC\ MAX}$. To most effectively utilize Figure 1, perform the following steps:

1. Determine desired duty factor.
   Example: Four digit display, duty factor = 1/4
2. Determine desired refresh rate, f. Use duty factor to calculate pulse duration, t_P.
   Note: ft_P = Duty Factor
   Example: f=1 kHz; t_P=250 μsec
3. Enter Figure 1 at the calculated t_P. Move vertically to the refresh rate line and then record the corresponding value of $I_{P\ MAX}/I_{DC\ MAX}$.
   Example: At t_P=250 μsec and f=1 kHz,
   $I_{P\ MAX}/I_{DC\ MAX}$ = 4.0
4. From Figure 2, determine the value for $I_{DC\ MAX}$.
   Note: $I_{DC\ MAX}$ is derated above T_A=50° C
   Example: At T_A=70° C, $I_{DC\ MAX}$=12mA
5. Calculate $I_{P\ MAX}$ from $I_{P\ MAX}/I_{DC\ MAX}$ ratio and calculate I_{AVG} from I_P and duty factor.
   Example: I_P = (4.0) (12mA) = 48mA peak
   I_{AVG}=(1/4) (48mA) = 12mA average.

   The above calculations determine the maximum tolerable strobing conditions. Operation at a reduced peak current or duty factor is suggested to help insure even more reliable operation.

Refresh rates of 1kHz or faster provide the most efficient operation resulting in the maximum possible time average luminous intensity.

These displays may be operated in the strobed mode at currents up to 60mA peak. When operating at peak currents above 5mA for red and yellow or 10mA for green, there will be an improvement in the relative efficiency of the display (see Figure 3). Light output at higher currents can be calculated using the following relationship:

$$I_{V\ TIME\ AVG} = \left[\frac{I_{AVG}}{I_{AVG\ SPEC}}\right]\left[\frac{\eta_{I\ PEAK}}{\eta_{I\ PEAK\ SPEC}}\right]\left[I_{V\ SPEC}\right]$$

I_{AVG} = Operating point average current

$I_{AVG\ SPEC}$ = Average current for data sheet luminous intensity value, $I_{V\ SPEC}$

η_{IPEAK} = Relative efficiency at operating peak current.

$\eta_{IPEAK\ SPEC}$ = Relative efficiency at data sheet peak current where luminous intensity $I_{V\ SPEC}$ is specified.

$I_{V\ SPEC}$ = Data sheet luminous intensity, specified at $I_{AVG\ SPEC}$ and $I_{PEAK\ SPEC}$.

Example: I_P = 40mA and I_{AVG} = 10mA:

$$I_{V\ TIME\ AVG} = \left(\frac{10mA}{5mA}\right)\left(\frac{1.58}{1}\right)(300\mu d) = 948\mu cd/seg.$$

CONTRAST ENHANCEMENT

The 5082-7600 series devices have been optimized for use in actual display systems. In order to maximum "ON-OFF" contrast, the bodies of the displays have been painted to match the appearance of an unilluminated segment. The emission wavelength of the red displays has been shifted from the standard GaAsP – 655nm to 635nm in order to provide an easier to read device.

All of the colored display products should be used in conjunction with contrast enhancing filters. Some suggested contrast filters: for red displays, Panelgraphic Scarlet Red 65 or Homalite 1670; for yellow displays, Panelgraphic Amber 23 or Homalite (100-1720, 100-1726); for green, Panelgraphic Green 48 or Homalite (100-1440, 100-1425). Another excellent contrast enhancement material for all colors is the 3M light control film.

MECHANICAL

The 5082-7600 series devices are constructed utilizing a lead frame in a standard DIP package. The individual packages may be close-packed on 12.7mm (.5 in.) centers on a PC board. Also, the larger character height allows other character spacing options when desired. The leadframe has an integral seating plane which will hold the package approximately 1.52mm (.060 in.) above the PC board during standard soldering and flux removal operation. To optimize device performance, new materials are used that are limited to certain solvent materials for flux removal. It is recommended that only mixtures of Freon and alcohol be used for post solder vapor cleaning processes, with an immersion time in the vapors up to two minutes maximum. Suggested products are Freon TF, Freon TE, Genesolv DI-15 and Genesolv DE-15. Isoproponal, Ethanol or water may also be used for cleaning operations.

HEWLETT hp PACKARD

COMPONENTS

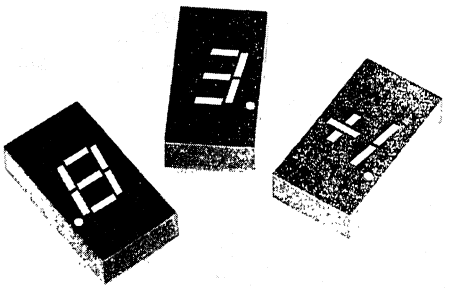
0.3 INCH RED SEVEN SEGMENT DISPLAY

5082-7730 SERIES
5082-7740

TECHNICAL DATA APRIL 1979

Features

- **5082-7730**
  Common Anode
  Left Hand D.P.
- **5082-7731**
  Common Anode
  Right Hand D.P.
- **5082-7736**
  Polarity and Overflow Indicator
  Universal Pinout
  Right Hand D.P.
- **5082-7740**
  Common Cathode
  Right Hand D.P.
- **EXCELLENT CHARACTER APPEARANCE**
  Continuous Uniform Segments
  Wide Viewing Angle
  High Contrast
- **IC COMPATIBLE**
  1.6V dc per Segment
- **STANDARD 0.3" DIP LEAD CONFIGURATION**
  PC Board or Standard Socket Mountable
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit withing a Single Category



Description

The HP 5082-7730/7740 series devices are common anode LED displays. The series includes a left hand and a right hand decimal point numeric display as well as a polarity and overflow indicator. The large 7.62 mm (0.3 in.) high character size generates a bright, continuously uniform seven segment display. Designed for viewing distances of up to 3 meters (9.9 feet), these single digit displays provide a high contrast ratio and a wide viewing angle.

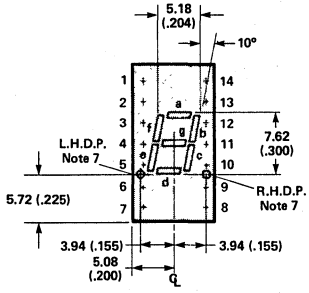
The 5082-7730 series devices utilize a standard 7.62 mm (0.3 in.) dual-in-line package configuration that permits mounting on PC boards or in standard IC sockets. Requiring a low forward voltage, these displays are inherently IC compatible, allowing for easy integration into electronic instrumentation, point of sale terminals, TVs, radios, and digital clocks.

Devices

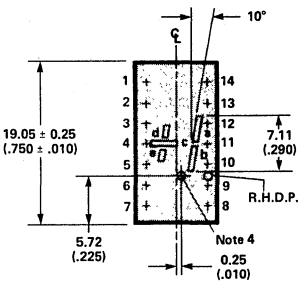
Part No. 5082-	Description	Package Drawing
7730	Common Anode Left Hand Decimal	A
7731	Common Anode Right Hand Decimal	B
7736	Universal Overflow ±1 Right Hand Decimal	C
7740	Common Cathode Right Hand Decimal	D

Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram C.

Package Dimensions

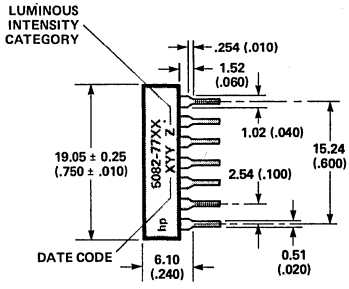


A,B,D

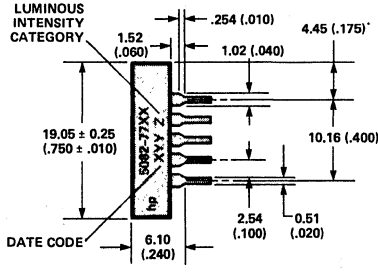


C

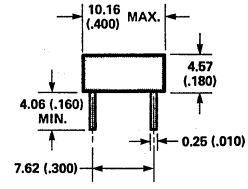
PIN	FUNCTION A -7730	B -7731	C -7736	D -7740
1	CATHODE-a	CATHODE-a	ANODE-d	CATHODE[6]
2	CATHODE-f	CATHODE-f	NO PIN	ANODE-f
3	ANODE[3]	ANODE[3]	CATHODE-d	ANODE-g
4	NO PIN	NO PIN	CATHODE-c	ANODE-e
5	NO PIN	NO PIN	CATHODE-e	ANODE-d
6	CATHODE-dp	NO CONN.[5]	ANODE-e	CATHODE[6]
7	CATHODE-e	CATHODE-e	ANODE-c	ANODE-dp
8	CATHODE-d	CATHODE-d	ANODE-dp	ANODE-c
9	NO CONN.[5]	CATHODE-dp	NO PIN	ANODE-b
10	CATHODE-c	CATHODE-c	CATHODE-dp	ANODE-a
11	CATHODE-g	CATHODE-g	CATHODE-b	
12	NO PIN	NO PIN	CATHODE-a	
13	CATHODE-b	CATHODE-b	ANODE-a	
14	ANODE[3]	ANODE[3]	ANODE-b	



A,B,C
SIDE



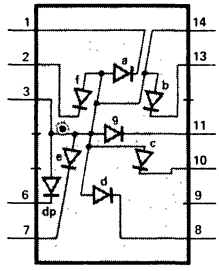
D
SIDE



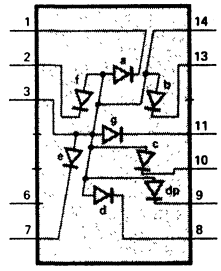
A,B,C,D
END

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathode.
7. See part number table for L.H.D.P. and R.H.D.P. designation.

Internal Circuit Diagram



A



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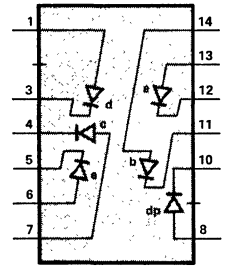
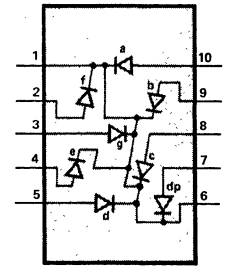


C



D

Absolute Maximum Ratings

DC Power Dissipation Per Segment or D.P.[1] (T_A=25°C) 42mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -40°C to +85°C
Peak Forward Current Per Segment or D.P.[3] (T_A=25°C) 150mA
Average Forward Current Per Segment or D.P.[1,2] (T_A=25°C) 25mA
Reverse Voltage Per Segment or D.P. 6.0V
Lead Soldering Temperature ..... 260°C for 3 Sec
[1.59mm (1/16 inch) below seating plane[4]]

Notes: 1. See power derating curve (Fig.2). 2. Derate DC current from 50°C at 0.43mA/°C per segment. 3. See Fig. 1 to establish pulsed operating conditions. 4. Clean only in water, isopropanol, ethanol, Freon TF or TE (or equivalent) and Genesolv DI-15 or DE-15 (or equivalent).

Electrical/Optical Characteristics at T_A=25°C

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment [2,4] (Digit Average)	I_V	I_{PEAK} = 100mA 10% Duty Cycle		200		μcd
		I_F = 20mA	100	350		
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength [2]	λ_d			640		nm
Forward Voltage, any Segment or D.P.	V_F	I_F = 20mA		1.6	2.0	V
Reverse Current, any Segment or D.P.	I_R	V_R = 6V		10		μA
Rise and Fall Time [3]	t_r, t_f			10		ns
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$			-2.0		mV/°C

Notes:
1. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
3. Time for a 10% - 90% change of light intensity for step change in current.
4. Temperature coefficient of luminous intensity I_V/°C is determined by the formula: $I_{V_{T_A}} = I_{V_{25°C}} e^{[(-.0188/°C)(T_A - 25°C)]}$.

Operational Considerations

ELECTRICAL

The 5082-7730/7740 series display is composed of eight light emitting diodes optically magnified to form seven individual segments and decimal point.

The diodes are made of GaAsP (Gallium Arsenide Phosphide) junction on a GaAs substrate. Diode turn-on voltage is approximately 1.55 volts and typical forward diode resistance is 5 ohms. For strobing at peak currents a user should take this forward resistance into account.

Typical forward voltage may be scaled from Figure 4 or calculated from the following formula:

$V_F = 1.55V + (3\Omega \times I_{PEAK})$

Figure 1 relates refresh rate, f, and pulse duration, t_P, to a ratio which defines the maximum desirable operating peak current as a function of derated dc current, $I_{P\ MAX}/I_{DC\ MAX}$. To most effectively utilize Figure 1, perform the following steps:

1. Determine desired duty factor.
   Example: Four digit display, duty factor = 1/4.
2. Determine desired refresh rate, f. Use duty factor to calculate pulse duration, t_P. Note: ft_P = Duty Factor
   Example: f = 1kHz; t_P = 250 μsec.
3. Enter Figure 1 at the calculated t_P. Move vertically to the refresh rate line and then record the corresponding value of $I_{P\ MAX}/I_{DC\ MAX}$.
   Example: At t_P = 250 μsec and f=1kHz,
   $I_{P\ MAX}/I_{DC\ MAX}$ = 4.0
4. From Figure 2, determine the value for $I_{DC\ MAX}$.
   Note: $I_{DC\ MAX}$ is derated above T_A=50°C
   Example: At T_A=70°C, $I_{DC\ MAX}$ = 16.4mA.
5. Calculate $I_{P\ MAX}$ from $I_{P\ MAX}/I_{DC\ MAX}$ ratio and calculate I_{AVG} from I_P and duty factor.
   Example: I_P=(4.0) (16.4mA) = 65.6mA peak
   I_{AVG}=(1/4) (65.6mA) = 16.4mA average.

   The above calculations determine the maximum tolerable strobing conditions. Operation at a reduced peak current or duty factor is suggested to help insure even more reliable operation.

Refresh rates of 1kHz or faster provide the most efficient operation reulting in the maximum possible time average luminous intensity.

This display may be operated at various peak currents (see Figure 3). Light output for a selected peak current can be calculated as follows:

$$I_{V\ TIME\ AVG} = \left[\frac{I_{AVG}}{I_{AVG\ SPEC}}\right]\left[\frac{\eta_{IPEAK}}{\eta_{IPEAK\ SPEC}}\right]\left[I_{V\ SPEC}\right]$$

I_{AVG} = Operating point average current
$I_{AVG\ SPEC}$ = Average current for data sheet luminous intensity value, $I_{V\ SPEC}$
η_{IPEAK} = Relative efficiency at operating peak current
$\eta_{IPEAK\ SPEC}$ = Relative efficiency at data sheet peak current where luminous intensity $I_{V\ SPEC}$ is specified.
$I_{V\ SPEC}$ = Data sheet luminous intensity, specified at $I_{AVG\ SPEC}$ and $I_{PEAK\ SPEC}$

CONTRAST ENHANCEMENT

The 5082-7730/7740 series display may be effectively filtered using one of the following filter products: Homalite H100-1605: H 100-1804 (purple); Panelgraphic Ruby Red 60: Dark Red 63: Purple 90; Plexiglas 2423; 3M Brand Light Control Film for daylight viewing. For further information see Application Note 964.

MECHANICAL

The 5082-7730/7740 series devices are constructed utilizing a lead frame in a standard DIP package. The individual packages may be close-packed on 10.16mm (.4 in.) centers on a PC board. Also, the larger character height allows other character spacing options when desired. The lead frame has an integral seating plane which will hold the package approximately 1.52mm (.060 in.) above the PC board during standard soldering and flux removal operation. To optimize device performance, new materials are used that are limited to certain solvent materials for flux removal. It is recommended that only mixtures of Freon and alcohol be used for post solder vapor cleaning processes, with an immersion time in the vapors up to two minutes maximum. Suggested products are Freon TF, Freon TE, Genesolv DI-15 and Genesolv DE-15. Isoproponal, Ethanol or water may also be used for cleaning operations.

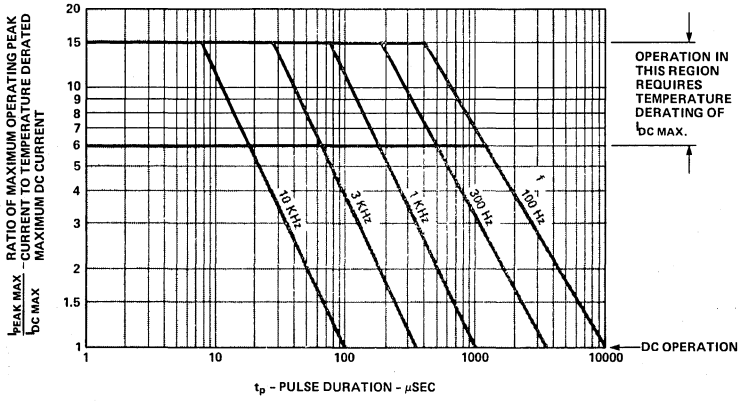


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration.

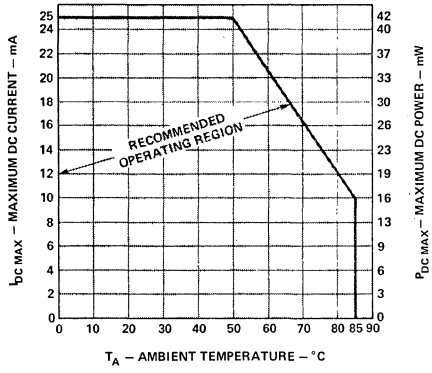


Figure 2. Maximum Allowable DC Current and DC Power Dissipation per Segment as a Function of Ambient Temperature.

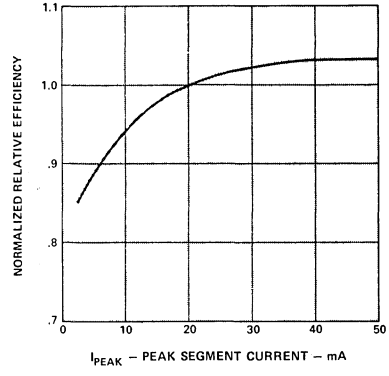


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current per Segment.

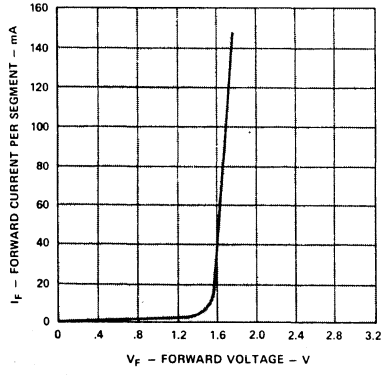


Figure 4. Forward Current vs. Forward Voltage.

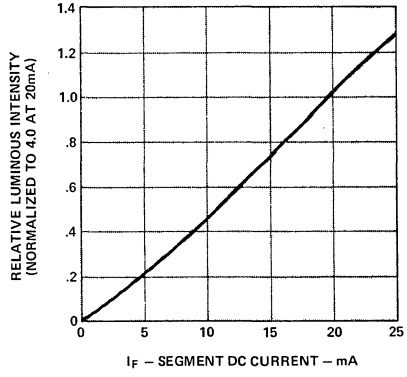


Figure 5. Relative Luminous Intensity vs. DC Forward Current

HEWLETT hp PACKARD
COMPONENTS

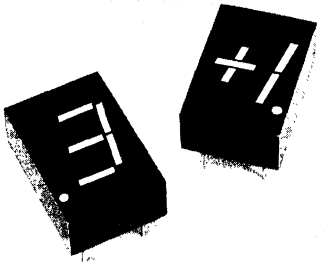
.43 INCH RED SEVEN SEGMENT DISPLAY

5082-7750 SERIES
5082-7760

TECHNICAL DATA APRIL 1979

Features

- **5082-7750**
  Common Anode
  Left Hand D.P.
- **5082-7751**
  Common Anode
  Right Hand D.P.
- **5082-7756**
  Polarity and Overflow Indicator
  Universal Pinout
  Right Hand D.P.
- **5082-7760**
  Common Cathode
  Right Hand D.P.
- **LARGE DIGIT**
  Viewing Up to 6 Meters (19.7 Feet)
- **EXCELLENT CHARACTER APPEARANCE**
  Continuous Uniform Segments
  Wide Viewing Angle
  High Contrast
- **IC COMPATIBLE**
- **STANDARD 7.62mm (.3 in.) DIP LEAD CONFIGURATION**
  PC Board or Standard Socket Mountable
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit within a Single Category



Description

The 5082-7750/7760 series are large 10.92mm (.43 in.) GaAsP LED seven segment displays. Designed for viewing distances up to 6 meters (19.7 feet), these single digit displays provide a high contrast ratio and a wide viewing angle.

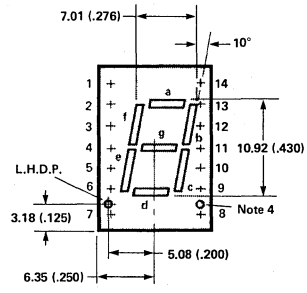
These devices utilize a standard 7.62mm (.3 in.) dual-in-line package configuration that permits mounting on PC boards or in standard IC sockets. Requiring a low forward voltage, these displays are inherently IC compatible, allowing for easy integration into electronic instrumentation, point of sale terminals, TVs, radios, and digital clocks.

Devices

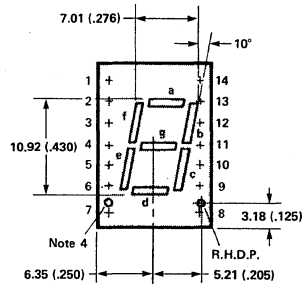
Part No. 5082-	Description	Package Drawing
-7750	Common Anode Left Hand Decimal	A
-7751	Common Anode Right Hand Decimal	B
-7756	Universal Overflow ±1 Right Hand Decimal	C
-7760	Common Cathode Right Hand Decimal	D

Note: Universal pinout brings the anode and cathode of each segment's LED out to separate pins. See internal diagram C.

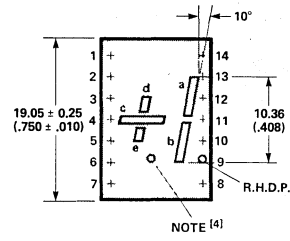
Package Dimensions



A

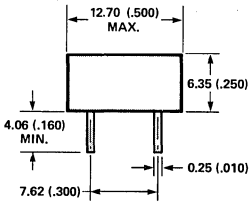


B,D

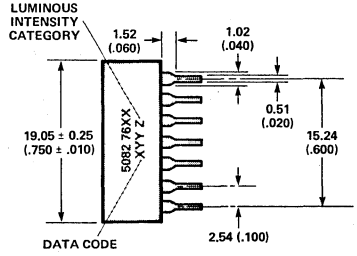


C

FRONT VIEW



END VIEW

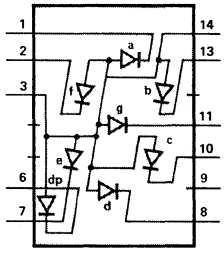


SIDE VIEW

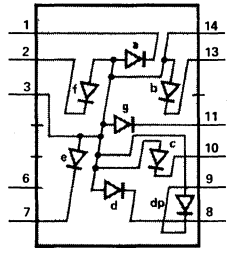
PIN	FUNCTION			
	A -7750	B -7751	C -7756	D -7760
1	CATHODE-a	CATHODE-a	CATHODE-d	ANODE-a
2	CATHODE-f	CATHODE-f	ANODE-d	ANODE-f
3	ANODE[3]	ANODE[3]	NO PIN	CATHODE[6]
4	NO PIN	NO PIN	CATHODE-c	NO PIN
5	NO PIN	NO PIN	CATHODE-e	NO PIN
6	CATHODE-dp	NO CONN.[5]	ANODE-e	NO CONN.[5]
7	CATHODE-e	CATHODE-e	ANODE-c	ANODE-e
8	CATHODE-d	CATHODE-d	ANODE-dp	ANODE-d
9	NO CONN.[5]	CATHODE-dp	CATHODE-dp	ANODE-dp
10	CATHODE-c	CATHODE-c	CATHODE-b	ANODE-c
11	CATHODE-g	CATHODE-g	CATHODE-a	ANODE-g
12	NO PIN	NO PIN	NO PIN	NO PIN
13	CATHODE-b	CATHODE-b	ANODE-a	ANODE-b
14	ANODE[3]	ANODE[3]	ANODE-b	CATHODE[6]

NOTES:
1. Dimensions in millimeters and (inches).
2. All untoleranced dimensions are for reference only.
3. Redundant anodes.
4. Unused dp position.
5. See Internal Circuit Diagram.
6. Redundant cathodes.

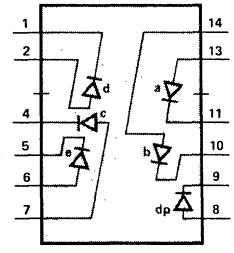
Internal Circuit Diagram



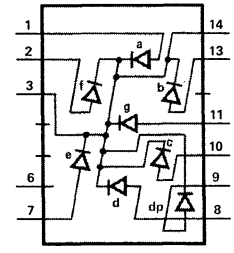
A



B



C



D

Absolute Maximum Ratings

DC Power Dissipation Per Segment or D.P.[1] (T_A=25°C) 42mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -40°C to +85°C
Peak Forward Current Per Segment or D.P[3] (T_A=25°C) 150mA
DC Forward Current Per Segment or D.P.[1,2] (T_A=25°C) 25mA
Reverse Voltage Per Segment or D.P. 6.0V
Lead Soldering Temperature ..... 260°C for 3 Sec
[1.59mm (1/16 inch) below seating plane[4]]

Notes: 1. See power derating curve (Fig.2). 2. Derate average current from 50°C at 0.43mA/°C per segment. 3. See Maximum Tolerable Segment Peak Current vs. Pulse Duration curve, (Fig. 1). 4. Clean only in water, isopropanol, ethanol, Freon TF or TE (or equivalent) and Genesolv DI-15 or DE-15 (or equivalent).

Electrical/Optical Characteristics at T_A=25°C

Description	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment [2,4]	I_V	I_{PEAK} = 100mA 12.5% Duty Cycle		350		μcd
(Digit Average)		I_F = 20mA	150	400		
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength [2]	λ_d			645		nm
Forward Voltage, any Segment or D.P.	V_F	I_F = 20mA		1.6	2.0	V
Reverse Current, any Segment or D.P.	I_R	V_R = 6V		10		μA
Rise and Fall Time [3]	t_r, t_f			10		ns
Temperature Coefficient of Forward Voltage	$\Delta V_F/°C$			−2.0		mV/°C

Notes:
1. The digits are categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
2. The dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
3. Time for a 10% - 90% change of light intensity for step change in current.
4. Temperature coefficient of luminous intensity I_V/°C is determined by the formula: $I_{V_{TA}} = I_{V25°C}\, e^{[(-.0188/°C)\,(T_A - 25°C)]}$

Operational Considerations

ELECTRICAL

The 5082-7750/7760 series display is composed of eight light emitting diodes optically magnified to form seven individual segments and decimal point.

The diodes are made of GaAsP (Gallium Arsenide Phosphide) junction on a GaAs substrate. Diode turn-on voltage is approximately 1.55 volts and typical forward diode resistance is 5 ohms. For strobing at peak currents a user should take this forward resistance into account.

Typical forward voltage may be scaled from Figure 4 or calculated from the following formula:

$V_F = 1.55V + (3\Omega \times I_{PEAK})$

Figure 1 relates refresh rate, f, and pulse duration, t_P, to a ratio which defines the maximum desirable operating peak current as a function of derated dc current, $I_{P\ MAX}/I_{DC\ MAX}$. To most effectively utilize Figure 1, perform the following steps:

1. Determine desired duty factor.
   Example: Four digit display, duty factor = 1/4.
2. Determine desired refresh rate, f. Use duty factor to calculate pulse duration, t_P. Note: ft_P = Duty Factor
   Example: f = 1kHz; t_P = 250 μsec.
3. Enter Figure 1 at the calculated t_P. Move vertically to the refresh rate line and then record the corresponding value of $I_{P\ MAX}/I_{DC\ MAX}$.
   Example: At t_P = 250 μsec anf f=1kHz,
   $I_{P\ MAX}/I_{DC\ MAX}$ = 4.0
4. From Figure 2, determine the value for $I_{DC\ MAX}$.
   Note: $I_{DC\ MAX}$ is derated above T_A=50°C
   Example: At T_A=70°C, $I_{DC\ MAX}$ = 16.4mA.
5. Calculate $I_{P\ MAX}$ from $I_{P\ MAX}/I_{DC\ MAX}$ ratio and calculate I_{AVG} from I_P and duty factor.
   Example: I_P=(4.0) (16.4mA) = 65.6mA peak
   I_{AVG}=(1/4) (65.6mA) = 16.4mA average.

   The above calculations determine the maximum tolerable strobing conditions. Operation at a reduced peak current or duty factor is suggested to help insure even more reliable operation.

Refresh rates of 1kHz or faster provide the most efficient operation reulting in the maximum possible time average luminous intensity.

This display may be operated at various peak currents (see Figure 3). Light output for a selected peak current may be calculated from the 20mA value using the following formula:

$$I_v = (I_{v\ 20mA})\ \eta I_{PEAK} \left(\frac{I_{F\ AVG}}{20mA}\right)$$

Where: I_v = Luminous Intensity at desired I_{AVG}

$I_{v\ 20mA}$ = Luminous Intensity at I_F = 20mA

I_{AVG} = Average Forward Current per segment = (I_{PEAK} × Duty Factor)

ηI_{PEAK} = Relative Efficiency Factor at Peak Operating Forward Current from Figure 3.

CONTRAST ENHANCEMENT

The 5082-7750/7760 series display may be effectively filtered using one of the following filter products: Homalite H 100-1605 or H 100-1804 Purple; Panelgraphic Ruby Red 60, Dark Red 63 or Purple 90; Plexiglas 2423; 3M Brand Light Control Film for daylight viewing.

MECHANICAL

The 5082-7750/7760 series devices are constructed utilizing a lead frame in a standard DIP package. The individual packages may be close-packed on 12.7mm (.5 in.) centers on a PC board. Also, the larger character height allows other character spacing options when desired. The lead frame has an integral seating plane which will hold the package approximately 1.52mm (.060 in.) above the PC board during standard soldering and flux removal operation. To optimize device performance, new materials are used that are limited to certain solvent materials for flux removal. It is recommended that only mixtures of Freon and alcohol be used for post solder vapor cleaning processes, with an immersion time in the vapors up to two minutes maximum. Suggested products are Freon TF, Freon TE, Genesolv DI-15 and Genesolv DE-15. Isoproponal, Ethanol or water may also be used for cleaning operations.

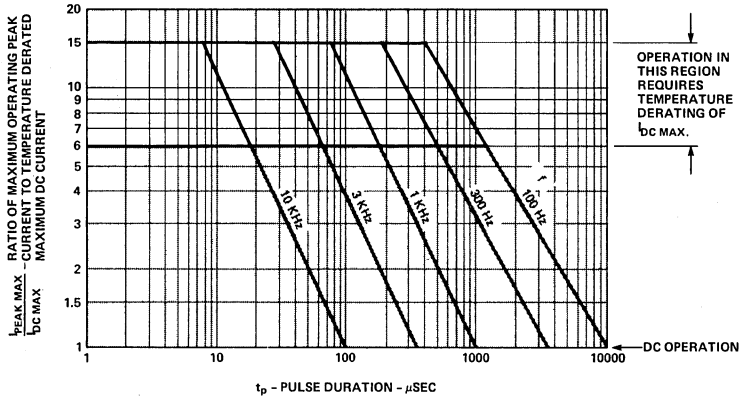


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration.

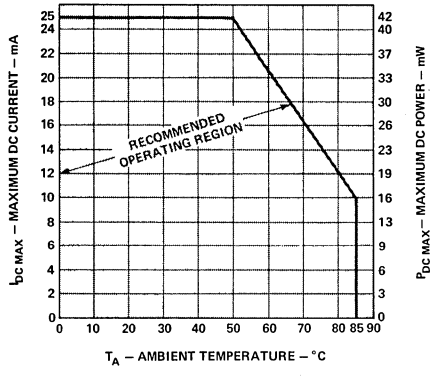


Figure 2. Maximum Allowable DC Current and DC Power Dissipation per Segment as a Function of Ambient Temperature.

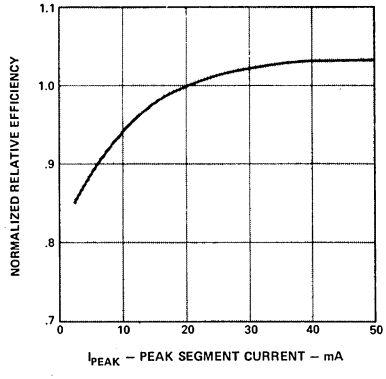


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current per Segment.

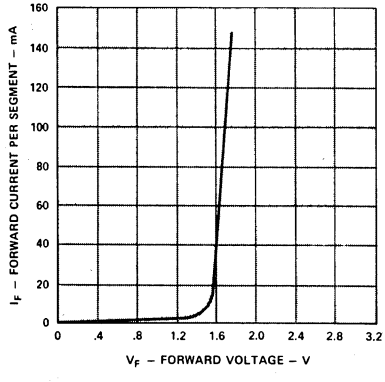


Figure 4. Forward Current versus Forward Voltage.

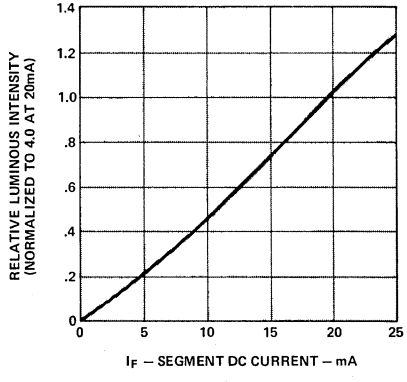


Figure 5. Relative Luminous Intensity vs. D.C. Forward Current.

HEWLETT hp PACKARD

COMPONENTS

SOLID STATE NUMERIC INDICATOR (7 Segment Monolithic)

5082-7400 SERIES

TECHNICAL DATA APRIL 1979

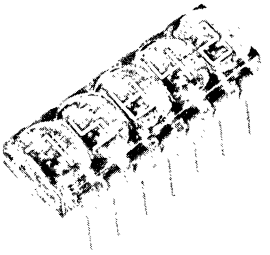
Features

- **ULTRA LOW POWER**
  Excellent Readability at Only 500 µA Average per Segment
- **CONSTRUCTED FOR STROBED OPERATION**
  Minimizes Lead Connections
- **STANDARD DIP PACKAGE**
  End Stackable
  Integral Red Contrast Filter
  Rugged Construction
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit within a Single Category
- **IC COMPATIBLE**

Description

The HP 5082-7400 series are 2.79mm (.11"), seven segment GaAsP numeric indicators packaged in 3, 4, and 5 digit end-stackable clusters. An integral magnification technique increases the luminous intensity, thereby making ultra-low power consumption possible. Options include either the standard lower right hand decimal point or a centered decimal point for increased legibility in multi-cluster applications.

Applications include hand-held calculators, portable instruments, digital thermometers, or any other product requiring low power, low cost, minimum space, and long lifetime indicators.



Device Selection Guide

Digits per Cluster	Configuration: Device		Part Number: Center Decimal Point	Part Number: Right Decimal Point
3 (right)			5082-7402	5082-7412
3 (left)			5082-7403	5082-7413
4			5082-7404	5082-7414
5			5082-7405	5082-7415

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment (Duration < 1 msec)	I_{PEAK}		110	mA
Average Current per Segment	I_{AVG}		5	mA
Power Dissipation per Digit [1]	P_D		80	mW
Operating Temperature, Ambient	T_A	–40	75	°C
Storage Temperature	T_S	–40	100	°C
Reverse Voltage	V_R		5	V

NOTES: 1. At 25°C; derate 1mW/°C above 25°C ambient. 2. See Mechanical Section for recommended flux removal solvents.

Electrical /Optical Characteristics at T_A=25°C

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp [3,4] (Time Averaged)	I_V	I_{AVG} = 1mA (I_{PK} = 10mA duty cycle = 10%)	5	20		µcd
Peak Wavelength	λ_{PEAK}			655		nm
Forward Voltage/Segment or dp	V_F	I_F = 10mA		1.6	2.0	V
Reverse Current/Segment or dp	I_R	V_R = 5V			100	µA
Rise and Fall Time [5]	t_r, t_f			10		ns

NOTES: 3. The digits are categorized for luminous intensity. Intensity categories are designated by a letter located on the back side of the package. 4. Operation at Peak Currents less than 5mA is not recommended. 5. Time for a 10%-90% change of light intensity for step change in current.

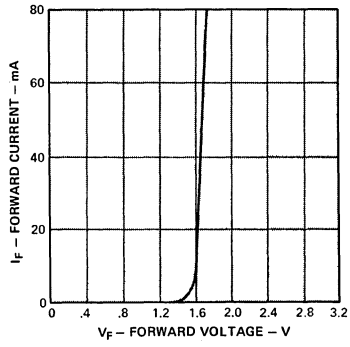


Figure 1. Forward Current vs. Forward Voltage.

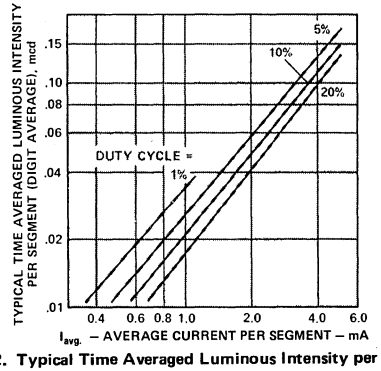


Figure 2. Typical Time Averaged Luminous Intensity per Segment (Digit Average) vs. Average Current per Segment.

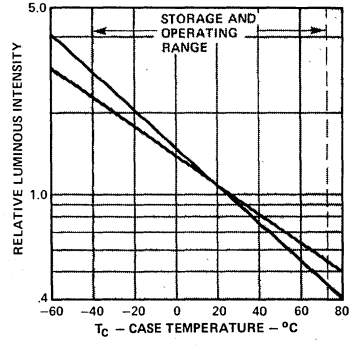


Figure 3. Relative Luminous Intensity vs. Case Temperature at Fixed Current Level.

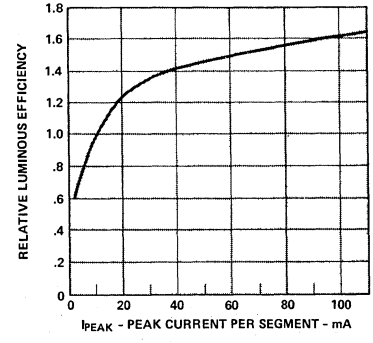


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment.

Package Description

NOTES: 1. Dimensions in millimeters and (inches).
2. Tolerances on all dimensions are ±0.038mm (±.015 in.) unless otherwise noted.

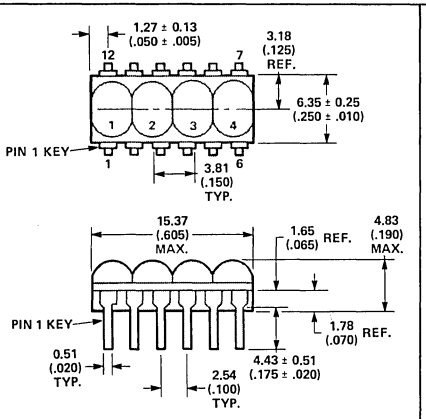


Figure 5. 5082-7402/-7403/-7404/ -7412/-7413/-7414

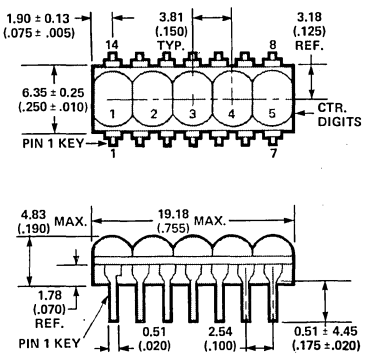
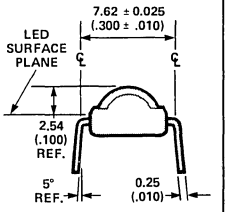


Figure 6. 5082-7405/7415



All Devices

Magnified Character Font Description

DIMENSIONS IN MILLIMETERS AND (INCHES).

DEVICES

5082-7402
5082-7403
5082-7404
5082-7405

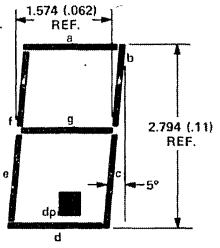


Figure 7. Center Decimal Point Configuration.

DIMENSIONS IN MILLIMETERS AND (INCHES).

DEVICES

5082-7412
5082-7413
5082-7414
5082-7415

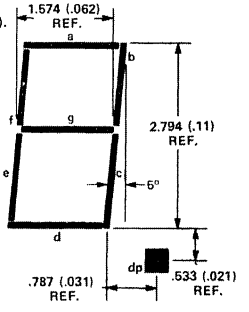


Figure 8. Right Decimal Point Configuration

Device Pin Description

PIN NO.	5082-7402/7412 FUNCTION	5082-7403/7413 FUNCTION	5082-7404/7414 FUNCTION	5082-7405/7415 FUNCTION
1	SEE NOTE 1.	CATHODE 1	CATHODE 1	CATHODE 1
2	ANODE e	ANODE e	ANODE e	ANODE e
3	ANODE c	ANODE c	ANODE c	ANODE c
4	CATHODE 3	CATHODE 3	CATHODE 3	CATHODE 3
5	ANODE dp	ANODE dp	ANODE dp	ANODE dp
6	CATHODE 4	SEE NOTE 1.	CATHODE 4	ANODE d
7	ANODE g	ANODE g	ANODE g	CATHODE 5
8	ANODE d	ANODE d	ANODE d	ANODE g
9	ANODE f	ANODE f	ANODE f	CATHODE 4
10	CATHODE 2	CATHODE 2	CATHODE 2	ANODE f
11	ANODE b	ANODE b	ANODE b	(See Note 1)
12	ANODE a.	ANODE a	ANODE a	ANODE b
13	–	–	–	CATHODE 2
14	–	–	–	ANODE a

NOTE 1. Leave Pin unconnected

Electrical

Character encoding can be performed by commercially available BCD-7 segment decoder/driver circuits. Through the use of a strobing technique, only one decoder/driver is required for each display. In addition, the number of interconnection lines between the display and the drive circuitry is minimized to 8 + N, where N is the number of characters in the display.

Each of the segments on the display is "addressable" on two sets of lines – the "character enable" lines and the "segment enable" lines. Displays are wired so that all of the cathodes of all segments comprising one character are wired together to a single character enable line. Similarly, the anodes of each of like segments (e.g., all of the decimal points, all of the center line anodes, etc.) are wired to a single line. Therefore, a single digit in the cluster can be illuminated by connecting the appropriate character enable line, with the appropriate segment enable lines for the character being displayed. When each character in the display is illuminated in sequence, at a minimum of 100 times a second, flicker free characters are formed.

The decimal point in the 7412, 7413, 7414, and 7415 displays is located at the lower right of the digit for conventional driving schemes.

The 7402, 7403, 7404 and 7405 displays contain a centrally located decimal point which is activated in place of a digit. In long registers, this technique of setting off the decimal point significantly improves the display's readability. With respect to timing, the decimal point is treated as a separate character with its own unique time frame.

A detailed discussion of display circuits and drive techniques appears in Application Note 937.

Mechanical

The 5082-7400 series package is a standard 12 or 14 Pin DIP consisting of a plastic encapsulated lead frame with integral molded lenses. It is designed for plugging into DIP sockets or soldering into PC boards. The lead frame construction allows use of standard DIP insertion tools and techniques. Alignment problems are simplified due to the clustering of digits in a single package. The shoulders of the lead frame pins are intentionally raised above the bottom of the package to allow tilt mounting of up to 20° from the PC board.

To improve display contrast, the plastic incorporates a red dye that absorbs strongly at all visible wavelengths except the 655 nm emitted by the LED. In addition, the lead frames are selectively darkened to reduce reflectance. An additional filter, such as Plexiglass 2423, Panelgraphic 60 or 63, and Homalite 100-1600, will further lower the ambient reflectance and improve display contrast.

The devices can be soldered for up to 5 seconds at a maximum solder temperature of 230°C (1/16" below the seating plane). The plastic encapsulant used in these displays may be damaged by some solvents commonly used for flux removal. It is recommended that only Freon TE, Freon TE-35, Freon TF, Isopropanol, or soap and water be used for cleaning operations.

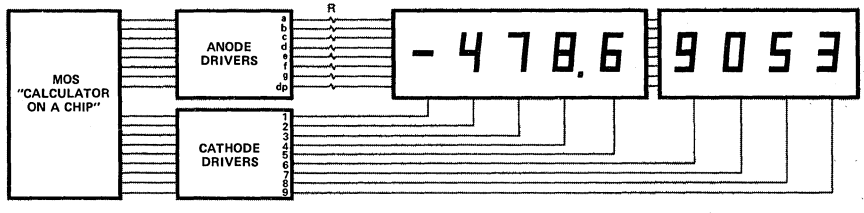


Figure 9. Block Diagram for Calculator Display Using Lower Right Hand Decimal Point.

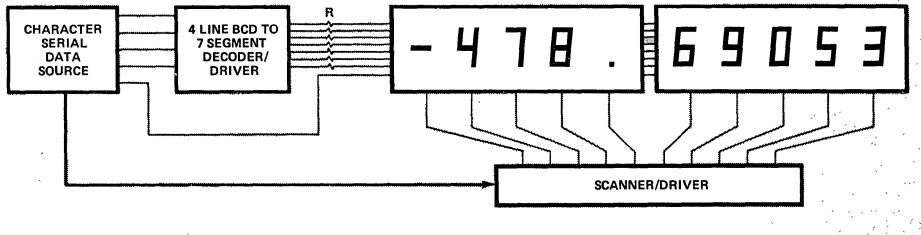


Figure 10. Block Diagram for Display Using Center Decimal Point.

HEWLETT PACKARD
COMPONENTS

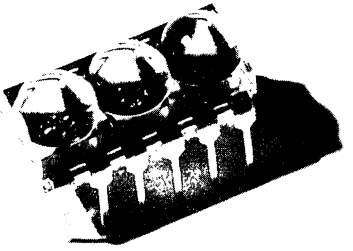
SOLID STATE NUMERIC INDICATOR (7 Segment Monolithic)

5082-7430 SERIES

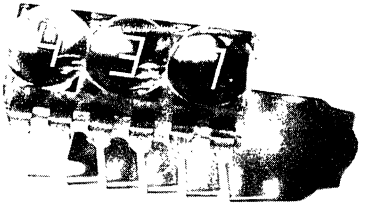
TECHNICAL DATA APRIL 1979

SOLID STATE DISPLAYS

Features



- **MOS COMPATIBLE**
  Can be Driven Directly from many MOS Circuits
- **LOW POWER**
  Excellent Readability at Only 250 μA Average per Segment
- **CONSTRUCTED FOR STROBED OPERATION**
  Minimizes Lead Connections
- **STANDARD DIP PACKAGE**
  End Stackable
  Integral Red Contrast Filter
  Rugged Construction
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit within a Single Category

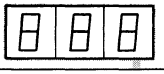


Description

The HP 5082-7430 series displays are 2.79mm (.11 inch, seven segment GaAsP numeric indicators packaged in 2 or 3 digit end-stackable clusters on 200 mil centers. An integral magnification technique increases the luminous intensity, thereby making ultra-low power consumption possible. These clusters have the standard lower right hand decimal points.

Applications include hand-held calculators, portable instruments, digital thermometers, or any other product requiring low power, low cost, minimum space, and long lifetime indicators.

Device Selection Guide

Digits per Cluster	Configuration		Part Number
	Device	Package	
2(right)		(Figure 5)	5082-7432
3		(Figure 5)	5082-7433

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or dp (Duration < 500μs)	I_{PEAK}		50	mA
Average Current per Segment or dp	I_{AVG}		5	mA
Power Dissipation per Digit [1]	P_D		80	mW
Operating Temperature, Ambient	T_A	–40	75	°C
Storage Temperature	T_S	–40	100	°C
Reverse Voltage	V_R		5	V
Solder Temperature 1/16" below seating plane (t ≤ 3 sec.) [2]			230	°C

NOTES: 1. Derate linearly @ 1 mW/°C above 25°C ambient. 2. See Mechanical section for recommended flux removal solvents.

Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp [3,4]	I_V	I_{AVG} = 500μA (I_{PK} = 5mA duty cycle = 10%)	10	40		μcd
Peak Wavelength	λ_{PEAK}			655		nm
Forward Voltage/Segment or dp	V_F	I_F = 5mA		1.55	2.0	V
Reverse Current/Segment or dp	I_R	V_R = 5V			100	μA
Rise and Fall Time [5]	t_r, t_f			10		ns

NOTES: 3. The digits are categorized for luminous intensity. Intensity categories are designated by a letter located on the back side of the package. 4. Operation at Peak Currents less than 3.5mA is not recommended. 5. Time for a 10%-90% change of light intensity for step change in current.

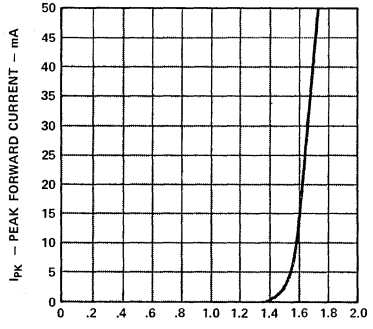


Figure 1. Peak Forward Current vs. Peak Forward Voltage

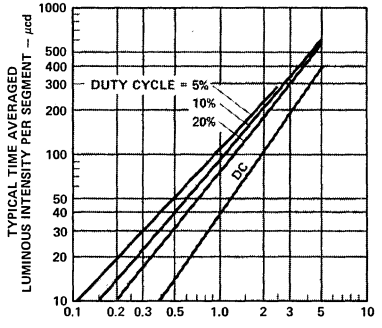


Figure 2. Typical Time Averaged Luminous Intensity per Segment vs. Average Current per Segment

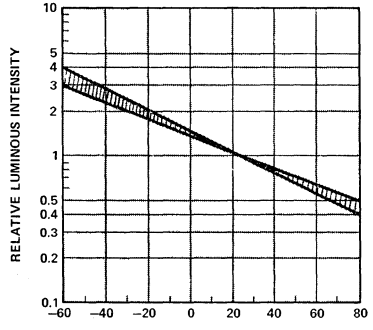


Figure 3. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level

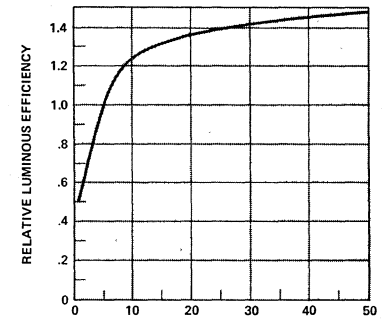


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment

Package Description

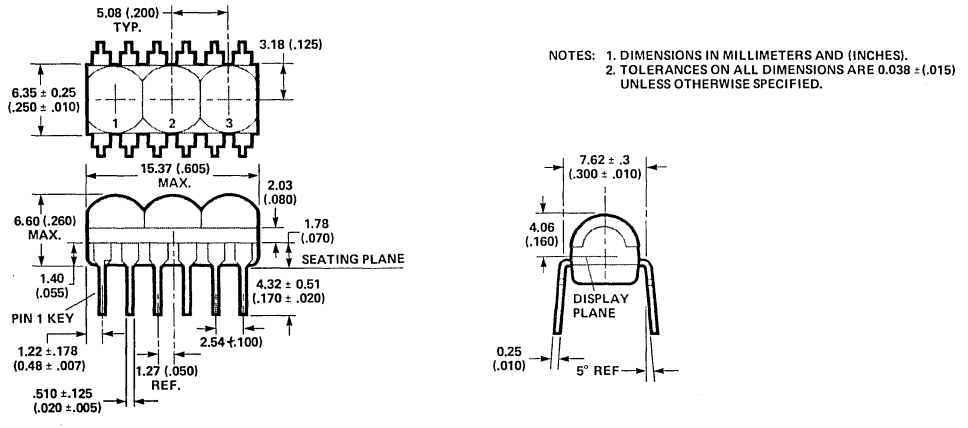
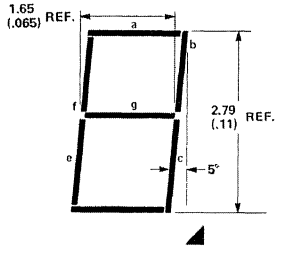


Figure 5.

Magnified Character Font Description

DEVICES
5082-7432
5082-7433



DIMENSIONS IN MILLIMETERS AND (INCHES).

Figure 6.

Device Pin Description

PIN NUMBER	5082-7432 FUNCTION	5082-7433 FUNCTION
1	SEE NOTE 1.	CATHODE 1
2	ANODE e	ANODE e
3	ANODE d	ANODE d
4	CATHODE 2	CATHODE 2
5	ANODE c	ANODE c
6	ANODE dp	ANODE dp
7	CATHODE 3	CATHODE 3
8	ANODE b	ANODE b
9	ANODE g	ANODE g
10	ANODE a	ANODE a
11	ANODE f	ANODE f
12	SEE NOTE 1.	SEE NOTE 1.

NOTE 1. Leave Pin unconnected.

Electrical/Optical

The 5082-7430 series devices utilize a monolithic GaAsP chip of 8 common cathode devices for each display digit. The segment anodes of each digit are interconnected, forming an 8 by N line array, where N is the number of characters in the display. Each chip is positioned under an integrally molded lens giving a magnified character height of 2.79mm (0.11) inches. Satisfactory viewing will be realized within an angle of approximately ±20° from the center-line of the digit.

To improve display contrast, the plastic encapsulant contains a red dye to reduce the reflected ambient light. An additional filter, such as Plexiglass 2423, Panelgraphic 60 or 63, and Homalite 100-1600, will further lower the ambient reflectance and improve display contrast.

Character encoding on the 5082-7430 series devices is performed by standard 7 segment decoder/driver circuits. Through the use of strobing techniques only one decoder/driver is required for very long multidigit displays.

A discussion of display circuits and drive techniques appears in Application Note 946.

Mechanical

The 5082-7430 series package is a standard 12 Pin DIP consisting of a plastic encapsulated lead frame with integrally molded lenses. It is designed for plugging into DIP sockets or soldering into PC boards. Alignment problems are simplified due to the clustering of digits in a single package.

The devices can be soldered for up to 5 seconds at a maximum solder temperature of 230°C (1/16" below the seating plane). The plastic encapsulant used in these displays may be damaged by some solvents commonly used for flux removal. It is recommended that only Freon TE, Freon TE-35, Freon TF, Isopropanol, or soap and water be used for cleaning operations.

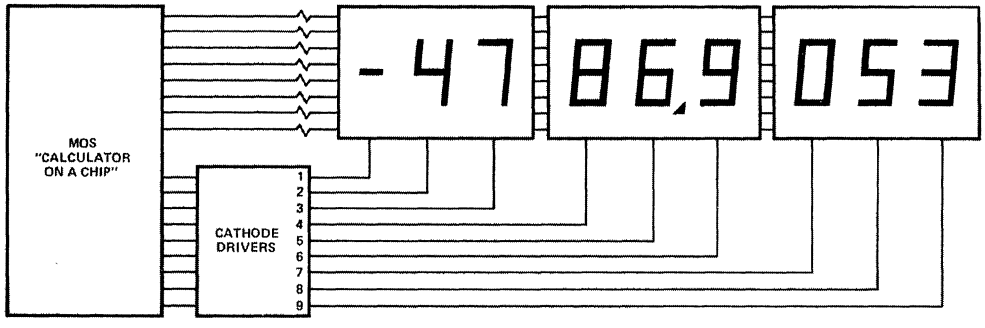


Figure 7. Block Diagram for Calculator Display

HEWLETT hp PACKARD
COMPONENTS

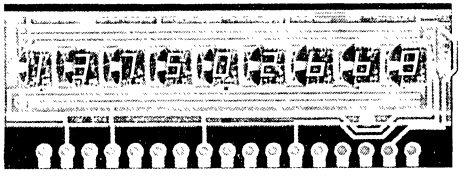
SPECIAL PARTS FOR CALCULATORS

5082-7440 SERIES

TECHNICAL DATA APRIL 1979

Features

- **MOS COMPATIBLE**
  Can be driven directly from MOS circuits.
- **LOW POWER**
  Excellent readability at only 250μA average per segment.
- **UNIFORM ALIGNMENT**
  Excellent alignment is assured by design.
- **MATCHED BRIGHTNESS**
  Uniformity of light output from digit to digit on a single PC Board.
- **AVAILABLE IN 50.8mm (2.0 inch) AND 60.325mm (2.375 inch) BOARD LENGTHS**



Description

The HP 5082-7440 series displays are 2.67mm (.105") high, seven segment GaAsP Numeric Indicators mounted in an eight or nine digit configuration on a P.C. Board. These special parts, designed specifically for calculators, have right hand decimal points and are mounted on 5.08mm (200 mil) centers. The plastic lens magnifies the digits and includes an integral protective bezel.

Applications are primarily portable, hand-held calculators and other products requiring low power, low cost and long lifetime indicators which occupy a minimum of space.

Device Selection Guide

Digits Per PC Board	Configuration		Part No.
	Device	Package	
8	8.8.8.8.8.8.8.8.	(Figure 5)	5082-7440
			5082-7448
9	8.8.8.8.8.8.8.8.8.	(Figure 5)	5082-7441
			5082-7449

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or dp (Duration < 500μs)	I_{PEAK}		50	mA
Average Current per Segment or dp[1]	I_{AVG}		3	mA
Power Dissipation per Digit	P_D		50	mW
Operating Temperature, Ambient	T_A	-20	+85	°C
Storage Temperature	T_S	-20	+85	°C
Reverse Voltage	V_R		5	V
Solder Temperature at connector edge (t≤3 sec.)[2]			230	°C

NOTES: 1. Derate linearly @ 0.1mA/°C above 60° C ambient.
2. See Mechanical section for recommended soldering techniques and flux removal solvents.

Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp[3,4]	I_V	I_{AVG} = 500μA (I_{PK} = 5mA duty cycle = 10%)	9	40		μcd
Peak Wavelength	λ_{peak}			655		nm
Forward Voltage/Segment or dp	V_F	I_F = 5mA		1.55		V

NOTES: 3. See Figure 7 for test circuit.
4. Operation at Peak Currents of less than 3.5mA is not recommended.

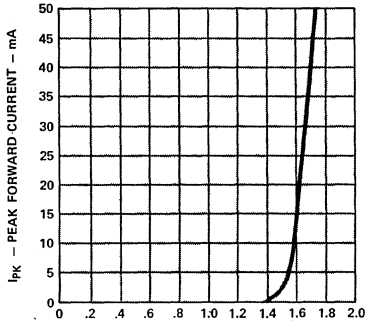


Figure 1. Peak Forward Current vs. Peak Forward Voltage

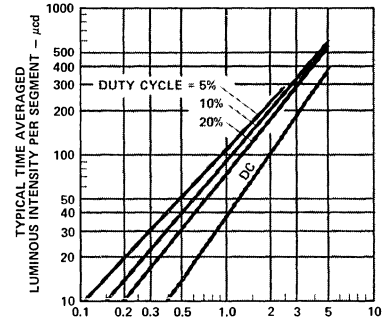


Figure 2. Typical Time Averaged Luminous Intensity per Segment vs. Average Current per Segment

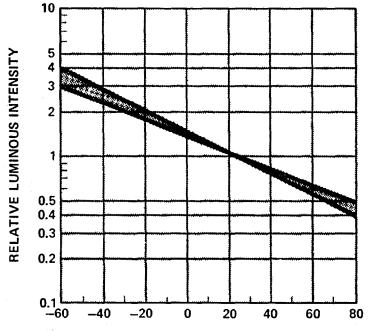


Figure 3. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level

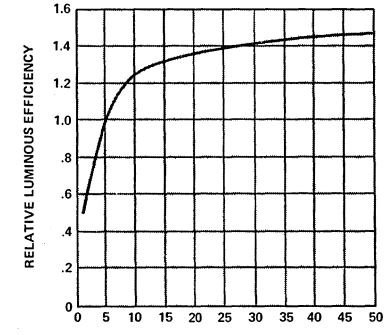
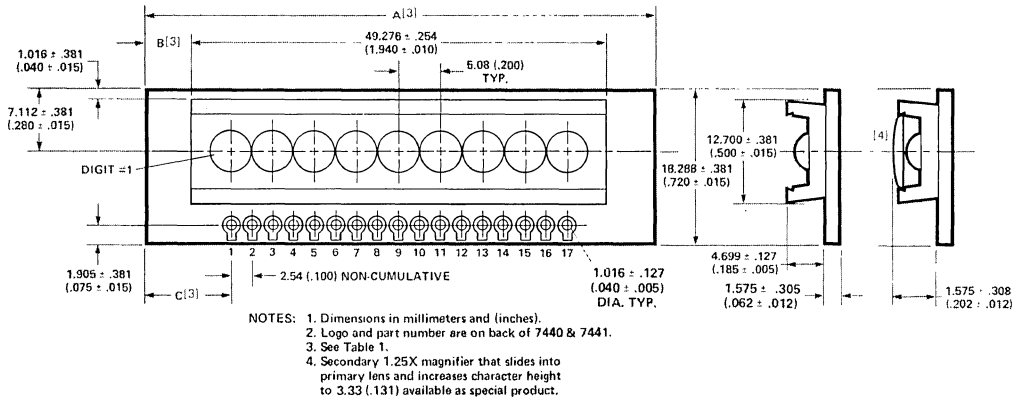


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment

Package Description

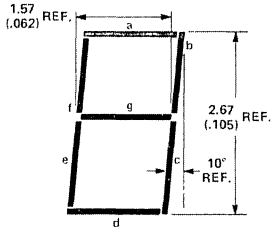


NOTES: 1. Dimensions in millimeters and (inches).
2. Logo and part number are on back of 7440 & 7441.
3. See Table 1.
4. Secondary 1.25X magnifier that slides into primary lens and increases character height to 3.33 (.131) available as special product.

Figure 5.

Magnified Character Font Description

DEVICES
5082-7440
5082-7441
5082-7448
5082-7449



Note: All dimensions in millimeters and (inches).

Figure 6.

Part No.	Dim. A	Dim. B	Dim. C
5082-7440	50.800(2.000)	0.760(.030)	5.08(.200)
5082-7441	50.800(2.000)	0.760(.030)	5.08(.200)
5082-7448	60.325(2.375)	5.512(.217)	9.830(.387)
5082-7449	60.325(2.375)	5.512(.217)	9.830(.387)

Tolerances: ±.381(.015)

Table 1.

Device Pin Description

Pin No.	5082-7440 5082-7448 Function	5082-7441 5082-7449 Function	Pin No.	5082-7440 5082-7448 Function	5082-7441 5082-7449 Function
1	N/C	Dig. 1 Cathode	10	Seg. d Anode	Seg. d Anode
2	Seg. c Anode	Seg. c Anode	11	Dig. 6 Cathode	Dig. 6 Cathode
3	Dig. 2 Cathode	Dig. 2 Cathode	12	Seg. g Anode	Seg. g Anode
4	d.p. Anode	d.p. Anode	13	Dig. 7 Cathode	Dig. 7 Cathode
5	Dig. 3 Cathode	Dig. 3 Cathode	14	Seg. b Anode	Seg. b Anode
6	Seg. a Anode	Seg. a Anode	15	Dig. 8 Cathode	Dig. 8 Cathode
7	Dig. 4 Cathode	Dig. 4 Cathode	16	Seg. f Anode	Seg. f Anode
8	Seg. e Anode	Seg. e Anode	17	Dig. 9 Cathode	Dig. 9 Cathode
9	Dig. 5 Cathode	Dig. 5 Cathode			

Electrical/Optical

The HP 5082-7440 series devices utilize a monolithic GaAsP chip containing 7 segments and a decimal point for each display digit. The segments of each digit are interconnected, forming an 8 by N line array, where N is the number of characters in the display. Each chip is positioned under a separate element of a plastic magnifying lens, producing a magnified character height of 0.105" (2,67mm). Satisfactory viewing will be realized within an angle of approximately ±20° from the centerline of the digit. The secondary lens magnifier that will increase character height from 2.67mm (0.105") to 3.33mm (0.131") and reduce viewing angle in the vertical plane only from ±20° to approximately ±18° is available as a special product. A filter, such as Plexiglass 2423, Panelgraphic 60 or 63, and Homalite 100-1600, will lower ambient reflectance and improve display contrast. Character encoding of the -7440 series devices is performed by standard 7 segment decoder driver circuits.

The 5082-7440 series devices are tested for digit to digit luminous intensity matching using the circuit depicted in Figure 7. Component values are chosen to give an I_F of 5mA per segment at a segment V_F of 1.55 volts. This test method is preferred in order to provide the best possible simulation of the end product drive circuit, thereby insuring excellent digit to digit matching. If the device is to be driven from V_{CC} potentials of less than 3.5 volts, it is recommended that the factory be contacted.

Mechanical

The 5082-7440 series devices are constructed on a standard printed circuit board substrate. A separately molded plastic lens containing 9 individual magnifying elements is attached to the PC board over the digits. The device may be mounted either by use of pins which may be soldered into the plate through holes at the connector edge of the board or by insertion into a standard PC board connector.

The devices may be soldered for up to 3 seconds per tab at a maximum soldering temperature of 230°C. Heat should be applied only to the edge connector tab areas of the PC board. Heating other areas of the board to temperatures in excess of 85°C can result in permanent damage to the display. It is recommended that a rosin core wire solder or a low temperature deactivating flux and solid core wire solder be used in soldering operations.

Special Cleaning Instructions

For bulk cleaning after a flow solder operation, the following process is recommended: Wash display in clean liquid Freon TP-35 or Freon TE-35 solvent for a time period up to 2 minutes maximum. Air dry for a sufficient length of time to allow solvent to evaporate from beneath display lens. Maintain solvent temperature below 30°C (86°F). Methanol, isopropanol, or ethanol may be used for hand cleaning at room temperature. Water may be used for hand cleaning if it is not permitted to collect under display lens.

Solvent vapor cleaning at elevated temperatures is not recommended as such processes will damage display lens. Ketones, esters, aromatic and chlorinated hydrocarbon solvents will also damage display lens. Alcohol base active rosin flux mixtures should be prevented from coming in contact with display lens.

These devices are constructed on a silver plated printed circuit board. To prevent the formation of a tarnish (Ag_2S) which could impair solderability, the boards should be stored in the unopened shipping packages until they are used. Further information on the storage, handling and cleaning of silver-plated components is contained in Hewlett-Packard Application Bulletin No. 3.

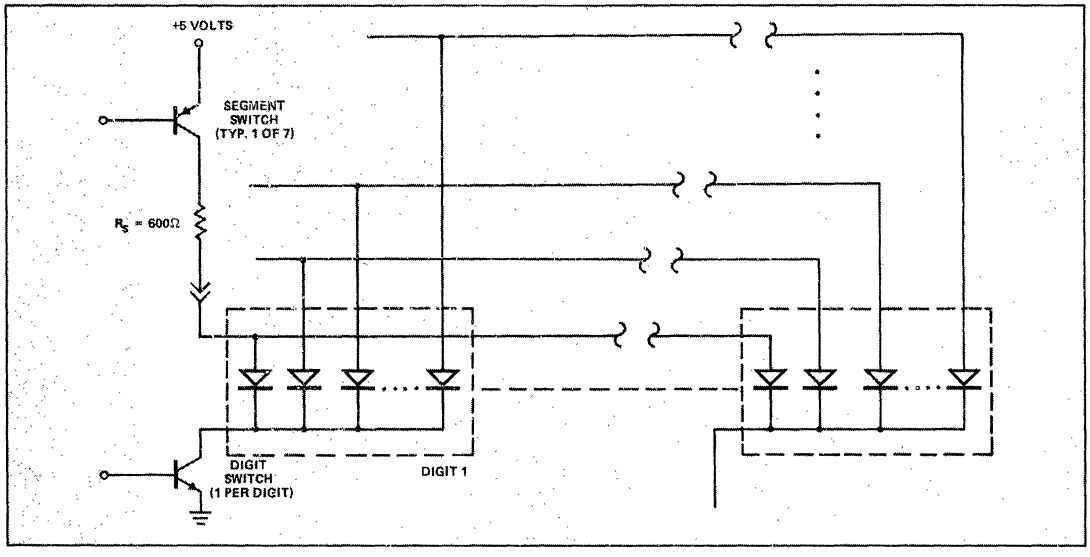


Figure 7. Circuit Diagram used for Testing the Luminous Intensity of the HP 5082-7440

HEWLETT hp PACKARD

COMPONENTS

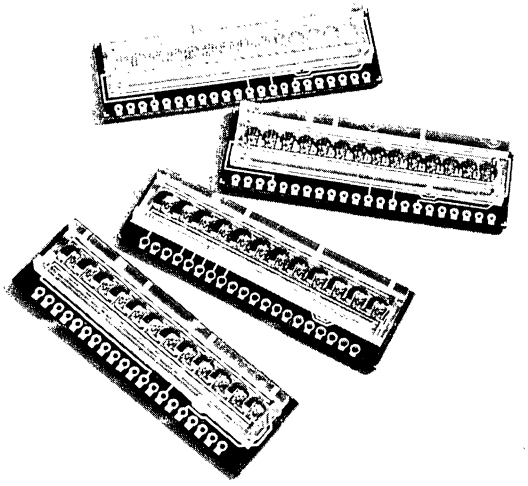
SPECIAL PARTS FOR SCIENTIFIC AND BUSINESS CALCULATORS

5082-7442
5082-7444
5082-7445
5082-7446
5082-7447

TECHNICAL DATA APRIL 1979

Features

- **12, 14, AND 16 DIGIT CONFIGURATIONS**
- **MOS COMPATIBLE**
  Can be driven directly from most MOS circuits.
- **LOW POWER**
  Excellent readability at only 250μA average per segment.
- **UNIFORM ALIGNMENT**
  Excellent Alignment is assured by design.
- **MATCHED BRIGHTNESS**
  Uniformity of light output from digit to digit on a single PC board.



Description

The HP 5082-7442, 7444, 7446, and 7447 are seven segment GaAsP Numeric indicators mounted in 12, 14, or 16 digit configurations on a P.C. board. These special parts, designed specifically for scientific and business calculators, have right hand decimal points and are mounted on 175 mil (4.45mm) centers in the 12 digit configurations and 150 mil (3.81mm) centers in the 14 and 16 digit configurations. The plastic lens magnifies the digits and includes an integral protective bezel.

Applications are primarily portable, hand held calculators, digital telephone peripherals, data entry terminals and other products requiring low power, low cost, and long lifetime indicators which occupy a minimum of space.

Device Selection Guide

Digits Per PC Board	Digit Height mm (inches)	Configuration DEVICE	Package	Part No. 5082-
12	2.54 (.100)	8.8.8.8.8.8.8.8.8.8.8.8.	Figure 4	7442 and 7445
14	2.54 (.100)	8.8.8.8.8.8.8.8.8.8.8.8.8.8.	Figure 5	7444
14	2.84 (.112)	8.8.8.8.8.8.8.8.8.8.8.8.8.8.	Figure 5	7447 *
16	2.92 (.115)	8.8.8.8.8.8.8.8.8.8.8.8.8.8.8.8.	Figure 6	7446

*5082-7447 is a 5082-7444 with a slide-in cylindrical lens to provide added magnification.

Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or dp (Duration <500μs)	I_{PEAK}		50	mA
Average Current per Segment or dp[1]	I_{AVG}		3	mA
Power Dissipation per Digit	P_D		50	mW
Operating Temperature, Ambient	T_A	−20	+85	°C
Storage Temperature	T_S	−20	+85	°C
Reverse Voltage	V_R		5	V
Solder Temperature at connector edge (t ≤3 sec.)[2]			230	°C

NOTES: 1. Derate linearly at 0.1mA/°C above 60°C ambient.
2. See Mechanical section for recommended soldering techniques and flux removal solvents.

Electrical/Optical Characteristics at T_A=25°C

Part No.	Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
7442/7445	Luminous Intensity/ Segment or dp[3] (Digit Average)	I_V	5mA Peak 1/12 Duty Cycle	7	35		μcd
7444/7447			5mA Peak 1/14 Duty Cycle	7	35		μcd
7446			5mA Peak 1/16 Duty Cycle				
7442/7445 7444/7447 7446	Peak Wavelength	λ_{PEAK}			655		nm
	Forward Voltage/ Segment or dp	V_F	I_F = 5mA		1.55		V

NOTE: 3. Operation at Peak Currents of less than 3.5mA is not recommended.

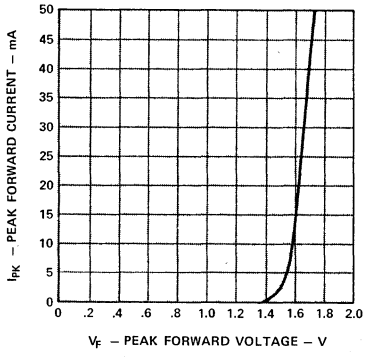


Figure 1. Peak Forward Current vs. Peak Forward Voltage

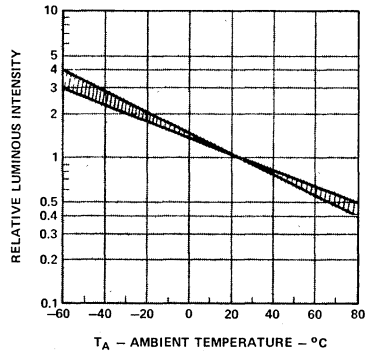


Figure 2. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level.

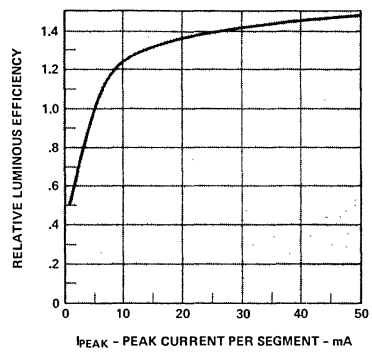


Figure 3. Relative Luminous Efficiency vs. Peak Current per Segment.

Electrical/Optical

The HP 5082-7442, 7444, 7445, 7446 and 7447 devices utilize a monolithic GaAsP chip containing 7 segments and a decimal point for each display digit. The segments of each digit are interconnected, forming an 8 by N line array, where N is the number of digits in the display. Each chip is positioned under a separate element of a plastic magnifying lens, producing a magnified character. Satisfactory viewing will be realized within an angle of approximately ±20° from the centerline of the digit. A filter, such as plexiglass 2423, Panelgraphic 60 or 63, and Homalite 100-1600, will lower the ambient reflectance and improve display contrast. Digit encoding of these devices is performed by standard 7 segment decoder driver circuits.

These devices are tested for digit-to-digit luminous intensity matching. This test is performed with a power supply of 5V and component values selected to supply 5mA I_{PEAK} at V_F = 1.55V. If the device is to be driven from V_{CC} potentials of less than 3.5 volts, it is recommended that the factory be contacted.

Mechanical Specifications

The 5082-7442, 7444, 7445, 7446, and 7447 devices are constructed on a silver plated printed circuit board substrate. A molded plastic lens array is attached to the PC board over the digits to provide magnification.

These devices may be mounted using any one of several different techniques. The most straightforward is the use of standard PC board edge connectors. A less expensive approach can be implemented through the use of stamped or etched metal mounting clips such as those available from Burndy (Series LED-B) or JAV Manufacturing (Series 1255). Some of these devices will also serve as an integral display support. A third approach would be the use of a row of wire stakes which would first be soldered to the PC mother-board and the display board then inserted over the wire stakes and soldered in place.

The devices may be soldered for up to 3 seconds per tab at a maximum soldering temperature of 230° C. Heat should be applied only to the edge connector tab areas of the PC board. Heating other areas of the board to temperatures in excess of 85° C can result in permanent damage to the lens. It is recommended that a rosin core wire solder or a low temperature deactivating flux and solid core wire solder be used in soldering operations. A solder containing approximately 2% silver (Sn 62) will enhance solderability by preventing leaching of the plated silver off the PC board into the solder solution.

Special Cleaning Instructions

For bulk cleaning after a flow solder operation, the following process is recommended. Wash display in clean liquid Freon TP - 35 or Freon TE - 35 solvent for a time period up to 2 minutes maximum. Air dry for a sufficient length of time to allow solvent to evaporate from beneath display lens. Maintain solvent temperature below 30° C (86° F). Methanol, isopropanol, or ethanol may be used for cleaning at room temperature. Soap and water solutions may be utilized for removing water-soluble fluxes from the contact area but must not be allowed to collect under the display lens.

Solvent vapor cleaning at elevated temperatures is not recommended as such processes will damage display lens. Ketones, esters, aromatic and chlorinated hydrocarbon solvents will also damage display lens. Alcohol base active rosin flux mixtures should be prevented from coming in contact with display lens.

These devices are constructed on a silver plated printed circuit board. To prevent the formation of a tarnish (Ag_2S) which could impair solderability, the boards should be stored in the unopened shipping packages until they are used. Further information on the storage, handling and cleaning of silver-plated components is contained in Hewlett-Packard Application Bulletin No. 3.

Device Pin Description

Pin No.	5082-7442 5082-7444 5082-7447 Function	5082-7445 Function	5082-7446 Function
1	Cathode-Digit 1	Anode-Segment a	Cathode-Digit 1
2	Cathode-Digit 2	Anode-Segment f	Cathode-Digit 2
3	Cathode-Digit 3	Anode-Segment b	Cathode-Digit 3
4	Anode-Segment c	Anode-Segment c	Cathode-Digit 4
5	Cathode-Digit 4	Anode-Segment d	Cathode-Digit 5
6	Anode-DP	Anode-Segment DP	Anode-Segment e
7	Cathode-Digit 5	Anode-Segment e	Cathode-Digit 6
8	Anode-Segment a	Anode-Segment g	Anode-Segment d
9	Cathode-Digit 6	Cathode-Digit 3	Cathode-Digit 7
10	Anode-Segment e	Cathode-Digit 2	Anode-Segment a
11	Cathode-Digit 7	Cathode-Digit 4	Cathode-Digit 8
12	Anode-Segment d	Cathode-Digit 1	Anode-Segment DP
13	Cathode-Digit 8	Cathode-Digit 5	Cathode-Digit 9
14	Anode-Segment g	Cathode-Digit 12	Anode-Segment c
15	Cathode-Digit 9	Cathode-Digit 6	Cathode-Digit 10
16	Anode-Segment b	Cathode-Digit 11	Anode-Segment g
17	Cathode-Digit 10	Cathode-Digit 7	Cathode-Digit 11
18	Anode-Segment f	Cathode-Digit 10	Anode-Segment b
19	Cathode-Digit 11	Cathode-Digit 9	Cathode-Digit 12
20	Cathode-Digit 12	Cathode-Digit 8	Anode-Segment f
21	Cathode-Digit 13		Cathode-Digit 13
22	Cathode-Digit 14		Cathode-Digit 14
23			Cathode-Digit 15
24			Cathode-Digit 16

Package Dimensions

DEVICE	X	Y	Z
5082-7442	60.3 (2.375)	6.03 (.2375)	1.02 (.040)
5082-7445	59.6 (2.345)	5.70 (.2225)	1.42 (.056)

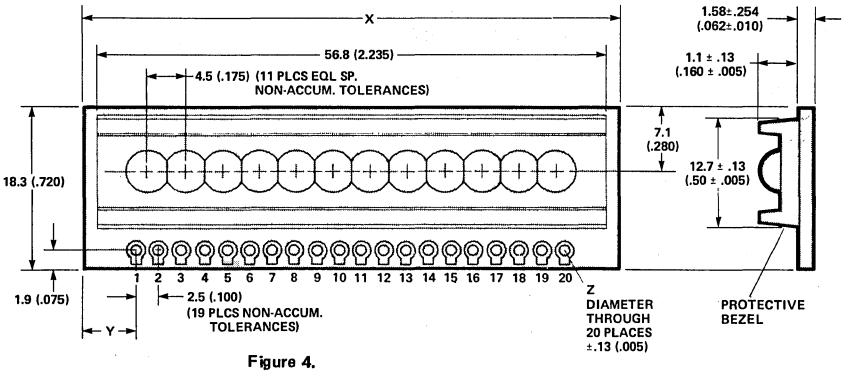


Figure 4.

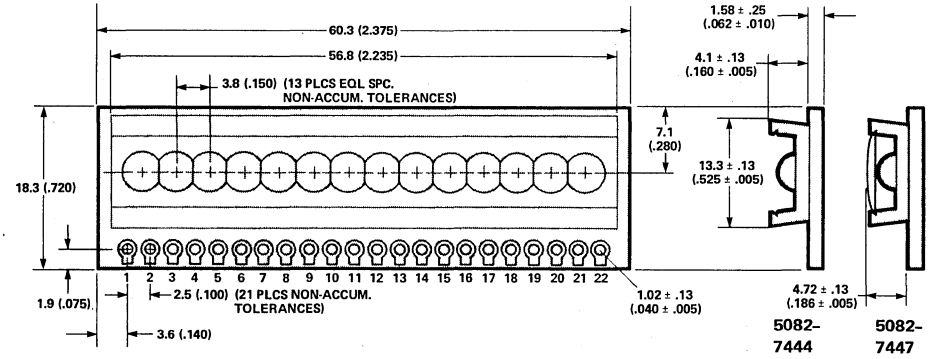


Figure 5.

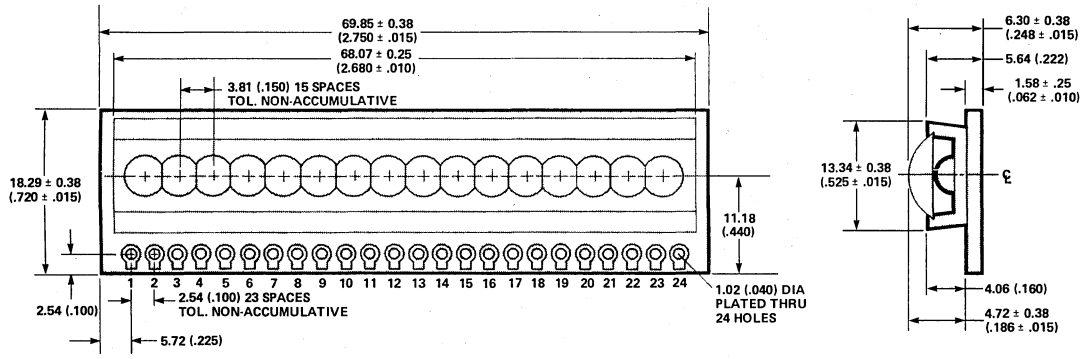
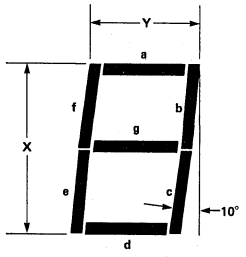


Figure 6.



DEVICE	X	Y
5082-7442	2.54 (.100)	1.42 (.056)
5082-7444	2.54 (.100)	1.40 (.055)
5082-7445	2.54 (.100)	1.42 (.056)
5082-7446	2.92 (.115)	1.40 (.055)
5082-7447	2.84 (.112)	1.40 (.055)

NOTES: 1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. TOLERANCES ON ALL DIMENSIONS ARE ±0.38 (.015) UNLESS OTHERWISE SPECIFIED.

HEWLETT hp PACKARD
COMPONENTS

SPECIAL PARTS FOR CALCULATORS

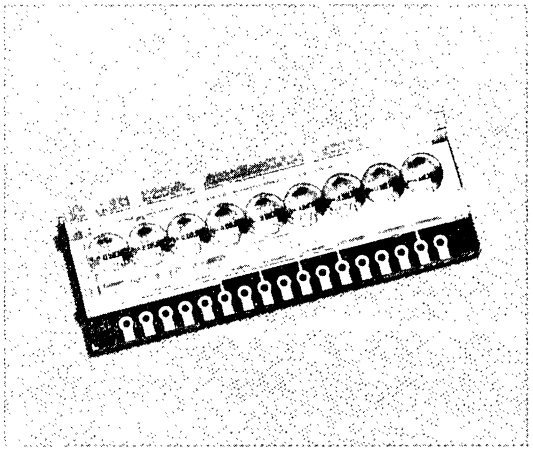
5082-7240 SERIES

TECHNICAL DATA APRIL 1979

SOLID STATE DISPLAYS

Features

- **MOS COMPATIBLE**
  Can be driven directly from MOS circuits.
- **LOW POWER**
  Excellent readability at only 250μA average per segment.
- **UNIFORM ALIGNMENT**
  Excellent alignment is assured by design.
- **MATCHED BRIGHTNESS**
  Uniformity of light output from digit to digit on a single PC Board.
- **STATE OF THE ART LENS DESIGN**
  Assures the best possible character height, viewing angle, off-axis distortion tradeoff.



Description

The HP 5082-7240 series displays are 2.59mm (.102") high, seven segment GaAsP Numeric Indicators mounted in an eight or nine digit configuration on a P. C. Board. These special parts, designed specifically for calculators, have right hand decimal points and are mounted on 5.08mm (200 mil) centers. The plastic lens over the digits has a magnifier and a protective bezel built-in. A secondary magnifying lens, available on special request, can be added to the primary lens for additional character enlargement.

Applications are primarily portable, hand-held calculators and other products requiring low power, low cost and long lifetime indicators which occupy a minimum of space.

Device Selection Guide

Digits Per PC Board	Configuration		Part No.
	Device	Package	
8	8.8.8.8.8.8.8.8.	(Figure 5)	5082-7240
9	8.8.8.8.8.8.8.8.8.	(Figure 5)	5082-7241

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or dp (Duration $< 500\mu s$)	I_{PEAK}		50	mA
Average Current per Segment or dp[1]	I_{AVG}		3	mA
Power Dissipation per Digit	P_D		50	mW
Operating Temperature, Ambient	T_A	-20	+85	°C
Storage Temperature	T_S	-20	+85	°C
Reverse Voltage	V_R		5	V
Solder Temperature at connector edge ($t \leq 3$ sec.)[2]			230	°C

NOTES: 1. Derate linearly @ 0.1mA/°C above 60°C ambient.
2. See Mechanical section for recommended soldering techniques and flux removal solvents.

Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp[3,4]	I_V	I_{AVG} = 500μA (I_{PK} = 5mA duty cycle = 10%)	12.5	50		μcd
Peak Wavelength	λ_{peak}			655		nm
Forward Voltage/Segment or dp	V_F	I_F = 5mA		1.6		V

NOTES: 3. See Figure 7 for test circuit.
4. Operation at Peak Currents of less than 3.0mA is not recommended.

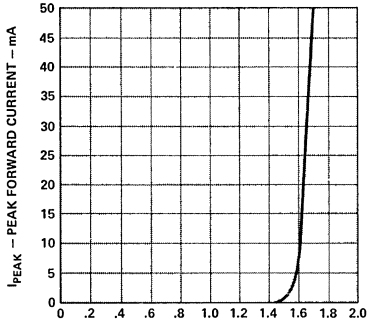


Figure 1. Peak Forward Current vs. Peak Forward Voltage

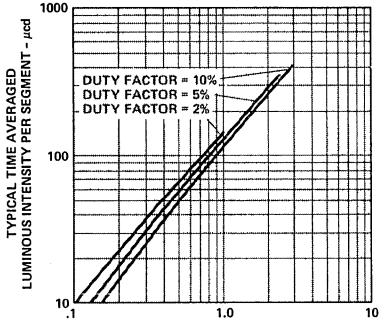


Figure 2. Typical Time Averaged Luminous Intensity per Segment vs. Average Current per Segment

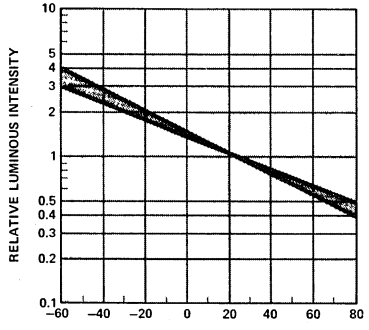


Figure 3. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level

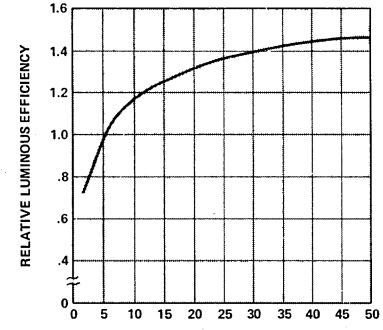
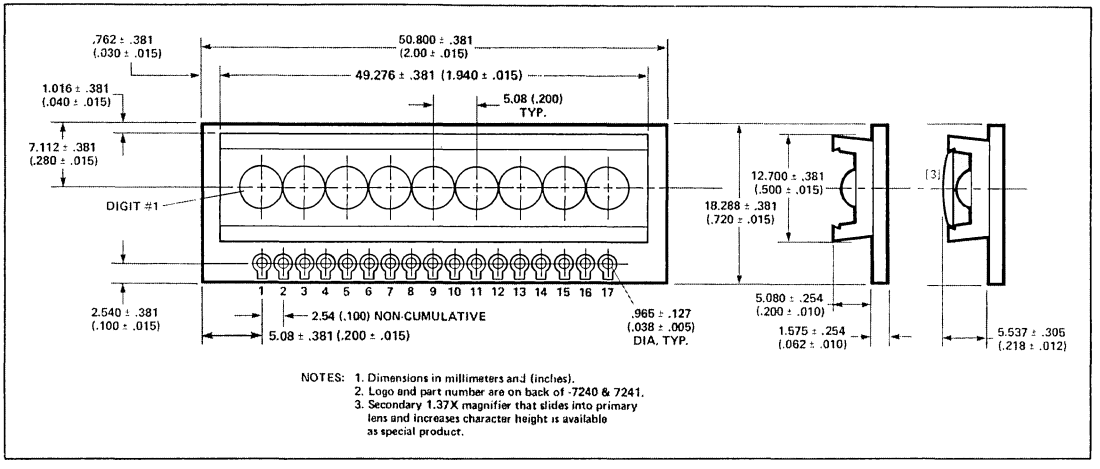


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment

Package Description

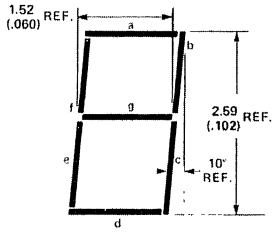


NOTES: 1. Dimensions in millimeters and (inches).
2. Logo and part number are on back of -7240 & 7241.
3. Secondary 1.37X magnifier that slides into primary lens and increases character height is available as special product.

Figure 5.

Magnified Character Font Description

DEVICES
5082-7240
5082-7241



Note: All dimensions in millimeters and (inches).

Figure 6.

Device Pin Description

Pin No.	5082-7240 Function	5082-7241 Function	Pin No.	5082-7240 Function	5082-7241 Function
1	NOTE 4	Dig. 1 Cathode	10	Seg. d Anode	Seg. d Anode
2	Seg. c Anode	Seg. c Anode	11	Dig. 6 Cathode	Dig. 6 Cathode
3	Dig. 2 Cathode	Dig. 2 Cathode	12	Seg. g Anode	Seg. g Anode
4	d.p. Anode	d.p. Anode	13	Dig. 7 Cathode	Dig. 7 Cathode
5	Dig. 3 Cathode	Dig. 3 Cathode	14	Seg. b Anode	Seg. b Anode
6	Seg. a Anode	Seg. a Anode	15	Dig. 8 Cathode	Dig. 8 Cathode
7	Dig. 4 Cathode	Dig. 4 Cathode	16	Seg. f Anode	Seg. f Anode
8	Seg. e Anode	Seg. e Anode	17	Dig. 9 Cathode	Dig. 9 Cathode
9	Dig. 5 Cathode	Dig. 5 Cathode			

NOTE 4: Leave pin 1 unconnected on the 5082-7240.

Electrical/Optical

The HP 5082-7240 series devices utilize a monolithic GaAsP chip containing 7 segments and a decimal point for each display digit. The segments of each digit are interconnected, forming an 8 by N line array, where N is the number of characters in the display. Each chip is positioned under a separate element of a plastic magnifying lens, producing a magnified character height of 2.59mm (0.102"). Satisfactory viewing will be realized within an angle of approximately ±20° from the centerline of the digit. A secondary lens magnifier that will increase character height from 2.59mm (.102") to 3.56mm (.140") is available as a special product. Character encoding of the 7240 series devices is performed by standard 7 segment decoder driver circuits.

The 5082-7240 series devices are tested for digit to digit luminous intensity matching using the circuit depicted in Figure 7. Component values are chosen to give an I_F of 5mA per segment at a segment V_F of 1.6 volts. This test method is preferred in order to provide the best possible simulation of the end product drive circuit, thereby insuring excellent digit to digit matching. If the device is to be driven from V_{CC} potentials of less than 3.5 volts, it is recommended that the factory be contacted.

Mechanical

The 5082-7240 series devices are constructed on a standard printed circuit board substrate. A separately molded plastic lens bar containing 9 individual magnifying elements is attached to the PC board over the digits. The device may be mounted either by use of pins which may be soldered into the plate through holes at the connector edge of the board or by insertion into a standard PC board connector.

The devices may be soldered for up to 3 seconds per tab at a maximum soldering temperature of 230°C. Heat should be applied only to the edge connector tab areas of the PC board. Heating other areas of the board to temperatures in excess of 85°C can result in permanent damage to the display. It is recommended that a rosin core wire solder or a low temperature deactivating flux and solid core wire solder be used in soldering operations.

Special Cleaning Instructions

For bulk cleaning after a flow solder operation, the following process is recommended: Wash display in clean liquid Freon TP-35 or Freon TE-35 solvent for a time period up to 2 minutes maximum. Air dry for a sufficient length of time to allow solvent to evaporate from beneath display lens. Maintain solvent temperature below 30°C (86°F). Methanol, isopropanol, or ethanol may be used for hand cleaning at room temperature. Water may be used for hand cleaning if it is not permitted to collect under display lens.

Solvent vapor cleaning at elevated temperatures is not recommended as such processes will damage display lens. Ketones, esters, aromatic and chlorinated hydrocarbon solvents will also damage display lens. Alcohol base active rosin flux mixtures should be prevented from coming in contact with display lens.

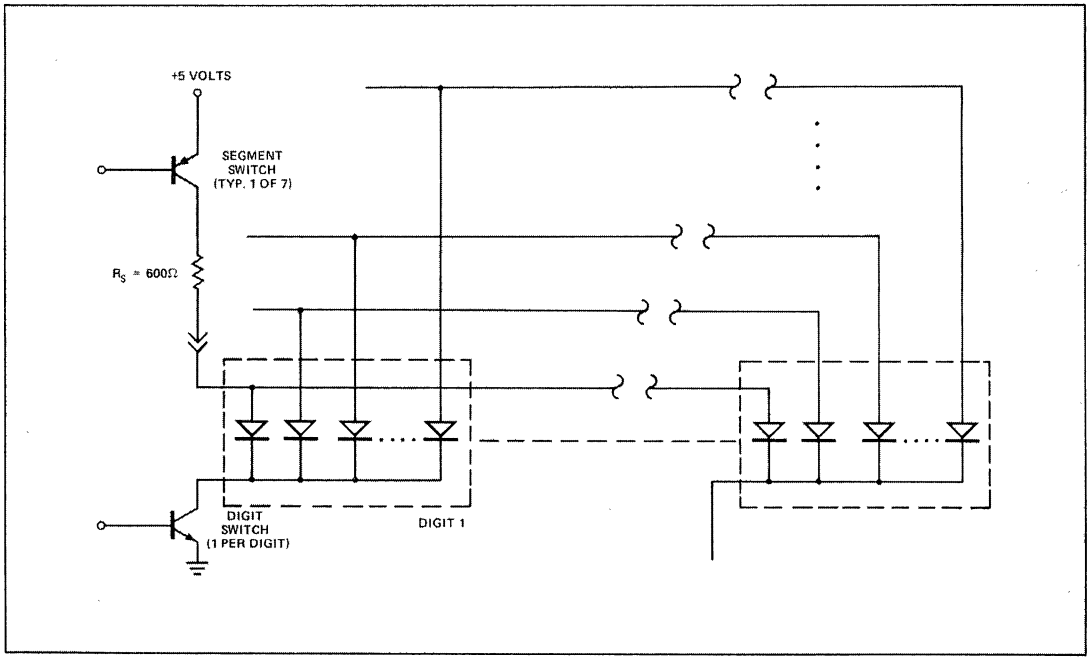


Figure 7. Circuit Diagram used for Testing the Luminous Intensity of the HP 5082-7240

HEWLETT hp PACKARD

COMPONENTS

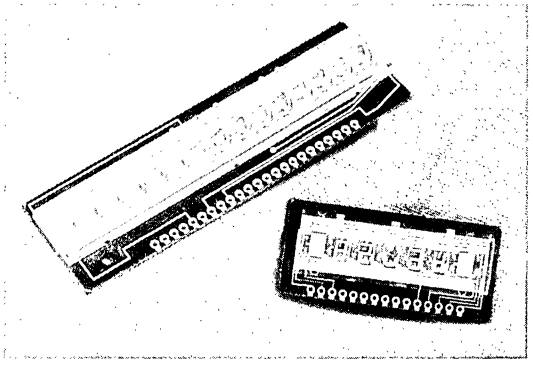
LARGE MONOLITHIC NUMERIC INDICATORS

5082-7265
5082-7275
5082-7285
5082-7295

TECHNICAL DATA APRIL 1979

Features

- **LARGE 4.45mm (.175") CHARACTER HEIGHT**
- **LOW POWER**
  Satisfactory Readability can be Achieved with Drive Currents as Low as 1.0-1.5mA Average per Segment Depending on Peak Current Levels
- **MOS COMPATIBLE**
  Can be Driven Directly from MOS Circuits
- **COMPACT INFORMATION DISPLAY**
  5.84mm (.23") Digit Spacing Yields Over 4 Characters per Inch.
- **HIGH AMBIENT READABILITY**
  High Sterance Emitting Areas Mean Excellent Readability in High Ambient Light Conditions
- **HIGH LEGIBILITY AND NUMBER RECOGNITION**
  High On/Off Contrast and Fine Line Segments Improve Viewer Recognition of the Displayed Number
- **UNIFORM ALIGNMENT**
  Excellent Alignment is Assured by Design
- **MATCHED BRIGHTNESS**
  Provides Uniform Light Output from Digit to Digit on a Single PC Board
- **EASY MOUNTING**
  Flexible Mounting in Desired Position with Edge Connectors or Soldered Wires

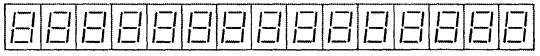
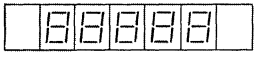
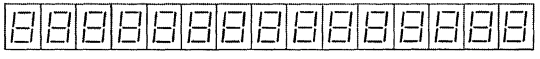


Description

The HP 5082-7265, 7275, 7285, and 7295 displays are 4.45 mm (.175") seven segment GaAsP numeric indicators mounted in 5 or 15 digit configurations on a PC Board. The monolithic light emitting diode character is magnified by the integral lens which increases both character size and luminous intensity, thereby making low power consumption possible. Options include both a right hand decimal point and centered decimal version for improved legibility. The digits are mounted on 5.84 mm (230 mil) centers.

These displays are attractive for applications such as digital instruments, desk top calculators, avionics and automobile displays, P.O.S. terminals, in-plant control equipment, and other products requiring low power, display compactness, readability in high ambients, or highly legible, long lifetime numerical displays.

Device Selection Guide

Digits Per PC Board	Configuration			Part No. 5082-
	Device	Package	Character	
5		(Figure 5)	Center Decimal Point (Figure 7)	7265
15		(Figure 6)	Center Decimal Point (Figure 7)	7275
5		(Figure 5)	Right Decimal Point (Figure 7)	7285
15		(Figure 6)	Right Decimal Point (Figure 7)	7295

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current per Segment or DP (Duration <35μs)	I_{PEAK}		200	mA
Average Current per Segment or DP [1]	I_{AVG}		7	mA
Power Dissipation per Digit [2]	P_D		125	mW
Operating Temperature, Ambient	T_A	-20	+70	°C
Storage Temperature	T_S	-20	+80	°C
Reverse Voltage	V_R		5	V
Solder Temperature at connector edge (t≤3 sec.) [3]			230	°C

NOTES: 1. Derate linearly at 0.12 mA/°C above 25°C ambient.
2. Derate linearly at 2.3 mW/°C above 25°C ambient.
3. See Mechanical section for recommended soldering techniques and flux removal solvents.

Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Luminous Intensity/Segment or dp (Time Averaged) 15 digit display 5082-7275, 5082-7295 [4,6]	I_v	$I_{avg.}$ = 2 mA (30 mA Peak 1/15 duty cycle)	30	90		μcd
Luminous Intensity/Segment or dp (Time Averaged) 5 digit display 5082-7265, 5082-7285 [4,6]	I_v	$I_{avg.}$ = 2 mA (10 mA Peak 1/5 duty cycle)	30	70		μcd
Forward Voltage per Segment or dp 5082-7275, 5082-7295 15 digit display	V_F	I_F = 30 mA		1.60	2.3	V
Forward Voltage per Segment or dp 5082-7265, 5082-7285 5 digit display	V_F	I_F = 10 mA		1.55	2.0	V
Peak Wavelength	λ_{PEAK}			655		nm
Dominant Wavelength [5]	λ_d			640		nm
Reverse Current per Segment or dp	I_R	V_R = 5V			100	μA
Temperature Coefficient of Forward Voltage	ΔV_F/°C			-2.0		mV/°C

NOTES: 4. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship:
$I_V(T_A) = I_{V(25°C)}(.985)^{(T_A - 25°C)}$
5. The dominant wavelength λ_d, is derived from the C.I.E. Chromaticity Diagram and represents the single wavelength which defines the color of the device.
6. Operation at peak currents of less than 6.0 mA is not recommended.

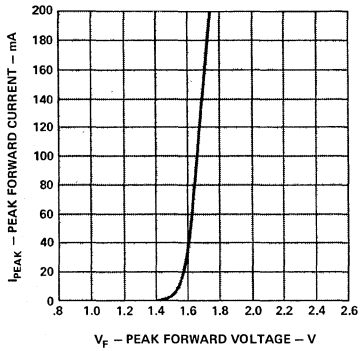


Figure 1. Peak Forward Current vs. Peak Forward Voltage.

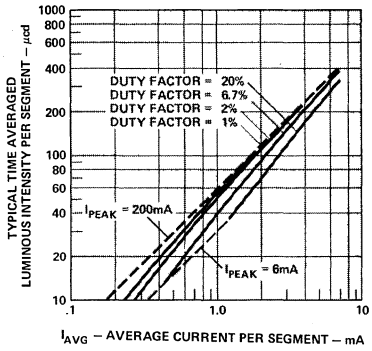


Figure 2. Typical Time Averaged Luminous Intensity per Segment vs. Average Current per Segment.

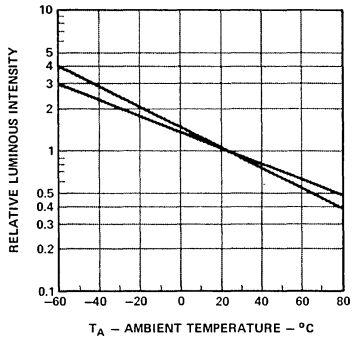


Figure 3. Relative Luminous Intensity vs. Ambient Temperature at Fixed Current Level.

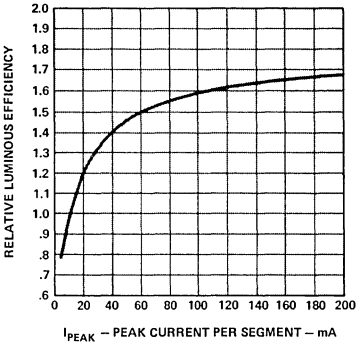


Figure 4. Relative Luminous Efficiency vs. Peak Current per Segment.

Electrical

The HP 5082-7265, 7275, 7285, and 7295 devices utilize a seven segment monolithic GaAsP chip. The 5082-7285 and 7295 devices use a separate decimal point chip located to the right of each digit. The 5082-7265 and 7275 devices use a centered decimal point on the monolithic seven segment chip. The centered decimal point version improves the displays readability by dedicating an entire digit position to distinguishing the decimal point. In the driving scheme for the centered decimal point version the decimal point is treated as a separate character with its own time frame.

The segments and decimal points of each digit are interconnected, forming an 8 by N line array, where N is the number of characters in the display. Character encoding is performed by standard 7 segment decoder driver circuits. A detailed discussion of display circuits and drive techniques appears in Applications Note 937.

These devices are tested for digit to digit luminous intensity using the circuit depicted in Figure 8. Component values are chosen to give a Peak I_F of 10 mA per segment for the 5 digit displays and 30 mA per segment for the 15 digit displays. This test method is preferred in order to provide the best possible simulation of the end product drive circuit, thereby ensuring excellent digit to digit matching. If the device is to be driven at peak currents of less than 6.0 mA, it is recommended that the HP field salesman or factory be contacted.

For special product applications, the number of digits per display can be altered. It is also possible to provide a colon instead of the centered decimal point. Contact the HP field salesman or factory to discuss such special modifications.

Optical

Each chip is positioned under a separate element of a plastic magnifying lens, producing a magnified character height of 4.45mm (.175"). To increase vertical viewing angle the secondary cylindrical magnifier can be removed reducing character height to 3.86mm (.152"). A filter, such as Panelgraphic 60 or 63, or Homalite 100-1600, will lower ambient reflectance and improve display contrast.

Mechanical

These devices are constructed on a standard printed circuit board substrate. A separately molded plastic lens is attached to the PC board over the digits. The lens is an acrylic styrene material that gives good optical lens performance, but is subject to scratching so care should be exercised in handling.

The device may be mounted either by use of pins which may be soldered into the plated through holes at the connector edge of the PC board or by insertion into a standard PC board connector. The devices may be soldered for up to 3 seconds per tab at a maximum soldering temperature of 230°C. Heat should be applied only to the edge connector tab areas of the PC board. Heating other areas of the board to temperatures in excess of 85°C can result in permanent damage to the display. It is recommended that a rosin core wire solder or a low temperature deactivating flux and solid wire solder be used in soldering operations.

The PC board is silver plated. To prevent the formation of a tarnish (Ag_2S) which could impair solderability the displays should be stored in the unopened shipping packages until they are used. Further information on the storage, handling, and cleaning of silver plated components is contained in Hewlett-Packard Application Bulletin No. 3.

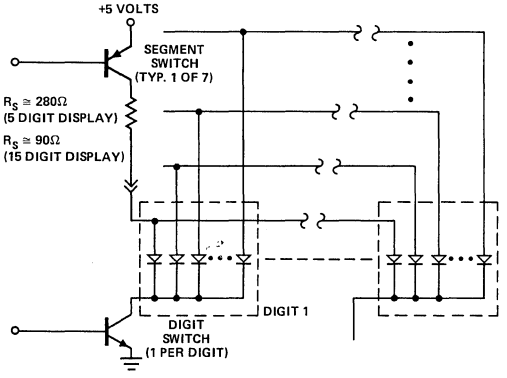


Figure 5. Circuit Diagram used for Testing the Luminous Intensity.

Package Dimensions

ALL DIMENSIONS IN MILLIMETERS AND (INCHES). TOLERANCES ARE ±0.203 (±.008) UNLESS OTHERWISE NOTED

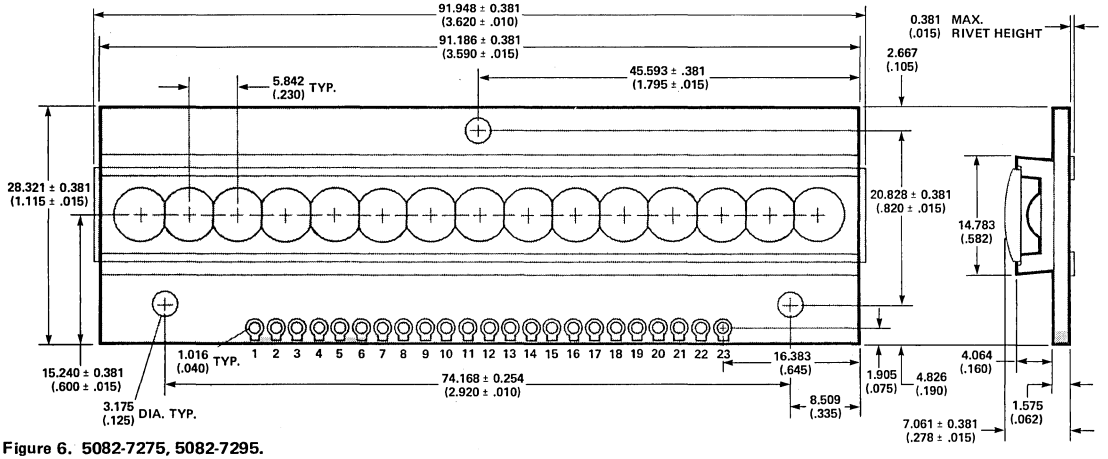


Figure 6. 5082-7275, 5082-7295.

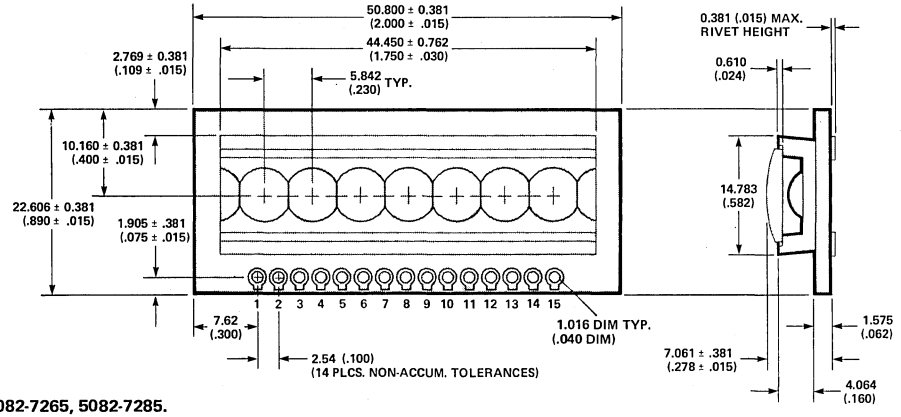
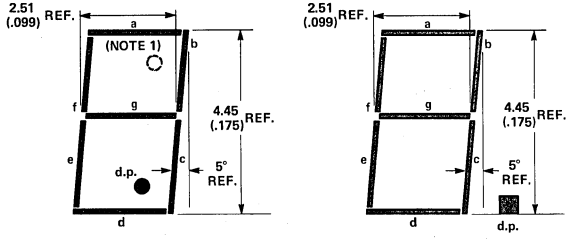


Figure 7. 5082-7265, 5082-7285.

Magnified Character Font Description

DEVICES
5082-7265
5082-7275

DEVICES
5082-7285
5082-7295



ALL DIMENSIONS IN MILLIMETERS AND (INCHES).

NOTE 1. Bonding Option for Colon Instead of Decimal Point. See Electrical Section.

Figure 8.

Device Pin Description

Pin No.	5082-7265 5082-7285 Function	5082-7275 5082-7295 Function
1	Anode Segment b	Cathode Digit 1
2	Anode Segment g	Cathode Digit 2
3	Anode Segment e	Cathode Digit 3
4	Cathode Digit 1	Cathode Digit 4
5	Cathode Digit 2	Anode Segment dp
6	Cathode Digit 3	Cathode Digit 5
7	Cathode Digit 4	Anode Segment c
8	Cathode Digit 5	Cathode Digit 6
9	Cathode Digit 6	Anode Segment e
10	Cathode Digit 7	Cathode Digit 7
11	Anode Segment dp	Anode Segment a
12	Anode Segment d	Cathode Digit 8
13	Anode Segment c	Anode Segment g
14	Anode Segment a	Cathode Digit 9
15	Anode Segment f	Anode Segment d
16		Cathode Digit 10
17		Anode Segment f
18		Cathode Digit 11
19		Anode Segment b
20		Cathode Digit 12
21		Cathode Digit 13
22		Cathode Digit 14
23		Cathode Digit 15

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COMPONENTS

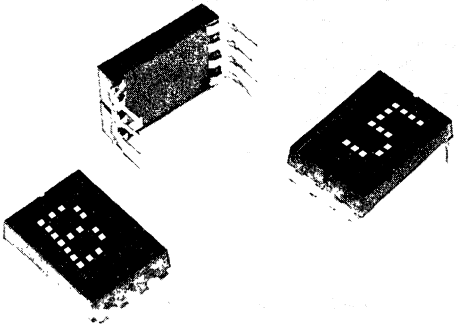
NUMERIC and HEXADECIMAL INDICATORS

5082-7300
5082-7302
5082-7304
5082-7340

TECHNICAL DATA APRIL 1979

Features

- NUMERIC 5082-7300/-7302
  - 0-9, Test State, Minus Sign, Blank States
  - Decimal Point
    - 7300 Right Hand D.P.
    - 7302 Left Hand D.P.
- HEXADECIMAL 5082-7340
  - 0-9, A-F, Base 16 Operation
  - Blanking Control, Conserves Power
  - No Decimal Point
- DTL/TTL COMPATIBLE
- INCLUDES DECODER/DRIVER WITH 5 BIT MEMORY
  - 8421 Positive Logic Input
- 4 x 7 DOT MATRIX ARRAY
  - Shaped Character, Excellent Readibility
- STANDARD .600 INCH x .400 INCH DUAL-IN-LINE PACKAGE INCLUDING CONTRAST FILTER
- CATEGORIZED FOR LUMINOUS INTENSITY
  - Assures Uniformity of Light Output from Unit to Unit within a Single Category



Description

The HP 5082-7300 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory provide a reliable, low-cost method for displaying digital information.

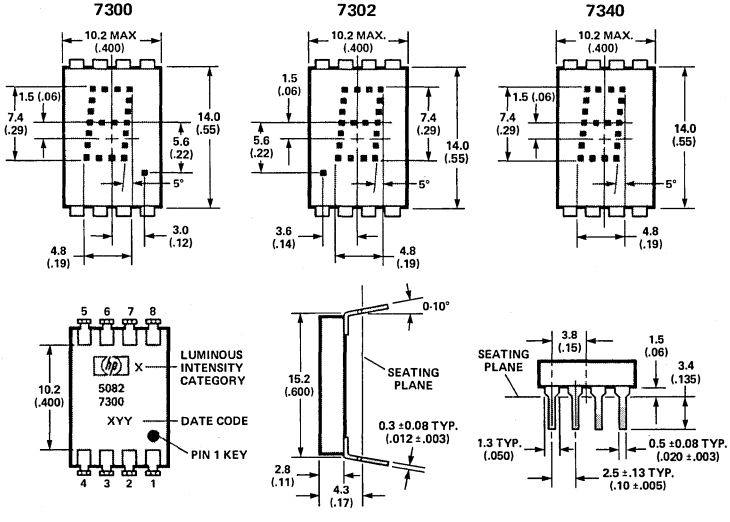
The 5082-7300 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a "-" sign, a test pattern, and four blanks in the invalid BCD states, The unit employs a right-hand decimal point. Typical applications include point-of-sale terminals, instrumentation, and computer systems.

The 5082-7302 is the same as the 5082-7300, except that the decimal point is located on the left-hand side of the digit.

The 5082-7340 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7304 is a (±1.) overrange character, including decimal point, used in instrumentation applications.

Package Dimensions



PIN	FUNCTION	
	5082-7300 and 7302 Numeric	5082-7340 Hexadecimal
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{cc}	V_{cc}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015")
3. Digit center line is ±.25mm (±.01") from package center line.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−40	+100	°C
Operating temperature, case [1,2]	T_C	−20	+85	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			230	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, case	T_C	-20		+85	°C
Enable Pulse Width	t_W	120			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_C = -20° C to +85° C, unless otherwise specified).

Description	Symbol	Test Conditions	Min.	Typ.[4]	Max.	Unit
Supply Current	I_{CC}	V_{CC}=5.5V (Numeral		112	170	mA
Power dissipation	P_T	5 and dp lighted)		560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_C=25° C	32	70		μcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			20	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			2.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+250	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+250	μA
Peak wavelength	λ_{PEAK}	T_C=25° C		655		nm
Dominant Wavelength [8]	λ_d	T_C=25° C		640		nm
Weight				0.8		gm

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50° C/W; Θ_{JC}=15° C/W; 2. Θ_{CA} of a mounted display should not exceed 35° C/W for operation up to T_C = +85° C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_C=25° C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific case temperature, $I_v(T_C)$ may be calculated from this relationship: $I_v(T_C)=I_v$ (25° C) $e^{[-.0188/°C\,(T_C-25°C)]}$ 7. Applies only to 7340. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

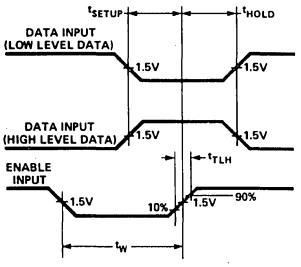


Figure 1. Timing Diagram of 5082-7300 Series Logic.

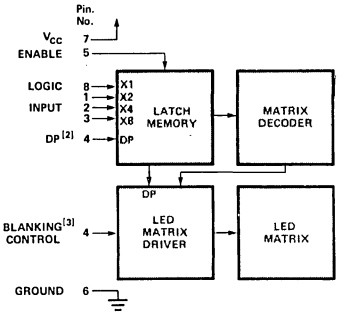


Figure 2. Block Diagram of 5082-7300 Series Logic.

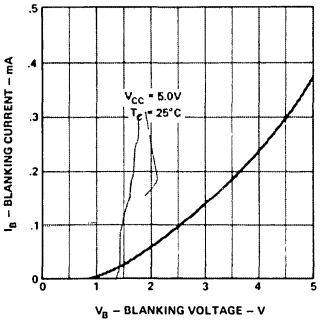


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7340.

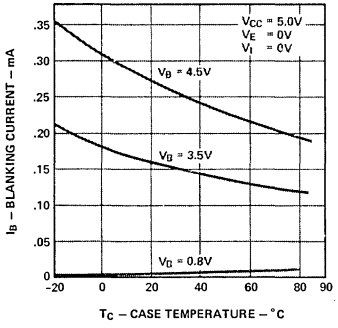


Figure 4. Typical Blanking Control Input Current vs. Temperature 5082-7340.

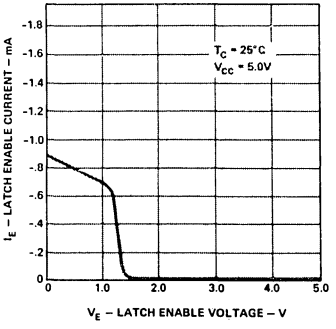


Figure 5. Typical Latch Enable Input Current vs. Voltage for the 5082-7300 Series Devices.

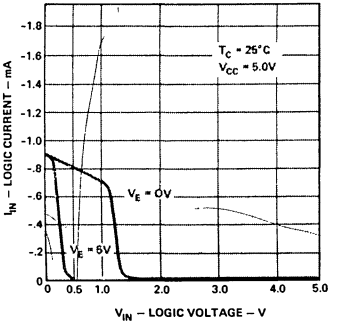


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage for the 5082-7300 Series Devices. Decimal Point Applies to 5082-7300 and -7302 Only.

TRUTH TABLE						
BCD DATA[1]				5082-7300/7302	5082-7340	
X_8	X_4	X_2	X_1			
L	L	L	L	0	0	
L	L	L	H	1	1	
L	L	H	L	2	2	
L	L	H	H	3	3	
L	H	L	L	4	4	
L	H	L	H	5	5	
L	H	H	L	6	6	
L	H	H	H	7	7	
H	L	L	L	8	8	
H	L	L	H	9	9	
H	L	H	L	H	A	
H	L	H	H	(BLANK)	B	
H	H	L	L	(BLANK)	C	
H	H	L	H	-	D	
H	H	H	L	(BLANK)	E	
H	H	H	H	(BLANK)	F	
DECIMAL PT.[2]				ON	V_{DP} = L	
				OFF	V_{DP} = H	
ENABLE[1]				LOAD DATA	V_E = L	
				LATCH DATA	V_E = H	
BLANKING[3]				DISPLAY-ON	V_B = L	
				DISPLAY-OFF	V_B = H	

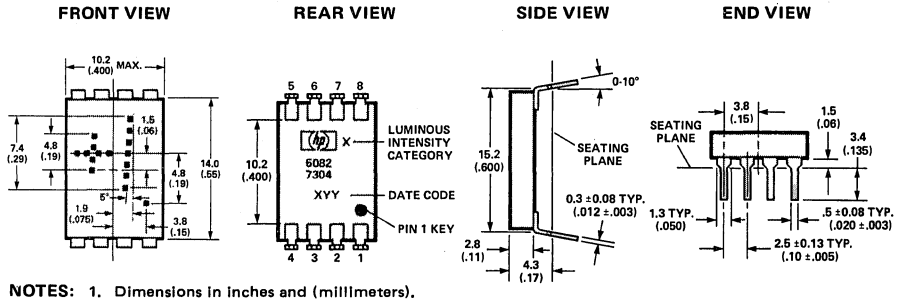
Notes:

1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7300 and 5082-7302 displays.
3. The blanking control input, B, pertains only to the 5082-7340 hexadecimal display. Blanking input has no effect upon display memory.

Solid State Over Range Character

For display applications requiring a ±, 1, or decimal point designation, the 5082-7304 over range character is available. This display module comes in the same package as the 5082-7300 series numeric indicator and is completely compatible with it.

Package Dimensions



PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

NOTES: 1. Dimensions in inches and (millimeters).
2. Unless otherwise specified, the tolerance on all dimensions is ±.015 inches. (± .38mm)

5082–7304

TRUTH TABLE FOR 5082-7304

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Fig. 7 cutoff.
H: Line switching transistor in Fig. 7 saturated.
X: 'don't care'

TYPICAL DRIVING CIRCUIT FOR 5082-7304.

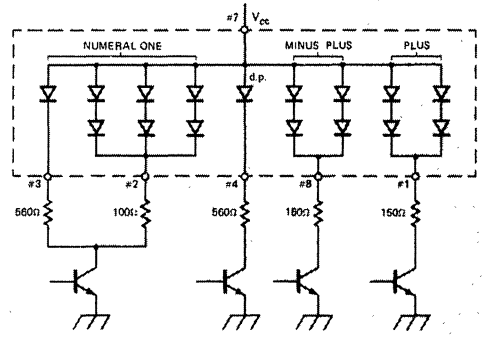


Figure 7.

Absolute Maximum Ratings

DESCRIPTION	SYMBOL	MIN	MAX	UNIT
Storage temperature, ambient	T_s	-40	+100	°C
Operating temperature, case	T_C	-20	+85	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{cc}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to figure 7 for recommended resistor values.

Electrical/Optical Characteristics (T_C = -20°C TO +85°C, UNLESS OTHERWISE SPECIFIED)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		250	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	32	70		µcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Spectral halfwidth	$\Delta\lambda 1/2$	T_C = 25°C		30		nm
Weight				0.8		gm

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COMPONENTS

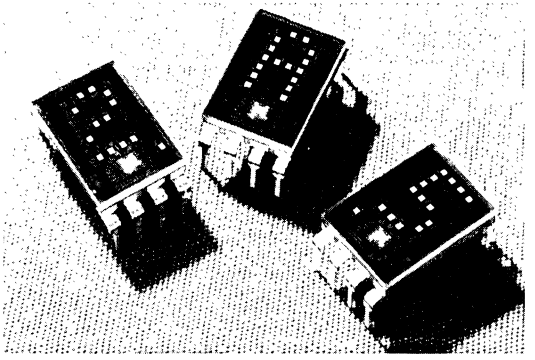
NUMERIC AND HEXADECIMAL DISPLAYS FOR INDUSTRIAL APPLICATIONS

5082-7356
5082-7357
5082-7358
5082-7359

TECHNICAL DATA APRIL 1979

Features

- **CERAMIC/GLASS PACKAGE**
- **ADDED RELIABILITY**
- **NUMERIC 5082-7356/-7357**
  - **0-9, Test State, Minus Sign, Blank States**
  - **Decimal Point**
    - **7356 Right Hand D.P.**
    - **7357 Left Hand D.P.**
- **HEXADECIMAL 5082-7359**
  - **0-9, A-F, Base 16 Operation**
  - **Blanking Control, Conserves Power**
  - **No Decimal Point**
- **TTL COMPATIBLE**
- **INCLUDES DECODER/DRIVER WITH 5 BIT MEMORY**
  - **8421 Positive Logic Input and Decimal Point**
- **4 x 7 DOT MATRIX ARRAY**
  - **Shaped Character, Excellent Readability**
- **STANDARD DUAL-IN-LINE PACKAGE**
  - **15.2mm x 10.2mm (.6 inch x .4 inch)**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  - **Assures Uniformity of Light Output from Unit to Unit within a Single Category**



Description

The HP 5082-7350 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory provide 7.4mm (0.29 inch) displays for use in adverse industrial environments.

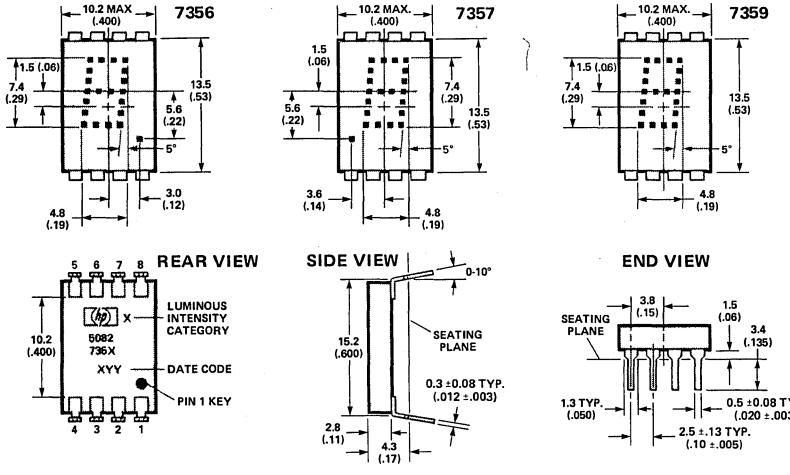
The 5082-7356 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a " –" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point. Typical applications include control systems, instrumentation, communication systems and transportation equipment.

The 5082-7357 is the same as the 5082-7356 except that the decimal point is located on the left-hand side of the digit.

The 5082-7359 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7358 is a "±1." overrange display, including a right hand decimal point.

Package Dimensions



PIN	FUNCTION	
	5082-7356 AND 7357 NUMERIC	5082-7359 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015")
3. Digit center line is ±.25mm (±.01") from package center line.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1,2]	T_A	−55	+100	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ⩽ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient	T_A	0		+70	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_A = 0°C to +70°C, unless otherwise specified).

Description	Symbol	Test Conditions	Min.	Typ.[4]	Max.	Unit
Supply Current	I_{CC}	V_{CC}=5.5V (Numeral		112	170	mA
Power dissipation	P_T	5 and dp lighted)		560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_A=25°C	40	85		μcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			50	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			1.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+100	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+130	μA
Peak wavelength	λ_{PEAK}	T_A=25°C		655		nm
Dominant Wavelength [8]	λ_d	T_A=25°C		640		nm
Weight				1.0		gm

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50°C/W; Θ_{JC}=15°C/W; 2. Θ_{CA} of a mounted display should not exceed 35°C/W for operation up to T_A=+100°C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_A=25°C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A)=I_{V(25°C)}(.985)^{[T_A-25°C]}$ 7. Applies only to 7359. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

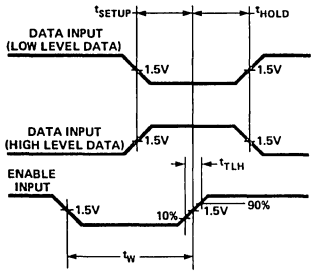


Figure 1. Timing Diagram of 5082-7350 Series Logic.

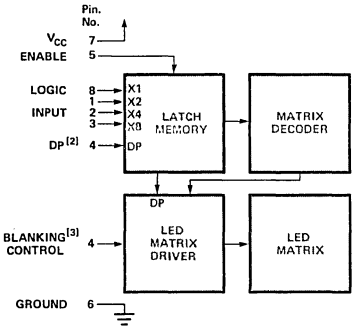


Figure 2. Block Diagram of 5082-7350 Series Logic.

TRUTH TABLE					
BCD DATA[1]				5082-7356/7357	5082-7359
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L		A
H	L	H	H	(BLANK)	b
H	H	L	L	(BLANK)	C
H	H	L	H	-	d
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]			ON		V_{DP} = L
			OFF		V_{DP} = H
ENABLE[1]			LOAD DATA		V_E = L
			LATCH DATA		V_E = H
BLANKING[3]			DISPLAY-ON		V_B = L
			DISPLAY-OFF		V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7356 and 5082-7357 displays.
3. The blanking control input, B, pertains only to the 5082-7359 hexadecimal display. Blanking input has no effect upon display memory.

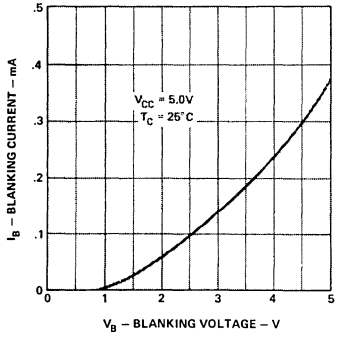


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7359.

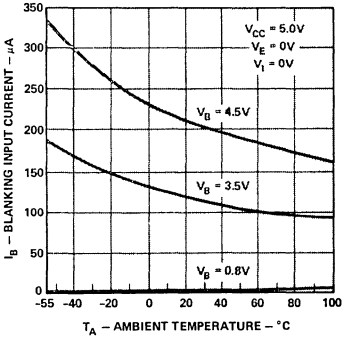


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 5082-7359.

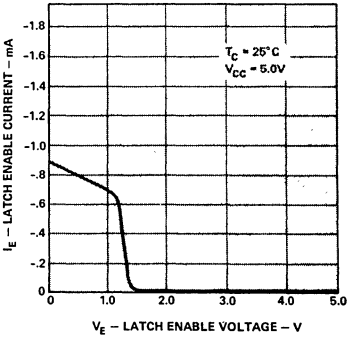


Figure 5. Typical Latch Enable Input Current vs. Voltage.

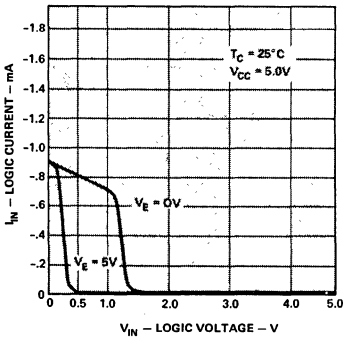


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

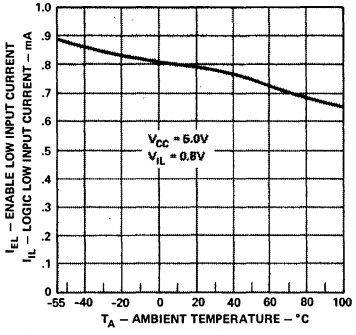


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

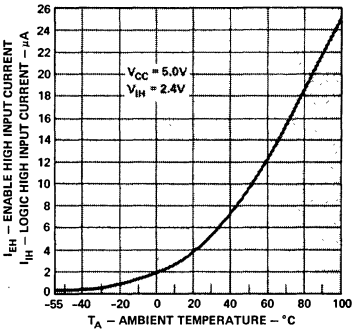


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

ELECTRICAL

The 5082-7350 series devices use a modified 4 x 7 dot matrix of light emitting diodes (LED's) to display decimal/hexadecimal numeric information. The LED's are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7MHz rate.

The blanking control input on the 5082-7395 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$$R_{blank} = (V_{CC} - 3.5V)/[N\ (1.0mA)]$$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as is the BCD data. The decimal point LED is driven by the on-board IC.

MECHANICAL

These hermetic displays are designed for use in adverse industrial environments.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54mm (0.100 inch) and the lead row spacing is 15.24mm (0.600 inch). These displays may be end stacked with 2.54mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100° C, it is important to maintain a case-to-ambient thermal resistance of less than 35° C/watt as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

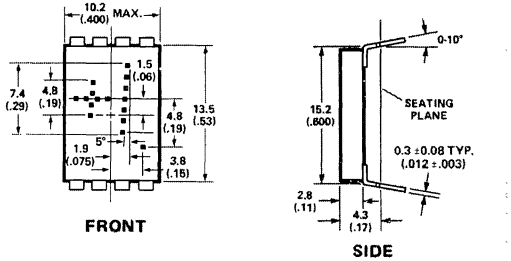
CONTRAST ENHANCEMENT

The 5082-7350 displays have been designed to provide the maximum posible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60 and Dark Red 63, SGL Homalite H100-1605, 3M Light Control Film and Polaroid HRCP Red Circular Polarizing Filter. For further information see Hewlett-Packard Application Note 964.

Solid State Over Range Character

For display applications requiring a ±, 1, or decimal point designation, the 5082-7358 over range character is available. This display module comes in the same package as the 5082-7350 series numeric indicator and is completely compatible with it.

Package Dimensions



NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±.38 MM (± .015 INCHES).

PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{CC}
8	Minus/Plus

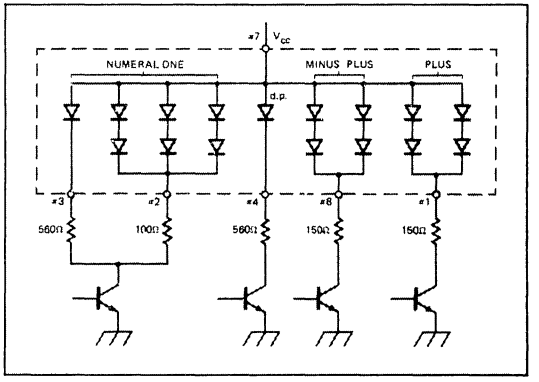


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics

5082-7358 (T_A = 0°C to 70°C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		280	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	40	85		μcd
Peak wavelength	λ_{peak}	T_C = 25°C		655		nm
Dominant Wavelength	λ_d	T_C = 25°C		640		nm
Weight				1.0		gm

Recommended Operating Conditions

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

Absolute Maximum Ratings

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	-65	+125	°C
Operating temperature, ambient	T_A	-55	+100	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

HEWLETT PACKARD

COMPONENTS

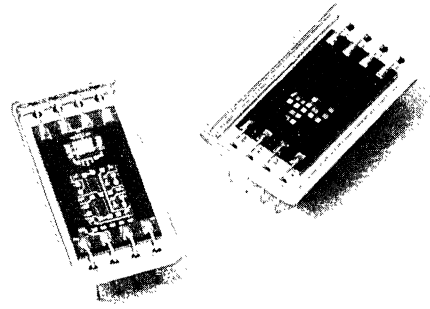
SOLID STATE NUMERIC INDICATOR

5082-7010
5082-7011

TECHNICAL DATA APRIL 1979

Features

- **RUGGED, SHOCK RESISTANT, HERMETIC**
- **DESIGNED TO MEET MIL STANDARDS**
- **INCLUDES DECODER/DRIVER**
  BCD Inputs
- **TTL/DTL COMPATIBLE**
- **CONTROLLABLE LIGHT OUTPUT**
- **5 x 7 LED MATRIX CHARACTER**



Description

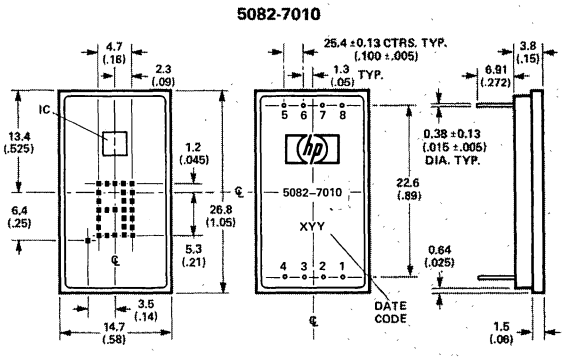
The HP 5082-7010 solid state numeric indicator with built-in decoder/driver provides a hermetically tested 6.8mm (0.27 in.) display for use in military or adverse industrial environments. Typical applications include ground, airborne and shipboard equipment, fire control systems, medical instruments, and space flight systems.

The 5082-7010 is a modified 5x7 matrix display that indicates the numerals 0-9 when presented with a BCD code. The BCD code is negative logic with blanks displayed for invalid codes. A left-hand decimal point is included which must be externally current limited.

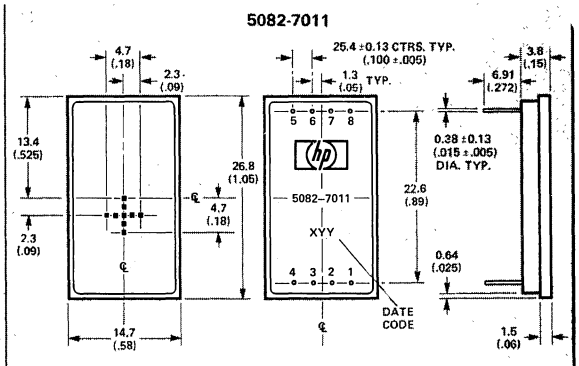
The 5082-7011 is a companion plus/minus sign in the same hermetically tested package. Plus/minus indications require only that voltage be applied to two input pins.

Both displays allow luminous intensity to be varied by changing the DC drive voltage or by pulse duration modulation of the LED voltage.

Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	Input 1	5	Input 4
2	V_{DP}	6	Ground
3	V_{LED}	7	V_{CC}
4	Input 8	8	Input 2



PIN	FUNCTION	PIN	FUNCTION
1	NC	5	NC
2	NC	6	Ground
3	Plus	7	Minus/Plus
4	NC	8	NC

Notes:
1. **Unless otherwise specified, the tolerance on all dimensions is ±0.38 mm. (±0.015 inches).**
2. **All dimensions in millimetres and (inches).**
3. **The package and mounting pins are tin plated Kovar.**

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	−65	+100	°C
Operating Temperature, Case	T_C	−55	+95	°C
Logic Supply Voltage to Ground	V_{CC}	−0.5	+7.0	V
Logic Input Voltage	V_I	−0.5	+5.5	V
LED Supply Voltage to Ground	V_{LED} [1]	−0.5	+5.5	V
Decimal Point Current	I_{DP}		−10	mA

Note: 1. Above T_C = 65°C derate V_{LED} per derating curve in Figure 10.

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Logic Supply Voltage	V_{CC}	4.5	5.0	5.5	V
LED Supply Voltage, Display Off	V_{LED}	−0.5	0	+1.0	V
LED Supply Voltage, Display On	V_{LED}	3.0	4.2	5.5	V
Decimal Point Current	I_{DP}[2]	0	−5.0	−10.0	mA
Logic Input Voltage, "H" State	V_{IH}	2.0		5.5	V
Logic Input Voltage, "L" State	V_{IL}	0		0.8	V

Note: 2. Decimal point current must be externally current limited. See application information.

Electrical/Optical Characteristics

Case Temperature, T_C = 0°C to 70°C, unless otherwise specified

Description	Symbol	Test Conditions		Min.	Typ.[4]	Max.	Unit
Logic Supply Current	I_{CC}	V_{CC} = 5.5V			45	75	mA
LED Supply Current	I_{LED} [3] [5]	V_{CC}	V_{LED}				mA
		5.5V	5.5V		255	350	
		5.5V	4.2V		170	235	
		5.5V	3.5V		125		
Logic Input Current, "H" State (ea. input)	I_{IH}	V_{CC} = 5.5V V_{IH} = 2.4V				100	µA
Logic Input Current, "L" State (ea. input)	I_{IL}	V_{CC} = 5.5V V_{IL} = 0.4V				−1.6	mA
Decimal Point Voltage Drop	V_{LED} − V_{DP}	I_{DP} = −10mA			1.6	2.0	V
Power Dissipation	P_T [3] [5]	V_{CC}	V_{LED}				W
		5.5V	5.5V		1.7	2.3	
		5.5V	4.2V		1.0	1.4	
		5.5V	3.5V		0.7		
Luminous Intensity per LED (digit avg.)	I_V	V_{LED}	T_C				µcd
		5.5V	25°C	60	115		
		4.2V	25°C	40	80		
		3.5V	25°C		50		
Peak Wavelength	λ_{peak}				655		nm
Spectral Halfwidth	$\Delta\lambda_{1/2}$				30		nm
Weight					4.9		gram

Notes: 3. With numeral 8 displayed.
4. All typical values at T_C = 25°C.
5. T_C = 0°C to 65°C for V_{LED} = 5.5V.

Truth Table

Character	Logic X8	X4	X2	X1	
0	H	H	H	H	
1	H	H	H	L	
2	H	H	L	H	
3	H	H	L	L	
4	H	L	H	H	
5	H	L	H	L	
6	H	L	L	H	
7	H	L	L	L	
8	L	H	H	H	
9	L	H	H	L	
Blank	L	H	L	H	
Blank	L	H	L	L	
Blank	L	L	H	H	
Blank	L	L	H	L	
Blank	L	L	L	H	
Blank	L	L	L	L	

V_{IL} = 0.0 to 0.8V
V_{IH} = 2.0 to 5.5V

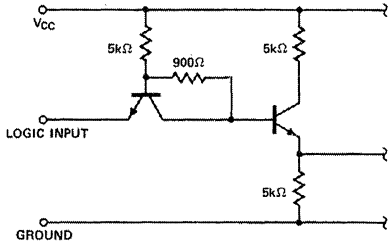


Figure 1. Equivalent input circuit of the 5082-7010 decoder. Note: Display metal case is isolated from ground pin #6.

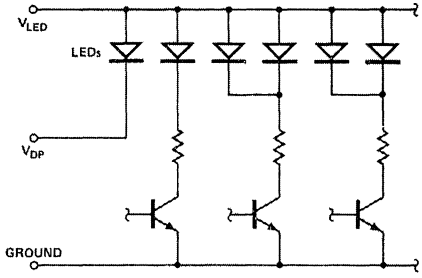


Figure 2. Equivalent circuit of the 5082-7010 as seen from LED and decimal point drive lines.

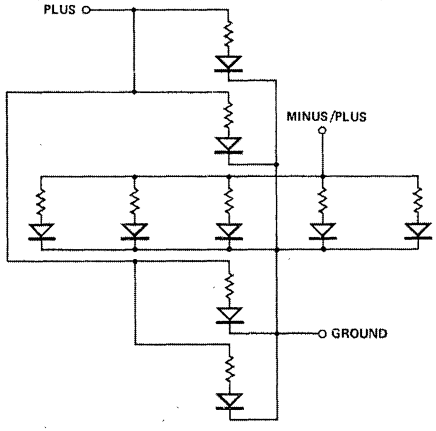


Figure 3. Equivalent circuit of 5082-7011 plus/minus sign. All resistors 345Ω typical. Note: Display metal case is isolated from ground pin #6.

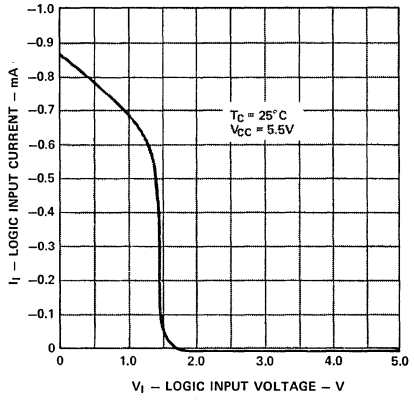


Figure 4. Input current as a function of input voltage, each input.

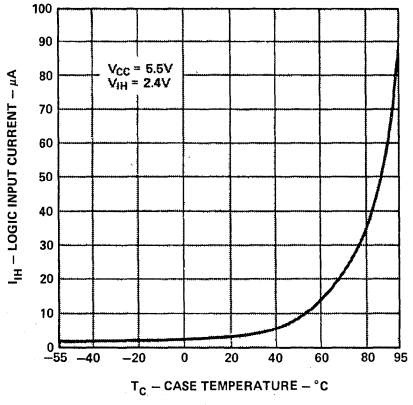


Figure 5. Logic "H" input current as a function of case temperature, each input.

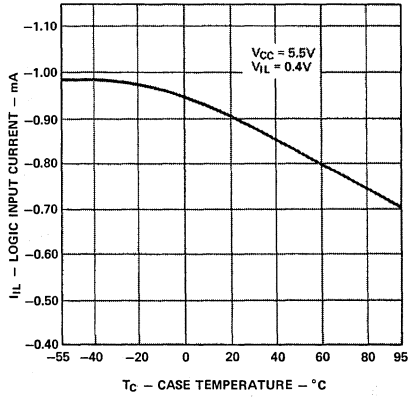


Figure 6. Logic "L" input current as a function of case temperature, each input.

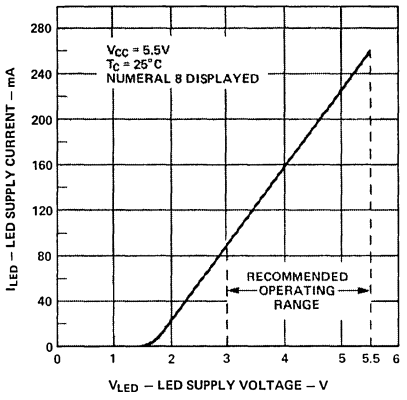


Figure 7. LED supply current as a function of LED supply voltage.

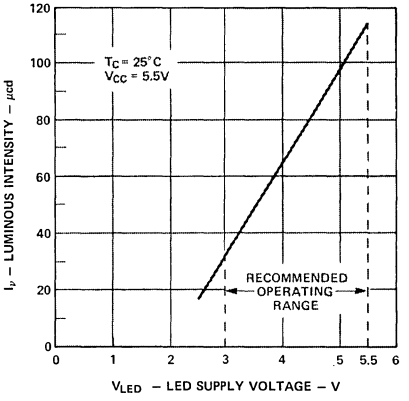


Figure 8. Luminous intensity per LED (digit average) as a function of LED supply voltage.

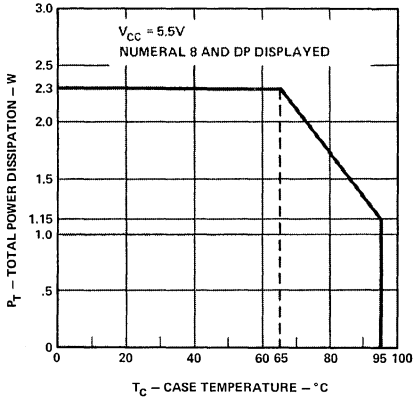


Figure 9. Maximum power derating as a function of case temperature.

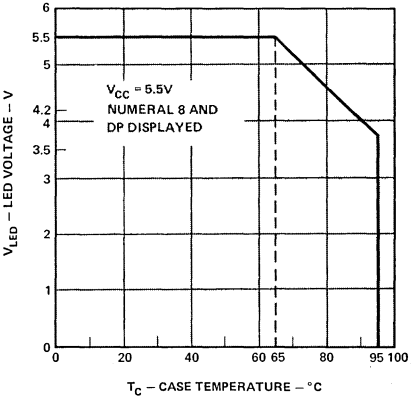


Figure 10. LED voltage derating as a function of case temperature.

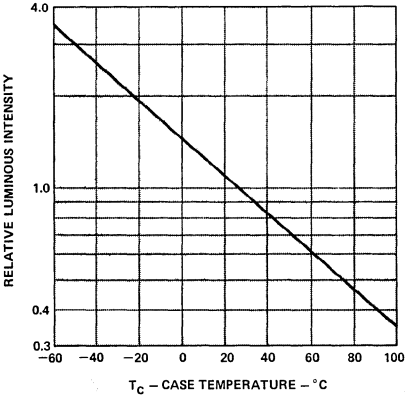


Figure 11. Relative luminous intensity as a function of case temperature at fixed current level.

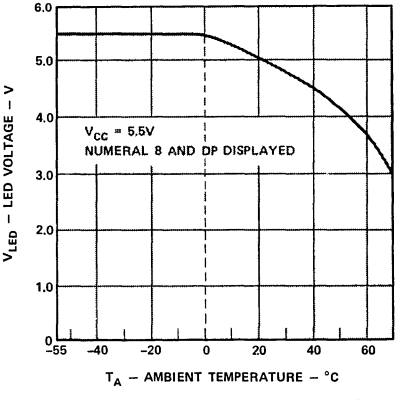


Figure 12. LED voltage derating as a function of ambient temperature, display soldered into P.C. board without heat sink.

Solid State Plus/Minus Sign 5082-7011

For display applications requiring ± designation, the 5082-7011 solid state plus/minus sign is available. This display module comes in the same package as the 5082-7010 numeric indicator and is completely compatible with it. Plus or minus information can be indicated by supplying voltage to one (minus sign) or two (plus sign) input leads. A third lead is provided for the ground connection. Luminous intensity is controlled by changing the LED drive voltage. Each LED has its own built-in 345Ω (nominal) current limiting resistor. Therefore, no external current limiting is required for voltages at 5.5V or lower. Like the numeric indicator, the -7011 plus/minus sign is TTL/DTL compatible.

Truth Table

CHARACTER	PIN	
	3	7
+	H	H
–	L	H
Blank	L	L

V_L = –0.5 to 1.0V

V_H = 3.0 to 5.5V

Electrical /Optical Characteristics

Case Temperature, T_C = 0°C to 70°C, unless otherwise specified

Description	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit
LED Supply Current	I_{LED}	V_{LED} = 5.5V		105	150	mA
		V_{LED} = 4.2V		70	100	
Power Dissipation	P_T	V_{LED} = 5.5V		0.6	0.9	W
		V_{LED} = 4.2V		0.3	0.6	
Luminous Intensity per LED (Digit Avg.)	I_v [2]	V_{LED} = 5.5V	60	115		μcd
		V_{LED} = 4.2V	40	80		
		V_{LED} = 3.5V		50		
Peak Wavelength	λ_{peak}			655		nm
Spectral Halfwidth	$\Delta\lambda_{1/2}$			30		nm
Weight				4.9		gram

Notes:
1. All typical values at T_C = 25°C
2. At T_C = 25°C

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage Temperature, Ambient	T_S	–65	+100	°C
Operating Temperature, Case	T_C	–55	+95	°C
Plus, Plus/Minus Input Potential to Ground	V_{LED}	–0.5	5.5	V

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
LED Supply Voltage, Display Off	V_{LED}	–0.5	0	1.0	V
LED Supply Voltage, Display On	V_{LED}	3.0	4.2	5.5	V

Applications

Decimal Point Limiting Resistor

The decimal point of the 5082-7010 display requires an external current limiting resistor, between pin 2 and ground. Recommended resistor value is 220Ω, 1/4 watt.

Mounting

The 5082-7010 and 5082-7011 displays are packaged with two rows of 4 contact pins each in a DIP configuration with a row center line spacing of 0.890 inches.

Normal mounting is directly onto a printed circuit board. If desired, these displays may be socket mounted using contact strip connectors such as Augat's 325-AGI or AMP 583773-1 or 583774-1.

Heat Sink Operation

Optimum display case operating temperature for the 5082-7010 and 7011 displays is T_C=0°C to 70°C as measured on back surface. Maintaining the display case operating temperature within this range may be achieved by mounting the display on an appropriate heat sink or metal core printed circuit board. Thermal conducting compound such as Wakefield 120 or Dow Corning 340 can be used between display and heat sink. See figure 10 for V_{LED} derating vs. display case temperature.

Operation Without Heat Sink

These displays may also be operated without the use of a heat sink. The thermal resistance from case to ambient for these displays when soldered into a printed circuit board is nominally θ_{CA}=30°C/W. See figure 12 for V_{LED} derating vs. ambient temperature.

Cleaning

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

HEWLETT hp PACKARD

COMPONENTS

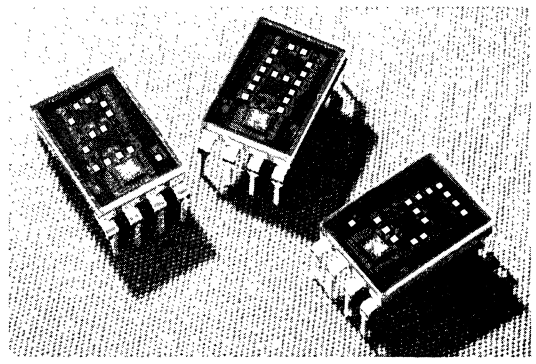
HERMETIC NUMERIC AND HEXADECIMAL DISPLAYS FOR HIGH RELIABILITY APPLICATIONS

5082-7391
5082-7392
5082-7393
5082-7395

TECHNICAL DATA APRIL 1979

Features

- **PERFORMANCE GUARANTEED OVER TEMPERATURE**
- **HERMETICITY GUARANTEED**
- **TXV SCREENING AVAILABLE**
- **GOLD PLATED LEADS**
- **HIGH TEMPERATURE STABILIZED**
- **NUMERIC**
  5082-7391 Right Hand D.P.
  5082-7392 Left Hand D.P.
- **HEXADECIMAL**
  5082-7395
- **TTL COMPATIBLE**
- **DECODER/DRIVER WITH 5 BIT MEMORY**
- **4 x 7 DOT MATRIX ARRAY**
  Shaped Character, Excellent Readability
- **STANDARD DUAL-IN-LINE PACKAGE**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output from Unit to Unit within a Single Category



Description

The HP 5082-7390 series solid state numeric and hexadecimal indicators with on-board decoder/driver and memory are hermetically tested 7.4mm (0.29 inch) displays for use in military and aerospace applications.

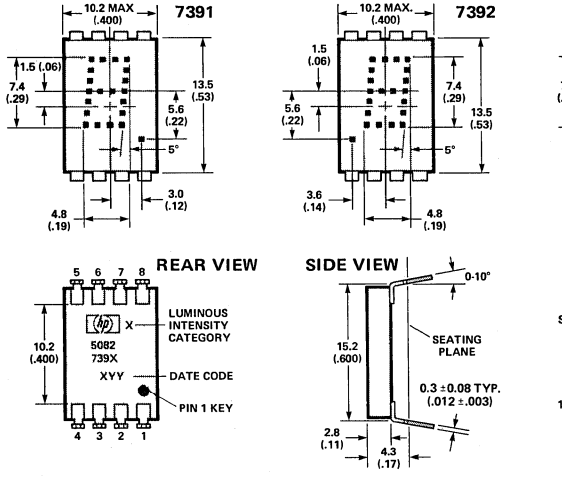
The 5082-7391 numeric indicator decodes positive 8421 BCD logic inputs into characters 0-9, a " −" sign, a test pattern, and four blanks in the invalid BCD states. The unit employs a right-hand decimal point. Typical applications include control systems, instrumentation, communication systems and transportation equipment.

The 5082-7392 is the same as the 5082-7391 except that the decimal point is located on the left-hand side of the digit.

The 5082-7395 hexadecimal indicator decodes positive 8421 logic inputs into 16 states, 0-9 and A-F. In place of the decimal point an input is provided for blanking the display (all LED's off), without losing the contents of the memory. Applications include terminals and computer systems using the base-16 character set.

The 5082-7393 is a "±1." overrange display, including a right hand decimal point.

Package Dimensions



PIN	FUNCTION	
	5082-7391 AND 7392 NUMERIC	5082-7395 HEXA-DECIMAL
1	Input 2	Input 2
2	Input 4	Input 4
3	Input 8	Input 8
4	Decimal point	Blanking control
5	Latch enable	Latch enable
6	Ground	Ground
7	V_{CC}	V_{CC}
8	Input 1	Input 1

NOTES:
1. Dimensions in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±.38mm (±.015").
3. Digit center line is ±.25mm (±.01") from package center line.
4. Lead material is gold plated copper alloy.

Absolute Maximum Ratings

Description	Symbol	Min.	Max.	Unit
Storage temperature, ambient	T_S	−65	+125	°C
Operating temperature, ambient [1,2]	T_A	−55	+100	°C
Supply voltage [3]	V_{CC}	−0.5	+7.0	V
Voltage applied to input logic, dp and enable pins	V_I, V_{DP}, V_E	−0.5	+7.0	V
Voltage applied to blanking input [7]	V_B	−0.5	V_{CC}	V
Maximum solder temperature at 1.59mm (.062 inch) below seating plane; t ≤ 5 seconds			260	°C

Recommended Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Operating temperature, ambient [1,2]	T_A	−55		+100	°C
Enable Pulse Width	t_W	100			nsec
Time data must be held before positive transition of enable line	t_{SETUP}	50			nsec
Time data must be held after positive transition of enable line	t_{HOLD}	50			nsec
Enable pulse rise time	t_{TLH}			200	nsec

Electrical/Optical Characteristics (T_A = −55°C to +100°C, unless otherwise specified)

Description	Symbol	Test Conditions	Min.	Typ. [4]	Max.	Unit
Supply Current	I_{CC}	V_{CC}=5.5V (Numeral		112	170	mA
Power dissipation	P_T	5 and dp lighted)		560	935	mW
Luminous intensity per LED (Digit average) [5,6]	I_v	V_{CC}=5.0V, T_A=25°C	40	85		μcd
Logic low-level input voltage	V_{IL}	V_{CC}=4.5V			0.8	V
Logic high-level input voltage	V_{IH}		2.0			V
Enable low-voltage; data being entered	V_{EL}				0.8	V
Enable high-voltage; data not being entered	V_{EH}		2.0			V
Blanking low-voltage; display not blanked [7]	V_{BL}				0.8	V
Blanking high-voltage; display blanked [7]	V_{BH}		3.5			V
Blanking low-level input current [7]	I_{BL}	V_{CC}=5.5V, V_{BL}=0.8V			50	μA
Blanking high-level input current [7]	I_{BH}	V_{CC}=5.5V, V_{BH}=4.5V			1.0	mA
Logic low-level input current	I_{IL}	V_{CC}=5.5V, V_{IL}=0.4V			−1.6	mA
Logic high-level input current	I_{IH}	V_{CC}=5.5V, V_{IH}=2.4V			+100	μA
Enable low-level input current	I_{EL}	V_{CC}=5.5V, V_{EL}=0.4V			−1.6	mA
Enable high-level input current	I_{EH}	V_{CC}=5.5V, V_{EH}=2.4V			+130	μA
Peak wavelength	λ_{PEAK}	T_A=25°C		655		nm
Dominant Wavelength [8]	λ_d	T_A=25°C		640		nm
Weight				1.0		gm
Leak Rate					$5x10^{-7}$	cc/sec

Notes: 1. Nominal thermal resistance of a display mounted in a socket which is soldered into a printed circuit board: Θ_{JA}=50°C/W; Θ_{JC}=15°C/W. 2. Θ_{CA} of a mounted display should not exceed 35°C/W for operation up to T_A=+100°C. 3. Voltage values are with respect to device ground, pin 6. 4. All typical values at V_{CC}=5.0 Volts, T_A=25°C. 5. These displays are categorized for luminous intensity with the intensity category designated by a letter located on the back of the display contiguous with the Hewlett-Packard logo marking. 6. The luminous intensity at a specific ambient temperature, $I_V(T_A)$, may be calculated from this relationship: $I_V(T_A)=I_{V(25°C)}(.985)^{[T_A-25°C]}$ 7. Applies only to 7395. 8. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.

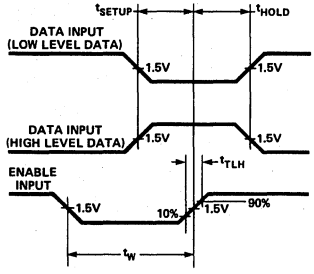


Figure 1. Timing Diagram of 5082-7390 Series Logic.

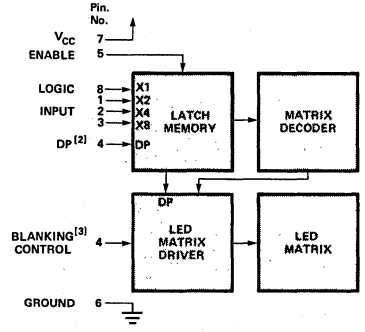


Figure 2. Block Diagram of 5082-7390 Series Logic.

TRUTH TABLE					
BCD DATA[1]				5082-7391/7392	5082-7395
X_8	X_4	X_2	X_1		
L	L	L	L	0	0
L	L	L	H	1	1
L	L	H	L	2	2
L	L	H	H	3	3
L	H	L	L	4	4
L	H	L	H	5	5
L	H	H	L	6	6
L	H	H	H	7	7
H	L	L	L	8	8
H	L	L	H	9	9
H	L	H	L	A	A
H	L	H	H	(BLANK)	B
H	H	L	L	(BLANK)	C
H	H	L	H	-	D
H	H	H	L	(BLANK)	E
H	H	H	H	(BLANK)	F
DECIMAL PT.[2]				ON	V_{DP} = L
				OFF	V_{DP} = H
ENABLE[1]				LOAD DATA	V_E = L
				LATCH DATA	V_E = H
BLANKING[3]				DISPLAY-ON	V_B = L
				DISPLAY-OFF	V_B = H

Notes:
1. H = Logic High; L = Logic Low. With the enable input at logic high changes in BCD input logic levels or D.P. input have no effect upon display memory, displayed character, or D.P.
2. The decimal point input, DP, pertains only to the 5082-7391 and 5082-7392 displays.
3. The blanking control input, B, pertains only to the 5082-7395 hexadecimal display. Blanking input has no effect upon display memory.

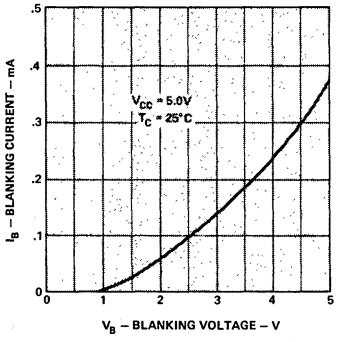


Figure 3. Typical Blanking Control Current vs. Voltage for 5082-7395.

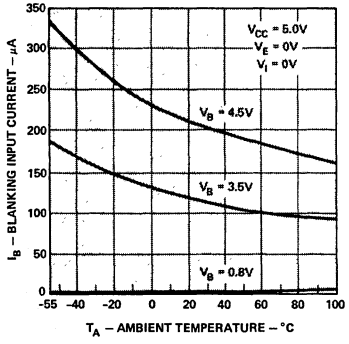


Figure 4. Typical Blanking Control Input Current vs. Ambient Temperature for 5082-7395.

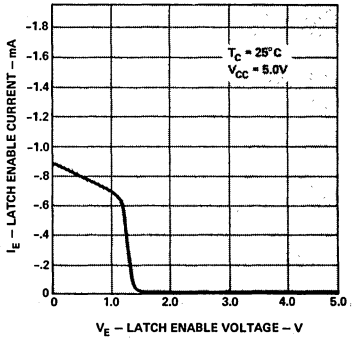


Figure 5. Typical Latch Enable Input Current vs. Voltage.

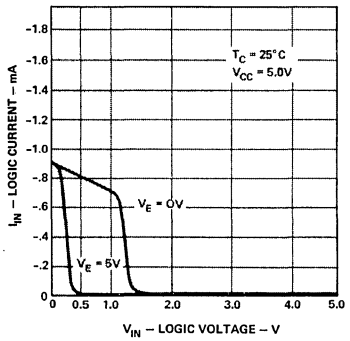


Figure 6. Typical Logic and Decimal Point Input Current vs. Voltage.

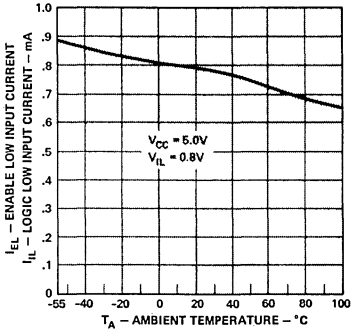


Figure 7. Typical Logic and Enable Low Input Current vs. Ambient Temperature.

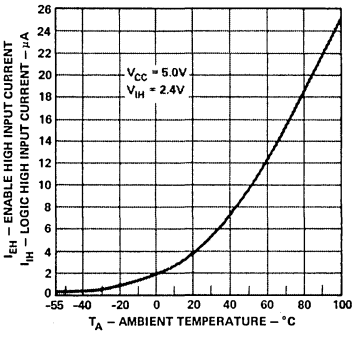


Figure 8. Typical Logic and Enable High Input Current vs. Ambient Temperature.

Operational Considerations

ELECTRICAL

The 5082-7390 series devices use a modified 4 x 7 dot matrix of light emitting diodes (LED's) to display decimal/hexadecimal numeric information. The LED's are driven by constant current drivers. BCD information is accepted by the display memory when the enable line is at logic low and the data is latched when the enable is at logic high. To avoid the latching of erroneous information, the enable pulse rise time should not exceed 200 nanoseconds. Using the enable pulse width and data setup and hold times listed in the Recommended Operating Conditions allows data to be clocked into an array of displays at a 6.7MHz rate.

The blanking control input on the 5082-7395 display blanks (turns off) the displayed hexadecimal information without disturbing the contents of display memory. The display is blanked at a minimum threshold level of 3.5 volts. This may be easily achieved by using an open collector TTL gate and a pull-up resistor. For example, (1/6) 7416 hexinverter buffer/driver and a 120 ohm pull-up resistor will provide sufficient drive to blank eight displays. The size of the blanking pull-up resistor may be calculated from the following formula, where N is the number of digits:

$$R_{blank} = (V_{CC} - 3.5V)/[N\ (1.0mA)]$$

The decimal point input is active low true and this data is latched into the display memory in the same fashion as is the BCD data. The decimal point LED is driven by the on-board IC.

MECHANICAL

5082-7390 series displays are hermetically tested for use in environments which require a high reliability device. These displays are designed and tested to meet a helium leak rate of 5×10^{-7} cc/sec and a standard dye penetrant gross leak test.

These displays may be mounted by soldering directly to a printed circuit board or inserted into a socket. The lead-to-lead pin spacing is 2.54mm (0.100 inch) and the lead row spacing is 15.24mm (0.600 inch). These displays may be end stacked with 2.54mm (0.100 inch) spacing between outside pins of adjacent displays. Sockets such as Augat 324-AG2D (3 digits) or Augat 508-AG8D (one digit, right angle mounting) may be used.

The primary thermal path for power dissipation is through the device leads. Therefore, to insure reliable operation up to an ambient temperature of +100° C, it is important to maintain a case-to-ambient thermal resistance of less than 35° C/watt as measured on top of display pin 3.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

PRECONDITIONING

5082-7390 series displays are 100% preconditioned by 24 hour storage at 125° C.

CONTRAST ENHANCEMENT

The 5082-7390 displays have been designed to provide the maximum posible ON/OFF contrast when placed behind an appropriate contrast enhancement filter. Some suggested filters are Panelgraphic Ruby Red 60 and Dark Red 63, SGL Homalite H100-1605, 3M Light Control Film and Polaroid HRCP Red Circular Polarizing Filter. For further information see Hewlett-Packard Application Note 964.

High Reliability Test Program

Hewlett-Packard provides standard high reliability test programs, patterned after MIL-M-38510 in order to facilitate the use of HP products in military programs.

HP offers two levels of high reliability testing:

The TXV prefix identifies a part which has been preconditioned and screened per Table 1.

The TXVB prefix identifies a part which has been preconditioned and screened per Table 1, and comes from a lot which has been subjected to the Group B tests described in Table 2.

PART NUMBER SYSTEM

Standard Product	With TXV Screening	With TXV Screening Plus Group B
5082-7391	TXV-7391	TXVB-7391
5082-7392	TXV-7392	TXVB-7392
5082-7395	TXV-7395	TXVB-7395

Table 1. TXV Preconditioning and Screening — 100%.

Examination or Test	MIL-STD-883 Methods	Conditions
1. Internal Visual Inspection	HP Procedure A-5956-7572-52	
2. Electrical Test: I_V, I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH}.		Per Electrical/Optical Characterstics.
3. High Temperature Storage	1008	125°C, 168 hours.
4. Temperature Cycling	1010	−65°C to +125°C, 10 cycles.
5. Acceleration	2001	2,000 G, Y_1 orientation.
6. Helium Leak Test	1014	Condition A
7. Gross Leak Test	1014	Condition D
8. Electrical Test: Same as Step 2		
9. Burn-in	1015	T_A=100°C, t=168 hours, at V_{CC}=5.0V and cycling through logic at 1 character per sec.
10. Electrical Test as in Step 2		
11. Sample Electrical Test Over Temperature: I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH}		Per Electrical Characteristics, T_A = -55°C, LTPD = 7
12. Sample Electrical Test Over Temperature I_{CC}, I_{BL}, I_{BH}, I_{EL}, I_{EH}, I_{IL}, I_{IH}		Per Electrical Characteristics, T_A = +100°C, LTPD = 7
13. External Visual	2009	

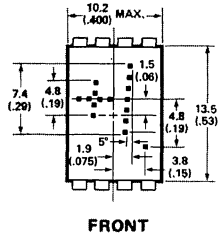
Table 2. Group B.

Examination or Test	MIL-STD-883 Method	MIL-STD-883 Condition	LTPD
Subgroup 1			20
Physical Dimensions	2008	Package Dimensions per Product Outline Drawing.	
Subgroup 2			15
Solderability	2003	Immersion within 0.062" of seating plane 260°C, t=5 sec., omit aging.	
Temperature Cycling	1010	10 cycles −65°C to +125°C	
Thermal Shock	1011	Test Condition A	
Hermetic Seal	1014	Condition A and Condition D	
Moisture Resistance	1004	Omit initial conditioning.	
End Points: Electrical Test		Same as Step 2, Table 1.	
Subgroup 3			15
Shock – Non-operating	2002	1500 G, t=0.5ms, 5 blows in each orientation X_1, Y_1, Y_2.	
Vibration Variable Frequency	2007	Non-operating.	
Constant Acceleration	2001	2,000 G, Y_1 orientation.	
End Points: Electrical Test		Same as Step 2, Table 1.	
Subgroup 4			15
Terminal Strength	2004	Test Condition B2.	
End Points: Hermetic Seal	1014	Condition A and Condition D	
Subgroup 5			15
Salt Atmosphere	1009	Test Condition A	
Subgroup 6			λ=7
High Temperature Life	1008	T_A=125°C, non-operating, t=1000 hours.	
End Points: Electrical Test		Same as Step 2, Table 1.	
Subgroup 7			λ=5
Steady State Operating Life	1005	T_A=100°C, t=1000 hours, at V_{CC}=5.0V and cycling through logic at 1 character per second.	
End Points: Electrical Test		Same as Step 2, Table 1.	

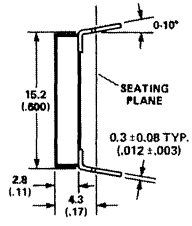
Solid State Over Range Character

For display applications requiring a ±, 1, or decimal point designation, the 5082-7393 over range character is available.This display module comes in the same package as the 5082-7390 series numeric indicator and is completely compatible with it.

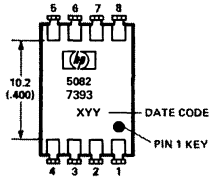
Package Dimensions



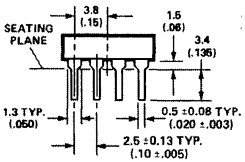
FRONT



SIDE



REAR



END

NOTES:
1. DIMENSIONS IN MILLIMETRES AND (INCHES).
2. UNLESS OTHERWISE SPECIFIED, THE TOLERANCE ON ALL DIMENSIONS IS ±.38 MM (± .015 INCHES).

PIN	FUNCTION
1	Plus
2	Numeral One
3	Numeral One
4	DP
5	Open
6	Open
7	V_{cc}
8	Minus/Plus

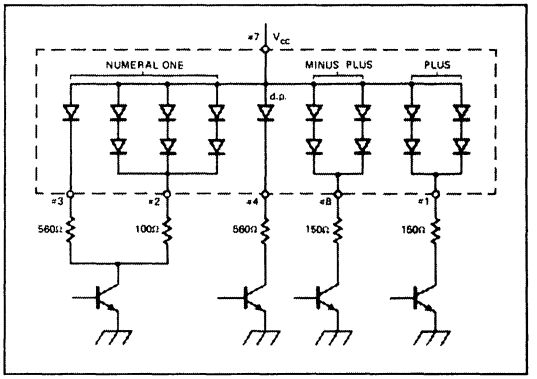


Figure 9. Typical Driving Circuit.

TRUTH TABLE

CHARACTER	PIN			
	1	2,3	4	8
+	H	X	X	H
–	L	X	X	H
1	X	H	X	X
Decimal Point	X	X	H	X
Blank	L	L	L	L

NOTES: L: Line switching transistor in Figure 9 cutoff.
H: Line switching transistor in Figure 9 saturated.
X: 'Don't care'

Electrical/Optical Characteristics

5082-7393 (T_A = -55°C to +100°C, Unless Otherwise Specified)

DESCRIPTION	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Forward Voltage per LED	V_F	I_F = 10 mA		1.6	2.0	V
Power dissipation	P_T	I_F = 10 mA all diodes lit		280	320	mW
Luminous Intensity per LED (digit average)	I_v	I_F = 6 mA T_C = 25°C	40	85		μcd
Peak wavelength	λpeak	T_C = 25°C		655		nm
Dominant Wavelength	λ_d	T_C = 25°C		640		nm
Weight				1.0		gm

Recommended Operating Conditions

	SYMBOL	MIN	NOM	MAX	UNIT
LED supply voltage	V_{CC}	4.5	5.0	5.5	V
Forward current, each LED	I_F		5.0	10	mA

NOTE:
LED current must be externally limited. Refer to Figure 9 for recommended resistor values.

Absolute Maximum Ratings

DESCRIPTION	SYMBOL	MIN.	MAX.	UNIT
Storage temperature, ambient	T_S	-65	+125	°C
Operating temperature, ambient	T_A	-55	+100	°C
Forward current, each LED	I_F		10	mA
Reverse voltage, each LED	V_R		4	V

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COMPONENTS

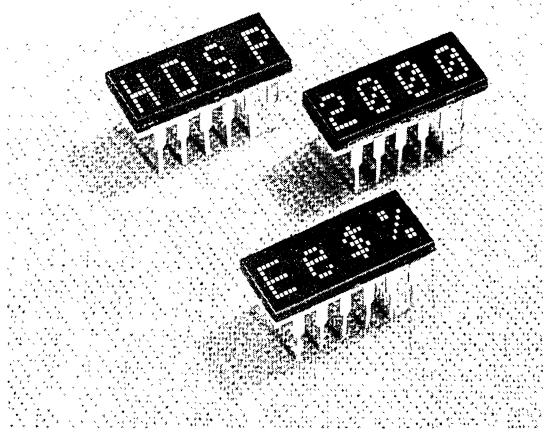
FOUR CHARACTER SOLID STATE ALPHANUMERIC DISPLAY

HDSP-2000

TECHNICAL DATA APRIL 1979

Features

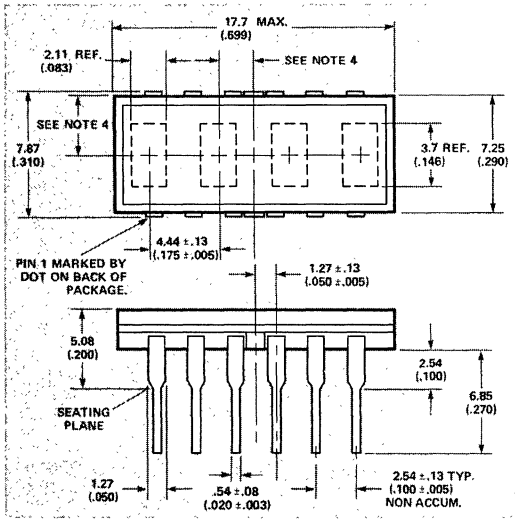
- **INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS**
- **CERAMIC 7.62 mm (.3 in.) DIP**
  Integral Red Glass Contrast Filter
- **WIDE VIEWING ANGLE**
- **END STACKABLE 4 CHARACTER PACKAGE**
- **PIN ECONOMY**
  12 Pins for 4 Characters
- **TTL COMPATIBLE**
- **5x7 LED MATRIX DISPLAYS FULL ASCII CODE**
- **RUGGED, LONG OPERATING LIFE**
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Ease of Package to Package Brightness Matching



Description

The HP HDSP-2000 display is a 3.8mm (0.15 inch) 5x7 LED array for display of alphanumeric information. The device is available in 4 character clusters and is packaged in a 12-pin dual-in-line type package. An on-board SIPO (serial-in-parallel-out) 7 bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing. The constant current LED drivers are externally programmable and typically capable of sinking 13.5mA peak per diode. Applications include interactive I/O terminals, point of sale equipment, portable telecommunications gear, and hand held equipment requiring alphanumeric displays.

Package Dimensions



PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38 mm (±.015")
3. LEAD MATERIAL IS GOLD PLATED COPPER ALLOY.
4. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±.13mm (±.005").

Absolute Maximum Ratings

Supply Voltage V_{CC} to Ground ..... −0.5V to 6.0V
Inputs, Data Out and V_B ..... −0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... −0.5V to +6.0V
Free Air Operating Temperature Range, T_A[2] ..... −20°C to +70°C
Storage Temperature Range, T_S ..... -55°C to +100°C
Maximum Allowable Package Dissipation at T_A = 25°C[1,2,6] ..... 1.70 Watts
Maximum Solder Temperature 1.59mm (.063") Below Seating Plane t<5 secs ..... 260°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Data Out Current, Low State	I_{OL}			1.6	mA
Data Out Current, HighState	I_{OH}			−0.5	mA
Column Input Voltage, Column On	V_{COL}	2.6		V_{CC}	V
Setup Time	t_{setup}	70	45		ns
Hold Time	t_{hold}	30	0		ns
Width of Clock	$t_{w(Clock)}$	75			ns
Clock Frequency	f_{clock}	0		3	MHz
Clock Transition Time	t_{THL}			200	ns
Free Air Operating Temperature Range	T_A	−20		70	°C

Electrical Characteristics Over Operating Temperature Range

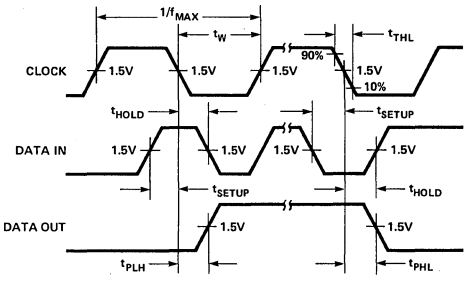
(Unless otherwise specified.)

Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		45	60	mA
				V_B = 2.4V		73	95	mA
Column Current at any Column Input		I_{COL}	V_{CC} = V_{COL} = 5.25V, All SR Stages = Logical 1	V_B=0.4V			1.5	mA
Column Current at any Column Input		I_{COL}		V_B=2.4V		335	410	mA
Peak Luminous Intensity per LED[3,7] (Character Average)		I_{vPEAK}	V_{CC} = 5.0V, V_{COL} = 3.5V, T_i = 25°C[4] V_B=2.4V		105	200		µcd
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = V_{COL} = 4.75V		2.0			V
V_B, Clock or Data Input Threshold Low		V_{IL}					0.8	V
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA
	Data In	I_{IH}				10	40	µA
Input Current Logical 0	V_B,Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA
	Data In	I_{IL}				-250	-400	µA
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = −0.5mA, V_{COL} = 0V		2.4	3.4		V
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6mA, V_{COL} = 0V			0.2	0.4	V
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 2.6V, 15 LEDs on per character, V_B = 2.4V			0.66		W
Peak Wavelength		λ_{PEAK}				655		nm
Dominant Wavelength[5]		λ_d				639		nm

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.
**Power dissipation per package with 4 characters illuminated.

NOTES:
1. Maximum absolute dissipation is with the device in a socket having a thermal resistance from pins to ambient of 35°C/watt.
2. The device should be derated linearly above 25°C at 16mW/°C (see Electrical Description on page 3).
3. The characters are categorized for Luminous Intensity with the intensity category designated by a letter code on the bottom of the package.
4. T_i refers to the initial case temperature of the device immediately prior to the light measurement.
5. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
6. Maximum allowable dissipation is derived from V_{CC} = V_B = V_{COL} = 5.25 Volts, 20 LEDs on per character.
7. The luminous stearance of the LED may be calculated using the following relationships:

L_v (Lux) = I_v (Candela)/A (Metre)^2
L_v (Footlamberts) = πI_v (Candela)/A (Foot)^2
A = 5.3 x 10^{-8} M^2 = 5.8 x 10^{-7} (Foot)^2



Parameter	Condition	Min.	Typ.	Max.	Units
f_{max} Max. CLOCK Rate		3			MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics. (V_{CC} = 5V, T_A = -20°C to +70°C)

Mechanical and Thermal Considerations

The HDSP-2000 is available in a standard 12 lead ceramic-glass dual in-line package. It is designed for plugging into DIP sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size.

The -2000 can be operated over a wide range of temperature and supply voltages. Full power operation at T_A = 25°C (V_{CC} = V_B = V_{COL} = 5.25V) is possible by providing a total thermal resistance from the seating plane of the pins to ambient of 35°C/W/cluster maximum. For operation above T_A = 25°C, the maximum device dissipation should be derated above 25°C at 16mW/°C (see Figure 2). Power derating can be achieved by either decreasing V_{COL} or decreasing the average drive current through pulse width modulation of V_B.

The -2000 display has an integral contrast enhancement filter in the glass lens. Additional front panel contrast filters may by desirable in most actual display applications. Some suggested filters are Panelgraphic Ruby Red 60, SGL Homalite H100-1605 and Plexiglass 2423. Hewlett-Packard Application Note 964 treats this subject in greater detail.

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

Electrical Description

The HDSP-2000 four character alphanumeric display has been designed to allow the user maximum flexibility in interface electronics design. Each four character display module features Data In and Data Out terminals arrayed for easy PC board interconnection such that display strings of up to 80 digits may be driven from a single character generator. Data Out represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the Clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the HDSP-2000. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5x7 diode array.

The reference current for the current mirror is generated from the output voltage of the V_B input buffer applied across the resistor R. The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

The normal mode of operation is depicted in the block diagram of Figure 6. In this circuit, binary input data for digit 4, column 1 is decoded by the 7 line output ROM and then loaded into the 7 on board shift register locations 1 through 7 through a parallel-in-serial-out shift register. Column 1 data for digits 3, 2 and 1 is similarly decoded and shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5(t+T)}$$

The time frame, t + T, allotted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary

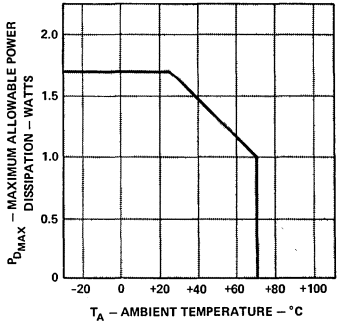


Figure 2. Maximum Allowable Power Dissipation vs. Temperature.

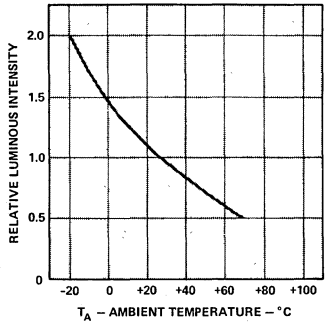


Figure 3. Relative Luminous Intensity vs. Temperature.

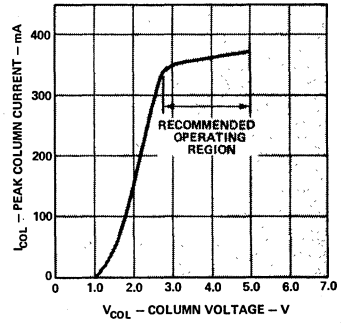


Figure 4. Peak Column Current vs. Column Voltage.

to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With 5 columns to be addressed, this refresh rate then gives a value for the time t + T of:

$1/[5 \times (100)] = 2$ msec.

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain $t \ll T$. For short display strings, the duty factor will then approach 20%. For longer display strings operation at column duty factors of less than 10% will still provide adequate display intensity in most applications. For further applications information, refer to HP Application Note 966 and Application Note 1001.

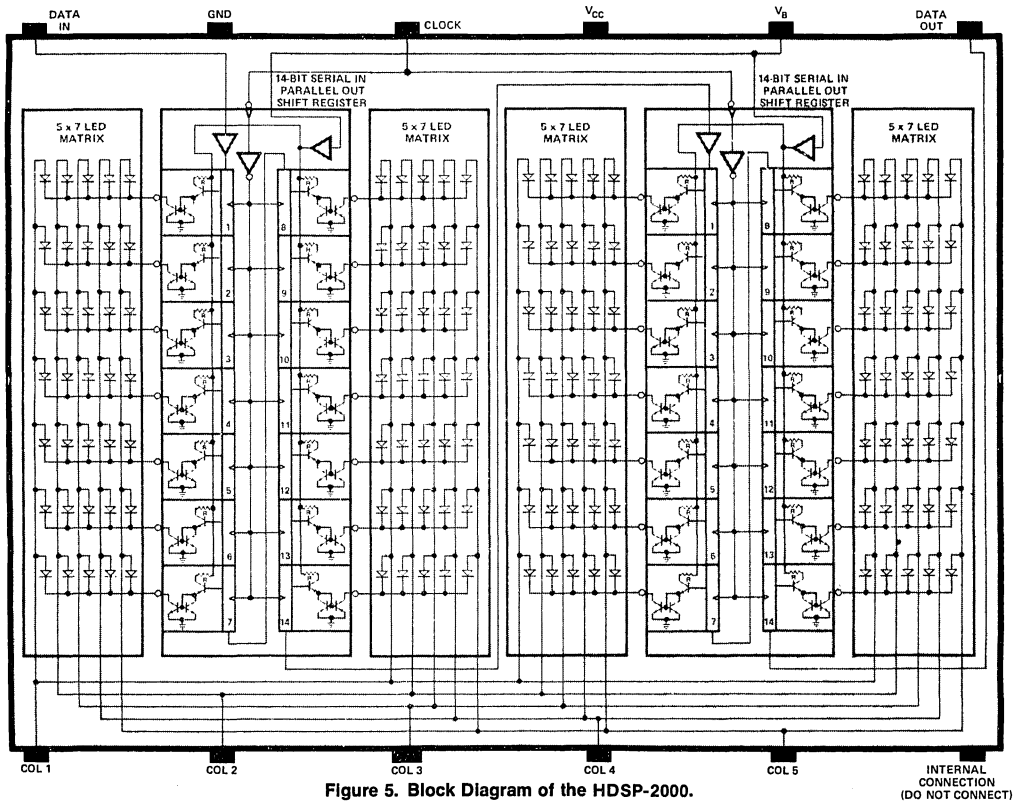


Figure 5. Block Diagram of the HDSP-2000.

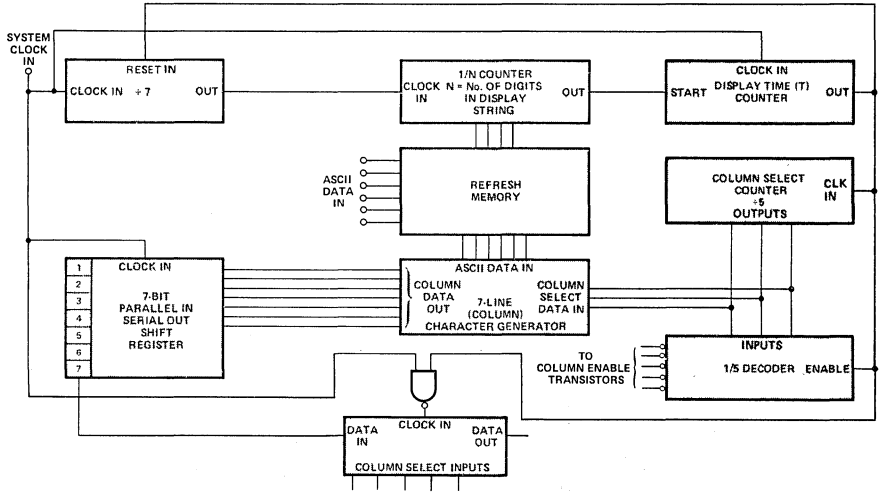


Figure 6. Block Diagram of a Basic Display System.

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COMPONENTS

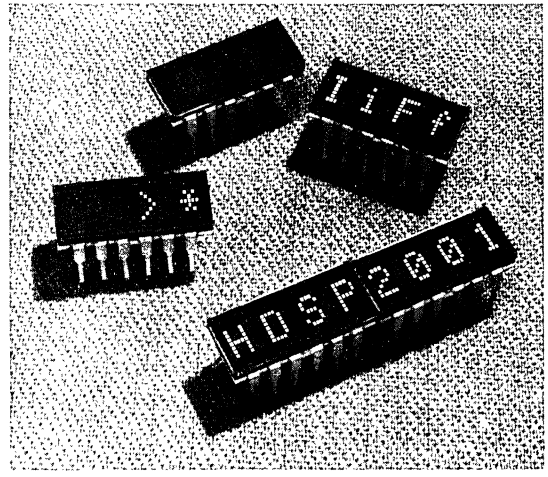
YELLOW FOUR CHARACTER SOLID STATE ALPHANUMERIC DISPLAY

HDSP-2001

TECHNICAL DATA APRIL 1979

Features

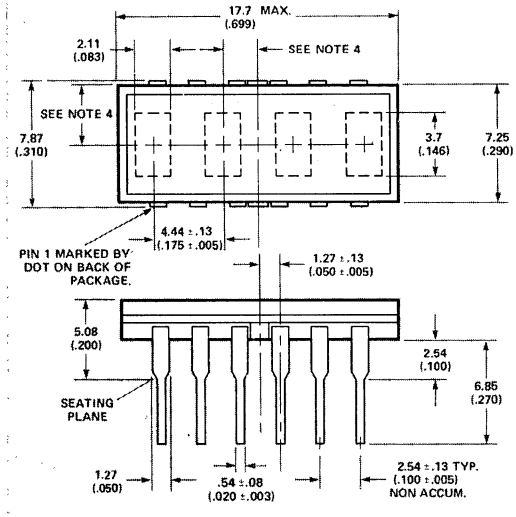
- **INTEGRATED SHIFT REGISTERS WITH CONSTANT CURRENT DRIVERS**
- **CERAMIC 7.62 mm (.3 in.) DIP**
- **WIDE VIEWING ANGLE**
- **END STACKABLE 4 CHARACTER PACKAGE**
- **PIN ECONOMY**
  12 Pins for 4 Characters
- **TTL COMPATIBLE**
- **5x7 LED MATRIX DISPLAYS FULL ASCII CODE**
- **RUGGED, LONG OPERATING LIFE**
- **CATEGORIZED FOR LUMINOUS INTENSITY AND COLOR**
  Assures Ease of Package to Package Brightness and Color Matching

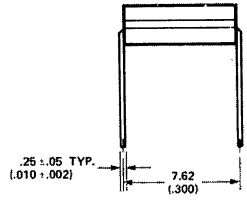


Description

The HP HDSP-2001 display is a 3.8mm (0.15 inch) 5x7 yellow LED array for display of alphanumeric information. The device is available in 4 character clusters and is packaged in a 12-pin dual-in-line type package. An on-board SIPO (serial-in-parallel-out) 7-bit shift register associated with each digit controls constant current LED row drivers. Full character display is achieved by external column strobing. The constant current LED drivers are externally programmable and typically capable of sinking 13.5mA peak per diode. Applications include interactive I/O terminals, avionics, portable telecommunications gear, and hand held equipment requiring alphanumeric displays.

Package Dimensions





PIN	FUNCTION	PIN	FUNCTION
1	COLUMN 1	7	DATA OUT
2	COLUMN 2	8	V_B
3	COLUMN 3	9	V_{CC}
4	COLUMN 4	10	CLOCK
5	COLUMN 5	11	GROUND
6	INT. CONNECT*	12	DATA IN

*DO NOT CONNECT OR USE

NOTES:
1. DIMENSIONS IN mm (inches).
2. UNLESS OTHERWISE SPECIFIED THE TOLERANCE ON ALL DIMENSIONS IS ±.38 mm (±.015").
3. LEAD MATERIAL IS GOLD PLATED COPPER ALLOY.
4. CHARACTERS ARE CENTERED WITH RESPECT TO LEADS WITHIN ±.13mm (±.005").

Absolute Maximum Ratings

Supply Voltage V_{CC} to Ground ..... −0.5V to 6.0V
Inputs, Data Out and V_B ..... −0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... −0.5V to +6.0V
Free Air Operating Temperature
Range, T_A[2] ..... −20°C to +70°C

Storage Temperature Range, T_S ..... -55°C to +100°C
Maximum Allowable Package Dissipation
at T_A = 25°C[1,2,6] ..... 1.70 Watts
Maximum Solder Temperature 1.59mm (.063")
Below Seating Plane t<5 secs ..... 260°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Nom.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Data Out Current, Low State	I_{OL}			1.6	mA
Data Out Current, HighState	I_{OH}			−0.5	mA
Column Input Voltage, Column On	V_{COL}	2.75		V_{CC}	V
Setup Time	t_{setup}	70	45		ns
Hold Time	t_{hold}	30	0		ns
Width of Clock	$t_{w(Clock)}$	75			ns
Clock Frequency	f_{clock}	0		3	MHz
Clock Transition Time	t_{THL}			200	ns
Free Air Operating Temperature Range	T_A	−20		70	°C

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified.)

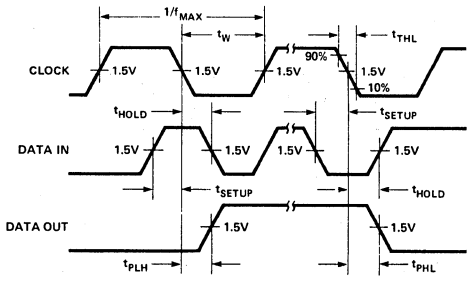
Description		Symbol	Test Conditions		Min.	Typ.*	Max.	Units
Supply Current		I_{CC}	V_{CC} = 5.25V, V_{CLOCK} = V_{DATA} = 2.4V, All SR Stages = Logical 1	V_B = 0.4V		45	60	mA
				V_B = 2.4V		73	95	mA
Column Current at any Column Input		I_{COL}	V_{CC} = V_{COL} = 5.25V, All SR Stages = Logical 1	V_B=0.4V			1.5	mA
Column Current at any Column Input		I_{COI}		V_B=2.4V		335	410	mA
Peak Luminous Intensity per LED[3,7] (Character Average)		I_{vPEAK}	V_{CC} = 5.0V, V_{COL} = 3.5V, T_i = 25°C[4] V_B=2.4V		500	750		µcd
V_B, Clock or Data Input Threshold High		V_{IH}	V_{CC} = V_{COL} = 4.75V		2.0			V
V_B, Clock or Data Input Threshold Low		V_{IL}					0.8	V
Input Current Logical 1	V_B, Clock	I_{IH}	V_{CC} = 5.25V, V_{IH} = 2.4V			20	80	µA
	Data In	I_{IH}				10	40	µA
Input Current Logical 0	V_B,Clock	I_{IL}	V_{CC} = 5.25V, V_{IL} = 0.4V			-500	-800	µA
	Data In	I_{IL}				-250	-400	µA
Data Out Voltage		V_{OH}	V_{CC} = 4.75V, I_{OH} = −0.5mA, V_{COL} = 0V		2.4	3.4		V
		V_{OL}	V_{CC} = 4.75V, I_{OL} = 1.6mA, V_{COL} = 0V			0.2	0.4	V
Power Dissipation Per Package**		P_D	V_{CC} = 5.0V, V_{COL} = 2.75V, 15 LEDs on per character, V_B = 2.4V			0.68		W
Peak Wavelength		λ_{PEAK}				583		nm
Dominant Wavelength[5]		λ_d				585		nm

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

**Power dissipation per package with 4 characters illuminated.

NOTES:
1. Maximum absolute dissipation is with the device in a socket having a thermal resistance from pins to ambient of 35°C/watt/device.
2. The device should be derated linearly above 25°C at 16mW/°C (see Electrical Description on page 3).
3. The characters are categorized for Luminous Intensity and color with the category designated by a letter code on the bottom of the package.
4. T_i refers to the initial case temperature of the device immediately prior to the light measurement.
5. Dominant wavelength λ_d, is derived from the CIE chromaticity diagram, and represents the single wavelength which defines the color of the device.
6. Maximum allowable dissipation is derived from V_{CC} = V_B = V_{COL} = 5.25 Volts, 20 LEDs on per character.
7. The luminous stearance of the LED may be calculated using the following relationships:

L_v (Lux) = I_v (Candela)/A (Metre)^2
L_v (Footlamberts) = πI_v (Candela)/A (Foot)^2
A = 8.02 x 10^{-8} M^2 = 8.64 x 10^{-7} (Foot)^2



Parameter	Condition	Min.	Typ.	Max.	Units
f_{max} Max. CLOCK Rate		3			MHz
t_{PLH}, t_{PHL} Propagation delay CLOCK to DATA OUT	C_L = 15pF R_L=2.4KΩ			125	ns

Figure 1. Switching Characteristics. (V_{CC} = 5V, T_A = -20°C to +70°C)

Mechanical and Thermal Considerations

The HDSP-2001 is available in a standard 12 lead ceramic-glass dual in-line package. It is designed for plugging into DIP sockets or soldering into PC boards. The packages may be horizontally or vertically stacked for character arrays of any desired size.

The HDSP-2001 can be operated over a wide range of temperature and supply voltages. Full power operation at T_A = 25°C (V_{CC} = V_B = V_{COL} = 5.25V) is possible by providing a total thermal resistance from the seating plane of the pins to ambient of 35°C/W/device maximum. For operation above T_A = 25°C, the maximum device dissipation should be derated above 25°C at 16mW/°C (see Figure 2). Power derating can be achieved by either decreasing V_{COL} or decreasing the average drive current through pulse width modulation of V_B.

The HDSP-2001 display has an integral untinted glass lens. A front panel contrast filter is desirable in most actual display applications. Some suggested filters are Panelgraphic Gray 10, SGL Homalite H100-1266 Gray and 3M Light Control Film (louvered filters).

Post solder cleaning may be accomplished using water, Freon/alcohol mixtures formulated for vapor cleaning processing (up to 2 minutes in vapors at boiling) or Freon/alcohol mixtures formulated for room temperature cleaning. Suggested solvents: Freon TF, Freon TE, Genesolv DI-15, Genesolv DE-15.

Electrical Description

The HDSP-2001 four character alphanumeric display has been designed to allow the user maximum flexibility in interface electronics design. Each four character display module features Data In and Data Out terminals arrayed for easy PC board interconnection such that display strings of up to 80 digits may be driven from a single character generator. Data Out represents the output of the 7th bit of digit number 4 shift register. Shift register clocking occurs on the high to low transition of the Clock input. The like columns of each character in a display cluster are tied to a single pin. Figure 5 is the block diagram for the HDSP-2001. High true data in the shift register enables the output current mirror driver stage associated with each row of LEDs in the 5x7 diode array.

The reference current for the current mirror is generated from the output voltage of the V_B input buffer applied across the resistor R. The TTL compatible V_B input may either be tied to V_{CC} for maximum display intensity or pulse width modulated to achieve intensity control and reduction in power consumption.

The normal mode of operation is depicted in the block diagram of Figure 6. In this circuit, binary input data for digit 4, column 1 is decoded by the 7 line output ROM and then loaded into the 7 on board shift register locations 1 through 7 through a parallel-in-serial-out shift register. Column 1 data for digits 3, 2 and 1 is similarly decoded and shifted into the display shift register locations. The column 1 input is now enabled for an appropriate period of time, T. A similar process is repeated for columns 2, 3, 4 and 5. If the time necessary to decode and load data into the shift register is t, then with 5 columns, each column of the display is operating at a duty factor of:

$$D.F. = \frac{T}{5(t+T)}$$

The time frame, t + T, allotted to each column of the display is generally chosen to provide the maximum duty factor consistent with the minimum refresh rate necessary

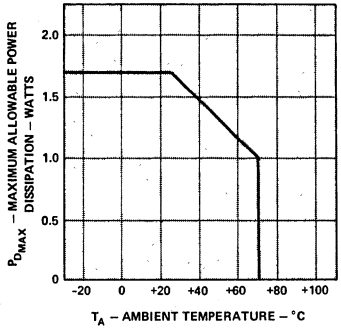


Figure 2. Maximum Allowable Power Dissipation vs. Temperature.

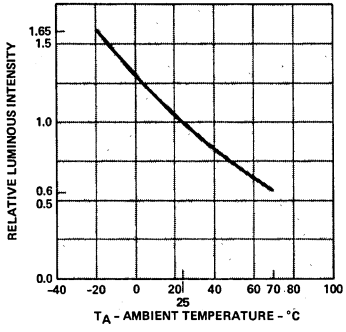


Figure 3. Relative Luminous Intensity vs. Temperature.

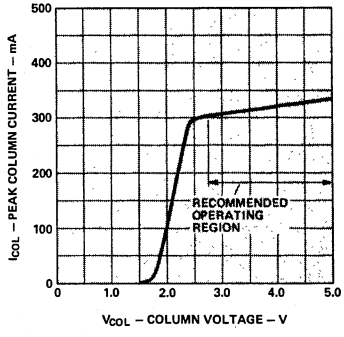


Figure 4. Peak Column Current vs. Column Voltage.

to achieve a flicker free display. For most strobed display systems, each column of the display should be refreshed (turned on) at a minimum rate of 100 times per second.

With 5 columns to be addressed, this refresh rate then gives a value for the time t + T of:

$1/[5 \times (100)] = 2$ msec.

If the device is operated at 3.0 MHz clock rate maximum, it is possible to maintain $t \ll T$. For short display strings, the duty factor will then approach 20%. For longer display strings operation at column duty factors of less than 10% will still provide adequate display intensity in most applications. For further applications information, refer to HP Application Note 1001.

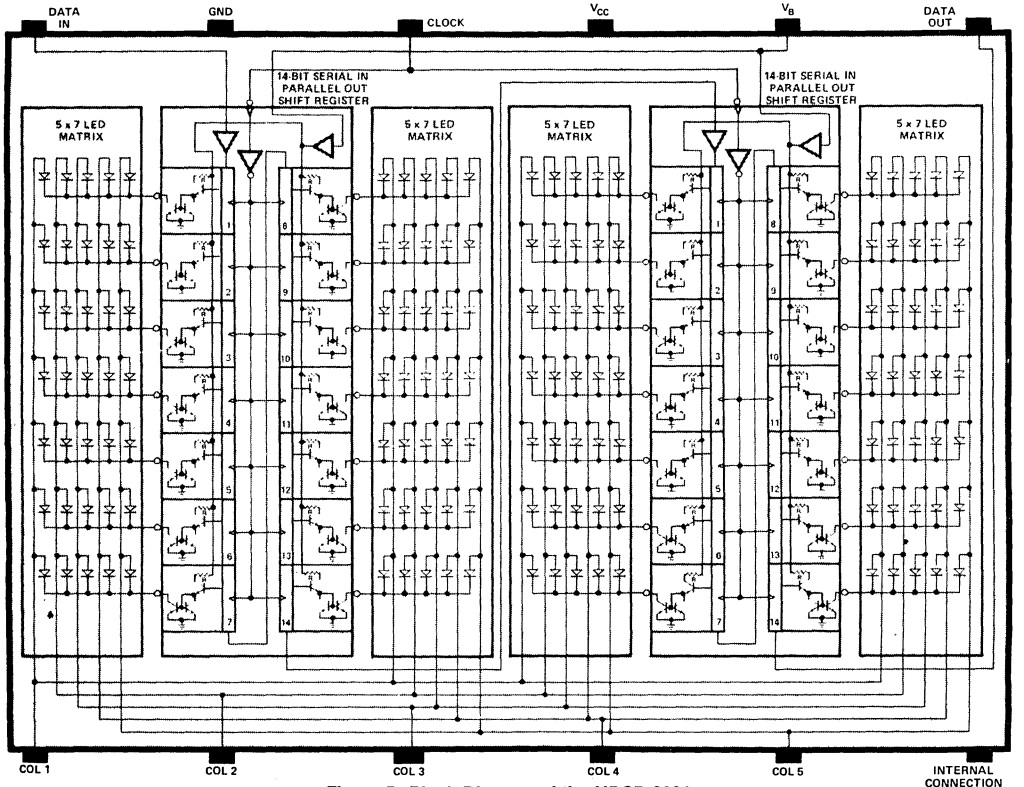


Figure 5. Block Diagram of the HDSP-2001.

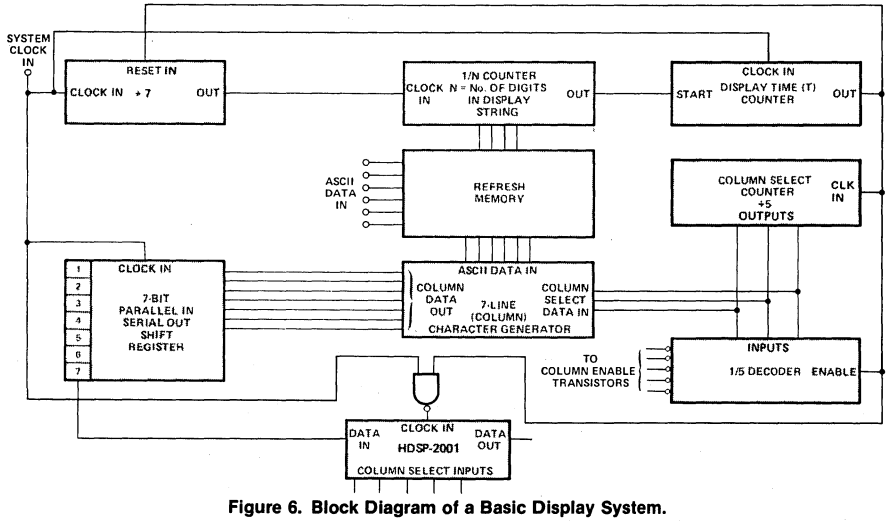


Figure 6. Block Diagram of a Basic Display System.

HEWLETT hp PACKARD

COMPONENTS

NEW PRODUCT

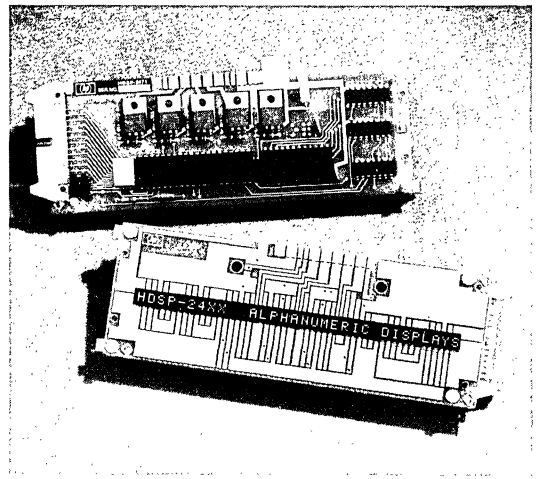
5 x 7 DOT MATRIX ALPHANUMERIC DISPLAY SYSTEM

HDSP-2416
HDSP-2424
HDSP-2432
HDSP-2440
HDSP-2470
HDSP-2471
HDSP-2472

TECHNICAL DATA APRIL 1979

Features

- **COMPLETE ALPHANUMERIC DISPLAY SYSTEM UTILIZING THE HDSP-2000 DISPLAY**
- **CHOICE OF 64, 128, OR USER DEFINED ASCII CHARACTER SET**
- **CHOICE OF 16, 24, 32, or 40 ELEMENT DISPLAY PANEL**
- **MULTIPLE DATA ENTRY FORMATS — Left, Right, RAM, or Block Entry**
- **EDITING FEATURES THAT INCLUDE CURSOR, BACKSPACE, FORWARDSPACE, INSERT, DELETE, AND CLEAR**
- **DATA OUTPUT CAPABILITY**
- **SINGLE 5.0 VOLT POWER SUPPLY**
- **TTL COMPATIBLE**
- **EASILY INTERFACED TO A KEYBOARD OR A MICROPROCESSOR**



Description

The HDSP-24XX series of alphanumeric display systems provides the user with a completely supported 5 x 7 dot matrix display panel. These products free the user's system from display maintenance and minimize the interaction normally required for alphanumeric displays. Each alphanumeric display system is composed of two component parts:

1. An alphanumeric display controller which consists of a preprogrammed microprocessor plus associated logic, which provides decode, memory, and drive signals necessary to properly interface a user's system to an HDSP-2000 display. In addition to these basic display support operations, the controller accepts data in any of four data entry formats and incorporates several powerful editing routines.
2. A display panel which consists of HDSP-2000 displays matched for luminous intensity and mounted on a P.C. board designed to have low thermal resistance.

These alphanumeric display systems are attractive for applications such as data entry terminals, instrumentation, electronic typewriters, and other products which require an easy to use 5 x 7 dot matrix alphanumeric display system.

PART NUMBER	DESCRIPTION
Display Boards	
HDSP-2416	Single-line 16 character display panel utilizing the HDSP-2000 display
HDSP-2424	Single-line 24 character display panel utilizing the HDSP-2000 display
HDSP-2432	Single-line 32 character display panel utilizing the HDSP-2000 display
HDSP-2440	Single-line 40 character display panel utilizing the HDSP-2000 display
Controller Boards	
HDSP-2470	HDSP-2000 display interface incorporating a 64 character ASCII decoder
HDSP-2471	HDSP-2000 display interface incorporating a 128 character ASCII decoder
HDSP-2472	HDSP-2000 display interface without ASCII decoder. Instead, a 24 pin socket is provided to accept a custom 128 character set from a user programmed 1K x 8 PROM.

When ordering, specify one each of the Controller Board and the Display Board for each complete system.

Absolute Maximum Ratings

V_{CC} ..... -0.5V to 6.0V

Operating Temperature Range, Ambient (T_A) ..... 0°C to 70°C

Storage Temperature Range (T_S) .... -55°C to 100°C

Voltage Applied to any Input or Output ..-0.5V to 6.0V

I_{SOURCE} Continuous for any Column Driver ..... 5.0 Amps (60 sec. max. duration)

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.25	V
Data Out	I_{OL}		0.4	mA
	I_{OH}		-20	μA
Ready, Data Valid, Column On, Display Data	I_{OL}		1.6	mA
	I_{OH}		-40	μA
Clock	I_{OL}		10.0	mA
	I_{OH}		-1.0	mA
$Column_{1-5}$	I_{SOURCE}		-5.0	A

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current[1]	I_{CC}			400	mA	V_{CC} = 5.25V Column On and All Outputs Open
Input Threshold High (except Reset)	V_{IH}	2.0			V	V_{CC} = 5.0V ± .25V
Input Threshold High — Reset[2]	V_{IH}	3.0			V	V_{CC} = 5.0V ± .25V
Input Threshold Low — All Inputs	V_{IL}			0.8	V	V_{CC} = 5.0V ± .25V
Data Out Voltage	V_{OH}Data	2.4			V	I_{OH} = -20μA V_{CC} = 4.75V
	V_{OL}Data			0.5	V	I_{OL} = 0.4mA V_{CC} = 4.75V
Clock Output Voltage	V_{OH}Clk	2.4			V	I_{OH} = -1000μA V_{CC} = 4.75V
	V_{OL}Clk			0.5	V	I_{OL} = 10.0mA V_{CC} = 4.75V
Ready, Display Data, Data Valid, Column on Output Voltage	V_{OH}	2.4			V	I_{OH} = -40μA V_{CC} = 4.75V
	V_{OL}			0.5	V	I_{OL} = 1.6mA V_{CC} = 4.75V
Input Current,[3] All Inputs Except Reset, Chip Select, D_7	I_{IH}			-0.3	mA	V_{IH} = 2.4V V_{CC} = 5.25V
	I_{IL}			-0.6	mA	V_{IL} = 0.5V V_{CC} = 5.25V
$\overline{\text{Reset}}$ Input Current	I_{IH}			-0.3	mA	V_{IH} = 3.0V V_{CC} = 5.25V
	I_{IL}			-0.6	mA	V_{IL} = 0.5V V_{CC} = 5.25V
Chip Select, D_7 Input Current	I_I	-10		+10	μA	$0 < V_I < V_{CC}$
Column Output Voltage	V_{OL}COL	2.6	3.2		V	I_{OUT} = -5.0A V_{CC} = 5.00V

NOTES:

1. See Figure 11 for total system supply current.
2. External reset may be initiated by grounding Reset with either a switch or open collector TTL gate for a minimum time of 50ms. For Power On Reset to function properly, V_{CC} power supply should turn on at a rate > 100V/s.
3. Momentary peak surge currents may exist on these lines. However, these momentary currents will not interfere with proper operation of the HDSP-2470/1/2.

HDSP-2416/-2424/-2432/-2440

Absolute Maximum Ratings

Supply Voltage V_{CC} to Ground ..... -0.5V to 6.0V
Inputs, Data Out and V_B ..... -0.5V to V_{CC}
Column Input Voltage, V_{COL} ..... -0.5V to +6.0V
Free Air Operating Temperature Range, T_A[1] ..... 0°C to +55°C
Storage Temperature Range, T_S .... -55°C to +100°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Norm.	Max.	Units
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Column Input Voltage, Column On	V_{COL}	2.6			V
Setup Time	t_{SETUP}	70	45		ns
Hold Time	t_{HOLD}	30	0		ns
Width of Clock	$t_{W(CLOCK)}$	75			ns
Clock Frequency	f_{CLOCK}	0		3	MHz
Clock Transition Time	t_{THL}			200	ns
Free Air Operating[1] Temperature Range	T_A	0		55	°C

Electrical Characteristics Over Operating Temperature Range

(Unless otherwise specified)

Parameter		Symbol	Min.	Typ.*	Max.	Units	Conditions	
Supply Current		I_{CC}		45n	60n[2]	mA	V_{CC} = 5.25V, V_{CLOCK}=V_{DATA}=2.4V, All SR Stages = Logical 1	V_B = 0.4V
				73n	95n	mA		V_B = 2.4V
Column Current at any Column Input		I_{COL}			1.5n	mA	V_{CC} = V_{COL} = 5.25V, All SR Stages = Logical 1	V_B = 0.4V
		I_{COL}		335n	410n	mA		V_B = 2.4V
Peak Luminous Intensity per LED (Character Average)		$I_{V\ PEAK}$	105	200		µcd	V_{CC} = 5.0V, V_{COL} = 3.5V, T_j = 25°C[3], V_B = 2.4V	
V_B, Clock or Data Input Threshold High		V_{IH}	2.0			V	V_{CC} = V_{COL} = 4.75V	
V_B, Clock or Data Input Threshold Low		V_{IL}			0.8	V		
Input Current Logical 1	V_B, Clock	I_{IH}			80	µA	V_{CC} = 5.25V, V_{IH} = 2.4V	
	Data In	I_{IH}			40	µA		
Input Current Logical 0	V_B, Clock	I_{IL}		-500	-800	µA	V_{CC} = 5.25V, V_{IL} = 0.4V	
	Data In	I_{IL}		-250	-400	µA		
Power Dissipation Per Board[4]		P_D		0.66n		W	V_{CC} = 5.0V, V_{COL} = 2.6V, 15 LED's on per Character, V_B = 2.4V	

*All typical values specified at V_{CC} = 5.0V and T_A = 25°C unless otherwise noted.

NOTES:

1. Operation above 55°C (70°C MAX) may be achieved by the use of forced air (150 fpm normal to component side of HDSP-247X controller board at sea level). Operation down to -20°C is possible in applications that do not require the use of HDSP-2470/-2471/-2472 controller boards.
2. n = number of HDSP-2000 packages
   HDSP-2416 n = 4
   HDSP-2424 n = 6
   HDSP-2432 n = 8
   HDSP-2440 n = 10
3. Tj refers to initial case temperature immediately prior to the light measurement.
4. Power dissipation with all characters illuminated.

System Overview

The HDSP-2470/-2471/-2472 Alphanumeric Display Controllers provide the interface between any ASCII based Alphanumeric System and the HDSP-2000 Alphanumeric Display. ASCII data is loaded into the system by means of any one of four data entry modes — Left, Right, RAM or Block Entry. This ASCII data is stored in the internal RAM memory of the system. The system refreshes HDSP-2000 displays from 4 to 48 characters with the decoded data.

The user interfaces to any of the systems through eight DATA IN inputs, five ADDRESS inputs (RAM mode), a CHIP SELECT input, RESET input, seven DATA OUT outputs, a READY output, DATA VALID output, and a COLUMN ON output. A low level on the RESET input clears the display and initializes the system. A low level on the CHIP SELECT input causes the system to load data from the DATA IN and ADDRESS inputs into the system. The controller outputs a status word, cursor address and 32 ASCII data characters through the DATA OUT outputs and DATA VALID output during the time the system is waiting to refresh the next column of the display. The COLUMN ON output can be used to synchronize the DATA OUT function. A block diagram for the HDSP-2470/-2471/-2472 systems is shown in Figure 1.

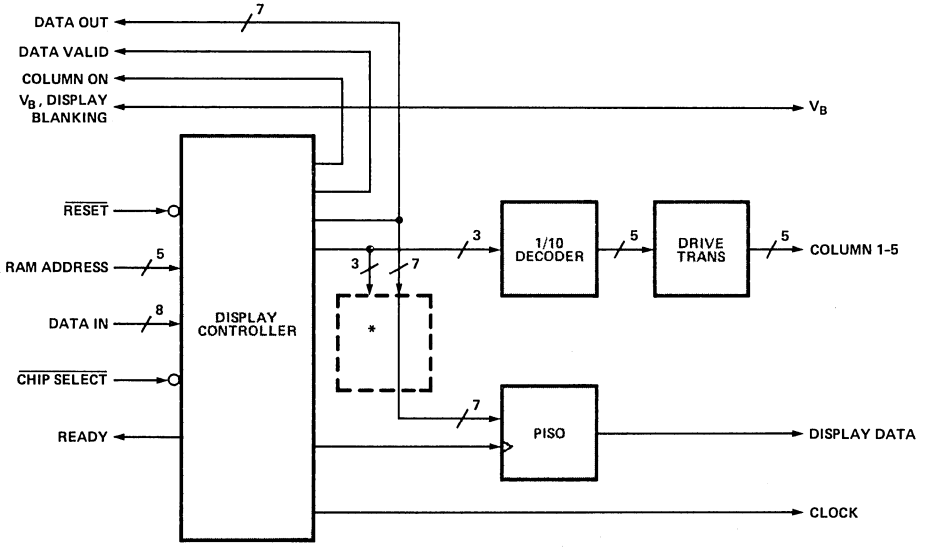


Figure 1. Block Diagram for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

The system interfaces to the HDSP-2000 display through five COLUMN outputs, a CLOCK output, DISPLAY DATA output, and the COLUMN ON output. The user should connect DISPLAY DATA to DATA IN of the leftmost HDSP-2000 cluster and cascade DATA OUT to DATA IN of all HDSP-2000 clusters. COLUMN outputs from the system are connected to the COLUMN inputs of all HDSP-2000 clusters. The HDSP-24XX Series display boards are designed to interconnect directly with the HDSP-247X Series display controllers. The COLUMN outputs can source enough current to drive up to 48 characters of the HDSP-2000 display. Pulse width modulation of display luminous intensity can be provided by connecting COLUMN ON to the input of a monostable multivibrator and the output of the monostable multivibrator to the V_B inputs of the HDSP-2000 displays. The system is designed to refresh the display at a fixed refresh rate of 100 Hz. COLUMN ON time is optimized for each display length in order to maximize light output as shown in Figure 2.

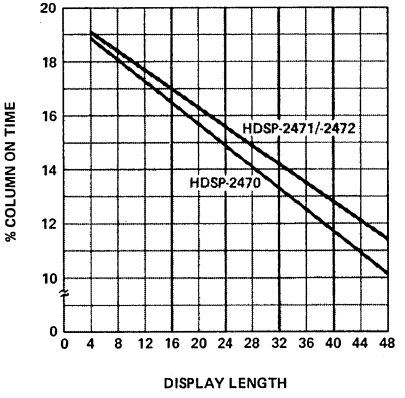


Figure 2. Column on Time vs. Display Length for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Control Mode/Data Entry

User interface to the HDSP-247X Series controller is via an 8 bit word which provides to the controller either a control word or standard ASCII data input. In addition to this user provided 8 bit word, two additional control lines, CHIP SELECT and READY, allow easily generated "handshake" signals for interface purposes.

A logic low applied to the CHIP SELECT input (minimum six microseconds) causes the controller to read the 8 DATA IN lines and determine whether a control word or ASCII data word is present, as determined by the logic state of the most significant bit (D_7). If the controller detects a logic high at D_7, the state of D_6-D_0 will define the data entry mode and the number of alphanumeric characters to be displayed.

The 8 bit control data word format is outlined in Figure 3. For the control word (D_7 high), bits D_6 and D_5 define the selected data entry mode (Left entry, Right entry, etc.) and bits D_3 to D_0 define display length. Bit D_4 is ignored.

Control word inputs are first checked to verify that the control word is valid. The system ignores display lengths greater than 1011 for left block or right, or 0111 for RAM. If the word is valid, the present state—next state table shown in Figure 4 is utilized to determine whether or not to clear the display. For display lengths of up to 32 characters, RAM entry can be used as a powerful editing tool, or can be used to preload the cursor. With other transitions, the internal data memory is cleared.

CONTROL WORD: $D_7D_6D_5D_4D_3D_2D_1D_0$

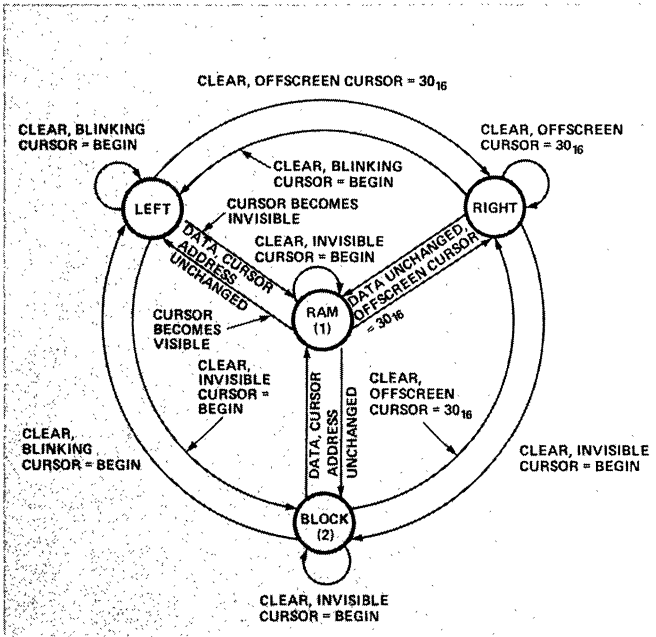
1	X	X	–	Y	Y	Y	Y

Y Y Y Y	DISPLAY LENGTH:
0 0 0 0	4 DIGITS
0 0 0 1	8 "
0 0 1 0	12 "
0 0 1 1	16 "
0 1 0 0	20 "
0 1 0 1	24 "
0 1 1 0	28 "
0 1 1 1	32* "
1 0 0 0	36 "
1 0 0 1	40 "
1 0 1 0	44 "
1 0 1 1	48 "

*maximum for RAM data entry mode

X X	DATA ENTRY MODES
0 0	RAM DATA ENTRY
0 1	LEFT DATA ENTRY
1 0	RIGHT DATA ENTRY
1 1	BLOCK DATA ENTRY

Figure 3. Control Word Format for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.



(1) RAM ENTRY MODE IS VALID FOR DISPLAYS OF 32 CHARACTERS OR LESS IN LENGTH.
(2) FOLLOWING A TRANSITION FROM RAM TO BLOCK, WHEN THE CURSOR ADDRESS IS 48 (30_{16}) DURING THE TRANSITION, THE FIRST VALID ASCII CHARACTER WILL BE IGNORED AND THE SECOND VALID ASCII CHARACTER WILL BE LOADED IN THE LEFT-MOST DISPLAY LOCATION.

WHERE BEGIN IS DEFINED AS FOLLOWS:

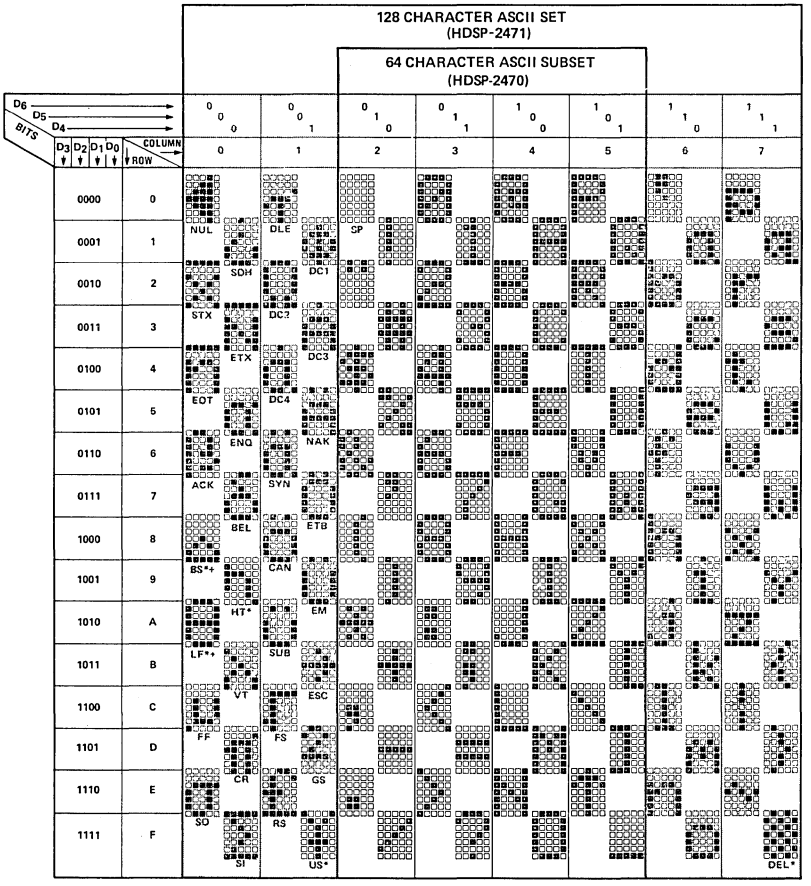
DISPLAY LENGTH	CURSOR ADDRESS OF BEGIN
4	$2C_{16}$, 44_{10}
8	28_{16}, 40_{10}
12	24_{16}, 36_{10}
16	20_{16}, 32_{10}
20	$1C_{16}$, 28_{10}
24	18_{16}, 24_{10}
28	14_{16}, 20_{10}
32	10_{16}, 16_{10}
36	$0C_{16}$, 12_{10}
40	08_{16}, 8_{10}
44	04_{16}, 4_{10}
48	00_{16}

Figure 4. Present State-Next State Diagram for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

If D_7 is a logic low when the DATA IN lines are read, the controller will interpret D_6-D_0 as standard ASCII data to be stored, decoded and displayed. The system accepts seven bit ASCII for all three versions. However, the HDSP-2470 system displays only the 64 character subset [20_{16} (space) to $5F_{16}$ (_)] and ignores all ASCII characters outside this subset with the exception of those characters defined as display commands. These display commands are shown in Figure 5. Displayed character sets for the HDSP-2470/-2471 systems are shown in Figure 6.

DATA WORD:	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
ASCII ASSIGNMENT	0	A	A	A	A	A	A	A	DISPLAY COMMAND	
LF	0	0	0	1	0	1	0		CLEAR	Valid in Right Entry Mode
BS	0	0	0	1	0	0	0		BACKSPACE CURSOR	Valid in Right Entry Mode
HT	0	0	0	1	0	0	1		FORWARDSPACE CURSOR	Valid in Left Entry Mode
US	0	0	1	1	1	1	1		INSERT CHARACTER	Valid in Left Entry Mode
DEL	1	1	1	1	1	1	1		DELETE CHARACTER	Valid in Left Entry Mode

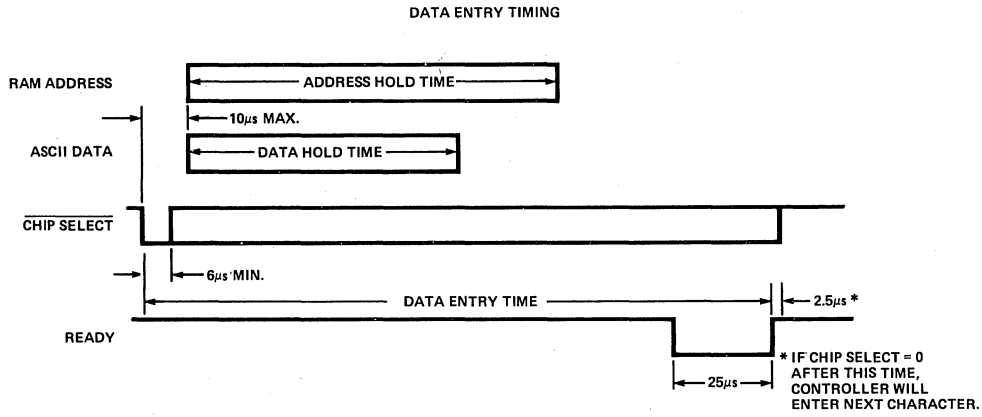
Figure 5. Display Commands for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.



*DISPLAY COMMANDS WHEN USED IN LEFT ENTRY
+DISPLAY COMMANDS WHEN USED IN RIGHT ENTRY

Figure 6. Display Font for the HDSP-2470 (64 Character ASCII Subset), and HDSP-2471 (128 Character ASCII Set) Alphanumeric Display Controller.

Regardless of whether a control word or ASCII data word is presented by the user, a READY signal is generated by the controller after the input word is processed. This READY signal goes low for 25μs and upon a positive transition, a new CHIP SELECT may be accepted by the controller. Data Entry Timing is shown in Figure 7.



MAXIMUM DATA ENTRY TIMES OVER OPERATING TEMPERATURE RANGE

DATA ENTRY MODE			FUNCTION					
HDSP-	DATA HOLD TIME*		DATA ENTRY	BACK SPACE	CLEAR	FORWARD SPACE	DELETE	INSERT
LEFT (2471/2)	135μs		235μs	195μs	505μs	205μs	725μs	725μs
LEFT (2470)	150μs		245μs	215μs	530μs	225μs	745μs	735μs
RIGHT (2471/2)	85μs		480μs	470μs	465μs			
RIGHT (2470)	105μs		490μs	490μs	485μs			
RAM (2471/2)	55μs	120μs**	190μs					
RAM (2470)	55μs	130μs**	200μs					
BLOCK (2471/2)	55μs		120μs	(155μs FOR RIGHTMOST CHARACTER)				
BLOCK (2470)	55μs		130μs	(165μs FOR RIGHTMOST CHARACTER)				
LOAD CONTROL (2471/2)	50μs		505μs					
LOAD CONTROL (2470)	50μs		505μs					

*Minimum time that data inputs must remain valid after Chip Select goes low.
**Minimum time that RAM address inputs must remain valid after Chip Select goes low.

Figure 7. Data Entry Timing and Data Entry Times for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Left Entry Mode

With Left entry, characters are entered in typewriter fashion, i.e., to the right of all previous characters. Left entry uses a blinking cursor to indicate the location where the next character is to be entered. CLEAR loads the display with spaces and resets the cursor to the leftmost display location. BACKSPACE and FORWARDSPACE move the cursor without changing the character string. Thus, the user can backspace to the character to be edited, enter a character and then forward space the cursor. The DELETE function deletes the displayed character at the cursor location and then shifts the character string following the cursor one location to the left to fill the void of the deleted character. The INSERT CHARACTER sets a flag inside the system that causes subsequent ASCII characters to be inserted to the left of the character at the cursor location. As new characters are entered, the cursor, the character at the cursor, and all characters to the right of the cursor are shifted one location to the right. The INSERT function is terminated by a second INSERT CHARACTER, or by BACKSPACE, FORWARDSPACE, CLEAR or DELETE. In Left entry mode, after the display is filled, the system ignores all characters except BACKSPACE and CLEAR. The system allows the cursor to be positioned only in the region between the leftmost display character and immediately to the right (offscreen) of the rightmost display character.

Right Entry Mode

In Right entry mode, characters are entered at the right hand side of the display and shifted to the left as new characters are entered. In this mode, the system stores 48 ASCII characters, although only the last characters entered are displayed. CLEAR loads the display with spaces. BACKSPACE shifts the display one location to the right, deleting the last character entered and displaying the next character in the 48 character buffer. Right entry mode is a simple means to implement the walking or "Times-Square" display. FORWARDSPACE, INSERT, and DELETE have character assignments in this mode since they are not treated as editing characters. In this mode, the cursor is located immediately to the right (offscreen) of the rightmost displayed character.

Block Entry Mode

Block entry allows the fastest data entry rate of all four modes. In this mode, characters are loaded from left to right as with Left entry. However, with Block entry, after the display is completely loaded, the next ASCII character is loaded in the leftmost display location, replacing the previous displayed character. While Block entry has a nonvisible cursor, the cursor is always loaded with the address of the next character to be entered. In this entry mode, the system can display the complete 128 character ASCII set. The display can be cleared and the cursor reset to the leftmost display location by loading in a new BLOCK control word.

RAM Entry Mode

In RAM entry, ASCII characters are loaded at the address specified by the five bit RAM address. Due to the limitation of only five address lines, RAM data entry is allowed only for displays less than or equal to 32 characters. Regardless of display length, address 00 is the leftmost display character. Out of range RAM addresses are ignored. While RAM entry has a non-visible cursor, the cursor is always preloaded with the address to the right of the last character entered. This allows the cursor to be preloaded with an address prior to going into any other entry mode. In RAM entry, the system can display the complete 128 character ASCII set because it does not interpret any of the characters as control functions. The display can be cleared by loading in a new RAM control word.

Data Out

For display lengths of 32 characters or less, the data stored in the internal RAM is available to the user during the time between display refresh cycles. The system outputs a STATUS WORD, CURSOR ADDRESS, and 32 ASCII data characters. The STATUS WORD specifies the data entry mode and the display length of the system. The STATUS WORD output differs slightly from the CONTROL WORD input. This difference is depicted in Figure 8. Regardless of display length, the CURSOR ADDRESS of the rightmost character location is address 47 ($2F_{16}$) and the offscreen address of the cursor is address 48 (30_{16}). The CURSOR ADDRESS of the leftmost location is defined as address 48 minus the display length. A general formula for CURSOR ADDRESS is:

CURSOR ADDRESS =

(47 - Display Length) + Number of Characters from Left.

For example, suppose the alphanumeric display is 16 characters long and the cursor was blinking at the third digit from the left. Then the CURSOR ADDRESS would be 47 - 16 + 3 or 34 (22_{16}) and the 18th ASCII data word would correspond to the ASCII character at the location of the display cursor. In Left and Block entry, the CURSOR ADDRESS specifies the location where the next ASCII data character is to be entered. In RAM entry, the CURSOR ADDRESS specifies the location to the right of the last character entered. In Right entry, the CURSOR ADDRESS is always 48 (30_{16}). The negative edge of the DATA VALID output can be used to load the 34 DATA OUT words into the user's system. The DATA OUT timing for the HDSP-247X systems are summarized in Figure 8. For displays longer than 32 characters, the system only outputs the STATUS WORD between refresh cycles.

Master/Power On Reset

When power is first applied to the system, the system clears the display and tests the state of the DATA INPUT, D_7. If $D_7 > 2.0V$, the systems loads the control word on the DATA INPUTS into the system. If $D_7 \leq .8V$ or the system sees an invalid control word, the system initializes as Left entry for a 32 character display with a flashing cursor in the leftmost location. For POWER ON RESET to function properly, the power supply must turn on at a rate > 100 V/s. In addition, the system can be reset by pulling the RESET input low for a minimum of 50 milliseconds. POWER ON/MASTER RESET timing is shown in Figure 9.

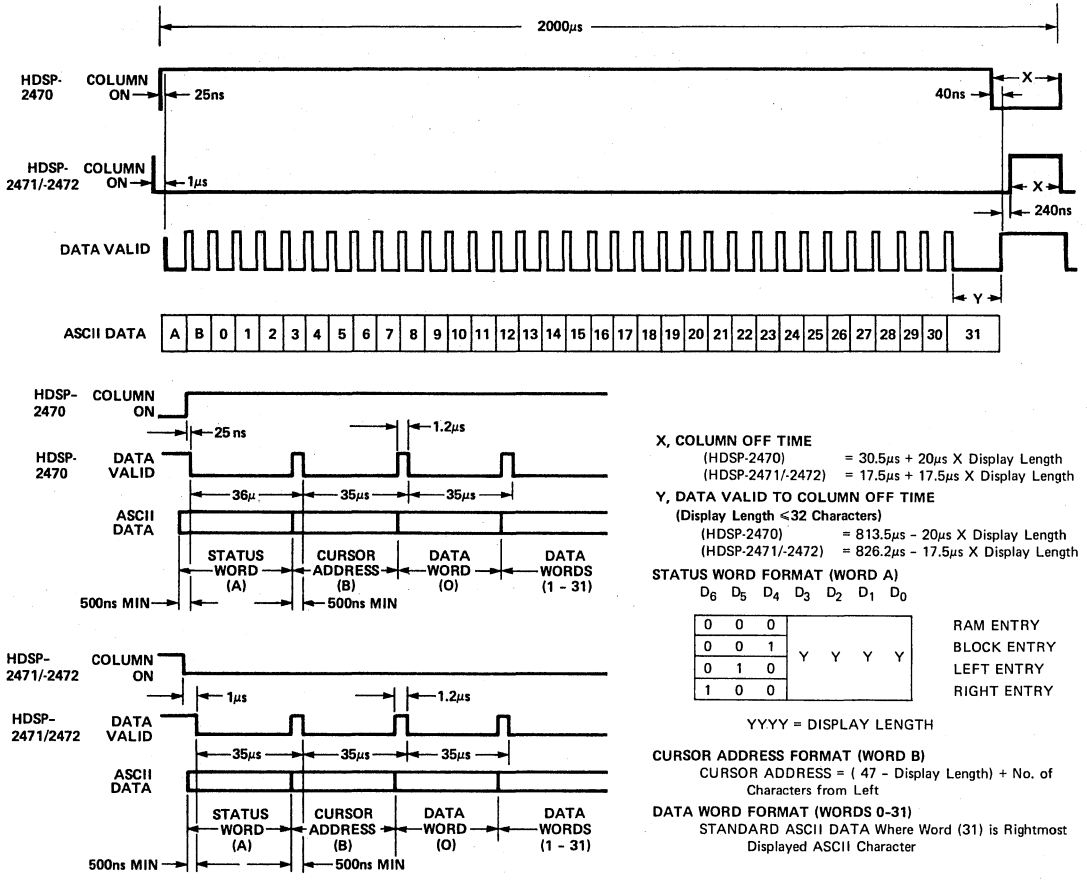


Figure 8. Data Out Timing and Format for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

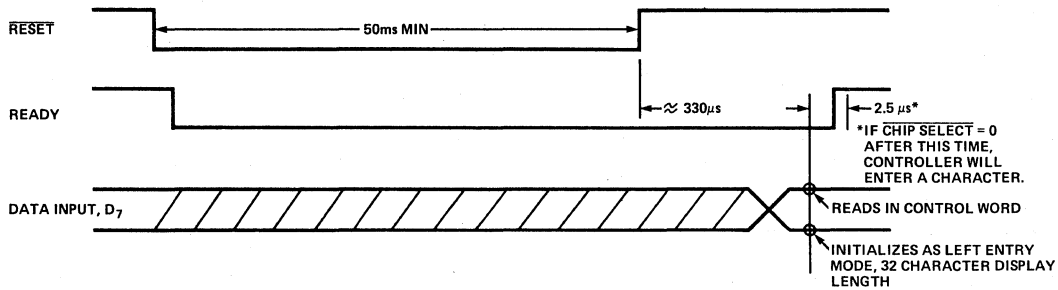


Figure 9. Power-On/Master Reset Timing for the HDSP-2470/-2471/-2472 Alphanumeric Display Controller.

Custom Character Sets

The HDSP-2472 system has been specifically designed to permit the user to insert a custom 128 ASCII character set. This system features a 24 pin socket that is designed to accept a custom programmed 1K X 8 PROM, EPROM, or ROM. The read only memory should have an access time ≤ 500ns, $I_{IL} \leq |-.4mA|$ and $I_{IH} \leq 40\mu A$. A list of pin compatible read only memories is shown in Figure 10. Jumper locations are provided on the HDSP-2472 P.C. board which allow the use of ROM's requiring chip enables tied either to 0 or 5V. For further information on ROM programming, please contact the factory.

Power Supply Requirements

The HDSP-247X Alphanumeric Display System is designed to operate from a single 5 volt supply. Total I_{CC} requirements for the HDSP-247X Alphanumeric Display Controller and HDSP-24XX Display Panel are shown in Figure 11. Peak I_{CC} is the instantaneous current required for the system. Maximum Peak I_{CC} occurs for $V_{CC} = 5.25V$ with 7 dots ON in the same Column in all display characters. This current must be supplied by a combination of the power supply and supply filter capacitor. Maximum Average I_{CC} occurs for $V_{CC} = 5.25V$ with 21 dots ON per character in all display characters. The inclusion of a 375 X microfarad capacitor (where X is the number of characters in the display) adjacent to the HDSP-247X Alphanumeric Display System will permit the use of a power supply capable of supplying the maximum average I_{CC}.

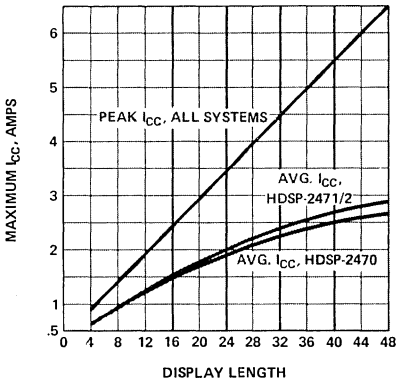


Figure 11. Maximum Peak and Average I_{CC} for the HDSP-2470/71/72 Alphanumeric Display Controller and HDSP-2000 Display.

CONNECTORS

FUNCTION	TYPE OF CONNECTOR	SUGGESTED MANUFACTURER
CONTROL/DATA ENTRY	26 Pin Ribbon Cable	3M P/N 3399-X000 Series
POWER(1)	3 Pin With Locking Ramp	Molex P/N 09-50-3031 with 08-50-0106 Terminals
DISPLAY DRIVE(2,3)	17 Lead Board to Board	Amp P/N 1-530500-7, also available in board to cable and other configurations

NOTES:
(1) Power leads should be 18-20 gauge stranded wire.
(2) The maximum lead length from the controller board to the display should not exceed 1 metre.
(3) The suggested Amp connector is supplied with the controller.

PART NUMBER	MANUFACTURER	TYPE	CONSTRUCTION	EXTERNAL CONNECTION* X	Y	Z
2758	Intel	EPROM	NMOS	GND	GND	+5
7608	Harris	PROM	BIPOLAR-NiCr	NC	NC	NC
3628-4	Intel	PROM	BIPOLAR-Si	+5	+5	GND
82S2708	Signetics	PROM	BIPOLAR-NiCr	NC	NC	NC
6381	Monolithic Mem.	PROM	BIPOLAR-NiCr	+5	+5	GND
6385	Monolithic Mem.	PROM	BIPOLAR-NiCr	NC	NC	NC
87S228	National	PROM	BIPOLAR-TiW	+5	+5	GND
93451	Fairchild	PROM	BIPOLAR-NiCr	+5	+5	GND
68308	Motorola	ROM	NMOS	**	NC	NC
2607	Signetics	ROM	NMOS	**	NC	NC
30000	Mostek	ROM	NMOS	**	+5	NC

*Board jumpers correspond to pins 18, 19 & 21 of ROM.

**As defined by customer

Figure 10. Pin Compatible 1K x 8 Read Only Memories for the HDSP-2472 Alphanumeric Display Controller.

Display Boards/Hardware

The mechanical layout of the HDSP-247X Series allows direct mating of the controller P.C. board to a compatible series of display boards available from Hewlett-Packard. These display boards consist of matched and tested HDSP-2000 clusters soldered to a P.C. board.

Included with the controller board are: 1 each Amp P/N 1-530500-7 board to board connector, and 4 each locking circuit board support nylon standoffs (Richco LCBS-4). This hardware allows the controller board to interconnect with any of the standard display boards. Figure 12 depicts correct assembly technique.

Assembly Steps

1. Insert the standoffs into .151 diameter holes (noted as "S" on Figure 12. The long end of the standoffs should protrude through the controller board side.
2. Position the controller board and display board with the components and displays facing out. The HP logo should be in the upper left corner when viewed facing the boards. Insert the standoffs through the mating holes on the display board and press the boards together so that the standoffs lock in place.
3. After the standoffs are secured, the Amp connector should be placed on the edge connect pads (marked "A" through "Q" Figure 12) at the top of the boards. Visual alignment of this connector may be done on the controller board by determining that the first connector contact finger is centered on the pad labeled "A".

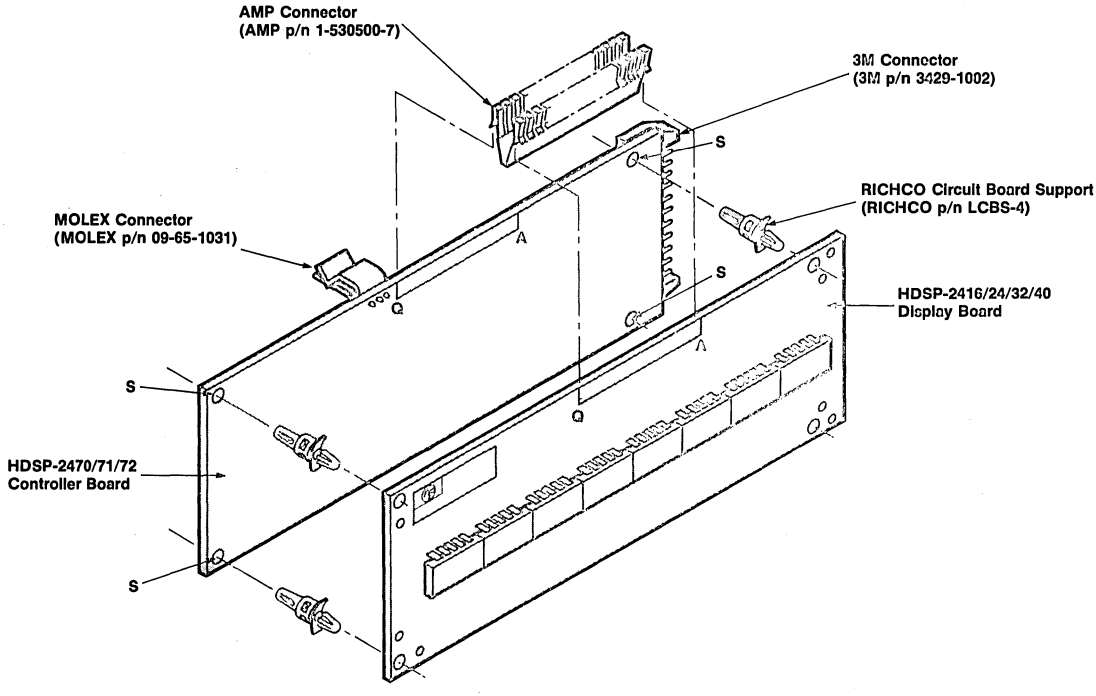
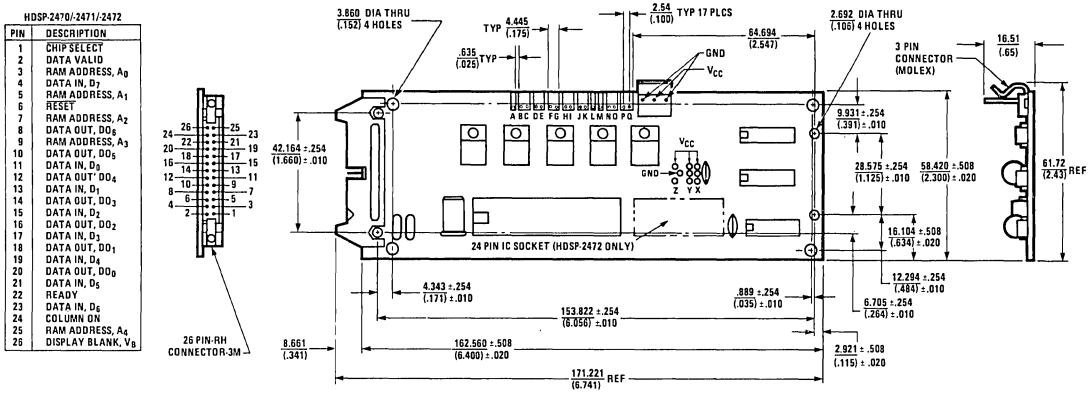


Figure 12. Assembly Drawing.

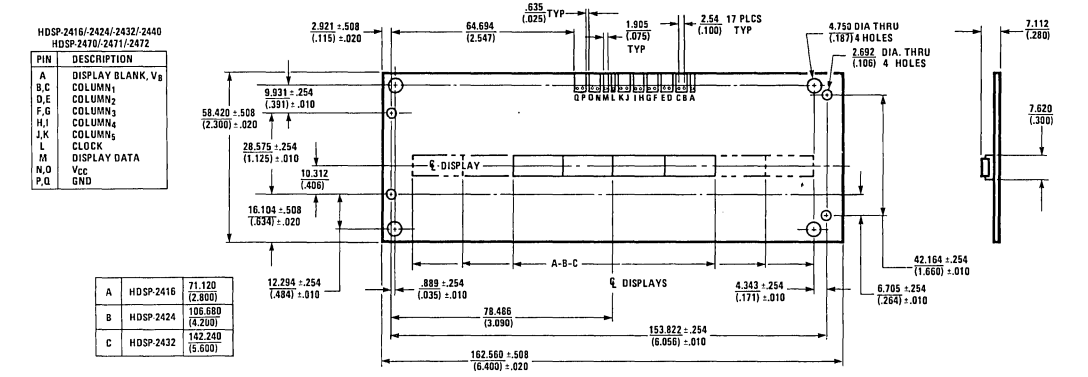
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN mm AND (INCHES)



HDSP-2470/-2471/-2472

PIN	DESCRIPTION
1	CHIP SELECT
2	DATA VALID
3	RAM ADDRESS, A_0
4	DATA IN, D_7
5	RAM ADDRESS, A_1
6	RESET
7	RAM ADDRESS, A_2
8	DATA OUT, DO_6
9	RAM ADDRESS, A_3
10	DATA OUT, DO_5
11	DATA IN, D_6
12	DATA OUT DO_4
13	DATA IN, D_5
14	DATA OUT, DO_3
15	DATA IN, D_2
16	DATA OUT, DO_2
17	DATA IN, D_3
18	DATA OUT, DO_1
19	DATA IN, D_4
20	DATA OUT, DO_0
21	DATA IN, D_5
22	READY
23	DATA IN, D_6
24	COLUMN ON
25	RAM ADDRESS, A_4
26	DISPLAY BLANK, V_B

Figure 13. HDSP-2470/-2471/-2472



HDSP-2416/-2424/-2432/-2440
HDSP-2470/-2471/-2472

PIN	DESCRIPTION
A	DISPLAY BLANK, V_B
B,C	$COLUMN_1$
D,E	$COLUMN_2$
F,G	$COLUMN_3$
H,I	$COLUMN_4$
J,K	$COLUMN_5$
L	CLOCK
M	DISPLAY DATA
N,O	V_{CC}
P,Q	GND

A	HDSP-2416	71.120 (2.800)
B	HDSP-2424	106.680 (4.200)
C	HDSP-2432	142.240 (5.600)

Figure 14. HDSP-2416/-2424/-2432

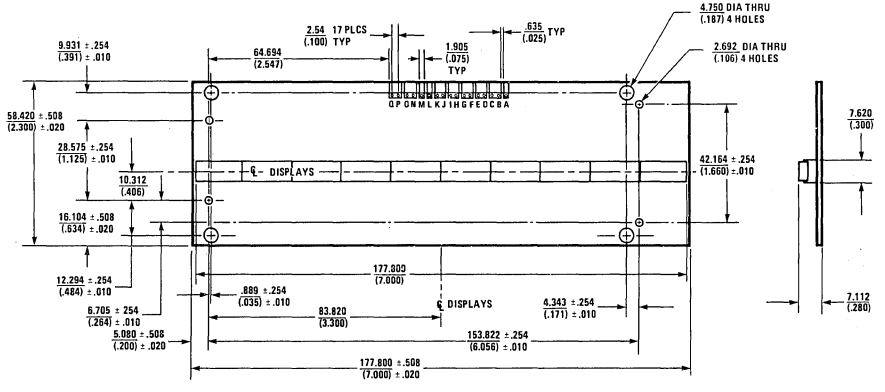


Figure 15. HDSP-2440

HEWLETT hp PACKARD

COMPONENTS

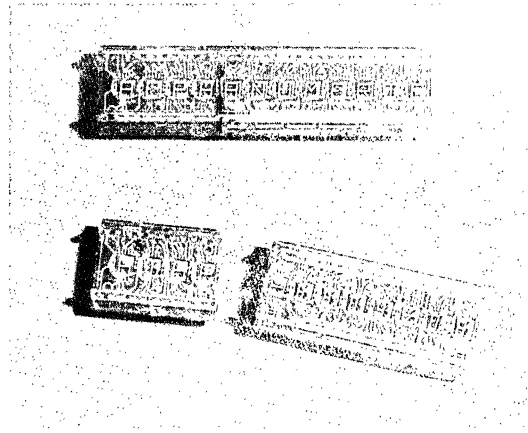
18 SEGMENT SOLID STATE ALPHANUMERIC DISPLAY

HDSP-6504
HDSP-6508

TECHNICAL DATA APRIL 1979

Features

- **ALPHANUMERIC**
  Displays 64 Character ASCII Set and Special Characters
- **16 SEGMENT FONT PLUS CENTERED D.P. AND COLON**
- **3.81mm (0.150") CHARACTER HEIGHT**
- **APPLICATION FLEXIBILITY WITH PACKAGE DESIGN**
  4 and 8 Character Dual-In-Line Packages
  End Stackable-On Both Ends for 8 Character and On One End for 4 Character
  Sturdy Gold-Plated Leads on 2.54mm (0.100") Centers
  Environmentally Sealed Package
  Common Cathode Configuration
- **LOW POWER**
  As Low as 1.0-1.5mA Average Per Segment Depending on Peak Current Levels
- **EXCELLENT CHARACTER APPEARANCE**
  Continuous Segment Font
  High On/Off Contrast
  6.35mm (0.250") Character Spacing
  Excellent Character Alignment
  Excellent Readability at 2 Metres
- **SUPPORT ELECTRONICS**
  Can Be Driven With ROM Decoders and Drivers
  Easy Interfacing With Microprocessors and LSI Circuitry
- **CATEGORIZED FOR LUMINOUS INTENSITY**
  Assures Uniformity of Light Output From Unit to Unit Within a Single Category



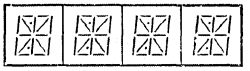
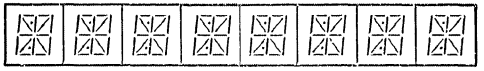
Description

The HDSP-6504 and HDSP-6508 are 3.81mm (0.150") eighteen segment GaAsP red alphanumeric displays mounted in 4 character and 8 character dual-in-line package configurations that permit mounting on PC boards or in standard IC sockets. The monolithic light emitting diode character is magnified by the integral lens which increases both character size and luminous intensity, thereby making low power consumption possible. The rugged package construction offers extended environmental capabilities compared to the standard PC board/lens type of display package. Its temperature cycling capability is the result of the environmentally sealed air gap which exists between the semiconductor chip/wire bond assembly and the lens. Moisture resistance is assured by the epoxy encapsulant on the bottom of the package. In addition to the sixteen segments, a centered D.P. and colon are included. Character spacing yields 4 characters per inch.

Applications

These alphanumeric displays are attractive for applications such as computer peripherals and terminals, computer base emergency mobile units, automotive instrument panels, desk top calculators, in-plant control equipment, hand-held instruments and other products requiring low power, display compactness and alphanumeric display capability.

Device Selection Guide

Characters Per Display	Configuration: Device	Configuration: Package	Part No. HDSP-
4		(Figure 6)	6504
8		(Figure 7)	6508

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
I_{PEAK}	Peak Forward Current Per Segment or DP (Duration ≤ 312μs)		200	mA
I_{AVG}	Average Current Per Segment or DP[1]		7	mA
P_D	Average Power Dissipation Per Character[1,2]		138	mW
T_A	Operating Temperature, Ambient	-40	85	°C
T_S	Storage Temperature	-40	100	°C
V_R	Reverse Voltage		5	V
	Solder Temperature at 1.59mm (1/16 inch) below seating plane, t ≤ 3 Seconds		260	°C

NOTES:
1. Maximum allowed drive conditions for strobed operation are derived from Figures 1 and 2. See electrical section of operational considerations.
2. Derate linearly above T_A = 50°C at 2.17mW/°C. P_D Max. (T_A = 85°C) = 62mW.

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I_V	Luminous Intensity, Time Average, Character Total with 16 Segments Illuminated [3,4]	I_{PEAK} = 30mA 1/16 Duty Factor	0.45	1.65		mcd
V_F	Forward Voltage Per Segment or DP	I_F = 30mA (One Segment On)		1.6	1.9	V
λ_{PEAK}	Peak Wavelength			655		nm
λ_d	Dominant Wavelength [5]			640		nm
I_R	Reverse Current Per Segment or DP	V_R = 5V		10		μA
$\Delta V_F/\Delta°C$	Temperature Coefficient of Forward Voltage			-2		mV/°C

NOTES:
3. The luminous intensity ratio between segments within a digit is designed so that each segment will have the same luminous sterance. Thus each segment will appear with equal brightness to the eye.
4. Operation at peak currents of less than 7mA is not recommended.
5. The dominant wavelength, λd, is derived from the C.I.E. chromaticity diagram and represents that single wavelength which defines the color of the device, standard red.

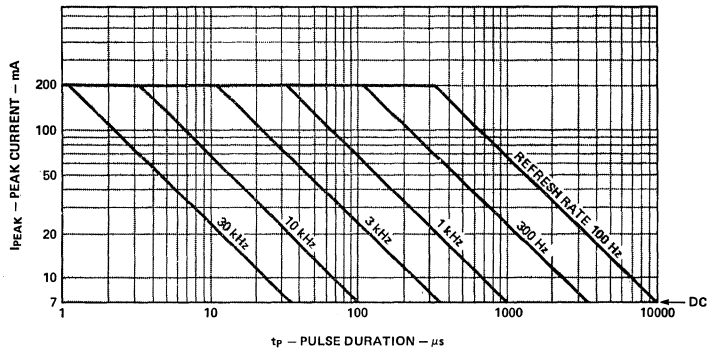


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration. Derate derived operating conditions above T_A = 50°C using Figure 2.

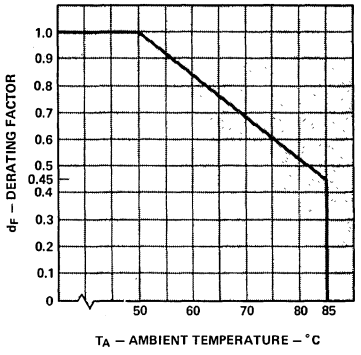


Figure 2. Temperature Derating Factor For Operating Conditions When T_A Exceeds 50°C.

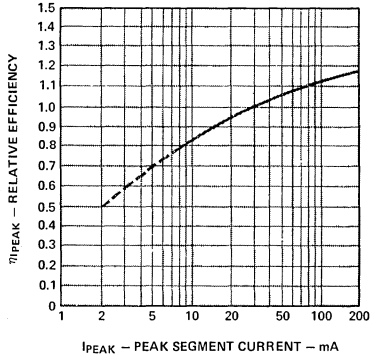


Figure 3. Relative Luminous Efficiency (Luminous Intensity Per Unit Current) vs. Peak Segment Current.

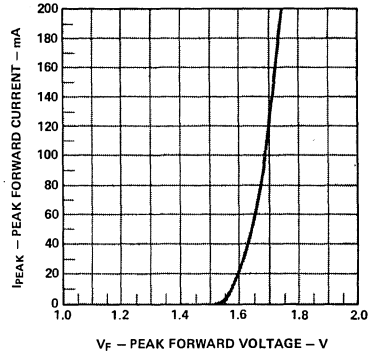


Figure 4. Peak Forward Segment Current vs. Peak Forward Voltage.

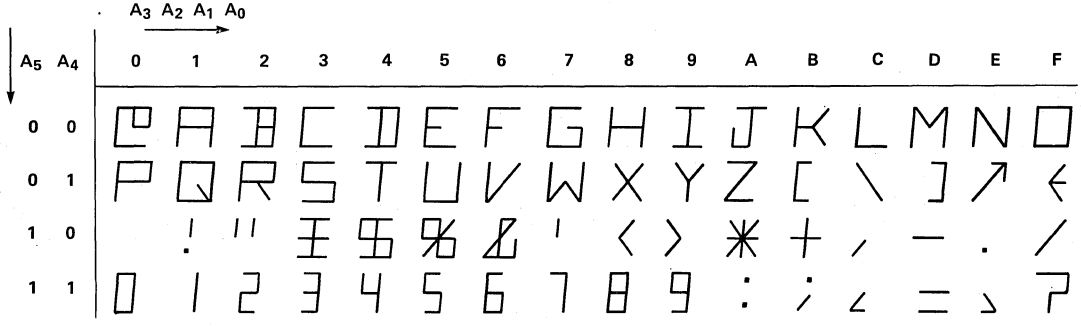
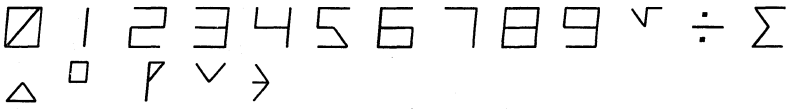


Figure 5. Typical 64 Character ASCII Set.



Additional Character Font

Package Dimensions

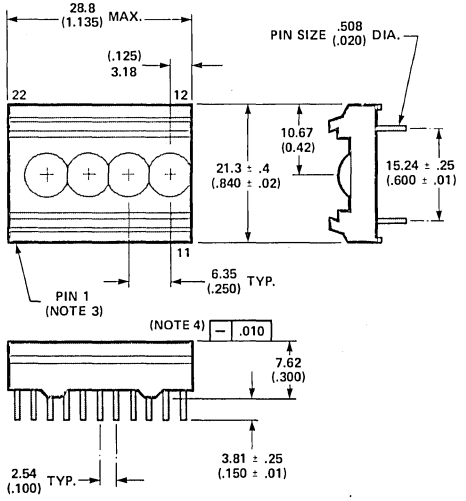


Figure 6. HDSP-6504

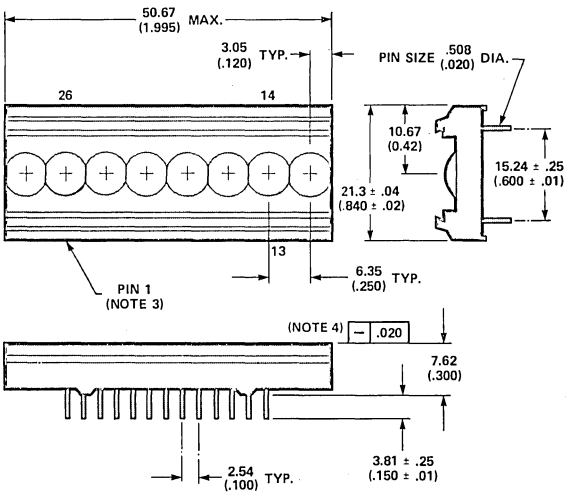


Figure 7. HDSP-6508

NOTES:
1. ALL DIMENSIONS IN MILLIMETRES AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. PIN 1 IDENTIFIED BY INK DOT ADJACENT TO LEAD.
4. DEVICE PACKAGE IS STRAIGHT WITHIN INDICATED LIMIT.

Magnified Character Font Description

DEVICES
HDSP-6504
HDSP-6508

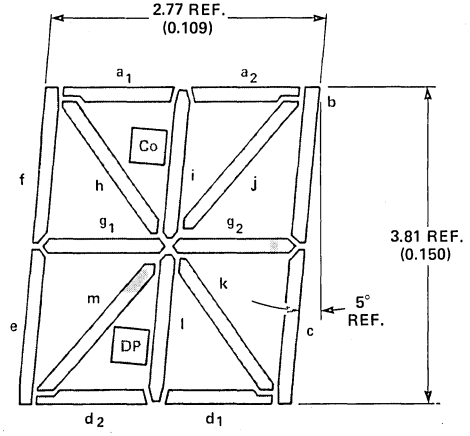


Figure 8.

Device Pin Description

Pin No.	Function			
	HDSP-6504		HDSP-6508	
1	Anode	Segment g_1	Anode	Segment g_1
2	Anode	Segment DP	Anode	Segment DP
3	Cathode	Digit 1	Cathode	Digit 1
4	Anode	Segment d_2	Anode	Segment d_2
5	Anode	Segment l	Anode	Segment l
6	Cathode	Digit 3	Cathode	Digit 3
7	Anode	Segment e	Anode	Segment e
8	Anode	Segment m	Anode	Segment m
9	Anode	Segment k	Anode	Segment k
10	Cathode	Digit 4	Cathode	Digit 4
11	Anode	Segment d_1	Anode	Segment d_1
12	Anode	Segment j	Cathode	Digit 6
13	Anode	Segment C_O	Cathode	Digit 8
14	Anode	Segment g_2	Cathode	Digit 7
15	Anode	Segment a_2	Cathode	Digit 5
16	Anode	Segment i	Anode	Segment j
17	Cathode	Digit 2	Anode	Segment C_O
18	Anode	Segment b	Anode	Segment g_2
19	Anode	Segment a_1	Anode	Segment a_2
20	Anode	Segment c	Anode	Segment i
21	Anode	Segment h	Cathode	Digit 2
22	Anode	Segment f	Anode	Segment b
23			Anode	Segment a_1
24			Anode	Segment c
25			Anode	Segment h
26			Anode	Segment f

Operational Considerations

ELECTRICAL

The HDSP-6504 and -6508 devices utilize large monolithic 16 segment GaAsP LED chips with centered decimal point and colon. Like segments of each digit are electrically interconnected to form an 18 by N array, where N is the quantity of characters in the display. In the driving scheme the decimal point or colon is treated as a separate character with its own time frame. A detailed discussion of character font capabilities, ASCII code to 18 segment decoding and display drive techniques will appear in a forthcoming application note.

These displays are designed specifically for strobed (multiplexed) operation, with a minimum recommended time peak forward current per segment of 7mA. Under normal operating situations the maximum number of illuminated segments needed to represent a given character is 10. Therefore, except where noted, the information presented in this data sheet is for a maximum of 10 segments illuminated per character.*

The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design may be calculated using the following V_F model:

$$V_F = 1.85V + I_{PEAK}\,(1.8\Omega)$$
For: $30mA \le I_{PEAK} \le 200mA$
$$V_F = 1.58V + I_{PEAK}\,(10.7\Omega)$$
For: $10mA \le I_{PEAK} \le 30mA$

Pulsed operating conditions on a per segment basis are derived from Figure 1 and are temperature derated using Figure 2. Figure 1 relates maximum allowed segment peak current, I_{PEAK}, to the maximum allowed pulse duration, t_p, for various strobing refresh rates, f. To most effectively utilize Figure 1, perform the following steps:

1. Determine desired duty factor, DF.
   Example: Sixteen characters, DF = 1/16
2. Determine desired refresh rate, f. Use duty factor to calculate pulse duration, t_p. Note: $DF = ft_p$
   Example: f = 1kHz, $t_p = 62.5\mu s$
3. Enter Figure 1 at the calculated t_p. Move vertically to the refresh rate line and record the corresponding value of I_{PEAK}.
   Example: At $t_p = 62.5\mu s$ and f = 1kHz, I_{PEAK} = 100mA
   $I_{AVG} = I_{PEAK} \bullet DF = (100mA)\,(1/16) = 6.25mA$
4. The maximum allowed operating conditions, not temperature derated, are now known. If the operating ambient temperature is above 50°C, the operating conditions derived from Figure 1 must be temperature derated.

   Figure 2 derates the product $I_{PEAK} \bullet t_p$ with ambient temperature. The designer has the option of maintaining either t_p or I_{PEAK} and derating I_{PEAK} or t_p. The choice of derating I_{PEAK} results in a lower power dissipation with the least loss of light output. To obtain the temperature derated operating conditions perform the following steps.
5. Determine maximum operating ambient temperature.
   Example: $T_A = 70°C$
6. Multiply $I_{PEAK} \bullet t_p$.
   Example: $(100mA)\,(62.5\mu s) = 6250mA - \mu s$
7. From Figure 2 determine derating factor, d_F. Multiply above $I_{PEAK} \bullet t_p$ product by d_F.
   Example: At $T_A = 70°C$, $d_F = 0.69$
   $d_F (I_{PEAK} \bullet t_p) = (0.69)\,(6250) = 4312.5mA - \mu s$
8. Calculate derated operating conditions.
   Example: Maintain $t_p = 62.5\mu s$ and derate I_{PEAK}

$$I_{PEAK} = \frac{4312.5mA - \mu s}{62.5\mu s} = 69mA \text{ peak current}$$

The maximum allowed operating conditions, temperature derated to an ambient of 70°C are now determined.

Example: f = 1kHz, $t_p = 62.5\mu s$, I_{PEAK} = 69mA and I_{AVG} = 4.31mA.

The above calculations determine the maximum allowed strobing conditions. Operation at a reduced combination of peak current and pulse width may be desirable to adjust display light output to match ambient light levels and/or to insure even more reliable operation.

Refresh rates of 1kHz or faster provide the most efficient operation resulting in the maximum possible light output for long character strings.

The time average luminous intensity may be calculated using the relative efficiency characteristic of Figure 3, $\eta_{I_{PEAK}}$, and correcting for operating ambient temperature. The time average luminous intensity at $T_A = 25°C$ is calculated as follows:

$$I_{V\ TIME\ AVG} = \left[\frac{I_{PEAK} \bullet DF}{1.875mA}\right] [\eta_{I_{PEAK}}] [I_{V\ DATA\ SHEET}]$$

$$\text{Example: } I_{V\ TIME\ AVG} = \left[\frac{(69mA)\,(1/16)}{1.875mA}\right] [1.10] [1.65mcd]$$

$I_{V\ TIME\ AVG}$ = 4.17mcd/digit, total for 16 segments, $T_A = 25°C$

This time average luminous intensity is corrected for temperature by the following exponential equation:

$$I_V (T_A) = I_V (25°C) e^{[-.0188°/C\,(T_A - 25°C)]}$$

Example: for $T_A = 70°C$,

$I_V (70°C) = (4.17mcd) e^{[-.0188\,(70 - 25°C)]}$ = 1.79mcd/digit total for 16 segments

OPTICAL AND CONTRAST ENHANCEMENT

Each large monolithic chip is positioned under a separate element of a plastic aspheric magnifying lens, producing a magnified character height of 3.810mm (.150 inch). The aspheric lens provides wide included viewing angles of typically 75 degrees horizontal and 75 degrees vertical with low off axis distortion. These two features, coupled

*More than 10 segments may be illuminated in a given character, provided the maximum allowed character power dissipation, temperature derated, is not exceeded.

with the very high segment luminous sterance, provide to the user a display with excellent readability in bright ambient light for viewing distances in the range of 2 metres. Effective contrast enhancement can be obtained by employing any of the following optical filter products: Panelgraphic: Ruby Red 60, Dark Red 63 or Purple 90; SGL Homalite: H100-1605 Red or H100-1804 Purple, Plexiglas 2423. For very bright ambients, such as indirect sunlight, the 3M Light Control Film is recommended: Red 655, Violet, Purple or Neutral Density.

For those applications requiring only 4 or 8 characters, a secondary barrel magnifier, HP part number HDSP-6505 (four character) and -6509 (eight character), may be inserted into support grooves on the primary magnifier. This secondary magnifier increases the character height to 4.45mm (.175 inch) without loss of horizontal viewing angle (see below).

MECHANICAL

These devices are constructed by LED die attaching and wire bonding to a high temperature PC board substrate. A precision molded plastic lens is attached to the PC board and the resulting assembly is backfilled with a sealing epoxy to form an environmentally sealed unit.

The four character and eight character devices can be end stacked to form a character string which is a multiple of a basic four character grouping. As an example, one -6504 and two -6508 devices will form a 20 character string. These devices may be soldered onto a printed circuit board or inserted into 24 and 28 pin DIP LSI sockets. The socket spacing must allow for device end stacking.

The absolute maximum allowed LED junction temperature, $T_J$max, is 110° C. The maximum power ratings have been established so as not to exceed this limit. For most reliable operation, it is recommended that the PC board thermal resistance to ambient be less than 108° C/W/character. This will then establish a maximum thermal resistance LED junction-to-ambient of 340° C/W/character.

Optimum wave soldering is accomplished by using a good quality RMA rosin or organic acid flux and setting the solder wave temperature and dwell time at 245° C for 1-1/2 to 2 seconds. For device cleaning in a vapor cleaning process, only mixtures of Freon (F113) and alcohol is recommended with an immersion time in the vapors for less than 2 minutes. Suggested cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

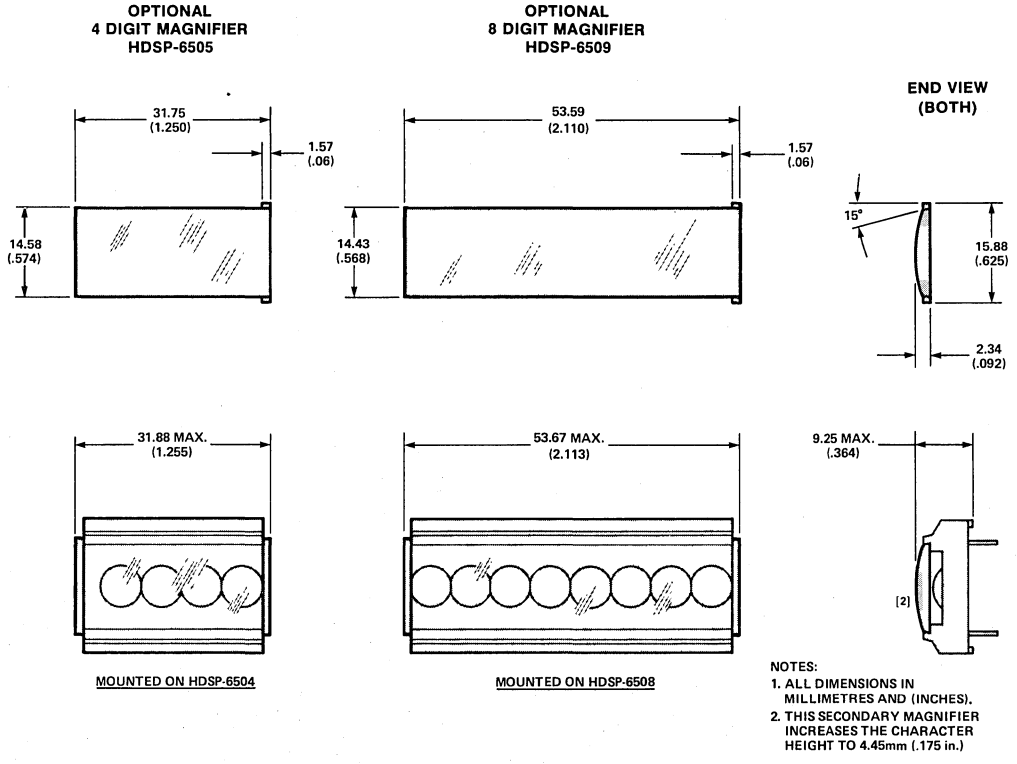


Figure 9. Design Data for Optional Barrel Magnifier in Single Display Applications.

HEWLETT PACKARD

COMPONENTS

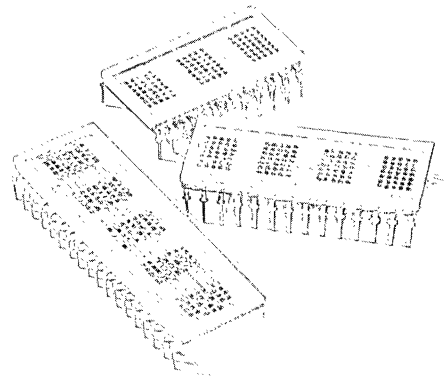
LED SOLID STATE ALPHANUMERIC INDICATOR

5082-7100
5082-7101
5082-7102

TECHNICAL DATA APRIL 1979

Features

- **5 x 7 LED MATRIX CHARACTER**
  Human Factors Engineered
- **BRIGHTNESS CONTROLLABLE**
- **IC COMPATIBLE**
- **SMALL SIZE**
  Standard 15.24mm (.600 inch) Dual In-Line Package; 6.9mm (.27 inch) Character Height
- **WIDE VIEWING ANGLE**
- **RUGGED, SHOCK RESISTANT**
  Hermetically Sealed
  Designed to Meet MIL Standards
- **LONG OPERATING LIFE**



Description

The Hewlett-Packard 5082-7100 Series is an X-Y addressable, 5 x 7 LED Matrix capable of displaying the full alphanumeric character set. This alphanumeric indicator series is available in 3, 4, or 5 character end-stackable clusters. The clusters permit compact presentation of information, ease of character alignment, minimum number of interconnections, and compatibility with multiplexing driving schemes.

Alphanumeric applications include computer terminals, calculators, military equipment and space flight readouts.

The **5082-7100** is a three character cluster.
The **5082-7101** is a four character cluster.
The **5082-7102** is a five character cluster.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Peak Forward Current Per LED (Duration < 1 ms)	I_{PEAK}		100	mA
Average Current Per LED	I_{AVG}		10	mA
Power Dissipation Per Character (All diodes lit) [1]	P_D		700	mW
Operating Temperature, Case	T_C	–55	95	°C
Storage Temperature	T_S	–55	100	°C
Reverse Voltage Per LED	V_R		4	V

Note 1: At 25°C Case Temperature; derate 8.5 mW/°C above 25°C.

Electrical / Optical Characteristics at T_C=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units
Peak Luminous Intensity Per LED (Character Average) @ Pulse Current of 100mA/LED	$I_{V\ (PEAK)}$	1.0	2.2		mcd
Reverse Current Per LED @ V_R = 4V	I_R		10		μA
Peak Forward Voltage @ Pulse Current of 50mA/LED	V_F		1.7	2.0	V
Peak Wavelength	λ_{PEAK}		655		nm
Spectral Line Halfwidth	$\Delta\lambda_{1/2}$		30		nm
Rise and Fall Times [1]	t_r, t_f		10		ns

Note 1. Time for a 10% - 90% change of light intensity for step change in current.

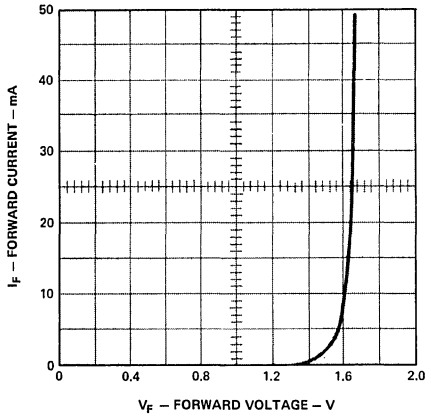


Figure 1. Forward Current-Voltage Characteristic.

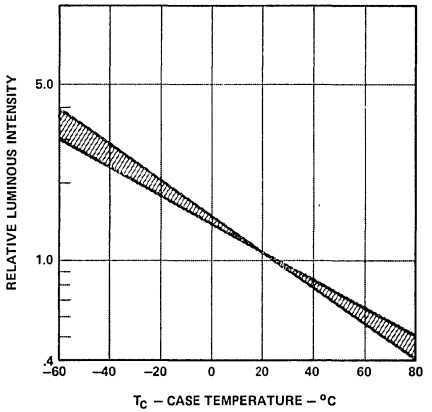


Figure 2. Relative Luminous Intensity vs. Case Temperature at Fixed Current Level.

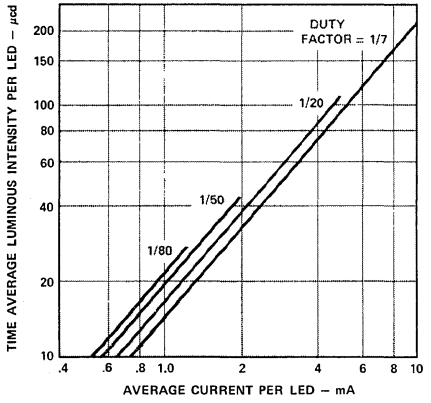


Figure 3. Typical Time Average Luminous Intensity per LED vs. Average Current per LED.

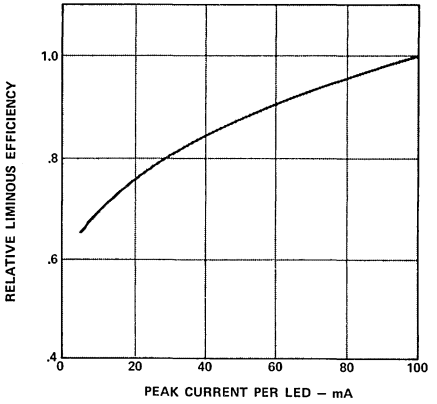
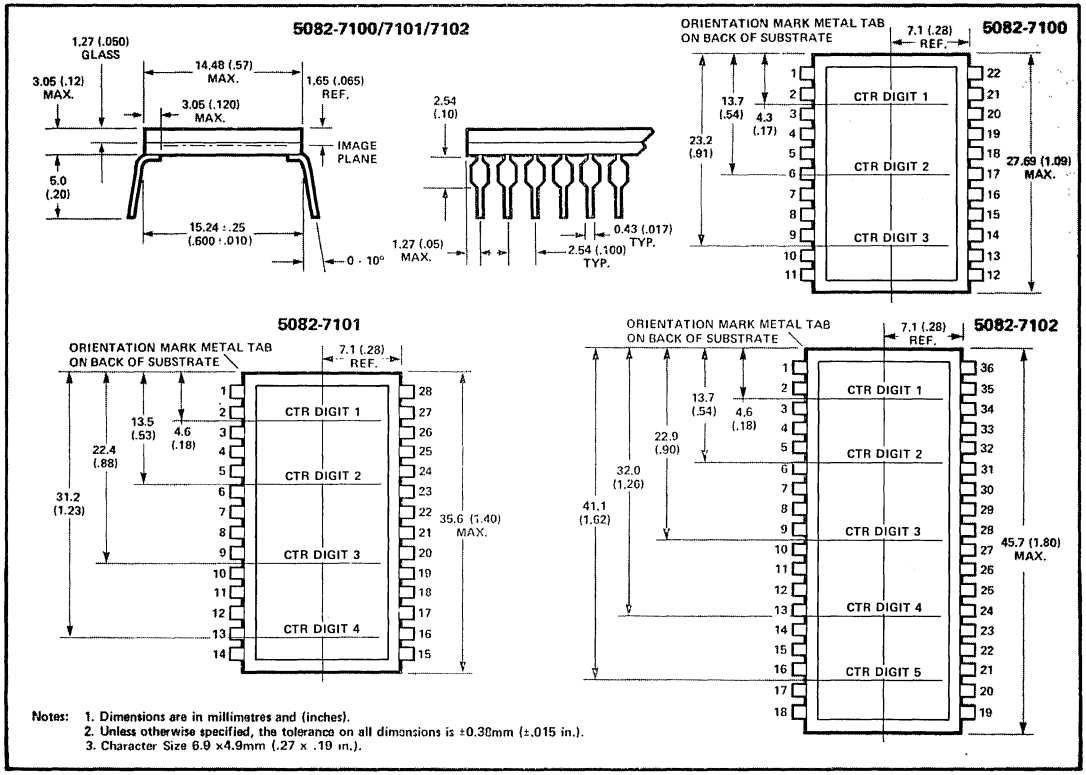


Figure 4. Typical Relative Luminous Efficiency vs. Peak Current per LED.

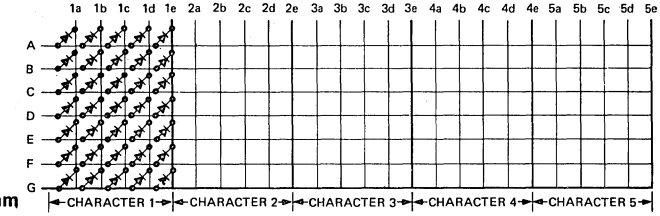
Package Dimensions and Pin Configurations



Notes:
1. Dimensions are in millimetres and (inches).
2. Unless otherwise specified, the tolerance on all dimensions is ±0.38mm (±.015 in.).
3. Character Size 6.9 x4.9mm (.27 x .19 in.).

Device Pin Description

5082-7100				5082-7101				5082-7102			
Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	Anode G	12	Anode B	1	N/C	15	Anode C	1	N/C	19	5e
2	1c	13	3d	2	1c	16	4c	2	1c	20	5c
3	1d	14	3b	3	1e	17	4a	3	1e	21	5a
4	Anode F	15	Anode A	4	Anode G	18	Anode B	4	Anode F	22	Anode D
5	Anode E	16	2e	5	2b	19	3e	5	2b	23	4e
6	2b	17	2c	6	2d	20	3b	6	2d	24	4c
7	2d	18	2a	7	Anode D	21	3a	7	2e	25	N/C
8	Anode C	19	Anode D	8	Anode E	22	2e	8	Anode E	26	Anode C
9	3a	20	1e	9	3c	23	2c	9	3c	27	3d
10	3c	21	1b	10	3d	24	2a	10	3e	28	3b
11	3e	22	1a	11	Anode F	25	Anode A	11	Anode G	29	3a
				12	4b	26	1d	12	4a	30	Anode B
				13	4d	27	1b	13	4b	31	2c
				14	4e	28	1a	14	4d	32	2a
								15	N/C	33	Anode A
								16	5b	34	1d
								17	5d	35	1b
								18	N/C	36	1a



5082-7100/7101/7102
Schematic Wiring Diagram

Operating Considerations

ELECTRICAL

The 5 x 7 matrix of LED's, which make up each character, are X-Y addressable. This allows for a simple addressing, decoding and driving scheme between the display module and customer furnished logic.

There are three main advantages to the use of this type of X-Y addressable array:

1. It is an elementary addressing scheme and provides the least number of interconnection pins for the number of diodes addressed. Thus, it offers maximum flexibility toward integrating the display into particular applications.
2. This method of addressing offers the advantage of sharing the Read-Only-Memory character generator among several display elements. One character generating ROM can be shared over 25 or more 5 x 7 dot matrix characters with substantial cost savings.
3. In many cases equipments will already have a portion of the required decoder/driver (timing and clock circuitry plus buffer storage) logic circuitry available for the display.

To form alphanumeric characters a method called "scanning" or "strobing" is used. Information is addressed to the display by selecting one row of diodes at a time, energizing the appropriate diodes in that row and then proceeding to the next row. After all rows have been excited one at a time, the process is repeated. By scanning through all rows at least 100 times a second, a flicker free character can be produced. When information moves sequentially from row to row of the display (top to bottom) this is row scanning, as illustrated in Figure 5. Information can also be moved from column to column (left to right across the display) in a column scanning mode. For most applications (5 or more characters to share the same ROM) it is more economical to use row scanning.

A much more detailed description of general scanning techniques along with specific circuit recommendations is contained in HP Application Note 931.

MECHANICAL/THERMAL MOUNTING

The solid state display typically operates with 200 mW power dissipation per character. However, if the operating conditions are such that the power dissipation exceeds the derated maximum allowable value, the device should be heat sunk. The usual mounting technique combines mechanical support and thermal heat sinking in a common structure. A metal strap or bar can be mounted behind the display using silicone grease to insure good thermal control. A well-designed heat sink can limit the case temperature to within 10°C of ambient.

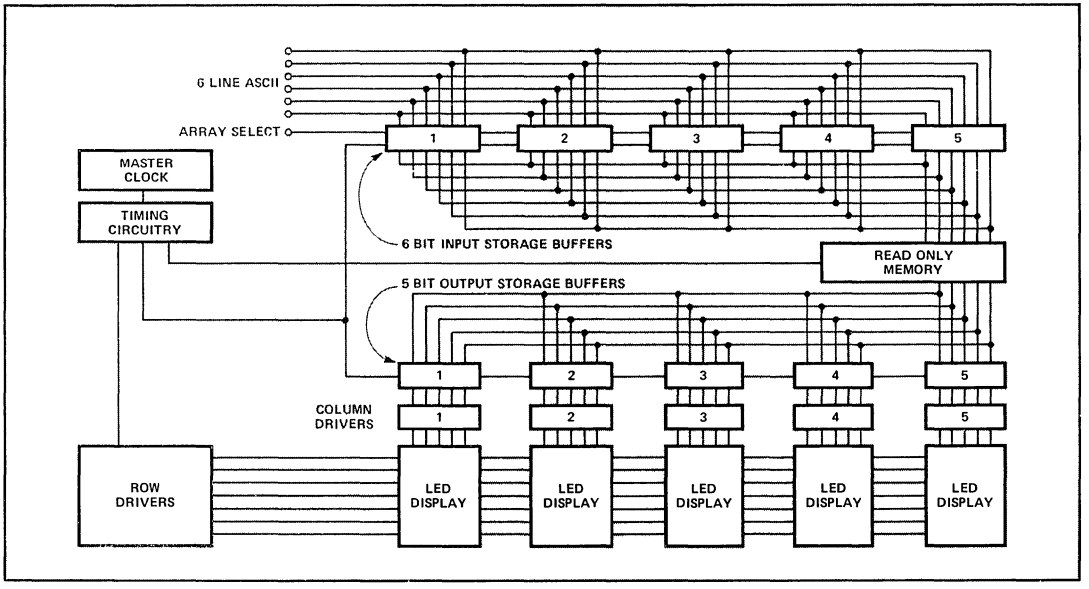
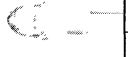
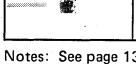


Figure 5. Row Scanning Block Diagram.

Solid State Lamps

Optoelectronics Designer's Catalog 1979

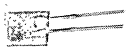
High Efficiency Red, Yellow, Green LED Lamps

Device		Description				Typical Luminous Intensity	2Θ½ [1]	Typical Forward Voltage	Page No.
Photo	Part No. 5082-	Color	Emitting Material	Lens	Package				
	4650	High Efficiency Red (635nm)[2]	GaAsp on GaP	Red Diffused	T-1¾; Plastic; Long, General Purpose Leads[3]	2.0mcd @10mA	90°	2.2 Volts @10mA	149
	4655					4.0mcd @10mA			
	4657			Red Non-Diffused		12.0mcd @10mA	35°		
	4658					24.0mcd @10mA			
	4690			Red Diffused	T-1¾ (Low Profile) Plastic; Long, General Purpose Leads	3.5mcd @10mA	50°		157
	4693					7.0mcd @10mA			
	4694			Red Non-Diffused		8.0mcd @10mA	45°		
	4695					11.0mcd @10mA			
	HLMP-1300			Red Diffused	T-1, Plastic, Long Leads[4]	1.5mcd @10mA	70°		141
	HLMP-1301 (5082-4684)					2.0mcd @10mA			
	HLMP-1302					2.5mcd @10mA			
	4160				Submin.; Plastic; Radial Leads	3.0mcd @10mA	80°		163
	HLMP-0300				Rectangular; Plastic; Long, Gen. Purpose Leads	1.0mcd @25mA	100°	2.5 Volts @25mA	137
	HLMP-0301 (5082-4670)					2.5mcd @25mA 1.5mcd @15mA			
	HLMP-2300				Light Bar Module; 4 Pin In-Line; .100" Centers; .400" L x .195"W x .240"H	7mcd @ 20mA	–	1.9 Volts @20mA	131
	HLMP-2350				Light Bar Module; 8 Pin In-Line; .100" Centers; .800" L x .195"W x .240"H	15mcd @ 20mA			
	4550	Yellow (583nm)[2]	GaAsP on GaP	Yellow Diffused	T-1¾; Plastic; Long General Purpose Leads[3]	1.8mcd @10mA	90°	2.2 Volts @10mA	149
	4555					3.0mcd @10mA			
	4557			Yellow Non-Diffused		9.0mcd @10mA	35°		
	4558					16.0mcd @10mA			
	4590			Yellow Diffused	T-1¾ (Low Profile) Plastic; Long, General Purpose Leads	3.5mcd @10mA	50°		157
	4592					6.0mcd @10mA			
	4595			Yellow Non-Diffused		6.5mcd @10mA	45°		
	4597					11.0mcd @10mA			
	HLMP-1400			Yellow Diffused	T-1; Plastic; Long Leads[4]	1.5mcd @10mA	60°		141
	HLMP-1401 (5082-4584)					2.5mcd @10mA			
	HLMP-1402					4.0mcd @10mA			
	4150				Submin.; Plastic; Radial Leads	2.0mcd @10mA	90°		163

Notes: See page 130.

For Applications Information, see page 247.

High Efficiency Red, Yellow, Green LED Lamps (Cont.)

Device		Description				Typical Luminous Intensity	2Θ½ [1]	Typical Forward Voltage	Page No.
Photo	Part No. 5082-	Color	Emitting Material	Lens	Package				
	HLMP-0400	Yellow (583nm) [2]	GaAsP on GaP	Yellow Diffused	Rectangular; Plastic; Long, Gen. Purpose Leads	1.2mcd @25mA	100°	2.5 Volts @25mA	137
	HLMP-0401 (5082-4570)					2.5mcd @25mA 1.5mcd @15mA			
	HLMP-2400				Light Bar Module; 4 Pin In-Line; .100" Centers: .400" L x .195"W x .240" H	5mcd @ 20mA	–	2.0 Volts @20mA	131
	HLMP-2450				Light Bar Module; 8 Pin In-Line; .100" Centers; .800" L x .195"W x .240"H	11mcd @ 20mA			
	4950	Green (565nm) [2]	GaP	Green Diffused	T-1¾; Plastic; Long General Purpose Leads [3]	1.8mcd @20mA	90°	2.4 Volts @20mA	149
	4955					3.0mcd @20mA			
	4957			Green Non-Diffused		9.0mcd @20mA	30°		
	4958					16.0mcd @20mA			
	4990			Green Diffused	T-1¾ (Low Profile) Plastic; Long General Purpose Leads	4.5mcd @20mA	50°		157
	4992					7.5mcd @20mA			
	4995			Green Non-Diffused		6.5mcd @20mA	40°		
	4997					11.0mcd @20mA			
	HLMP-1500			Green Diffused	T-1; Plastic; Long Leads [4]	1.2mcd @10mA	60°		141
	HLMP-1501 (5082-4984)					2.0mcd @10mA			
	HLMP-1502					3.0mcd @10mA			
	4190				Submin.; Plastic; Radial Leads	1.5mcd @20mA	70°		163
	HLMP-0500				Rectangular; Plastic; Long, Gen. Purpose Leads	1.2mcd @25mA	100°	2.5 Volts @25mA	137
	HLMP-0501 (5082-4970)					2.5mcd @25mA 1.5mcd @15mA			
	HLMP-2500				Light Bar Module; 4 Pin In-Line; .100" Centers: .400" L x .195"W x .240"H	3.5mcd @ 20mA	–	2.1 Volts @20mA	131
	HLMP-2550				Light Bar Module; 8 Pin In-Line; .100" Centers: .800"L x .195"W x .240"H	7.5mcd @ 20mA			

Notes: See page 130.

For Applications Information, see page 247.

Red LED Lamps

Device		Description				Typical Luminous Intensity	2Θ½ [1]	Typical Forward Voltage	Page No.
Photo	Part No. 5082-	Color	Emitting Material	Lens	Package				
	HLMP-6203	Red (655nm)[2]	GaAsP on GaAs	Red Diffused	Array; Plastic Radial Leads	1.0mcd @ 10mA	45°	1.6 Volts @10mA	167
	HLMP-6204								
	HLMP-6205								
	4100				Submin.; Plastic; Radial Leads	0.5mcd @ 10mA			163
	4101					1.0mcd @ 10mA			
 4403/4440	4403				T-1¾; Plastic; Short, Leads[3]	1.2mcd @ 20mA	75°	1.6 Volts @20mA	145
	4415				T-1¾; Plastic; Short, Bent Leads[4]				
 4415/4444	4440				T-1¾; Plastic; Short Leads[3]	0.7mcd @ 20mA			
	4444				T-1¾; Plastic; Short Bent Leads[4]				
	4480				T-1; Plastic; Long Leads[4]	0.8mcd @ 20mA	120°		147
	4483			Clear Diffused					
	4486			Clear Non-Diffused			80°		
	4484					1.4mcd @ 20mA	120°		153
	4494								
	4487				T-1 (Low Profile); Plastic; Long Leads[4]	0.8mcd @ 20mA			155
	4488					Guaranteed Min. 0.3mcd @ 20mA			
	4790			Red Diffused	T-1¾ (Low Profile); Plastic; Long, Gen. Purpose Leads	1.2mcd @ 20mA	60°		157
	4791					2.5mcd @ 20mA			
	4850				T-1¾; Plastic; Long Wire Wrap Leads[3]	0.8mcd @ 20mA	95°		153
	4855					1.4mcd @ 20mA			

Notes: See page 130.

For Applications Information, see page 247.

Red LED Lamps (Cont.)

Device		Description				Typical Luminous Intensity	2Θ½ [1]	Typical Forward Voltage	Page No.
Photo	Part No. 5082-	Color	Emitting Material	Lens	Package				
	4880	Red (655nm)[2]	GaAsP on GaAs	Red Diffused	T-1¾; Plastic; Long Wire Wrap. Leads[3]	0.8mcd @20mA	58°	1.6 Volts @20mA	145
	4883			Clear Non-Diffused			50°		
	4886			Clear Diffused			65°		
	4881			Red Diffused		1.3mcd @20mA	58°		
	4884			Clear Non-Diffused			50°		
	4887			Clear Diffused			65°		
	4882			Red Diffused		1.8mcd @20mA	58°		
	4885			Clear Non-Diffused			50°		
	4888			Clear Diffused			65°		

Integrated LED Lamps

Device		Description				Typical Luminous Intensity	2Θ½ [1]	Typical Forward Current	Page No.
Photo	Part No. 5082-	Color	Integration	Lens	Package				
	4732	Red (655nm) [2]	Voltage Sensing IC integrated with GaAsP LED chip	Red Diffused	T-1; Plastic; Long Leads[4]	0.7mcd @2.75V	95°	13mA @ 2.75V	171
	4860		Resistor chip integrated with GaAsP LED chip	Red Diffused	T-1¾; Plastic; Long Leads[3]	0.8mcd @5.0V	58°	16mA @ 5.0V	173
	4468			Clear Diffused	T-1; Plastic; Long Leads[4]		70°		
	HLMP-6620		Resistor chip integrated with High Efficiency Red LED chip	Red Diffused	Submin., Plastic; Radial Leads	0.6mcd @5.0V	90°	3.5mA @ 5.0V	169
	HLMP-6600					2.4mcd @5.0V		9.6mA @ 5.0V	

Notes: See page 130.

For Applications Information, see page 247.

Hermetically Sealed and High Reliability LED Lamps

Device		Description				Minimum Luminous Intensity	2Θ½ [1]	Typical Forward Voltage	Page No.
Photo	Part No.	Color	Emitting Material	Lens	Package				
	1N5765 JAN 1N5765[5] JAN TX 1N5765[5]	Red (655nm)[2]	GaAsP on GaAs	Red Diffused	Hermetic/TO-46; Long Leads[4]	0.5mcd @ 20mA	70°	1.6 Volts @ 20mA	175
	5082-4787 HLMP-0930[5] HLMP-0931[5]				Panel Mount Version				
	1N6092 JAN 1N6092[5] JANTX 1N6092[5]	High Efficiency Red (635nm)[2]	GaAsP on GaP	Red Diffused	Hermetic/TO-46 Long Leads[4]	1.0mcd @ 20mA		2.0 Volts @ 20mA	
	5082-4687 M 19500/519-01[5] M 19500/519-02[5]				Panel Mount Version				
	1N6093 JAN 1N6093[5] JANTX 1N6093[5]	Yellow (583nm)[2]	GaAsP on GaP	Yellow Diffused	Hermetic/TO-46 Long Leads[4]				
	5082-4587 M 19500/520-01[5] M 19500/520-02[5]				Panel Mount Version				
	1N6094 JAN 1N6094[5] JANTX 1N6094[5]	Green (565nm)[2]	GaP	Green Diffused	Hermetic/TO-46 Long Leads[4]	0.8mcd @ 25mA		2.1 Volts @ 25mA	
	5082-4987 M 19500/521-01[5] M19500/521-02[5]				Panel Mount Version				

NOTES:
1. Θ½ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. Peak Wavelength.
3. Panel Mountable. For Panel Mounting Kit, see page 50.
4. PC Board Mountable.
5. Military Approved and qualified for High Reliability Applications.

For Applications Information, see page 247.

HEWLETT hp PACKARD

COMPONENTS

NEW PRODUCT

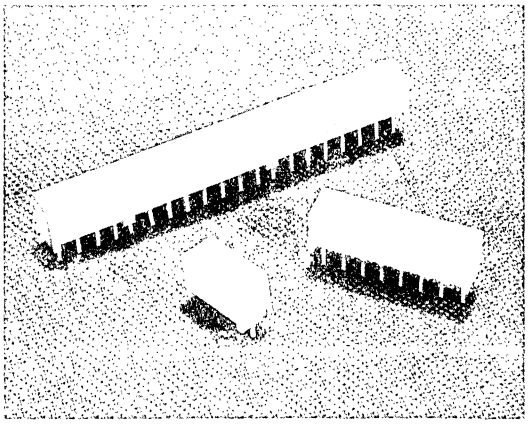
9 mm (0.35 INCH) AND 19 mm (0.75 INCH) LIGHT BAR MODULES

HIGH EFFICIENCY RED HLMP-2300 SERIES
YELLOW HLMP-2400 SERIES
GREEN HLMP-2500 SERIES

TECHNICAL DATA APRIL 1979

Features

- **LARGE, BRIGHT, UNIFORM LIGHT EMITTING SURFACE**
  - **Typical Luminous Stearance 260 cd/m² at 100mA Peak, 20mA Average**
  - **Approximately Lambertian Radiation Pattern**
- **SUITABLE FOR MULTIPLEX OPERATION**
  - **LED's in Either Parallel, Series or Parallel/ Series Connection**
- **CHOICE OF THREE COLORS**
  - **High Efficiency Red**
  - **Yellow**
  - **Green**
- **CATEGORIZED FOR LIGHT OUTPUT**
  - **Use of Like Chip Categories Yields a Uniform Display**
- **EASILY MOUNTED ON P.C. BOARDS OR SOCKETS**
  - **Single In-Line Package, Leads on Industry Standard 2.54mm (0.1 in.) Centers**
  - **I.C. Compatible**
  - **Mechanically Rugged**
- **X–Y STACKABLE**
- **FLUSH MOUNTABLE**
- **EASY ALIGNMENT**
- **EXCELLENT ON-OFF CONTRAST**



Applications

- **ILLUMINATED LEGENDS**
- **INDICATORS**
- **BAR GRAPHS**
- **LIGHTED SWITCHES**

Description

The HLMP-2300/-2400/-2500 series light bar modules are 9mm (.35 inch) and 19mm (.75 inch) rectangular light sources designed for a variety of applications where a large, bright source of light is required. The -2300 and -2400 series devices utilize LED chips which are made from GaAsP on a transparent GaP substrate. The-2500 series devices utilize chips made from GaP on a transparent GaP substrate.

Devices

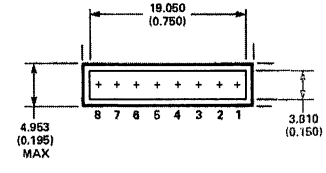
Part No. HLMP-	Color	Size of Emitting Area	Package Drawing
2300	High Efficiency Red	8.89mm x 3.81mm (.350 in. x .150 in.)	A
2350		19.05mm x 3.81mm (.750 in. x .150 in.)	B
2400	Yellow	8.89mm x 3.81mm (.350 in. x .150 in.)	A
2450		19.05mm x 3.81mm (.750 in. x .150 in.)	B
2500	Green	8.89mm x 3.81mm (.350 in. x .150 in.)	A
2550		19.05mm x 3.81mm (.750 in. x .150 in.)	B

Absolute Maximum Ratings

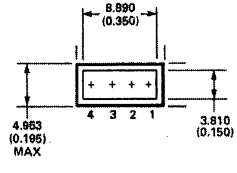
Average Power Dissipation Per LED Chip (T_A=50°C) 87mW
Operating Temperature Range ..... −40°C to +85°C
Storage Temperature Range ..... −40°C to +85°C
Peak Forward Current Per LED Chip (T_A=50°C)[2,3] 120mA
(Maximum Pulse Width = 1.25ms)
DC Forward Current Per LED Chip (T_A=50°C)[1,3] 30mA
Reverse Voltage Per LED Chip 6.0V
Lead Soldering Temperature [1.6mm (1/16 inch) below seating plane] ..... 260°C for 3 Seconds

NOTES: 1. Derate maximum DC current above T_A=50°C at 0.51 mA/°C per LED chip, see Figure 2.
2. See Figure 1 to establish pulsed operating conditions.
3. For extended temperature operation, see Figure 6 for P.C. board thermal resistance requirements.

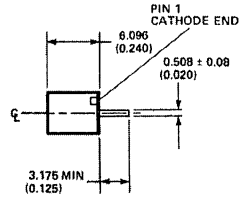
Package Dimensions



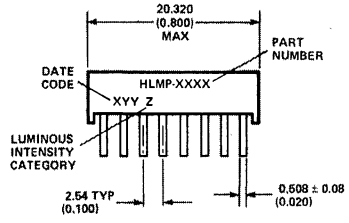
TOP B



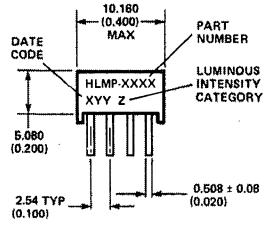
TOP A



END VIEW A, B

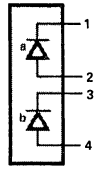


SIDE B

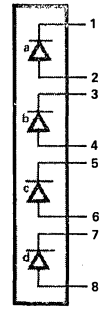


SIDE A

Internal Circuit Diagram



A



B

	FUNCTION	
PIN	A -2300/-2400 -2500	B -2350/-2450 -2550
1	Cathode — a	Cathode — a
2	Anode — a	Anode — a
3	Cathode — b	Cathode — b
4	Anode — b	Anode — b
5		Cathode — c
6		Anode — c
7		Cathode — d
8		Anode — d

NOTES: 1. Dimensions in millimetres and (inches).
2. Tolerances ±.25 mm unless otherwise indicated.

Electrical/Optical Characteristics at T_A=25°C

HIGH EFFICIENCY RED HLMP-2300/-2350

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity[4] with All LED's Illuminated	-2300	I_V	100mA Pk: 1 of 5 Duty Factor		10		mcd
			20mA DC	3	7		mcd
	-2350	I_V	100mA Pk: 1 of 5 Duty Factor		21		mcd
			20mA DC	7	15		mcd
Peak Wavelength		λpeak			635		nm
Dominant Wavelength[5]		λ_d			626		nm
Forward Voltage Per LED		V_F	I_F=100mA		2.5	3.5	V
			I_F= 20mA		1.9	2.6	
Reverse Current Per LED		I_R	V_R=6V		10		μA
Temperature Coefficient of V_F Per LED		ΔV_F/°C	I_F=100mA		−1.1		mV/°C

YELLOW HLMP-2400/-2450

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity[4] with All LED's Illuminated	-2400	I_V	100mA Pk: 1 of 5 Duty Factor		8		mcd
			20mA DC	2	5		mcd
	-2450	I_V	100mA Pk: 1 of 5 Duty Factor		18		mcd
			20mA DC	5	11		mcd
Peak Wavelength		λpeak			583		nm
Dominant Wavelength[5]		λ_d			585		nm
Forward Voltage Per LED		V_F	I_F=100mA		2.6	3.5	V
			I_F= 20mA		2.0	2.6	
Reverse Current Per LED		I_R	V_R=6V		10		μA
Temperature Coefficient of V_F Per LED		ΔV_F/°C	I_F=100mA		−1.1		mV/°C

GREEN HLMP-2500/-2550

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Units
Luminous Intensity[4] with All LED's Illuminated	-2500	I_V	100mA Pk: 1 of 5 Duty Factor		6		mcd
			20mA DC	1.5	3.5		mcd
	-2550	I_V	100mA Pk: 1 of 5 Duty Factor		13		mcd
			20mA DC	3.5	7.5		mcd
Peak Wavelength		λpeak			565		nm
Dominant Wavelength[5]		λ_d			572		nm
Forward Voltage Per LED		V_F	I_F=100mA		2.7	3.6	V
			I_F= 20mA		2.1	2.6	
Reverse Current Per LED		I_R	V_R=6V		10		μA
Temperature Coefficient of V_F Per LED		ΔV_F/°C	I_F=100mA		−1.1		mV/°C

NOTES: 4. Each device is categorized for luminous intensity with the intensity category designated by a letter located on the right hand side of the package.
5. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and is that single wavelength which defines the color of the device.

Operational Considerations

Electrical

The HLMP-2300/-2400/-2500 series of light bar devices are composed of two or four light emitting diodes, with the light from each LED optically scattered to form an evenly illuminated light emitting surface. The LED's have a large area P-N junction diffused into the epitaxial layer on a GaP transparent substrate.

The anode and cathode of each LED is brought out by separate pins. This universal pinout arrangement allows for the wiring of the LED's within a device in any of three possible configurations: parallel, series, or series/parallel.

These light bar devices are designed for strobed operation at high peak currents. The typical forward voltage values, scaled from Figure 4, should be used for calculating the current limiting resistor values and typical power dissipation. Expected maximum V_F values for the purpose of driver circuit design and maximum power dissipation may be calculated using the following V_F models:

$$V_F = 2.5V + I_{PEAK}\ (10\Omega)$$
$$\text{For } I_{PEAK} \geq 30mA$$
$$V_F = 2.3V + I_{DC}\ (15.7\Omega)$$
$$\text{For } 10mA \leq I_{DC} < 30mA$$

Temperature derated strobed operating conditions are obtained from Figures 1 and 2. Figure 1 relates pulse duration (t_p), refresh rate (f), and the ratio of maximum peak current to maximum dc current (I_{PEAK} MAX/I_{DC} MAX). Figure 2 presents the maximum allowed dc current vs. ambient temperature. To most effectively use Figures 1 and 2, perform the following steps:

1. Determine desired duty factor, DF.
   Example: DF = 1/6
2. Determine desired refresh rate, f. Use duty factor to calculate pulse duration, tp. Note: DF = f · tp.
   Example: f = 1 kHz, t_p = 167μs
3. Enter Figure 1 at the calculated t_p. Move vertically to the refresh rate line and record the corresponding value of I_{PEAK} MAX/I_{DC} MAX.
   Example: At t_p = 167μs and f = 1 kHz, I_{PEAK} MAX/I_{DC} MAX = 4.3
4. From Figure 2, determine I_{DC} MAX. Note: I_{DC} MAX is derated above T_A = 50°C.
   Example: At T_A = 65°C, I_{DC} MAX = 22.5mA
5. Calculate I_{PEAK} MAX from I_{PEAK} MAX/I_{DC} MAX ratio and calculate I_{AVG} from I_{PEAK} MAX and DF.
   Example: I_{PEAK} MAX = (4.3)(22.5mA) = 96.8mA PEAK
   · I_{AVG} = (1/6)(96.8mA) = 16.1mA AVG

The above calculations determine the maximum allowed strobing conditions. Operation at a reduced peak current and/or pulse width may be desirable to adjust display light output to match ambient light level or to reduce power dissipation to insure even more reliable operation.

Refresh rates of 1 kHz or faster provide the most efficient operation resulting in the maximum possible time average luminous intensity.

The time average luminous intensity may be calculated using the relative efficiency characteristic of Figure 3, $\eta_{I_{PEAK}}$, and adjusted for operating ambient temperature. The time average luminous intensity at T_A = 25°C is calculated as follows:

$$I_{V\ TIME\ AVG} = \left[\frac{I_{AVG}}{20mA}\right] [\eta_{I_{PEAK}}]\ [I_V \text{ Data Sheet}]$$

Example: For HLMP-2450 series

$$\eta_{I_{PEAK}} = 1.67 \text{ at } I_{PEAK} = 96.8mA$$

$$I_{V\ TIME\ AVG} = \left[\frac{16.1mA}{20mA}\right] [1.67]\ [18mcd] = 24mcd$$

The time average luminous intensity may be adjusted for operating ambient temperature by the following exponential equation:

$$I_V(T_A) = I_V(25°C)\, e^{[K\ (T_A - 25°C)]}$$

DEVICE	K
-2300 Series	−0.0131/°C
-2400 Series	−0.0112/°C
-2500 Series	−0.0104/°C

Example: I_V (65°C) = (24mcd) $e^{[-0.0112\ (65-25)]}$ = 15mcd

Mechanical

These devices are constructed utilizing a lead frame in a single in-line pin, SIP, package. The LED dice are attached directly to the lead frame. Therefore, the cathode leads are the direct thermal and mechanical stress paths to the LED dice. The absolute maximum allowed junction temperature, T_J MAX, is 100°C. The maximum power ratings have been established so that the worst case V_F device does not exceed this limit. For most reliable operation, it is recommended that the device pin-to-ambient thermal resistance through the PC board be less than 425°C/W/LED. This will then establish a maximum thermal resistance LED junction-to-ambient of 575°C/W/LED.

These light bar devices may be operated in ambient temperatures above +50°C without derating when installed in a PC board configuration that provides a thermal resistance to ambient value less than 425°C/W/LED. See Figure 6 to determine the maximum allowed thermal resistance for the PC board, $R_{\theta PC\text{-}A}$, which will permit nonderated operation in a given ambient temperature.

To optimize device optical performance, specially developed plastics are used which restrict the solvents that may be used for cleaning. It is recommended that only mixtures of Freon (F113) and alcohol be used for vapor cleaning processes, with an immersion time in the vapors of less than two (2) minutes maximum. Some suggested vapor cleaning solvents are Freon TE, Genesolv DI-15 or DE-15, Arklone A or K. A 60°C (140°F) water cleaning process may also be used, which includes a neutralizer rinse (3% ammonia solution or equivalent), a surfactant rinse (1% detergent solution or equivalent), a hot water rinse and a thorough air dry. Room temperature cleaning may be accomplished with Freon T-E35 or T-P35, Ethanol, Isopropanol or water with a mild detergent.

Optical

The radiation pattern for these light bar devices is approximately Lambertian. The luminous sterance may be calculated using one of the two following formulas:

$$L_V(cd/m^2) = \frac{I_V(cd)}{A(m^2)}$$

$$L_V(footlamberts) = \frac{\pi I_V(cd)}{A(ft^2)}$$

SIZE OF EMITTING SURFACE	AREA	
	SQ. METRES	SQ. FEET
8.89mm x 3.81mm	33.87×10^{-6}	364.58×10^{-6}
19.05mm x 3.81mm	72.58×10^{-6}	781.25×10^{-6}

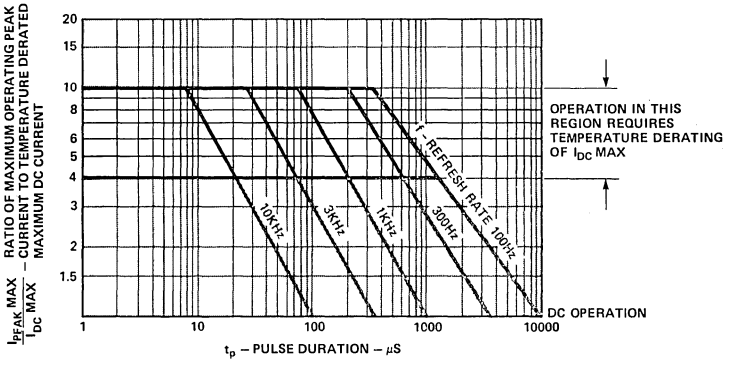


Figure 1. Maximum Allowed Peak Current vs. Pulse Duration

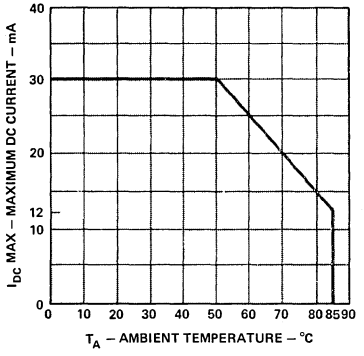


Figure 2. Maximum Allowable DC Current Per LED vs. Ambient Temperature.

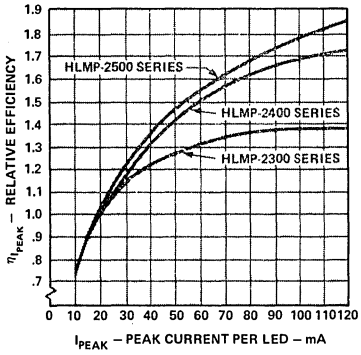


Figure 3. Relative Efficiency (Luminous Intensity Per Unit Current) vs. Peak LED Current.

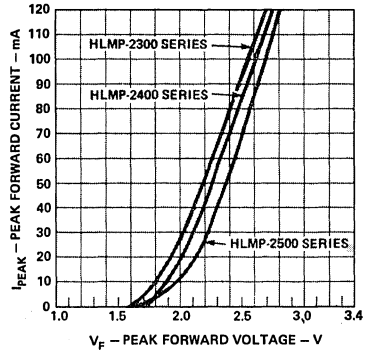


Figure 4. Peak Forward Current Per LED vs. Peak Forward Voltage.

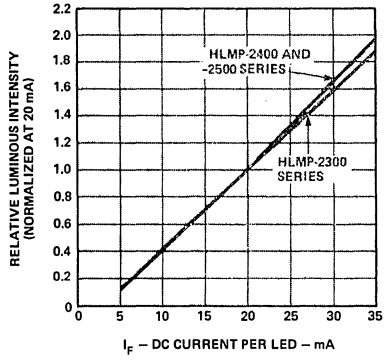


Figure 5. Relative Luminous Intensity vs. DC Forward Current.

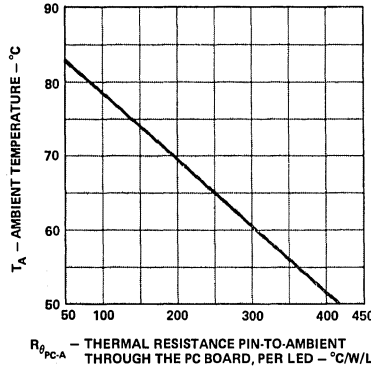


Figure 6. Maximum Operating Ambient Temperature vs. Thermal Resistance to Ambient Through the PC Board, for Device Operation without Derating Forward Current.

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COMPONENTS

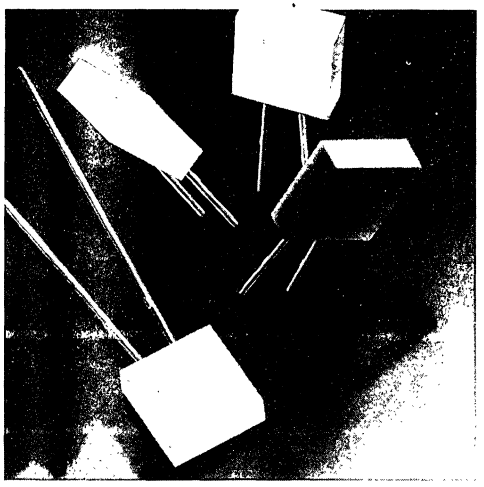
RECTANGULAR SOLID STATE LAMPS

HIGH EFFICIENCY RED HLMP-0300/0301 (5082-4670)
YELLOW HLMP-0400/0401 (5082-4570)
GREEN HLMP-0500/0501 (5082-4970)

TECHNICAL DATA APRIL 1979

Features

- **RECTANGULAR LIGHT EMITTING SURFACE**
- **FLAT HIGH STERANCE EMITTING SURFACE**
- **STACKABLE ON 2.54 MM (0.100 INCH) CENTERS**
- **IDEAL AS FLUSH MOUNTED PANEL INDICATORS**
- **IDEAL FOR BACKLIGHTING LEGENDS**
- **LONG LIFE: SOLID STATE RELIABILITY**
- **CHOICE OF 3 BRIGHT COLORS**
  - **HIGH EFFICIENCY RED**
  - **YELLOW**
  - **GREEN**
- **IC COMPATIBLE/LOW CURRENT REQUIREMENTS**



Description

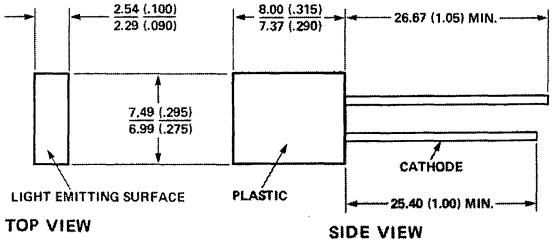
The HLMP-03XX, -04XX, -05XX are solid state lamps encapsulated in an axial lead rectangular epoxy package. They utilize a tinted, diffused epoxy to provide high on-off contrast and a flat high intensity emitting surface. Borderless package design allows creation of uninterrupted light emitting areas.

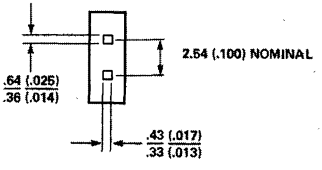
The HLMP-0300 and -0301 have a high-efficiency red GaAsP on GaP LED chip in a light red epoxy package. This lamp's efficiency is comparable to that of the Gap red, but extends to higher current levels.

The HLMP-0400 and -0401 provide a yellow GaAsP on GaP LED chip in a yellow epoxy package.

The HLMP-0500 and -0501 provide a green GaP LED chip in a green epoxy package.

Package Dimensions





NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER-PLATED LEADS. SEE APPLICATION BULLETIN 3.
3. AN EPOXY MINISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

AXIAL LUMINOUS INTENSITY

		MIN.	TYP.	TEST CONDITIONS
HER	HLMP-0300	.8	1.0 mcd	I_F = 25mA
	HLMP-0301	1.5	2.5 mcd	I_F = 25mA
	(5082-4670)	.8	1.5 mcd	I_F = 15mA
YELLOW	HLMP-0400	1.0	1.2 mcd	I_F = 25mA
	HLMP-0401	2.0	2.5 mcd	I_F = 25mA
	(5082-4570)	1.0	1.5 mcd	I_F = 15mA
GREEN	HLMP-0500	1.0	1.2 mcd	I_F = 25mA
	HLMP-0501	1.5	2.5 mcd	I_F = 25mA
	(5082-4970)	1.0	1.5 mcd	I_F = 20mA

NOTE: Luminous sterance, L_V, in foot lamberts, may be found from the equation $L_V = 16.7\ I_V$, where I_V is the luminous intensity in millicandelas.

Absolute Maximum Ratings at T_A=25°C

Parameter	High-Efficiency Red HLMP-0300/0301	Yellow HLMP-0400/0401	Green HLMP-0500/0501	Units
Power Dissipation	120	120	120	mW
Average Forward Current	30 [1]	30 [1]	30 [1]	mA
Peak Forward Current	60 See Figure 5	60 See Figure 10	60 See Figure 15	mA
Operating and Storage Temperature Range	-55°C to 100°C			
Lead Soldering Temperature [1.6mm (0.063 in.) from body]	260°C for 5 seconds			

1. Derate from 50°C at 0.4mA/°C.

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	HLMP-0300/0301			HLMP-0400/0401			HLMP-0500/0501			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points, Both Axes		100			100			100		deg.	Note 1. Figures 6,11,16
λ_{PEAK}	Peak Wavelength		635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		626			585			571		nm	Note 2
τ_S	Speed of Response		90			90			200		ns	
C	Capacitance		17			17			17		pF	V_F=0; f=1 MHz
Θ_{JC}	Thermal Resistance		130			130			130		°C/W	Junction to Cathode Lead at 1.6 mm (0.063 in.) from Body
V_F	Forward Voltage		2.5	3.0		2.5	3.0		2.5	3.0	V	I_F= 25mA Figures 2,7,12
BV_R	Reverse Breakdown Voltage	5.0			5.0			5.0			V	I_R = 100 μA
η_v	Luminous Efficacy		147			570			665		lm/W	Note 3

NOTES:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e=I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

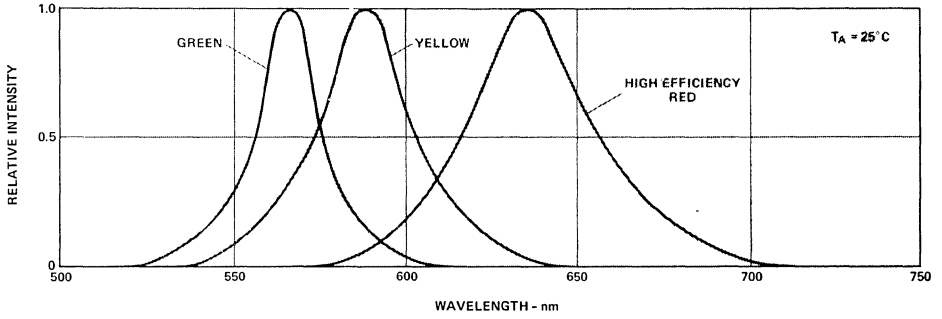


Figure 1. Relative Intensity vs. Wavelength.

HIGH EFFICIENCY RED HLMP-0300/0301 (5082-4670)

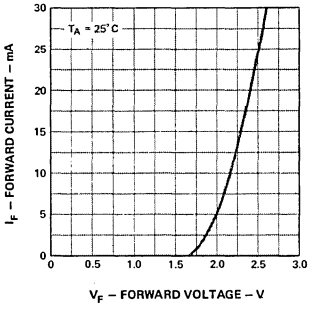


Figure 2. Forward Current vs. Forward Voltage.

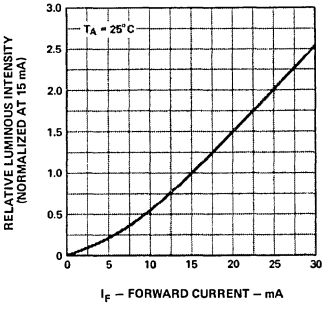


Figure 3. Relative Luminous Intensity vs. Forward Current.

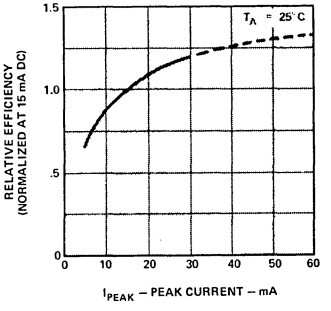


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

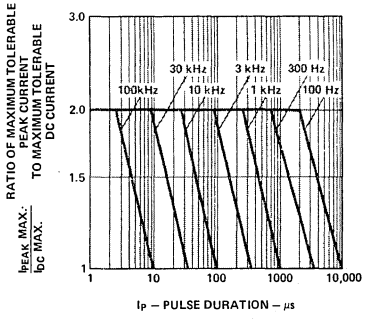


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

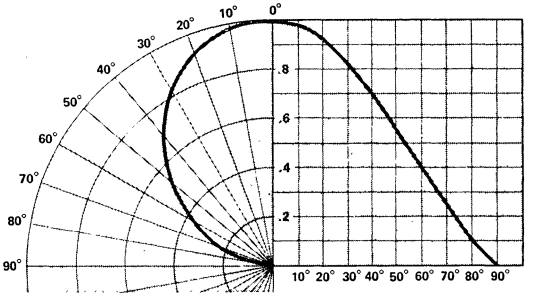


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

YELLOW HLMP-0400/0401 (5082-4570)

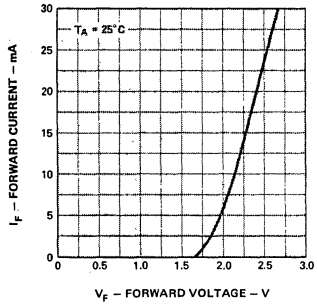


Figure 7. Forward Current vs. Forward Voltage.

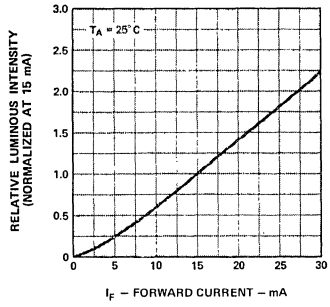


Figure 8. Relative Luminous Intensity vs. Forward Current.

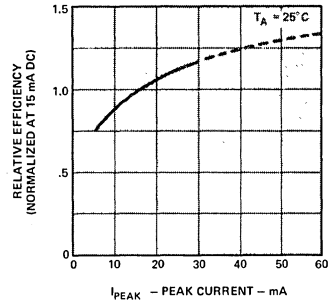


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

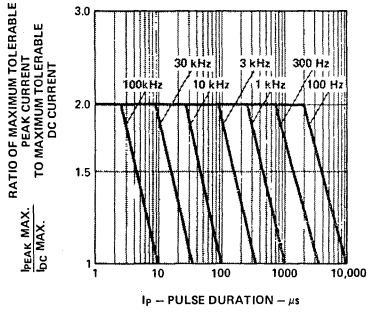


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

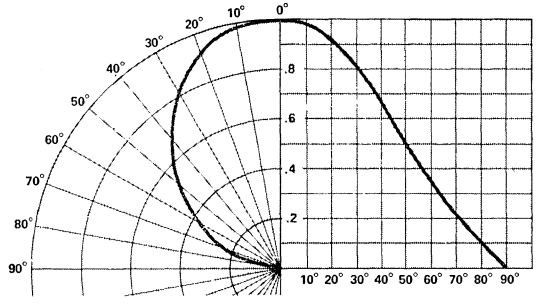


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

GREEN HLMP-0500/0501 (5082-4970)

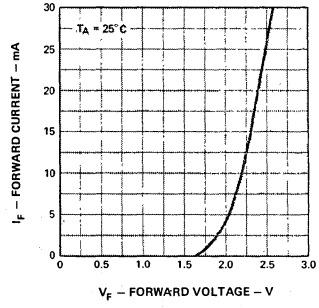


Figure 12. Forward Current vs. Forward Voltage.

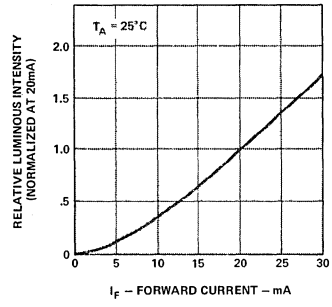


Figure 13. Relative Luminous Intensity vs. Forward Current.

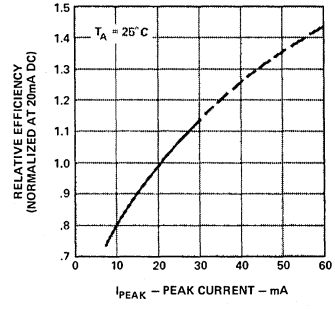


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

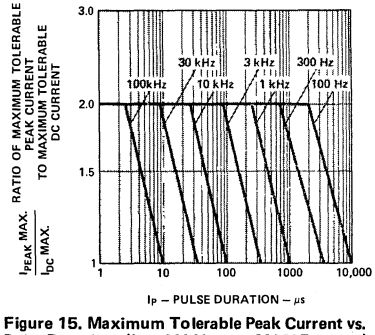


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

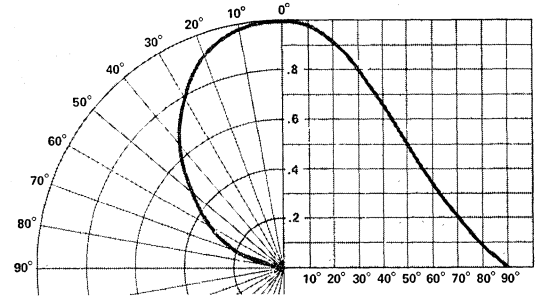


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT hp PACKARD

COMPONENTS

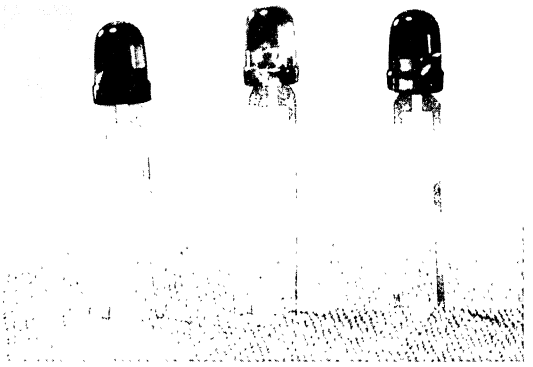
SOLID STATE LAMPS

HIGH EFFICIENCY RED • HLMP-1300,-1301(5082-4684),-1302
YELLOW • HLMP-1400,-1401(5082-4584),-1402
GREEN • HLMP-1500,-1501(5082-4984),-1502

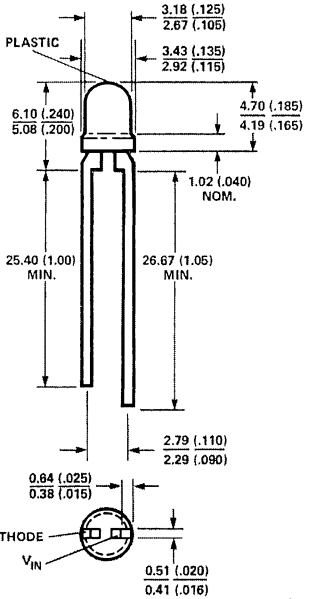
TECHNICAL DATA APRIL 1979

Features

- HIGH INTENSITY
- WIDE VIEWING ANGLE
- SMALL SIZE T-1 DIAMETER 3.18mm (0.125 inch)
- IC COMPATIBLE
- RELIABLE AND RUGGED
- CHOICE OF 3 BRIGHT COLORS
  - HIGH EFFICIENCY RED
  - YELLOW
  - GREEN



Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATIONS BULLETIN 3.
3. AN EPOXY MINISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Description

The HLMP-1300, -1301, and -1302 have a Gallium Arsenide Phosphide on Gallium Phosphide High Efficiency Red Light Emitting Diode packaged in a T-1 outline with a red diffused lens, which provides excellent on-off contrast ratio, high axial luminous intensity and a wide viewing angle.

The HLMP-1400, -1401, and -1402 have a Gallium Arsenide Phosphide on Gallium Phosphide Yellow Light Emitting Diode packaged in a T-1 outline with a yellow diffused lens, which provides good on-off contrast ratio, high axial luminous intensity and a wide viewing angle.

The HLMP-1500, -1501, and -1502 have a Gallium Phosphide Green Light Emitting Diode packaged in a T-1 outline with a green diffused lens, which provides good on-off contrast ratio, high axial luminous intensity, and a wide viewing angle.

I_V — Axial Luminous Intensity at 25°C (Figures 3,8,15)

	I_V (mcd)		
	Min.	Typ.	Test Conditions
High Efficiency Red			
HLMP-1300	0.5	1.5	
HLMP-1301 (-4684)	1.0	2.0	I_F=10 mA
HLMP-1302	2.0	2.5	
Yellow			
HLMP-1400	0.5	1.5	
HLMP-1401 (-4584)	1.0	2.5	I_F=10 mA
HLMP-1402	2.5	4.0	
Green			
HLMP-1500	0.5	1.2	
HLMP-1501 (-4984)	0.8	2.0	I_F=20 mA
HLMP-1502	2.0	3.0	

Absolute Maximum Ratings at T_A=25°C

Parameter	High Efficiency Red HLMP-1300,1301,1302	Yellow HLMP-1400,1401,1402	Green HLMP-1500,1501,1502	Units
Power Dissipation	120	120	120	mW
Average Forward Current	20[1]	20[1]	30[2]	mA
Peak Forward Current	60 See Figure 5	60 See Figure 10	60 See Figure 15	mA
Operating and Storage Temperature Range	-55°C to 100°C			
Lead Soldering Temperature [1.6mm (0.063 in.) from Body]	230°C for 7 Seconds			

1. Derate from 50° C at 0.2mA/° C
2. Derate from 50° C at 0.4mA/° C

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	HLMP-1300,-1301, -1302			HLMP-1400,-1401, -1402			HLMP-1500,-1501, -1502			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		70			60			60		Deg.	Note 1 (Figs. 6, 11, 16)
λ_{peak}	Peak Wavelength		635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		628			585			572		nm	Note 2
τ_s	Speed of Response		90			90			200		ns	
C	Capacitance		20			15			8		pF	V_F=0; f=1 MHz
Θ_{JC}	Thermal Resistance		95			95			95		°C/W	Junction to Cathode Lead at 0.79mm (0.031 in.) From Body
V_F	Forward Voltage		2.2	3.0		2.2	3.0		2.4 at I_F = 20mA	3.0	V	I_F=10mA (Figs. 2,7,12)
BV_R	Reverse Breakdown Voltage	5.0			5.0			5.0			V	I_R=100μA
η_v	Luminous Efficacy		147			570			665		lm/W	Note 3

1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e=I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

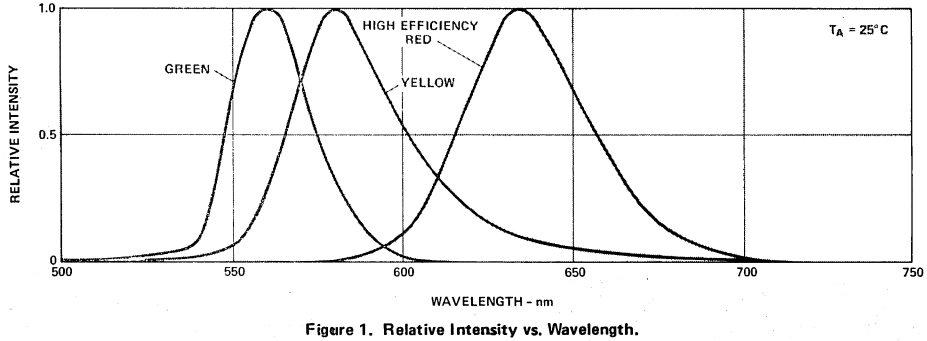


Figure 1. Relative Intensity vs. Wavelength.

High Efficiency Red HLMP-1300,-1301(5082-4684),-1302

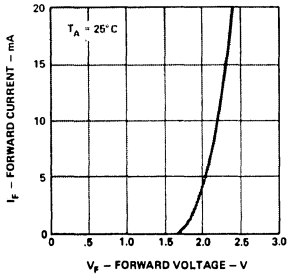


Figure 2. Forward Current vs. Forward Voltage.

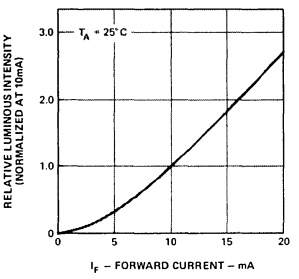


Figure 3. Relative Luminous Intensity vs. Forward Current.

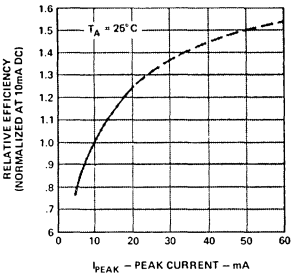


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

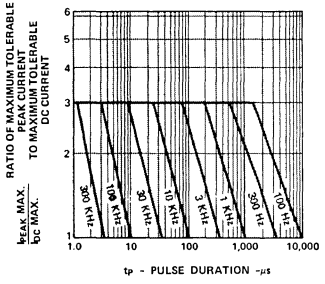


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC}MAX as per MAX Ratings).

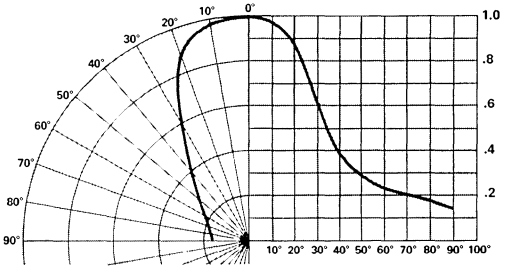


Figure 6. Rolative Luminous Intensity vs. Angular Displacement.

Yellow HLMP-1400,-1401(5082-4584),-1402

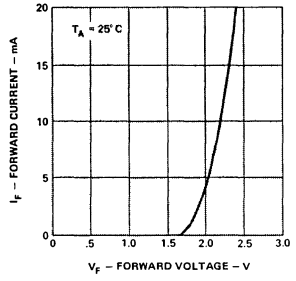


Figure 7. Forward Current vs. Forward Voltage.

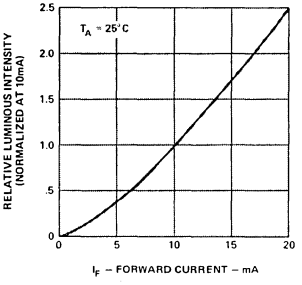


Figure 8. Relative Luminous Intensity vs. Forward Current.

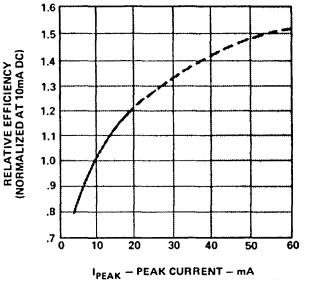


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

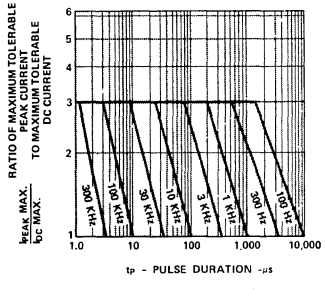


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

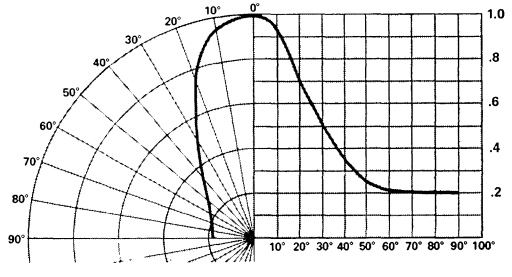


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

SOLID STATE LAMPS

Green HLMP-1500,-1501 (5082-4984),-1502

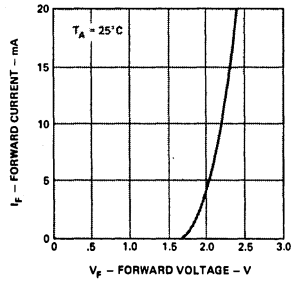


Figure 12. Forward Current vs. Forward Voltage.

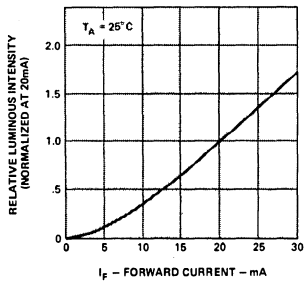


Figure 13. Relative Luminous Intensity vs. Forward Current.

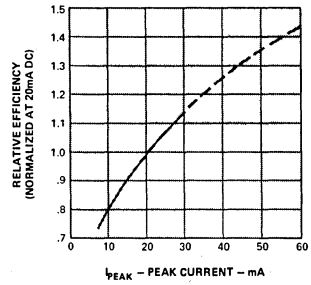


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

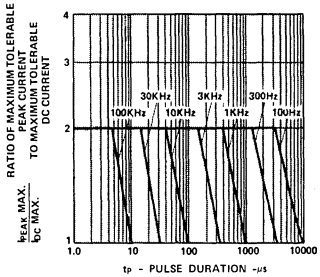


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

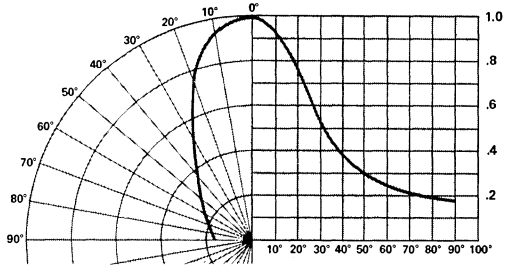


Figure 16. Relative Luminious Intensity vs. Angular Displacement.

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COMPONENTS

SOLID STATE LAMPS

5082-4403
5082-4415
5082-4440
5082-4444
5082-4880 SERIES

TECHNICAL DATA APRIL 1979

Features

- **EASILY PANEL MOUNTABLE**
- **HIGH BRIGHTNESS OVER A WIDE VIEWING ANGLE**
- **RUGGED CONSTRUCTION FOR EASE OF HANDLING**
- **STURDY LEADS ON 25.4mm (0.10 in.) CENTERS**
- **IC COMPATIBLE/LOW POWER CONSUMPTION**
- **LONG LIFE**

Description

The 5082-4403, -4415, -4440, -4444 and the -4880 series are plastic encapsulated Gallium Arsenide Phosphide Light Emitting Diodes. They radiate light in the 655 nanometer (red light) region.

The 5082-4403 and -4440 are LEDs with a red diffused plastic lens, providing high visibility for circuit board or panel mounting with a clip.

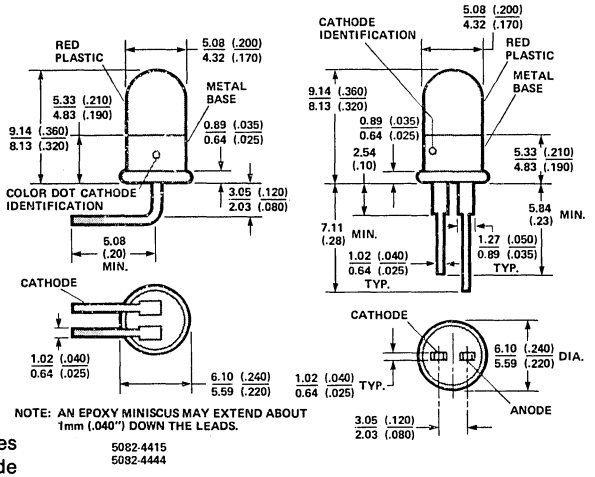
The 5082-4415 and -4444 have the added feature of a 90° lead bend for edge mounting on circuit boards.

The 5082-4880 series is available in three different lens configurations. These are Red Diffused, Clear Diffused, and Clear Non-Diffused.

The Red Diffused lens provides an excellent off/on contrast ratio. The Clear Non-Diffused lens is designed for applications where a point source is desired. It is particularly useful where the light must be focused or diffused with external optics. The Clear Diffused lens is useful in masking the red color in the off condition.

LED SELECTION GUIDE

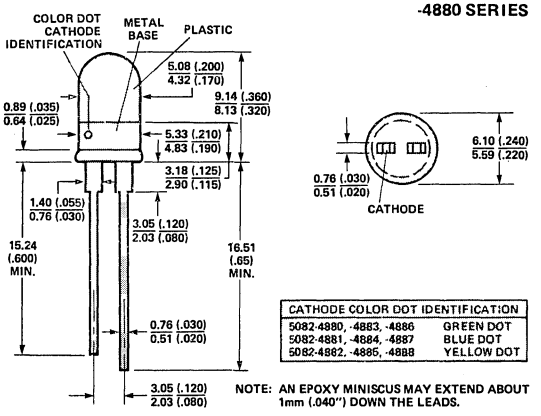
MINIMUM LIGHT OUTPUT (mcd)	LONG LEAD (UNBENT)		
	Red Diffused Lens	Clear Non-Diffused Lens	Clear Diffused Lens
0.5	5082-4880	5082-4883	5082-4886
1.0	5082-4881	5082-4884	5082-4887
1.6	5082-4882	5082-4885	5082-4888
	SHORT LEAD		
0.3	5082-4440	UNBENT	
0.8	5082-4403		
0.3	5082-4444	BENT	
0.8	5082-4415		



CATHODE COLOR DOT IDENTIFICATION	
5082-4403	WHITE DOT
5082-4440	ORANGE DOT
5082-4415	WHITE DOT
5082-4444	ORANGE DOT

DIMENSIONS IN MILLIMETRES AND (INCHES).

-4880 SERIES



CATHODE COLOR DOT IDENTIFICATION	
5082-4880, -4883, -4886	GREEN DOT
5082-4881, -4884, -4887	BLUE DOT
5082-4882, -4885, -4888	YELLOW DOT

NOTE: AN EPOXY MINISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Maximum Ratings at T_A=25°C

DC Power Dissipation ..... 100 mW
DC Forward Current ..... 50 mA
(Derate linearly from 50° C at 0.2mA/° C)
Peak Transient Forward Current ..... 1 Amp
(1μsec pulse width, 300 pps)
Isolation Voltage (between lead and base) ..... 300 V
Operating and Storage
Temperature Range .....-55° C to +100° C
Lead Soldering Temperature ..... 230° C for 7 sec

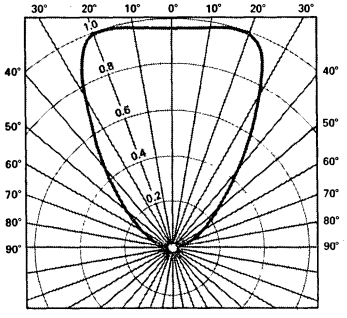
SOLID STATE LAMPS

Electrical Characteristics at $T_A = 25°C$

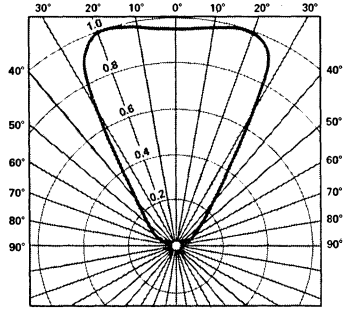
Symbol	Parameter	5082-4403 5082-4415			5082-4440 5082-4444			5082-4880 5082-4883 5082-4886			5082-4881 5082-4884 5082-4887			5082-4882 5082-4885 5082-4888			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Luminous Intensity	0.8	1.2		0.3	0.7		0.5	0.8		1.0	1.3		1.6	1.8		mcd	I_F = 20mA
λ_{PEAK}	Wavelength		655			655			655			655			655		nm	Measurement at Peak
τ_s	Speed of Response		15			15			15			15			15		ns	
C	Capacitance		100			100			100			100			100		pF	
θ_{JC}	Thermal Resistance		87			87			100			100			100		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.6	2.0		1.6	2.0		1.6	2.0		1.6	2.0		1.6	2.0	V	I_F = 20mA
BV_R	Reverse Breakdown Voltage	3	10		3	10		3	10		3	10		3	10		V	I_R = 100μA

TYPICAL RELATIVE LUMINOUS INTENSITY VERSUS ANGULAR DISPLACEMENT

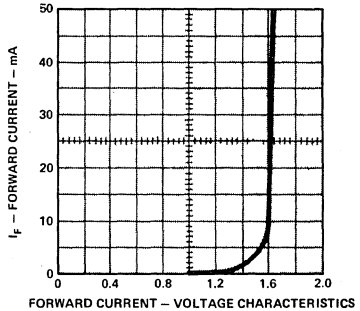
44XX



4880, 4881, 4882

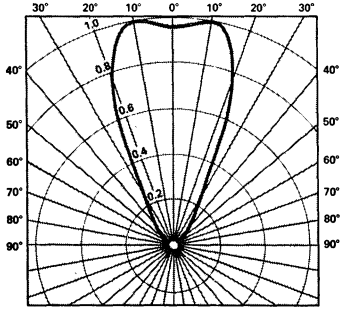


FORWARD CURRENT VS. VOLTAGE CHARACTERISTICS

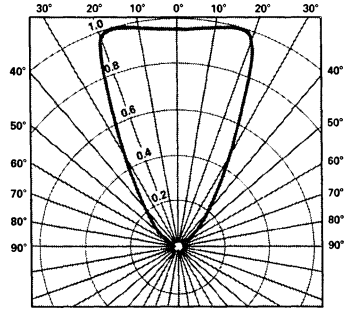


FORWARD CURRENT – VOLTAGE CHARACTERISTICS

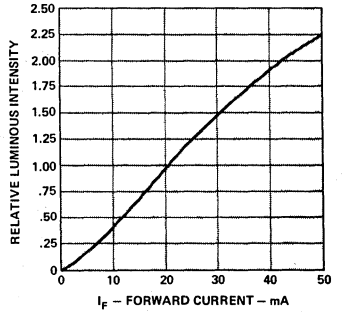
4883, 4884, 4885



4886, 4887, 4888



LUMINOUS INTENSITY VS. FORWARD CURRENT (I_F)



HEWLETT hp PACKARD
COMPONENTS

SOLID STATE LAMPS

5082-4480
SERIES

TECHNICAL DATA APRIL 1979

Features

- **HIGH INTENSITY: 0.8mcd TYPICAL**
- **WIDE VIEWING ANGLE**
- **SMALL SIZE T-1 DIAMETER 3.18mm (0.125")**
- **IC COMPATIBLE**
- **RELIABLE AND RUGGED**

Description

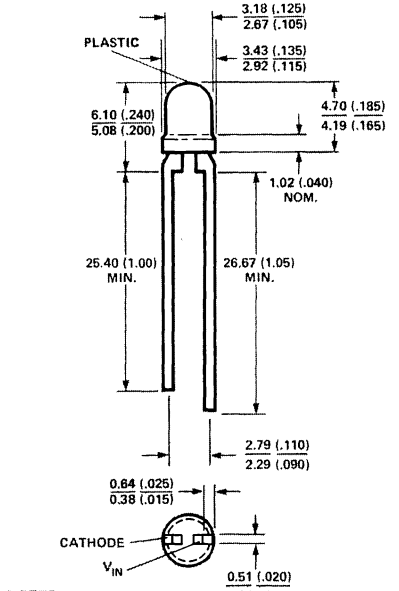
The 5082-4480 is a series of Gallium Arsenide Phosphide Light Emitting Diodes designed for applications where space is at a premium, such as in high density arrays.

The 5082-4480 series is available in three lens configurations.

5082-4480 — Red Diffused lens provides excellent on-off contrast ratio, high axial luminous intensity, and wide viewing angle.

5082-4483 — Same as 5082-4480, but Clear Diffused to mask red color in the "off" condition.

5082-4486 — Clear Non-Diffused plastic lens provides a point source. Useful when illuminating external lens, annunciators, or photo-detectors.



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATIONS BULLETIN 3.
3. AN EPOXY MINISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

PART NO.	LENS CONFIGURATION
5082-4480	Red Diffused
5082-4483	Untinted Diffused
5082-4486	Clear Plastic

Maximum Ratings at T_A=25°C

DC Power Dissipation 100mW

DC Forward Current 50mA
(Derate linearly from 50°C at 0.2mA/°C)

Peak Forward Current . . . . . 1 Amp
(1 μsec pulse width, 300 pps)

Operating and Storage
Temperature Range . . . . . –55°C to +100°C

Lead Soldering Temperature . . . . . 230°C for 7 sec.

Electrical Characteristics at T_A=25°C

Symbol	Parameters	5082-4480 5082-4483 5082-4486			Units	Test Conditions
		Min.	Typ.	Max.		
I_V	Luminous Intensity	0.3	0.8		mcd	I_F = 20mA
λ_{PEAK}	Wavelength		655		nm	Measurement at Peak
τ_s	Speed of Response		15		ns	
C	Capacitance		100		pF	V_F = 0, f = 1MHz
θ_{JC}	Thermal Resistance		270		°C/W	Junction to Cathode Lead
V_F	Forward Voltage		1.6	2.0	V	I_F = 20mA
BV_R	Reverse Breakdown Voltage	3	10		V	I_R = 10μA

SOLID STATE LAMPS

5082-4480 AND 5082-4483

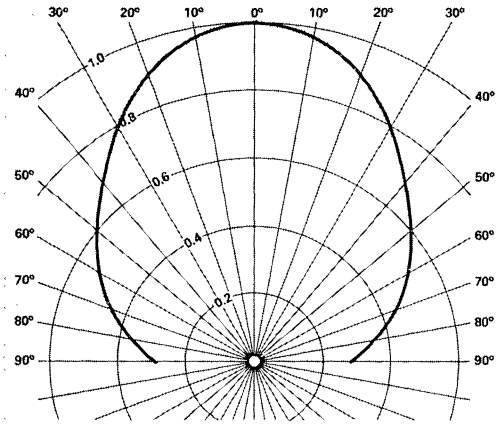


Figure 1. Relative Luminous Intensity vs. Angular Displacement.

5082-4486

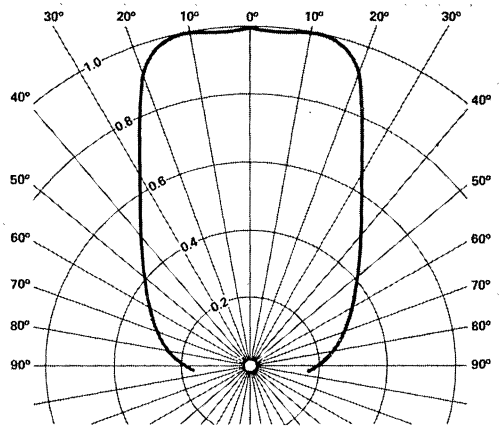


Figure 2. Relative Luminous Intensity vs. Angular Displacement.

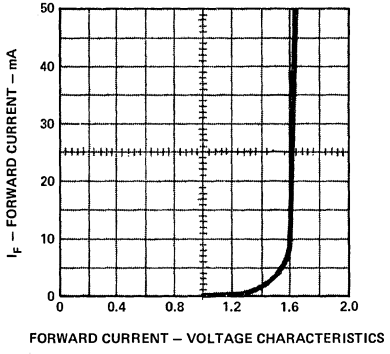


Figure 3. Forward Current vs. Voltage Characteristic.

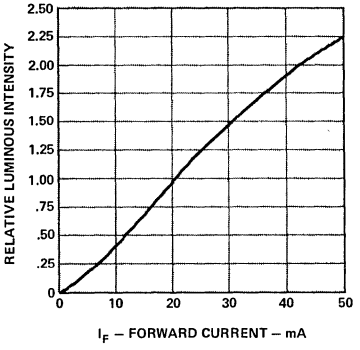


Figure 4. Luminous Intensity vs. Forward Current (I_F).

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COMPONENTS

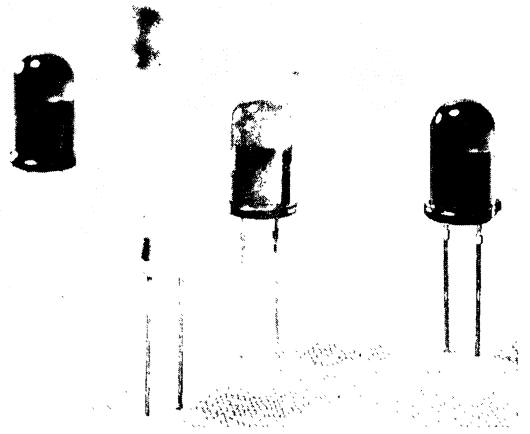
SOLID STATE LAMPS

HIGH EFFICIENCY RED · 5082-4650 Series
YELLOW · 5082-4550 Series
GREEN · 5082-4950 Series

TECHNICAL DATA APRIL 1979

Features

- **HIGH INTENSITY**
- **CHOICE OF 3 BRIGHT COLORS**
  - **High Efficiency Red**
  - **Yellow**
  - **Green**
- **POPULAR T-1¾ DIAMETER PACKAGE**
- **LIGHT OUTPUT CATEGORIES**
- **WIDE VIEWING ANGLE AND NARROW VIEWING ANGLE TYPES**
- **GENERAL PURPOSE LEADS**
- **IC COMPATIBLE/LOW CURRENT REQUIREMENTS**
- **RELIABLE AND RUGGED**

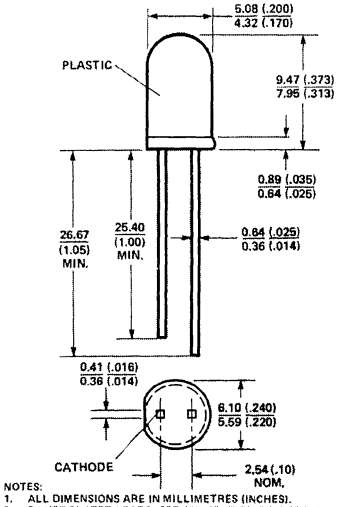


Description

The 5082-4650 and the 5082-4550 Series lamps are Gallium Arsenide Phosphide on Gallium Phosphide diodes emitting red and yellow light respectively. The 5082-4950 Series lamps are green light emitting Gallium Phosphide diodes.

General purpose and selected brightness versions of both the diffused and non-diffused lens type are available in each family.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATION BULLETIN 3.
3. AN EPOXY MINISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Part Number 5082-	Application	Lens	Color
4650	Indicator — General Purpose	Diffused	High Efficiency Red
4655	Indicator — High Ambient	Wide Angle	
4657	Illuminator/Point Source	Non Diffused	
4658	Illuminator/High Brightness	Narrow Angle	
4550	Indicator General Purpose	Diffused	Yellow
4555	Indicator — High Ambient	Wide Angle	
4557	Illuminator/Point Source	Non-Diffused	
4558	Illuminator/High Brightness	Narrow Angle	
4950	Indicator — General Purpose	Diffused	Green
4955	Indicator — High Ambient	Wide Angle	
4957	Illuminator/Point Source	Non-Diffused	
4958	Illuminator/High Brightness	Narrow Angle	

Electrical Characteristics at T_A=25°C

Symbol	Description	Device 5082-	Min.	Typ.	Max.	Units	Test Conditons
I_V	Luminous Intensity	4650	1.0	2.0		mcd.	I_F = 10mA (Fig. 3)
		4655	3.0	4.0			
		4657	9.0	12.0			
		4658	15.0	24.0			
		4550	1.0	1.8		mcd.	I_F = 10mA (Fig. 8)
		4555	2.2	3.0			
		4557	6.0	9.0			
		4558	12.0	16.0			
		4950	1.0	1.8		mcd.	I_F = 20mA (Fig. 13)
		4955	2.2	3.0			
		4957	6.0	9.0			
		4958	12.0	16.0			
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	4650		90		Deg.	I_F = 10mA See Note 1 (Fig. 6)
		4655		90			
		4657		35			
		4658		35			
		4550		90		Deg.	I_F = 10mA See Note 1 (Fig. 11)
		4555		90			
		4557		35			
		4558		35			
		4950		90		Deg.	I_F = 20mA See Note 1 (Fig. 16)
		4955		90			
		4957		30			
		4958		30			
λ_{PEAK}	Peak Wavelength	4650s		635		nm	Measurement at Peak (Fig. 1)
		4550s		583			
		4950s		565			
λ_d	Dominant Wavelength	4650s		626		nm	See Note 2 (Fig.1)
		4550s		585			
		4950s		572			
τ_S	Speed of Response	4650s		90		ns	
		4550s		90			
		4950s		200			
C	Capacitance	4650s		16		pF	V_F = 0, f = 1 MHz
		4550s		18			
		4950s		18			
Θ_{JC}	Thermal Resistance	4650s		135		°C/W	Junction to Cathode Lead at Seating Plane
		4550s		135			
		4950s		145			
V_F	Forward Voltage	4650s		2.2	3.0	V	I_F = 10mA (Fig. 2,
		4550s		2.2	3.0		I_F = 10mA Fig. 7,
		4950s		2.4	3.0		I_F = 20mA Fig. 12)
BV_R	Reverse Breakdown Volt.	All	5.0			V	I_R = 100μA
η_V	Luminous Efficacy	4650s		147		lumens/watt	See Note 3
		4550s		570			
		4950s		665			

NOTES:

1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

Absolute Maximum Ratings at T_A=25°C

Parameter	High Efficiency Red 4650 Series	Yellow 4550 Series	Green 4950 Series	Units
Power Dissipation	120	120	120	mW
Average Forward Current	20[1]	20[1]	30[2]	mA
Peak Operating Forward Current	60 (Fig. 5)	60 (Fig. 10)	60 (Fig. 15)	mA
Operating and Storage Temperature Range	-55°C to +100°C			
Lead Solder Temperature (1.6mm[0.063 inch] below package base)	260°C for 5 seconds			

1. Derate from 50° C at 0.2mA/° C
2. Derate from 50° C at 0.4mA/° C

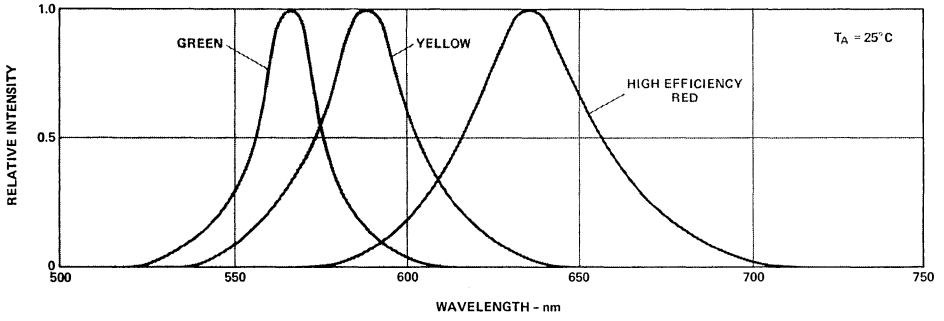


Figure 1. Relative Intensity vs. Wavelength.

High Efficiency Red 5082-4650 Series

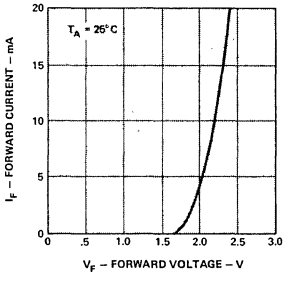


Figure 2. Forward Current vs. Forward Voltage

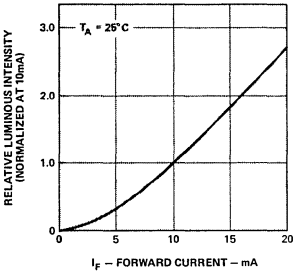


Figure 3. Relative Luminous Intensity vs. Forward Current.

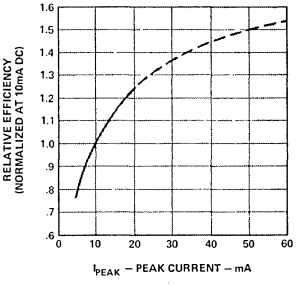


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

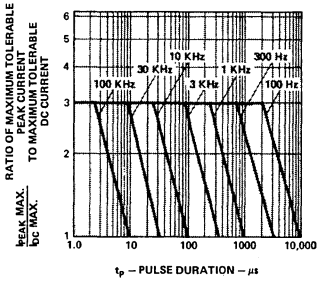


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings.)

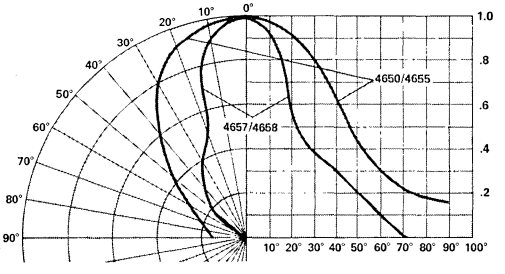


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

Yellow 5082-4550 Series

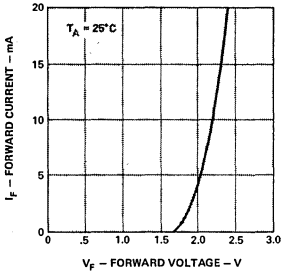


Figure 7. Forward Current vs. Forward Voltage.

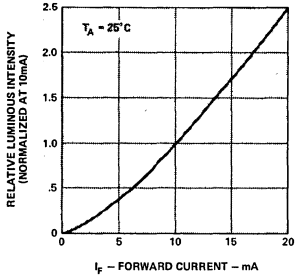


Figure 8. Relative Luminous Intensity vs. Forward Current.

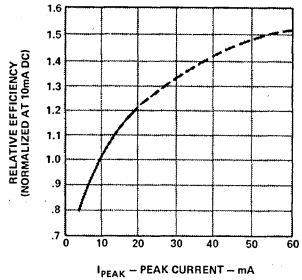


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

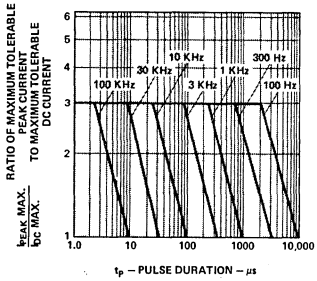


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

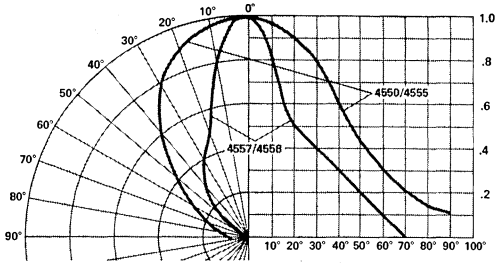


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

Green 5082-4950 Series

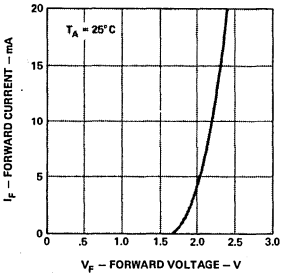


Figure 12. Forward Current vs. Forward Voltage.

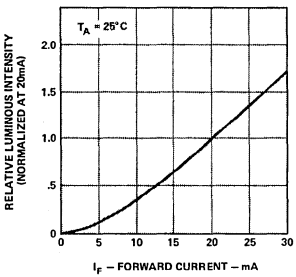


Figure 13. Relative Luminous Intensity vs. Forward Current.

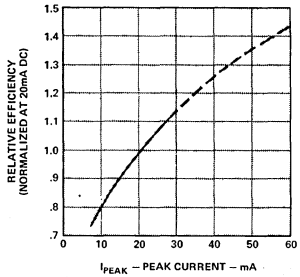


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

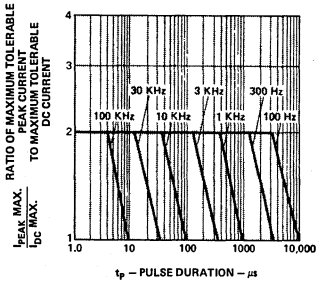


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

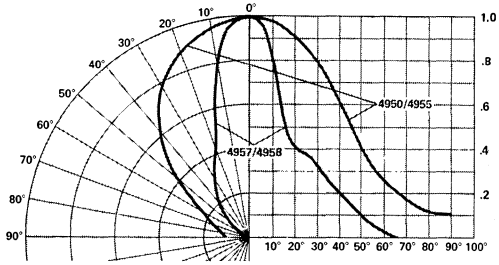


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT hp PACKARD

COMPONENTS

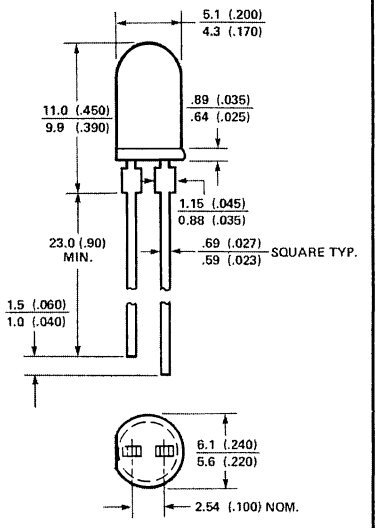
COMMERCIAL LIGHT EMITTING DIODES

5082-4850
5082-4855
5082-4484
5082-4494

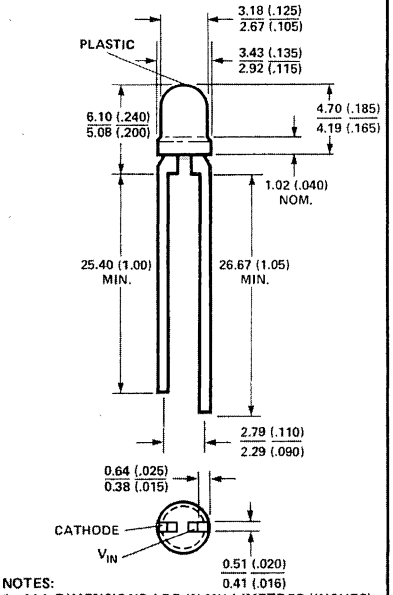
TECHNICAL DATA APRIL 1979

SOLID STATE LAMPS

5082-4850/4855



5082-4484/4494



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATIONS BULLETIN 3.
3. AN EPOXY MINISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Features

- **LOW COST: BROAD APPLICATION**
- **LONG LIFE: SOLID STATE RELIABILITY**
- **LOW POWER REQUIREMENTS: 20mA @ 1.6V**
- **HIGH LIGHT OUTPUT**
  0.8 mcd TYPICAL FOR 5082-4850/4484
  1.4 mcd TYPICAL FOR 5082-4855/4494
- **WIDE VIEWING ANGLE**
- **RED DIFFUSED LENS**

Description

The 5082-4850/4855 and 5082-4484/4494 are Gallium Arsenide Phosphide Light Emitting Diodes intended for **High Volume/Low Cost** applications such as indicators for appliances, automobile instrument panels and many other commercial uses.

The 5082-4850/4855 are T-1¾ lamp size, have red diffused lenses and can be panel mounted using mounting clip 5082-4707.

The 5082-4484/4494 are T-1 lamp size, have red diffused lenses and are ideal where space is at a premium, such as high density arrays.

Absolute Maximum Ratings at T_A=25°C

Power Dissipation 100mW

DC Forward Current (Derate linearly from 50°C at 0.2mA/°C) 50mA

Peak Forward Current 1Amp
(1μsec pulse width, 300pps)

Operating and Storage Temperature Range ..... -55°C to +100°C

Lead Soldering Temperature ..... 230°C for 7 sec.

Electrical Characteristics at T_A=25°C

Symbol	Parameters	5082-4850			5082-4855			5082-4484			5082-4494			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Luminous Intensity		0.8		0.8	1.4			0.8		0.8	1.4		mcd	I_F = 20mA
λ_{PEAK}	Wavelength		655			655			655			655		nm	Measurement at Peak
τ_s	Speed of Response		10			10			10			10		ns	
C	Capacitance		100			100			100			100		pF	V_F = 0, f = 1MHz
V_F	Forward Voltage		1.6	2.0		1.6	2.0		1.6	2.0		1.6	2.0	V	I_F = 20mA
BV_R	Reverse Breakdown Voltage	3	10		3	10		3	10		3	10		V	I_R = 100μA
θ_{JC}	Thermal Resistance		100			100			100			100		°C/W	Junction to Cathode Lead

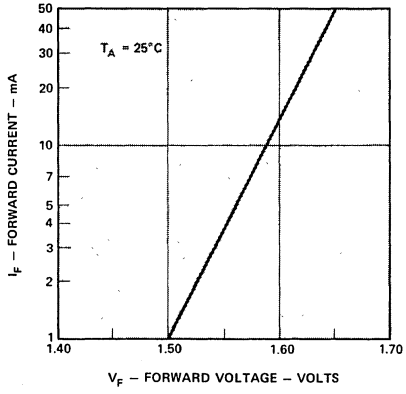


Figure 1. Forward Current Versus Forward Voltage Characteristic For 5082-4850/4855/4484/4494.

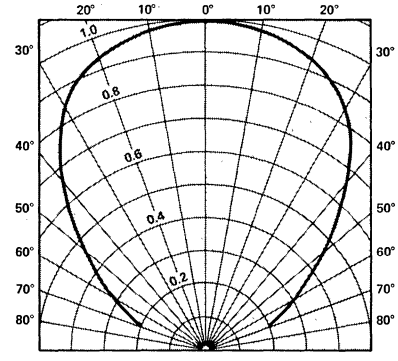


Figure 2. Relative Luminous Intensity Versus Angular Displacement For 5082-4850/4855.

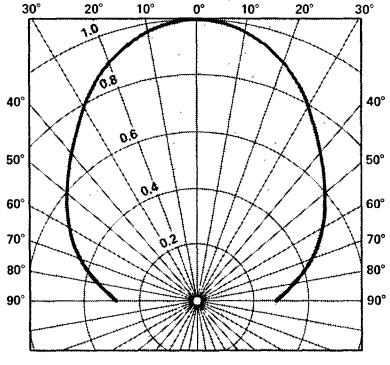


Figure 3. Relative Luminous Intensity Versus Angular Displacement For 5082-4484/4494.

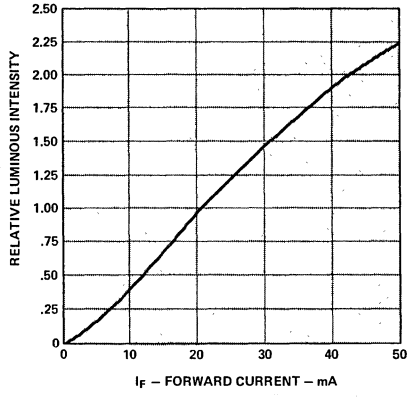


Figure 4. Relative Luminous Intensity Versus Forward Current For 5082-4850/4855/4484/4494.

HEWLETT hp PACKARD
COMPONENTS

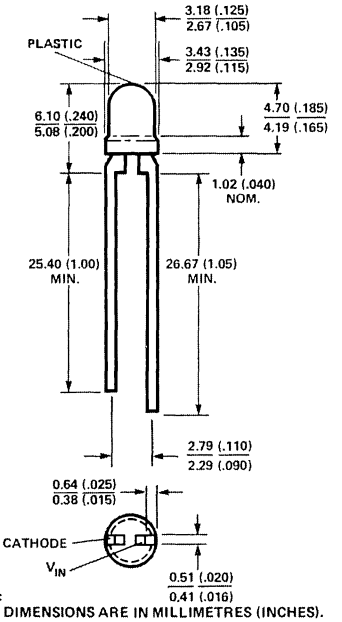
LOW PROFILE SOLID STATE LAMPS

5082-4487
5082-4488

TECHNICAL DATA APRIL 1979

Features

- **LOW COST: BROAD APPLICATION**
- **LOW PROFILE: 4.57mm (0.18") LENS HEIGHT TYPICAL**
- **HIGH DENSITY PACKAGING**
- **LONG LIFE: SOLID STATE RELIABILITY**
- **LOW POWER REQUIREMENTS: 20mA @ 1.6V**
- **HIGH LIGHT OUTPUT: 0.8mcd TYPICAL**



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATIONS BULLETIN 3.
3. AN EPOXY MINISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

Description

The 5082-4487 and 5082-4488 are Gallium Arsenide Phosphide Light Emitting Diodes for High Volume/ Low Cost Applications such as indicators for calculators, cameras, appliances, automobile instrument panels, and many other commercial uses.

The 5082-4487 is a clear non-diffused lens, low profile T-1 LED lamp, and has a typical light output of 0.8 mcd at 20 mA.

The 5082-4488 is a clear non-diffused, low profile T-1 LED lamp, and has a guaranteed minimum light output of 0.3 mcd at 20 mA.

Absolute Maximum Ratings at T_A=25°C

DC Power Dissipation	100mW
DC Forward Current [Derate linearly from 50°C at 0.2mA/°C]	50mW
Peak Forward Current [1 μsec pulse width, 300pps]	1 Amp
Operating and Storage Temperature Range	–55°C to +100°C
Lead Soldering Temperature	230°C for 7 sec.

SOLID STATE LAMPS

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameters	5082-4487			5082-4488			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Luminous Intensity		0.8		0.3	0.8		mcd	I_F = 20mA
λ_{PEAK}	Wavelength		655			655		nm	Measurement at Peak
τ_s	Speed of Response		10			10		ns	
C	Capacitance		100			100		pF	V_F = 0, f = 1MHz
V_F	Forward Voltage		1.6	2.0		1.6	2.0	V	I_F = 20mA
BV_R	Reverse Breakdown Voltage	3	10		3	10		V	I_R = 100μA

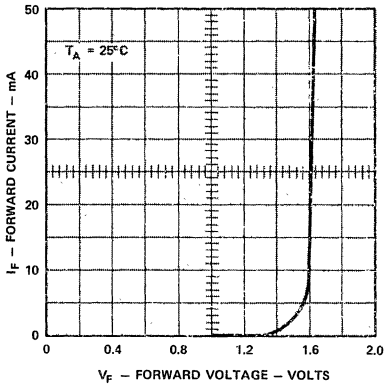


Figure 1. Typical Forward Current Versus Voltage Characteristic.

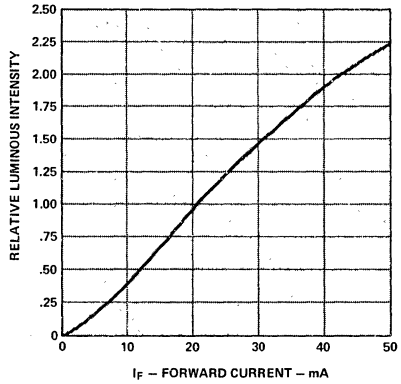


Figure 2. Typical Luminous Intensity Versus Forward Current.

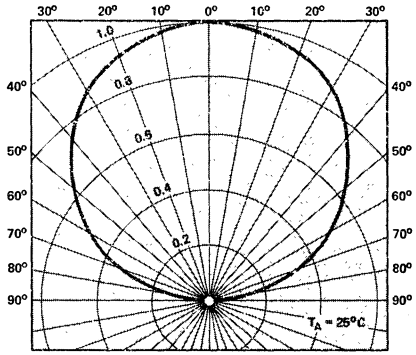


Figure 3. Typical Relative Luminous Intensity Versus Angular Displacement.

HEWLETT hp PACKARD

COMPONENTS

LOW PROFILE SOLID STATE LAMPS

RED • 5082-4790 SERIES
HIGH EFFICIENCY RED • 5082-4690 SERIES
YELLOW • 5082-4590 SERIES
GREEN • 5082-4990 SERIES

TECHNICAL DATA APRIL 1979

Features

- **HIGH INTENSITY**
- **LOW PROFILE: 5.8mm (0.23 in) NOMINAL**
- **T-1¾ DIAMETER PACKAGE**
- **LIGHT OUTPUT CATEGORIES**
- **DIFFUSED AND NON-DIFFUSED TYPES**
- **GENERAL PURPOSE LEADS**
- **IC COMPATIBLE/LOW CURRENT REQUIREMENTS**
- **RELIABLE AND RUGGED**
- **CHOICE OF 4 BRIGHT COLORS**
  Red High Efficiency Red
  Yellow Green

Description

The 5082-4790/4791 are Gallium Arsenide Phosphide Red Light Emitting Diodes packaged in a Low Profile T-1¾ outline with a red diffused lens.

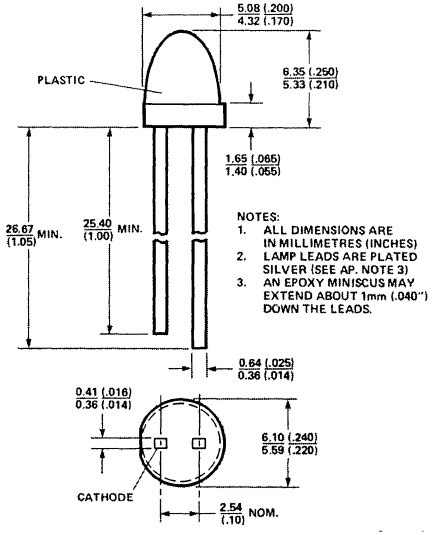
The 5082-4690 Series are Gallium Arsenide Phosphide on Gallium Phosphide High Efficiency Red Light Emitting Diodes packaged in a Low Profile T-1¾ outline.

The 5082-4590 Series are Gallium Arsenide Phosphide on Gallium Phosphide Yellow Light Emitting Diodes packaged in a Low Profile T-1¾ outline.

The 5082-4990 Series are Gallium Phosphide Green Light Emitting Diodes packaged in a Low Profile T-1¾ outline.

The Low Profile T-1¾ package provides space savings and is excellent for backlighting applications.

Package Dimensions



Part Number 5082-	Application	Lens	Color
4690	Indicator — General Purpose	Diffused Wide Angle	High Efficiency Red
4693	Indicator — High Brightness		
4694	General Purpose Point Source	Non-diffused Narrow Angle	
4695	High Brightness Annunciator		
4590	Indicator — General Purpose	Diffused Wide Angle	Yellow
4592	Indicator — High Brightness		
4595	General Purpose Point Source	Non-diffused Narrow Angle	
4597	High Brightness Annunciator		
4990	Indicator — General Purpose	Diffused Wide Angle	Green
4992	Indicator — High Brightness		
4995	General Purpose Point Source	Non-diffused Narrow Angle	
4997	High Brightness Annunicator		
4790	Indicator — General Purpose	Diffused Wide Angle	Red
4791	Indicator — High Brightness		

SOLID STATE LAMPS

Absolute Maximum Ratings at T_A=25°C

Parameter	Red 4790 Series	Hi-Eff. Red 4690 Series	Yellow 4590 Series	Green 4990 Series	Units
Power Dissipation	100	120	120	120	mW
Average Forward Current	50[1]	20[1]	20[1]	30[2]	mA
Peak Forward Current	1000 See Fig. 5	60 See Fig. 10	60 See Fig. 15	60 See Fig. 20	mA
Operating and Storage Temperature Range	-55°C to + 100°C				
Lead Solder Temperature (1.6mm [0.63 inch] from body)	260°C For 5 Seconds				

1. Derate from 50°C at 0.2mA/°C
2. Derate from 50°C at 0.4mA/°C

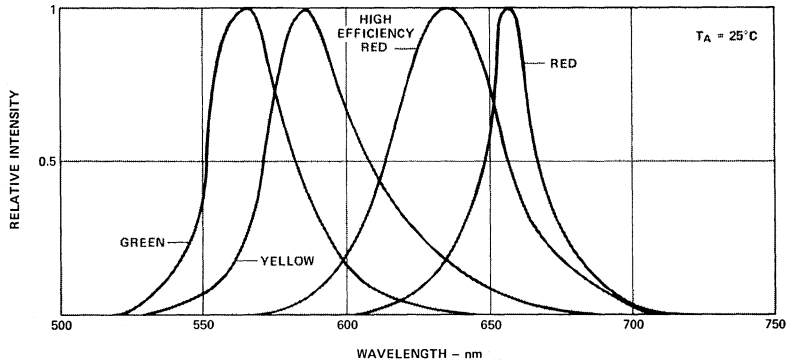


Figure 1. Relative Intensity versus Wavelength.

RED 5082-4790 SERIES
Electrical Specifications at T_A=25°C

Symbol	Description	Device 5082-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	4790	0.8	1.2		mcd	I_F = 20mA (Fig. 3)
		4791	1.6	2.5			
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points			60		deg.	Note 1 (Fig. 6)
λ_{PEAK}	Peak Wavelength			655		nm	Measurement @ Peak (Fig. 1)
λ_d	Dominant Wavelength			648		nm	Note 2
τ_s	Speed of Response			15		ns	
C	Capacitance			100		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			125		°C/W	Junction to Cathode Lead 1.6 mm (0.063 in.) from Body
V_F	Forward Voltage			1.6	2.0	V	I_F = 20mA (Fig. 2)
BV_R	Reverse Breakdown Voltage		3	10		V	I_R = 100μA
η_V	Luminous Efficacy			55		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

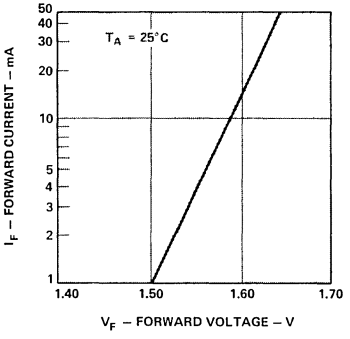


Figure 2. Forward Current versus Forward Voltage.

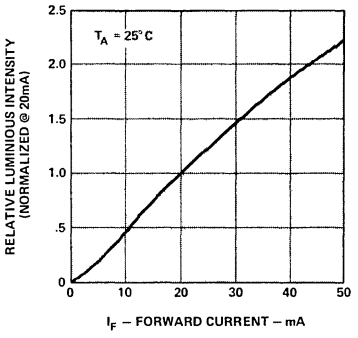


Figure 3. Relative Luminous Intensity versus Forward Current.

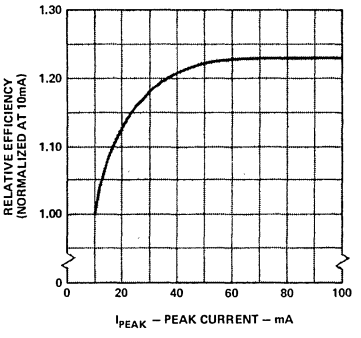


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

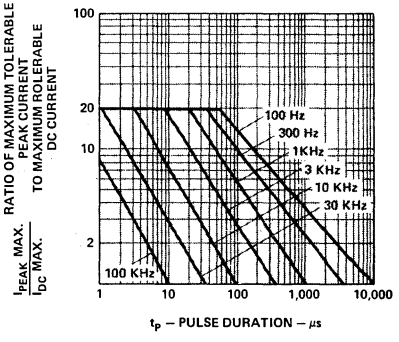


Figure 5. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

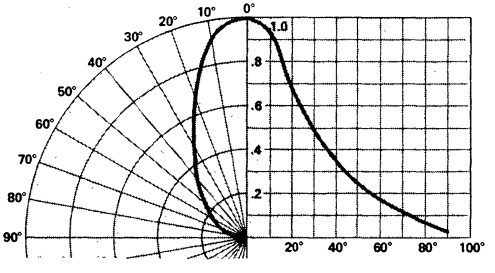


Figure 6. Relative Luminous Intensity versus Angular Displacement.

HIGH EFFICIENCY RED 5082-4690 SERIES
Electrical Specifications at T_A=25°C

Symbol	Description	Device 5082-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	4690 4693 4694 4695	1.5 5.0 4.0 8.0	3.5 7.0 8.0 11.0		mcd	I_F = 10mA (Fig.8)
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	4690 4693 4694 4695		50 50 45 45		deg.	Note 1 (Fig. 11)
λ_{PEAK}	Peak Wavelength			635		nm	Measurement @ Peak (Fig. 1)
λ_d	Dominant Wavelength			626		nm	Note 2
τ_s	Speed of Response			90		ns	
C	Capacitance			16		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			130		°C/W	Junction to Cathode Lead 1.6mm (0.063 in.) from Body
V_F	Forward Voltage			2.2	3.0	V	I_F = 10mA (Fig. 7)
BV_R	Reverse Breakdown Voltage		5.0			V	I_R = 100μA
η_V	Luminous Efficacy			147		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

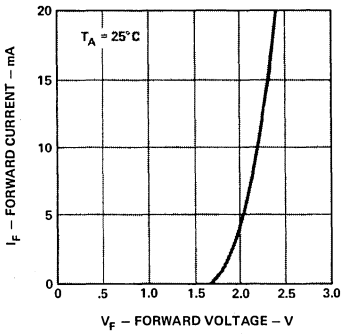


Figure 7. Forward Current versus Forward Voltage.

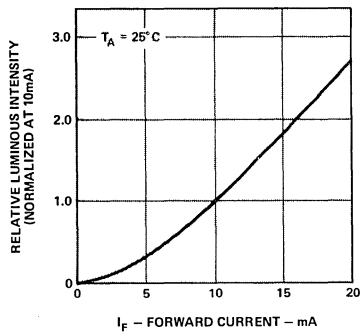


Figure 8. Relative Luminous Intensity versus Forward Current.

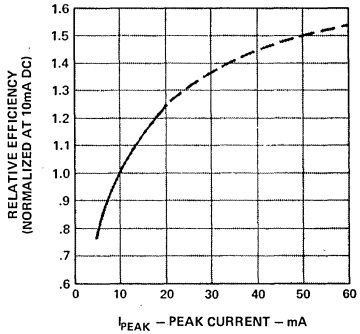


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

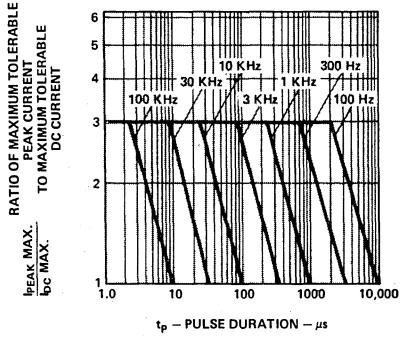


Figure 10. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

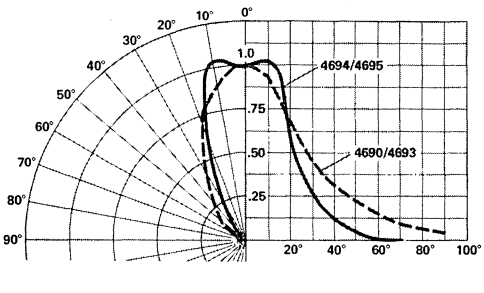


Figure 11. Relative Luminous Intensity versus Angular Displacement.

YELLOW 5082-4590 SERIES
Electrical Specifications at T_A=25°C

Symbol	Description	Device 5082-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	4590 4592 4595 4597	1.5 4.5 4.0 8.0	3.5 6.0 6.5 11.0		mcd	I_F = 10mA (Fig. 13)
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	4590 4592 4595 4597		50 50 45 45		deg.	Note 1 (Fig. 16)
λ_{PEAK}	Peak Wavelength			583		nm	Measurement @ Peak (Fig. 1)
λ_d	Dominant Wavelength			585		nm	Note 2
τ_s	Speed of Response			90		ns	
C	Capacitance			18		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			100		°C/W	Junction to Cathode Lead 1.6mm (0.063 in.) from Body
V_F	Forward Voltage			2.2	3.0	V	I_F = 10mA (Fig. 12)
BV_R	Reverse Breakdown Voltage		5.0			V	I_R = 100μA
η_V	Luminous Efficacy			570		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

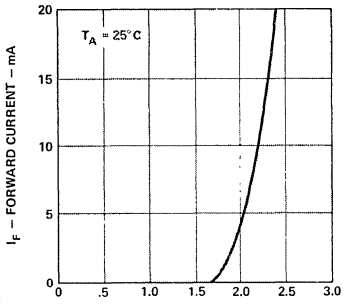


Figure 12. Forward Current versus Forward Voltage.

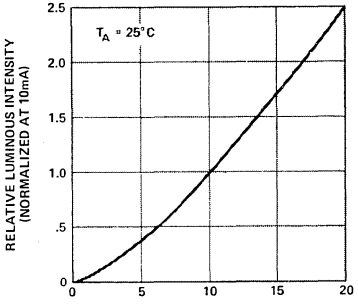


Figure 13. Relative Luminous Intensity versus Forward Current.

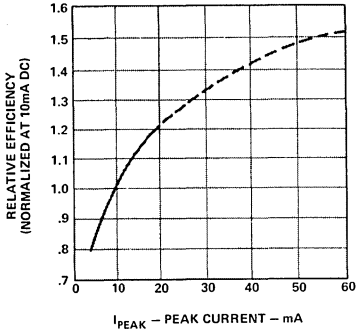


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

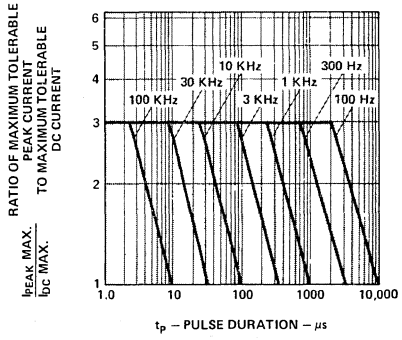


Figure 15. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings).

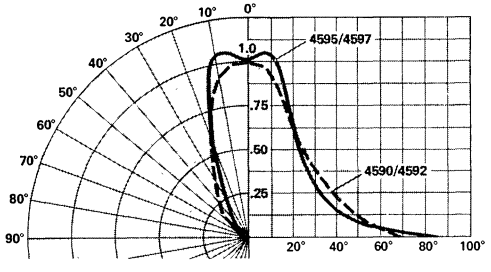


Figure 16. Relative Luminous Intensity versus Angular Displacement

GREEN 5082-4990 SERIES
Electrical Specifications at T_A=25°C

Symbol	Description	Device 5082-	Min.	Typ.	Max.	Units	Test Conditions
I_V	Axial Luminous Intensity	4990 4992 4995 4997	2.0 6.0 3.5 8.0	4.5 7.5 6.5 11.0		mcd	I_F = 20mA (Fig.18)
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points	4990 4992 4995 4997		50 50 40 40		deg.	Note 1 (Fig.21)
λ_{PEAK}	Peak Wavelength			565		nm	Measurement @ Peak (Fig. 1)
λ_d	Dominant Wavelength			570		nm	Note 2
τ_s	Speed of Response			200		ns	
C	Capacitance			12		pF	V_F = 0; f = 1 MHz
θ_{JC}	Thermal Resistance			90		°C/W	Junction to Cathode Lead 1.6mm (0.063 in.) from Body
V_F	Forward Voltage			2.4	3.0	V	I_F = 20mA (Fig. 17)
BV_R	Reverse Breakdown Voltage		5.0			V	I_R = 100μA
η_V	Luminous Efficacy			665		lm/W	Note 3

Notes: 1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity. 2. Dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device. 3. Radiant Intensity I_e, in watts/steradian may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

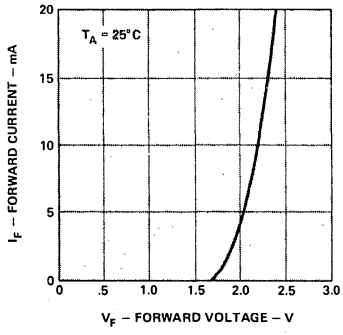


Figure 17. Forward Current versus Forward Voltage.

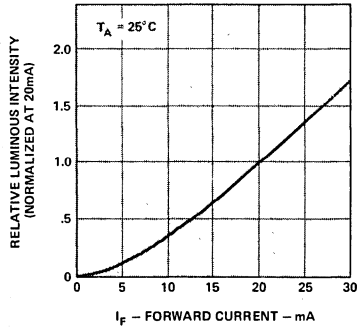


Figure 18. Relative Luminous Intensity versus Forward Current.

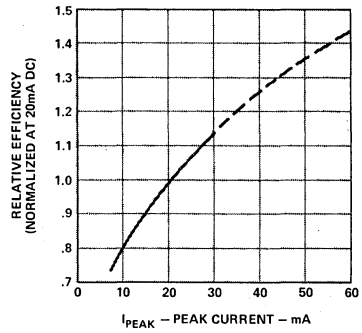


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current.

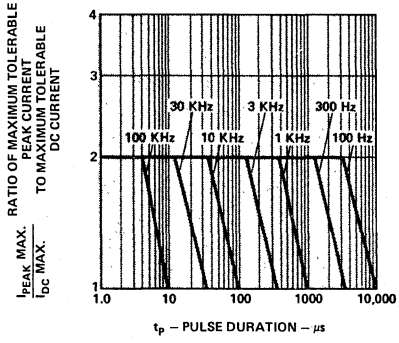


Figure 20. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX ratings).

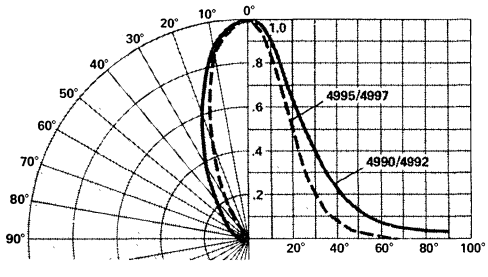


Figure 21. Relative Luminous Intensity versus Angular Displacement.

HEWLETT hp PACKARD

COMPONENTS

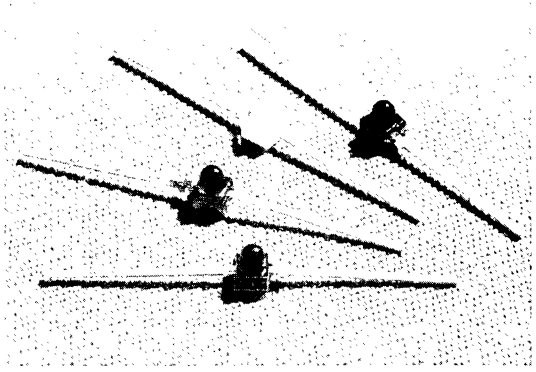
SUBMINIATURE SOLID STATE LAMPS

RED • 5082-4100/4101
HIGH EFFICIENCY RED • 5082-4160
YELLOW • 5082-4150
GREEN • 5082-4190

TECHNICAL DATA APRIL 1979

Features

- **SUBMINIATURE PACKAGE STYLE**
- **END STACKABLE ON 2.21mm (0.087 in.) CENTERS**
- **LOW PACKAGE PROFILE**
- **RADIAL LEADS**
- **WIDE VIEWING ANGLE**
- **LONG LIFE — SOLID STATE RELIABILITY**
- **CHOICE OF 4 BRIGHT COLORS**
  - **Red**
  - **High Efficiency Red**
  - **Yellow**
  - **Green**



Description

The 5082-4100/4101, 4150, 4160 and 4190 are solid state lamps encapsulated in a radial lead subminiature package of molded epoxy. They utilize a tinted, diffused lens providing high on-off contrast and wide-angle viewing.

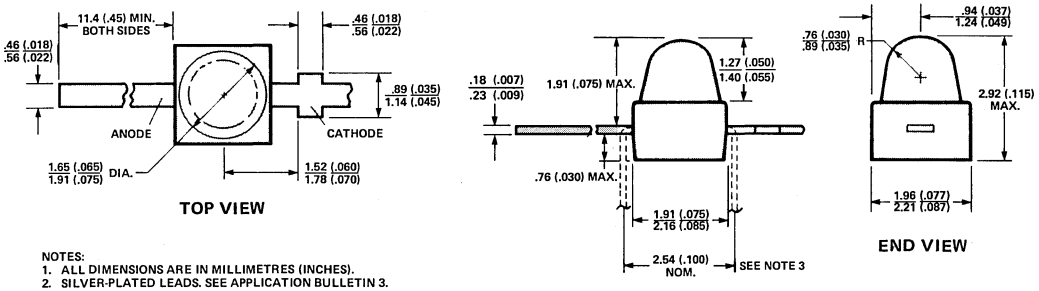
The -4100/4101 utilizes a GaAsP LED chip in a deep red molded package.

The -4160 has a high-efficiency red GaAsP on GaP LED chip in a light red molded package. This lamp's efficiency is comparable to that of the GaP red but does not saturate at low current levels.

The -4150 provides a yellow GaAsP on GaP LED chip in a yellow molded package.

The -4190 provides a green GaP LED chip in a green molded package.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER-PLATED LEADS. SEE APPLICATION BULLETIN 3.
3. USER MAY BEND LEADS AS SHOWN.

Absolute Maximum Ratings at T_A=25°C

Parameter	Red 4100/4101	High Eff. Red 4160	Yellow 4150	Green 4190	Units
Power Dissipation	100	120	120	120	mW
Average Forward Current	50[1]	20[1]	20[1]	30[2]	mA
Peak Forward Current	1000 See Fig. 5	60 See Fig. 10	60 See Fig. 15	60 See Fig. 20	mA
Operating and Storage Temperature Range	-55°C to 100°C				
Lead Soldering Temperature [1.6mm (0.063 in.) from body]	230°C for 3 seconds				

1. Derate from 50° C at 0.2mA/° C
2. Derate from 50° C at 0.4mA/° C

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	5082-4100/4101			5082-4160			5082-4150			5082-4190			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Axial Luminous Intensity	—/0.5	.7/1.0		1.0	3.0		1.0	2.0		0.8	1.5		mcd	I_F=10mA, Figs. 3,8,13,18
											At I_F = 20mA				
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		45			80			90			70		deg.	Note 1. Figures 6, 11, 16, 21
λ_{PEAK}	Peak Wavelength		655			635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		640			628			585			572		nm	Note 2
τ_S	Speed of Response		15			90			90			200		ns	
C	Capacitance		100			11			15			13		pF	V_F=0; f=1 MHz
Θ_{JC}	Thermal Resistance		125			120			100			100		°C/W	Junction to Cathode Lead at 0.79mm (.031 in) from Body
V_F	Forward Voltage		1.6	2.0		2.2	3.0		2.2	3.0		2.4	3.0	V	I_F=10mA, Figures 2, 7, 12, 17
											At I_F = 20mA				
BV_R	Reverse Breakdown Voltage	3.0	10		5.0			5.0			5.0			V	I_R = 100μA
η_V	Luminous Efficacy		55			147			570			665		lm/W	Note 3

NOTES:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e=I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

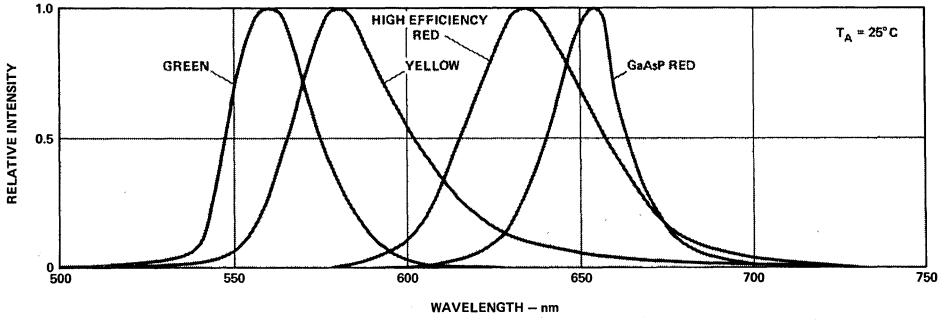


Figure 1. Relative Intensity vs. Wavelength.

Red 5082-4100/4101

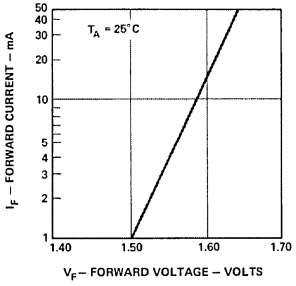


Figure 2. Forward Current vs. Forward Voltage.

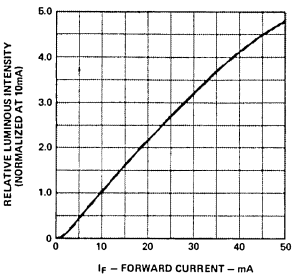


Figure 3. Relative Luminous Intensity vs. Forward Current.

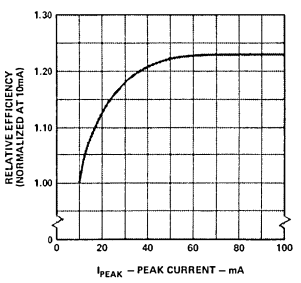


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

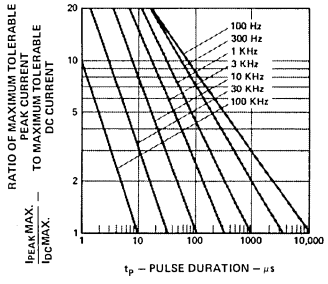


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

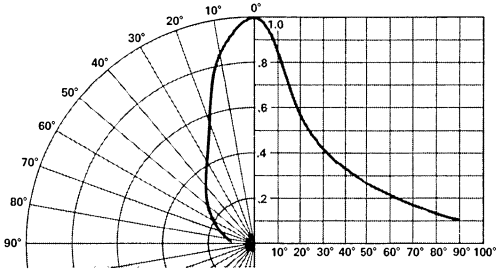


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

High Efficiency Red 5082-4160

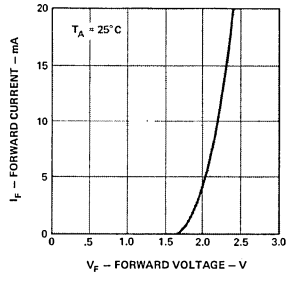


Figure 7. Forward Current vs. Forward Voltage.

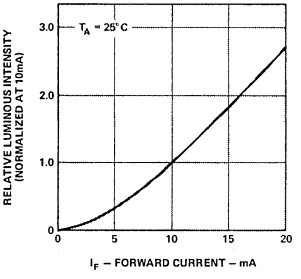


Figure 8. Relative Luminous Intensity vs. Forward Current.

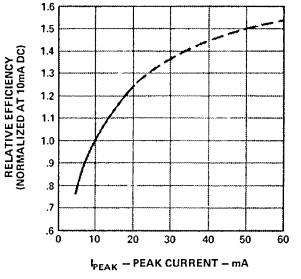


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

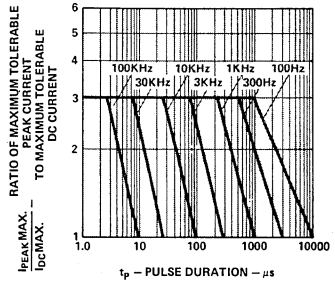


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

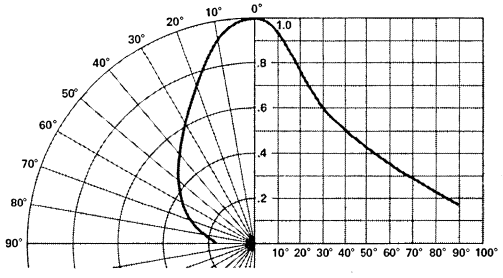


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

SOLID STATE LAMPS

Yellow 5082-4150

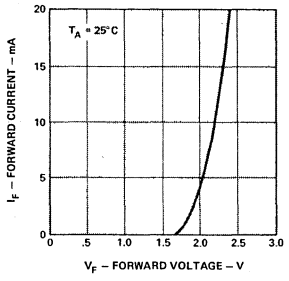


Figure 12. Forward Current vs. Forward Voltage.

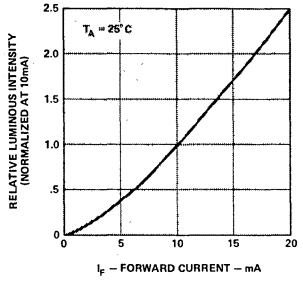


Figure 13. Relative Luminous Intensity vs. Forward Current.

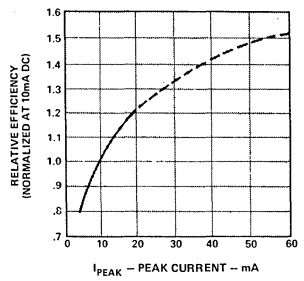


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

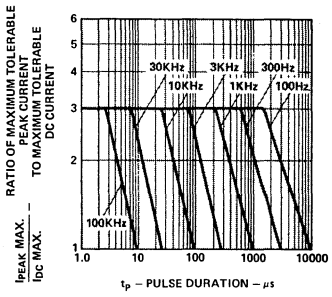


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

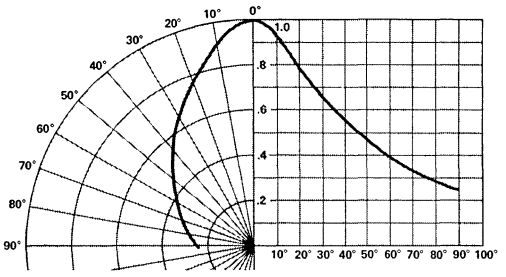


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

Green 5082-4190

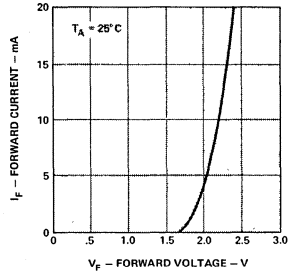


Figure 17. Forward Current vs. Forward Voltage.

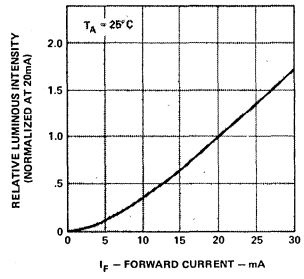


Figure 18. Relative Luminous Intensity vs. Forward Current.

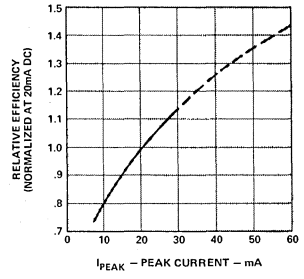


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

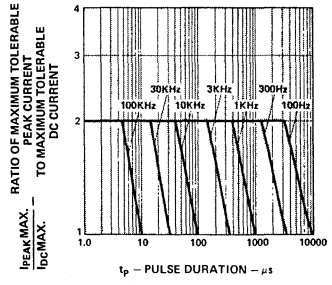


Figure 20. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

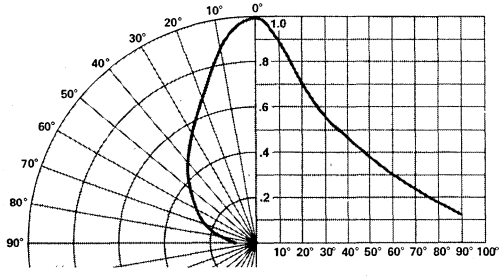


Figure 21. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT hp PACKARD

COMPONENTS

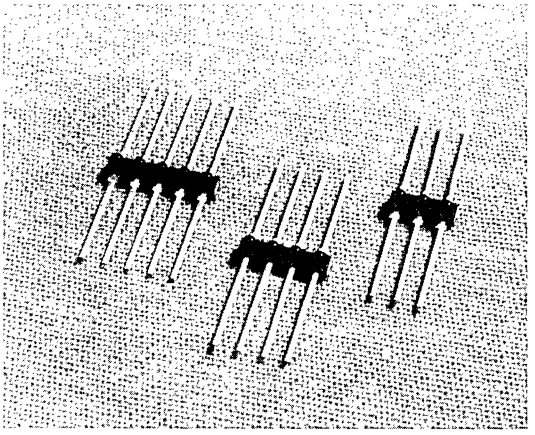
MATCHED ARRAYS OF SUBMINIATURE RED SOLID STATE LAMPS

3 - ELEMENT • HLMP - 6203
4 - ELEMENT • HLMP - 6204
5 - ELEMENT • HLMP - 6205

TECHNICAL DATA APRIL 1979

Features

- **EXCELLENT UNIFORMITY BETWEEN ELEMENTS AND BETWEEN ARRAYS**
- **EASY INSERTION AND ALIGNMENT**
- **VERSATILE LENGTHS — 3,4,5 ELEMENTS**
- **END STACKABLE FOR LONGER ARRAYS**
- **COMPACT SUBMINIATURE PACKAGE STYLE**
- **NO CROSSTALK BETWEEN ELEMENTS**



Description

The HLMP-62XX Series arrays are comprised of several Gallium Arsenide Phosphide Red Solid State Lamps molded as a single bar. Arrays are tested to assure uniformity between elements and matching between arrays. Each element has separately accessible leads and a red diffused lens which provides a wide viewing angle and a high on/off contrast ratio. Center-to-center spacing is 2.54mm (.100 in.) between elements and arrays are end stackable on 2.54mm (.100 in.) centers.

Absolute Maximum Ratings/Element at $T_A = 25°C$

Power Dissipation ..... 100 mW

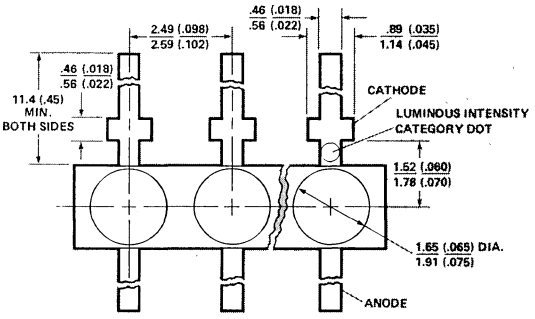
Average Forward Current (Derate linearly from 50°C at 0.2mA/°/C) ..... 50 mA

Peak Forward Current (see Figure 4) ..... 1000 mA

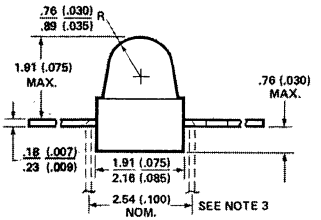
Operating and Storage Temperature Range ..... -55°C to +100°C

Lead Soldering Temperature [1.6 mm (0.063 in.) from body] ..... 230°C for 3 sec.

Package Dimensions



Notes:
1. All dimensions are in millimetres (inches).
2. Silver-plated leads. See Application Bulletin 3.
3. User may bend leads as shown.
4. Overall length is the number of elements times 2.54mm (.100 in.).



SOLID STATE LAMPS

Electrical Specifications/Element at T_A=25°C

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions	Figure
I_V	Axial Luminous Intensity	.5	1.0		mcd	I_F = 10 mA; Note 1	2
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		45		Deg.	Note 2	5
λ_{PEAK}	Peak Wavelength		655		nm	Measurement @ Peak	
λ_d	Dominant Wavelength		640		nm	Note 3	
τ_s	Speed of Response		15		ns		
C	Capacitance		100		pF	V_F = 0; f = 1 MHz	
θ_{JC}	Thermal Resistance		125		°C/W	Junction to Cathode Lead at .79mm(.031in)from the body	
V_F	Forward Voltage		1.6	2.0	V	I_F = 10 mA	1
BV_R	Reverse Breakdown Voltage	3	10		V	I_R = 100 μA	
η_V	Luminous Efficacy		55		lm/W	Note 4	

Notes:
1. Arrays are categorized for luminous intensity with the intensity category designated by a color dot located on the cathode side of the package.
2. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
3. Dominant wavelength, λ_d, is derived from the CIE Chromaticity Diagram and is that single wavelength which defines the color of the device.
4. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

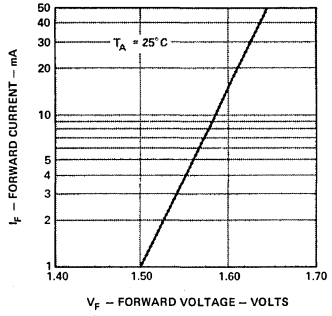


Figure 1. Forward Current vs. Forward Voltage.

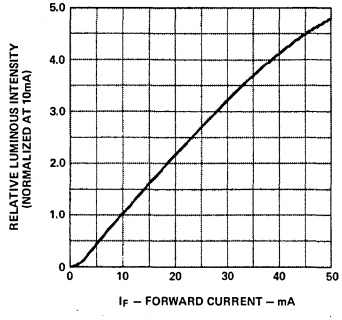


Figure 2. Relative Luminous Intensity vs. DC Forward Current.

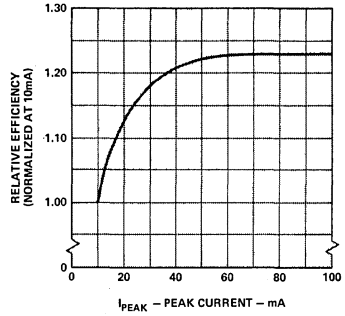


Figure 3. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

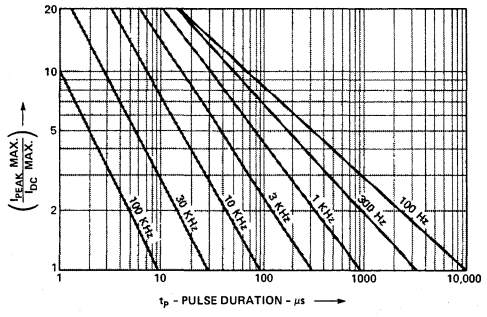


Figure 4. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings).

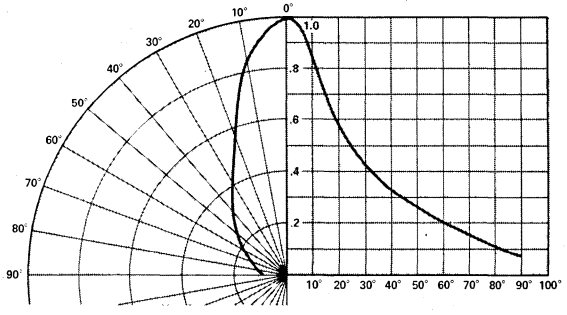


Figure 5. Relative Luminous Intensity vs. Angular Displacement.

HEWLETT hp PACKARD

COMPONENTS

SUBMINIATURE RESISTOR LAMPS

HIGH EFFICIENCY RED

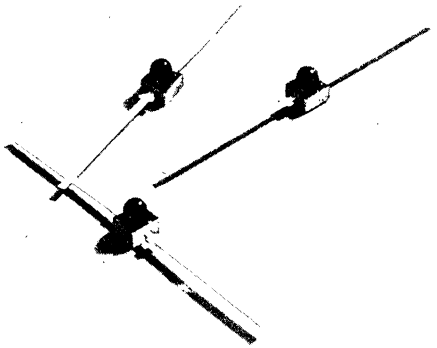
5 VOLT, 4mA • HLMP-6620
5 VOLT, 10mA • HLMP-6600

TECHNICAL DATA APRIL 1979

SOLID STATE LAMPS

Features

- **IDEAL FOR TTL AND LSTTL GATE STATUS INDICATION**
- **REQUIRES NO EXTERNAL RESISTORS WITH 5 VOLT SUPPLY**
- **SPACE SAVING SUBMINIATURE PACKAGE**
- **TWO CHOICES OF CURRENT LEVEL**
- **RUGGED INTEGRAL RESISTOR AND REVERSE PROTECTION DIODE**
- **EXCELLENT VIEWING ANGLE**



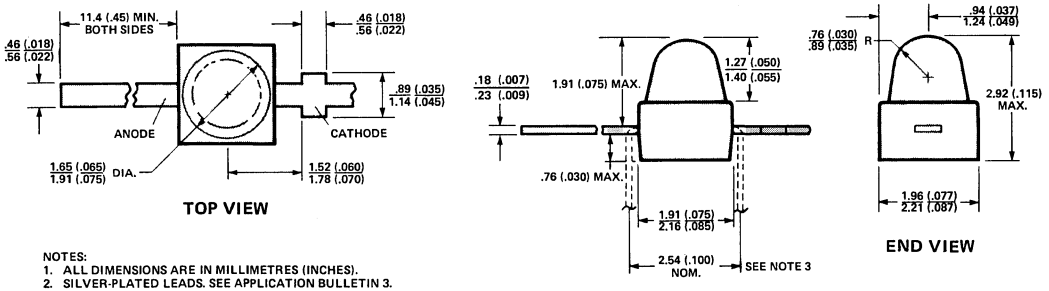
Description

The HLMP-6600 and HLMP-6620 provide a Red Gallium Arsenide Phosphide on Gallium Phosphide Light Emitting Diode together with an integral biasing resistor and reverse protection diode. The package has a red diffused lens and radial leads. Tape-and-reel mounting is available on request.

Absolute Maximum Ratings

	HLMP-6600	HLMP-6620
DC Forward Voltage	6 Volts	6 Volts
Reverse Voltage	15 Volts	15 Volts
Operating Temperature Range	-55°C to 70°C	
Storage Temperature Range	-55°C to 100°C	
Lead Soldering Temperature [1.6mm (0.063 in.) from body]	230°C for 5 sec.	

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER-PLATED LEADS. SEE APPLICATION BULLETIN 3.
3. USER MAY BEND LEADS AS SHOWN.

Electrical/Optical Characteristics at T_A=25°C

Symbol	Parameter	HLMP-6600			HLMP-6620			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Axial Luminous Intensity	1.0	2.4	—	0.2	0.6	—	mcd	V_F = 5 Volts (See Figure 1)
$2\Theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		90°			90°			Note 1 (See Figure 2)
λ_{PEAK}	Peak Wavelength		635			635		nm	Measurement at Peak
λ_d	Dominant Wavelength		628			628		nm	Note 2
Θ_j	Thermal Resistance		120			120		°C/W	Junction to Cathode Lead at 0.79mm (0.031 in.) From Body
I_F	Forward Current		9.6	13		3.5	5	mA	V_F=5 Volts (See Figure 3)
I_R	Reverse Current			10			10	μA	V_R=15 Volts
η_V	Luminous Efficacy		147			147		lm/W	Note 3

NOTES:
1. $\Theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_V/\eta_V$, where I_V is the luminous intensity in candelas and η_V is the luminous efficacy in lumens/watt.

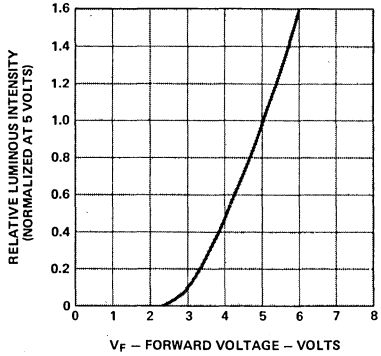


Figure 1. Relative Luminous Intensity vs. Forward Voltage.

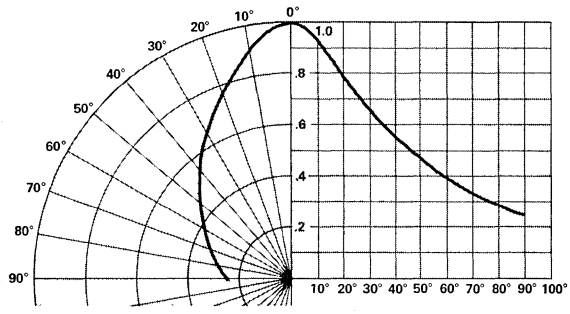


Figure 2. Relative Luminous Intensity vs. Angular Displacement.

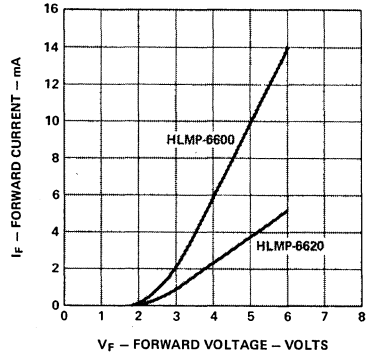


Figure 3. Forward Current vs. Forward Voltage.

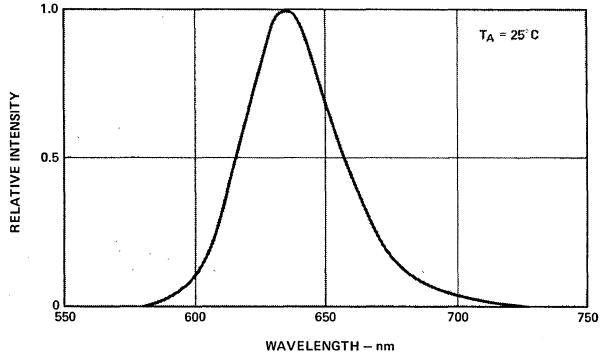


Figure 4. Relative Intensity vs. Wavelength.

HEWLETT hp PACKARD

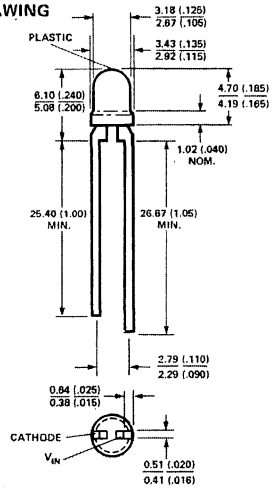
COMPONENTS

VOLTAGE SENSING LED

5082-4732

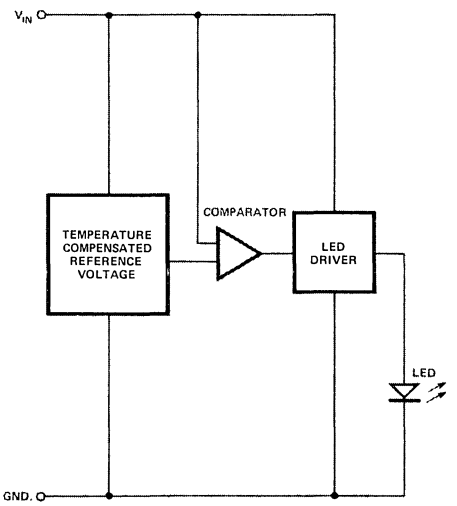
TECHNICAL DATA APRIL 1979

OUTLINE DRAWING



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATIONS BULLETIN 3.
3. AN EPOXY MINISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

BLOCK DIAGRAM



Features

- **HIGH SENSITIVITY: 10mV ON TO OFF**
- **BUILT IN LED CURRENT LIMITING**
- **TEMPERATURE COMPENSATED THRESHOLD VOLTAGE**
- **COMPACT: PACKAGE INCLUDES INTEGRATED CIRCUIT AND LED**
- **GUARANTEED MINIMUM LUMINOUS INTENSITY**
- **THRESHOLD VOLTAGE CAN BE INCREASED WITH EXTERNAL COMPONENT**

Applications

- Push-to-test battery voltage tester (pagers, cameras, appliances, radios, test equipment. . .)
- Logic level indicator
- Power supply voltage monitor
- V-U meter
- Analog level sense
- Voltage indicating arrays — use several with different thresholds
- Current monitor

Description

The HP voltage sensing LEDs use an integrated circuit and a red GaAsP LED to provide a complete voltage sensing function in a standard red diffused T-1 LED package. When the input voltage (V_{IN}) exceeds the threshold voltage (V_{TH}) the LED turns "on". The high gain of the comparator provides unambiguous indication by the LED of the input voltage with respect to the threshold voltage. The V-I characteristics are resistive above and below the threshold voltage. This allows battery testing under simulated load conditions. Use of a resistor, diode or zener in series allows the threshold voltage to be increased to any desired voltage. A resistor in parallel allows the sensing LED to be used as a current threshold indicator.

The 5082-4732 has a nominal threshold voltage of 2.7V.

Absolute Maximum Ratings

Storage Temperature	-55°C to +100°C
Operating Temperature	-55°C to +85°C
Lead Solder Temperature	230°C for 7 Sec
Input Voltage — V_{IN} [1]	+5V dc
Reverse Input Voltage — V_R	-0.5V

NOTES:
1. Derate linearly above 50° C free-air temperature at a rate of 37mV/°C.

SOLID STATE LAMPS

Electro-Optical Characteristics at T_A=25°C

Parameter	Sym.	5082-4732 Min.	Typ.	Max.	Units	Test Conditions	Fig.
Threshold Voltage	V_{TH}	2.5	2.7	2.9	V		1,2
Temperature Coefficient of Threshold	$\frac{\Delta V_{TH}}{\Delta T_A}$		−1		mV/°C		
Input Current	I_{IN}		13		mA	V_{IN} = 2.75V	2
			33	50	mA	V_{IN} = 5.0V	2
Luminous Intensity	I_v	0.3	0.7		mcd	V_{IN} = 2.75V	1
Wavelength	λ_{PEAK}		655		nm	Measurement at peak	
Dominant Wavelength	λ_d		639		nm	Note 1	

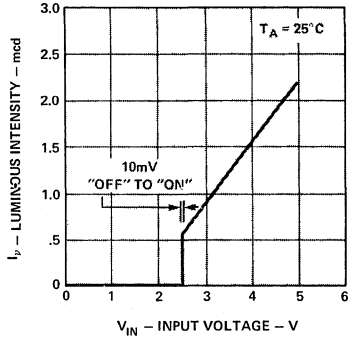


Figure 1. Luminous Intensity vs. Input Voltage.

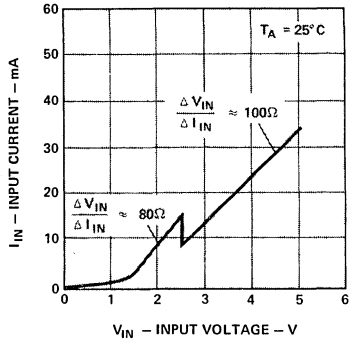


Figure 2. Input Current vs. Input Voltage.

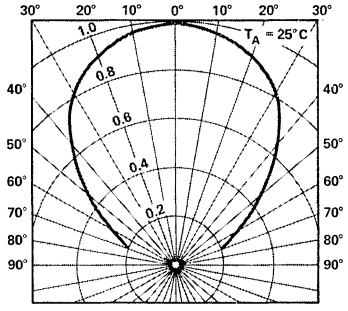
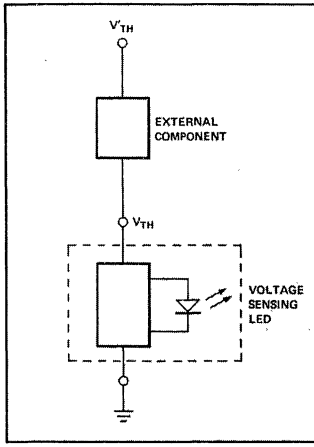


Figure 3. Relative Luminous Intensity vs. Angular Displacement.

Techniques For Increasing The Threshold Voltage



External Component	V'_{TH}	$TC = \frac{\Delta V'_{TH}}{\Delta T_A}$ (mV/°C)
Schottky Diode (HP 5082-2835)	V_{TH} + 0.45V	−2
P-N Diode (1N914)	V_{TH} + 0.75V	−2.5
LED (HP 5082-4484)	V_{TH} + 1.6V	−2.9
Zener Diode	$V_{TH} + V_Z$	−1 + Zener TC

Notes:
1. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
2. I_{TH} is the maximum current just below the threshold, V_{TH}. Since both I_{TH} and V_{TH} are variable, a precise value of V'_{TH} is obtainable only by selecting R to fit the measured characteristics of the individual devices (e.g., with curve tracer).
3. The temperature coefficient (TC) will be a function of the resistor TC and the value of the resistor.

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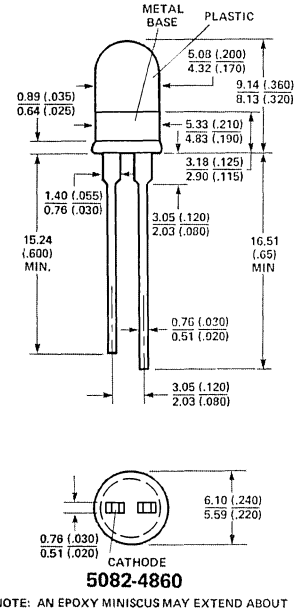
COMPONENTS

RESISTOR LEDs

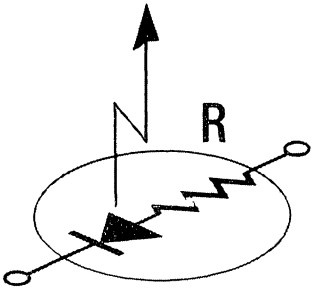
5082-4860
5082-4468

TECHNICAL DATA APRIL 1979

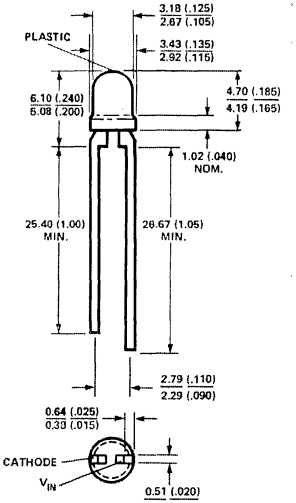


5082-4860

NOTE: AN EPOXY MINISCUS MAY EXTEND ABOUT 1mm (0.040") DOWN THE LEADS.



DIMENSIONS IN MILLIMETRES AND (INCHES)



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER PLATED LEADS. SEE APPLICATIONS BULLETIN 3.
3. AN EPOXY MINISCUS MAY EXTEND ABOUT 1mm (.040") DOWN THE LEADS.

5082-4468

Features

- **TTL COMPATIBLE: 16mA @ 5 VOLTS TYPICAL**
- **INTEGRAL CURRENT LIMITING RESISTOR**
- **T-1 DIAMETER PACKAGE, 3.18mm (.125 in.)**
  T-1¾ DIAMETER PACKAGE, 5.08mm (.200 in.)
- **RUGGED AND RELIABLE**

Description

The HP Resistor-LED series provides an integral current limiting resistor in series with the LED. Applications include panel mounted indicators, cartridge indicators, and lighted switches.

The 5082-4860 is a standard red diffused 5.08mm (.200") diameter (T-1¾ size) LED, with long wire wrappable leads.

The 5082-4468 is a clear diffused 3.18mm (.125") diameter (T-1 size) LED.

Absolute Maximum Ratings at T_A=25°C

DC Forward Voltage [Derate linearly to 5V @ 100°C]	7.5V
Reverse Voltage	7V
Isolation Voltage [between lead and base of the 5082-4860]	300V
Operating and Storage Temperature Range	–55°C to +100°C
Lead Soldering Temperature	230°C for 7 sec.

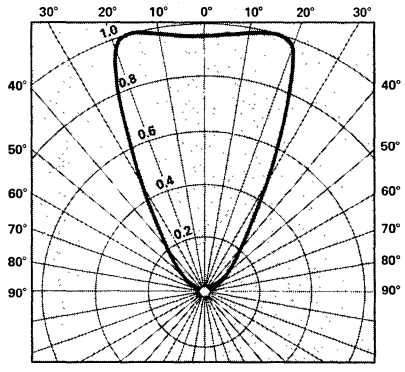
SOLID STATE LAMPS

Electrical Characteristics at T_A=25°C

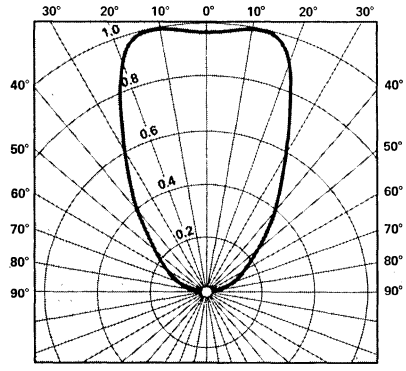
Symbol	Parameters	5082-4860/-4468			Units	Test Conditions
		Min.	Typ.	Max.		
I_V	Luminous Intensity	0.3	0.8		mcd	V_F = 5.0V
λ_{PEAK}	Wavelength		655		nm	Measurement at Peak
τ_s	Speed of Response		15		ns	
I_F	Forward Current		16	20	mA	V_F = 5.0V
BV_R	Reverse Breakdown Voltage	3			V	I_R = 100μA

TYPICAL RELATIVE LUMINOUS INTENSITY VERSUS ANGULAR DISPLACEMENT

4860



4468



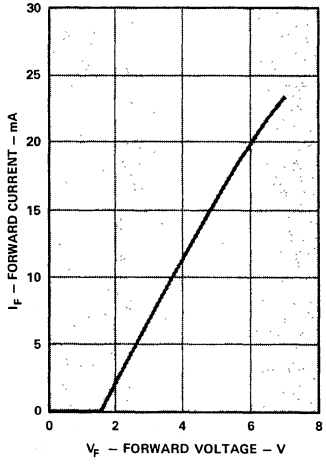


Figure 1. Typical DC Forward Current – Voltage Characteristic

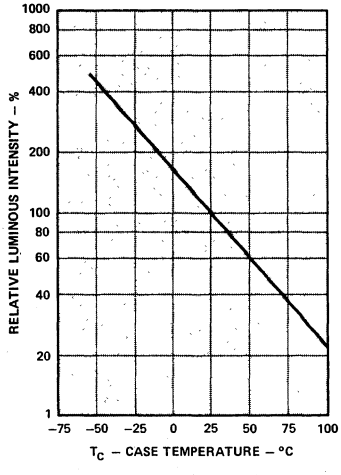


Figure 2. Relative Luminosity vs. Case Temperature

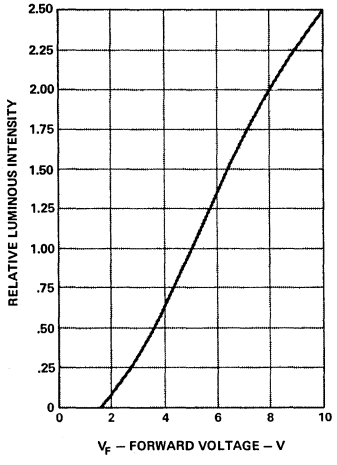


Figure 3. Relative Luminous Intensity vs. Voltage

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COMPONENTS

HERMETIC SOLID STATE LAMPS*

1N6092 1N6094
1N6093 1N5765

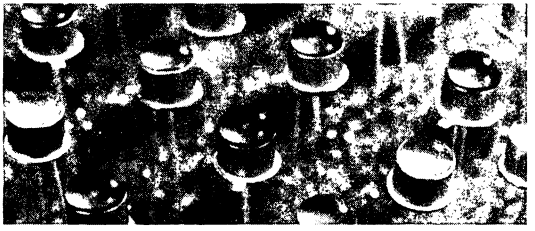
JAN 1N5765/ 1N6092/1N6093/1N6094

JAN TX 1N5765/ 1N6092/1N6093/1N6094

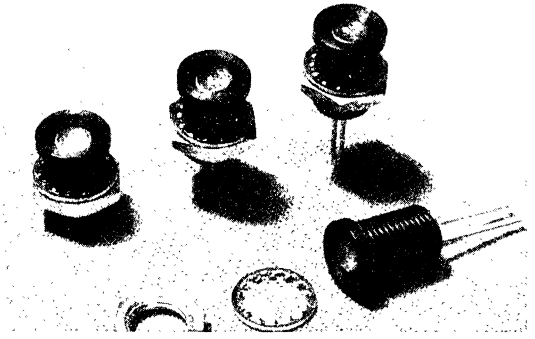
TECHNICAL DATA APRIL 1979

Features

- **CHOICE OF 4 COLORS**
  - **Red**
  - **High Efficiency Red**
  - **Yellow**
  - **Green**
- **DESIGNED FOR HIGH-RELIABILITY APPLICATIONS**
- **HERMETICALLY SEALED**
- **WIDE VIEWING ANGLE**
- **LOW POWER OPERATION**
- **IC COMPATIBLE**
- **LONG LIFE**
- **PANEL MOUNT OPTION HAS WIRE WRAPPABLE LEADS AND AN ELECTRICALLY ISOLATED CASE**



TO-46



HERMETIC PANEL MOUNT

Description

The 1N5765, 1N6092, 1N6093, and 1N6094 are hermetically sealed solid state lamps encapsulated in a TO-46 package with a tinted diffused plastic lens over a glass window. These hermetic lamps provide good on-off contrast, high axial luminous intensity and a wide viewing angle.

All of these devices are available in a panel mountable fixture. The semiconductor chips are packaged in a hermetically sealed TO-46 package with a tinted diffused plastic lens over glass window. This TO-46 package is then encapsulated in a panel mountable fixture designed for high reliability applications. The encapsulated LED lamp assembly provides a high on-off contrast, a high axial luminous intensity and a wide viewing angle.

The 1N5765 utilizes a GaAsP LED chip with a red diffused plastic lens over glass window.

The 1N6092 has a high efficiency red GaAsP on GaP LED chip with a red diffused plastic lens over glass window. This lamp's efficiency is comparable to that of a GaP red but extends to higher current levels.

The 1N6093 provides a yellow GaAsP on GaP LED chip with a yellow diffused plastic lens over glass window.

The 1N6094 provides a green GaP LED chip with a green diffused plastic lens over glass window.

Color — Part Number — Panel Mount Matrix

Description	Red	High Efficiency Red	Yellow	Green
Base Hermetic Part	1N5765	1N6092	1N6093	1N6094
Base Hermetic Part in Panel-Mount	5082-4787	5082-4687	5082-4587	5082-4987
JAN Part	JAN1N5765	JAN1N6092	JAN1N6093	JAN1N6094
JAN Part in Panel-Mount	HLMP-0930	M19500/519-01	M19500/520-01	M19500/521-01
JANTX Part	JANTX1N5765	JANTX1N6092	JANTX1N6093	JANTX1N6094
JANTX Part in Panel-Mount	HLMP-0931	M19500/519-02	M19500/520-02	M19500/521-02

*Panel-Mount versions of all of the above are available per the selection matrix on this page.

JAN 1N5765: Samples of each lot are subjected to Group A inspection for parameters listed in Table I, and to Group B and Group C tests listed below. All tests are to the conditions and limits specified by MIL-S-19500/467. A summary of the data gathered in Groups A, B, and C lot acceptance testing is supplied with each shipment.

JAN TX 1N5765: Devices undergo 100% screening tests as listed below to the conditions and limits specified by MIL-S-19500/467. The JAN TX lot is then subjected to Group A, Group B and Group C tests as for the JAN 1N5765 above. A summary of the data gathered in Groups A, B and C acceptance testing can be provided upon request. Serialized data can be gathered, but lead times will be increased accordingly.

Group B Sample Acceptance Tests	Method MIL-STD-750
Physical Dimensions	2066
Solderability	2026
Thermal Shock	1056A
Temperature Cycling	1051A
Fine Leak Test	1071H
Gross Leak Test	1071C
Moisture Resistance	1021
Mechanical Shock	2016
Vibration	2056
Constant Acceleration	2006
Terminal Strength	2036E
Salt Atmosphere	1041
Temp. Storage (100°C, 340 hours)	1032
Operating Life (50mAdc, 340 hours)	1027

Group C Sample Acceptance Tests	Method MIL-STD-750
Low Temp. Operation (−55°C)	
Breakdown Voltage	4021
Temperature Cycling	1051A
Resistance to Solvents	*
Temp. Storage (100°C, 1K hours)	1031
Operating Life (50mAdc, 1K hours)	1026
Peak Forward Pulse Current	
TX Screening (100%)	
Temp. Storage (100°C, 72 hours)	
Temperature Cycling	1051A
Constant Acceleration	2006
Fine Leak Test	1071H
Gross Leak Test	1071C
Burn-in (50mAdc, 168 hours)	
Evaluation of Drift (I_{V1}, V_F, I_R)	

*MIL-STD-202 Method 215

Electrical / Optical Characteristics at T_A=25°C

(Per Table I, Group A Testing of MIL-S 19500/467)

Specification	Symbol	Min.	Max.	Units	Test Conditions
Luminous Intensity (Axial)	I_{v1}	0.5	3.0	mcd	I_F = 20mAdc, θ = 0°
Luminous Intensity (off Axis)	I_{v2}	0.3		mcd	I_F = 20mAdc, θ = 30° [see Note 2]
Wavelength	λ_v	630	700	nM	Design Parameter
Capacitance	C		300	pF	V_R = 0, f = 1MHz
Forward Voltage	V_F		2.0	Vdc	I_F = 20mAdc
Reverse Current	I_R		1	μAdc	V_R = 3Vdc [see Note 2]

NOTES:

1. Derate 0.67 mAdc/°C for T_A above 25°C.
2. These specifications apply only to JAN/JAN TX levels.

Absolute Maximum Ratings at T_A=25°C

Parameter	Red 1N5765/4787	High Eff. Red 1N6092/4687	Yellow 1N6093/4587	Green 1N6094/4987	Units
Power Dissipation (derate linearly from 50°C at 1.6mW/°C)	100	120	120	120	mW
Average Forward Current	50[1]	35[2]	35[2]	35[2]	mA
Peak Forward Current	1000 See Fig. 5	60 See Fig. 10	60 See Fig. 15	60 See Fig. 20	mA
Operating and Storage Temperature Range	-65°C to 100°C				
Lead Soldering Temperature [1.6mm (0.063 in.) from body]	260°C for 7 seconds.				

1. Derate from 50°C at 0.2mA/°C
2. Derate from 50°C at 0.5mA/°C

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	1N5765/5082-4787			1N6092/5082-4687			1N6093/5082-4587			1N6094/5082-4987			Units	Test Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_V	Axial Luminous Intensity	0.5	1.0		1.0	2.5		1.0	2.5		0.8	1.6		mcd	I_F = 20mA Figs. 3,8,13,18
											At I_F = 25mA				
$2\theta_{1/2}$	Included Angle Between Half Luminous Intensity Points		60			70			70			70		deg.	Note 1. Figures 6, 11, 16, 21
λ_{PEAK}	Peak Wavelength		655			635			583			565		nm	Measurement at Peak
λ_d	Dominant Wavelength		640			626			585			570		nm	Note 2
τ_S	Speed of Response		10			200			200			200		ns	
C	Capacitance		200			35			35			35		pF	V_F=0; f=1 MHz
θ_{JC}	Thermal Resistance*		425			425			425			425		°C/W	Note 3
θ_{JC}	Thermal Resistance**		550			550			550			550		°C/W	Note 3
V_F	Forward Voltage		1.6	2.0		2.0	3.0		2.0	3.0		2.1	3.0	V	I_F = 20mA Figures 2, 7, 12, 17
												At I_F = 25mA			
BV_R	Reverse Breakdown Voltage	4	5		5.0			5.0			5.0			V	I_R = 100μA
η_v	Luminous Efficacy		56			140			455			600		lm/W	Note 4

NOTES:
1. $\theta_{1/2}$ is the off-axis angle at which the luminous intensity is half the axial luminous intensity.
2. The dominant wavelength, λ_d, is derived from the CIE chromaticity diagram and represents the single wavelength which defines the color of the device.
3. Junction to Cathode Lead with 3.18mm (0.125 inch) of leads exposed between base of flange and heat sink.
4. Radiant intensity, I_e, in watts/steradian, may be found from the equation $I_e = I_v/\eta_v$, where I_v is the luminous intensity in candelas and η_v is the luminous efficacy in lumens/watt.

*Panel mount.
**T0-46

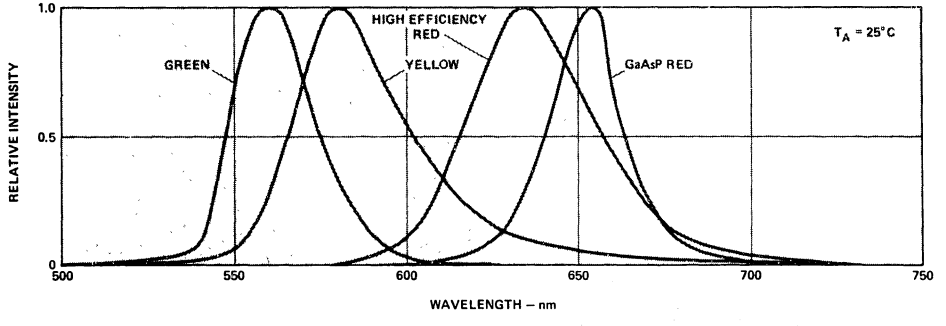
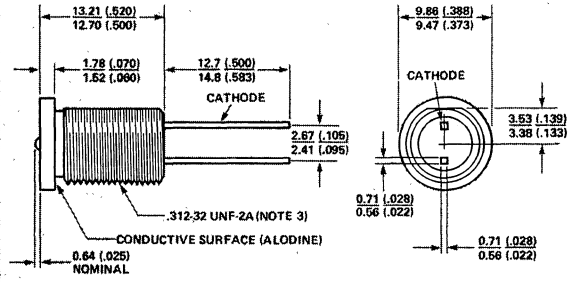


Figure 1. Relative Intensity vs. Wavelength.

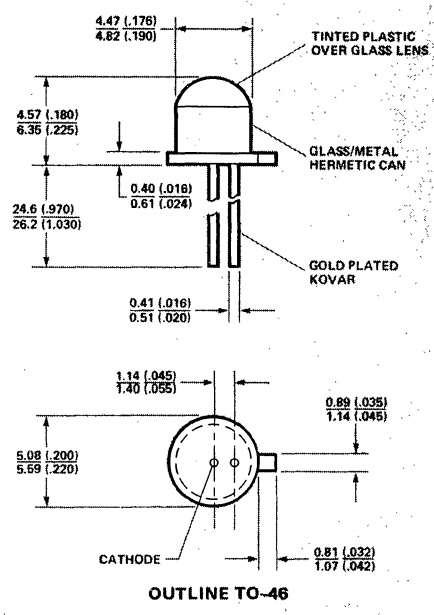
Package Dimensions

5082-4787, 4687, 4587, 4987



NOTES:
1. ALL EXTERNAL METAL SURFACES OF THE PACKAGE ARE BLACK ANODIZED EXCEPT FOR THE ALODINE AREA OF THE FLANGE AND THE GOLD PLATED LEADS.
2. MOUNTING HARDWARE WHICH INCLUDES ONE LOCK WASHER AND ONE HEX-NUT IS INCLUDED WITH EACH PANEL MOUNTABLE HERMETIC SOLID STATE LAMP.
3. USE OF METRIC DRILL SIZE 8.20 MILLIMETRES OR ENGLISH DRILL SIZE P (0.323 INCH) IS RECOMMENDED FOR PRODUCING HOLE IN THE PANEL FOR PANEL MOUNTING.
4. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).

1N5765, 1N6092, 1N6093, 1N6094



OUTLINE TO-46

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. GOLD-PLATED LEADS.

RED 1N5765/5082-4787

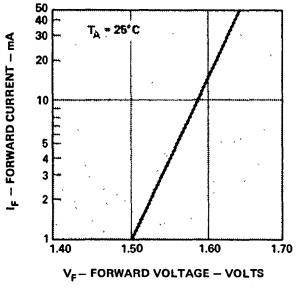


Figure 2. Forward Current vs. Forward Voltage.

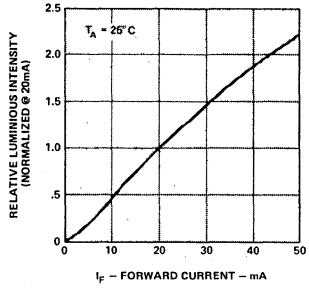


Figure 3. Relative Luminous Intensity vs. Forward Current.

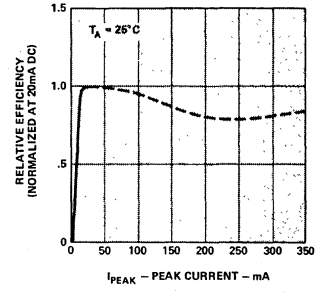


Figure 4. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

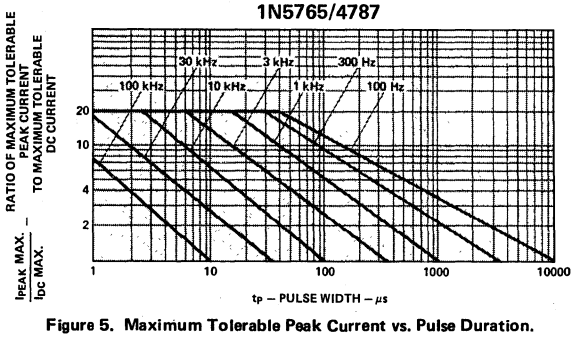


Figure 5. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

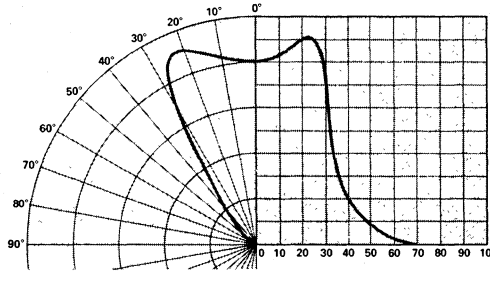


Figure 6. Relative Luminous Intensity vs. Angular Displacement.

HIGH EFFICIENCY RED 1N6092/5082-4687

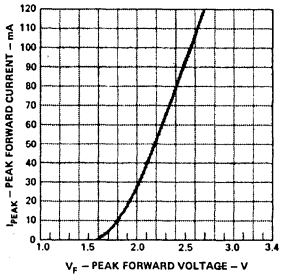


Figure 7. Forward Current vs. Forward Voltage.

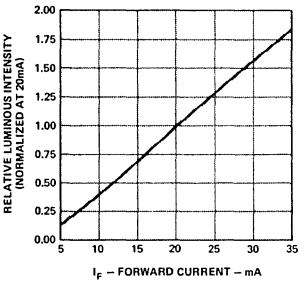


Figure 8. Relative Luminous Intensity vs. Forward Current.

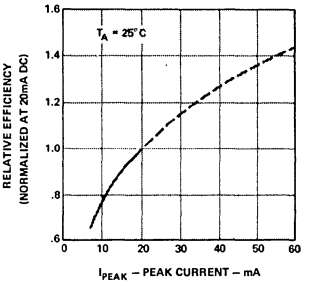


Figure 9. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

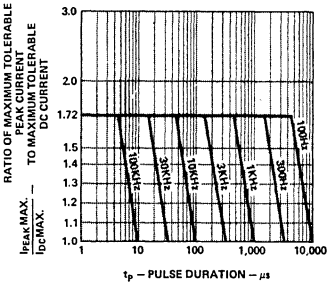


Figure 10. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

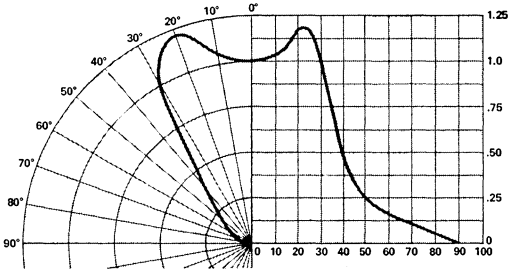


Figure 11. Relative Luminous Intensity vs. Angular Displacement.

YELLOW 1N6093/5082-4587

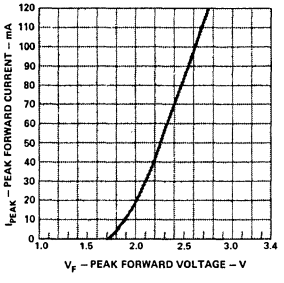


Figure 12. Forward Current vs. Forward Voltage.

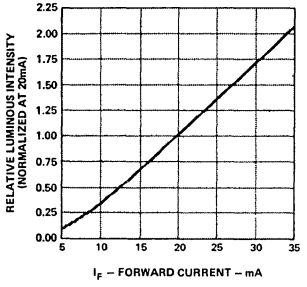


Figure 13. Relative Luminous Intensity vs. Forward Current.

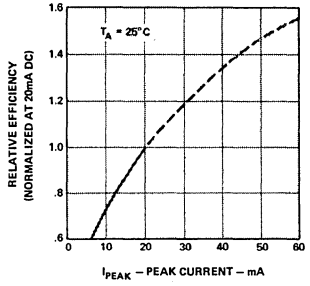


Figure 14. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

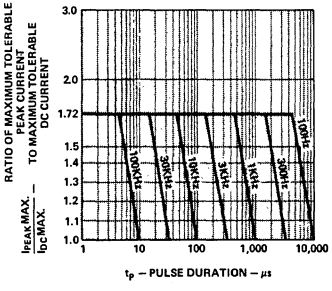


Figure 15. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

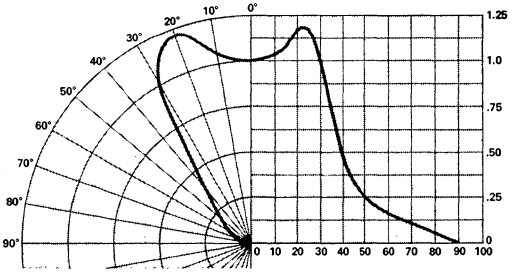


Figure 16. Relative Luminous Intensity vs. Angular Displacement.

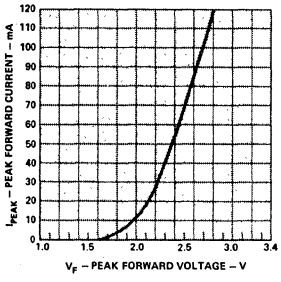


Figure 17. Forward Current vs. Forward Voltage.

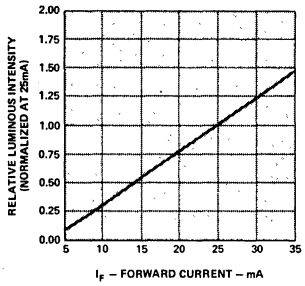


Figure 18. Relative Luminous Intensity vs. Forward Current.

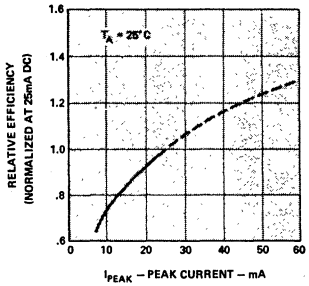


Figure 19. Relative Efficiency (Luminous Intensity per Unit Current) vs. Peak Current.

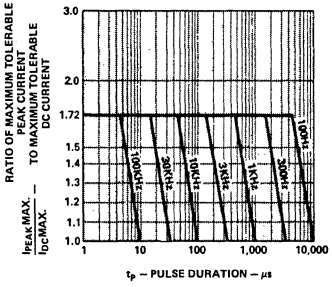


Figure 20. Maximum Tolerable Peak Current vs. Pulse Duration. (I_{DC} MAX as per MAX Ratings)

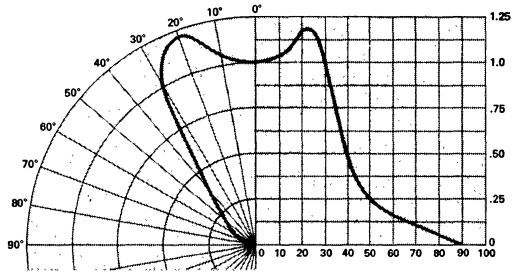


Figure 21. Relative Luminous Intensity vs. Angular Displacement.

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COMPONENTS

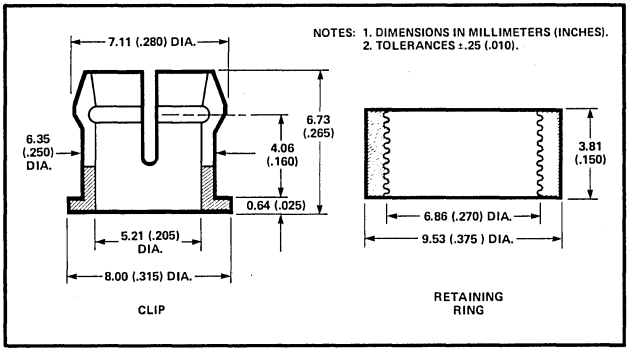
CLIP AND RETAINING RING FOR PANEL MOUNTED LEDs

5082-4707

TECHNICAL DATA APRIL 1979

Description

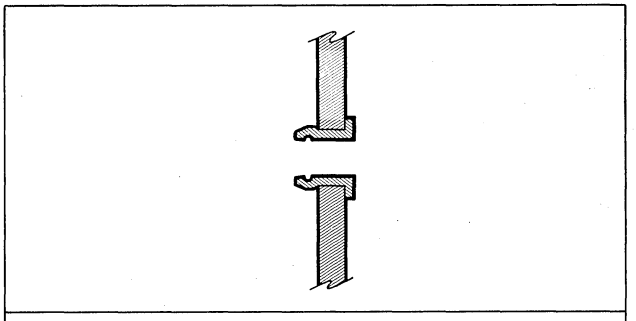
The 5082-4707 is a black plastic mounting clip and retaining ring. It is designed to panel mount Hewlett Packard Solid State high profile T - 1¾ size lamps. This clip and ring combination is intended for installation in instrument panels up to 3.18mm (.125") thick. For panels greater than 3.18mm (.125"), counterboring is required to the 3.18mm (.125") thickness.



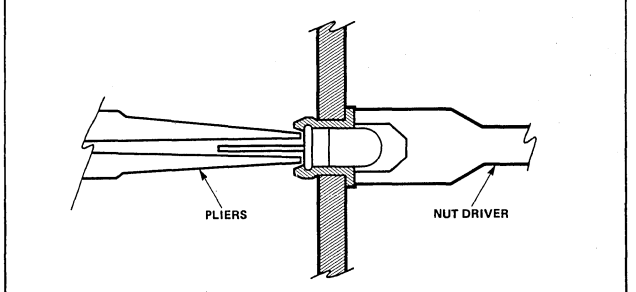
Mounting Instructions

1. Drill a 6.35mm (.250") dia. hole in the panel. Deburr but do not chamfer the edges of the hole.

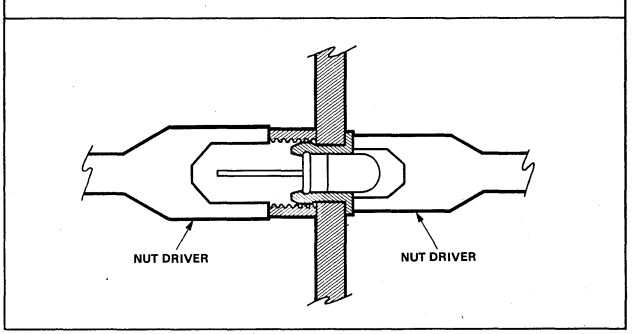
2. Press the panel clip into the hole from the front of the panel.



3. Press the LED into the clip from the back. Use blunt long nose pliers to push on the LED. Do not use force on the LED leads. A tool such as a nut driver may be used to press on the clip.



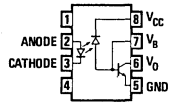
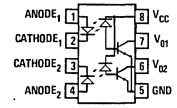
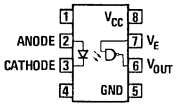
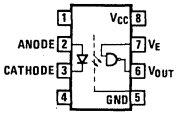
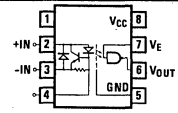
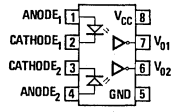
4. Slip a plastic retaining ring onto the back of the clip and press tight using tools such as two nut drivers.



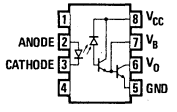
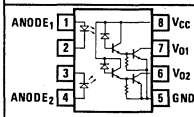
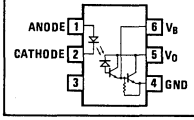
Optocouplers

Optoelectronics Designer's Catalog 1979

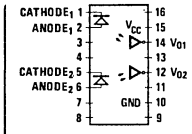
High Speed Optocouplers

Device		Description	Application[1]	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Input To Output Insulation	Page No.
	6N135 (5082-4350)	Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1M bit/s	7% Min.	16mA	3000Vdc[3]	186
	6N136 (5082-4351)				19% Min.			
	HCPL-2502 (5082-4352)				15-22%[2]			
	HCPL-2530 (5082-4354)	Dual Channel Transistor Output	Line Receiver, Analog Circuits, TTL/CMOS, TTL/LSTTL Ground Isolation	1M bit/s	7% Min.	16mA	3000Vdc[3]	190
	HCPL-2531 (5082-4355)				19% Min.			
	6N137 (5082-4360)	Optically Coupled Logic Gate	Line Receiver, High Speed Logic Ground Isolation	10M Bit/s	700% Typ.	5.0mA	3000Vdc[3]	194
	HCPL-2601 (5082-4361)	High Common Mode Rejection, Optically Coupled Logic Gate	Line Receiver, High Speed Logic Ground Isolation In High Ground or Induced Noise Environments	10M bit/s	700% Typ.	5.0mA	3000Vdc[3]	198
	HCPL-2602	Optically Coupled Line Receiver	Replace Conventional Line Receivers In High Ground or Induced Noise Environments	10M bit/s	700% Typ.	5.0mA	3000Vdc[3]	202
	HCPL-2630 (5082-4364)	Dual Channel Optically Coupled Gate	Line Receiver, High Speed Logic Ground Isolation	10M bit/s	700% Typ.	5.0mA	3000Vdc[3]	208

Low Input Current/High Gain Optocouplers

Device		Description	Application[1]	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Input To Output Insulation	Page No.
	6N138 (5082-4370)	Low Saturation Voltage, High Gain Output, V_{CC}=7VMax.	Line Receiver, Low Current Ground Isolation, TTL/TTL, LSTTL/TTL, CMOS/TTL	300k bit/s	300% Min.	1.6mA	3000Vdc[3]	212
	6N139 (5082-4371)	Low Saturation Voltage, High Gain Output, V_{CC}=18V Max.	Line Receiver, Ultra Low Current Ground Isolation, CMOS/LSTTL CMOS/TTL, CMOS/CMOS		400% Min.	0.5mA		
	HCPL-2730	Dual Channel, High Gain, V_{CC}=7V Max.	Line Receiver, Polarity Sensing, Low Current Ground Isolation	300k bit/s	300% Min.	1.6mA	3000Vdc[3]	216
	HCPL-2731	Dual Channel, High Gain, V_{CC}=18V Max.			400%Min.	0.5mA		
	4N45	Darlington Output V_{CC}=7V Max.	AC Isolation, Relay-Logic Isolation	3k bit/s	250% Min.	1.0mA	3000Vdc[3]	220
	4N46	Darlington Output V_{CC}=20V Max.			350% Min.	0.5mA		

High Reliability Optocouplers

Device		Description	Application[1]	Typical Data Rate (NRZ)	Current Transfer Ratio	Specified Input Current	Input To Output Insulation	Page No.
	6N134 (5082-4365) 6N134 TXV (TX-4365) 6N134 TXVB (TXB-4365)	Dual Channel Hermetically Sealed Optically Coupled Logic Gate. TXV – Screened TXVB – Screened with Group B Data	Line Receiver, Ground Isolation for High Reliability Systems	10M bit/s	400% Typ.	10mA	1500Vdc	224

Notes: 1. AN 948, AN 951-1, and AN 951-2 are located in Application Notes Section, beginning on page 247. For further information ask for AN 939 and AN 947.
2. The HCPL-2502 Current Transfer Ratio Specification is guaranteed to be 15% minimum and 22% maximum.
3. Recognized under the Component Recognition Program of Underwriters Laboratories Inc. (File No. E55361).

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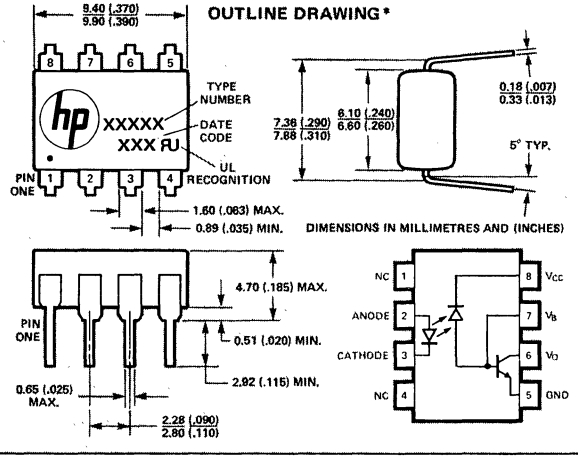
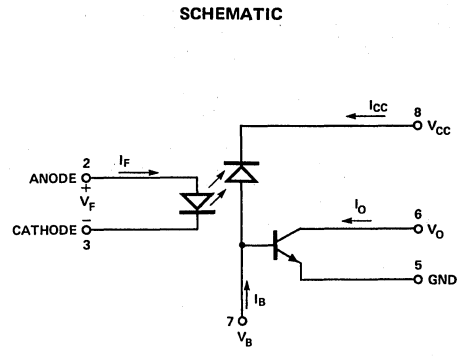
COMPONENTS

HIGH SPEED OPTOCOUPLERS

6N135
6N136
HCPL-2502

TECHNICAL DATA APRIL 1979





Features

- **HIGH SPEED: 1 Mbit/s**
- **TTL COMPATIBLE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**
- **HIGH COMMON MODE TRANSIENT IMMUNITY: 1000V/μs**
- **3000Vdc INSULATION VOLTAGE**
- **2 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUT**

Description

These diode-transistor optocouplers use a light emitting diode and an integrated photon detector to provide 3000V dc electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collector improve the speed up to a hundred times that of a conventional photo-transistor coupler by reducing the base-collector capacitance.

The 6N135 is suitable for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the 6N135 is 7% minimum at I_F = 16 mA.

The 6N136 is suitable for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR of the 6N136 is 19% minimum at I_F = 16 mA.

The HCPL-2502 is suitable for use in applications where matched or known CTR is desired. CTR is 15 to 22% at I_F = 16 mA.

*JEDEC Registered Data. (The HCPL-2502 is not registered.)

Applications

- **Line Receivers** — High common mode transient immunity (>1000V/μs) and low input-output capacitance (0.6pF).
- **High Speed Logic Ground Isolation** — TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Slow Phototransistor Isolators** — Pins 2-7 of the 6N135/6 series conform to pins 1-6 of 6 pin phototransistor couplers. Pin 8 can be tied to any available bias voltage of 1.5V to 15V for high speed operation.
- **Replace Pulse Transformers** — Save board space and weight.
- **Analog Signal Ground Isolation** — Integrated photon detector provides improved linearity over phototransistor type.

Absolute Maximum Ratings*

Storage Temperature	-55°C to +125°C
Operating Temperature	-55°C to 100°C
Lead Solder Temperature	260°C for 10s (1.6mm below seating plane)
Average Input Current — I_F	25mA[1]
Peak Input Current — I_F	50mA[2] (50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F	1.0A (≤1μs pulse width, 300pps)
Reverse Input Voltage — V_R (Pin 3-2)	5V
Input Power Dissipation	45mW[3]
Average Output Current — I_O (Pin 6)	8mA
Peak Output Current	16mA
Emitter-Base Reverse Voltage (Pin 5-7)	5V
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 6-5)	-0.5V to 15V
Base Current — I_B (Pin 7)	5mA
Output Power Dissipation	100mW[4]

See notes, following page.

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	6N135	7	18		%	I_F = 16mA, V_O = 0.4V, V_{CC} = 4.5V, T_A = 25°C	1,2	5
		6N136	19	24		%			
		HCPL-2502	15		22	%			
	CTR	6N135	5	13		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V		
		6N136	15	21		%			
Logic Low Output Voltage	V_{OL}	6N135		0.1	0.4	V	I_F = 16mA, I_O = 1.1mA, V_{CC} = 4.5V		
		6N136 HCPL-2502		0.1	0.4	V	I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}*			3	500	nA	I_F = 0mA, V_O = V_{CC} = 5.5V, T_A = 25°C	6	
				0.1	100	µA	I_F = 0mA, V_O = V_{CC} = 15V, T_A = 25°C		
	I_{OH}				250	µA	I_F = 0mA, V_O = V_{CC} = 15V		
Logic Low Supply Current	I_{CCL}			40		µA	I_F = 16mA, V_O = Open, V_{CC} = 15V		
Logic High Supply Current	I_{CCH}*			0.02	1	µA	I_F = 0mA, V_O = Open, V_{CC} = 15V, T_A = 25°C		
	I_{CCH}				2	µA	I_F = 0mA, V_O = Open, V_{CC} = 15V		
Input Forward Voltage	V_F*			1.5	1.7	V	I_F = 16mA, T_A = 25°C	3	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16mA		
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10µA, T_A = 25°C		
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		
Input-Output Insulation Leakage Current	I_{I-O}*				1.0	µA	45% Relative Humidity, t = 5s, V_{I-O} = 3000Vdc, T_A = 25°C		6
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		6
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		6
Transistor DC Current Gain	h_{FE}			175		—	V_O = 5V, I_O = 3mA		

**All typicals at T_A = 25°C.

Switching Specifications at T_A=25°C V_{CC} = 5V, I_F = 16mA, unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}*	6N135		0.5	1.5	µs	R_L = 4.1kΩ	5,9	8,9
		6N136 HCPL-2502		0.2	0.8	µs	R_L = 1.9kΩ		
Propagation Delay Time To Logic High at Output	t_{PLH}*	6N135		0.4	1.5	µs	R_L = 4.1kΩ	5,9	8,9
		6N136 HCPL-2502		0.3	0.8	µs	R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic High Level Output	CM_H	6N135		1000		V/µs	I_F = 0mA, V_{CM} = 10Vp-p, R_L = 4.1kΩ	10	7,8,9
		6N136 HCPL-2502		1000		V/µs	I_F = 0mA, V_{CM} = $10V_{p-p}$, R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic Low Level Output	CM_L	6N135		-1000		V/µs	V_{CM} = $10V_{p-p}$, R_L = 4.1kΩ	10	7,8,9
		6N136 HCPL-2502		-1000		V/µs	V_{CM} = $10V_{p-p}$, R_L = 1.9kΩ		
Bandwidth	BW			2		MH_z	R_L = 100Ω	8	10

NOTES:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 2.0mW/°C.
5. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
8. The 1.9kΩ load represents 1 TTL unit load of 1.6mA and the 5.6kΩ pull-up resistor.
9. The 4.1kΩ load represents 1 LSTTL unit load of 0.36mA and 6.1kΩ pull-up resistor.
10. The frequency at which the ac output voltage is 3dB below the low frequency asymptote.

*JEDEC Registered Data.

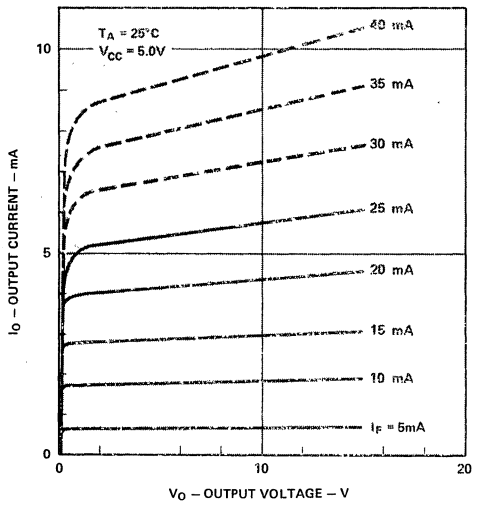


Figure 1. DC and Pulsed Transfer Characteristics.

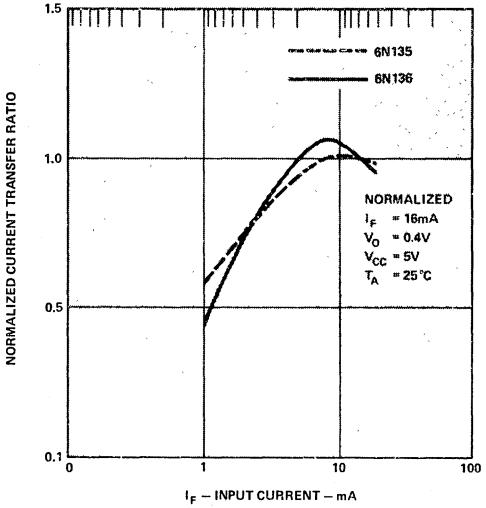


Figure 2. Current Transfer Ratio vs. Input Current.

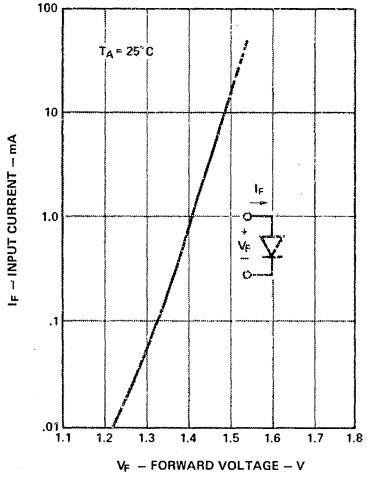


Figure 3. Input Current vs. Forward Voltage.

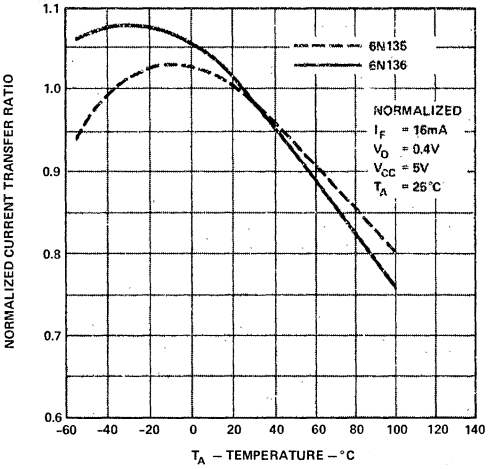


Figure 4. Current Transfer Ratio vs. Temperature.

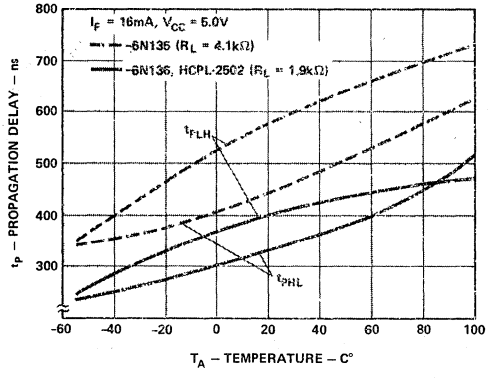


Figure 5. Propagation Delay vs. Temperature.

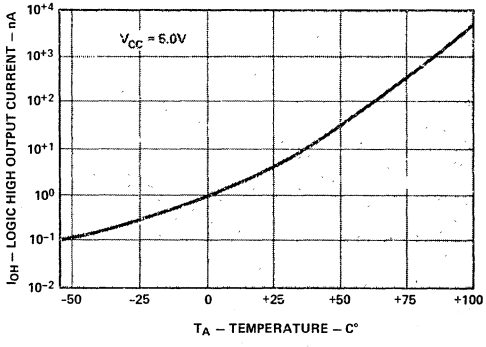


Figure 6. Logic High Output Current vs. Temperature.

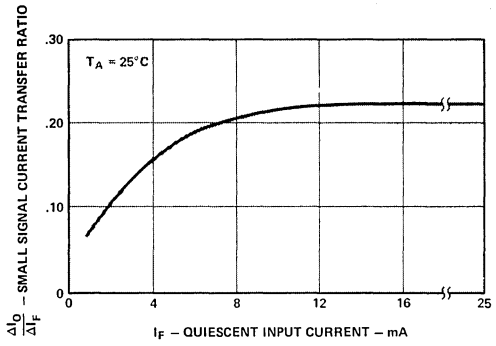
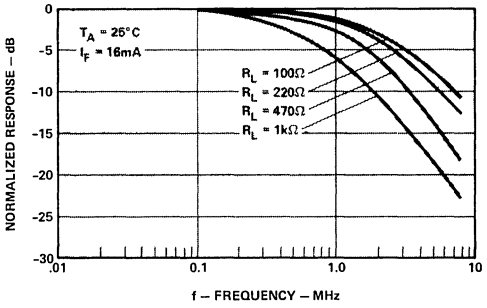


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.



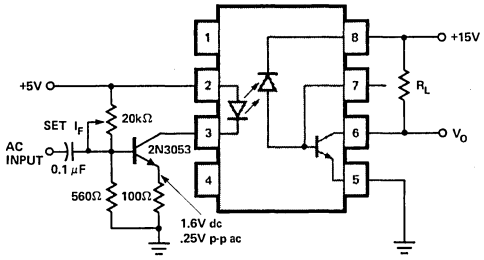


Figure 8. Frequency Response.

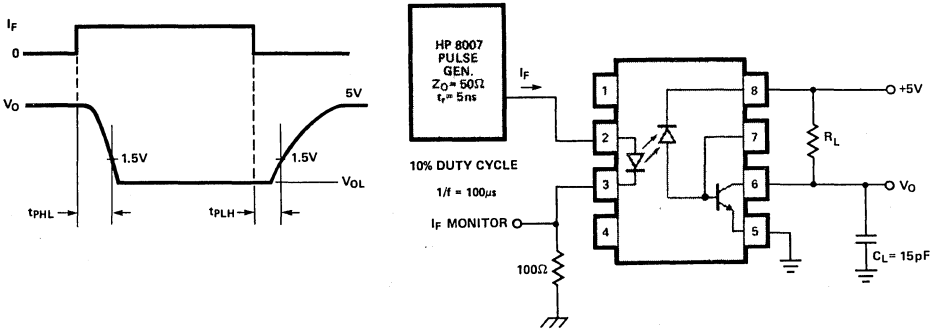


Figure 9. Switching Test Circuit.

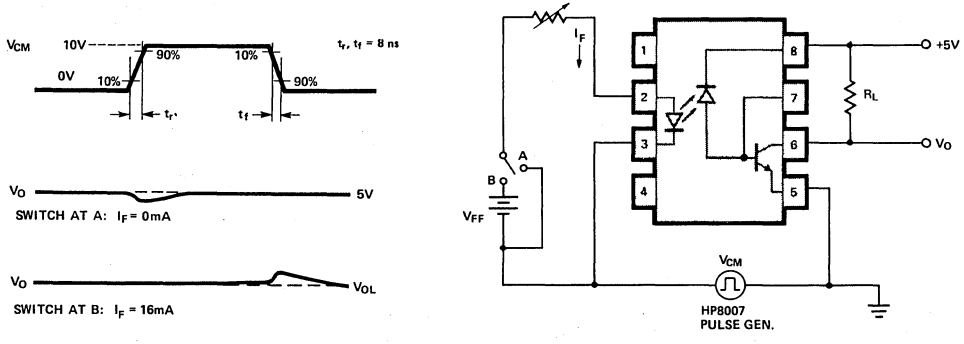


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

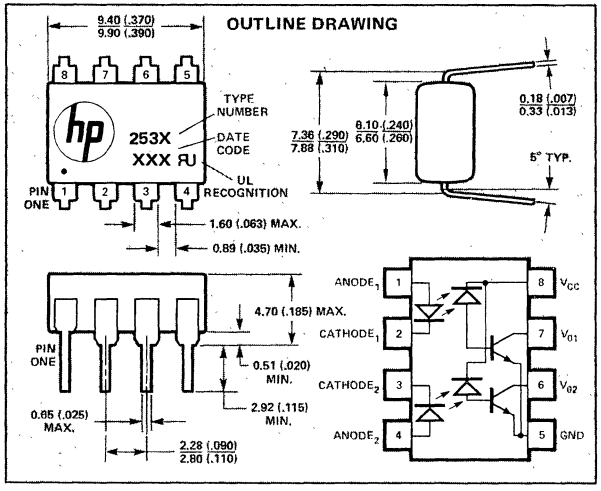
*JEDEC Registered Data.

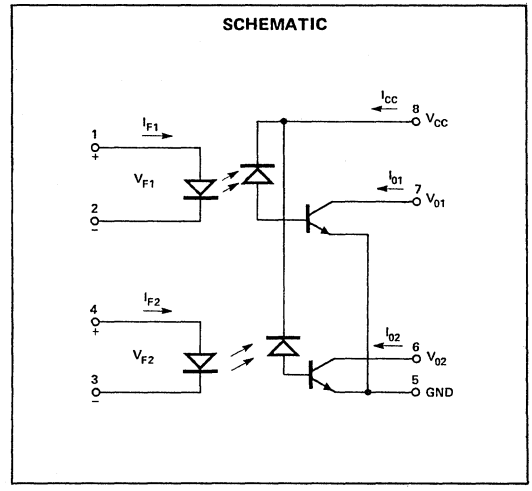
HEWLETT PACKARD
COMPONENTS

DUAL HIGH SPEED OPTOCOUPLER

HCPL-2530
HCPL-2531

TECHNICAL DATA APRIL 1979





Features

- **HIGH SPEED: 1 Mbit/s**
- **TTL COMPATIBLE**
- **HIGH COMMON MODE TRANSIENT IMMUNITY: >1000V/μs**
- **HIGH DENSITY PACKAGING**
- **3000Vdc INSULATION VOLTAGE**
- **3 MHz BANDWIDTH**
- **OPEN COLLECTOR OUTPUTS**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**

Applications

- **Line Receivers** – High common mode transient immunity (>1000V/μs) and low input-output capacitance (0.6pF).
- **High Speed Logic Ground Isolation** – TTL/TTL, TTL/LTTL, TTL/CMOS, TTL/LSTTL.
- **Replace Pulse Transformers** – Save board space and weight.
- **Analog Signal Ground Isolation** – Integrated photon detector provides improved linearity over phototransistor type.
- **Polarity Sensing.**
- **Isolated Analog Amplifier** – Dual channel packaging enhances thermal tracking.

Description

The HCPL-2530/31 dual couplers contain a pair of light emitting diodes and integrated photon detectors with 3000V dc electrical insulation between input and output. Separate connection for the photodiode bias and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

The HCPL-2530 is suitable for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications. Current transfer ratio (CTR) for the -2530 is 7% minimum at I_F = 16 mA.

The HCPL-2531 is suitable for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6kΩ pull-up resistor. CTR of the -2531 is 19% minimum at I_F = 16 mA.

Absolute Maximum Ratings

Storage Temperature . . . . . -55°C to +125°C
Operating Temperature . . . . . -55°C to +100°C
Lead Solder Temperature . . . . . 260°C for 10s
(1.6mm below seating plane)
Average Input Current – I_F (each channel) . . . . . 25mA[1]
Peak Input Current – I_F (each channel) . . . . . 50mA[2]
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current – I_F (each channel) . . . . 1.0 A
(≤1μs pulse width, 300pps)
Reverse Input Voltage – V_R (each channel) 5V
Input Power Dissipation (each channel) . . . . . 45mW[3]
Average Output Current – I_O (each channel) 8mA
Peak Output Current – I_O (each channel) 16mA
Supply and Output Voltage – V_{CC} (Pin 8-5), V_O (Pin 7,6-5)
. . . . . -0.5V to 15V
Output Power Dissipation (each channel) . . . . . 35mW[4]

See notes, following page.

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Sym.	Device HCPL	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	2530	7	18		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V, T_A = 25°C	1,2	5,6
		2531	19	24		%			
		2530	5	13		%	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V		
		2531	15	21		%			
Logic Low Output Voltage	V_{OL}	2530		0.1	0.5	V	I_F = 16mA, I_O = 1.1mA, V_{CC} = 4.5V, T_A = 25°C		5
		2531		0.1	0.5	V	I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V, T_A = 25°C		
Logic High Output Current	I_{OH}			3	500	nA	I_F = 0mA, V_O = V_{CC} = 5.5V, T_A = 25°C	6	5
					250	μA	I_F = 0mA, V_O = V_{CC} = 15V		5
Logic Low Supply Current	I_{CCL}			80		μA	I_{F1} = I_{F2} = 16mA, V_{O1} = V_{O2} = Open, V_{CC} = 15V		
Logic High Supply Current	I_{CCH}			0.05	4	μA	I_{F1} = I_{F2} = 0mA, V_{O1} = V_{O2} = Open, V_{CC} = 15V		
Input Forward Voltage	V_F			1.5	1.7	V	I_F = 16mA, T_A = 25°C	3	5
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.6		mV/°C	I_F = 16mA		5
Input Reverse Breakdown Voltage	V_R		5			V	I_F = 10μA, T_A = 25°C		5
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		5
Input – Output Insulation Leakage Current	I_{I-O}				1.0	μA	45% Relative Humidity, t = 5 s, V_{I-O} = 3000Vdc, T_A = 25°C		7
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		7
Input-Input Insulation Leakage Current	I_{I-I}			0.005		μA	45% Relative Humidity, t = 5 s, V_{I-I} = 500Vdc		8
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω	V_{I-I} = 500Vdc		8
Capacitance (Input-Input)	C_{I-I}			0.25		pF	f = 1MHz		8

**All typicals at 25°C.

Switching Specifications at T_A=25°C V_{CC} = 5V, I_F = 16mA, unless otherwise specified

Parameter	Sym.	Device HCPL-	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}	2530		0.3	1.5	μs	R_L = 4.1kΩ	5,9	10,11
		2531		0.2	0.8	μs	R_L = 1.9kΩ		
Propagation Delay Time to Logic High at Output	t_{PLH}	2530		0.4	1.5	μs	R_L = 4.1kΩ	5,9	10,11
		2531		0.3	0.8	μs	R_L = 1.9kΩ		
Common Mode Transient Immunity at Logic High Level Output	CM_H	2530		1000		V/μs	I_F =0mA, R_L=4.1kΩ, V_{CM}=10V_{p-p}	10	9,10,11
		2531		1000		V/μs	I_F=0mA, R_L=1.9kΩ, V_{CM}=10V_{p-p}		
Common Mode Transient Immunity at Logic Low Level Output	CM_L	2530		-1000		V/μs	V_{CM}=10V_{p-p}, R_L = 4.1kΩ	10	9,10,11
		2531		-1000		V/μs	V_{CM} = 10V_{p-p}, R_L = 1.9kΩ		
Bandwidth	BW			3		MHz	R_L = 100Ω	8	12

NOTES:
1. Derate linearly above 70°C free-air temperature at a rate of 0.8mA/°C.
2. Derate linearly above 70°C free-air temperature at a rate of 1.6mA/°C.
3. Derate linearly above 70°C free-air temperature at a rate of 0.9mW/°C.
4. Derate linearly above 70°C free-air temperature at a rate of 1.0mW/°C.
5. Each channel.
6. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
10. The 1.9kΩ load represents 1 TTL unit load of 1.6mA and the 5.6kΩ pull-up resistor.
11. The 4.1kΩ load represents 1 LSTTL unit load of 0.36mA and 6.1kΩ pull-up resistor.
12. The frequency at which the ac output voltage is 3dB below the low frequency asymptote.

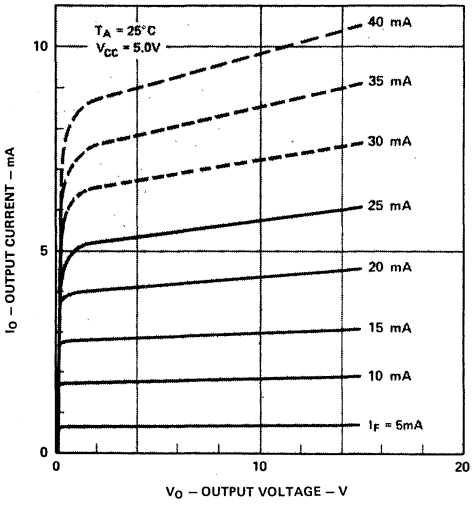


Figure 1. DC and Pulsed Transfer Characteristics.

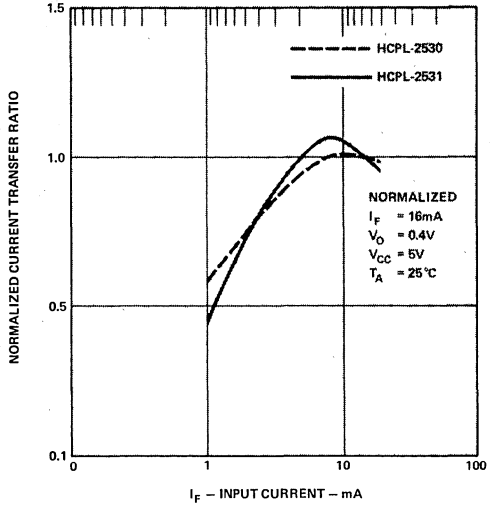


Figure 2. Current Transfer Ratio vs. Input Current.

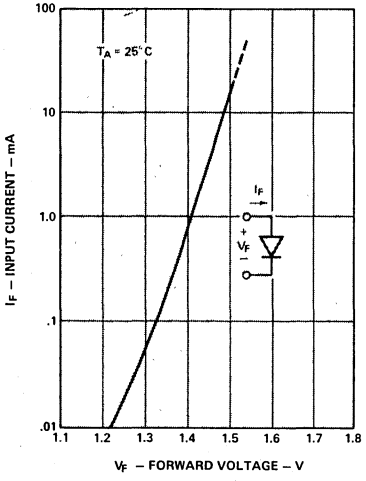


Figure 3. Input Current vs. Forward Voltage.

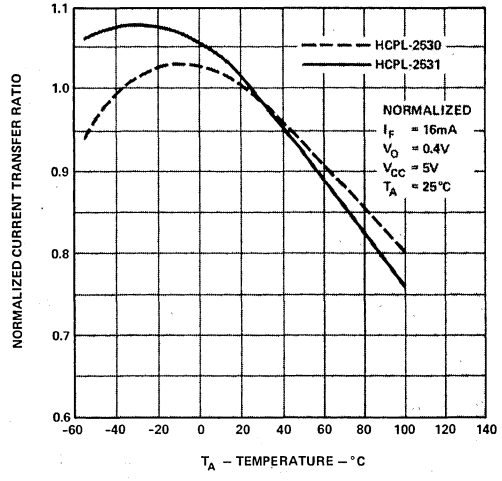


Figure 4. Current Transfer Ratio vs. Temperature.

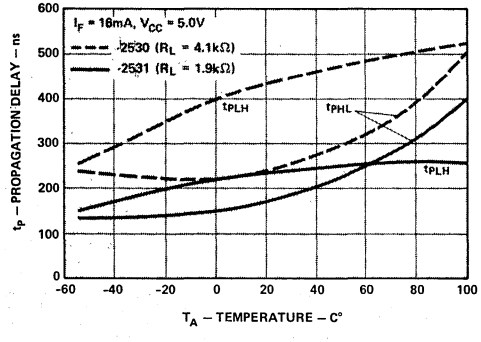


Figure 5. Propagation Delay vs. Temperature.

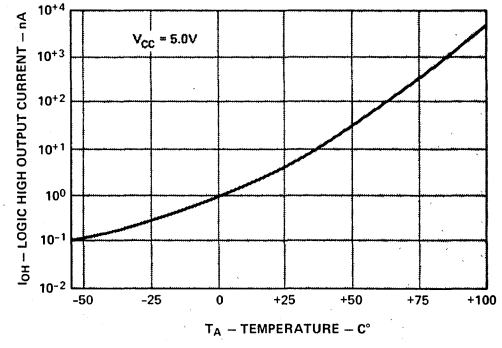


Figure 6. Logic High Output Current vs. Temperature.

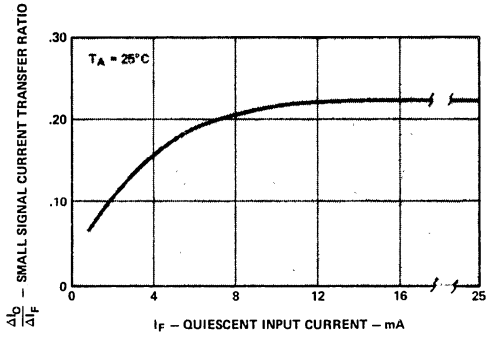


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.

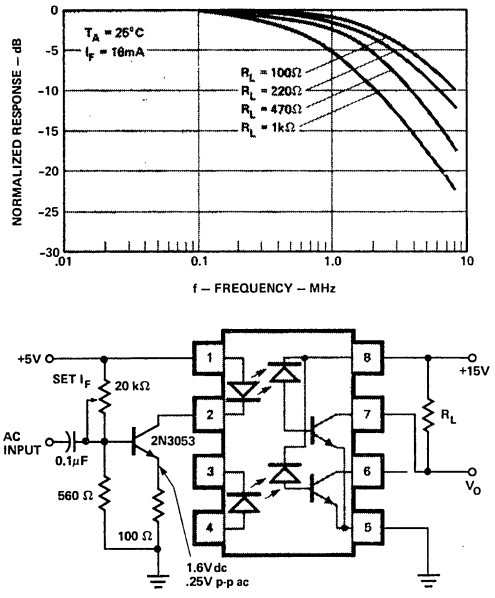


Figure 8. Frequency Response.

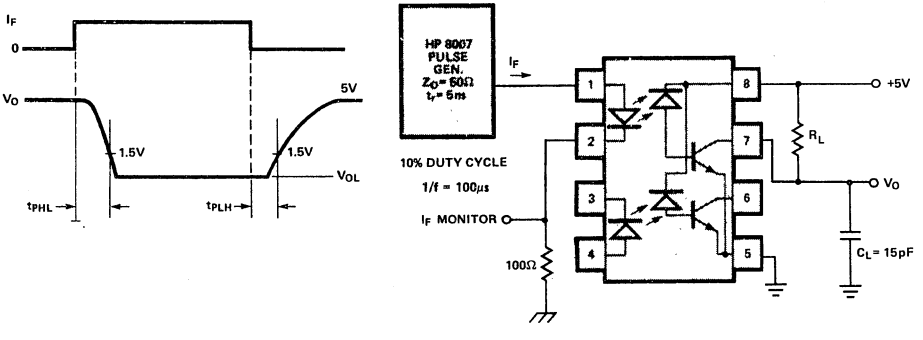


Figure 9. Switching Test Circuit.

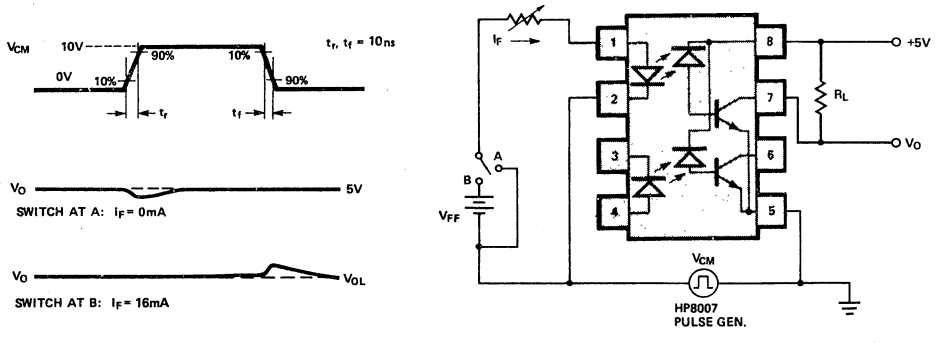


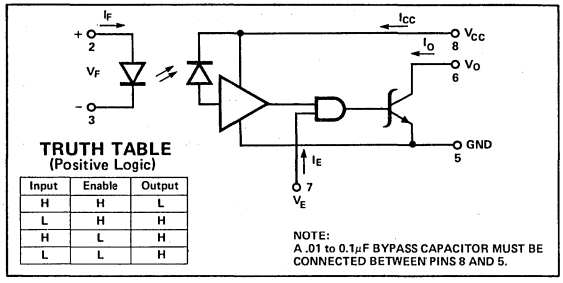
Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

HEWLETT PACKARD
COMPONENTS

LSTTL/TTL COMPATIBLE OPTOCOUPLER

6N137

TECHNICAL DATA APRIL 1979



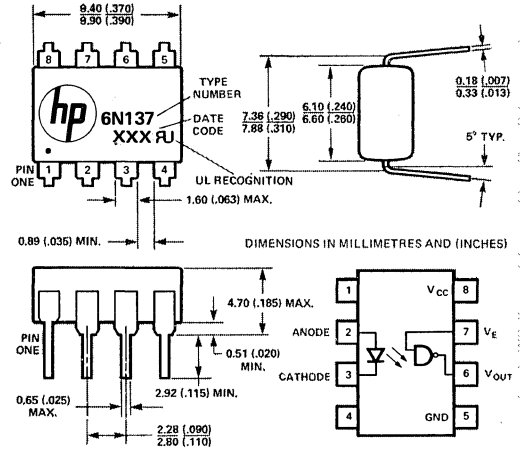
TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

NOTE:
A .01 to 0.1μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5.

Figure 1.

OUTLINE DRAWING*



Features

- **LSTTL/TTL COMPATIBLE: 5V SUPPLY**
- **ULTRA HIGH SPEED**
- **LOW INPUT CURRENT REQUIRED**
- **HIGH COMMON MODE REJECTION**
- **GUARANTEED PERFORMANCE OVER TEMPERATURE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**
- **3000V dc INSULATION VOLTAGE**

Description Applications

The 6N137 consists of a GaAsP photon emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. The circuit is temperature, current and voltage compensated.

This unique isolator design provides maximum DC and AC circuit isolation between input and output while achieving LSTTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5mA will sink an eight gate fan-out (13mA) at the output with 5 volt V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 45ns. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with LSTTL/TTL interfacing and a propagation delay of 25ns typical.

The 6N137 can be used in high speed digital interfacing applications where common mode signals must be rejected, such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished in system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

The open collector output provides capability for bussing, OR'ing and strobing.

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	6.3**	15	mA
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage (Output High)	V_{EL}	0	0.8	V
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings*

(No derating required up to 70°C)

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10s
(1.6mm below seating plane)
Peak Forward Input Current ..... 40mA (1≤ 1msec Duration)
Average Forward Input Current 20mA
Reverse Input Voltage 5V
Enable Input Voltage 5.5V
(Not to exceed V_{CC} by more than 500mV)
Supply Voltage - V_{CC} ..... 7V (1 Minute Maximum)
Output Current - I_O 50mA
Output Collector Power Dissipation 85mW
Output Voltage - V_O 7V

**6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

*JEDEC Registered Data.

Electrical Characteristics

OVER RECOMMENDED TEMPERATURE (T_A = 0°C TO 70°C) UNLESS OTHERWISE NOTED

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}*		50	250	μA	V_{CC}=5.5V, V_O=5.5V, I_F=250μA, V_E=2.0V	6	
Low Level Output Voltage	V_{OL}*		0.5	0.6	V	V_{CC}=5.5V, I_F=5mA, V_{EH}=2.0V I_{OL} (Sinking) =13mA	3,5	
High Level Enable Current	I_{EH}		-1.0		mA	V_{CC}=5.5V, V_E=2.0V		
Low Level Enable Current	I_{EL}*		-1.6	-2.0	mA	V_{CC}=5.5V, V_E=0.5V		
High Level Supply Current	I_{CCH}*		7	15	mA	V_{CC}=5.5V, I_F=0 V_E=0.5V		
Low Level Supply	I_{CCL}*		13	18	mA	V_{CC}=5.5V, I_F=10mA V_E=0.5V		
Input-Output Insulation Leakage Current	I_{I-O}*			1.0	μA	Relative Humidity=45% T_A=25°C, t=5s V_{I-O}=3000Vdc		5
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O}=500V, T_A=25°C		5
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f=1MHz, T_A=25°C		5
Input Forward Voltage	V_F*		1.5	1.75	V	I_F=10mA, T_A=25°C	4	8
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R=10μA, T_A=25°C		
Input Capacitance	C_{IN}		60		pF	V_F=0, f=1MHz		
Current Transfer Ratio	CTR		700		%	I_F=5.0mA, R_L=100Ω	2	7

**All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics at T_A=25°C, V_{CC}=5V

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}*		45	75	ns	R_L=350Ω, C_L=15pF, I_F=7.5mA	7,9	1
Propagation Delay Time to Low Output Level	t_{PHL}*		45	75	ns	R_L=350Ω, C_L=15pF, I_F=7.5mA	7,9	2
Output Rise-Fall Time (10-90%)	t_r, t_f		25		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA		
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		25		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA, V_{EH}=3.0V, V_{EL}=0.5V	8	3
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		15		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA V_{EH}=3.0V, V_{EL}=0.5V	8	4
Common Mode Transient Immunity at Logic High Output Level	CM_H		50		v/μs	V_{CM}=10V R_L=350Ω, V_O(min.)=2V, I_F=0mA	11	6
Common Mode Transient Immunity at Logic Low Output Level	CM_L		-150		v/μs	V_{CM}=10V R_L=350Ω, V_O(max.)=0.8V, I_F=5mA	11	6

*JEDEC Registered Data.

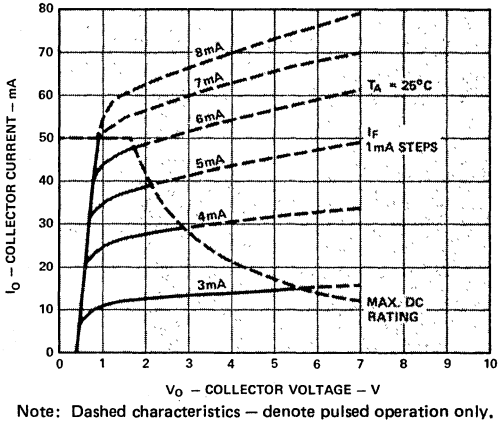
Operating Procedures and Definitions

Logic Convention. The 6N137 is defined in terms of positive logic.

Bypassing. A ceramic capacitor (.01 to 0.1μF) should be connected from pin 8 to pin 5 (Figure 12). Its purpose is to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between capacitor and coupler should not exceed 20mm.

Polarities. All voltages are referenced to network ground (pin 5). Current flowing toward a terminal is considered positive.

Enable Input. No external pull-up required for a logic (1), i.e., can be open circuit.



Note: Dashed characteristics — denote pulsed operation only.

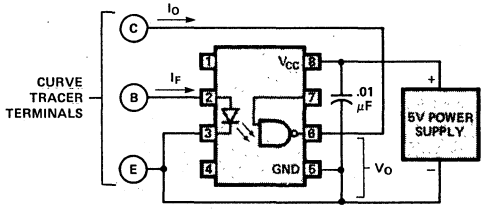
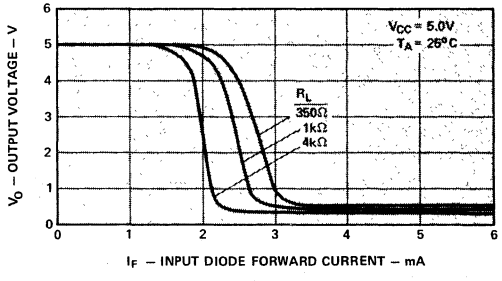


Figure 2. Optocoupler Collector Characteristics.



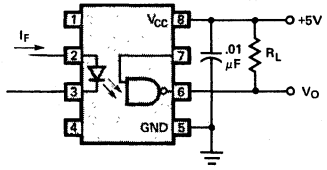


Figure 3. Input-Output Characteristics.

NOTES:

1. The t_{PLH} propagation delay is measured from the 3.75mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
2. The t_{PHL} propagation delay is measured from the 3.75mA point on the leading edge of the input pulse to 1.5V point on the leading edge of the output pulse.
3. The t_{ELH} enable propagation delay is measured from the 1.5V point of the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
4. The t_{EHL} enable propagation delay is measured from the 1.5V point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
5. Device considered a two terminal device: pins 2 and 3 shorted together, and pins 5, 6, 7, and 8 shorted together.
6. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O>2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O<0.8V).
7. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
8. At 10mA V_F decreases with increasing temperature at the rate of 1.6mV/°C.

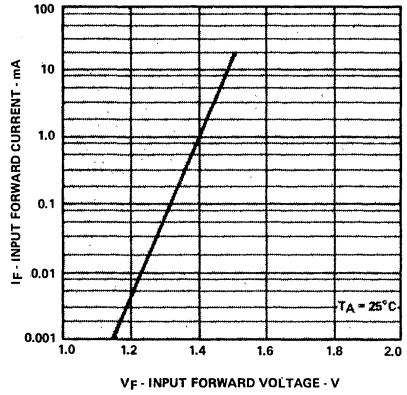


Figure 4. Input Diode Forward Characteristic.

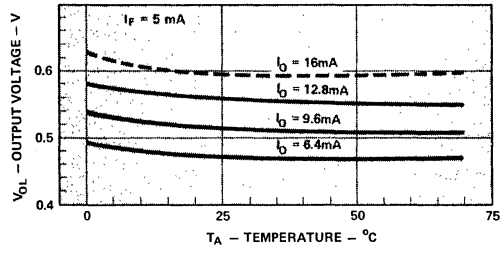


Figure 5. Output Voltage, V_{OL} vs. Temperature and Fan-Out.

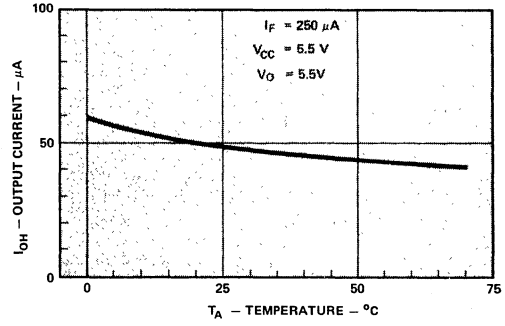


Figure 6. Output Current, I_{OH} vs. Temperature (I_F=250μA).

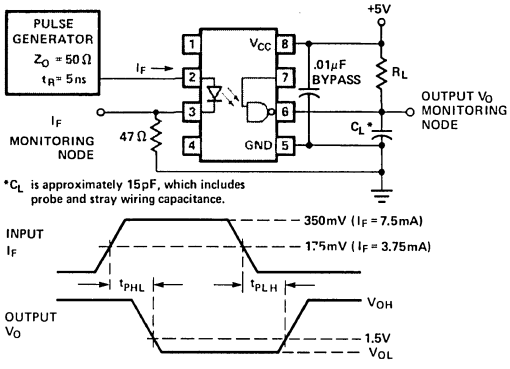


Figure 7. Test Circuit for t_{PHL} and t_{PLH}.**

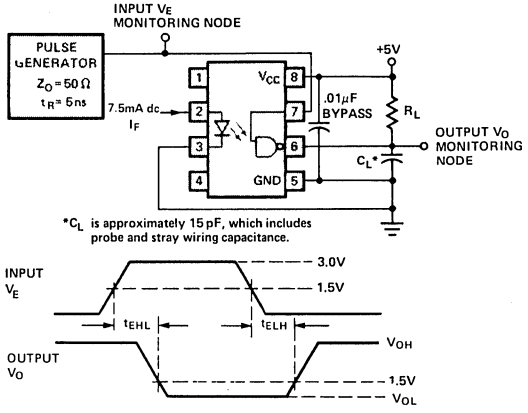


Figure 8. Test Circuit for t_{ELH} and t_{EHL}.

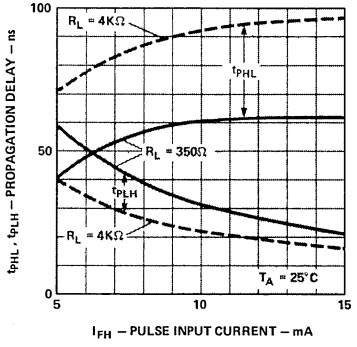


Figure 9. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.

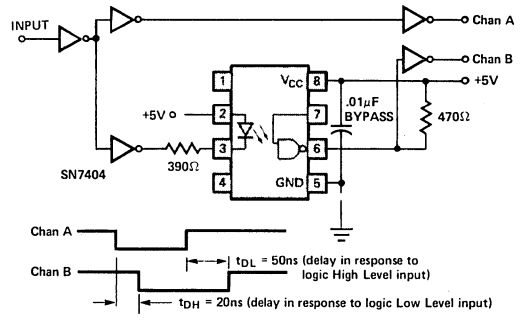
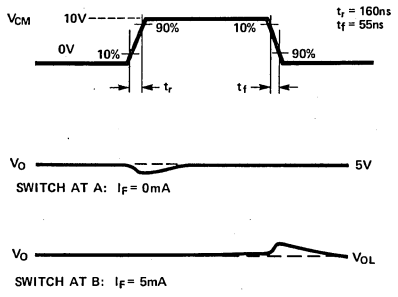


Figure 10. Response Delay Between TTL Gates.



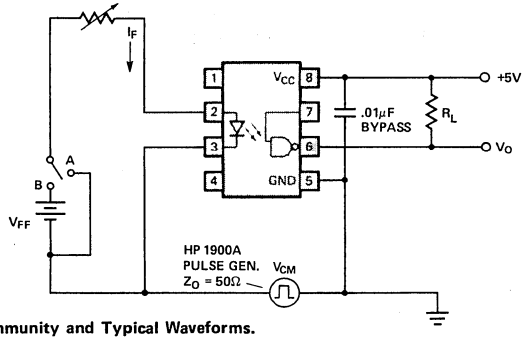


Figure 11. Test Circuit for Transient Immunity and Typical Waveforms.

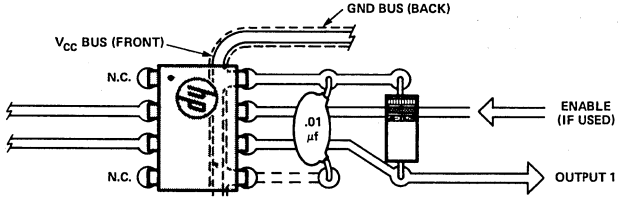


Figure 12. Recommended Printed Circuit Board Layout.

** JEDEC Registered Data.

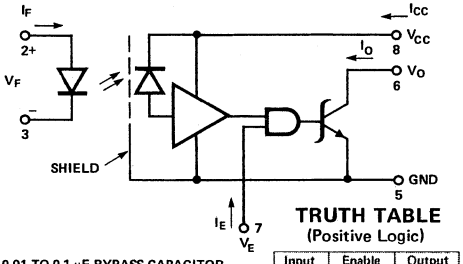
HEWLETT hp PACKARD

COMPONENTS

HIGH CMR, HIGH SPEED OPTOCOUPLER

HCPL - 2601

TECHNICAL DATA APRIL 1979

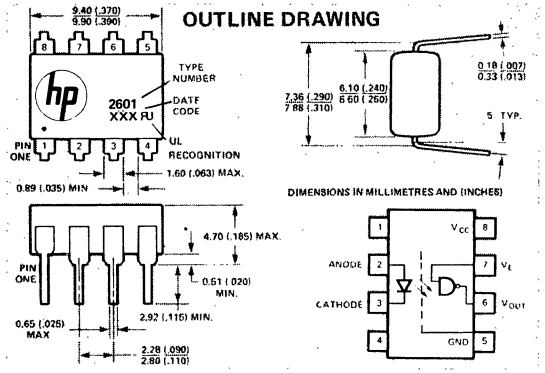


A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5 (See Note 1).

Figure 1. Schematic.

TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H



Features

- **INTERNAL SHIELD FOR HIGH COMMON MODE REJECTION (CMR)**
- **HIGH SPEED**
- **GUARANTEED MINIMUM COMMON MODE TRANSIENT IMMUNITY: 1000V/μs**
- **LSTTL/TTL COMPATIBLE**
- **LOW INPUT CURRENT REQUIRED: 5mA**
- **GUARANTEED PERFORMANCE OVER TEMPERATURE: 0°C to 70°C**
- **STROBABLE OUTPUT**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**
- **3000 Vdc INSULATION VOLTAGE**

Description

The HCPL-2601 optically coupled gate combines a GaAsP light emitting diode and an integrated high gain photon detector. An enable input allows the detector to be strobed. The output of the detector I.C. is an open collector Schottky clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 1000 volts/μsec., equivalent to rejecting a 300 volt P-P sinusoid at 1 MHz.

This unique design provides maximum D.C. and A.C. circuit isolation while achieving TTL compatibility. The isolator D.C. operational parameters are guaranteed from 0°C to 70°C allowing troublefree system performance. This isolation is achieved with a typical propagation delay of 35 nsec.

The HCPL-2601's are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Applications

- Isolated Line Receiver
- Simplex/Multiplex Data Transmission
- Computer-Peripheral Interface
- Microprocessor System Interface
- Digital Isolation for A/D, D/A Conversion
- Switching Power Supply
- Instrument Input/Output Isolation
- Ground Loop Elimination
- Pulse Transformer Replacement

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level	I_{FL}	0	250	μA
Input Current, High Level	I_{FH}	6.3*	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings

(No Derating Required up to 70°C)

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6mm below seating plane)
Forward Input Current − I_F (see Note 2) ..... 20 mA
Reverse Input Voltage ..... 5 V
Supply Voltage − V_{CC} ..... 7V (1 Minute Maximum)
Enable Input Voltage − V_E ..... 5.5 V
(Not to exceed V_{CC} by more than 500 mV)
Output Collector Current − I_O ..... 25 mA
Output Collector Power Dissipation ..... 40 mW
Output Collector Voltage − V_O ..... 7 V

*6.3 mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

Electrical Characteristics

(Over Recommended Temperature, T_A = 0°C to +70°C, Unless Otherwise Noted)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		7	250	μA	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250 μA, V_E = 2.0 V	2	
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC} = 5.5V, I_F = 5 mA V_E = 2.0 V, I_{OL} (Sinking) = 13 mA	3,5	
High Level Supply Current	I_{CCH}		10	15	mA	V_{CC} = 5.5V, I_F = 0, V_E = 0.5 V		
Low Level Supply Current	I_{CCL}		15	18	mA	V_{CC} = 5.5V, I_F = 10 mA, V_E = 0.5 V		
Low Level Enable Current	I_{EL}		−1.6	−2.0	mA	V_{CC} = 5.5 V, V_E = 0.5 V		
High Level Enable Current	I_{EH}		−1.0		mA	V_{CC} = 5.5 V, V_E = 2.0V		
High Level Enable Voltage	V_{EH}	2.0			V			11
Low Level Enable Voltage	V_{EL}			0.8	V			
Input Forward Voltage	V_F		1.5	1.75	V	I_F = 10 mA, T_A = 25°C	4	
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10 μA, T_A = 25°C		
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1 MHz		
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		−1.6		mV/°C	I_F = 10 mA		
Input-Output Insulation Leakage Current	I_{I-O}			1	μA	Relative Humidity = 45% T_A = 25°C, t = 5 s, V_{I-O} = 3000 Vdc		3
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500 V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

*All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics (T_A = 25°C, V_{CC} = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output level	t_{PLH}		35	75	ns	R_L = 350 Ω, C_L = 15 pF, I_F = 7.5 mA	6	4
Propagation Delay Time to Low Output Level	t_{PHL}		35	75	ns		6	5
Output Rise Time (10–90%)	t_r		25		ns			
Output Fall Time (90–10%)	t_f		15		ns			
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		25		ns	R_L = 350 Ω, C_L = 15 pF, I_F = 7.5 mA, V_{EH} = 3 V, V_{EL} = 0 V	9	6
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		15		ns	R_L = 350 Ω, C_L = 15 pF, I_F = 7.5 mA, V_{EH} = 3 V, V_{EL} = 0 V	9	7
Common Mode Transient Immunity at High Output Level	CM_H	1000	10,000		V/μs	V_{CM} = 50 V (peak), V_O (min.) = 2 V, R_L = 350 Ω, I_F = 0 mA	12	8,10
Common Mode Transient Immunity at Low Output Level	CM_L	−1000	−10,000		V/μs	V_{CM} = 50 V (peak), V_O (max.) = 0.8 V, R_L = 350 Ω, I_F = 7.5 mA	12	9,10

NOTES:

1. Bypassing of the power supply line is required, with a 0.01 μF ceramic disc capacitor adjacent to each isolator as illustrated in Figure 15. The power supply bus for the isolator(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
6. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
7. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
8. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} >2.0 V).
9. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} <0.8 V).
10. For sinusoidal voltages, $\left(\frac{|dv_{CM}|}{dt}\right)_{max} = \pi f_{CM} V_{CM}$ (p-p)
11. No external pull up is required for a high logic state on the enable input.

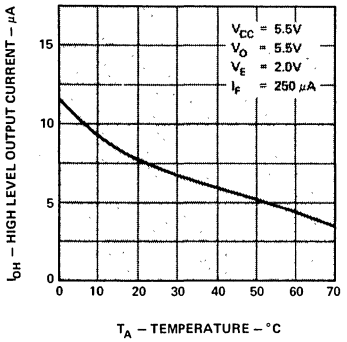


Figure 2. High Level Output Current vs. Temperature.

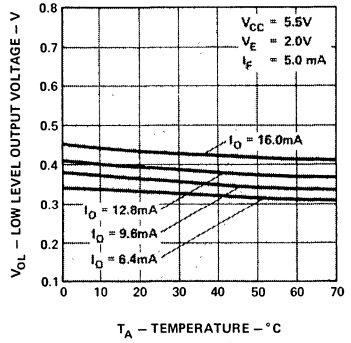


Figure 3. Low Level Output Voltage vs. Temperature.

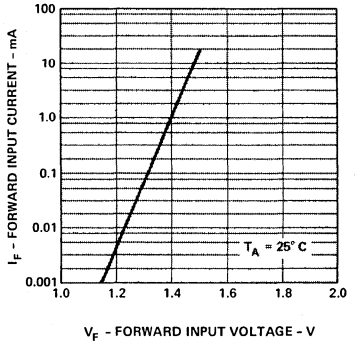


Figure 4. Input Diode Forward Characteristic.

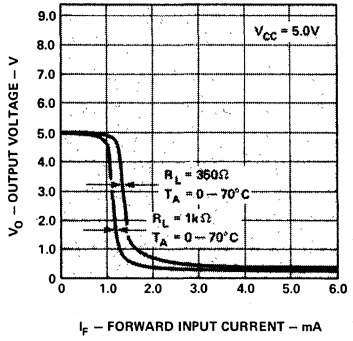


Figure 5. Output Voltage vs. Forward Input Current.

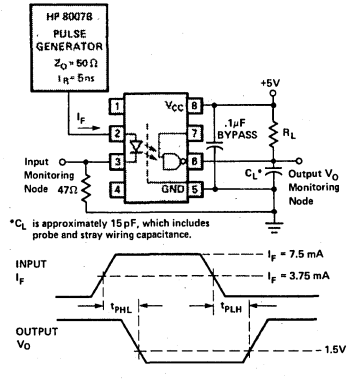


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

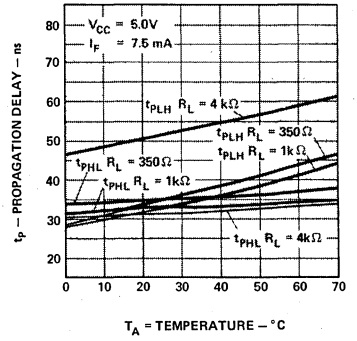


Figure 7. Propagation Delay vs. Temperature.

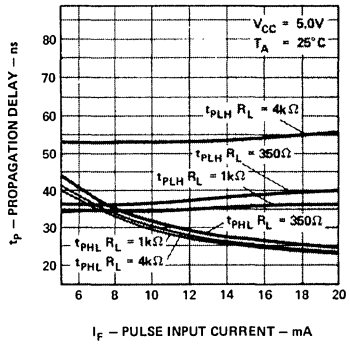


Figure 8. Propagation Delay vs. Pulse Input Current.

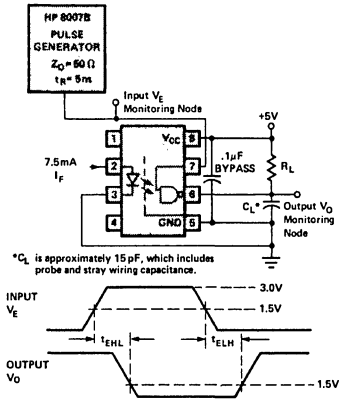


Figure 9. Test Circuit for t_{EHL} and t_{ELH}.

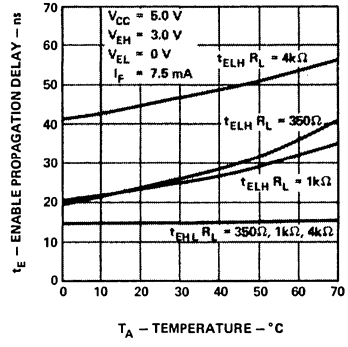


Figure 10. Enable Propagation Delay vs. Temperature.

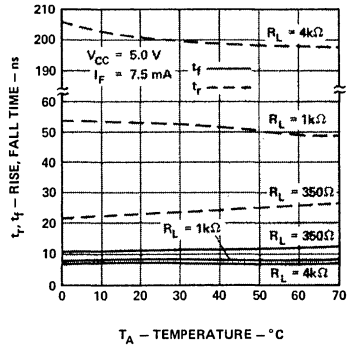


Figure 11. Rise, Fall Time vs. Temperature.

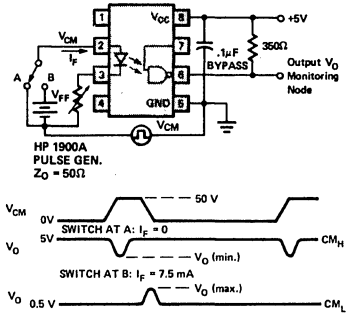


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

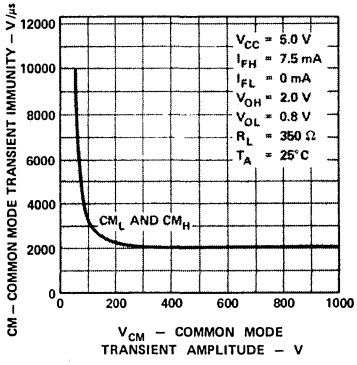


Figure 13. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

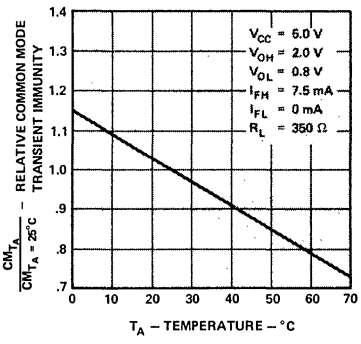


Figure 14. Relative Common Mode Transient Immunity vs. Temperature.

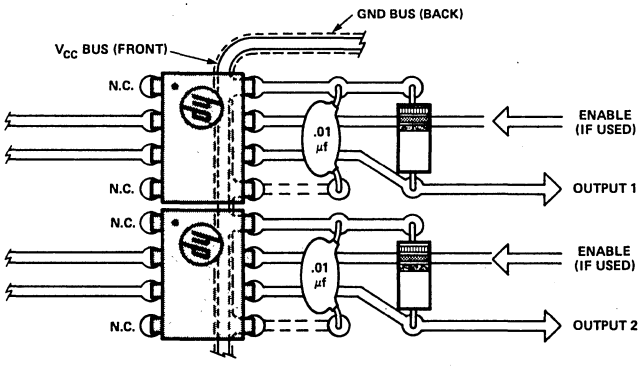


Figure 15. Recommended Printed Circuit Board Layout.

OPTO-COUPLERS

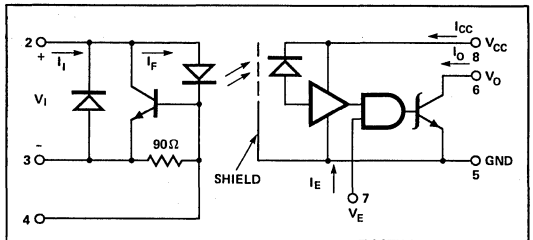
HEWLETT PACKARD

COMPONENTS

HIGH CMR LINE RECEIVER OPTOCOUPLER

HCPL-2602

TECHNICAL DATA APRIL 1979



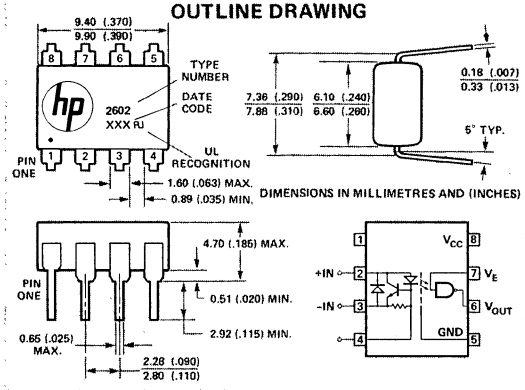
A 0.01 TO 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 8 AND 5 (See Note 1).

Figure 1. Schematic.

TRUTH TABLE
(Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

OUTLINE DRAWING



Features

- **LINE TERMINATION INCLUDED — NO EXTRA CIRCUITRY REQUIRED**
- **ACCEPTS A BROAD RANGE OF DRIVE CONDITIONS**
- **GUARDBANDED FOR LED DEGRADATION**
- **LED PROTECTION MINIMIZES LED EFFICIENCY DEGRADATION**
- **HIGH SPEED — 10Mbs (LIMITED BY TRANSMISSION LINE IN MANY APPLICATIONS)**
- **INTERNAL SHIELD PROVIDES EXCELLENT COMMON MODE REJECTION**
- **EXTERNAL BASE LEAD ALLOWS "LED PEAKING" AND LED CURRENT ADJUSTMENT**
- **3000 Vdc INSULATION VOLTAGE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**

Applications

- **Isolated Line Receiver**
- **Simplex/Multiplex Data Transmission**
- **Computer-Peripheral Interface**
- **Microprocessor System Interface**
- **Digital Isolation for A/D, D/A Conversion**
- **Current Sensing**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**

Description

The HCPL-2602 optically coupled line receiver combines a GaAsP light emitting diode, an input current regulator and an integrated high gain photon detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance.

The regulator allows a typical LED current of 8.5 mA before it starts to shunt excess current. The output of the detector IC is an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of 1000V/μsec, equivalent to rejecting a 300V P-P sinusoid at 1 MHz.

DC specifications are defined similar to TTL logic and are guaranteed from 0° C to 70° C allowing trouble free interfacing with digital logic circuits. An input current of 5 mA will sink an eight gate fan-out (TTL) at the output with a typical propagation delay from input to output of only 45 nsec.

The HCPL-2602's are useful as line receivers in high noise environments that conventional line receivers cannot tolerate. The higher LED threshold voltage provides improved immunity to differential noise and the internally shielded detector provides orders of magnitude improvement in common mode rejection with little or no sacrifice in speed.

Electrical Characteristics

(Over Recommended Temperature, T_A = 0°C to +70°C, Unless Otherwise Noted)

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		7	250	μA	V_{CC} = 5.5V, V_O = 5.5V I_I=250 μA, V_E=2.0V	4	
Low Level Output Voltage	V_{OL}		0.4	0.6	V	V_{CC}=5.5V, I_I=5 mA V_E=2.0V, I_{OL} (Sinking)=13 mA	2,5	2
Input Voltage	V_I		2.0	2.4	V	I_I=5 mA	3	
			2.3	2.7		I_I=60 mA	3	
Input Reverse Voltage	V_R		0.75	0.95	V	I_R=5 mA		
Low Level Enable Current	I_{EL}		-1.6	-2.0	mA	V_{CC}=5.5V, V_E=0.5V		
High Level Enable Current	I_{EH}		-1.0		mA	V_{CC}=5.5V, V_E=2.0V		
High Level Enable Voltage	V_{EH}	2.0			V			11
Low Level Enable Voltage	V_{EL}			0.8	V			
High Level Supply Current	I_{CCH}		10	15	mA	V_{CC}=5.5V, I_I=0, V_E=0.5V		
Low Level Supply Current	I_{CCL}		16	19	mA	V_{CC}=5.5V, I_I=60 mA V_E=0.5V		
Input Capacitance	C_{IN}		90		pF	V_I=0, f=1 MHz, (PIN 2-3)		
Input-Output Insulation Leakage Current	I_{I-O}			1	μA	Relative Humidity=45% T_A=25°C, t=5 s, V_{I-O}=3000 Vdc		3
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O}=500V		3
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1 MHz		3

*All typical values are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics

(T_A = 25°C, V_{CC} = 5V)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}		45	75	ns	R_L = 350 Ω C_L = 15 pF I_I = 7.5 mA	6	4
Propagation Delay Time to Low Output Level	t_{PHL}		45	75	ns		6	5
Output Rise Time (10-90%)	t_r		25		ns			
Output Fall Time (90-10%)	t_f		15		ns			
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		25		ns	R_L=350Ω, C_L=15 pF, I_I=7.5 mA, V_{EH}=3 V, V_{EL}=0 V	10	6
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		15		ns		10	7
Common Mode Transient Immunity at High Output Level	CM_H	1000	10,000		V/μs	V_{CM}=50 V (peak), V_O (min.)=2 V, R_L=350Ω, I_I=0 mA	12	8
Common Mode Transient Immunity at Low Output Level	CM_L	-1000	-10,000		V/μs	V_{CM}=50 V (peak), V_O (max.)=0.8 V, R_L=350Ω, I_I=7.5 mA	12	9

Using the HCPL-2602 Line Receiver Optocoupler

The primary objectives to fulfill when connecting an optocoupler to a transmission line are to provide a minimum, but not excessive, LED current and to properly terminate the line. The internal regulator in the HCPL-2602 simplifies this task. Excess current from variable drive conditions such as line length variations, line driver differences and power supply fluctuations are shunted by the regulator. In fact, with the LED current regulated, the line current can be increased to improve the immunity of the system to differential-mode-noise and to enhance the data rate capability. The designer must keep in mind the 60 mA input current maximum rating of the HCPL-2602, in such cases, and may need to use series limiting or shunting to prevent overstress.

Design of the termination circuit is also simplified; in most cases the transmission line can simply be connected directly to the input terminals of the HCPL-2602 without the need for additional series or shunt resistors. If reversing line drive is used it may be desirable to use two HCPL-2602's, or an external Schottky diode to optimize data rate.

Polarity Non-Reversing Drive

High data rates can be obtained with the HCPL-2602 with polarity non-reversing drive. Figure (a) illustrates how a 74S140 line driver can be used with the HCPL-2602 and shielded, twisted pair or coax cable without any additional components. There are some reflections due to the "active termination" but they do not interfere with circuit performance because the regulator clamps the line voltage. At longer line lengths t_{PLH} increases faster than t_{PHL} since the switching threshold is not exactly halfway between asymptotic line conditions. If optimum data rate is desired, a series resistor and peaking capacitor can be used to equalize t_{PLH} and t_{PHL}. In general, the peaking capacitance should be as large as possible; however, if it is too large it may keep the regulator from achieving turn-off during the negative (or zero) excursions of the input signal. A safe rule:

make $C \leqslant 16t$
where C = peaking capacitance in picofarads
t = data bit interval in nanoseconds

Polarity Reversing Drive

A single HCPL-2602 can also be used with polarity reversing drive (Figure b). Current reversal is obtained by way of the substrate isolation diode (substrate to collector). Some reduction of data rate occurs, however, because the substrate diode stores charge, which must be removed when the current changes to the forward direction. The effect of this is a longer t_{PHL}. This effect can be eliminated and data rate improved considerably by use of a Schottky diode on the input of the HCPL-2602.

For optimum noise rejection as well as balanced delays a split-phase termination should be used along with a flip-flop at the output (Figure c). The result of current reversal in split-phase operation is seen in Figure (c) with switches A and B both OPEN. The coupler inputs are then connected in ANTI-SERIES; however, because of the higher steady-state termination voltage, in comparison to the single HCPL-2602 termination, the forward current in the substrate diode is lower and consequently there is less junction charge to deal with when switching.

Closing switch B with A open is done mainly to enhance common mode rejection, but also reduces propagation delay slightly because line-to-line capacitance offers a slight peaking effect. With switches A and B both CLOSED, the shield acts as a current return path which prevents either input substrate diode from becoming reversed biased. Thus the data rate is optimized as shown in Figure (c).

Improved Noise Rejection

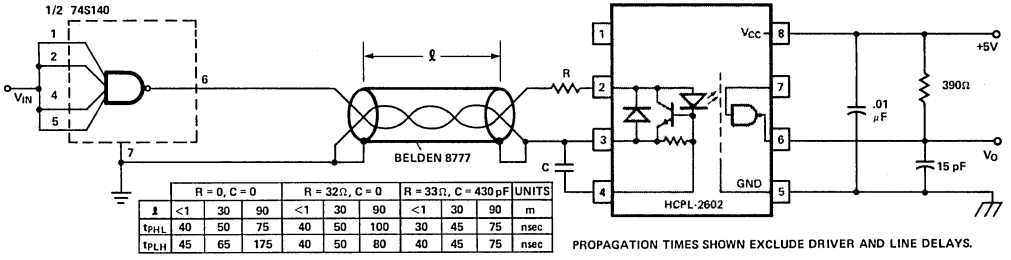
Use of additional logic at the output of two HCPL-2602's operated in the split phase termination, will greatly improve system noise rejection in addition to balancing propagation delays as discussed earlier.

A NAND flip-flop offers infinite common mode rejection (CMR) for NEGATIVELY sloped common mode transients but requires $t_{PHL} > t_{PLH}$ for proper operation. A NOR flip-flop has infinite CMR for POSITIVELY sloped transients but requires $t_{PHL} < t_{PLH}$ for proper operation. An exclusive-OR flip-flop has infinite CMR for common mode transients of EITHER polarity and operates with either $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$.

With the line driver and transmission line shown in Figure (c), $t_{PHL} > t_{PLH}$, so NAND gates are preferred in the R-S flip-flop. A higher drive amplitude or different circuit configuration could make $t_{PHL} < t_{PLH}$, in which case NOR gates would be preferred. If it is not known whether $t_{PHL} > t_{PLH}$ or $t_{PHL} < t_{PLH}$, or if the drive conditions may vary over the boundary for these conditions, the exclusive-OR flip-flop of Figure (d) should be used.

RS-422 and RS-423

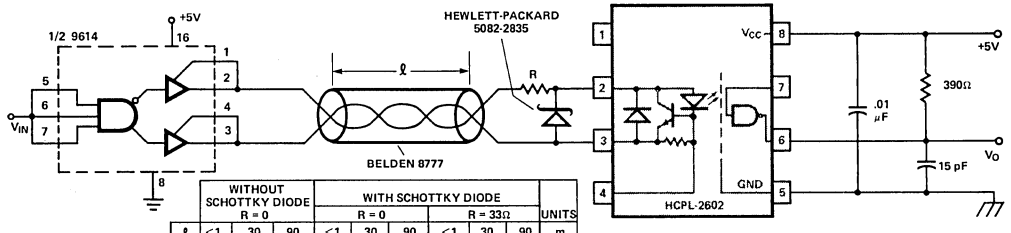
Line drivers designed for RS-422 and RS-423 generally provide adequate voltage and current for operating the HCPL-2602. Most drivers also have characteristics allowing the HCPL-2602 to be connected directly to the driver terminals. Worst case drive conditions, however, would require current shunting to prevent overstress of the HCPL-2602.



	R = 0, C = 0			R = 32Ω, C = 0			R = 33Ω, C = 430 pF			UNITS
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	40	50	75	40	50	100	30	45	75	nsec
t_{PLH}	45	65	175	40	50	80	40	45	75	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

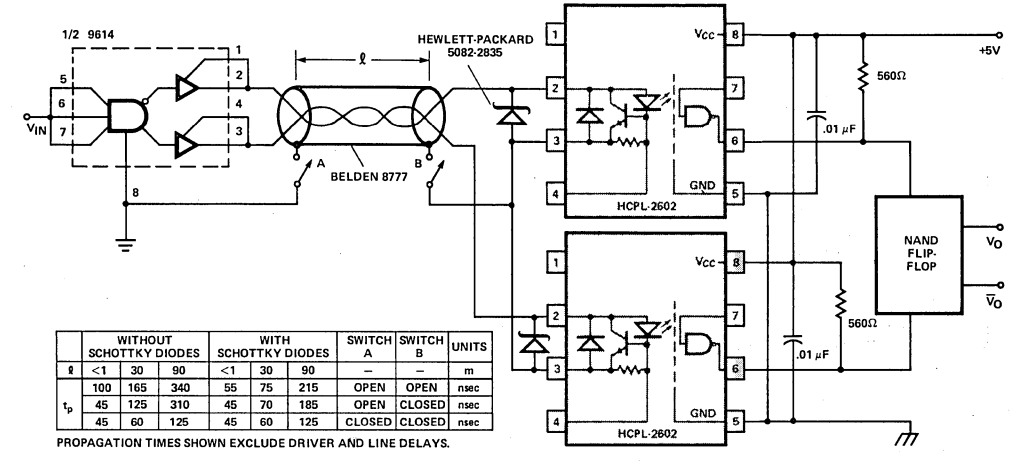
Figure a. Polarity Non-Reversing.



	WITHOUT SCHOTTKY DIODE R = 0			WITH SCHOTTKY DIODE R = 0			WITH SCHOTTKY DIODE R = 33Ω			UNITS
ℓ	<1	30	90	<1	30	90	<1	30	90	m
t_{PHL}	210	365	450	50	80	235	50	70	200	nsec
t_{PLH}	35	45	60	35	45	60	35	45	60	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

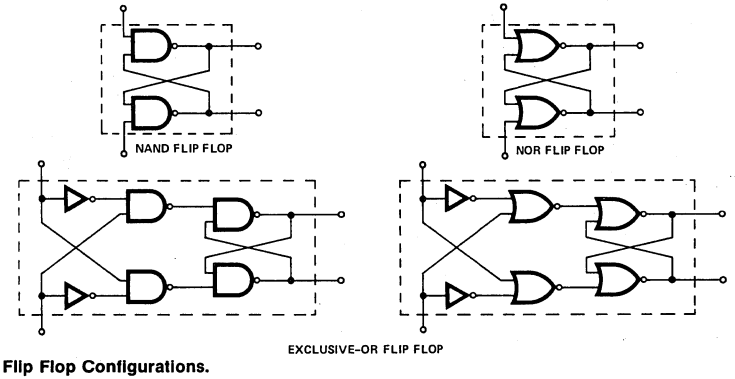
Figure b. Polarity Reversing, Single Ended.



	WITHOUT SCHOTTKY DIODES			WITH SCHOTTKY DIODES			SWITCH A	SWITCH B	UNITS
ℓ	<1	30	90	<1	30	90	–	–	m
t_p	100	165	340	55	75	215	OPEN	OPEN	nsec
	45	125	310	45	70	185	OPEN	CLOSED	nsec
	45	60	125	45	60	125	CLOSED	CLOSED	nsec

PROPAGATION TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

Figure c. Polarity Reversing, Split Phase.



NAND flip flop tolerates simultaneously HIGH inputs; NOR flip flop tolerates simultaneously LOW inputs; EXCLUSIVE-OR flip flop tolerates simultaneously HIGH OR LOW inputs without causing either of the outputs to change.

Figure d. Flip Flop Configurations.

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level	I_{IL}	0	250	μA
Input Current, High Level	I_{IH}	5	60	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage	V_{EL}	0	0.8	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6mm below seating plane)
Forward Input Current — I_I ..... 60 mA
Reverse Input Current ..... 60 mA
Supply Voltage — V_{CC} ..... 7V (1 Minute Maximum)
Enable Input Voltage — V_E ..... 5.5 V
(Not to exceed V_{CC} by more than 500 mV)
Output Collector Current — I_O ..... 25 mA
Output Collector Power Dissipation ..... 40 mW
Output Collector Voltage — V_O ..... 7 V
Input Current, Pin 4 ..... ±10 mA

NOTES:

1. Bypassing of the power supply line is required, with a 0.01 μF ceramic disc capacitor adjacent to each isolator as illustrated in Figure 15. The power supply bus for the isolator(s) should be separate from the bus for any active loads, otherwise a larger value of bypass capacitor (up to 0.1 μF) may be needed to suppress regenerative feedback via the power supply.
2. The HCPL-2602 is tested such that operation at I_I minimum of 5 mA will provide the user a minimum of 20% guardband for LED light output degradation.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
5. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
6. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5 V point on the trailing edge of the output pulse.
7. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5 V point on the leading edge of the output pulse.
8. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_{OUT} >2.0 V).
9. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_{OUT} <0.8 V).
10. For sinusoidal voltages, $\left(\frac{|dv_{CM}|}{dt}\right)_{max} = \pi f_{CM} V_{CM}$ (p-p)
11. No external pull up is required for a high logic state on the enable input.

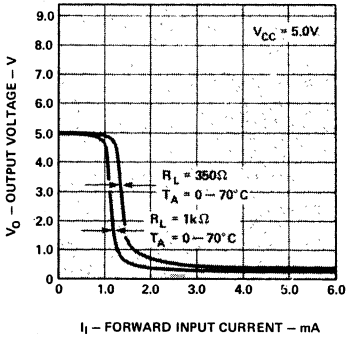


Figure 2. Output Voltage vs. Forward Input Current.

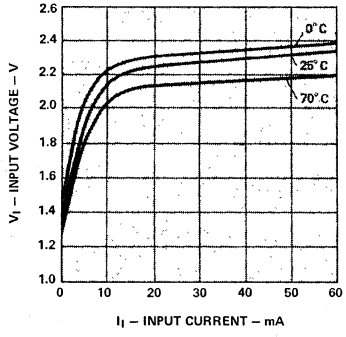


Figure 3. Input Characteristics.

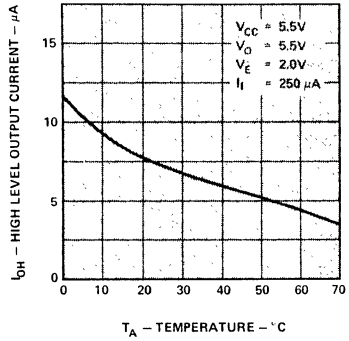


Figure 4. High Level Output Current vs. Temperature.

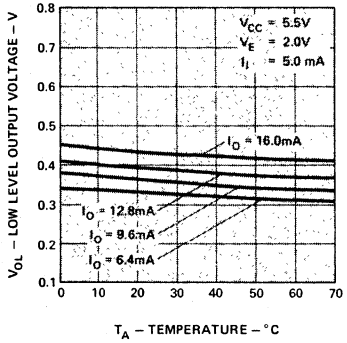


Figure 5. Low Level Output Voltage vs. Temperature.

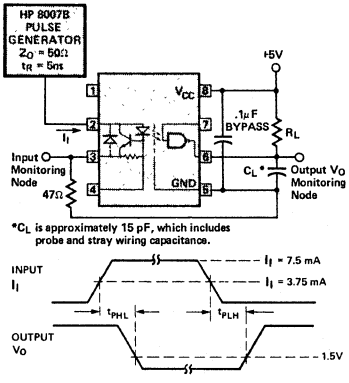


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

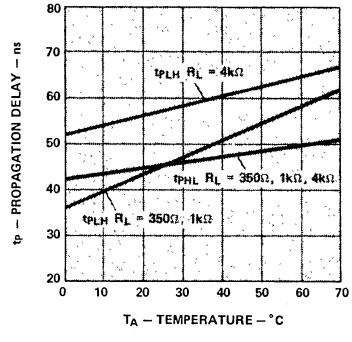


Figure 7. Propagation Delay vs. Temperature.

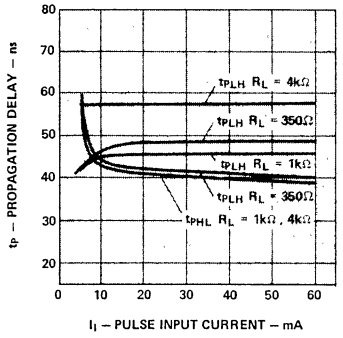


Figure 8. Propagation Delay vs. Pulse Input Current.

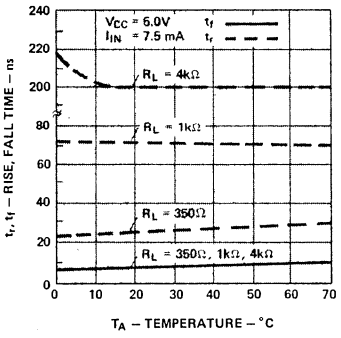


Figure 9. Rise, Fall Time vs. Temperature.

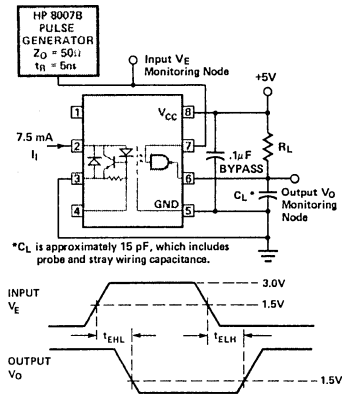


Figure 10. Test Circuit for t_{EHL} and t_{ELH}.

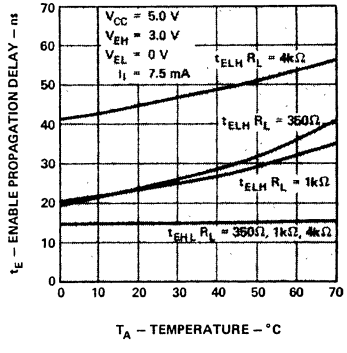


Figure 11. Enable Propagation Delay vs. Temperature.

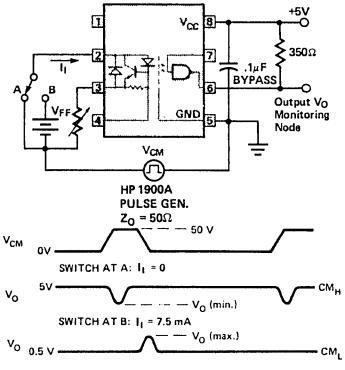


Figure 12. Test Circuit for Common Mode Transient Immunity and Typical Waveforms.

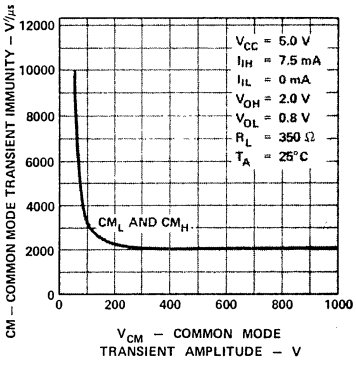


Figure 13. Common Mode Transient Immunity vs. Common Mode Transient Amplitude.

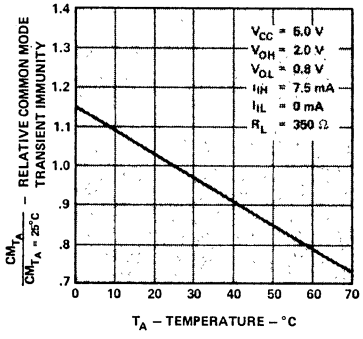


Figure 14. Relative Common Mode Transient Immunity vs. Temperature.

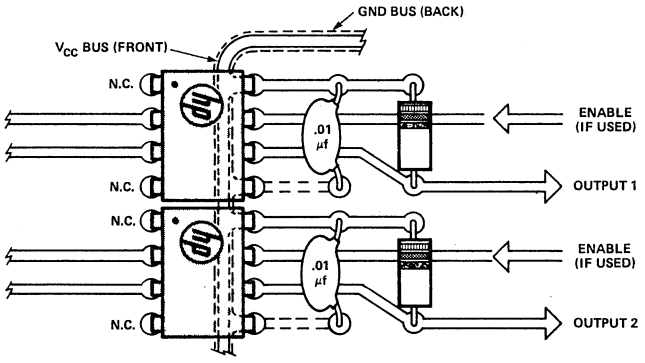


Figure 15. Recommended Printed Circuit Board Layout.

OPTO-COUPLERS

HEWLETT hp PACKARD

COMPONENTS

DUAL TTL COMPATIBLE OPTOCOUPLER

HCPL-2630

TECHNICAL DATA APRIL 1979

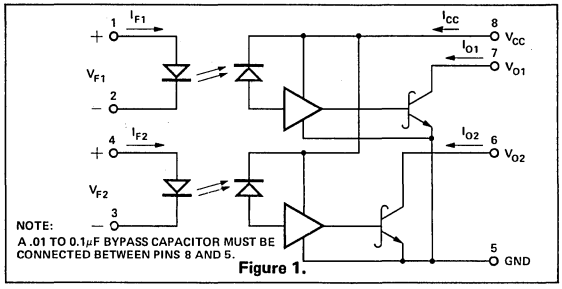


Figure 1.

Features

- **HIGH DENSITY PACKAGING**
- **DTL/TTL COMPATIBLE: 5V SUPPLY**
- **ULTRA HIGH SPEED**
- **LOW INPUT CURRENT REQUIRED**
- **HIGH COMMON MODE REJECTION**
- **GUARANTEED PERFORMANCE OVER TEMPERATURE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**
- **3000Vdc INSULATION VOLTAGE**

Description/Applications

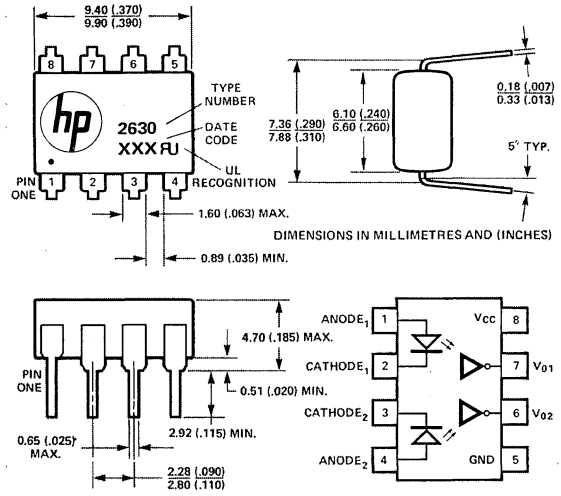
The HCPL-2630 consists of a pair of inverting optically coupled gates each with a GaAsP photon emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. Each circuit is temperature, current and voltage compensated.

This unique dual coupler design provides maximum DC and AC circuit isolation between each input and output while achieving DTL/TTL circuit compatibility. The coupler operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5 mA in each channel will sink an eight gate fan-out (13 mA) at the output with 5 volt V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 50 nsec.

The HCPL-2630 can be used in high speed digital interface applications where common mode signals must be rejected such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished between system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

The open collector output provides capability for bussing, strobing and "WIRED-OR" connection. In all applications, the dual channel configuration allows for high density packaging, increased convenience and more usable board space.

OUTLINE DRAWING



Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	6.3*	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings

(No derating required up to 70°C)

Storage Temperature ..... -55°C to +125°C

Operating Temperature ..... 0°C to +70°C

Lead Solder Temperature ..... 260°C for 10s (1.6mm below seating plane)

Peak Forward Input Current (each channel) ..... 30 mA (≤ 1 msec Duration)

Average Forward Input Current (each channel) ..... 15 mA

Reverse Input Voltage (each channel) 5V

Supply Voltage - V_{CC} ..... 7V (1 Minute Maximum)

Output Current - I_O (each channel) ..... 16 mA

Output Voltage - V_O (each channel) 7V

Output Collector Power Dissipation ..... 60 mW

*6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

Electrical Characteristics

OVER RECOMMENDED TEMPERATURE (T_A = 0°C TO 70°C) UNLESS OTHERWISE NOTED

Parameter	Symbol	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}		50	250	μA	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250μA		3
Low Level Output Voltage	V_{OL}		0.5	0.6	V	V_{CC} = 5.5V, I_F = 5mA I_{OL} (Sinking) = 13mA	3	3
High Level Supply Current	I_{CCH}		14	30	mA	V_{CC} = 5.5V, I_F = 0 (Both Channels)		
Low Level Supply	I_{CCL}		26	36	mA	V_{CC} = 5.5V, I_F = 10mA (Both Channels)		
Input - Output Insulation Leakage Current	I_{I-O}			1.0	μA	Relative Humidity = 45% T_A = 25°C, t = 5s, V_{I-O} = 3000Vdc		4
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500V, T_A = 25°C		4
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f = 1MHz, T_A = 25°C		4
Input Forward Voltage	V_F		1.5	1.75	V	I_F = 10mA, T_A = 25°C	4	7,3
Input Reverse Breakdown Voltage	BV_R	5			V	I_R = 10μA, T_A = 25°C		
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1MHz		3
Input-Input Insulation Leakage Current	I_{I-I}		0.005		μA	Relative Humidity = 45%, t=5s, V_{I-I}=500V		8
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500V		8
Capacitance (Input-Input)	C_{I-I}		0.25		pF	f = 1MHz		8
Current Transfer Ratio	CTR		700		%	I_F = 5.0mA, R_L = 100Ω	2	6

*All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics at T_A=25°C, V_{CC}=5V

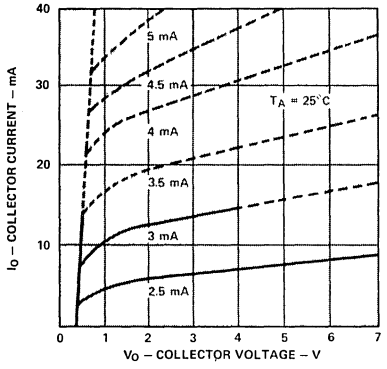
\CH CHANNEL

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}		55	75	ns	R_L = 350 Ω, C_L = 15pF, I_F = 7.5mA	6,7	1
Propagation Delay Time to Low Output Level	t_{PHL}		40	75	ns	R_L = 350 Ω, C_L = 15pF, I_F = 7.5mA	6,7	2
Output Rise-Fall Time (10-90%)	t_r, t_f		25		ns	R_L = 350 Ω, C_L = 15pF, I_F = 7.5mA		
Common Mode Transient Immunity at High Output Level	CM_H		50		V/μs	V_{CM} = 10V_{p-p}, R_L = 350 Ω, V_O (min.) = 2V, I_F = 0mA	9	5
Common Mode Transient Immunity at Low Output Level	CM_L		-150		V/μs	V_{CM} = 10V_{p-p}, R_L = 350 Ω, V_O (max.) = 0.8V I_F = 7.5mA	9	5

NOTE: It is essential that a bypass capacitor (.01μF to 0.1μF, ceramic) be connected from pin 8 to pin 5. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20mm. Failure to provide the bypass may impair the switching properties (Figure 5).

NOTES:

1. The t_{PLH} propagation delay is measured from the 3.75 mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
2. The t_{PHL} propagation delay is measured from the 3.75 mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
3. Each channel.
4. Measured between pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together.
5. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O>2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O<0.8V).
6. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
7. At 10mA VF decreases with increasing temperature at the rate of 1.9mV/°C.
8. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.



NOTE: Dashed characteristics indicate pulsed operation.

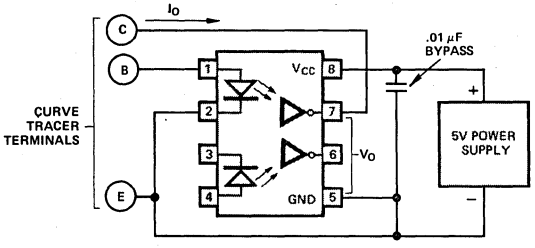
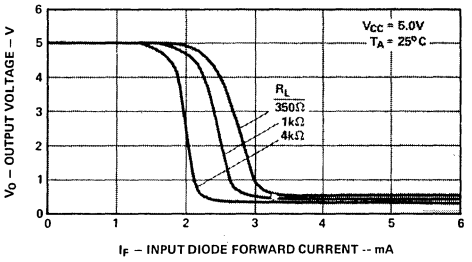


Figure 2. Optocoupler Transfer Characteristics.



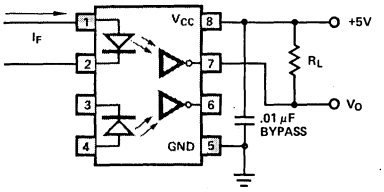


Figure 3. Input-Output Characteristics.

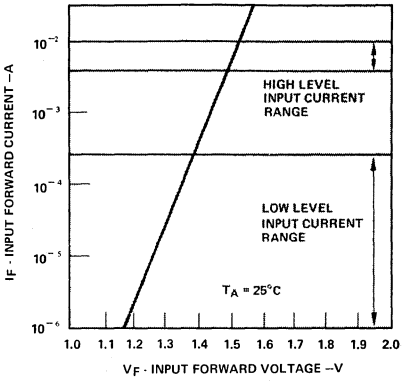


Figure 4. Input Diode Forward Characteristic

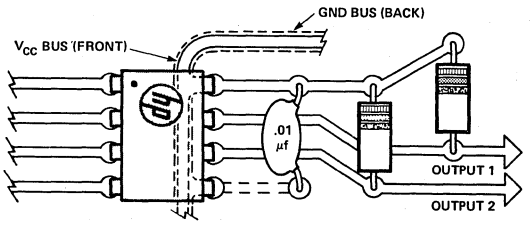
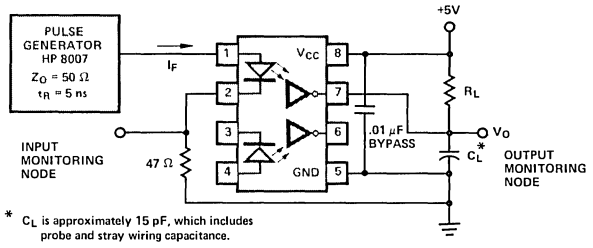


Figure 5. Recommended Printed Circuit Board Layout.



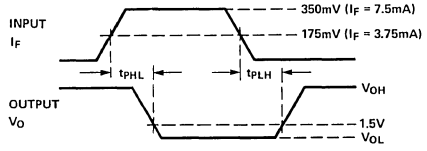


Figure 6. Test Circuit for t_{PHL} and t_{PLH}.

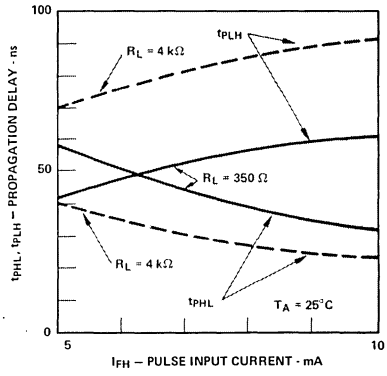


Figure 7. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.

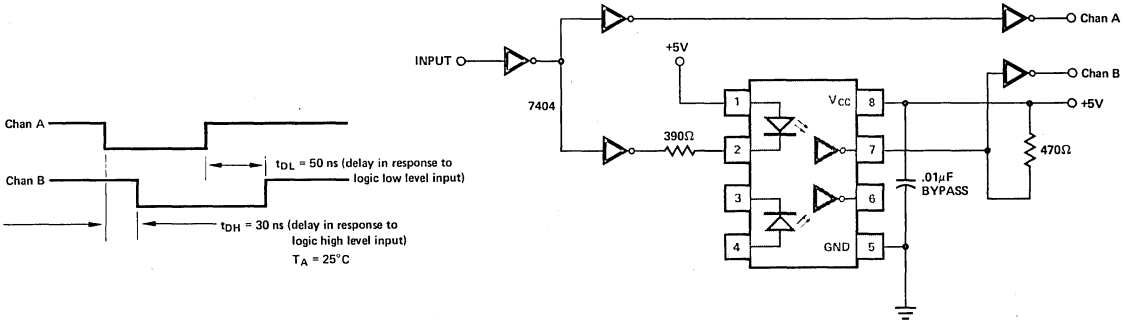


Figure 8. Response Delay Between TTL Gates.

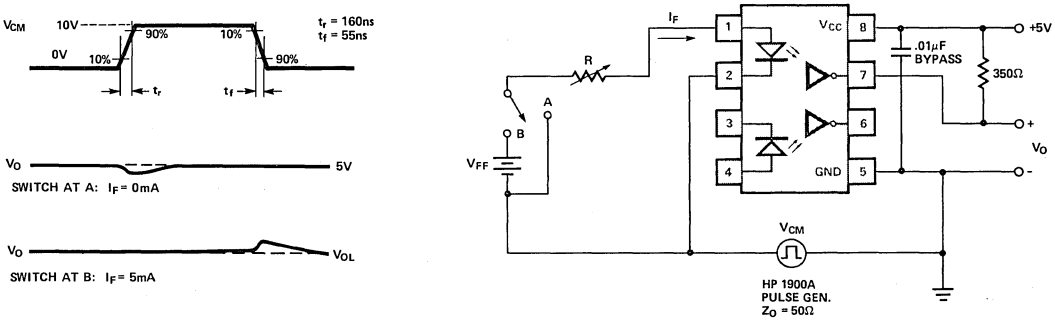


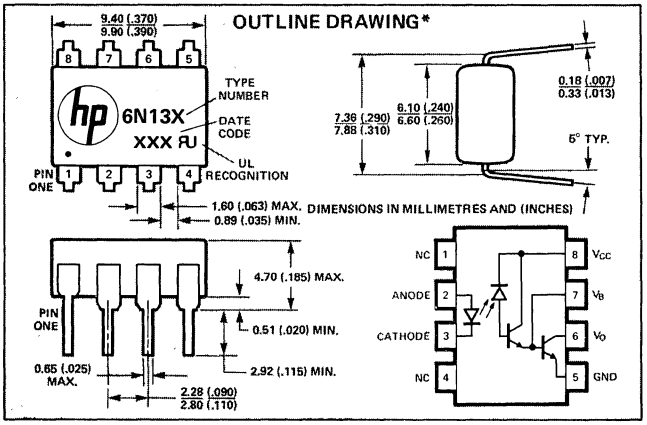
Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

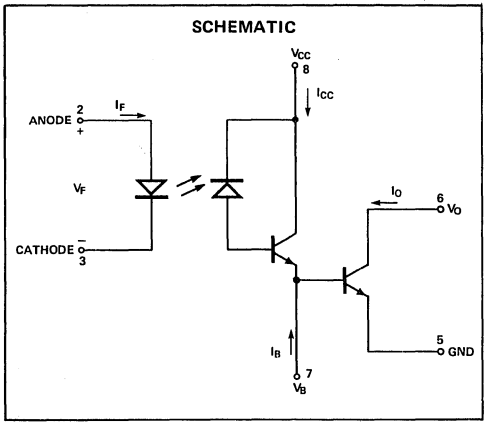
HEWLETT PACKARD
COMPONENTS

LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

6N138
6N139

TECHNICAL DATA APRIL 1979





Features

- **HIGH CURRENT TRANSFER RATIO — 800% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT — 0.5mA**
- **TTL COMPATIBLE OUTPUT — 0.1V V_{OL}**
- **3000 Vdc INSULATION VOLTAGE**
- **HIGH COMMON MODE REJECTION — 500V/μs**
- **PERFORMANCE GUARANTEED OVER TEMPERATURE 0°C to 70°C**
- **BASE ACCESS ALLOWS GAIN BANDWIDTH ADJUSTMENT**
- **HIGH OUTPUT CURRENT — 60mA**
- **DC TO 1M bit/s OPERATION**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)**

Applications

- Ground Isolate Most Logic Families — TTL/TTL, CMOS/TTL, CMOS/CMOS, LTTL/TTL, CMOS/LTTL
- Low Input Current Line Receiver — Long Line or Partyline
- EIA RS-232C Line Receiver
- Telephone Ring Detector
- 117 V ac Line Voltage Status Indicator — Low Input Power Dissipation
- Low Power Systems — Ground Isolation

Description

These high gain series couplers use a Light Emitting Diode and an integrated high gain photon detector to provide 3000V dc electrical insulation, 500V/μs common mode transient immunity and extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage result in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation. A base access terminal allows a gain bandwidth adjustment to be made.

The 6N139 is suitable for use in CMOS, LTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70°C operating range for only 0.5mA of LED current.

The 6N138 is suitable for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70°C for an LED current of 1.6mA [1 TTL unit load (U.L.)]. A 300% minimum CTR enables operation with 1 U.L. in, 1 U.L. out with a 2.2 kΩ pull-up resistor.

*JEDEC Registered Data.

Absolute Maximum Ratings*

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10s
(1.6mm below seating plane)
Average Input Current — I_F ..... 20mA [1]
Peak Input Current — I_F 40mA
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current — I_F 1.0A
(≤ 1μs pulse width, 300 pps)
Reverse Input Voltage — V_R 5V
Input Power Dissipation ..... 35mW [2]
Output Current — I_O (Pin 6) ..... 60mA [3]
Emitter-Base Reverse Voltage (Pin 5-7) 0.5V
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 6-5)
6N138 .....−0.5 to 7V
6N139 .....−0.5 to 18V
Output Power Dissipation ..... 100mW [4]

See notes, following page.

Electrical Specifications

OVER RECOMMENDED TEMPERATURE (T_A = 0°C to 70°C), UNLESS OTHERWISE SPECIFIED

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	6N139	400 500	800 900		%	I_F = 0.5mA, V_O = 0.4V, V_{CC} = 4.5V I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V	3	5,6
		6N138	300	600		%	I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V		
Logic Low Output Voltage	V_{OL}	6N139		0.1 0.1 0.2	0.4 0.4 0.4	V	I_F = 1.6mA, I_O = 6.4mA, V_{CC} = 4.5V I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V	1,2	6
		6N138		0.1	0.4	V	I_F = 1.6mA, I_O = 4.8mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}*	6N139		0.05	100	μA	I_F = 0mA, V_O = V_{CC} = 18V		6
		6N138		0.1	250	μA	I_F = 0mA, V_O = V_{CC} = 7V		
Logic Low Supply Current	I_{CCL}			0.2		mA	I_F = 1.6mA, V_O = Open, V_{CC} = 5V		6
Logic High Supply Current	I_{CCH}			10		nA	I_F = 0mA, V_O = Open, V_{CC} = 5V		6
Input Forward Voltage	V_F*			1.4	1.7	V	I_F = 1.6mA, T_A = 25°C	4	
Input Reverse Breakdown Voltage	BV_R*		5		V		I_R = 10μA, T_A=25°C		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			−1.8		mV/°C	I_F = 1.6mA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		
Input - Output Insulation Leakage Current	I_{I-O}*				1.0	μA	45% Relative Humidity, T_A = 25°C t = 5 s, V_{I-O} = 3000Vdc		7
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 Vdc		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		7

**All typicals at T_A = 25°C and V_{CC} = 5V, unless otherwise noted.

Switching Specifications

AT T_A = 25°C

Parameter	Sym.	Device	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}*	6N139		5 0.2	25 1	μs	I_F = 0.5mA, R_L = 4.7kΩ I_F = 12mA, R_L = 270Ω	9	6,8
		6N138		1	10	μs	I_F = 1.6mA, R_L = 2.2kΩ		
Propagation Delay Time To Logic High at Output	t_{PLH}*	6N139		5 1	60 7	μs	I_F = 0.5mA, R_L = 4.7kΩ I_F = 12mA, R_L = 270Ω	9	6,8
		6N138		4	35	μs	I_F = 1.6mA, R_L = 2.2kΩ		
Common Mode Transient Immunity at Logic High Level Output	CM_H			500		V/μs	I_F = 0mA, R_L = 2.2kΩ, R_{CC} = 0 $\|V_{cm}\|$ = 10V_{p-p}	10	9,10
Common Mode Transient Immunity at Logic Low Level Output	CM_L			−500		V/μs	I_F = 1.6mA, R_L = 2.2kΩ, R_{CC} = 0 $\|V_{cm}\|$ = 10V_{p-p}	10	9,10

NOTES:

1. Derate linearly above 50°C free-air temperature at a rate of 0.4mA/°C.
2. Derate linearly above 50°C free-air temperature at a rate of 0.7mW/°C.
3. Derate linearly above 25°C free-air temperature at a rate of 0.7mA/°C.
4. Derate linearly above 25°C free-air temperature at a rate of 2.0mW/°C.
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Pin 7 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
8. Use of a resistor between pin 5 and 7 will decrease gain and delay time. See Application Note 951-1 for more details.
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
10. In applications where dV/dt may exceed 50,000V/μs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is $R_{CC} \approx \frac{1V}{0.15\ I_F\ (mA)}$ kΩ.

*JEDEC Registered Data.

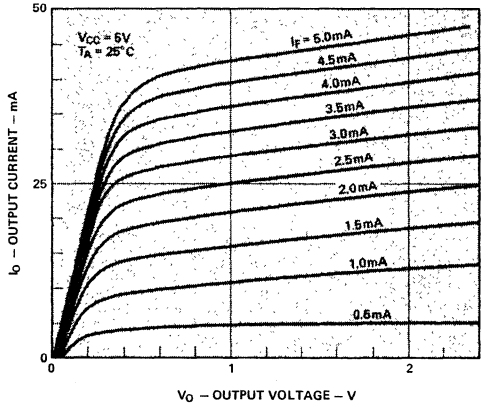


Figure 1. 6N139 DC Transfer Characteristics.

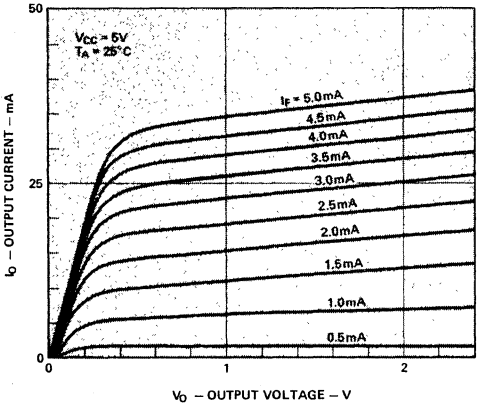


Figure 2. 6N138 DC Transfer Characteristics.

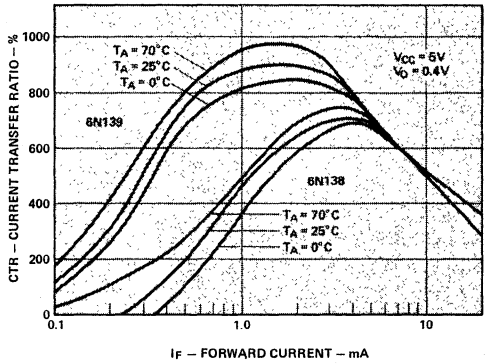


Figure 3. Current Transfer Ratio vs. Forward Current.

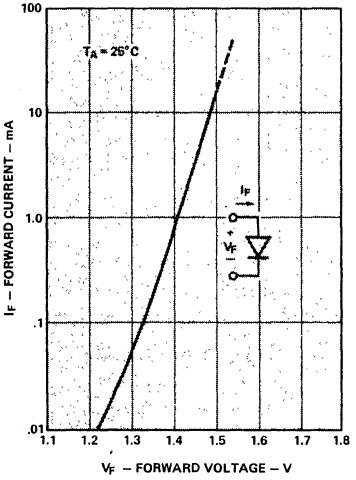


Figure 4. Input Diode Forward Current vs. Forward Voltage.

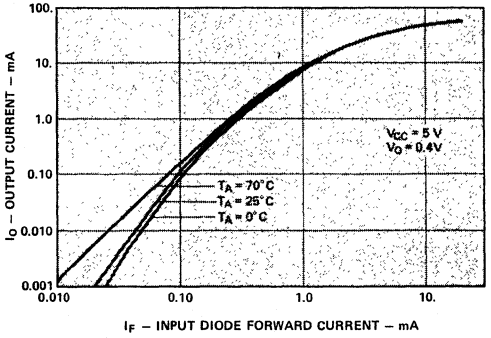


Figure 5. 6N139 Output Current vs. Input Diode Forward Current.

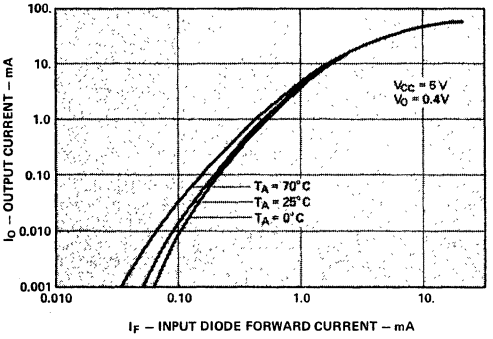


Figure 6. 6N138 Output Current vs. Input Diode Forward Current.

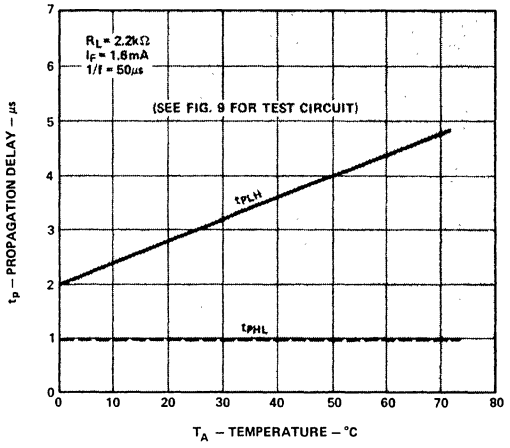


Figure 7. Propagation Delay vs. Temperature.

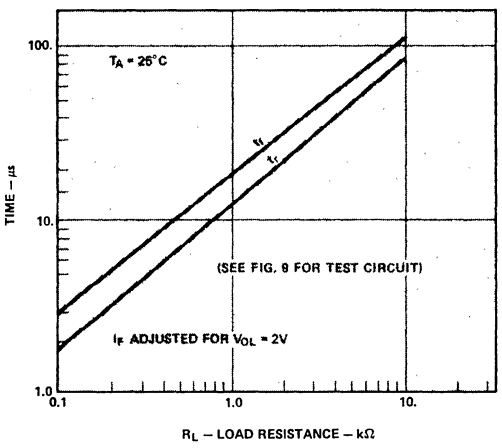


Figure 8. Non Saturated Rise and Fall Times vs. Load Resistance.

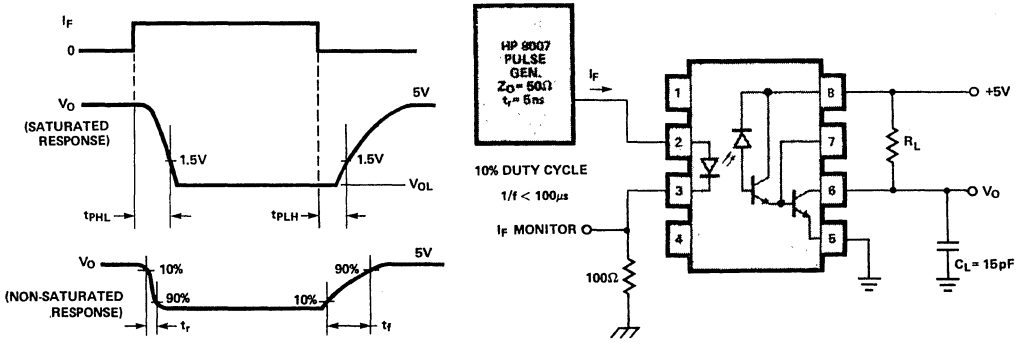


Figure 9. Switching Test Circuit.*

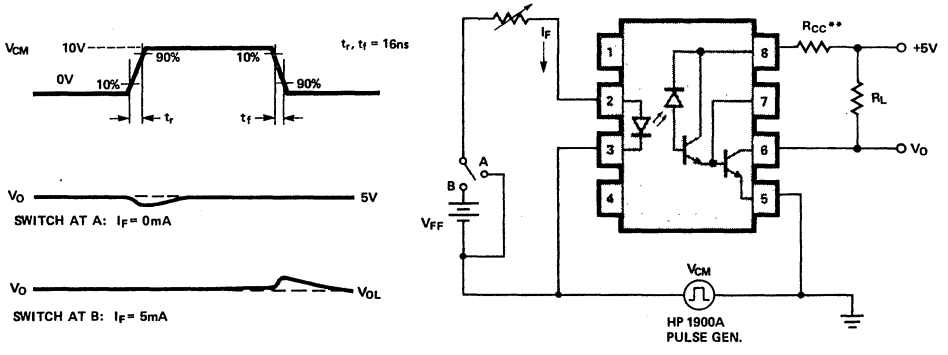


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

*JEDEC Registered Data.

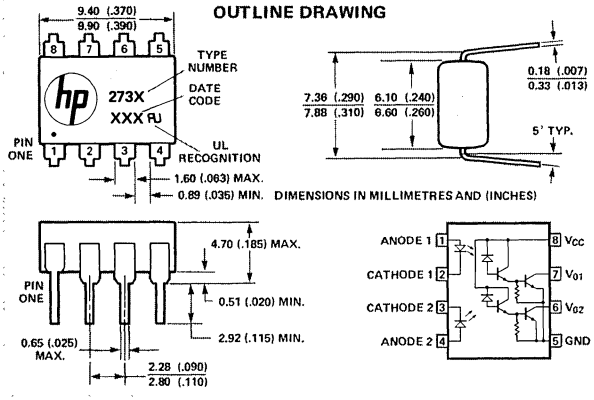
**See Note 10

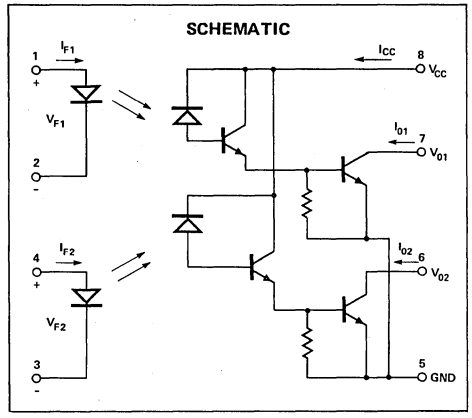
HEWLETT PACKARD
COMPONENTS

DUAL LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLERS

HCPL-2730
HCPL-2731

TECHNICAL DATA APRIL 1979





Features

- HIGH CURRENT TRANSFER RATIO — 1000% TYPICAL
- LOW INPUT CURRENT REQUIREMENT — 0.5 mA
- LOW OUTPUT SATURATION VOLTAGE — 1.0V TYPICAL
- HIGH DENSITY PACKAGING
- 3000V DC INSULATION VOLTAGE
- PERFORMANCE GUARANTEED OVER 0°C TO 70°C TEMPERATURE RANGE
- HIGH COMMON MODE REJECTION
- DATA RATES UP TO 200K BIT/s
- HIGH FANOUT
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361).

Applications

- Digital Logic Ground Isolation
- Telephone Ring Detector
- EIA RS-232C Line Receiver
- Low Input Current Line Receiver — Long Line or Partyline
- Microprocessor Bus Isolation
- Current Loop Receiver
- Polarity Sensing
- Level Shifting
- Line Voltage Status Indicator — Low Input Power Dissipation

Description

The HCPL-2730/31 dual channel couplers contain a separated pair of GaAsP light emitting diodes optically coupled to a pair of integrated high gain photon detectors. They provide extremely high current transfer ratio, 3000V dc electrical insulation and excellent input-output common mode transient immunity. A separate pin for the photodiodes and first gain stages (V_{CC}) permits lower output saturation voltage and higher speed operation than possible with conventional photodarlington type isolators. The separate V_{CC} pin can be strobed low as an output disable. In addition V_{CC} may be as low as 1.6V without adversely affecting the parametric performance.

Guaranteed operation at low input currents and the high current transfer ratio (CTR) reduce the magnitude and effects of CTR degradation.

The outstanding high temperature performance of this split Darlington type output amplifier results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground.

The HCPL-2731 has a 400% minimum CTR at an input current of only 0.5 mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing or RS232C data transmission systems. In addition, the high CTR and high output current capability make this device extremely useful in applications where a high fanout is required. Compatibility with high voltage CMOS logic systems is guaranteed by the 18V V_{CC} and V_O specifications and by testing output high leakage (I_{OH}) at 18V.

The HCPL-2730 is specified at an input current of 1.6 mA and has a 7V V_{CC} and V_O rating. The 300% minimum CTR allows TTL to TTL interfacing with an input current of only 1.6 mA.

Important specifications such as CTR, leakage current and output saturation voltage are guaranteed over the 0°C to 70°C temperature range to allow trouble-free system operation.

Electrical Specifications

(Over Recommended Temperature T_A = 0°C to 70°C, Unless Otherwise Specified)

Parameter	Sym.	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	2731	400 500	1000 1100		%	I_F = 0.5mA, V_O = 0.4V, V_{CC} = 4.5V I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V	2	6,7
		2730	300	1000		%	I_F = 1.6mA, V_O = 0.4V, V_{CC} = 4.5V	2	
Logic Low Output Voltage	V_{OL}	2731		0.1 0.1 0.2	0.4 0.4 0.4	V	I_F = 1.6mA, I_O = 8mA, V_{CC} = 4.5V I_F = 5mA, I_O = 15mA, V_{CC} = 4.5V I_F = 12mA, I_O = 24mA, V_{CC} = 4.5V	1	6
		2730		0.1	0.4	V	I_F = 1.6mA, I_O = 4.8mA, V_{CC} = 4.5V		
Logic High Output Current	I_{OH}	2731		0.005	100	μA	I_F = 0 mA, V_O = V_{CC} = 18V		6
		2730		0.01	250	μA	I_F = 0mA, V_O = V_{CC} = 7V		
Logic Low Supply Current	I_{CCL}	2731		1.2		mA	I_{F1} = I_{F2} = 1.6mA, V_{CC} = 18V		
		2730		0.9			V_{O1} = V_{O2} = Open, V_{CC} = 7V		
Logic High Supply Current	I_{CCH}	2731		5		nA	I_{F1} = I_{F2} = 0mA, V_{CC} = 18V		
		2730		4			V_{O1} = V_{O2} = Open, V_{CC} = 7V		
Input Forward Voltage	V_F			1.4	1.7	V	I_F = 1.6mA, T_A = 25°C	4	6
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 μA, T_A = 25°C		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.6mA		6
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		6
Input-Output Insulation Leakage Current	I_{I-O}				1.0	μA	45% Relative Humidity, T_A = 25°C t = 5s, V_{I-O} = 3000 Vdc		8
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500Vdc		8
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		8
Input-Input Insulation Leakage Current	I_{I-I}			0.005		μA	45% Relative Humidity, t=5s, V_{I-I} = 500Vdc		9
Resistance (Input-Input)	R_{I-I}			10^{11}		Ω	V_{I-I} = 500Vdc		9
Capacitance (Input-Input)	C_{I-I}			0.25		pF	f = 1 MHz		9

*All typicals at T_A = 25°C

Switching Specifications at T_A=25°C

Parameter	Sym.	Device HCPL-	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}	2731		25	100	μs	I_F = 0.5mA, R_L = 4.7kΩ	9	
		2730/1		5 0.5	20 2	μs	I_F = 1.6mA, R_L = 2.2kΩ I_F = 12mA, R_L = 270Ω		
Propagation Delay Time To Logic High at Output	t_{PLH}	2731		20	60	μs	I_F = 0.5mA, R_L = 4.7kΩ	9	
		2730/1		10 1	35 10		I_F = 1.6mA, R_L = 2.2kΩ I_F = 12mA, R_L = 270Ω		
Common Mode Transient Immunity at Logic High Level Output	CM_H			500		V/μs	I_F = 0mA, R_L = 2.2kΩ $\lvert V_{CM} \rvert$ = $10V_{p-p}$	10	10,11
Common Mode Transient Immunity at Logic Low Level Output	CM_L			-500		V/μs	I_F = 1.6mA, R_L = 2.2kΩ $\lvert V_{CM} \rvert$ = $10V_{p-p}$	10	10,11

NOTES:
1. Derate linearly above 50° C free-air temperature at a rate of 0.5mA/° C.
2. Derate linearly above 50° C free-air temperature at a rate of 0.9mW/° C.
3. Derate linearly above 35° C free-air temperature at a rate of 0.6mA/° C.
4. Pin 5 should be the most negative voltage at the detector side.
5. Derate linearly above 35° C free-air temperature at a rate of 1.7mW/° C. Output power is collector output power plus supply power.
6. Each channel.
7. CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
8. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
9. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.
10. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in Logic High state (i.e., V_O > 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM} dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8V).
11. In applications where dV/dt may exceed 50,000 V/μs (such as a static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is $R_{CC} \approx \frac{1V}{0.3\ I_F\ (mA)}$ kΩ.

Absolute Maximum Ratings

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 sec
(1.6mm below seating plane)
Average Input Current — I_F
(each channel) ..... 20 mA[1]
Peak Input Current — I_F
(each channel) ..... 40 mA
(50% duty cycle, 1 ms pulse width)
Reverse Input Voltage — V_R
(each channel) 5V
Input Power Dissipation
(each channel) ..... 35 mW[2]
Output Current — I_O
(each channel) ..... 60 mA[3]
Supply and Output Voltage — V_{CC} (Pin 8-5), V_O (Pin 7,6-5)[4]
HCPL-2730 ..... -0.5 to 7V
HCPL-2731 ..... -0.5 to 18V
Output Power Dissipation
(each channel) ..... 100 mW[5]

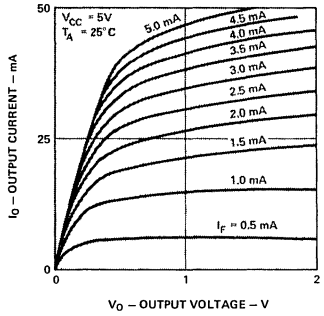


Figure 1. DC Transfer Characteristics.

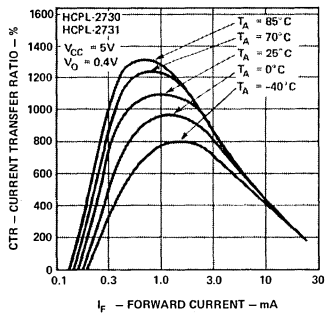


Figure 2. Current Transfer Ratio vs. Forward Current.

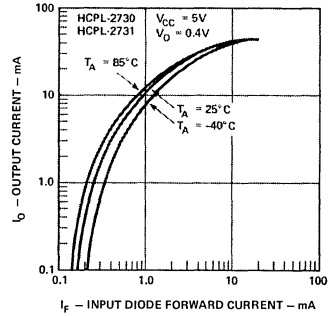


Figure 3. Output Current vs. Input Diode Forward Current.

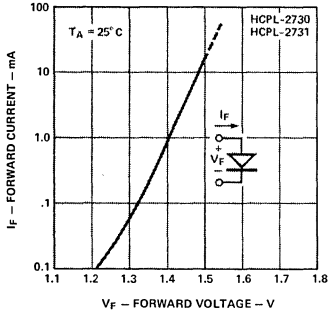


Figure 4. Input Diode Forward Current vs. Forward Voltage.

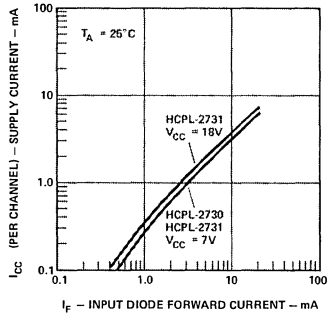


Figure 5. Supply Current Per Channel vs. Input Diode Forward Current.

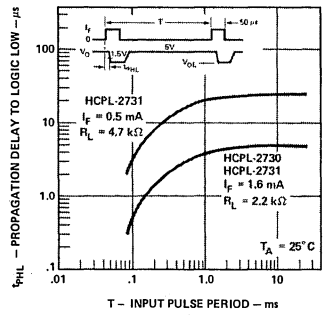


Figure 6. Propagation Delay To Logic Low vs. Pulse Period.

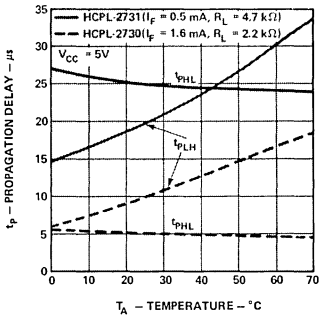


Figure 7. Propagation Delay vs. Temperature.

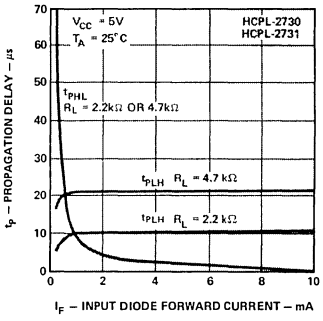


Figure 8. Propagation Delay vs. Input Diode Forward Current.

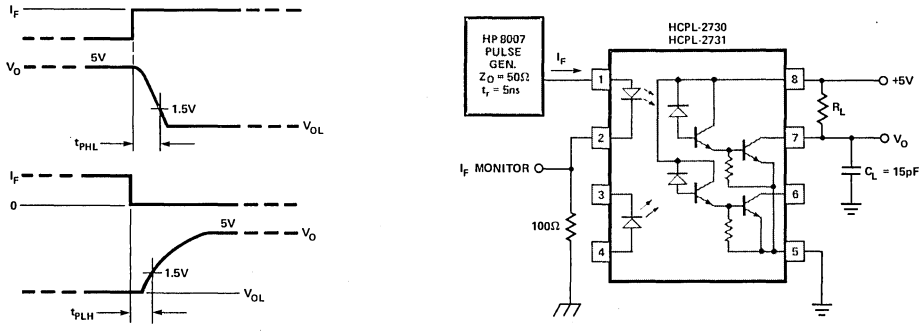


Figure 9. Switching Test Circuit.

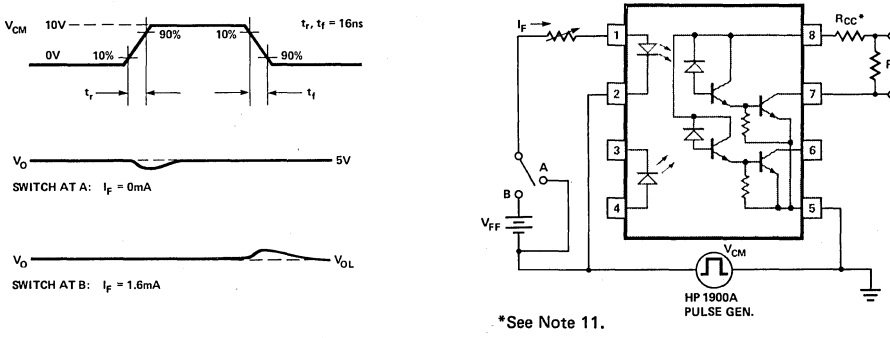


Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

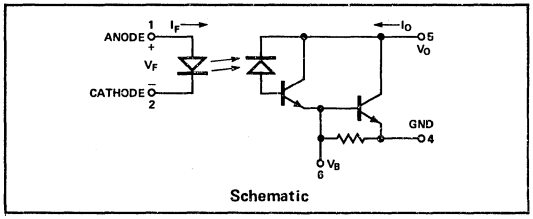
HEWLETT hp PACKARD

COMPONENTS

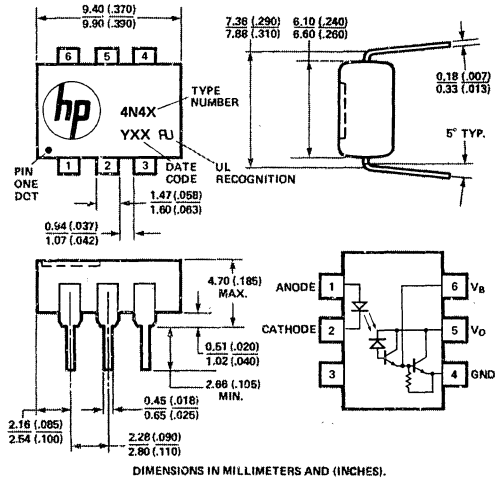
LOW INPUT CURRENT, HIGH GAIN OPTOCOUPLER

4N45
4N46

TECHNICAL DATA APRIL 1979



Schematic



DIMENSIONS IN MILLIMETERS AND (INCHES).

Cutlins Drawing*

Features

- **HIGH CURRENT TRANSFER RATIO — 1000% TYPICAL**
- **LOW INPUT CURRENT REQUIREMENT — 0.5 mA**
- **3000 Vdc INSULATION VOLTAGE**
- **PERFORMANCE GUARANTEED OVER 0°C TO 70°C TEMPERATURE RANGE**
- **RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES INC. (FILE NO. E55361)**
- **INTERNAL BASE-EMITTER RESISTOR MINIMIZES OUTPUT LEAKAGE**
- **GAIN-BANDWIDTH ADJUSTMENT PIN**
- **HIGH COMMON MODE REJECTION**

Description

The 4N45/46 optocouplers contain a GaAsP light emitting diode optically coupled to a high gain photodetector IC.

The excellent performance over temperature results from the inclusion of an integrated emitter-base bypass resistor which shunts photodiode and first stage leakage currents to ground. External access to the second stage base provides better noise rejection than a conventional photodarlington detector. An external resistor or capacitor at the base can be added to make a gain-bandwidth or input current threshold adjustment. The base lead can also be used for feedback.

The high current transfer ratio at very low input currents permits circuit designs in which adequate margin can be allowed for the effects of CTR degradation over time.

The 4N46 has a 350% minimum CTR at an input current of only 0.5mA making it ideal for use in low input current applications such as MOS, CMOS and low power logic interfacing. Compatibility with high voltage CMOS logic systems is assured by the 20V minimum breakdown voltage of the output transistor and by the guaranteed maximum output leakage (I_{OH}) at 18V.

The 4N45 has a 250% minimum CTR at 1.0mA input current and a 7V minimum breakdown voltage rating.

*JEDEC Registered Data.

Applications

- **Telephone Ring Detector**
- **Digital Logic Ground Isolation**
- **Low Input Current Line Receiver**
- **Line Voltage Status Indicator — Low Input Power Dissipation**
- **Logic to Reed Relay Interface**
- **Level Shifting**
- **Interface Between Logic Families**

Absolute Maximum Ratings*

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +70°C
Lead Solder Temperature ..... 260°C for 10 s.
(1.6mm below seating plane)
Average Input Current — I_F ..... 20 mA[1]
Peak Input Current — I_F ..... 40 mA
(50% duty cycle, 1ms pulse width)
Peak Transient Input Current — I_F 1.0A
($\leq$1 µs pulse width, 300pps)
Reverse Input Voltage — V_R 5V
Input Power Dissipation ..... 35mW[2]
Output Current — I_O (Pin 5) ..... 60 mA[3]
Emitter-Base Reverse Voltage (Pins 4-6) 0.5V
Output Voltage — V_O (Pin 5-4)
4N45 ..... -0.5 to 7V
4N46 ..... -0.5 to 20V
Output Power Dissipation ..... 100mW[4]

See notes, following page

Electrical Specifications

OVER RECOMMENDED TEMPERATURE (T_A = 0°C TO 70°C), UNLESS OTHERWISE SPECIFIED

Parameter	Sym.	Device	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR*	4N46	350 500 200	1500 1500 600		%	I_F = 0.5mA, V_O = 1.0V I_F = 1.0mA, V_O = 1.0V I_F = 10mA, V_O = 1.2V	4	5,6
		4N45	250 200	1200 500		%	I_F = 1.0mA, V_O = 1.0V I_F = 10mA, V_O = 1.2V		
Logic Low Output Voltage	V_{OL}	4N46		.90 .92 .95	1.0 1.0 1.2	V	I_F = 0.5mA, I_{OL} = 1.75mA I_F = 1.0mA, I_{OL} = 5.0mA I_F = 10mA, I_{OL} = 20mA	2	6
		4N45		.90 .95	1.0 1.2	V	I_F = 1.0mA, I_{OL} = 2.5mA I_F = 10mA, I_{OL} = 20mA		
Logic High Output Current	I_{OH}*	4N46		.001	100	µA	I_F = 0mA, V_O = 18V		6
		4N45		.001	250	µA	I_F = 0mA, V_O = 5V		
Input Forward Voltage	V_F*			1.4	1.7	V	I_F = 1.0mA, T_A = 25°C	1	
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			-1.8		mV/°C	I_F = 1.0mA		
Input Reverse Breakdown Voltage	BV_R*		5			V	I_R = 10µA, T_A = 25°C		
Input Capacitance	C_{IN}			60		pF	f = 1MHz, V_F = 0		
Input-Output Insulation Leakage Current	I_{I-O}*				1.0	µA	45% Relative Humidity, T_A=25°C t = 5 s, V_{I-O} = 3000VDC		7
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500VDC		7
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1MHz		7

Switching Specifications

AT T_A = 25°C

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}		80		µs	I_F = 1.0mA, R_L = 10kΩ	8	6,8
	t_{PHL}*		5	50	µs	I_F = 10mA, R_L = 220Ω		
Propagation Delay Time To Logic High at Output	t_{PLH}		1500		µs	I_F = 1.0mA, R_L = 10kΩ	8	6,8
	t_{PLH}*		150	500	µs	I_F = 10mA, R_L = 220Ω		
Common Mode Transient Immunity at Logic High Level Output	CM_H		500		V/µs	I_F = 0mA, R_L = 10kΩ $\|V_{cm}\|$ = 10V_{p-p}	9	9
Common Mode Transient Immunity at Logic Low Level Output	CM_L		-500		V/µs	I_F = 1.0mA, R_L = 10kΩ $\|V_{cm}\|$ = 10V_{p-p}	9	9

*JEDEC Registered Data.

**All typicals at T_A = 25°C, unless otherwise noted.

NOTES:

1. Derate linearly above 50° C free-air temperature at a rate of 0.4mA/° C.
2. Derate linearly above 50° C free-air temperature at a rate of 0.7mW/° C.
3. Derate linearly above 25° C free-air temperature at a rate of 0.8mA/° C.
4. Derate linearly above 25° C free-air temperature at a rate of 1.5mW/° C.
5. DC CURRENT TRANSFER RATIO is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.
6. Pin 6 Open.
7. Device considered a two-terminal device: Pins 1, 2, 3 shorted together and Pins 4, 5, and 6 shorted together.
8. Use of a resistor between pin 4 and 6 will decrease gain and delay time. (See Figures 10 and 12).
9. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse, V_{cm}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.5V$). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{cm}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 2.5V$).

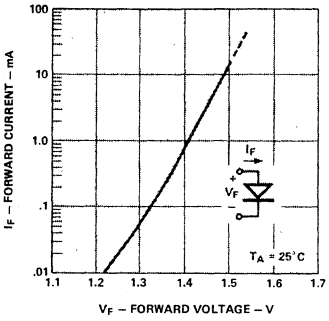


Figure 1. Input Diode Forward Current vs. Forward Voltage.

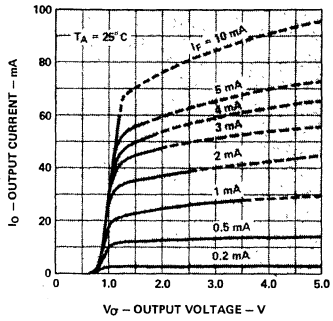


Figure 2. Typical DC Transfer Characteristics.

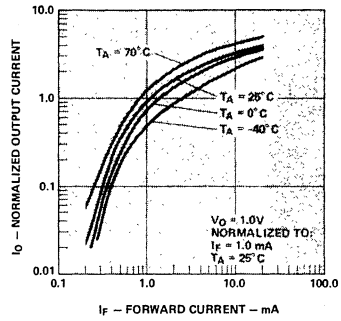


Figure 3. Output Current vs. Input Current.

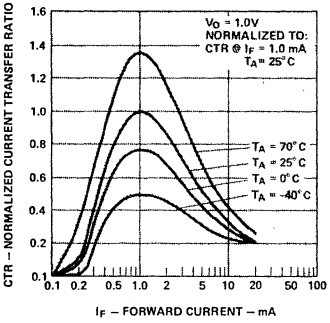


Figure 4. Current Transfer Ratio vs. Input Current.

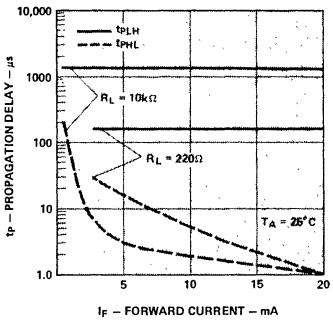


Figure 5. Propagation Delay vs. Forward Current.

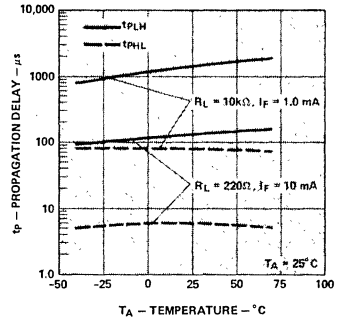


Figure 6. Propagation Delay vs. Temperature.

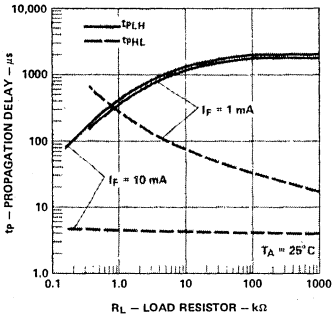
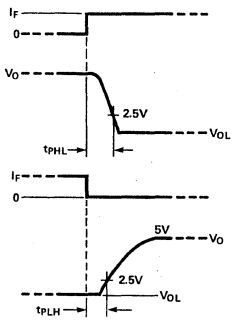


Figure 7. Propagation Delay vs Load Resistor.



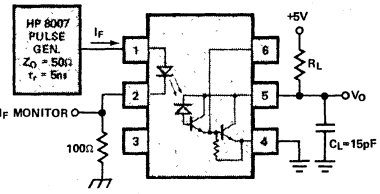
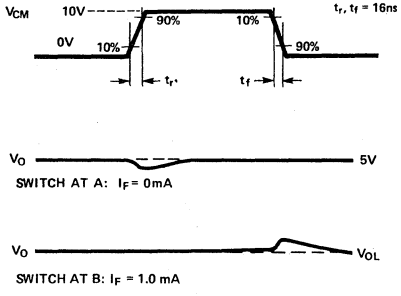


Figure 8. Switching Test Circuit



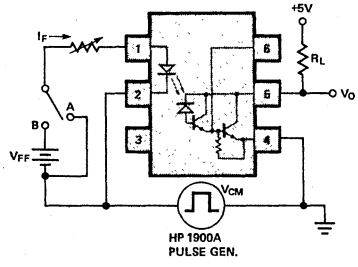


Figure 9. Test Circuit for Transient Immunity and Typical Waveforms.

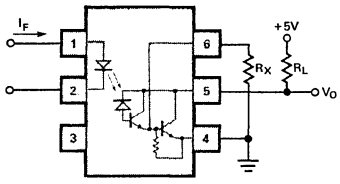


Figure 10. External Base Resistor, R_X

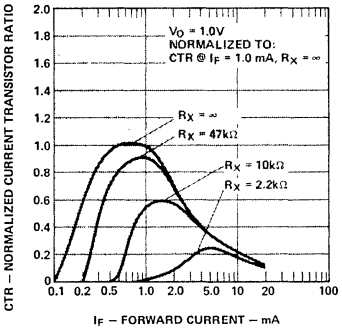


Figure 11. Effect of R_X On Current Transfer Ratio

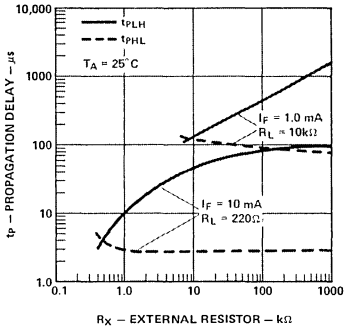
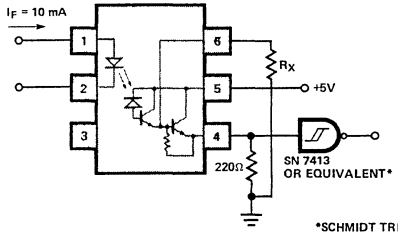


Figure 12. Effect of R_X On Propagation Delay

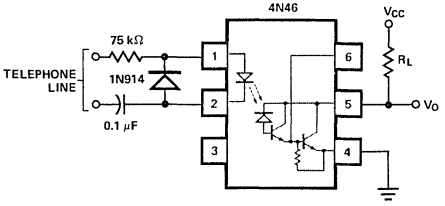
Applications



R_X (kΩ)	t_{PHL} (μs)	t_{PLH} (μs)
∞	5	320
100	5	200
47	5	140
20	6	80
10	6	45

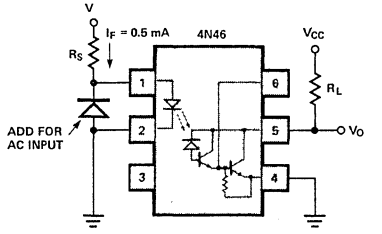
*SCHMIDT TRIGGER RECOMMENDED BECAUSE OF LONG t_r, t_f.

TTL Interface



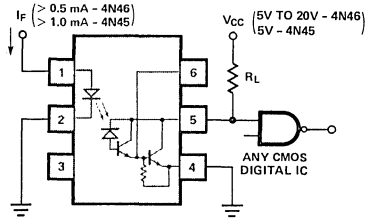
NOTE: AN INTEGRATOR MAY BE REQUIRED AT THE OUTPUT TO ELIMINATE DIALING PULSES AND LINE TRANSIENTS.

Telephone Ring Detector

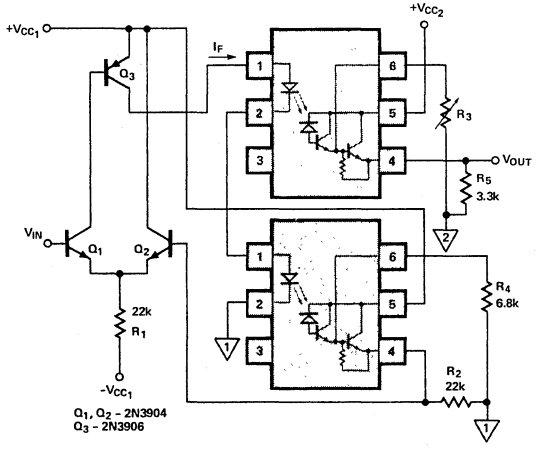


V (Vdc or Vrms)	R_S	V • I_F (mW)
24	47kΩ	11
48	100kΩ	22
115	220kΩ	62
230	470kΩ	113

Line Voltage Monitor



CMOS Interface



Analog Signal Isolation

CHARACTERISTICS

$R_{IN} \approx 30M\Omega$, $R_{OUT} \approx 50\Omega$
$V_{IN(MAX.)} = V_{CC_1} - 1V$, LINEARITY BETTER THAN 5%

DESIGN COMMENTS

R_1 - NOT CRITICAL $\left(\ll \frac{V_{IN\ (MAX.)} - (-V_{CC_1}) - V_{BE}}{I_{F\ (MAX.)}}\right) h_{FE}\ Q_3$

R_2 - NOT CRITICAL (OMIT IF 0.2 TO 0.3V OFFSET IS TOLERABLE)

$R_4 > \frac{V_{IN\ (MAX.)} + V_{BE}}{1\ mA}$

$R_5 > \frac{V_{IN\ (MAX.)}}{2.5\ mA}$

NOTE: ADJUST R_3 SO $V_{OUT} = V_{IN}$ AT $V_{IN} = \frac{V_{IN\ (MAX.)}}{2}$

OPTO-COUPLERS

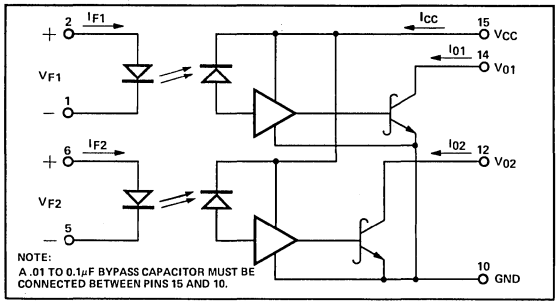
HEWLETT hp PACKARD

COMPONENTS

DUAL CHANNEL HERMETICALLY SEALED OPTOCOUPLER

6N134
6N134 TXV
6N134 TXVB

TECHNICAL DATA APRIL 1979



Features

- **HERMETICALLY SEALED**
- **HIGH SPEED**
- **PERFORMANCE GUARANTEED OVER -55°C TO +125°C AMBIENT TEMPERATURE RANGE**
- **STANDARD HIGH RELIABILITY SCREENED PARTS AVAILABLE**
- **TTL COMPATIBLE INPUT AND OUTPUT**
- **HIGH COMMON MODE REJECTION**
- **DUAL-IN-LINE PACKAGE**
- **1500Vdc INSULATION VOLTAGE**
- **EIA REGISTRATION**
- **HIGH RADIATION IMMUNITY**

Applications

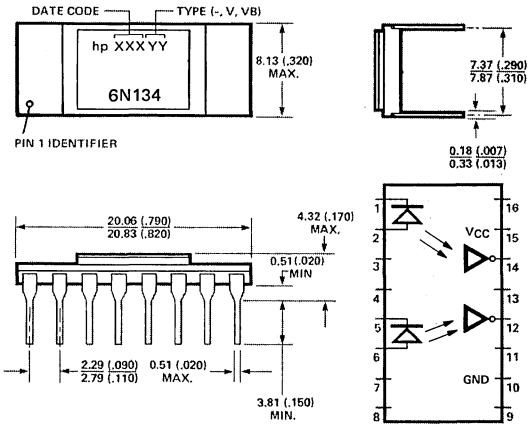
- Logic Ground Isolation
- Line Receiver
- Computer - Peripheral Interface
- Vehicle Command/Control Isolation
- High Reliability Systems
- System Test Equipment Isolation

Description

The 6N134 consists of a pair of inverting optically coupled gates, each with a light emitting diode and a unique high gain integrated photon detector in a hermetically sealed ceramic package. The output of the detector is an open collector Schottky clamped transistor.

This unique dual coupler design provides maximum DC and AC circuit isolation between each input and output while achieving TTL circuit compatibility. The isolator operational parameters are guaranteed from -55°C to +125°C, such that a minimum input current of 10 mA in each channel will sink a six gate fanout (10 mA) at the output with 4.5 to 5.5 V V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 55 nsec.

OUTLINE DRAWING*



DIMENSIONS IN MILLIMETRES AND (INCHES).

Recommended Operating Conditions

TABLE I

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	12.5*	20	mA
Supply Voltage	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		6	
Operating Temperature	T_A	−55	125	°C

Absolute Maximum Ratings*

(No derating required up to 125°C)

Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Lead Solder Temperature ..... 260°C for 10s (1.6mm below seating plane)
Peak Forward Input Current (each channel) ..... 40 mA (≤ 1 ms Duration)
Average Input Forward Current (each channel) ..... 20 mA
Input Power Dissipation (each channel) ..... 35 mW
Reverse Input Voltage (each channel) 5V
Supply Voltage - V_{CC} ..... 7V (1 minute maximum)
Output Current - I_O (each channel) ..... 25 mA
Output Power Dissipation (each channel) ..... 40 mW
Output Voltage - V_O (each channel) 7V
Total Power Dissipation (both channels) ..... 350 mW

**12.5mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 10mA or less.

*JEDEC Registered Data.

TABLE II

Electrical Characteristics

OVER RECOMMENDED TEMPERATURE (T_A = –55°C TO +125°C) UNLESS OTHERWISE NOTED

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}*		5	250	μA	V_{CC} = 5.5V, V_O = 5.5V, I_F = 250μA		1
Low Level Output Voltage	V_{OL}*		0.5	0.6	V	V_{CC} = 5.5V, I_F = 10mA I_{OL} (Sinking) = 10mA	4	1, 9
High Level Supply Current	I_{CCH}*		18	28	mA	V_{CC} = 5.5V, I_F = 0 (Both Channels)		
Low Level Supply Current	I_{CCL}*		26	36	mA	V_{CC} = 5.5V, I_F = 20mA (Both Channels)		
Input Forward Voltage	V_F*		1.5	1.75	V	I_F = 20mA, T_A = 25°C	1	1
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R = 10μA, T_A = 25°C		
Input-Output Insulation Leakage Current	I_{I-O}*			1.0	μA	V_{I-O} = 1500Vdc, Relative Humidity = 45% T_A = 25°C, t = 5s		2
Propagation Delay Time to High Output Level	t_{PLH}*		65	90	ns	R_L = 510Ω, C_L = 15pF, I_F = 13mA, T_A = 25°C	2,3	5
Propagation Delay Time to Low Output Level	t_{PHL}*		55	90	ns	R_L = 510Ω, C_L = 15pF I_F = 13mA, T_A = 25°C	2,3	6

TABLE III

Typical Characteristics AT T_A = 25°C, V_{CC} = 5V EACH CHANNEL

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Input Capacitance	C_{IN}		60		pF	V_F = 0, f = 1MHz		1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		-1.9		mV/°C	I_F = 20mA		1
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O} = 500V		3
Capacitance (Input-Output)	C_{I-O}		1.7		pF	f = 1MHz		3
Input-Input Insulation Leakage Current	I_{I-I}		0.5		nA	Relative Humidity = 45% V_{I-I} = 500V, t = 5s		4
Resistance (Input-Input)	R_{I-I}		10^{12}		Ω	V_{I-I} = 500V		4
Capacitance (Input-Input)	C_{I-I}		0.55		pF	f = 1MHz		4
Output Rise-Fall Time (10-90%)	t_r, t_f		35		ns	R_L = 510Ω, C_L = 15pF I_F = 13mA		
Common Mode Transient Immunity at High Output Level	CM_H		100		V/μs	V_{CM} = 10V (peak), V_O (min.) = 2V, R_L = 510Ω, I_F = 0mA	6	7
Common Mode Transient Immunity at Low Output Level	CM_L		-400		V/μs	V_{CM} = 10V (peak), V_O (max.) = 0.8V R_L = 510Ω, I_F = 10mA	6	8

NOTES:

1. Each channel.
2. Measured between pins 1 through 8 shorted together and pins 9 through 16 shorted together.
3. Measured between pins 1 and 2 or 5 and 6 shorted together, and pins 9 through 16 shorted together.
4. Measured between pins 1 and 2 shorted together, and pins 5 and 6 shorted together.
5. The t_{PLH} propagation delay is measured from the 6.5mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 6.5mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
7. CM_H is the max. tolerable common mode transient to assure that the output will remain in a high logic state (i.e., $V_O > 2.0V$).
8. CM_L is the max. tolerable common mode transient to assure that the output will remain in a low logic state (i.e., $V_O < 0.8V$).
9. It is essential that a bypass capacitor (.01 to 0.1μF, ceramic) be connected from pin 10 to pin 15. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20mm (Fig. 7).

*JEDEC Registered Data.

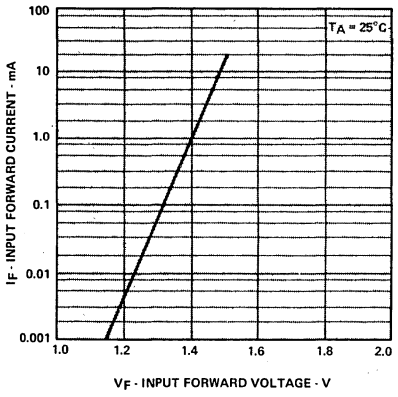


Figure 1. Input Diode Forward Characteristic

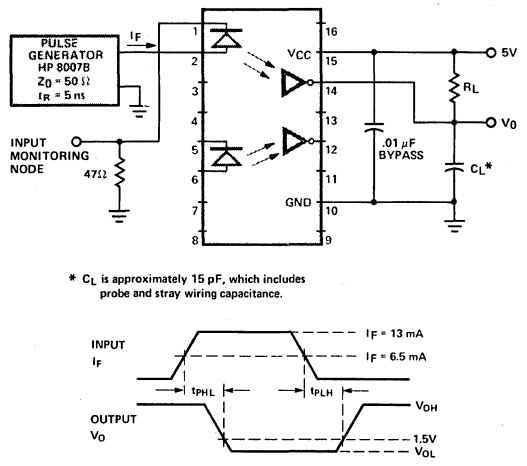


Figure 2. Test Circuit for t_{PHL} and t_{PLH}*

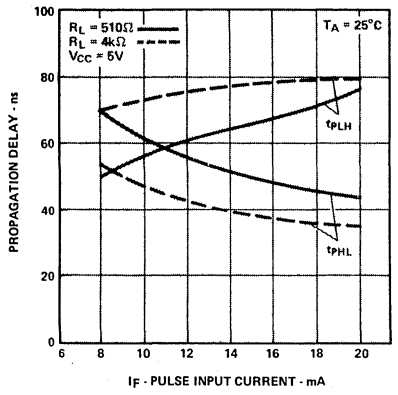


Figure 3. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}

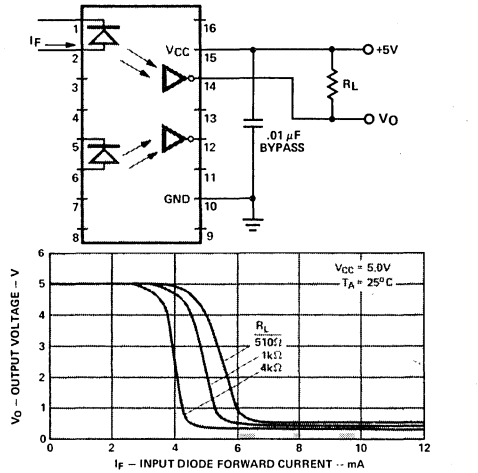


Figure 4. Input-Output Characteristics

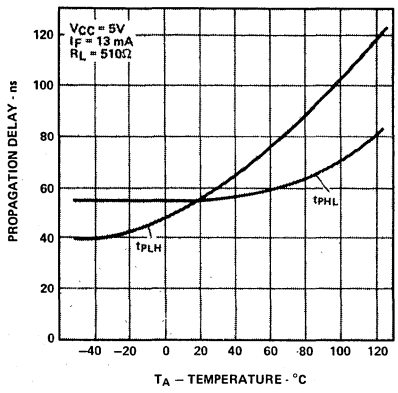


Figure 5. Propagation Delay vs. Temperature

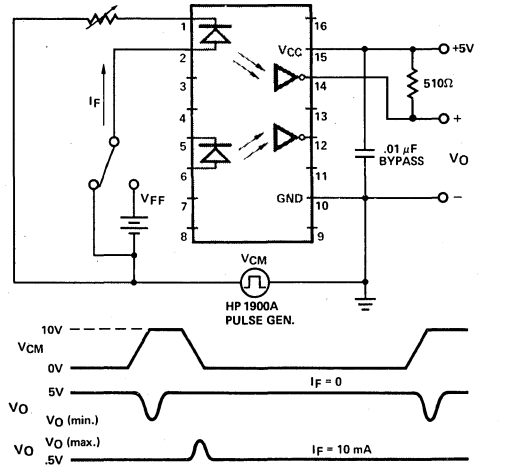


Figure 6. Typical Common Mode Rejection Characteristics/Circuit

*JEDEC Registered Data.

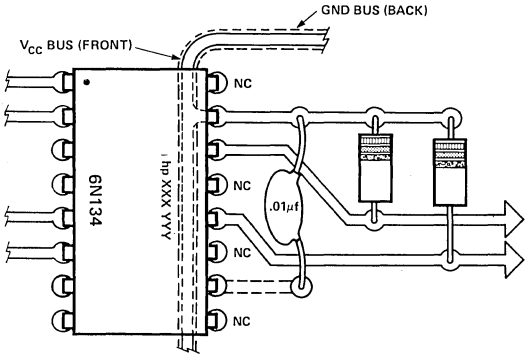


Figure 7. Recommended Circuit Board Layout.

High Reliability Test Program

Hewlett Packard provides standard high reliability test programs, patterned after MIL-M-38510.

- The TXV suffix identifies a part which has been preconditioned and screened per Table IV.
- The TXVB suffix identifies a part which has been preconditioned and screened per Table IV, and comes from a lot which has been subjected to the Group B tests detailed in Table V.

Part Number System

Commercial Product	With TX Screening	With TX Screening Plus Group B
6N134	6N134 TXV	6N134 TXVB

TABLE IV TXV Preconditioning and Screening —100%

Examination or Test	MIL-STD-883 Methods	Conditions
1. Pre-Cap Visual Inspection	2010	Condition B
2. Electrical Test: I_{OH}, V_{OL}, I_{CCH}, I_{CCL}, V_F, BV_R, I_{I-O}		Per Table II, T_A = 25°C
3. High Temperature Storage	1008	168 hrs. @ 150°C
4. Temperature Cycling	1010	-65°C to +150°C
5. Acceleration	2001	5KG, Y_1
6. Helium Leak Test	1014	Test Cond. A
7. Gross Leak Test	1014	Test Cond. C
8. Electrical Test: V_{OL}		Per Table II, T_A = 25°C
9. Burn-In	1015	168 hrs., T_A = 125°C, V_{CC}=5.5V, I_F=13mA, I_O=25mA
10. Electrical Test: Same as Step 2		
11. Evaluate Drift		Max. ΔV_{OL} = ±20%
12. Sample Electrical Test: I_{OH}, V_{OL}, I_{CCH}, I_{CCL}		Per Table II, LTPD = 7, T_A = -55°C
13. Sample Electrical Test: I_{OH}, V_{OL}, I_{CCH}, I_{CCL}		Per Table II, LTPD = 7, T_A = +125°C
14. Sample Electrical Test: t_{PLH}, t_{PHL}		Per Table II, T_A = 25°C, LTPD = 7
15. External Visual	2009	

TABLE V, GROUP B

Examination or Test	MIL-STD-883 Method	Condition	LTPD
Subgroup 1			15
Physical Dimensions	2008	See Product Outline Drawing	
Subgroup 2			20
Solderability	2003	Immersion within 2.5mm of body, 16 terminations	
Subgroup 3			15
Temperature Cycling	1010	Test Condition C	
Thermal Shock	1011	Test Condition A, 5 cycles	
Hermetic Seal, Fine Leak	1014	Test Condition A	
Hermetic Seal, Gross Leak	1014	Test Condition C,	
End Points: I_{OH}, V_{OL}, I_{CCH}, I_{CCL}, V_F, BV_R, I_{I-O}		Per Table II, T_A = 25°C	
Subgroup 4			15
Shock, non-operating	2002	1500 G, t = 0.5 ms, 5 blows in each orientation	
Constant Acceleration	2001	X_1, Y_1, Y_2 5KG, Y_1	
End Points: Same as Subgroup 3			
Subgroup 5			15
Terminal Strength, tension	2004	Test Condition A, 4.5N (1 lb.), 15s	
Subgroup 6			
High Temperature Life	1008	T_A = 150°C	λ = 7
End Points: Same as Subgroup 3			
Subgroup 7			
Steady State Operating Life	1005	V_{CC} = 5.5V, I_F = 13mA, I_O = 25mA, T_A = 125°C	λ = 7
End Points: Same as Subgroup 3			

Emitters/Detectors

Optoelectronics Designer's Catalog 1979

Emitter/Detector System

• Features	• Advantages	• Benefits
Focused optics	Gives higher resolution	Less error No precision alignment of discrete components
Visible light source	Can detect most colors (dye based inks absorb at 700nm not at 800nm)	Not limited to black & white patterns and objects
Photo IC detector	A. Faster response time	A. Can detect more transitions in less time
	B. Speed, linearity, and gain options available	B. Simplified interface electronics
Standard TO-5 package	Mounting hardware readily available	Easy to mount and use
Sealed package	Lens surface is protected from fog and moisture	Reliable operation in indoor/ outdoor environments
Detector IC operates from single ended 3.5V to 20V power supply	Compatible with all IC technologies	Easy to use
Metal-glass package	More rugged and durable than competing plastic designs	Easy to handle and clean
Fully integrated, assembled and tested component system	No precision alignment tools, optical test gear, or special training required	Easy to use Faster design-in
Important performance parameters fully specified and guaranteed	Much more information is available to the user	Assured performance

HEWLETT hp PACKARD
COMPONENTS

NEW PRODUCT

HIGH RESOLUTION OPTICAL REFLECTIVE SENSOR

HEDS-1000

TECHNICAL DATA APRIL 1979

Features

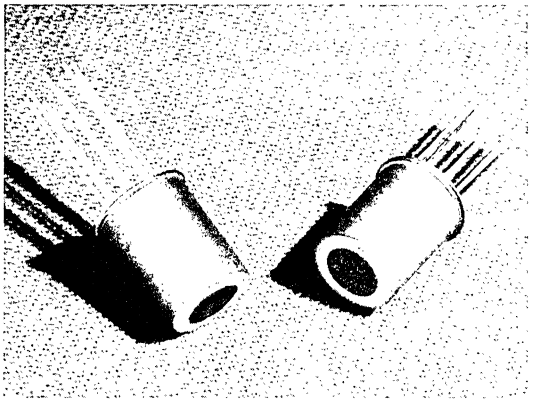
- **FOCUSED EMITTER AND DETECTOR IN A SINGLE PACKAGE**
- **HIGH RESOLUTION — .190mm SPOT SIZE**
- **700nm VISIBLE EMITTER**
- **LENS FILTERED TO REJECT AMBIENT LIGHT**
- **TO-5 MINIATURE SEALED PACKAGE**
- **PHOTODIODE AND TRANSISTOR OUTPUT**
- **SOLID STATE RELIABILITY**

Description

The HEDS-1000 is a fully integrated module designed for optical reflective sensing. The module contains a .178mm (.007 in.) diameter 700nm visible LED emitter and a matched I.C. photodetector. A bifurcated aspheric lens is used to image the active areas of the emitter and the detector to a single spot 4.34mm (.171 in.) in front of the package. The reflected signal can be sensed directly from the photodiode or through an internal transistor that can be configured as a high gain amplifier.

Applications

Applications include pattern recognition, object sizing, optical limit switching, tachometry, defect detection, dimensional monitoring, line locating, mark, and bar code scanning, and paper edge detection.

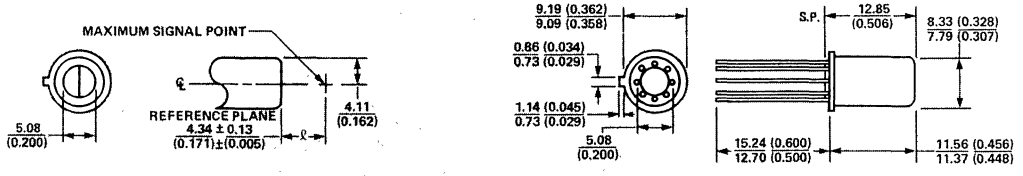


Mechanical Considerations

The HEDS-1000 is packaged in a high profile 8 pin TO-5 metal can with a glass window. The emitter and photodetector chips are mounted on the header at the base of the package. Positioned above these active elements is a bifurcated aspheric acrylic lens that focuses them to the same point.

The sensor can be rigidly secured by commercially available two piece TO-5 style heat sinks, such as Thermalloy 2205, or Aavid Engineering 3215. These fixtures provide a stable reference platform and their tapped mounting holes allow for ease of affixing this assembly to the circuit board.

Package Dimensions



NOTES:
1. ALL DIMENSIONS IN MILLIMETERS AND (INCHES).
2. ALL UNTOLERANCED DIMENSIONS ARE FOR REFERENCE ONLY.
3. THE REFERENCE PLANE IS THE TOP SURFACE OF THE PACKAGE.
4. NICKEL CAN AND GOLD PLATED LEADS.
5. S.P. SEATING PLANE.
6. THE LEAD DIAMETER IS 0.45mm (0.018in.) TYP.

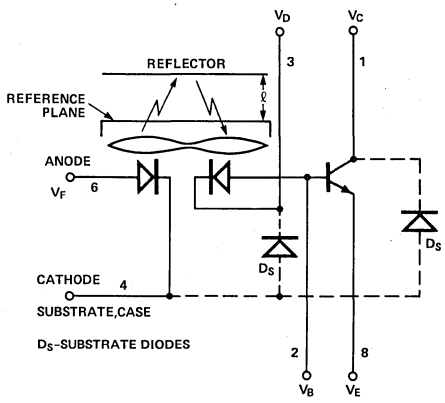
Electrical Operation

The detector section of the sensor can be connected as a single photodiode, or as a photodiode transistor amplifier. When photodiode operation is desired, it is recommended that the substrate diodes be defeated by connecting the collector of the transistor to the positive potential of the power supply and shorting the base-emitter junction of the transistor. Figure 14 shows photocurrent being supplied from the anode of the photodiode to an inverting input of the operational amplifier. The circuit is recommended to improve the reflected photocurrent to stray photocurrent ratio by keeping the substrate diodes from acting as photodiodes.

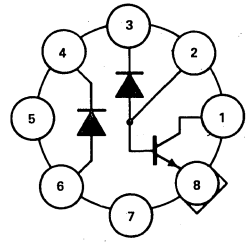
The cathode of the 700nm emitter is physically and electrically connected to the case-substrate of the device. Applications that require modulation or switching of the LED should be designed to have the cathode connected to the electrical ground of the system. This insures minimum capacitive coupling of the switching transients through the substrate diodes to the detector amplifier section.

The HEDS-1000 detector also includes an NPN transistor which can be used to increase the output current of the sensor. A current feedback amplifier as shown in Figure 6 provides moderate current gain and bias point stability.

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



TOP VIEW

PIN	FUNCTION
1	TRANSISTOR COLLECTOR
2	TRANSISTOR BASE, PHOTODIODE ANODE
3	PHOTODIODE CATHODE
4	LED CATHODE, SUBSTRATE, CASE
5	NC
6	LED ANODE
7	NC
8	TRANSISTOR EMITTER

Absolute Maximum Ratings at T_A=25°C

Parameter	Symbol	Min.	Max.	Units	Fig.	Notes
Storage Temperature	T_S	-40	+75	°C		
Operating Temperature	T_A	-20	+70	°C		
Lead Soldering Temperature 1.6mm from Seating Plane			260 for 10 sec.	°C		11
Average LED Forward Current	I_F		50	mA		2
Peak LED Forward Current	I_{FPK}		75	mA	1	1
Reverse LED Input Voltage	V_R		5	V		
Package Power Dissipation	P_P		120	mW		3
Collector Output Current	I_O		8	mA		
Supply and Output Voltage	V_D,V_C,V_E	-5	20	V		10
Transistor Base Current	I_B		5	mA		
Transistor Emitter Base Voltage	V_{EB}		.5	V		

System Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Total Photocurrent (I_{PR}+I_{PS})	I_P			375	nA	T_A=-20°C		
		100	140	250		T_A=25°C, I_F=35mA, V_D=V_C=5V	2,3	4
		50				T_A=70°C	14	
Reflected Photocurrent (I_{PR}) to Internal Stray Photocurrent (I_{PS})	$\frac{I_{PR}}{I_{PS}}$	4	6.5			I_F=35mA, V_C=V_D=5V	3	
Transistor DC Static Current Transfer Ratio	h_{FE}	50				T_A=-20°C / T_A=25°C, V_{CE}=5V, I_C=10μA	4,5	
		100	200					
Slew Rate			.08		V/μs	R_L=100K, I_{PK}=50mA; R_F= 10M, t_{ON}=100μs, Rate = 1kHz	6	
Image Diameter	d		.17		mm	I_F=35mA, ℓ=4.34mm (.171in.)	7,9	8,9
Maximum Signal Point	ℓ	4.21	4.34	4.47	mm	Measured from Reference Plane	8	
50% Modulation Transfer Function	MTF		2.5		$l_{npr/mm}$	I_F=35mA, ℓ=4.34mm	9,10	5,7
Depth of Focus	$\frac{\Delta\ell}{FWHM}$		1.2		mm	50% of I_P at ℓ=4.34mm	8	5
Effective Numerical Aperature	N.A.		.3					
Image Location	D		.51		mm	Diameter Reference to Centerline ℓ=4.34mm		6
Thermal Resistance	Θ_{JC}		85		°C/W			

Detector Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Dark Current	I_{PD}		5	120	pA	T_A=25°C, I_F=0, V_D=5V; Reflection=0%		
				10	nA	T_A=70°C		
Capacitance	C_D		45		pF	V_D=0V, I_P=0, f=1MHz		
Flux Responsivity	$R\phi$		.22		$\frac{A}{W}$	λ=700nm, V_D=5V	11	
Detector Area	A_D		.160		mm^2	Square, with Length=.4mm/Side		

Emitter Electrical/Optical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Forward Voltage	V_F		1.6	1.8	V	I_F=35mA	12	
Reverse Breakdown Voltage	BV_R	5			V	I_R=100μA		
Radiant Flux	ϕ_E	5	9.0		μW	I_F=35mA, λ=700nm	13	
Peak Wavelength	λ_P	680	700	720	nm	I_F=35mA	13	
Thermal Resistance	Θ_{JC}		150		°C/W			
Temperature Coefficient of V_F	$\Delta V_F/\Delta T$		-1.2		mV/°C	I_F=35mA		

Transistor Electrical Characteristics at T_A=25°C

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Fig.	Note
Collector-Emitter Leakage	I_{CEO}		1		pA	V_{CE}=5V		
Base-Emitter Voltage	V_{BE}		.6		V	I_C=10μA, I_B=70nA		
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$		.4		V	I_B=1μA, I_E=10μA		
Collector-Base Capacitance	C_{CB}		.3		pF	f=1MHz, V_{CB}=5V		
Base-Emitter Capacitance	C_{BE}		.4		pF	f=1MHz, V_{BE}=0V		
Thermal Resistance	Θ_{JC}		200		°C/W			

NOTES:
1. 300μs pulse width, 1 kHz pulse rate.
2. Derate Maximum Average Current linearly from 65°C by 6mA/°C.
3. Without heat sinking from T_A = 65° C, derate Maximum Average Power linearly by 12mW/° C.
4. Measured from a reflector coated with a 99% reflective white paint (Kodak 6080) positioned 4.34mm (0.171 in.) from the reference plane.
5. Peak-to-Peak response to black and white bar patterns.
6. Center of image lies within a circle of diameter D relative to the center line of the package.
7. This measurement is made with the lens cusp parallel to the black-white transition.
8. Image size is defined as the distance for the 10%-90% response as the sensor moves over an abrupt black-white edge.
9. (+) indicates an increase in the distance from the reflector to the reference plane.
10. All voltages referenced to Pin 4.
11. CAUTION: The thermal constraints of the acrylic lens will not permit the use of conventional wave soldering procedures. The typical preheat and post cleaning temperatures and dwell times can subject the lens to thermal stresses beyond the absolute maximum ratings and can cause it to defocus.

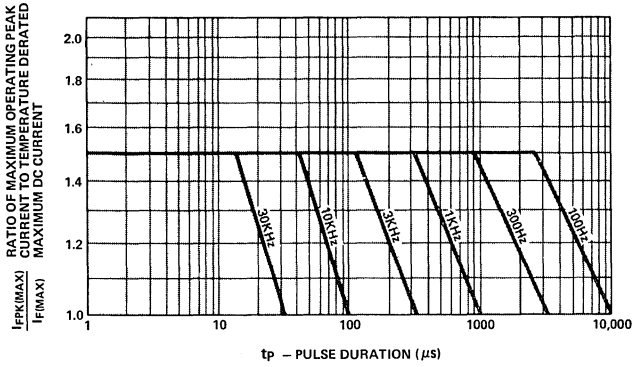


Figure 1. Maximum Tolerable Peak Current vs. Pulse Duration

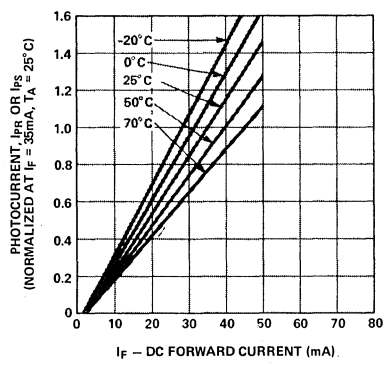


Figure 2. Relative Total Photocurrent vs. LED DC Forward Current

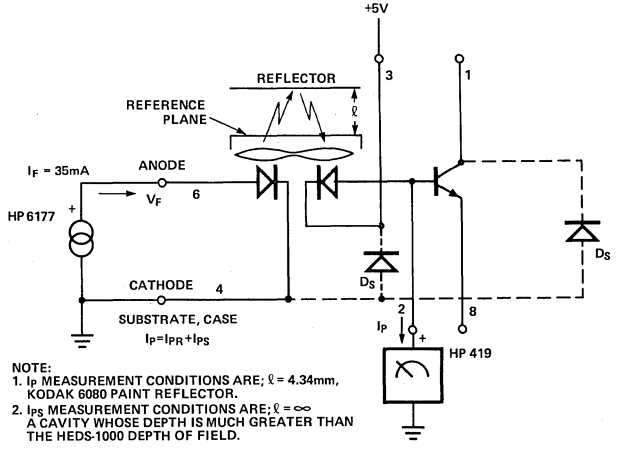


Figure 3. I_P Test Circuit

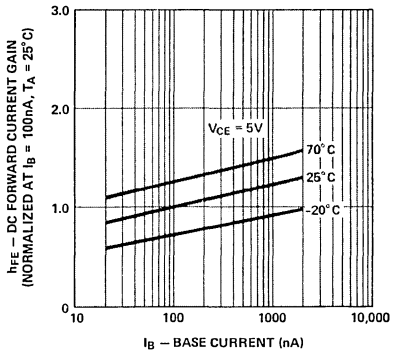


Figure 4. Normalized Transistor DC Forward Current Gain vs. Base Current at Temperature

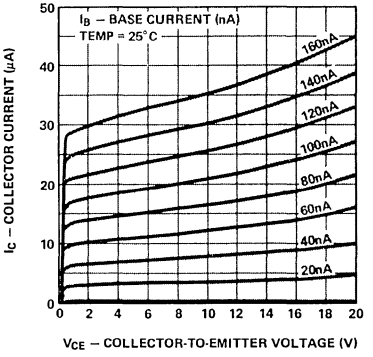


Figure 5. Common Emitter Collector Characteristics

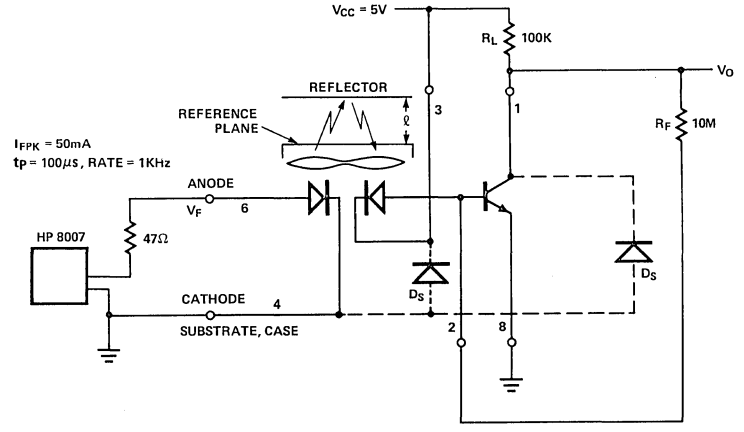


Figure 6. Slew Rate Measurement Circuit

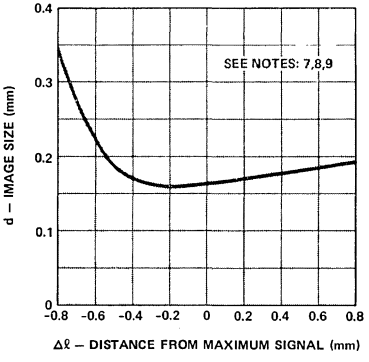


Figure 7. Image Size vs. Maximum Signal Point

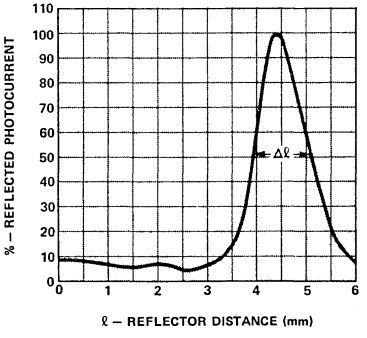


Figure 8. Reflector Distance vs. % Reflected Photocurrent

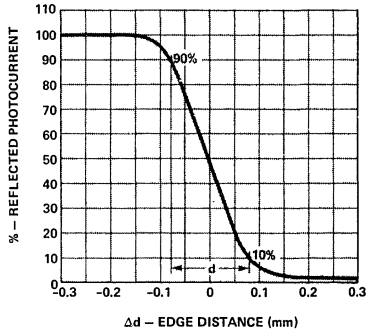


Figure 9. Step Edge Response

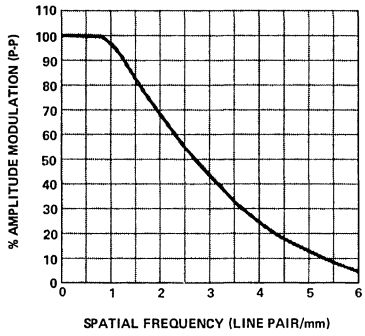


Figure 10. Modulation Transfer Function

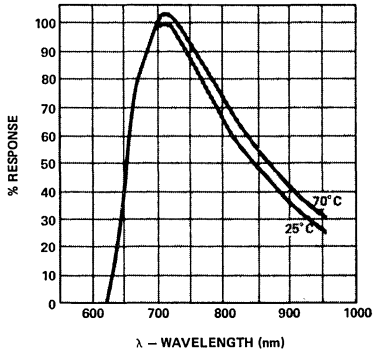


Figure 11. Detector Spectral Response

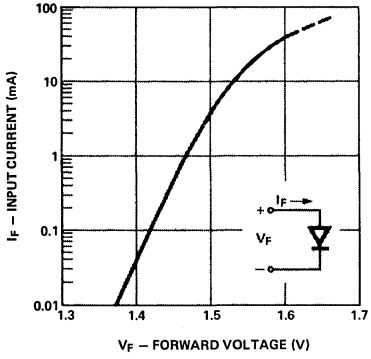


Figure 12. LED Forward Current vs. Forward Voltage Characteristics

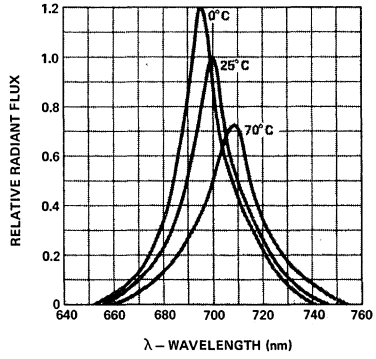


Figure 13. Relative Radiant Flux vs. Wavelength

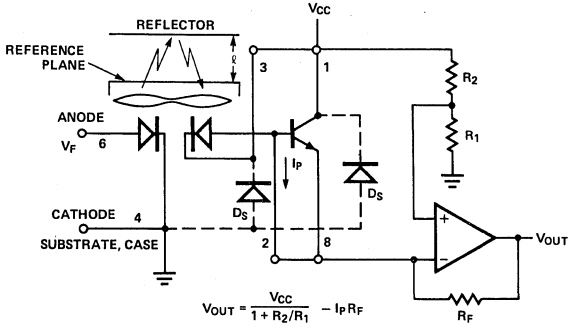


Figure 14. Photodiode Interconnection

Emitters

• Features	○ Advantages	◉ Benefits
Near IR emission	Visible	Facilitates alignment
Functions with most silicon phototransistors and photodiodes	Easy to use	Cost effective implementation
Plastic Package	Low cost	Cost effective implementation
HEMT 3300 uses isotropic LED chip	Provides floodlight type beam	Well suited for applications that require a large area to be irradiated
HEMT 6000 uses surface emitter LED chip	Provides bright spot of light	Facilitates focusing light on active area of photodetector
HEMT 6000 has offset wirebond	Active area of the chip is not masked or shadowed	Facilitates use with fiber optics

Detectors (PIN Photodiodes)

• Features	○ Advantages	◉ Benefits
Offset wirebond	Can be used with fiber optics	Fiber can be placed directly over active area
All HP PIN photodiodes have anti-reflective coating	Converts more incident radiation (light) into photocurrent	High Responsivity
Wide spectral response (ultraviolet through IR)	A single device can cover the light spectrum plus UV and IR	Works with a variety of sources
Low junction capacitance	Wide bandwidth	Can detect high speed pulses
ULTRA Linear	Permits operation over 10 decades	Eliminates the need for equalization

HEWLETT hp PACKARD

COMPONENTS

670nm HIGH RADIANT INTENSITY EMITTER

HEMT-3300

TECHNICAL DATA APRIL 1979

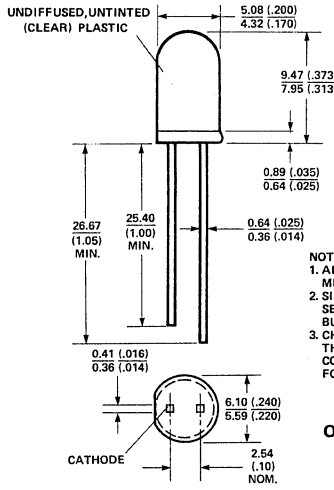
Features

- **HIGH EFFICIENCY**
- **NONSATURATING OUTPUT**
- **NARROW BEAM ANGLE**
- **VISIBLE FLUX AIDS ALIGNMENT**
- **BANDWIDTH: DC TO 3 MHz**
- **IC COMPATIBLE/LOW CURRENT REQUIREMENT**

Description

The HEMT-3300 is a visible, near-IR, source using a GaAsP on GaP LED chip optimized for maximum quantum efficiency at 670 nm. The emitter's beam is sufficiently narrow to minimize stray flux problems, yet broad enough to simplify optical alignment. This product is suitable for use in consumer and industrial applications such as optical transducers and encoders, smoke detectors, assembly line monitors, small parts counters, paper tape readers and fiber optic drivers.

Package Dimensions



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER-PLATED LEADS SEE APPLICATION BULLETIN 3.
3. CHIP CENTERING WITHIN THE PACKAGE IS CONSISTENT WITH FOOTNOTE 3.

Outline T - 1¾

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions	Figure
I_e	Axial Radiant Intensity	200	500		μW/sr	I_F = 10 mA	3,4
K_e	Temperature Coefficient of Intensity		-0.009		°C^{-1}	I_F = 10 mA, Note 1	
η_v	Luminous Efficacy		22		lm/W	Note 2	
$2\Theta_{½}$	Half Intensity Total Angle		22		deg.	Note 3, I_F = 10 mA	6
λ_{PEAK}	Peak Wavelength		670		nm	Measured at Peak	1
$\Delta\lambda_{PEAK}/\Delta T$	Spectral Shift Temperature Coefficient		0.089		nm/°C	Measured at Peak, Note 4	
t_r	Output Rise Time (10% – 90%)		120		ns	I_{PEAK} = 10 mA	
t_f	Output Fall Time (90% – 10%)		50		ns	I_{PEAK} = 10 mA Pulse	
C_O	Capacitance		15		pF	V_F = 0; f = 1 MHz	
BV_R	Reverse Breakdown Voltage	5.0			V	I_R = 100 μA	
V_F	Forward Voltage		1.9	2.5	V	I_F = 10 mA	2
$\Delta V_F/\Delta T$	Temperature Coefficient of V_F		-2.2		mV/°C	I_F = 100 μA	
Θ_{JC}	Thermal Resistance		160		°C/W	Junction to cathode lead at seating plane.	

Notes: 1. I_e (T) = I_e (25°C)exp [K_e(T – 25°C)] 2. $I_v = \eta_v I_e$ where I_v is in candela, I_e in watts/steradian and η_v in lumen/watt.
3. $\Theta_{½}$ is the off-axis angle at which the radiant intensity is half the axial intensity. The deviation between the mechanical and optical axis is typically within a conical half-angle of five degrees. 4. λ_{PEAK} (T) = λ_{PEAK} (25°C) + ($\Delta\lambda_{PEAK}/\Delta T$) (T – 25°C).

Maximum Ratings at T_A=25°C

Power Dissipation ..... 120 mW
(derate linearly from 50°C at 1.6 mW/°C)
Average Forward Current ..... 30 mA
(derate linearly from 50°C at 0.4 mA/°C)
Peak Forward Current ..... See Figure 5
Operating and Storage
Temperature Range ..... -55°C to +100°C
Lead Soldering Temperature ..... 260°C for 5 sec.
(1.6 mm [0.063 inch] from body)

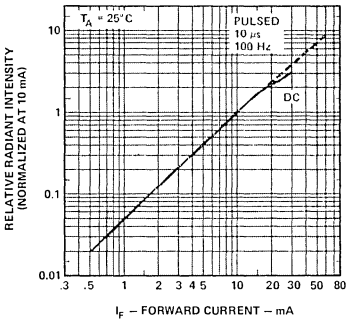


Figure 3. Relative Radiant Intensity versus Forward Current.

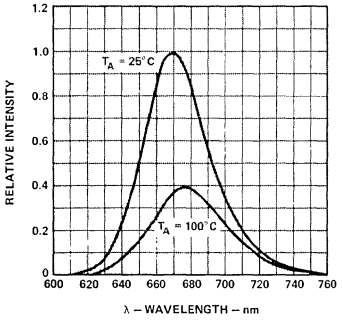


Figure 1. Relative Intensity versus Wavelength.

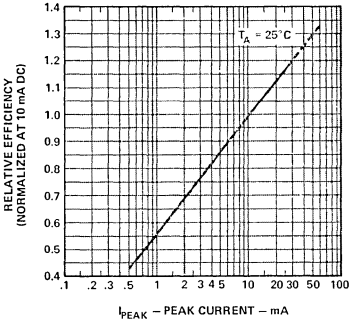


Figure 4. Relative Efficiency (Radiant Intensity per Unit Current) versus Peak Current.

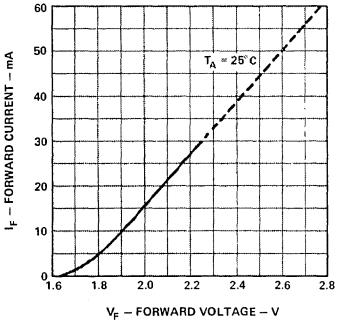


Figure 2. Forward Current versus Forward Voltage.

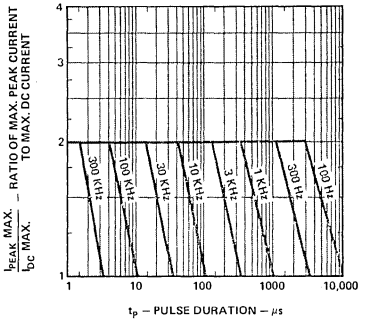


Figure 5. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

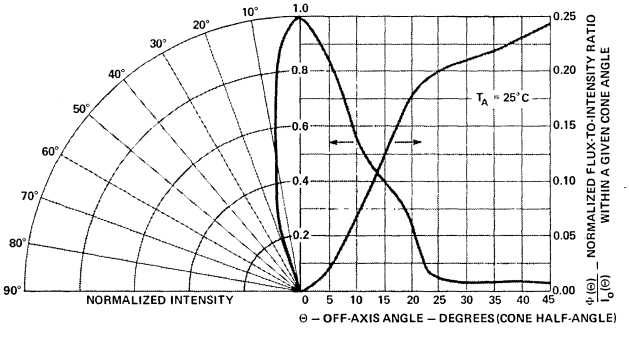


Figure 6. Far-Field Radiation Pattern.

HEWLETT hp PACKARD
COMPONENTS

700nm HIGH INTENSITY SUBMINIATURE EMITTER

HEMT-6000

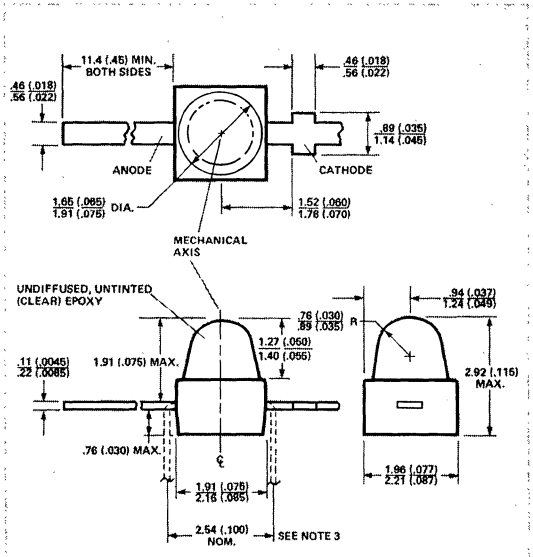
TECHNICAL DATA APRIL 1979

Features

- **HIGH RADIANT INTENSITY**
- **NARROW BEAM ANGLE**
- **NONSATURATING OUTPUT**
- **BANDWIDTH: DC TO 5 MHz**
- **IC COMPATIBLE/LOW CURRENT REQUIREMENT**
- **VISIBLE FLUX AIDS ALIGNMENT**

Description

The HEMT-6000 uses a GaAsP chip designed for optimum tradeoff between speed and quantum efficiency. This optimization allows a flat modulation bandwidth of 5 MHz without peaking, yet provides a radiant flux level comparable to that of 900nm IREDs. The subminiature package allows operation of multiple closely-spaced channels, while the narrow beam angle minimizes crosstalk. The nominal 700nm wavelength can offer spectral performance advantages over 900nm IREDs, and is sufficiently visible to aid optical alignment. Applications include paper-tape readers, punch-card readers, bar code scanners, optical encoders or transducers, interrupt modules, safety interlocks, tape loop stabilizers and fiber optic drivers.



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETRES (INCHES).
2. SILVER-PLATED LEADS. SEE APPLICATION BULLETIN 3.
3. USER MAY BEND LEADS AS SHOWN.
4. EPOXY ENCAPSULANT HAS A REFRACTIVE INDEX OF 1.53.
5. CHIP CENTERING WITHIN THE PACKAGE IS CONSISTENT WITH FOOTNOTE 3.

Maximum Ratings at $T_A = 25°C$

Power Dissipation ..... 50 mW
(derate linearly from 70°C @ 1.0mW/°C)

Average Forward Current ..... 20 mA
(derate linearly from 70°C @ 0.4mA/°C)

Peak Forward Current ..... See Figure 5

Operating and Storage Temperature Range ..... -55° to +100°C

Lead Soldering Temperature ..... 260°C for 5 sec.
[1.6 mm (0.063 in.) from body]

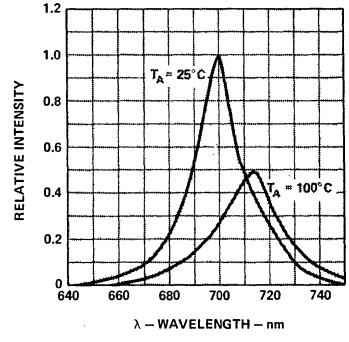


Figure 1. Relative Intensity versus Wavelength.

Electrical/Optical Characteristics at $T_A = 25°C$

Symbol	Description	Min.	Typ.	Max.	Units	Test Conditions	Fig.
I_e	Radiant Intensity along Mechanical Axis	100	250		$\mu W/sr$	I_F = 10 mA	3,4
K_e	Temperature Coefficient of Intensity		-0.005		$°C^{-1}$	Note 1	
η_v	Luminous Efficacy		2.5		lm/W	Note 2	
$2\Theta_{1/2}$	Optical Axis Half Intensity Total Angle		16		deg.	Note 3, I_F = 10 mA	6
λ_{PEAK}	Peak Wavelength (Range)		690-715		nm	Measured @ Peak	1
$\Delta\lambda_{PEAK}/\Delta T$	Spectral Shift Temperature Coefficient		.193		nm/°C	Measured @ Peak, Note 4	
t_r	Output Rise Time (10%-90%)		70		ns	I_{PEAK} = 10 mA	
t_f	Output Fall Time (90%-10%)		40		ns	I_{PEAK} = 10 mA	
C_o	Capacitance		65		pF	V_F = 0; f = 1 MHz	
BV_R	Reverse Breakdown Voltage	5	12		V	I_R = 100 μA	
V_F	Forward Voltage		1.5	1.8	V	I_F = 10 mA	2
$\Delta V_F/\Delta T$	Temperature Coefficient of V_F		-2.1		mV/°C	I_F = 100 μA	
Θ_{JC}	Thermal Resistance		140		°C/W	Junction to cathode lead at 0.79 mm (.031 in) from body	

NOTES:
1. $I_e(T) = I_e\,(25°C)\exp[K_e\,(T - 25°C)]$.
2. $I_v = \eta_v I_e$ where I_v is in candela, I_e in watts/steradian, and η_v in lumen/watt.
3. $\Theta_{1/2}$ is the off-axis angle at which the radiant intensity is half the intensity along the optical axis. The deviation between the mechanical and the optical axis is typically within a conical half-angle of three degrees.
4. $\lambda_{PEAK}\,(T) = \lambda_{PEAK}\,(25°C) + (\Delta\lambda_{PEAK}/\Delta T)\,(T - 25°C)$

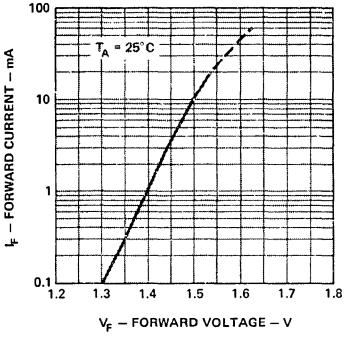


Figure 2. Forward Current versus Forward Voltage.

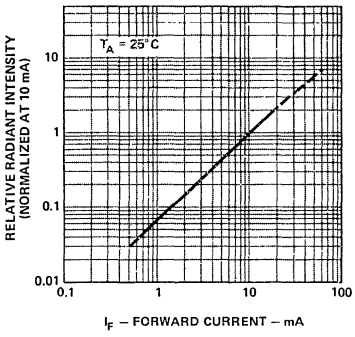


Figure 3. Relative Radiant Intensity versus Forward Current.

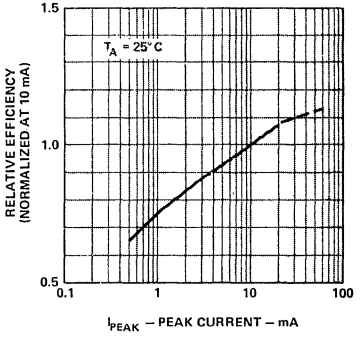


Figure 4. Relative Efficiency (Radiant Intensity per Unit Current) versus Peak Current.

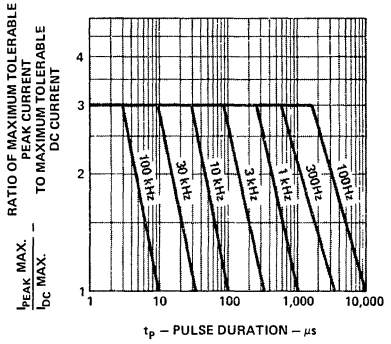


Figure 5. Maximum Tolerable Peak Current versus Pulse Duration. (I_{DC} MAX as per MAX Ratings)

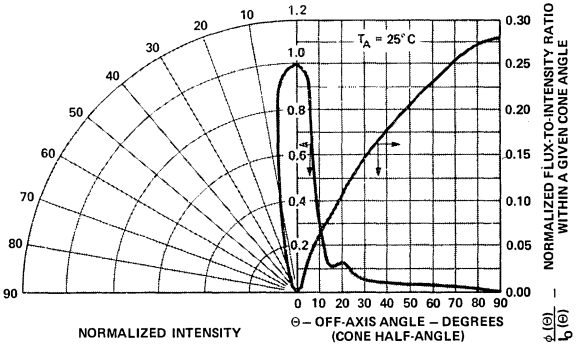


Figure 6. Far-Field Radiation Pattern.

HEWLETT hp PACKARD
COMPONENTS

PIN PHOTODIODES

5082-4200 SERIES

TECHNICAL DATA APRIL 1979

Features

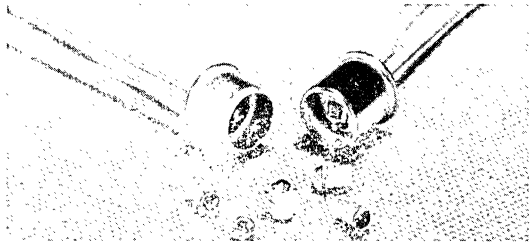
- **HIGH SENSITIVITY (NEP<-108 dBm)**
- **WIDE DYNAMIC RANGE (1% LINEARITY OVER 100 dB)**
- **BROAD SPECTRAL RESPONSE**
- **HIGH SPEED (T_r, T_f<1ns)**
- **STABILITY SUITABLE FOR PHOTOMETRY/ RADIOMETRY**
- **HIGH RELIABILITY**
- **FLOATING, SHIELDED CONSTRUCTION**
- **LOW CAPACITANCE**
- **LOW NOISE**

Active area: 1mm Diam — **5082-4207**, **5082-4203** — **TALL SIZE (TO-18)**

0.5mm Diam — **5082-4204**

5082-4220 — **Short (TO-46)**

0.25mm Magnified 2.5x — **5082-4205** — **Subminiature**



Description

The HP silicon planar PIN photodiodes are ultra-fast light detectors for visible and near infrared radiation. Their response to blue and violet is unusually good for low dark current silicon photodiodes.

These devices are suitable for applications such as high speed tachometry, optical distance measurement, star tracking, densitometry, radiometry, and fiber-optic termination.

The speed of response of these detectors is less than one nanosecond. Laser pulses shorter than 0.1 nanosecond may be observed. The frequency response extends from dc to 1 GHz.

The low dark current of these planar diodes enables detection of very low light levels. The quantum detection efficiency is constant over ten decades of light intensity, providing a wide dynamic range.

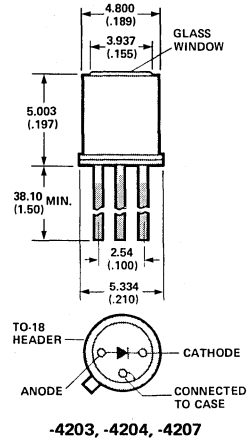
The 5082-4203, -4204, and -4207 are packaged on a standard TO-18 header with a flat glass window cap. For versatility of circuit connection, they are electrically insulated from the header. The light sensitive area of the 5082-4203 and -4204 is 0.508mm (0.020 inch) in diameter and is located 1.905mm (0.075 inch) behind the window. The light sensitive area of the 5082-4207 is 1.016mm (0.040 inch) in diameter and is also located 1.905mm (0.075 inch) behind the window.

The 5082-4205 is in a low capacitance Kovar and ceramic package of very small dimensions, with a hemispherical glass lens.

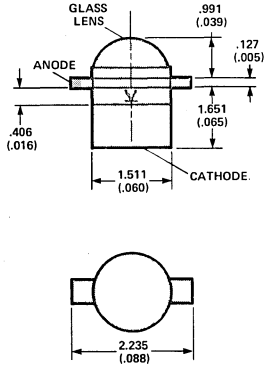
The 5082-4220 is packaged on a TO-46 header with the 0.508mm(0.020 inch) diameter sensitive area located 2.540mm (0.100 inch) behind a flat glass window.

Package Dimensions

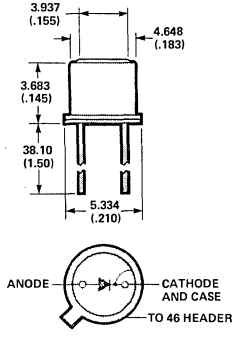
DIMENSIONS IN MILLIMETERS (INCHES).



-4203, -4204, -4207



-4205



-4220

Absolute Maximum Ratings Operating and Storage Temperature -55° to 125°C

Parameter	-4203	-4204	-4205	-4207	-4220	Units
P_{MAX} Power Dissipation [1]	100	100	50	100	100	mW
Steady Reverse Voltage[3]	50	20	50	20	50	volts

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	-4203			-4204			-4205			-4207			-4220			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
R_E, 0= R_ϕ * A	Axial Incidance Response at 770nm[4]		1.0			1.0			1.5*			4.0			1.0		$\frac{\mu A}{mW/cm}$ [2]
A	Active Area[4]		2 x 10^{-3}			2 x 10^{-3}			3 x 10^{-3}*			8 x 10^{-3}			2 x 10^{-3}		cm[2]
R_ϕ	Flux Responsivity 770 nm[5] (Fig. 1, 3)		.5			.5			.5			.5			.5		$\frac{\mu A}{\mu W}$
I_D	Dark Current[6] (Fig. 4)			2.0			0.6			.15			2.5			5.0	nA
NEP	Noise Equivalent Power [7] (Fig. 8)			5.1 x 10^{-14}			2.8 x 10^{-14}			1.4 x 10^{-14}			5.7 x 10^{-14}			8.1 x 10^{-14}	$\frac{W}{\sqrt{Hz}}$
D*	Detectivity[8]	8.7 x 10^{11}			1.6 x 10^{12}			4.0 x* 10^{12}			1.5 x 10^{12}			5.6 x 10^{11}			$\frac{cm\sqrt{Hz}}{W}$
C_j	Junction Capacitance[9] (Fig. 5)		1.5			2.0			0.7			5.6			2.0		pF
C_P	Package Capacitance 10		2			2						2					pF
t_r, t_f	Zero Bias Speed (Rise, Fall Time) 11		300			300			300			300			300		ns
t_r, t_f	Rev.-Bias Speed (Rise, Fall Time) 12			1			1			1			1			1	ns
R_S	Series Resistance			50			50			50			50			50	Ω

*see Note 4.

NOTES:

1. Peak Pulse Power

   When exposing the diode to high level incidance the following photocurrent limits must be observed:

   $$i_p \text{ (avg MAX.)} < \frac{P_{MAX} - P_\phi}{E_c}$$; and in addition:

   $$I_{p(PEAK)} < \frac{1000\ A}{t\ (\mu sec)}$$ or <500mA or $< \frac{I_p \text{ (avg MAX.)}}{f \times t}$

   whichever of the above three conditions is least.

   I_p - photocurrent (A) f - pulse repetion rate (MHz)
   E_c - supply voltage (V) P_ϕ - power input via photon flux
   t - pulse duration (μs) P_{MAX} - max dissipation (W)

   Power dissipation limits apply to the sum of both the optical power input to the device and the electrical power input from flow of photocurrent when reverse voltage is applied.
2. Exceeding the Peak Reverse Voltage will cause permanent damage to the diode. Forward current is harmless to the diode, within the power dissipation limit. For optimum performance, the diode should be reversed biased with E_c between 5 and 20 volts.
3. Exceeding the Steady Reverse Voltage may impair the low-noise properties of the photodiodes, an effect which is noticeable only if operation is diode-noise limited (see Figure 8).
4. The 5082-4205 has a lens with approximately 2.5x magnification; the actual junction area is 0.5 x 10^{-3} cm^2, corresponding to a diameter of 0.25mm (.010"). Specification includes lens effect.
5. At any particular wavelength and for the flux in a small spot falling entirely within the active area, responsivity is the ratio of incremental photodiode current to the incremental flux producing it. It is related to quantum efficiency, η_q in electrons per photon by:

   $$R_\phi = \eta_q \left(\frac{\lambda}{1240}\right)$$

   where λ is the wavelength in nanometers. Thus, at 770nm, a responsivity of 0.5 A/W corresponds to a quantum efficiency of 0.81 (or 81%) electrons per photon.
6. At -10V for the 5082-4204, -4205, and -4207; at -25V for the 5082-4203 and -4220.
7. For (λ, f, Δf) = (770nm, 100Hz, 6Hz) where f is the frequency for a spot noise measurement and Δf is the noise bandwidth, NEP is the optical flux required for unity signal/noise ratio normalized for bandwidth. Thus:

   $$NEP = \frac{I_N/\sqrt{\Delta f}}{R_\phi}$$ where $I_N/\sqrt{\Delta f}$ is the bandwidth — normalized noise current computed from the shot noise formula:

   $I_N/\sqrt{\Delta f} = \sqrt{2qI_D} = 17.9 \times 10^{-15}\sqrt{I_D}$ $(A/\sqrt{Hz})$ where I_D is in nA.
8. Detectivity, D*is the active-area-normalized signal to noise ratio. It is computed: for (λ, f, Δf) = (770nm, 100Hz, 6Hz).

   $$D^* = \frac{\sqrt{A}}{NEP}\left(\frac{cm\sqrt{Hz}}{W}\right)$$ for A in cm^2,
9. At -10V for 5082-4204, -4205, -4207, -4220; at -25V for 5082-4203.
10. Between diode cathode lead and case — does not apply to 5082-4205, -4220.
11. With 50Ω load.
12. With 50Ω load and -20V bias.

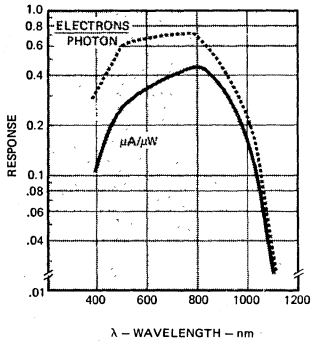


Figure 1. Spectral Response.

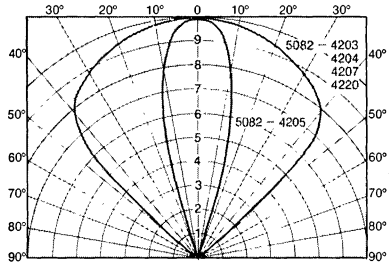


Figure 2. Relative Directional Sensitivity of the PIN Photodiodes.

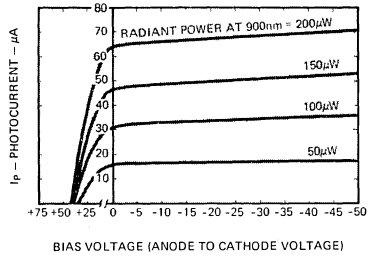


Figure 3. Typical Output Characteristics at λ = 900nm.

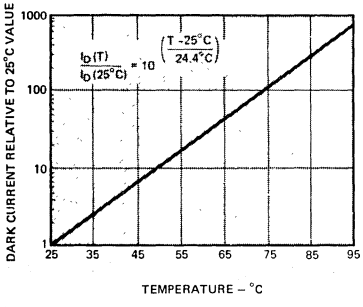


Figure 4. Dark Current at -10V Bias vs. Temperature.

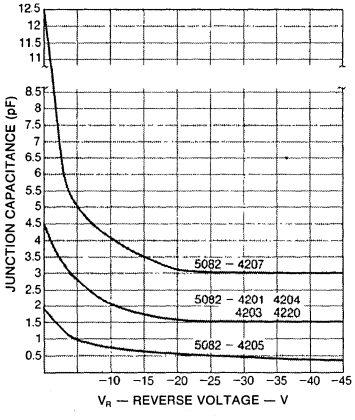


Figure 5. Typical Capacitance Variation With Applied Voltage.

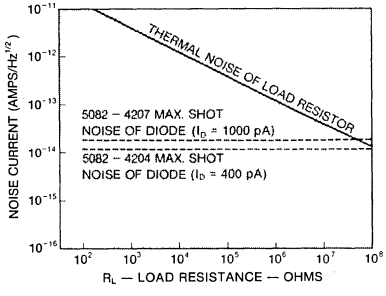


Figure 6. Noise vs. Load Resistance.

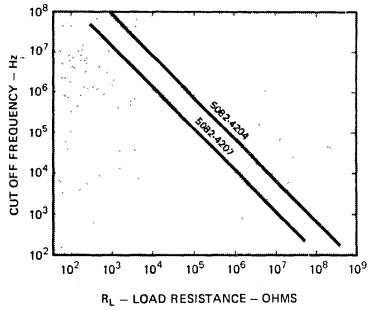


Figure 7. Photodiode Cut-Off Frequency vs. Load Resistance (C = 2pF).

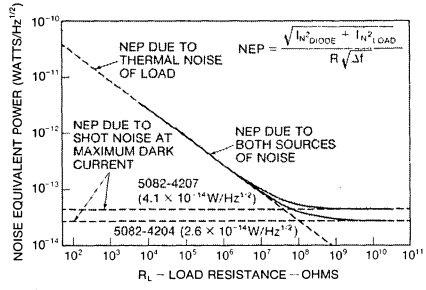


Figure 8. Noise Equivalent Power vs. Load Resistance.

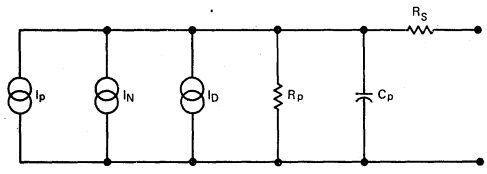


Figure 9. Photodiode Equivalent Circuit.

Ip=Signal current ≈ 0.5μA/μW x flux input at 770 nm
IN = Shot noise current
<1.2 x 10-14 amps/Hz1/2(5082-4204)
<4 x 10-14 amps/Hz1/2(5082-4207)
ID= Dark current
<600 x 10-12 amps at -10 V dc (5082-4204)
<2500 x 10-12 amps at -10 V dc (5082-4207)
RP = 10¹¹Ω
RS = <50Ω

Application Information

NOISE FREE PROPERTIES

The noise current of the PIN diodes is negligible. This is a direct result of the exceptionally low leakage current, in accordance with the shot noise formula $I_N = (2qI_R\Delta f)^{1/2}$. Since the leakage current does not exceed 600 picoamps for the 5082-4204 at a reverse bias of 10 volts, shot noise current is less than 1.4×10^{-14} amp $Hz^{-1/2}$ at this voltage.

Excess noise is also very low, appearing only at frequencies below 10 Hz, and varying approximately as 1/f. When the output of the diode is observed in a load, thermal noise of the load resistance (R_L) is 1.28×10^{-10} $(R_L)^{-1/2} \times (\Delta f)^{1/2}$ at 25°C, and far exceeds the diode shot noise for load resistance less than 100 megohms (see Figure 6). Thus in high frequency operation where low values of load resistance are required for high cut-off frequency, all PIN photodiodes contribute virtually no noise to the system (see Figures 6 and 7).

HIGH SPEED PROPERTIES

Ultra-fast operation is possible because the HP PIN photodiodes are capable of a response time less than one nanosecond. A significant advantage of this device is that the speed of response is exhibited at relatively low reverse bias (−10 to −20 volts).

OFF-AXIS INCIDANCE RESPONSE

Response of the photodiodes to a uniform field of radiant incidance E_e, parallel to the polar axis is given by $I = (RA) \times E_e$ for 770nm. The response from a field not parallel to the axis can be found by multiplying (RA) by a normalizing factor obtained from the radiation pattern at the angle of operation. For example, the multiplying factor for the 5082-4207 with incidance E_e at an angle of 40° from the polar axis is 0.8. If $E_e = 1mW/cm^2$, then $I_p = k \times (RA) \times E_e$; $I_p = 0.8 \times 4.0 \times 1 = 3.2$ μamps.

SPECTRAL RESPONSE

To obtain the response at a wavelength other than 770nm, the relative spectral response must be considered. Referring to the spectral response curve, Figure 1, obtain response, X, at the wavelength desired. Then the ratio of the response at the desired wavelength to response at 770nm is given by:

$$\text{RATIO} = \frac{X}{0.5}$$

Multiplying this ratio by the incidance response at 770nm gives the incidance response at the desired wavelength.

ULTRAVIOLET RESPONSE

Under reverse bias, a region around the outside edge of the nominal active area becomes responsive. The width of this annular ring is approximately 25μm (0.001 inch) at −20V, and expands with higher reverse voltage. Responsivity in this edge region is higher than in the interior, particularly at shorter wavelengths; at 400nm the interior, responsivity is 0.1 A/W while edge responsivity is 0.35 A/W. At wavelengths shorter than 400nm, attenuation by the glass window affects response adversely. Speed of response for edge incidance is t_r, $t_f \approx 300ns$.

5082-4205 MOUNTING RECOMMENDATIONS

a. The 5082-4205 is intended to be soldered to a printed circuit board having a thickness of from 0.51 to 1.52mm (0.02 to 0.06 inch).
b. Soldering temperature should be controlled so that at no time does the case temperature approach 280°C. The lowest solder melting point in the device is 280°C (gold-tin eutectic). If this temperature is approached, the solder will soften, and the lens may fall off. Lead-tin solder is recommended for mounting the package, and should be applied with a small soldering iron, for the shortest possible time, to avoid the temperature approaching 280°C.
c. Contact to the lens end should be made by soldering to one or both of the tabs provided. Care should be exercised to prevent solder from coming in contact with the lens.
d. If printed circuit board mounting is not convenient, wire leads may be soldering or welded to the devices using the precautions noted above.

LINEAR OPERATION

Having an equivalent circuit as shown in Figure 9, operation of the photodiode is most linear when operated with a current amplifier as shown in Figure 10.

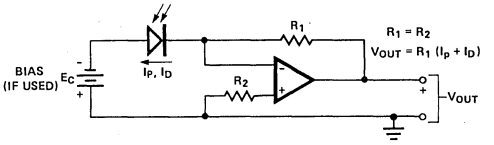


Figure 10. Linear Operation.

Lowest noise is obtained with $E_c = 0$, but higher speed and wider dynamic range are obtained if $5 < E_c < 20$ volts. The amplifier should have as high an input resistance as possible to permit high loop gain. If the photodiode is reversed, bias should also be reversed.

LOGARITHMIC OPERATION

If the photodiode is operated at zero bias with a very high impedance amplifier, the output voltage will be:

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{kT}{q} \cdot \ln \left(1 + \frac{I_P}{I_S}\right)$$

where $I_S = I_F \left(e^{\frac{qV}{kT}} - 1\right)^{-1}$ at $0 < I_F < 0.1mA$

using a circuit as shown in Figure 11.

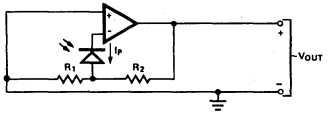


Figure 11. Logarithmic Operation.

Output voltage, V_{OUT}, is positive as the photocurrent, I_P, flows back through the photodiode making the anode positive.

Applications Information

- Applications Manual
- Application Bulletins Summary
- Applications
- Application Notes Summary

Optoelectronics Designer's Catalog 1979

HEWLETT hp PACKARD
COMPONENTS

NEW PRODUCT

OPTOELECTRONICS APPLICATIONS MANUAL

HPBK - 1000

TECHNICAL DATA APRIL 1979

Features

- **Clarifies terms, definitions, symbols, and units of energy measurement used in generic, radiometric, and photometric contexts**
- **Generously illustrated with large, clear isometric diagrams, circuit diagrams, and mathematical developments of major concepts**
- **Explains theory, mechanics, and operation of optoelectronic components; text is presented in a how-to-do-it fashion.**
- **Each chapter focuses on a complete handling of an optoelectronic discipline. (See Table of Contents section for specifics).**

Description

Practical solutions to the most common applications problems of optoelectronic devices are fully analyzed in Hewlett-Packard's Optoelectronics Applications Manual. Written as both a practical guide to the use of optoelectronic devices and as a foundation for the development of new design ideas, this volume demonstrates the broad potential for these components that exists in systems being implemented today.

Of special interest to experienced designers is the Manual's treatment of CTR degradation, a controversial and frequently misunderstood subject among users of optocouplers. The Manual also shows how microprocessors can be interfaced with monolithic displays. In addition, the reader will find a section detailing the six advantages of on-board-integrated-circuit (OBIC) displays that offset their initial cost.

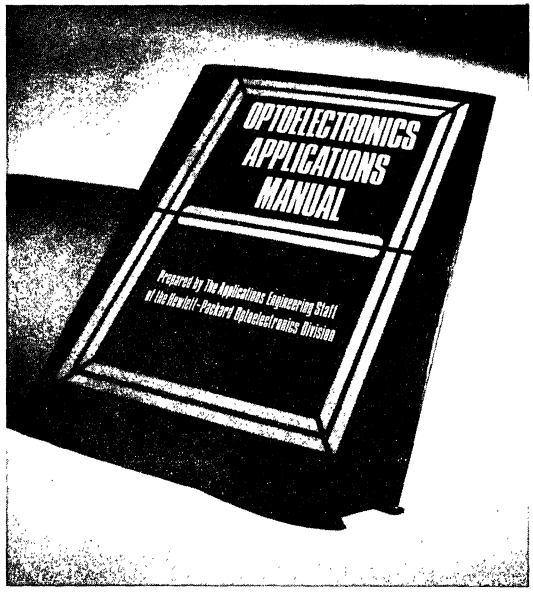
The contents of the book are divided into nine discrete categories, fully explained in the Table of Contents section.

Table of Contents

Chapter 1. Presents a simplified review of the theory of LED operation, introducing LED devices to engineers.

Chapter 2. Explores the design and packaging of LED lamps, emphasizing their applications and such considerations as safe design, driving arrays, backlighting, and communications and signaling applications.

Chapter 3. Reviews the theory and important parameters of optocouplers, covering both digital and analog applications of isolators and the techniques of design allowances for CTR degradation.



Optoelectronics Applications Manual
Part No. HPBK-1000, 279 Pages
Prepared by the Applications Engineering Staff of the
Hewlett-Packard Optoelectronics Division

Chapter 4. Covers the theory and applications of high-speed PIN photodiodes.

Chapter 5. Examines LED displays, display subsystems, and data pathing, focusing on the characteristics and uses of the major displays, with particular emphasis on their interface with microprocessor systems.

Chapter 6. Explains the objectives of contrast enhancement and offers numerous practical examples of techniques and materials which can be used to improve display appearance.

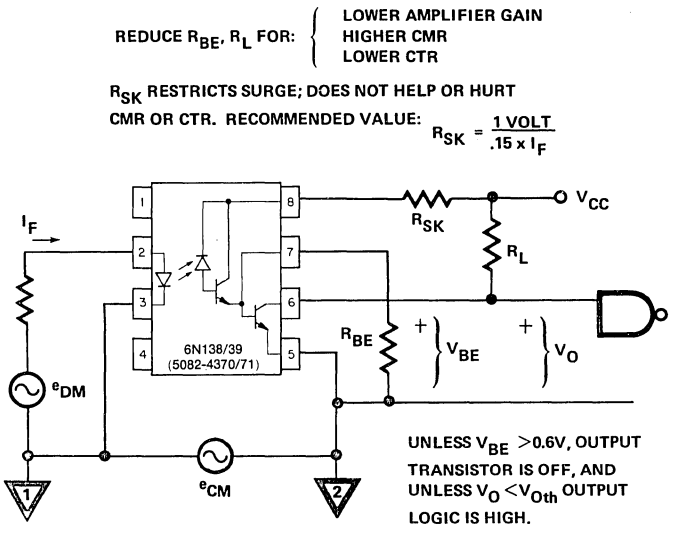
Chapter 7. Offers practical insights into photometry and radiometry and recommends techniques for accurate emitted energy measurement.

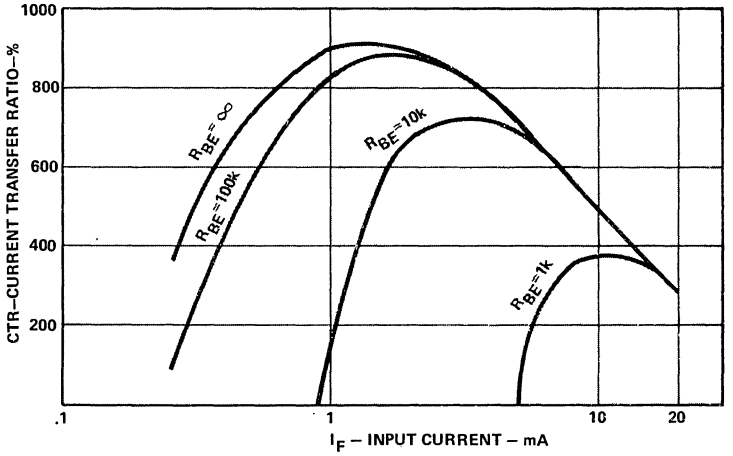
Chapter 8. Discusses the reliability of LED products and puts failure modes into perspective with comparisons to other semiconductor devices.

Chapter 9. Covers the basic principles of lead forming, soldering, cleaning and heat sinking as they apply to LED optoelectronic components.

Example

Optocouplers offer a unique solution to the problem of high common mode transient voltages in data transmission systems. In Chapter 3 on optocouplers, the reader will find numerous examples of how to optimize the design of data transmission systems using optocouplers as line receivers. Below is an example of such an application taken from the manual.





Amplifier Desensitization for CMR Enhancement by Lowering CTR.

Ordering

The Hewlett-Packard Optoelectronics Applications Manual is published by McGraw-Hill Company. Copies can either by purchased through McGraw-Hill, or, for your convenience, from your Hewlett-Packard franchised distributor. When ordering from an HP distributor, ask for the HPBK-1000.

Application Bulletins

Below is a brief summary of all Optoelectronic Application Bulletins which are not included in the catalog. (AB 3 is included in its entirety). All of the Bulletins are available from your local HP Sales Office or nearest HP Components Franchised Distributor or Representative.

APPLICATION BULLETIN 1
Construction and Performance of High Efficiency Red, Yellow and Green LED Materials

The high luminous efficiency of Hewlett-Packard's High Efficiency Red, Yellow and Green lamps and displays is made possible by a new kind of light emitting material utilizing a GaP transparent substrate. This application bulletin discusses the construction and performance of this material as compared to standard red GaAsP and red GaP materials.

APPLICATION BULLETIN 3
Soldering Hewlett-Packard Silver Plated Lead Frame LED Devices ..... **page 251**

APPLICATION BULLETIN 4
Detection and Indication of Segment Failures in Seven Segment LED Displays

The occurrence of a segment failure in certain applications of seven segment displays can have serious consequences if a resultant erroneous message is read by the viewer. This application bulletin discusses three techniques for detecting open segment lines and presenting this information to the viewer.

APPLICATION BULLETIN 52
Large Monolithic LED Displays

The trend to incorporate more complex functions into smaller package configurations that are portable and battery powered is reaching a point where the limiting items are the space and power constraints imposed upon the display at the operator-to-machine interface. The large monolithic LED display has been designed to meet many of these constraints. This application bulletin describes the beneficial features of a large monolithic LED display and presents circuits which interface the display to CMOS logic and to a microprocessor.

APPLICATION BULLETIN 53
Interfacing the HDSP-6504/6508 16 segment Alphanumeric Display

The man machine interface can most efficiently be bridged through the use of an Alphanumeric Display. Advances in monolithic LED manufacturing technology have permitted the introduction of an alphanumeric display using a sixteen segment font with a decimal and colon. The use of this new display is the topic of this application bulletin and it is intended to assist the designer in the following areas:

1. Electrical drive conditions;
2. Design of a stand-alone ASCII to eighteen segment decoder, and;
3. A 6800 microprocessor interface.

APPLICATION BULLETIN 54
Mechanical Handling of Subminiature LED Lamps and Arrays

The Need for Careful Mechanical Handling

Hewlett-Packard manufactures a series of individual LED lamps and lamp arrays that are very small epoxy encapsulated devices. These devices are classified as having a SUBMINIATURE package configuration. When carefully installed on a printed circuit board, these devices will reliably function with a long predictable operating life.

To obtain long operating life, these subminiature devices must be carefully installed on the printed circuit board in such a manner as to insure the integrity of the encapsulating epoxy. This will in turn maintain the integrity of the device by not permitting mechanical and thermal stresses to induce strains on the LED die attach and wire bonds which may cause failure.

This application bulletin describes the subminiature package assembly, the package's mechanical limitations and offers specific suggestions for proper installation.

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APPLICATION BULLETIN 3

Soldering Hewlett-Packard Silver Plated Lead Frame LED Devices

INTRODUCTION

Since the price of gold has increased several times over past years, the cost of a gold plated lead frame has increased substantially above the cost of a silver plated lead frame. The impact of this increase in cost has been industry wide.

By using silver plating, no additional manufacturing process steps are required. Silver has excellent electrical conductivity. LED die attach and wire bonding to a silver lead frame is accomplished with the same reliability as with a gold lead frame. Also, soldering to a silver lead frame provides a reliable electrical and mechanical solder joint. Soldering silver plated lead frame LED devices into a printed circuit board is not more complicated than soldering LED devices with gold plated lead frames. This application bulletin offers some suggestions on how to solder HP silver plated lead frame LED devices.

THE SILVER PLATING

The silver plating process is performed as follows: The lead frame base metal is activated (cleaned) and then plated with a copper strike, nominally 50 microinches (0.00127mm) thick. Then a minimum 150 microinch (0.00381mm) thick plating of silver is added. A "brightener" is usually added to the silver plating bath to insure an optimum surface texture to the silver plating. The term "brightener" comes from the medium bright surface reflectance of the silver plate.

Since silver is porous with respect to oxygen, the copper strike acts as an oxygen barrier for the lead frame base metal. Thus, oxide compounds of the base metal are prevented from forming underneath the silver plating. Copper readily diffuses into silver forming a solution that has a low temperature eutectic point. The interdiffusion between the copper strike and the silver overplate improves the solderability of the overall plating system. If basic soldering time and temperature limits are not exceeded, a lead frame base metal-copper-silver-solder metallurgical bonding system will be obtained.

THE EFFECT OF TARNISH

Silver reacts chemically with sulfur to form the tarnish, silver sulfide (Ag_2S). The build-up of tarnish is the primary reason for poor solderability. However, the density of the tarnish and the kind of solder flux used actually determine the solderability. As the density of the tarnish increases, the more active the flux must be to penetrate and remove the tarnish layer. Some recommended fluxes and cleaner/surface conditions are discussed in the "Solder, Flux and Cleaners" section.

STORAGE AND HANDLING

The best technique for insuring good solderability of a silver plated lead frame device is to prevent the formation of tarnish. This is easily accomplished by preventing the leads from being exposed to sulfur and sulfur compounds. The two primary sources of sulfur are free air and most paper products such as paper sacks and cardboard containers. The best defense against the formation of tarnish is to keep silver lead frame devices in protective packaging until just prior to the soldering operation. One way to accomplish this is to store the LED devices unwrapped in their original packaging as received from HP. For example, Hewlett-Packard ships its seven segment display products in plastic tubes which are sealed air tight in polyethylene. It is best to leave the polyethylene intact during storage and open just prior to soldering.

Listed below are a few suggestions for storing silver lead frame devices.

1. Store the devices in the original wrapping unopened until just prior to soldering.
2. If only a portion of the devices from a single tube are to be used, tightly re-wrap the plastic tube containing the unused devices in the original or a new polyethylene sheet to keep out free air.
3. Loose devices may be stored in zip-lock or tightly sealed polyethylene bags.
4. For long term storage of parts, place one or two petroleum napthalene mothballs inside the plastic package containing the devices. The evaporating napthalene creates a vapor pressure inside the plastic package which keeps out free air.
5. Any silver lead frame device may be wrapped in "Silver Saver" paper for positive protection against the formation of tarnish. "Silver Saver" is manufactured by:

   The Orchard Corporation
   1154 Reco Avenue
   St. Louis, Missouri 63126 (312) 822-3888

6. To reduce shelf storage time, it will be worthwhile to use inventory control to insure that the devices first received will be the first devices to be used.

   One caution: The adhesives used on pressure sensitive tapes such as cellophane, electrical and masking tape can soak through silver protecting papers and may leave an adhesive film on the leads. This film reduces solderability and should be removed with freon T-P35, freon T-E35 or equivalent prior to soldering.

SOLDER, FLUX AND CLEANERS

The solder most widely used for soldering electronic components into printed circuit boards is Sn60 (60% tin and 40% lead) per federal standard QQ-S-571. Two alternates are the eutectic composition Sn63 and the 2% silver solder Sn62.

As the device leads pass through the solder wave of a flow solder process, the tin in the solder scavenges silver from the silver plating and forms one of two silver-tin intermetallics (Ag_6Sn or Ag_3Sn). This silver in the molten solder should not be considered a contaminant. As the silver content increases, the rate of scavenging decreases and the probability of obtaining the desired base metal-copper-silver-solder metallurgical system is improved. The result is that the silver content in solder, which reaches a maximum of 2-1/2% in Sn60 at 230°C, aids in producing reliable solder joints on silver plated lead frames.

Solder flux classifications per federal standard QQ-S-571, listed in order of increasing strength, are as follows:

Type R: Non-Activated Rosin Flux
Type RMA: Mildly Activated Rosin Flux
Type RA: Activated Rosin Flux
Type AC: Organic Acid Flux, Water Soluble

Suggested applications of these flux types with respect to various tarnish levels are as follows:

Silver plated lead frames that are clean, contaminant and tarnish free may be soldered using a Type R flux such as Alpha 100.

Minor Tarnish

Since some minor tarnish or other contaminant may be present on the leads, a type RMA flux such as Alpha 611 or 611 Foam, Kester 197 or equivalent is recommended. Minor tarnish may be identified by reduced reflectance of the ordinarily medium bright surface of the silver plating. Type RMA fluxes which meet MIL-F-14256 are used in the construction of telephone communication, military and aero space equipment.

Mild Tarnish

For a mild tarnish, a type RA flux such as Alpha 711-35, Alpha 809 foam, Kester 1544, Kester 1585 or equivalent should be used. A mild tarnish may be identified by a light yellow tint to the surface of the silver plating.

Moderate Tarnish

A type AC water soluable flux such as Alpha 830, Alpha 842, Kester 1429 or 1429 foam, Lonco 3355 or equivalent will give acceptable results on surface conditions up to a moderate tarnish. A moderate tarnish may be identified by a light yellow-tan color on the surface of the silver plating.

If a more severe tarnish is present, such as a heavy tarnish identified by a dark tan to black color, a cleaner/surface conditioner must be used. Some possible cleaner/surface conditioners are Alpha 140, Alpha 174, Kester 5560, and Lonco TL-1. The immersion time for each cleaner/surface conditioner will be just a few seconds and each is used at room temperature. For example, Alpha 140 will remove severe tarnish almost upon contact; therefore, the immersion time need not exceed 2 seconds. These cleaner/surface conditioners are acidic formulations. Therefore, thoroughly wash all devices which have been cleaned with a cleaner/surface conditioner in cold water. A hot water wash will cause undue etching of the surface of the silver plating. A post rinse in deionized water is advisable.

CAUTION: These cleaner/surface conditioners may etch exposed glass and may have a detrimental effect upon the glass filled encapsulating epoxies used in optoelectronic devices. Complete immersion of an optoelectronic device into a surface conditioner solution is NOT recommended. For best results, immerse only the tarnished leads and do not expose the encapsulating epoxy to the solutions.

The cleaning of printed circuit boards after soldering is important to remove ionic contaminants and increase circuit reliability. When a Type RMA or Type RA flux is used, vapor clean with an azeotrope of fluorocarbon F113 and approximately 15% alcohol by weight. Some equivalent products are Allied Chemical Genesolve DI-15/DE-15, Blaco-Tron DE-15/DI-15 and Arklone K. A Type RMA or Type RA flux is a mixture of basic Type R rosin flux and an organic acid. The fluorocarbon F113 removes the residual rosin and the alcohol removes the residual active ions. Room temperature cleaning may be accomplished by using Freon T-E35, T-P35 or equivalent. When a Type AC flux is used, wash thoroughly with water. Specific cleaning processes are suggested in the soldering process section.

SOLDERING PROCESS

Before the actual soldering begins, the printed circuit boards and components to be soldered should be free of dirt, oil, grease, finger prints and other contaminants. Fluorinated cleaners such as Freon T-P35 may be used to preclean both the printed circuit boards and LED devices. Operators may wear cotton gloves to prevent finger prints when loading components into the printed circuit boards.

If the silver lead frames have acquired an unacceptable layer of tarnish, remove this tarnish layer with a cleaner/surface conditioner just prior to soldering. Since a cleaner/surface conditioner does slightly etch the surface of the silver plating, the silver leads are now more susceptible to tarnish formation. Therefore, use a cleaner/surface conditioner only on those silver lead frame devices which will be soldered within a four hour time period. The effect of various tarnish levels on the choice of flux is discussed in the previous section.

Many of Hewlett-Packard's LED Lamps and Display products have a soldering specification of 230°C (446°F) for a maximum time period of 5 seconds. Therefore, in a flow solder operation adjust the solder temperature and belt speed to conform to this specification, or as is specified on the device data sheet. The flow solder operation may now proceed in a normal fashion. For best results, any one single lead should be immersed in molten solder for as short a time period as possible. At a solder

temperature of 230°C (446°F), Sn60 solder will dissolve silver at the rate of 60 microinches per second. Therefore, with an initial silver plating thickness of 150 microinches, an immersion time of 2 seconds will provide the desired lead base metal-copper-silver-solder metallurgical system. At a solder temperature of 260°C (500°F), Sn60 solder will dissolve silver at the rate of 80 microinches per second. These dissolving rates decrease as the silver content increases in the molten solder bath.

Post cleaning of soldered assemblies when a type RMA or Type RA flux has been used may be accomplished via a vapor cleaning process in a degreasing tank, using an azeotrope of fluorocarbon F113 and alcohol as the cleaning agent. A recommended method is a 15 second suspension in vapors, a 15 to 30 second spray wash in liquid cleaner, and finally a one minute suspension in the vapors. When a water soluable Type AC flux such as Alpha 830 or Kester 1429/1429F is used, the following post cleaning process is suggested: thoroughly wash with water, neutralize using Alpha 2441 or Kester 5760 or Kester 5761 foaming, then thoroughly wash with water and air dry.

CAUTION: The use of tetrachloro-di-fluoroethane (F112), acetone, trichloroethylene, MEK, carbon tetrachloride and similar solvents as cleaning agents is NOT recommended, as these cleaners will attack or dissolve the epoxies used in optoelectronic devices.

A WORD ABOUT PRINTED CIRCUIT BOARDS

Printed circuit boards, either single sided, double sided or multilayer, may be manufactured with plated through holes with a metal trace pad surrounding the hole on both sides of the printed circuit board. The plated through hole is desirable to provide a sufficient surface for the solder to wet, and thereby be pulled up by capillary attraction along the lead through the hole to the top of the printed circuit board. This provides the best possible solder connection between the printed circuit board and the leads of the LED device.

SOLDERED LEADS

Figure 1 illustrates an ideally soldered lead. The amount of solder which has flowed to the top of the printed circuit board is not critical. A sound electrical and mechanical joint is formed.

Figure 2 illustrates a soldered lead which is undesirable.

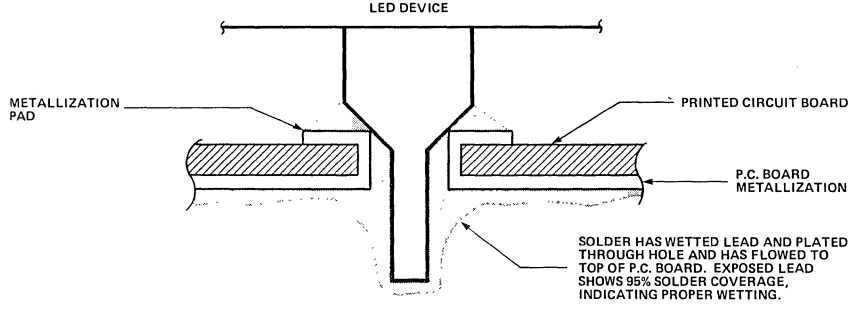

Figure 1. Ideally Soldered Lead

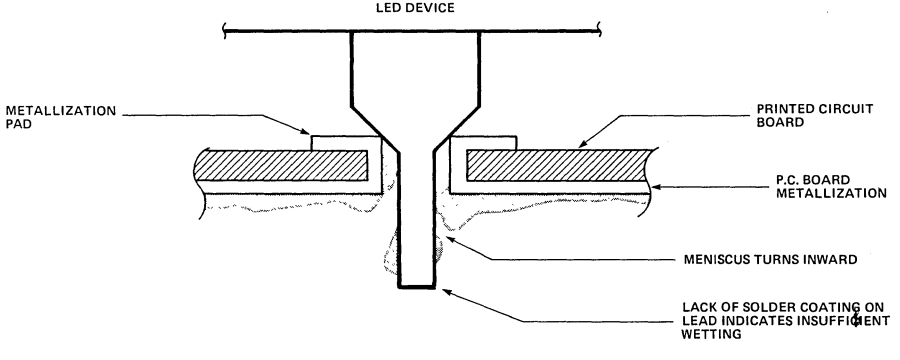

Figure 2. Undesirable Soldered Lead

LIST OF MANUFACTURERS

Alpha Metals, Inc.
56 G Water Street
Jersey City, New Jersey 07304
(302) 434-6778

London Chemical Co. (Lonco®)
240 G Foster
Bensenville, Illinois 60106
(312) 287-9477

E.I. DuPonte De Nemours & Co.
Freon Products Division
Wilminton, Delaware 19898
(302) 774-8341

Frank Curran Co. (Petroleum Napthalene Mothballs)
8101 South Lemont Road
Downers Grove, Illinois 60515
(312) 969-2200

Kester Solder Co.
4201 G Wrightwood Avenue
Chicago, Illinois 60639
(312) 235-1600

Allied Chemical Corporation
Speciality Chemicals Division
P.O. Box 1087R
Morristown, New Jersey 07960
(201) 455-5083

Baron-Blakeslee (Blaco-Tron)®
1620 S. Laramie Avenue
Chicago, Illinois 60650
(312) 656-7300

Imperial Chemical Industries, Ltd. (Arklone)®
Imperial Chemical House, Millbank
London SW1P3JF, England

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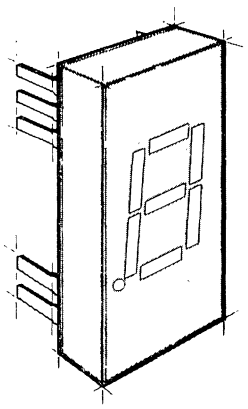
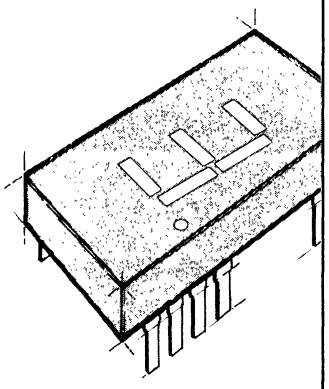
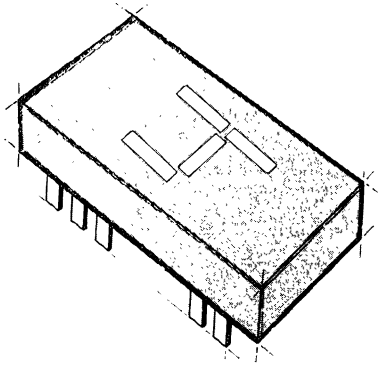
Coombs, Clyde F. *Printed Circuits Handbook. New York: McGraw-Hill, 1964.*

Flaskerud, Paul and Rick Mann. "Silver Plated Lead Frames for Large Molded Packages," IEEE Catalog No. 74CH0839-1PHY (1974), pp. 211-222.







5082-7700 Series Seven Segment LED Display Applications

5082-7700 Series Seven Segment LED Display Applications

INTRODUCTION

The HP 5082-7700 series of LED displays are available in both common anode and common cathode configurations.. The large 0.3" high character size generates a bright, continuously uniform seven segment display of both numeric and selected alphabetic information.

Designed for viewing distances of up to 10 feet, these single digit displays have been engineered to provide a high contrast ratio and a wide viewing angle.

The 7700 series utilizes a standard 0.3" dual-in-line package configuration that allows for easy mounting on PC boards or in standard IC sockets. Requiring a forward voltage of only 1.7 volts, the displays are inherently IC compatible, allowing for easy integration into electronic systems.

The 5082-7730 and the 5082-7731 are common anode displays employing a left hand or a right hand decimal point respectively. Typical applications would be found in electronic instrumentation, computer systems, and business machines. The 5082-7740 is the common cathode version featuring a right hand decimal point for applications that include electronic calculators and business terminals such as credit card verifiers.

This Application Note begins with DC drive techniques and circuits. Next is an explanation of the strobe drive technique and the resultant increase in device efficiency. This is followed by general strobing circuits and some typical applications such as clocks, calculators and counters.

Finally, information is presented on general operating conditions, including intensity uniformity, light output control as a function of ambient, contrast enhancement and device mounting.

DC DRIVE

In DC or non-strobed drive the display is operated with each character continuously illuminated, usually with one decoder per character. This technique is commonly used for short character strings where the cost of the decoders for DC drive is less than that for the timing and drive circuits for strobed operation. The LEDs are more efficient when strobed; however, in DC operation the drivers need not handle high current levels. The DC drive circuit for the common anode display is shown in Figure 1a. The current level, set here at 20mA per segment, is determined by the relation

$$R = \frac{V_{CC} - V_{LED} - V_{CE}}{I_{SEGMENT}}$$

where V_{CC} = voltage supply potential,
V_{LED} = forward voltage of LED at $I_{SEGMENT}$
V_{CE} = "ON" voltage of segment switch.

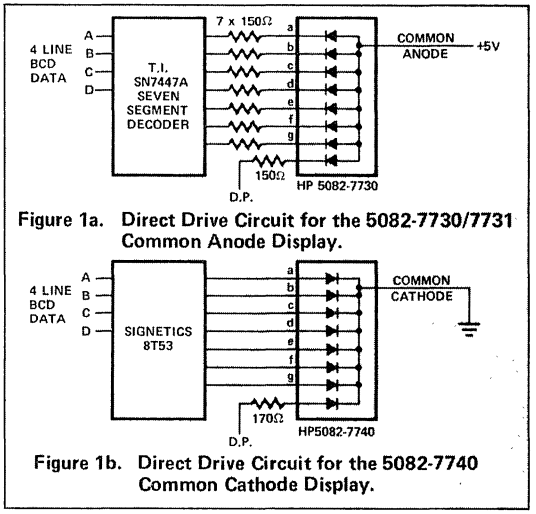


Figure 1a. Direct Drive Circuit for the 5082-7730/7731 Common Anode Display.

Figure 1b. Direct Drive Circuit for the 5082-7740 Common Cathode Display.

An analogous circuit is shown in Figure 1b for a common cathode DC drive system utilizing a current sourcing decoder/driver instead of a standard decoder/driver and external resistors.

See Table I for a list and comparative ratings of some of the commercially available seven segment decoder/driver circuits.

STROBING DRIVE CIRCUITS

In strobing, the decoder is timeshared among the digits in the display, which are illuminated one at a time. The digits are electrically connected with like segments wired in parallel. This forms an 8 (7 segments and decimal point) x N (number of digits) array. In operation, the appropriate segment enable lines are activated for the particular character to be displayed. At the same time a digit enable line is selected so that the character appears at the proper digit location. The strobe then progresses to the next digit position, activating the proper segments and digit enable line for that position.

Since the eye is a relatively slow sensor, a viewer will perceive as continuous a repetitive visual phenomena which occurs at a rate in excess of about 60 events per second. Therefore, if the refresh rate for each digit is maintained at 100 times or more per second, the perceived display will appear flicker-free and easy to read. In displays subject to vibration, a minimum strobe rate of 5 times the vibration frequency should be maintained.

In addition to reducing the number of decoders and drivers, strobing requires less power than DC drive to achieve the same display intensity. This is due to a basic property of GaAsP where luminous efficiency (light output/unit current) increases with the peak current level (see Figure 2a). Thus, for the same average current, use of lower duty cycles (and higher peak current levels) results in increased light output (see Figure 2b). For example, from

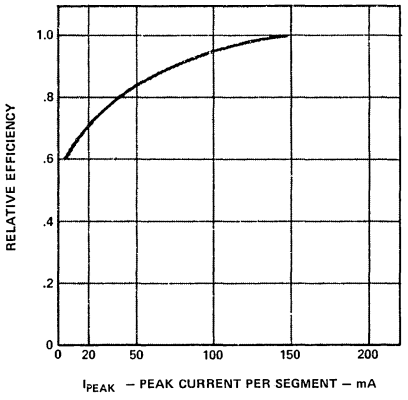


Figure 2a. Relative Efficiency (Luminous Intensity per Unit Current) versus Peak Current per Segment.

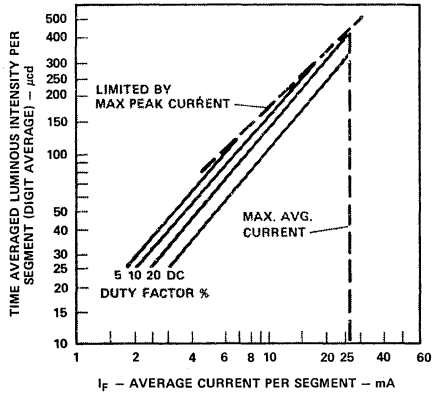


Figure 2b. Typical Time Averaged Luminous Intensity per Segment versus Average Current.

Figure 2b, a typical device operated at 10mA DC would produce a luminous intensity of approximately 120 microcandelas. The same device operated at 50mA peak, 20% duty cycle (as if in a 5 digit strobed display) will produce approximately 145 mcd time averaged luminous intensity.

For common decoder/driver circuits, a series resistor is placed in each segment enable line to limit the light emitting diode current. They are placed in the segment enable lines to prevent uneven current distribution among segments, commonly referred to as "current hogging". The resistive current limiting approach for LEDs outlined above is compact and easy to implement. However, the resistor consumes power.

Various techniques for driving LED displays from energy storage devices (such as inductors or capacitors) are quite practical though generally somewhat higher in cost and bulkier. However, power savings of as much as 50% over the resistive drive techniques are attainable. SCR switches may be attractive in circuits utilizing energy storage devices.

Figures 3 and 4 illustrate two possible memory buffer and display drive techniques used in strobed applications. Both memory techniques assume a bit-parallel/character-serial data entry format. If the system memory is available to supply data to the decoder, the buffer portion of these circuits may be deleted.

Figure 3 depicts a 5-digit strobed display employing a recirculating shift register memory. One shift register is used for each bit of the 4-bit BCD code. Four lines of data from the shift registers drive an SN7447A seven-segment decoder. The value of the current limiting resistors is calculated to provide 40mA per segment peak drive current. The resistor value may be calculated using the following formula:

$$R = \frac{V_{CC} - V_{LED} - V_{CE1} - V_{CE2}}{N\, I_{AVE}}$$

where V_{CC} = voltage supply potential, V_{LED} = forward voltage of LED at peak $I_{SEGMENT}$ ($N\, I_{AVE}$), V_{CE1} = "ON" voltage of segment switch at peak $I_{SEGMENT}$, V_{CE2} = "ON" voltage of digit switch at 8 times peak $I_{SEGMENT}$, I_{AVE} = desired average operating current per segment, and N = number of digits in the display.

Data for each digit of the display is sequentially shifted to the QE output of the shift register by the display scan clock. The scan clock also drives an SN7496 shift register set up as a ripple scanner. The scan shift register outputs are buffered to source the 320mA peak digit current. Data entry to the storage registers is controlled by the system clock of the data source. During data entry, the display is blanked and the scan shift register is reset to the

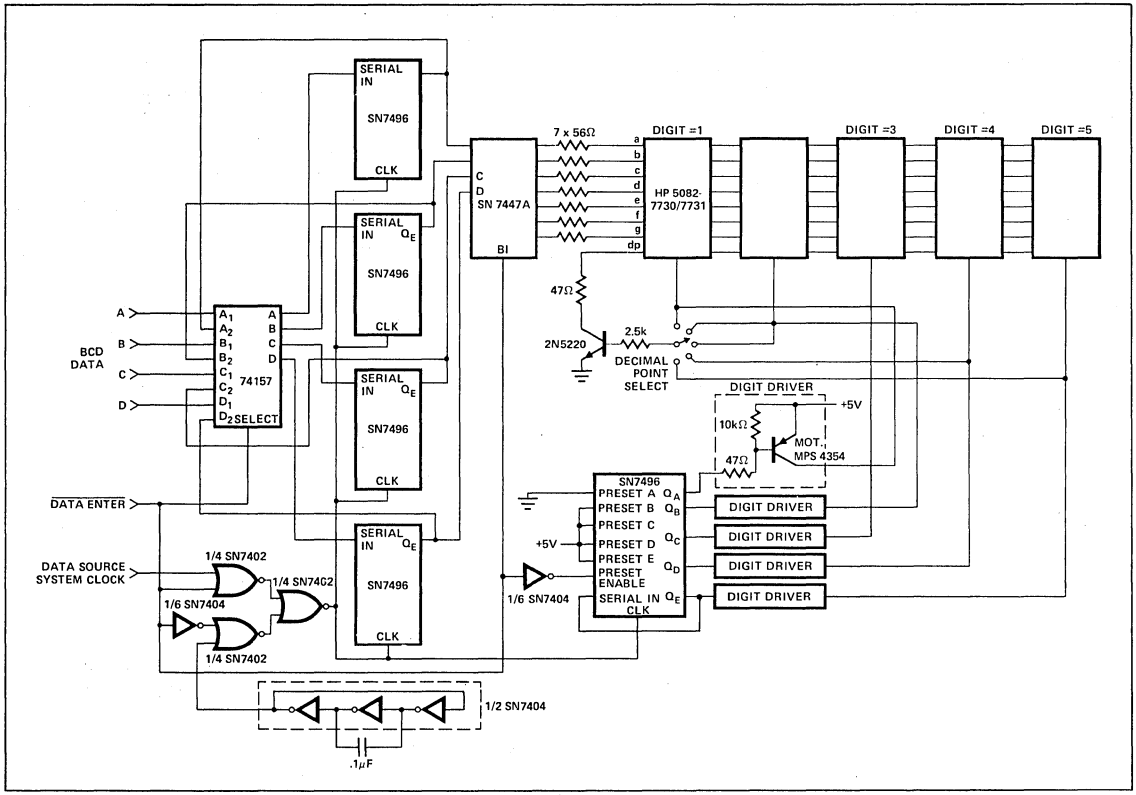


Figure 3. Five Digit Strobed Display with Recirculating Shift Register Memory.

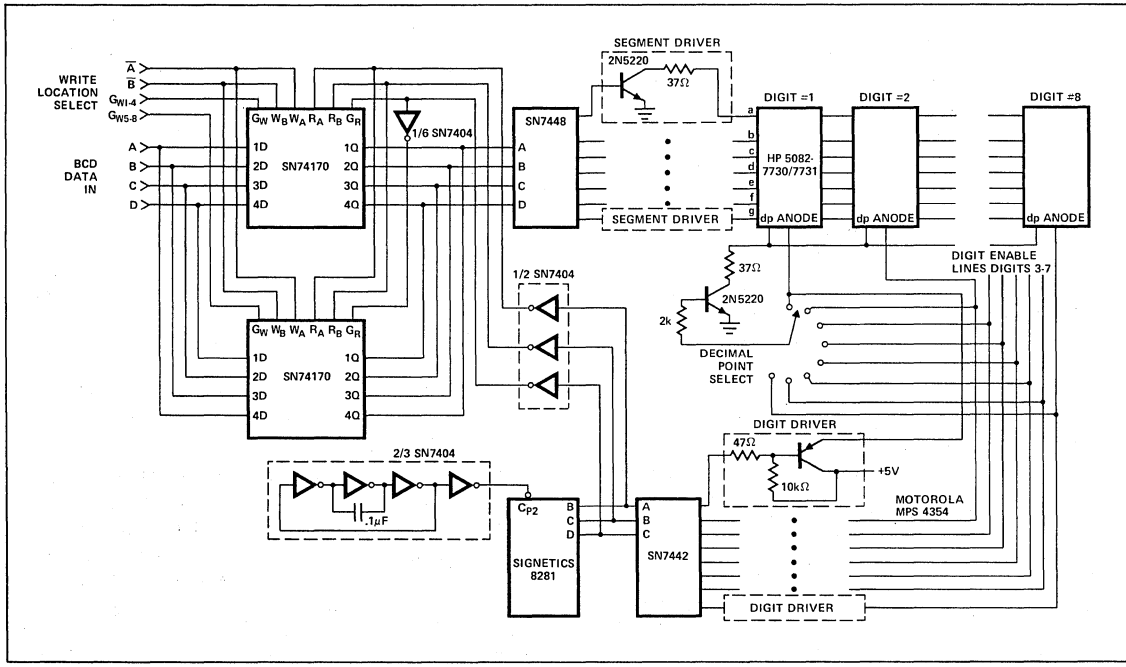


Figure 4. Strobed Eight Digit Common Anode Display with Static Memory Buffer.

first digit position by a logic "0" at $\overline{\text{DATA ENTER}}$. The DATA SOURCE SYSTEM CLOCK and the external BCD lines are also enabled by $\overline{\text{DATA ENTER}}$. The 5 digits of new data will be entered into the shift registers on each positive transition of the system clock. After data entry, $\overline{\text{DATA ENTER}}$ is returned to a high state, and scanning begins at position "A" under control of the SCAN CLOCK.

Figure 4 depicts an eight digit strobed display employing a static 4 x 8 bit memory. Data from the memory buffer is selected by the read lines under the control of the scan counter. This data is decoded by an SN7448 to drive the display segment lines. In this case the 80mA per segment peak current is beyond the current sinking capability of any common decoder/driver so an output buffer transistor must be used. Current limiting resistor values are calculated as before. The digit scan counter uses a Signetics 8281 binary counter in the divide by 8 mode. Data entry to the memory buffer can occur simultaneously with data read and any one of the eight digits may be selected or written independently.

The display length illustrated in either of the above schemes may be changed by simply providing the additional memory requirements and extending the capacity of the digit scanner. Displays of up to 16 digits are practical.

Numerous manufacturers are now supplying transistor arrays and buffer drivers which offer the advantages of lower costs and improved packing densities over discrete segment and digit drivers. See Table II for a list of some of the presently available products. See Table III for other useful display circuits.

CALCULATORS

The display circuit for a 10-digit calculator is given in Figure 5. A MOSTEK MK5010P single chip calculator circuit provides the calculating, decoding, and timing for a four function (+, −, x, ÷), 10-digit calculator. The displays are strobed at 100mA peak on a 1 of 10 duty cycle. The Darlington segment drivers source 100mA while the digit drivers sink 800mA peak. The MOS output transistor connecting the output to V_{SS} is "OFF" when the segment (or digit) is to be activated. In this state, the pull-down resistor connected to V_{GG} sinks the current necessary to turn on the PNP drive stage. When the MOS transistor is "ON", the 1mA output current through the pull-down resistor biases the PNP drive stage "OFF".

There are a variety of calculator chips for 8, 10, and 12-digit applications with varying voltage supply requirements and features. These include circuits from companies such as AMI, Cal-Tex, MOSTEK, NORTEC, Rockwell Int'l., and TI. Output stages vary although the P-channel, open-drain approach used in the MK5010P example is the most common.

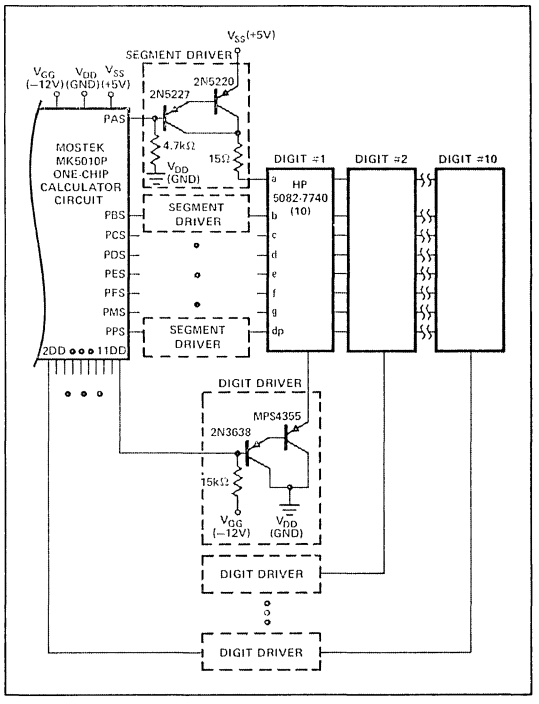


Figure 5. Typical Single Chip Calculator Circuit.

CLOCKS

Figures 6 and 7 depict the complete circuitry for 6-character digital clocks using monolithic clock chips from two different manufacturers. Both clocks use the 60Hz AC line as a time base and derive power from unregulated bridge rectifier power supplies.

Figure 6 illustrates a 6-digit clock circuit using the National Semiconductor NM5314 clock chip. This chip uses a strobed technique with all scanning logic and memory buffers on board. Scan frequency is established by an external RC network and should be maintained between 60Hz and 10kHz. The values shown should generate approximately a 1kHz scan rate. Each of the P-channel MOS outputs is buffered to provide adequate drive current to the individual segment and digit enable lines.

Figure 7 illustrates a 6 digit clock radio circuit using the MOSTEK MK5010PAN clock chip and HP 5082-7740 common cathode displays. Since the MK5010P series chips provide a 12.85% duty cycle digit enable, the component values shown will supply approximately 10mA average or 77mA peak current to each segment of the strobed display. The base inputs of the MPSA-13 segment drivers and the MPSU 45 digit drivers each have series current limiting resistors and pull-down resistors to limit maximum drain current and assure cut-off in the "OFF" state. In this circuit, the digit drive lines are multiplexed to accept input data for alarm set, time set, and other functions.

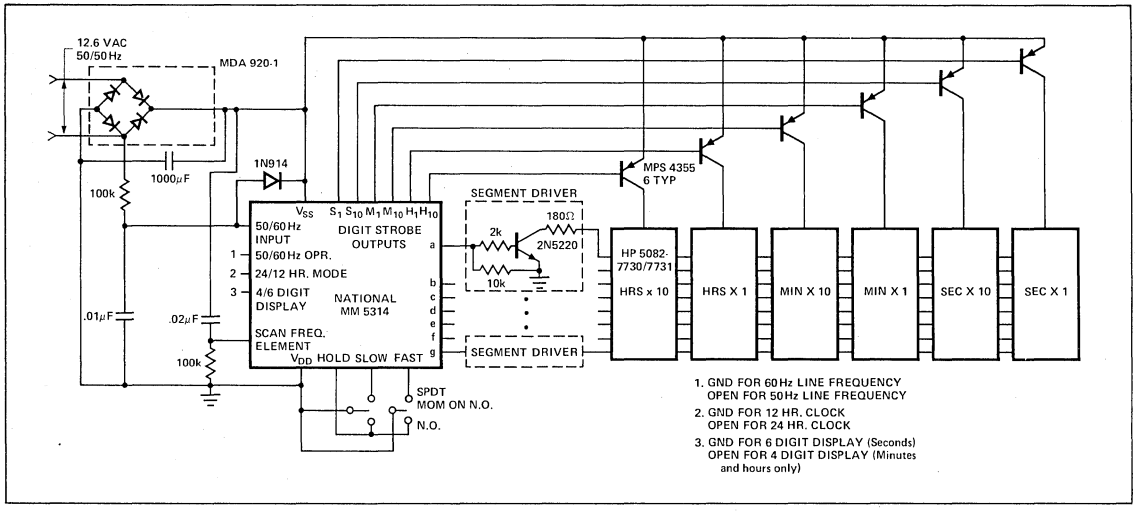


Figure 6. Strobed Drive for a Six Digit Clock.

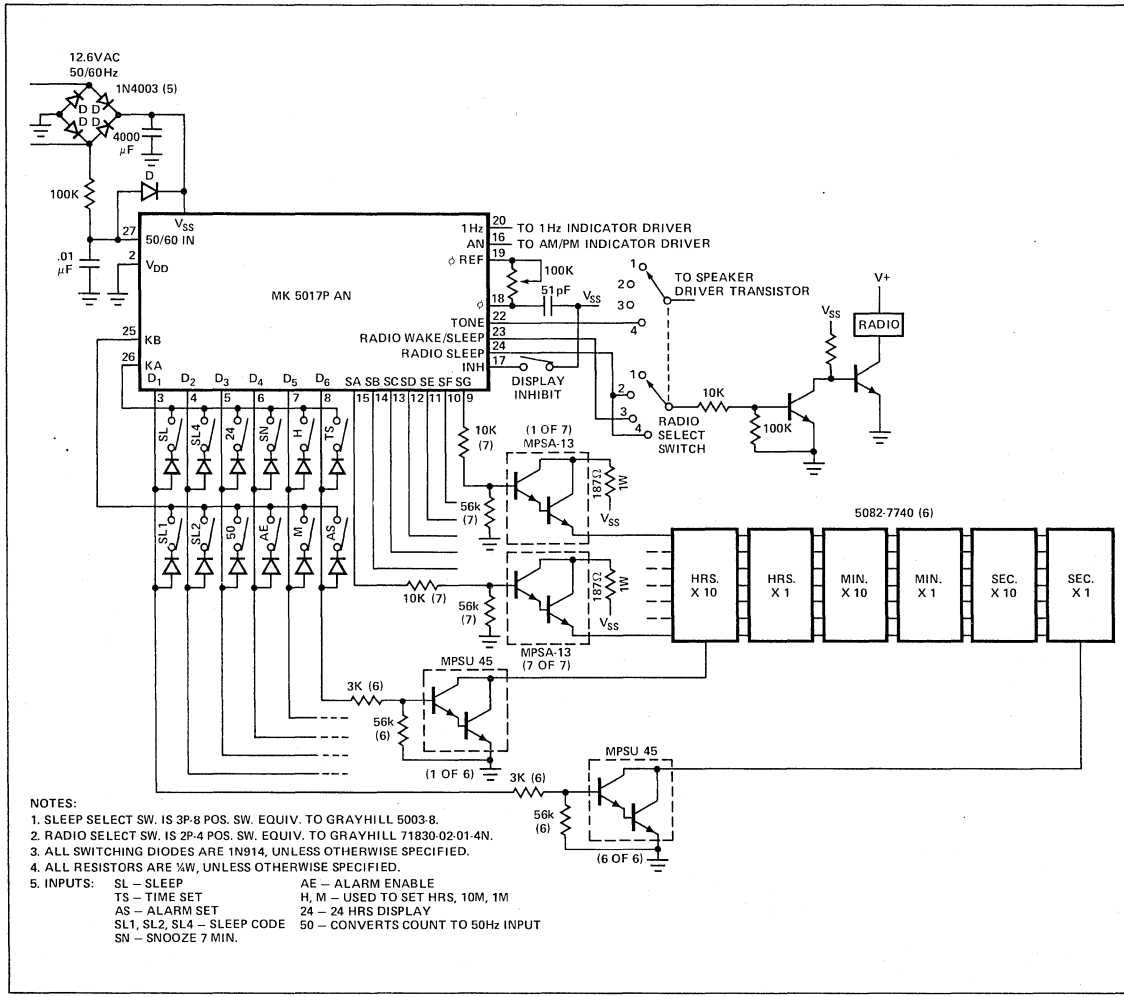


Figure 7. Six Digit Clock Radio.

COUNTERS

The strobe display circuit for a 4½ digit counter is shown in Figure 8 utilizing the 7730 common anode display (left hand decimal point) and the MOSTEK MK5007P four decade counter. Available in a 16-pin package, this circuit is a less expensive version of the familiar MK5002P, and includes latches, decoding and multiplexing functions. In addition to counting, this circuit can be used with its internal clock for DVM, timer and other measuring applications. In this example, the MK5007P's BCD outputs are converted to a seven segment format by the SN7447A decoder/driver which can sink 40mA per segment. A flip-flop is used to implement an overflow digit "1", providing a 4½ digit display. The average light level of the display is controlled by two factors. First, R controls the peak current per segment, set here for 40mA. The second factor is the duty cycle of the counter's SCAN INPUT signal. The internal multiplexing circuit for scanning the digits is triggered on the falling edge of the scan clock. While this signal is low, the segment and digit outputs are blanked.

Therefore, a duty cycle greater than 80% of the SCAN INPUT signal is desirable for efficient operation. In this circuit, use has been made of the MK5007P's internal scan clock; a timing capacitor at the SCAN INPUT sets the frequency. The MOSTEK units can be cascaded for greater than 4 decades of readout. Similar circuits in function are General Instrument's AY-5-4007 series, which have the additional feature of a 25mA sourcing capability at each segment output line.

A DC drive circuit for a 5 digit counter is outlined in Figure 9. This combines the -7730 common anode display (left hand decimal point) with the TI SN74143, a 4-bit counter/latch/decoder having 15mA constant current outputs. For applications requiring counting up to 12MHz, the use of this circuit greatly reduces the component count (even the current limiting resistors are eliminated). The LATCH STROBE INPUT allows the display to operate in a data sampling mode while the counter continues to function. The BLANKING INPUT allows total suppression or intensity modulation of the display. The stored BCD data is available for driving other logic via the LATCH OUTPUTS (Q_A, Q_B, Q_C, Q_D). For higher current drives, the SN74144 with its open-collector outputs can sink 25mA per segment.

INTENSITY UNIFORMITY

The 5082-7700 series devices are categorized for light output intensity to minimize the variation between digits or segments within a digit. Luminous intensity categories are designated by a letter located on the right hand side of the package. Display appearance will be optimized when a group of display digits uses devices from a single category.

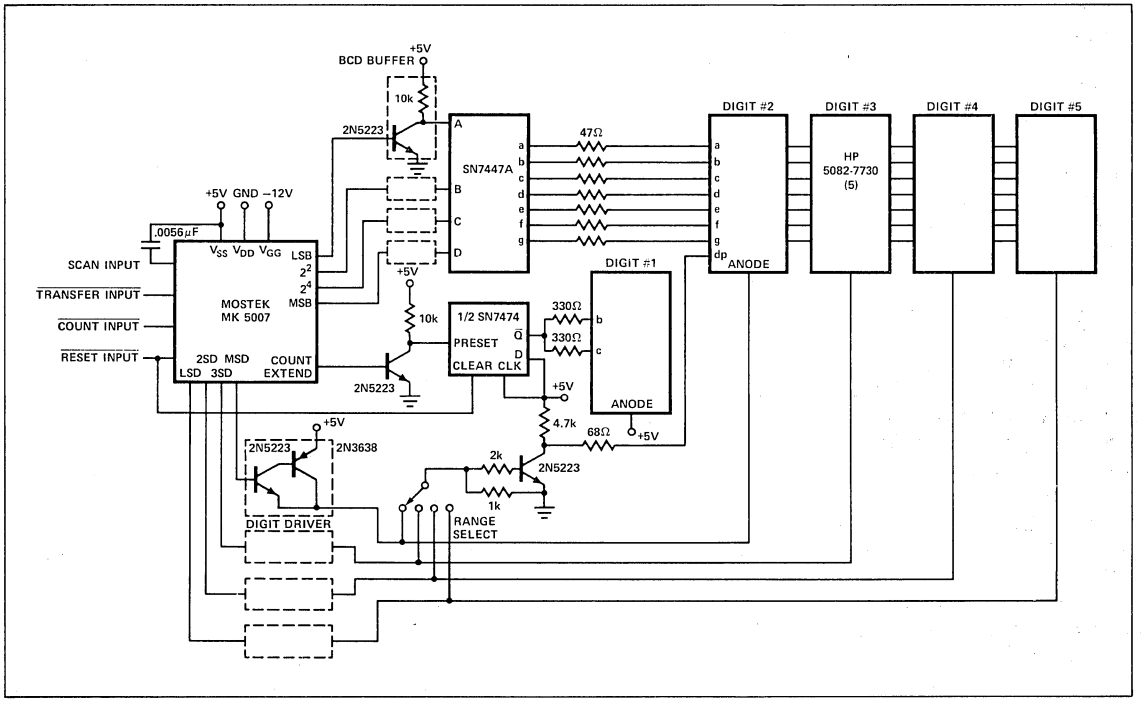
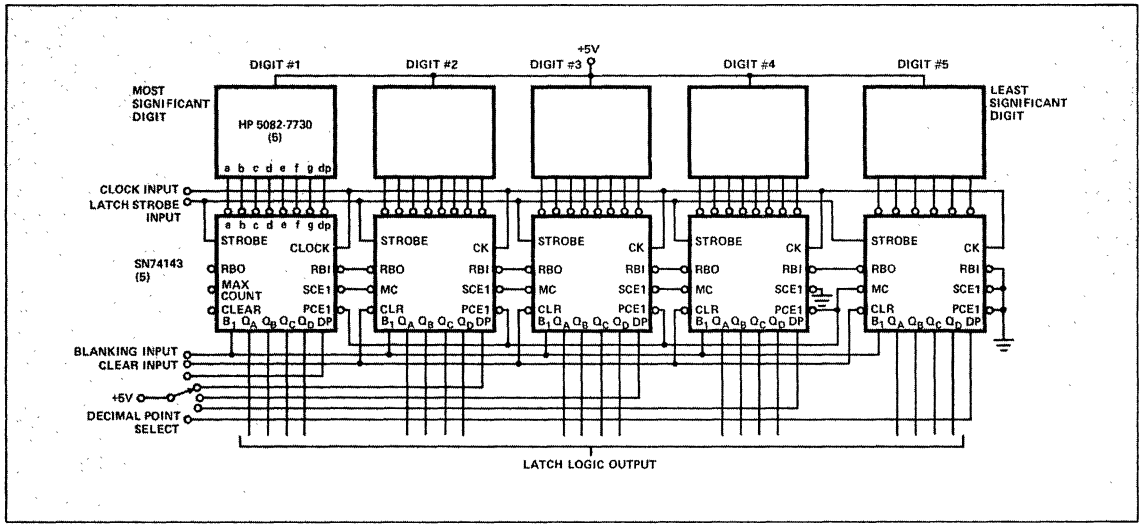


Figure 8. Four and One-half Digit Strobed Counter



INTENSITY MODULATION

It is often desirable to vary the intensity of a display to provide improved readability under varying ambient lighting conditions. Intensity control can be achieved using either amplitude or pulse width modulation techniques. The latter is recommended for broad dynamic range of intensity control. Pulse width modulation offers the advantage of good tracking between segments as the intensity is decreased, and also allows the LEDs to operate with a high peak current where they are more efficient. Figures 10 and 11 illustrate two possible techniques of control.

In Figure 10 a monostable multivibrator is triggered by the scan clock. Photo-resistor R_1 tracks with ambient light intensity and causes the monostable multivibrator to produce an output pulse width proportional to ambient lighting. This method will provide duty cycles ranging from approximately 20% to 100%.

Figure 11 depicts another intensity modulation technique. The scan clock input square wave is integrated by R_1 and C_1 to form a triangular wave. Ambient light is monitored by a phototransistor and an amplified output voltage proportional to ambient lighting is produced by A_1. These two signals are presented to the comparator A_2. The output of A_2 will be true only as long as the triangle wave voltage is greater than the ambient light signal. The LM311 amplifier used in this circuit can be replaced with any medium to high gain amplifier which will give adequate swing with a single 5 volt supply. This technique offers a 0 to 100% dynamic range of modulation.

In both of the above examples, the pulse width modulated signal is connected to the blanking input

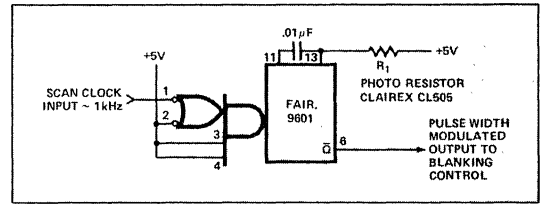


Figure 10. Multivibrator Modulation Circuit.

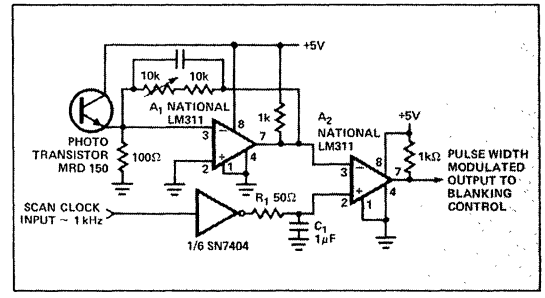


Figure 11. Wide Dynamic Range Intensity Control Circuit.

of the display driver. The display duty cycle is then controlled by the modulated signal which is proportional to the ambient intensity. If the scan frequency is substantially greater or less than 1 kHz in either of the above circuits, timing and integrating component values will have to be changed to produce satisfactory results.

CONTRAST ENHANCEMENT

The quality of the perceived display is a function not only of light intensity but also of contrast to the background. To improve display contrast, the

entire front surface of the display, except for the light emitting areas, is finished in a uniform flat black. The plastic encapsulant in the light emitting areas contains a red dye to further reduce the reflected ambient light. The display's background and the type of contrast enhancing filter used affect the display quality. Typically, PC board mounting and an inexpensive red filter (e.g., Plexiglass 2423 or materials having similar transmission characteristics) are used. Under strobe drive conditions of 10 mA/segment average, the display is easily readable to distances of ten feet and will retain good contrast under relatively high ambient lighting conditions.

There are several additional contrast enhancing measures that can be implemented to allow lower display intensity and power levels. With respect to PC board design, keep as many metallized lines as possible out of the normal viewing area. These surfaces reduce contrast by reflecting ambient light. Whenever possible, the lines running to the displays should be placed out of sight on the board's back side. You can also hide metal traces by placing them beneath the display package. To minimize the light reflected from the PC board, the area surrounding the display can be darkened either through use of a screened black epoxy ink (e.g., WORNOW W-O-N black ink) or a black piece of material cut as a collar to fit around the display. Circular polarizing filters (such as Polaroid HRCP-red) or 3M Display Film are particularly effective in enhancing contrast in high ambient light although they may be more expensive. Antiglare coatings are available from firms such as Panelgraphic Corp. to reduce front filter reflections. An antiglare surface finish may also be incorporated into the molds used to manufacture the filters.

MOUNTING CONSIDERATIONS

The 5082-7700 series devices are constructed utilizing a lead frame in a standard DIP package. In addition to easy PC board mounting, the standard pin spacing of 0.100" between pins and 0.300" between pin rows allows use of the familiar 14-pin IC sockets. See Table IV for a list of some of the available display sockets. The displays may be end-stacked as close as 0.400" center-to-center. The lead frame has an integral seating plane which holds the package approximately 0.035" above the PC board during standard soldering and flux removal operations. The devices can be soldered for up to 5 seconds at a maximum solder temperature of 230°C (1/16" below the seating plane). To optimize device performance, materials are used that are limited to certain solvents for flux removal. It is recommended that only Freon TE, Freon TE-35, Freon TF, Isopropanol, or soap and water be used for cleaning operations.

Note: See following pages for Tables I, II, III and IV.

Table I. Decoder/Driver Circuits for Seven Segment Displays

Manufacturer's Product No.	Manufacturer	Common Anode or Common Cathode	Rated Maximum Output Current [mA]	Other Features	Other Manufacturers
7447	Texas Instr.	CA	40		National Semi, Fairchild, Motorola, Signetics
7448	Texas Instr.	CC	4*		National Semi, Fairchild, Motorola, Signetics
9307	Fairchild	CC	5.6*		
9317 B/C	Fairchild	CA	40/20		
9357	Fairchild	CA	40		
9368	Fairchild	CC	19***	Quad Latch	
9369	Fairchild	CC	50		
9370	Fairchild	CA	25	Quad Latch	
9660	Fairchild	CC	5-50**	Pgmbl Current and Decimal Pt. Drive	
MC 14511	Motorola	CC	25	CMOS	
MC 4039	Motorola	CA	20		
N8T51 B N8T59 B	Signetics	CA, CC		MOS Compatible Inputs	
N8T74 B N8T75 B	Signetics	CA, CC		Quad latch MOS Compatible Inputs	
8140	Harris	CA	40	Quad latch	
1001/1002	SCS Microsystems		120*	Quad latch, some versions available w/resistors on board	

*with external pull-up resistance **constant current supply ***current limit resistors on board

Table II. Driver Arrays for LED Displays

Manufacturer and Product No.	Maximum Output Current	Drivers Per Package	Typical Application
ITT Semiconductor			
502	200mA Sink	6	Digit Drive
503	34mA Source	4	Segment Drive
National Semiconductor			
DM8861	50mA Source or Sink	5	Segment Drive
DM8863	500mA Sink	8	Digit Drive
Sprague Electronics			
ULN 2031A	80mA Sink	7	Segment Drive
ULN 2032A	80mA Source	7	Segment Drive
Series 400	250mA Sink	4	Digit Drive
Texas Instruments			
SN75491*	50mA Source or Sink	4	Segment Drive
SN75492*	250mA Sink	6	Digit Drive

Table III. Circuits for Seven Segment Displays

Manufacturer and Product No.	Description	Comments
Texas Instruments		
SN74143	BCD Counter/4 Bit Latch/BCD-7 Segment Decoder/15mA Constant Current Driver	Ideal for Counting Applications (Time or frequency measurements, A-D Converters).
SN74145	BCD to Decimal Decoder (1 of 10 Decoder)/ Driver	Capable of sinking 80mA per line making it ideal for a digit scanner.
SN74144	Same as SN74143 except output driver can sink up to 25mA per line	Need current limiting resistor for each segment.
SN74142	BCD Counter/4 Bit Latch/BCD to Decimal Decoder (1 of 10 Decoder) Driver	Useful for digit scanner. Need only a clock signal since counter is in circuit.
National 8551 TI SN74173 Signetics 8T10	Tri-State Quad Latches (Also known as "Bus Buffers")	Allows bussing of data lines eliminating numerous gates.
Mostek		
MK5002, 5007, 5005	4 Decade Counter/BCD-7 Segment Decoder/ 4 Digit Scanner in 1 package, 3 options	Provides all counting and timing signals for a 4 Decade Strobed Counter Display (can be end stacked for 8 decades, ...)
GI		
AY-5-4007 Series	4 Decade Counter/BCD-7 Segment Decoder/ 4 Digit Scanner/LED Driver	Similar in function to Mostek 5002 series but adds 25mA LED drivers for strobed display.

Table IV. 14 Pin DIP Sockets for 7700 Series Displays

Manufacturer and Product No.	Termination	Description
Amphenol-Barnes		
821-20011-144	Solder	Nylon, Low Profile
821-20013-144	Wire Wrap	Nylon, Low Profile
821-25011-144	Solder	Full Sized Body
821-25012-144	Wire Wrap	Full Sized Body
Augut		
314-AG50-2R	Solder	Full Sized, Phenolic
Cinch		
14-W-DIP	Wire Wrap	Low Profile, Nylon
14-DIP	Socket	Phenolic
Cambion		
3777-01-0312	Solder	Nylon
3897-01-0316	Wire Wrap	DAP Plastic

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APPLICATION NOTE 946

5082-7430 Series Monolithic Seven Segment Displays

INTRODUCTION

The HP 5082-7430 series solid state displays are common cathode, 2 and 3 digit clusters capable of displaying numeric and selected alphabetic data. These GaAsP displays employ an integral magnification technique to increase both the character size and the luminous intensity of each monolithic digit. The resultant 0.11" (2,79mm) high character is viewable at distances of up to 5 feet when operated at as little as 0.5mW per segment.

These displays are designed for strobed operation. In strobing, the decoder is timeshared among the digits in the display, which are illuminated one at a time. The digits in each cluster are electrically connected with like segments wired in parallel. This forms an 8 (7 segments and decimal point) x N (number of digits) array. Several clusters may be wired with the segment lines in parallel to form longer display strings. In operation, the appropriate segment enable lines are activated for the particular character to be displayed. At the same time a digit enable line is selected so that the character appears at the proper digit location. The strobe then progresses to the next digit position, activating the proper segments and digit enable line for that position.

Since the eye is a relatively slow sensor, the average viewer will perceive as continuous a repetitive visual phenomena which occurs at a rate in excess of about 60 events per second. Therefore, if the refresh rate for each digit is maintained at 100 times or more per second, the perceived display will appear flicker-free and easy to read. In displays subject to vibration, a minimum strobe rate of 5 times the vibration frequency should be maintained.

In addition to reducing the number of decoders and drivers, strobing requires less power than DC drive to achieve the same display intensity. This is due to a basic property of GaAsP where luminous efficiency (light output/unit current) increases with the peak current level (see Figure 1). Thus, for the same average current, use of lower duty cycles (and higher peak current levels) results in increased light output (see Figure 2). For example, in Figure 2, a typical segment operated at 1mA DC would produce a luminous intensity of approximately 40 microcandelas. This same segment operated at 10mA peak, 10% duty cycle will produce approximately 95μcd time averaged luminous intensity. This is similar to a 10 digit strobed display operated at 1mA average current. At current levels below 2mA peak, device to device efficiency variations may produce inter-digit matching problems. Operation at very low peak current levels is, therefore, not recommended.

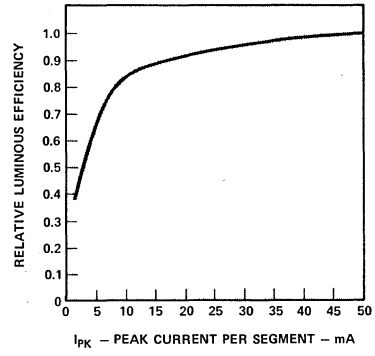

Figure 1. Relative luminous Efficiency vs. Peak Current per Segment.

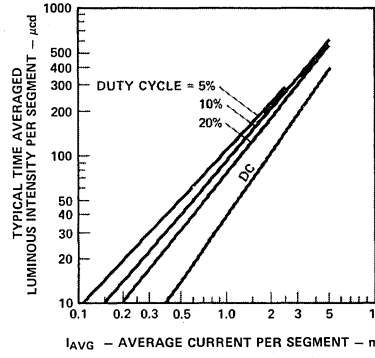

Figure 2. Typical Time Averaged Luminous Intensity per Segment (Digit Average) vs. Average Current per Segment.

TYPICAL APPLICATIONS

The 5082-7430 series devices are ideal for use in circuits where low power drain and high luminous intensity are important. Figure 3 depicts a battery operated electronic stopwatch circuit employing the Intersil ICM 7045 timer circuit, and four 5082-7432 displays. This circuit chip contains all of the logic necessary to implement the 8 digit timer with the addition of only the displays, an external frequency element, and control switches. When driven from a 3.6V NiCd battery, the 15mA peak (1.9mA average) segment current will provide adequate intensity for viewing even in bright outdoor lighting conditions. The push to read switch for the display will allow standard batteries to deliver many hours of satisfactory operation.

Figure 4 shows a battery-operated 4 digit event counter. This circuit utilizes the General Instrument AY-5-4007A 4 digit display driver/counter. On board electronics provide a 4 decade up/down counter, storage registers, multiplexing circuits, an internal oscillator for digit selection and a seven segment decoder/driver. This circuit utilizes a single 9 volt battery to supply V_{CC} (V_{SS}) with respect to V_{GG}. V_{GI} (ground) reference is supplied through a 270k resistor to V_{GG}. The digit drivers are buffered using a 2N4123 NPN transistor as a digit switch. Series resistors in the segment enable lines limit the segment current to 6mA peak, 1.2mA average. This current level will provide a satisfactory display for outdoor viewing. For indoor viewing, a 3mA peak current level using 4kΩ series resistors will be satisfactory. A switch in the emitter common of the digit enable transistors allows the display to be disabled in order to extend battery life.

Standard MOS calculator chips that source as little as 3mA peak will directly drive the 7430 series displays.

Figure 5 depicts a circuit using a minimum number of components for a 9 digit electronic four function calculator. Using the CAL TEX CT 5030 MOS chip, the segment lines may be driven directly at up to 10mA peak, 1 of 13 duty cycle. The segment current may be limited to as little as 250μA average through the use of a single resistor in the digit common line. The digit outputs are buffered using two 75492 Darlington drivers. As no V_{GG} supply is required and all clock signals are internally generated, a single 6 volt battery may be used to supply power for the entire circuit.

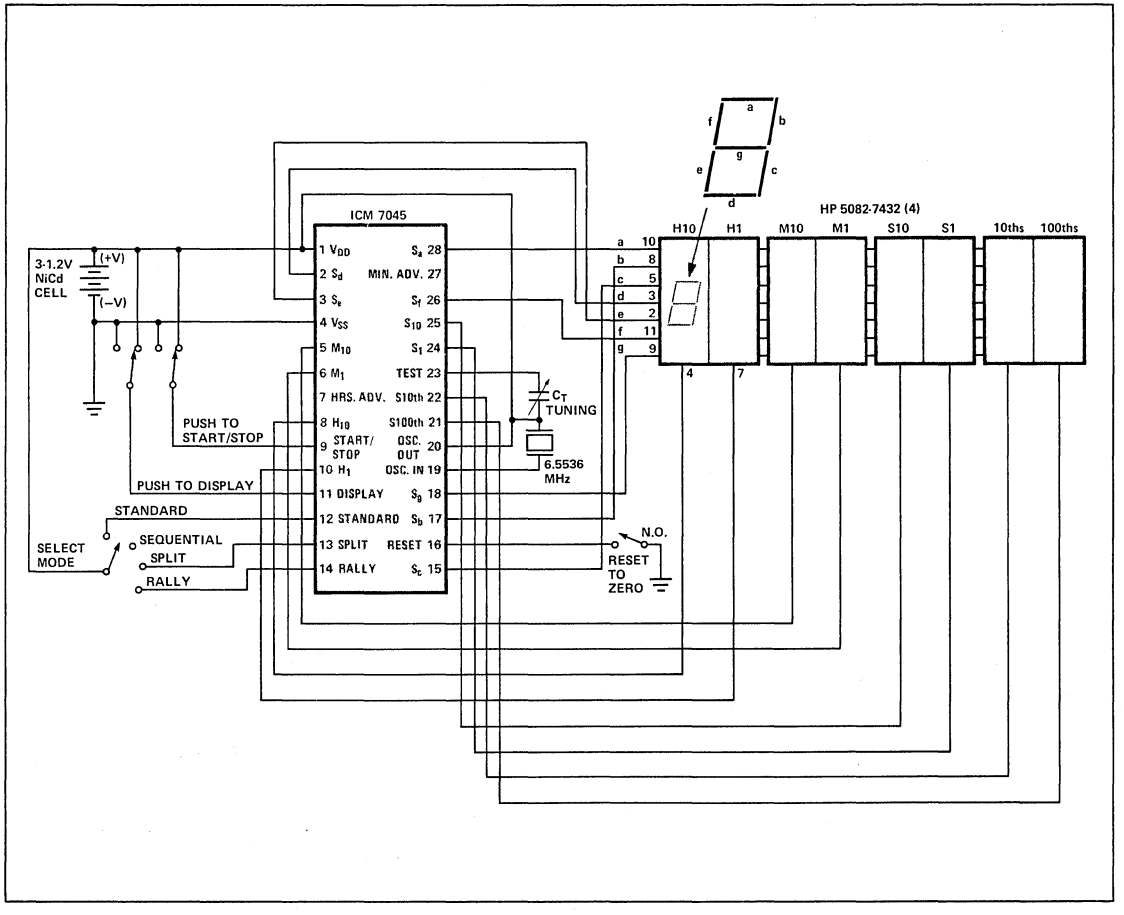

Figure 3. Electronic Stopwatch.

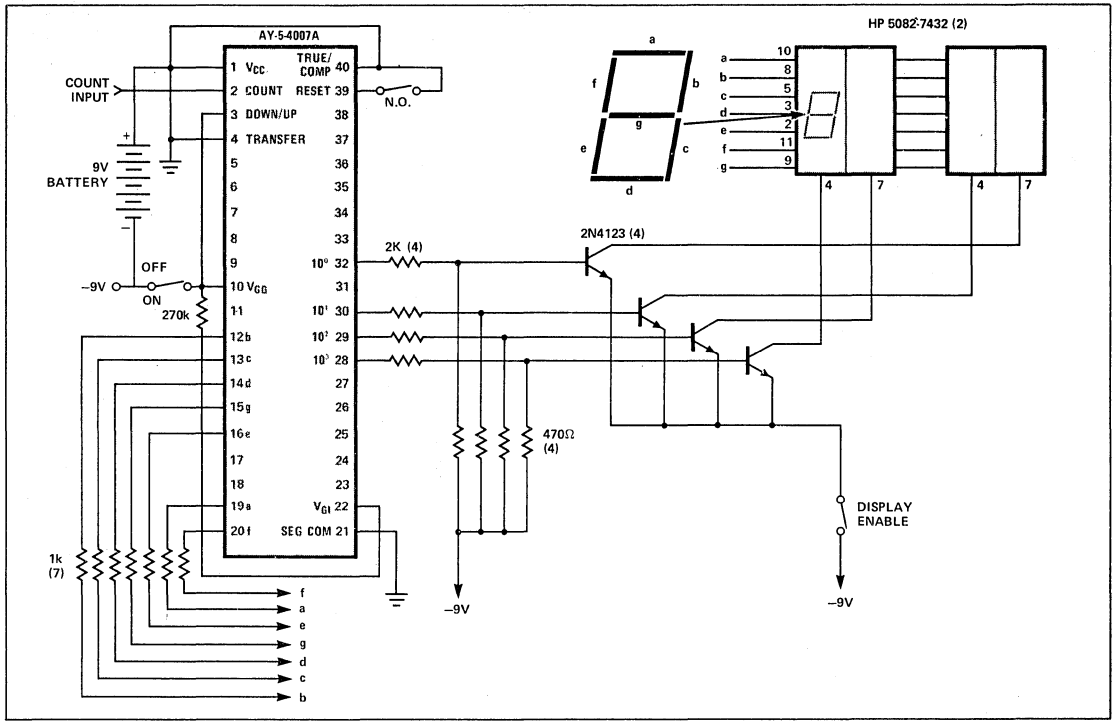

Figure 4. Battery Operated Event Counter.

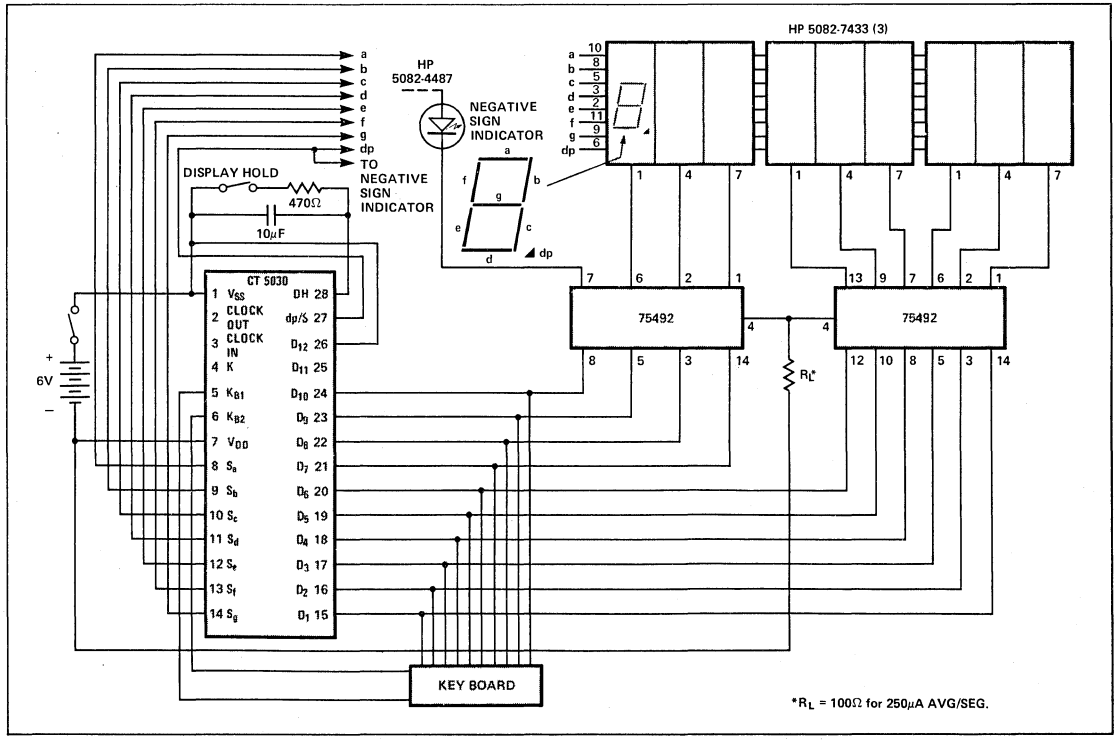

Figure 5. Four Function Calculator.

CONTRAST ENHANCEMENT

The quality of the perceived display is a function not only of the display intensity but also of ambient light intensity and contrast to the display background. When expected usage will be in relatively low ambient intensity areas (home or office) the display may be mounted near the surface of the instrument case and covered with an inexpensive red filter such as Plexiglass 2423 or a material having similar transmission characteristics. To improve contrast in bright ambient situations, the display may be recessed into the instrument case so as to provide a relatively dark background and thereby high display to background contrast. Contrast may be further enhanced through the use of polarizing filters such as Polaroid HRCP-red or louver type filters such as 3M display film. The latter material, though it may reduce viewing angle somewhat, will significantly reduce extraneous ambient light in the region of the display.

With proper mounting and anti-glare coatings (such as available from Panelgraphic Corp.) to reduce front panel reflections, satisfactory viewing may be achieved in bright ambient conditions.

MECHANICAL

The 5082-7430 series package utilizes a standard DIP lead frame with pin spacing of 0.100" between pins and 0.300" between rows.

The devices may be soldered for up to 5 seconds at a maximum solder temperature of 230°C (1/16" below the seating plane). In order to achieve the best possible display appearance, it is important that the individual display clusters be held in close alignment during soldering operations. Figure 6 shows a mounting fixture and loading block which will function both as an alignment aid and an insertion tool. This fixture will also act as a heat sink allowing a wider selection of soldering time and temperature parameters. Further alignment from cluster to cluster may be achieved with a mechanical alignment after soldering. The plastic encapsulant used in these devices may be damaged by some solvents commonly used for flux removal. It is recommended that only Freon TE, Freon TE-35, Freon TF, Isopropanol, or soap and water be used for cleaning operation.

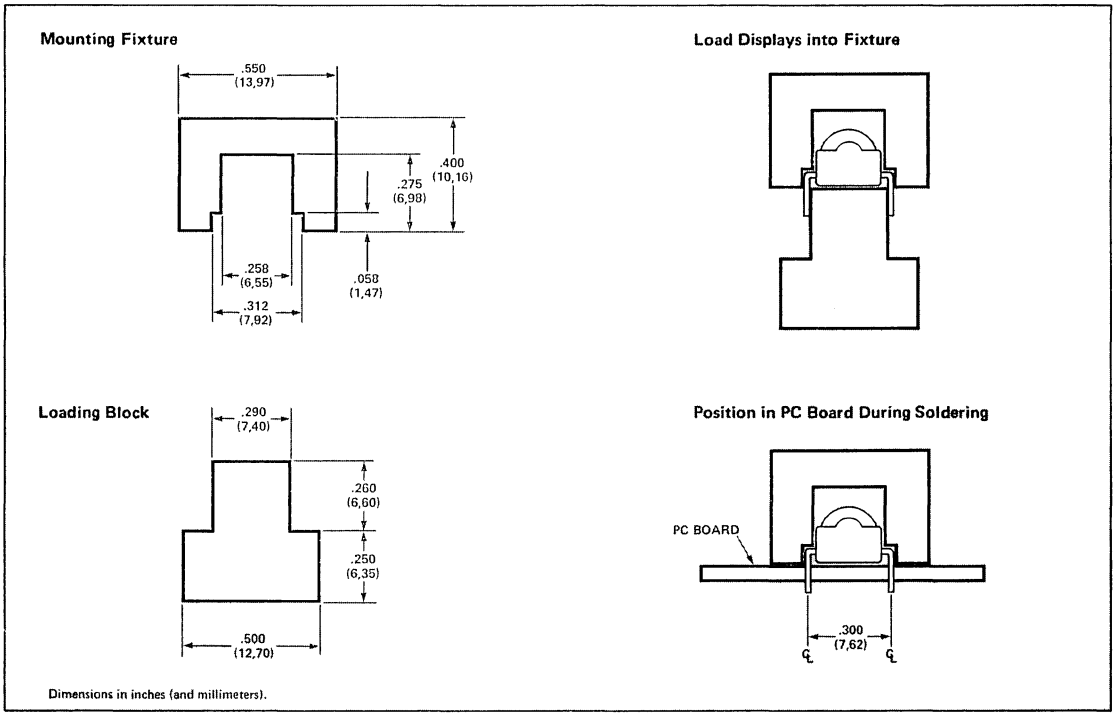

Figure 6. Mounting Fixture.

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APPLICATION NOTE 948

Performance of the 6N135, 6N136 and 6N137 Optocouplers in Short To Moderate Length Digital Data Transmission Systems

This application note assists system designers by describing the performance to be expected from the use of HP 6N135-6N137 optocouplers as a line receiver in a TTL-TTL compatible NRZ[1] data transmission link. It describes several useful total systems including line driver, cable, terminations and TTL compatible connections. The systems described utilize inexpensive cable and operate satisfactorily over the range of transmission distances from 1 ft. to 300 ft. Over this range of distances, the data rate varies from 0.6 megabits per second to 19 megabits per second largely limited by coupler performance at short distances, and cable losses at longer distances.

[1] Non-return to zero

INTRODUCTION

Optocouplers can function as excellent alternatives to integrated circuit line receivers in digital data transmission applications. Their major advantages consist of superior common-mode noise rejection and true ground isolation between the two subsystems. For example, a conventional line receiver is limited to a ±20V common-mode noise rejection at best from DC over its operating frequency range, while an optocoupler can achieve rejections of ±2.5kV at 60Hz.

A conventional optocoupler that utilizes a photo-transistor is limited in its minimum total switching time. At the higher data rates, above 200-500 kbits/s, these delay times can become very significant. The HP 6N135 and 6N136 utilize an integrated photo-diode and transistor to produce lower total switching time. The HP 6N137 adds an integrated amplifier within its package to decrease these delay times still further. All three units can produce data rates well in excess of 500 kbits/s, while the 6N137 can couple an isolated 9.5MHz (19M bits/s) clock from its input to its output. These data rates are achieved with common-mode noise voltage rejection in excess of that provided by most types of line receivers at all frequencies.

The information contained in this application note covers the performance of optocoupler line receiver circuits; however, it does not describe design details. These details are covered in Application Note 947 "Digital Data Transmission Using Optically Coupled Isolators".

This application note describes the basic design elements of a data transmission link and presents several examples of total systems that will be useful to systems designers at distances that range from 1 ft. to 300 ft. and have a moderate overall cost. First, a few measures of performance are defined to allow systems to be compared with one another. Second, the elements of an optocoupler data transmission system are discussed. Third, circuit examples and demonstrated performance of a selected set of systems are presented for the various transmission distances. This presentation includes schematics, representative waveforms at intermediate circuit points, and a summary performance table. It compares the results of passive (resistive) terminations with active terminations that improve overall performance at the longer transmission distances. Fourth, the trade-offs that were made to arrive at the selected system components are described. Along with the trade-offs, there is a discussion of approaches to increase performance by selection of other circuit components or by "peaking" a given length system.

DEFINITIONS OF PERFORMANCE

In data transmission systems that utilize optocouplers, there are no standardized definitions that allow performance capability to be specified. The major performance parameters that are of interest are data rate capability, usually specified in bits per second; and immunity to common mode noise at the coupler input, usually specified as AC or DC common mode voltage rejection in volts, or transient voltage noise rejection in volts/microsecond.

To arrive at a definition of maximum data rate capability requires that the total system be specified including all components, and in addition, data modulation and demodulation techniques. In order to compare the various systems presented in the application note, it is necessary to define some useful terms.

One commonly used modulation technique for digital data data transmission is NRZ, or non-return-to-zero transmission. In the most common form of this technique, a twisted pair transmission line is driven by a balanced driver with an alternating plus or minus voltage signal. A number of integrated circuits are available to provide the drive signals and create a straightforward design.

One potential measure of system performance for NRZ, and potentially other modulation techniques as well, is the measurement of the maximum 50% duty cycle clock frequency that the system will pass. Since a clock represents a total 1/0 and 0/1 transition each full cycle, this square wave provides two bits of data for each cycle. As the upper clock frequency limit of a system using couplers is reached, the duty cycle will change from 50%. The MAXIMUM CLOCK DATA RATE is found by observing the system output as a function of a square wave input until the output distorts to a 10% duty cycle and multiplying this frequency by two (two bits/cycle). At this input frequency, the system data rate is very close to its absolute maximum and any potential recovery of a signal at a higher data rate is impractical. A more detailed definition of this term appears in the glossary.

Another parameter indicative of the performance of a system is to measure the system transient response in its worst case condition. The step response of a transmission system using isolators is a function of the duty cycle and repetition rate. For NRZ, if this term is properly defined, it can indicate a worst case maximum data rate that the system will faithfully transmit, regardless of the combination of ones and zeroes in the data bit stream. This step response term will be referred to as the STEP TRANSIENT DATA RATE MAXIMUM. It assumes that the pulse propagation delay down the transmission line is essentially constant, and defines a data rate maximum at which a single bit of data in a stream of all zeroes and a one, or all ones and a zero may be successfully sent through the system. This is simulated by placing a very low frequency square wave input into the line. Then the circuit delay time from a pulse received at the *end* of the line until the system output makes a transition is measured. This delay time is a function of the cable output risetime and the delays experienced in the coupler and its associated circuitry. The specific delay times are called t_{PHL} and t_{PLH}, indicating delay times for a 1/0 and 0/1 transition respectively. The STEP TRANSIENT DATA RATE MAXIMUM is defined as the inverse of t_{PLH} or t_{PHL}, whichever is longer. In general, this data rate will be lower than the MAXIMUM CLOCK DATA RATE. A more exact definition of t_{PHL}, t_{PLH} and STEP TRANSIENT DATA RATE appears in the glossary.

The parameters used to define worst-case common mode noise immunity are measured for the coupler and associated circuitry without the transmission cable. The common mode voltage rejection is a function of frequency and indicates the maximum AC steady state signal voltage common to both inputs and output ground that will not create an error in the output. This rejection reaches a minimum at some frequency. The transient voltage noise immunity is a measure of the maximum rate of rise (or fall) that can be placed across the common input terminals and output ground without producing an error voltage in the output. This term is a function of the input pulse magnitude and rate of rise for an optocoupler and is stated as a dv/dt minimum in volts per microsecond. Further definitions of these terms appear in the glossary. It should be noted that common mode characteristics of such systems are largely determined by the point at which the noise enters the transmission system. Common mode rejection for a total system would be expected to improve with increasing distance between the common mode insertion point and the input to optocoupler.

ELEMENTS OF AN OPTOCOUPLER DATA TRANSMISSION SYSTEM

The basic elements of an optocoupler transmission system are:

- ☐ Line Driver
- ☐ Transmission Cable
- ☐ Line Termination Circuit
- ☐ Optocoupler
- ☐ TTL Interface Circuit

In order that the performance of systems using the 6N135-6N137 optocouplers might be demonstrated, component elements had to be defined for several systems. These elements are chosen to be TTL compatible at the input and the output. They are also chosen to produce high performance, be moderate in cost, and work over a range of distances of one foot to 300 feet. This can then maximize the utility to systems designers of the circuits demonstrated, thus allowing them to be used without change in a variety of specific applications to produce a known level of performance.

CIRCUIT EXAMPLES AND DEMONSTRATED PERFORMANCE

To reduce the number of complete systems upon which performance is demonstrated to a practical number, a basic representative set of elements must be selected or designed. This includes a single line driver and cable type with performance measurements taken at three transmission distances — 1 ft., 100 ft., and 300 ft. It also includes two termination types, active and passive, and three types of couplers with companion TTL interface circuits. This produces six total data transmission systems upon which data rate performance can be observed at the three transmission distances. Figure 1 illustrates the line driver and cable combination selected. Figure 2 illustrates the pulse response of this driver/cable combination. Figures 3 through 8 indicate the line termination, coupler, and TTL interface circuitry for the various terminations. Included are representative waveforms measured on the three passive termination systems at the 300 ft. transmission distance. Table 1 outlines the critical parameters of the cable used and Tables 2, 3, and 4 summarize the performance demonstrated on all of the transmission systems.

The performance tabulated for the 1 ft. transmission length is indicative of that which might be achieved by a system with negligible performance degradation in the cable. The performance at 100 ft. and 300 ft. indicates the decrease in data rate due to cable losses as the transmission distance increases. This decrease is the most critical data rate limitation and is indicative of the change in performance of systems using low cost cable. Clearly evident in the tables is the increase in performance of the active termination at the 300 ft. transmission distance. Note also that the data rate of the system utilizing the 6N137 at short transmission distances is less with the active than with the passive termination. This decrease is due to the additional delay added by the active termination.

These performance tables can be used to select a design suitable for an application required by a system designer. For example, assume it is desired to design a data transmission system of variable lengths up to 100 ft. and data rates of up to 1.6 Mbits/s. The circuit shown in Figure 4 and the line driver and cable shown in Figure 1 could be selected to assure this level of performance.

SELECTION OF DEMONSTRATION CIRCUIT ELEMENTS

The foregoing systems exemplify achievable performance and incorporate a number of design decisions which are discussed in this section.

LINE DRIVER

Line Drivers generate the signal that is sent down the transmission line. They have limits as to voltage swing, output impedance, and switching time. A good compromise is provided by National Semiconductor's DM 8830. Any similar device with a low output impedance such as the Fairchild 9614 would operate satisfactorily. These devices are TTL input compatible, require no external components, are relatively inexpensive and readily available. They provide adequate performance and produce directly a dual rail (inverting and non-inverting) output.

For systems requiring higher data rates, more sophisticated and expensive drivers can be selected or designed. Figure 9 illustrates a circuit that has a higher current output and produces a higher data rate than an integrated driver. It uses several components, but does not require a supply voltage above the standard TTL 5 volts. To obtain still higher data rates, the driver line voltage output must be increased. This in turn requires a supply voltage above 5 volts. The National Semiconductor LH 0002C is an example of an integrated circuit that can be used to produce directly a higher line voltage. Numerous other discrete circuits could be designed.

TRANSMISSION CABLE

Transmission cables are very critical in the overall system. They can decrease the effect of extraneous noise voltages on system performance by providing shielding. They also greatly affect the signal losses as the transmission length increases. By controlling these losses, cables can permit a single set of system elements to function adequately for both long and short transmission distances. The critical performance parameters of a transmission cable include cost, transmission length, line series resistance (DC losses), high frequency losses, type and amount of shielding and characteristic impedance.

The Belden type 8777 is representative of a relatively well-shielded, inexpensive cable with typical transmission loss. The important characteristics of this cable are summarized in Table 1.

If it is desired to attain higher performance, the line cost becomes considerably more expensive and tends to dominate system costs. These higher performance cables utilize a large conductor size to lower DC losses, and provide considerably lower losses at high frequencies. Examples of such a cable would be Belden 9269 (IBM 32392), Belden 9250 or their equivalents.

The pulse response of the DM 8830 and the Belden 8777 illustrates the waveform degradation of signals sent down this driver/transmission line pair, regardless of the line receiver employed. Figure 1 illustrates this circuit combination, and Figure 2 illustrates the pulse waveform degradation at 1 ft., 100 ft., and 300 ft. into a 68Ω equivalent load.

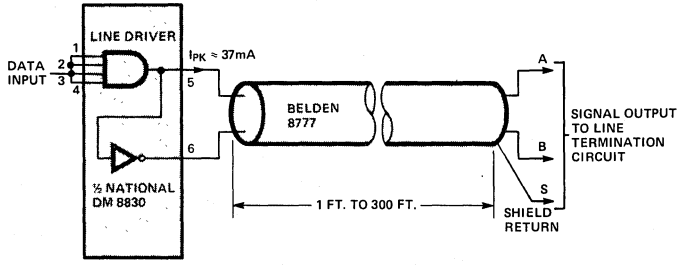


Figure 1. Line Driver and Cable Combination Selected for Use on All Six Systems to Indicate Their Performance.

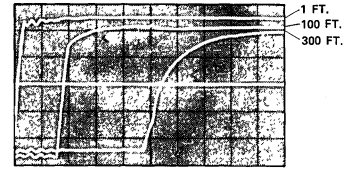


Figure 2. Pulse Characteristics of the Selected Line Driver and Cable. Measurement Observed with a 68Ω Equivalent Termination at One, 100, and 300' Distances. All Waveforms are Line to Line Voltage, Time Referenced to zero feet. Note Time Delay and Waveform Degradation.

LINE TERMINATION CIRCUIT

The line termination circuit converts the voltage arriving at the end of the line to a current impulse to drive the coupler emitter diode. In these system examples, performance of both passive and active circuits was measured.

A passive circuit consists of a set of resistors to match the line to its characteristic impedance and to convert the line voltage to a current. The circuits illustrated here were designed to provide good performance at 300 ft., while not exceeding the coupler input drive current maximum at the 1 ft. line length condition. With this design criterion, these circuits are useful over this *range* of transmission cable lengths. These design characteristics required that two resistive line termination circuits be designed for the three isolators. They are illustrated in Figures 3, 4, and 5.

An improvement in the performance of a resistive termination can be obtained by peaking the line to operate at a specific length as shown in Figure 10. This technique allows the coupler to operate from the peak to peak voltage at the end of the line. To avoid overdriving the coupler, the peaking capacitor value must be minimized. It is chosen by observing the circuit delay time t_{PLH} and selecting the smallest value of capacitor that significantly decreases this delay. With this technique, performance can be expected to improve by as much as 20-30% or more, but the values of peaking capacitor tend to vary with many of the characteristics of components in all of the elements of the system. These include driver output voltage, line length, line losses, coupler delay, etc. This in turn requires each individual system to have a selected value of peaking capacitor.

An active termination utilizes a transistor to act as a line voltage to coupler input current regulator. This technique ignores any attempt to match the line, but instead converts any incoming voltage to a suitable current, once the circuit threshold voltage is exceeded. This tends to decrease circuit sensitivity to line length and other line voltage variations. The delay of an active circuit can limit the maximum system data rate, especially for short transmission distances. But, in general, their use can improve the maximum data rate at the longer distances. In the system examples, two active termination circuits were designed and are illustrated in Figures 6, 7 and 8.

Improving the performance of the active circuit consists of finding transistors and circuit designs to perform the voltage to input current regulation function without limiting overall system performance.

OUTPUT TO TTL INTERFACE

The 6N136 and 6N137 have sufficiently high input to output coupling efficiency (CTR) that the only component required to interface the optocoupler to a TTL input gate is a pull-up resistor. The 6N135 has a somewhat lower CTR and requires an external transistor and resistor to interface with a TTL gate input. The actual circuit configuration and values required for these interface circuits are illustrated in Figures 3 through 8. The circuits illustrate, in general, the optimum interface for a TTL-TTL compatible circuit. Performance could be improved through the use of lower pull-up resistor values in the coupler output collectors and high speed TTL compatible comparators.

Table 1

IMPORTANT LINE CHARACTERISTICS OF BELDEN 8777

- Three sets of two conductor, twisted and individually foil shielded, 22 gauge wire
- Z_0 (Measured Characteristic Impedance) – 68Ω line to line
- Line-to-line capacitance – 30pF/ft.
- Line Resistance – 3.2Ω/100 ft. (per conductor pair)
- Attenuation at 10MHz ≃ 4 dB/100 ft.
- Delay ≃ 1.5 nsec/ft.
- Cost ≈ 5¢/ft./Transmission Pair

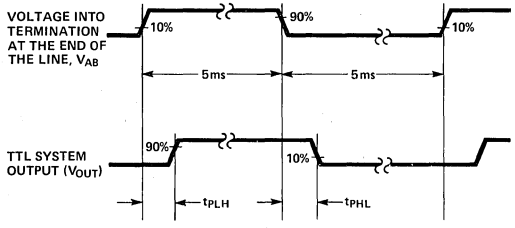
GLOSSARY

1. DATA RATE – This term is typically stated in bits per second and has no standardized definition when used in reference to optocouplers. It is related to the minimum pulse transition time that will be passed by the system and detected. This in turn is related to the distortion or change in duration the pulse experiences upon passing through the system.

2. STEP TRANSIENT DATA RATE MAXIMUM – This term, stated in bits per second, is a function of the maximum delay experienced by a 0/1 or a 1/0 transition in passing through the optocoupler. The step transient data rate maximum is defined as:

$$\text{STEP TRANSIENT DATA RATE (MAX)} = \frac{1}{t_{PHL}} \text{ or } \frac{1}{t_{PLH}}$$

whichever is smaller. Where t_{PLH} and t_{PHL} are measured at the coupler termination input (end of the line) and the TTL output and are defined as follows:

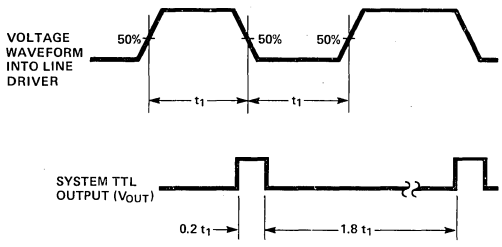


The t_{PHL} and t_{PLH} measured under these conditions approach the maximum delay that will be experienced by data sent through the isolator.

3. MAXIMUM CLOCK DATA RATE – This term defines the maximum data rate at which a 50% duty cycle square wave (clock) will be distorted to a 90%/10% pulse. It is very close to the maximum alternating 1/0 and 0/1 transition that can be passed by the system. It is defined mathematically as:

$$\text{MAXIMUM CLOCK DATA RATE} = \frac{1}{t_1}$$

where t_1 is defined as:



4. COMMON MODE REJECTION VOLTAGE – This term is defined as the maximum sinusoidal voltage at a given frequency that can be applied *simultaneously* to both inputs with respect to output ground and not produce an error signal in the system output. In optocouplers, the value of this voltage is very high at low frequencies and decreases with increasing frequency until it reaches a minimum. The effect is caused by the effective intercircuit capacitance of the emitter and detector chips, and the detector gain and bandwidth. (See Figure 11.)

5. COMMON MODE dv/dt REJECTION MINIMUM – This term is defined as the maximum rate of change of voltage that can be applied to both inputs *simultaneously* with respect to output ground and not produce an error in the system output. Note that this parameter is a function of the duration of the change, or equivalently the pulse amplitude. The stated values in this application note are for a 10V step pulse amplitude generated by a source having a controlled risetime and falltime (e.g., HP 8007B). (See Figure 11.)

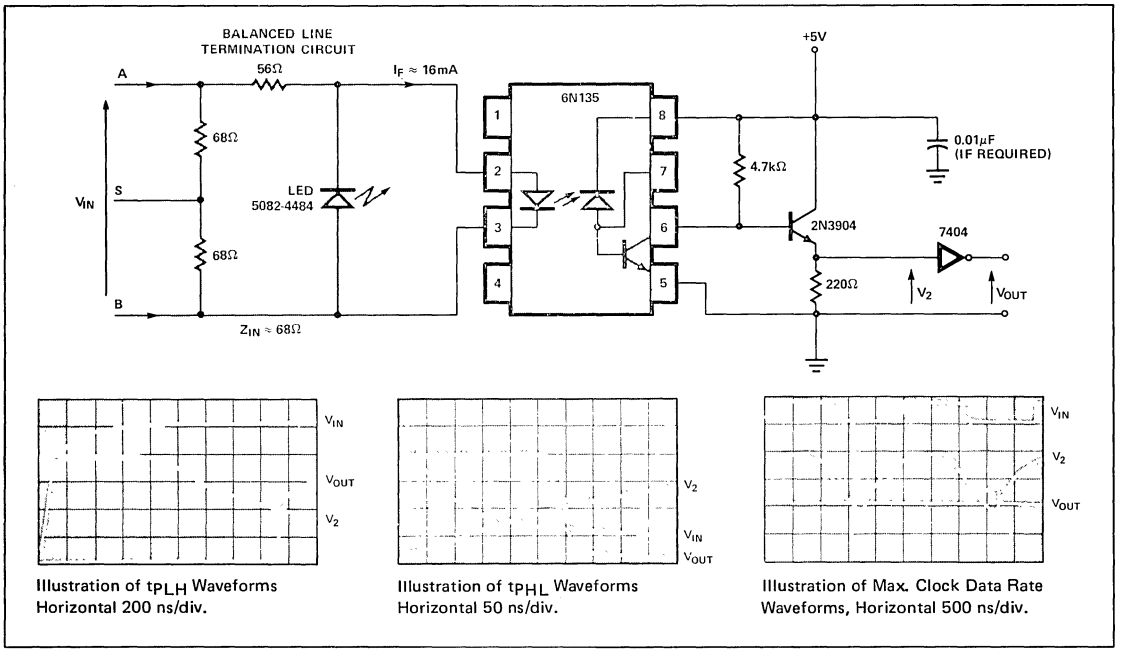


Figure 3. TTL Compatible Passive (Resistive) Termination for the 6N135 and Photographs Indicating Measured Performance at the End of the 300 Ft. Transmission Cable.

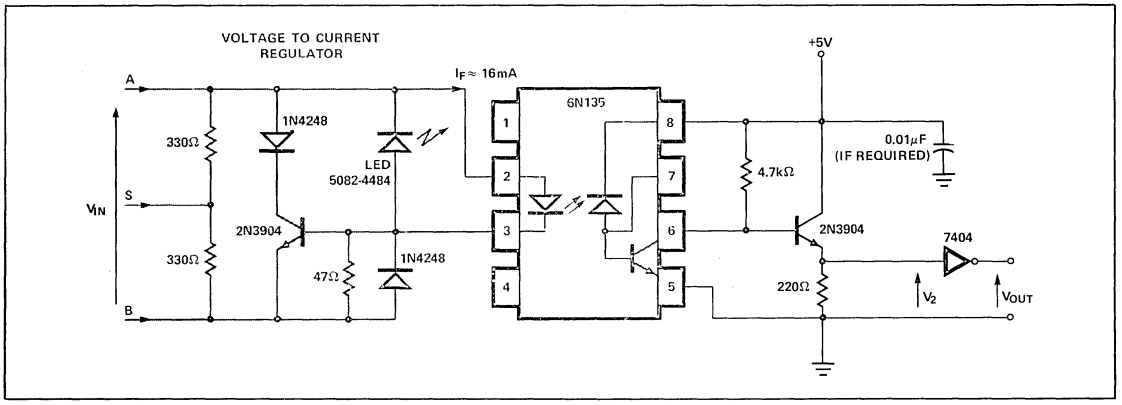


Figure 6. TTL Compatible Active Termination for the 6N135.

Table 2. Summary of Performance of 6N135 Data Transmission Systems at 1, 100, and 300 ft.

Termination	Transmission Distance (ft)	t_{PLH} (ns)	t_{PHL} (ns)	Step Transient Data Rate Max. (Mbits/s)	Clock Data Rate Max. (Mbits/s)	Worst Case Common Mode Noise Rejection	
						Sinusoidal	dV/dt
RESISTIVE (PASSIVE)	1	475	500	2.0	11.2	≤10kHz: 5.0kV pk-pk 1MHz: 84V pk-pk min.	250V/μs min.
	100	900	425	1.1	3.0		
Fig. 3	300	1700	300	0.6	0.8		
ACTIVE	1	500	330	2.0	5.3		
Fig. 6	100	580	270	1.7	4.0		
	300	875	330	1.1	1.6		

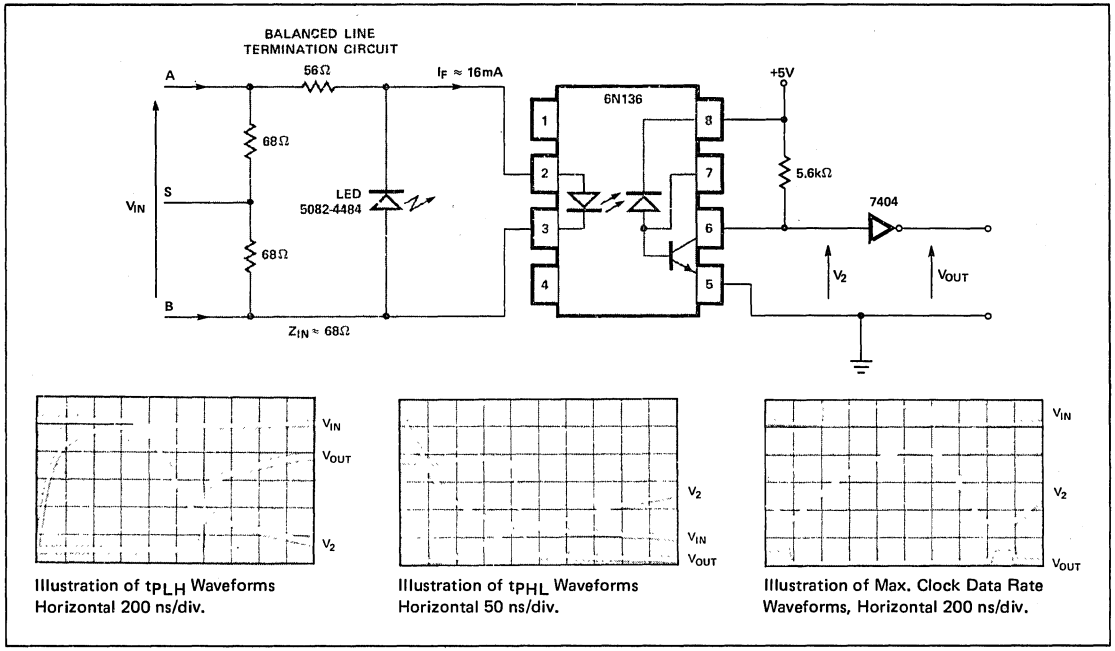


Illustration of t_{PLH} Waveforms
Horizontal 200 ns/div.

Illustration of t_{PHL} Waveforms
Horizontal 50 ns/div.

Illustration of Max. Clock Data Rate
Waveforms, Horizontal 200 ns/div.

Figure 4. TTL Compatible Passive (Resistive) Termination for the 6N136 and Photographs Indicating Measured Performance at the End of the 300 Ft Cable.

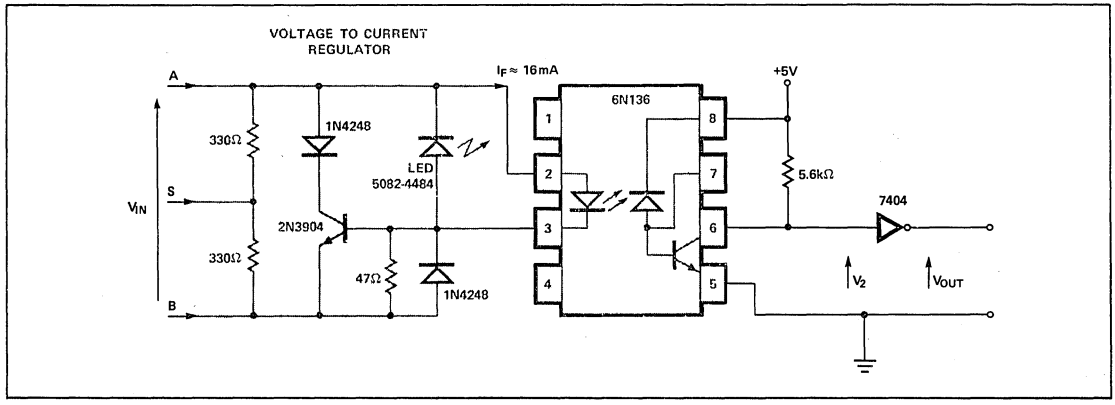


Figure 7. TTL Compatible Active Termination for the 6N136.

Table 3. Summary of Performance of 6N136 Data Transmission Systems at 1, 100, and 300 ft.

	Transmission Distance (ft)	t_{PLH} (ns)	t_{PHL} (ns)	Step Transient Data Rate Max. (Mbits/s)	Clock Data Rate Max. (Mbits/s)	Worst Case Common Mode Noise Rejection	
						Sinusoidal	dV/dt
RESISTIVE (PASSIVE)	1	320	270	2.7	10.0	≤10kHz: 5.0kV pk-pk 1MHz: 84V pk-pk min.	250V/μs min.
	100	640	265	1.6	4.0		
Fig. 4	300	1200	220	0.8	1.2		
ACTIVE	1	375	250	2.7	6.6		
Fig. 7	100	440	250	2.3	5.0		
	300	700	250	1.4	2.4		

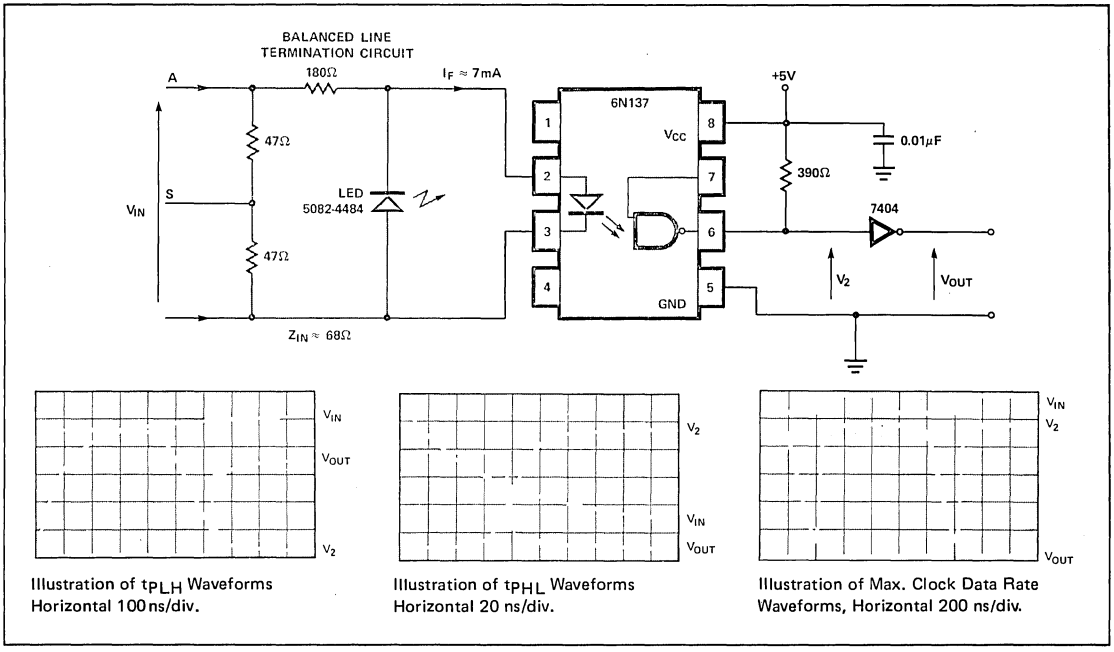


Illustration of t_{PLH} Waveforms
Horizontal 100 ns/div.

Illustration of t_{PHL} Waveforms
Horizontal 20 ns/div.

Illustration of Max. Clock Data Rate
Waveforms, Horizontal 200 ns/div.

Figure 5. TTL Compatible Passive (Resistive) Termination for the 6N137 and Photographs Indicating Measured Performance at the End of the 300 Ft. Transmission Cable.

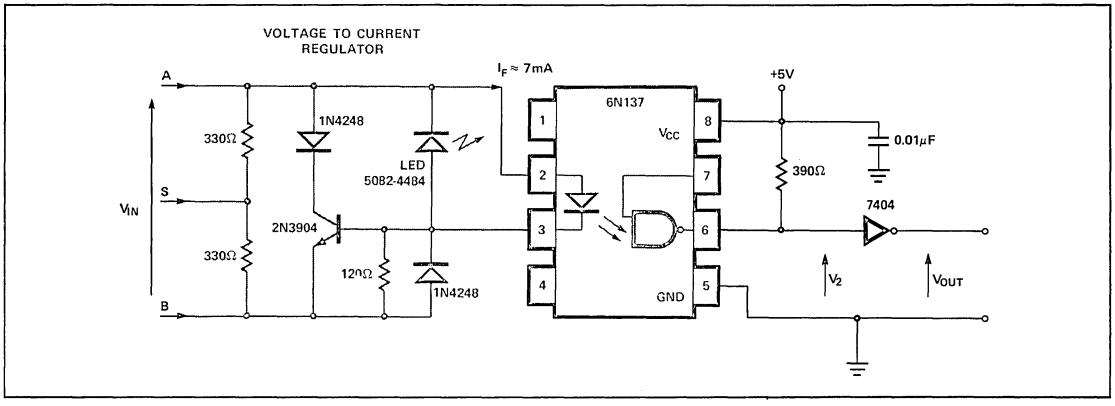


Figure 8. TTL Compatible Active Termination for the 6N137.

Table 4. Summary of Performance of 6N137 Data Transmission Systems at 1, 100, and 300 ft.

	Transmission Distance (ft)	t_{PLH} (ns)	t_{PHL} (ns)	Step Transient Data Rate Max. (Mbits/s)	Clock Data Rate Max. (Mbits/s)	Worst Case Common Mode Noise Rejection	
						Sinusoidal	dV/dt
RESISTIVE (PASSIVE)	1	105	70	9.5	19.0	≤10kHz: 5.0kV pk-pk 8MHz: 22V pk-pk min.	40V/μs min.
	100	170	70	5.8	8.0		
	300	625	70	1.6	2.0		
ACTIVE	1	190	65	5.3	11.0		
	100	190	70	5.3	13.2		
	300	275	80	3.9	8.2		

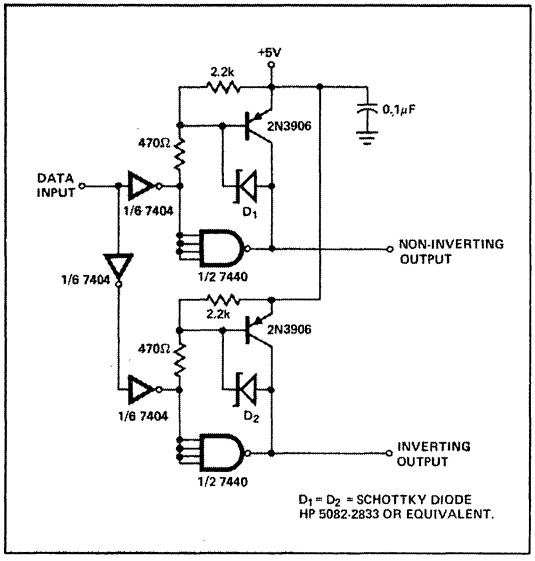


Figure 9. High Output Voltage Swing, High Current, Wide Bandwidth Line Driver that Operates From a 5 Volt Supply and Produces a >8.5V Pk to Pk Pulse into 300 Ft. of Belden 8777 at 10 MHz.

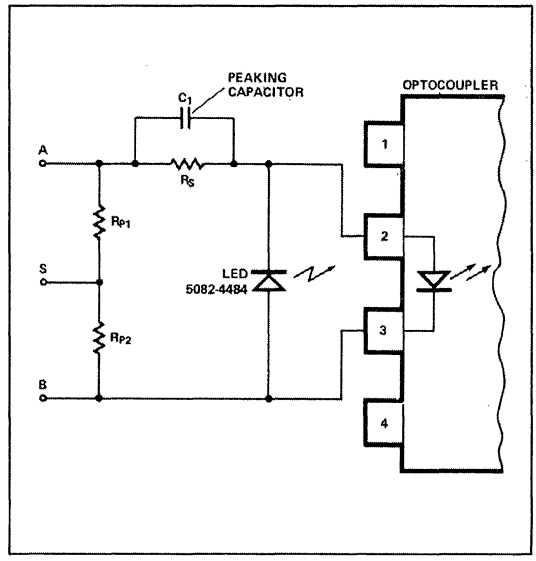


Figure 10. An Example of Circuit Peaking to Improve the Performance of the Passive Termination. C_1 is Chosen for the Minimum Value that Significantly Reduces Input to Output Delay Time. In General, C_1 Must be Selected Individually For Each System.

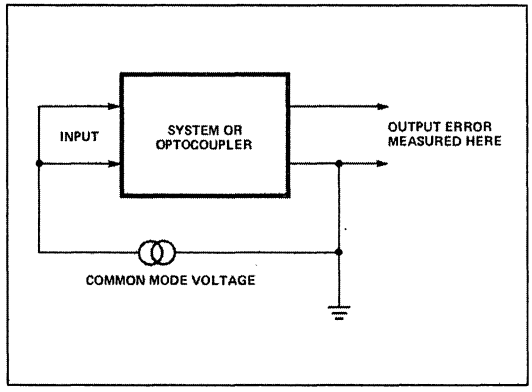


Figure 11. Common Mode Measurement Circuit.

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COMPONENTS

APPLICATION NOTE 951-1

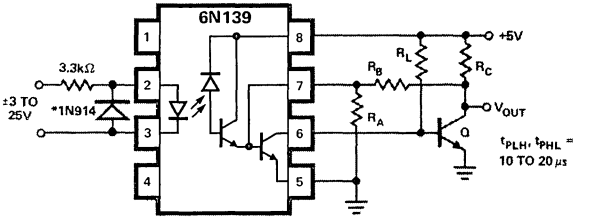
Applications for Low Input Current, High Gain Optocouplers

Optically coupled isolators are useful in applications where large common mode signals are encountered. Examples are: line receivers, logic isolation, power lines, medical equipment and telephone lines. This application note has at least one example in each of these areas for the 6N138/9 series high CTR couplers.

HP's 6N138/9 series couplers contain a high gain, high speed photodetector that provides a minimum current transfer ratio (CTR) of 300% at input currents of 1.6 mA for the 6N138 and 400% at 0.5 mA for the 6N139. The excellent low input current CTR enables these devices to be used in applications where low power consumption is required and those applications that do not provide sufficient input current for other couplers. Separate pin connections for the photodiode and output transistor permit high speed operation and TTL compatible output. A base access terminal allows a gain bandwidth adjustment to be made.

RS-232C COMPATIBLE LINE RECEIVER

- 2500V 60Hz Common Mode Rejection
- Allows use of Low Cost Line
- Full 40kbs Data Rate for Line Lengths up to 5000'
- Hysteresis for Increased Noise Immunity



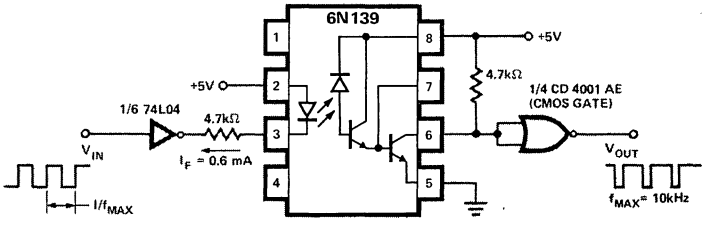
*ANTIPARALLEL DIODE IS NEEDED ONLY IF REVERSE LINE VOLTAGE EXCEEDS 15V (TO PREVENT HIGH REVERSE VOLTAGE FROM CAUSING POWER DISSIPATION IN EXCESS OF INPUT DIODE MAXIMUM RATING).

REMOVE R_A AND R_B FOR NO HYSTERESIS

R_A	R_B	R_C	R_L	Q
680kΩ	1.5MΩ	1.8kΩ	15kΩ	2N3904

LOW POWER INTERFACE

- Operation at $I_F \geq 0.5mA$
- 10kHz f_{MAX}
- Low Power Consumption

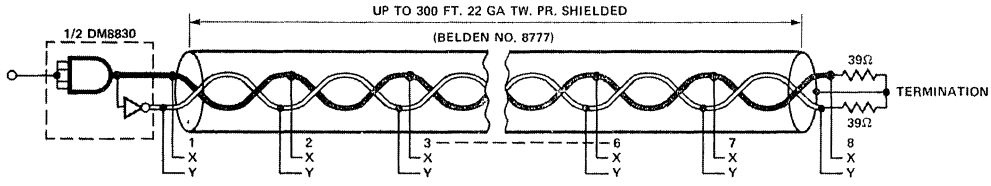


f_{MAX} IS THE FREQUENCY AT WHICH A 50% DUTY FACTOR AT THE INPUT IS DEGENERATED TO 10% OR 90% DUTY FACTOR AT THE OUTPUT.

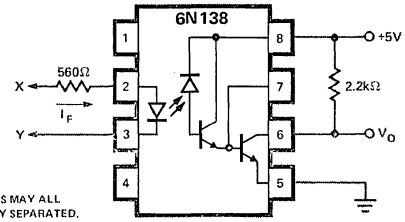
APPLICATION NOTES

LINE RECEIVER FOR PARTY LINE

- 1-8 Receivers can be used with circuit shown
- Uses conventional IC Line Driver
- Total Line Length 1-300'
- Typical Data Rate —180kbs (t_{PHL}, t_{PLH} = 3 μsec)
- Allows use of Low Cost Line



ISOLATOR LOADS MAY BE DISTRIBUTED RANDOMLY ALONG THE LENGTH OF THE LINE, OR ALL MAY BE LUMPED AT THE END. I_F FOR 1 AND 8 ISOLATOR LOADS WOULD BE 2.7 AND 1.8mA RESPECTIVELY.

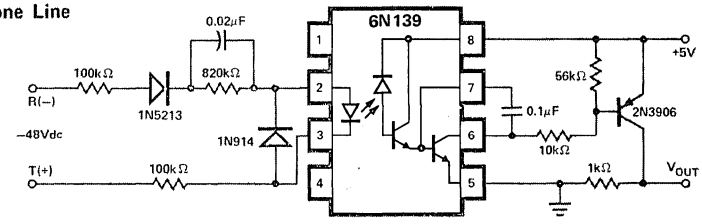


PROPAGATION DELAY: t_{PHL}, t_{PLH} = 0.5 to 5μs

OUTPUT GROUNDS MAY ALL BE ELECTRICALLY SEPARATED.

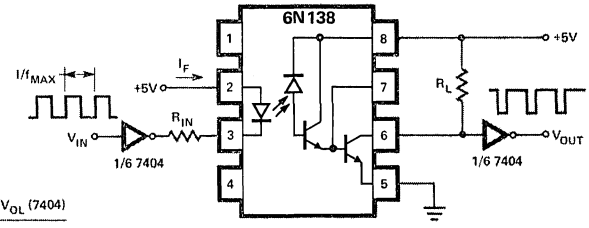
TELEPHONE RING DETECTOR

- Discriminates between Ring and Dial Signals
- Minimal Line Loading (1MΩ dc, 450kΩ at 20Hz)
- 2500V Insulation from Telephone Line
- Small Size
- Integrator Included



TTL TO TTL INTERFACE

- Direct Input and Output Compatibility
- Adjustable Data Rate
- High Fan-Out



$$I_F = \frac{5V - V_F - V_{OL}(7404)}{R_{IN}}$$

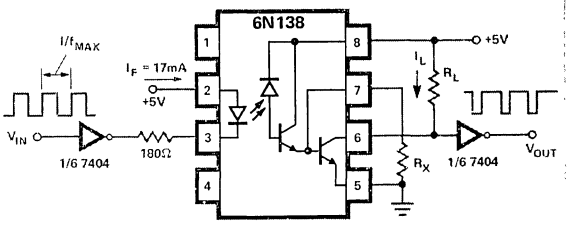
FOR HIGHER FANOUT WITH COMPARABLE DATA RATES USE SMALLER VALUES OF R_{IN}

f_{MAX} IS THE FREQUENCY AT WHICH A 50% DUTY FACTOR AT THE INPUT IS DEGENERATED TO 10% OR 90% DUTY FACTOR AT THE OUTPUT.

R_L(Ω)	R_{IN}(Ω)	I_F(mA)	f_{MAX} (kHz)
2200	1800	1.7	40
270	390	8	125
100	180	17	250

GAIN/SPEED TRADE OFF

- Obtain Maximum Speed at Required Gain
- Single Resistor Required
- Use same device for Multiple Applications

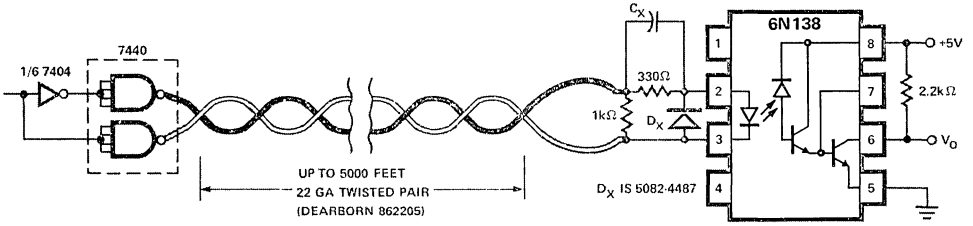


f_{MAX} IS THE FREQUENCY AT WHICH A 50% DUTY FACTOR AT THE INPUT IS DEGENERATED TO 10% or 90% DUTY FACTOR AT THE OUTPUT.

R_X (Ω)	R_L (Ω)	I_L (mA)	f_{MAX} (kHz)
NONE	100	46	250
820	1000	4.6	650

1-5000 FT. LINE RECEIVER

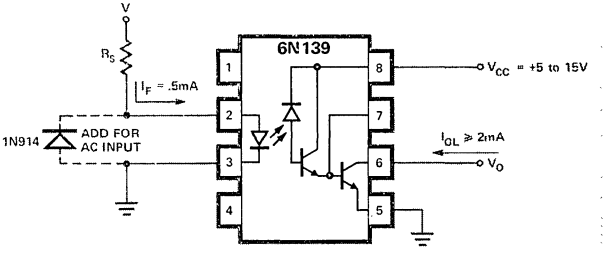
- Drive with Standard TTL Buffer Gate
- 2500V 60Hz Common Mode Rejection
- Allows use of Low Cost Line
- 40kbs Data Rate
- TTL Compatible Output



PROPAGATION DELAY: WITHOUT C_X,D_X, t_{PLH} = 2 to 5 μs; t_{PHL} = 25μs
WITH D_X, C_X ≥ 0.002μF, t_{PLH} = 2μs; t_{PHL} = 7μs

HIGH VOLTAGE STATUS INDICATOR

- Low Power Consumption
- TTL Compatible Output
- High Speed
- Use for Power Turn On Anticipation Circuit, 117V Line Monitor or Other High Voltage Sensing

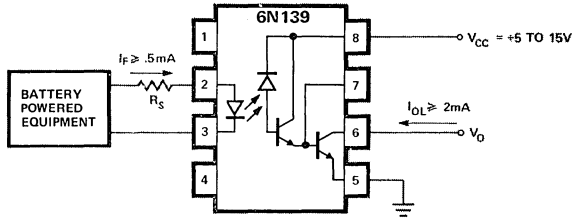


V(Vdc or Vrms)	R_S	V • I_F (mW)
24	47kΩ	11
48	100kΩ	22
117	220kΩ	62
230	470kΩ	113

APPLICATION NOTES

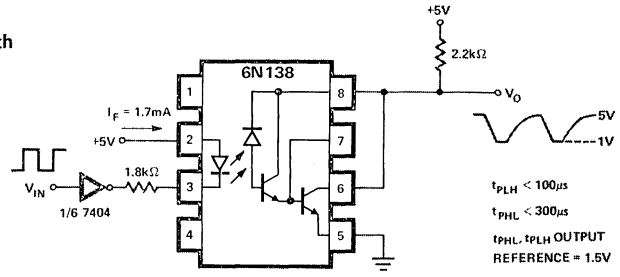
MEDICAL EQUIPMENT ISOLATION

- Low Power Consumption
- 2500V 60Hz Isolation
- Digital or Analog Operation



CONVENTIONAL DARLINGTON

- No Bias Supply Required
- Base Lead available for Gain/Bandwidth Adjust
- Data Rates of 2kbs



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COMPONENTS

APPLICATION NOTE 951-2

Linear Applications of Optocouplers

Optocouplers are useful in applications where analog or DC signals need to be transferred from one module to another in the presence of a large potential difference or induced noise between the ground or common points of these modules.

Potential applications are those in which large transformers, expensive instrumentation amplifiers or complicated A/D conversion schemes are used. Examples are: sensing circuits (thermocouples, transducers ...), patient monitoring equipment, power supply feedback, high voltage current monitoring, adaptive control systems, audio amplifiers and video amplifiers.

HP's optocouplers have integrated photodetector/amplifiers with speed and linearity advantages over conventional phototransistors. In a photo transistor, the photodetector is the collector-base junction so the capacitance impairs the collector rise time. Also, amplified photocurrent flows in the collector-base junction and modulates the photo-response, thereby causing non-linearity. The photodetector in an HP optocoupler is a separately integrated diode so its photoresponse is not affected by amplified photocurrent and its capacitance does not impair speed. Some linear isolation schemes employ digital conversion techniques (A/D-D/A, PWM, PCM, etc.) in which the higher speed of the integrated photodetector permits better linearity and bandwidth.

The 6N135/6N136 is recommended for single channel AC analog designs. The HCPL-2530/31 is recommended for dual channel DC linear designs. The 6N135/6 series or the 6N137 series are recommended for digital conversion schemes.

If the output transistor is biased in the active region, the current transfer relationship for the 6N135 series optocoupler can be represented as:

$$I_C = K \left(\frac{I_F}{I_F'}\right)^n$$

where I_C is the collector current; I_F is the input LED current; I_F' is the current at which K is measured; K is the collector current when $I_F = I_F'$; and n is the slope of I_C vs. I_F on logarithmic coordinates.

The exponent n varies with I_F, but over some limited range of ΔI_F, n can be regarded as a constant. The current transfer relationship for an opto isolator will be linear only if n equals one.

For the 6N135 series optocoupler, n varies from approximately 2 at input currents less than 5mA to approximately 1 at input currents greater than 16mA. For AC coupled applications, reasonable linearity can be obtained with a single optocoupler. The optocoupler is biased at higher levels of input LED current where the ratio of incremental photodiode current to incremental LED current ($\partial I_D/\partial I_F$) is more nearly constant.

For better linearity and stability, servo or differential linearization techniques can be used.

The servo linearizer forces the input current of one optocoupler to track the input current of the second optocoupler by servo action. Thus, if $n_1 \simeq n_2$ over the excursion range, the non linearities will cancel and the overall transfer function will be linear. In the differential linearizer, an input signal causes the input current of one optocoupler to increase by the same amount that input current of the second optocoupler is decreased. If $n_2 \simeq n_2 \simeq 2$, then a gain increment in the first optocoupler will be balanced by a gain decrement in the second optocoupler and the overall transfer function will be linear. With these techniques, matching of K will not effect the overall linearity of the circuit but will simplify circuit realization by reducing the required dynamic range of the zero and offset potentiometers.

Gain and offset stability over temperature is dependent on the stability of current sources, resistors, and the optocoupler. For the servo technique, changes of K over temperature will have only a small effect on overall gain and offset as long as the ratio of K_1 to K_2 remains constant. With the differential technique, changes of K over temperature will cause a change in gain of the circuit. Offset will remain stable as long as the ratio of K_1 to K_2 remains constant. In the AC circuit, since ($\partial I_D/\partial I_F$) varies with temperature, the gain will also vary with temperature. A thermister can be used in the output amplifiers of the Differential and AC circuits to compensate for this change in gain over temperature.

There are also several digital techniques to transmit an optocoupler analog signal. Optocouplers can be used to transmit a frequency or pulse width modulated signal. In these applications, overall circuit bandwidth is determined by the required linearity as well as the propagation delay of the optocoupler. The 6N137 series optocoupler features propagation delays typically less than 50ns and

the 6N135 series optocoupler features propagation typically less than 300ns.

In several places the circuits shown call for a current source. They can be realized in several ways. If V_{CC} is stable, the current source can be a mirror type circuit as shown in Figure 1.

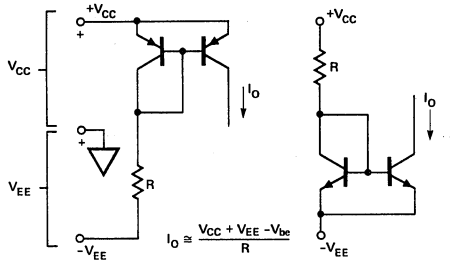


Figure 1.

If V_{CC} is not stable, a simple current source such as the ones shown in Figure 2 can be realized with an LED as a voltage reference. The LED will approximately compensate the transistor over temperature since $\Delta V_{be}/\Delta T \cong \Delta V_F/\Delta T = -2mV/°C$:

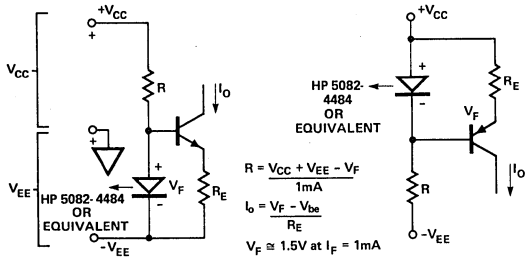


Figure 2.

SERVO ISOLATION AMPLIFIER

The servo amplifier shown in Figure 3 operates on the principle that two optocouplers will track each other if their gain changes by the same amount over some operating region. U_2 compares the outputs of each optocoupler and forces I_{F2} through D_2 to be equal to I_{F1} through D_1. The constant current sources bias each I_F at 3mA quiescent current. R_1 has been selected so that I_{F1} varies over the range of 2mA to 4mA as V_{IN} varies from —5V to +5V. R_1 can be adjusted to accommodate any desired range. With V_{IN}=0, R_2, is adjusted so that V_{OUT}=0. Then with V_{IN} at some value, R_4 can be adjusted for a gain of 1. Values for R_2 and R_4 have been picked for a worst case spread of optocoupler or current transfer ratios. The transfer function of the servo amplifier is:

$$V_{OUT} = R_4\left[\left(\frac{I_F}{2}\right)\left(\frac{K_1 R_2 (I_{CC_1})^{n_1}}{K_2 R_3 (I_F')^{n_1}}\right)^{1/n_2}\left(1+\frac{V_{IN}}{R_1 I_{CC_1}}\right)^{n_1/n_2} - I_{CC_2}\right]$$

After zero adjustment, this transfer function reduces to:

$$V_{OUT} = R_4 I_{CC_2}\left[(1+x)^n - 1\right], \text{ where } x = \frac{V_{IN}}{R_1 I_{CC_1}}, n = \frac{n_1}{n_2}$$

The non linearities in the transfer function where $n_1 \neq n_2$ can be written as shown below. For example, if $|x| \leq .35$, $n = 1.05$, then the linearity error is 1% of the desired signal.

$$\frac{\text{linearity error}}{\text{desired signal}} = \frac{(1+x)^n - n\,x - 1}{n\,x}$$

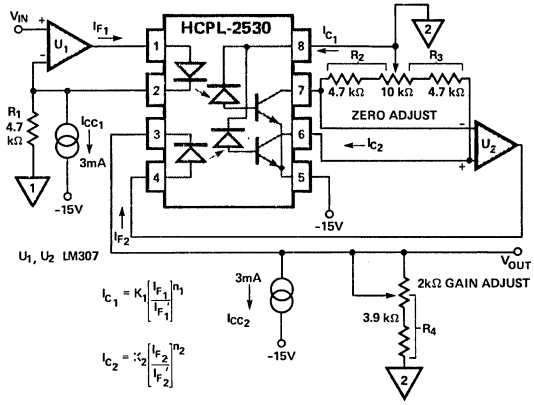


Figure 3. Servo Type DC Isolation Amplifier.

Typical Performance for the Servo Linearized DC Amplifier:

1% linearity for 10V p-p dynamic range
Unity voltage gain
25 kHz bandwidth (limited by U_1, U_2)
Gain drift: —.03%/°C
Offset drift: ±1 mV/°C
Common mode rejection: 46dB at 1 kHz
500V DC insulation (3000V if 2 single couplers are used)

DIFFERENTIAL ISOLATION AMPLIFIER

The differential amplifier shown in Figure 4 operates on the principle that an operating region exists where a gain increment in one optocoupler can be approximately balanced by a gain decrement in the second optocoupler. As I_{F1} increases due to changes in V_{IN}, I_{F2} decreases by an equal amount. If $n_1 = n_2 = 2$, then the gain increment caused by increases in I_{F1} will be balanced by the gain decrement caused by decreases in I_{F2}. The constant current source biases each I_F at 3mA quiescent current. R_1 and R_2 are designed so that I_F varies over the range of 2mA to 4mA as V_{IN} varies from —5V to +5V. R_1 and R_2 can be adjusted to accommodate any desired dynamic range. U_3 and U_4 are used as a differential current amplifier:

$$V_{OUT} = R_5\left[(R_3/R_4)\, I_{C1} - I_{C2}\right]$$

R_3, R_4, R_5 have been picked for an amplifier with a gain of 1 for a worst case spread of coupler current transfer ratios. The transfer function of the differential amplifier is:

$$V_{OUT} = R_5\left[\left(\frac{K_1 R_3}{R_4}\right)\left(\frac{I_{CC}}{2 I_F'}\right)^{n_1}\left(1+\frac{V_{IN}}{R\, I_{CC}}\right)^{n_1} - K_2\left(\frac{I_{CC}}{2 I_F'}\right)^{n_2}\left(1-\frac{V_{IN}}{R\, I_{CC}}\right)^{n_2}\right]$$

if $R \equiv R_1 \equiv R_2$

After zero adjustment, this transfer function reduces to:

$$V_{OUT} = R_5 K' \left[\left(1 + \frac{V_{IN}}{R\ I_{CC}}\right)^{n_1} - \left(1 - \frac{V_{IN}}{R\ I_{CC}}\right)^{n_2} \right],$$

$$\text{where } K' = \frac{K_1 R_3}{R_4} \left(\frac{I_{CC}}{2\ I_{F'1}}\right)^{n_1} = K_2 \left(\frac{I_{CC}}{2\ I_{F'2}}\right)^{n_2}$$

The non linearities in the transfer function when $n_1 \neq n_2 \neq 2$ can be written as shown below. For example, if $|x| \leq .35$, $n_1 = 1.9$, $n_2 = 1.8$, then the linearity error is 1.5% of the desired signal.

$$\frac{\text{linearity error}}{\text{desired signal}} = \frac{(1+x)^{n_1} - (1-x)^{n_2} - (n_1 + n_2)\,x}{(n_1 + n_2)\,x}, \text{ where } x = \frac{V_{IN}}{R\ I_{CC}}$$

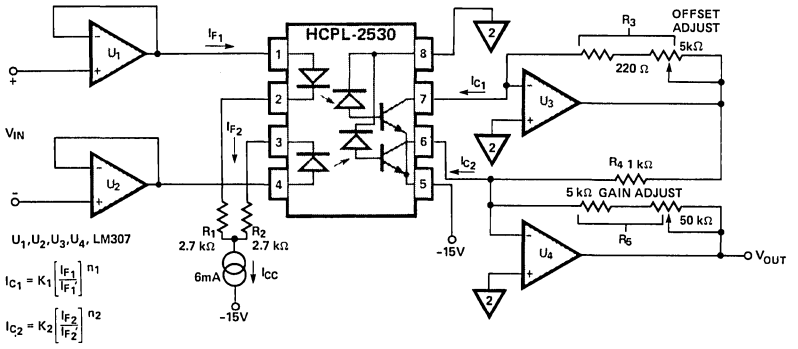


Figure 4. Differential Type DC Isolation Amplifier.

Typical Performance of the Differential Linearized DC Amplifier:

3% linearity for 10V p-p dynamic range
Unity voltage gain
25 kHz bandwidth (limited by U_1, U_2, U_3, U_4)
Gain drift: −.4%/°C
Offset drift: ±4mV/°C
Common mode rejection: 70dB at 1 kHz
3000V DC insulation

AC COUPLED AMPLIFIER

In an AC circuit, since there is no requirement for a DC reference, a single optocoupler can be utilized by biasing the optocoupler in a region of constant incremental CTR ($\partial I_D/\partial I_F$). An example of this type of circuit is shown in Figure 5. Q_1 is biased by R_1, R_2 and R_3 for a collector quiescent current of 20mA. R_3 is selected so that I_F varies from 15mA to 25mA for V_{IN} of 1V p-p. Under these operating conditions, the 6N136 operates in a region of almost constant incremental CTR. Linearity can be improved at the expense of signal-to-noise ratio by reducing I_F excursions. This can be accomplished by increasing R_3, then adding a resistor from the collector of Q_1 to ground to obtain the desired quiescent I_F of 20mA. Q_2 and Q_3 form a cascade amplifier with feedback applied through R_4 and R_6. R_6 is selected as V_{be}/I_3 with I_3 selected for maximum gain bandwidth product of Q_3. R_7 is selected to allow maximum excursions of V_{OUT} without clipping. R_5 provides DC bias to Q_3. Closed loop gain ($\Delta V_{OUT}/\Delta V_{IN}$) can be adjusted with R_4. The transfer function of the amplifier is:

$$\frac{V_{OUT}}{V_{IN}} \cong \left(\frac{\partial I_D}{\partial I_F}\right)\left(\frac{1}{R_3}\right)\left(\frac{R_4\ R_7}{R_6}\right)$$

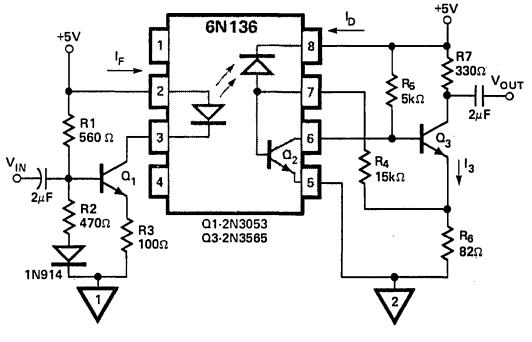


Figure 5. Wide Bandwidth AC Isolation Amplifier.

Typical Performance of the Wide Bandwidth AC Amplifier:

2% linearity over 1V p-p dynamic range
Unity voltage gain
10 MHz bandwidth
Gain drift: −.6%/°C
Common mode rejection: 22dB at 1 MHz
3000V DC insulation

DIGITAL ISOLATION TECHNIQUES

Digital conversion techniques can be used to transfer an analog signal between two isolated systems. With these techniques, the analog signal is converted into some digital form and transmitted through the optocoupler. This digital information is then converted back to the analog signal at the output. Since the optocoupler is used only as a switch, the overall circuit linearity is primarily dependent on the accuracy by which the analog signal can be converted into digital form and then back to the analog signal. However, the overall circuit bandwidth is limited by the propagation delays of the optocoupler.

Figure 6 shows a pulse width modulated scheme to isolate an analog signal. The oscillator operates at a fixed frequency, f, and the monostable multivibrator varies the duty factor of the oscillator proportional to the input signal, V_{IN}. The maximum frequency at which the oscillator can be operated is determined by the required linearity of the circuit and the propagation delay of the opto isolators:

$$(t_{max} - t_{min}) \text{ (required linearity)} \geq |t_{PLH} - t_{PHL}|$$

At the output, the pulse width modulated signal is then converted back to the original analog signal. This can be accomplished with an integrator circuit followed by a low pass filter or through some type of demodulator circuit that gives an output voltage proportional to the duty factor of the oscillator.

Figure 7 shows a voltage to frequency conversion scheme to isolate an analog signal. The voltage to frequency converter gives an output frequency proportional to V_{IN}. The maximum frequency that can be transmitted through the optocoupler is approximately:

$$f_{max} \approx \frac{1}{t}, \text{ where } t = t_{PLH} \text{ or } t_{PHL}, \text{ whichever is larger.}$$

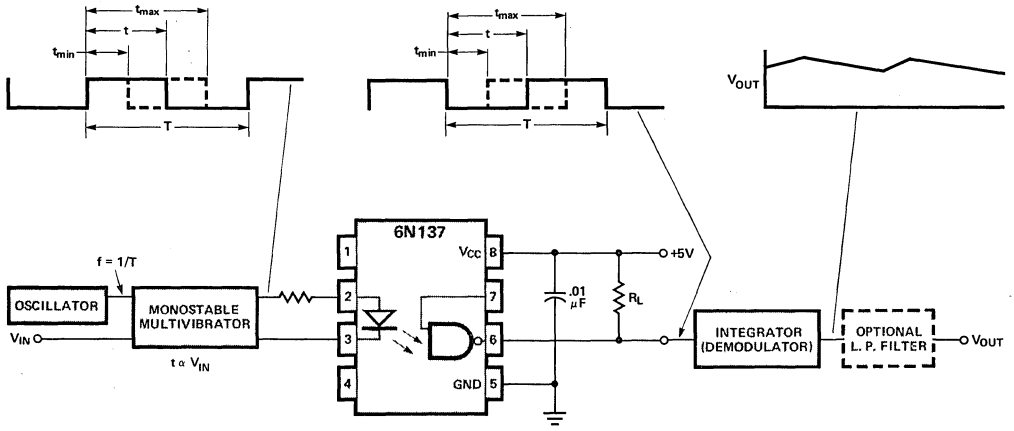


Figure 6. Pulse Width Modulation.

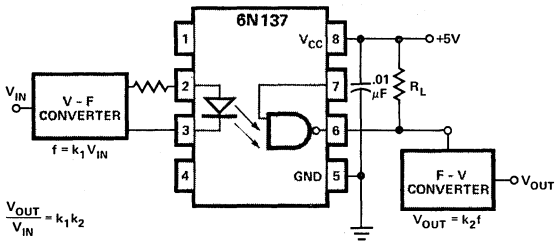


Figure 7. Voltage to Frequency Conversion.

At the output, the frequency is converted back into a voltage. The overall circuit linearity is dependent only on the linearity of the V-F and F-V converters.

Another scheme similar to voltage to frequency conversion is frequency modulation. A carrier frequency, f_o, is modulated by Δf such that $f_o \pm \Delta f$ is proportional to V_{IN}. Then at the output, V_{OUT} is reconstructed with a phase locked loop or similar circuit.

One further scheme to isolate an analog signal is to use A-D and D-A converters and transfer the binary or BCD information through optocoupler. The information can be transmitted through the optocoupler in parallel or serial format depending on the outputs available from the A-D converter. If serial outputs are not available, the A-D outputs can be converted into serial form with a PISO shift register and transmitted through one high speed optocoupler. This scheme becomes economical especially where high resolution is required allowing several optocouplers to be replaced with one high speed optocoupler. Refer to HP Application Note 947 for further discussion of digital data transmission techniques.

HEWLETT PACKARD

COMPONENTS

APPLICATION NOTE 964

Contrast Enhancement Techniques

Why Contrast Enhancement?

The most important attribute of any equipment utilizing a digital readout is the ability to clearly display information to an observer. A person viewing the display must be able to quickly and accurately recognize the information being displayed by the instrument. The display, usually front panel mounted, must be visible without difficulty in the ambient light conditions where the instrument will be used.

Since most ambient light levels are sufficiently bright to impair the visibility of an LED display it is necessary to employ certain techniques to develop a high viewing contrast between the display and its background. Since the quality of visibility is primarily subjective, it is not easily measured or treated by analytical means. Thus, human engineering plays a very important role in display applications. The best judge of the viewing esthetics of a display is the human eye. In short, is the final display design pleasing to the eye when viewed in the end use ambient?

This application note presents various criteria and techniques that a display designer should consider to obtain optimum contrast enhancement for red, yellow and green LED displays. A representative list of filter manufacturers and available filters is given at the end of this discussion.

Basic Concepts

The objective of contrast enhancement is to maximize the contrast between display "On" and display "Off" conditions. This is accomplished by (1) reducing to a minimum the reflected ambient light from the face of the display and (2) allowing a maximum of the display's emitted light to reach the eye of a viewer. The goal is to achieve a maximum contrast between "On" segments and "Off" segments as well as a maximum contrast between "Off" segments and display package and background.

Let us begin by defining the following basic terms:
Contrast Ratio, CR, may be defined as follows:

$$CR = \frac{\text{Source Luminance} + \text{Background Luminance}}{\text{Background Luminance}}$$

Contrast Improvement Ratio, CIR, may be defined as follows:

$$CIR = \frac{CR\ (\text{With Filter})}{CR\ (\text{Without Filter})}$$

It is desirable to have as high a CR as possible. One is able to measure the improvement in contrast enhancement by the CIR.

Contrast Ratio is usually applied to the face of a display as a whole. However, with stretched segment displays, such as Hewlett-Packard's 5082-7750 and 5082-7760 displays, it is difficult to achieve a high value of segment on/off contrast while effectively concealing the display package from view. For example, a display with a black package is easily concealed from view, however, the "Off" segments will be visible. This is due to the difference in reflectivity between the "Off" segments and the black package.

A reduction in the reflectivity difference between the "Off" segments and the package of a stretched segment display may be obtained by adding a small amount of dye to color tint the segments, and the display package may be colored to match the off segment color. With the addition of an appropriate optical filter placed in front of the display, the "Off" segments tend to be indistinguishable from the background. The trade-off is that a colored package is more visible than a black package. Because of this trade-off a designer has to decide which is more important, concealing "Off" segments or concealing the display package. Since the usual choice is to conceal "Off" segments, Hewlett-Packard is using this colored package technique on its 5082-7600 series High-Efficiency Red, Yellow and Green Stretched Segment Displays.

Contrast enhancement under artificial lighting conditions may be accomplished by use of selected wavelength optical filters. Under bright sunlight conditions contrast enhancement becomes more difficult and requires additional techniques such as the use of louvered filters combined with shading of the display. The effect of a wavelength optical filter is illustrated in Figure 1. The filtered portion of the display can be easily read while the "Off" segments are not apparent. By comparison, reading the unfiltered portion of the display is difficult.

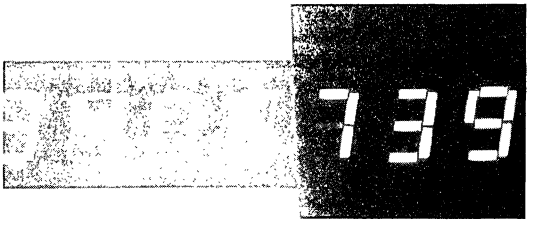


Figure 1. Effect of wavelength optical filter on LED display.

APPLICATION NOTES

Eye Response, Peak Wavelength and Dominant Wavelength

The 1931 CIE (Commission Internationale De L'Eclairage) standard observer curve, also known as the photopic curve, is shown in Figure 2. This curve represents the eye response of a standard observer to various wavelengths of light. The vivid color ranges are also identified in Figure 2. The photopic curve peaks at 555 nanometers (nm) in the yellowish-green region. This peak corresponds to 680 lumens of luminous flux (lm) per watt of radiated power (W).

Two wavelengths of the LED emission are important to a user of LED displays; Peak Wavelength and Dominant Wavelength. **Peak Wavelength** (λ_p) is the wavelength of the peak of the radiated spectrum. The peak wavelength may be used to estimate the approximate amount of display emitted light that is passed by an optical filter. For example, if an optical filter has a relative transmission of 40% at a given λ_p, then approximately 40% of the display emitted light at the peak wavelength will pass through the filter to the viewer while 60% will be absorbed. This gives a designer an initial estimate of the amount of loss of display emitted light he should expect.

Dominant Wavelength (λ_d) is used to define the color of an LED display. Since an LED approximates a monochromatic light source, the dominant wavelength of an LED may be defined as the single wavelength which is perceived by the eye to match the complete radiated spectrum of the device. As an example, the dominant wavelength of Hewlett-Packard's "Yellow" Display, which has a peak wavelength of 583 nm, is 585 nm. As shown in Figure 2, the actual color corresponding to λ_d = 585 nm is yellowish-orange. Therefore, an optimum wavelength filter will be one that is yellowish-orange (or amber) in color.

Both peak wavelength and dominant wavelength are listed in the electrical-optical characteristics on the data sheets for Helwett-Packard's LED display and lamp products.

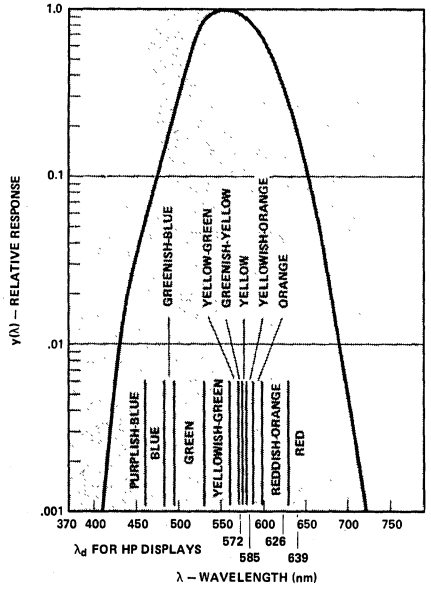


Figure 2. CIE Standard observer eye response curve (photopic curve), including CIE vivid color ranges.

Filter Transmittance

The relative transmittance of an optical filter with respect to wavelength is:

$$T(\lambda) = \frac{\text{Luminous Flux with Filter at Wavelength } \lambda}{\text{Luminous Flux without Filter at Wavelength } \lambda}$$

Most manufacturers of wavelength filters for use with LED displays provide relative transmittance curves for their products. Sample transmittance curves are presented in Figures 3, 4, 5 and 6. These curves represent approximate filter characteristics which may be used in various ambient light levels. The total transmittance curve shape and wavelength cut-off points have been chosen in direct relationship to the LED radiated spectrum. Each filter curve has been empirically determined and is similar to commercially available products. The higher the ambient light[1], the more optically dense the filter must be to absorb reflected light from the face of the display. Because the display emitted light is also strongly absorbed, the display must be driven at a high average current to be readily visible. For dim ambient light, the filter may have a high value of transmittance as the ambient light will be at levels much less than display emitted light. The display can now be driven at a low average current.

Listed on each filter transmittance curve (Figures 3, 4, 5 and 6) are empirically selected ranges of relative transmittance values at the peak wavelength which may give satisfactory filtering. For example, a filter to be used with a yellow display in moderate ambient lighting could have a transmittance value at the peak wavelength [$T(\lambda_p)$] between 0.15 and 0.30. The filter wavelength cut-off should occur between 530 and 550 nm for best results.

When selecting a filter, the transmittance curve shape, attenuation at the peak wavelength and wavelength cut-off should be carefully considered in relationship to the LED radiated spectrum and ambient light level so as to obtain optimum contrast enhancement.

[1] Dim ambients are in the range of 3 to 20 footcandles (32 to 215 lux), moderate ambients are in the range of 20 to 100 footcandles (215 to 1076 lux), and bright ambients are in the range of 100 to 500 footcandles (1076 to 5382 lux). Footcandle = (lm/ft^2) and lux = (lm/m^2).

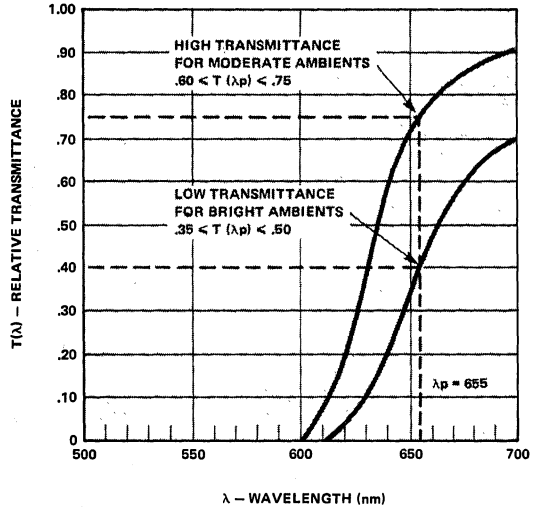


Figure 3. Typical transmittance curve for filters to be used with HP standard GaAsP red displays.

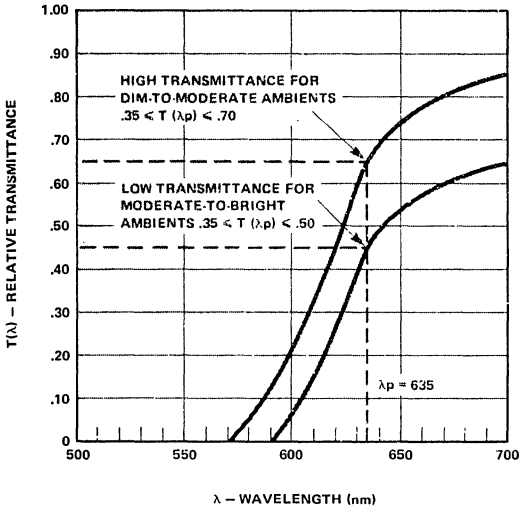


Figure 4. Typical transmittance curves for filters to be used with HP high-efficiency red displays.

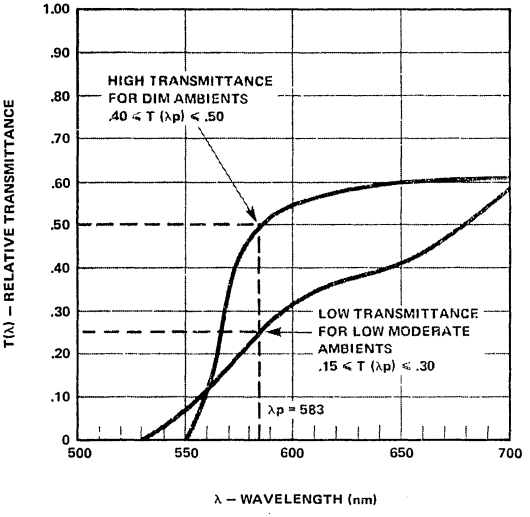


Figure 5. Typical transmittance curves for filters to be used with HP yellow displays.

Wavelength Filtering

The application of wavelength filters as described in the previous section is the most widely used method of contrast enhancement under artificial lighting conditions. Wavelength filters are very effective in artificial lighting. However, they are not very effective in daylight due to the high level ambient light. Filtering in daylight conditions is best achieved by using louvered filters (discussed in a later section).

Figures 7, 8, 9 and 10 show the relationship between artificial lighting and the spectra of LED displays, both unfiltered and filtered. Figures 7a through 10a show the relationship between the various LED spectra and the spectra of daylight flourescent and incandescent light. The photometric spectrum (shaded curve) is obtained by multiplying the LED radiated spectrum [f(λ)] by the photopic curve

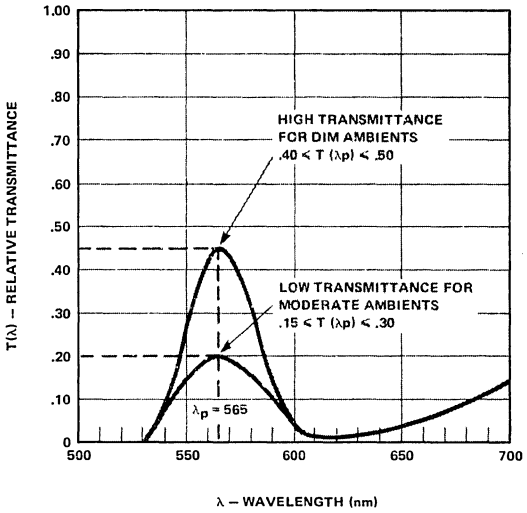


Figure 6. Typical transmittance curves for filters to be used with HP green displays.

[y(λ)]. Thus, photometric spectrum = f(λ)•y(λ). Figures 7b through 10b demonstrate the effect of a wavelength filter. The filtered photometric spectrum is what the eye perceives when viewing a display through a filter (shaded curve). Thus, filtered photometric spectrum = f(λ)•y(λ)•T(λ). The ratio of the area under the filtered photometric spectrum to the area under the unfiltered photometric spectrum is the fraction of the visible light emitted by the display which is transmitted by the filter:

$$\text{Fraction of Available Light from Filtered Display} = \frac{\int f(\lambda)\cdot y(\lambda)\cdot T(\lambda)\cdot d\lambda}{\int f(\lambda)\cdot y(\lambda)\cdot d\lambda}$$

In addition to attenuating a portion of the light emitted by the display, a filter also shifts the dominant wavelength, thus causing a shift in the perceived color. For a given display spectrum, the color shift depends on the cut-off wavelength and shape of the filter transmittance characteristic. A choice among available filters must be made on the basis of which filter and LED combination is most pleasing to the eye. A designer must experiment with each filter as he cannot tell by transmittance curves alone. The filter spectra presented in Figures 3, 4, 5 and 6 are suggested starting points. Filters with similar characteristics are commercially available.

Filtering Red Displays (λp = 655 nm) Filtering out reflected ambient light from red displays is easily accomplished with a long wavelength pass filter having a sharp cut-off in the 600 nm to 625 nm range (see Figures 3 and 7b). Under bright flourescent light, a red filter is very effective due to the low concentration of red in the flourescent spectrum. The spectrum of incandescent light contains a large amount of red, and therefore, it is difficult to filter red displays effectively in bright incandescent light.

Filtering High-Efficiency Red Displays (λp = 635 nm) The use of a long wavelength pass filter with a cut-off in the 570 nm to 590 nm range gives essentially the same results as is obtained when filtering red displays (see Figures 4 and 8b). The resulting color is a rich reddish-orange.

Filtering Yellow Displays (λp = 583 nm) The peak wavelength of a yellow LED display is in the region of the

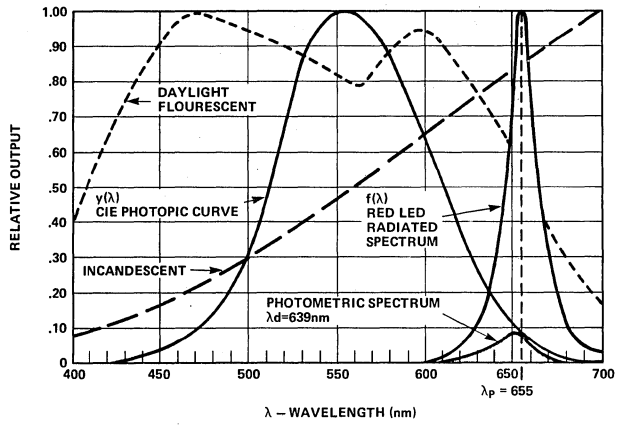


Figure 7A. Relative relationship between standard GaAsP red LED display spectrum, photopic curve and artificial lighting.

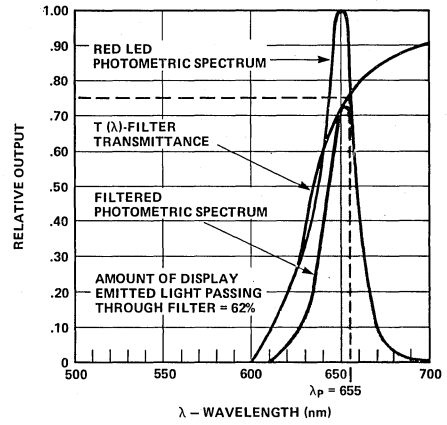


Figure 7B. Effect of a long pass wavelength filter on red LED displays.

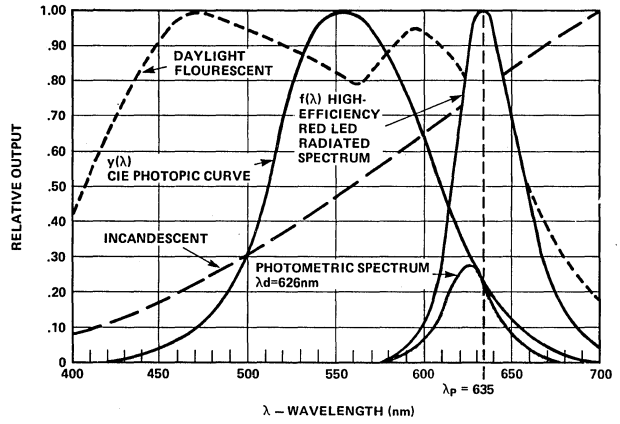


Figure 8A. Relative relationship between high-efficiency red LED display, photopic curve and artificial lighting.

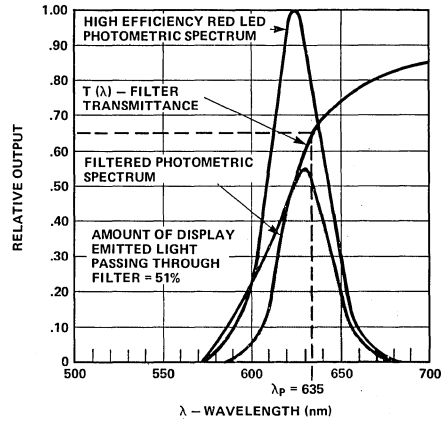


Figure 8B. Effect of a long pass wavelength filter on high-efficiency red LED displays.

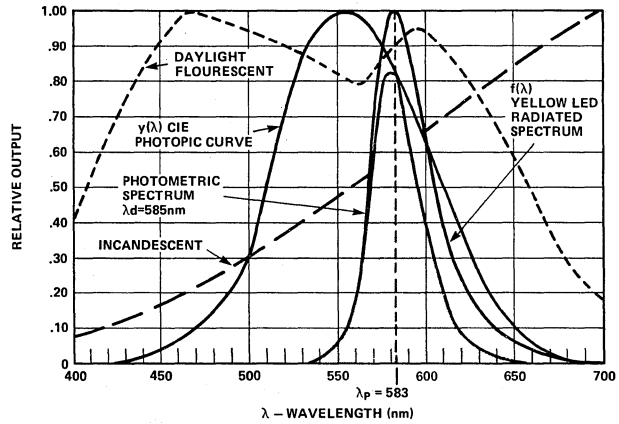


Figure 9A. Relative relationship between yellow LED displays, photopic curve and artificial lighting.

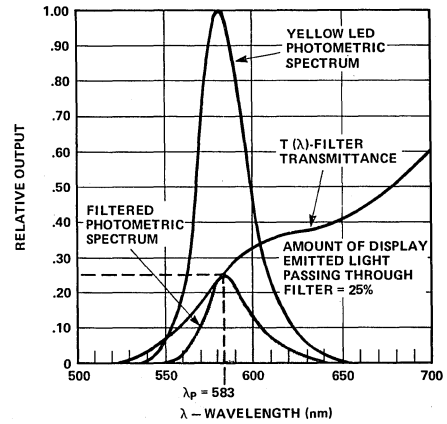


Figure 9B. Effect of a long pass wavelength filter on yellow LED displays.

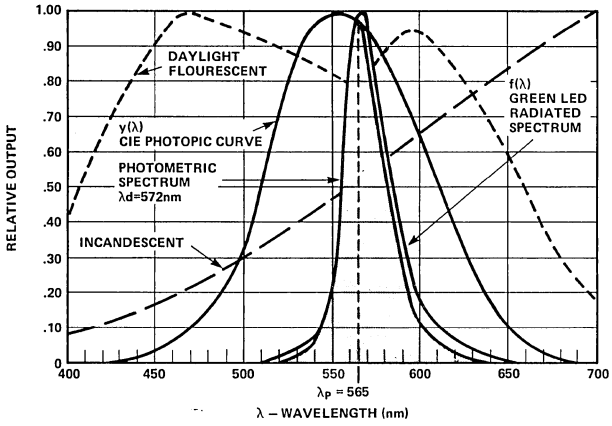


Figure 10A. Relative relationship between green LED displays, photopic curve and artificial lighting.

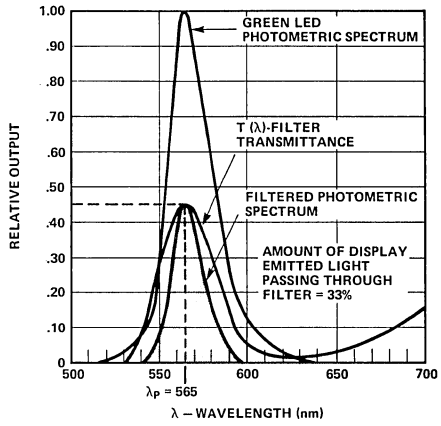


Figure 10B. Effect of a bandpass wavelength filter on green LED displays.

photopic curve where the eye is most sensitive (see Figure 9a). Also, there is a high concentration of yellow in the spectrum of flourescent light and a lesser amount of yellow in incandescent light. Therefore, filters that are more optically dense than red filters at the peak wavelength are required to filter yellow displays. The most effective filters are the dark yellowish-orange (or dark amber) filters as shown in Figure 5. The use of a low transmittance yellowish-orange filter, as shown in Figure 9b, results in a similar color to that of a gas discharge display. Pure yellow filters provide very little contrast enhancement.

Filtering Green Displays (λp = 565 nm) The peak wavelength of a green LED display is only 10 nm from the peak of the eye response curve (see Figure 10a). Therefore, it is very difficult to effectively filter green displays. A long wavelength pass filter, such as is used for red and yellow displays, is no longer effective. An effective filter is obtained by combining the dye of a short wavelength pass filter with the dye of a long wavelength pass filter, thus forming a bandpass yellow-green filter which peaks at 565 nm as shown in Figure 6. Pure green filters peak at 520 nm and drop off rapidly in the 550 nm to 570 nm range and are not recommended. The best possible filters for green LED displays are those which are yellow-green bandpass, peaking at 565 nm and dropping off rapidly between 575 nm and 590 nm. As shown in Figure 10b, this filter passes wavelengths 550 to 570 while sharply reducing the longer wavelengths in the yellow region. To effectively filter green LED displays in flourescent light would require the use of a filter with a low transmittance value at the peak wavelength. This is due to the high concentration of green in the flourescent spectrum. It is easier to filter green displays in bright incandescent light due to the low concentration of green in the incandescent spectrum, see Figure 10a.

Three manufacturers of wavelength filters are **Panelgraphic Corporation** (Chromafilter®), **SGL Homalite** and **Rohm & Haas Company** (Plexiglas). The LED filters produced by these manufacturers are useable with all of Hewlett-Packard's display and lamp products. Table 2 lists some of the filter manufacturers and where to go for further information. Table 3 lists some specific wavelength filter products with recommended applications.

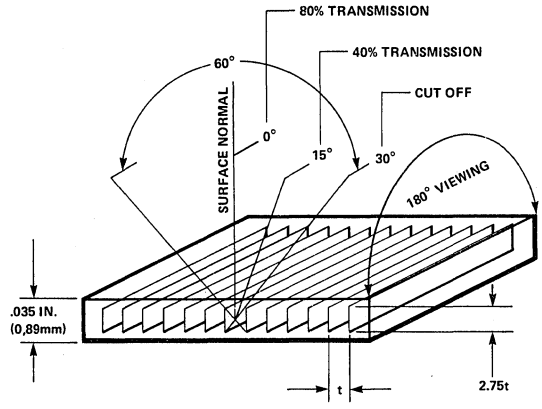
Louvered Filters

Louvered filters are very effective in reducing the amount of bright artificial light or daylight reflected from the face of a display, without a substantial reduction in display emitted light. The construction of a louvered filter is diagrammed in Figure 11. Inside a plastic sheet are thin parallel louvers which may be oriented at a specific angle with respect to the surface normal. The zero degree louvered filter has the louvers perpendicular to the filter surface.

The operation of a louvered filter is similar to a venetian blind as shown in Figure 12. Light from the LED display passes between the parallel louvers to the viewer. Off-axis ambient light is blocked by the louvers and therefore is not able to reach the face of the display to be reflected back to the viewer. This results in a very high contrast ratio with minimal loss of display emitted light at the On-axis viewing angle. The trade-off is a restricted viewing angle. For example, the zero degree louvered filter shown in Figure 11 has a horizontal viewing angle of 180°; however, the vertical viewing included angle is 60°. The louver aspect ratio (louver depth/distance between louvers) determines viewing angle. A list of louver option possibilities is given in Table 1.

Some applications require a louver orientation other than zero degrees. For example, an 18 degree louvered filter may be used on the sloping top surface of a point of sale terminal. A second, is the use of a 45 degree louvered filter on overhead instrumentation to block out ambient light from ceiling mounted lighting fixtures.

Louvered filters are effective filters for enhancing the viewing of LED displays installed in equipment operating under daylight ambient conditions. In bright sunlight, the most effective filter is the crosshatch louvered filter. This is essentially two zero degree neutral density louvered filters oriented at 90 degrees to each other. Red, yellow and green digits may be mounted side by side in the same display. Using only the crosshatch filter, all digits will be clearly visible and easily read in bright sunlight as long as the sunlight is not parallel to the viewing axis. The trade-off is restricted vertical and horizontal viewing. The effective viewing cone is an included angle of 40° degrees (for a filter aspect ratio of 2.75:1).



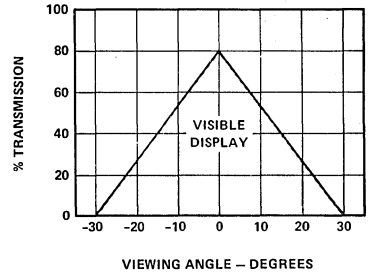


Figure 11. Construction characteristics of 0° neutral density louvered filter.

Table 1. Available Options for Louvered Filters – Any Combination is Possible

Aspect Ratio and Viewing Angle	Louver Angle	Louver Color
2.75:1 = 60°	0°	Opaque Black
2.0:1 = 90°	18°	Translucent Gray
3.5:1 = 48°	30°	Transparent Black
	45°	

Example: 2.75:1 – 18° – Transparent Black

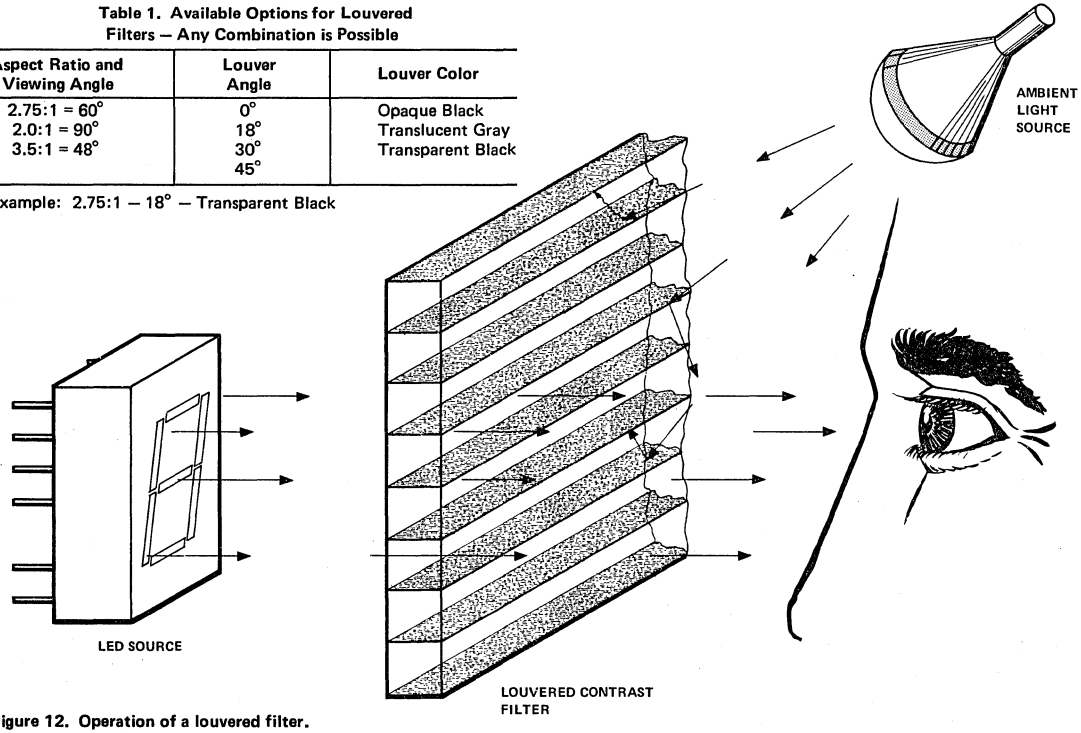


Figure 12. Operation of a louvered filter.

Neutral density louvered filters are effective by themselves in most bright ambient lighting conditions without the aid of a secondary wavelength filter. However, colored louvered filters may be used for additional wavelength filtering at the expense of display emitted light.

3M Company, Light Control Divison, manufactures louvered filters for LED displays. Their product trade name is "Light Control Film", which is useable with all of Hewlett-Packard's LED display and lamp products.

Circular Polarizing Filters

Circular Polarizing Filters are effective when used with LED displays that have specular reflecting front surfaces. Specular reflecting surfaces reflect light without scattering. Displays that have polished glass or plastic facial surfaces belong to this category. Circular Polarizing Filters are effective when used with Hewlett-Packard's 5082-7010, -7100 and -7300 series displays.

The operation of a circular polarizer may be described as follows. As shown in Figure 13, the filter consists of a laminate of a linear polarizer and a quarter wave plate. A quarter wave plate has its optical axis parallel to the flat surface of the polarizer and is oriented at 45° to the linear polarization axis. Non-polarized light is first linearly polarized by the linear polarizer. The linearly polarized light has x and y components with respect to the quarter wave plate.

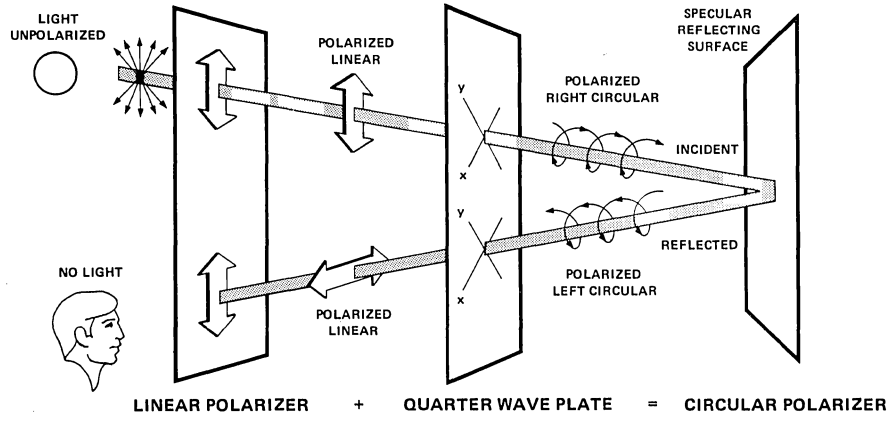


Figure 13. The operation of a circular polarizer.

As the light passes through the quarter wave plate, the x and y components emerge 90° out of phase with each other. The polarized light now has x and y forming a helical pattern with respect to the optical path, and is termed circular polarized light. As this circular polarized light is reflected by the specular reflecting surface, the circular polarization is reversed. When the light passes back through the quarter wave plate it becomes linearly polarized at 90° to the linear polarizer. Thus reflected ambient light is blocked.

The advantage of a circular polarizer is that reflected ambient light is reduced more than 95%. However, the trade-off is that display emitted light passing through the circular polarizer is reduced by approximately 65% at the peak wavelength. This then necessitates an increased drive current for the display, more than that required for a wavelength filter.

Circular polarizers are normally colored to obtain additional selected wavelength filtering. **One Caution:** outdoor applications will require the use of an ultraviolet, uv, filter in front of the circular polarizer. Prolonged exposure to ultraviolet light will destroy the filter's polarizing properties.

Polaroid Corporation manufactures circular polarizing filters in the United States. In Europe, E. Käseman of West Germany produces high quality circular polarizers.

Anti-Reflection Filters, Mounting Bezels and Other Suggestions

Anti-reflection filters: A filtered display still may not be readable by an observer if glare is present on the filter surface. Glare can be reduced by the addition of an anti-reflection surface as part of the filter. Both sections of the display shown in Figure 14 are filtered. The left hand filter has an anti-reflection surface while the right hand filter does not.

An anti-reflection surface is a mat, or textured, finish or coating which diffuses incident light. The trade-off is that both incident ambient and display emitted light are diffused. It is therefore desirable to mount the filter as close to the display as possible to prevent the display image from appearing fuzzy.

Panelgraphic Chromafilters® come standard with an anti-reflection coating. SGL Homalite offers two grades of a molded anti-reflection surface. 3M Company and Polaroid also offer anti-reflection surface options. Optical coating companies will apply anti-reflection coating for specialized applications, though this is usually an expensive process. Three companies of many which do commercial filter coating are: Optical Coating Labs, Inc., Santa Rosa, California; Optics Technology, Inc., Redwood City, California; Valpey Corporation, Holliston, Massachusetts.

Mounting bezels: It is wise to take into account the added appearance of a front panel that has the display set-off by a bezel. A bezel of black plastic, satin chrome or brushed aluminum, as examples, will accent the display and attract the eye of the viewer. The best effect can be achieved by a custom bezel. Commercial black plastic bezels for digits up to .3 inch (7.62 mm) tall are available, see Table 2.

Other suggestions: When designing the mounting configuration of a display, consider recessing the display and filter 0.25 inch (6.35 mm) to 0.5 inch (12.7 mm) to add some shading effect. If a double sided printed circuit board is used, keep traces away from the normal viewing area or cover the top surface traces with a dark coating so they can not be seen. Mount the display panel in such a manner as to be easily removed if service should become necessary. If possible, mount current limiting resistors on a separate board to reduce the ambient temperature in the vicinity of the displays.

Figure 14. Effect of anti-reflection surface on an optical filter.

Table 2. List of Filter and Bezel Product Manufacturers

Manufacturer	Product
Panelgraphic Corporation 10 Henderson Drive West Caldwell, New Jersey 07006 Phone: (201) 227-1500	Chromafilter® — Wavelength filters with anti-reflective coating; Red, Yellow, Green
SGL Homalite 11 Brookside Drive Wilmington, Delaware 19804 Phone: (302) 652-3686	Wavelength filters; two optional anti-reflective surfaces; three plastic grades; Red, Yellow, Green
3M – Company Visual Products Division 3M Center, Bldg. 235-2E Saint Paul, Minnesota 55101 Phone: (612) 733-5747	3M – Brand Light control film; louvered filters
Rohm and Haas Independence Mall West Philadelphia, Pennsylvania 19105 Phone: (215) 592-3000	Plexiglas; sheet and molding powder; wavelength filters; sold as Oroglas in Europe
Polaroid Corporation Polarizer Division 549 Technology Square Cambridge, Massachusetts 02139 Phone: (617) 864-6000	Circular polarizing filters
E. Käsemann GmbH D 8203 Oberaudorf West Germany Phone: (08033) 342	Circular polarizing filters
Norbex Division Griffith Plastics Corporation 1027 California Drive Burlingame, California 94010 Phone: (415) 344-7691	DIGIBEZEL®; Plastic bezels for LED displays
Industrial Electronic Engineers, Inc. 7720-40 Lemona Avenue Van Nuys, California 91405 Phone: (213) 787-0311	Plastic bezels for .30 inch (7,62mm) tall LED displays
Rochester Digital Displays, Inc. 120 North Main Street Fairport, New York 14450 Phone: (716) 223-6855	Complete mounting kits for H.P. 5082-7300, -7700 and -7600 displays.

Table 3. Specific Wavelength Filter Products

Filter Product	Type of LED Display	Ambient Lighting
Panelgraphic Chromafilter® With Anti-Reflection		
Ruby Red 60 Dark Red 63	Standard Red	Moderate Bright
Yellow 25 Amber 23	Yellow	Dim Moderate
Green 48	Green	Moderate
Gray 10	All Colors	Sunlight
SGL Homalite, Grade 100		
H100-1605	Standard Red	Moderate
H100-1670	High-Efficiency Red	Moderate
H100-1726 H100-1720	Yellow	Dim Moderate
H100-1440 H100-1425	Green	Dim Moderate
H100-1266 Gray	All Colors	Sunlight
Anti-Reflection LR-72: 0.5 inch (12.70mm) Mounting Distance From Display LR-92: Up to 3.0 inch (76.20mm) Mounting Distance From Display		
Rohm & Haas		
Plexiglas 2423 Oroglas 2444	Standard Red	Moderate
3M Company — Visual Products Division Louvered Filters		
R6510	Standard Red	Indirect Sunlight
R6310	High-Efficiency Red	Indirect Sunlight
A5910	Yellow	Indirect Sunlight
G5610	Green	Indirect Sunlight
N0220 25% N.D. Gray	All Colors	Sunlight
Anti-Reflective Matte or Very Light Matte Front Surface Finish		

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Gunter Wyszecki and W.S. Stiles; Color Science Concepts and Methods, Quantitative Data and Formulas; John Wiley & Sons; New York; 1967.

Fred W. Billmeyer, Jr., and Max Saltzman; Principles of Color Technology; Interscience Publishers, Division of John Wiley & Sons; New York; 1966.

J. Pucilowski, R. Schuman, and J. Velasquez; Contrast Enhancement of Light Emitting Diode Displays; Applied Optics, Volume 13, Number 10, October 1974; pp 2248-2252.

J.M. Ralston; Filter Considerations for Light Emitting Diode Displays; Proceeding of the SID; 3rd Quarter 1973; Volume 1413; pp 81-86.

M.R. Allyn, R.W. Dixon, and R.Z. Bachrach; Visibility of Red and Green Electroluminescent Diodes for Color-Anomalous Observers; Applied Optics, Volume 11, Number 11, November 1972; pp 2450-2454.

Application Note 945; Photometry of Red LED's; Hewlett-Packard; October 1973.

HEWLETT hp PACKARD
COMPONENTS

APPLICATION NOTE 966

Applications of the HP HDSP-2000 Alphanumeric Display

This note is intented to serve as a design and application guide for users of the HP HDSP-2000 alphanumeric display device. The information presented will cover: the theory of the device design and operation; considerations for specific circuit designs; thermal management, power derating, and heat sinking; and intensity modulation techniques.

The HP HDSP-2000 device has been designed to provide a high resolution information display subsystem. Each character of the 4 character package consists of a 5x7 array of LEDs which can display a full range of alphabetic and numeric characters plus punctuation, mathematical and other special symbols.

Each character is 3.8mm high by 2.2mm wide with 4.5mm center to center spacing. The overall package size is designed to allow end stacking of multiple clusters to form character strings of any desired length.

ELECTRICAL DESCRIPTION

The on-board electronics of the HP HDSP-2000 display will eliminate some of the classical difficulties associated with the use of alphanumeric displays. Traditionally, single digit LED dot matrix displays have been organized in an x-y addressable array requiring 12 interconnect pins per digit plus extensive row and column drive support electronics. The HP HDSP-2000 provides on-board storage of decoded row data plus constant current sinking row drivers for each of the 28 rows in the 4 character display. This approach allows the user to address each display package through just 11 active interconnections vs. the 176 interconnections and 36 components required to effect a similar function using conventional LED matrices.

Figure 1 is a block diagram of the internal circuitry of the HP HDSP-2000 display. The device consists of four LED matrices and two 14-bit serial-in-parallel-out shift registers. The LED matrix for each character is a 5x7 diode array organized with the anodes of each column tied in common and the cathodes of each row tied in common. The 7 row cathode commons of each character are tied to the constant current sinking outputs of 7 successive stages of the shift register. The like columns of the 4 characters are tied together and brought to a single address pin (i.e., column 1 of all 4 characters is tied to pin 1, etc.). In this way, any diode in the four 5x7 matrices may be addressed by shifting data to the appropriate shift register location and applying a voltage to the appropriate column.

The serial-in-parallel-out (SIPO) shift register has a constant current sinking output associated with each shift register stage. The output stage is a current mirror design with a nominal current gain of 10. The current to the reference diode is established from the output voltage of the brightness input buffer applied across the current reference resistors, R. The reference current flow is controlled by a switching transistor tied to the output of the associated shift register stage. A logical 1 loaded into the shift register will turn the current source "ON" thereby sinking current from the row line. A voltage applied to the appropriate column input will then turn "ON" the desired diode.

Data is loaded serially into the shift register on the high to low transition of the clock line. The data output terminal is a TTL buffer interface to the 28th bit of the shift register (i.e., the 7th row of character 4 in each package). The Data Output is arranged to directly interconnect to the Data Input on a succeeding 4 digit HP HDSP-2000 display package. The Data, Clock and V_B inputs are all buffered to allow direct interface to any TTL or DTL logic family.

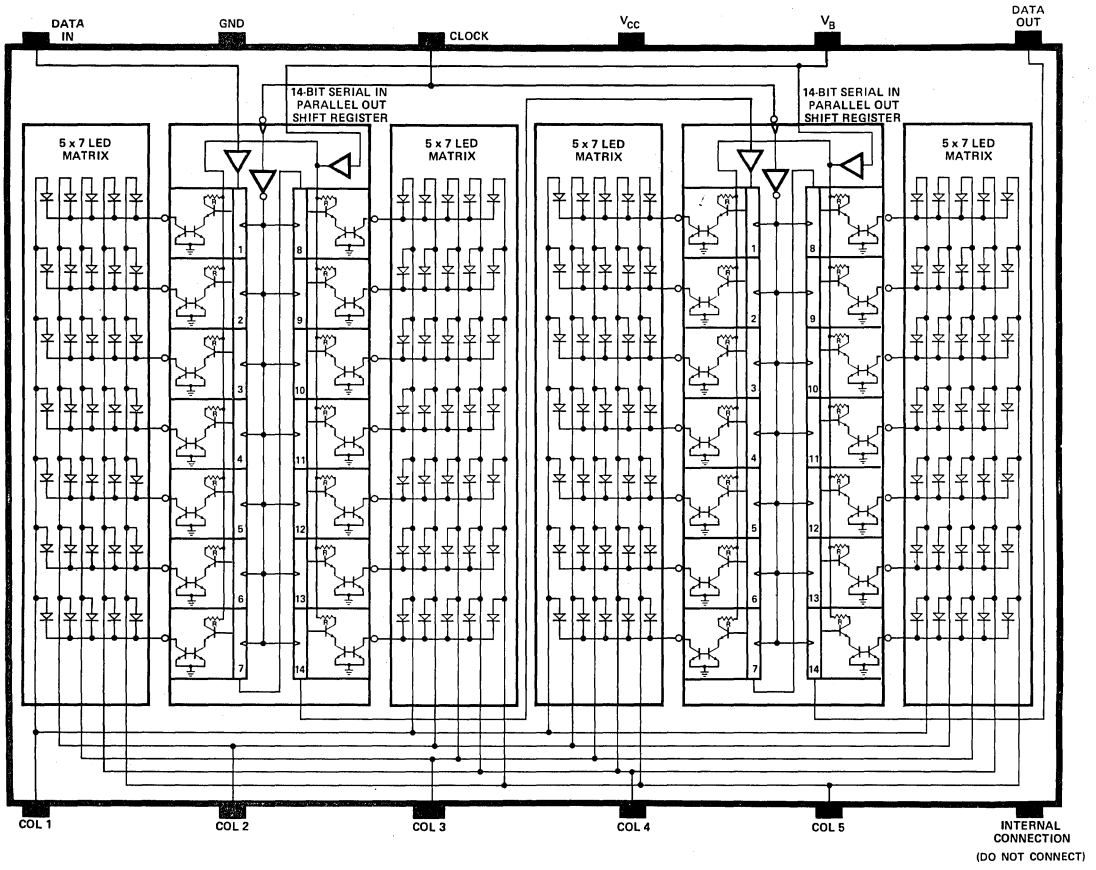


Figure 1. Block Diagram of the HDSP-2000.

THEORY OF OPERATION

Dot matrix alphanumeric display systems generally have a logical organization which prescribes that any character be generated as a combination of several subsets of data. In a 5x7 matrix, this could be either 5 subsets of 7 bits each or 7 subsets of 5 bits each. This technique is utilized to reduce from 35 to 5 or 7 the number of outputs required from the character generator. In order to display a complete character, these subsets of data are then presented sequentially to the appropriate locations of the display matrix. If this process is repeated at a rate which insures that each of the appropriate matrix locations is re-energized, a minimum of 100 times per second, the eye will perceive a continuous image of the entire character. The apparent intensity of each of the display elements will be equal to the intensity of that element during the "ON" period multiplied by the ratio of "ON" time to refresh period. This ratio is referred to as the display duty factor, and the technique is referred to as "strobing". In the case of the HP HDSP-2000, each character is made up of 5 subsets of 7 bits. For a four character display, 28 bits representing the first subset of each of the four characters are loaded serially into the on-board SIPO shift register and the first column is then energized for a period of time, T. This process is then repeated for columns 2 through 5.

If the time required to load the 28 bits into the SIPO shift register is t, then the duty factor is:

$$D.F. = \frac{T}{5(t+T)} \; ; \qquad (1)$$

the term 5(t+T) is then the refresh period. For a satisfactory display, the refresh period should be:

$$1/[5(t+T)] \geq 100 \text{ Hz} \qquad (2)$$

or conversely

$$5(t+T) \leq 10 \text{ msec}, \qquad (3)$$

which gives

$$(t+T) \leq 2 \text{ msec}. \qquad (4)$$

Two milliseconds then is the maximum time period which should be allowed for loading and display of each column location. For $t \ll T$, the duty factor will approach 20%. The number of digits which can be addressed in a single string is then dependent upon the minimum acceptable duty factor and the choice of clock rate. For instance, at 1 MHz clock rate, a 100 character string of 25 packages could be operated at a duty factor of

$$D.F. = \frac{(T+t) - (\text{No. of bits to be loaded}) \times (1/1\ \text{MHz})}{5(T+t)}$$

$$= \frac{(2\ \text{msec}) - (700)\ (1\mu\text{sec})}{5 \times 2\ \text{msec}} = 13\%$$

For most applications, a duty factor of 10% or greater will provide more than satisfactory display intensity. In brightly illuminated ambient environments, a higher duty factor may be desirable whereas, in dim ambient situations, the duty factor may have to be reduced in order to provide a display with satisfactory contrast.

DRIVE CIRCUIT CONCEPTS

A practical display system utilizing the HP HDSP-2000 display requires interfacing with a character generator and refresh memory. A block diagram of such a display system is depicted in Figure 2. In explanation, assume that this system is for a four character display. Therefore, the 1/N counter becomes a 1/4 counter where N is equal to the number of characters in the string. The refresh memory is utilized to store the information to be displayed. Information can be coded in any one of several different standard data codes, such as ASCII or EBDIC, or the code and the display font can be customized through the use of a custom coded ROM. The only requirement is the output data be generated as 5 subsets of 7 bits each. The character generator receives data from the refresh memory and outputs 7 display data bits corresponding to the character and the column select data input. This data is converted to serial format in the parallel to serial shift register for clocking into the HP HDSP-2000 display shift register. In the typical system, the right most character to be displayed is selected first and the data corresponding to the ON and OFF display elements in the fist column is clocked into the first 7 shift register locations of the HP HDSP-2000. In a similar manner, column 1 data for characters 3, 2, and 1 is selected by the 1/N counter, decoded and shifted into the display shift register. After 28 clock counts, data for each character is located in the HP HDSP-2000 shift register locations which are associated with the 7 rows of the appropriate LED matrix. The 1/N counter overflows, triggering the display time counter, enabling the output of the 1/5 column select decoder and disabling the clock input to the HP HDSP-2000. The information now present in the shift registers will be displayed for a period, T, at the column 1 location. At the end of the display period, T, the divide by 5 counter which provides column select data for both the HP HDSP-2000 and the character generator is incremented one count and column 2 data is then loaded and displayed in the same manner as column 1. This process is repeated for each of the 5 columns which comprise the 5 subsets of data necessary to display the desired characters. After the fifth count, the 1/5 decoder automatically resets to one and the sequence is repeated. The only changes required to extend this interface to character strings of more than 4 digits are to increase the size of the refresh memory and to change the divide by four counter to a modulus equal to the number of digits in the desired string.

Since data is loaded for all of the like columns in the display string and these columns are then enabled simultaneously, only five column switch transistors are required regardless of the number of characters in the string. The column switch transistors should be selected to handle approxmately 110mA per character in the display string. The collector emitter saturation voltage characteristics and column voltage supply should be chosen to provide a $2.6V \leqslant V_{COL} \leqslant V_{CC}$. To save on power

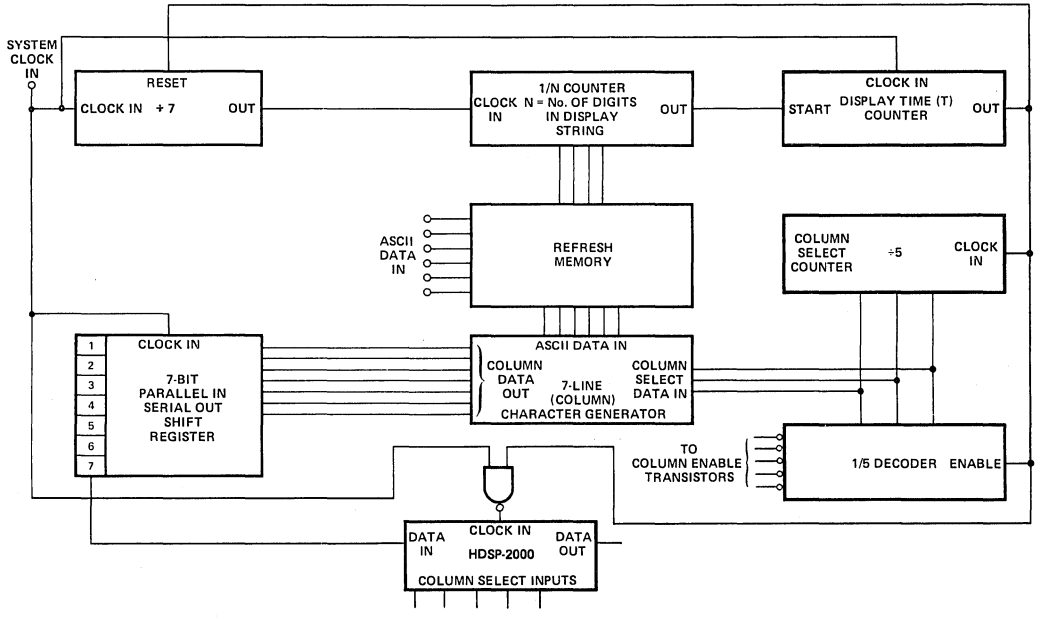


Figure 2. Block Diagram of a Basic Display System.

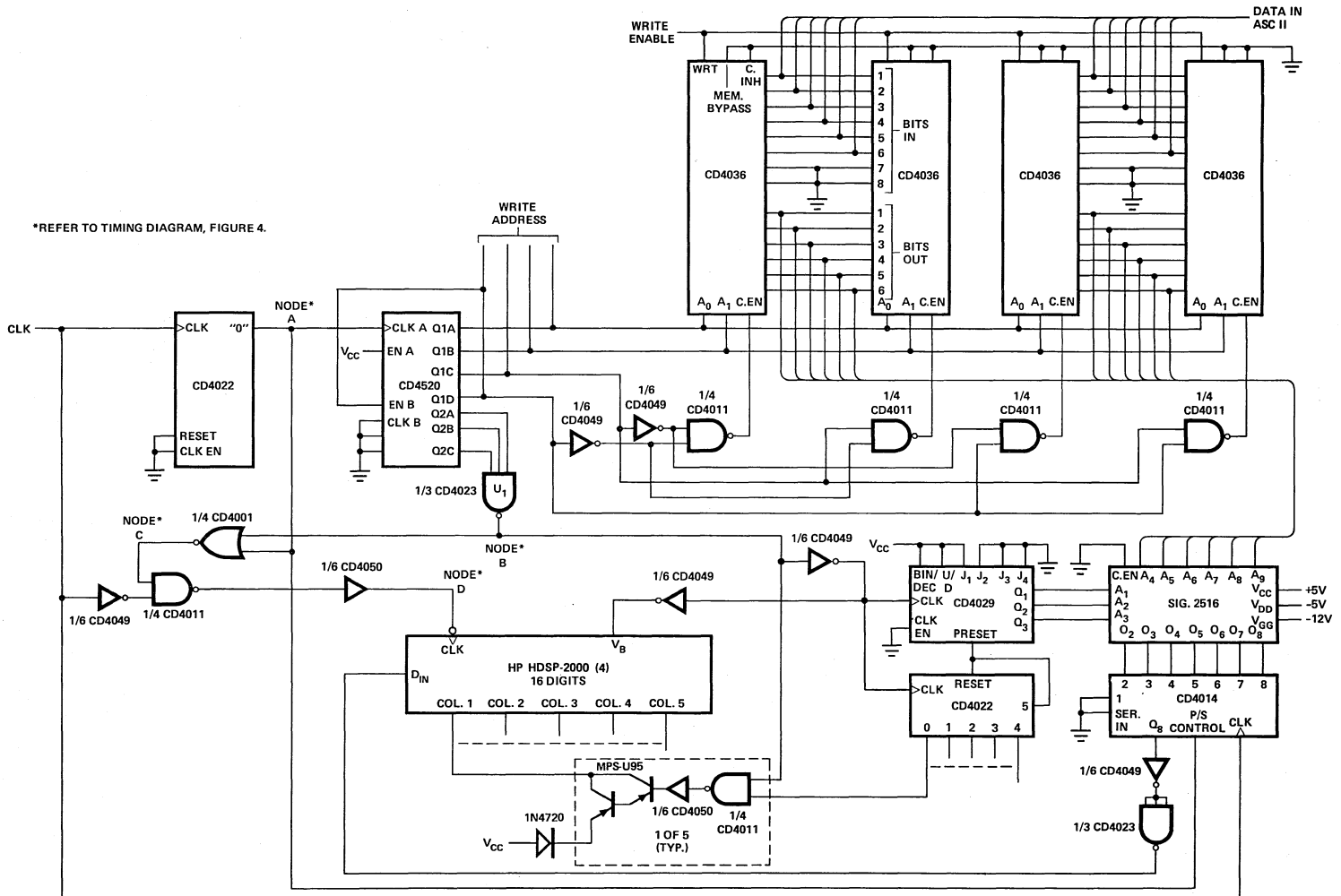


Figure 3. 16 Character CMOS Logic Interface to the HP HDSP-2000.

supply costs and improve efficiency, this supply may be a fullwave rectified unregulated DC voltage as long as the PEAK value does not exceed the value of V_{CC} and the minimum value does not drop below 2.6 volts.

Since large current transients can occur if a column line is enabled during data shifting operations, the most satisfactory operation will be achieved if the column current is switched off before clocking begins. I_{CC} will be reduced by about 10-15% if the clock is held in the logical 1 state during the display period, T.

INTERFACE CIRCUITS FOR THE HP HDSP-2000

There are many possible practical techniques for interfacing to the HP HDSP-2000 alphanumeric display. Three basic approaches will be treated here.

Instrumentation Interface Circuit

The circuit shown in Figure 3 is for a 16 character display and is designed to function primarily as a readout for general instrumentation systems. CMOS logic circuitry is utilized in this design, however, it should be a simple exercise to substitute TTL functions if CMOS is not desired. In this circuit, a CD4022 and CD4520 are combined to perform the functions of the divide by 7, divide by 16 (1/N) and display time counters as depicted in Figure 2. The timing diagram, Figure 4, demonstrates the relationship of the various critical outputs and inputs. The CD4022 actually acts here as a divide by 8 counter with the first count used to latch data into the parallel-in-serial-out (PISO) shift register and the other 7 counts shifting data out of the PISO and into the HP HDSP-2000. The CD4520 is a dual 4 bit counter wired as an 8 bit binary ripple counter. The NAND gate, U_1, establishes the ratio of loading time to display time. In this case, loading will occur once in every 8×2^7 clock counts for a period of 8×2^4 clock counts. Duty factor is then from (1)

$$\text{D.F.} = \frac{(8 \times 2^7) - (8 \times 2^4)}{5\,(8 \times 2^7)} = 17.5\% \quad (1)$$

and the refresh period is

$$5\,(8 \times 2^7)\,\tau,$$

where τ = clock period.

The four least significant bits of the CD4520 counter are used to continually address the CD4036 refresh memory. Data can be written into the desired memory address by strobing the WRITE ENABLE line when the appropriate memory address appears on the WRITE ADDRESS lines. This function can occur simultaneously with a read from memory.

Two counters, a CD4029 and a CD4022, are used for the column data generator and the column select decoder, respectively. Note that the Signetics 2516 character generator requires column select inputs of binary codes 1 to 5 instead of binary 0 to 4. For this reason, the CD4029 is preset to a binary 1 by the same pulse which is used to reset the CD4022 column select decoder. To minimize I_{CC}, the V_B terminal is held low during data load operations, turning "OFF" the current mirror reference current. The column current switch is a PNP Darlington transistor driven from a buffered NAND gate. The 1N4720 serves to reduce the column voltage by approximately 1 volt, thereby reducing on board power dissipation in the HP HDSP-2000 devices. Due to maximum clock rate limitations of the CMOS logic, clock input should not exceed 1 MHz.

32 Character Keyboard Interface Circuit

The circuit shown in Figure 5 will directly interface the HP HDSP-2000 display to most standard keyboards. Interfac-

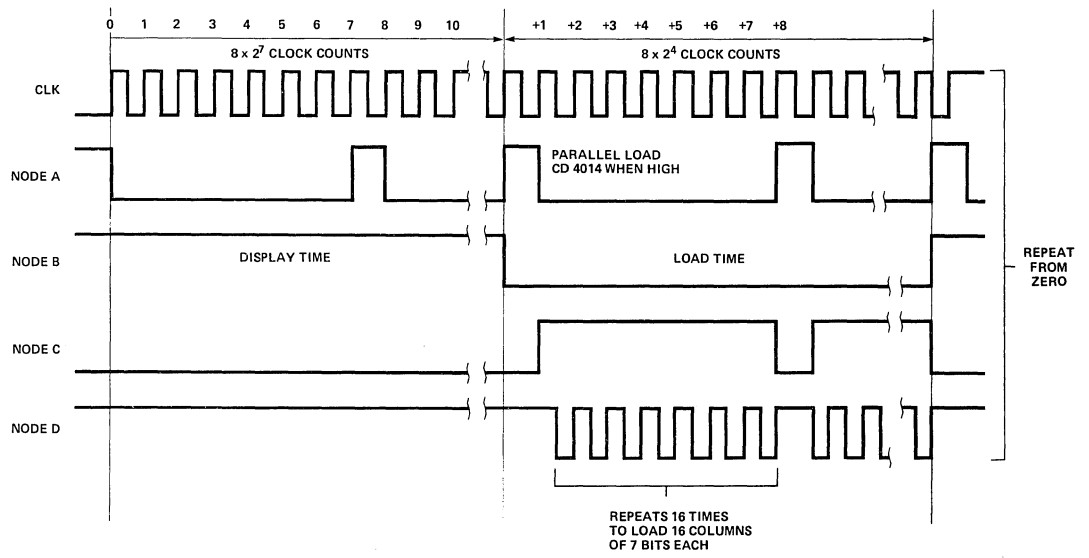


Figure 4. Timing Diagram for Display Interface.

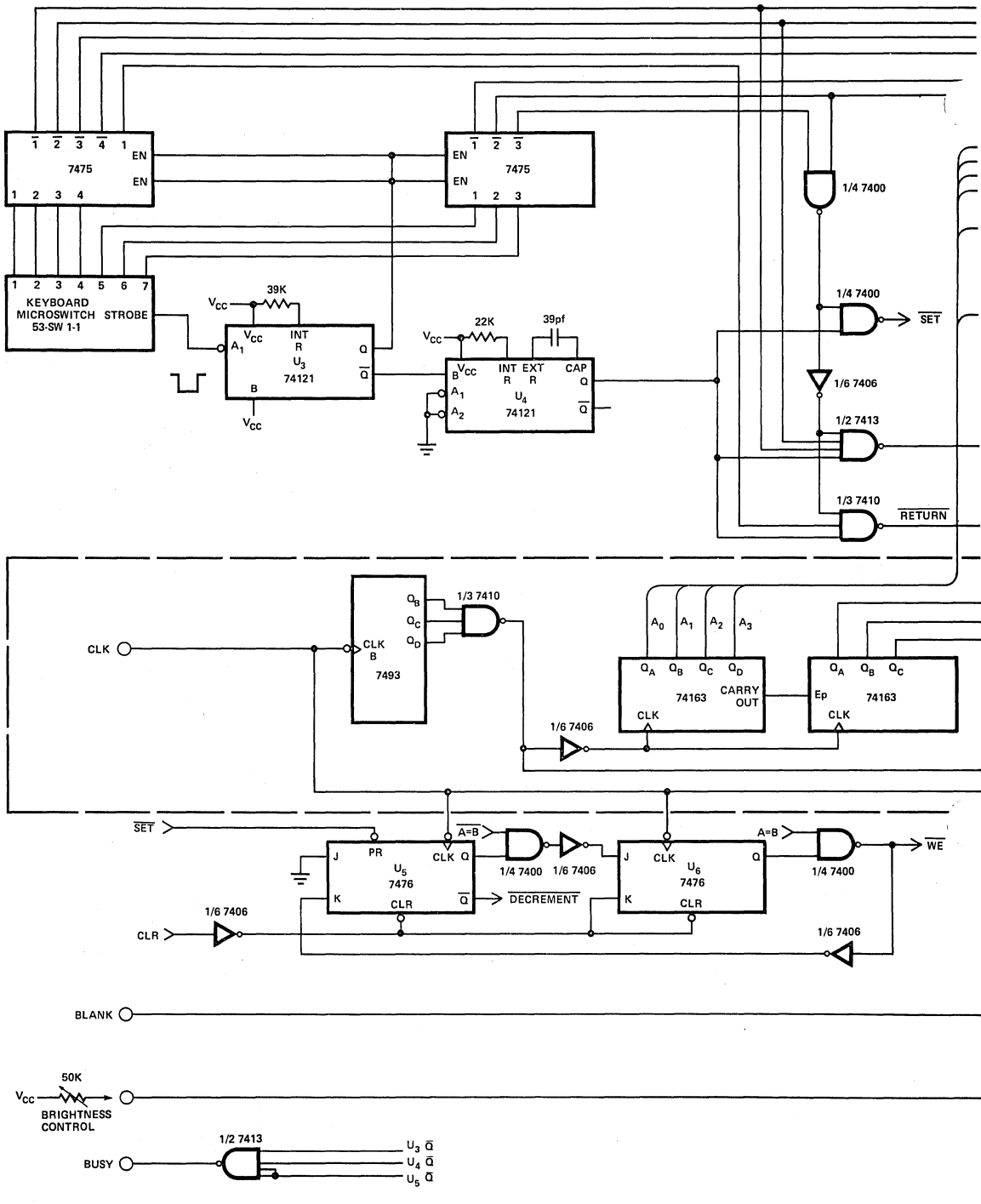
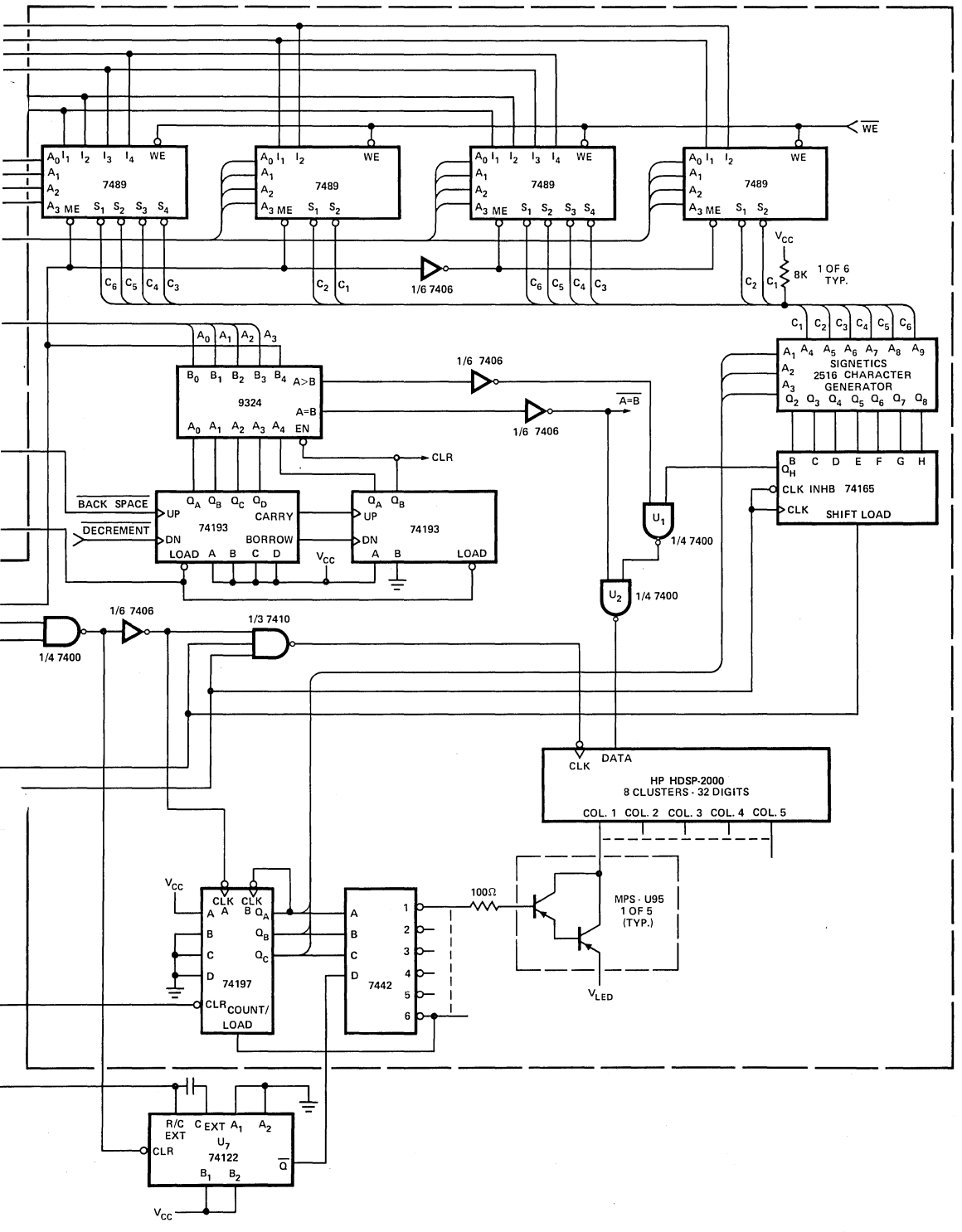


Figure 5. 32 Character Keyboard Interface Circuit.


7489
WE
1/6 7406
1 OF 6 TYP.
8K
9324
A>B
A=B
EN
CLR
BACK SPACE
DECREMENT
74193
UP
DN
CARRY
BORROW
LOAD
SIGNETICS 2516 CHARACTER GENERATOR
74165
CLK INHB
SHIFT LOAD
1/4 7400
1/3 7410
HP HDSP-2000
8 CLUSTERS - 32 DIGITS
COL. 1 COL. 2 COL. 3 COL. 4 COL. 5
DATA
74197
COUNT/ LOAD
7442
100Ω
MPS - U95
1 OF 5
(TYP.)
74122
R/C EXT
C EXT
V_{CC}
V_{LED}

ing to a keyboard without a "smart" system to generate some of the special functions required can result in some unique problems which must be considered. This system provides the following special features:

- Provides a cursor to indicate the position in the line of the next character to be entered.
- Blanks all data to the right of the cursor in the display.
- Provides for external display blanking and intensity control.
- Implements "Return" and "Backspace" functions.

The timing and data scan portions of this circuit are similar to those of the circuit shown in Figure 3 and will not be reviewed in detail. These portions of the circuit are enclosed in the dashed line. The major addition to the circuit which allows simple implementation of the special functions is a position counter and comparator. The position counter is an up-down counter which is preset to n-1 (n = number of characters in the display string) by "RETURN". The counter is decremented for each keystroke representing a valid display character and incremented for a "BACKSPACE" input code. A Fairchild 9324 five bit comparator compares the position counter output to the memory scan address. The memory scan begins at zero and represents the data for the right most (32nd) character in the display. The position count is indicative of the number of character keystrokes which have decremented the position counter from 31. The comparator senses two conditions of the relative values of the two counters. For memory scan equal to position count, the A=B output of the comparator will be a logical "1". For all other conditions of the two counters, A=B is a logical "0". This signal is inverted and is used to gate data from the PISO via U_1 into the HP HDSP-2000. For the condition A=B, the gating input is a logical "0" and the output of NAND gate U_2 is therefore held at a logical "1". This will cause all of the diodes associated with the character position A=B to be illuminated, thus forming the "cursor". The second condition which is sensed by the comparator is for a memory scan count less than position count, (A>B). This condition represents all character data to the right of the cursor and results in a logical "1" at the "A>B" output of the comparator. It is normally desirable for these characters to blank, hence a logical "0" should be loaded into the corresponding HP HDSP-2000 shift register locations. This is implemented by inverting the "A>B" output and applying the resulting signal to one input of NAND gate, U_1. For "A>B" at a logical "1", the output of U_1 will be a logical "1". This signal will then be inverted by U_2, causing logical "0" data to be loaded into the HP HDSP-2000 shift register for all characters to the right of the cursor. For "A=B" and "A<B", U_1 will pass inverted data from the PISO to U_2. These comparator signals are also used to control the loading of data into the proper refresh memory location. Keyboard data is initially stored in the 7475 D latches using the keyboard "STROBE" signal to trigger a one shot clock pulse from U_3. This pulse triggers a second one shot, U_4, which gates a "SET" signal to the load control flip flops, U_5 and U_6, for any valid character code. This arms the load control so that a write enable pulse will be sent to the 7489 RAM as soon as "A=B". The "$\overline{A=B}$" signal is used to prevent a second data entry from occurring during the middle of a write pulse. The write pulse also clears the load control flip-flops on the next clock cycle so that a new arriving signal can be recognized. The $\overline{Q}$ output of U_5 is also used to decrement the position counter.

The other special functions which are added to the circuit of Figure 3 are an intensity control and a blanking input. Intensity control is realized through the 74122 retriggerable monostable multivibrator, U_7. This circuit controls the time that the column select decoder is enabled during the display time, T. The display is externally blanked by holding the "RESET" input of the column select counter at a logical "0".

The circuit shown in Figure 5 is also convenient for use in instrumentation and computer readouts. In this situation, a "Busy" signal composed of $\overline{Q}$-U_2, $\overline{Q}$-U_3 and $\overline{Q}$-U_4 will allow the display interface to indicate to the driving system when data can be accepted.

Remote Display-Interface

In many systems, it is desirable to display data at multiple remote locations without having to provide the relatively complex and expensive decoding and timing scheme depicted in the previous two examples. This type of application may most often be utilized in paging system readouts, remote message displays and other systems where multiple displays would be addressed from a single central processor. The circuit shown in Figure 6 is designed to store and display a string of decoded data. The circuit requires data input from a system which can generate and serially output display and column select data — for instance, a minicomputer or microprocessor. The total number of bits of storage required (including the HP HDSP-2000 and the 5 bit column select shift register) is:

$$\text{Storage} = 35\,N + 25. \qquad (5)$$

where N = the number of characters in the display string.

The data input format should be divided into 5 equal subsets of information. Each subset should contain all of the data required to completely load the HP HDSP-2000 display string shift register (7N bits) for a given column, preceeded by a 5-bit column select code which will be shifted into the 5-bit SIPO at the HP HDSP-2000 output. The circuit has been designed to operate from two different clocks. This is important in systems where the display may be radio link addressed with the DATA ENTRY CLOCK being reconstituted from the data stream. For loading, $\overline{\text{LOAD DATA}}$ is taken low and loading can commence after $\overline{\text{READY}}$ goes low. Data is entered into the shift register through a gated input. The data string must contain the proper number of bits as defined by (5) and should be loaded in the shift register with one of the 5-bit column select codes loaded fully in the column select SIPO shift register. After loading is complete, $\overline{\text{LOAD DATA}}$ is returned high and clocking will be controlled by the DISPLAY CLOCK. The display clocking is designed to shift the stored data by 7N + 5 bits and then stop and display the shift-register contents for a period of time, T, as defined by the period of the one shot, U_1. U_1 is triggered when the clock line goes low after the synchronous counter has counted to 7N + 5. The output of U_1 resets the counter and disables the counting until the end of the period, T. The D flip-flop, U_2, insures that clock pulses to

the shift registers always start synchronous with the beginning of a full clock cycle so that erroneous clocking will not occur. U_3 is utilized to give intensity control for the HP HDSP-2000, if desired. It can be overridden by connecting the $U_{4(1-5)}$ input to the Q output of U_1 instead of U_3.

The shift register memory utilized in this circuit is only one of several forms of memory which could be chosen. Another possibility would be the use of a 512 x 1 bit or 1024 x 1 bit RAM. The counter outputs would then be used to select the RAM address.

POWER DISSIPATION/JUNCTION TEMPERATURE CALCULATIONS

The HP HDSP-2000 combines a significant amount of logic and display capability in a very small package. As such, on board power dissipation is relatively high and thermal design of the display mounting becomes an important consideration. The HP HDSP-2000 is designed to permit operation over a wide range of temperature and supply voltages. Full power operation at $T_A = 25°C$ (with $V_{CC} = V_B = V_{COL} = 5.25V$) is acceptable if the thermal resistance from pins to ambient, θ_{CA}, is no greater than 35° C/watt/cluster. This value assumes that the mounting surface of the display becomes an isothermal plane. If only one display is operated on this isothermal plane at 1.7 watts maximum, then the temperature raise above ambient is:

$$T_{RISE} = [35°C/watt] \times 1.7 \text{ watts} = 42.5°C. \quad (6)$$

If a second display is placed on this same thermal plane, with no increase in thermal dissipation capability the temperature would be doubled (i.e., 85° C) — reaching catastrophic levels very quickly. However, in most applications maximum achievable power dissipation is considerably less than the maximum allowable package dissipation of 1.7W. Calculation of power dissipation in the HP HDSP-2000 can be made using the following formula:

$$P_D = P(I_{CC}) + P(I_{REF}) + P(I_{COL}) \quad (7)$$

where

$$P(I_{CC}) = I_{CC} (V_B = 0.4V) \times V_{CC} \quad (8)$$

$$P(I_{REF}) = [I_{CC} (V_B = 2.4V) - I_{CC} (V_B = 0.4V)] \times V_{CC} \times (n/35) \times 5 \times D.F. \quad (9)$$

$$P(I_{COL}) = I_{COL} \times V_{COL} \times (n/35) \times 5 \times D.F. \quad (10)$$

where

I_{CC} is measured with all S.R. stages equal to logical 1.
n = average number of diodes illuminated per character.
D.F. = Column On Time from equation (1) or the Column On Time due to pulse width modulation of V_B, whichever is lower.

As can be seen from formulas (8), (9) and (10), there are several techniques by which total power dissipation can be derated:

- Lower V_{CC} to minimum
- Lower V_{COL} to minimum
- Lower D.F.

Maximum and typical power dissipation can be calculated from the maximum and typical values of I_{CC} and I_{COL} published in the HP HDSP-2000 data sheet. While it is possible to operate the columns of the HDSP-2000 display using fullwave rectified unregulated DC, lower power dissipation can be achieved by using the regulated V_{CC} supply. Then, V_{COL} is equal to V_{CC} minus the collector to emitter saturation voltage across the column switching

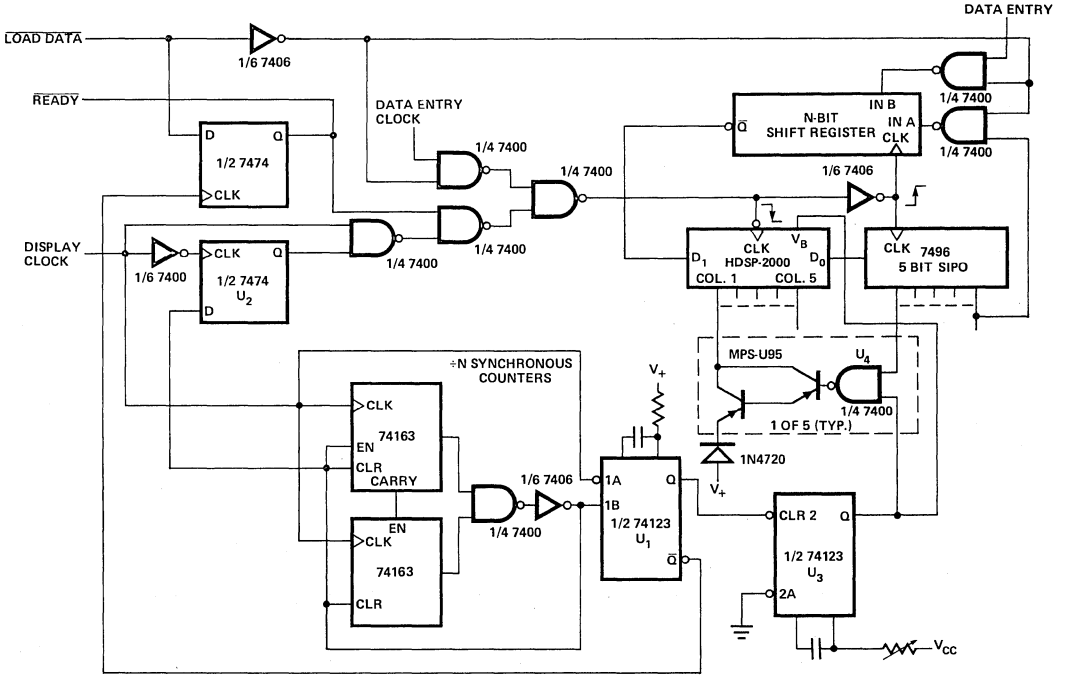


Figure 6. Display Interface Designed to Accept Decoded Data.

transistors. Since the minimum recommended V_{COL} is 2.6V, PNP Darlington transistors with a silicon diode in series with the emitter can be used to lower the power dissipation within the display. In most implementations of the ASCII character set the maximum number of diodes illuminated within a display character, n, is 21 while a typical character has 15 dots illuminated. While the maximum D.F. is 20%, in most applications D.F. ≤ 17.5% due to the required time to load the display. A D.F. of 17.5% represents a (7/8) ratio of display time to total time such as illustrated in the circuit shown in Figure 3. Many applications achieve a D.F. much lower than 17.5%. For example, the HDSP-2470 alphanumeric display system when configured for 40 characters has a D.F. of 11.6%.

As an example, the maximum power dissipation can be calculated for the circuit shown in Figure 3. In this circuit $V_{COL(MAX)}$ = 5.25V − 1.3V (MPS-U95 @ 1.6A) − .85V (1N4720 @ 1.6A) = 3.10V. Thus maximum achievable power dissipation can be calculated as shown below:

$$P(I_{CC}) = 60mA \times 5.25V = 315\ mW \quad (11)$$

$$P(I_{REF}) = (95mA - 60mA) \times 5.25V \times (21/35) \times 5 \times 0.175 = 96.5\ mW \quad (12)$$

$$P(I_{COL}) = 410mA \times 3.1V \times (21/35) \times 5 \times 0.175 = 667\ mW \quad (13)$$

$$P_D = P(I_{CC}) + P(I_{REF}) + P(I_{COL}) = 1079\ mW \quad (14)$$

Similarly, typical power dissipation can be calculated as:

$$P(I_{CC}) = 45mA \times 5.00V = 225\ mW \quad (15)$$

$$P(I_{REF}) = (73mA - 45mA) \times 5.00V \times (15/35) \times 5 \times 0.175 = 52.5\ mW \quad (16)$$

$$P(I_{COL}) = 335mA \times (5.00V - 1.3V - .85V) \times (15/35) \times 5 \times 0.175 = 358\ mW \quad (17)$$

$$P_D = P(I_{CC}) + P(I_{REF}) + P(I_{COL}) = 636\ mW \quad (18)$$

For operation at the maximum temperature of 70° C, it is important that the following criteria be met:

a. $T_{CASE} \leq 100°C$, where T_{CASE} = hottest pin temperature

b. $T_{IC\ JUNCTION} \leq 125°C$

Thermal resistance from junction to case, θ_{JC}, is typically 25° C/watt. Using these factors, it is possible to determine the required heat sink power dissipation capability and associated power derating through the following assumptions:

$$T_{IC\ JUNCTION} = (\theta_{CA} \times P_D) + \theta_{JC}\left(\frac{P_D - .015n}{2}\right) \quad (19)$$

$$T_{CASE} = (\theta_{CA})\ P_D \quad (20)$$

where $\left(\frac{P_D - .015n}{2}\right)$ is the power dissipated in each IC.

HEAT SINKING CONSIDERATIONS

In practice, heat sink design for the HP HDSP-2000 involves optimization of techniques to dissipate heat through the device leads. Figures 7 and 8 schematically depict two possible heat sink designs. In many applications, a maximum metalized printed circuit board such as shown in Figure 7 can provide adequate heat sinking for the HDSP-2000 display. For example, the HDSP-2416/-2424/-2432/-2440 display boards consist of a 16, 24, 32 or 40 character HDSP-2000 display mounted on a maximum metalized printed circuit board. These display boards are designed for free air operation to 55° C and operation to 70° C with forced air cooling of 150 fpm normal to the component side of the board. A free air operating temperature of 70° C can be achieved by heat sinking the display. Figure 8 depicts a two part heat sink which can be assembled using two different extruded

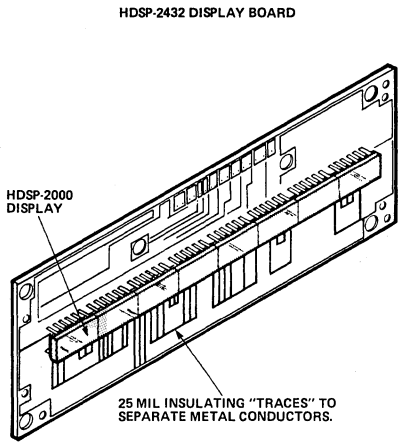


Figure 7. Maximum Metalized Printed Circuit for the HP HDSP-2000.

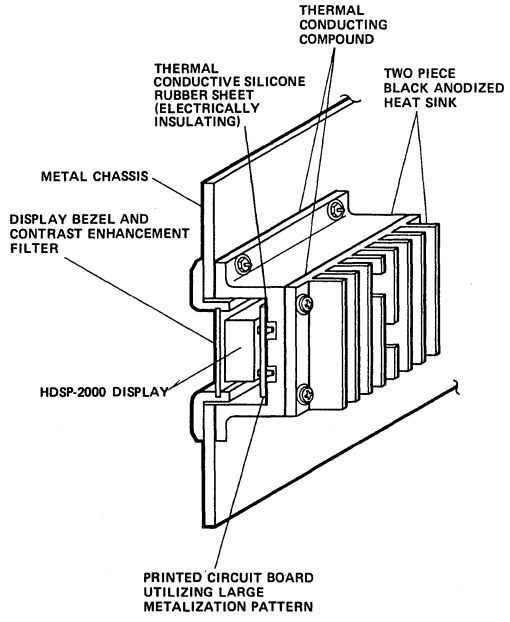


Figure 8. Two-Part Heat Sink for the HP HDSP-2000.

parts. In this design, the vertical fins promote heat transfer due to naturally induced convection. Care should be taken to insure a good thermal path between the two portions of the heat sink. To optimize power handling capability, the metal heat transfer contact area between the PCB metalization and the heat sink should be maximized. A surface area of approximately 8 square inches per cluster will permit operation at 1.1 watts/cluster at the maximum operating temperature of 70°C ambient. The value of 1.1 watts/cluster is easily achieved by reduction of V_{COL} to 3 volts. Next to increasing total heat sink area, a provision for at least some forced air flow is probably the most effective means of improving heat transfer. Thermal design for the HP HDSP-2000 must be carefully considered as operation at excess temperatures can lead to premature failure.

The HP HDSP-2000 displays may also be mounted in standard DIP sockets which are cut down to accept the 6 pin devices in end-to-end strings. Another alternative for socket mounting is the stripline socket such as the Augat 325-AG1D or AMP 583773. These sockets will allow enough space bewteen the PCB and the HP HDSP-2000 to permit a heat sink bar to be inserted to conduct heat to an external sink. Most sockets add a thermal resistance of about 2° C/watt bewteen the device leads and the PCB.

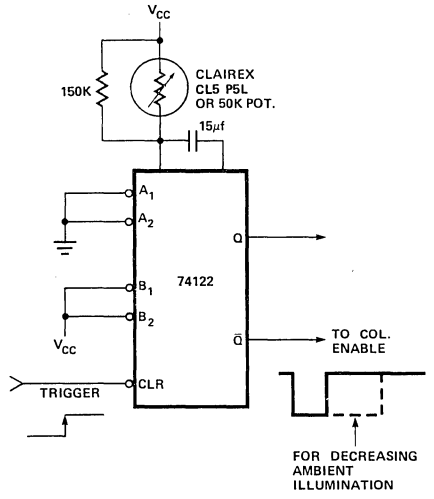


Figure 9. Intensity Modulation Control Using a One Shot Multivibrator.

DISPLAY INTENSITY MATCHING AND CONTROL

The luminous intensity of LED displays in general has a fairly wide dynamic range. If there is too great a difference between the luminous intensity of adjacent characters in the display string, the display will appear objectionable to the viewer. To solve the problem, the HP HDSP-2000 displays are categorized for luminous intensity. The category of each display package is indicated by a letter preceding the date code on the package. When assembling display strings, all packages in the string should have the same intensity category. This will insure satisfactory intensity matching of the characters. The HP HDSP-2000 displays are categorized in 8 overlapping intensity categories. All characters of all packages designated to be within a given letter category will fall within an intensity ratio of less than 2:1. For dot matrix displays, a character-to-character intensity ratio of 2:1 is not generally discernable to the human eye.

A more important consideration regarding display intensity is the control of the intensity with respect to the ambient lighting level. In dim ambients, a very bright display will produce very rapid viewer fatigue. Conversely, in bright ambient situations, a dim display will be difficult, if not impossible, to read and will also produce viewer fatigue and high error rates. For this reason, control of display intensity with respect to the environment ambient intensity is an important consideration. Figure 9 depicts a scheme which will automatically control display intensity as a function of ambient intensity. This circuit utilizes a resettable one shot multivibrator which is triggered by the column enable pulse. The duration of the multivibrator output is controlled by a photoconductor. At the end of a column enable pulse, the multivibrator is reset to insure that column current is off prior to the initiation of a new display shift register loading sequence. The output of this circuit is used to modulate either the V_B inputs of the HP HDSP-2000 displays or the column enable input circuitry. For maximum reduction in display power, both inputs should be modulated.

In the circuit shown in Figure 9, the photocell may be replaced by a 50K potentiometer to allow manual control of display intensity.

Contrast Enhancement

Another important consideration for optimum display appearance and readablity is the contrast between the display "ON" elements and the background. High contrast can be achieved by merely driving the highest possible power into the display. This, of course, is feasible in some situations as long as ambient lighting is not too intense and power dissipation is not a consideration. A much more practical technique is the use of an effective contrast enhancement filter material. The following materials, Panelgraphic Ruby Red 60 and Dark Red 63 or SGL Homalite H100-1605 and H100-1670 will all provide improved contrast for the HP HDSP-2000 display. Other good practices to enhance display contrast are to avoid PCB traces in the visible areas around the display and, if possible, the utilization of a black silk screen over the relatively light PCB areas around the display. The subject of contrast enhancement is treated in greater detail in HP Application Note 964. Microprocessor interfaces to the HDSP-2000 display are shown in HP Application Note 1001.

KEY POINTS REGARDING THE HP HDSP-2000:

- A logical "1" in the display shift register turns a corresponding LED "ON".
- Clocking occurs on the high to low transition of the clock input.
- A character generator which produces 7 bit "COLUMN" data should be utilized.
- The internal shift register is 28 bits in length.
- Each column should be refreshed at a minimum rate of 100 Hz.

The following is a list of commercially available character generators which can be used in conjunction with the HP HDSP-2000. These devices are all programmed to convert from ASCII input code to 5 sets of 7 bits each for a 5 x 7 display format. Any desired input-output coding can be utilized in custom programmed ROMs.

Manufacturer	Part Number	Typical Access Time	Required Power Supplies	Typical Power Dissipation
Texas Instruments	TMS 4100	500 nsec	±12V	450 mW
National	5241 ABL	700 nsec	±12V	
Signetics	2513	450 nsec	±5V −12V	290 mW
	2516	500 nsec	±5V −12V	280 mW
AMI	S8773B	450 nsec	+5V −12V	625 mW (max)
Mostek	2002 2302		±14V +5V −12V	320 mW 200 mW
Electronic Arrays	40105	750 nsec	±12V	430 mW
Fairchild	3257	500 nsec	+5V −12V	360 mW

Figure 10. Column Output Character Generators Suitable for Use with the HP HDSP-2000.

The refresh memory for the HP HDSP-2000 display can take any one of several different forms. The following table lists a few of the devices which the display system designer may find convenient.

Type	Organization
Bipolar RAM	Words x Bits
*7489	16 x 4
*7481A	16 x 1
*7484A	16 x 1
Fairchild 93403	16 x 4
Intel 3101	16 x 4
Intel 3104	4 x 4
MOS RAM	
TI TMS 4000 JC/NC	16 x 8
CMOS RAM	
RCA CD 4036	4 x 8
RCA CD 4039	4 x 8
National 74C89	16 x 4
Motorola MCM 4064	16 x 4
Shift Register	
TI TMS 3112	32 x 6
Signetics 2518	32 x 6
Signetics 2519	40 x 6
Fairchild 3348	32 x 6
Fairchild 3349	32 x 6

*Standard 7400 Series TTL logic parts available from most Integrated Circuits manufacturers.

Figure 11. Memory Elements Which can be Utilized in HDSP-2000 Display Systems.

HEWLETT hp PACKARD

COMPONENTS

NEW PRODUCT APPLICATION

APPLICATION NOTE 1000

Digital Data Transmission With the HP Fiber Optic System

Fiber optics can provide solutions to many data transmission system design problems. The purpose of this application note is to aid designers in obtaining optimal benefits from this relatively new technology. Following a brief review of the merits, as well as the limitations, of fiber optics relative to other media, there is a description of the optical, mechanical, and electrical fundamentals of fiber optic data transmission system design. How these fundamentals apply is seen in the detailed description of the Hewlett-Packard system. The remainder of the note deals with techniques recommended for operation and maintenance of the Hewlett-Packard system, with particular attention given to deriving maximum benefit from the unique features it provides.

ELECTRICAL WIRE VS. FIBER OPTICS

In fiber optic cables, the signals are transmitted in the form of energy packets (photons) which have no electrical charge. Consequently, it is physically impossible for high electric fields (lightning, high-voltage, etc.) or large magnetic fields (heavy electrical machinery, transformers, cyclotrons, etc.) to affect the transmission. Although there can be a slight leakage of flux from an optical fiber, shielding is easily done with an opaque jacket, so signal-bearing fibers cannot interfere with each other or with the most sensitive electric circuits, and the optically-transmitted information is, therefore, secure from external detection. In some applications, optical fibers carry signals large enough to be energetically useful (e.g., for photocoagulation) and potentially harmful, but in most data communication applications, economy dictates the use of flux levels of 100μW or less. Such levels are radiologically safe and in the event of a broken or damaged cable, the escaping flux is harmless in explosive environments where a spark from a broken wire could be disastrous. Jacketed fiber optic cables can tolerate more mechanical abuse (crush, impact, flexure) than electrical cables of comparable size; moreover, fiber optic cables have an enormous weight and size advantage — for equivalent information capacity. Properly cabled optical fibers can tolerate any kind of weather and can, without ill-effect, be immersed in most fluids, including polluted air and water.

Bandwidth considerations clearly give the advantage to fiber optics. In either parallel- or coaxial-wire cable, the bandwidth varies inversely as the square of the length, while in fiber optic cable it varies inversely as only the FIRST power of the length. Here are some typical values for length, ℓ , in metres:

(1) $f_{3dB} = \frac{12{,}000}{\ell}$ MHz for HFBR-3001 to 3005 cables

(2) $f_{3dB} = \frac{225{,}000}{\ell^2}$ MHz for typical 50Ω coax (RG-59)

For example, if ℓ = 100m, the 3dB frequency is only 22.5MHz for the coax cable, but for the fiber optic cable it is 120MHz.

The limitations of fiber optics arise mainly from the means for producing the optical flux and from flux losses. While the power into a wire cable can easily and inexpensively be made several watts, the flux into a fiber optic cable is typically much less than a milliwatt. Wire cable may have several signal "taps"; multiple taps on fiber optic cables are economically impractical at present.

The losses in a point-to-point fiber optic system are insertion loss at the input and output, connector loss, and transmission loss proportional to cable length. Variations in these losses require a receiver with a dynamic range capable of accommodating these variations and yet able to provide adequate BW (bandwidth) and SNR (signal-to noise) ratio at the lowest flux level. Fortunately, no noise is picked up by a fiber optic cable so the receiver SNR at any BW is limited only by the noise produced within the receiver.

Fiber optics is not the best solution to every data transmission problem; but where safety, security, durability, electrical isolation, noise immunity, size, weight, and bandwidth are paramount, it has a clear advantage over wire.

FIBER OPTIC FUNDAMENTALS

Flux coupled into an optical fiber is largely prevented from escaping through the wall by being re-directed toward the center of the fiber. The basis for such re-direction is the index of refraction, n_1, of the core relative to the index of refraction, n_2, of the cladding.

Index of refraction is defined as the ratio of the velocity of light in a given medium to the velocity of light in a vacuum.

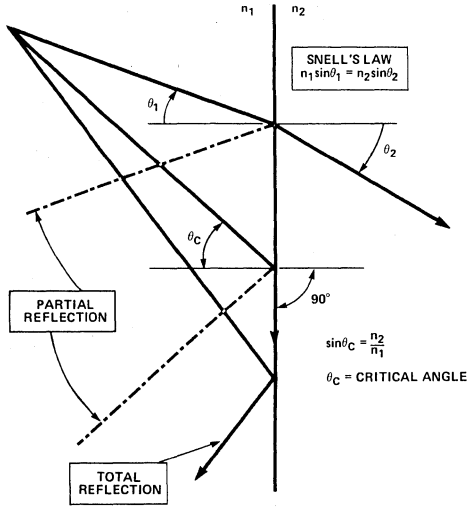


Figure 1. Snell's Law.

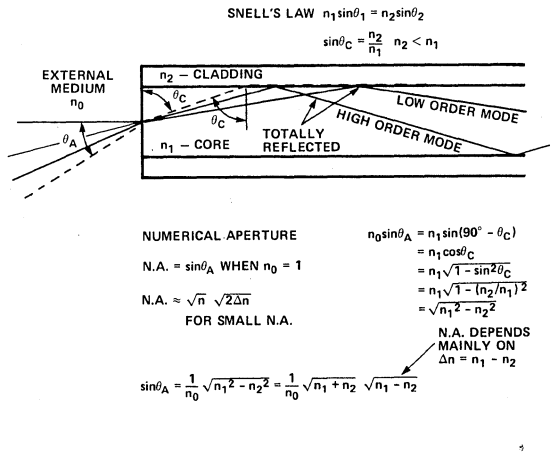


Figure 2. Total Internal Reflection.

As a ray of light passes from one medium into another of a different index of refraction, the direction changes according to Snell's Law:

(3) $n_1 \sin\theta_1 = n_2 \sin\theta_2$ SNELL'S LAW

This is illustrated in Figure 1. Notice that the relationship between the angles is the same, whether the ray is incident from the high-index side (n_1) or low-index side (n_2). For rays incident from the high-index side, there is a particular incidence angle for which the exit angle is ninety degrees. This is called the critical angle. At incidence angles less than the critical angle, there is only a partial reflection, but for angles greater than the critical angle, the ray is totally reflected. This phenomenon is called TOTAL INTERNAL REFLECTION (TIR).

Numerical Aperture.

Rays within the core of an optical fiber may be incident at various angles, but TIR applies only to those rays which are incident at angles greater than the critical angle. TIR prevents these rays from leaving the core until they reach the far end of the fiber. Figure 2 shows how the reflection angle at the core/cladding interface is related to the angle at which a ray enters the face of the fiber. The acceptance angle, θ_A, is the maximum angle, with respect to the fiber axis, at which an entering ray will experience TIR. With respect to the index of refraction, n_0, of the external medium, the acceptance angle is related to the indices of refraction of the core and cladding. When the external medium is air ($n_0 \approx 1$), the sine of the acceptance angle is called the NUMERICAL APERTURE (N.A.) of the fiber:

(4) NUMERICAL APERTURE, N.A. = $\sin\theta_A$

The derivation in Figure 2 applies only to meridional rays, i.e., rays passing through the axis of the fiber; skew rays (non-meridional) can also be transmitted, and these account for the observation that the reception and radiation patterns of optical fibers are not perfect step functions at the acceptance angle. For this reason, the practical definition of N.A. is somewhat arbitrary.

Modes of Propagation

Within the limits imposed by the N.A., rays may propagate at various angles. Those propagating at small angles with respect to the fiber axis are called LOW-ORDER MODES, and those propagating at larger angles are called HIGH-ORDER MODES. These modes do not exist as a continuum. At any given wavelength, there are a number of discrete angles where propagation occurs. SINGLE-MODE fibers result when the core area and the N.A. are so small that only one mode can propagate.

In addition to high- and low-order modes, there are others, called LEAKY MODES, which are trapped as skew rays — partly in the core, but mostly in the cladding where they are called CLADDING MODES. As implied by the term, leaky modes do not propagate as well as the more nearly meridional modes; their persistence, depending mainly on the structure of the optical fiber, ranges from less than a metre to more than fifty metres. The presence of leaky modes will, of course, affect the results obtained in measurement of N.A. and transmission loss, making them both artificially high. For this reason, N.A. is usually specified in terms of the EXIT N.A. for a fiber of length adequate to assure that leaky modes have effectively disappeared.

Since most leaky mode propagation is in the cladding, it can be "stripped." Such cladding mode stripping is done by surrounding the unjacketed fiber with a material having a refractive index higher than that of the cladding. EXIT N.A. is defined as the sine of the angle at which the radiation pattern (relative intensity vs. off-axis angle) has a particular value. This value is usually taken at 10% of the axial (maximum) value.

Transmission Loss

Regular core (non-leaky) modes also exhibit transmission losses. These are due to (1) scattering by foreign matter, (2) molecular (material) absorption, (3) irregularities at the core/cladding interface, and (4) microbending of the optical fiber by the cable structure. The first two loss mechanisms depend on the length of path taken by a ray; the third depends on the number of reflections of the ray before it emerges. It is clear from Figure 2 that the higher order modes have longer paths and more reflections with consequently higher loss. Larger N.A. fibers permit higher-order-mode propagation and, therefore, exhibit generally a higher transmission loss. Transmission loss is exponential and is, therefore, usually expressed in "dB per km." Coupling loss consideration usually favors larger N.A.

The three main loss mechanisms for coupling between fibers or between fibers and the optical ports of other devices are: (1) relative N.A.'s, (2) relative area of the optical ports, and (3) Fresnel (reflection) loss. In addition to these, there may be coupling loss due to misalignment and/or separation of optical ports. Relative N.A. loss can be ignored (≈ zero dB) whenever the N.A. of the receiving port (fiber or detector) is larger than the N.A. of the source port (flux generator or fiber), otherwise:

$$(5)\ \text{N.A. LOSS (dB)} = 20 \log \frac{\text{N.A. of Source Port}}{\text{N.A. of Receiver Port}}$$

Relative area loss can be ignored whenever the area of the receiver port is larger than the area of the source port, otherwise:

$$(6)\ \text{AREA LOSS (dB)} = 20 \log \frac{\text{Diameter of Source}}{\text{Diameter of Receiver}}$$

In applying equation (6) to coupling between single fibers, the diameter to be used is the CORE DIAMETER. If the receiver port is a FIBER OPTIC BUNDLE, the "packing fraction" loss must be added to the area loss, even when the area of the bundle is larger than the area of the source port.

$$(7)\ \text{PACKING FRACTION LOSS (dB)} = 10 \log \frac{\text{Active Area}}{\text{Total Area}}$$

"Active area" is the sum of areas of the cores of individual fibers, and "total" area is that of the bundle.

Fresnel loss occurs when a ray passes from one medium to another having a different index of refraction. Part of the flux is reflected; the fraction transmitted is described by the transmittance, τ, so the loss is:

$$(8)\ \text{FRESNEL LOSS (dB)} = 10 \log \frac{1}{\tau} = 10 \log \frac{2 + \frac{n_x}{n_y} + \frac{n_y}{n_x}}{4}$$

n_x = index of refraction of medium x
n_y = index of refraction of medium y

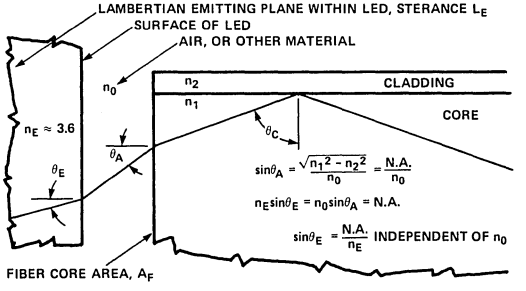
It is clear from equation (8) that the loss is the same in either direction. If two fibers are joined with an air gap between their faces, taking $n_x = 1$ for air and $n_y = 1.49$ for the cores of the fibers, the fiber-to-air Fresnel loss is 0.17dB. The air-to-fiber loss is the same, so the total airgap loss is 0.34dB. If several such connections are made, the loss could be high enough to make it worthwhile to use a coupling medium, such as silicone, to remove the air gap. Often, however, connector loss comes mainly from a gap deliberately inserted to prevent scratch damage to the fiber face and to reduce the variability of misalignment loss; i.e., it is sometimes more important to make the connector loss be consistent rather than low.

The use of a coupling medium is more significant when a fiber is coupled to an LED or IRED source. These sources are usually of gallium arsenide, or related substances, with a refractive index of 3.6. With such a high index of refraction, the use of an epoxy cement can reduce coupling loss by approximately 1dB. Figure 3 shows how the flux coupling is derived. If the size of the LED is much less than that of the fiber, a more effective technique is the use of a tiny lens over the LED. If the size of the fiber is smaller, the lens should be on the fiber, rather than the LED.

Rise Time Dispersion

Bandwidth limitation in fiber optics is the result of a phenomenon called DISPERSION, which is a composite of MATERIAL dispersion and MODAL dispersion. Both of these relate to the velocity of flux transmission in the core. Velocity varies inversely as the index of refraction, and if the index of refraction varies over the wavelength spectrum of the source, the flux having a wavelength at which the refractive index is lower will travel faster than the flux having a wavelength at which the index is higher. Thus, all portions of the spectrum of flux launched simultaneously will not arrive simultaneously, but will suffer time dispersion due to differences in travel time. This is MATERIAL DISPERSION. It is reduced by using sources of narrow spectrum (e.g., lasers) or fibers with a core index of refraction which is constant over the source spectrum.

In Figure 2, notice that rays moving parallel to the axis travel a path length which is shorter than that of rays which are not paraxial. Those rays propagating in the higher-order modes will, therefore, have a longer travel time than those in lower-order modes, and simultaneously launched rays will suffer dispersion of their arrival times. This is MODAL DISPERSION. It can be reduced only by reducing the N.A. (smaller acceptance angle) to allow only lower-order modes to propagate.



FLUX COUPLED, $\phi = \pi\tau L_E A_F \sin^2\theta_E$

LED–TO–CORE TRANSMITTANCE $\tau = \left(\frac{4}{2 + \frac{n_E}{n_0} + \frac{n_0}{n_E}}\right)\left(\frac{4}{2 + \frac{n_0}{n_1} + \frac{n_1}{n_0}}\right) = 1 - \left(\frac{\text{FRESNEL}}{\text{LOSS}}\right)$

WITH AIR, $n_0 = 1.0$, $\tau_1 = 0.65$

$10 \log \frac{\tau_2}{\tau_1} = 1.03$ dB

WITH EPOXY, $n_0 = 1.5$, $\tau_2 = 0.83$

EPOXY DOES NOT AFFECT ACCEPTANCE ANGLE BUT DOES REDUCE FRESNEL LOSS

Figure 3. Acceptance Angle and Fresnel Loss Effects.

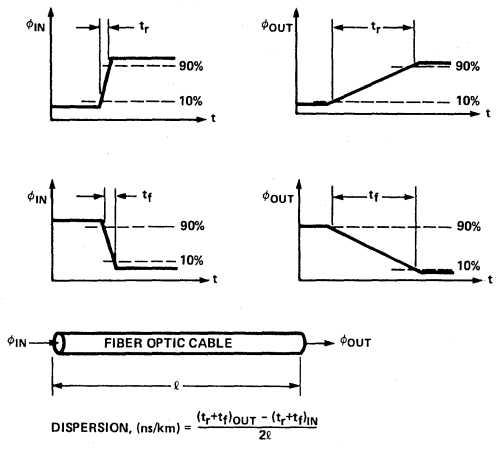


Figure 4. Rise Time Dispersion.

Whether the dispersion is material or modal (or both), it is measured, as shown in Figure 4, by applying positive and negative steps of flux and measuring the rise and fall times at the input and output of a fiber long enough to exhibit significant dispersion. Time dispersion is then defined as

(9) RISE TIME DISPERSION

$$\frac{\Delta t}{\ell}\ (\text{ns/km}) = \frac{1}{2\ell}\left[(t_r + t_f)_{OUT} - (t_r + t_f)_{IN}\right]$$

where ℓ is the length (in kilometres) of the fiber and t_r, t_f are the 10% to 90% rise and fall times.

Flux steps, rather than pulses, are used to avoid incorrect results that source or detector rise and fall times might introduce. Both polarities of step are recommended in order to compensate for non-linearity in either the source or the detector used.

Modulation frequency response of a fiber has a 6dB per octave roll-off, so the effect of rise time dispersion can also be described in terms of a length-bandwidth product:

(10) 3dB BANDWIDTH CONSTANT = $\Delta f \cdot \ell = 0.35\frac{\ell}{\Delta t}$

Construction of Fiber Optics

Fibers having a sharp boundary between core and cladding, as in Figure 2, are called STEP INDEX fibers. The reflection at the boundary is not a "zero-distance" phenomenon — the ray, in being reflected, is actually entering a minute distance into the cladding and there is some loss. This loss can be seen as a faint glow along the length of unjacketed lossy fibers carrying visible flux. To reduce such reflection loss, it is possible to make the rays turn less sharply by reducing the index of refraction gradually, rather than sharply, from core to cladding. A fiber of such a form is called a GRADED INDEX fiber and the rays propagate as shown in Figure 5. Graded index fiber has not only a very low transmission loss, but modal dispersion is also very low. Higher-order modes do travel longer paths, but in the off-axis, lower-index regions they travel faster so the travel time differential between high-order and low-order modes is not as large as it is in step index fibers.

Graded index fiber has higher coupling loss and may be more costly than step index fiber. It is, therefore, used mainly in applications requiring transmission over many kilometres at modulation bandwidths over 50MHz. For shorter distances and/or lower bandwidths, a variety of step index fibers are available at a variety of costs.

Figure 6 shows the construction of a Hewlett-Packard fiber optic cable. Over the fused-silica, step-index, glass-clad fiber there is a silicone coating to protect the thin

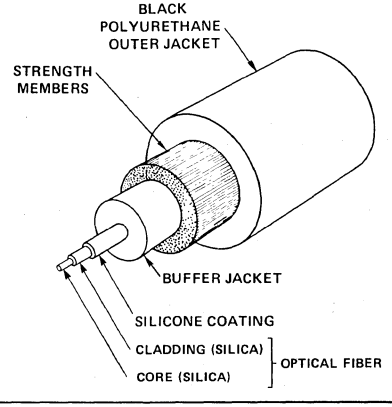


Figure 6. Step Index Fiber Optic Cable Construction.

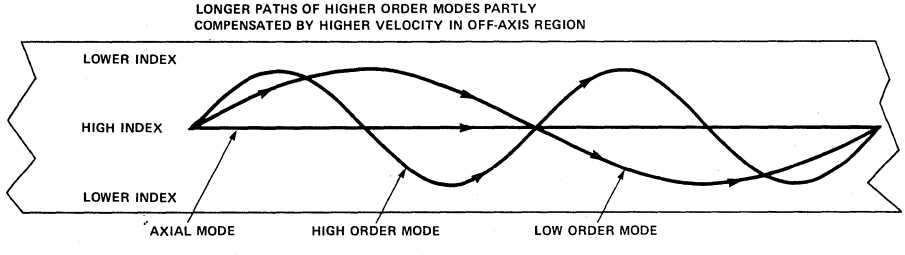


Figure 5. Graded Index Fiber Modes.

(20μm) cladding from scuffing. Over the buffer jacket are the tensile strength members, which allow the cable to be pulled through long conduits, and an outer jacket to protect the cable against crush and impact damage. This cable tolerates far more abuse than most wire cable. A sample was laid across the main entrance to the Hewlett-Packard headquarters and factory at 1501 Page Mill Road, Palo Alto. After several weeks of being driven over, night and day, there was no impairment of performance.

Other materials used in step index fibers are glass-clad glass, plastic-clad glass or fused silica, and plastic-clad plastic. These have N.A.'s ranging from less than 0.2 to more than 0.5, and transmission losses from less than 10dB/km to more than 1000dB/km. Some manufacturers offer bundled fibers in which the individual glass fibers are small enough to allow the cable to be very flexible. In earlier days of fiber optic development, bundled fibers were considered necessary for reliability because breakage of one or more fibers could be tolerated without total loss of signal transmission. Also, the large diameter of the fiber bundle allowed more tolerance in connector alignment. The popularity of fiber bundles has dwindled because the single-fiber cable durability is better than had been anticipated, and connectors are now available which are capable of providing the precise alignment required for low coupling loss with small-diameter single fibers.

Flux Budgeting

Flux requirements for fiber optic systems are established by the characteristics of the receiver noise and bandwidth, coupling losses at connectors, and transmission loss in the cable.

The flux level at the receiver must be high enough that the signal-to-noise ratio (SNR) allows an adequately low probability of error, P_e. In the Hewlett-Packard fiber optic system, the receiver bandwidth and noise properties allow a $P_e < 10^{-9}$ with a receiver input flux of 0.8μW under worst-case conditions. At higher flux levels, the P_e is reduced.

From the receiver flux requirement (for given P_e), the flux which the transmitter must produce is determined from the expression for a point-to-point system:

$$(11)\quad 10 \log \left(\frac{\phi_T}{\phi_R} \right) = \alpha_0 \ell + \alpha_{TC} + \alpha_{CR} + n\alpha_{CC} + \alpha_M$$

where ϕ_T is the flux (in μW) available from the transmitter
ϕ_R is the flux (in μW) required by the Receiver at P_e
α_0 is the fiber attenuation constant (dB/km)
ℓ is the fiber length (km)
α_{TC} is the Transmitter-to-Fiber coupling loss (dB)
α_{CC} is the Fiber-to-Fiber loss (dB) for in-line connectors
n is the number of in-line connectors; n does not include connectors at the transmitter and receiver optical ports
α_{CR} is the Fiber-to-Receiver coupling loss (dB)
α_M is the Margin (dB), chosen by the designer, by which the Transmitter flux exceeds the system requirement

Equation (11) is called the FLUX BUDGET and it is represented graphically in Figure 7. The same basic units (watts) are used for flux and for power, so it is correct and convenient to express flux in "dBm".

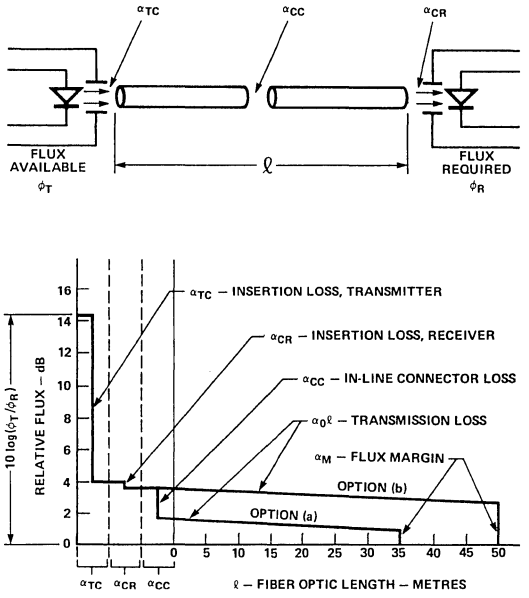


Figure 7. Flux Budget — Graphical Representation.

$$(12)\quad \phi(\text{dBm}) = 10 \log \left(\frac{\phi(\text{mW})}{1\ \text{mW}} \right) = 10 \log \left(\frac{\phi\ (\mu\text{W})}{1000\ \mu\text{W}} \right)$$

Here is an example of how the flux budget works:

1. Transmitter $\phi_T = 44\mu W$
2. Receiver $\phi_R = 1.6\mu W$

$$\Big\rangle\ 10 \log \left(\frac{\phi_T}{\phi_R} \right) = 14.39\text{dB}$$

Transmitter optical port: diameter = 200μm, N.A. = 0.5

Optical fiber (in connector): core diam. = 100μm, N.A. = 0.3

3. $\alpha_{TC} = \alpha_A + \alpha_{NA} = 20 \log \left(\frac{200}{100} \right) + 20 \log \left(\frac{0.5}{0.3} \right)$

$= 6.02\text{dB} + 4.44\text{dB} = 10.46\text{dB}$

Receiver optical port: diameter = 200μm, N.A. = 0.5

4. Because the diameter and N.A. of the receiver are both larger than those of the fiber, there is only a small amount of Fresnel loss, making $\alpha_{CR} \approx 0.34\text{dB}$

5. Apply equation (11) to see what the flux budget allows:

$14.39\text{dB} = \alpha_0 \ell + 10.46\text{dB} + n\alpha_{CC} + 0.34\text{dB} + \alpha_M$

$\alpha_0 \ell + n\alpha_{CC} + \alpha_M = (14.39 - 10.46 - 0.34)\text{dB} = 3.59\text{dB}$

6. Assume a transmission distance of 35 metres at 20dB/km

If cable length selections are 10-, 25-, and 50-metre lengths and connector loss is α_{CC} = 2dB, then either of two options may be chosen:

7. a) Use a 10m and 25m length with one connector:
$\alpha_0 \ell + \alpha_{CC}$ = (35m x 0.02dB/m) + 2dB = 2.7dB
This leaves α_M = (3.59 - 2.7)dB = 0.89dB

7. b) Use a 50m length and no connector:
$\alpha_0 \ell$ = (50m x 0.02dB/m) = 1.0dB leaving α_M = 2.59dB

Unless there is some good reason (cost, convenience, etc.) for choosing the 10m/25m option, it would be better to select the 50-metre option because it allows a larger α_M. In flux budgeting, α_M should always be large enough to allow for degradation of the efficiency of the flux generator in the transmitter (LED, IRED, laser, etc.). On the other hand, in dealing with more powerful transmitters, α_M must not be so large that it exceeds the dynamic range of the receiver.

Dynamic Range

The dynamic range of the receiver must be large enough to accommodate all the variables a system may present. For example, if the system flexibility requirement is for transmission distances ranging from 10 metres to 1000 metres with 12.5dB/km cable, and up to two in-line connectors, the dynamic range requirement is:

$$\begin{aligned} \alpha_0 \ell &= 1\text{km} \times 12.5\text{dB/km} = 12.5\text{dB} \\ n\alpha_{CC} &= 2 \times 2\text{dB} = 4.0\text{dB} \\ \alpha_M &= 3.0\text{dB} \\ \text{thermal variations} &= 1.0\text{dB (estimated)} \\ & 20.5\text{dB} \end{aligned}$$

Accommodating a 20dB optical power dynamic range plus high sensitivity requires the receiver to have two important features: automatic level control, and a-c coupling or its equivalent. The a-c coupling keeps the output of the amplifier at a fixed quiescent level, relative to the logic thresholds, so that signal excursions as small as the specified minimum can cause the amplifier output to exceed the logic threshold. This function can also be called d-c restoration.

ALC (automatic level control) adjusts the gain of the amplifier. Low-amplitude excursions are amplified at full gain; high-amplitude excursions are amplified at a gain which is automatically reduced enough to prevent saturation of the output amplifier. Saturation affects propagation delay adversely so ALC is needed to allow high speed performance at high, as well as low, signal levels.

HEWLETT-PACKARD'S FIBER OPTIC SYSTEM

A number of objectives were established as targets for this development. Convenience and simplicity of installation and operation were the primary objectives, along with a probability of error $P_e < 10^{-9}$ at 10Mb/s NRZ, over moderate distances. In addition, there were the traditional Hewlett-Packard objectives of rugged construction and reliable performance. Manufacturing costs had to be low enough to make the system attractively priced relative to its performance.

Electrical convenience is provided by several system features. The Receiver and the Transmitter require only a single +5-volt supply. All inputs and outputs function at TTL logic levels. No receiver adjustments are ever necessary because the dynamic range of the Receiver is 21dB or more, accommodating fiber length variations as well as age and thermal affects. When the system is operated in its internally coded mode, it has NRZ (arbitrarily timed data) capability and is no more complicated to operate than a non-inverting logic element. Built-in performance indicators are available in the Receiver; the Link Monitor indicates satisfactory signal conditions and the Test Point allows simple periodic maintenance checks on the system's flux margin.

There are also several optical and mechanical convenience features. The optical ports of the Transmitter and Receiver are well defined by optical fiber stubs built into receptacles that mate with self-aligning connectors. Low-profile packaging and low power dissipation permit the modules to be mounted without heat-sink provision on P.C. boards spaced as close as 12.5mm (0.5 in.).

The internally-coded mode of operation is the simplest way to use the Hewlett-Packard system. This mode places no restriction on the data format as long as either positive or negative pulse duration is not less than the minimum specified. The simplicity is achieved by use of a 3-level coding scheme called a PULSE BI-POLAR (PBP) code. This mode is selected simply by applying a logic low (or grounding) to the Mode Select terminal on the Transmitter — no conditioning signal or adjustment is necessary in the Hewlett-Packard Receiver because it automatically responds to the PBP code.

Transmitter Description

Figure 8 shows symbolically the logical arrangement of the Transmitter, waveforms for the signal currents I_A and I_B, and the resulting waveforms for the output flux. The arrangement shown is logically correct but circuit details are not actually realized as shown. For example, the current sources actually have partial compensation for the negative temperature coefficient of the LED (or IRED). In Figure 8, there are five important things to notice.

First, notice that the bias current, I_C, is never turned off — not even when the Transmitter is operated in the externally coded mode (Mode Select "high"). This is done to enhance the switching speed of the LED (or IRED) in either internally- or externally-coded mode. The bias current also stabilizes the flux excursion ratio (k in Equation 14) symmetry in the internally-coded mode.

Second, notice that

ϕ_L, the low-level flux, is produced by I_C
ϕ_M, the mid-level flux, requires $I_B + I_C$
ϕ_H, the high-level flux, requires $I_A + I_B + I_C$

As far as the Receiver is concerned, the excursion flux, $\Delta\phi$, produced by switching I_A and I_B, is the important parameter of the Transmitter. Average flux is, of course, related to excursion flux but is not as important in establishing the SNR of the system.

Third, notice that with Mode Select "low" and a 500kHz signal at Data Input, there will be only one refresh pulse generated in each logic state. The excursions (ϕ_H-ϕ_M) and (ϕ_M-ϕ_L) are nearly balanced so an average-reading flux meter will indicate the mid-level flux, ϕ_M, within +0.6% or -0.6% depending on whether the flux excursion ratio, k, is at its maximum or at its minimum limit.

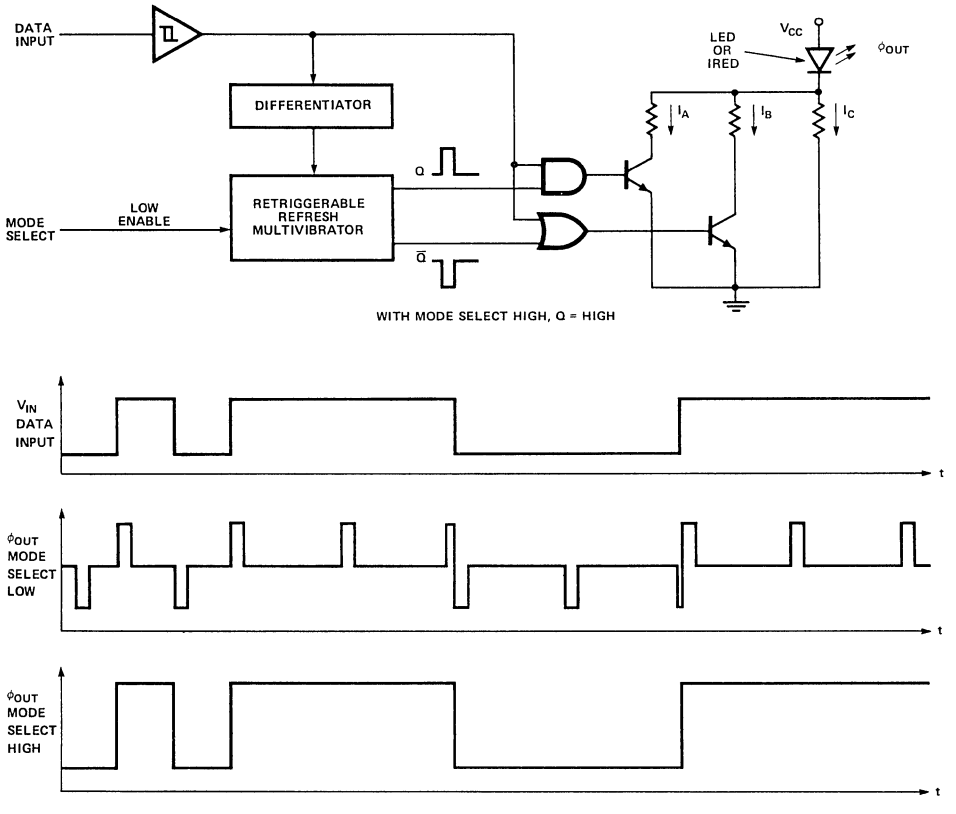


Figure 8. Transmitter Block Diagram and Waveforms.

Fourth, notice that, with Mode Select "low", any Data Input transition (either H-L or L-H) retriggers the Refresh Multivibrator to start a new train of pulses. All refresh pulses for either logic state have the same duration. This keeps the average flux very near the mid-level even when the duration in either logic state of arbitrarily timed input data is very short. Notice also that any refresh pulse is overridden (abbreviated) by the occurrence of a Data Input transition so there is no additional jitter when the duration of the Data Input in either state is at or near the same length of time as the refresh interval. The refresh interval is very long, relative to the refresh pulse duration, making a duty factor of approximately 2%; this also is done to keep the average flux near mid-level regardless of how long Data Input remains in either logic state. The only condition under which the average flux can deviate significantly from the mid-level occurs when Data Input remains in one state for a period of time LESS than the duration of the refresh pulse. If this is likely to occur, the format should be configured so the numbers of 1's and 0's are balanced as they would be in Manchester code. Observing this data format allows the use of the internally-coded mode of the Hewlett-Packard system at data rates ranging from arbitrarily low to higher than 10M Baud, with the absolute limit being that at which the signal intervals become as short as t_{PHL} and/or t_{PLH}.

Fifth, notice that with Mode Select "high," the Q output of the Refresh Multivibrator is "high" (and $\overline{Q}$ is "low"). Under this condition, I_A and I_B are both ON when Data Input is "high" and both OFF when it is "low". This makes the output flux excursion a logical replica of the Data Input.

Flux Measurement

A high-speed photodetector and oscilloscope could be used for measuring the excursion flux, but an average-reading flux meter can be used to measure $\Delta\phi$ as follows:

With Mode Select "high":

1. Apply steady-state "low" to Data Input and observe ϕ_L with flux meter.
2. Apply a 500kHz square wave (50% duty factor) to Data Input and observe $(\Delta\phi + \phi_L)$ with the flux meter and subtract ϕ_L (Step 1) to obtain $\Delta\phi$.

This procedure also yields the proper value of the high-level flux, ϕ_H, to be used in computing the flux excursion ratio, k. Since $\phi_H = (\phi_L + 2\Delta\phi)$, the value of ϕ_H is:

(13) HIGH-LEVEL FLUX, $\phi_H = 2(\Delta\phi + \phi_L) - (\phi$)
Step 2 Step 1

It appears, from the waveforms in Figure 8, that the 500kHz signal prescribed in Step 2 is not necessary; that is, with Data Input at a steady-state high, the flux meter would read ϕ_H directly, from which $\Delta\phi$ could be calculated by

subtracting ϕ_L (observed in Step 1) and dividing by two. However, this method would cause slightly more heating of the LED and lead to a slightly different (and incorrect) measurement of ϕ_H and $\Delta\phi$. With the values of ϕ_H and ϕ_L from Step 1 and 2, the flux excursion ratio can now be computed:

$$(14)\ \text{FLUX EXCURSION RATIO, } k = \frac{\phi_H - \phi_M}{\phi_M - \phi_L}$$

In a 2-Level Code, there is, of course, no mid-level; however, the definition of flux excursion ratio is the same as for Pulse Bi-Polar code, i.e., Equation (14). It is only necessary to substitute average flux for mid-level flux, ϕ_M, in Equation (14). For 2-Level Code, the average flux is:

$$(15)\ \text{AVERAGE FLUX (2-Level Code)} = \frac{\phi_H \Sigma t_H + \phi_L \Sigma t_L}{\Sigma t_H + \Sigma t_L}$$

where Σt_H is the total time the flux is at level ϕ_H
Σt_L is the total time the flux is at level ϕ_L

Substitution of this expression for ϕ_M in Equation (14) leads to:

$$(16)\ \text{FLUX EXCURSION RATIO} = k = \frac{\Sigma t_L}{\Sigma t_H}$$

Equation (16) shows why it is that when a 2-Level Code is used (e.g., with Mode-Select "high" in the Hewlett-Packard Transmitter) the data input signal must, on average, have a 50% duty factor to make k = 1. That is, in the averaging interval, the total number of "mark" intervals should be equal to the total number of "space" intervals, such as in Manchester code.

Use of 2-Level Code also requires that the input flux remain for less than 5μs at either high or low level. This is necessary to avoid "pulling" the receiver dc restorer voltage too far away from the value corresponding to the average flux, and possibly losing occasional bits.

Receiver Description

The Hewlett-Packard Receiver block diagram is shown in Figure 9. There are four functional blocks:

1. The amplifier, including a gain-control stage and split-phase outputs with a voltage divider for each.
2. The dc-restorer with a long time constant.
3. Logic comparators with an R-S latch.
4. Positive and negative peak comparator with single-ended output for the ALC and link monitor circuits.

Optical flux at the input is converted by the PIN photodiode to a photocurrent, I_P, which is converted to a voltage by the PREAMPLIFIER. This voltage is amplified to a positive-going output, V_{P1}, and a negative-going output, V_{N1}. A rising input flux will cause V_{P1} to rise and V_{N1} to fall. These voltages are applied to the differential inputs of the DC RESTORER AMPLIFIER whose output, V_T, falls until it is low enough to draw the average photocurrent away from the preamplifier via the 25k resistor. This makes $V_{P1} \approx V_{N1}$ when the input flux is at the average level. The output impedance of the dc restorer amplifier is very high, making a long time constant with the filter capacitor, C_T. The long time constant is required for loop stability when input flux levels are so low that there is little or no ALC gain reduction, with consequently high loop gain. With no input flux, $V_T = V_{TMAX}$; as input flux rises, V_T falls proportionately, so the voltage at the TEST POINT can be used as an indicator of the average input

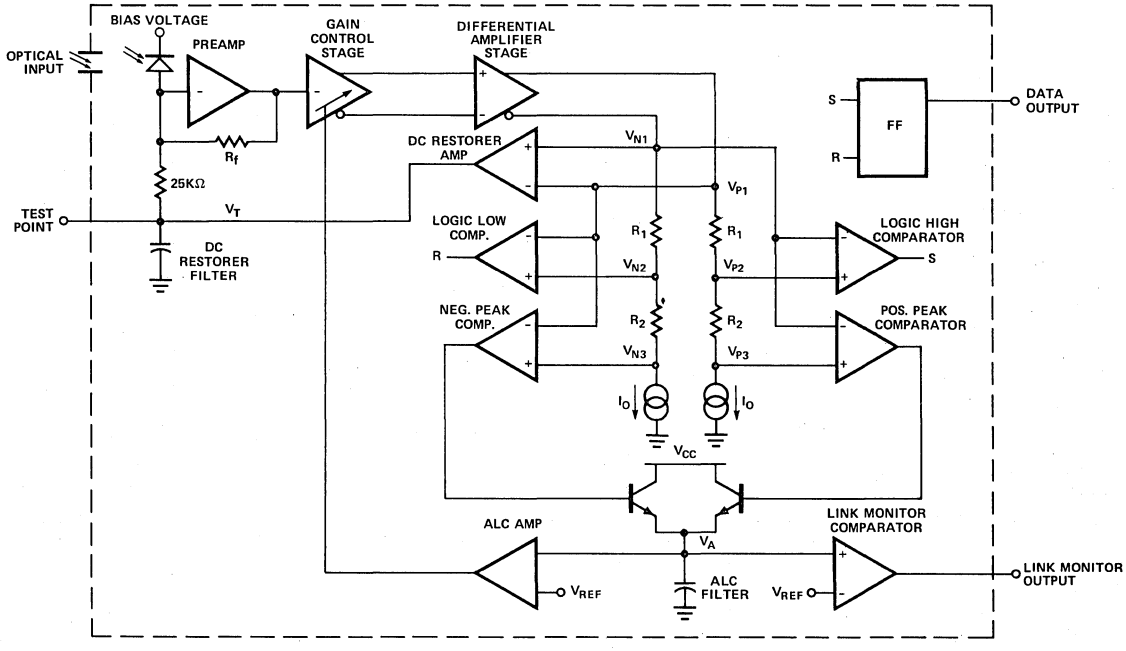


Figure 9. Receiver Block Diagram.

flux. With respect to the Receiver optical port, the responsivity of the PIN photodiode is approximately 0.4A/W, leading to the expression:

$$(17)\ \text{AVERAGE INPUT FLUX}, \phi_{AV}(\mu W) \approx \frac{[V_{TMAX} - V_T]\ (mV)}{10}$$

where V_{TMAX} = Test Point Voltage with no optical input signal.

The instrument for observing V_T must not load the Test Point significantly, so an input resistance of 10MΩ is recommended.

As described above, when the input flux is at the average level, the positive-going and negative-going output voltages V_{P1} and V_{N1} are approximately equal. Notice that this makes the outputs of both logic comparators low. A positive flux excursion, rising faster than the dc restorer (with its long time constant) can follow, will cause V_{P1} to rise and V_{N1} to fall. If the positive flux excursion is high enough, the LOGIC$_1$ HIGH COMPARATOR input voltage (V_{P2} - V_{N1}) becomes positive, and a SET pulse is produced for the R-S flip-flop. [Similarly, a negative flux excursion of such amplitude would make (V_{N2} - V_{P1}) become positive and a RESET pulse would be produced.] A larger amplitude of positive flux excursion would make the POSITIVE PEAK DETECTOR input voltage (V_{P3} - V_{N1}) change from negative to positive and cause current to flow into the ALC FILTER capacitor. When the voltage V_A starts to rise above V_{REF}, the ALC AMPLIFIER output will operate on the GAIN CONTROL AMPLIFIER to limit the Receiver's forward gain. Notice that the ALC action is the same for a negative flux excursion, so that the Receiver's gain limitation is determined EITHER by positive flux excursion OR by negative flux excursion — whichever is the larger. For this reason, the positive and negative excursions must be nearly balanced with respect to the average flux. The allowable imbalance is determined by the values of the resistors in the negative and positive voltage dividers. The ALC action limits the maximum excursion to a voltage I_O (R_1 + R_2), whereas the logic threshold is only I_O R_1. Actual limits are established by the tolerances on the resistors and current sources. Notice that the ALC voltage, V_A, activates both the ALC COMPARATOR and the LINK MONITOR COMPARATOR. Therefore, a "high" LINK MONITOR signifies two conditions:

1. The input flux excursions are high enough to cause ALC action (gain limitation).
2. The excursions are more than adequate for operation of the logic comparator.

Notice that the LINK MONITOR could be "high," but k could be outside the specified limits such that P_e exceeds 10^{-9}. Conversely, because of safety margin in the Receiver design, it is also possible to have $P_e < 10^{-9}$ when the flux excursions are too small to make the LINK MONITOR "high".

OPERATION OF THE HEWLETT-PACKARD SYSTEM

With Hewlett-Packard Components Exclusively

The main concern in a fiber optic link is the flux budget. Other areas of concern are: data rate, data format, and the interface with other elements of a data transmission system.

Flux budgeting, using the Hewlett-Packard Transmitter, Receiver, Connector, and Cable components is very straightforward for most applications. It is necessary only to use the data sheet information correctly in making the coupling loss and transmission loss allowances.

When used with other Hewlett-Packard components, the characteristics of the Receivers are not critical. Their optical ports have a diameter and N.A. which are both greater than the size and N.A. of the Hewlett-Packard Cable. The Receivers also have a high responsivity and the spectral response is nearly constant over the spectrums radiated by Hewlett-Packard Transmitters.

With Components From Other Manufacturers

When using the Hewlett-Packard Receivers with other cables, it may be necessary to account for N.A. loss and/or area mismatch loss. When other sources are used, it may be necessary to compute an effective flux ratio:

$$(18)\ \text{EFFECTIVE FLUX RATIO, EFR}_S\ (\text{Source Spectrum}) = \frac{\int \phi_\lambda R_{r\lambda} d_\lambda}{\int \phi_\lambda d_\lambda}$$

where $R_{r\lambda}$ is the relative response of the Receiver (from data sheet)

ϕ_λ is the spectral flux function of the source

If the transmission loss of the cable varies sharply over the wavelength range of the source spectrum, then the spectral transmittance of the cable should be included in the computation of EFR. The spectral transmittance varies with cable length, so the integration must be performed using the cable length required in a particular installation:

$$(19)\ \text{EFFECTIVE FLUX RATIO, EFR}_{CS}\ (\text{Cable and Source}) = \frac{\int \tau_\lambda \phi_\lambda R_{r\lambda} d_\lambda}{\int \tau_\lambda \phi_\lambda d_\lambda}$$

where τ_λ is the spectral transmittance of a particular length of fiber optic cable, computed as:

$$(20)\ \tau_\lambda = 10^{-\left(\frac{\ell}{10}\right)\alpha_{0\lambda}}$$

where $\alpha_{0\lambda}$ is the spectral function in (dB/km) of the fiber optic cable and ℓ is the particular cable length (km)

Notice that as the length is reduced, τ_λ becomes more nearly a constant and may be factored out of both numerator and denominator of Equation (19). When EFR is significantly less than unity, it enters the flux budget expression, Equation (11).

$$(21)\ 10 \log\left(\frac{\phi_T}{\phi_R}\right) = \alpha_{TC} + \alpha_{CR} + n\alpha_{CC} + \alpha_0 \ell + \alpha_M \underset{-10 \log (EFR)}{}$$

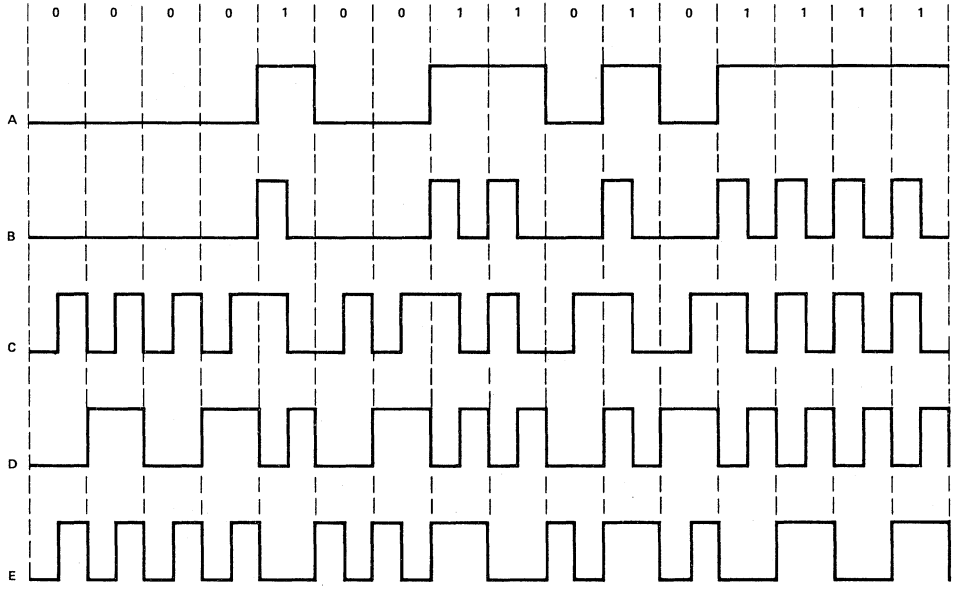
See Equations 11, 18, and 19 for definition of terms.

The optical ports of Hewlett-Packard Transmitters are designed for mating with Hewlett-Packard Cable/Connector assemblies, but their characteristics require a little more attention than do the Receiver optical ports. The Transmitter and Cable/Connector data sheets should be consulted for the correct values of size and N.A., or for the directly-given value of transmitter-to-fiber coupling loss, α_{TC}, to use in flux budgeting. In applications having very short transmission distances, but requiring a number of in-line (cable-to-cable) connections, it is likely to be advantageous to use fiber optics of larger core diameter

and N.A., such as some of the plastic types. The larger core diameter reduces the likelihood of losses in connectors due to misalignment. Depending on the size and N.A. of the Transmitter optical port, a larger core diameter and N.A. in the fiber optic cable may also reduce α_{TC}, but if the cable core diameter is too large, the cable-to-receiver loss, α_{CR}, may be excessive.

Data Rate and Format

The other areas of concern (data rate, data format, and interface) are interactive, depending on system requirements. In any single transmitter-to-receiver link, the flux budget along with probability of error P_e, establish the signaling rate, in baud units, while the data rate, in bits per second, depends also on the data format, or transmission code. NRZ (Non-Return-to-Zero) is the term for a transmission code in which the signal does not periodically return to zero. If a stream of NRZ data contains a series of consecutive "1's", the signal remains at the "1" level; similarly, the signal remains at the "0" level for consecutive "0's". With RZ (Return-to-Zero) codes, the level periodically changes from high level to low level or back, never remaining at either level for a period of time longer than one bit interval. Some examples of codes are given in Figure 10. Notice that NRZ code uses the channel capacity most efficiently since it requires only one code interval per bit interval. The RZ codes illustrated use two code intervals per bit interval while other codes may require an even higher channel capacity for a given data rate. NRZ code requires a clock signal at the receiving end to define, for each interval, the point in time at which the data is valid. The time at which the data is clocked must be sufficiently clear of the interval edges to avoid phase-shift errors due to jitter, rise time, or propagation delay. Since the clock signal is separately transmitted, phase shift in the clock channel can contribute to the phase-shift error unless it is equal, in direction and magnitude, to the phase shift in the data channel. For this reason, fiber optic



	CODE	DESCRIPTION	CHANNEL REQUIRED	REQUIRES DC?	REQUIRES CLOCK?
A	NON-RETURN TO ZERO (NRZ)	High during entire "mark", low during entire "space" interval	1 Mbaud per Mb/s	YES	YES
B	RETURN TO ZERO (RZ)	Low during entire "space", momentarily high during "mark" interval	2 Mbaud per Mb/s	NO	YES
C	MANCHESTER (SELF-CLOCKING RZ)	Positive transition for "space", negative transition for "mark"	2 Mbaud per Mb/s	NO	NO
D	BIPHASE MARK (MANCHESTER II)	Each bit period begins with a transition. "Space" has NO transition during bit period — "mark" has one transition during bit period	2 Mbaud per Mb/s	NO	NO
E	BIPHASE SPACE	Same as Biphase Mark except "mark" and "space" reversed	2 Mbaud per Mb/s	NO	NO

NOTE THAT C, D, E HAVE 50% DUTY FACTOR (k = 1.00)

Figure 10. Examples of NRZ and RZ Code Patterns.

channels carrying clock signals should use the same type of cable and the same length, unless the transmission distance is very short. Note that the transmission time delay in an optical fiber depends on the core index of refraction:

(22) TRANSMISSION DELAY, $t_\ell = \left(\frac{1}{c}\right) \ell n$

where c is the velocity of light in a vacuum, $c = 3 \times 10^8$ m/s
ℓ is the fiber optic cable length (m)
n is the core index of refraction

and differential delay between a data channel and a clock channel is:

(23) DIFFERENTIAL DELAY, $t = \left(\frac{1}{c}\right) [\ell_2 n_2 - \ell_1 n_1]$

Some RZ codes are self-clocking — i.e., a separate channel to transmit the clock signal is not required, so there is no problem with differential delay. For this reason, RZ codes may be preferred even though the data rate is less than that of NRZ. Note that in its internally coded mode, the Hewlett-Packard fiber optic system transmits either NRZ or RZ codes of arbitrary format and duty factor. In the externally coded mode, the system requires the code to be RZ; moreover, the duty factor of the code must be 50% and the signal must remain LESS than 5μs in either high state or low state.

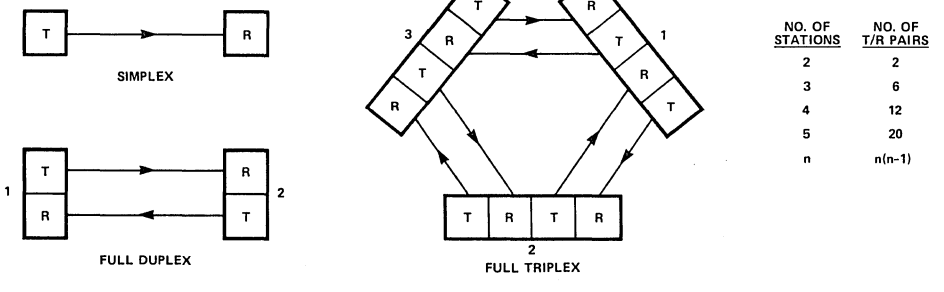
The Hewlett-Packard system is capable of a 10 Mbaud signaling rate. If a higher data rate is required, the data stream can be divided among additional channels. If each channel is RZ coded, such as with Manchester code, the capacity of each channel is 5Mb/s and if the total data rate requirement is 20Mb/s, four channels are required. Using NRZ, the 20Mb/s data can be transmitted on two channels, with a third channel for the clock signal. Thus, if the data rate requirement exceeds 15Mb/s, the NRZ format requires fewer fiber optic channels.

System Configuration

The simplex arrangement in Figure 11 allows data in one direction only, and the format should, therefore, include error checks, such as parity bits. The full duplex arrangement requires two Transmitter/Receiver (T/R) pairs and two cables but allows data to go in both directions simultaneously. If, at a given time, Station 1 is transmitting, the return transmission from Station 2 can be unrelated to the information from Station 1, but could also be a relay or re-transmission of the data received by Station 2, so a logic delay and comparator circuit in Station 1 can check for errors and allow corrections. The same is true for the full triplex arrangement. Extension to larger numbers of stations is possible and the benefits are the same, but the number of T/R pairs increase rapidly, as shown by the series in Figure 11, requiring n (n-1) T/R pairs for n stations.

Half-duplex (not illustrated) is a means for allowing two stations to alternately use the same transmission medium. With a wire cable, half-duplex operation is commonly and easily done; it can also be done with fiber optic cable but the fiber-furcating couplers for accomplishing it are very lossy, are not commonly available, and will not be discussed.

Data interchange among a large number of stations can be accomplished with fewer T/R pairs by using the Master Station Multiplex (MSM) arrangement in Figure 12. The MSM arrangement requires only 2(n-1) T/R pairs for n stations (master + (n-1) slaves). Its operation differs from the full n-plex arrangement of Figure 11 in that only the master station transmits directly to all other stations. Data from any slave station is transmitted to master and re-transmitted to all slave stations according to the "re-transmit enable" ($E_1 ... E_X$) selection made in the master station. Thus, a complete error check is possible. Regardless of how many slave stations are added, the transmission delay from any slave to any other slave is just the delay of two fiber optic links plus the propagation



NO. OF STATIONS	NO. OF T/R PAIRS
2	2
3	6
4	12
5	20
n	n(n-1)

APPLICATION NOTES

Figure 11. Simplex, Full-Duplex, Full Triplex, Full-n-plex Fiber Optic Links.

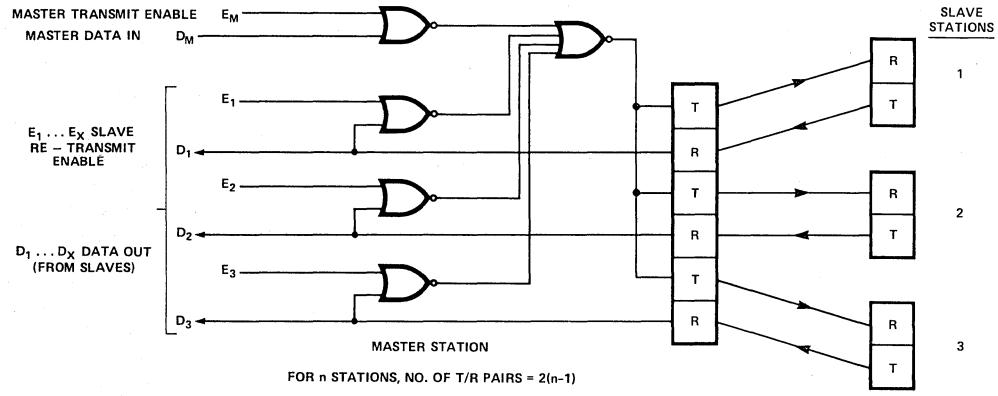


Figure 12. Master Station Multiplex Arrangement for Fiber Optic Links.

delay in the master station's relay circuit. The time delay between re-transmission from the master and the error-check return transmissions from the slaves is the same if each link length is the same, i.e., two links plus relay time. Notice that a complete error check requires an error check in the master, plus an error check in the station where the data originated. Another feature of the MSM system is that any slave station can be disconnected or turned off without affecting the other stations. With slightly more complicated relay control logic in the master stations, the MSM system can provide even more flexibility in the control of data movement — the schematic in Figure 12 is intended only to illustrate the potential flexibility of MSM.

At the expense of less flexibility and longer transmission delay, multiplex operation can be done with an even smaller number of T/R pairs by means of Looped-Station Multiplexing (LSM) as in Figure 13. In addition to requiring only n T/R pairs for n stations, LSM offers the advantage that an error check is required only at the station from which the data originates. There are some disadvantages. A relatively minor disadvantage is the data delay around the loop to where the data originated. A less minor disadvantage is the fact that, even if one of the stations in the loop is designated for loop control, it does not have control as absolute as that of the master station in MSM. A major disadvantage is that removal of one or more stations from the loop may require a re-run of the fiber optic cable unless the flux budget allows insertion of a connector to replace the station(s) removed. There is some error accumulation around the loop, but this is not a disadvantage if error correction is applied.

Error Accumulation

Where error correction is inconvenient or impossible, the accumulation of error through data relay units may be significant. With Hewlett-Packard components operated within the limits prescribed by the data sheet parameters and the flux budget, any point-to-point link has a

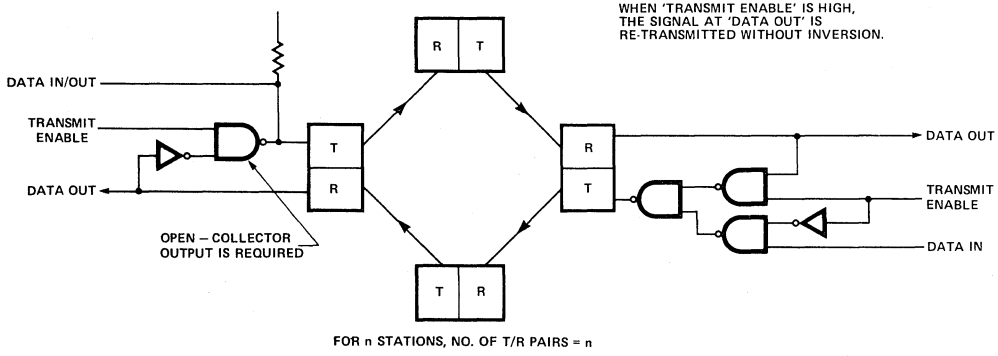


Figure 13. Looped-Stations Multiplex Arrangement for Fiber Optic Links.

probability of error $P_e < 10^{-9}$. This means that $P_e < 10^{-9}$ as long as the loss margin, α_M(dB) is above zero. With a number, n, of repeater links, the worst case estimate of cumulative probability of error is the RMS value:

(24) CUMULATIVE PROBABILITY OF ERROR,

$$P_{e,n} = 1 - \prod_{i=1}^{n}(1 - P_{e,i}) \approx \sum_{i=1}^{n} P_{e,i}$$

where $P_{e,i}$ is the probability of error in link "i"

If each link has the same probability of error, P_e, then the cumulative value of P_e is estimated at:

(25) CUMULATIVE PROBABILITY OF ERROR FOR EQUAL P_e's $\quad P_{e,n} \approx nP_e$

However, as in any chain, the probability of error is usually just that of the "weakest link," that is, the link having the highest probability of error.

Measuring the probability of error can be very time-consuming if P_e has a very low value. For instance, if $P_e = 10^{-9}$ at 10 Mbaud (BER = 10^{-9}), this suggests that if the system is operated for 100 seconds at 10 Mbaud (accumulate 10^9 bits) with one error, the $P_e = 10^{-9}$ is verified. This is not necessarily true. The significance of $P_e = 10^{-9}$ is that over several such periods the average error is one per 100 seconds. A less time-consuming procedure is to lower the signal (flux) level until the error rate, $P_{e,N}$ is measurably high in a comfortable period of time, and note this flux level as ϕ_N, the Noise measurement flux level. The operating flux level is designated ϕ_0, and is found from the ratio:

26. $$\frac{X_0}{X_N} = \frac{\phi_0}{\phi_N} \text{ and } X_0 = X_N \frac{\phi_0}{\phi_N}$$

and from the complementary error function:

$P_e = \text{erfc}(X_0) = 1 - \text{erf}(X_0)$ calculated for ϕ_0

$P_{e,N} = \text{erfc}(X_N) = 1 - \text{erf}(X_N)$ measured at ϕ_N

$$\text{erfc}(X) \approx \frac{.54}{X}(\epsilon^{-X^2}) \text{ for } P_e < 10^{-4}$$

This measurement and relationship can be useful in evaluating the relative merits in the tradeoff between running a single link over a long distance versus operating with one or more repeaters. The use of repeaters usually yields the lower P_e, but may be "overkill" in some cases.

INSTALLATION, MEASUREMENT, AND MAINTENANCE

The shielded metal packages of Hewlett-Packard Fiber Optic Modules are very sturdy and can be mounted in any position. Both Transmitter and Receiver dissipate very low power, so heat sinking is not required. A cool location is preferred, especially for the Transmitter. The main concern in selecting the locations of both modules is accessibility of the optical ports.

Mounting

The preferred mounting is with two #2-56 screws on a printed circuit board. Clearance must be provided for the Lock Nut, which protrudes 0.5mm to 1.0mm (depending on angular position) beyond the plane of the module's bottom surface. The usual way to deal with this is to allow the Lock Nut to overhang the edge of the P.C. board as in Figure 14. Lock Nut clearance could also be provided by an opening in the board, or by using washers of 1mm thickness on the #2-56 mounting screws to space the Module bottom 1mm from the board. Screws entering the #2-56 tapped holes MUST NOT TOUCH BOTTOM AS THIS MAY DAMAGE THE MODULE. The #2-56 tapped hole is 5.6mm (0.22 in.) deep, which provides an ample purchase on the thread.

P.C. Board Thickness		Recommended Screw Length — mm (in.)	
mm	in.	W/O Spacer	W/1-mm Spacer
0.79	1/32	4.78 (.188)	6.35 (.250)
1.59	1/16	6.35 (.250)	6.35 (.250)
2.38	3/32	6.35 (.250)	6.35 (.250)

The #2-56 holes near the front of the package are the only screw holes that may be used for mounting the module. UNDER NO CIRCUMSTANCES MAY THE SCREWS ALREADY INSTALLED OR THE SET SCREW BE DISTURBED. Disturbing these may cause interior damage.

For additional support, the electrical leads may be bent down and soldered into the P.C. board. In bending the leads, care must be taken to avoid strain at the point where the leads enter the glass seal. This can be done by applying mechanical support between the module and the bending point which should be at least 1.0mm (0.04 in.) from the end of the module. A needle-nose pliers can also be used to bend the leads individually, providing no bending moment is transferred to the seal. See Figure 14 for details fo these techniques.

Panel mounting can also be used. This is an especially attractive mounting when R.F. shield integrity must be maintained. As seen in Figure 15, the panel thickness must be less than 4mm (5/32 in.) and have a counter-bore to receive the Lock Nut. This will make the mounting secure and leave enough of the Barrel outside the panel to permit installation of an external mounting nut as well as the Cable Connector.

Fiber Optic Cable Connections

The data sheet cautions against disturbing the Lock Nut and Barrel. This is to prevent damage by someone who has not read the following material:

As seen in Figure 16, there is a clearance between the interior end of the Barrel and a shoulder on the Fiber Alignment Sleeve. If this clearance is not maintained, there is a risk that a force applied to the Barrel may be transmitted by the Fiber Alignment Sleeve to the optical fiber stub, forcing the stub against the face of the source or detector. The source (or detector) is an extremely fragile semiconductor device and even a very small force can cause severe damage. Should it be necessary to remove the Lock Nut and Barrel, they should be reinstalled with this procedure:

1. Lightly and carefully thread the Barrel into the Module body until it comes against the shoulder of the Fiber Alignment Sleeve.
2. Back the Barrel OUT ONE FULL TURN, then HOLD THE BARREL FROM TURNING while seating the Lock Nut securely against the body. During final tightening of the Lock Nut, the Barrel may be allowed to enter no more than HALF A TURN.

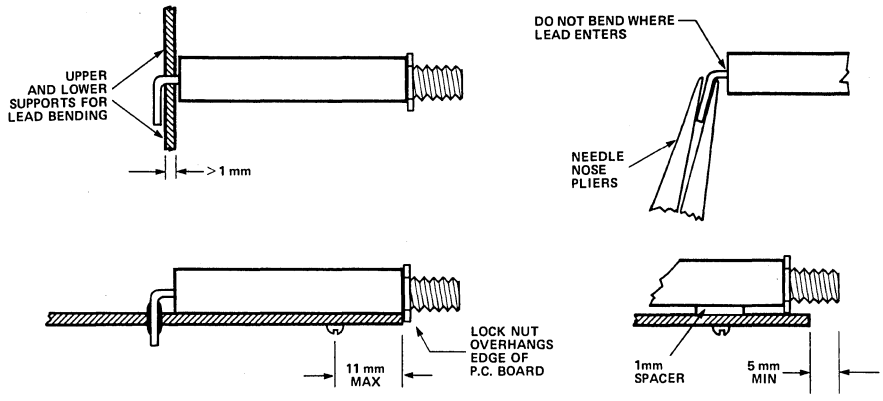


Figure 14. Lead Bending and P.C. Board Mounting.

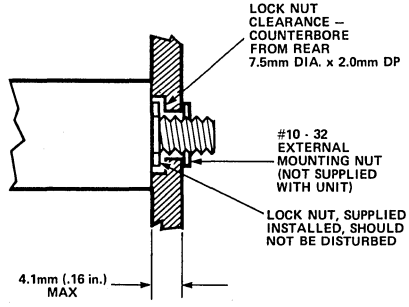


Figure 15. Panel Mounting.

When Hewlett-Packard Cable Connectors are joined, either to each other or to the optical port of a Transmitter or Receiver, there is a cylindrical spring Sleeve that aligns the Ferrules. This is shown in Figures 16 and 17. It may be difficult to see, but the Sleeve does have a slightly flattened "leaf" on either side of a notch. The notch makes the leaves spring separately, allowing the Ferrules at opposite ends of the sleeve to have slightly different diameters and yet be firmly aligned by the curved interior wall. A chamfer on the edge of the Ferrule aids insertion. In making temporary Cable-to-Cable connection, it is permissible, and often convenient, to omit the Barrel, since it does not perform an alignment function. When the Barrel is used for a more sturdy joint, the connection procedure is:

1. Install the Sleeve and Barrel on one Connector, using only FINGER TIGHTNESS of the Coupling on the Barrel.
2. Start the Ferrule of the second Connector into the Sleeve.
3. Engage the Coupling on the Barrel threads and tighten FINGER TIGHT.

Alignment of the Ferrules (and hence the fiber optics) is performed by the Sleeve; the Barrel and Couplings are intended only for tensile support, but if they are OVER tightened, they may cause misalignment. Loss of coupling due to misalignment can be observed at the V_T (Test Point) on the Receiver when the System is active:
$\Delta V_T/\Delta\phi \approx 10mV/\mu W$.

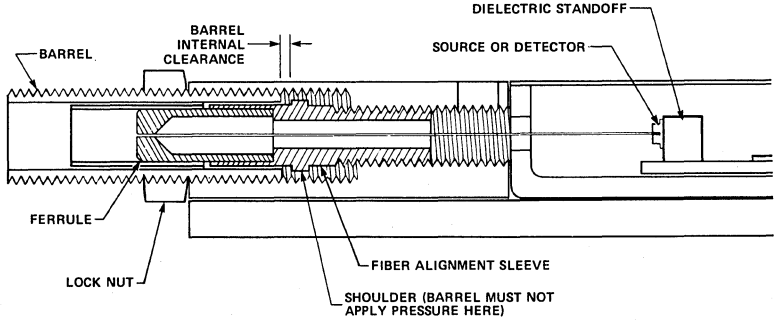


Figure 16. Opto-Mechanical Structure of T/R Modules.

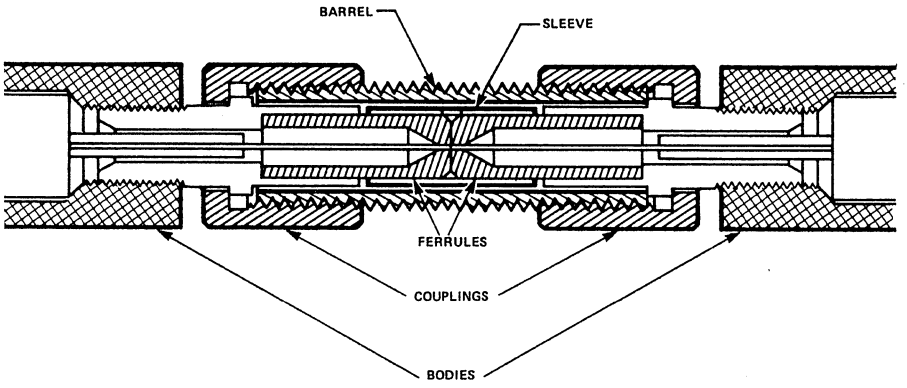


Figure 17. In-Line Connector Arrangement.

The procedure above applies also to making Cable connection at the Receiver and Transmitter, except that the Sleeve and Barrel are already installed. In manufacture, the Sleeve in the Module is pre-stressed for a tighter fit on the Ferrule in the Module than on the Ferrule in the Connector. The Sleeve is not likely to be pulled out when the Module is disconnected, but if that does happen, it can be reinstalled without removing the Barrel by using the Connector Ferrule to guide and support it.

In connecting fiber optics other than those from Hewlett-Packard to a Hewlett-Packard module, it is necessary to center the fiber in a cylinder with the same outside diameter as the Hewlett-Packard Ferrule over a length (to first shoulder) equal to half the length of the Sleeve, i.e., 3.5mm. This is adequate for a temporary connection. For a more permanent connection, add a coupling to fit the #10-32 thread on the Barrel.

Power Supply Requirements

Power supply lines for the Transmitter and the Receiver should each have a pi filter of two 60μF shunt capacitors and a 2.2μH (<1Ω) inductor. The Transmitter needs this filter to prevent transients from reaching other equipment when the LED (or IRED) currents are switched. The Receiver needs the filter to keep line transients from interfering with its extremely sensitive amplifier. In addition, the Receiver may need its own regulator, as shown in the data sheet, to prevent low-frequency transients or ripple from interfering with the data stream. If a regulator is used, the pi filter should be between the regulator output and the Receiver supply terminal. The Transmitter needs no regulator if the supply voltage is in the specified range.

System Performance Evaluation

System performance checks may be done by using error-detection equipment, such as the Hewlett-Packard Mod. 3760A Word Generator and 3761 Error Detector as indicated in Figure 18. The Mod. 3780A Pattern Generator/Error Detector which contains both word generator and error detector is also usable, although it has less flexibility in word generation and a lower data rate capability. These instruments have low-impedance (50Ω and 75Ω) inputs and outputs. The outputs have adequate voltage swing to drive the Fiber Optic Transmitter Data Input, but ringing may occur unless the signal line is properly terminated. The low-impedance inputs require a buffer amplifier between the Receiver output and the Error Detector input. Here also the voltage swing is ample, so a simple emitter follower will do as a buffer.

With Mode Select "low" (on the Fiber Optic Transmitter), the Word Generator may be set for either NRZ or RZ code, and there is no restriction of any kind on word length or composition (pseudo random or selected). With Mode Select "high", the code selection can be either NRZ or RZ but in either code the word composition must be such that:

1. No interval > 5μs of consecutive marks or consecutive spaces
2. Duty factor: .44 < DF < .57 or .75 < k < 1.25

The first condition can be examined with an oscilloscope, but if word length is such that:

$$\frac{\text{word length (bits)}}{\text{data rate (bits/second)}} < 5 \text{ microseconds}$$

then there is no way that any consecutive marks or spaces can extend over 5μs.

The easiest way to check duty factor is by observing k directly on an ac coupled oscilloscope: first establish the baseline position (e.g., center of scope face) with zero signal input, then with the data signal applied:

$$k = \frac{\text{excursion above baseline position}}{\text{excursion below baseline position}}$$

where the oscilloscope deflects upward for positive input. For this observation, the oscilloscope need not be synchronized — it could be free-running. The word composition should be adjusted to bring k within the specified limits. The word composition can be adjusted by adding zeroes, changing word length, or by handselecting the bit sequence.

Either error detector has two modes of operation: BER (Bit Error Rate) mode and "count" mode. The count mode is simplest to use and gives an earlier indication of the result of any system adjustment.

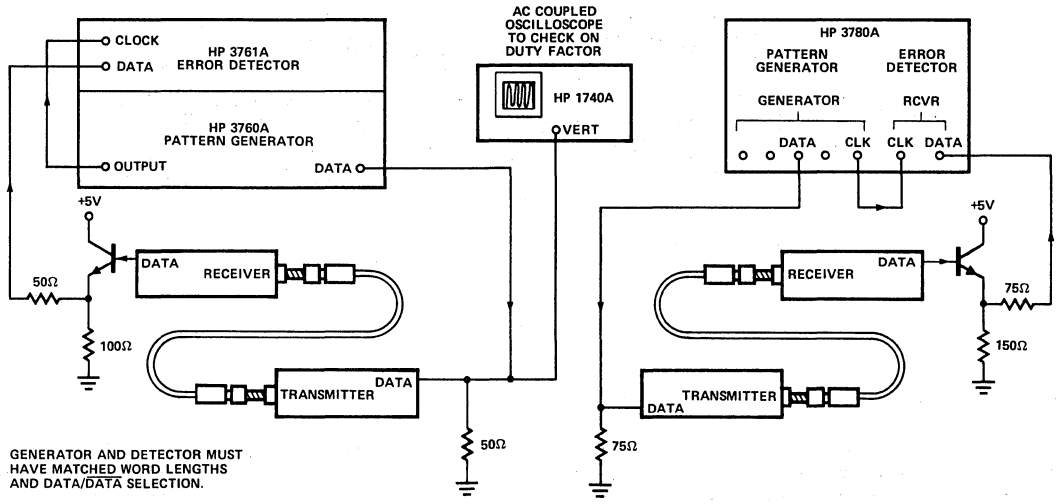


Figure 18. Bit Error Rate Measurement Arrangement.

With the System at normal operating flux level, the error rate is so low that it would take several hours or even days to make an accurate BER measurement. If the flux level is reduced, SNR falls and BER rises until it becomes measurable. Then the error function [see Equation (26)] can be applied to determine the BER at the normal flux level in terms of the ratio ϕ_O/ϕ_N where ϕ_O is the operating flux level and ϕ_N is the flux at the reduced level where the BER was measured. The problem now is that ϕ_N may be too low to measure with equipment at hand. The solution is in the Receiver Test Point voltage, V_T, which varies linearly as Receiver input flux — see Equation (17). But even this method has limits; when the flux becomes a small fraction of a microwatt, the voltage difference ($V_{TMAX} - V_T$) cannot be accurately observed. The solution to this problem is in the Transmitter-to-Cable connection. Just back off the Coupling, noting the number of turns while observing V_T, then plot a curve like that of Figure 19. The curve is quite repeatable if care is taken to avoid backlash and rotation of the Connector Body (rotate Coupling only) but the curve is not the same for each System.

Operating Margin Measurement

The flux budget margin, α_M, for a given P_e can be found using the Connector on the Transmitter as an adjustable attenuator as described above, proceeding as follows:

1. Prepare a curve similar to Figure 19.
2. Count the turns, N, needed to get measurable error, $P_{e,N}$.
3. Find α_N(dB) from N and the curve from Step 1.
4. Find X_N from erfc (X_N) = $P_{e,N}$ (measured).
5. Find X_0 from erfc (X_0) = P_e (given).

$$(27)\ \alpha_M(dB) = \alpha_N - 10 \log \frac{X_0}{X_N} \text{ FOR GIVEN } P_e$$

Absolute flux levels at "N" turns can be found by measuring the flux level when N = 0 and applying a ratio. A rough measurement can be made using the Test Point voltage, V_T, and Equation (15). A more precise measurement requires a calibrated radiometer, such as the EG&G Mod. 550, used as shown in Figure 20a. With its "flat" filter installed, the EG&G Mod. 550 reads the radiant

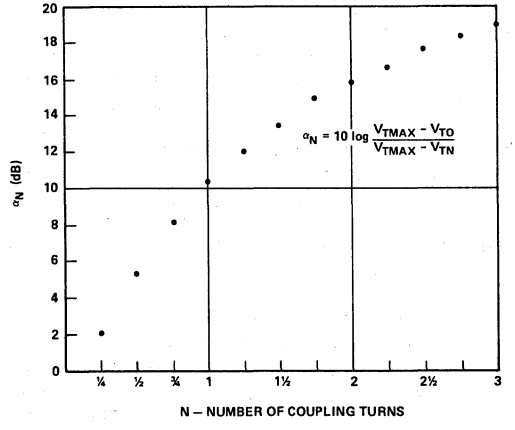
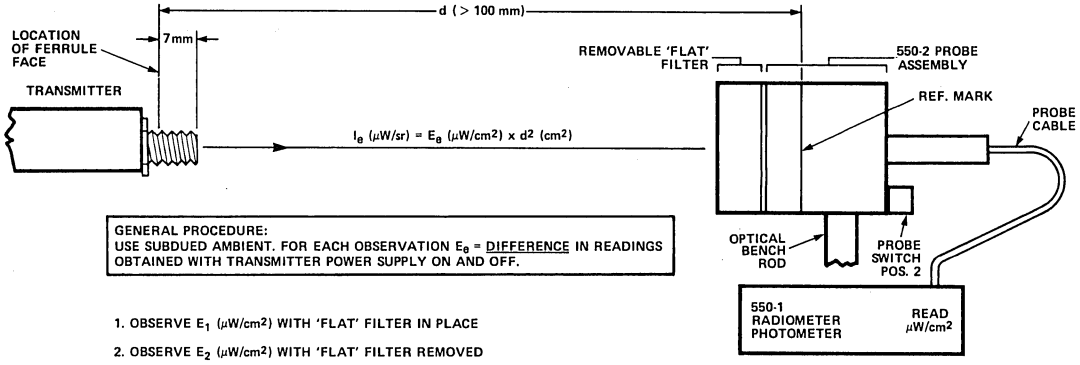


Figure 19. Flux Decoupling by Rotation of Connector Coupling.



GENERAL PROCEDURE:
USE SUBDUED AMBIENT. FOR EACH OBSERVATION E_θ = DIFFERENCE IN READINGS OBTAINED WITH TRANSMITTER POWER SUPPLY ON AND OFF.

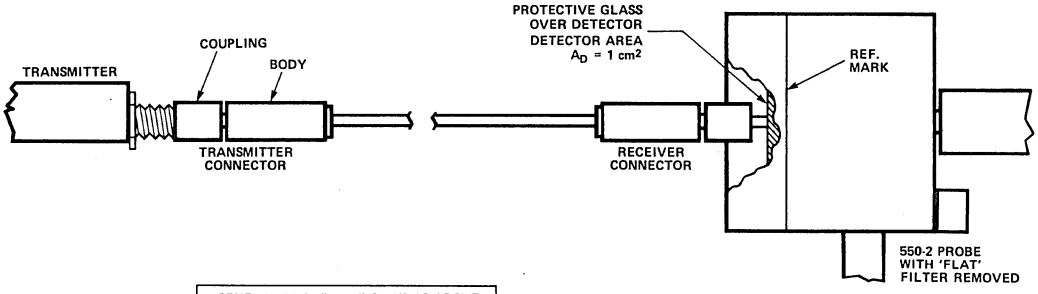
1. OBSERVE E_1 (μW/cm²) WITH 'FLAT' FILTER IN PLACE
2. OBSERVE E_2 (μW/cm²) WITH 'FLAT' FILTER REMOVED

FILTER TRANSMITTANCE: $\tau_F = E_1 / E_2$

AVERAGE FLUX FROM TRANSMITTER: $\phi\ (\mu W) = \left[E_1\left(\frac{\mu W}{cm^2}\right)\right]\left[d^2(cm^2)\right]\left[\left(\frac{\phi}{I}\right)_{MAX}\right]$

$\left(\frac{\phi}{I}\right)_{MAX}$ IS THE MAXIMUM VALUE OF THE RADIATION PATTERN INTEGRAL: $\frac{\phi(\theta)}{I(0)}$ (SEE DATA SHEET)

(a) MEASUREMENT OF TRANSMITTER AVERAGE FLUX



GENERAL PROCEDURE SAME AS ABOVE

3. WITH TRANSMITTER CONNECTOR SEATED, CENTER RECEIVER CONNECTOR OVER DETECTOR, THEN POSITION AGAINST GLASS. (DO NOT SLIDE – SLIDING MAY CAUSE SCRATCH DAMAGE.) OBSERVE E_O (μW/cm²).
4. WITHOUT ROTATING THE BODY, ROTATE THE COUPLING BY SMALL INCREMENTS OF TURNS, NOTING THE NUMBER OF TURNS, N, AND FOR EACH VALUE OF N: OBSERVE E_N (μW/cm²).

RECEIVER INPUT FLUX, AT OPERATING LEVEL $\phi_O\ (\mu W) = \frac{[E_O\ (\mu W/cm^2)]\ [A_D\ (cm^2)]}{\tau_F\ (\text{SEE ABOVE})}$

FLUX DECOUPLING (SEE FIG. 19) $\alpha_N = 10 \log_{10}(E_O / E_N)$

(b) MEASUREMENT OF AVERAGE RECEIVER INPUT FLUX AND FLUX DECOUPLING AT TRANSMITTER CONNECTOR.

Figure 20. Flux Measurement with EG&G Mod 550 Radiometer.

incidance, E, in W/cm² on an aperture area, A_D = 1 cm² and N.A. = 1. With the filter removed, a fiber optic cable can be placed so close to the aperture that there is no flux loss, and since the radiometer N.A. exceeds the fiber N.A., the radiometer will have a reading in W/cm² which is numerically equal to the flux in watts. However, a correction must be made for the removal of the filter.

The insertion loss of the filter must be evaluated at the measurement wavelength because it varies with wavelength to compensate for spectral variation in the response of the silicon detector. The arrangement shown in Figure 20 for measurement of radiant intensity is a good one for measuring insertion loss of the filter. Two observations are made — one with and one without the filter. Error due to ambient radiation is avoided by working in subdued ambient and for each observation taking two radiometer readings (source off and source on); the difference in readings is the observation of the radiant incidance, E_e, produced by the radiant intensity, I_e, of the source. The ratio of the two observations gives:

$$(28)\ \text{FILTER INSERTION LOSS, } \alpha_F = 10 \log \frac{E_{e(\text{filter out})}}{E_{e(\text{filter in})}}$$

This same arrangement can be used to measure the average flux of the Transmitter as shown in Figure 20b. From the observation of E_e with the filter IN:

$$(29)\ \text{AVERAGE INTENSITY, } I_e\left(\frac{\mu W}{sr}\right) = E_e\left(\frac{\mu W}{cm^2}\right) \times d^2\ (cm^2)$$

$$(30)\ \text{AVERAGE FLUX, } \phi_e(\mu W) = I_e \left(\frac{\mu W}{sr}\right)\left[\frac{\phi(\theta)}{I(0)}\ (MAX)\right]$$

(from Equation (29); value from radiation pattern integral in Transmitter Data Sheet)

SYSTEM MAINTENANCE

Preventive Maintenance

Long-term degradation occurs in any LED and LED degradation affects the Hewlett-Packard Fiber Optic System in two ways: reduced average flux, affecting either externally- or internally-coded mode, and altered flux excursion ratio, affecting only the internally-coded mode. Significant degradation of either the flux or the flux excursion ratio can be detected by regular observation of the flux margin, α_M, and of k.

α_M is evaluated as explained under Operating Margin Measurement from Equation (27). A plot of α_M against the logarithm of the cumulative hours of operation will allow an estimate to be made of the operating time remaining until α_M = 0 FOR THE P_e DESIRED.

k must be evaluated by measuring ϕ_H, ϕ_M, and ϕ_L as explained in the Transmitter description. The Test Point voltage can be used in making this measurement — see Equation (15). The upper and lower margins on k for a particular Receiver can be found by operating the Transmitter with Mode Select "high" and a rectangular signal (f ≈ 500kHz) at Data Input. As the duty factor of the signal is varied, the limits on k are found as those at which the Receiver fails to follow the Data Input signal.

$$(31)\ k = \left(\frac{1}{ft_P}\right) - 1 = \frac{1}{\frac{1}{ft_N} - 1}$$

where ft_P is the positive-pulse duty factor
ft_N is the negative-pulse duty factor

Changes in k do not affect externally-coded mode performance, and if this mode is used, then flux margin, α_M, is the only concern.

Corrective Maintenance

Trouble in the System may range from complete breakdown to excessive BER. The flux used in the Hewlett-Packard System is visible so the cause of complete breakdown can sometimes be localized by simply looking at the output of the Cable and the Transmitter. If there is visible output from the cable, then, when the Cable is connected to the Receiver, there should be an 8mV change in Test Point voltage, V_T, as the Transmitter (Mode Select "low") is turned on and off by switching V_{CC}. If ΔV_T is more than 8mV but the system is not working, then either the Receiver logic is not functioning properly or the flux excursion ratio, k, is either too high or too low. Excursion ratio can be checked as described above, using V_T. If k is satisfactory, the logic malfunction could be due to incorrect supply voltage or output loading.

If the System is functioning but has excessive BER, either the flux and flux excursion ratio are marginal (can be checked as described above) or there is too much interference from noise or other effects. If the Data Input voltage levels are correct, either random noise is high or errors are occurring due to incorrect supply voltage or output loading, or due to noise on the supply line. Random noise effects can be checked by lowering the flux level to a point where P_e is measurably high. If P_e varies with flux level according to P_e = erfc(X), as in Equation (26), then the problem is excessive random noise. Random noise can also be checked by changing the data rate while the flux level is low enough to make P_e measurable. If P_e is the same at any data rate, the problem is excessive random noise. Excessive random noise is more likely to occur in the Receiver than in the Transmitter; the best way to check is by replacement of the Receiver. Noise on the supply line is difficult to trace. If there is any doubt, the Receiver should be operated from its own supply (e.g., a 5V regulator). Receiver noise should be low enough to make $P_e < 10^{-9}$ at 10 Mbaud with normal flux level ($\Delta V_T > 8$ mV by the method described above indicates normal flux level).

HEWLETT hp PACKARD

COMPONENTS

NEW PRODUCT APPLICATION

APPLICATION NOTE 1001

Interfacing the HDSP-2000 to Microprocessor Systems

INTRODUCTION

Over the past two years, the need for alphanumeric displays has grown very rapidly due to the extensive use of microprocessors in new systems design. The presence of the microprocessor in such systems substantially simplifies the traditionally difficult task of designing an alphanumeric display into a system. This task is further simplified by using a display element such as the HDSP-2000 which has in one package a four character display, as well as most of the basic electronics necessary to drive the display. Depending upon overall systems configuration, microprocessor time available to dedicate to display support, and the type of information to be displayed, one may choose several different partitioning schemes to drive such a display.

This note will deal with four different techniques (see Figure 1) for interfacing the HDSP-2000 display to microprocessor systems:

1. The REFRESH CONTROLLER interrupts the microprocessor at a 500 Hz rate to request refresh data for the display.
2. The DECODED DATA CONTROLLER accepts 5 x 7 matrix data from the microprocessor and then automatically refreshes the display with the same information until new data is supplied by the microprocessor.
3. The RAM CONTROLLER accepts ASCII data and interfaces like a RAM to the microprocessor.
4. The DISPLAY PROCESSOR CONTROLLER (HDSP-247X series) employs a dedicated single chip microprocessor as a data display/control/keyboard interface which has many of the features of a complete terminal.

The interface techniques depicted are specifically for the 8080A or 6800 microprocessor families. Extension of these techniques to other processors should be a relatively simple software chore with little or no hardware changes required.

COMPARISON OF INTERFACE TECHNIQUES

The choice of a particular interface is an important consideration because it affects the design of the entire microprocessor system. The REFRESH CONTROLLER provides the lowest cost interface because it uses the microprocessor to provide ASCII decoding and display strobing. Because the ASCII decoder is located within the microprocessor system, the designer has total control over the display font within the program. This feature is particularly important when the system will be used to display different languages and special graphic symbols. However, the REFRESH CONTROLLER requires a significant amount of microprocessor time. Furthermore, while the interrupt allows the refresh program to operate asynchronously from the main program, this technique limits some of the software techniques that can be used in the main program.

The DECODED DATA CONTROLLER requires microprocessor interaction only when the display message is changed. Like the REFRESH CONTROLLER, the ASCII decoder is located within the microprocessor program. However, the time required to decode the ASCII string and store the resulting 5 x 7 display data into the interface requires several milliseconds of microprocessor time.

The RAM CONTROLLER also requires interaction from the microprocessor system only when the display message is changed. Because the ASCII decoder is located within the display interface, the microprocessor requires much less time to load a new message into the display.

The DISPLAY PROCESSOR CONTROLLER, the HDSP-247X series, is the most powerful interface. The software within the DISPLAY PROCESSOR CONTROLLER further reduces the microprocessor interaction by providing more powerful left and right data entry modes compared to the RAM entry mode of the DECODED DATA and RAM CONTROLLERS. The DISPLAY PROCESSOR CONTROLLER can also provide features such as a Blinking Cursor, Editing Commands, and a Data Out function. One version of the DISPLAY PROCESSOR CONTROLLER allows the user to provide a custom ASCII decoder for applications needing a special character font.

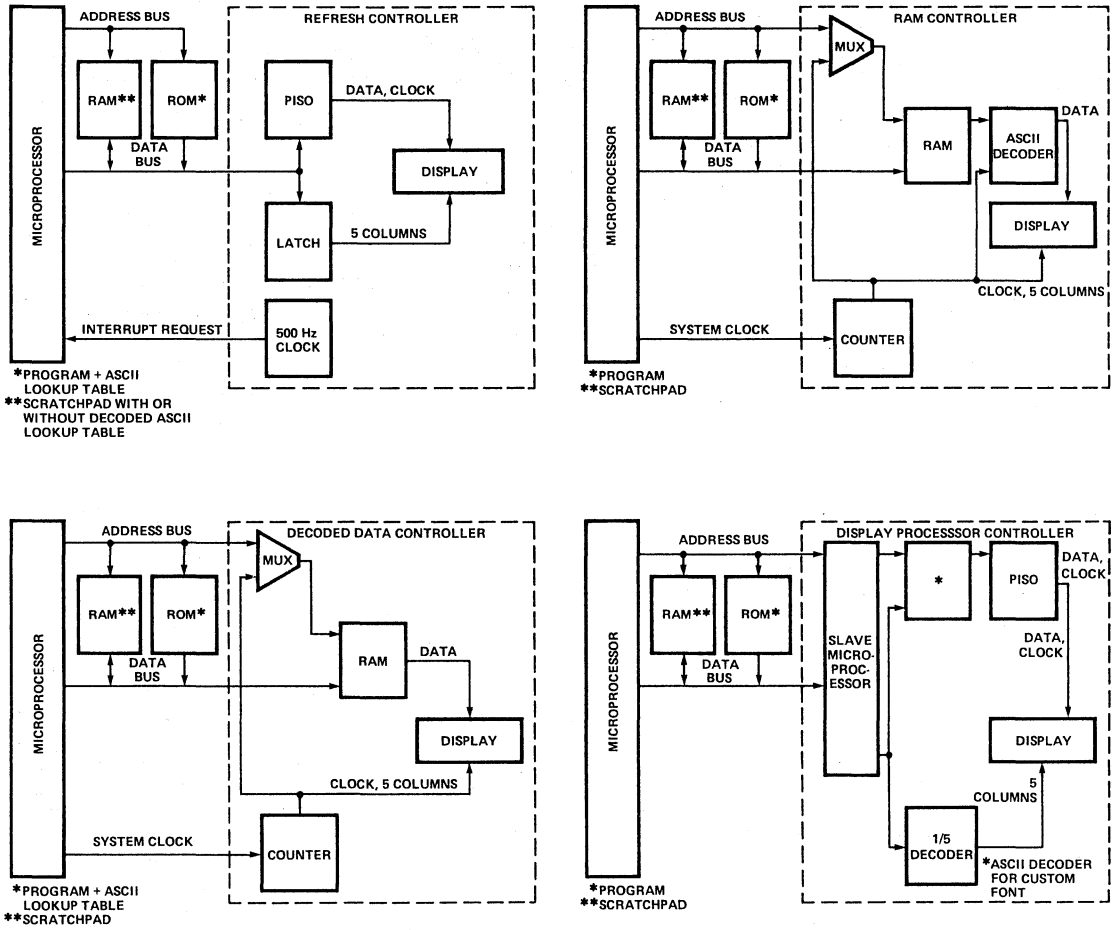


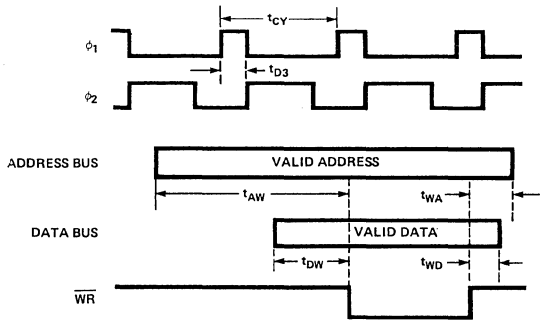
Figure 1. Four Different Techniques to Interface the HDSP-2000 Alphanumeric Display to a Microprocessor System

MICROPROCESSOR OVERVIEW

In order to effectively utilize the interface techniques listed above, an understanding of microprocessor fundamentals is required. A microprocessor system usually consists of a microprocessor, ROM memory, RAM memory, and some specific I/O interface. The microprocessor performs the desired system function by executing a program stored within the ROM. The RAM memory is used to provide a stack for the microprocessor, as well as a temporary scratchpad memory. The I/O interface consists of circuitry that is used as an input to the system as well as an output from the system. The alphanumeric display subsystem would be considered part of this interface. The microprocessor interfaces to this system through an Address Bus, a Data Bus, and a Control Bus. The Address Bus consists of several outputs from the microprocessor (A_0, A_1...A_n) which collectively specify a binary number. This number or "address" uniquely specifies each word in the ROM memory, RAM memory, and I/O interface. The Data Bus consists of several lines from the microprocessor which are used both as inputs and outputs. The Data Bus serves as an input during a memory or I/O read operation and as an output for a memory or I/O write operation. The Control Bus provides the required signals and timing to the rest of the microprocessor system to distinguish a memory read from a memory write, and in some systems an I/O read from an I/O write. These control lines and the timing between the Address, Data, and Control Buses vary for different microprocessors.

For the 8080A microprocessor, the Address Bus consists of 16 lines, the Data Bus consists of 8 lines, and the Control Bus consists of several lines including DBIN (Data Bus In), $\overline{WR}$ (Write), and clock signals ϕ_1 and ϕ_2. DBIN and $\overline{WR}$ are used to specify a memory read or write. The 8080A microprocessor provides several other control lines which are usually decoded with DBIN and $\overline{WR}$ to generate composite control signals $\overline{MEM\ R}$ (Memory Read), $\overline{MEM\ W}$ (Memory Write), $\overline{I/O\ R}$ (I/O Read), and $\overline{I/O\ W}$ (I/O Write). Since the alphanumeric display subsystem is an

output of the microprocessor system, the timing between the Address Bus, Data Bus, and $\overline{WR}$ is of particular significance. This timing is generalized in Figure 2.



8080 MICROPROCESSOR WITH 8228 CLOCK	MINIMUM TIMES (ns)			
	t_{AW}	t_{WA}	t_{DW}	t_{WD}
8080A, t_{CY} = 480	740	90	230	90
8080A-2, t_{CY} = 380	560	80	140	80
8080A-1, t_{CY} = 320	470	70	110	70

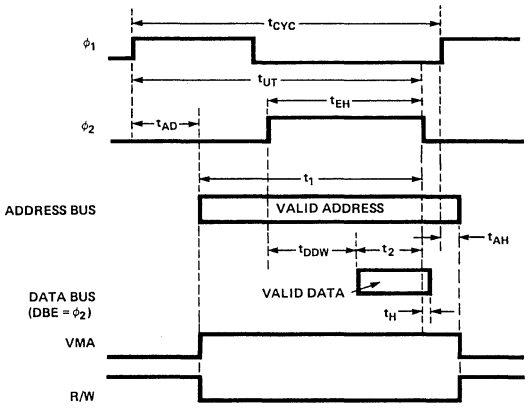
$t_{AW} = 2t_{CY} - t_{D3} - [140(A), 130(A\text{-}2), 110(A\text{-}1)]$

$t_{WA} = t_{WD} = t_{D3} + 10$

$t_{DW} = t_{CY} - t_{D3} - [170(A), 170(A\text{-}2), 150(A\text{-}1)]$

From INTEL Component Data Catalog, 1978

Figure 2. Memory Write Timing for the Intel 8080A Microprocessor Family



6800 MICROPROCESSOR	MINIMUM TIMES (ns)			
	t_1	t_{AH}	t_2	t_H
6800, t_{CYC} = 1000	630	30	225	10
68A00, t_{CYC} = 666	420	30	80	10
68B00, t_{CYC} = 500	290	30	60	10

$t_1(MIN) = t_{UT}(MIN) - t_{AD}(MAX)$

$t_2(MIN) = t_{EH}(MIN) - t_{DDW}(MAX)$

From MOTOROLA Semiconductor MC6800 Data Sheet (DS9471), 1978

Figure 3. Memory Write Timing for the Motorola 6800 Microprocessor Family

The 6800 microprocessor has a 16 line Address Bus, 8 line Data Bus, and a Control Bus that includes the signals VMA (Valid Memory Address), R/W (Read/Write), DBE (Data Bus Enable), and clock signals ϕ_1 and ϕ_2. R/W specifies either a memory read or write while VMA is used in conjunction with R/W to specify a Valid Memory Address. DBE gates the internal data bus of 6800 into the Data Bus. In many applications, DBE is connected to ϕ_2. The timing between the Address Bus, Data Bus, VMA, and R/W (when DBE = ϕ_2) is shown in Figure 3. Additional data hold time, t_H, can be achieved by delaying ϕ_2 to the microprocessor or by extending DBE beyond the falling edge of ϕ_2.

The ASCII to 5 x 7 dot matrix decoder used by the REFRESH CONTROLLER and DECODED DATA CONTROLLER is located within the microprocessor program. This decoder requires 640 bytes of storage to decode the 128 character ASCII set. The decoder used by these controllers is formatted so that the first 128 bytes contain column 1 information; the next 128 bytes contain column 2 information, etc. Each byte of this decoder is formatted such that D_6 through D_0 contain Row 7 through Row 1 display data respectively. The data is coded so that a HIGH bit would turn the corresponding 5 x 7 display dot ON. This decoder table is shown in Figure 20. The resulting 5 x 7 dot matrix display font is shown in the HDSP-2471 data sheet.

REFRESH CONTROLLER

The REFRESH CONTROLLER circuit depicted in Figure 4 is designed for interface to either 6800 or 8080A microprocessors. This circuit operates by interrupting the microprocessor every two milliseconds to request a new block of display data and column select data. Display data is loaded from the data bus into the serial input of the HDSP-2000 via a 74165 parallel in, serial out shift register. The 74LS293 counter and associated gates insure that only seven clock pulses are delivered to the shift register and the HDSP-2000 for each word loaded. Column Select data is loaded into a 74174 latch which, in turn, drives the column switch transistors. The circuit timing relative to the microprocessor clock and I/O is depicted in Figure 5.

The 6800 software necessary to support this interface is divided into two separate subroutines, "RFRSH" and "LOAD" (Figure 6). This approach is desirable to minimize microprocessor involvement during display refresh. The subroutine "RFRSH" loads a new set of decoded display data from the microprocessor scratchpad memory into the interface at each interrupt request. The subroutine "LOAD" is utilized to decode a string of 32 ASCII characters into 5 x 7 formatted display data and store this data in the scratchpad memory used by "RFRSH".

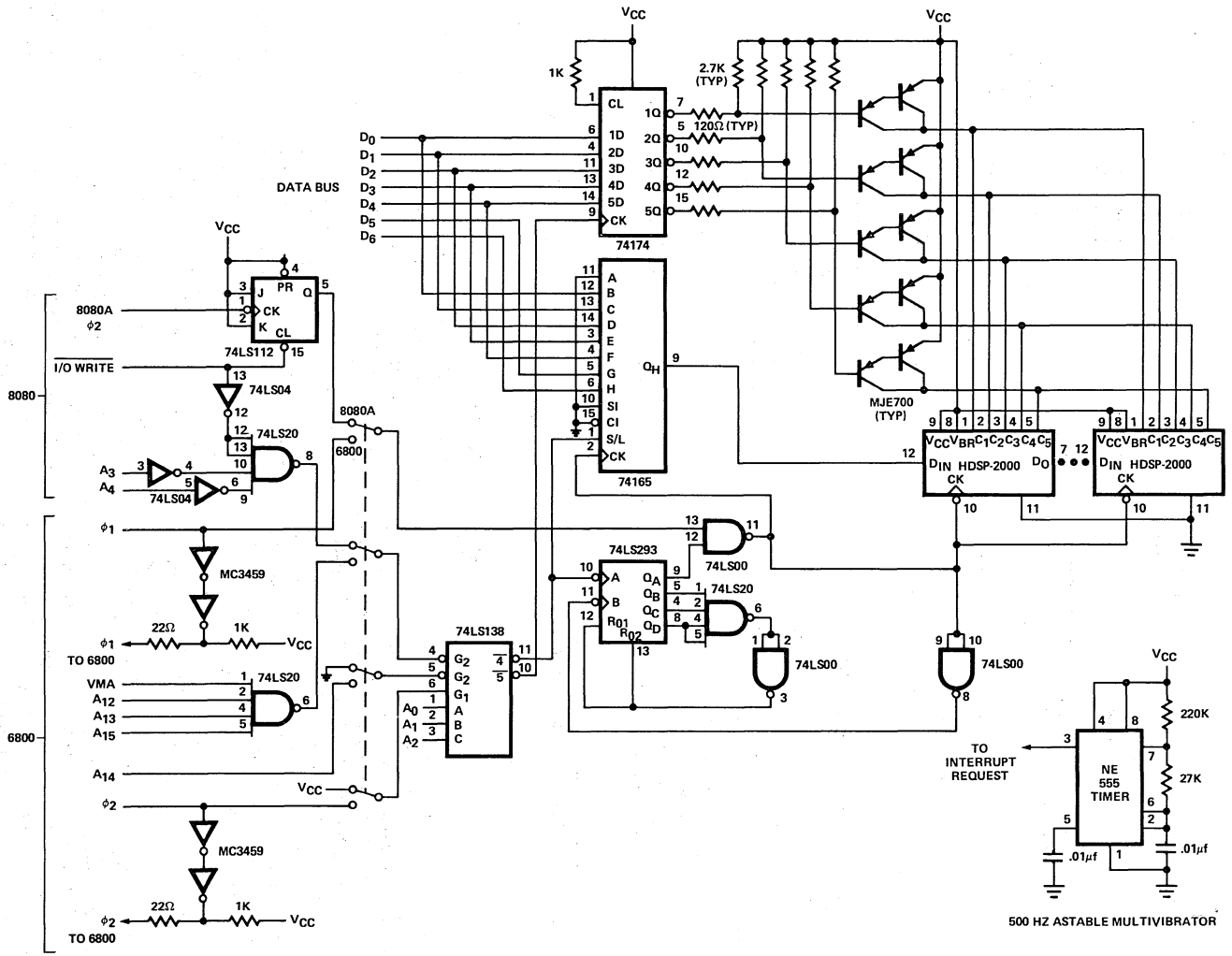


Figure 4. 6800 or 8080A Microprocessor Interface to the HDSP-2000 REFRESH CONTROLLER

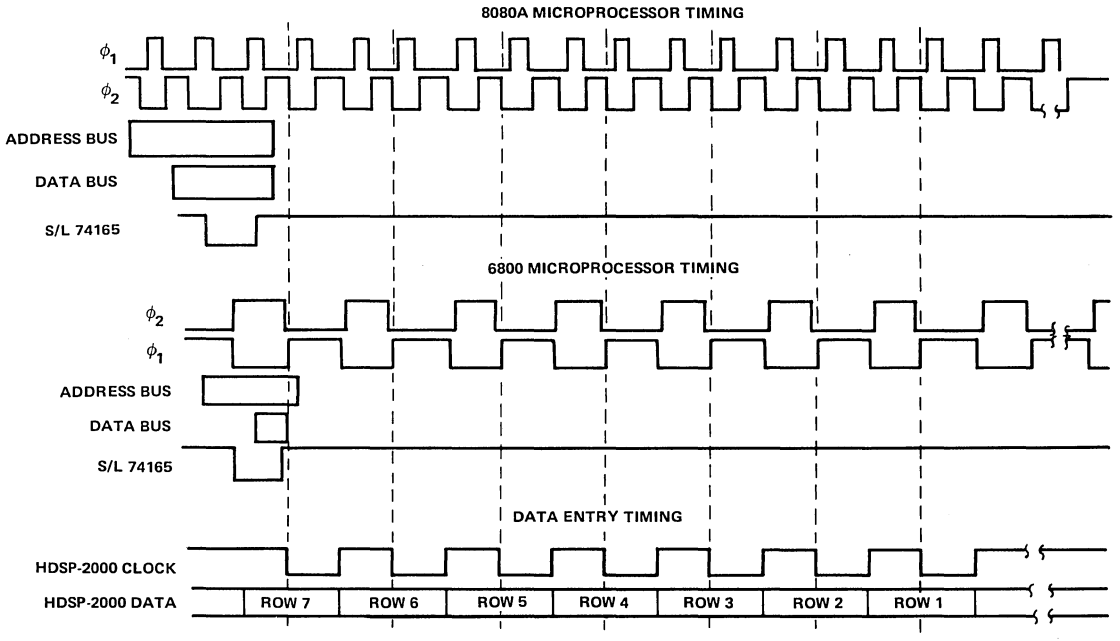


Figure 5. REFRESH CONTROLLER Timing

Figures 7a and 7b depict two different software routines for interfacing the REFRESH CONTROLLER to an 8080A microprocessor. The two subroutines shown in Figure 7a are functional replacements for the 6800 program shown in Figure 6. The programs shown in Figures 6 and 7a require a 5n byte scratchpad memory where n is the display length. The routine in Figure 7b eliminates this scratchpad memory by decoding and loading data each time a new interrupt request is received.

Because the microprocessor system is interrupted every 2ms, proper software design is especially important for the REFRESH CONTROLLER. The use of the scratchpad memory significantly reduces the time required to refresh the display. The fastest program, shown in Figure 6, uses in-line code to access data from the buffer and output it to the display. This program requires 3.7% + .50n% of the available microprocessor time for a 1MHz clock. The program shown in Figure 7a is similar to the one shown in Figure 6, except that it uses a program loop instead of the in-line code. This program uses 5.4% + .93n% of the microprocessor time for a 2MHz clock. These programs utilize a subroutine "LOAD" which is called whenever the display message is changed. This subroutine executes in 10.2ms and 7.5ms respectively for Figure 6 and Figure 7a. The program in Figure 7b uses 7.6% + 1.35n% of the microprocessor time for a 2MHz clock. A 50% reduction in the previously described microprocessor times can be achieved by using faster versions of the 6800 and 8080A microprocessors.

```
LOC   OBJECT CODE     SOURCE STATEMENTS
                      *
                      *
      BF 05           CDVR    EQU     $BF05
      BF 04           RDVR    EQU     $BF04
      06 00           DECDR   EQU     $0600
0000                  POINT   RMB     2
0002                  COLMN   RMB     1
0003                  COUNT   RMB     2

0005  00 AD           ASCII   FDB     DATA
0007                  DISPNT  RMB     2
0009                  DCRPNT  RMB     2
000B                  COLCNT  RMB     1
000C                  DIGCNT  RMB     1

000D                  BUFFR   RMB     160
00AD                  DATA    RMB     32

0400                          ORG     $0400
0400  86 FF           RFRSH   LDA A   I, $FF
0402  B7 BF 05                STA A   E, CDVR
0405  DE 00                   LDX     D, POINT
0407  A6 00           LOOPHH  LDA A   X, 0
0409  B7 BF 04                STA A   E, RDVR
040C  A6 01                   LDA A   X, 1
040E  B7 BF 04                STA A   E, RDVR
                              •
                              •
                              •
04A2  A6 1F                   LDA A   X, 31
04A4  B7 BF 04                STA A   E, RDVR
04A7  96 02                   LDA A   D, COLMN
04A9  B7 BF 05                STA A   E, CDVR
04AC  81 EF                   CMP A   I, $EF
04AE  27 10                   BEQ     LOOPB
04B0  D6 00                   LDA B   D, POINT +1
04B2  CB 20                   ADD B   I, 32
04B4  D7 00                   STA B   D, POINT +1
04B6  24 03                   BCC     LOOPA
04B8  7C 00 00                INC     E, POINT
04BB  0D              LOOPA   SEC
04BC  79 00 02                ROL     E, COLMN
04BF  3B                      RTI
04C0  CE 00 0D LOOPB          LDX     I, BUFFR
04C3  DF 00                   STX     D, POINT
04C5  DE 03                   LDX     D, COUNT
04C7  09                      DEX
04C8  DF 03                   STX     D, COUNT
04CA  86 FE                   LDA A   I, $FE
04CC  97 02                   STA A   D, COLMN
04CE  3B                      RTI

04CF  5F              LOAD    CLR B
04D0  CE 00 0D                LDX     I, BUFFR
04D3  DF 07                   STX     D, DISPNT
04D5  86 06                   LDA A   I, <DECDR
04D7  97 09                   STA A   D, DCRPNT
04D9  86 05                   LDA A   I, 5
04DB  97 0B                   STA A   D, COLCNT
04DD  86 20           LOOP1   LDA A   I, 32
04DF  97 0C                   STA A   D, DIGCNT
04E1  9B 06                   ADD A   D, ASCII+1
04E3  24 03                   BCC     LOOP2
04E5  7C 00 05                INC     E, ASCII
04E8  97 06           LOOP2   STA A   D, ASCII+1
04EA  DE 05           LOOP3   LDX     D, ASCII
04EC  09                      DEX
04ED  A6 00                   LDA A   X, 0
04EF  DF 05                   STX     D, ASCII
04F1  1B                      ABA
04F2  97 0A                   STA A   D, DCRPNT+1
04F4  DE 09                   LDX     D, DCRPNT
04F6  A6 00                   LDA A   X, 0
04F8  DE 07                   LDX     D, DISPNT
04FA  A7 00                   STA A   X, 0
04FC  08                      INX
04FD  DF 07                   STX     D, DISPNT
04FF  7A 00 0C                DEC     E, DIGCNT
0502  26 E6                   BNE     LOOP3
0504  CB 80                   ADD B   I, $80
0506  24 03                   BCC     LOOP4
0508  7C 00 09                INC     E, DCRPNT
050B  7A 00 0B LOOP4          DEC     E, COLCNT
050E  26 CD                   BNE     LOOP1
0510  39                      RTS
```

Figure 6. 6800 Microprocessor Program Utilizing a 160 Byte RAM Buffer that Interfaces to the REFRESH CONTROLLER

```
LOC   OBJECT CODE     SOURCE STATEMENTS
0004                  RDVR    EQU     0004H
0005                  CDVR    EQU     0005H
E500                  DECDR   EQU     0E500H

                              ORG     0E000H
E000  05 E0           POINT   DW      BUFFR
E002  FE              COLMN   DB      0FEH
E003  FF FF           COUNT   DW      0FFFFH
E005  00              BUFFR   DS      160

                              ORG     0E0A5H
E0A5  A7 E0           ASCII   DW      DATA
E0A7  00              DATA    DS      32

                              ORG     0E400H
E400  F5              RFRSH   PUSH    PSW
E401  C5                      PUSH    B
E402  E5                      PUSH    H
E403  2A 00 E0                LHLD    POINT
E406  06 20                   MVI     B, 32
E408  3E FF                   MVI     A, 0FFH
E40A  D3 05                   OUT     CDVR
F40C  7E              LOOP    MOV     A, M
E40D  D3 04                   OUT     RDVR
E40F  23                      INX     H
E410  05                      DCR     B
E411  C2 0C E4                JNZ     LOOP
E414  3A 02 E0                LDA     COLMN
E417  D3 05                   OUT     CDVR
E419  FE EF                   CPI     0EFH
E41B  CA 28 E4                JZ      FIRST
E41E  22 00 E0                SHLD    POINT
E421  07                      RLC
E422  32 02 E0                STA     COLMN
E425  C3 3A E4                JMP     END
E428  21 05 E0 FIRST          LXI     H, BUFFR
E42B  22 00 E0                SHLD    POINT
E42E  3E FE                   MVI     A, 0FEH
E430  32 02 E0                STA     COLMN
E433  2A 03 E0                LHLD    COUNT
E436  2B                      DCX     H
E437  22 03 E0                SHLD    COUNT
E43A  E1              END     POP     H
E43B  C1                      POP     B
E43C  F1                      POP     PSW
E43D  C9                      RET

E43E  11 24 E0 LOAD           LXI     D, BUFFR+31
E441  0E 20                   MVI     C, 32
E443  2A A5 E0 LOOP1          LHLD    ASCII
E446  7E                      MOV     A, M
E447  23                      INX     H
E448  22 A5 E0                SHLD    ASCII
E44B  26 E5                   MVI     H, DECDR/256
E44D  6F                      MOV     L, A
E44E  06 05                   MVI     B, 5
E450  7E              LOOP2   MOV     A, M
E451  12                      STAX    D
E452  7D                      MOV     A, L
E453  C6 80                   ADI     80H
E455  6F                      MOV     L, A
E456  D2 5A E4                JNC     LOOP3
E459  24                      INR     H
E45A  7B              LOOP3   MOV     A, E
E45B  C6 20                   ADI     32
E45D  5F                      MOV     E, A
E45E  05                      DCR     B
E45F  C2 50 E4                JNZ     LOOP2
E462  7B                      MOV     A, E
E463  C6 5F                   ADI     5FH
E465  5F                      MOV     E, A
E466  0D                      DCR     C
E467  C2 43 E4                JNZ     LOOP1
E46A  C9                      RET
```

Figure 7a. 8080A Microprocessor Program Utilizing a 160 Byte RAM Buffer that Interfaces to the REFRESH CONTROLLER

```
LOC   OBJECT CODE     SOURCE STATEMENTS

0004                  RDVR    EQU     0004H
0005                  CDVR    EQU     0005H
E500                  DECDR   EQU     0E500H

                              ORG     0E000H
E000  07 E0           ASCII   DW      DATA
E002  FE              COLMN   DB      0FEH
E003  FF FF           COUNT   DW      0FFFFH
E005  00 E5           BASE    DW      DECDR
E007  00              DATA    DS      32

                      ORG             0E400H
E400  F5              RFRSH   PUSH    PSW
E401  C5                      PUSH    B
E402  D5                      PUSH    D
E403  E5                      PUSH    H
E404  2A 05 E0                LHLD    BASE
E407  EB                      XCHG
E408  2A 00 E0                LHLD    ASCII
E40B  01 1F 00                LXI     B, 31
E40E  09                      DAD     B
E40F  43                      MOV     B, E
E410  0E 20                   MVI     C, 32
E412  3E FF                   MVI     A, 0FFH
E414  D3 05                   OUT     CDVR
E416  78              LOOP    MOV     A, B
E417  86                      ADD     M
E418  5F                      MOV     E, A
E419  1A                      LDAX    D
E41A  D3 04                   OUT     RDVR
E41C  2B                      DCX     H
E41D  0D                      DCR     C
E41E  C2 16 E4                JNZ     LOOP
E421  EB                      XCHG
E422  3A 02 E0                LDA     COLMN
E425  D3 05                   OUT     CDVR
E427  FE EF                   CPI     0EFH
E429  CA 3B E4                JZ      FIRST
E42C  07                      RLC
E42D  32 02 E0                STA     COLMN
E430  68                      MOV     L, B
E431  01 80 00                LXI     B, 0080H
E434  09                      DAD     B
E435  22 05 E0                SHLD    BASE
E438  C3 4D E4                JMP     END
E43B  3E FE           FIRST   MVI     A, 0FEH
E43D  32 02 E0                STA     COLMN
E440  21 00 E5                LXI     H, DECDR
E443  22 05 E0                SHLD    BASE
E446  2A 03 E0                LHLD    COUNT
E449  2B                      DCX     H
E44A  22 03 E0                SHLD    COUNT
E44D  E1              END     POP     H
E44E  D1                      POP     D
E44F  C1                      POP     B
E450  F1                      POP     PSW
E451  C9                      RET
```

Figure 7b. 8080A Microprocessor Program that Decodes a 32 Character ASCII String Prior to Loading into the REFRESH CONTROLLER

DECODED DATA CONTROLLER

The DECODED DATA CONTROLLER circuit schematic for a 32 character display is depicted in Figure 8. The circuit is specifically designed for interface to an 8080A microprocessor. This circuit is designed to accept and store in local memory all of the display data for a 32 character HDSP-2000 display (1120 bits). The microprocessor loads 160 bytes of display data into the two 1K x 1 RAM's via the 74165 parallel in, serial out shift register. Each byte of data represents one column of display data. The counter string automatically generates the proper address location for each serial bit of data after initialization by MEM W, the character address, and the desired column. Once the loading is complete, the counter sequentially loads and displays each column (224 bits) of data at a 90Hz rate (2MHz input clock rate). The timing for this circuit is shown in Figure 9. The software required to decode a 32 character ASCII string is shown in Figure 10. This program decodes the 32 ASCII characters into 160 bytes of display data which are then stored in the controller. The program requires about 6.6ms, for a 2MHz clock, to decode and load the message into the DECODED DATA CONTROLLER.

RAM CONTROLLER

The RAM CONTROLLER (Figure 11a) is designed to accept ASCII coded data for storage in a local 128 x 8 RAM. After the microprocessor has loaded the RAM, local scanning circuitry controls the decoding of the ASCII, the display data loading, and the column select function. With minor modification, the circuit can be utilized for up to 128 display characters. The RAM used in this circuit is an MCM6810P with the Address and Data inputs isolated via 74LS367 tristate buffers. This allows the RAM to be accessed either by the microprocessor or by the local electronics. The protocol is arranged such that the microprocessor always takes precedence over the local scanning electronics. The "Write" cycle timing for the RAM CONTROLLER is depicted in Figure 11b. This circuit, as with the DECODED DATA CONTROLLER, requires no microprocessor time once the local RAM has been loaded with the desired data.

DISPLAY PROCESSOR CONTROLLER

The previously mentioned interface techniques provide only for the display of ASCII coded data. Such important features as a blinking cursor, editing routines, and character addressing must be provided by other subroutines in the microprocessor software. The DISPLAY PROCESSOR CONTROLLER is a system which utilizes a dedicated 8048 single chip microprocessor to provide these important features. This controller, as depicted in Figure 12, is a series of printed circuit board subsystems available from Hewlett-Packard under the following part numbers:

HDSP-2470 — Controller with 64 character ASCII to 5 x 7 decoder
HDSP-2471 — Controller with 128 character universal ASCII to 5 x 7 decoder
HDSP-2472 — Controller with socket for user supplied custom coded ROM/PROM/EPROM.

All of the controllers have the following features:

- Choice of character string length:
  4-48 characters in increments of four characters
- Four modes of data entry
  Left Entry
  Right Entry
  RAM Entry (≤ 32 characters only)
  Block Entry
- Flashing Cursor — Left Entry Only
- Data Out (≤ 32 characters only)
- Edit Functions
  Clear Display, Backspace Cursor — RIGHT ENTRY
  Forwardspace Cursor, Insert, Delete — LEFT ENTRY

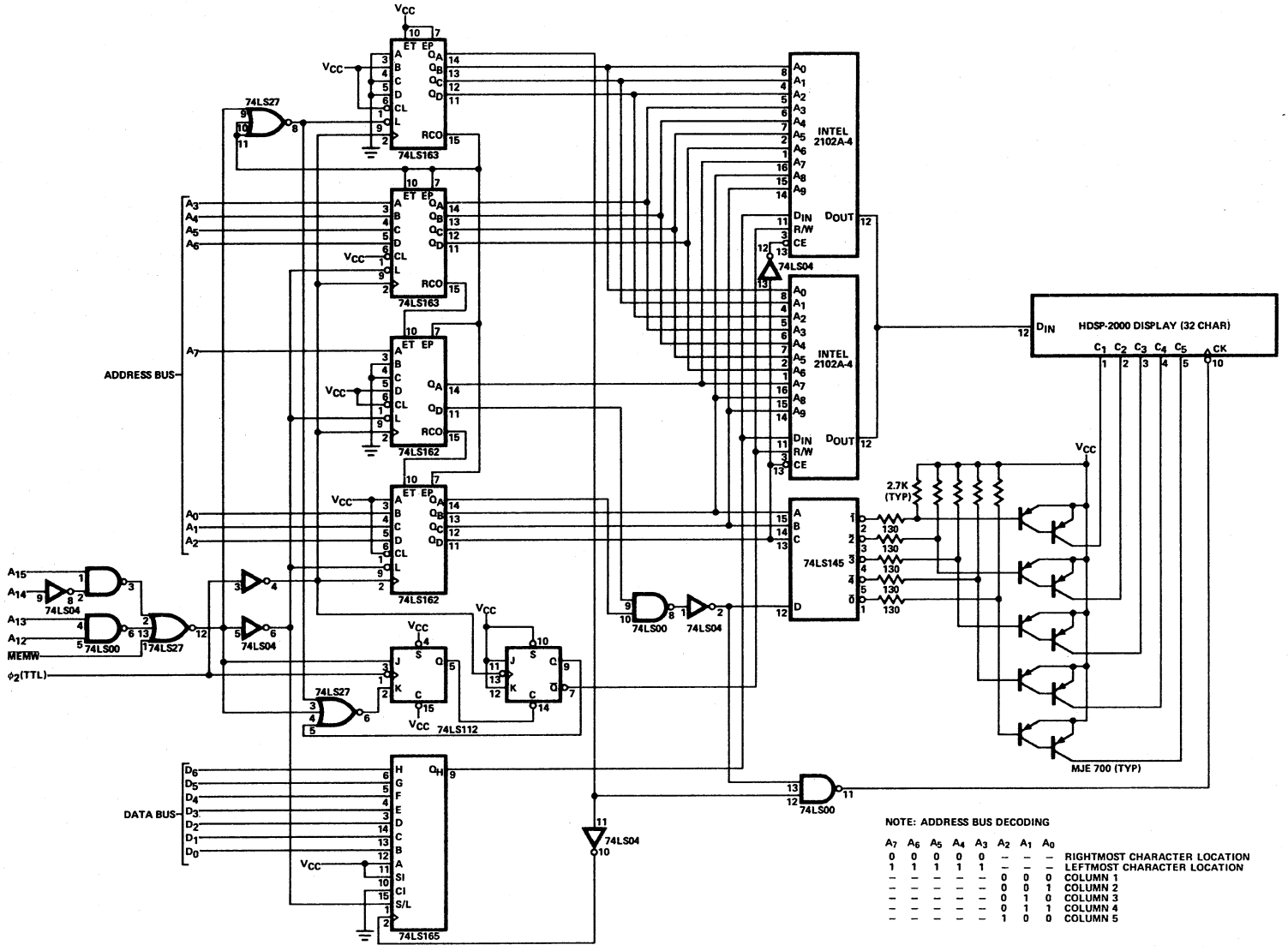


Figure 8. 8080A Microprocessor Interface to the HDSP-2000 DECODED DATA CONTROLLER

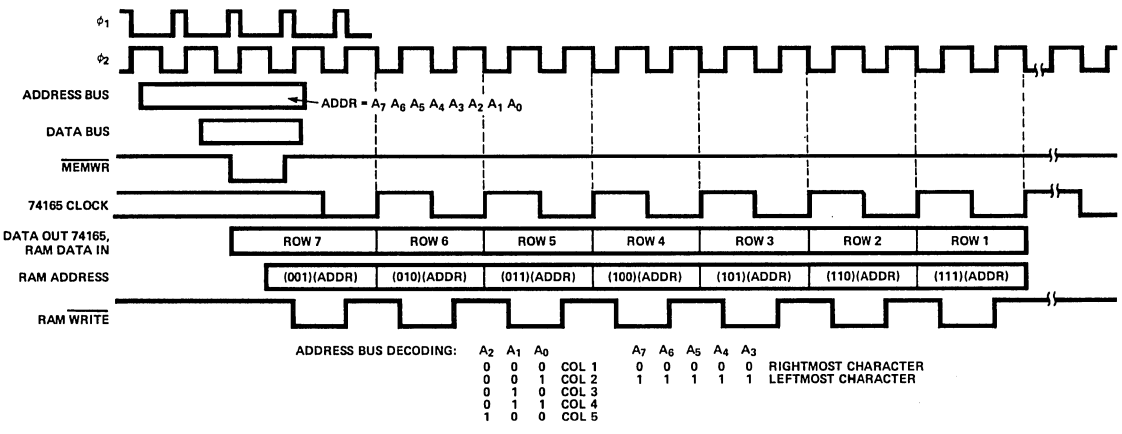


Figure 9. Data Entry Timing for DECODED DATA CONTROLLER

```
LOC   OBJECT CODE     SOURCE STATEMENTS

B000                  DISPL   EQU     0B000H
E500                  DECDR   EQU     0E500H

                      ORG     0E000H
E000  02 E0           ASCII   DW      DATA
E002  00              DATA    DS      32

                      ORG     0E400H
E400  11 F8 B0        LOAD    LXI     D, DISPL+00F8H
E403  0E 20                   MVI     C, 32
E405  2A 00 E0        LOOP1   LHLD    ASCII
E408  7E                      MOV     A, M
E409  23                      INX     H
E40A  22 00 E0                SHLD    ASCII
E40D  26 E5                   MVI     H, DECDR/256
E40F  6F                      MOV     L, A
E410  06 05                   MVI     B, 5
E412  7E              LOOP2   MOV     A, M
E413  12                      STAX    D
E414  13                      INX     D
E415  7D                      MOV     A, L
E416  C6 80                   ADI     80H
E418  6F                      MOV     L, A
E419  D2 1D E4                JNC     LOOP3
E41C  24                      INR     H
E41D  05              LOOP3   DCR     B
E41E  C2 12 E4                JNZ     LOOP2
E421  7B                      MOV     A, E
E422  D6 0D                   SUI     13
E424  5F                      MOV     E, A
E425  0D                      DCR     C
E426  C2 05 E4                JNZ     LOOP1
E429  C9                      RET
```

Figure 10. 8080A Microprocessor Program that Decodes a 32 Character ASCII String Prior to Loading into the DECODED DATA CONTROLLER

These controllers have been designed to eliminate the burden of data handling between keyboard, display, and microprocessor. The product data sheet describes the technical function of the controllers in detail.

Interfacing the controller to microprocessor systems depends on the needs of the particular application. Figures 13a and 13b depict latched interfaces from a master microprocessor to the HDSP-247X series of controllers. These interfaces are utilized to avoid having the master processor wait for the controller to accept data.

In sophisticated systems, it may be desirable to have the HDSP-247X controller handle all of the keyboard/display interface while the microprocessor reads edited messages from the controller DATA OUT port. This function can be achieved through the use of peripheral interface adapters (PIA) available from the microprocessor manufacturers. Figure 14 depicts a 6800 based system in which data may enter the display from either a keyboard or a microprocessor. This interface uses a 6821 PIA configured so that PB_7 controls whether the microprocessor or keyboard enters data into the controller. The 6800 program is shown in Figure 15. Subroutine "LOAD" uses CA_1 and CA_2 to provide a data entry handshake that allows the 6800 to load data into the controller as fast as the controller can accept it. After the prompting message has been loaded, the microprocessor turns the control of data entry over to the keyboard. A signal from the keyboard ("ER" in the example) sets a flag within the 6821. Depending on how the 6821 is configured, the microprocessor can either test the flag or allow the flag to automatically interrupt the microprocessor. Subroutine "READ" would then be used to read the DATA OUT

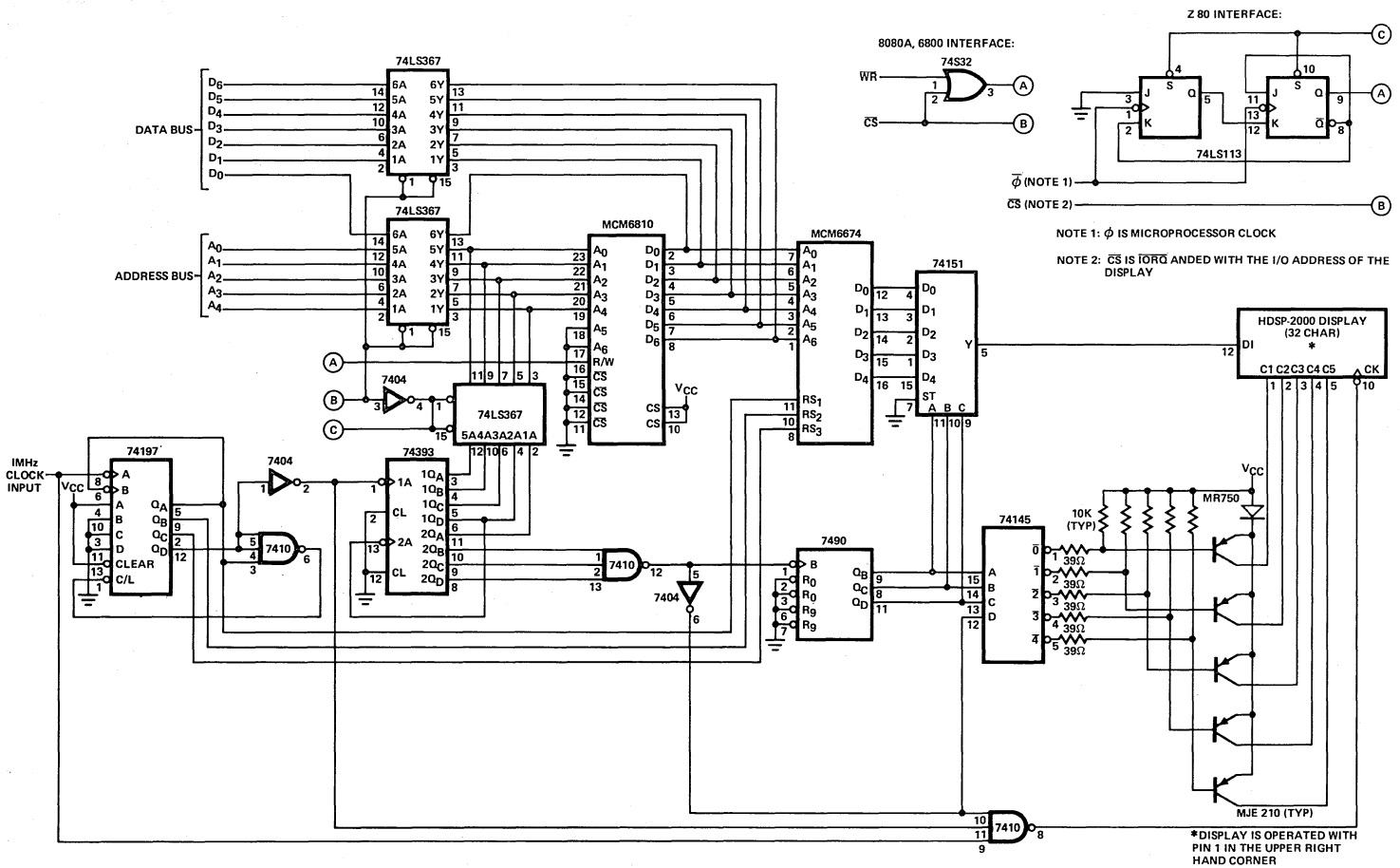


Figure 11a. 8080A Microprocessor Interface to the HDSP-2000 RAM CONTROLLER

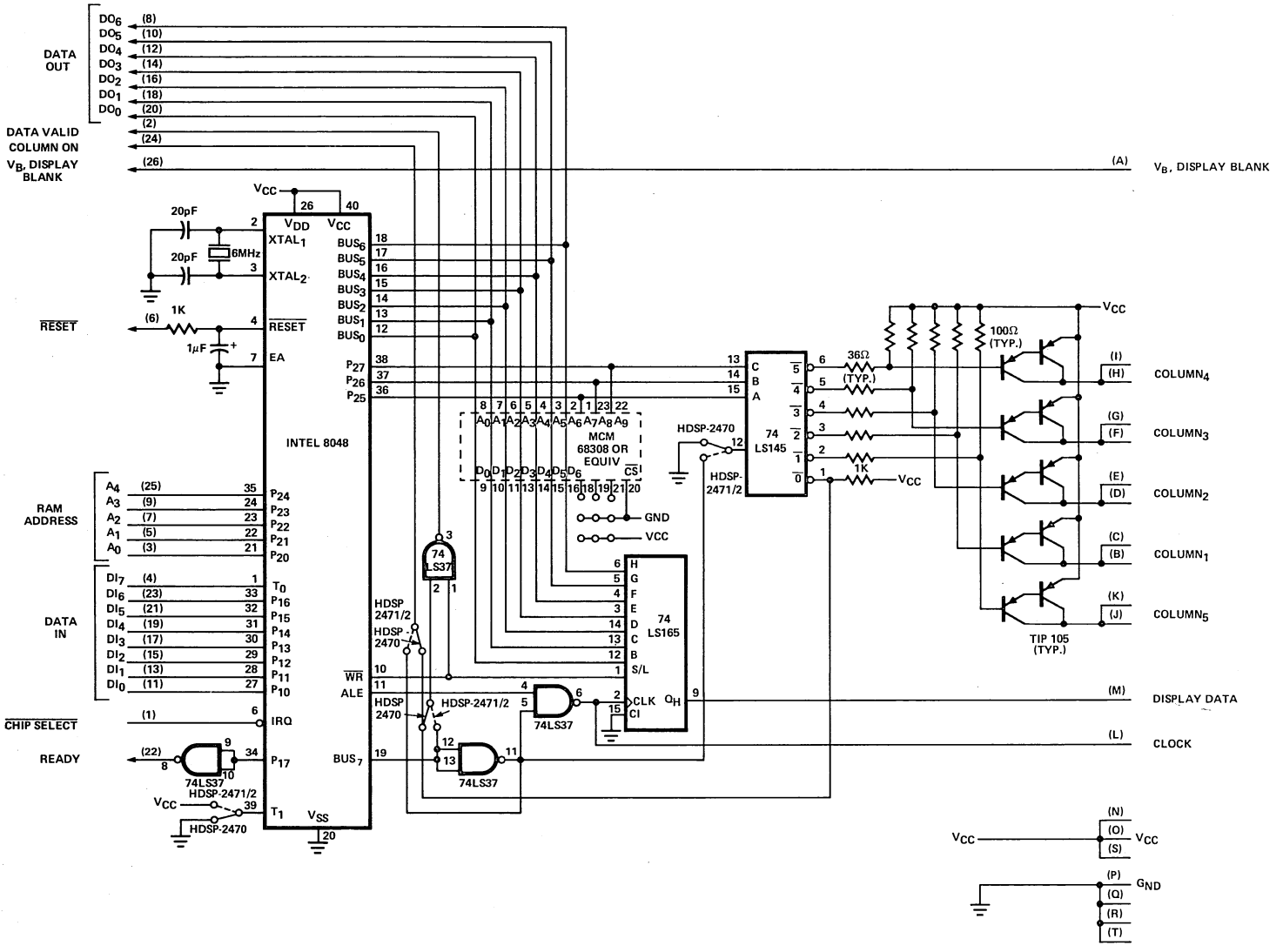
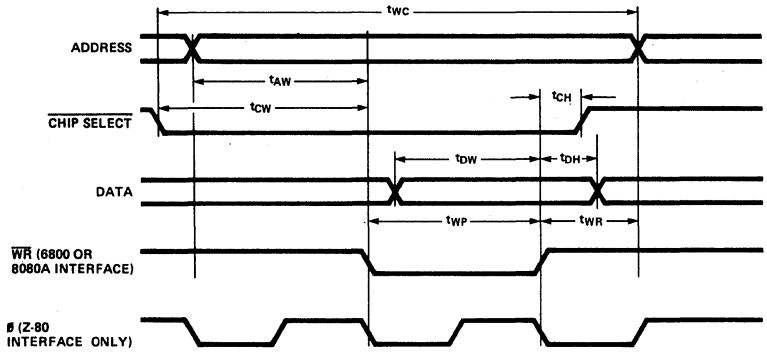


Figure 12. HDSP-2470/-2471/-2472 DISPLAY PROCESSOR CONTROLLER

APPLICATION NOTES



PARAMETER	SYMBOL	MIN.
WRITE CYCLE	t_{WC}	390ns
WRITE DELAY	t_{AW}	65ns
CHIP ENABLE TO WRITE	t_{CW}	65ns
DATA SETUP	t_{DW}	220ns
DATA HOLD	t_{DH}	20ns
WRITE PULSE	t_{WP}	310ns
WRITE RECOVERY	t_{WR}	10ns
CHIP ENABLE HOLD	t_{CH}	20ns

Figure 11b. Memory Write Timing for the HDSP-2000 RAM CONTROLLER

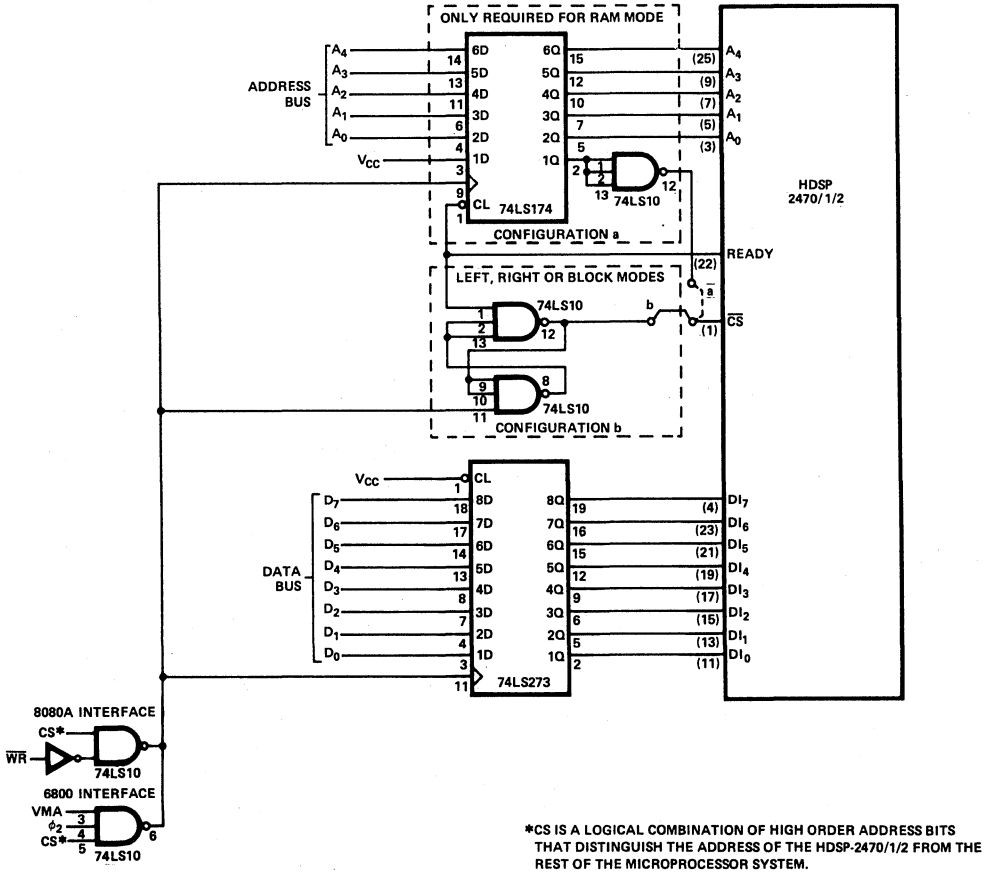


Figure 13. Latched Interface to the HDSP-2470/-2471/-2472 DISPLAY PROCESSOR CONTROLLER

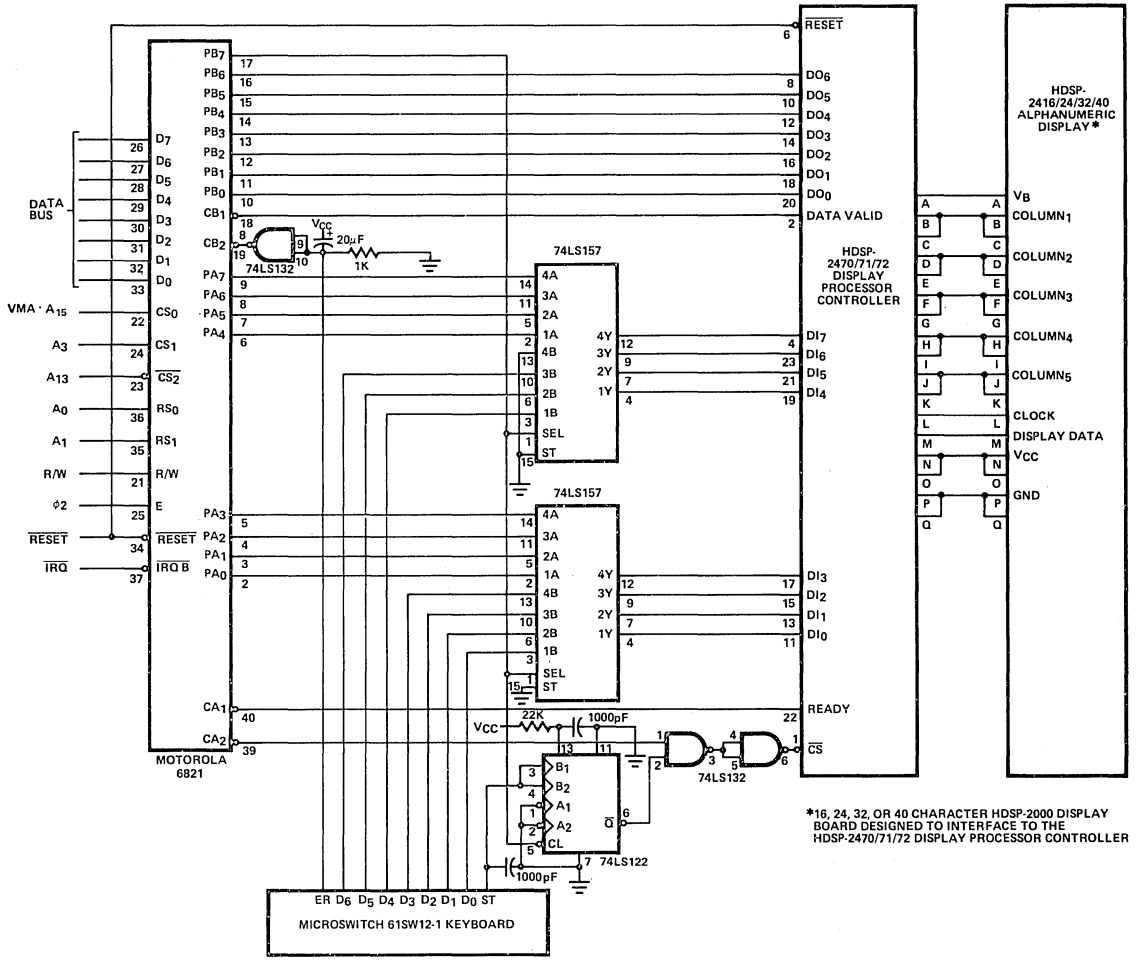


Figure 14. 6800 Microprocessor Interface Utilizing a 6820 PIA for an HDSP-2470/-2471/-2472 Alphanumeric Terminal

outputs from the controller into the microprocessor system. The microprocessor uses the CB_1 input of the 6821 PIA to determine when to read each of the 34 data output words into the system.

A similar PIA interface for the 8080A microprocessor is depicted in Figures 16 and 17.

The HDSP-247X series of controllers are programmed to default to "Left Entry" mode for a 32 character string of displays. If some other entry mode or string length is desired, it is necessary to either load the appropriate control word from the microprocessor or to provide a control word during POWER ON RESET. The controller will read the DATA IN lines during RESET and interpret the contents as the control word. The circuit depicted in Figure 18 can be utilized to load any desired preprogrammed word into the HDSP-247X controller, during power on.

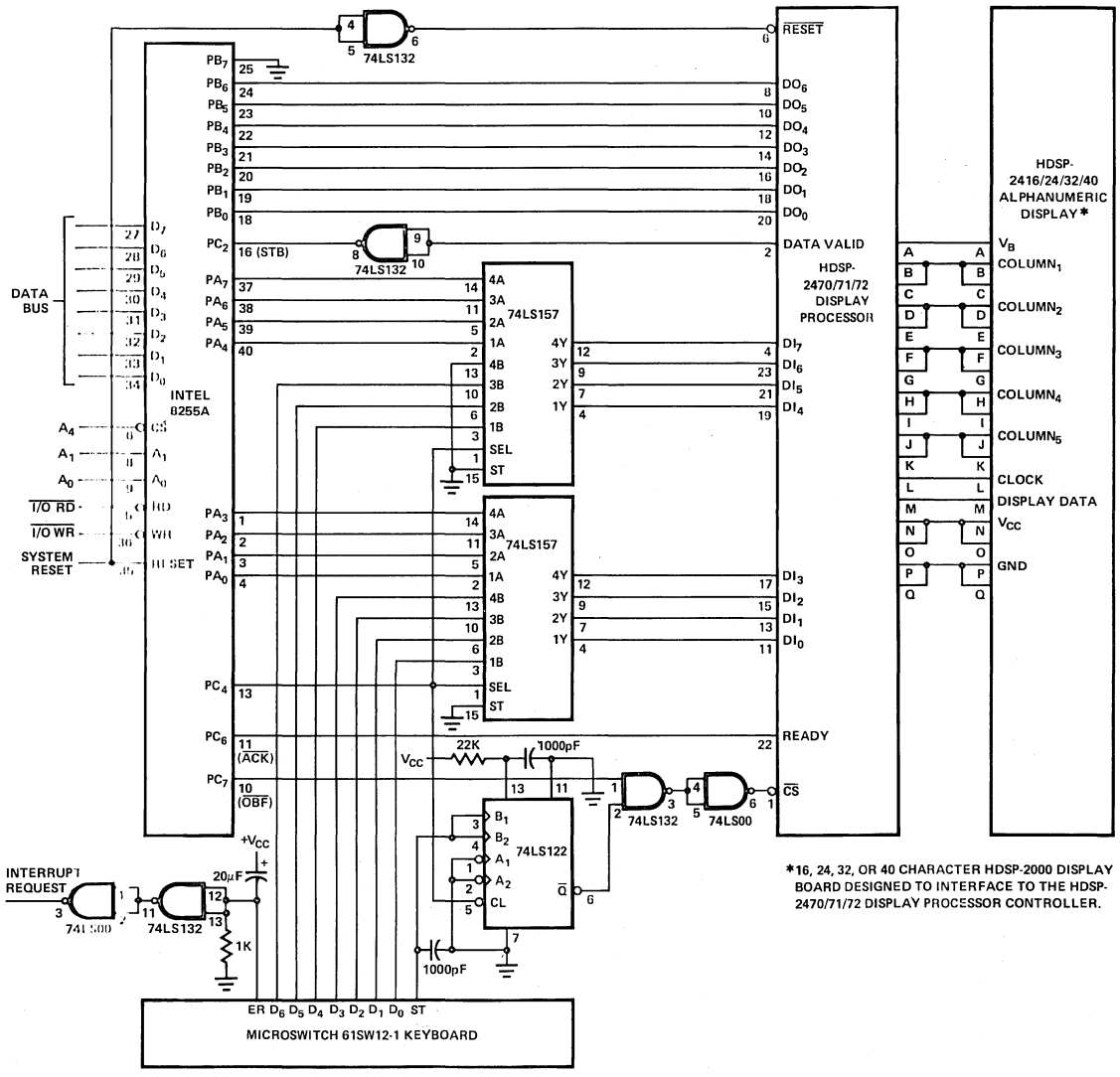
Under certain operating conditions, it may be desirable to vary the brightness of displays controlled by the HDSP-247X controllers. The circuit depicted in Figure 19 may be utilized to provide manual brightness control of the display through pulse width modulation. Automatic control may be achieved by substituting an appropriate value photoconductor for potentiometer R_1.

```
* PORT CONFIGURATION:
* 1.  PORT A:
*           PA0-PA7 OUTPUTS TO DATA IN OF HDSP-247X
*           CA1  (INPUT) MODE 00 SET FLAG NEG EDGE OF READY
*           CA2  (OUTPUT) MODE 100 CLEARED MPU READ PRA, SET
*           NEG  EDGE OF READY
* 1.  PORT B:
*           PB0-PB6 INPUTS DATA TO 6800 FROM DATA OUT OF HDSP-247X
*           CB1  (INPUT) MODE 00 SETS FLAG NEG EDGE OF DATA VALID
*           CB2  (INPUT) MODE 000 SETS FLAG NEG EDGE OF ER KEY
*           CB2  (INPUT) MODE 001 SETS FLAG NEG EDGE OF ER KEY
            CAUSING IRQ
*           PB7  (OUTPUT) LOW ENABLES PA0-PA7 TO MUX
*                         HIGH ENABLES  KEYBOARD TO MUX
*

LOC  OBJECT    CODE     SOURCE STATEMENT

     8008      PRA      EQU    $8008
     8008      DRA      EQU    $8008
     8009      CRA      EQU    $8009
     800A      PRB      EQU    $800A
     800A      DRB      EQU    $800A
     800B      CRB      EQU    $800B

                        ORG    $0000
0000           MESSAGE  RMB    2

                        ORG    $0100
0100           STATUS   RMB    1
0101           CURSOR   RMB    1
0102           DATA     RMB    32

                        ORG    $0400
0400 CE 0100   READ     LDX    I, STATUS
0403 B6 800A   LOOP1    LDA A  E, PRB          CLEAR CB1 AND CB2
0406 5F                 CLR B
0407 5C        LOOP2    INC B
0408 B6 800B            LDA A  E, CRB
040B 2A FA              BPL    LOOP2           WAIT FOR DATA VALID
040D C1 0A              CMP B  I, 10
040F 23 F2              BLS    LOOP1
0411 C6 21              LDA B  I, 33
0413 B6 800A   LOOP3    LDA A  E, PRB          READ AND CLEAR CB1
0416 84 7F              AND A  I, $7F
0418 A7 00              STA A  X, 0            STORE IN RAM
041A B6 800B   LOOP4    LDA A  E, CRB
041D 2A FB              BPL    LOOP4           WAIT FOR DATA VALID
041F 08                 INX
0420 5A                 DEC B
0421 26 F0              BNE    LOOP3           READ DATA
0423 B6 800A            LDA A  E, PRB
0426 84 7F              AND A  I, $7F
0428 A7 00              STA A  X, 0
042A 39                 RTS

042B DE 00     LOAD     LDX    D, MESSGE
042D A6 00     LOOP10   LDA A  X, 0
042F 08                 INX
0430 81 FF              CMP A  I, $FF          LAST WORD IN STRING
0432 27 0D              BEQ    ENDL            JUMP WHEN DONE
0434 B7 8008            STA A  E, PRA
0437 7D 8008            TST    E, PRA          CLEAR CA1 AND CA2
043A B6 8009   LOOP11   LDA A  E, CRA
043D 2A FB              BPL    LOOP11          WAIT
043F 20 EC              BRA    LOOP10
0441 DF 00     ENDL     STX    D, MESSGE
0443 39                 RTS

                        ORG    $0500
0500 7F 8009   START    CLR    E, CRA
0503 7F 800B            CLR    E, CRB
0506 86 FF              LDA A  I, $FF
0508 B7 8008            STA A  E, DRA
050B 86 24              LDA A  I, $24
050D B7 8009            STA A  E, CRA
0510 86 80              LDA A  I, $80
0512 B7 800A            STA A  E, DRB
0515 86 04              LDA A  I, $04
0517 B7 800B            STA A  E, CRB

                * PROCEDURE TO LOAD HDSP-247X SYSTEM
051A 0E                 CLI
051B 7F 800A            CLR    E, PRB          DISABLE KEYBD FROM MUX
051E BD 042B            JSR    E, LOAD

                * PROCEDURE TO READ DATA OUT OF HDSP-247X SYSTEM
0521 7D 800A            TST    E, PRB          CLEAR CB1, CB2
0524 86 80              LDA A  I, $80
0526 B7 800A            STA A  E, PRB          ENABLE KEYBD TO MUX
0529 86 0C              LDA A  I, $0C
042B B7 800B            STA A  E, CRB          ENABLE IRQ,
052E 0F                 SEI                    IRQ CAUSE JSR TO READ
```

Figure 15. 6800 Microprocessor Program that Interfaces to the Circuit shown in Figure 14.

```
* PORT CONFIGURATION:
* 1.  PORT A (MODE 1 OUTPUT):
*           PA0-PA7 OUTPUTS TO DATA IN OF HDSP-247X
*           PC7  (OBF) OUTPUT; TO CHIP SELECT
*           PC6 (ACK) INPUT; TO READY
*           FLAG PC7 (OBF) CLEARED BY OUTPUT; SET BY READY
*
* 2.  PORT B (MODE 1 INPUT):
*           PB0-PB6 INPUTS DATA FROM DATA OUT OF HDSP-247X
*           PC2 (STB) INPUT; LOADS DATA ON NEG EDGE OF DATA VALID
*           FLAG PC0 (INTR) CLEARED BY INPUT; SET BY DATA VALID
*
* 3.  PORT C:
*           PC4 OUTPUT; LOW ENABLES PA0-PA7 TO HDSP-247X
*                       HIGH ENABLES KEYBOARD TO HDSP-247X

LOC  OBJECT    CODE     SOURCE STATEMENTS

000C           PA       EQU    0CH
000D           PB       EQU    0DH
000E           PC       EQU    0EH
000F           CNTRL    EQU    0FH

                        ORG    0E000H
E000 02 E0     ASCII    DW     TEXT
E002 00        TEXT     DS     32

                        ORG    0E100H
E100 00        STAT     DB     0
E101 00        ADDR     DB     0
E102 00        DATA     DS     32

                        ORG    0E400H
E400 F3        READ     DI
E401 F5                 PUSH   PSW
E402 E5                 PUSH   H
E403 C5                 PUSH   B
E404 0E 20              MVI    C, 32
E406 21 00 E1           LXI    H, STAT         FIRST WORD
E409 DB 0D              IN     PB              CLEAR INTR
E40B 06 00     LOOP1    MVI    B, 0
E40D DB 0E     LOOP2    IN     PC
E40F 04                 INR    B
E410 1F                 RAR
E411 D2 0D E4           JNC    LOOP2           WAIT UNTIL INTR IS SET
E414 3E 0A              MVI    A, 10
E416 B8                 CMP    B
E417 DB 0D              IN     PB
E419 D2 0B E4           JNC    LOOP1           WAIT UNTIL STATUS WORD
E41C 77        LOOP3    MOV    M, A            STORE IN RAM
E41D 23                 INX    H
E41E DB 0E     LOOP4    IN     PC
E420 1F                 RAR
E421 D2 1E E4           JNC    LOOP4           WAIT UNTIL INTR IS SET
E424 DB 0D              IN     PB
E426 0D                 DCR    C
E427 C2 1C E4           JNZ    LOOP3
E42A 77                 MOV    M, A            STORE LAST WORD
E42B C1                 POP    B
E42C E1                 POP    H
E42D F1                 POP    PSW
E42E FB                 EI
E42F C9                 RET

E430 2A 00 E0  LOAD     LHLD   ASCII           FIRST WORD OF MESSAGE
E433 7E        LOOP5    MOV    A, M
F434 FE FF              CPI    0FFH            CHECK TO SEE IF DONE
E436 CA 45 E4           JZ     ENDL
E439 D3 0C              OUT    PA              OUTPUT TO DISPLAY
E43B 23                 INX    H
E43C DB 0E     LOOP6    IN     PC
E43E 17                 RAL
E43F D2 3C E4           JNC    LOOP6           WAIT
E442 C3 33 E4           JMP    LOOP5           NEXT WORD
E445 23        ENDL     INX    H
E446 22 00 E0           SHLD   ASCII
E449 C9                 RET

E44A 3E A7     START    MVI    A, 0A7H         PA OUTPUT, PB INPUT
E44C D3 0F              OUT    CNTRL
E44E 3E 0C              MVI    A, 0CH          CLEAR INTE A
E450 D3 0F              OUT    CNTRL
E452 3E 05              MVI    A, 05H
E454 D3 0F              OUT    CNTRL           SET INTE B

                * PROCEDURE TO LOAD HDSP-247X SYSTEM
E456 3E 08              MVI    A, 08H
E458 D3 0F              OUT    CNTRL           ENABLE A SIDE OF MUX
E45A CD 30 E4           CALL   LOAD

                * PROCEDURE TO READ DATA OUT OF HDSP-247X SYSTEM
E45D 3E 09              MVI    A, 09H
E45F D3 0F              OUT    CNTRL           ENABLE B SIDE OF MUX
E461 FB                 EI                     INT MUST CALL READ
```

Figure 16. 8080A Microprocessor Program that Interfaces to the Circuit shown in Figure 17.



*16, 24, 32, OR 40 CHARACTER HDSP-2000 DISPLAY BOARD DESIGNED TO INTERFACE TO THE HDSP-2470/71/72 DISPLAY PROCESSOR CONTROLLER.

Figure 17. 8080A Microprocessor Interface Utilizing an 8255 PIA for an HDSP-2470/-2471/-2472 Alphanumeric Terminal

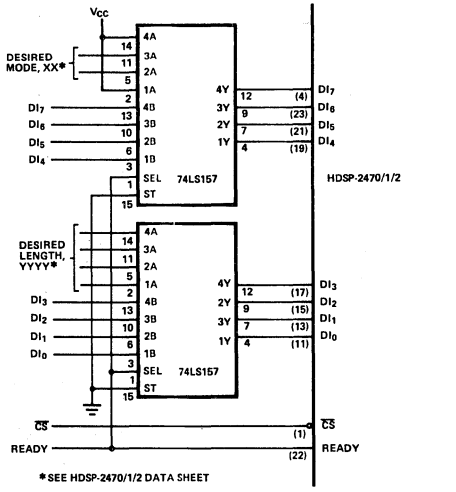


Figure 18. External Circuitry to Load a Control Word into the HDSP-2470/-2471/-2472 Alphanumeric System upon Reset

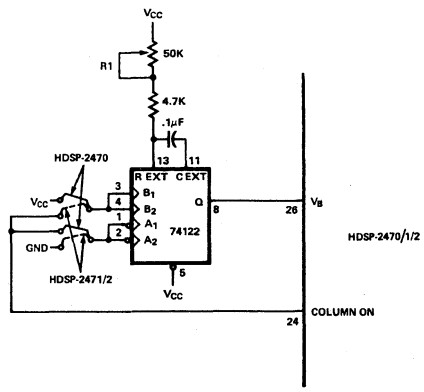


Figure 19. External Circuitry to Vary Luminous Intensity of the HDSP-2470/-2471/-2472 Alphanumeric Display System

DECODER ADDRESS FOR FIG. 7a, 7b, 10	DECODER ADDRESS FOR FIG. 6	HDSP-2471 ROM ADDRESS	HEXIDECIMAL DATA															
E500	0600	080	08	30	45	7D	7D	38	7E	30	60	1E	3E	62	40	08	38	41	$COLUMN_1$
		090	10	18	5E	78	38	78	38	3C	38	3C	38	08	20	12	48	01	
		0A0	00	00	00	14	24	23	36	00	00	00	08	08	00	08	00	20	
		0B0	3E	00	62	22	18	27	3C	01	36	06	00	00	00	14	41	06	
		0C0	3E	7E	7F	3E	7F	7F	7F	3E	7F	00	20	7F	7F	7F	7F	3E	
		0D0	7F	3E	7F	26	01	3F	07	7F	63	03	61	00	02	41	04	40	
		0E0	00	38	7F	38	38	38	08	08	7F	00	20	00	00	78	7C	38	
		0F0	7C	18	00	48	04	3C	1C	3C	44	04	44	00	00	00	08	2A	
E580	0680	100	1C	48	29	09	09	44	01	4A	50	04	49	14	3C	7C	44	63	$COLUMN_2$
		110	08	24	61	14	44	15	45	43	45	41	42	08	7E	19	7E	12	
		120	00	5F	03	7F	2A	13	49	08	00	41	2A	08	58	08	30	10	
		130	51	42	51	41	14	45	4A	71	49	49	36	5B	08	14	22	01	
		140	41	09	49	41	41	49	09	41	08	41	40	08	40	02	04	41	
		150	09	41	09	49	01	40	18	20	14	04	51	00	04	41	02	40	
		160	07	44	48	44	44	54	7E	14	08	44	40	7F	41	04	08	44	
		170	14	24	7C	54	3E	40	20	40	28	48	64	08	00	41	04	55	
E600	0700	180	3F	45	11	11	05	44	29	4D	48	04	49	08	20	04	44	55	$COLUMN_3$
		190	78	7E	01	15	45	14	44	42	44	40	40	2A	02	15	49	7C	
		1A0	00	00	00	14	7F	08	56	07	3E	3E	1C	3E	38	00	30	08	
		1B0	49	7F	49	49	12	45	49	09	49	49	36	3B	14	14	14	51	
		1C0	5D	09	49	41	41	49	09	41	08	7F	40	14	40	0C	08	41	
		1D0	09	51	19	49	7F	40	60	18	08	78	49	7F	08	7F	7F	40	
		1E0	0B	44	44	44	44	54	09	54	04	7D	44	10	7F	18	04	44	
		1F0	24	14	08	54	44	40	40	30	10	30	54	36	77	36	08	2A	
E680	0780	200	7F	40	29	21	05	38	2E	49	50	38	49	10	20	7C	3C	49	$COLUMN_4$
		210	08	24	61	14	3C	15	3D	43	45	41	42	1C	02	12	41	12	
		220	00	00	03	7F	2A	64	20	00	41	00	2A	08	00	08	00	04	
		230	45	40	49	49	7F	45	49	05	49	29	00	00	22	14	08	09	
		240	55	09	49	41	41	49	09	51	08	41	40	22	40	02	10	41	
		250	09	21	29	49	01	40	18	20	14	04	45	41	10	00	02	40	
		260	00	3C	44	44	48	54	02	54	04	40	3D	28	40	04	04	44	
		270	24	7C	04	54	20	20	20	40	28	08	4C	41	00	08	10	55	
E700	0800	280	00	30	45	7D	79	44	10	30	60	40	3E	60	1C	02	04	41	$COLUMN_5$
		290	04	18	5E	78	40	78	40	3C	38	3C	38	08	02	00	42	01	
		2A0	00	00	00	14	12	62	50	00	00	00	08	08	00	08	00	02	
		2B0	3E	00	46	36	10	39	30	03	36	1E	00	00	41	14	00	06	
		2C0	1E	7E	36	22	3E	41	01	72	7F	00	3F	41	40	7F	7F	3E	
		2D0	06	5E	46	32	01	3F	07	7F	63	03	43	41	20	00	04	40	
		2E0	00	40	38	20	7F	08	00	3C	78	00	00	44	00	78	78	38	
		2F0	18	40	04	20	00	7C	1C	3C	44	04	44	00	00	00	08	2A	

Figure 20. 128 Character ASCII Decoder Table Used by the 6800 Refresh Program in Figure 6, 8080A Refresh Programs in Figures 7a, 7b, and 10, and the HDSP-2471 DISPLAY PROCESSOR CONTROLLER. Decoded 5x7 Display Font is shown in the HDSP-247X Data Sheet

HEWLETT PACKARD
COMPONENTS

NEW PRODUCT APPLICATION

APPLICATION NOTE 1002

Consideration of CTR Variations in Optically Coupled Isolator Circuit Designs

INTRODUCTION — Optocouplers Aging Problem

A persistent, and sometimes crucial, concern of designers using optocouplers is that of the current transfer ratio, CTR, changing with time. The CTR is defined as the ratio of the output current, I_O, of the optocoupler divided by the input current, I_F, to the light emitting diode expressed as a percentage value at a specified input current. The resulting optocoupler's gain change, ΔCTR^+, with time is referred to as CTR degradation. This change, or degradation, must be accounted for if long, functional lifetime of a system is to be guaranteed.

A number of different sources for this degradation will be explained in the next section, but numerous studies have demonstrated that the predominant factor for degradation is reduction of the total photon flux being emitted from the LED, which, in turn, reduces the device's CTR. This degradation occurs to some extent in all optocouplers.

$$^+\Delta CTR = CTR_{final} - CTR_{initial} \quad (1)$$

Causes

The main cause for CTR degradation is the reduction in efficiency of the light emitting diode within the optocoupler. Its quantum efficiency, η, defined as the total photons per electron of input current, decreases with time at a constant current. The LED current is comprised primarily of two components, a diffusion current component, and a space-charge recombination current:

$$I_F(V_F) = \underbrace{A\, e^{qV_F/kT}}_{\text{Diffusion}} + \underbrace{B\, e^{qV_F/2kT}}_{\text{Space-Charge Recombination}} \quad (2)$$

where A and B are independent of V_F, q is electron charge, k is Boltzmann's constant, T is temperature in degrees Kelvin, and V_F is the forward voltage across the light emitting diode.

The diffusion current component is the important radiative current and the non-radiative current is the space-charge recombination current. Over time, at fixed V_F, the total current increases through an increase in the value of B. From another point of view, with fixed total current, if the space-charge recombination current increases, due to an increase in the value of B, then the diffusion current, the radiative component, will decrease. The specific reasons for this increase in the space-charge recombination current component with time are not fully understood.

The reduction in light output through an increase in the proportion of recombination current at a specific I_F is due to both the junction current density, J, and junction temperature, T_J. In any particular optocoupler, the emitter current density will be a function of not only the required current necessary to produce the desired output, but also of the junction geometry and of the resistivity of both the P and N regions of the diode. For this reason, it is important not to operate a coupler at a current in excess of the manufacturer's maximum ratings. The junction temperature is a function of the coupler packaging, power dissipation and ambient temperature. As with current density, high T_J will promote a more rapid increase in the proportion of recombination current.

The junction and IC detector temperature of Hewlett-Packard optocouplers can be calculated from the following expressions:

$$T_J = T_A + \theta_{JA}(V_F I_F) + \theta_{D\text{-}E}(V_o I_o + V_{cc} I_{cc})$$

$$T_D = T_A + \theta_{E\text{-}D}(V_F I_F) + \theta_{DA}(V_o I_o + V_{cc} I_{cc}) \quad (3)$$

APPLICATION NOTES

where the T_J is the junction temperature of the LED emitter, T_D is the junction temperature of the detector IC, T_A is ambient temperature, and the thermal resistances are the emitter junction to ambient, $\theta_{JA} = 370°C/W = \theta_{DA}$ detector to ambient, and the detector to emitter thermal resistance is $\theta_{D\text{-}E} = 170°C/W = \theta_{E\text{-}D}$. V_F, I_F are the forward LED voltage and current; V_o, I_o are the output stage voltage, and current and V_{cc}, I_{cc} are the power supply voltage and current to the device. In general, it is desirable to maintain $T_J \leqslant 125°C$.

A useful model can be constructed to describe the basic optocoupler's parameters which are capable of influencing the current transfer ratio. The 6N135 optocoupler, Figure 1 is the simplest device and one which is easily accessible for needed parameter measurements. However, any optocoupler can be modeled in this fashion within its linear region. Figure 1 shows the system block diagram which yields the relationship of input current, I_F, to output current, I_o. The resulting expression for CTR is:

$$CTR = \frac{I_o}{I_F}(100\%) = K\,R\,\eta(I_F,t)\,\beta(I_P,t) \qquad (4)$$

where K represents the total transmission factor of the optical path, generally considered a constant as is R, the responsivity of the photodetector, defined in terms of electrons of photocurrent per photon. η is the quantum efficiency of the emitter defined as the photons emitted per electron of input current and depends upon the level of input current, I_F, and upon time. Finally, β is the gain of the output amplifier and is dependent upon I_P, the photocurrent, and time. Temperature variations would, of course, cause changes in η, β as well.

From Equation (4), a normalized change in CTR, at constant I_F, can be expressed as:

(5)

$$\frac{\Delta CTR}{CTR} = \left(\frac{\Delta\eta}{\eta}\right)_{I_F} + \left(\frac{\Delta\eta}{\eta}\right)_{I_F}\left(\frac{\partial \ln\beta}{\partial \ln I_P}\right)_t + \left(\frac{\Delta\beta}{\beta}\right)_{I_P}$$

The first term, $\Delta\eta/\eta$, represents the major contribution to ΔCTR due to the relative emitter efficiency change; generally, over time, $\Delta\eta$ is negative. This change is strongly related to the input current level, I_F, as discussed earlier and more elaboration will be given later. The second term, $(\Delta\eta/\eta)_{I_F}$ $(\partial\ln\beta/\partial\ln I_P)_t$, represents a second order effect of a shift, positive or negative, in the operating point of the output amplifier as the emitter efficiency changes. The third term, $(\Delta\beta/\beta)_{I_P}$, is a generally negligible effect which represents a positive or negative change in the output transistor gain over time. The parameters K and R are considered constants in this model.

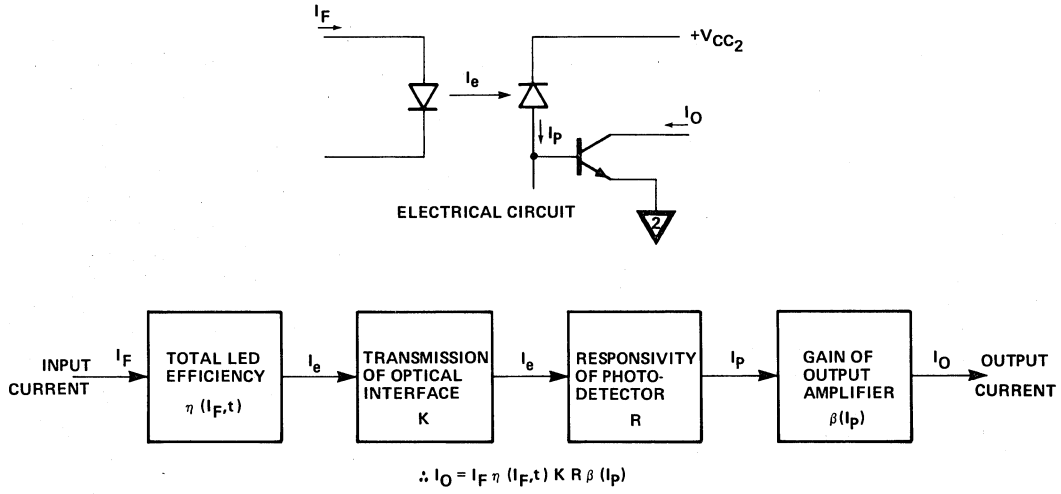


Figure 1. System Model for an Optocoupler

Degradation Model

In this section, an extensive test program conducted at Hewlett-Packard to characterize the CTR degradation of optocouplers is discussed. The development which will follow is mainly of interest to those concerned with reliability and quality assurance. From the basic data, the CTR degradation equations will be developed in order to predict the percentage change in CTR with time. Complete data and analysis of CTR degradation will be found in an internal Hewlett-Packard report.

This study is based on a total of 640 optocouplers of the 6N135 type (Figure 1) with 700 nm $GaAs_{.7}P_{.3}$ LEDs from twenty different epitaxial growth lots representing a range of n-type doping and radiance. The 6N135 allows access to measurement of the emitter degradation via the relative percentage change in photodiode current, $\Delta I_P/I_P$, as well as output amplifier β change. Stress currents of I_{FS} = .6, 7.5, 25 and 40 mA were applied to different groups of optocouplers, and at each measurement time of t = 0, 24, 168, 1000, 2000, 4000 and 10,000 hours, measurement currents of I_{FM} = .5, 1.6, 7.5, 25 and 40 mA were used to determine the CTR.

The important results to be noted are the following. First, a factor of major significance in the study of CTR degradation is the ΔCTR varies as a function of the ratio of $I_{FS}/I_{FM} \equiv R$. Large values of R will result in greater CTR degradation than at lower R values with the same magnitude of I_{FS}. However, knowledge of the ratio of I_{FS}/I_{FM} alone does not give a complete picture of degradation because ΔCTR is also dependent upon the absolute magnitude of the stress current, $|I_{FS}|$. The following data will allow the derivation of the necessary equations with which to predict ΔCTR as a function of I_{FS}, I_{FM} and time.

Figure 2 displays the mean and mean plus 2σ values of emitter degradation versus R for 1K, 4K, and 10K hours at 25°C. Accelerated degradation can be seen at larger R values.

The data of Figure 2 can be replotted to illustrate the percentage degradation versus time as a function of R. Figure 3 illustrates the mean and mean plus 2σ distribution with R = 1 and 50.

From this curve, a useful expression which relates the average degradation in emitter efficiency to time is obtained for the mean or mean plus 2σ distributions. [The symbol "D" will refer to CTR degradation due solely to emitter degradation, $\Delta\eta/\eta$, whereas ΔCTR/CTR will refer to total CTR degradation as expressed in Equation (5)].

$$D_{\bar{x}} \text{ or } D_{\bar{x}+2\sigma} \equiv \frac{-\Delta I_P}{I_P} = A_o R^{\alpha} t^{n(R)} \quad \text{for } I_{FS} = \bar{I}_{FS} \text{ in \%} \tag{6}$$

where t is in 10^3 hours and A_o and α differ for mean or mean plus 2σ. Equation (6) represents an average degradation corresponding to a specific R, t, and an average stress current I_{FS}. A knowledge of I_{FS} and the actual device operating stress I_{FS} can be utilized to correct D to reflect the absolute magnitude of I_{FS}. This will be shown in the development of Equations (11) and (13). The data shows that I_{FS} increases with R and can be represented as follows:

$$\bar{I}_{FS}(R) = 14.13 + 9.06 \log_{10} R \quad , T_A = 25°C \tag{7}$$

$$\bar{I}_{FS}(R) = 10.5 + 5.76 \log_{10} R \quad , T_A = 85°C \tag{8}$$

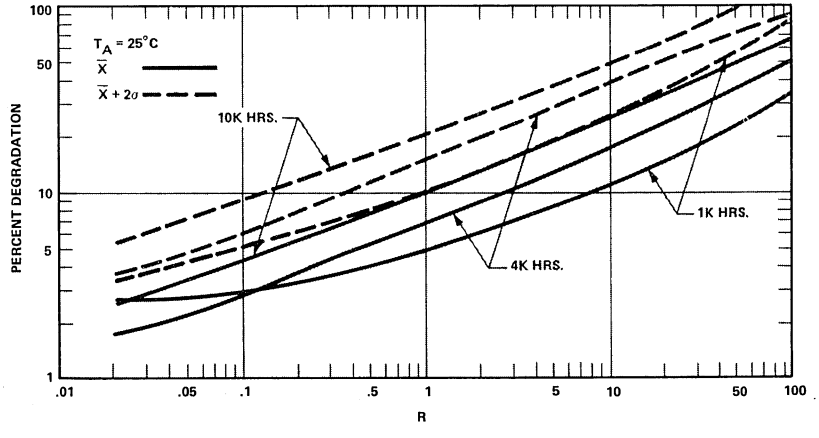


Figure 2. Emitter Degradation vs. R (Ratio of Stress Current to Measurement Current) for 1k, 4k, and 10k Hours, Mean, Mean +2σ Distribution, T_A = 25°C.

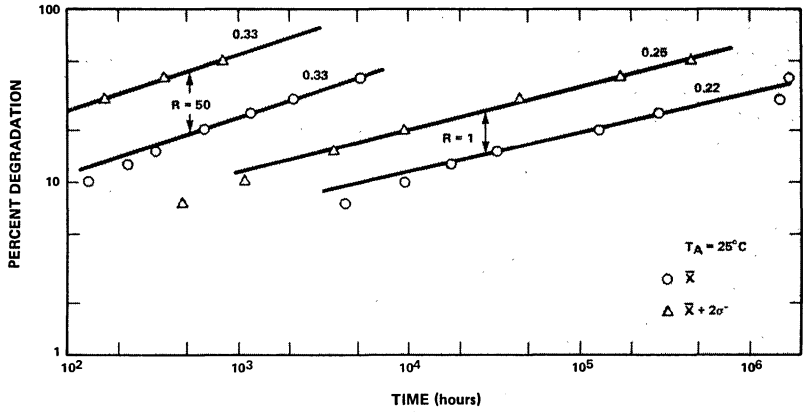


Figure 3. Degradation vs. Time at R = 1 and R = 50 for Mean, Mean + 2σ Distributions, T_A = 25°C.

These equations are obtained from averaged degradation data versus I_{FS} at different measurement times.

The expression for n(R) was found to obey the relationship

$$n(R) = .0475 \log_{10} R + .25 \qquad (9)$$

A_o and α were determined from degradation data versus R and are found in Figure 7, "Matrix of Coefficients."

Equation (6) gives a direct relationship between the average degradation, $\bar{D}$, and time. As mentioned earlier, the magnitude of the stress current also determines the amount of degradation. In order to allow for the effect of $|I_{FS}|$, empirical observations were made on D at different I_{FS} and at different times for several values of R. The dependence of degradation on stress current is linear up to I_{FS} = 40 mA, for all values of R. From these observations, the average rate of change, or slope, S(R,t), of degradation D with I_{FS} over time was found to behave in the following fashion for any R:

$$S \equiv \frac{\partial D}{\partial I_{FS}} = \alpha(R) \log_{10} t + \beta(R) \quad \%/mA \qquad (10)$$

where t is in 10^3 hours, the coefficients $\alpha(R)$ and $\beta(R)$ can be found on Figure 7.

Along with Equation (10), the mean distribution degradation, $D_{\bar{X}}$, can be estimated for any specific stress current, I_{FS}, ratio R, and time t via the subsequent expression:

$$D_{\bar{X}} = \bar{D}_{\bar{X}} + S\,[I_{FS} - \bar{I}_{FS}] \quad \% \qquad (11)$$

or substituting Equation (6),

$$D_{\bar{X}} = A_o R^{\alpha} t^{n(R)} + S\,[I_{FS} - \bar{I}_{FS}] \quad \% \qquad (12)$$

where, again, $D_{\bar{X}}$ is the average degradation at time t, in units of 10^3 hours, corresponding to a stress current, $\bar{I}_{FS}$, given by Equations (7) and (8); I_{FS} is the actual stress current and $R = I_{FS}/I_{FM}$; S is the expression (10) for the change of slope of D versus I_{FS} with time; n(R) is a power of t, given by Equation (9), and A_o,α are found in Figure 7.

Equation (12) gives the mean distribution degradation by using a degradation value, $\bar{D}$ (first term), corresponding to the ratio of I_{FS}/I_{FM}, or a stress current, $\bar{I}_{FS}$, and then applying a correction quantity (second term) to $\bar{D}$ due to the magnitude of the actual stress current, I_{FS}, yielding the actual degradation D.

The expression for the mean + 2σ distribution degradation, $D_{\bar{X}+2\sigma}$, (worst case) is almost of the same form as Equation (12). The dissimilarity arises from the fact that the standard deviation, σ, is dependent upon the stress current, I_{FS}, the ratio R, and upon time. This complex dependency was analytically deduced from the data to be the following expression:

$$D_{\bar{X}+2\sigma} = \bar{D}_{\bar{X}+2\sigma} + [S + 2P]\,[I_{FS} - \bar{I}_{FS}] \quad \% \qquad (13)$$

or substituting Equation (6)

$$D_{\bar{X}+2\sigma} = A_o R^{\alpha} t^{n(R)} + [S + 2P]\,[I_{FS} - \bar{I}_{FS}] \qquad (14)$$

where $D_{\bar{X}+2\sigma}$ is the degradation for $\bar{X}$ + 2σ distribution corresponding to the stress current $\bar{I}_{FS}$, Equations (7)

and (8). A_o and α are found in Figure 7 under the $\bar{X}+2\sigma$ category. S [Equation (10)] represents the slope to correct for actual I_{FS} versus $\bar{I}_{FS}$ current levels, and P [Equation (15)] is the new term which is a slope to correct for the σ variation with I_{FS}, R and t. The coefficients $\gamma(R)$, $\delta(R)$ in P are found in Figure 7.

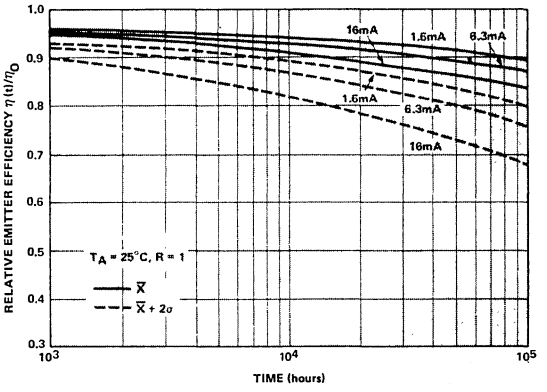
$$P = \gamma(R) \log_{10} t + \delta(R) \quad \%/mA \qquad (15)$$

where t is in 10^3 hours.

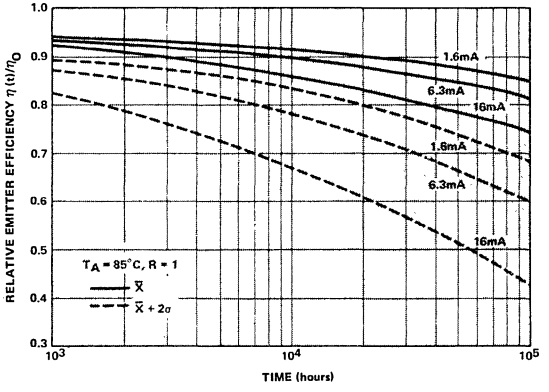
The degradation Equations (11) and (13) are considered accurate for the ranges of $I_{FS} \leq 40$ mA and $R \leq 20$; outside this range, the model does not predict degradation as well. Hence, check to see if I_{FS} and R satisfy the above conditions. If I_{FS} or R exceed these limits, predition of D will be, in general, greater than the actual degradation due to large values for S and P which do not reflect actual S and P. If $\bar{I}_{FS}$ is approximately equal to the actual I_{FS}, then the second term in the degradation equations need not be determined. Otherwise, the second term needs to be determined to obtain true emitter degradation, D. If $\bar{I}_{FS} < I_{FS}$, then the degradation, D, will be less than the degradation, $\bar{D}$, corresponding to $\bar{I}_{FS}$, and vice versa when $\bar{I}_{FS} > I_{FS}$. A quick and coarse estimate for degradation $\bar{D}$ can be obtained by using $\bar{D} = A_o R^{\alpha} t^{n(R)}$ for a specific R with approximate values for $\alpha \approx 0.4$ and $n \approx 0.3$. Figure 4 represents plots of Equations (11) and (13) for R = 1 and I_{FS} = 1.6, 6.3, and 16mA at both T_A = 25°C and T_A = 85°C. These plots are very useful in making a quick approximation of D for the specific conditions for which the plots have been made. These conditions represent the recommended operating conditions for the three HP optocoupler families.

This discussion of reliability data and its interpretation with model equations is qualified to specific optocouplers, 6N135 and 6N138, where continuous LED operation was maintained, and extrapolation of data for times beyond 10,000 hours is assumed to be valid. Different types of LEDs or preparation processes may produce different results than those presented in this section. These expressions only incorporate the first order effect, emitter degradation $\Delta\eta/\eta$, whereas comments about higher order effects upon total CTR degradation will be given in the following section. With these expressions for degradation, accelerated testing may be accomplished by employing large values of R. Such testing can provide a means by which to determine acceptable emitter lots for optocoupler fabrication, acceptable degradation performed for lot selection, or predict functional lifetime expectance for optocouplers under specific operational conditions.

An important point to note is that the total operational life of an optocoupler is greater than the worst case mean plus 2σ distribution implies. Specifically, the worst case degradation given in Figures 4a (25°C) and 4b (85°C) are for the continuous operation of the 6N135 optocoupler. The actual lifetime for an optocoupler is greater than Figures 4a and 4b would indicate since the majority of units will be centered around the mean distribution lifetime. Secondly, the optocoupler which is operated at some signal duty factor less than 100%, for example 50%, would increase the optocoupler's life by a factor of two. Third, the fact that an optocoupler is used within equipment which may have a typical 2000 hours per year (8 hours/day – 5 days/week – 50 weeks/year) instrument or system operating time, could expect to increase the optocoupler's life by another factor of 4.4 in terms of years of useful life.



a



b

Figure 4. Calculated Curves of Relative Emitter Efficiency vs. Time for P = 1: $I_{FS} = I_{FM}$ = 1.6, 6.3, and 16mA which are Recommended I_F for 6N138, 6N137, and 6N135 Optocouplers Respectively. Mean, Mean + 2σ Distributions. a) T_A = 25°C, b) T_A = 85°C.

The appropriate operating time considerations will vary depending upon the designer's knowledge of the system in which the optocoupler will be used. The operating lifetime of an optocoupler can be expressed, for a maximum allowable degradation at a particular I_{FS}, by using Figures 4a and 4b for $t_{continuous}$ lifetime and the following expression:

$$t_{\text{continuous lifetime}} = \left[t_{\text{system lifetime}}\right]\left[\text{Data Duty Factor}\right]\left[\text{System Use Data Factor}\right] \quad (16)$$

Another equally important point to observe is that of the worst case conditions under which the optocoupler is used. As will be illustrated in the design examples, the worst possible combination of variations in V_{cc1}, V_{cc2}, R_{in}, CTR, R_L, I_{IL}, and temperature still result in the optocoupler functioning over an extended length of time (10^5 hours) for a particular maximum allowable degradation. However, the likelihood of seven parameters all deviating in their worst directions at the same time is extremely remote. A thorough statistical error accumulation analysis would illustrate that this worst-worst case is not a representative situation from which to design.

Higher Order Effects

The first order effect of emitter degradation, $\Delta\eta/\eta$, has a pronounced influence upon the ΔCTR as explained in the previous sections; however, consideration of higher order effects is important as well.

Consider the second term in Equation (5) $(\Delta\eta/\eta)I_F$ $(\partial \text{In}\beta/\partial \text{In}Ip)t$, the emitter degradation part has been explained; however, $(\partial \text{In}\beta/\partial \text{In}IP)_t$ represents a shift in the operating point of the output amplifier of an optocoupler. The term $(\partial \ln\beta/\partial \ln I_P)$ can be rewritten as $(1/2.3\beta)(\partial\beta/\partial \log_{10} I_P)$ which is more convenient to use with the accompanying typical curves of β versus $\log_{10} I_P$ for the two optocouplers 6N135 and 6N138, given in Figure 5a.

If the operating photocurrent, I_P, is to the right of the maximum β point of either curve, then with reduced emitter efficiency over time, I_P will decrease, but the increasing β will tend to compensate for this degradation. However, if the operating I_P is to the left of the maximum β and then I_P decreases, the β change will accentuate the emitter's degradation, yielding a larger CTR loss. The magnitude of the contributions of $\partial \ln\beta/\partial \ln I_P$ to overall CTR degradation can be illustrated by the following examples.

Consider a 6N138 optocoupler of Figure 5c operating at its recommended I_F = 1.6 mA which corresponds to an $I_P \approx 1.6\mu$A. (An I_F to I_P relationship for Hewlett-Packard optocouplers is 1 mA input current yields approximately 1μA of photodiode current.) At $I_P = 1.6\mu$A. the slope of the V_{CE} = 5V curve is equal to -15,000 and the gain is β = 26,000; hence, $\partial \ln\beta/\partial \ln I_P \approx$ -0.25. If, for instance, the emitter degradation $\Delta\eta/\eta$ is -10%, then the second order term would improve the overall CTR degradation, i.e.,

$$\frac{\Delta CTR}{CTR} = \left(\frac{\Delta\eta}{\eta}\right) + \left(\frac{\Delta\eta}{\eta}\right)\left(\frac{\partial \ln\beta}{\partial \ln I_P}\right) + \ldots = -10\% + 2.5\% = -7.5\% \quad (17)$$

This improvement is what was expected while operating on the right side of the β maximum. In fact, with an I_F = 4 mA or $I_P \approx 4\mu$A, the term $\partial \ln\beta/\partial \ln I_P$ = -0.8, and again, if $\Delta\eta/\eta$ = -10%, the resulting ΔCTR/CTR = -2%, nearly cancelling the emitter's degradation.

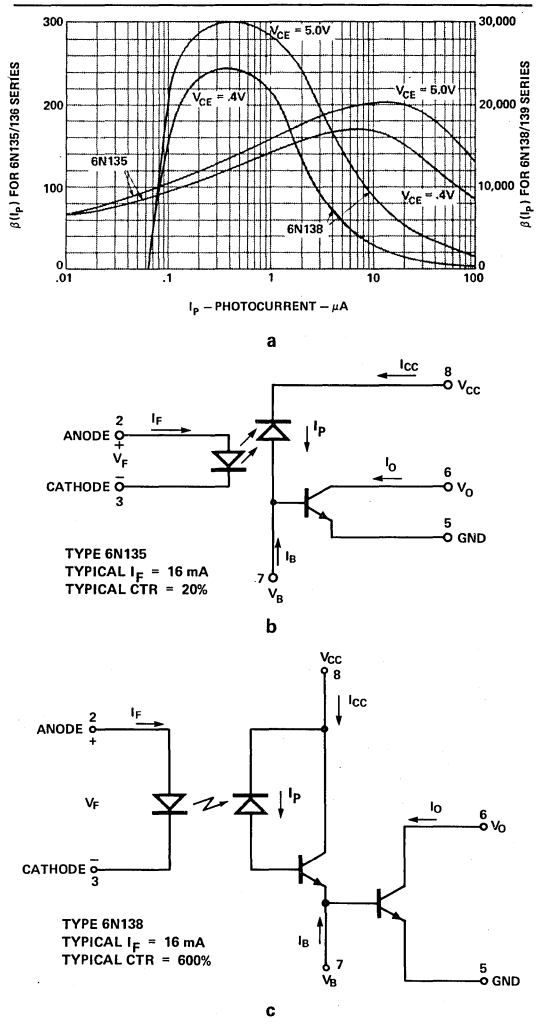


Figure 5. a) DC Current Gain, β, vs. Photocurrent, I_P, for 6N135 and 6N138 Optocouplers. Current Diagrams and Typical Values of I_F and CTR for Hewlett-Packard Optocouplers, b) 6N135, c) 6N138.

With the 6N135 optocoupler, Figure 5b operating at I_F = 10 mA, or $I_P \approx 10\mu A$, which corresponds to the maximum β point on the V_{CE} = .4V curve, the slope is zero and the total CTR degradation is basically the emitter's degradation.

Another subtle effect is seen from the third term in Equation (5), $(\Delta\beta/\beta)I_P$, over time. At constant I_P, β can increase or decrease by a few percent over 10,000 hours. This change is so small that the third term is generally neglected.

For the optocouplers containing an output amplifier, such as the 6N137, which switches abruptly about a particular threshold input current, the actual emitter degradation can be determined from Equations (11) and (13). An appropriate $I_{F_{initial}}$ can be determined to provide for adequate guard band current which will allow the optocoupler emitter to degrade while maintaining sufficient I_P to switch the amplifier. An actual design procedure to determine the needed $I_{F_{initial}}$ for proper operation of Hewlett-Packard optocouplers is given in the design examples section.

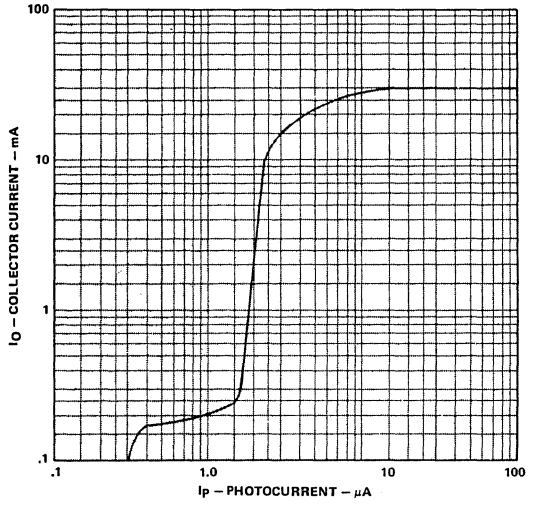


Figure 6. a) Output Current, I_O, vs. Photocurrent, I_P, for 6N137 Optocoupler.
b) Circuit Diagram and Typical Values of I_F and CTR for 6N137 Optocoupler.

MATRIX OF COEFFICIENTS

	25°C		85°C			
	$\bar{X}$	$\bar{X}+2\sigma$	$\bar{X}$		$\bar{X}+2\sigma$	
			R<6	6≤R	R<8	8≤R
A_o	4.95	9.7	6.8	5.0	15.0	11.0
α	.388	.428	.302	.467	.284	.430
	25°C		85°C			
	R≤1	R≥1	R≤1		R≥1	
$\alpha(R)$	$.19\ R^{.052}$	$.19\ R^{.32}$	$.32\ R^{.08}$		$.32\ R^{.30}$	
$\beta(R)$	.055	$.055\ R^{.68}$	$.11\ R^{.25}$		$.11\ R^{.65}$	
	25°C		85°C			
$\gamma(R)$	$.063\ R^{.30}$		$.154\ R^{.26}$			
$\delta(R)$	$.081\ R^{.38}$		$.196\ R^{.39}$			

Figure 7. Matrix of Coefficients.

APPLICATION NOTES

Procedure for Calculation of CTR Degradation

1. Specify I_{FS}, I_{FM}

2. Determine $R = I_{FS}/I_{FM} \leq 20$, $I_{FS} \leq 40$ mA — Degradation Model Equations (11) and (13) Valid

3. First Approximation of Degradation

$$\bar{D}_{\bar{x}} \text{ or } \bar{x}+2\sigma = A_o R^{\alpha} t^{n} \quad (\%)$$

with $\alpha \approx .4$, A_o (Figure 7), $n \approx .3$, t in 10^3 hours (D corresponds to I_{FS})

4. Calculate $\bar{I}_{FS}$ =

$$\begin{cases} 14.13 + 9.06 \log_{10} R \text{ @ } 25^\circ C & \text{Equation (7)} \\ 10.5 + 5.76 \log_{10} R \text{ @ } 85^\circ C & \text{Equation (8)} \end{cases}$$

If $I_{FS} \approx \bar{I}_{FS}$, Step 6 and the second terms in Equations (11) and (13) do not need to be calculated.

5. Calculate $n(R) = .0475 \log_{10} R + .25$

6. Calculate $S = \alpha(R) \log_{10} t + \beta(R)$ — $\alpha(R)$, $\beta(R)$ — Figure 7

$P = \gamma(R) \log_{10} t + \delta(R)$ — $\gamma(R)$, $\delta(R)$ — t in 10^3 hours

7. Calculate Mean, Mean + 2σ Degradation

$$D_{\bar{x}} = A_o R^{\alpha} t^{n(R)} + S\,[I_{FS} - \bar{I}_{FS}] \quad \% \quad \text{Equation (11)}$$

$$D_{\bar{x}+2\sigma} = A_o R^{\alpha} t^{n(R)} + [S + 2P]\,[I_{FS} - \bar{I}_{FS}] \quad \% \quad \text{Equation (13)}$$

(A_o, α via Figure 7, t in 10^3 hours)

8 For Second Order Effect, Determine Slope

$$\frac{\partial \ln \beta}{\partial \ln I_P} = \frac{1}{2.3\beta} \frac{\partial \beta}{\partial \log_{10} I_P}$$

Figure 5a — typical curves with an approximation for HP optocouplers of $I_F = 1$ mA yields $I_P \approx 1\mu A$

9a. Total CTR Degradation for Mean Distribution

$$\frac{\Delta CTR}{CTR} = D_{\bar{x}} + D_{\bar{x}} \frac{\partial \ln \beta}{\partial \ln I_P}$$

9b. Total CTR Degradation for Mean + 2σ Distribution

$$\frac{\Delta CTR}{CTR} = D_{\bar{x}+2\sigma} + D_{\bar{x}+2\sigma} \frac{\partial \ln \beta}{\partial \ln I_P}$$

Practical Application

A very common application of an optocoupler is to function as the interfacing element between digital logic. In this section, the designer will be shown an approach which will insure the initial and long term performance of such an interface, and take into account the practical aspects of the system that surrounds it. These system elements include the data rate, the logic families being interfaced, the variations of the power supply, the tolerances of the components used, the operational temperature range, and lastly the expected lifetime of the system.

The system data speed can be considered as the primary selection criteria for selecting a specific optocoupler family. Figure 9 lists the ranges of data rates for four Hewlett-Packard optocoupler families when driven at specified LED input current, I_F. With this table, and the knowledge of the system data rate requirements, it is possible to select an optimum coupler.

An example of an optocoupler interconnecting two logic gates is shown in Figure 8. A logic low level is insured when the saturated output sinking current, I_O, is greater than the combined sourcing currents of the pull-up resistor, and the logic low input current, I_{IL}, of the interconnecting gate. Using the coupler specifications selected from Figure 9 and the corresponding CTR (MIN) from Figure 10,

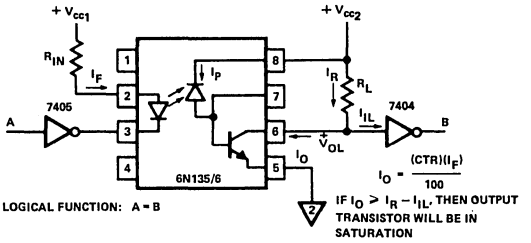


Figure 8. Typical Digital Interface Using an Optocoupler.

$$I_{F\,(MIN)} = \frac{V_{cc1\,(MIN)} - V_{F\,(MAX)} - V_{OL}}{R_{in\,(MAX)}} \quad (18)$$

$$I_{F\,(MAX)} = \frac{V_{cc1\,(MAX)} - V_{F\,(MIN)} - V_{OL}}{R_{in\,(MIN)}} \quad (19)$$

$$I_F = \frac{I_o \times 100}{CTR(MIN)} \quad (20)$$

$$R_{in} = \frac{V_{cc1} - V_F - V_{OL}}{I_F} \quad (21)$$

FAMILY	RZ DATA RATE BITS/S	INPUT CURRENT – I_F						
		.5mA	1.0mA	1.6mA	7.5mA	10mA	12mA	16mA
6N135/6 SINGLE TRANSISTOR	MIN							333k
	TYP							2M
6N138/9 SPLIT DARLINGTON	MIN	12k		22k			125k	
	TYP	100k		200k			840k	
4N45/6 DARLINGTON	MIN					1.8k		
	TYP		640			6.5k		
6N137 OPTICALLY COUPLED GATE	MIN				6.7M			
	TYP				10M			

Figure 9. Figure 13.5-2. Optocoupler Data Rates Specifications.

FAMILY		% CTR @ I_F = (mA)						TEMP °C	V_{OL}
		.5	1.0	1.6	5	10	16		
SINGLE TRANSISTOR	6N135						7	25	0.4
	6N136						19		
SPLIT DARLINGTON	6N138		300					0–70	0.4
	6N139	400	500					0–70	0.4
DARLINGTON	4N45		250			200		0–70	1.0
	4N46	350	500			200		0–70	1.0
OPTICALLY COUPLED GATE	6N137				400			0–70	0.6

Figure 10. Optocoupler CTR (MIN).

it is possible to determine from Equation (20) the minimum initial value of I_F for the coupler. The design criteria is that $I_O \geq I_{IL} + I_R$ for the V_{IL} specified in Figure 11.

Using Equation (21), the typical value of R_{in} can be calculated for the selected I_F and the logic low output voltage, V_{OL}, of the driving gate. The V_{OL} of the logic family is given in Figure 11. The next step is to determine the worst case value of the LED input current, I_F, resulting from the tolerance variations of the LED current limiting resistor, R_{in}, and the power supply voltage, V_{cc1}. The conditions of $I_{F(MIN)}$ and the initial CTR(MIN) are then used to determine the initial worst case value of $I_{O(MIN)}$. Conversely, the worst case CTR degradation will occur when the LED is stressed at $I_{F(MAX)}$ conditions; thus, $I_{F\ (MAX)}$ will be used to determine the worst case degradation of the optocoupler performance. Using the maximum V_{cc1} and the minimum R_{in} will accomplish this worst case calculation, as shown in Equation (19).

TTL FAMILY	I_{IL}	V_{IL}	I_{IH}	V_{IH}	I_{OL}	V_{OL}	I_{OH}	V_{OH}
74S	–2 mA	.8V	50 μA	2V	20 mA	.5V	–1000 μA	2.7V
74H	–2 mA	.8V	50 μA	2V	20 mA	.4V	– 500 μA	2.4V
74	–1.6 mA	.8V	40 μA	2V	16 mA	.4V	– 400 μA	2.4V
74LS	–.36 mA	.8V	20 μA	2V	8 mA	.5V	– 400 μA	2.7V
74L	–.18 mA	.7V	10 μA	2V	3.6 mA	.4V	– 200 μA	2.4V

Figure 11. Logic Interface Parameters.

The change in CTR from the initial value at time t = 0 to a final value at some later time can be compensated by choosing a value of R_L which is consistent with $I_{O(MIN)} - mI_{IL}$ at the end of system life. Equation (22) describes this worst case calculation.

(22)

$$R_{L\ (MIN)} \geq \left[\frac{V_{cc2\ (MAX)} - V_{OL}}{I_{F(MIN)} \cdot CTR(MIN) \cdot 1 - \left(\frac{D_{\bar{x}} + 2\sigma}{100} \right)} - mI_{IL} \right]$$

$D_{x} + 2\sigma$ = worst case CTR degradation

The selection of the maximum value of R_L is also of important in that its value insures that the collector is pulled up to the logic one voltage conditions, V_{IH}, under the conditions of maximum I_{OH} of the coupler, and the I_{IH} of the interconnecting gate.

(23)

$$R_{L\ (MAX)} \leq \frac{V_{cc2\ (MIN)} - V_{IH}}{I_{OH\ (MAX)} + m\, I_{IH}}$$

The selection of the value of R_L between the boundaries of $R_{L\ (MIN)}$, and $R_{L\ (MAX)}$ has certain trade offs. As in any open collector logic system, T_{PLH} increases with increasing R_L. Conversely, as R_L is increased above R_{LMIN}, a larger guardband between I_{OMIN} and $I_{IL} + I_R$ is achieved. Engineering judgement should be employed here to achieve the optimum trade off for desired performance.

Using the coefficient Figure 7 and Equations (11) and (13), the following examples are developed to demonstrate the methods of optocoupler system design in the presence of the mean and mean plus two sigma CTR degradation.

Example 1.

System Specifications

Data Rate	20 k bit NRZ
Logic Family	Standard TTL
Power Supply 1 & 2	5V ± 5
Component Tolerances	± 5%
Temperature Range	0 – 70°C
Expected System Lifetime	350 k hr (40 yr) at 50% system use time and 50% Data Duty Factor

Interface Specifications

Coupler 6N139

$CTR\ (MIN) = 500\% @ I_F = 1.6\ mA$
$V_{OL}\ (MAX) = .4V @ I_F = 1.6\ mA$
$I_{OH}\ (MAX) = 250\mu A @ V_{cc2} = 7V$
$V_F\ (MAX) = 1.7V @ I_F = 1.6\ mA$
$V_F\ (MIN) = 1.4V @ I_F = 1.6\ mA$
$V_F\ (TYP) = 1.6V @ I_F = 1.6\ mA$

Logic Standard TTL

$I_{IL} = 1.6\ mA$ $\quad I_{IH} = 40\mu A$
$V_{IL} = .8V$ $\quad V_{IH} = 2V$
$I_{OL} = 16\ mA$ $\quad I_{OH} = 400\mu A$
$V_{OL} = .4V$ $\quad V_{OH} = 2.4V$

Step 1. $R_{in\ (TYP)}$

$$R_{in} = \frac{V_{cc1} - V_{F\ (TYP)} - V_{OL}}{I_{F\ (TYP)}} \qquad (24)$$

$$R_{in} = \frac{5.0 - 1.6 - .4}{1.6 \times 10^{-3}} = 1.87k\Omega, \text{ select } 1.8k\Omega \pm 5\%$$

$R_{(MIN)} = 1710\Omega$
$R_{(MAX)} = 1890\Omega$

Step 2. $I_{F\ (MAX)}$

$$I_{F\ (MIN)} = \frac{V_{cc1\ (MIN)} - V_{F\ (MAX)} - V_{OL}}{R_{in\ (MAX)}} \qquad (25)$$

$$I_{F\ (MIN)} = \frac{4.75 - 1.7 - .4}{1890\Omega} = 1.4\ mA$$

Step 3. $I_{F\ (MAX)}$

$$I_{F\ (MAX)} = \frac{V_{cc1\ (MAX)} - V_{F\ (MIN)} - V_{OL}}{R_{in\ (MIN)}} \qquad (26)$$

$$I_{F\ (MAX)} = \frac{5.25 - 1.4 - .4}{1710\Omega} = 2.02\ mA$$

Step 4. Determine continuous operation time for LED emitter.

$$t_{\text{continuous lifetime}} = \left[t_{\text{system lifetime}}\right]\left[\text{Data Duty Factor}\right]\left[\text{System Use Duty Factor}\right]$$

$$= (40\ yr \times 8.76\ k\ hr/yr)(50\%)(50\%)$$

$$t_{\text{continuous lifetime}} = 87.60K\ hr$$

Step 5. Obtain the mean and mean + 2σ CTR degradation at $I_{F\ (MAX)}$ and $t_{\text{continuous lifetime}}$ either as an approximation from Figure 4 or by calculations as shown below.

Step 5a. Determine $D_{\bar{x}}$

$$D_{\bar{x}} = A_o t^{.25} + S\,[I_{FS} - \bar{I}_{FS}] \qquad (27)$$

$$D_{\bar{x}} = 4.95 t_{(k\ hr)}^{.25} + [.186 \log t_{(k\ hr)} + .055]$$

$$[I_{F\ (MAX)} - 14.13\ mA]$$

$$D_{\bar{x}} = 4.95\ (87.6)^{.25} + (.186 \log 87.6 + .055)$$

$$(2.02\ mA - 14.13\ mA)$$

$D_{\bar{x}} = 10.10\%$ for 40 yr system operation

Step 5b. Determine $\bar{D}_x + 2\sigma$

$$D_{\bar{x}} + 2\sigma = A_o t^{.25} + [S + 2P]\,[I_{FS} + \bar{I}_{FS}] \qquad (28)$$

$$D_{\bar{x}} + 2\sigma = 9.7 t_{(k\ hr)}^{.25} + [2\ (.063 \log t_{(k\ hr)} + .081)$$

$$+ (.186 \log t_{(k\ hr)} + .055)]$$

$$\times [I_{F\ (MAX)} - 14.13\ mA]$$

$$D_{\bar{x}+2\sigma} = 9.7\ (87.6)^{.25} + [2\ (.063 \log 87.6 + .081)$$

$$+ (.186 \log 87.6 + .055)]$$

$$\times [2.02\ mA - 14.13\ mA]$$

$$D_{\bar{x}+2\sigma} = 19.71\%$$

Step 6. Guardband the worst case value of CTR degradation.

It is often desirable to add some additional operating margin over and above conditions dictated by simple worst case analysis. The use of engineering judgement to increase the worst possible CTR degradation by an additional 5% margin would insure that the entire distribution would fall within the analysis. Thus,

$$D_{\bar{x}+2\sigma} + 5\% = 24.71\%$$

Step 7. Selecting $R_{L\ (MIN)}$ for guardbanded worst case

$D_{\bar{x}+2\sigma} + 5\%$, m = 1

(22)

$$R_{L(MIN)} \geq \frac{V_{cc2\ (MAX)} - V_{OL}}{\frac{I_{F(MIN)} \cdot CTR_{(MIN)} \cdot 1 - \left(\frac{D_{\bar{x}+2\sigma} + 5\%}{100}\right)}{100} - mI_{IL}}$$

$$R_{L(MIN)} \geq \frac{5.25 - .4}{\frac{1.4 \times 10^{-3} \cdot 500\% \cdot 1 - \left(\frac{24.71\%}{100}\right)}{100} - 1\ 1.6\ mA}$$

$$R_{L\ (MIN)} = 1.32k\Omega$$

Step 8. Select $R_{L\ (MAX)}$

$$R_{L\ (MAX)} \leq \frac{V_{cc2\ (MAX)} - V_{OL}}{I_{OH\ (MAX)} + mI_{IH}} \qquad (29)$$

$$R_{L\ (MAX)} \leq \frac{4.75 - 2.4}{250\mu A + 40\mu A} = 8.1k$$

The range of R_L is from 1.32kΩ to 8.1kΩ. It is desirable to select a pull-up resistor which optimizes both speed performance and additional I_O guardband. This criteria leads to a tradeoff between a value close to $R_{L\ (MIN)}$ for speed performance and one bordering near $R_{L(MAX)}$ for I_O guardbanding. In this design example, the system's lifetime has a higher priority than does the moderate speed performance demanded from the optocoupler. An R_L of 3.3kΩ ± 5% is selected under this condition.

An additional guardband of 5% was added to the worst case $D_{\bar{x}+2\sigma}$ CTR degradation guardband to insure that even a greater percentage of the distribution would be accounted for. The actual percentage difference between $I_{OL\ (MAX)}$ and $I_{O\ (MIN)}$ at the end of system life is shown below:

(30)

$$I_{O\ (MIN)} = \frac{CTR_{(MIN)} \cdot I_{F\ (MIN)} \cdot 1 - \left(\frac{\bar{D}_{\bar{x}+2\sigma}}{100}\right)}{100}$$

(31)

$$I_{OL\ (MAX)} = \frac{V_{cc2\ (MAX)} - V_{OL}}{R_{L\ (TYP-5\%)}} + m|I_{IL}|$$

$$\%\ Guardband = \left[1 - \frac{I_{OL\ (MAX)}}{I_{O\ (MIN)}}\right] X\ 100 \qquad (32)$$

For the example shown, the additional end of system life I_O guardband results from the selection of an R_L greater than the $R_{L\ (MIN)}$ as shown in Steps 9, 10, and 11.

Step 9. $I_{O\ (MIN)}$ at end of system life

$$I_{O\ (MIN)} = \frac{500\% \cdot 1.4\ mA \cdot \left(1 - \frac{19.17\%}{100}\right)}{100} = 5.65\ mA$$

Step 10. $I_{OL\ (MAX)}$ for worst case of $I_{R\ (MAX)} + I_{IL}$

(33)

$$I_{OL\ (MAX)} = \frac{5.25 - .4}{3.13k\Omega} + 1.6\ mA = 3.14\ mA$$

Step 11. % Guardband

$$\% = 1 - \frac{3.14\ mA}{5.65\ mA}\ 100 = 44.4\% \qquad (34)$$

Thus, this circuit interface design offers an additional 44.4% I_O guardband beyond the 19.71% required to compensate for the CTR change caused by 86.7k hr of continuous operation at an $I_{F\ (MAX)}$ of 2 mA. This extra guardband results from having chosen an $R_L = 3.3k$ rather than the lowest allowable value of R_L plus the engineering guardband chosen in Step 6.

Example 2.

System Specifications

Data Rate	250K bit NRZ
Logic Family	TTL to LSTTL
Power Supply 1 and 2	5V ± 5%
Component Tolerance	± 5%
Temperature Range	25°C
Expected System Lifetime	175 k hr (20 yr) at 50% System Use Time and 50% Data Duty Factor

Interface Conditions

Coupler 6N136

$CTR_{(MIN)}$ = 19% @ I_F = 16 mA
V_{OL} = .4V
I_{OH} = 500 nA @ V_{cc2} = 5.0V
$V_{F(TYP)}$ = 1.6V @ I_F = 16 mA
$V_{F(MIN)}$ = 1.5V @ I_F = 16 mA
$V_{F(MAX)}$ = 1.7V @ I_F = 16 mA

Logic LSTTL

I_{IL} = .36 mA I_{OL} = 8 mA
V_{IL} = .8V V_{OL} = .5V
I_{IH} = 40μA I_{OH} = 400μA
V_{IH} = 2V V_{OH} = 2.7V

Again using Figure 7, the data rate dictates the use of a 6N136 at an $I_{F\ (TYP)}$ of 16 mA. Using the same 12 step worst case analysis, it is possible to determine the values of R_{in}, R_L and the degree of guardbanding of I_O at end of system lifetime.

Step 1. R_{in} = 187Ω, select 180Ω ± 5%
$R_{L\ (MIN)}$ = 179Ω
$R_{L\ (MAX)}$ = 189Ω

Step 2. $I_{F\ (MIN)}$ = 14.02 mA

Step 3. $I_{F\ (MAX)}$ = 19 mA

Step 4. System Lifetime

t = 43.8k hr

Step 5. $D_{\bar{x}}$ and $D_{\bar{x}+2\sigma}$ for $I_{F\ (MAX)}$ of 19 mA

by calculation or from Figure 4

$D_{\bar{x}}$ = 14.5% } 43.8k hr
$D_{\bar{x}+2\sigma}$ = 28.5% } continuous lifetime

Step 6. Engineering Guardband of 5%,

$D_{\bar{x}+2\sigma}$ + 5% = 33.5%

Step 7. R_L selection with guardbanding of $D_{x+2\sigma}$ + 5%

$R_{L\ (MIN)}$ = 3.44kΩ

Step 8. $R_{L\ (MAX)}$ = 50kΩ

Step 9. $R_{L\ (TYP)}$ = 5.1kΩ ± 5%, $R_{L\ (TYP\ -\ 5\%)}$
= 4.84kΩ, $R_{L\ (MAX\ +\ 5\%)}$
= 5.35kΩ

Step 10. End of System Life $I_{O\ (MIN)}$

$I_{O\ (MIN)}$ = 1.5 mA

Step 11. $I_{OL\ (MAX)}$ = 1.36 mA

Step 12. Engineering % Guardband of $I_{O\ (MIN)}$ = 9.3%

Example 3.

If a particular design requirements specifies a maximum tolerable degradation over a system lifetime, the optimum value of $I_{F(TYP)}$ can be obtained from Figure 12. For example, if a maximum acceptable degradation, $D_{\bar{x}+2\sigma}$, is 40%, and a continuous operation of 400k hr is desired, this curve specifies that $I_{F\ (TYP)}$ should be less than or equal to 10 mA. A 400k hr continuous operation with 100% system duty factor as might be encountered in telephone switching equipment is equivalent to 45 years of system lifetime.

If a 6N139 split Darlington were used to interface an LSTTL logic gate with the system specifications stated, a collector pull-up resistor of as low as 160Ω could be used. If an R_L of 1k were selected, this optocoupler would offer an additional end of life guardband of 81.8%. This worst case analysis points out that with the knowledge of selecting proper values of R_L, the CTR performance of the

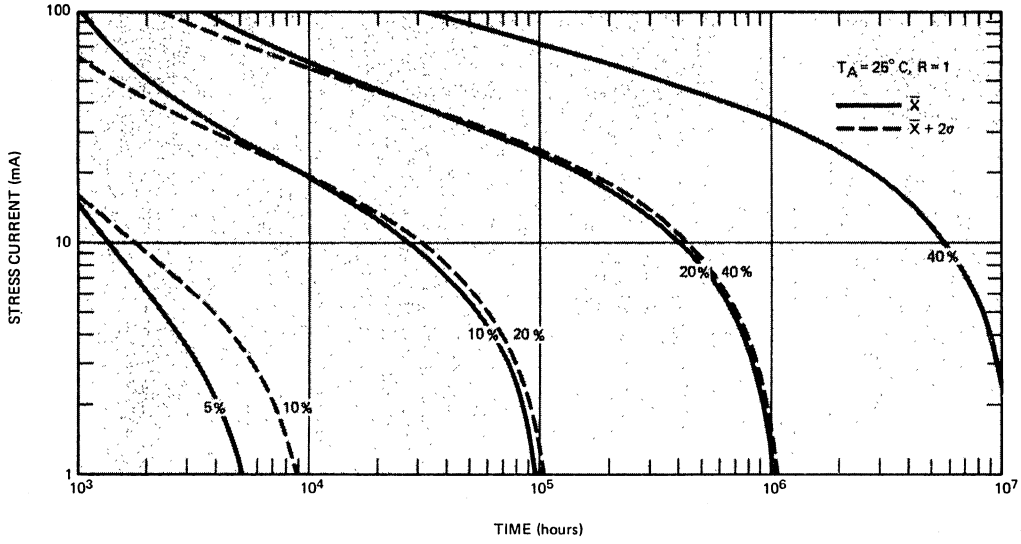


Figure 12. Stress Current (I_{FS}) vs. Time vs. % Degradation.

coupler far exceeds the normal MTBF requirements for most commercial electronic systems.

Consideration of the Optically Coupled Gate

System data speed requirements in the multi-megabit range can also be communicated through an optocoupler. The first three coupler families listed in Figure 9 are not applicable in these very high speed data interface applications; however, the optically coupled gate, 6N137, will function to speeds of up to 10 MHz. This type of coupler differs in operation from the single transistor and Darlington style units in that it exhibits a non-linear transfer relationship of I_F to I_O. This is shown in Figure 13. The relationship is described as a minimum threshold of LED input current, I_{Fth} which is required to cause the output transistor to sink the current supplied by the pull-up resistor and interconnected gate. As the LED degrades, the effect is that a larger value of $I_{F\,th}$ is required to create the same detector photodiode current necessary to switch the output gate.

In the previous interface examples, the worst case analysis and guardbanding is based on the output collector current, I_O. With the optically coupled gate, worst case guardbanding is concerned with the selection of the initial value of the I_F, which at end of system lifetime will generate the necessary threshold photocurrent demanded by the gate's amplifier to change state.

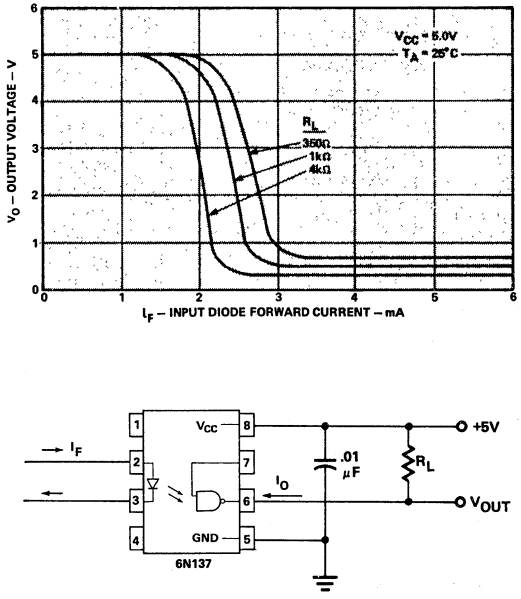


Figure 13. 6N137 Input – Output Characteristics.

The calculation of the required I_F to allow for worst case LED degradation is approached by guardbanding the guaranteed minimum isolator input current, I_{FH}, for a specified I_{OL} and V_{OL} interface. Equation (35) shows the relationship of the I_P to I_F for this coupler.

$$I_P \alpha (I_F)^n \quad \text{, where } 1.1 \leq n \leq 1.3 \tag{35}$$

Using the concept that the guardbanding of the initial value of I_F will result in a similarly guardbanded I_P, the relationship presented in Equation (36) results:

$$\left[1 - \frac{D_{\bar{x}} + 2\sigma}{100}\right] = \left[\frac{I_{PH}}{I_P}\right] = \left[\frac{I_{FH}}{I_F}\right]^n \tag{36}$$

$$I_F = \frac{I_{FH}}{\left[1 - \frac{D_{\bar{x}} + 2\sigma}{100}\right]^n} \tag{37}$$

The previous interface example showed that the first term of the $D_X + 2\sigma$ equation dominated the magnitude of the worst case degradation. This term, $A_o R^{\alpha} t^{n(R)}$, i.e., $(9.7\ t_{(k\ hr)}^{.25})$, does not contain an I_F current dependent term; thus, an approximation of the worst case LED degradation can be made that relates to the system's lifetime. This initial value of $D_X + 2\sigma$ can be used in Equation (37) to calculate the initial value of the I_F. With this initial I_F, a more accurate degradation value can be calculated using Equation (28). This procedure results in an iterative process to zero in on a value of I_F that will insure reliable operation.

The following example will illustrate this approach.

Example 4.

System Specifications

Data Rate	6 MHz NRZ
Logic Family	LSTTL to TTL
Power Supply 1 and 2	5V ± 5%
Component Tolerance	± 5%
Temperature Range	0 – 70°C
Expected System Lifetime	203k hr (23 yr) at 50% System Use Time and 50% Data Duty Factor

Step 1. Determine the continuous operation time for LED emitter

$$t_{\text{continuous lifetime}} = \left[t_{\text{system lifetime}}\right]\left[\text{Data Duty Factor}\right]\left[\text{System Use Factor}\right]$$

$$= \left[23\text{ yr}\ \ 8.76\text{k hr/yr}\right]\left[50\%\right]\left[50\%\right]$$

$$= 50.3\text{k hr}$$

Step 2. Calculate the worst case LED degradation

$$D_{x+2\sigma} \approx 9.7\ t_{(k\ hr)}^{.25}$$

$$D_{x+2\sigma} \approx 9.7\ (50.3)^{.25}$$

$$D_{x+2\sigma} \approx 26\%$$

Step 3. Calculate the first approximation of guardbanded I_F, n = 1.2

$$I_F = \frac{I_{FH}}{\left[1 - \frac{(\approx D_{\bar{x}} + 2\sigma)}{100}\right]^{1/n}} = \frac{5\text{ mA}}{.78} = 6.41\text{ mA}$$

Step 4. Calculate input resistor R_{in}

$$R_{in} \leq \frac{V_{cc1\ (MIN)} - V_{F\ (MAX)} - V_{OL}}{I_F}$$

$$R_{in} \leq \frac{4.75 - 1.7 - .4}{.00641}$$

$R_{in} \leq 413\Omega$ select $R_{in} = 390\Omega \pm 5\%$

Rin (MAX)

$R_{in\ (MAX)} = 409\Omega$

$R_{in\ (MIN)} = 370\Omega$

Step 5. Calculate the $I_{F\ (MAX)}$

$$I_{F\ (MAX)} = \frac{V_{cc1\ (MAX)} - V_{F\ (MIN)} - V_{OL}}{R_{in\ (MIN)}}$$

$$I_F = \frac{5.25 - 1.4 - .4}{370}$$

$I_F = 9.32$ mA

Step 6. Calculate the worst case $D_{\bar{x}} + 2\sigma$ for $I_{F\ (MAX)}$

$D_{\bar{x}} + 2\sigma = 25.8\% + .747\ (9.32\text{ mA} - 14.13\text{ mA})$

$D_{\bar{x}} + 2\sigma = 22.2\%$

APPENDIX

Step 7. Calculate the new minimum required I_F at end of life based on degradation found in Step 6.

$$I_{F(EOL)} = \frac{I_{FH}}{\left[1 - \frac{22.2}{100}\right]^{1/1.2}} = \frac{5}{.81} = 6.16\,mA$$

Step 8. Calculate $I_{F\,(MIN)}$

$$I_{F\,(MIN)} = \frac{V_{cc1\,(MIN)} - V_{F\,(MAX)} - V_{OL}}{R_{in\,(MAX)}}$$

$$I_{F\,(MIN)} = \frac{4.75 - 1.7 - .4}{409}$$

$$I_{F\,(MIN)} = 6.47\,mA$$

Step 9. $R_{L\,(MIN)}$, m = 1

$$R_{L\,(MIN)} = \frac{V_{cc2\,(MAX)} - V_{OL}}{I_{OL\,(MIN)} - mI_{IL}}$$

$$= \frac{5.25 - .6}{.016 - .0016}$$

$$R_{L\,(MIN)} = 332\Omega$$

Step 10. $R_{L\,(MAX)}$, m = 1

$$R_{L\,(MAX)} = \frac{V_{cc2\,(MAX)} - V_{OH}}{I_{OH\,(MAX)} + mI_{IH}}$$

$$R_{L\,(MAX)} = \frac{4.75 - 2.4}{250\mu A + 40\mu A}$$

$$R_{L\,(MAX)} = 8.1k\Omega$$

Step 11. Minimum % Emitter Degradation Guardband

$$\%_{(MIN)} = \left[1 - \frac{I_{F\,(EOL)}}{I_{F\,(MIN)}}\ 100\right] \qquad (38)$$

$$4.8\% = \left[1 - \frac{6.16\,mA}{6.47\,mA}\ 100\right]$$

where $I_{F\,(EOL)}$ represents the switching threshold at the end of life.

Step 12. Maximum % Emitter Degradation Guardband

$$\%_{(MAX)} = \left[1 - \frac{I_{F\,(EOL)}}{I_{F\,(MAX)}}\right] 100 \qquad (39)$$

$$34\% = \left[1 - \frac{6.16\,mA}{9.32\,mA}\ 100\right]$$

The conclusions that are to be drawn from this analysis are that as long as the $I_{F\,(MAX)}$ is less than $I_{\overline{FS}} = 14.13$ mA, the worst-worst case CTR degradation may be calculated using only the first term, $A_o R^{\alpha_t n(R)}$, of the $D_{\overline{X}+2\sigma}$ case. In the example presented, 26% degradation was determined from the first term, and when the more accurate calculation using Equation (28) was used, a 22% degradation resulted. The end of life I_F guardband may be calculated using Equations (38) and (39). Using Equation (38), the minimum guardband is 5.7%, and with Equation (39), the maximum guardband is 35%.

Appendix

- Hewlett-Packard Components Franchised Distributor and Representative Directory
- Hewlett-Packard Sales and Service Offices
- Profile and Inquiry Card

Optoelectronics Designer's Catalog 1979

Application Notes

Below is a brief summary of all Optoelectronic Application Notes which are not included in the catalog. Those that are included are listed also with corresponding page number. All of the Application Notes are available from your local HP Sales Office or nearest HP Components Franchised Distributor or Representative.

APPLICATION NOTE 931
Solid State Alphanumeric Display...Decoder/ Driver Circuitry

Hewlett-Packard offers a series of solid state displays capable of producing multiple alphanumeric characters utilizing 5 x 7 dot arrays of GaAsP light emitting diodes (LED's). These 5 x 7 dot arrays exhibit clear, easily read characters. In addition, each array is X-Y addressable to allow for a simple addressing, decoding, and driving scheme between the display module and external logic.

Methods of addressing, decoding and driving information to such an X-Y addressable matrix are covered in detail in this application note. The note starts with a general definition of the scanning or strobing technique used for this simplified addressing and then proceeds to describe horizontal and vertical strobing. Finally, a detailed circuit description is given for a practical vertical strobing application.

APPLICATION NOTE 934
5082-7300 Series Solid State Display Installation Techniques

The 5082-7300 series Numeric/Hexadecimal indicators are an excellent solution to most standard display problems in commercial, industrial and military applications. The unit integrates the display character and associated drive electronics in a single package. This advantage allows for space, pin and labor cost reductions, at the same time improving overall reliability.

The information presented in this note describes general methods of incorporating the -7730 into varied applications.

APPLICATION NOTE 937
Monolithic Seven Segment LED Display Installation Techniques

The Hewlett-Packard series of small end-stackable monolithic GaAsP displays are designed for strobing, a drive method that allows time sharing of the character generator among the digits in a display.

This Application Note begins with an explanation of the strobing technique, followed by a discussion of the uses and advantages of the right hand and center decimal point products.

Several circuits are given for typical applications. Finally, a discussion of interfacing to various data forms is presented along with comments on mounting the displays.

APPLICATION NOTE 939
High Speed Optically Coupled Isolators

Often designers are faced with the problem of providing circuit isolation in order to prevent ground loops and common mode signals. Typical devices for doing this have been relays, transformers and line receivers. However, both relays and transformers are low speed devices, incompatible with modern logic circuits. Line receiver circuits are fast enough, but are limited to a common mode voltage of 3 volts.

In addition, they do not protect very well against ground loop signals. Now Optically Coupled Isolators are available which solve most isolation problems.

This Application Note contains a description of Hewlett-Packard's high speed isolators, and discusses their applications in digital and analog systems.

APPLICATION NOTE 945
Photometry of Red LEDs

Nearly all LEDs are used either as discrete indicator lamps or as elements of a segmented or dot-matrix display. As such, they are viewed directly by human viewers, so the primary criteria for determining their performance is the judgment of a viewer. Equipment for measuring LED light output should, therefore, simulate human vision.

This Application Note will provide answers to these questions:

1. What to measure (definitions of terms)
2. How to measure it (apparatus arrangement)
3. Whose equipment to use (criteria for selection)

Optically coupled isolators make ideal line receivers for digital data transmission applications. They are especially useful for elimination of common mode interference between two isolated data transmission systems. This application note describes design considerations and circuit techniques with special emphasis on selection of line drivers, transmission lines, and line receiver termination for optimum data rate and common mode rejection. Both resistive and active terminations are described in detail. Specific techniques are described for multiplexing applications, and for common mode rejection and data rate enhancement.

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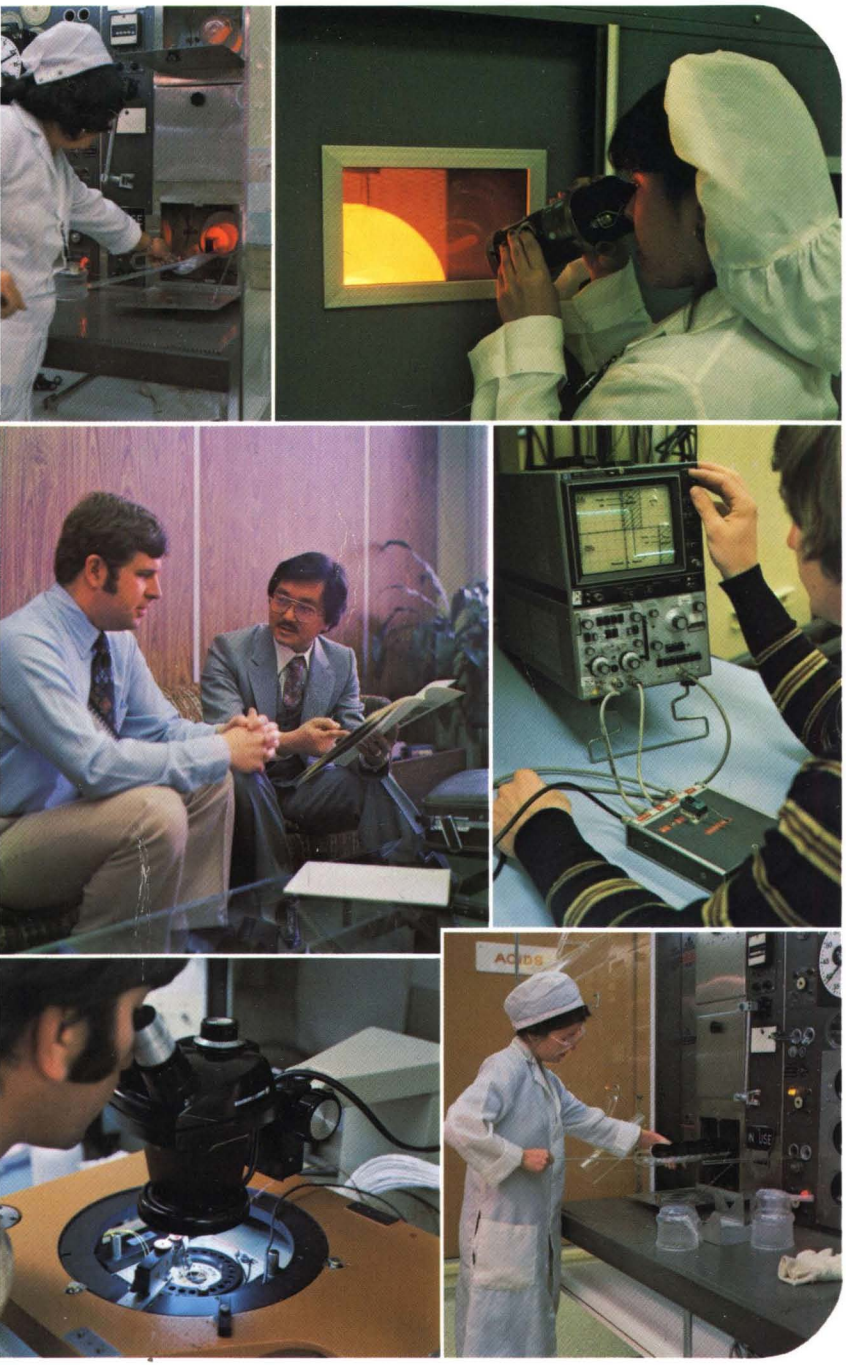

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Printed in U.S.A.

Revised from 5953-0372 D (4/78)
Data Subject to Change

5953-0400 D
(April, 1979)