ALL AMERICAN
2360 Qume Dr.
Suite C
San Jose, CA. 95131
408-943-1200 800-222-6001

HYUNDAI

Hyundai Electronics
Industries Co., Ltd.

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HYUNDAI
SEMICONDUCTOR

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DATA BOOK

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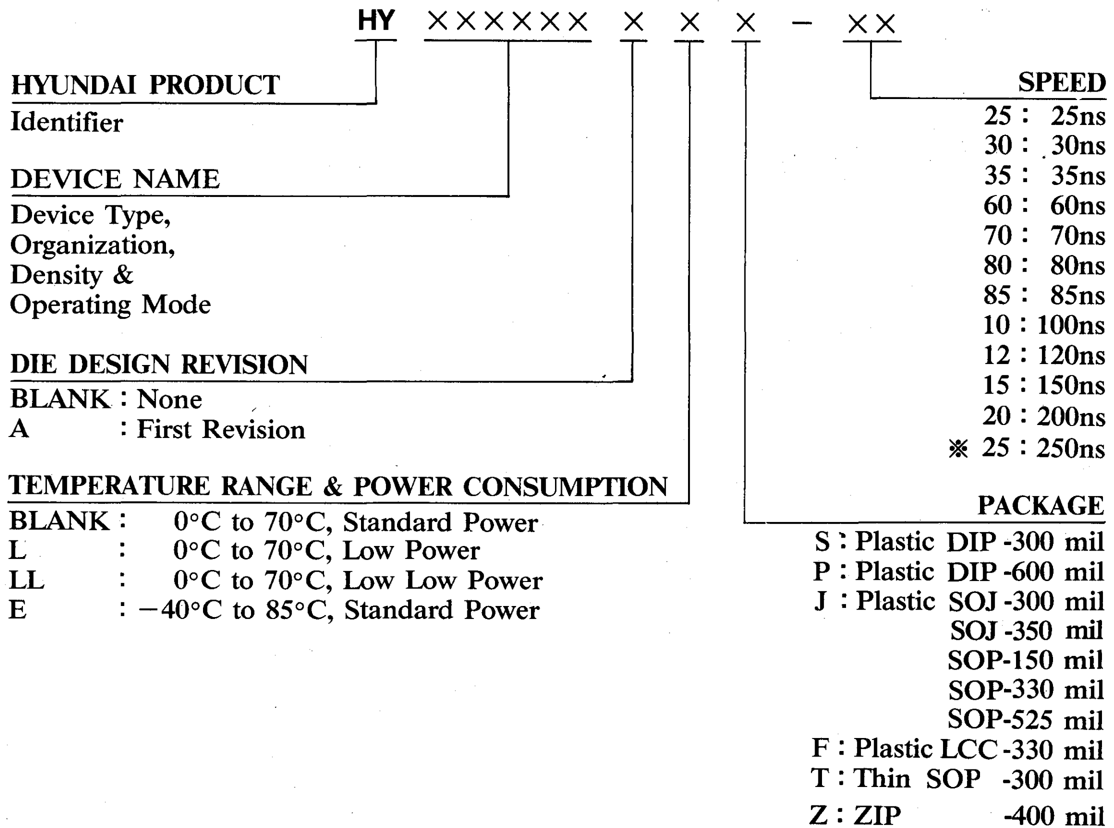
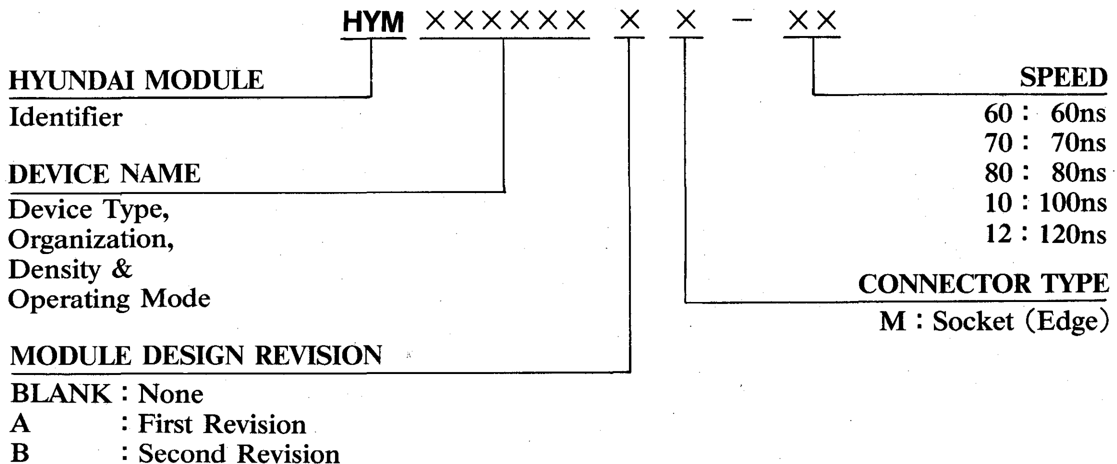
ORDERING INFORMATION

1. COMPONENT



2. MODULE



※ MASK ROM only

QUICK REFERENCE

1. DRAM

DENSITY	PART NO	ORGANIZATION	t_{RAC} ns	t_{PC} ns	I_{DD1} mA	I_{DD2} mA	I_{DD5} mA	t_{REF} cycle/ms	PACKAGE
256K bit	HY53C256S-70	256K × 1	70	50	70	3	2	256/4	16Pin PDIP
	HY53C256S-80	256K × 1	80	55	60	3	2	256/4	16Pin PDIP
	HY53C256S-10	256K × 1	100	60	50	3	2	256/4	16Pin PDIP
	HY53C256S-12	256K × 1	120	70	45	3	2	256/4	16Pin PDIP
	HY53C256F-70	256K × 1	70	50	70	3	2	256/4	18Pin PLCC
	HY53C256F-80	256K × 1	80	55	60	3	2	256/4	18Pin PLCC
	HY53C256F-10	256K × 1	100	60	50	3	2	256/4	18Pin PLCC
	HY53C256F-12	256K × 1	120	70	45	3	2	256/4	18Pin PLCC
	HY53C256LS-70	256K × 1	70	50	70	2	1	256/4	16Pin PDIP
	HY53C256LS-80	256K × 1	80	55	60	2	1	256/4	16Pin PDIP
	HY53C256LS-10	256K × 1	100	60	50	2	1	256/4	16Pin PDIP
	HY53C256LS-12	256K × 1	120	70	45	2	1	256/4	16Pin PDIP
	HY53C256LF-70	256K × 1	70	50	70	2	1	256/4	18Pin PLCC
	HY53C256LF-80	256K × 1	80	55	60	2	1	256/4	18Pin PLCC
	HY53C256LF-10	256K × 1	100	60	50	2	1	256/4	18Pin PLCC
	HY53C256LF-12	256K × 1	120	70	45	2	1	256/4	18Pin PLCC
	HY53C464S-70	64K × 4	70	50	70	3	2	256/4	18Pin PDIP
	HY53C464S-80	64K × 4	80	55	60	3	2	256/4	18Pin PDIP
	HY53C464S-10	64K × 4	100	60	50	3	2	256/4	18Pin PDIP
	HY53C464S-12	64K × 4	120	70	45	3	2	256/4	18Pin PDIP
	HY53C464F-70	64K × 4	70	50	70	3	2	256/4	18Pin PLCC
	HY53C464F-80	64K × 4	80	55	60	3	2	256/4	18Pin PLCC
	HY53C464F-10	64K × 4	100	60	50	3	2	256/4	18Pin PLCC
	HY53C464F-12	64K × 4	120	70	45	3	2	256/4	18Pin PLCC
	HY53C464LS-70	64K × 4	70	50	70	2	1	256/4	18Pin PDIP
	HY53C464LS-80	64K × 4	80	55	60	2	1	256/4	18Pin PDIP
	HY53C464LS-10	64K × 4	100	60	50	2	1	256/4	18Pin PDIP
	HY53C464LS-12	64K × 4	120	70	45	2	1	256/4	18Pin PDIP
	HY53C464LF-70	64K × 4	70	50	70	2	1	256/4	18Pin PLCC
	HY53C464LF-80	64K × 4	80	55	60	2	1	256/4	18Pin PLCC
	HY53C464LF-10	64K × 4	100	60	50	2	1	256/4	18Pin PLCC
	HY53C464LF-12	64K × 4	120	70	45	2	1	256/4	18Pin PLCC
1M bit	HY51C1000S-80	1M × 1	80	45	95	2.5	1.5	512/8	18Pin PDIP
	HY51C1000S-10	1M × 1	100	55	75	2.5	1.5	512/8	18Pin PDIP
	HY51C1000S-12	1M × 1	120	65	70	2.5	1.5	512/8	18Pin PDIP
	HY51C1000J-80	1M × 1	80	45	95	2.5	1.5	512/8	20/26Pin SOJ
	HY51C1000J-10	1M × 1	100	55	75	2.5	1.5	512/8	20/26Pin SOJ
	HY51C1000J-12	1M × 1	120	65	70	2.5	1.5	512/8	20/26Pin SOJ

DRAM(continued)

DENSITY	PART NO	ORGANIZATION	t_{RAC} ns	t_{PC} ns	I_{DD1} mA	I_{DD2} mA	I_{DD5} mA	t_{REF} cycle/ms	PACKAGE
1M bit	HY51C4256S-80	256K × 4	80	50	95	2.5	1.5	512/8	20Pin PDIP
	HY51C4256S-10	256K × 4	100	65	75	2.5	1.5	512/8	20Pin PDIP
	HY51C4256S-12	256K × 4	120	75	70	2.5	1.5	512/8	20Pin PDIP
	HY51C4256J-80	256K × 4	80	50	95	2.5	1.5	512/8	20/26Pin SOJ
	HY51C4256J-10	256K × 4	100	65	75	2.5	1.5	512/8	20/26Pin SOJ
	HY51C4256J-12	256K × 4	120	75	70	2.5	1.5	512/8	20/26Pin SOJ
	HY531000S-60	1M × 1	60	40	85	2	1	512/8	18Pin PDIP
	HY531000S-70	1M × 1	70	40	75	2	1	512/8	18Pin PDIP
	HY531000S-80	1M × 1	80	45	65	2	1	512/8	18Pin PDIP
	HY531000S-10	1M × 1	100	55	55	2	1	512/8	18Pin PDIP
	HY531000J-60	1M × 1	60	40	85	2	1	512/8	20/26Pin SOJ
	HY531000J-70	1M × 1	70	40	75	2	1	512/8	20/26Pin SOJ
	HY531000J-80	1M × 1	80	45	65	2	1	512/8	20/26Pin SOJ
	HY531000J-10	1M × 1	100	55	55	2	1	512/8	20/26Pin SOJ
	HY531000AS-60	1M × 1	60	40	85	2	1	512/8	18Pin PDIP
	HY531000AS-70	1M × 1	70	40	75	2	1	512/8	18Pin PDIP
	HY531000AS-80	1M × 1	80	45	65	2	1	512/8	18Pin PDIP
	HY531000AJ-60	1M × 1	60	40	85	2	1	512/8	20/26Pin SOJ
	HY531000AJ-70	1M × 1	70	40	75	2	1	512/8	20/26Pin SOJ
	HY531000AJ-80	1M × 1	80	45	65	2	1	512/8	20/26Pin SOJ
	* HY531000AZ-60	1M × 1	60	40	85	2	1	512/8	20Pin ZIP
	* HY531000AZ-70	1M × 1	70	40	75	2	1	512/8	20Pin ZIP
	* HY531000AZ-80	1M × 1	80	45	65	2	1	512/8	20Pin ZIP
	HY531000ALS-60	1M × 1	60	40	85	2	0.2	512/64	18Pin PDIP
	HY531000ALS-70	1M × 1	70	40	75	2	0.2	512/64	18Pin PDIP
	HY531000ALS-80	1M × 1	80	45	65	2	0.2	512/64	18Pin PDIP
	HY531000ALJ-60	1M × 1	60	40	85	2	0.2	512/64	20/26Pin SOJ
	HY531000ALJ-70	1M × 1	70	40	75	2	0.2	512/64	20/26Pin SOJ
	HY531000ALJ-80	1M × 1	80	45	65	2	0.2	512/64	20/26Pin SOJ
	* HY531000ALZ-60	1M × 1	60	40	85	2	0.2	512/64	20Pin ZIP
	* HY531000ALZ-70	1M × 1	70	40	75	2	0.2	512/64	20Pin ZIP
	* HY531000ALZ-80	1M × 1	80	45	65	2	0.2	512/64	20Pin ZIP
	HY534256S-60	256K × 4	60	40	90	2	1	512/8	20Pin PDIP
	HY534256S-70	256K × 4	70	40	80	2	1	512/8	20Pin PDIP
	HY534256S-80	256K × 4	80	45	70	2	1	512/8	20Pin PDIP
	HY534256S-10	256K × 4	100	55	60	2	1	512/8	20Pin PDIP
	HY534256J-60	256K × 4	60	40	90	2	1	512/8	20/26Pin SOJ
	HY534256J-70	256K × 4	70	40	80	2	1	512/8	20/26Pin SOJ
	HY534256J-80	256K × 4	80	45	70	2	1	512/8	20/26Pin SOJ
	HY534256J-10	256K × 4	100	55	60	2	1	512/8	20/26Pin SOJ

REMARK : 1. All the above DRAMs employ Fast Page Mode for fast access operation.
2. Refresh mode of all the above DRAMs can be selected or combined among $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden Refresh cycles.
3. (*) under development

2

DRAM(continued)

DENSITY	PART NO	ORGANIZATION	t_{RAC} ns	t_{PC} ns	I_{DD1} mA	I_{DD2} mA	I_{DDS} mA	t_{REF} cycle/ms	PACKAGE
1M bit	HY534256AS-60	256K × 4	60	40	90	2	0.2	512/8	20Pin PDIP
	HY534256AS-70	256K × 4	70	40	80	2	0.2	512/8	20Pin PDIP
	HY534256AS-80	256K × 4	80	45	70	2	0.2	512/8	20Pin PDIP
	HY534256AJ-60	256K × 4	60	40	90	2	0.2	512/8	20/26Pin SOJ
	HY534256AJ-70	256K × 4	70	40	80	2	0.2	512/8	20/26Pin SOJ
	HY534256AJ-80	256K × 4	80	45	70	2	0.2	512/8	20/26Pin SOJ
	*HY534256AZ-60	256K × 4	60	40	90	2	0.2	512/8	20Pin ZIP
	*HY534256AZ-70	256K × 4	70	40	80	2	0.2	512/8	20Pin ZIP
	*HY534256AZ-80	256K × 4	80	45	70	2	0.2	512/8	20Pin ZIP
	HY534256ALS-60	256K × 4	60	40	90	2	0.2	512/64	20Pin PDIP
	HY534256ALS-70	256K × 4	70	40	80	2	0.2	512/64	20Pin PDIP
	HY534256ALS-80	256K × 4	80	45	70	2	0.2	512/64	20Pin PDIP
	HY534256ALJ-60	256K × 4	60	40	90	2	0.2	512/64	20/26Pin SOJ
	HY534256ALJ-70	256K × 4	70	40	80	2	0.2	512/64	20/26Pin SOJ
	HY534256ALJ-80	256K × 4	80	45	70	2	0.2	512/64	20/26Pin SOJ
	*HY534256ALZ-60	256K × 4	60	40	90	2	0.2	512/64	20Pin ZIP
	*HY534256ALZ-70	256K × 4	70	40	80	2	0.2	512/64	20Pin ZIP
	*HY534256ALZ-80	256K × 4	80	45	70	2	0.2	512/64	20Pin ZIP
4M bit	HY514100J-70	4M × 1	70	50	90	2	1	1024/16	20/26Pin SOJ
	HY514100J-80	4M × 1	80	50	80	2	1	1024/16	20/26Pin SOJ
	HY514100J-10	4M × 1	100	60	70	2	1	1024/16	20/26Pin SOJ
	HY514100AJ-60	4M × 1	60	40	105	2	1	1024/16	20/26Pin SOJ
	HY514100AJ-70	4M × 1	70	45	95	2	1	1024/16	20/26Pin SOJ
	HY514100AJ-80	4M × 1	80	55	85	2	1	1024/16	20/26Pin SOJ
	HY514100AT-60	4M × 1	60	40	105	2	1	1024/16	20/26Pin TSOP
	HY514100AT-70	4M × 1	70	45	95	2	1	1024/16	20/26Pin TSOP
	HY514100AT-80	4M × 1	80	55	85	2	1	1024/16	20/26Pin TSOP
	*HY514100AZ-60	4M × 1	60	40	105	2	1	1024/16	20Pin ZIP
	*HY514100AZ-70	4M × 1	70	45	95	2	1	1024/16	20Pin ZIP
	*HY514100AZ-80	4M × 1	80	55	85	2	1	1024/16	20Pin ZIP
	HY514100ALJ-60	4M × 1	60	40	105	2	0.2	1024/128	20/26Pin SOJ
	HY514100ALJ-70	4M × 1	70	45	95	2	0.2	1024/128	20/26Pin SOJ
	HY514100ALJ-80	4M × 1	80	55	85	2	0.2	1024/128	20/26Pin SOJ
	HY514100ALT-60	4M × 1	60	40	105	2	0.2	1024/128	20/26Pin TSOP
	HY514100ALT-70	4M × 1	70	45	95	2	0.2	1024/128	20/26Pin TSOP
	HY514100ALT-80	4M × 1	80	55	85	2	0.2	1024/128	20/26Pin TSOP
	*HY514100ALZ-60	4M × 1	60	40	105	2	0.2	1024/128	20Pin ZIP
	*HY514100ALZ-70	4M × 1	70	45	95	2	0.2	1024/128	20Pin ZIP
	*HY514100ALZ-80	4M × 1	80	55	85	2	0.2	1024/128	20Pin ZIP

REMARK : 1. All the above DRAMs employ Fast Page Mode for fast access operation.

2. Refresh mode of all the above DRAMs can be selected or combined among $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden Refresh cycles.

3. (*) under development

DRAM(continued)

DENSITY	PART NO	ORGANIZATION	t_{RAC} ns	t_{PC} ns	I_{DD1} mA	I_{DD2} mA	I_{DD5} mA	t_{REF} cycle/ms	PACKAGE
4M bit	HY514400J-70	1M × 4	70	50	95	2	1	1024/16	20/26Pin SOJ
	HY514400J-80	1M × 4	80	50	85	2	1	1024/16	20/26Pin SOJ
	HY514400J-10	1M × 4	100	60	75	2	1	1024/16	20/26Pin SOJ
	HY514400AJ-60	1M × 4	60	40	110	2	1	1024/16	20/26Pin SOJ
	HY514400AJ-70	1M × 4	70	45	100	2	1	1024/16	20/26Pin SOJ
	HY514400AJ-80	1M × 4	80	55	90	2	1	1024/16	20/26Pin SOJ
	HY514400AT-60	1M × 4	60	40	110	2	1	1024/16	20/26Pin TSOP
	HY514400AT-70	1M × 4	70	45	100	2	1	1024/16	20/26Pin TSOP
	HY514400AT-80	1M × 4	80	55	90	2	1	1024/16	20/26Pin TSOP
	*HY514400AZ-60	1M × 4	60	40	110	2	1	1024/16	20Pin ZIP
	*HY514400AZ-70	1M × 4	70	45	100	2	1	1024/16	20Pin ZIP
	*HY514400AZ-80	1M × 4	80	55	90	2	1	1024/16	20Pin ZIP
	HY514400ALJ-60	1M × 4	60	40	110	2	0.2	1024/128	20/26Pin SOJ
	HY514400ALJ-70	1M × 4	70	45	100	2	0.2	1024/128	20/26Pin SOJ
	HY514400ALJ-80	1M × 4	80	55	90	2	0.2	1024/128	20/26Pin SOJ
	HY514400ALT-60	1M × 4	60	40	110	2	0.2	1024/128	20/26Pin TSOP
	HY514400ALT-70	1M × 4	70	45	100	2	0.2	1024/128	20/26Pin TSOP
	HY514400ALT-80	1M × 4	80	55	90	2	0.2	1024/128	20/26Pin TSOP
	*HY514400ALZ-60	1M × 4	60	40	110	2	0.2	1024/128	20Pin ZIP
	*HY514400ALZ-70	1M × 4	70	45	100	2	0.2	1024/128	20Pin ZIP
	*HY514400ALZ-80	1M × 4	80	55	90	2	0.2	1024/128	20Pin ZIP
	HY514410AJ-60	1M × 4	60	40	110	2	1	1024/16	20/26Pin SOJ
	HY514410AJ-70	1M × 4	70	45	100	2	1	1024/16	20/26Pin SOJ
	HY514410AJ-80	1M × 4	80	55	90	2	1	1024/16	20/26Pin SOJ
	HY514410AT-60	1M × 4	60	40	110	2	1	1024/16	20/26Pin TSOP
	HY514410AT-70	1M × 4	70	45	100	2	1	1024/16	20/26Pin TSOP
	HY514410AT-80	1M × 4	80	55	90	2	1	1024/16	20/26Pin TSOP
	*HY514410AZ-60	1M × 4	60	40	110	2	1	1024/16	20Pin ZIP
	*HY514410AZ-70	1M × 4	70	45	100	2	1	1024/16	20Pin ZIP
	*HY514410AZ-80	1M × 4	80	55	90	2	1	1024/16	20Pin ZIP
	HY514410ALJ-60	1M × 4	60	40	110	2	0.2	1024/128	20/26Pin SOJ
	HY514410ALJ-70	1M × 4	70	45	100	2	0.2	1024/128	20/26Pin SOJ
	HY514410ALJ-80	1M × 4	80	55	90	2	0.2	1024/128	20/26Pin SOJ
	HY514410ALT-60	1M × 4	60	40	110	2	0.2	1024/128	20/26Pin TSOP
	HY514410ALT-70	1M × 4	70	45	100	2	0.2	1024/128	20/26Pin TSOP
	HY514410ALT-80	1M × 4	80	55	90	2	0.2	1024/128	20/26Pin TSOP
	*HY514410ALZ-60	1M × 4	60	40	110	2	0.2	1024/128	20Pin ZIP
	*HY514410ALZ-70	1M × 4	70	45	100	2	0.2	1024/128	20Pin ZIP
	*HY514410ALZ-80	1M × 4	80	55	90	2	0.2	1024/128	20Pin ZIP
	HY524800J-70	512K × 8	70	45	135	2	1	1024/16	28Pin SOJ
	HY524800J-80	512K × 8	80	50	115	2	1	1024/16	28Pin SOJ

REMARK : 1. All the above DRAMs employ Fast Page Mode for fast access operation.

2. Refresh mode of all the above DRAMs can be selected or combined among $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden Refresh cycles.

3. (*) under development

2. DRAM MODULE

DENSITY	PART NO	ORGANIZATION	t_{RAC} ns	t_{PC} ns	I_{DD1} mA	I_{DD2} mA	I_{DD5} mA	t_{REF} cycle/ms	CONNECTOR TYPE
2M bit	HYM5C8256M-70	256K × 8	70	50	560	16	8	256/4	30Pin Socket
	HYM5C8256M-80	256K × 8	80	55	480	16	8	256/4	30Pin Socket
	HYM5C8256M-10	256K × 8	100	60	400	16	8	256/4	30Pin Socket
	HYM5C8256M-12	256K × 8	120	70	360	16	8	256/4	30Pin Socket
	HYM58256AM-60	256K × 8	60	40	180	4	2	512/8	30Pin Socket
	HYM58256AM-70	256K × 8	70	40	160	4	2	512/8	30Pin Socket
	HYM58256AM-80	256K × 8	80	45	140	4	2	512/8	30Pin Socket
	HYM58256AM-10	256K × 8	100	55	120	4	2	512/8	30Pin Socket
2.25M bit	HYM5C9256M-70	256K × 9	70	50	630	18	9	256/4	30Pin Socket
	HYM5C9256M-80	256K × 9	80	55	540	18	9	256/4	30Pin Socket
	HYM5C9256M-10	256K × 9	100	60	450	18	9	256/4	30Pin Socket
	HYM5C9256M-12	256K × 9	120	70	405	18	9	256/4	30Pin Socket
	HYM59256AM-70	256K × 9	70	50	230	6	3	512/8	30Pin Socket
	HYM59256AM-80	256K × 9	80	55	200	6	3	512/8	30Pin Socket
	HYM59256AM-10	256K × 9	100	60	170	6	3	512/8	30Pin Socket
8M bit	HYM581000M-60	1M × 8	60	40	680	16	8	512/8	30Pin Socket
	HYM581000M-70	1M × 8	70	40	600	16	8	512/8	30Pin Socket
	HYM581000M-80	1M × 8	80	45	520	16	8	512/8	30Pin Socket
	HYM581000M-10	1M × 8	100	55	440	16	8	512/8	30Pin Socket
	HYM581000AM-70	1M × 8	70	50	190	4	2	1024/16	30Pin Socket
	HYM581000AM-80	1M × 8	80	50	170	4	2	1024/16	30Pin Socket
	HYM581000AM-10	1M × 8	100	60	150	4	2	1024/16	30Pin Socket
	HYM581000BM-60	1M × 8	60	40	220	4	2	1024/16	30Pin Socket
	HYM581000BM-70	1M × 8	70	45	200	4	2	1024/16	30Pin Socket
	HYM581000BM-80	1M × 8	80	55	180	4	2	1024/16	30Pin Socket
	HYM581000BLM-60	1M × 8	60	40	220	4	0.4	1024/128	30Pin Socket
	HYM581000BLM-70	1M × 8	70	45	200	4	0.4	1024/128	30Pin Socket
	HYM581000BLM-80	1M × 8	80	55	180	4	0.4	1024/128	30Pin Socket
9M bit	HYM591000M-60	1M × 9	60	40	765	18	9	512/8	30Pin Socket
	HYM591000M-70	1M × 9	70	40	675	18	9	512/8	30Pin Socket
	HYM591000M-80	1M × 9	80	45	585	18	9	512/8	30Pin Socket
	HYM591000M-10	1M × 9	100	55	495	18	9	512/8	30Pin Socket
	HYM591000AM-70	1M × 9	70	50	265	6	3	1024/16	30Pin Socket
	HYM591000AM-80	1M × 9	80	50	235	6	3	1024/16	30Pin Socket
	HYM591000AM-10	1M × 9	100	60	205	6	3	1024/16	30Pin Socket
	HYM591000BM-60	1M × 9	60	40	305	6	3	1024/16	30Pin Socket
	HYM591000BM-70	1M × 9	70	45	275	6	3	1024/16	30Pin Socket
	HYM591000BM-80	1M × 9	80	55	245	6	3	1024/16	30Pin Socket
	HYM591000BLM-60	1M × 9	60	40	305	6	0.6	1024/128	30Pin Socket
	HYM591000BLM-70	1M × 9	70	45	275	6	0.6	1024/128	30Pin Socket
	HYM591000BLM-80	1M × 9	80	55	245	6	0.6	1024/128	30Pin Socket

REMARK : 1. All the above DRAM MODULEs employ Fast Page Mode for fast access operation.
2. Refresh mode of all the above DRAM MODULEs can be selected or combined among $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden Refresh cycles.

DRAM MODULE(continued)

DENSITY	PART NO	ORGANIZATION	t_{RAC} ns	t_{PC} ns	I_{DD1} mA	I_{DD2} mA	I_{DD5} mA	t_{REF} cycle/ms	CONNECTOR TYPE
32M bit	HYM584000M-70	4M × 8	70	50	720	16	8	1024/16	30Pin Socket
	HYM584000M-80	4M × 8	80	50	640	16	8	1024/16	30Pin Socket
	HYM584000M-10	4M × 8	100	60	560	16	8	1024/16	30Pin Socket
	HYM584000AM-60	4M × 8	60	40	840	16	8	1024/16	30Pin Socket
	HYM584000AM-70	4M × 8	70	45	760	16	8	1024/16	30Pin Socket
	HYM584000AM-80	4M × 8	80	55	680	16	8	1024/16	30Pin Socket
	HYM584000ALM-60	4M × 8	60	40	840	16	1.6	1024/128	30Pin Socket
	HYM584000ALM-70	4M × 8	70	45	760	16	1.6	1024/128	30Pin Socket
	HYM584000ALM-80	4M × 8	80	55	680	16	1.6	1024/128	30Pin Socket
	HYM532100M-70	1M × 32	70	50	760	16	8	1024/16	72Pin Socket
	HYM532100M-80	1M × 32	80	50	680	16	8	1024/16	72Pin Socket
	HYM532100M-10	1M × 32	100	60	600	16	8	1024/16	72Pin Socket
36M bit	HYM594000M-70	4M × 9	70	50	810	18	9	1024/16	30Pin Socket
	HYM594000M-80	4M × 9	80	50	720	18	9	1024/16	30Pin Socket
	HYM594000M-10	4M × 9	100	60	630	18	9	1024/16	30Pin Socket
	HYM594000AM-60	4M × 9	60	40	947	18	9	1024/16	30Pin Socket
	HYM594000AM-70	4M × 9	70	45	855	18	9	1024/16	30Pin Socket
	HYM594000AM-80	4M × 9	80	55	765	18	9	1024/16	30Pin Socket
	HYM594000ALM-60	4M × 9	60	40	945	18	1.8	1024/128	30Pin Socket
	HYM594000ALM-70	4M × 9	70	45	855	18	1.8	1024/128	30Pin Socket
	HYM594000ALM-80	4M × 9	80	55	765	18	1.8	1024/128	30Pin Socket
	HYM536100M-70	1M × 36	70	50	1046	24	12	1024/16	72Pin Socket
	HYM536100M-80	1M × 36	80	50	940	24	12	1024/16	72Pin Socket
	HYM536100M-10	1M × 36	100	60	820	24	12	1024/16	72Pin Socket

REMARK : 1. All the above DRAM MODULEs employ Fast Page Mode for fast access operation.
2. Refresh mode of all the above DRAM MODULEs can be selected or combined among $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, and Hidden Refresh cycles.

3. SRAM

DENSITY	PART NO	ORGANIZATION	t_{AA} ns	I_{CC1} mA	I_{SB} mA	I_{SB1} μA	V_{DR} V	I_{CCDR} μA	PACKAGE
16K bit	HY6116AP-85	2K × 8	85	60	3	50	NA	NA	24Pin PDIP
	HY6116AP-10	2K × 8	100	60	3	50	NA	NA	24Pin PDIP
	HY6116AP-12	2K × 8	120	60	3	50	NA	NA	24Pin PDIP
	HY6116AP-15	2K × 8	150	60	3	50	NA	NA	24Pin PDIP
	HY6116ALP-85	2K × 8	85	60	3	5	2	2	24Pin PDIP
	HY6116ALP-10	2K × 8	100	60	3	5	2	2	24Pin PDIP
	HY6116ALP-12	2K × 8	120	60	3	5	2	2	24Pin PDIP
	HY6116ALP-15	2K × 8	150	60	3	5	2	2	24Pin PDIP
64K bit	HY6264P-70	8K × 8	70	70	3	2000	NA	NA	28Pin PDIP
	HY6264P-85	8K × 8	85	70	3	2000	NA	NA	28Pin PDIP
	HY6264P-10	8K × 8	100	70	3	2000	NA	NA	28Pin PDIP
	HY6264P-12	8K × 8	120	70	3	2000	NA	NA	28Pin PDIP
	HY6264P-15	8K × 8	150	70	3	2000	NA	NA	28Pin PDIP
	HY6264J-70	8K × 8	70	70	3	2000	NA	NA	28Pin SOP
	HY6264J-85	8K × 8	85	70	3	2000	NA	NA	28Pin SOP
	HY6264J-10	8K × 8	100	70	3	2000	NA	NA	28Pin SOP
	HY6264J-12	8K × 8	120	70	3	2000	NA	NA	28Pin SOP
	HY6264J-15	8K × 8	150	70	3	2000	NA	NA	28Pin SOP
	HY6264LP-70	8K × 8	70	70	3	100	2	50	28Pin PDIP
	HY6264LP-85	8K × 8	85	70	3	100	2	50	28Pin PDIP
	HY6264LP-10	8K × 8	100	70	3	100	2	50	28Pin PDIP
	HY6264LP-12	8K × 8	120	70	3	100	2	50	28Pin PDIP
	HY6264LP-15	8K × 8	150	70	3	100	2	50	28Pin PDIP
	HY6264LJ-70	8K × 8	70	70	3	100	2	50	28Pin SOP
	HY6264LJ-85	8K × 8	85	70	3	100	2	50	28Pin SOP
	HY6264LJ-10	8K × 8	100	70	3	100	2	50	28Pin SOP
	HY6264LJ-12	8K × 8	120	70	3	100	2	50	28Pin SOP
	HY6264LJ-15	8K × 8	150	70	3	100	2	50	28Pin SOP
	HY6264AP-70	8K × 8	70	50	2	1000	NA	NA	28Pin PDIP
	HY6264AP-85	8K × 8	85	50	2	1000	NA	NA	28Pin PDIP
	HY6264AP-10	8K × 8	100	50	2	1000	NA	NA	28Pin PDIP
	HY6264AP-12	8K × 8	120	50	2	1000	NA	NA	28Pin PDIP
	HY6264AP-15	8K × 8	150	50	2	1000	NA	NA	28Pin PDIP
	HY6264AJ-70	8K × 8	70	50	2	1000	NA	NA	28Pin SOP
	HY6264AJ-85	8K × 8	85	50	2	1000	NA	NA	28Pin SOP
	HY6264AJ-10	8K × 8	100	50	2	1000	NA	NA	28Pin SOP
	HY6264AJ-12	8K × 8	120	50	2	1000	NA	NA	28Pin SOP
	HY6264AJ-15	8K × 8	150	50	2	1000	NA	NA	28Pin SOP

SRAM(continued)

DENSITY	PART NO	ORGANIZATION	t_{AA} ns	I_{CC1} mA	I_{SB} mA	I_{SB1} μA	V_{DR} V	I_{CCDR} μA	PACKAGE
64K bit	HY6264ALP-70	8K × 8	70	50	2	100	2	50	28Pin PDIP
	HY6264ALP-85	8K × 8	85	50	2	100	2	50	28Pin PDIP
	HY6264ALP-10	8K × 8	100	50	2	100	2	50	28Pin PDIP
	HY6264ALP-12	8K × 8	120	50	2	100	2	50	28Pin PDIP
	HY6264ALP-15	8K × 8	150	50	2	100	2	50	28Pin PDIP
	HY6264ALJ-70	8K × 8	70	50	2	100	2	50	28Pin SOP
	HY6264ALJ-85	8K × 8	85	50	2	100	2	50	28Pin SOP
	HY6264ALJ-10	8K × 8	100	50	2	100	2	50	28Pin SOP
	HY6264ALJ-12	8K × 8	120	50	2	100	2	50	28Pin SOP
	HY6264ALJ-15	8K × 8	150	50	2	100	2	50	28Pin SOP
	HY6264ALLP-70	8K × 8	70	50	2	50	2	5	28Pin PDIP
	HY6264ALLP-85	8K × 8	85	50	2	50	2	5	28Pin PDIP
	HY6264ALLP-10	8K × 8	100	50	2	50	2	5	28Pin PDIP
	HY6264ALLP-12	8K × 8	120	50	2	50	2	5	28Pin PDIP
	HY6264ALLP-15	8K × 8	150	50	2	50	2	5	28Pin PDIP
	HY6264ALLJ-70	8K × 8	70	50	2	50	2	5	28Pin SOP
	HY6264ALLJ-85	8K × 8	85	50	2	50	2	5	28Pin SOP
	HY6264ALLJ-10	8K × 8	100	50	2	50	2	5	28Pin SOP
	HY6264ALLJ-12	8K × 8	120	50	2	50	2	5	28Pin SOP
	HY6264ALLJ-15	8K × 8	150	50	2	50	2	5	28Pin SOP
256K bit	HY62C256P-85	32K × 8	85	70	3	1000	NA	NA	28Pin PDIP
	HY62C256P-10	32K × 8	100	70	3	1000	NA	NA	28Pin PDIP
	HY62C256P-12	32K × 8	120	70	3	1000	NA	NA	28Pin PDIP
	HY62C256P-15	32K × 8	150	70	3	1000	NA	NA	28Pin PDIP
	HY62C256J-85	32K × 8	85	70	3	1000	NA	NA	28Pin SOP
	HY62C256J-10	32K × 8	100	70	3	1000	NA	NA	28Pin SOP
	HY62C256J-12	32K × 8	120	70	3	1000	NA	NA	28Pin SOP
	HY62C256J-15	32K × 8	150	70	3	1000	NA	NA	28Pin SOP
	HY62C256LP-85	32K × 8	85	70	3	100	2	50	28Pin PDIP
	HY62C256LP-10	32K × 8	100	70	3	100	2	50	28Pin PDIP
	HY62C256LP-12	32K × 8	120	70	3	100	2	50	28Pin PDIP
	HY62C256LP-15	32K × 8	150	70	3	100	2	50	28Pin PDIP
	HY62C256LJ-85	32K × 8	85	70	3	100	2	50	28Pin SOP
	HY62C256LJ-10	32K × 8	100	70	3	100	2	50	28Pin SOP
	HY62C256LJ-12	32K × 8	120	70	3	100	2	50	28Pin SOP
	HY62C256LJ-15	32K × 8	150	70	3	100	2	50	28Pin SOP
	HY62256AP-70	32K × 8	70	70	2	1000	NA	NA	28Pin PDIP
	HY62256AP-85	32K × 8	85	70	2	1000	NA	NA	28Pin PDIP
	HY62256AP-10	32K × 8	100	70	2	1000	NA	NA	28Pin PDIP
	HY62256AP-12	32K × 8	120	70	2	1000	NA	NA	28Pin PDIP

SRAM(continued)

DENSITY	PART NO	ORGANIZATION	t_{AA} ns	I_{CC1} mA	I_{SB} mA	I_{SB1} μA	V_{DR} V	I_{CCDR} μA	PACKAGE
256K bit	HY62256AJ-70	32K × 8	70	70	2	1000	NA	NA	28Pin SOP
	HY62256AJ-85	32K × 8	85	70	2	1000	NA	NA	28Pin SOP
	HY62256AJ-10	32K × 8	100	70	2	1000	NA	NA	28Pin SOP
	HY62256AJ-12	32K × 8	120	70	2	1000	NA	NA	28Pin SOP
	HY62256ALP-70	32K × 8	70	70	2	100	2	50	28Pin PDIP
	HY62256ALP-85	32K × 8	85	70	2	100	2	50	28Pin PDIP
	HY62256ALP-10	32K × 8	100	70	2	100	2	50	28Pin PDIP
	HY62256ALP-12	32K × 8	120	70	2	100	2	50	28Pin PDIP
	HY62256ALJ-70	32K × 8	70	70	2	100	2	50	28Pin SOP
	HY62256ALJ-85	32K × 8	85	70	2	100	2	50	28Pin SOP
	HY62256ALJ-10	32K × 8	100	70	2	100	2	50	28Pin SOP
	HY62256ALJ-12	32K × 8	120	70	2	100	2	50	28Pin SOP
	HY62256ALLP-70	32K × 8	70	70	2	50	2	20	28Pin PDIP
	HY62256ALLP-85	32K × 8	85	70	2	50	2	20	28Pin PDIP
	HY62256ALLP-10	32K × 8	100	70	2	50	2	20	28Pin PDIP
	HY62256ALLP-12	32K × 8	120	70	2	50	2	20	28Pin PDIP
	HY62256ALLJ-70	32K × 8	70	70	2	50	2	20	28Pin SOP
	HY62256ALLJ-85	32K × 8	85	70	2	50	2	20	28Pin SOP
	HY62256ALLJ-10	32K × 8	100	70	2	50	2	20	28Pin SOP
	HY62256ALLJ-12	32K × 8	120	70	2	50	2	20	28Pin SOP
1M bit	* HY628100P-70	128K × 8	70	70	3	2000	NA	NA	32Pin PDIP
	* HY628100P-85	128K × 8	85	70	3	2000	NA	NA	32Pin PDIP
	* HY628100P-10	128K × 8	100	70	3	2000	NA	NA	32Pin PDIP
	* HY628100P-12	128K × 8	120	70	3	2000	NA	NA	32Pin PDIP
	HY628100J-70	128K × 8	70	70	3	2000	NA	NA	32Pin SOP
	HY628100J-85	128K × 8	85	70	3	2000	NA	NA	32Pin SOP
	HY628100J-10	128K × 8	100	70	3	2000	NA	NA	32Pin SOP
	HY628100J-12	128K × 8	120	70	3	2000	NA	NA	32Pin SOP
	* HY628100LP-70	128K × 8	70	70	3	100	2	50	32Pin PDIP
	* HY628100LP-85	128K × 8	85	70	3	100	2	50	32Pin PDIP
	* HY628100LP-10	128K × 8	100	70	3	100	2	50	32Pin PDIP
	* HY628100LP-12	128K × 8	120	70	3	100	2	50	32Pin PDIP
	HY628100LJ-70	128K × 8	70	70	3	100	2	50	32Pin SOP
	HY628100LJ-85	128K × 8	85	70	3	100	2	50	32Pin SOP
	HY628100LJ-10	128K × 8	100	70	3	100	2	50	32Pin SOP
	HY628100LJ-12	128K × 8	120	70	3	100	2	50	32Pin SOP
	* HY628100LLP-70	128K × 8	70	70	3	50	2	30	32Pin PDIP
	* HY628100LLP-85	128K × 8	85	70	3	50	2	30	32Pin PDIP
	* HY628100LLP-10	128K × 8	100	70	3	50	2	30	32Pin PDIP
	* HY628100LLP-12	128K × 8	120	70	3	50	2	30	32Pin PDIP
	HY628100LLJ-70	128K × 8	70	70	3	50	2	30	32Pin SOP
	HY628100LLJ-85	128K × 8	85	70	3	50	2	30	32Pin SOP
	HY628100LLJ-10	128K × 8	100	70	3	50	2	30	32Pin SOP
	HY628100LLJ-12	128K × 8	120	70	3	50	2	30	32Pin SOP

REMARK : (*) available from the lst Quarter 1993.

4. MASK ROM

DENSITY	PART NO	ORGANIZATION	t_{AA} ns	I_{CC} mA	I_{SB1} mA	I_{SB2} μA	PACKAGE
4M bit	HY234000P-15	512K × 8	150	15	2	100	32Pin PDIP
	HY234000P-20	512K × 8	200	15	2	100	32Pin PDIP
	HY234000P-25	512K × 8	250	15	2	100	32Pin PDIP
	HY234000J-15	512K × 8	150	15	2	100	32Pin SOP
	HY234000J-20	512K × 8	200	15	2	100	32Pin SOP
	HY234000J-25	512K × 8	250	15	2	100	32Pin SOP
	HY234001P-15	512K × 8	150	15	NA	NA	32Pin PDIP
	HY234001P-20	512K × 8	200	15	NA	NA	32Pin PDIP
	HY234001P-25	512K × 8	250	15	NA	NA	32Pin PDIP
	HY234001J-15	512K × 8	150	15	NA	NA	32Pin SOP
	HY234001J-20	512K × 8	200	15	NA	NA	32Pin SOP
	HY234001J-25	512K × 8	250	15	NA	NA	32Pin SOP
	HY234100P-15	512K × 8/256K × 16	150	20	2	100	40Pin PDIP
	HY234100P-20	512K × 8/256K × 16	200	20	2	100	40Pin PDIP
	HY234100P-25	512K × 8/256K × 16	250	20	2	100	40Pin PDIP

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5. EEPROM

DENSITY	PART NO	OPERATING TEMPERATURE RANGE	ACCESS MODE	Icc mA	CLOCK FREQ. KHz	Vpp V	RETEN-TION TIME	ERASE/ WRITE CYCLE	PACKAGE
1K bit	HY93C46S	0 to 70℃	serial	3	250	5	10 year	10,000	8Pin PDIP
	HY93C46J	0 to 70℃	serial	3	250	5	10 year	10,000	8Pin SOP
	HY93C46ES	−40 to 85℃	serial	3	250	5	10 year	10,000	8Pin PDIP
	HY93C46EJ	−40 to 85℃	serial	3	250	5	10 year	10,000	8Pin SOP

6. EEPLD

DENSITY	INPUT	I/O	MACRO CELL	PROGRA-MMABLE ARRAY	PRODUCT TERM X INPUT ARRAY	I_{CCAT} mA @10MHz	I_{CCAC} mA @10MHz	PACKAGE
HY18CV8S-25	10	8	8	AND	74 × 36	32	27	20 Pin PDIP
HY18CV8S-30	10	8	8	AND	74 × 36	32	27	20 Pin PDIP
HY18CV8S-35	10	8	8	AND	74 × 36	32	27	20 Pin PDIP

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HYUNDAI SEMICONDUCTOR

HY53C256

256K×1-Bit CMOS DRAM

M111201B-JAN92

DESCRIPTION

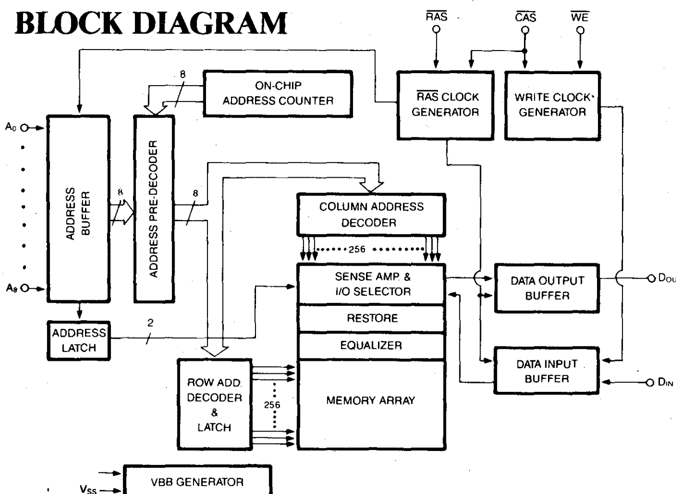
The HY53C256 is a high speed 262,144×1 bit CMOS dynamic random access memory. Fabricated with HYUNDAI CMOS technology, the HY53C256 offers a fast page mode for high data bandwidth, fast usable speed, CMOS standby current and, for the HY53C256L, reduced CMOS standby mode supply current (I_{DD5}).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance.

Fast page mode operation allows random or sequential access of up to 512 bits within a row with cycle times as fast as 50 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the HY53C256 design is optimized suited for cache based mainframe and minicomputers, graphics, digital signal processing and high performance microprocessor systems.

The HY53C256L offers a maximum data retention power of 5 mW when operating in CMOS standby mode and performs $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. This mode is entered by holding $\overline{RAS}$ at a voltage greater than V_{DD}-0.2 when it is inactive.

BLOCK DIAGRAM

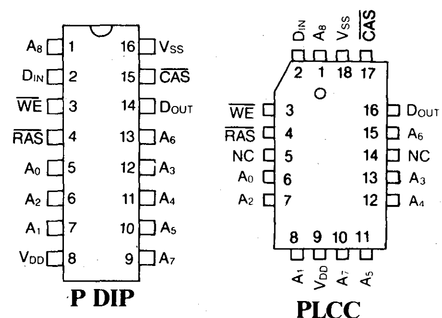


FEATURES

- Low power dissipation for HY53C256L
  - Operating Current, 100ns : 50mA (max.)
  - TTL Standby Current : 2mA (max.)
  - CMOS Standby Current : 1mA (max.)
- Read-Modify-Write Capability
- $\overline{RAS}$-only, Hidden, $\overline{CAS}$-before-$\overline{RAS}$ Refresh Capability
- Common I/O capability
- Fast Page Mode operation for a sustained data rate up to 20 MHz
- 256 Refresh cycles/4 ms
- High reliability 16 pin 300 mil P-DIP and 18 pin PLCC
- Fast access time and cycle time (ns)

	HY53C256-70	HY53C256-80	HY53C256-10	HY53C256-12
Max $\overline{RAS}$ Access Time, t_{RAC}	70	80	100	120
Max $\overline{CAS}$ Access Time, t_{CAC}	15	20	25	30
Min Fast Page Mode Cycle Time, t_{PC}	50	55	60	70
Min Cycle Time, t_{RC}	130	145	175	205

PIN CONNECTIONS



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0—A_8	ADDRESS INPUT
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

3

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature Under Bias	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 125	℃
V_{TERM}	Voltage on Any Pin Except V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Data Out Current	50	mA
P_T	Power Dissipation	1.0	W

NOTE :
1. Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC CHARACTERISTICS

(T_A=0℃ to 70℃, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY53C256		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		—	10	µA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		—	10	µA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−70	—	70	mA	1,2
			−80	—	60		
			−10	—	50		
			−12	—	45		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH}, other inputs $\geq V_{SS}$	HY53C256	—	3	mA	
			HY53C256L	—	2		
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−70	—	70	mA	2
			−80	—	60		
			−10	—	50		
			−12	—	45		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−70	—	45	mA	1,2
			−80	—	40		
			−10	—	35		
			−12	—	30		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}$-0.2V, $\overline{CAS}$= V_{IH}, other inputs $\geq V_{SS}$	HY53C256	—	2	mA	
			HY53C256L	—	1		
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min)	−70	—	70	mA	2
			−80	—	60		
			−10	—	50		
			−12	—	45		
V_{IL}	Input Low Voltage(all inputs)			−1	0.8	V	
V_{IH}	Input High Voltage(all inputs)			2.4	V_{DD}+1	V	
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		—	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	—	V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD}(max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY53C256-70		HY53C256-80		HY53C256-10		HY53C256-12		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	70	75K	80	75K	100	75K	120	75K	ns	
2	t_{RC}	Read or Write Cycle Time	130	—	145	—	175	—	205	—	ns	
3	t_{RP}	$\overline{\text{RAS}}$ Precharge Time	50	—	55	—	65	—	75	—	ns	
4	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	0	—	ns	
5	t_{RAH}	Row Address Hold Time	15	—	15	—	15	—	20	—	ns	
6	t_{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	35	—	40	—	45	—	55	—	ns	
7	t_{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	20	35	20	40	20	55	25	65	ns	1
8	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	ns	
9	t_{CAH}	Column Address Hold Time	15	—	15	—	20	—	25	—	ns	
10	t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	25	55	25	60	25	75	30	90	ns	2
11	t_{RAC}	Access Time from $\overline{\text{RAS}}$	—	70	—	80	—	100	—	120	ns	3,4,5
12	t_{AA}	Access Time from Column Address	—	35	—	40	—	45	—	55	ns	5,6,12
13	t_{CAC}	Access Time from $\overline{\text{CAS}}$	—	15	—	20	—	25	—	30	ns	5,12
14	$t_{CAS(R)}$	$\overline{\text{CAS}}$ Pulse Width in Read Cycle	15	75K	20	75K	25	75K	30	75K	ns	
15	$t_{RSH(R)}$	$\overline{\text{RAS}}$ Hold Time in Read Cycel	15	—	20	—	25	—	30	—	ns	
16	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	0	—	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	5	—	5	—	5	—	5	—	ns	7
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	5	—	5	—	5	—	5	—	ns	7
19	t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	15	—	15	—	15	—	20	—	ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	15	0	20	0	25	0	30	ns	8
21	t_{OH}	Data Hold Time From $\overline{\text{CAS}}$	0	—	0	—	0	—	0	—	ns	8
22	t_{WP}	Write Pulse Width	15	—	15	—	20	—	25	—	ns	
23	t_{CP}	$\overline{\text{CAS}}$ Precharge Time	15	—	15	—	20	—	25	—	ns	
24	t_{AR}	Column Address Hold Time From $\overline{\text{RAS}}$	55	—	60	—	70	—	80	—	ns	
25	$t_{CAS(W)}$	$\overline{\text{CAS}}$ Pulse Width in Write Cycle	20	—	25	—	30	—	35	—	ns	
26	$t_{RSH(W)}$	$\overline{\text{RAS}}$ Hold Time in Write Cycle	25	—	25	—	30	—	35	—	ns	
27	t_{WCR}	Write Command Hold Time from $\overline{\text{RAS}}$	55	—	60	—	70	—	80	—	ns	
28	t_{WCS}	Write Command Setup Time	0	—	0	—	0	—	0	—	ns	9,10
29	t_{WCH}	Write Command Hold Time	15	—	15	—	20	—	25	—	ns	
30	t_{DS}	Data In Setup Time	0	—	0	—	0	—	0	—	ns	11
31	t_{DH}	Data In Hold Time	15	—	15	—	20	—	25	—	ns	11
32	t_{DHR}	Data In Hold Time Referenced to $\overline{\text{RAS}}$	55	—	60	—	70	—	80	—	ns	
33	t_{RWC}	Read-Modify-Write Cycle Time	155	—	175	—	210	—	245	—	ns	
34	t_{RRW}	Read-Modify-Write Cycle, $\overline{\text{RAS}}$ Pulse Width	95	—	110	—	135	—	160	—	ns	
35	t_{RWD}	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay in RMW Cycle	70	—	80	—	100	—	120	—	ns	9
36	t_{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	15	—	20	—	25	—	30	—	ns	9
37	t_{AWD}	Column Address to $\overline{\text{WE}}$ Delay	35	—	40	—	45	—	55	—	ns	9
38	t_{CAP}	Access Time from Column Precharge	—	45	—	50	—	55	—	65	ns	12

#	SYMBOL	PARAMETER	HY53C256-70		HY53C256-80		HY53C256-10		HY53C256-12		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
39	t_{PC}	Fast Page Mode Read or Write Cycle Time	50	—	55	—	60	—	70	—	ns	
40	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	75	—	85	—	95	—	110	—	ns	
41	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	30	—	35	—	ns	
42	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	25	—	30	—	35	—	ns	
43	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	—	0	—	0	—	0	—	ns	
44	t_{CSR}	$\overline{CAS}$ Setup Time, $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10	—	10	—	10	—	10	—	ns	
45	t_{CHR}	$\overline{CAS}$ Hold Time, $\overline{CAS}$-before-$\overline{RAS}$ Refresh	20	—	25	—	30	—	40	—	ns	
46	t_{CSH}	$\overline{CAS}$ Hold Time	70	—	80	—	100	—	120	—	ns	
47	t_T	Transition Time(Rise and Fall)	3	25	3	25	3	25	3	25	ns	13
48	t_{RI}	Refresh Interval(256 Cycles)	—	4	—	4	—	4	—	4	ms	14

NOTES :

1. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, the access time is controlled by t_{AA} and t_{CAC}.
2. t_{RCD}(max.) is specified for reference only. Operation within t_{RCD}(max.) limits insures that t_{RAC}(max.) and t_{AA}(max.) can be met. If t_{RCD} is greater than the specified t_{RCD}(max.), the access time is controlled by t_{AA} and t_{CAC}.
3. Assumes that $t_{RAD} \leq t_{RAD}$(max.). If t_{RAD} is greater than t_{RAD}(max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.).
4. Assumes that $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.).
5. Measured with a load equivalent to two TTL inputs and 100 pF in parallel.
6. Assumes that $t_{RAD} \geq t_{RAD}$(max.).
7. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
8. t_{OFF} and t_{ON} define the time at which D_{OUT} reaches an open circuit condition and are not referenced to the output voltage levels.
9. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
10. t_{WCS}(min.) must be satisfied in an Early Write Cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
12. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CAP}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max.). AC measurements assume t_T=5 ns.
14. An initial 200μs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

CAPACITANCE[1]

(T_A=25℃, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

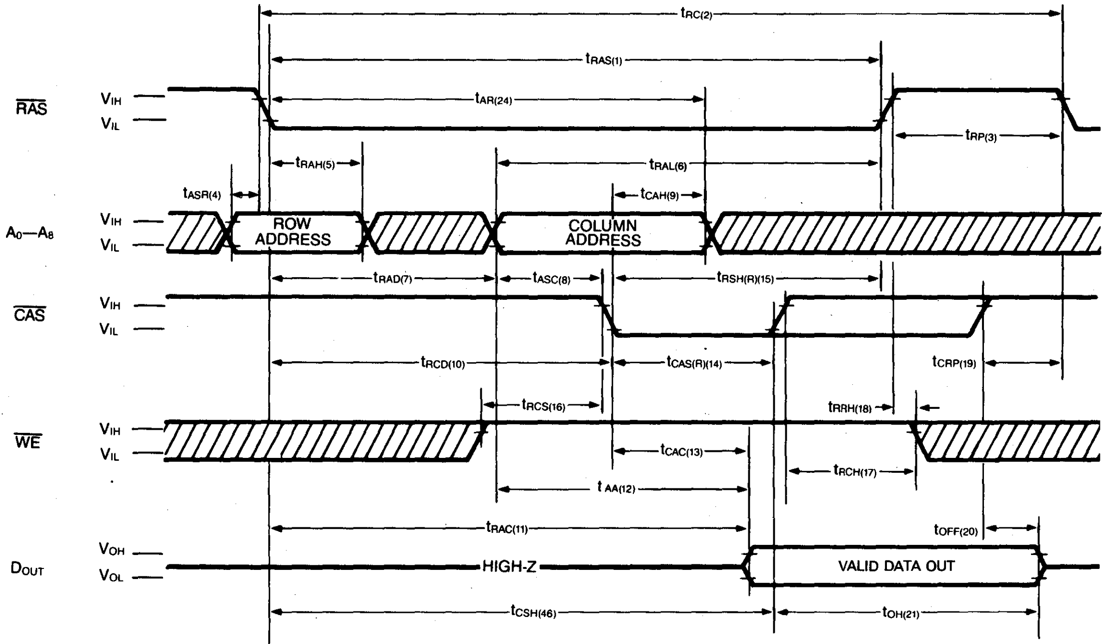
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, D_{IN}	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	—	8	pF
C_{OUT}	D_{OUT}	—	8	pF

NOTE :

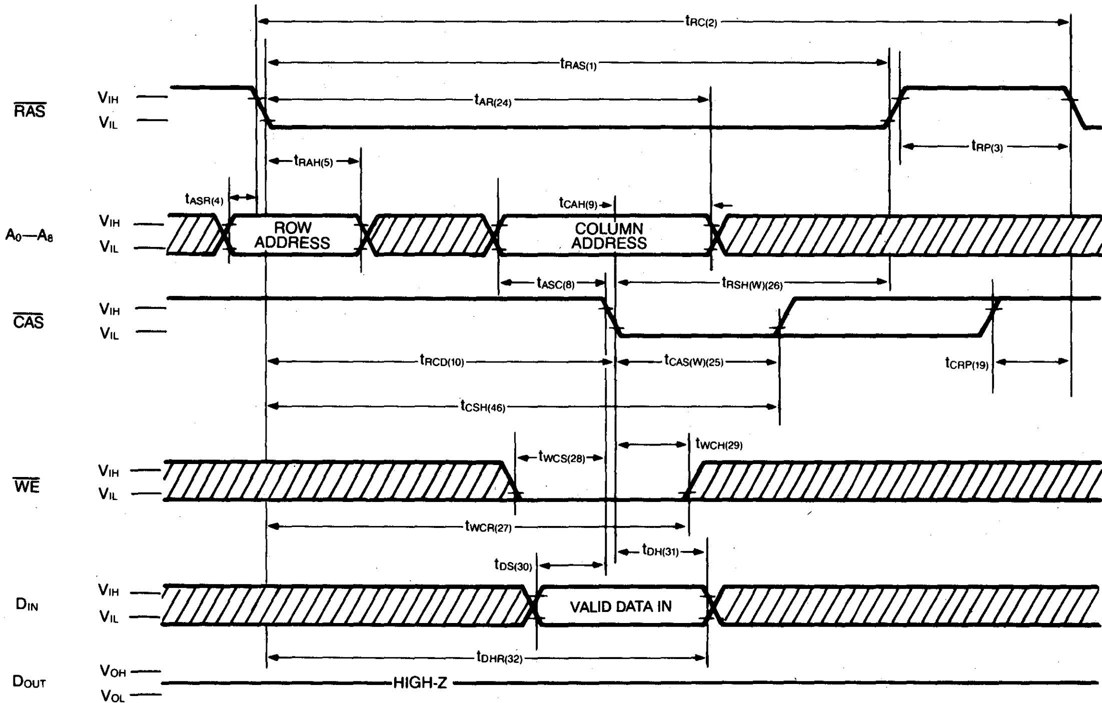
1. Capacitance is measured at the worst case of voltage levels with a programmable capacitance meter.

TIMING DIAGRAMS

READ CYCLE

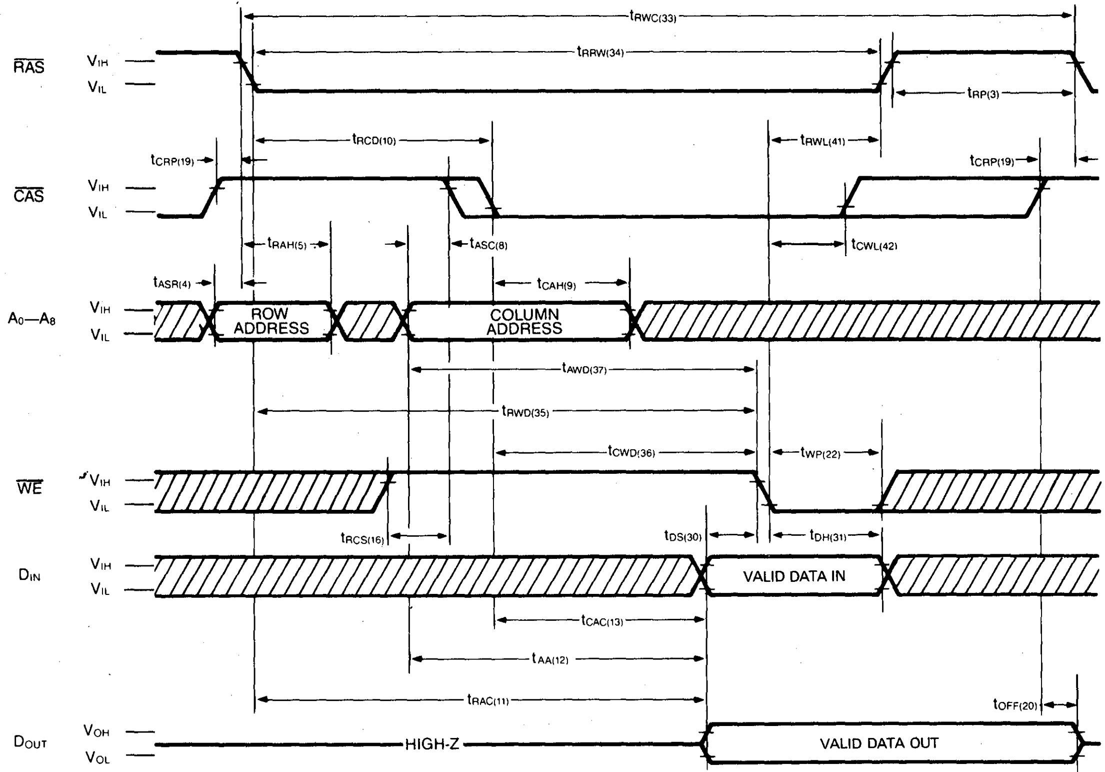


EARLY WRITE CYCLE

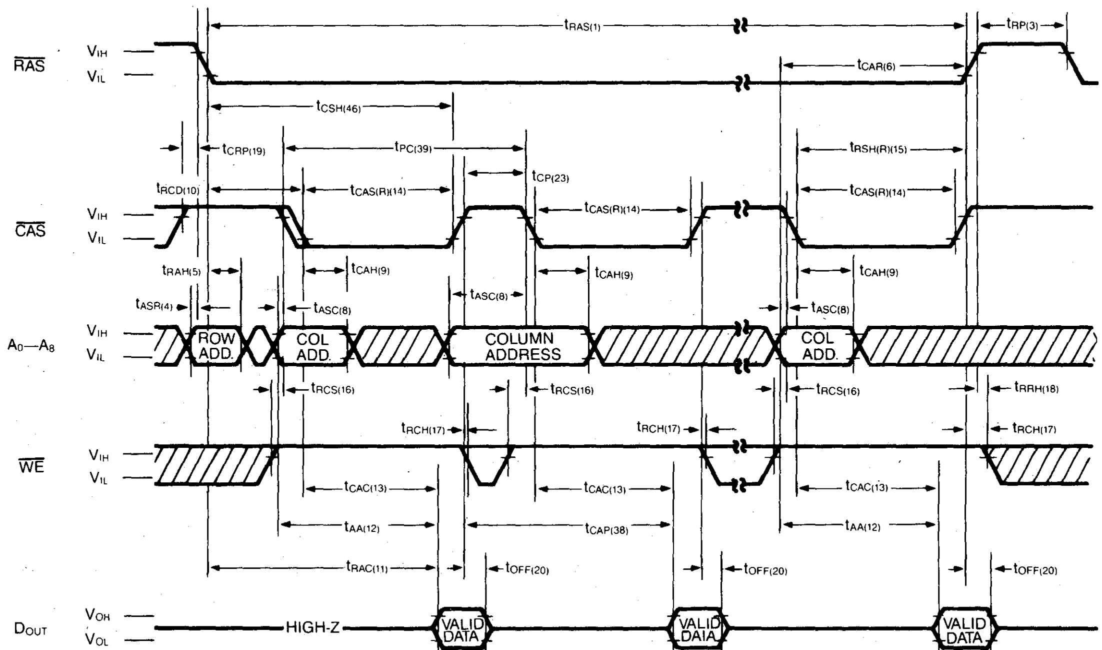


3

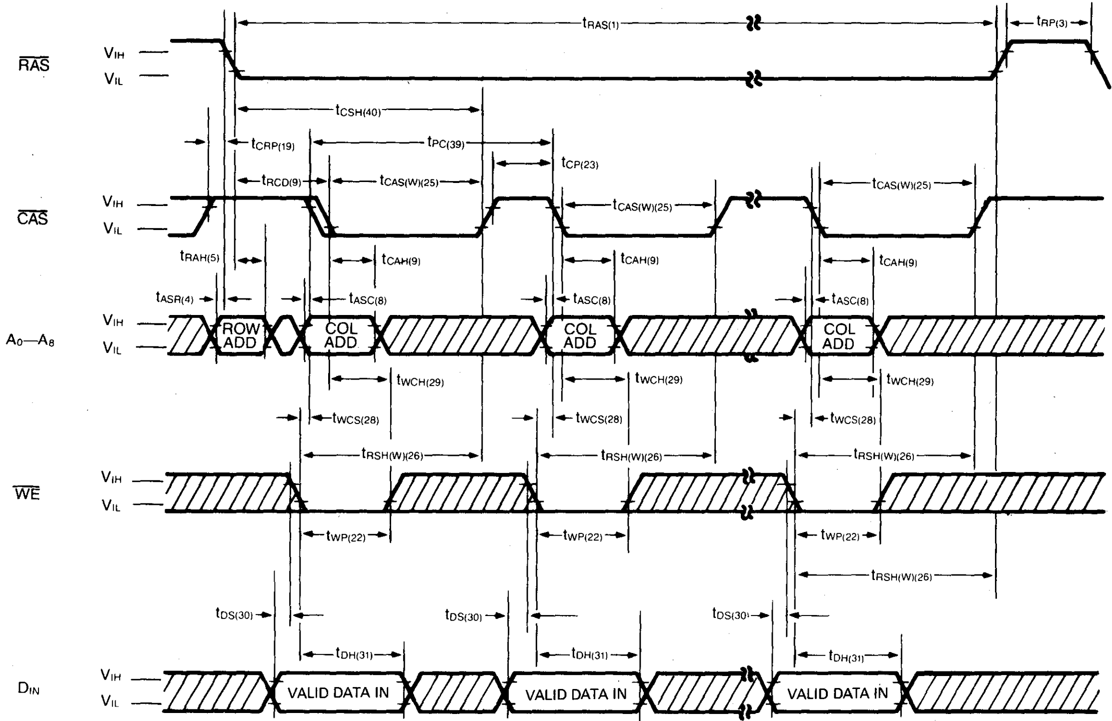
READ-MODIFY-WRITE CYCLE



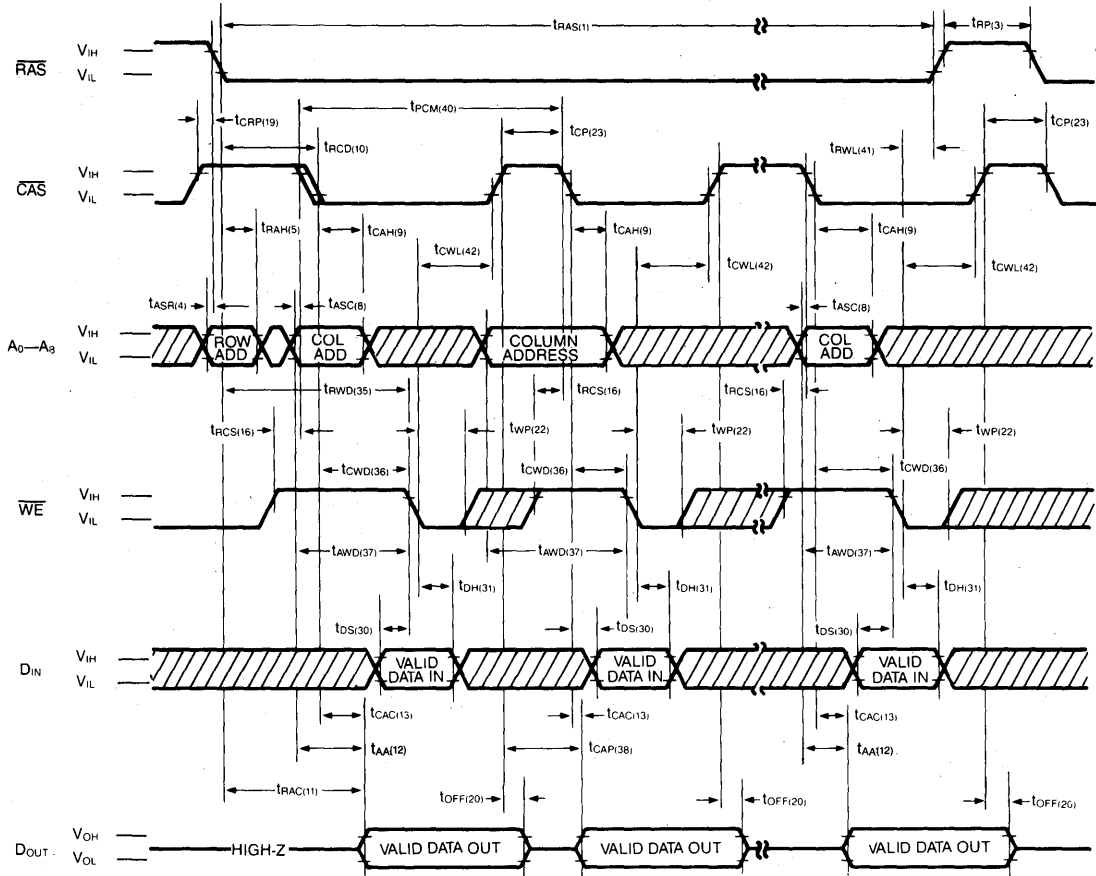
FAST PAGE MODE READ CYCLE



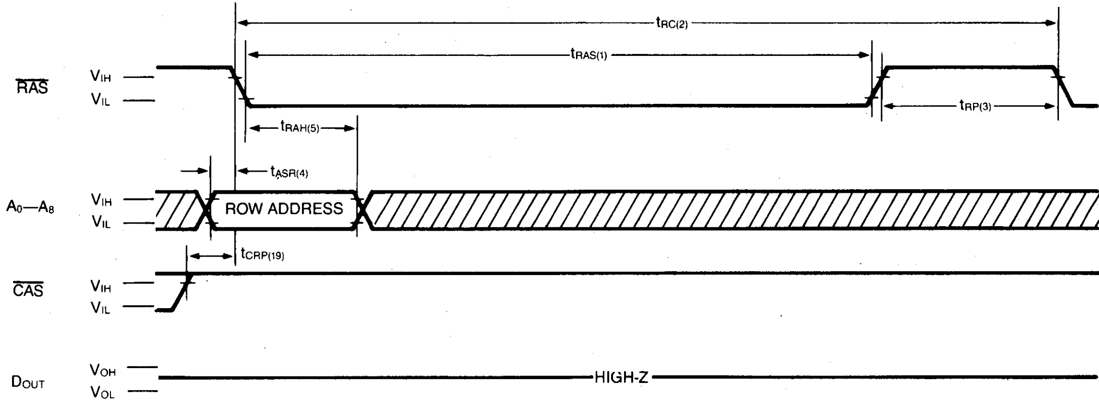
FAST PAGE MODE WRITE CYCLE



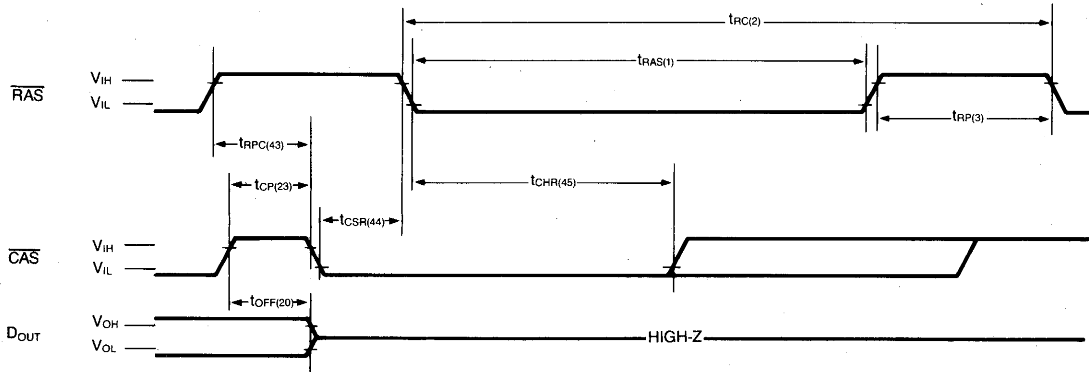
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



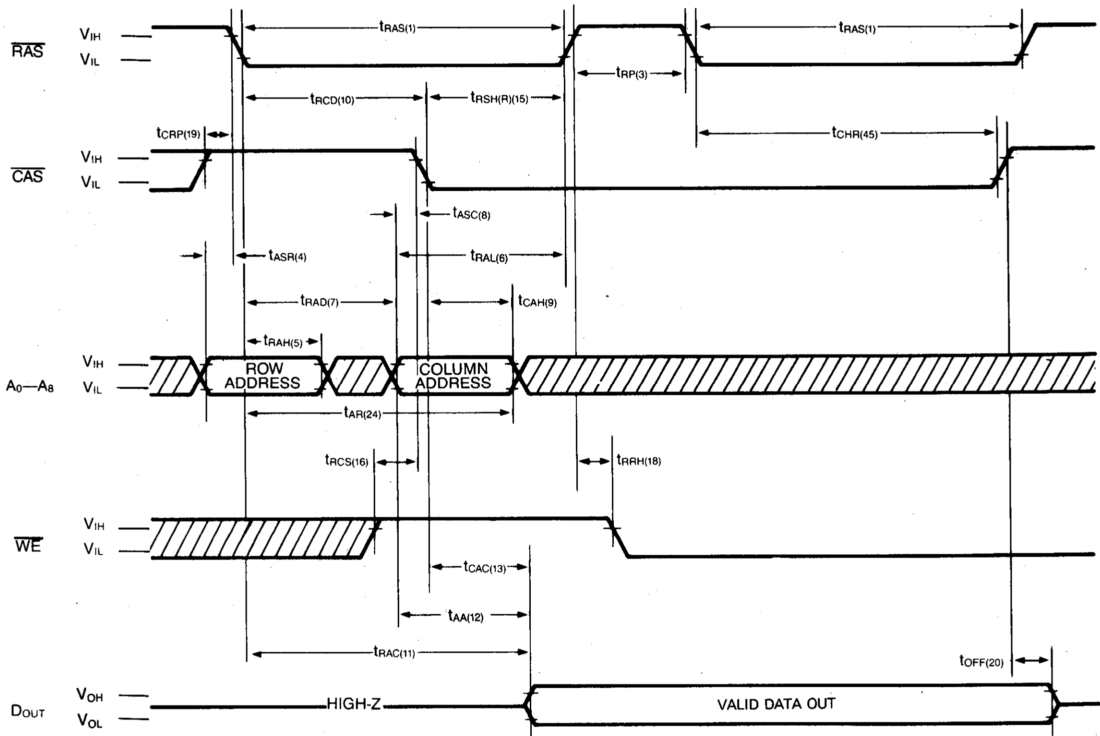
$\overline{RAS}$-ONLY REFRESH CYCLE



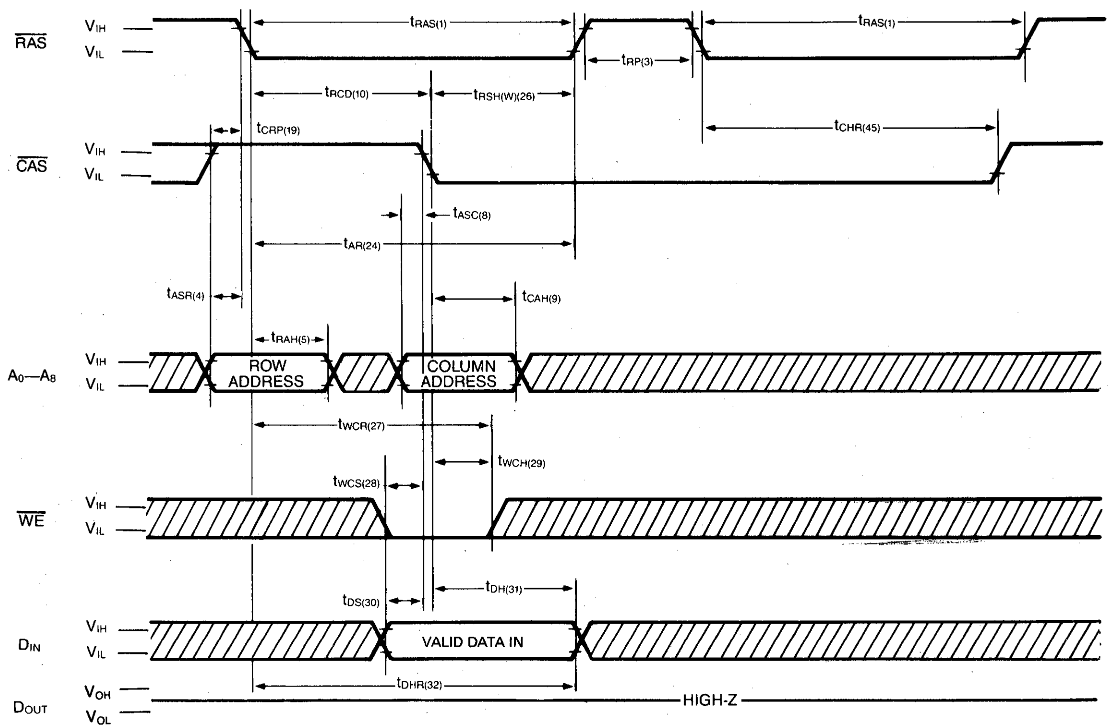
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



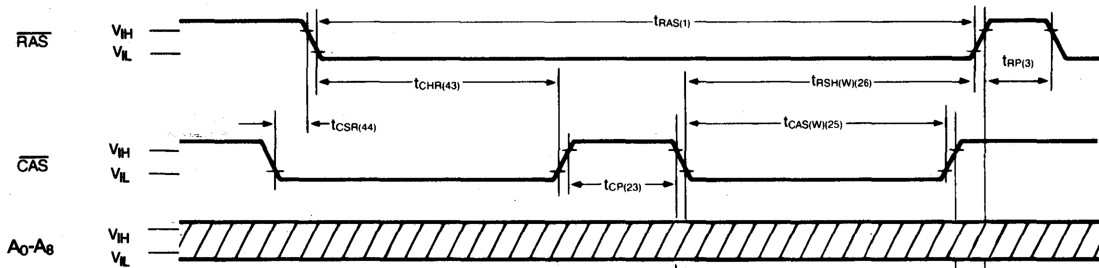
HIDDEN REFRESH CYCLE (READ)



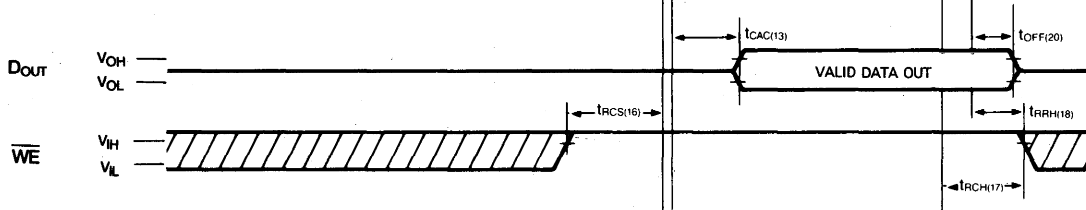
HIDDEN REFRESH CYCLE (WRITE)



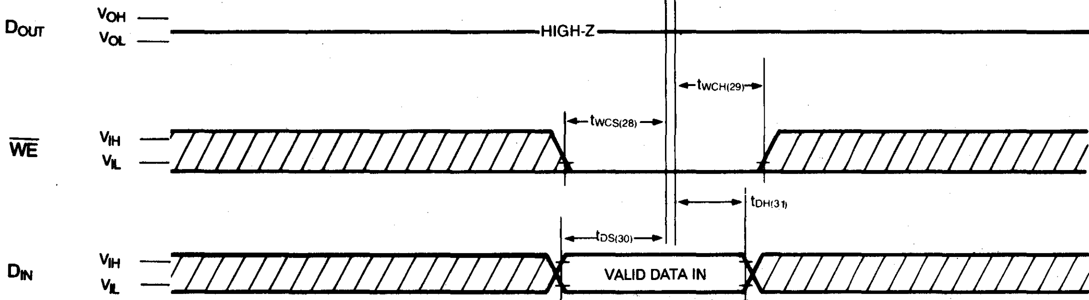
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



READ CYCLE



WRITE CYCLE



FUNCTIONAL DESCRIPTION

The HY53C256 is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The HY53C256 reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe($\overline{RAS}$). The column address flows through an internal address buffer and is latched by the Column Address Strobe($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

MEMORY CYCLE

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data out becomes valid only when t_{RAC}, t_{AA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between t_{RAC}, t_{AA} and t_{CAC}. For example, the access time is limited by t_{AA} when t_{RAC}(min.) are both satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled write cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the output(D_{OUT}) pin will be in the High-Z state at the beginning of the write function. Ending the write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

REFRESH CYCLE

To retain data, 256 refresh cycles are required in each 4 ms period. There are two ways to refresh the memory :

1. By clocking each of the 256 row addresses(A_0 through A_7) with $\overline{RAS}$ at least every 4 ms. Any read, wrtie, read-modify-write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The HY53C256 will use the output of an internal 8-bit counter as the source of row address and ignore external address inputs.
   $\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, D_{OUT} will remain in the High-Z state during the cycle.

A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter. The user can use the counter test mode to write consecutive data patterns (256 write cycles) and then verify the written data by applying 256 consecutive read cycles.

DATA RETENTION MODE

The HY53C256 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY53C256 power consumption is reduced to the low I_{DD5} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows :

$$I=\frac{(t_{RC})\times(I\ active)+(t_{RX}-t_{RC})\times(I_{DD5})}{t_{RX}}$$

Where t_{RC}=Refresh Cycle Time
t_{RX}=Refresh Interval/256

FAST PAGE MODE OPERATION

Fast page mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high.

Thus, access begins at the occurrence of a valid column address rather than at the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable.

During fast page mode operation, read, write, read-modify-write, or read-write-read cycles are possible at random addresses within a row. Following the initial entry cycle into fast page mode, access is t_{AA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is determined by the $\overline{CAS}$ rising edge(specified by t_{CAP} as shown in figure 1). If the column address is valid after the rising edge of $\overline{CAS}$, the access is timed from the occurrence of the valid address and is specified by t_{AA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast page mode provides a sustained data rate of over 20 MHz for applications that require high data rates like bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate :

$$\text{Data Rate}=\frac{512}{t_{RC}+511\times t_{PC}}$$

DATA OUTPUT OPERATION

The HY53C256 data output pin(D_{OUT}) has a three-state capability and is controlled by $\overline{CAS}$. When $\overline{CAS}$ is high($\geq V_{IH}$), the output is in the High-Z state. Table 1 summarizes the D_{OUT} states possible for various memory cycles.

POWER ON

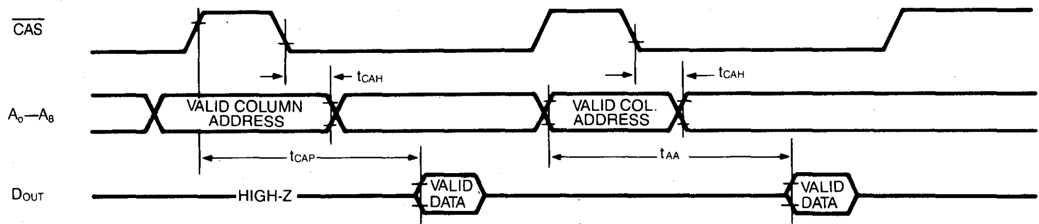
After application of the V_{DD} an initial pause of 200μs is required followed by a minimum of 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

During power on, the V_{DD} current requirement of the HY53C256 is dependant on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during power on, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on to avoid current surges.

TABLE 1. DATA OUTPUT OPERATION FOR VARIOUS CYCLE TYPES

CYCLE TYPE	D_{OUT} STATE
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle(Early Write)	High-Z
$\overline{WE}$-Controlled Wirte Cycle(Late Write)	Active, not valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle(Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh Cycle	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data Remains as in Previous Cycle
$\overline{CAS}$-only Cycle	High-Z

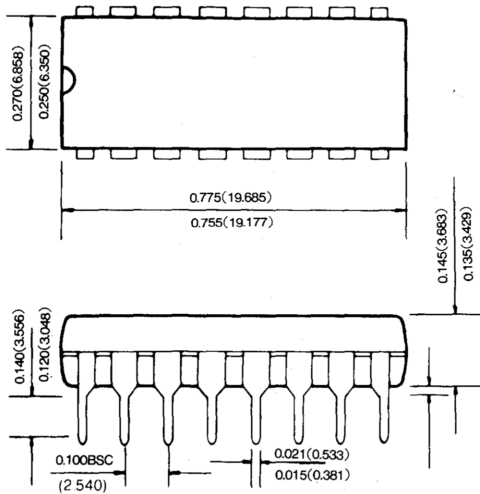
FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION

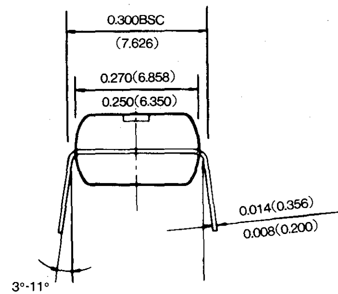


PACKAGE INFORMATION

• 16 PIN PLASTIC DUAL IN LINE PACKAGE−300 MIL

UNIT : INCH(mm) MAX./MIN.

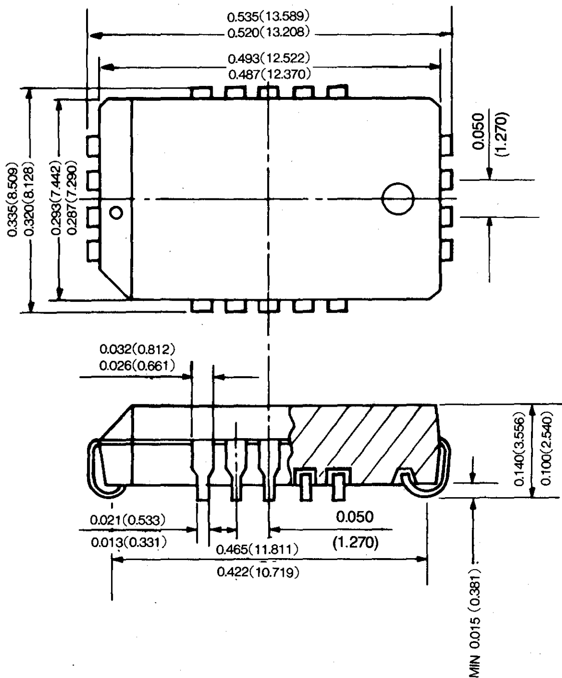


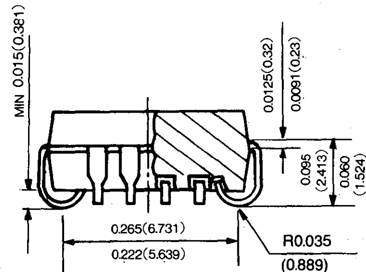


3

• 18 PIN PLASTIC LEADED CHIP CARRIER−330 MIL

UNIT : INCH(mm) MAX./MIN.





MEMO

HYUNDAI SEMICONDUCTOR

HY53C464

64K×4-Bit CMOS DRAM

M121202B-JAN92

DESCRIPTION

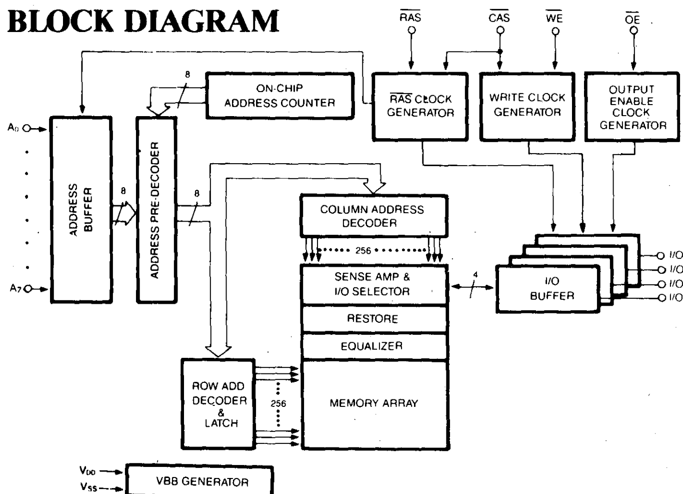
The HY53C464 is a high speed 65,536×4 bit CMOS dynamic random access memory. Fabricated with HYUNDAI CMOS technology, the HY53C464 offers a fast page mode for high data bandwidth, fast usable speed, CMOS standby current and, on request exteened refresh for very low data retention power (HY53C464L).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance.

Fast page mode operation allows random access of up to 256(×4) bits within a row with cycle times as fast as 50 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the HY53C464 design is optimized suited for graphics, digital signal processing and high performance computing system.

The HY53C464L offers a maximum data retention power of 5 mW when operating in CMOS standby mode and performs $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycels. This mode is entered by holding $\overline{RAS}$ at a voltage greater than V_{DD}-0.2 when it is inactive.

BLOCK DIAGRAM

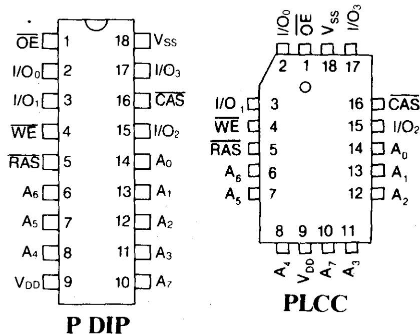


FEATURES

- Low power dissipation for HY53C464L
  - Operating Current, 100ns : 50mA (max.)
  - TTL Standby Current : 2mA (max.)
  - CMOS Standby Current : 1mA (max.)
- Read-Modify-Write Capability
- $\overline{RAS}$-only, Hidden, $\overline{CAS}$-before-$\overline{RAS}$ Refresh Capability
- Fast Page Mode operation for a sustained data rate up to 20 MHz
- 256 Refresh cycles/4 ms
- High reliability 18 pin 300 mil P-DIP and 18 pin PLCC
- Fast access time and cycle time (ns)

	HY53C464-70	HY53C464-80	HY53C464-10	HY53C464-12
Max. $\overline{RAS}$ Access Time, t_{RAC}	70	80	100	120
Max. $\overline{CAS}$ Access Time, t_{CAC}	25	30	35	40
Min. Fast Page Mode Cycle Time, t_{PC}	50	55	65	75
Min. Cycle Time, t_{RC}	130	145	175	205

PIN CONNECTIONS



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
A_0—A_7	ADDRESS INPUT
I/O_0—I/O_3	DATA INPUT OUTPUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature Under Bias	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 125	℃
V_{TERM}	Voltage on Any Pin Except V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Data Out Current	50	mA
P_T	Power Dissipation	1.0	W

NOTE :
1. Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC CHARACTERISTICS

(T_A=0℃ to 70℃, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY53C464		UNIT	NOTE
				MIN.	MAX.		
$\mid I_{LI} \mid$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		—	10	μA	
$\mid I_{LO} \mid$	Output Leakage Current for High Impedance State	$V_{SS} \leq V_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		—	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−70	—	70	mA	1,2
			−80	—	60		
			−10	—	50		
			−12	—	45		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH}, other inputs$\geq V_{SS}$	HY53C464	—	3	mA	
			HY53C464L	—	2		
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−70	—	70	mA	2
			−80	—	60		
			−10	—	50		
			−12	—	45		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−70	—	45	mA	1,2
			−80	—	40		
			−10	—	35		
			−12	—	30		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}$-0.2V, $\overline{CAS}$= V_{IH}, other inputs$\geq V_{SS}$	HY53C464	—	2	mA	
			HY53C464L	—	1		
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min)	−70	—	70	mA	2
			−80	—	60		
			−10	—	50		
			−12	—	45		
V_{IL}	Input Low Voltage(all inputs)			−1	0.8	V	
V_{IH}	Input High Voltage(all inputs)			2.4	V_{DD}+1	V	
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		—	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	—	V	

NOTES :
1. I_{DD} is dependent upon output loading when the device output is selected. Specified I_{DD}(max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY53C464-70		HY53C464-80		HY53C464-10		HY53C464-12		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	70	75K	80	75K	100	75K	120	75K	ns	
2	t_{RC}	Read or Write Cycle Time	130	—	145	—	175	—	205	—	ns	
3	t_{RP}	$\overline{\text{RAS}}$ Precharge Time	50	—	55	—	65	—	75	—	ns	
4	t_{CSH}	$\overline{\text{CAS}}$ Hold Time	70	—	80	—	100	—	120	—	ns	
5	t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	25	—	30	—	35	—	40	—	ns	
6	t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	25	45	25	50	25	65	30	80	ns	1
7	t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	0	—	ns	
8	t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	0	—	ns	
9	t_{RAH}	Row Address Hold Time	15	—	15	—	15	—	20	—	ns	
10	t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	ns	
11	t_{CAH}	Column Address Hold Time	15	—	15	—	20	—	25	—	ns	
12	$t_{RSH(R)}$	$\overline{\text{RAS}}$ Hold Time in Read Cycle	25	—	30	—	35	—	40	—	ns	
13	t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	15	—	15	—	15	—	20	—	ns	
14	t_{RCH}	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	5	—	5	—	5	—	5	—	ns	2
15	t_{RRH}	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	5	—	5	—	5	—	5	—	ns	2
16	t_{ROH}	$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{OE}}$	0	—	0	—	0	—	0	—	ns	
17	t_{OAC}	Access Time from $\overline{\text{OE}}$	—	15	—	20	—	25	—	30	ns	
18	t_{CAC}	Access Time from $\overline{\text{CAS}}$	—	25	—	30	—	35	—	40	ns	3,4
19	t_{RAC}	Access Time from $\overline{\text{RAS}}$	—	70	—	80	—	100	—	120	ns	3,5,6
20	t_{AA}	Access Time from Column Address	—	35	—	40	—	45	—	55	ns	3,4,7
21	t_{LZ}	$\overline{\text{OE}}$ or $\overline{\text{CAS}}$ to Low-Z Output	0	—	0	—	0	—	0	—	ns	13
22	t_{HZ}	$\overline{\text{OE}}$ or $\overline{\text{CAS}}$ to High-Z Output	0	15	0	20	0	25	0	30	ns	13
23	t_{AR}	Column Address Hold Time from $\overline{\text{RAS}}$	55	—	60	—	70	—	80	—	ns	
24	t_{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	20	35	20	40	20	55	25	65	ns	8
25	$t_{RSH(W)}$	$\overline{\text{RAS}}$ Hold Time in Write Cycle	25	—	30	—	35	—	40	—	ns	
26	t_{CWL}	Write Command to $\overline{\text{CAS}}$ Lead Time	25	—	30	—	35	—	40	—	ns	
27	t_{WCS}	Write Command Setup Time	0	—	0	—	0	—	0	—	ns	9,10
28	t_{WCH}	Write Command Hold Time	15	—	15	—	20	—	25	—	ns	
29	t_{WP}	Write Pulse Width	15	—	15	—	20	—	25	—	ns	
30	t_{WCR}	Write Command Hold Time from $\overline{\text{RAS}}$	55	—	60	—	70	—	80	—	ns	11
31	t_{RWL}	Writ Command to $\overline{\text{RAS}}$ Lead Time	25	—	30	—	35	—	40	—	ns	
32	t_{DS}	Data In Setup Time	0	—	0	—	0	—	0	—	ns	11
33	t_{DH}	Data In Hold Time	15	—	15	—	20	—	25	—	ns	11
34	t_{WOH}	Write to $\overline{\text{OE}}$ Hold Time	20	—	20	—	25	—	30	—	ns	11
35	t_{OED}	$\overline{\text{OE}}$ to Data Delay Time	20	—	25	—	30	—	35	—	ns	11
36	t_{RWC}	Read-Modify-Write Cycle Time	195	—	225	—	265	—	305	—	ns	
37	t_{RRW}	Read-Modify-Write Cycle, $\overline{\text{RAS}}$ Pulse Width	125	—	145	—	175	—	205	—	ns	
38	t_{CWD}	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	50	—	60	—	70	—	80	—	ns	9

#	SYMBOL	PARAMETER	HY53C464-70		HY53C464-80		HY53C464-10		HY53C464-12		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
39	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	95	—	110	—	135	—	160	—	ns	9
40	t_{CRW}	$\overline{CAS}$ Pulse Width(RMW)	80	—	95	—	110	—	125	—	ns	
41	t_{AWD}	Column Address to $\overline{WE}$ Delay	60	—	70	—	80	—	85	—	ns	9
42	t_{PC}	Fast Page Mode Read or Write Cycle Time	50	—	55	—	65	—	75	—	ns	
43	t_{CP}	$\overline{CAS}$ Precharge Time	15	—	15	—	20	—	25	—	ns	
44	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	40	—	45	—	55	—	ns	
45	t_{CAP}	Access Time from Column Precharge	—	45	—	50	—	55	—	65	ns	4
46	t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	55	—	60	—	70	—	80	—	ns	
47	t_{CSR}	$\overline{CAS}$ Setup time, $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10	—	10	—	10	—	10	—	ns	
48	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	—	0	—	0	—	0	—	ns	
49	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	20	—	25	—	30	—	40	—	ns	
50	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	105	—	120	—	140	—	165	—	ns	
51	t_T	Transition Time(Rise and Fall)	3	25	3	25	3	25	3	25	ns	12
52	t_{RI}	Refresh Interval(256 Cycles)	—	4	—	4	—	4	—	4	ms	14

NOTES :

1. t_{RCD}(max.) is specified for reference only. Operation within t_{RCD}(max.) limits insures that t_{RAC}(max.) and t_{AA}(max.) can be met. If t_{RCD} is greater than the specified t_{RCD}(max.), the access time is controlled by t_{AA} and t_{CAC}.
2. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle to occur.
3. Measured with a load equivalent to two TTL inputs and 100 pF.
4. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CAP}.
5. Assumes that $t_{RAD} \leq t_{RAD}$(max.). If t_{RAD} is greater than t_{RAD}(max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.).
6. Assumes that $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.).
7. Assumes that $t_{RAD} \geq t_{RAD}$(max.).
8. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, the access time is controlled by t_{AA} and t_{CAC}.
9. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are no restrictive operating parameters.
10. t_{WCS}(min.) must be satisfied in an Early Write Cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
12. t_T is measured between V_{IH}(min.) and V_{IL}(max.). AC-measurements assume t_T=5ns.
13. Assumes a three-state test load(5 pF and a 380 Ohm Thevenin equivalent)
14. An initial 200μs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

CAPACITANCE[1]

(T_A=25℃, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

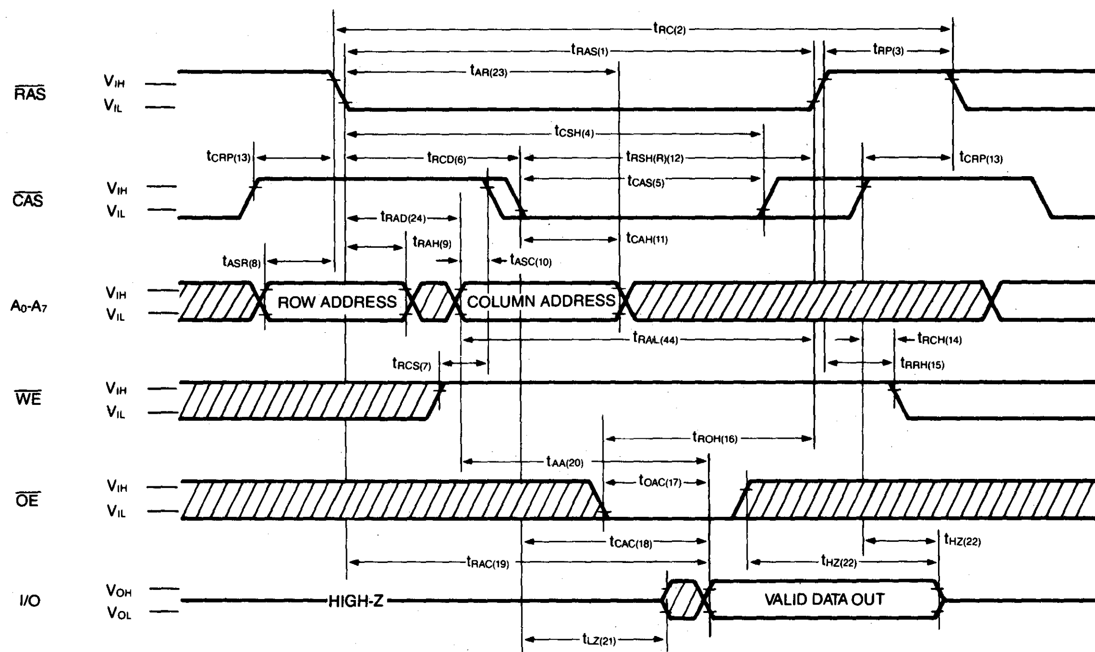
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, D_{IN}	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	—	8	pF
C_{OUT}	D_{OUT}	—	8	pF

NOTES :

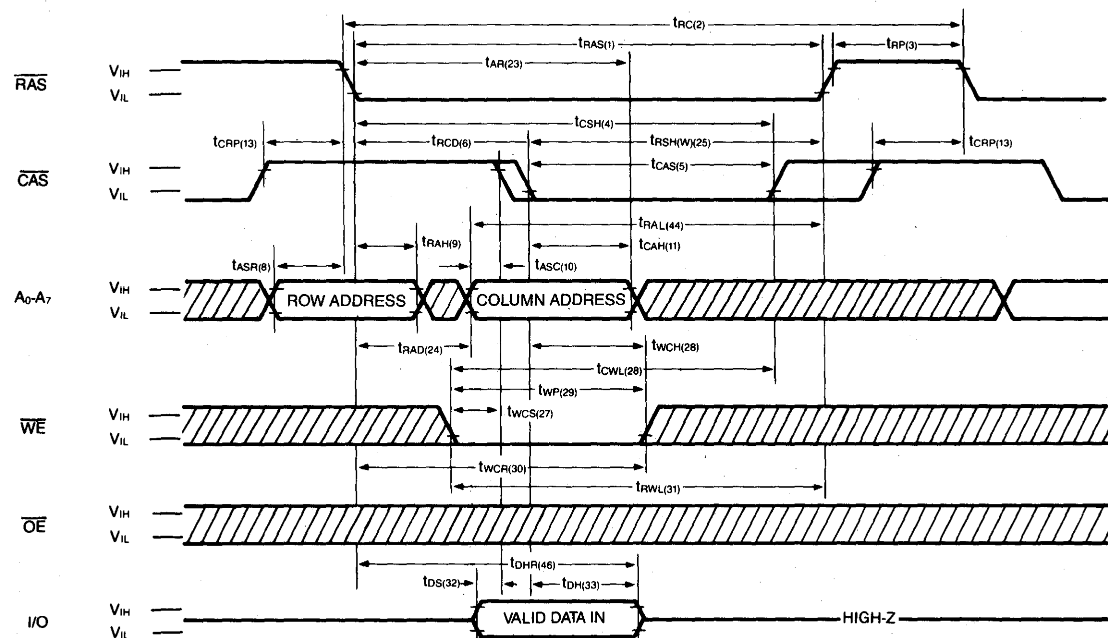
1. Capacitance is measured at the worst case of voltage levels with a programmable capacitance meter.

TIMING DIAGRAMS

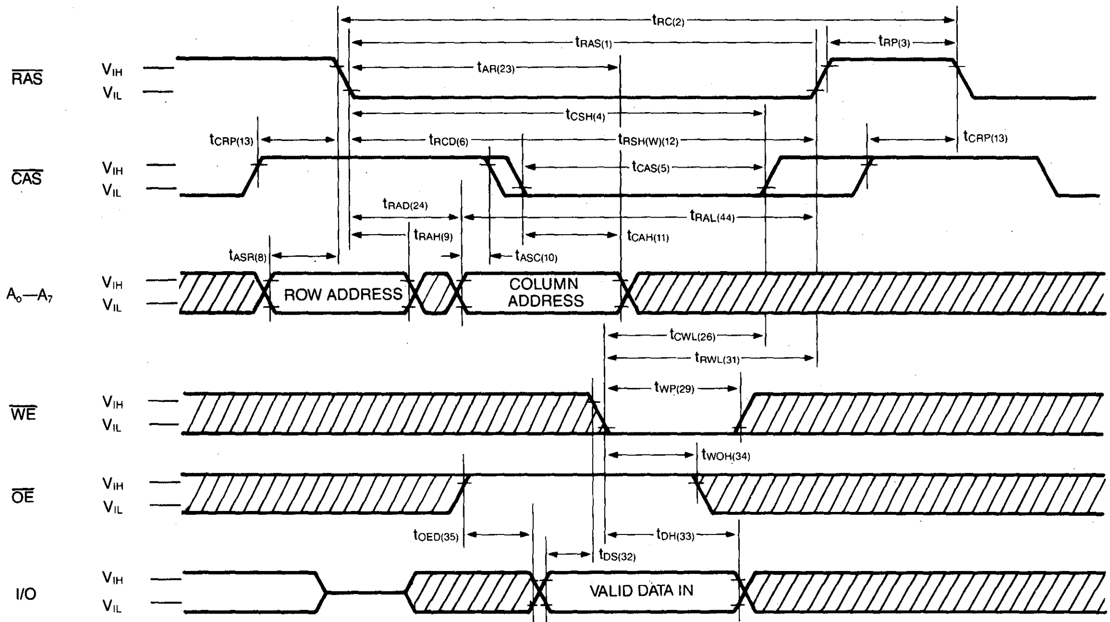
READ CYCLE



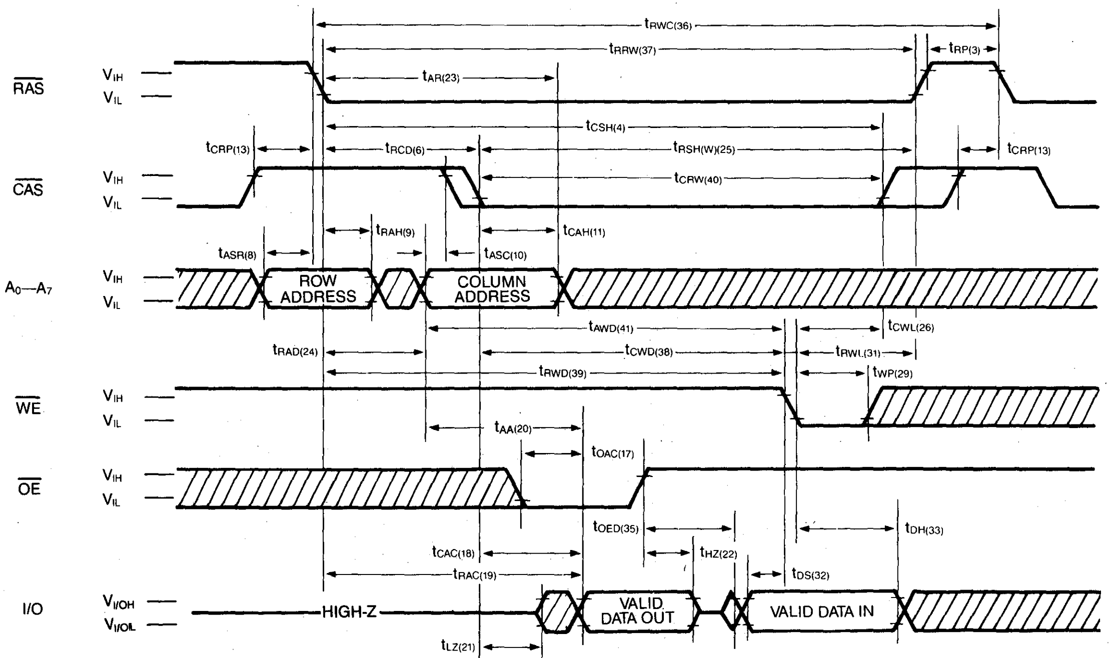
EARLY WRITE CYCLE



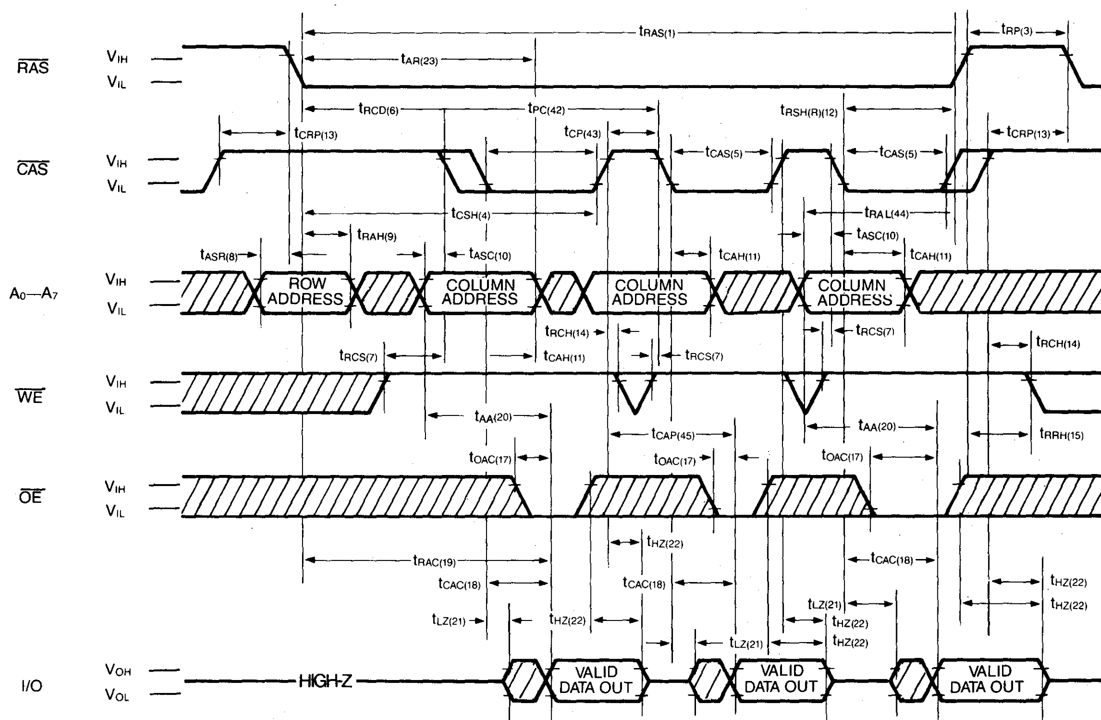
$\overline{\text{OE}}$ CONTROLLED WRITE CYCLE



READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE



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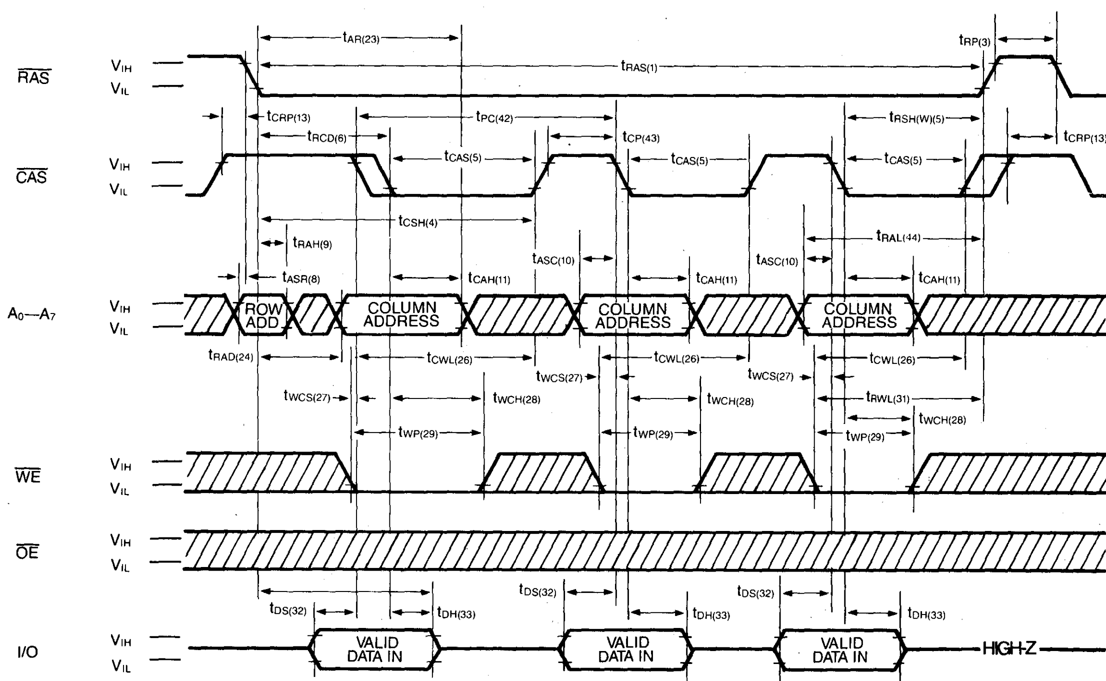
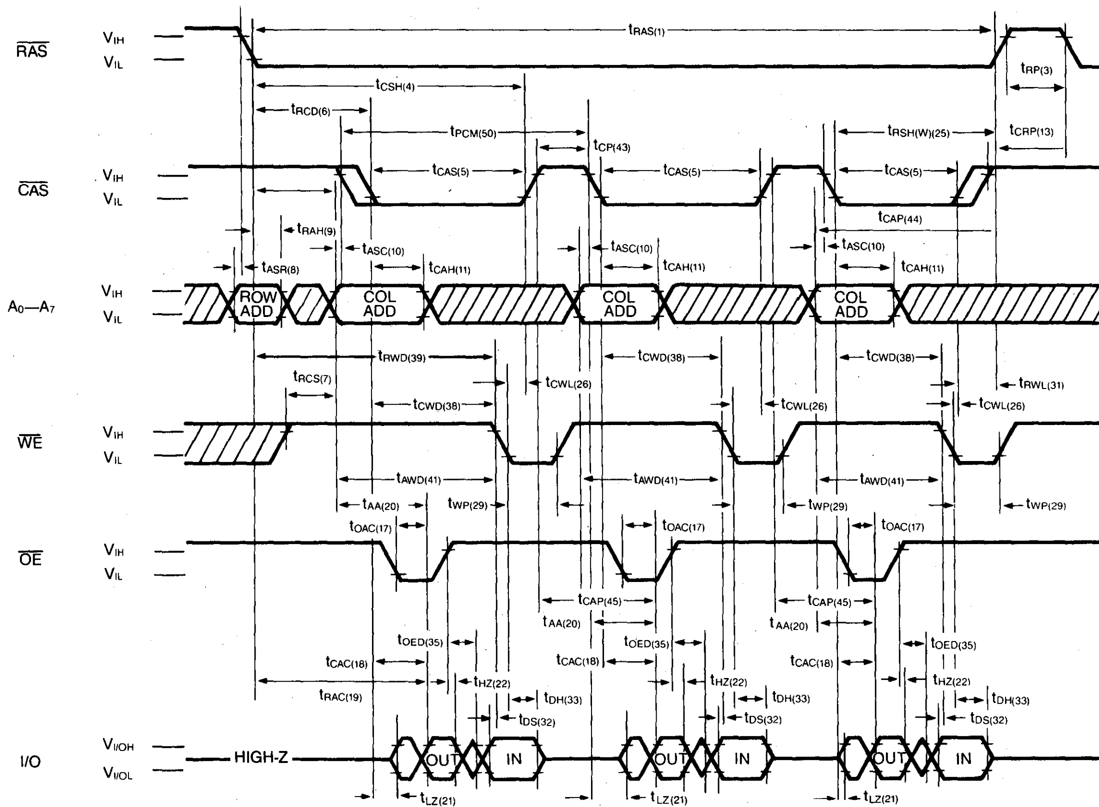
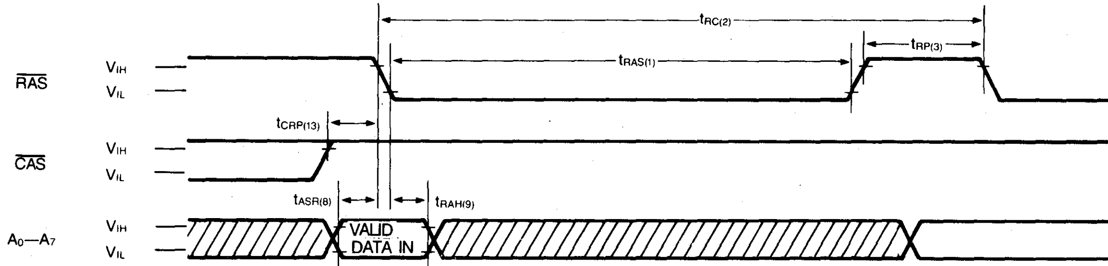
FAST PAGE MODE WRITE CYCLE



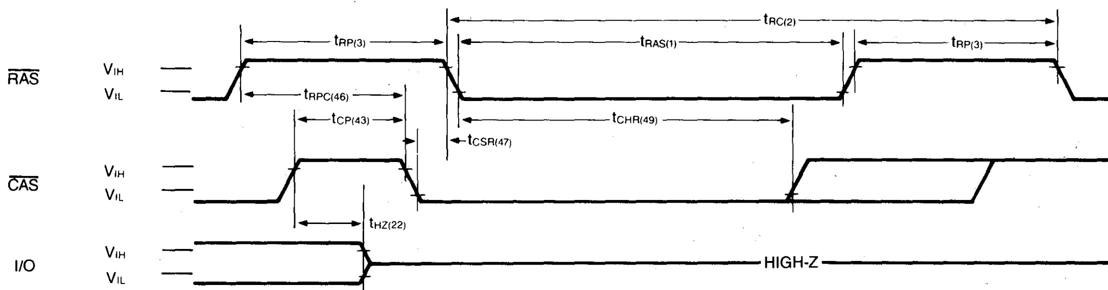
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



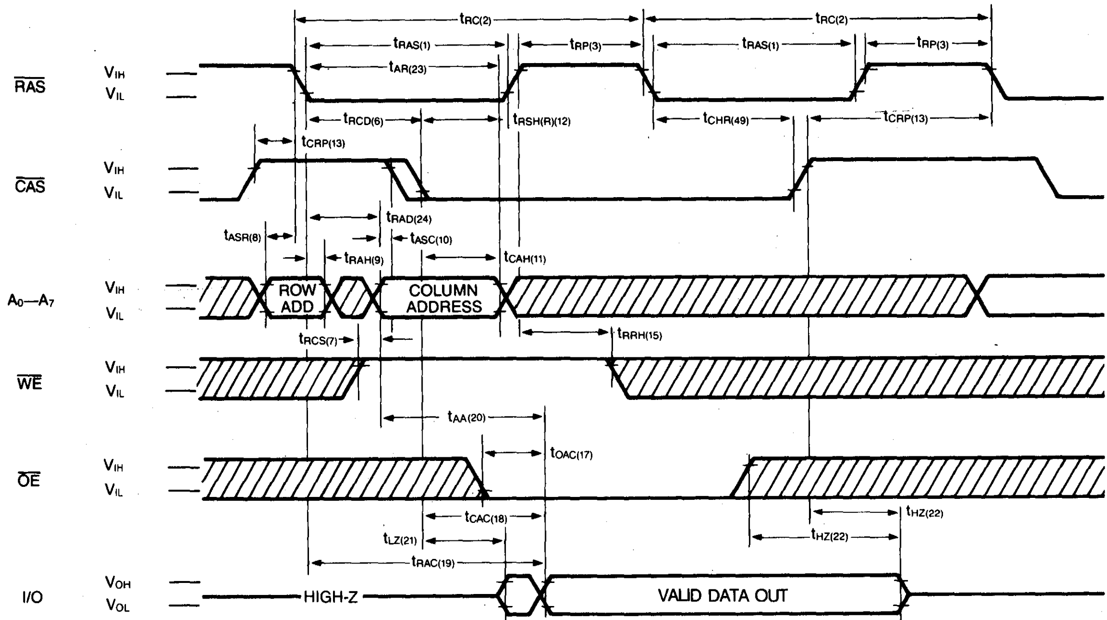
RAS-ONLY REFRESH CYCLE



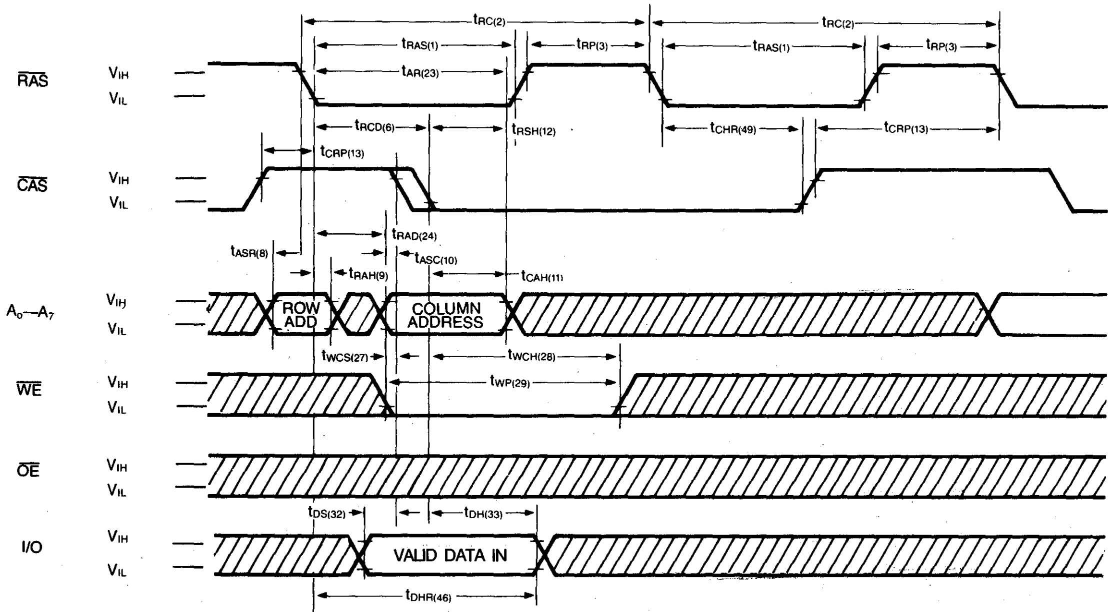
CAS-BEFORE-RAS REFRESH CYCLE



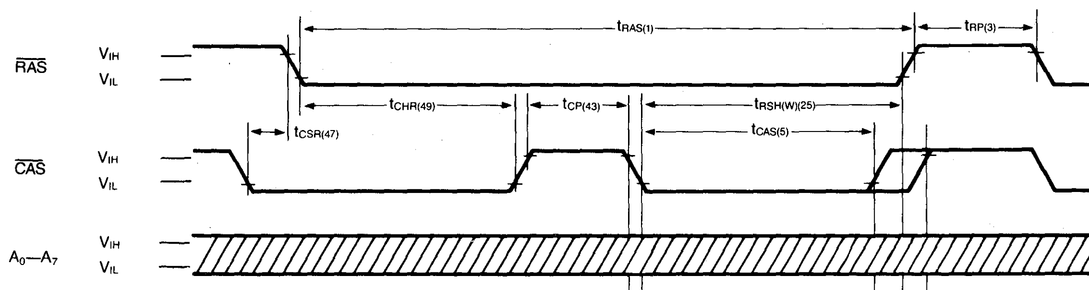
HIDDEN REFRESH CYCLE (READ)



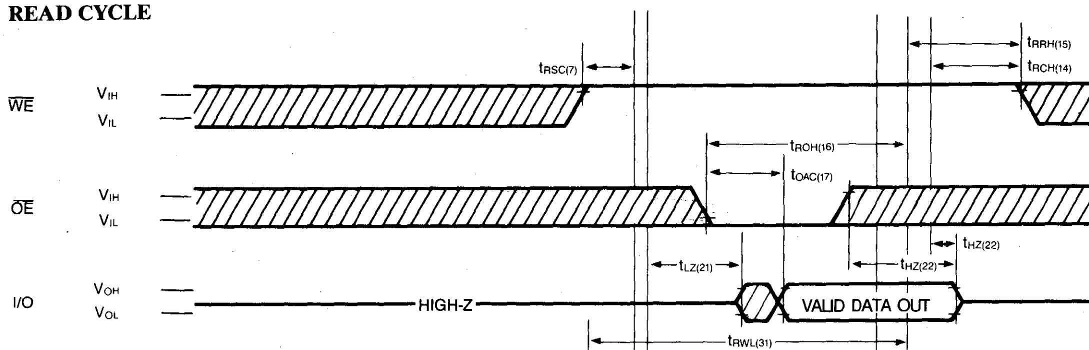
HIDDEN REFRESH CYCLE (WRITE)



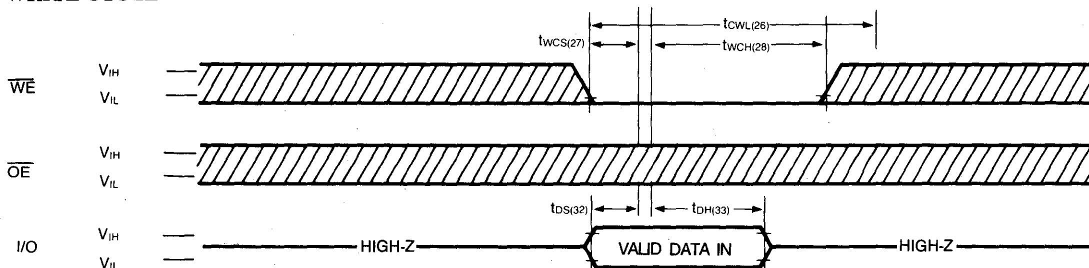
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



READ CYCLE



WRITE CYCLE



3

FUNCTIONAL DESCRIPTION

The HY53C464 is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The HY53C464 reads and writes data by multiplexing a 16-bit address into a 8-bit row and a 8-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address flows through an internal address buffer and is latched by the Column Address Strobe($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

MEMORY CYCLE

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data out becomes valid only when t_{OAC}, t_{AA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{AA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled write cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the write functionl. Ending the write $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled write cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

REFRESH CYCLE

To retain data, 256 refresh cycles are required in each 4 ms period. There are two ways to refresh the memory.

1. By clocking each of the 256 row addresses(A_0 through A_7) with $\overline{RAS}$ at least once every 4ms. Any read, wrtie, read-modify-write or $\overline{RAS}$-only cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The HY53C464 will use the output of an internal 8-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output will remain in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure rehable operation of the internal refresh counter.

DATA RETENTION MODE

The HY53C464 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY53C464 power consumption is reduced to the low I_{DD5} level. Overall I_{DD} consumption when operating in this mode can be calculated as foolows :

$$I=\frac{(t_{RC})\times(I\ active)+(t_{RX}-t_{RC})\times(I_{DD5})}{t_{RX}}$$

Where t_{RC}=Refresh Cycle Time
t_{RX}=Refresh Interval/256

FAST PAGE MODE OPERATION

Fast page mode operation permits all 256 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable.

During fast page mode operation, read, write, read-modify-write, or read-write-read cycles are possible at random addresses within a row. Following the initial entry cycle into fast page mode, access is t_{AA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge.(Specified by t_{CAP} as shown in figure 1). If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of the valid address and is specified by t_{AA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enable the output.

Fast page mode provides a sustained data rate of over 20 MHz for applications that require high data rates such as bit-mapped graphics or highspeed signal processing. The following equation can be used to calculate the maximum data rate :

$$\text{Data Rate} = \frac{256}{t_{RC} + 255 \times t_{PC}}$$

DATA OUTPUT OPERATION

The HY53C464 input/output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the memory array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the outpu drivers when $\overline{CAS}$ is low. During a write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow data in setup time(t_{DS}) to be satisfied.

POWER ON

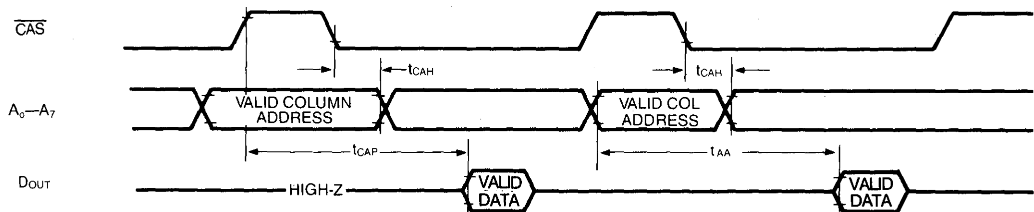
After application of the V_{DD} an initial pause of 200μs is required followed by a minimum of 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clcocks(greater than the Refresh Interval).

During power on, the V_{DD} current requirement of the HY53C464 is dependant on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during power on, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on to avoid current surges.

TABLE 1. DATA OUTPUT OPERATION FOR VARIOUS CYCLE TYPES

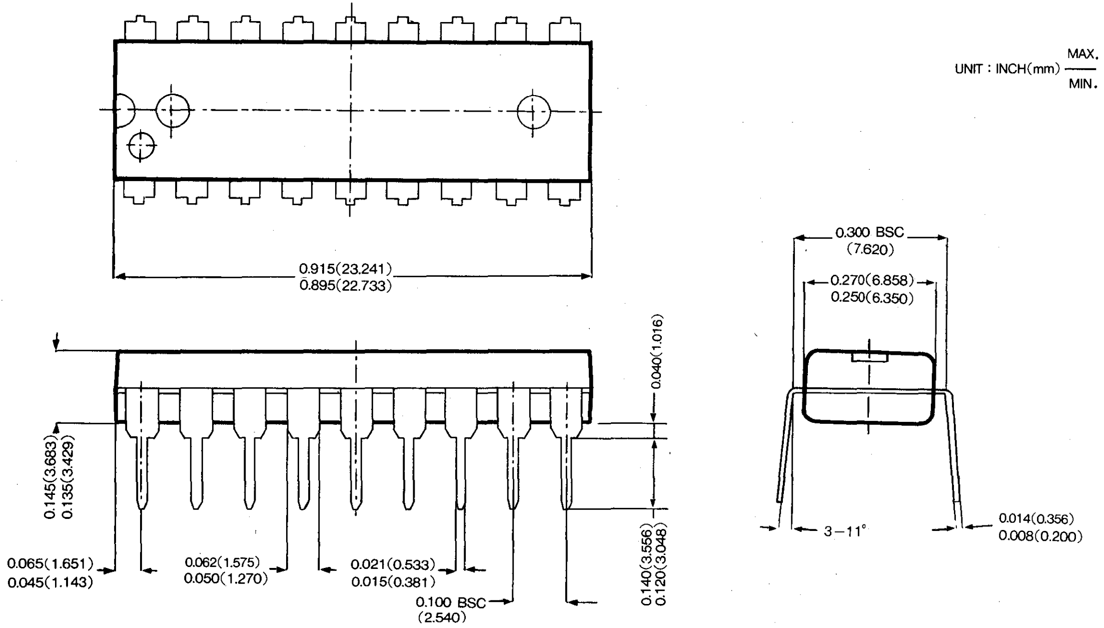
CYCLE TYPE	D_{OUT} STATE
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle(Early Write)	High-Z
$\overline{WE}$-Controlled Wirte Cycle(Late Write)	$\overline{OE}$ Controlled, High $\overline{OE}$=High-Z I/O
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh Cycle	High-Z
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle	Data Remains as in Previous Cycle
$\overline{CAS}$-only Cycle	High-Z

FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION

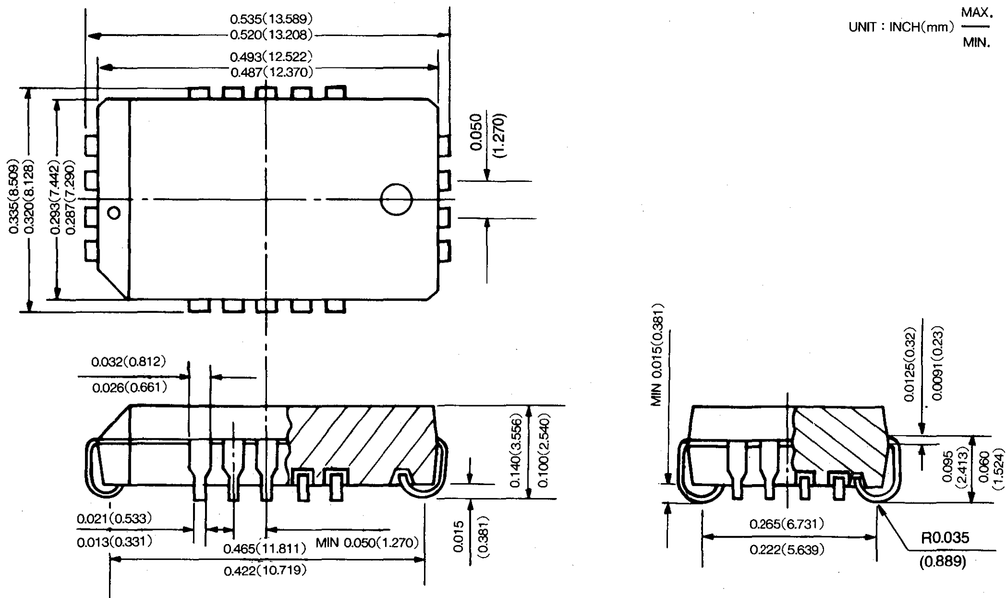


PACKAGE INFORMATION

• **18 PIN PLASTIC DUAL IN LINE PACKAGE−300 MIL**



• **18 PIN PLASTIC LEADED CHIP CARRIER −330 MIL**



MEMO

HY51C1000

1M×1-Bit CMOS DRAM

M131202B-APR91

DESCRIPTION

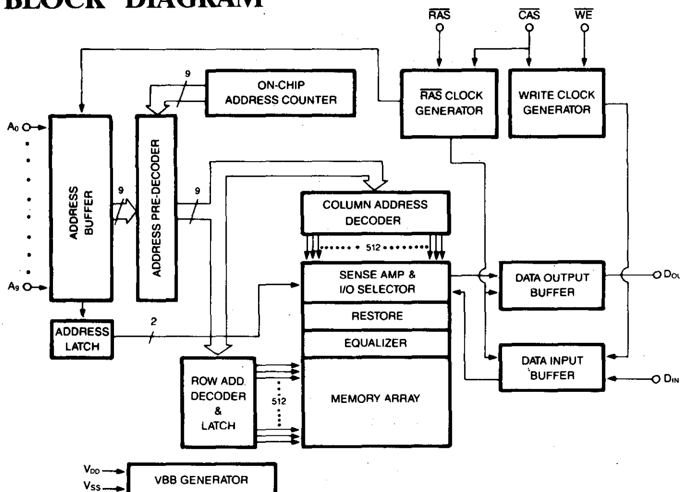
The HY51C1000 is a high speed, low power 1,048,576×1 bit CMOS dynamic random access memory. Fabricated with the HYUNDAI CMOS process, the HY51C1000 offers a fast page mode for high bandwidth and clock-free page operation, fast usable speed, CMOS standby current and inherently high CMOS reliability.

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance.

Fast page mode operation allows random or sequential access of up to 1,024 bits within a row with cycle times as fast as 45ns. Because of static circuitry, the $\overline{\text{CAS}}$ clock is no longer in the critical timing path. The flow-through column latch allows address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the HY51C1000 ideally suited for cache based mainframe and mini computers, graphics, digital signal processing, and high performance microprocessor systems.

When $\overline{\text{RAS}}$ is $\geq V_{DD}-0.2V$, CMOS standby operation mode is active, and power drops to 1.5 mW (typically).

BLOCK DIAGRAM



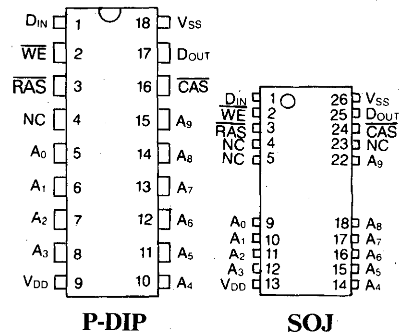
FEATURES

- Low power dissipation
  - Operating current, 100ns : 75mA (max.)
  - TTL standby current : 2.5mA (max.)
  - CMOS standby current : 1.5mA (max.)
- Read-Modify-Write capability
- $\overline{\text{RAS}}$-only, Hidden, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- Common I/O capability
- Fast Page mode operation for a sustained data rate up to 22 MHz
- 512 refresh cycles/8 ms
- High reliability 18 pin 300 mil P-DIP and 20/26 pin SOJ
- Fast access time and cycle time (ns)

	HY51C1000-80	HY51C1000-10	HY51C1000-12
Max $\overline{\text{RAS}}$ Access Time, t_{RAC}	80	100	120
Max $\overline{\text{CAS}}$ Access Time, t_{CAC}	20	25	30
Min Fast Page Mode Cycle Time, t_{PC}	45	55	65
Min Cycle Time, t_{RC}	160	190	220

3

PIN CONNECTIONS



PIN NAMES

$\overline{\text{RAS}}$	ROW ADDRESS STROBE
$\overline{\text{CAS}}$	COLUMN ADDRESS STROBE
$\overline{\text{WE}}$	WRITE ENABLE
A_0-A_9	ADDRESS INPUT
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature (Plastic)	−55 to 125	°C
V_{TERM}	Voltage on Any Pin Except V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Data Out Current	50	mA
P_T	Power Dissipation	1.0	W

NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY51C1000		UNIT	NOTE
				MIN.	MAX.		
$\lvert I_{LI}\rvert$	Input Leakage Current (any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		–	10	μA	
$\lvert I_{LO}\rvert$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$ (min.)	−80	–	95	mA	1,2
			−10	–	75		
			−12	–	70		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH}, other inputs $\geq V_{SS}$		–	2.5	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$ (min.)	−80	–	95	mA	2
			−10	–	75		
			−12	–	70		
I_{DD4}	V_{DD} Supply Current, Fast page mode	Minimum Cycle	−80	–	50	mA	1,2
			−10	–	40		
			−12	–	35		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}$ −0.2V, $\overline{CAS}$= V_{IH}, other inputs $\geq V_{SS}$		–	1.5	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$ (min.)	−80	–	95	mA	2
			−10	–	75		
			−12	–	70		
V_{IL}	Input Low Voltage (all inputs)			−0.5	0.8	V	3
V_{IH}	Input High Voltage (all inputs)			2.4	$V_{DD}+1$	V	3
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTES:
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast page mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} may undershoot to −1.0V for a period not to exceed 20ns. All AC parameters are measured with V_{IL} (min.) $\geq V_{SS}$ and V_{IH} (max.) $\leq V_{DD}$.

AC CHARACTERISTICS
(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY51C1000						UNIT	NOTES
			80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	80	85K	100	85K	120	85K	ns	
2	t_{RC}	Random Read or Write Cycle Time	160	–	190	–	220	–	ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	70	–	80	–	90	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	15	–	15	–	15	–	ns	
6	t_{CAR}	Column Address to $\overline{RAS}$ Set-up Time	40	–	45	–	55	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	55	20	65	ns	1
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	20	–	25	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	60	25	75	25	90	ns	2
11	t_{RAC}	Access Time From $\overline{RAS}$	–	80	–	100	–	120	ns	3,4,5
12	t_{CAA}	Access Time From Column Address	–	40	–	45	–	55	ns	5,6,12
13	t_{CAC}	Access Time From $\overline{CAS}$	–	20	–	25	–	30	ns	6,12
14	$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width in Read Cycle	20	–	25	–	30	–	ns	
15	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time in Read Cycle	20	–	25	–	30	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5	–	5	–	5	–	ns	7
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5	–	5	–	5	–	ns	7
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	25	0	30	ns	8
21	t_{OH}	Output Data Hold Time From $\overline{CAS}$	0	–	0	–	0	–	ns	8
22	t_{WP}	Write Pulse Width	10	–	10	–	15	–	ns	
23	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	15	–	ns	
24	t_{AR}	Column Address Hold Time From $\overline{RAS}$	60	–	70	–	80	–	ns	
25	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width in Write Cycle	25	–	30	–	35	–	ns	
26	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time in Write Cycle	25	–	30	–	35	–	ns	
27	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	60	–	70	–	80	–	ns	
28	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	9,10
29	t_{WCH}	Write Command Hold Time	15	–	20	–	25	–	ns	
30	t_{DS}	Data-In Set-up Time	0	–	0	–	0	–	ns	11
31	t_{DH}	Data-In Hold Time	15	–	20	–	25	–	ns	11
32	t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	60	–	70	–	80	–	ns	
33	t_{RWC}	RMW Cycle Time	190	–	220	–	255	–	ns	
34	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	110	–	130	–	155	–	ns	
35	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in RMW Cycle	80	–	100	–	120	–	ns	9
36	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	20	–	25	–	30	–	ns	9
37	t_{AWD}	Column Address to $\overline{WE}$ Delay	40	–	45	–	55	–	ns	9
38	t_{CAP}	Access Time From Column Precharge	–	40	–	50	–	60	ns	12

#	SYMBOL	PARAMETER	HY51C1000						UNIT	NOTES
			80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
39	t_{PC}	Fast page mode Read or Write Cycle time	45	–	55	–	65	–	ns	
40	t_{PCM}	Fast page mode Read-Modify-Write Cycle	70	–	85	–	100	–	ns	
41	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	–	25	–	30	–	ns	
42	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	–	25	–	30	–	ns	
43	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
44	t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
45	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	20	–	30	–	30	–	ns	
46	t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	120	–	ns	
47	t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	13,14
48	t_{RI}	Refresh Interval (512 Cycle)	–	8	–	8	–	8	ms	15

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{CAA} and t_{CAC}.
2. t_{RCD}(max.) is specified for reference only. Operation within t_{RCD}(max.) and t_{RAD}(max.) limit insure that t_{RAC}(max.) and t_{CAA}(max.) can be met. If t_{RCD} is greater than the specified t_{RCD}(max.) then the access time is controlled by t_{CAA} and t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.) If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.)
4. Assume $t_{RCD} \leq t_{RCD}$(max.) If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.)
5. Measured with a load equivalent to two TTL loads and 100 pF.
6. Assume $t_{RAD} \geq t_{RAD}$(max.)
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
8. t_{OFF} and t_{OH} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
9. t_{WCS}, t_{WHC}, t_{WHR}, t_{RWD}, t_{AWD}, t_{CWD}, are not restrictive operating parameters.
10. t_{WCS}(min.) must be satisfied in the early write cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$.
12. Access time is determined by the longer of t_{CAA}, t_{CAC} or t_{CAP}.
13. t_T is measured between V_{IH} (min.) and V_{IL} (max.)
14. AC measurements assume t_T=5ns.
15. An initial pause of 200μs is required after power-up and followed by a minimum of 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

CAPACITANCE

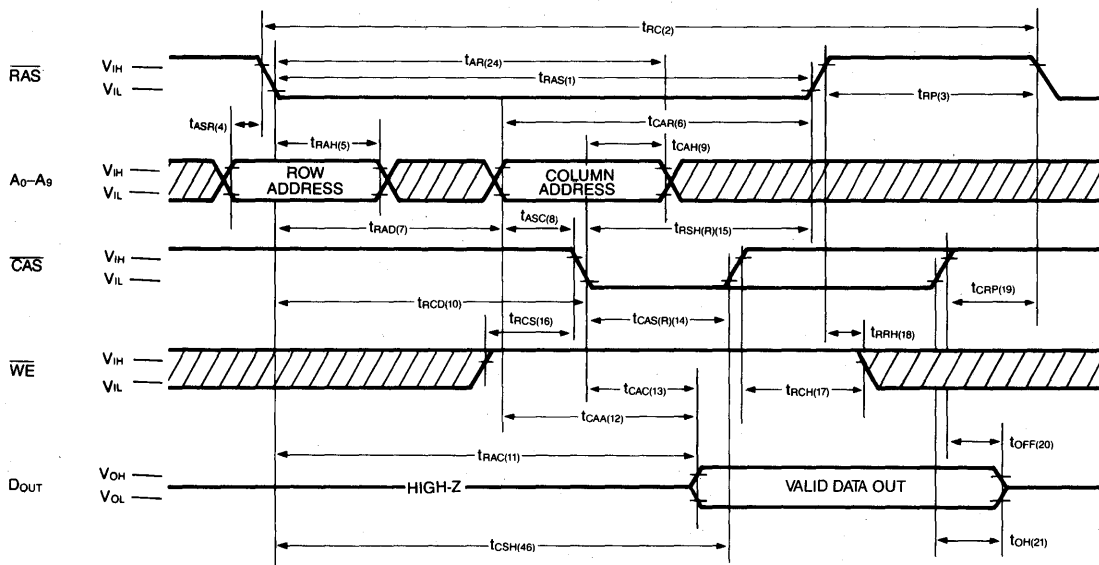
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, D_{IN}	–	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	–	8	pF
C_{OUT}	D_{OUT}	–	8	pF

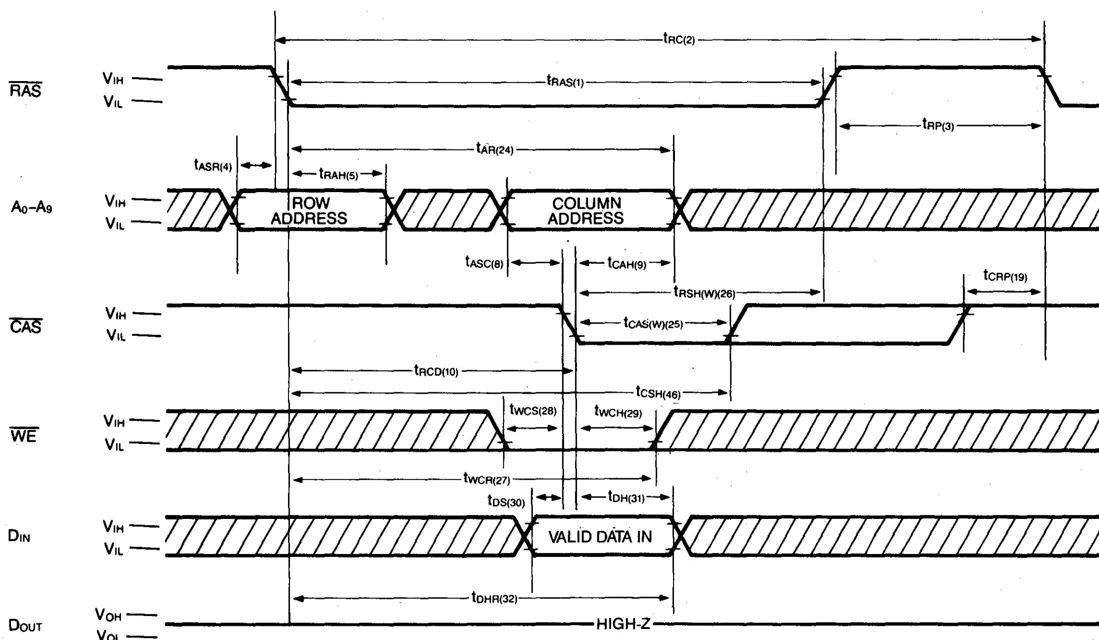
NOTE: Capacitance is measured at the worst case of voltage levels with a programmable capacitance meter.

TIMING DIAGRAM

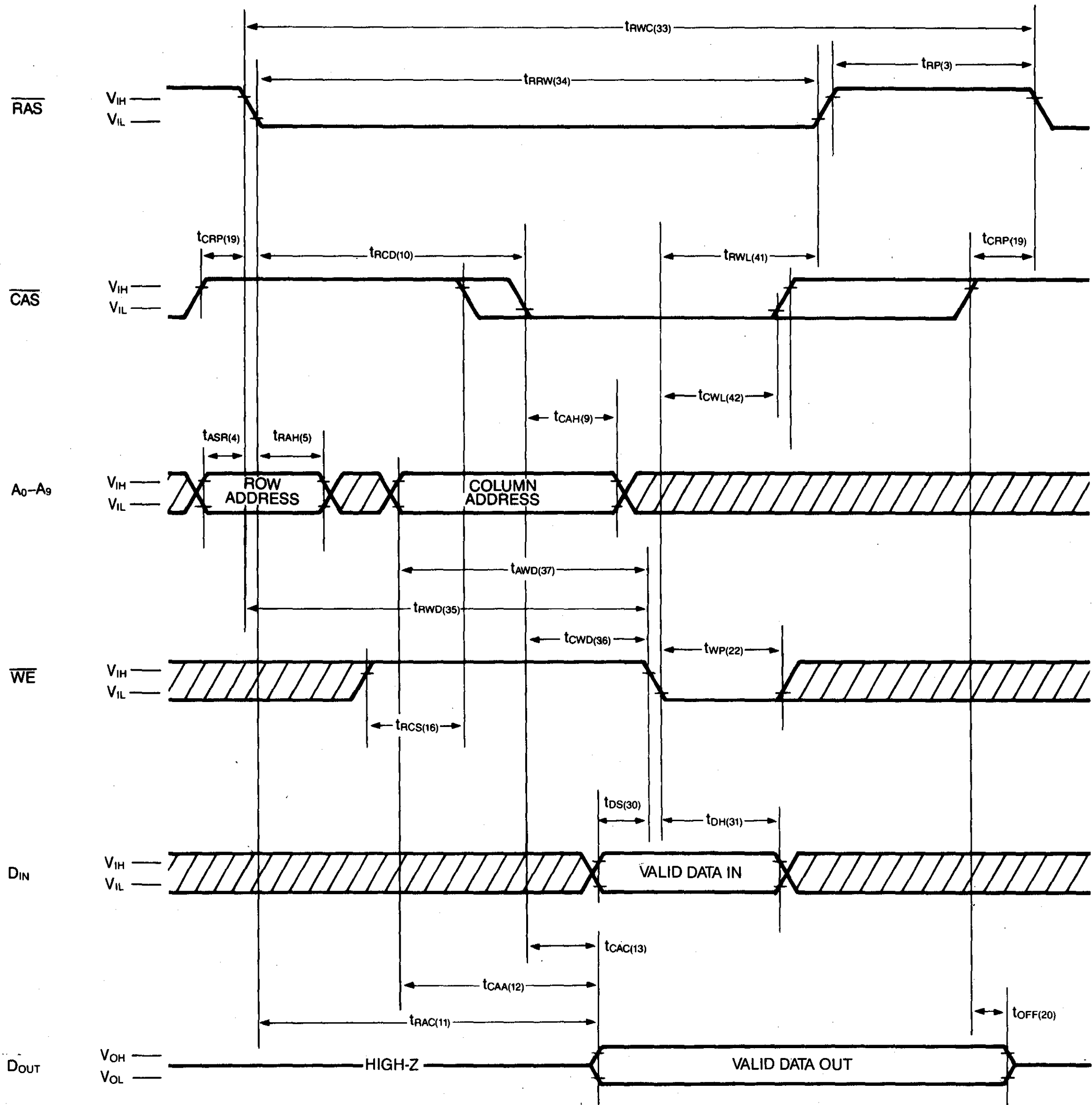
READ CYCLE



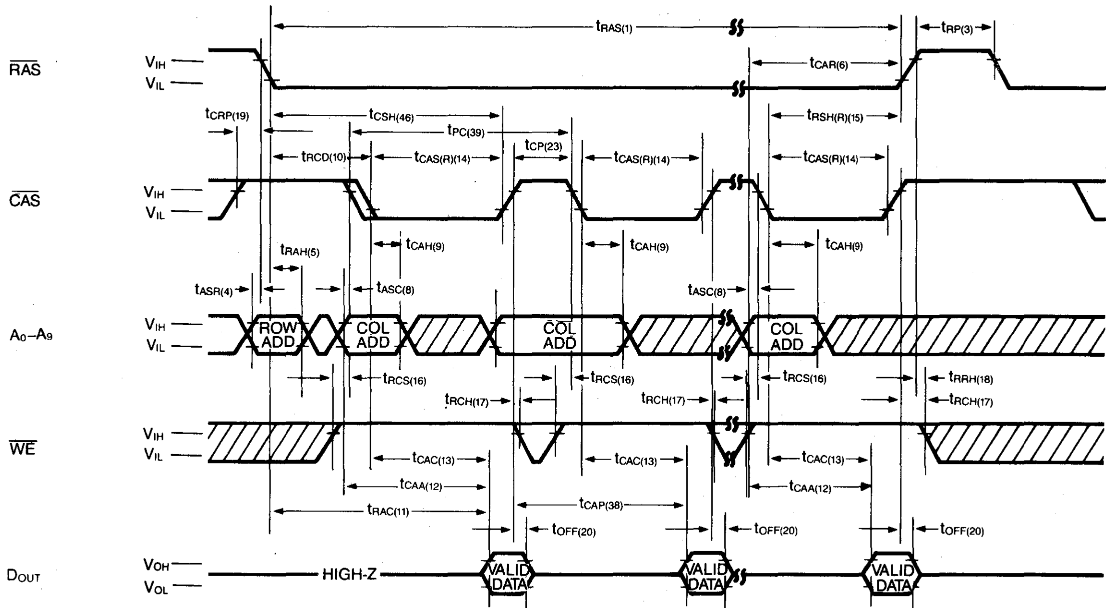
EARLY WRITE CYCLE



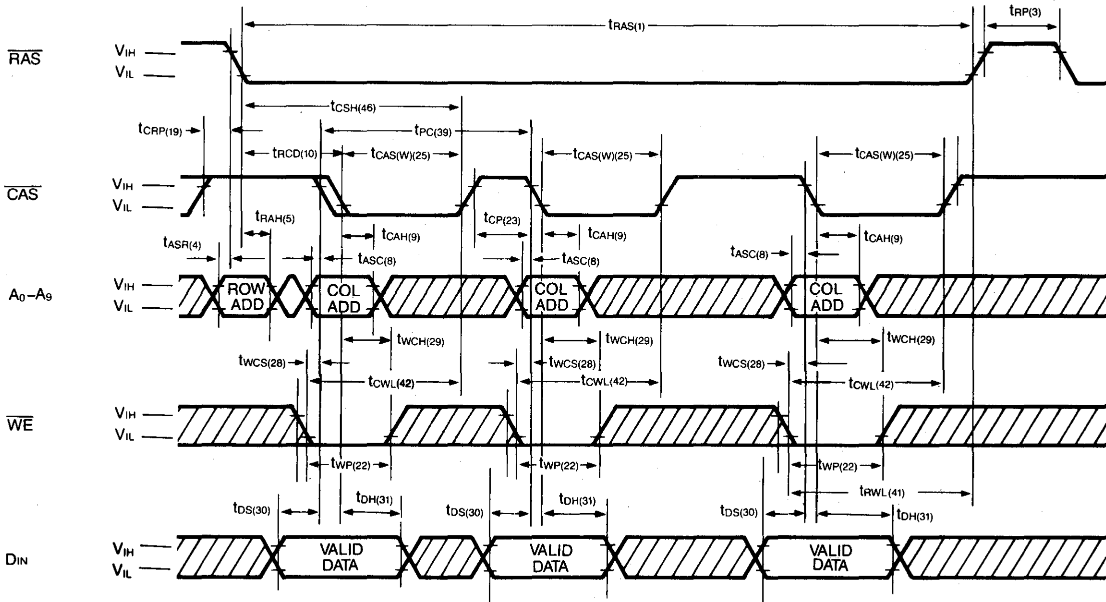
READ-MODIFY-WRITE CYCLE



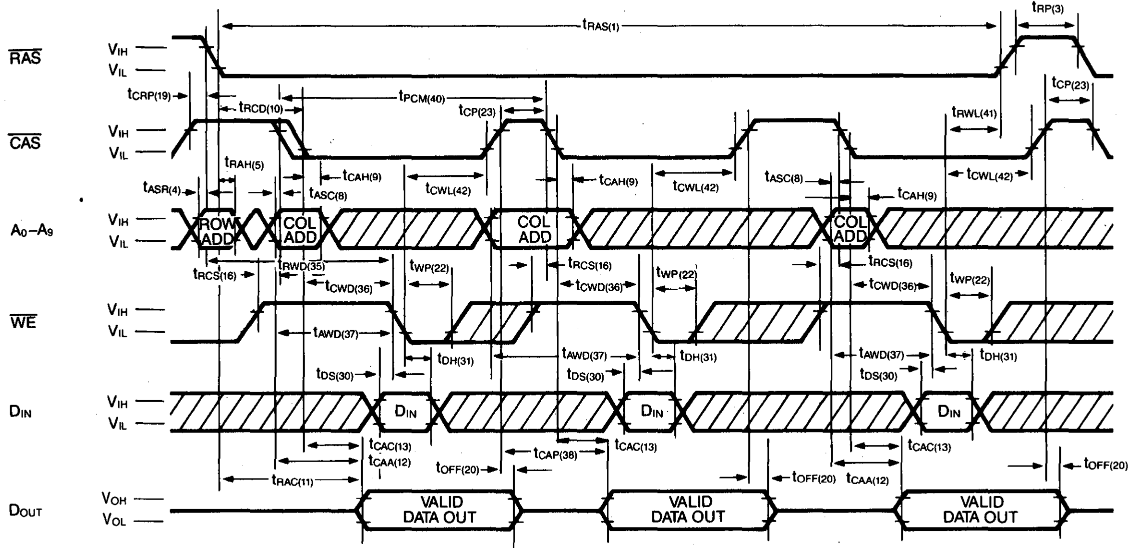
FAST PAGE MODE READ CYCLE



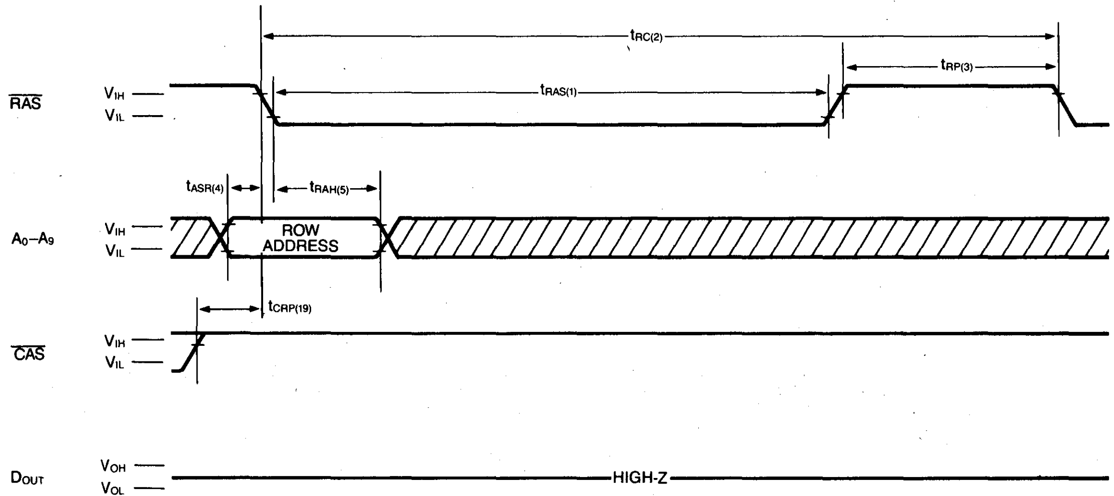
FAST PAGE MODE EARLY WRITE CYCLE



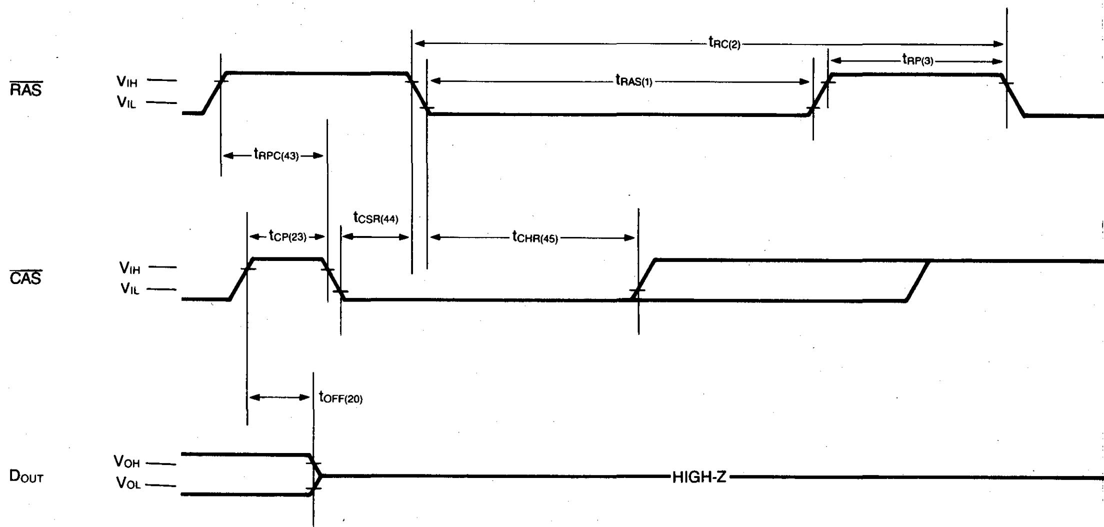
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



Note: $\overline{WE}$, $\overline{A_0–A_9}$ = Don't care

HIDDEN REFRESH CYCLE (READ)

$\overline{RAS}$ VIH VIL

tRAS(1) tRP(3) tRAS(1)

tCRP(19) tRCD(10) tRSH(R)(15) tCHR(45)

$\overline{CAS}$ VIH VIL

tASC(8)

tCAR(6)

tRAD(7)

tRAH(5)

tASR(4) tCAH(9)

$A_0–A_9$ VIH VIL ROW ADDRESS COLUMN ADDRESS

tAR(24)

tRCS(16) tRRH(18)

$\overline{WE}$ VIH VIL

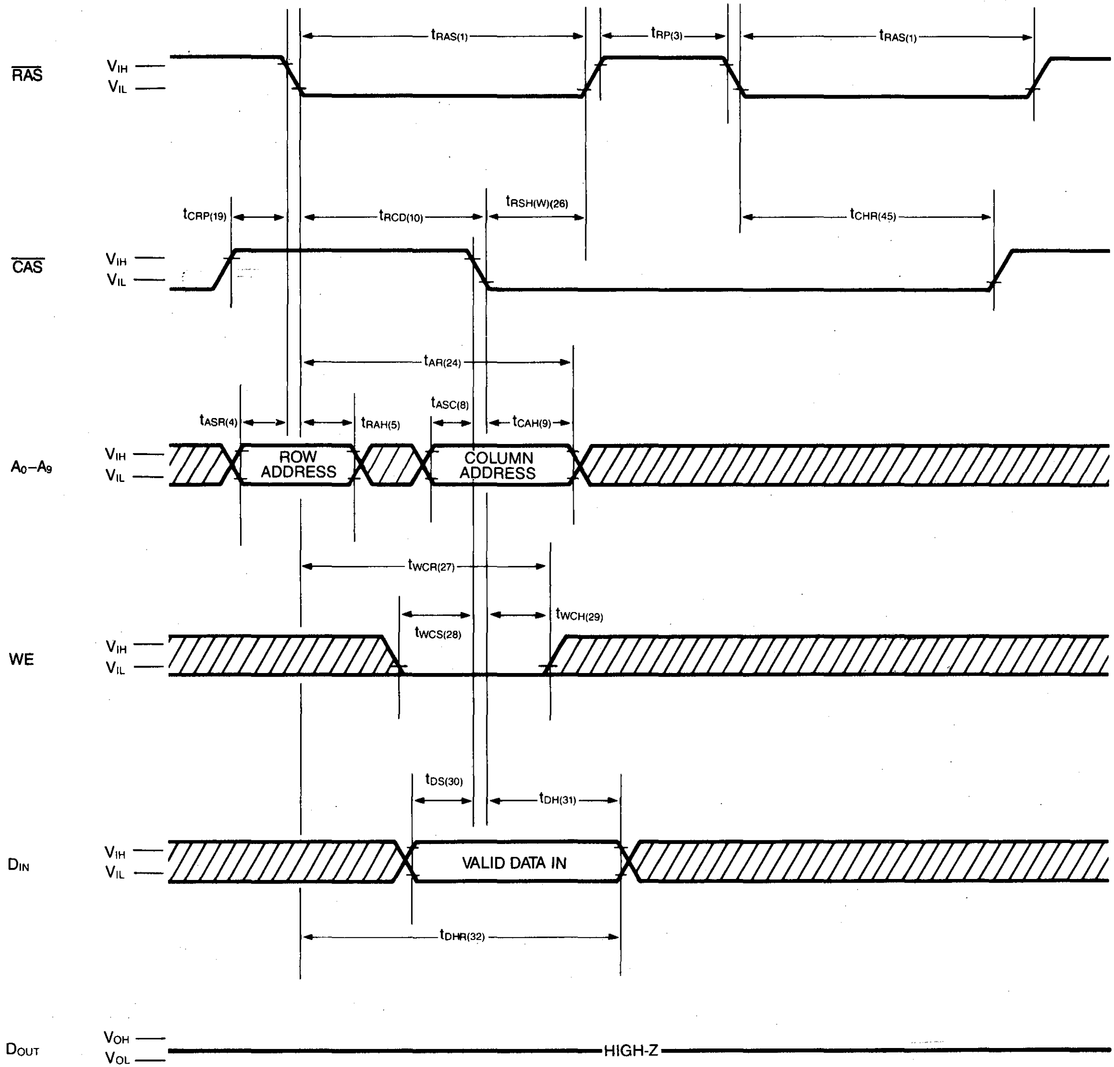
tCAC(13)

tCAA(12)

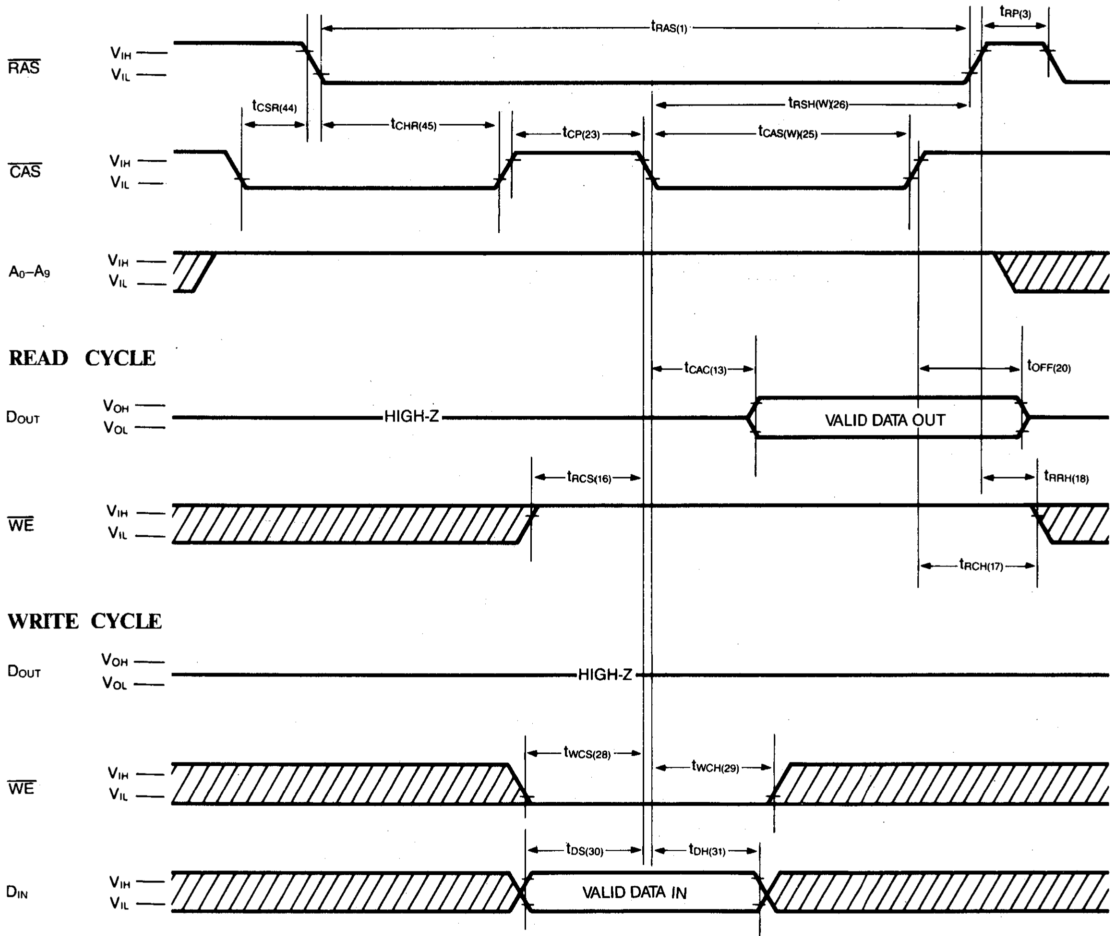
tRAC(11) tOFF(20)

DOUT VOH VOL HIGH-Z VALID DATA OUT

HIDDEN REFRESH CYCLE (WRITE)



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

The HY51C1000 is a CMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The HY51C1000 reads and writes one bit of data by multiplexing 20 bit address into 10 bit row and 10 bit column address. The row address is latched by Row Address Strobe($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

MEMORY CYCLE

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle can not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data output becomes valid only when t_{RAC}, t_{CAC} and t_{CAA} are all satisfied. Consequently, the access time is dependent upon the timing relationship among the t_{RAC}, t_{CAC} and t_{CAA}. For example, the access time is limited by t_{CAA} when t_{RAC} and t_{CAC} are both satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the latter of $\overline{WE}$ or $\overline{CAS}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$ controlled write cycle (the leading edge or $\overline{WE}$ occurs priors to or coincident with the $\overline{CAS}$ low transition) the output(D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{RAS}$ or $\overline{CAS}$ going high will maintain the data output (D_{OUT}) in the high impedance state.

REFRESH CYCLE

To retain data, 512 $\overline{RAS}$ refresh cycle are required in an 8 ms period. The refresh operation can be performed two ways :

1. Clocking each of 512 row address(A_0 through A_8) with $\overline{RAS}$ at least every 8 ms period. Any combination of $\overline{RAS}$ cycle such as read, write, read-modify-write, or $\overline{RAS}$-Only refresh cycle will perform a refresh on the selected row.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle : If $\overline{CAS}$ go low prior to $\overline{RAS}$ go low, the chip enters a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. In $\overline{CAS}$ before-$\overline{RAS}$-refresh cycle the HY51C1000 will use an internal nine-bit counter output as the source of the row address and will ignore the external address input.

This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh only mode and no data access is allowed. Also, the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle does not cause device selection and the state of the data output pin will remain in a high impedance state.

In order to guarantee the reliable operation of the $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, a internal counter test mode is provided. The user can use the counter test mode to write in a data pattern consecutively (512 write cycles) and then verify the data which has been written by 512 consecutive read cycles.

DATA RETENTION MODE

The HY51C1000 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock

to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY51C1000 power consumption is reduced to the low I_{DD5} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows :

$$I = \frac{(t_{RC}) \times (I\ active) + (t_{RX} - t_{RC}) \times (I_{DD5})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval/512

FAST PAGE MODE OPERATION

Fast page mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent or flow through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latch the address into column address buffer and acts as an output enable.

During this operation, read, write, and read-modify-write, or read-write-read cycles are possible at random or sequential address within a row. Following the entry cycle into fast page mode, access time is t_{CAA} or t_{CAP} dependent. If the column adderess is valid prior to or coincident by t_{CAP} as shown in figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{CAA}. For both cases, the falling edge of $\overline{CAS}$ latches the address and enable the output.

Fast page mode provides a sustanined data rate over 22 MHz for applications that require high data rates, such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate :

$$Data\ Rate = \frac{1024}{t_{RC} + 1023 \times t_{PC}}$$

DATA OUT OPERATION

The HY51C1000 data output(D_{OUT}), which has tri-state capability, is controlled by $\overline{CAS}$. During a $\overline{CAS}$ the high state ($\overline{CAS}$ at V_{IH}), the data output is in the high impedance state. The following table summarize the D_{OUT} state for various types of cycles.

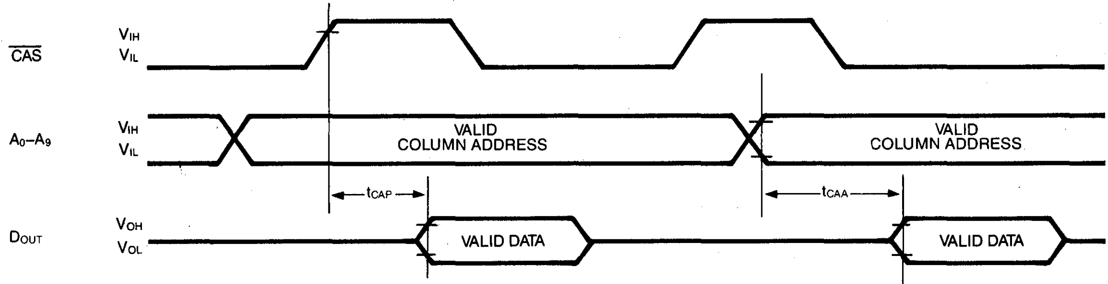
CYCLE	D_{OUT} STATE
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$ Controlled Write Cycle (Early Write)	High Impedance
$\overline{WE}$ Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High Impedance
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-Only Refresh Cycle	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle	Data remain the previous cycle's state (high Impedance or low Impedance
$\overline{CAS}$-Only Cycle	High Impedance

POWER ON

An initial pause of 200 μs is required after the application of the V_{DD} power supply, followed by a minimum of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh cycle). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

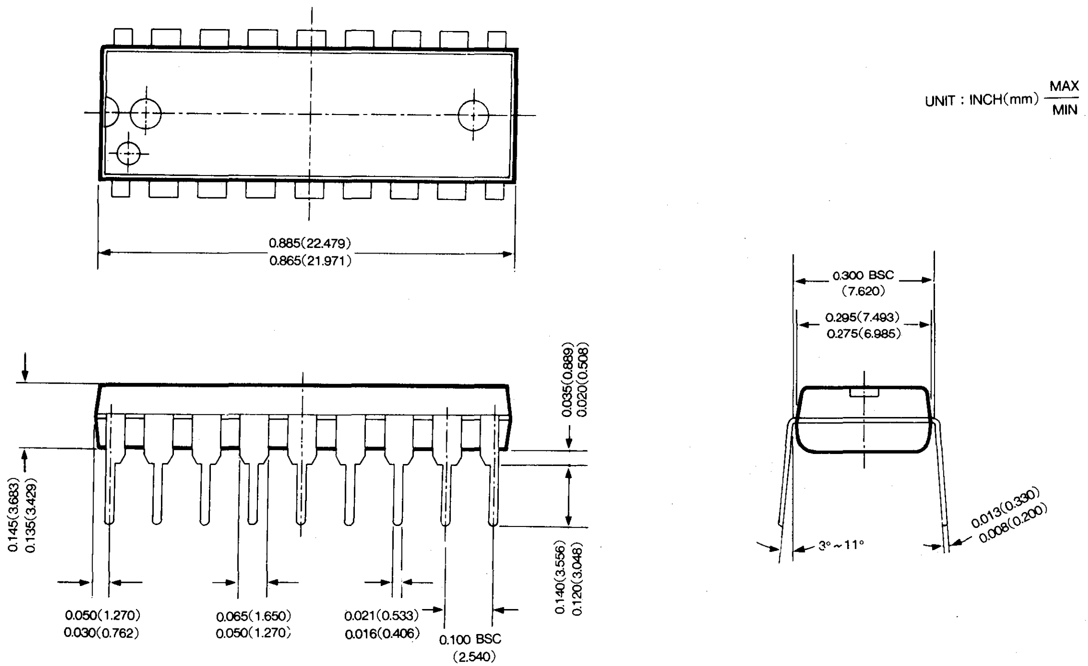
The V_{DD} current (I_{DD}) requirement of the HY51C1000 during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS} = V_{SS}$ during power on, the device will go into an active cycle and I_{DD} will exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} level during power on.

FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION

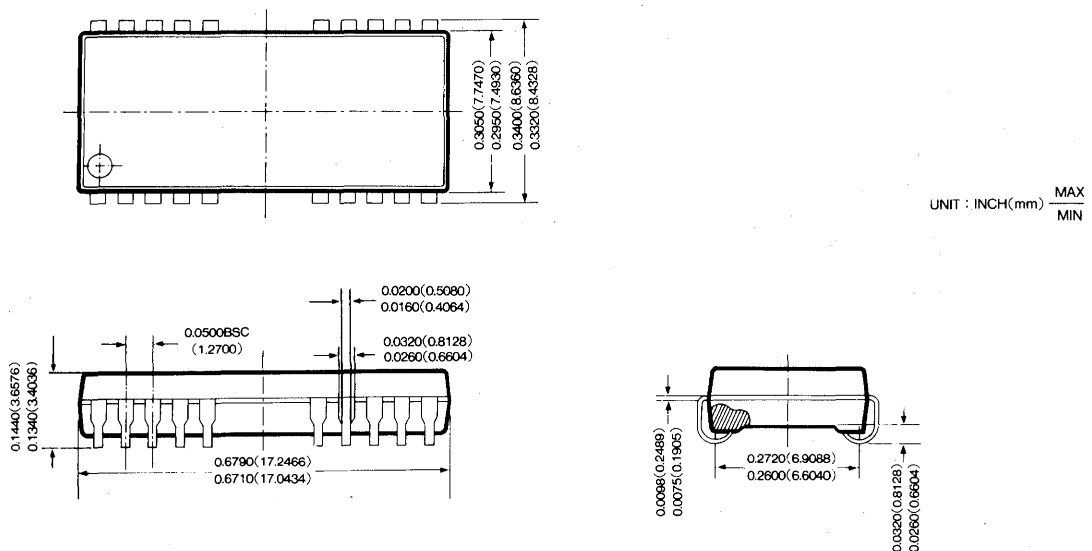


PACKAGE INFORMATION

- **18 PIN PLASTIC DUAL IN LINE PACKAGE – 300 MIL**



- **20/26 PIN SMALL OUTLINE J-FORM PACKAGE – 300 MIL**



MEMO

HYUNDAI SEMICONDUCTOR

HY51C4256

256K×4-Bit CMOS DRAM

M151201C-JAN92

DESCRIPTION

The HY51C4256 is a high speed, low power 262,144×4 CMOS dynamic random access memory. Fabricated with HYUNDAI CMOS technology, HY51C4256 offers a fast page mode for high data bandwidth, fast usable speed, CMOS standby current and extended $\overline{RAS}$-only refresh for low standby power.

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance.

Fast page mode operation allows random or sequencial access of all 512(×4)bits within a row simply by changing the column address. Because the column address access time is as fast as 50ns, a continuous data rate exceeding 20 MHz can be achieved.

The HY51C4256 offers high performance while relaxing many critical system timing requirements. These features make HY51C4256 ideally suited for graphics, digital signal processing, and high performance systems.

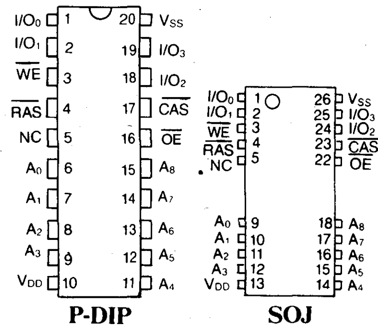
When $\overline{RAS}$ is $\geq V_{DD}-0.2V$, CMOS standby operation mode is active, and power drops to 1.5 mW (typically).

FEATURES

- **Low power dissipation**
  - **Operating current, 100ns : 75mA (max.)**
  - **TTL standby current : 2.5mA (max.)**
  - **CMOS standby current : 1.5mA (max.)**
- **Read-Modify-Write capability**
- **$\overline{RAS}$-only, Hidden, $\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **Fast Page mode operation for a sustained data rate up to 20 MHz**
- **512 refresh cycles/8 ms**
- **High reliability 20 pin 300 mil P-DIP and 20/26 pin SOJ**
- **Fast access time and cycle time (ns)**

	HY51C4256-80	HY51C4256-10	HY51C4256-12
Max $\overline{RAS}$ Access Time, t_{RAC}	80	100	120
Max $\overline{CAS}$ Access Time, t_{CAC}	20	25	30
Min Fast Page Mode Cycle Time, t_{PC}	50	65	75
Min Cycle Time, t_{RC}	160	190	220

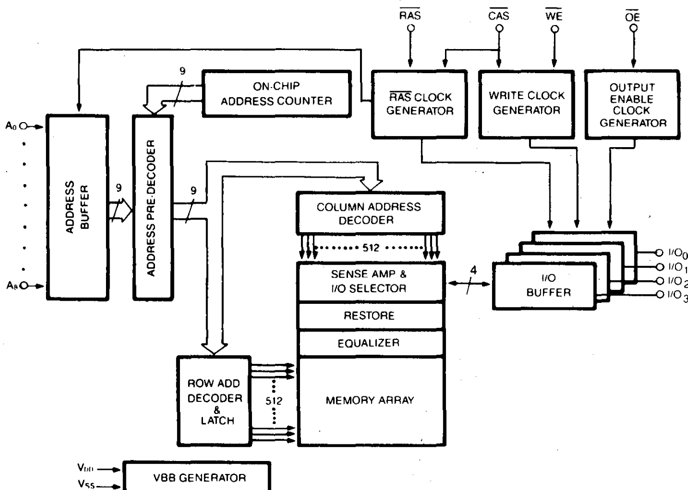
PIN CONNECTIONS



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
A_0-A_8	ADDRESS INPUT
I/O_0-I/O_3	DATA INPUT/OUTPUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature (Plastic)	−55 to 125	°C
V_{TERM}	Voltage on Any Pin Except V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Data Out Current	50	mA
P_T	Power Dissipation	1.0	W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" might cause permanent damage to the device.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY51C4256		UNIT	NOTE
				MIN.	MAX.		
$\lvert I_{LI} \rvert$	Input Leakage Current (any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$		–	10	μA	
$\lvert I_{LO} \rvert$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC} = t_{RC}$ (min.)	−80	–	95	mA	1,2
			−10	–	75		
			−12	–	70		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH}, other inputs $\ge V_{SS}$		–	2.5	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC} = t_{RC}$ (min.)	−80	–	95	mA	2
			−10	–	75		
			−12	–	70		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−80	–	50	mA	1,2
			−10	–	40		
			−12	–	35		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD} - 0.2V$, $\overline{CAS} = V_{IH}$, other inputs $\ge V_{SS}$		–	1.5	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC} = t_{RC}$ (min)	−80	–	95	mA	2
			−10	–	75		
			−12	–	70		
V_{IL}	Input Low Voltage (all inputs)			−0.5	0.8	V	3
V_{IH}	Input High Voltage (all inputs)			2.4	V_{DD}+1	V	3
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH} = −5mA		2.4	–	V	

NOTES:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in fast page mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} may undershoot to −1.0V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY51C4256						UNIT	NOTE
			80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	80	85K	100	85K	120	85K	ns	
2	t_{RC}	Random Read or Write Cycle Time	160	–	190	–	220	–	ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	70	–	80	–	90	–	ns	
4	t_{CSH}	$\overline{CAS}$ Hold Time	80	–	100	–	120	–	ns	
5	t_{CAS}	$\overline{CAS}$ Pulse Width	30	–	35	–	40	–	ns	
6	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	50	25	65	30	80	ns	2
7	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
8	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{RAH}	Row Address Hold Time	15	–	15	–	20	–	ns	
10	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
11	t_{CAH}	Column Address Hold Time	15	–	20	–	25	–	ns	
12	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time in Read Cycle	30	–	35	–	40	–	ns	
13	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	–	15	–	20	–	ns	
14	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5	–	5	–	5	–	ns	7
15	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5	–	5	–	5	–	ns	7
16	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	0	–	0	–	0	–	ns	
17	t_{OAC}	Access Time from $\overline{OE}$	–	20	–	25	–	30	ns	
18	t_{CAC}	Access Time from $\overline{CAS}$	–	30	–	35	–	40	ns	12
19	t_{RAC}	Access Time from $\overline{RAS}$	–	80	–	100	–	120	ns	3,4,5
20	t_{CAA}	Access Time from Column Address	–	40	–	45	–	55	ns	5,6,12
21	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	14,15
22	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to Output High Impedance	0	20	0	25	0	30	ns	11,14,15
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	60	–	70	–	80	–	ns	
24	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	55	25	65	ns	1
25	$t_{RSH(W)}$	$\overline{RAS}$ Hold Time in Write Cycle	30	–	35	–	40	–	ns	
26	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	–	35	–	40	–	ns	
27	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	8,9
28	t_{WCH}	Write Command Hold Time	15	–	20	–	25	–	ns	
29	t_{WP}	Write Command Pulse Width	15	–	20	–	25	–	ns	
30	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	60	–	70	–	80	–	ns	
31	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	–	35	–	40	–	ns	
32	t_{DS}	Data-In Set-up Time	0	–	0	–	0	–	ns	10
33	t_{DH}	Data-In Hold Time	15	–	20	–	25	–	ns	10
34	t_{WOH}	Write to $\overline{OE}$ Hold Time	20	–	25	–	30	–	ns	
35	t_{OED}	$\overline{OE}$ to Data Delay	20	–	25	–	30	–	ns	
36	t_{RWC}	Read-Modify-Write (RMW) Cycle Time	220	–	265	–	305	–	ns	

#	SYMBOL	PARAMETER	HY51C4256						UNIT	NOTE
			80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
37	t_{RRW}	$\overline{RAS}$ Pulse Width (RMW)	140	–	175	–	205	–	ns	
38	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	60	–	70	–	80	–	ns	8
39	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	110	–	135	–	160	–	ns	8
40	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	90	–	110	–	125	–	ns	
41	t_{AWD}	Column Address to $\overline{WE}$ Delay	70	–	80	–	85	–	ns	8
42	t_{PCM}	Fast page mode Read-Modify-Write Cycle	50	–	65	–	75	–	ns	
43	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	20	–	25	–	ns	
44	t_{CAR}	Column Address to $\overline{RAS}$ Set-up Time	40	–	45	–	55	–	ns	
45	t_{CAP}	Access Time from Column Precharge	–	45	–	60	–	70	ns	12
46	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	60	–	70	–	80	–	ns	
47	t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
48	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
49	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	20	–	30	–	40	–	ns	
50	t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	13
51	t_{RI}	Refresh Interval (512 Cycle)	–	8	–	8	–	8	ms	16

NOTES:

1 Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then the access time is controlled by t_{CAA} and t_{CAC}.
2. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) and t_{RAD} (max.) limit insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.) then the access time is controlled by t_{CAA} and t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
4. Assume $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
5. Measured with a load equivalent to two TTL loads and 100pF.
6. Assume $t_{RAD} \geq t_{RAD}$ (max.).
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
8. t_{WCS}, t_{RWD}, t_{AWD}, t_{CWD} are not restrictive operating parameters.
9. t_{WCS} (min.) must be satisfied in the early write cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$.
11. t_{HZ} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
12. Access time is determined by the longer of t_{CAA}, t_{CAC}, or t_{CAP}.
13. t_T is measured between V_{IH} (min.) and V_{IL} (max.) AC Measurements assume $t_T = 5$ ns.
14. Assume tri-state test load (5 pF and a 380 Ohm Thevenin equivalent)
15. At any given temperature and voltage combination, coincident deselection/selection is permissible for wired-OR devices.
16. An initial pause of 200μs is required after power-up and followed by a minimum of 8 initialization cycle (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only Refresh). 8 initialization cycles are required after extended period of bias without clocks.

CAPACITANCE

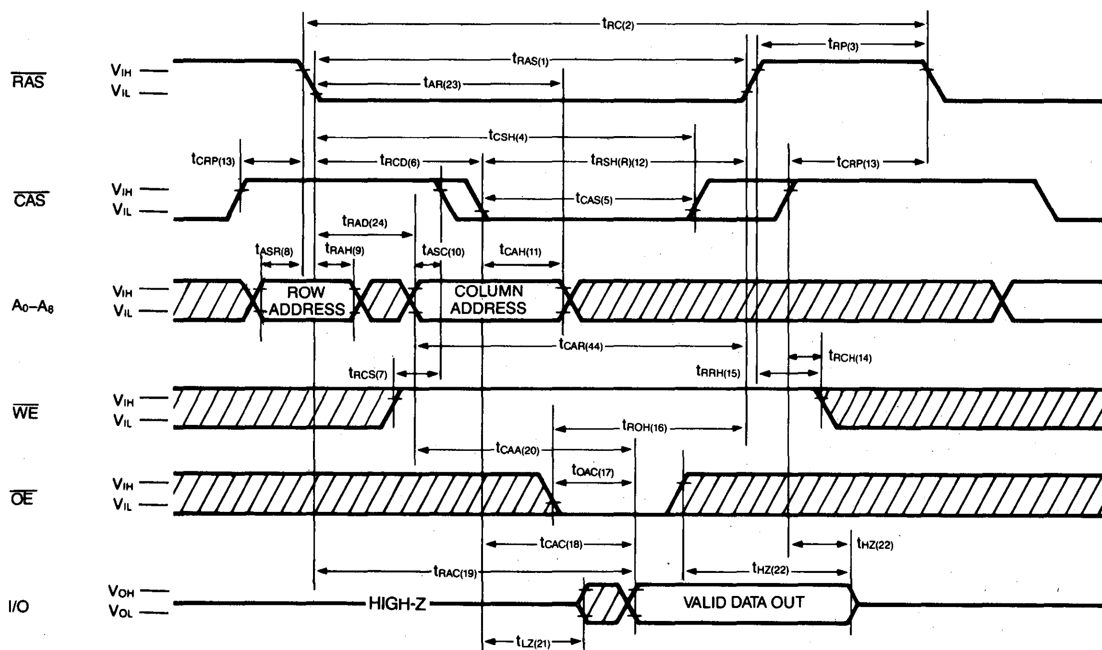
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, Data Input	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	—	8	pF
C_{OUT}	Data Output	—	8	pF

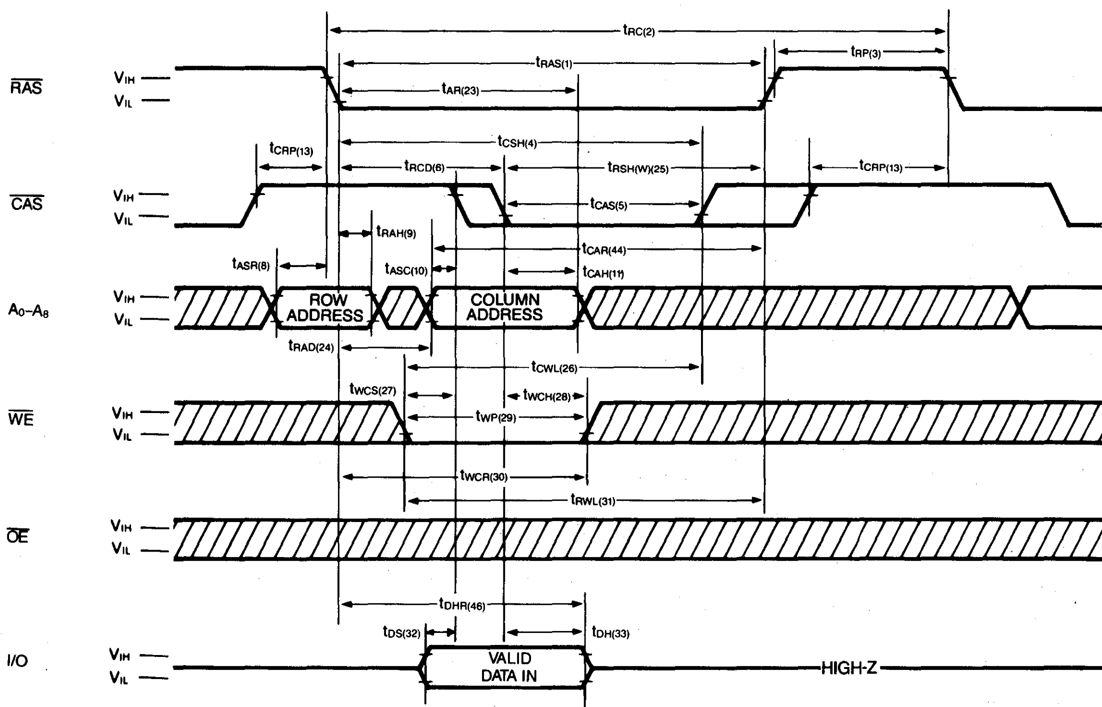
NOTE: Capacitance is measured at the worst case of voltage levels with a programmable capacitance meter.

TIMING DIAGRAMS

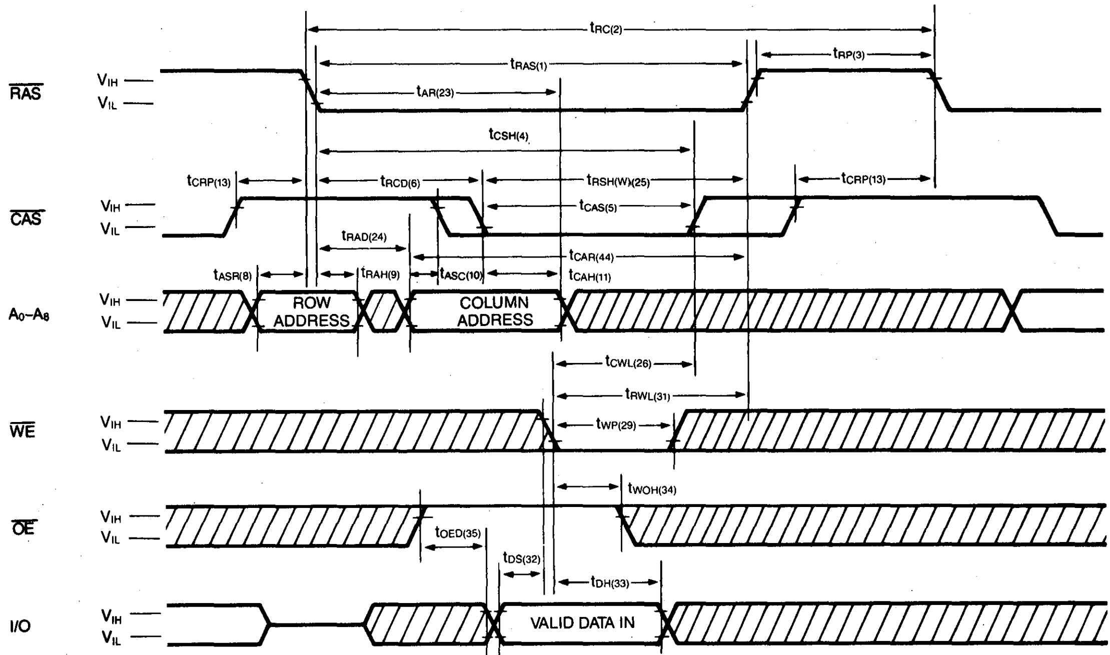
READ CYCLE



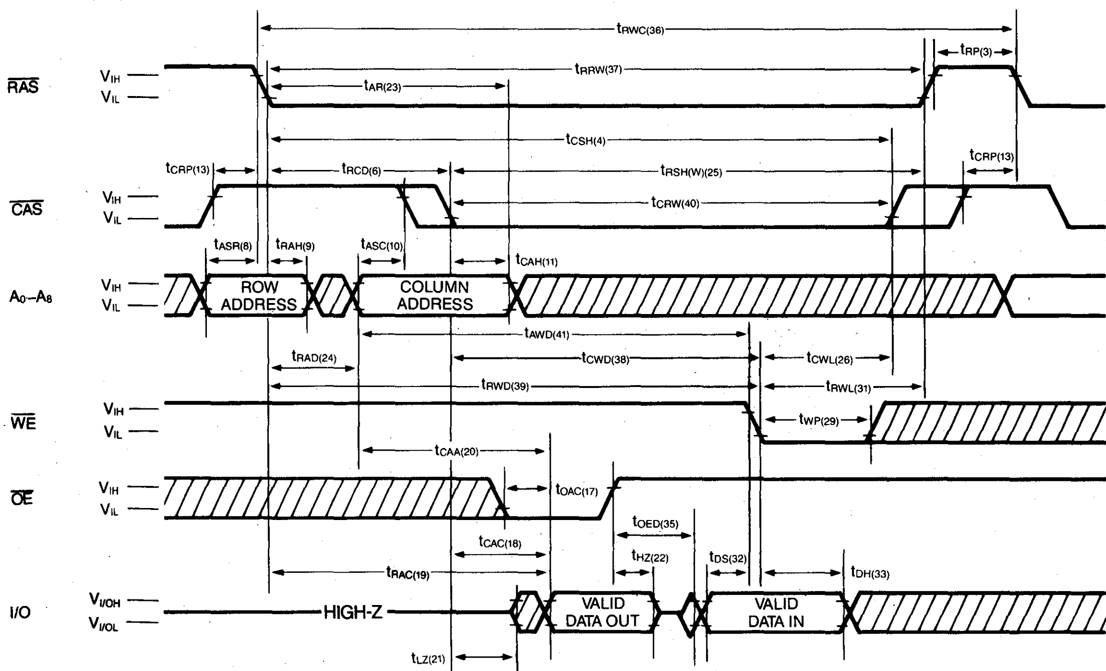
EARLY WRITE CYCLE



WRITE CYCLE (OE CONTROLLED)



READ-MODIFY-WRITE CYCLE



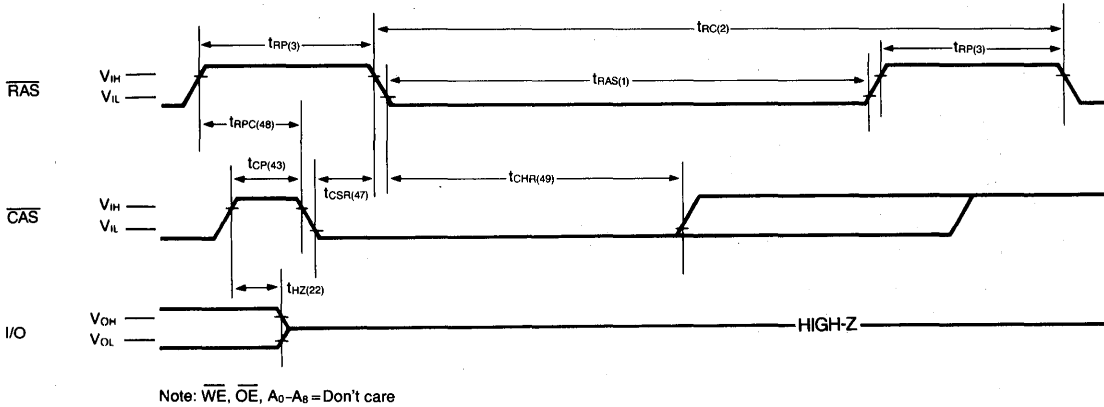
FAST PAGE MODE READ CYCLE

FAST PAGE MODE EARLY WRITE CYCLE

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

RAS-ONLY REFRESH CYCLE

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$, A_0–A_8 = Don't care

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

$\overline{RAS}$ VIH VIL tRAS(1) tRP(3)

$\overline{CAS}$ VIH VIL tCSR(47) tCHR(49) tCP(43) tRSH(W)(25) tCAS(5)

A_0–A_8 VIH VIL

READ CYCLE

tRCS(7) tRRH(15) tRCH(14)

$\overline{WE}$ VIH VIL

tROH(16) tOAC(17)

$\overline{OE}$ VIH VIL

tHZ(22) tLZ(21) tHZ(22)

I/O VOH VOL HIGH-Z VALID DATA OUT

WRITE CYCLE

tRWL(31) tCWL(26) tWCS(27) tWCH(28)

$\overline{WE}$ VIH VIL

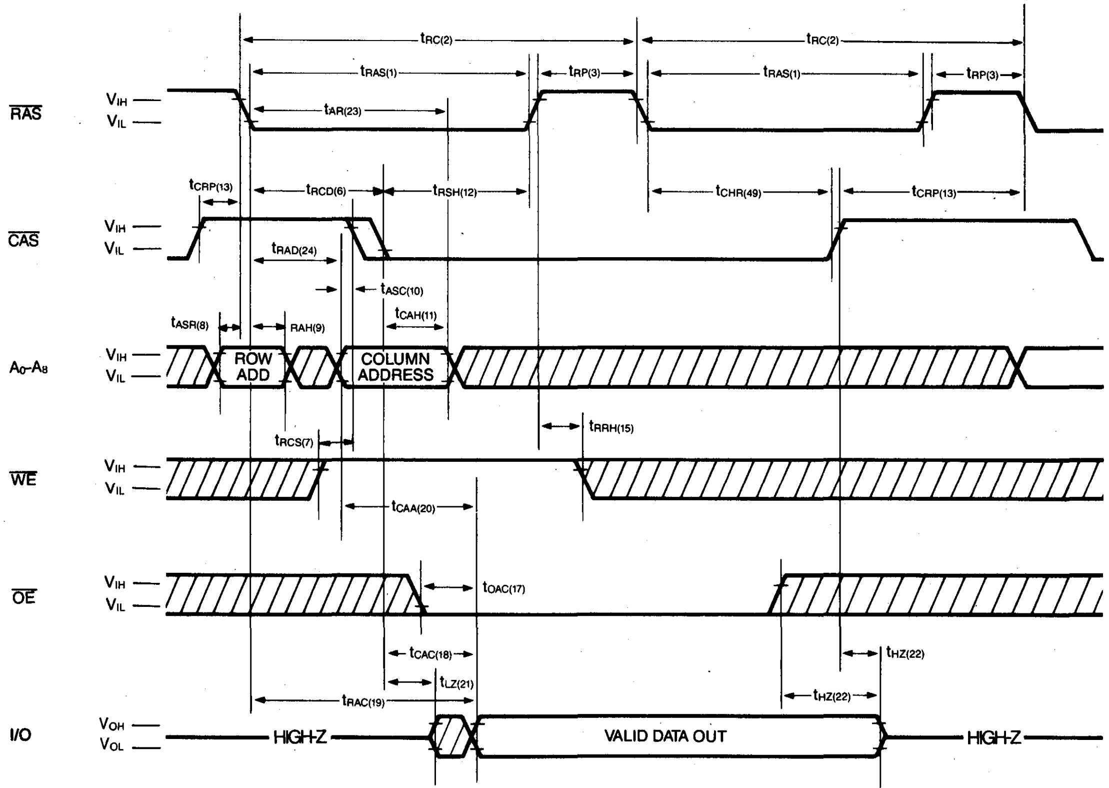
$\overline{OE}$ VIH VIL

tDS(32) tDH(33)

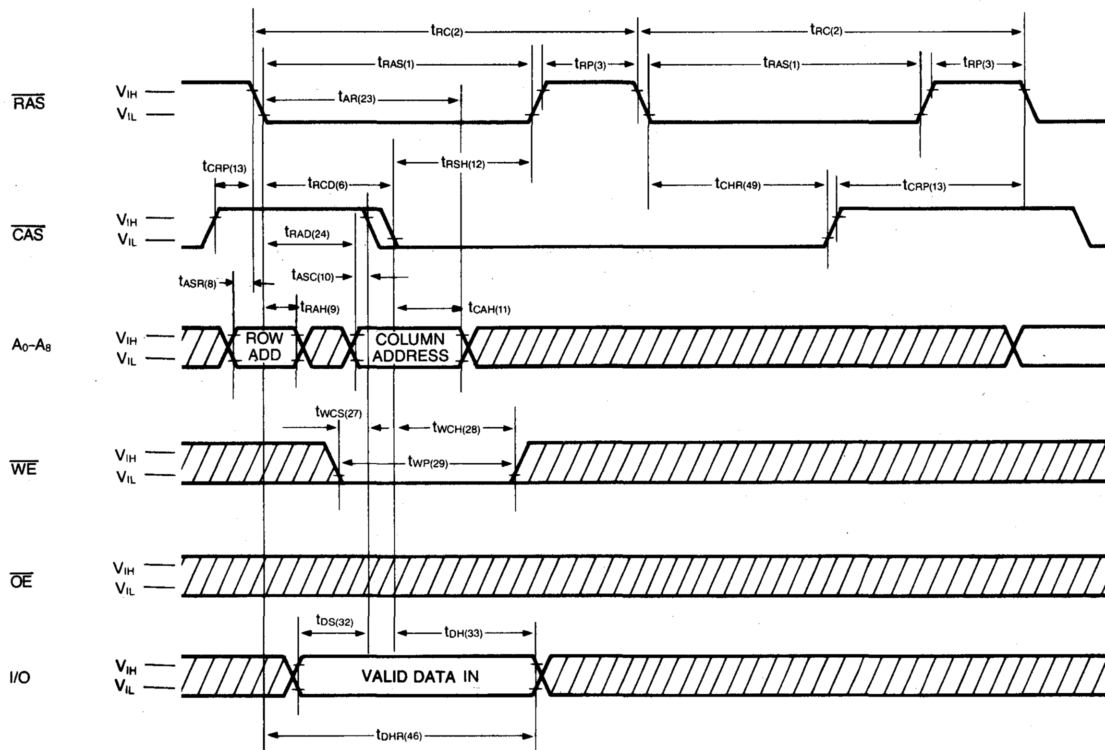
I/O VIH VIL HIGH-Z VALID DATA IN HIGH-Z

3

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



3

FUNCTIONAL DESCRIPTION

The HY51C4256 is a CMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The HY51C4256 reads and writes 4 bits of data at a time by multiplexing a 18 bit address into a 9 bit row and a 9 bit column address. The row address is latched by the Row Address Strobe($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

MEMORY CYCLE

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP}, and t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data out is controlled by the Out Enable($\overline{OE}$) and $\overline{CAS}$(See the write cycle description).

Data out becomes valid only when t_{RAC}, t_{CAA}, t_{OAC} and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC}, t_{OAC} and t_{CAC} are all satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ low during a $\overline{RAS}$ operation.

The column address is latched by $\overline{CAS}$, The input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Consequently, the write cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the latter of $\overline{WE}$ or $\overline{CAS}$ low transition. In a $\overline{CAS}$ controlled write cycle(the leading edge or $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition) the input/output (I/O) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{CAS}$ going high will maintain the I/O in the high impedance state, terminating with $\overline{WE}$ going high allows the output to go active, and $\overline{OE}$ must be brought high to allow for inputs on the I/O.

The HY51C4256 incorporates a self-timed write feature which simplifies the system interface and optimizes data bandwidth. After the write function has been initiated, the HY51C4256 internally completes the write action and unlatches the address and data latches. Thus, the latches are ready for the next input/output cycle. This eliminates the need for long address and data hold times during the write operation and allows a subsequent column address to be applied earlier. This minimizes a write pulse width, write precharge time, and hold time which provides maximum flexibility in system design.

REFRESH CYCLE

To retain data, 512 $\overline{RAS}$ refresh cycle are required in an 8 ms period. The refresh operation can be performed two ways :

1. Clocking each of 512 row address(A_0 through A_8) with $\overline{RAS}$ at least every 8 ms period. Any combination of $\overline{RAS}$ cycles such as read, write, read-modify-write, or $\overline{RAS}$-Only refresh cycle will perform refresh.
2. $\overline{CAS}$-Before-$\overline{RAS}$ refresh cycle : If $\overline{CAS}$ go low prior to $\overline{RAS}$ go low, the chip enters $\overline{CAS}$-Before-$\overline{RAS}$ refresh cycle. The HY51C4256 will use an internal nine bits counter output as the source of the row address and will ignore the external address inputs.

This $\overline{CAS}$-Before-$\overline{RAS}$ refresh mode is a refresh only mode and no data access is allowed. Also, the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle does

not cause device selection and the state of the Data Output pin will remain in a high impedence state.

In order to guarantee the reliable operation of $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, an internal counter test mode is provided. The user can use the counter test mode to write in a data pattern consecutively (512 write cycles) and, then verify the data which have been written by 512 consecutive read cycle.

DATA RETENTION MODE

The HY51C4256 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY51C4256 power consumption is reduced to the low I_{DD5} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows :

$$I=\frac{(t_{RC})\times(I\ active)+(t_{RX}-t_{RC})\times(I_{DD5})}{t_{RX}}$$

Where t_{RC}=Refersh Cycle Time
t_{RX}=Refresh Interval/512

FAST PAGE MODE OPERATION

Fast page mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while successive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as transparent or flow through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into column address buffer and acts as an output enable.

During this operation, read, write, and read-modify-write, or read-write-read cycles are possible at random or sequential address within a row. Following the entry cycle into fast page mode access time is t_{CAA} or t_{CAP} dependent. If the column adderess is valid prior to or coincident with the rising edge of $\overline{CAS}$, then the access time is determined by the rising edge of $\overline{CAS}$ specified by t_{CAP} as shown in figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{CAA}. For both cases, the falling edge of $\overline{CAS}$ latches the address and enable the output.

Fast page mode provides a sustanined data rate over 20 MHz for applications that require high data rate such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate :

$$\text{Data Rate}=\frac{512}{t_{RC}+511\times t_{PC}}$$

DATA OUT OPERATION

The HY51C4256 input/output(I/O) is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables data to transfer into and from a selected row address. A $\overline{RAS}$ high transition disables data transfer and will latch the output data if the output is enabled. After a memory cycle is initiated by a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or a $\overline{CAS}$ low level enables the internal I/O data path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O data path and disables the output driver if the driver was enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path, nor on the output driver.

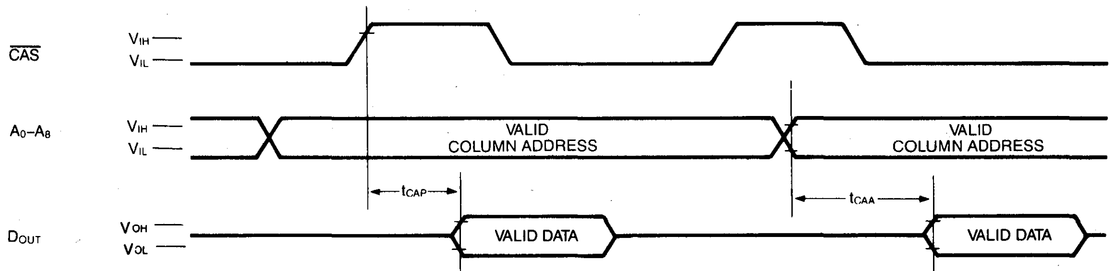
An $\overline{OE}$ low transiton or an $\overline{OE}$ low level enables the output driver when the I/O data path is enabled. An $\overline{OE}$ high transition or an $\overline{OE}$ high level disables the output driver, but does not disable the data latch when it has been enabled. A $\overline{WE}$ low level disables the output driver when a $\overline{CAS}$ low level occurs. If the $\overline{WE}$ low transition occurs after the $\overline{CAS}$ low transition such that the output driver is enable prior to the $\overline{WE}$ low transition, it is necessary to use $\overline{OE}$ to disable the output driver prior to the $\overline{WE}$ low transition to allow data in set-up time(t_{DS}). A $\overline{WE}$ high transition passes control of the output drive to $\overline{OE}$.

POWER ON

An initial pause of 200 μs is required after the application of the V_{DD} supply, followed by a minimum of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

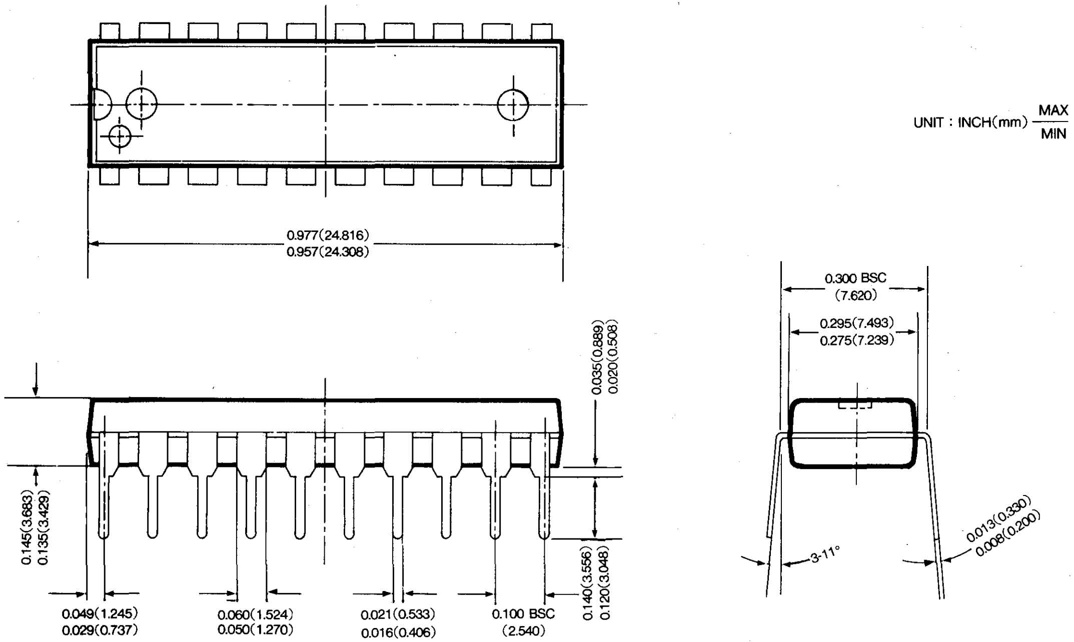
The V_{DD} current (I_{DD}) requirement of the HY 51C4256 during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS} = V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.

FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION

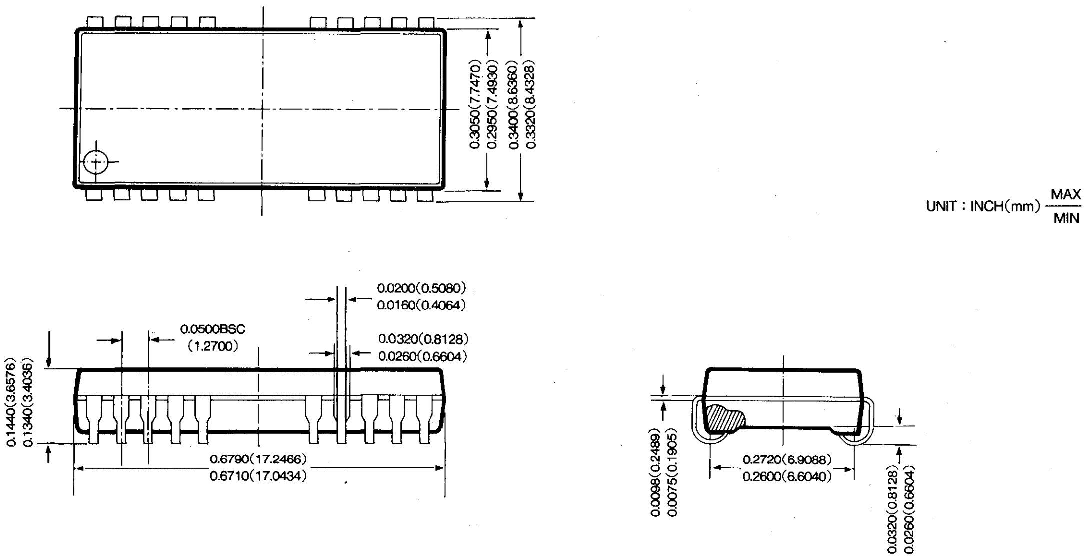


PACKAGE INFORMATION

• 20 PIN PLASTIC DUAL IN LINE PACKAGE – 300 MIL



• 20/26 PIN SMALL OUTLINE J-FORM PACKAGE –300 MIL



MEMO

DESCRIPTION

The HY531000 is a high speed, low power 1,048,576×1 bit CMOS dynamic random access memory. Fabricated with the HYUNDAI CMOS process, the HY531000 offers a fast page mode for high bandwidth operation, fast usable speed, CMOS standby current, and inherently high CMOS reliability.

All inputs and output are TTL compatible. Fast page mode operation allows random or sequential access of up to 1,024 bits within a row with cycle times as fast as 40ns.

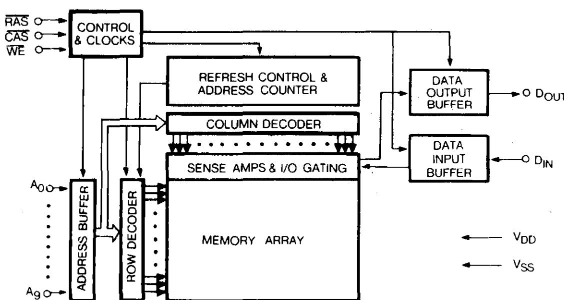
The HY531000 design is optimized for cache based mainframe and minicomputers, graphics, digital signal processing, and high performance microprocessor systems.

FEATURES

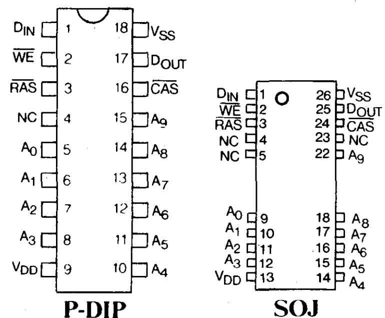
- Low power dissipation
  - Operating Current, 100ns : 55mA(max.)
  - TTL Standby Current : 2mA(max.)
  - CMOS Standby Current : 1mA(max.)
- Read-Modify-Write Capability
- $\overline{RAS}$-only, Hidden, $\overline{CAS}$-before-$\overline{RAS}$ Refresh Capability
- Common I/O capability
- Fast Page mode operation for a sustained data rate up to 25 MHz
- 512 refresh cycles/8 ms
- High reliability 300 mil 18 pin P-DIP and 20/26 pin SOJ
- Fast access time and cycle time (ns)

	HY531000-60	HY531000-70	HY531000-80	HY531000-10
Max $\overline{RAS}$ Access Time, t_{RAC}	60	70	80	100
Max $\overline{CAS}$ Access Time, t_{CAC}	20	20	20	25
Min Fast Page Mode Cycle Time, t_{PC}	40	40	45	55
Min Cycle Time, t_{RC}	120	130	150	180

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0-A_9	ADDRESS INPUT
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	−55 to 150	°C
V_{TERM}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	0.6	W

NOTE : Stress above those listed under "Absolute Maximum Rating" might cause permanent damage to the device.

DC CHARACTERISTICS

(T_A=0 ℃ to 70 ℃, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY531000		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$			10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60	–	85	mA	1, 2
			−70	–	75		
			−80	–	65		
			−10	–	55		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}		–	2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60	–	85	mA	2
			−70	–	75		
			−80	–	65		
			−10	–	55		
I_{DD4}	V_{DD} Supply Current, Fast page mode	Minimum Cycle	−60	–	65	mA	1, 2
			−70	–	55		
			−80	–	45		
			−10	–	35		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs≥V_{SS}		–	1	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60	–	85	mA	2
			−70	–	75		
			−80	–	65		
			−10	–	55		
V_{IL}	Input Low Voltage(all inputs)			−1	0.8	V	
V_{IH}	Input High Voltage(all inputs)			2.4	V_{DD}+1	V	
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD}(max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in Fast page mode.

AC CHARACTERISTICS

(T_A=0 °C to 70 °C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY531000								UNIT	NOTE
			60		70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	180	–	ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	50	–	60	–	70	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	15	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	50	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Tme	15	30	15	35	15	40	20	50	ns	1
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	20	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	60	25	75	ns	2
11	t_{RAC}	Access Time From $\overline{RAS}$	–	60	–	70	–	80	–	100	ns	3,4,5
12	t_{AA}	Access Time From Column Address	–	30	–	35	–	40	–	50	ns	5,7
13	t_{CAC}	Access Time From $\overline{CAS}$	–	20	–	20	–	20	–	25	ns	5,6
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	20	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	20	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	0	–	ns	8
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	0	–	ns	8
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	5	–	ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	0	20	ns	9
21	t_{OH}	Output Data Hold Time From $\overline{CAS}$	0	–	0	–	0	–	0	–	ns	9
22	t_{WP}	Write Pulse Width	15	–	15	–	15	–	20	–	ns	
23	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	10	–	ns	
24	t_{AR}	Column Address Hold Time From $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
25	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
26	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	0	–	ns	10
27	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	20	–	ns	
28	t_{DS}	Data-In Set-up Time	0	–	0	–	0	–	0	–	ns	11
29	t_{DH}	Data-In Hold Time	15	–	15	–	15	–	20	–	ns	11
30	t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
31	t_{RWC}	RMW Cycle Time	145	–	155	–	175	–	210	–	ns	
32	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in RMW Cycle	60	–	70	–	80	–	100	–	ns	10
33	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	20	–	20	–	20	–	25	–	ns	10
34	t_{AWD}	Column Address to $\overline{WE}$ Delay	30	–	35	–	40	–	50	–	ns	10
35	t_{CPA}	Access Time From $\overline{CAS}$ precharge	–	35	–	35	–	40	–	50	ns	5,12

#	SYMBOL	PARAMETER	HY531000								UNIT	NOTE
			60		70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t_{PC}	Fast page mode Read or Write Cycle time	40	–	40	–	45	–	55	–	ns	
37	t_{PCM}	Fast page mode Read-Modify-Write Cycle	65	–	65	–	70	–	85	–	ns	
38	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
39	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	20	–	25	–	ns	
40	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	0	–	ns	
41	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	5	–	ns	
42	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	20	–	ns	
43	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	100	–	ns	
44	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	3	50	ns	13,14
45	t_{CLZ}	$\overline{CAS}$ to output in Low-Z	0	–	0	–	0	–	0	–	ns	5
46	t_{REF}	Refresh Interval(512 Cycle)	–	8	–	8	–	8	–	8	ms	15
47	t_{RASP}	$\overline{RAS}$ Pulse Width Fast Page Mode	60	100K	70	100K	80	100K	100	100K	ns	
48	t_{CPT}	$\overline{CAS}$ Precharge Time (CBR Counter Test Cycle)	40	–	40	–	40	–	50	–	ns	

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA}.
2. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a referenced point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then the access time is controlled by t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.). If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.).
4. Assume $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.).
5. Measured with a load equivalent to two TTL loads and 100 pF.
6. Assumes that $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.)
7. Assumes that $t_{RCD} \leq t_{RCD}$(max.) and $t_{RAD} \geq t_{RAD}$(max.)
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{OFF} and t_{OH} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle ; if $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), the cycle is a read/write and the data output will contain data from the selected cell : if neither of the above sets of conditions is satisfied, the condition of the data out (at access time)is indeterminate.
11. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$
12. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{CPA}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max.).
14. AC measurements assume t_T=5ns.
15. An initial pause of 200μs is required after power-up and followed by a minimum of 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

CAPACITANCE

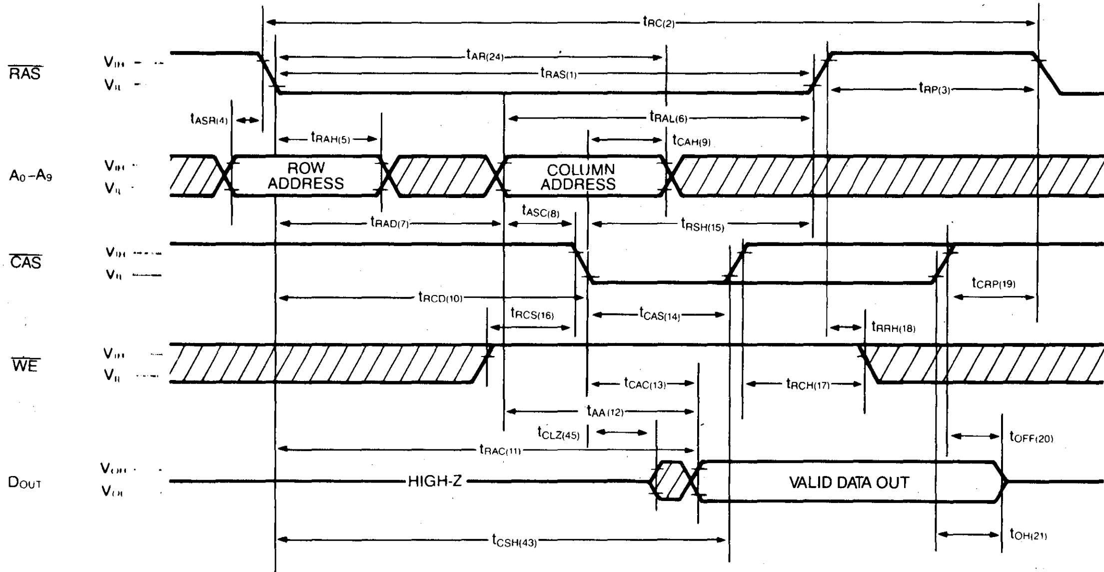
(T_A=25 ℃, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, Data In	–	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	–	7	pF
C_{OUT}	Data Out	–	7	pF

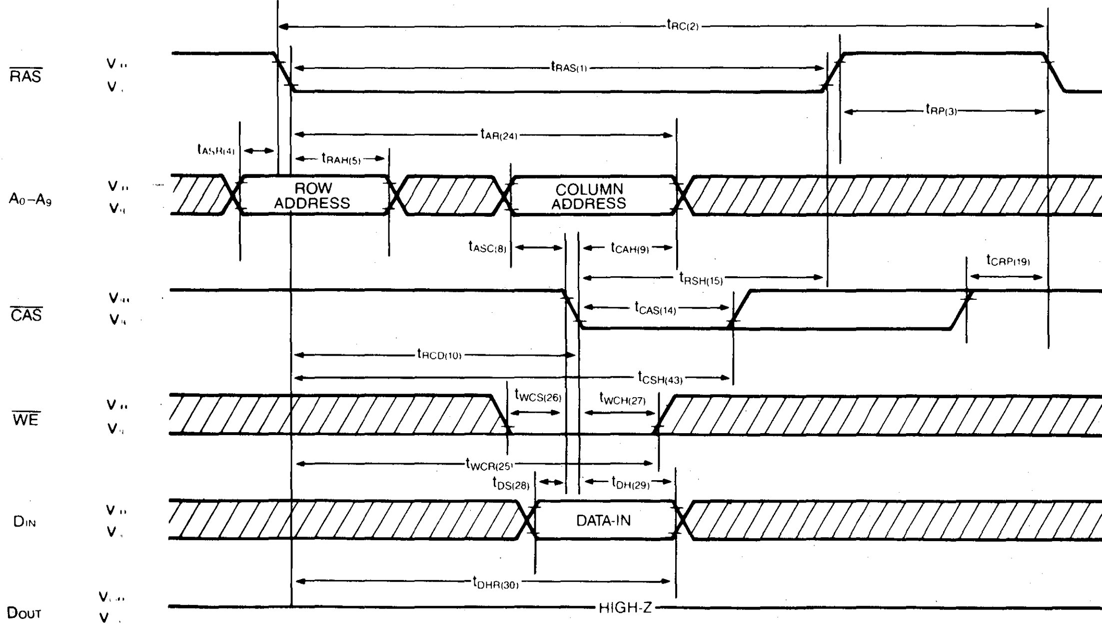
NOTE : Capacitance is measured at worst case of voltage levels with a programmable capacitance meter.

TIMING DIAGRAM

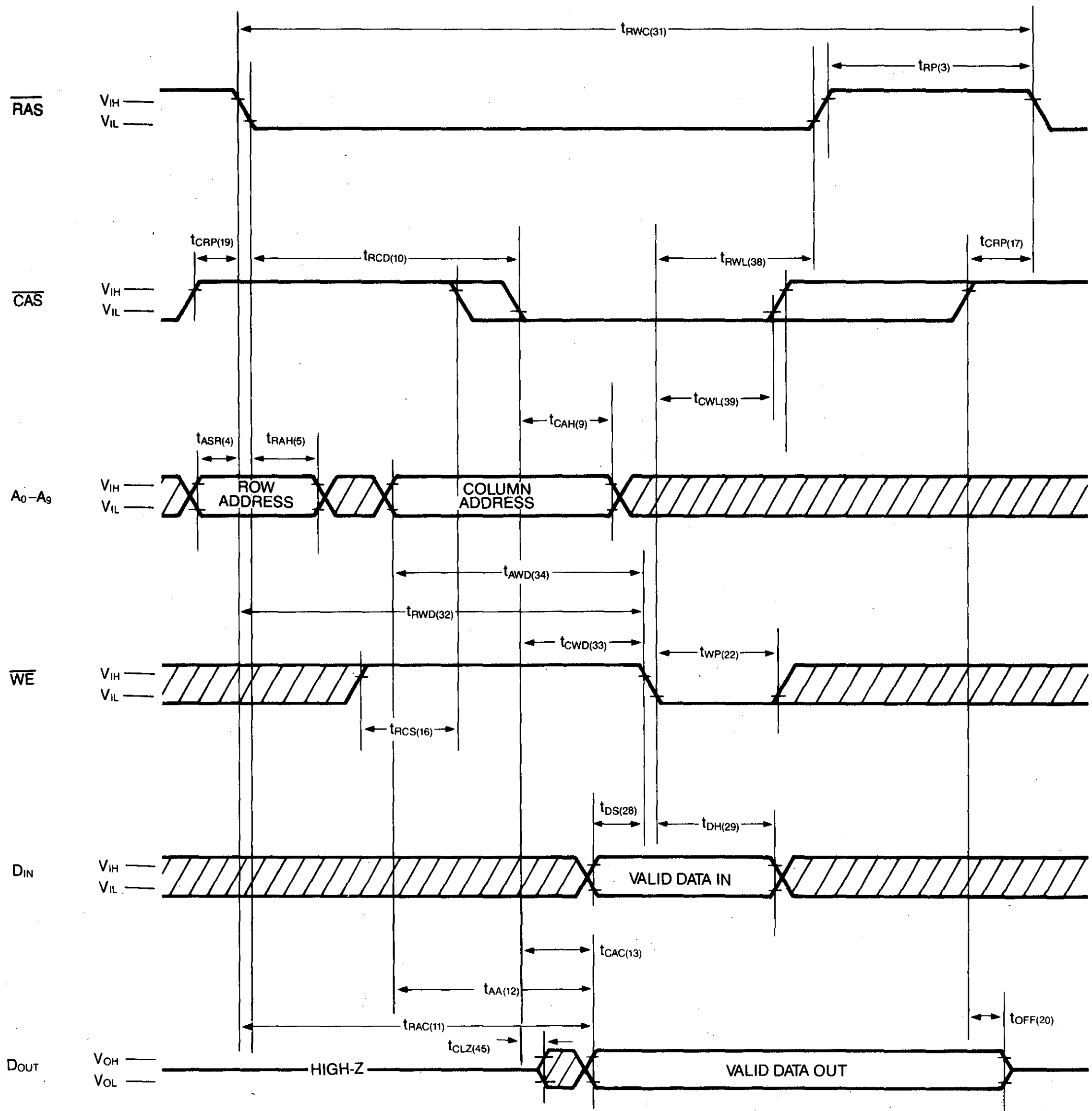
READ CYCLE



EARLY WRITE CYCLE



READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

RAS V_{IH} V_{IL}
CAS V_{IH} V_{IL}
A_0–A_9 V_{IH} V_{IL} ROW ADD COL ADD COL ADD COL ADD
WE V_{IH} V_{IL}
DOUT V_{OH} V_{OL} HIGH-Z VALID DATA VALID DATA VALID DATA HIGH-Z

$t_{RASP(47)}$ $t_{RP(3)}$ $t_{RAL(6)}$ $t_{CRP(19)}$ $t_{CSH(43)}$ $t_{PC(36)}$ $t_{RSH(15)}$ $t_{CP(23)}$ $t_{RCD(10)}$ $t_{CAS(14)}$ $t_{CAH(9)}$ $t_{RAH(5)}$ $t_{ASR(4)}$ $t_{ASC(8)}$ $t_{RCS(16)}$ $t_{RRH(18)}$ $t_{RCH(17)}$ $t_{CAC(13)}$ $t_{AA(12)}$ $t_{RAC(11)}$ $t_{CAP(35)}$ $t_{CLZ(45)}$ $t_{OFF(20)}$

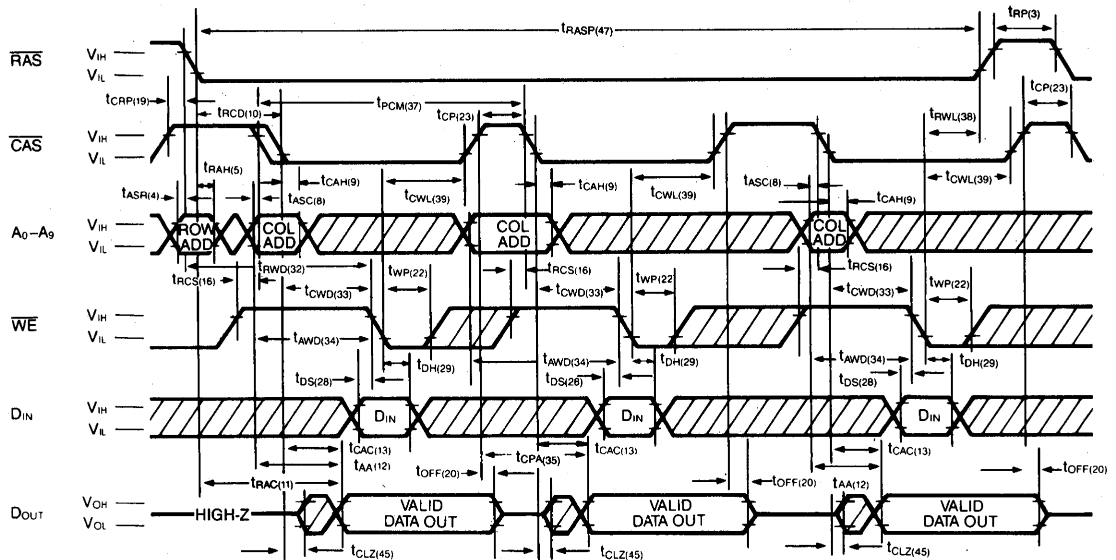
FAST PAGE MODE EARLY WRITE CYCLE

RAS V_{IH} V_{IL}
CAS V_{IH} V_{IL}
A_0–A_9 V_{IH} V_{IL} ROW ADD COL ADD COL ADD COL ADD
WE V_{IH} V_{IL}
DIN V_{IH} V_{IL} VALID DATA IN VALID DATA IN VALID DATA IN

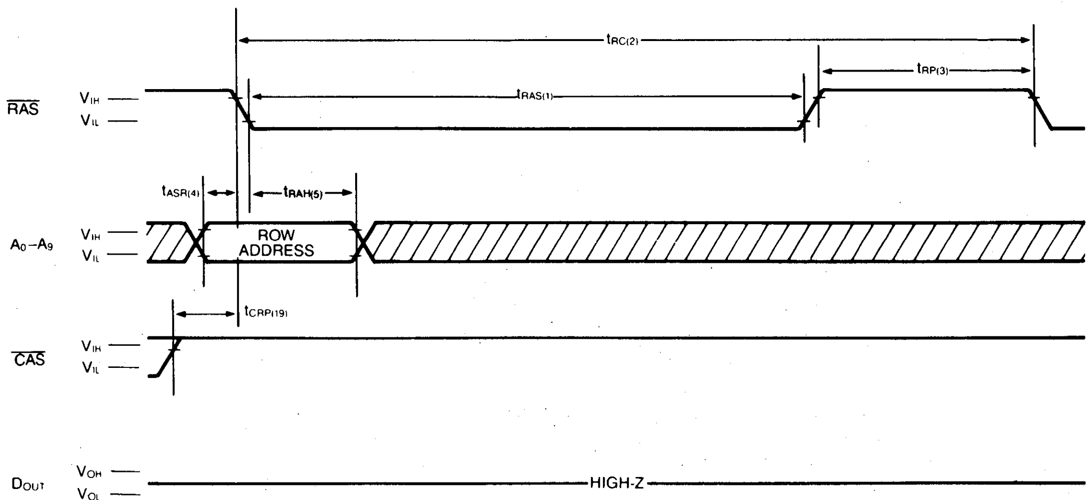
$t_{RASP(47)}$ $t_{RP(3)}$ $t_{CSH(43)}$ $t_{CRP(19)}$ $t_{PC(36)}$ $t_{RCD(10)}$ $t_{CAS(14)}$ $t_{RAH(5)}$ $t_{CP(23)}$ $t_{CAH(9)}$ $t_{ASR(4)}$ $t_{ASC(8)}$ $t_{WCH(27)}$ $t_{WCS(26)}$ $t_{CWL(39)}$ $t_{WP(22)}$ $t_{RWL(38)}$ $t_{DS(28)}$ $t_{DH(29)}$

3

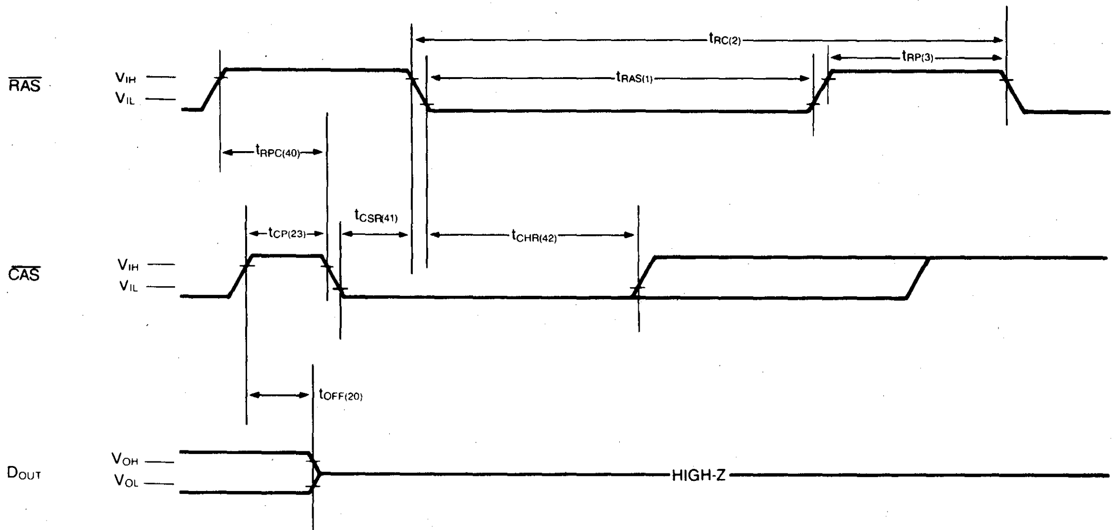
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



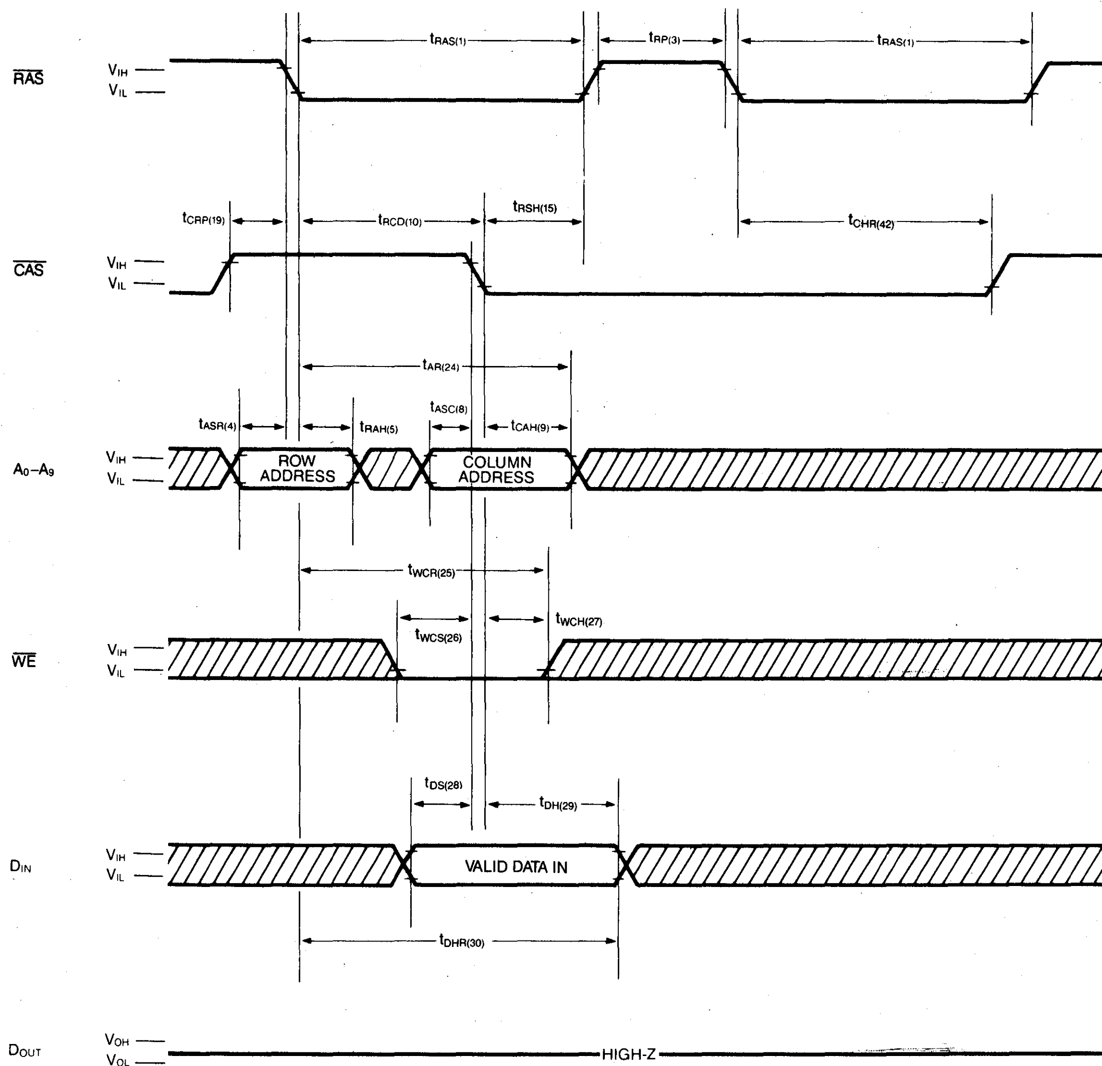
Note: $\overline{WE}$, A_0–A_9 = Don't care

HIDDEN REFRESH CYCLE (READ)

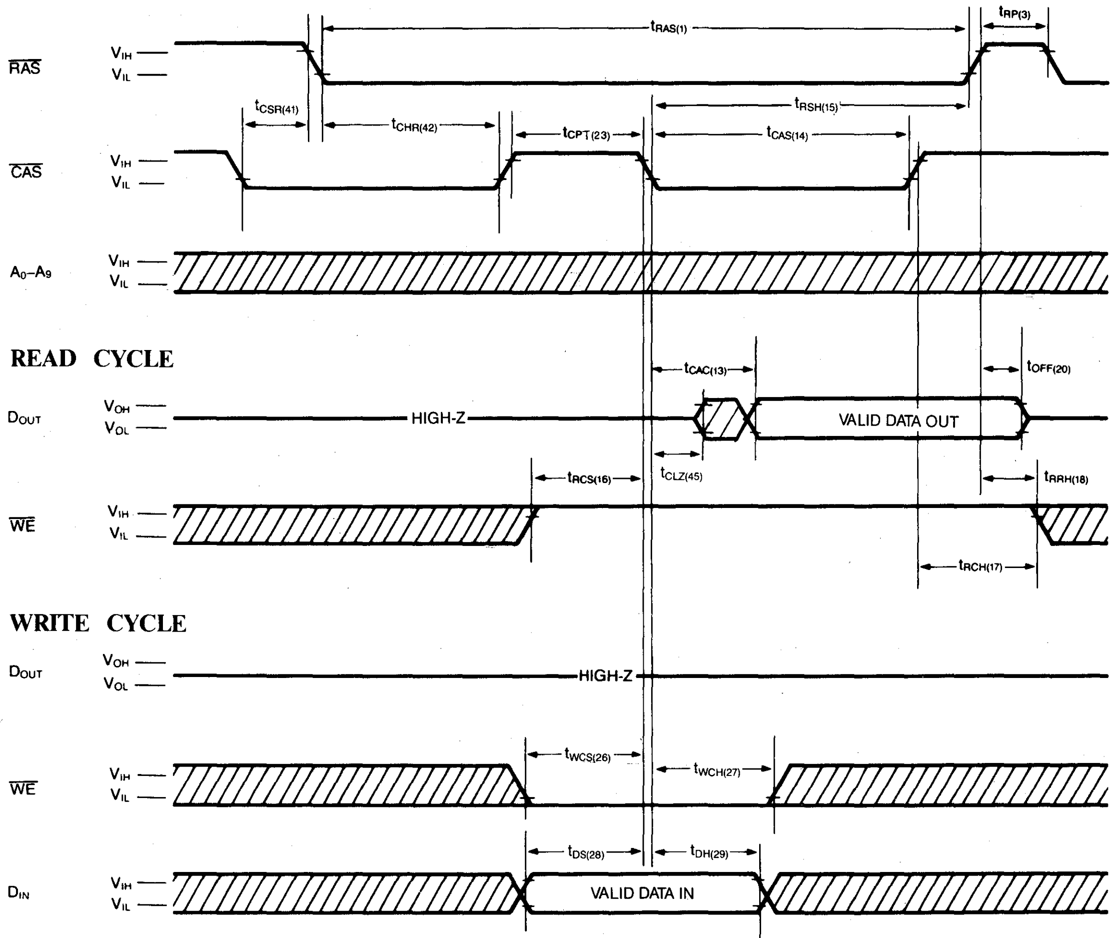
RAS VIH VIL
tRAS(1) tRP(3) tRAS(1)
tCRP(19) tRCD(10) tRSH(15) tCHR(42)
CAS VIH VIL
tASC(8) tRAL(6) tRAD(7)
tASR(4) tRAH(5) tCAH(9)
A0–A9 VIH VIL ROW ADDRESS COLUMN ADDRESS
tAR(24)
tRCS(16) tRRH(18)
WE VIH VIL
tCAC(13)
tAA(12)
tRAC(11) tOFF(20)
DOUT VOH VOL HIGH-Z VALID DATA OUT
tCLZ(45)

3

HIDDEN REFRESH CYCLE (WRITE)



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

The HY531000 is a CMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The HY531000 reads and writes data by multiplexing 20 bit address into 10 bit row and 10 bit column address. The row address is latched by Row Address Strobe ($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

MEMORY CYCLE

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle can not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by holding the Write Enable($\overline{WE}$) signal high during a $\overline{RAS}$ /$\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data output becomes valid only when t_{RAC}, t_{CAC}, and t_{AA} are all satisfied. Consequently, the access time is dependent upon the timing relationship among the t_{RAC}, t_{CAC} and t_{AA}. For example, the access time is limited by t_{AA} when t_{RAC} and t_{CAC} are both satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the latter of $\overline{WE}$ or $\overline{CAS}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$ controlled write cycle (the leading edge of $\overline{WE}$ occurs priors to or coincident with the $\overline{CAS}$ low transition)the output(D_{OUT}) pin will be in the high impedance state at the beginning of the write function.

Terminating the write action with $\overline{RAS}$ or $\overline{CAS}$ going high will maintain the data output (D_{OUT}) in the high impedance state.

REFRESH CYCLE

To retain data, 512 $\overline{RAS}$ refresh cycles are required in an 8 ms period. The refresh operation can be performed two ways :

1. Clocking each of 512 row address(A_0 through A_8) with $\overline{RAS}$ at least every 8 ms period. Any combination of $\overline{RAS}$ cycle such as read, write, read-modify-write, or $\overline{RAS}$-only refresh cycle will perform a refresh on the selected row.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle : If $\overline{CAS}$ go low prior to $\overline{RAS}$ go low, the chip enters a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. In $\overline{CAS}$ -before-$\overline{RAS}$ refresh cycle the HY531000 will use an internal nine-bit counter output as the source of the row address and will ignore the external address input.

This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh only mode and no data access is allowed. Also, The $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle does not cause device selection and the state of the data output pin will remain in a high impedance state.

In order to guarantee the reliable operation of the $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, a internal counter test mode is provided. The user can use the counter test mode to write in a data pattern consecutively(512 write cycles) and then verify the data which has been written by 512 consecutive read cycles.

The HY531000 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY531000 power consumption is reduced to the low I_{DDS} level. Overall I_{DD} consumption when operating

in this mode can be calculated as follows :

$$I = \frac{(t_{RC}) \times (I\ active) + (t_{RX} - t_{RC}) \times (I_{DD5})}{t_{RX}}$$

Where t_{RC}=Refresh Cycle Time
t_{RX}=Refresh Interval/512

FAST PAGE MODE OPERATION

Fast page mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while sucessive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent or flow through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latch the address into column address buffer and acts as an output enable.

During this operation, read, write, and read-modify-write, or read-write-read cycles are possible at random or sequential address within a row. Following the entry cycle into fast page mode, access time is t_{AA} or t_{CAP} dependent. If the column address is valid prior to or coincident by t_{CAP} as shown in figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{AA}. For both cases, the falling edge of $\overline{CAS}$ latches the address and enable the output.

Fast page mode provides a sustained data rate over 25 MHz for applications that require high data rates, such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate :

$$\text{Data Rate} = \frac{1024}{t_{RC} + 1023 \times t_{PC}}$$

DATA RETENTION MODE

The HY531000 data output (D_{OUT}), which has tri-state capability, is controlled by $\overline{CAS}$. During a $\overline{CAS}$ the high state ($\overline{CAS}$ at V_{IH}), the data output is in the high impedance state. The following table summarize the D_{OUT} state for various types of cycles.

CYCLE	D_{OUT} STATE
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$ Controlled Write Cycle (Early Write)	High Impedance
$\overline{WE}$ Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High Impedance
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-Only Refresh Cycle	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle	Data remain the previous cycle's state (high impedance or low impedance)
$\overline{CAS}$-Only Cycle	High Impedance

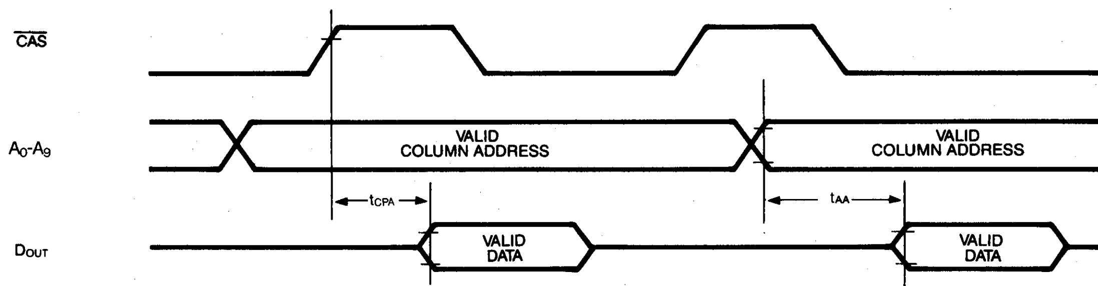
POWER ON

An initial pause of 200 μs is required after the application of V_{DD} power supply, followed by a minimum of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh cycle). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

The V_{DD} current (I_{DD}) requirement of the HY531000 during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}=V_{SS}$ during power on, the device will go into an active and I_{DD} will exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} level during power on.

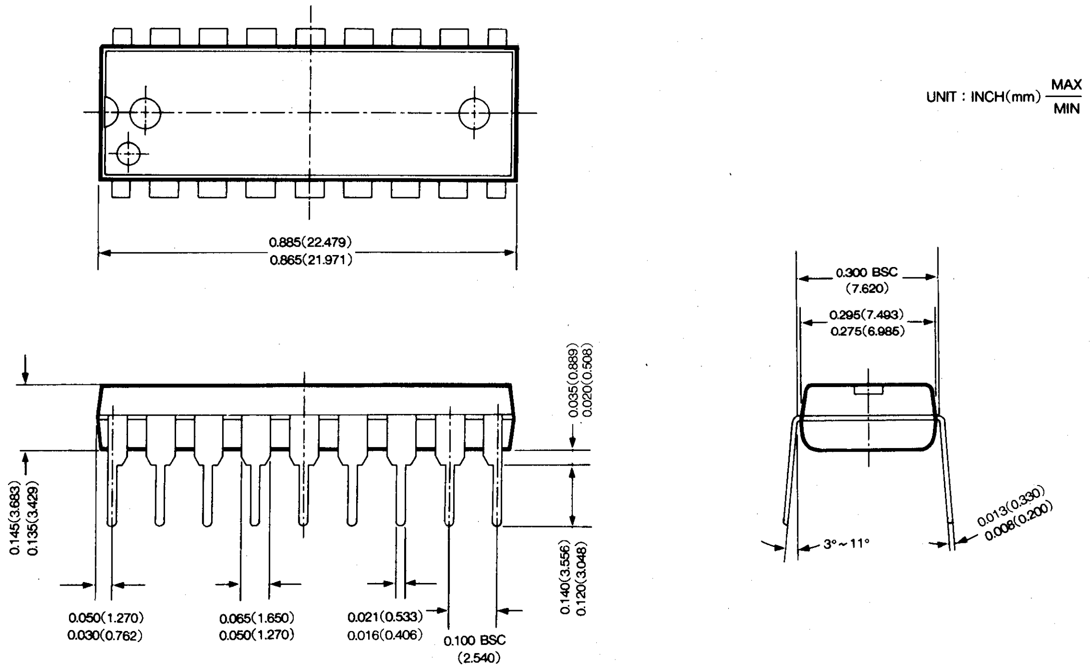
3

FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION

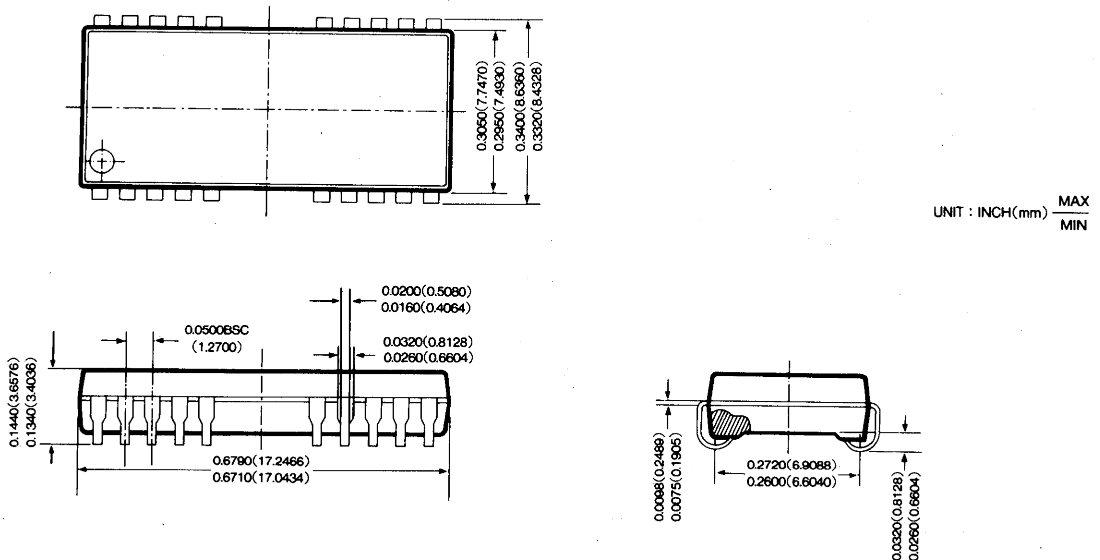


PACKAGE INFORMATION

- **18 PIN PLASTIC DUAL IN LINE PACKAGE − 300 MIL**



- **20/26 PIN SMALL OUTLINE J-FORM PACKAGE −330 MIL**



MEMO

PRELIMINARY

•HYUNDAI SEMICONDUCTOR

HY531000A

1M×1-Bit CMOS DRAM

M1E1200A-JAN92

DESCRIPTION

The HY531000A is a high speed, low power 1,048,576×1 bit CMOS dynamic random access memory. Fabricated with the HYUNDAI CMOS process, the HY531000A offers a fast page mode for high bandwidth fast usable speed, CMOS standby current and inherently high CMOS reliability.

All inputs and outputs are TTL compatible. Fast page mode operation allows random or sequential access of up to 1,024 bits within a row with cycle times as fast as 40ns.

The HY531000A design is optimized for cache based mainframe, minicomputers, graphics, digital signal processing and high performance microprocessor systems.

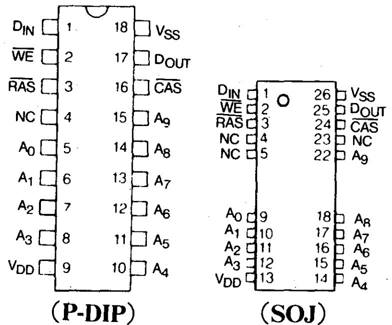
FEATURES

- Low power dissipation for The HY531000A
  - Operating Current, 60ns : 85mA(max.)
  - TTL Standby Current : 2mA(max.)
  - CMOS Standby Current : 1mA(max.)

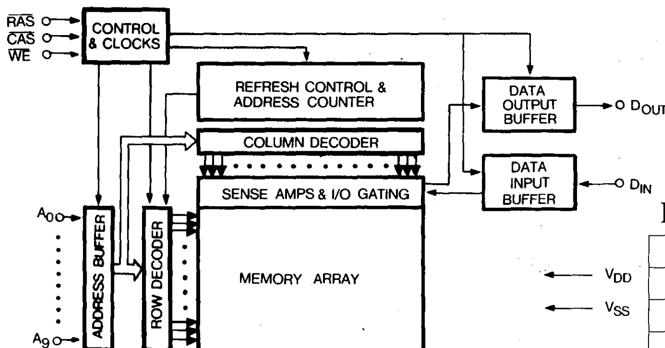
  Read-Modify-Write Capability
- $\overline{RAS}$-only, Hidden, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Capability
- Common I/O capability
- Fast Page mode operation for a sustained data rate up to 25 MHz
- 512 refresh cycles/8ms
- High reliability 300 mil P-DIP, 18 pin 20/26 pin SOJ and 400 mil ZIP
- Fast access time and cycle time (ns)

	HY531000A-60	HY531000A-70	HY531000A-80
Max $\overline{RAS}$ Access Time, t_{RAC}	60	70	80
Max $\overline{CAS}$ Access Time, t_{CAC}	20	20	20
Min Fast Page Mode Cycle Time, t_{PC}	40	40	45
Min Cycle Time, t_{RC}	110	130	150

PIN CONNECTIONS

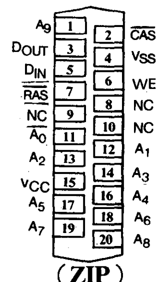


BLOCK DIAGRAM



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0-A_9	ADDRESS INPUT
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_{BIAS}	Ambient Temperature Under Bias	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to +150	℃
V_{TERM}	Voltage on Any Pin Except V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Data Out Current	50	mA
P_T	Power Dissipation	0.6	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY531000A		UNIT	NOTE
				MIN.	MAX.		
$\vert I_{LI}\vert$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$			10	μA	
$\vert I_{LO}\vert$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10		
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60		85		1, 2
			−70		75		
			−80		65		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs$\ge V_{SS}$			2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60		85	mA	2
			−70		75		
			−80		65		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−60		70	mA	1, 2
			−70		55		
			−80		45		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD}-0.2V$, $\overline{CAS}=V_{IH}$, other inputs$\ge V_{SS}$			1	mA	1, 2
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60		85	mA	2
			−70		75		
			−80		65		
V_{IL}	Input Low Voltage(all inputs)			−1	0.8	V	
V_{IH}	Input High Voltage(all inputs)			2.4	$V_{DD}+1$	V	
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD}(max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions, Specified I_{DD}(max.) is measured with a maximum of of two transitions per address cycle in Fast page mode.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY531000A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	110		130		150		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	40		50		60		ns	
4	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
5	t_{RAH}	Row Address Hold Time	10		10		10		ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	1
8	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
9	t_{CAH}	Column Address Hold Time	15		15		15		ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	60	ns	2
11	t_{RAC}	Access Time From $\overline{RAS}$		60		70		80	ns	3, 4, 5
12	t_{AA}	Access Time From Column Address		30		35		40	ns	5, 6, 12
13	t_{CAC}	Access Time From $\overline{CAS}$		20		20		20	ns	6, 12
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	20	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20		20		20		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	7
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	7
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	ns	8
21	t_{OH}	Output Data Hold Time From $\overline{CAS}$	0		0		0		ns	8
22	t_{WP}	Write Pulse Width	15		15		15		ns	
23	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
24	t_{AR}	Column Address Hold Time From $\overline{RAS}$	50		55		60		ns	
25	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	50		55		60		ns	
26	t_{WCS}	Write Command Set-up Time	0		0		0		ns	9, 10
27	t_{WCH}	Write Command Hold Time	15		15		15		ns	
28	t_{DS}	DAta-In Set-up Time	0		0		0		ns	11
29	t_{DH}	Data-In Hold Time	15		15		15		ns	11
30	t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	50		55		60		ns	
31	t_{RWC}	RMW Cycle Time	135		155		175		ns	
32	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in RMW Cycle	60		70		80		ns	9
33	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	20		20		20		ns	9
34	t_{AWD}	Column Address to $\overline{WE}$ Delay	30		35		40		ns	9
35	t_{CAP}	Access Time From $\overline{CAS}$ precharge		35		35		40	ns	12

#	SYMBOL	PARAMETER	HY53100A-60		HY53100A-70		HY53100A-80		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t_{PC}	Fast page mode Read or Write Cycle time	40		40		45		ns	
37	t_{PCM}	Fast page mode Read-Modify-Write Cycle	65		65		70		ns	
38	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		20		ns	
39	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		20		ns	
40	t_{RPC}	RAS to $\overline{CAS}$ Precharge Time	0		0		0		ns	
41	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5		5		5		ns	
42	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15		15		15		ns	
43	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns	
44	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	13, 14
45	t_{CLZ}	$\overline{CAS}$ to output in Low-z	0		0		0		ns	
46	t_{REF}	Refresh Interval(512 Cycle)		8		8		8	ms	
47	t_{RASP}	$\overline{RAS}$ Pulse width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
48	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR counter Test Cycle)	40		40		40		ns	

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. t_{RCD}(max.) is specified for reference only. Operation within t_{RCD}(max.) and t_{RAD}(max.) limit insure that t_{RAC}(max.) and t_{AA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD}(max.) then the access time is controlled by t_{AA} and t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.) If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.)
4. Assume $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.)
5. Measured with a load equivalent to two TTL loads and 100pF.
6. Assume $t_{RAD} \geq t_{RAD}$(max.)
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
8. t_{OFF} and t_{OH} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
9. t_{WCS}, t_{WHC}, t_{WHR}, t_{RWD}, t_{AWD}, t_{CWD} are not restrictive operating parameters.
10. t_{WCS}(min.) must be satisfied in the early write cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurenced of $\overline{CAS}$ or $\overline{WE}$.
12. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CAP}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max.).
14. AC measurements assume t_T=5ns
15. An initial pause of 200μs is requlred after power-up and followed by a minimum of 8 initialization cycle(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

CAPACITANCE

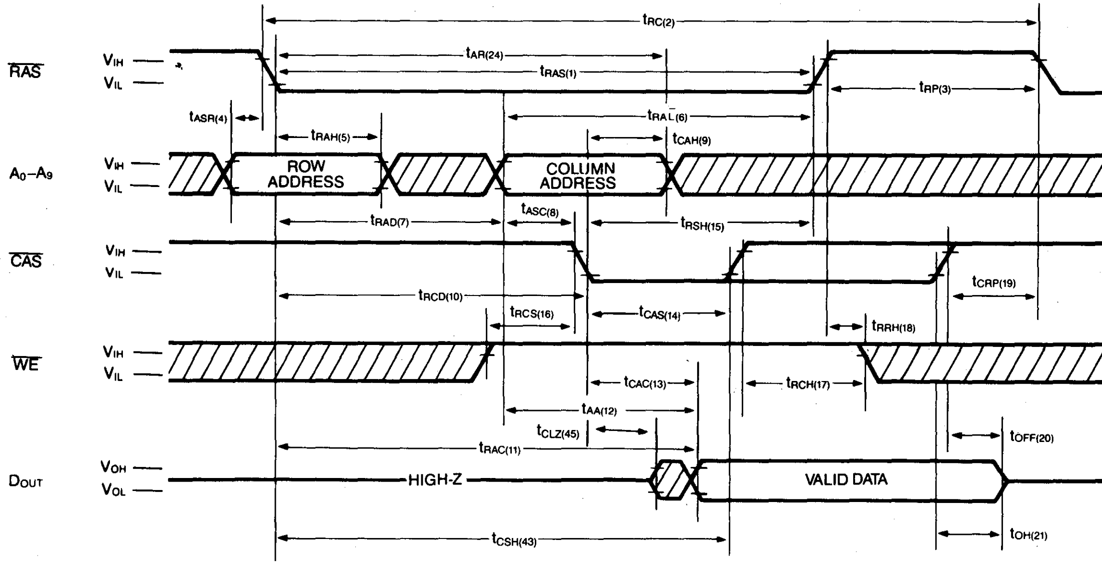
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, Data In	–	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	–	7	pF
C_{OUT}	Data Out	–	7	pF

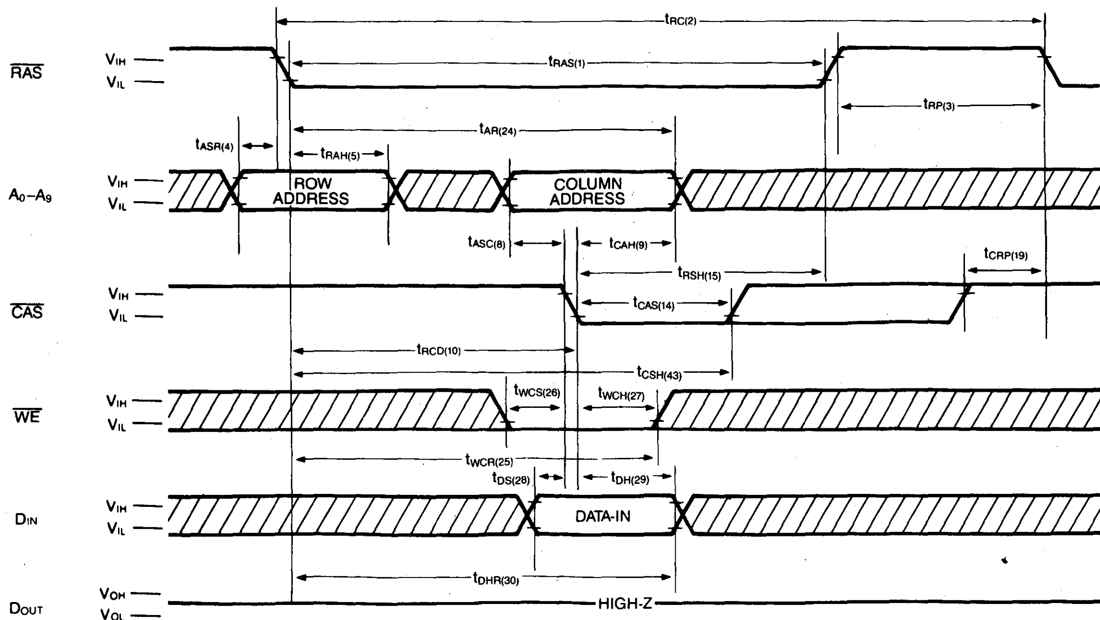
NOTE : Capacitance is measured at worst case of voltage levels with a programmable capacitance meter.

TIMING DIAGRAM

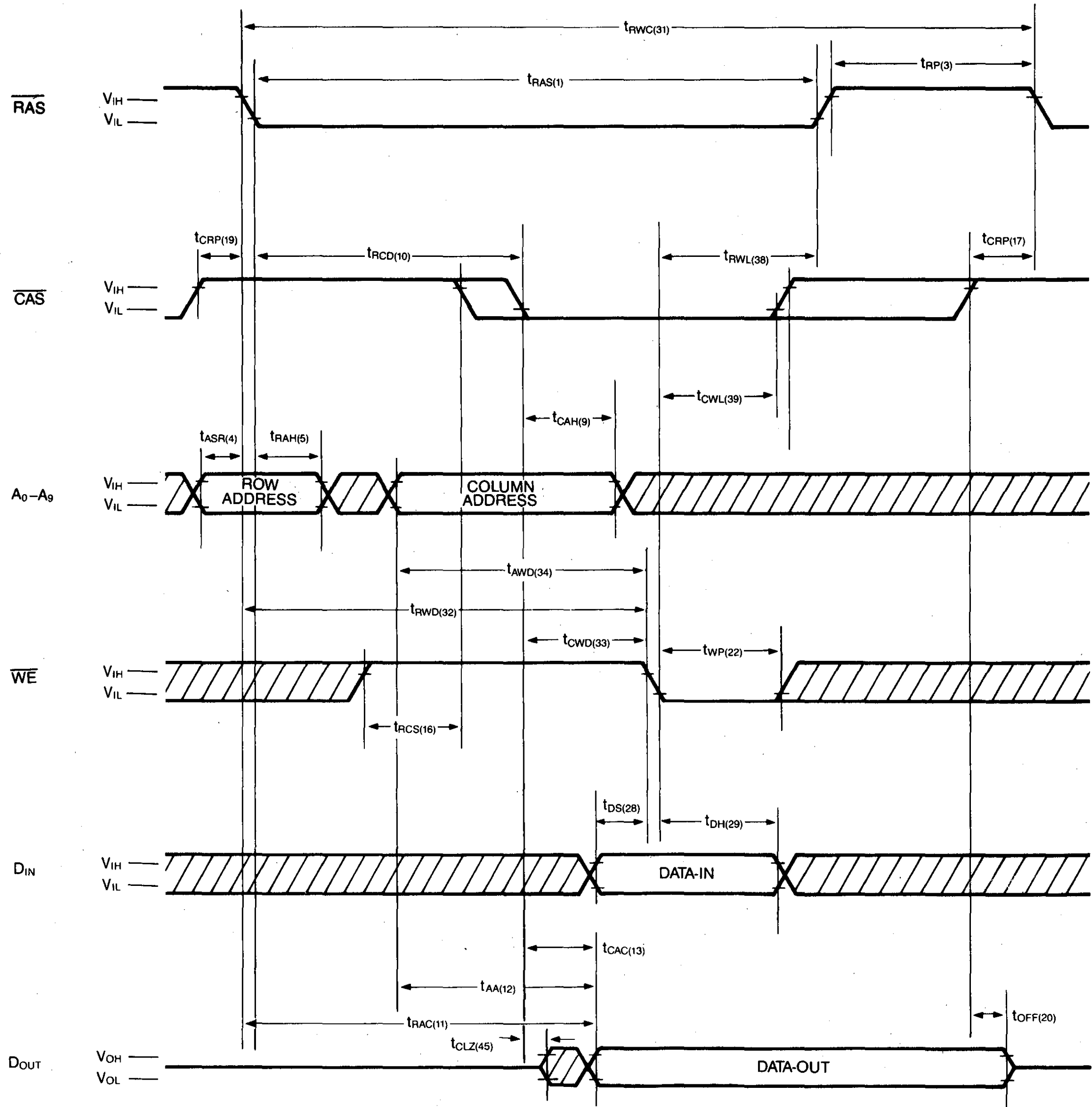
READ CYCLE



EARLY WRITE CYCLE



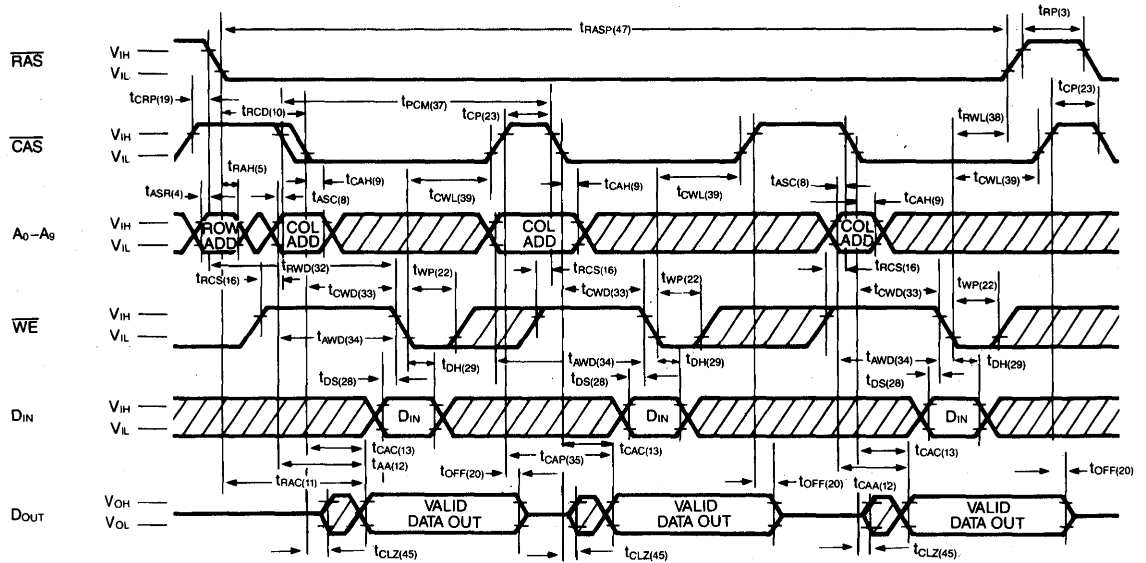
READ-MODIFY-WRITE CYCLE



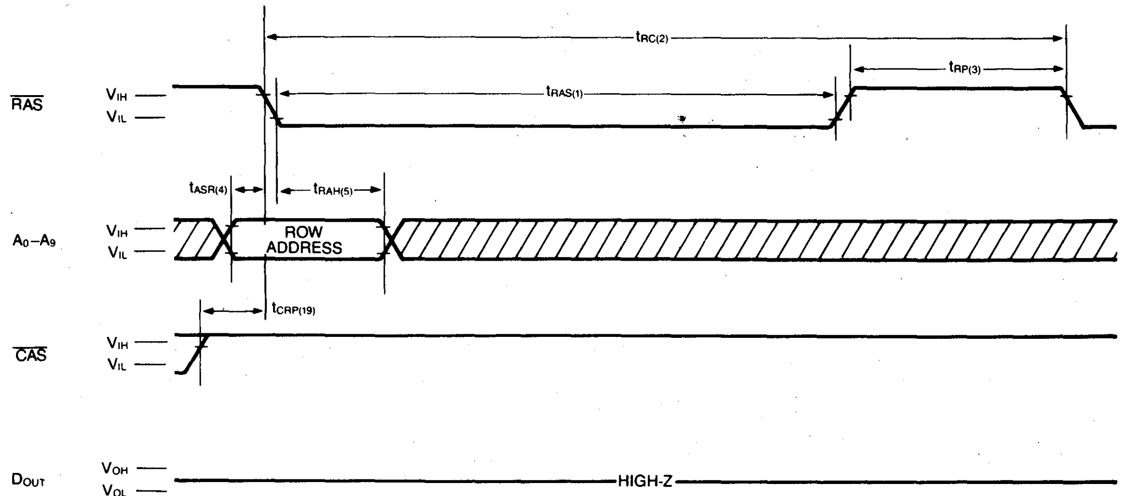
FAST PAGE MODE READ CYCLE

FAST PAGE MODE EARLY WRITE CYCLE

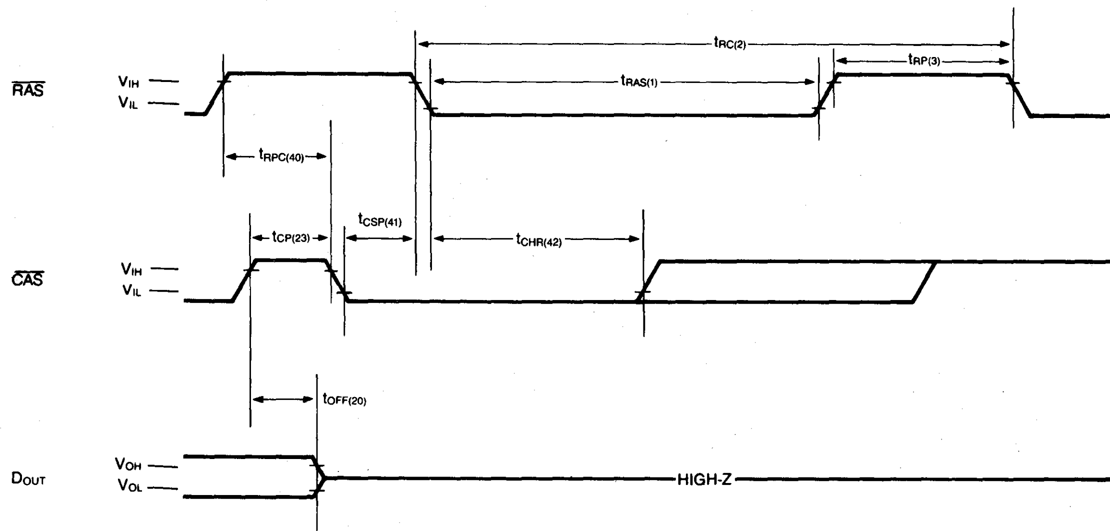
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



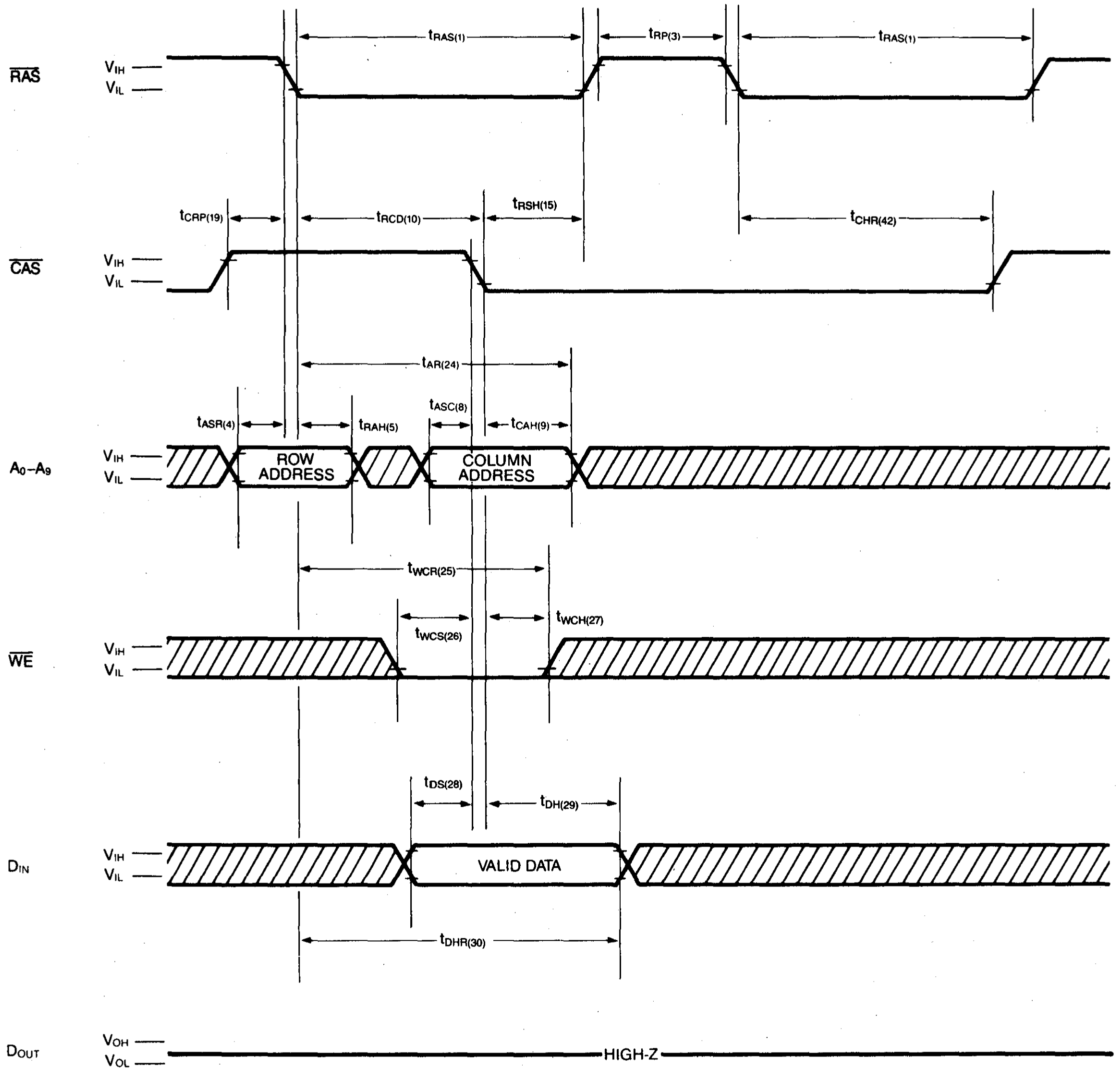
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



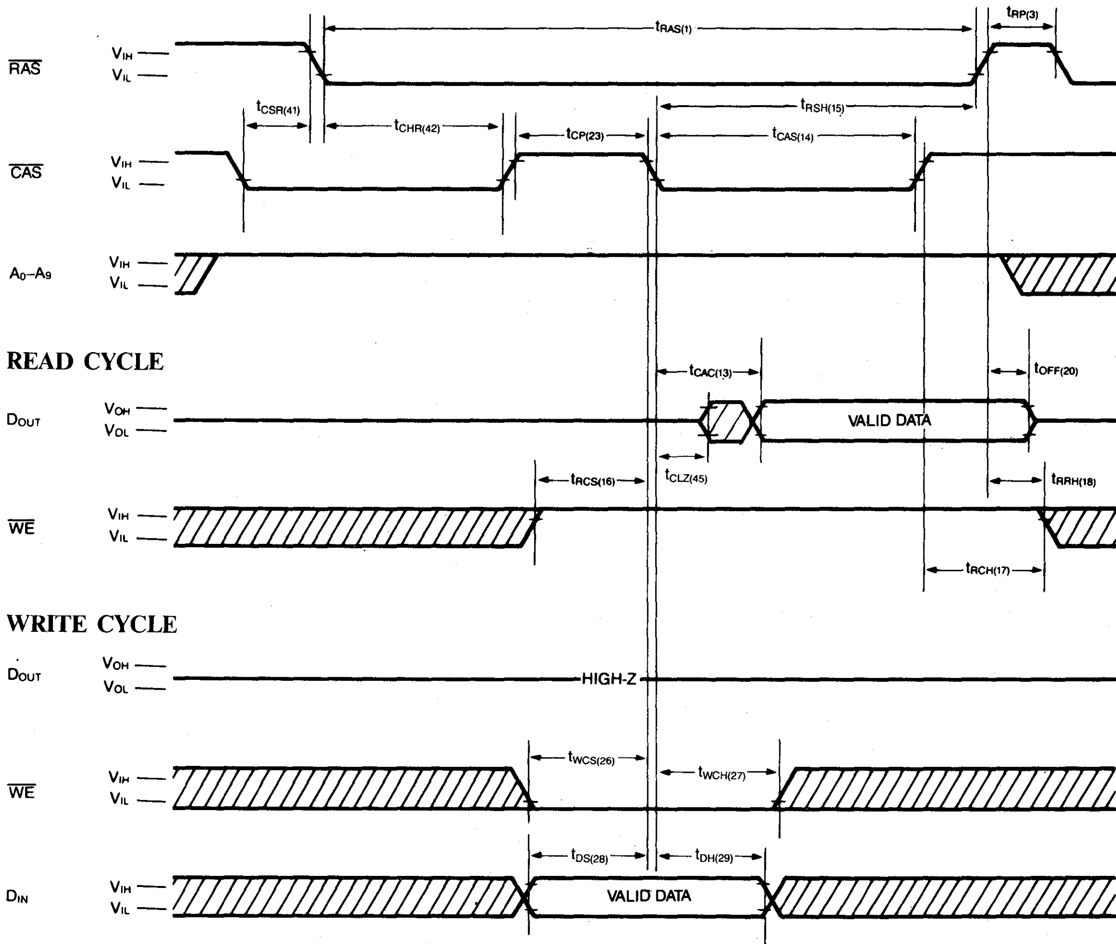
Note: $\overline{WE}$, A_0–A_9 = Don't care

HIDDEN REFRESH CYCLE (READ)

HIDDEN REFRESH CYCLE (WRITE)



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



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FUNCTIONAL DESCRIPTION

The HY531000A is a CMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The HY531000A reads and writes data by multiplexing 20 bit address into 10 bit row and 10 bit column address. The row address is latched by Row Address Strobe ($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

MEMORY CYCLE

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle can not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by holding the Write Enable($\overline{WE}$) signal high during a $\overline{RAS}$ /$\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data output becomes valid only when t_{RAC}, t_{CAC}, and t_{AA} are all satisfied. Consequently, the access time is dependent upon the timing relationship among the t_{RAC}, t_{CAC} and t_{AA}. For example, the access time is limited by t_{AA} when t_{RAC} and t_{CAC} are both satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the latter of $\overline{WE}$ or $\overline{CAS}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$ controlled write cycle (the leading edge of $\overline{WE}$ occurs priors to or coincident with the $\overline{CAS}$ low transition)the output(D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{RAS}$ or $\overline{CAS}$ going high will maintain the data output (D_{OUT}) in the high impedance state.

REFRESH CYCLE

To retain data, 512 $\overline{RAS}$ refresh cycles are required in an 8 ms period. The refresh operation can be performed two ways :

1. Clocking each of 512 row address(A_0 through A_8) with $\overline{RAS}$ at least every 8 ms period. Any combination of $\overline{RAS}$ cycle such as read, write, read-modify-write, or $\overline{RAS}$-only refresh cycle will perform a refresh on the selected row.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle : If $\overline{CAS}$ go low prior to $\overline{RAS}$ go low, the chip enters a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. In $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle the HY531000A will use an internal nine-bit counter output as the source of the row address and will ignore the external address input.

This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh only mode and no data access is allowed. Also, The $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle does not cause device selection and the state of the data output pin will remain in a high impedance state.

In order to guarantee the reliable operation of the $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, a internal counter test mode is provided. The user can use the counter test mode to write in a data pattern consecutively(512 write ycles)and then verify the data which has been written by 512 consecutive read cycles.

DATA RETENTION MODE

The HY531000A offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY531000A power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating

in this mode can be calculated as follows :

$$I = \frac{(t_{RC}) \times (I\ active) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval/512

FAST PAGE MODE OPERATION

Fast page mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while sucessive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent or flow through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latch the address into column address buffer and acts as an output enable.

During this operation, read, write, and read-modify-write, or read-write-read cycles are possible at random or sequential address within a row. Following the entry cycle into fast page mode, access time is t_{AA} or t_{CAP} dependent. If the column address is valid prior to or coincident by t_{CAP} as shown in figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{AA}, For both cases, the falling edge of $\overline{CAS}$ latches the address and enable the output.

Fast page mode provides a sustained data rate over 25 MHz for applications that require high data rates, such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate :

$$\text{Data Rate} = \frac{1024}{t_{RC} + 1023 \times t_{PC}}$$

DATA OUTPUT OPERATION

The HY531000A data output (D_{OUT}), which has tri-state capability, is controlled by $\overline{CAS}$. During a $\overline{CAS}$ the high state ($\overline{CAS}$ at V_{IH}), the data output is in the high impedance state. The following table summarize the D_{OUT} state for various types of cycles.

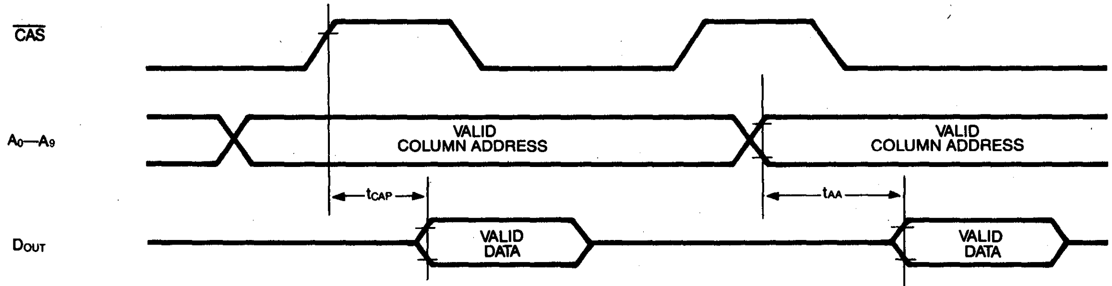
CYCLE	D_{OUT} STATE
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$ Controlled Write Cycle (Early Write)	High Impedance
$\overline{WE}$ Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High Impedance
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-Only Refresh Cycle	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle	Data remain the previous cycle's state (High impedance or low impedance)
$\overline{CAS}$-Only Cycle	High Impedance

POWER ON

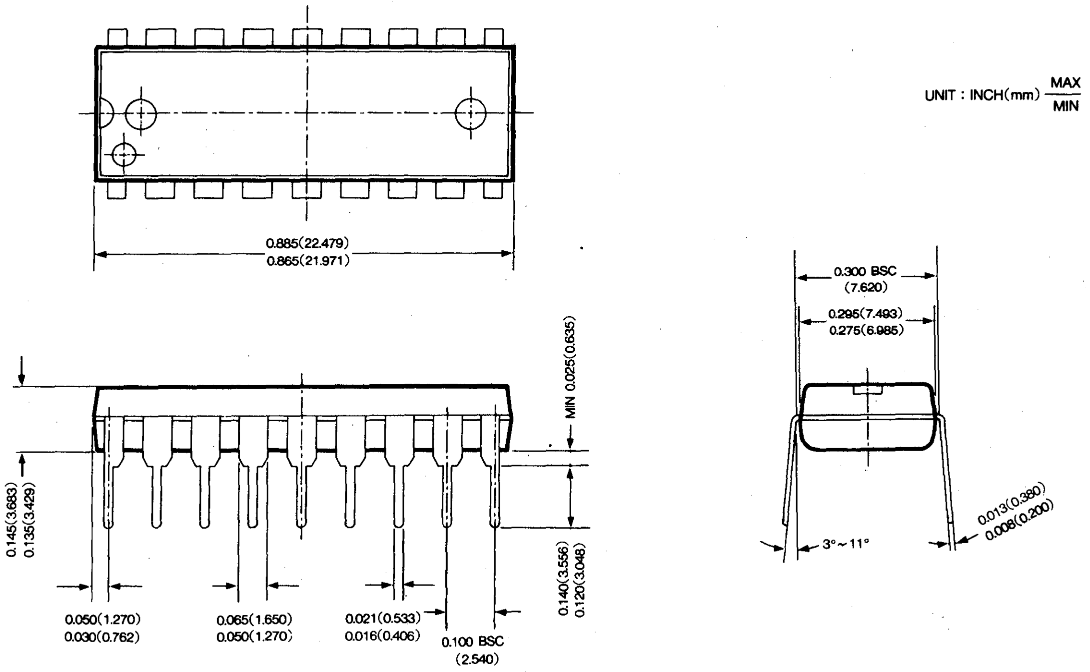
An initial pause of 200 μs is required after the application of V_{DD} power supply, followed by a minimum of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh cycle). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

The V_{DD} current (I_{DD}) requirement of the HY531000A during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ = V_{SS} during power on, the device will go into an active cycle and I_{DD} will exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} level during power on.

FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION



- **18 PIN PLASTIC DUAL IN LINE PACKAGE – 300 MIL**



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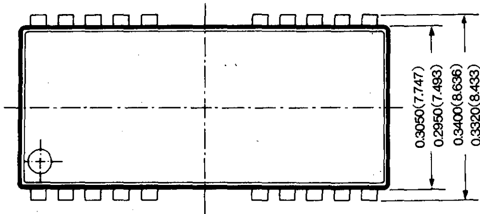
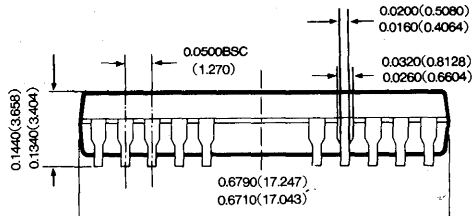
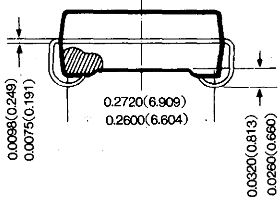
• **20/26 PIN SMALL OUTLINE J-FORM PACKAGE**

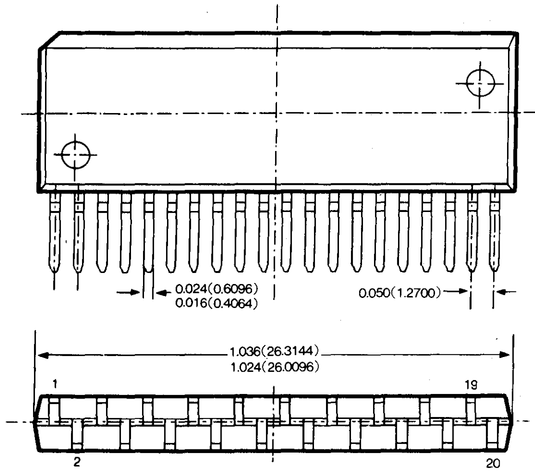


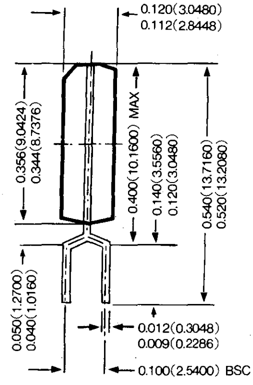
UNIT : INCH(mm) MAX / MIN





• **20 PIN ZIGZAG-IN-LINE PACKAGE－400MIL**





3

MEMO

PRELIMINARY

HYUNDAI SEMICONDUCTOR

HY531000AL

1M×1-Bit CMOS DRAM

M1F1200A-JAN92

DESCRIPTION

The HY531000AL is a high speed, low power 1,048,576×1 bit CMOS dynamic random access memory. Fabricated with the HYUNDAI CMOS process, the HY531000 offers a fast page mode for high bandwidth fast usable speed, CMOS standby current and inherently high CMOS reliability.

All inputs and outputs are TTL compatible. Fast page mode operation allows random or sequential access of up to 1,024 bits within a row with cycle times as fast as 40ns.

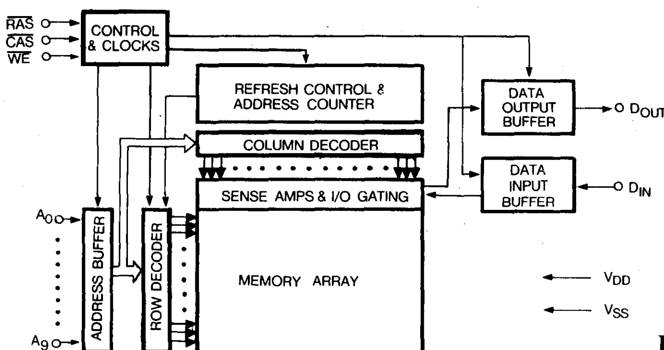
The HY531000AL design is optimized for cache based mainframe and minicomputers, graphics, digital signal processing, high performance microprocessor systems and note book pc.

FEATURES

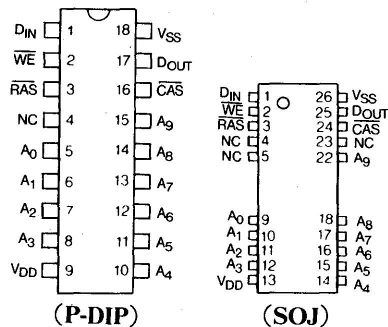
- Low power dissipation for The HY531000AL
  - Operating Current, 60ns : 85mA(max.)
  - TTL Standby Current : 2mA(max.)
  - CMOS Standby Current : 200μA(max.)
  - Battery Back Up Current : 300μA(max.)
- Read-Modify-Write Capability
- $\overline{RAS}$-only, Hidden, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Capability
- Common I/O capability
- Fast Page mode operation for a sustained data rate up to 25 MHz
- 512 refresh cycles/64ms
- High reliability 300 mil P-DIP, 18 pin 20/26 pin SOJ and 400 mil ZIP.
- Fast access time and cycle time (ns)

	HY531000AL-60	HY531000AL-70	HY531000AL-80
Max $\overline{RAS}$ Access Time, t_{RAC}	60	70	80
Max $\overline{CAS}$ Access Time, t_{CAC}	20	20	20
Min Fast Page Mode Cycle Time, t_{PC}	40	40	45
Min Cycle Time, t_{RC}	110	130	150

BLOCK DIAGRAM

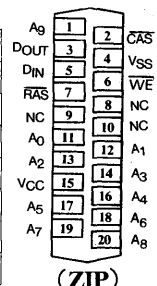


PIN CONNECTIONS



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0-A_9	ADDRESS INPUT
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND



(ZIP)

3

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_{BIAS}	Ambient Temperature Under Bias	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to +150	℃
V_{TERM}	Voltage on Any Pin Except V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Data Out Current	50	mA
P_T	Power Dissipation	0.6	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY531000AL		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$			10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60		85		1, 2
			−70		75		
			−80		65		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs$\ge V_{SS}$			2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60		85	mA	2
			−70		75		
			−80		65		
I_{DD4}	V_{DD} Supply Current, Fast page mode	Minimum Cycle	−60		70	mA	1, 2
			−70		55		
			−80		45		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$			200	μA	
I_{DD6}	V_{DD} Supply Current $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60		85	mA	2
			−70		75		
			−80		65		
I_{DD7}	V_{DD} Supply Current, Battery Back Up	Battery Back Up Current $\overline{CAS}$=CBR cycling or 0.2V, $\overline{WE}=V_{DD}-0.2V$, Add=$V_{DD}-0.2V$ or 0.2V I/O=$V_{DD}-0.2V$ or 0.2V or open, t_{RC}=125μs, $t_{RAS}=t_{RAS}$(min.) ~300ns			300	μA	1
		Same as above except t_{RAS}=300ns~1μs			400	μA	
V_{IL}	Input Low Voltage(all inputs)			−1	0.8	V	
V_{IH}	Input High Voltage(all inputs)			2.4	$V_{DD}+1$	V	
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD}(max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions, Specified I_{DD}(max.) is measured with a maximum of of two transitions per address cycle in Fast page mode.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY53100AL-60		HY53100AL-70		HY53100AL-80		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	110		130		150		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	40		50		60		ns	
4	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
5	t_{RAH}	Row Address Hold Time	10		10		10		ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	1
8	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
9	t_{CAH}	Column Address Hold Time	15		15		15		ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	60	ns	2
11	t_{RAC}	Access Time From $\overline{RAS}$		60		70		80	ns	3, 4, 5
12	t_{AA}	Access Time From Column Address		30		35		40	ns	5, 6, 12
13	t_{CAC}	Access Time From $\overline{CAS}$		20		20		20	ns	6, 12
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	20	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20		20		20		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	7
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	7
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	ns	8
21	t_{OH}	Output Data Hold Time From $\overline{CAS}$	0		0		0		ns	8
22	t_{WP}	Write Pulse Width	15		15		15		ns	
23	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
24	t_{AR}	Column Address Hold Time From $\overline{RAS}$	50		55		60		ns	
25	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	50		55		60		ns	
26	t_{WCS}	Write Command Set-up Time	0		0		0		ns	9, 10
27	t_{WCH}	Write Command Hold Time	15		15		15		ns	
28	t_{DS}	Data-In Set-up Time	0		0		0		ns	11
29	t_{DH}	Data-In Hold Time	15		15		15		ns	11
30	t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	50		55		60		ns	
31	t_{RWC}	RMW Cycle Time	135		155		175		ns	
32	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in RMW Cycle	60		70		80		ns	9
33	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	20		20		20		ns	9
34	t_{AWD}	Column Address to $\overline{WE}$ Delay	30		35		40		ns	9
35	t_{CAP}	Access Time From $\overline{CAS}$ precharge		35		35		40	ns	12

#	SYMBOL	PARAMETER	HY53100AL-60		HY53100AL-70		HY53100AL-80		UNIT	NOTE
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t_{PC}	Fast page mode Read or Write Cycle time	40		40		45		ns	
37	t_{PCM}	Fast page mode Read-Modify-Write Cycle	65		65		70		ns	
38	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		20		ns	
39	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		20		ns	
40	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		ns	
41	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5		5		5		ns	
42	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15		15		15		ns	
43	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns	
44	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	13, 14
45	t_{CLZ}	$\overline{CAS}$ to output in Low-z	0		0		0		ns	
46	t_{REF}	Refresh Interval(512 Cycle)		64		64		64	ms	
47	t_{RASP}	$\overline{RAS}$ Pulse width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
48	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR counter Test Cycle)	40		40		40		ns	

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. t_{RCD}(max.) is specified for reference only. Operation within t_{RCD}(max.) and t_{RAD}(max.) limit insure that t_{RAC}(max.) and t_{AA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD}(max.) then the access time is controlled by t_{AA} and t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.) If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.)
4. Assume $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.)
5. Measured with a load equivalent to two TTL loads and 100pF.
6. Assume $t_{RAD} \geq t_{RAD}$(max.)
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
8. t_{OFF} and t_{OH} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
9. t_{WCS}, t_{WHC}, t_{WHR}, t_{RWD}, t_{AWD}, t_{CWD} are not restrictive operating parameters.
10. t_{WCS}(min.) must be satisfied in the early write cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurenced of $\overline{CAS}$ or $\overline{WE}$.
12. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CAP}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max.).
14. AC measurements assume t_T=5ns
15. An initial pause of 200μs is requlred after power-up and followed by a minimum of 8 initialization cycle(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

CAPACITANCE

(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, Data In	–	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	–	7	pF
C_{OUT}	Data Out	–	7	pF

TIMING DIAGRAM

READ CYCLE

$t_{RC(2)}$ $t_{AR(24)}$ $t_{RAS(1)}$ $t_{RP(3)}$ $t_{ASR(4)}$ $t_{RAL(6)}$ $t_{RAH(5)}$ $t_{CAH(9)}$

$\overline{RAS}$ V_{IH} V_{IL}

A_0–A_9 V_{IH} V_{IL} ROW ADDRESS COLUMN ADDRESS

$t_{RAD(7)}$ $t_{ASC(8)}$ $t_{RSH(15)}$

$\overline{CAS}$ V_{IH} V_{IL}

$t_{RCD(10)}$ $t_{CRP(19)}$ $t_{RCS(16)}$ $t_{CAS(14)}$ $t_{RRH(18)}$

$\overline{WE}$ V_{IH} V_{IL}

$t_{CAC(13)}$ $t_{RCH(17)}$ $t_{AA(12)}$ $t_{CLZ(45)}$ $t_{OFF(20)}$ $t_{RAC(11)}$

D_{OUT} V_{OH} V_{OL} HIGH-Z VALID DATA

$t_{CSH(43)}$ $t_{OH(21)}$

EARLY WRITE CYCLE

$t_{RC(2)}$

$\overline{RAS}$ V_{IH} V_{IL} $t_{RAS(1)}$ $t_{RP(3)}$

$t_{AR(24)}$ $t_{ASR(4)}$ $t_{RAH(5)}$

A_0–A_9 V_{IH} V_{IL} ROW ADDRESS COLUMN ADDRESS

$t_{ASC(8)}$ $t_{CAH(9)}$ $t_{CRP(19)}$ $t_{RSH(15)}$

$\overline{CAS}$ V_{IH} V_{IL} $t_{CAS(14)}$

$t_{RCD(10)}$ $t_{CSH(43)}$ $t_{WCS(26)}$ $t_{WCH(27)}$

$\overline{WE}$ V_{IH} V_{IL}

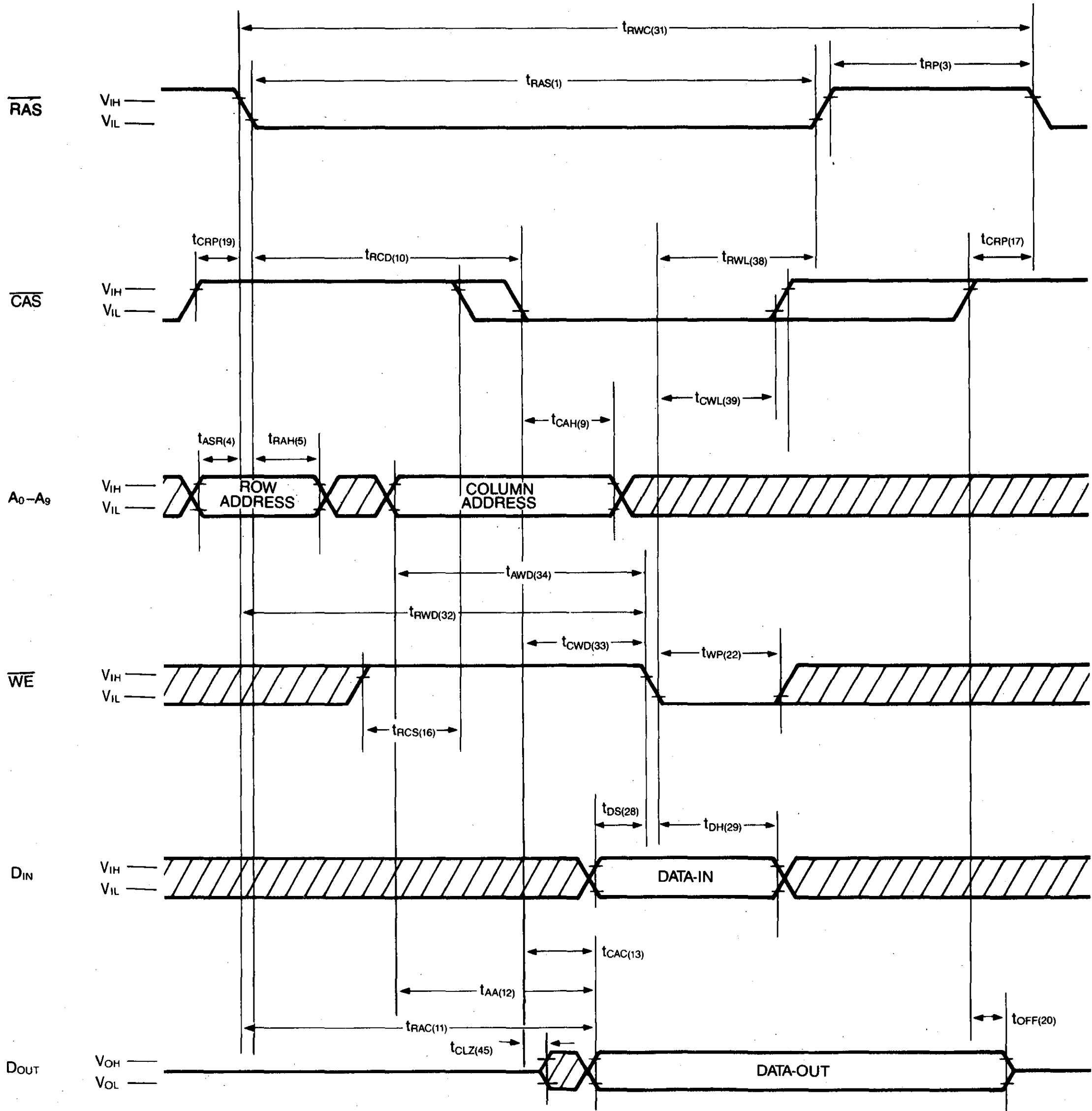
$t_{WCR(25)}$ $t_{DS(28)}$ $t_{DH(29)}$

D_{IN} V_{IH} V_{IL} DATA-IN

$t_{DHR(30)}$

D_{OUT} V_{OH} V_{OL} HIGH-Z

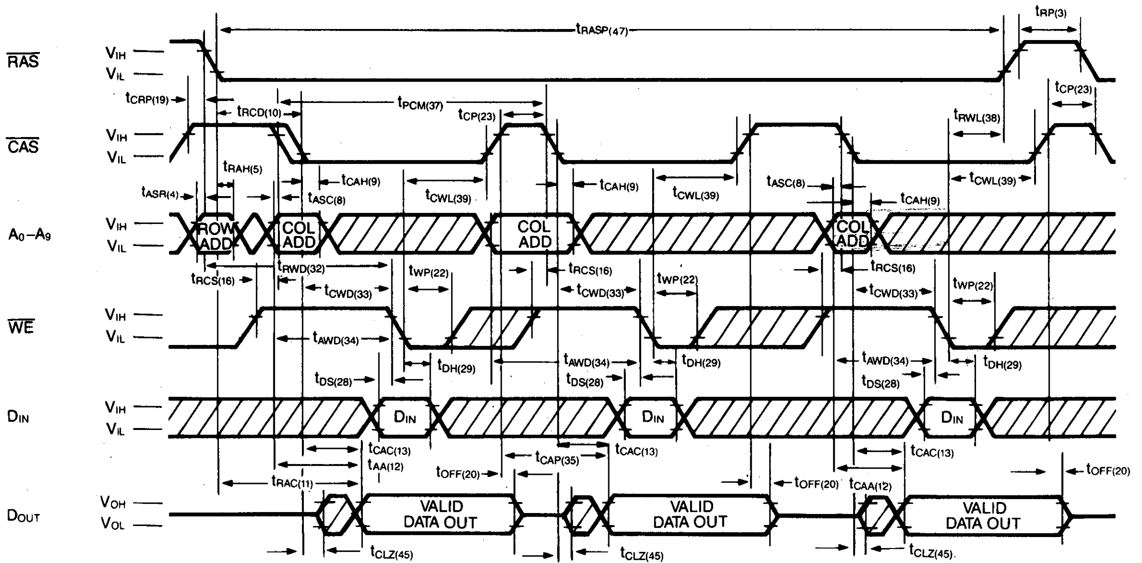
READ-MODIFY-WRITE CYCLE



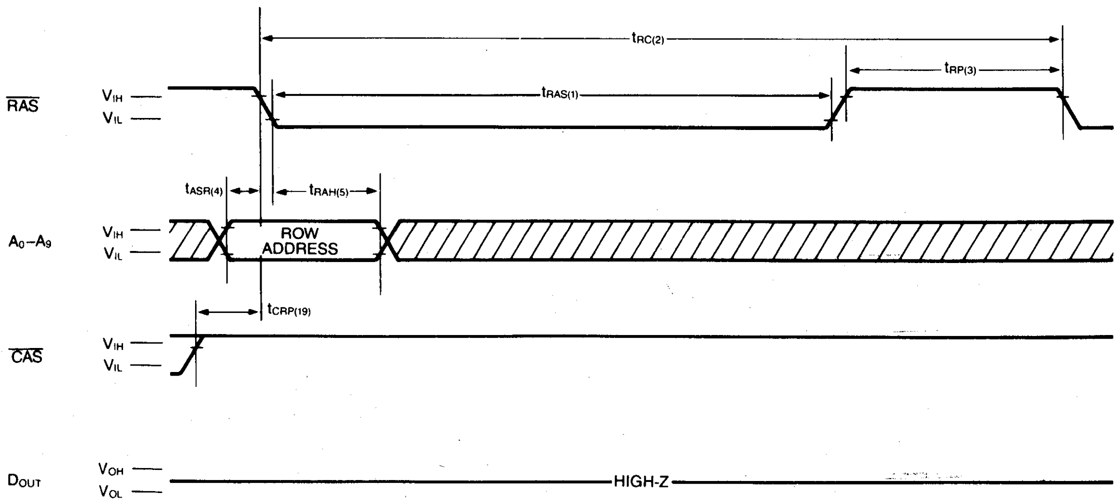
FAST PAGE MODE READ CYCLE

FAST PAGE MODE EARLY WRITE CYCLE

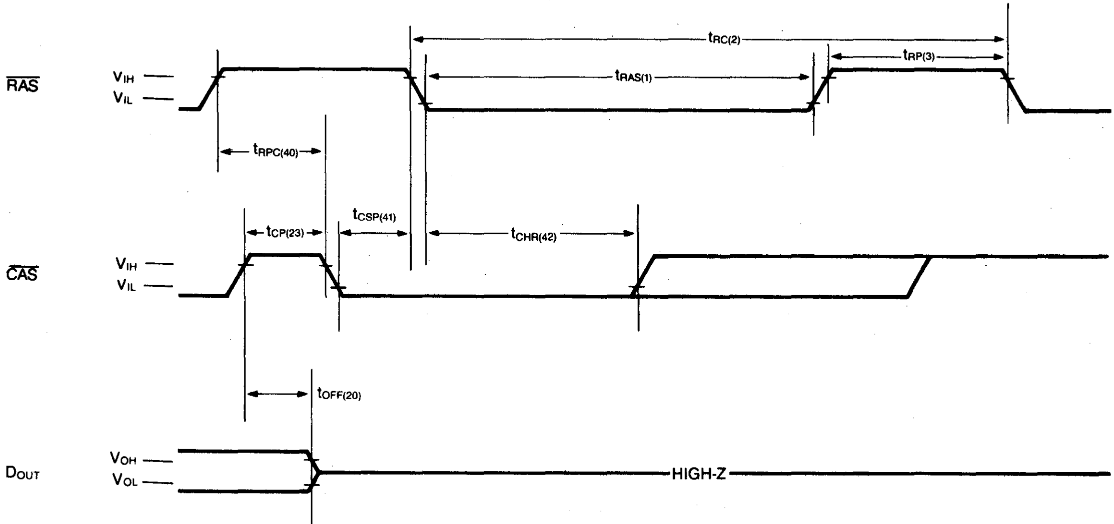
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



Note: $\overline{WE}$, A_0–A_9 = Don't care

HIDDEN REFRESH CYCLE (READ)

$t_{RAS(1)}$ $t_{RP(3)}$ $t_{RAS(1)}$

$\overline{RAS}$ V_{IH} V_{IL}

$t_{CRP(19)}$ $t_{RCD(10)}$ $t_{RSH(15)}$ $t_{CHR(42)}$

$\overline{CAS}$ V_{IH} V_{IL}

$t_{ASC(8)}$ $t_{RAL(6)}$ $t_{RAD(7)}$ $t_{RAH(5)}$ $t_{ASR(4)}$ $t_{CAH(9)}$

A_0–A_9 V_{IH} V_{IL} ROW ADDRESS COLUMN ADDRESS

$t_{AR(24)}$

$t_{RCS(16)}$ $t_{RRH(18)}$

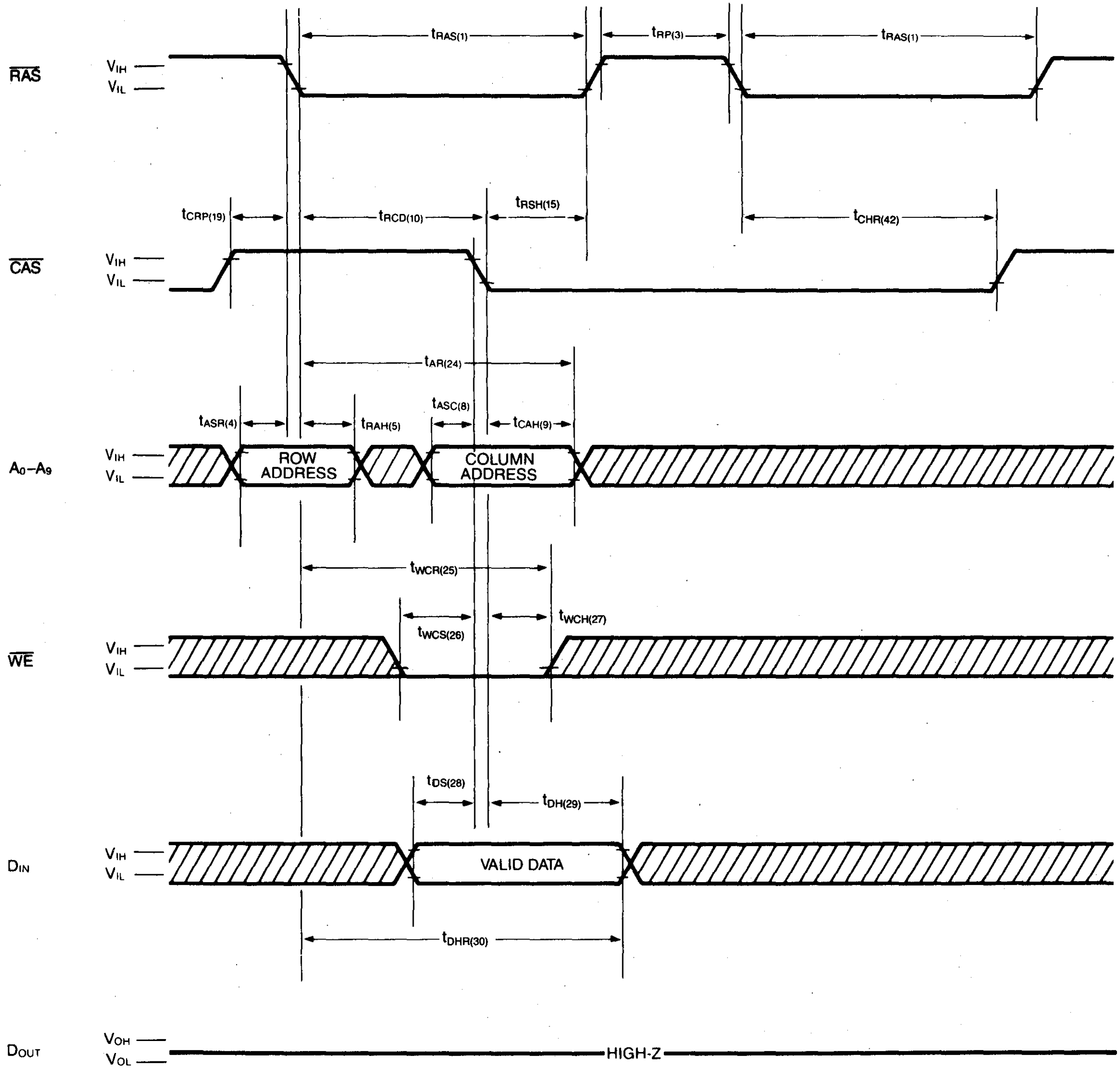
$\overline{WE}$ V_{IH} V_{IL}

$t_{CAC(13)}$ $t_{AA(12)}$ $t_{RAC(11)}$ $t_{OFF(20)}$

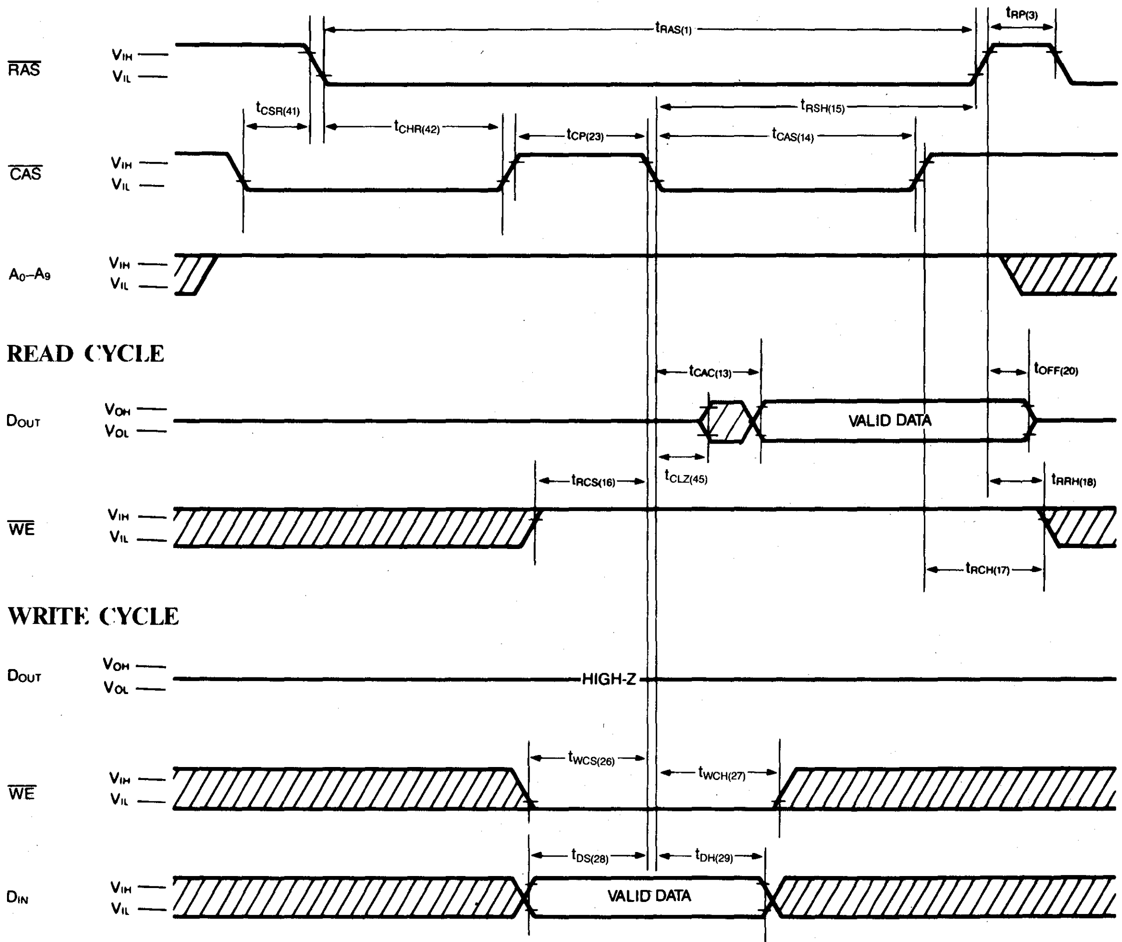
D_{OUT} V_{OH} V_{OL} HIGH-Z VALID DATA

$t_{CLZ(45)}$

HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



3

FUNCTIONAL DESCRIPTION

The HY531000AL is a CMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The HY531000AL reads and writes data by multiplexing 20 bit address into 10 bit row and 10 bit column address. The row address is latched by Row Address Strobe ($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

MEMORY CYCLE

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle can not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by holding the Write Enable($\overline{WE}$) signal high during a $\overline{RAS}$/$\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data output becomes valid only when t_{RAC}, t_{CAC}, and t_{CAA} are all satisfied. Consequently, the access time is dependent upon the timing relationship among the t_{RAC}, t_{CAC} and t_{AA}. For example, the access time is limited by t_{AA} when t_{RAC} and t_{CAC} are both satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the latter of $\overline{WE}$ or $\overline{CAS}$ low transition. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$ controlled write cycle (the leading edge of $\overline{WE}$ occurs priors to or coincident with the $\overline{CAS}$ low transition)the output(D_{OUT}) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{RAS}$ or $\overline{CAS}$ going high will maintain the data output (D_{OUT}) in the high impedance state.

REFRESH CYCLE

To retain data, 512 $\overline{RAS}$ refresh cycles are required in an 64 ms period. The refresh operation can be performed two ways :

1. Clocking each of 512 row address(A_0 through A_8) with $\overline{RAS}$ at least every 64 ms period. Any combination of $\overline{RAS}$ cycle such as read, write, read-modify-write, or $\overline{RAS}$-only refresh cycle will perform a refresh on the selected row.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle : If $\overline{CAS}$ go low prior to $\overline{RAS}$ go low, the chip enters a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. In $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle the HY531000AL will use an internal nine-bit counter output as the source of the row address and will ignore the external address input.

This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh only mode and no data access is allowed. Also, The $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle does not cause device selection and the state of the data output pin will remain in a high impedance state.

In order to guarantee the reliable operation of the $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, a internal counter test mode is provided. The user can use the counter test mode to write in a data pattern consecutively(512 write ycles)and then verify the data which has been written by 512 consecutive read cycles.

DATA RETENTION MODE

The HY531000AL offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY531000AL power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating

in this mode can be calculated as follows :

$$I=\frac{(t_{RC})\times(I\ active)+(t_{RX}-t_{RC})\times(I_{DD6})}{t_{RX}}$$

Where t_{RC}=Refresh Cycle Time
t_{RX}=Refresh Interval/512

FAST PAGE MODE OPERATION

Fast page mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while sucessive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as a transparent or flow through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latch the address into column address buffer and acts as an output enable.

During this operation, read, write and read-modify-write, or read-write-read cycles are possible at random or sequential address within a row. Following the entry cycle into fast page mode, access time is t_{AA} or t_{CAP} dependent. If the column address is valid prior to or coincident by t_{CAP} as shown in figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{AA}, For both cases, the falling edge of $\overline{CAS}$ latches the address and enable the output.

Fast page mode provides a sustained data rate over 25 MHz for applications that require high data rates, such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate :

$$\text{Data Rate}=\frac{1024}{t_{RC}+1023\times t_{PC}}$$

DATA OUTPUT OPERATION

The HY531000AL data output (D_{OUT}), which has tri-state capability, is controlled by $\overline{CAS}$. During a $\overline{CAS}$ the high state ($\overline{CAS}$ at V_{IH}), the data output is in the high impedance state. The following table summarize the D_{OUT} state for various types of cycles.

CYCLE	D_{OUT} STATE
Read Cycle	Data from Addressed Memory Cell
$\overline{CAS}$ Controlled Write Cycle (Early Write)	High Impedance
$\overline{WE}$ Controlled Write Cycle (Late Write)	Active, Not Valid
Read-Modify-Write Cycle	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High Impedance
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-Only Refresh Cycle	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle	Data remain the previous cycle's state (High impedance or low impedance)
$\overline{CAS}$-Only Cycle	High Impedance

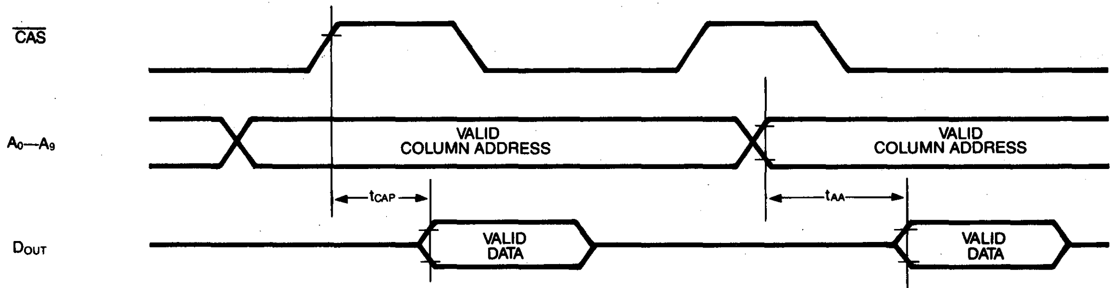
POWER ON

An initial pause of 200 μs is required after the application of V_{DD} power supply, followed by a minimum of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh cycle). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

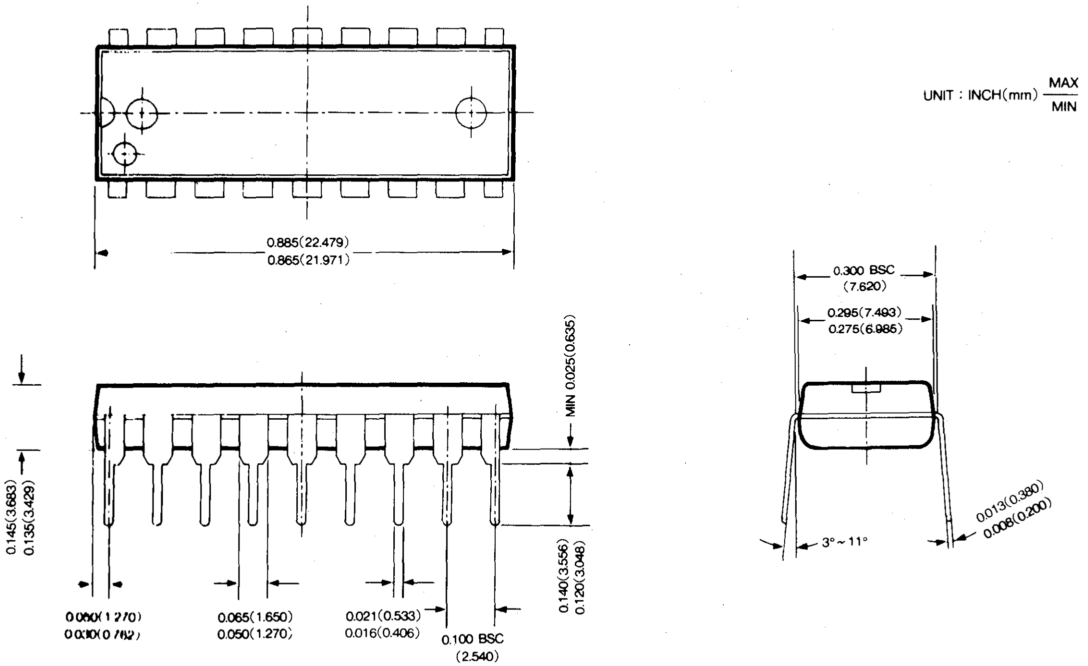
The V_{DD} current (I_{DD}) requirement of the HY531000AL during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}=V_{SS}$ during power on, the device will go into an active cycle and I_{DD} will exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} level during power on.

3

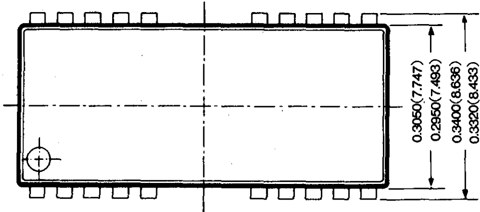
FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION



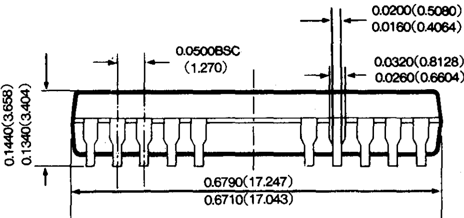
• **18 PIN PLASTIC DUAL IN LINE PACKAGE – 300 MIL**

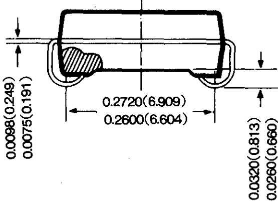


- **20/26 PIN SMALL OUTLINE J-FORM PACKAGE**

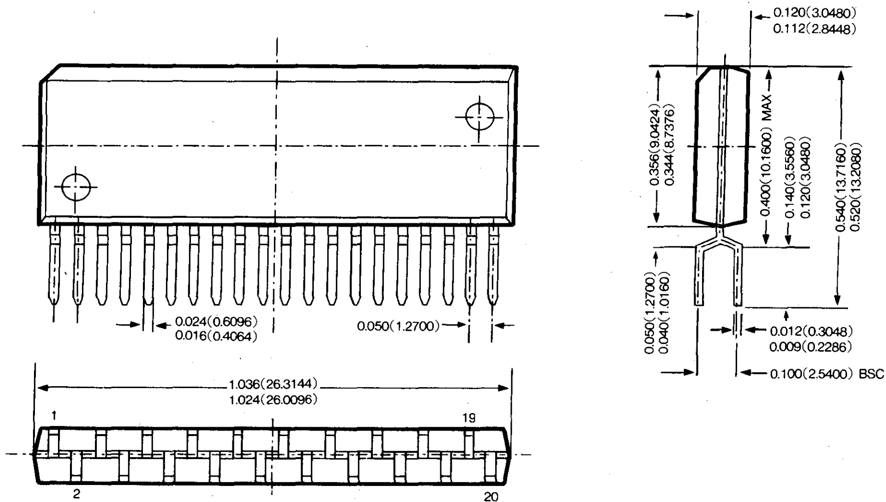


UNIT : INCH(mm) MAX/MIN





- **20 PIN ZIGZAG-IN-LINE PACKAGE－400MIL**



3

MEMO

DESCRIPTION

The HY534256 is a high speed, low power 262,144×4 bit CMOS dynamic random access memory. Fabricated with the HYUNDAI CMOS process, the HY534256 offers a fast page mode for high bandwidth operation, fast usable speed, CMOS standby current, and inherently high CMOS reliability.

All inputs and outputs are TTL compatible. Fast page mode operation allows random or sequential access of up to 512(×4)bits within a row with cycle times as fast as 40ns.

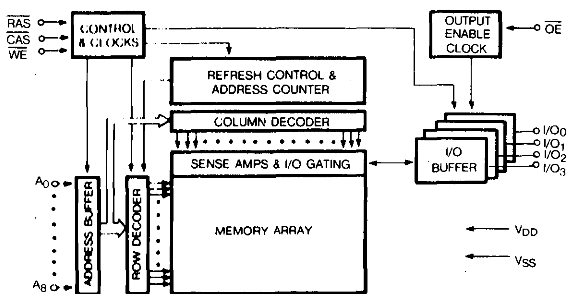
The HY534256 design is optimized for cache based mainframe and minicomputers, graphics, digital signal processing, and high performance microprocessor systems.

FEATURES

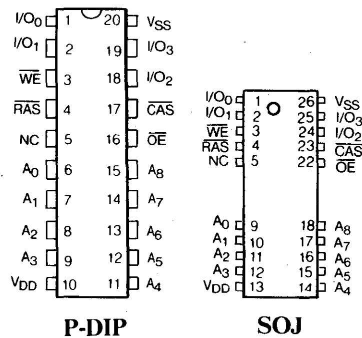
- **Low power dissipation**
  - **Operating current, 100ns : 60mA(max.)**
  - **TTL standby current : 2mA(max.)**
  - **CMOS standby current : 1mA(max.)**
- **Read-Modify-Write capability**
- **$\overline{RAS}$-only, Hidden, $\overline{CAS}$-before-$\overline{RAS}$ refresh capability**
- **Fast Page mode operation for a sustained data rate up to 25 MHz**
- **512 refresh cycles/8 ms**
- **High reliability 300 mil 20 pin P-DIP and 20/26 pin SOJ**
- **Fast access time and cycle time (ns)**

	HY534256-60	HY534256-70	HY534256-80	HY534256-10
Max $\overline{RAS}$ Access Time, t_{RAC}	60	70	80	100
Max $\overline{CAS}$ Access Time, t_{CAC}	20	20	20	25
Min Fast Page Mode Cycle Time, t_{PC}	40	40	45	55
Min Cycle Time, t_{RC}	120	130	150	180

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
A_0-A_8	ADDRESS INPUT
I/O_0-I/O_3	DATA INPUT/OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	−55 to 150	°C
V_{TERM}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	0.6	W

NOTE : Stress above those listed under "Absolute Maximum Ratings" might cause permanent damage to the device.

DC CHARACTERISTICS

(T_A=0 ℃ to 70 ℃, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY534256		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		–	10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60	–	90	mA	1,2
			−70	–	80		
			−80	–	70		
			−10	–	60		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH}, other inputs$\geq V_{SS}$		–	2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60	–	90	mA	2
			−70	–	80		
			−80	–	70		
			−10	–	60		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−60	–	70	mA	1,2
			−70	–	60		
			−80	–	50		
			−10	–	40		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs$\geq V_{SS}$		–	1	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60	–	90	mA	2
			−70	–	80		
			−80	–	70		
			−10	–	60		
V_{IL}	Input Low Voltage(all inputs)			−1	0.8	V	
V_{IH}	Input High Voltage(all inputs)			2.4	V_{DD}+1	V	
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD}(max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in fast page mode.

AC CHARACTERISTICS

(T_A=0 ℃ to 70 ℃, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY534256 60 MIN.	60 MAX.	70 MIN.	70 MAX.	80 MIN.	80 MAX.	10 MIN.	10 MAX.	UNIT	NOTE
1	t_{RAS}	RAS Pulse Width	60	10K	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	180	–	ns	
3	t_{RP}	RAS Precharge Time	50	–	50	–	60	–	70	–	ns	
4	t_{CSH}	CAS Hold Time	60	–	70	–	80	–	100	–	ns	
5	t_{CAS}	CAS Pulse Width	20	10K	20	10K	20	10K	25	10K	ns	
6	t_{RCD}	RAS to CAS Delay	20	40	20	50	20	60	25	75	ns	2
7	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	0	–	ns	
8	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	0	–	ns	
9	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	15	–	ns	
10	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	0	–	ns	
11	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	20	–	ns	
12	t_{RSH}	RAS Hold Time	20	–	20	–	20	–	25	–	ns	
13	t_{CRP}	CAS to RAS Precharge Time	5	–	5	–	5	–	5	–	ns	
14	t_{RCH}	Read Command Hold Time Referenced to CAS	0	–	0	–	0	–	0	–	ns	8
15	t_{RRH}	Read Command Hold Time Referenced to RAS	0	–	0	–	0	–	0	–	ns	8
16	t_{ROH}	RAS Hold Time Referenced to OE	10	–	10	–	15	–	20	–	ns	
17	t_{OAC}	Access Time from OE	–	20	–	20	–	20	–	25	ns	
18	t_{CAC}	Access Time from CAS	–	20	–	20	–	20	–	25	ns	5,6
19	t_{RAC}	Access Time from RAS	–	60	–	70	–	80	–	100	ns	3,4,5
20	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	–	50	ns	5,7
21	t_{LZ}	OE or CAS to Output Low Impedance	0	–	0	–	0	–	0	–	ns	3
22	t_{HZ}	OE or CAS to Output High Impedance	0	20	0	20	0	20	0	20	ns	11
23	t_{AR}	Column Address Hold Time from RAS	50	–	55	–	60	–	75	–	ns	
24	t_{RAD}	RAS to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	1
25	t_{CWL}	Write Command to CAS Lead Time	20	–	20	–	20	–	25	–	ns	
26	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	0	–	ns	9
27	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	20	–	ns	
28	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	20	–	ns	11
29	t_{WCR}	Write Command Hold Time from RAS	50	–	55	–	60	–	75	–	ns	
30	t_{RWL}	Write Command to RAS Lead Time	20	–	20	–	20	–	25	–	ns	
31	t_{DS}	Data-In Set-up Time	0	–	0	–	0	–	0	–	ns	10
32	t_{DH}	Data-In Hold Time	15	–	15	–	15	–	20	–	ns	10
33	t_{WOH}	Write to OE Hold Time	20	–	20	–	20	–	25	–	ns	
34	t_{OED}	OE to Data Delay	20	–	20	–	20	–	25	–	ns	
35	t_{RWC}	Read-Modify-Write(RMW) Cycle Time	175	–	185	–	205	–	245	–	ns	

3

#	SYMBOL	PARAMETER	HY534256								UNIT	NOTE
			60		70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	50	–	50	–	50	–	60	–	ns	9
37	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	90	–	100	–	110	–	135	–	ns	9
38	t_{AWD}	Column Address to $\overline{WE}$ Delay	60	–	65	–	70	–	85	–	ns	9
39	t_{PC}	Fast Page Mode Read or Write Cycle Time	40	–	40	–	45	–	55	–	ns	
40	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	95	–	95	–	100	–	115	–	ns	
41	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	10	–	ns	
42	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	50	–	ns	
43	t_{CPA}	Access Time from Column Precharge	–	35	–	35	–	40	–	50	ns	12
44	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50	–	55	–	60	–	75	–	ns	
45	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5	–	5	–	5	–	5	–	ns	
46	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	0	–	ns	
47	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	15	–	15	–	20	–	ns	
48	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	3	50	ns	13
49	t_{REF}	Refresh Interval(512 Cycle)	–	8	–	8	–	8	–	8	ms	
50	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	100K	70	100K	80	100K	100	100K	ns	
51	t_{CPT}	$\overline{CAS}$ Precharge Time (CBR Counter Test Cycle)	40	–	40	–	40	–	50	–	ns	

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{CAC}.
2. Operation with in the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a referenced point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then the access lime is controlled by t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.). If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.).
4. Assume $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.).
5. Measured with a load equivalent to two TTL loads and 100 pF.
6. Assumes that $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.)
7. Assumes that $t_{RCD} \leq t_{RCD}$(max.) and $t_{RAD} \geq t_{RAD}$(max.)
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle ; if $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), the cycle is a read/write and the data output will contain data from the selected cell : if neither of the above sets of conditions is satisfied, the condition of the data out (at access time)is indeterminate.
10. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$
11. t_{HZ} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
12. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{CPA}.
13. V_{IL}(max.) and AC measurements assumen t_T=5ns
14. An initial pause of 200μs is required after power-up and followed by a minimum of 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

CAPACITANCE

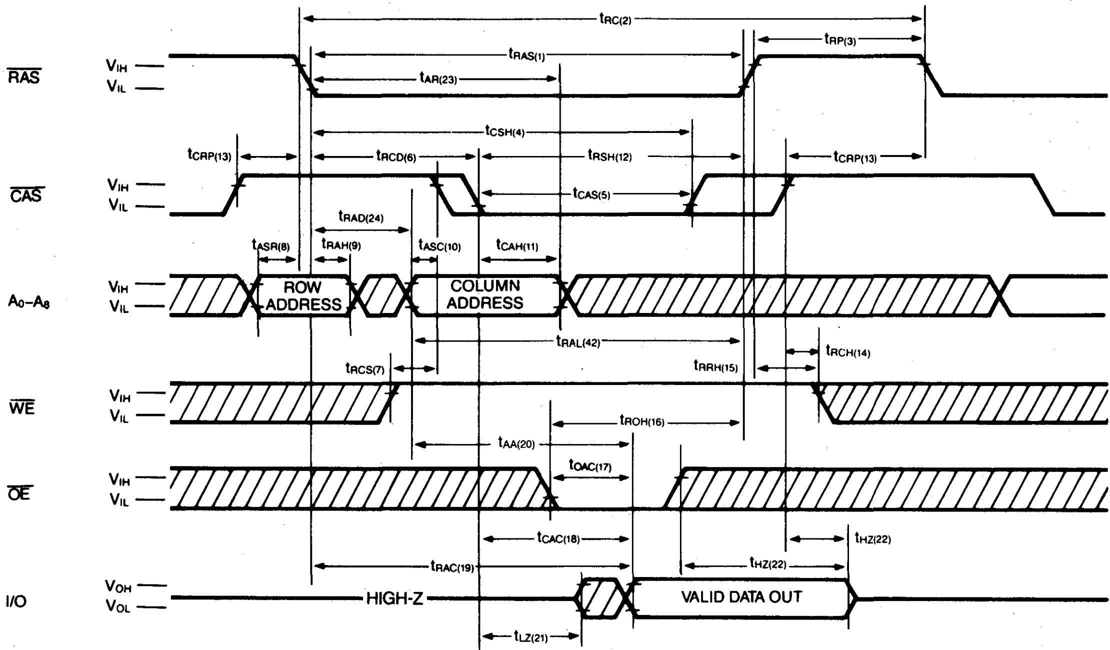
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, Data input	–	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	–	7	pF
C_{IN3}	Data Out	–	7	pF

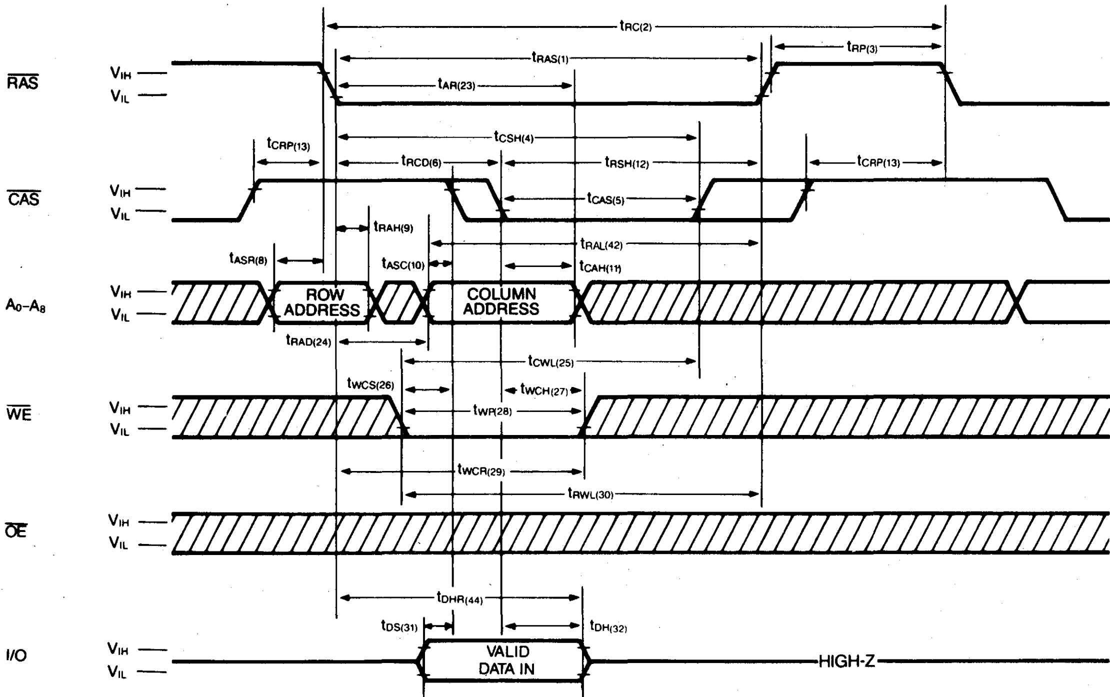
NOTE : Capacitance is measured at worst case of voltage levels with a programmable capacitance meter.

TIMING DIAGRAMS

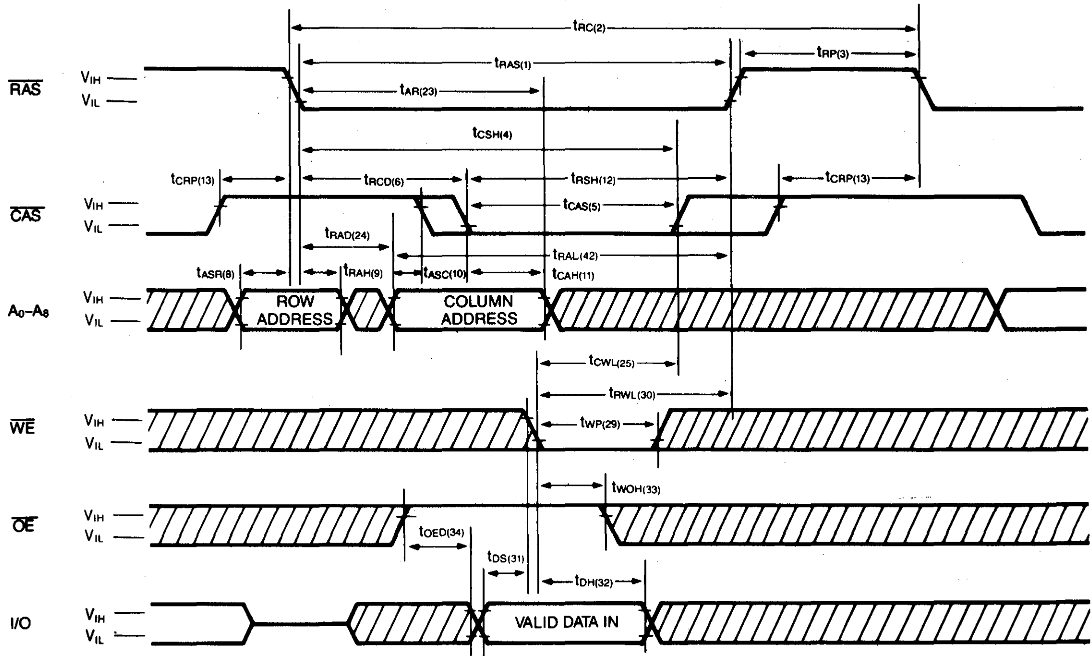
READ CYCLE



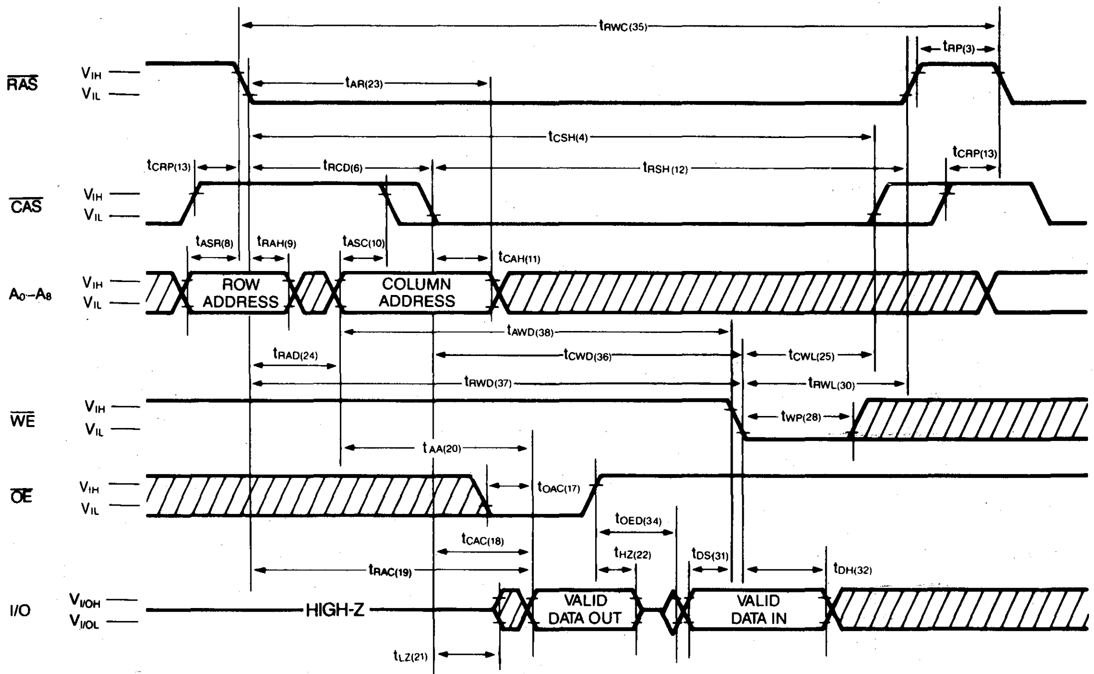
EARLY WRITE CYCLE



WRITE CYCLE (OE CONTROLLED)



READ-MODIFY-WRITE CYCLE

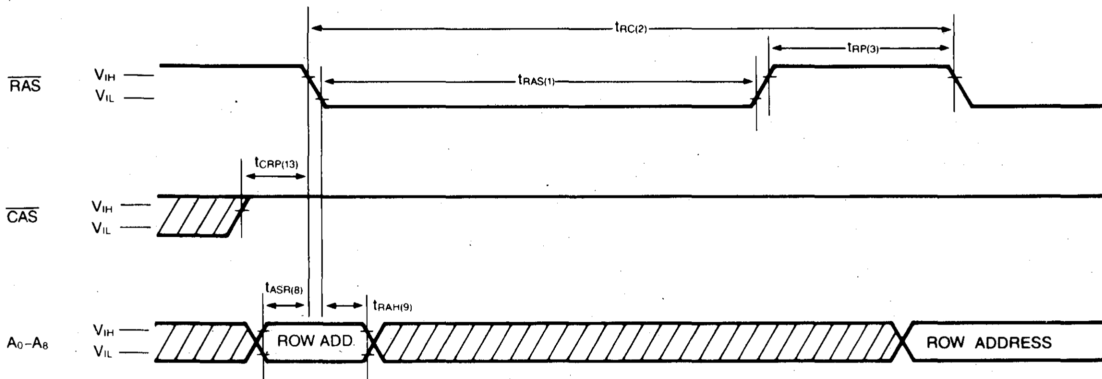


FAST PAGE MODE READ CYCLE

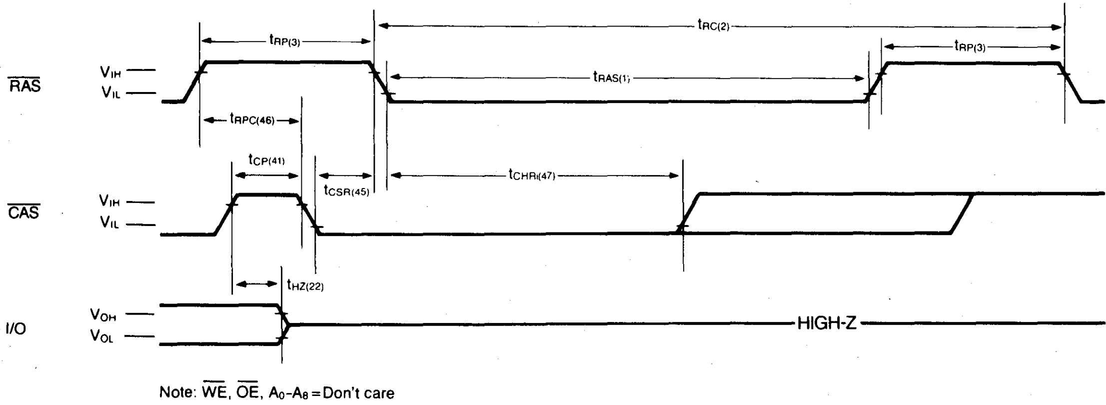
FAST PAGE MODE EARLY WRITE CYCLE

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

$\overline{RAS}$-ONLY REFRESH CYCLE



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE



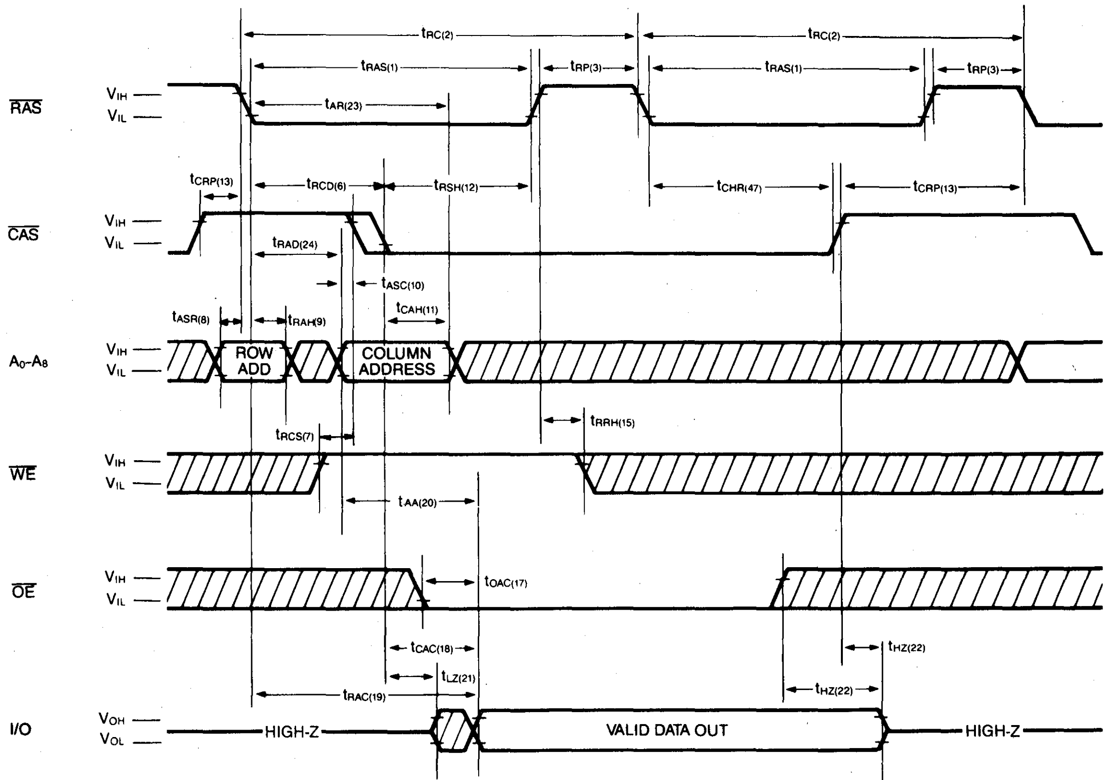
Note: $\overline{\text{WE}}$, $\overline{\text{OE}}$, A_0–A_8 = Don't care

$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE

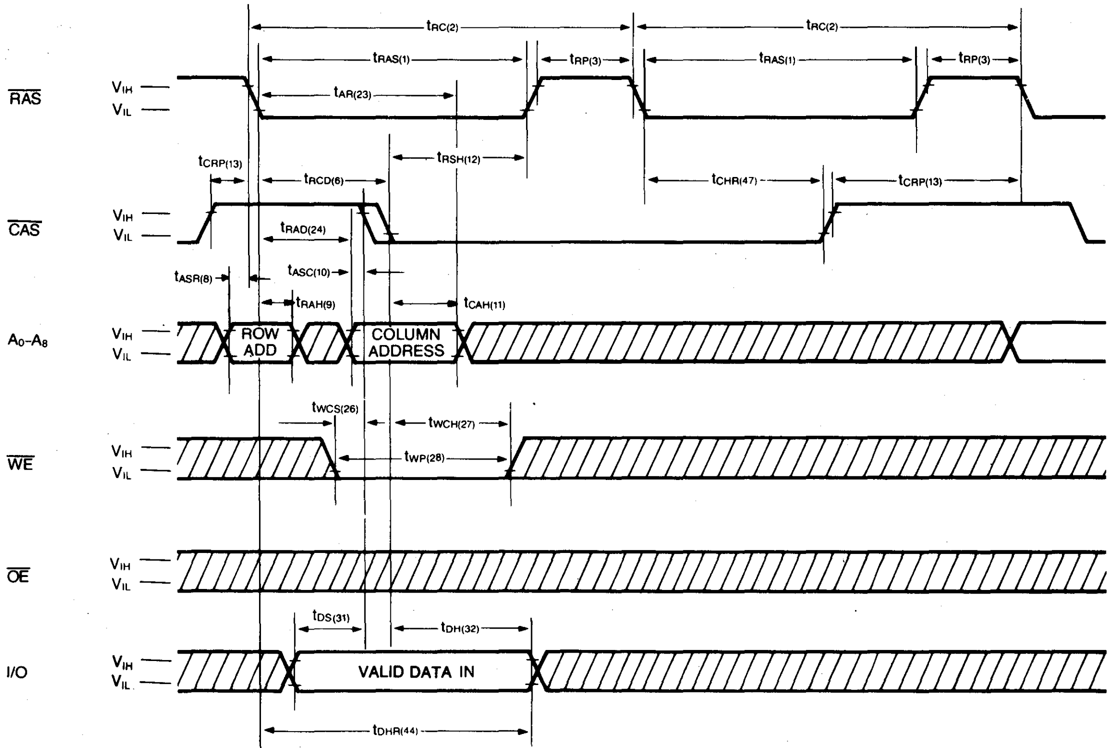
READ CYCLE

WRITE CYCLE

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



FUNCTIONAL DESCRIPTION

The HY534256 is a CMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The HY534256 reads and writes 4 bits of data at a time by multiplexing a 18 bit address into a 9 bit row and a 9 bit column address. The row address is latched by the Row Address Strobe($\overline{\text{RAS}}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{\text{CAS}}$). Because access time is primarily dependent on a valid column address, the delay time between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ can be long without affecting the access time.

MEMORY CYCLE

The memory cycle is initiated by bringing $\overline{\text{RAS}}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be inititiated until the minimum precharge time, t_{RP}, and t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by maintaining the Write Enable ($\overline{\text{WE}}$) signal high during the $\overline{\text{RAS}}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data out is controlled by the Out Enable($\overline{\text{OE}}$) and $\overline{\text{CAS}}$(See the write cycle description).

Data out becomes valid only when t_{RAC}, t_{AA}, t_{OAC} and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC}, t_{OAC} and t_{CAC} are all satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{\text{WE}}$ low during a $\overline{\text{RAS}}$ operation.

The column address is latched by $\overline{\text{CAS}}$, The input data must be valid at or before the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. Consequently, the write cycle can be $\overline{\text{WE}}$ controlled or $\overline{\text{CAS}}$ controlled depending upon the latter of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$ low transition. In a $\overline{\text{CAS}}$ controlled write cycle(the leading edge or $\overline{\text{WE}}$ occurs prior to or coincident with the $\overline{\text{CAS}}$ low transition)the input/output (I/O) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{\text{CAS}}$ going high will maintain the I/O in the high impedance state, terminating with $\overline{\text{WE}}$ going high allows the output to go active, and $\overline{\text{OE}}$ must be brought high to allow for inputs on the I/O.

The HY534256 incorporates a self-timed write feature which simplifies the system interface and optimizes data bandwidth. After the write funcition has been initiated, the HY534256 internally completes the write action and unlatches the address and data latches. Thus, the latches are ready for the next input/output cycle. This eliminates the need for long address and data hold times during the write operation and allows a subsequent column address to be applied earlier. This minimizes a write pulse width, write precharge time, and hold time which provides maximum flexibility in system design.

REFRESH CYCLE

To retain data, 512 $\overline{\text{RAS}}$ refresh cycle are required in an 8 ms period. The refresh operation can be performed two ways :

1. Clocking each of 512 row address(A_0 through A_8) with $\overline{\text{RAS}}$ at least every 8 ms period. Any combination of $\overline{\text{RAS}}$ cycle such as read, write, read-modify-write, or $\overline{\text{RAS}}$-only refresh cycle will perform a refresh.
2. $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle : If $\overline{\text{CAS}}$ go low prior to $\overline{\text{RAS}}$ go low, the chip enters $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle. The HY534256 will use an internal nine bits counter output as the source of the row address and will ignore the external address inputs.

This $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh mode is a refresh only mode and no data access is

allowed. Also, the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle does not cause device selection and the state of the data output pin will remain in a high impedance state.

In order to guarantee the reliable operation of $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, an internal counter test mode is provided. The user can use the counter test mode to write in a data pattern consecutively (512 write cycles) and, then verify the data which has been written by 512 consecutive read cycles.

DATA RETENTION MODE

The HY534256 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY534256 power consumption is reduced to the low I_{DD5} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows :

$$I=\frac{(t_{RC})\times(I\ active)+(t_{RX}-t_{RC})\times(I_{DD5})}{t_{RX}}$$

Where t_{RC}=Refersh Cycle Time
t_{RX}=Refresh Interval/512

FAST PAGE MODE OPERATION

Fast page mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while sucessive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as transparent or flow through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into column address buffer and acts as an output enable.

During this operation, read, write, and read-modify-write, or read-write-read cycles are possible at random or sequential address within a low. Following the entry cycle into fast page mode, access time is t_{AA} or t_{CAP} dependent. It the column address is valid prior to or coincident by t_{CAP} as shown in figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{AA}, For both cases, the falling edge of $\overline{CAS}$ latches the address and enable the output.

Fast page mode provides a sustanined data rate over 25 MHz for applications that require high data rate such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate :

$$\text{Data Rate}=\frac{512}{t_{RC}+511\times t_{PC}}$$

DATA OUTPUT OPERATION

The HY534256 input/output(I/O) is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables data to transfer into and from a selected row address. A $\overline{RAS}$ high transition disables data transfer and will latch the output data if the output is enabled. After a memory cycle is initiated by a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or a $\overline{CAS}$ low level enables the internal I/O data. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O data path and disables the output driver if the driver was enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path, nor on the output driver.

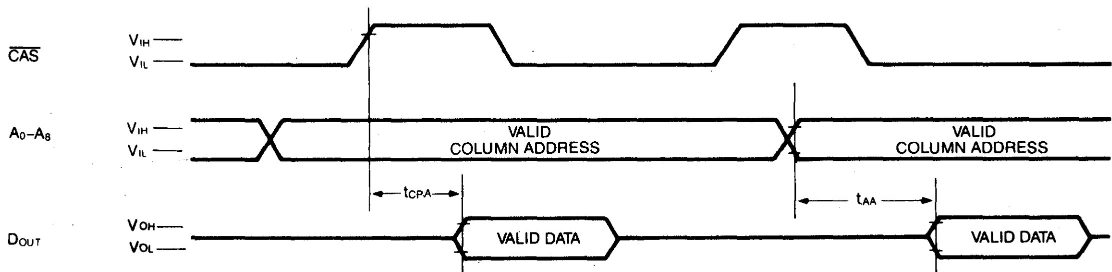
An $\overline{OE}$ low transiton or an $\overline{OE}$ low level enables the output driver when the I/O data path is enabled. An $\overline{OE}$ high transition or an OE high level disables the output driver, but does not disable the data when it has been enabled. A $\overline{WE}$ low level disables the output driver when a $\overline{CAS}$ low level occurs. If the $\overline{WE}$ low transition occurs after the $\overline{CAS}$ low transition such that the output driver is enable prior to the $\overline{WE}$ low transition, it is neccessary to use $\overline{OE}$ to disable the output driver prior to the $\overline{WE}$ low transition to allow data in set-up time(t_{DS}). A $\overline{WE}$ high transition passes control of the output drive to $\overline{OE}$.

POWER ON

An initial pause of 200 μs is required after the application of V_{DD} power supply, followed by a minimum of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh cycle). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

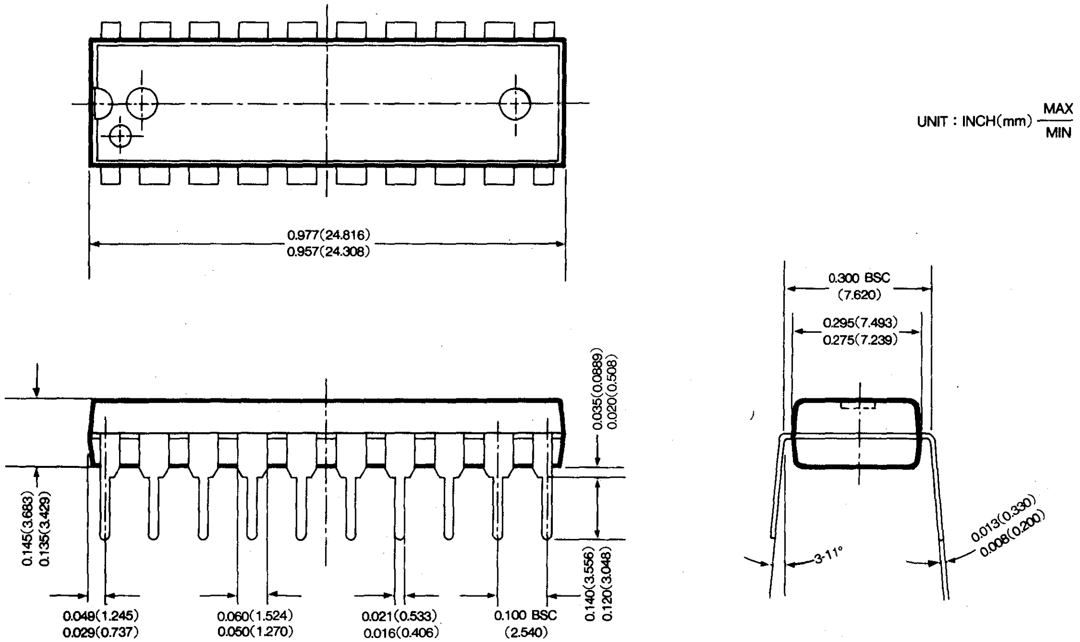
The V_{DD} current (I_{DD}) requirement of the HY534256 during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}=V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.

FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION

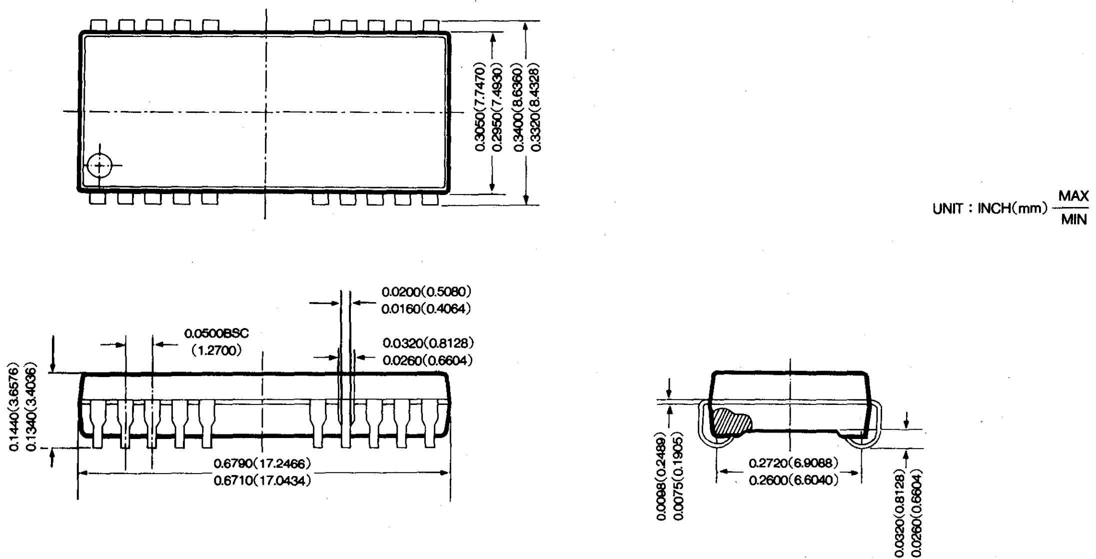


PACKAGE INFORMATION

- **20 PIN PLASTIC DUAL IN LINE PACKAGE – 300 MIL**



- **20/26 PIN SMALL OUTLINE J-FORM PACKAGE**



MEMO

PRELIMINARY

HYUNDAI SEMICONDUCTOR

HY534256A

256K×4-Bit CMOS DRAM

M1C1200A-JAN92

DESCRIPTION

The HY534256A is a high speed, low power 262,144×4 bit CMOS dynamic random access memory. Fabricated with the HYUNDAI CMOS process, the HY534256A offers a fast page mode for high bandwide operation, fast usable speed, CMOS standby current, and inherently high CMOS reliability.

All inputs and outputs are TTL compatible. Fast page mode operation allows random or sequential access of up to 512×4 bits within a row with cycle times as fast as 40ns.

The HY534256A design is optimized for cache based mainframe, minicomputers, graphics, digital signal processing and high performance microprocessor systems.

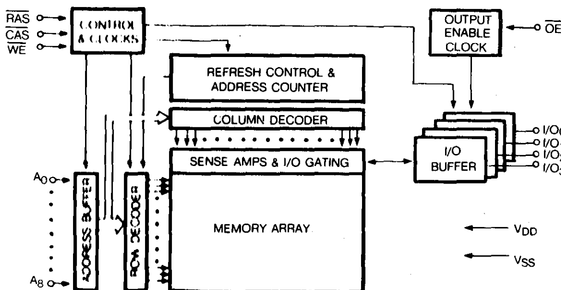
FEATURES

- **Low power dissipation**
  - **Operating current, 60ns : 90mA(max.)**
  - **TTL Standby current : 2mA(max.)**
  - **CMOS Standby Current : 1mA (max.)**
- **Read-Modify-Write capability**
- **$\overline{RAS}$-only, Hidden, $\overline{CAS}$-Before-$\overline{RAS}$ refresh capability**
- **Fast Page mode operation for a sustained data rate up to 25 MHz**
- **512 refresh cycles/8ms**
- **High reliability 300 mil 20 pin P-DIP, 20/26 pin SOJ and 400 mil ZIP.**
- **Fast access time and cycle time (ns)**

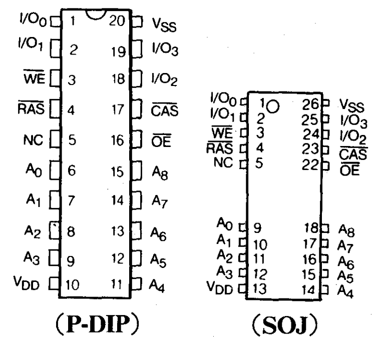
	HY534256A-60	HY534256A-70	HY534256A-80
Max $\overline{RAS}$ Access Time, t_{RAC}	60	70	80
Max $\overline{CAS}$ Access Time, t_{CAC}	20	20	20
Min Fast Page Mode Cycle Time, t_{PC}	40	40	45
Min Cycle Time, t_{RC}	110	130	150

3

BLOCK DIAGRAM



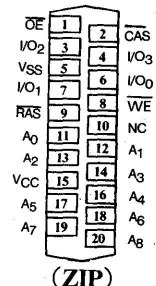
PIN CONNECTIONS



(P-DIP) (SOJ)

PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
A_0-A_8	ADDRESS INPUT
I/O_0-I/O_3	DATA INPUT/OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND



(ZIP)

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_{BIAS}	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	−55 to +150	℃
V_{TERM}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	0.6	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY534256A		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$			10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60		90	mA	1, 2
			−70		80		
			−80		70		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\geq V_{SS}$			2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60		90	mA	2
			−70		80		
			−80		70		
I_{DD4}	V_{DD} Supply Current, Fast page mode	Minimum Cycle	−60		70	mA	1, 2
			−70		60		
			−80		50		
I_{DD5}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS}=V_{IH}$ Other inputs $\geq V_{SS}$			1	mA	
I_{DD6}	V_{DD} Supply Current $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60		90	mA	2
			−70		80		
			−80		70		
V_{IL}	Input Low Voltage(all inputs)			−1	0.8	V	
V_{IH}	Input High Voltage(all inputs)			2.4	V_{DD}+1	V	
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD}(max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions, Specified I_{DD}(max.) is measured with a maximum of of two transitions per address cycle in Fast page mode.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY534256A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	110		120		150		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	40		50		60		ns	
4	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns	
5	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	20	10K	ns	
6	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	15	40	20	50	20	60	ns	
7	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
8	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
9	t_{RAH}	Row Address Hold Time	10		10		10		ns	
10	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
11	t_{CAH}	Column Address Hold Time	15		15		15		ns	
12	t_{RSH}	$\overline{RAS}$ Hold Time	20		20		20		ns	8
13	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	8
14	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	
15	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	
16	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10		10		15		ns	
17	t_{OAC}	Access Time from $\overline{OE}$		20		25		20	ns	3,4,5
18	t_{CAC}	Access Time from $\overline{CAS}$		20		20		20	ns	5, 7
19	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80	ns	3
20	t_{AA}	Access Time from Column Address		30		35		40	ns	11
21	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Output Low Impedance	0		0		0		ns	
22	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to Output High Impedance	0	20	0	20	0	20	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		ns	
24	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	1
25	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		20		ns	
26	t_{WCS}	Write Command Set-up Time	0		0		0		ns	9
27	t_{WCH}	Write Command Hold Time	10		15		15		ns	
28	t_{WP}	Write Command Pulse Width	10		15		15		ns	11
29	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		ns	
30	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		20		ns	
31	t_{DS}	Data-In Set-up Time	0		0		0		ns	10
32	t_{DH}	Data-In Hold Time	10		15		15		ns	10
33	t_{WOH}	Write to $\overline{OE}$ Hold Time	20		20		20		ns	
34	t_{OED}	$\overline{OE}$ to Data Delay	20		20		20		ns	
35	t_{RWC}	Read-Modify-Write(RMW)Cycle-Time	165		185		205		ns	

#	SYMBOL	PARAMETER	HY534256A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	50		50		50		ns	9
37	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	90		100		110		ns	9
38	t_{AWD}	Column Address to $\overline{WE}$ Delay	60		65		70		ns	9
39	t_{PC}	Fast Page Mode Read or Write Cycle Time	40		40		45		ns	
40	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	95		95		100		ns	
41	t_{CP}	$\overline{CAS}$ precharge Time	10		10		10		ns	
42	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		ns	
43	t_{CPA}	Access Time from Column Precharge		35		35		40	ns	12
44	t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50		55		60		ns	
45	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5		5		5		ns	
46	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		ns	
47	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15		15		15		ns	
48	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	13
49	t_{REF}	Refresh Interval(512 Cycle)		8		8		8	ms	
50	t_{RASP}	$\overline{RAS}$ Pulse width(Fast Page Mode)	60	100K	70	100K	80	100K	ns	
51	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40		40		40		ns	

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. t_{RCD}(max.) is specified for reference only. Operation within t_{RCD}(max.) and t_{RAD}(max.) limit insure that t_{RAC}(max.) and t_{AA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD}(max.) then the access time is controlled by t_{AA} and t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.) If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.)
4. Assume $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.)
5. Measured with a load equivalent to two TTL loads and 100pF.
6. Assume that $t_{RCD} \geq t_{RCD}$(max.), $t_{RAD} \leq t_{RAD}$(max.)
7. Assume that $t_{RCD} \leq t_{RCD}$(max.) and $t_{RAD} \geq$(max.)
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : If $t_{WCS} > t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle : if $t_{RWD} > t_{RWD}$(min), $t_{CWD} > t_{CWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), the cycle is a read/write and the data output will contain data from the selected cell : if neither of the above sets of conditions is satisfied, the condition of the data out(at access time) is indeterminate.
10. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$
11. t_{HZ} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
12. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CAP}.
13. V_{IL}(max.) and AC measurements assumen t_T=5ns
14. An initial
15. An initial pause of 200μs is required after power-up and followed by a minimum of 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

3

CAPACITANCE

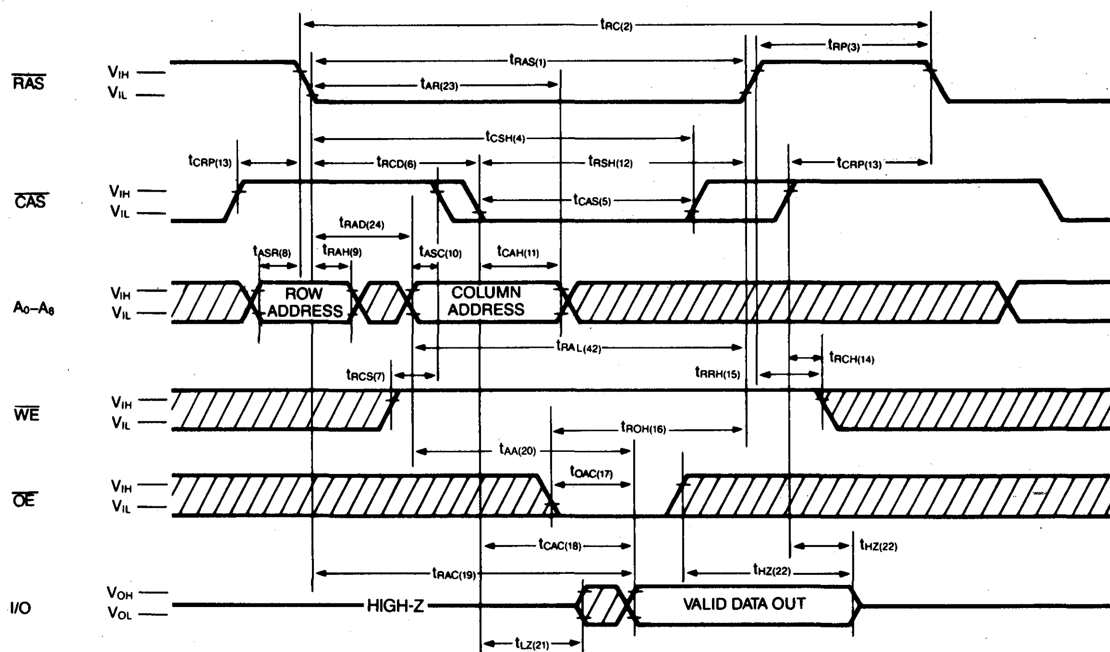
(T_A=25, C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, Data input	–	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	–	7	pF
C_{OUT}	Data Out	–	7	pF

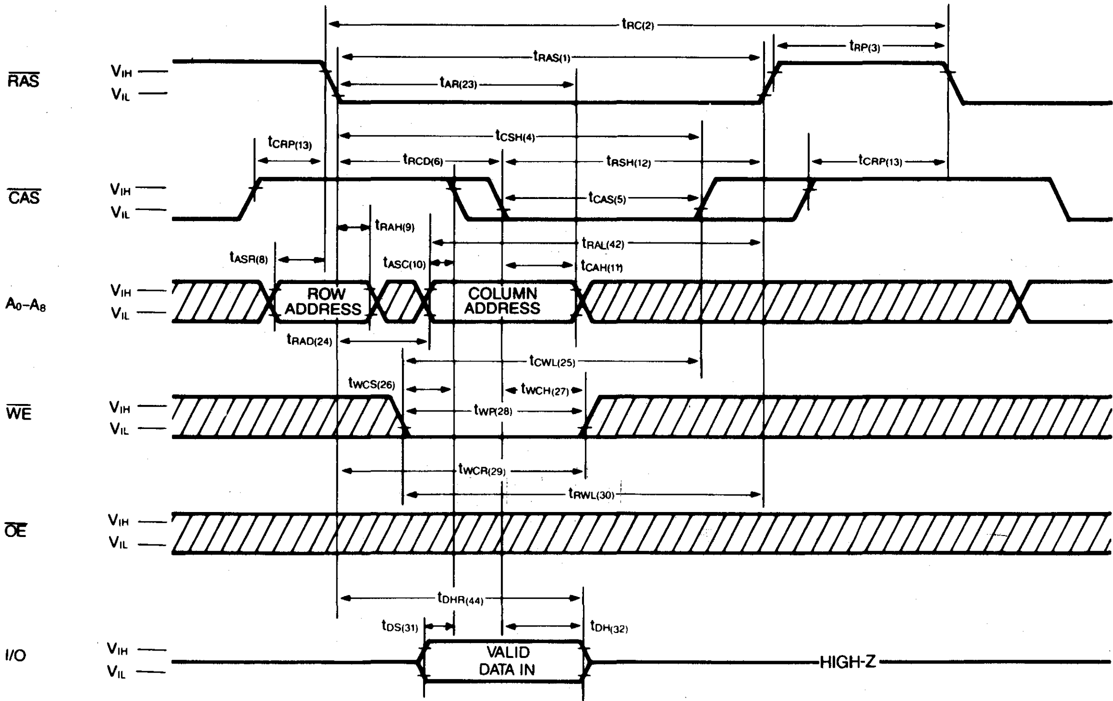
NOTE : Capacitance is measured at worst case of voltage levels with a programmable capacitance meter.

TIMING DIAGRAM

READ CYCLE

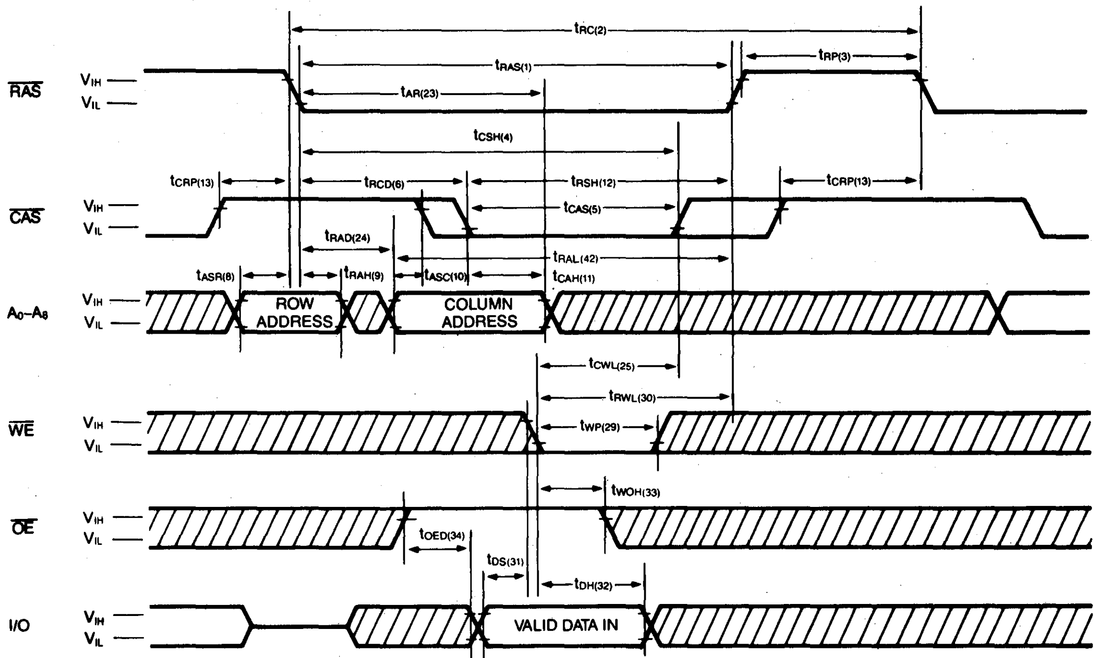


EARLY WRITE CYCLE

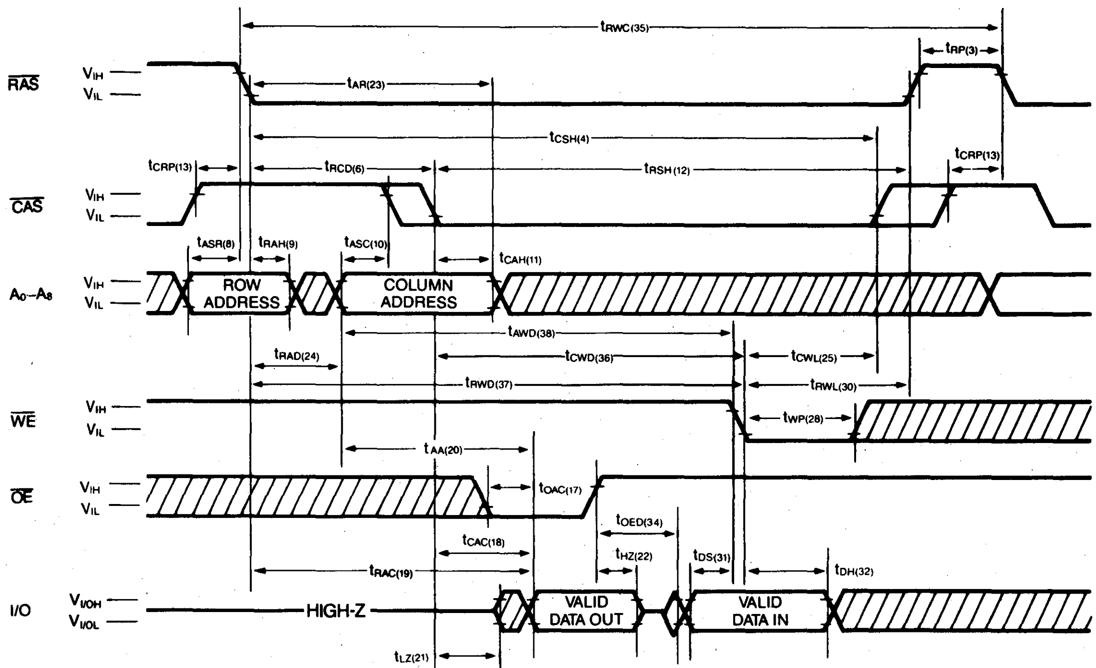


3

WRITE CYCLE ($\overline{OE}$ CONTROLLED)



READ-MODIFY-WRITE CYCLE

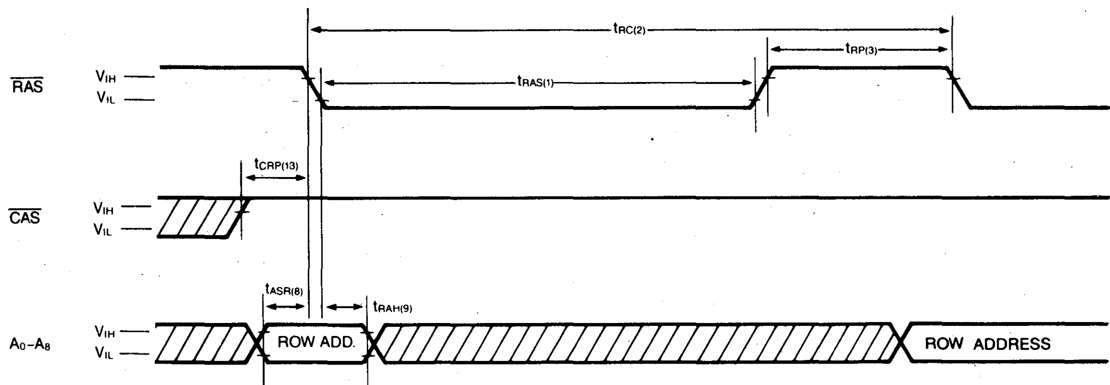


FAST PAGE MODE READ CYCLE

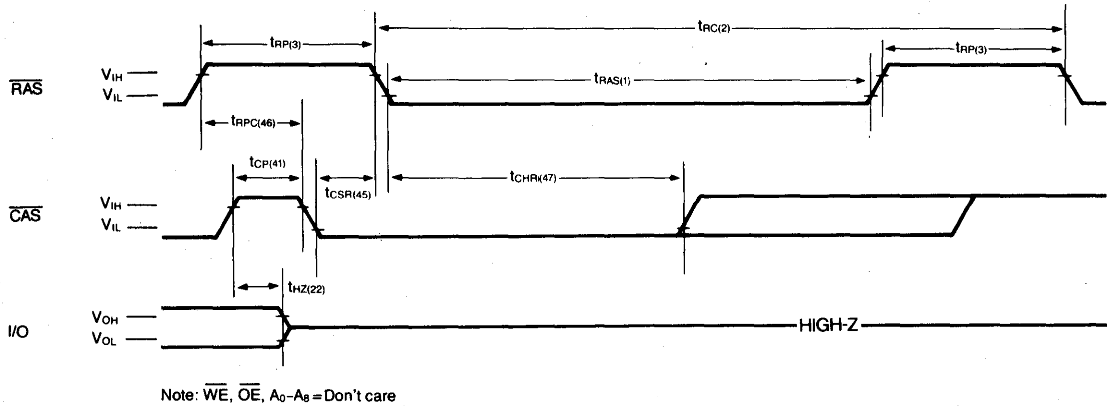
FAST PAGE MODE EARLY WRITE CYCLE

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

RAS-ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$, A_0–A_8 = Don't care

3

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

RAS VIH VIL
tRAS(1)
tRP(3)
tCSR(45)
tCHR(47)
tCPT(51)
tRSH(12)
tCAS(5)
CAS VIH VIL
A0–A8 VIH VIL

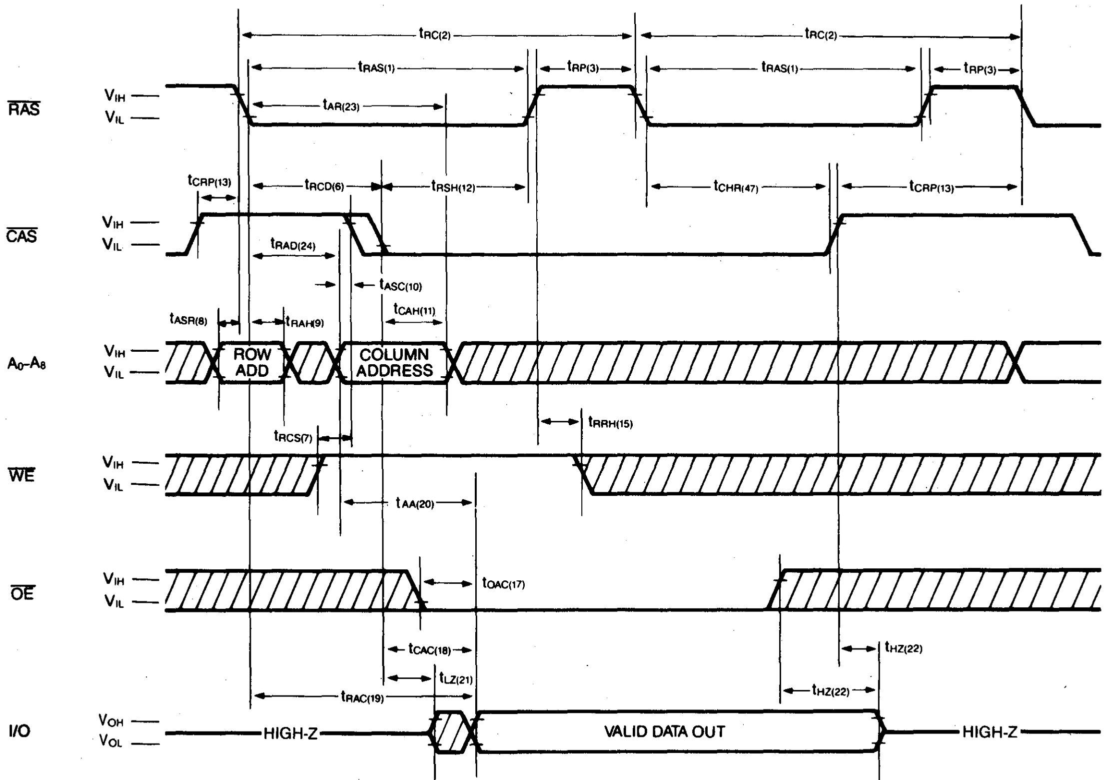
READ CYCLE

tRCS(7)
tRRH(15)
tRCH(14)
WE VIH VIL
tROH(16)
tOAC(17)
OE VIH VIL
tHZ(22)
tLZ(21)
tHZ(22)
I/O VOH VOL
HIGH-Z
DATA OUT

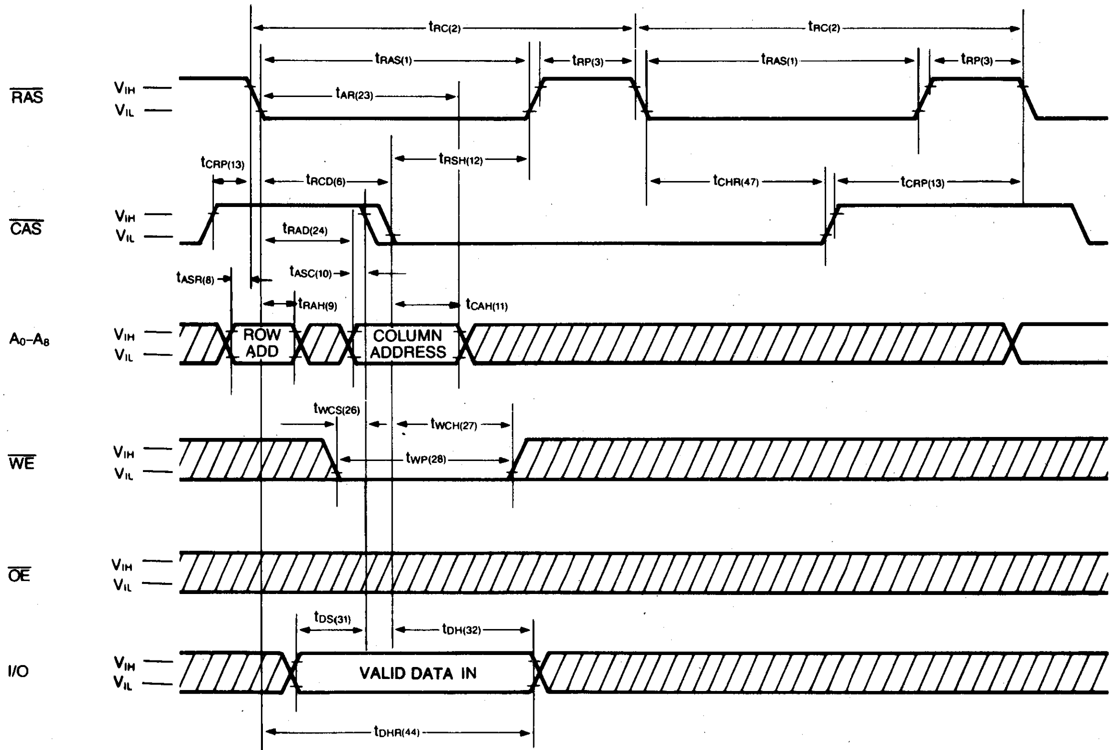
WRITE CYCLE

tRWL(30)
tCWL(25)
tWCS(26)
tWCH(27)
WE VIH VIL
OE VIH VIL
tDS(31)
tDH(32)
I/O VIH VIL
HIGH-Z
VALID DATA IN
HIGH-Z

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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FUNCTIONAL DESCRIPTION

The HY534256A is a CMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The HY534256A reads and writes 4 bits of data at a time by multiplexing a 18 bit address into a 9 bit row and a 9 bit column address. The row address is latched by the Row Address Strobe($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

MEMORY CYCLE

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initi-tiated until the minimum precharge time, t_{RP}, and t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data out is controlled by the Out Enable($\overline{OE}$) and $\overline{CAS}$(See the write cycle description).

Data out becomes valid only when t_{RAC}, t_{AA}, t_{OAC} and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC}, t_{OAC} and t_{CAC} are all satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ low during a $\overline{RAS}$ operation.

The column address is latched by $\overline{CAS}$, The input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Consequently, the write cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the latter of $\overline{WE}$ or $\overline{CAS}$ low transition. In a $\overline{CAS}$ controlled write cycle(the leading edge or $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition)the input/output (I/O) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{CAS}$ going high will maintain the I/O in the high impedance state, terminating with $\overline{WE}$ going high allows the output to go active, and $\overline{OE}$ must be brought high to allow for inputs on the I/O.

The HY534256A incorporates a self-timed write feature which simplifies the system interface and optimizes data bandwidth. After the write funcition has been initiated, the HY534256A internally completes the write action and unlatches the address and data latches. Thus, the latches are ready for the next input/output cycle. This eliminates the need for long address and data hold times during the write operation and allows a subsequent column address to be applied earlier. This minimizes a write pulse width, write precharge time, and hold time which provides maximum flexibility in system design.

REFRESH CYCLE

To retain data, 512 $\overline{RAS}$ refresh cycle are required in an 8 ms period. The refresh operation can be performed two ways :

1. Clocking each of 512 row address(A_0 through A_8) with $\overline{RAS}$ at least every 8 ms period. Any combination of $\overline{RAS}$ cycle such as read, write, read-modify-write, or $\overline{RAS}$-only refresh cycle will perform a refresh.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle : If $\overline{CAS}$ go low prior to $\overline{RAS}$ go low, the chip enters $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The HY534256A will use an internal nine bits counter output as the source of the row address and will ignore the external address inputs.

This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh only mode and no data access is

allowed. Also, the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle does not cause device selection and the state of the data output pin will remain in a high impedance state.

In order to guarantee the reliable operation of $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, an internal counter test mode is provided. The user can use the counter test mode to write in a data pattern consecutively (512 write cycles) and, then verify the data which has been written by 512 consecutive read cycles.

DATA RETENTION MODE

The HY534256A offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY534256A power consumption is reduced to the low I_{DD5} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows :

$$I = \frac{(t_{RC}) \times (I\ active) + (t_{RX} - t_{RC}) \times (I_{DD5})}{t_{RX}}$$

Where t_{RC}=Refersh Cycle Time
t_{RX}=Refresh Interval/512

FAST PAGE MODE OPERATION

Fast page mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while sucessive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as transparent or flow through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into column address buffer and acts as an output enable.

During this operation, read, write, and read-modify-write, or read-write-read cycles are possible at random or sequential address within a low. Following the entry cycle into fast page mode, access time is t_{AA} or t_{CAP} dependent. It the column address is valid prior to or coincident by t_{CAP} as shown in figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{AA}, For both cases, the falling edge of $\overline{CAS}$ latches the address and enable the output.

Fast page mode provides a sustanined data rate over 25 MHz for applications that require high data rate such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate :

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

DATA OUT OPERATION

The HY534256A input/output(I/O) is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables data to transfer into and from a selected row address. A $\overline{RAS}$ high transition disables data transfer and will latch the output data if the output is enabled. After a memory cycle is initiated by a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or a $\overline{CAS}$ low level enables the internal I/O data. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O data path and disables the output driver if the driver was enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path, nor on the output driver.

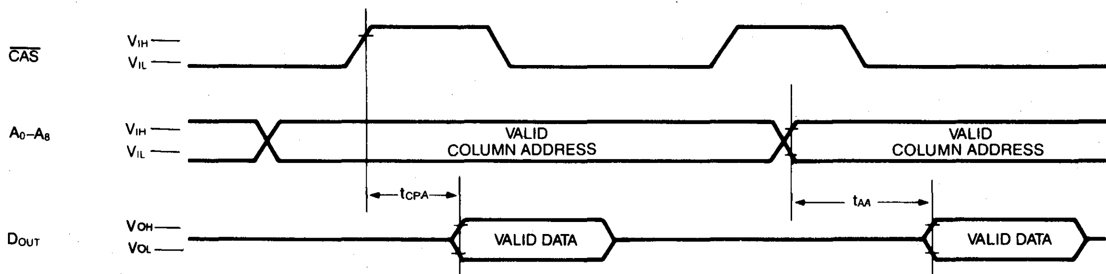
An $\overline{OE}$ low transiton or an $\overline{OE}$ low level enables the output driver when the I/O data path is enabled. An $\overline{OE}$ high transition or an OE high level disables the output driver, but does not disable the data when it has been enabled. A $\overline{WE}$ low level disables the output driver when a $\overline{CAS}$ low level occurs. If the $\overline{WE}$ low transition occurs after the $\overline{CAS}$ low transition such that the output driver is enable prior to the $\overline{WE}$ low transition, it is neccessary to use $\overline{OE}$ to disable the output driver prior to the $\overline{WE}$ low transition to allow data in set-up time(t_{DS}). A $\overline{WE}$ high transition passes control of the output drive to $\overline{OE}$.

POWER ON

An initial pause of 200 μs is required after the application of V_{DD} power supply, followed by a minimum of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh cycle). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

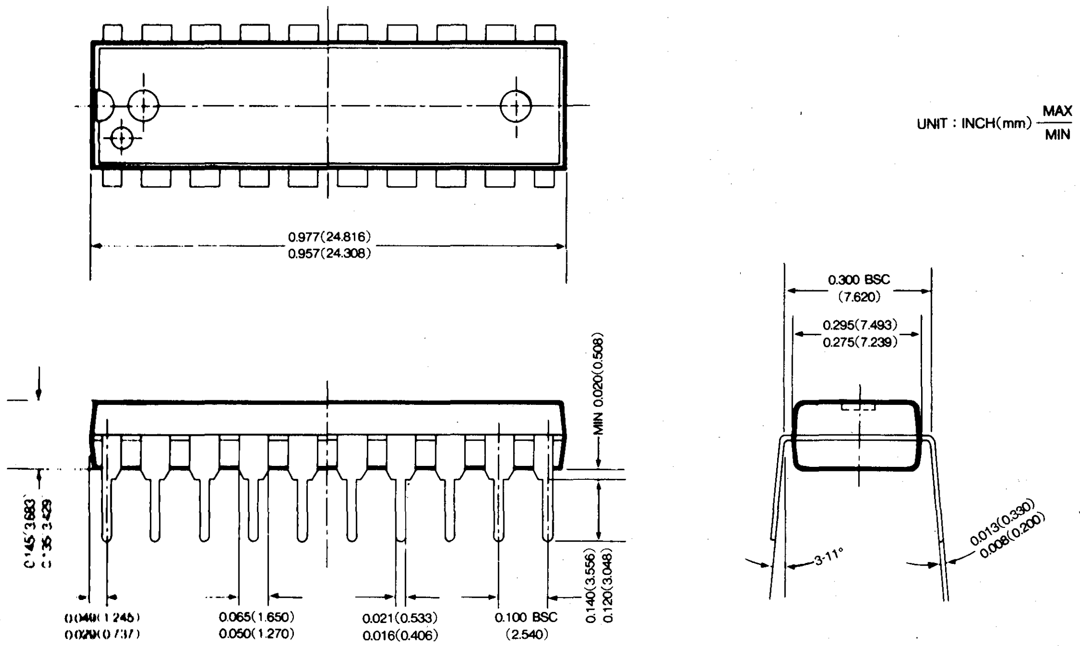
The V_{DD} current (I_{DD}) requirement of the HY534256A during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}=V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.

FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION



PACKAGE INFORMATION

• 20 PIN PLASTIC DUAL IN LINE PACKAGE − 300 MIL



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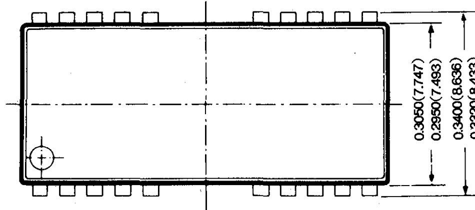
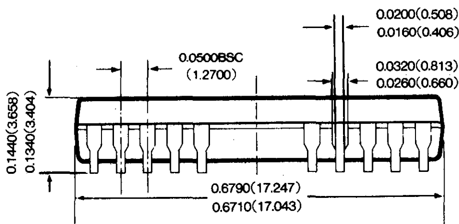
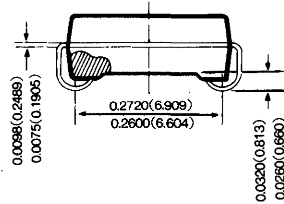
• 20/26 PIN SMALL OUTLINE J-FORM PACKAGE – 300 MIL



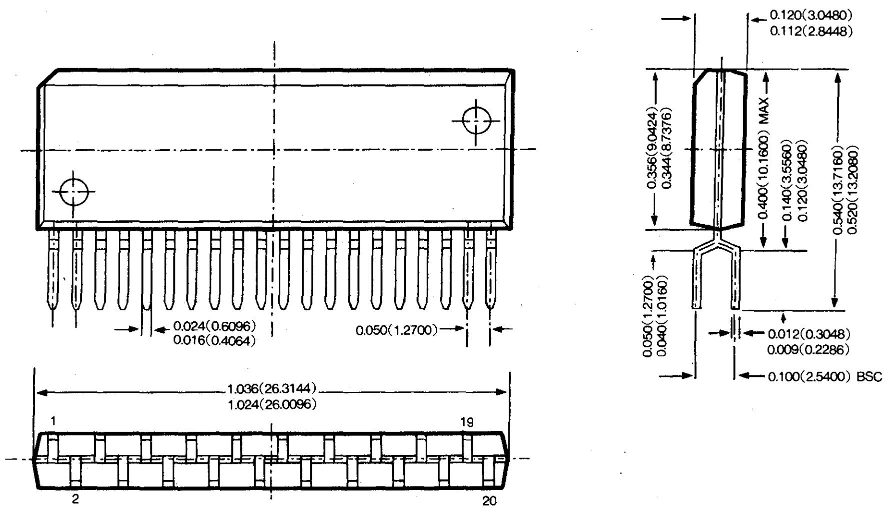
UNIT : INCH(mm) MAX/MIN





- **20 PIN ZIGZAG-IN-LINE PACKAGE−400MIL**

UNIT : INCH(mm) MAX/MIN



MEMO

HY534256AL

256K×4-Bit CMOS DRAM

M1D1200A-JAN92

DESCRIPTION

The HY534256AL is a high speed, low power 262,144×4 bit CMOS dynamic random access memory. Fabricated with the HYUNDAI CMOS process, the HY534256AL offers a fast page mode for high bandwide operation, fast usable speed, CMOS standby current and inherently high CMOS reliability.

All inputs and outputs are TTL compatible. Fast page mode operation allows random or sequential access of up to 512×4 bits within a row with cycle times as fast as 40ns.

The HY534256AL design is optimized for cache based mainframe, minicomputers, graphics, digital signal processing high performance microprocessor systems and note book pc.

FEATURES

- **Low power dissipation**
  - **Operating current, 60ns : 90mA(max.)**
  - **TTL Standby current : 2mA(max.)**
  - **CMOS Standby Current : 200μA(max.)**
  - **Battery Back Up Current : 300μA(max.)**
- **Read-Modify-Write capability**
- **$\overline{RAS}$-only, Hidden, $\overline{CAS}$-Before-$\overline{RAS}$ refresh capability**
- **Fast Page mode operation for a sustained data rate up to 25 MHz**
- **512 refresh cycles/64ms**
- **High reliability 300 mil 20 pin P-DIP, 20/26 pin SOJ and 400 mil ZIP**
- **Fast access time and cycle time (ns)**

	HY534256AL-60	HY534256AL-70	HY534256AL-80
Max $\overline{RAS}$ Access Time, t_{RAC}	60	70	80
Max $\overline{CAS}$ Access Time, t_{CAC}	20	20	20
Min Fast Page Mode Cycle Time, t_{PC}	40	40	45
Min Cycle Time, t_{RC}	110	130	150

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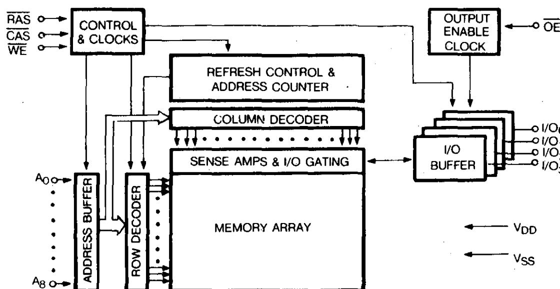
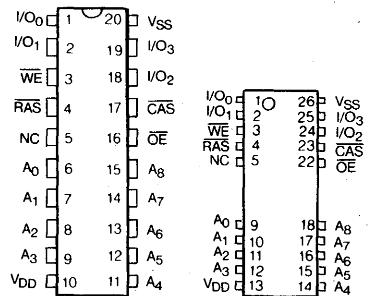
BLOCK DIAGRAM

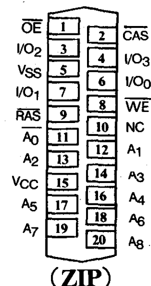


PIN CONNECTIONS



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
A_0-A_8	ADDRESS INPUT
I/O_0-I/O_3	DATA INPUT/OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_{BIAS}	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	−55 to +150	℃
V_{TERM}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	0.6	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY534256AL		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$			10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60		90	mA	1, 2
			−70		80		
			−80		70		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs$\geq V_{SS}$			2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60		90	mA	2
			−70		80		
			−80		70		
I_{DD4}	V_{DD} Supply Current, Fast page mode	Minimum Cycle	−60		70	mA	1, 2
			−70		60		
			−80		50		
I_{DD5}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$\overline{RAS}=\overline{CAS}=V_{CC}-0.2V$			200	μA	
I_{DD6}	V_{DD} Supply Current $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60		90	mA	2
			−70		80		
			−80		70		
I_{DD7}	V_{DD} Supply Current, Battery Back up	$\overline{CAS}$=CBR cycling or 0.2V, $\overline{OE}=\overline{WE}=V_{DD}-0.2V$, Add=$V_{DD}$−0.2V or 0.2V, I/O=$V_{DD}$−0.2V or 0.2V or open, t_{RC}=125μs, $t_{RAS}=t_{RAS}$(min.) ~300ns			300	μA	1
		Same as above except t_{RAS}=300ns~1μs			400	μA	
V_{IL}	Input Low Voltage(all inputs)			−1	0.8	V	
V_{IH}	Input High Voltage(all inputs)			2.4	V_{DD}+1	V	
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD}(max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions, Specified I_{DD}(max.) is measured with a maximum of of two transitions per address cycle in Fast page mode.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY534256AL 60 MIN.	60 MAX.	70 MIN.	70 MAX.	80 MIN.	80 MAX.	UNIT	NOTE
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	110		120		150		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	40		50		60		ns	
4	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns	
5	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	20	10K	ns	
6	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	15	40	20	50	20	60	ns	
7	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
8	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
9	t_{RAH}	Row Address Hold Time	10		10		10		ns	
10	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
11	t_{CAH}	Column Address Hold Time	15		15		15		ns	
12	t_{RSH}	$\overline{RAS}$ Hold Time	20		20		20		ns	8
13	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	8
14	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	
15	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	
16	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10		10		15		ns	
17	t_{OAC}	Access Time from $\overline{OE}$		20		25		20	ns	3,4,5
18	t_{CAC}	Access Time from $\overline{CAS}$		20		20		20	ns	5, 7
19	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80	ns	3
20	t_{AA}	Access Time from Column Address		30		35		40	ns	11
21	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Output Low Impedance	0		0		0		ns	
22	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to Output High Impedance	0	20	0	20	0	20	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		ns	
24	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	1
25	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		20		ns	
26	t_{WCS}	Write Command Set-up Time	0		0		0		ns	9
27	t_{WCH}	Write Command Hold Time	10		15		15		ns	
28	t_{WP}	Write Command Pulse Width	10		15		15		ns	11
29	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		ns	
30	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		20		ns	
31	t_{DS}	Data-In Set-up Time	0		0		0		ns	10
32	t_{DH}	Data-In Hold Time	10		15		15		ns	10
33	t_{WOH}	Write to $\overline{OE}$ Hold Time	20		20		20		ns	
34	t_{OED}	$\overline{OE}$ to Data Delay	20		20		20		ns	
35	t_{RWC}	Read-Modify-Write(RMW)Cycle-Time	165		185		205		ns	

#	SYMBOL	PARAMETER	HY534256AL						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	50		50		50		ns	9
37	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	90		100		110		ns	9
38	t_{AWD}	Column Address to $\overline{WE}$ Delay	60		65		70		ns	9
39	t_{PC}	Fast Page Mode Read or Write Cycle Time	40		40		45		ns	
40	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	95		95		100		ns	
41	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
42	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		ns	
43	t_{CPA}	Access Time from Column Precharge		35		35		40	ns	12
44	t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50		55		60		ns	
45	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5		5		5		ns	
46	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		ns	
47	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15		15		15		ns	
48	t_{T}	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	13
49	t_{REF}	Refresh Interval(512 Cycle)		64		64		64	ms	
50	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	100K	70	100K	80	100K	ns	
51	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40		40		40		ns	

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. t_{RCD}(max.) is specified for reference only. Operation within t_{RCD}(max.) and t_{RAD}(max.) limit insure that t_{RAC}(max.) and t_{AA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD}(max.) then the access time is controlled by t_{AA} and t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.) If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.)
4. Assume $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.)
5. Measured with a load equivalent to two TTL loads and 100pF.
6. Assume that $t_{RCD} \geq t_{RCD}$(max.), $t_{RAD} \leq t_{RAD}$(max.)
7. Assume that $t_{RCD} \leq t_{RCD}$(max.) and $t_{RAD} \geq$(max.)
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : If $t_{WCS} > t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle : if $t_{RWD} > t_{RWD}$(min), $t_{CWD} > t_{CWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), the cycle is a read/write and the data output will contain data from the selected cell : if neither of the above sets of conditions is satisfied, the condition of the data out(at access time) is indeterminate.
10. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$
11. t_{HZ} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
12. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CAP}.
13. V_{IL}(max.) and AC measurements assumen t_T=5ns
14. An initial
15. An initial pause of 200μs is required after power-up and followed by a minimum of 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

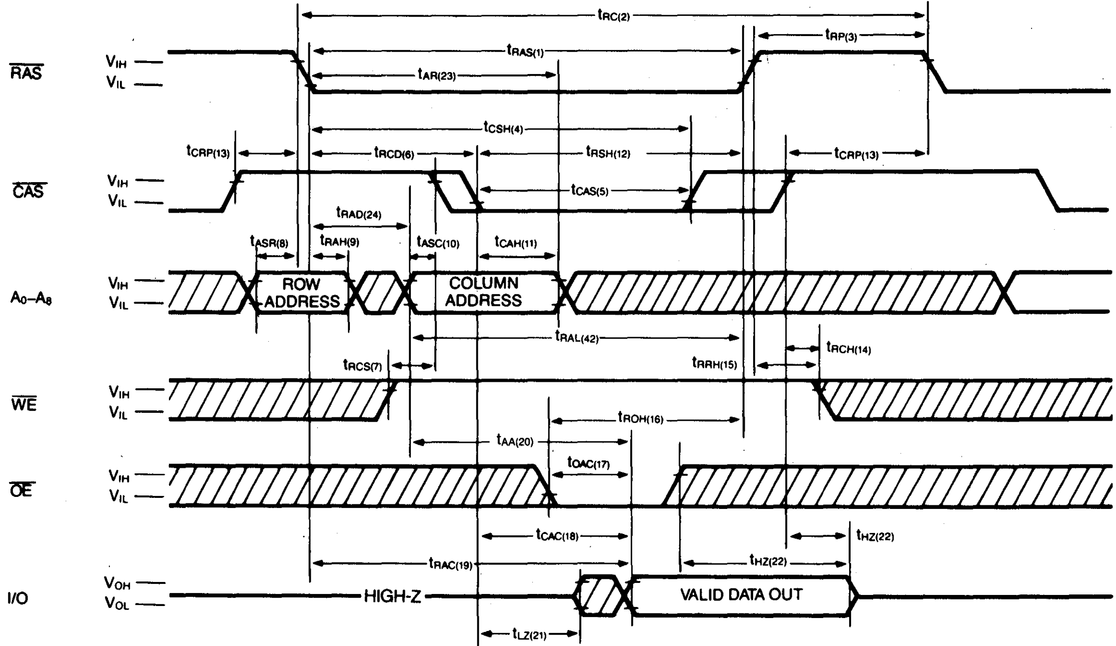
CAPACITANCE
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Address, Data input	–	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	–	7	pF
C_{OUT}	Data Out	–	7	pF

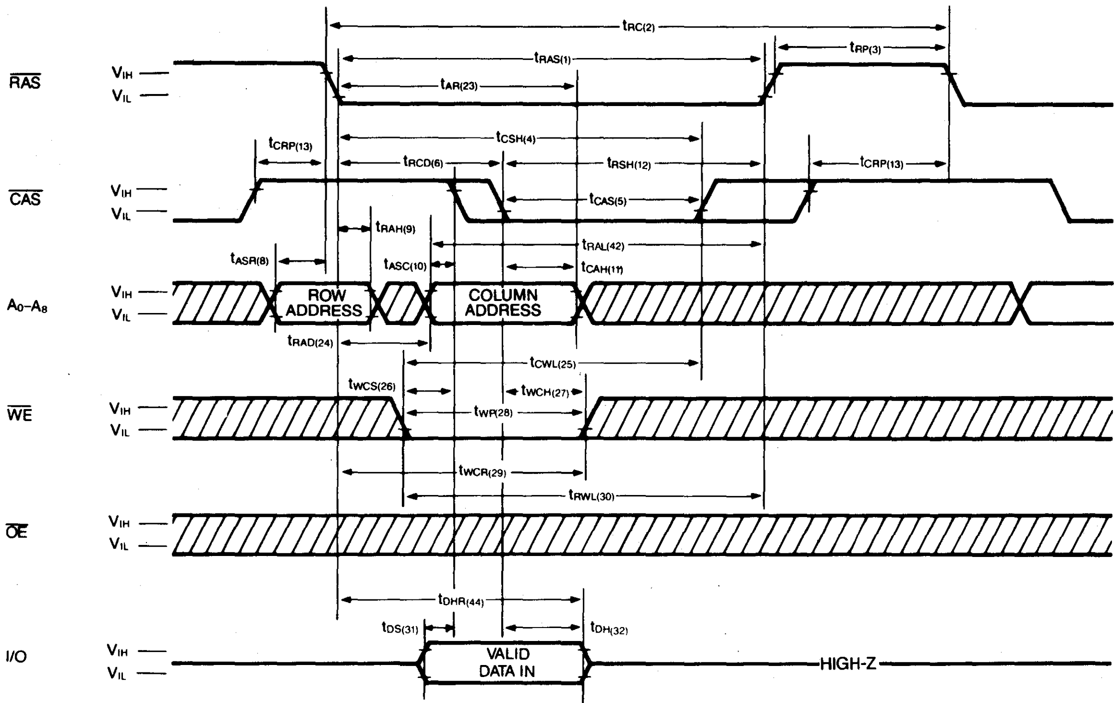
NOTE : Capacitance is measured at worst case of voltage levels with a programmable capacitance meter.

TIMING DIAGRAM

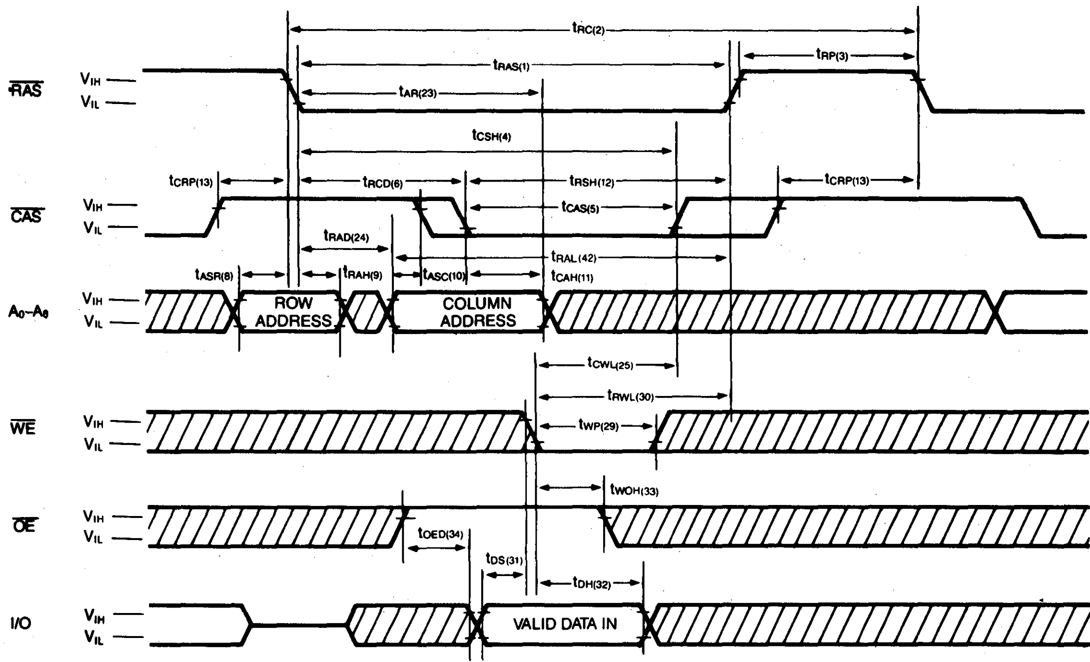
READ CYCLE



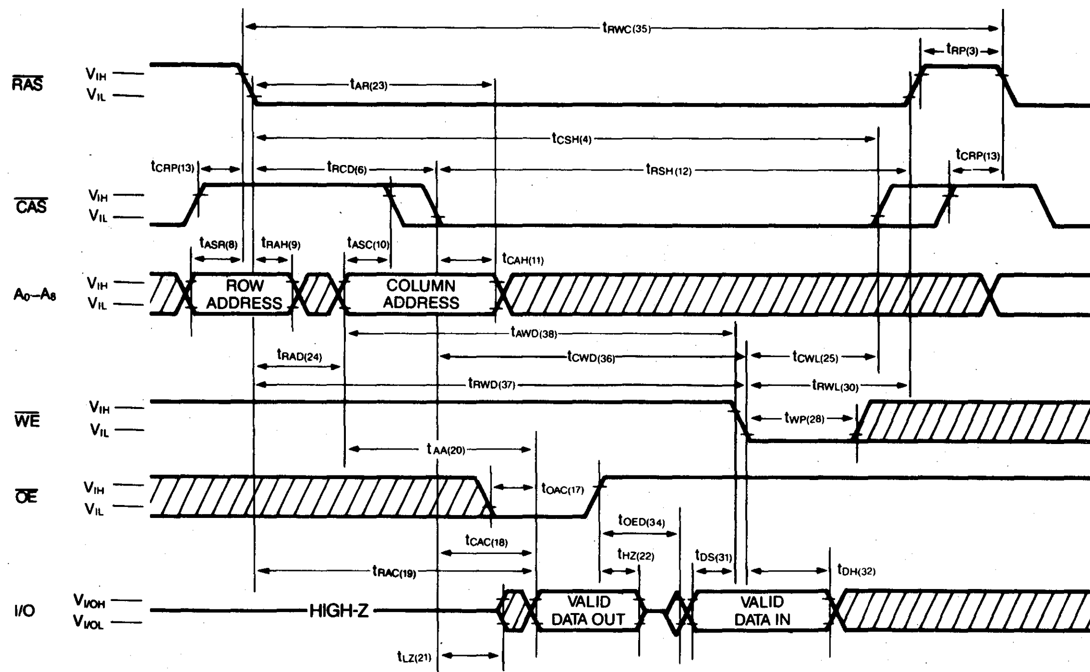
EARLY WRITE CYCLE



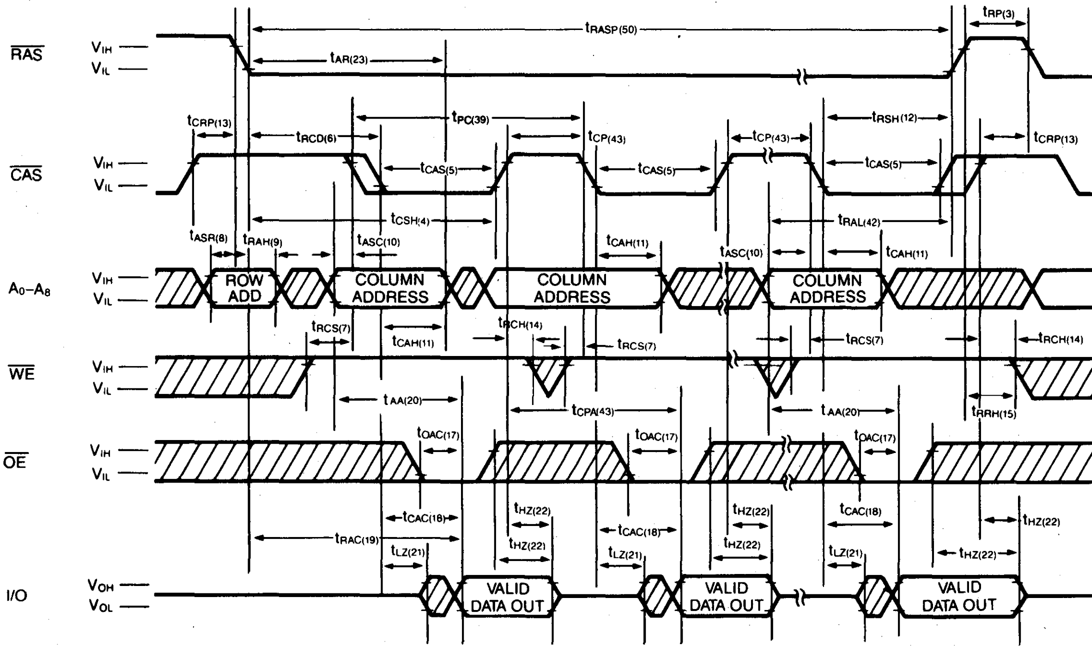
WRITE CYCLE ($\overline{OE}$ CONTROLLED)



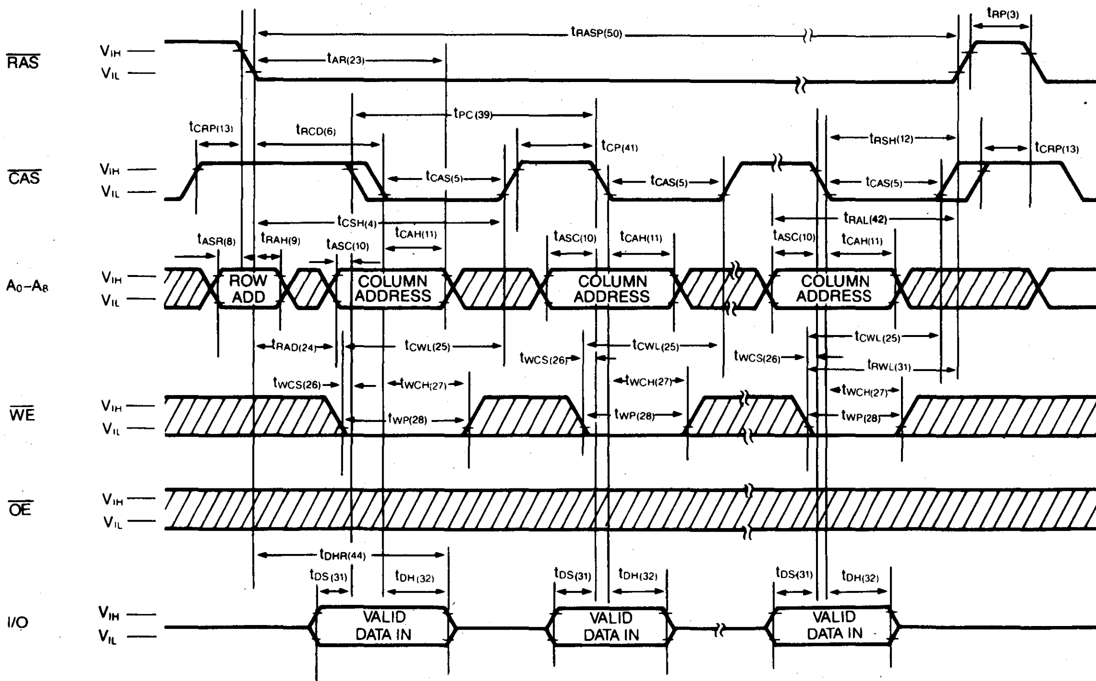
READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE



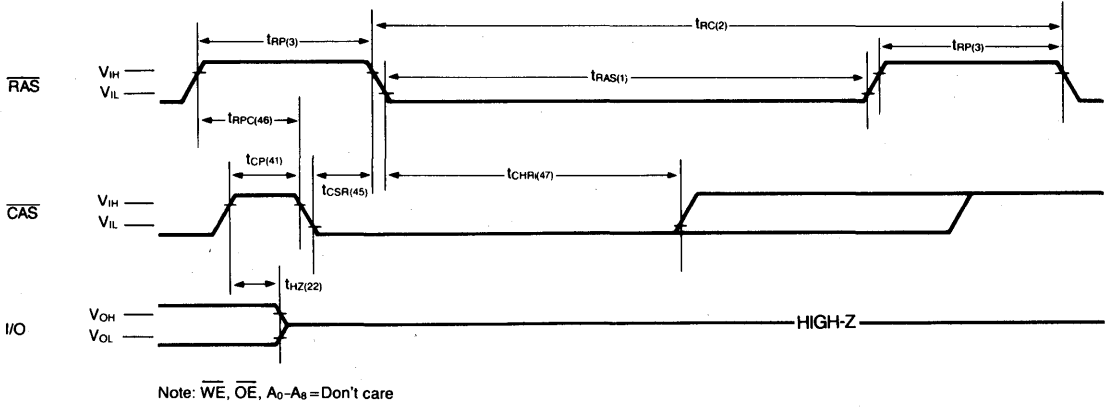
FAST PAGE MODE READ-MODIFY-WRITE CYCLE

RAS VIH VIL tRASP(1) tRP(3) tCSH(4) tRCD(6) tPCM(44) tRSH(12) tCP(41) tCRP(13)
CAS VIL VIH tRAD(24) tRAH(9) tCAH(11) tASC(10) tRAL(42) tASR(8)
A0–A8 VIH VIL ROW ADD COLUMN ADD COL ADD
tRWD(37) tRWL(30) tRCS(7) tCWD(36) tCWL(25)
WE VIH VIL tAWD(38) tAA(20) tWP(28) tOAC(17)
OE VIH VIL tOED(34) tCPA(43) tCAC(18) tHZ(22) tRAC(19) tDH(32) tCAA(20) tDS(31)
I/O VI/OH VI/OL OUT IN tLZ(21)

RAS-ONLY REFRESH CYCLE

RAS VIH VIL tRC(2) tRP(3) tRAS(1)
CAS VIH VIL tCRP(13)
A0–A8 VIH VIL tASR(8) tRAH(9) ROW ADD ROW ADDRESS

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



Note: $\overline{WE}$, $\overline{OE}$, A_0–A_8 = Don't care

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

$\overline{RAS}$ tRAS(1) tRP(3)

$\overline{CAS}$ tCSR(45) tCHR(47) tCPT(51) tRSH(12) tCAS(5)

A_0–A_8

READ CYCLE

tRCS(7) tRRH(15) tRCH(14) tROH(16) tOAC(17) tLZ(21) tHZ(22)

$\overline{WE}$

$\overline{OE}$

I/O HIGH-Z DATA OUT

WRITE CYCLE

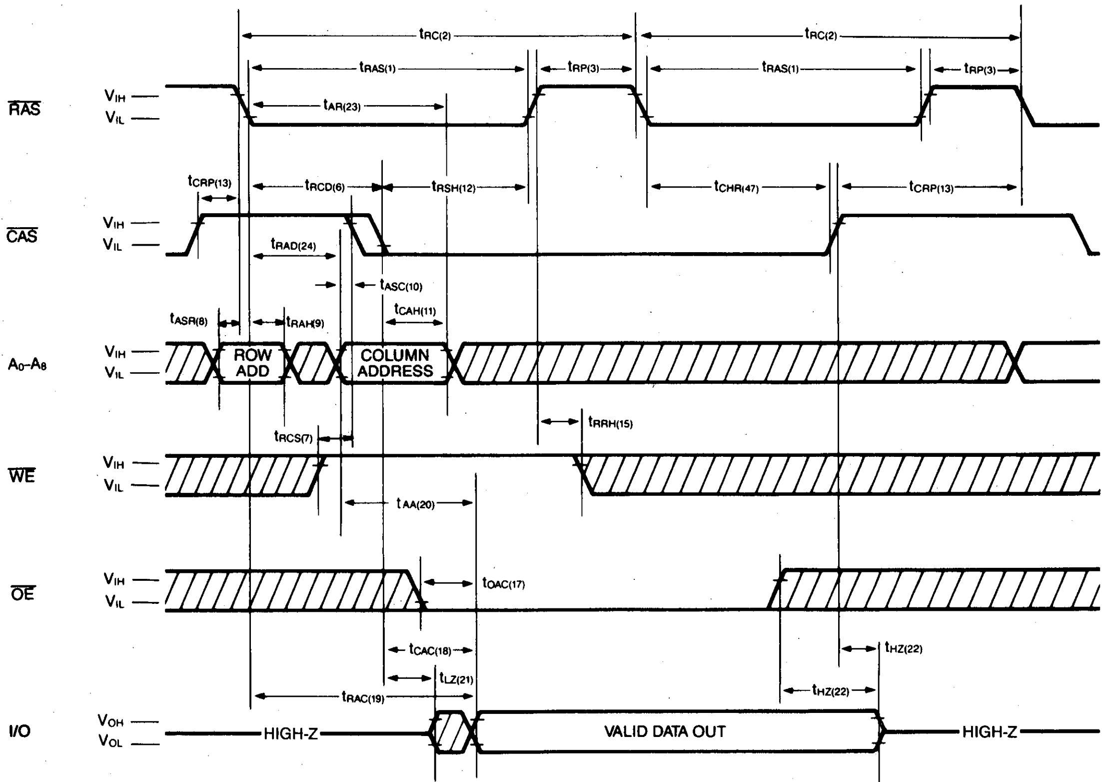
tRWL(30) tCWL(25) tWCS(26) tWCH(27) tDS(31) tDH(32)

$\overline{WE}$

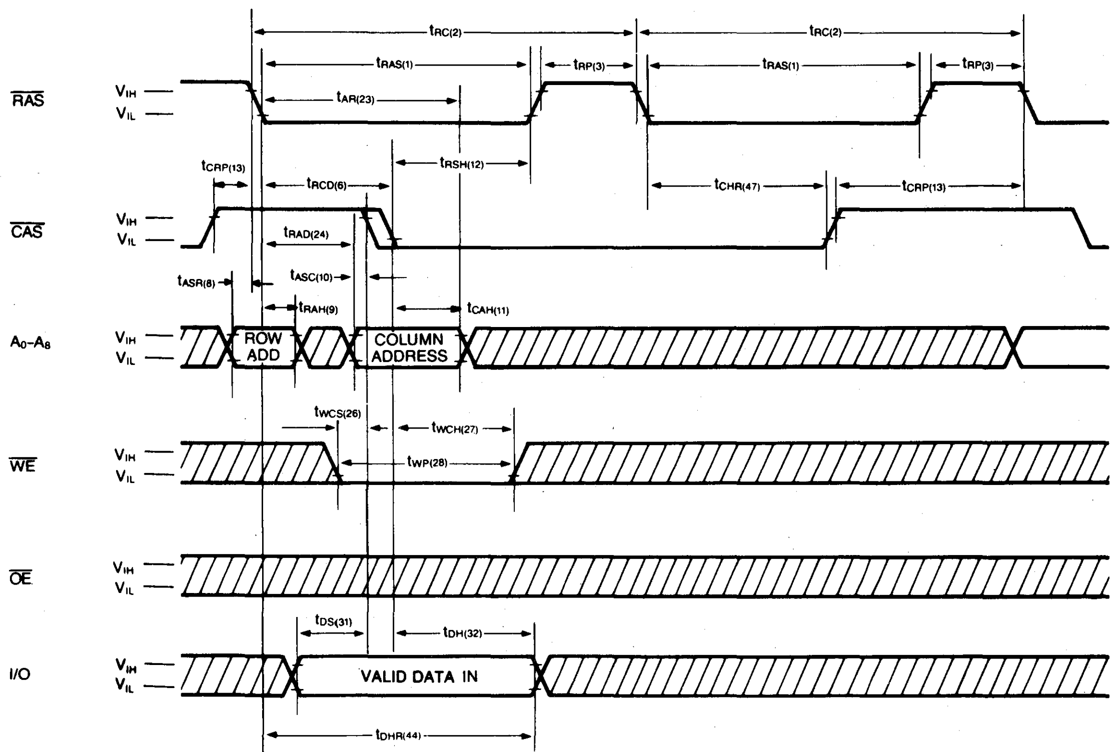
$\overline{OE}$

I/O HIGH-Z VALID DATA IN HIGH-Z

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



FUNCTIONAL DESCRIPTION

The HY534256AL is a CMOS dynamic RAM optimized for high data bandwidth and low power applications. The functionality is similar to a traditional dynamic RAM. The HY534256AL reads and writes 4 bits of data at a time by multiplexing a 18 bit address into a 9 bit row and a 9 bit column address. The row address is latched by the Row Address Strobe($\overline{RAS}$). The column address, however, flows through the internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address, the delay time between $\overline{RAS}$ and $\overline{CAS}$ can be long without affecting the access time.

MEMORY CYCLE

The memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle once initiated must not be ended or aborted prior to fulfilling the minimum t_{RAS} timing specification. This ensures proper device operation and data integrity. Additionally, a new cycle cannot be initiated until the minimum precharge time, t_{RP}, and t_{CP} has elapsed.

READ CYCLE

A read cycle is performed by maintaining the Write Enable ($\overline{WE}$) signal high during the $\overline{RAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data out is controlled by the Out Enable($\overline{OE}$) and $\overline{CAS}$(See the write cycle description).

Data out becomes valid only when t_{RAC}, t_{AA}, t_{OAC} and t_{CAC} are all satisfied. Consequently, the access time is dependent upon the timing relationship among t_{RAC}, t_{OAC} and t_{CAC} are all satisfied.

WRITE CYCLE

A write cycle is performed by taking $\overline{WE}$ low during a $\overline{RAS}$ operation.

The column address is latched by $\overline{CAS}$, The input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Consequently, the write cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending upon the latter of $\overline{WE}$ or $\overline{CAS}$ low transition. In a $\overline{CAS}$ controlled write cycle(the leading edge or $\overline{WE}$ occurs prior to or coincident with the $\overline{CAS}$ low transition)the input/output (I/O) pin will be in the high impedance state at the beginning of the write function. Terminating the write action with $\overline{CAS}$ going high will maintain the I/O in the high impedance state, terminating with $\overline{WE}$ going high allows the output to go active, and $\overline{OE}$ must be brought high to allow for inputs on the I/O.

The HY534256AL incorporates a self-timed write feature which simplifies the system interface and optimizes data bandwidth. After the write funcition has been initiated, the HY534256AL internally completes the write action and unlatches the address and data latches. Thus, the latches are ready for the next input/output cycle. This eliminates the need for long address and data hold times during the write operation and allows a subsequent column address to be applied earlier. This minimizes a write pulse width, write precharge time, and hold time which provides maximum flexibility in system design.

REFRESH CYCLE

To retain data, 512 $\overline{RAS}$ refresh cycle are required in an 64 ms period. The refresh operation can be performed two ways :

1. Clocking each of 512 row address(A_0 through A_8) with $\overline{RAS}$ at least every 64 ms period. Any combination of $\overline{RAS}$ cycle such as read, write, read-modify-write, or $\overline{RAS}$-only refresh cycle will perform a refresh.
2. $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle : If $\overline{CAS}$ go low prior to $\overline{RAS}$ go low, the chip enters $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. The HY534256 will use an internal nine bits counter output as the source of the row address and will ignore the external address inputs.

This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh only mode and no data access is

allowed. Also, the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle does not cause device selection and the state of the data output pin will remain in a high impedance state.

In order to guarantee the reliable operation of $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, an internal counter test mode is provided. The user can use the counter test mode to write in a data pattern consecutively (512 write cycles) and, then verify the data which has been written by 512 consecutive read cycles.

DATA RETENTION MODE

The HY534256AL offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the HY534256AL power consumption is reduced to the low I_{DD5} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows :

$$I=\frac{(t_{RC})\times(I\ active)+(t_{RX}-t_{RC})\times(I_{DD5})}{t_{RX}}$$

Where t_{RC} = Refersh Cycle Time
t_{RX} = Refresh Interval/512

FAST PAGE MODE OPERATION

Fast page mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while sucessive $\overline{CAS}$ cycles are performed retains the row address internally, eliminating the need to reapply it. The column address buffer acts as transparent or flow through latch while $\overline{CAS}$ is high. Access begins from the valid column address rather than from $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into column address buffer and acts as an output enable.

During this operation, read, write, and read-modify-write or read-write-read cycles are possible at random or sequential address within a low. Following the entry cycle into fast page mode, access time is t_{AA} or t_{CAP} dependent. It the column address is valid prior to or coincident by t_{CAP} as shown in figure 1. If the column address is valid after the rising edge of $\overline{CAS}$, then the access time is determined by the valid column address specified by t_{AA}, For both cases, the falling edge of $\overline{CAS}$ latches the address and enable the output.

Fast page mode provides a sustanined data rate over 25 MHz for applications that require high data rate such as bit mapped graphics or high speed signal processing. The following equation can be used to calculate the data rate :

$$\text{Data Rate}=\frac{512}{t_{RC}+511\times t_{PC}}$$

DATA OUTPUT OPERATION

The HY534256AL input/output(I/O) is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables data to transfer into and from a selected row address. A $\overline{RAS}$ high transition disables data transfer and will latch the output data if the output is enabled. After a memory cycle is initiated by a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or a $\overline{CAS}$ low level enables the internal I/O data. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O data path and disables the output driver if the driver was enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path, nor on the output driver.

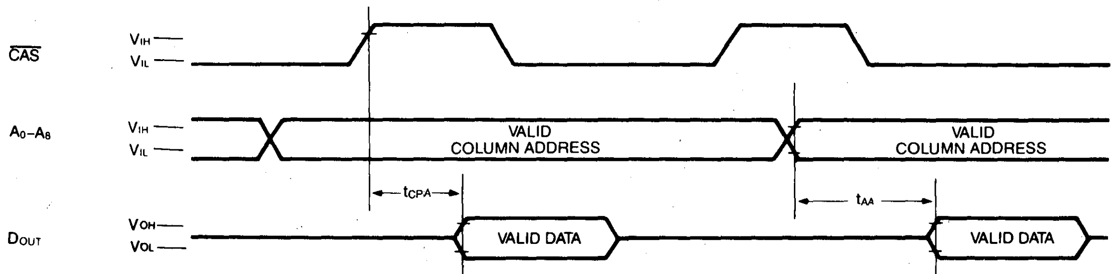
An $\overline{OE}$ low transiton or an $\overline{OE}$ low level enables the output driver when the I/O data path is enabled. An $\overline{OE}$ high transition or an OE high level disables the output driver, but does not disable the data when it has been enabled. A $\overline{WE}$ low level disables the output driver when a $\overline{CAS}$ low level occurs. If the $\overline{WE}$ low transition occurs after the $\overline{CAS}$ low transition such that the output driver is enable prior to the $\overline{WE}$ low transition, it is neccessary to use $\overline{OE}$ to disable the output driver prior to the $\overline{WE}$ low transition to allow data in set-up time(t_{DS}). A $\overline{WE}$ high transition passes control of the output drive to $\overline{OE}$.

POWER ON

An initial pause of 200 μs is required after the application of V_{DD} power supply, followed by a minimum of eight initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh cycle). Eight initialization cycles are required after extended periods of bias without clocks(greater than the refresh interval).

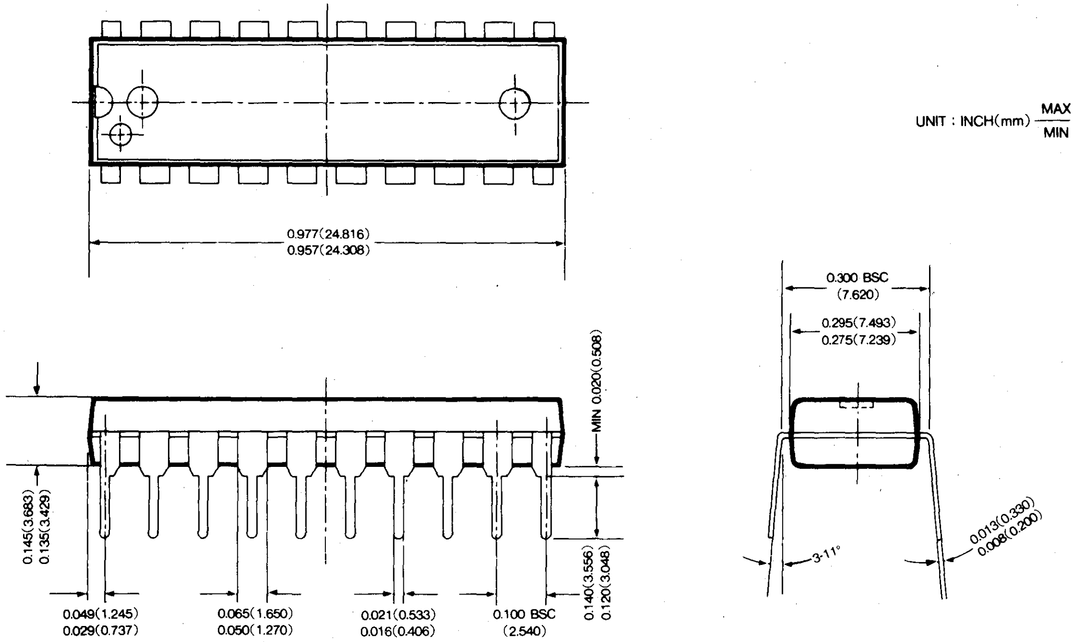
The V_{DD} current (I_{DD}) requirement of the HY534256AL during power on is dependent upon the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}=V_{SS}$ during power on, the device would go into an active cycle and I_{DD} would exhibit large current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on.

FIGURE 1. FAST PAGE MODE ACCESS TIME DETERMINATION

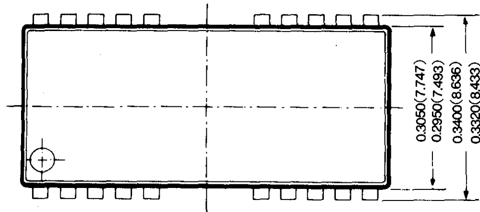


PACKAGE INFORMATION

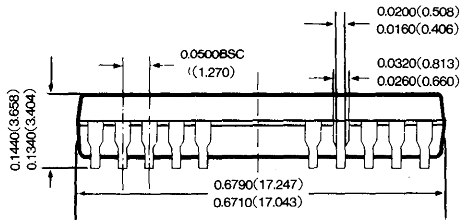
- **20 PIN PLASTIC DUAL IN LINE PACKAGE – 300 MIL**

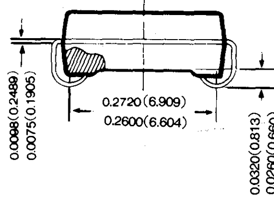


• 20/26 PIN SMALL OUTLINE J-FORM PACKAGE − 300 MIL



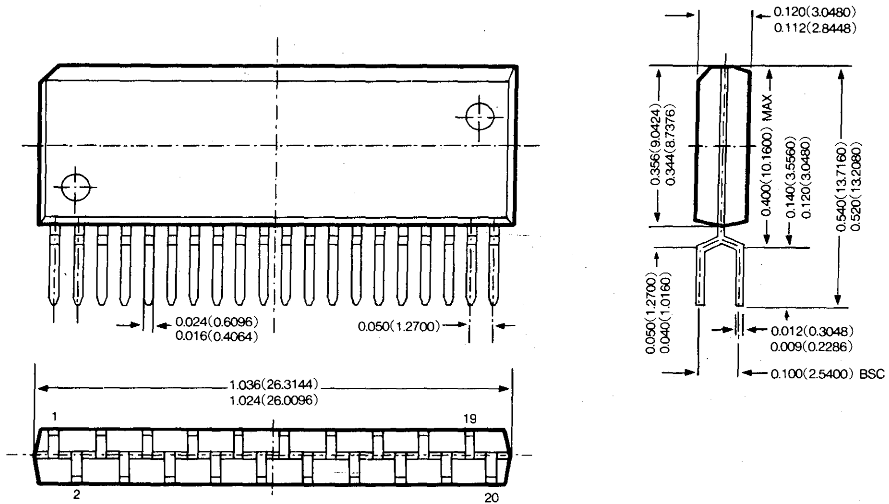
UNIT : INCH(mm) MAX/MIN





• **20 PIN ZIGZAG-IN-LINE PACKAGE－400MIL**

UNIT : INCH(mm) MAX/MIN



MEMO

HYUNDAI SEMICONDUCTOR

HY514100

4M×1-Bit CMOS DRAM

M191202A-JAN92

DESCRIPTION

The HY514100 is a low power and new generation dynamic RAM organized 4,194,304 words by 1 bit. The HY514100 utilizes HYUNDAI's CMOS process technology as well as advanced circuit technology to provide wide operating margins and very low power to the user.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

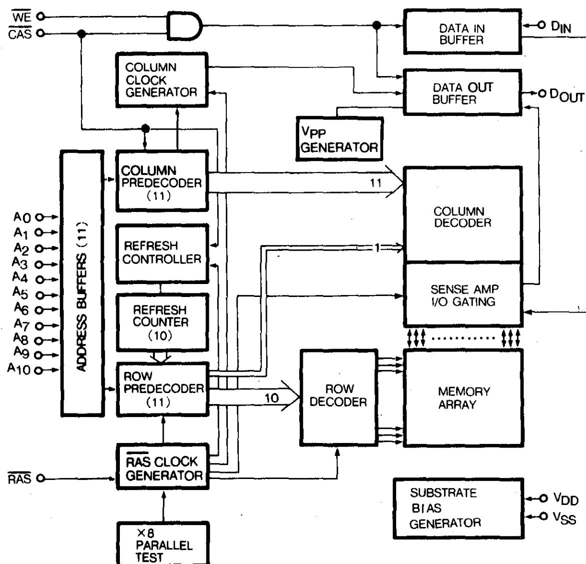
All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance.

FEATURES

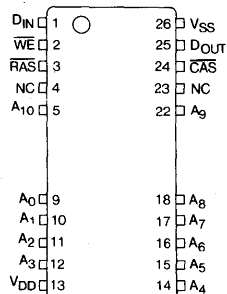
- **Low power dissipation**
  - **Operating Current, 100ns : 70mA(max.)**
  - **TTL Standby Current : 2mA(max.)**
  - **CMOS Standby Current : 1mA(max.)**
- **Read-Modify-Write Capability**
- **$\overline{RAS}$-only, Hidden, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Capability**
- **Common I/O capability**
- **Fast Page mode and Test mode capability**
- **1024 refresh cycles/16 ms**
- **High reliability 300 mil 20/26 pin SOJ.**
- **Fast access time and cycle time(ns)**

	HY514100-70	HY514100-80	HY514100-10
Max $\overline{RAS}$ Access Time, t_{RAC}	70	80	100
Max $\overline{CAS}$ Access Time, t_{CAC}	20	25	25
Min Fast Page Mode Cycle Time, t_{PC}	50	50	60
Min Cycle Time, t_{RC}	130	150	180

BLOCK DIAGRAM



PIN CONNECTIONS



SOJ

PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0-A_{10}	ADDRESS INPUT
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER (+ 5V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	0.6	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS
(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY514100		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	0V≤V_{IN}≤6.5V, All other pin not under test=V_{SS}		−	10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	D_{OUT} is disable, 0V≤V_{OUT}≤5.5V		−	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$\overline{RAS}$, $\overline{CAS}$, Address cycling, t_{RC}=t_{RC}(min.)	−70	−	90	mA	1, 2
			−80	−	80		
			−10	−	70		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$=$\overline{CAS}$=V_{IH}		−	2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}, t_{RC}=t_{RC}(min.)	−70	−	90	mA	2
			−80	−	80		
			−10	−	70		
I_{DD4}	V_{DD} Supply Current, Fast page mode	$\overline{RAS}$=V_{IL}, Address cycling, t_{PC}=t_{PC}(min.)	−70	−	70	mA	1, 2
			−80	−	60		
			−10	−	50		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}$=$\overline{CAS}$=V_{DD}−0.2V		−	1	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{RC}(min.)	−70	−	90	mA	2
			−80		80		
			−10	−	70		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		−	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	−	V	

NOTES :
1. I_{DD1} and I_{DD4} depend on output loading, specified values are abtained with the output open.
2. I_{DD1}, I_{DD3}, I_{DD4} and I_{DD6} depend on cycle rate.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1, 2, 3

#	SYMBOL	PARAMETER	HY514100						UNIT	NOTES
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
2	t_{RWC}	Read-Modify-Write Cycle Time	155	–	180	–	210	–	ns	
3	t_{PC}	Fast Page Mode Cycle Time	50	–	50	–	60	–	ns	
4	t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	75	–	80	–	90	–	ns	
5	t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	4, 9
6	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	–	25	ns	4, 9
7	t_{AA}	Access Time from Column Address	–	35	–	40	–	45	ns	4, 9
8	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	45	–	55	ns	4
9	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	ns	4
10	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
11	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
12	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
13	t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	ns	
14	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	70	200K	80	200K	100	200K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	25	–	ns	
16	t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
17	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	25	10K	25	10K	ns	
18	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	55	25	75	ns	9
19	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	55	ns	10
20	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
21	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
22	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
23	t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
24	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
25	t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
26	t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	60	–	80	–	ns	
27	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	45	–	ns	
28	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
29	t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	6
30	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
31	t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
32	t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	60	–	80	–	ns	
33	t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
34	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	25	–	ns	
35	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	25	–	ns	
36	t_{DS}	Data Set-up Time	0	–	0	–	0	–	ns	7
37	t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	7
38	t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	60	–	80	–	ns	
39	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
40	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	8
41	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	20	–	25	–	25	–	ns	8
42	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	70	–	80	–	100	–	ns	8
43	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	35	–	40	–	45	–	ns	8

#	SYMBOL	PARAMETER	HY514100						UNIT	NOTES
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
44	t_{CSR}	CAS Set-up Time(CAS Before RAS Cycle)	10	–	10	–	10	–	ns	
45	t_{CHR}	CAS Hold Time(CAS Before RAS Cycle)	30	–	30	–	30	–	ns	
46	t_{RPC}	RAS to CAS Precharge Time	0	–	0	–	0	–	ns	
47	t_{CPT}	CAS Precharge Time(CBR Counter Test Cycle)	40	–	40	–	50	–	ns	
48	t_{WTS}	Write Command Set-up Time(Test Mode In)	10	–	10	–	10	–	ns	
49	t_{WTH}	Write Command Hold Time(Test Mode In)	10	–	10	–	10	–	ns	
50	t_{WRP}	WE to RAS Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
51	t_{WRH}	WE to RAS Hold Time(CAS Before RAS Cycle)	10	–	10	–	10	–	ns	
52	t_{CPWD}	CAS Precharge to WE Delay	40	–	45	–	50	–	ns	
53	t_{RHCP}	RAS Hold Time from CAS Precharge	40	–	45	–	50	–	ns	

AC CHARACTERISTICS IN TEST MODE NOTE 11

#	SYMBOL	PARAMETER	HY514100						UNIT	NOTES
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
54	t_{RC}	Random Read or Write Cycle Time	135	–	155	–	185	–	ns	
55	t_{RWC}	Read-Modify-Write Cycle Time	160	–	185	–	215	–	ns	
56	t_{PC}	Fast Page Mode Cycle Time	55	–	55	–	65	–	ns	
57	t_{PRWC}	Fast Page Mode RMW Cycle Time	80	–	85	–	95	–	ns	
58	t_{RAC}	Access Time from RAS	–	75	–	85	–	105	ns	4, 9
59	t_{CAC}	Access Time from CAS	–	25	–	30	–	30	ns	4, 9
60	t_{AA}	Access Time from Column Address	–	40	–	45	–	50	ns	4, 9
61	t_{CPA}	Access Time from CAS Precharge	–	50	–	50	–	60	ns	4
62	t_{RAS}	RAS Pulse Width	75	10K	85	10K	105	10K	ns	
63	t_{RASP}	RAS Pulse Width(Fast Page Mode)	75	200K	85	200K	105	200K	ns	
64	t_{RSH}	RAS Hold Time	25	–	30	–	30	–	ns	
65	t_{CSH}	CAS Hold Time	75	–	85	–	105	–	ns	
66	t_{CAS}	CAS Pulse Width	25	10K	30	10K	30	10K	ns	
67	t_{RAL}	Column Address to RAS Lead Time	35	–	45	–	50	–	ns	
68	t_{CWD}	CAS to WE Delay Time	25	–	30	–	30	–	ns	8
69	t_{RWD}	RAS to WE Delay Time	75	–	85	–	105	–	ns	8
70	t_{AWD}	Column Address to WE Dealy Time	40	–	45	–	50	–	ns	8

NOTES :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle : If $t_{RWD} \geq t_{RWD}$(min.). $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.) the cycle is a read-modify-write cycle and data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out(at access time) is indeterminate.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.)can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. These specifications are applied to the test mode.

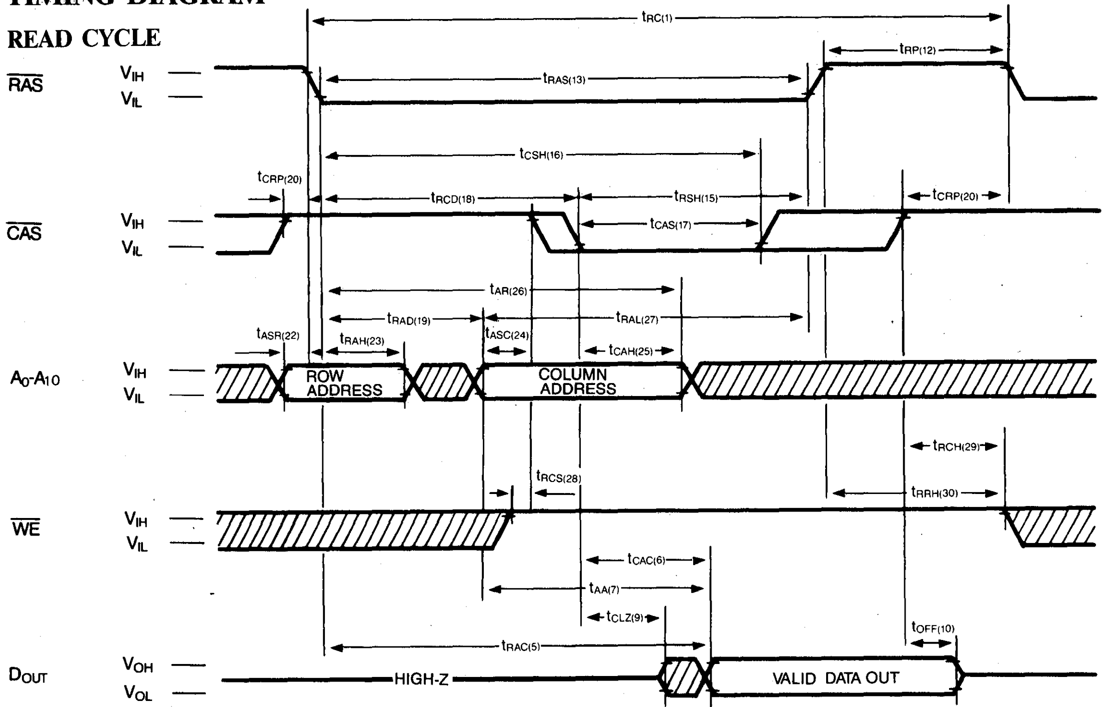
CAPACITANCE

(T_A=0°C to 70°C, V_{DD}=5V+10%, f=1MHz)

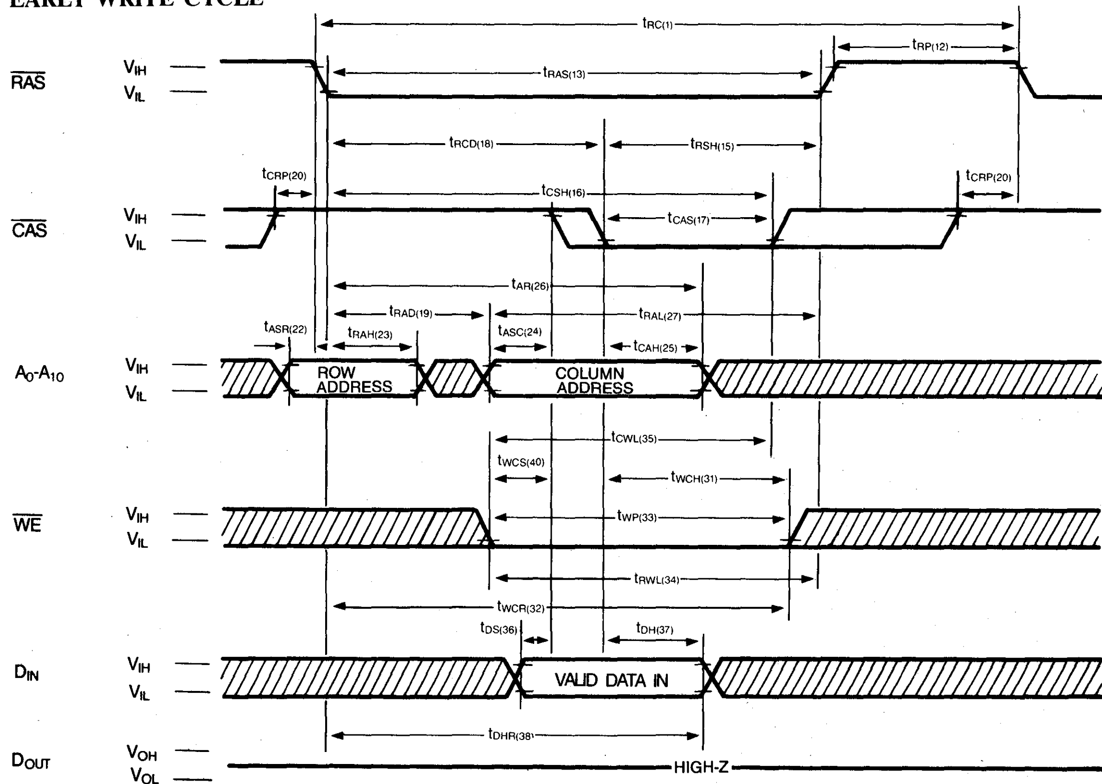
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_{10}, D_{IN})	–	5	pF
C_{IN2}	Input Capacitance($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	–	7	pF
C_{OUT}	Output Capacitance(D_{OUT})	–	7	pF

TIMING DIAGRAM

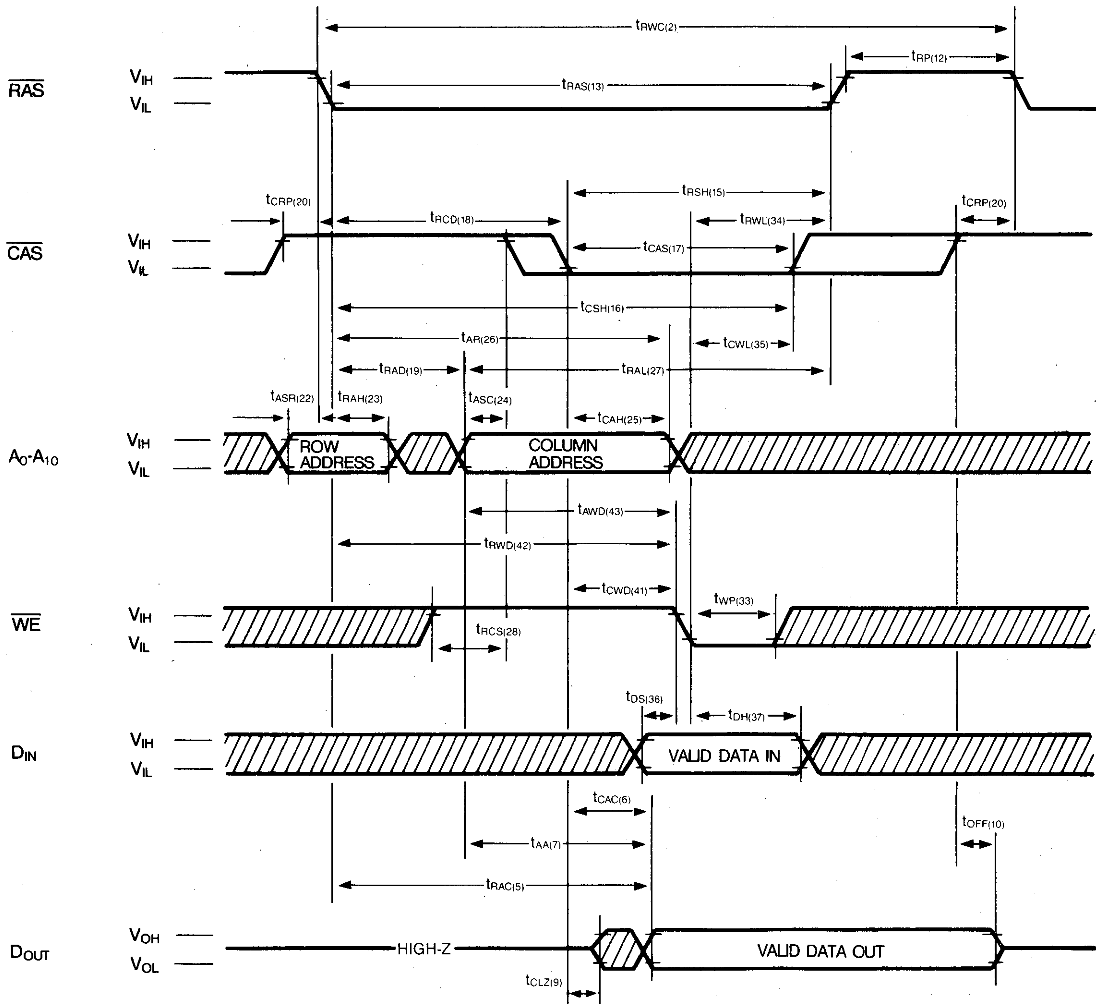
READ CYCLE



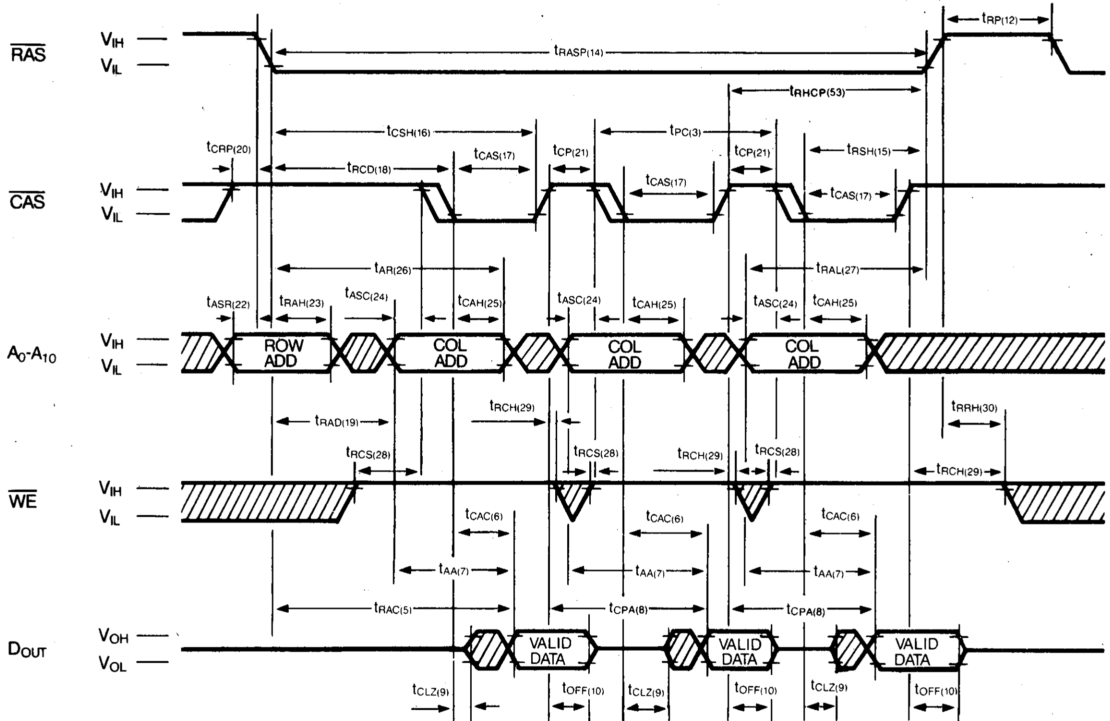
EARLY WRITE CYCLE



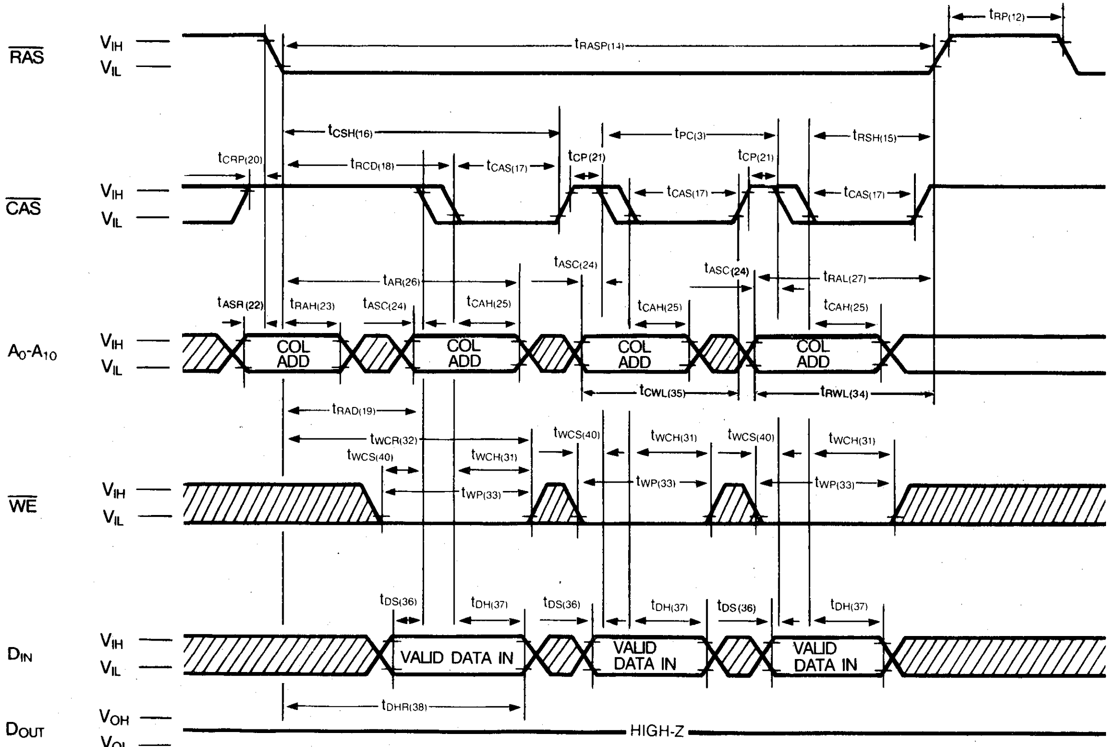
READ-MODIFY-WRITE CYCLE



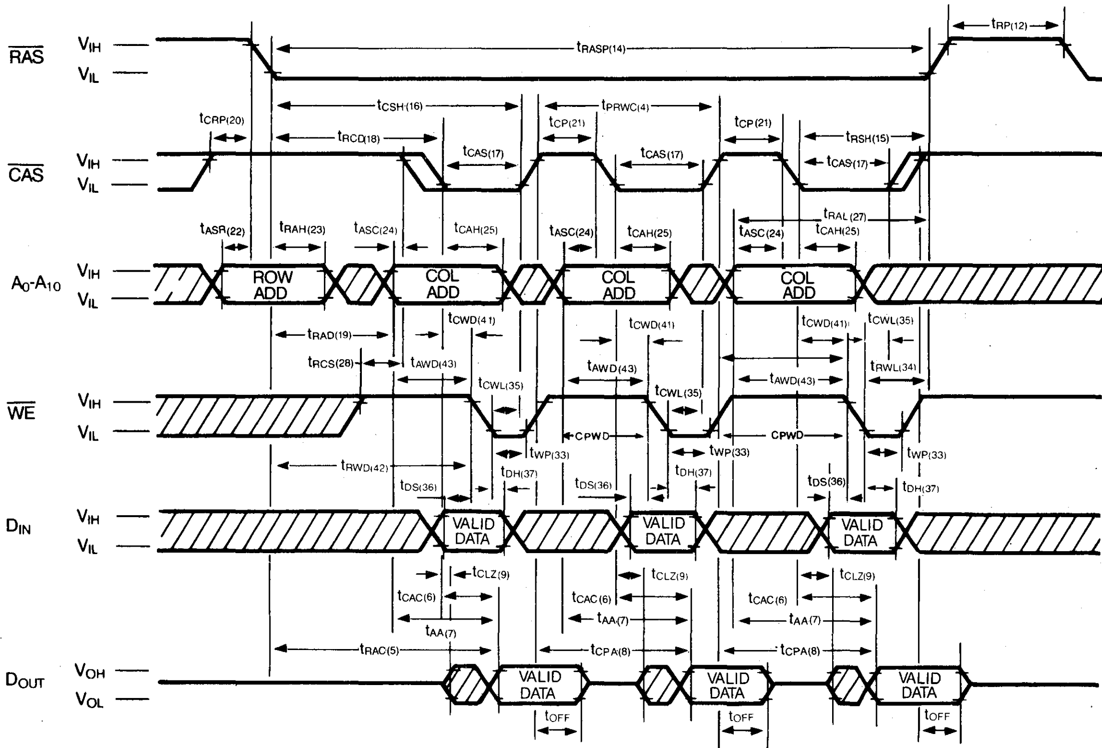
FAST PAGE MODE READ CYCLE



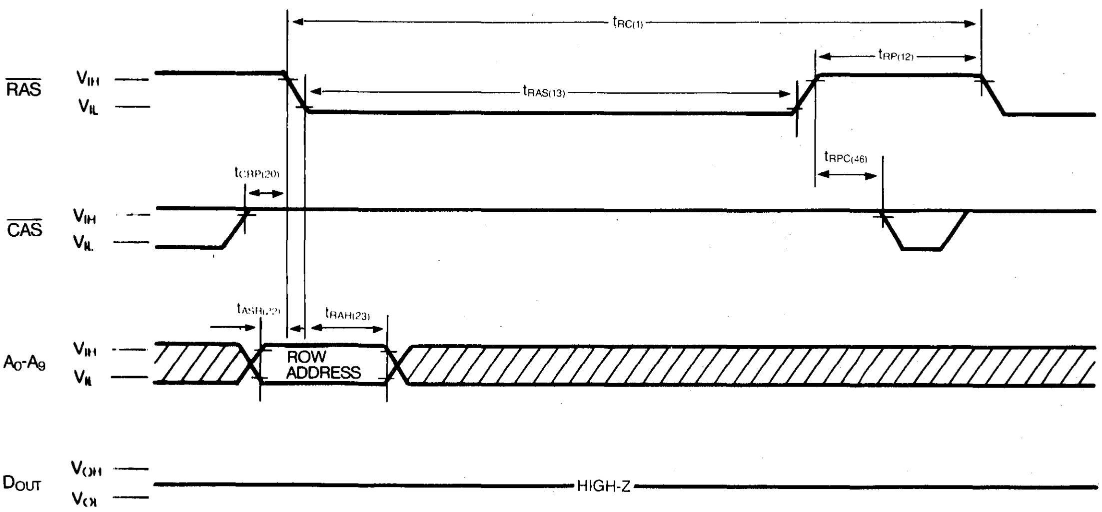
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE

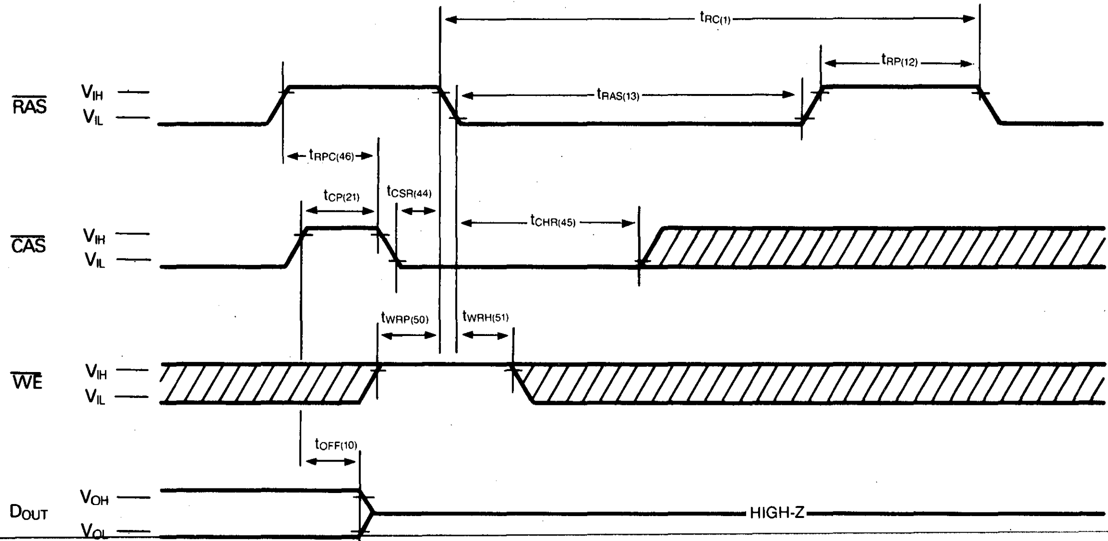


RAS-ONLY REFRESH CYCLE



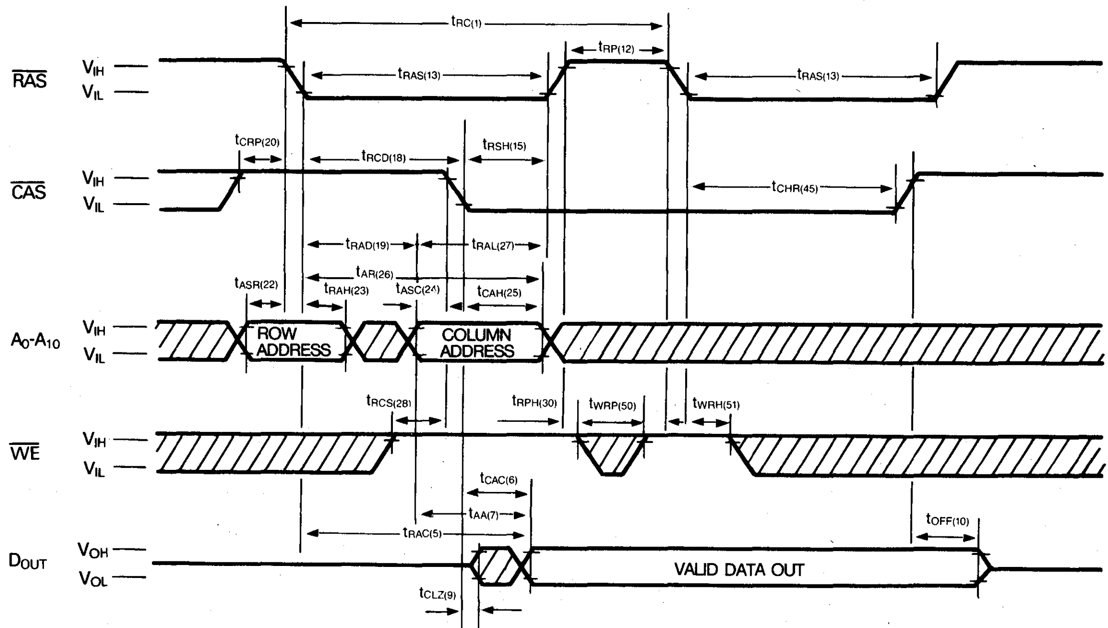
NOTE : $\overline{WE}$ and A_{10}="H" or "L"

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

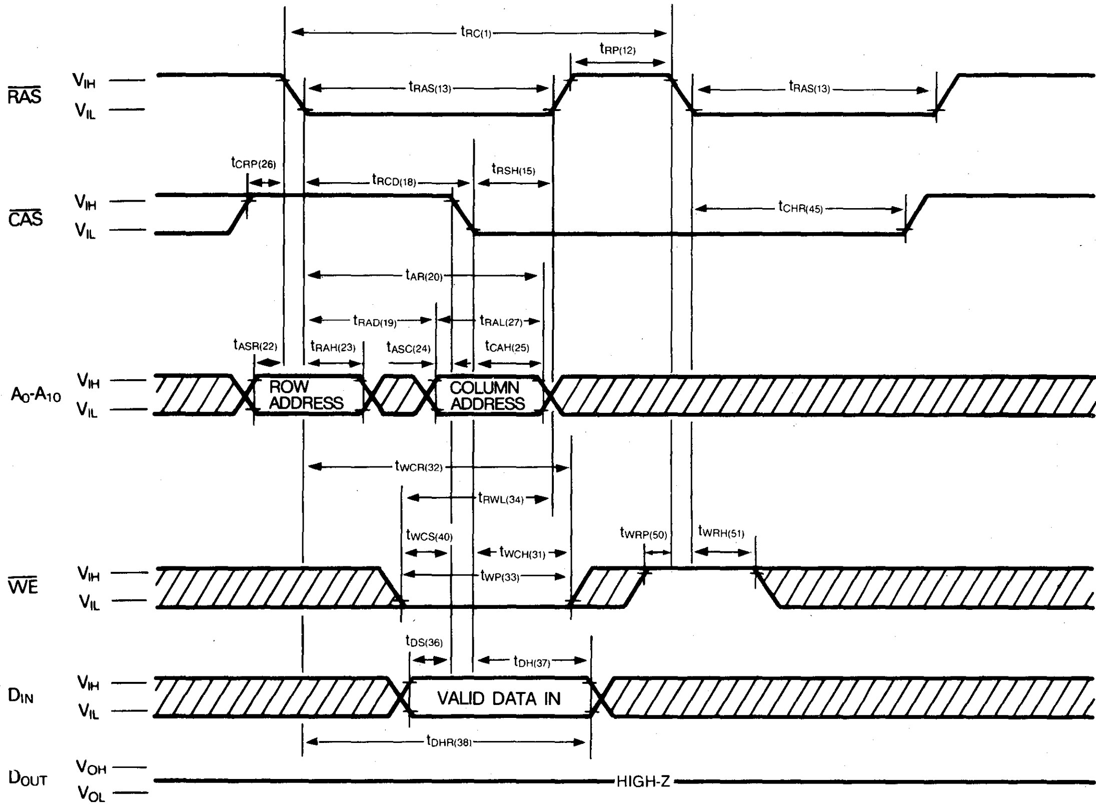


NOTE : A_0-A_{10}= "H" or "L"

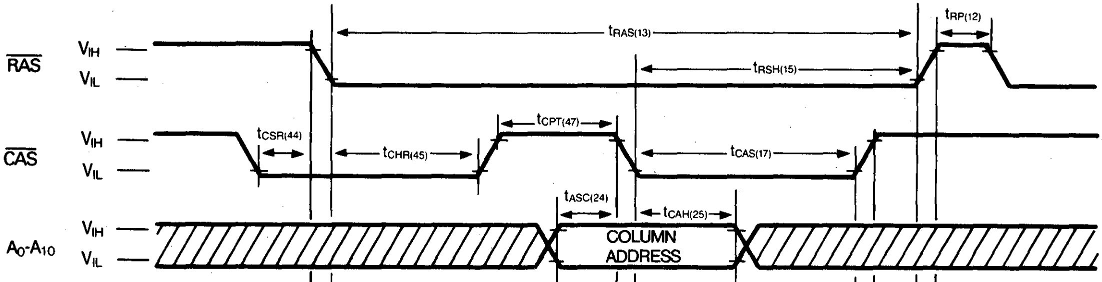
HIDDEN REFRESH CYCLE (READ)



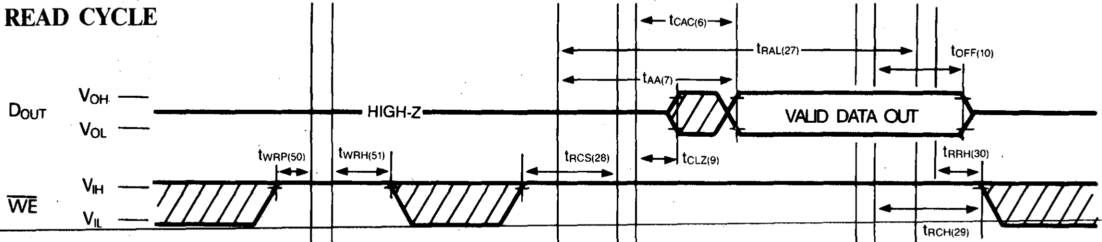
HIDDEN REFRESH CYCLE (WRITE)



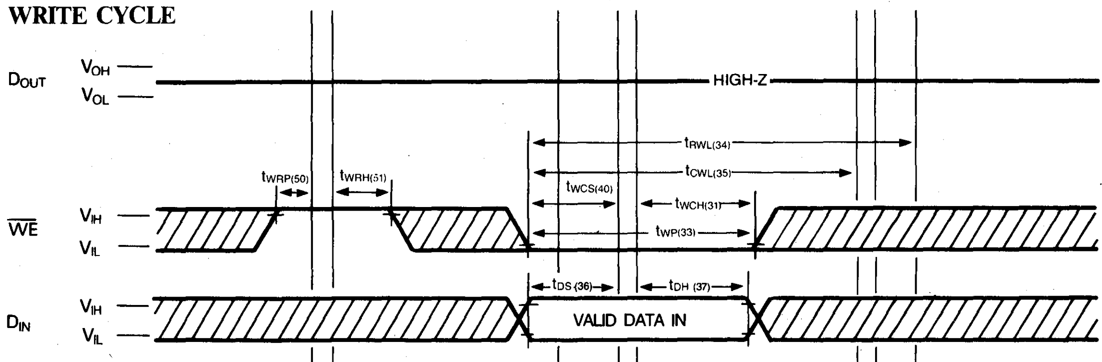
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



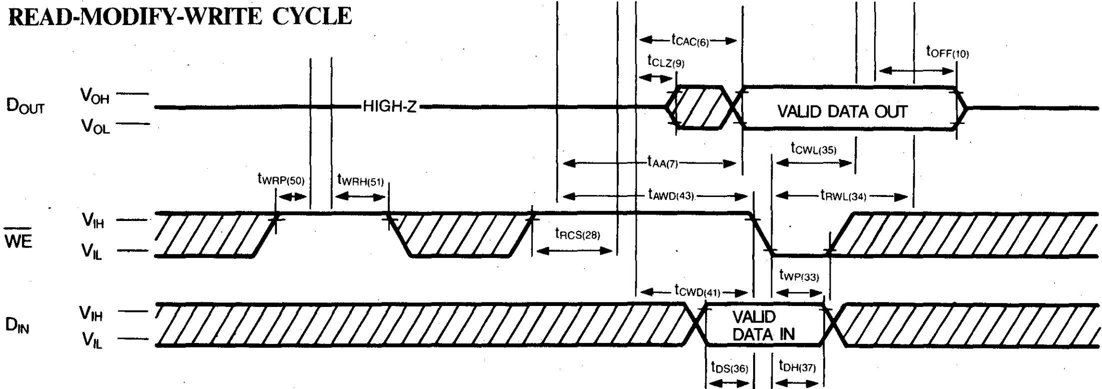
READ CYCLE



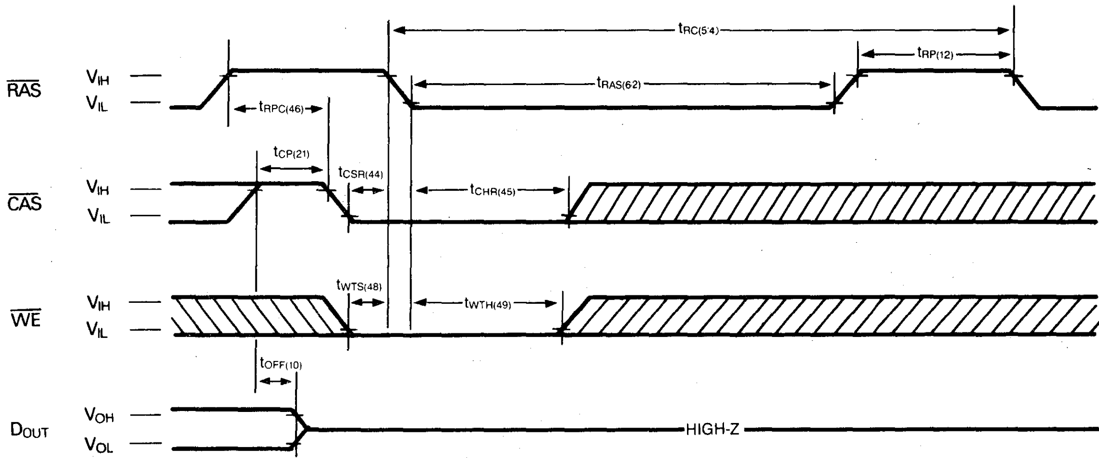
WRITE CYCLE



READ-MODIFY-WRITE CYCLE



TEST MODE IN CYCLE



NOTE : D_{IN} and A_0-A_{10} : "H" or "L"

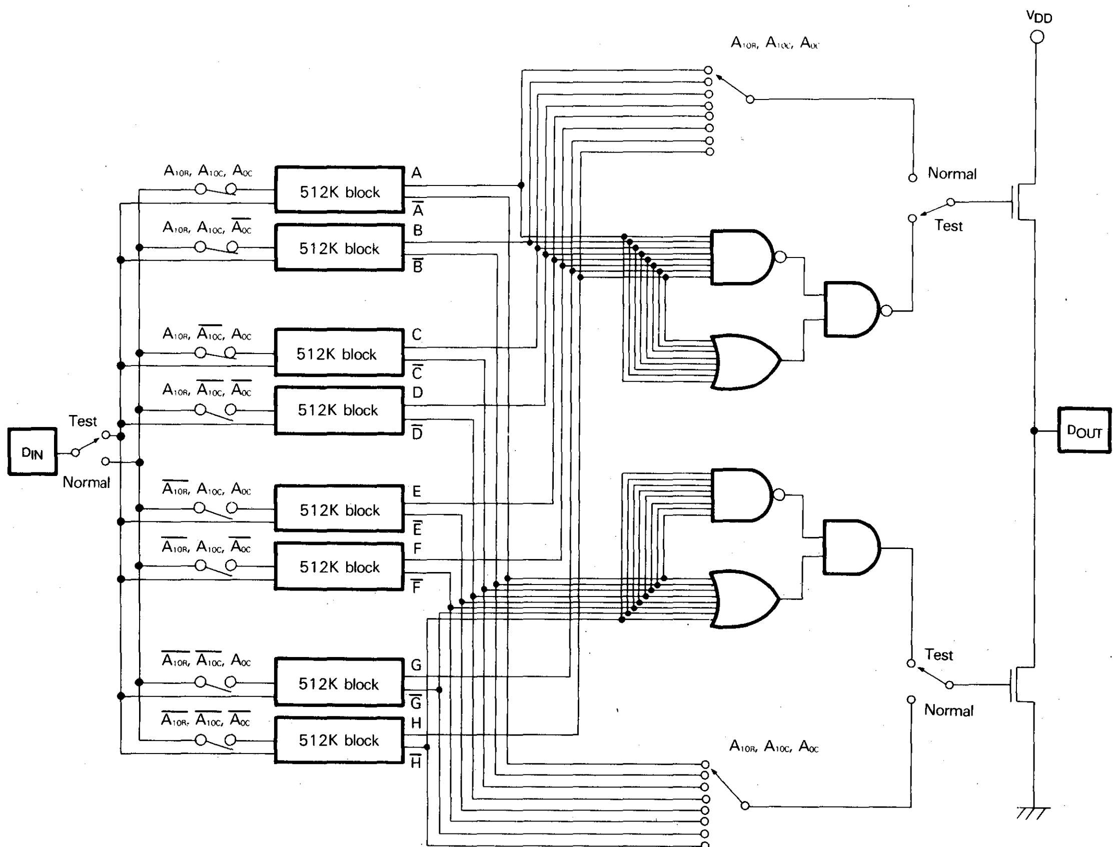
3

TEST MODE

The HY514100 is a DRAM organized 4,194, 304 words by 1 bits and it is internally organized 524,288 words by 8bits. In Test Mode, data are written into 8 sectors in parellel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal(all 1s or 0s), the data output indicates 1. If any of the bits differed, the data output pin indicates 0. The following figure shows the block diagram of HY514100. In Test Mode, 4M×1 DRAM can be tested as if it were a 512K×1 DRAM.

$\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle(Test Mode In) puts the device into Test Mode. And $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle or $\overline{RAS}$-Only-Refresh Cycle puts it back into Normal Mode. In Test Mode, $\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle performs the refresh operation with the internal refresh address counter. The Test Mode funtion reduces test time to one-eighth of normal in case of N test pattern.

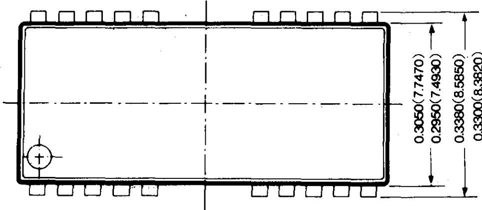
BLOCK DIAGRAM IN TEST MODE

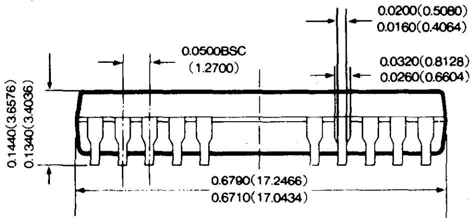


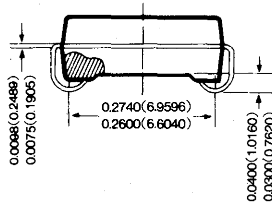
PACKAGE INFORMATION

- **20/26 PIN SMALL OUT LINE J-FORM PACKAGE-300 MIL**

UNIT : INCH(mm) MAX/MIN







3

MEMO

PRELIMINARY

HYUNDAI SEMICONDUCTOR

HY514100A

4M×1-Bit CMOS DRAM

M1G1200A-MAR92

DESCRIPTION

The HY514100A is a high speed, and new generation 4,194,304 words by 1 bit CMOS dynamic random access memory, fabricated with the HYUNDAI CMOS process. The HY514100A offers a fast page mode operation, fast usable speed, and inherently high CMOS reliability.

All inputs and output are TTL compatible. Multiplexed address inputs permit the HY514100A to be packaged in a standard 20/26 pin SOJ, TSOP, and 20 pin ZIP.

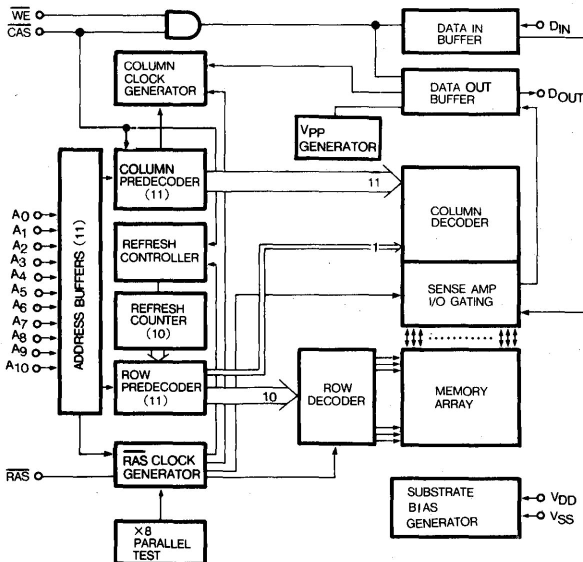
HY514100A design is optimized for cache based mainframe, and microcomputers, graphics, digital signal processing, and high performance microprocessor systems.

FEATURES

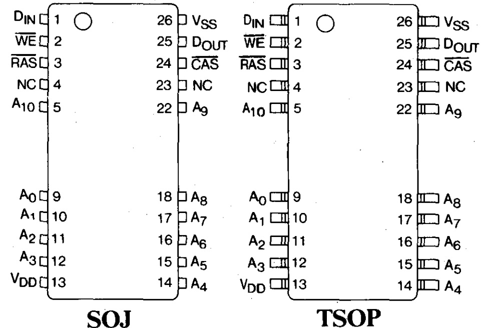
- Low power dissipation
  - Operating Current, 80ns : 85mA(max.)
  - TTL Standby Current : 2mA(max.)
  - CMOS Standby Current : 1mA(max.)
- Read-Modify-Write Capability
- $\overline{RAS}$-only, Hidden, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Capability
- Fast Page mode and Test mode Capability
- Single 5V± 10% power supply
- 1024 refresh cycles/16ms
- High reliability 300 mil 20/26 pin SOJ, TSOP and 400mil 20pin ZIP.
- Fast access time and cycle time(ns)

	HY514100A-60	HY514100A-70	HY514100A-80
Max $\overline{RAS}$ Access Time, t_{RAC}	60	70	80
Max $\overline{CAS}$ Access Time, t_{CAC}	20	20	25
Min Fast Page Mode Cycle Time, t_{PC}	40	45	55
Min Cycle Time, t_{RC}	120	130	150

BLOCK DIAGRAM

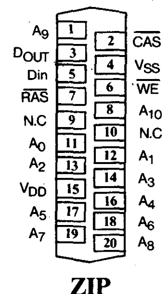


PIN CONNECTIONS



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
A_0-A_{10}	ADDRESS INPUT
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND



3

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
T_{SOLDER}	Soldering Temperature, Time	260, 10	℃, sec
P_T	Power Dissipation	735	mW

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY514100A		UNIT	NOTE
				MIN.	MAX.		
$\mid I_{LI} \mid$	Input Leakage Current(any input pin)	0V≤V_{IN}≤6.5V, All other pin not under test=V_{SS}		–	10	μA	
$\mid I_{LO} \mid$	Output Leakage Current for High Impedance State	D_{OUT} is disable, 0V≤V_{OUT}≤5.5V		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$\overline{RAS}$, $\overline{CAS}$, Address cycling, t_{RC}=t_{RC}(min.)	−60	–	105	mA	1, 2
			−70	–	95		
			−80	–	85		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$=$\overline{CAS}$=V_{IH}		–	2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}, t_{RC}=t_{RC}(min.)	−60	–	105	mA	1
			−70	–	95		
			−80	–	85		
I_{DD4}	V_{DD} Supply Current, Fast page mode	$\overline{RAS}$=V_{IL}, Address cycling, t_{PC}=t_{PC}(min.)	−60	–	65	mA	1, 2
			−70	–	55		
			−80	–	45		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}$=$\overline{CAS}$=V_{DD}−0.2V		–	1	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{RC}(min.)	−60	–	105	mA	1, 4
			−70		95		
			−80	–	85		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 3, 4, 5

#	SYMBOL	PARAMETER	HY514100A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
2	t_{RWC}	Read-Modify-Write Cycle Time	145	–	155	–	180	–	ns	
3	t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	55	–	ns	
4	t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	65	–	70	–	85	–	ns	
5	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	7, 12
6	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	7, 12
7	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	7, 12
8	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	7
9	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	ns	7
10	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	8
11	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	6
12	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	50	–	60	–	ns	
13	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	200K	70	200K	80	200K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
17	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
18	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	55	ns	12
19	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	13
20	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
21	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
22	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
23	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
24	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
25	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
26	t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
27	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
28	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
29	t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	9
30	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	9
31	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
32	t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
33	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
34	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
35	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
36	t_{DS}	Data Set-up Time	0	–	0	–	0	–	ns	10
37	t_{DH}	Data Hold Time	15	–	15	–	15	–	ns	10
38	t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
39	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
40	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	11
41	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	20	–	20	–	25	–	ns	11
42	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	60	–	70	–	80	–	ns	11
43	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	30	–	35	–	40	–	ns	11

#	SYMBOL	PARAMETER	HY514100A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
44	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
45	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	30	–	ns	
46	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
47	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	30	–	35	–	40	–	ns	
48	t_{WTS}	Write Command Set-up Time(Test Mode In)	10	–	10	–	10	–	ns	
49	t_{WTH}	Write Command Hold Time(Test Mode In)	10	–	10	–	10	–	ns	
50	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
51	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

AC CHARACTERISTICS IN TEST MODE NOTE 14

#	SYMBOL	PARAMETER	HY514100A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
52	t_{RC}	Random Read or Write Cycle Time	125	–	135	–	155	–	ns	
53	t_{RWC}	Read-Modify-Write Cycle Time	150	–	160	–	185	–	ns	
54	t_{PC}	Fast Page Mode Cycle Time	45	–	50	–	60	–	ns	
55	t_{PRWC}	Fast Page Mode RMW Cycle Time	70	–	75	–	90	–	ns	
56	t_{RAC}	Access Time from $\overline{RAS}$	–	65	–	75	–	85	ns	7, 12
57	t_{CAC}	Access Time form $\overline{CAS}$	–	25	–	25	–	30	ns	7, 12
58	t_{AA}	Access Time form Column Address	–	35	–	40	–	45	ns	7, 12
59	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	45	–	55	ns	7
60	t_{RAS}	$\overline{RAS}$ Pulse Width	65	10K	75	10K	85	10K	ns	
61	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	65	200K	75	200K	85	200K	ns	
62	t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
63	t_{CSH}	$\overline{CAS}$ Hold Time	65	–	75	–	85	–	ns	
64	t_{CAS}	$\overline{CAS}$ Pulse Width	25	10K	25	10K	30	10K	ns	
65	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	45	–	ns	
66	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	25	–	25	–	30	–	ns	11
67	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	65	–	75	–	85	–	ns	11
68	t_{AWD}	Column Address to $\overline{WE}$ Dealy Time	35	–	40	–	45	–	ns	11

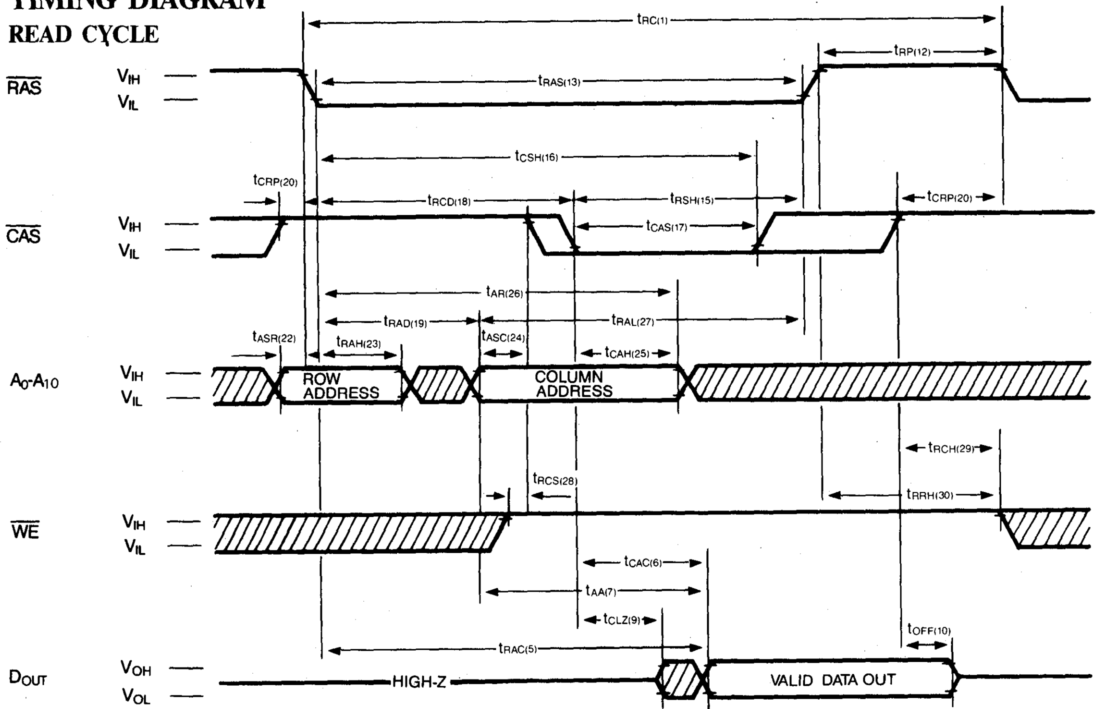
NOTES :
1. I_{DD1}, I_{DD3}, I_{DD4}, I_{DD6}, I_{DD7} depend on cycle rate.
2. I_{DD1}, I_{DD4} depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. It depends on user whether column address is changed or not at least once while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
5. AC measurements assume t_T=5ns.
6. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Measured with a load equivalent to 2 TTL loads and 100pF.
8. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycle.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and data out pin will remain open circuit(high impedance) through the entire cycle : If $t_{RWD} \geq t_{RWD}$(min.). $t_{CWD} \geq t_{CWD}$(min) and $t_{AWD} \geq t_{AWD}$(min.) the cycle is a read-modify-write cycle and data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out(at access time) is indeterminate.
12. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
13. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
14. These specifications are applied to the test mode.

CAPACITANCE
(T_A= 0°C to 70°C, V_{DD}=5V± 10%, f=1MHz)

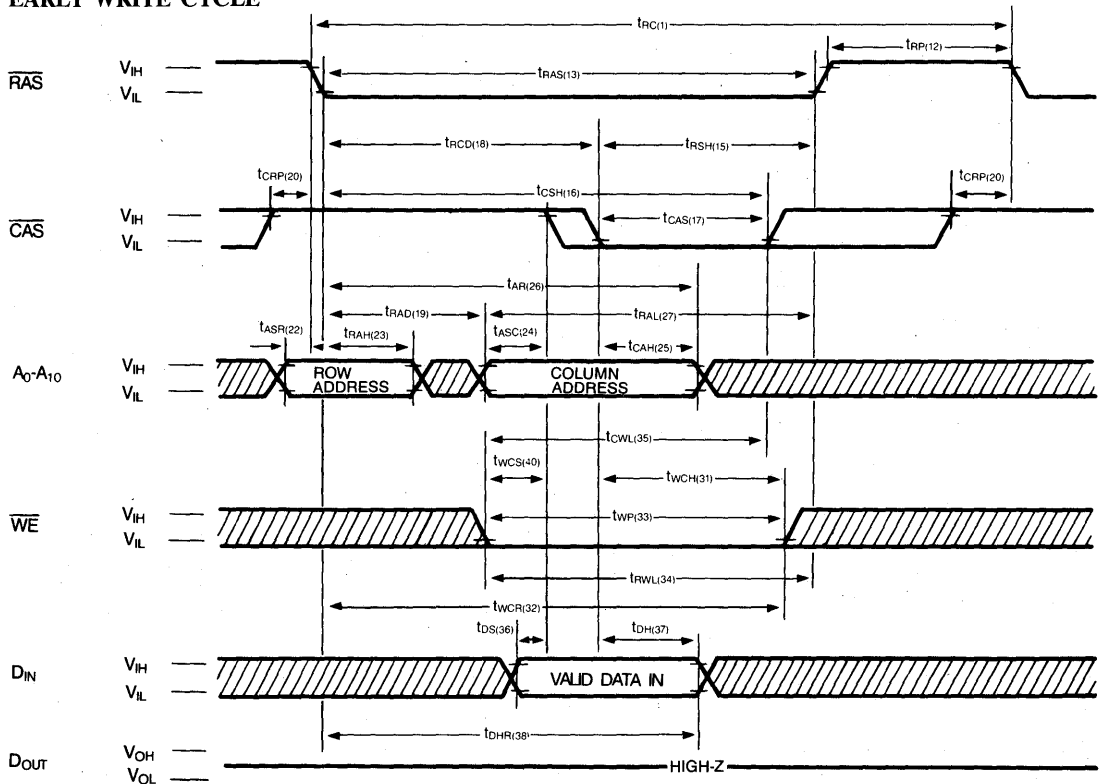
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN1}	Input Capacitance (A_0-A_{10}, D_{IN})	–	5	pF
C_{IN2}	Input Capacitance($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	–	7	pF
C_{OUT}	Output Capacitance(D_{OUT})	–	7	pF

TIMING DIAGRAM

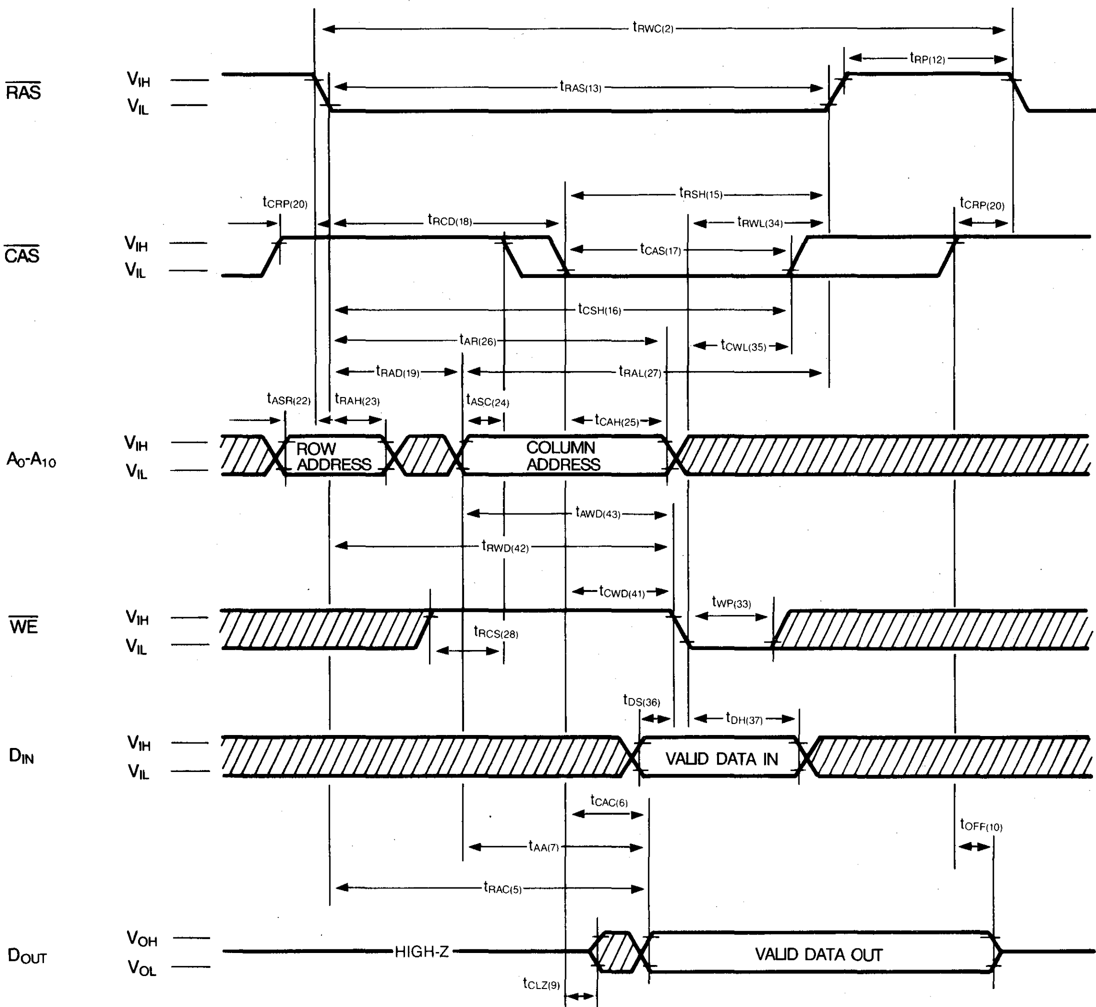
READ CYCLE



EARLY WRITE CYCLE



READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

FAST PAGE MODE EARLY WRITE CYCLE

FAST PAGE MODE READ-MODIFY-WRITE

$\overline{RAS}$ V_{IH} / V_{IL}; $\overline{CAS}$ V_{IH} / V_{IL}; A_0-A_{10} V_{IH} / V_{IL} (ROW ADD, COL ADD, COL ADD, COL ADD); $\overline{WE}$ V_{IH} / V_{IL}; D_{IN} V_{IH} / V_{IL} (VALID DATA); D_{OUT} V_{OH} / V_{OL} (VALID DATA)

Timing parameters: $t_{RASP(14)}$, $t_{RP(12)}$, $t_{CSH(16)}$, $t_{PRWC(4)}$, $t_{CRP(20)}$, $t_{RCD(18)}$, $t_{CAS(17)}$, $t_{CP(21)}$, $t_{RSH(15)}$, $t_{RAL(27)}$, $t_{ASR(22)}$, $t_{RAH(23)}$, $t_{ASC(24)}$, $t_{CAH(25)}$, $t_{CWD(41)}$, $t_{CWL(35)}$, $t_{RAD(19)}$, $t_{RCS(28)}$, $t_{AWD(43)}$, $t_{RWL(34)}$, $t_{WP(33)}$, $t_{RWD(42)}$, $t_{DH(37)}$, $t_{DS(36)}$, $t_{CLZ(9)}$, $t_{CAC(6)}$, $t_{AA(7)}$, $t_{RAC(5)}$, $t_{CPA(8)}$, t_{OFF}

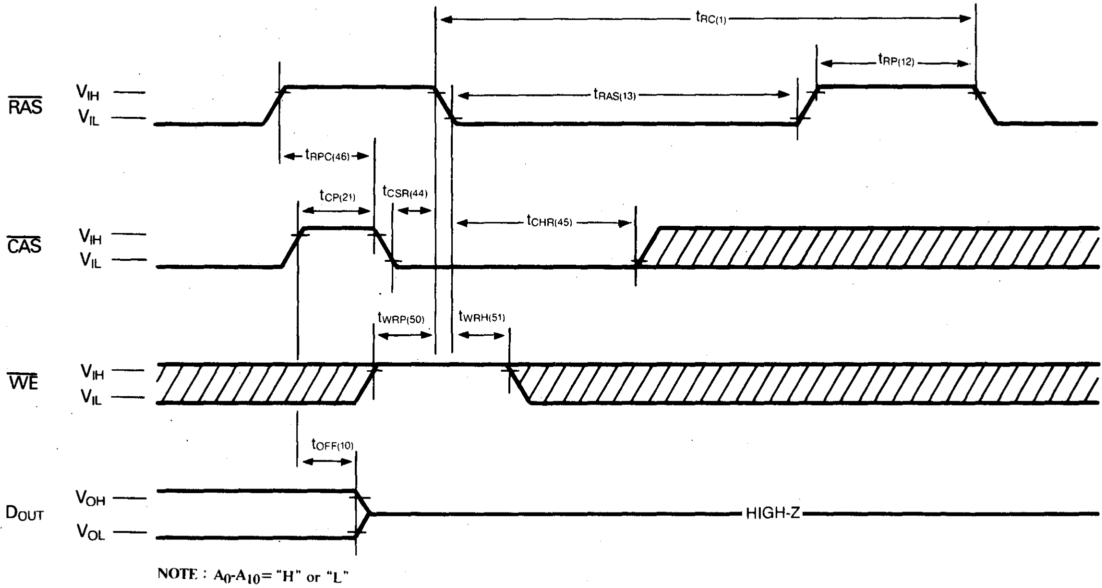
$\overline{RAS}$-ONLY REFRESH CYCLE

$\overline{RAS}$ V_{IH} / V_{IL}; $\overline{CAS}$ V_{IH} / V_{IL}; A_0-A_9 V_{IH} / V_{IL} (ROW ADDRESS); D_{OUT} V_{OH} / V_{OL} (HIGH-Z)

Timing parameters: $t_{RC(1)}$, $t_{RP(12)}$, $t_{RAS(13)}$, $t_{RPC(46)}$, $t_{CRP(20)}$, $t_{ASR(22)}$, $t_{RAH(23)}$

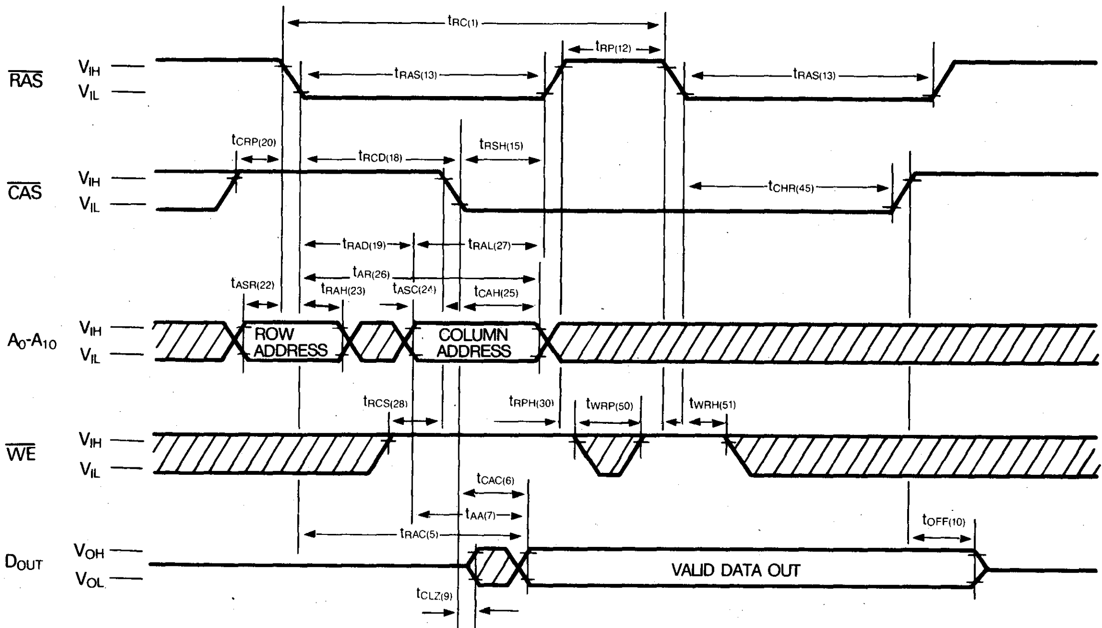
NOTE : $\overline{WE}$ and A_{10}="H" or "L"

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

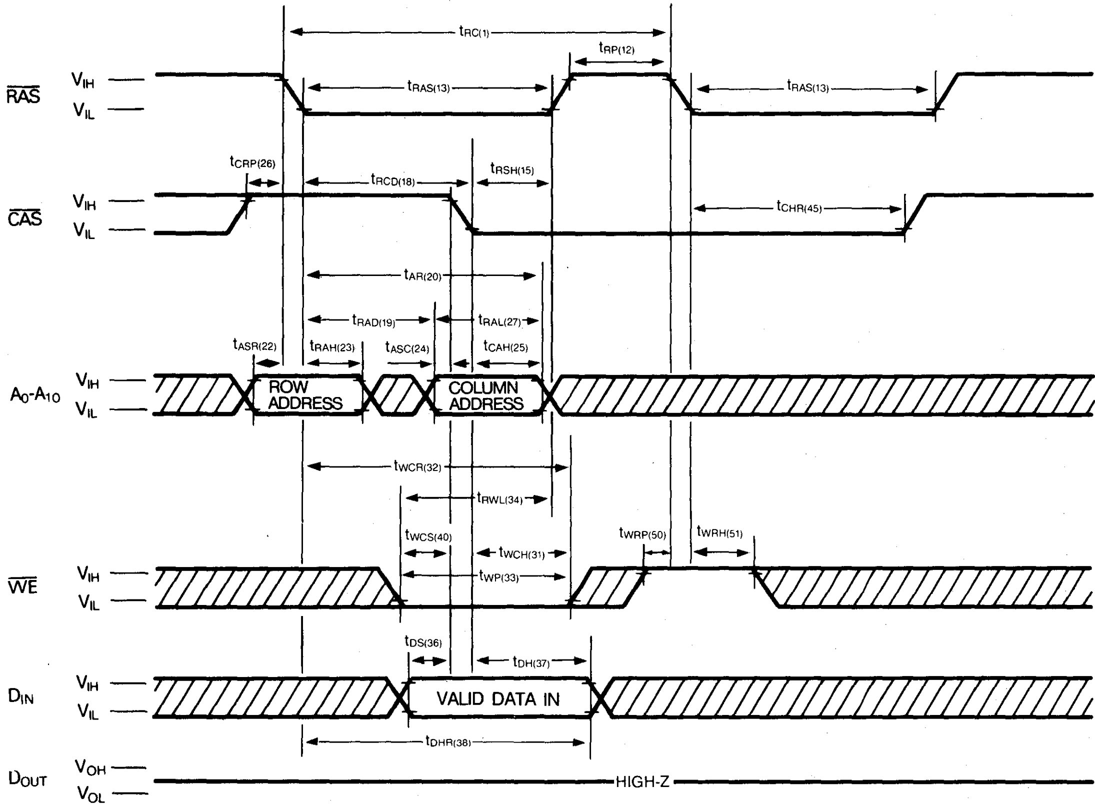


NOTE : A_0-A_{10}= "H" or "L"

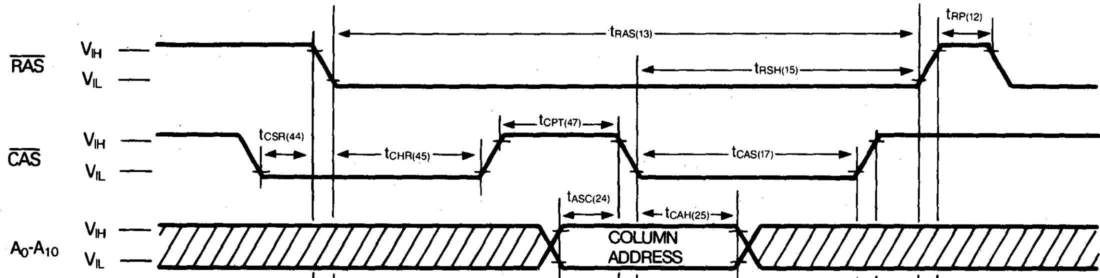
HIDDEN REFRESH CYCLE (READ)



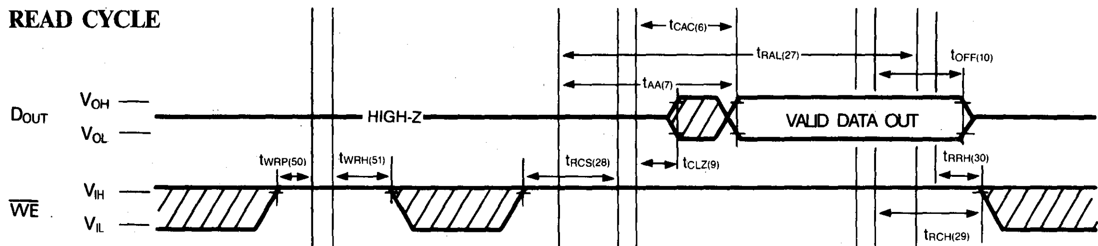
HIDDEN REFRESH CYCLE(WRITE)



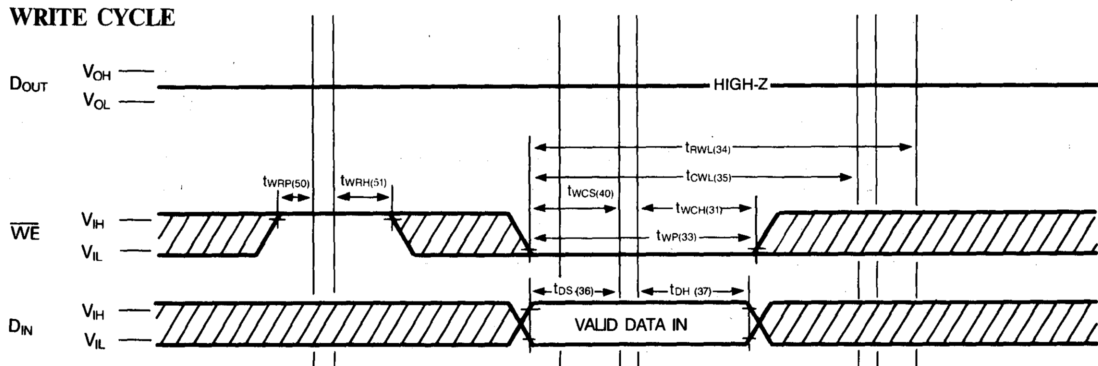
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



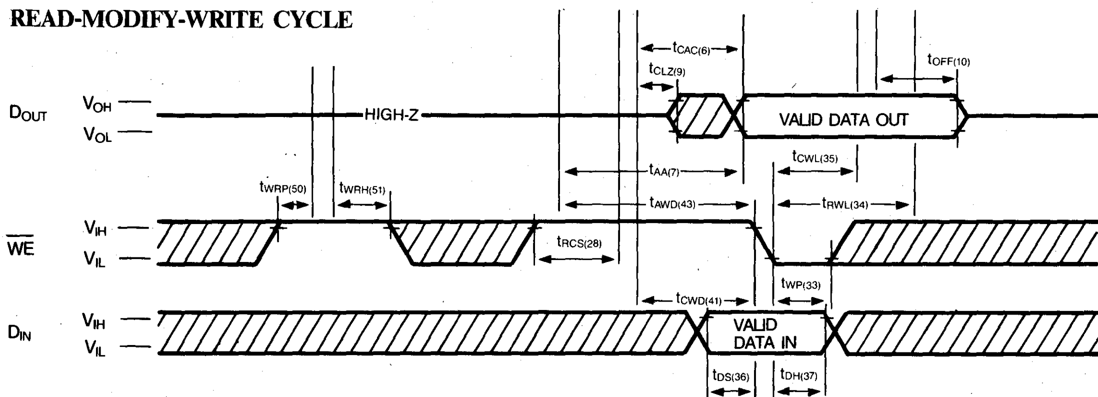
READ CYCLE



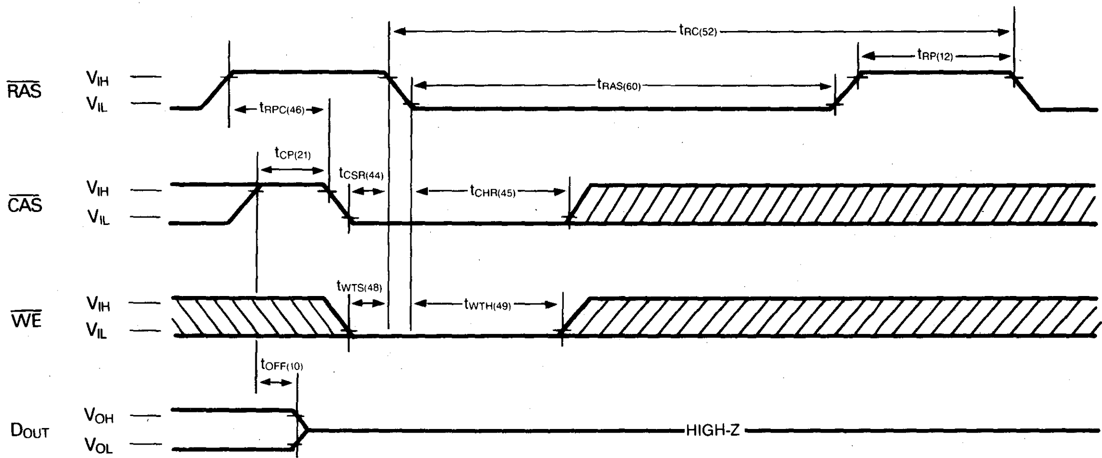
WRITE CYCLE



READ-MODIFY-WRITE CYCLE



TEST MODE IN CYCLE



NOTE : D_{IN} and A_0-A_{10} : "H" or "L"

BLOCK DIAGRAM IN TEST MODE

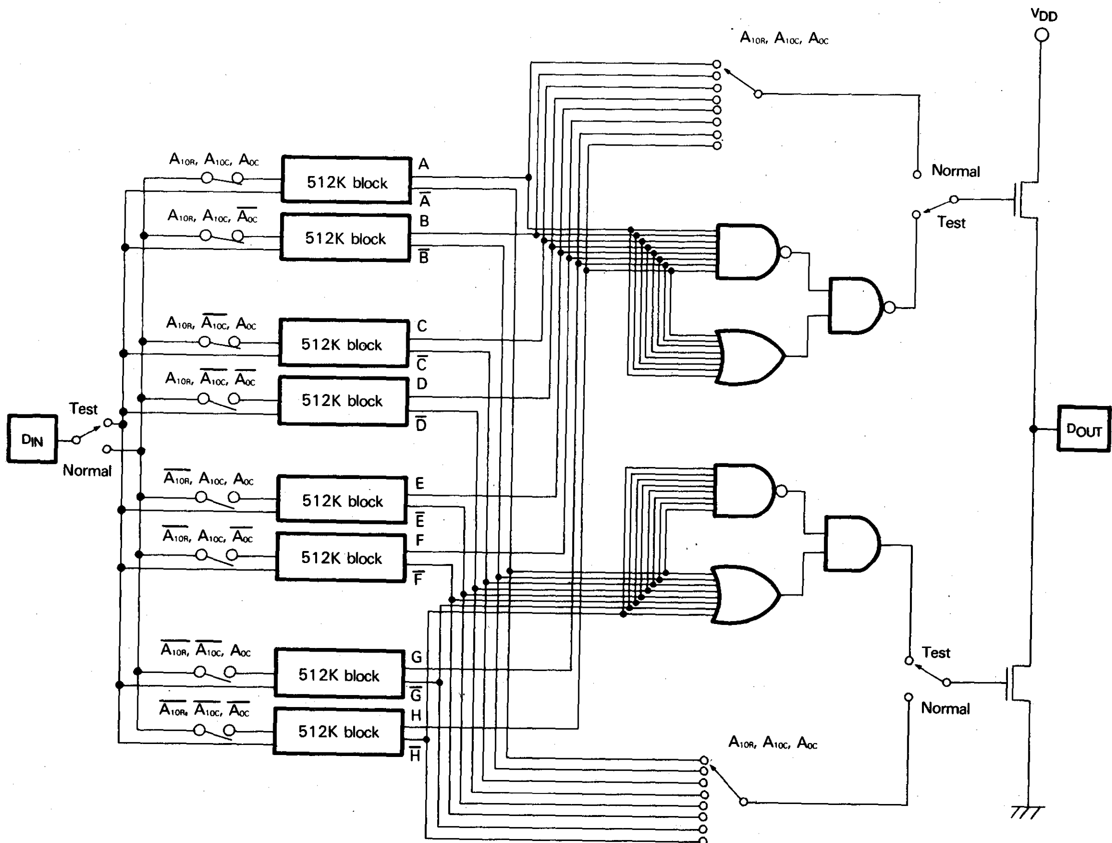


Fig. 1

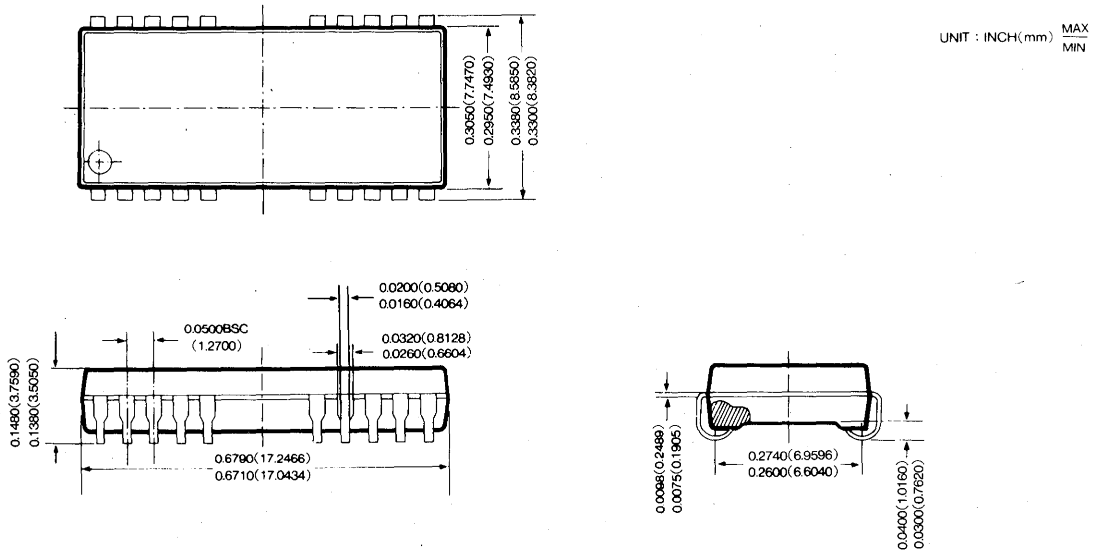
TEST MODE

The HY514100A is a DRAM organized 4,194,304 words by 1 bits and it is internally organized 524,288 words by 8 bits. In Test Mode, data are written into 8 sectors in parellel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal (all 1s or 0s), the data output indicates 1. If any of the bits differed, the data output pin indicates 0. The figure 1 shows the block diagram of HY514100A. In Test Mode, 4M×1 DRAM can be tested as if it were a 512K×8 DRAM.

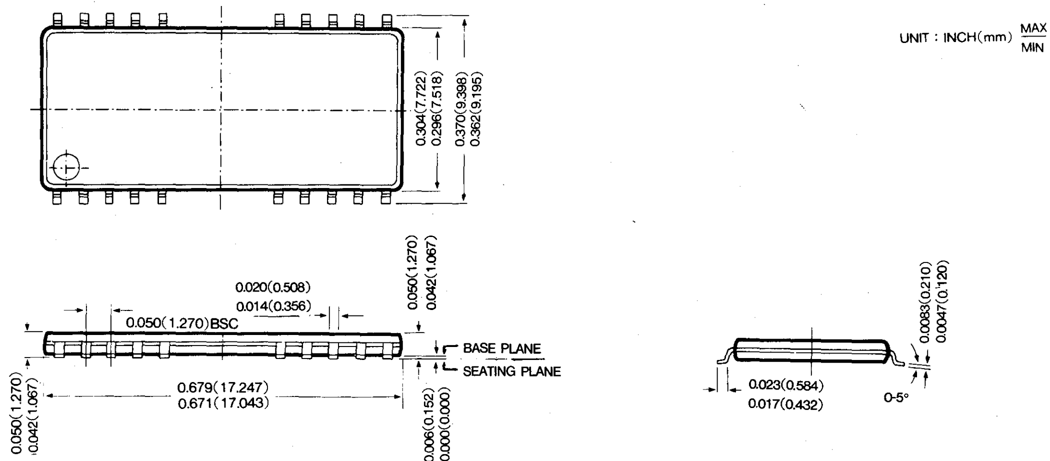
$\overline{\text{WE}}$, $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Cycle(Test Mode In) puts the device into Test Mode. And $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle or $\overline{\text{RAS}}$-Only-Refresh Cycle puts it back into Normal Mode. In Test Mode, $\overline{\text{WE}}$, $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle performs the refresh operation with the internal refresh address counter. The Test Mode funtion reducess test time to one-eighth of normal in case of N test pattern.

PACKAGE INFORMATION

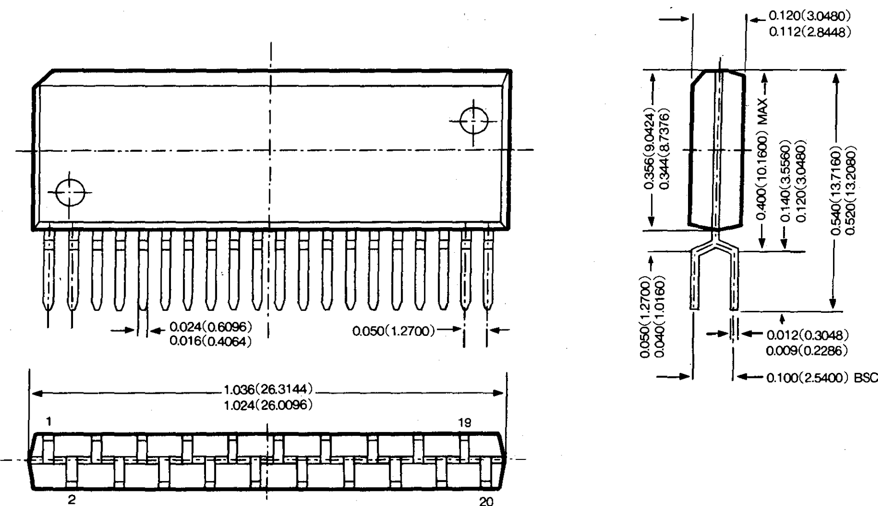
- 20/26 PIN SMALL OUT LINE J-FORM PACKAGE-300 MIL



- **20/26 PIN THIN SMALL OUTLINE PACKAGE−300 MIL**



- **20 PIN ZIGZAG-IN-LINE PACKAGE-400 MIL**



MEMO

PRELIMINARY

HYUNDAI SEMICONDUCTOR — HY514100AL

4M×1-Bit CMOS DRAM

M1H1200A-MAR92

DESCRIPTION

The HY514100AL is a high speed, low power 4,194,304 words by 1 bit CMOS dynamic random access memory, fabricated with the HYUNDAI CMOS process. The HY514100AL offers a fast page mode operation, fast usable speed and inherently high CMOS reliability.

All inputs and output are TTL compatible. Multiplexed address inputs permit the HY514100AL to be packaged in a standard 20/26 pin SOJ, TSOP, and 20 pin ZIP.

HY514100AL design is optimized for cache based mainframe, and microcomputers, graphics, digital signal processing, and high performance microprocessor system.

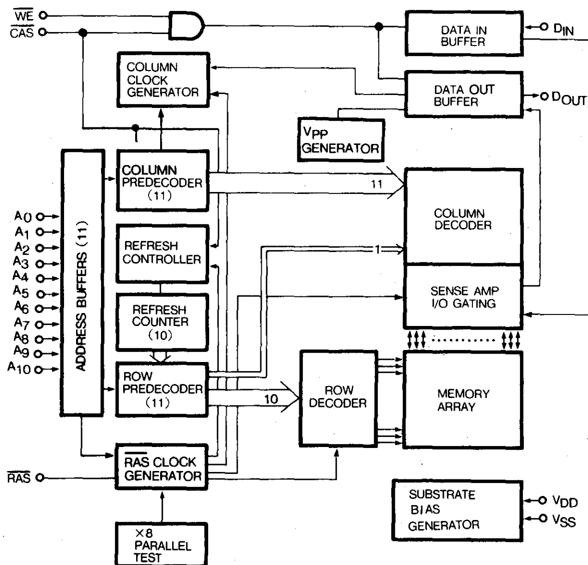
FEATURES

- **Low power dissipation**
  - **Operating Current, 80ns : 85mA(max.)**
  - **TTL Standby Current : 2mA(max.)**
  - **CMOS Standby Current : 200μA(max.)**
  - **Battery Back Up Current : 300μA(max.)**
- **Read-Modify-Write Capability**
- **RAS-only, Hidden, CAS-Before-RAS Refresh Capability**
- **Fast Page mode and Test mode Capability**
- **Single 5V± 10% power supply**
- **1024 refresh cycles/128ms**
- **High reliability 300 mil 20/26 pin SOJ, TSOP and 400mil 20pin ZIP.**
- **Fast access time and cycle time(ns)**

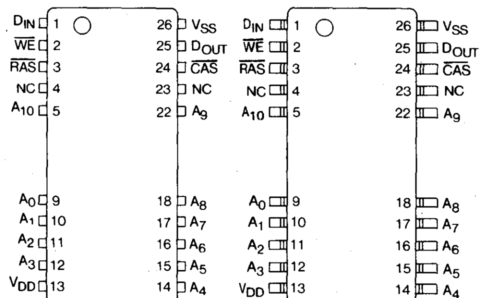
	HY514100AL-60	HY514100AL-70	HY514100AL-80
Max RAS Access Time, t_{RAC}	60	70	80
Max CAS Access Time, t_{CAC}	20	20	25
Min Fast Page Mode Cycle Time, t_{PC}	40	45	55
Min Cycle Time, t_{RC}	120	130	150

3

BLOCK DIAGRAM

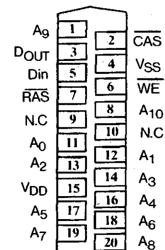


PIN CONNECTIONS



PIN NAMES

RAS	ROW ADDRESS STROBE
CAS	COLUMN ADDRESS STROBE
WE	WRITE ENABLE
A_0-A_{10}	ADDRESS INPUT
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
T_{SOLDER}	Soldering Temperature Time	260, 10	℃, sec
P_T	Power Dissipation	735	mW

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY514100AL MIN.	HY514100AL MAX.	UNIT	NOTE
$\mid I_{LI} \mid$	Input Leakage Current(any input pin)	0V≤V_{IN}≤6.5V, All other pin not under test=V_{SS}		−	10	μA	
$\mid I_{LO} \mid$	Output Leakage Current for High Impedance State	D_{OUT} is disable, 0V≤V_{OUT}≤5.5V		−	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$\overline{RAS}$, $\overline{CAS}$, Address cycling, t_{RC}=t_{RC}(min.)	−60	−	105	mA	1, 2, 5
			−70	−	95		
			−80	−	85		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$=$\overline{CAS}$=V_{IH}		−	2	mA	
I_{DD3}	V_{DD} Supply Current, RAS-only Refresh	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}, t_{RC}=t_{RC}(min.)	−60	−	105	mA	1, 4
			−70	−	95		
			−80	−	85		
I_{DD4}	V_{DD} Supply Current, Fast page mode	$\overline{RAS}$=V_{IL}, Address cycling, t_{PC}=t_{PC}(min.)	−60	−	65	mA	1, 2, 5
			−70	−	55		
			−80	−	45		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}$=$\overline{CAS}$=V_{DD}−0.2V		−	200	μA	
I_{DD6}	V_{DD} Supply Current, CAS-Before-RAS Refresh	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{RC}(min.)	−60	−	105	mA	1, 4
			−70		95		
			−80	−	85		
I_{DD7}	V_{DD} Supply Current, Battery Back up	$\overline{CAS}$=CBR cycling or 0.2V, $\overline{WE}$=V_{DD}−0.2V, Add=V_{DD}−0.2V or 0.2V I/O=V_{DD}−0.2V or 0.2V or open, t_{RC}=125μs, t_{RAS}=t_{RAS}(min.) ~300ns		−	300	μA	1
		Same as above except t_{RAS}=300ns~1μs		−	400	μA	1, 5
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		−	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	−	V	

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 3, 4, 5, 6

#	SYMBOL	PARAMETER	HY514100AL						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
2	t_{RWC}	Read-Modify-Write Cycle Time	145	–	155	–	180	–	ns	
3	t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	55	–	ns	
4	t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	65	–	70	–	85	–	ns	
5	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	8, 13
6	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	8, 13
7	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	8, 13
8	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	8
9	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	ns	8
10	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	9
11	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	7
12	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	50	–	60	–	ns	
13	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	200K	70	200K	80	200K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
17	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
18	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	55	ns	13
19	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	14
20	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
21	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
22	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
23	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
24	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
25	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
26	t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
27	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
28	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
29	t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	10
30	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	10
31	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
32	t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
33	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
34	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
35	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
36	t_{DS}	Data Set-up Time	0	–	0	–	0	–	ns	11
37	t_{DH}	Data Hold Time	15	–	15	–	15	–	ns	11
38	t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
39	t_{REF}	Refresh Period	–	128	–	128	–	128	ms	
40	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	12
41	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	20	–	20	–	25	–	ns	12
42	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	60	–	70	–	80	–	ns	12
43	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	30	–	35	–	40	–	ns	12

#	SYMBOL	PARAMETER	HY514100AL						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
44	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
45	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	30	–	ns	
46	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
47	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter test cycle)	30	–	35	–	40	–	ns	
48	t_{WTS}	Write Command Set-up Time(Test Mode In)	10	–	10	–	10	–	ns	
49	t_{WTH}	Write Command Hold Time(Test Mode In)	10	–	10	–	10	–	ns	
50	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
51	t_{WRH}	$\overline{WE}$ to RAS Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

AC CHARACTERISTICS IN TEST MODE NOTE 11

#	SYMBOL	PARAMETER	HY514100AL						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
52	t_{RC}	Random Read or Write Cycle Time	125	–	135	–	155	–	ns	
53	t_{RWC}	Read-Modify-Write Cycle Time	150	–	160	–	185	–	ns	
54	t_{PC}	Fast Page Mode Cycle Time	45	–	50	–	60	–	ns	
55	t_{PRWC}	Fast Page Mode RMW Cycle Time	70	–	75	–	90	–	ns	
56	t_{RAC}	Access Time from $\overline{RAS}$	–	65	–	75	–	85	ns	8, 13
57	t_{CAC}	Access Time form $\overline{CAS}$	–	25	–	25	–	30	ns	8, 13
58	t_{AA}	Access Time form Column Address	–	35	–	40	–	45	ns	8, 13
59	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	45	–	55	ns	8
60	t_{RAS}	$\overline{RAS}$ Pulse Width	65	10K	75	10K	85	10K	ns	
61	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	65	200K	75	200K	85	200K	ns	
62	t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
63	t_{CSH}	$\overline{CAS}$ Hold Time	65	–	75	–	85	–	ns	
64	t_{CAS}	$\overline{CAS}$ Pulse Width	25	10K	25	10K	30	10K	ns	
65	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	45	–	ns	
66	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	25	–	25	–	30	–	ns	12
67	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	65	–	75	–	85	–	ns	12
68	t_{AWD}	Column Address to $\overline{WE}$ Dealy Time	35	–	40	–	45	–	ns	12

NOTES :

1. I_{DD1}, I_{DD3}, I_{DD4}, I_{DD6}, I_{DD7} depend on cycle rate.
2. I_{DD1}, I_{DD4} depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. It depends on user whether column address is changed or not at least once while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
5. Only t_{RAS}(max.)=1μs is applied to refresh of batlery-back up but $t_{RAS(max.)}$=10μs is applied to normal functional operating.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle : If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.) the cycle is a read-modify-write cycle and data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out(at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
15. These specifications are applied to the test mode.

3

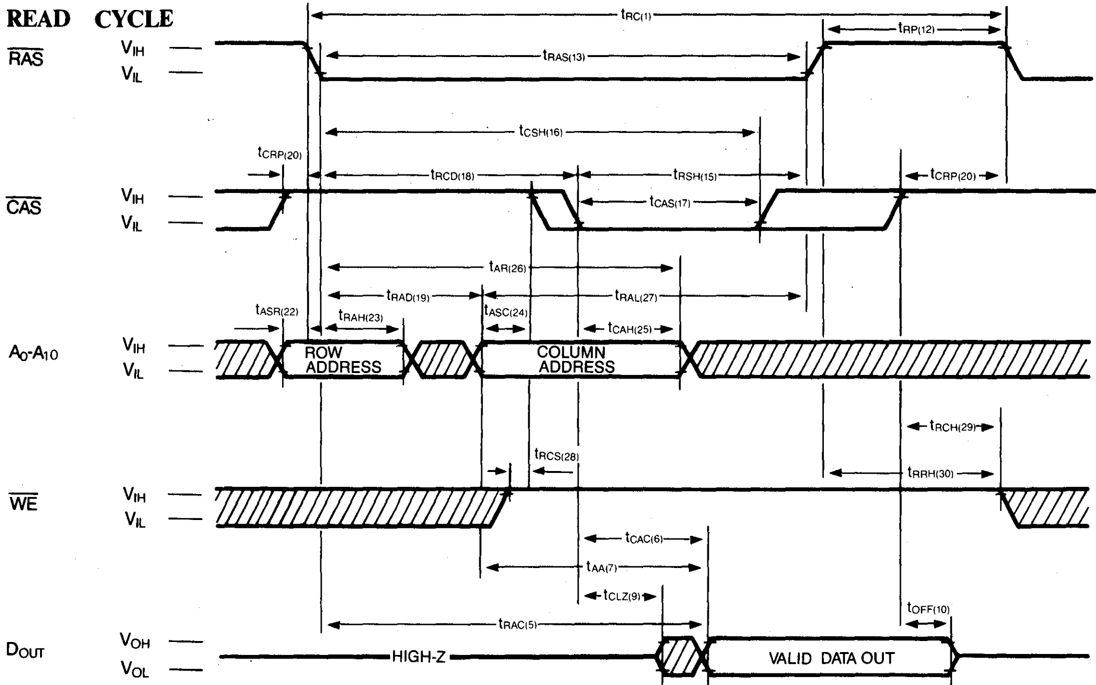
CAPACITANCE

(T_A=0°C to 70°C, V_{DD}=5V±10%, f=1MHz)

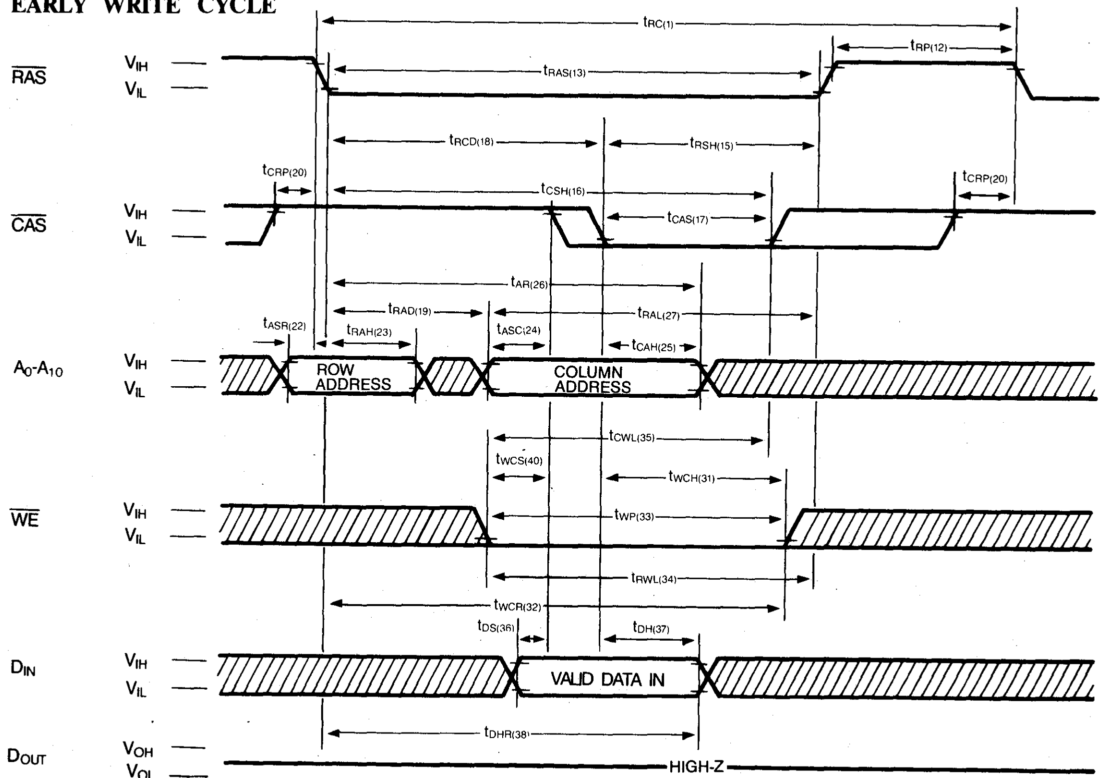
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_{10}, D_{IN})	–	5	pF
C_{IN2}	Input Capacitance($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	–	7	pF
C_{OUT}	Output Capacitance(D_{OUT})	–	7	pF

TIMING DIAGRAM

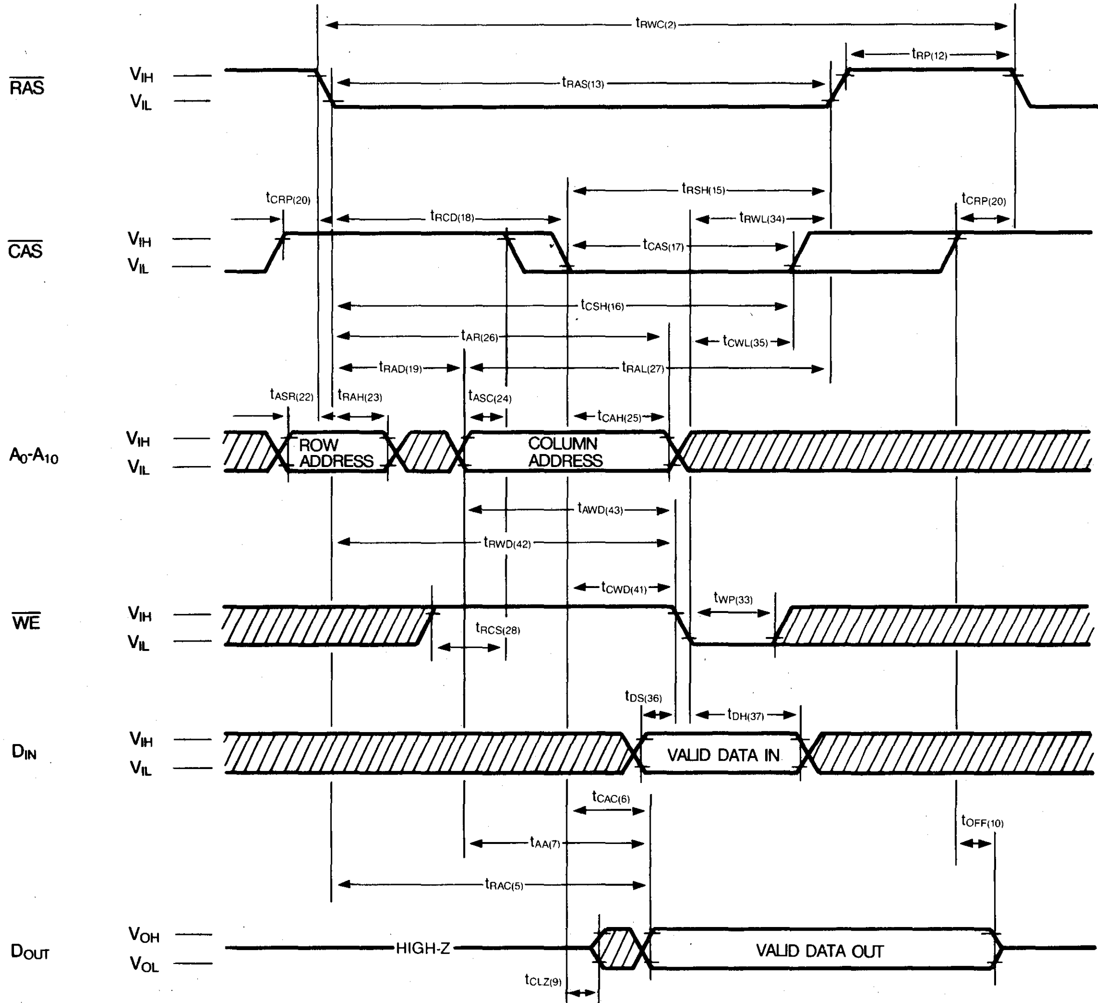
READ CYCLE



EARLY WRITE CYCLE

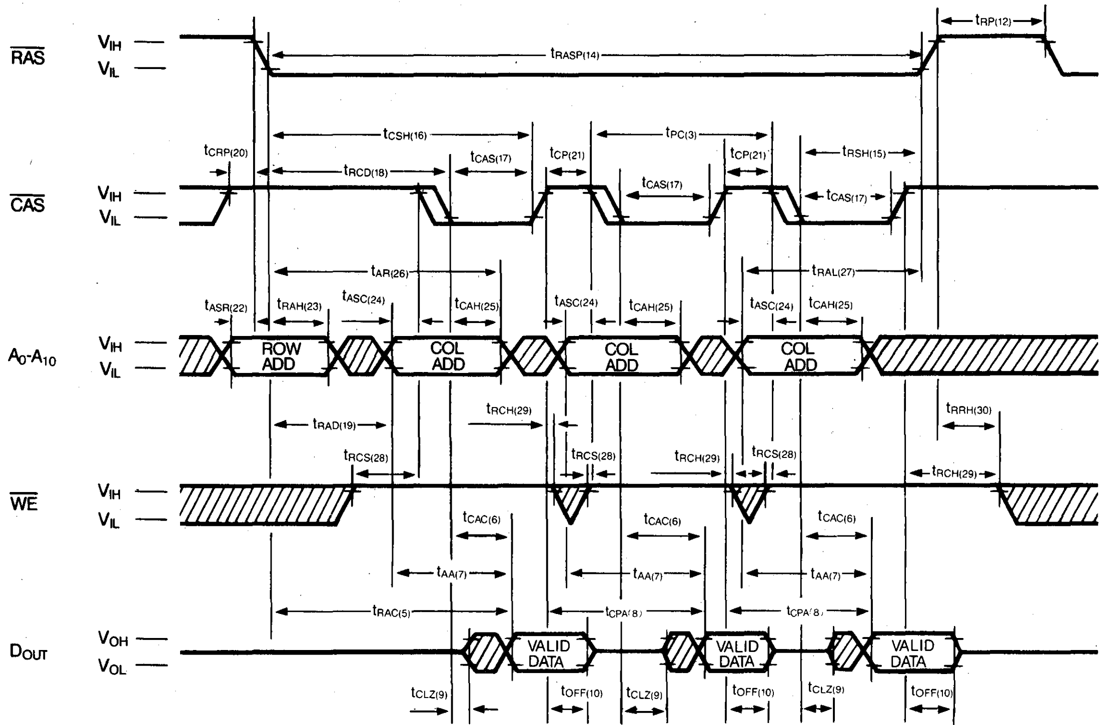


READ-MODIFY-WRITE CYCLE

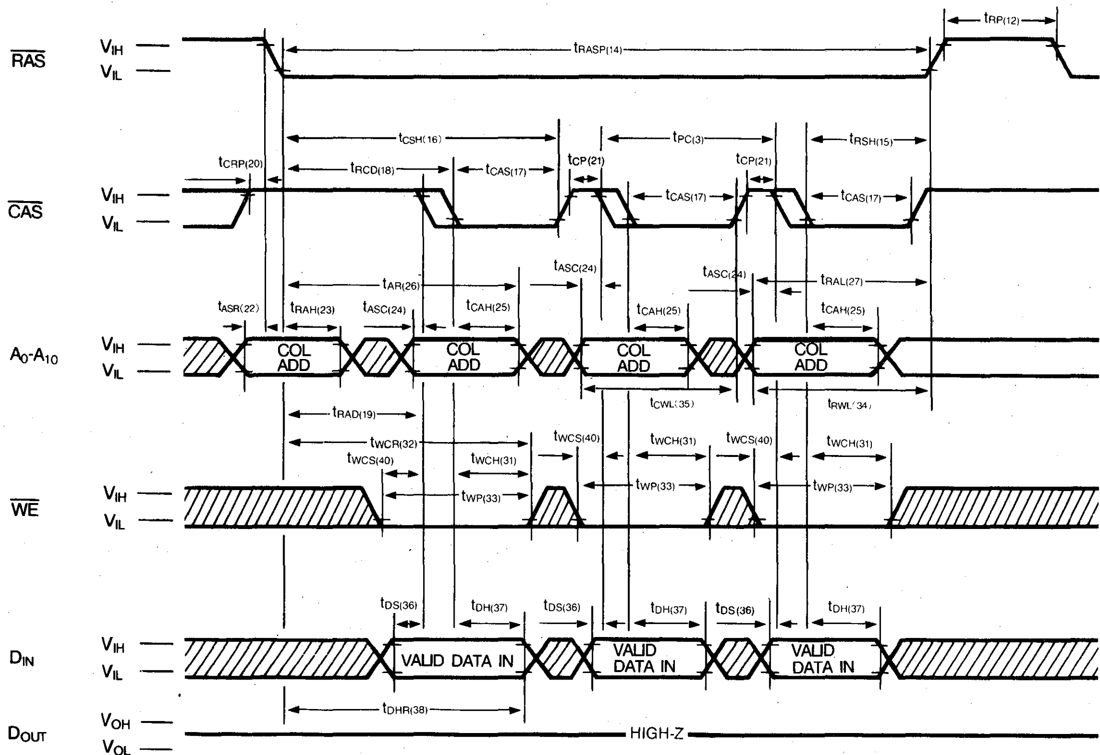


3

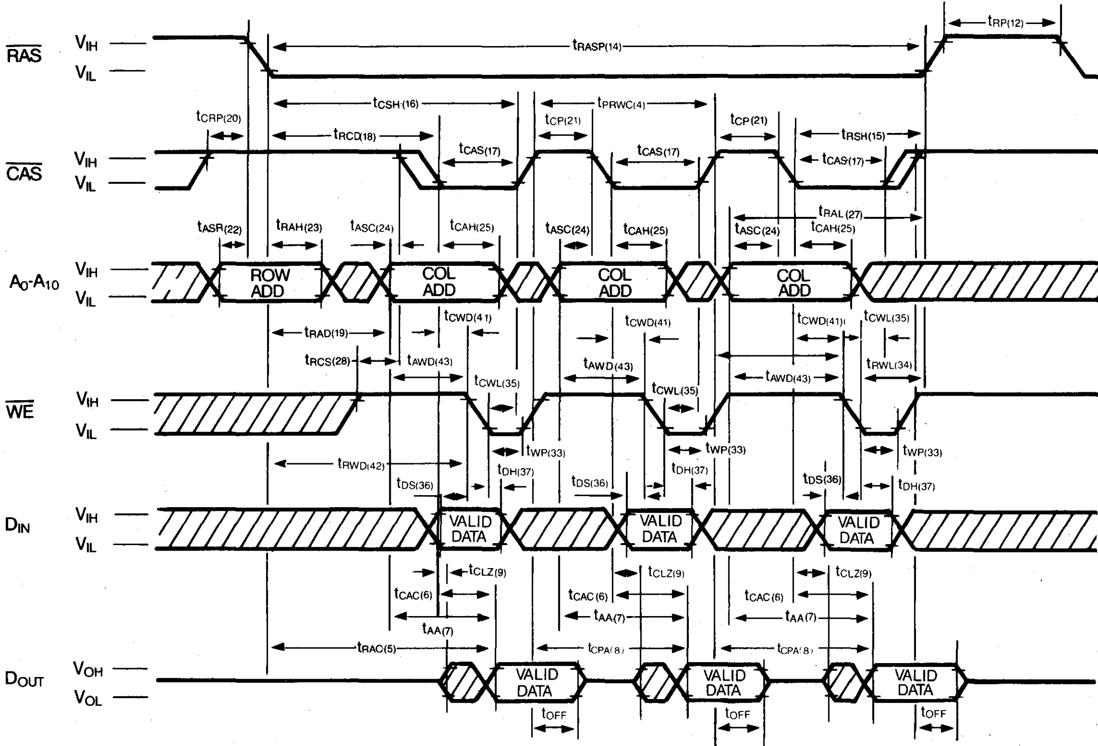
FAST PAGE MODE READ CYCLE



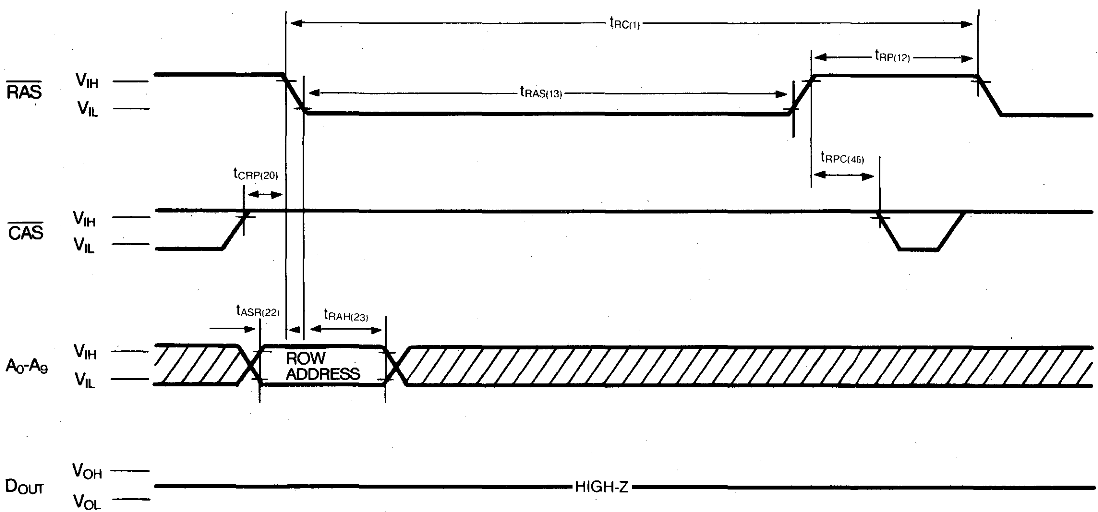
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE

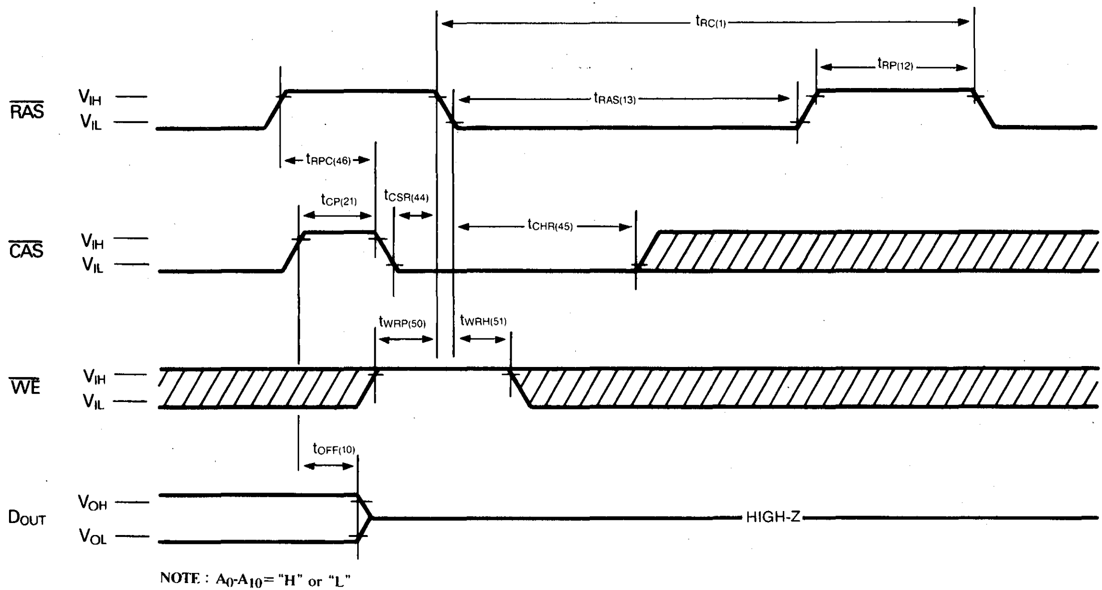


RAS-ONLY REFRESH CYCLE

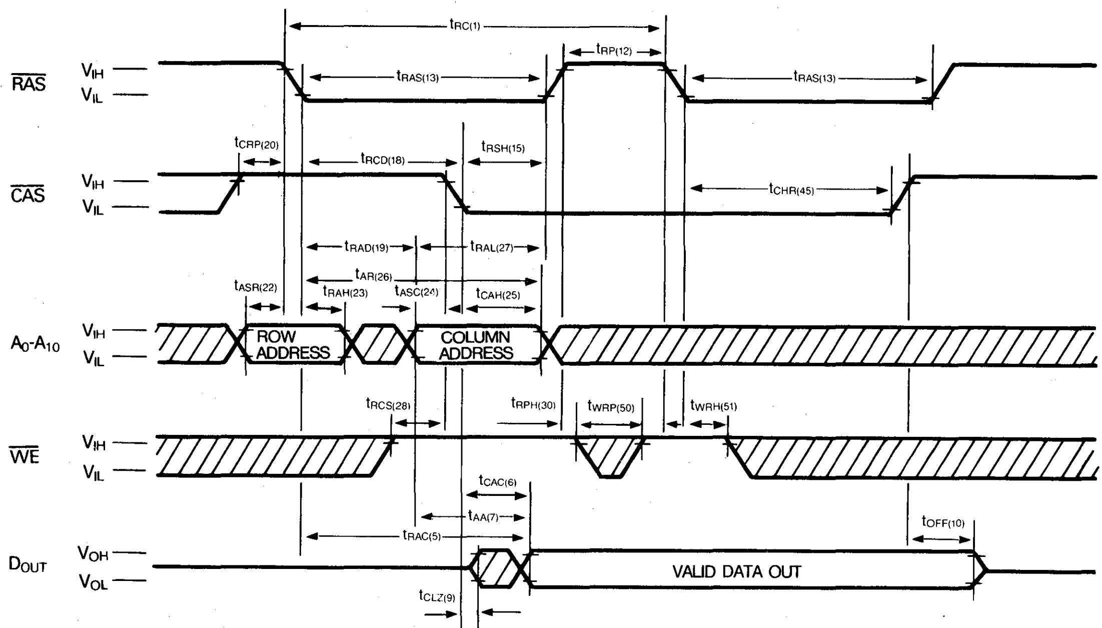


NOTE : $\overline{WE}$ and A_{10}="H" or "L"

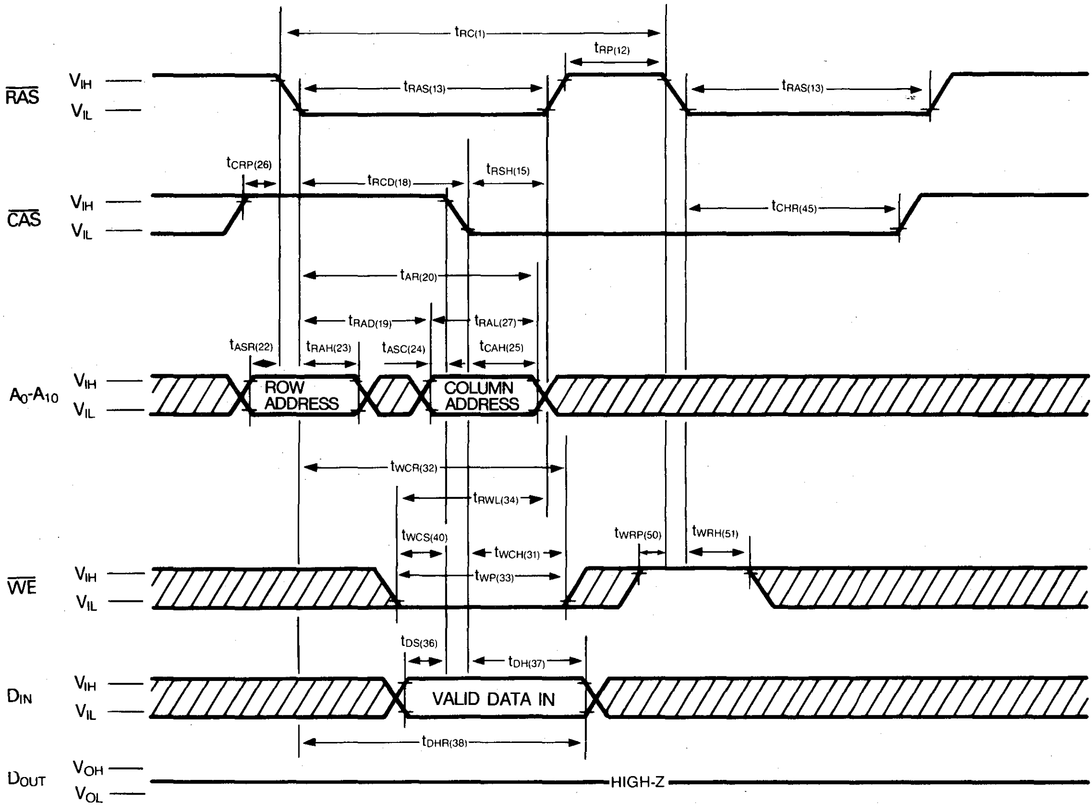
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



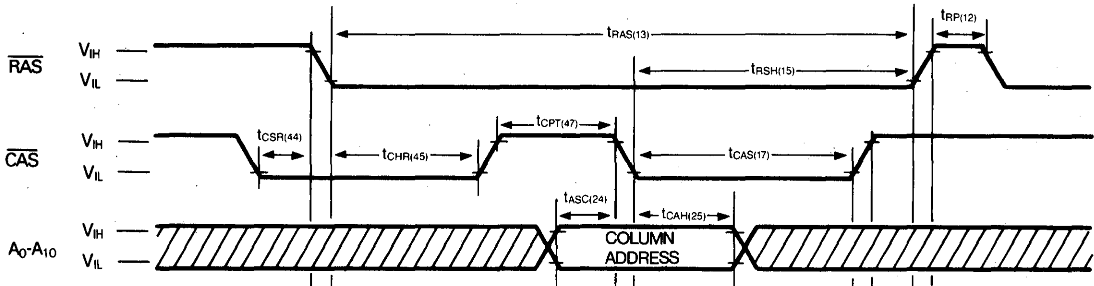
HIDDEN REFRESH CYCLE (READ)



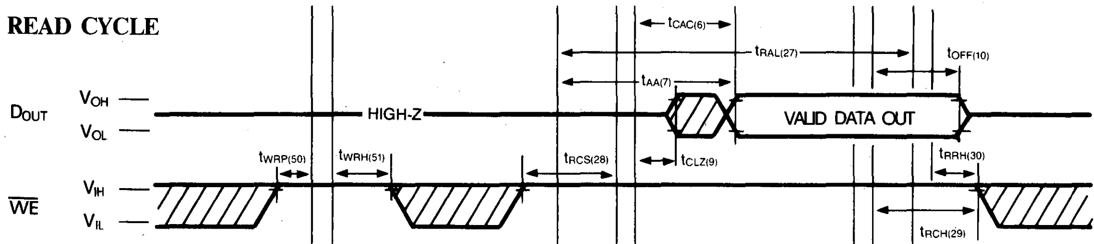
HIDDEN REFRESH CYCLE (WRITE)



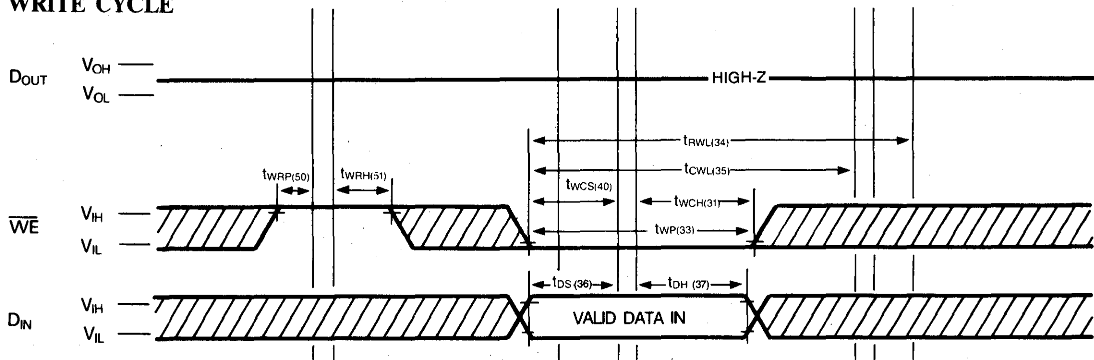
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



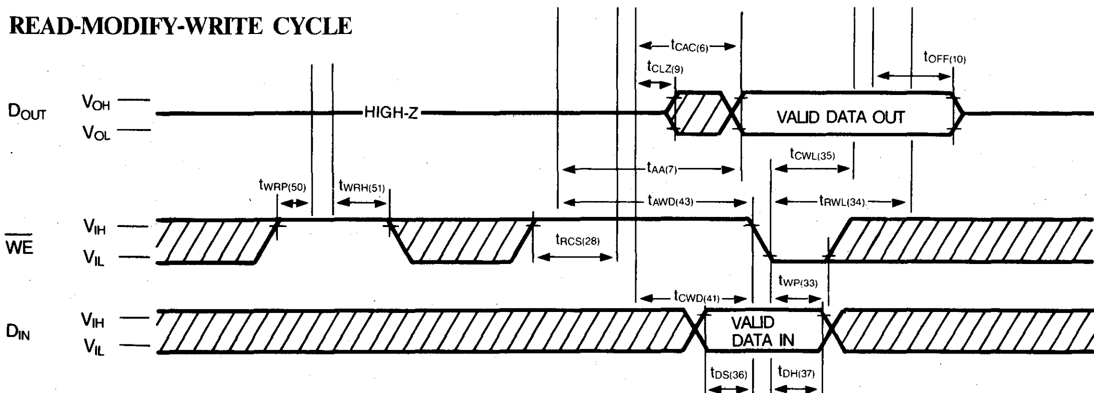
READ CYCLE



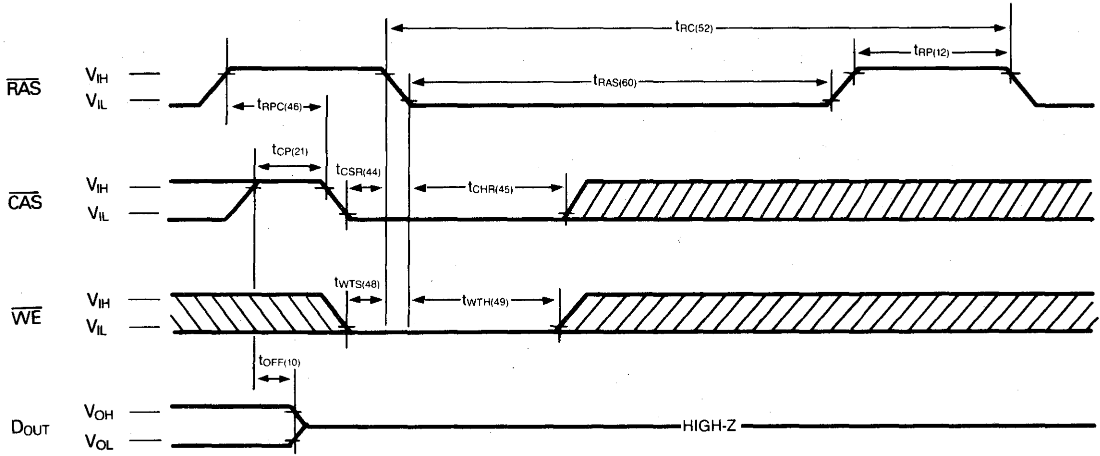
WRITE CYCLE



READ-MODIFY-WRITE CYCLE



TEST MODE IN CYCLE



NOTE : D_{IN} and A_0-A_{10} : "H" or "L"

BLOCK DIAGRAM IN TEST MODE

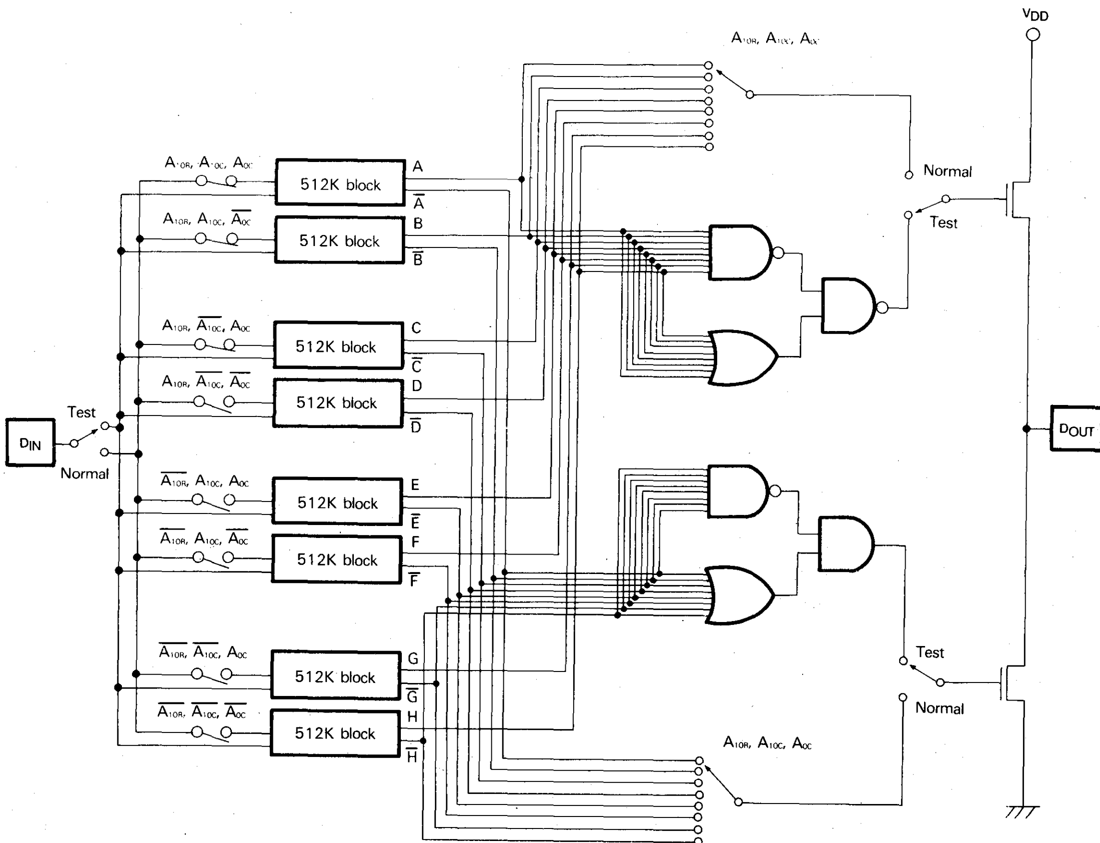


Fig. 1

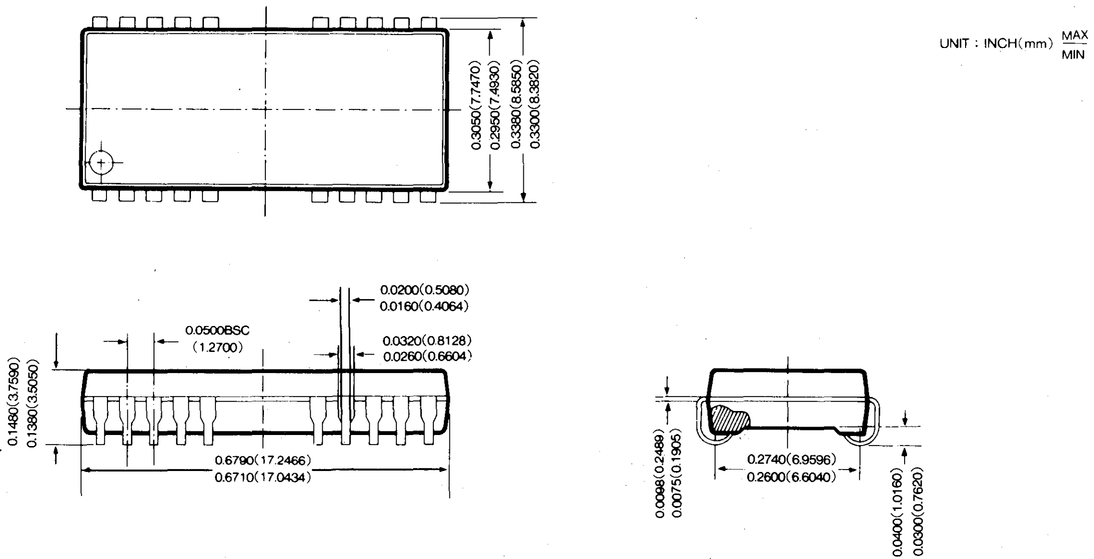
TEST MODE

The HY514100AL is a DRAM organized 4,194,304 words by 1 bits and it is internally organized 524,288 words by 8 bits. In Test Mode, data are written into 8 sectors in parellel and retrieved the same way. A_{10R}, A_{10C} and A_{0C} are not used. If, upon reading, all bits are equal(all 1s or 0s), the data output indicates 1. If any of the bits differed, the data output pin indicates 0. The figure 1 shows the block diagram of HY514100AL. In Test Mode, 4M×1 DRAM can be tested as if it were a 512K×8 DRAM.

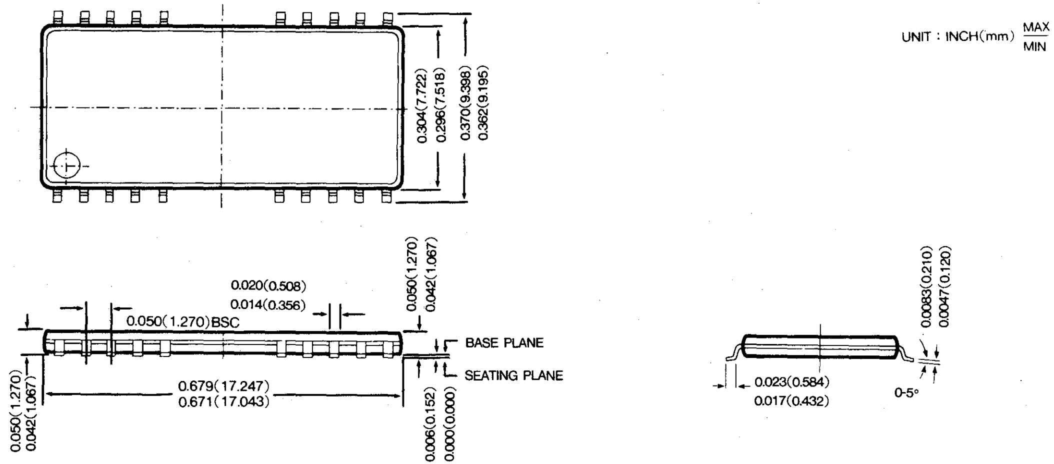
$\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle(Test Mode In) puts the device into Test Mode. And $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle or $\overline{RAS}$-Only Refresh Cycle puts it back into Normal Mode. In Test Mode, $\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle performs the refresh operation with the internal refresh address counter. The Test Mode funtion reduces test time to one-eighth of normal in case of N test pattern.

PACKAGE INFORMATION

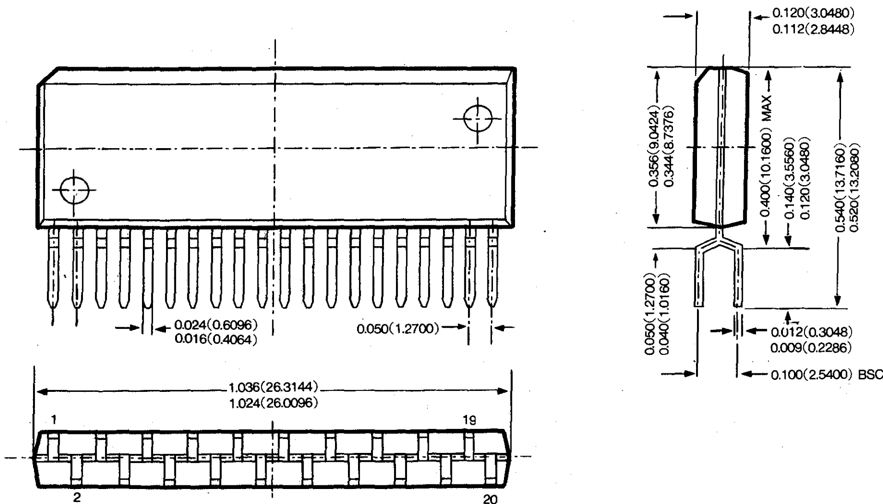
• 20/26 PIN SMALL OUTLINE J-FORM PACKAGE-300 MIL



- **20/26 PIN THIN SMALL OUTLINE PACKAGE−300 MIL**



- **20 PIN ZIGZAG-IN-LINE PACKAGE−400MIL**



3

MEMO

HY514400

1M×4-Bit CMOS DRAM

M1A1202A-JAN92

DESCRIPTION

The HY514400 is the new generation dynamic RAM organized 1,048,576 words by 4 bits. The HY514400 utilizes HYUNDAI's CMOS process technology as well as advanced circuit techniques to provide wide operating margins. Multiplexed address inputs permit the HY514400 to be packaged in a standard 20/26 pin plastic SOJ.

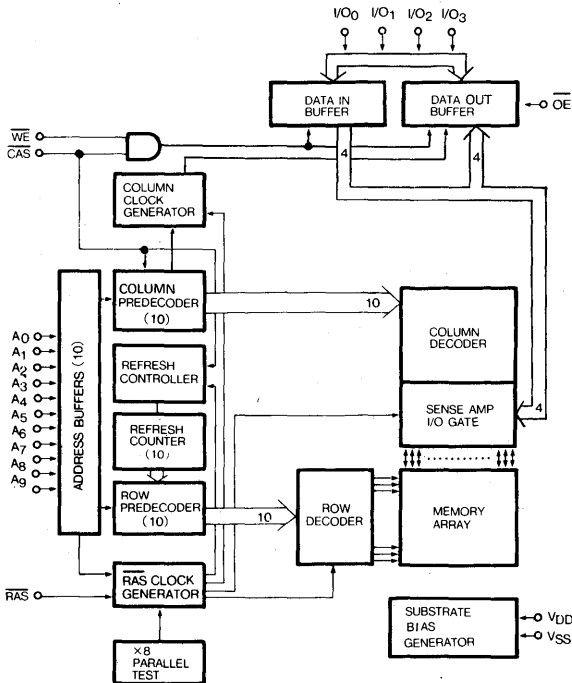
The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented feature include single power supply of 5V± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

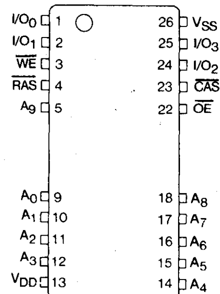
- **Low power dissipation**
  - **Operating Current, 100ns : 75mA(max.)**
  - **TTL Standby Current : 2mA(max.)**
  - **CMOS Standby Current : 1mA(max.)**
- **Read-Modify-Write Capability**
- **$\overline{RAS}$-only, Hidden, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Capability**
- **Common I/O capability**
- **Fast Page mode and Test mode capability**
- **1024 refresh cycles/16 ms**
- **High reliability 300 mil 20/26 pin SOJ**
- **Fast access time and cycle time(ns)**

	HY514400-70	HY514400-80	HY514400-10
Max $\overline{RAS}$ Access Time, t_{RAC}	70	80	100
Max $\overline{CAS}$ Access Time, t_{CAC}	20	25	25
Min Fast Page Mode Cycle Time, t_{PC}	50	50	60
Min Cycle Time, t_{RC}	130	150	180

BLOCK DIAGRAM



PIN CONNECTIONS



SOJ

PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
A_0-A_9	ADDRESS INPUT
I/O_0-I/O_3	DATA INPUT/OUTPUT
V_{DD}	POWER (+5V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	0.6	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY514400		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	0V≤V_{IN}≤6.5V, All other pin not under test=V_{SS}		−	10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	D_{OUT} is disable, 0V≤V_{OUT}≤5.5V		−	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$\overline{RAS}$, $\overline{CAS}$, Address cycling, t_{RC}=t_{RC}(min.)	−70	−	95	mA	1, 2
			−80	−	85		
			−10	−	75		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$=$\overline{CAS}$=V_{IH}		−	2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}, t_{RC}=t_{RC}(min.)	−70	−	95	mA	2
			−80	−	85		
			−10	−	75		
I_{DD4}	V_{DD} Supply Current, Fast page mode	$\overline{RAS}$=V_{IL}, Address cycling, t_{PC}=t_{PC}(min.)	−70	−	80	mA	1, 2
			−80	−	70		
			−10	−	60		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}$=$\overline{CAS}$=V_{DD}−0.2V		−	1	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{RC}(min.)	−70	−	95	mA	2
			−80	−	85		
			−10	−	75		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		−	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	−	V	

NOTES :
1. I_{DD1} and I_{DD4} depend on output loading, specified values are obtained with the output open.
2. I_{DD1}, I_{DD3}, I_{DD4} and I_{DD6} depend on cycle rate.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1, 2, 3

#	SYMBOL	PARAMETER	HY514400						UNIT	NOTES
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
2	t_{RWC}	Read-Modify-Write Cycle Time	185	–	210	–	245	–	ns	
3	t_{PC}	Fast Page Mode Cycle Time	50	–	50	–	60	–	ns	
4	t_{PRWC}	Fast Page Mode RMW Cycle Time	105	–	115	–	125	–	ns	
5	t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	4, 9
6	t_{CAC}	Access Time From $\overline{CAS}$	–	20	–	25	–	25	ns	4, 9
7	t_{AA}	Access Time from Column Address	–	35	–	40	–	45	ns	4, 9
8	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	45	–	45	–	55	ns	4
9	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	ns	4
10	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
11	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
12	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
13	t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	ns	
14	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	70	200K	80	200K	100	200K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	25	–	ns	
16	t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
17	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	25	10K	25	10K	ns	
18	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	55	25	75	ns	9
19	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	55	ns	10
20	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
21	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
22	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
23	t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
24	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
25	t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
26	t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	–	60	–	80	–	ns	
27	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	45	–	ns	
28	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
29	t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	6
30	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
31	t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
32	t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55	–	60	–	80	–	ns	
33	t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
34	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	25	–	ns	
35	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	25	–	ns	
36	t_{DS}	Data Set-up Time	0	–	0	–	0	–	ns	7
37	t_{DH}	Data Hold Time	15	–	15	–	20	–	ns	7
38	t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	–	60	–	80	–	ns	
39	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
40	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	8
41	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	–	55	–	60	–	ns	8
42	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100	–	110	–	135	–	ns	8
43	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	70	–	80	–	ns	8

3

#	SYMBOL	PARAMETER	HY514400						UNIT	NOTES
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
44	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
45	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	30	–	30	–	30	–	ns	
46	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
47	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40	–	40	–	50	–	ns	
48	t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	20	–	ns	
49	t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	25	ns	
50	t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	25	–	ns	
51	t_{OEZ}	Output Buffer Turn-off Delay Time from $\overline{OE}$	0	20	0	20	0	20	ns	
52	t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	25	–	ns	
53	t_{WTS}	Write Command Set-up Time(Test Mode In)	10	–	10	–	10	–	ns	
54	t_{WTH}	Write Command Hold Time(Test Mode In)	10	–	10	–	10	–	ns	
55	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
56	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	
57	t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay	70	–	75	–	85	–	ns	
58	t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	–	45	–	50	–	ns	

AC CHARACTERISTICS IN THE TEST MODE NOTE : 11

#	SYMBOL	PARAMETER	HYM514400						UNIT	NOTES
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
59	t_{RC}	Random Read or Write Cycle Time	135	–	155	–	185	–	ns	
60	t_{RWC}	Read-Modify-Write Cycle Time	190	–	215	–	250	–	ns	
61	t_{PC}	Fast Page Mode Cycle Time	55	–	55	–	65	–	ns	
62	t_{PRWC}	Fast Page Mode RMW Cycle Time	110	–	120	–	130	–	ns	
63	t_{RAC}	Access Time from $\overline{RAS}$	–	75	–	85	–	105	ns	4, 9
64	t_{CAC}	Access Time from $\overline{CAS}$	–	25	–	30	–	30	ns	4, 9
65	t_{AA}	Access Time from Column Address	–	40	–	45	–	50	ns	4, 9
66	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	50	–	50	–	60	ns	4
67	t_{RAS}	$\overline{RAS}$ Pulse Width	75	10K	85	10K	105	10K	ns	
68	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	75	200K	85	200K	105	200K	ns	
69	t_{RSH}	$\overline{RAS}$ Hold Time	25	–	30	–	30	–	ns	
70	t_{CSH}	$\overline{CAS}$ Hold Time	75	–	85	–	105	–	ns	
71	t_{CAS}	$\overline{CAS}$ Pulse Width	25	10K	30	10K	30	10K	ns	
72	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	45	–	50	–	ns	
73	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	55	–	60	–	65	–	ns	8
74	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	105	–	115	–	140	–	ns	8
75	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	70	–	75	–	85	–	ns	8
76	t_{OEA}	$\overline{OE}$ Access Time	–	25	–	25	–	30	ns	
77	t_{OED}	$\overline{OE}$ to Data Delay	25	–	25	–	30	–	ns	
78	t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	25	–	30	–	ns	

NOTES :

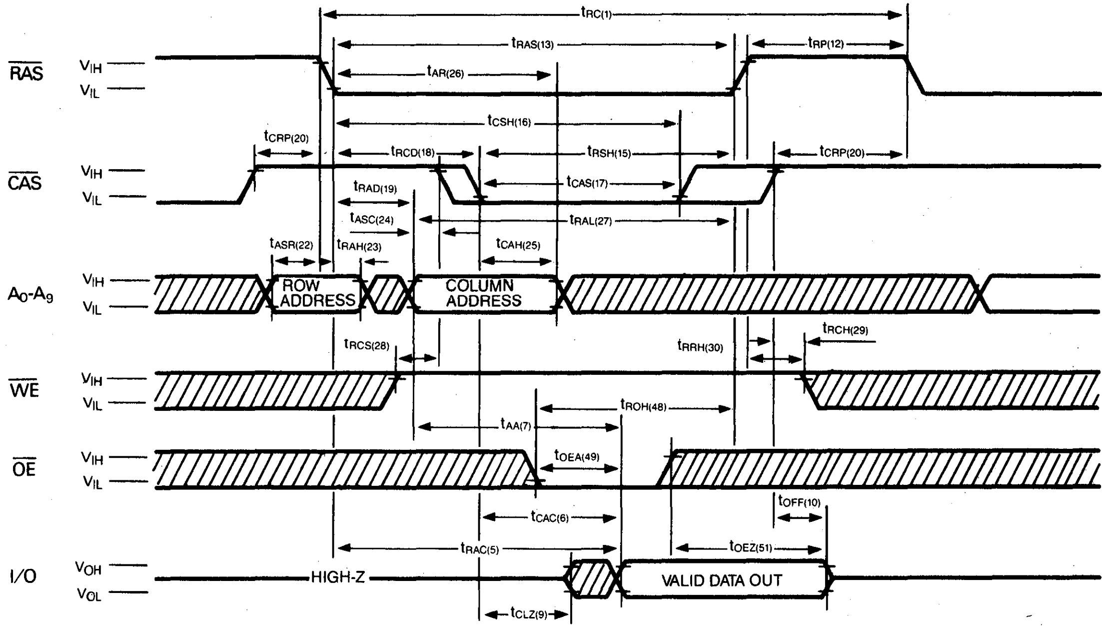
1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) and t_{OEZ} defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
8. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle : If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.) the cycle is a read-modify-write cycle and data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
10. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. These specifications are applied to the test mode.

CAPACITANCE
(T_A=0°C to 70°C, V_{DD}=5V± 10%, f=1MHz)

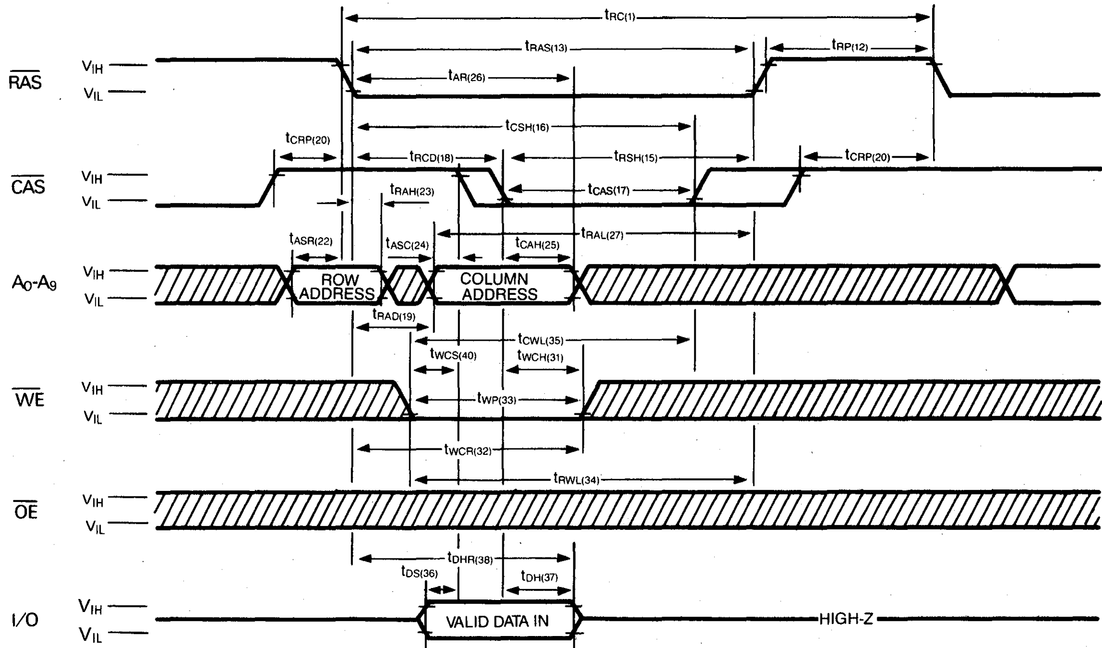
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_9, Data In)	–	5	pF
C_{IN2}	Input Capacitance($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	–	7	pF
C_{OUT}	Output Capacitance(Data Out)	–	7	pF

TIMING DIAGRAM

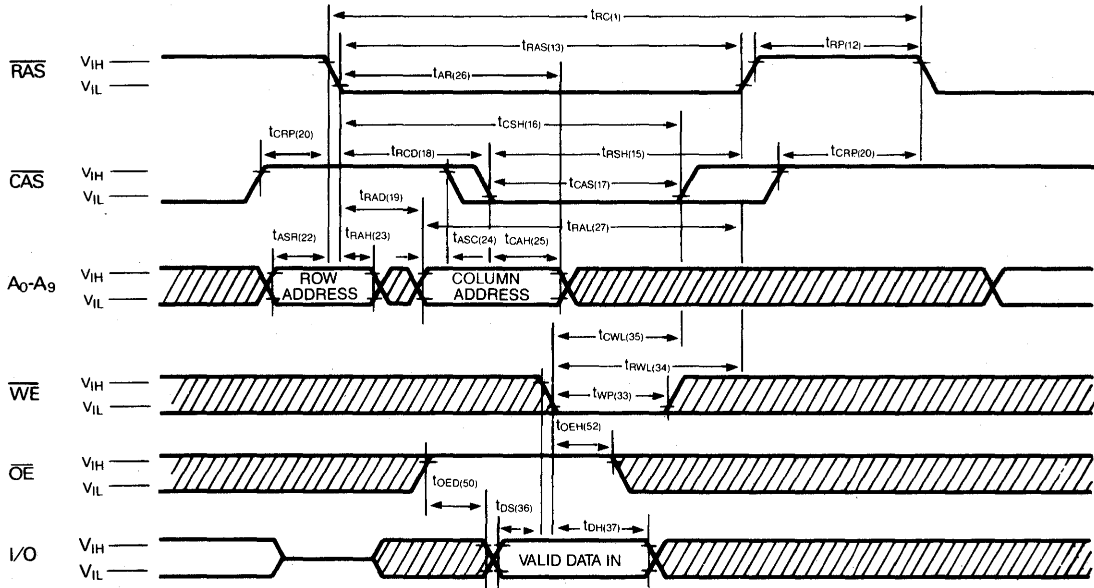
READ CYCLE



WRITE CYCLE



WRITE CYCLE($\overline{OE}$ CONTROLLED WRITE)



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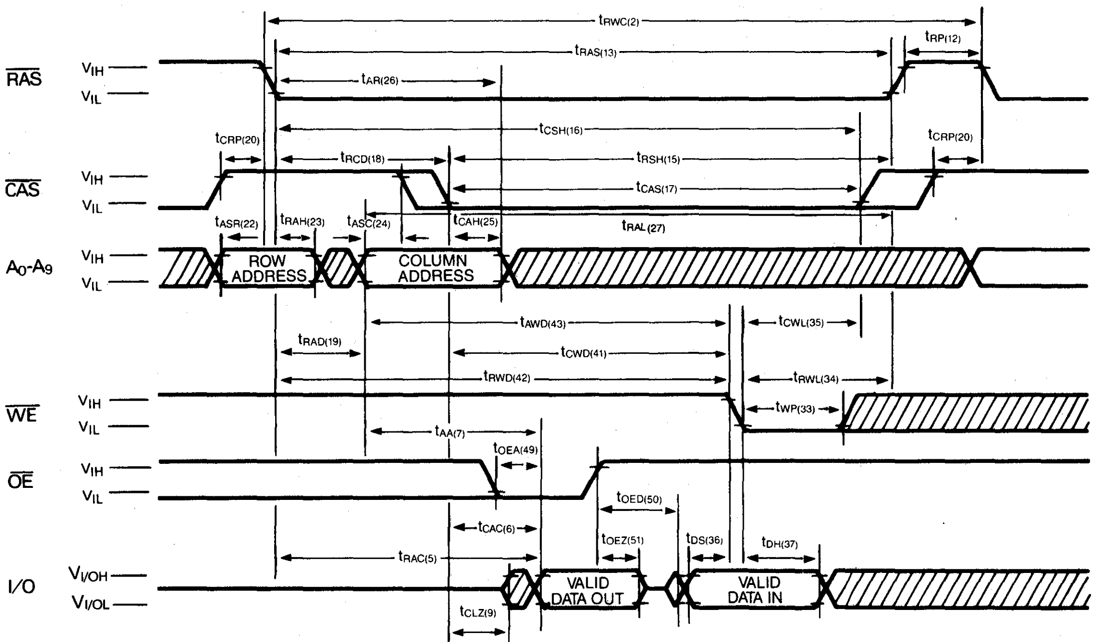
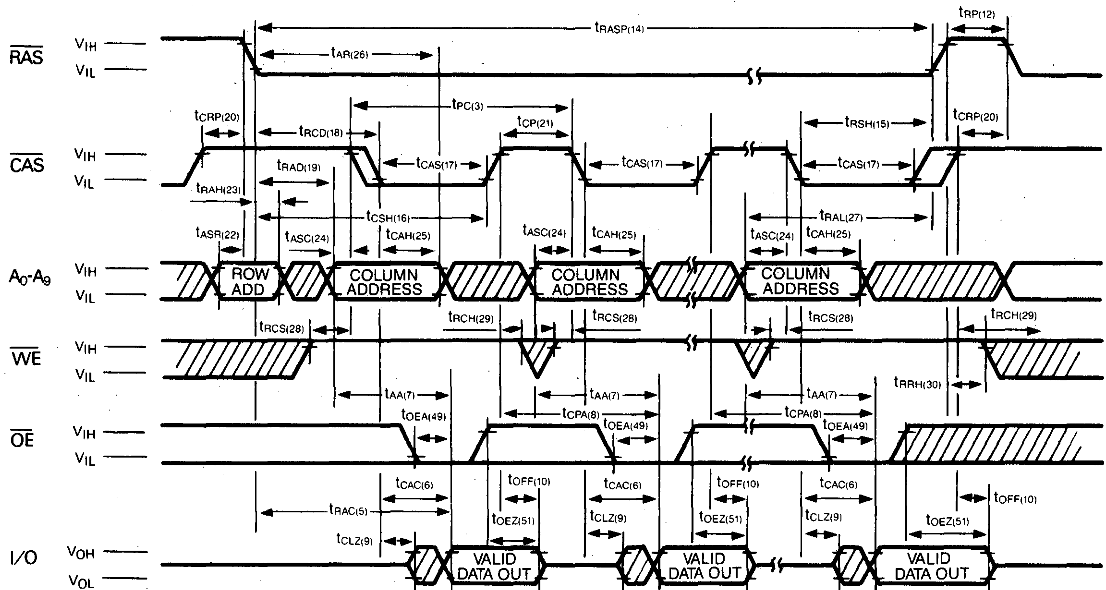
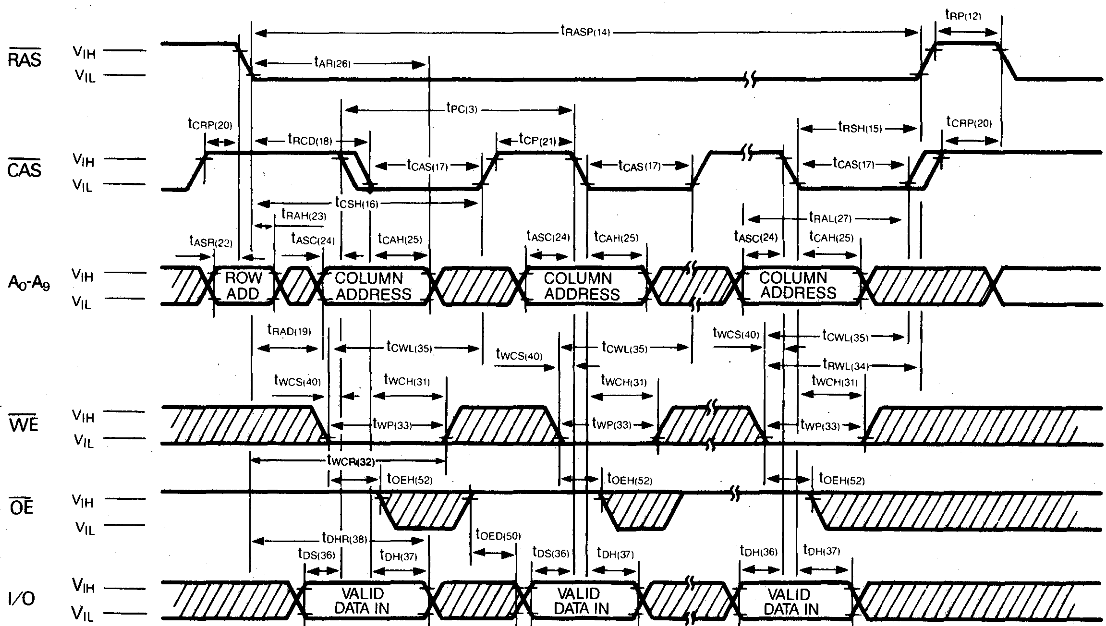
READ-MODIFY-WRITE CYCLE



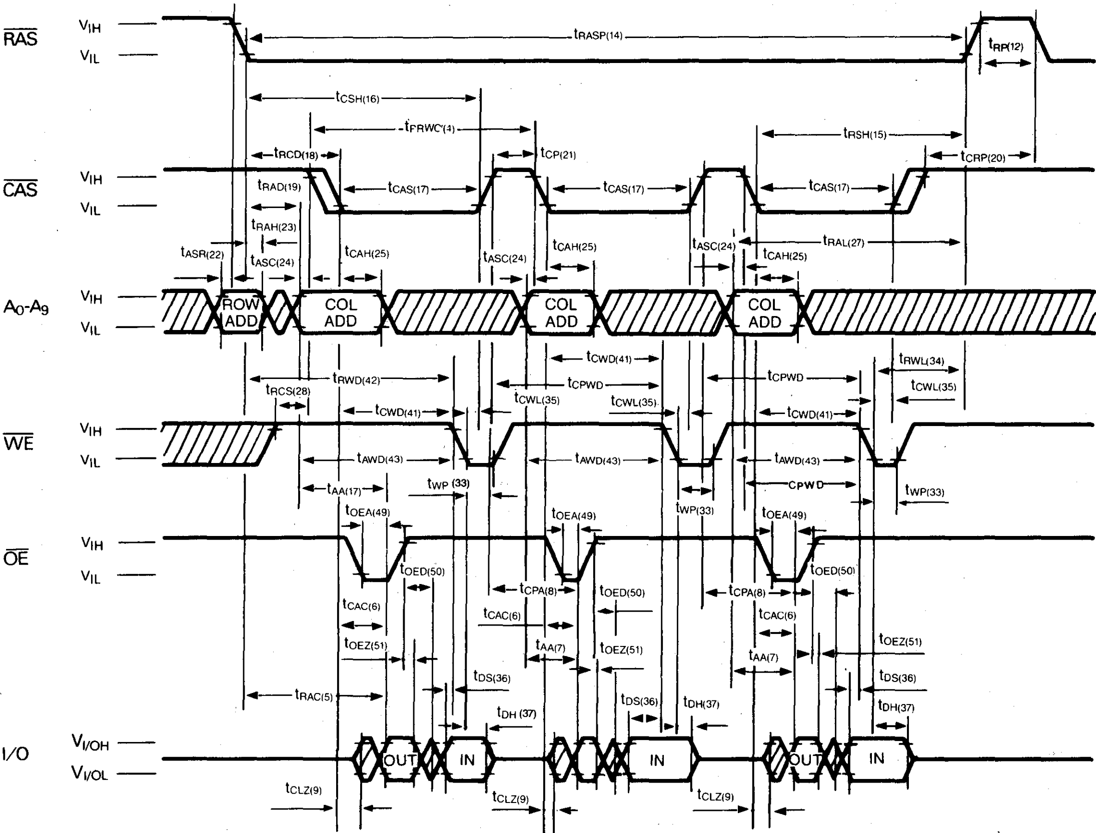
FAST PAGE MODE READ CYCLE



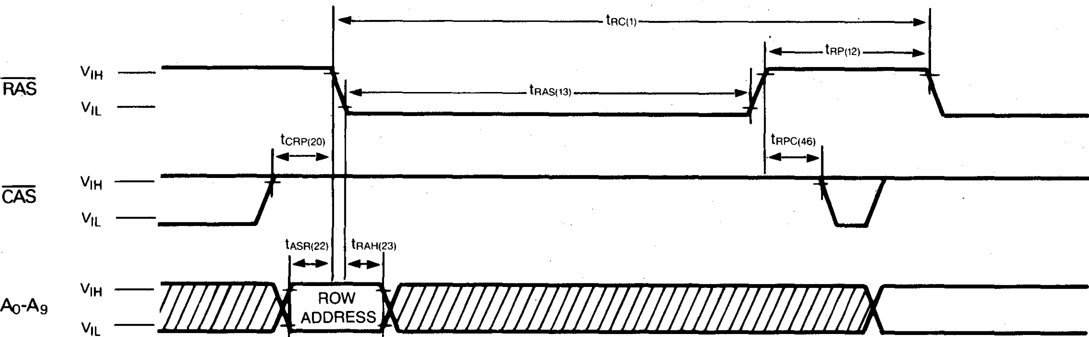
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



NOTE : $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

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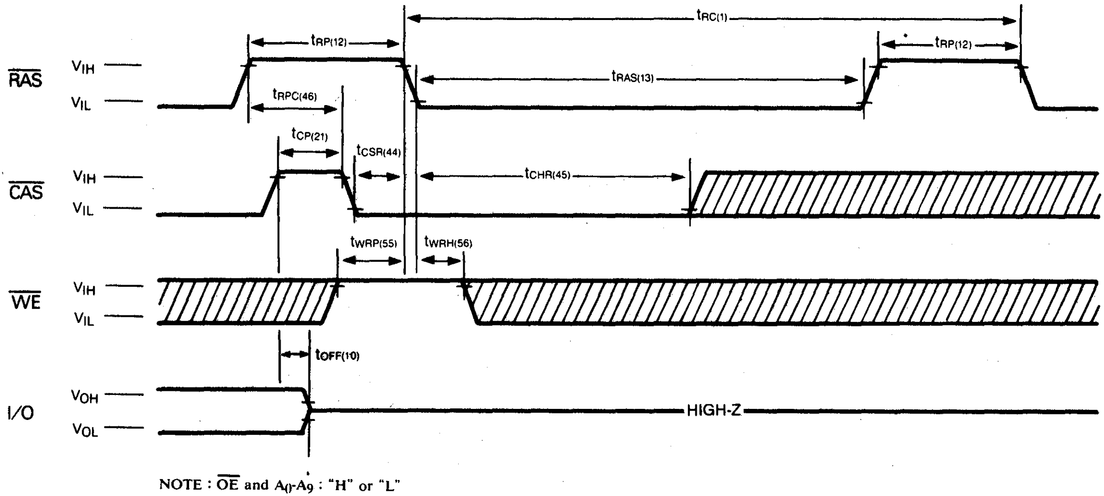
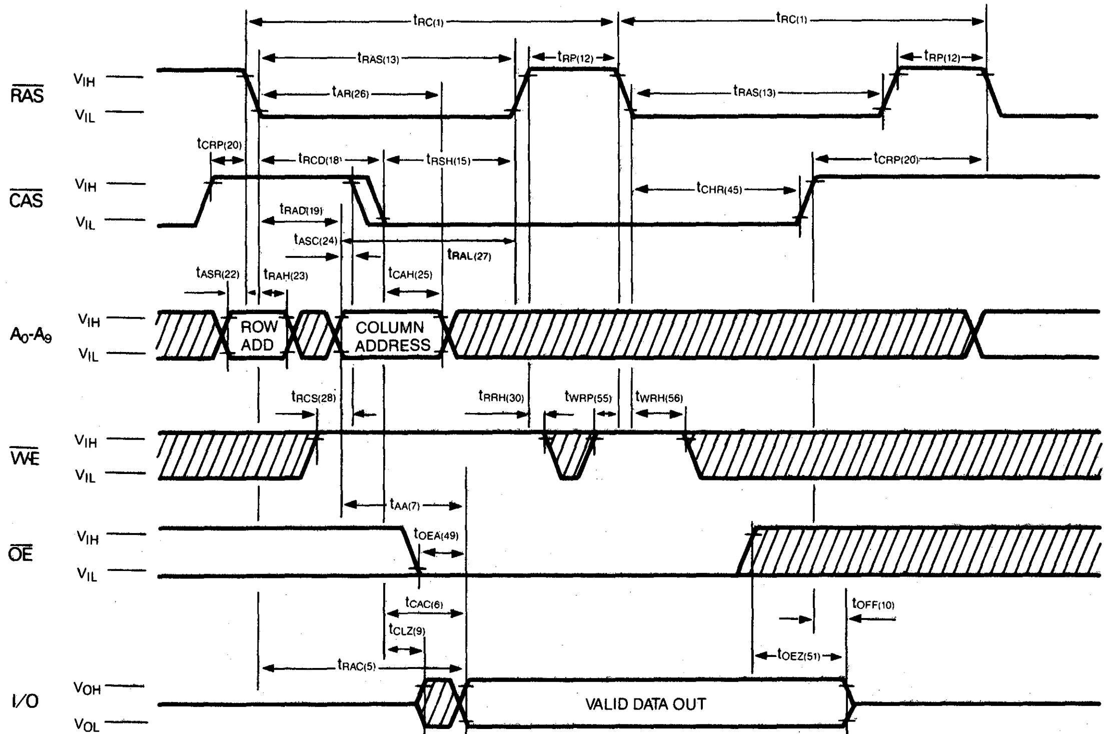
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

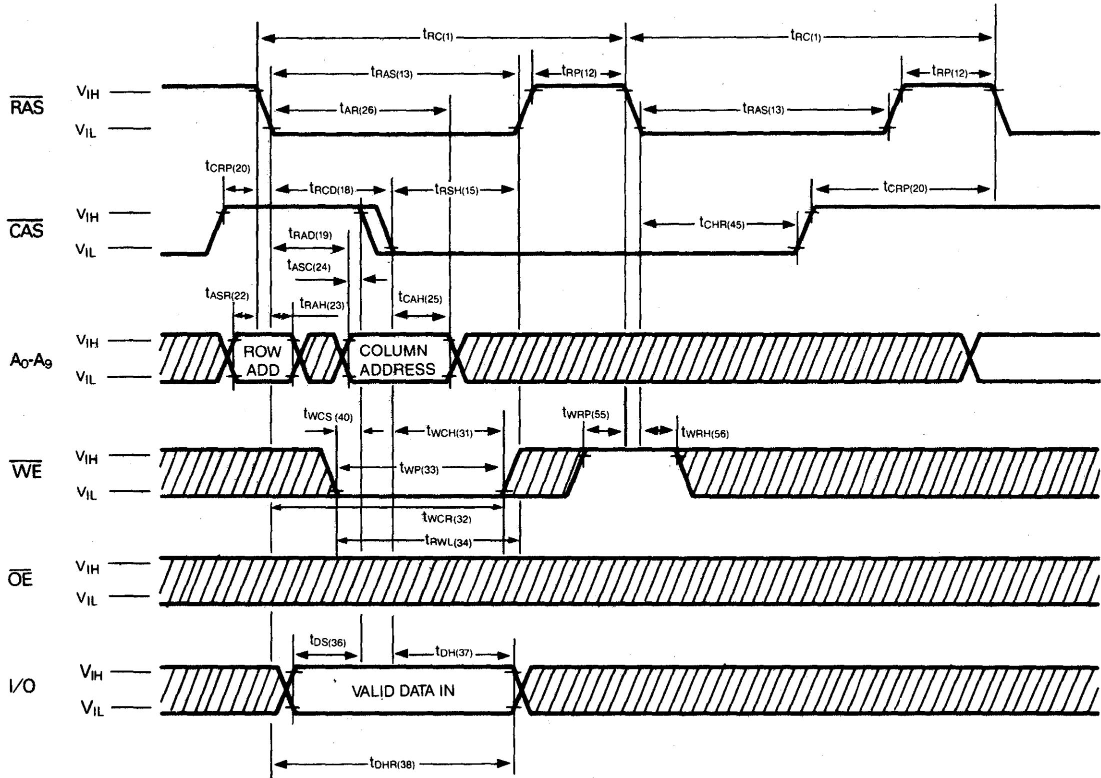


NOTE : $\overline{OE}$ and A_0-A_9 : "H" or "L"

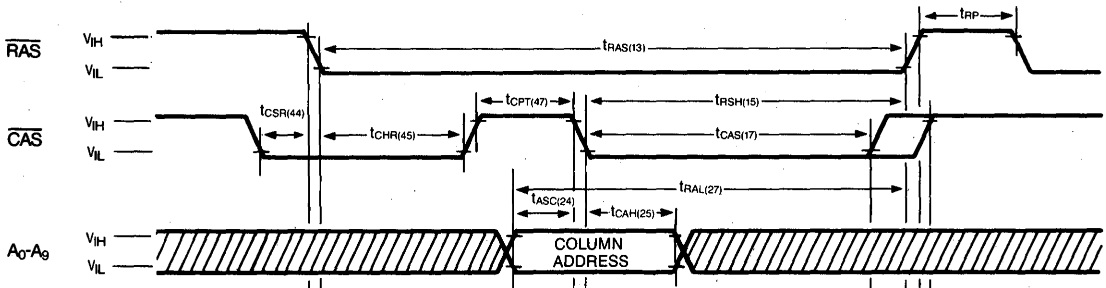
HIDDEN REFRESH CYCLE (READ)



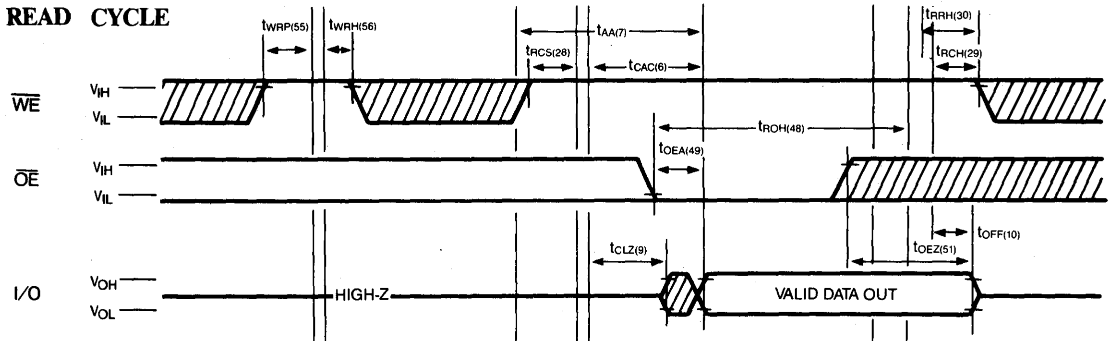
HIDDEN REFRESH CYCLE (WRITE)



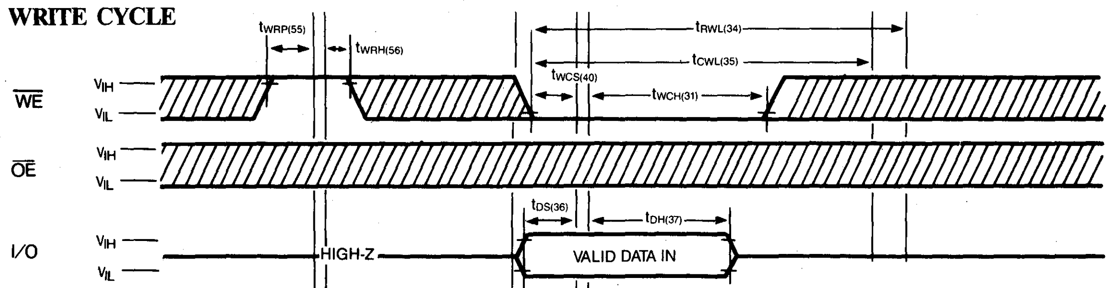
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



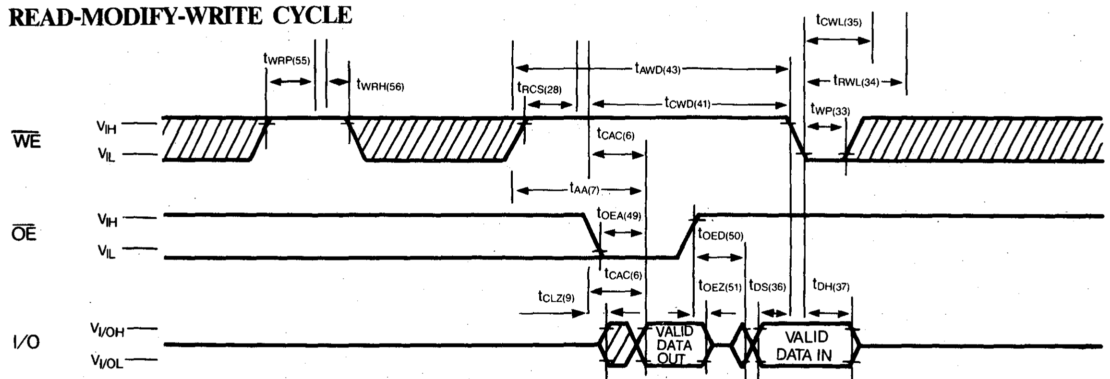
READ CYCLE



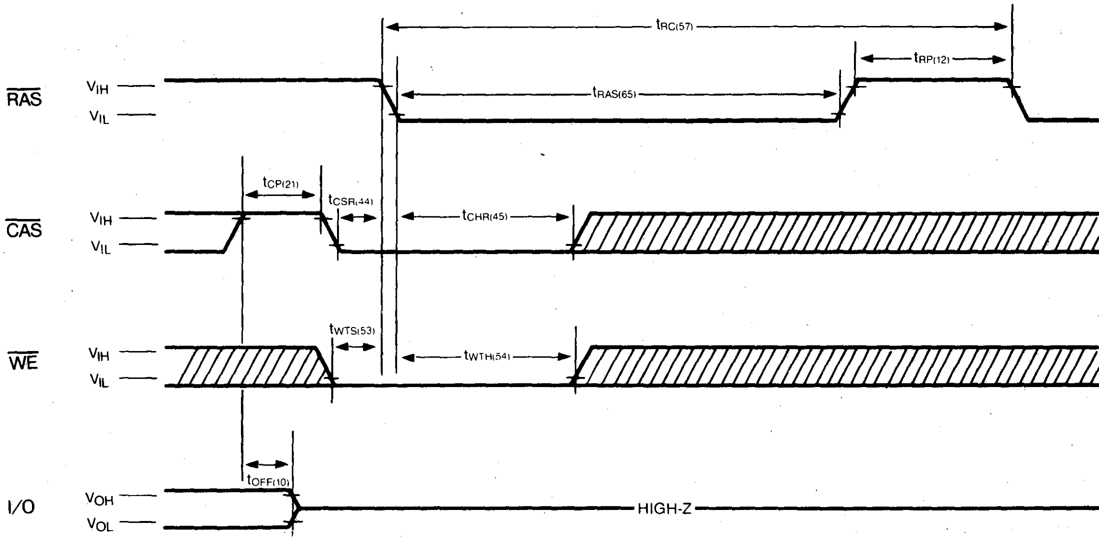
WRITE CYCLE



READ-MODIFY-WRITE CYCLE



TEST MODE IN CYCLE



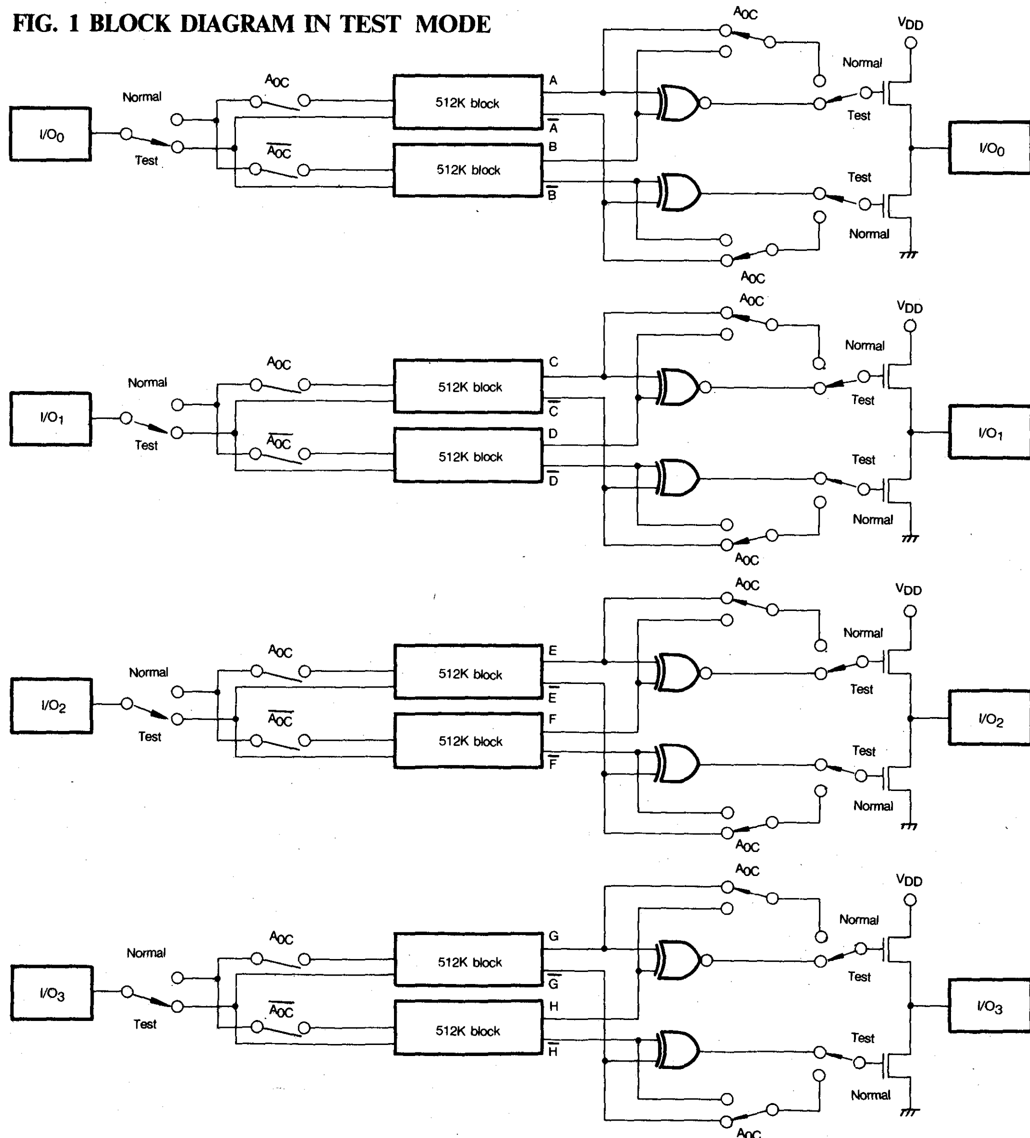
NOTE : $\overline{OE}$ and A_0-A_9 : "H" or "L"

TEST MODE

The HY514400 is a DRAM organized 1,048, 576 words by 4 bits and it is internally organized 524,288 words by 8 bits. In Test Mode, data are written into 8 sectors in parallel and retrieved the same way. A_{0C} is not used. If, upon reading, two bits on one I/O are equal(all 1s or 0s), the I/O pin indicates 1. If they were not equal, the I/O pin indicates 0. The following figure shows the block diagram of HY514400. In Test Mode, 1M×4 DRAM can be tested as if it were a 512K×4 DRAM.

$\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle puts the device into Test Mode. And $\overline{CAS}$-Before-RAS Refresh Cycle or RAS-Only-Refresh Cycle puts it back into Normal Mode. In Test Mode, $\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle performs the refresh operation with the internal refresh address couter. The Test Mode function reduces test time to one-second in case of N test pattern.

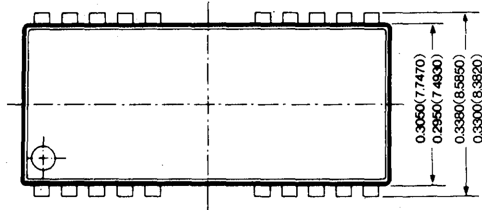
FIG. 1 BLOCK DIAGRAM IN TEST MODE

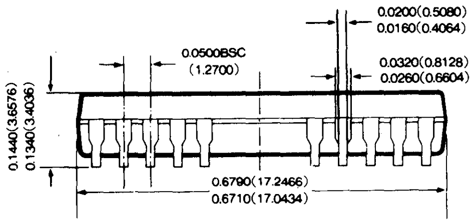


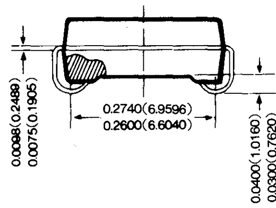
PACKAGE INFORMATION

- 20/26 PIN SMALL OUTLINE J-FORM PACKAGE-300 MIL

UNIT : INCH(mm) MAX/MIN







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MEMO

•HYUNDAI SEMICONDUCTOR

HY514400A

1M×4-Bit CMOS DRAM

M1I1200A-MAR92

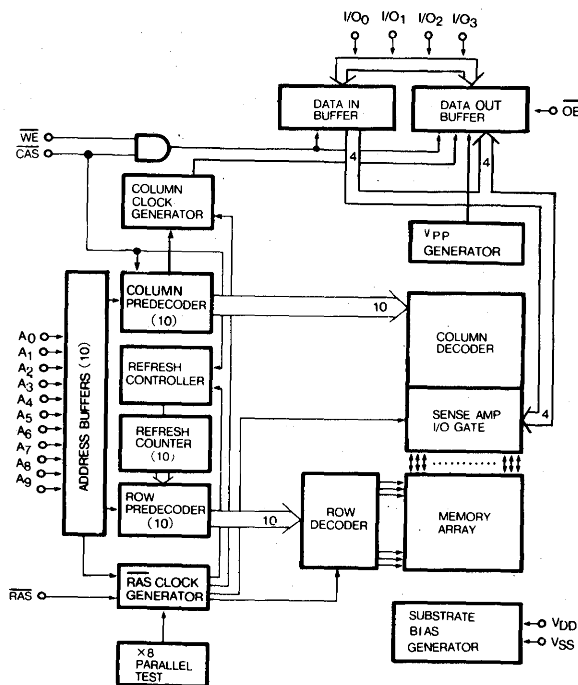
DESCRIPTION

The HY514400A is a high speed and new generation 1,048,576 words by 4 bits CMOS dynamic random access memory, fabricated with the HYUNDAI CMOS process. The HY514400A offers a fast page mode operation, wide operating margins, and inherently high CMOS reliability.

All inputs and outputs are TTL compatible. Multiplexed address inputs permit the HY514400A to be packaged in a standard 20/26 pin SOJ, TSOP, and 20 pin ZIP.

HY514400A design is optimized for cache based mainframe, and microcomputers, graphics digital signal processing, and high performance microprocessor systems.

BLOCK DIAGRAM

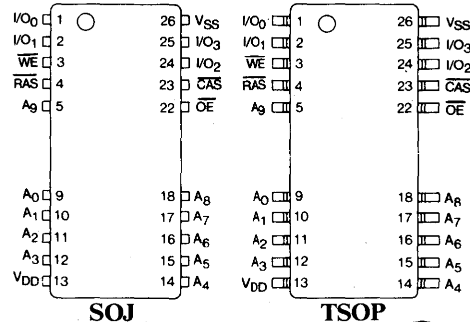


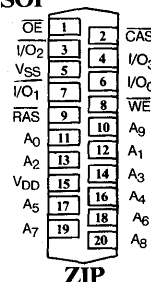
FEATURES

- Low power dissipation
  - Operating Current, 80ns : 90mA(max.)
  - TTL Standby Current : 2mA(max.)
  - CMOS Standby Current : 1mA(max.)
- Read-Modify-Write Capability
- $\overline{RAS}$-only, Hidden, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Capability
- Common I/O Capability
- Fast Page mode and Test mode Capability
- Single 5V± 10% power supply
- 1024 refresh cycles/16 ms
- High reliability 300 mil 20/26 pin SOJ, TSOP and 400mil 20 pin ZIP
- Fast access time and cycle time(ns)

	HY514400A-60	HY514400A-70	HY514400A-80
Max $\overline{RAS}$ Access Time, t_{RAC}	60	70	80
Max $\overline{CAS}$ Access Time, t_{CAC}	20	20	25
Min Fast Page Mode Cycle Time, t_{PC}	40	45	55
Min Cycle Time, t_{RC}	120	130	150

PIN CONNECTIONS





PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
A_0-A_9	ADDRESS INPUT
I/O_0-I/O_3	DATA INPUT/OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
T_{SOLDER}	Soldering Temperature, Time	260, 10	℃, sec
P_T	Power Dissipation	770	mW

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS
(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY514400A		UNIT	NOTE
				MIN.	MAX.		
$\mid I_{LI}\mid$	Input Leakage Current(any input pin)	0V≤V_{IN}≤6.5V, All other pin not under test=V_{SS}		−	10	μA	
$\mid I_{LO}\mid$	Output Leakage Current for High Impedance State	D_{OUT} is disable, 0V≤V_{OUT}≤5.5V		−	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$\overline{RAS}$, $\overline{CAS}$, Address cycling, t_{RC}=t_{RC}(min.)	−60	−	110	mA	1, 2, 4
			−70	−	100		
			−80	−	90		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$=$\overline{CAS}$=V_{IH}		−	2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}, t_{RC}=t_{RC}(min.)	−60	−	110	mA	1, 4
			−70	−	100		
			−80	−	90		
I_{DD4}	V_{DD} Supply Current, Fast page mode	$\overline{RAS}$=V_{IL}, Address cycling, t_{PC}=t_{PC}(min.)	−60	−	70	mA	1, 2, 4
			−70	−	60		
			−80	−	50		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}$=$\overline{CAS}$=V_{DD}−0.2V		−	1	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{RC}(min.)	−60	−	110	mA	1, 4
			−70		100		
			−80	−	90		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		−	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	−	V	

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 3, 4, 5

#	SYMBOL	PARAMETER	HY514400A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
2	t_{RWC}	Read-Modify-Write Cycle Time	175	–	185	–	210	–	ns	
3	t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	55	–	ns	
4	t_{PRWC}	Fast Page Mode RMW Cycle Time	95	–	100	–	115	–	ns	
5	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	7, 12
6	t_{CAC}	Access Time From $\overline{CAS}$	–	20	–	20	–	25	ns	7, 12
7	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	7, 12
8	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	7
9	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	ns	7
10	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	8
11	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	6
12	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	50	–	60	–	ns	
13	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	200K	70	200K	80	200K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
17	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
18	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	55	ns	12
19	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	13
20	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
21	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
22	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
23	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
24	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
25	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
26	t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
27	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
28	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
29	t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	9
30	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	9
31	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
32	t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
33	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
34	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
35	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
36	t_{DS}	Data Set-up Time	0	–	0	–	0	–	ns	10
37	t_{DH}	Data Hold Time	15	–	15	–	15	–	ns	10
38	t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
39	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
40	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	11
41	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	–	50	–	55	–	ns	11
42	t_{RWD}	RAS to $\overline{WE}$ Delay Time	90	–	100	–	110	–	ns	11
43	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60	–	65	–	70	–	ns	11

#	SYMBOL	PARAMETER	HY514400A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
44	t_{CSR}	CAS Set-up Time(CAS Before RAS Cycle)	10	–	10	–	10	–	ns	
45	t_{CHR}	CAS Hold Time(CAS Before RAS Cycle)	15	–	20	–	30	–	ns	
46	t_{RPC}	RAS to CAS Precharge Time	0	–	0	–	0	–	ns	
47	t_{CPT}	CAS Precharge Time(CBR Counter Test Cycle)	30	–	35	–	40	–	ns	
48	t_{ROH}	RAS Hold Time referenced to OE	10	–	10	–	10	–	ns	
49	t_{OEA}	OE Access Time	–	20	–	20	–	20	ns	
50	t_{OED}	OE to Data Delay	20	–	20	–	20	–	ns	
51	t_{OEZ}	Output Buffer Turn-off Delay Time from OE	0	20	0	20	0	20	ns	
52	t_{OEH}	OE Command Hold Time	20	–	20	–	20	–	ns	
53	t_{WTS}	Write Command Set-up Time(Test Mode In)	10	–	10	–	10	–	ns	
54	t_{WTH}	Write Command Hold Time(Test Mode In)	10	–	10	–	10	–	ns	
55	t_{WRP}	WE to RAS Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
56	t_{WRH}	WE to RAS Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

AC CHARACTERISTICS IN THE TEST MODE Note : 14

#	SYMBOL	PARAMETER	HY514400A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
57	t_{RC}	Random Read or Write Cycle Time	125	–	135	–	155	–	ns	
58	t_{RWC}	Read-Modify-Write Cycle Time	180	–	190	–	215	–	ns	
59	t_{PC}	Fast Page Mode Cycle Time	45	–	50	–	60	–	ns	
60	t_{PRWC}	Fast Page Mode RMW Cycle Time	100	–	105	–	120	–	ns	
61	t_{RAC}	Access Time from RAS	–	65	–	75	–	85	ns	7, 12
62	t_{CAC}	Access Time from CAS	–	25	–	25	–	30	ns	7, 12
63	t_{AA}	Access Time from Column Address	–	35	–	40	–	45	ns	7, 12
64	t_{CPA}	Access Time from CAS Precharge	–	40	–	45	–	55	ns	7
65	t_{RAS}	RAS Pulse Width	65	10K	75	10K	85	10K	ns	
66	t_{RASP}	RAS Pulse Width(Fast Page Mode)	65	200K	75	200K	85	200K	ns	
67	t_{RSH}	RAS Hold Time	25	–	25	–	30	–	ns	
68	t_{CSH}	CAS Hold Time	65	–	75	–	85	–	ns	
69	t_{CAS}	CAS Pulse Width	25	10K	25	10K	30	10K	ns	
70	t_{RAL}	Column Address to RAS Lead Time	35	–	40	–	45	–	ns	
71	t_{CWD}	CAS to WE Delay Time	55	–	55	–	60	–	ns	11
72	t_{RWD}	RAS to WE Delay Time	95	–	105	–	115	–	ns	11
73	t_{AWD}	Column Address to WE Delay Time	65	–	70	–	75	–	ns	11
74	t_{OEA}	OE Access Time	–	25	–	25	–	25	ns	
75	t_{OED}	OE to Data Delay	25	–	25	–	25	–	ns	
76	t_{OEH}	OE Command Hold Time	25	–	25	–	25	–	ns	

NOTES :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6}, I_{CC7} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. It depends on user whether column address is changed or not at least once while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
5. AC measurements assume t_T=5ns.
6. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Measured with a load equivalent to 2 TTL loads and 100pF.
8. t_{OFF}(max.) and t_{OEZ} define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle : If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.) the cycle is a read-modify-write cycle and data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
12. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
13. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
14. These specifications are applied to the test mode.

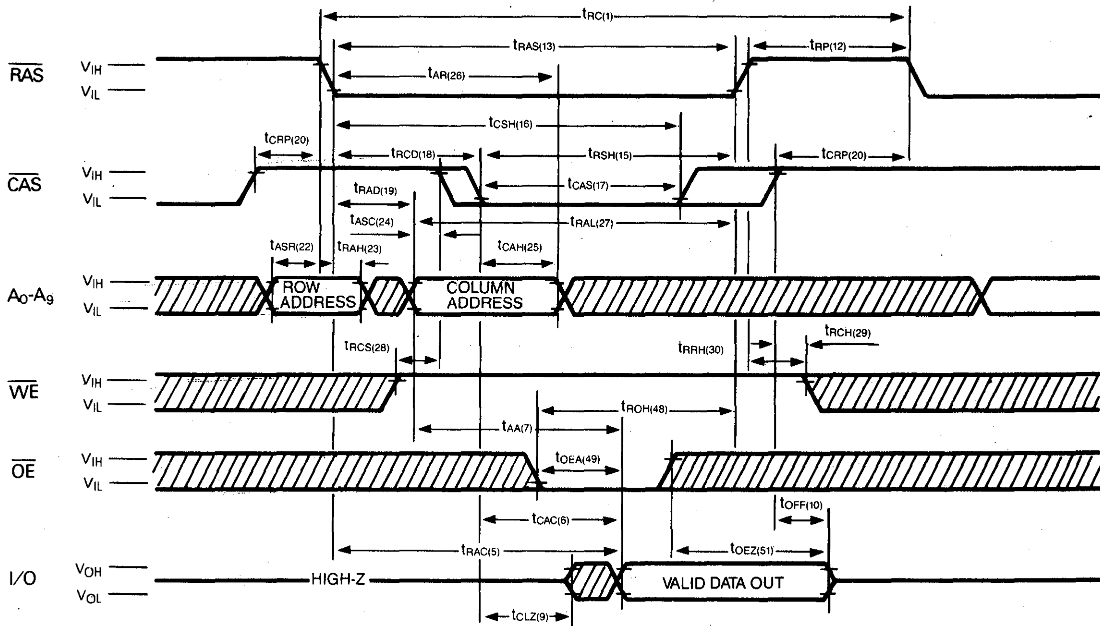
CAPACITANCE

(T_A=0°C to 70°C, V_{DD}=5V± 10%, f=1MHz)

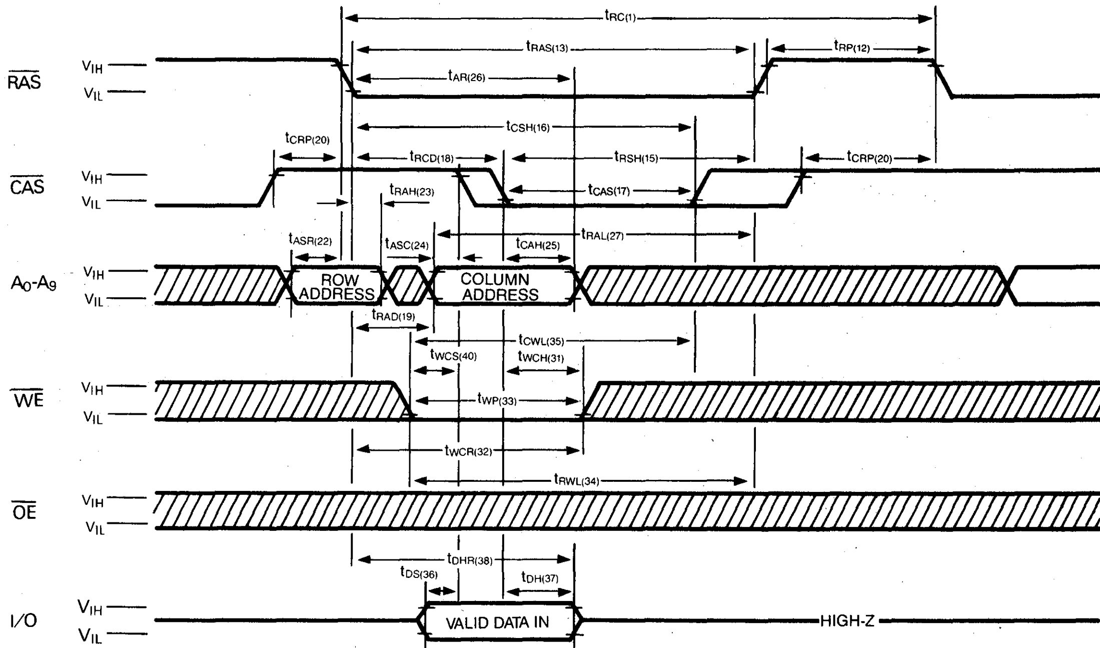
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_9, Data In)	–	5	pF
C_{IN2}	Input Capacitance($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	–	7	pF
C_{OUT}	Output Capacitance(Data Out)	–	7	pF

TIMING DIAGRAM

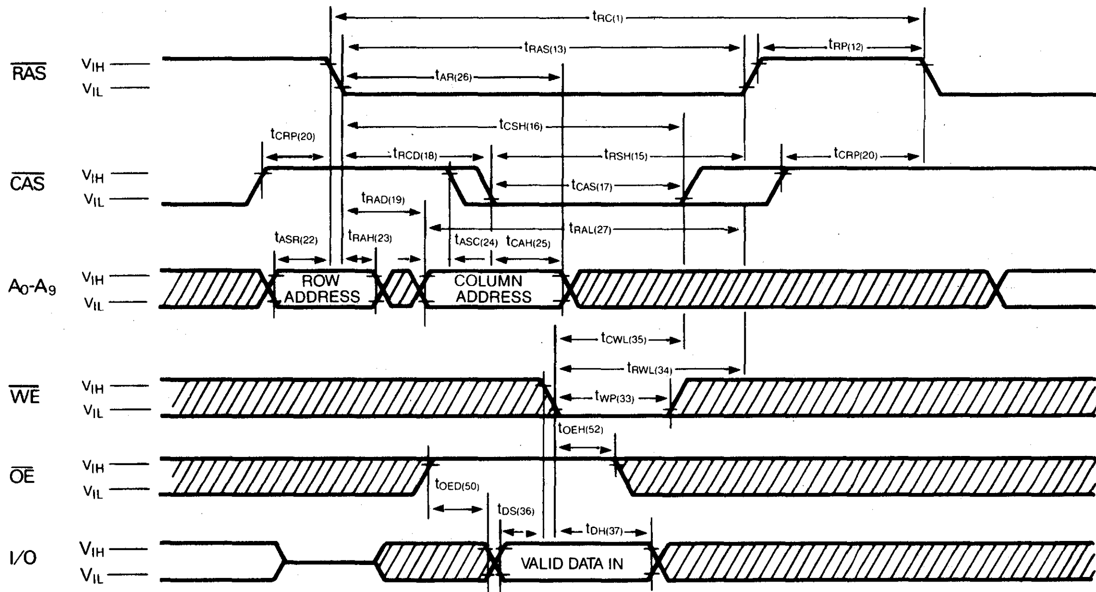
READ CYCLE



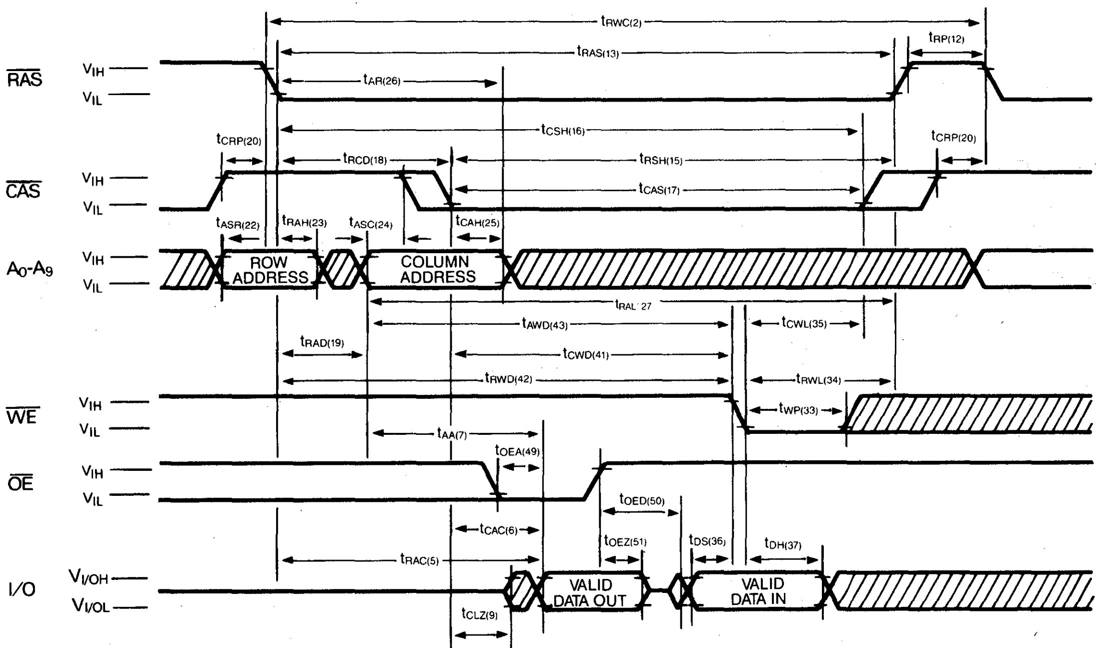
WRITE CYCLE



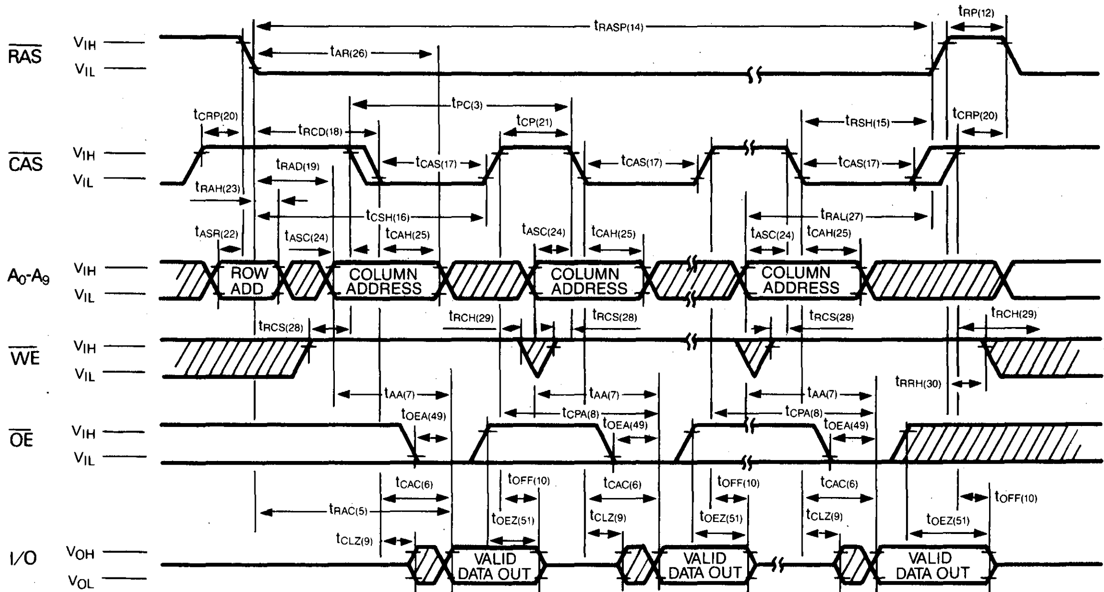
WRITE CYCLE(OE CONTROLLED WRITE)



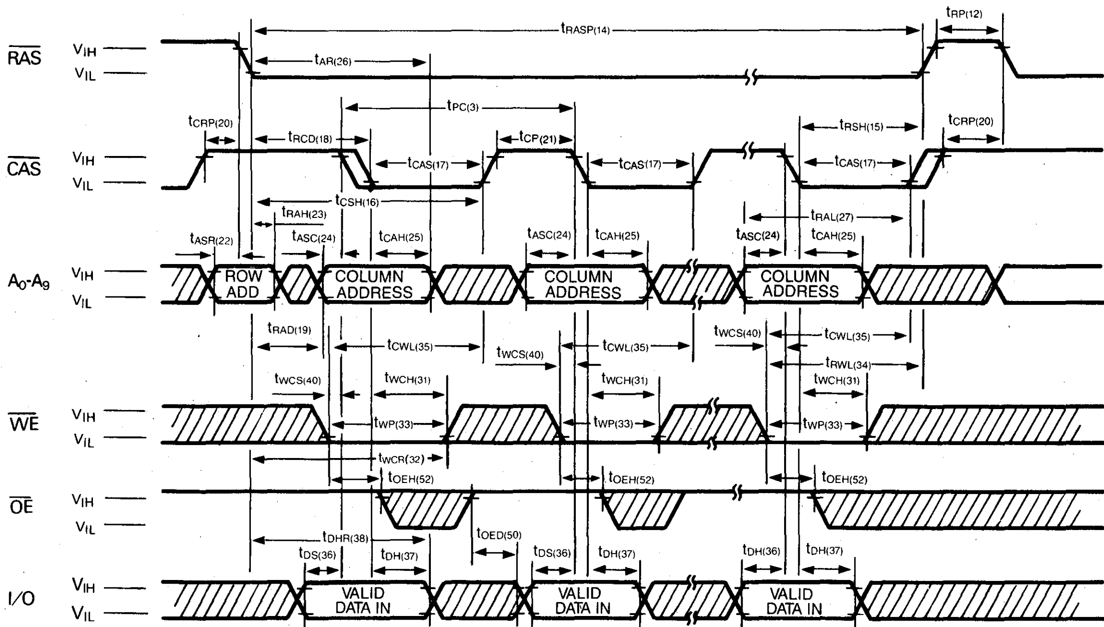
READ-MODIFY-WRITE CYCLE



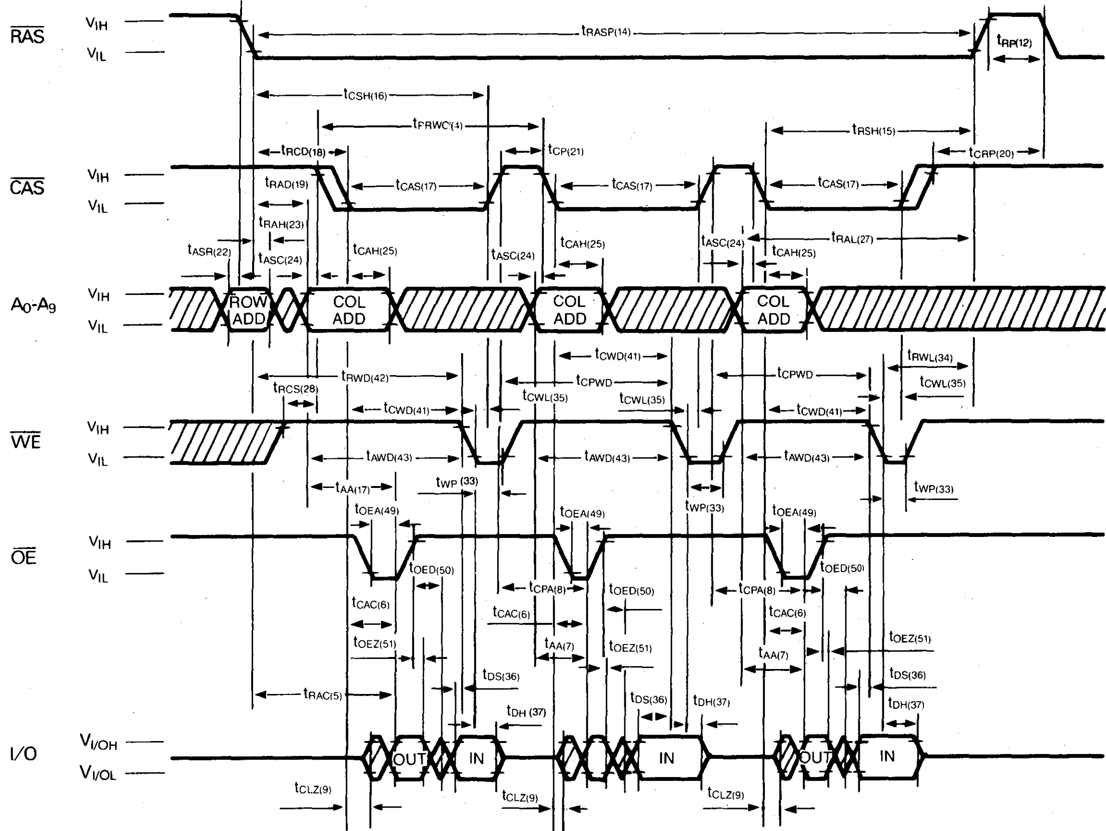
FAST PAGE MODE READ CYCLE



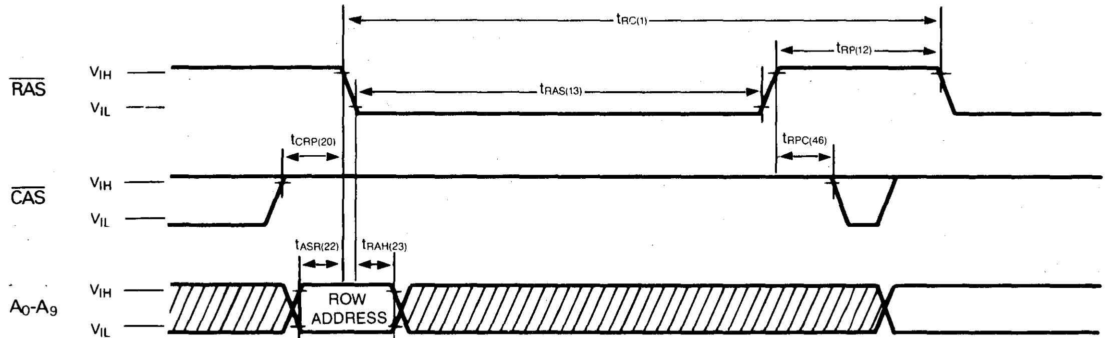
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

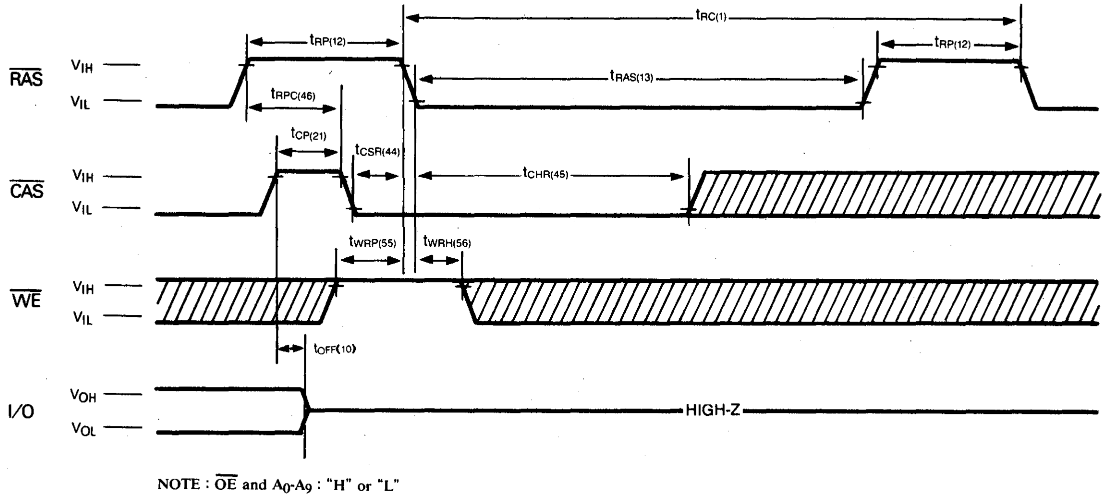


$\overline{RAS}$-ONLY REFRESH CYCLE



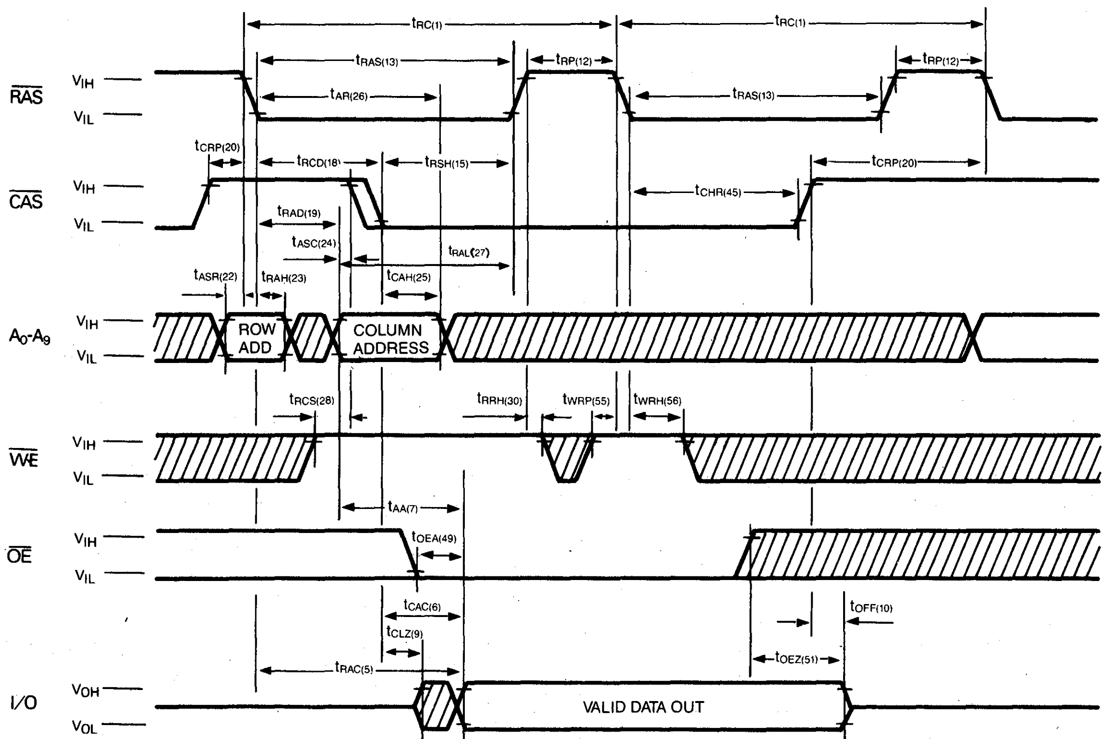
NOTE : $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

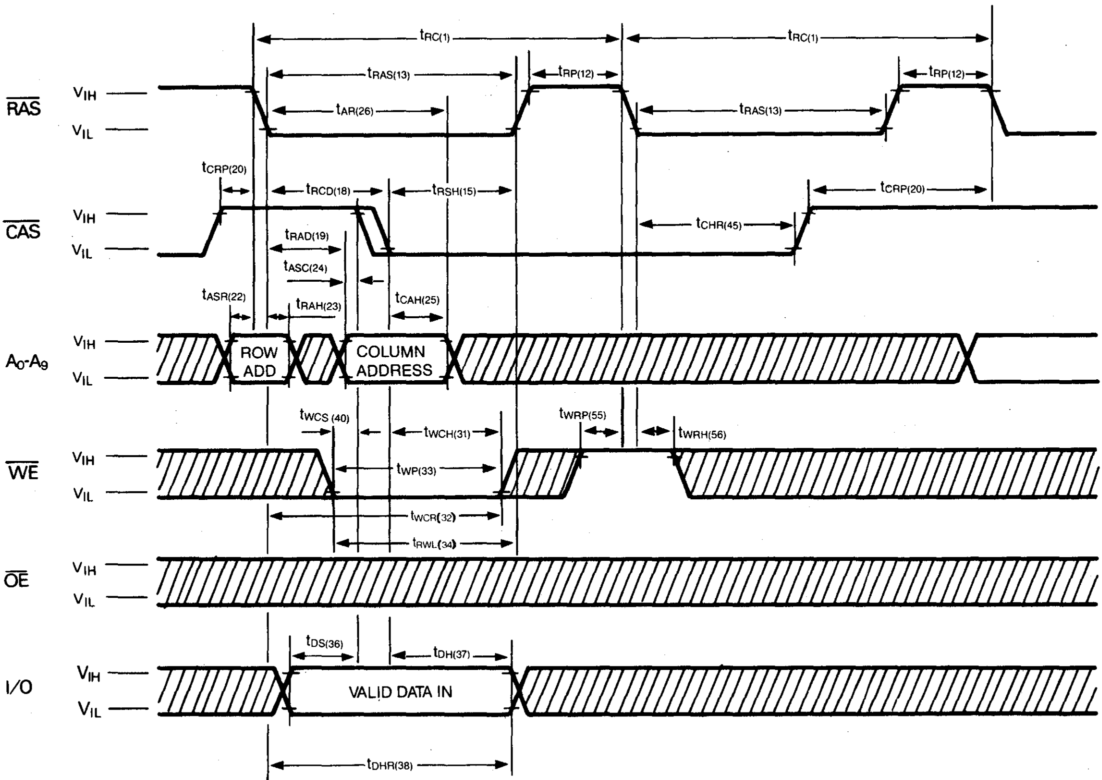


NOTE : $\overline{OE}$ and A_0-A_9 : "H" or "L"

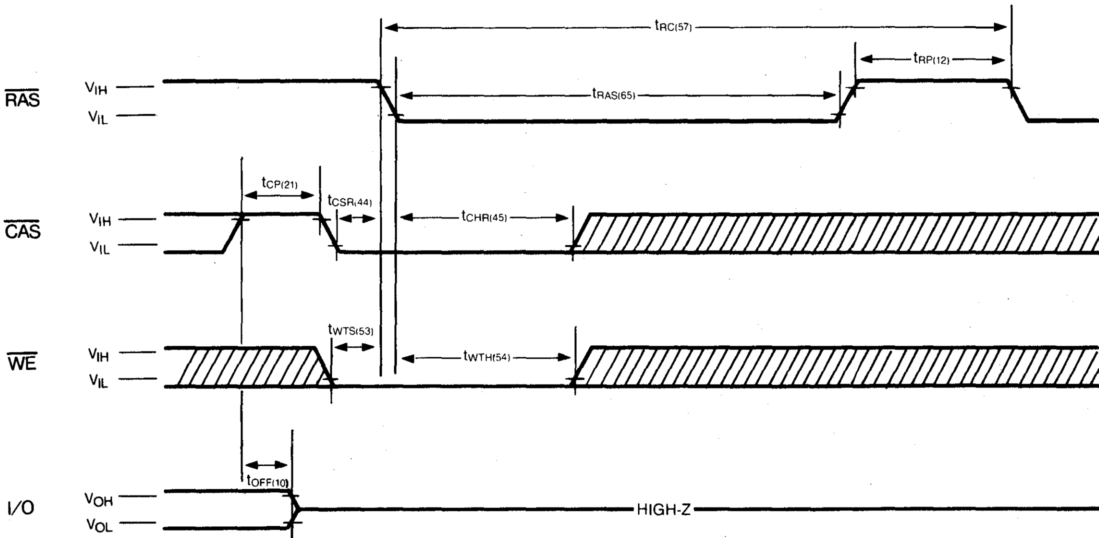
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

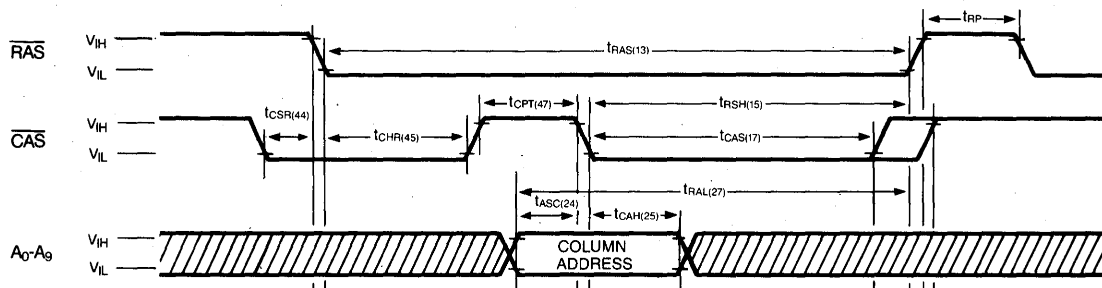


TEST MODE IN CYCLE

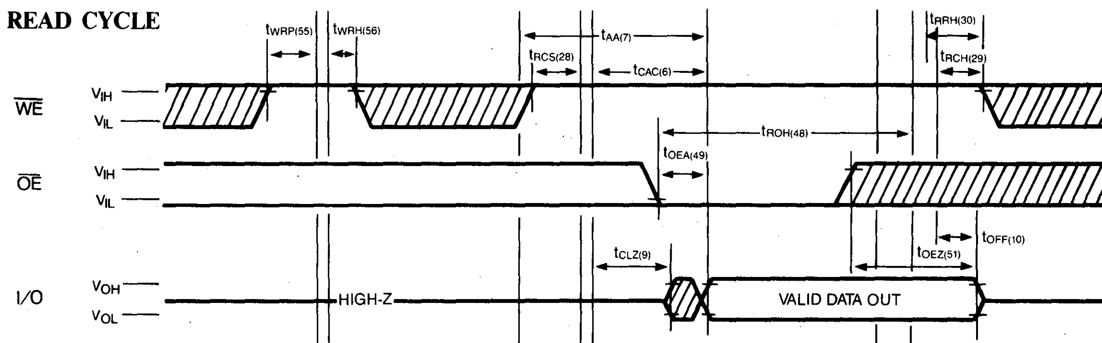


NOTE : $\overline{OE}$ and A_0-A_9 : "H" or "L"

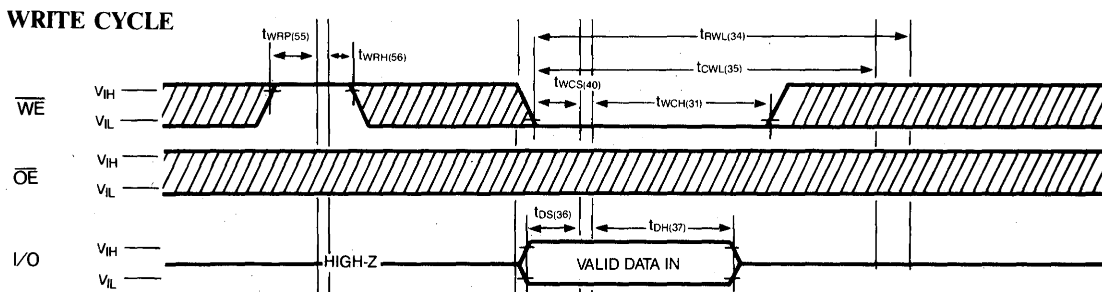
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



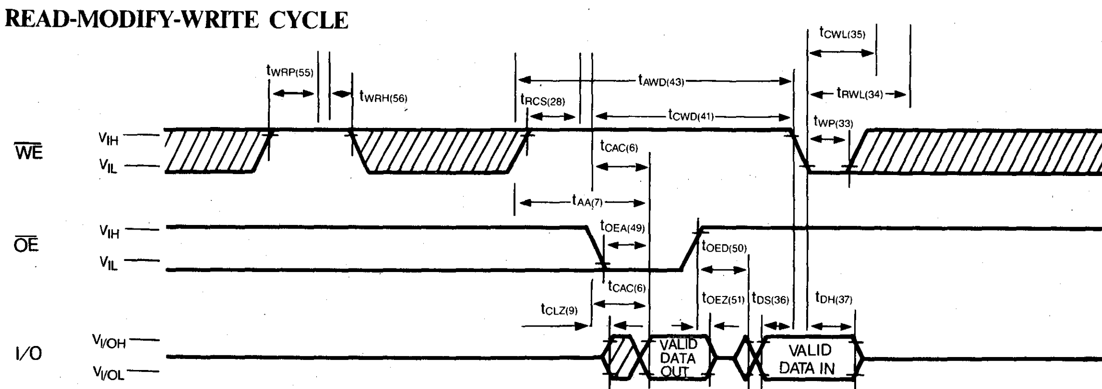
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE

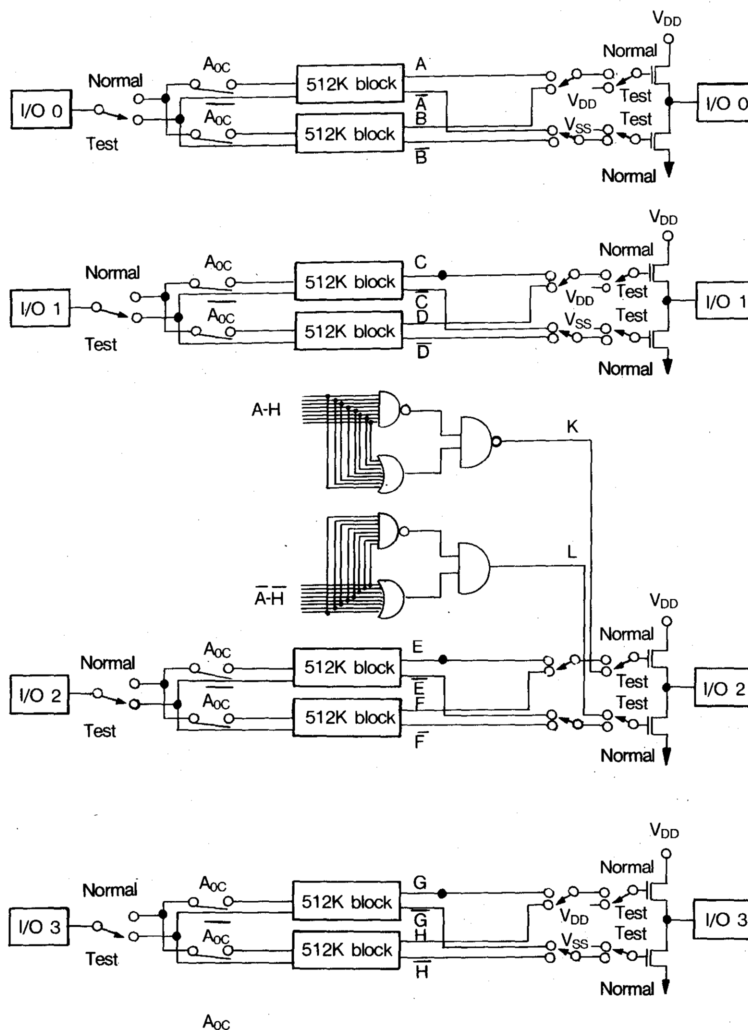


TEST MODE

The HY514400A is a DRAM organized 1,048,576 words by 4 bits and it is internally organized 524,288 words by 8 bits. In Test Mode, data are written into 8 sectors in parallel and retrieved the same way. A_{0C} is not used. If, upon reading, the 8 bits are equal(all 1s or 0s), the I/O pin indicates 1. If they were not equal, the I/O pin indicates 0. The following figure shows the block diagram of HY514400A. In Test Mode, 1M×4 DRAM cab be tested as if it were a 512K×8 DRAM.

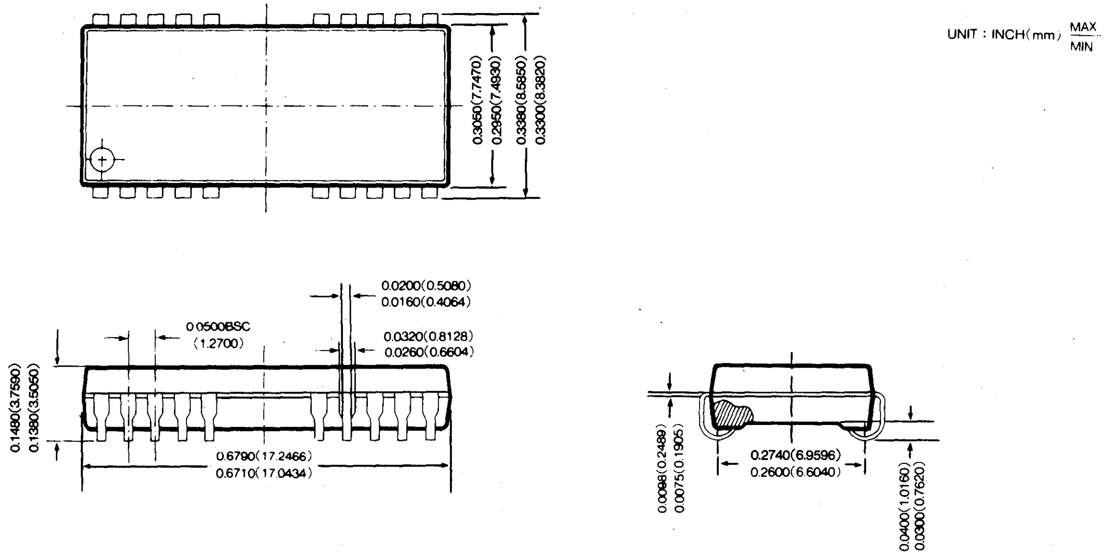
$\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle puts the device into Test Mode. And $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle or $\overline{RAS}$-Only Refresh Cycle puts it back into Normal Mode. In Test Mode, $\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle performs the refresh operation with the internal refresh address couter. The Test Mode function reduces test time to one-second in case of N test pattern.

BLOCK DIAGRAM IN TEST MODE

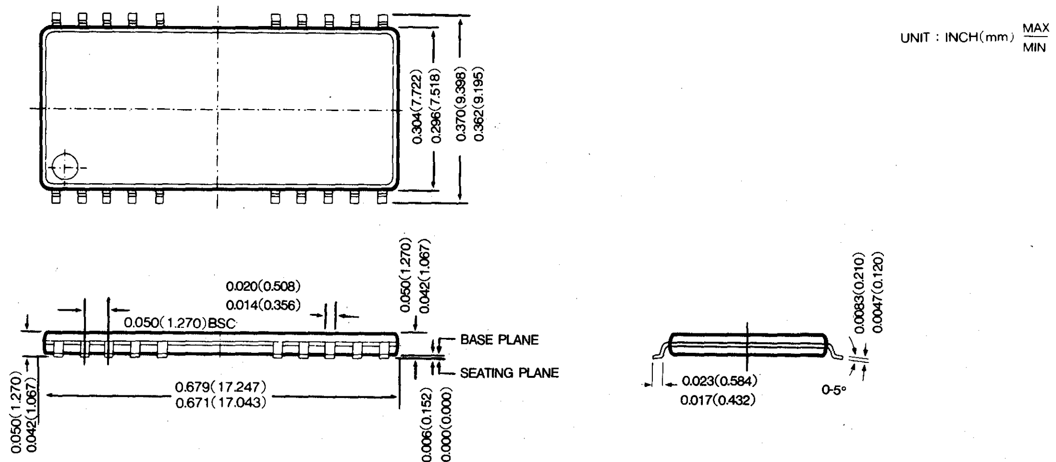


PACKAGE INFORMATION

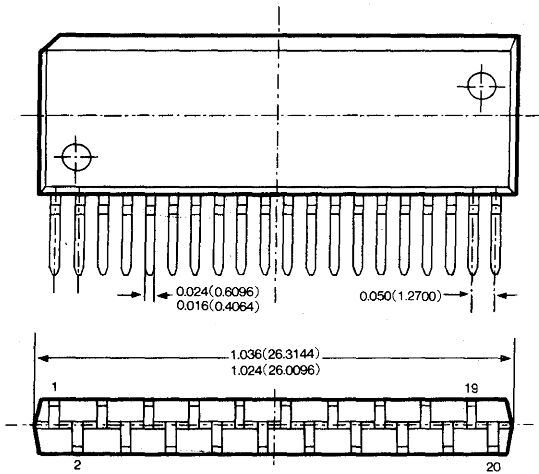
- **20/26 PIN SMALL OUTLINE J-FORM PACKAGE −300 MIL**

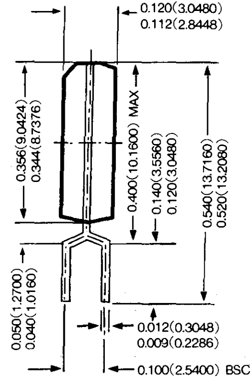


- **20/26 PIN THIN SMALL OUTLINE PACKAGE−300 MIL**



- **20 PIN ZIGZAG-IN-LINE PACKAGE－400MIL**





MEMO

•HYUNDAI SEMICONDUCTOR

HY514400AL

1M×4-Bit CMOS DRAM

M1J1200A-MAR92

DESCRIPTION

The HY514400AL is a high speed, low power 1,048,576 words by 4 bits CMOS dynamic random access memory, fabricated with the HYUNDAI CMOS process. The HY514400AL offers a fast page mode operation, wide operating margins, and inherently high CMOS reliability.

All inputs and outputs are TTL compatible. Multiplexed address inputs permit the HY514400AL to be packaged in a standard 20/26 pin SOJ, TSOP, and 20 pin ZIP.

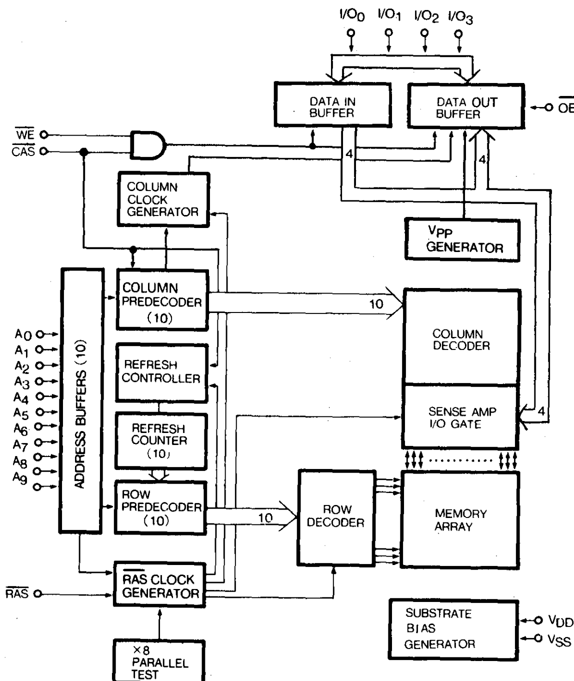
HY514400AL design is optimized for cache based mainframe, and microcomputers, graphics digital signal processing, and high performance microprocessor systems.

FEATURES

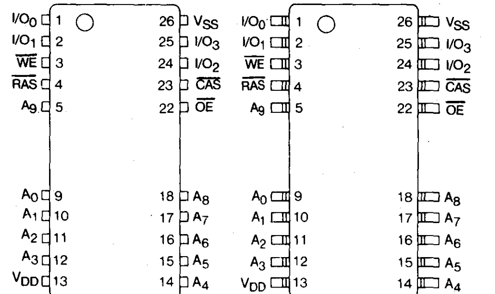
- **Low power dissipation**
  - **Operating Current, 80ns : 90mA(max.)**
  - **TTL Standby Current : 2mA(max.)**
  - **CMOS Standby Current : 200μA(max.)**
  - **Battery Back Up Current : 300μA(max.)**
- **Read-Modify-Write Capability**
- **RAS-only, Hidden, CAS-Before-RAS Refresh Capability**
- **Common I/O Capability**
- **Fast Page mode and Test mode Capability**
- **Single 5V± 10% power supply**
- **1024 refresh cycles/128 ms**
- **High reliability 300 mil 20/26 pin SOJ, TSOP and 400mil 20 pin ZIP**
- **Fast access time and cycle time(ns)**

	HY514400AL-60	HY514400AL-70	HY514400AL-80
Max RAS Access Time, t_{RAC}	60	70	80
Max CAS Access Time, t_{CAC}	20	20	25
Min Fast Page Mode Cycle Time, t_{PC}	40	45	55
Min Cycle Time, t_{RC}	120	130	150

BLOCK DIAGRAM

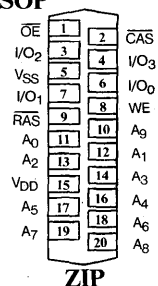


PIN CONNECTIONS



PIN NAMES

RAS	ROW ADDRESS STROBE
CAS	COLUMN ADDRESS STROBE
WE	WRITE ENABLE
OE	OUTPUT ENABLE
A_0-A_9	ADDRESS INPUT
I/O_0-I/O_3	DATA INPUT/OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
T_{SOLDER}	Soldering Temperature Time	260, 10	℃, sec
P_T	Power Dissipation	770	mW

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY514400AL		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	OV≤V_{IN}≤6.5V, All other pin not under test=V_{SS}		−	10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	D_{OUT} is disable, OV≤V_{OUT}≤5.5V		−	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$\overline{RAS}$, $\overline{CAS}$, Address cycling, t_{RC}=t_{RC}(min.)	−60	−	110	mA	1, 2, 4
			−70	−	100		
			−80	−	90		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$=$\overline{CAS}$=V_{IH}		−	2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}, t_{RC}=t_{RC}(min.)	−60	−	110	mA	1, 4
			−70	−	100		
			−80	−	90		
I_{DD4}	V_{DD} Supply Current, Fast page mode	$\overline{RAS}$=V_{IL}, Address cycling, t_{PC}=t_{PC}(min.)	−60	−	70	mA	1, 2, 4
			−70	−	60		
			−80	−	50		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}$=$\overline{CAS}$=V_{DD}−0.2V		−	200	μA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{RC}(min.)	−60	−	110	mA	1, 4
			−70		100		
			−80	−	90		
I_{DD7}	V_{DD} Supply Current, Battery Back up	$\overline{CAS}$=CBR cycling or 0.2V, $\overline{OE}$=$\overline{WE}$=V_{DD}−0.2V, Add=V_{DD}−0.2V or 0.2V, I/O=V_{DD}−0.2V or 0.2V or open, t_{RC}=125μs, t_{RAS}=t_{RAS}(min.) ~300ns		−	300	μA	1
		Same as above except t_{RAS}=300ns~1μs		−	400	μA	1, 5
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		−	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	−	V	

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 3, 4, 5, 6

#	SYMBOL	PARAMETER	HY514400AL						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
2	t_{RWC}	Read-Modify-Write Cycle Time	175	–	185	–	210	–	ns	
3	t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	55	–	ns	
4	t_{PRWC}	Fast Page Mode RMW Cycle Time	95	–	100	–	115	–	ns	
5	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	8, 13
6	t_{CAC}	Access Time From $\overline{CAS}$	–	20	–	20	–	25	ns	8, 13
7	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	8, 13
8	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	8
9	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	ns	8
10	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	9
11	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	7
12	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	50	–	60	–	ns	
13	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	200K	70	200K	80	200K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
17	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
18	t_{RCD}	$\overline{RAS}$ to CAS Delay Time	20	40	20	55	20	55	ns	13
19	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	14
20	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
21	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
22	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
23	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
24	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
25	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
26	t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
27	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
28	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
29	t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	10
30	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	10
31	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
32	t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
33	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
34	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
35	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
36	t_{DS}	Data Set-up Time	0	–	0	–	0	–	ns	11
37	t_{DH}	Data Hold Time	15	–	15	–	15	–	ns	11
38	t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
39	t_{REF}	Refresh Period	–	128	–	128	–	128	ms	
40	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	12
41	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	–	50	–	55	–	ns	12
42	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	90	–	100	–	110	–	ns	12
43	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60	–	65	–	70	–	ns	12

#	SYMBOL	PARAMETER	HY514400AL						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
44	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
45	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	30	–	ns	
46	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
47	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	30	–	35	–	40	–	ns	
48	t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	10	–	ns	
49	t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	20	ns	
50	t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	20	–	ns	
51	t_{OEZ}	Output Buffer Turn-off Delay Time from $\overline{OE}$	0	20	0	20	0	20	ns	
52	t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	20	–	ns	
53	t_{WTS}	Write Command Set-up Time(Test Mode In)	10	–	10	–	10	–	ns	
54	t_{WTH}	Write Command Hold Time(Test Mode In)	10	–	10	–	10	–	ns	
55	t_{WRP}	WE to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
56	t_{WRH}	WE to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

AC CHARACTERISTICS IN THE TEST MODE Note : 15

#	SYMBOL	PARAMETER	HY514400AL						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
57	t_{RC}	Random Read or Write Cycle Time	125	–	135	–	155	–	ns	
58	t_{RWC}	Read-Modify-Write Cycle Time	180	–	190	–	215	–	ns	
59	t_{PC}	Fast Page Mode Cycle Time	45	–	50	–	60	–	ns	
60	t_{PRWC}	Fast Page Mode RMW Cycle Time	100	–	105	–	120	–	ns	
61	t_{RAC}	Access Time from $\overline{RAS}$	–	65	–	75	–	85	ns	8, 13
62	t_{CAC}	Access Time from $\overline{CAS}$	–	25	–	25	–	30	ns	8, 13
63	t_{AA}	Access Time from Column Address	–	35	–	40	–	45	ns	8, 13
64	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	45	–	55	ns	8
65	t_{RAS}	$\overline{RAS}$ Pulse Width	65	10K	75	10K	85	10K	ns	
66	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	65	200K	75	200K	85	200K	ns	
67	t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
68	t_{CSH}	$\overline{CAS}$ Hold Time	65	–	75	–	85	–	ns	
69	t_{CAS}	$\overline{CAS}$ Pulse Width	25	10K	25	10K	30	10K	ns	
70	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	45	–	ns	
71	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	55	–	55	–	60	–	ns	12
72	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	95	–	105	–	115	–	ns	12
73	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	70	–	75	–	ns	12
74	t_{OEA}	$\overline{OE}$ Access Time	–	25	–	25	–	25	ns	
75	t_{OED}	$\overline{OE}$ to Data Delay	25	–	25	–	25	–	ns	
76	t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	25	–	25	–	ns	

NOTES :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6}, I_{CC7} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. It depends on user whether column address is changed or not at least once while RAS=V_{IL} and CAS=V_{IH}.
5. Only t_{RAS}(max.)=1μs is applied to refresh of battery back up but t_{RAS}(max.)=10μs is applied to normal functional operating.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) and t_{OEZ} define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle : If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.) the cycle is a read-modify-write cycle and data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
15. These specifications are applied to the test mode.

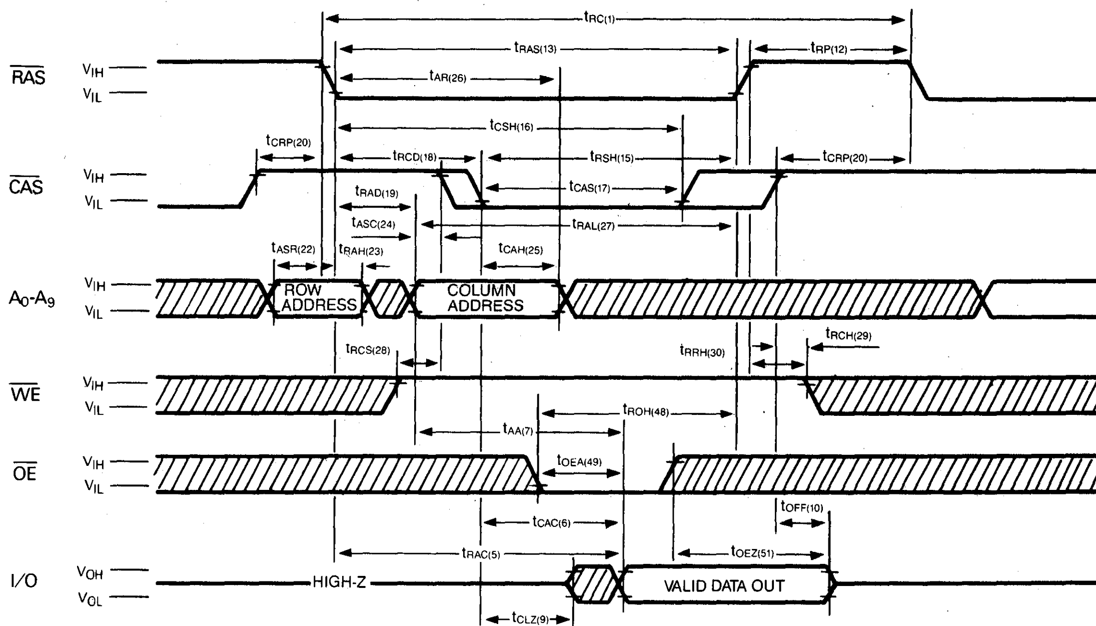
CAPACITANCE

(T_A=0°C to 70°C, V_{DD}=5V± 10%, f=1MHz)

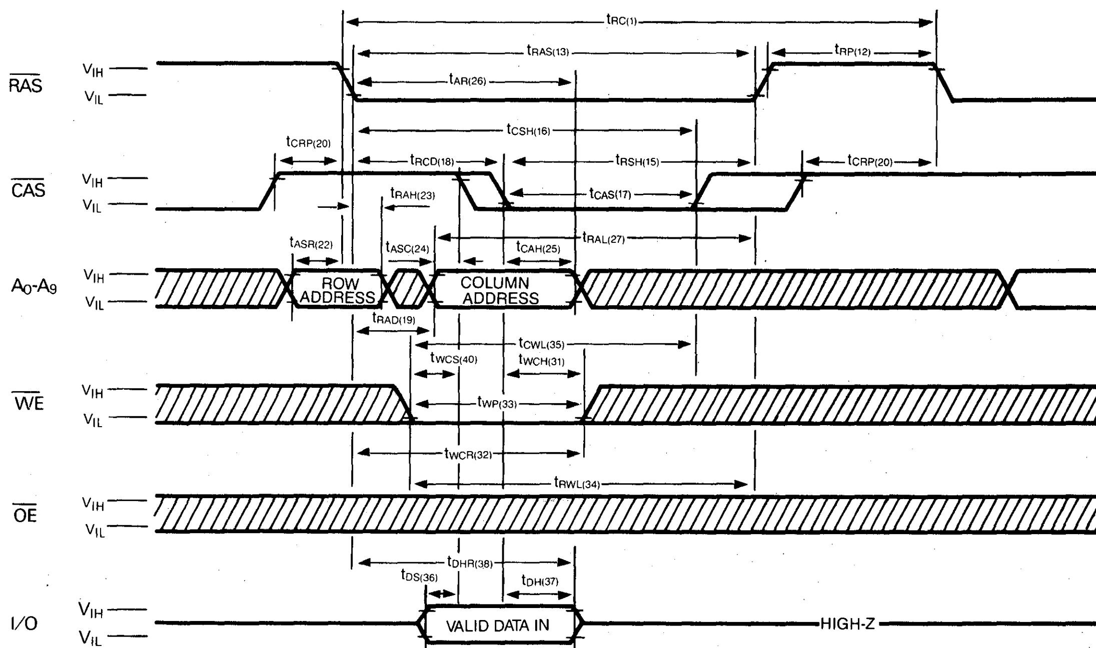
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_9, Data In)	–	5	pF
C_{IN2}	Input Capacitance($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	–	7	pF
C_{OUT}	Output Capacitance(Data Out)	–	7	pF

TIMING DIAGRAM

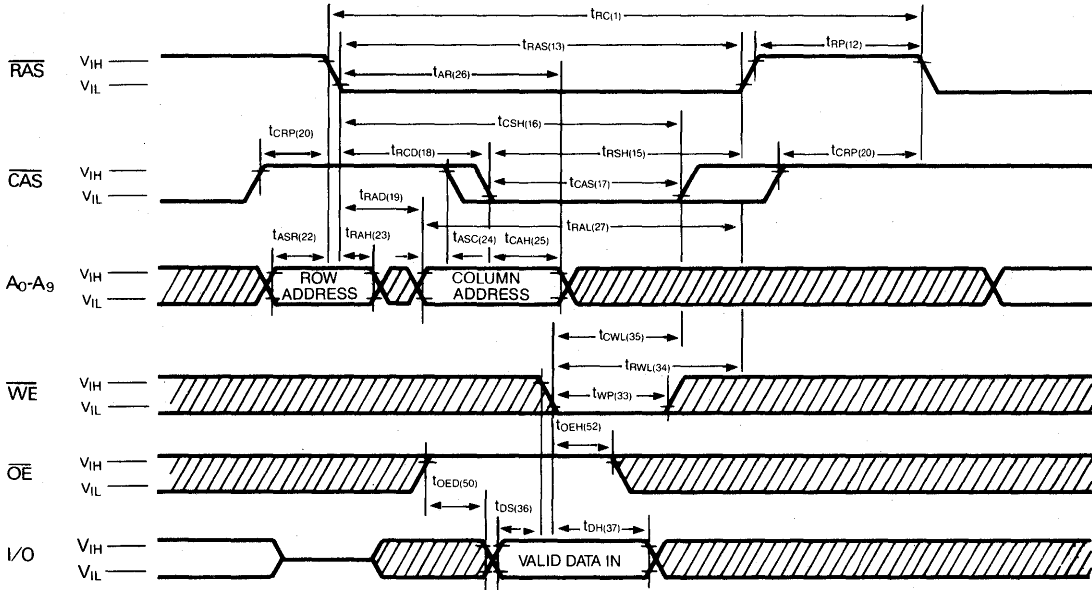
READ CYCLE



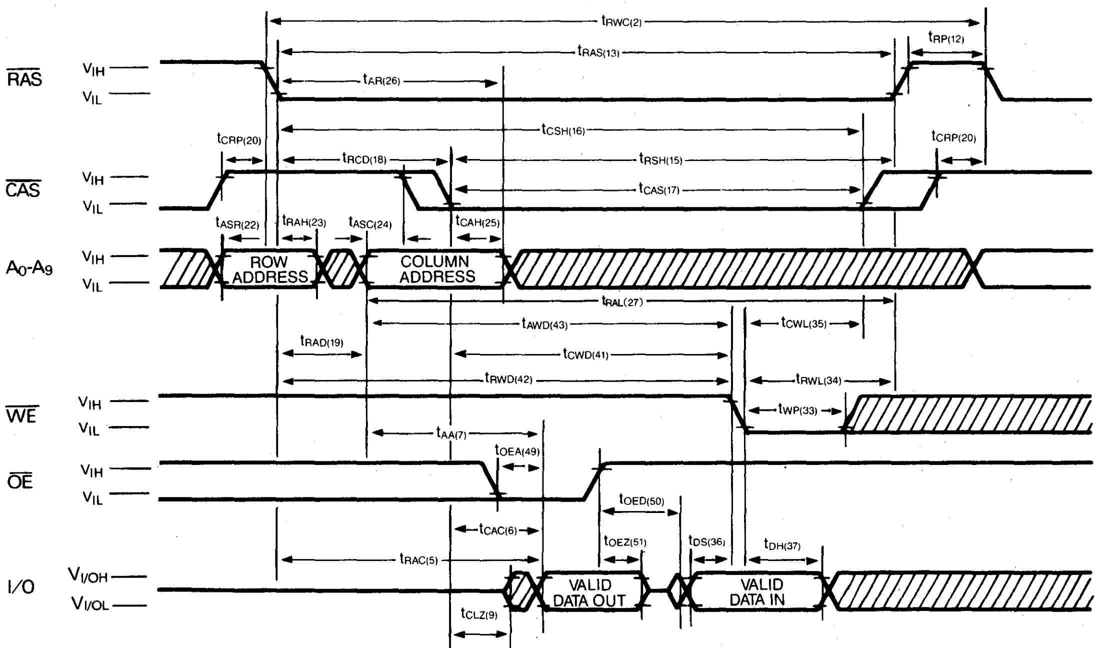
WRITE CYCLE



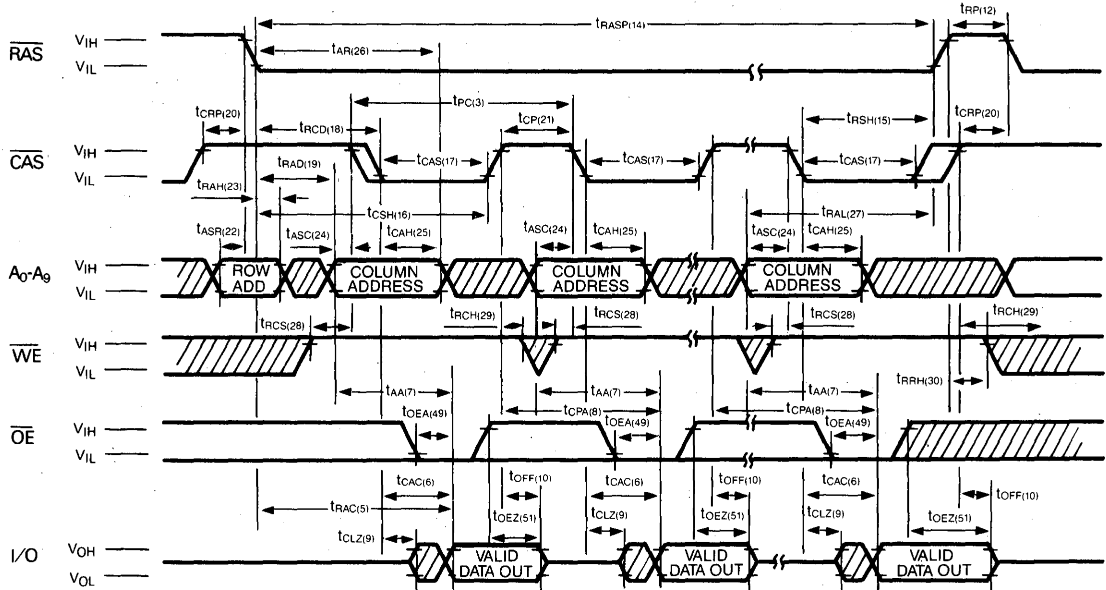
WRITE CYCLE($\overline{OE}$ CONTROLLED WRITE)



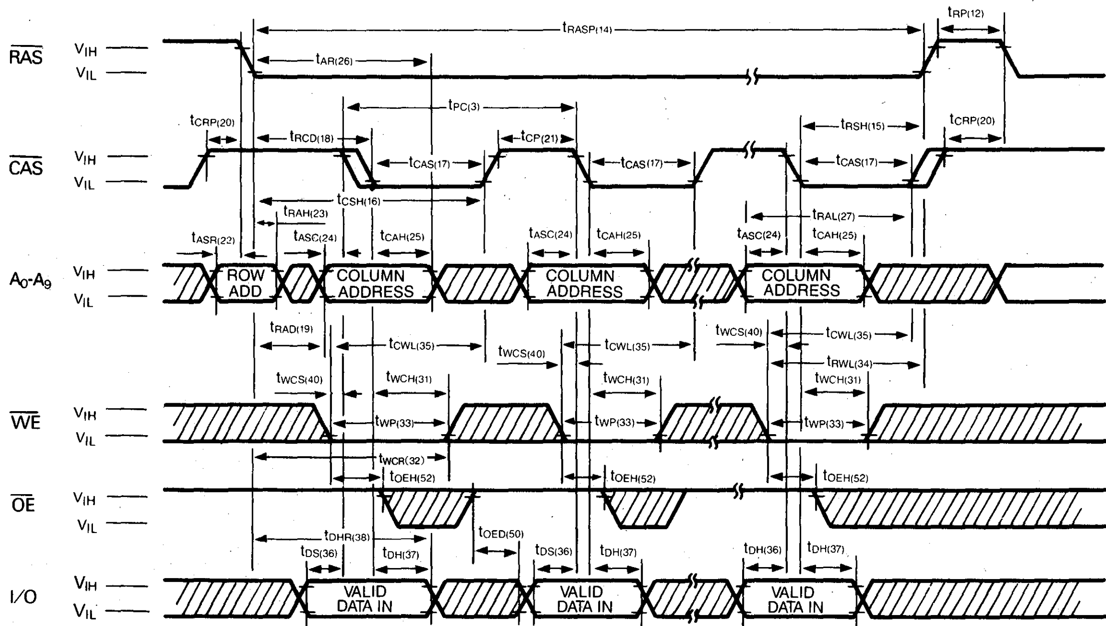
READ-MODIFY-WRITE CYCLE



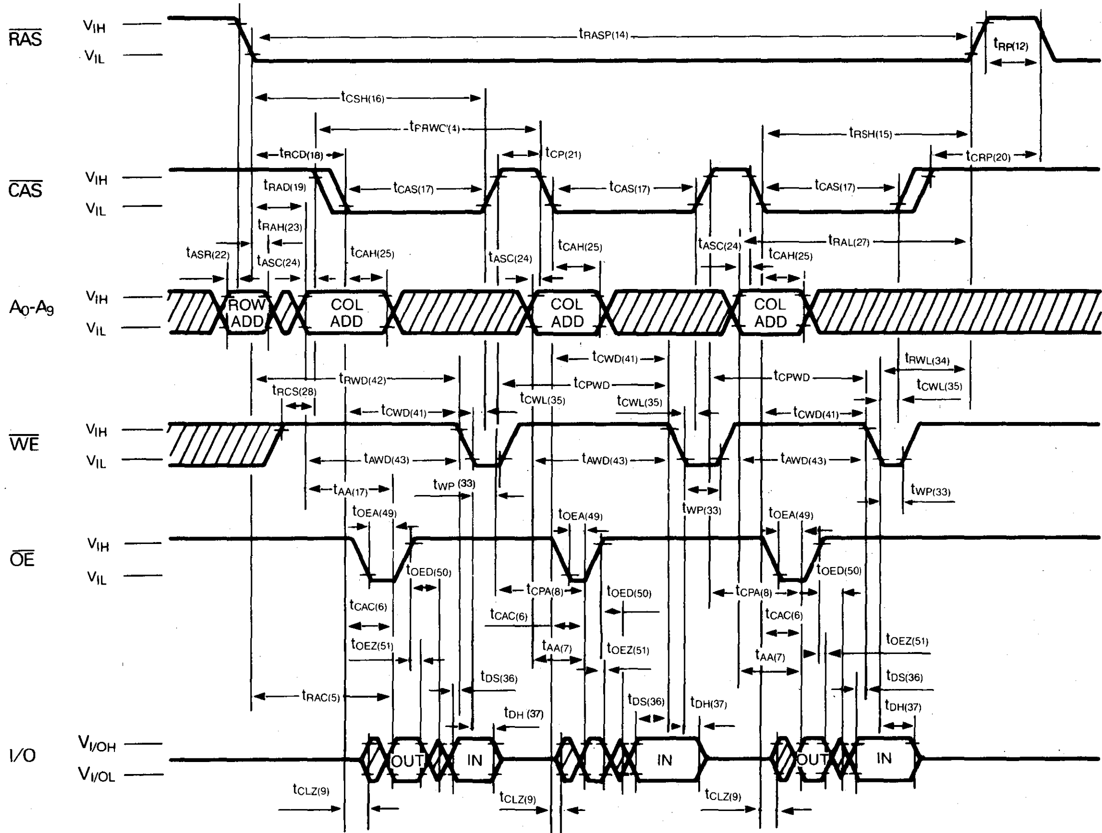
FAST PAGE MODE READ CYCLE



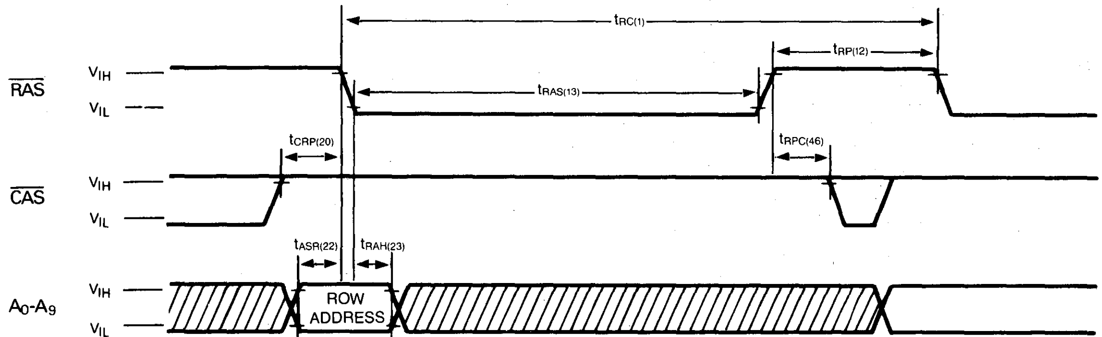
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

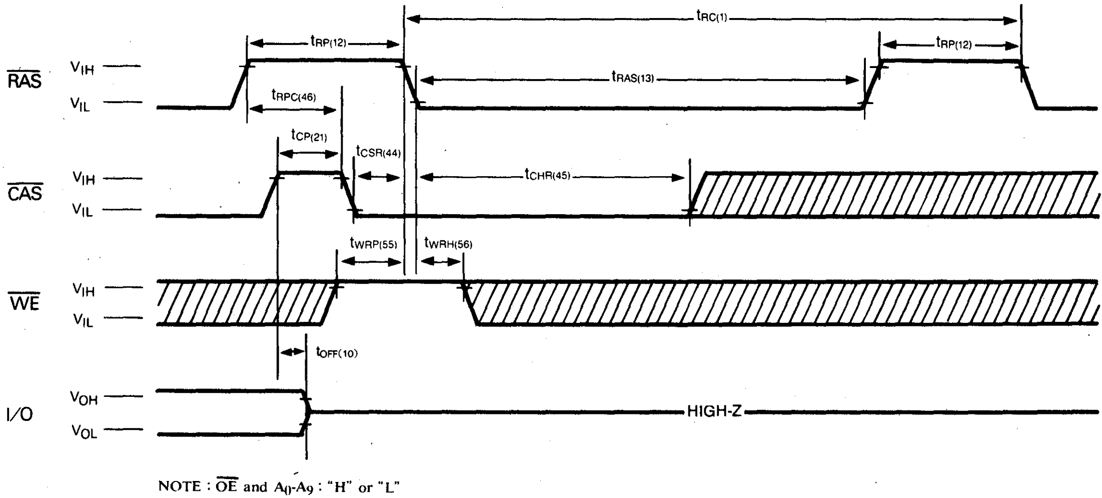


RAS-ONLY REFRESH CYCLE



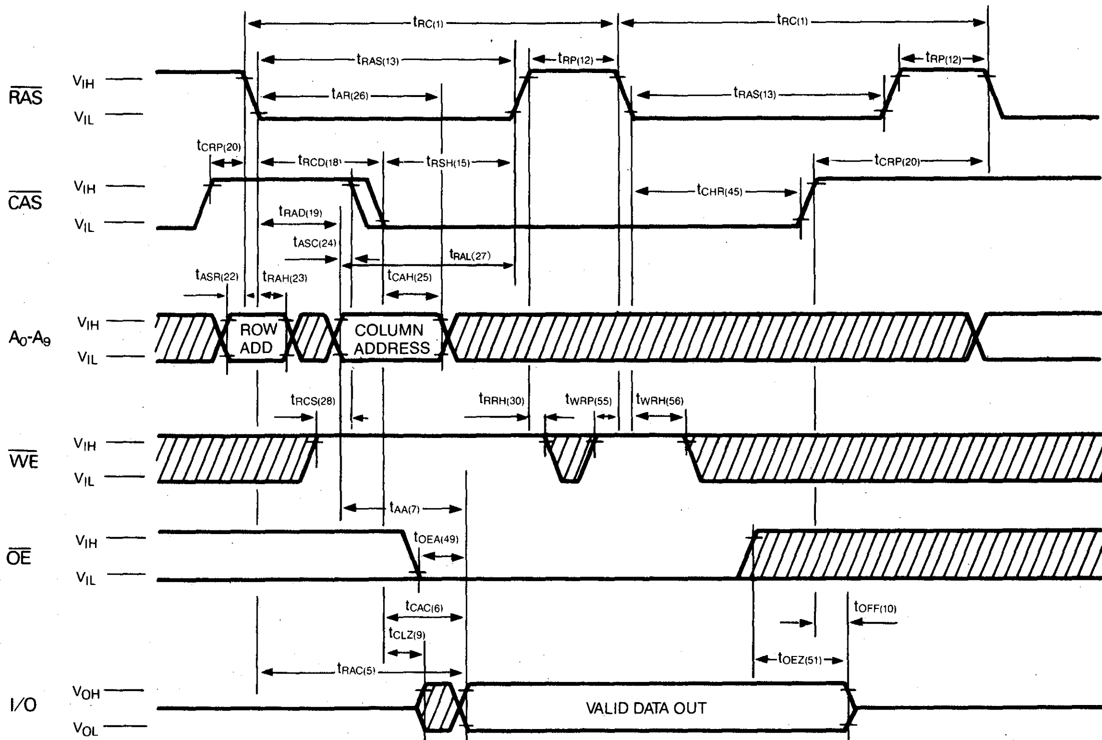
NOTE : $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

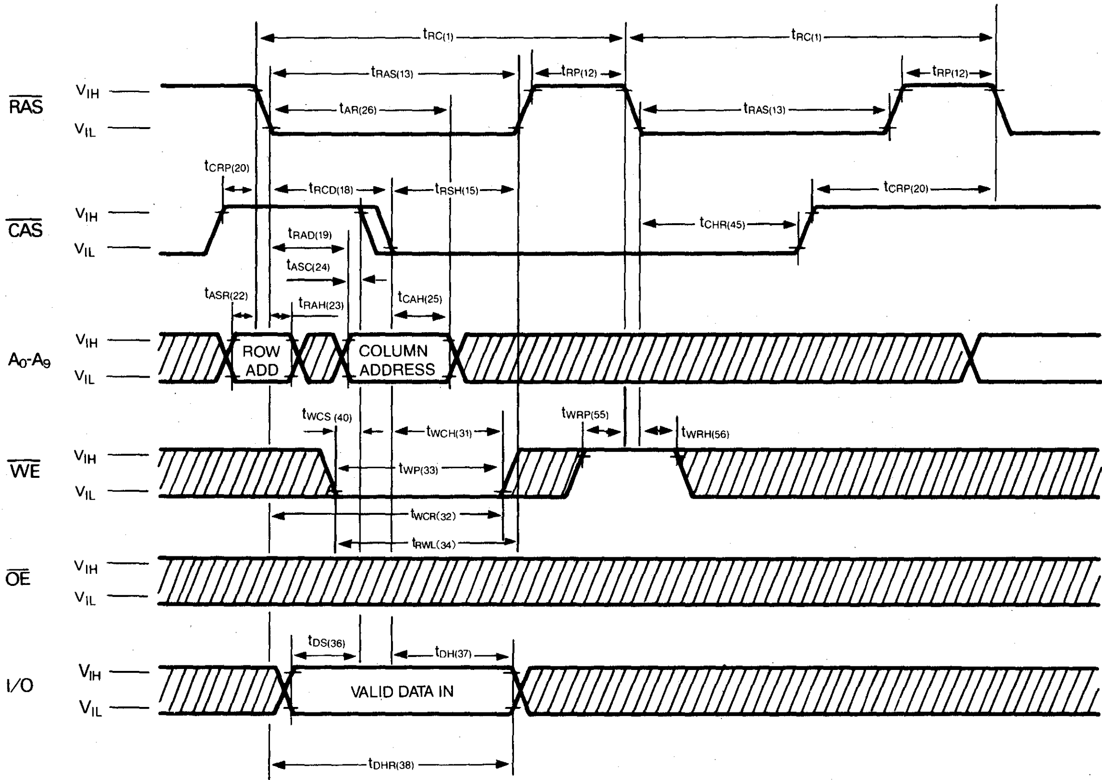


NOTE : $\overline{OE}$ and A_0-A_9 : "H" or "L"

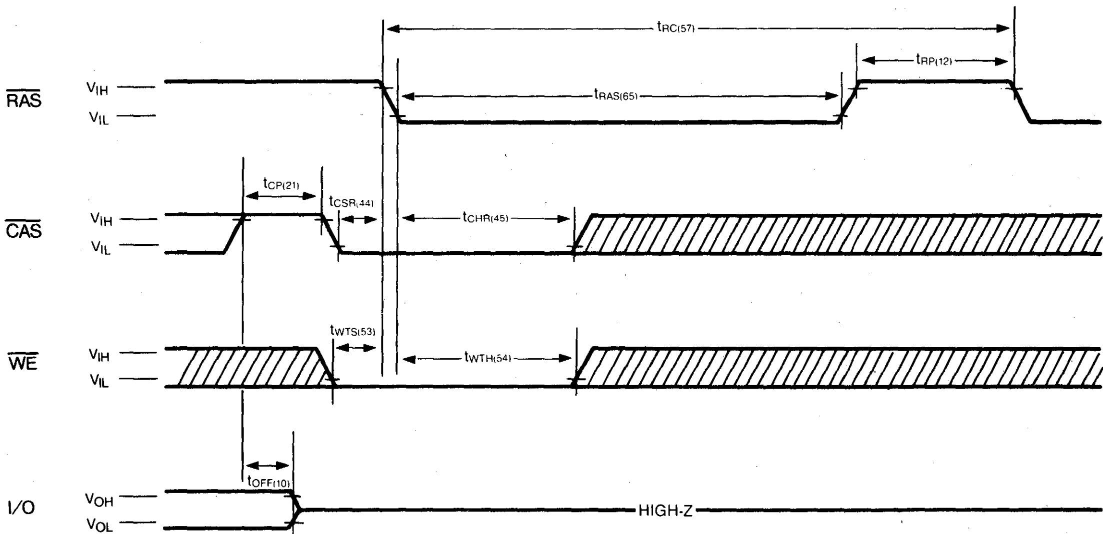
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



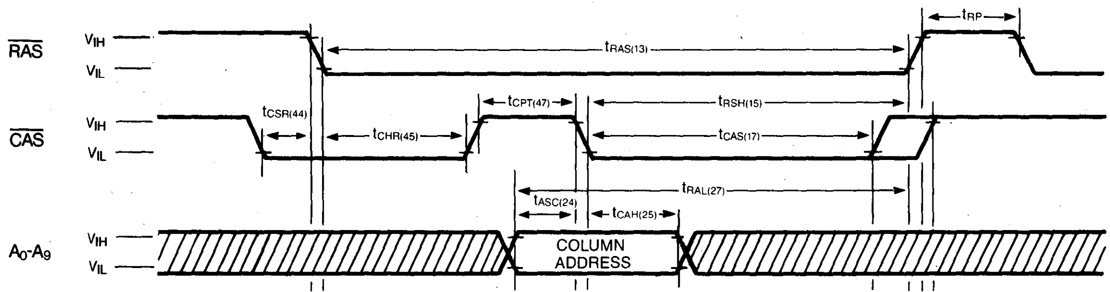
TEST MODE IN CYCLE



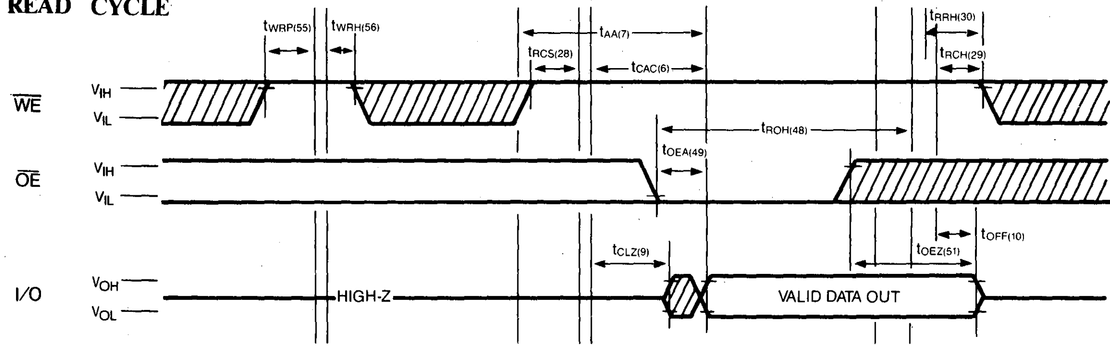
NOTE : $\overline{OE}$ and A_0-A_9 : "H" or "L"

3

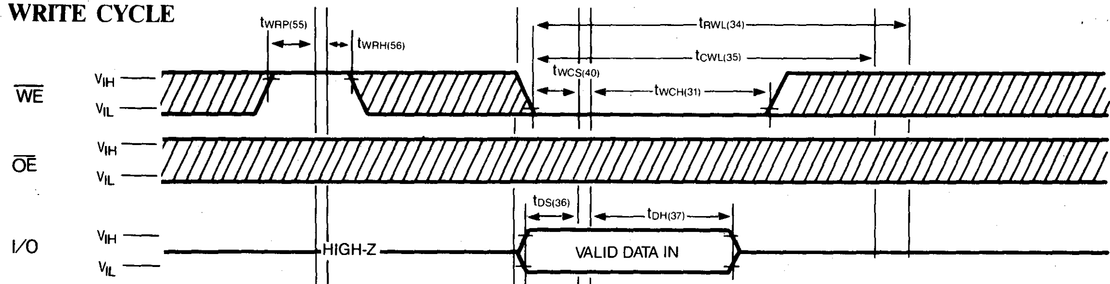
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



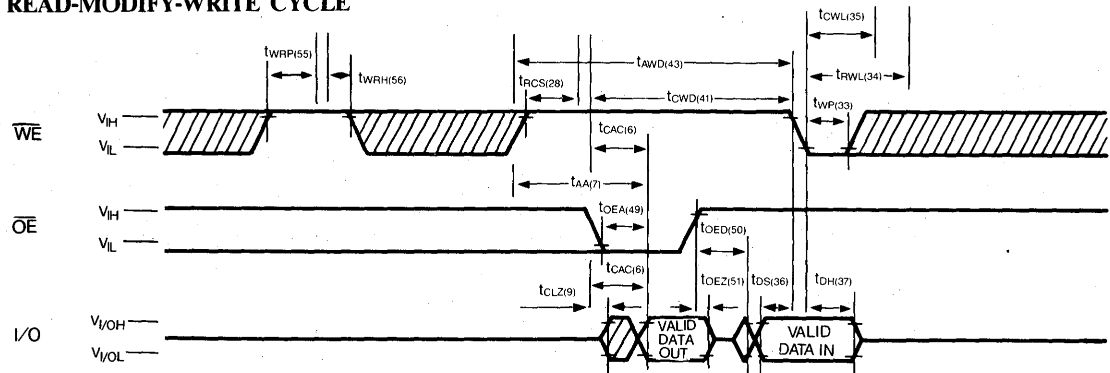
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE

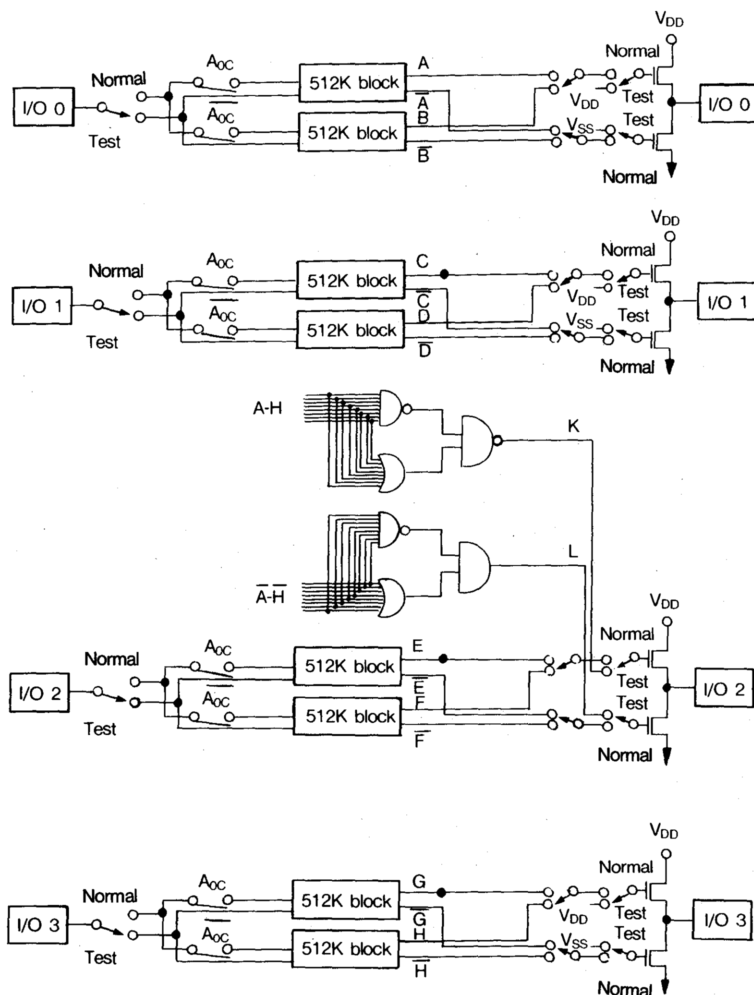


TEST MODE

The HY514400AL is a DRAM organized 1,048,576 words by 4 bits and it is internally organized 524,288 words by 8 bits. In Test Mode, data are written into 8 sectors in parallel and retrieved the same way. A_{0C} is not used. If, upon reading, the 8 bits are equal(all 0s or 1s), the I/O pin indicates 1. If they were not equal, the I/O pin indicates 0. The following figure shows the block diagram of HY514400AL. In Test Mode, 1M×4 DRAM can be tested as if it were a 512K×8 DRAM.

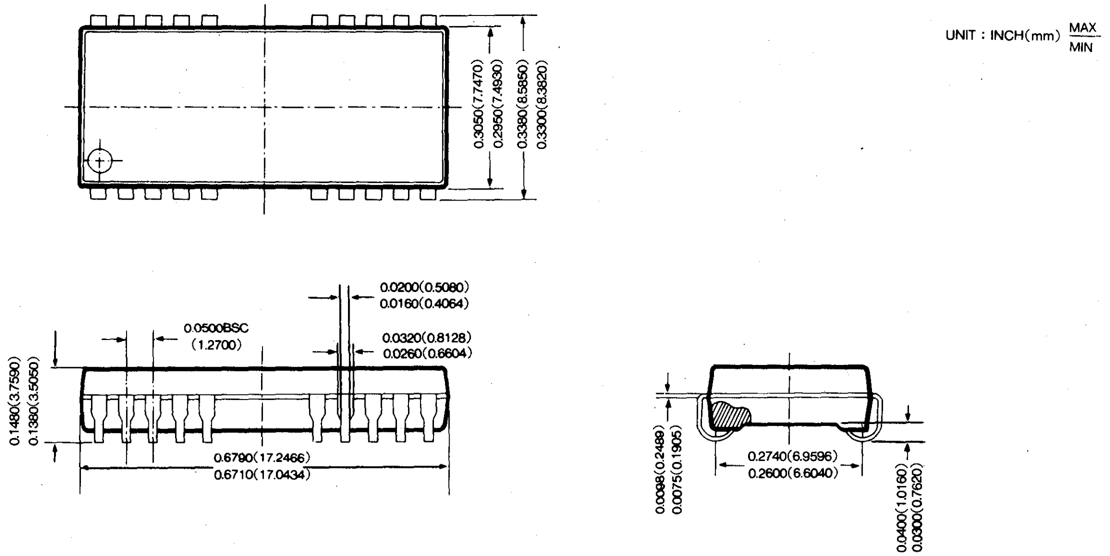
$\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle puts the device into Test Mode. And $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle or $\overline{RAS}$-Only Refresh Cycle puts it back into Normal Mode. In Test Mode, $\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle performs the refresh operation with the internal refresh address couter. The Test Mode function reduces test time to one-second in case of N test pattern.

BLOCK DIAGRAM IN TEST MODE

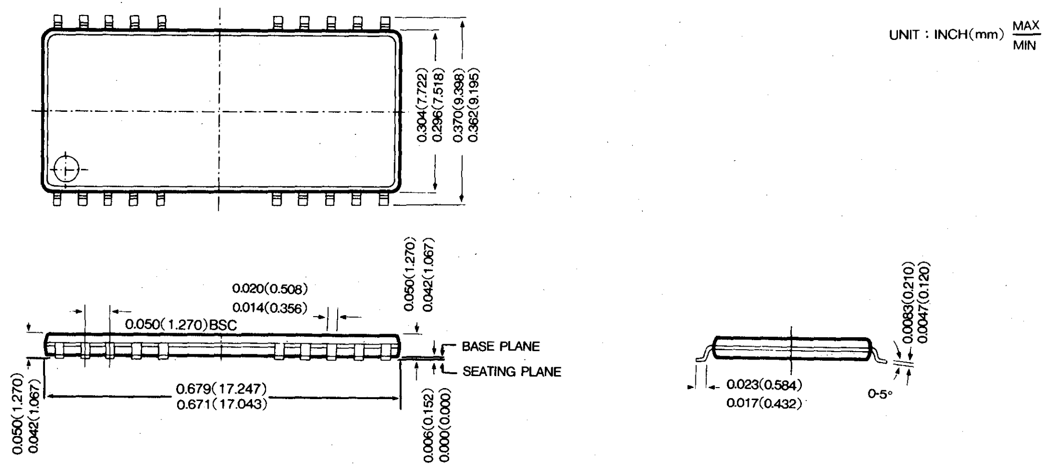


PACKAGE INFORMATION

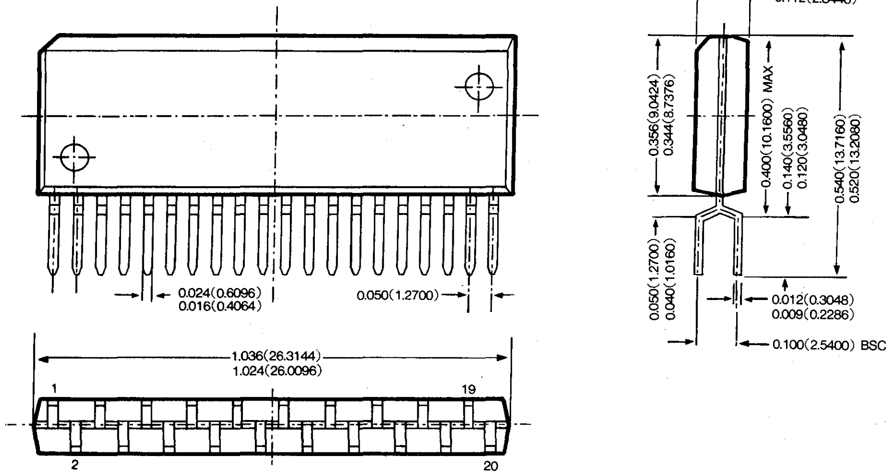
- **20/26 PIN SMALL OUTLINE J-FORM PACKAGE −300 MIL**



- **20/26 PIN THIN SMALL OUTLINE PACKAGE−300 MIL**



• **20 PIN ZIGZAG-IN-LINE PACKAGE-400 MIL**



3

MEMO

HYUNDAI SEMICONDUCTOR

HY514410A

1M×4-Bit CMOS DRAM

M1K1200A-MAR92

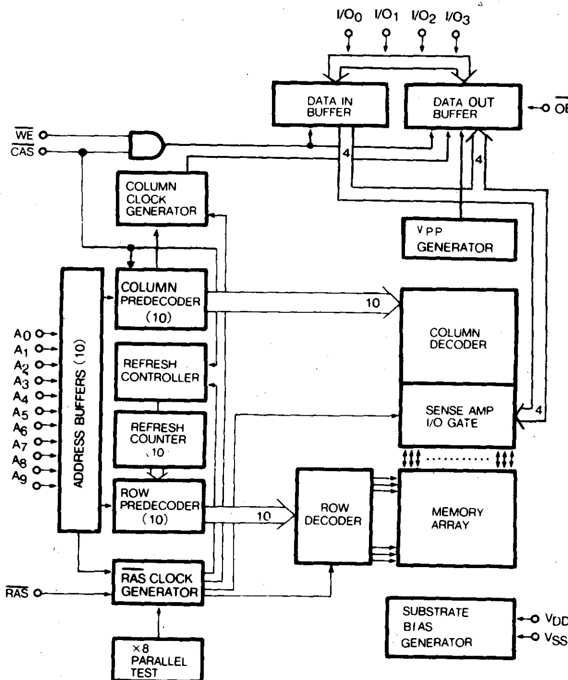
DESCRIPTION

The HY514410A is a high speed and new generation 1,048,576 words by 4 bits CMOS dynamic random access memory, fabricated with the HYUNDAI CMOS process. The HY514410A offers a fast page mode operation, write per bit function, wide operating margins, and inherently high CMOS reliability.

All inputs and outputs are TTL compatible. Multiplexed address inputs permit the HY514410A to be packaged in a standard 20/26 pin SOJ, TSOP, and 20 pin ZIP.

HY514410A design is optimized for cache based mainframe, and microcomputers, graphics digital signal processing, and high performance microprocessor systems.

BLOCK DIAGRAM

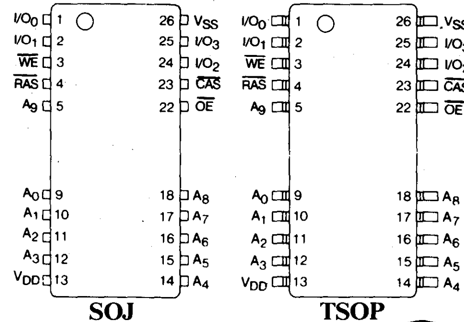


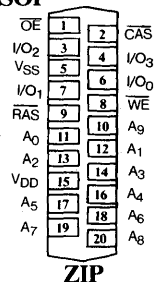
FEATURES

- Low power dissipation
  - Operating Current, 80ns : 90mA(max.)
  - TTL Standby Current : 2mA(max.)
  - CMOS Standby Current: 1mA(max.)
- Read-Modify-Write Capability
- $\overline{RAS}$-only, Hidden, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Capability
- Common I/O Capability
- Fast Page mode and Test mode Capability
- Write per Bit mode Capability
- Single 5V± 10% power supply
- 1024 refresh cycles/16 ms
- High reliability 300 mil 20/26 pin SOJ, TSOP and 400mil 20 pin ZIP
- Fast access time and cycle time(ns)

	HY514410A-60	HY514410A-70	HY514410A-80
Max $\overline{RAS}$ Access Time, t_{RAC}	60	70	80
Max $\overline{CAS}$ Access Time, t_{CAC}	20	20	25
Min Fast Page Mode Cycle Time, t_{PC}	40	45	55
Min Cycle Time, t_{RC}	120	130	150

PIN CONNECTIONS





PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
A_0-A_9	ADDRESS INPUT
I/O_0-I/O_3	DATA INPUT/OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
T_{SOLDER}	Soldering Temperature, Time	260, 10	℃, sec
P_T	Power Dissipation	770	mW

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS
(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY514410A		UNIT	NOTE
				MIN.	MAX.		
$\mid I_{LI} \mid$	Input Leakage Current(any input pin)	0V≤V_{IN}≤6.5V, All other pin not under test=V_{SS}		−	10	μA	
$\mid I_{LO} \mid$	Output Leakage Current for High Impedance State	D_{OUT} is disable, 0V≤V_{OUT}≤5.5V		−	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$\overline{RAS}$, $\overline{CAS}$, Address cycling, t_{RC}=t_{RC}(min.)	−60	−	110	mA	1, 2, 4
			−70	−	100		
			−80	−	90		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$=$\overline{CAS}$=V_{IH}		−	2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}, t_{RC}=t_{RC}(min.)	−60	−	110	mA	1, 4
			−70	−	100		
			−80	−	90		
I_{DD4}	V_{DD} Supply Current, Fast page mode	$\overline{RAS}$=V_{IL}, Address cycling, t_{PC}=t_{PC}(min.)	−60	−	70	mA	1, 2, 4
			−70	−	60		
			−80	−	50		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}$=$\overline{CAS}$=V_{DD}−0.2V		−	1	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{RC}(min.)	−60	−	110	mA	1, 4
			−70		100		
			−80	−	90		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		−	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	−	V	

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 3, 4, 5

#	SYMBOL	PARAMETER	HY514410A 60 MIN.	60 MAX.	70 MIN.	70 MAX.	80 MIN.	80 MAX.	UNIT	NOTE
1	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
2	t_{RWC}	Read-Modify-Write Cycle Time	175	–	185	–	210	–	ns	
3	t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	55	–	ns	
4	t_{PRWC}	Fast Page Mode RMW Cycle Time	95	–	100	–	115	–	ns	
5	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	7, 12
6	t_{CAC}	Access Time From $\overline{CAS}$	–	20	–	20	–	25	ns	7, 12
7	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	7, 12
8	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	7
9	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	ns	7
10	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	8
11	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	6
12	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	50	–	60	–	ns	
13	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	200K	70	200K	80	200K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
17	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
18	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	20	55	ns	12
19	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	13
20	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
21	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
22	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
23	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
24	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
25	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
26	t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
27	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
28	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
29	t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	9
30	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	9
31	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
32	t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
33	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
34	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
35	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
36	t_{DS}	Data Set-up Time	0	–	0	–	0	–	ns	10
37	t_{DH}	Data Hold Time	15	–	15	–	15	–	ns	10
38	t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
39	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
40	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	11
41	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	–	50	–	55	–	ns	11
42	t_{RWD}	RAS to $\overline{WE}$ Delay Time	90	–	100	–	110	–	ns	11
43	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60	–	65	–	70	–	ns	11

3

#	SYMBOL	PARAMETER	HY514410A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
44	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
45	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	30	–	ns	
46	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
47	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	30	–	35	–	40	–	ns	
48	t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	10	–	ns	
49	t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	20	ns	
50	t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	20	–	ns	
51	t_{OEZ}	Output Buffer Turn-off Delay Time from $\overline{OE}$	0	20	0	20	0	20	ns	
52	t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	20	–	ns	
53	t_{WTS}	Write Command Set-up Time(Test Mode In)	10	–	10	–	10	–	ns	
54	t_{WTH}	Write Command Hold Time(Test Mode In)	10	–	10	–	10	–	ns	
55	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
56	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

AC CHARACTERISTICS IN THE TEST MODE Note : 14

#	SYMBOL	PARAMETER	HY514410A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
57	t_{RC}	Random Read or Write Cycle Time	125	–	135	–	155	–	ns	
58	t_{RWC}	Read-Modify-Write Cycle Time	180	–	190	–	215	–	ns	
59	t_{PC}	Fast Page Mode Cycle Time	45	–	50	–	60	–	ns	
60	t_{PRWC}	Fast Page Mode RMW Cycle Time	100	–	105	–	120	–	ns	
61	t_{RAC}	Access Time from $\overline{RAS}$	–	65	–	75	–	85	ns	7, 12
62	t_{CAC}	Access Time from $\overline{CAS}$	–	25	–	25	–	30	ns	7, 12
63	t_{AA}	Access Time from Column Address	–	35	–	40	–	45	ns	7, 12
64	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	45	–	55	ns	7
65	t_{RAS}	$\overline{RAS}$ Pulse Width	65	10K	75	10K	85	10K	ns	
66	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	65	200K	75	200K	85	200K	ns	
67	t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
68	t_{CSH}	$\overline{CAS}$ Hold Time	65	–	75	–	85	–	ns	
69	t_{CAS}	$\overline{CAS}$ Pulse Width	25	10K	25	10K	30	10K	ns	
70	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	45	–	ns	
71	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	55	–	55	–	60	–	ns	11
72	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	95	–	105	–	115	–	ns	11
73	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	70	–	75	–	ns	11
74	t_{OEA}	$\overline{OE}$ Access Time	–	25	–	25	–	25	ns	
75	t_{OED}	$\overline{OE}$ to Data Delay	25	–	25	–	25	–	ns	
76	t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	25	–	25	–	ns	

AC CHARACTERISTICS IN THE WRITE PER BIT MODE

#	SYMBOL	PARAMETER	HY514410A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
77	t_{WBS}	Write Per Bit Set-Up Time	0	—	0	—	0	—	ns	
78	t_{WBH}	Write Per Bit Hold Time	10	—	10	—	10	—	ns	
79	t_{WPS}	Write Per Bit Selection Set-Up Time	0	—	0	—	0	—	ns	
80	t_{WPH}	Write Per Bit Selection Hold Time	10	—	10	—	10	—	ns	

NOTES :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6}, I_{CC7} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. It depends on user whether column address is changed or not at least once while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
5. AC measurements assume t_T=5ns.
6. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Measured with a load equivalent to 2 TTL loads and 100pF.
8. t_{OFF}(max.) and t_{OEZ} define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle : If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.) the cycle is a read-modify-write cycle and data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
12. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
13. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
14. These specifications are applied to the test mode.

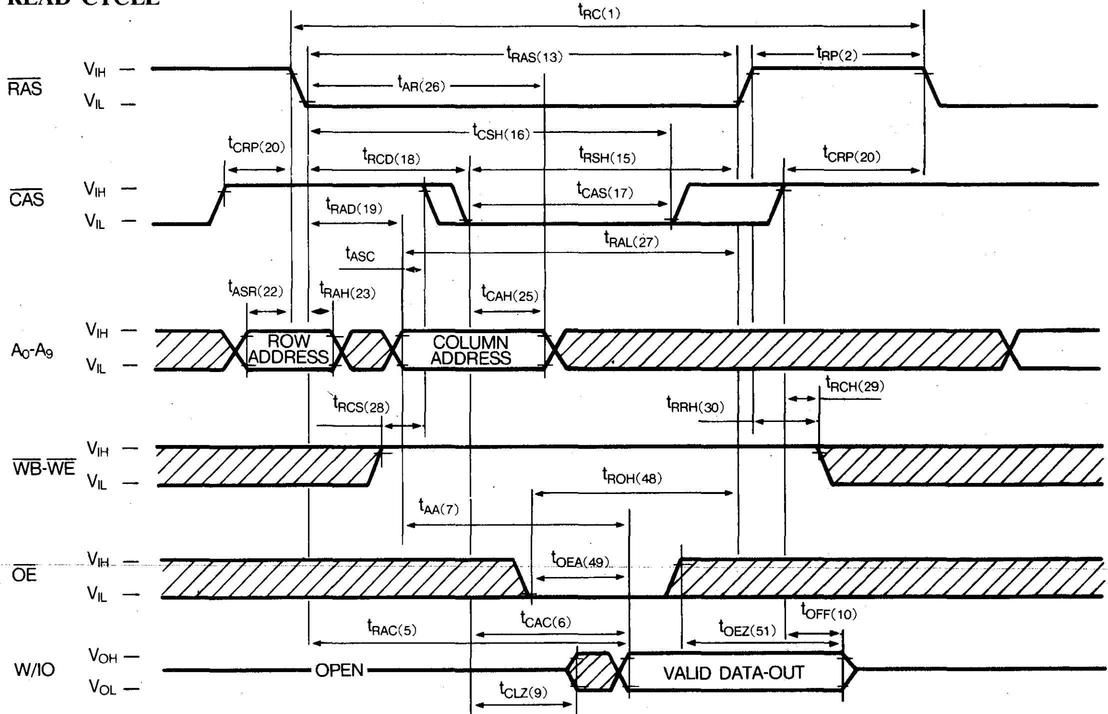
CAPACITANCE

(T_A=0°C to 70°C, V_{DD}=5V± 10%, f=1MHz)

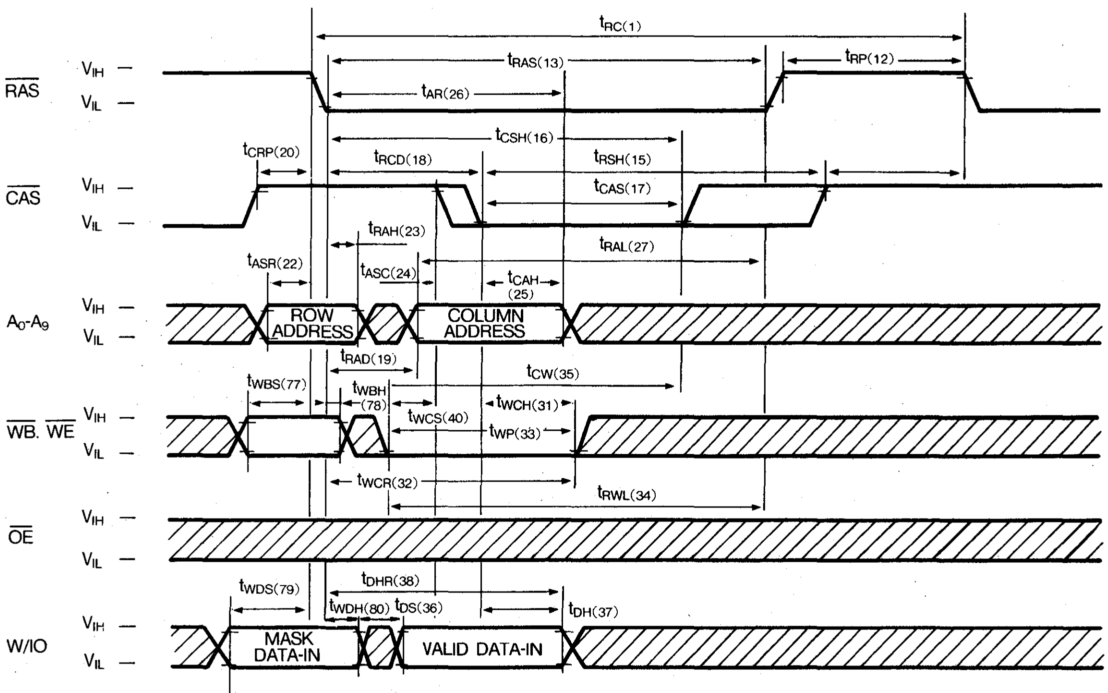
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_9, Data In)	–	5	pF
C_{IN2}	Input Capacitance($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	–	7	pF
C_{OUT}	Output Capacitance(Data Out)	–	7	pF

TIMING DIAGRAM

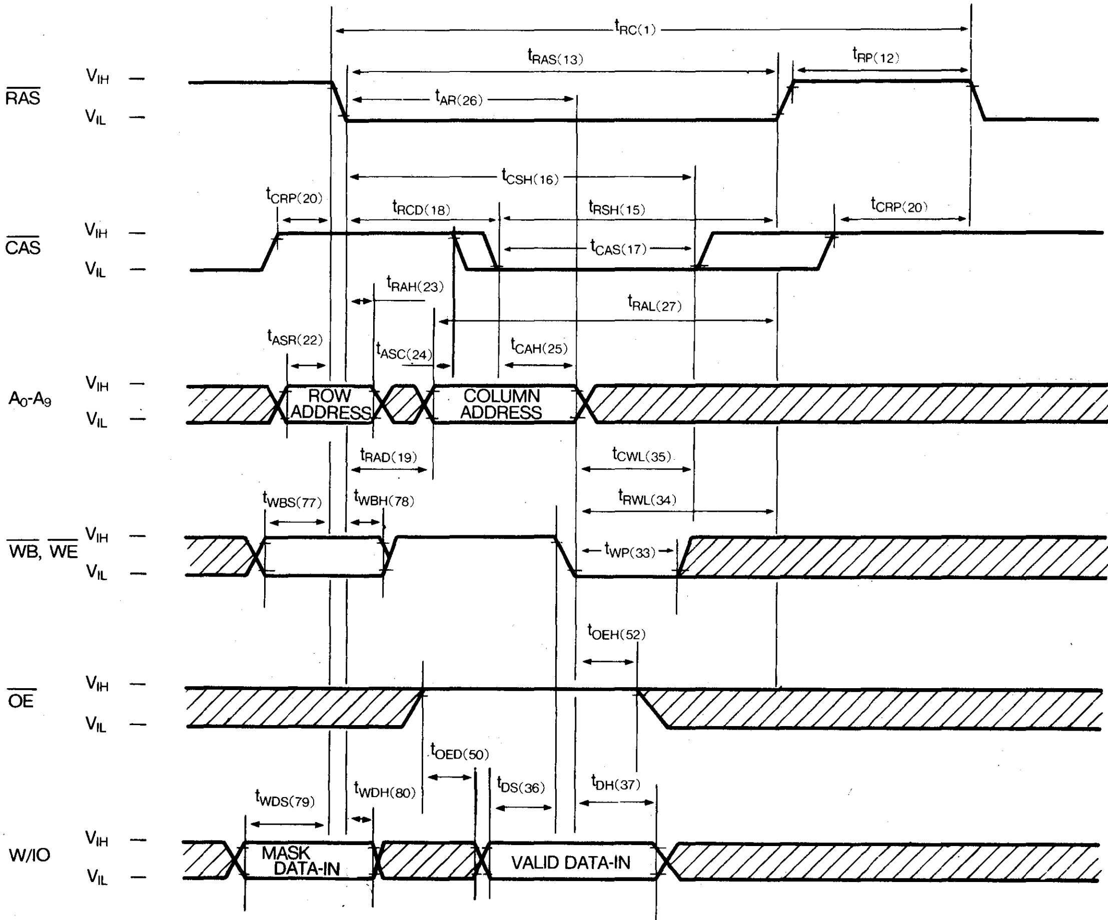
READ CYCLE



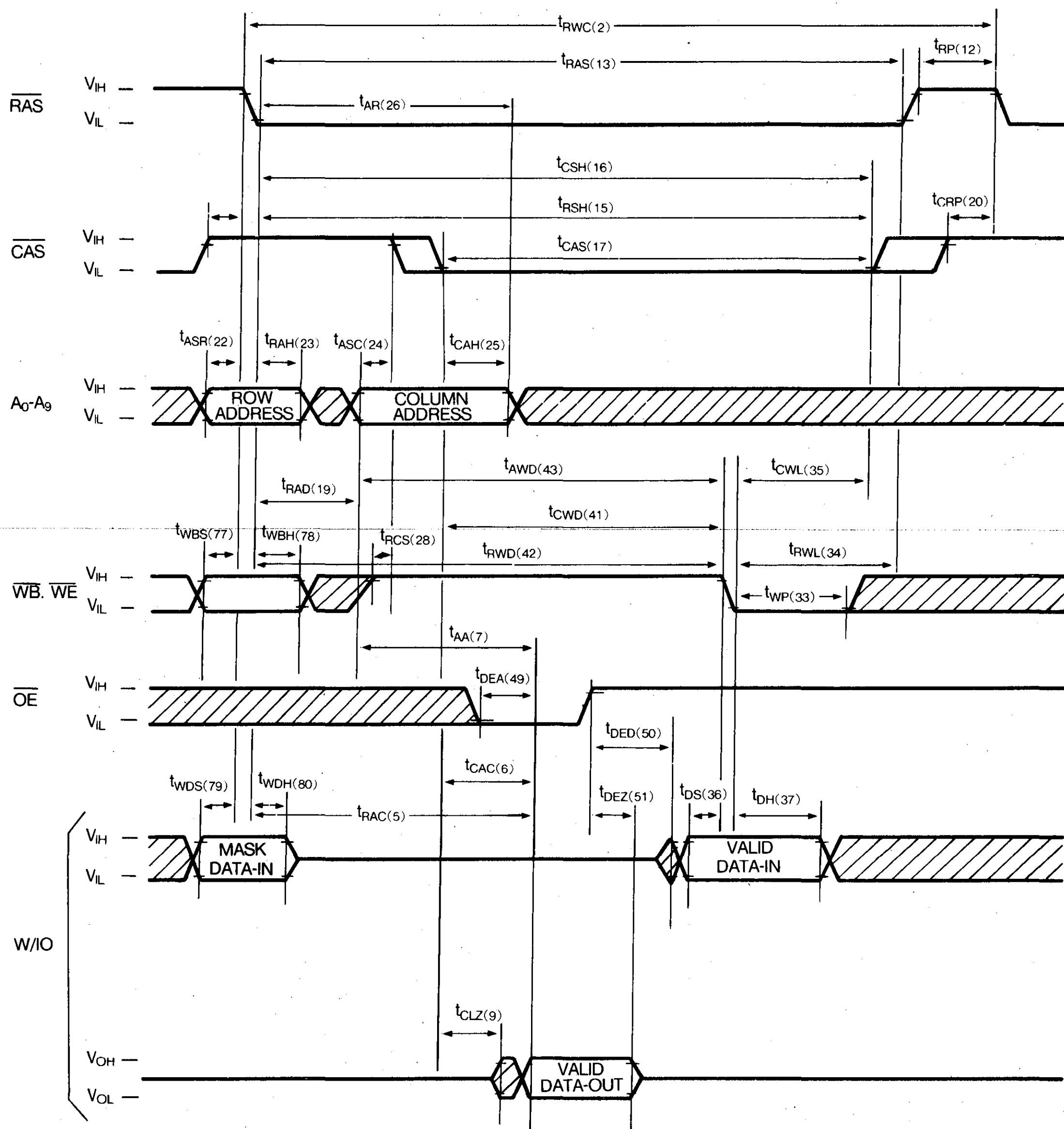
WRITE CYCLE (EARLY WRITE)



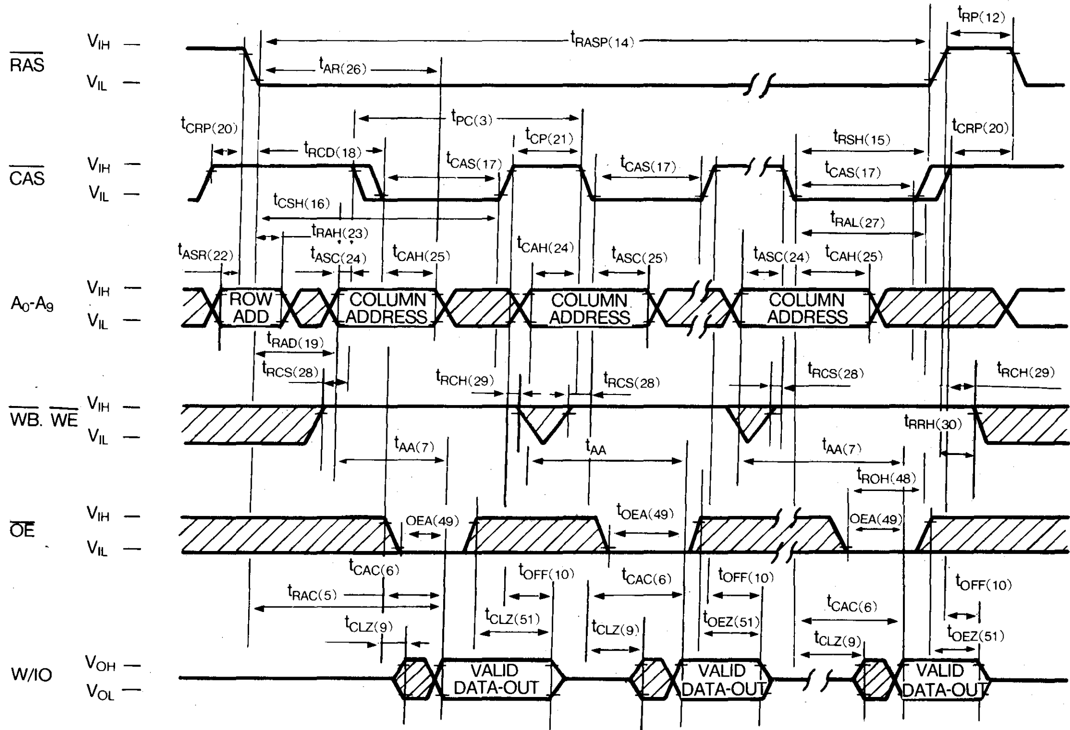
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



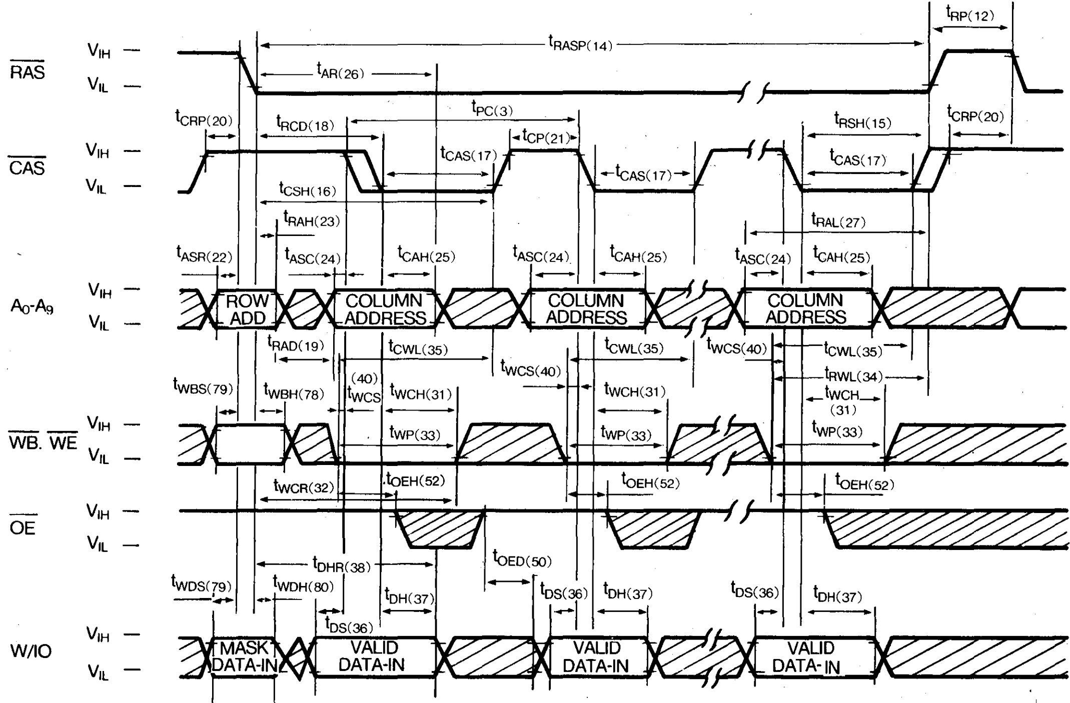
READ-MODIFY-WRITE CYCLE



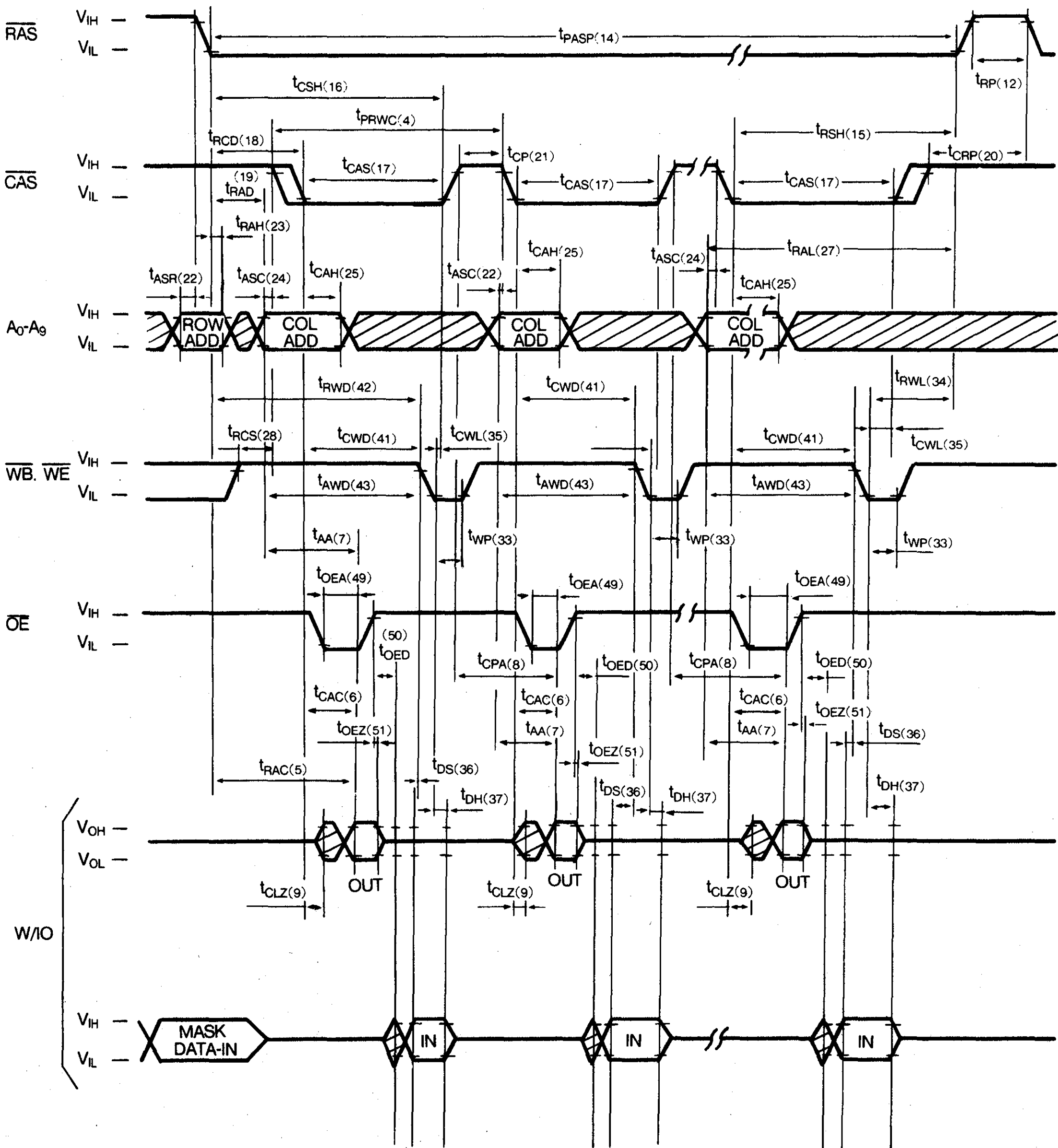
FAST PAGE MODE READ CYCLE



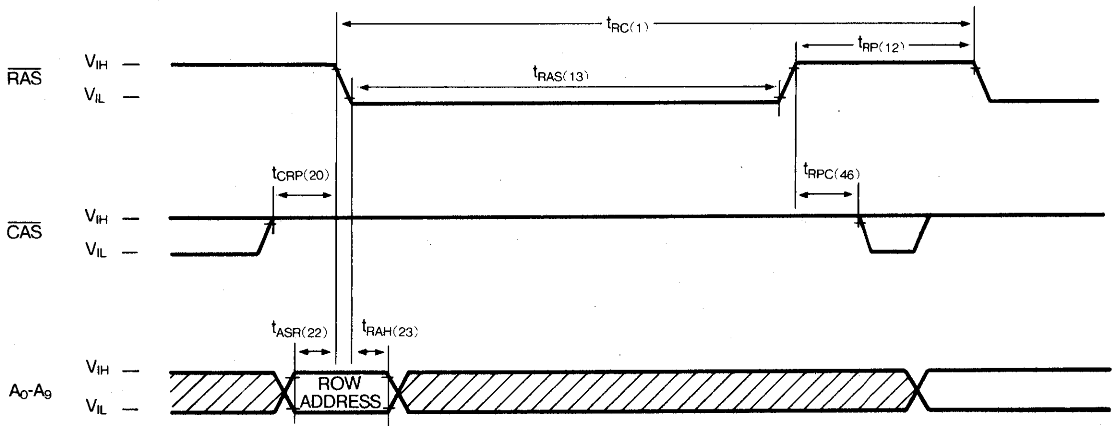
FAST PAGE MODE WRITE CYCLE



FAST PAGE MODE READ-MODIFY-WRITE CYCLE

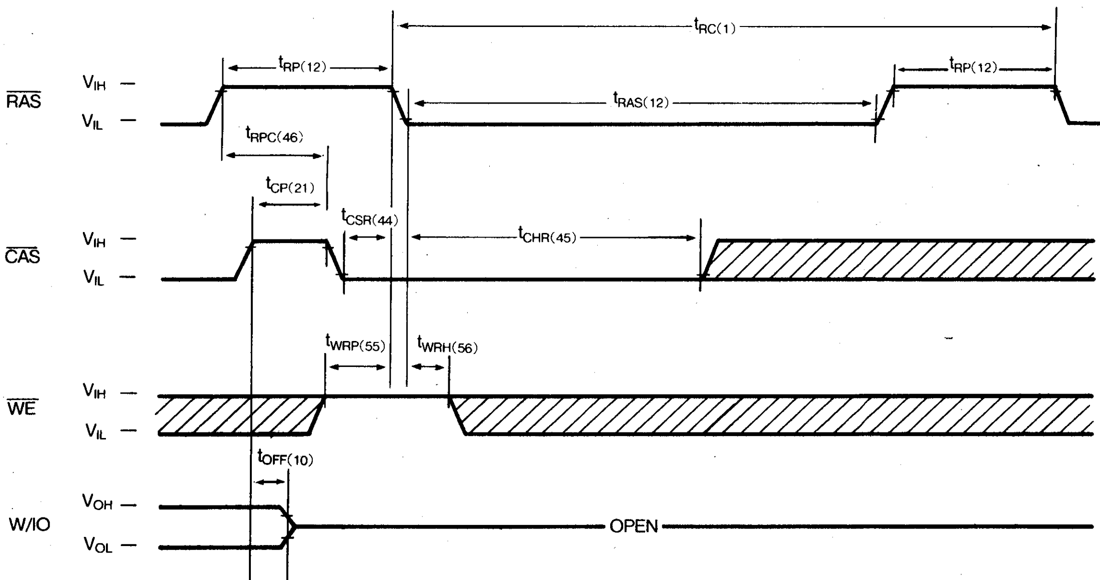


RAS ONLY REFRESH CYCLE



NOTE : WB/WE, OE : "H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE



NOTE : OE A0~A9 : "H" or "L"

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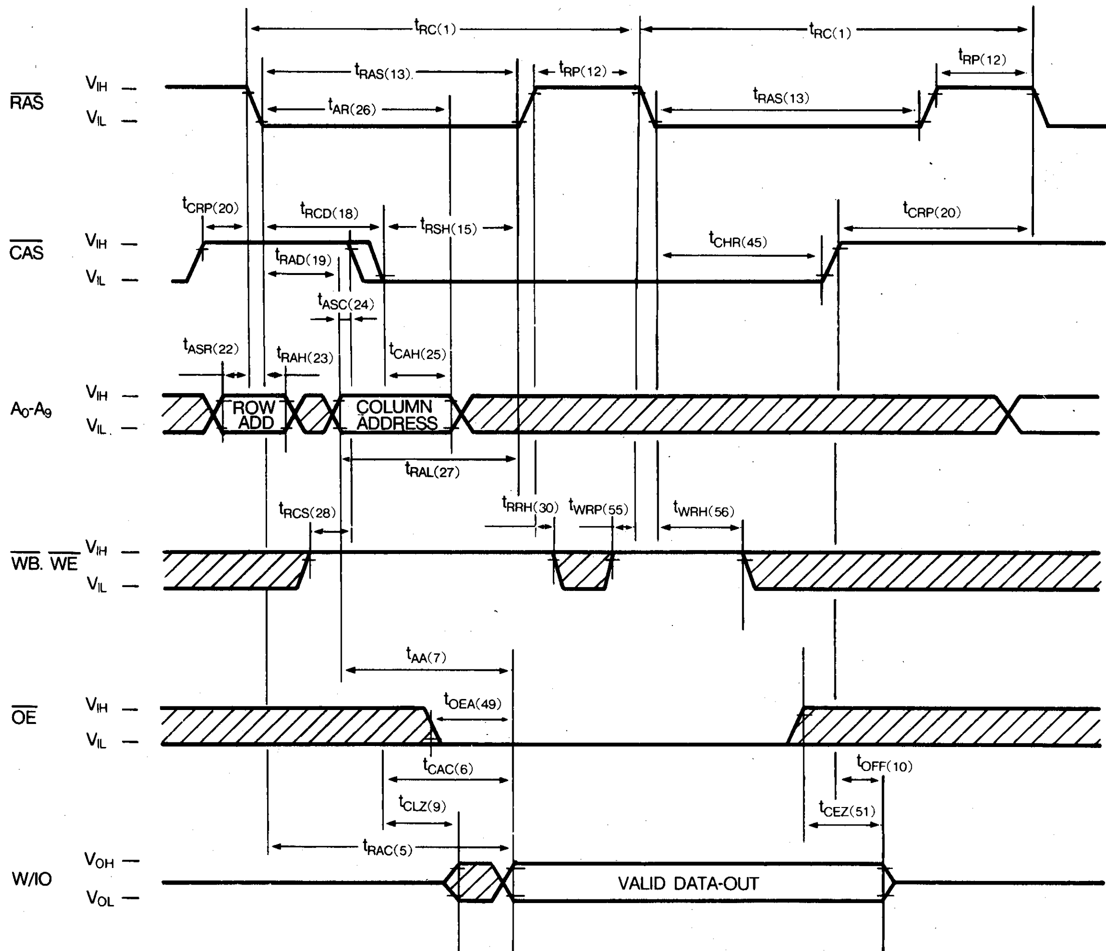
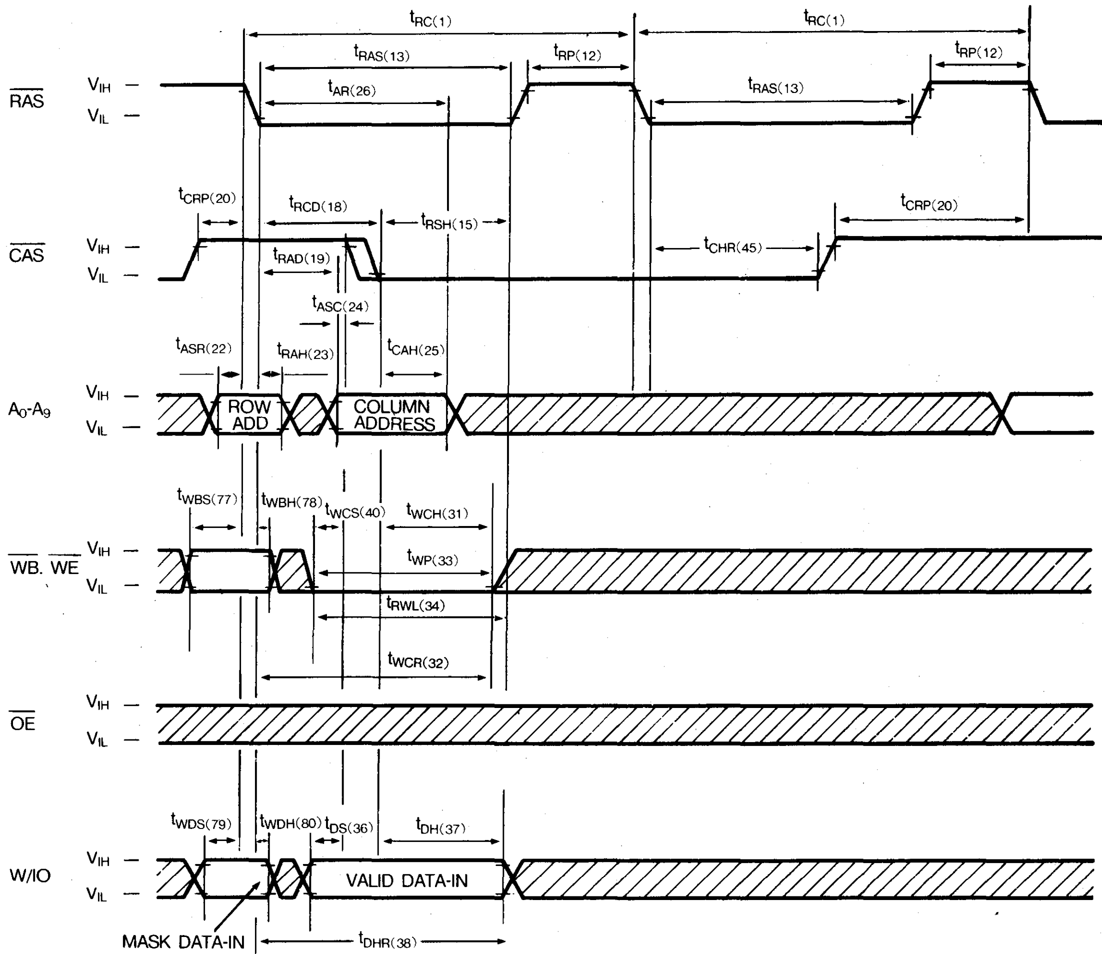
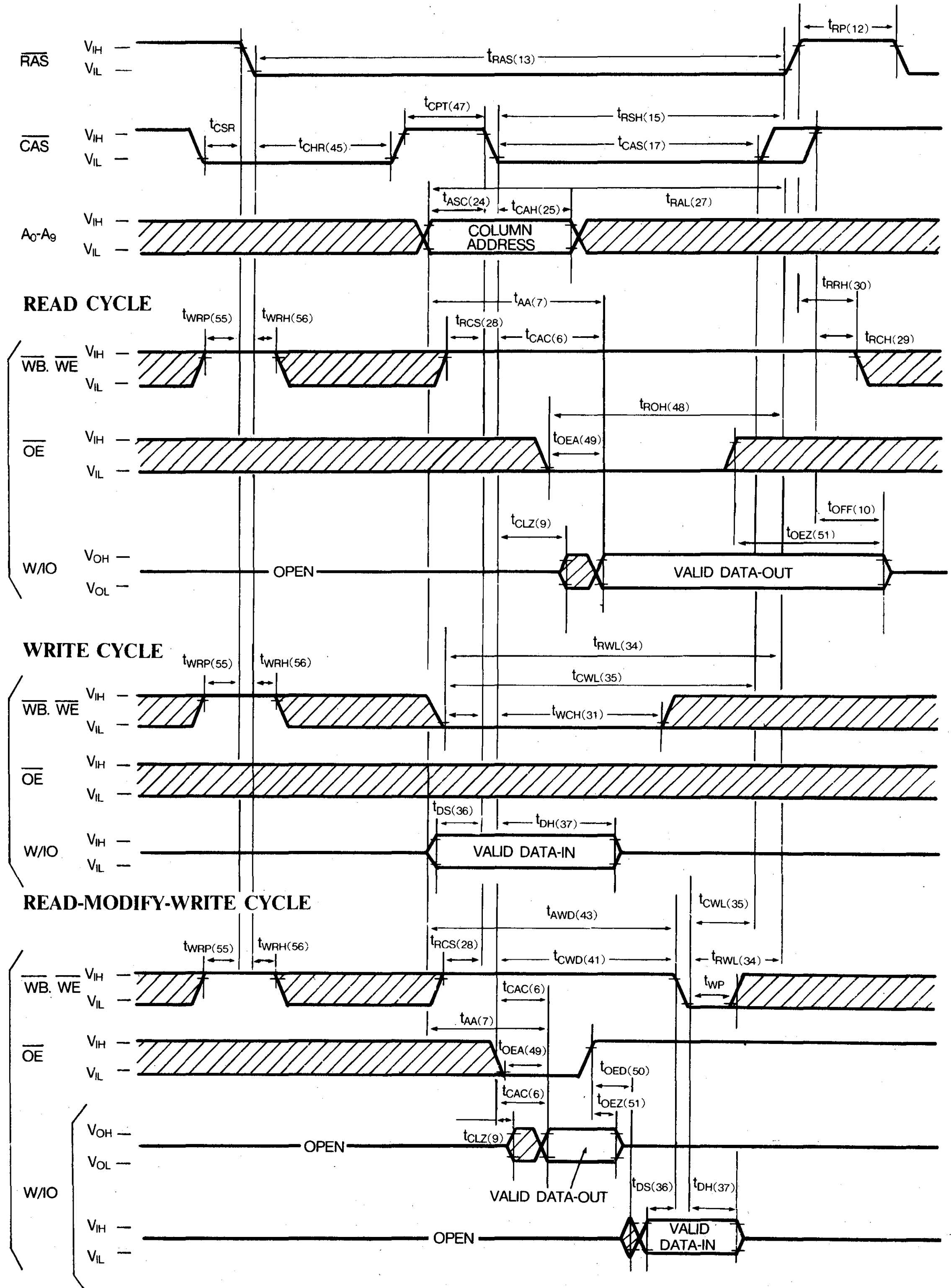
HIDDEN REFRESH CYCLE(READ)



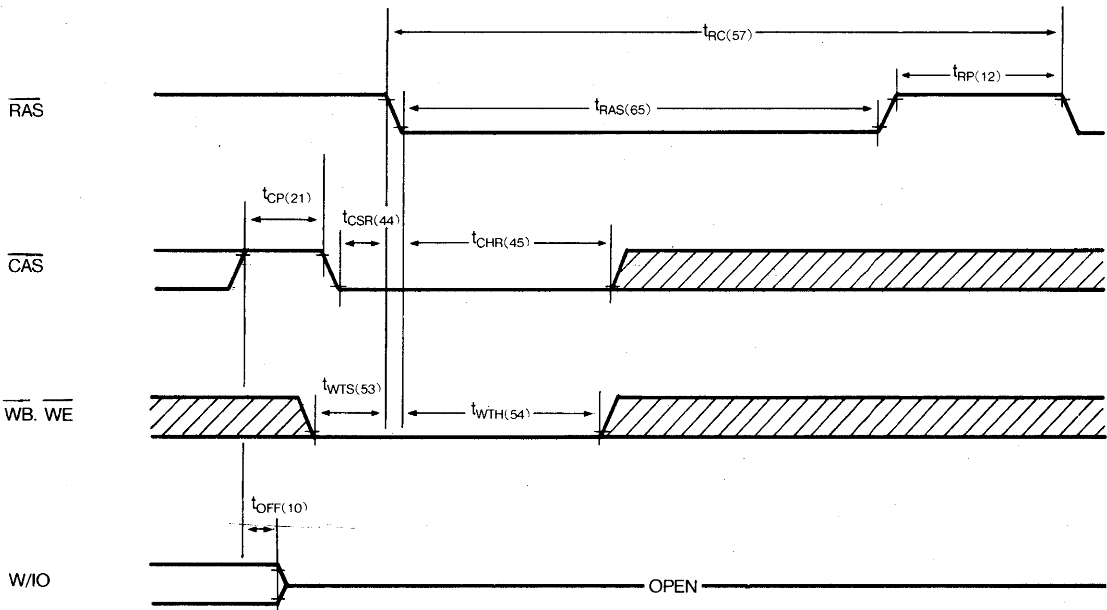
HIDDEN REFRESH CYCLE(WRITE)



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TEST MODE IN CYCLE



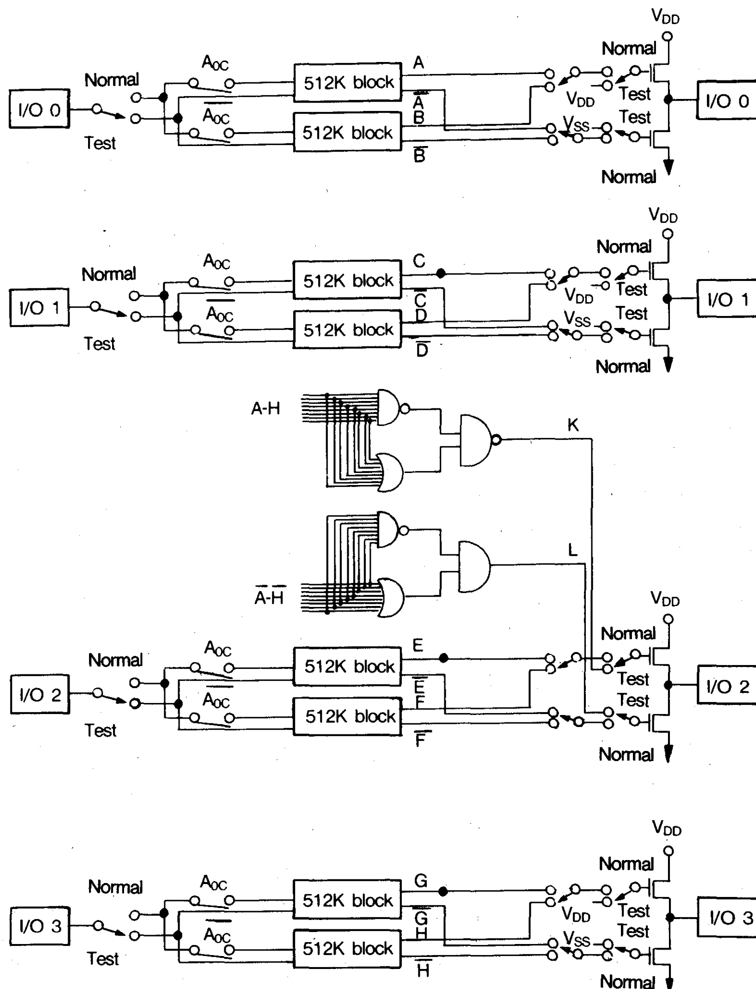
NOTE : OE $A_0 \sim A_9$: "H" or "L"

TEST MODE

The HY514410A is a DRAM organized 1,048,576 words by 4 bits and it is internally organized 524,288 words by 8 bits. In Test Mode, data are written into 8 sectors in parallel and retrieved the same way. A_{0C} is not used. If, upon reading, the 8 bits are equal(all 1s or 0s), the I/O pin indicates 1. If they were not equal, the I/O pin indicates 0. The following figure shows the block diagram of HY514410A. In Test Mode, 1M×4 DRAM cab be tested as if it were a 512K×8 DRAM.

$\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle puts the device into Test Mode. And $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle or $\overline{RAS}$-Only Refresh Cycle puts it back into Normal Mode. In Test Mode, $\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle performs the refresh operation with the internal refresh address couter. The Test Mode function reduces test time to one-second in case of N test pattern.

BLOCK DIAGRAM IN TEST MODE



WRITE-PER-BIT FUNCTION

The write-per-bit function selectively control the internal write-enable circuit of the DRAM. When $\overline{WB}/\overline{WE}$ is held 'low' at the falling edge of $\overline{RAS}$ during a random access operation, the write-mask is enabled. At the sametime, the mask data on the W_i/IO_i pins is latched onto the write-mask register(WMR). When a '0' is sensed on any of the W_i/IO_i pins, their corresponding write circuits are disabled and new data will not be written.

When '1" is sensed on any of the W_i/IO_i pins, their corresponding write circuit will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in table 1.

Table1 : Truth table for write-per-bit function

At the falling edge of $\overline{RAS}$				Function
$\overline{CAS}$	$\overline{OE}$	$\overline{WB}/\overline{WE}$	$W_i/IO_i(i=1\sim4)$	
H	H	H	•	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

An example of the write-per-bit function illustrating its application to displays is shown in Fig-1 and Fig-2.

Fig-1 : Write-per-bit timing cycle

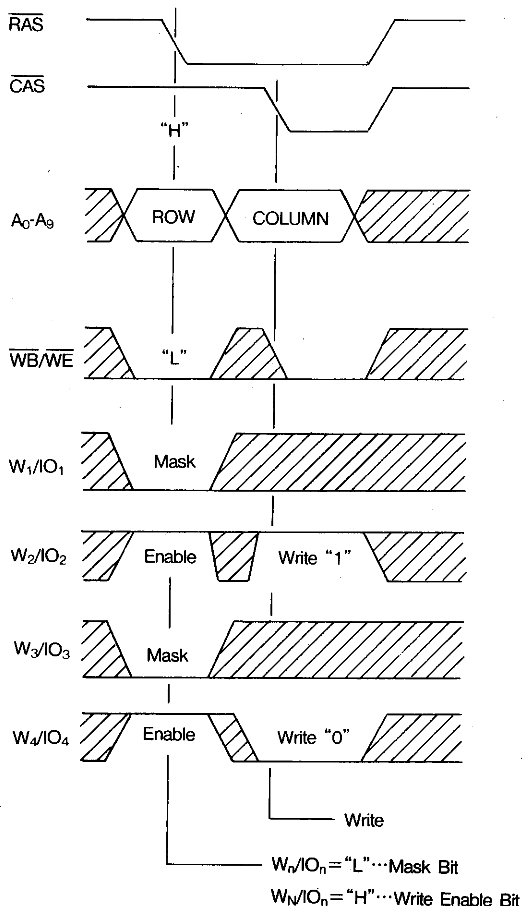
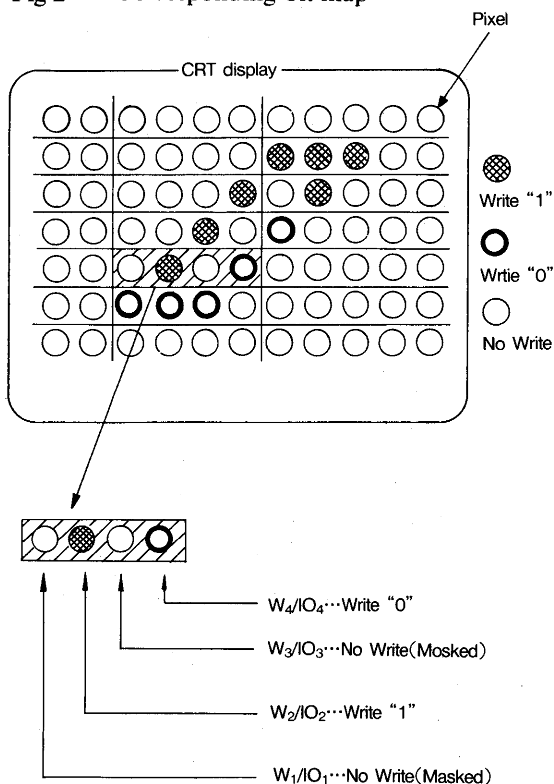


Fig-2 : Corresponding bit-map



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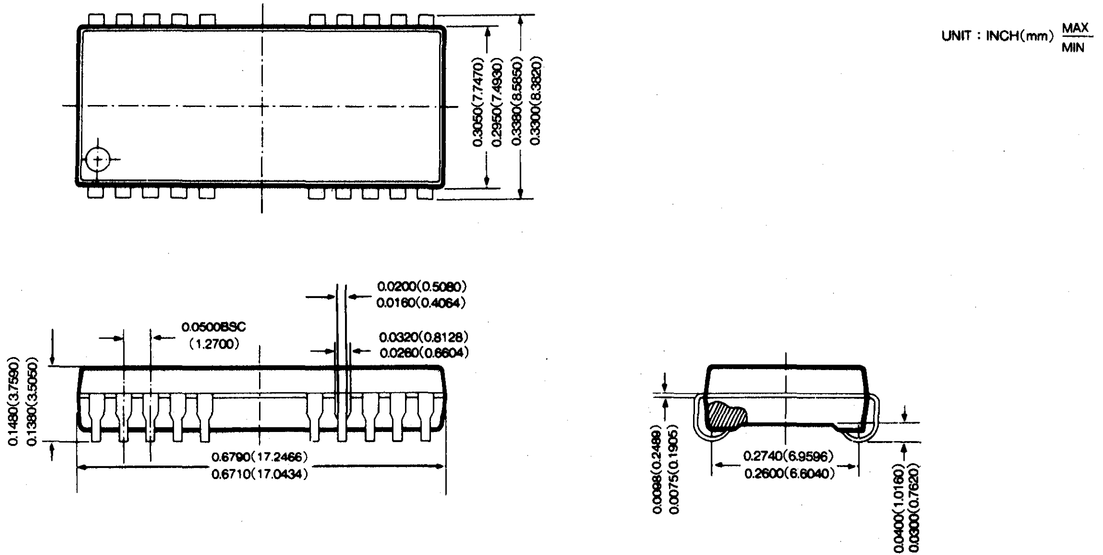
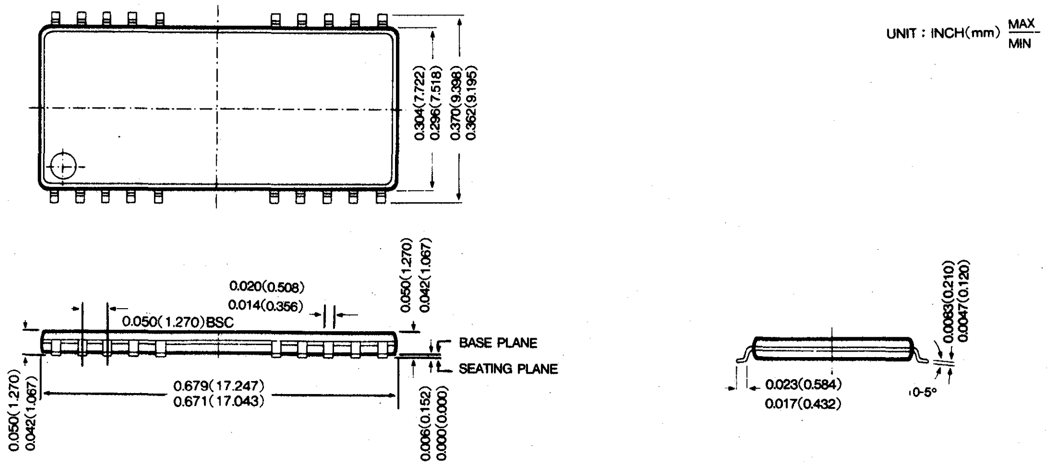
PACKAGE INFORMATION

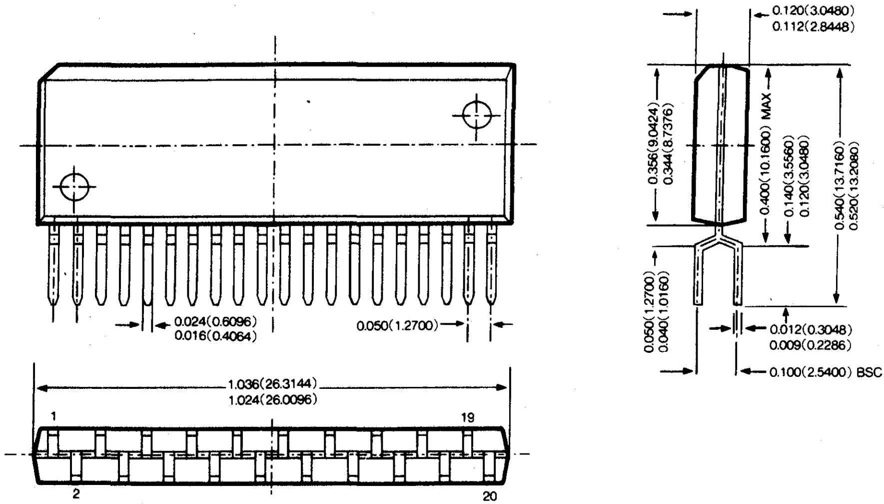
- **20/26 PIN SMALL OUTLINE J-FORM PACKAGE −300 MIL**



- **20/26 PIN THIN SMALL OUTLINE PACKAGE−300 MIL**



- **20 PIN ZIGZAG-IN-LINE PACKAGE−400MIL**



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MEMO

HYUNDAI SEMICONDUCTOR

HY514410AL

1M×4-Bit CMOS DRAM

M1L1200A-MAR92

DESCRIPTION

The HY514410AL is a high speed, low power 1,048,576 words by 4 bits CMOS dynamic random access memory, fabricated with the HYUNDAI CMOS process. The HY514410AL offers a fast page mode operation, write per bit function, wide operating margins, and inherently high CMOS reliability.

All inputs and outputs are TTL compatible. Multiplexed address inputs permit the HY514410AL to be packaged in a standard 20/26 pin SOJ, TSOP, and 20 pin ZIP.

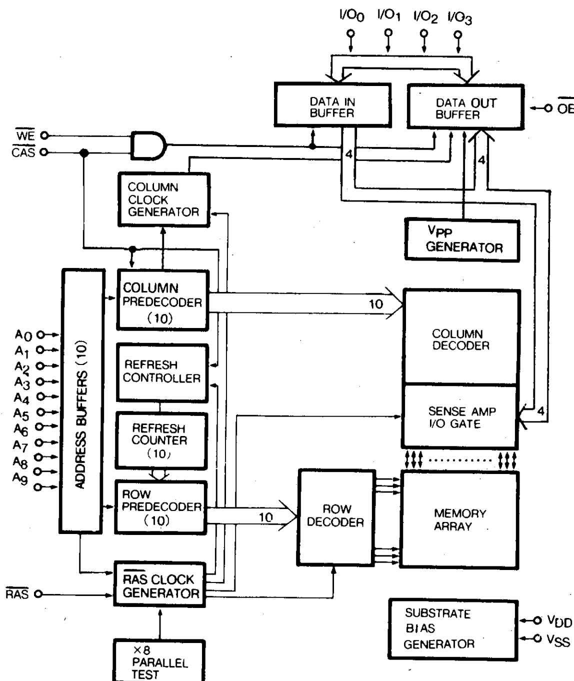
HY514410AL design is optimized for cache based mainframe, and microcomputers, graphics digital signal processing, and high performance microprocessor systems.

FEATURES

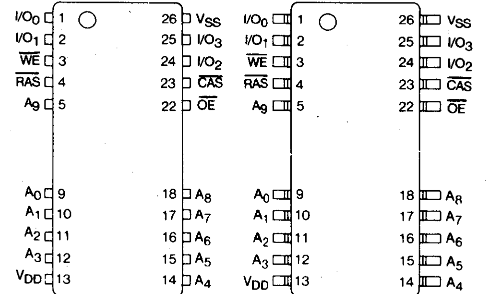
- **Low power dissipation**
  - **Operating Current, 80ns : 90mA(max.)**
  - **TTL Standby Current : 2mA(max.)**
  - **CMOS Standby Current : 200μA(max.)**
  - **Battery Back Up Current : 300μA(max.)**
- **Read-Modify-Write Capability**
- **$\overline{\text{RAS}}$-only, Hidden, $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Capability**
- **Common I/O Capability**
- **Fast Page mode and Test mode Capability**
- **Write per Bit mode Capability**
- **Single 5V± 10% power supply**
- **1024 refresh cycles/128 ms**
- **High reliability 300 mil 20/26 pin SOJ, TSOP and 400mil 20 pin ZIP**
- **Fast access time and cycle time(ns)**

	HY514410AL-60	HY514410AL-70	HY514410AL-80
Max $\overline{\text{RAS}}$ Access Time, t_{RAC}	60	70	80
Max $\overline{\text{CAS}}$ Access Time, t_{CAC}	20	20	25
Min Fast Page Mode Cycle Time, t_{PC}	40	45	55
Min Cycle Time, t_{RC}	120	130	150

BLOCK DIAGRAM

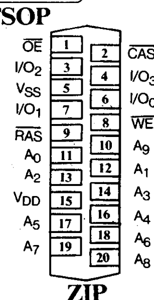


PIN CONNECTIONS



PIN NAMES

$\overline{\text{RAS}}$	ROW ADDRESS STROBE
$\overline{\text{CAS}}$	COLUMN ADDRESS STROBE
$\overline{\text{WE}}$	WRITE ENABLE
$\overline{\text{OE}}$	OUTPUT ENABLE
A_0-A_9	ADDRESS INPUT
I/O_0-I/O_3	DATA INPUT/OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
T_{SOLDER}	Soldering Temperature Time	260, 10	℃, sec
P_T	Power Dissipation	770	mW

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A= 0°C to 70°C V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY514410AL MIN.	HY514410AL MAX.	UNIT	NOTE
$\|I_{LI}\|$	Input Leakage Current(any input pin)	0V≤V_{IN}≤6.5V, All other pin not under test=V_{SS}		−	10	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	D_{OUT} is disable, 0V≤V_{OUT}≤5.5V		−	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$\overline{RAS}$, $\overline{CAS}$, Address cycling, t_{RC}=t_{RC}(min.)	−60	−	110	mA	1, 2, 4
			−70	−	100		
			−80	−	90		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$=$\overline{CAS}$=V_{IH}		−	2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}, t_{RC}=t_{RC}(min.)	−60	−	110	mA	1, 4
			−70	−	100		
			−80	−	85		
I_{DD4}	V_{DD} Supply Current, Fast page mode	$\overline{RAS}$=V_{IL}, Address cycling, t_{PC}=t_{PC}(min.)	−60	−	70	mA	1, 2, 4
			−70	−	60		
			−80	−	50		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}$=$\overline{CAS}$=V_{DD}−0.2V		−	200	μA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{RC}(min.)	−60	−	110	mA	1, 4
			−70		100		
			−80	−	90		
I_{DD7}	V_{DD} Supply Current, Battery Back up	$\overline{CAS}$=CBR cycling or 0.2V, $\overline{OE}$=$\overline{WE}$=V_{DD}−0.2V, Add=V_{DD}−0.2V or 0.2V, I/O=V_{DD}−0.2V or 0.2V or open, t_{RC}=125μs, t_{RAS}=t_{RAS}(min.) ~300ns		−	300	μA	1
		Same as above except t_{RAS}=300ns~1μs		−	400	μA	1, 5
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		−	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	−	V	

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 3, 4, 5, 6

#	SYMBOL	PARAMETER	HY514410AL 60 MIN.	60 MAX.	70 MIN.	70 MAX.	80 MIN.	80 MAX.	UNIT	NOTE
1	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
2	t_{RWC}	Read-Modify-Write Cycle Time	175	–	185	–	210	–	ns	
3	t_{PC}	Fast Page Mode Cycle Time	40	–	45	–	55	–	ns	
4	t_{PRWC}	Fast Page Mode RMW Cycle Time	95	–	100	–	115	–	ns	
5	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	8, 13
6	t_{CAC}	Access Time From $\overline{CAS}$	–	20	–	20	–	25	ns	8, 13
7	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	8, 13
8	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	8
9	t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	–	0	–	0	–	ns	8
10	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	9
11	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	7
12	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	50	–	60	–	ns	
13	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	200K	70	200K	80	200K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
17	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
18	t_{RCD}	$\overline{RAS}$ to CAS Delay Time	20	40	20	55	20	55	ns	13
19	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	14
20	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
21	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
22	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
23	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
24	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
25	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
26	t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
27	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
28	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
29	t_{RCH}	Read Command Hold Time	0	–	0	–	0	–	ns	10
30	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	10
31	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
32	t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
33	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
34	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
35	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
36	t_{DS}	Data Set-up Time	0	–	0	–	0	–	ns	11
37	t_{DH}	Data Hold Time	15	–	15	–	15	–	ns	11
38	t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
39	t_{REF}	Refresh Period	–	128	–	128	–	128	ms	
40	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	12
41	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	–	50	–	55	–	ns	12
42	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	90	–	100	–	110	–	ns	12
43	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60	–	65	–	70	–	ns	12

3

#	SYMBOL	PARAMETER	HY514410AL						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
44	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
45	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	30	–	ns	
46	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
47	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	30	–	35	–	40	–	ns	
48	t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	10	–	ns	
49	t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	–	20	ns	
50	t_{OED}	$\overline{OE}$ to Data Delay	20	–	20	–	20	–	ns	
51	t_{OEZ}	Output Buffer Turn-off Delay Time from $\overline{OE}$	0	20	0	20	0	20	ns	
52	t_{OEH}	$\overline{OE}$ Command Hold Time	20	–	20	–	20	–	ns	
53	t_{WTS}	Write Command Set-up Time(Test Mode In)	10	–	10	–	10	–	ns	
54	t_{WTH}	Write Command Hold Time(Test Mode In)	10	–	10	–	10	–	ns	
55	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
56	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

AC CHARACTERISTICS IN THE TEST MODE Note : 15

#	SYMBOL	PARAMETER	HY514410AL						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
57	t_{RC}	Random Read or Write Cycle Time	125	–	135	–	155	–	ns	
58	t_{RWC}	Read-Modify-Write Cycle Time	180	–	190	–	215	–	ns	
59	t_{PC}	Fast Page Mode Cycle Time	45	–	50	–	60	–	ns	
60	t_{PRWC}	Fast Page Mode RMW Cycle Time	100	–	105	–	120	–	ns	
61	t_{RAC}	Access Time from $\overline{RAS}$	–	65	–	75	–	85	ns	8, 13
62	t_{CAC}	Access Time from $\overline{CAS}$	–	25	–	25	–	30	ns	8, 13
63	t_{AA}	Access Time from Column Address	–	35	–	40	–	45	ns	8, 13
64	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	45	–	55	ns	8
65	t_{RAS}	$\overline{RAS}$ Pulse Width	65	10K	75	10K	85	10K	ns	
66	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	65	200K	75	200K	85	200K	ns	
67	t_{RSH}	$\overline{RAS}$ Hold Time	25	–	25	–	30	–	ns	
68	t_{CSH}	$\overline{CAS}$ Hold Time	65	–	75	–	85	–	ns	
69	t_{CAS}	$\overline{CAS}$ Pulse Width	25	10K	25	10K	30	10K	ns	
70	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	45	–	ns	
71	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	55	–	55	–	60	–	ns	12
72	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	95	–	105	–	115	–	ns	12
73	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65	–	70	–	75	–	ns	12
74	t_{OEA}	$\overline{OE}$ Access Time	–	25	–	25	–	25	ns	
75	t_{OED}	$\overline{OE}$ to Data Delay	25	–	25	–	25	–	ns	
76	t_{OEH}	$\overline{OE}$ Command Hold Time	25	–	25	–	25	–	ns	

AC CHARACTERISTICS IN THE WRITE PER BIT MODE

#	SYMBOL	PARAMETER	HY514410AL						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
77	t_{WBS}	Write Per Bit Set-Up Time	0	–	0	–	0	–	ns	
78	t_{WBH}	Write Per Bit Hold Time	10	–	10	–	10	–	ns	
79	t_{WDS}	Write Per Bit Selection Set-Up Time	0	–	0	–	0	–	ns	
80	t_{WDH}	Write Per Bit Selection Hold Time	10	–	10	–	10	–	ns	

NOTES :

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6}, I_{CC7} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. It depends on user whether column address is changed or not at least once while $\overline{RAS}=V_{IL}$ and $\overline{CAS}=V_{IH}$.
5. Only t_{RAS}(max.)=1μs is applied to refresh of battery back up but t_{RAS}(max.)=10μs is applied to normal functional operating.
6. AC measurements assume t_T=5ns.
7. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Measured with a load equivalent to 2 TTL loads and 100pF.
9. t_{OFF}(max.) and t_{OEZ} define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-modify-write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle : If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.) and $t_{AWD} \geq t_{AWD}$(min.) the cycle is a read-modify-write cycle and data out will contain data read from the selected cell : If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
13. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
14. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
15. These specifications are applied to the test mode.

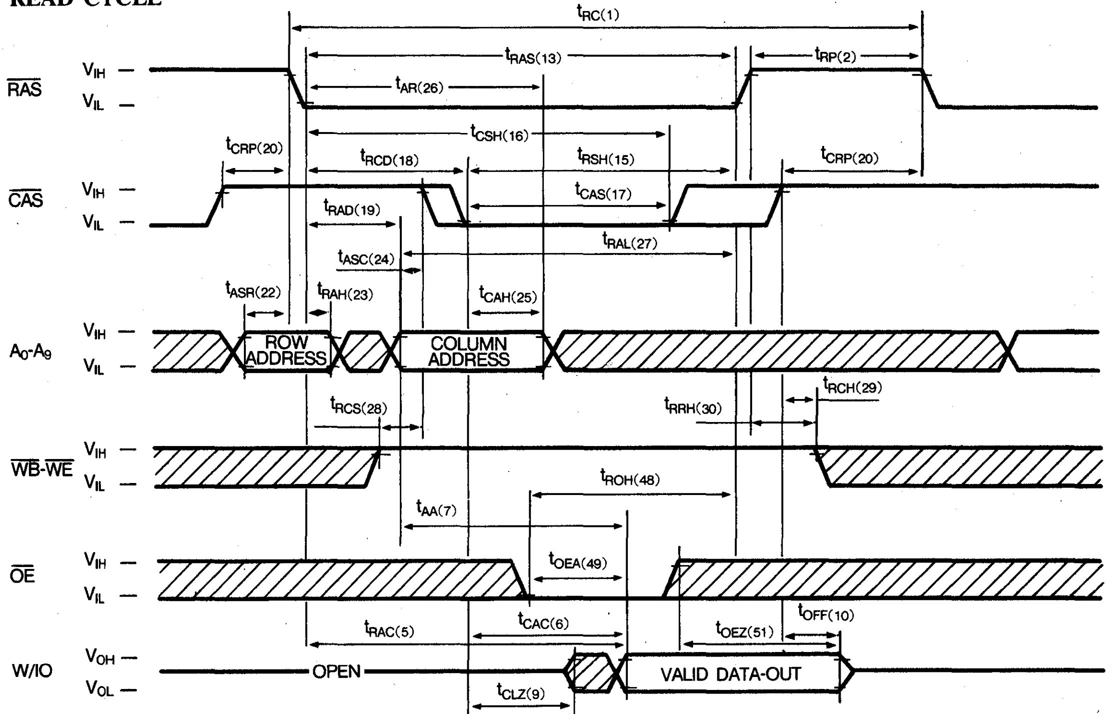
CAPACITANCE
(T_A=0°C to 70°C, V_{DD}=5V± 10%, f=1MHz)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_9, Data In)	–	5	pF
C_{IN2}	Input Capacitance($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	–	7	pF
C_{OUT}	Output Capacitance(Data Out)	–	7	pF

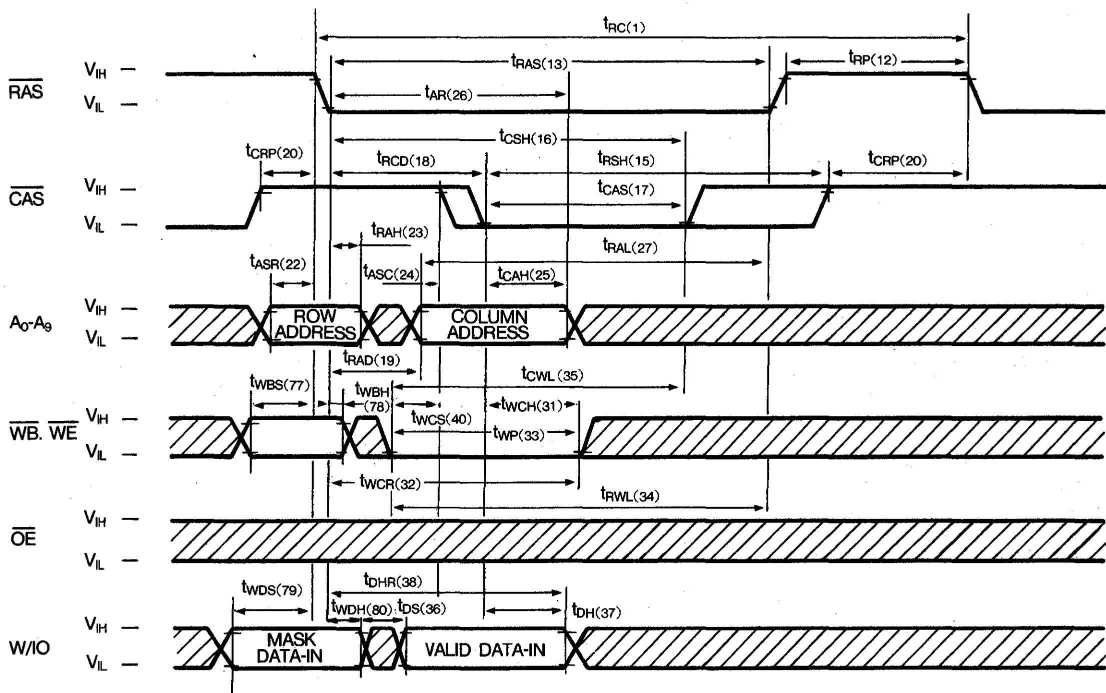
3

TIMING DIAGRAM

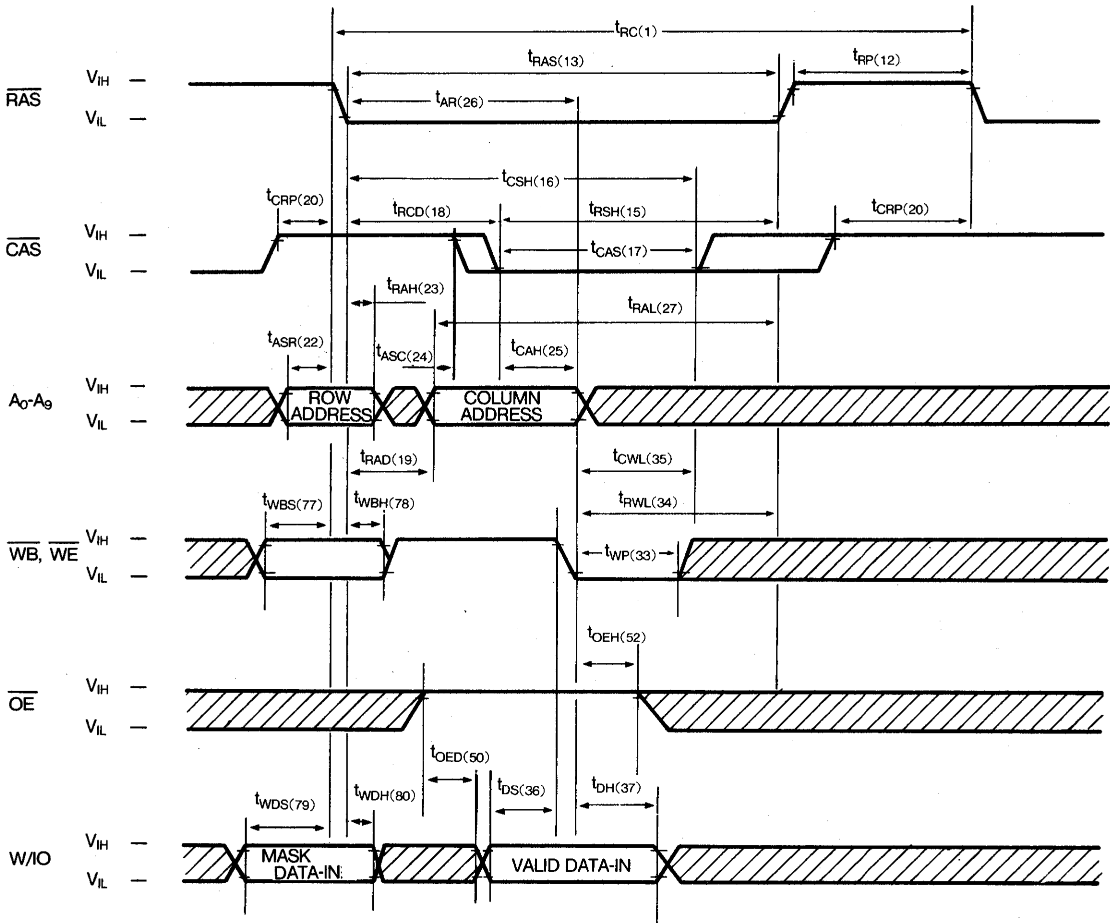
READ CYCLE



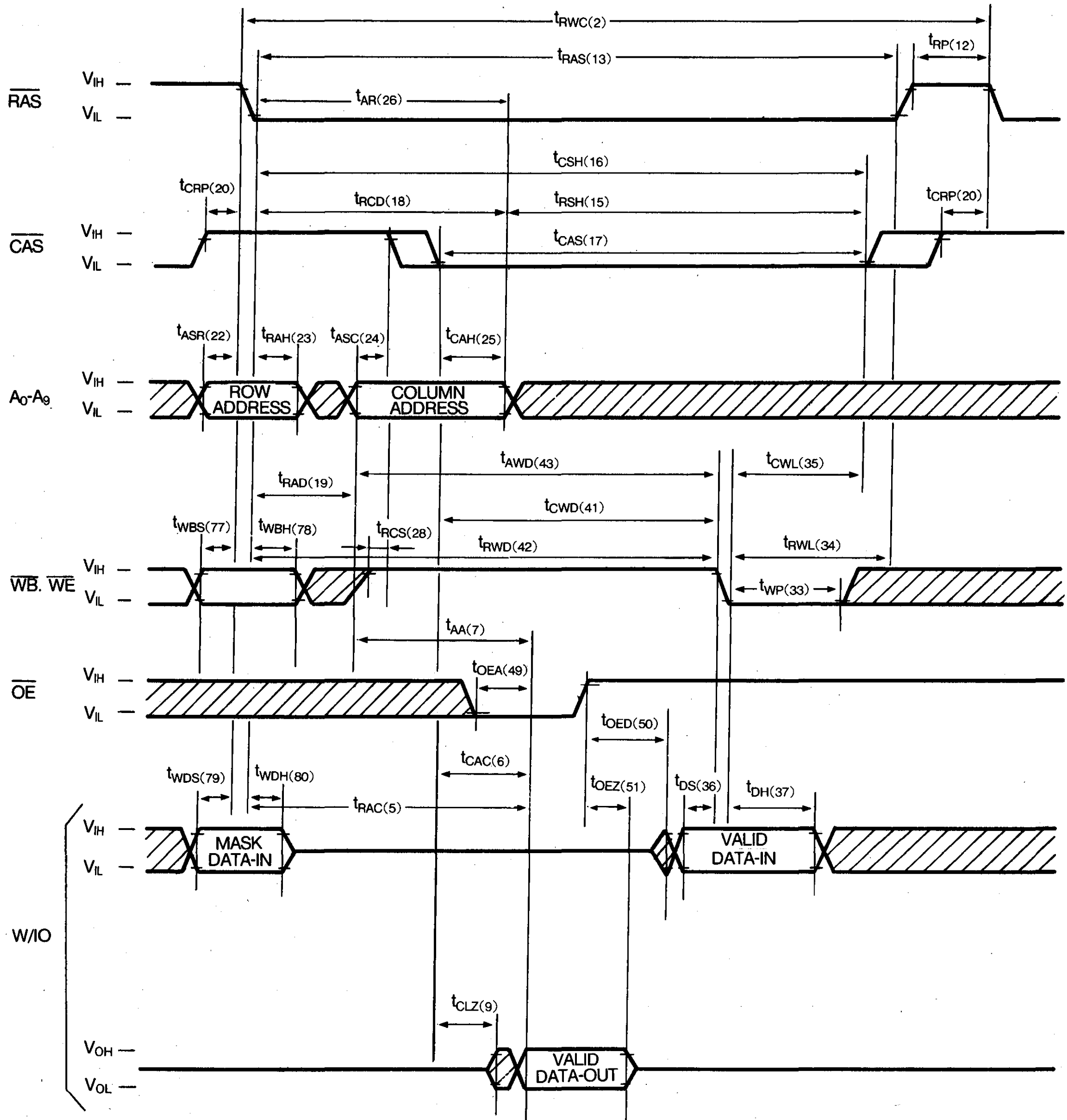
WRITE CYCLE (EARLY WRITE)



WRITE CYCLE (OE CONTROLLED WRITE)



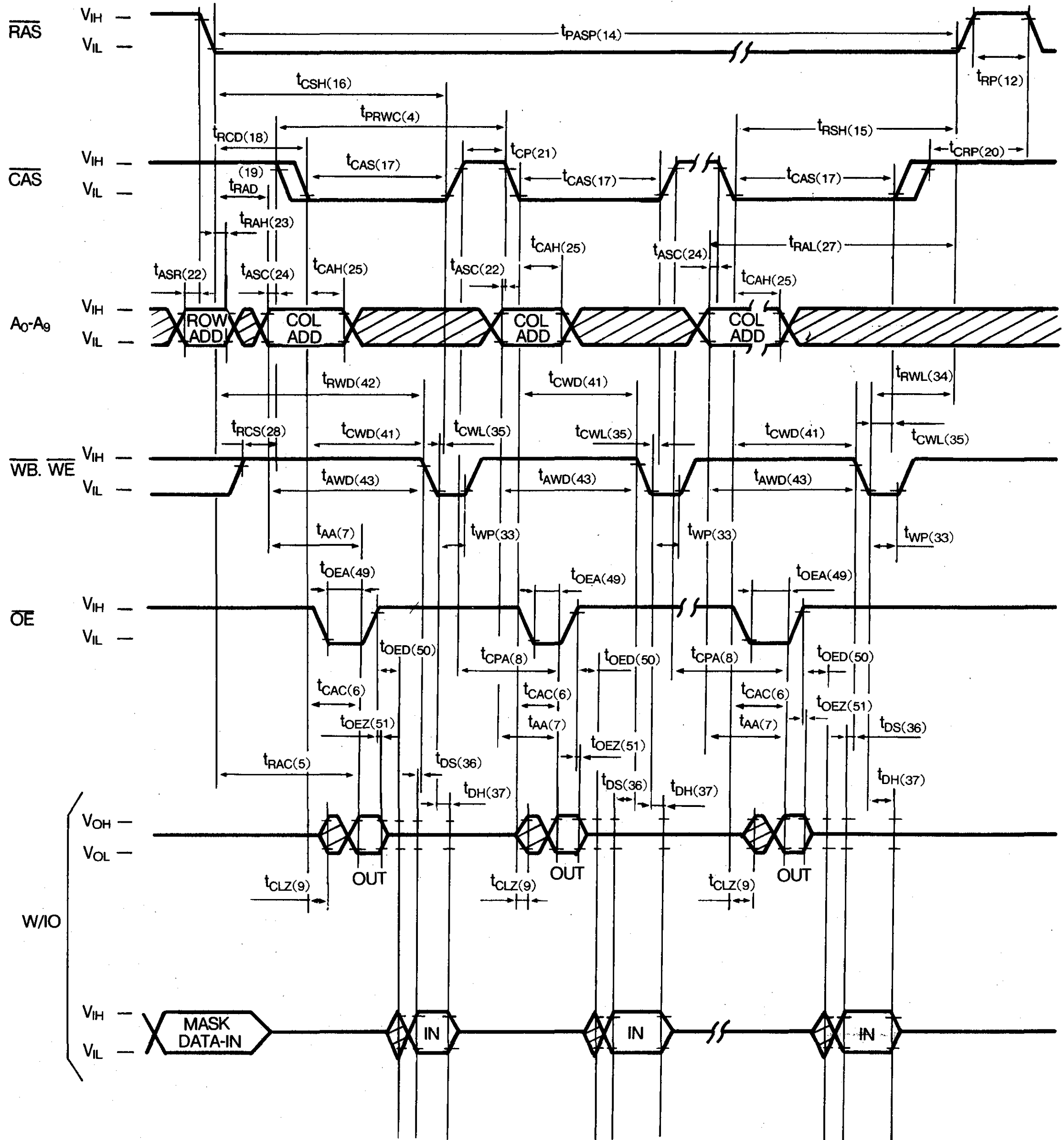
READ-MODIFY-WRITE CYCLE



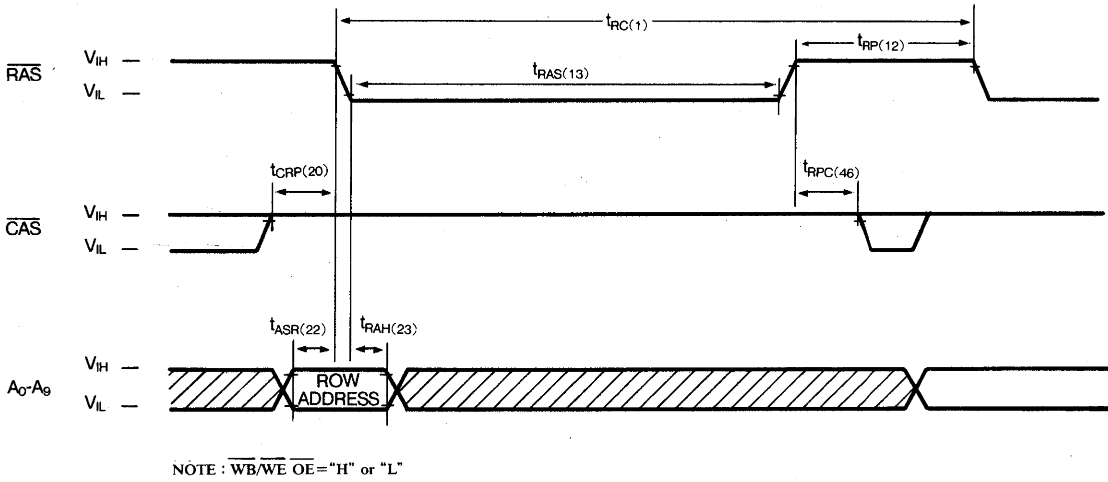
FAST PAGE MODE READ CYCLE

FAST PAGE MODE WRITE CYCLE

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

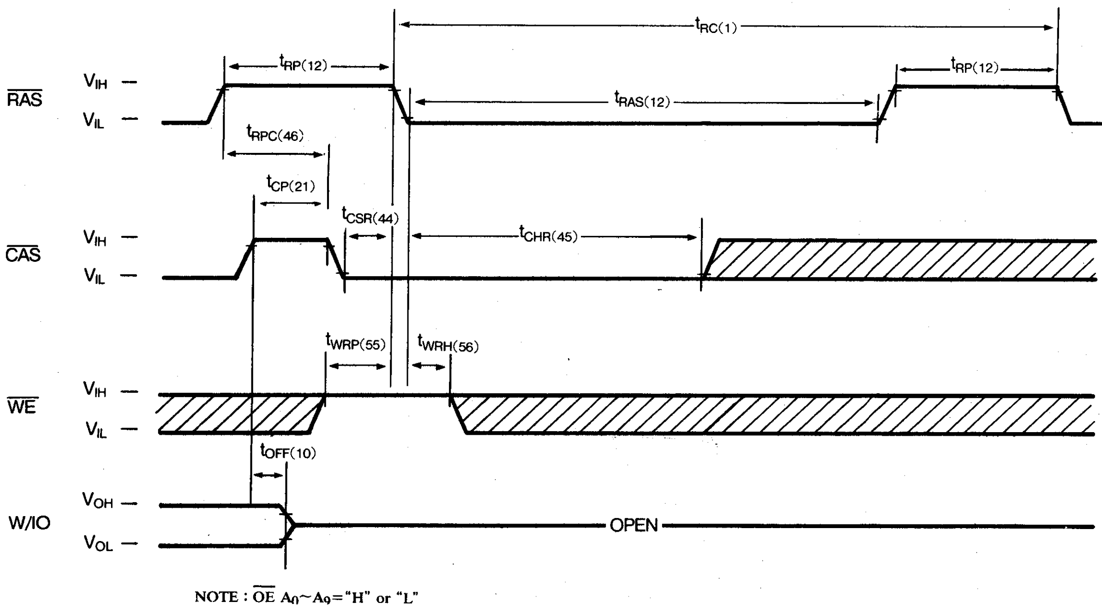


RAS-ONLY REFRESH CYCLE



NOTE : WB/WE OE="H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE



NOTE : OE A0~A9="H" or "L"

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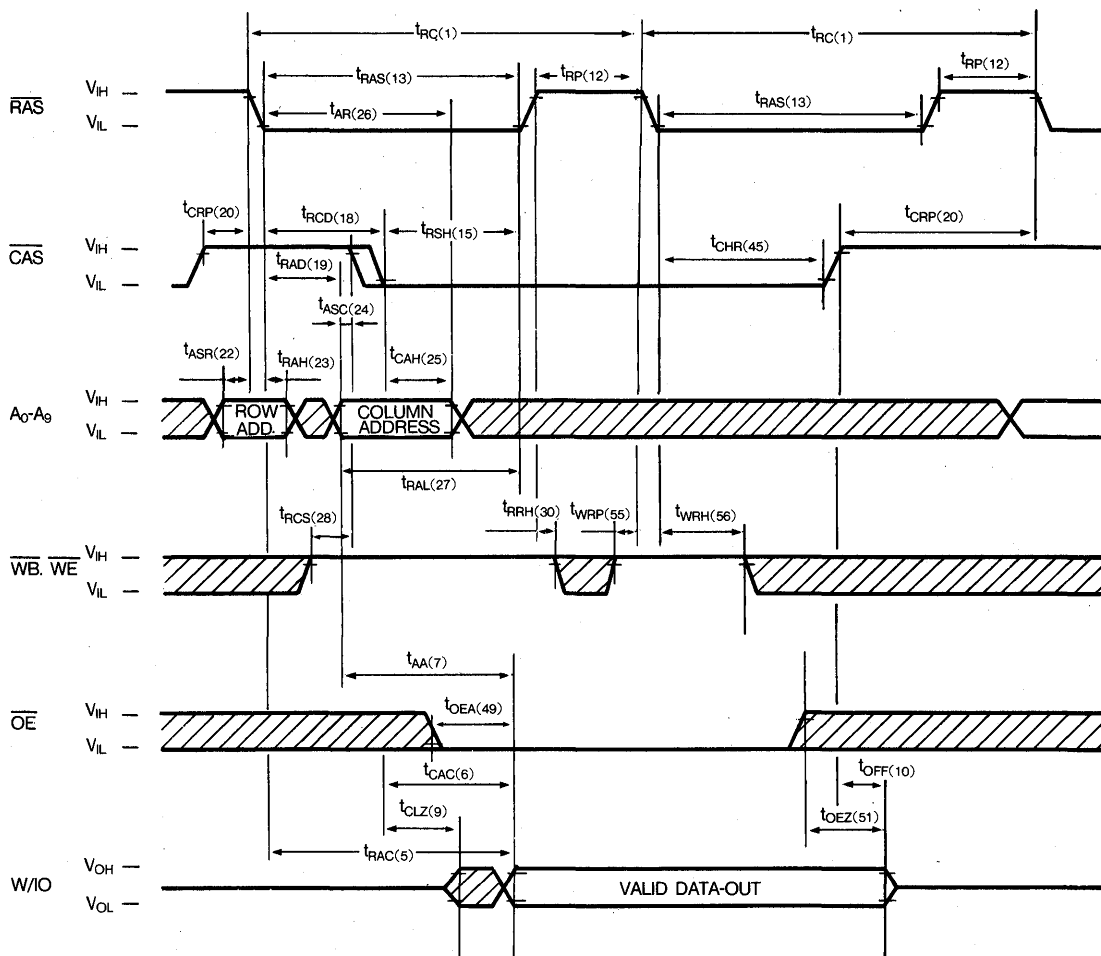
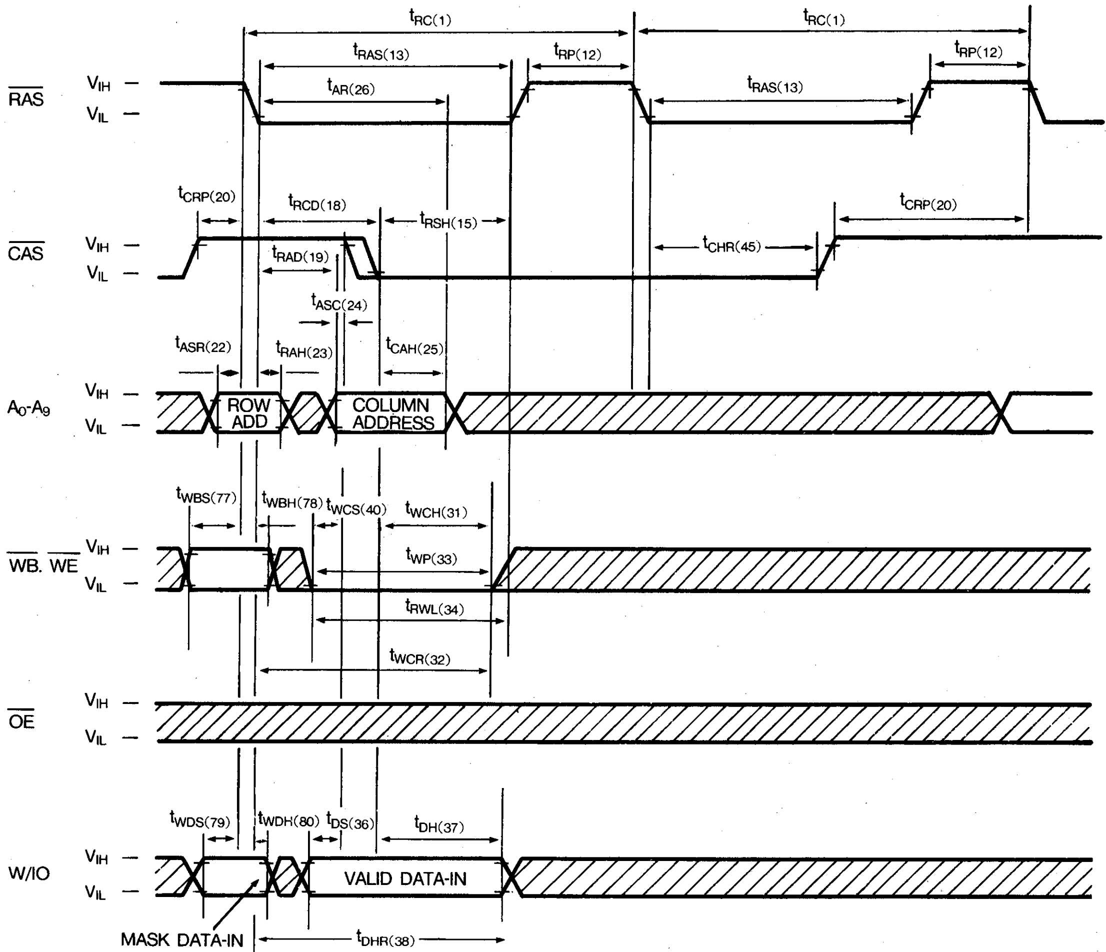
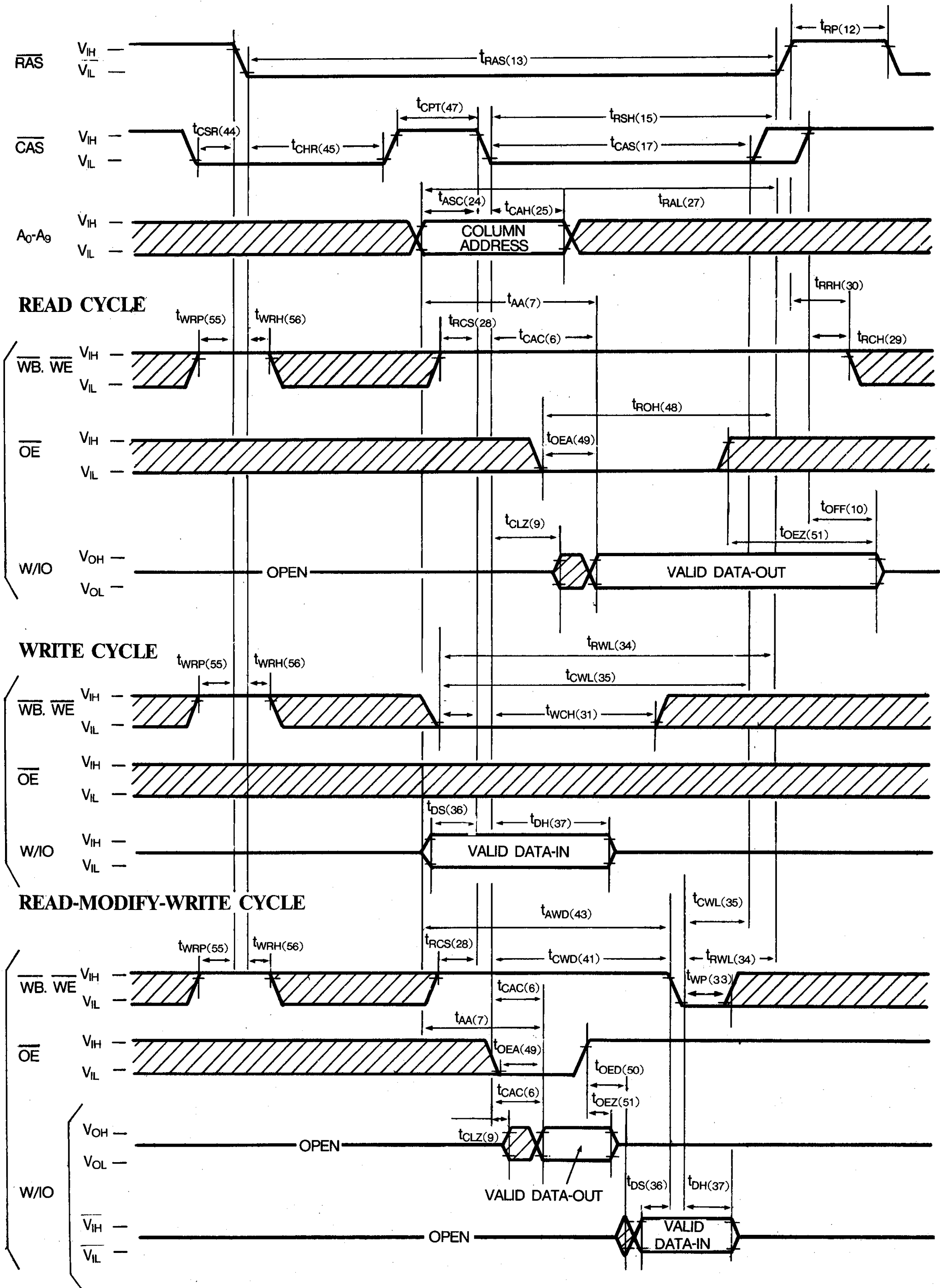
HIDDEN REFRESH CYCLE(READ)



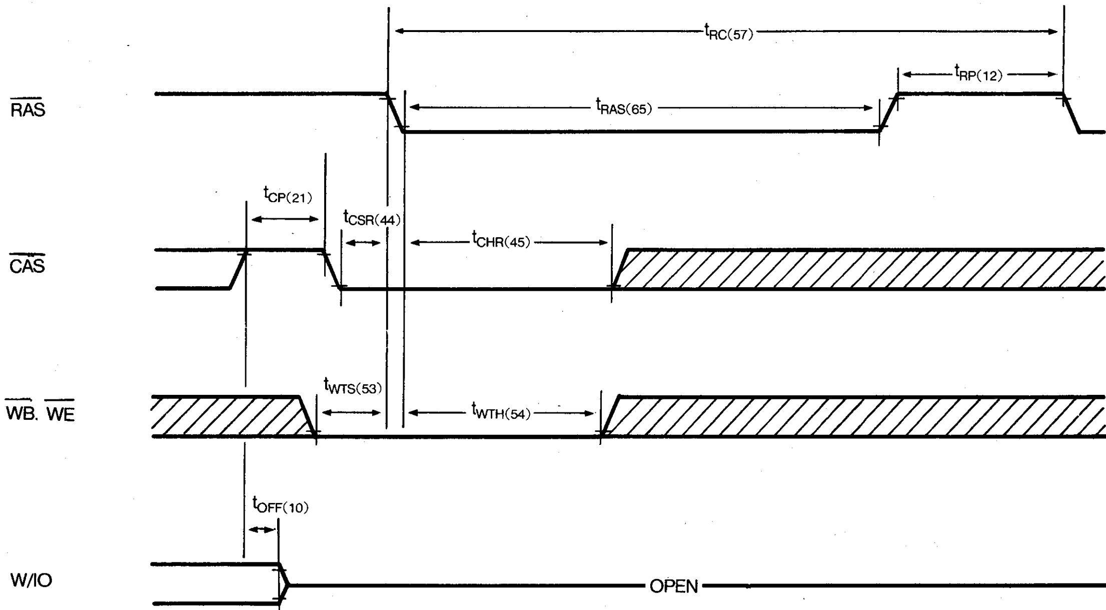
HIDDEN REFRESH CYCLE(WRITE)



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



TEST MODE IN CYCLE



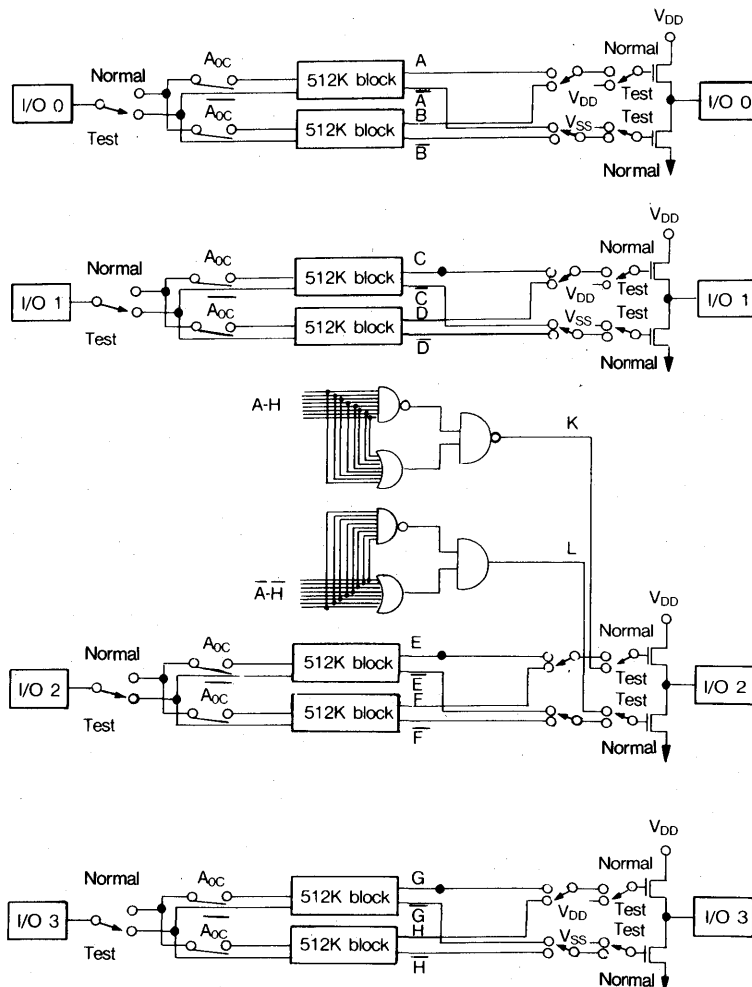
NOTE : OE, A_0~A_9="H" or "L"

TEST MODE

The HY514410AL is a DRAM organized 1,048,576 words by 4 bits and it is internally organized 524,288 words by 8 bits. In Test Mode, data are written into 8 sectors in parallel and retrieved the same way. A_{0C} is not used. If, upon reading, the 8 bits are equal(all 0s or 1s), the I/O pin indicates 1. If they were not equal, the I/O pin indicates 0. The following figure shows the block diagram of HY514410AL. In Test Mode, 1M×4 DRAM can be tested as if it were a 512K×8 DRAM.

$\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle puts the device into Test Mode. And $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle or $\overline{RAS}$-Only Refresh Cycle puts it back into Normal Mode. In Test Mode, $\overline{WE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle performs the refresh operation with the internal refresh address couter. The Test Mode function reduces test time to one-second in case of N test pattern.

BLOCK DIAGRAM IN TEST MODE



WRITE-PER-BIT FUNCTION

The write-per-bit function selectively control the internal write-enable circuit of the DRAM. When $\overline{WB}/\overline{WE}$ is held 'low' at the falling edge of $\overline{RAS}$ during a random access operation, the write-mask is enabled. At the sametime, the mask data on the W_I/IO_I pins is latched onto the write-mask register (WMR). When a '0' is sensed on any of the W_I/IO_I pins, their corresponding write circuits are disabled and new data will not be written.

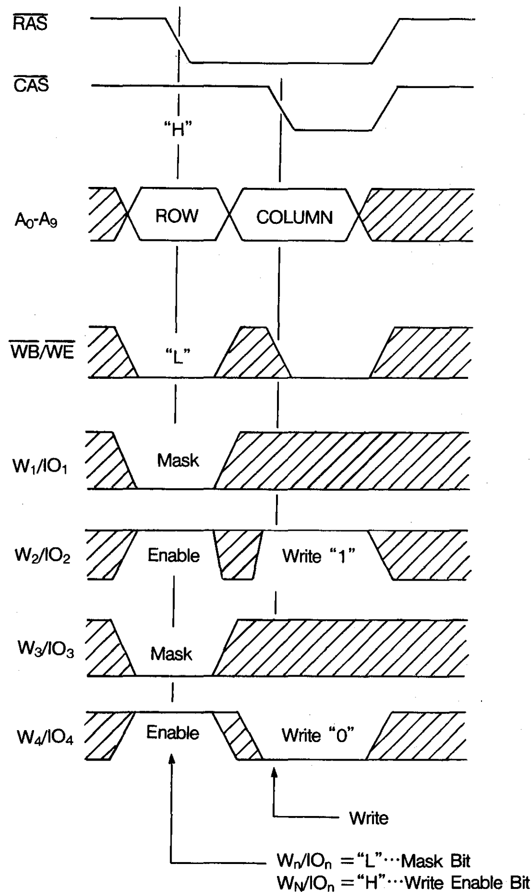
When '1" is sensed on any of the $\overline{W_I/IO_I}$ pins, their corresponding write circuit will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in table 1.

Table1 : Truth table for write-per-bit function

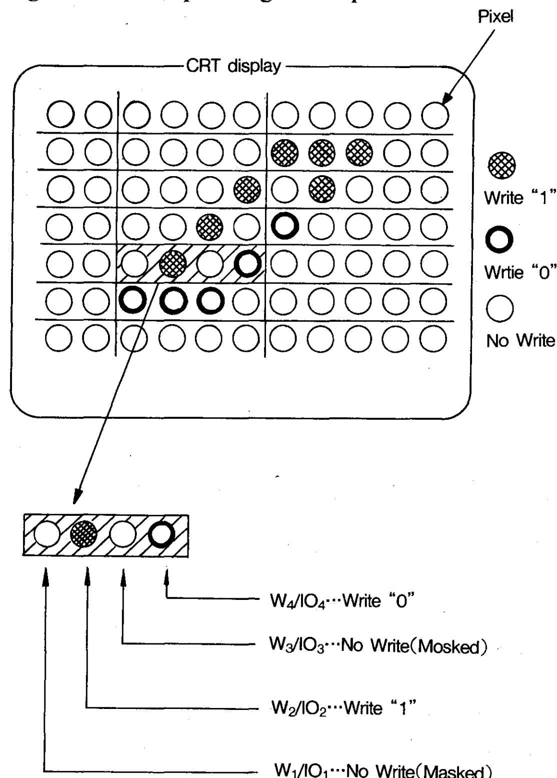
At the falling edge of $\overline{RAS}$				Function
$\overline{CAS}$	$\overline{OE}$	$\overline{WB}/\overline{WE}$	$W_i/IO_i(i=1\sim4)$	
H	H	H	•	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

An example of the write-per-bit function illustrating its application to displays is shown in Fig−1 and Fig-2.

Fig-1. : Write-per-bit timing cycle



Fig−2. : Corresponding bit-map



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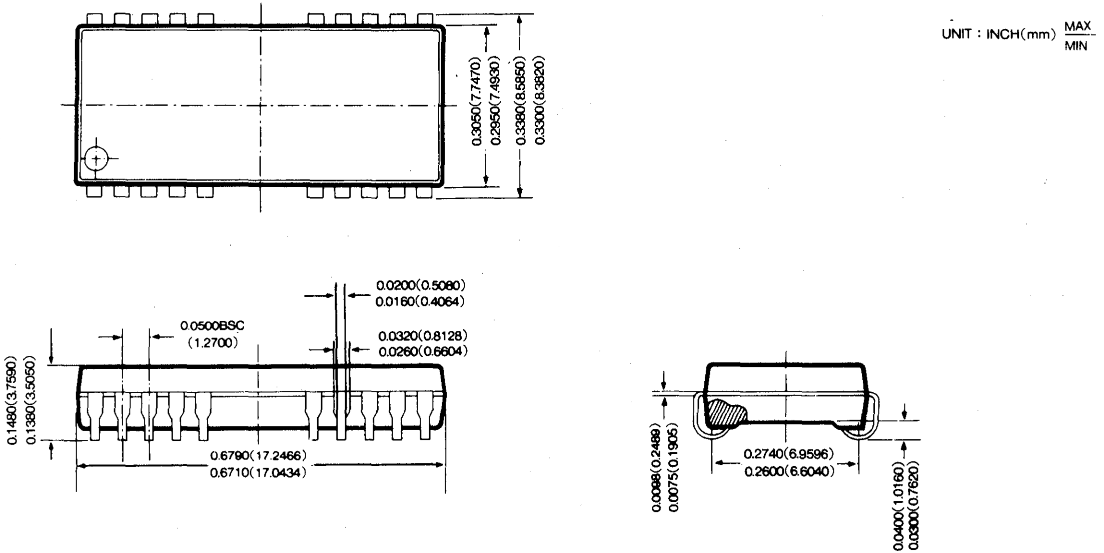
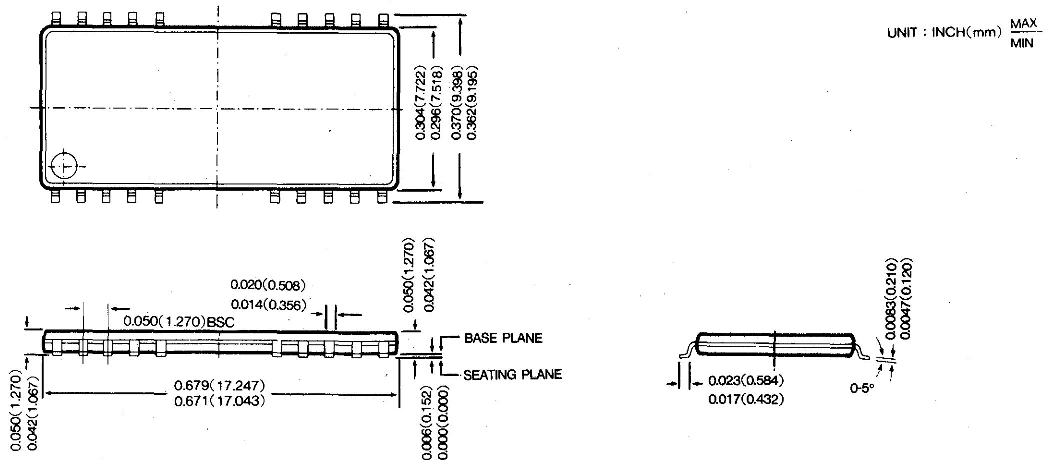
PACKAGE INFORMATION

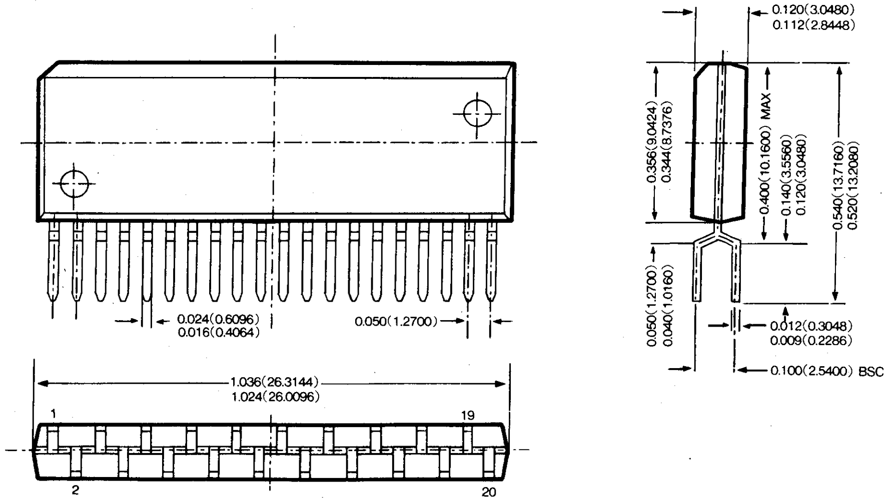
- **20/26 PIN SMALL OUTLINE J-FORM PACKAGE −300 MIL**



- **20/26 PIN THIN SMALL OUTLINE PACKAGE−300 MIL**



• **20 PIN ZIGZAG-IN-LINE PACKAGE-400 MIL**



MEMO

HYUNDAI SEMICONDUCTOR

HY524800

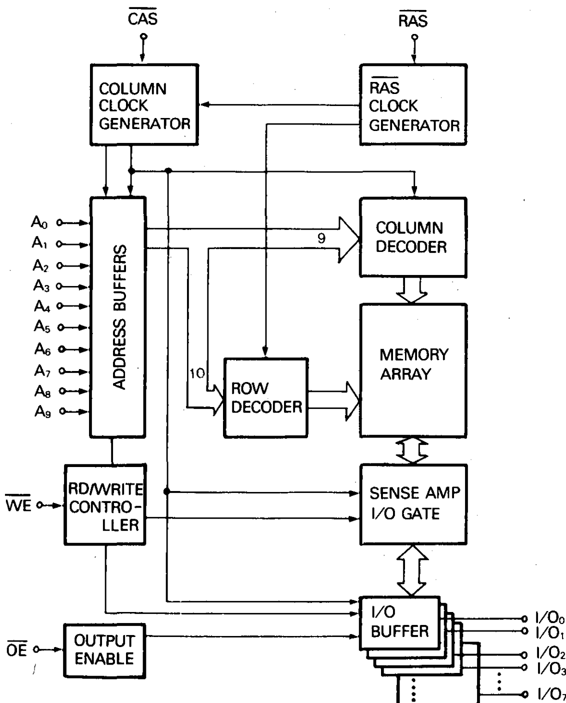
512K×8-Bit CMOS DRAM

M1B1201A-NOV91

DESCRIPTION

The HY524800 is the new generation dynamic RAM organized 524,288 words by 8 bits. The HY524800 utilizes CMOS process technology as well as advanced circuit techniques to provide wide operating margins. Multiplexed address inputs permit the HY524800 to be packaged in a 350mil 28 pin plastic SOJ.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented feature include single power supply of 5V±10% tolerance direct interfacing capability with high performance logic families such as Schottky TTL.



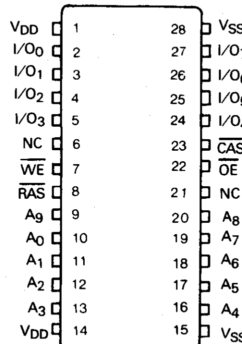
* Column address($A_0 \sim A_8$) is trapped in colun. address buffer at $\overline{CAS}$ falling edge.

FEATURES

- **Low power dissipation**
  - **Operating Current, 80 ns : 115mA(max.)**
  - **TTL Standby Current : 2mA(max.)**
  - **CMOS Standby Current : 1mA(max.)**
- **Read-Modify-Write Capability**
- **$\overline{RAS}$-only, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Capability**
- **Common I/O capability**
- **Fast Page mode capability**
- **1024 refresh cycles/16 ms**
- **High reliability 350 mil 28 pin SOJ**
- **Fast access time and cycle time (ns)**

	HY524800-70	HY524800-80
Max $\overline{RAS}$ Access Time, t_{RAC}	70	80
Max $\overline{CAS}$ Access Time, t_{CAC}	20	20
Min Fast Page Mode Cycle Time, t_{PC}	45	50
Min Cycle Time, t_{RC}	130	150

PIN CONNECTUINS



PIN NAMES

$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
A_0-A_9	ADDRESS INPUT
I/O_0-I/O_7	DATA INPUT/OUTPUT
V_{DD}	POWER(+5V)
V_{SS}	GROUND

3

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature	−55 to 125	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−0.7 to V_{DD}	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−0.5 to 6.5	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	1.0	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input Hight Voltage	2.4	–	V_{DD}	V
V_{IL}	Input Low Voltage	0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HY524800		UNIT	NOTE
				MIN.	MAX.		
$\vert I_{LI}\vert$	Input Leakage Current(any input pin)	0V ≤ V_{IN} ≤ 6.0V, All other pin not under test=V_{SS}		–	10	μA	
$\vert I_{LO}\vert$	Output Leakage Current for High Impedance State	D_{OUT} is disable, 0V ≤ V_{OUT} ≤ 5.5V		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$\overline{RAS}$, $\overline{CAS}$, Address cycling, t_{RC}=t_{RC}(min.)	70	–	135	mA	1, 2
			80	–	115		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$=$\overline{CAS}$=V_{IH}		–	2	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH}, t_{RC}=t_{RC}(min.)	70	–	135	mA	2
			80	–	115		
I_{DD4}	V_{DD} Supply Current, Fast page mode	$\overline{RAS}$=V_{IL}, Address cycling, t_{PC}=t_{PC}(min.)	70	–	65	mA	1, 2
			80	–	55		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}$=$\overline{CAS}$=V_{DD}−0.2V		–	1	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{RC}(min.)	70	–	135	mA	2
			80	–	115		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTES :
1. I_{DD1} and I_{DD4} depend on output loading, specified values are obtained with the output open.
2. I_{DD1}, I_{DD3}, I_{DD4} and I_{DD6} depend on cycle rate.

AC CHARACTERISTICS

(T_a=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted). NOTES : 1, 2, 3

SYMBOL	PARAMETER	HY524800				UNIT	NOTES
		70		80			
		MIN.	MAX.	MIN.	MAX.		
t_{RC}	Random Read or Write Cycle Time	130	128K	150	128K	ns	1,2
t_{RWC}	Read-Modify-Write Cycle Time	180	128	205	128	ns	1,2,10
t_{PC}	Fast Page Mode Cycle Time	45	–	50	–	ns	2
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	90	–	100	–	ns	2, 12
t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	ns	3, 4, 5
t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	ns	3, 4, 5
t_{AA}	Access Time from Column Address	–	35	–	40	ns	4, 5
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	40	–	45	ns	5
t_{OFF}	Output Buffer Turn-off Delay	0	15	0	15	ns	7
t_T	Transition Time(Rise and Fall)	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	16	80	16	ns	1, 2
t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Read-Modify-Write)	120	16	135	16	ns	1, 2, 10
t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	–	20	–	ns	
t_{CASP}	$\overline{CAS}$ Pulse Width(Fast Page Read-Modify-Write)	70	–	75	–	ns	10
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	60	ns	3
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	–	15	–	ns	6
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	–	10	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	ns	9
t_{ASR}	Row Address Set-up Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	10	–	10	–	ns	
t_{ASC}	Column Address Set-up Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	15	–	15	–	ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50	–	55	–	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	ns	
t_{RCS}	Read Command Set-up Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time	0	–	0	–	ns	
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	–	0	–	ns	
t_{WCH}	Write Command Hold Time	15	–	15	–	ns	
t_{WP}	Write Command Pulse Width	15	–	15	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	ns	
t_{DS}	Data Set-up Time	0	–	0	–	ns	8
t_{DH}	Data Hold Time	15	–	15	–	ns	8
t_{REF}	Refresh Period	–	16	–	16	ms	
t_{WCS}	Write Command Set-up Time	0	–	0	–	ns	
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	–	50	–	ns	10
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	95	–	110	–	ns	10
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60	–	70	–	ns	10

SYMBOL	PARAMETER	HY524800				UNIT	NOTES
		70		80			
		MIN.	MAX.	MIN.	MAX.		
t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	ns	9
t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	ns	
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	–	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	20	–	20	ns	4, 5
t_{OED}	$\overline{OE}$ to Data Delay	15	–	15	–	ns	
t_{OEZ}	Output Buffer Turn-off Delay Time from $\overline{OE}$	–	15	–	15	ns	7
t_{OEH}	$\overline{OE}$ Command Hold Time	15	–	15	–	ns	
t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5	–	5	–	ns	9
t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	ns	9

NOTEs :

1. 1024 refreshes are required every 16ms. A burst of eight consecutive refreshes are allowed to keep t_{RAS}=16μs average. A maximum of 128μs between refreshes is allowed, however 16ms retention must be met.
2. All AC timings assume $t_{T(max)}$=5ns. If the actual t_T is greater than $t_{T(max)}$, then the cycle times need to be greater than that specified by the amount each transition exceeds $t_{T(max)}$. HY524800 will support a t_T up to 50ns. The transition time is defined between the V_{IH} and V_{IL}. All timings are referenced to an V_{IL} or V_{IH}.
3. $t_{RCD(max)}$ is specified as a reference point only. If $t_{RCD} > t_{RCD(max)}$ then this parameter is increased by the amount t_{RCD} exceeds $t_{RCD(max)}$.
4. t_{RAC}, t_{CAC}, t_{AA} and t_{OEA} must be satisfied to guarantee access. Please check that all parameters are met for your application.
5. Access assumes a load equivalent to 100pF.
6. t_{RAD} is specified as a reference point only. If $t_{RAD} > t_{RAC} - t_{AA}$ then the access is increased by the difference.
7. This parameter defines the time at which the output achieves the open circuit and is not referenced to the output voltage levels.
8. Data In Set up and Holds are measured from the later of falling signal $\overline{CAS}$ or $\overline{WE}$
9. t_{CP}, t_{CSR}, t_{WRP}, t_{WRH} all need to be valid for CBR users.
10. A 5ns delta is used between Data reaching Hi Impedance and having valid Data In for these numbers.

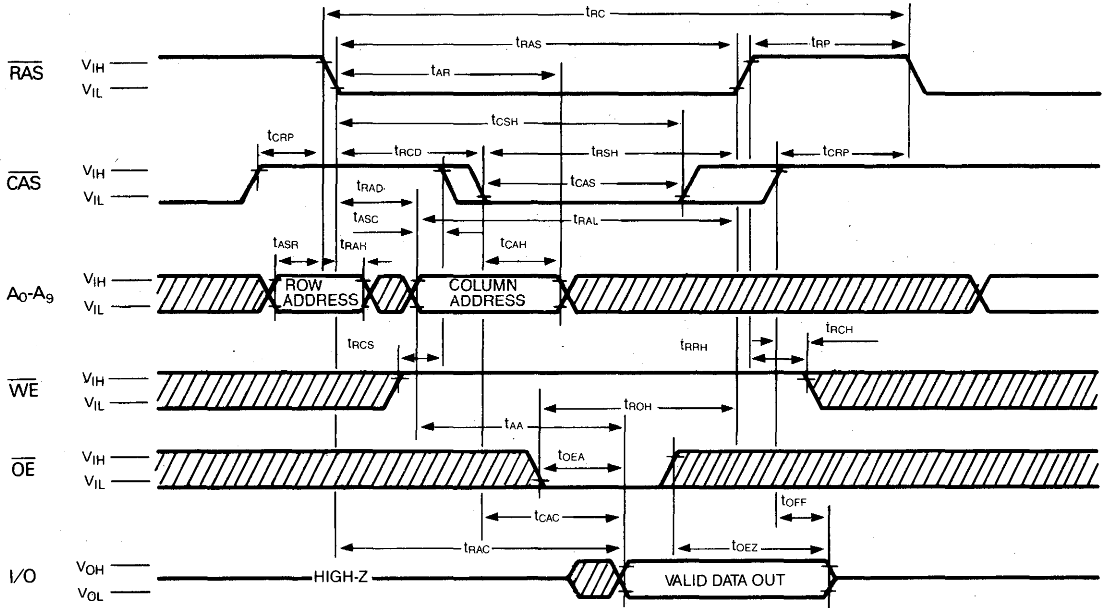
CAPACITANCE

(T_A=0,C to 70,C, V_{DD}=5V± 10%, f=1MHz)

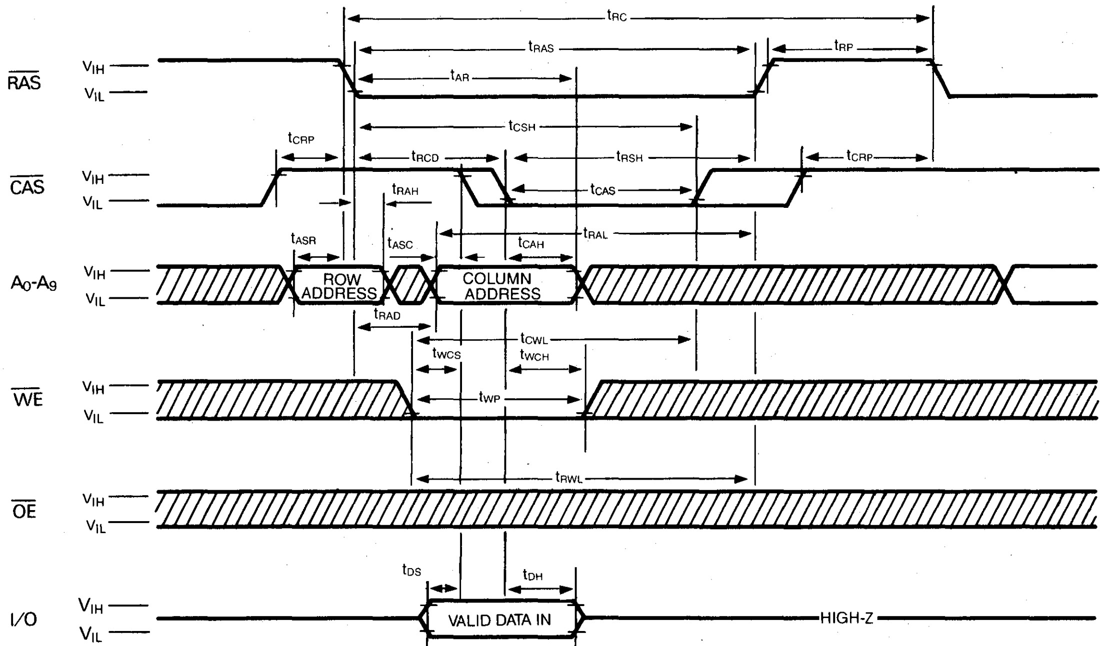
SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C_{IN1}	Input Capacitance (A_0-A_9)	–	5	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	–	5	pF
$C_{I/O}$	Input/Output Capacitance(Data Input/Data Output)	–	8	pF

TIMING DIAGRAM

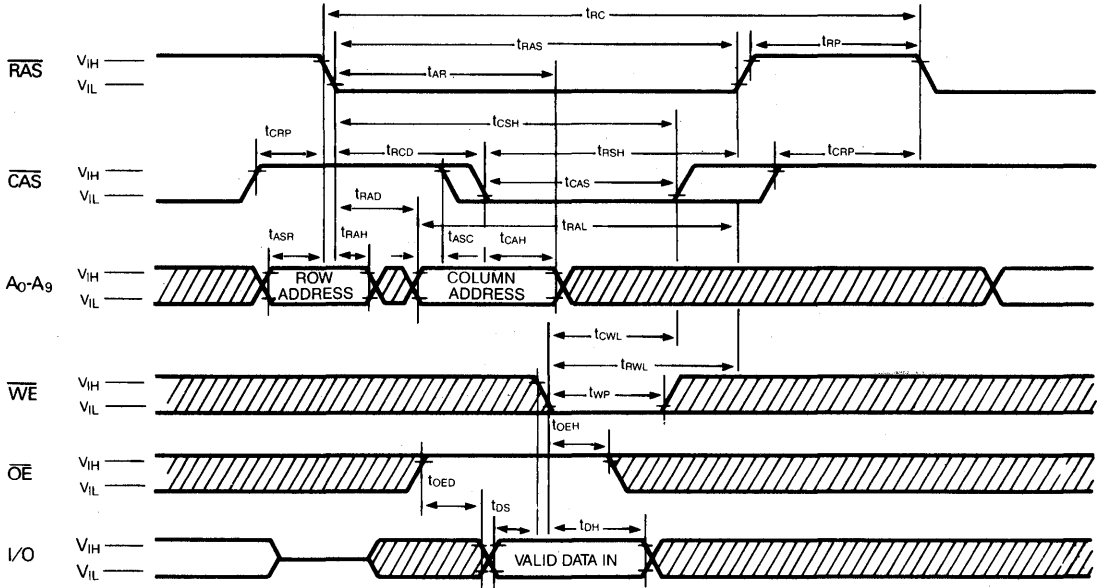
READ CYCLE



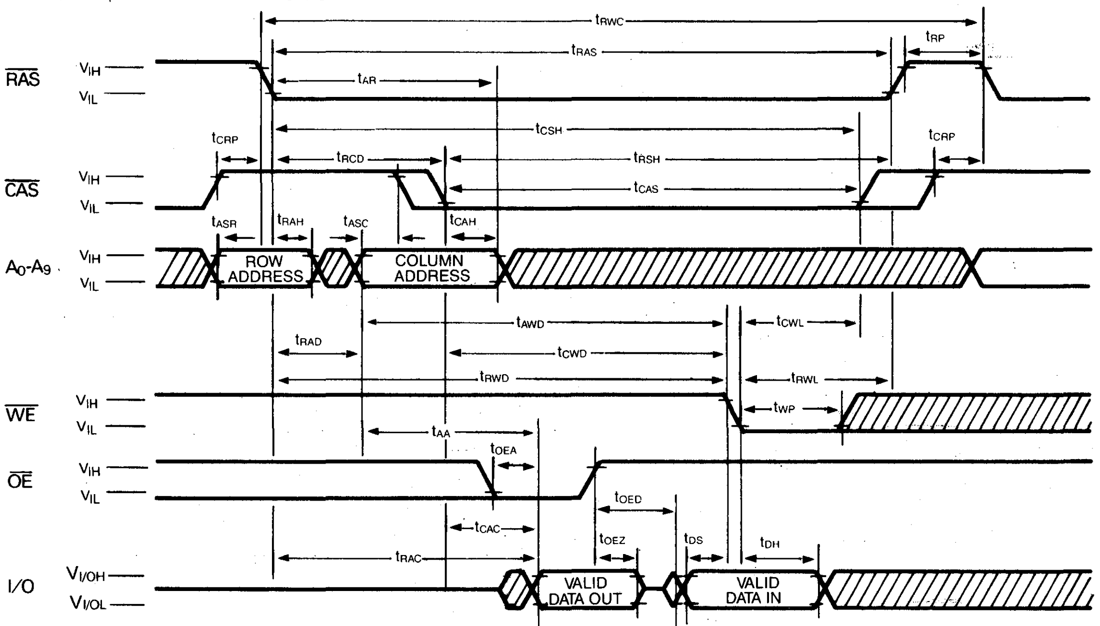
WRITE CYCLE



WRITE CYCLE (OE CONTROLLED WRITE)



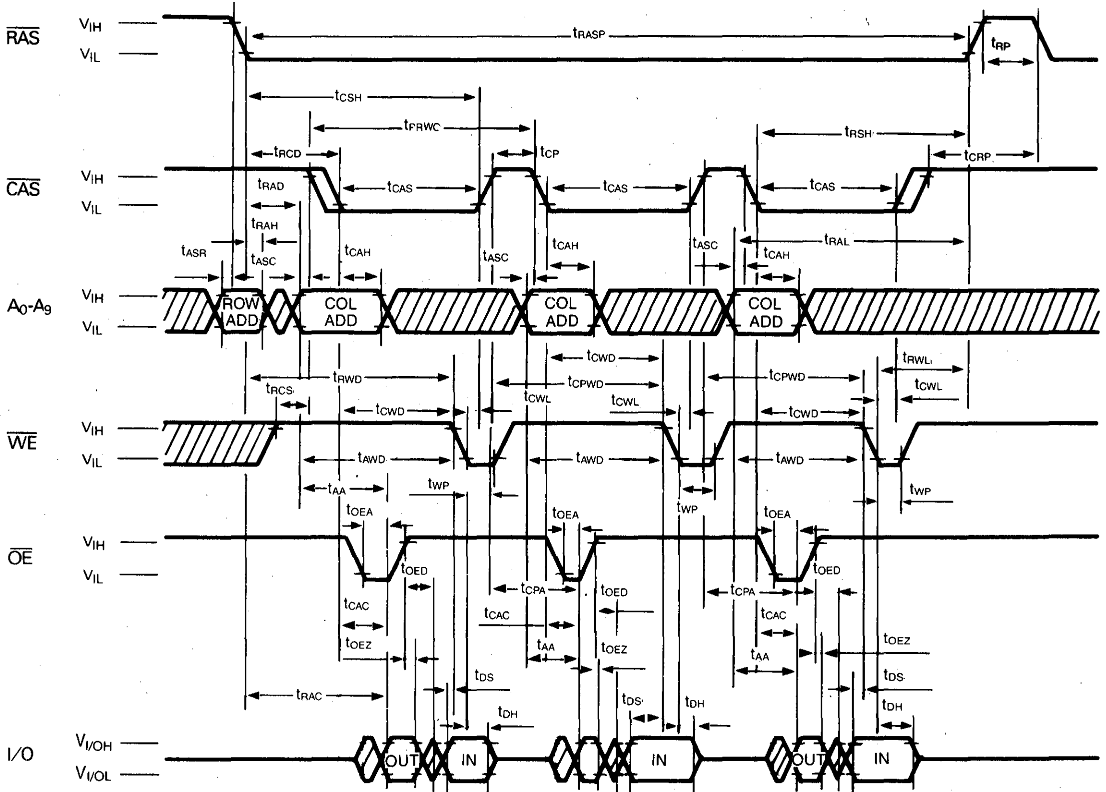
READ-MODIFY-WRITE CYCLE



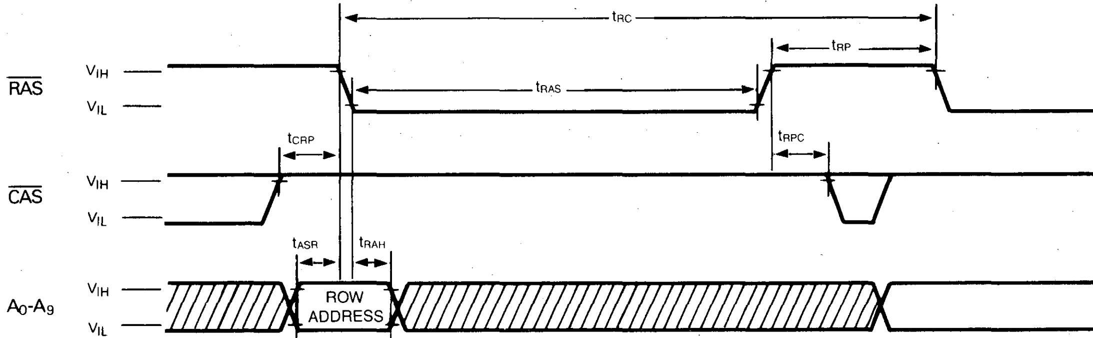
FAST PAGE MODE READ CYCLE

FAST PAGE MODE WRITE CYCLE

FAST PAGE MODE READ-MODIFY-WRITE CYCLE

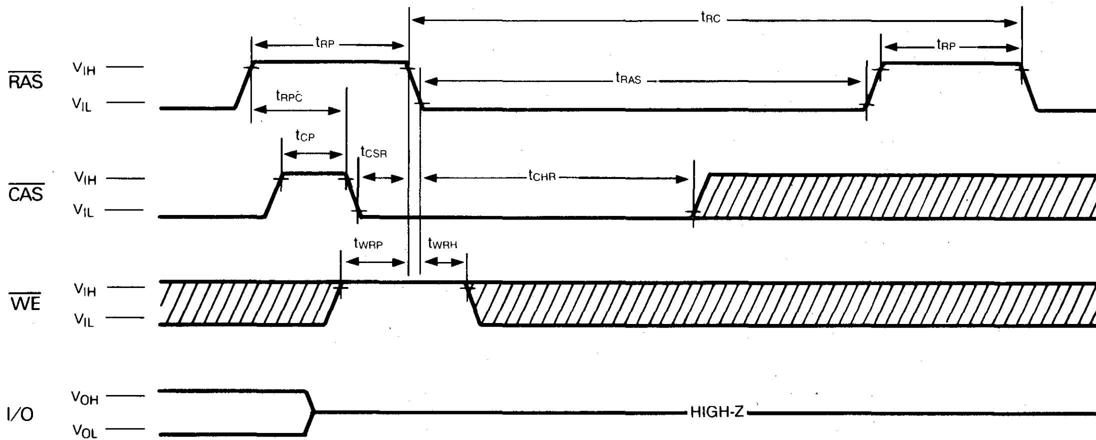


$\overline{RAS}$-ONLY REFRESH CYCLE



NOTE : $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



NOTE : $\overline{OE}$ and A_0-A_9 : "H" or "L"

DEVICE OPERATION

POWER ON/INITIALIZATION/POWER OFF

After V_{CC} stabilizes, a pause of at least 500 microseconds is required before initialization begin. During this interval, $\overline{RAS}$ must be inactive($>V_{IH}$). a minimum of 8 cycles are required to initialized the device. these must be either $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, whose t_{RP} must be greater than 70ns. After the initialization cycles the device is ready for normal use.

PAGE MODE OPERATION

The industy standard Page Mode for $\overline{CAS}$-Before-$\overline{RAS}$ and $\overline{RAS}$-Only REfresh, Early-and Late-Write, Read and Read-Modify-Write cycles are supported.

ADDRESS CONTROL

The Row Address is trapped with the falling edge of $\overline{RAS}$, which is common for all modes of operation. This selects the word line to be used during the $\overline{RAS}$ cycle. The W/L selected cannot be changed without $\overline{RAS}$ going inactive.

The Column Address($A_0 \sim A_8$) is trapped with the falling edge of $\overline{CAS}$, for both the Read and Write operations. Each falling $\overline{CAS}$ allows a new Read or Write operation to occur on a selected new bit address on the same W/L. $\overline{CAS}$ cycles may continue with new random addresses trapped each time $\overline{CAS}$ falls, up to the limit of the $\overline{RAS}$ active time$-t_{RAS}$.

The $\overline{CAS}$ pulse must rise past the V_{IH} value and remain at a Hi level for a specified time. Only one Write operation can occur while $\overline{CAS}$ is Lo.

The device's access is impacted by active $\overline{RAS}$, active $\overline{CAS}$, active $\overline{OE}$, as well as valid address and inactive $\overline{CAS}$. All conditions must be met in order to have a valid access. Therfore the Set Up time for column address may impact the device's access.

READ/WRITE CONTROL

The state of the $\overline{WE}$ pin at $\overline{CAS}$ fall time determines the type of cycle the device will start to do. If $\overline{WE}$ is low when $\overline{CAS}$ falls, an Early Write operation is initiated. Because the device knows that a Write operation has be initiated, the Off-Chip-Drivers will remain in high impedance for the entire $\overline{CAS}$ cycle and only allows one Write operation for each $\overline{CAS}$ cycle.

If $\overline{WE}$ is high when $\overline{CAS}$ falls, a Read operation is performed, and the $\overline{OE}$ pin will control the OCD impedance. The $\overline{OE}$ pin is independent of $\overline{CAS}$, but does have an access requirement. $\overline{CAS}$ and $\overline{WE}$ must not change state until Data Out is read.

If $\overline{WE}$ does fall while $\overline{CAS}$ is still Lo, a Read-Modify-Write or Late-Write cycle will be initiated. In this case, the $\overline{OE}$ pin will control the OCD impedance. When $\overline{WE}$ falls, it will trap Data In information for the Write operation. The $\overline{OE}$ pin must be used for this cycle to guarantee correct "hand shaking" on the I/O pin for Data Out and Data In control. Until Data Out is read and Data In is set up, Write must not go low. In this case, the Data In will be written on the same Column address which was trapped when $\overline{CAS}$ fell. $\overline{CAS}$ must remain Lo for a specified time after $\overline{WE}$ is Lo. and can not start another cycle until after a t_{RMW} cycle time has passed.

The customer can mix the above cycle types as long as all other timings are obeyed.

DATA IN CONTROL

Data In is trapped when the Write cycle is initiated. For an Early-Write operation, $\overline{CAS}$ will be the trapping signal. During a Late-Write or Read-Modify-Write operation, $\overline{WE}$ will be the trapping signal.

IMPEDANCE CONTROL

The following signals are used to control the impedance of the OCDs ; $\overline{OE}$ pin, $\overline{WE}$ pin, $\overline{RAS}$ pin, and $\overline{CAS}$ pin. All pins must be in there proper state in order to drive DATA Out.

With the $\overline{OE}$ pin hi, the OCDs are turned off and will maintain hi impedance. Thus DATA Out can be turned "off" by returning the $\overline{OE}$ pin to hi level. $\overline{OE}$ pin going lo will allow the Output Driver to be turned "on", but only if the device is doing a Read operation ($\overline{WE}$ pin hi) and both the $\overline{CAS}$ and $\overline{RAS}$ pins are still lo.

If $\overline{CAS}$ never falls($\overline{RAS}$-Only Refresh), the device will also maintain hi impedance. Data Out can be turned "off" by returning the $\overline{CAS}$ pin to hi level.

If $\overline{\text{WE}}$ is lo when $\overline{\text{CAS}}$ falls, the device will maintain hi impedance. Data Out will not be turned "off" by returning the $\overline{\text{RAS}}$ pin to a hi level, but when $\overline{\text{RAS}}$ falls to start another cycle, the device will return to a hi impedance even if $\overline{\text{CAS}}$ had remained lo. Thus hidden Refresh is not supported.

REFRESH CYCLE

Because 512K×8 is a dynamic memory(data is represented by charge stored on a capacitor), each cell must be refreshed periodically to replace charge leakage. Refreshing the entire chip requires sequencing through all 1024 row address. This must be done within each 16ms Refresh interval. Two refresh methods are provided.

A $\overline{\text{RAS}}$-Only Refresh uses a $\overline{\text{RAS}}$ select with $\overline{\text{CAS}}$ held high. The selected row address (A_0-A_9) must be provided to the device.

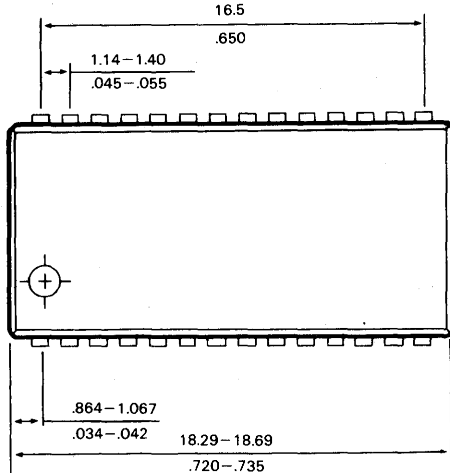
A $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh capability is also provided. If $\overline{\text{CAS}}$ is low at the time $\overline{\text{RAS}}$ is pulled low to initiate the Refresh, an on-chip Row Address Counter(RAC) will provide the next row address for the Refresh. No external addresses are used.

NOTE :
1. Refresh occurs whenever $\overline{\text{RAS}}$ is selected ; eg, Read or Write.
2. If both $\overline{\text{CAS}}$ & $\overline{\text{WE}}$ are low when $\overline{\text{RAS}}$ becomes active(low), the device will be forced into a test mode. Since some test modes may cause physical damage to the device, the above sequece is not allowed. Test modes are cleared by $\overline{\text{RAS}}$-Only and $\overline{\text{CAS}}$ Before-$\overline{\text{RAS}}$ refresh cycles.

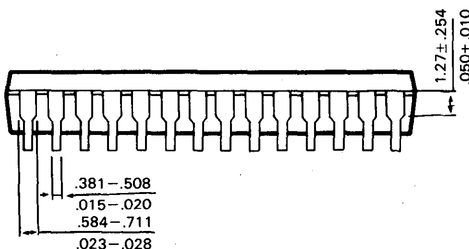
3

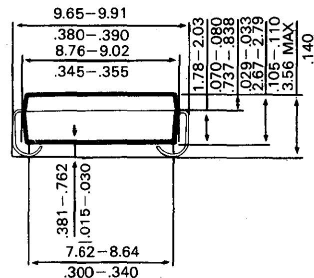
PACKAGE INFORMATION

• **28 PIN SMALL OUTLINE J-FORM PACKAGE −350 MIL**



UNIT : mm / INCH





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•HYUNDAI SEMICONDUCTOR

HYM5C8256

256K×8-Bit CMOS DRAM MODULE

M411202C-JAN92

DESCRIPTION

The HYM5C8256M is a 256K words by 8bits dynamic RAM module and consists of eight HY53C256LF Fast Page mode CMOS DRAM in 18 pin PLCC package mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the 256K DRAMs.

HYM5C8256M is suitable for easy interchange and addition of 256K bytes memory.

FEATURES

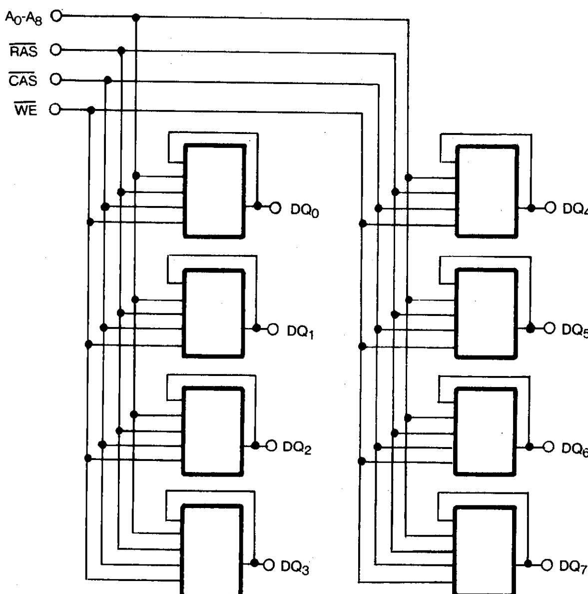
- **Fast Page Mode operation**
- **Fast access time**

	t_{RAC}	t_{CAC}	t_{PC}
HYM5C8256M-70	70	15	50
HYM5C8256M-80	80	20	55
HYM5C8256M-10	100	25	60
HYM5C8256M-12	120	30	70

- **Single power supply of 5V± 10%**
- **$\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh.**
- **Low power operating**
  3.08W max.(HYM5C8256M-70)
  2.64W max.(HYM5C8256M-80)
  2.20W max.(HYM5C8256M-10)
  1.98W max.(HYM5C8256M-12)
- **TTL compatible inputs and outputs**
- **256 refresh cycles / 4ms**

4

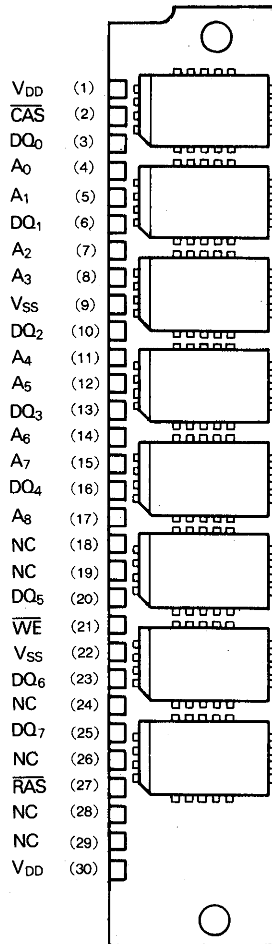
BLOCK DIAGRAM



PIN NAMES

A_0-A_8	ADDRESS INPUTS
DQ_0-DQ_7	DATA INPUT/OUTPUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBES
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS



NOTES :
1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
2. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	−55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS
(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM5C8256M MIN.	HYM5C8256M MAX.	UNIT	NOTE
$\vert I_{LI} \vert$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		–	80	μA	
$\vert I_{LO} \vert$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−70	–	560	mA	1, 2
			−80	–	480		
			−10	–	400		
			−12	–	360		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}		–	16	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−70	–	560	mA	2
			−80		480		
			−10		400		
			−12		360		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−70		360	mA	1, 2
			−80		320		
			−10		280		
			−12		240		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}$ ≥ V_{DD}−0.2V, $\overline{CAS}$= V_{IH}, other inputs ≥ V_{SS}			8	mA	1
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−70		560	mA	2
			−80		480		
			−10		400		
			−12		360		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :
1. I_{DD} is depends on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.
2. I_{DD} is depends upon the number of address transitions. Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in fast page mode.

4

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HYM5C8256M								UNIT	NOTE
			70		80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	120	10K	ns	
2	t_{RC}	Read or Write Cycle Time	130		145		175		205		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50		55		65		75		ns	
4	t_{ASR}	Row Address Set-up Time	0		0		0		0		ns	
5	t_{RAH}	Row Address Hold Time	15		15		15		20		ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35		40		45		55		ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	35	20	40	20	55	25	65	ns	1
8	t_{ASC}	Column Address Set-up Time	0		0		0		0		ns	
9	t_{CAH}	Column Address Hold Time	15		15		20		25		ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	55	25	60	25	75	30	90	ns	2
11	t_{RAC}	Access Time from $\overline{RAS}$		70		80		100		120	ns	3,4,5
12	t_{AA}	Access Time From Column Address		35		40		45		55	ns	5,6,12
13	t_{CAC}	Access Time from $\overline{CAS}$		15		20		25		30	ns	5,12
14	t_{CAS}	$\overline{CAS}$ Pulse Width	15	75K	20	75K	25	75K	30	75K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	15		20		25		30		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		0		ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		5		ns	7
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		5		ns	7
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15		15		15		20		ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	15	0	20	0	25	0	30	ns	8
21	t_{WP}	Write Command Pulse Width	15		15		20		25		ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	15		15		20		25		ns	
23	t_{AR}	Column Address Hold Time From $\overline{RAS}$	55		60		70		80		ns	
24	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	55		60		70		80		ns	
25	t_{WCS}	Write Command Set-up Time	0		0		0		0		ns	9,10
26	t_{WCH}	Write Command Hold Time	15		15		20		25		ns	
27	t_{DS}	Data In Set-up Time	0		0		0		0		ns	11
28	t_{DH}	Data In Hold Time	15		15		20		25		ns	11
29	t_{DHR}	Data In Hold Time Reference to $\overline{RAS}$	55		60		70		80		ns	
30	t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		50		55		65	ns	12

#	SYMBOL	PARAMETER	HYM5C8256M								UNIT	NOTE
			70		80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
31	t_{PC}	Fast Page Mode Cycle time	50		55		60		70		ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25		30		35		ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25		30		35		ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time, $\overline{CAS}$ before $\overline{RAS}$ Refresh	10		10		10		10		ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time, $\overline{CAS}$ before $\overline{RAS}$ Refresh	20		25		30		40		ns	
37	t_T	Transition Time(Rise and Fall)	3	25	3	25	3	25	3	25	ns	
38	t_{REF}	Refresh Interval(256 cycle)		4		4		4		4	ms	

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then the access time is controlled by t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.). If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.)
4. Assume $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.)
5. Measured with a load equivalent to two TTL loads and 100 pF.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max.) and $t_{RAD} \leq t_{RAD}$(max.).
7. Assumes that $t_{RCD} \leq t_{RCD}$(max.) and $t_{RAD} \geq t_{RAD}$(max.).
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{OFF} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
10. t_{WCS} is not a ristrictive operating parameter. This is included in the data sheet as a electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(max.), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$
12. Access time is determined by the longer of t_{AA}, t_{CAC}, t_{CPA}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max.).
14. AC measurements assume t_T=5ns.
15. An initial pause of 200μs is required after power-up and followed at least 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

4

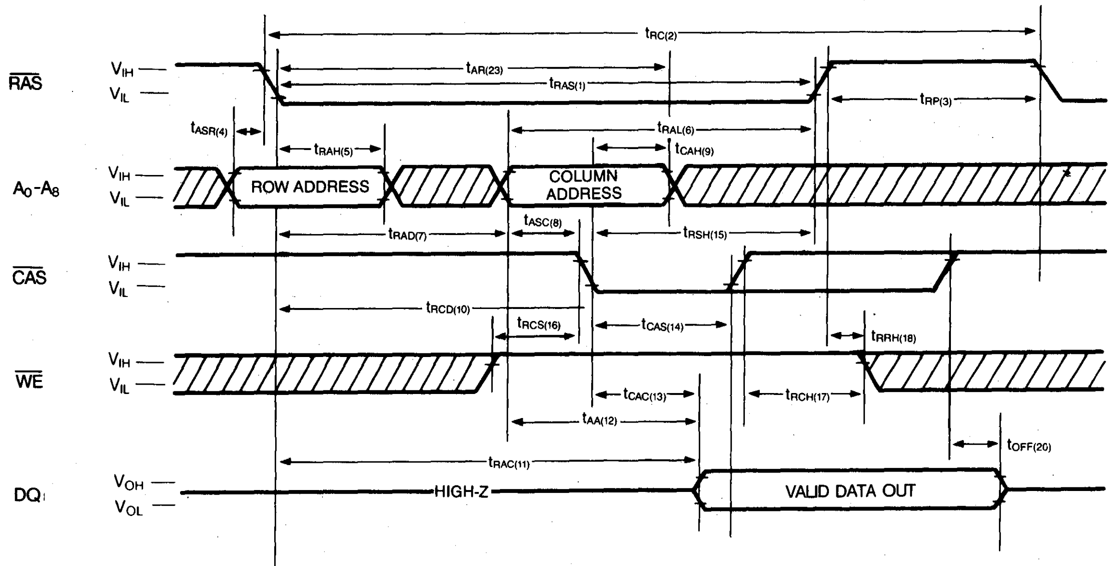
CAPACITANCE

(T_A=25°C, V_{DD}=5V+10%, V_{SS}=0V, unless otherwise noted

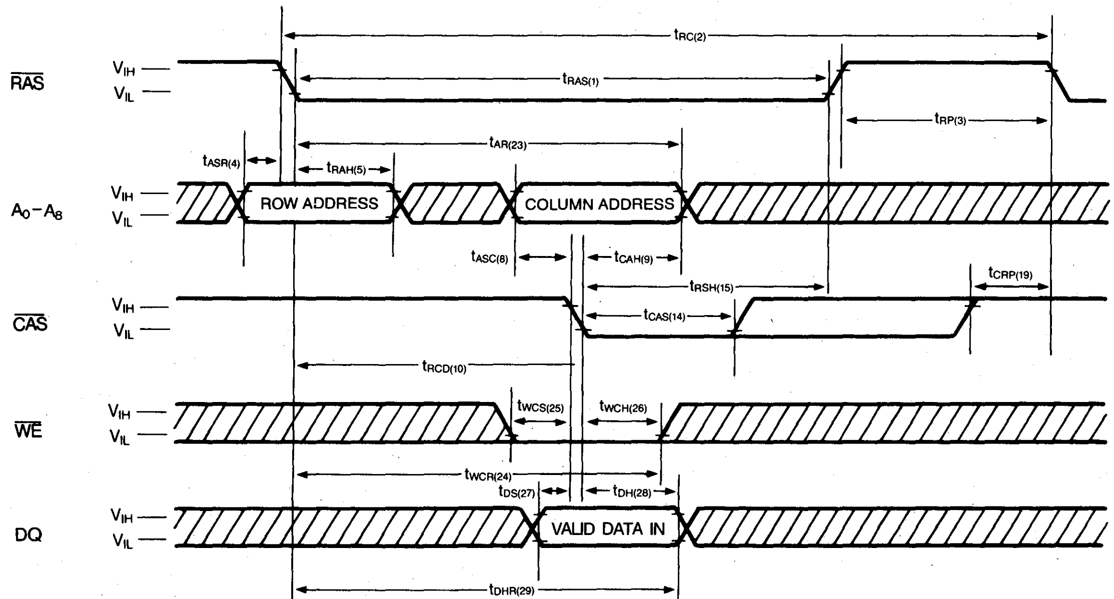
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance(A_0-A_8, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	55	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF

TIMING DIAGRAM

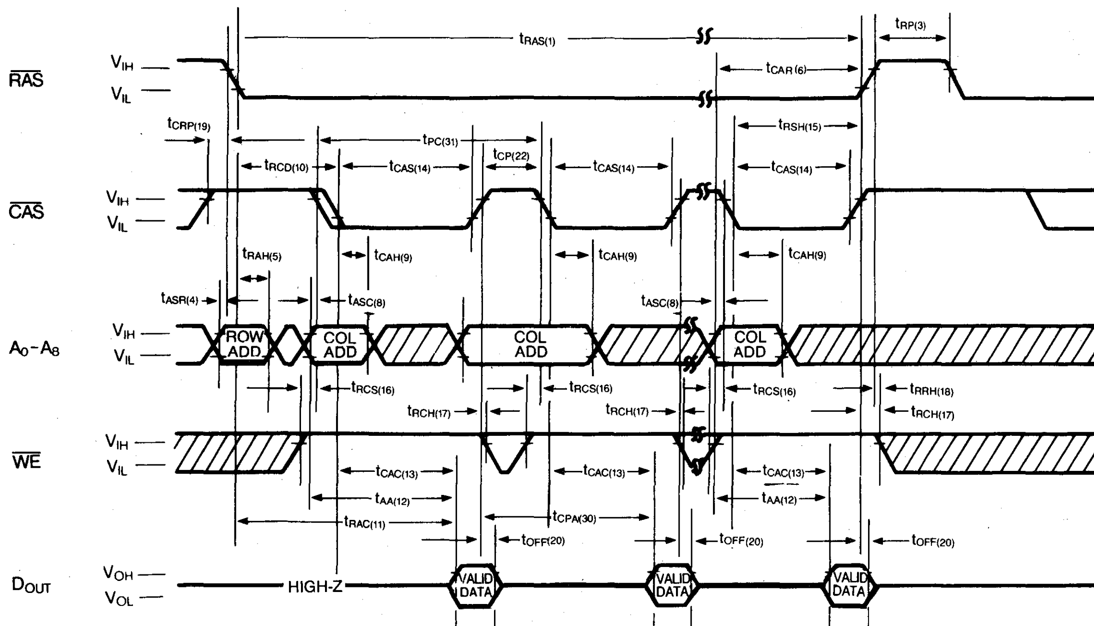
READ CYCLE



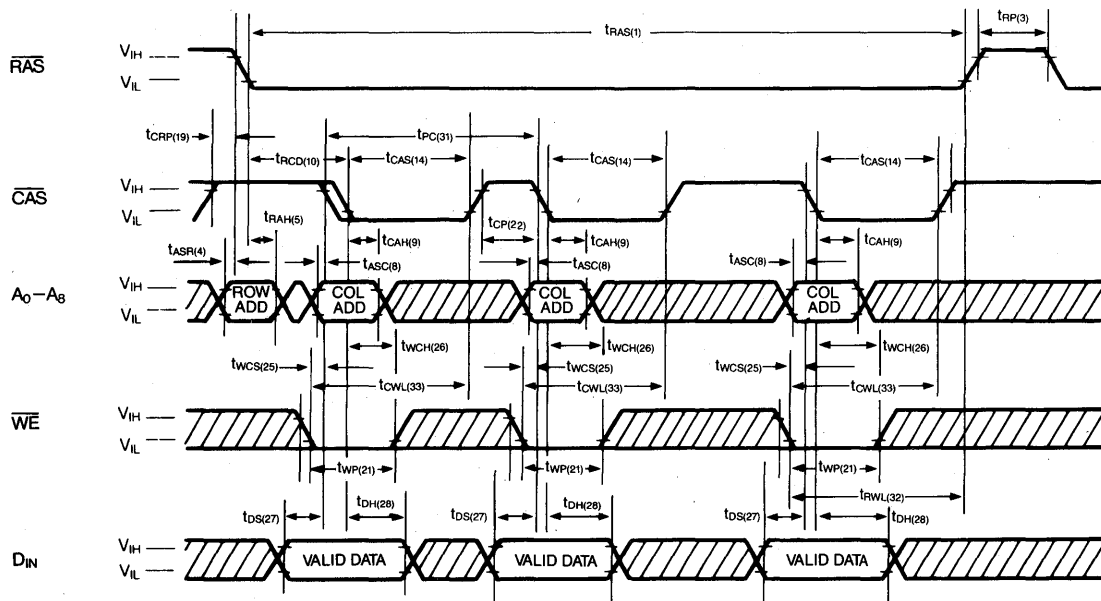
EARLY WRITE CYCLE



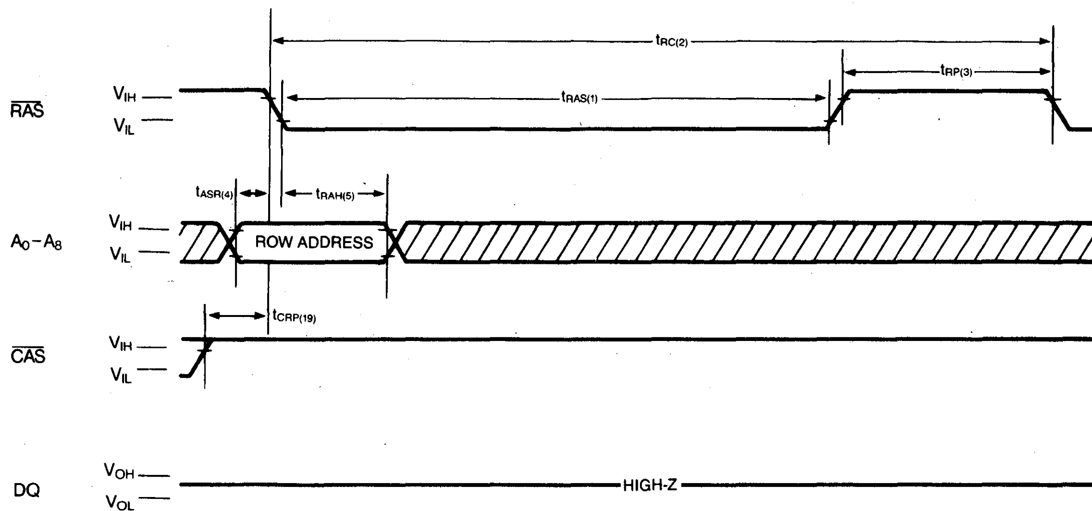
FAST PAGE MODE READ CYCLE



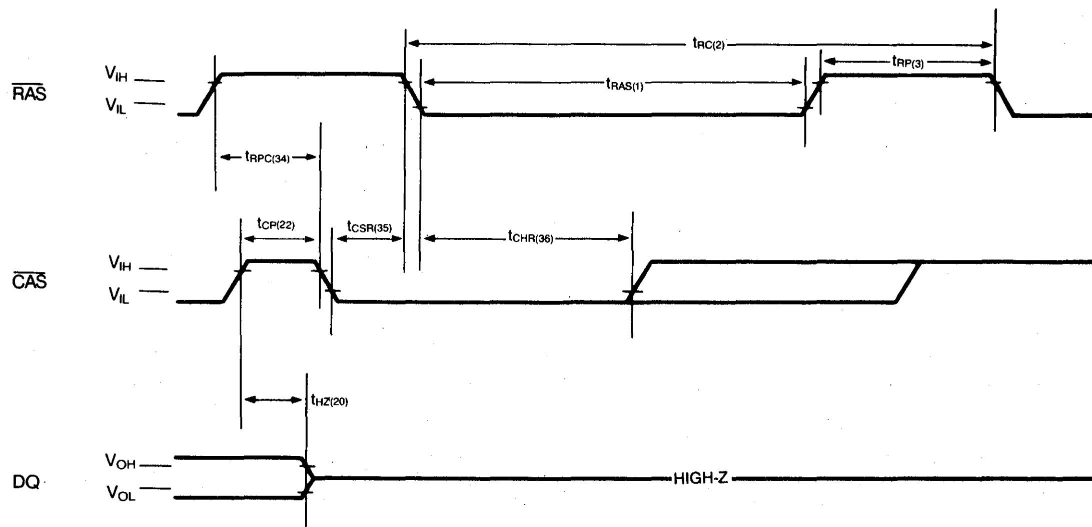
FAST PAGE MODE EARLY WRITE CYCLE



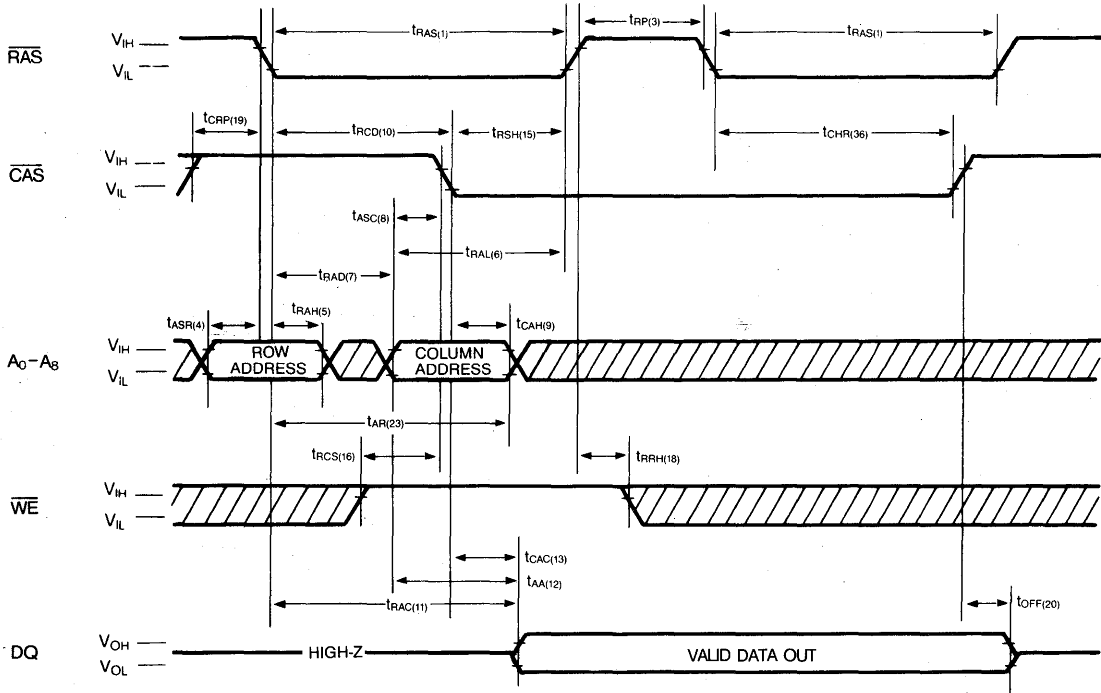
$\overline{RAS}$-ONLY REFRESH CYCLE



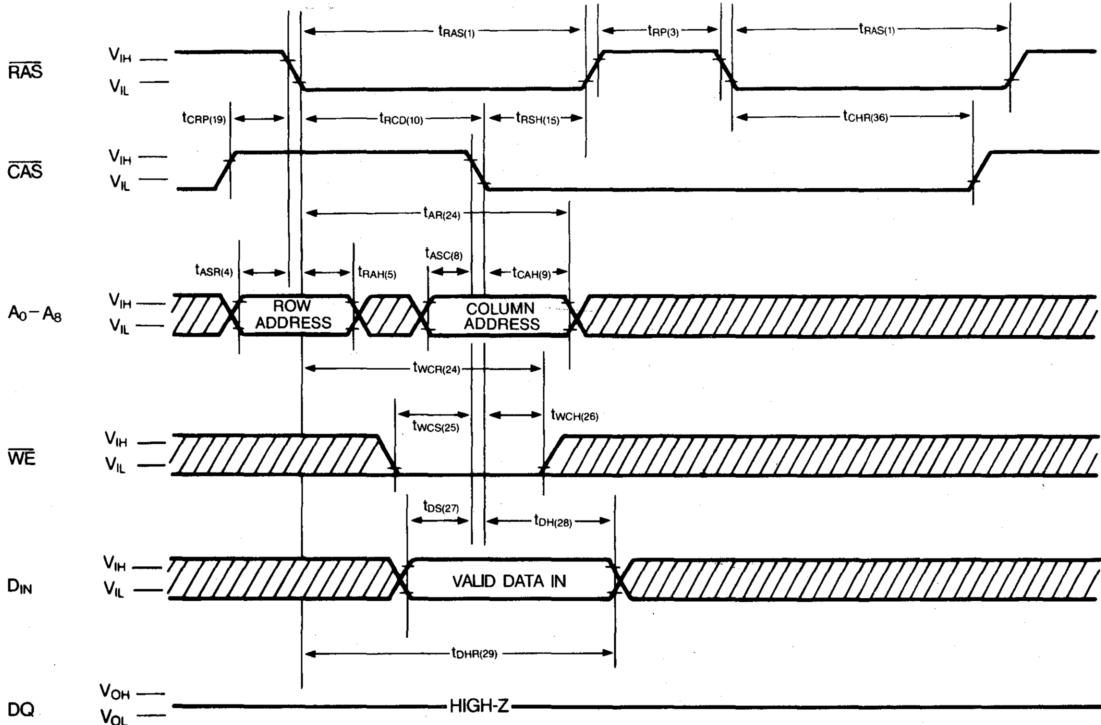
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)

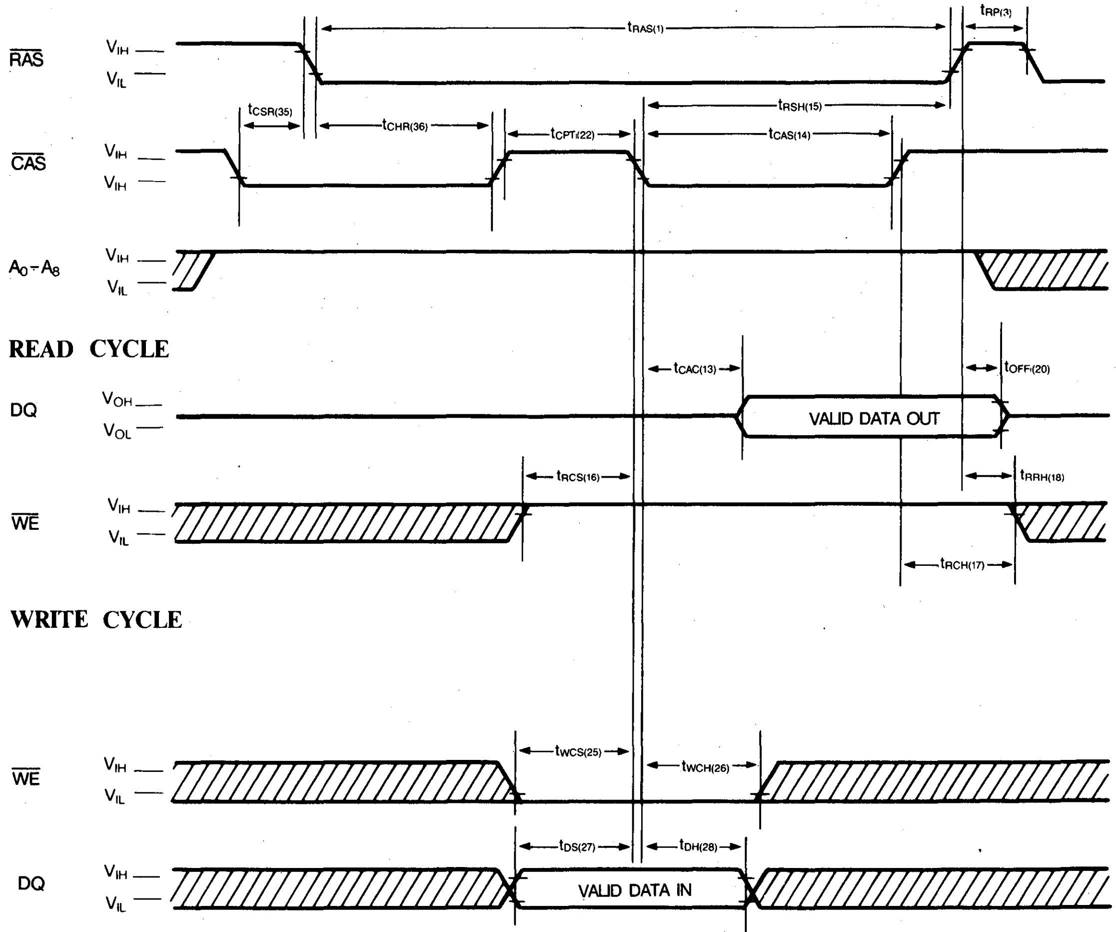


HIDDEN REFRESH CYCLE (WRITE)



4

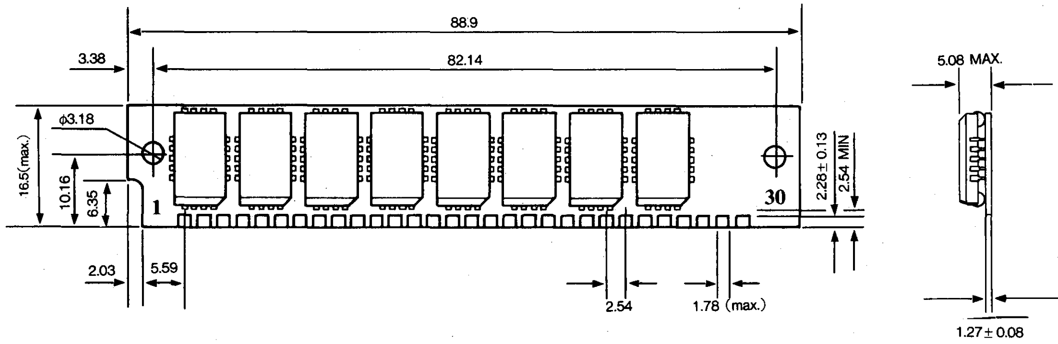
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



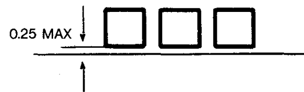
PACKAGE INFORMATION

HYM5C8256M

UNIT : mm



* DETAIL OF CONTACTS



4

MEMO

HYM58256A

256K×8-Bit CMOS DRAM MODULE

M451201B-OCT91

DESCRIPTION

The HYM58256AM is a 256K words by 8bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of two HY534256J in 20/26 pin SOJ mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM58256AM is suitable for easy interchange and addition of 256K bytes memory.

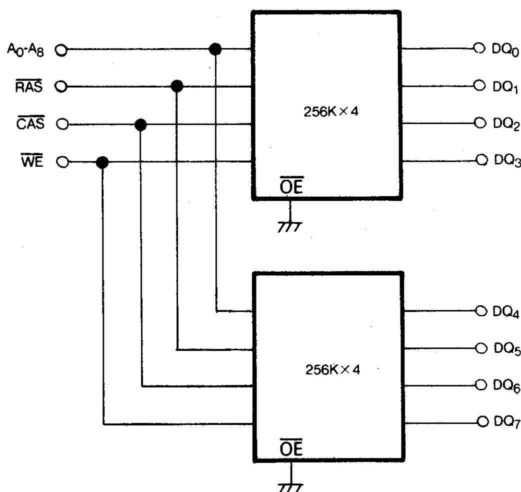
FEATURES

- **Fast Page Mode operation**
- **Fast Access Time**

	t_{RAC}	t_{CAC}	t_{PC}
HYM58256A-60	60	20	40
HYM58256A-70	70	20	40
HYM58256A-80	80	25	45
HYM58256A-10	100	25	55

- **Single power supply of 5V± 10%**
- **$\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh.**
- **Low power operating**
  0.99W max (HYM58256AM-60)
  0.88W max (HYM58256AM-70)
  0.77W max (HYM58256AM-80)
  0.66W max (HYM58256AM-10)
- **TTL compatible inputs and outputs**
- **512 refresh cycles / 8ms**

BLOCK DIAGRAM

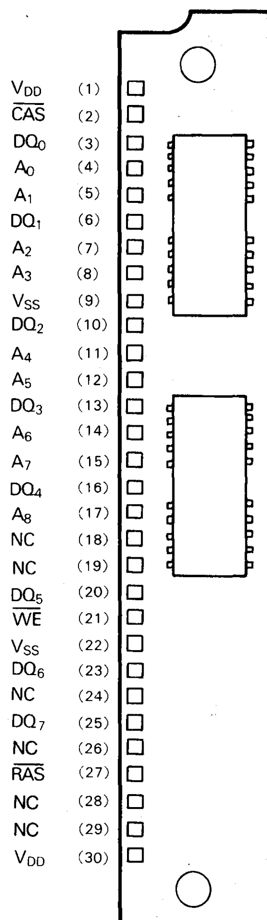


PIN NAMES

A_0-A_8	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS

HYM58256AM



NOTES :
1. Common $\overline{CAS}$ control for eight data-in and data-out lines(DQ_0DQ_7).
2. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature(Plastic)	−55 to 125	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	1.2	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

4

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM58256AM		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$			20	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60		180	mA	1, 2
			−70		160		
			−80		140		
			−10		120		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\geq V_{SS}$			4	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60		180	mA	2
			−70		160		
			−80		140		
			−10		120		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−60		140	mA	1.2
			−70		120		
			−80		100		
			−10		80		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs $\geq V_{SS}$			2	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60		180	mA	2
			−70		160		
			−80		140		
			−10		120		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in fast page mode.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HYM58256AM								UNIT	NOTE
			60		70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	85K	70	85K	80	85K	100	85K	ns	
2	t_{RC}	Read or Write Cycle Time	120		130		150		180		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		600		70		ns	
4	t_{ASR}	Row Address Set-up Time	0		0		0		0		ns	
5	t_{RAH}	Row Address Hold Time	10		10		10		10		ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		50		ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	20	50	25	60	25	75	ns	1
8	t_{ASC}	Column Address Set-up Time	0		0		0		0		ns	
9	t_{CAH}	Column Address Hold Time	15		15		15		20		ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	25	60	25	75	ns	2
11	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	3,4,5
12	t_{AA}	Access Time from Column Address		30		35		40		50	ns	5,7
13	t_{CAC}	Access Time from $\overline{CAS}$		20		20		20		25	ns	5,6
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20		20		25		25		ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20		20		20		25		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		0		ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	8
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	8
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		5		ns	
20	t_{HZ}	$\overline{CAS}$ to Output High Impedance	0	20	0	20	0	25	0	30	ns	11
21	t_{WP}	Write Command Pulse Width	15		15		15		20		ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		10		ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		75		ns	
24	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		75		ns	
25	t_{WCS}	Write Commnad Set-up Time	0		0		0		0		ns	9
26	t_{WCH}	Write Command Hold Time	15		15		15		20		ns	
27	t_{DS}	Data In Set-up Time	0		0		0		0		ns	10
28	t_{DH}	Data In Hold Time	15		15		15		20		ns	10

#	SYMBOL	PARAMETER	HYM58256AM								UNIT	NOTE
			60		70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50		55		60		75		ns	
30	t_{CPA}	Access Time from Column Precharge		35		35		40		50	ns	12
31	t_{PC}	Fast Page Mode Read or Write Cycle time	40		40		45		55		ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20			20		20		25	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	20		20					ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5		5		5		5		ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15		15		15		20		ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	3	50	ns	13
38	t_{REF}	Refresh Interval(512 Cycle)		8		8		8		8	ms	
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	100	70	100K	80	100K	100	100K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter test cycle)	55		65		70		85		ns	8
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0		0		0		0		ns	

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.), If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds $t_{RAD(max.)}$.
4. Assume $t_{RCD} \leq t_{RCD}$(max.), If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increaes by the amount that t_{RCD} exceeds t_{RCD}(max.).
5. Measured with a load equivalent to two TTL loads and 100pF.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max.) $t_{RAD} \leq t_{RAD}$(max.).
7. Assumes that $t_{RCD} \leq t_{RCD}$(max.) and $t_{RAD} \leq t_{RAD}$(max.).
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{WCS} is not restrictive operating parameters. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$.
11. t_{HZ} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
12. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CPA}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max.) and AC Measurements assume t_T=5ns.
14. An initial pause of 200μs is required after power-up and followed at least 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only Refresh). 8 initialization cycles are required after extended periods of bias without clocks.

CAPACITANCE

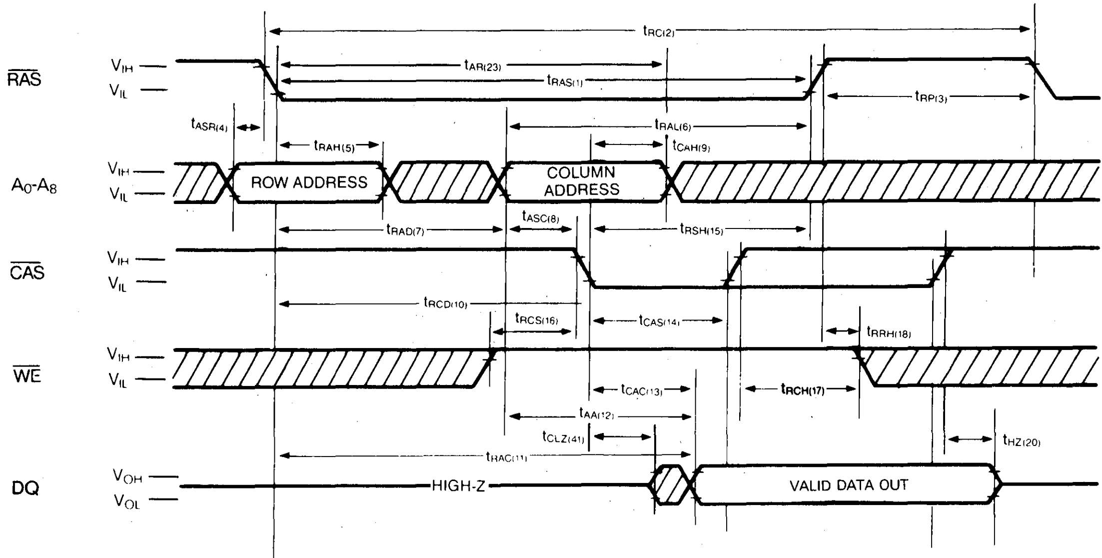
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance(A_0-A_8, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	20	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF

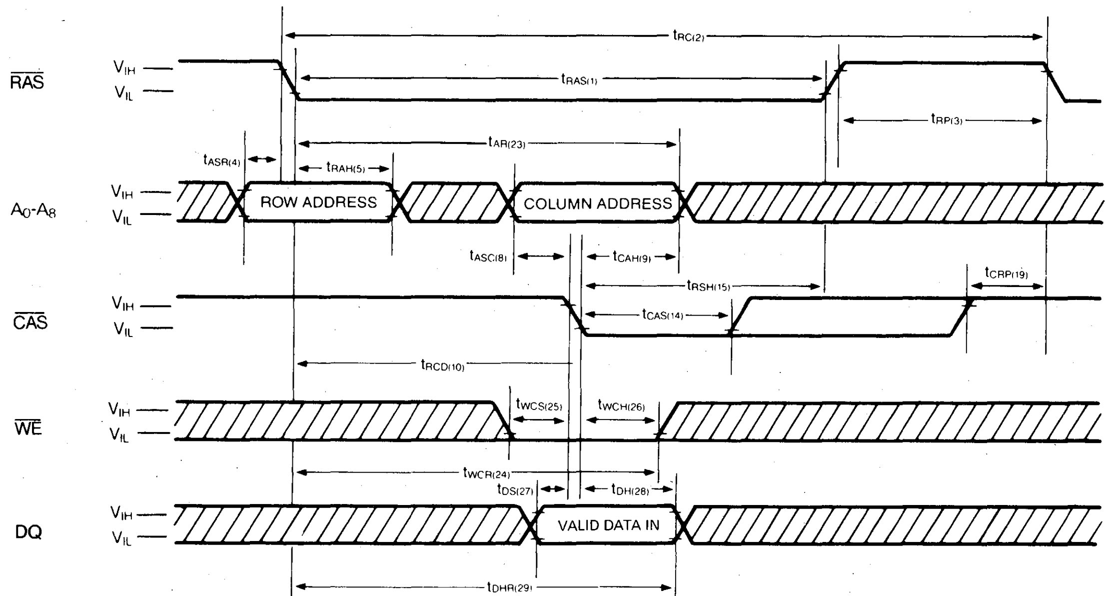
4

TIMING DIAGRAM

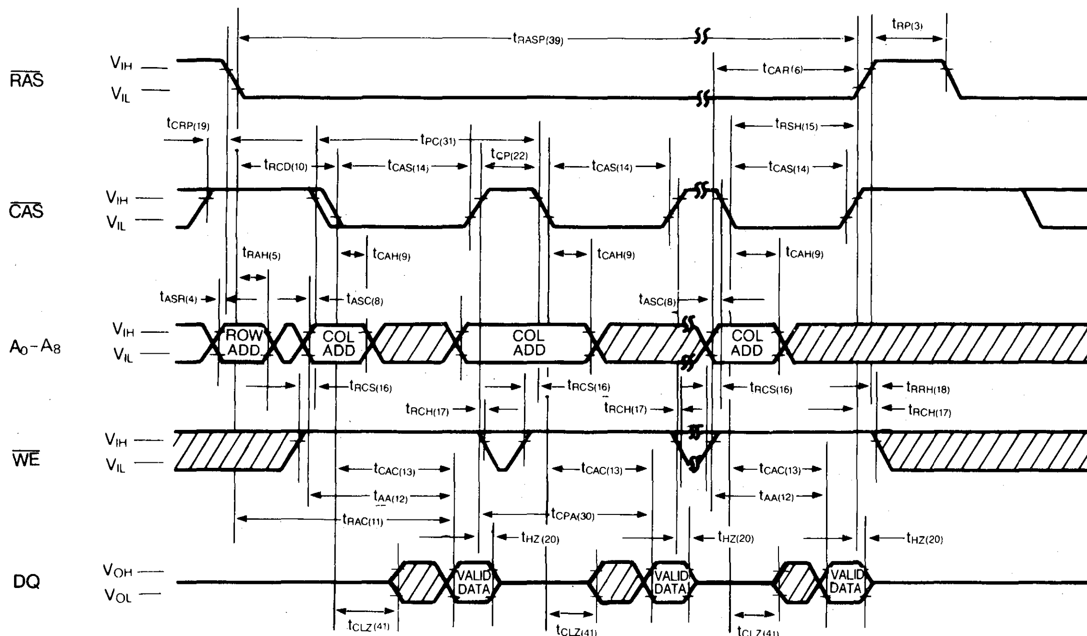
READ CYCLE



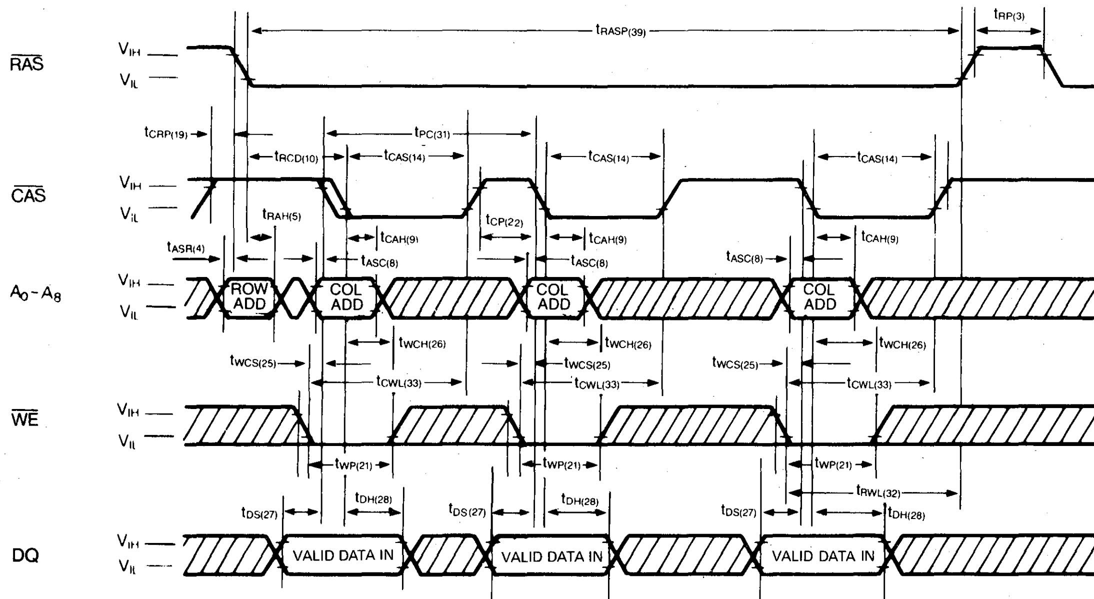
EARLY WRITE CYCLE



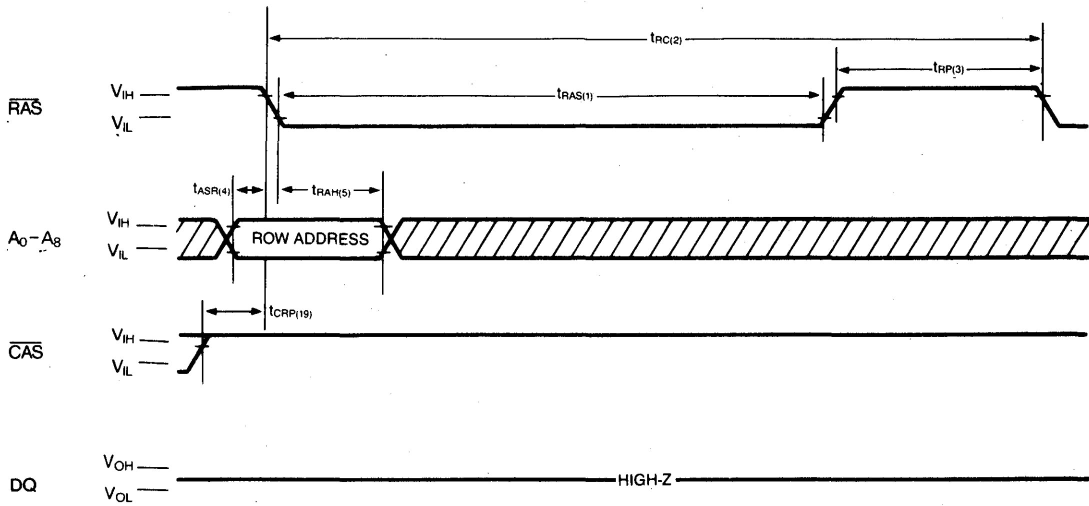
FAST PAGE MODE READ CYCLE



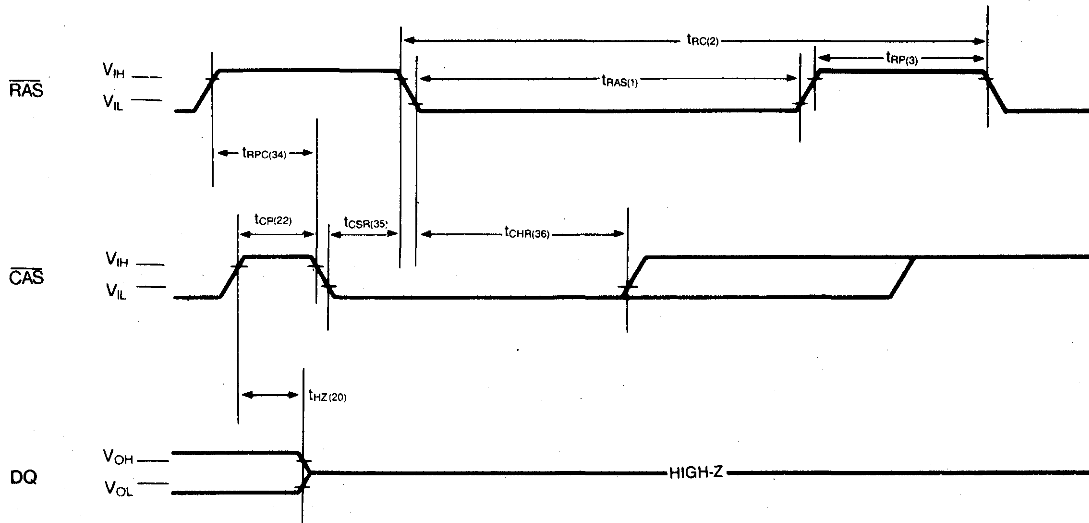
FAST PAGE MODE EARLY WRITE CYCLE



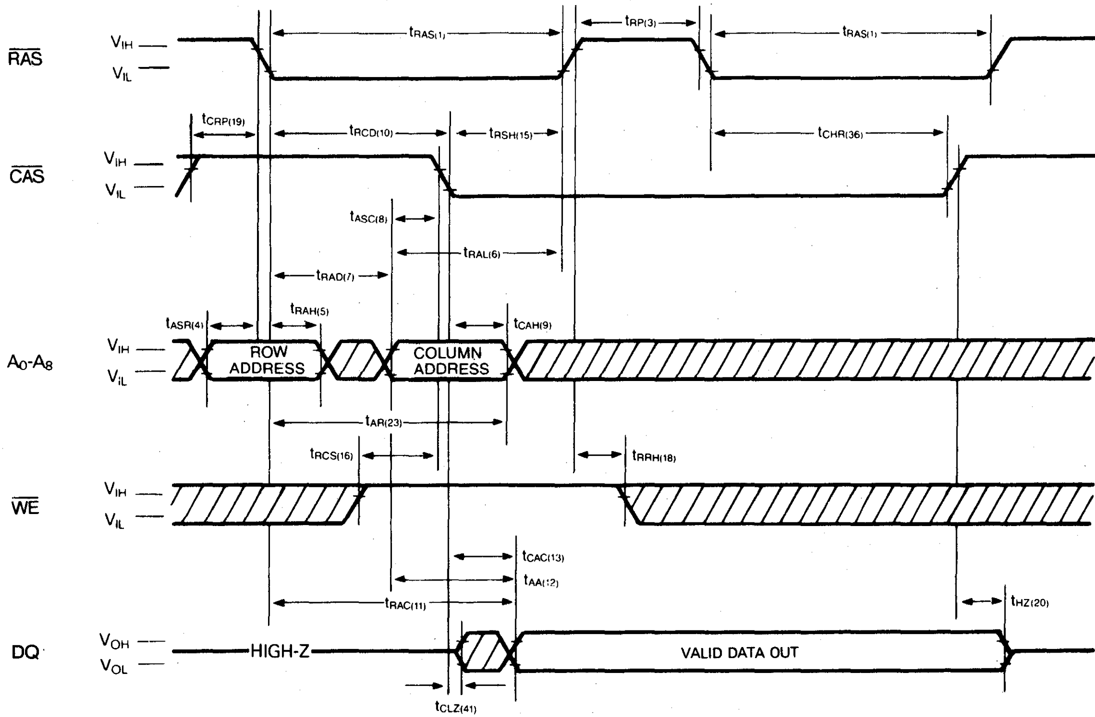
$\overline{RAS}$-ONLY REFRESH CYCLE



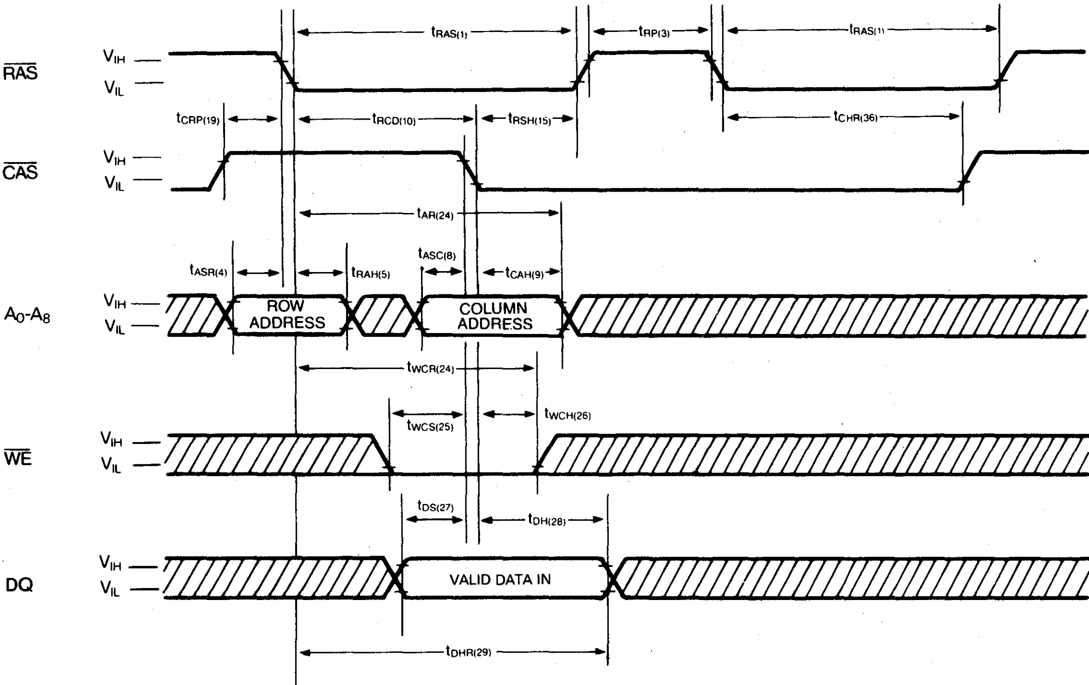
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



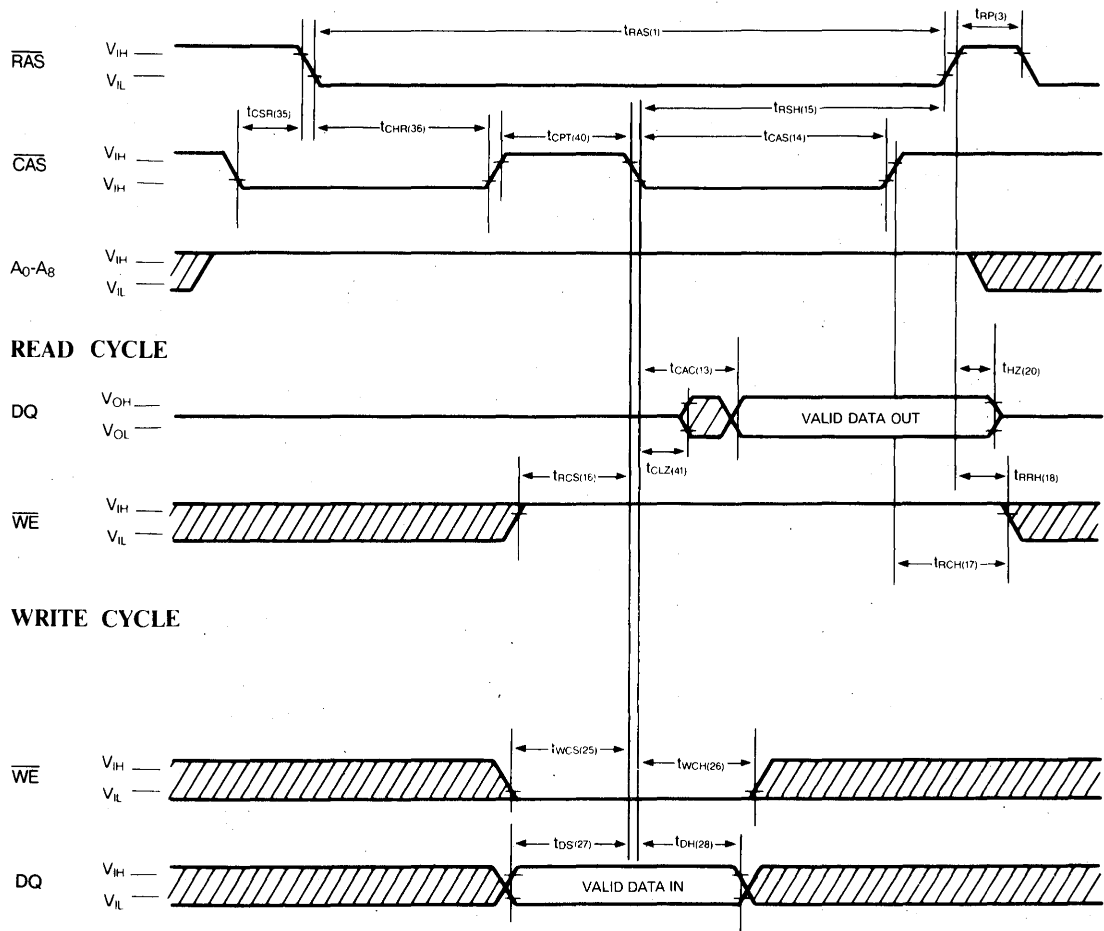
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

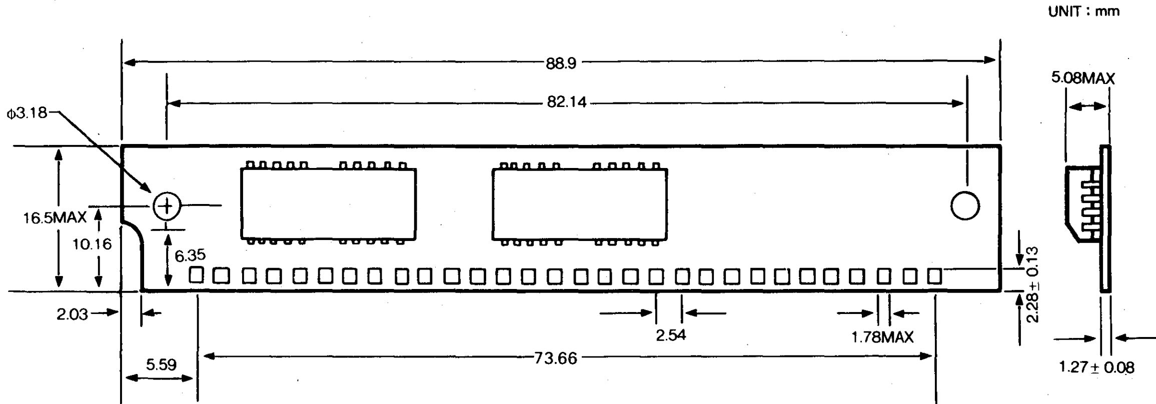


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

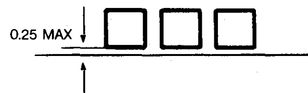


PACKAGE INFORMATION

HYM58256AM



* DETAIL OF CONTACTS



MEMO

HYM5C9256

256K×9-Bit CMOS DRAM MODULE

M421202B-OCT91

DESCRIPTION

The HYM5C9256M is a 256K words by 9 bits dynamic RAM module and consists of nine HY53C256LF Fast Page mode CMOS DRAMs in 18 pin PLCC package mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the 256K DRAMs.

HYM5C9256M is suitable for easy interchange and addition of 256K bytes memory with parity RAM.

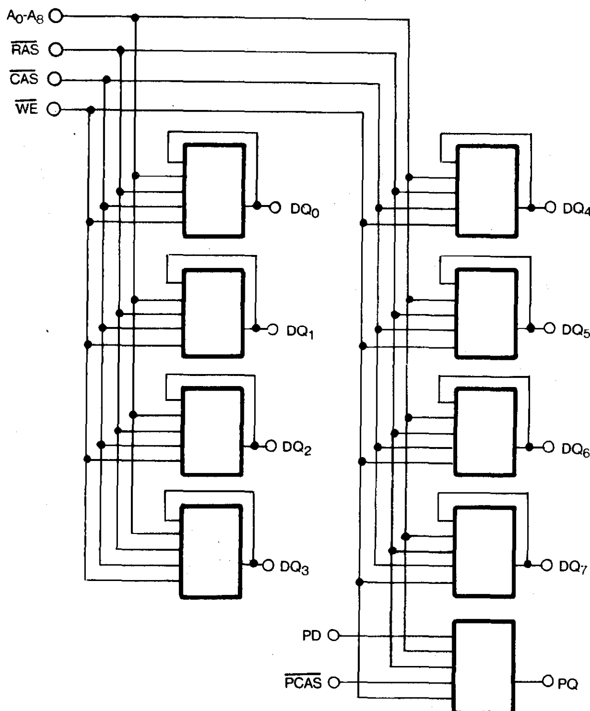
FEATURES

- **Fast Page Mode operation**
- **Fast access time**

	t_{RAC}	t_{CAC}	t_{PC}
HYM5C9256-70	70	15	50
HYM5C9256-80	80	20	55
HYM5C9256-10	100	25	60
HYM5C9256-12	120	30	70

- **Single power supply of 5V± 10%**
- **$\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh.**
- **Low power operating**
  3.47W max. (HYM5C9256M-70)
  2.97W max. (HYM5C9256M-80)
  2.48W max. (HYM5C9256M-10)
  2.23W max. (HYM5C9256M-12)
- **TTL compatible inputs and outputs**
- **256 refresh cycles / 4ms**

BLOCK DIAGRAM

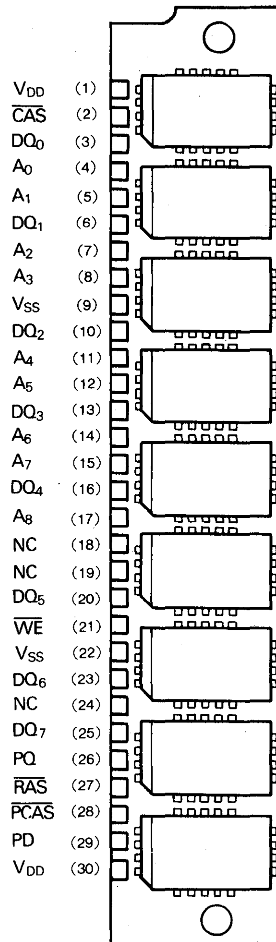


PIN NAMES

A_0-A_8	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
PD	DATA IN PARITY
PQ	DATA OUT FOR PARITY
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{PCAS}$	$\overline{CAS}$ FOR PARITY
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS

HYM5C9256M



NOTES :
1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
2. Separate $\overline{PCAS}$ control for one separate pair of data-in (PD) and data-out (PQ) lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out(DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	−55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	9	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS
(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM5C9256M MIN.	HYM5C9256M MAX.	UNIT	NOTE
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$			90	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−70		630	mA	1, 2
			−80		540		
			−10		450		
			−12		405		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\ge V_{SS}$			18	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−70		630	mA	2
			−80		540		
			−10		450		
			−12		405		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−70		405	mA	1, 2
			−80		360		
			−10		315		
			−12		270		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs $\ge V_{SS}$			9	mA	1
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−70		630	mA	2
			−80		540		
			−10		450		
			−12		405		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :
1. I_{DD} is depends on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.
2. I_{DD} is depends upon the number of address transitions. Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in fast page mode.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HYM5C9256M								UNIT	NOTE
			70		80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	120	10K	ns	
2	t_{RC}	Read or Write Cycle Time	130		145		175		205		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50		55		65		75		ns	
4	t_{ASR}	Row Address Set-up Time	0		0		0		0		ns	
5	t_{RAH}	Row Address Hold Time	15		15		15		20		ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35		40		45		55		ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	35	20	40	20	55	25	65	ns	1
8	t_{ASC}	Column Address Set-up Time	0		0		0		0		ns	
9	t_{CAH}	Column Address Hold Time	15		15		20		25		ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	55	25	60	25	75	30	90	ns	2
11	t_{RAC}	Access Time from $\overline{RAS}$		70		80		100		120	ns	3,4,5
12	t_{AA}	Access Time From Column Address		35		40		45		55	ns	5,6,12
13	t_{CAC}	Access Time from $\overline{CAS}$		15		20		25		30	ns	5,12
14	t_{CAS}	$\overline{CAS}$ Pulse Width	15	75K	20	75K	25	75K	30	75K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	15		20		25		30		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		0		ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		5		ns	7
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		5		ns	7
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15		15		15		20		ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	15	0	20	0	25	0	30	ns	8
21	t_{WP}	Write Command Pulse Width	15		15		20		25		ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	15		15		20		25		ns	
23	t_{AR}	Column Address Hold Time From $\overline{RAS}$	55		60		70		80		ns	
24	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	55		60		70		80		ns	
25	t_{WCS}	Write Command Set-up Time	0		0		0		0		ns	9,10
26	t_{WCH}	Write Command Hold Time	15		15		20		25		ns	
27	t_{DS}	Data In Set-up Time	0		0		0		0		ns	11
28	t_{DH}	Data In Hold Time	15		15		20		25		ns	11
29	t_{DHR}	Data In Hold Time Reference to $\overline{RAS}$	55		60		70		80		ns	
30	t_{CPA}	Access Time from $\overline{CAS}$ Precharge		45		50		55		65	ns	12

#	SYMBOL	PARAMETER	HYM5C9256M								UNIT	NOTE
			70		80		10		12			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
31	t_{PC}	Fast Page Mode Cycle time	50		55		60		70		ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25		30		35		ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25		30		35		ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time, $\overline{CAS}$ before $\overline{RAS}$ Refresh	10		10		10		10		ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time, $\overline{CAS}$ before $\overline{RAS}$ Refresh	20		25		30		40		ns	
37	t_T	Transition Time(Rise and Fail)	3	25	3	25	3	25	3	25	ns	
38	t_{REF}	Refresh Interval(256 cycle)		4		4		4		4	ms	

NOTES :

1. Operation within the t_{RAD}(max.)limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. Operation within the t_{RCD}(max.)limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then the access time is controlled by t_{CAC}.
3. Assume $t_{RAD} \leq t_{RAD}$(max.). If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.)
4. Assume $t_{RCD} \leq t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.)
5. Measured with a load equivalent to two TTL loads and 100 pF.
6. Assumes that $t_{RCD} \geq t_{RCD}$(max.) and $t_{RAD} \leq t_{RAD}$(max.).
7. Assumes that $t_{RCD} \leq t_{RCD}$(max.) and $t_{RAD} \geq t_{RAD}$(max.).
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{OFF} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
10. t_{WCS} is not a ristrictive operating parameter. This is included in the data sheet as a electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$
12. Access time is determined by the longer of t_{AA}, t_{CAC}, t_{CPA}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max).
14. AC measurements assume t_T=5ns.
15. An initial pause of 200μs is required after power-up and followed by at least 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

CAPACITANCE

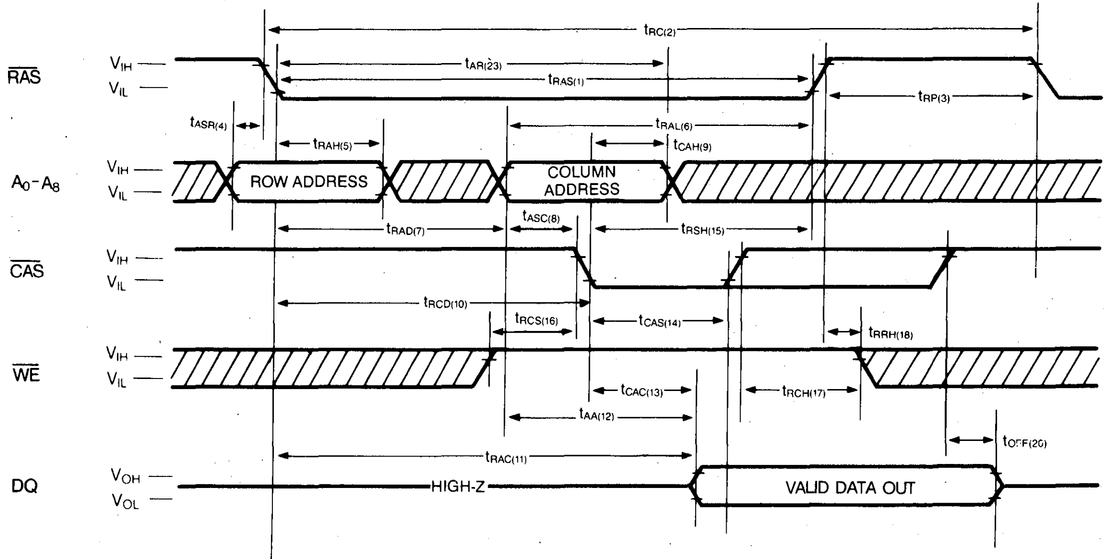
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_8, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{IN2}	Input Capacitance(PD, $\overline{PCAS}$)	–	10	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF
C_{PQ}	Output Capacitance(PQ)	–	10	pF

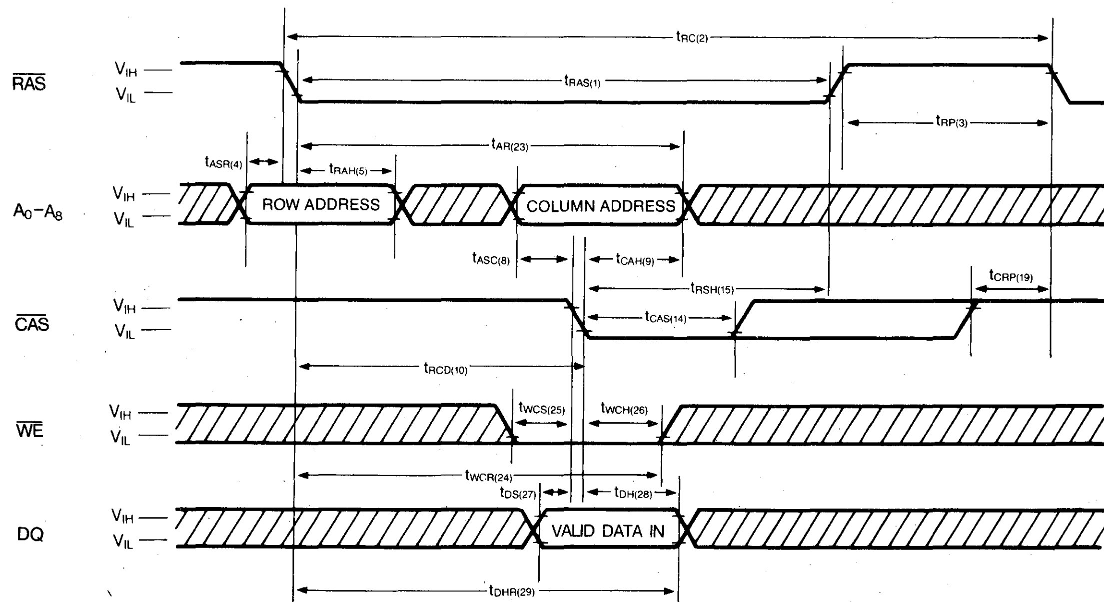
TIMING DIAGRAM

(CAS includes PCAS and CAS, D_{IN} includes DQ_0-DQ_7 and PD, D_{OUT} includes DQ_0-DQ_7 and PQ.)

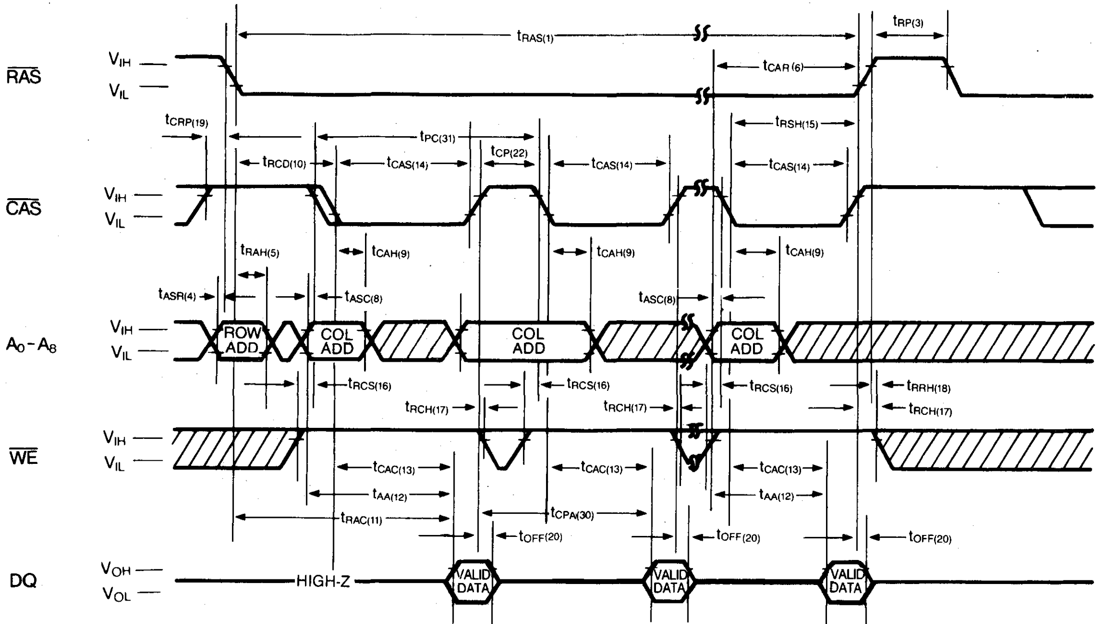
READ CYCLE



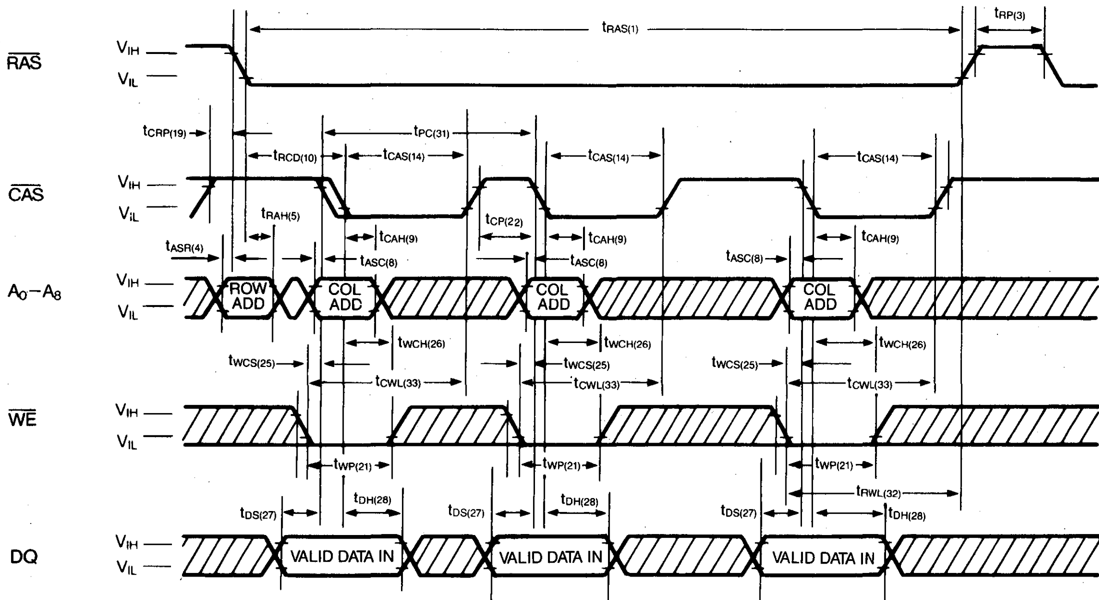
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE



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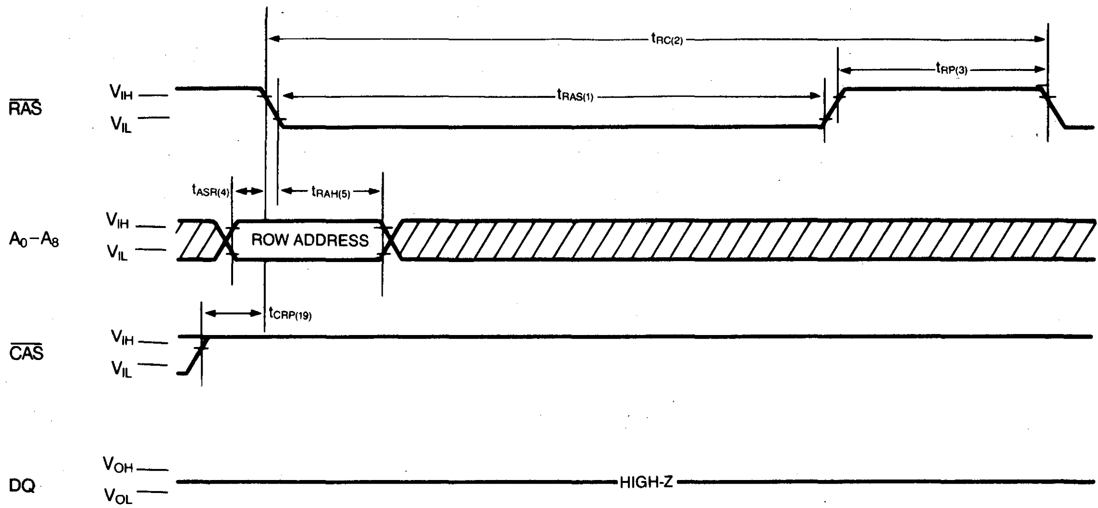
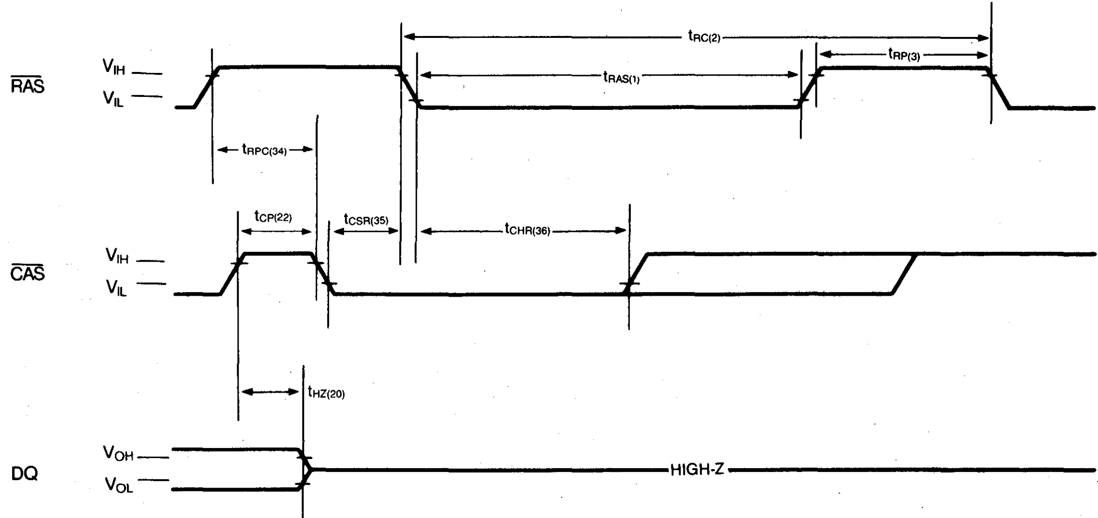
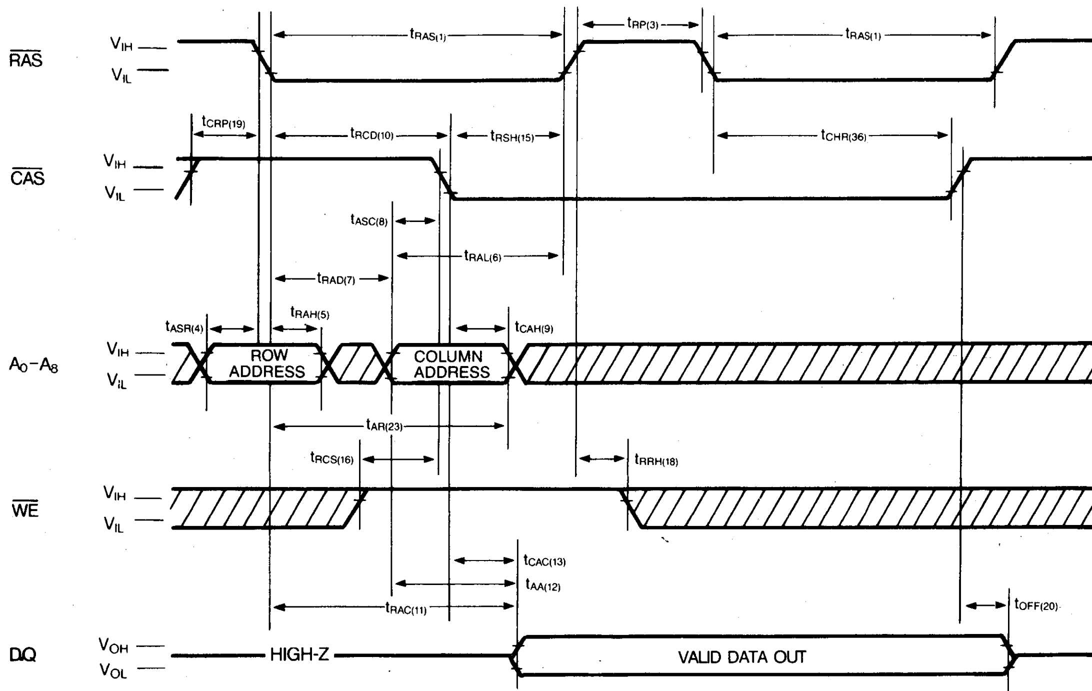
$\overline{RAS}$-ONLY REFRESH CYCLE



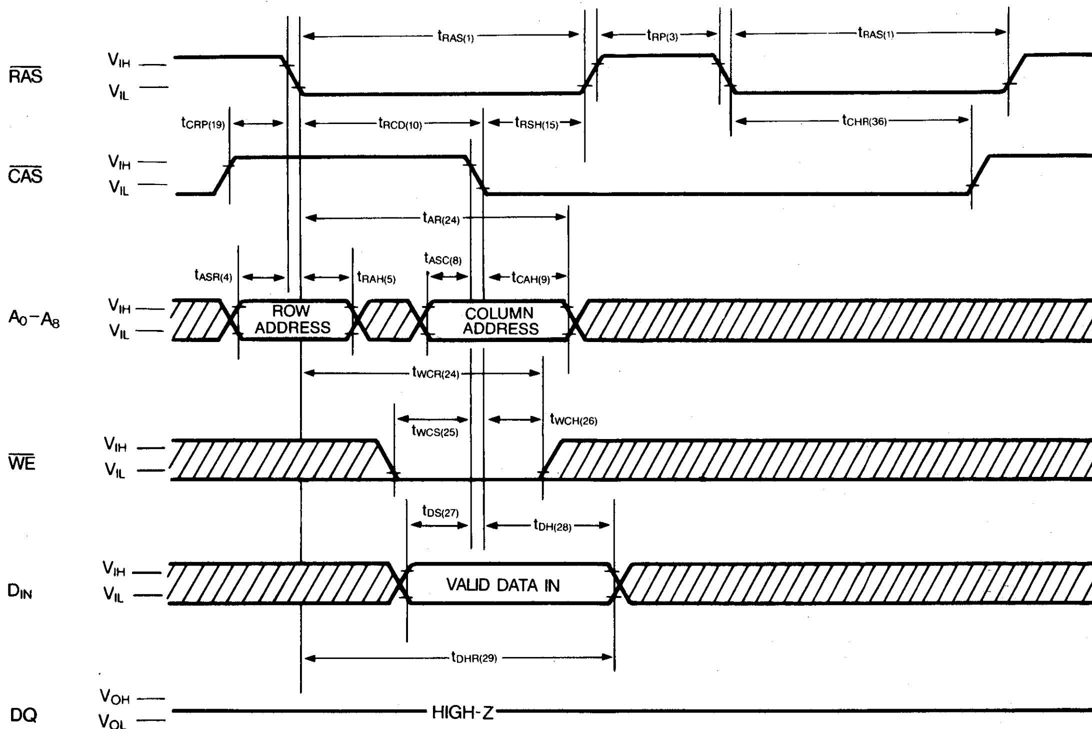
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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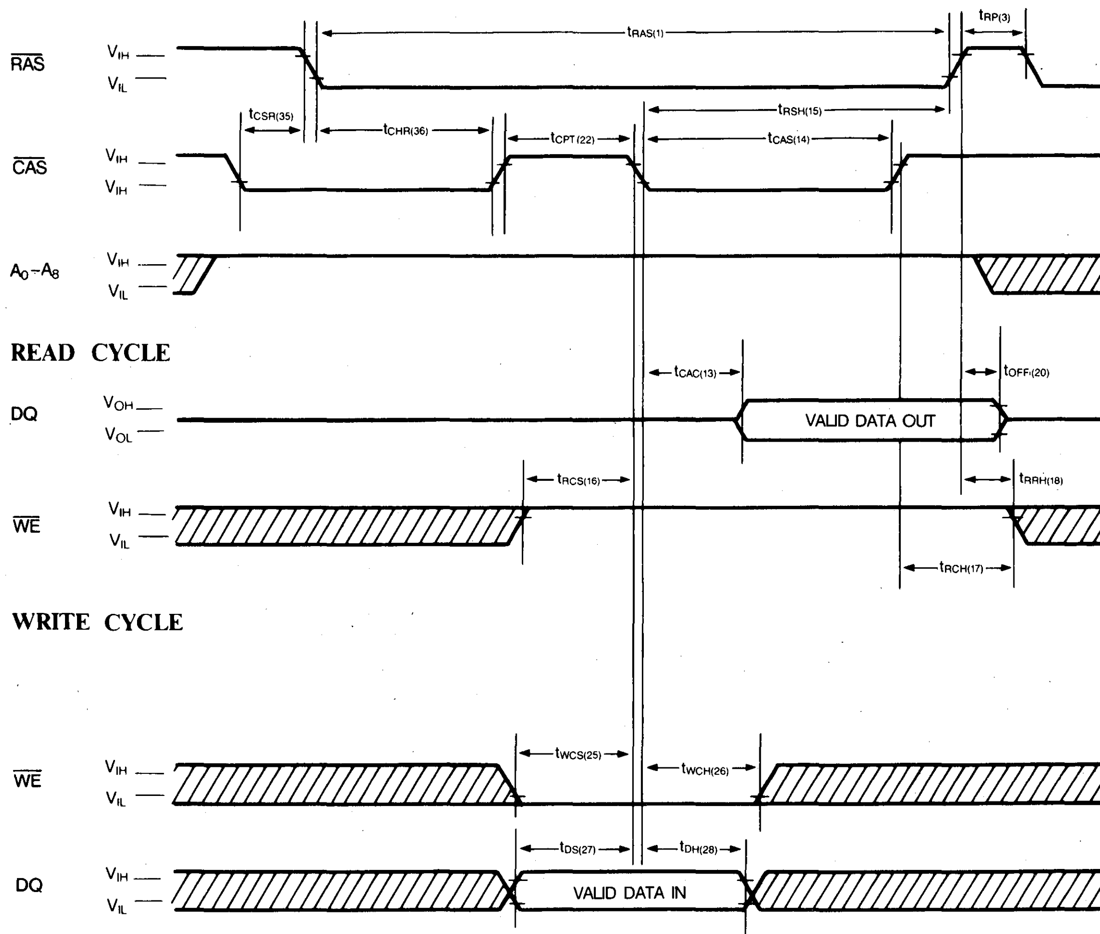
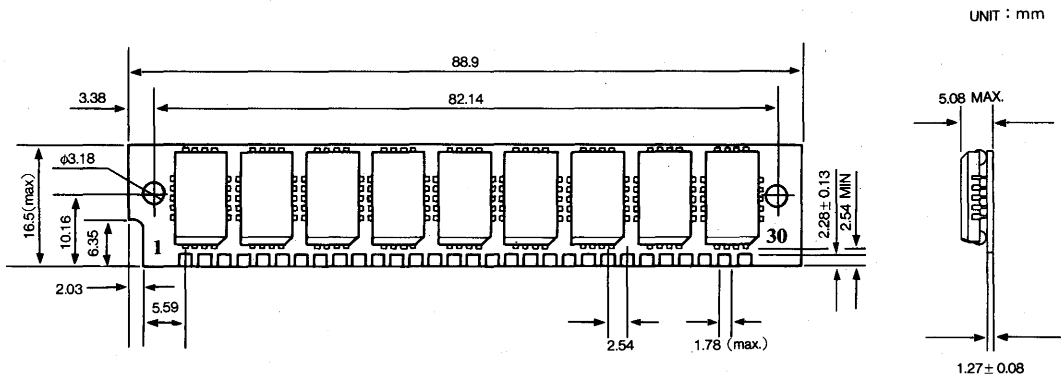
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

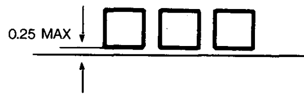


PACKAGE INFORMATION

HYM5C9256M



* DETAIL OF CONTACTS



4

MEMO

HYUNDAI SEMICONDUCTOR

HYM59256A

256K×9-Bit CMOS DRAM MODULE

M451202B-OCT91

DESCRIPTION

The HYM59256AM is a 256K words by 9bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of two HY534256J in 20/26 pin SOJ and one HY53C256LF in 18 pin PLCC mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM59256AM is suitable for easy interchange and addition of 256K bytes memory with parity RAM.

FEATURES

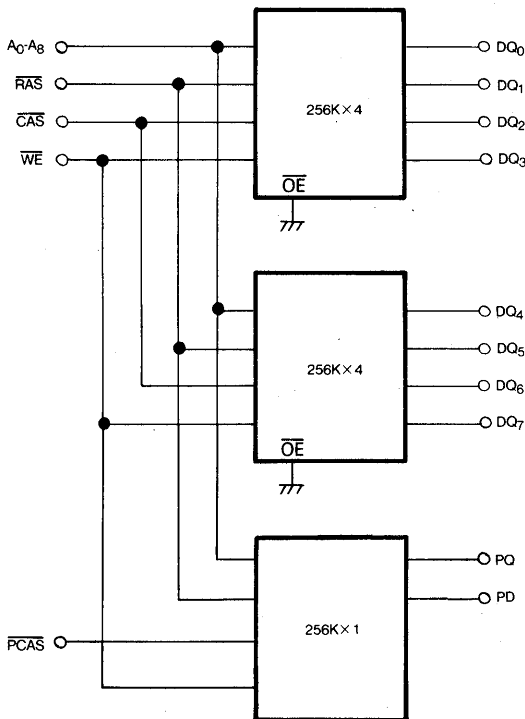
- Fast Page Mode operation
- Fast Access Time

	t_{RAC}	t_{CAC}	t_{PC}
HYM59256AM-70	70	20	50
HYM59256AM-80	80	25	55
HYM59256AM-10	100	25	60

- Single power supply of 5V± 10%
- $\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh.
- Low power operating
  1.26W max (HYM59256AM-70)
  1.10W max (HYM59256AM-80)
  0.93W max (HYM59256AM-10)
- TTL compatible inputs and outputs
- 512 refresh cycles / 8ms

4

BLOCK DIAGRAM

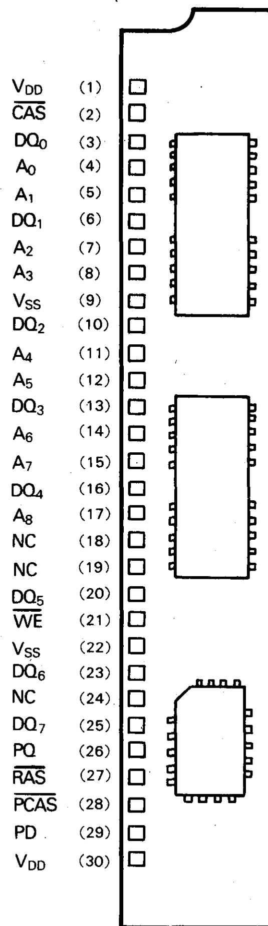


PIN NAMES

A_0-A_8	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
PD	DATA IN FOR PARITY
PQ	DATA OUT FOR PARITY
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{PCAS}$	$\overline{CAS}$ FOR PARITY
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS

HYM59256AM



NOTES :

1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
2. Separate $\overline{PCAS}$ control for one separate pair of data-in (PD) and data-out (PQ) lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature(Plastic)	−55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	1.8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

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DC CHARACTERISTICS
(T_A=0°C to70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM59256AM		UNIT	NOTE
				MIN.	MAX.		
$\mid I_{LI} \mid$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$			30	µA	
$\mid I_{LO} \mid$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	µA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−70		230	mA	1, 2
			−80		200		
			−10		170		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\ge V_{SS}$			6	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−70		230	mA	2
			−80		200		
			−10		170		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−70		165	mA	1, 2
			−80		140		
			−10		115		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs $\ge V_{SS}$			3	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−70		230	mA	2
			−80		200		
			−10		170		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in fast page mode.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HYM59256AM						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	130		150		180		ns	
3	t_{RP}	$\overline{\text{RAS}}$ Precharge Time	50		60		70		ns	
4	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
5	t_{RAH}	Row Address Hold Time	15		15		15		ns	
6	t_{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	35		40		50		ns	
7	t_{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	20	50	20	60	25	75	ns	1
8	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
9	t_{CAH}	Column Address Hold Time	15		15		20		ns	
10	t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	25	55	25	60	25	75	ns	2
11	t_{RAC}	Access Time from $\overline{\text{RAS}}$		70		80		100	ns	3,4,5
12	t_{AA}	Access Time from Column Address		35		40		50	ns	5,7
13	t_{CAC}	Access Time from $\overline{\text{CAS}}$		20		25		25	ns	5,6
14	t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	20		25		30		ns	
15	t_{RSH}	$\overline{\text{RAS}}$ Hold Time	25		25		30		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	5		5		5		ns	8
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	5		5		5		ns	8
19	t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	15		15		15		ns	
20	t_{HZ}	$\overline{\text{CAS}}$ to Output High Impedance	0	20	0	25	0	30	ns	11
21	t_{WP}	Write Command Pulse Width	15		15		20		ns	
22	t_{CP}	$\overline{\text{CAS}}$ Precharge Time	15		15		20		ns	
23	t_{AR}	Column Address Hold Time from $\overline{\text{RAS}}$	55		60		75		ns	
24	t_{WCR}	Write Command Hold Time from $\overline{\text{RAS}}$	55		60		75		ns	
25	t_{WCS}	Write Commnad Set-up Time	0		0		0		ns	9
26	t_{WCH}	Write Command Hold Time	15		15		20		ns	
27	t_{DS}	Data In Set-up Time	0		0		0		ns	10
28	t_{DH}	Data In Hold Time	15		15		20		ns	10

#	SYMBOL	PARAMETER	HYM59256AM						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	55		60		75		ns	
30	t_{CPA}	Access Time from Column Precharge		35		40		50	ns	12
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	50		55		60		ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25		30		ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25		30		ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5		5		5		ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	20		25		30		ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	13
38	t_{REF}	Refresh Interval(512 Cycle)		8		8		8	ms	16
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	70	100K	80	100K	100	100K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40		40		50		ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0		0		0		ns	3

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
3. Assume $t_{RAD} \le t_{RAD}$(max.), If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds $t_{RAD(max.)}$.
4. Assume $t_{RCD} \le t_{RCD}$(max.), If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.).
5. Measured with a load equivalent to two TTL loads and 100pF.
6. Assumes that $t_{RCD} \ge t_{RCD}$(max.) and $t_{RAD} \le t_{RAD}$(max.).
7. Assumes that $t_{RCD} \le t_{RCD}$(max.) and $t_{RAD} \le t_{RAD}$(max.).
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as a electrical characteristic only. If $t_{WCS} \ge t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
10. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$.
11. t_{HZ} defines the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
12. Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CPA}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max.) and AC Measurements assume t_T=5ns.
14. An initial pause of 200μs is required after power-up and followed at least 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only Refresh). 8 initialization cycles are required after extended periods of bias without clocks.

CAPACITANCE

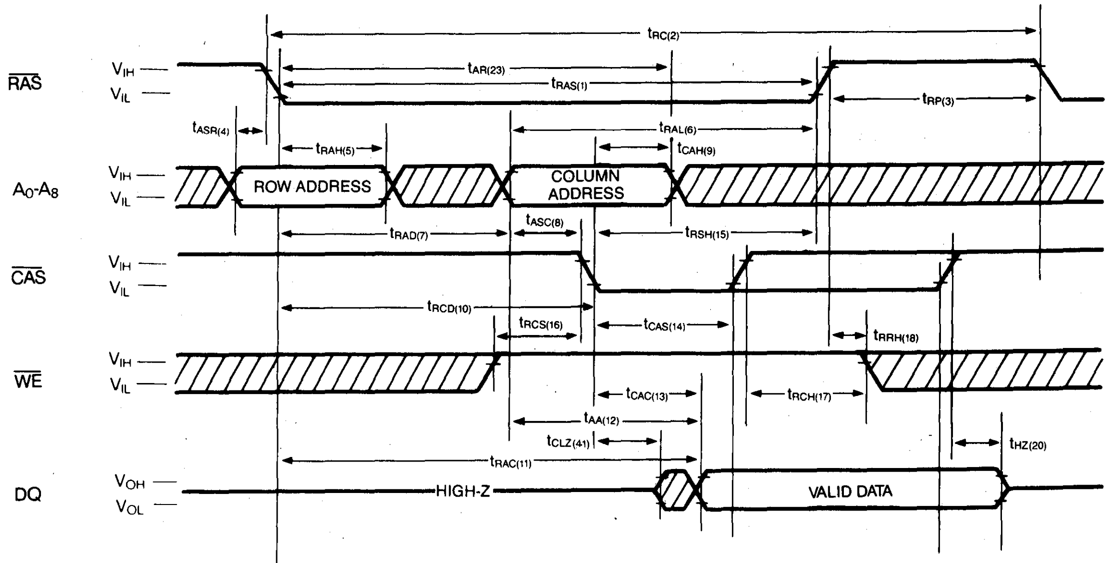
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_8, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	25	pF
C_{IN2}	Input Capacitance(PD, $\overline{PCAS}$)	–	10	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF
C_{PQ}	Output Capacitance(PQ)	–	10	pF

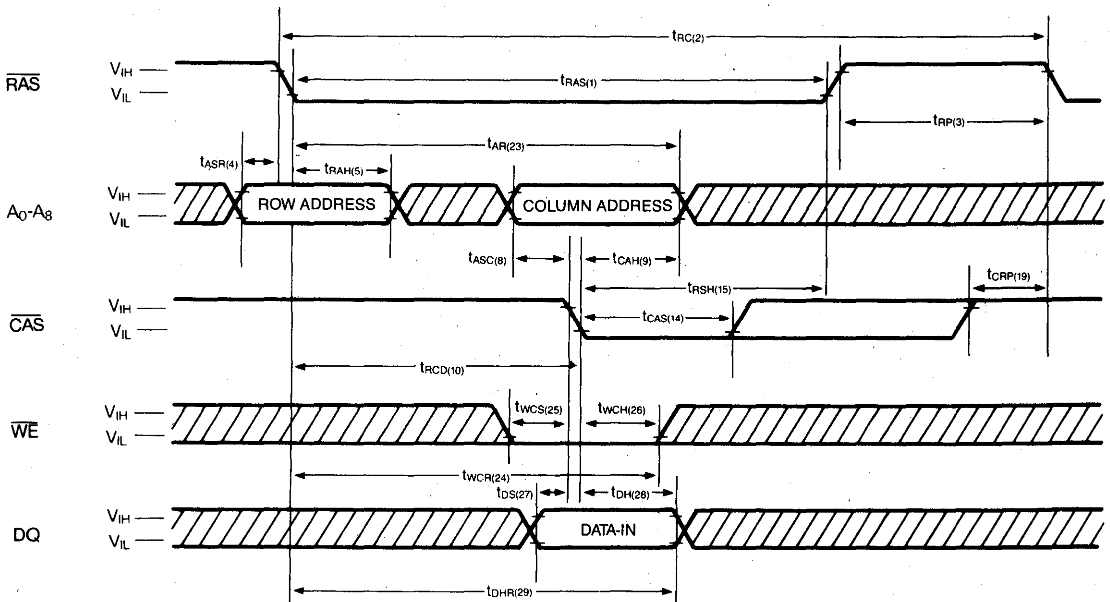
4

TIMING DIAGRAM

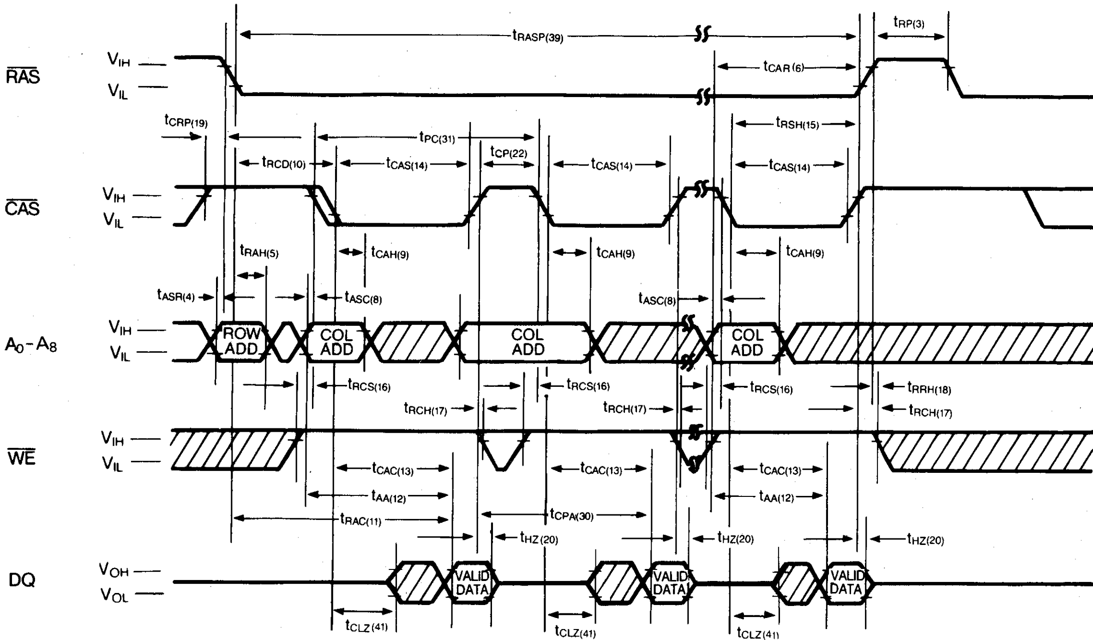
READ CYCLE



EARLY WRITE CYCLE

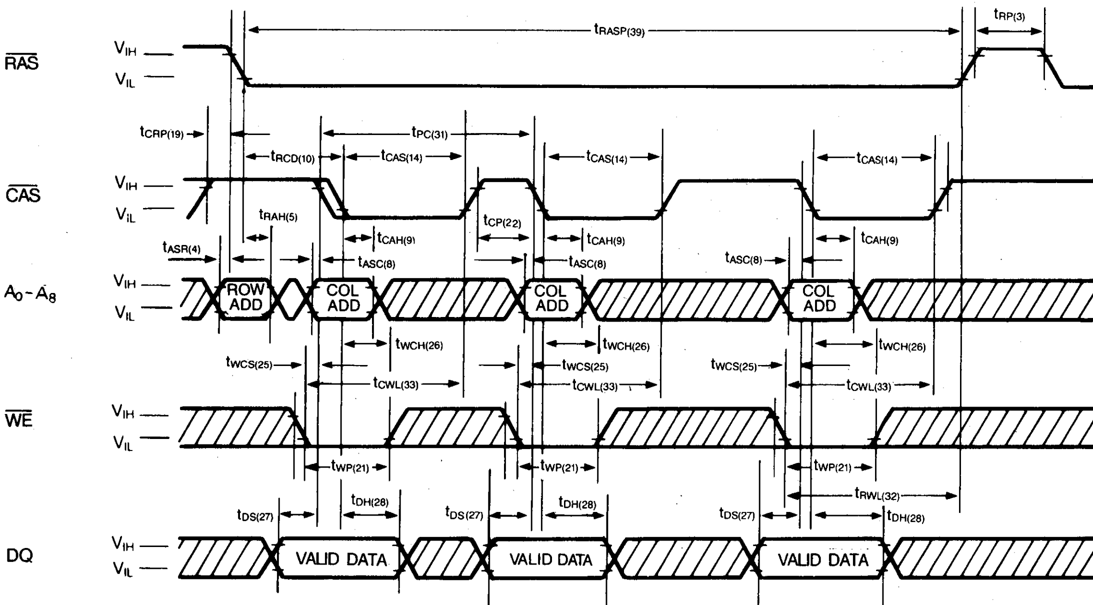


FAST PAGE MODE READ CYCLE

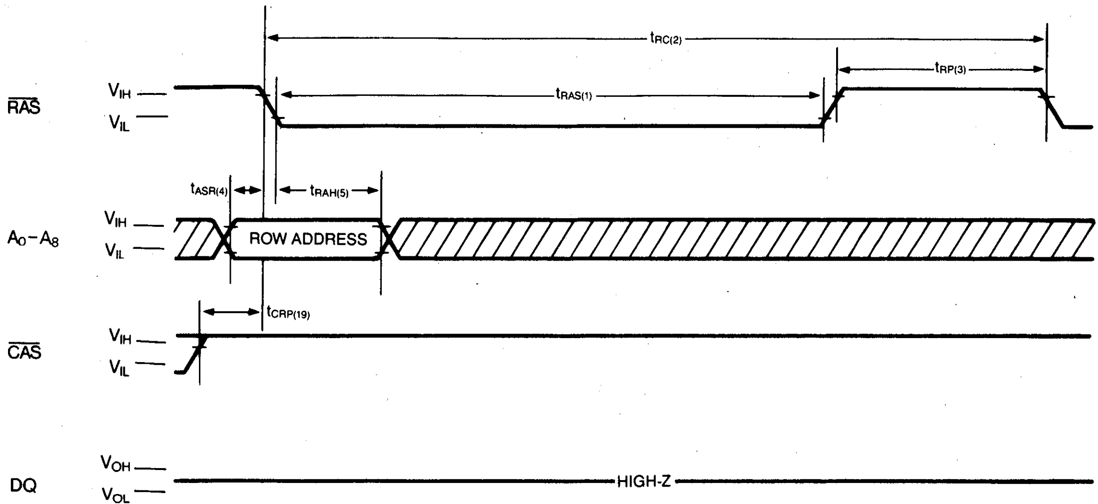


4

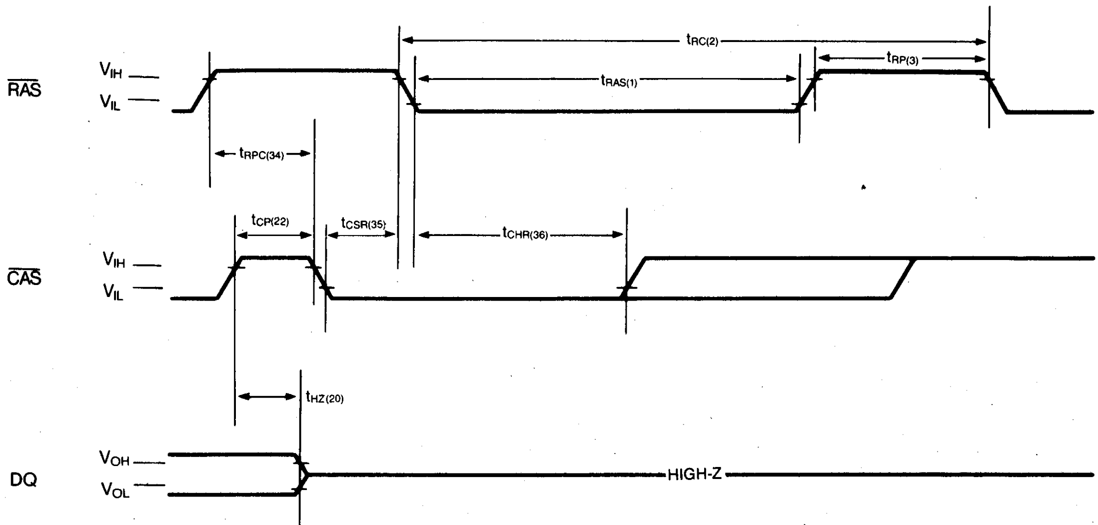
FAST PAGE MODE EARLY WRITE CYCLE



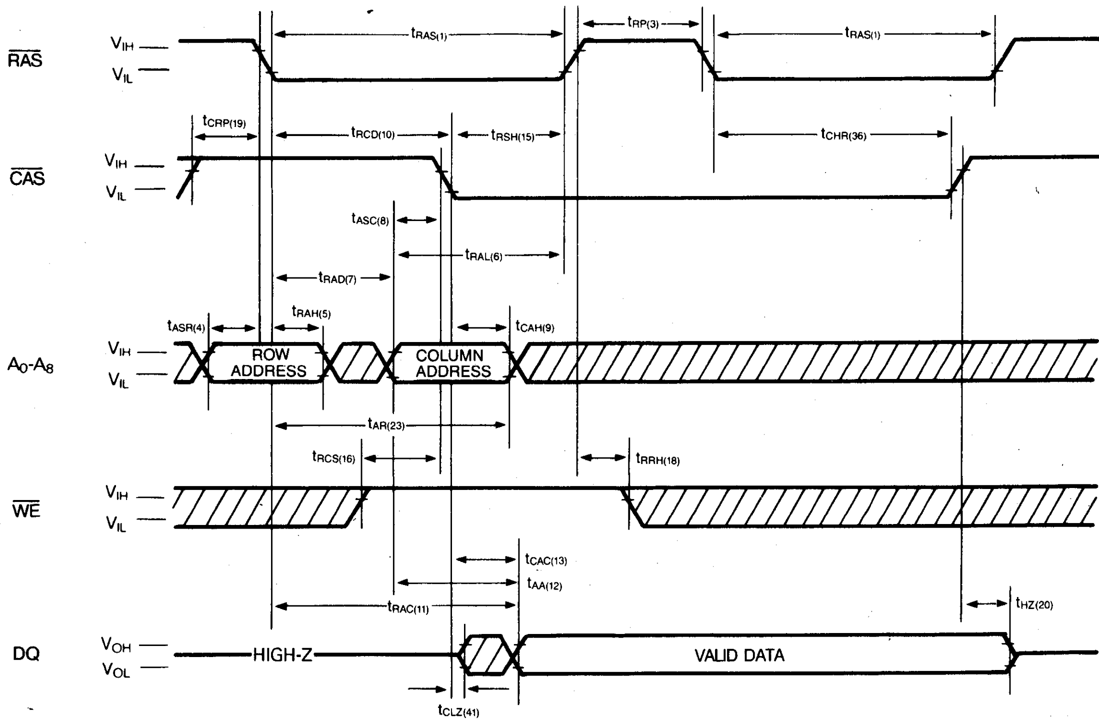
$\overline{RAS}$-ONLY REFRESH CYCLE



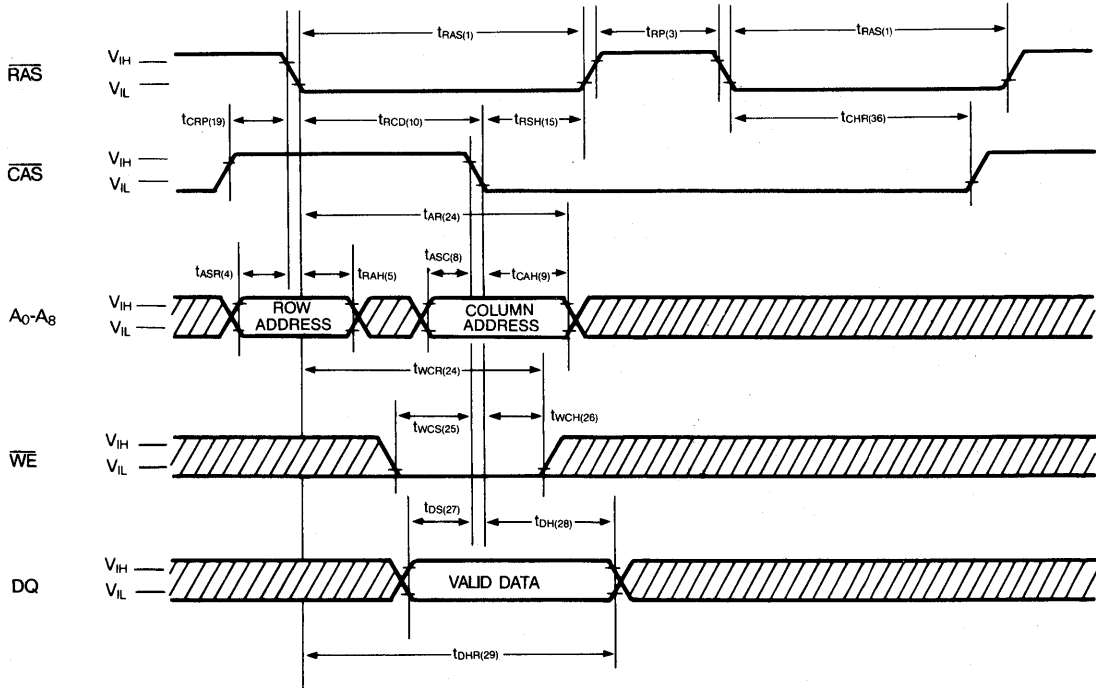
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



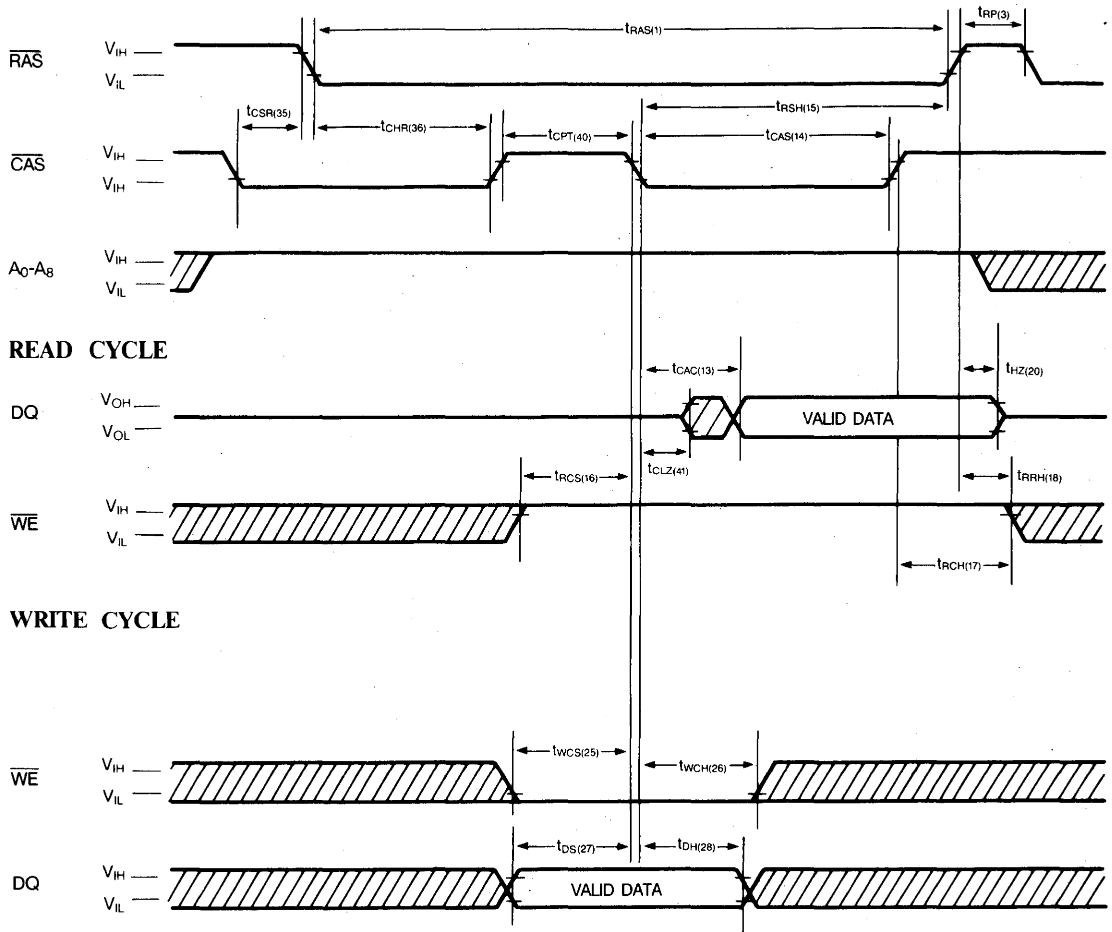
HIDDEN REFRESH CYCLE(READ)



HIDDEN REFRESH CYCLE(WRITE)

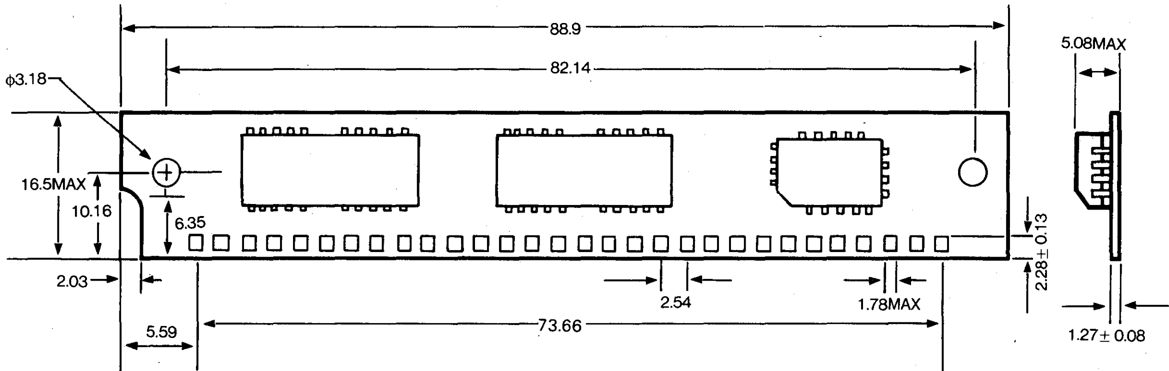


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

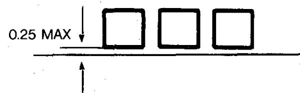


PACKAGE INFORMATION

HYM59256AM



* DETAIL OF CONTACTS



MEMO

HYM581000

1M×8-Bit CMOS DRAM MODULE

M431201B-OCT91

DESCRIPTION

The HYM581000M is a 1M words by 8bits dynamic RAM module and consists of eight HY531000J Fast Page mode CMOS DRAM in 20/26 pin SOJ package mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the 1M DRAMs.

HYM581000M is suitable for easy interchange and addition of 1M bytes memory.

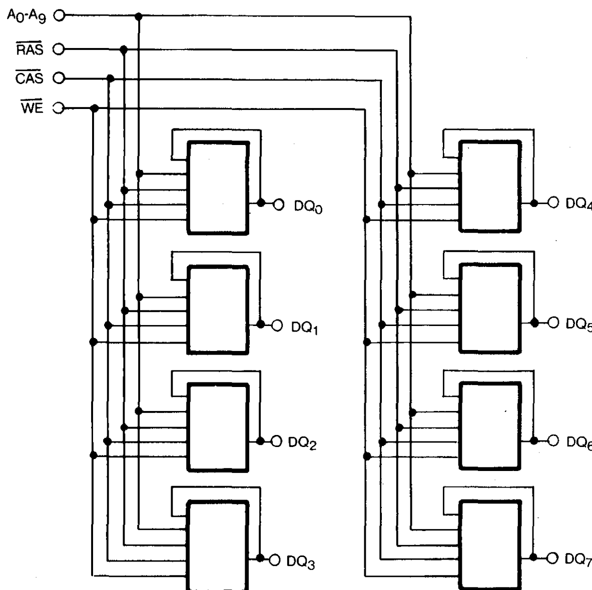
FEATURES

- Fast Page Mode operation
- Fast access time

	t_{RAC}	t_{CAC}	t_{PC}
HYM581000-60	60	20	40
HYM581000-70	70	20	40
HYM581000-80	80	20	45
HYM581000-10	100	25	55

- Single power supply of 5V± 10%
- $\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh
- Low power operating
  3.74W max (HYM581000M-60)
  3.30W max (HYM581000M-70)
  2.86W max (HYM581000M-80)
  2.42W max (HYM581000M-10)
- TTL compatible inputs and outputs
- 512 refresh cycles / 8ms

BLOCK DIAGRAM

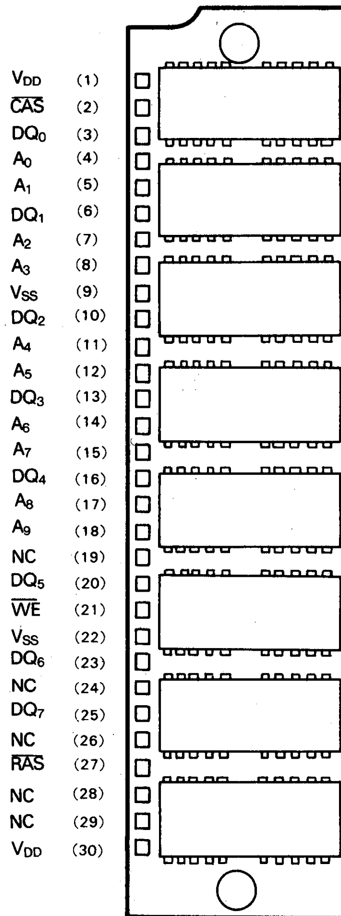


PIN NAMES

A_0-A_9	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS

HYM581000M



NOTES :
1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ0-DQ7).
2. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out(DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	4.8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM581000 MIN.	HYM581000 MAX	UNIT	NOTE
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$			80	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60		680	mA	1, 2
			−70		600		
			−80		520		
			−10		440		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\ge V_{SS}$			16	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60		680	mA	2
			−70		600		
			−80		520		
			−10		440		
I_{DD4}	V_{DD} Supply Current, Fast page mode	Minimum Cycle	−60		520	mA	1, 2
			−70		440		
			−80		360		
			−10		280		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs $\ge V_{SS}$			8	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60		680	mA	2
			−70		600		
			−80		520		
			−10		440		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :

1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions, Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in fast page mode.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HYM581000								UNIT	NOTE
			60		70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120		130		150		180		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50		50		60		70		ns	
4	t_{ASR}	Row Address Set-up Time	0		0		0		0		ns	
5	t_{RAH}	Row Address Hold Time	10		10		10		15		ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		50		ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	1
8	t_{ASC}	Column Address Set-up Time	0		0		0		0		ns	
9	t_{CAH}	Column Address Hold Time	15		15		15		20		ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	60	25	75	ns	2
11	t_{RAC}	Access Time From $\overline{RAS}$		60		70		80		100	ns	3,4,5
12	t_{AA}	Access Time From Column Address		30		35		40		50	ns	5,7
13	t_{CAC}	Access Time From $\overline{CAS}$		20		20		20		25	ns	5,6
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	20	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20		20		20		25		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		0		ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	8
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	8
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		5		ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	0	20	ns	9
21	t_{WP}	Write Command Pulse Width	15		15		15		20		ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		10		ns	
23	t_{AR}	Column Address Hold Time From $\overline{RAS}$	50		55		60		75		ns	
24	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	50		55		60		75		ns	
25	t_{WCS}	Write Command Set-up Time	0		0		0		0		ns	10
26	t_{WCH}	Write Command Hold Time	15		15		15		20		ns	
27	t_{DS}	Data-In Set-up Time	0		0		0		0		ns	11
28	t_{DH}	Data-In Hold Time	15		15		15		20		ns	11
29	t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	50		55		60		75		ns	
30	t_{CPA}	Access Time From $\overline{CAS}$ Precharge		35		35		40		50	ns	5,12
31	t_{PC}	Fast page mode Cycle time	40		40		45		55		ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		20		25		ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		20		25		ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5		5		5		5		ns	

#	SYMBOL	PARAMETER	HYM581000								UNIT	NOTE
			60		70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15		15		15		20		ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	3	50	ns	13,14
38	t_{CLZ}	$\overline{CAS}$ to output in Low-z	0		0		0		0		ns	5
39	t_{REF}	Refresh Interval(512 Cycle)		8		8		8		8	ms	15
40	t_{RASP}	Fast page Mode $\overline{RAS}$ Pulse Width	60		70		80		100		ns	
41	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40		40		40		50		ns	

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then the access time is controlled by t_{CAC}.
3. Assume $t_{RAD} \le t_{RAD}$(max.). If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max.).
4. Assume $t_{RCD} \le t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max.).
5. Measured with a load equivalent to two TTL loads and 100 pF.
6. Assumes that $t_{RCD} \ge t_{RCD}$(max.) and $t_{RAD} \le t_{RAD}$(max.).
7. Assumes that $t_{RCD} \le t_{RCD}$(max.) and $t_{RAD} \ge t_{RAD}$(max.).
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{OFF} and t_{OH} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
10. t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as a electrical characteristic only. If $t_{WCS} \ge t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$
12. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{CPA}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max.).
14. AC measurements assume t_T=5ns.
15. An initial pause of 200μs is required after power-up and followed at least 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-only refresh). 8 initialization cycles are required after extended period of bias without clocks.

CAPACITANCE

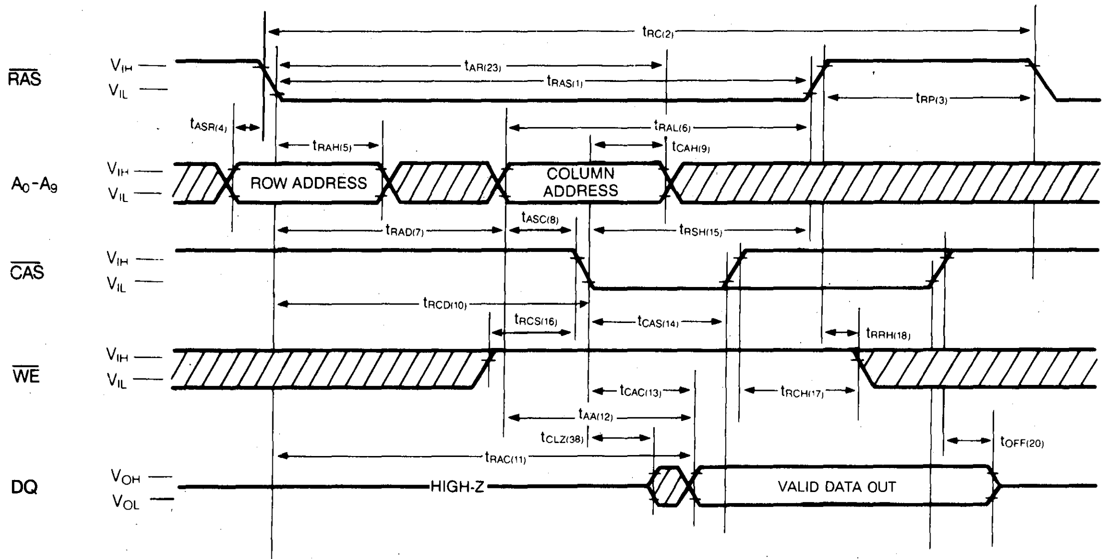
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance(A_0-A_9, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)		55	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)		15	pF

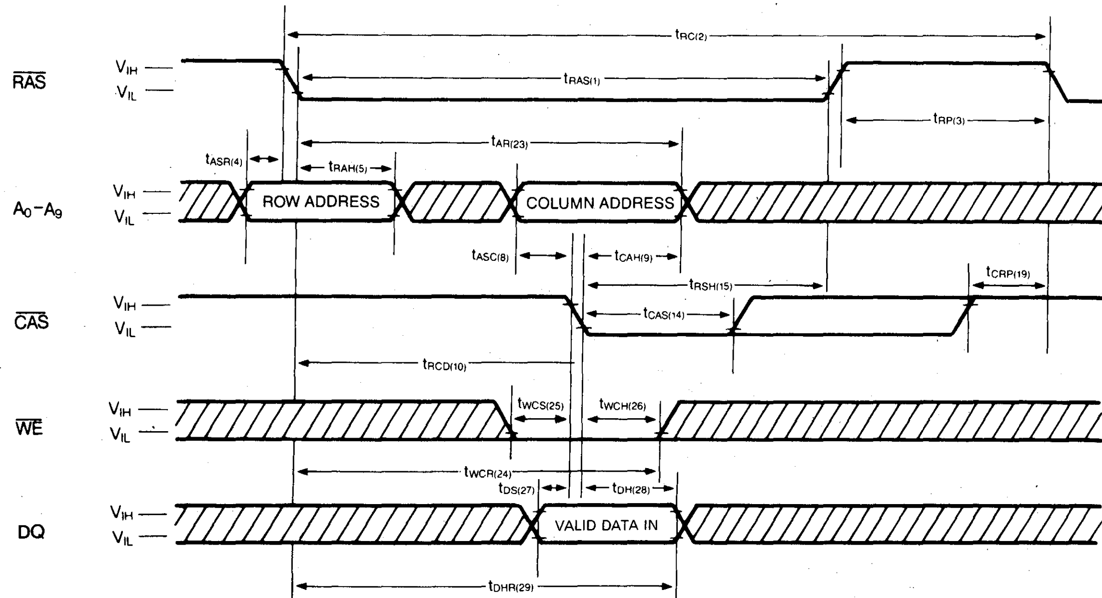
4

TIMING DIAGRAM

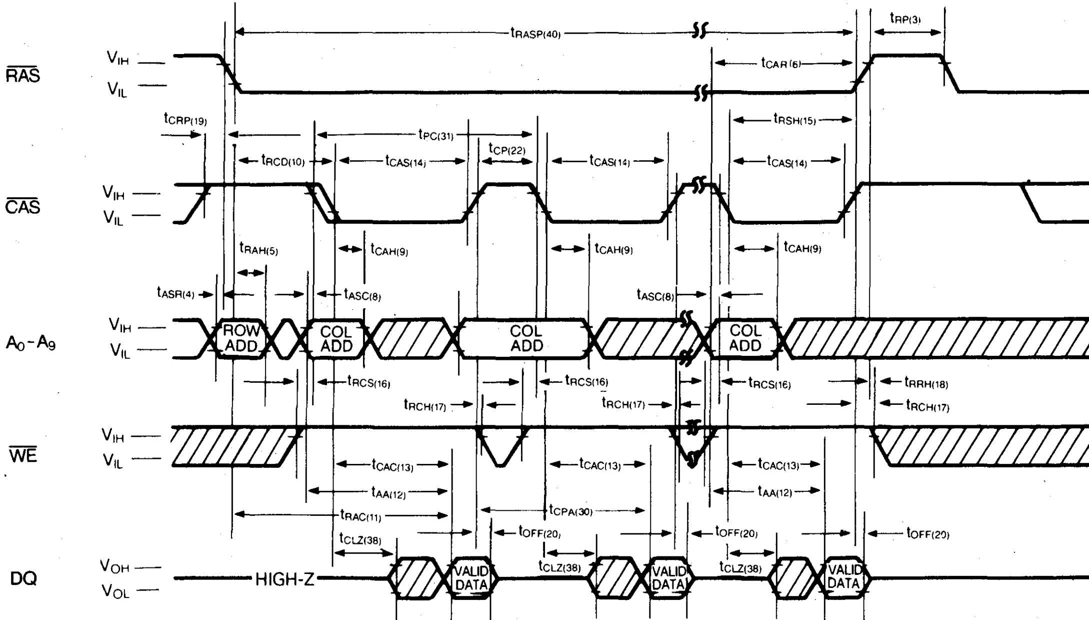
READ CYCLE



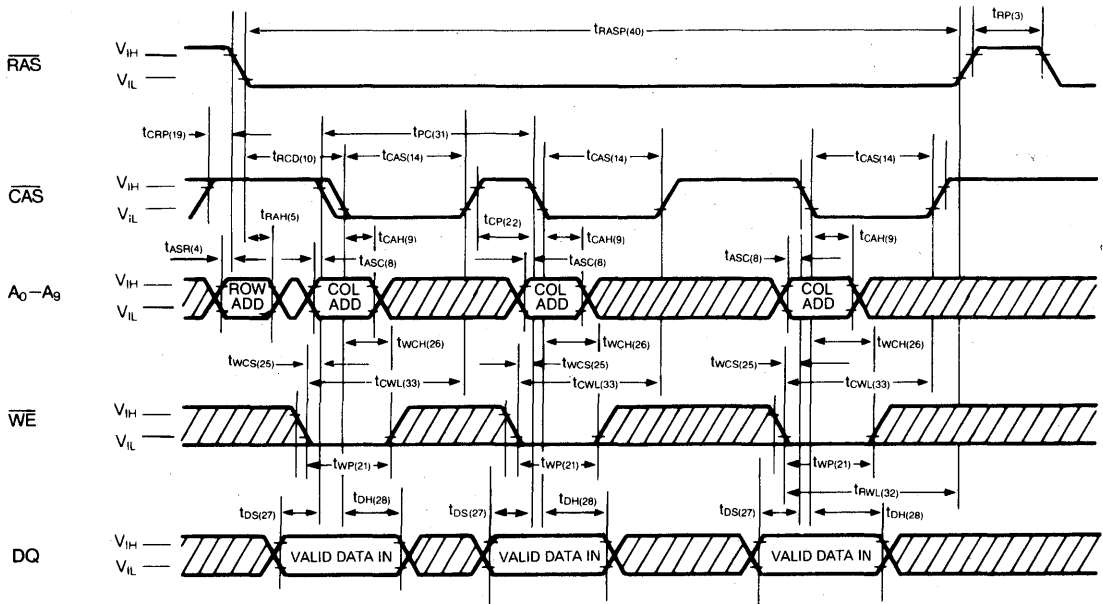
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

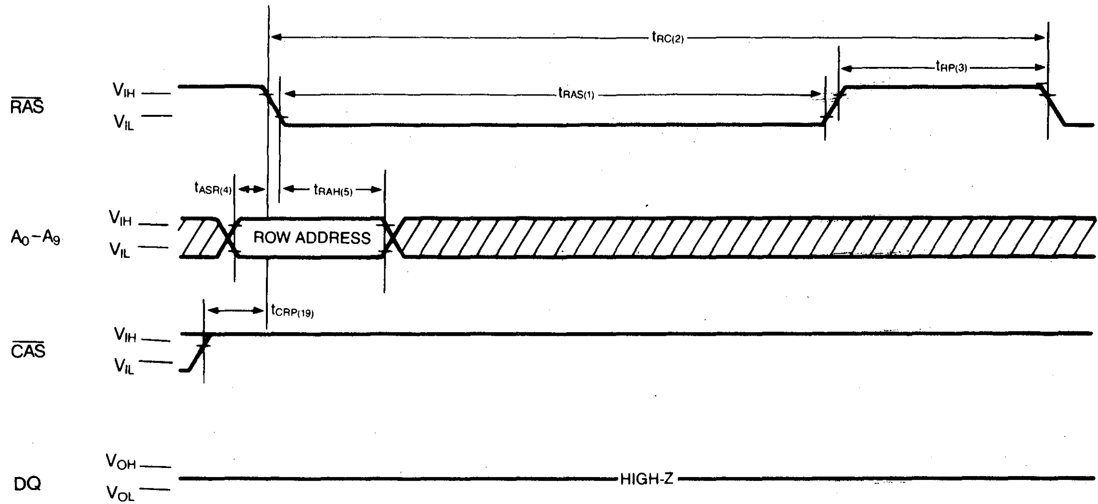


FAST PAGE MODE EARLY WRITE CYCLE

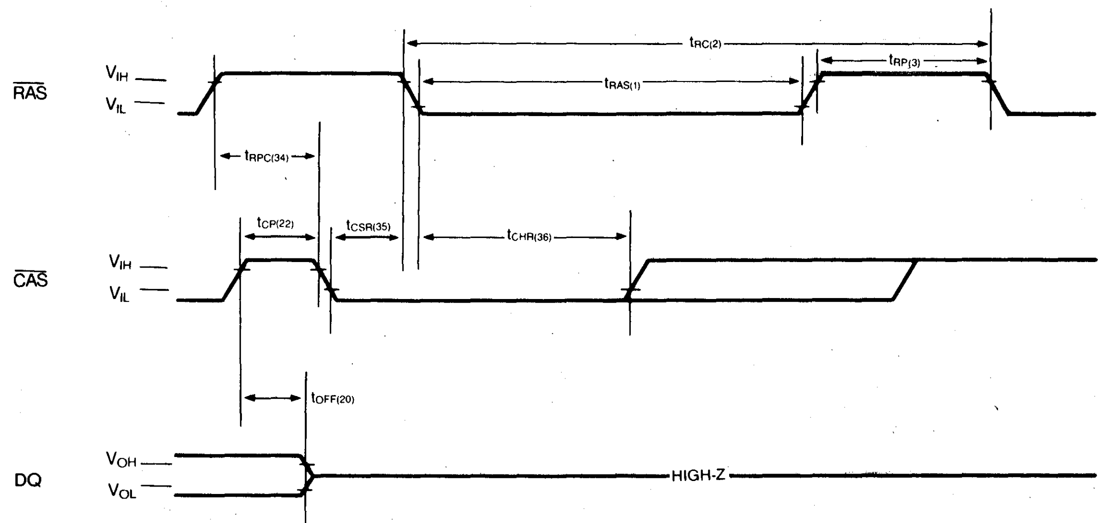


4

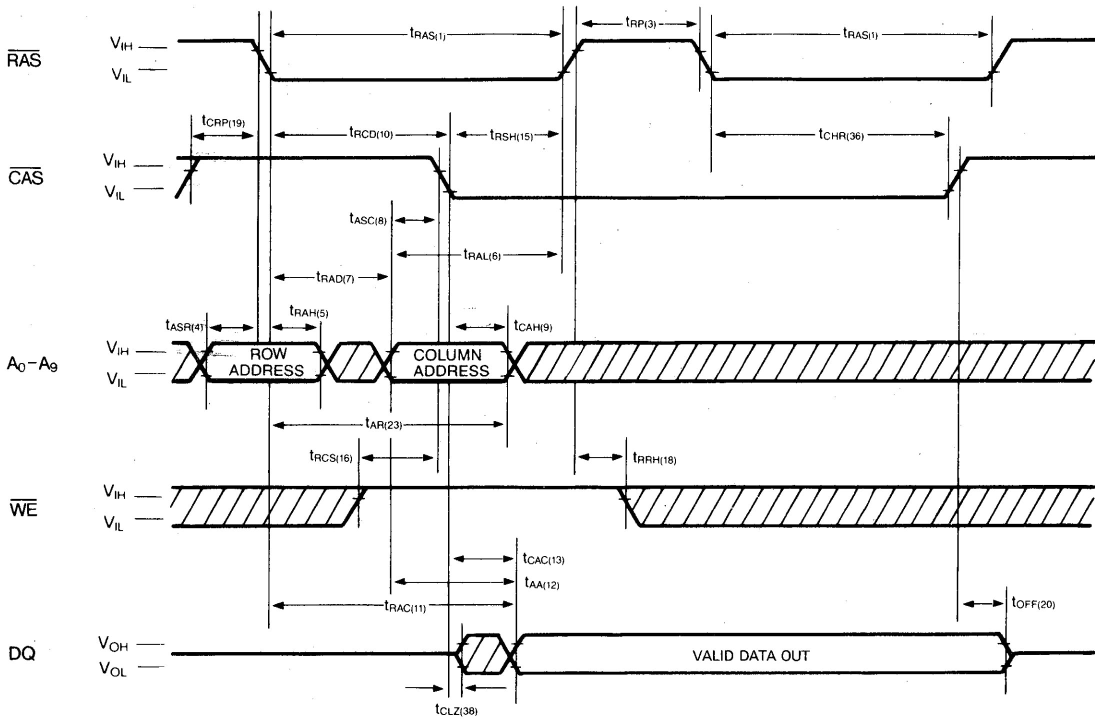
$\overline{RAS}$-ONLY REFRESH CYCLE



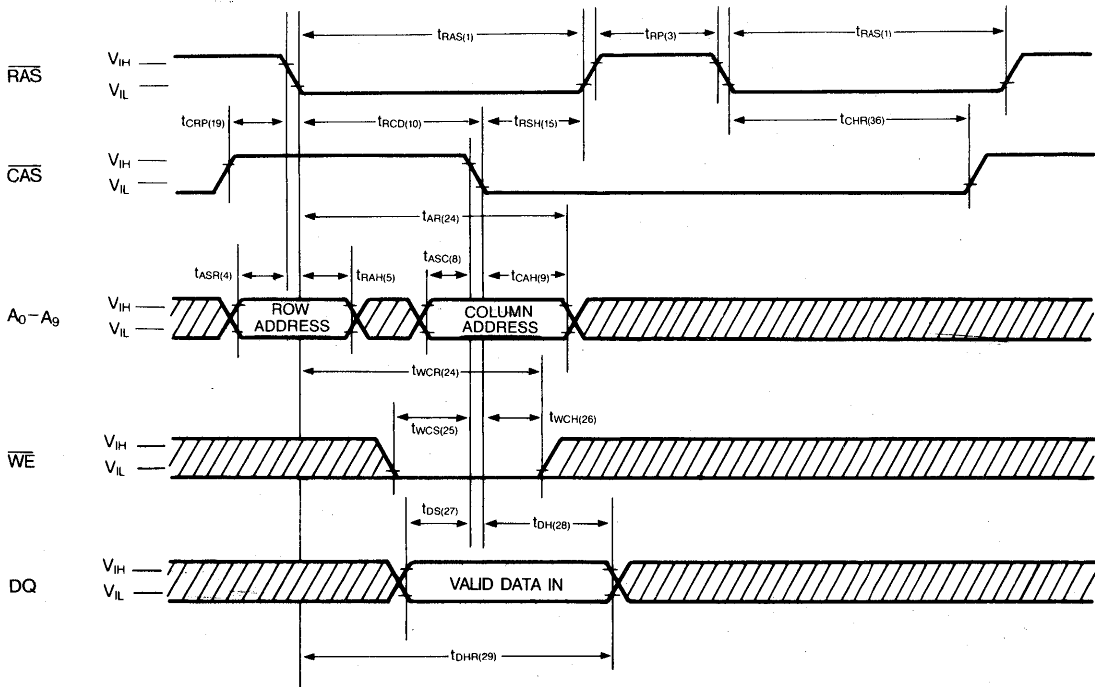
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)

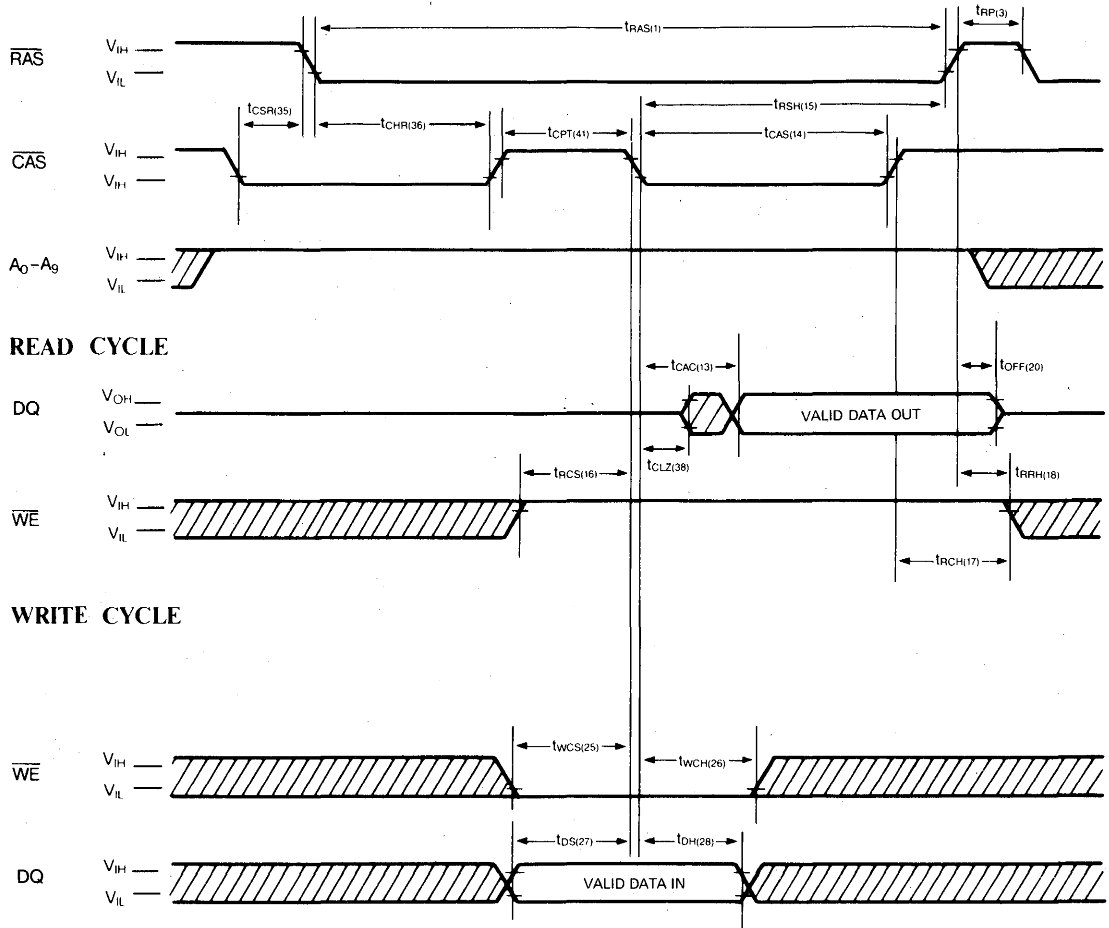


HIDDEN REFRESH CYCLE (WRITE)



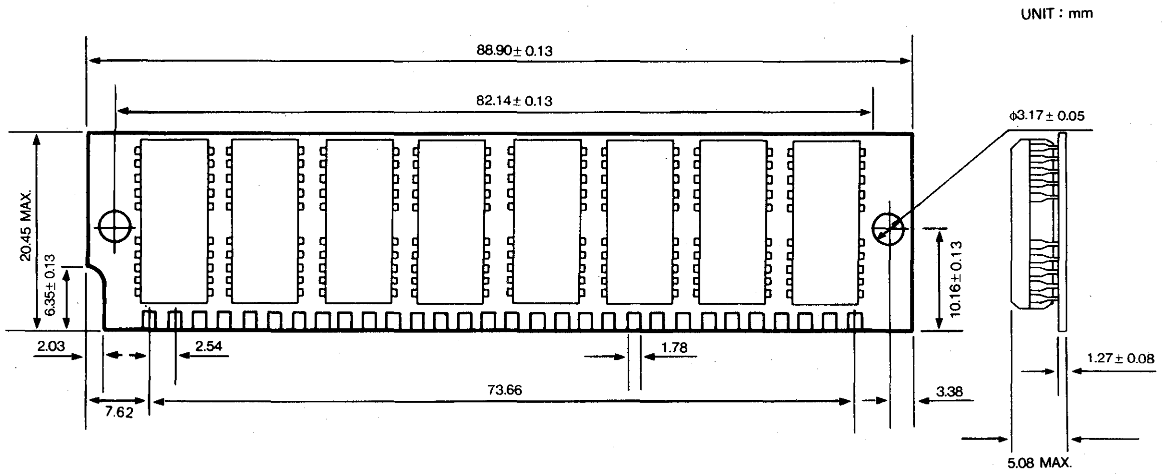
4

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

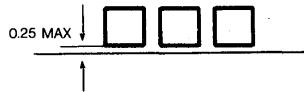


PACKAGE INFORMATION

HYM581000M



* DETAIL OF CONTACTS



4

MEMO

HYM581000A

1M×8-Bit CMOS DRAM MODULE

M471202A-JAN92

DESCRIPTION

The HYM581000AM is a 1M words by 8bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of two HY514400J in 20/26 pin SOJ mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM581000AM is a socket type single-in line module suitable for easy interchange and addition of 1M bytes memory.

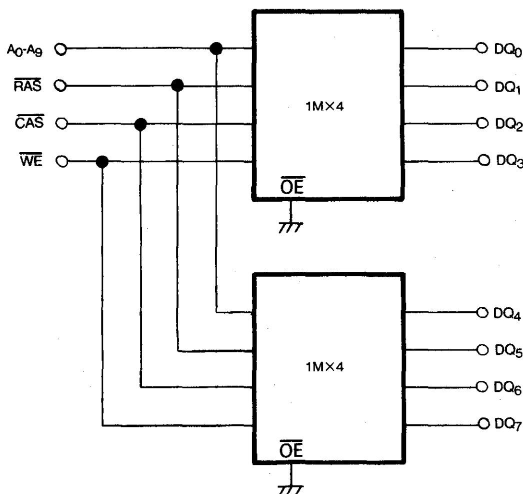
FEATURES

- Fast Page Mode operation
- Fast Access Time

	t_{RAC}	t_{CAC}	t_{PC}
HYM581000AM-70	70	20	50
HYM581000AM-80	80	25	55
HYM581000AM-10	100	25	60

- Single power supply of 5V± 10%
- $\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh.
- Low power operating
  1.05W max (HYM581000AM-70)
  0.94W max (HYM581000AM-80)
  0.83W max (HYM581000AM-10)
- TTL compatible inputs and outputs
- 1024 refresh cycles/16ms

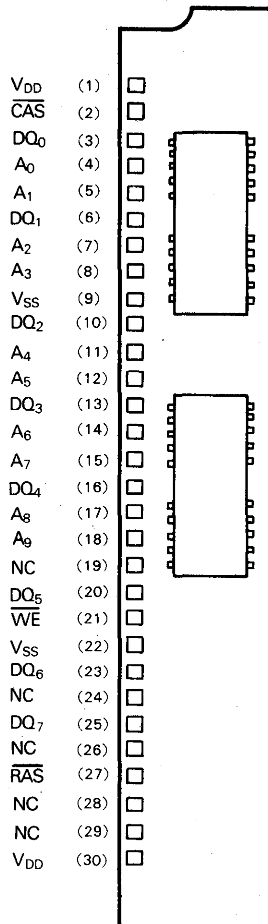
BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS



NOTES :

1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
2. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	1.2	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM581000AM		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		–	20	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min)	−70	–	190	mA	1
			−80	–	170		
			−10	–	150		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\geq V_{SS}$		–	4	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−70	–	190	mA	
			−80	–	170		
			−10	–	150		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−70	–	160	mA	1
			−80	–	140		
			−10	–	120		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs $\geq V_{SS}$		–	2	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−70	–	190	mA	
			−80	–	170		
			−10	–	150		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1, 2, 3

#	SYMBOL	PARAMETER	HYM581000AM						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
3	t_{RP}	$\overline{\text{RAS}}$ Precharge Time	50	–	60	–	70	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
6	t_{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	35	–	40	–	45	–	ns	
7	t_{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	15	35	15	40	20	55	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
10	t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	20	50	20	55	25	75	ns	8
11	t_{RAC}	Access Time from $\overline{\text{RAS}}$	–	70	–	80	–	100	ns	4,8,9
12	t_{AA}	Access Time from Column Address	–	35	–	40	–	45	ns	4,9
13	t_{CAC}	Access Time from $\overline{\text{CAS}}$	–	20	–	25	–	25	ns	4,8
14	t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	20	10K	25	10K	25	10K	ns	
15	t_{RSH}	$\overline{\text{RAS}}$ Hold Time	25	–	25	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	–	5	–	5	–	ns	
20	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
22	t_{CP}	$\overline{\text{CAS}}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time from $\overline{\text{RAS}}$	55	–	60	–	80	–	ns	
24	t_{WCR}	Write Command Hold Time from $\overline{\text{RAS}}$	55	–	60	–	80	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
27	t_{DS}	Data In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data In Hold Time	15	–	15	–	20	–	ns	7

#	SYMBOL	PARAMETER	HYM581000AM						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	55	–	60	–	80	–	ns	
30	t_{CPA}	Access Time from Column Precharge	–	45	–	50	–	55	ns	4
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	50	–	55	–	60	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	30	–	30	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	70	100K	80	100K	100	100K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time (CBR Counter Test Cycle)	40	–	40	–	50	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	4
42	t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
43	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

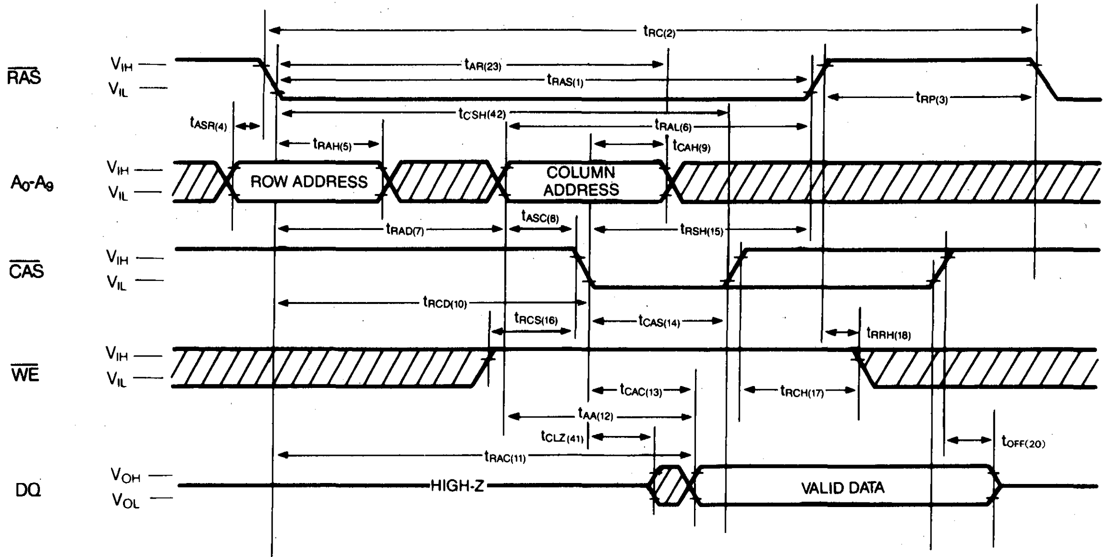
CAPACITANCE

(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

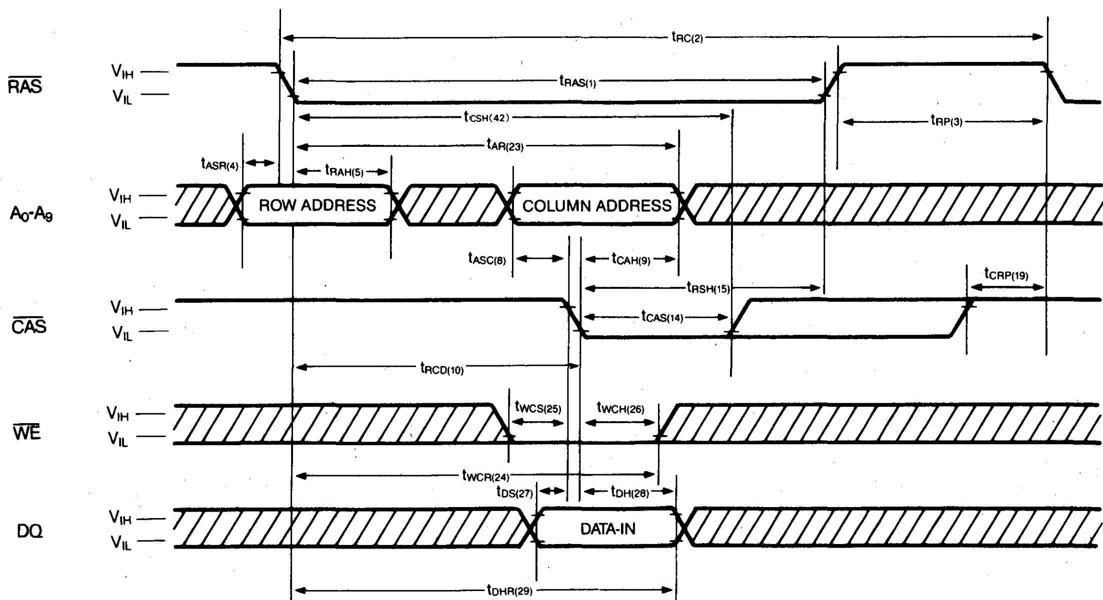
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance(A_0-A_9, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	25	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF

TIMING DIAGRAM

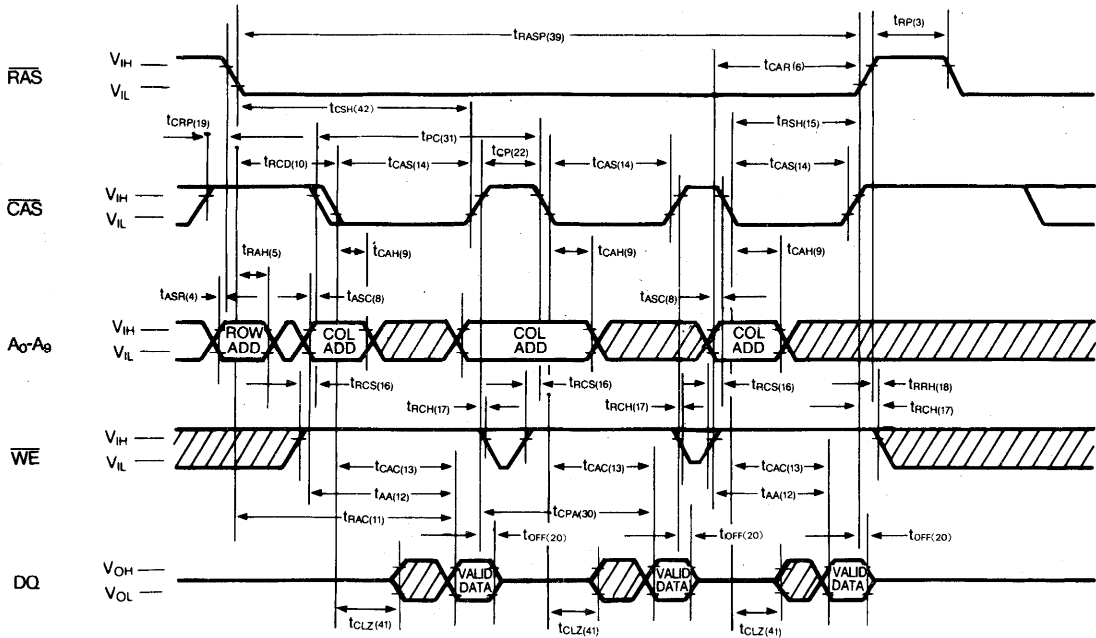
READ CYCLE



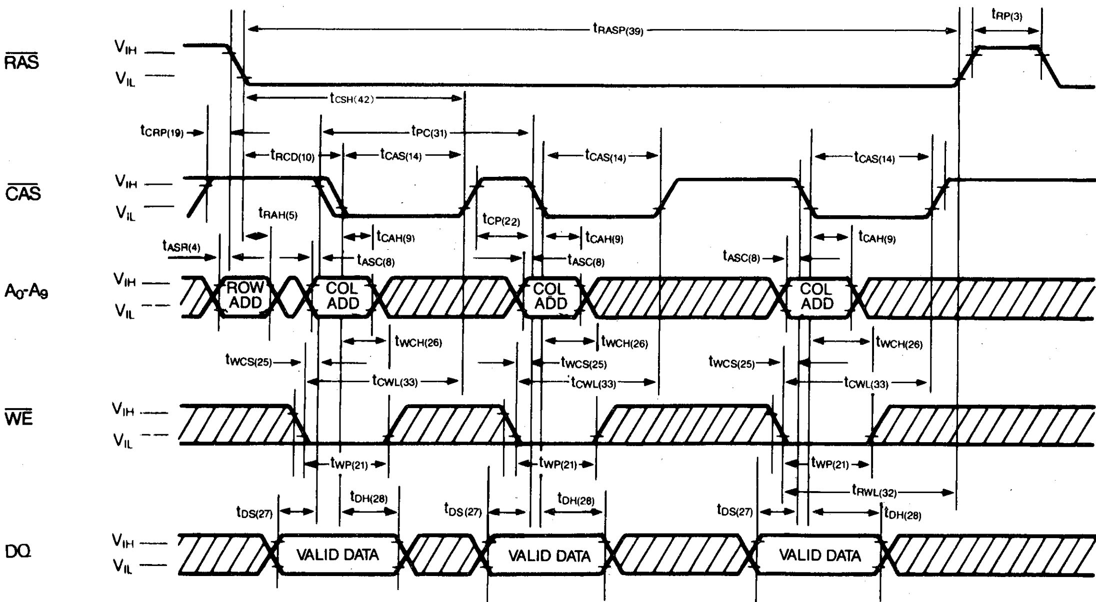
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

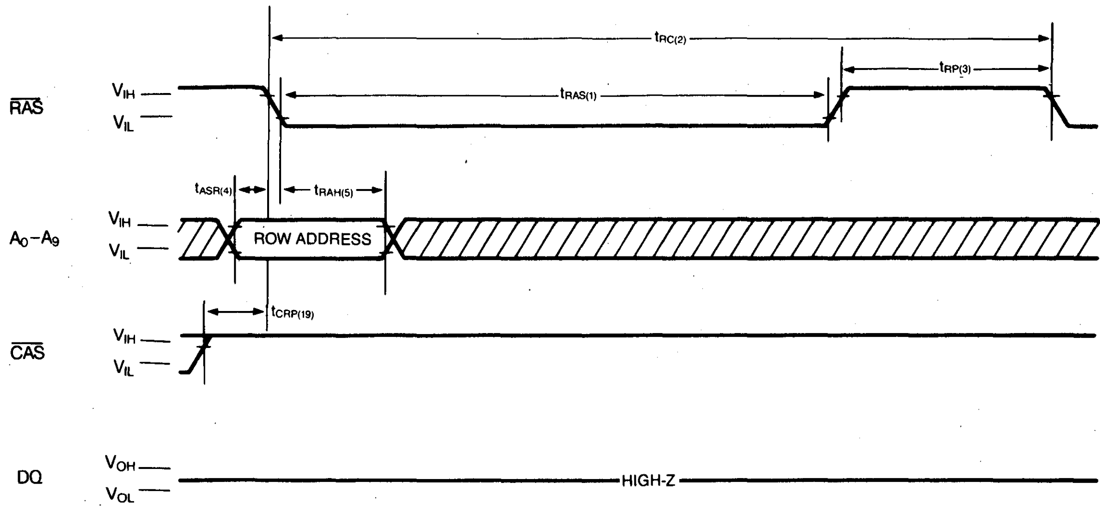


FAST PAGE MODE EARLY WRITE CYCLE

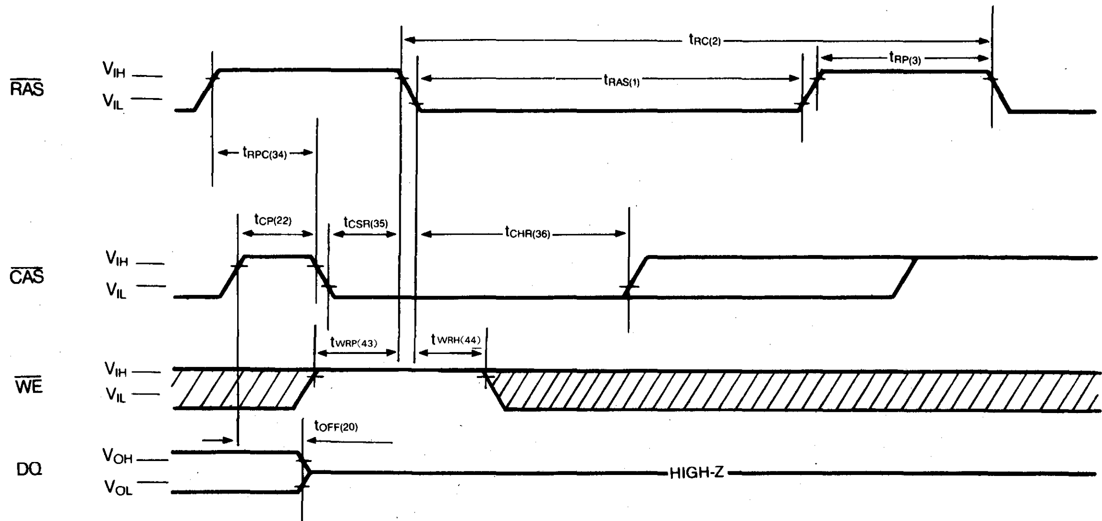


4

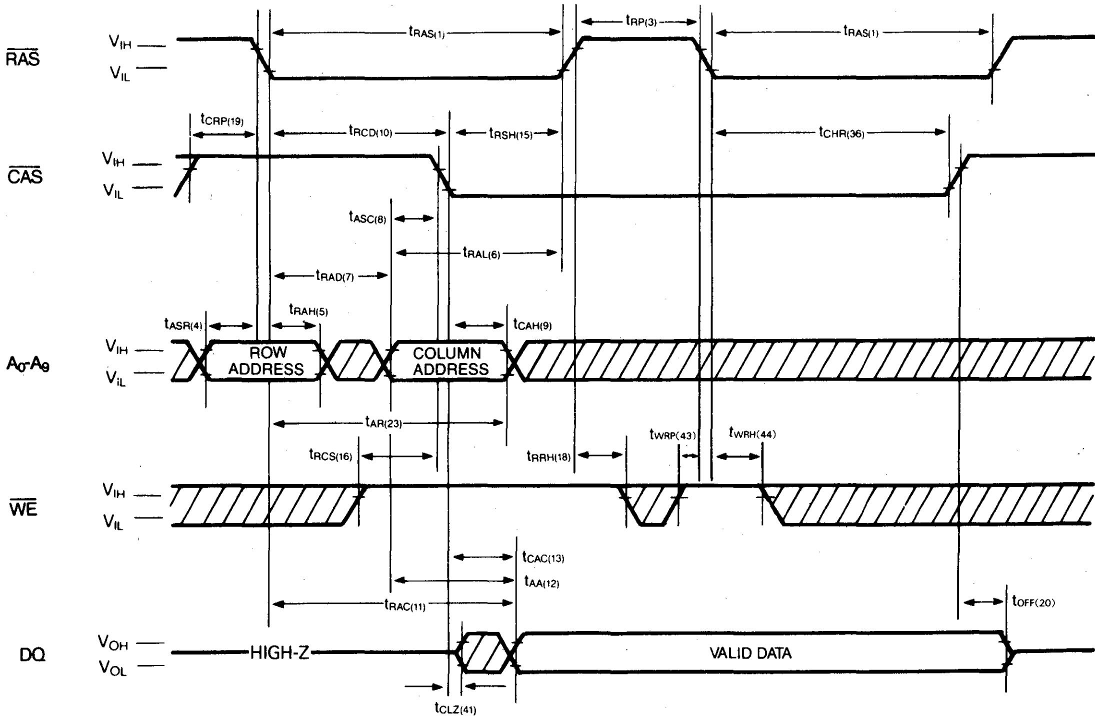
$\overline{RAS}$-ONLY REFRESH CYCLE



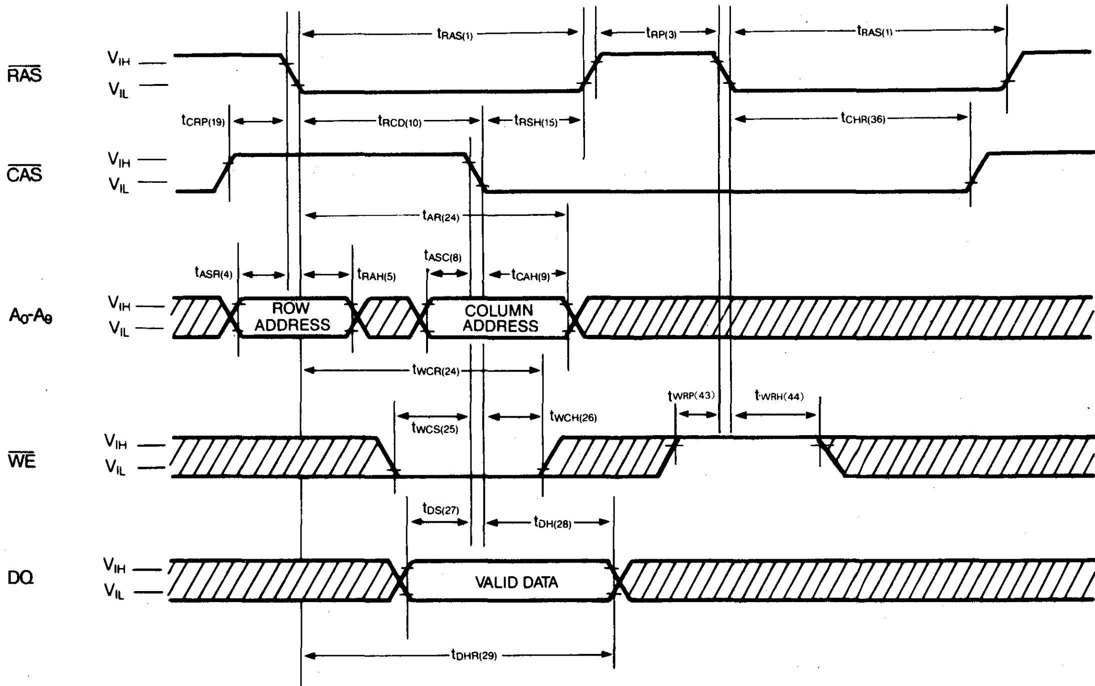
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE(READ)

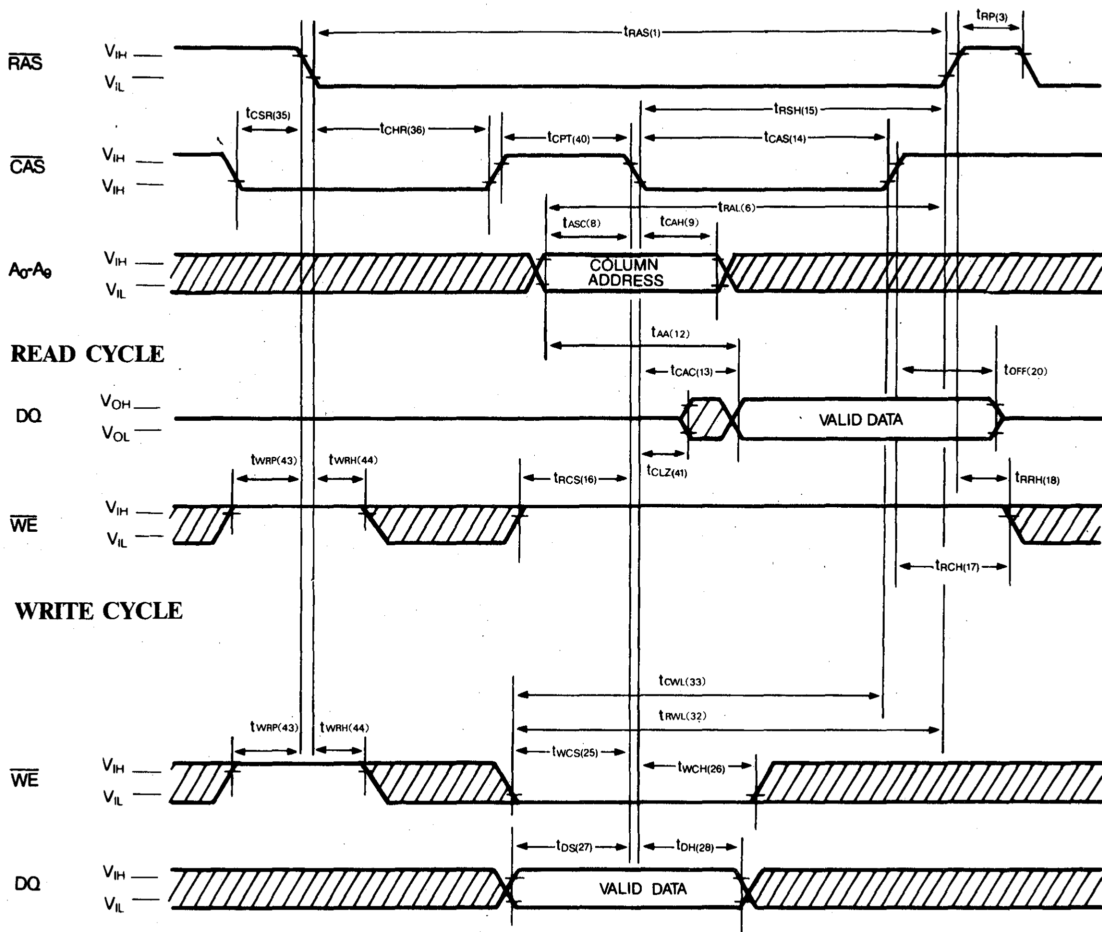


HIDDEN REFRESH CYCLE(WRITE)



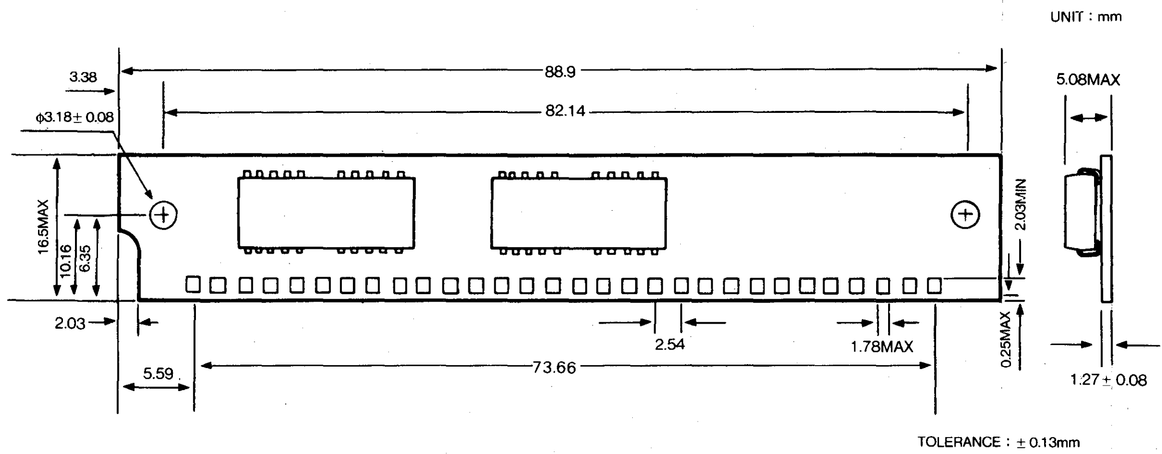
4

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



PACKAGE INFORMATION

HYM581000AM



* DETAIL OF CONTACTS

0.25 MAX

MEMO

PRELIMINARY

HYUNDAI SEMICONDUCTOR

HYM581000B

1M×8-Bit CMOS DRAM MODULE

M4C1200A-MAR92

DESCRIPTION

The HYM581000BM is a 1M words by 8bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of two HY514400AJ in 20/26 pin SOJ mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM581000BM is a socket type single-in line module suitable for easy interchange and addition of 1M bytes memory.

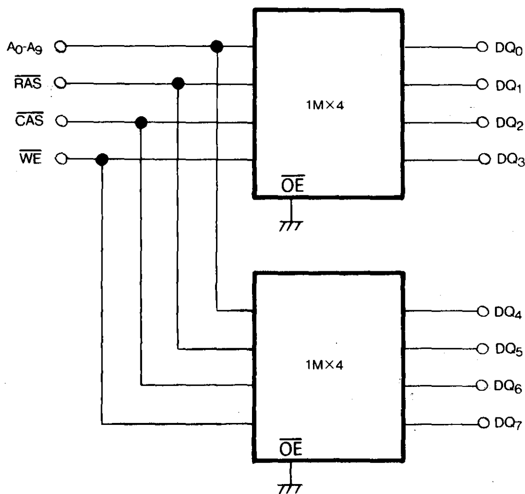
FEATURES

- Fast Page Mode operation
- Fast Access Time

	t_{RAC}	t_{CAC}	t_{PC}
HYM581000BM-60	60	20	40
HYM581000BM-70	70	20	45
HYM581000BM-80	80	25	55

- Single power supply of 5V± 10%
- $\overline{CAS}$-Before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden Refresh.
- Low power operating
  1.21W max (HYM581000BM-60)
  1.10W max (HYM581000BM-70)
  0.99W max (HYM581000BM-80)
- TTL compatible inputs and outputs
- 1024 refresh cycles/16ms

BLOCK DIAGRAM

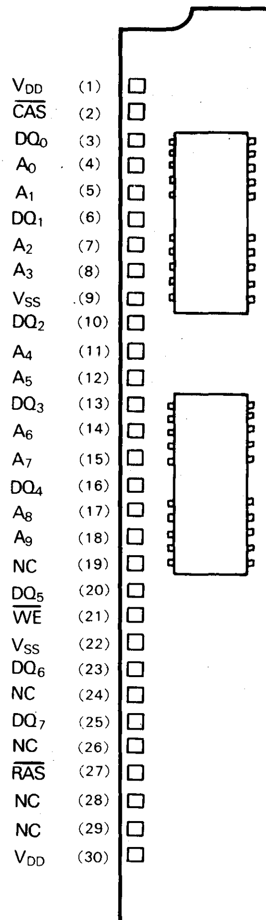


PIN NAMES

A_0-A_9	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

4

PIN CONNECTIONS



NOTES :
1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
2. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	1.54	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS
(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM581000BM MIN.	HYM581000BM MAX.	UNIT	NOTE
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		–	20	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min)	−60	–	220	mA	1
			−70	–	200		
			−80	–	180		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\geq V_{SS}$		–	4	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60	–	220	mA	
			−70	–	200		
			−80	–	180		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−60	–	140	mA	1
			−70	–	120		
			−80	–	100		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS}=V_{IH}$, other inputs $\geq V_{SS}$		–	2	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60	–	220	mA	
			−70	–	200		
			−80	–	180		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1. 2. 3

#	SYMBOL	PARAMETER	HYM581000BM						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
3	t_{RP}	$\overline{RAS}$ Prechange Time	50	–	50	–	60	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	55	ns	8
11	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	4,8,9
12	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	4,9
13	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	4,8
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
20	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
24	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
27	t_{DS}	Data In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data In Hold Time	15	–	15	–	15	–	ns	7

#	SYMBOL	PARAMETER	HYM581000BM						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
30	t_{CPA}	Access Time from Column Precharge	–	35	–	40	–	50	ns	4
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	40	–	45	–	55	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	200K	70	200K	80	200K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	30	–	35	–	40	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	4
42	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
43	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :
1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

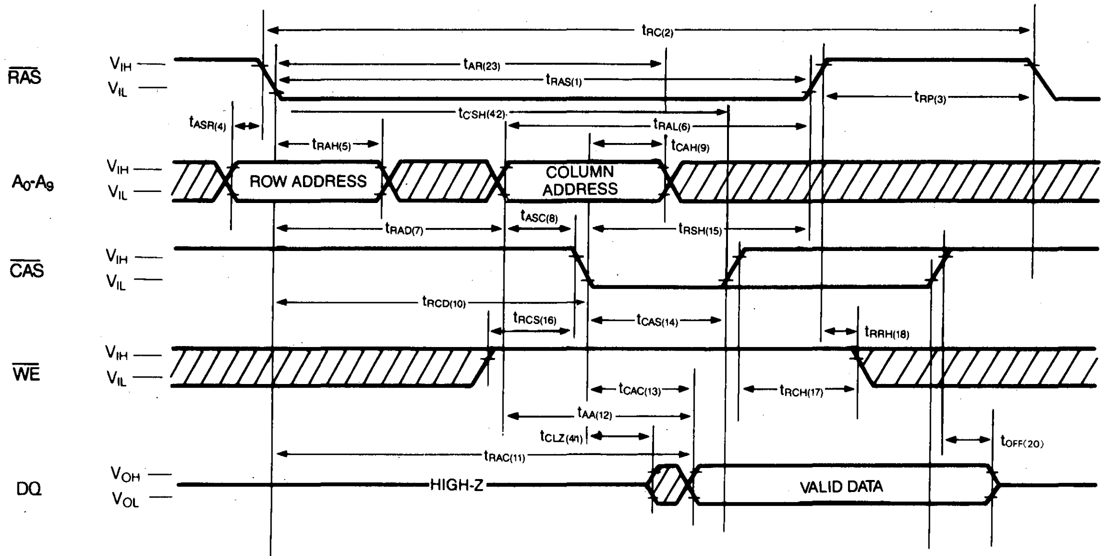
CAPACITANCE

(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

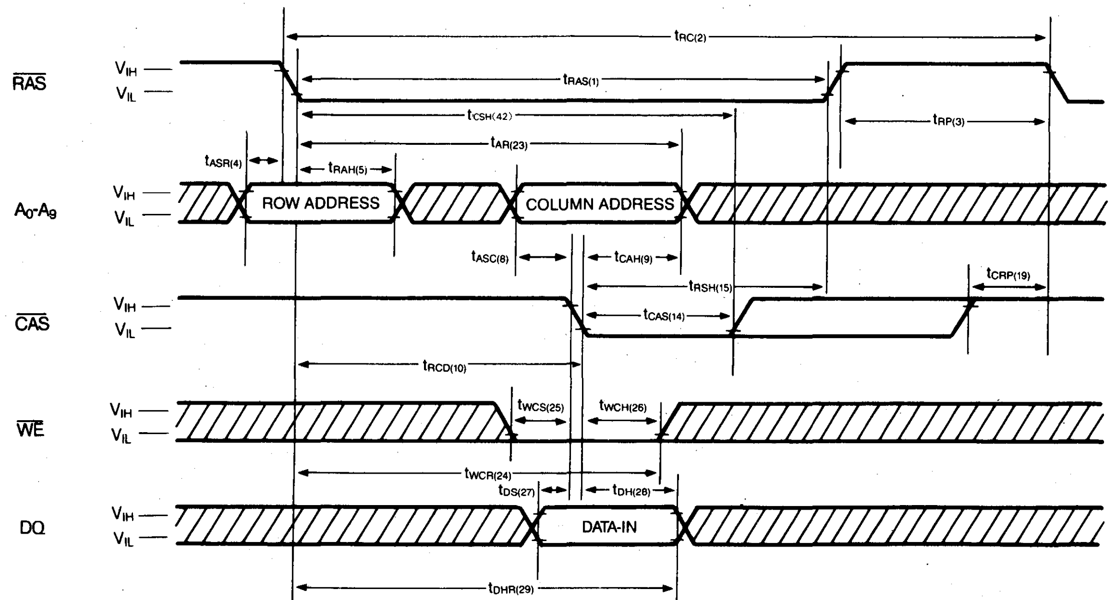
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance(A_0-A_9, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	25	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF

TIMING DIAGRAM

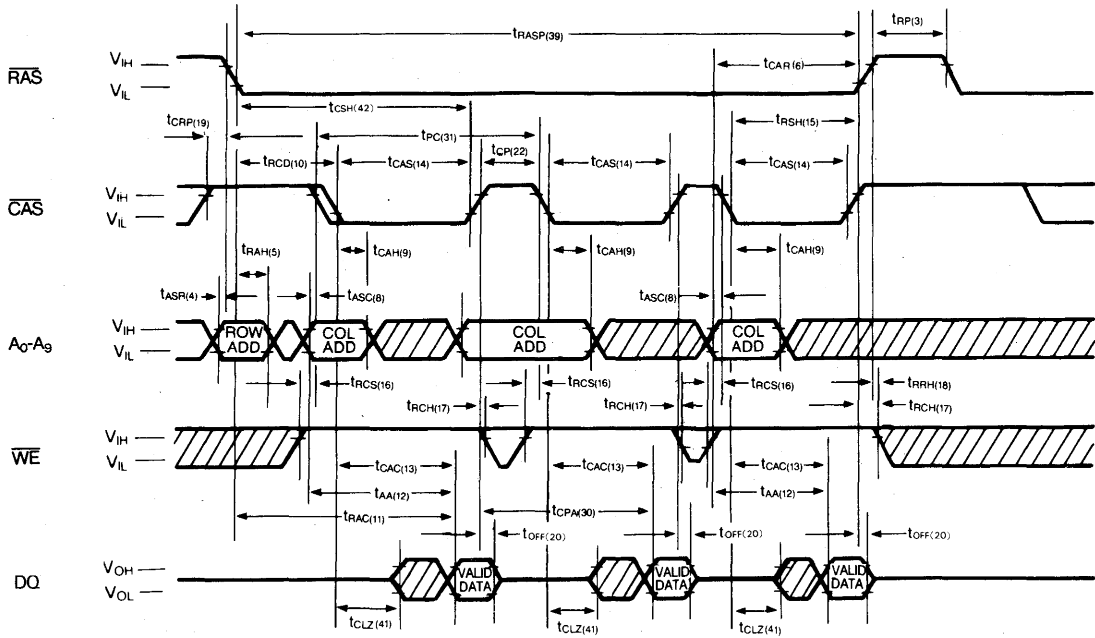
READ CYCLE



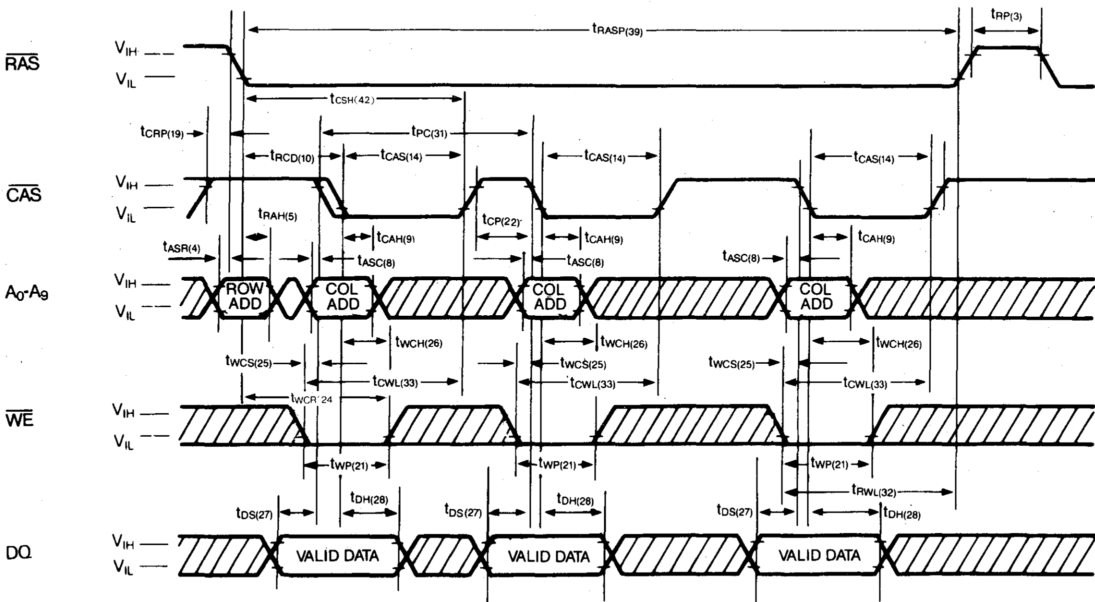
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

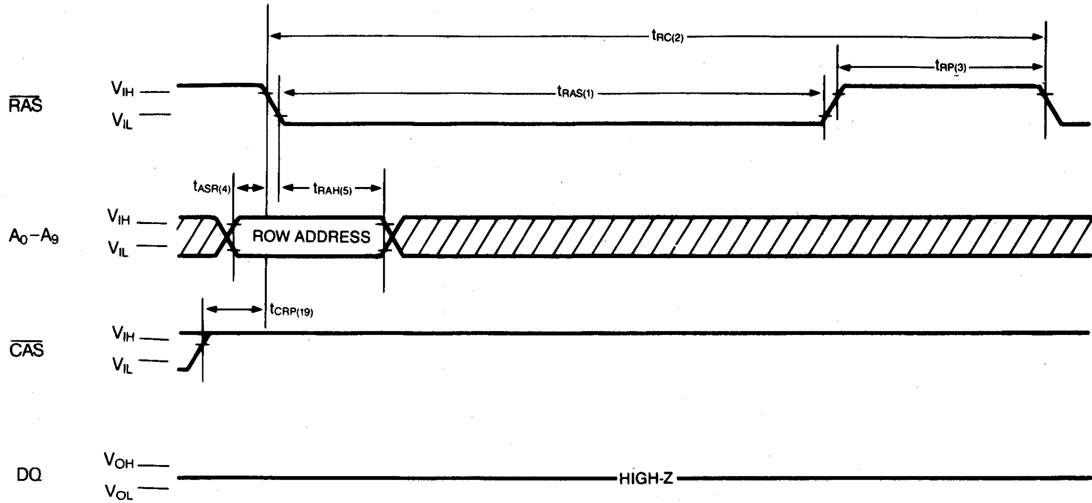


FAST PAGE MODE EARLY WRITE CYCLE

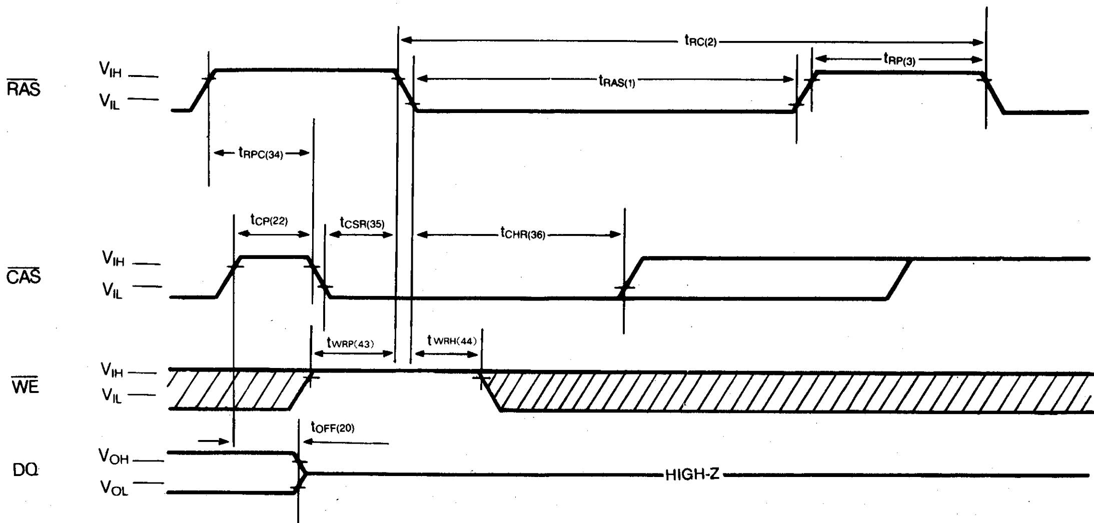


4

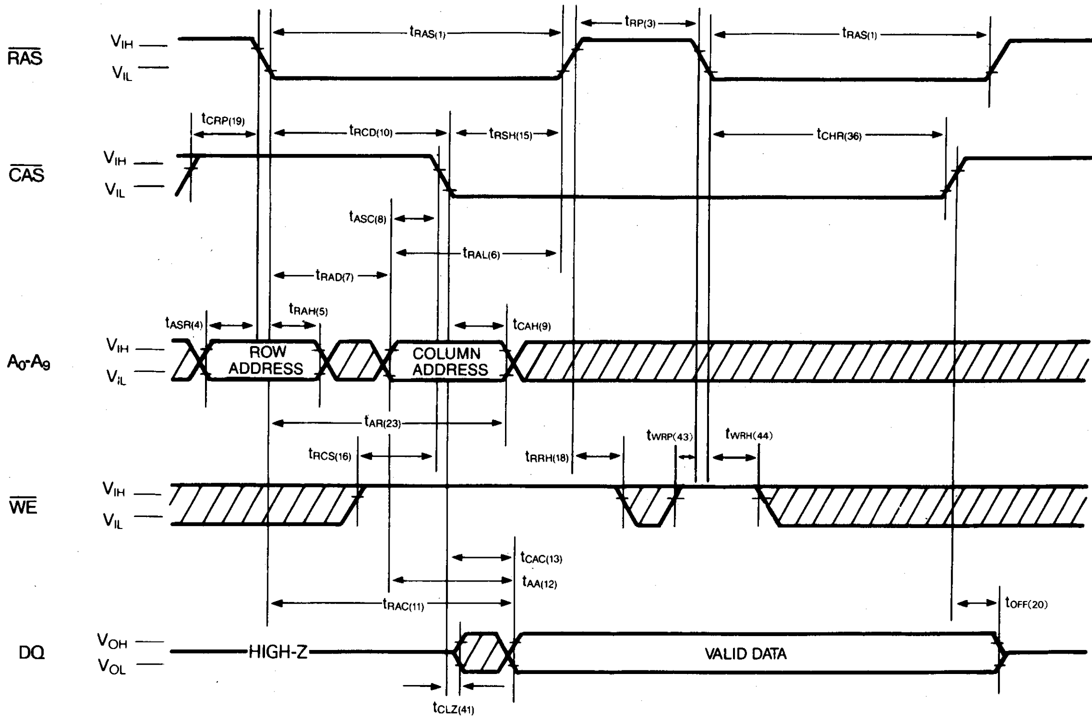
RAS-ONLY REFRESH CYCLE



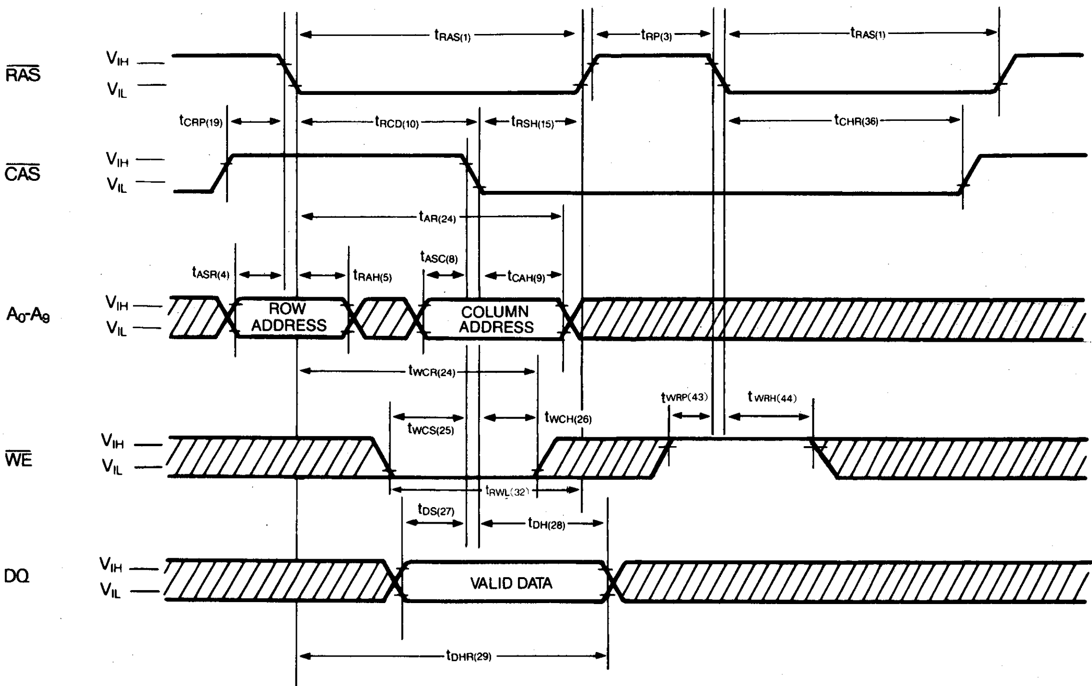
CAS-BEFORE-RAS REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)

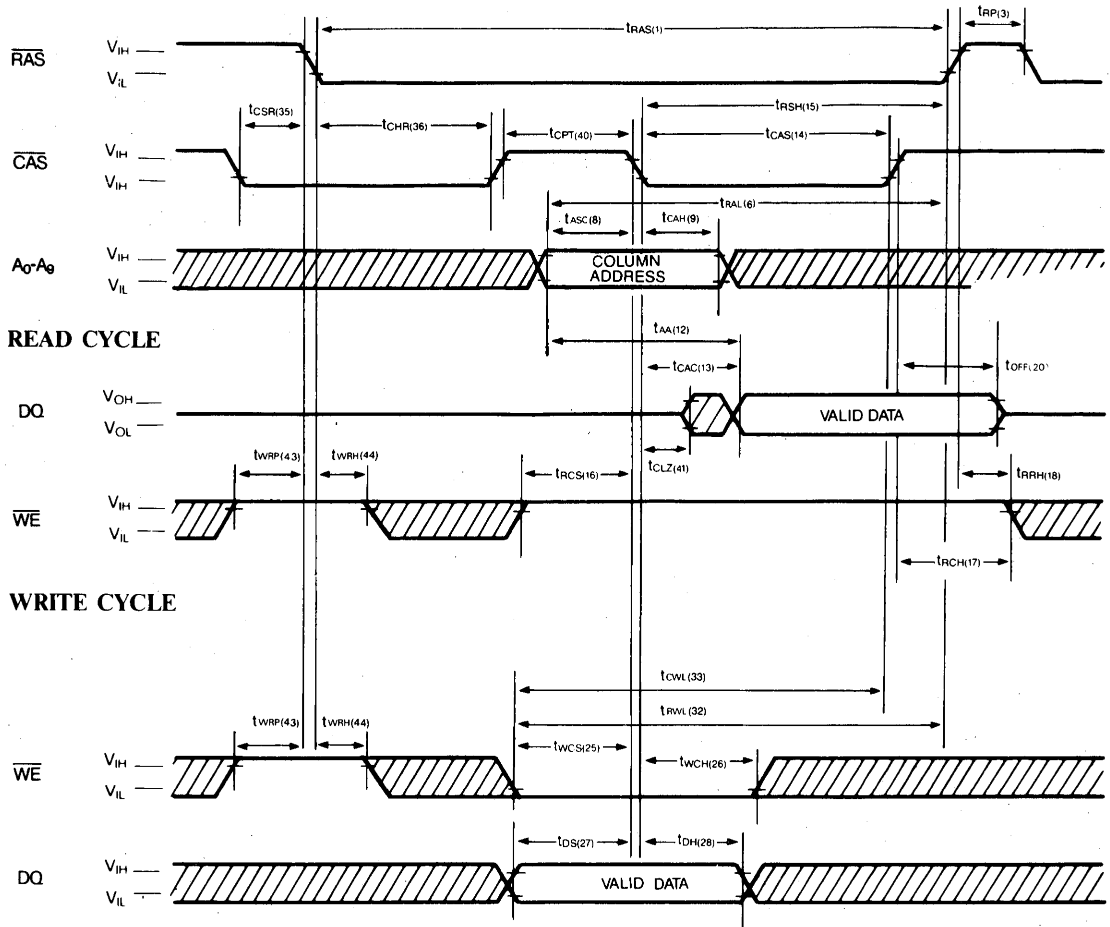


HIDDEN REFRESH CYCLE (WRITE)



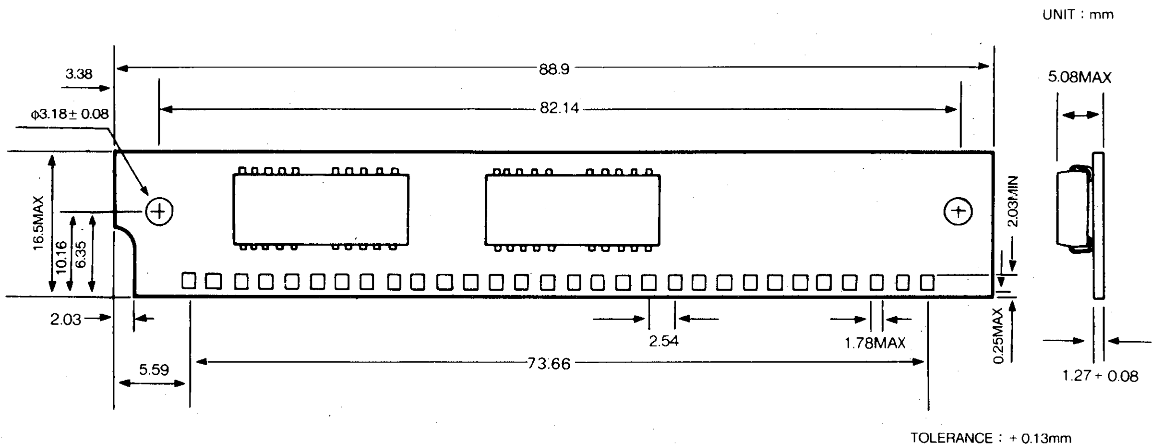
4

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

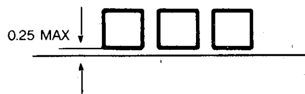


PACKAGE INFORMATION

HYM581000BM



∗ DETAIL OF CONTACTS



MEMO

HYUNDAI SEMICONDUCTOR

HYM581000BL

1M×8-Bit CMOS DRAM MODULE

M4K1200A-MAR92

DESCRIPTION

The HYM581000BLM is a 1M words by 8bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of two HY514400ALJ in 20/26 pin SOJ mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM581000BLM is a socket type single-in line module suitable for easy interchange and addition of 1M bytes memory.

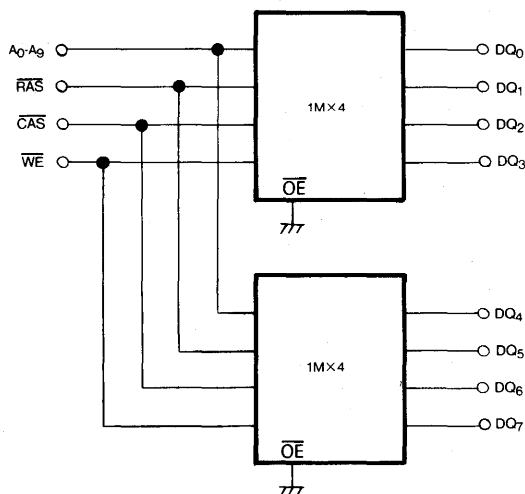
FEATURES

- Fast Page Mode operation
- Fast Access Time

	t_{RAC}	t_{CAC}	t_{PC}
HYM581000BLM-60	60	20	40
HYM581000BLM-70	70	20	45
HYM581000BLM-80	80	25	55

- Single power supply of 5V± 10%
- $\overline{CAS}$-Before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden Refresh.
- Low power operating
  1.21W max (HYM581000BLM-60)
  1.10W max (HYM581000BLM-70)
  0.99W max (HYM581000BLM-80)
- TTL compatible inputs and outputs
- 1024 refresh cycles/128ms

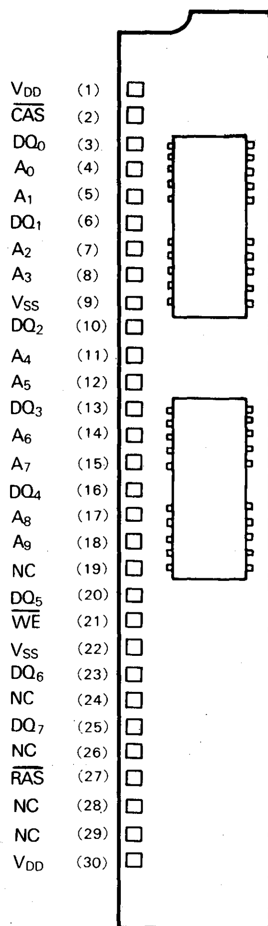
BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS



NOTES :

1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
2. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	1.54	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS
(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM581000BLM		UNIT	NOTE
				MIN.	MAX.		
$\vert I_{LI} \vert$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$		−	20	μA	
$\vert I_{LO} \vert$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		−	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	t_{RC}=t_{RC}(min)	−60	−	220	mA	1
			−70	−	200		
			−80	−	180		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\ge V_{SS}$		−	4	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	t_{RC}=t_{RC}(min.)	−60	−	220	mA	
			−70	−	200		
			−80	−	180		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−60	−	140	mA	1
			−70	−	120		
			−80	−	100		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs $\ge V_{SS}$		−	0.4	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	t_{RC}=t_{RC}(min.)	−60	−	220	mA	
			−70	−	200		
			−80	−	180		
I_{DD7}	V_{DD} Supply Current, Battery Back up	$\overline{CAS}$=CBR cycling or 0.2V, $\overline{OE}$=$\overline{WE}$=V_{DD}−0.2V, Add=V_{DD}−0.2V or 0.2V, I/O=V_{DD}−0.2V or 0.2V or open, t_{RC}=125μs, t_{RAS}=t_{RAS}(min.) ~300ns		−	0.6	mA	1
		Same as above except t_{RAS}=300ns~1μs		−	0.8	mA	1, 5
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		−	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	−	V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected, Speciiied I_{DD}(max.) is measured with the output open.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1. 2. 3

#	SYMBOL	PARAMETER	HYM581000BLM						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
3	t_{RP}	$\overline{RAS}$ Prechange Time	50	–	50	–	60	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	55	ns	8
11	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	4,8,9
12	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	4,9
13	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	4,8
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
20	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
24	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
27	t_{DS}	Data In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data In Hold Time	15	–	15	–	15	–	ns	7

#	SYMBOL	PARAMETER	HYM581000BLM						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
30	t_{CPA}	Access Time from Column Precharge	–	35	–	40	–	50	ns	4
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	40	–	45	–	55	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	128	–	128	–	128	ms	
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	200K	70	200K	80	200K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	30	–	35	–	40	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	4
42	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
43	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

CAPACITANCE

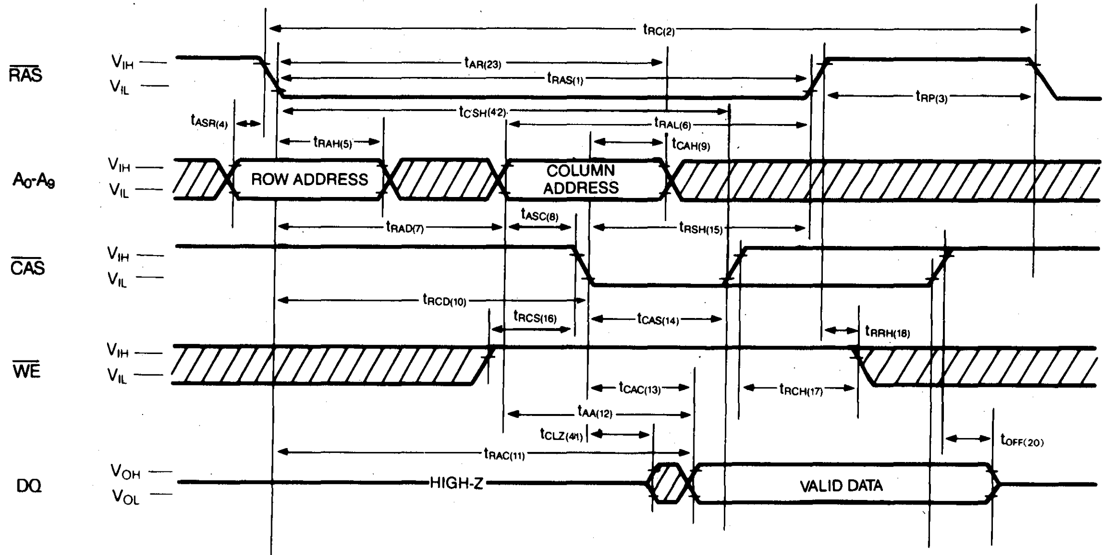
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance(A_0-A_9, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	25	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF

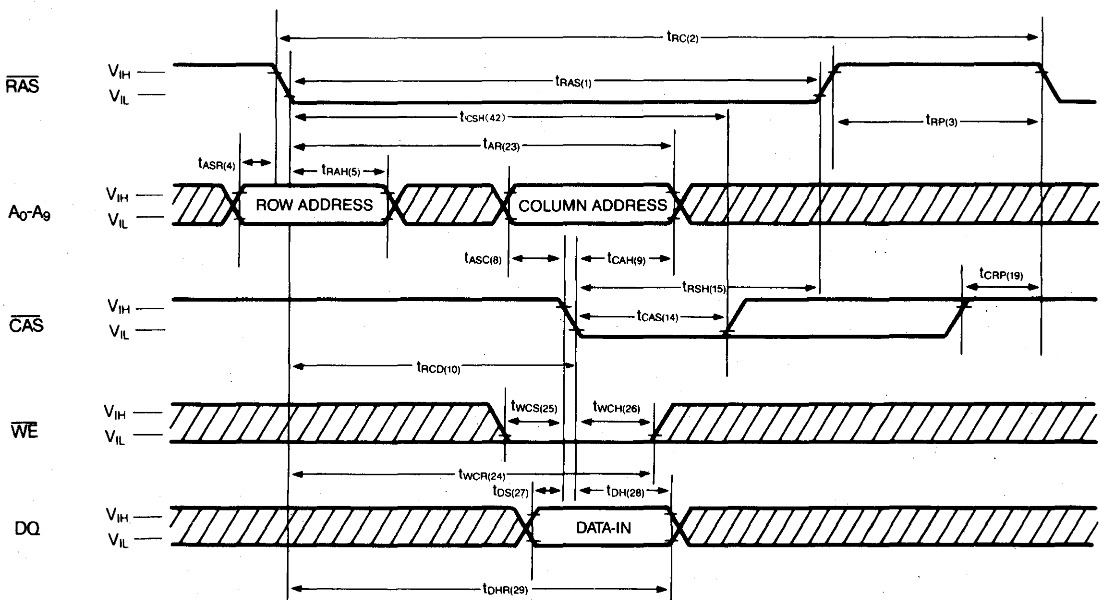
4

TIMING DIAGRAM

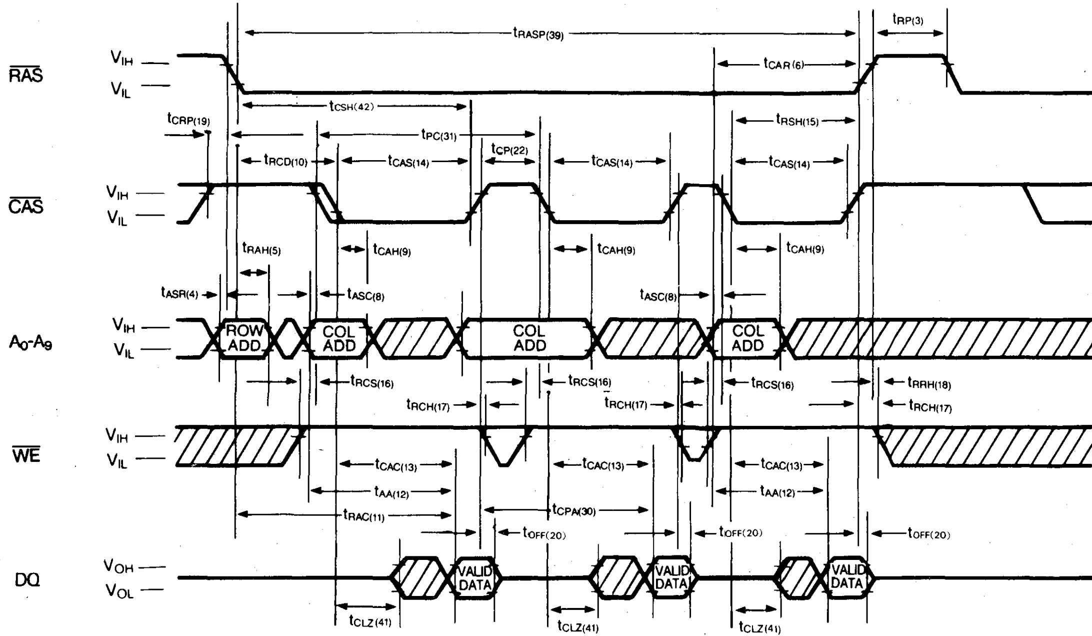
READ CYCLE



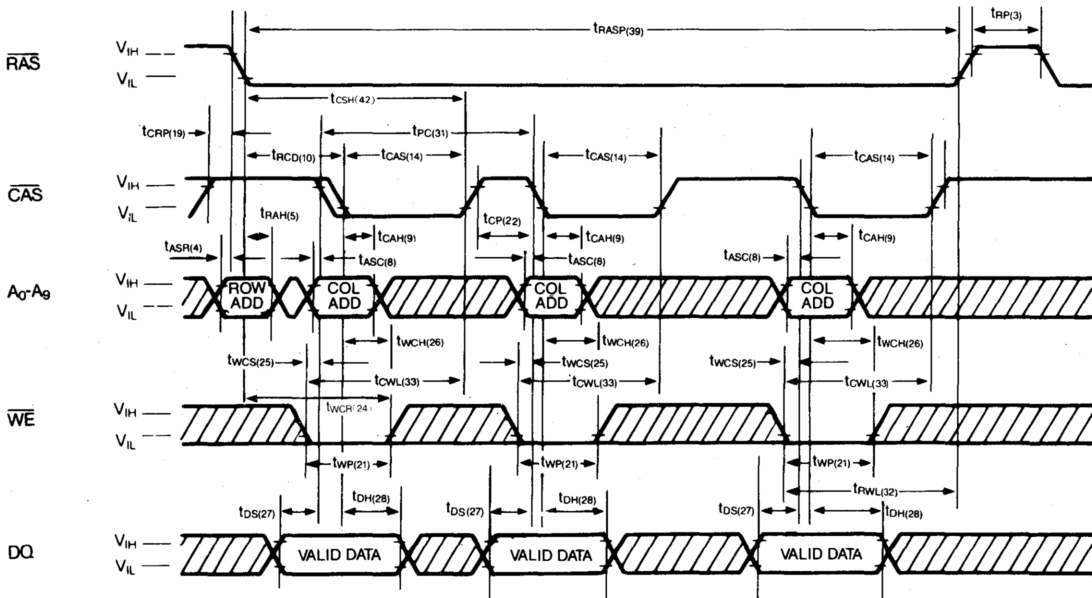
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

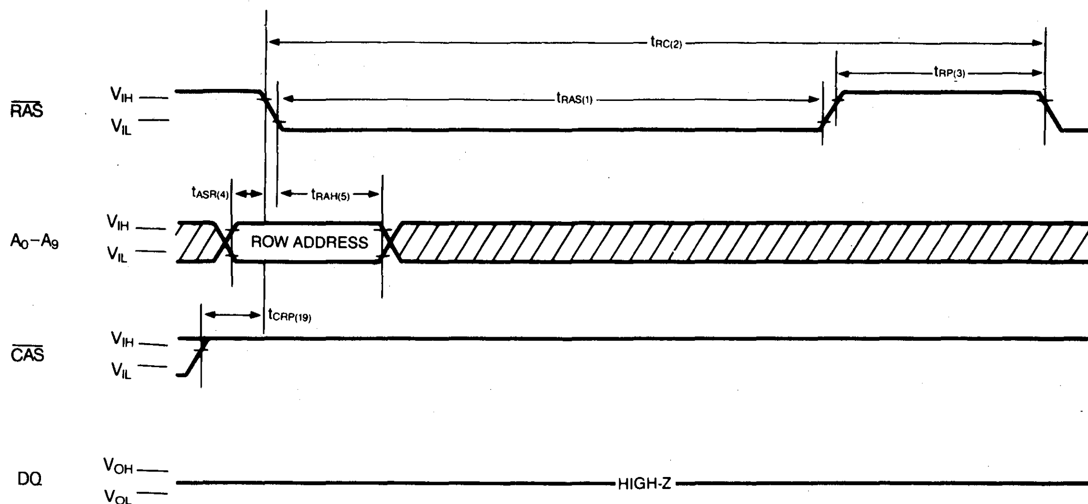


FAST PAGE MODE EARLY WRITE CYCLE

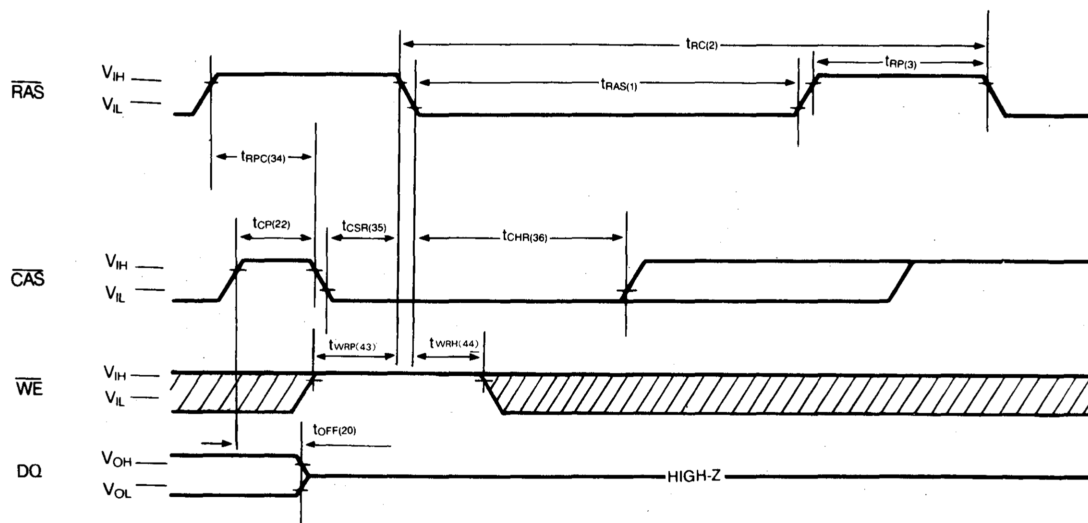


4

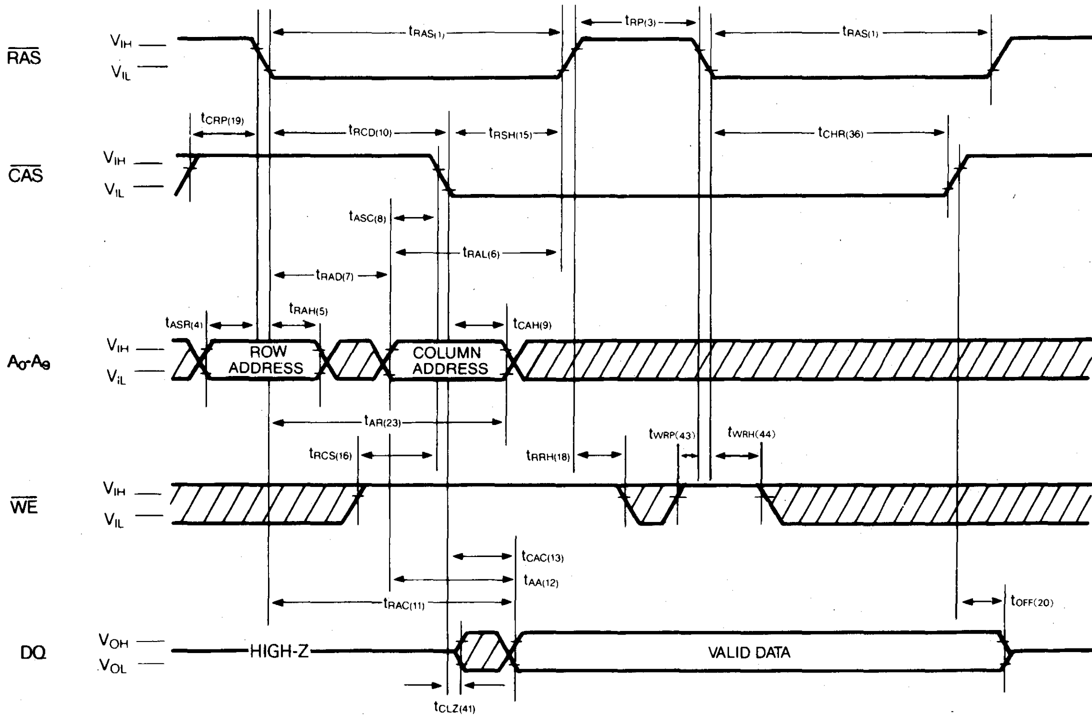
$\overline{RAS}$-ONLY REFRESH CYCLE



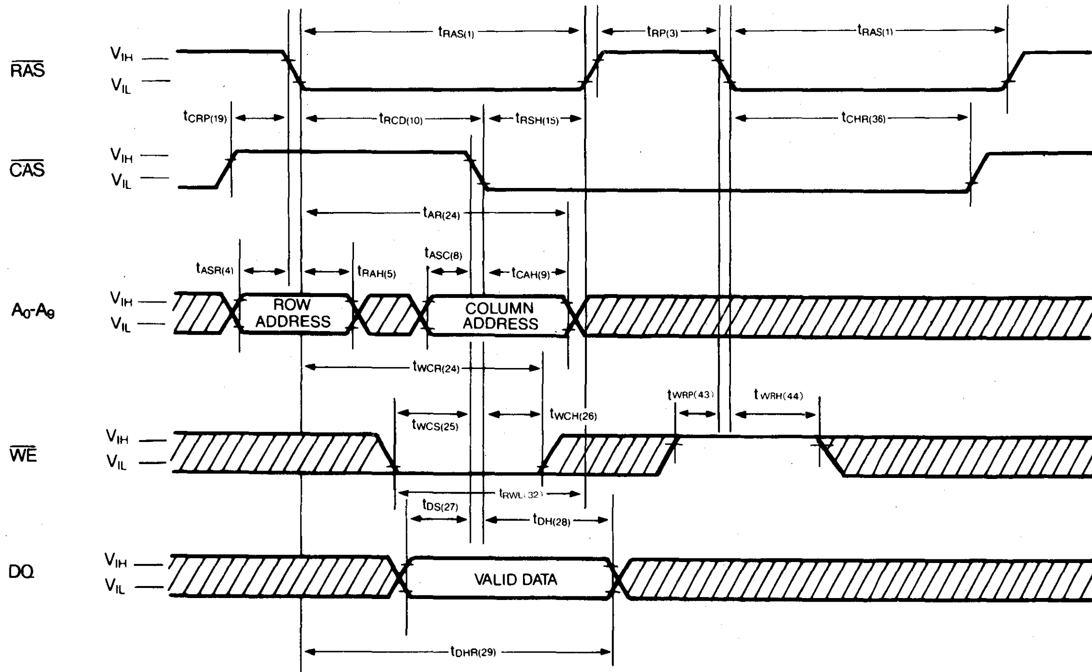
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)

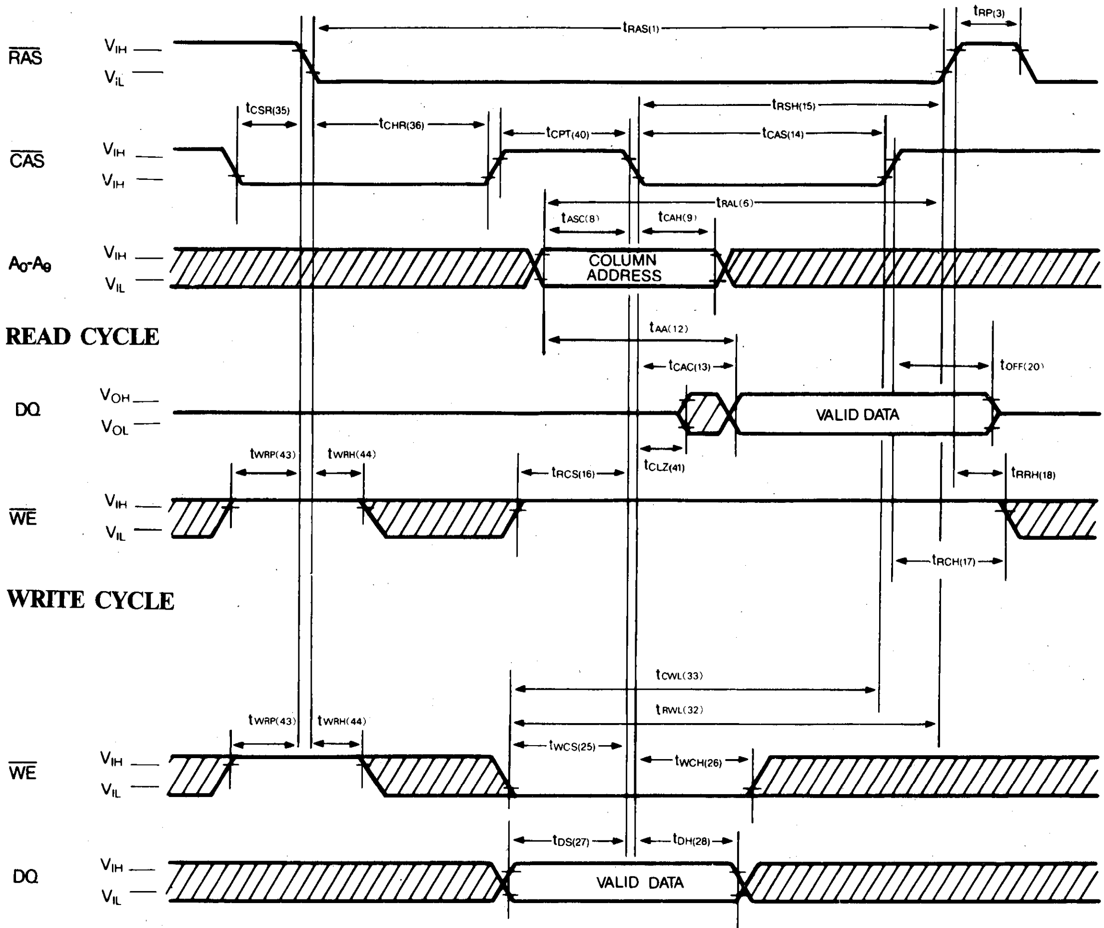


HIDDEN REFRESH CYCLE (WRITE)



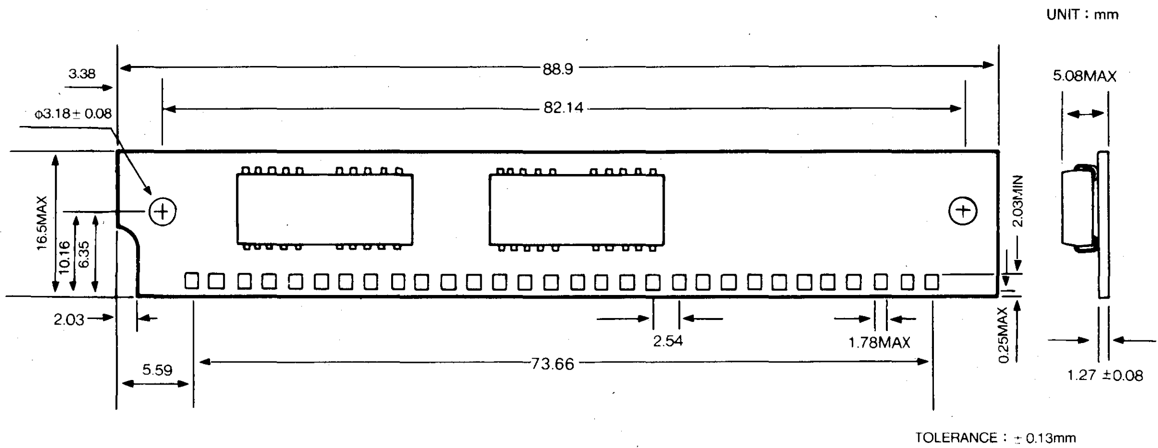
4

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

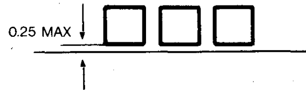


PACKAGE INFORMATION

HYM581000BLM



* DETAIL OF CONTACTS



MEMO

HYUNDAI SEMICONDUCTOR

HYM591000

1M×9-Bit CMOS DRAM MODULE

M441201C-JAN92

DESCRIPTION

The HYM591000M is a 1M words by 9 bits dynamic RAM module and consists of nine HY531000J Fast Page mode CMOS DRAM in 20/26 pin SOJ package mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF de-coupling capacitors are mounted under all the 1M DRAMs.

HYM591000M is suitable for easy inter-change and addition of 1M bytes memory with parity RAM.

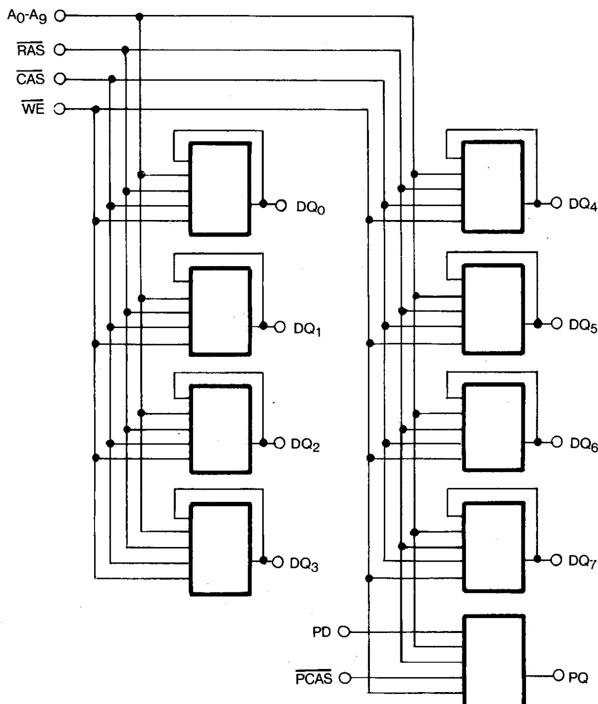
FEATURES

- Fast Page Mode operation
- Fast access time

	t_{RAC}	t_{CAC}	t_{PC}
HYM591000M-60	60	20	40
HYM591000M-70	70	20	40
HYM591000M-80	80	20	45
HYM591000M-10	100	25	55

- Single power supply of 5V± 10%
- $\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh
- Low power operating
  4.21W max (HYM591000M-60)
  3.71W max (HYM591000M-70)
  3.22W max (HYM591000M-80)
  2.72W max (HYM591000M-10)
- TTL compatible inputs and outputs
- 512 refresh cycles / 8ms

BLOCK DIAGRAM

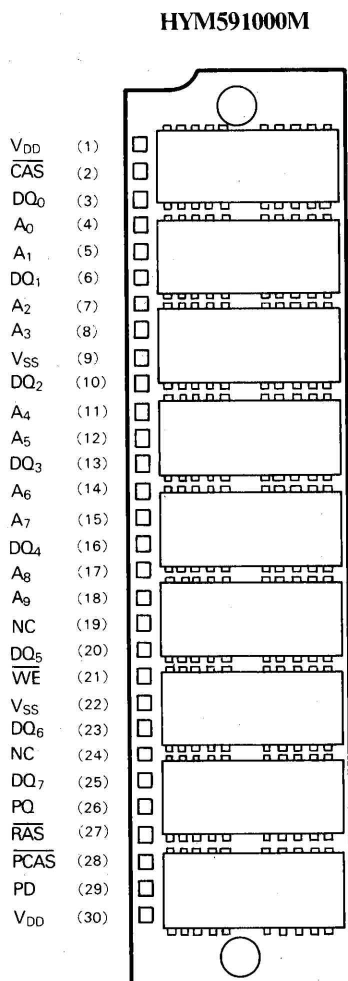


PIN NAMES

A_0-A_9	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
PD	DATA IN FOR PARITY
PQ	DATA OUT FOR PARITY
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{PCAS}$	$\overline{CAS}$ FOR PARITY
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

4

PIN CONNECTIONS



NOTES :

1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ0-DQ7).
2. Separate $\overline{PCAS}$ control for one separate pair of data-in (PD) and data-out (PQ) lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ0-DQ7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	5.4	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS
(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM591000M MIN.	HYM591000M MAX	UNIT	NOTE
$\lvert I_{LI} \rvert$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$			90	μA	
$\lvert I_{LO} \rvert$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60		765	mA	1, 2
			−70		675		
			−80		585		
			−10		495		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\geq V_{SS}$			18	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60		765	mA	2
			−70		675		
			−80		585		
			−10		495		
I_{DD4}	V_{DD} Supply Current, Fast page mode	Minimum Cycle	−60		585	mA	1, 2
			−70		495		
			−80		405		
			−10		315		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS}=V_{IH}$, other inputs $\geq V_{SS}$			9	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60		765	mA	2
			−70		675		
			−80		585		
			−10		495		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA			0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4		V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with output open.
2. I_{DD} is dependent upon the number of address transitions, Specified I_{DD}(max.) is measured with a maximum of two transitions per address cycle in fast page mode.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HYM591000M								UNIT	NOTE
			60		70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120		130		150		180		ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50		50		60		70		ns	
4	t_{ASR}	Row Address Set-up Time	0		0		0		0		ns	
5	t_{RAH}	Row Address Hold Time	10		10		10		15		ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		50		ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	1
8	t_{ASC}	Column Address Set-up Time	0		0		0		0		ns	
9	t_{CAH}	Column Address Hold Time	15		15		15		20		ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	60	25	75	ns	2
11	t_{RAC}	Access Time From $\overline{RAS}$		60		70		80		100	ns	3,4,5
12	t_{AA}	Access Time From Column Address		30		35		40		50	ns	5,7
13	t_{CAC}	Access Time From $\overline{CAS}$		20		20		20		25	ns	5,6
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	20	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20		20		20		25		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		0		ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	8
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	8
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		5		ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	0	20	ns	9
21	t_{WP}	Write Command Pulse Width	15		15		15		20		ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		10		ns	
23	t_{AR}	Column Address Hold Time From $\overline{RAS}$	50		55		60		75		ns	
24	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	50		55		60		75		ns	
25	t_{WCS}	Write Command Set-up Time	0		0		0		0		ns	10
26	t_{WCH}	Write Command Hold Time	15		15		15		20		ns	
27	t_{DS}	Data-In Set-up Time	0		0		0		0		ns	11
28	t_{DH}	Data-In Hold Time	15		15		15		20		ns	11
29	t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	50		55		60		75		ns	
30	t_{CPA}	Access Time From $\overline{CAS}$ Precharge		35		35		40		50	ns	5,12
31	t_{PC}	Fast page mode Cycle time	40		40		45		55		ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		20		25		ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		20		25		ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	5		5		5		5		ns	

#	SYMBOL	PARAMETER	HYM591000M								UNIT	NOTE
			60		70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15		15		15		20		ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	3	50	ns	13,14
38	t_{CLZ}	$\overline{CAS}$ to output in Low-z	0		0		0		0		ns	5
39	t_{REF}	Refresh Interval(512 Cycle)		8		8		8		8	ms	15
40	t_{RASP}	Fast page Mode $\overline{RAS}$ Pulse Width	60		70		80		100		ns	
41	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40		40		40		50		ns	

NOTES :

1. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a referenced point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
2. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then the access time is controlled by t_{CAC}.
3. Assume $t_{RAD} \le t_{RAD}$(max.). If t_{RAD} is greater than t_{RAD}(max.) then t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD}(max).
4. Assume $t_{RCD} \le t_{RCD}$(max.). If t_{RCD} is greater than t_{RCD}(max.) then t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD}(max).
5. Measured with a load equivalent to two TTL loads and 100 pF.
6. Assumes that $t_{RCD} \ge t_{RCD}$(max.) and $t_{RAD} \le t_{RAD}$(max.).
7. Assumes that $t_{RCD} \le t_{RCD}$(max.) and $t_{RAD} \ge t_{RAD}$(max.).
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
9. t_{OFF} and t_{OH} define the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
10. t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as a electrical characteristic only. If $t_{WCS} \ge t_{WCS}$(min.), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle.
11. t_{DS} and t_{DH} are referenced to the latter occurence of $\overline{CAS}$ or $\overline{WE}$
12. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{CPA}.
13. t_T is measured between V_{IH}(min.) and V_{IL}(max.).
14. AC measurements assume t_T=5ns.
15. An initial pause of 200μs is required after power-up and followed at least 8 initialization cycles(any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). 8 initialization cycles are required after extended period of bias without clocks.

4

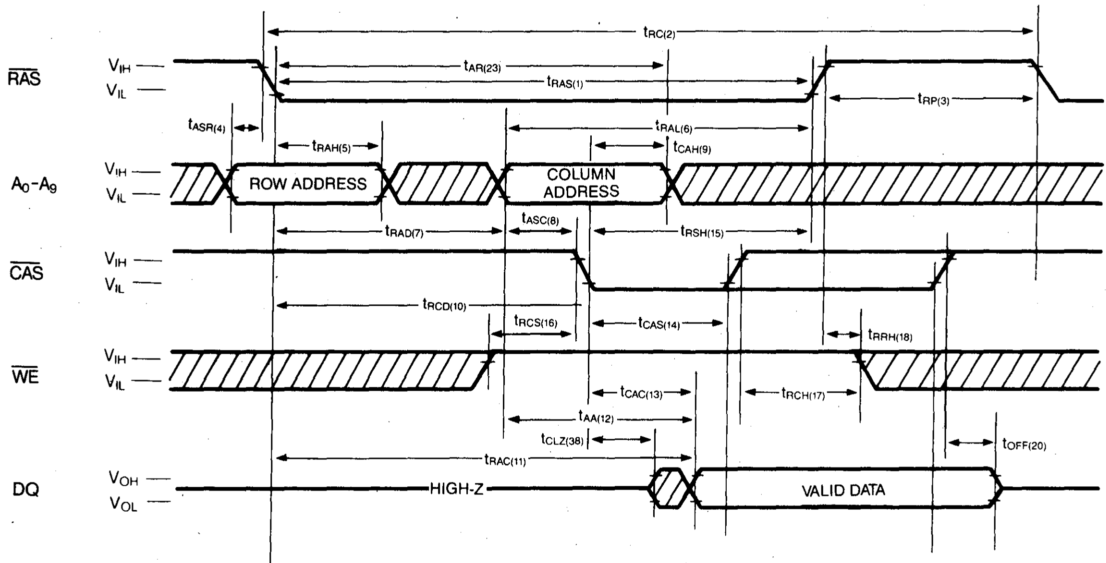
CAPACITANCE

(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted)

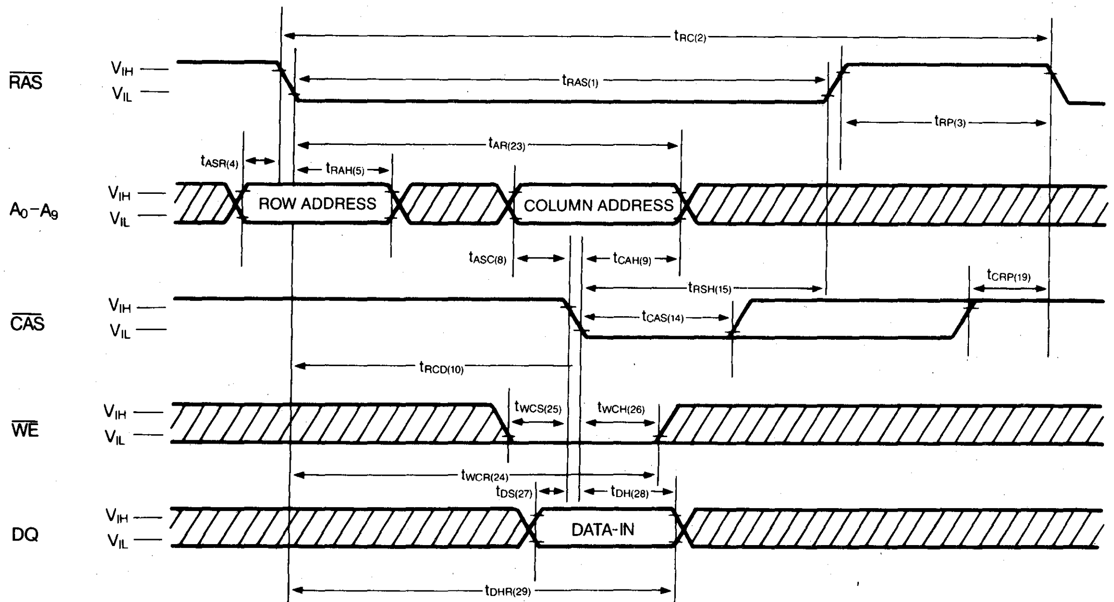
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_9, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{IN2}	Input Capacitance(PD, $\overline{PCAS}$)	–	10	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF
C_{PQ}	Output Capacitance(PQ)	–	10	pF

TIMING DIAGRAM

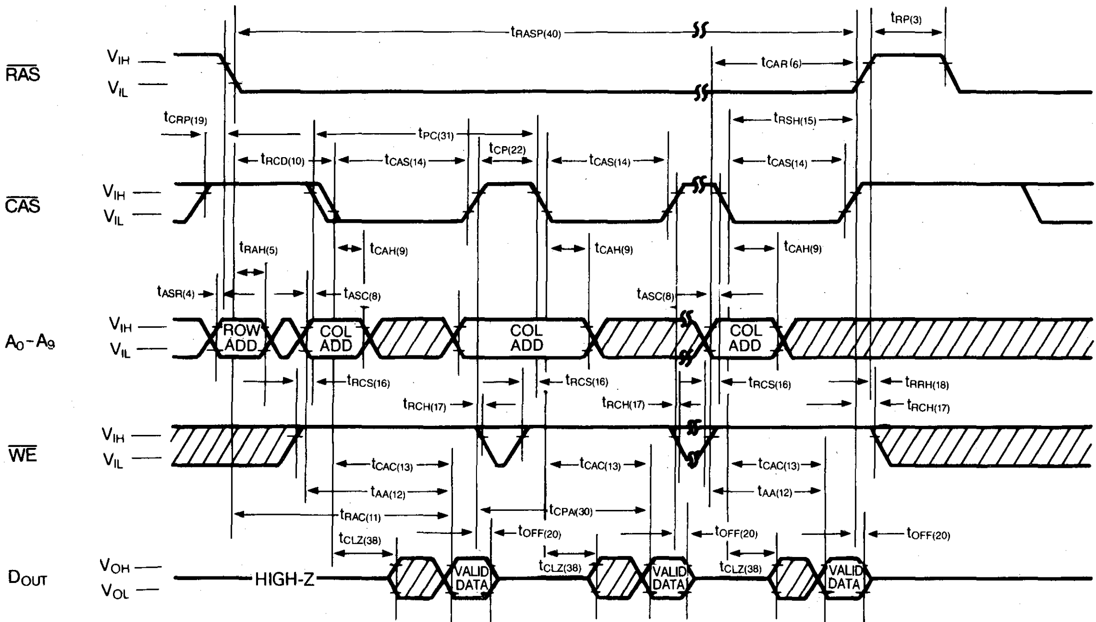
READ CYCLE



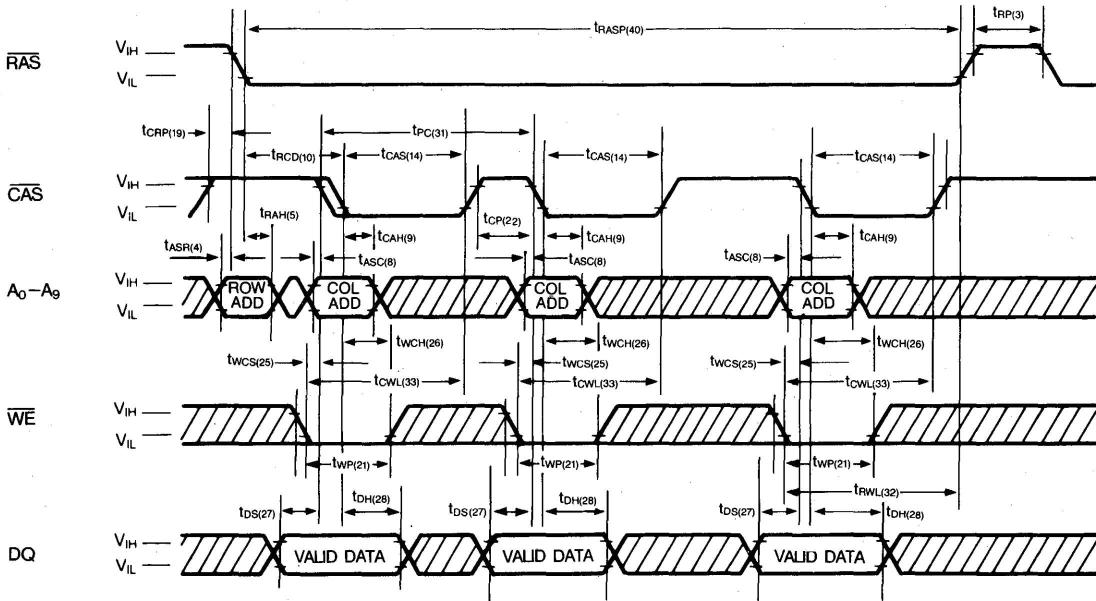
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

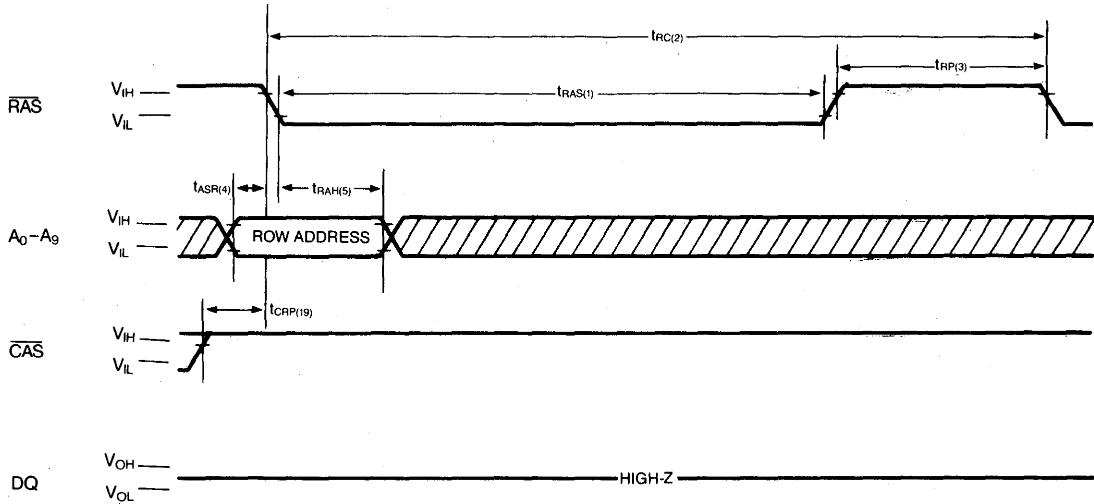


FAST PAGE MODE EARLY WRITE CYCLE

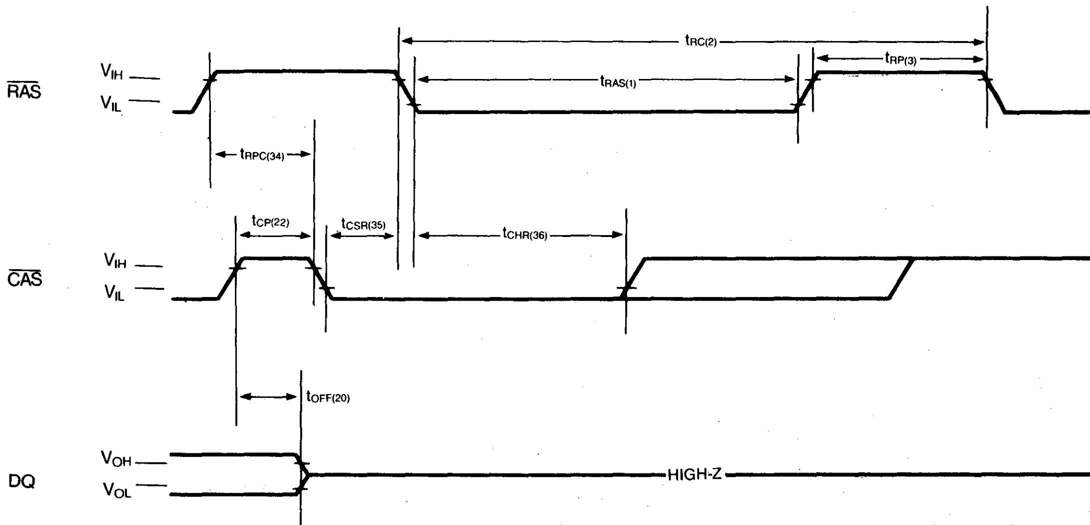


4

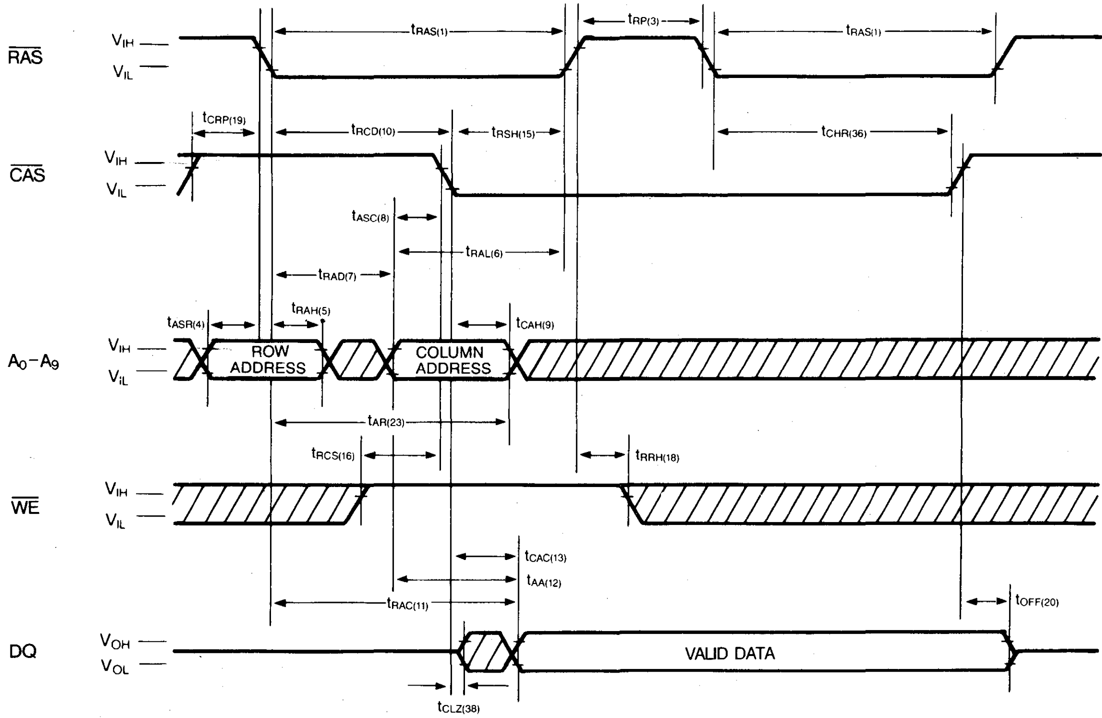
$\overline{RAS}$-ONLY REFRESH CYCLE



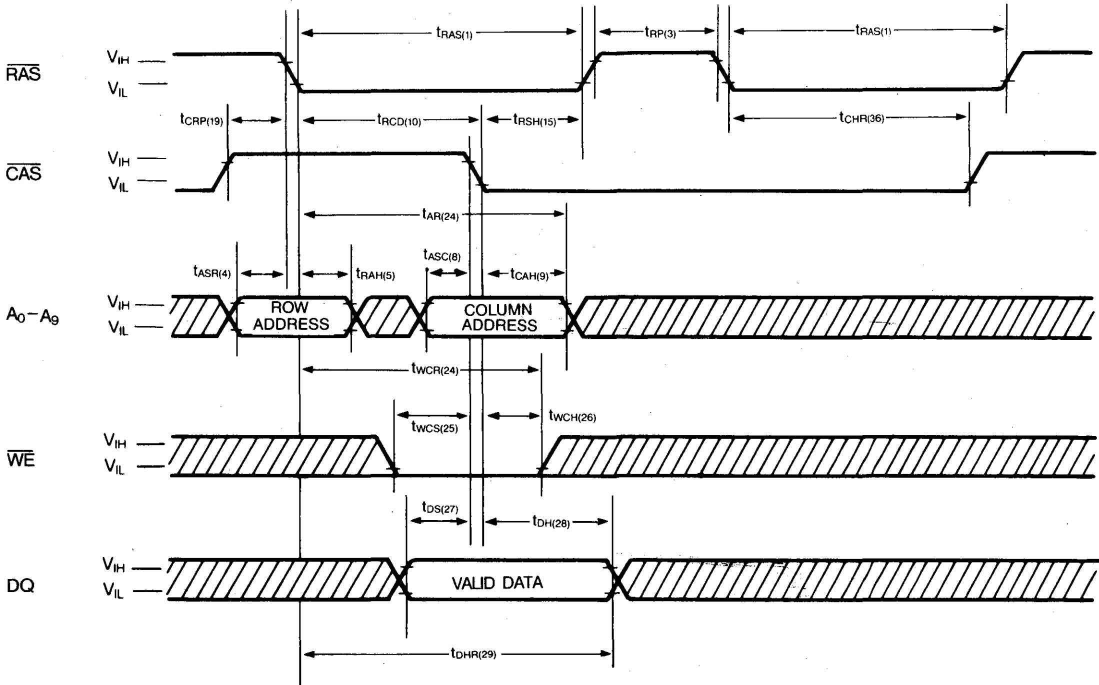
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)

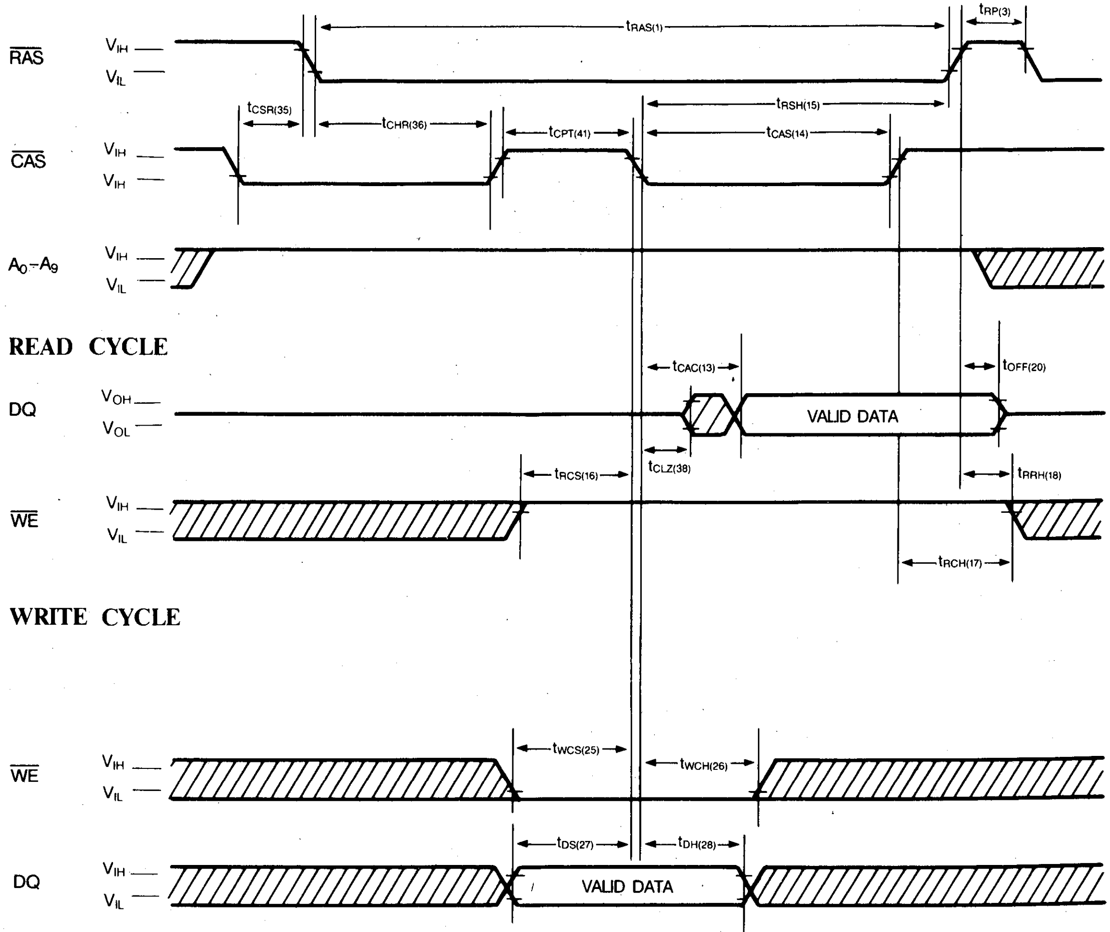


HIDDEN REFRESH CYCLE (WRITE)



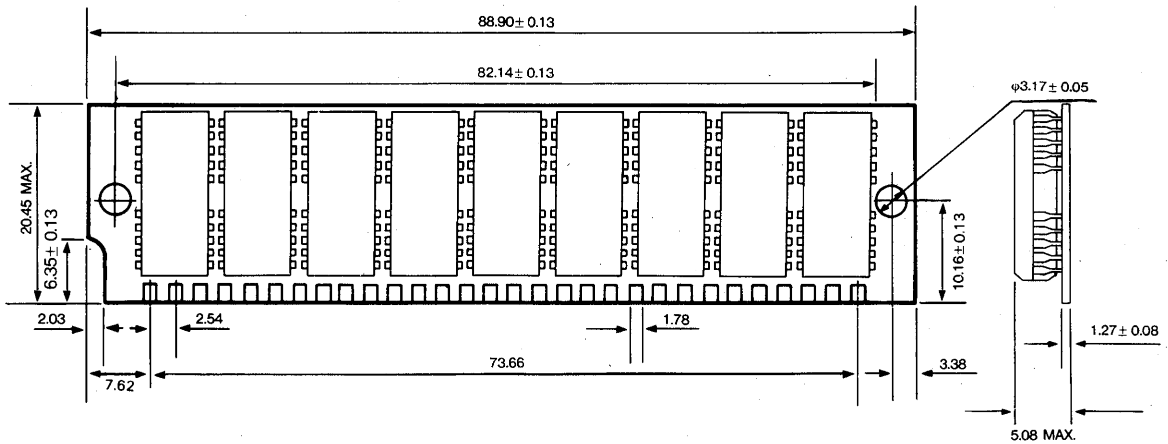
4

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE



PACKAGE INFORMATION

HYM591000M



∗ DETAIL OF CONTACTS

0.25 MAX

MEMO

HYM591000A

1M×9-Bit CMOS DRAM MODULE

M481202A-JAN92

DESCRIPTION

The HYM591000AM is a 1M words by 9bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of two HY514400J and one HY531000J both in 20/26 pin SOJ mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM591000AM is a socket type single-in line module suitable for easy interchange and addition of 1M bytes memory with parity RAM.

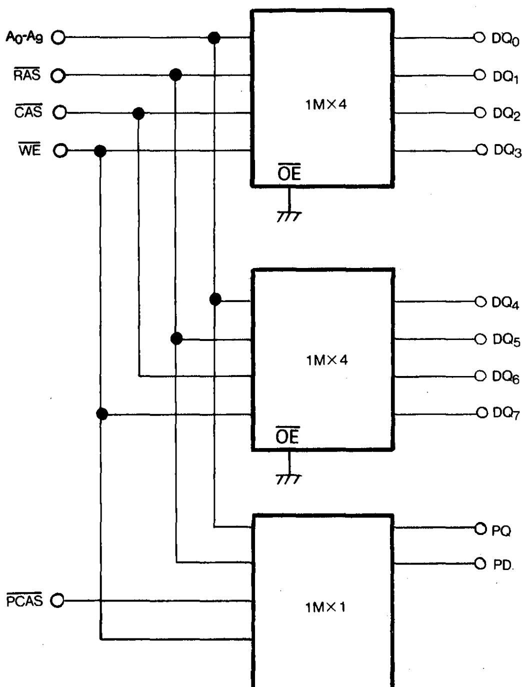
FEATURES

- Fast Page Mode operation
- Fast Access Time

	t_{RAC}	t_{CAC}	t_{PC}
HYM591000AM-70	70	20	50
HYM591000AM-80	80	25	55
HYM591000AM-10	100	25	60

- Single power supply of 5V± 10%
- $\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh.
- Low power operating
  1.46W max (HYM591000AM-70)
  1.30W max (HYM591000AM-80)
  1.13W max (HYM591000AM-10)
- TTL compatible inputs and outputs
- 1024 refresh cycles/16ms

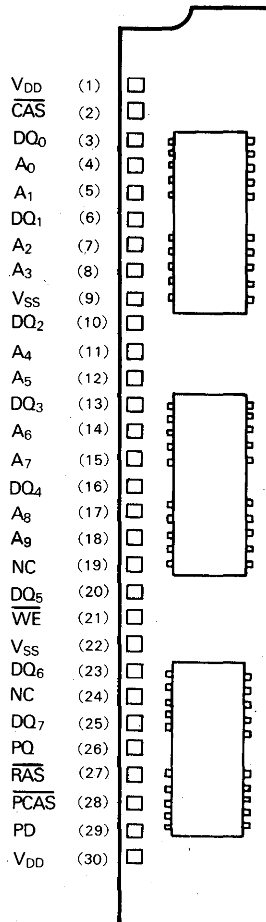
BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
PD	DATA IN FOR PARITY
PQ	DATA OUT FOR PARITY
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{PCAS}$	$\overline{CAS}$ FOR PARITY
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS



NOTES :

1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
2. Separate $\overline{PCAS}$ control for one separate pair of data-in (PD) and data-out (PQ) lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature(Plastic)	−55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	1.8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM591000AM		UNIT	NOTE
				MIN.	MAX.		
$\mid I_{LI} \mid$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		–	30	μA	
$\mid I_{LO} \mid$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min)	−70	–	265	mA	1
			−80	–	235		
			−10	–	205		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs≥ V_{SS}		–	6	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−70	–	265	mA	
			−80	–	235		
			−10	–	205		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−70	–	215	mA	1
			−80	–	185		
			−10	–	155		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs≥V_{SS}		–	3	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−70	–	265	mA	
			−80	–	235		
			−10	–	205		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTES :

1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1. 2. 3

#	SYMBOL	PARAMETER	HYM591000AM						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	55	25	75	ns	8
11	t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	4,8,9
12	t_{AA}	Access Time from Column Address	–	35	–	40	–	50	ns	4,9
13	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	–	25	ns	4,8
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	25	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
20	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55	–	60	–	80	–	ns	
24	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55	–	60	–	80	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
27	t_{DS}	Data In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data In Hold Time	15	–	15	–	20	–	ns	7

#	SYMBOL	PARAMETER	HYM591000AM						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	55	–	60	–	80	–	ns	
30	t_{CPA}	Access Time from Column Precharge	–	45	–	50	–	55	ns	4
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	50	–	55	–	60	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	30	–	30	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	70	100K	80	100K	100	100K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40	–	40	–	50	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	4
42	t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
43	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

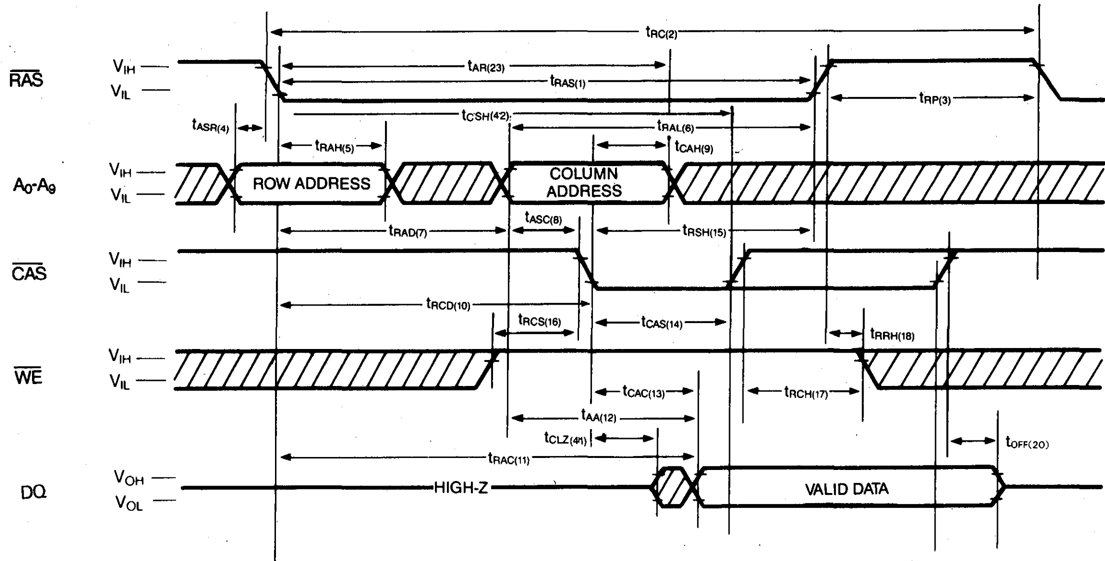
CAPACITANCE

(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

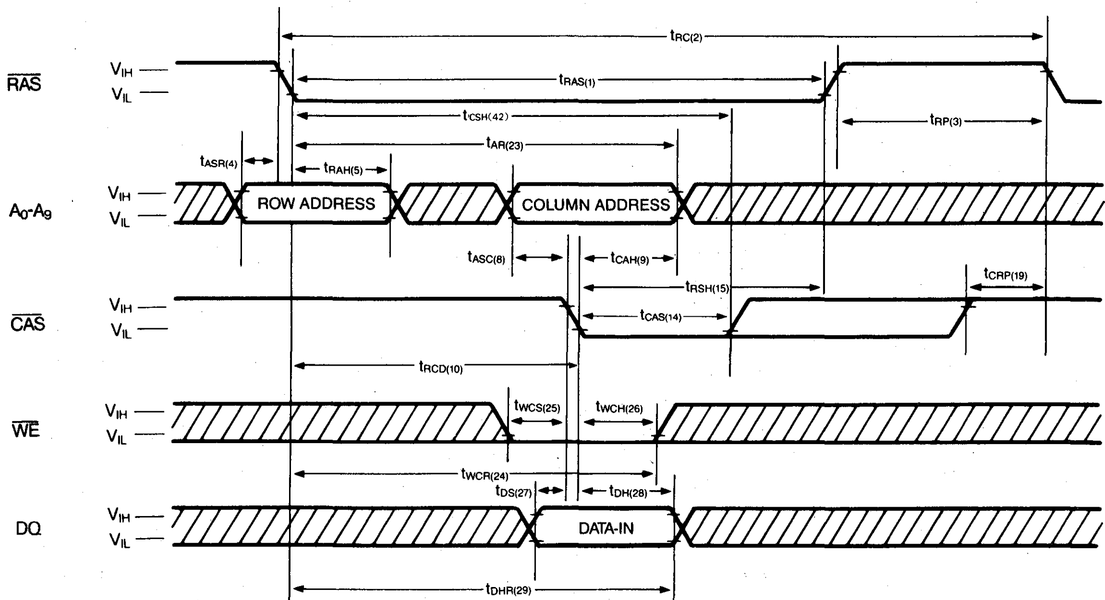
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_9, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	25	pF
C_{IN2}	Input Capacitance(PD, $\overline{PCAS}$)	–	10	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF
C_{PQ}	Output Capacitance(PQ)	–	10	pF

TIMING DIAGRAM

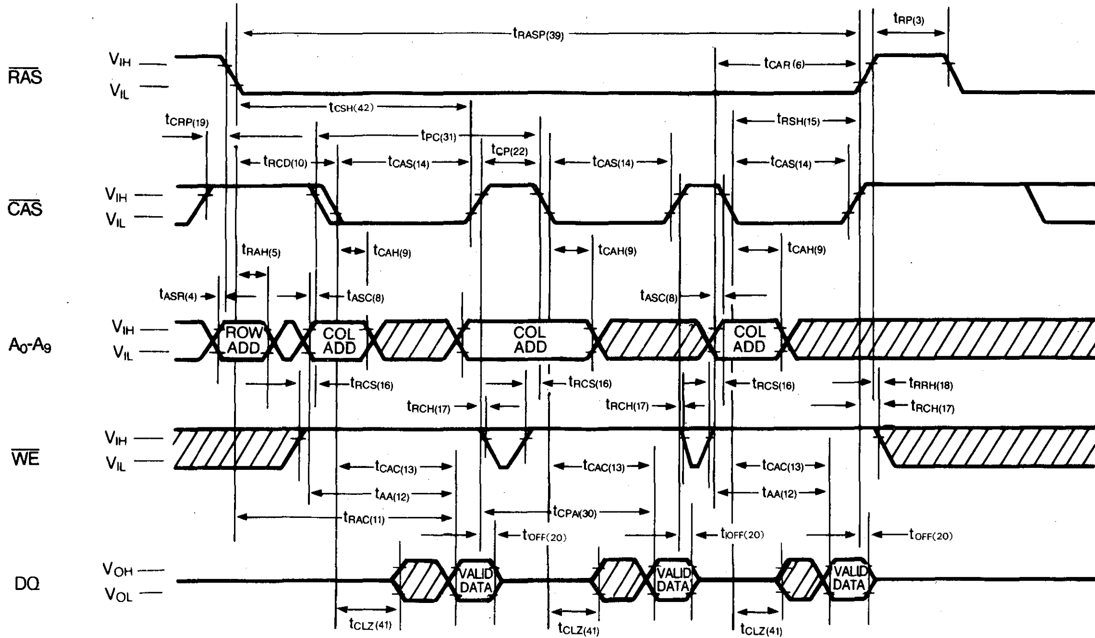
READ CYCLE



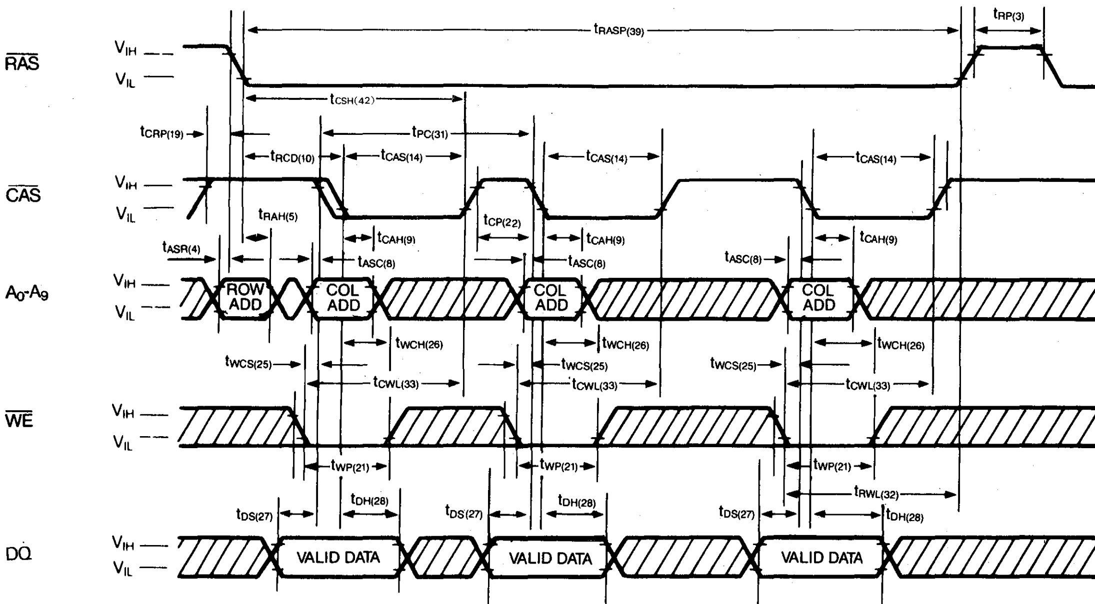
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

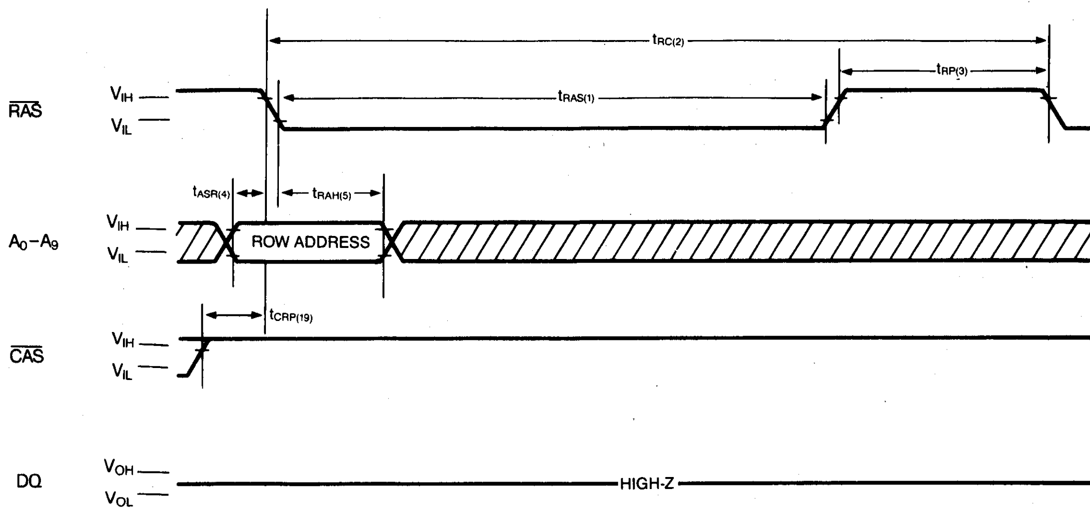


FAST PAGE MODE EARLY WRITE CYCLE

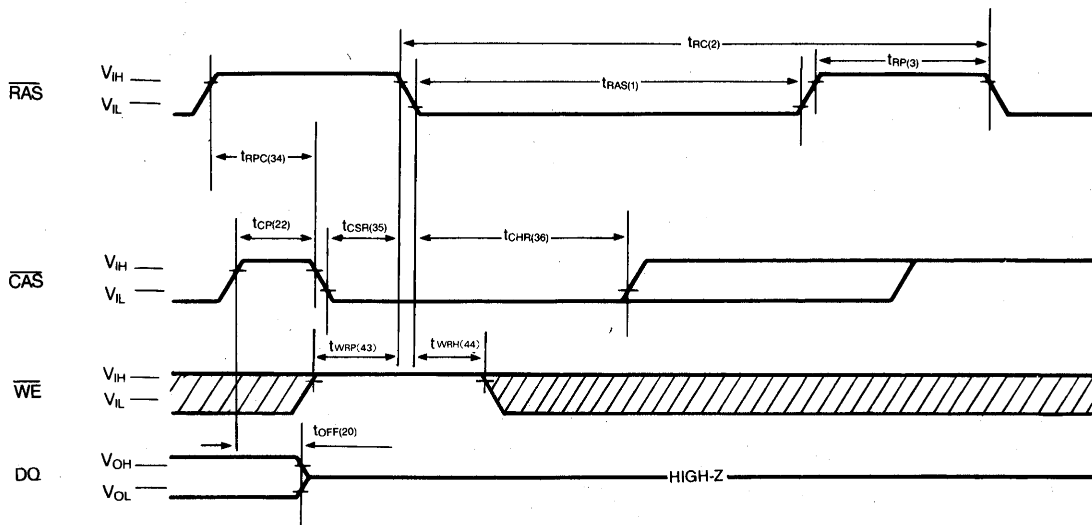


4

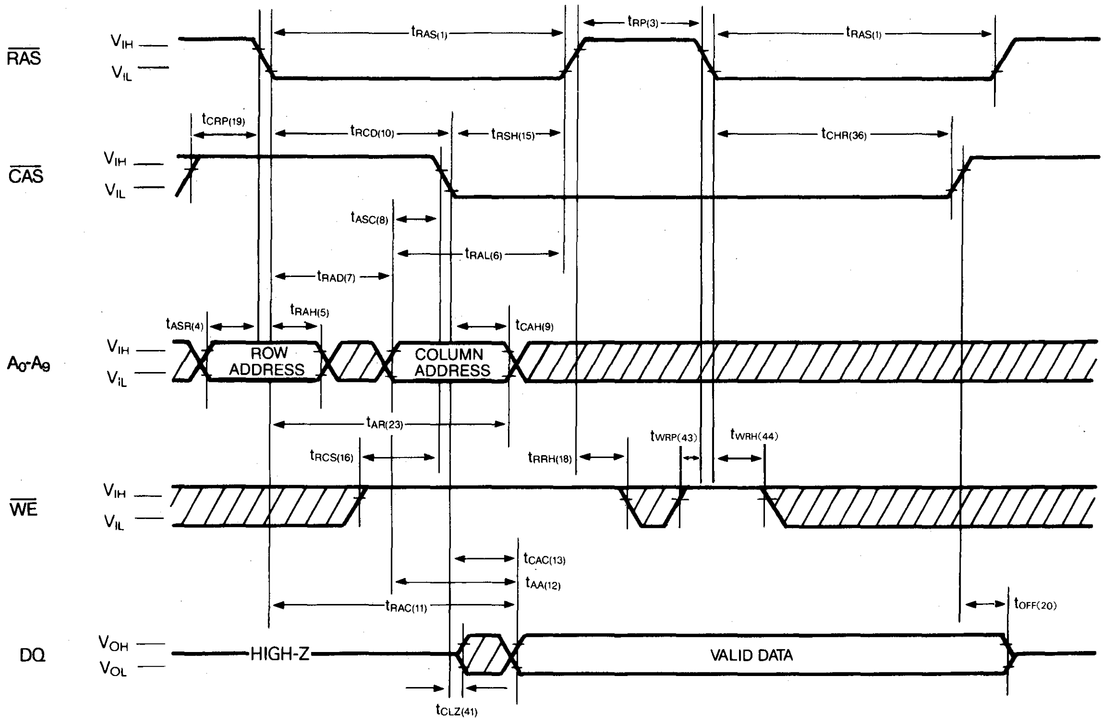
$\overline{RAS}$-ONLY REFRESH CYCLE



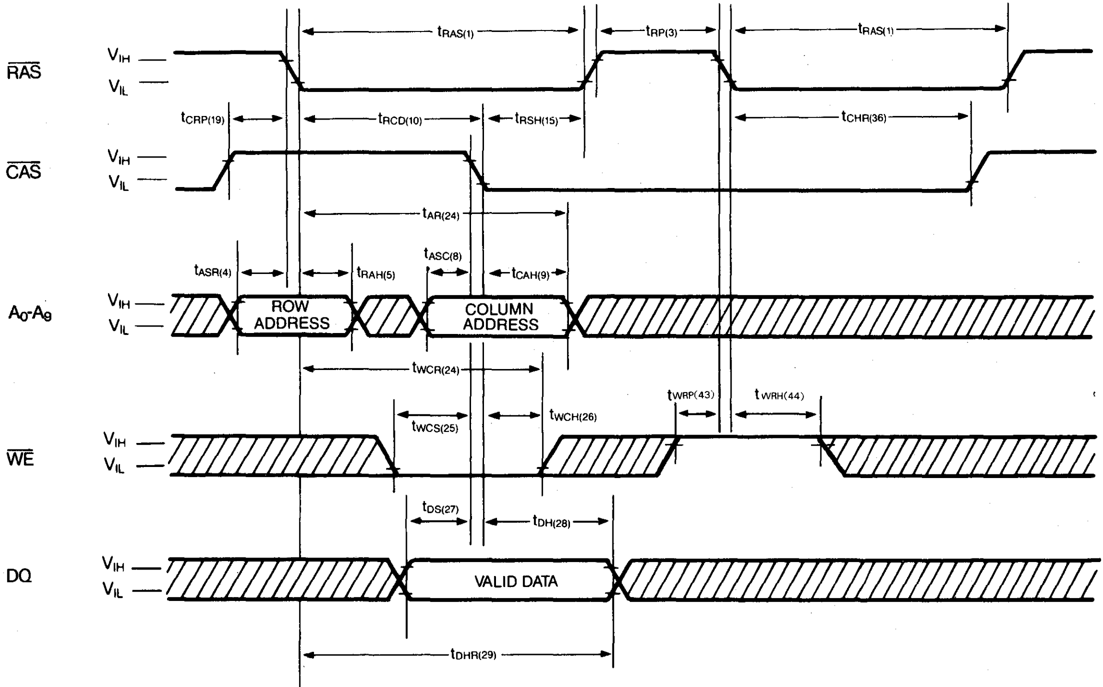
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)

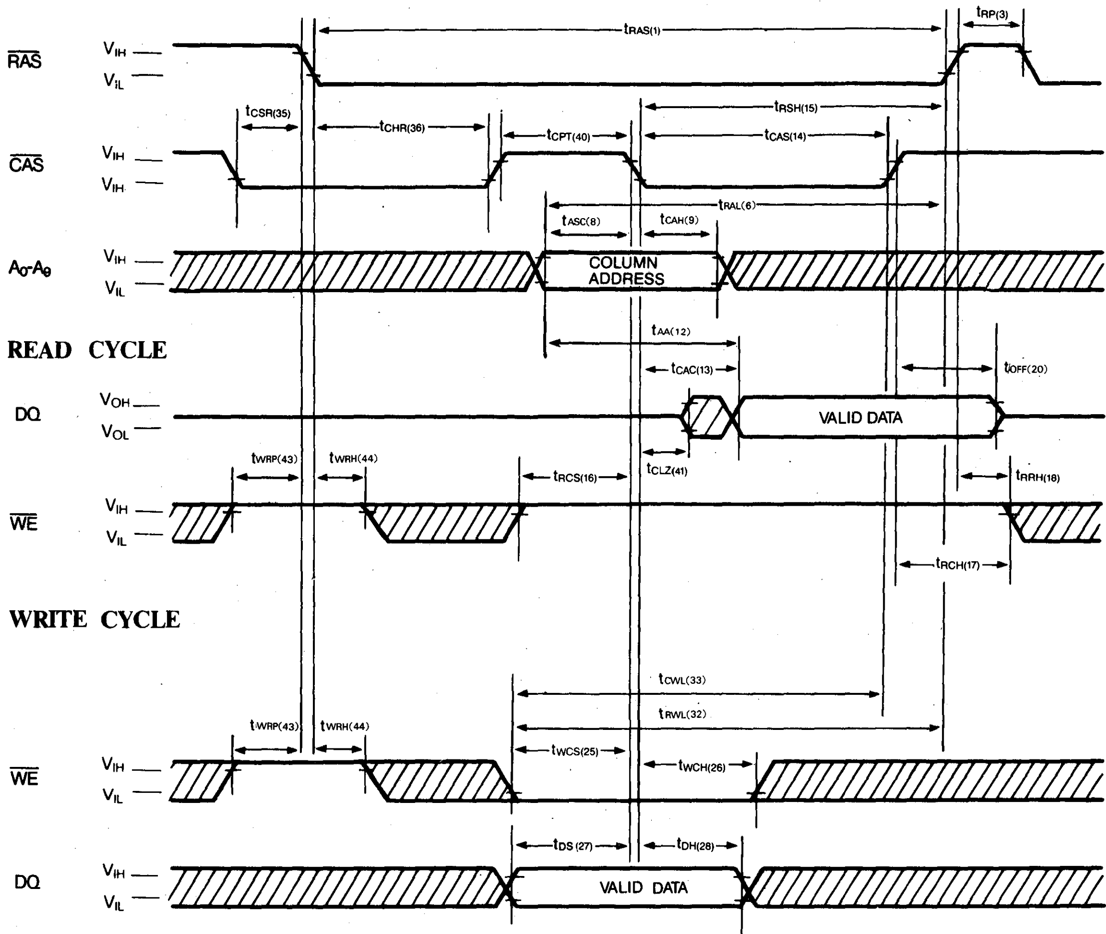


HIDDEN REFRESH CYCLE (WRITE)



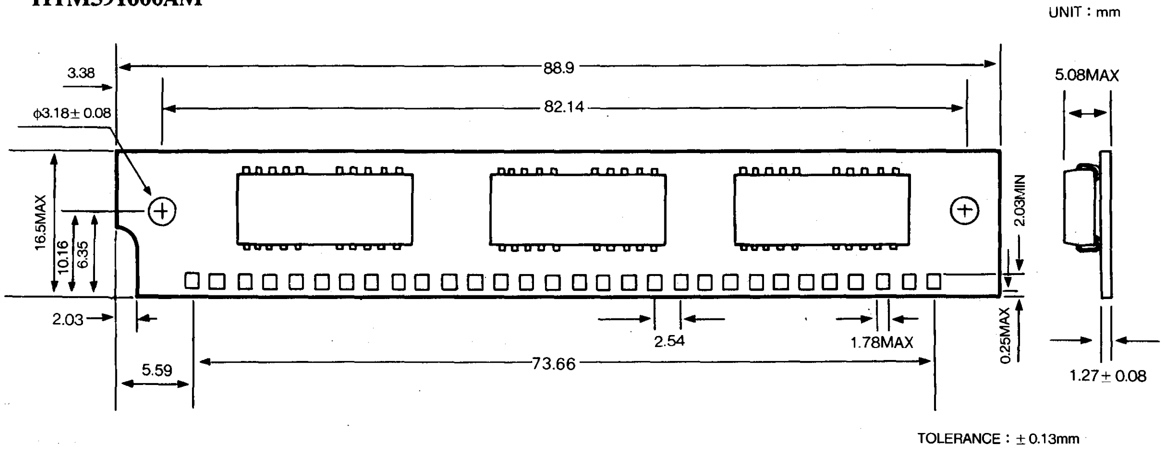
4

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

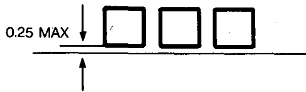


PACKAGE INFORMATION

HYM591000AM



* DETAIL OF CONTACTS



MEMO

PRELIMINARY

HYUNDAI SEMICONDUCTOR

HYM591000B

1M×9-Bit CMOS DRAM MODULE

M4M1200A-MAR92

DESCRIPTION

The HYM591000BM is a 1M words by 9 bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of two HY514400AJ and one HY531000AJ both in 20/26 pin SOJ mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM591000BM is a socket type single-in line module suitable for easy interchange and addition of 1M bytes memory with parity RAM.

FEATURES

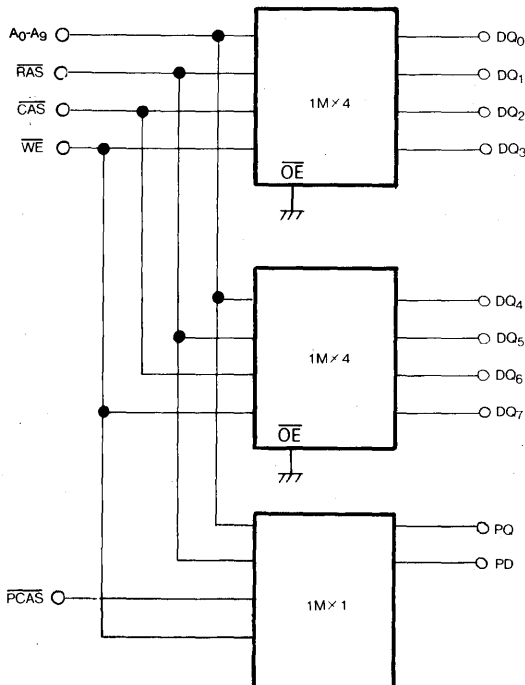
- Fast Page Mode operation
- Fast Access Time

	t_{RAC}	t_{CAC}	t_{PC}
HYM591000BM-60	60	20	40
HYM591000BM-70	70	20	45
HYM591000BM-80	80	25	55

- Single power supply of 5V± 10%
- $\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh.
- Low power operating
  1.68W max (HYM591000BM-60)
  1.51W max (HYM591000BM-70)
  1.35W max (HYM591000BM-80)
- TTL compatible inputs and outputs
- 1024 refresh cycles/16ms

4

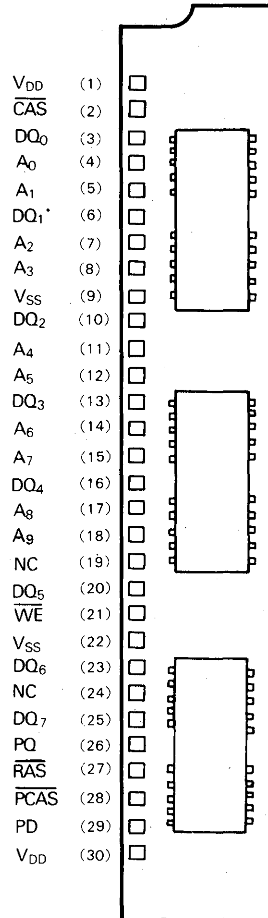
BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
PD	DATA IN FOR PARITY
PQ	DATA OUT FOR PARITY
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{PCAS}$	CAS FOR PARITY
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS



NOTES :

1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
2. Separate $\overline{PCAS}$ control for one separate pair of data-in (PD) and data-out (PQ) lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	2.1	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS
(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM591000BM MIN.	HYM591000BM MAX.	UNIT	NOTE
$\mid I_{LI} \mid$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$		−	30	μA	
$\mid I_{LO} \mid$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		−	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min)	−60	−	305	mA	1
			−70	−	275		
			−80	−	245		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}		−	6	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60	−	305	mA	
			−70	−	275		
			−80	−	245		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−60	−	205	mA	1
			−70	−	175		
			−80	−	145		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs ≥ V_{SS}		−	3	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60	−	305	mA	
			−70	−	275		
			−80	−	245		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		−	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	−	V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.

4

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1. 2. 3

#	SYMBOL	PARAMETER	HYM591000BM						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
3	t_{RP}	$\overline{RAS}$ Prechange Time	50	–	50	–	60	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	60	ns	8
11	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	4,8,9
12	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	4,9
13	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	4,8
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
20	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
24	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
27	t_{DS}	Data In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data In Hold Time	15	–	15	–	15	–	ns	7

#	SYMBOL	PARAMETER	HYM591000BM						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
30	t_{CPA}	Access Time from Column Precharge	–	35	–	40	–	50	ns	4
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	40	–	45	–	55	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	200K	70	200K	80	200K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40	–	40	–	50	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	4
42	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
43	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :
1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

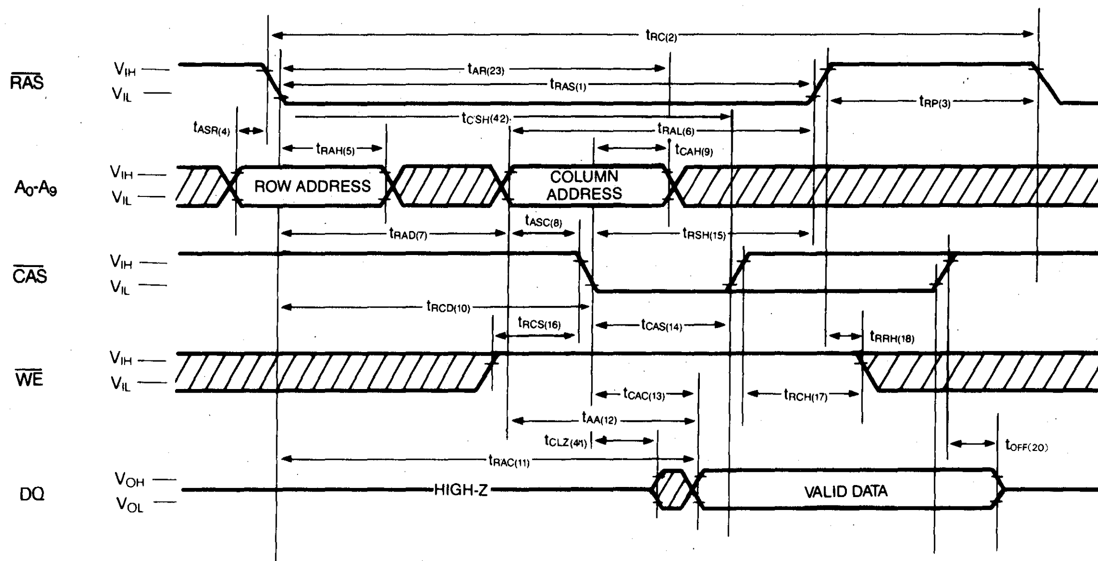
CAPACITANCE

(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

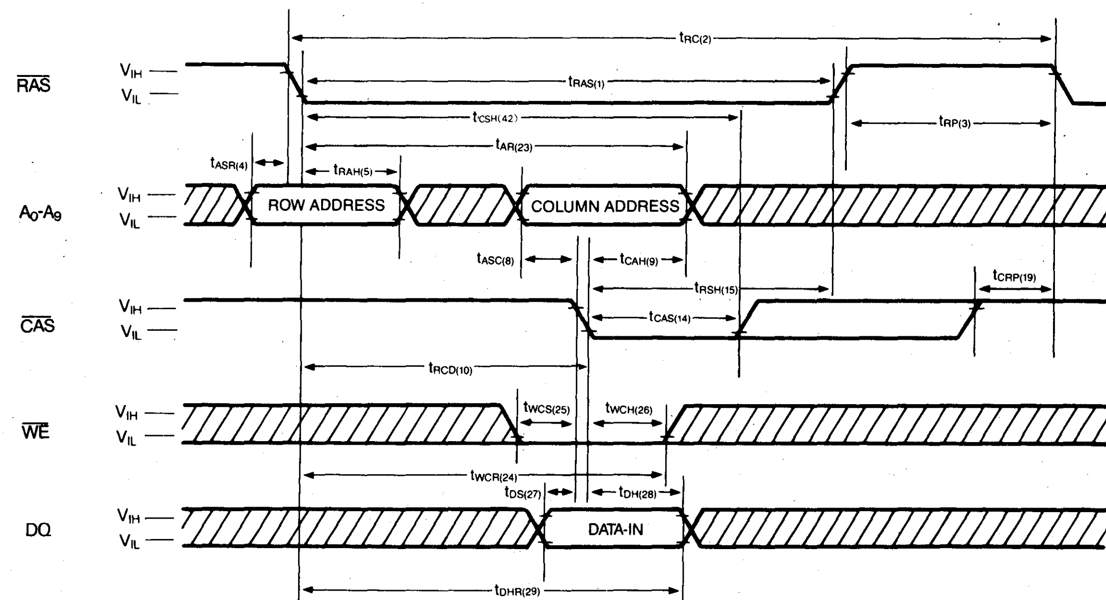
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_9, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	25	pF
C_{IN2}	Input Capacitance(PD, $\overline{PCAS}$)	–	10	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF
C_{PQ}	Output Capacitance(PQ)	–	10	pF

TIMING DIAGRAM

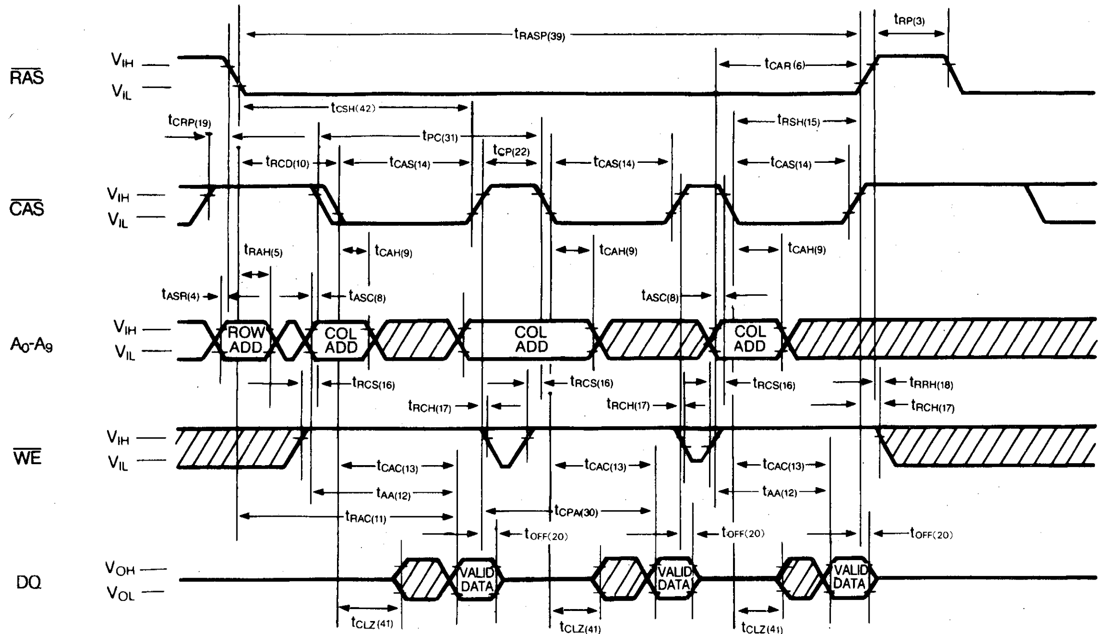
READ CYCLE



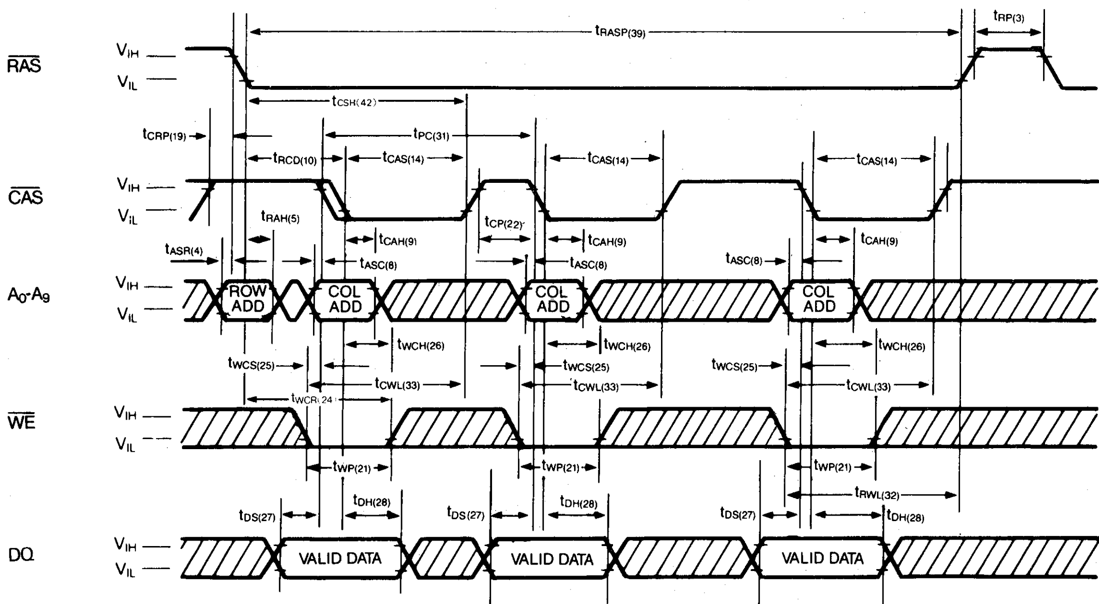
EARLY WRITE CYCLE



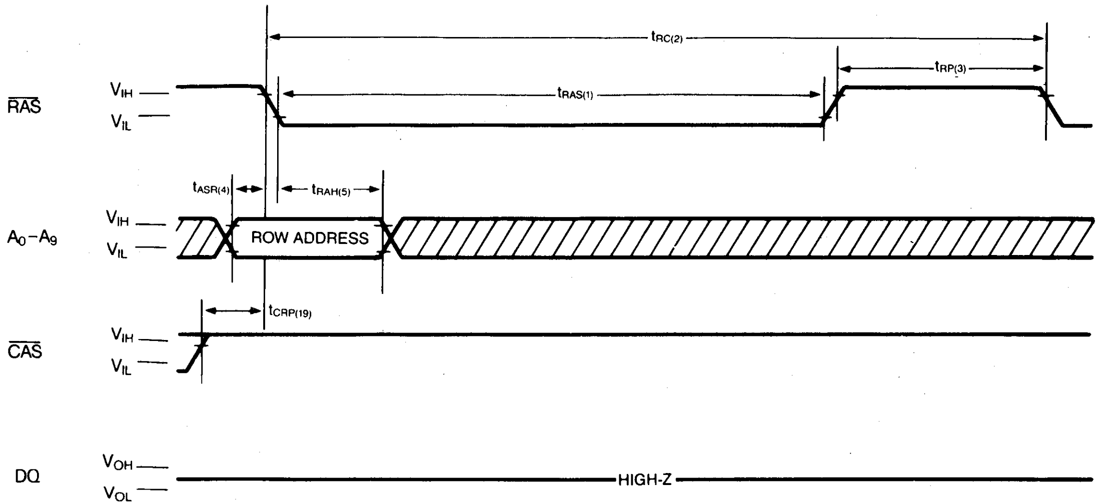
FAST PAGE MODE READ CYCLE



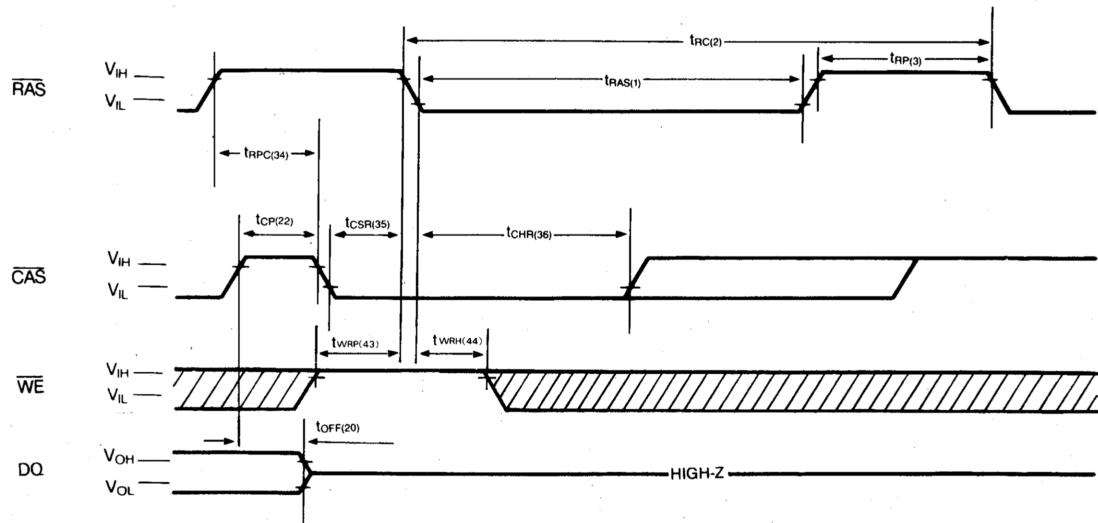
FAST PAGE MODE EARLY WRITE CYCLE



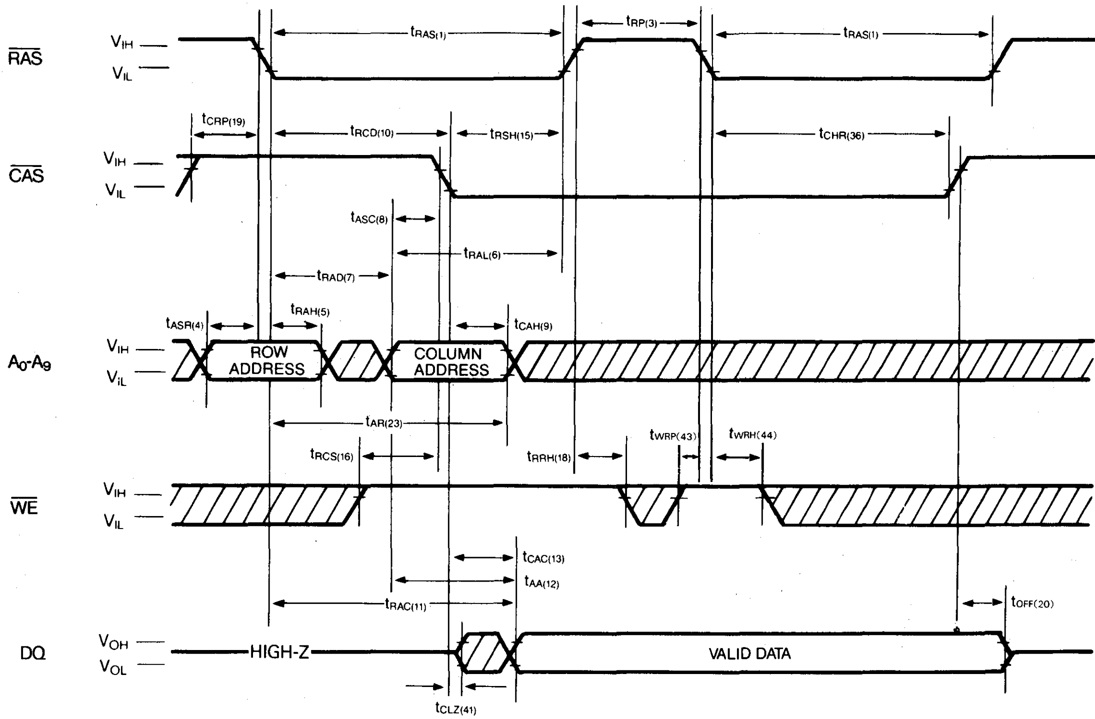
$\overline{RAS}$-ONLY REFRESH CYCLE



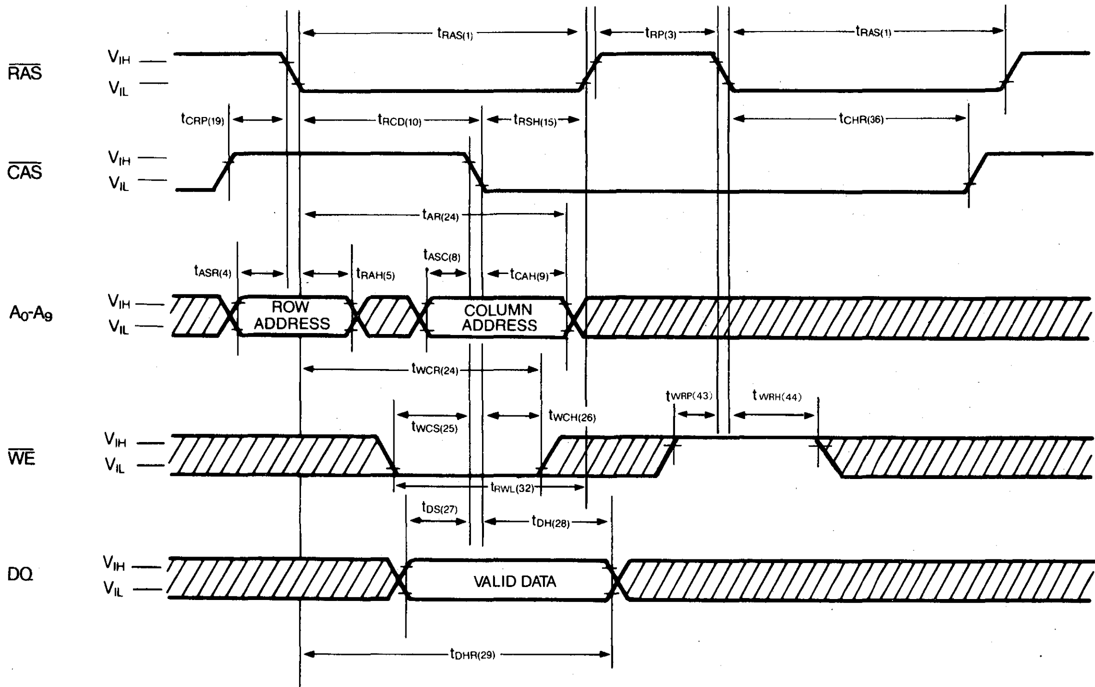
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



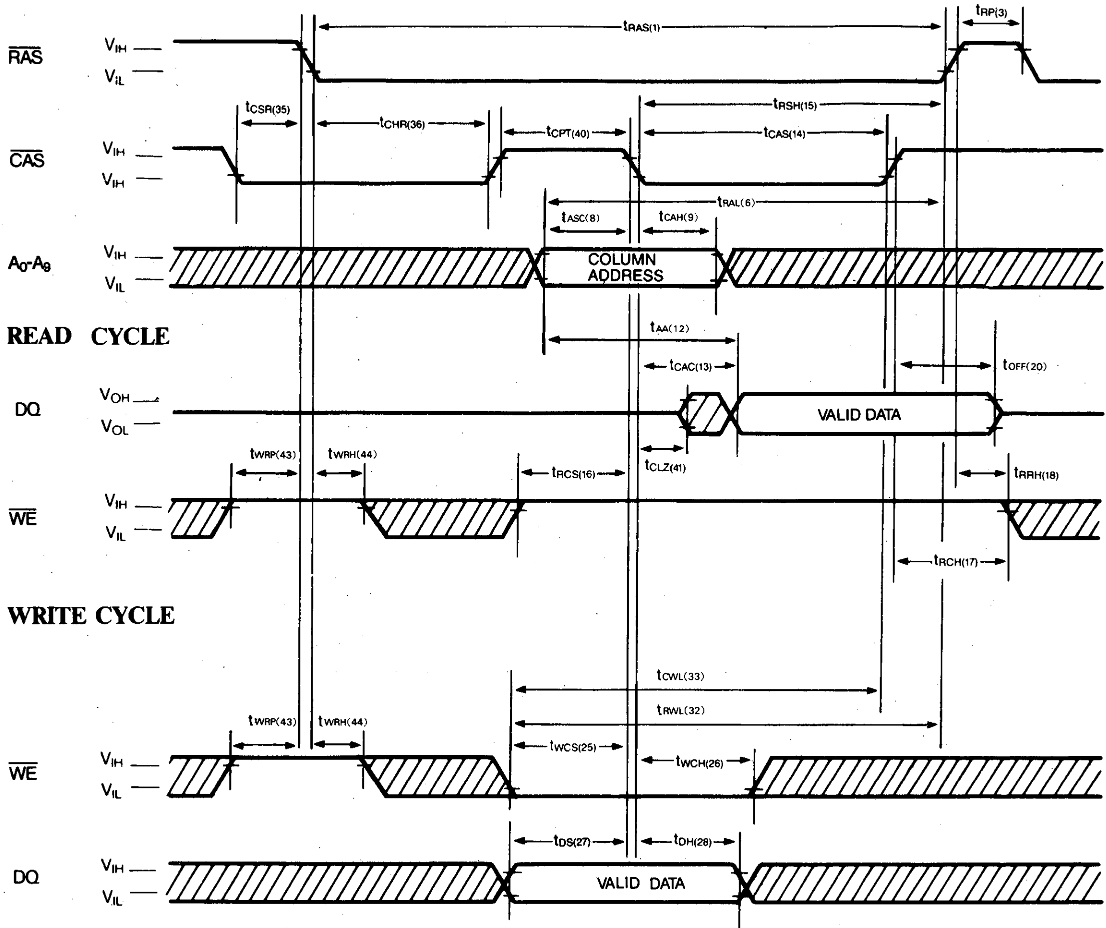
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

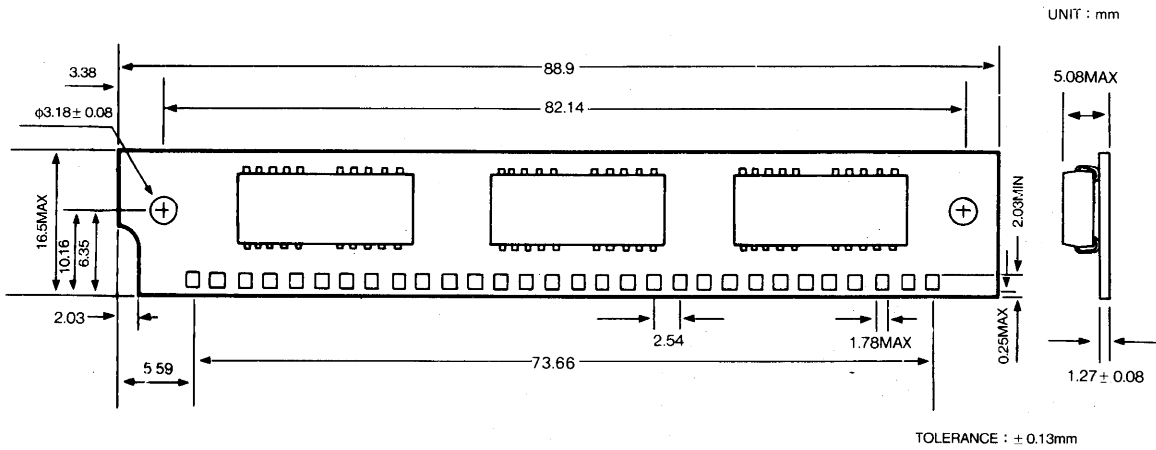


$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE

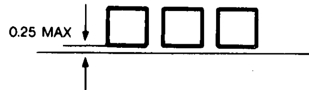


PACKAGE INFORMATION

HYM591000BM



* DETAIL OF CONTACTS



MEMO

•HYUNDAI SEMICONDUCTOR

HYM591000BL

1M×9-Bit CMOS DRAM MODULE

M4N1200A-MAR92

DESCRIPTION

The HYM591000BM is a 1M words by 9 bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of two HY514400ALJ and one HY531000ALJ both in 20/26 pin SOJ mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM591000BLM is a socket type single-in line module suitable for easy interchange and addition of 1M bytes memory with parity RAM.

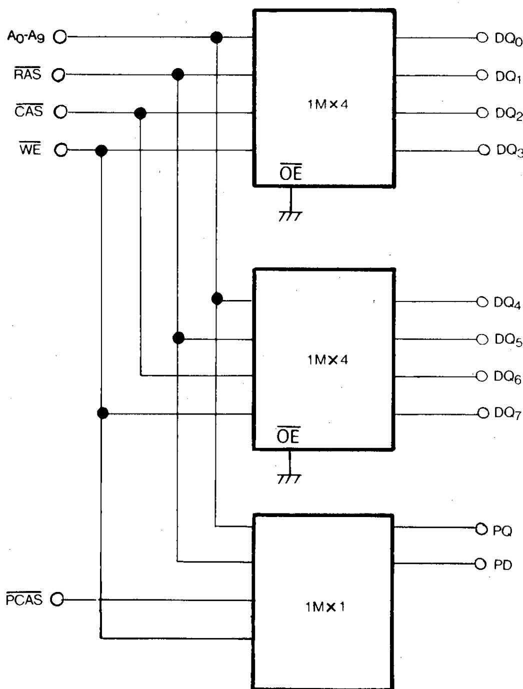
FEATURES

- Fast Page Mode operation
- Fast Access Time

	t_{RAC}	t_{CAC}	t_{PC}
HYM591000BLM-60	60	20	40
HYM591000BLM-70	70	20	45
HYM591000BLM-80	80	25	55

- Single power supply of 5V± 10%
- $\overline{CAS}$-Before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden Refresh.
- Low power operating
  1.68W max (HYM591000BLM-60)
  1.51W max (HYM591000BLM-70)
  1.35W max (HYM591000BLM-80)
- TTL compatible inputs and outputs
- 1024 refresh cycles/128ms

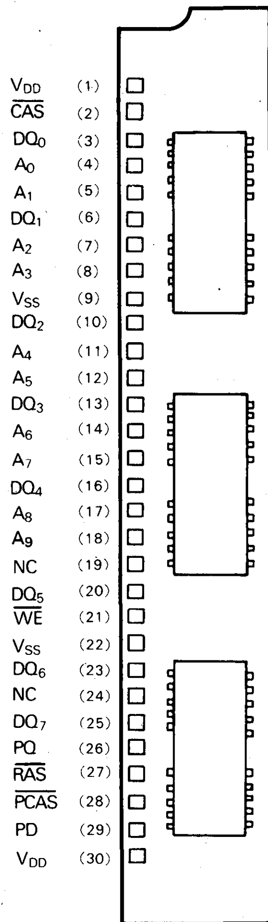
BLOCK DIAGRAM



PIN NAMES

A0-A9	ADDRESS INPUT
DQ0-DQ7	DATA INPUT/OUTPUT
PD	DATA IN FOR PARITY
PQ	DATA OUT FOR PARITY
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{PCAS}$	CAS FOR PARITY
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS



NOTES :

1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
2. Separate $\overline{PCAS}$ control for one separate pair of data-in (PD) and data-out (PQ) lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	1.8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM591000BLM MIN.	HYM591000BLM MAX.	UNIT	NOTE
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		–	30	µA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		–	10	µA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min)	60	–	305	mA	1
			70	–	275		
			80	–	245		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\geq V_{SS}$		–	6	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	60	–	305	mA	
			70	–	275		
			80	–	245		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	60	–	205	mA	1
			70	–	175		
			80	–	145		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs $\geq V_{SS}$		–	0.6	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	60	–	305	mA	
			70	–	275		
			80	–	245		
I_{DD7}	V_{DD} Supply Current, Battery Back up	$\overline{CAS}$=CBR cycling or 0.2V, $\overline{OE}=\overline{WE}=V_{DD}-0.2V$, Add=$V_{DD}$−0.2V or 0.2V, I/O=$V_{DD}$−0.2V or 0.2V or open, t_{RC}=125µs, $t_{RAS}=t_{RAS}$(min.)~300ns		–	0.9	mA	1
		Same as above except t_{RAS}=300ns~1µs		–	1.2	mA	1, 5
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTES :

1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1. 2. 3

#	SYMBOL	PARAMETER	HYM591000BLM						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
3	t_{RP}	$\overline{RAS}$ Prechange Time	50	–	50	–	60	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	60	ns	8
11	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	4,8,9
12	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	4,9
13	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	4,8
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
20	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
24	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
27	t_{DS}	Data In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data In Hold Time	15	–	15	–	15	–	ns	7

#	SYMBOL	PARAMETER	HYM591000BM						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
30	t_{CPA}	Access Time from Column Precharge	–	35	–	40	–	50	ns	4
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	40	–	45	–	55	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	128	–	128	–	128	ms	
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	200K	70	200K	80	200K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40	–	40	–	50	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	4
42	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
43	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

CAPACITANCE

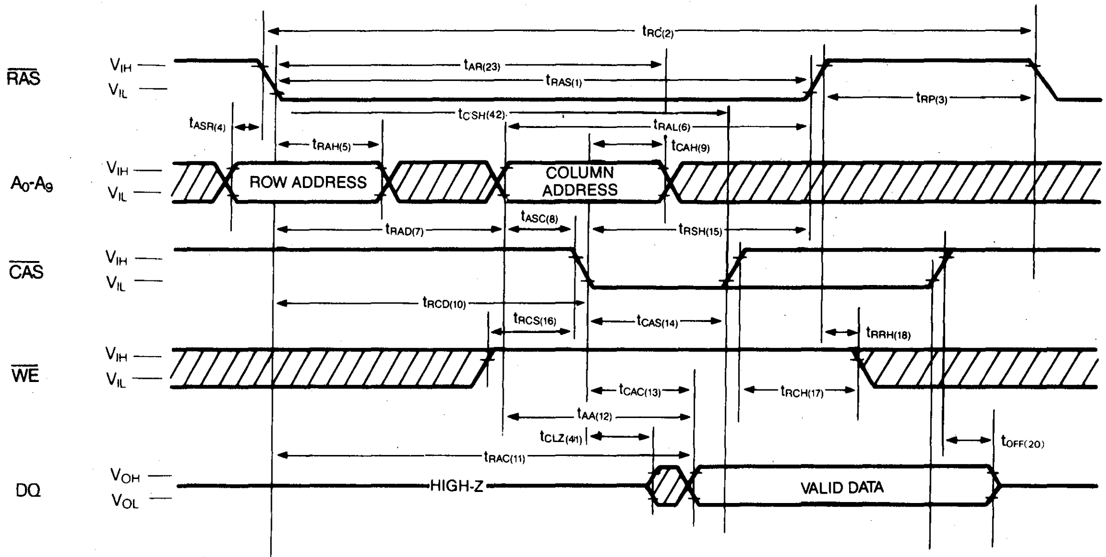
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_9, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	25	pF
C_{IN2}	Input Capacitance(PD, $\overline{PCAS}$)	–	10	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF
C_{PQ}	Output Capacitance(PQ)	–	10	pF

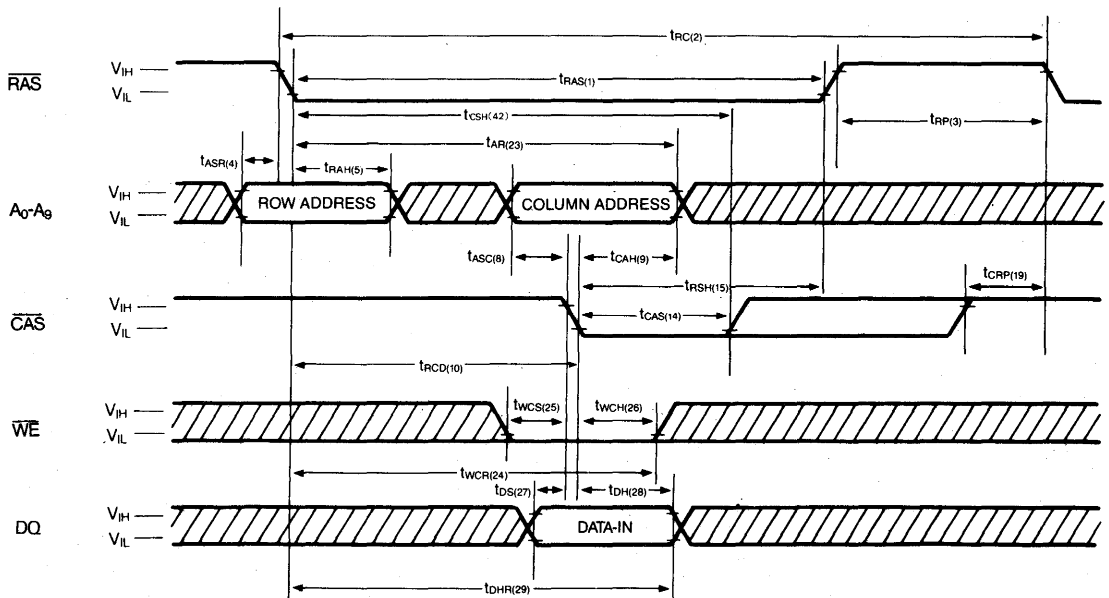
4

TIMING DIAGRAM

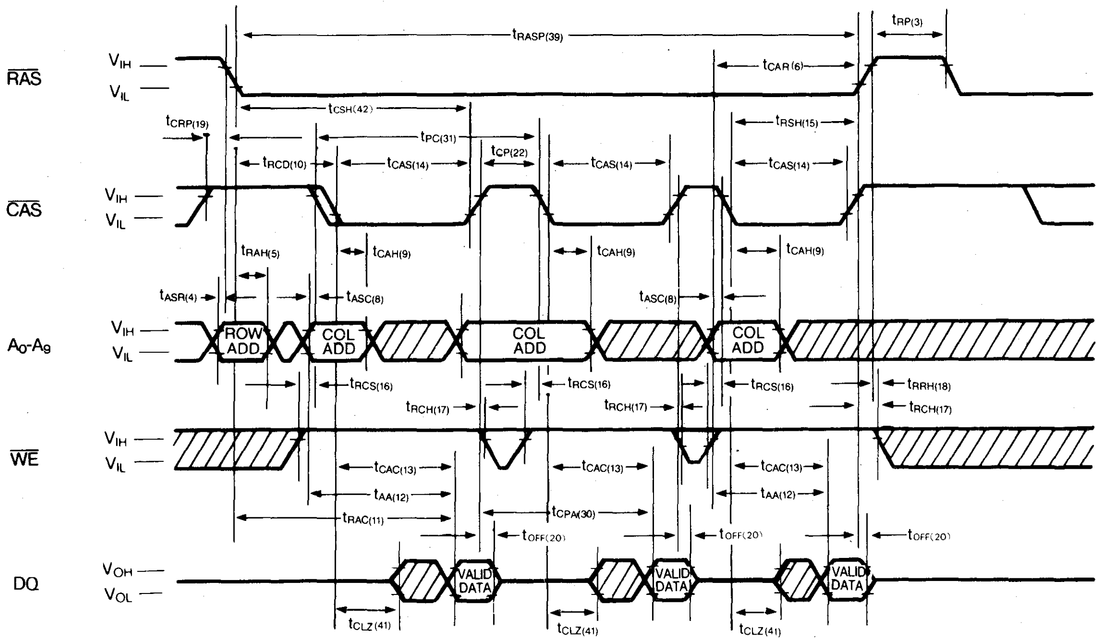
READ CYCLE



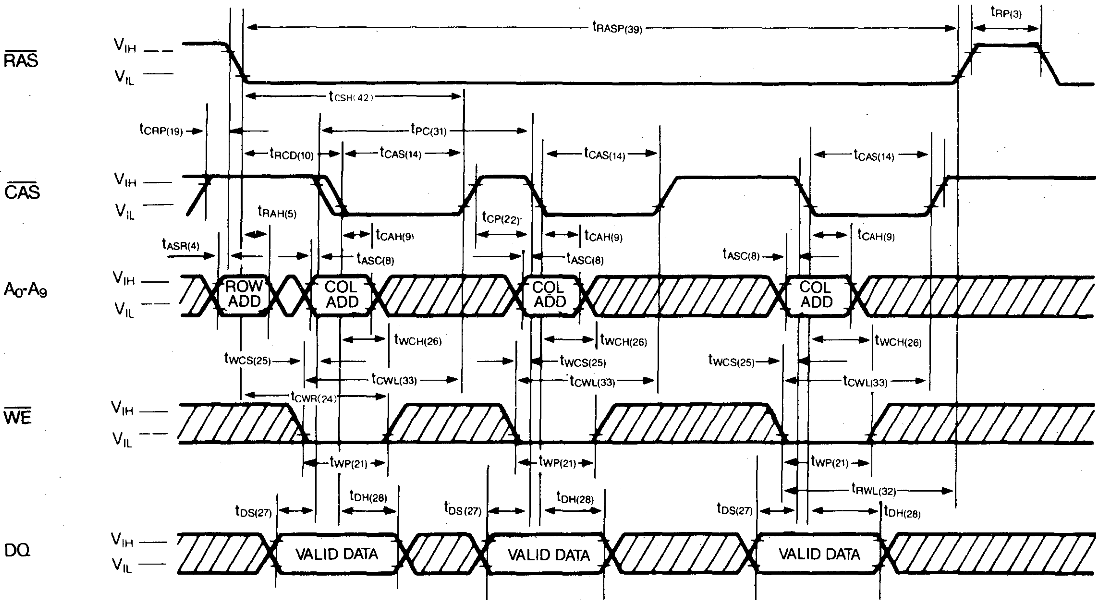
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

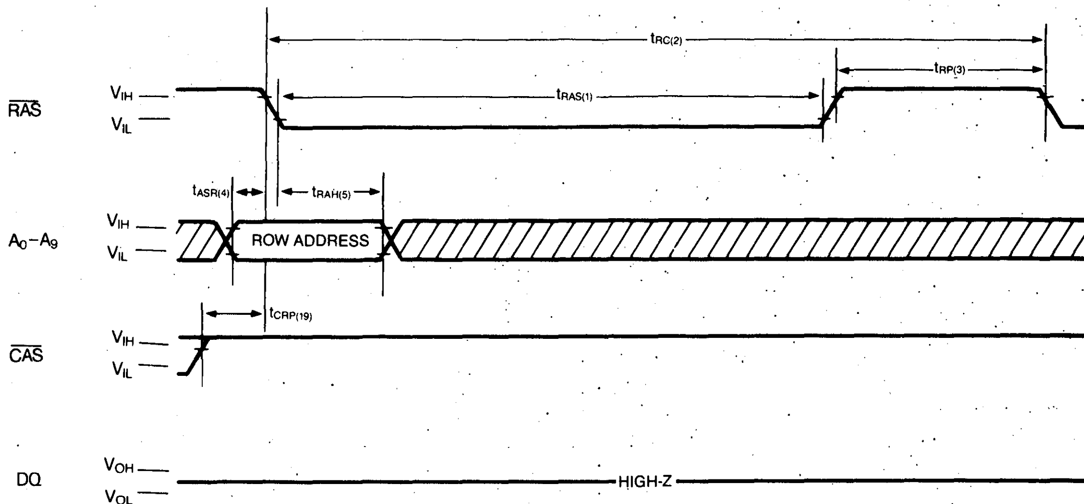


FAST PAGE MODE EARLY WRITE CYCLE

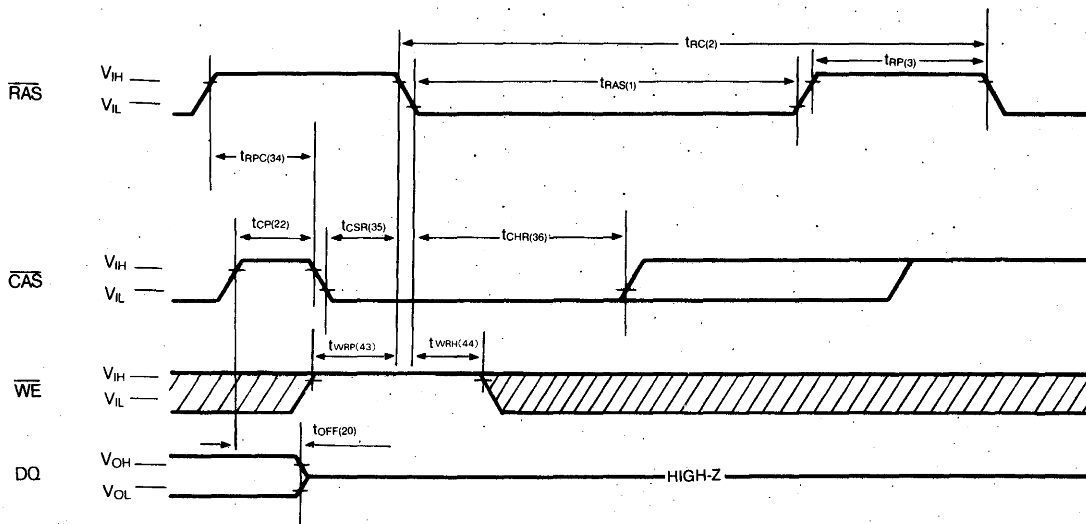


4

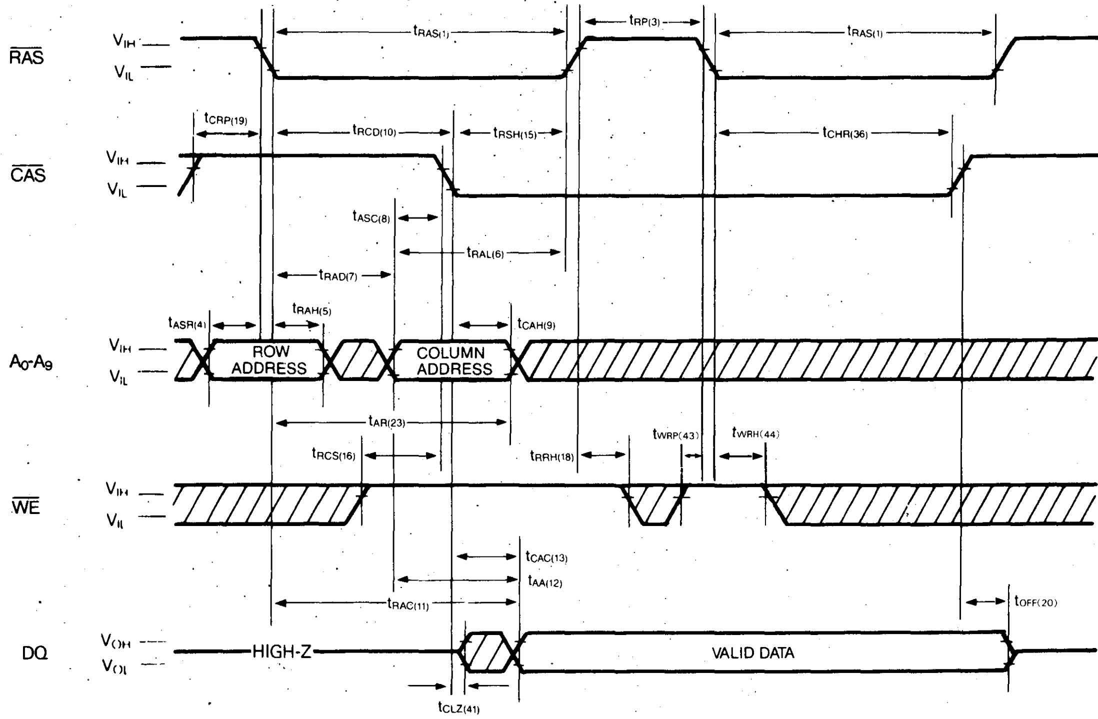
$\overline{RAS}$-ONLY REFRESH CYCLE



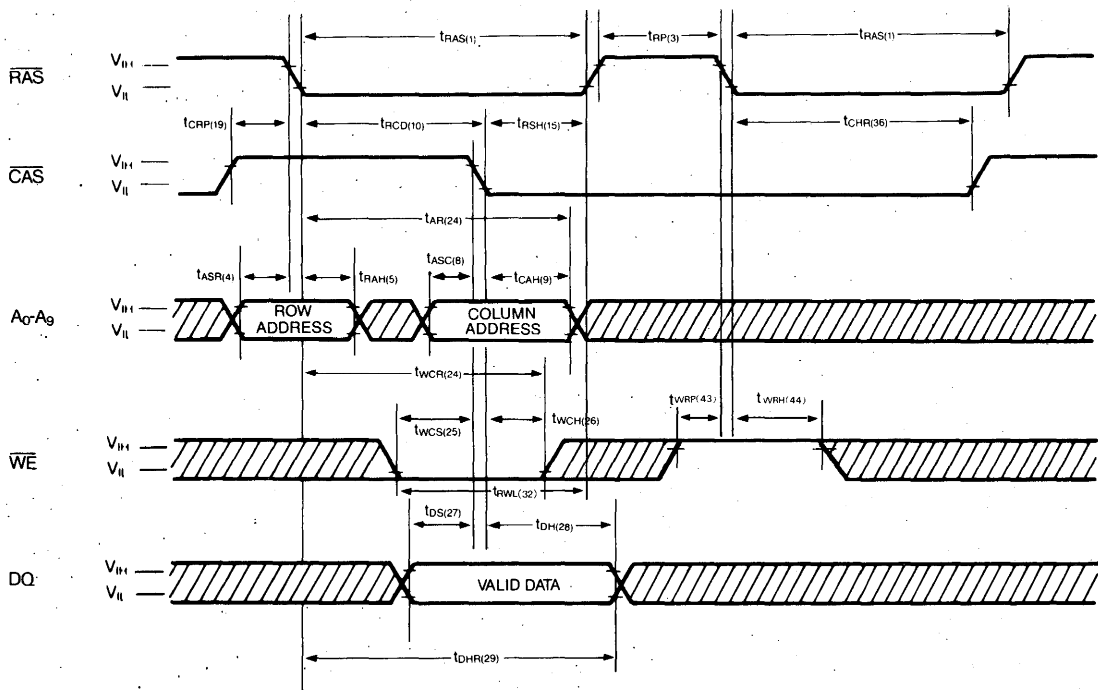
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



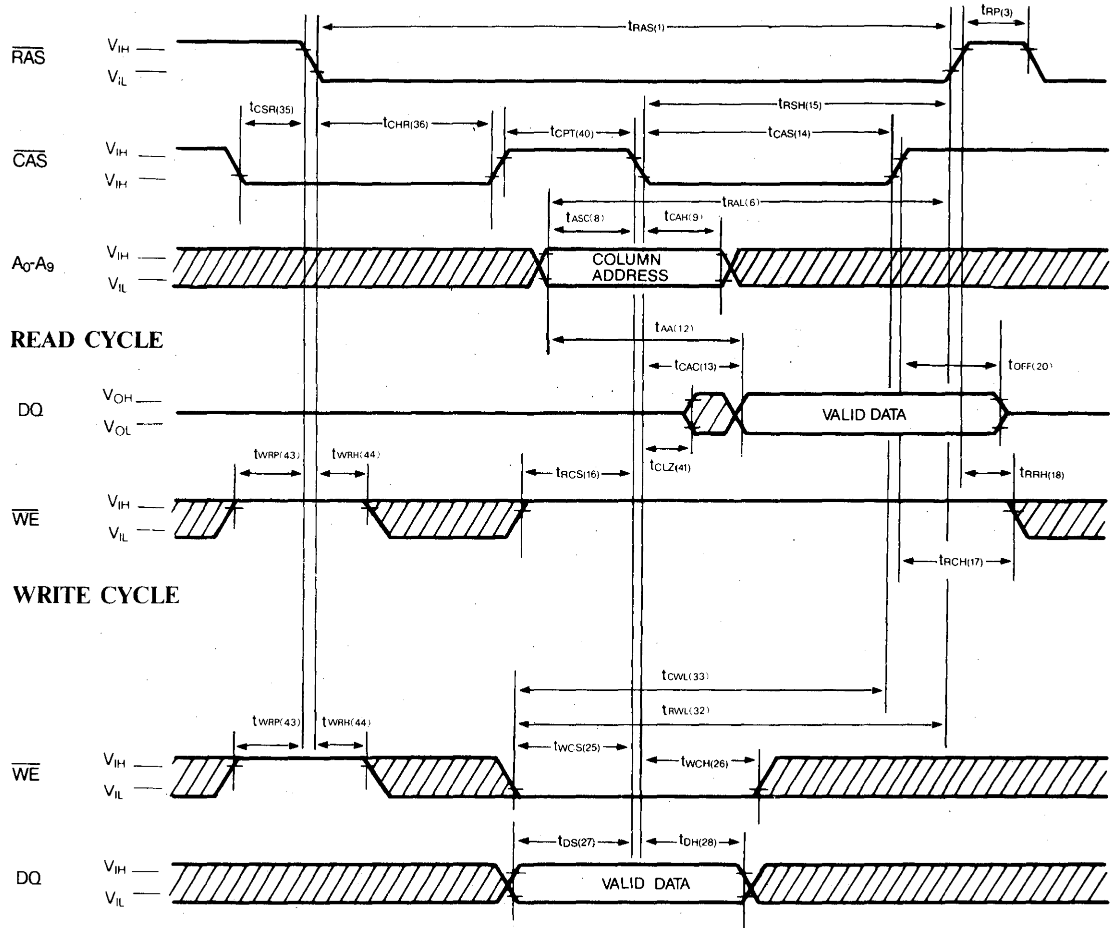
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

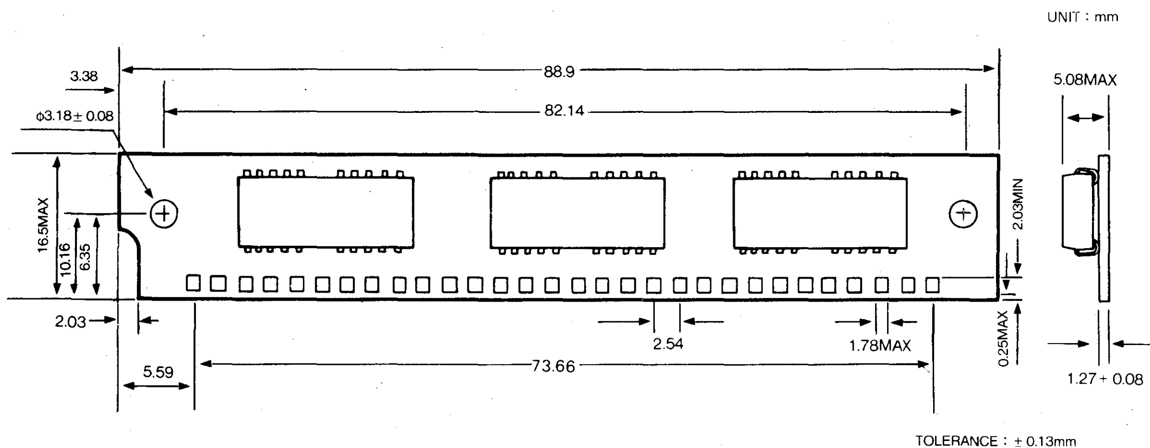


$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE

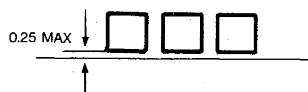


PACKAGE INFORMATION

HYM591000BLM



* DETAIL OF CONTACTS



MEMO

HYUNDAI SEMICONDUCTOR

HYM584000

4M×8-Bit CMOS DRAM MODULE

M491202A-JAN92

DESCRIPTION

The HYM584000M is a 4M words by 8bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of eight HY514100J in 20/26 pin SOJ mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM584000M is a socket type single-in line module suitable for easy interchange and addition of 4M bytes memory.

FEATURES

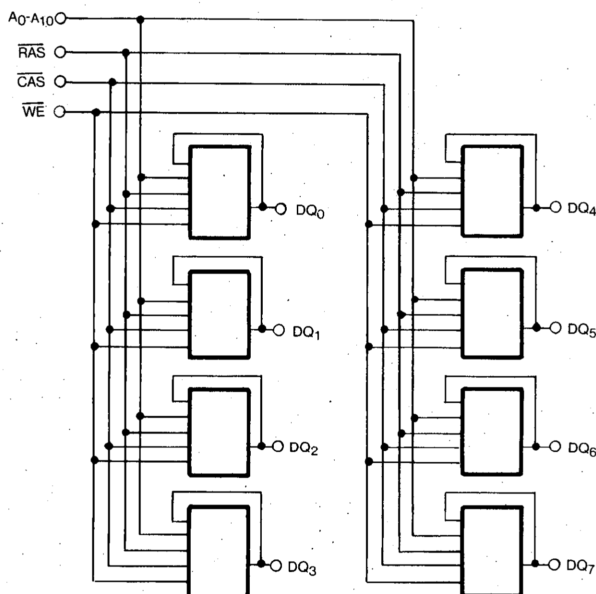
- Fast Page Mode operation
- Fast Access Time

	t_{RAC}	t_{CAC}	t_{PC}
HYM584000M-70	70	20	50
HYM584000M-80	80	25	55
HYM584000M-10	100	25	60

- Single power supply of 5V± 10%
- $\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh.
- Low power operating
  3.96W max (HYM584000M-70)
  3.52W max (HYM584000M-80)
  3.08W max (HYM584000M-10)
- TTL compatible inputs and outputs
- 1024 refresh cycles/16ms

4

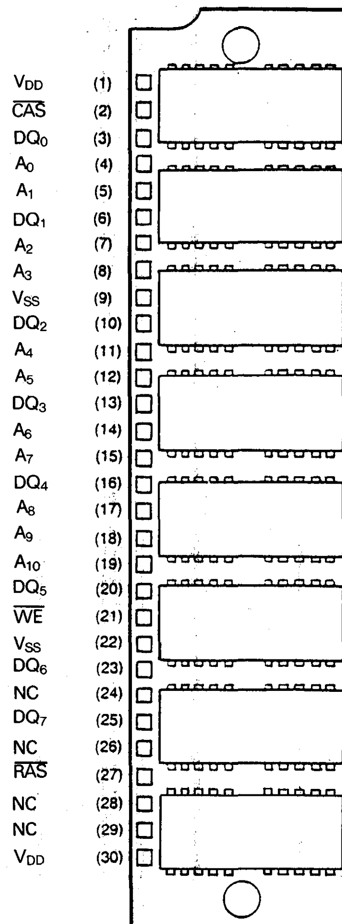
BLOCK DIAGRAM



PIN NAMES

A_0-A_{10}	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS



NOTES :
1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
2. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	4.8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS
(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM584000M		UNIT	NOTE
				MIN.	MAX.		
$\mid I_{LI} \mid$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		−	80	μA	
$\mid I_{LO} \mid$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		−	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min)	−70	−	720	mA	1
			−80	−	640		
			−10	−	560		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}		−	16	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−70	−	720	mA	
			−80	−	640		
			−10	−	560		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−70	−	560	mA	1
			−80	−	480		
			−10	−	400		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs ≥ V_{SS}		−	8	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−70	−	720	mA	
			−80	−	640		
			−10	−	560		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		−	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	−	V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1, 2, 3

#	SYMBOL	PARAMETER	HYM584000M						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	45	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	55	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	55	25	75	ns	8
11	t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	4,8,9
12	t_{AA}	Access Time from Column Address	–	35	–	40	–	45	ns	4,9
13	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	–	25	ns	4,8
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	25	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
20	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55	–	60	–	80	–	ns	
24	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55	–	60	–	80	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
27	t_{DS}	Data In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data In Hold Time	15	–	15	–	20	–	ns	7

#	SYMBOL	PARAMETER	HYM584000M						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	55	–	60	–	80	–	ns	
30	t_{CPA}	Access Time from Column Precharge	–	45	–	50	–	55	ns	4
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	50	–	55	–	60	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	30	–	30	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
39	t_{RASP}	RAS Pulse Width(Fast Page Mode)	70	200K	80	200K	100	200K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40	–	40	–	50	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	4
42	t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
43	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :
1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

CAPACITANCE

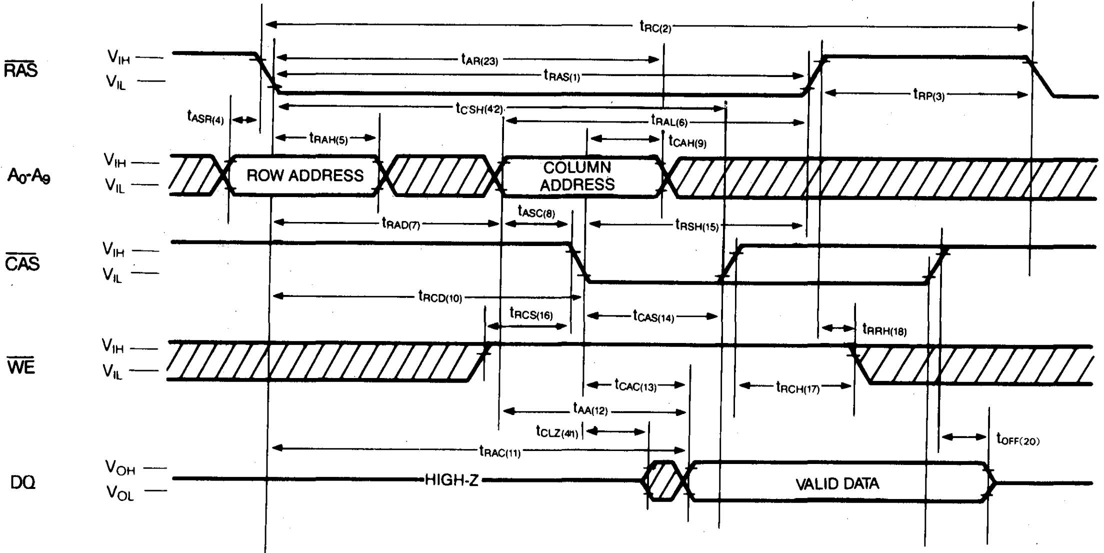
(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance(A_0-A_{10}, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	55	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF

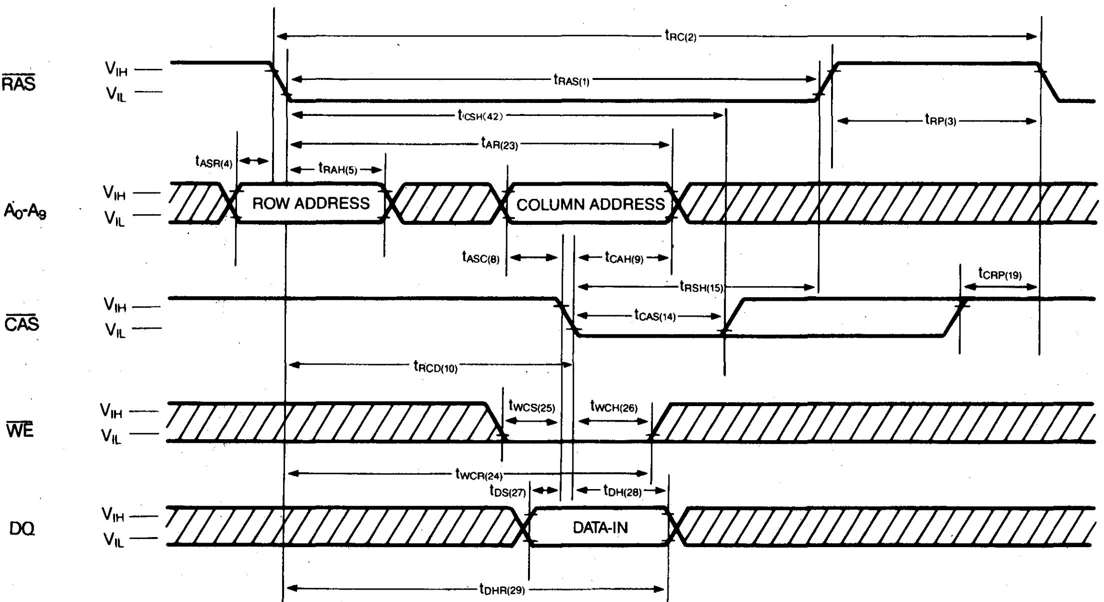
4

TIMING DIAGRAM

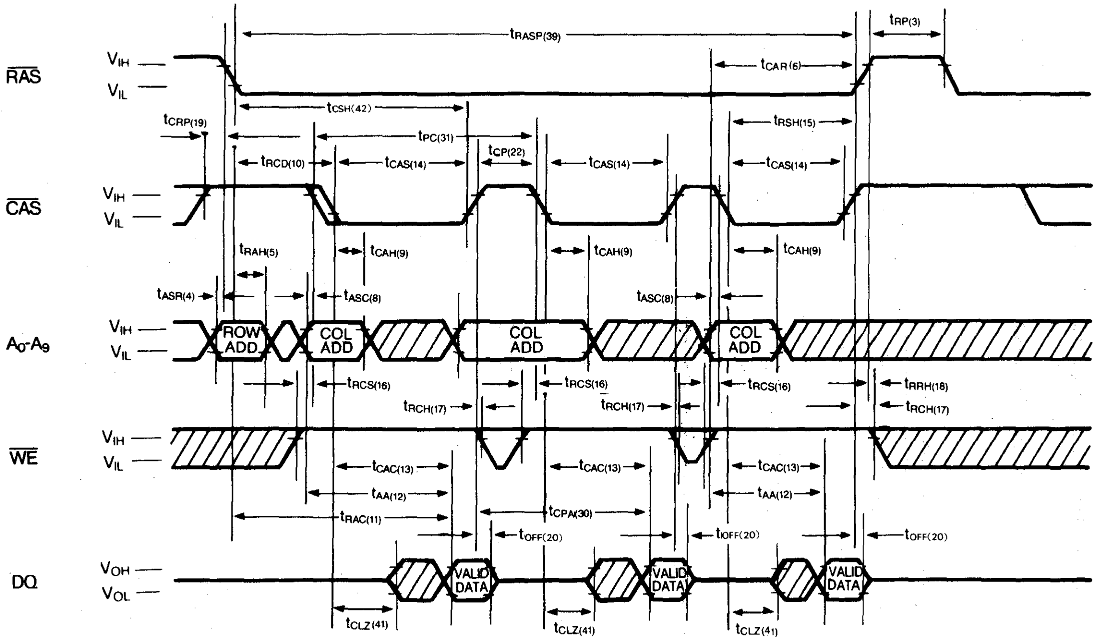
READ CYCLE



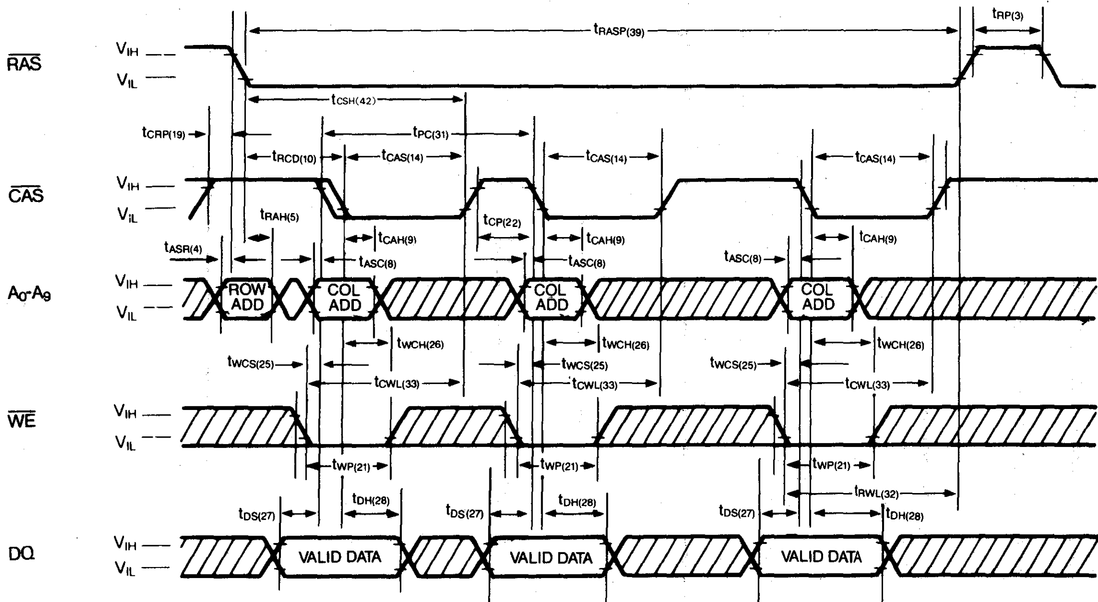
EARLY WRITE CYCLE



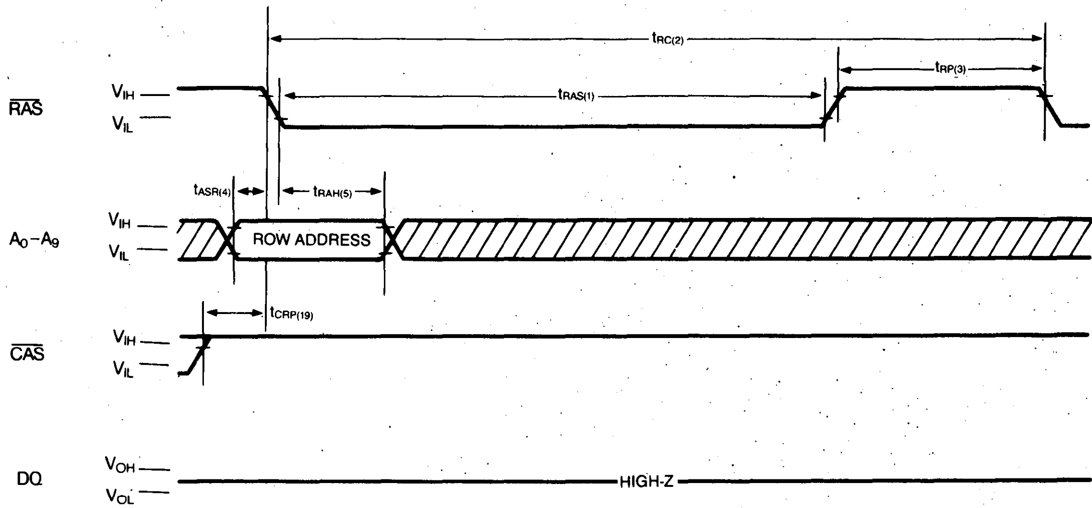
FAST PAGE MODE READ CYCLE



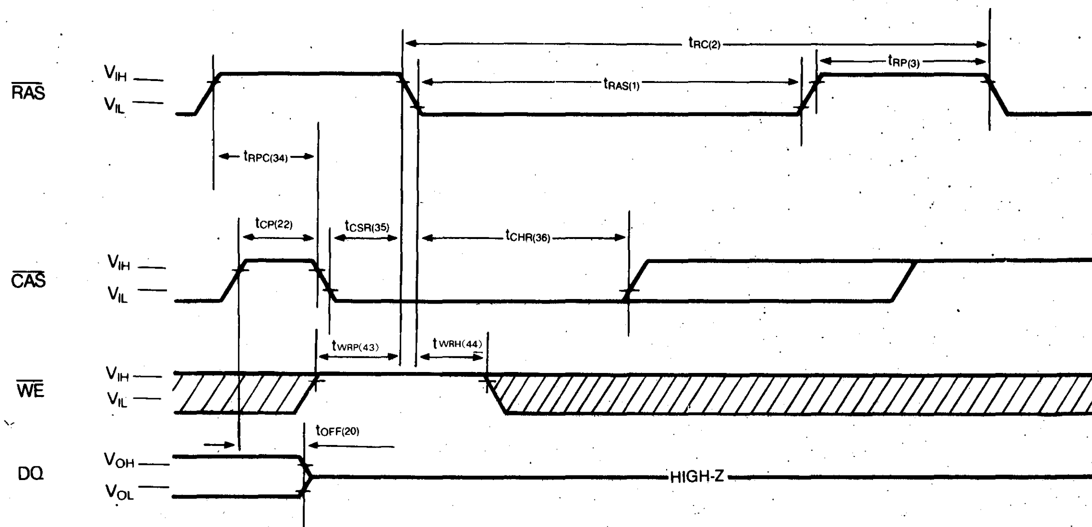
FAST PAGE MODE EARLY WRITE CYCLE



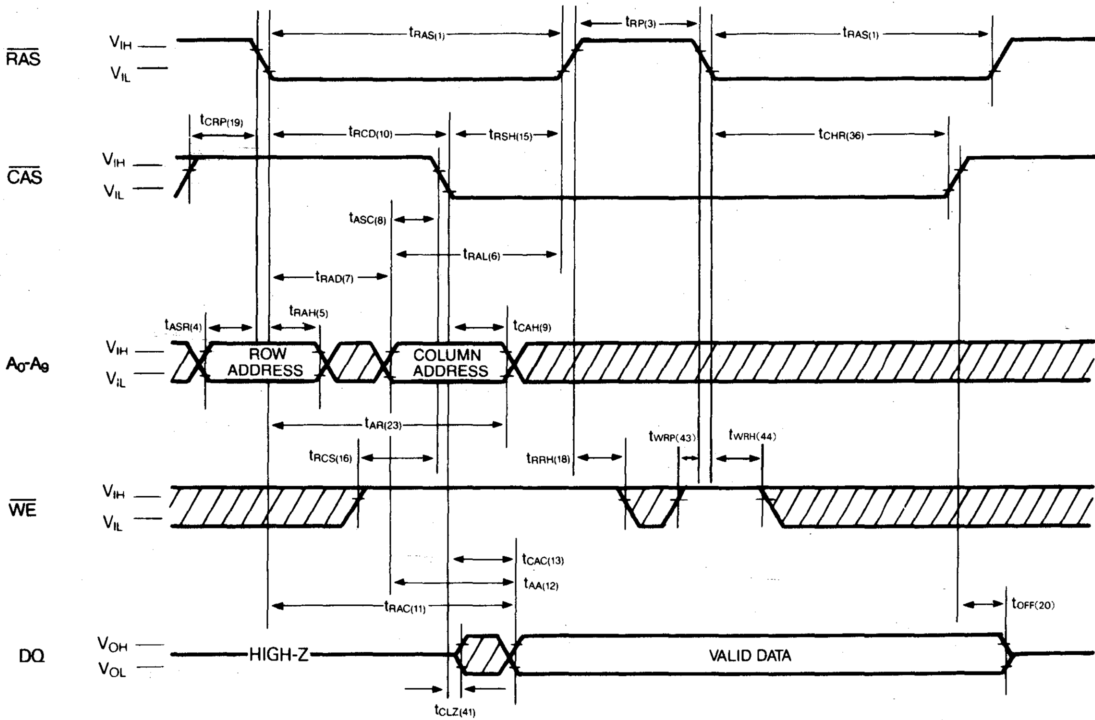
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE



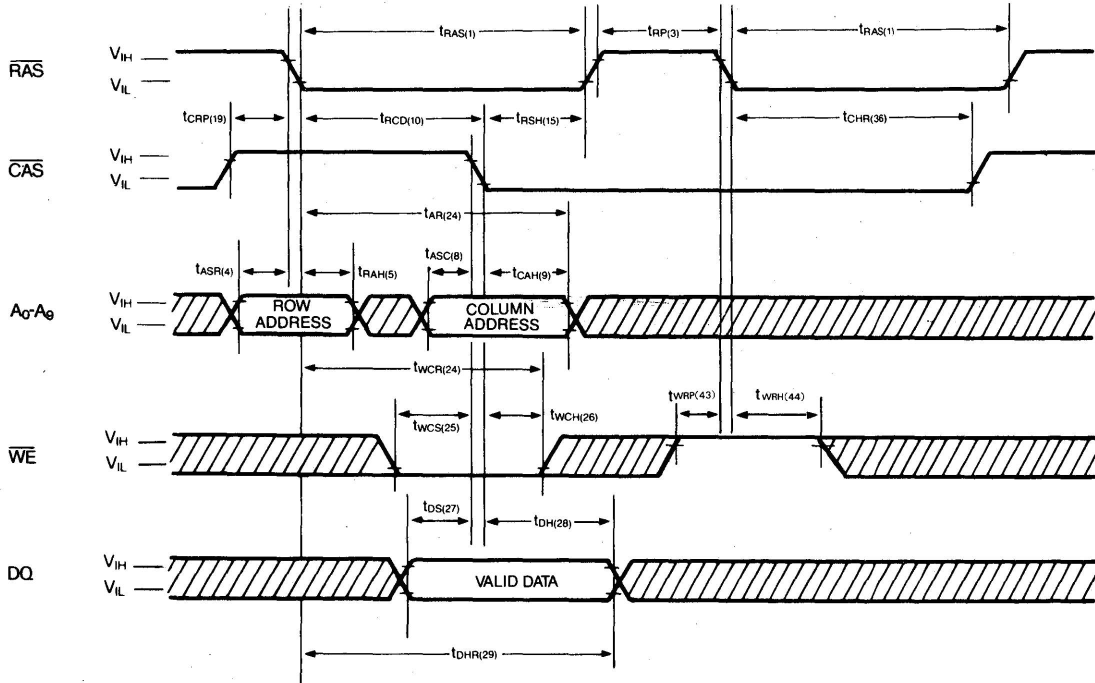
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE



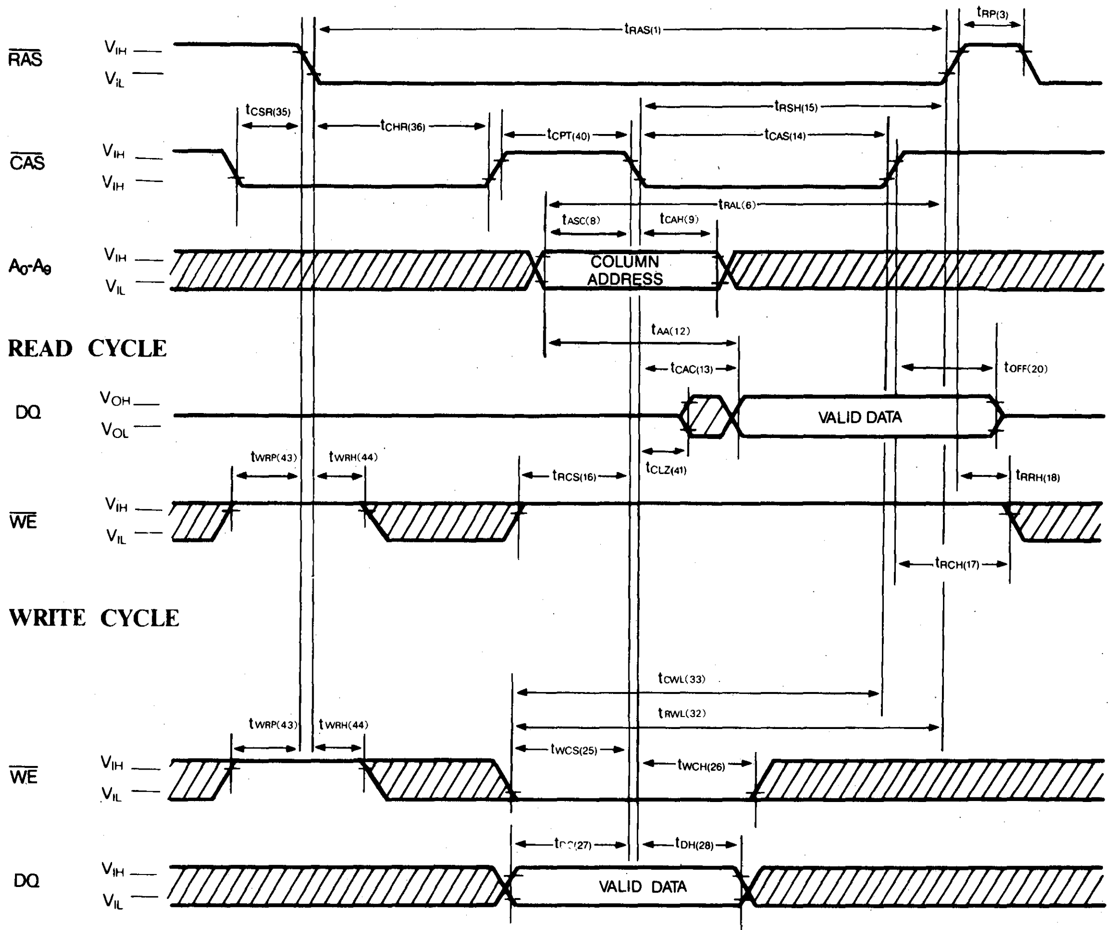
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

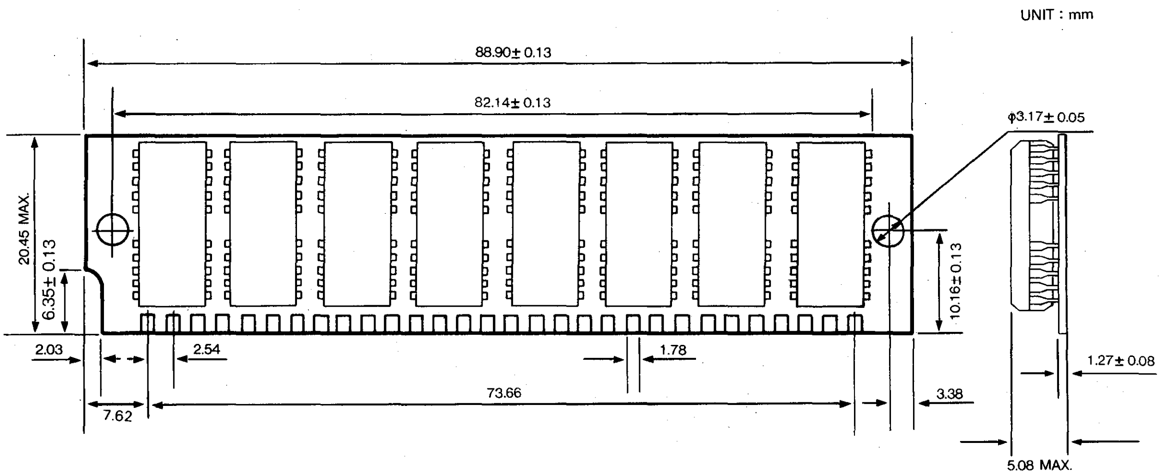


$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE

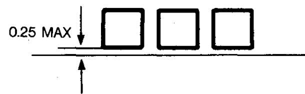


PACKAGE INFORMATION

HYM584000M



* DETAIL OF CONTACTS



MEMO

HYUNDAI SEMICONDUCTOR

HYM584000A

4M×8-Bit CMOS DRAM MODULE

M4H1200A-MAR92

DESCRIPTION

The HYM584000AM is a 4M words by 8 bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of eight HY514100AJ in 20/26 pin SOJ mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM584000AM is a socket type single-in line module suitable for easy interchange and addition of 4M bytes memory.

FEATURES

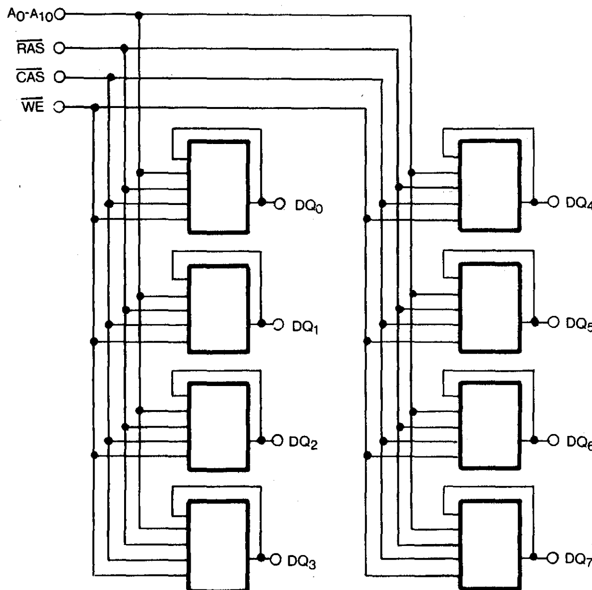
- Fast Page Mode operation
- Fast Access Time

	t_{RAC}	t_{CAC}	t_{PC}
HYM584000AM-60	60	20	40
HYM584000AM-70	70	20	45
HYM584000AM-80	80	25	55

- Single power supply of 5V± 10%
- $\overline{CAS}$-Before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden Refresh.
- Low power operating
  4.62W max (HYM584000AM-60)
  4.18W max (HYM584000AM-70)
  3.74W max (HYM584000AM-80)
- TTL compatible inputs and outputs
- 1024 refresh cycles/16ms

4

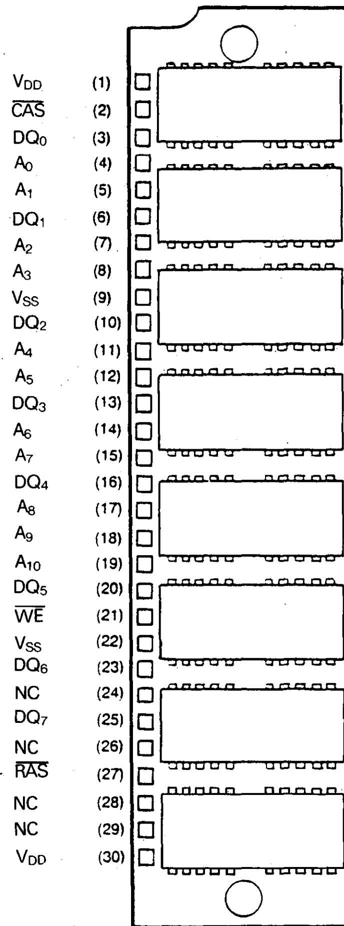
BLOCK DIAGRAM



PIN NAMES

A_0-A_9	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS



NOTES :

1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
2. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	5.88	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS
(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM584000AM		UNIT	NOTE
				MIN.	MAX.		
$\vert I_{LI}\vert$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		−	80	μA	
$\vert I_{LO}\vert$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		−	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min)	−60	−	840	mA	1
			−70	−	760		
			−80	−	680		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}		−	16	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60	−	840	mA	
			−70	−	760		
			−80	−	680		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−60	−	520	mA	1
			−70	−	440		
			−80	−	360		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}$ ≥ V_{DD}−0.2V, $\overline{CAS}$= V_{IH}, other inputs ≥ V_{SS}		−	8	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60	−	840	mA	
			−70	−	760		
			−80	−	680		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		−	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	−	V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1, 2, 3

#	SYMBOL	PARAMETER	HYM584000AM						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
3	t_{RP}	$\overline{RAS}$ Prechange Time	50	–	50	–	60	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	55	ns	8
11	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	4,8,9
12	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	4,9
13	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	4,8
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
20	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
24	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
27	t_{DS}	Data In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data In Hold Time	15	–	15	–	15	–	ns	7

#	SYMBOL	PARAMETER	HYM584000A						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
30	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	4
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	40	–	45	–	55	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	60	200K	75	200K	80	200K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	30	–	35	–	40	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	4
42	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
43	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	0	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :
1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

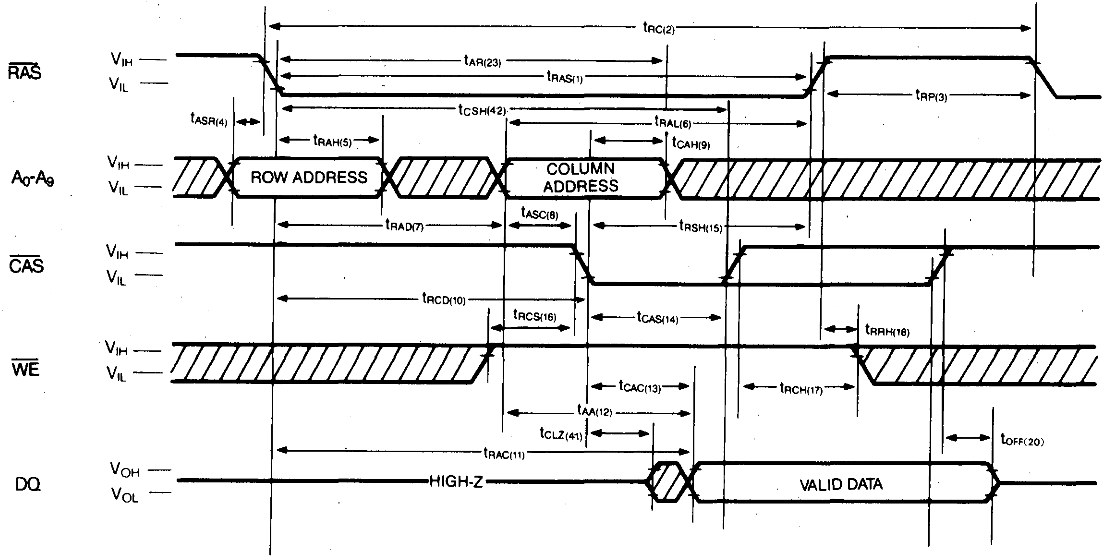
CAPACITANCE

(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

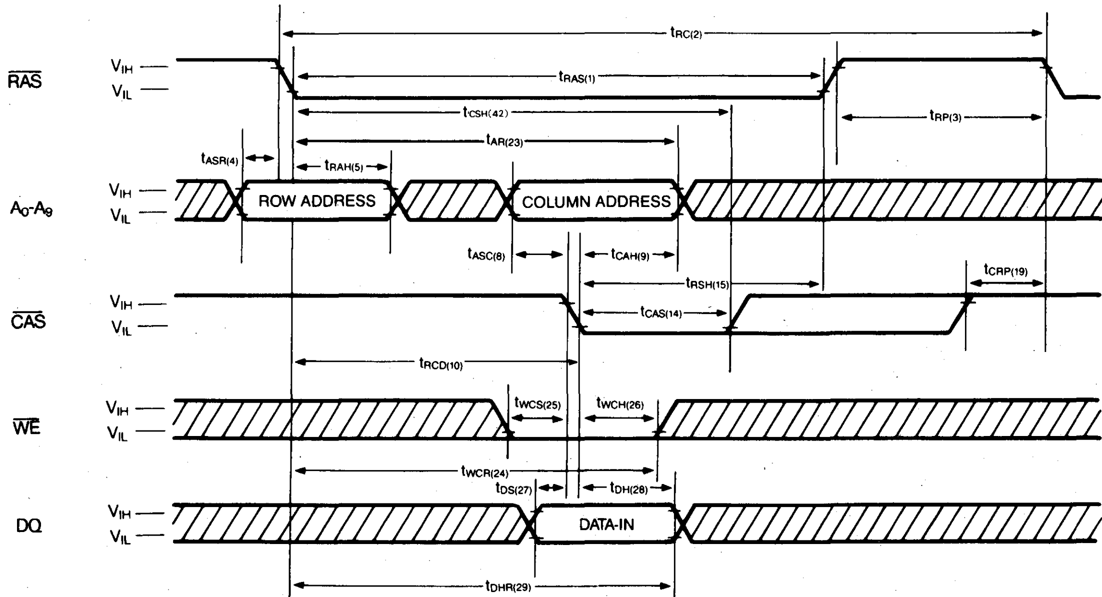
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance(A_0-A_9, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	55	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF

TIMING DIAGRAM

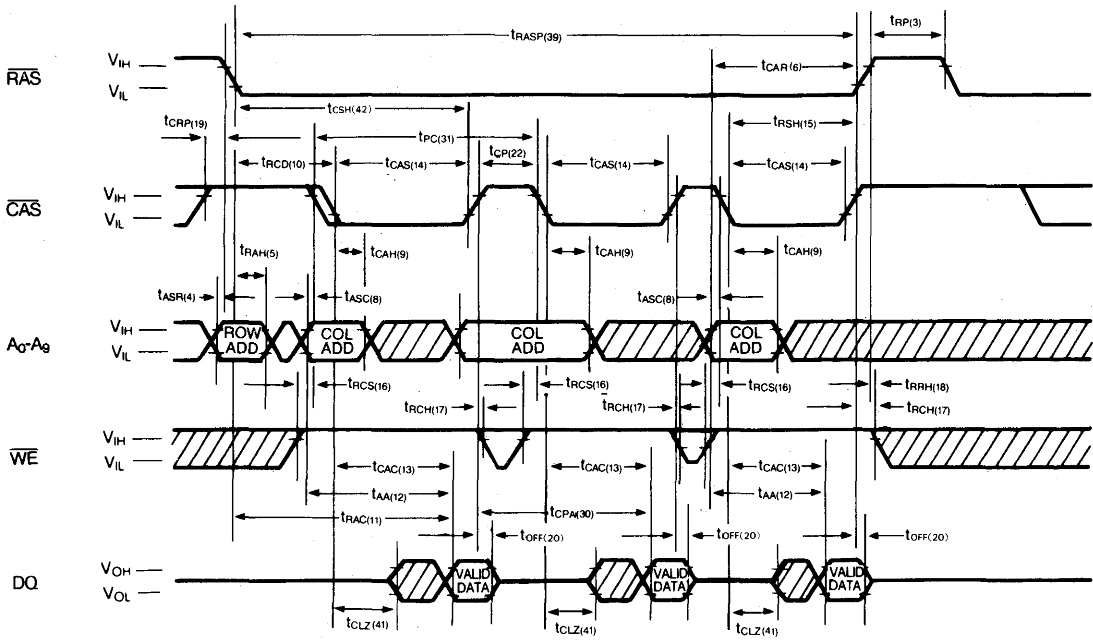
READ CYCLE



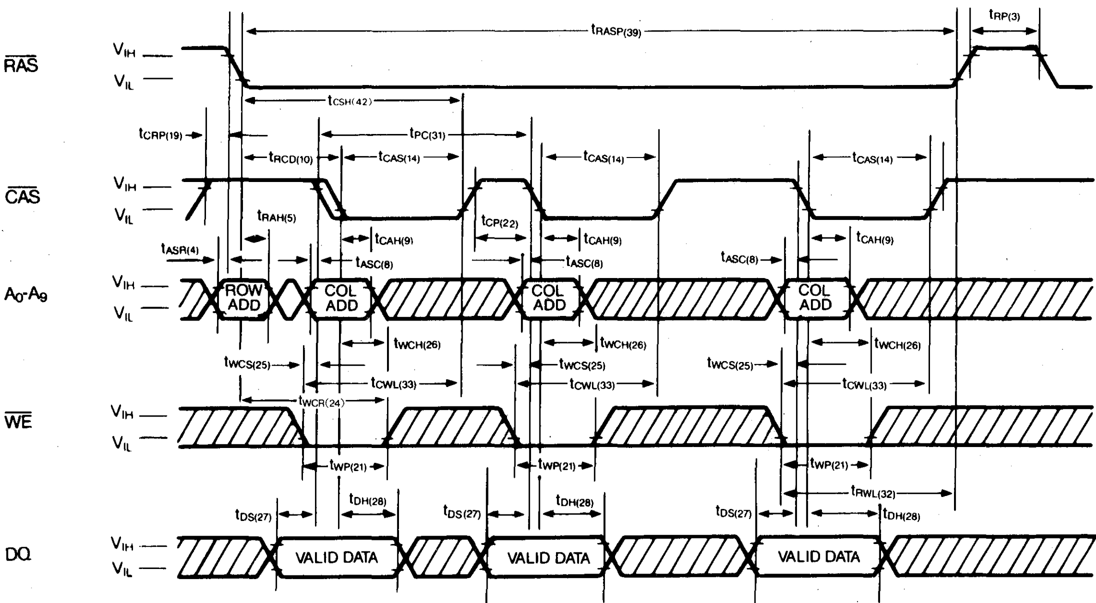
EARLY WRITE CYCLE



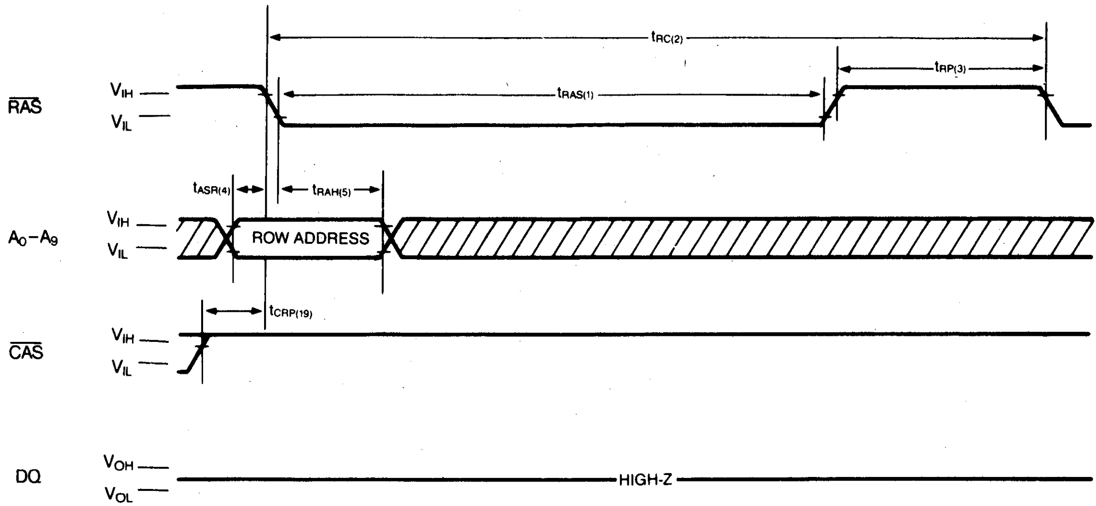
FAST PAGE MODE READ CYCLE



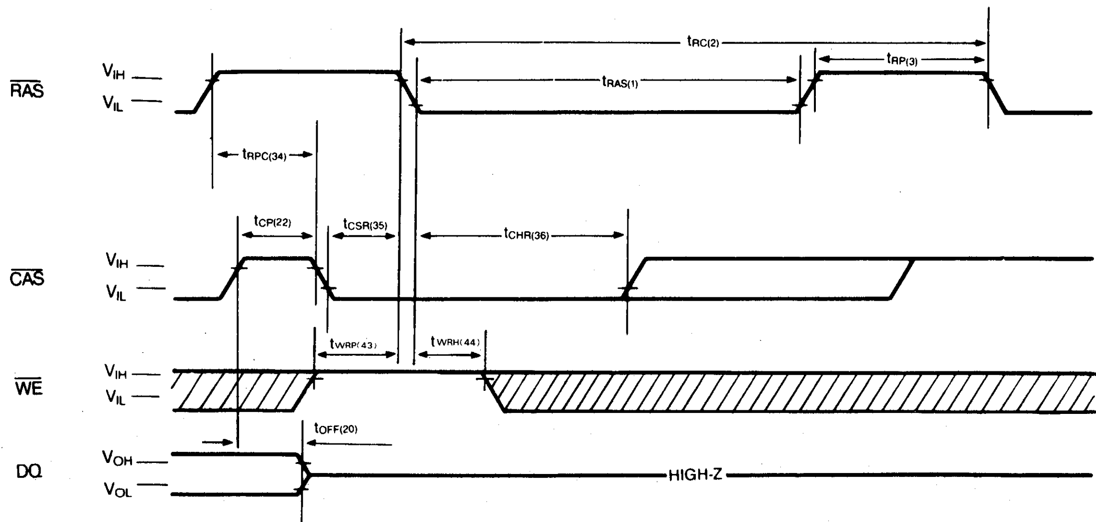
FAST PAGE MODE EARLY WRITE CYCLE



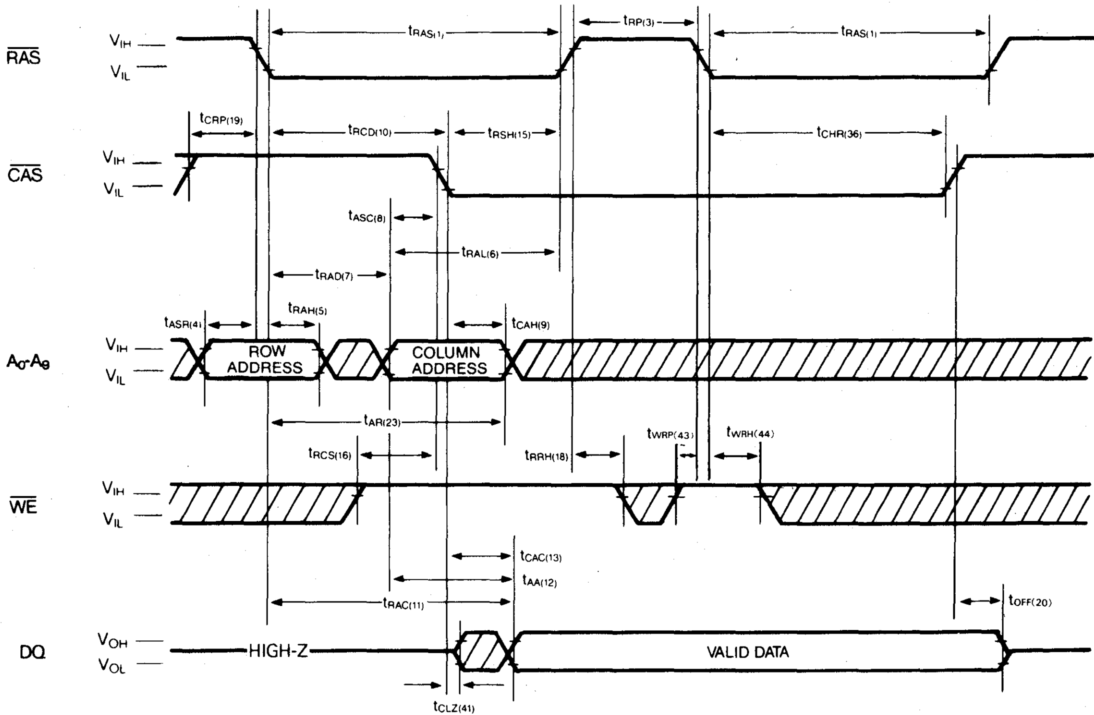
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE



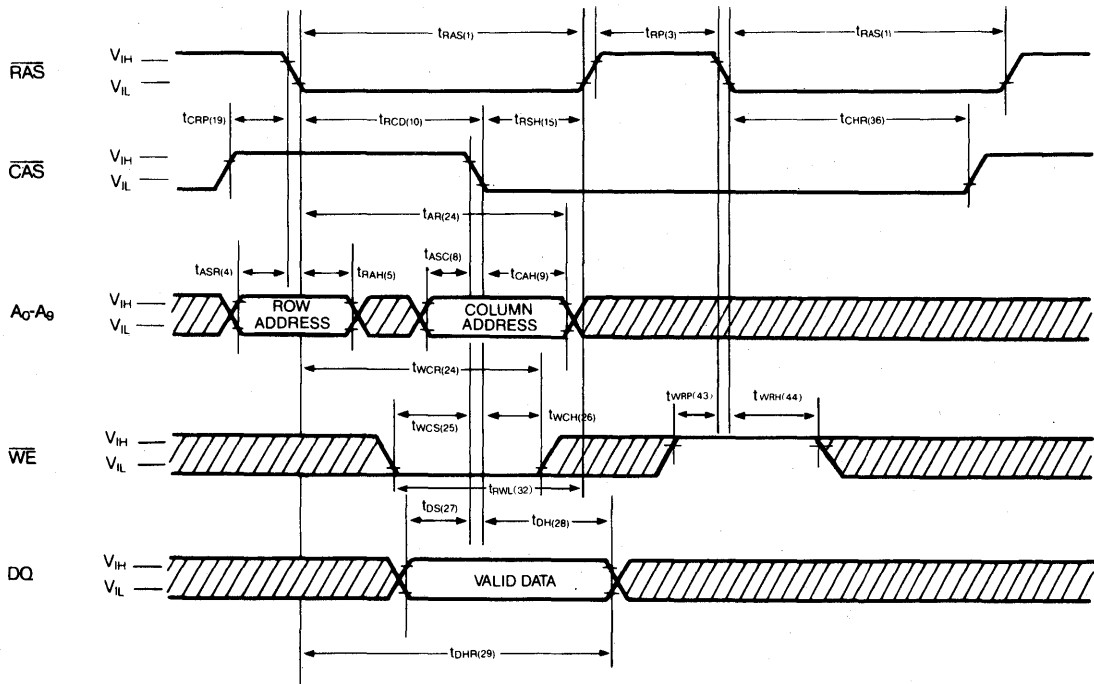
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE



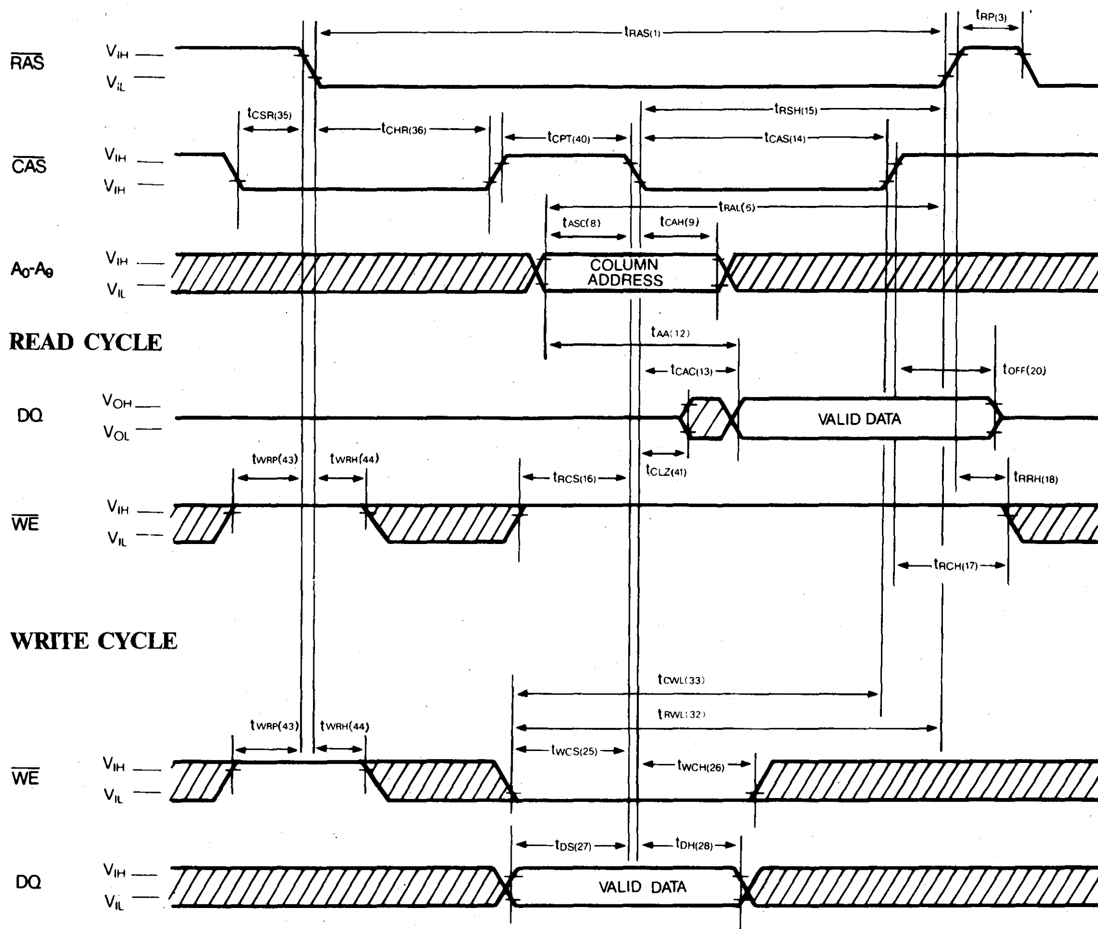
HIDDEN REFRESH CYCLE(READ)



HIDDEN REFRESH CYCLE(WRITE)

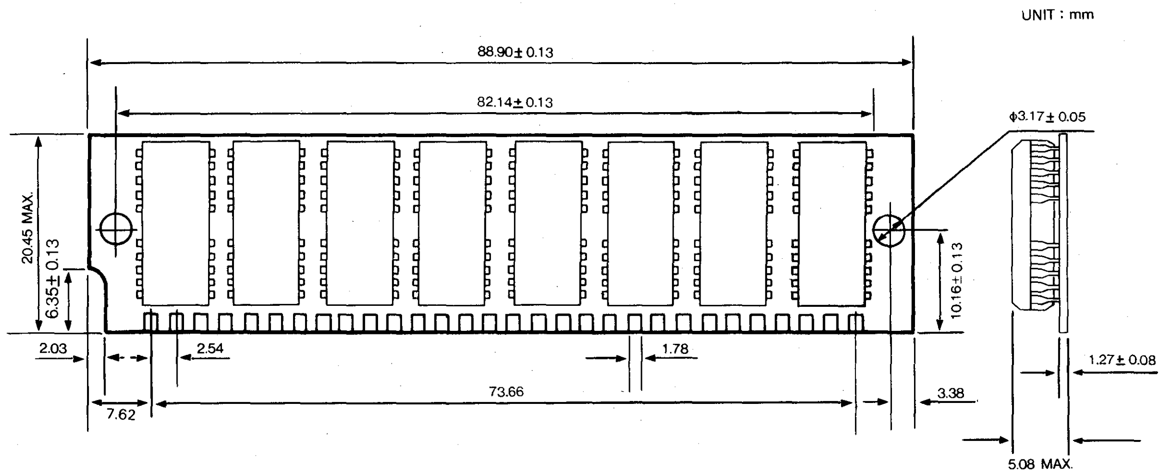


$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

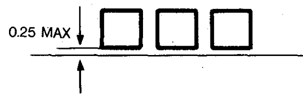


PACKAGE INFORMATION

HYM584000AM



* DETAIL OF CONTACTS



MEMO

HYUNDAI SEMICONDUCTOR

HYM584000AL

4M×8-Bit CMOS DRAM MODULE

M4G1200A-MAR92

DESCRIPTION

The HYM584000ALM is a 4M words by 8 bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of eight HY514100ALJ in 20/26 pin SOJ mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM584000ALM is a socket type single-in line module suitable for easy interchange and addition of 4M bytes memory.

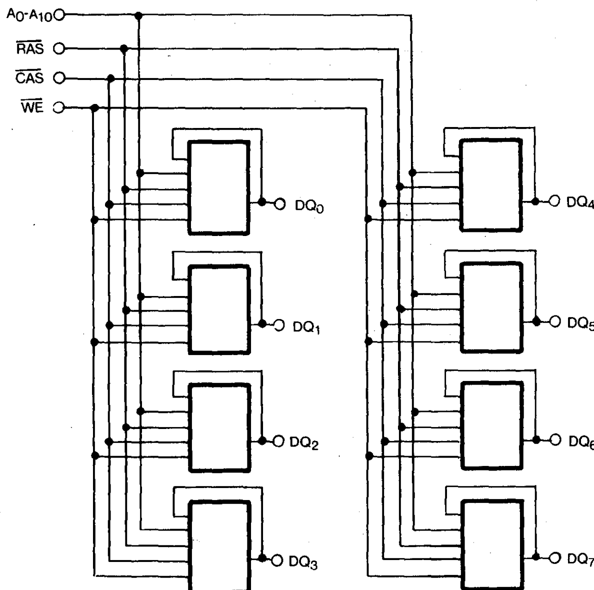
FEATURES

- Fast Page Mode operation
- Fast Access Time

	t_{RAC}	t_{CAC}	t_{PC}
HYM584000ALM-60	60	20	40
HYM584000ALM-70	70	20	45
HYM584000ALM-80	80	25	55

- Single power supply of 5V± 10%
- $\overline{CAS}$-Before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden Refresh.
- Low power operating
  4.62W max(HYM584000ALM-60)
  4.18W max(HYM584000ALM-70)
  3.74W max(HYM584000ALM-80)
- TTL compatible inputs and outputs
- 1024 refresh cycles/128ms

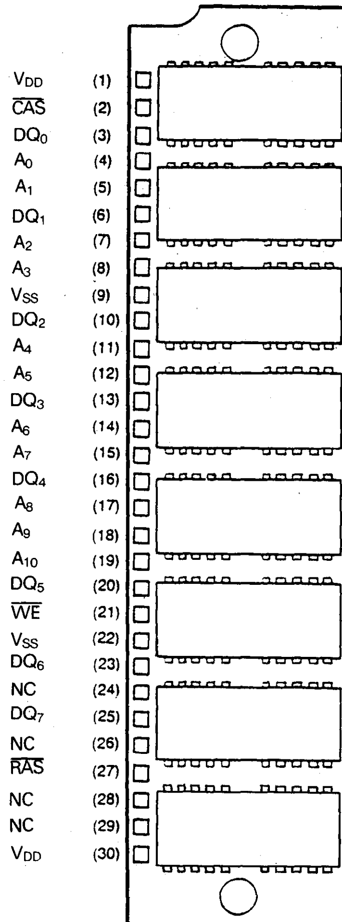
BLOCK DIAGRAM



PIN NAMES

A_0-A_{10}	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS



NOTES :
1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ_0-DQ_7).
2. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ_0-DQ_7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	5.88	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{ss}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM584000ALM		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		–	80	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60	–	840	mA	1
			−70	–	760		
			−80	–	680		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs$\geq V_{SS}$		–	16	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60	–	840	mA	
			−70	–	760		
			−80	–	680		
I_{DD4}	V_{DD} Supply Current, Fast page mode	Minimum Cycle	−60	–	520	mA	
			−70	–	440		
			−80	–	360		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs$\geq V_{SS}$		–	1.6	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60	–	840	mA	
			−70	–	760		
			−80	–	680		
I_{DD7}	V_{DD} Supply Current, Battery Back up	$\overline{CAS}$=CBR cycling or 0.2V, $\overline{WE}=V_{DD}-0.2V$, Add=$V_{DD}-0.2V$ or 0.2V I/O=$V_{DD}-0.2V$ or 0.2V or open, t_{RC}=125μs, $t_{RAS}=t_{RAS}$(min.) ~300ns		–	2.4	mA	1
		Same as above except t_{RAS}=300ns~1μs		–	3.2	mA	1, 5
V_{OL}	Output Low Voltage	I_{OL}=4.5mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1, 2, 3

#	SYMBOL	PARAMETER	HYM584000ALM						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
3	t_{RP}	$\overline{RAS}$ Prechange Time	50	–	50	–	60	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	55	ns	8
11	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	4,8,9
12	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	4,9
13	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	4,8
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
20	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
24	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
27	t_{DS}	Data In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data In Hold Time	15	–	15	–	15	–	ns	7

#	SYMBOL	PARAMETER	HYM584000AL						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
30	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	–	35	–	40	–	50	ns	4
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	40	–	45	–	55	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	128	–	128	–	128	ms	
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	65	200K	75	200K	85	200K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	30	–	35	–	40	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	4
42	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
43	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

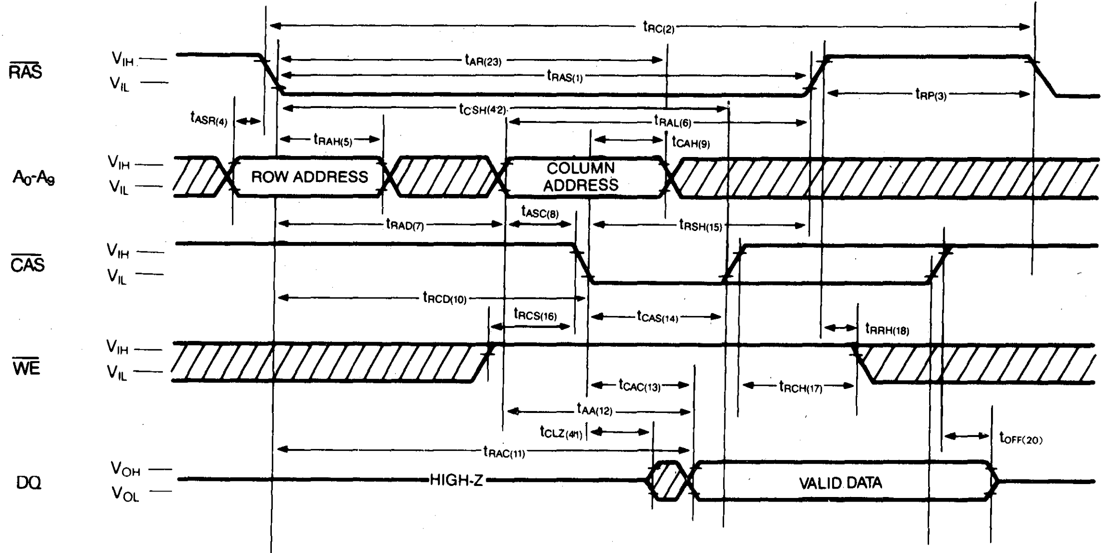
CAPACITANCE

(T_A=25°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted.)

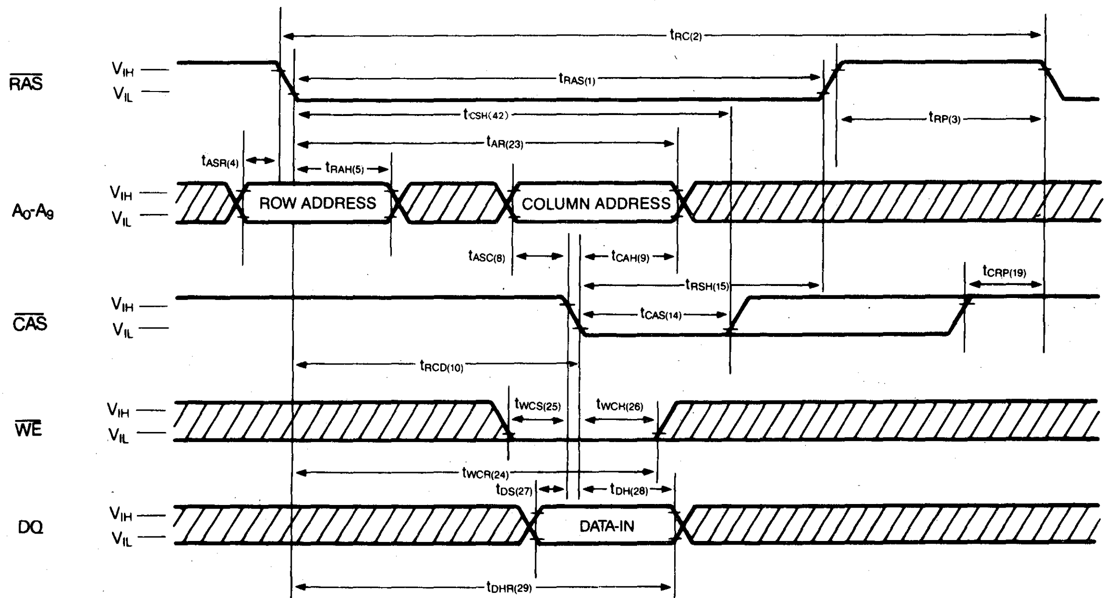
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance(A_0-A_{10}, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	55	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF

TIMING DIAGRAM

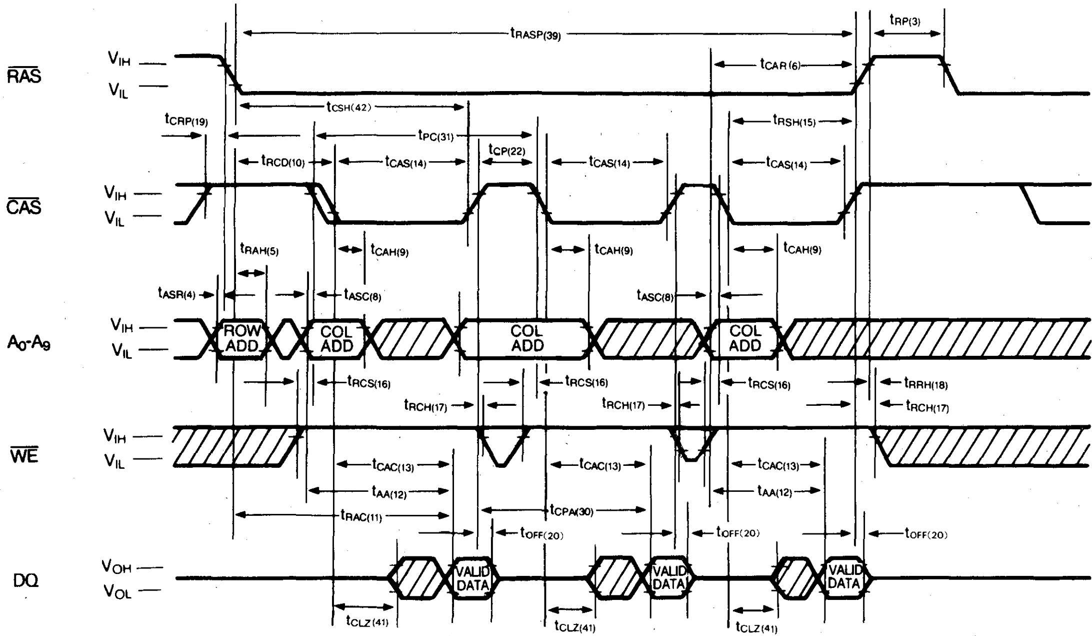
READ CYCLE



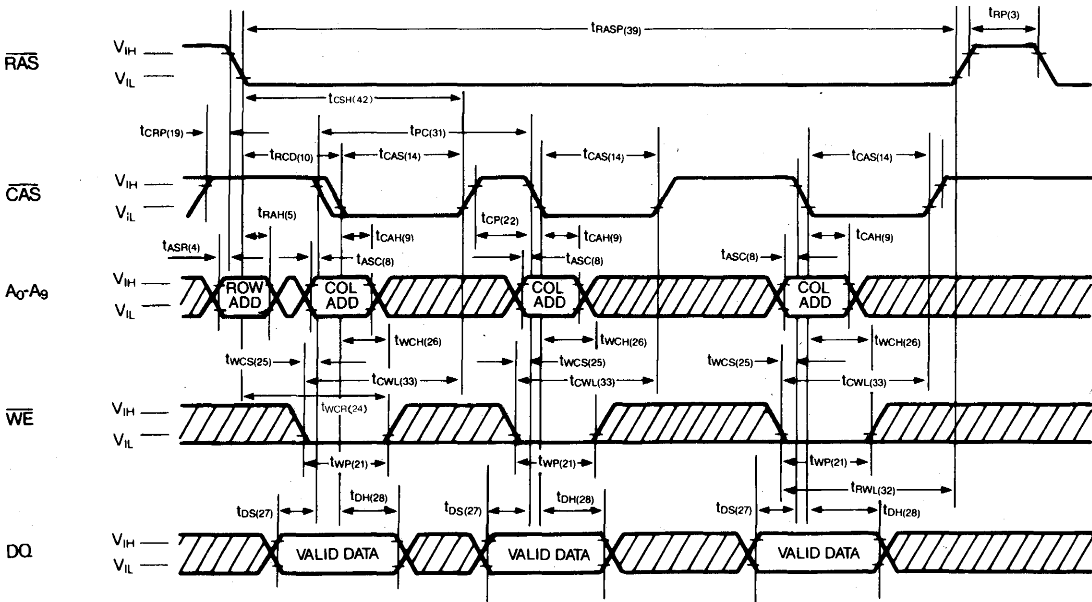
EARLY WRITE CYCLE



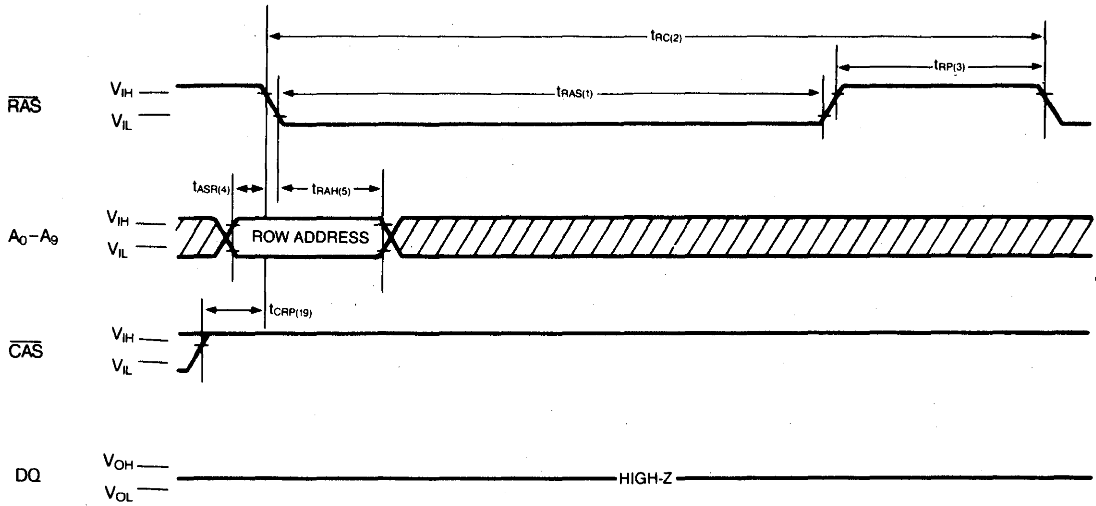
FAST PAGE MODE READ CYCLE



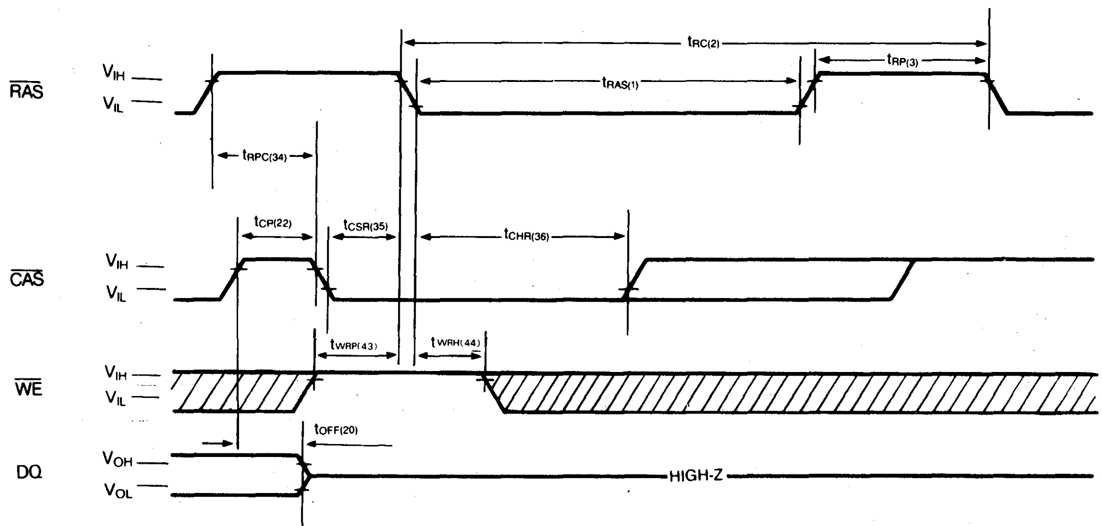
FAST PAGE MODE EARLY WRITE CYCLE



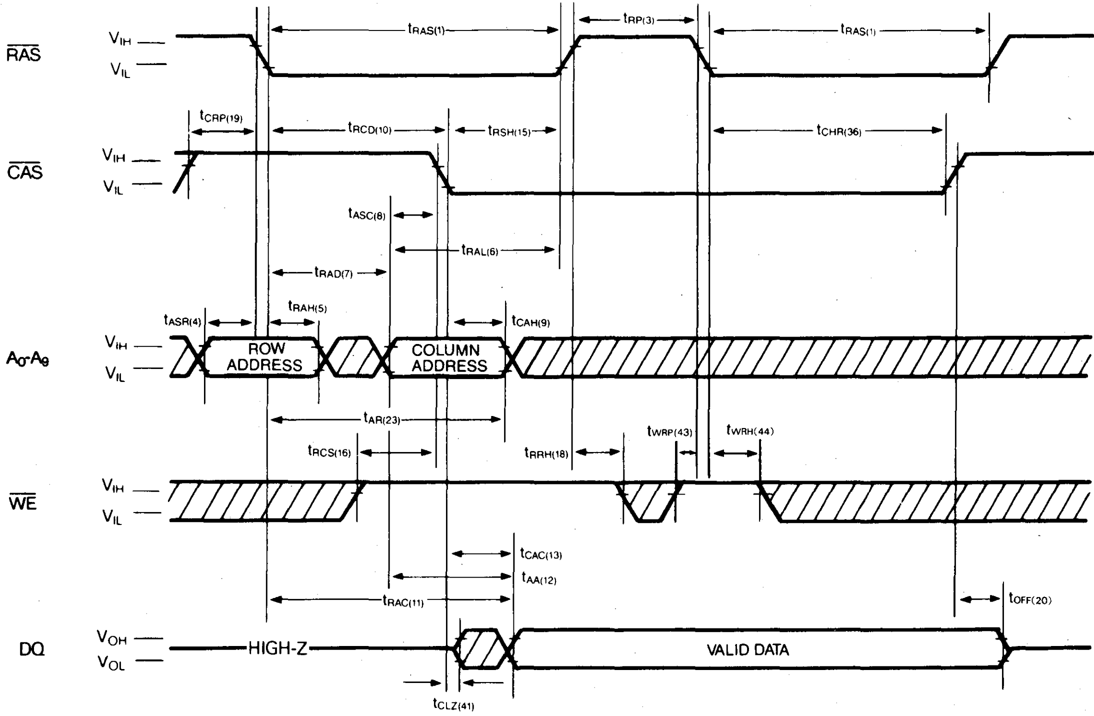
RAS-ONLY REFRESH CYCLE



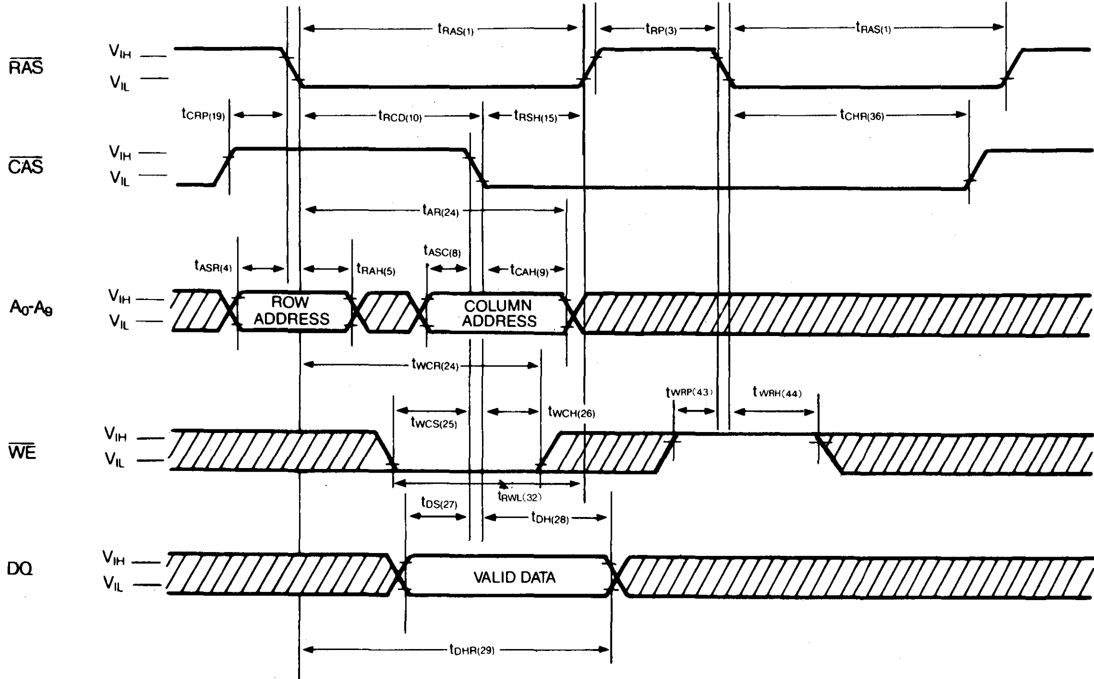
CAS-BEFORE-RAS REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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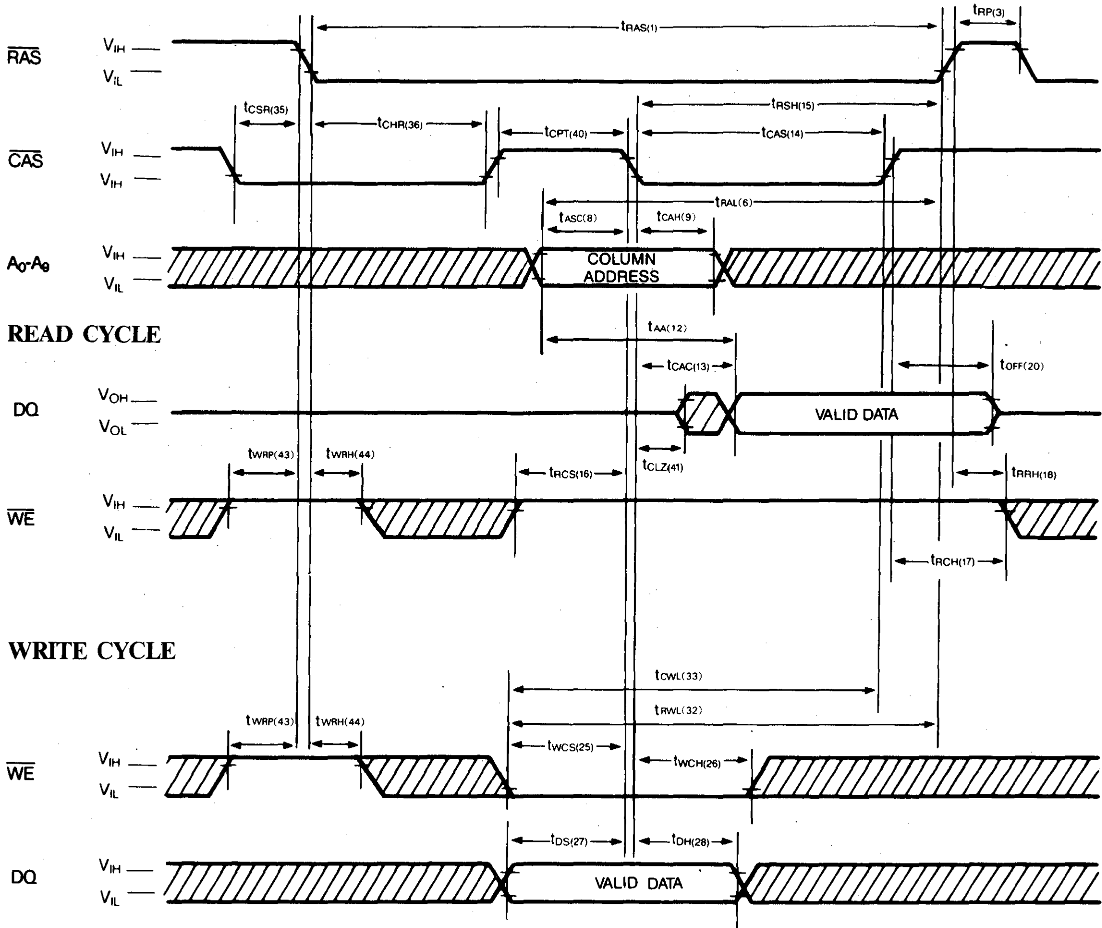
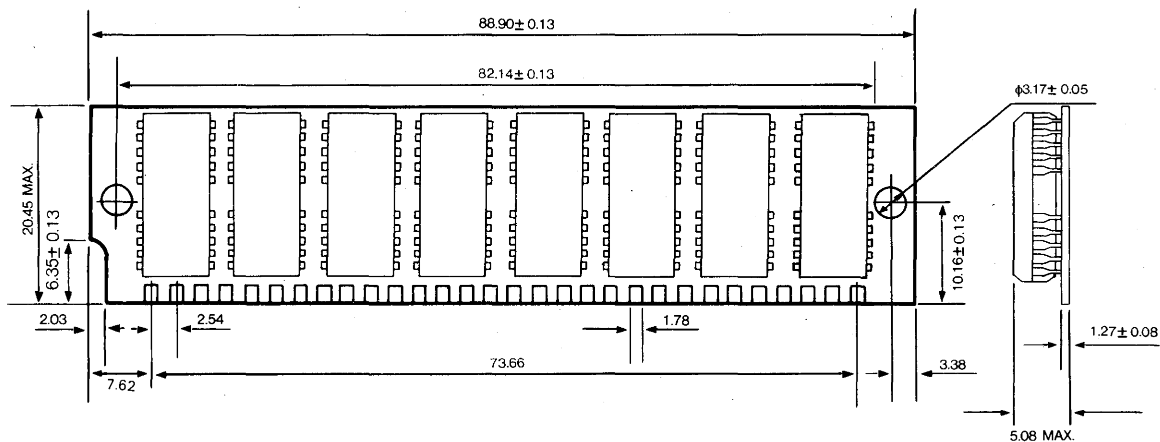
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

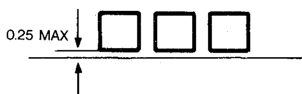


PACKAGE INFORMATION

HYM584000ALM



* DETAIL OF CONTACTS



MEMO

HYUNDAI SEMICONDUCTOR

HYM532100

1M×32-Bits CMOS DRAM MODULE

M551200A-JAN92

DESCRIPTION

The HYM532100 is a 1M words by 32 bits dynamic RAM module which mounted Fast Page mode CMOS DRAMs of eight HY514400J and 20/26 pin SOJ on a 72 pin glass-epoxy printed circuit board. Decoupling capacitors are mounted under all the DRAMs.

The HYM532100 is optimized for applications required high density and large capacity memory. The HYM532100 can be used as 2M words by 16 bits dynamic DRAM module by using of connecting $DQ_0...DQ_{15}$ to $DQ_{16}...DQ_{31}$ respectively and selecting with RAS_0 or RAS_2.

The HYM532100 is a socket type single-in-line module suitable for easy interchange and addition of 4M bytes memory.

FEATURES

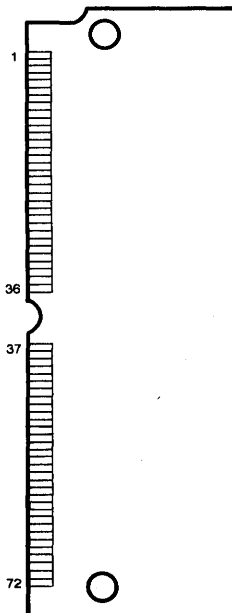
- Fast page mode operation
- Fast access Time

	t_{RAC}	t_{CAC}	t_{PC}
HYM532100M-70	70	20	50
HYM532100M-80	80	25	50
HYM532100M-10	100	25	60

- Single power supply of 5V± 10%
- $\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh.
- Low power operation
  - 4.18 W max. (HYM532100M-70)
  - 3.74 W max. (HYM532100M-80)
  - 3.30 W max. (HYM532100M-10)
- TTL compatible inputs and outputs
- 1024 refresh cycles/16ms
- High reliability gold plated contact pads

4

PIN CONNECTIONS



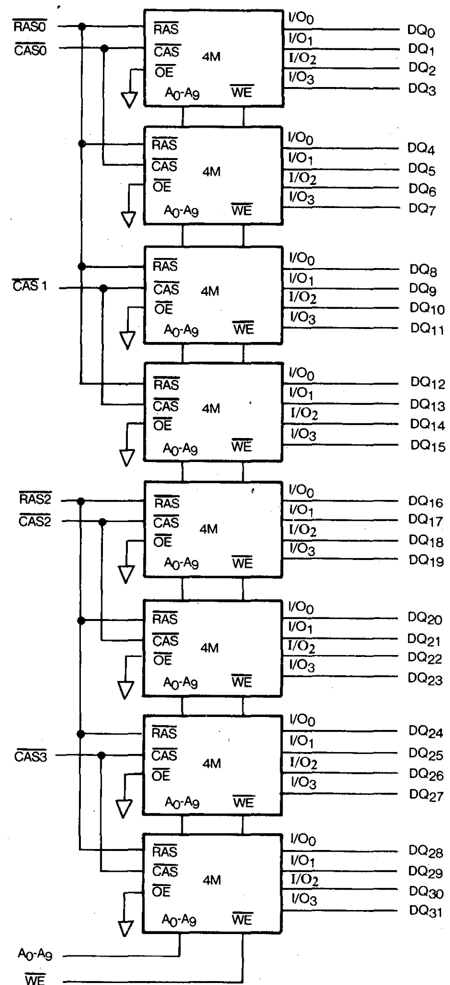
PIN NAMES

A_0-A_9	ADDRESS INPUT
DQ_0-DQ_{31}	DATA INPUT/OUTPUT
$\overline{RAS_0}$-$\overline{RAS_2}$	ROW ADDRESS STROBE
$\overline{CAS_0}$-$\overline{CAS_3}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
PD_1-PD_4	PRESENCE DETECT
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN DESCRIPTIONS

#	NAME	#	NAME
1	V_{SS}	37	NC
2	DQ_0	38	NC
3	DQ_{16}	39	V_{SS}
4	DQ_1	40	$\overline{CAS_0}$
5	DQ_{17}	41	$\overline{CAS_2}$
6	DQ_2	42	$\overline{CAS_3}$
7	DQ_{18}	43	$\overline{CAS_1}$
8	DQ_3	44	$\overline{RAS_0}$
9	DQ_{19}	45	NC
10	V_{CC}	46	NC
11	NC	47	$\overline{WE}$
12	A_0	48	NC
13	A_1	49	DQ_8
14	A_2	50	DQ_{24}
15	A_3	51	DQ_9
16	A_4	52	DQ_{25}
17	A_5	53	DQ_{10}
18	A_6	54	DQ_{26}
19	NC	55	DQ_{11}
20	DQ_4	56	DQ_{27}
21	DQ_{20}	57	DQ_{12}
22	DQ_5	58	DQ_{28}
23	DQ_{21}	59	V_{CC}
24	DQ_6	60	DQ_{29}
25	DQ_{22}	61	DQ_{13}
26	DQ_7	62	DQ_{30}
27	DQ_{23}	63	DQ_{14}
28	A_7	64	DQ_{31}
29	NC	65	DQ_{15}
30	V_{CC}	66	NC
31	A_8	67	PD_1
32	A_9	68	PD_2
33	NC	69	PD_3
34	$\overline{RAS_2}$	70	PD_4
35	NC	71	NC
36	NC	72	V_{SS}

BLOCK DIAGRAM



4M : HY514400J

PRESENCE DETECT PINS

PIN	-70	-80	-10
PD_1	V_{SS}	V_{SS}	V_{SS}
PD_2	V_{SS}	V_{SS}	V_{SS}
PD_3	V_{SS}	NC	V_{SS}
PD_4	NC	V_{SS}	V_{SS}

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	4.8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS
(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	MAX.	UNIT	NOTE
$\vert I_{LI} \vert$	Input Leakage Current(Any Input Pins)	$V_{SS} \leq V_{IN} \leq V_{DD}$		–	80	μA	
$\vert I_{LO} \vert$	Output Leakage Current for High-Impedance State	$V_{SS} \leq V_{OUT} \leq V_{DD}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−70	–	760	mA	1
			−80	–	680		
			−10	–	600		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, Other inputs$\geq V_{SS}$		–	16	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−70	–	760	mA	
			−80	–	680		
			−10	–	600		
I_{DD4}	V_{DD} Supply Current, Fast Page mode	Minimum Cycle $t_{PC}=t_{PC}$(min.)	−70	–	640	mA	1
			−80	–	560		
			−10	–	480		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS} \geq V_{DD}-0.2V$ other inputs$\geq V_{SS}$		–	8	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−70	–	760	mA	
			−80	–	680		
			−10	–	600		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTE :
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD}(max.) is measured with the output open.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1, 2, 3

#	SYMBOL	PARAMETER	HYM532100M						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	45	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	55	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
10	t_{RCD}	$\overline{RAS}$ to CAS Delay	20	50	20	55	25	75	ns	8
11	t_{RAC}	Access Time From $\overline{RAS}$	–	70	–	80	–	100	ns	4, 8, 9
12	t_{AA}	Access Time From Column Address	–	35	–	40	–	45	ns	4, 9
13	t_{CAC}	Access Time From $\overline{CAS}$	–	20	–	25	–	25	ns	4, 8
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	25	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time From $\overline{RAS}$	55	–	60	–	80	–	ns	
24	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	55	–	60	–	80	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
27	t_{DS}	Data-In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data-In Hold Time	15	–	15	–	20	–	ns	7

#	SYMBOL	PARAMETER	HYM536100M						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	55	–	60	–	80	–	ns	
30	t_{CPA}	Access Time From $\overline{CAS}$ Precharge	–	45	–	45	–	55	ns	4
31	t_{PC}	Fast Page Mode oir Wirte Cycle Time	50	–	50	–	60	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	30	–	30	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	70	200K	80	200K	100	200K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40	–	40	–	50	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	
42	t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
43	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

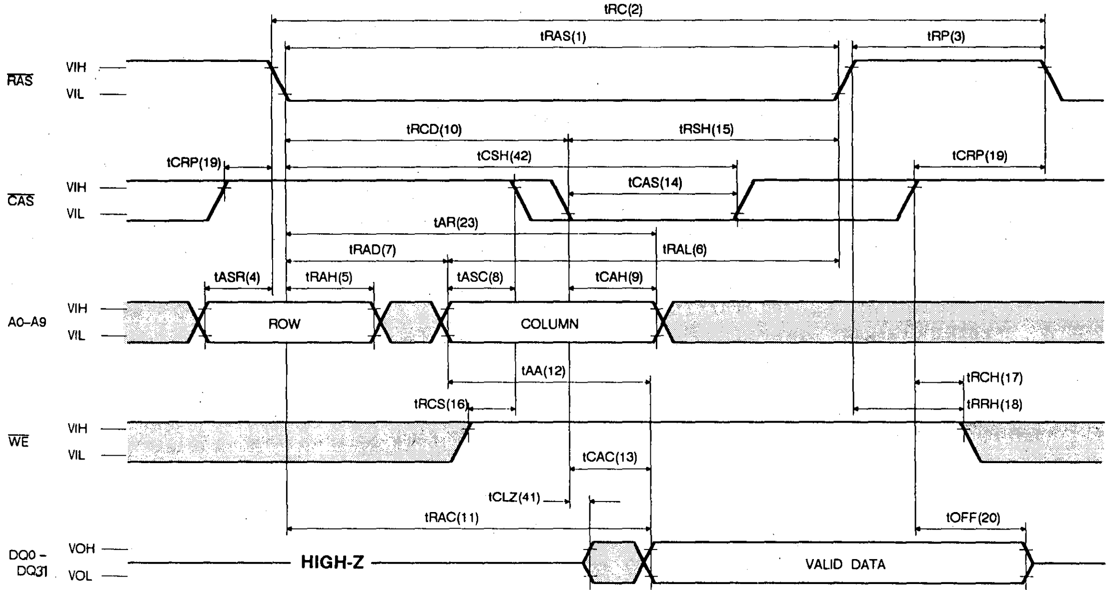
CAPACITANCE

(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

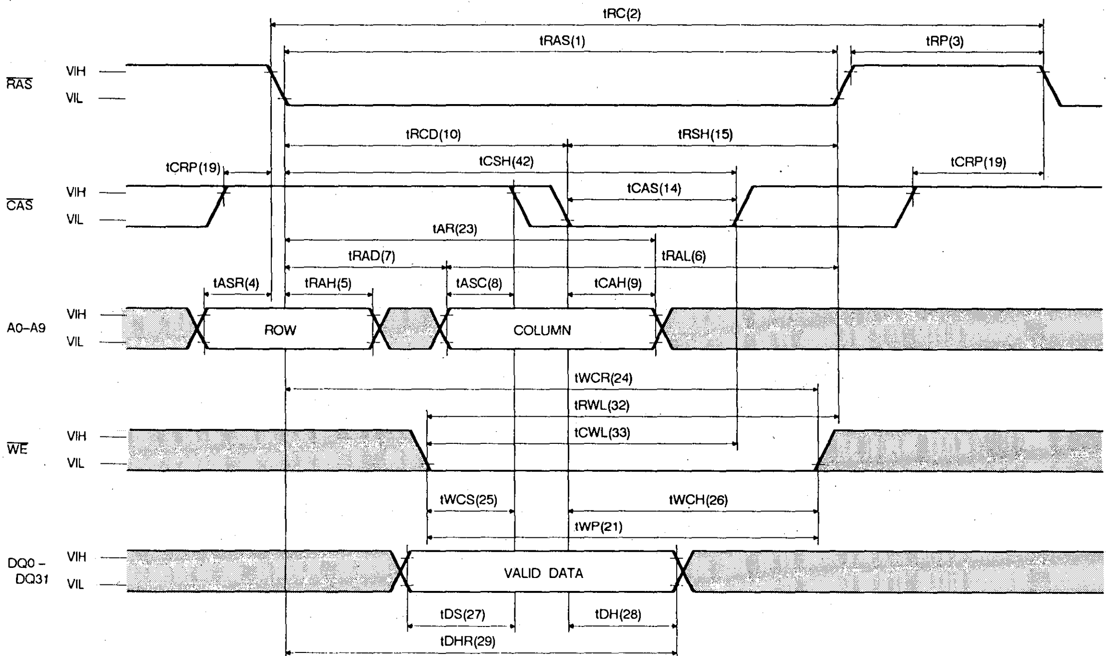
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_9)	–	68	pF
C_{IN2}	Input Capacitance($\overline{WE}$)	–	76	pF
C_{IN3}	Input Capacitance($\overline{RAS_0}$-$\overline{RAS_2}$)	–	43	pF
C_{IN4}	Input Capacitance($\overline{CAS_0}$-$\overline{CAS_3}$)	–	29	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_{31})	–	17	pF

TIMING DIAGRAM

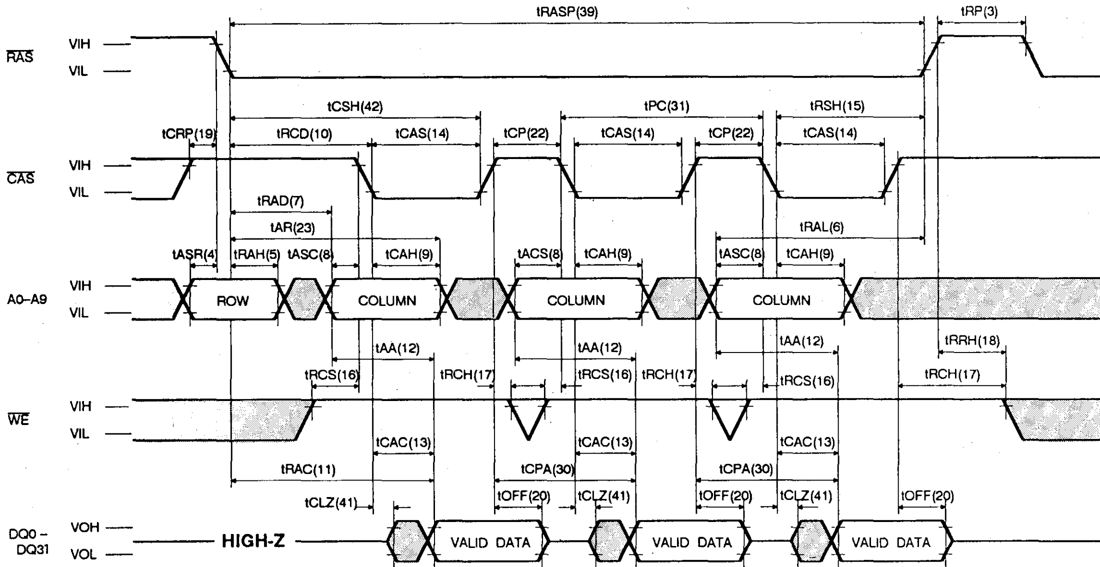
READ CYCLE



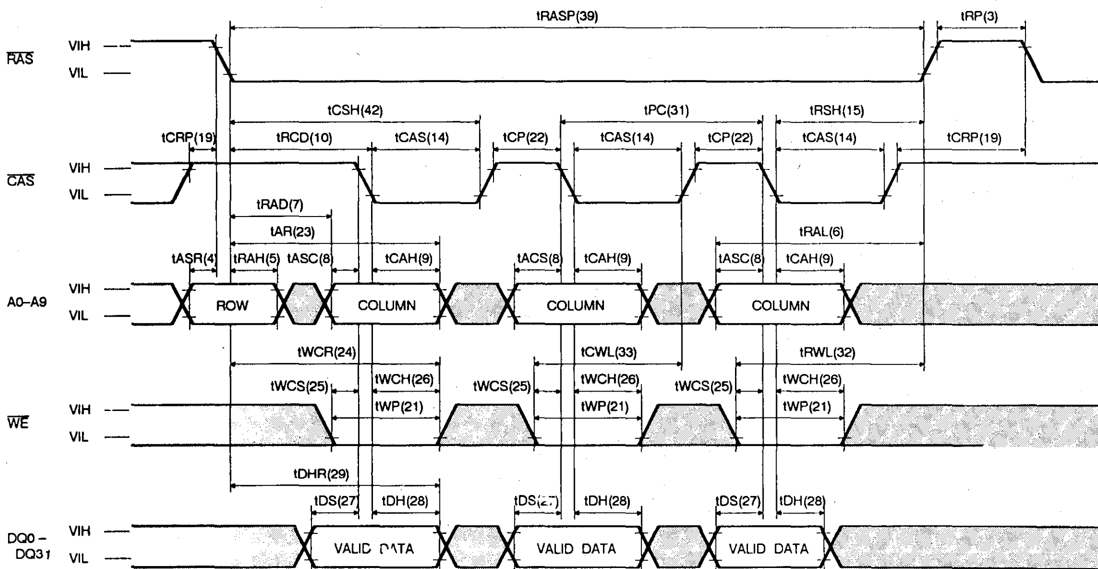
EARLY WRITE CYCLE



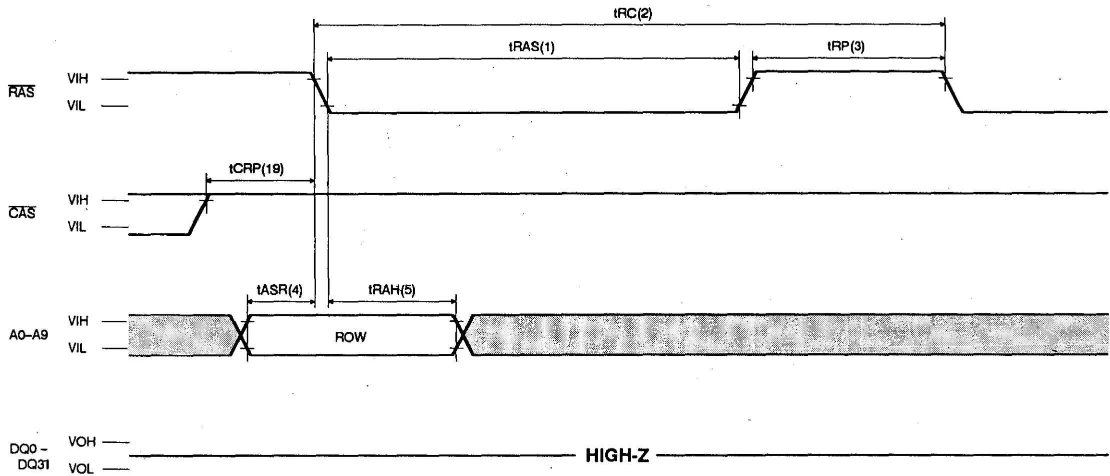
FAST PAGE MODE READ CYCLE



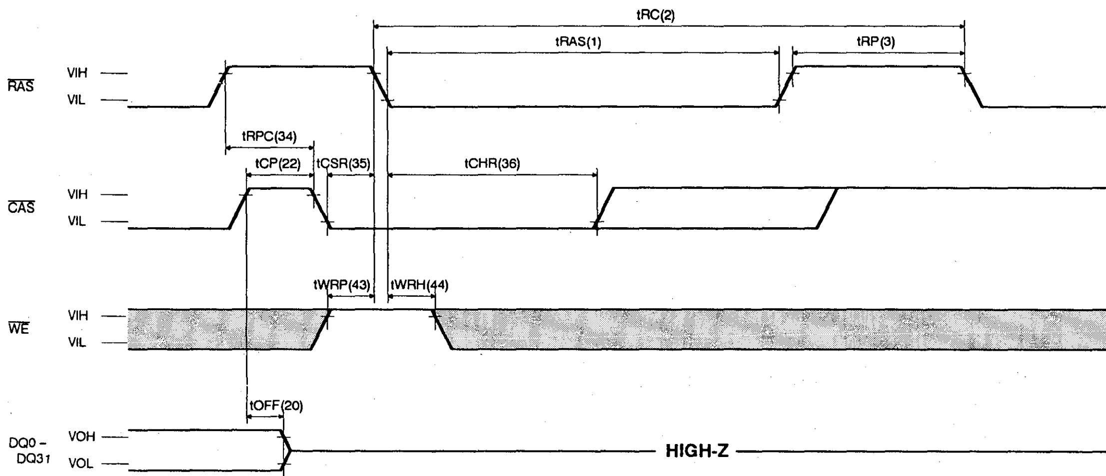
FAST PAGE MODE EARLY WRITE CYCLE



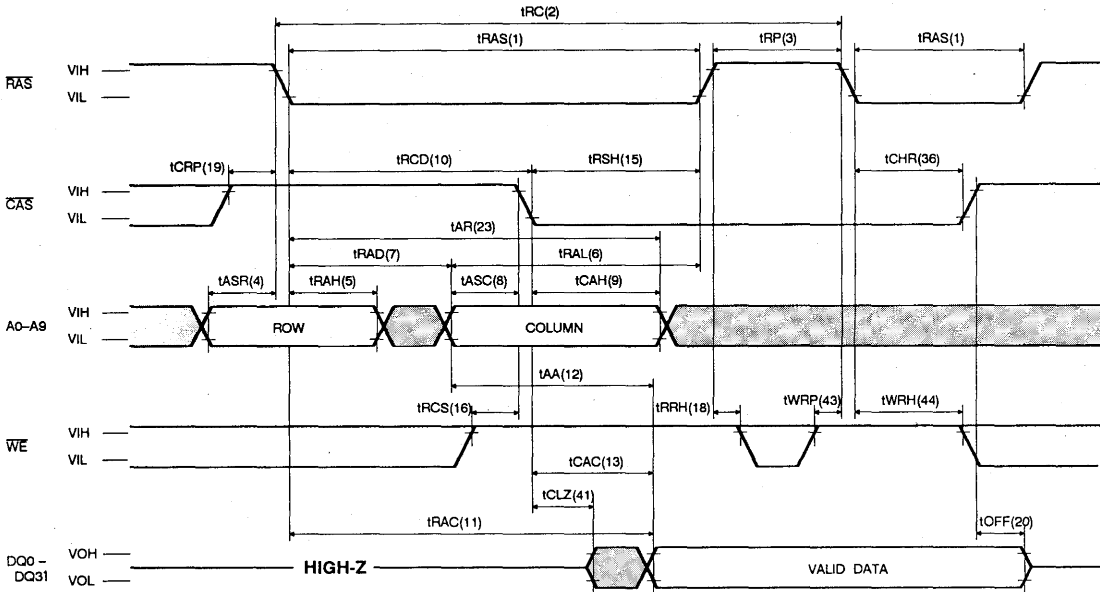
$\overline{RAS}$-ONLY REFRESH CYCLE



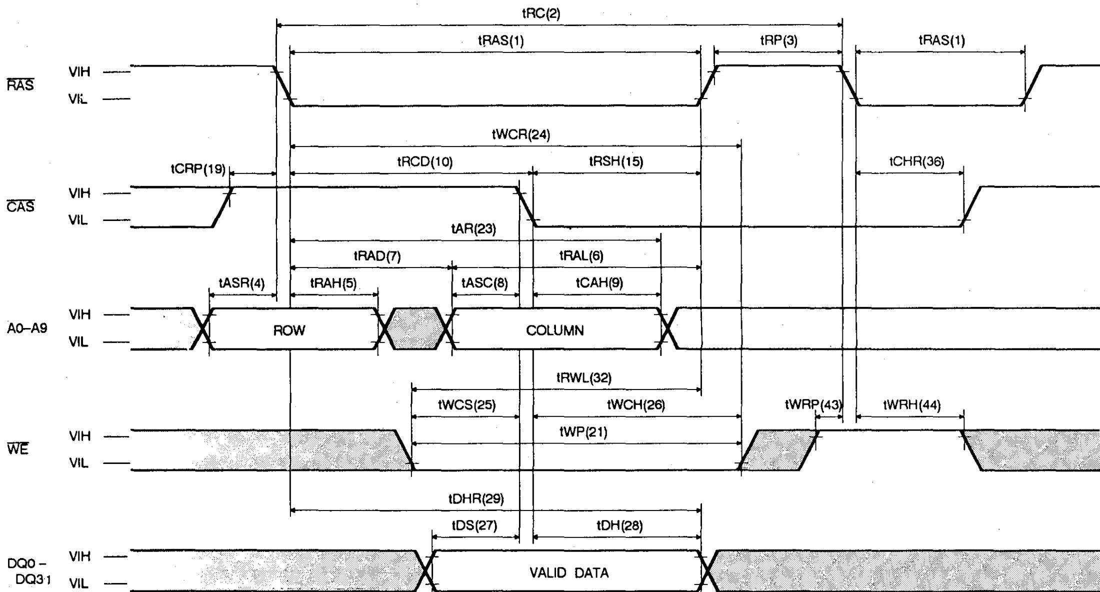
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)

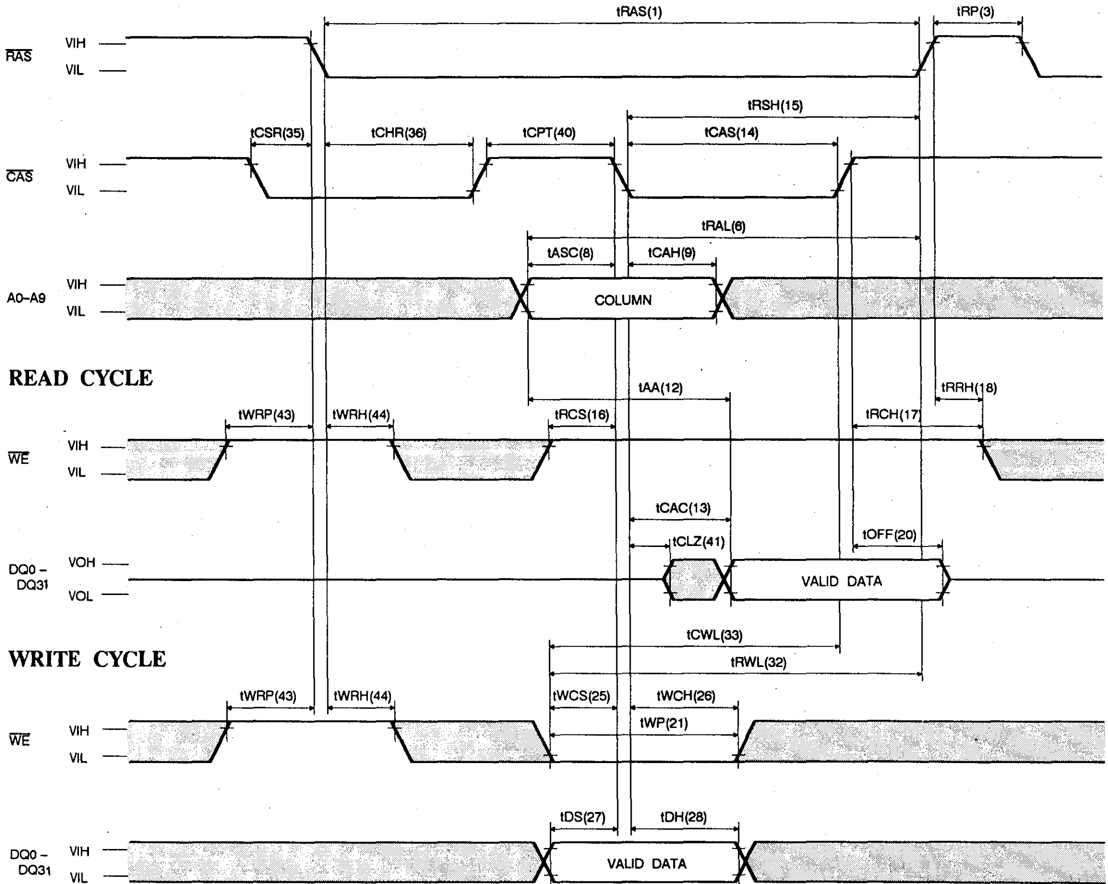


HIDDEN REFRESH CYCLE (WRITE)



4

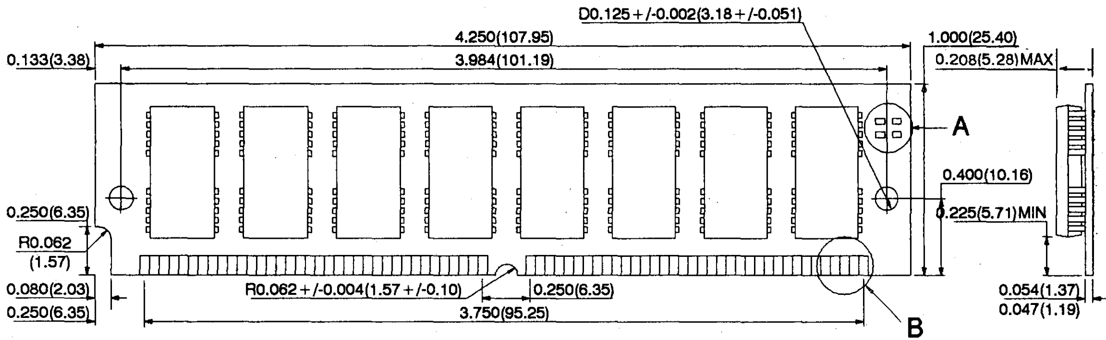
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



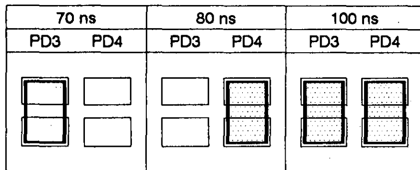
PACKAGE INFORMATION

HYM532100M

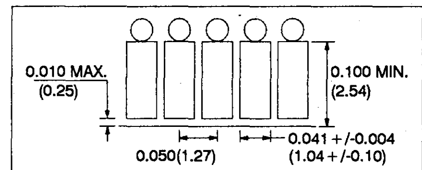
UNIT : INCH(mm)
TOLERANCE : +/-0.005(0.13)



DETAIL A



DETAIL B



MEMO

HYM594000

4M×9-Bit CMOS DRAM MODULE

M4A1202A-JAN92

DESCRIPTION

The HYM594000M is a 4M words by 9bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of nine HY514100J in 20/26 pin SOJ mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM594000M is a socket type single-in line module suitable for easy interchange and addition of 4M bytes memory with parity RAM.

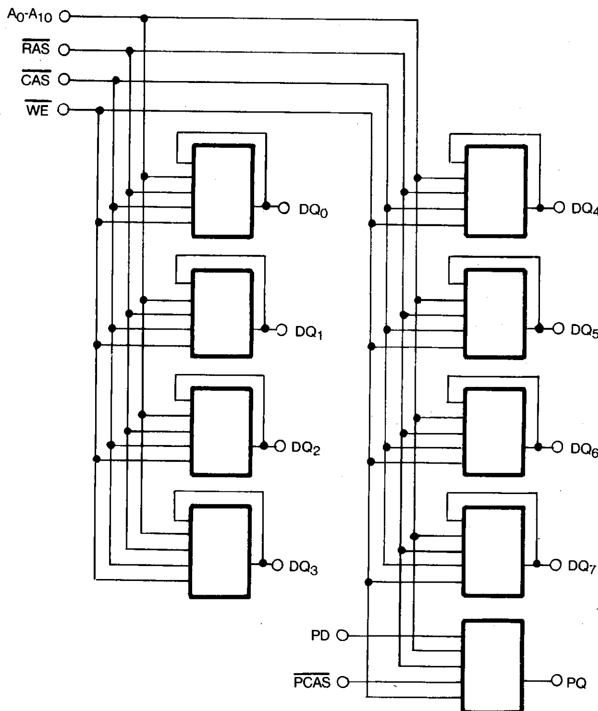
FEATURES

- Fast Page Mode operation
- Fast Access Time

	t_{RAC}	t_{CAC}	t_{PC}
HYM594000M-70	70	20	50
HYM594000M-80	80	25	55
HYM594000M-10	100	25	60

- Single power supply of 5V± 10%
- $\overline{CAS}$ Before $\overline{RAS}$, $\overline{RAS}$ only, Hidden Refresh.
- Low power operating
  4.46W max (HYM594000M-70)
  3.96W max (HYM594000M-80)
  3.47W max (HYM594000M-10)
- TTL compatible inputs and outputs
- 1024 refresh cycles/16ms

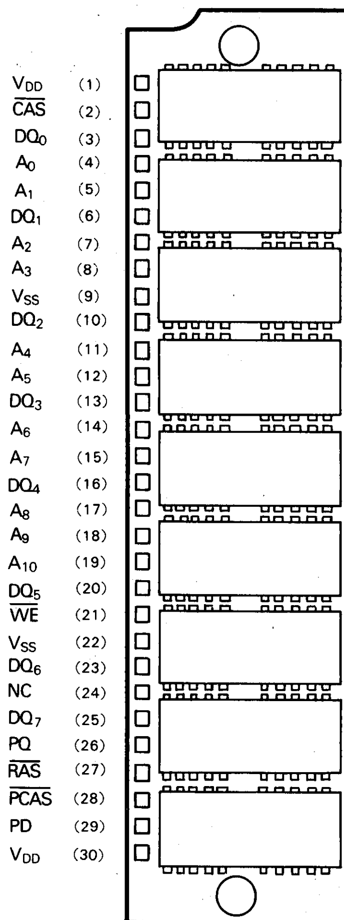
BLOCK DIAGRAM



PIN NAMES

A_0-A_{10}	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
PD	DATA IN FOR PARITY
PQ	DATA OUT FOR PARITY
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{PCAS}$	$\overline{CAS}$ FOR PARITY
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS



NOTES :

1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ0-DQ7).
2. Separate $\overline{PCAS}$ control for one separate pair of data-in (PD) and data-out (PQ) lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ0-DQ7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature(Plastic)	−55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	5.4	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM594000M		UNIT	NOTE
				MIN.	MAX.		
$\lvert I_{LI} \rvert$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		–	90	μA	
$\lvert I_{LO} \rvert$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min)	−70	–	810	mA	1
			−80	–	720		
			−10	–	630		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs $\geq V_{SS}$		–	18	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−70	–	810	mA	
			−80	–	720		
			−10	–	630		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−70	–	630	mA	1
			−80	–	540		
			−10	–	450		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs$\geq V_{SS}$		–	9	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−70	–	810	mA	
			−80	–	720		
			−10	–	630		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTES :

1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1. 2. 3

#	SYMBOL	PARAMETER	HYM594000M						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
3	t_{RP}	$\overline{RAS}$ Prechange Time	50	–	60	–	70	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	45	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	55	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	55	25	75	ns	8
11	t_{RAC}	Access Time from $\overline{RAS}$	–	70	–	80	–	100	ns	4,8,9
12	t_{AA}	Access Time from Column Address	–	35	–	40	–	45	ns	4,9
13	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	25	–	25	ns	4,8
14	t_{CAS}	$\overline{CAS}$ Pulse width	20	10K	25	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
20	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55	–	60	–	80	–	ns	
24	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55	–	60	–	80	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
27	t_{DS}	Data In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data In Hold Time	15	–	15	–	20	–	ns	7

#	SYMBOL	PARAMETER	HYM594000M						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	55	–	60	–	80	–	ns	
30	t_{CPA}	Access Time from Column Precharge	–	45	–	50	–	55	ns	4
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	50	–	55	–	60	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	30	–	30	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
39	t_{REF}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	70	200K	80	200K	100	200K	ns	
40	t_{RASP}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40	–	40	–	50	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	4
42	t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
43	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

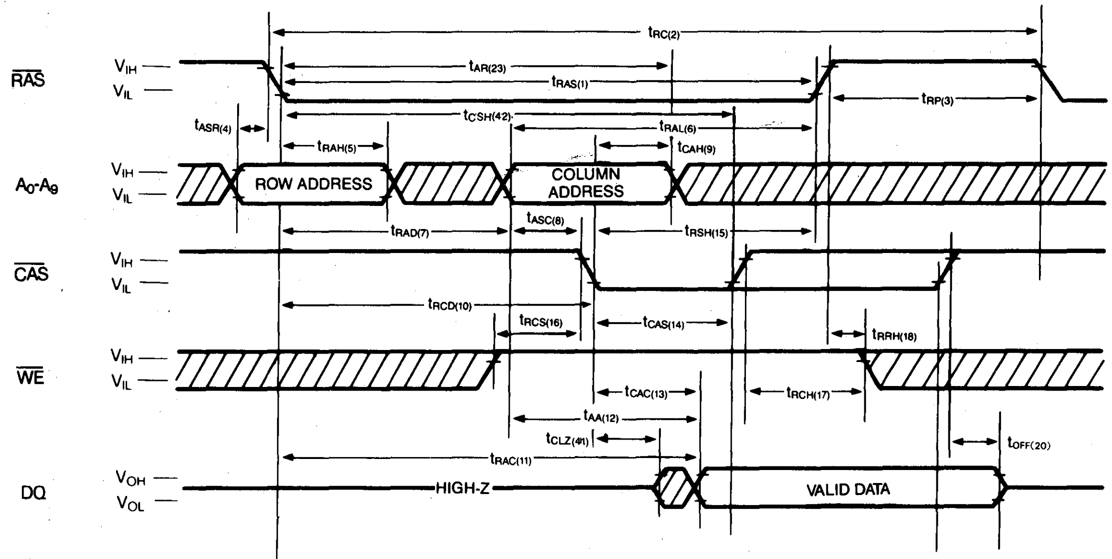
CAPACITANCE

(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

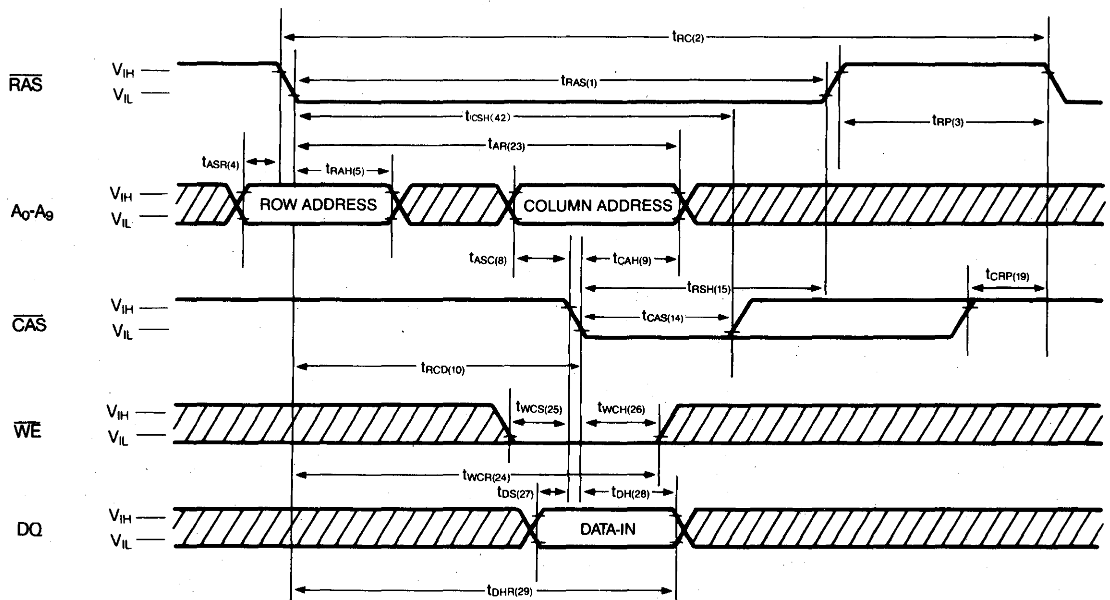
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_{10}, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{IN2}	Input Capacitance(PD, $\overline{PCAS}$)	–	10	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF
C_{PQ}	Output Capacitance(PQ)	–	10	pF

TIMING DIAGRAM

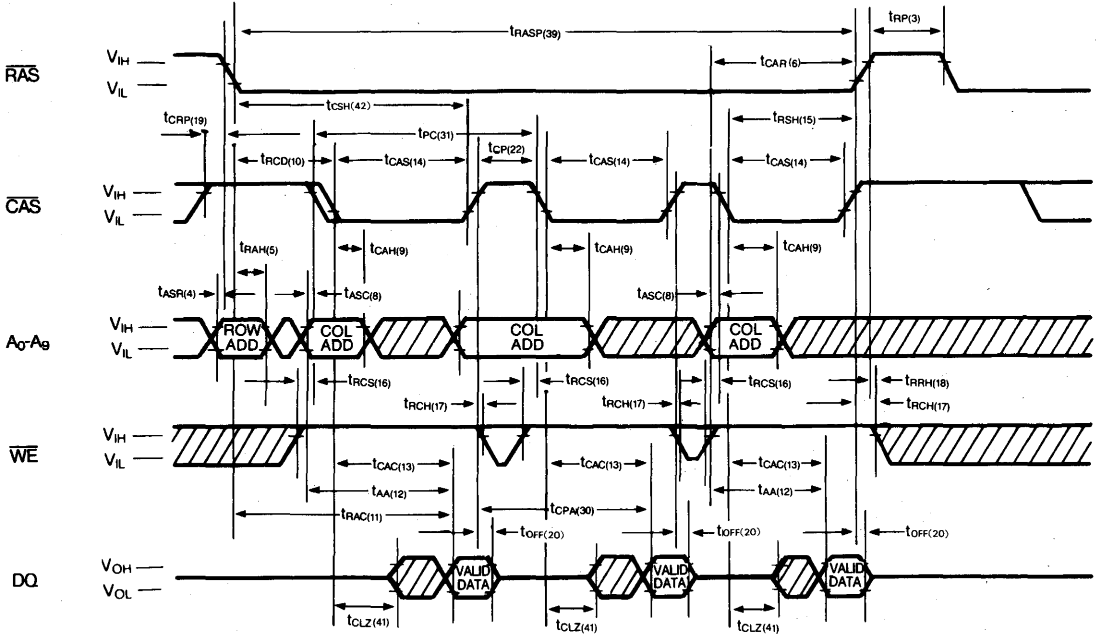
READ CYCLE



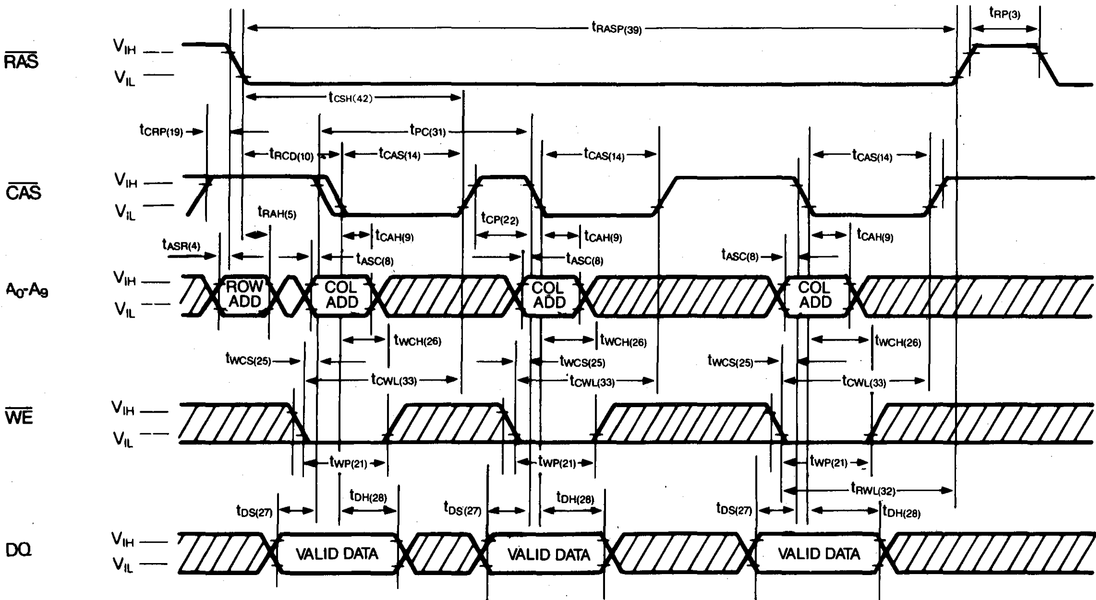
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

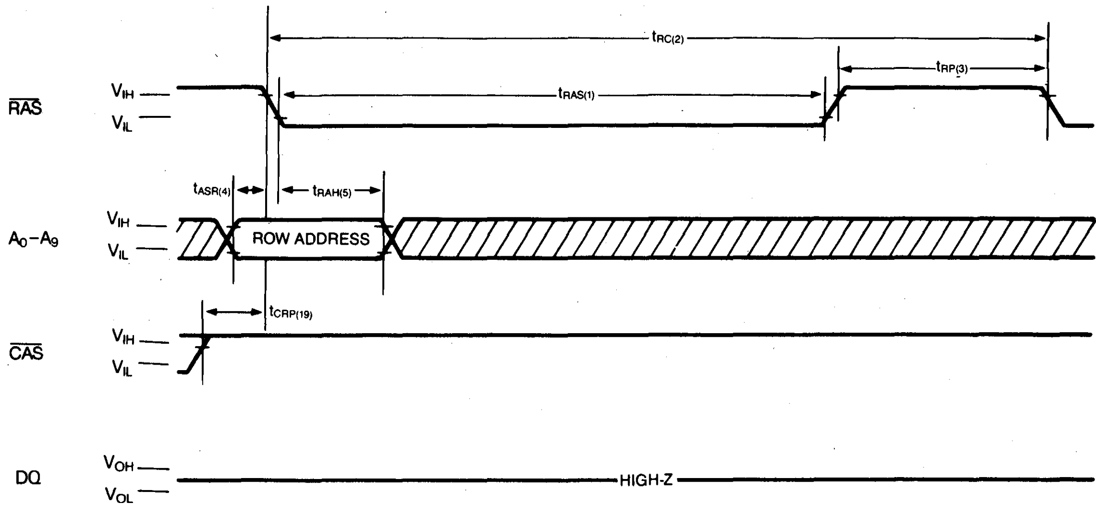


FAST PAGE MODE EARLY WRITE CYCLE

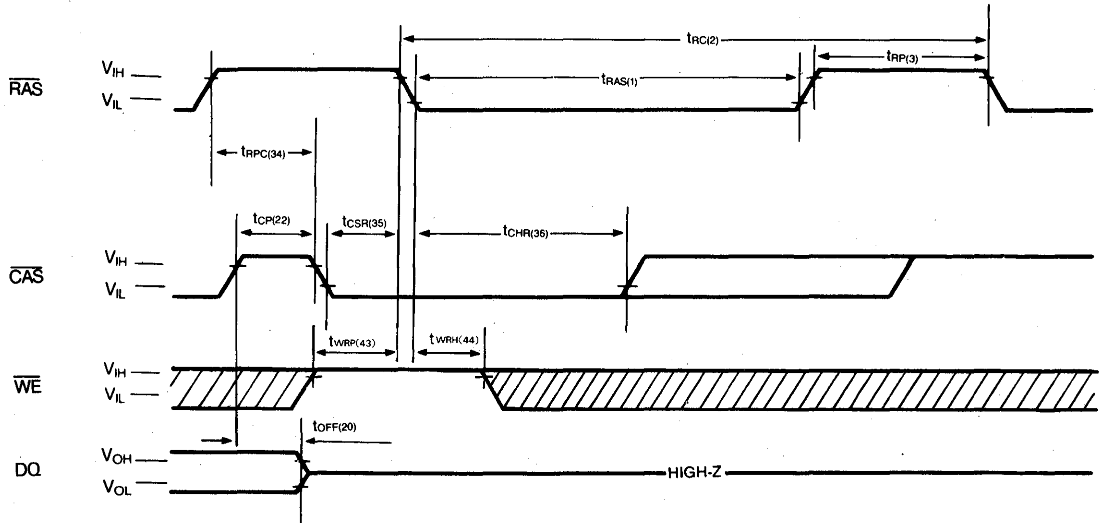


4

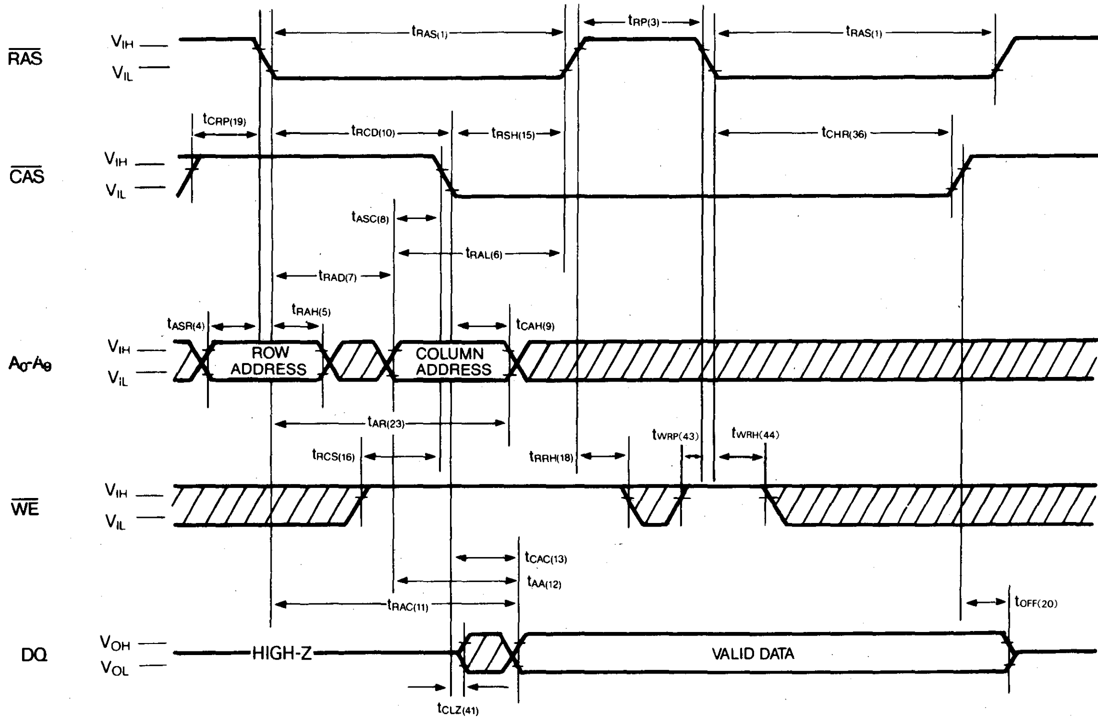
$\overline{RAS}$-ONLY REFRESH CYCLE



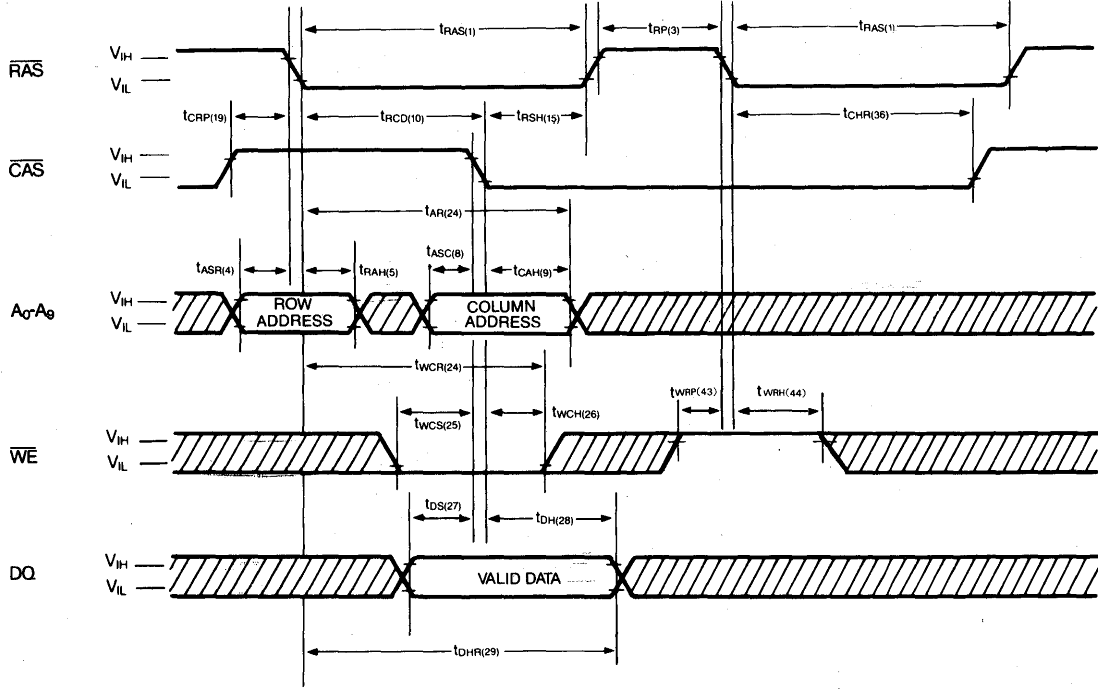
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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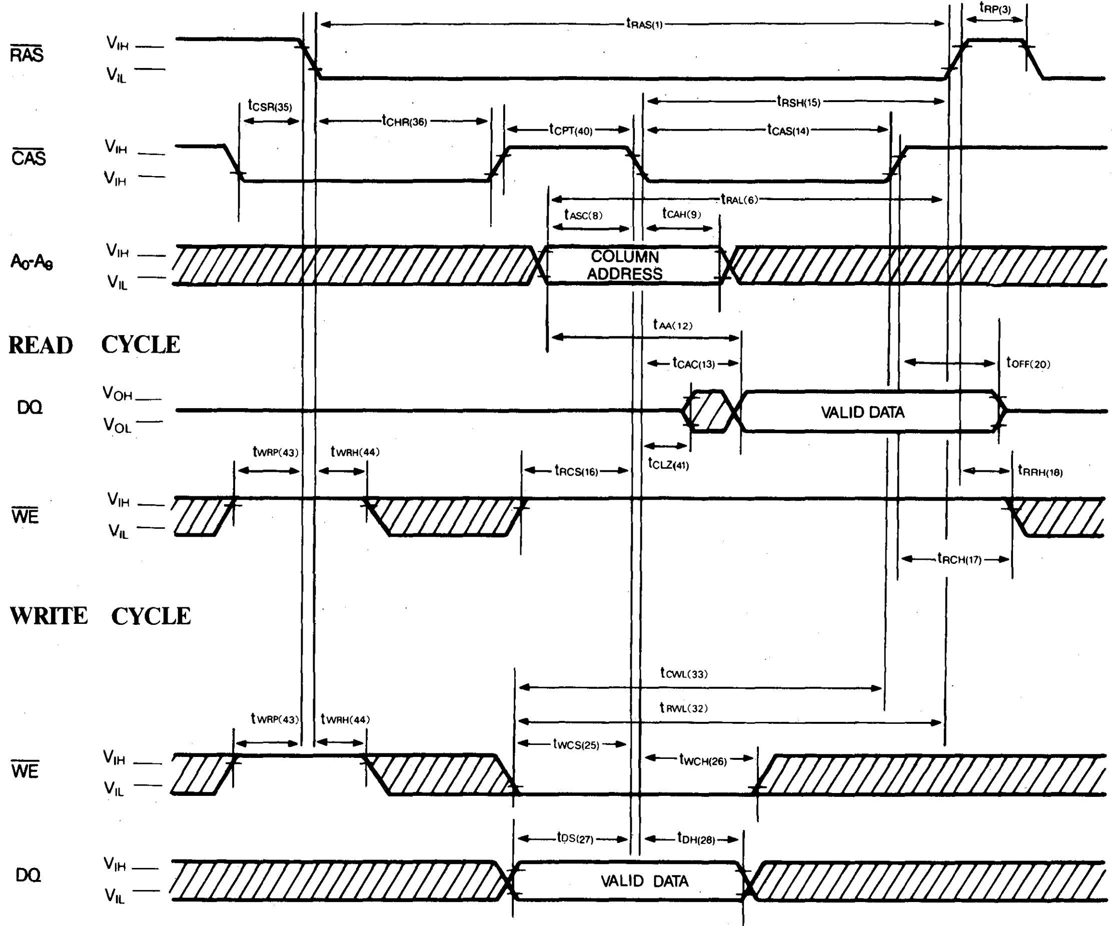
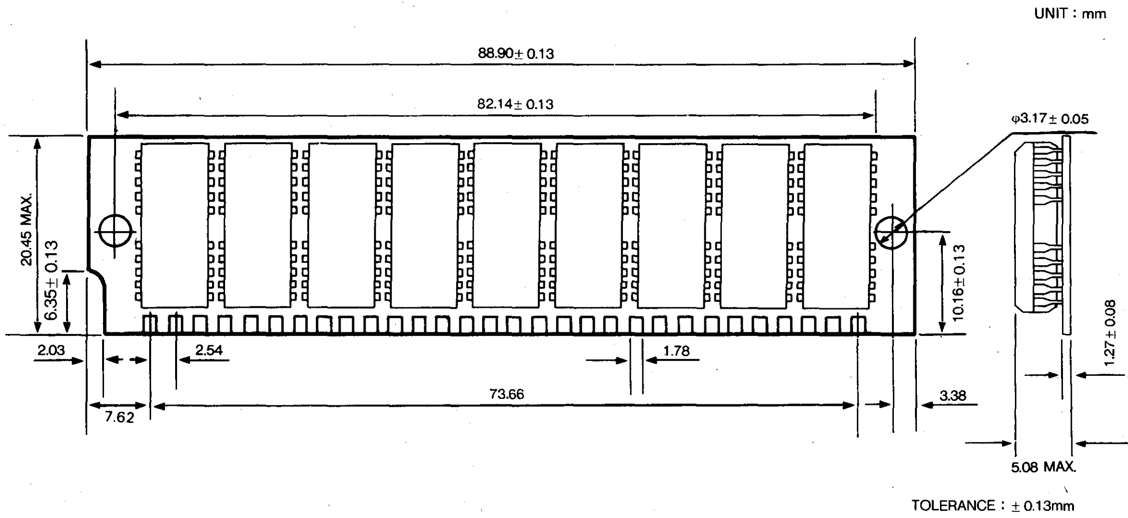
$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE

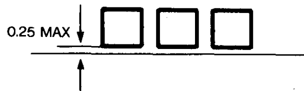


PACKAGE INFORMATION

HYM594000M



* DETAIL OF CONTACTS



MEMO

PRELIMINARY

HYUNDAI SEMICONDUCTOR

HYM594000A

4M×9-Bit CMOS DRAM MODULE

M4J1200A-MAR92

DESCRIPTION

The HYM594000AM is a 4M words by 9 bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of nine HY514100AJ in 20/26 pin SOJ mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM594000AM is a socket type single-in line module suitable for easy interchange and addition of 4M bytes memory with parity RAM.

FEATURES

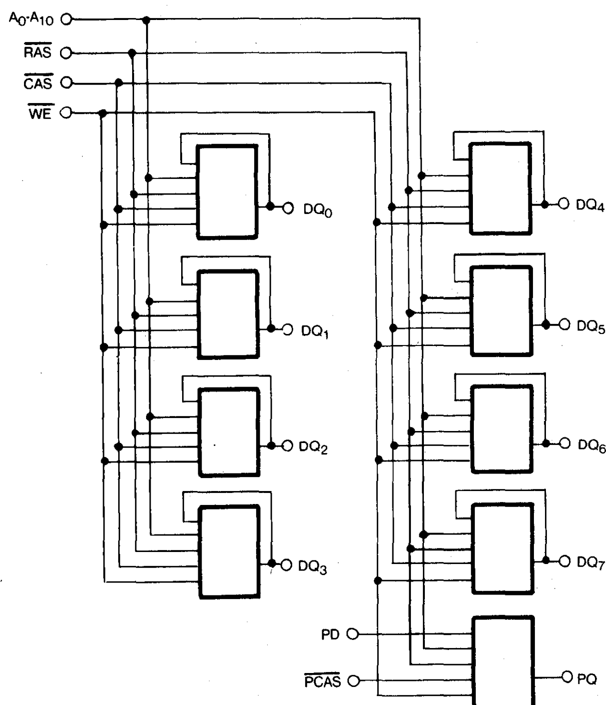
- **Fast Page Mode operation**
- **Fast Access Time**

	t_{RAC}	t_{CAC}	t_{PC}
HYM594000AM-60	60	20	40
HYM594000AM-70	70	20	45
HYM594000AM-80	80	25	55

- **Single power supply of 5V± 10%**
- **$\overline{CAS}$-Before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden Refresh.**
- **Low power operating**
  5.12W max(HYM594000AM-60)
  4.70W max(HYM594000AM-70)
  4.21W max(HYM594000AM-80)
- **TTL compatible inputs and outputs**
- **1024 refresh cycles/16ms**

4

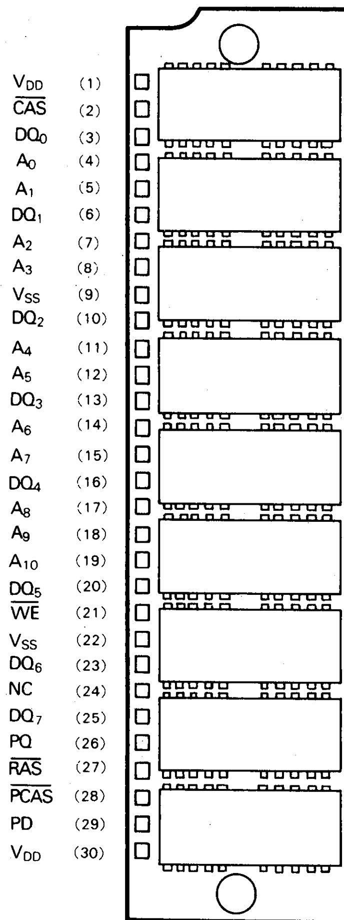
BLOCK DIAGRAM



PIN NAMES

A0-A10	ADDRESS INPUT
DQ0-DQ7	DATA INPUT/OUTPUT
PD	DATS IN FOR PARITY
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{PCAS}$	CAS FOR PARITY
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS



NOTES :

1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ0-DQ7).
2. Separate $\overline{PCAS}$ control for one separate pair of data-in (PD) and data-out (PQ) lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ0-DQ7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	C
T_{STG}	Storage Temperature(Plastic)	−55 to 150	C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	6.6	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS
(T_A=0, C to 70, C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM594000AM		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \le V_{IN} \le V_{DD}$		–	90	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min)	−60	–	945	mA	1
			−70	–	855		
			−80	–	765		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs$\ge V_{SS}$		–	18	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60	–	945	mA	
			−70	–	855		
			−80	–	765		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	−60	–	585	mA	
			−70		495		
			−80	–	405		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \ge V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs$\ge V_{SS}$		–	9	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60	–	945	mA	
			−70	–	855		
			−80	–	765		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTES :
1. I_{DD} is dependent on output loading when the device output is selected, Specified I_{DD}(max.) is measured with the output open.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1, 2, 3

#	SYMBOL	PARAMETER	HYM594000AM						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
3	t_{RP}	$\overline{RAS}$ Prechange Time	50	–	50	–	60	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	55	ns	8
11	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	4,8,9
12	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	4,9
13	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	4,8
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	20K	20	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
20	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
24	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
27	t_{DS}	Data In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data In Hold Time	15	–	15	–	15	–	ns	7

#	SYMBOL	PARAMETER	HYM594000A						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
30	t_{CPA}	Access Time from Column Precharge	–	35	–	40	–	50	ns	4
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	40	–	45	–	55	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	65	200K	75	200K	85	200K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	30	–	35	–	40	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	4
42	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
43	t_{WRP}	$\overline{WE}$ to RAS Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to RAS Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

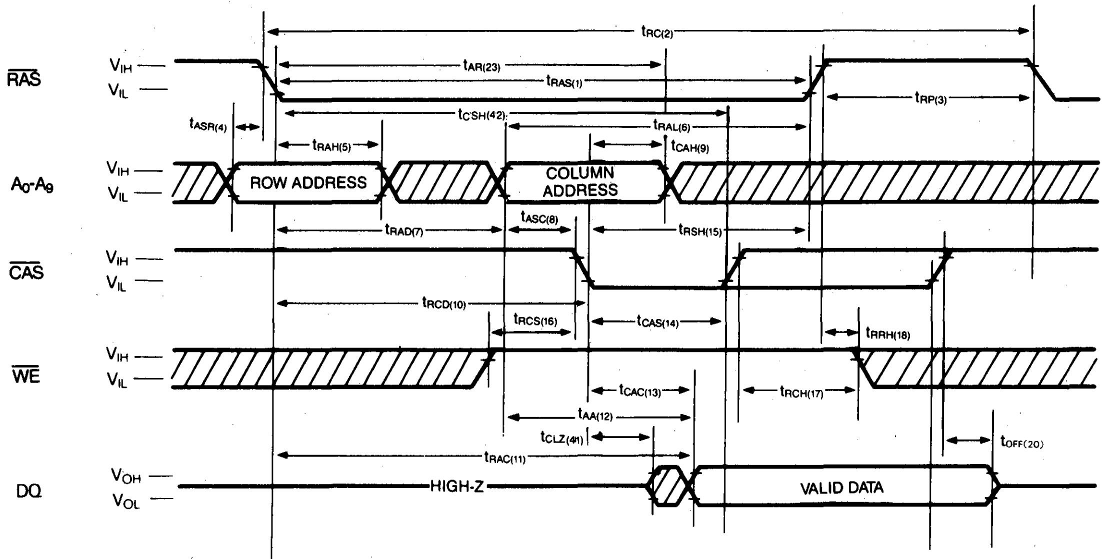
CAPACITANCE

(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

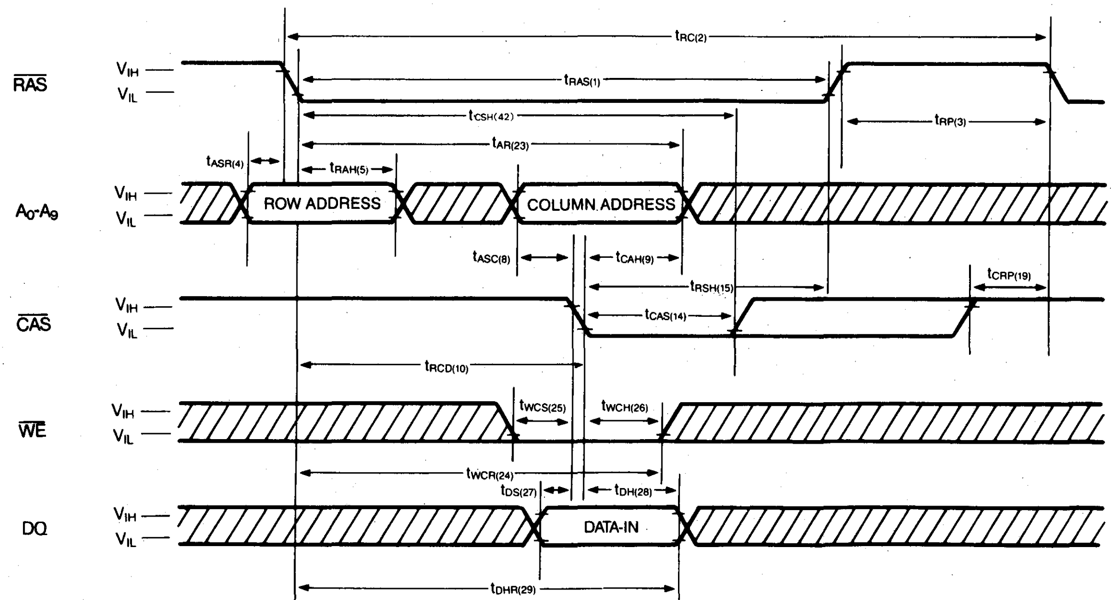
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_{10}, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	60	pF
C_{IN2}	Input Capacitance(PD, $\overline{PCAS}$)	–	10	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF
C_{PQ}	Output Capacitance(PQ)	–	10	pF

TIMING DIAGRAM

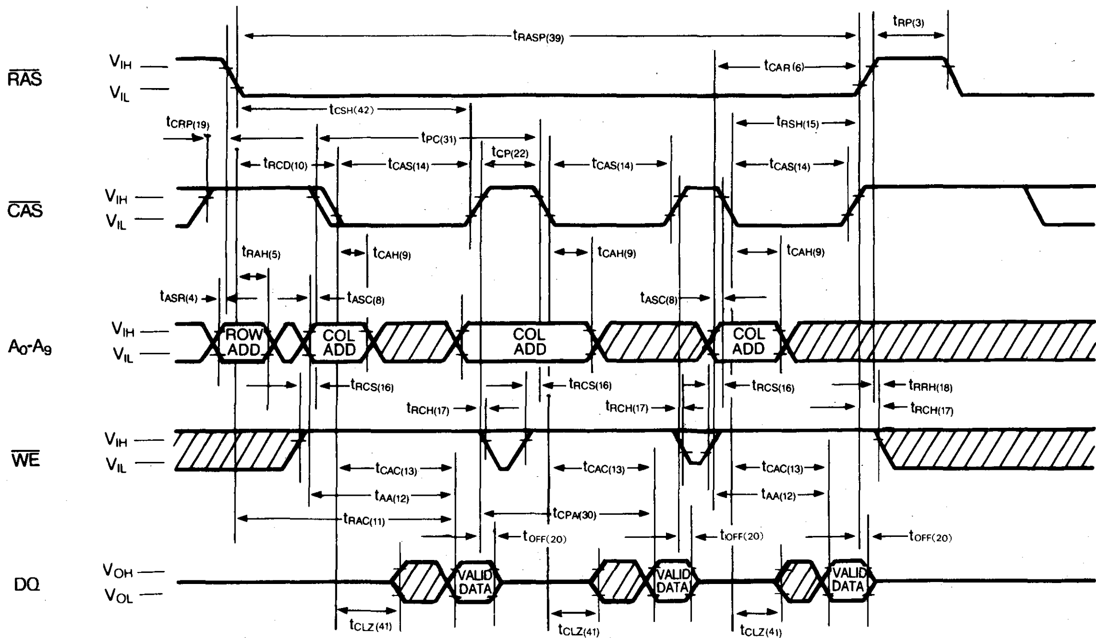
READ CYCLE



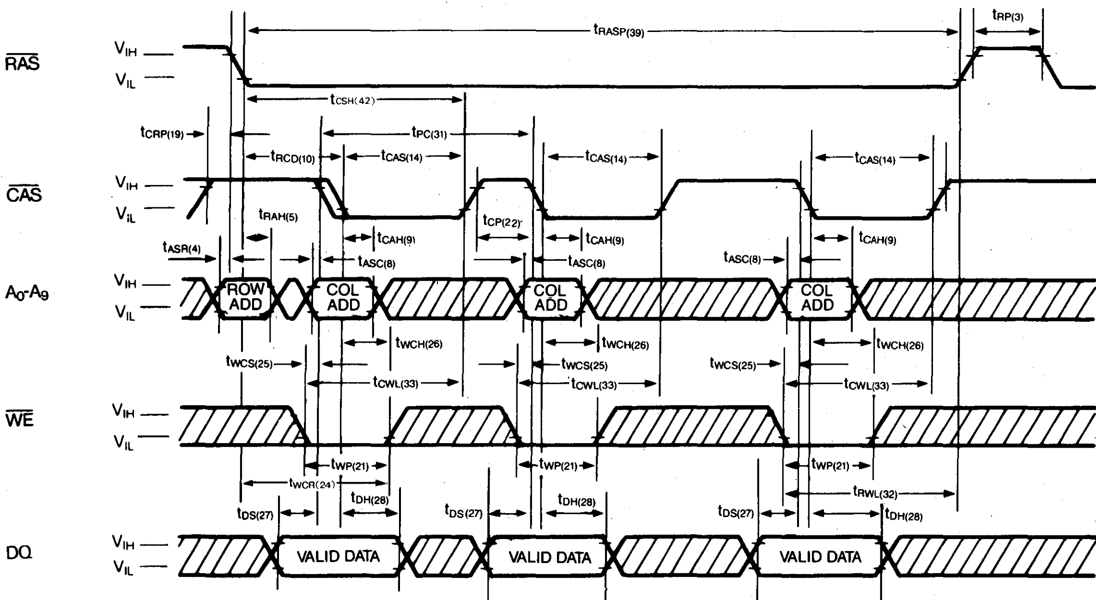
EARLY WRITE CYCLE



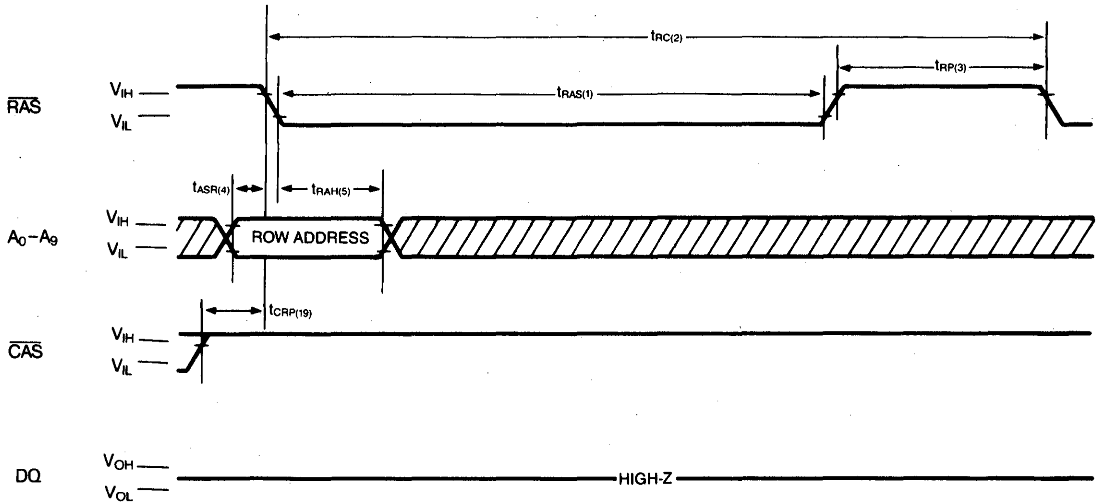
FAST PAGE MODE READ CYCLE



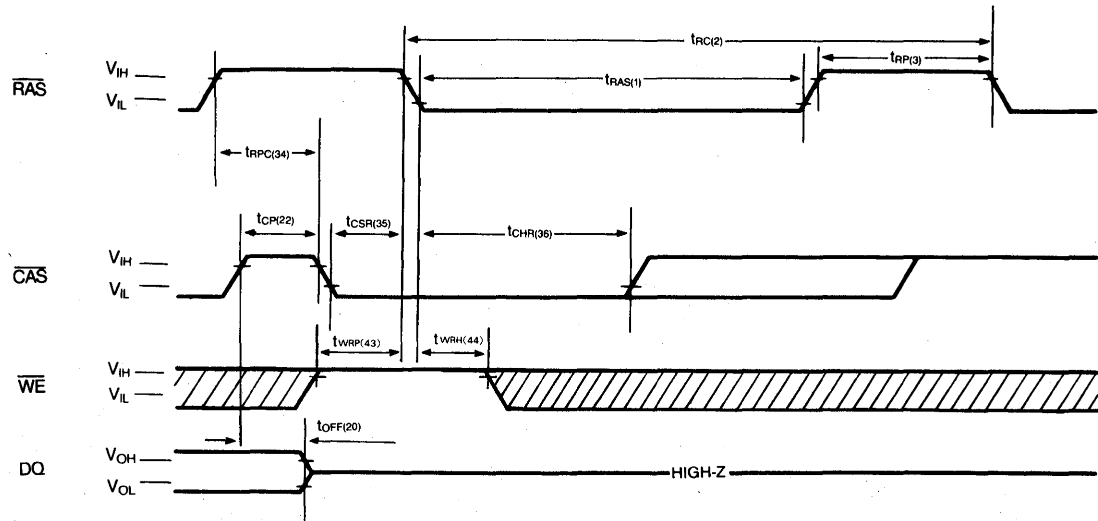
FAST PAGE MODE EARLY WRITE CYCLE



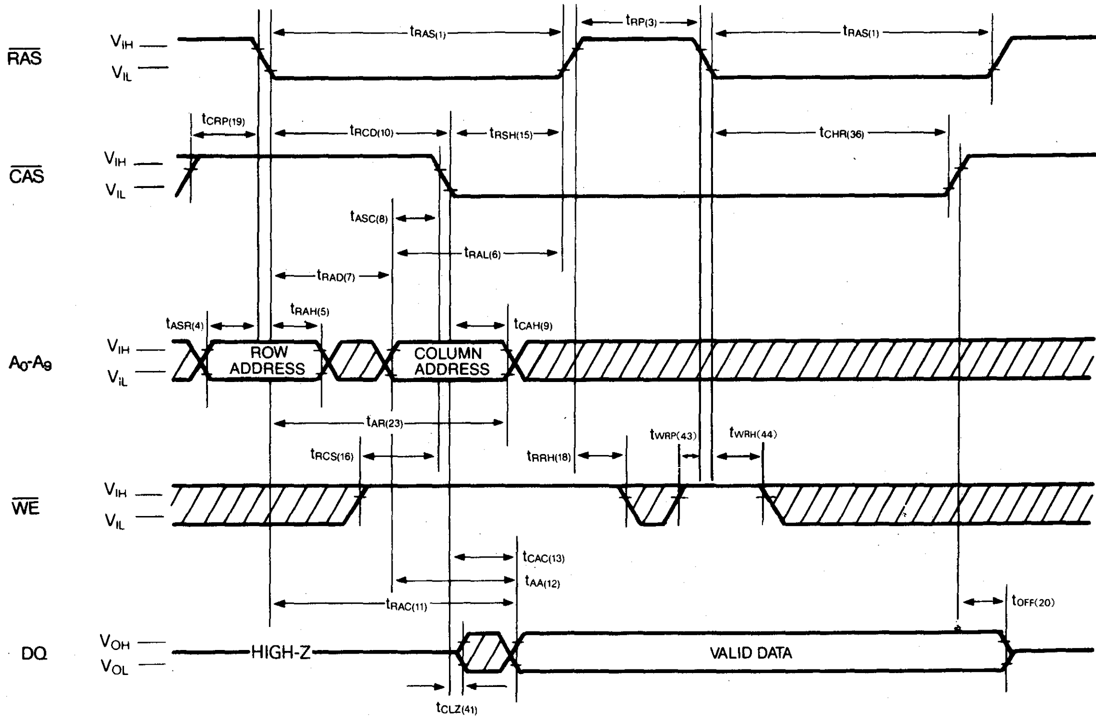
$\overline{RAS}$-ONLY REFRESH CYCLE



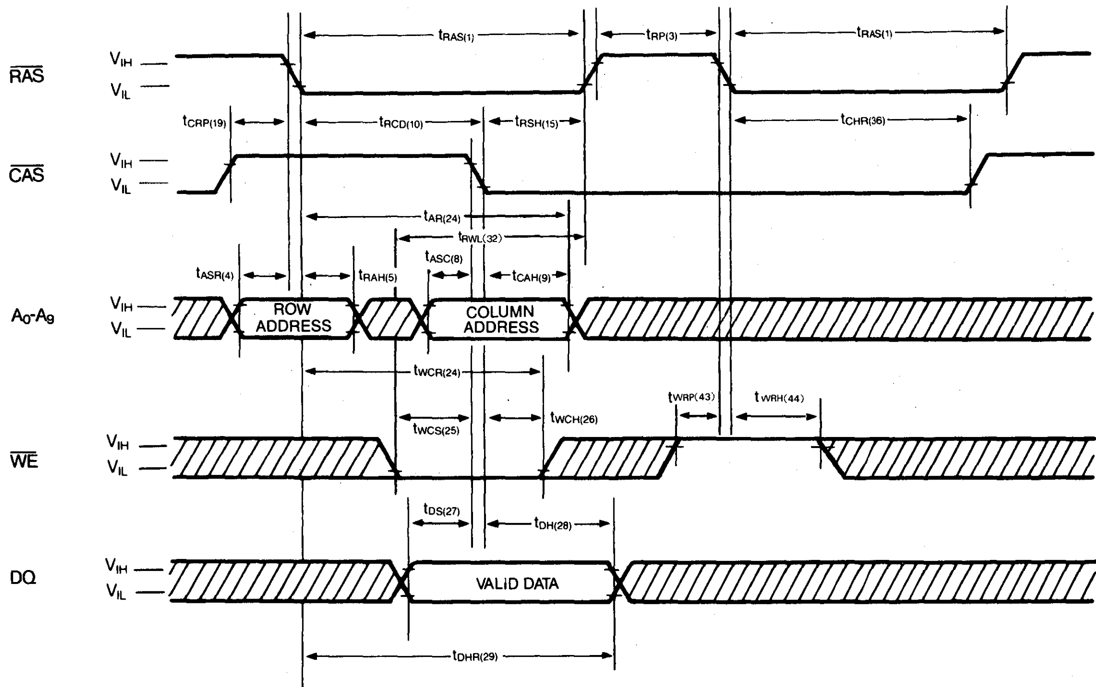
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



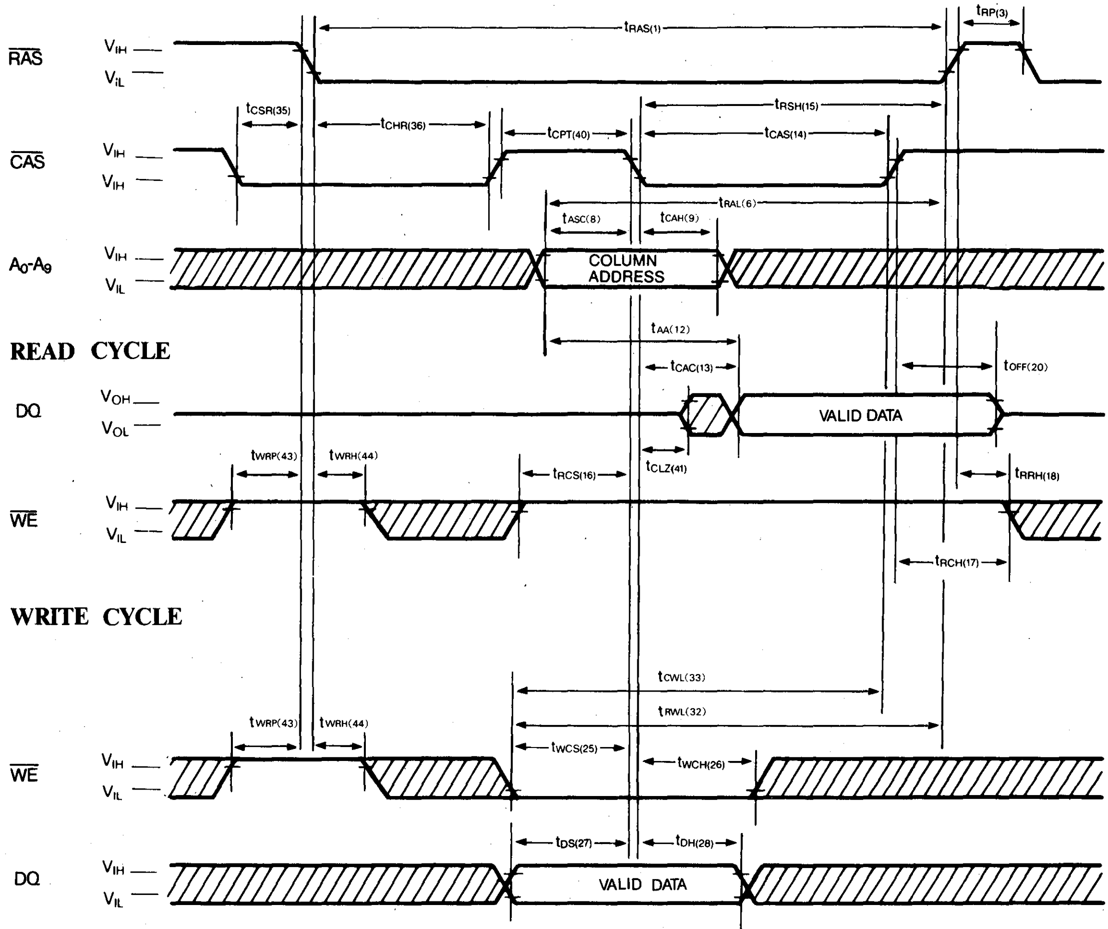
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

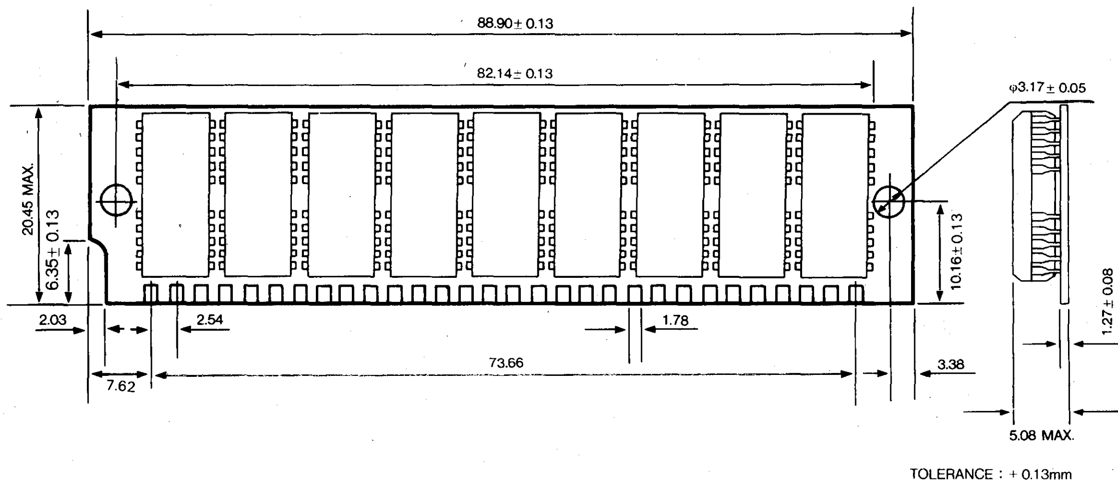


$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE

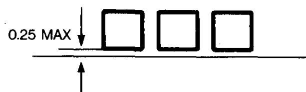


PACKAGE INFORMATION

HYM594000AM



* DETAIL OF CONTACTS



4

MEMO

HYUNDAI SEMICONDUCTOR

HYM594000AL

4M×9-Bit CMOS DRAM MODULE

M4I1200A-MAR92

DESCRIPTION

The HYM594000ALM is a 4M words by 9 bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of nine HY514100ALJ in 20/26 pin SOJ mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM594000ALM is a socket type single-in line module suitable for easy interchange and addition of 4M bytes memory with parity RAM.

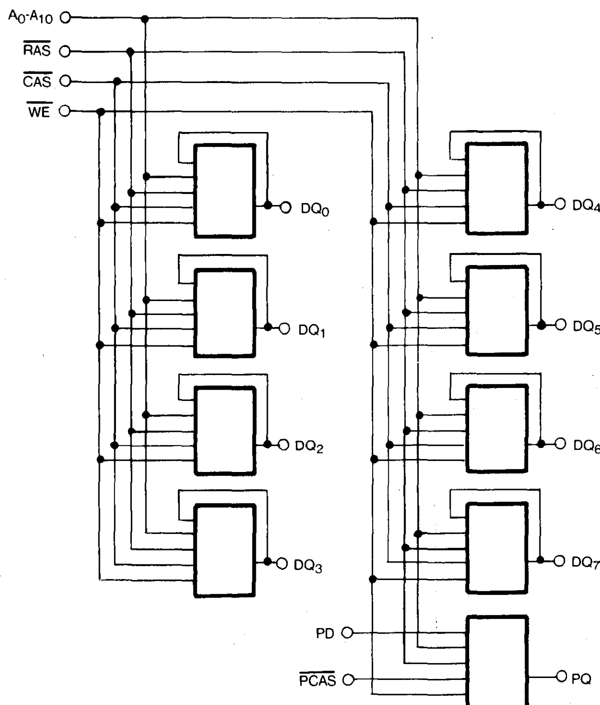
FEATURES

- **Fast Page Mode operation**
- **Fast Access Time**

	t_{RAC}	t_{CAC}	t_{PC}
HYM594000ALM-60	60	20	40
HYM594000ALM-70	70	20	45
HYM594000ALM-80	80	25	55

- **Single power supply of 5V± 10%**
- **$\overline{CAS}$-Before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden Refresh.**
- **Low power operating**
  5.12W max(HYM594000ALM-60)
  4.70W max(HYM594000ALM-70)
  4.21W max(HYM594000ALM-80)
- **TTL compatible inputs and outputs**
- **1024 refresh cycles/128ms**

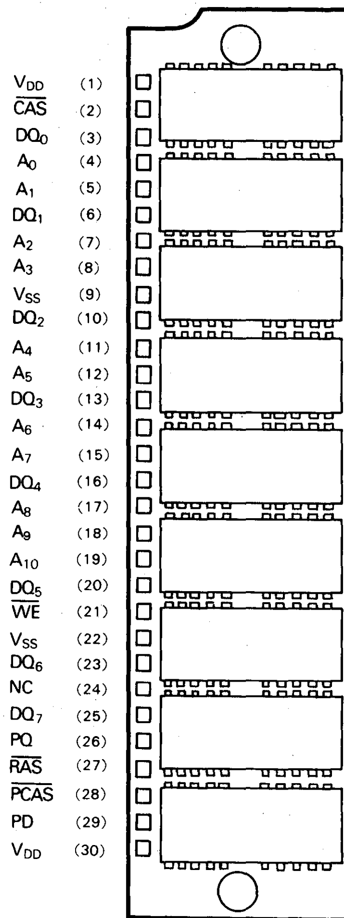
BLOCK DIAGRAM



PIN NAMES

A_0-A_{10}	ADDRESS INPUT
DQ_0-DQ_7	DATA INPUT/OUTPUT
PD	DATS IN FOR PARITY
$\overline{RAS}$	ROW ADDRESS STROBE
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{PCAS}$	CAS FOR PARITY
$\overline{WE}$	WRITE ENABLE
V_{DD}	POWER(+5V)
V_{SS}	GROUND

PIN CONNECTIONS



NOTES :

1. Common $\overline{CAS}$ control for eight data-in and data-out lines (DQ0-DQ7).
2. Separate $\overline{PCAS}$ control for one separate pair of data-in (PD) and data-out (PQ) lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ0-DQ7).

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	6.6	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	−	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	−	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM594000AL		UNIT	NOTE
				MIN.	MAX.		
$\|I_{LI}\|$	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$		−	90	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}		−	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC}=t_{RC}$(min.)	−60	−	945	mA	1
			−70	−	855		
			−80	−	765		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}=\overline{CAS}$ at V_{IH} other inputs$\geq V_{SS}$		−	18	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	$t_{RC}=t_{RC}$(min.)	−60	−	945	mA	
			−70	−	855		
			−80	−	765		
I_{DD4}	V_{DD} Supply Current, Fast page mode	Minimum Cycle	−60	−	585	mA	
			−70	−	495		
			−80	−	405		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS}<V_{DD}-0.2V$, $\overline{CAS}$= V_{IH}, other inputs$\geq V_{SS}$	−70	−	1.8	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh	$t_{RC}=t_{RC}$(min.)	−60	−	945	mA	
			−70	−	855		
			−80	−	765		
I_{DD7}	V_{DD} Supply Current, Battery Back up	$\overline{CAS}$=CBR cycling or 0.2V, $\overline{WE}=V_{DD}-0.2V$, Add=$V_{DD}$−0.2V or 0.2V I/O=$V_{DD}$−0.2V or 0.2V or open, t_{RC}=125μs, $t_{RAS}=t_{RAS}$(min.) ~300ns		−	2.7	mA	1
		Same as above except t_{RAS}=300ns~1μs		−	3.6	mA	1, 5
V_{OL}	Output Low Voltage	I_{OL}=4.5mA		−	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	−	V	

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AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1, 2, 3

#	SYMBOL	PARAMETER	HYM594000ALM						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	120	–	130	–	150	–	ns	
3	t_{RP}	$\overline{RAS}$ Prechange Time	50	–	50	–	60	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	10	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	–	35	–	40	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	15	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	20	50	20	55	ns	8
11	t_{RAC}	Access Time from $\overline{RAS}$	–	60	–	70	–	80	ns	4,8,9
12	t_{AA}	Access Time from Column Address	–	30	–	35	–	40	ns	4,9
13	t_{CAC}	Access Time from $\overline{CAS}$	–	20	–	20	–	25	ns	4,8
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	20	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	5	–	ns	
20	t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	15	–	ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
24	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50	–	55	–	60	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	15	–	ns	
27	t_{DS}	Data In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data In Hold Time	15	–	15	–	15	–	ns	7

#	SYMBOL	PARAMETER	HYM594000AL						UNIT	NOTE
			60		70		80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	50	–	55	–	60	–	ns	
30	t_{CPA}	Access Time from CAS Precharge	–	35	–	40	–	50	ns	4
31	t_{PC}	Fast Page Mode Read or Write Cycle Time	40	–	45	–	55	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	20	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	20	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	15	–	20	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	128	–	128	–	128	ms	
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	65	200K	75	200K	85	200K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	30	–	35	–	40	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	4
42	t_{CSH}	$\overline{CAS}$ Hold Time	60	–	70	–	80	–	ns	
43	t_{WRP}	$\overline{WE}$ to RAS Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to RAS Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

CAPACITANCE

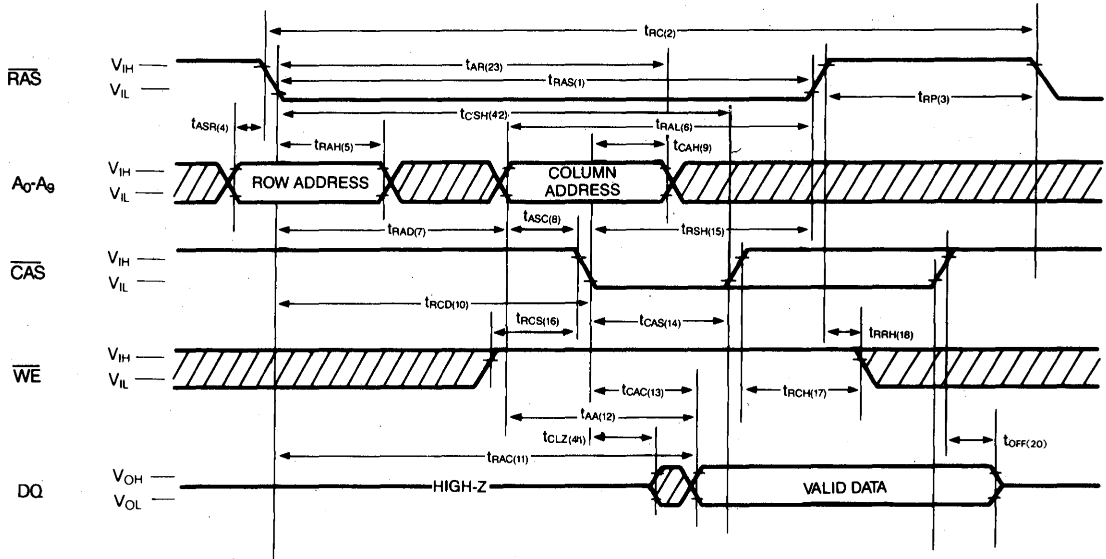
(T_A=25 °C,V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance(A_0-A_{10}, $\overline{WE}$, $\overline{CAS}$, $\overline{RAS}$)	–	55	pF
C_{DQ}	I/O Capacitance(DQ_0-DQ_7)	–	15	pF

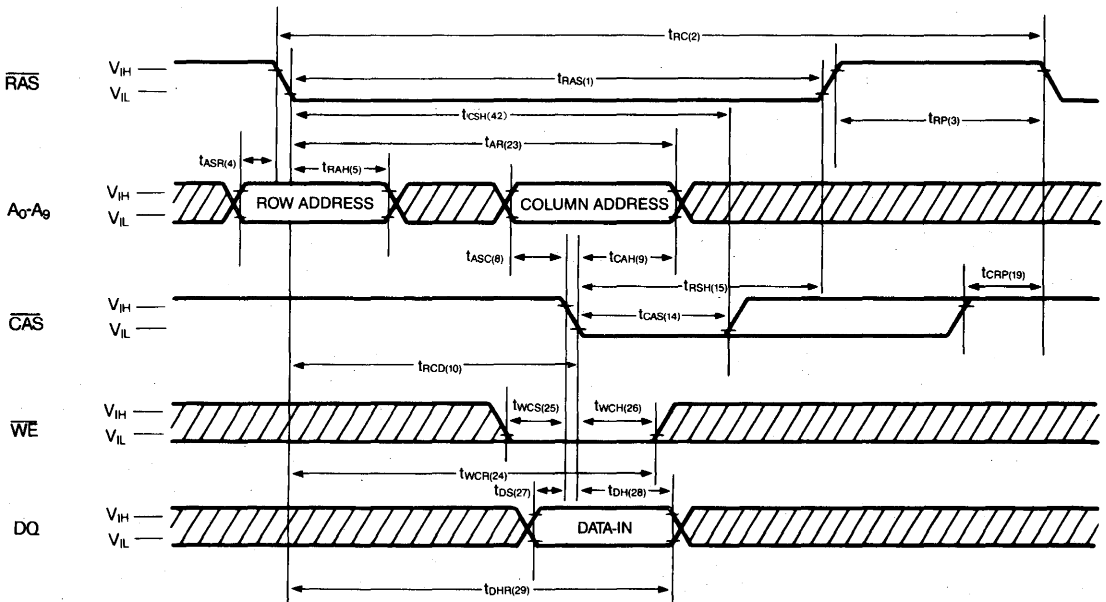
4

TIMING DIAGRAM

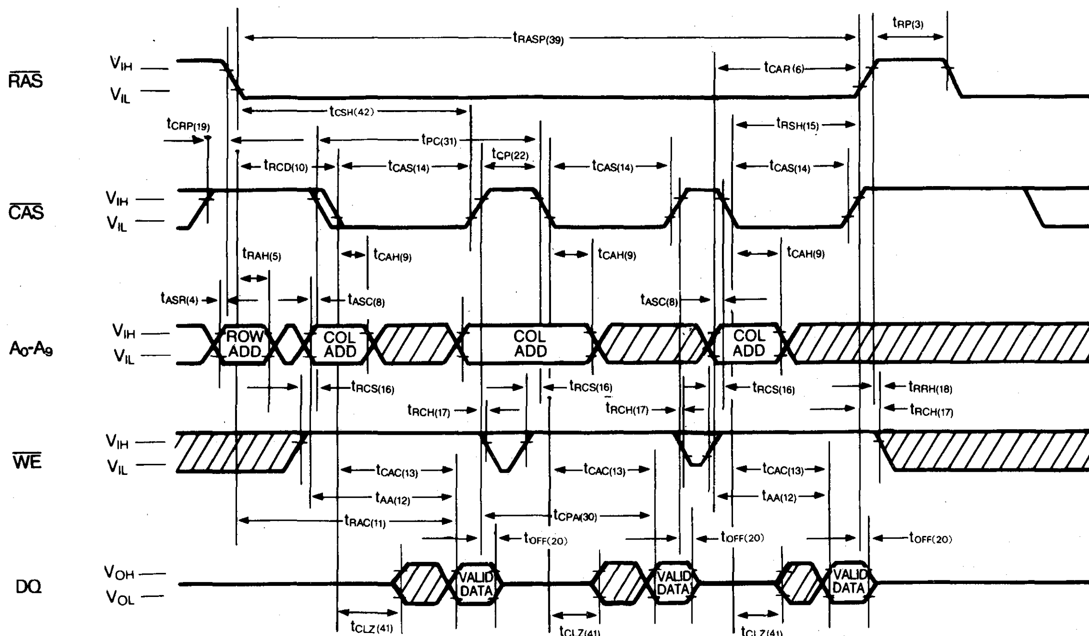
READ CYCLE



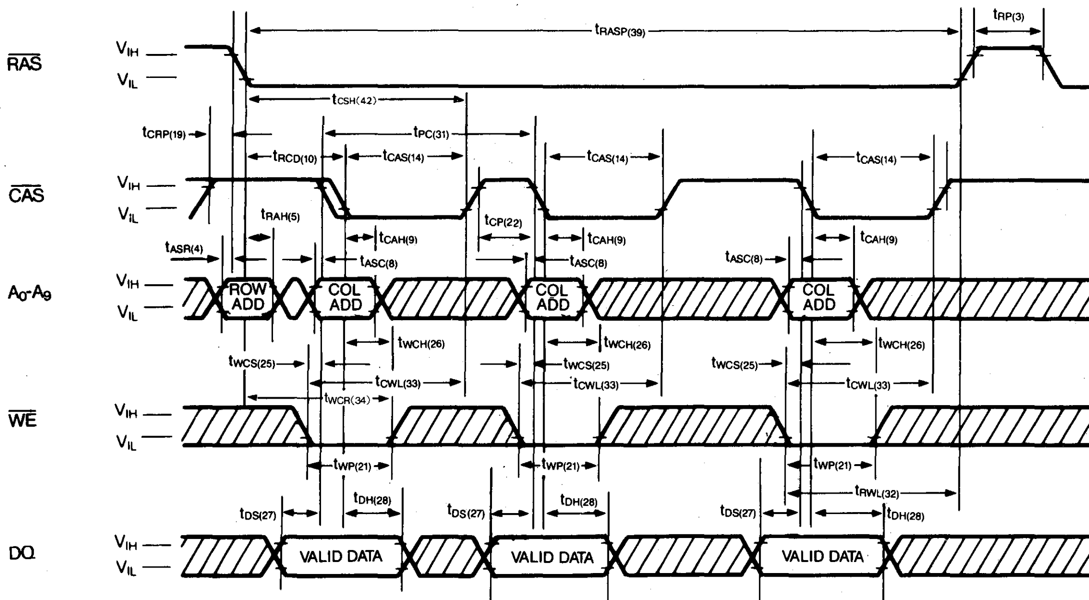
EARLY WRITE CYCLE



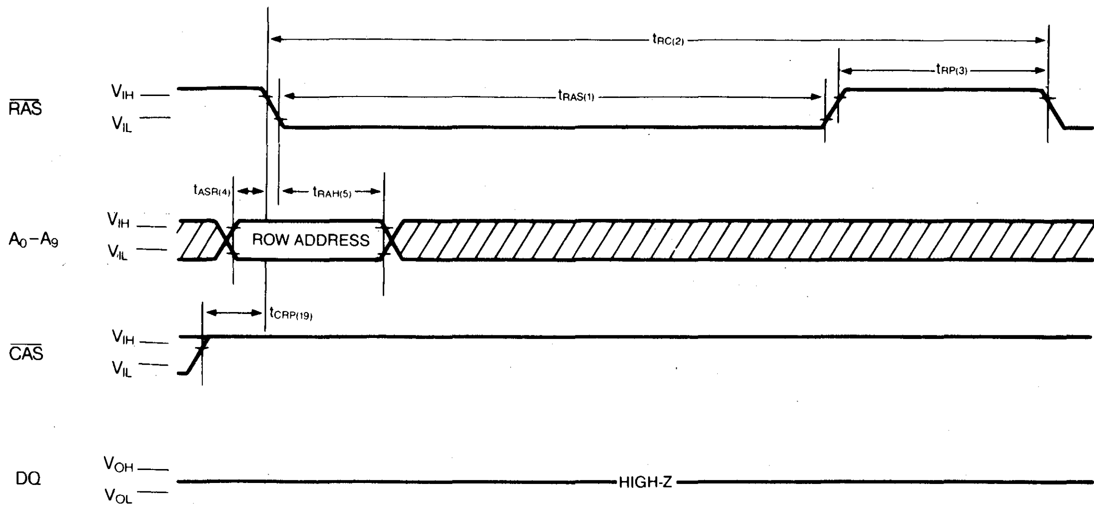
FAST PAGE MODE READ CYCLE



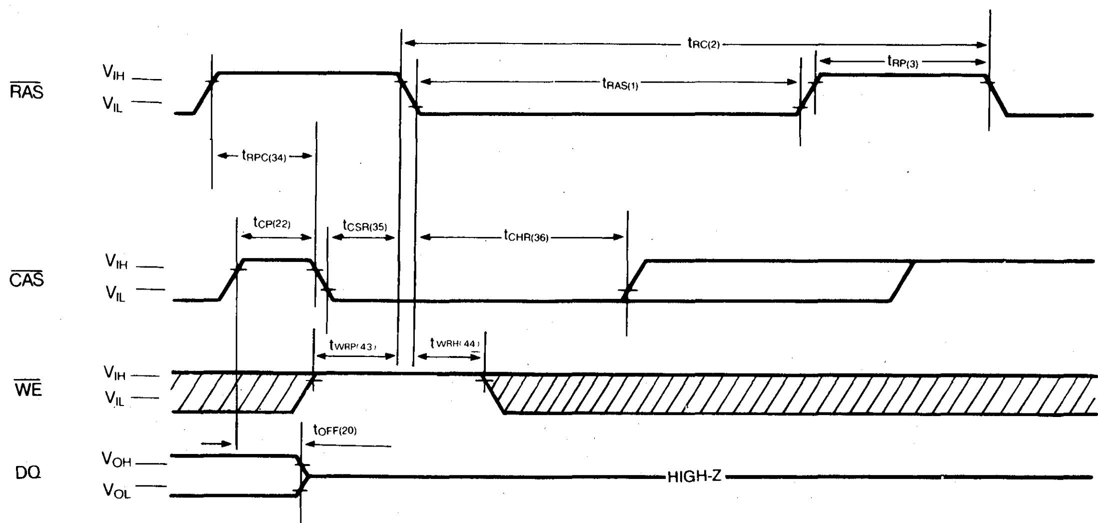
FAST PAGE MODE EARLY WRITE CYCLE



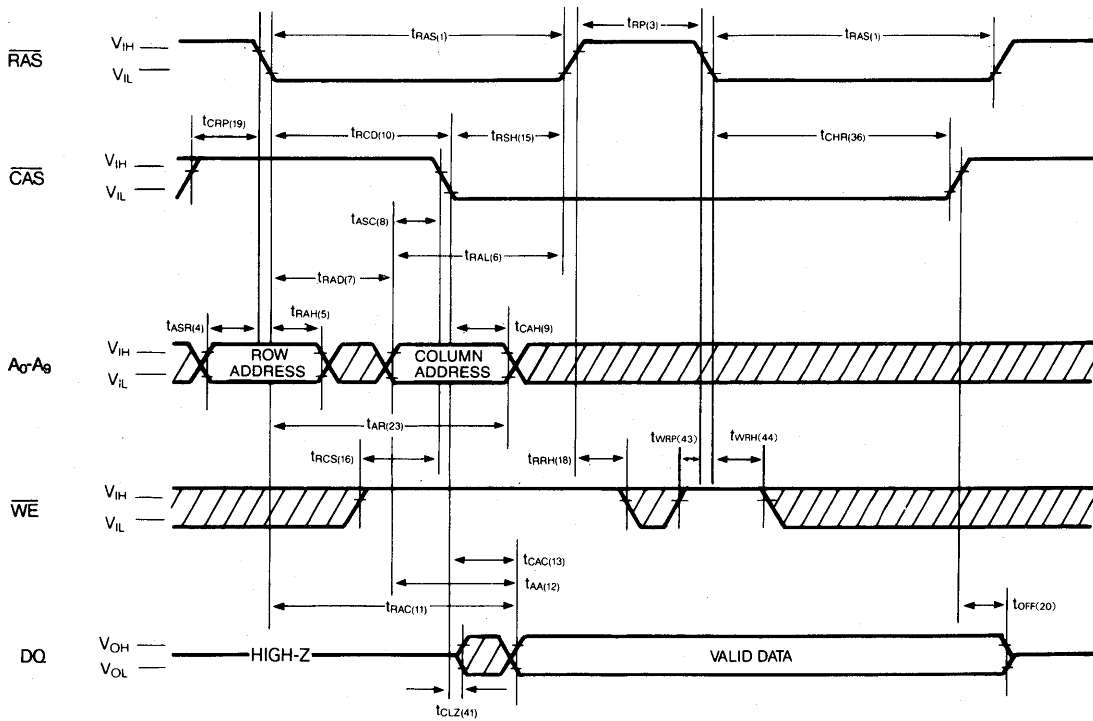
$\overline{RAS}$-ONLY REFRESH CYCLE



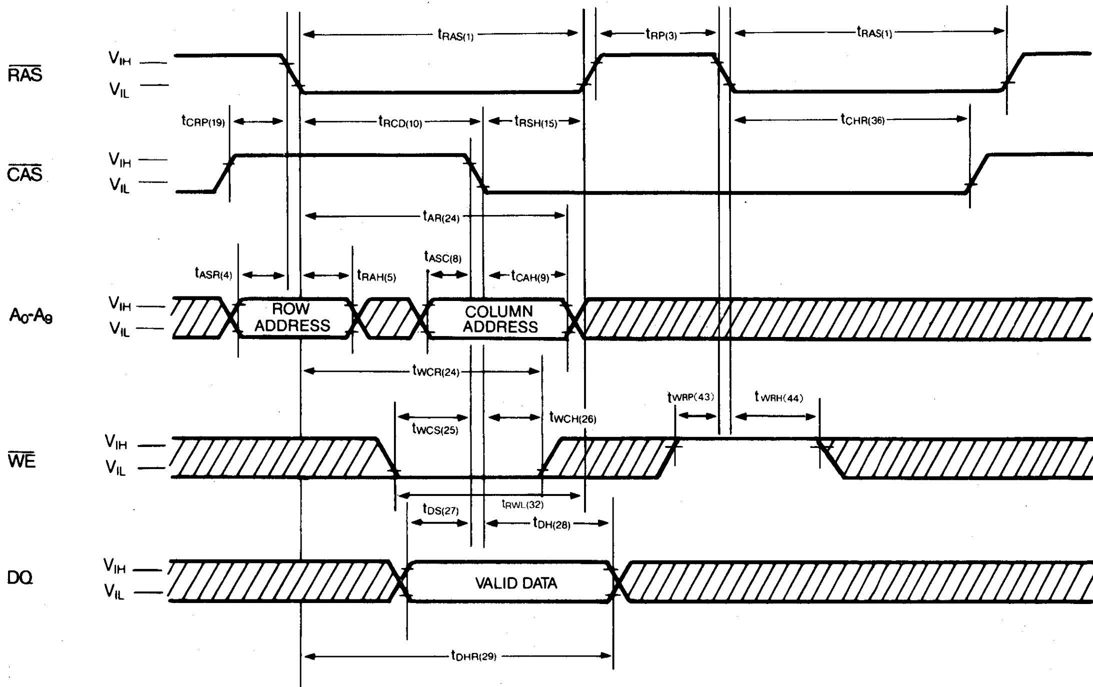
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE (READ)

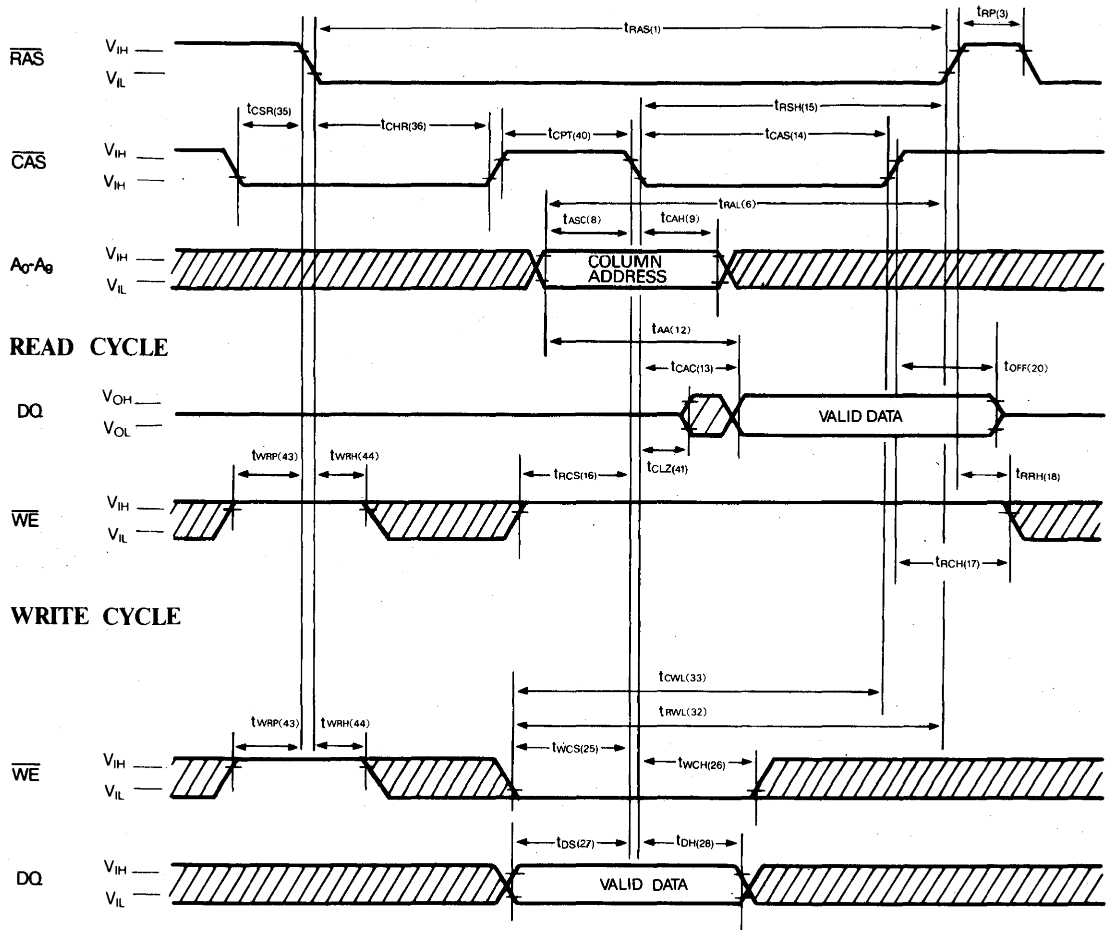


HIDDEN REFRESH CYCLE (WRITE)



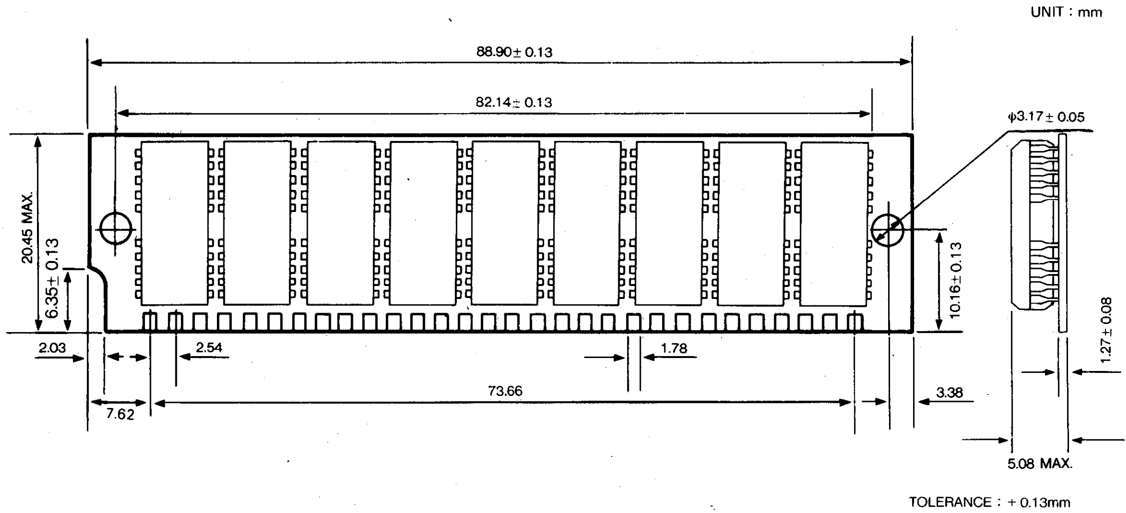
4

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

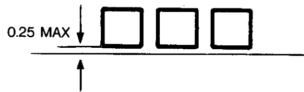


PACKAGE INFORMATION

HYM594000ALM



* DETAIL OF CONTACTS



MEMO

HYM536100

1M×36-Bits CMOS DRAM MODULE

M561200A-JAN92

DESCRIPTION

The HYM536100 is a 1M words by 36 bits dynamic RAM module which mounted Fast Page mode CMOS DRAMs of eight HY514400J and four HY531000J both in 20/26 pin SOJ on a 72 pin glass-epoxy printed circuit board. Decoupling capacitors are mounted under all the DRAMs.

The HYM536100 is optimized for applications required high density and large capacity memory. The HYM536100 can be used as 2M words by 18 bits dynamic DRAM module by using of connecting $DQ_0...DQ_{17}$ to $DQ_{18}...DQ_{35}$ respectively and selecting with RAS_0 or RAS_2.

The HYM536100M is a socket type single-in-line module suitable for easy interchange and addition of 4M bytes memory with parity.

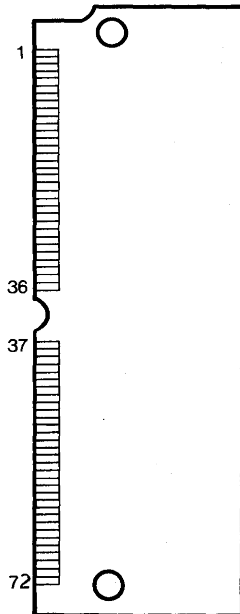
FEATURES

- Fast page mode operation
- Fast access Time

	t_{RAC}	t_{CAC}	t_{PC}
HYM536100M-70	70	20	50
HYM536100M-80	80	25	50
HYM536100M-10	100	25	60

- Single power supply of 5V± 10%
- $\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh
- Low power operation
  - 5.83W max. (HYM536100M-70)
  - 5.17W max. (HYM536100M-80)
  - 4.51W max. (HYM536100M-10)
- TTL compatible inputs and outputs
- 1024 refresh cycles/16ms
- High reliability gold plated contact pads

PIN CONNECTIONS



PIN NAMES

A_0-A_9	ADDRESS INPUT
DQ_0-DQ_{35}	DATA INPUT/OUTPUT
$\overline{RAS_0}$-$\overline{RAS_2}$	ROW ADDRESS STROBE
$\overline{CAS_0}$-$\overline{CAS_3}$	COLUMN ADDRESS STROBE
$\overline{WE}$	WRITE ENABLE
PD_1-PD_4	PRESENCE DETECT
V_{DD}	POWER(+5V)
V_{SS}	GROUND

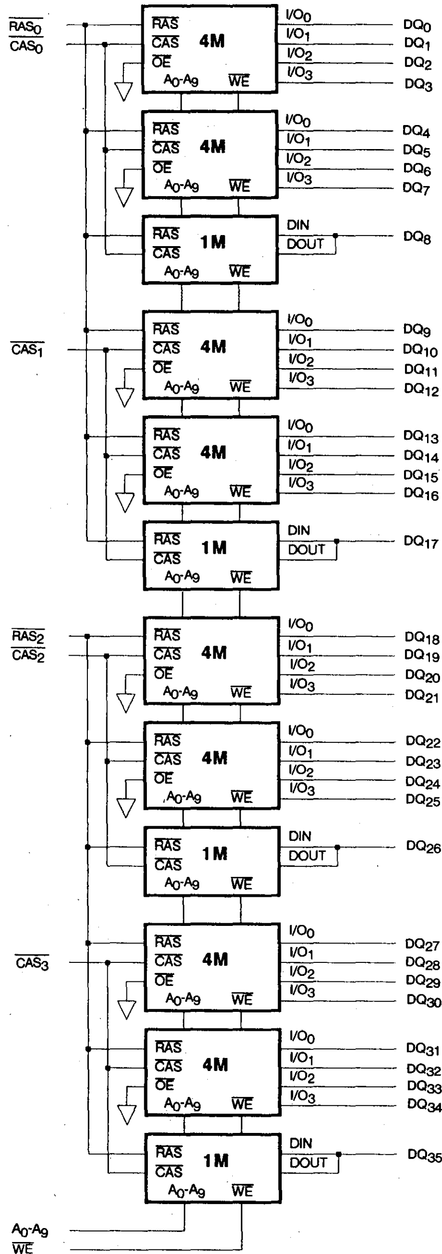
PIN DESCRIPTIONS

#	NAME	#	NAME
1	V_{SS}	37	DQ_{17}
2	DQ_0	38	DQ_{35}
3	DQ_{18}	39	V_{SS}
4	DQ_1	40	$\overline{CAS_0}$
5	DQ_{19}	41	$\overline{CAS_2}$
6	DQ_2	42	$\overline{CAS_3}$
7	DQ_{20}	43	$\overline{CAS_1}$
8	DQ_3	44	$\overline{RAS_0}$
9	DQ_{21}	45	NC
10	V_{DD}	46	NC
11	NC	47	$\overline{WE}$
12	A_0	48	NC
13	A_1	49	DQ_9
14	A_2	50	DQ_{27}
15	A_3	51	DQ_{10}
16	A_4	52	DQ_{28}
17	A_5	53	DQ_{11}
18	A_6	54	DQ_{29}
19	NC	55	DQ_{12}
20	DQ_4	56	DQ_{30}
21	DQ_{22}	57	DQ_{13}
22	DQ_5	58	DQ_{31}
23	DQ_{23}	59	V_{DD}
24	DQ_6	60	DQ_{32}
25	DQ_{24}	61	DQ_{14}
26	DQ_7	62	DQ_{33}
27	DQ_{25}	63	DQ_{15}
28	A_7	64	DQ_{34}
29	NC	65	DQ_{16}
30	V_{DD}	66	NC
31	A_8	67	PD_1
32	A_9	68	PD_2
33	NC	69	PD_3
34	$\overline{RAS_2}$	70	PD_4
35	DQ_{26}	71	NC
36	DQ_8	72	V_{SS}

PRESENCE DETECT PINS

PIN	-70	-80	-10
PD_1	V_{SS}	V_{SS}	V_{SS}
PD_2	V_{SS}	V_{SS}	V_{SS}
PD_3	V_{SS}	NC	V_{SS}
PD_4	NC	V_{SS}	V_{SS}

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	℃
T_{STG}	Storage Temperature(Plastic)	−55 to 150	℃
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	−1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	7.2	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	V_{DD}+1	V
V_{IL}	Input Low Voltage	−1.0	–	0.8	V

NOTE : All voltages are reference to V_{SS}.

DC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	MIN.	MAX.	UNIT	NOTE
$\|I_{LI}\|$	Input Leakage Current(Any Input Pins)	$V_{SS} \leq V_{IN} \leq V_{DD}$		–	120	μA	
$\|I_{LO}\|$	Output Leakage Current for High Impedance State	$V_{SS} \leq V_{OUT} \leq V_{DD}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		–	10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	t_{RC}=t_{RC}(min.)	−70	–	1060	mA	1
			−80	–	940		
			−10	–	820		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, Other inputs$\geq V_{SS}$		–	24	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-only Refresh	t_{RC}=t_{RC}(min.)	−70	–	1060	mA	
			−80	–	940		
			−10	–	820		
I_{DD4}	V_{DD} Supply Current, Fast Page mode	Minimum Cycle t_{PC}=t_{PC}(min.)	−70	–	860	mA	1
			−80	–	740		
			−10	–	620		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD}-0.2V$, $\overline{CAS} \geq V_{DD}-0.2V$ other inputs$\geq V_{SS}$		–	12	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ Refresh	t_{RC}=t_{RC}(min.)	−70	–	1060	mA	
			−80	–	940		
			−10	–	820		
V_{OL}	Output Low Voltage	I_{OL}=4.2mA		–	0.4	V	
V_{OH}	Output High Voltage	I_{OH}=−5mA		2.4	–	V	

NOTE :
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD}(max.) is measured with the output open.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.) NOTES : 1, 2, 3

#	SYMBOL	PARAMETER	HYM536100M						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	ns	
2	t_{RC}	Random Read or Write Cycle Time	130	–	150	–	180	–	ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	50	–	60	–	70	–	ns	
4	t_{ASR}	Row Address Set-up Time	0	–	0	–	0	–	ns	
5	t_{RAH}	Row Address Hold Time	10	–	10	–	15	–	ns	
6	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	–	40	–	50	–	ns	
7	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	9
8	t_{ASC}	Column Address Set-up Time	0	–	0	–	0	–	ns	
9	t_{CAH}	Column Address Hold Time	15	–	15	–	20	–	ns	
10	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	55	25	75	ns	8
11	t_{RAC}	Access Time From $\overline{RAS}$	–	70	–	80	–	100	ns	4, 8, 9
12	t_{AA}	Access Time From Column Address	–	35	–	40	–	50	ns	4, 9
13	t_{CAC}	Access Time From $\overline{CAS}$	–	20	–	25	–	25	ns	4, 8
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	25	10K	25	10K	ns	
15	t_{RSH}	$\overline{RAS}$ Hold Time	20	–	25	–	25	–	ns	
16	t_{RCS}	Read Command Set-up Time	0	–	0	–	0	–	ns	
17	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0	–	0	–	0	–	ns	6
18	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0	–	0	–	0	–	ns	6
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	10	–	ns	
20	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	ns	5
21	t_{WP}	Write Command Pulse Width	15	–	15	–	20	–	ns	
22	t_{CP}	$\overline{CAS}$ Precharge Time	10	–	10	–	10	–	ns	
23	t_{AR}	Column Address Hold Time From $\overline{RAS}$	55	–	60	–	80	–	ns	
24	t_{WCR}	Write Command Hold Time From $\overline{RAS}$	55	–	60	–	80	–	ns	
25	t_{WCS}	Write Command Set-up Time	0	–	0	–	0	–	ns	
26	t_{WCH}	Write Command Hold Time	15	–	15	–	20	–	ns	
27	t_{DS}	Data-In Set-up Time	0	–	0	–	0	–	ns	7
28	t_{DH}	Data-In Hold Time	15	–	15	–	20	–	ns	7

#	SYMBOL	PARAMETER	HYM536100M						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	t_{DHR}	Data-In Hold Time Reference to $\overline{RAS}$	55	–	60	–	80	–	ns	
30	t_{CPA}	Access Time From $\overline{CAS}$ Precharge	–	45	–	45	–	55	ns	4
31	t_{PC}	Fast Page Mode Read or Write Cycle time	50	–	50	–	60	–	ns	
32	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	–	25	–	25	–	ns	
33	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	–	25	–	25	–	ns	
34	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	–	0	–	0	–	ns	
35	t_{CSR}	$\overline{CAS}$ Set-up Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	10	–	10	–	10	–	ns	
36	t_{CHR}	$\overline{CAS}$ Hold Time($\overline{CAS}$ Before $\overline{RAS}$ Cycle)	30	–	30	–	30	–	ns	
37	t_T	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	3
38	t_{REF}	Refresh Period	–	16	–	16	–	16	ms	
39	t_{RASP}	$\overline{RAS}$ Pulse Width(Fast Page Mode)	70	100K	80	100K	100	100K	ns	
40	t_{CPT}	$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	40	–	40	–	50	–	ns	
41	t_{CLZ}	$\overline{CAS}$ to Output Low Impedance	0	–	0	–	0	–	ns	
42	t_{CSH}	$\overline{CAS}$ Hold Time	70	–	80	–	100	–	ns	
43	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle)	10	–	10	–	10	–	ns	
44	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle)	10	–	10	–	10	–	ns	

NOTES :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
8. Operation within the t_{RCD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only : If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
9. Operation within the t_{RAD}(max.) limit insures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only : If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.

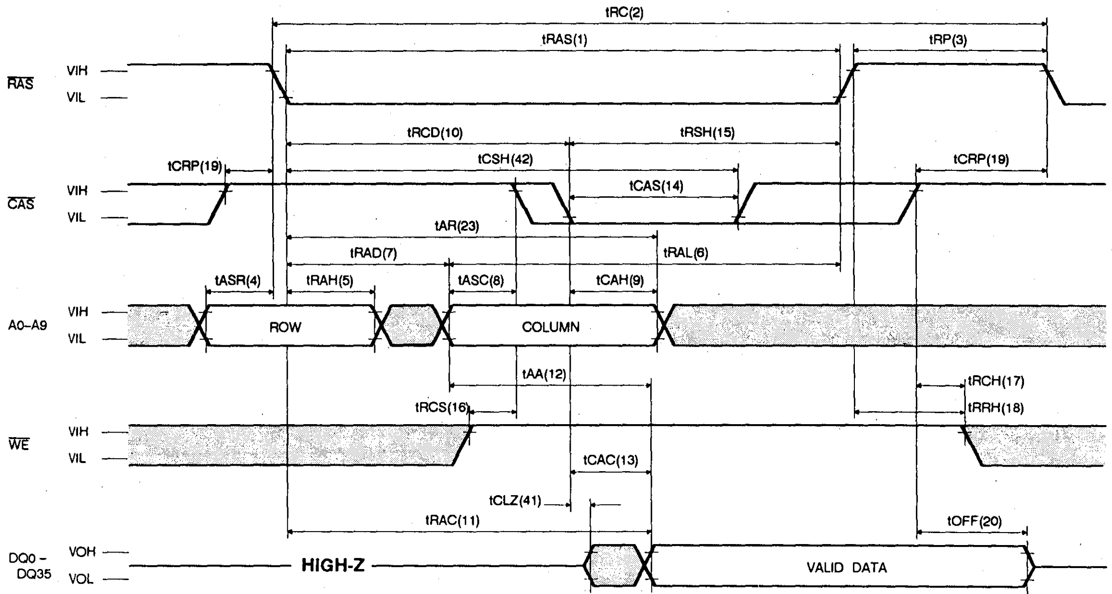
CAPACITANCE

(T_A=25°C, V_{DD}=5V± 10%, V_{SS}=0V, unless otherwise noted.)

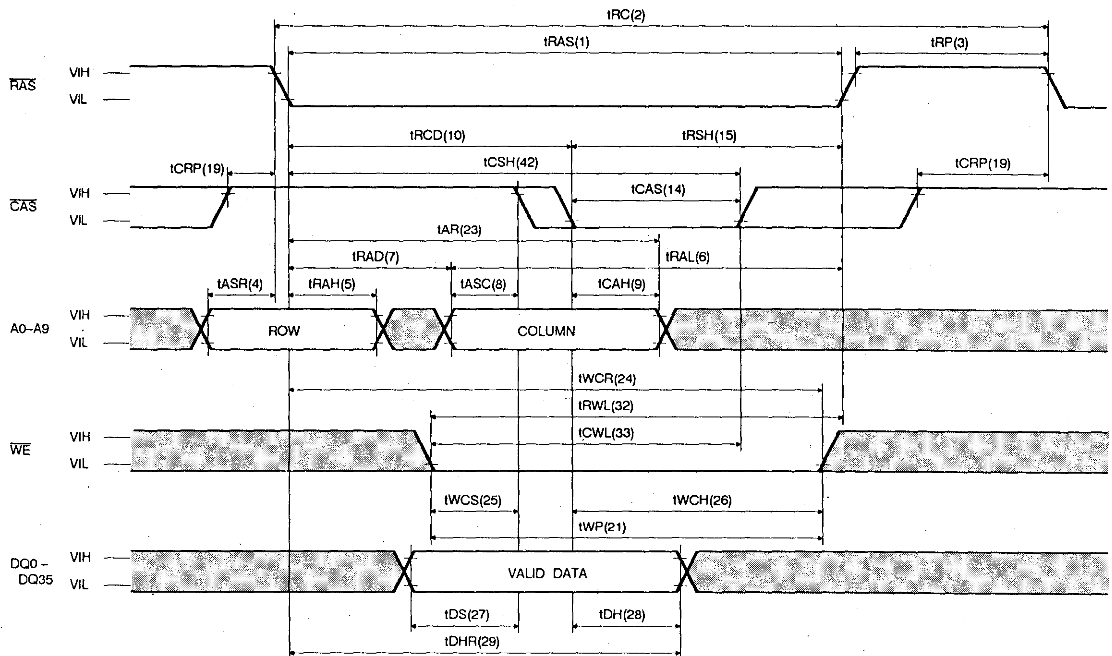
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance(A_0-A_9)	–	88	pF
C_{IN2}	Input Capacitance($\overline{WE}$)	–	104	pF
C_{IN3}	Input Capacitance($\overline{RAS_0}$-$\overline{RAS_2}$)	–	57	pF
C_{IN4}	Input Capacitance($\overline{CAS_0}$-$\overline{CAS_3}$)	–	36	pF
C_{DQ1}	I/O Capacitance($DQ_{0-7,\ 9-16,\ 18-25,\ 27-34}$)	–	17	pF
C_{DQ2}	I/O Capacitance($DQ_{8,\ 17,\ 26,\ 35}$)	–	22	pF

TIMING DIAGRAM

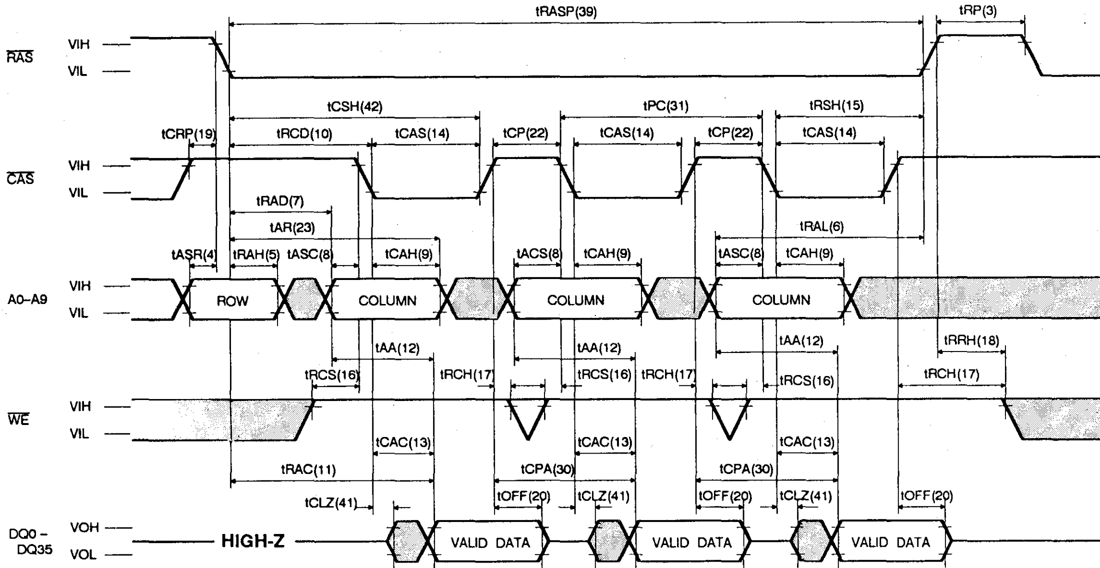
READ CYCLE



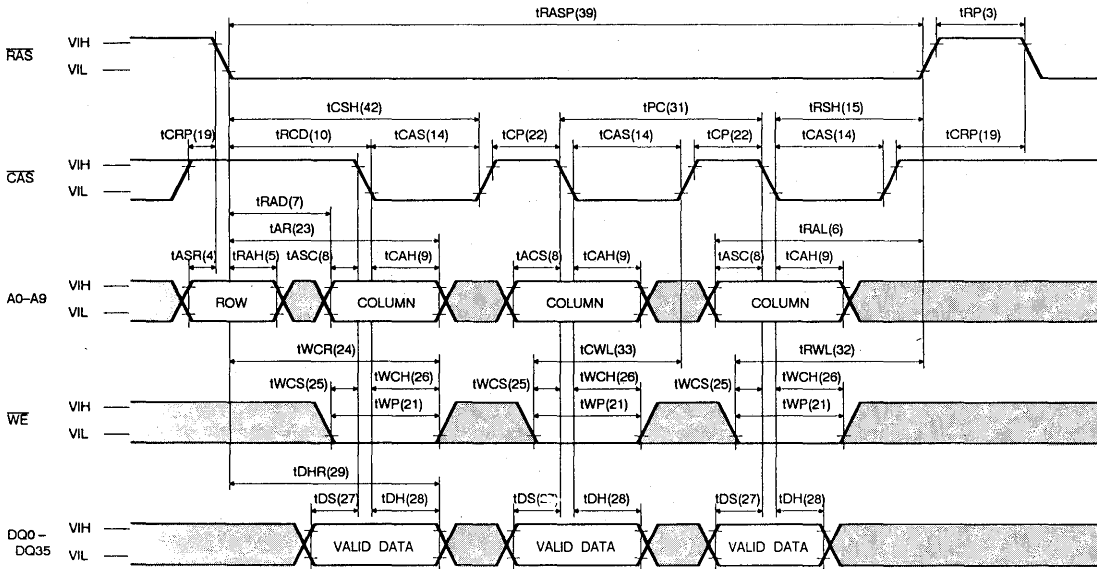
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

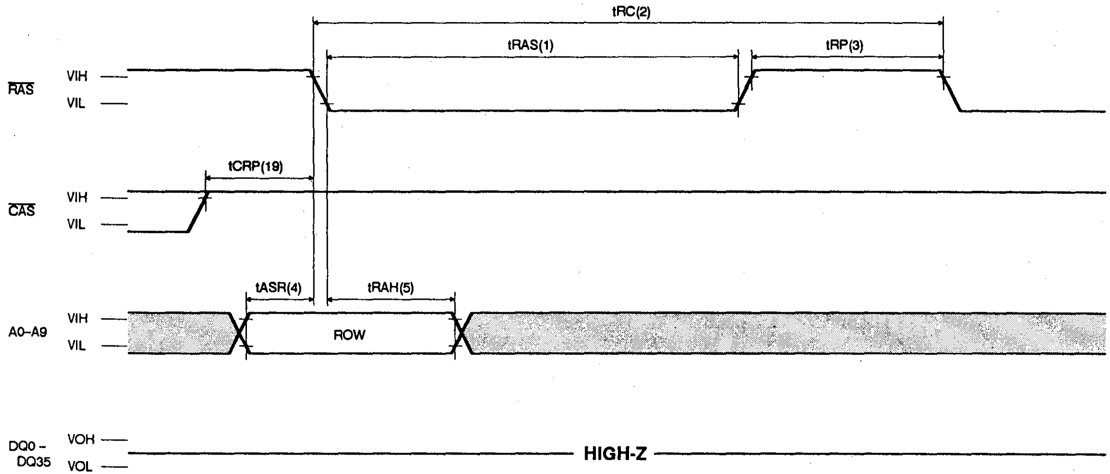


FAST PAGE MODE EARLY WRITE CYCLE



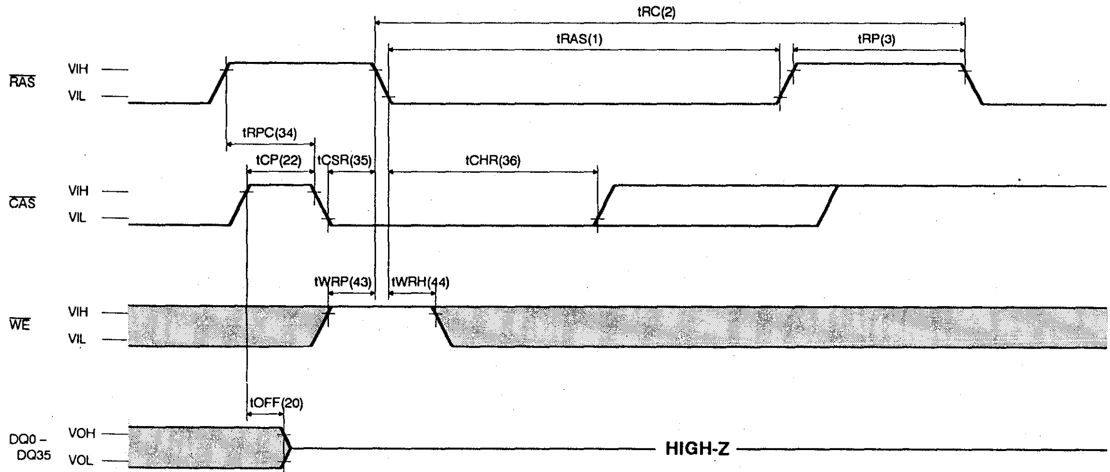
4

RAS-ONLY REFRESH CYCLE



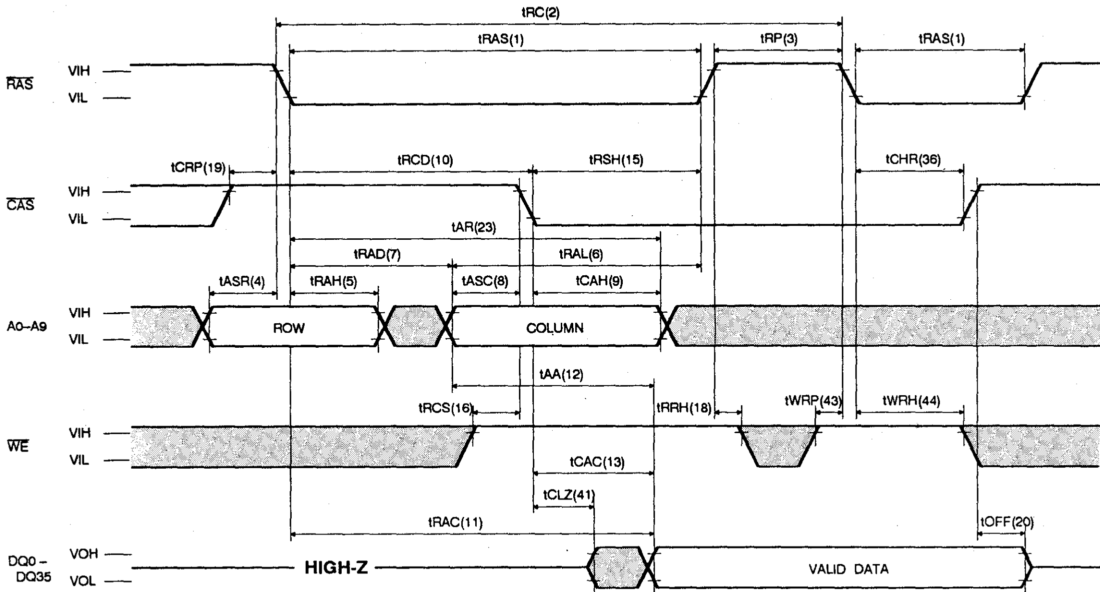
NOTE : WE = DON'T CARE

CAS-BEFORE-RAS REFRESH CYCLE

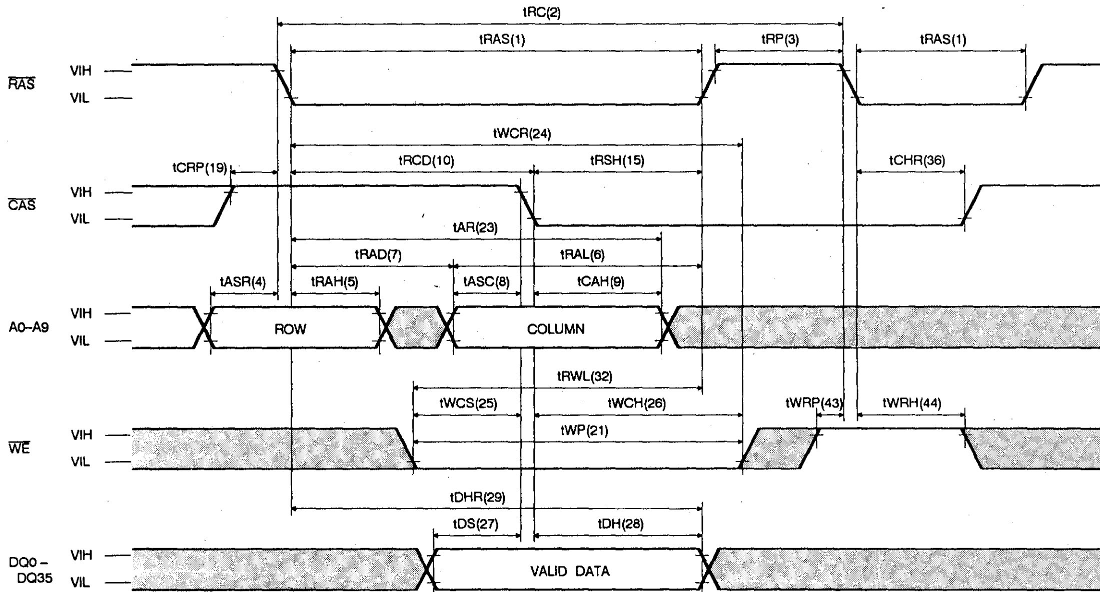


NOTE : A0~A9 = DON'T CARE

HIDDEN REFRESH CYCLE (READ)

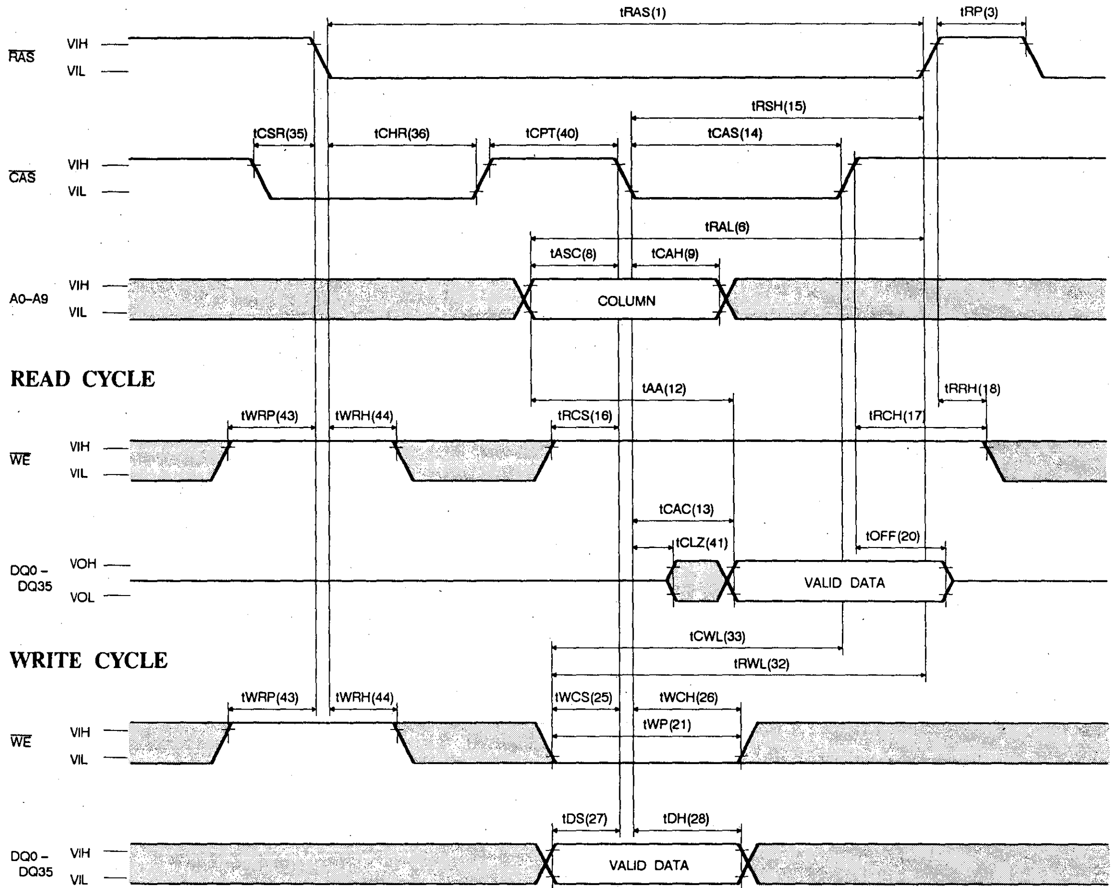


HIDDEN REFRESH CYCLE (WRITE)



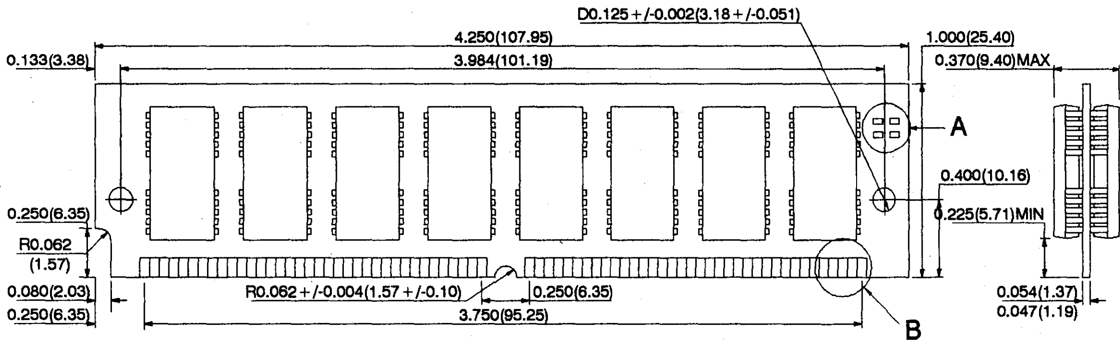
4

$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE

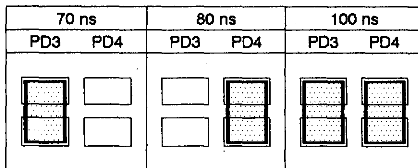


PACKAGE INFORMATION

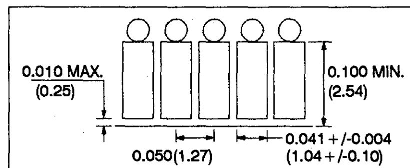
HYM536100M



DETAIL A



DETAIL B



MEMO

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HYUNDAI SEMICONDUCTOR

HY6116A

2K×8-Bit CMOS SRAM

M211201A-MAY92

DESCRIPTION

The HY6116A is a high speed, low power, 2,048 words by 8-bit CMOS static RAM fabricated using high performance CMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 85ns.

The HY6116A has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt.

Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY6116A family.

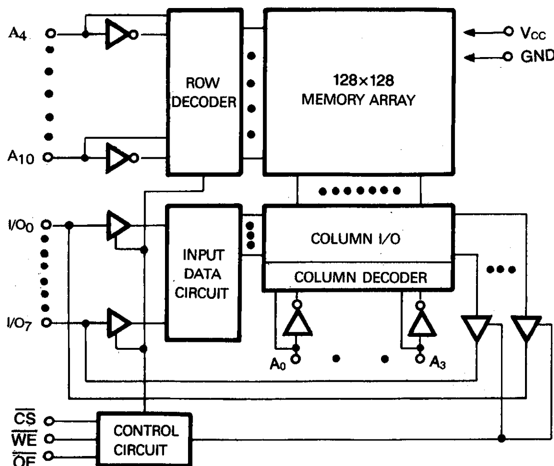
FEATURES

- High speed−85/100/120/150ns (max.)
- Low power consumption
  - 150 mW typical operating
  - 0.5 μW typical standby (L-version)
- Battery backup (L-version)
  - 2 volt data retention
- Fully static operation
  - No clock or refresh required
- All inputs and outputs directly TTL compatible
- Tri-state output
- High reliability 24 pin 600 mil P-DIP

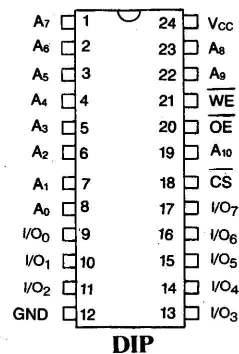
		HY6116A-85	HY6116A-10	HY6116A-12	HY6116A-15
Maximum Access Time (ns)		85	100	120	150
Maximum Operating Current (mA)		60	60	60	60
Maximum Standby Current (μA)		50	50	50	50
	L	5	5	5	5

5

BLOCK DIAGRAM



PIN CONNECTIONS



DIP

PIN NAMES

A0−A10	ADDRESS INPUT
I/O0−I/O7	DATA INPUT / OUTPUT
CS	CHIP SELECT
WE	WRITE ENABLE
OE	OUTPUT ENABLE
Vcc	POWER
GND	GROUND

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}, V_{IN}, $V_{I/O}$	Power Supply, Input, Input/Output Voltage	−0.5[2] to 7.0	V
T_{BIAS}	Temperature Under Bias	−10 to 125	℃
T_{STG}	Storage Temperature	− 55 to 150	℃
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA

NOTES :
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. −3.5V for 20 ns pulse.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5[1]	0	0.8	V

NOTE :
1. −3.5V for 20ns pulse.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O OPERATION
Standby	H	X	X	High-Z
Output Disabled	L	H	H	High-Z
Read	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

NOTE :
1. X : H or L

DC CHARACTERISTICS
(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS		HY6116A			UNIT
				MIN.	TYP.[1]	MAX.	
$\vert I_{LI} \vert$	Input Leakage Current	V_{IN}=GND to V_{CC}		–	–	2	μA
$\vert I_{LO} \vert$	Output Leakage Current	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=GND to V_{CC}		–	–	2	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}$=V_{IL}, Duty Cycle=100%		–	30	60	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$=V_{IH}		–	0.5	3	mA
I_{SB1}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{CC}−0.2,		–	4	50	μA
		V_{IN}=GND to V_{CC}	L	–	0.1	5	μA
V_{OL}	Output Low Voltage	I_{OL}=4.0mA		–	–	0.4	V
V_{OL}	Output High Voltage	I_{OH}=−1.0mA		2.4	–	–	V

NOTE :
1. Typical values are at V_{CC}=5V, T_A=25°C and specified loading

AC CHARACTERISTICS
(V_{CC}=5V± 10%, T_A=0°C to 70°C)

READ CYCLE

SYMBOL	PARAMETER	HY6116A-85		HY6116A-10		HY6116A-12		HY6116A-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	120	–	150	–	ns
t_{AA}	Address Access Time	–	85	–	100	–	120	–	150	ns
t_{ACS}	Chip Select Access Time	–	85	–	100	–	120	–	150	ns
t_{CLZ}	Chip Select to Output in Low-Z	10	–	10	–	10	–	10	–	ns
t_{OE}	Output Enable to Output Valid	–	45	–	50	–	55	–	60	ns
t_{OLZ}	Output Enable to Output in Low-Z	10	–	10	–	10	–	10	–	ns
t_{CHZ}	Chip Deselect to Output in High-Z	0	40	0	40	0	40	0	50	ns
t_{OHZ}	Output Disable to Output in High-Z	0	40	0	40	0	40	0	50	ns
t_{OH}	Output Hold from Address Change	10	–	10	–	10	–	15	–	ns

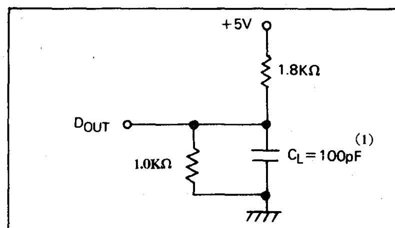
WRITE CYCLE

SYMBOL	PARAMETER	HY6116A-85		HY6116A-10		HY6116A-12		HY6116A-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	120	–	150	–	ns
t_{CW}	Chip Select to End of Write	60	–	65	–	70	–	90	–	ns
t_{AW}	Address Valid to End of Write	70	–	80	–	105	–	120	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Wirte Pulse Width	55	–	60	–	70	–	80	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{OHZ}	Output Disable to Output in High-Z	0	40	0	40	0	40	0	50	ns
t_{WHZ}	Wirte to Output in High-Z	0	30	0	30	0	35	0	40	ns
t_{DW}	Data to Write Time Overlap	30	–	30	–	35	–	40	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write	10	–	10	–	10	–	10	–	ns

AC TEST CONDITIONS
(T_A=0°C to 70°C)

Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V

OUTPUT LOAD



NOTE :
1. Including scope and the jig.

CAPACITANCE[1]
(T_A=25°C,f=1.0 MHz)

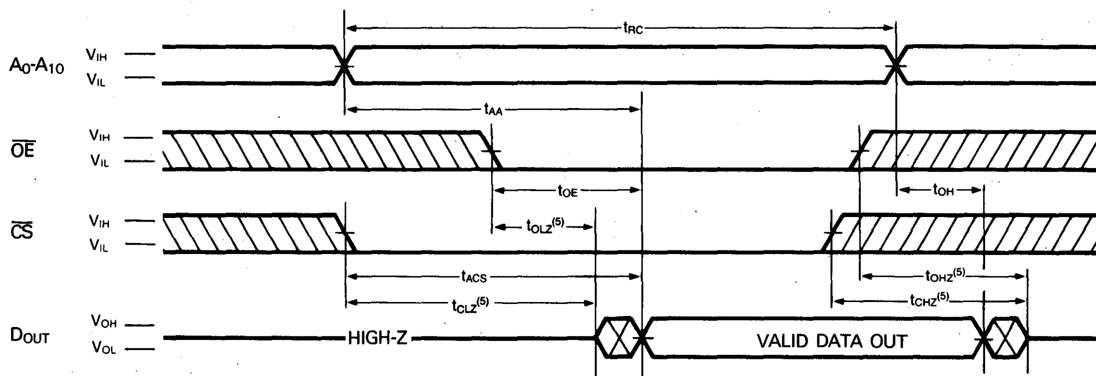
SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

NOTE :
1. This parameter is sampled and not 100% tested.

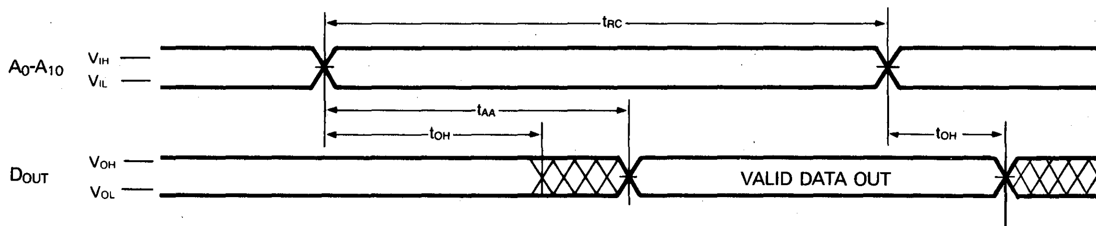
5

TIMING DIAGRAMS

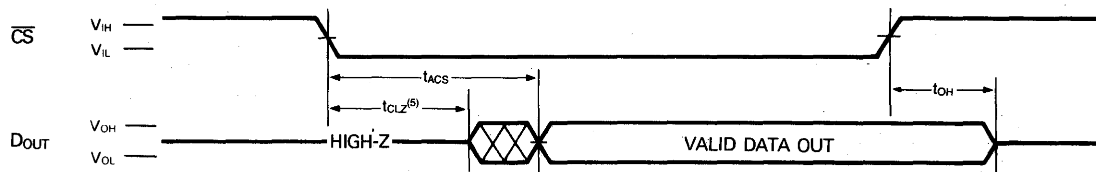
READ CYCLE 1[1]



READ CYCLE 2[1,2,4]

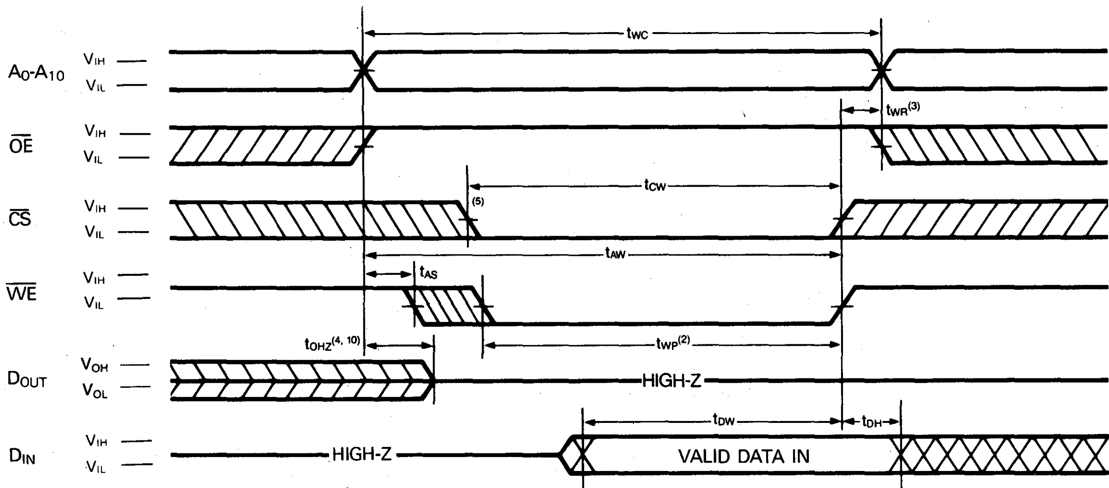


READ CYCELE 3[1,3,4]

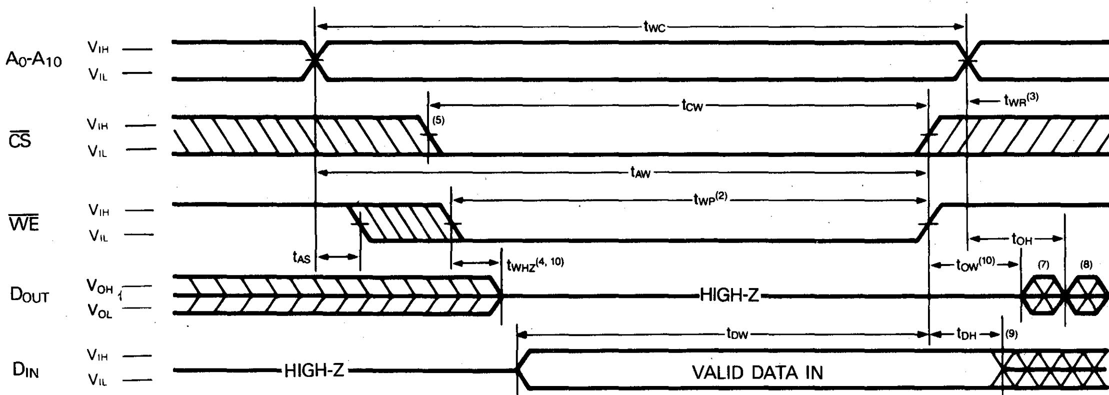


NOTES:
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected $\overline{CS}=V_{IL}$
3. Addresses are valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}=V_{IL}$
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE 1(1)



WRITE CYCLE 2(1, 6)



NOTES:

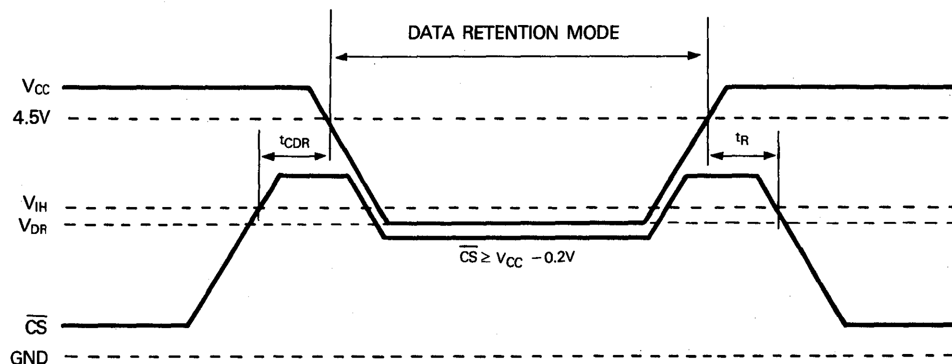
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ± 500mV from steady state.

DATA RETENTION CHARACTERISTICS[1]
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.[2]	MAX.	UNIT
V_{DR}	Data Retention Supply Voltage	V_{IN}=0 to V_{CC}, $\overline{CS} \geq V_{CC}-0.2V$	2.0	–	–	V
I_{CCDR}	Data Retention Supply Current	V_{CC}=3V, V_{IN}=0 to V_{CC}, $\overline{CS} \geq V_{CC}-0.2V$	–	0.05	2.0	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram	0	–	–	ns
t_R	Operation Recovery Time		t_{RC}[3]	–	–	ns

NOTES :
1. These characteristics are guaranteed for L-version.
2. T_A=25℃
3. t_{RC}=Read Cycle Time

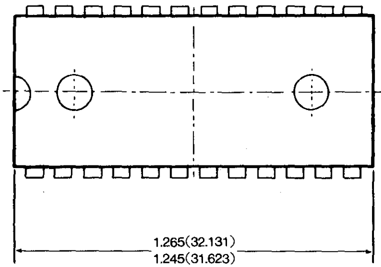
DATA RETENTION TIMING DIAGRAM

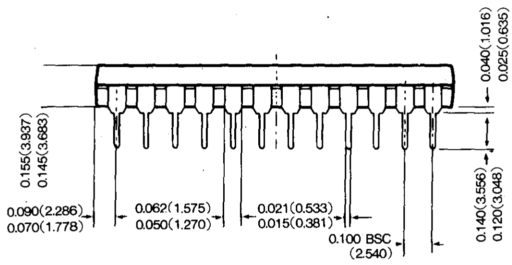


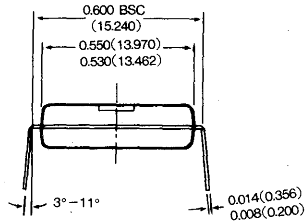
PACKAGE INFORMATION

- **24 PIN PLASTIC DUAL IN LINE PACKAGE − 600 MIL**

UNIT : INCH(mm) MAX/MIN







MEMO

HYUNDAI SEMICONDUCTOR

HY6264

8K×8-Bit CMOS SRAM

M221201B-MAY92

DESCRIPTION

The HY6264 is a high speed, low power 8,192 words by 8-bit CMOS static RAM fabricated using high performance CMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 70ns.

The HY6264 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt.

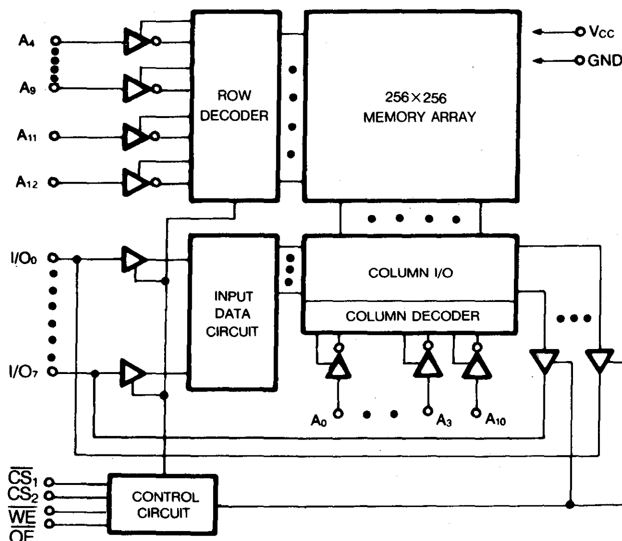
Using CMOS technology, supply voltages from 2.0 to 5.5 volts have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY6264 family.

FEATURES

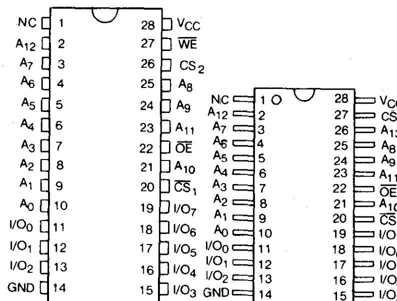
- **High speed—70/85/100/120/150ns (max.)**
- **Low power consumption**
  - **—200 mW typical operating**
  - **—10 μW typical standby (L-version)**
- **Battery back up (L-version)**
  - **—2 volt data retention**
- **Fully static operation**
  - **—No clock or refresh required**
- **All inputs and outputs directly TTL compatible**
- **Tri-state output**
- **High reliability 28-pin 600 mil P-DIP and 330 mil SOP**

		HY6264-70	HY6264-85	HY6264-10	HY6264-12	HY6264-15
Maximum Access Time (ns)		70	85	100	120	150
Maximum Operating Current (mA)		70	70	70	70	70
Maximum Standby Current (mA)		2	2	2	2	2
	L	0.1	0.1	0.1	0.1	0.1

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_{12}	ADDRESS INPUT
I/O_0-I/O_7	DATA INPUT/OUTPUT
$\overline{CS_1}$	CHIP SELECT ONE
CS_2	CHIP SELECT TWO
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
V_{cc}	POWER
GND	GROUND

5

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}, V_{IN}, $V_{I/O}$	Power Supply, Input, Input/Output Voltage	−0.5[2] to 7.0	V
T_{BIAS}	Temperature Under Bias	−10 to 125	°C
T_{STG}	Storage Temperature	−65 to 150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA

NOTES :
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. −3.5V for 20ns pulse.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5	0	0.8	V

TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	I/O OPERATION	V_{CC} CURRENT	NOTE
Not Selected (Power Down)	X	H	X	X	High-Z	I_{SB}, I_{SB1}	
	X	X	L	X	High-Z	I_{SB}, I_{SB2}	
Output Disabled	H	L	H	H	High-Z	I_{CC}, I_{CC1}	
Read	H	L	H	L	D_{OUT}	I_{CC}, I_{CC1}	
Write	L	L	H	H	D_{IN}	I_{CC}, I_{CC1}	Write Cycle 1
	L	L	H	L	D_{IN}	I_{CC}, I_{CC1}	Write Cycle 2

DC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS		HY6264 MIN.	HY6264 TYP.[1]	HY6264 MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{IN}=GND to V_{CC}		–	–	2	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}_1=V_{IH}$, $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}		–	–	2	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}_1=V_{IL}$, $CS_2=V_{IH}$, $I_{I/O}$=0mA		–	30	50	mA
I_{CC1}	Average Operating Current	Min. Duty Cycle=100%, $\overline{CS}_1=V_{IL}$, $CS_2=V_{IH}$		–	40	70	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$		–	1	3	mA
I_{SB1}[2]		$\overline{CS}_1 \geq V_{CC}-0.2V$, $CS_2 \leq 0.2V$ or $\geq V_{CC}-0.2V$		–	20	2000	μA
			L	–	2	100	
I_{SB2}[2]		$\overline{CS}_1 \leq 0.2V$ or $\geq V_{CC}-0.2V$, $CS_2 \leq 0.2V$		–	20	2000	μA
			L	–	2	100	
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH}=−1.0mA		2.4	–	–	V

NOTES :
1. Typical limits are at V_{CC}=5.0V, T_A=25°C and specified loading
2. V_{IL} min=−0.5V

AC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A= 0°C to 70°C)

READ CYCLE

SYMBOL	PARAMETER		HY6264-70 MIN.	HY6264-70 MAX.	HY6264-85 MIN.	HY6264-85 MAX.	HY6264-10 MIN.	HY6264-10 MAX.	HY6264-12 MIN.	HY6264-12 MAX.	HY6264-15 MIN.	HY6264-15 MAX.	UNIT
t_{RC}	Read Cycle Time		70	–	85	–	100	–	120	–	150	–	ns
t_{AA}	Address Access Time		–	70	–	85	–	100	–	120	–	150	ns
t_{ACS1}	Chip Select Access Time	$\overline{CS}_1$	–	70	–	85	–	100	–	120	–	150	ns
t_{ACS2}		CS_2	–	70	–	85	–	100	–	120	–	150	ns
t_{OE}	Output Enable to Output Valid		–	45	–	50	–	55	–	60	–	70	ns
t_{CLZ1}	Chip Select to Output in Low-Z	$\overline{CS}_1$	10	–	10	–	10	–	10	–	15	–	ns
t_{CLZ2}		CS_2	10	–	10	–	10	–	10	–	15	–	ns
t_{OLZ}	Output Enable to Output in Low-Z		5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ1}	Chip Deselect to Output in High-Z	$\overline{CS}_1$	0	30	0	35	0	35	0	40	0	50	ns
t_{CHZ2}		CS_2	0	30	0	35	0	35	0	40	0	50	ns
t_{OHZ}	Output Disable to Output in High-Z		0	30	0	35	0	35	0	40	0	50	ns
t_{OH}	Output Hold from Address Change		10	–	10	–	10	–	10	–	15	–	ns

WRITE CYCLE

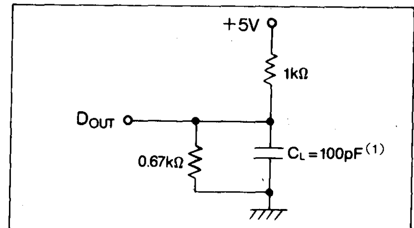
SYMBOL	PARAMETER		HY6264-70		HY6264-85		HY6264-10		HY6264-12		HY6264-15		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time		70	–	85	–	100	–	120	–	150	–	ns
t_{CW}	Chip Select to End of Write		55	–	60	–	70	–	85	–	100	–	ns
t_{AS}	Address Setup Time		0	–	0	–	0	–	0	–	0	–	ns
t_{AW}	Address Valid to End of Write		60	–	70	–	80	–	85	–	100	–	ns
t_{WP}	Write Pulse Width		50	–	55	–	60	–	70	–	90	–	ns
t_{WR1}	Write Recovery Time	$\overline{CS_1}$,$\overline{WE}$	5	–	5	–	5	–	10	–	10	–	ns
t_{WR2}		CS_2	5	–	10	–	10	–	15	–	15	–	ns
t_{WHZ}	Write to Output in High-Z		0	30	0	35	0	35	0	40	0	50	ns
t_{DW}	Data to Write Time Overlap		30	–	35	–	40	–	50	–	60	–	ns
t_{DH}	Data Hold from Write Time		0	–	0	–	0	–	0	–	0	–	ns
t_{OHZ}	Output Enable to Output in High-Z		0	30	0	35	0	35	0	40	0	50	ns
t_{OW}	Output Active from End of Write		5	–	5	–	5	–	5	–	10	–	ns

AC TEST CONDITIONS

(T_A=0°C to 70°C)

Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V

OUTPUT LOAD



NOTE :
1. Including scope and the jig

CAPACITANCE[1]

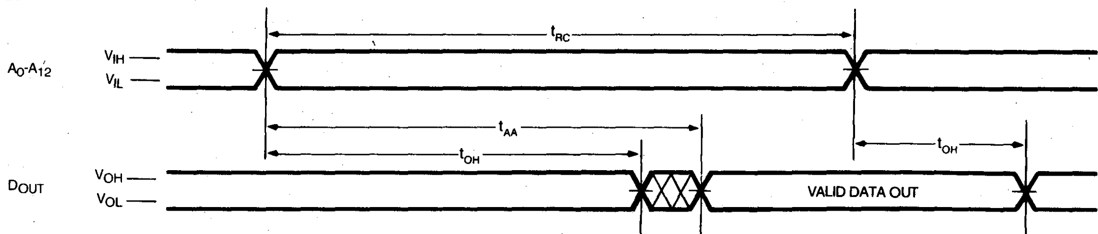
(T_A=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

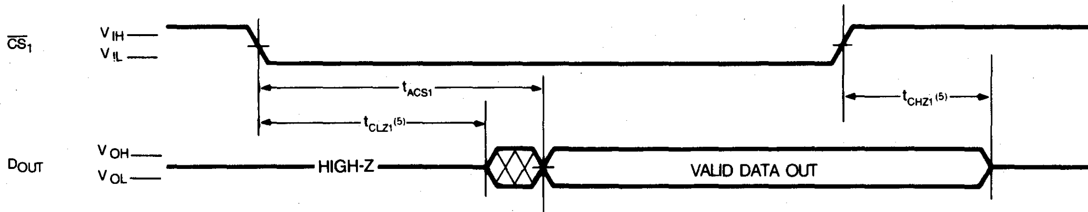
NOTE :
1. This parameter is sampled and not 100% tested.

TIMING DIAGRAMS

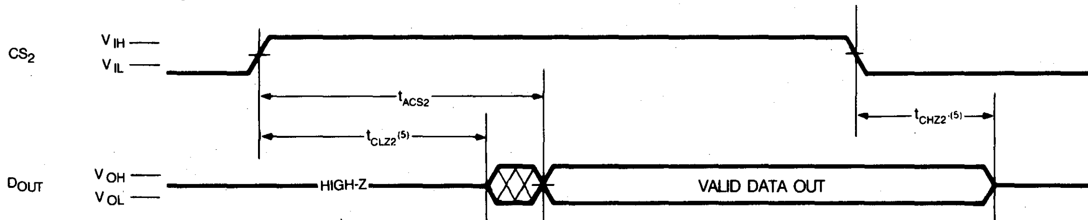
READ CYCLE 1[1,2,4]



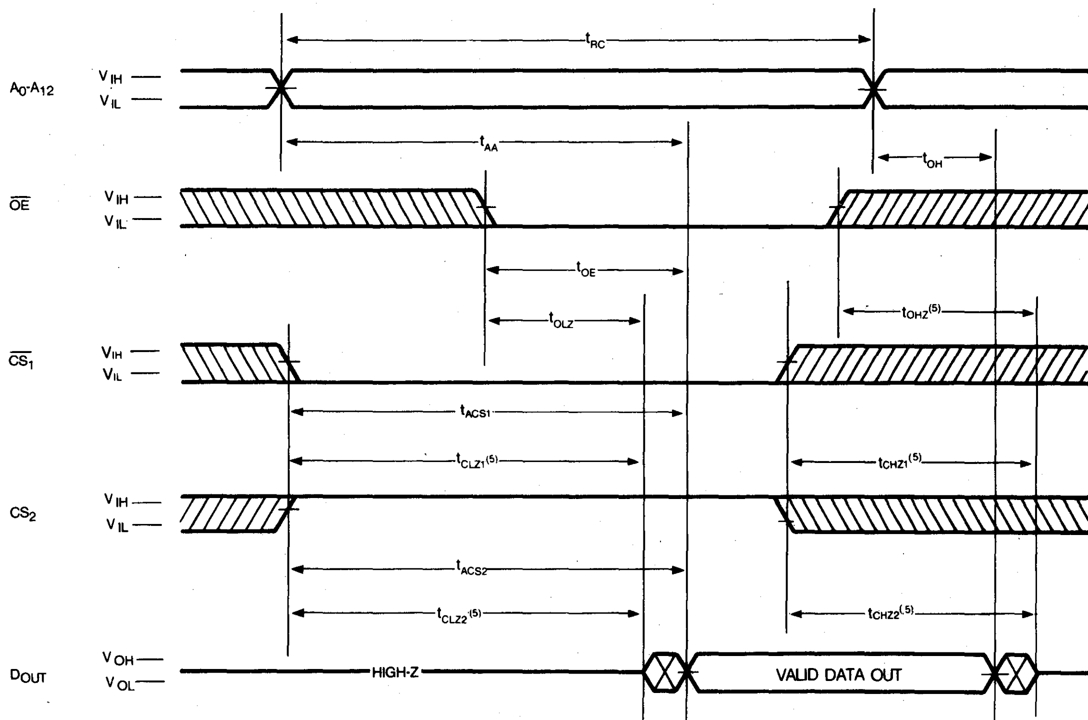
READ CYCLE 2[1,3,4,6]



READ CYCLE 3[1,4,7]



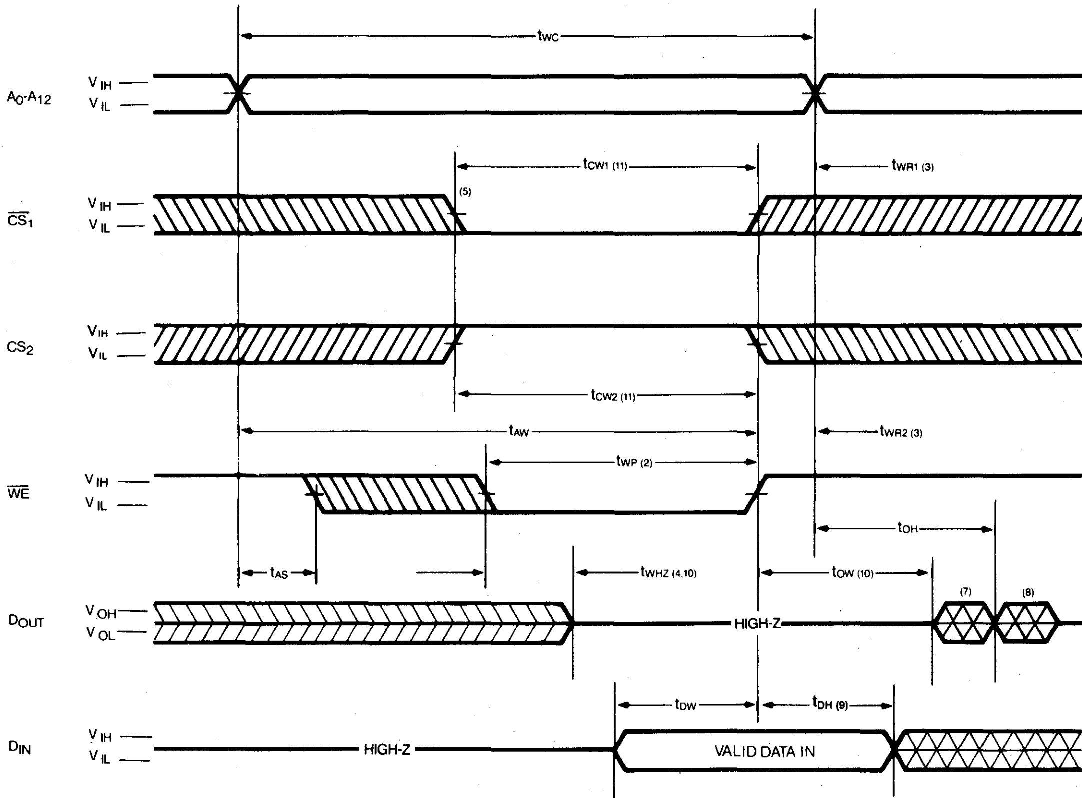
READ CYCLE 4[1,2]



NOTES :
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{CS_1}=V_{IL}$ and $CS_2=V_{IH}$.
3. Addresses are valid prior to or coincident with $\overline{CS_1}$ transition low.
4. $\overline{OE}=V_{IL}$.
5. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
6. CS_2 is high.
7. $\overline{CS_1}$ is low.

WRITE CYCLE 1[1]

WRITE CYCLE 2(1,6)



NOTES :

1. $\overline{WE}$ must be high during address transitions.
2. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$, high CS_2 and low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in output state so that the input signals of opposite phase to the output must not be applied.
5. If the $\overline{CS_1}$ low transition or the CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low($\overline{OE}=V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the output must not be applied to them.
10. Transition is measured ± 500mV from steady state.
11. t_{CW} is measured from the later of $\overline{CS_1}$ going low or CS_2 going high to the end of write.

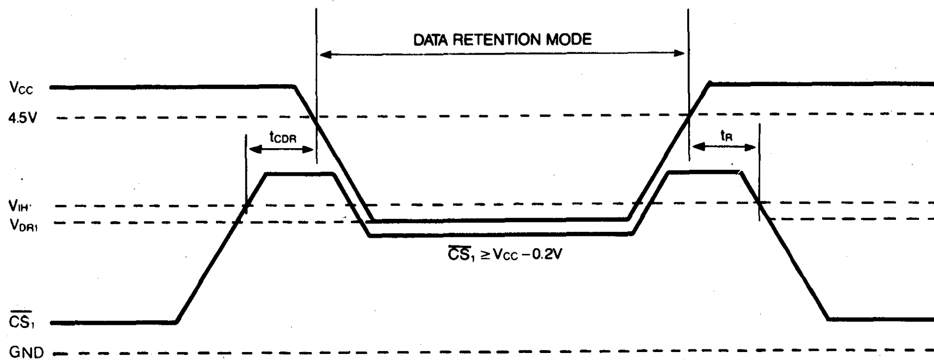
DATA RETENTION CHARACTERISTICS[1]

(T_A=0°C to 70°C)

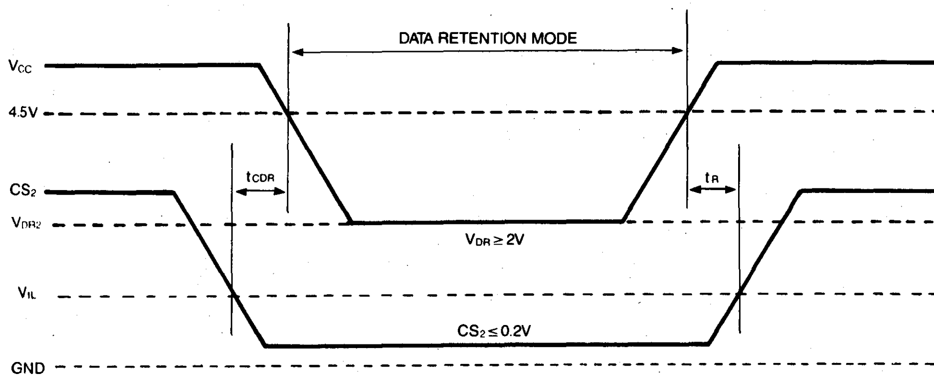
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.[2]	MAX.	UNIT
V_{DR1}	Data Retention Supply Voltage	$\overline{CS_1} \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ or $CS_2 \leq 0.2V$	2.0	–	–	V
V_{DR2}		$CS_2 \leq 0.2V$, $\overline{CS_1} \geq V_{CC}-0.2V$ or $\overline{CS_1} \leq 0.2V$	2.0	–	–	V
I_{CCDR1}	Data Retention Current	V_{CC}=3V, V_{IN}= 0V to V_{CC} $\overline{CS_1} \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ or $CS_2 \leq 0.2V$	–	2	50	μA
I_{CCDR2}		V_{CC}=3V, V_{IN}= 0V to V_{CC} $CS_2 \leq 0.2V$, $\overline{CS_1} \geq V_{CC}-0.2V$ or $\overline{CS_1} \leq 0.2V$	–	2	50	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram	0	–	–	ns
t_R	Operation Recovery Time		t_{RC}[3]	–	–	ns

NOTES :
1. These characteristics are guaranteed only for L-version
2. T_A= 25°C
3. t_{RC}=Read Cycle Time

DATA RETENTION TIMING DIAGRAM 1 ($\overline{CS_1}$ Controlled)

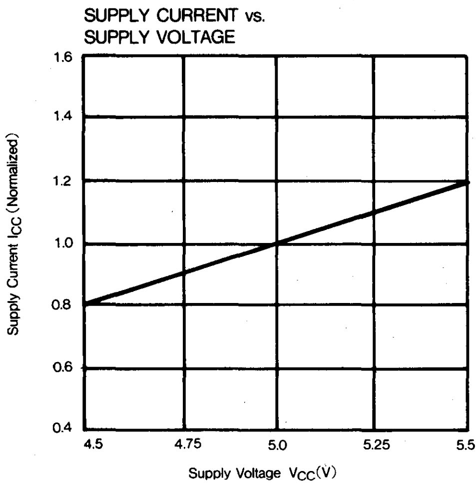


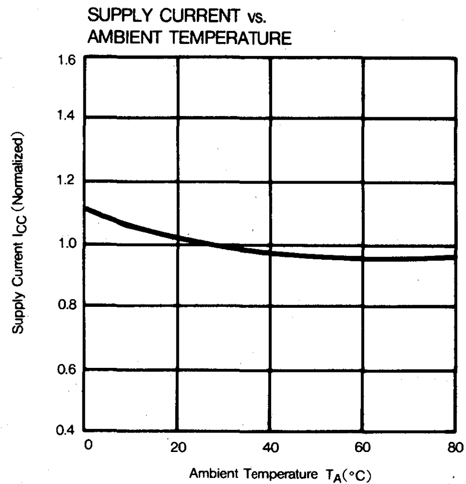
DATA RETENTION TIMING DIAGRAM 2 ($\overline{CS_2}$ Controlled)

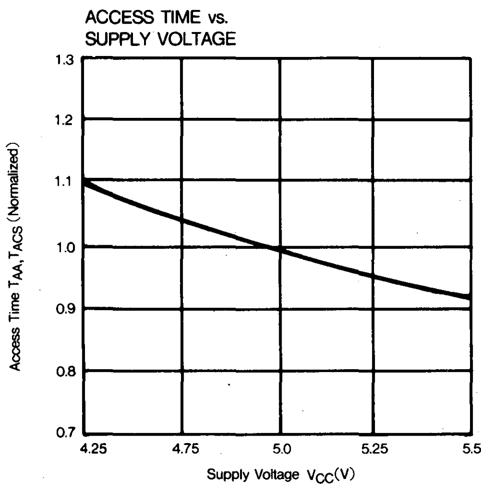


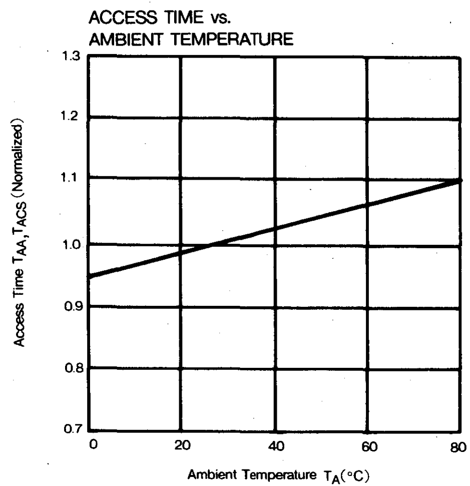
ELECTRICAL CHARACTERISTIC CURVES

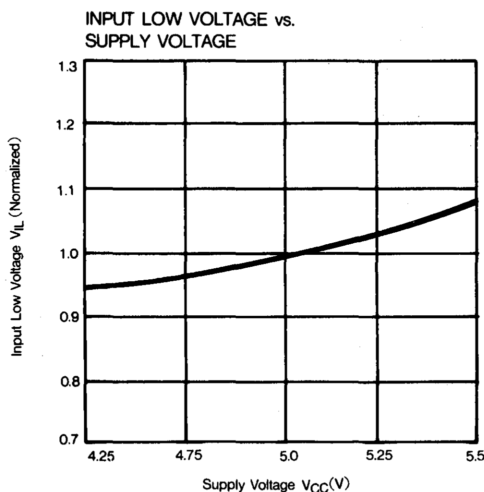
(V_{CC}=5V, T_A=25°C, unless otherwise noted)

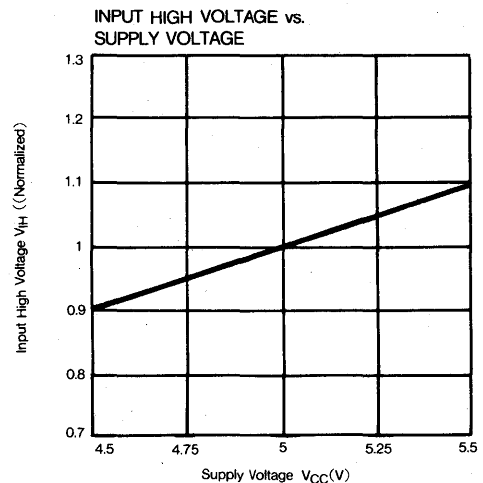


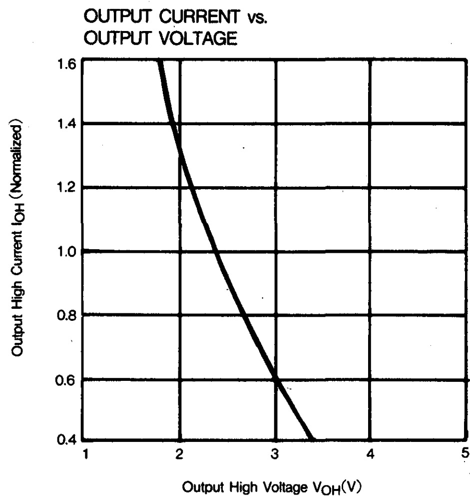


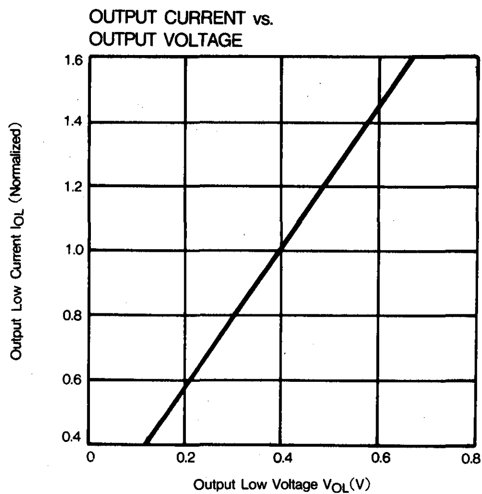


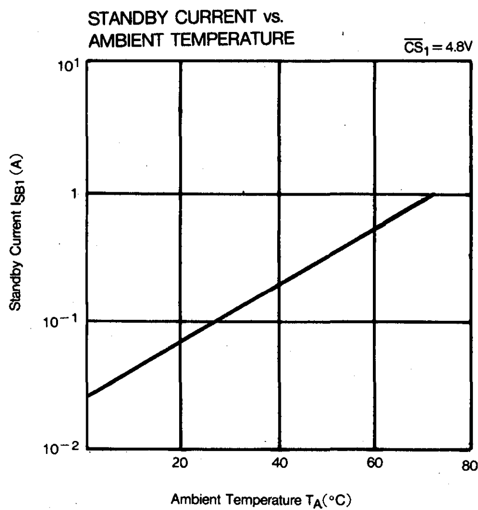


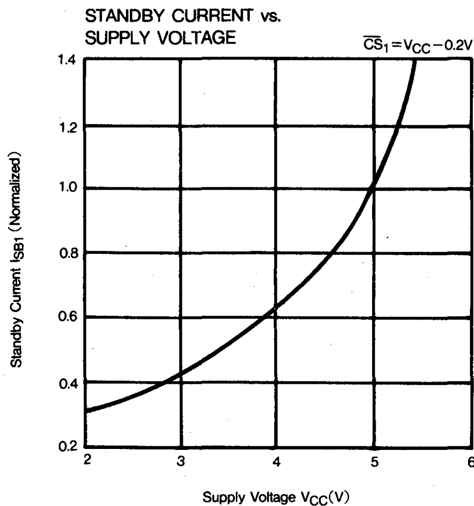





OUTPUT CURRENT vs.
OUTPUT VOLTAGE
Output High Current IOH (Normalized)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
1
2
3
4
5
Output High Voltage VOH(V)

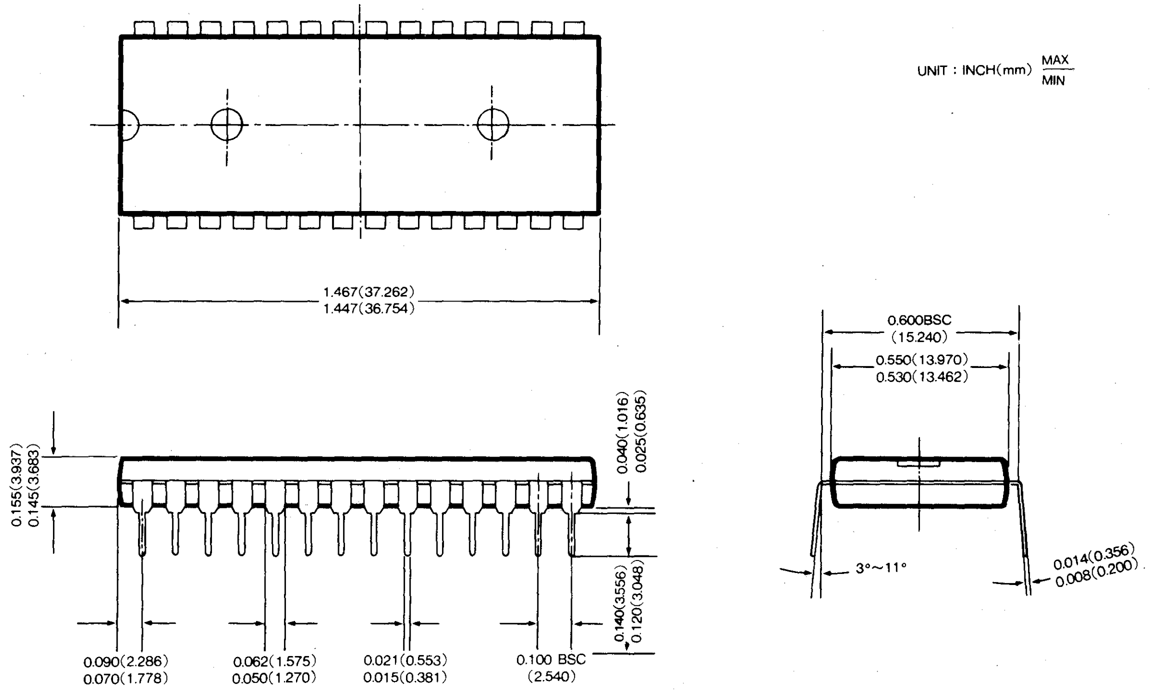

OUTPUT CURRENT vs.
OUTPUT VOLTAGE
Output Low Current IOL (Normalized)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0
0.2
0.4
0.6
0.8
Output Low Voltage VOL(V)


STANDBY CURRENT vs.
AMBIENT TEMPERATURE
CS1 = 4.8V
Standby Current ISB1 (A)
10^1
1
10^-1
10^-2
20
40
60
80
Ambient Temperature TA(°C)

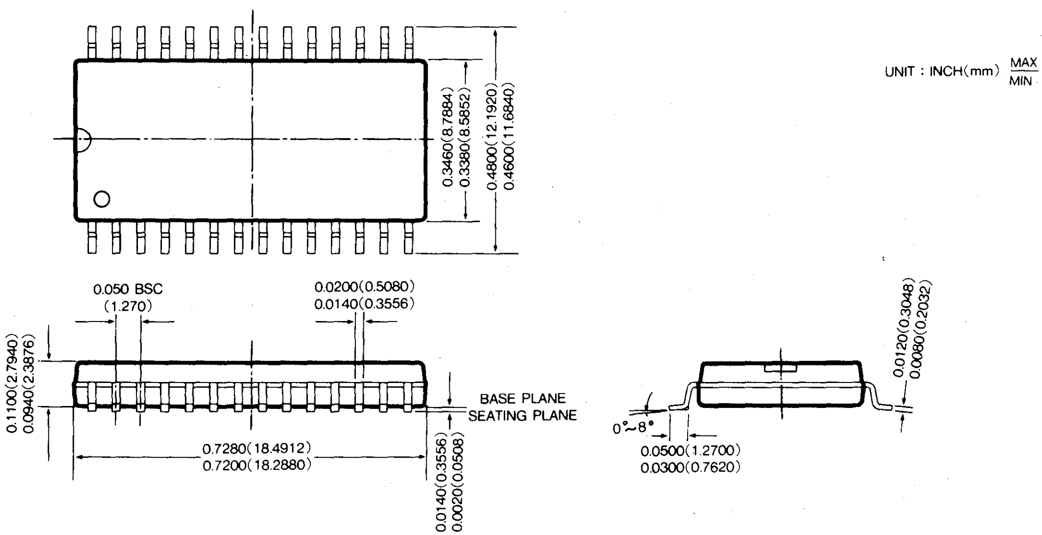

STANDBY CURRENT vs.
SUPPLY VOLTAGE
CS1 = VCC − 0.2V
Standby Current ISB1 (Normalized)
1.4
1.2
1.0
0.8
0.6
0.4
0.2
2
3
4
5
6
Supply Voltage VCC(V)

PACKAGE INFORMATION

• 28 PIN PLASTIC DUAL IN LINE PACKAGE−600MIL



• 28 PIN SMALL OUTLINE PACKAGE−330MIL



5

MEMO

•HYUNDAI SEMICONDUCTOR

HY6264A

8K×8-Bit CMOS SRAM

M261201B-MAY92

DESCRIPTION

The HY6264A is a high speed, low power 8,192 words by 8-bit CMOS static RAM fabricated using a twin tub CMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 70ns.

The HY6264A has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt.

Using CMOS technology, supply voltage from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY6264A family.

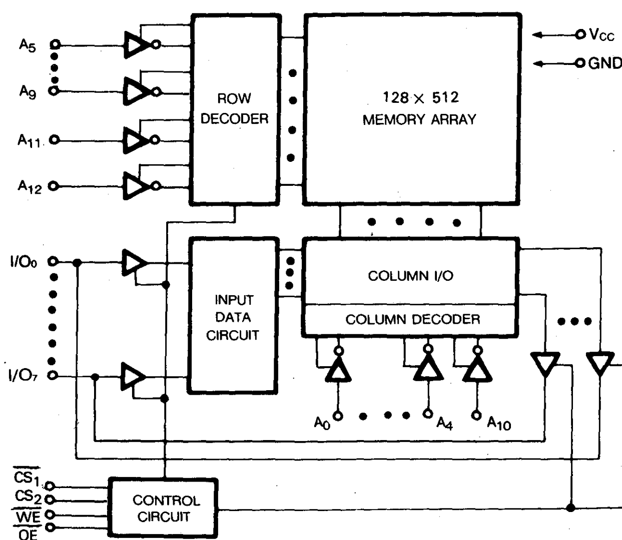
FEATURES

- High speed — 70/85/100/120/150ns (max.)
- Low power consumption
  - 200 mW typical operating
  - 10 μW typical standby (L/LL-version)
- Battery back up (L/LL-version)
  - 2 volt data retention
- Fully static operation
  - No clock or refresh required
- All inputs and outputs directly TTL compatible
- Tri-state output
- High reliability 28 pin 600 mil P-DIP and 330 mil SOP

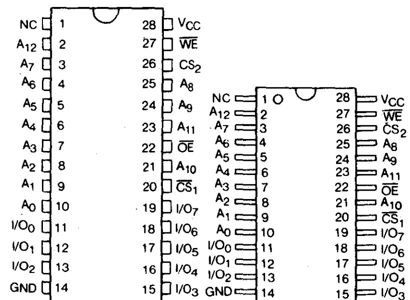
		HY6264A-70	HY6264A-85	HY6264A-10	HY6264A-12	HY6264A-15
Maximum Access Time(ns)		70	85	100	120	150
Maximum Operating Current(mA)		50	50	50	50	50
Maximum Standby Current(mA)		2	2	2	2	2
	L	0.1	0.1	0.1	0.1	0.1
	LL	0.05	0.05	0.05	0.05	0.05

5

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_{12}	ADDRESS INPUT
I/O_0-I/O_7	DATA INPUT/OUTPUT
$\overline{CS_1}$	CHIP SELECT ONE
CS_2	CHIP SELECT TWO
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
V_{cc}	POWER
GND	GROUND

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}, V_{IN}, $V_{I/O}$	Power Supply, Input, Input/Output Voltage	−0.5[2] to 7.0	V
T_{BIAS}	Temperature Under Bias	−10 to 125	°C
T_{STG}	Storage Temperature	−65 to 150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA

NOTES :
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. −3.5V for 20ns pulse.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5[1]	0	0.8	V

NOTES :
1. −3.5V for 20ns pulse.

TRUTH TABLE

MODE	$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	I/O OPERATION
Standby	H	X	X	X	High-Z
	X	L	X	X	High-Z
Output Disabled	L	H	H	H	High-Z
Read	L	H	H	L	D_{OUT}
Write	L	H	L	X	D_{IN}

DC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS		HY6264A MIN.	TYP.[1]	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{IN}=GND to V_{CC}		–	–	1	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}_1=V_{IH}$, $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$, $V_{I/O}$=GND to V_{CC}		–	–	1	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}_1=V_{IL}$, $CS_2=V_{IH}$, $I_{I/O}$=0mA		–	7	15	mA
I_{CC1}	Average Operating Current	$\overline{CS}_1=V_{IL}$, $CS_2=V_{IH}$, Min, Duty Cycle=100%.	70	–	30	50	mA
			85	–	27	50	mA
			100	–	24	50	mA
			120	–	21	50	mA
			150	–	18	50	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$		–	0.4	2	mA
I_{SB1}[2]		$\overline{CS}_1 \geq V_{CC}-0.2V$, $CS_2 \leq 0.2V$ or $\geq V_{CC}-0.2V$		–	20	1000	μA
			L	–	2	100	
			LL	–	2	50	
I_{SB2}		$\overline{CS}_1 \leq 0.2V$ or $\geq V_{CC}-0.2V$, $CS_2 \leq 0.2V$		–	20	1000	μA
			L	–	2	100	
			LL	–	2	50	
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH}=−1.0mA		2.4	–	–	V

NOTES :
1. Typical values are at V_{CC}=5V, T_A=25°C and specified loading.
2. V_{IL} min=−0.5V

5

AC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A= 0°C to 70°C)

READ CYCLE

SYMBOL	PARAMETER		HY6264A-70 MIN.	MAX.	HY6264A-85 MIN.	MAX.	HY6264A-10 MIN.	MAX.	HY6264A-12 MIN.	MAX.	HY6264A-15 MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time		70	–	85	–	100	–	120	–	150	–	ns
t_{AA}	Address Access Time		–	70	–	85	–	100	–	120	–	150	ns
t_{ACS1}	Chip Select Access Time	$\overline{CS}_1$	–	70	–	85	–	100	–	120	–	150	ns
t_{ACS2}		CS_2	–	70	–	85	–	100	–	120	–	150	ns
t_{OE}	Output Enable to Output Valid		–	45	–	50	–	55	–	60	–	70	ns
t_{CLZ1}	Chip Select to Output in Low-Z	$\overline{CS}_1$	10	–	10	–	10	–	10	–	15	–	ns
t_{CLZ2}		CS_2	10	–	10	–	10	–	10	–	15	–	ns
t_{OLZ}	Output Enable to Output in Low-Z		5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ1}	Chip Deselect to Output in High-Z	$\overline{CS}_1$	0	30	0	35	0	35	0	40	0	50	ns
t_{CHZ2}		CS_2	0	30	0	35	0	35	0	40	0	50	ns
t_{OHZ}	Output Disable to Output in High-Z		0	30	0	35	0	35	0	40	0	50	ns
t_{OH}	Output Hold from Address Change		5	–	5	–	10	–	10	–	10	–	ns

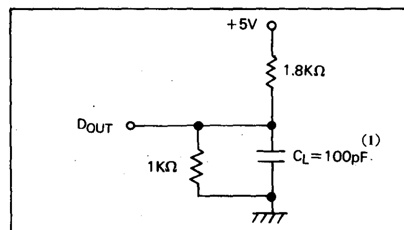
WRITE CYCLE

SYMBOL	PARAMETER		HY6264A-70		HY6264A-85		HY6264A-10		HY6264A-12		HY6264A-15		UNIT
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time		70	–	85	–	100	–	120	–	150	–	ns
t_{CW}	Chip Select to End of Write		55	–	60	–	70	–	85	–	100	–	ns
t_{AS}	Address Setup Time		0	–	0	–	0	–	0	–	0	–	ns
t_{AW}	Address Valid to End of Write		55	–	60	–	70	–	85	–	100	–	ns
t_{WP}	Write Pulse Width		50	–	55	–	60	–	70	–	90	–	ns
t_{WR1}	Write Recovery Time	$\overline{CS_1}$,$\overline{WE}$	0	–	0	–	0	–	0	–	0	–	ns
t_{WR2}		CS_2	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}	Write to Output in High-Z		0	30	0	35	0	35	0	40	0	50	ns
t_{DW}	Data to Write Time Overlap		35	–	35	–	40	–	50	–	60	–	ns
t_{DH}	Data Hold from Write Time		0	–	0	–	0	–	0	–	0	–	ns
t_{OHZ}	Output Disable to Output in High-Z		0	30	0	35	0	35	0	40	0	50	ns
t_{OW}	Output Active from End of Write		5	–	5	–	5	–	5	–	10	–	ns

AC TEST CONDITIONS
(T_A=0°C to 70°C)

Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V

OUTPUT LOAD



NOTE :
1. Including scope and the jig.

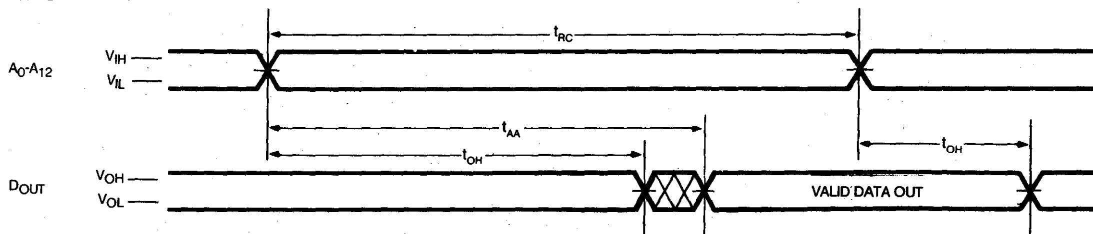
CAPACITANCE[1]
(T_A=25°C, f=1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

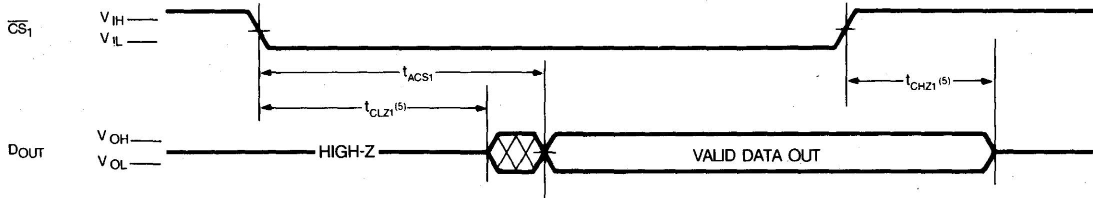
NOTE :
1. This parameter is sampled and not 100% tested.

TIMING DIAGRAMS

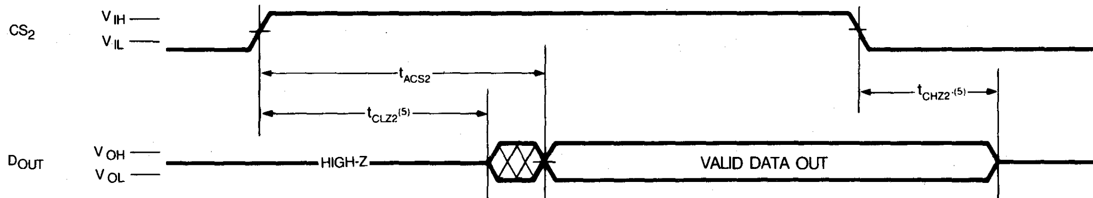
READ CYCLE 1[1,2,4]



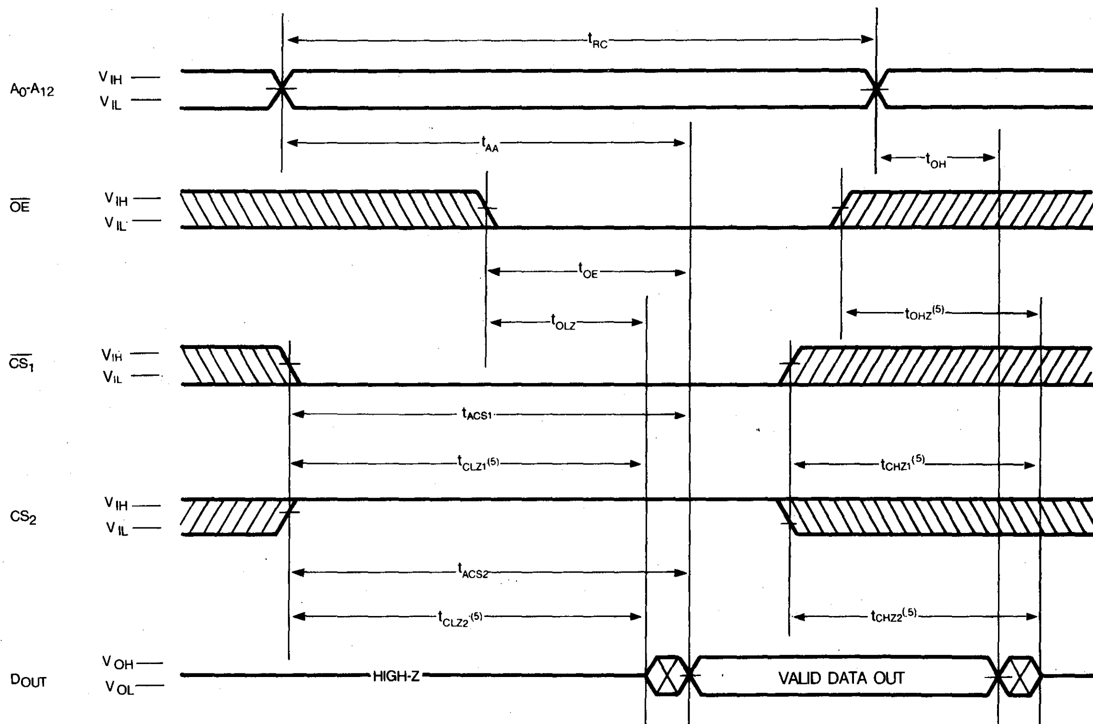
READ CYCLE 2(1,3,4,6)



READ CYCLE 3(1,4,7)



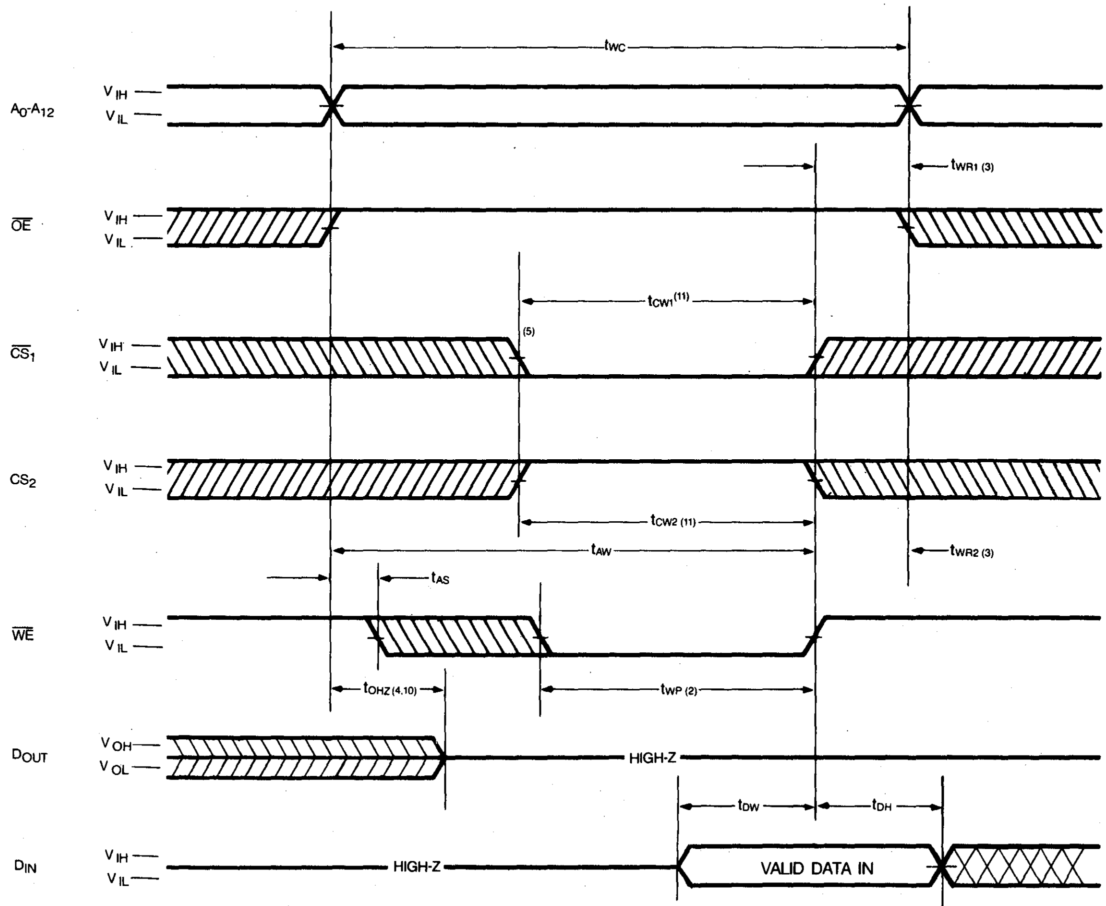
READ CYCLE 4(1,2)



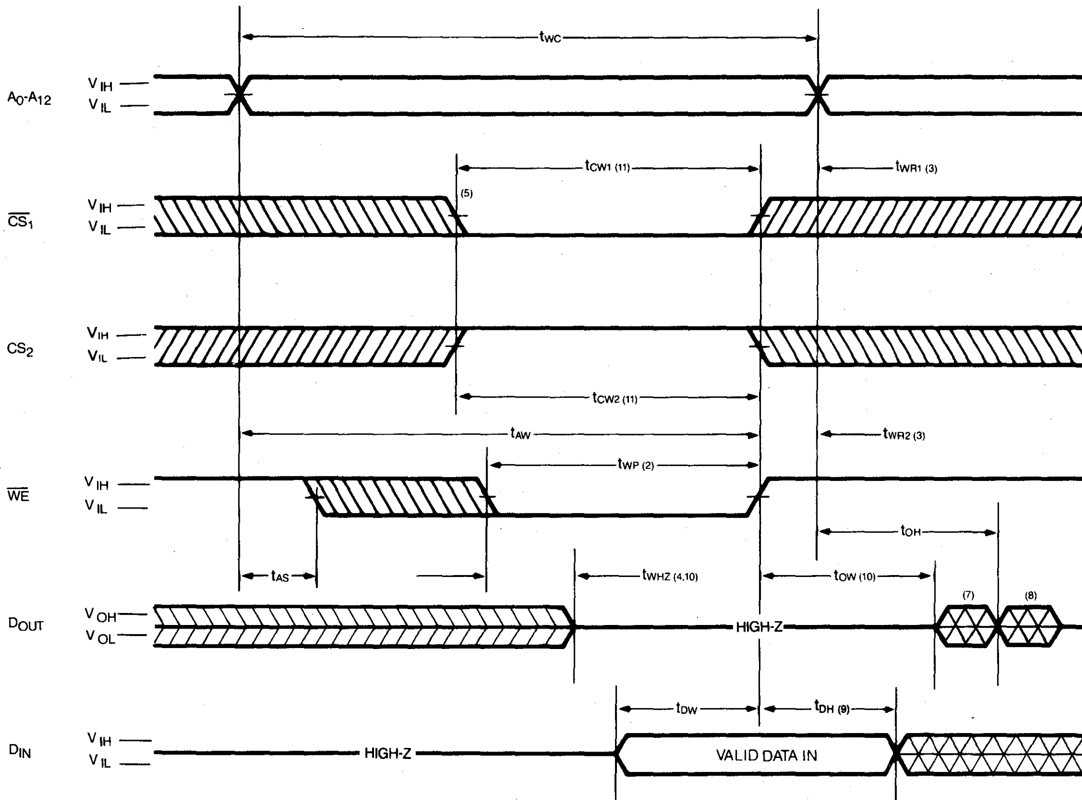
NOTES :
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected $\overline{CS_1}=V_{IL}$ and $CS_2=V_{IH}$.
3. Addresses are valid prior to or coincident with $\overline{CS_1}$ transition low.
4. $\overline{OE}=V_{IL}$.
5. Transition is measured ± 500mV from steady state. This parameter is sampled and not 100% tested.
6. CS_2 is high.
7. $\overline{CS_1}$ is low.

5

WRITE CYCLE 1[1]



WRITE CYCLE 2(1,6)



NOTES :

1. $\overline{WE}$ must be high during address transitions.
2. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$, high CS_2 and low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in output state so that the input signals of opposite phase to the output must not be applied.
5. If the $\overline{CS_1}$ low transition or the CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low($\overline{OE}=V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the output must not be applied to them.
10. Transition is measured ± 500mV from steady state.
11. t_{CW} is measured from the later of $\overline{CS_1}$ going low or CS_2 going high to the end of write.

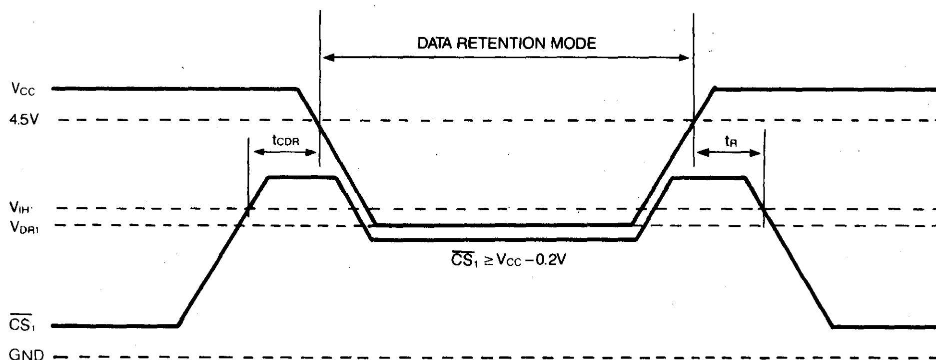
DATA RETENTION CHARACTERISTICS[1]

(T_A=0°C to 70°C)

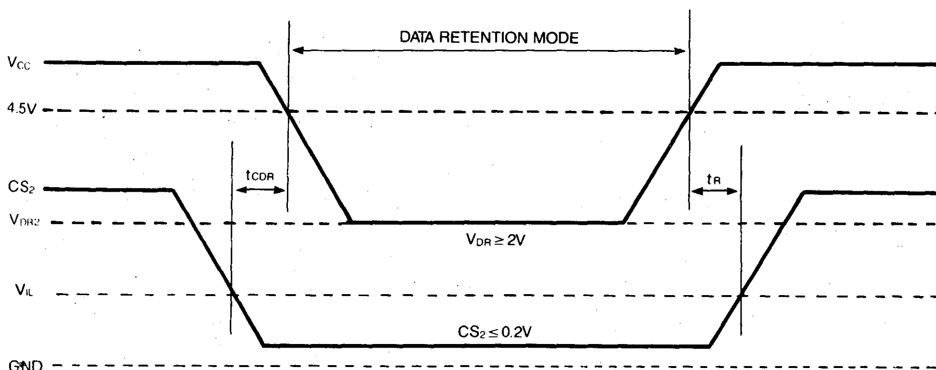
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{DR1}	Data Retention	$\overline{CS}_1 \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ or $CS_2 \leq 0.2V$		2.0	–	–	V
V_{DR2}	Supply Voltage	$CS_2 \leq 0.2V$, $\overline{CS}_1 \geq V_{CC}-0.2V$ or $\overline{CS}_1 \leq 0.2V$		2.0	–	–	V
I_{CCDR1}	Data Retention Current	V_{CC}=3V, V_{IN}= 0V to V_{CC}	L	–	1	50	μA
		$\overline{CS}_1 \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ or $CS_2 \leq 0.2V$	LL	–	1	5[2]	
I_{CCDR2}		V_{CC}=3V, V_{IN}= 0V to V_{CC}	L	–	1	50	μA
		$CS_2 \leq 0.2V$, $\overline{CS}_1 \geq V_{CC}-0.2V$ or $\overline{CS}_1 \leq 0.2V$	LL	–	1	5[2]	
t_{CDR}	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram		0	–	–	ns
t_R	Operation Recovery Time			t_{RC}[3]	–	–	ns

NOTES :
1. These characteristics are guaranteed for L and LL-version.
2. 3μA max. at T_A=0°C to 40°C
3. t_{RC}=Read Cycle Time

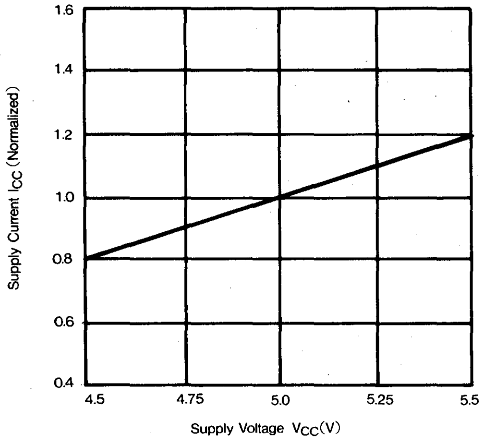
DATA RETENTION TIMING DIAGRAM 1 ($\overline{CS}_1$ Controlled)

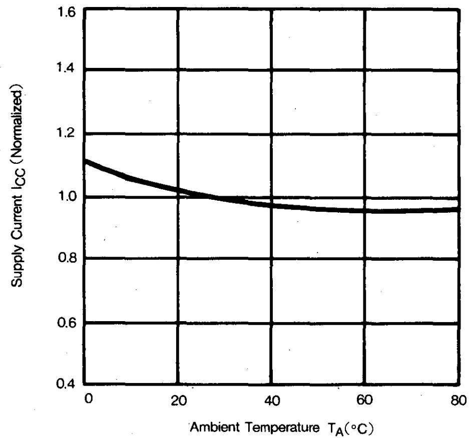


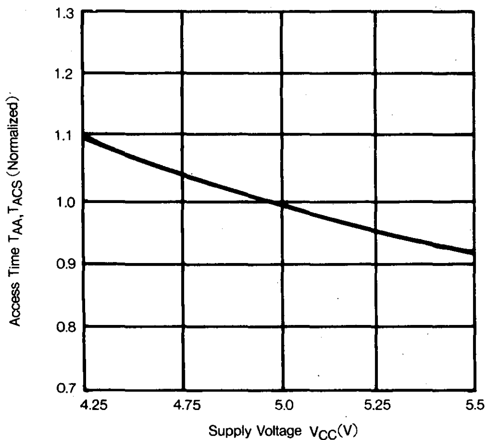
DATA RETENTION TIMING DIAGRAM 2 (CS_2 Controlled)

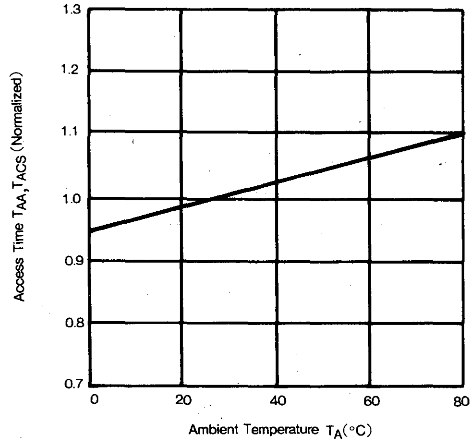


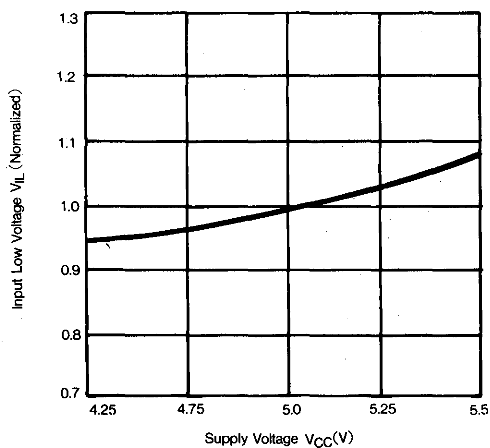
ELECTRICAL CHARACTERISTIC CURVES
(V_{CC}=5V, T_A=25°C, unless otherwise noted)

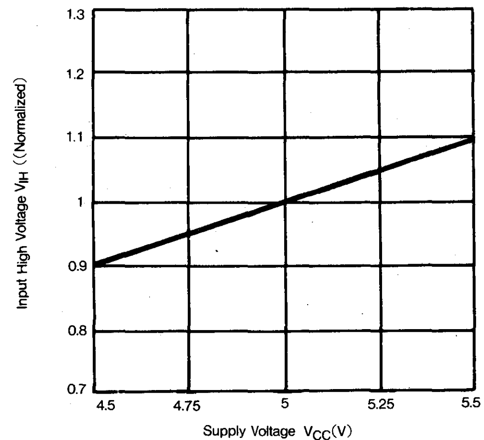












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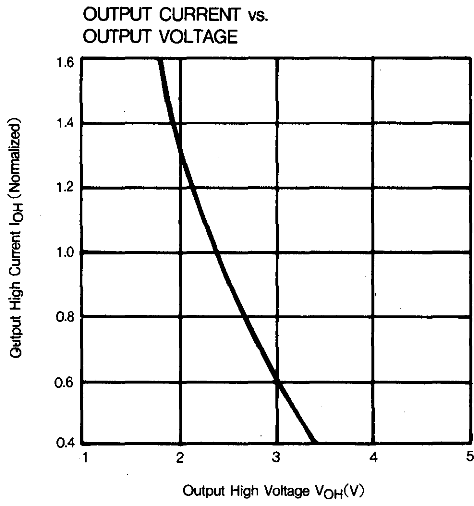
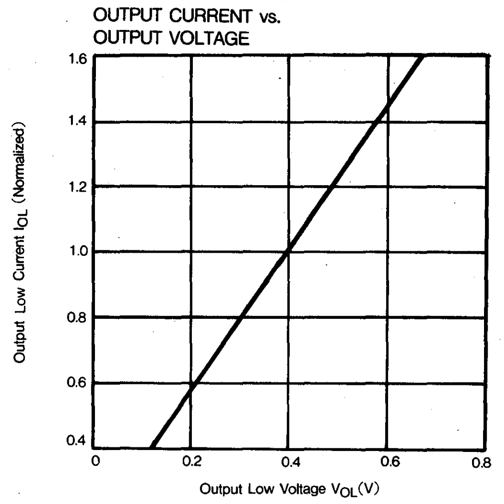
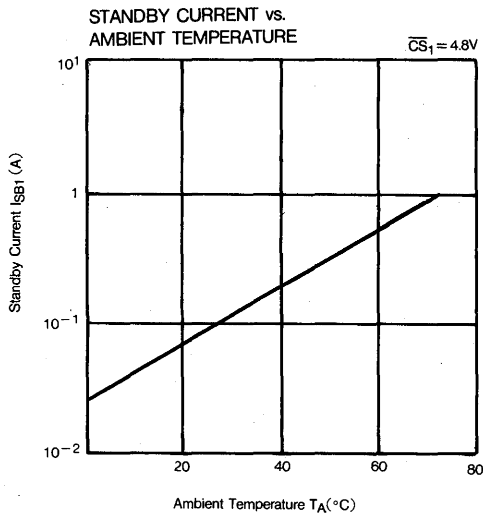
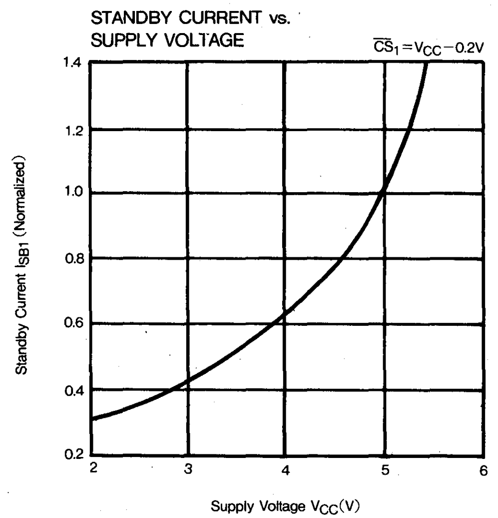

OUTPUT CURRENT vs.
OUTPUT VOLTAGE
Output High Current I_{OH} (Normalized)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
1
2
3
4
5
Output High Voltage V_{OH}(V)

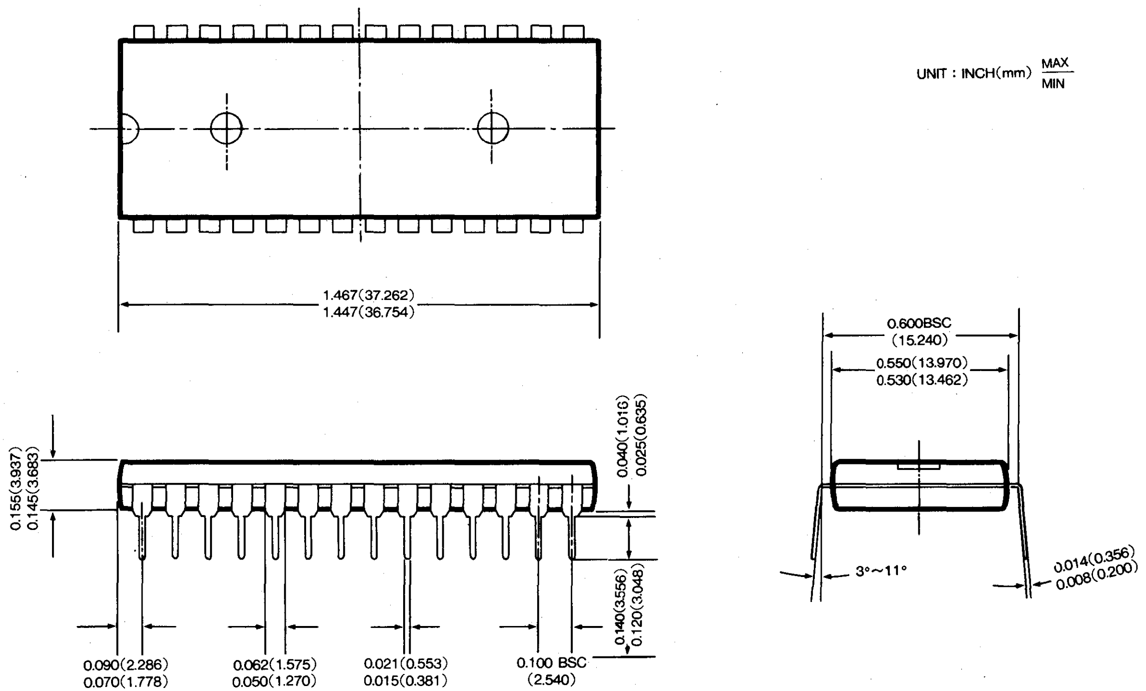

OUTPUT CURRENT vs.
OUTPUT VOLTAGE
Output Low Current I_{OL} (Normalized)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0
0.2
0.4
0.6
0.8
Output Low Voltage V_{OL}(V)


STANDBY CURRENT vs.
AMBIENT TEMPERATURE
$\overline{CS}_1$=4.8V
Standby Current I_{SB1} (A)
10^1
1
10^{-1}
10^{-2}
20
40
60
80
Ambient Temperature T_A(°C)

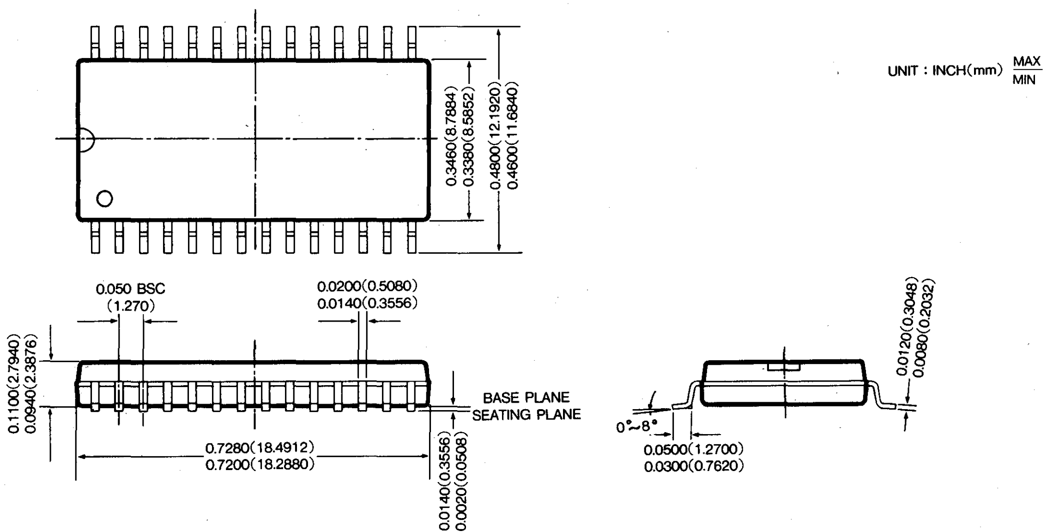

STANDBY CURRENT vs.
SUPPLY VOLTAGE
$\overline{CS}_1$=V_{CC}−0.2V
Standby Current I_{SB1} (Normalized)
1.4
1.2
1.0
0.8
0.6
0.4
0.2
2
3
4
5
6
Supply Voltage V_{CC}(V)

PACKAGE INFORMATION

- **28 PIN PLASTIC DUAL IN LINE PACKAGE-600MIL**



- **28 PIN SMALL OUTLINE PACKAGE-330MIL**



MEMO

HY62C256

32K×8-Bit CMOS SRAM

M231202B-MAY92

DESCRIPTION

The HY62C256 is a high speed low power, 32,768 words by 8-bit CMOS static RAM fabricated using HYUNDAI's high performance twin tub CMOS process. This high reliability process coupled with innovative circuit design techniques. yields maximum access time of 85ns.

The HY62C256 has a data retention mode that guarantees data will remain valid at a minimum power supply voltage of 2.0 volt.

Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY62C256 family.

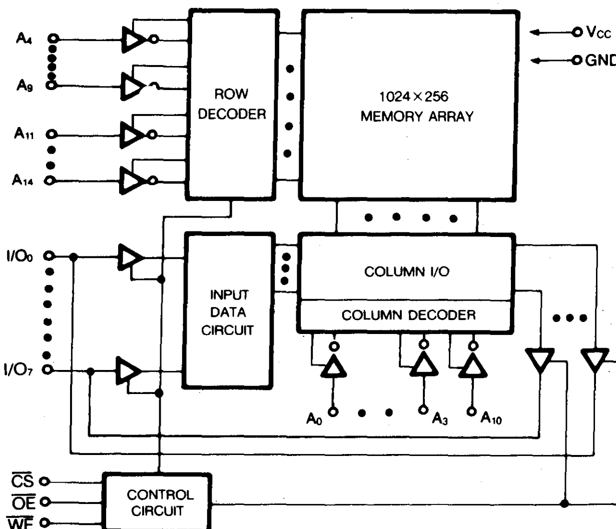
FEATURES

- High speed—85/100/120/150 ns (max.)
- Low power consumption
  - 175mW typical operating
  - 15 μW typical standby (L-version)
- Battery back up (L-version)
  - 2 volt data retention
- Fully static operation
  - No clock or refresh required
- All inputs and outputs directly TTL compatible
- Tri-state output
- High reliability 28 pin 600 mil P-DIP and 330 mil SOP

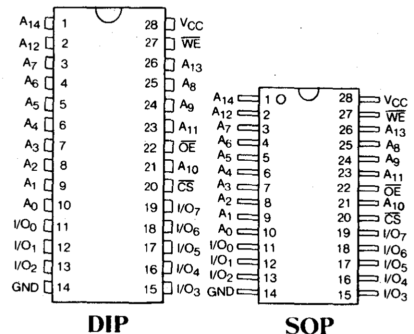
		HY62C256-85	HY62C256-10	HY62C256-12	HY62C256-15
Maximum Access Time (ns)		85	100	120	150
Maximum Average Operating Current (mA)		70	70	70	70
Maximum Standby Current (mA)		1.0	1.0	1.0	1.0
	L	0.1	0.1	0.1	0.1

5

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_{14}	ADDRESS INPUT
I/O_0-I/O_7	DATA INPUT / OUTPUT
$\overline{CS}$	CHIP SELECT
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
V_{CC}	POWER
GND	GROUND

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}, V_{IN}, $V_{I/O}$	Power Supply, Input, Input/Output Voltage	−0.5[2] to 7.0	V
T_{BIAS}	Temperature Under Bias	−10 to 125	°C
T_{STG}	Storage Temperature	−65 to 150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA

NOTES :

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended may affect reliability.
2. -3.5V for 20ns pulse.

RECOMMENDED DC OPERATING CONDITIONS

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5[1]	−	0.8	V

NOTE :

1. −3.5V for 20 ns pulse.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION
Standby	H	X	X	High-Z
output Disabled	L	H	H	High-Z
Read	L	L	H	D_{OUT}
Write	L	X	L	D_{IN}

NOTE :

1. X : H or L

DC CHARACTERISTICS
(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS		HY62C56 MIN.	TYP.[1]	MAX.	UNIT
$\vert I_{LI} \vert$	Input Leakage Current	V_{IN}=GND to V_{CC}		–	–	2	μA
$\vert I_{LO} \vert$	Output Leakage Current	$\overline{CS}=V_{IH}$, $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{I/O}$=GND to V_{CC}		–	–	2	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA		–	40	70	mA
I_{CC1}	Average Operating Current	$\overline{CS}=V_{IL}$, Min. Duty Cycle=100%		–	35	70	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}=V_{IH}$		–	–	3	mA
I_{SB1}		$\overline{CS} \geq V_{CC}-0.2V$,		–	–	1.0	mA
			L	–	3	100	μA
V_{OL}	Output Low Voltage	I_{OL}=4mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH}=−1.0mA		2.4	–	–	V

NOTE :
1. V_{CC}=5V, T_A=25°C

AC CHARACTERISTICS
(V_{CC}=5V± 10%, T_A=0°C to 70°C)

READ CYCLE

SYMBOL	PARAMETER	HY62C256-85		HY62C256-10		HY62C256-12		HY62C256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	85	–	100	–	120	–	150	–	ns
t_{AA}	Address Access Time	–	85	–	100	–	120	–	150	ns
t_{ACS}	Chip Select Access Time	–	85	–	100	–	120	–	150	ns
t_{CLZ}	Chip Selection to Output in Low-Z	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	45	–	50	–	60	–	70	ns
t_{OLZ}	Output Enable to Output in Low-Z	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Deselection to Output in High-Z	0	30	0	35	0	40	0	50	ns
t_{OHZ}	Output Disable to Output in High-Z	0	30	0	35	0	40	0	50	ns
t_{OH}	Output Hold from Address Change	5	–	10	–	10	–	10	–	ns

WRITE CYCLE

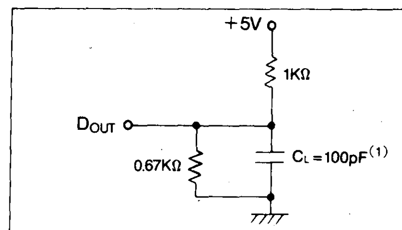
SYMBOL	PARAMETER	HY62C256-85		HY62C256-10		HY62C256-12		HY62C256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	85	–	100	–	120	–	150	–	ns
t_{CW}	Chip Selection to End of Write	75	–	80	–	85	–	100	–	ns
t_{AW}	Address Valid to End of Write	75	–	80	–	85	–	100	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	60	–	70	–	70	–	90	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{OHZ}	Output Disable to Output in High-Z	0	30	0	35	0	40	0	50	ns
t_{WHZ}	Write to Output in High-Z	0	30	0	35	0	40	0	50	ns
t_{DW}	Data to Write Time Overlap	40	–	40	–	50	–	60	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write	5	–	10	–	10	–	10	–	ns

AC TEST CONDITIONS

(T_A=0°C to 70°C)

Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V

OUTPUT LOAD



NOTE :
1. Including scope and the Jig.

CAPACITANCE

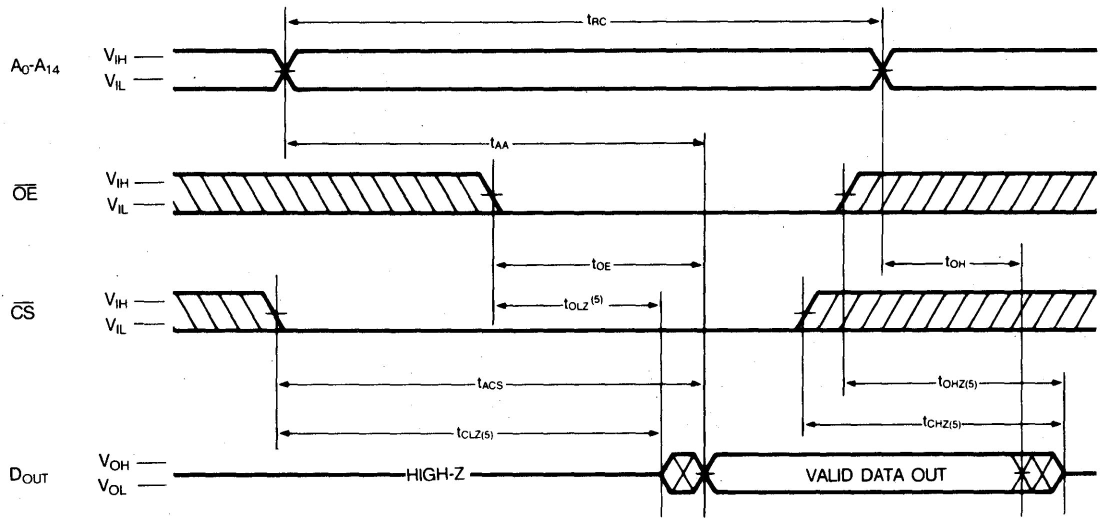
(T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	10	pF

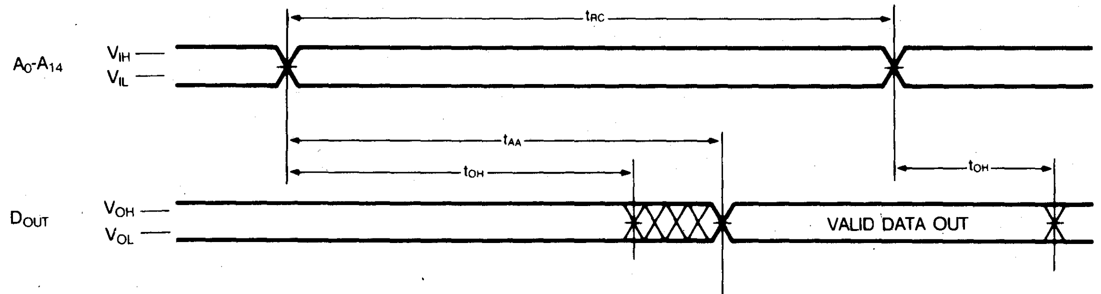
NOTE :
1. This parameter is sampled and not 100% tested.

TIMING DIAGRAMS

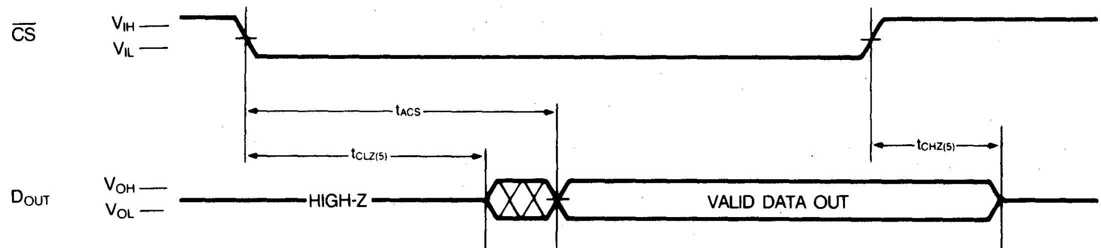
READ CYCLE 1[1]



READ CYCLE 2[1, 2, 4]

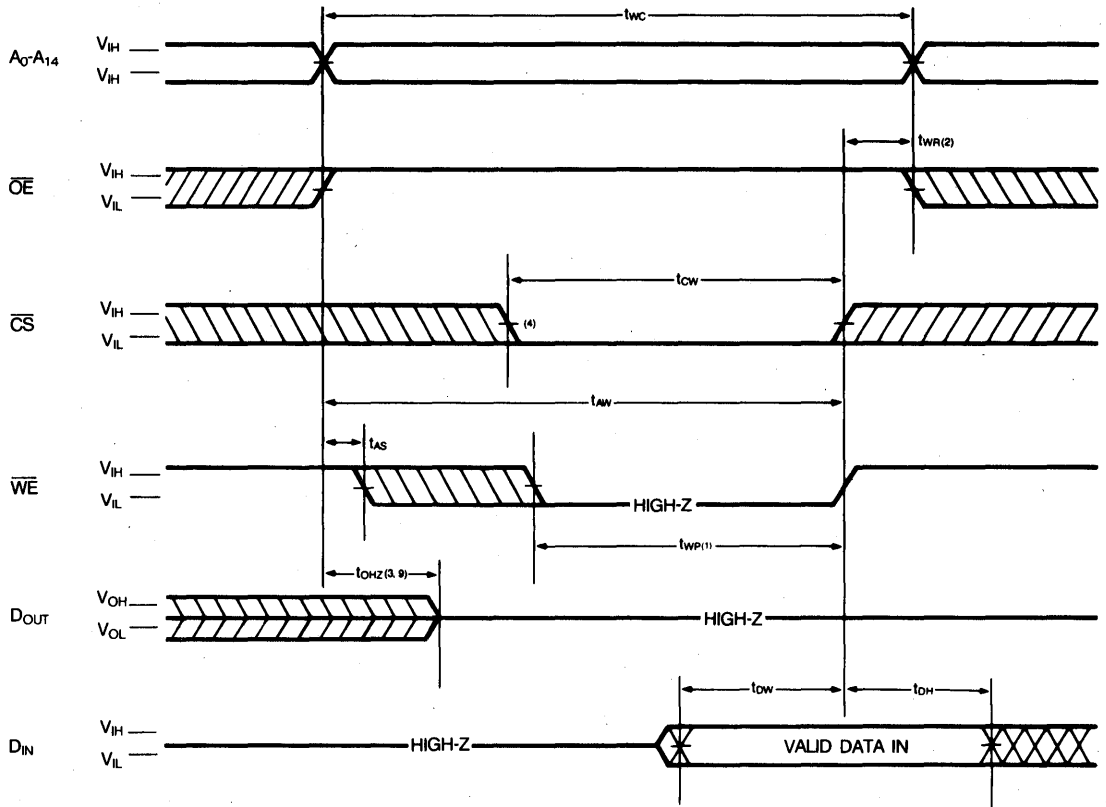


READ CYCLE 3[1, 3, 4]

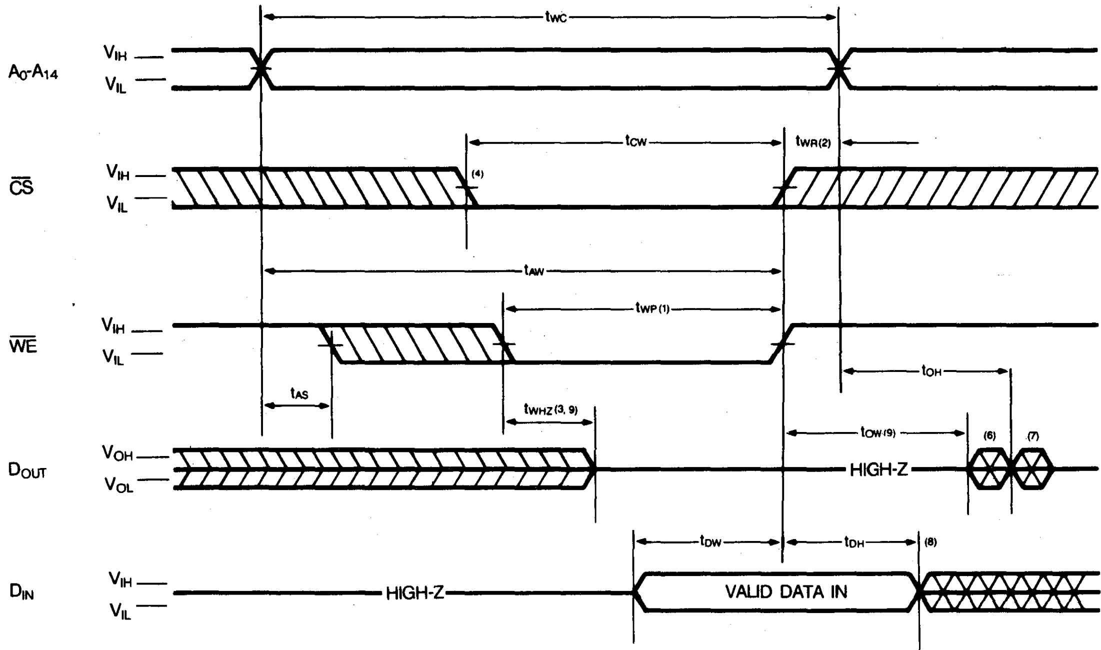


NOTES :
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}=V_{IL}$
3. Addresses are valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}=V_{IL}$
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE 1



WRITE CYCLE 2[5]



5

NOTES :
1. A write occurs during the overlap (t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high at the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE}=V_{IL}$).
6. D_{OUT} is the same phase of write data of this write cycle.
7. D_{OUT} is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

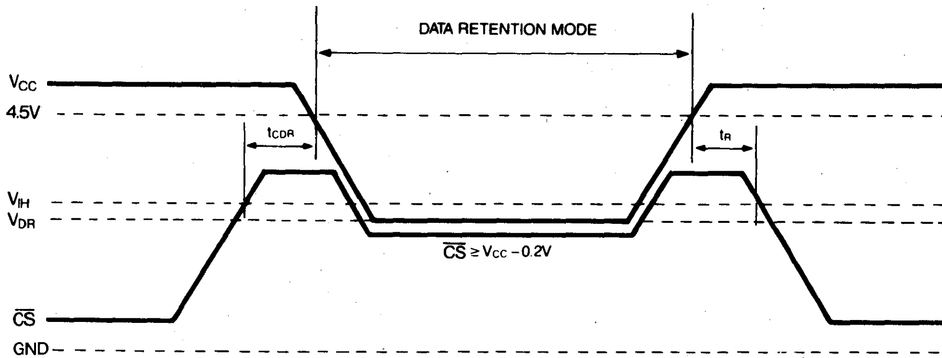
DATA RETENTION CHARACTERISTICS[1]

(T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DR}	Data Retention Supply Voltage	$V_{IN}=0$ to V_{CC}, $\overline{CS} \geq V_{CC}-0.2V$	2.0	–	–	V
I_{CCDR}	Data Retention Current	$V_{CC}=3.0V$, $V_{IN}=0$ to V_{CC}, $\overline{CS} \geq V_{CC}-0.2V$	–	2	50	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram	0	–	–	ns
t_R	Operating Recovery Time		t_{RC}[2]	–	–	ns

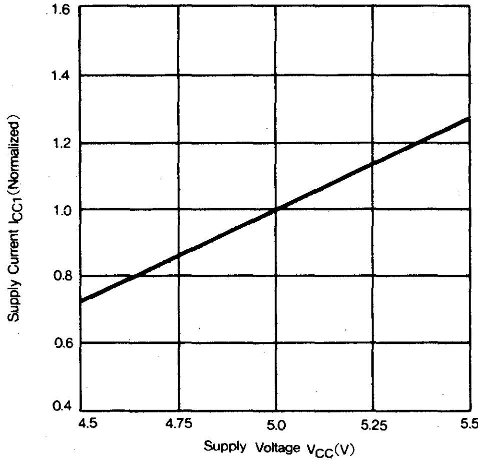
NOTES :
1. These characteristics are guaranteed for L-version.
2. t_{RC}=Read Cycle Time

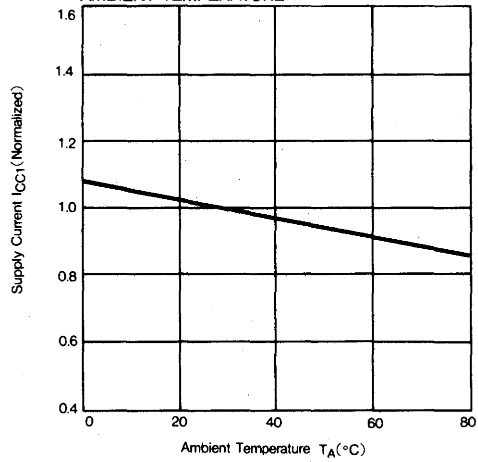
DATA RETENTION TIMING DIAGRAM

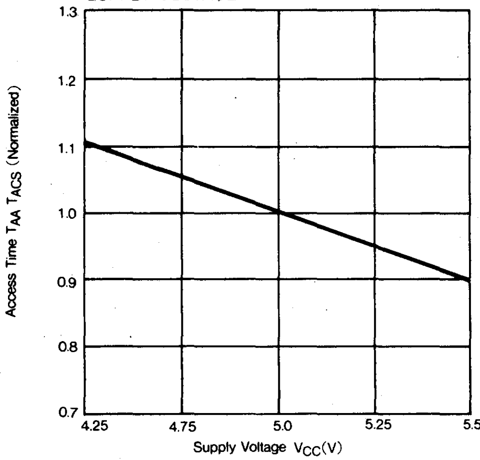


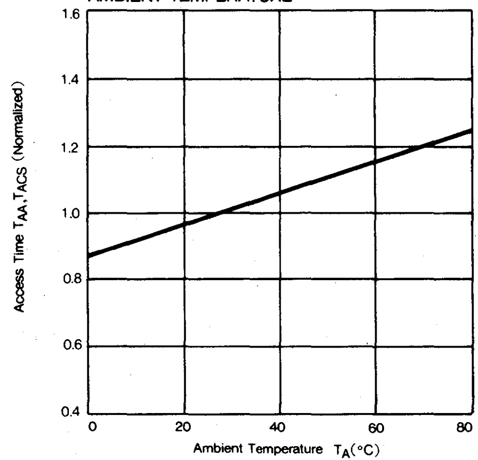
ELECTRICAL CHARACTERISTIC CURVES

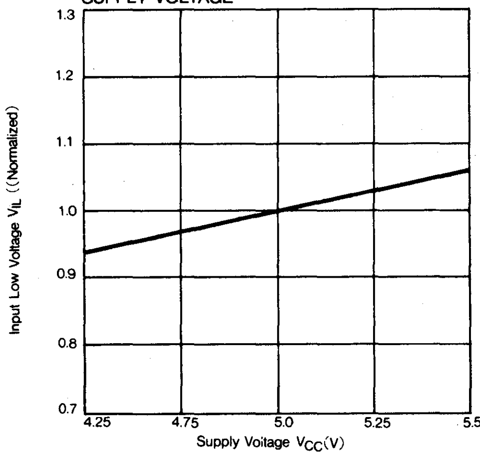
(V_{CC}=5V, T_A=25°C , unless otherwise noted)

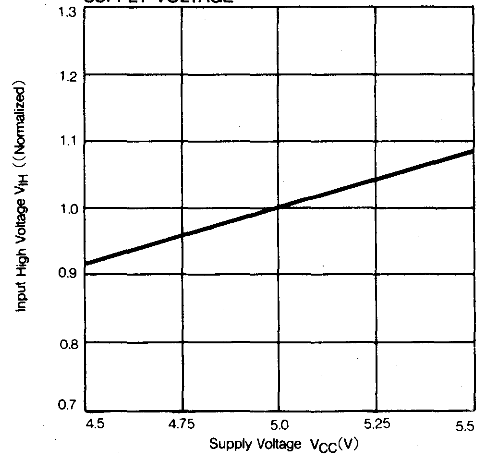


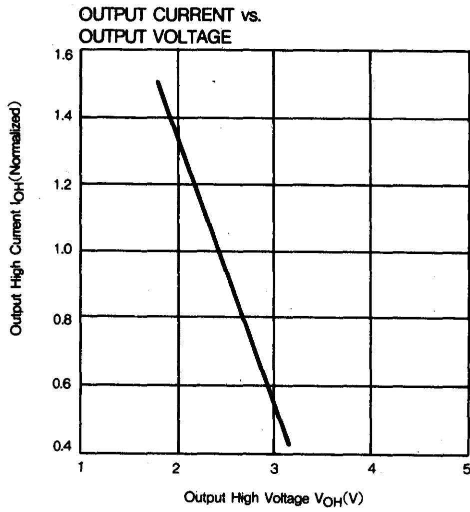


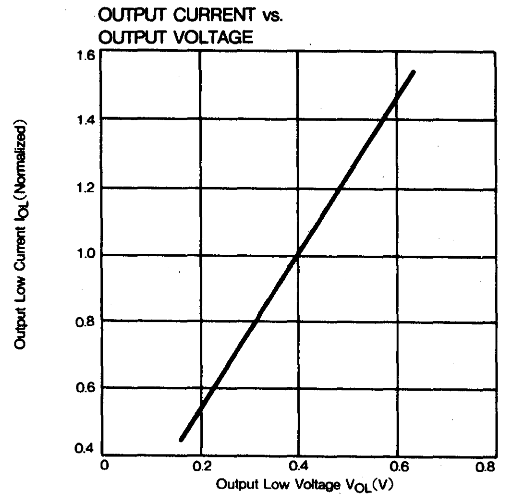


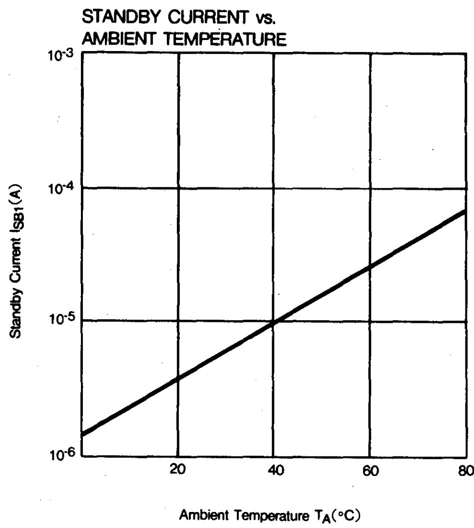


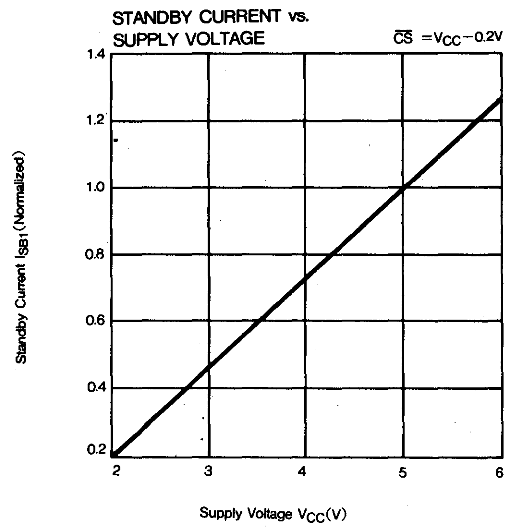





OUTPUT CURRENT vs.
OUTPUT VOLTAGE
Output High Current I_{OH}(Normalized)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
1
2
3
4
5
Output High Voltage V_{OH}(V)

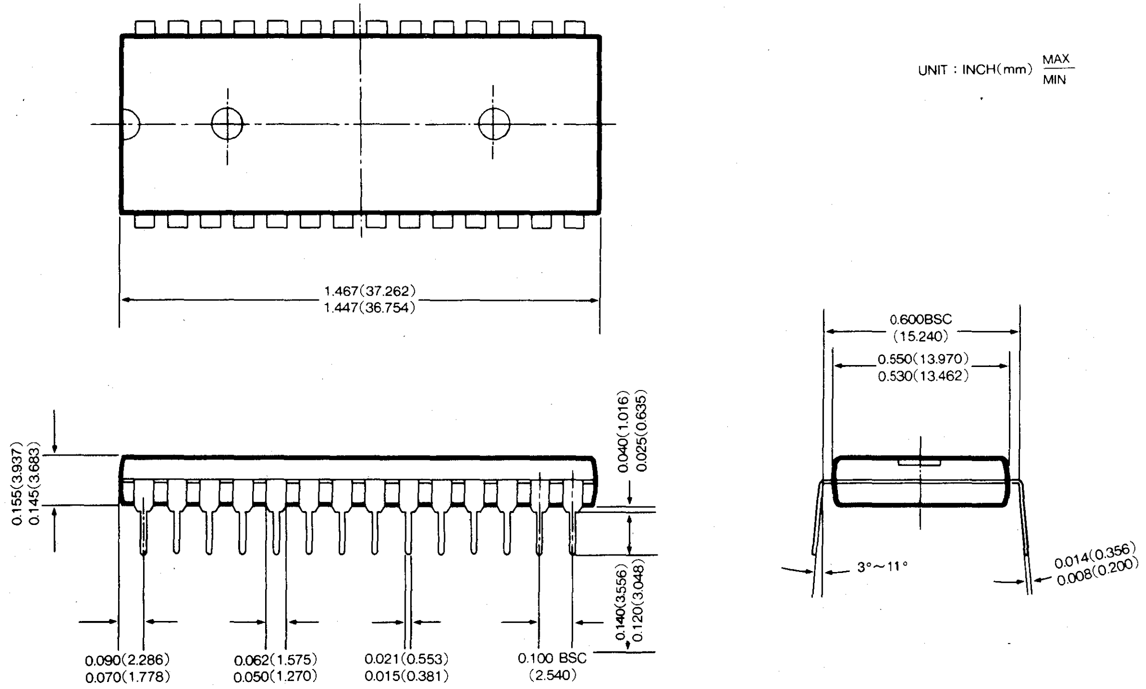

OUTPUT CURRENT vs.
OUTPUT VOLTAGE
Output Low Current I_{OL}(Normalized)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0
0.2
0.4
0.6
0.8
Output Low Voltage V_{OL}(V)


STANDBY CURRENT vs.
AMBIENT TEMPERATURE
Standby Current I_{SB1}(A)
10^{-3}
10^{-4}
10^{-5}
10^{-6}
20
40
60
80
Ambient Temperature T_A(°C)

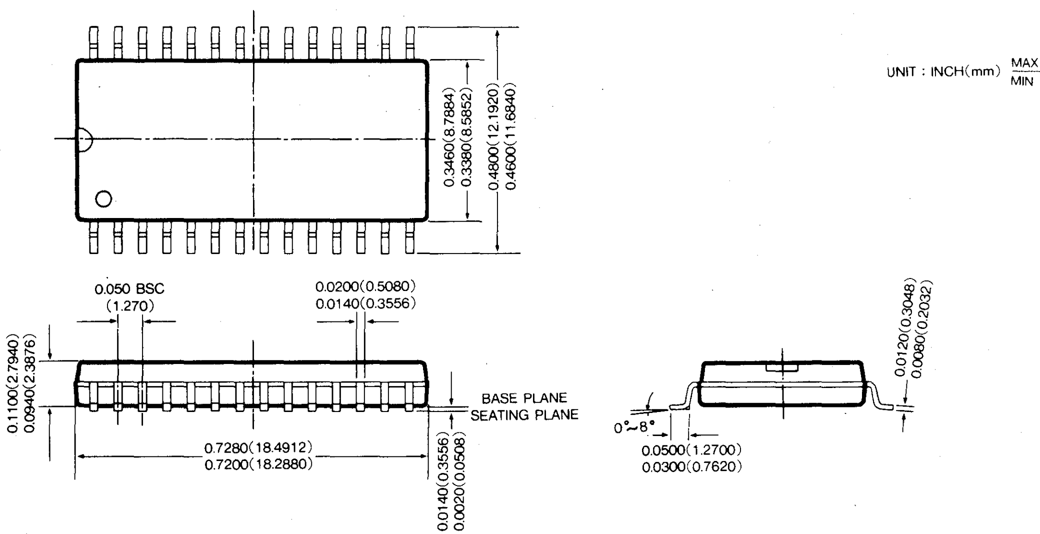

STANDBY CURRENT vs.
SUPPLY VOLTAGE
$\overline{CS}$ =V_{CC}−0.2V
Standby Current I_{SB1}(Normalized)
1.4
1.2
1.0
0.8
0.6
0.4
0.2
2
3
4
5
6
Supply Voltage V_{CC}(V)

PACKAGE INFORMATION

• 28 PIN PLASTIC DUAL IN LINE PACKAGE−600MIL



• 28 PIN SMALL OUTLINE PACKAGE−330MIL



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MEMO

HYUNDAI SEMICONDUCTOR

HY62256A

32K×8-Bit CMOS SRAM

M241201B-MAY92

DESCRIPTION

The HY62256A is a high speed low power, 32,768 words by 8-bit CMOS static RAM fabricated using HYUNDAI's high performance twin tub CMOS process. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 70ns.

The HY62256A has a data retention mode that guarantees data will remain valid at a minimum power supply voltage of 2.0 volt.

Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY62256A family.

FEATURES

- **High speed—70/85/100/120ns (max.)**
- **Low power consumption**
  - **—200mW typical operating (HY62256A-70)**
  - **—10µW typical standby (L/LL-version)**
- **Battery back up (L/LL-version)**
  - **—2 volt data retention**
- **Fully static operation**
  - **—No clock or refresh required**
- **All inputs and outputs directly TTL compatible**
- **Tri-state output**
- **High reliability 28 pin 600 mil P-DIP and 330 mil SOP**

		HY62256A-70	HY62256A-85	HY62256A-10	HY62256A-12
Maximum Access Time (ns)		70	85	100	120
Maximum Average Operating Current (mA)		70	70	70	70
Maximum Standby Current (mA)		1.0	1.0	1.0	1.0
	L	0.1	0.1	0.1	0.1
	LL	0.05	0.05	0.05	0.05

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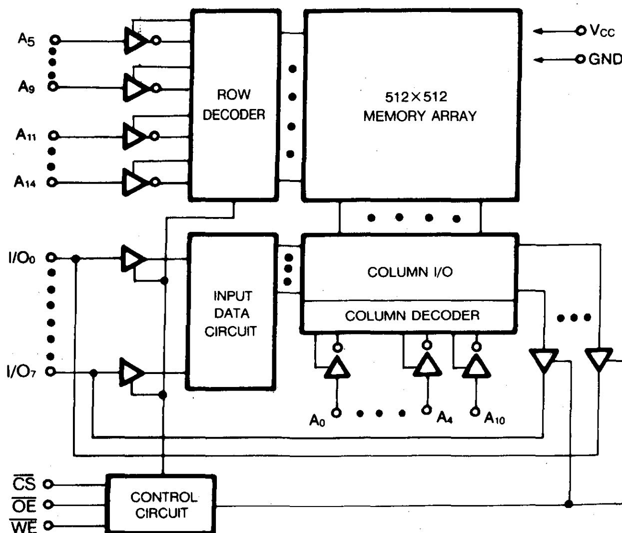
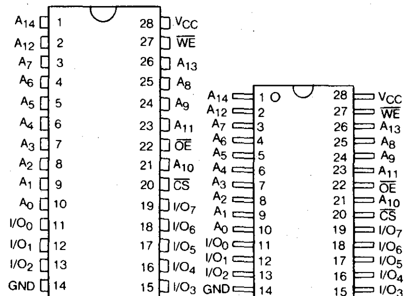
BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_{14}	ADDRESS INPUT
I/O_0-I/O_7	DATA INPUT/OUTPUT
$\overline{CS}$	CHIP SELECT
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
V_{CC}	POWER
GND	GROUND

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}, V_{IN}, $V_{I/O}$	Power Supply, Input, Input/Output Voltage	−0.5[2] to 7.0	V
T_{BIAS}	Temperature Under Bias	−10 to 125	°C
T_{STG}	Storage Temperature	−65 to 150	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA

NOTES :
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended may affect reliability.
2. -3.5V for 20ns pulse.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5[1]	−	0.8	V

NOTE :
1. −3.5V for 20 ns pulse

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION
Standby	H	X	X	High-Z
Read	L	L	H	D_{OUT}
Write	L	X	L	D_{IN}
Output Disabled	L	H	H	High-Z

NOTE :
1. X : H or L

DC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS		HY62256A MIN.	TYP.[1]	MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{IN}=GND to V_{CC}		–	–	1	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{I/O}$=GND to V_{CC}		–	–	1	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}=V_{IL}$, $V_{IN}=V_{IH}$ or V_{IL}, $I_{I/O}$=0mA		–	7	15	mA
I_{CC1}	Average Operating Current	$\overline{CS}=V_{IL}$ Min Duty Cycle=100% $I_{I/O}$=0mA	−70	–	40	70	mA
			−85	–	35	70	mA
			−10	–	30	70	mA
			−12	–	25	70	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}=V_{IH}$		–	–	2	mA
I_{SB1}		$\overline{CS}$ ≥ V_{CC}−0.2V,		–	–	1.0	mA
			L	–	2	100	μA
			LL	–	2	50	μA
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH}=−1.0mA		2.4	–	–	V

NOTE :
1. Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

AC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A=0°C to 70°C)

READ CYCLE

SYMBOL	PARAMETER	HY62256A-70 MIN.	MAX.	HY62256A-85 MIN.	MAX.	HY62256A-10 MIN.	MAX.	HY62256A-12 MIN.	MAX.	UNIT
t_{RC}	Read Cycle Time	70	–	85	–	100	–	120	–	ns
t_{AA}	Address Access Time	–	70	–	85	–	100	–	120	ns
t_{ACS}	Chip Select Access Time	–	70	–	85	–	100	–	120	ns
t_{CLZ}	Chip Selection to Output in Low-Z	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	35	–	45	–	50	–	60	ns
t_{OLZ}	Output Enable to Output in Low-Z	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Deselection to Output in High-Z	0	30	0	30	0	35	0	40	ns
t_{OHZ}	Output Disable to Output in High-Z	0	30	0	30	0	35	0	40	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	10	–	10	–	ns

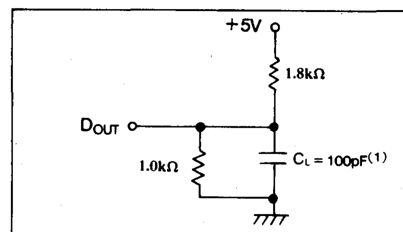
WRITE CYCLE

SYMBOL	PARAMETER	HY62256A-70		HY62256A-85		HY62256A-10		HY62256A-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	100	–	120	–	ns
t_{CW}	Chip Selection to End of Write	65	–	75	–	80	–	85	–	ns
t_{AW}	Address Valid to End of Write	65	–	75	–	80	–	85	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	55	–	60	–	70	–	70	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{OHZ}	Output Disable to Output in High-Z	0	30	0	30	0	35	0	40	ns
t_{WHZ}	Write to Output in High-Z	0	30	0	30	0	35	0	40	ns
t_{DW}	Data to Write Time Overlap	35	–	40	–	40	–	50	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write	5	–	5	–	10	–	10	–	ns

AC TEST CONDITIONS
(T_A=0°C to 70°C)

Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V

OUTPUT LOAD



NOTE:
1. Including scope and the Jig.

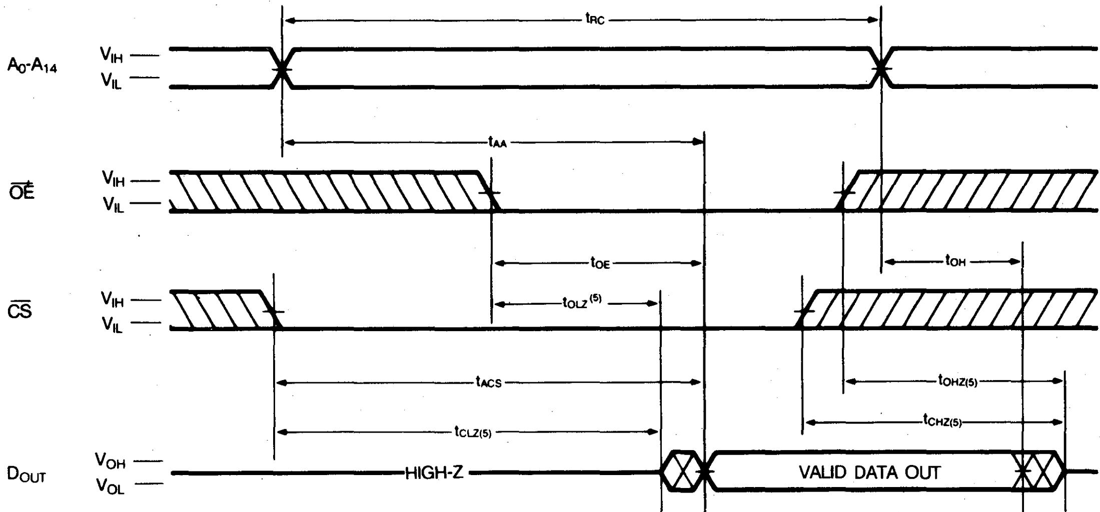
CAPACITANCE[1]
(T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

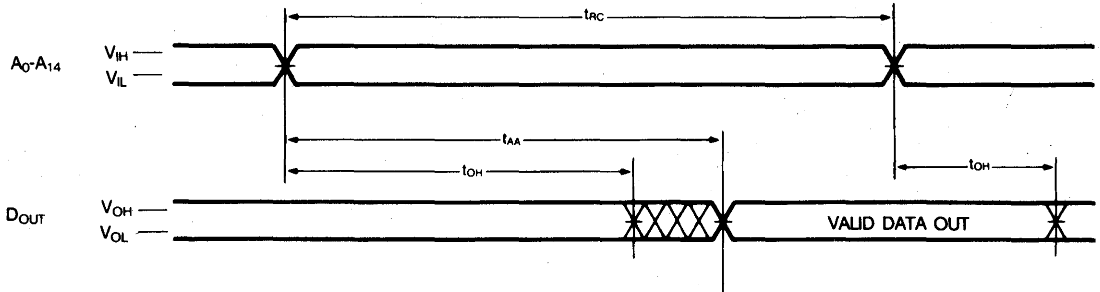
NOTE:
1. This parameter is sampled and not 100% tested.

TIMING DIAGRAMS

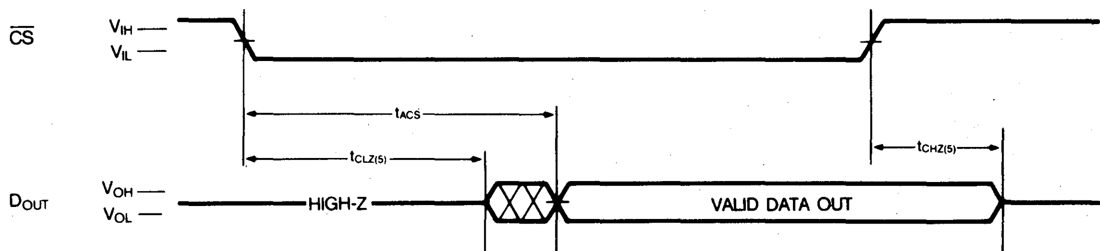
READ CYCLE 1(1)



READ CYCLE 2(1, 2, 4)



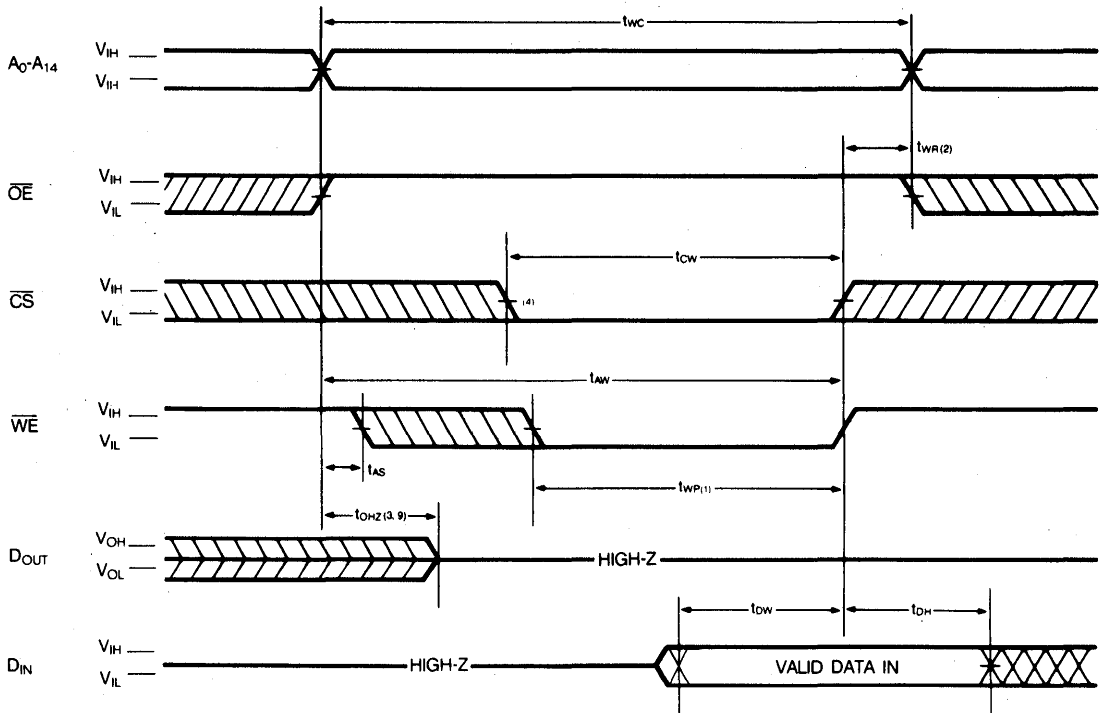
READ CYCLE 3(1, 3, 4)



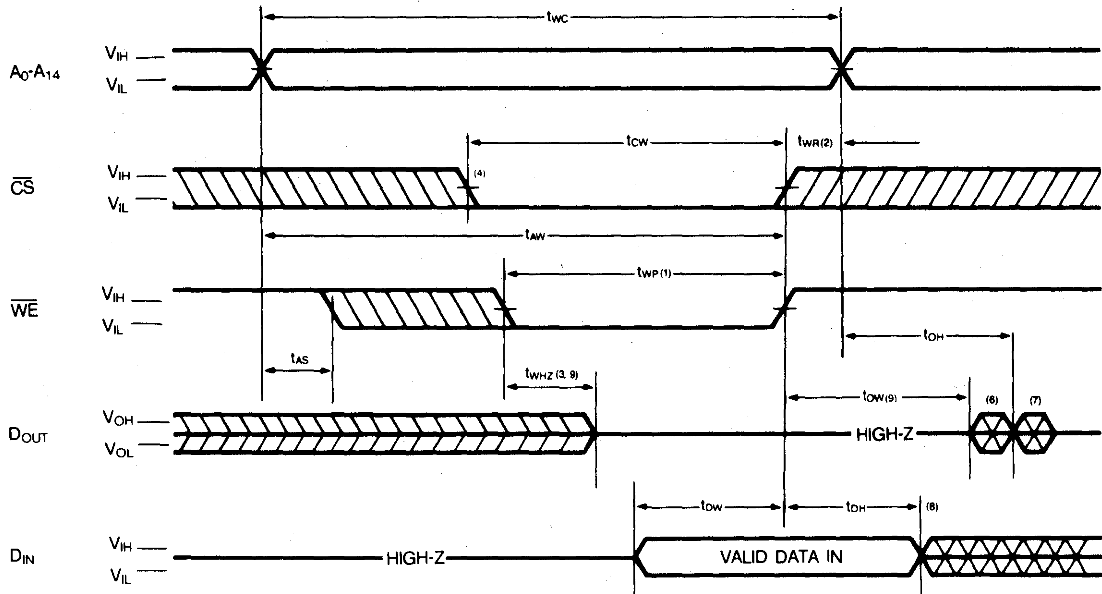
NOTES :

1. **$\overline{WE}$ is high for Read Cycle.**
2. Device is continuously selected. $\overline{CS}=V_{IL}$
3. Addresses are valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}=V_{IL}$
5. Transition is measured $\pm$500mV from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE 1



WRITE CYCLE 2(5)



NOTES :

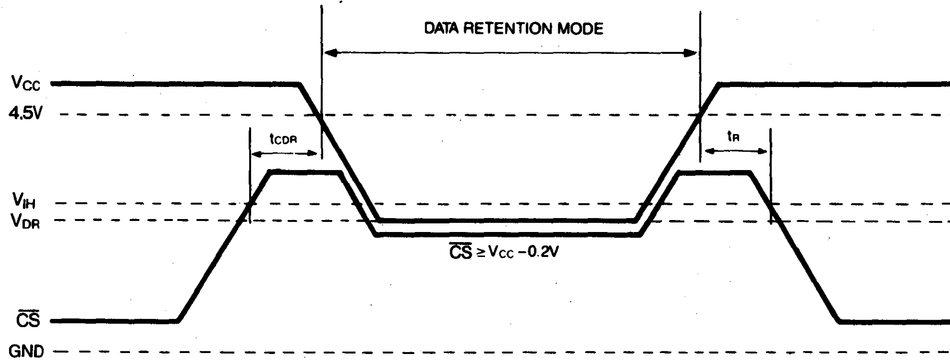
1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high at the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE}=V_{IL}$).
6. D_{OUT} is the same phase of write data of this write cycle.
7. D_{OUT} is the read data of next address.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

DATA RETENTION CHARACTERISTICS(1)
(V_A=0°C to 70°C)

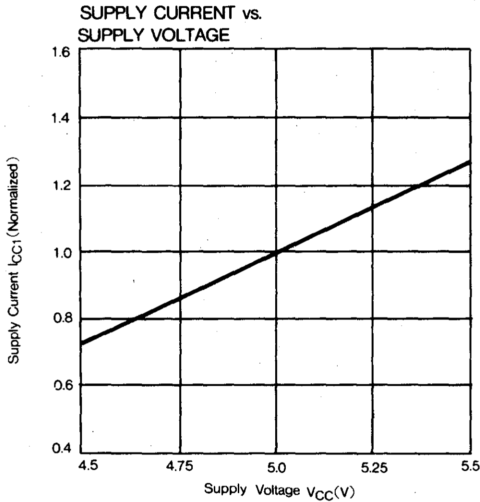
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{DR}	Data Retention Supply Voltage	V_{IN}=0 to V_{CC}, $\overline{CS} \geq V_{CC}-0.2V$		2.0	–	–	V
I_{CCDR}	Data Retention Current	V_{CC}=3.0V, V_{IN}=0 to V_{CC}, $\overline{CS} \geq V_{CC}-0.2V$	L	–	2	50	μA
			LL	–	2	20(2)	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram		0	–	–	ns
t_R	Operating Recovery Time			t_{RC}(3)	–	–	ns

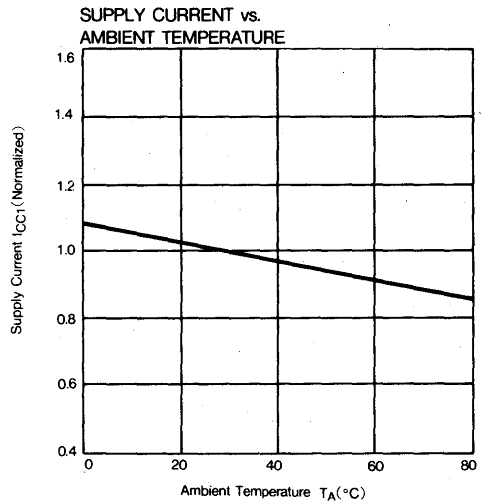
NOTES :
1. These characteristics are guaranteed for L and LL-version.
2. 3μA max. at T_A=0°C to 40°C
3. t_{RC}=Read Cycle Time

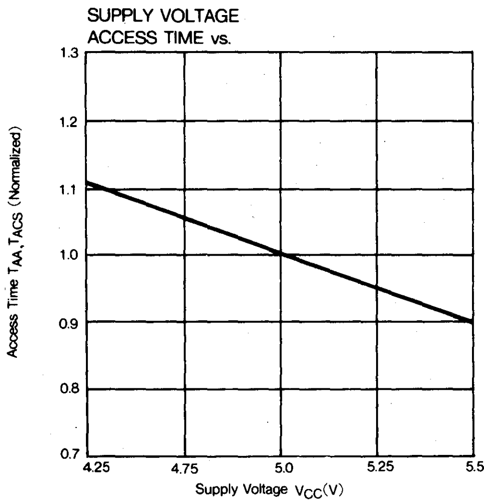
DATA RETENTION TIMING DIAGRAM

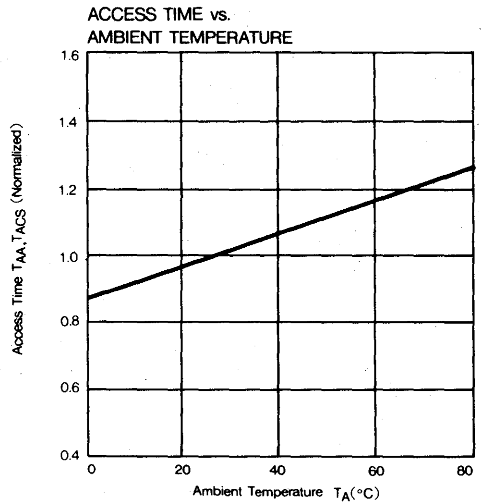


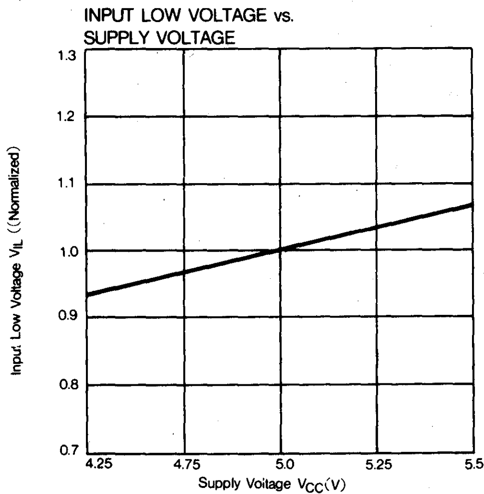
ELECTRICAL CHARACTERISTIC CURVES
(V_{CC}=5V, T_A=25°C, unless otherwise noted)

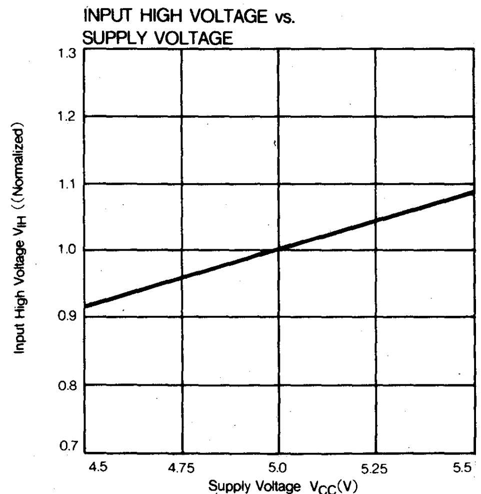












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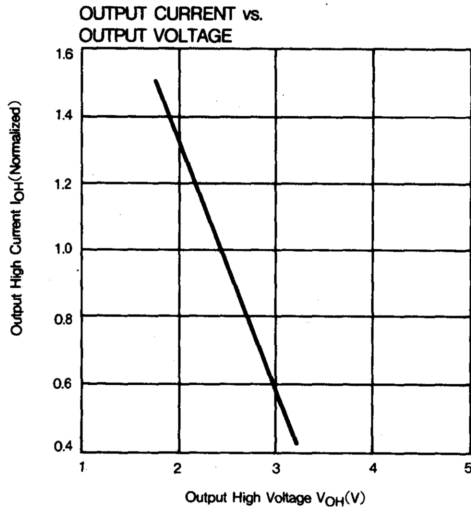
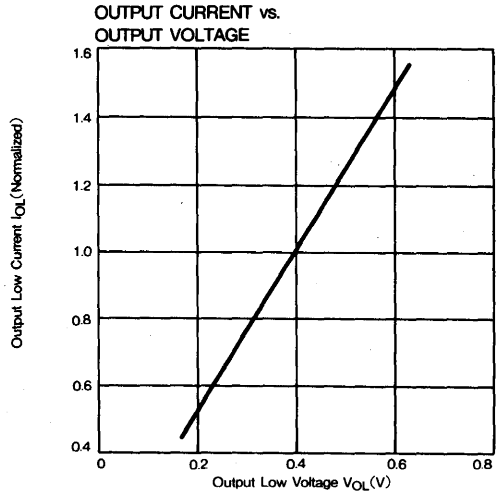
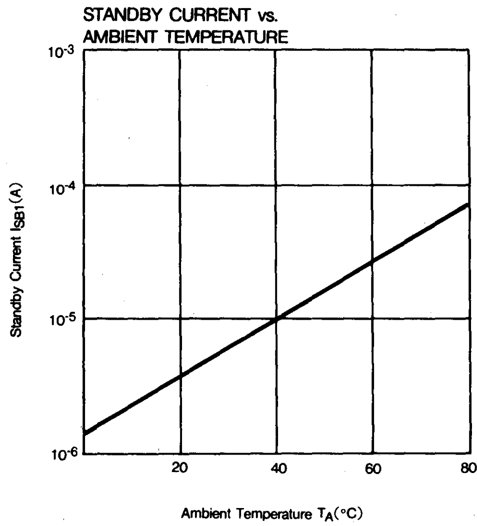
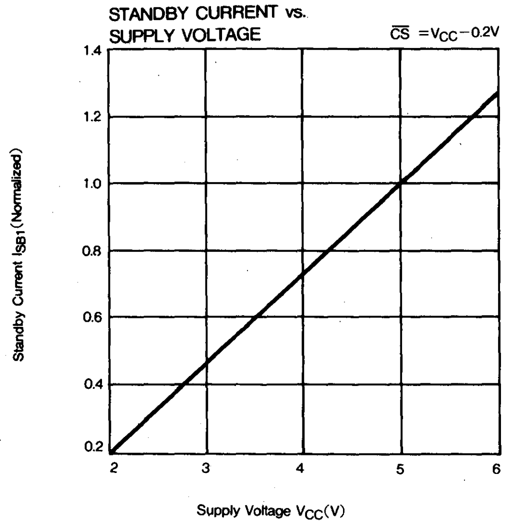

OUTPUT CURRENT vs.
OUTPUT VOLTAGE
Output High Current IOH(Normalized)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
1
2
3
4
5
Output High Voltage VOH(V)

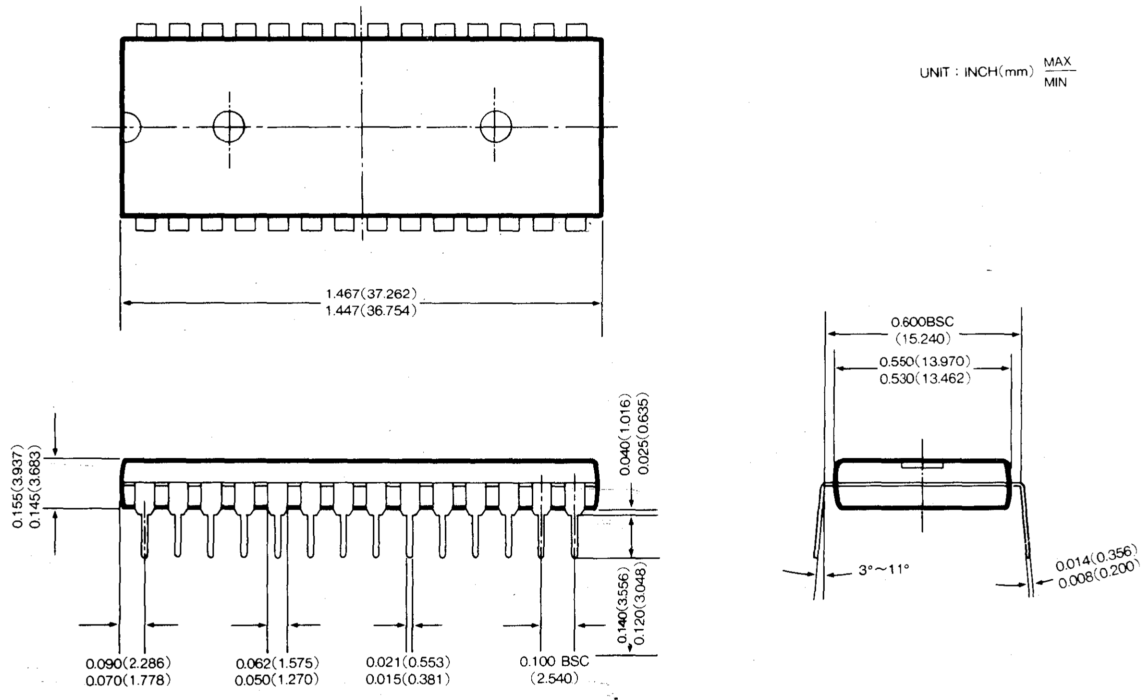

OUTPUT CURRENT vs.
OUTPUT VOLTAGE
Output Low Current IOL(Normalized)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0
0.2
0.4
0.6
0.8
Output Low Voltage VOL(V)


STANDBY CURRENT vs.
AMBIENT TEMPERATURE
Standby Current ISB1(A)
10-3
10-4
10-5
10-6
20
40
60
80
Ambient Temperature TA(°C)


STANDBY CURRENT vs.
SUPPLY VOLTAGE
CS =VCC−0.2V
Standby Current ISB1(Normalized)
1.4
1.2
1.0
0.8
0.6
0.4
0.2
2
3
4
5
6
Supply Voltage VCC(V)

PACKAGE INFORMATION

- 28 PIN PLASTIC DUAL IN LINE PACKAGE−600MIL



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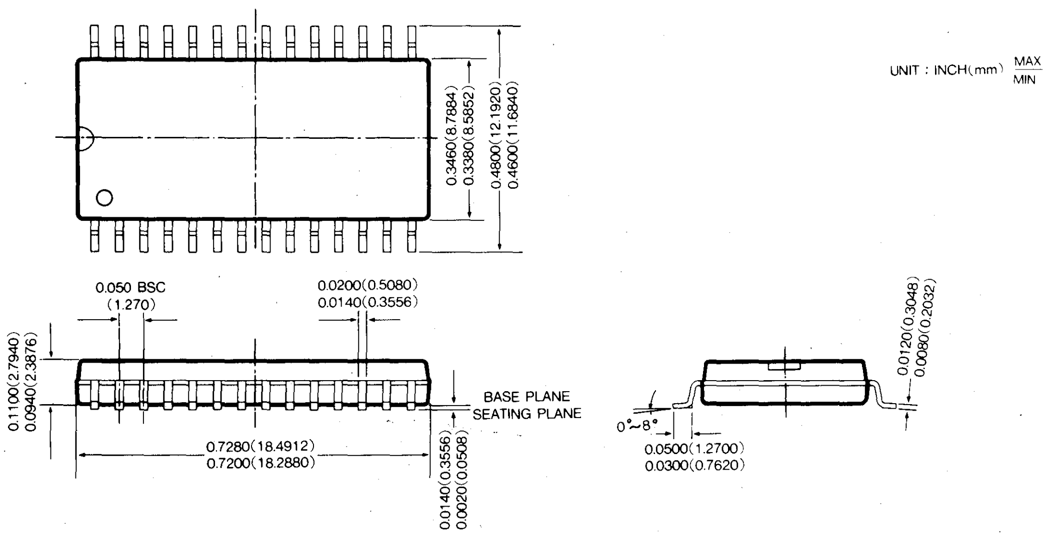
- 28 PIN SMALL OUTLINE PACKAGE−330MIL



MEMO

HYUNDAI SEMICONDUCTOR

HY628100

128K×8-Bit CMOS SRAM

M271200A-MAY92

DESCRIPTION

The HY628100 is a high speed low power, 131,072 words by 8-bit CMOS static RAM fabricated using HYUNDAI's high performance twin tub CMOS process. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 70ns.

The HY628100 has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt.

Using CMOS technology, supply voltages from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY628100 family.

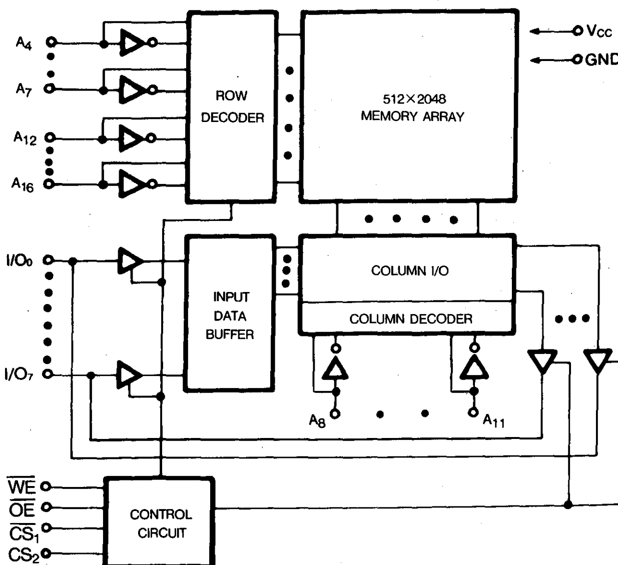
FEATURES

- **High speed — 70/85/100/120 ns (max.)**
- **Low power consumption**
  - **250mW typical operating**
  - **10μW typical standby (L/LL-version)**
- **Battery back up (L/LL-version)**
  - **2 volt data retention**
- **Fully static operation**
  - **No clock or refresh required**
- **All inputs and outputs directly TTL compatible**
- **Tri-state output**
- **High reliability 32 pin 600 mil P-DIP and 525 mil SOP**

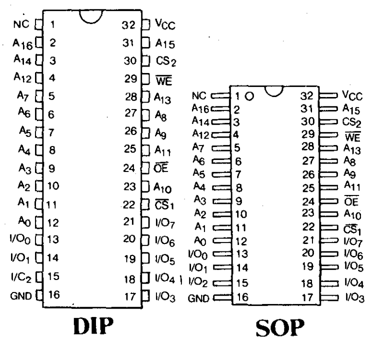
		HY628100-70	HY628100-85	HY628100-10	HY628100-12
Maximum Access Time (ns)		70	85	100	120
Maximum Average Operating Current (mA)		70	70	70	70
Maximum Standby Current (mA)		2.0	2.0	2.0	2.0
	L	0.1	0.1	0.1	0.1
	LL	0.05	0.05	0.05	0.05

5

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_{16}	ADDRESS INPUT
I/O_0-I/O_7	DATA INPUT/OUTPUT
$\overline{CS}_1$	CHIP SELECT ONE
CS_2	CHIP SELECT TWO
$\overline{WE}$	WRITE ENABLE
$\overline{OE}$	OUTPUT ENABLE
V_{CC}	POWER
GND	GROUND

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}, V_{IN}, $V_{I/O}$	Power Supply, Input, Input/Output Voltage	$-0.5^{(2)}$ to 7.0	V
T_{BIAS}	Temperature Under Bias	−10 to 125	℃
T_{STG}	Storage Temperature	−65 to 150	℃
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA

NOTES :
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating condition for extended may affect reliability.
2. −3.5V for 20ns pulse.

RECOMMENDED DC OPERATING CONDITIONS
(T_A=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	$-0.5^{(1)}$	–	0.8	V

NOTE :
1. −3.5V for 20ns pulse

TRUTH TABLE

MODE	$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	I/O OPERATION
Standby	H	X	X	X	High-Z
	X	L	X	X	High-Z
Output Disabled	L	H	H	H	High-Z
Read	L	H	H	L	D_{OUT}
Write	L	H	L	X	D_{IN}

NOTE :
1. X : H or L

DC CHARACTERISTICS
(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS		HY628100 MIN.	HY628100 TYP.[1]	HY628100 MAX.	UNIT
$\mid I_{LI} \mid$	Input Leakage Current	V_{IN}=GND to V_{CC}		–	–	1	μA
$\mid I_{LO} \mid$	Output Leakage Current	$\overline{CS_1}=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, $V_{I/O}$=GND to V_{CC}		–	–	1	μA
I_{CC}	Operating Power Supply Current	$\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$, $V_{IN}=V_{IH}$ or V_{IL}, $I_{I/O}$ =0mA		–	–	50	mA
I_{CC1}	Average Operating Current	Min cycle, Duty=100% $\overline{CS_1}=V_{IL}$, $CS_2=V_{IH}$ $V_{IN}=V_{IH}$ or V_{IL}, $I_{I/O}$ =0mA		–	50	70	mA
I_{CC2}		Cycle Time=1μs, Duty=100% $\overline{CS_1} \leq 0.2V$, $CS_2 \geq V_{CC}-0.2V$ $V_{IN} \leq 0.2V$ or $\geq V_{CC}-0.2V$, $I_{I/O}$ =0mA		–	–	40	mA
I_{SB}	Standby Power Supply Current	$\overline{CS_1}=V_{IH}$ or $CS_2=V_{IL}$		–	–	3	mA
I_{SB1}		$\overline{CS_1} \geq V_{CC}-0.2V$, $CS_2 \leq 0.2V$, $V_{IN} \leq 0.2V$ or $\geq V_{CC}-0.2V$		–	–	2	mA
			L	–	2	100	μA
			LL	–	2	50	μA
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH}=−1.0mA		2.4	–	–	V

NOTE :
1. V_{CC}=5V, T_A=25°C

AC CHARACTERISTICS
(V_{CC}=5V± 10%, T_A=0°C to 70°C)

READ CYCLE

SYMBOL	PARAMETER	HY628100-70 MIN.	HY628100-70 MAX.	HY628100-85 MIN.	HY628100-85 MAX.	HY628100-10 MIN.	HY628100-10 MAX.	HY628100-12 MIN.	HY628100-12 MAX.	UNIT
t_{RC}	Read Cycle Time	70	–	85	–	100	–	120	–	ns
t_{AA}	Address Access Time	–	70	–	85	–	100	–	120	ns
t_{ACS}	Chip Select Access Time	–	70	–	85	–	100	–	120	ns
t_{CLZ}	Chip Selection to Output in Low-Z	10	–	10	–	10	–	10	–	ns
t_{OE}	Output Enable to Output Valid	–	35	–	45	–	50	–	60	ns
t_{OLZ}	Output Enable to Output in Low-Z	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Deselection to Output in High-Z	–	25	–	30	–	35	–	40	ns
t_{OHZ}	Output Disable to Output in High-Z	–	25	–	30	–	35	–	40	ns
t_{OH}	Output Hold from Address Change	10	–	10	–	10	–	10	–	ns

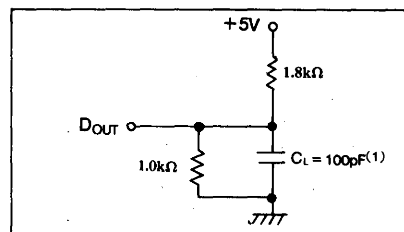
WRITE CYCLE

SYMBOL	PARAMETER	HY628100-70		HY628100-85		HY628100-10		HY628100-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	70	–	85	–	100	–	120	–	ns
t_{CW}	Chip Selection to End of Write	60	–	75	–	90	–	100	–	ns
t_{AW}	Address Valid to End of Write	60	–	75	–	90	–	100	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	55	–	65	–	75	–	85	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	ns
t_{OHZ}	Output Disable to Output in High-Z	–	30	–	30	–	35	–	40	ns
t_{WHZ}	Write to Output in High-Z	–	25	–	30	–	30	–	30	ns
t_{DW}	Data to Write Time Overlap	30	–	35	–	40	–	50	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	0	–	ns
t_{OW}	Output Active from End of Write	5	–	5	–	5	–	5	–	ns

AC TEST CONDITIONS
(T_A=0°C to 70°C)

Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V

OUTPUT LOAD



NOTE :
1. Including scope and the Jig.

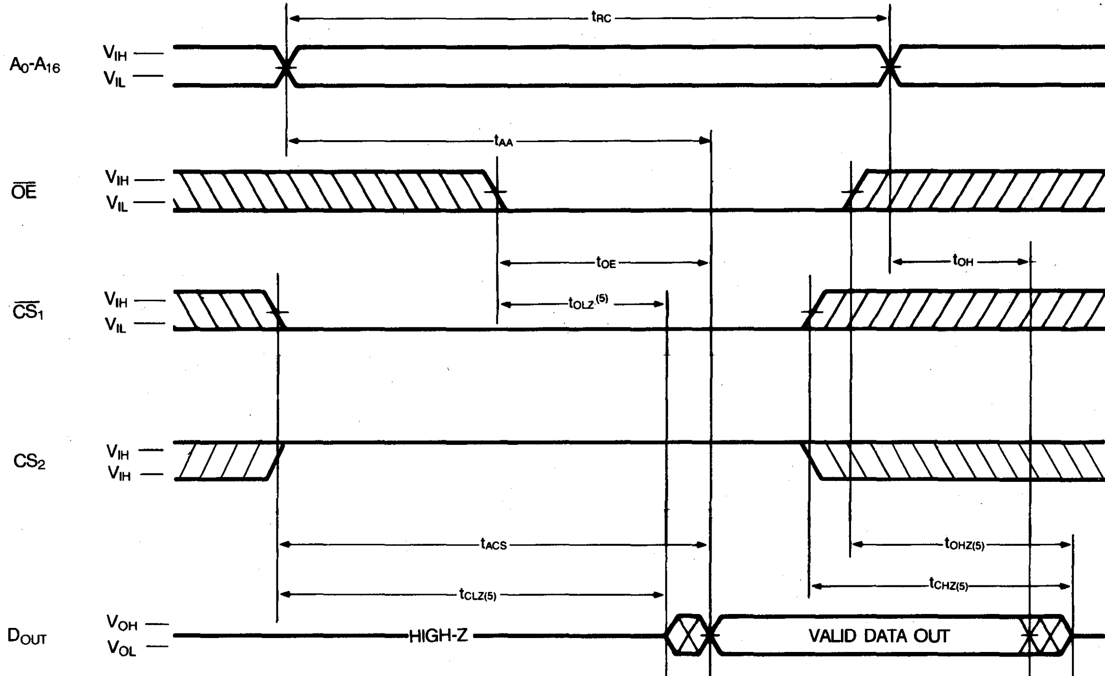
CAPACITANCE[1]
(T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$=0V	10	pF

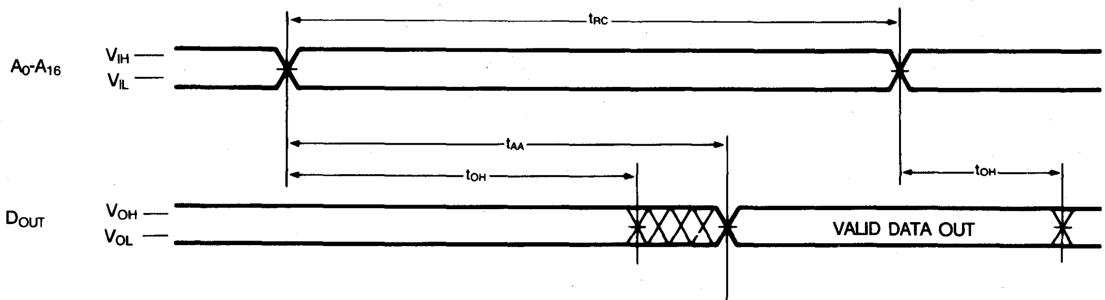
NOTE :
1. This parameter is sampled and not 100% tested.

TIMING DIAGRAMS

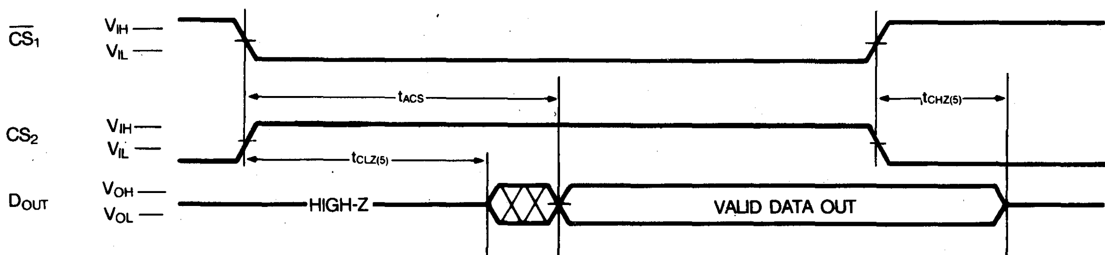
READ CYCLE 1[1]



READ CYCLE 2[1,2,4]



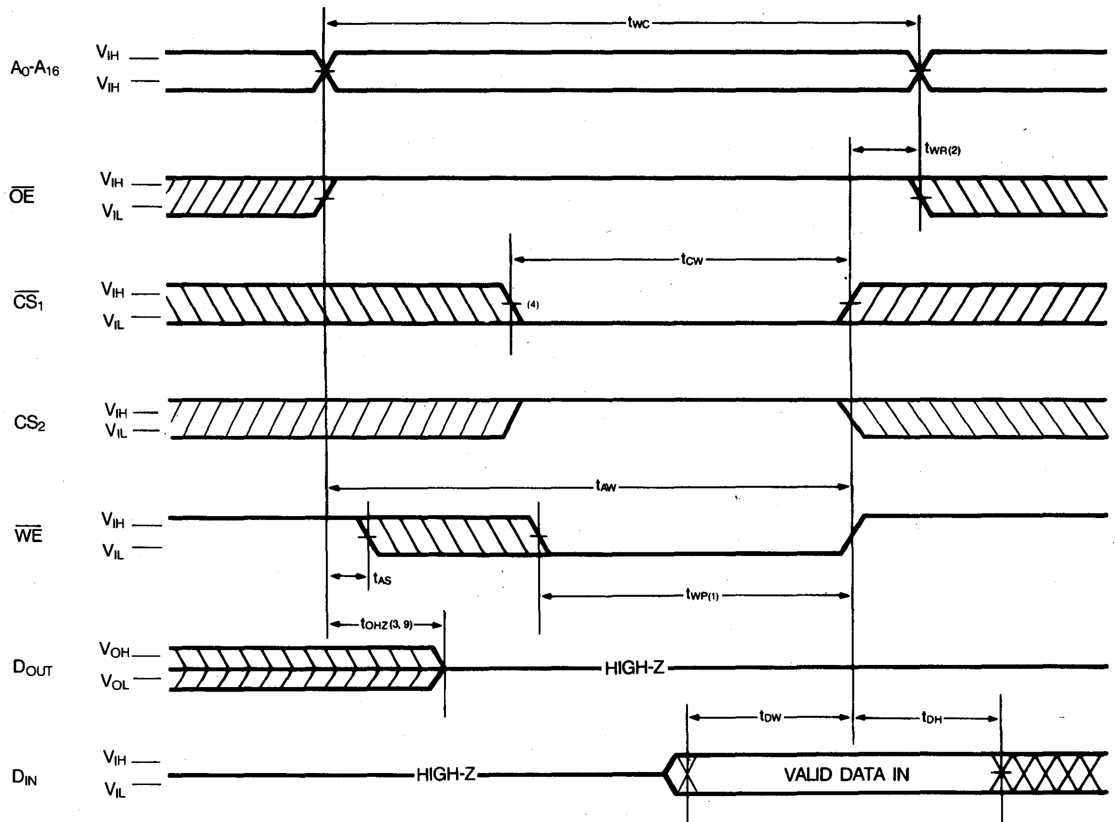
READ CYCLE 3[1,3,4]



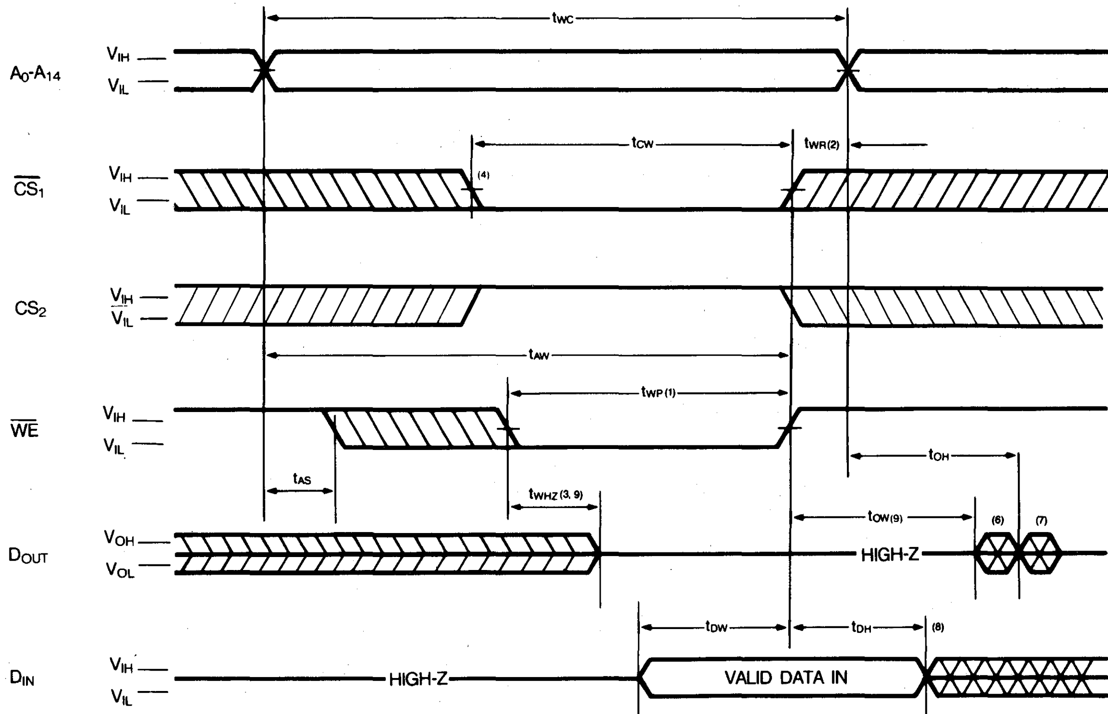
NOTES :

1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1=V_{IL}$, $CS_2=V_{IH}$
3. Addresses are valid prior to or coincident with $\overline{CS}_1$ transition low, and CS_2 transition high.
4. $\overline{OE}=V_{IL}$
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

WRITE CYCLE 1



WRITE CYCLE 2(5)



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NOTES :

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS_1}$, high CS_2 and low $\overline{WE}$.
2. t_{WR} is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS_1}$ low transition and the CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE}=V_{IL}$) for write cycle 2.
6. D_{OUT} is the same phase of write data of this write cycle.
7. D_{OUT} is the read data of next address.
8. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

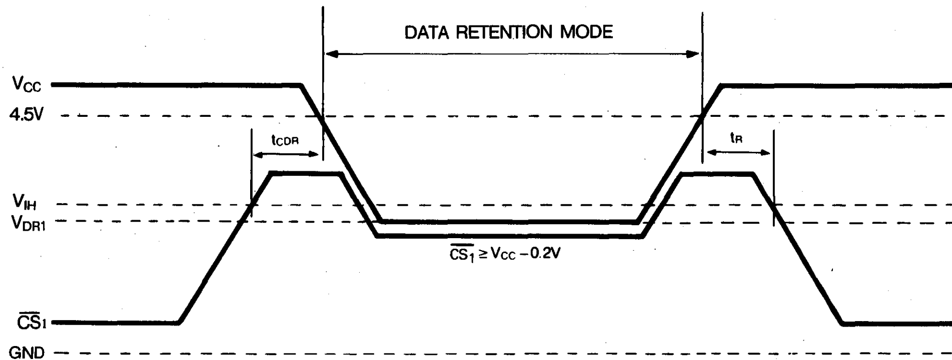
DATA RETENTION CHARACTERISTICS[1]

(V_A=0°C to 70°C)

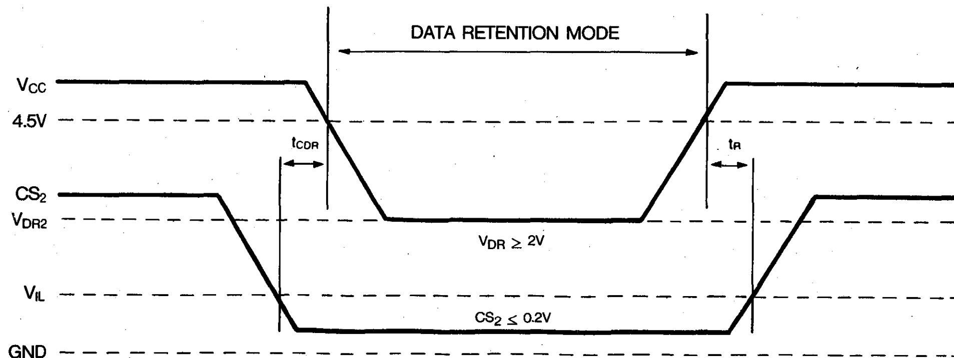
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.[2]	MAX.	UNIT
V_{DR}	Data Retention Supply Voltage	V_{IN}=0 to V_{CC}, $\overline{CS}_1 \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ or $0V \leq CS_2 \leq 0.2V$		2.0	–	–	V
I_{CCDR}	Data Retention Current	V_{CC}=3.0V, V_{IN}=0 to V_{CC}, $\overline{CS}_1 \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ or $0V \leq CS_2 \leq 0.2V$	L	–	2	50	μA
			LL	–	2	30	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram		0	–	–	ns
t_R	Operating Recovery Time			t_{RC}[3]	–	–	ns

NOTES :
1. These characteristics are guaranteed for L and LL-version.
2. T_A=25℃
3. t_{RC}=Read Cycle Time

DATA RETENTION TIMING DIAGRAM 1 ($\overline{CS}_1$ Controlled)



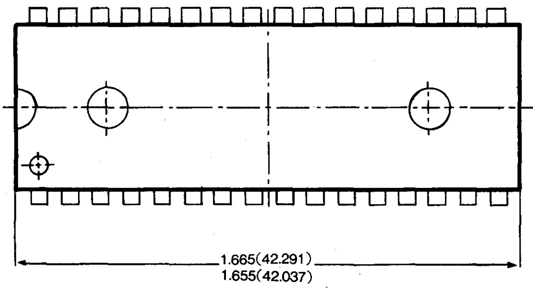
DATA RETENTION TIMING DIAGRAM 2 (CS_2 Controlled)

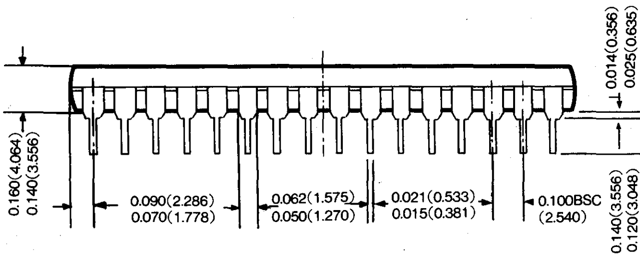


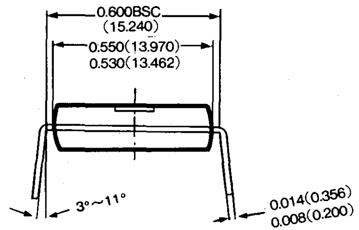
PACKAGE INFORMATION

• **32 PIN PLASTIC DUAL IN LINE PACKAGE−600 MIL**

UNIT : INCH(mm) MAX/MIN







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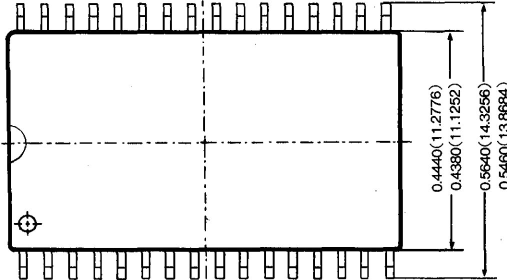
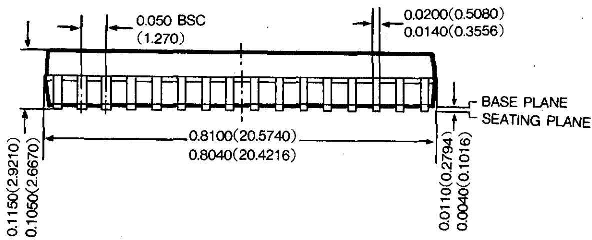
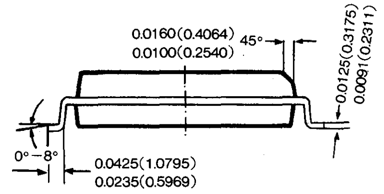
• **32 PIN SMALL OUTLINE PACKAGE−525 MIL**



UNIT : INCH(mm) MAX/MIN





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PRELIMINARY

HYUNDAI SEMICONDUCTOR

HY234000

512K×8-Bit CMOS MASK ROM

M611200A-MAY92

DESCRIPTION

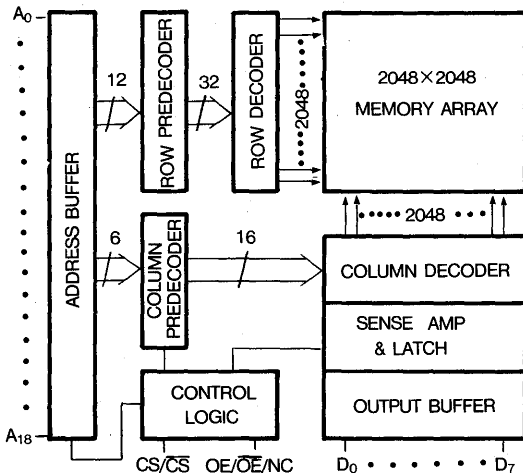
The HY234000 is mask-programmable ROM organized as 524,288 words by 8 bits. It is fabricated using HYUNDAI's CMOS process technology. The HY234000 operates with a 5V power supply and all inputs and outputs are TTL compatible. It satisfies user option modes with the polarity-programmable CS and OE.

FEATURES

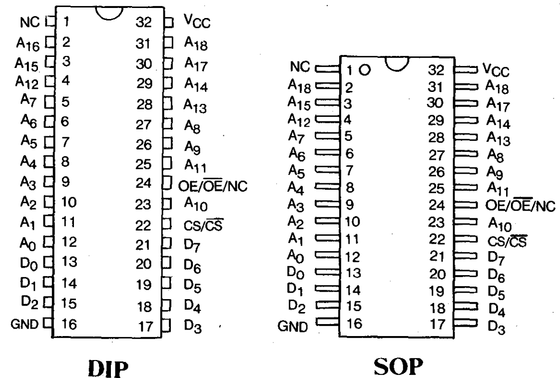
- Speed-150/200/250 ns (max.)
- Power consumption (max.)
  - 220mW (operating)
- Polarity-programmable pins
  - CS/$\overline{CS}$, OE/$\overline{OE}$/NC
- All inputs and outputs TTL compatible
- Tri-state output
- 32-pin 600 mil P-DIP and 440 mil SOP

	HY234000-15	HY234000-20	HY234000-25
Maximum Access Time (ns)	150	200	250
Maximum Operating Current (mA)	40	40	40
Maximum Standby Current (μA)	100	100	100

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_{18}	ADDRESS INPUT
D_0-D_7	DATA OUTPUT
CS/$\overline{CS}$	CHIP SELECT
OE/$\overline{OE}$	OUTPUT ENABLE
V_{CC}	POWER
GND	GROUND
N/C	NO CONNECTION

6

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}, V_{IN}, $V_{I/O}$	Power Supply, Input, Input/Output Voltage	−0.5 to 7.0	V
T_{BIAS}	Temperature Under Bias	−10 to 85	℃
T_{STG}	Storage Temperature	−65 to 150	℃

NOTES :

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	−0.5	–	0.8	V
T_A	Ambient Temperature	0	–	70	°C

TRUTH TABLE

MODE	CS/$\overline{CS}$	OE/$\overline{OE}$	D_0-D_7	OPERATION
Not Selected	L/H	$X^{(1)}$	High-Z	Standby
Output Disabled	H/L	L/H	High-Z	Active
Read	H/L	H/L	D_{OUT}	Active

NOTE :
1. X=L or H

DC CHARACTERISTICS
(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	HY234000		UNIT
			MIN.	MAX.	
$\|I_{LI}\|$	Input Leakage Current	V_{IN}=0 to V_{CC}	–	10	μA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT}=0 to V_{CC}	–	10	μA
I_{CC}	Opreating Current	f=6.7MHz, $\overline{CS}$=$\overline{OE}$=V_{IL} All D_{OUT}=open	–	40	mA
		f=1MHz, $\overline{CS}$=$\overline{OE}$=V_{IL} All D_{OUT}=open	–	15	mA
I_{SB1}	Standby Current(TTL)	$\overline{CS}$=V_{IH}, All D_{OUT}=open	–	2	mA
I_{SB2}	Standby Current(CMOS)	$\overline{CS}$=V_{CC}, All D_{OUT}=open	–	100	μA
V_{OH}	Output High Voltage	I_{OH}=–1mA	2.4	–	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		0.4	V

AC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	HY234000-15		HY234000-20		HY234000-25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	150	–	200	–	250	–	ns
t_{AA}	Address Access Time	–	150	–	200	–	250	ns
t_{ACS}	Chip Select Access Time	–	150	–	200	–	250	ns
t_{OE}	Output Enable Time	–	70	–	80	–	100	ns
t_{DH}	Data Hold Time	10	–	10	–	10	–	ns
t_{DF}	Data Floating Time	–	60	–	80	–	100	ns

CAPACITANCE

(V_{CC}=5V± 10%, T_A=0°C to 70°C, f=1MHz)

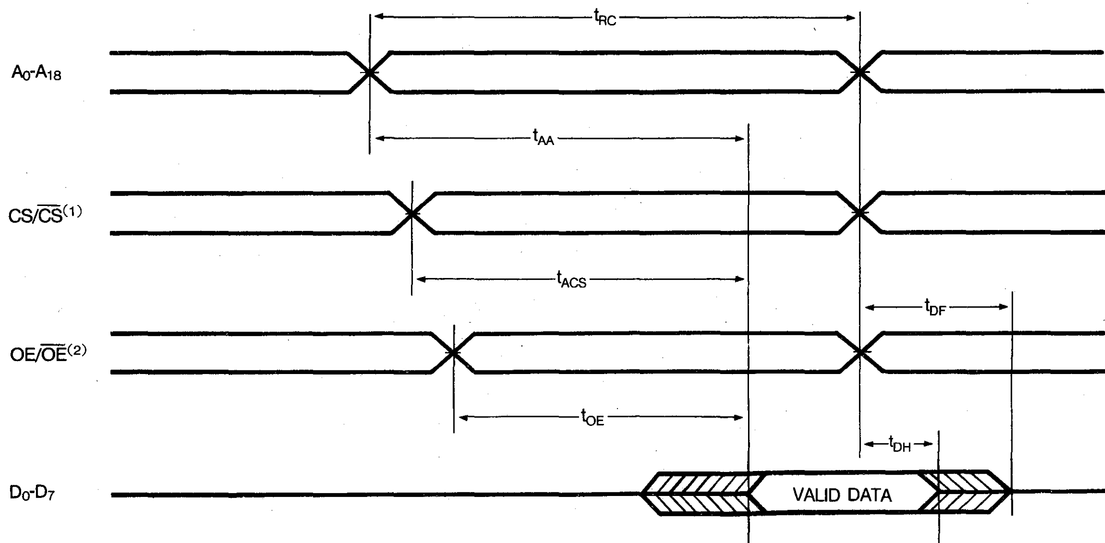
SYMBOL	PARAMETER	TEST CONDITION	TYPE	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	–	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	–	10	pF

AC TEST CONDITIONS

Input pulse level	0.6V to 2.4V
Input rise/fall time	10ns
Input reference level	1.5V
Output reference level	0.8V and 2.0V
Output load	1 TTL Gate and C_L=100pF

TIMING DIAGRAMS

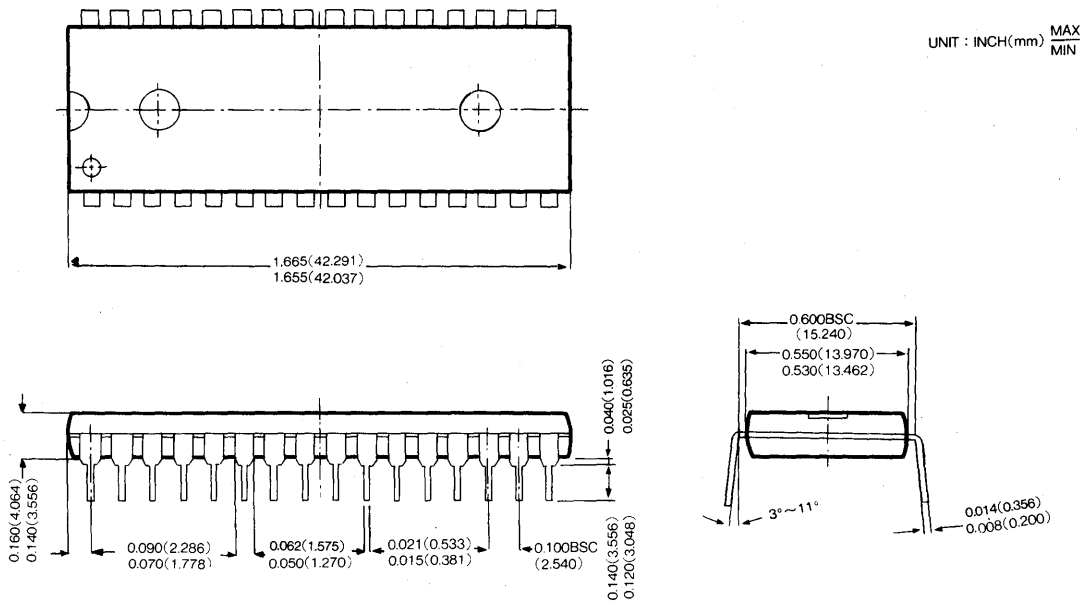
READ CYCLE



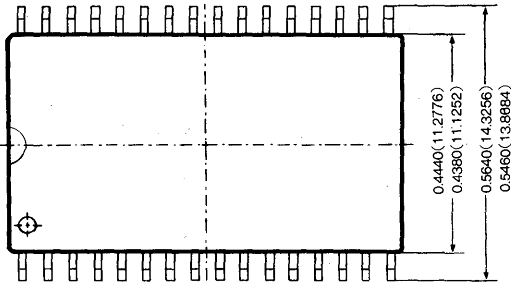
NOTES :
1. $\overline{CS}$ is low active. CS is high active.
2. $\overline{OE}$ is low active. OE is high active.

PACKAGE INFORMATION

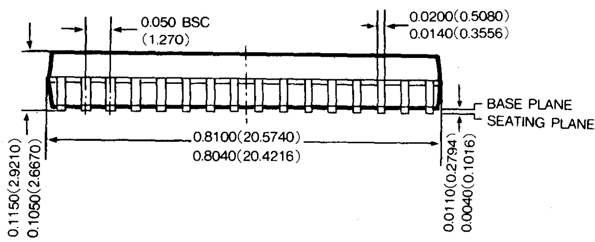
• 32 PIN PLASTIC DUAL IN LINE PACKAGE−600 MIL

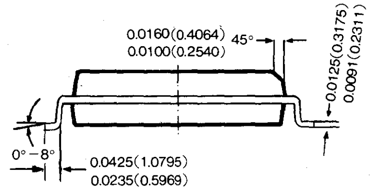


• 32 PIN SMALL OUTLINE PACKAGE−440 MIL



UNIT : INCH(mm) $\frac{MAX}{MIN}$





6

MEMO

PRELIMINARY

HYUNDAI SEMICONDUCTOR

HY234001

512K×8-Bit CMOS MASK ROM

M631200A-MAY92

DESCRIPTION

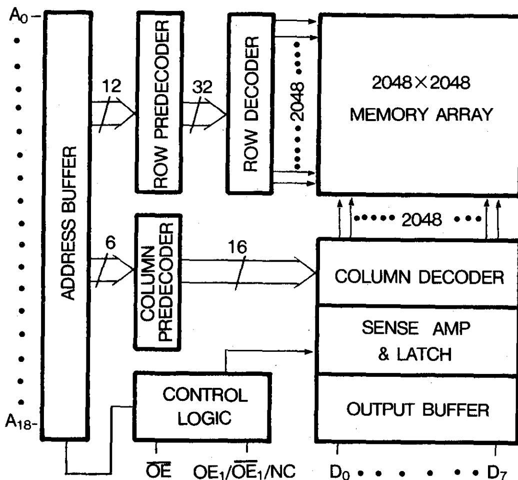
The HY234001 is mask-programmable ROM organized as 524,288 words by 8 bits. It is fabricated using HYUNDAI's CMOS process technology. The HY234001 operates with a 5V power supply and all inputs and outputs are TTL compatible. It satisfies user option modes with the polarity-programmable OE.

FEATURES

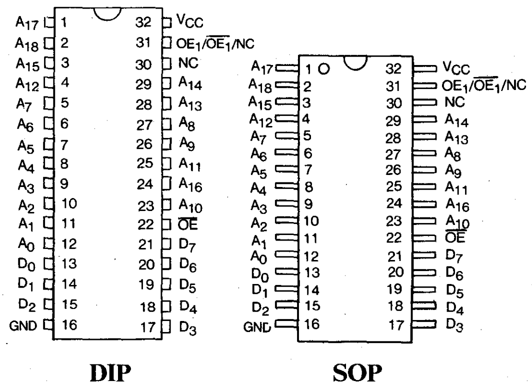
- Speed-150/200/250 ns (max.)
- Power consumption (max.)
  - 220mW (operating)
- Polarity-programmable pin
  - $OE_1/\overline{OE_1}$/NC
- All inputs and outputs TTL compatible
- Tri-state output
- 32-pin 600 mil P-DIP and 440 mil SOP

	HY234001-15	HY234001-20	HY234001-25
Maximum Access Time (ns)	150	200	250
Maximum Operating Current (mA)	40	40	40

BLOCK DIAGRAM



PIN CONNECTIONS



PIN NAMES

A_0-A_{18}	ADDRESS INPUT
D_0-D_7	DATA OUTPUT
$\overline{OE}$	OUTPUT ENABLE
$OE_1/\overline{OE_1}$	OUTPUT ENABLE
V_{CC}	POWER
GND	GROUND
N/C	NO CONNECTION

6

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}, V_{IN}, $V_{I/O}$	Power Supply, Input, Input/Output Voltage	−0.5 to 7.0	V
T_{BIAS}	Temperature Under Bias	−10 to 85	℃
T_{STG}	Storage Temperature	−65 to 150	℃

NOTES :
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	−	6.0	V
V_{IL}	Input Low Voltage	−0.5	−	0.8	V
T_A	Ambient Temperature	0	−	70	°C

TRUTH TABLE

MODE	$\overline{OE}$	$OE_1/\overline{OE_1}$	D_0-D_7	OPERATION
Output Disabled	H	X(1)	High-Z	Non-selected
Output Disabled	X	L/H	High-Z	Non-selected
Read	L	H/L	D_{OUT}	Active

NOTE :
1. X=L or H

DC CHARACTERISTICS
(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	HY234001		UNIT
			MIN.	MAX.	
$\lvert I_{LI} \rvert$	Input Leakage Current	V_{IN}=0 to V_{CC}	–	10	μA
$\lvert I_{LO} \rvert$	Output Leakage Current	V_{OUT}=0 to V_{CC}	–	10	μA
I_{CC}	Opreating Current	f=6.7MHz, V_{IN}=V_{IH}/V_{IL} All D_{OUT}=open	–	40	mA
		f=1MHz, V_{IN}=V_{IH}/V_{IL} All D_{OUT}=open	–	15	mA
V_{OH}	Output High Voltage	I_{OH}=–1mA	2.4	–	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		0.4	V

AC CHARACTERISTICS
(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	HY234001-15		HY234001-20		HY234001-25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	150	–	200	–	250	–	ns
t_{AA}	Address Access Time	–	150	–	200	–	250	ns
t_{OE}	Output Enable Time	–	70	–	80	–	100	ns
t_{DH}	Data Hold Time	10	–	10	–	10	–	ns
t_{DF}	Data Floating Time	–	60	–	80	–	100	ns

CAPACITANCE
(V_{CC}=5V± 10%, T_A=0°C, f=1MHz)

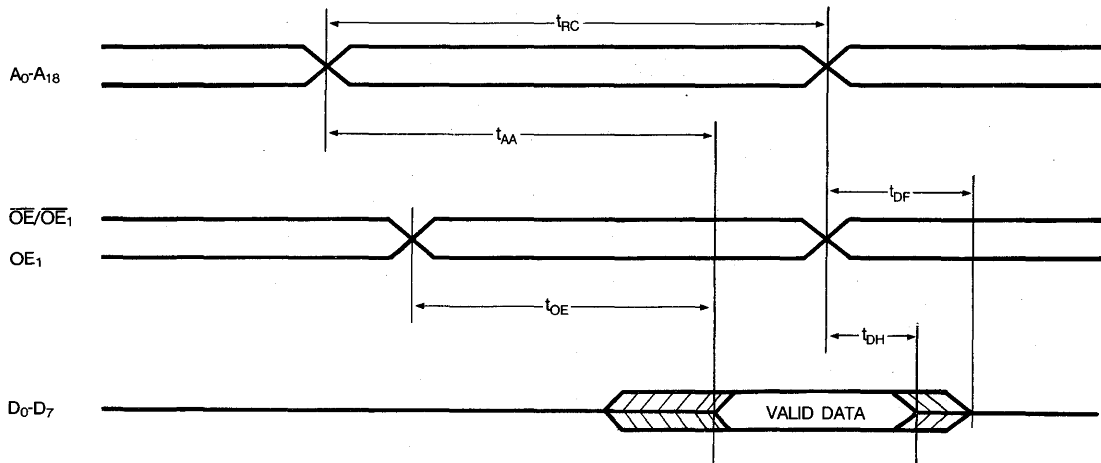
SYMBOL	PARAMETER	TEST CONDITION	TYPE	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	–	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	–	10	pF

AC TEST CONDITIONS

Input pulse level	0.6V to 2.4V
Input rise/fall time	10ns
Input reference level	1.5V
Output reference level	0.8V and 2.0V
Output load	1 TTL Gate and C_L=100pF

TIMING DIAGRAMS

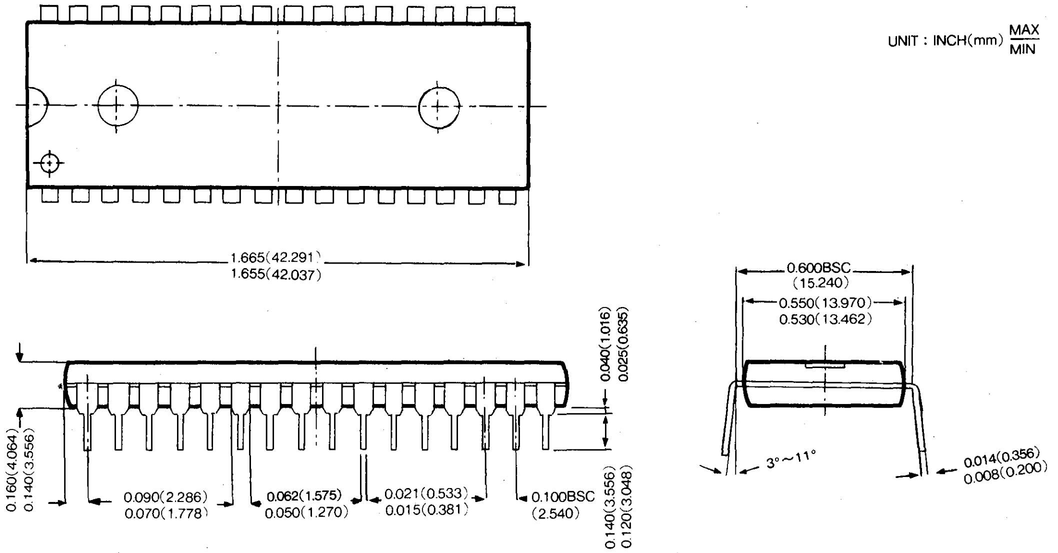
READ CYCLE



6

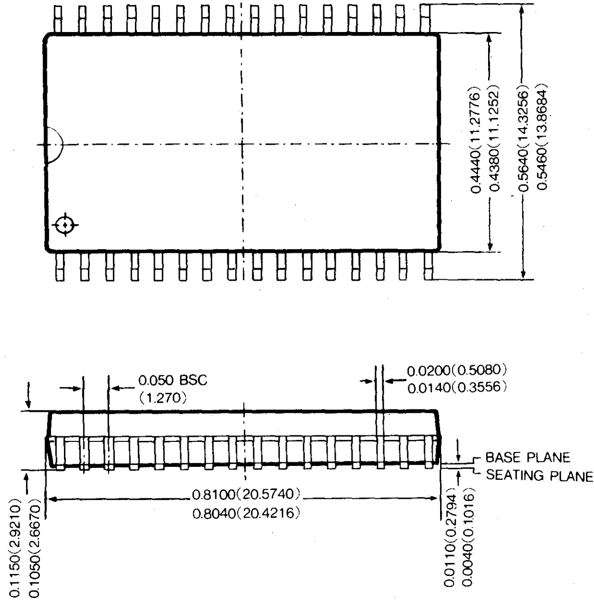
PACKAGE INFORMATION

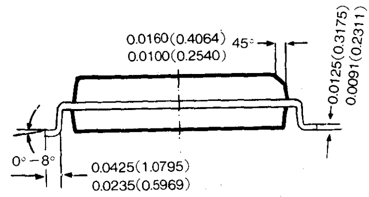
- 32 PIN PLASTIC DUAL IN LINE PACKAGE—600 MIL



• **32 PIN SMALL OUTLINE PACKAGE — 440 MIL**

UNIT : INCH(mm) MAX/MIN





6

MEMO

HYUNDAI SEMICONDUCTOR

HY234100

512K × 8/256K × 16-Bit CMOS MASK ROM

M621201A-MAY92

DESCRIPTION

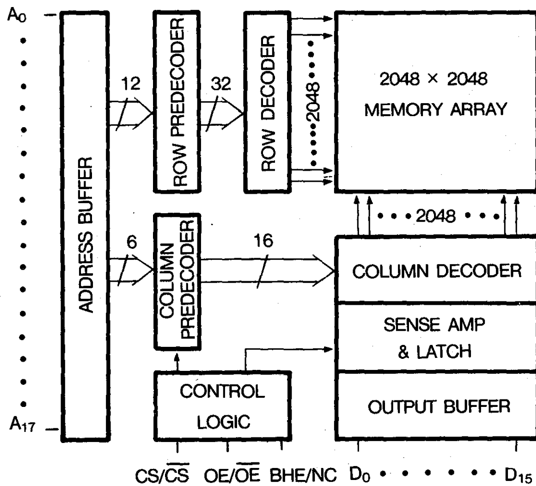
The HY234100 is mask-programmable ROM organized as 524,288 words by 8 bits or 262,144 words by 16 bits. It is fabricated using HYUNDAI's CMOS process technology. The HY234100 operates with a 5V power supply and all inputs and outputs are TTL compatible. It satisfies user option modes with the polarity-programmable CS and OE.

FEATURES

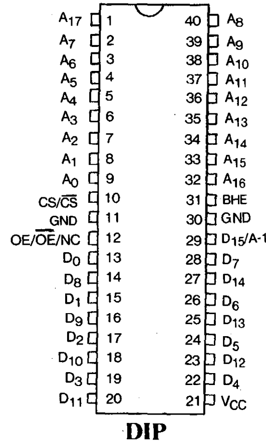
- **Speed- 150/200/250 ns (max.)**
- **524,288x8/262,144x16 bit organization**
- **Power consumption (max.)**
  - **275mW (operating)**
- **Polarity-programmable pins**
  - **CS/$\overline{CS}$, OE/$\overline{OE}$/NC**
- **All inputs and outputs TTL compatible**
- **Tri-state output**
- **40-pin 600 mil P-DIP**

	HY234100-15	HY234100-20	HY234100-25
Maximum Access Time (ns)	150	200	250
Maximum Operating Current (mA)	50	50	50
Maximum Standby Current (μA)	100	100	100

BLOCK DIAGRAM



PIN CONNECTIONS



DIP

PIN NAMES

A_0-A_{17}	ADDRESS INPUT
D_0-D_7	DATA OUTPUT
D_{15}/A-1	DATA15-WORD MODE/ LSB ADDR-BYTE MODE
CS/$\overline{CS}$	CHIP SELECT
OE/$\overline{OE}$	OUTPUT ENABLE
BHE	BYTE HIGH ENABLE
V_{CC}	POWER
GND	GROUND
N/C	NO CONNECTION

6

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
V_{DD}, V_{IN} $V_{I/0}$	Power Supply, Input, Input/Output Voltage	−0.5 to 7.0	V
T_{BIAS}	Temperature Under Bias	−10 to 85	°C
T_{STG}	Storage Temperature	−65 to 150	°C

NOTES :
1. Stresses greater than those listed under ABSOLUTE MAXIMUM may cause permanent damage to the device. This is a stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	−0.5	–	0.8	V
T_A	Ambient Temperature	0	–	70	°C

TRUTH TABLE

MODE	CS/$\overline{CS}$	OE/$\overline{OE}$	BHE	D_{15}/A-1	DATA	OPERATION
Not Selected	L/H	X	X	X	High-Z	Standby
Output Disable	H/L	L/H	X	X	High-Z	Active
Read	H/L	H/L	H	Output	D_0-D_{15}	Active
			L	Input	D_0-D_7	Active

NOTE : 1. X=L or H

DC CHARACTERISTICS
(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	HY234100		UNIT
			MIN	MAX	
$\vert I_{LI} \vert$	Input Leakage Current	V_{IN}=0 to V_{CC}	–	10	μA
$\vert I_{LO} \vert$	Output Leakage Current	V_{OUT}=0 to V_{CC}	–	10	μA
I_{CC}	Operating Current	f=6.7MHz, $\overline{CS}$=$\overline{OE}$=V_{IL} All D_{OUT}=open	–	50	mA
		f=1MHz, $\overline{CS}$=$\overline{OE}$=V_{IL} All D_{OUT}=open	–	20	mA
I_{SB1}	Standby Current (TTL)	$\overline{CS}$=V_{IH}, All D_{OUT}=open	–	2	mA
I_{SB2}	Standby Current (CMOS)	$\overline{CS}$=V_{CC}, All D_{OUT}=open	–	100	μA
V_{OH}	Output High Voltage	I_{OH}=–1mA	2.4	–	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA		0.4	V

AC CHARACTERISTICS

(V_{CC}=5V± 10%, T_A=0°C to 70°C)

SYMBOL	PARAMETER	HY234100-15		HY234100-20		HY234100-25		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	150	–	200	–	250	–	ns
t_{AA}	Address Access Time	–	150	–	200	–	250	ns
t_{ACS}	Chip Select Access Time	–	150	–	200	–	250	ns
t_{OE}	Output Enable Time	–	70	–	80	–	100	ns
t_{DH}	Data Hold Time	10	–	10	–	10	–	ns
t_{DF}	Data Floating Time	–	60	–	80	–	100	ns

CAPACITANCE

(V_{CC}=5V±10%, T_A=0°C to 70°C, f=1 MHz)

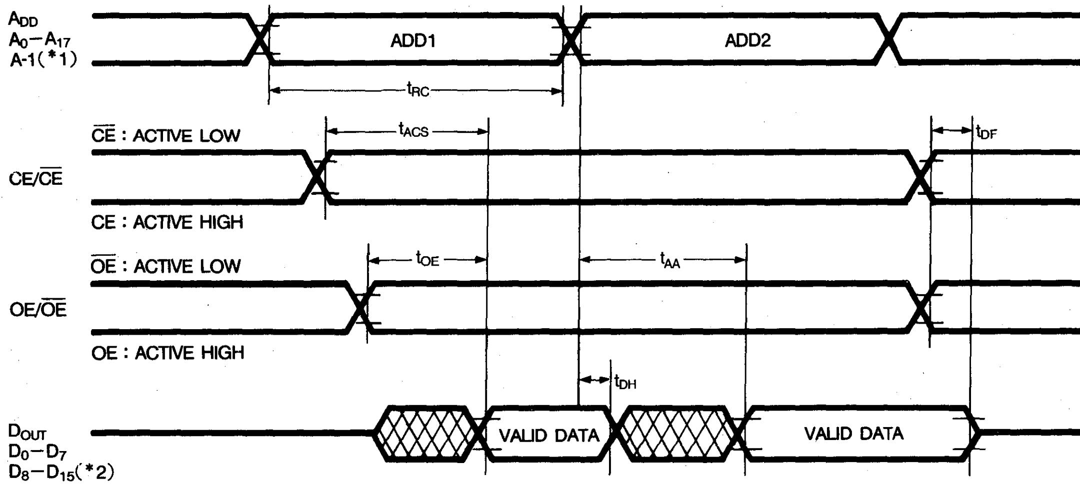
SYMBOL	PARAMETER	TEST CONDITION	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	–	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	–	10	pF

AC TEST CONDITIONS

Input Pulse Level	0.6 to 2.4V
Input rise/fall time	10ns
Input reference level	0.8V and 2.0V
Output load	1 TTL Gate and C_L=100PF

TIMING DIAGRAMS

READ CYCLE



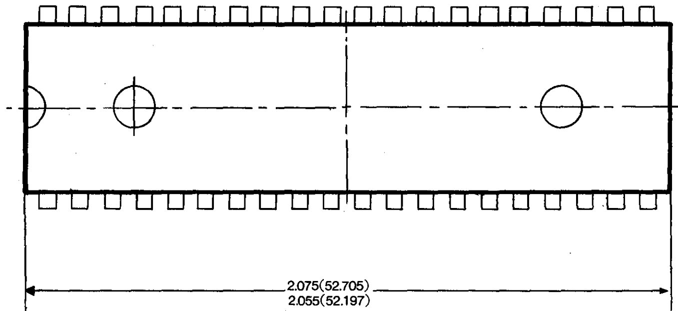
NOTES :
(*1) Byte Mode only. A-1 is Least Significant Bit Address.(BHE=V_{IL})
(*2) Word Mode only. (BHE=V_{IH})

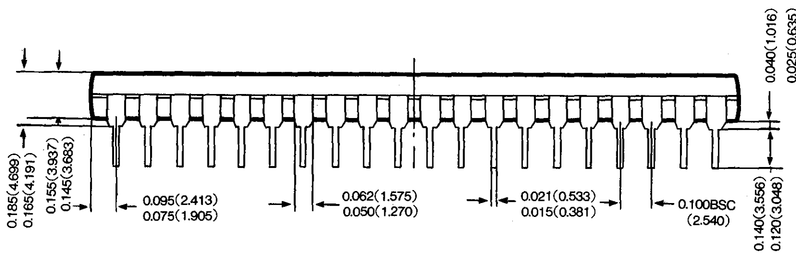
6

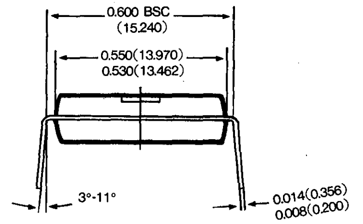
PACKAGE INFORMATION

• **40 PIN PLASTIC DUAL IN LINE PACKAGE−600 MIL**

UNIT : INCH(mm) MAX/MIN







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EEPROM DATA SHEETS 7

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HYUNDAI SEMICONDUCTOR

HY93C46

64 × 16-Bit CMOS SERIAL EEPROM

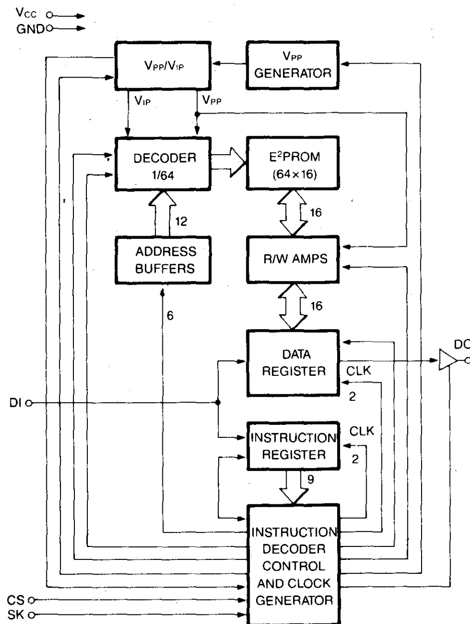
M311201B-APR91

DESCRIPTION

The HY93C46 is a 1,024-bit non-volatile memory organized as 64 registers of 16 bits each. Data can be written into or read out serially by most microprocessors or microcontrollers. Data is stored in a floating-gate cell with long data retention capability until updated by an erase or write cycle. The HY93C46 has been designed for applications requiring up to ten thousand erase/write cycles per register. Fabricated using advanced CMOS EEPROM technology, the HY93C46 offers very low power consumption. A standby mode is provided by chip select input (CS) to further reduce the power consumption by over 80%.

And to satisfy our customer's requirement, SO package is avaliable.

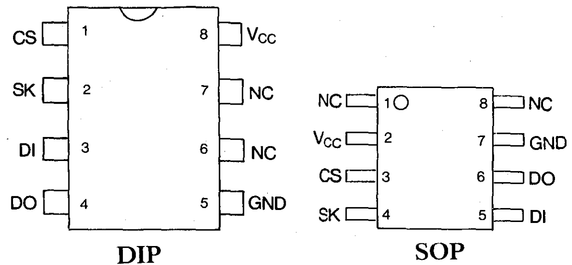
BLOCK DIAGRAM



FEATURES

- CMOS Technology
- Low cost
- TTL compatible
- 5V only erase and write(5V ± 10%)
- 64×16 serial read/write memory
- Simple interfacing
- Low standby power
- Reliable floating-gate technology
- Self-timed programming cycle
- Device status signal
- Compatible with NMC9346/COP495
- Long data retention (10 years)
- 8 pin 300 mil P-DIP and 150 mil SOP

PIN CONNECTIONS



PIN DESCRIPTION

SK	Serial Clock : External user clock shifts data into or out of the HY93C46.
CS	Chip Select : Enables internal logic when high. Note CS must be brought low between instruction.
DI	Serial Data In : Data bits and instructions are shifted in through this pin under control of SK and CS.
DO	Serial Data Out : Data is shifted out from this pin under SK and CS control. DO is active during data output(READ) or while checking status (See WRITE/ERASE Cycles). It is in high impedance state at all other periods.
V_{CC}	Power Supply(+5V)
GND	Ground
NC	No Connection

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER		RATING	UNIT
V_{TERM}	Voltage on Any Pin Relative to GND		−0.3 to 6.5	V
T_A	Ambient Operating Temperature	Standard	0 to 70	℃
		Extended	−40 to 85	℃
T_{STG}	Ambient Storage Temperature		−55 to 150	℃

NOTE :
1. Exceeding these ratings could cause permanent damage to the device. These are stress ratings only and functional operation of this device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS
(T_A=0℃ to 70℃, V_{CC}=5V±10%, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CC}	Operating Current	V_{CC}=5.5V, CS=V_{IH}, SK=V_{IH}		3	mA
	(Program and ERAL modes)	V_{CC}=5.5V		3	mA
I_{CCSB1}	Standby Current TTL Levels	V_{CC}=5.5V, CS=V_{IL}, SK=V_{IH}, DI=V_{IL}, V_{IH}=2.4V, V_{IL}=0.8V		1	mA
I_{CCSB2}	Standby Current CMOS Levels	V_{CC}=5.5V, CS=V_{IL}, SK=V_{IH}, DI=V_{IL}, V_{IH}=5.2V, V_{IL}=0.3V		400	µA
V_{IL}	Input Voltage Low		−0.1	0.8	V
V_{IH}	Input Voltage High		2.0	V_{CC}+1	V
V_{OL}	Output Voltage Low	I_{OL}=2.1mA		0.4	V
V_{OH}	Output Voltage High	I_{OH}=−0.4mA	2.4		V
$\vert I_{LI} \vert$	Input Leakage Current	V_{IN}=GND to V_{CC}		10	µA
$\vert I_{LO} \vert$	Output Leakage Current	V_{OUT}=GND to V_{CC}, CS=0V		10	µA

AC CHARACTERISTICS
(T_A=0℃ to 70 ℃, V_{CC}=5V±10%)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{SK}	Serial Clock Frequency		0	250	KHz
t_{SKH}	Clock High Time (2)		1		µs
t_{SKL}	Clock Low Time(2)		1		µs
t_{CSS}	Chip Select High to Serial Clock High Delay		200		ns
t_{CSH}	Serial Clock Low to Chip Select Low Delay		0		ns
t_{DIS}	Data Setup Time(WRITE)		400		ns
t_{DIH}	Data Hold Time(WRITE)		400		ns
$t_{PD0,1}$	Serial Clock to Output Delay	V_{OL}=0.8V, V_{OH}=2.0V, C_L=100PF V_{IL}=0.45V, V_{IH}=2.4V		2	µs
$t_{E/W}$	Self-Timed Program Cycle			10	ms
t_{CS}	Min. CS Low Time (3)		1		µs
t_{SV}	CS High to Status Valid Delay	C_L=100pF		1	µs
t_{OH}, t_{1H}	Falling Edge of CS to DO High-z			400	ns

NOTES :
2. The SK frequency spec. specifies a minmum SK clock period of 4 µs, therfore in an SK clock cycle $t_{SKH}+t_{SKL}$ must be greater than or equal to 4 µs. e.g., if t_{SKL}=1µs then the minimum t_{SKH}=3µs in order to meet the SK frequency specification.
3. CS must be brought low for a minimum of 1µs (t_{CS}) between consecutive instruction cycles.

INSTRUCTION SET FOR HY93C46

INSTRUCTION	START BIT	OPCODE	ADDRESS	DATA	COMMENTS
READ	1	10	$A_5, A_4, A_3, A_2, A_1, A_0$		Read Register $A_5, A_4, A_3, A_2, A_1, A_0$
WRITE	1	01	$A_5, A_4, A_3, A_2, A_1, A_0$	D_{15}-D_0	Write Register $A_5, A_4, A_3, A_2, A_1, A_0$
ERASE	1	11	$A_5, A_4, A_3, A_2, A_1, A_0$		Erase Register $A_5, A_4, A_3, A_2, A_1, A_0$
EWEN	1	00	11xxxx		Erase/Write Enable
EWDS	1	00	00xxxx		Erase/Write Disable
ERAL	1	00	10xxxx		Erase All Registers
WRAL	1	00	01xxxx	D_{15}-D_0	Write All Registers

FUNCTIONAL DESCRIPTION

The HY93C46 is a small peripheral memory intended for use in applications which require non-volatile storage of data. The HY93C46 is organized as 64 registers of 16 bits. Seven 9-bit instructions control the read, write and erase operations of the device. The HY93C46 operates on 5V(± 10%)supply. The high voltage required for programming is generated by an on-chip circuit which is enabled only during the write, erase, and chip erase modes to prevent spurious programming during other modes. The data out(DO) pin is also used as the status pin during self-timed programming cycles to indicate the ready/busy status of the device. All operations of the HY93C46 begin with the loading of an instruction to the device. Each of the 7 instructions has a logical "1" as a start bit, two op code bits followed by 6 bits of address.(See instruction set table for the HY93C46)

READ

After a read instruction is received, the data stored in the register specified by the address fields of the read instruction is transferred to a 16-bit serial shift register. Data can be shifted out through the DO pin by applying the clock pulses to the Serial Clock (SK) input. Note that a dummy bit(logical"0") precedes the 16-bit data output string. The data at the Data Out pin changes on the low to high transition of the serial clock.

ERASE/WRITE ENABLE AND DISABLE

On power-up, the HY93C46 is set to the programming disable state. In order to program the device, it must be set to the programming enable state by executing an EWEN instruction. After data is written into the device, an EWDS instruction may be executed to prevent accidental programming of the HY93C46. The read instruction, however, is independent of the device's programming state.

ERASE[(4)]

The registers in the HY93C46 must be erased (all bits set to logical "1") before new data can be written into the registers. After the erase instruction is loaded into the HY93C46, Chip Select(CS) must be pulled low. The falling edge of this signal initiates the self-timed programming cycle. If CS is brought high after a time equal to t_{CS}, the DO pin will indicate the ready/busy status of the device. The DO pin will remain low as long as the HY93C46 is still in the programming mode, and the return of this signal to logical "1" indicates the device is now ready for the next instruction. The register erase instruction (ERASE) will erase the data in the register that is addressed by the address field of the instruction. Chip Erase instruction (ERAL) will cause all registers in the device to be erased.

WRITE[4]

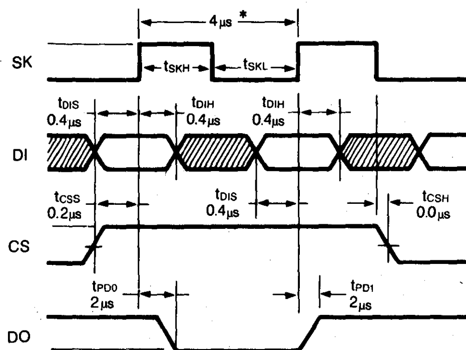
After a write instruction is loaded into the HY93C46 16 bits of data must also be loaded into the device. After the last bit of data is loaded, Chip Select (CS) must be brought low before the next rising edge of the serial clock. The high to low transition of CS will initiate a programming cycle to the register whose address was specified in the write instruction. If CS is again allowed to return to logical "1" after t_{CS}, DO can be examined for the ready/busy status of the device. Note that the register to be written into must have its data previously erased. The chip write instruction (WRAL) is normally used only by the manufacturer to guarantee write/erase endurance of the chip during test.

NOTES :
4. During a programming mode(write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the selftimed programming cycle and starus check.

AC TEST CONDITIONS

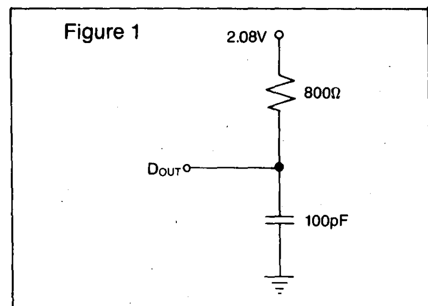
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10ns Max.
Timing Measurement Levels : Input	1.5V
Output	1.5V
Output Load	See Figure 1

TIMING DIAGRAMS
SYNCHRONOUS DATA TIMING



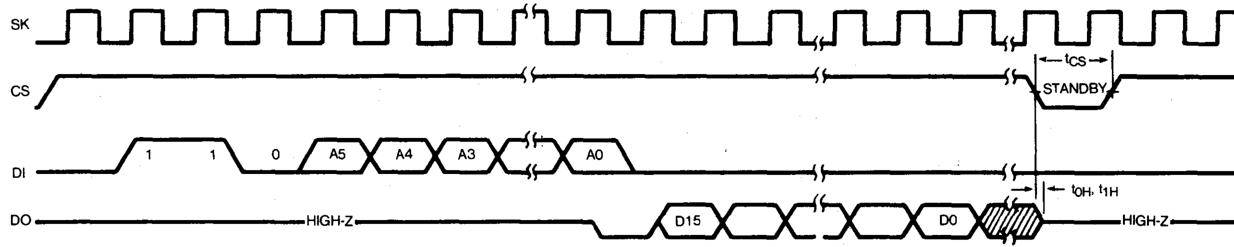
* This is the minimum SK period.

EQUIVALENT AC TEST CIRCUIT

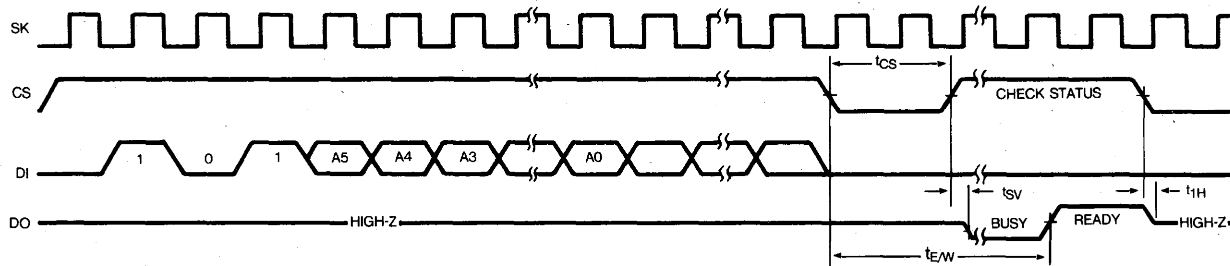


TIMING DIAGRAMS

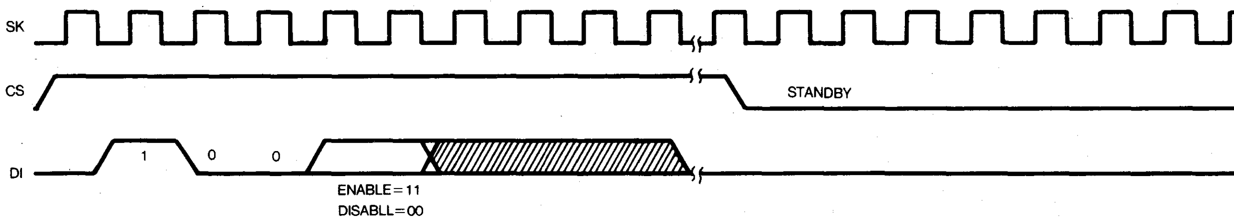
READ



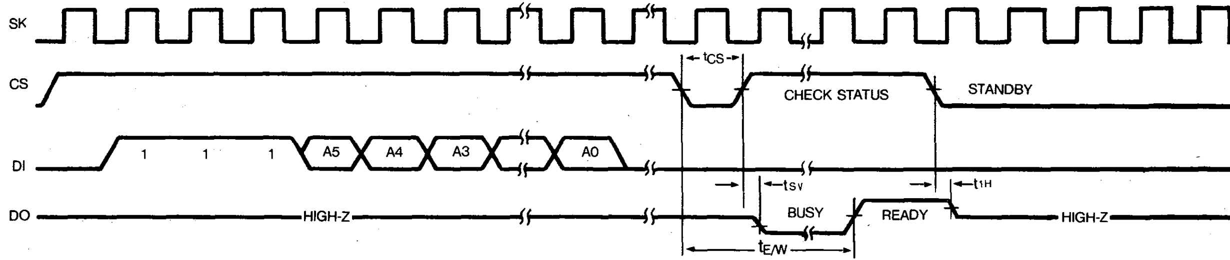
WRITE



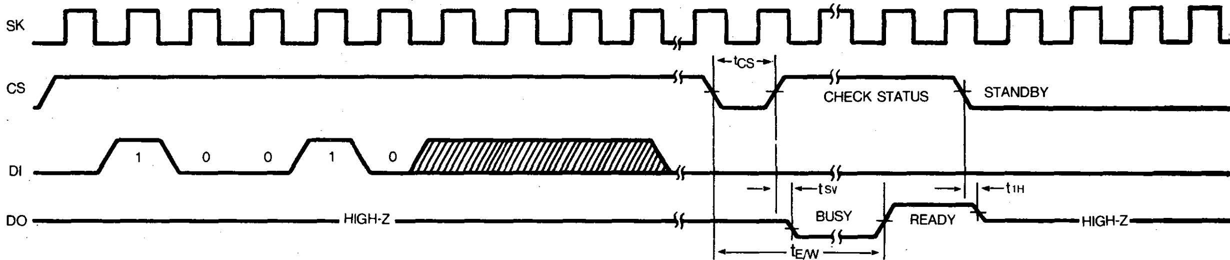
EWEN/EWDS



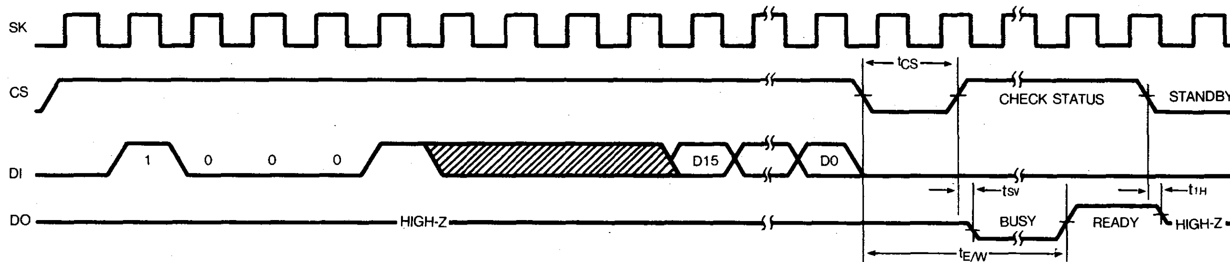
ERASE



ERAL

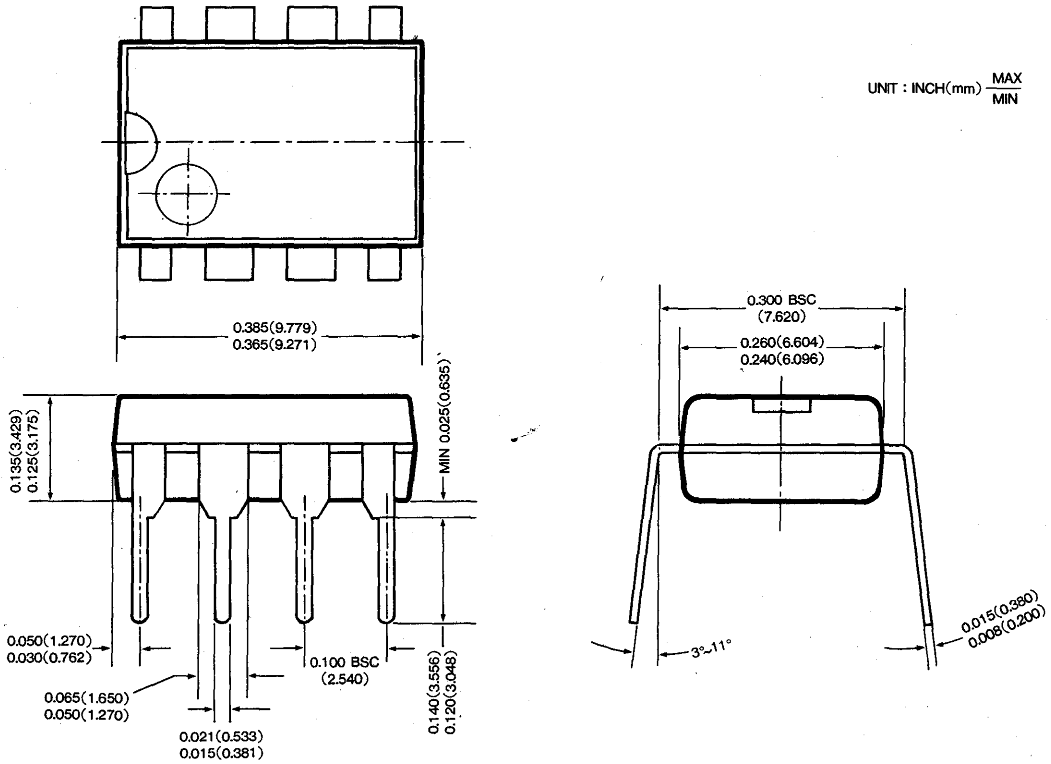


WRAL

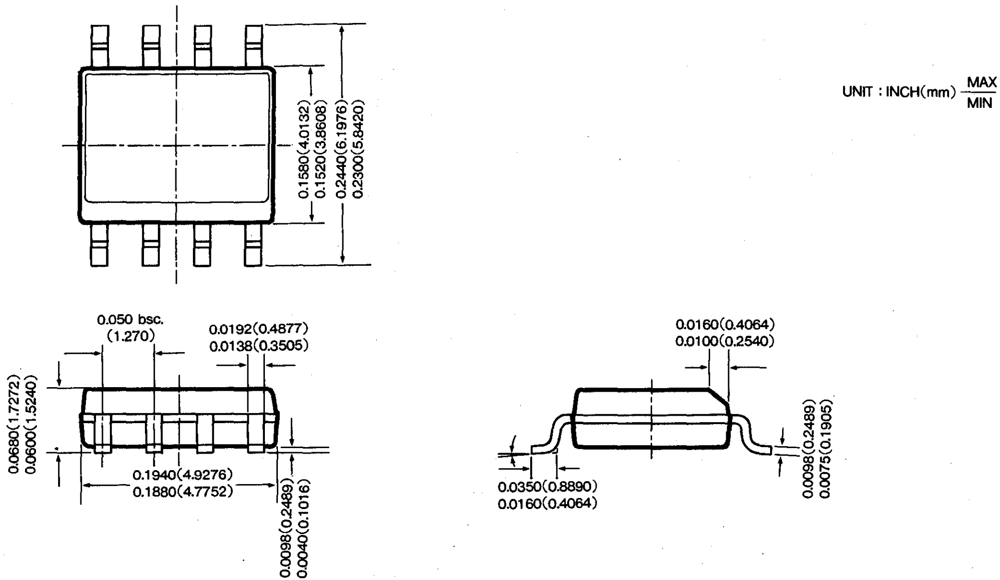


PACKAGE INFORMATION

- 8 PIN PLASTIC DUAL IN LINE PACKAGE−300 MIL



- 8 PIN SMALL OUTLINE PACKAGE−150 MIL



7

MEMO

DESCRIPTION

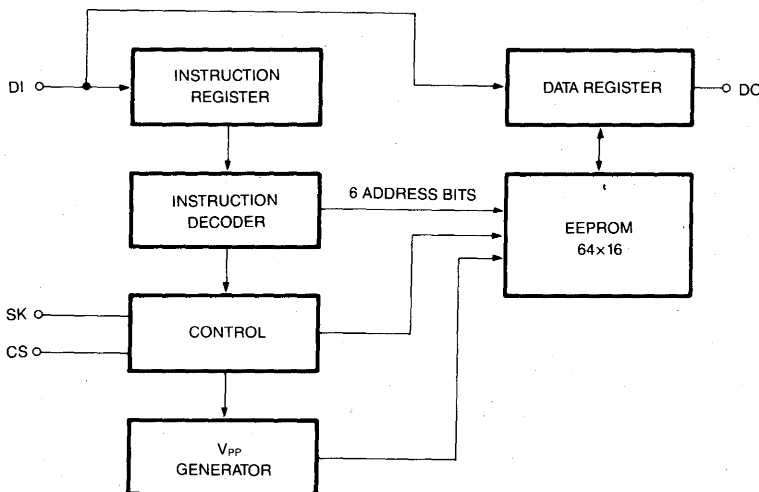
HYUNDAI's HY93C46 serial EEPROM provides a practical solution to a number of typical problems encountered in some microprocessor applications. These problems include ; the loss of data during a power shut-down, the absence of external address and data buses, the need for additional batteries and the meeting of special power on/off requirements.

Typical byte wide EEPROMs require a separate address bus and data bus to interface with a MPU. Most single-chip microcomputers have no external data or address bus, and often require non-volatile storage of data in the event of a power shut-down, whether planned or unplanned. One solution is to employ a single chip microcomputer with a power down standby mode for its on-chip RAM. However, this solution requries an additional battery and is inherently low inreliability and longevity, and has special power on/off requirements.

The HY93C46 is a 1,024-bit electrically erasable PROM with 64-registers of 16-bits. Because data is written in or read out from the device serially, no address bus or data bus is required – resulting in a low pin count package (8 pin DIP), and easy interface with any microprocessor-based system via I/O ports of a MPU.

The HY93C46 is fabricated in floating-gate CMOS EEPROM technology for very low power consumption between 33%–50% of typical NMOS devices. Deselecting the device will further reduce power consumption more than 80%, about 10% of NMOS standby current. The HY93C46 operates on 5V±10% power supply. High voltage required for programming is generated on-chip and controlled by internal logic.

Figure 1. Functional Block Diagram



7

PIN DESCRIPTIONS

SK-Serial clock : Clock generated externally by user for shifting data into or out of the HY93C46

CS-Chip select : When high enables the internal logic of the device. Note that CS must be brought low between instructions.

DI-Data in : Serial data a input; instructions and data bits shift in from this pin under the control of SK and CS.

DO-Data out : Serial data output; data is shifted out from this pin under control of SK and CS. DO is also used to monitor the ready/busy status of the device. DO is active only during data output or during the status checking period of WRITE/ERASE cycles. It is in high impedance state during all other periods.

FUNCTIONAL DESCRIPTION

The HY93C46 has seven instructions, which are 9-bits in length(see instruction set table for the HY93C46).

Each 9-bit instruction begins with a "1" as the start bit. The HY93C46 has 2 opcode bits and 6 address bits for READ, WRITE, and ERASE;or it has 4 opcode bits(2 imbedded in the address field) for the remaining instructions (ERASE/WRITE enable and disable. ERASE /WRITE all Register.) The address bits become dont't cares for these four instructions. On power-up, the HY93C46 is set to the programming disable state. This protects the device from accidental ERASE or WRITE during system power-up. To execute a WRITE or ERASE instruction, an EWEN(erase/write enable) instruction must be executed first. After data is written into the device, an EWDS instruction may be executed to disable the erase/write logic and prevent accidental programming.

READ

To read data out of the HY93C46, first shift in the 9-bit instruction. The address of the desired memory location is encoded in the address field of the read instruction. Note that the chip select pin(CS) must be brought low for a minimum of 1μs between consecutive instruction cycles to synchronize the internal logic of the device. To reduce the possibility of accidental programming, execute an EWDS instruction after each write operation and deselect the device(CS low) after each operation. Note further that data placed on the DI pin must be stable and satisfy the data setup time for the device (400ns), before the low-to-high transition of the serial clock (SK) input.

After the last address bit is shifted into the HY93C46, data from the memory location will be transferred to the data shift register and will be ready to be shifted out under the control of the shift clock(SK). A dummy "0" bit always preceeds the 16-bit output data. This dummy bit will be placed on the DO pin after the low-to-high transition of SK input for the last bit of the instruction and should be ignored. Start reading the first data bit that is shifted out after the next low-to-high transition of SK(see Figure 2).

ERASE

When the HY93C46 is erased, memory bits are set to logic "1"(i.e., reading an earsed memory location will get 16 ones). To erase a memory location, shift in the ERASE instruction with the address field set to the desired memory location address. After the last address bit is shifted in, drop CS to start the self-timed erasing cycle. In order to verify completion of the ERASE operation, raise CS again after tcs(1μs min.). The DO pin will output the device status. A low level indicates the device is busy. After approximately 10ms, the DO pin will change from a low level to a high level, indication the device has completed the ERASE cycle. CS should then be set to a low level, ready for loading of the next instruction. The sequence for erasing a memory is as follows, assuming

the erase/write enable instruction (EWEN) has been executed :

1. Set CS high(assuming CS is low when not accessing the HY93C46.)
2. Shift in ERASE instruction with the correct address.
3. Set CS low.
4. Set CS high, after minimum of 1μs.
5. Monitor DO pin;a change from low to high indicates the ERASE cycle is completed.

The "erase all" (ERAL) instruction is executed in the same manners as "erase register"(ERASE), except that the address bits of the instruction are don't care. Note that 9 bits are still needed to shift into the HY93C46 for those instrucations which have a don't care address field.

INSTRUCTION SET FOR HY93C46

INSTRUCTION	START BIT	OPCODE	ADDRESS	DATA	COMMENTS
READ	1	10	$A_5, A_4, A_3, A_2, A_1, A_0$		READ Register $A_5, A_4, A_3, A_2, A_1, A_0$
WRITE	1	01	$A_5, A_4, A_3, A_2, A_1, A_0$	D_{15}-D_0	WRITE Register $A_5, A_4, A_3, A_2, A_1, A_0$
ERASE	1	11	$A_5, A_4, A_3, A_2, A_1, A_0$		ERASE Register $A_5, A_4, A_3, A_2, A_1, A_0$
EWEN	1	00	11xxxx		ERASE/WRITE Enable
EWDS	1	00	00xxxx		ERASE/WRITE Disable
ERAL	1	00	10xxxx		Erase All Registers
WRAL	1	00	01xxxx	D_{15}-D_0	Write All Registers

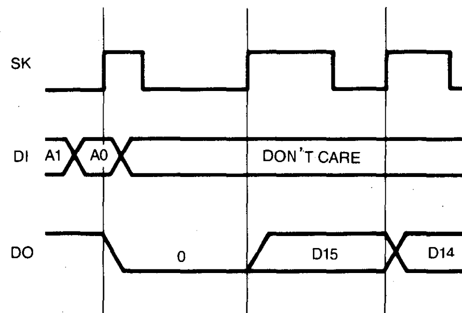
WRITE

After the 9-bit write instruction is shifted in, an additional 16 bits of data to be stored must be shifted in. After the last bit of data is loaded, chip select(CS) should be set low to initiate the WRITE cycle. The internal programming voltage generator will be turned on, and the programming will be finished in about 10ms. The ready/busy status of the HY93C46 can be read similar to the erase operation – through the DO pin, by returning the CS pin to high after the WRITE cycle is started.

The sequence for writing 16 bits of data into the HY93C46 can be summarized as follows, assuming that erase/write(EWEN) is already enabled :

1. Set CS high to enable the device.
2. Shift in the WRITE instruction with the address of the memory location to be modified.
3. Shift in the 16-bit data to be stored in that location.
4. Set CS low to initiate the WRITE cycle.
5. Set CS high again after 1μs or more, to monitor the ready/busy status.

Figure 2. Read Operation Timing



1. SK does not have to be symmetrical or regular, as long as it satisfies the data sheet limits.
2. After the last bit of instruction is shifted in, logic level at the DI pin will not affect internal operation.
3. Data(not the instructions) can be shifted into the HY93C46 MSB first or into LSB first;data shifted out from DO will be in the same order.

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6. Monitor DO pin;a change from low to high indicates the write cycle is completed.

The "write all" instruction(WRAL) is similar to the WRITE instruction, except that the address field of the instruction is ignored, and the 16-bit data that follows the instruction will be written to all memory locations. Note that a location should be erased before new data can be written in. Erasing is recommended before writing to a previously written memory location, but it is possible to change data. Writing is a uni-directional operation;bits that are 1 may be changed to 0 only. For example, if an address contains FFF0(hex), then bits 15 to 4 may to changed. Data FFF0 could be writen as FF70, FF30, FF10, and FF900 sequentially, without intervening erasures. Note that all 16 bits must be specified at each write, even if the data remains the same.

POWER REQUIREMENTS

The on-chip programming voltage generator is only turned on during WRITE or ERASE instructions. During these periods, the operation current will increase to a few milliamperes.

The HY93C46 will consume much less power when executing an instruction that does not require programming voltage—and even lower power consumption when the device is deselected. We recommend that a decoupling capacitor of 0.1μF or higher be placed between V_{CC} and GND near the device.

INTERFACING EXAMPLE

The HY93C46 can interface with most micro processor systems with only four connections in addition to power and ground. The following illustrated the connections to the 6500/1, 8051, and 6805 microcontrollers, and the 6522, 8255 peripheral I/O ports.

Figure 3. Interfacing with 6500/1

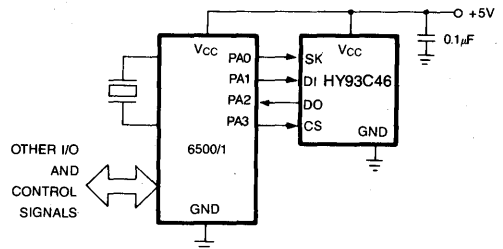


Figure 4. Interfacing with 8051

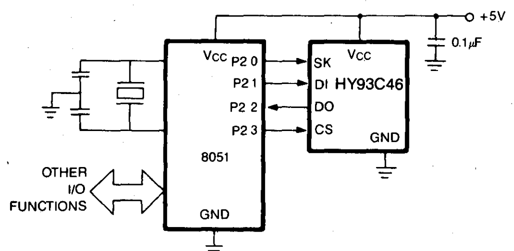


Figure 5. Interfacing with 6805

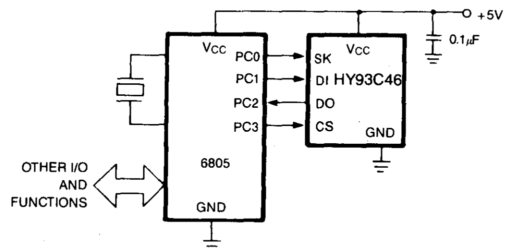


Figure 6. Interfacing with 6522

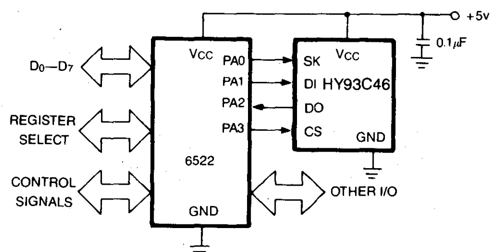
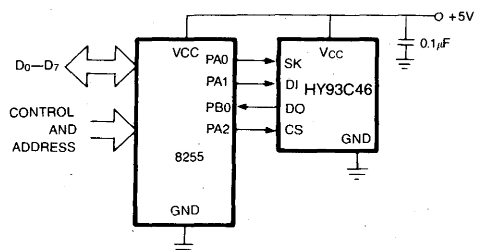
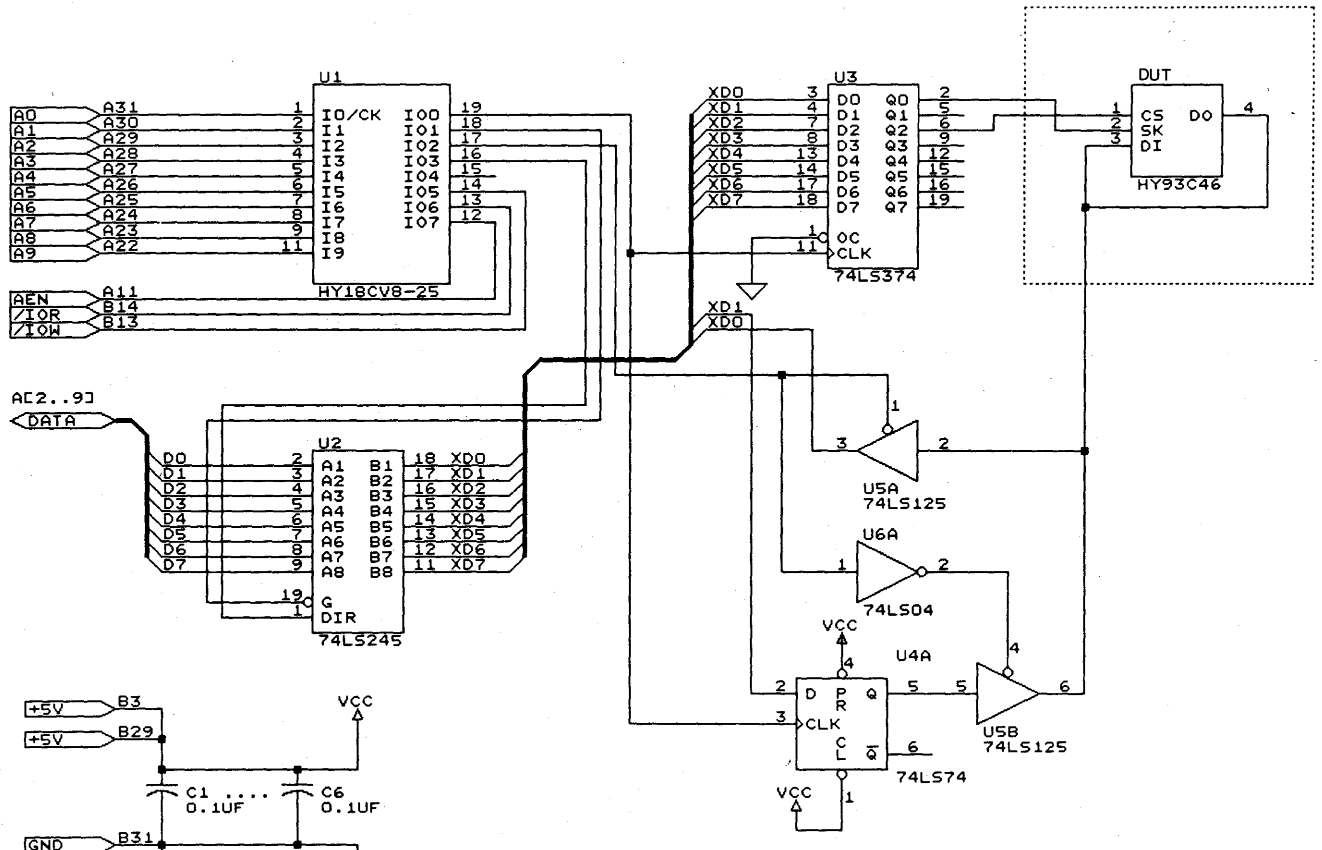


Figure 7. Interfacing with 8255 (mode 0, control word 2)



HY93C46 EVALUATION CIRCUITRY

SCHEMATIC



ADDRESS DECODER EQUATION SOURCE FILE FOR ABEL™ 3.0

```
module _decodel
title 'Address Decoder for HY93C46 Evaluation Board
Design by H.S.Cho - HEI Application Engineer
Dec. 13,1989
This address decoder logic implemented to HY18CV8 of the HEI EEPLD.

ul               device   'p18cv8';

a0,a1,a2,a3,a4   pin      1,2,3,4,5;
a5,a6,a7,a8,a9   pin      6,7,8,9,11;
aen              pin      12;
ior              pin      13;
iow              pin      14;

dec374           pin      19;
dec74            pin      18;
dec125           pin      17;
dec245           pin      16;


h,l,z = 1,0,.z.;
ioadd = [a9,a8,a7,a6,a5,a4,a3,a2,a1,a0];


equations

!dec374 = (ioadd == ^h300) & !aen ;
!dec74  = (ioadd == ^h300) & !aen;
!dec125 = (ioadd == ^h301) & !aen;
!dec245 = (ioadd == ^h300) # (ioadd == ^h301) & !aen & !ior;


test_vectors  'Test address decoder '

([aen,ioadd,ior,iow] -> [dec374,dec74,dec125,dec245])
 [ l ,^h300, h , h ] -> [  l    , l    ,  h    ,    l  ];
 [ l ,^h301, h , h ] -> [  h    , h    ,  l    ,    h  ];
 [ l ,^h301, l , h ] -> [  h    , h    ,  l    ,    l  ];

end _decodel
```

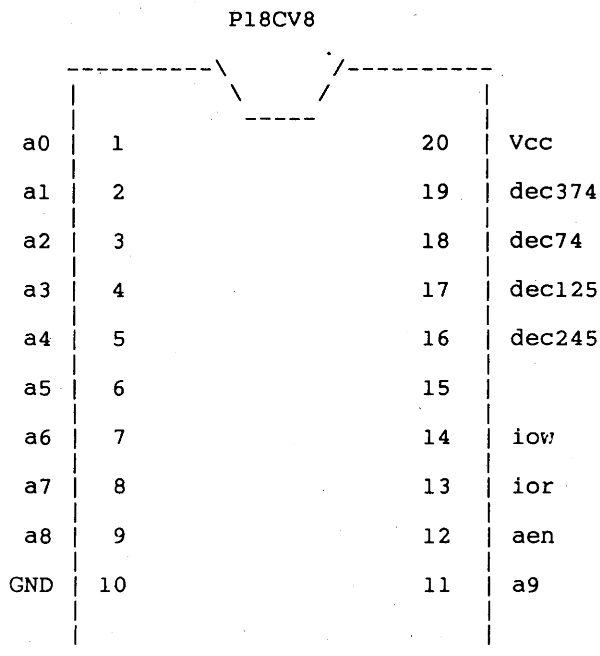
ADDRESS DECODER DOCUMENT FILE

```
ABEL(tm) 3.00a  -  Document Generator
Address Decoder for HY93C46 Evaluation Board
Design by H.S.Cho - HEI Application Engineer
Dec. 13,1989
This address decoder logic implemented to HY18CV8 of the HEI EEPLD.
Equations for Module _decode1

Device u1

- Reduced Equations:

    dec374 = !(!a0 & !a1 & !a2 & !a3 & !a4 & !a5 & !a6 & !a7 & a8 & a9 &
            !aen);

    dec74 = !(!a0 & !a1 & !a2 & !a3 & !a4 & !a5 & !a6 & !a7 & a8 & a9 &
           !aen);

    dec125 = !(a0 & !a1 & !a2 & !a3 & !a4 & !a5 & !a6 & !a7 & a8 & a9 &
            !aen);

    dec245 = !(a0 & !a1 & !a2 & !a3 & !a4 & !a5 & !a6 & !a7 & a8 & a9 &
            !aen & !ior
              # !a0 & !a1 & !a2 & !a3 & !a4 & !a5 & !a6 & !a7 & a8 & a9);
```

7

ABEL(tm) 3.00a - Document Generator
Address Decoder for HY93C46 Evaluation Board
Design by H.S.Cho - HEI Application Engineer
Dec. 13,1989
This address decoder logic implemented to HY18CV8 of the HEI EEPLD.
Chip diagram for Module _decode1

Device u1



end of module _decode1

ADDRESS DECODER JEDEC FILE

```
ABEL(tm) 3.00a FutureNet Div, Data I/O Corp.  JEDEC file for: P18CV8
Created on:
Address Decoder for HY93C46 Evaluation Board
Design by H.S.Cho - HEI Application Engineer
Dec. 13,1989
This address decoder logic implemented to HY18CV8 of the HEI EEPLD.*
QP20* QF2696* QV4*
L0000
100110111011101110111011101110110110
000000000000000000000000000000000000
000000000000000000000000000000000000
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100110111011101110111011101110110110
000000000000000000000000000000000000
000000000000000000000000000000000000
000000000000000000000000000000000000
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111111111111111111111111111111111111
111111111111111111111111111111111111
000000000000000000000000000000000000
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000000000000000000000000000000000000
000000000000000000000000000000000000*
L2664
1011
1011
1011
1011
0000
0000
0011
0011*
N Test address decoder *
V0001 000000001N1011XLHLLN*
V0002 100000001N1011XHLHHN*
V0003 100000001N1001XLLHHN*
C25E2*
7A84
```

FREE EVALUATION SOFTWARE

A HY93C46 evaluation software (IBM PC compatible) is available now. The program can be used for reading data from, modifying the data basis on bit, writing data into the HY93C46. Also, it is useful for you to verify data endurance test from 1 to 65,535 cycles. All the instructions in this sheet can be applicable to the HY93C46. When you need this program, contact to your nearest HYUNDAI representatives or distributors, or Semiconductor Application Engineering in Semiconductor Marketing & Sales Division.

- **ABEL is trademark of DATA I/O Corporation**
- **IBM is registered trademark of IBM Corporation**

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HYUNDAI SEMICONDUCTOR

HY18CV8

CMOS EEPLD

L111202B-JAN92

DESCRIPTION

The HY18CV8 is a CMOS Electrically Erasable Programmable Logic Device (EEPLD) that provides a high performance; low power, reprogrammable and architecturally flexible alternative to conventional programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the performance of the HY18CV8 rivals speed parameters of standard bipolar PLDs with a dramatic improvement in power consumption. The electrically erasable reprogrammable technology of the HY18CV8 not only reduces development and field retrofit cost but enhances testability enabling HYUNDAI to ensure 100% field programmability and function. Packaged in a cost effective "window-less" 20 pin DIP, the flexible architecture of the HY18CV8 allows for replacement of standard SSI/MSI logic circuitry or pin-out compatible emulation of 20 pin bipolar PAL® devices and the Altera EP310/320. In addition, over a hundred new logic configurations, not possible with earlier generation PLDs, can be implemented. Primary development and programming support of the HY18CV8 is provided by popular third-party PC based development tools and stand-alone programmers.

FEATURES

- **Advanced CMOS EEPROM Technology**
- **Low Power Consumption**
  - **CMOS : 20mA Standby +0.7mA/MHz max.**
  - **TTL : 25mA Standby +0.7mA/MHz max.**
- **High Performance**
  - **t_{PD} 25ns max., t_{CO} 18ns max., t_{SC} 20ns min.**
- **Reprogrammability**
  - **100% factory tested**
  - **Cost effective "window-less" package**
  - **3 second erase/program time**
  - **Adds convenience, reduces field retrofit and development cost**
- **Design Security**
  - **Prevents unauthorized reading or copying of design**
- **Architectural Flexibility**
  - **74 Product Term×36 Input Arrays**
  - **Up to 18 inputs and 8 I/O pins**
  - **Independently configurable I/O macro cell ; polarity, register, combinatorial, bi-directional**
  - **Synchronous preset, asynchronous clear**
  - **Independent output enables**
- **Application Versatility**
  - **Replaces SSI/MSI logic**
  - **Emulates bipolar PAL® devices and the Altera EP300/310**
  - **Replaces low density Gate Arrays**
  - **Simplifies inventory control**
  - **Allows new design possibilities**
- **Development/Programmer Support**
  - **Popular PC based development tools and programmers.**

BLOCK DIAGRAM

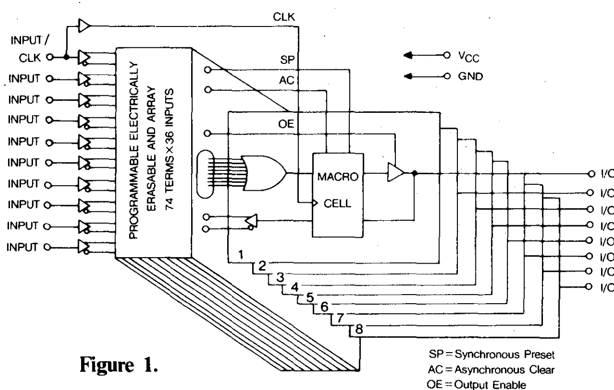
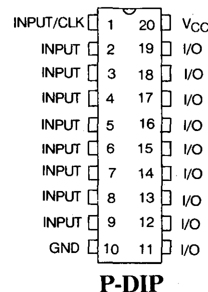


Figure 1.

PIN CONNECTIONS



P-DIP

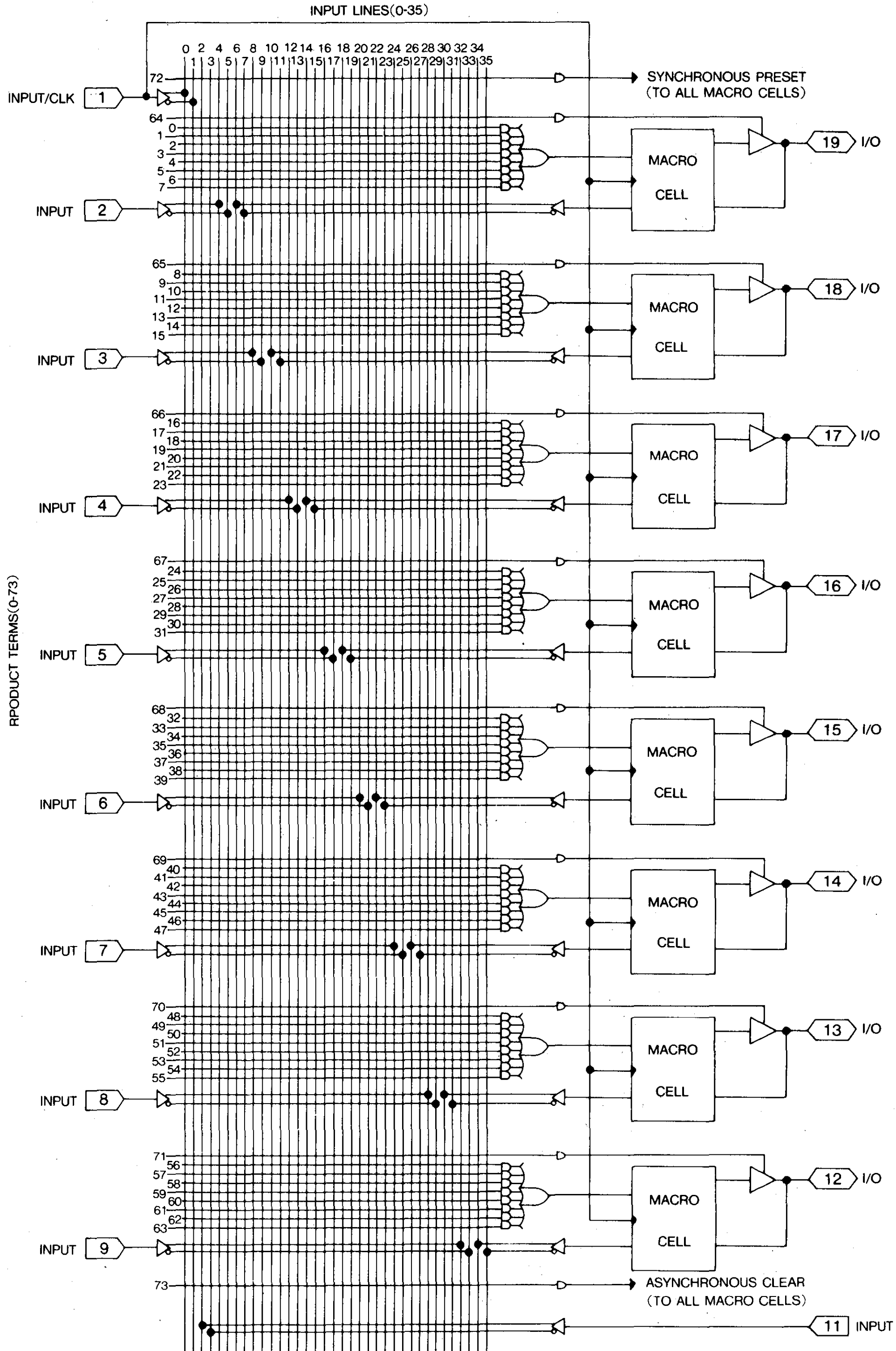
PIN NAMES

INPUT/CLK	INPUT AND/OR CLOCK
INPUT	INPUT
I/O	BI-DIRECTIONAL INPUT/OUTPUT
V_{CC}	POWER SUPPLY(+5V)
GND	GROUND

8

PAL® is a registered trademark of Advanced Micro Device, Inc.

Figure 2. HY18CV8 Logic Array Diagram



ARCHITECTURAL OVERVIEW

The basic architecture of the HY18CV8 is similar to of earlier generation PLDs to the extent that utilizes a sum-of-products logic array in a programmable AND fixed OR structure. This familiar logic arrangement allows user defined output functions to be created by programming the connection of input signals into the array. What makes the architecture of the HY18CV8 different, however, is the increased capability and flexibility it provides in a higher level of equivalent gate integration and a simplification of design.

The block diagram in figure 1. illustrates the key elements of the HY18CV8 architecture. Externally, the HY18CV8 provides up to 18 inputs and 8 outputs for use. At the core is a programmable electrically erasable "AND array" of 36 input lines by 74 product terms. The 36 input lines are derived from the true and complement of the 18 possible input pins. The 74 product terms are made up of ; 1 synchronous preset term, 1 asynchronous clear term, 8 output enable terms and 64 terms divided into groups of 8 each feeding into an OR function.

Each OR function is directly associated with one of eight macro cells and I/O pins. An individual macro cell can be programmed into one of twelve different configurations. Depending on the configuration, the output of the macro cell can be fed back into the array or output via its associated I/O pin. The configurations include various arrangements for bi-directional I/O, registered or combinatorial feedback, registered or combinatorial output and output polarity control. The output enable term of each I/O pin can be used to force a high impedance state for bidirectional I/O operations or for dedicated input usage. The synchronous preset term, asynchronous clear term and clock (pin 1. INPUT/CLK) are globally routed to all macro cells.

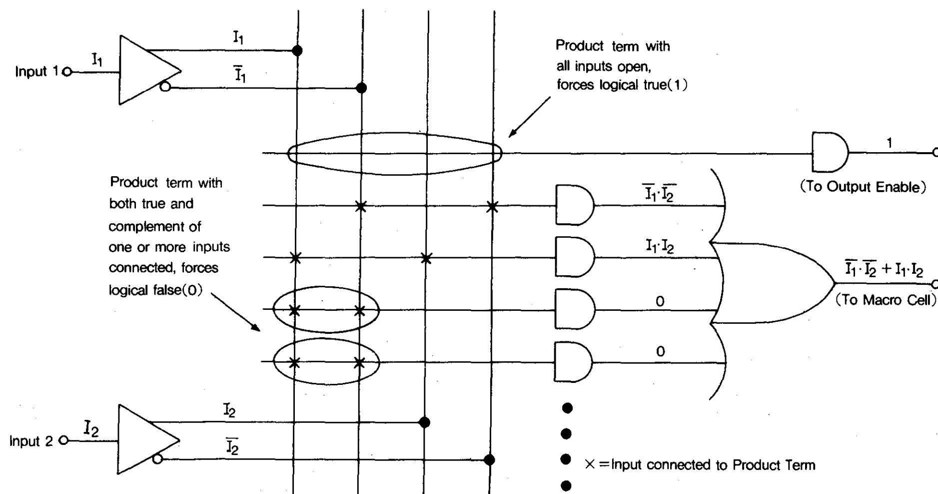
LOGIC ARRAY OPERATION

A more detailed view of the overall architecture, specifically the logic array, is illustrated by the HY18CV8 Logic Array Diagram in figure 2. As referred to previously, the logic array of the HY18CV8 consists of ;

36 Input Lines :
- 10 true and complement inputs
- 8 true and complement inputs/feedbacks

74 Product Terms :
- 64 product terms (8×8 Sum-of-Products terms)
- 8 output enable product terms
- 1 synchronous preset term
- 1 asynchronous clear term

Figure 3. Logic Function Implementation in HY18CV8 Array



Looking at the logic array diagram, the 36 input lines (0-35) run vertically and the 74 product terms (0-73) run horizontally. Each input line and product term intersection in the array has an associated programmable EEPROM memory cell that determines whether the intersection is connected or open. A connection allows an input line to become a logical input of the intersected product term (AND gate). Thus, each product term, although unlikely in a real application, truly equals a 36 input AND gate.

During programming of the HY18CV8, all EEPROM memory cells are first erased, opening all input line and product term intersections, specific intersections can then be selectively programmed for connection based on user defined logic functions. Figure 3 illustrates how a logic function, a 2 input exclusive NOR, is implemented in the HY18CV8 array. Note that if all true and complement inputs of product term are left open, the output of the AND gate will be a logical true (HIGH). If both true and complement of one or more inputs are connected to a product term, the output of the AND gate is forced to a logical false(LOW).

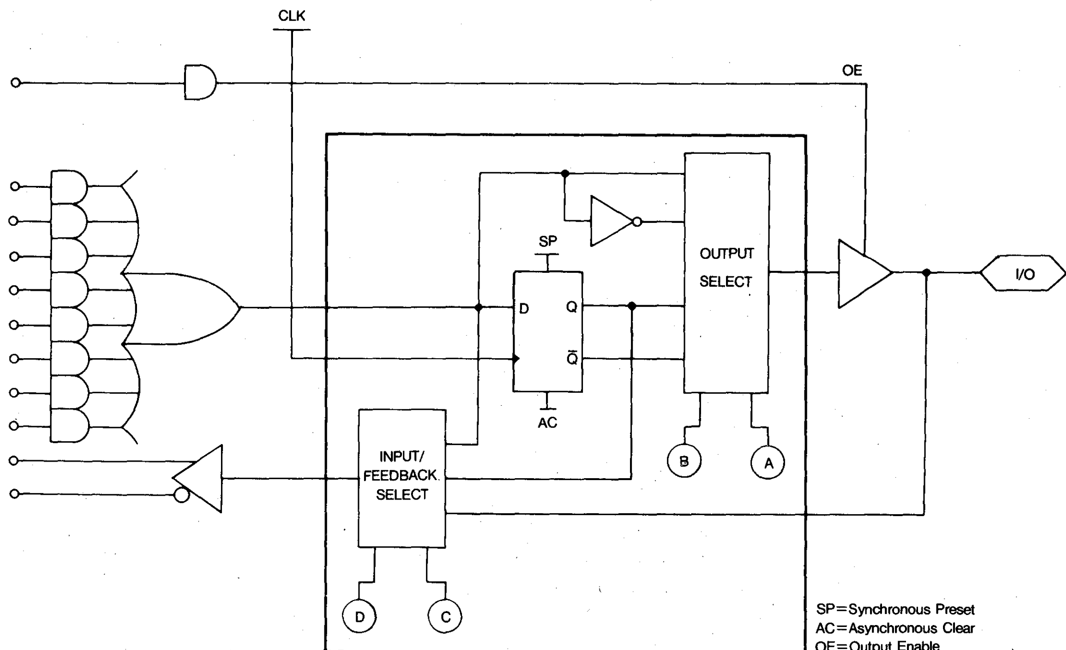
As illustrated in figure 2, the logic array has 64 product terms that are divided into groups of 8 each feeding into a sum (OR gate). By connecting specific inputs or I/O macro cell feedbacks to the product terms, complex sum-of-products logic functions can be created. Each sum feeds into its associated I/O macro cell where the logic function can be further controlled for output to an I/O pin of feedback into the array.

In addition to the 64 product terms of the 8 sum-of-product groups, there are 8 output enable product terms, 1 synchronous preset product term and 1 asynchronous clear product term. These additional terms are used to directly control specific I/O functions which are covered in the following section.

I/O MACRO CELL AND OUTPUT ENABLE OPERATION

A great amount of architectural flexibility is provided by the HY18CV8s reconfigurable I/O macro cells and independently controlled output endables. A closer look at the I/O macro

Figure 4. HY18CV8 Macro Cell Diagram



cell, figure 4, shows that it consists of a D-type flip-flop and two signal select multiplexers.

The D-type flip-flop operates similar to standard TTL D flip-flops to the extent that the D input is latched on the rising edge (LOW to HIGH transition) of the CLK input and Q or $\bar{Q}$ output signals can be used. Two additional inputs are controlled by the asynchronous clear and synchronous preset terms.

When the asynchronous clear product term is asserted (HIGH) the Q output will immediately be set to a LOW regardless of the clock state. When the synchronous preset term is asserted (HIGH) the Q output will be set to a HIGH on the following rising edge (LOW to HIGH transition) of the CLK input. Priority is given to the asynchronous clear signal if both asynchronous clear and synchronous preset have been asserted. Upon power-up, the asynchronous clear function is automatically performed setting the Q outputs of all macro cell flipflops to a LOW.

The two signal select multiplexers of each macro cell are controlled by four EEPROM programmable bits(A, B, C, and D) that determine which of the twelve possible configurations the macro cell will assume. This independent flexibility allows a single HY18CV8 to implement a combination of configurations among its eight macro cells. The configurations include various arrangements for bi-directional I/O, registered or combinatorial feedback, registered or combinatorial output and output polarity control. The twelve possible I/O macro cell configurations are listed in Table 1, Their equivalent circuits are illustated in figure 5.

Each of the 8 output enable terms can enable or disable the output of its associated I/O macro cell. When the output enable product term is a logical true (HIGH) the output signal is enabled to the I/O pin. When it is a logical false (LOW) the I/O pin is in a high impedance state. The output enable product term allow individual I/O pins to be input only or bi-directional I/O.

DESIGN SECURITY

The HY18CV8 provides a special EEPROM security bit feature that prevents unauthorized reading or copying of designs implemented. The security bit feature is typically used after a design is finalized and ready for production. The actual setting of the security bit is done via the PLD programmer used. Once set, the verify (read) and program operation using a PLD programmer or other method will not be allowed until the entire device has first been erased.

CMOS EEPROM TECHNOLOGY

The performance and flexibility provided by the HY18CV8 is primarily due to HYUNDAI's advanced CMOS EEPROM technology offering low power, high speed and nonvolatile reprogrammability. Utilizing this technology along with special design techniques, the HY18CV8 maintains the low power characteristics of CMOS while achieving the speeds of standard bipolar PLDs.

For HY18CV8 reprogrammability, Fowler Nordheim tunneling techniques are employed to trap charges onto a floating gate through a thin oxide insulator. The trapped charges remain after power has been removed allowing nonvolatility of programmed data. The charges can be removed by electrically erasing the device. Once fully eraged, it can then be reprogrammed into a new configuration.

The HY18CV8 is designed for programming endurance of up to 1000 complete erase/reprogram cycles with a data retention of 10 years, when used within the specified operating temperature range. This means that the HY18CV8 can be reprogrammed up to 1000 times without degrading device operation, and similar to other non-volatile memory technologies, the data last programmed will remain valid for ten years.

Althought implemented in EEPROM technology, often associated with in-system reprogrammable memory devices, the HY18CV8 is

programmed out-of-system via a PLD programmer. There are several other beneficial reasons, however, for using EEPROM techonlogy. Some of these benefits include ; enhanced factory testing allowing 100% programming and functional integrity, cost effective "windowless" packaging and 3 second erase/reprogram time instead of approximately 20 minutes for EPROM PLDs.

Figure 5. HY18CV8 Macro Cell Configuration Equivalent Circuits

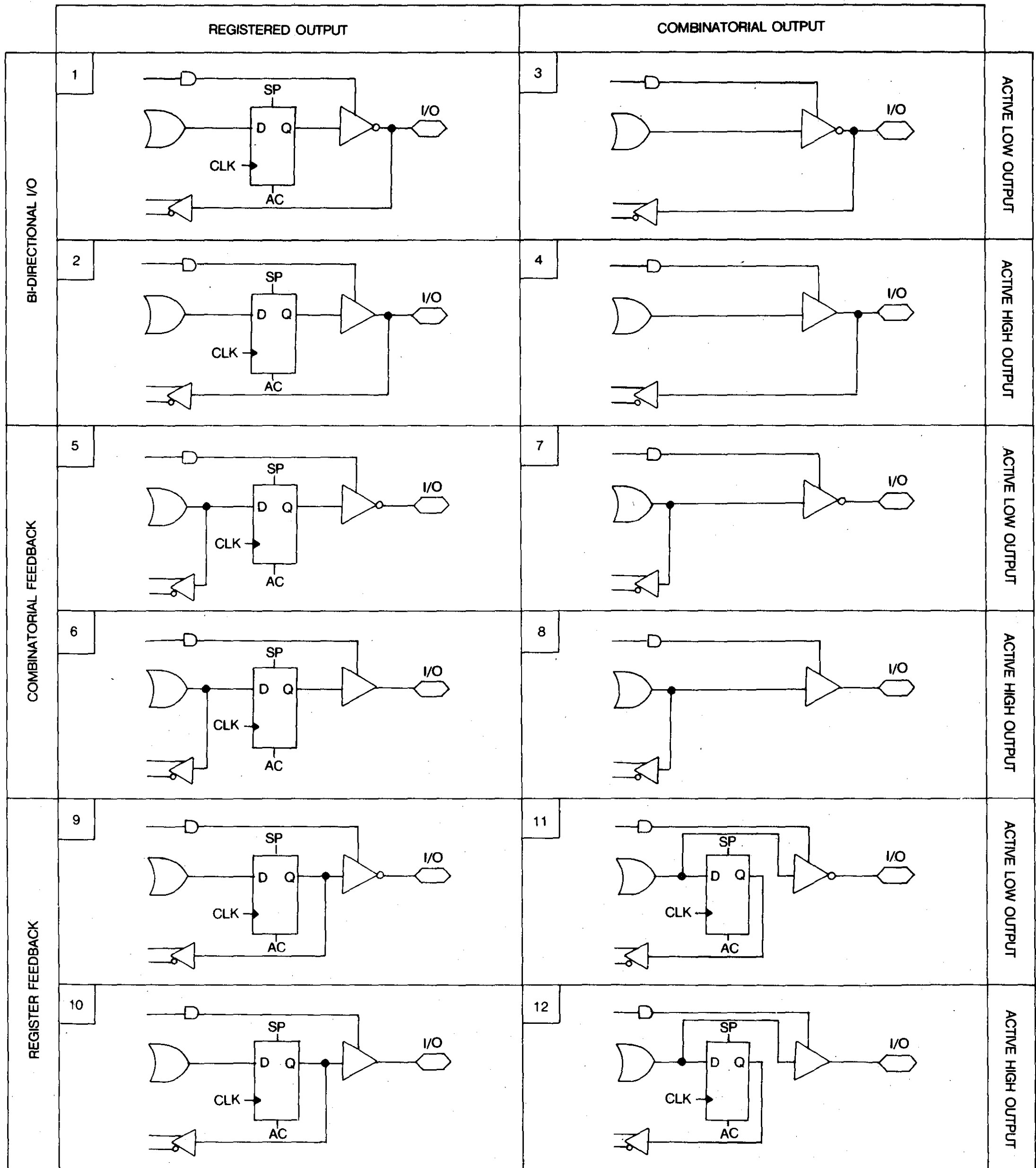


Table 1. HY18CV8 Macro Cell Configurations

CONFIGURATION					INPUT/FEEDBACK SELECT	OUTPUT SELECT	
#	A	B	C	D			
1	1	1	1	1	Bi-Directional I/O	Register	Active Low
2	0	1	1	1			Active High
3	1	0	1	1		Combinatorial	Active Low
4	0	0	1	1			Active High
5	1	1	1	0	Combinatorial Feedback	Register	Active Low
6	0	1	1	0			Active High
7	1	0	1	0		Combinatorial	Active Low
8	0	0	1	0			Active High
9	1	1	0	0	Register Feedback	Register	Active Low
10	0	1	0	0			Active High
11	1	0	0	0		Combinatorial	Active Low
12	0	0	0	0			Active High

Note : 0 – programmed, 1 – erased

APPLICATIONS OF THE HY18CV8

The versatility of the HY18CV8 makes it an effective alternative to conventional methods of logic design over a broad range of applications.

SSI/MSI logic replacement, the HY18CV8 enhances the design process with increased flexibility, higher performance, faster development time and design security. Manufacturing benefits are also realized by requiring fewer components and interconnects resulting in more efficient use of space, simplified inventory control and higher reliability.

As a bipolar PAL® replacement, the HY18CV8 has comparable speed and offers several advantages including : enhanced design flexibility, simplified inventory control, reduced power consumption, reprogrammability, and 100% factory testability for function and programming.

Design flexbility is of particular importance since the HY18CV8 not only emulates the majorty of the 20 pin PAL® devices (see table 2) but also allows functions found among several PAL® device types to be combined. In addition, completely new functions, not supported by the standard PAL® devices, can be implemented. This flexibility means a designer can focus on the design rather than on the restrictions of a fixed architecture. Reprogrammability is also a key benefit over one time programmable PAL®s. This feature adds convenience and cost savings in development prototyping and field retrofitting of systems. Converting existing PAL® designs to the HY18CV8 for plug-in replacement is easily accomplished using EEPLD evaluation or development tools.

As a design alternative to low-density gate arrays, one or more HY18CV8s offer a cost effective and low-risk option. With its architectural

Table 2. 20 pin PAL® devices that can be emulated by the HY18CV8

OUTPUT TYPE	PART NUMBER AND I/O CAPACITY							
Combinatorial – High	10H8	12H6	14H4	16H2		16H8	16HD8	
Combinatorial – Low	10L8	12L6	14L4	16L2	16L8	16LD8		
Combinatorial – Polarity							16P8	18P8
Registered – Low					16R4	16R6	16R8	
Registered – Polarity					16RP4	16RP6	16RP8	

flexibility and equivalent gate density of approximately 300 gates, designs traditionally employing low-density gate arrays can be implemented quickly at no factory development (NRE) cost. Unlike the lead times encountered with gate arrays, the HY18CV8 is off-the-shelf available. Furthermore, if a design error is made or an upgrade is necessary, the changes can simply be reprogrammed.

Similar to SSI/MSI logic, PAL®s and low density gate arrays, applications of the HY18CV8 cover all the primary areas of system design including, data processing, communications, consumer, military and transportation. Specific functions implemented using the HY18CV8 range from basic logic and system support circuitry to stand alone controllers.
Some applications include :

- **SSI/MSI Logic Replacement/Customization**
  - Random logic
  - Decoders/encoders
  - Comparators
  - Multiplexers
  - Counters
  - Shift registers
- **Processor System Support**
  - Address decoding
  - Wait-state generation
  - Memory protection
  - Memory refresh
  - DMA control
  - Interrupt control
  - Timer/counter functions
  - Bus arbitation and interface
  - Error detection and correction
- **I/O Interface and Support**
  - Intelligent I/O port
  - Data communication interface
  - Display interface
  - Keyboard scanning
  - Disk and tape drive control
  - Front panel interface
- **Stand-Alone Non μP Based Controllers**
  - Motor control
  - Sensor monitoring
  - Security access control
  - Display control

ABSOLUTE MAXIMUM RATINGS(10)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	Supply Voltage	Relative to GND	−0.5 to 7.0	V
V_I	Voltage Applied to Input(5)	Relative to GND(1)	−0.5 to 7.0	V
V_O	Voltage Applied to Output	Relative to GND(1)	−0.5 to 7.0	V
I_O	Output Current	Per Pin(I_{OL}, I_{OH})	±25	mA
T_{ST}	Storage Temperature		−65 to 125	°C
T_{LT}	Lead Temperature	Soldering 10 second	300	°C

OPERATING RANGES

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	Supply Voltage	Commercial	4.75	5.25	V
T_A	Operating Temperature	Commercial	0	70	°C
t_R	Clock Rise Time	See note 3		250	ns
t_F	Clock Fall Time	See note 3		250	ns
t_{RVCC}	V_{CC} Rise Time	See note 3		10	ms

DC ELECTRICAL CHARACTERISTICS
(Over Operating Range Specifications)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{OH}	Output HIGH Voltage	V_{CC}=Min, I_{OH}=−4.0mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC}=Min, I_{OL}=8mA		0.45	V
V_{IH}	Input HIGH Level		2.0	V_{CC}+0.3	V
V_{IL}	Input LOW Level		−0.3	0.8	V
$\mid I_{IL} \mid$	Input Leakage Current	V_{CC}=Max, GND≤V_{IN}≤V_{CC}		10	μA
$\mid I_{OZ} \mid$	Output Leakage Current	I/O=High-Z, GND≤V_O≤V_{CC}		10	μA
I_{SC}	Output Short Circuit Current	V_{CC}=Max, V_O=0.5V(9)	−30	−100	mA
I_{CCSC}	V_{CC} Current, Active, CMOS	V_{IN}=V_{CC} or GND(4)		20	mA
I_{CCAC}	V_{CC} Current, Active, CMOS	V_{IN}=V_{CC} or GND(4) All outputs open(4)		I_{CCSC}+ 0.7mA/MHz	mA
I_{CCST}	V_{CC} Current, Standby, TTL	V_{IN}=V_{IL} or V_{IH}(4)		25	mA
I_{CCAT}	V_{CC} Current, Active, TTL	V_{IN}=V_{IL} or V_{IH}, All outputs open(4)		I_{CCST}+ 0.7mA/MHz	mA

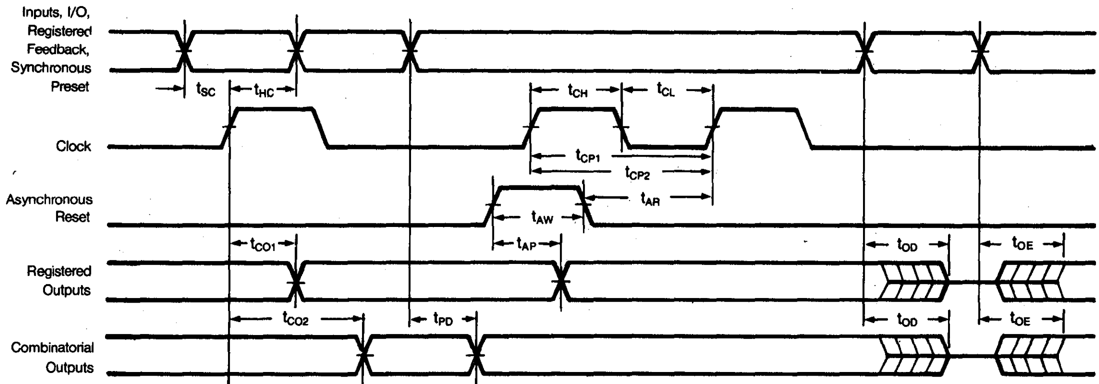
CAPACITANCE(7)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
C_{IN}	Input Capacitance	T_A=25°C, f=1MHz, V_{CC}=5.0V		6	pF
C_{OUT}	Output Capacitance	T_A=25°C, f=1MHz, V_{CC}=5.0V		12	pF

AC ELECTRICAL CHARACTERISTICS(2)
(Over Operating Range)

SYMBOL	PARAMETER	HY18CV8-25		HY18CV8-30		HY18CV8-35		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PD}	Input(5) or feedback to non-registered output		25		30		35	ns
t_{OE}	Input(6) to output enable		25		30		35	ns
t_{OD}	Input(6) to output disable		25		30		35	ns
t_{CO1}	Clock to output		18		20		22	ns
t_{CO2}	Clock to combinatorial output delay via internal registered feedback		35		45		50	ns
t_{SC}	Input(5) or feedback setup to clock	20		25		30		ns
t_{HC}	Input(5) hold after clock	0		0		0		ns
t_{CL}, t_{CH}	Clock width-CLK low time, CLK high time(3)	15		15		15		ns
t_{CP1}	Clock period (register feedback to registered output via internal path)	30		40		45		ns
t_{MAX1}	Maximum clock frequency(1/t_{CP1})		33.3		25		22.2	MHz
t_{CP2}	Clock period(t_{SC}+t_{CO1})	35		45		50		ns
t_{MAX2}	Maximum clock frequency(1/t_{CP2})		28.5		22.2		20	MHz
t_{AW}	Asynchronous clear pulse width	25		30		35		ns
t_{AP}	Input(5) to asynchronous clear		30		35		40	ns
t_{AR}	Asynchronous reset recovery time		20		25		30	ns
t_{RESET}	Power-on reset time for register in clear state.(3)		5		5		5	μs

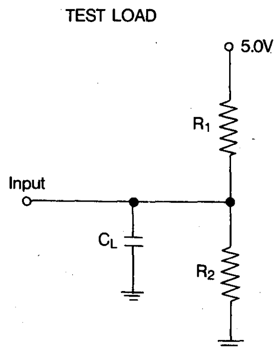
SWITCHING WAVEFORMS



NOTES
1. Minimum DC input is −0.5V, however inputs may undershoot to −2.0V for periods less than 20ns.
2. V_I and V_O are not specified for program/verify operation.
3. Test points for Clock and V_{CC} in t_R, t_F, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
4. I/O pins are open (no load).
5. "Input" refers to input pin signal.
6. t_{OE} is measured from input transition to $V_{REF}\pm 0.1V$, t_{OD} is measured from input transition to V_{OH}-0.1V or V_{OL}+0.1V ; V_{REF}=1.90V for TTL interface for 2.375V for CMOS interface.
7. Capacitances are tested on a sample basis.
8. Test conditions assume : signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
9. Test one output at a time for a duration less than 1 second.
10. Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage.

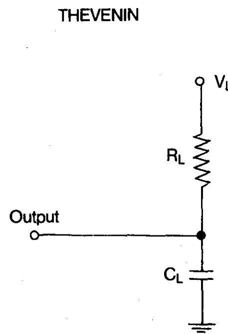
AC EQUIVALENT LOAD CIRCUIT

TEST LOAD



CMOS INTERFACE	TTL INTERFACE
R_1=480KΩ	R_1=464Ω
R_2=480KΩ	R_2=250Ω
C_L=30pF	C_L=30pF

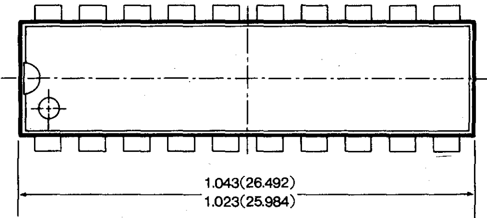
THEVENIN



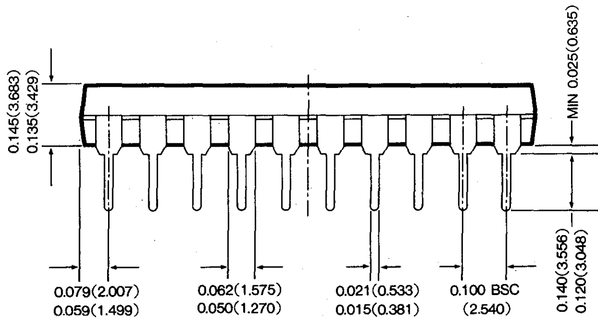
CMOS INTERFACE	TTL INTERFACE
R_L=228KΩ	R_L=163Ω
V_L=2.375V	V_L=1.75V
C_L=30pF	C_L=30pF

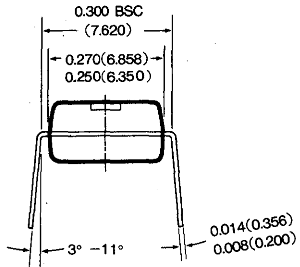
PACKAGE INFORMATION

• **20 PIN PLASTIC DUAL IN LINE PACKAGE−300 MIL**



UNIT : INCH(mm) MAX/MIN





8

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1570 McDaniel Drive — Tel : 215-692-6853
Westchester, PA 19380 — Fax : 215-692-6873

TEXAS

Comptech Sales, Inc.
868 W. Price Road — Tel : 512-542-7474
Brownsville, TX 78520 — Fax : 512-542-8254

Comptech Sales, Inc. (Corporate Office)
2401 Gateway Drive, Ste. 114 — Tel : 214-751-1181
Irving, TX 75063 — Fax : 214-550-8113

Comptech Sales, Inc.
1721 Villa Santos — Tel : 915-590-4590/1
El Paso, TX 79935 — Fax : 915-590-4577

Comptech Sales, Inc.
11130 Jollyville Rd., Ste, 200 — Tel : 512-343-0300
Austin, TX 78759 — Fax : 512-345-2530

Comptech Sales, Inc.
15415 Katy Freeway, Ste. 209 — Tel : 713-492-0005
Houston, TX 77094 — Fax : 713-492-6116

WASHINGTON

Quest Marketing, Inc. (Corporate Office)
15921 N.E. 8th, Ste. 207 — Tel : 206-747-9424
Bellevue, WA 98008 — Fax : 206-643-3488

WISCONSIN

Micro-Tax, Inc.
22660 Broadway, #4A — Tel : 414-542-5352
Waukesha, WI 53186 — Fax : 414-542-7934

DISTRIBUTORS

AUSTRIA

Bacher GmbH
Rotenmuehlgasse 26, A-1120 Tel : 01-813-5646
Wien Fax : 01-83-4276

CANADA

Memory Marketing Co.
1015 Matheson Blvd., Unit 6 Tel : 416-238-0366
Mississauga, Ontario Fax : 416-238-0319
L4W 3A4

DENMARK

Nordisk Elektronik A.S.
Transformervej 17, DK-2730 Tel : 42-84-2000
Herlev Fax : 44-92-1552

PRC Components
Olandsvej 18, 8800 Tel : 86-62-3799
Viborg Fax : 86-62-1295

FINLAND

Oy Fintronic AB
Heikkilantie 2A, 02100 Tel : 0-692-6022
Helsinki Fax : 0-682-1251

FRANCE

Tekelec Airtronic
B.P 2 92315 Serves Tel : 1-46-23-23-32
3edex Fax : 1-45-07-21-91

GERMANY

Rein Elektronik GmbH
Lotscher Weg 66, D-4054 Tel : 2-153-733209
Nettetal 1 Fax : 2-153-733371

Setron Schiffer Elektronik GmbH
Friedrich-Seele Str. 3A Tel : 531-80-980
3300 Braunschweig Fax : 531-80-987

HOLLANDS

Marcotec B.V.
57 Innsbruckweg 3047 AG Tel : 10-462-5060
Rotterdam Fax : 10-462-7076

HONG KONG

Components Agent Ltd.
36F Metroplaza, Tower 1 Tel : 852-487-8826
Hing Fong Road, Kwai Fax : 852-487-1268
Chung, HK

Dodwell Engineering
7F Cavendish Centre Tel : 852-555-4633
23 Yip Hing Street Fax : 852-873-0625
Wong Chuk Hang, HK

ITALY

Comprel S.P.A
Viale Fulvio Testi, 115 Tel : 2-612-0641
20092 Cinisello, Balsamo, Milan Fax : 2-612-8158

Fanton Components
Via 0 Simon15 Anzola Tel : 51-73-5015
Dell Emilia 1-40011 Fax : 51-73-5013
Bologna

JAPAN

Hakuto Co., Ltd.
2-29, Toranomon 1-Chome, Tel : 03-3225-8910
Minato-Ku, Tokyo 105 Fax : 03-3597-8975

Tachibana Tectron Co., Ltd.
2-2-5 Higashiyma Meguro-Ku Tel : 03-3719-2261
Tokyo 153 Fax : 03-3793-1329

KOREA

Bethel Electronics Intl., Inc(Corporate Office)
16-9 Hangangro 3-Ga — Tel : 02-704-5670, 02-716-5575
Yongsan-Ku, Seoul — Fax : 02-704-1839, 02-716-5576

Chongro Office — Tel : 02-273-2251/2
Yongsan Office — Tel : 02-702-3236, Fax : 02-702-3237

Jeil Nanotec Co.(Corporate Office)
3F Mansung Bldg. — Tel : 02-323-4291/6
460-25, Seokyo-Dong, — Fax : 02-323-4297
Mapo-Ku, Seoul
Sunin Office — Tel : 02-703-1378/9, Fax : 02-716-5930
Yongsan Office — Tel : 02-712-4700/1, Fax : 02-716-3605

Phalchun Co., Ltd.(Corporate Office)
16-9 Hangangro 3-Ga, — Tel : 02-702-1543/4
Yongsan-Ku, Seoul — Fax : 02-702-1545

Sales Shop — Tel : 02-702-3755/6

Seungjun Sangsa Ltd.
203-1 Jangsa-Dong, — Tel : 02-274-6800
Chongro-Ku, Seoul — Fax : 02-274-5929

Yongsan Office — Tel : 02-701-6800

NORWAY

Nordisk Elektronik A.S.
P.O Box 123, 1364 Hvalstad — Tel : 02-84-6210, Fax : 02-84-6545

SINGAPORE

Brilliant Electronics Pte, Ltd.
12A-14A Lorong 13, Geylang — Tel : 741-3455
Road. — Fax : 741-3016/7

Components Assembly & Sales Pte, Ltd.
112 Lavender Street, #04-02 — Tel : 293-0811
Chuan Building, Singapore 1233 — Fax : 293-3006

Eltee Electronics Pte, Ltd.
17 Harvey Road #03-01 — Tel : 285-0633
Singapore 1336 — Fax : 289-5327

Intraco Resources Trading Pte, Ltd.
78 Shenton Way, #04-01 — Tel : 220-6133
Singapore 0207 — Fax : 222-1123

SPAIN

Lober S.A
Monte Esquinza 28. — Tel : 1-410-6821
28010 Madrid — Fax : 1-410-6868

SWEDEN

Nortec Electronics AB
Box 1830 — Tel : 8-705-1800
S-171, 27 Solna — Fax : 8-83-6918

Titan Electronics
Box 7086 — Tel : 87-54-98-80
S-191, 07 Sollentuna — Fax : 87-54-89-15

SWITZERLAND

Ascom Primotec AG
Taefern Str. 37. CH 5405 — Tel : 56-84-0171
Baden-Daetwill — Fax : 56-83-3454

TAIWAN R.O.C.

Chung Teh Co., Ltd.
350, Min Sheng East Road, — Tel : 02-501-8181
P.O. Box : 27-088 — Fax : 02-501-5836
Taipei

Lebro Industrial Co., Ltd.
Rm 1102, No. 185, Sung Chiang — Tel : 02-503-6357
Road. Taipei — Fax : 02-501-7809

Unigate Corporation
5F 554 Lin Shen N. Road, — Tel : 02-597-3686
Taipei — Fax : 02-597-3684

UNITED KINGDOM

Mogul Electronics
Unit 11, Vestry Estate — Tel : 732-74-1841
Sevenoaks, Kent TN14 5EU — Fax : 732-74-2210

ESD Distribution Ltd.
Edinborough Way, Harlow — Tel : 279-62-6777
Essex CM10 2DF — Fax : 279-44-1687

UNITED STATES OF AMERICA

ARIZONA

Aved Electronics
7741 East Gray Rd., Ste. 9 Tel : 602-951-9788
Scottsdale, AZ 85260 Fax : 602-951-4182

CALIFORNIA

Aegis Electronics Group.
1015 Chestnut Ave., Ste. G2 Tel : 619-729-2026
Carlsbad, CA92008 Fax : 619-729-9295

All American Semiconductor
369 Van Ness Way, Ste. 701 Tel : 213-320-0240
Torrance, CA 90501 Fax : 213-320-7207

All American Semiconductor
5060 Shore Ham Plaza, Ste. 200 Tel : 619-458-5850
San Diego, CA 92122 Fax : 619-458-5866

All American Semiconductor
17220 New Hope Street, Ste. 211 Tel : 714-435-0115
Fountain Valley, CA 92708 Fax : 213-320-7207

All American Semiconductor
2360 Qume Drive, Ste. C Tel : 408-943-1200
San Jose, CA 95131 Fax : 408-943-1393

Aved(Corporate Office)
1582 Parkway Loop, Unit G Tel : 714-259-8258
Tustin, CA 92680 Fax : 714-259-0828

IEC
6-B Autry Street Tel : 714-837-9960
Irvine, CA 92718 Fax : 714-837-8308

IEC
9940 Business Park Dr., #145 Tel : 916-363-6030
Sacramento, CA 95827 Fax : 916-362-6926

ITT Multicomponents
1580 Oakland Rd., Ste. C-102 Tel : 408-453-1404
San Jose, CA 95131 Fax : 408-453-1407

ITT Multicomponents
5 Jenner Street Tel : 714-727-4001
Irvine, CA 92718 Fax : 714-727-2109

Jaco Electronics
2282 Townsgate Road, Ste. 100 Tel : 805-495-9998
Westlake Village, CA 91361 Fax : 805-494-3684

Jaco Electronics
2880 Zanker Road, Ste. 202 Tel : 408-432-9290
San Jose, Ca 93134 Fax : 408-432-9298

COLORADO

All American Semiconductor
25676 S. Norman Court Tel : 303-756-0817
Denver, CO 80224 Fax : 213-320-7207

Aved Electronics
4090 Youngsfield Tel : 303-422-1701
Wheat Ridge, CO 80033 Fax : 303-422-2529

IEC(Corporate Office)
420 E. 58th Avenue Tel : 303-292-6121
Denver, CO 80216 Fax : 303-297-2053

IEC
5750 N. Logan St. Tel : 303-292-6121
Denver, CO 80216 Fax : 303-292-0114

CONNECTICUT

GRS Electronics, Inc.
296 North Piains Highway Tel : 203-265-2078
Wallingford, CT 06492 Fax : 203-265-4274

Millenium Electronics
3872 Main Street Tel : 203-372-2037
Bridgeport, CT 06606 Fax : 203-374-3201

FLORIDA

All American Semiconductor(Corporate Office)
16251 NW 54th Avenue Tel : 305-621-8282
Miami, FL 33014 Fax : 305-620-7831

All American Semiconductor
5009 Hiatus Road Tel : 305-572-7999
Sunrise, FL 33351 Fax : 305-749-9229

GRS Electronics, Inc
296 North Wickem Road, Tel : 407-242-8157
Melbourne, FL 32935 Fax : 407-242-2372

ILLINOIS

Components. Inc.
1989J University Lane Tel : 708-852-7707
Lisle, IL 60532 Fax : 708-852-0263

IEC
2200 N. Stonington Ave., Ste. 210 Tel : 708-843-2040
Hoffman Estates, IL 60195 Fax : 708-843-2320

NEP Electronics
805 Mittle Drive Tel : 708-595-8500
Wooddale, IL 60191 Fax : 708-595-8706

QPS Electronics, Inc.
101 Commerce Drive — Tel : 708-884-6620
Schaumburg, IL 60173 — Fax : 708-884-7573

Voyager Electronics
804 Thorndale Avenue — Tel : 708-860-1300
Bensenville, IL 60106 — Fax : 708-860-1573

INDIANA

Altex Electronics
12774 Old Meridian St. — Tel : 800-783-2589
Carmel, IN 46032 — Fax : 317-844-6593

CAM RPC
1329 W. 96th St. Ste. 10 — Tel : 317-580-9999
Indianapolis, IN 46260 — Fax : 317-580-9615

RM Electronics
1329 W. 96th St., Ste. 10 — Tel : 317-843-9403
Indianapolis, IN 46260 — Fax : 317-580-9615

MARYLAND

GRS Electronics
6925 East Oakland Mills Rd. — Tel : 609-964-8560
Columbia, MD 21045 — Fax : 609-964-0423

All American Transistor
14636 Ruthgeb Drive — Tel : 301-251-1205
Rockville, MD 20850 — Fax : 301-251-8574

Jaco Electronics
Rivers Center
10270 Old Columbia Road — Tel : 301-995-6620
Columbia, MD 21046 — Fax : 301-995-6032

MASSACHUSETTS

All American Semiconductor
107 Audubon, Ste. 104, Bldg. 2 — Tel : 617-256-2300
Wakefield, MA 01880 — Fax : 617-246-2305

Jaco Electronics
1053 East Street — Tel : 508-640-0010
Tewksbury, MA 01876 — Fax : 508-640-0755

Now Electronics
28 Lord Road — Tel : 508-460-0187
Marlborough, MA 01752 — Fax : 508-460-0467

Worldtronics Corp. Inc.
68 Adler Road — Tel : 617-769-2344
Westwood, MA 02090 — Fax : 617-769-4588

MICHIGAN

Advent Electronics, Inc.
24713 Crestview Court — Tel : 313-477-1650
Farmington Hills, MI 48335 — Fax : 313-477-2630

CAM RPC
32468 Schoolcraft Rd. — Tel : 313-427-4800
Livonia, MI 48150 — Fax : 313-427-4820

RM Electronics(Corporate Office)
4310 Roger B Chaffee — Tel : 616-531-9300
Memorial Drive, SE — Fax : 616-531-2990
Grand Rapids, MI 49548

MINNESOTA

All American Semiconductor
11407 Valley View Road — Tel : 612-944-2151
Eden Prairie, MN 55344 — Fax : 612-944-9803

NEW JERSEY

Marlac Electronics
311 New Albany Road — Tel : 609-234-4200
Moorestown, NJ 08057 — Fax : 609-234-0672

GRS Electronics, Inc.(Corporate Office)
600 Penn Street — Tel : 609-964-8560
Camden, ,New Jersey 08102 — Fax : 609-964-0423
609-964-2585

NEW YORK

All American Semiconductor
711-2 Koehler Avenue — Tel : 516-981-3935
Ronkonkoma, NY 11779 — Fax : 516-981-3947

CAM RPC
2975 Brighton Henrietta — Tel : 716-427-9999
Town Line Road — Fax : 716-427-7559
Rochester, NY 14623

Jaco Electronics(Corporate Office)
145 Oser Avenue — Tel 1 : 800-645-5112
Hauppauge, NY 11788 — Tel 2 : 516-273-5500
Fax : 516-273-5528

Janesway Electronics(Corporate Office)
404 N. Terrace Avenue — Tel : 914-699-6710
Mt. Vernon, NY 10552 — Fax : 914-699-6969

Rome Electronics
216 Erie Blvd. East — Tel : 315-337-5400
Rome, NY 13440 — Fax : 315-337-2388

Rome Electronics
340 Harris Hill Road, — Tel : 716-626-1602
Williamsville. NY 14221 — Fax : 716-626-1609

NORTH CAROLINA

Jaco Electronics
3029-107 Stonybrook Drive — Tel : 919-876-7767
Raleigh, NC 27604 — Fax : 919-876-6964

OHIO

CAM RPC
733H Lakeview Plaza Rd. — Tel : 614-888-7777
Worthington, OH 43085 — Fax : 614-895-1550

CAM RPC(Corporate Office)
749 Miner Road — Tel : 216-461-4700
Cleveland, OH 44143 — Fax : 216-461-4329

Schuster Electronics
11320 Grooms Road — Tel : 513-489-1400
Cincinnati, OH 45242 — Fax : 513-489-8686

OREGON

IEC
6850 S.W. 105th Ave., Ste. B — Tel : 503-641-1690
Beaverton, OR 97005 — Fax : 503-646-3737

PENNSYLVANIA

CAM RPC
620 Alpha Drive — Tel : 412-963-6202
Pittsburgh, PA 15238 — Fax : 412-963-6210

GRS Electronics, Inc.
Route 183 & MacArthur Boulevard
Airport Industries, Bldg. No. 2 — Tel : 800-255-5756
Reading PA 19605 — Fax : 215-375-4513

TEXAS

All American Semiconductor
1819 Firman Dr., Ste. 127 — Tel : 214-231-5300
Richardson, TX 75081 — Fax : 214-437-0353

Jaco Electronics
1005 Industrial Blvd. — Tel : 713-240-2255
Sugarland, TX 77478 — Fax : 713-240-6988

Jaco Electronics
2120 A West Braker — Tel : 512-835-0220
Austin, TX 78758 — Fax : 512-339-9252

Jaco Electronics
4251 Kellway Circle — Tel : 214-733-4300
Addison, TX 75244 — Fax : 214-250-0216

Janesway Electronics
1701 N. Greenville Ave., Ste. 906
Richardson, TX 75081 — Tel : 214-437-5125
Fax : 214-699-3671

Omni Pro Electronics(Corporate Office)
4141 Billy Mitchell — Tel : 214-233-0500, 800-926-8926
Dallas, TX 75244 — Fax : 214-385-7508

Omni Pro Electronics
1014 Castile Road — Tel : 512-794-9200
Austin, TX 78733 — Fax : 512-338-9576

Omni Pro Electronics
10101 Southwest Freeway, — Tel : 713-270-1700
Suite 400 — Fax : 713-270-8020
Houston, TX 77074

UTAH

Aved Electronics
1836 Parkway Blvd. — Tel : 801-975-9500
Salt Lake City, UT 84119 — Fax : 801-977-0245

IEC
2117 South 3600 West — Tel : 801-977-9750
Salt Lake City, UT 84119 — Fax : 801-975-1207

WASHINGTON

IEC
1750 124th Ave., N.E. — Tel : 206-455-2727
Bellevue, WA 98005 — Fax : 206-453-2963

Jaco Electronics
14400 Bell-Red Road, Ste. 110 — Tel : 206-649-9867
Bellevue, WA 98007 — Fax : 206-649-8691

WISCONSIN

NEP Electronics
2604-06 S. 162 Street — Tel : 414-785-9100
New Berlin, WI 53151 — Fax : 414-785-9131

Progressive Image
10617 W. Oklahoma Avenue — Tel : 414-321-4722
Milwaukee, WI 53227 — Fax : 414-321-4665