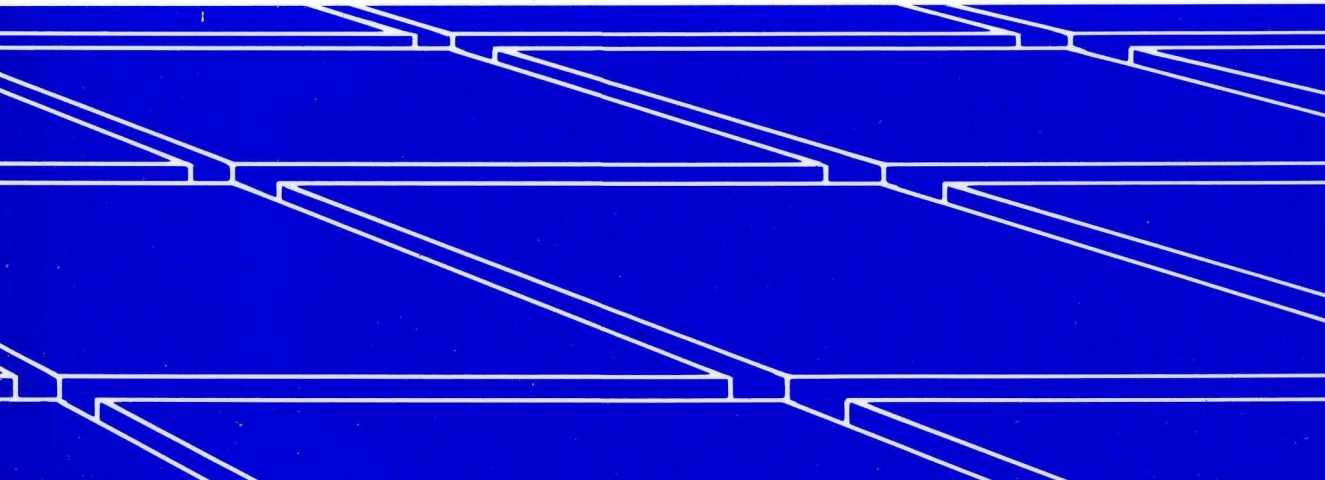
INC.



# PLACE™ Software and Applications Handbook



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Second Edition

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# Introduction to PLACE

# 1.0 Introduction to PLACE™



## 1.1 The PLACE Advanced Development Software

Welcome to the PLACE Advanced Development Software from ICT, Inc. PLACE (PEEL Logic Architectural Compiler and Editor) is an enhanced development package that offers complete support for ICT's family of PEEL (Programmable Electrically Erasable Logic) Arrays and Devices.

Below are the two main versions of the PLACE software.

### PLACE "Standard Version"

This version of the PLACE software (if the word "Evaluation" is not specified, the Standard Version is automatically assumed) provides everything needed to implement complete designs from architectural entry to the creation of a compiled and simulated JEDEC file for programming. Note that the PLACE Compiler (PLCOM.EXE) is copy-protected and has a limit of three hard disk installations. The PLACE original disk #1 has an additional copy-protect key which cannot be installed to the hard disk. This additional key serves as a back-up.

### PLACE "Evaluation Version"

The "Evaluation" version provides all features of the standard version with the exception of the logic compiler for creating JEDEC programming files. Complete designs can be entered and saved allowing you to start designs immediately and see how the PEEL Array architectures and PLACE software will suit your logic design needs. Designs created can later be compiled and simulated on the standard version.

### PLACE features

#### Architectural Editor

PLACE incorporates an innovative architectural editor which graphically illustrates and controls the architectures, logic equations, state-diagram and truth-table entries, hence making

making the overall design easy to understand while allowing for optimum utilization.

#### Logic Compiler (Standard version only)

The PLACE compiler performs logic transformation allowing equations to be specified in most any fashion. The compiler also features five levels of user-selectable logic reduction (including "auto-demorganization") making it possible to get more logic into every design.

#### Logic Simulator

PLACE provides a multi-level logic simulator that lets the external and internal signals be fully simulated, analyzed and edited via a graphically illustrated waveform display.

#### Documentation

PLACE designs can be documented through batch printing of the logic design description, architecture and waveform displays.

#### Programmer Interface

Programming is supported by a direct interface to the ICT PEEL Development System programmer, and by other popular programmers via the serial communication port or by automatically executing the third-party programming software from within PLACE.

## 1.2 About This Manual

The PLACE Software manual is organized in seven sections. Before trying to design with the PLACE software, make sure you read through the first three sections: "Introduction", "Installation" and "Getting Started". By doing so you will save yourself time.

After you have completed installing the PLACE software and have become familiar with the basic operations, chapters 4 and 5 "Operation Reference Guide" and "PLACE Design Language Reference Guide" can be referred to as you implement your first designs. Documentation describing several application examples are provided in chapter 6. These examples are also

included on diskette and will automatically be loaded during installation.

While using this manual and the software you may need to reference the PEEL Array product specifications. Please make sure you have a copy of the ICT Data Book.

☞ The software operations and features described in this manual are referenced to PLACE Version 2.10. For additional information on new features and manual corrections, please refer to the README.DOC file on PLACE disk #1.

## 1.3 PEEL Device and PEEL Array support

The devices supported in the PLACE software include:

**PEEL Arrays**

| | | |
|---|---|---|
| PA7024 | PA7140 | PA7128 |

**PEEL Devices**

| | | |
|---|---|---|
| PEEL18CV8 | PEEL173 | PEEL273 |
| PEEL22CV10 | PEEL22CV10A | PEEL22CV10A+ |
| PEEL20CG10 | PEEL22CV10Z | |

Additional devices will be supported in future software versions.

## 1.4 Converting APEEL File ".APL" to PLACE File ".PSF"

If you are a current user of the PEEL Device Development Software (PDS), then your designs done in the APEEL language can be converted to the PLACE design language format by using the APL2PSF (APL2PSF.EXE) utility. This allows the PLACE enhanced features available for the PEEL Arrays to be used to implement designs for the lower density PEEL devices.

The format for the APL2PSF utiltiy is:

APL2PSF *filename*

The extension of the *filename* defaults to ".APL" if not specified.

# PLACE Installation

2

# 2.0 PLACE Installation

## 2.1 System Requirements

- ❑ IBM PC, XT, AT or compatible
- ❑ 512K RAM memory for most designs, 540K for very large designs
- ❑ Hercules, EGA or VGA
- ❑ A hard disk with 2.6 M-bytes of free disk space (1.6 M-bytes for program storage and 1M-bytes for operational file storage)
- ❑ Microsoft mouse or compatible with driver
- ❑ DOS version 3.0 or greater
- ❑ (Optional) Expanded Memory Systems with drivers conforming to the LIM EMS specification version 3.2 or greater



## 2.2 "Evaluation Version" Hard Disk Installation Procedure

- ➤ Turn the computer on
- ➤ Boot-up DOS 3.0 or greater
- ➤ Install your mouse driver, otherwise PLACE will not boot-up
- ➤ Insert the PLACE Evaluation Software Disk into drive A
- ➤ Select drive A and type "INSTALL" followed by the [ENTER] key. The install program will guide you to copy all files to a selected directory on your hard disk. The default drive and directory is C:\ ICTPLACE. You can enter an alternate drive and directory by using the [Backspace] or cursor keys
- ➤ Once completed, the program will return to the DOS prompt. Type "INIT " followed by [ENTER] to initialize the software. For subsequent use, type "PLACE" followed by [ENTER]

- ❑ (Optional) If you wish to enter PLACE from any directory you can do this by adding the following to your AUTOEXEC.BAT file. Assuming "ICTPLACE is the directory name and it is in drive C:, you would add "C:\ICTPLACE" to the your DOS path and insert "SET ICTPLACE=C:\ICTPLACE"
  Ex:Path c:\;c:\DOS;c:\batch;C:\ICTPLACE
  Set ICTPLACE=C:\ICTPLACE

## 2.3 "Standard Version" Hard Disk Installation Procedure

The standard PLACE software is provided on multiple diskettes identified by the disk number. To properly operate the software, all files from the diskettes must be loaded on to the hard disk via the following installation procedure.

Please note that disk #1 of the original PLACE software diskette incorporates copy protection. **This copy protection allows up to three hard disk installations** (note that an additional un-installable copy-protection key (key disk) will serve as a back-up). To move the software to a different computer, the un-install procedure must be executed to reinstate the available number of installations onto the original disk #1. Please remember if you intend to re-format your hard disk make sure to un-install PLACE first. If this is not done the copy protection installation will be lost.

☞ The PLACE copy-protect key is made up of two files, "EV21.SYS" and "EV22.SYS". These hidden system files which reside in the root directory of the installed drive **must not be (manually) deleted** because other application programs may be utilizing the same copy-protection scheme. The un-install procedure (section 2.5) should be used to remove the copy-protect key from the installed drive.

### Types of Installation

The PLACE "Standard" Version hard disk installation software provides several options for installing the copy protection key. Note that each option specified below will copy all the files from the original PLACE diskettes to the hard disk (the only difference is the type of installation for the copy-protection key). **If you are a first-time PLACE user, we recommend option #4 because it allows PLACE to be run in the most efficient manner.** If you run into a problem with the copy-protection key, then you may want to try the other options.

- **Option 1: Evaluation Version**
  - Installs the PLACE Software (Evaluation Version), i.e. the PLACE Compile operation is disabled.
  - No PLACE copy-protect key installation.

- The PLACE Install-count will not be decremented, thus allowing unlimited installations.

- **Option 2: Original Floppy Disk #1 as (Copy-Protected) Key Disk**
  - Installs the PLACE Software (Standard Version). Compile operation is enabled.
  - No PLACE copy-protect key installation. Uses the copy-protect key from original disk #1.
  - The PLACE Install-count will not be decremented.
  - The major disadvantage with this option is the requirement of the original disk #1 to be in the floppy drive during the PLACE operation changes (i.e. any time the Compile operation is selected). The frequent access of the floppy drive slows down the PLACE software. However, unlimited installations can be implemented with this option.

- **Option 3: New Floppy Disk as Key Disk**
  - Installs the PLACE Software (Standard Version). Compile operation is enabled.
  - Installs the PLACE copy-protect key to a blank formatted floppy diskette (3.5/5.25" High or Double-Sided Densities).
  - The PLACE Install-count will be decremented by one.
  - Like Option 2, the installed work disk must always be in the floppy drive during the PLACE operation switching processes.
  - For advantages and disadvantages, refer to the descriptions in Option 2.
  - If possible, use option 3 instead of option 2 because option 2 is designed for use as a backup.

- **Option 4: Install Key to Hard Disk**
  - Installs the PLACE Software (Standard Version). Compile operation is enabled.
  - Installs the PLACE copy-protect key to the hard disk. The hidden system files "EV21.SYS" and "EV22.SYS"

which make up the copy-protect key will reside in the root directory of the installed drive.

- The PLACE Install-count will be decremented by one.

## Installation Procedure

- Turn the computer on.
- Boot-up DOS 3.0 or greater.
- Install your mouse driver, otherwise PLACE will not boot-up.
- (Optional) - **Upgrade for existing PLACE users only:** Un-install your current version of PLACE back to the original disk. Insert original disk #1 into floppy drive A and type "UNINSTAL" in the PLACE directory on the hard disk. The un-install procedure removes the existing copy-protect key "EV21.SYS" and "EV22.SYS" from the hard drive. **It should be noted that the PLACE installation procedure will not be hindered if the key is not removed first. The un-install process is used merely to recover the installation-count.**

☞ Reminder: Note that the copy-protect key files "EV21.SYS" and "EV22.SYS" should not be manually deleted because you may be using some other application programs that utilize the same copy protection scheme.

- Insert the PLACE original disk #1 into drive A. Do not write-protect this disk.
- At the A> prompt, type "INSTALL" followed by the [ENTER] key. Note that you can abort the installation any time by pressing Ctrl-Break. If you abort the installation procedure after the copy-protection key has been installed to the hard disk, please make sure to "UNINSTAL" it back to the PLACE original disk #1.
- Type in your company name and address, installation date, and your name.
- Select your options. Enter the directory you want PLACE to be installed to. Default drive and directory is C:\ICTPLACE.

- (Optional) - **For existing PLACE users only:** If the PLACE installation program senses that the copy-protect key has already been installed on the target hard drive, then a prompt will appear asking you whether you want to use the existing key. If you answered Yes, then the installation will proceed and the install-count of the PLACE 2.0 will not be decremented. If the answer is No, the installation procedure is aborted.
- Once installation is completed, type "INIT" to initialize the PLACE software. For subsequent use of the PLACE software, type "PLACE" followed by the [ENTER] key.

❑ (Optional) If you wish to run PLACE from any directory, you can do this by adding the following to your AUTOEXEC.BAT file. Assumming "C:\ICTPLACE" is the installed directory, you would add "C:\ICTPLACE" to your DOS path and insert "SET ICTPLACE=C:\ICTPLACE".



## 2.4 Initializing the PLACE Software using "INIT"

After each PLACE installation, it is recommended to initialize the PLACE software by typing "INIT" followed by the [ENTER] key in the PLACE directory. The initialization procedure erases the "PLACE.SAV" file which stores the set-up configurations of the PLACE software. Once this file is erased, the PLACE software during boot-up (i.e., by typing "PLACE" followed by the [ENTER] key) sets all of the configuration variables except for the color, graphic adapter (VGA only) and mouse type variables to the default conditions.

☞ You can re-initialize PLACE any time you run into problems with the software, or if you want to change the set-up configuration variables.

### VGA Graphic Adapter Option

If a VGA monitor is being used, the PLACE software can be set to operate using the 640X350 (EGA) or 640X480 (VGA) resolution. In most cases, the VGA resolution is preferred because the graphics are much cleaner and distinct. The EGA resolution option is provided in case a problem is encountered using the VGA resolution. If you are running PLACE for the first time, you

may want to experiment with both options before starting your designs.

### Color Type Option

This option allows the PLACE software to be displayed in 2 (monochrome) or 16-color mode. For Hercules monitors, always select the 2-color mode, i.e. answer "N" for No when prompted for the color option.

### Mouse Type Option

The PLACE software allows multiple mouse cursor types to be displayed depending on the mode selected (e.g. Edit Eqn, Edit Arch, Label, and etc.) in the Design operation. For instance, a left-pointing arrow ("<-") mouse cursor indicates the current mode is the "Edit Eqn" mode. Figure 2-1 illustrates the different mouse cursor types found in the Design operation. In addition, each of the PLACE operations has its own unique mouse cursor.

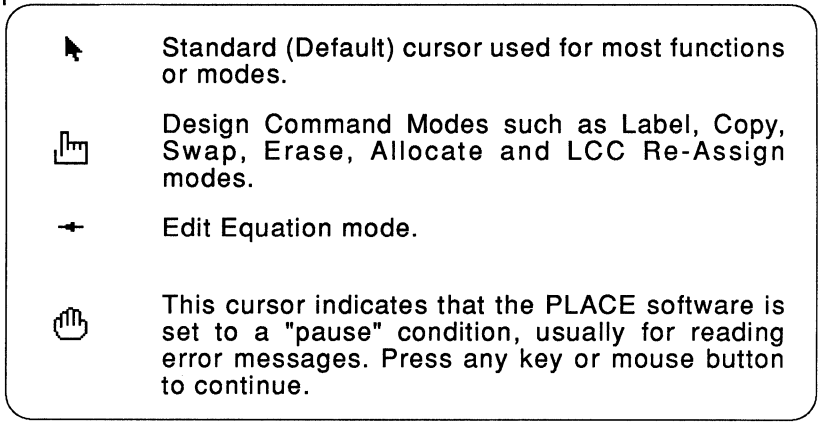


Figure 2-1, Multiple Mouse Cursor Types

If you are experiencing mouse problems with the multiple cursor mode, it is recommended to select the single cursor type in the initialization procedure.

## 2.5 Un-installing the PLACE software

The un-install procedure allows the PLACE copy-protect key to be removed from the installed (hard or floppy) drive. **Note that the copy-protect key need not be un-installed when installing an upgrade version with the same PLACE serial number to the same hard drive.** In this case, the same copy-protection key will be used by the upgrade software. If the serial number is different, then a new key will be installed. In the latter case, both the installed and upgrade versions will be functional, i.e. they both can be un-installed later.



### Un-Install Procedure

- Change to the PLACE directory on the installed hard disk. Example: C>CD\ICTPLACE
- Insert the PLACE original disk #1 of the installed version into drive A. Do not write-protect this diskette.
- Type "UNINSTAL" followed by the ENTER key at the PLACE directory prompt on the hard disk.
  Example: C:\ICTPLACE>UNINSTAL.
- Enter "A" when prompted for the target drive letter.
- If there are no error messages, then the PLACE copy-protect key has been un-installed successfully back to the original diskette. The resulting PLACE software on the hard disk is automatically converted to the Evaluation Version, i.e. all PLACE operations are functional with the exception of the Compile operation.

### Un-Install Errors

If an error occurred in the un-install procedure, please note down the first four digits of the 12-digit error code. Below is an example of an un-install error.

Security Error 7030-0000-0000

The following table lists the error codes for the un-install procedure.

| Error No. | Description |
|---|---|
| 7024 | Authorization code found, but not for the PLACE program. |
| 7032 | Un-install aborted - PLACE copy-protect key has not been installed on the target diskette. Please make sure the target diskette is the PLACE disk #1. |
| 7043 | The source disk does not have the copy-protect key for the current version of the PLACE software. |
| 7061 | RESET is not allowed to be run from any disk other than the PLACE disk #1. |
| 7072 | RESET has been run unsuccessful for 10 times. It can no longer be used on the PLACE disk #1. |
| Other Errors | Call ICT Technical Support or Software Department (408) 434-0678. |

# Getting Started with PLACE

3

# 3.0 Getting Started with PLACE

## 3.1 Entering the PLACE software

Once PLACE is properly installed (i.e. PLACE was initialized by using "INIT"), it can be entered by typing "PLACE" while in the ICTPLACE directory. Pressing the ENTER key twice after typing "PLACE" will bypass the boot-up messages. If you wish to enter PLACE from any directory, see section 2.2 or 2.3 on "Hard Disk Installation Procedure". Before using the PLACE software, please read through the following sections on "Using the Mouse" and "Getting HELP".

## 3.2 Using the Mouse

The PLACE software and manual will commonly refer to several mouse actions using the nomenclatures specified in Table 3-1.

| Term | Mouse Action |
|---|---|
| Click | press/release the left button of mouse. |
| Click-R | press/release the right button of mouse. |
| Click-LH | press/hold the left button of the mouse while moving the mouse. |
| Click-RH | press/hold the right button of the mouse while moving the mouse. |
| Click-MH | press/hold the middle button of the mouse while moving the mouse (3-button mouse only). |

Table 3-1, Nomenclatures for PLACE mouse actions

Note that the default mouse cursor is a North-West pointing Arrow. However, several cursor types (Figure 2-1) may appear depending on whether option #1 of the mouse cursor types was selected during the PLACE initialization procedure (section 2.4), or on the type of mode or function that was selected in the PLACE software.

### "Click" - press/release left button

"Click" is used in all operations and modes to make a selection. A selection can be made by moving the mouse cursor to the desired item, and press/release the left button of the mouse. In many cases this selected item will be highlighted. Items that can be selected include pop-down and pop-up menu windows, architectural elements in the design operation such as Logic Control Cells (LCC), I/O Cells (IOC), Input Cells (INC), Global Cells (GBC), test vector waveforms (Simulate operation) and etc.

### "Click-R" press/release right button

"Click-R" in most cases is used to exit, complete or return from the current function being performed. **In the Design operation, Click-R is also used to toggle back and forth from the default "Edit Architecture" mode to the "Edit Equation" mode.**

### "Click-LH" or press/hold the left button while moving the mouse

Click-LH is used in both the Design and Simulate operations. In the Design operation, it is used to scroll from one LCC/IOC to another in the LCC/IOC screen. In the Simulate operation, it is used for panning in the waveform screen as well as block selection for the copy, move, and delete functions in the "Edit" mode.

### "Click-RH" and "Click-MH" or press/hold the left and right button respectively while moving the mouse

For 3-button mouse systems, click-MH (click-RH for 2-button mouse) is used to display the menu options in the PLACE text editor utilized in the Design or Program operation. While holding the middle mouse button down (right button for 2-button mouse), move the mouse cursor and click at the menu option. Once the option is selected, the middle button can be released.

### Mouse support in the PLACE Text Editor

Mouse is supported in the PLACE Text Editors which are used within the Design, Compile and Program operations. To initiate the mouse support, press the middle button (3-button mouse)

or right button (2 button mouse) of the mouse but don't release the button. Move the mouse cursor to the top of the screen to select the functions. Table 3-2 lists the mouse actions in the text editor.

| Mouse Action | Function |
|---|---|
| Click within the text area | Move the text cursor to the mouse cursor |
| Click at the top border area | Scroll 6 lines up |
| Click at the bottom border area | Scroll 6 lines down |
| Click at the first line of the text | Scroll 1 line up |
| Click at the last line of the text | Scroll 1 line down |
| Click-R (right button) | Exit editor (3-button)<br>Access mouse menu (2-button) |
| Click-M (middle button) | Access mouse menu (3-button mouse only) |

Table 3-2, PLACE Text Editor Mouse Actions

### Re-initializing the mouse in PLACE

In the event a mouse problem is encountered, press the [ESC] key as many times as needed to exit the current mode or function to return to the main screen of the operation (Design, Compile, Simulate, Document and Program). Then, press the [Alt]-M keys (simultaneously press the [Alternate] and character "M" keys) to re-initialize the mouse.

## 3.3 Getting HELP

The PLACE software incorporates an on-line HELP feature which provides information and procedures for most PLACE functions and modes. To get HELP information, just point the mouse to the menu function or mode and simultaneously press the [F1] key . Besides this on-line command HELP, a general HELP menu is provided in the Utilities pop-down menu.

## 3.4 A Guided Tour through the PLACE software

To quicken the learning process, this section discusses some basic procedures commonly used in the PLACE software. The device used in this guided tour is the PA7024. So, some of the terms used in this section may only be applicable to the PA7024 device (or the PEEL Array family of devices). For instance, terms such as LCC (Logic Control Cell) and GBC (Global Cell) pertain only to devices in the PEEL Array family.

If you are a first-time PLACE user, it is recommended that you run the PLACE software while reading this section. By actually performing the instructions (specified in *italics*), you will be able to get a more complete understanding of the features, modes or functions found in the PLACE software.

There are five main operations that can be performed with PLACE; Design, Compile, Simulate, Document and Program. When first entering PLACE, it will default to the Design Operation in the edit architecture mode ("Edit Arch"). The display will show the PA7024 PEEL Array pin block diagram (Figure 3-1).

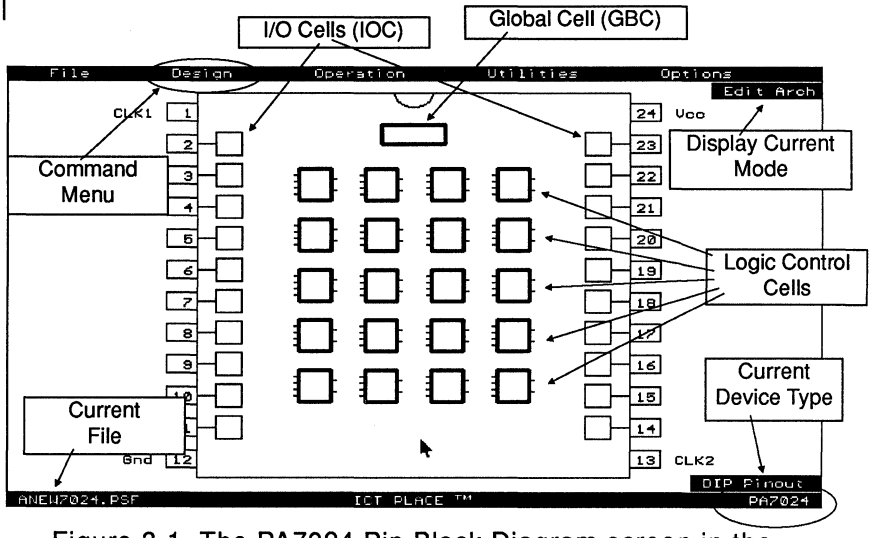


Figure 3-1, The PA7024 Pin Block Diagram screen in the Design Operation

☞ Note that PLACE automatically loads the ANEW template file upon initial boot-up. In Figure 3-1, the PLACE software has loaded the ANEW file (ANEW7024.PSF) for the PA7024 device. There is an ANEW template file for each device supported by the PLACE software. For instance, the ANEW7140.PSF file is the template file for the PA7140 device. Each ANEW file contains the device's default cell configurations.

At the top of the screen, there are five pop-down menu options: File, Design, Operations, Utilities and Options (available only in the Design operation). *Move the mouse cursor to the "Operation" menu.* A pop down window will appear showing the five main operations (Figure 3-2). Note the menu option titled "Design" to the left of the operation menu. This menu is called the "command" menu. Each time a new operation is selected, this command menu will change to allow the selection of commands specific for that operation. The command menu is also used as an indicator for the current operation.

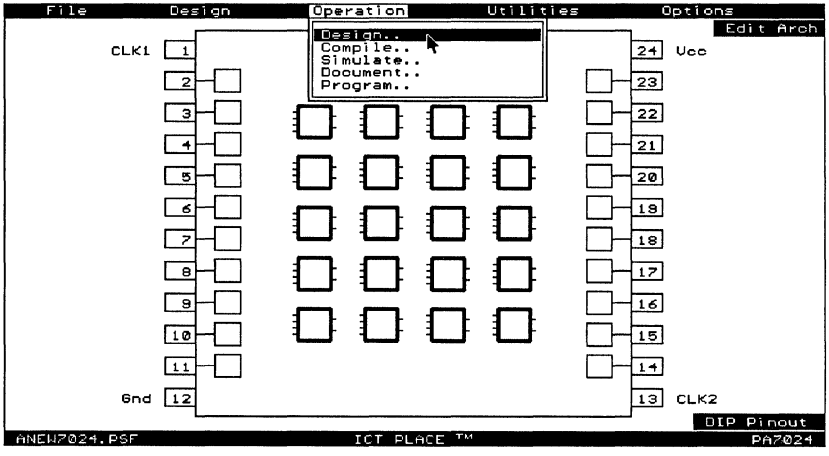


Figure 3-2, The Operations pop-down menu

*Move the mouse cursor to the "File" menu option and Click the "Read" command.* A list of the PLACE Source Files (.PSF) will appear (Figure 3-3). The design examples provided with the PLACE software include:

- Multiple-Application Design Example (PA7024, DEMO1A.PSF)
- Basic Gates (PA7024, GATES1.PSF)
- Basic Registers and Latches (PA7024, REG1.PSF)
- 8-Bit Counter with Hold, Reset and Preset (PA7024, COUNTER1.PSF)
- Bi-Directional I/O Port (PA7024, BI_PORT1.PSF)
- Bus Programmable Clock Generator/Timer (PA7024, TIMER.PSF)
- Blackjack Machine Example (PA7024, JACK7024.PSF)
- Timer/Counter (PA7140, TC7140)
- 4-Bit State Machine with 8-Bit Counter Application (ST7128, PA7128)
- Basic Gates (18CV8, V8GATES.PSF)
- Basic Registers and Latches (18CV8, V8REGS.PSF)
- Clock Divider and Address Decoder (18CV8, V8CLKADD.PSF)
- Bus Programmable 8-to-1 Multiplexer (18CV8, V8BUSMUX.PSF)
- 8-Bit Counter with Function Controls (18CV8, V8FCNTR.PSF)
- Change-of-state Input Port with Interrupt (18CV8, V8CPORT.PSF)
- Octal Synchronization Circuits (18CV8, V8SYNC.PSF)
- 16-to-4 Priority Encoder (173, PRI173.PSF)
- 8-Bit Up/Down Loadable Counter with Carry-out or Borrow-in (PEEL22CV10, V10CNT8.PSF)
- 9-Bit Even/Odd Parity Generator/Checker (PEEL22CV10A, PARV10A.PSF)
- 8-Bit Change-of-State Input Port with Interrupt (PEEL22CV10Z, V10ZPORT.PSF)

As shown in Figure 3-3, there are two methods of making a selection from the file menu window.

1. Click to highlight a file or directory, and then click at the [OK] selector.
2. "Double Click" at the file or directory. The first click highlights the selection, and the second click makes selection.

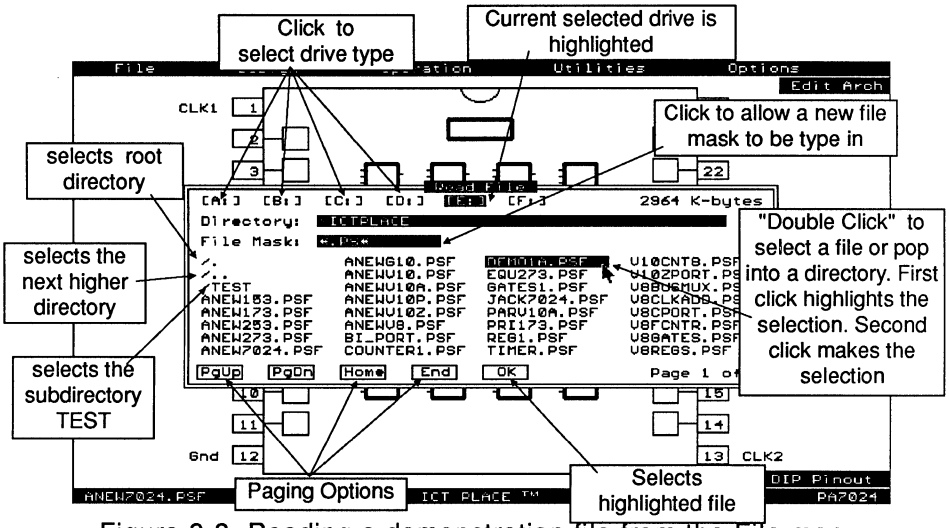


Figure 3-3, Reading a demonstration file from the File menu

3

*Click the DEMO1A.PSF file.* The PLACE Design operation will once again be displayed, but this time with the DEMO1A demonstration design file. For more detail information on the demonstration example files refer to chapter 6 of this manual.

Once the file is loaded, *move the mouse to the "Design" menu option at the top of the screen* (Figure 3-4). *Click at the "Title" command.* A window will appear on the screen displaying the title, designer and date of the design. The title of the design can

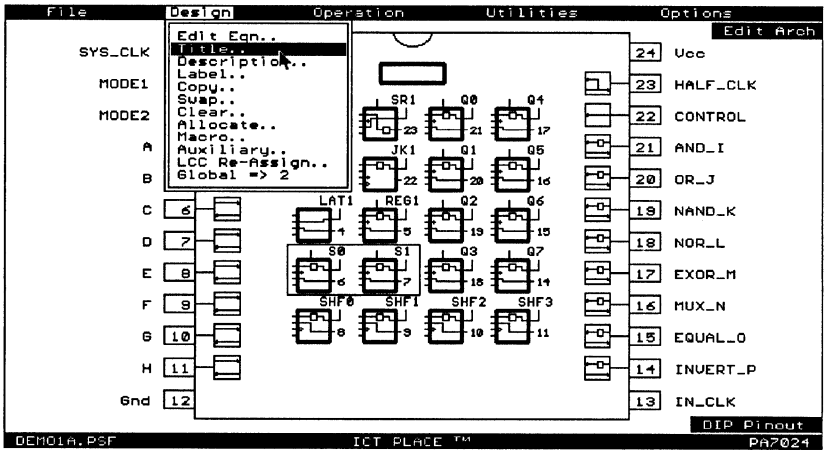


Figure 3-4, The "Design" command menu

now be entered by typing in the characters from the keyboard. *Click or press the [ENTER] key to move the cursor to the next Title field. Click-R or press the [ESC] key to exit this mode.*

*Move the mouse cursor back to the "Design" menu option and click the command listed as "Description".* The screen will now display the description of the design (Figure 3-5). *Move the mouse cursor into the displayed window and click the mouse button.* This procedure allows the design description to be entered or modified by having the PLACE software automatically open the text editor and highlight the text. *Press [ESC] to exit the text editor.*

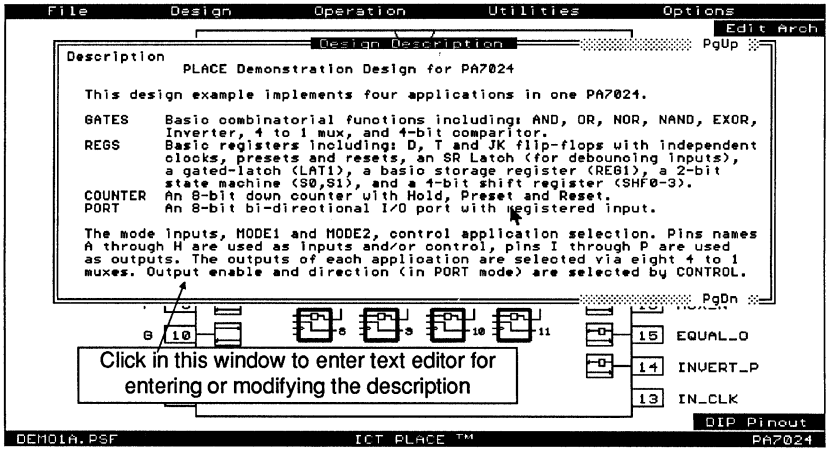


Figure 3-5, The "Description" window

With a 3-button mouse, click-R exits the text editor and returns to the previous screen. For the 2-button mouse system, click-RH (press and hold the mouse right button) to allow selection of the text editor menu at the top of the screen. Then while the right button is still held down, click at the "ESC" menu option to exit the editor. Please refer to section 4-14 on "Text Editor Commands" for more information.

*From the pin block diagram screen move the mouse cursor to the "Design" menu option and click the "Label" command.* Notice that the mouse cursor changes from a North-west pointing Arrow to a Hand cursor (the Hand cursor is available only if option #1 of the mouse cursor type was selected during the

PLACE initialization procedure). *Now move the cursor to one of the Logic Control Cells (LCCs), Input/Output Cells (IOCs), or Input Cells (INCs - PA7140 only) and click the mouse button.* A window will appear displaying the current label (or name). Figure 3-6 shows the I/O cell #2 was selected in the Label mode. To change the label use the [BACKSPACE] key and type in the new label followed by the [ENTER] key. The Label command is used to define all IOCs, INCs and LCCs that are used in a design.

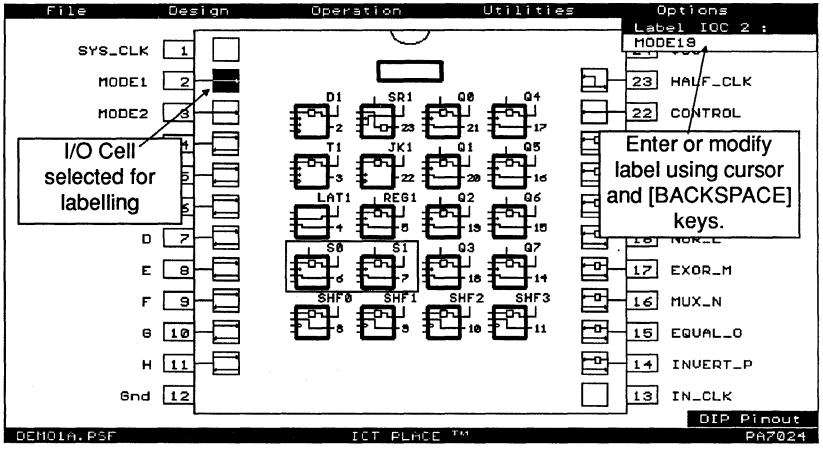


Figure 3-6, The "Label" command for Pin, INC, IOC and LCC

☞ The architecture of the LCCs, IOCs or INCs can be configured prior to labelling. However, labels must be specified before the equations, state-diagrams or truth-tables can be entered. Please refer to Chapter 4 "Operation Reference Guide" for options on the "Label" command.

*Click-R to exit the "Label" mode and return to the "Edit Arch" mode. Now, move the cursor to one of the LCCs.* Note that both the LCC and its interconnected IOC will be highlighted. *Click the mouse to bring up the associated "LCC and IOC Screen".* This screen displays a close-up view of the selected LCC and its associated IOC configuration.

*Select the configuration of the cells by clicking at any of the "select indicators"* (Figure 3-7). With the PA7024 device, over 4000 configurations can be selected by clicking at each of the

select indicators. Any time the mouse cursor is moved away from a select indicator, the pop-up window is cleared. *Click-LH (press/hold left mouse button) and move the cursor left and right or up and down.* This allows panning from one cell to another without returning to the pin block screen. Notice that the miniature pin block diagram in the upper left corner displays the current LCC/IOC location.

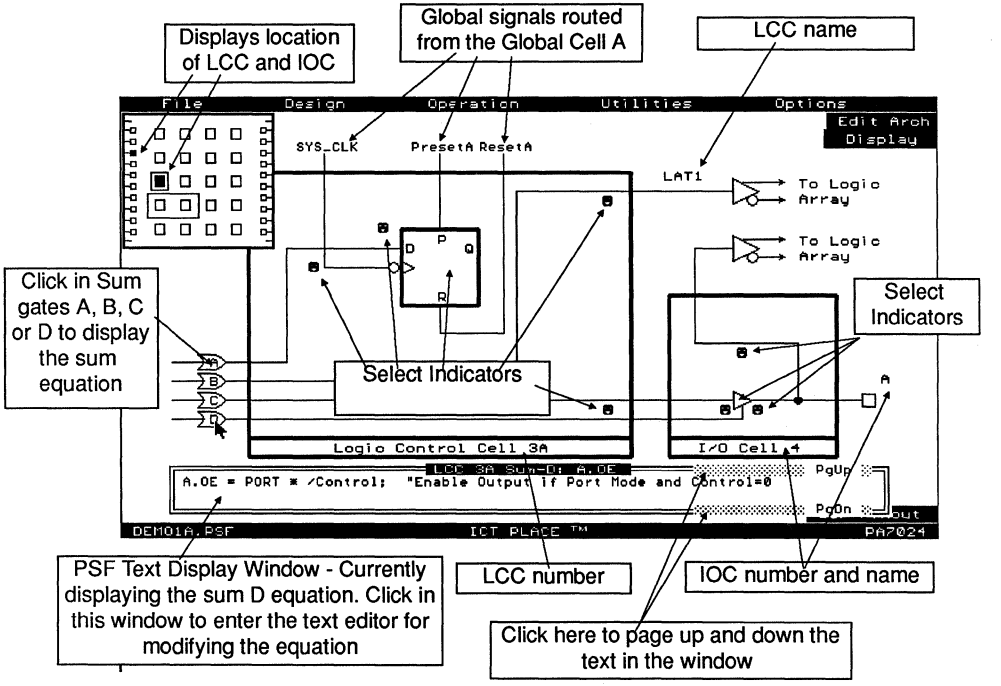


Figure 3-7, Configuring the LCC and IOC Architecture

*Move the cursor into the "D" OR or Sum-D gate (shown in Figure 3-7) and click the mouse button.* A window displaying the equation for the selected OR gate will be opened. This window will be referred to as PSF Text Display Window. The size of the window can be increased or decreased by pressing the [Up] or [Down] cursor key, and followed by the [ENTER] key (refer to Chapter 4 "Operation Reference Guide" for more information on the PSF Text Display window). *Click-R to close the display window. To return to the pin block diagram screen, click-R once again or press the [ESC] key.*

The Global Cell (GBC) configuration can be selected by the same process, i.e. by clicking the select indicators in the cell (Figure 3-8).

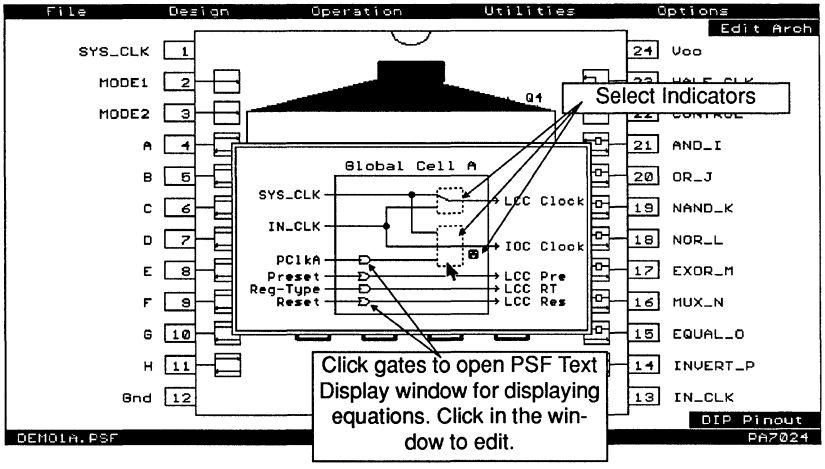


Figure 3-8, Configuring the Global Cell A (GBC) Architecture

There are multiple global cells in all PEEL Arrays. For instance, the PA7024 device has two global cells which are called Global Cell A and B. The default condition for the PA7024 (and all PEEL Arrays) is the one global cell mode. The two global cell mode can be selected by clicking at the "Global = 2" command found in the "Design" menu window. With two global cells, Global Cells A and B control global signals for all LCCs connected to the IOCs located on the left (pins 2 to 11) and right side (pins 14 to 23) of the pin block diagram respectively. Please refer to the PEEL Array data sheet for more information on the global cells.

*In the pin block screen, move the mouse cursor to the "Design" Command pop-down menu again. Click the command listed as "Edit Eqn" for edit equation.* Notice that the mouse cursor has changed to a "<-" (arrow) which is the Edit Equation cursor. *Move the cursor to one of the four inputs of any LCC and the input will be highlighted. Click to select the input equation.* In Figure 3-9, the PSF Text Display window displaying the sum-C equation was selected from the third input of the LCC "QO".

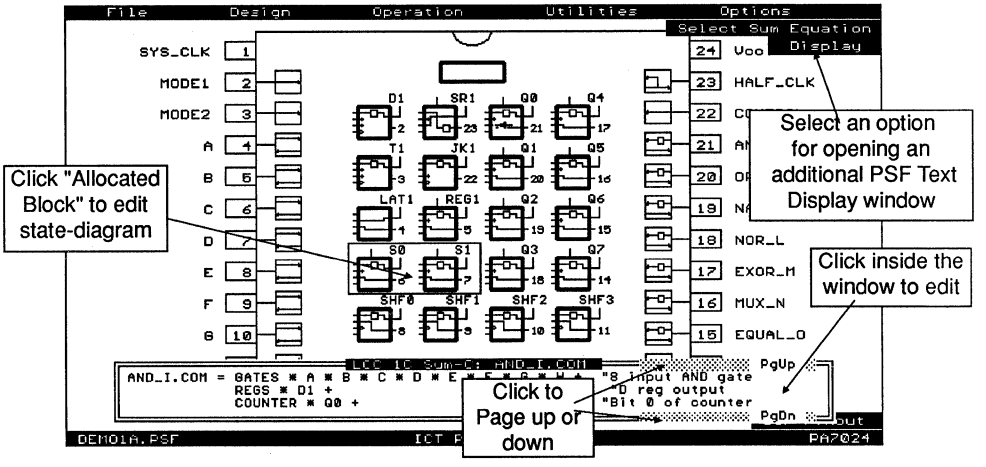


Figure 3-9, Selecting equations from the block diagram screen

*Move the mouse cursor to the "Display" option located in the upper right corner of the screen and click the mouse button.* This opens a window listing the options for opening an additional PSF Text Display window. *Move the cursor to highlight the "Macro Definition" option and click the mouse button.* The PSF Text Display window showing the macro definitions specified in the design will appear (Figure 3-10).

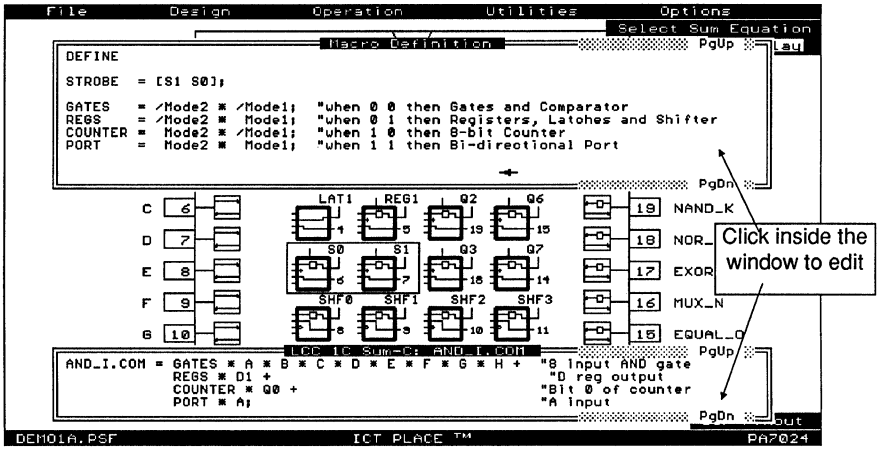


Figure 3-10, Selecting equations from the block diagram screen

*Move the cursor to the inside of the PSF Text Display window and click the mouse button.* This enters the text editor which is used for editing boolean equations, state diagram and truth table syntax. The selected equation will be highlighted (Figure 3-11). Note that equations can also be selected for the LCC/IOC screen by moving the cursor to the one of the four "Sum" inputs and clicking the mouse button (Figure 3-7). Equations for the Global Cell can also be selected this way (Figure 3-8). Once inside the editor, most of the standard Wordstar™ commands can be used (see Chapter 4 for the command reference information on the text editor). *Click-R or press the [ESC] key to return to the pin block diagram screen again.*

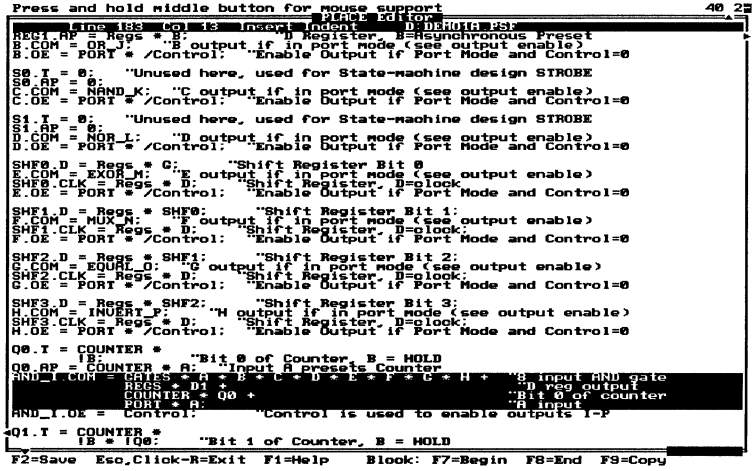


Figure 3-11, Inside the PLACE text editor

After returning from the text editor, the "Edit Eqn" mode is still selected (indicated by the "<-" mouse cursor). *Click-R and the cursor will change back to the default "Edit Architecture" cursor.* Click-R will toggle back and forth between Edit Equation and Edit Architecture for quick access to both modes.

If you have followed the instructions up to this point you have now familiarized yourself with the basic functions of the Design operation in the PLACE software. *Now, move the cursor to the "File" menu option and click the "SaveAs" command.* The file window will appear (figure 3-12). *Move the cursor to the box named "NEW" and click the mouse button. Type in the name "TEMP" or any other new name to save your modified file.* If the file extension is omitted, then it will be defaulted to ".PSF".

*Once your Design file is saved, select the File pop-down window again and read in the "GATES1.PSF" design example.*

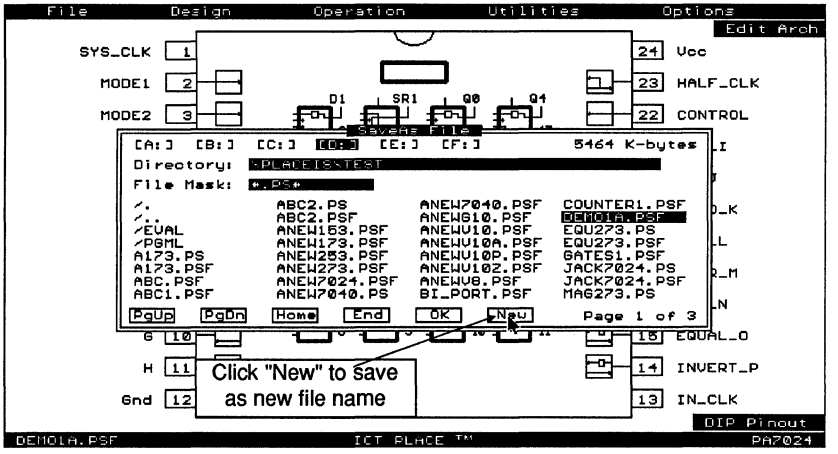


Figure 3-12, Using "SaveAs" to save a new PLACE source file

*Move the mouse cursor to the Operations pop-down window and try selecting the other operations starting with Compile, Simulate, Document, Program and back to Design.* The screens should look as displayed in Figures 3-13 through 3-16. For more information on the commands and functions in the five main operation, please refer to the "Operation Reference Guide" in Chapter 4.

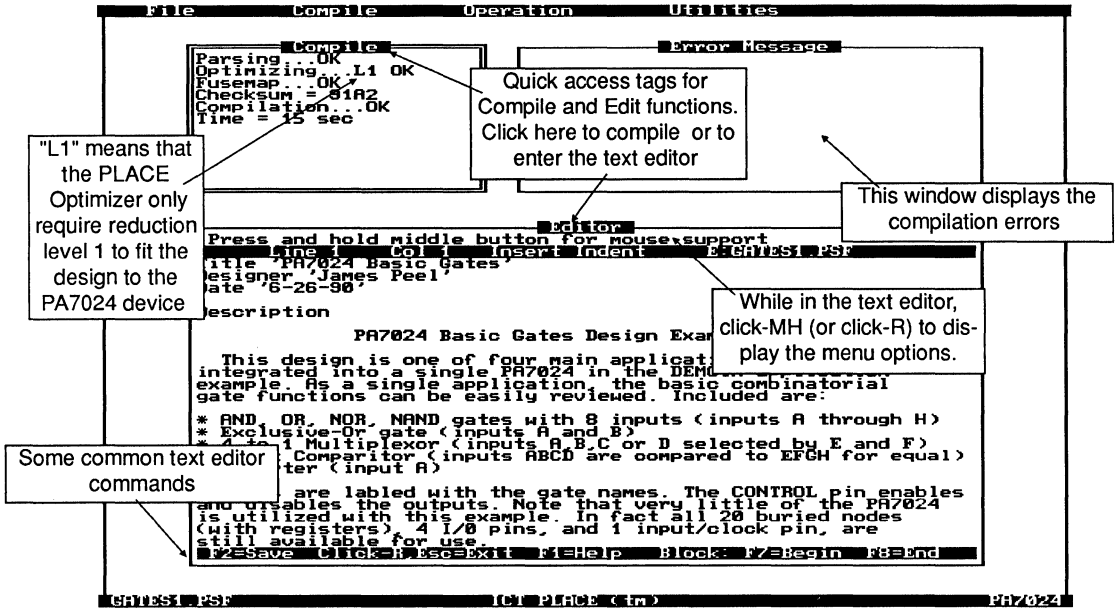


Figure 3-13, The Compile Operation Screen (Standard version only)

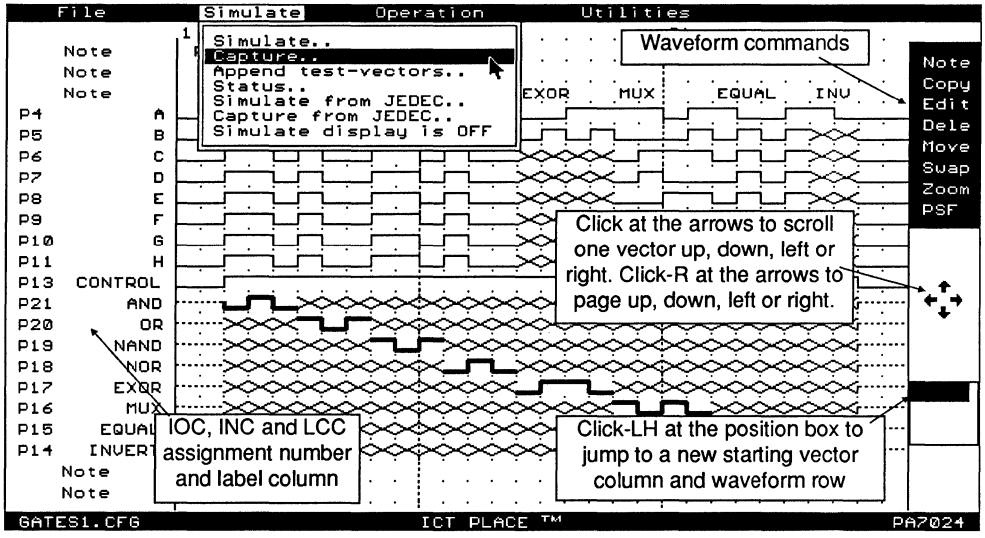


Figure 3-14, The Simulate Operation Main Screen

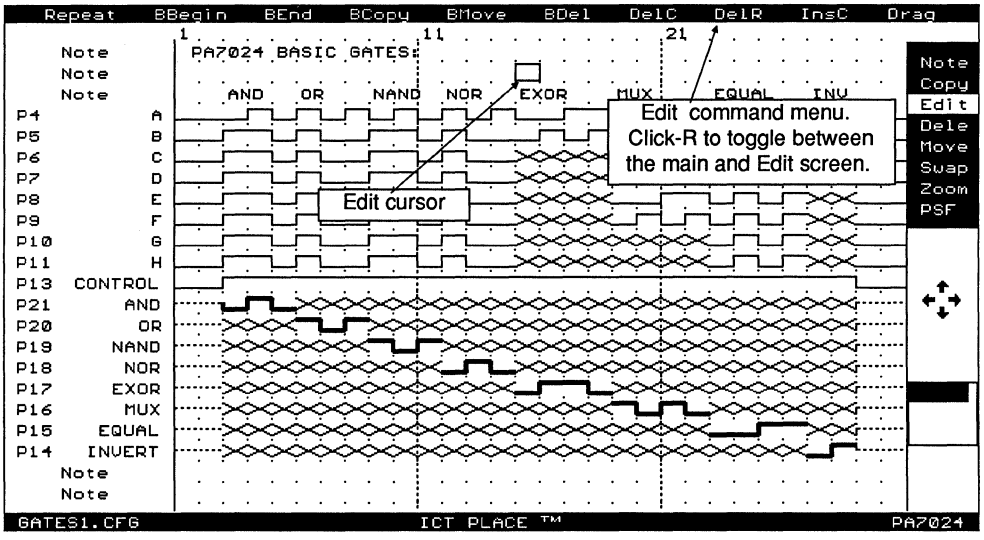


Figure 3-15, The Simulate Operation "Edit" Screen

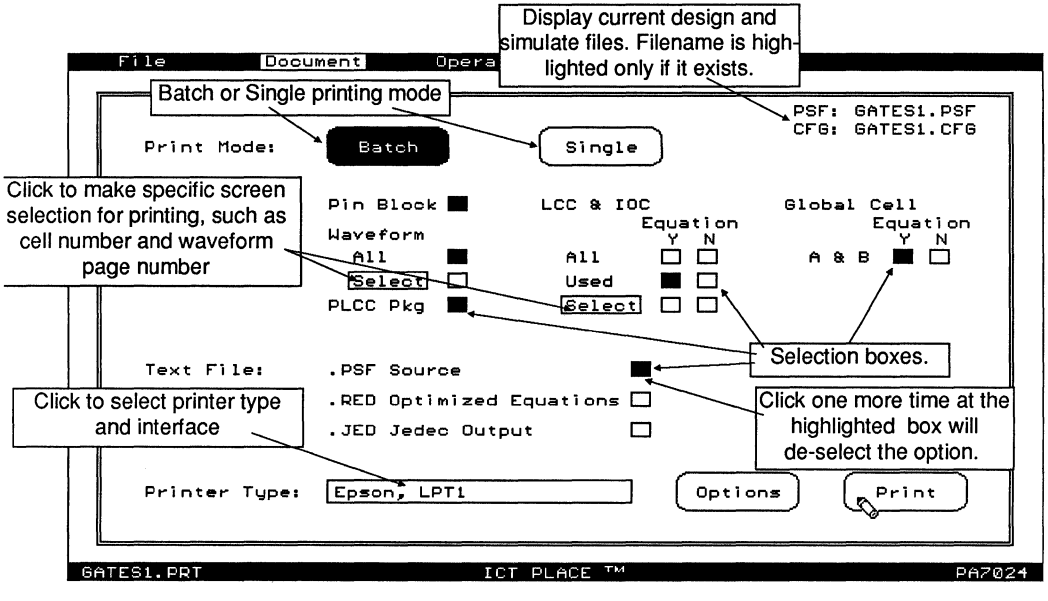


Figure 3-16, The Document Operation Screen

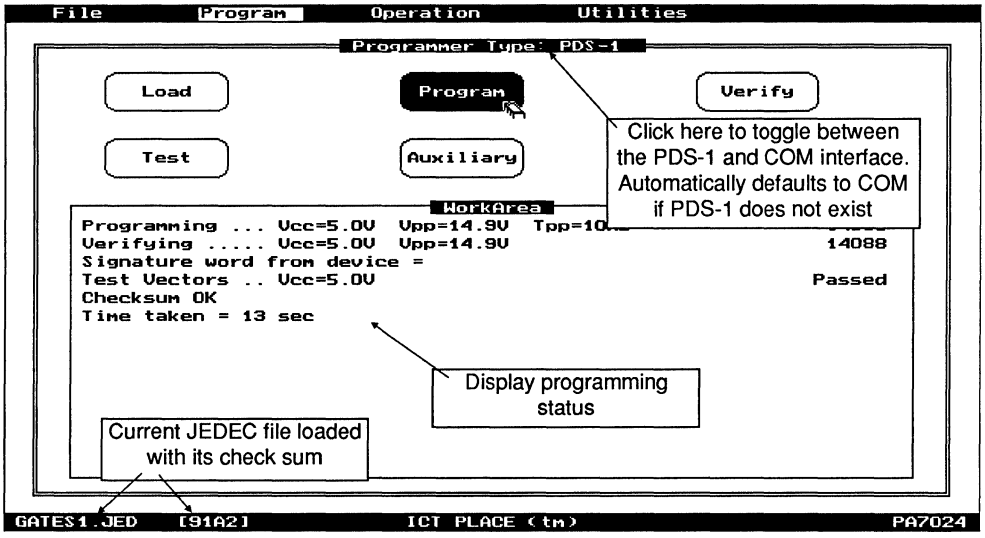


Figure 3-17, The Program Operation Screen (PDS-1 Interface)

## 3.5 The PLACE Design Process

Starting a new design can be accomplished by selecting the "New" command in the "File" menu option while in the Design Operation. This command loads the ANEW file which clears all of the pin and cell (INC, IOC and LCC) names. Note that when a cell is cleared, it will be set to its default configuration. Once this is done a new design can be entered. The following chart lists the typical procedure for implementing a design using PLACE. Please use this as a "road map" for implementing your PLACE designs while referring to the Operation and Language Reference Guides in Chapters 4 and 5 of this manual.

### Design

1. Select "New" from the "File" menu option.
2. Enter "Title" and "Description" from the "Design" menu option.
3. Label all the pins (IOCs and INCs) and LCC (node) names to be used in the design by using the "Label" command.
4. Configure the architectures of the INCs, IOCs and LCCs for the design. Use the "Copy" command to copy or dupli-

cate the INC, IOC or LCC configurations if needed. Use the "Swap" command to move pins, INCs, IOCs and LCCs for desired positioning.

5. For state-diagrams and truth-tables, use the "Allocate" command to allocate the labeled IOCs and/or LCCs for the state machine and truth-table designs.
6. For boolean equation design entry, select the Edit Equation ("Edit Eqn") mode and enter the equations for each LCC input. The equation entry can be done via the pin block or LCC and IOC screen.
7. Edit or modify the architectures and equations until ready to compile. Make sure to save the design through the "File" menu option or by pressing ^S (Ctrl-S).
8. If desired, use the "Swap" command again to reposition the pin and cell locations.
9. Pull down the "Operation" menu and select the Compile operation.

☞ Through out the design process, it is a good practice to periodically save your design. You can do this with the "Save" function in the "File" pop-down menu or hold the [Ctrl] key down and press "S" (^S).

**Compile (standard version only)**

1. If coming directly from the Design operation (i.e., with the design file loaded), select the "Compile" command menu and click the "Run" command. If the design file was not loaded prior to entering the Compile operation, then "Read" the appropriate source (.PSF) file from the "File" menu window.
2. If a compile error occurs, the compiler will indicate the error with a message and locate the error in the displayed source file. You may analyze the error and correct it within the compile operation (by clicking the "Editor" title bar to enter the editor). You may also return to the Design operation to correct the error. If the compilation is ok, proceed to the Simulate operation.

**Simulate**

1. Enter the input pin waveforms using the "Edit" command.

2. Enter expected output wavforms for test verification or use the "Capture" command in the "Simulate" menu window to automatically generate the output waveforms.
3. After simulation, click at the "Status" command to check if there are any simulation failures. Correct all simulation failures either by changing the vectors, or by returning to the Design operation and modifying the design.
4. Once properly simulated, append the vectors to the JEDEC file using the "Append test vectors" command from the "Simulate" menu window.
5. Save the ".CFG" simulation file using the "File" menu window. Like the design operation, periodically save your simulation (.CFG) files by pressing "^S". It is recommended to save your first simulation vector file with the ".CFG" file extension. Any vector file can be saved with the extension ".CFx", where x is an alphanumeric character.



### Document

1. In the Document operation, select the printer type and interface if you are running the PLACE Document operation for the first-time.
2. Select the Batch or Single option.
3. Click in all the desired print options, such as pin block diagram, PLCC package pinout, cell architectures, simulated waveforms and design texts (such as equations, state-diagrams or truth-tables).
4. Once the options are selected, click the "Print" command to send the documents to the printer.
4. Save your selections onto your hard disk. The filename will consists of the root filename with extension ".PRT".

### Program

1. If a JEDEC file exists for your current design, then the JEDEC file will automatically be loaded upon entering the Program operation. If the JEDEC file does not exist, then "Read" the JEDEC file via the "File" menu window.
2. Select the "Program" command for programming with the ICT PDS-1 programmer or the "Transmit" command for down-loading to a third-party programmer via the serial communication port.

# Operation Reference Guide

# 4.0 Operation Reference Guide

In this section, the features in the PLACE software are discussed in more detail. Sections 4.1 to 4.3 detail the features or functions that are similar in all PLACE operations. Then, the features specific to each of the operation are discussed in the following sections.

## 4.1 File Menu

The "File" menu option shown in Figure 4-1 provides options for file maintenance, system information and screen dump to IBM/Epson printer (additional printer support in Document operation) via the parallel port. This file menu is similar in all operations (i.e. Design, Compile, Simulate, Document and Program operations) with the exception of the type of file (see Table 4-1 for PLACE file types) that is read or saved.

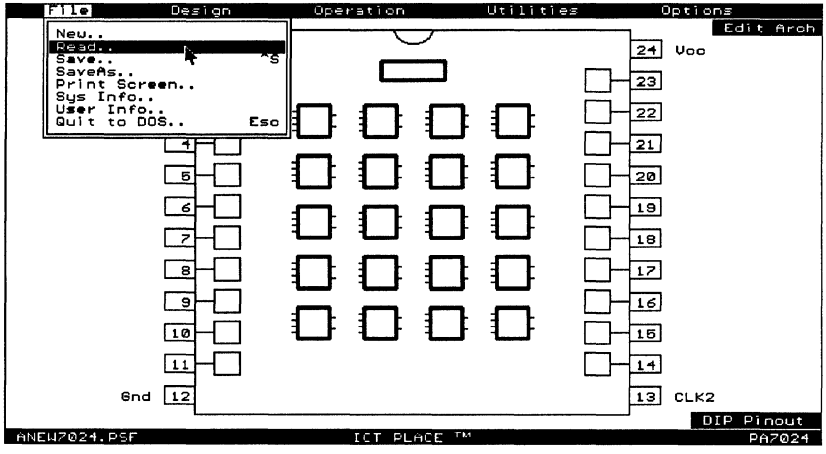


Figure 4-1, File Menu Option

New ..... When in Design operation "New" clears the file in memory and allows device selection for starting a new design. Loads "ANEWxxxx.PSF" (xxxx = device number) as a template file. The PLACE software automatically prevents your edited ANEW file from overwriting the original file by prompting for a new file name during the "Save" command.

Read ..... Allows a PSF source, simulation, documentation or JEDEC file to be loaded from the current directory in the current operation (e.g. loads PSF file in Design operation, CFG in Simulate operation, and etc. - refer to the Table 4-1). When selected, the File selection window will appear (Figure 4-2):

- A file can be read by clicking the desired file name and clicking the [OK] selector. For quick selection, you can do a "double click", i.e. click twice on the same file name (first click highlights the file, and the second click selects the file).
- New drive is selected by clicking the drive letter at the top of the directory window.
- New directory is selected by clicking the directory name preceded by a "/", or clicking the "/.." (next higher directory) or "/." (root directory). The selection action is similar to selecting a file, i.e., click the [OK] selector or "double click" the selection.
- New file mask can be changed by clicking the file mask highlighted area and typing in the file mask. Use the [Backspace] key, cursor keys or the mouse to move the text cursor. Press the [ENTER] key or click the mouse when completed. Default is "*.PS*". After the file is read, the name will appear in the lower left corner of the pin block screen.

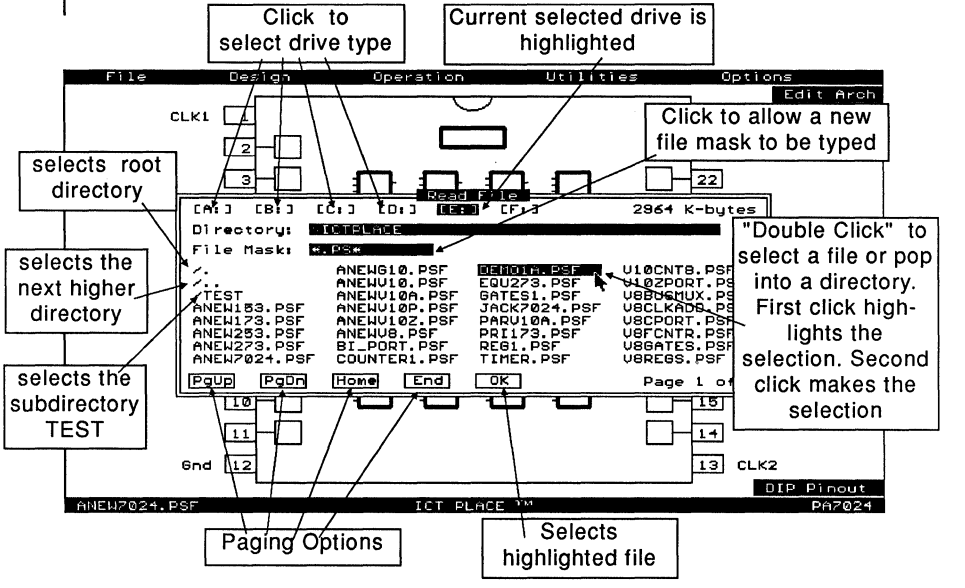


Figure 4-2, "Read" file selection screen

Save ..... Saves the current file to disk. If the file is a new design (i.e. an ANEW file), then a new file name will be prompted for.

SaveAs ..... Allows a new file to be saved to the current directory and disk. Click an existing file to over-write or click [New] selector to enter a new file name (the "SaveAs" file selection screen is similar to that of the "Read" screen in Figure 4-2 with the exception of the [New] function).
**Note that in the Simulate operation if the root name of the CFG simulation file is not changed, then the file will still reference the same PSF design file. An example is shown below.**
DEMO1A.CFG saved as DEMO1A.CF1 - both files reference the DEMO1A.PSF design during simulation.
DEMO1A.CFG saved as DEMO1B.CFG - these files reference DEMO1A.PSF and DEMO1B.PSF design respectively during simulation.

Print Screen .... Sends current screen to the IBM or Epson graphic printer. For more printer support such as HP Laserjet and Postscript printers, please refer to the Document operation.

Sys Info ..... Displays system information such as file name, current directory, memory usage and etc.

User Info ..... (PLACE Standard version only) Displays information about the user, such as company name and address, user's name and date of installation.

Quit to DOS .... Quits PLACE program to DOS.



| File Extension | Function |
|---|---|
| PSF | PLACE Source File (PSF) is the design source file used by the Design and Compile operations. |
| PS | Back-up file for the PSF design file. |
| MAP | Output file from the PLACE Compiler. This file provides detailed information of how the design equations are mapped into the JEDEC file. This information may be useful for design debugging. |
| RED | Output file from the PLACE Optimizer (prior to fuse mapping) in the Compile operation. This file contains the reduced or optimized equations in the sum-of-product form. It maintains the PLACE design format so that it can be read into the Design operation for design verification and |

Table 4-1, PLACE File Types

| | |
|---|---|
| | debug, or into the Document operation for documentation purposes. Note that the unused equations are omitted, so you will get "Equations not found" errors in the Design operation. |
| JED | Output JEDEC file from the PLACE Compiler and is used by the Simulate and Program operations. |
| JE | Back-up for the JED file. |
| INT | Output file from the PLACE Compiler. This file contains the IOC and LCC interconnects which are used for the waveform display in the Simulate operation. |
| CFG | Primary vector source file for the Simulate operation. This file contains the data for vector simulation and waveform display. The PLACE Simulator simulates the vector in the CFG file with reference to the PSF design file with the same root file name. Hence, other file extensions may be used for the vector source file instead of CFG. However, **we recommend using the CFG extension for your primary source file because all PLACE operations automatically reference to the CFG file during the operation switching process.** |
| CF(n) | (Recommended ) Alternate vector source file for the Simulate operation. The character "n" can be any alphanumeric character except of course "G". This file extension method is used for the convenience of displaying all the vector files in the directory pop-up window, i.e. with the file mask *.CF*. Remember that the vector source files with the same root file name reference the same PSF design file. Example, the DEMO1A.CFG and DEMO1A.CF1 are vector files for the DEMO1A.PSF design file. |
| PRT | Input file for the Document operation. This file contains print selection tags for documenting the design. |
| PR | Back-up for the PRT file. |
| PN1 | Default file extension for the output file from the PLACE Document operation (any file extension can be used with the exception for those that are specified in this table). The Document operation has a "Print to file" option which directs the screen capture data to this file. This file can then be sent to the printer using the DOS Copy command. |

Table 4-1, PLACE File Types (Continued)

## 4.2 Operation Menu

When an operation is selected from the "Operation" menu (Figure 4-3), the PLACE software automatically loads the proper input file for the selected operation. For instance, the PSF file is loaded for the Design and Compile operations, the CFG file for the Simulate operation, the PRT file for the Document operation, and JED (JEDEC) file for the Program operation.

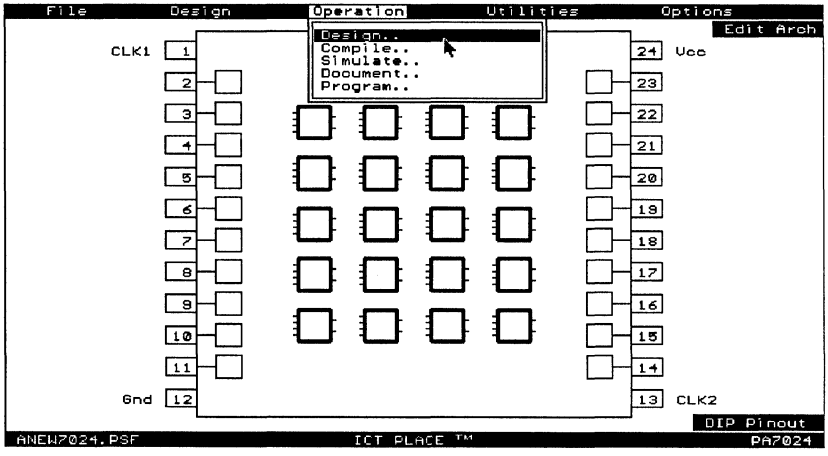


Figure 4-3, Operation Menu Option

Design ..... Selects Design operation for creating a PSF design source file. The PSF file (if exists) will automatically be loaded.

Compile ..... Selects Compile operation for compiling the PSF design source file to create a JED (JEDEC) file for simulation and programming use. The PSF file (if exists) will automatically be loaded upon entering the Compile operation.

Simulate ..... Selects Simulate operation for creating a CFG vector source file which can be edited and simulated to the JED file. The CFG file (if exists) will automatically be loaded.

Document ..... Selects Document operation for documenting the design via printing the graphic screens and text files. If it exists, the PRT file will automatically be loaded. If the PRT file does not exist, then the print selection tags will be set to the default settings.

Program ..... Selects Program operation for programming a PEEL Array or PEEL Device with the JED (JEDEC) file. The JED file (if exists) will automatically be loaded.

## 4.3 Utilities Menu

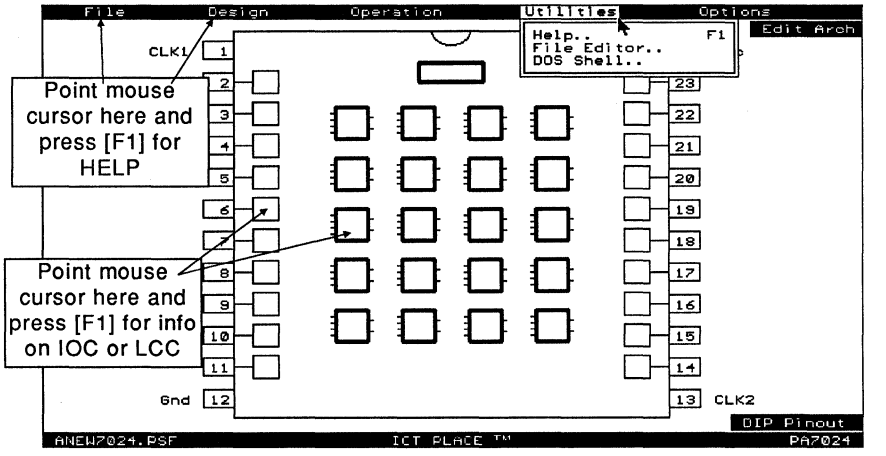


Figure 4-4, Utilities Menu Option

Help ..... Provides general information on the Help instruction. For individual Help per command, move the mouse to the command in the menu window and press the [F1] key. See Figure 4-4 for additional Help locations.

File Editor ..... Enter the file or text editor. To exit the editor press the [Esc] key or click-R if using a 3-button mouse. Refer to the "PLACE Text Editor" section in this chapter for more information on the editor commands.

DOS Shell ..... Enters a DOS shell. This feature temporarily exits the PLACE software. Type "EXIT" in the DOS shell to return to the PLACE software. Upon returning from the DOS shell, the previous set-up conditions will be restored. This means that the previous settings and the edited file is saved to disk and will be loaded automatically into the PLACE software. If EMS is available, it will be used to save the settings and file.

## 4.4 Design Operation - Design Menu

The "Design" menu contains commands used for implementing PEEL Array and PEEL Device designs. Note that some design commands such as "LCC Re-assign" and "Global => 2" commands are only applicable to the PEEL Array designs. The two cursor types used by some of the commands in the "Design" menu are the "Left Arrow" and "Hand" cursors.

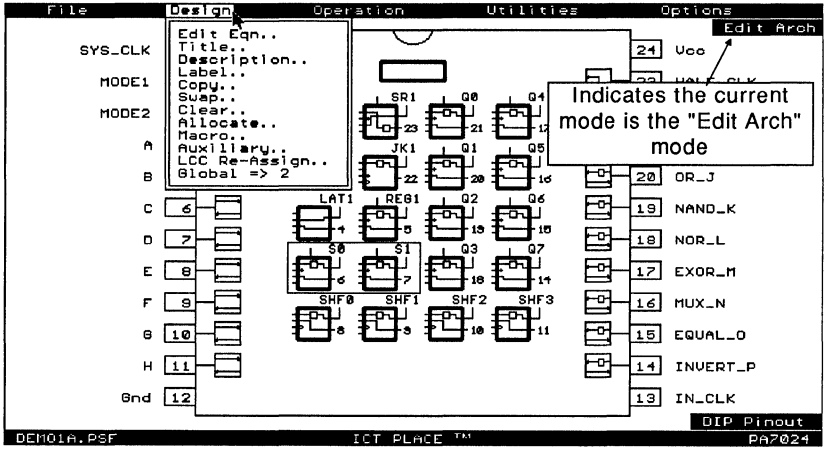


Figure 4-5, Design Menu Option

☞ In the PLACE software, all commands that are not applicable to the selected device will be disabled.

Edit Eqn ..... Selects Edit Eqn mode (also selected by clicking-R in the Edit Arch mode). This mode is identified by the left arrow mouse cursor (<-) if a 3-button mouse is used. In the "Edit Eqn" mode (also refer as "Select Sum Equation" mode), there are three ways of entering a logic description.

1. **Equation:** Move the cursor to highlight the OR (Sum) gate, and click to bring the sum equation out. Note that the equations for each cell are created by the label command. Hence, all cells must be labeled prior to selecting their OR gates.
2. **State diagram:** Move the cursor into the state diagram box without highlighting any of the OR gates in the LCC selected for the state diagram design. Then, click to open the window with the state diagram syntax. The requirement for designing with the state diagram syntax is that the cells

(LCCs and IOCs) must be allocated by using the "Allocate" command.

3. **Truth table:** Click at the T(n) labels located at the bottom of the LCC or IOC to open the window for displaying the truth table design syntax. Like the state diagram design, cells used in the truth table design must first be allocated.

After opening the window to display the design syntax (this window will be referred to as **PSF Display window**), move the cursor into the window and click to open the text editor for entering and editing the design syntax. Press the [Esc] key or click-R to exit editor. Refer to section 4.28 for the text editor commands.

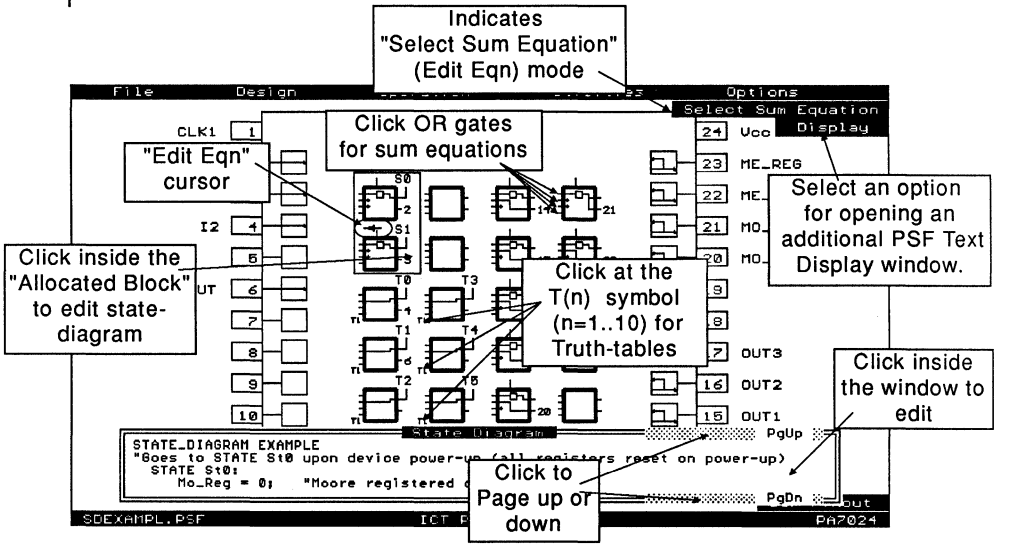


Figure 4-6, Edit Equation Mode

Title ..... Allows a title, designer's name and date to be entered into the source file.

Description ..... Opens a window to display the design description. The window size can be adjusted by pressing the Up or Down cursor keys followed by the ENTER key, or using the **"Display"** menu (see section 4-6). Paging can be accomplished by clicking at the PgUp or PgDn markers, or using the PgUp or PgDn keys. To enter the PLACE text editor for editing, click inside the displayed window. There is no limitation in terms of the type of characters you can use for describing your design, just as long as your description is specified within the reserved words "DESCRIPTION" and "END_DESC". Note you can use

the reserved word "DESCRIPTION" but not the word "END_DESC".

Label ..... Enters the "Label" mode so that any LCC, IOC, INC or pin can be labeled. After a LCC or IOC is labeled, the equations related to the labeled cell are automatically generated in the source file (all equations equate to 0) . The number and type (sum or product equations) of equations generated depends on the device type and the configuration of the cell (Table 4-2). **In PEEL Arrays, note that the equations are generated only if both the LCC and its associated IOC are previously unused or unlabeled.**

If the label for the LCC or IOC is deleted and its associated cell (IOC or LCC) is unused, then all the equations are automatically deleted.

Below is an example of the four equations generated for a labeled PA7024 LCC (assume the label is "!TEST").

**Example:**

| Configuration | Equations generated |
|---|---|
| D-type flip-flop | !TEST.D = 0; |
| Async. Preset | !TEST.AP = 0; |
| Async. Reset | !TEST.AR = 0; |
| Assigned IOC is an I/O type | !TEST.OE = 0; |

Assume that the flip-flop's output of the LCC is connected to the IOC.

| PEEL Device | Number of equations per IOC |
|---|---|
| 18CV8, 22CV10 22CV10Z, 22CG10, 22CV10A/A+, 173 | 1 sum equation, 1 product equation |
| 273 | 2 sum equations |

| PEEL Array | Number of equations per LCC/IOC pair |
|---|---|
| PA7024, PA7140 PA7128 | 4 sum equations |

Table 4-2, Number of Equations per IOC or LCC/IOC pair

## Labelling Methods

Below are the three methods of labelling cells and pins.

1) **Click and Type method:**
This is the normal method of labelling the cells or pins. Move the mouse cursor and click the mouse button to select the cell or pin. Type in the label and press the ENTER key or right button of the mouse to complete the label procedure. Repeat this procedure for all cells and pins.

2) **Group (Set) method:**
The group or set method is designed for labelling a group of cells or pins with names that differ by a single alphabet character or a set of numbers. Some examples of the group names are: ModeA, ModeB, ModeC; AD0, AD1, .., AD15; and A0, A1, .., A12.

The first step in implementing this method is to click at a cell (IOC, INC, LCC or pin) which will be the starting cell, i.e. the first label in the group will be assigned to this cell. If the starting cell is an IOC, INC or pin, then the labels will be assigned to the next cell or pin **in ascending order**. For PEEL Arrays, if the starting cell is a LCC, then the labels will be assigned to the subsequent LCCs in ascending order (i.e. 1A, 2A, .., 1B, 2B, ..,5D). After the starting cell has been selected, type the *group name* in the label window.

**Format of the group name is:**

prefix name + [A..Z] + suffix name
+ [Z..A] +
+ [1..n] +
+ [n..1] + (where n > 1)

Some examples are:

| Group Name | Assigned Labels |
|---|---|
| Q[0..3] | Q0, Q1, Q2, Q3 |
| ADDR[9..13] | ADDR9, ADDR10, ADDR11, ADDR12, ADDR13 |
| D[99..102]_IN | D99_IN, D100_IN, D101_IN, D102_IN |
| OUT[1000..998] | OUT1000, OUT999, OUT998 |
| IN[51..49]DATA | IN51DATA, IN50DATA, IN49DATA, IN48DATA |
| [A..C]10 | A10, B10, C10 |
| ![Z..X]1 | !Z1, !Y1, !X1 |

3) **Keyboard method:**
Like the Group method, the keyboard method also allows labels to be assigned quickly. However, this method is more suitable for assigning labels which are significantly different from each other, i.e. they differ by more than two alphabet characters. Some of the label examples are INPUT, OUTPUT, ADDRAA, ADDRBB, OE, READ, !WRITE and etc. Normally to assign these labels you would need to implement the "Click and Type" method. But, performing this click and type task repeatedly for twenty cells is a very tedious job. The "Keyboard" method shortcuts this task by bypassing the mouse click procedure.

In this method, you should first click on a cell (or pin) which you want the label to start from (defaults to the first pin if no pin or cell is selected). After typing in the label, press the [ENTER] key to implement the assignment (like in the "Click and Type" method). If the [ENTER] key is pressed the second time, the hand mouse cursor automatically advances to the next cell **in ascending order**. You can now type in the label for the current selected cell, and then press the [ENTER] key twice to advance to the next cell. Repeat the procedure until all the cells are labeled. **Please note that if you move your mouse cursor at any time during this mode, the "Keyboard" labelling will be aborted.**


Note that all three methods of labelling cells and pins can be used in conjunction with each other. The "Click and Type" method can be used to select a new starting cell for the "Group" and "Keyboard" methods.

## Renaming labels

The Label function can also be used for renaming the pins, IOCs, INCs or LCCs. During the renaming process, the previous labels used in the IOC, INC and LCC configuration, DEFINE, STATE_DIAGRAM, TRUTH_TABLE and EQUATIONS sections will automatically be replaced by the new label. This replacement process allows the user to change the pin or cell

labels with ease so that the labels that are used throughout the PSF file need not be manually changed. An example of the label replacement is:

| | Before Change | After Change |
|---|---|---|
| Pin Label | TEST | /TEST1 |
| Equations | OUT.COM = A & TEST | OUT.COM = A & TEST1 |
| | OUT.OE = /TEST | OUT.OE = /TEST1 |

As seen in the previous example, the replacement process only replaces the label. Even though the input signal active level is changed, the logic of the equation remains unchanged. For instance, the OUT output which is controlled by the OUT.OE equation is enabled on a FALSE or OFF condition. With the TEST input the FALSE condition is a HIGH signal. On the other hand, the FALSE condition for the /TEST1 input is a LOW signal.

Copy ..... Copies the selected LCC's, IOC's or INC's configuration into another cell. This will not copy the equations. Select the "Multiple" option in the Copy Type window for doing multiple copying (Figure 4-7), i.e. copying from one cell into many cells. Select "Done" to complete the current "Multiple" copying set and to start another. The only restriction in the "Copy" mode is that the source and target cells must be of the same type, i.e. LCC to LCC, IOC to IOC and INC to INC.

Swap ..... This mode allows swapping of LCCs, IOCs, INCs or pins to reorganize your design. The functions of the cells do not change. There are two restrictions when swapping the two cells.

1. Both the source and target cells must be of the same type, i.e. LCC with another LCC, IOC with another IOC, and INC with another INC.
2. For PEEL Arrays, the swapping of IOCs or LCCs are not permitted if the two global cell mode is used and if one of the following is true: a) the cells that are being swapped are IOCs which are located on the opposite sides of the pin block diagram; or b) the cells that are being swapped are LCCs which are connected to IOCs that are located on the opposite sides of the pin block diagram.

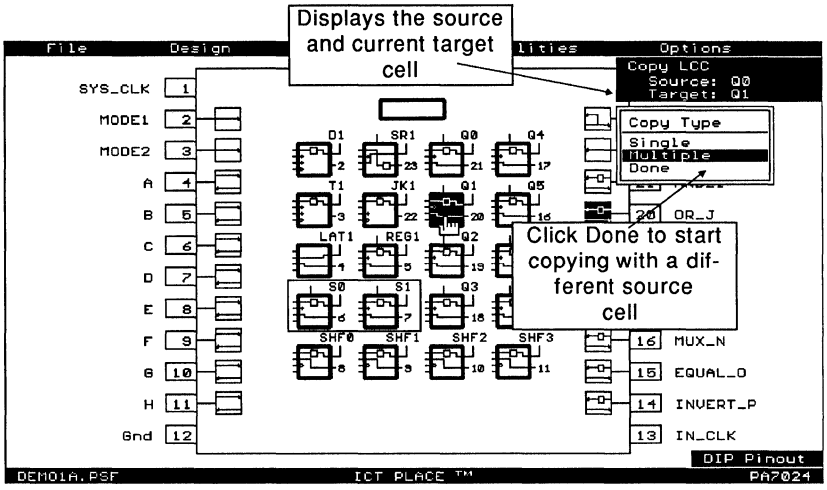


Figure 4-7, Copy Mode

Clear ..... Clears the LCC, IOC or INC. This sets a default configuration to the cells and re-name the sum output names to the new configuration. After clearing both the LCC and its assigned IOC, then all the sum equations associated with this cell are deleted.

Allocate ..... Allocates the LCC or IOC for state-machine or truth table design. Before the cell can be used for allocation, it must first be labeled. This mode also allows a state-machine or truth table design to be created, deleted or modified. For state-machine design, the allocated cells will be surrounded by a border. For truth table design, the allocated cells will be indicated by "In" and "Tn" (inputs and outputs respectively), where n ranges from 1 to 10. Note that only the outputs of the truth table ("Tn") will be marked after exiting the "Allocate" mode. See sections 4.10 and 4.11 for detailed descriptions of the state diagram and truth table designs.

Macro ..... Displays the macro definitions in the PSF design file. Macro definitions are text statements which succeed the keyword "DEFINE" but precede one of the following reserved words: STATE_DIAGRAM; TRUTH_TABLE; or EQUATIONS. The size of the window follows the number of lines set for the Option Display window option in the "Display" menu (refer to section 4-12). The window size can be adjusted by pressing the Up or Down cursor keys followed by the ENTER key, or using the "Display" menu. Paging can be accomplished by clicking at the PgUp or PgDn markers, or using the PgUp or PgDn keys. To

enter the PLACE text editor, click inside the displayed window.

Auxiliary . . . . . Additional functions such as Security Bit, Signature and Zero-Power options which are found in the Peel Arrays and in some PEEL devices. Below is a brief description of each function but you should refer to the ICT data book for more information.

**Security Bit** - Setting this feature ON enables the security bit to be programmed on the device (inserts the "G1" field in the JEDEC file). Once the security bit has been programmed, the design programmed into the device cannot be read back (except for the Signature Word). All PEEL products provide the security bit feature except for the PEEL173 devices.

**Signature Word** - The Signature Word of the device allows a user ID to be stored in the device so that it can be read back for design verification even after the security bit has been programmed. Devices with the Signature Word (number of 8-bit bytes in parenthesis) are PA7024 (8 bytes), PA7140 (2 bytes), PA7128 (1 byte), PEEL22CV10Z (3 bytes), PEEL22CV10A+ (3 bytes), and PEEL273 (2 bytes).

Example: Signature = ABC [ENTER]
(converts the characters A, B, C to the ASCII values 65, 66 and 67 respectively. Each character requires an 8-bit byte)

**Zero-Power** - When the Zero-Power bit of the device is set to ON, the device goes to "sleep" in which a low standby current condition is entered. This feature is available only in the PEEL22CV10Z device. For more updated information on the current consumed, timing and other restrictions, please refer to the PEEL22CV10Z data sheet.

LCC Re-Assign . . (PEEL Arrays only) Allows the two internal and external outputs of the LCC to be separated and re-assigned. Below lists the requirements for re-assigning the LCC.

1) The IOCs and LCCs of both source and target cells must be labeled.
2) The internal and external LCC outputs must not be sharing the same sum term, i.e they must be from separate sum terms.
3) All sum terms must be used, i.e. the output equation extensions must not contain the ".SUMx" extension where x = A..D for sums A through D.
4) The source and target LCCs must have the same configurations prior to the re-assignment. Use the

"Copy" function to copy the configurations of the LCC (and possibly the IOC too) from the source to the target cell. All LCCs and IOCs can be re-configured later for your specific application requirements.

**Example:**
Figure 4-8 illustrates a typical example which requires the LCC re-assignment feature. In this example, a design modification is required to make the output "TESTOUT" synchronous with the clock "CK1". Currently, the output "TESTOUT" is a combinatorial output. This output would need to become a registered output in order to be synchronous with the clock "CK1". The problem is that the register in the LCC associated with this output is already being used for another function. The internal output "IN" for the LCC 3C can be duplicated by copying the configuration of the LCC 3C into an empty LCC and retyping the equations. However, a faster method is to use the "LCC Re-Assign" command which separates the output "IN" from the LCC 3C and re-assigns it to another IOC with an unused LCC (LCC 4C or 5B).

The procedure for re-assignning the internal output "IN" in LCC 3C is as follows:

1) Change the configuration of the LCC 3C and IOC "TESTIN" so that all the sum terms are used. In this example, set the IOC "TESTIN" to an I/O type instead of input only.
2) Label the LCC 4C which will be the target cell.
3) Copy the cell configurations, using the LCC 3C "IN" and IOC "TESTIN" as the source cells. The target

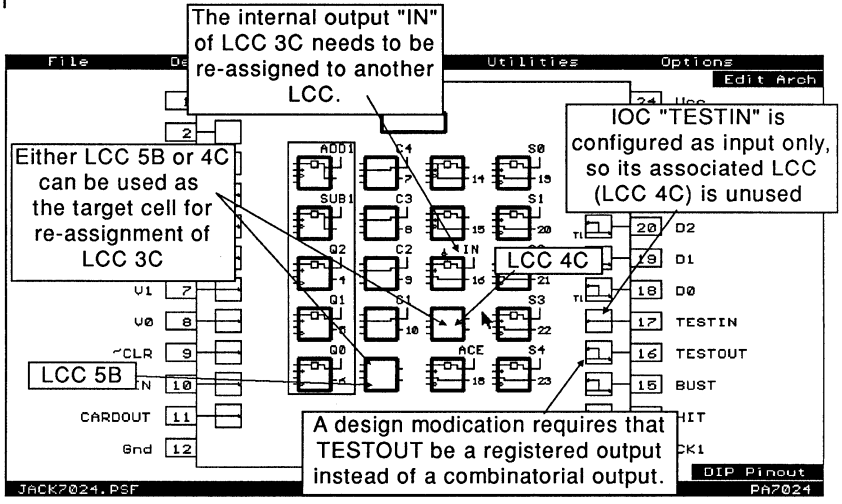


Figure 4-8, A typical example for re-assignning the LCC

cells will be the newly labeled LCC 4C and the IOC "TESTOUT".

4) Select the "LCC Re-Assign" command and click the source and target LCC (LCC 3C and 4C respectively).

5) Re-configure all the cells (both source and target LCCs and IOCs) for their specific application requirements, i.e. IOC "TESTIN" to input only, IOC "TESTOUT" to output only, and etc.

Global ..... Toggles between the one or two global cell mode. If two global cells are used, swapping is not allowed with IOCs that are located on the left and right sides of the device, or with LCCs which are associated with IOCs that are located on the left and right sides of the device. This feature allows the device to be separated into two parts with each part containing its own high speed clock. Please refer to the ICT data book for more information on the benefits of the one and two global cell modes.

## 4.5 Design Operation - Pin Block Diagram Screen

The default function for the pin block diagram screen is the Edit Architecture mode (Edit Arch). This mode is automatically set when the PLACE software is initially entered. It allows selection of the Logic Control Cells (LCCs), I/O Cells (IOCs), Input Cells (INCs) or Global Cells (GBCs) for controlling cell configurations.

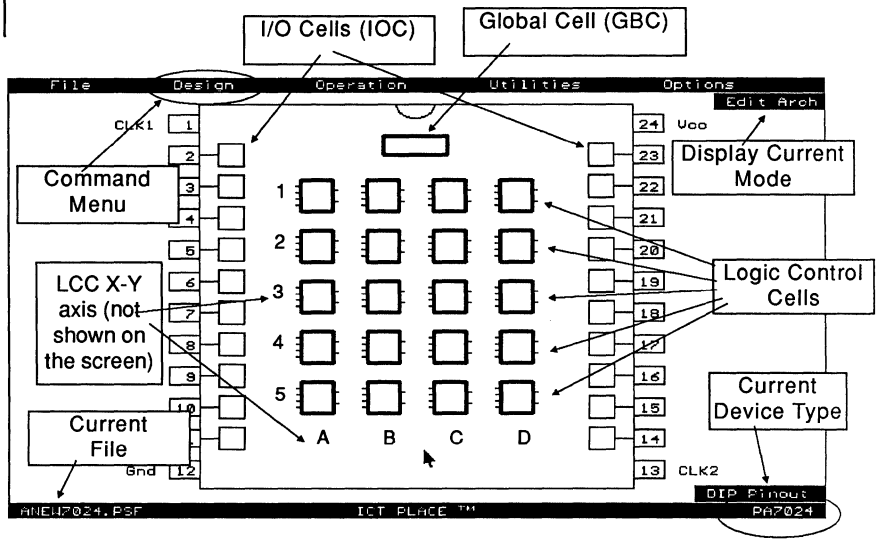


Figure 4-9, Pin Block Diagram of the PA7024

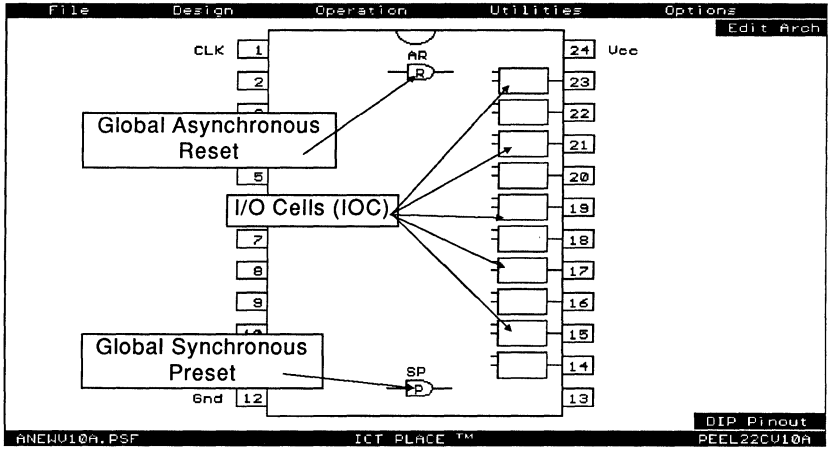


Figure 4-10, Pin Block Diagram of the PEEL22CV10A

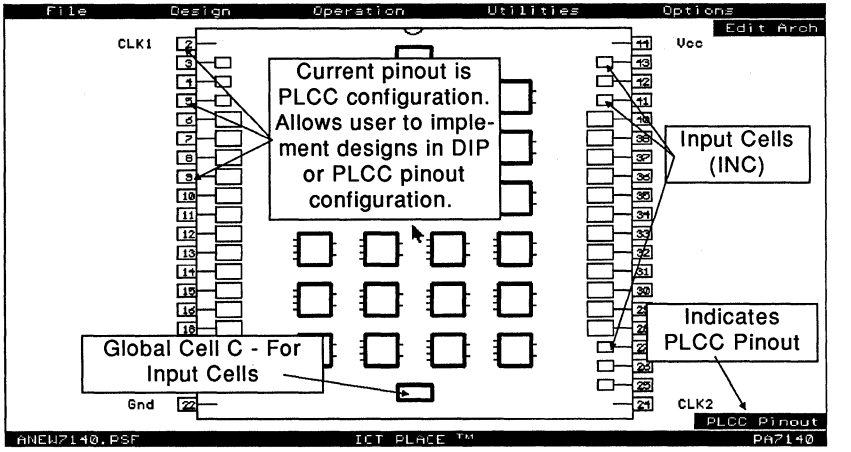


Figure 4-11, Pin Block Diagram of the PA7140

The PA7140 pin block diagram shown in Figure 4-11 illustrates the PLCC pinout configuration. For the PA7140 device, the PLCC pinout is the default configuration because this device is available in the PLCC package only. As for devices with availability in both the DIP and PLCC packages, the DIP (default configuration) or PLCC pinout configuration can be set in the "Options" menu. Refer to section 4-13 for more information on the "Options" menu.

## 4.6 Design Operation - LCC and IOC Screen

If a Logic Control Cell (LCC) or I/O Cell (IOC) is selected from the pin block diagram screen, the screen zooms into the selected cell for a close-up view of the cell configurations (Figure 4-11). Note that both the LCC and its currently connected IOC are displayed. In this screen, selections can be accomplished by moving the mouse cursor to the "selectors" such as the registers "rectangle", polarity "bubble", OR gates, or the "Smile Face" selectors. Except for the OR gate, all of the above selectors are highlighted when selected and are used for controlling the cell configurations.

Selecting any of the four OR gates will display its associated equation. Move the cursor inside the equation window and click to enter text editor. Click-R to return from editor, to complete the selected mode or function, or to return to the block diagram screen.

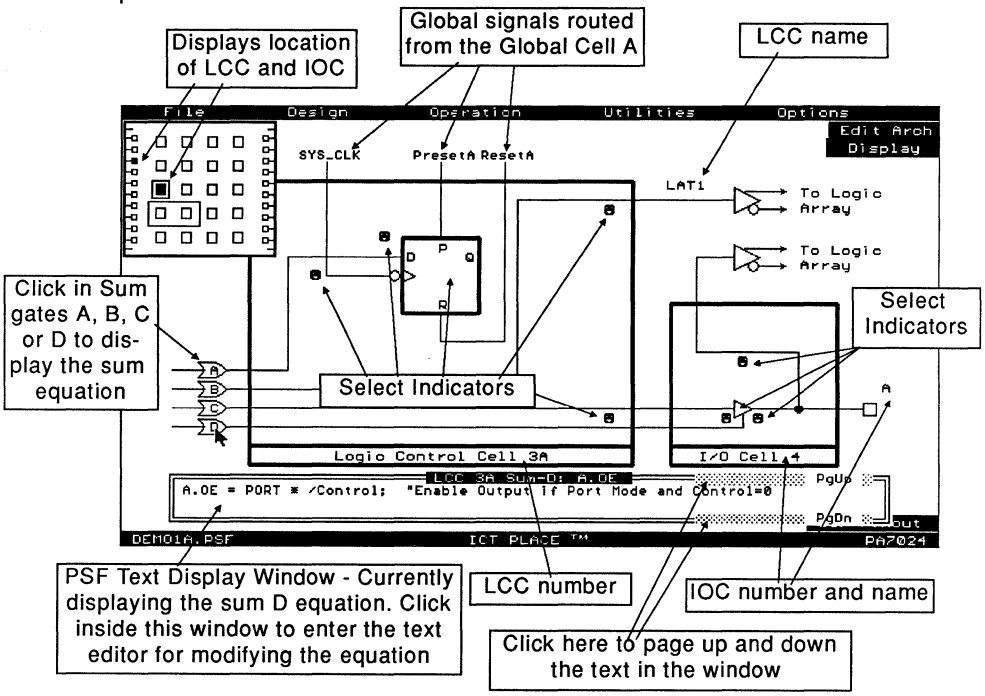


Figure 4-12, LCC and IOC screen of the PA7024

## Select Indicators in PEEL Arrays (PA7024, PA7140 and PA7128)

Below are the descriptions of the "select indicators" found in all PEEL Arrays. Unless specified otherwise, all "select indicators" are applicable for all the PEEL Array devices.

### Clk (Clock) Select

| | |
|---|---|
| **/Global** | Inverted clock signal from the Global Cell A or B. If the two global cell mode is used, then LCCs connected to IOCs on the left and right sides of the pin block diagram are controlled by Global Cells A and B respectively. For one global cell mode, all global signals are routed from Global Cell A. |
| **Global** | **Default configuration.** Non-inverted clock signal from the Global Cell A or B. |
| **Sum-C** | Clock signal from the Sum-C gate. The Reset signal for the LCC register will automatically be routed from the Global Cell A or B if it was originally connected to the Sum-C gate. |
| **Sum-D** | Clock signal from the Sum-D gate. If the IOC connected to the LCC is an I/O type, then the output will be disabled. If the IOC is an output type, then it will remain as an output type with only combinatorial feedback from the pin. |

### RT (Register Type) Control

| | |
|---|---|
| **Off** | **Default configuration.** Sets the dynamic register control to Off. This means that any signal on the RT line (RTA or RTB equation in the PSF file) will not implement a dynamic register change. |
| **On** | Sets the dynamic register control to On. A TRUE logic on the RTA or RTB equation (in the PSF file) changes the type of register in the LCC during normal operation. For instance, if RT is "On" and Register Type is "D -> T", then the D-type register will be changed to a T-type register when the logic on the RTA equation is TRUE. For the one global cell mode, the RTA equation controls the RT signals in all LCCs. For the two global cell mode, the RTA and RTB equations control the RT signals of the LCCs which are connected to IOCs on the left and right sides of the pin block diagram respectively. |

### Register Type

If RT is Off:

| | |
|---|---|
| **D** | **Default configuration.** D-type register. Reset and preset of the register can be locally (through the sum B or C gate) or globally (ResetA or PresetA equation) controlled. |
| **T** | T-type register. Reset and preset of the register can be locally (through the sum B or C gate) or globally (ResetA or PresetA equation) controlled. |
| **JK** | JK register. Sum-A for the J-input, and Sum-B for the K-input. Reset can be controlled locally or globally, but the preset will automatically be set to global preset. |

IF RT is On:

| | |
|---|---|
| **D -> T** | **Default configuration.** D-type register when the RT signal is FALSE, and T-type register when it is TRUE. Reset and preset can be locally or globally controlled. |
| **D -> JK** | D-type register when the RT signal is FALSE, and JK-type register when it is TRUE. For the JK-type register, Sum-A is used for the J-input, and Sum-B for the K-input. Reset can be controlled locally or globally, but the preset will automatically be set to global preset. |
| **T -> D** | T-type register when the RT signal is FALSE, and D-type register when it is TRUE. Reset and preset can be locally or globally controlled. |
| **JK -> D** | JK-type register when the RT signal is FALSE, and D-type register when it is TRUE. For the JK-type register, Sum-A is used for the J-input, and Sum-B for the K-input. Reset can be controlled locally or globally, but the preset will automatically be set to global preset. |

Note that the Sum-B gate cannot be used for both K-input and preset for the register.

## Preset and Reset for the LCC Register

The output of the LCC register is set to a HIGH signal when the preset signal is TRUE. On the other hand, the output of the register goes LOW if the reset signal is TRUE. **If both the preset and reset signals are TRUE, then the preset signal takes precedence over the reset signal.**

There is no dedicated MUX for controlling the preset or reset of the LCC register. Both of these signals are indirectly controlled by the "Clk Select", "Register Type", "Buried Output" and "Ext Output" selections. **The same Sum (OR) gate allocated for any of the above configurations cannot be used for presetting or resetting the LCC register.** So, the PLACE software automatically switches the preset or reset to the global signal when the local sum gate is used.

## Buried Output (Internal Output of the LCC)

| | |
|---|---|
| **Reg-Q** | **Default configuration** Connects the output of the LCC register to the internal or buried output of the LCC. |
| **Sum-A** | Connects the Sum-A gate to the internal or buried output of the LCC. |
| **Sum-B** | Connects the Sum-B gate to the internal or buried output of the LCC. If the preset of the register is locally controlled (through Sum-B), it will automatically be set to global preset. |
| **Sum-C** | Connects the Sum-C gate to the internal or buried output of the LCC. If the reset of the register is locally controlled |

(through Sum-C), it will automatically be set to global preset.

## Ext Output (External Output of the LCC to the IOC)

| | |
|---|---|
| **Reg-Q** | **Default configuration.** Connects the output of the LCC register to the external output of the LCC. |
| **Sum-A** | Connects the Sum-A gate to the external output of the LCC. |
| **Sum-B** | Connects the Sum-B gate to the external output of the LCC. If the preset of the register is locally controlled (through Sum-B), it will automatically be set to global preset. |
| **Sum-C** | Connects the Sum-C gate to the external output of the LCC. If the reset of the register is locally controlled (through Sum-C), it will automatically be set to global preset. |

## OE (Output Enable) Select

| | |
|---|---|
| **I/O** | **Default configuration.** Sets the IOC to I/O type. Sum-D is used for the output enable control. If the LCC Clk Select is set to Sum-D, the IOC changes from the I/O to input type automatically. |
| **Input** | Sets the IOC to input type. If Sum-D is not used for the LCC clock, then it will be disabled. |
| **Output** | Sets the IOC to output type. If Sum-D is used for the LCC clock, then the Feedback Type will automatically be set to combinational. |

## Feedback Type

In the normal configuration, whether the IOC is an I/O, input or output type, this multiplexer controls the path from the pin. However in the PA7140 and PA7128 devices, the option "FB Mux" allows the path to come from the Sum-D gate.

| | |
|---|---|
| **Com** | **Default configuration.** Combinatorial path from the pin or Sum-D. |
| **Reg** | Registered path from the pin or Sum-D. The clock for the register can be directly from the CLK1 or CLK2 pin, or PCLK product term. |
| **Lat** | Latched path from the pin or Sum-D. The latch trigger can be directly from the CLK1 or CLK2 pin, or PCLK product term. |

## Out (Output) Polarity

| | |
|---|---|
| **Invert** | Inverts the output to the pin for active Low output. |
| **Non-Invert** | **Default configuration.** Non-inverted output for active High output. |

## FB Mux (PA7140 and PA7128 only)

| | |
|---|---|
| **Pin** | **Default configuration.** Sets the feedback path to come from the pin. |
| **Sum-D** | Sets the feedback path to come from the Sum-D gate. With this configuration, the IOC automatically becomes an output pin with no feedback from the pin. This means that the Sum-D signal will be buried. See Figure 4-13. |

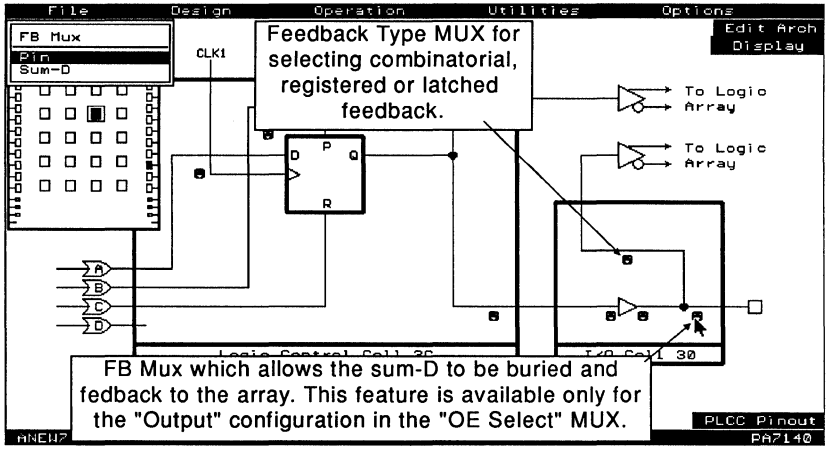


Figure 4-13, LCC and IOC screen of the PA7140

## Select Indicators in the PEEL Devices

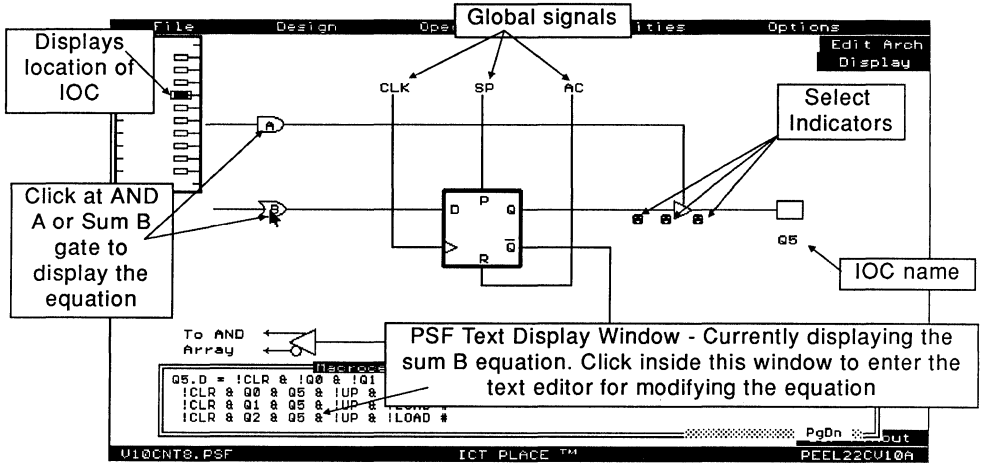


Figure 4-14, IOC screen of the PEEL22CV10A

### Output Select (All devices except PEEL173 and 273)

| | |
|---|---|
| Com | **Default configuration.** Sets the IOC to combinatorial output. In the PEEL22CV10 and 22CV10A devices, the feedback path is automatically set to come from the pin with this configuration. For other devices such as PEEL18CV8 and 22CV10Z, the feedback path is controlled by the "Feedback Type" MUX. |

| | |
|---|---|
| Reg | Sets the IOC to registered output. In the PEEL22CV10 and 22CV10A devices, the feedback path is automatically set to come from the $\overline{Q}$ of the register with this configuration. The register is triggered on the rising-edge of the clock. |

### OE (Output Enable) Select

| | |
|---|---|
| I/O | **Default configuration.** Sets the IOC to I/O type. Depending on the device, a sum or product term controls the output enable term. |
| Output Enabled | Enables the output in the IOC. |
| Output Disabled | Disables the output in the IOC. |

### Out (Output) Polarity

| | |
|---|---|
| Invert | **Default configuration.** Inverts the output to get an active Low output. |
| Non-invert | Buffers the active High output. |

### Feedback Select (18CV8, 20CG10, 22CV10Z and 22CV10A+)

| | |
|---|---|
| Pin | Feedback path from the pin. |
| Reg | Feedback path from the Q (PEEL18CV8 only) or $\overline{Q}$ (all other devices) of the register. |
| Or | Feedback from the OR gate, i.e. prior to the register and output buffer. |

## Global Asynchronous Reset and Synchronous Preset in PEEL Devices (except PEEL173 and 273)

In all registered PEEL devices, the IOC (or macro cell) register can be reset or preset using an internal reset or preset product term. The PLACE software automatically assigns node numbers for both product terms.

When the reset product term is TRUE, the output of the register in the IOC (or Macrocell) is set to a LOW signal asynchronously. **For 20-pin devices, the asynchronous reset node number is 21, and for 24-pin devices the node number is 25.**

When the preset product term is TRUE, the output of the register in the IOC changes to a HIGH signal (synchronously) with the rising-edge of the clock signal. **The node number for the preset product term is 22 and 26 for the 20 and 24-pin devices respectively.**

**When both the reset and preset signals are TRUE, then the reset signal takes precedence over the preset signal.**

# 4.7 Design Operation - Input Cell (INC) for PA7140 and PA7128

In addition to the IOCs and LCCs, the PA7140 and PA7128 have Input Cells (INCs). Each INC allows the input to be configured as combinational, registered or latched input (Figure 4-15).

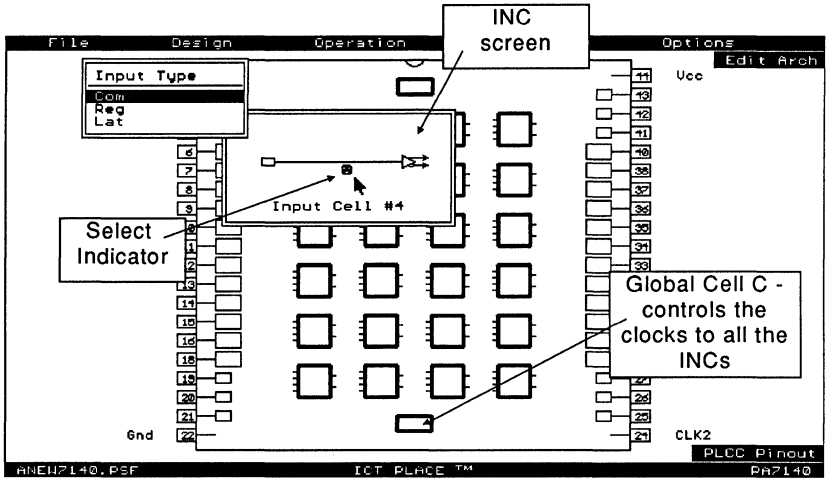


Figure 4-15, INC screen of the PA7140

## Input Type

| | |
|---|---|
| Com | **Default configuration.** Sets the input to be combinational. |
| Reg | Sets the input to be registered. The clock for the register is controlled by the Global Cell C. |
| Lat | Sets the input to be latched. The trigger for the latch is controlled by the Global Cell C. |

# 4.8 Design Operation - Global Cell (GBC) for PEEL Arrays

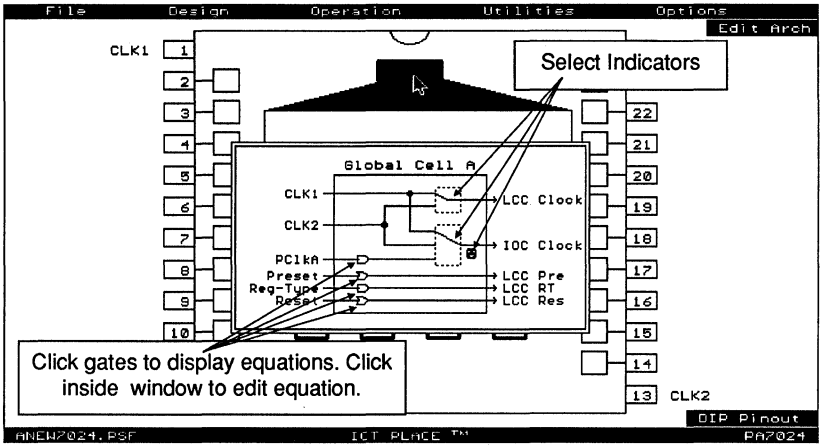


Figure 4-16, Global Cell A screen of the PA7024

## Global Cells A and B

In PEEL Arrays, the Global Cells (GBCs) A and B which are located at the top of the pin block diagram are used to control the global signals for the LCC and IOC. These global signals include the clock for the LCC and IOC, and preset, reset and register type control for the LCC.

After clicking the GBC to bring the Global Cell window up for selection, click at the MUX "rectangle" to set the desired clock selection for the LCCs and IOCs. The IOC clock polarity is controlled by the "Clock Polarity" select indicator. Click at the AND or OR (Sum) gates to display the global equations for register-type, PCLK, global reset or preset. Move the cursor inside the equation window and click the mouse to enter the text editor. In the text editor , press the [Esc] key or click-R to return to the global cell window. The same procedure can be used in the one or two global cell mode.

**In the one global cell mode, the Global Cell A controls the global signals to all the LCCs and IOCs in the device (Global Cell B is ignored). In the two global cell mode, Global Cell A controls the global signals to the LCCs and its associated IOCs that are located on the left side of the pin block diagram. Global Cell B controls the global signals to the**

**remaining LCCs and IOCs which are located on the right side of the pin block diagram.**

### Global Signals

| | |
|---|---|
| **LCC Clock** | This signal clocks the register in the LCCs. The signal comes from one of the two dedicated clock pins, CLK1 or CLK2. |
| **IOC Clock** | This signal clocks the register in the IOCs. In addition to the two dedicated clock pins CLK1 and CLK2, the signal can come from a product term PCLKA (GBC A) or PCLKB (GBC B). The select indicator "Clock Polarity" allows the IOC clock polarity to be changed. The default configuration is "Pos" which means that the IOC register or latch is triggered on the rising-edge or HIGH signal. If the configuration is set to "Neg", then the register or latch is triggered on the falling-edge or LOW signal. |
| **LCC Pre** | This sum (OR) term is the global preset for the LCC register. The LCC register is preset to a HIGH signal when this sum term is TRUE. **This term takes precedence over the reset term for the LCC register.** |
| **LCC RT** | This product term is the global register-type change for the LCC. Each LCC has the option ("RT Control") of enabling the dynamic register-type change when this term is TRUE. |
| **LCC Res** | This sum (OR) term is the global reset for the LCC register. The LCC register is reset to a LOW signal when this sum term is TRUE. |

## Global Cell C (PA7140 and PA7128 only)

In addition to Global Cells A and B, the PA7140 and PA7128 have Global Cell C. This cell which is located at the bottom of the pin block diagram controls the global clock signal for the Input Cells (INCs).

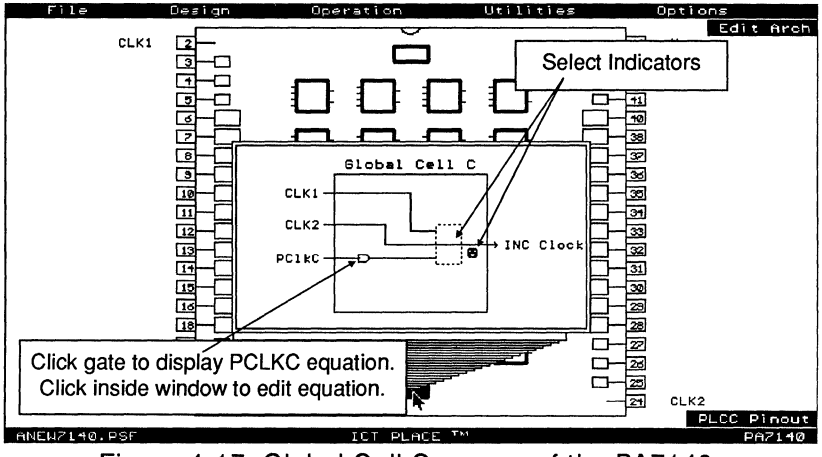


Figure 4-17, Global Cell C screen of the PA7140

## 4.9 Design Operation - Entering Equations

One of the primary methods of entering the design equations is via the "Edit Eqn" mode which was discussed in section 4.4. Figures 4-18 and 4-19 shows the "Edit Eqn" mode for the PA7024 and PEEL22CV10A devices respectively.

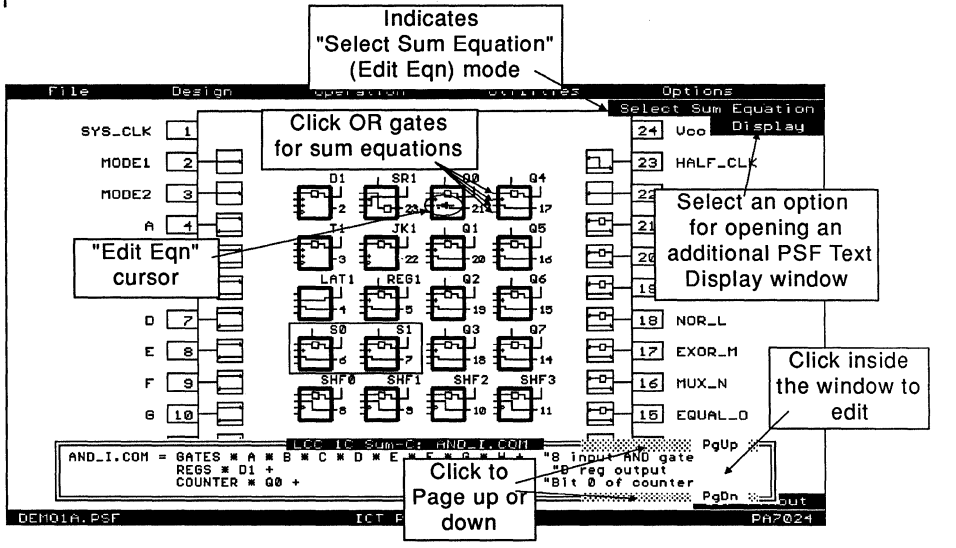


Figure 4-18, "Edit Eqn" mode of the PA7024

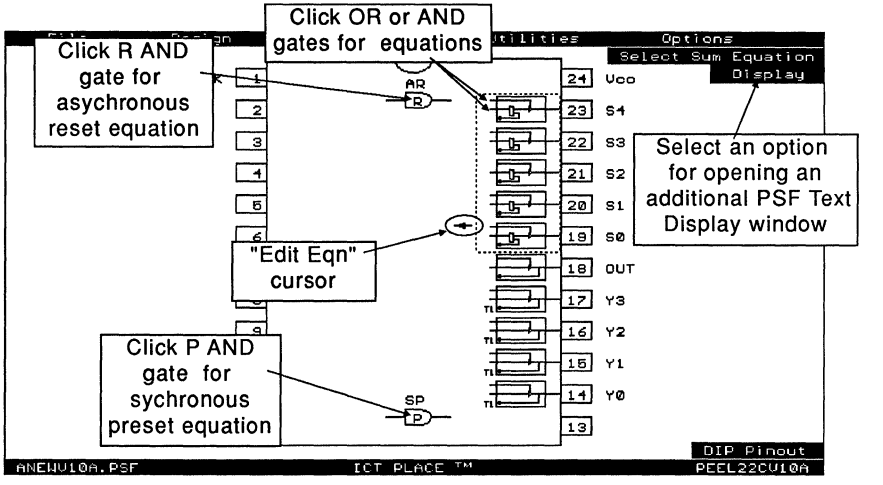


Figure 4-19, "Edit Eqn" mode of the PEEL22CV10A

In addition to the "Edit Eqn" mode, equations can also be edited via the LCC and IOC screen (or just IOC screen for the PEEL devices). Refer to Figures 4-20 and 4-21.

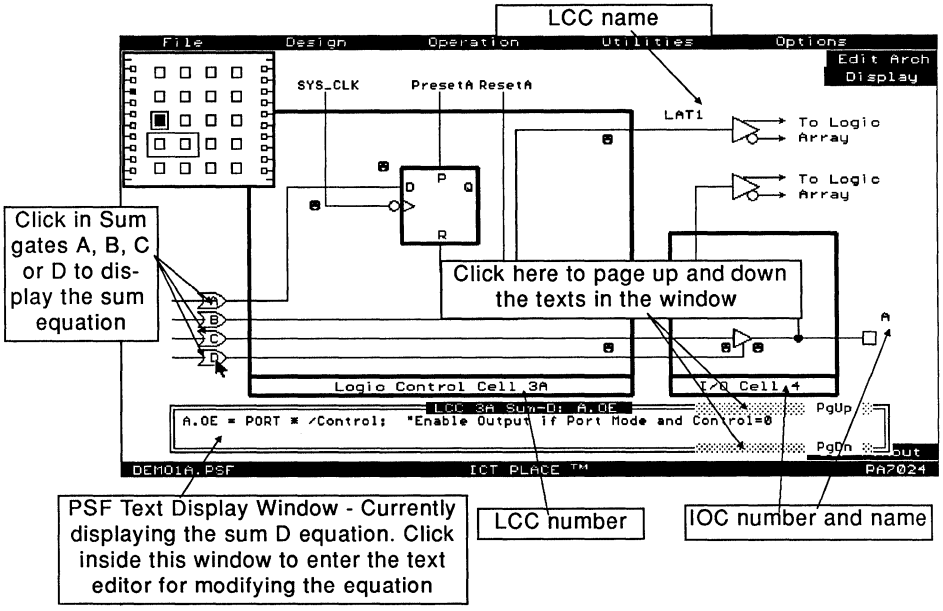


Figure 4-20, Editing equations in the LCC and IOC screen of the PA7024

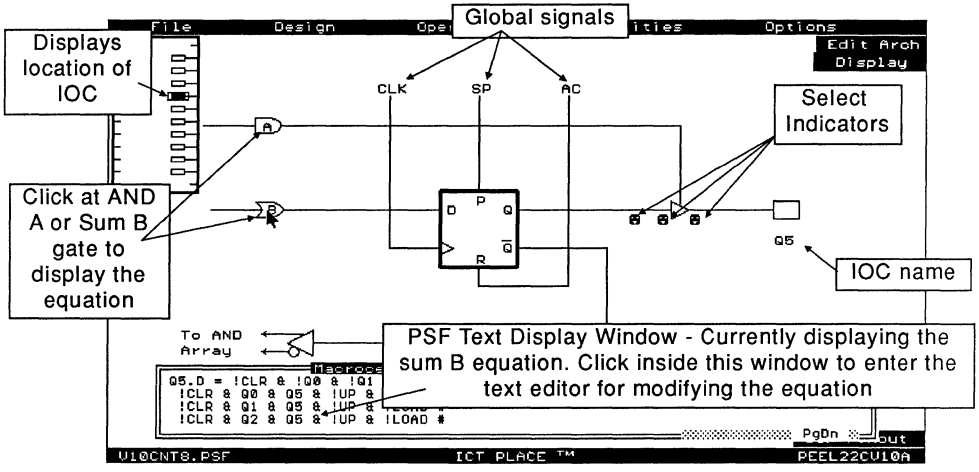


Figure 4-21, Editing equations in the IOC screen of the PEEL22CV10A

For editing equations for the global signals in the PEEL Arrays, please refer to section 4.8 on "Global Cells for PEEL Arrays".

After the cell (LCC or IOC) is labeled using the "Label" command in the "Design" menu window, the PLACE software automatically generates the equations. To edit or modify these equations, first, click at the desired OR (sum) or AND (product) gate to bring the equations out in PSF Text Display window (section 4.12). Then, click inside the window to enter the text editor. When you are done editing the equations, press the [Esc] key or click-R to return to the previous screen. Whether the device is a PA7024, PEEL22CV10A or any other device, the procedure for entering the design equations remains the same.

## 4.10 Design Operation - State Diagram Designs

An alternate method of describing a logic design is the state diagram design implementation. In this section, the procedure to implement the state diagram designs is discussed. The syntax for these state diagram designs are discussed in detail in chapter 5 on "PLACE Design Language".

The first step in the state diagram design is to label the cells to be used as state variables for the state diagram. These cells will be referred to as "State Cells". Then, configure each state cell and use the "Copy" command to duplicate the configurations to other state cells. Next, select the "Allocate" command (section 4.4) in the "Design" menu window to implement the state cell assignments. Choose the "State Diagram" option in the "Design Type" window. A window pops up allowing the options of adding or erasing state diagrams (Figure 4-22).

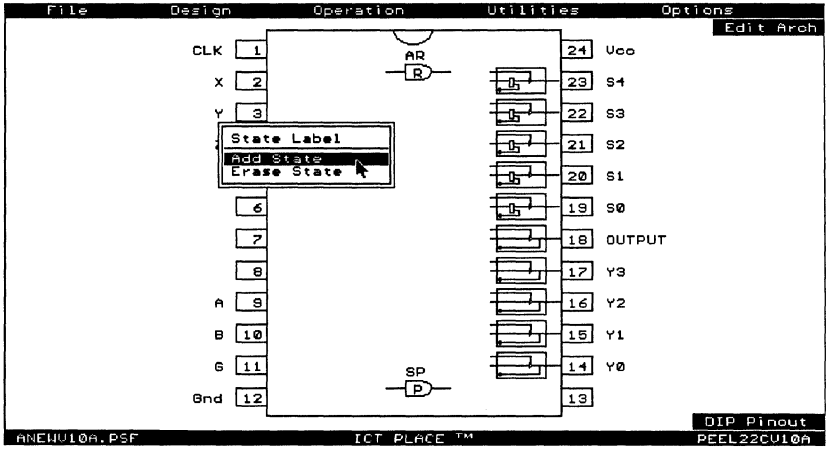


Figure 4-22, Adding a state diagram design

Note that the PEEL22CV10A device is used in the example described in this section. The procedure of implementing the state diagram design remains the same for all devices. In addition to the IOCs, LCCs in the PEEL Arrays can also be allocated as state cells.

Type in the label for the new state diagram. The syntax of the label is similar to those used for labelling pins or cells (refer to

chapter 5 on "PLACE Design Language"). The next step is to allocate the state cells as illustrated in Figure 4-23.

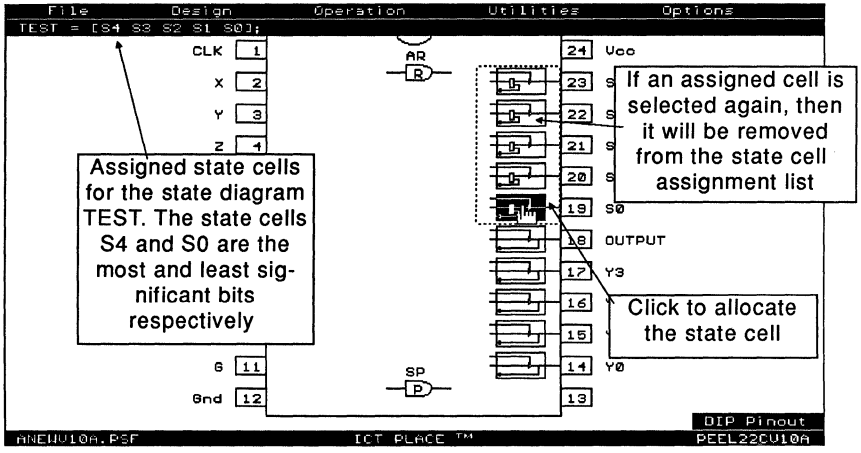


Figure 4-23, Allocating state cells for a state-diagram design

After completing the state cell assignments (by pressing the [Esc] key or click-R), a border surrounds the assigned state cells to indicate the state diagram. Additional state diagrams are differentiated by the line types in the borders.

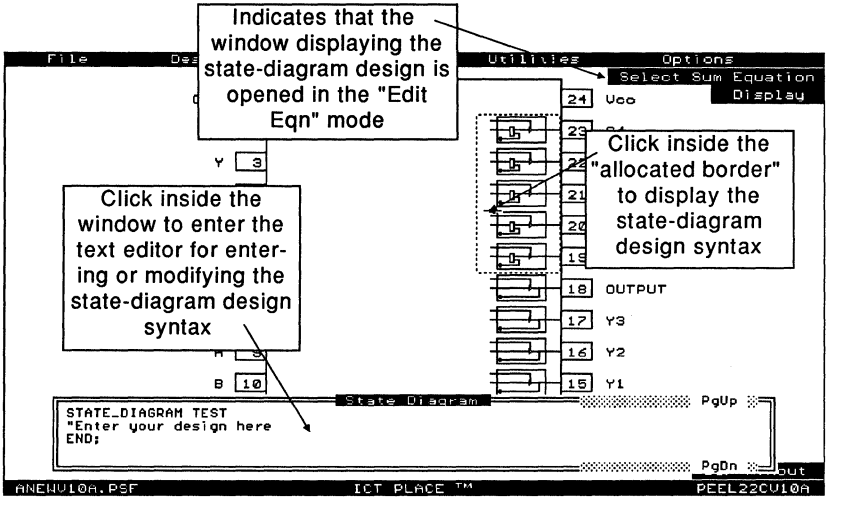


Figure 4-24, Entering design description for the state-diagram

## 4.11 Design Operation - Truth table Designs

In truth table designs, the description of the logic design is in the form of a truth table. This design method is most suitable for random combinatorial logic applications.

Like the state diagram design procedure discussed in the previous section, the truth table design begins with allocating labeled pins and cells. Figure 4-25 shows a new truth table being labeled "DECODE" at the beginning of the truth table "Allocate" command.

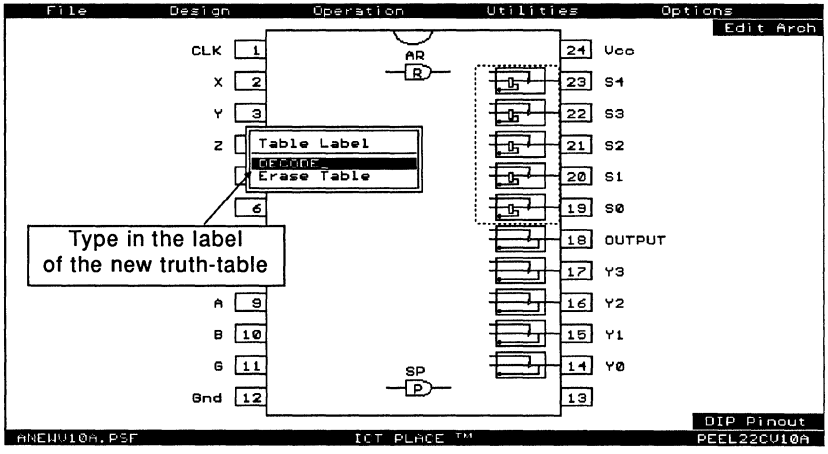


Figure 4-25, Entering the label for a new truth-table design

After typing in the label, the next step is to select the inputs of the truth table (Figure 4-26). A truth table input can be a pin, INC, IOC, or LCC. Click at the "Output" option in the pop-up window to complete the input selection and to start the output selection. Press the [Esc] key or click-R to complete the output selection.

Note that during the input or output selection process, if you click on a selected pin or cell, then it will be removed from the input or output selection list.

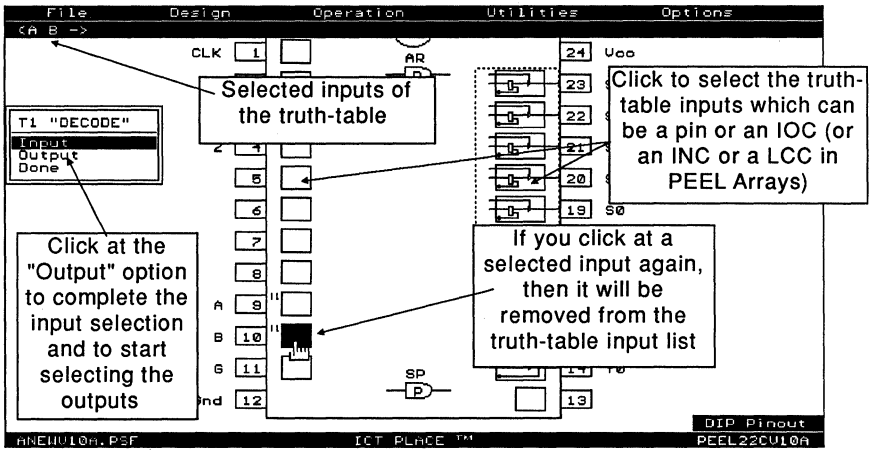


Figure 4-26, Selecting truth-table inputs

☞ Press the [Esc] key or click-R during the input or output selection process to abort or complete the "Allocate" command. A window will pop up to confirm implementing the changes made. Pressing the [Esc] key or clicking-R when the "Implement changes?" window is popped up will return you to the previous mode (input or output selection).

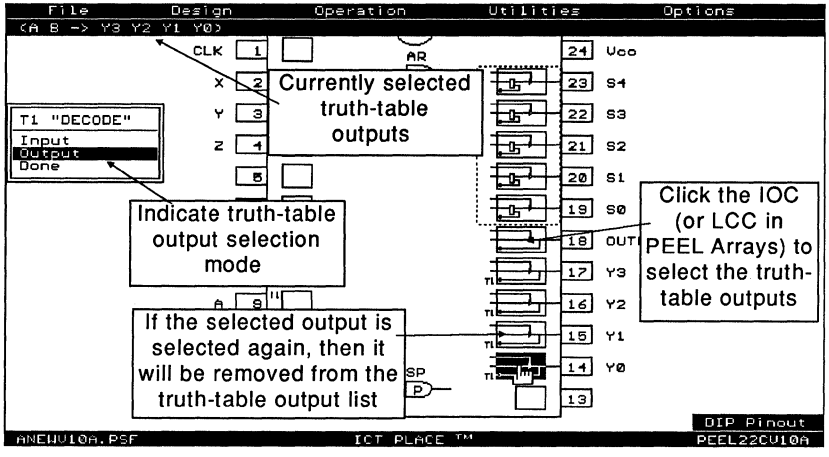


Figure 4-27, Selecting truth-table outputs

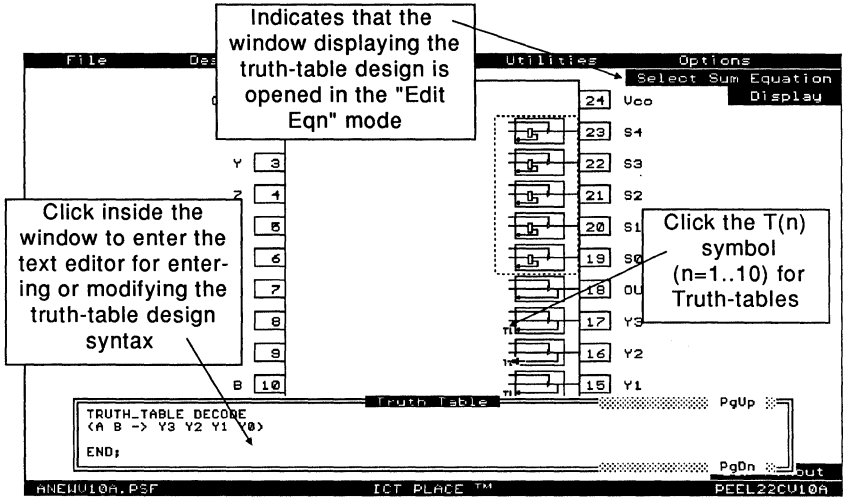


Figure 4-28, To enter the truth-table design description

☞ For more information on the syntax of the truth table design description, please refer to chapter 5 on "PLACE Design Language".

## 4.12 Design Operation - PSF Text Display Window

The PSF Text Display Windows are the windows which can be opened to display the logic description of the current design, such as equations, state diagrams, truth tables, macro definitions, and etc. The two types of windows in the PLACE software are the Equation and Option Display windows. An Equation Display window is opened by clicking the left mouse button on any SUM or AND node (gate), state diagram block and truth table marker (indicated by Tn where n = 1 to 10). This window is always located at the bottom of the screen. Refer to Figures 4-29 through 4-31. On the other hand, the Option Display window is located at the top of the screen and is opened from the "Display" menu. The "Display" menu is selectable in the "Edit Eqn" mode, LCC/IOC screen for the PEEL Arrays, and IOC screen for PEEL Devices. See Figures 4-29 and 4-30.

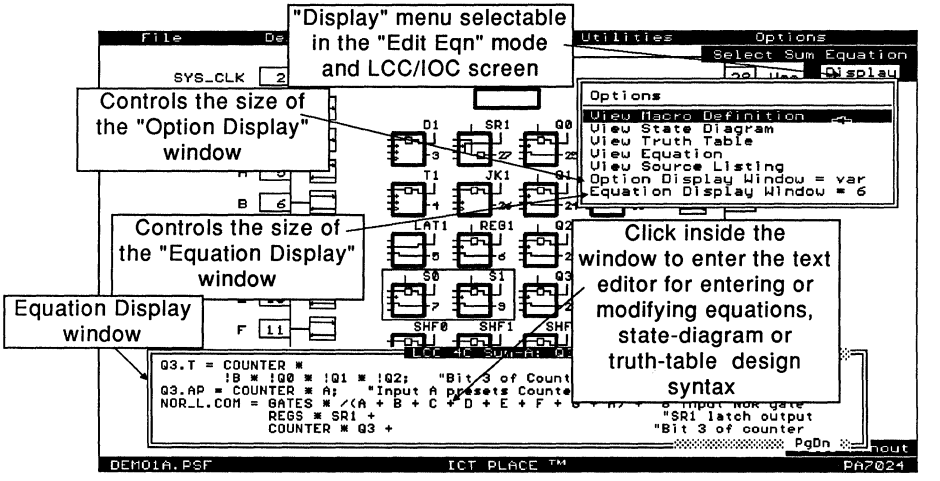


Figure 4-29, "Display" menu in "Edit Eqn" mode

### Display Options

In the "Display" menu, there are several categories of the PSF design file in which it can be selected for viewing. The list includes Macro Definition, State Diagram, Truth table, Equation and Source File. With or without the Equation Display window opened, you can open this additional window by clicking at the selected category (Figure 4-32).

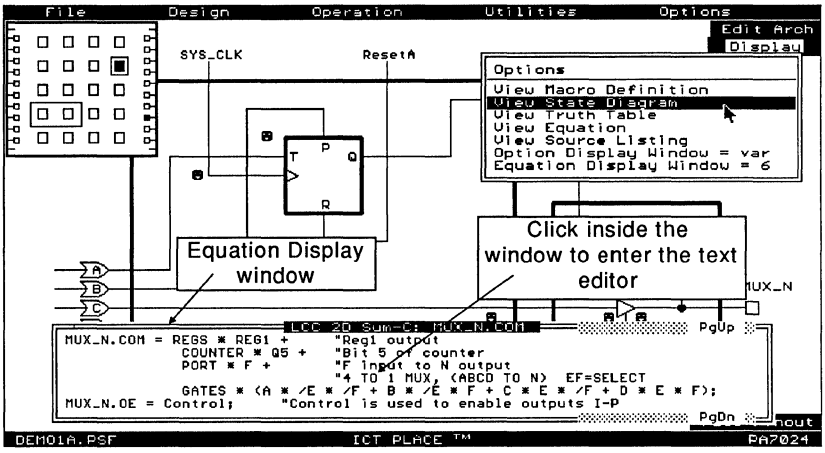


Figure 4-30, "Display" menu in the LCC/IOC screen

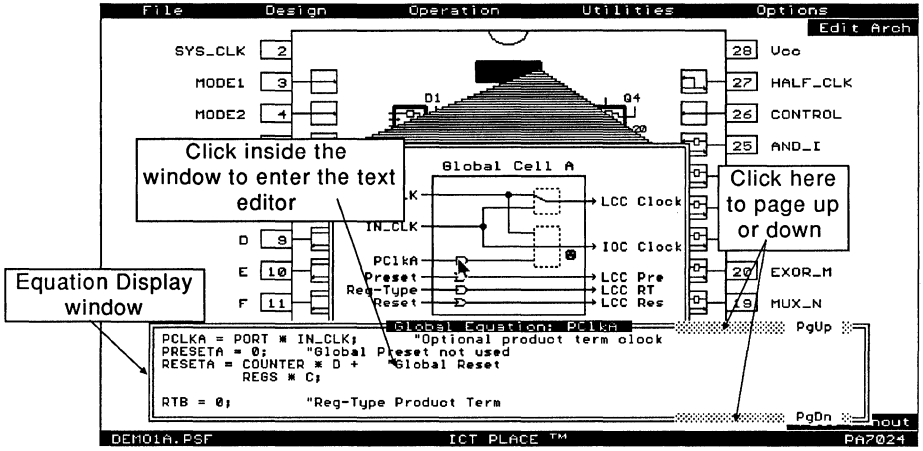


Figure 4-31, Equation Display window of the Global Cell A

☞ If the "Equation" or "Source File" option is selected, the window opens by displaying the most recently displayed page. This means that if you have previously opened the "Equation" or "Source File" window and have paged up or down, then the next time you select the same option the previous page will be displayed.

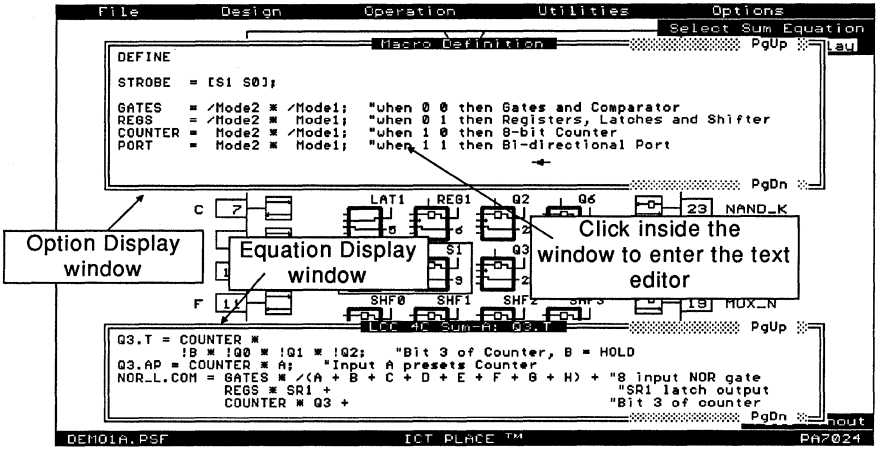


Figure 4-32, Both Equation and Option Display windows opened

## Sizing the Display Windows

There are two ways which you can size the display windows:

- The first method is by pressing the Up and Down cursor keys followed by the [ENTER] key when the window is displayed. The first cursor key pressed enters the sizing mode by outlining the current window. Each subsequent cursor key moves the window border up or down. Then, press the [ENTER] key to accept the selected size. The maximum number of lines for each window is 19.

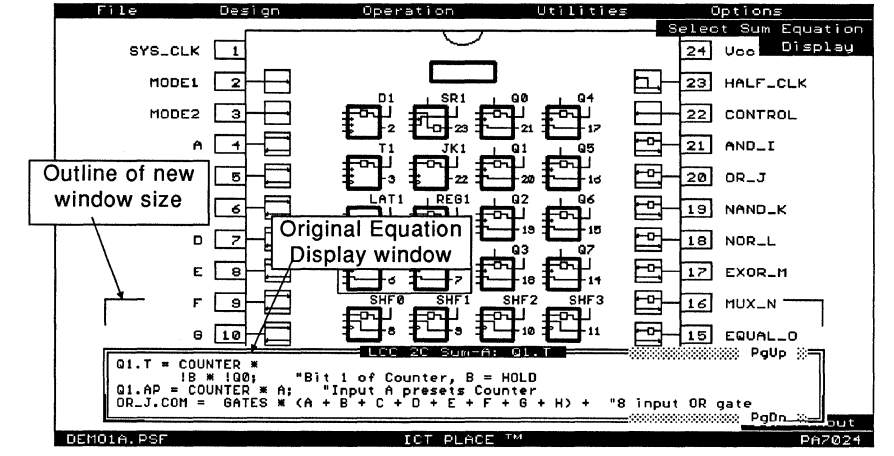


Figure 4-33, Sizing the Equation Display window

- The second method is to use the last two options in the "Display" menu (Figure 4-29). Click at either option to advance the number of lines for the window. This number will be used the next time the window is opened. In addition, the selection "var" ("variable") is available for both these optionsc. This selection (illustrated by "Option Display Window = var" or "Equation Display Window = var") allows the size of the window to be dependent on the type of design syntax selected. The criteria for setting the "var" window size are:
  - **Equations (Equation Display Window only):** A set of equation will be displayed. This equation starts from the selected SUM or AND gate label (e.g. Q1.D) and ends with any of the following characters (in prioritized order): ";", "=", "TEST_VECTORS" or ASCII# 26 (End-of-File) character.
  - **State Diagrams:** A state diagram design group which begins and ends with the keywords "STATE_DIAGRAM *statename*" and "END;" respectively.
  - **Truth Tables:** A truth table design group which begins and ends with the keywords "TRUTH_TABLE" and "END;" respectively.
  - **Macro Definitions:** The displayed text will succeed the keyword "DEFINE" but precede "STATE_DIAGRAM *statename*", "TRUTH_TABLE" or "EQUATIONS".

For the "Equations" and "Source File" options in the Options menu, the "var" selection sets the window size to 19 lines (maximum number).

## Paging Up and Down

The contents of the window can be paged up and down by pressing the PgUp and PgDn keys respectively. It can also be accomplished by clicking at the PgUp and PgDn markers in the upper and lower right corner of the window (Figure 4-30).

## Entering the PLACE Text Editor via the Display Window

Clicking the left button of the mouse within the Equation or Option Display window opens the PLACE text editor for entering or modifying the design syntax. In addition, the PLACE text editor highlights the selected block and moves the text cursor to the top of the block. The block that is highlighted depends on which Display Window the text editor was opened from. If the editor was opened via the Equation Display Window, then the equation, state diagram or truth table block will be highlighted depending on which design type was selected. If the Option Display Window was used instead, then the block displayed on the window will be highlighted in the text editor. To return to the previous screen, press the ESC key.

# 4.13 Design Operation - Options Menu

Set Pinout to DIP/PLCC ..... Allows the pin numbers in the pin block diagram and LCC/IOC screen to show the pinout of DIP or PLCC package type. Figures 4-34 and 4-35 show the pinouts for DIP and PLCC packages respectively. **The default is the DIP pinout for all devices with the exception for the PA7140 device which has PLCC pinout configuration only.** The PLCC pinout configuration is available to all devices except the PEEL173 and PEEL273 devices.

PLCC Configuration ..... Displays the design in the actual PLCC package form (Figure 4-36). Press the [Esc] key or click-R to return to the previous screen. This command is applicable to all devices except PEEL173 and PEEL273.

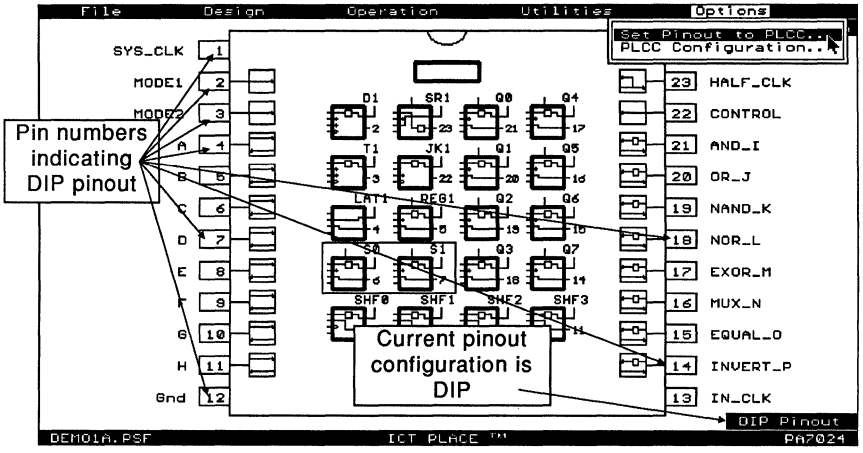


Figure 4-34, "Options" menu and DIP pinout for the PA7024

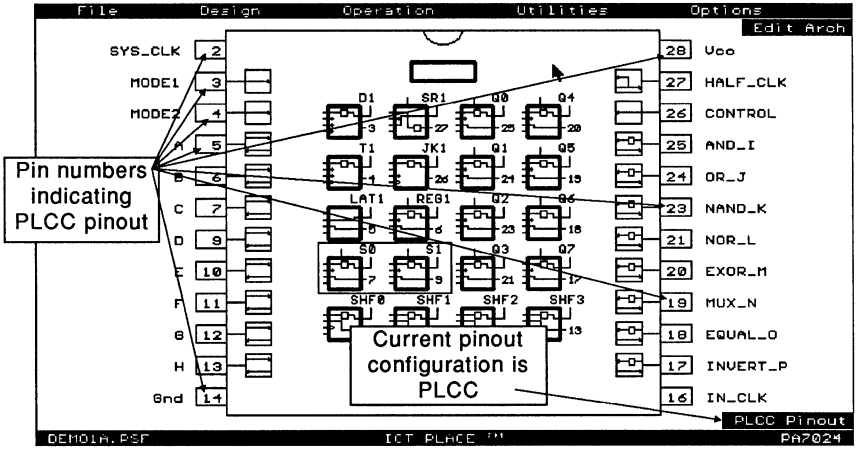


Figure 4-35, PLCC pinout for the PA7024

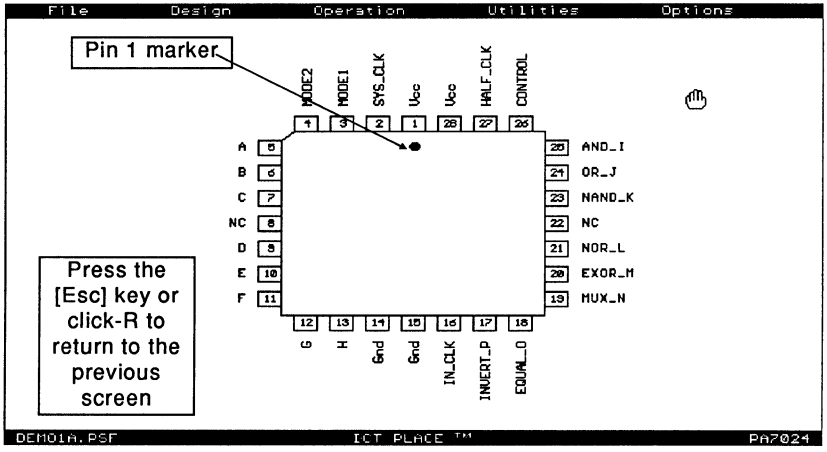


Figure 4-36, PLCC package configuration for the PA7024

# 4.14 Compile Operation - Main Screen

There are three windows in the main screen of the Compile Operation (Figure 4-37). Each of these windows provides a specific function in regards to the compilation process of the PLACE Source File (PSF).

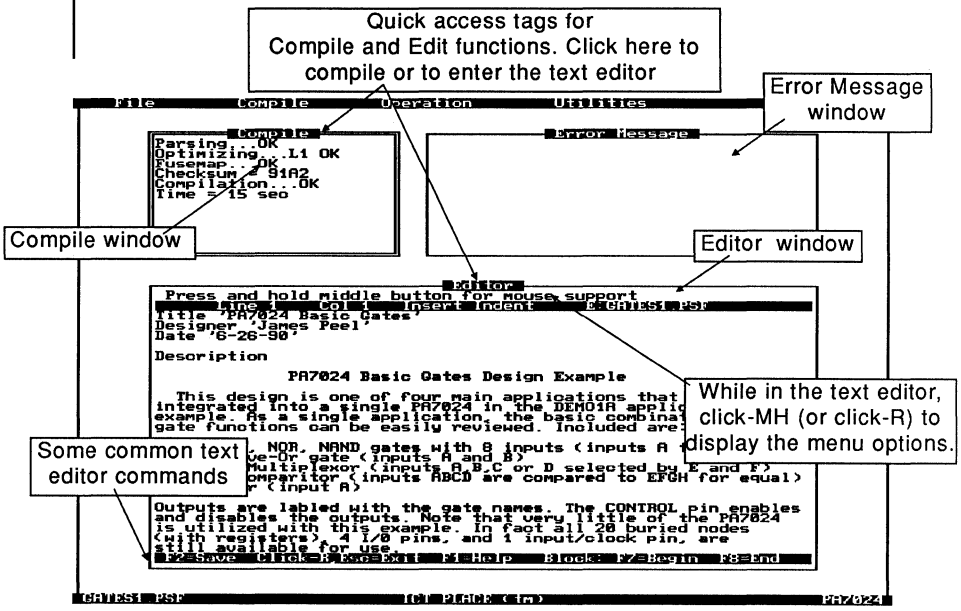


Figure 4-37, Compile Operation screen

Compile ..... This window displays the information regarding the status of the compilation. The compilation of a PSF file is a three step process: Parsing; Optimization; and Fuse-mapping.

**Parsing** - Checks the syntax of the PSF file and displays the error in the Error Message window.
**Optimization** - Implements logic transformation (complex equations into sum-of-product form conversion) and reduction to the parsed PSF file, and outputs the results to a file with extension ".RED". The RED file is in the PSF format, hence it can be read into the Design Operation for analysis of the reduced equations. After optimization is completed, the reduction level implemented is displayed. For instance in Figure 4-37, the "L1" term in "Optimizing ...L1 OK" indicates that the reduction level L1

was used for the GATES1.PSF design, and the reduction process was successful (as indicated by OK).

**Fuse-mapping** - This is the final step of the compilation process. After successful optimizations, the reduced equations are mapped into the device by outputing a JEDEC file. In addition, the fuse-mapper outputs a ".MAP" file which contains the information on how each equation is mapped in the JEDEC file.

Once the compilation is completed and successful, the check sum of the JEDEC file and compilation time will be displayed.

Error Message .. This window displays any error encountered during the compilation process. Figure 4-38 shows an example of a syntax error in which an unknown signal "MØDE2" was encountered in the macro definition (the correct signal is "Mode2"). Once an error is encountered the compilation is aborted, and the text editor is opened automatically to allow the highlighted error to be investigated or analyzed. Note that the highlighted line sometimes does not contain the error. This may be due to an incorrect format for comments in the previous lines. Please refer to chapter 5 for more information on the Comment format.

Editor ..... The Editor window allows the text editor to be opened for design edits or modifications. If a syntax error is found during the compiling process, the editor opens and highlights the error line automatically. A full screen editor is available via the "Utilities" menu.

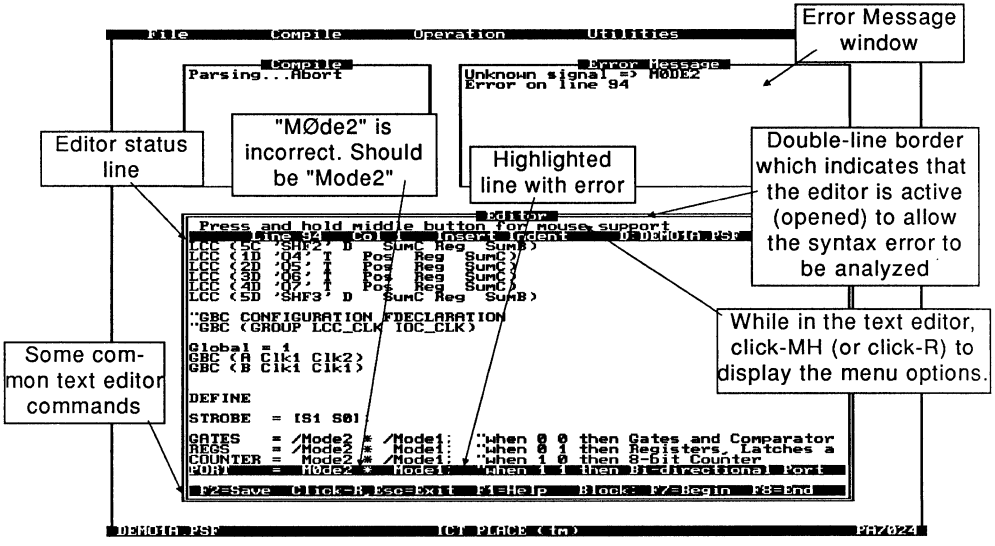


Figure 4-38, Encountering a compilation syntax error

# 4.15 Compiler Operation - Compile Menu

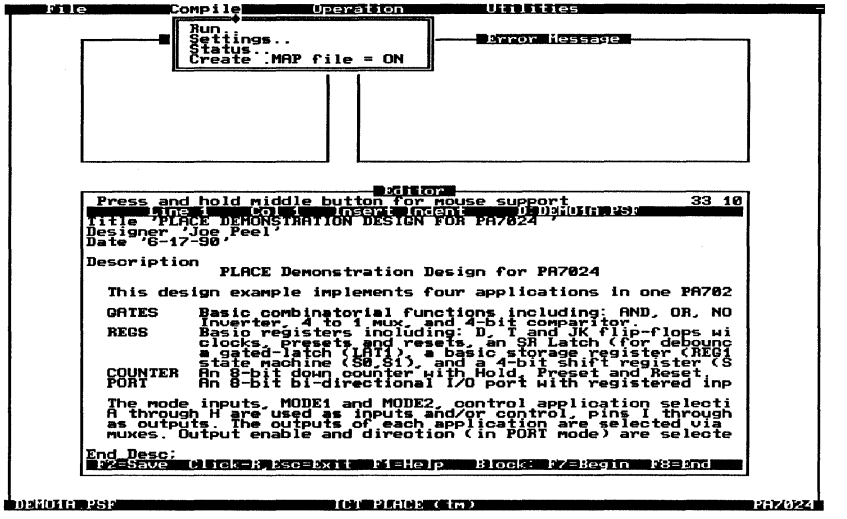


Figure 4-39, Compile menu

Run ..... Compiles currently selected PSF design file. If the compilation process is successful, then a JEDEC ".JED" file will be created. If a compilation error occurs, an error message will be displayed in the Error Message window. In addition, the editor will be opened and the line containing the error highlighted automatically. You can then make the edits here or go back to the Design operation to correct the source file. Please refer back to section 4.14 for more information on the compilation process. **Note: The compiler can be executed by clicking at the "Compile" window heading.**

Settings ..... Allows the selection of logic reduction level and product term utilization as listed in Table 4-3.

- **The default option for the reduction level selection is "Auto 1-5".** The "Auto" reduction levels refer to the automatic increments of the reduction levels. For instance, the "Auto 1-5" means that the optimization process starts with reduction level 1. If the design does not fit the device after the completion of level 1, then it proceeds to level 2. If the design still does not fit the device, it proceeds to level 3 and so on until a fit occurs. Once the design achieves a device fit, the reduction level will be displayed in the Compile window (Figure 4-37).
- There are five reduction levels, ranging from no logic reduction to group reduction with deMorganization of

outputs. The higher the level the better the utilization but the optimization time will also be longer. So when compiling a design for the first time, it is recommended to use the "Auto 1-5" option. Then, note the level needed (displayed in the Compile window) to successfully compile the design. For subsequent compilations, select the single reduction level.

- **"Utilization":** This command allows the maximum number of product terms (in percentage) used during the logic optimization process to be set. For instance in the PA7024 device, if the product utilization is set as "Utilization = 60 %", then 60% of 80 product terms (80 product terms is the maximum for the PA7024) will be used during logic optimization. Hence, this command allows you to estimate whether additional logic can be implemented into the selected device. **The default product term utilization is "Utilization = 100 %".**

| Reduction Level | Function |
|---|---|
| Level 1 | No reduction. Transforms equations to sum-of-products. |
| Level 2 | Simple reduction. Combines duplicate product terms. |
| Level 3 | Pin reduction. Optimizes terms per individual equation. |
| Level 4 | Group reduction. Optimizes terms over all equations which can be shared. |
| Level 5 | Group with output polarity inversion reduction. DeMorganizes Outputs (automatically inverts polarity) to achieve best optimization of terms. |
| Auto 1-2 | Optimizes from Level 1 to 2 until logic fits. |
| Auto 1-3 | Optimizes from Level 1 to 3 until logic fits. |
| Auto 1-4 | Optimizes from Level 1 to 4 until logic fits. |
| Auto 1-5 | Optimizes from Level 1 to 5 until logic fits. |
| Utilization | Sets the maximum product terms which can be shared to be used in the logic reduction or optimization process. The number set is in percentage. |

Table 4-3, "Settings" menu in the Compile menu window

Status ..... Displays the device utilization and use of architecture after the design is compiled.

Create .MAP file . During the fuse-mapping process, a ".MAP" file can be created in addition to the JEDEC file. This MAP file contains the detailed information regarding how each equation is mapped in the JEDEC file. **The default condition is ON.**

## 4.16 Simulate Operation - Waveform Screen

After successful compilation of a PSF design file, test-vectors may be necessary to verify the design. In the Simulate operation, these test-vectors are displayed as waveform signals (Figure 4-40). The vectors are created using the "Edit" command. Then, they are used to simulate (logically only) the function of the design by retrieving the design's logic from the JEDEC file which was created in the Compile operation. These vectors can also be appended to the JEDEC file so that they can be used to exercise the device after programming.

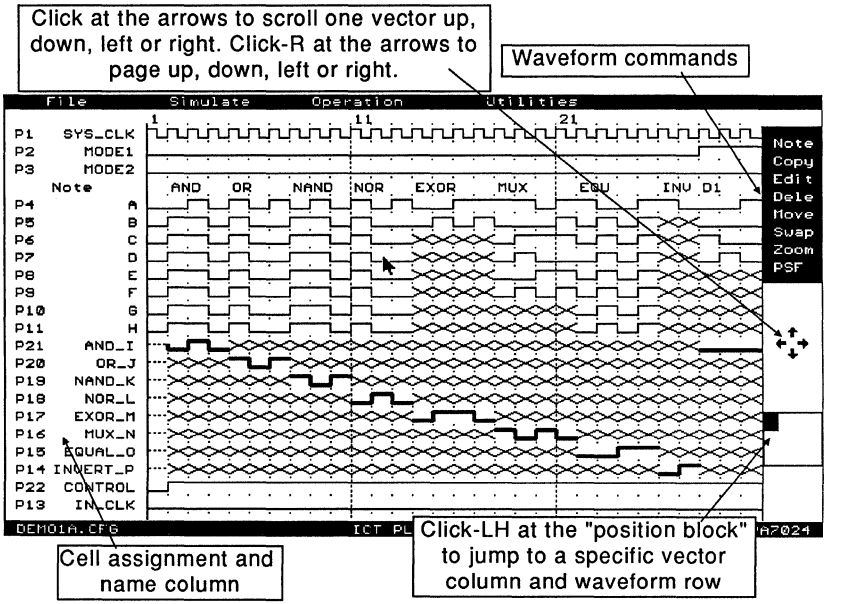


Figure 4-40, Simulate waveform screen

In the waveform display, each waveform row represents a signal from a pin or an internal node (e.g. a LCC, IOC or INC). The external pins are indicated by "P" followed by the pin number. LCC internal output is indicated by "L" with the cell assignment coordinates. The prefix for the IOC or INC node (i.e. the output of the IOC or INC register) is an "I" followed by the assigned pin number. The IOC and INC nodes are differentiated by the as-

signed pin numbers. For instance in the PA7140 device, pins 3-5, 19-21, 25-27 and 41-43 are assigned to INCs. The rest of the pins except pins 2 and 24 (CLK pins) are assigned to IOCs. For more information, please refer to the ICT data book.

Examples of the waveform pin and cell assignments, and labels found in the TC7140.PSF design file of the PA7140 (the PA7140 device has all the cells, i.e. LCCs, IOCs and INCs) are:

| | | |
|---|---|---|
| P2 | CLK | => pin 2 with label CLK |
| L3A | P2 | => LCC 3A with label P2 |
| I15 | C2 | => IOC 15 with label C2 |
| I4 | SELECT | => INC 4 with label SELECT |

## Scrolling and paging in the waveform display

As illustrated in Figure 4-40, scrolling and paging can be accomplished by clicking and clicking-R at the arrow markers located on the right side of the screen. An additional method of scrolling and paging is to use the left, right, up and down cursor keys, and the [PgUp] and [PgDn] keys respectively.

Alternately, you can click-LH (click and hold the left mouse button) at the "position block" to jump to another waveform display section. Once you have selected the location, release the left button to return to the normal screen mode.



## Functions of the waveform signals

In the Simulate operation, the graphical image of each waveform signal represents a specific function. For instance, the waveform signal image ⌜⌝_ which is represented by the test-vector C in the JEDEC file indicates a Low-High-Low input pulse. This signal functions as a clock for triggering a register on the rising or falling edge of the signal. Please refer to Tables 4-4 and 4-5 for additional information on other waveform signals.

☞ Figures 4-40 through 4-56 illustrated in this section were captured via a monochrome monitor. Refer to Table 4-5 for the functions of the waveform signals in these figures.

| Symbol | Color | Function | JEDEC Vector Symbol |
|---|---|---|---|
|  | Blue | System Clock | C |
|  | Blue | Input High | 1 |
|  | Blue | Input Low | 0 |
|  | Blue | High Voltage Preload | P |
|  | Blue | Input or Output Don't Care | X |
|  | Yellow | Output High | H |
|  | Yellow | Output Low | L |
|  | Yellow | Output High Impedance | Z |
|  | Red | Buried or Internal Signals which cannot be modified | N/A |

Table 4-4, Waveform signal symbol table for a color monitor

| Symbol | Linewidth | Function | JEDEC Vector Symbol |
|---|---|---|---|
|  | Normal | System Clock | C |
|  | Normal | Input High | 1 |
|  | Normal | Input Low | 0 |
|  | Normal | High Voltage Preload | P |
|  | Normal | Input or Output Don't Care | X |
|  | Thick | Output High | H |
|  | Thick | Output Low | L |
|  | Dotted | Output High Impedance | Z |
|  | Center | Buried or Internal Signals which cannot be modified | N/A |

Table 4-5, Waveform signal symbol table for a monochrome monitor

# 4.17 Simulate Operation - Simulate Menu

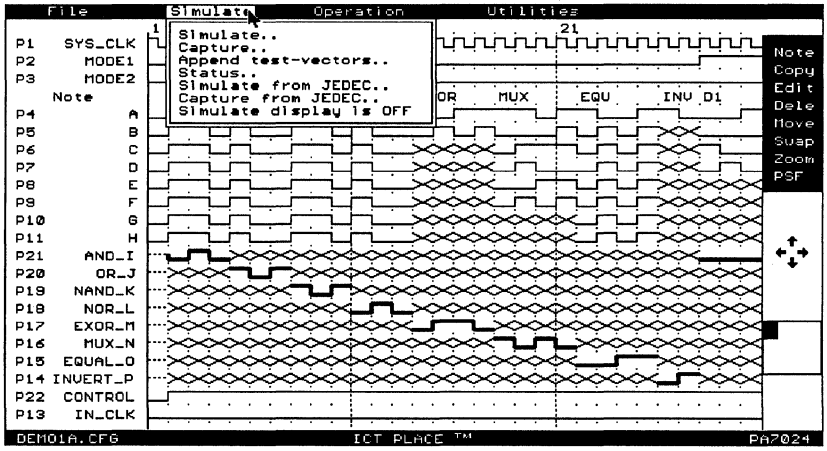


Figure 4-41, Simulate waveform screen

Simulate ..... Performs logic simulation of waveform vectors on external signals, i.e. on the "P" waveform rows only. The simulator compares the simulated signals with the current signals on the pins, and then mark the locations with signals that do not match. These marked locations are vector simulation errors (Figure 4-42 and 4-43). The special symbols used indicate the type of simulation errors (Table 4-6). On the other hand, the signals for all internal nodes are not checked but are automatically captured during logic simulation.

During simulation, the design's logic is retrieved from the JEDEC file that has the same root name. For example, the JEDEC file DEMO1A.JED will be used during the vector simulation of DEMO1A.CFG.

Capture ..... Unlike the "Simulate" command, this command "captures" the signal on all external outputs. With this command, signals on the output pins need not be generated because the simulated signals are automatically inserted by the simulator. In addition, the simulated signals are also inserted into vector locations which contain the output Low "L", output High "H" and Don't Care "X" signals. This means that if you have simulation errors on any of these vector locations, they will be replaced by the simulated signals. See Figure 4-42.

☞ Please refer to Figure 4-44 for information on the "Simulate" and "Capture" commands for asynchronous clock designs.

| Error Symbol | Function |
|---|---|
| L | Indicates that a LOW signal is simulated on the pin at the current vector location. |
| H | Indicates that a HIGH signal is simulated on the pin at the current vector location. |
| Z | Indicates that the pin is in a High Impedance condition at the current vector location. An example is the insertion of output signals ("L" or "H") on inputs. |
| C | Indicates that a signal contention condition exists at the current vector location. An example is the insertion of input signals ("0" or "1") on outputs. |
| U | Indicates that the signal at the current vector location is unstable or in an indeterminate state. An example of an application which causes this error is an oscillator. When an unstable error occurs, the simulation process is aborted and the pin number(s) reported.<br><br>Note that the PLACE Simulator will not flag an error if the unstable output has a Don't Care symbol. |

Table 4-6, Simulation error symbols for pins

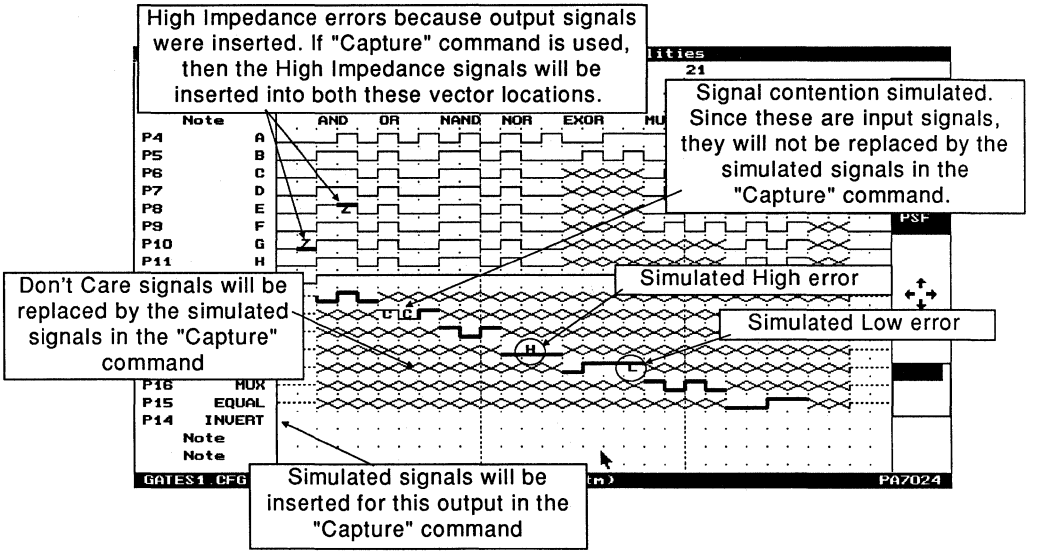


Figure 4-42, Vector simulate errors

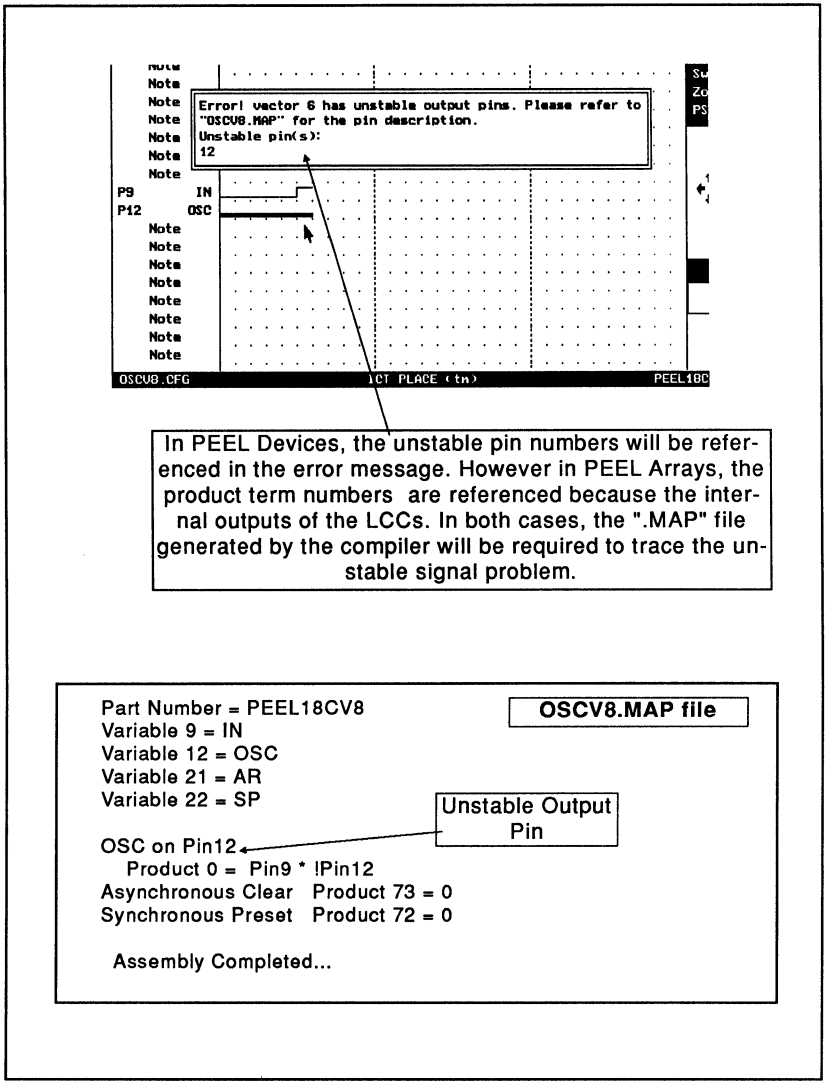


Figure 4-43, Unstable output simulation error example

## Test Vectors for Asynchronous Clock Applications

**Asynchronous clock refers to the triggerring of the LCC or IOC register via a sum or product term.** Devices with the asynchronous clock capability include PA7024, PA7140 and PA7128. If the simulated waveform vectors are appended to the JEDEC file for exercising the device, then special attention for the asynchronous clock designs is needed. This is because of possible data set-up time violations due to how the input signals are applied on the PLD programmer.

☞ For the ICT PDS-1 programmer, the input signals are applied serially starting from pin 1 after the device has been powered-up (set the Vcc pin to 5V). First, input signals "0" and "1" are applied, then preset signals "P" (this is high voltage preset which is not supported in many PEEL devices), then clock signals ("C"), and then the output pins are sensed and compared with the vectors from the JEDEC file. With this method, data set-up time violations for asynchronous clock designs are very possible, especially if the input signals "0" and "1" are used to emulate the clock signals.

There are two methods to ensure the proper test vectors for testing the asynchronous clock designs.

1. The first method is to use the dedicated clock signal ⌐⌐_ (JEDEC "C") in the sum or product term equation. Since this signal exhibits a Low-High-Low voltage level in a given vector period, the standard logic operation of the AND and OR operators may be applied, but with some modifications.

| Clock | Operator | Input | Result |
|---|---|---|---|
| C | & (AND) | 1 | C |
| C | & | 0 | 0 |
| C | # (OR) | 1 | C |
| C | # | 0 | C |

Figure 4-44, Test Vectors for asynchronous clock applications - Sum or Product term clock

By using the dedicated clock signal, the programmer applies the signal to the clock only after all input signals are applied. Note that if the result "C" is routed to an external output, then a signal contention error will be flagged.

2. The second method is to add dummy or Wait states prior to all clock edges which are generated by the "0" and "1" input signals. The advantage with this method is that the same clock signal can be routed to an external output without encountering a signal contention simulation error as in the preceding method. However, the disadvantage is that a minimum of two vectors are required to generate a clock cycle, "0" and "1" signals on successive vectors. If a Low-High-Low signal is required, then three vectors are necessary.

Figure 4-44, Test Vectors for asynchronous clock applications - Sum or Product term clock (Continued)

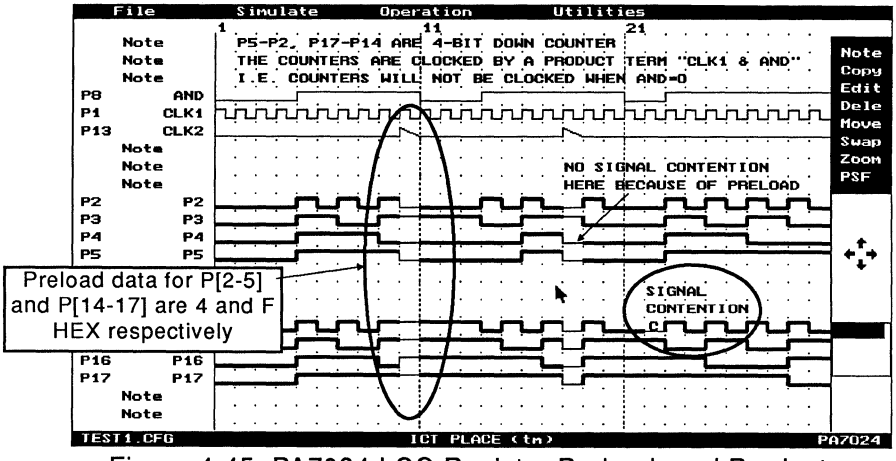


Figure 4-45, PA7024 LCC Register Preload, and Product or Sum Clock Application

**Preloading the LCC registers (in logic simulation only)**

In the Simulate operation for the PA7024, PA7140 and PA7128 devices, all the LCC registers can be preloaded with the user-specified data. Note that this feature is only a software feature and does not exist in the device physically. If the preload vectors are applied to the device on a PLD programmer, these vectors will fail.

In Figure 4-45, the PA7024 application example has two sets of registered output pins P2..P5 and P14..P17. At the preload vector column 10, the LCC registers for these outputs are preloaded with data 4 and F HEX respectively. The preload condition is activated by the waveform symbol \ (JEDEC "P") on the dedicated preload pin 13 (each device type has a specific pin dedicated for the preload function). The clock symbol ⌈⌉_ on pin 1 is not necessary because the preload symbol automatically loads the data in asynchronously.

Below is a list of the preload pins and the assigned pins for the LCC registers for the PA7024, PA7140 and PA7128 devices.

| Device | Preload Pin | Preload Data Pins | LCC Registers |
|---|---|---|---|
| PA7024 | 13 | 2 - 6 | LCC 1A - 5A |
| | | 7 - 11 | LCC 1B - 5B |
| | | 14 - 18 | LCC 1C - 5C |
| | | 19 - 23 | LCC 1D - 5D |
| PA7140 (PLCC) | 24 | 6 - 11 | LCC 1A - 6A |
| | | 12 - 16, 18 | LCC 1B - 6B |
| | | 28 - 33 | LCC 1C - 6C |
| | | 34 - 38, 40 | LCC 1D - 6D |
| PA7128 | 1 | 15 - 17 | LCC 1A - 3A |
| | | 18 - 20 | LCC 1B - 3B |
| | | 21 - 23 | LCC 1C - 3C |
| | | 24 - 27 | LCC 1D - 3D |

By adding the preload condition at the beginning of each CFG file (except for the first one), then up to 36 CFG files (CFA, CFB, .., CFZ and CF0, CF2, .., CF9) can be linked together for simulating a large PEEL Array design. With approximately 700 vectors per CFG file for a 512K system, about 25,000 "continuous" vectors can be simulated for a design.

Figure 4-46, LCC Register Preload function

Append test vectors ..... This command converts the waveform vectors into the JEDEC file test-vectors and appends them to the ".JED" file. This allows the vectors to exercise the device on a PLD programmer.

Status ..... Provides status information such as the maximum vector columns available with the current system configuration (more system RAM memory, more vector columns available), number of total vectors used, number of simulation errors, and the previous simulation time.

Simulate from JEDEC ..... With this function, the PLACE Simulate waveforms can be generated from the test vectors specified in the JEDEC file. If an ICT PDS-1 programmer is present, this function together with the "Capture" function in the "Test" menu of the Program operation allow viewing of device vector results via the waveform screen. Refer to Figure 4-47.

Capture from JEDEC ..... This command is similar to that of the "Simulate from JEDEC" command except that the output signal levels will be replaced by the simulated signal levels.

Simulate display ..... When the Simulate display is set to the ON condition, the waveform vectors are displayed during the simulation or capture process. If this command is set to the OFF condition, the waveform vectors will not be displayed during simulation. Instead, each vector will be illustrated by a "." for a vector which passes simulation, and a "*" for a failed vector.

**Using the "Simulate from JEDEC" command to display vector errors encountered on the PDS-1 programmer**

The procedure for displaying the hardware device vector results when using a PDS-1 programmer is:

1. After encountering test vector failures on the device in the Program operation, use the "Capture" command in the "Test" menu to capture all the output signal levels.
2. Select the "saveAs" command in the "File" menu to save the JEDEC file containing the captured vectors with a different file extension. It is recommend to change the last character of the file extension only so that both files will be displayed in the directory window. For instance, change the "DEMO1A.JED" to "DEMO1A.JE1".
3. Return to the Simulate operation and select the "Simulate from JEDEC" command. Enter the JEDEC file name containing the captured vectors when prompted for a file name ("DEMO1A.JE1").
4. Waveform vectors will be generated during the simulation process. Vector failures will be indicated by simulation error symbols L, H, Z, C and U which represent simulated signals. This means that the simulated signals are the correct signals for the current design.

☞ Below are additional notes when using the above procedure.

1. In the Program operation, the "Capture" mode captures all pins with "L", "H", "Z" and "X" symbols assigned to them in the test vector portion of the JEDEC file. The problem arises for the input pins with the "X" (Don't Care) symbols. For these pins, the captured signal levels will be LOW because the Don't Care pins on the PDS-1 programmer socket are pulled-down to ground.
2. Ensure proper test vectors for designs with asynchronous clock applications. Please refer to Figure 4-44 for more information.

Figure 4-47, Using "Simulate from JEDEC" to display vector errors encountered on the PDS-1 programmer

# 4.18 Simulation Operation - Entering or Editing Waveforms

In the Simulate operation, the test vectors are entered or modified via the "Edit" command. All other commands on the right side of the screen (such as Note, Copy, and etc.) are merely used for organizing the waveform screen. This means that these commands do not affect the results of the vector simulation. Please refer to section 4.19 for more information on the waveform organization commands.

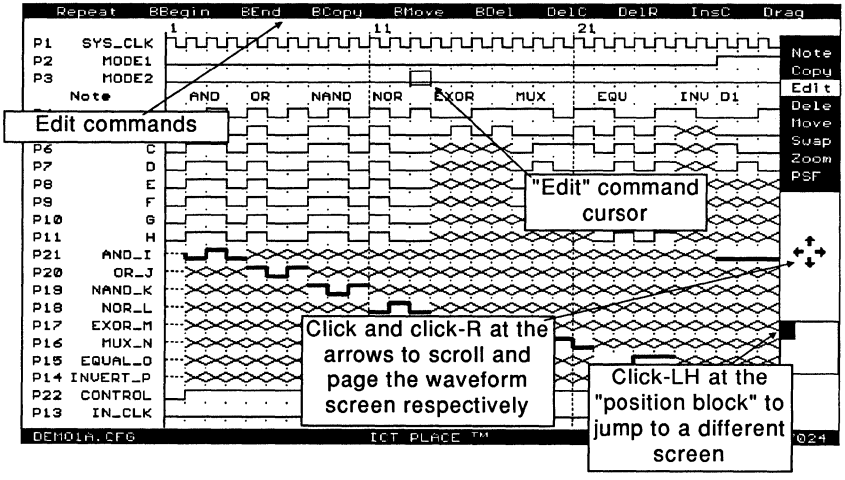


Figure 4-48, "Edit" command in the Simulate operation

Note that only waveform signals for the external pins (inputs or outputs) can be entered or edited. All internal node signals are captured by the simulator and displayed for analysis.

Edit ..... Edits input or output vectors, or inserts the text into the rows generated by the Note command. There are three methods of entering or editing the waveform vectors.

1. Move the edit "box" cursor to a vector location and click the mouse button. Continue clicking until the desired waveform signal is displayed. Since there are eight different signals possible, each vector is selected again after every eight clicks.
2. Move the edit cursor to a vector location and press the vector symbol keys such as C, 1, 0, P, H, L, X or Z to select the type of waveform signal. For instance, pressing the key "C" will select the clock signal for the current vector location. Refer to Table 4-4 or 4-5 for the description of each

waveform signal. Note that the vector symbols are actually the standard symbols used in the test vector section of the JEDEC file.

3. Use the "Drag" command which will be described later in this section.

Once the "Edit" command is selected, the advanced commands for editing test vectors will appear at the top of the screen and can be selected with the mouse. In addition, the previous block of vectors selected via the BBegin and BEnd commands will be displayed. **Click-R to exit the "Edit" command.**

Repeat . . . . . Repeat allows a single vector to be repeated by a specified number. Click "Repeat" then move the edit cursor to a vector location and click. This vector location will be the starting location. Then, enter the number of vectors to repeat and press Enter. All existing vectors following the starting vector will be overwritten.

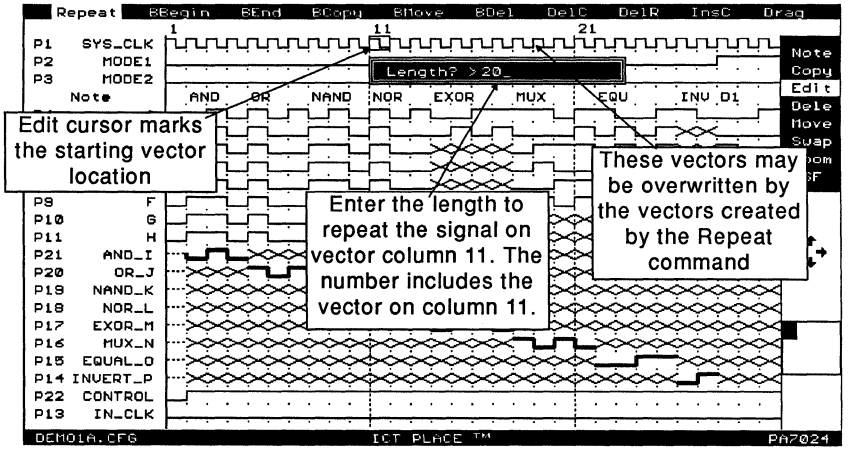


Figure 4-49, "Repeat" command

The commands which begin with the letter "B" indicate that they are block commands. Block commands are commands which manipulate a block of test vector referred to as a "vector block" (Figure 4-50).

BBegin . . . . . This command allows a vector location to be selected as the beginning vector of the "vector block". If no current block exists, then the PLACE software automatically enters the "BEnd" command immediately after the selection of the beginning vector. If a block exists, then a new beginning vector can be selected. The previous ending vector will remain unchanged.

BEnd ..... Allows the selection of an ending vector for the "vector block". Like the "BBegin" command, a new ending vector can be selected for a current "vector block". If a block does not exist, then the selected ending vector is still applicable the next time a beginning vector is selected.

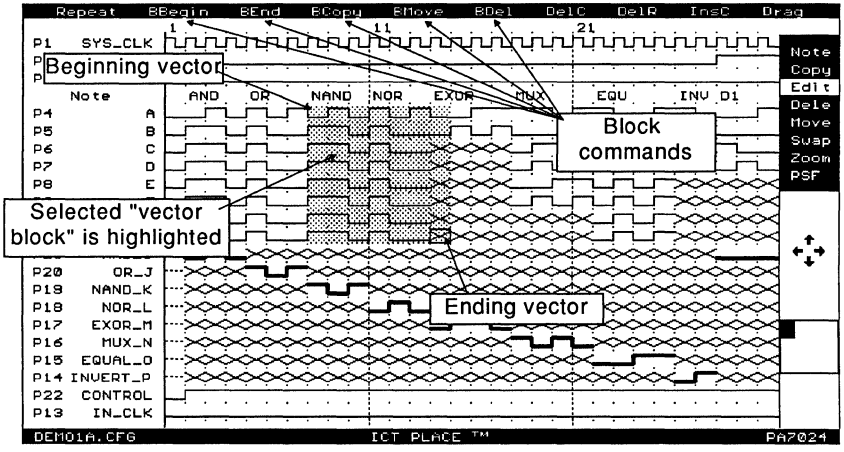


Figure 4-50, Vector block selected

☞ The beginning and ending vectors of the "vector block" must always be located on the upper-left and lower-right of the block respectively. A block can have a single row or column. In this case, the beginning vectors are the most-left or top vectors, and the ending vectors are the most-right or bottom vectors. In addition, beginning and ending vectors can be located on separate waveform screens.

BCopy ..... Copies the currently selected block into another waveform area after the selection of a starting vector location.

BMove ..... Moves the currently selected block into another waveform area after the selection of a starting vector location.

BDel ..... Deletes the currently selected block of vectors. A pop-up window to confirm the deletion will appear.

The following lists the row or column commands.

DelC ..... Enters a mode which allows the current waveform vector column to be deleted. Additional clicks will continue to delete the next vector column. Click-R to exit this mode.

DelR ..... Enters a mode which allows all the vectors on the selected waveform vector row to be deleted. Click-R to exit.

InsC ..... Enters a mode to allow vector columns to be inserted. The vector column is inserted prior to the selected vector column (Figure 4-51). Additionally, the signals on the new column follow the selected vector column.

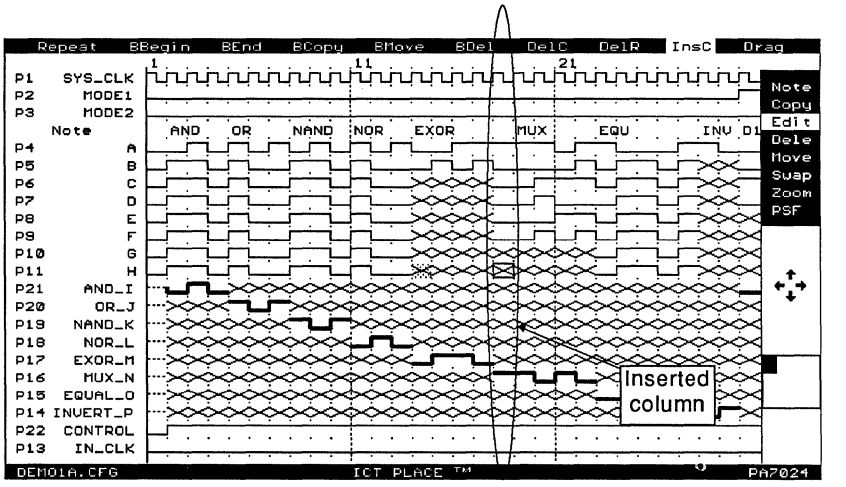


Figure 4-51, Inserting a vector column

Drag ..... Enters a mode which allows input or output signals to be entered or edited. Only four signals are available in the drag mode: input "0"; input "1"; output "L"; and output "H".

Select the waveform vector row and column after you have entered the "Drag" command. The drag edits will start from this location. Move the cursor horizontally across from left to right and click at the selected vector location to end the current signal. Click again to select another vector location. To exit the drag mode, click-R or press the [Esc] key. **Note that the drag edits will overwrite the previous vectors.**

Selecting the input or output signal

The input signal (blue or normal width) is selected when the "Drag" command is first selected. **To "drag" an output signal, press ^X or [Ctrl]-X during the "dragging" process, i.e. the input signal is currently being dragged. Pressing [Ctrl]-X during the drag process toggles between dragging an input or an output signal.** The output signal is indicated by a yellow or thick line.

## 4.19 Simulation Operation - Organizing Waveforms

All the commands in this section are used to organize the display of the waveform screen for a better understanding of the PLACE designs. This means that these commands do not affect the results of the simulation or the actual generation of the test-vectors for the JEDEC file. In each CFG Simulate file, a maximum of 99 waveform rows are allowed.

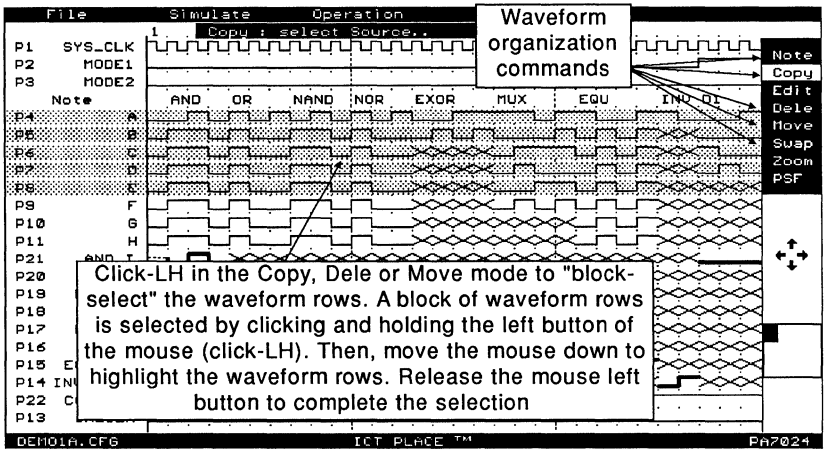


Figure 4-52, Commands for organizing the waveform screen

Note ..... Allows a "Note" row to be inserted for adding comments to the waveform display. Add the note line by clicking at the desired line, click-R to exit note command then select the "Edit" mode. Move the edit cursor to the note line and click to enter text for the comments.

Copy ..... Copies a waveform vector row or a "block" of selected waveform rows to another location. This command will prompt for a source and target selection. Click-R to exit this mode.

Dele ..... Removes a waveform vector row or a "block" of selected waveform rows from the current waveform screen. Note that the unduplicated waveform rows for external pins and internal nodes will be appended to the bottom of the CFG file (last screen of the waveform display). All other waveform rows such as Notes and duplicated rows (i.e. rows that were copied using the "Copy" command) can be removed from the CFG file. The CFG file has a minimum number of waveform rows allocated for each device type that cannot be removed. For instance, the PA7024

device has 62 waveform signals (22 inputs/outputs + 20 LCC internal outputs + 20 IOC registered nodes) that are always present in the CFG file.e. Click-R to exit.

Move ..... Allows a waveform vector row or a "block" of selected waveform rows to be moved from one location into another location. This command will prompt for a source and target selection. Click-R to exit.

Swap ..... Allows a waveform vector row to be swapped with another vector row. This command will prompt for a source and target selection. Click-R to exit. No "block" swapping is available.

## 4.20 Simulate Operation - Zoom Command

When the **"Zoom"** command is selected, the waveform screen displays 170% more vectors than the normal screen. Normally, the waveform screen is 22 rows by 30 columns. But in the zoom mode, the screen is 30 rows by 60 columns. With more vectors being displayed, more waveform vectors can be viewed on a single screen, which may lead to a better understanding of the overall design.

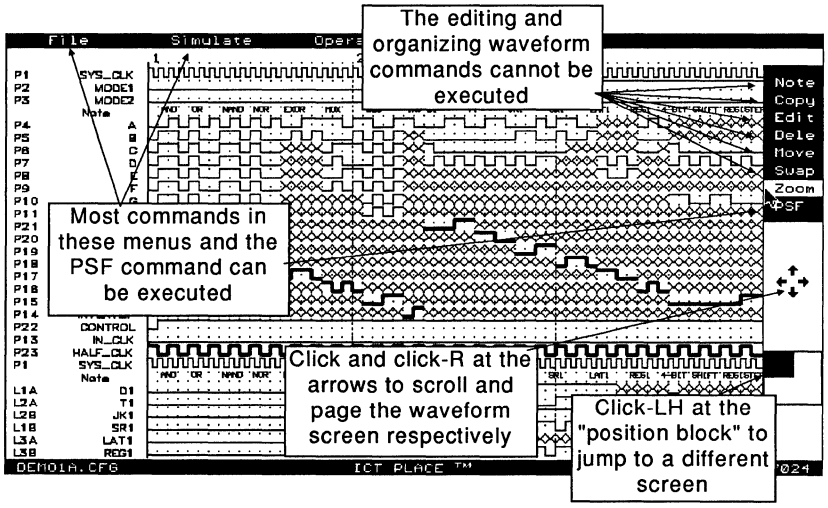


Figure 4-53, Mode A of the "Zoom" waveform screen

Within the Zoom mode, there are actually two separate modes which will be referred to as Zoom Modes A and B. A typical procedure of using the Zoom mode is:

- From the normal waveform screen mode, click at the **"Zoom"** menu on the right side of the screen to enter Zoom Mode A. The screen in this mode consists of 30 rows of waveforms and 60 columns of vectors.
- In Mode A, almost all commands in the Simulate operation can be executed. These commands include file read and save, simulate, capture, or the PSF command (section 4.21). Some of the commands not executable in Mode A are the Note, Edit, Erase, Copy, Move and Swap commands. If you click-R in Mode A, you will be returned to the normal waveform screen mode.

➤ To enter Mode B, click at the **"Zoom"** menu once again but this time don't release the left button of the mouse. A rectangular box depicting a window view of the current selected waveform screen is displayed (Figure 4-54). This rectangular "view" window can be moved to another location by moving the mouse. If you wish to return to Mode A at this time, press the right button of the mouse while the left button is being pressed. Otherwise, releasing the left button of the mouse will return you to the normal waveform screen selected via the rectangular "view" window.

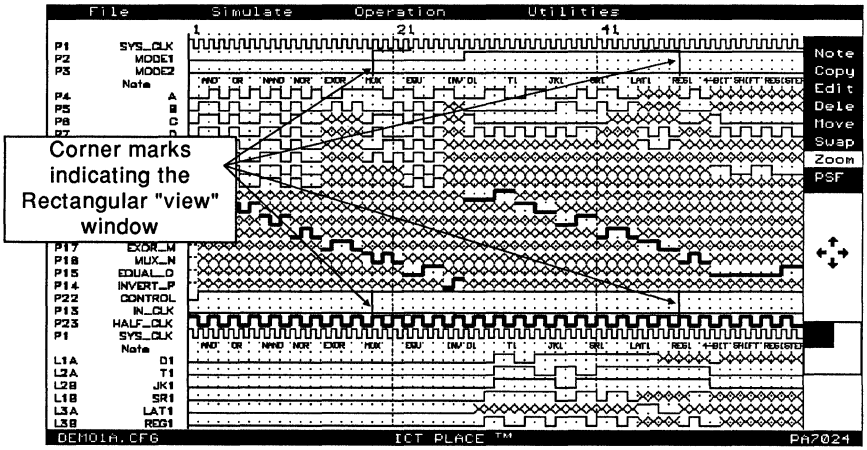


Figure 4-54, Mode B of the "Zoom" waveform screen

## 4.21 Simulate Operation - PSF Command

The PSF design file can be displayed on the waveform screen by selecting the **"PSF"** command located on the right side of the screen. With the PLACE design source file displayed, you can compare the simulation results with the design logic. If a simulation waveform vector error is detected, then the modification can be done instantly using the "Edit" command. If the error is in the design logic, then return to Design operation to correct the error and re-compile the PSF file.

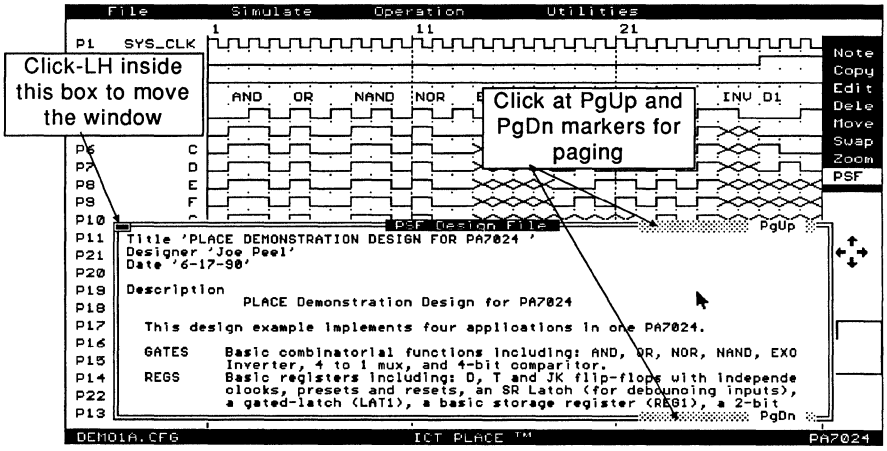


Figure 4-55, Mode B of the "Zoom" waveform screen

As shown in Figure 4-55, a window will pop-up displaying the PLACE design source file. The features of this window are similar to those available for the PSF Text Display windows found in the Design operation. These features include paging up and down the display screen and window sizing. An additional feature not available in the Design operation is the moving of the display window to another location (Figure 4-57). **To close the PSF window, press the [Esc] key or click-R.**

### Paging Up and Down

Like in the Design operation, paging within the PSF window is accomplished by clicking at the PgUp or PgDn markers located at the top and bottom of the window, or by pressing the PgUp and PgDn keys. See Figure 4-55.

## Sizing the Display Window

The size of the window can be adjusted by pressing the Up and Down cursor keys followed by the ENTER key. The Up cursor key increases the window size while the Down cursor key decreases the size. A maximum of 19 lines of text can be displayed on the window.

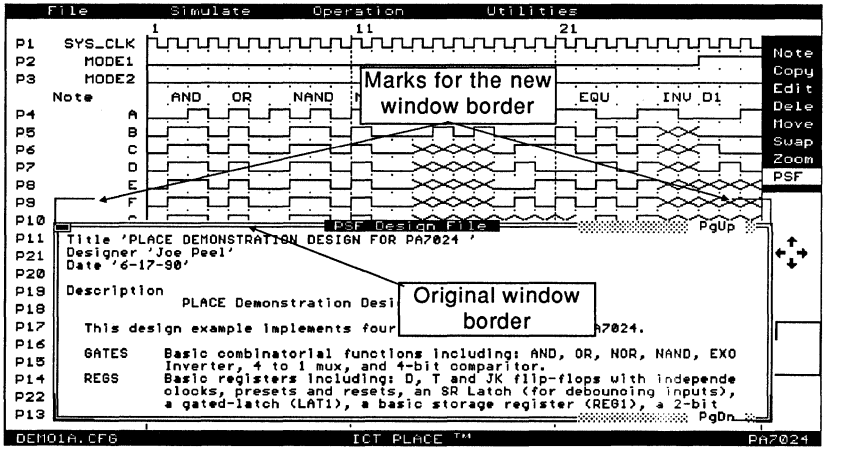


Figure 4-56, Sizing the PSF display window

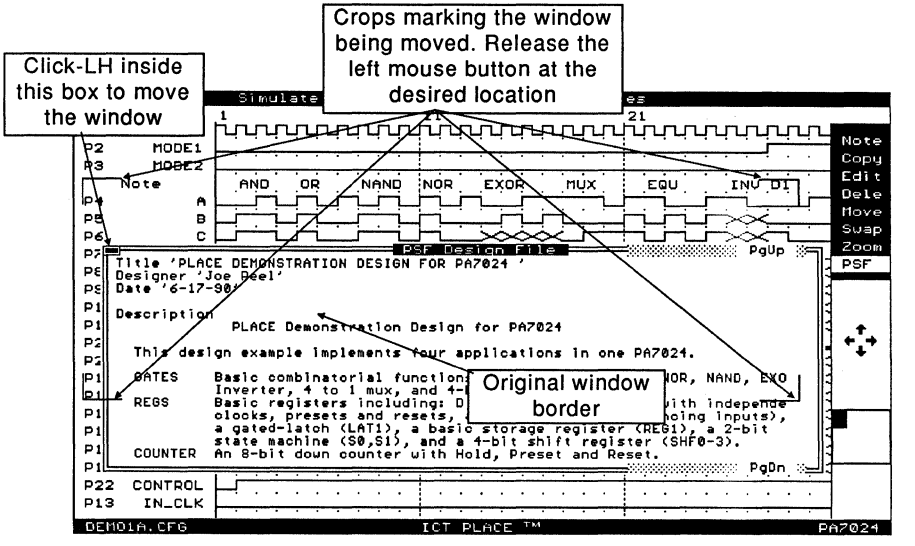


Figure 4-57, Moving the PSF display window

## 4.22 Document Operation - Document Window

In the Document operation, the documents relating to a PLACE design can be printed via some of the most popular printers, such as IBM and Epson graphic printers, HP Laserjet II and postscript laser printers. In addition, the printing of these documents (including the design configuration and simulate waveform screen images, PSF design file, compiled outputs and etc.) can be set up in a queue or batch mode.

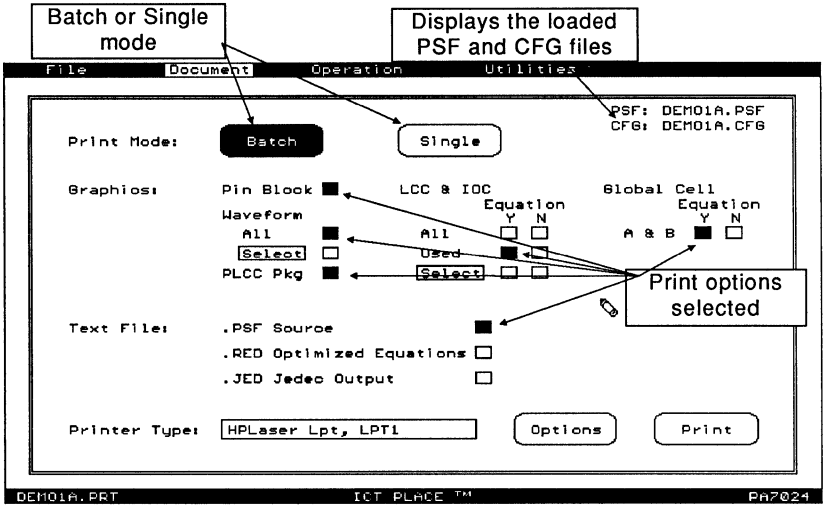


Figure 4-58, Document window for PA7024

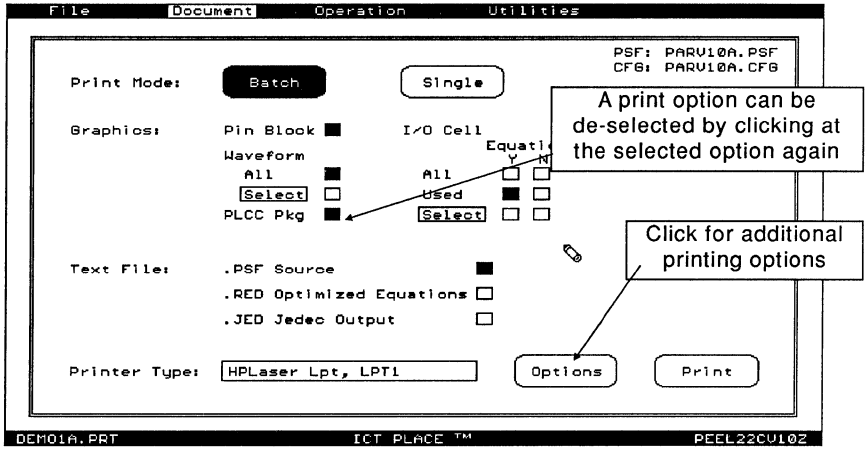


Figure 4-59, Document window for PEEL22CV10A

☞ As shown in the Figures 4-58 and 4-59, the current PSF and CFG files loaded are displayed at the upper-right corner of the window. If these files exist, they will be loaded automatically upon boot-up of the Document operation. However if desired, a different PSF design file or simulation waveform CFG file can be read from the "File" menu.

After making the print option selections, the printing is initiated by clicking at the "Print" command located at the lower-right corner of the window. **Remember that a print option can be de-selected by clicking at the selected (highlighted) option again.** Note that all selected print options can be saved via the "Save" or "saveAs" command (as a ".PRT" file) in the "File" menu window.

Print Mode ..... Allows the selection of "Batch" or "Single" printing.
- Single printing allows one graphics screen or text file to be selected and printed at a time.
- Batch printing allows several screens or text files to be selected, each printed out sequentially.

Graphics ..... This option is used to select the graphics screens to be printed, including: Block Diagram Screen "Pin-Block", PLCC package configuration (if applicable), LCC/IOC and GBC graphic screens for PEEL Arrays or IOC graphic screens for PEEL Devices and the CFG waveform screens. In addition, the logic equations for the LCC or IOC may be appended to each printed design configuration graphic screen .

To select a graphic screen, click at the print option box until it is highlighted. The equation (Y/N) selection includes or excludes the equations for each LCC/IOC or IOC screen.
- **Pin Block:** Selects the pin block diagram for printing. The pinout will be in DIP configuration for all devices except for the PA7140 device which will be in PLCC configuration.
- **Waveform:** Allows waveform screens to be selected for printing.
  - All: Selecting "All" will print all waveforms.
  - Select: Selecting the "Select" option allows specific waveform screen to be chosen for printing. See to section 4.23 for more information.
- **LCC / IOC (PEEL Arrays) or IOC (PEEL Devices):** Allows the design cell configuration screens to be selected for printing. For PEEL Arrays, the LCC/IOC screens will be printed. If it is a PEEL device, then the IOC screens will be selected for printing.

All: Selects all cells (LCC/IOC for PEEL Arrays and IOC for PEEL Devices) for printing.
Used: Selects only used or labeled cells for printing.
Select: Allows specific cells to be selected for printing. Refer to section 4.24 for more information.

- **Global Cell (PEEL Arrays only):** Selects all global cells for printing. The equation (Y/N) selection includes or excludes the equations for each Global Cell screen.

Text File ..... Selects the PSF design source file, the RED compiled reduction file which contains the reduced equations from the PLACE optimizer, and the JEDEC file for printing.

Printer Type .... Selects printer type and set-up. Refer to section 4.25.

Options ..... Selects additional printing options (Figure 4-60).

- **Waveform Zoom:** Sets whether the waveform screens to be printed are in the normal or zoom screen mode.
- **Print to file:** Redirects all printer outputs to a file. The file name will be prompted for immediately after selecting this option.
- **COM Rdy Handshake (Postscript printer only):** If sets to the ON condition, the PLACE software waits for an end-of-job character (ASCII# 4) from the printer after sending each graphic screen. If set to the OFF condition, the PLACE software continues to the next print job without waiting for an answer from the printer. The PLACE software utilizes the XON/XOFF handshake signals when communicating with the postscript via the COM port. **It is recommended to set to the OFF condition if a printer buffer or spooler is used.**

Print ..... Initiates the printing with the currently selected options.

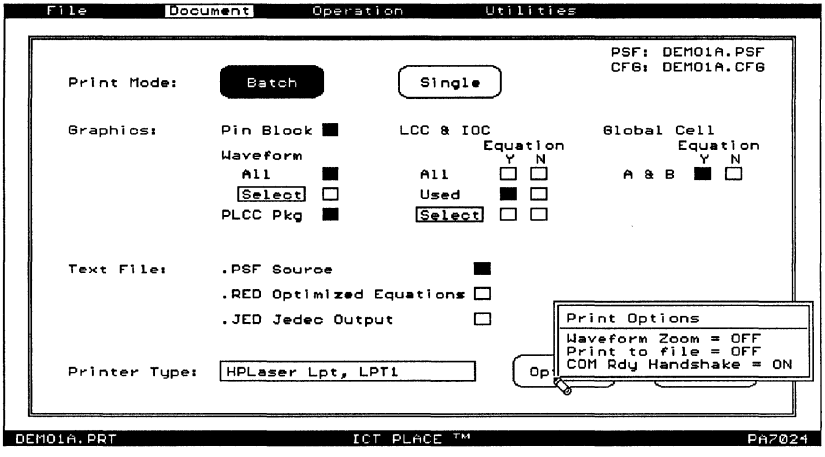


Figure 4-60, "Options" command

# 4.23 Document Operation - Waveform "Select" Print Option

The waveform "Select" option allows specific waveform screens to be selected for printing. Figure 4-61 shows the waveform "Select" screen.

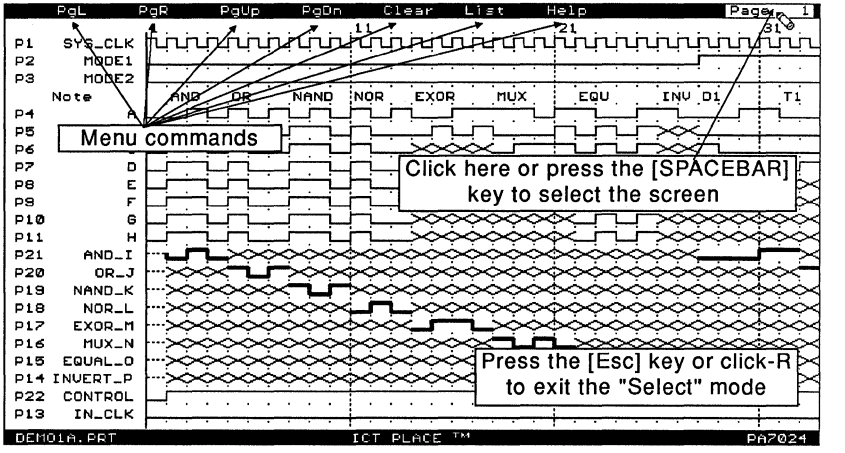


Figure 4-61, Waveform "Select" screen

Selecting a screen ..... A waveform screen can be selected by pressing the [SPACEBAR] key or clicking at the page number located at the upper-right corner of the screen. Once selected, the page number of the screen will be highlighted. For a list of selected waveform screen, click at the "List" command.

PgL or
Left cursor key .... Pages the screen to the left.

PgR
Right cursor key .. Pages the screen to the right.

PgUp or
Up cursor key or
[PgUp] key ..... Pages the screen up.

PgDn or
Down cursor key or
[PgDN] key ..... Pages the screen down.

List ..... Lists all the selected waveform page numbers.

Help ..... Displays the Help screen.

## 4.24 Document Operation - LCC/IOC or IOC "Select" Option

In PEEL Arrays, the LCC and IOC "Select" screen allows specific LCC/IOC pairs to be selected for printing. The selection is made by clicking at the LCCs or IOCs and the LCC/IOC pairs will be highlighted. In PEEL devices, the IOCs are selected with the similar method, i.e. clicking at the IOCs until highlighted.

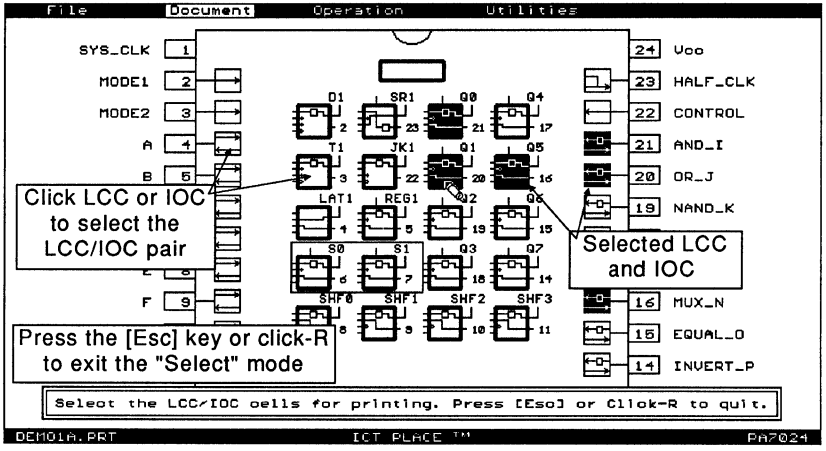


Figure 4-62, LCC/IOC "Select" screen for PA7024

# 4.25 Document Operation - Printer Type Selection

Unlike the "Print" command in the "File" menu window of the Design, Compile, Simulate and Program operations (in which only the IBM and Epson graphic printers are supported), several popular printers are supported in the Document operation. These printers include IBM, Epson, HP Laserjet II and Postscript laser printers.

If you are setting up the Document operation for the first time, then you will need to configure the printer type and set-up. Once configured, the printer type and its set-up will automatically be loaded each time the Document operation is selected.

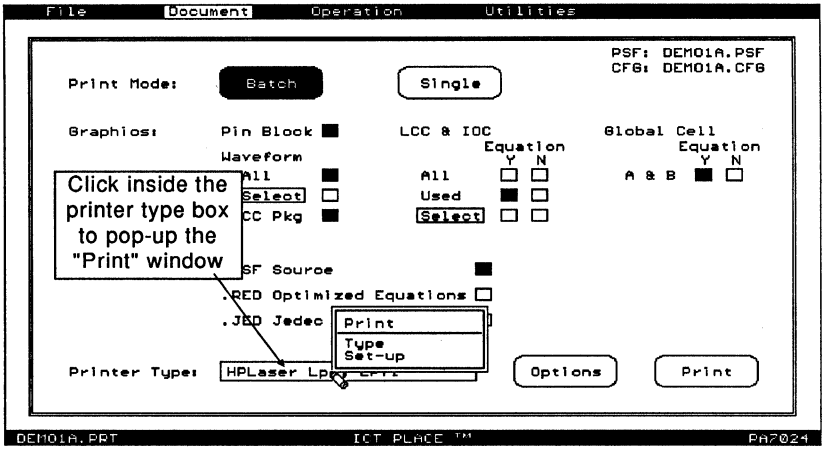


Figure 4-63, Setting the printer type and set-up

After opening the "Print" window as shown in Figure 4-63, select the "Type" option to choose your printer type. Note that the printer type selection also sets the type of interface (parallel or COM) used. The "Set-up" option sets the parameters of the selected printer interface.

Type ..... Printer with the type of interface (paraller or COM) used.
- **IBM:** Sends the printer outputs in IBM printer command format via the parallel port.
- **Epson:** Sends the printer outputs in Epson printer command format via the parallel port. Both IBM's and Epson's command format are very similar to each other.
- **HPLaser Lpt:** Sends the printer outputs in HP Laserjet II printer command language via the parallel port.

- **HPLaser Ser:** Sends the printer outputs in HP Laserjet II printer command language via the serial communication port (COM port).
- **Postscript:** Sends the printer outputs in Postscript printer command language via the serial communication port (COM port). Uses the XON/XOFF handshake signals. For more information, refer to section 4.22 for the description of the "Options" menu.

Set-up ..... Allows the printer interface to be configured. To make the set-up selections, click at the options in the "Printer Setup" window until the desired selection appears. Then, press the [Esc] key or click-R to return to the "Print" pop-up window.

- **Parallel port (LPT):** Allows the port number LPT1, LPT2 or LPT3 to be selected.
- **COM:** Allows the port number COM1 or COM2, baud rate, data size, stop bits and parity to be selected.

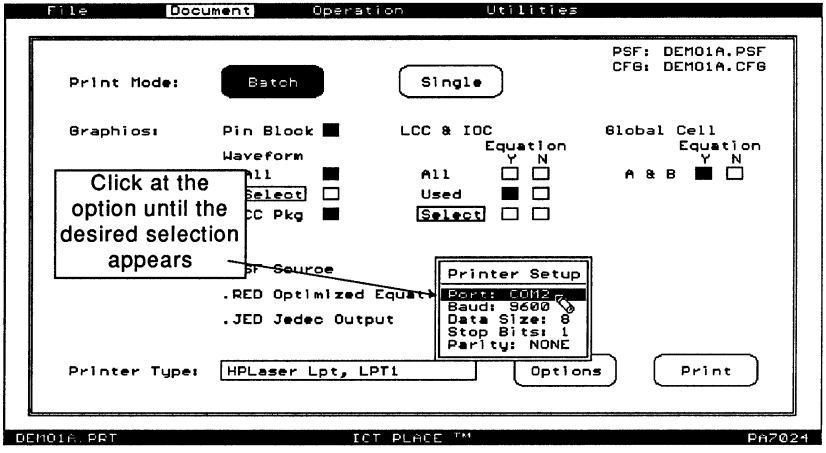


Figure 4-64, "Printer Setup" window

## 4.26 Program Operation - PDS-1 Interface Window

If an ICT PDS-1 programmer is installed in your computer, the PLACE senses it and automatically sets the PDS-1 Interface window in the Program operation. This window contains commands specifically used for programming, verification, loading, applying test vectors and other hardware related operations via the PDS-1 programmmer.

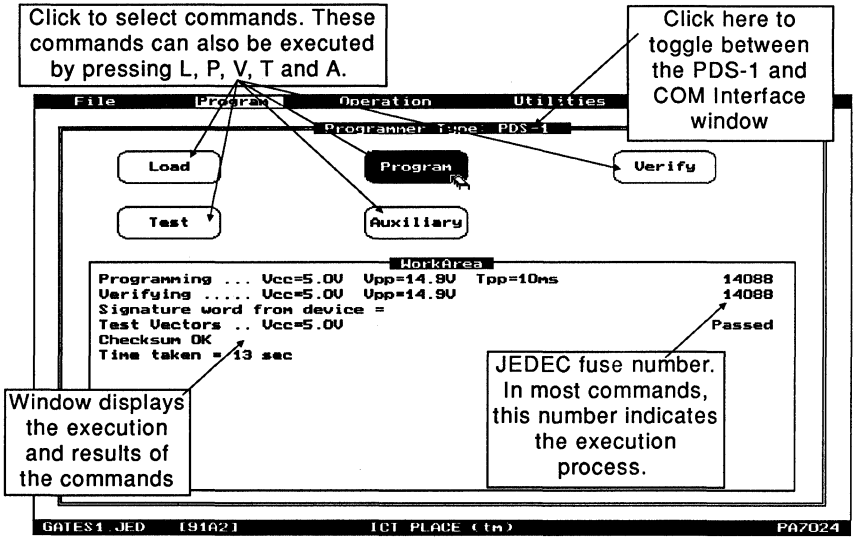


Figure 4-65, PDS-1 Interface window in the Program operation

☞ If the JEDEC file with extension ".JED" exists (i.e. successful compilation of the PSF design file), then it will be loaded into the memory automatically upon boot-up of the Program operation. Otherwise, the JEDEC file can be read via the "File" menu.

Programmer Type ..... The "Programmer Type" box allows selecting between two programmer interfaces, the PDS-1 or COM port. This feature is activated only if a PDS-1 programmer is installed in the computer.

Load ..... Loads the device and stores the data in JEDEC format in the memory. The file name is defaulted to DEVICE.JED. Check sum is calculated and displayed beside the file name.

Program ..... The programming process includes (in the order of execution):
- Bulk erase of the device (similar to the "Erase All" command in the "Auxiliary" menu window).
- Programs the device with the JEDEC file in memory.
- Verification of the programmed data.
- If the "Auto-secure" feature in the "Auxiliary" menu window is turned ON , then the device security bit will be automatically programmed and verified after device verification. After the device is secured, its contents cannot be read out.
- If the JEDEC file has test vectors, then they will be used to exercise the device.
- The device check sum is re-calculated and compared with the check sum of the JEDEC file in the memory.
- Time taken for the programming process.

If an error is encountered (such as verification, security bit or test vector error), the programming process is aborted.

Verify ..... Verifies the device with the current loaded JEDEC file in memory. If the JEDEC file has test vectors, then they will be used to exercise the device. The device check sum is re-calculated and compared with the check sum of the JEDEC file in the memory.

Test ..... Allows application of test-vectors to the device. The test vectors are applied to the device in a serial manner, i.e. input signals are applied from pin 1 to 24 (default condition - see "Apply pins" option below). Inputs 0 and 1 are applied first, then C (clock pulse), then the outputs are sensed and compared with the current output signal.
- **Normal:** Applies the test vectors normally. If a test vector error occurs, the testing stops. To continue testing, press the [SPACEBAR] key or click the mouse button. To abort testing, press "Q".
- **Single step:** Single step each vector by pressing any key or clicking the mouse button.
- **Capture:** Captures the outputs of the device. The captured signals will overwrite the current signals. Note that only pins (include both input and output pins) with the signals L, H and X will be captured. The captured vectors reside only in memory and can be saved by the "Save" or "saveAs" command. Refer to Figure 4-47 for information on its applications.
- **Begin/End:** Sets the Begin and End vectors during the Normal, Capture or Single step process.
- **To file:** If set to YES, then the test vectors displayed during the Normal, Capture or Single step process are sent to a file. The file name follows the JEDEC file name but with extension ".VEC".
- **Apply pins:** This option allows the device test vectors to be applied starting from pin 1 to 24 (**Default condition**) or pin 24 to 1. This feature may be useful for testing asynchronous applications. Refer to Figure 4-44.

Auxiliary ..... Selects Auxiliary functions which include:

- **Space Bar:** If set to ON, the last command will be executed in the main window. For instance, if the last command was the Program command, then pressing the [SPACEBAR] key will repeat this command.
- **Auto Secure:** If set to ON, the security bit will be programmed and verified in the Program command.
- **Read Signature:** Reads the Signature word of the device.
- **Write Signature:** Allows the Signature word to be added into the JEDEC file in the memory. It will then be written to the device. Restriction is that the signature word must be unprogrammed initially.
- **Compute Checksum:** Computes the check sum of the device.
- **Secure:** Sets the security bit of the device. After the device is secured, its contents cannot be read out. The security bit of the device can only be cleared by the "Erase All" procedure.
- **Erase All:** Bulk erases the device.
- **Write All:** Writes the data "0" to all the JEDEC fuses in the device.

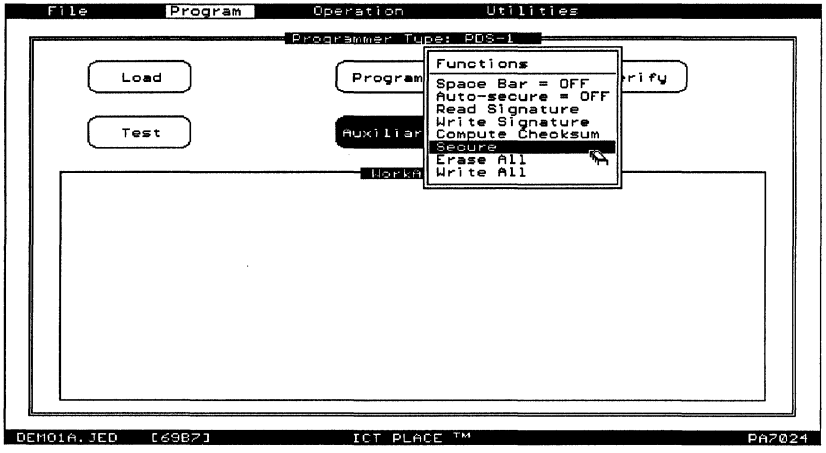


Figure 4-66, "Auxiliary" menu window

## To view the current JEDEC file

The current JEDEC file in the memory can be analyzed using the "Editor" command in the "Utilities" menu window. Once in the editor, all the features and functions available in the editor of the Design or Compile operation are applicable here. Refer to section 4.28. **Press the [Esc] key or click-R to return to the previous screen.**

## 4.27 Program Operation - Serial Communication Port Window

The "PC Com" Interface window is automatically displayed if the ICT PDS-1 programmer is not installed in your computer. The commands in this window allow the JEDEC file to be transmitted or received via the COM port to or from a third-party programmer which has a serial communication file transfer utility.

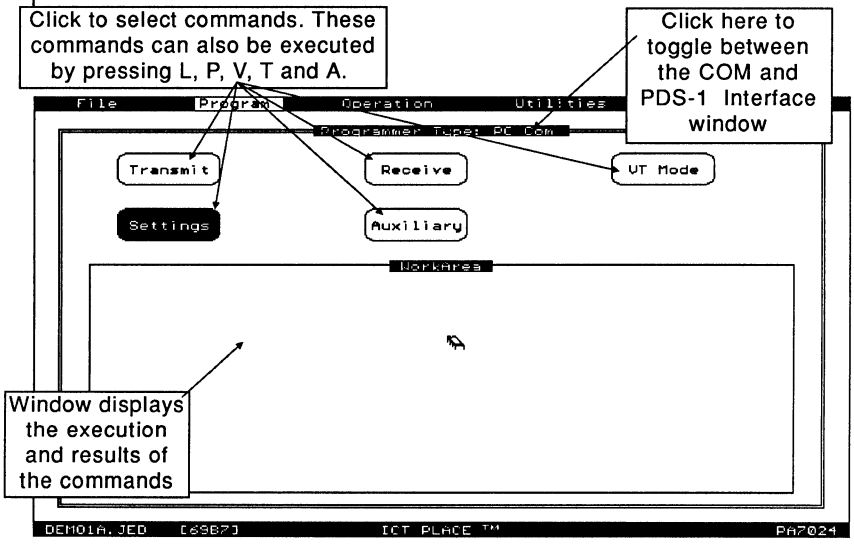


Figure 4-67, "PC Com" Interface window

☞ If the JEDEC file with extension ".JED" exists (i.e. successful compilation of the PSF design file), then it will be loaded into the memory automatically upon boot-up of the Program operation. Otherwise, the JEDEC file can be read via the "File" menu.

Programmer Type ..... The "Programmer Type" box allows selecting between two programmer interfaces, the PDS-1 or COM port. This feature is activated only if a PDS-1 programmer is installed in the computer.

Upload ..... Sets computer to receive JEDEC file from the serial communication (COM) port.

Download ..... Sends currently loaded JEDEC file to the serial communication (COM) port.

VT Mode ..... Sets video terminal emulation mode with current settings. See "Settings" below.

Settings ..... Allows communication port parameters such as baud rate, data bits, parity, stop bits, and serial COM port number to be selected.

Auxiliary ..... Selects Auxiliary functions such as
- **Space Bar:** If set to ON, the last command will be executed in the main window. For instance, if the last command was the Program command, then pressing the [SPACEBAR] key will repeat this command.
- **Auto-secure:** If set to ON, the JEDEC field "G1" is added to the JEDEC file in the memory. This field enables the security bit programming in the PLD programmer. Note that some programmers will override this option and require you to turn the security bit programming manually.
- **Read Signature:** Reads the Signature word of the JEDEC file in memory.
- **Write Signature:** Allows the Signature word to be added into the JEDEC file in the memory.
- **Compute Checksum**: Computes the check sum of the JEDEC file in memory.

## To view the current JEDEC file

The current JEDEC file in the memory can be analyzed using the "Editor" command in the "Utilities" menu window. Once in the editor, all the features and functions available in the editor of the Design or Compile operation are applicable here. Refer to section 4.28. **Press the [Esc] key or click-R to return to the previous screen.**

## 4.28 PLACE Text Editor

Figure 4-68 shows the PLACE text editor (a Wordstar™-like) that is used in the Design, Compile and Document operations. In the Design operation, the text editor is primarily used for entering or modifying the logic descriptions of the design. In the Compile operation, the editor is interfaced closely with the PLACE compiler. If a compilation syntax error is encountered, the editor opens automatically and displays the line with the error. If possible, this error can then be analyzed and modified without returning to the Design operation. In the Document operation, the editor is mainly used for displaying the JEDEC file.

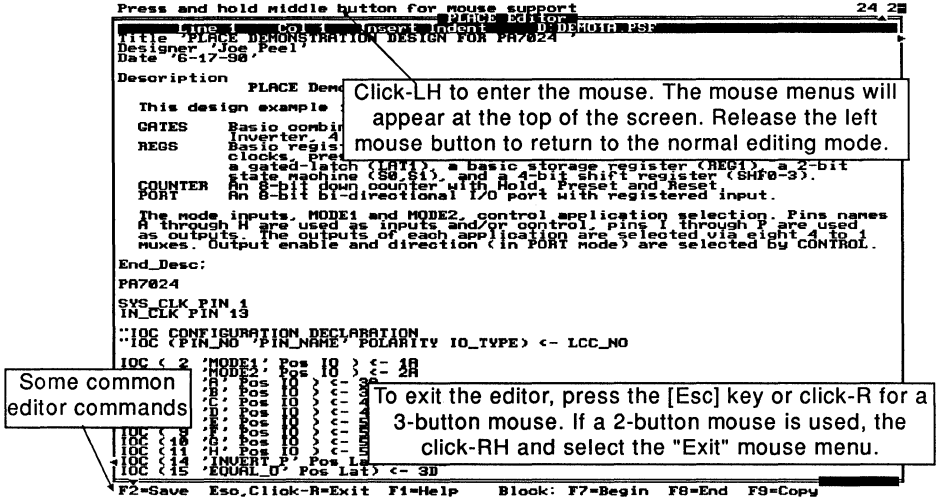


Figure 4-68, PLACE text editor

### Using mouse in the editor

The PLACE text editor supports some of the editor commands via the mouse. As shown in Figure 4-68, press and hold the middle or right button of the mouse (the button depends on whether a 2 or 3-button mouse is used) to enter the mouse mode. Once in the mouse mode, no text editing can be done. Instead, only screen paging and scrolling, and cursor movement can be performed (Figure 4-69). To exit the mouse mode, release the left button of the mouse. The best application of the mouse is to quickly move the editor cursor to another location.

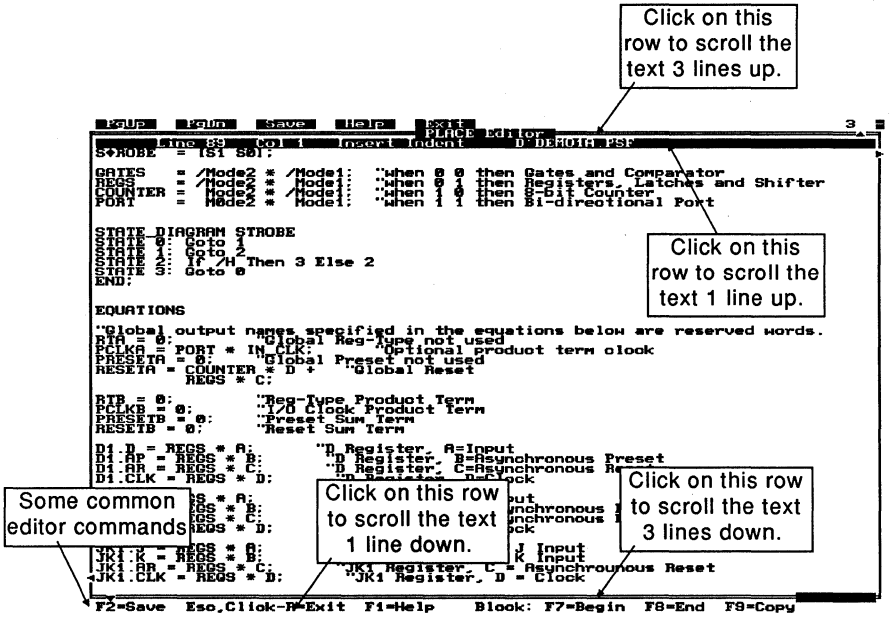


Figure 4-69, Mouse mode in the PLACE Text Editor

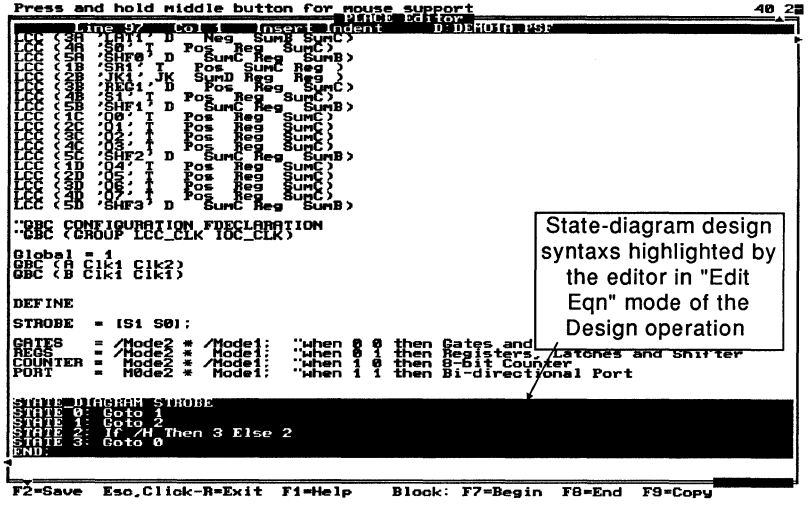


Figure 4-70, Automatic block selection by the editor in the Design operation

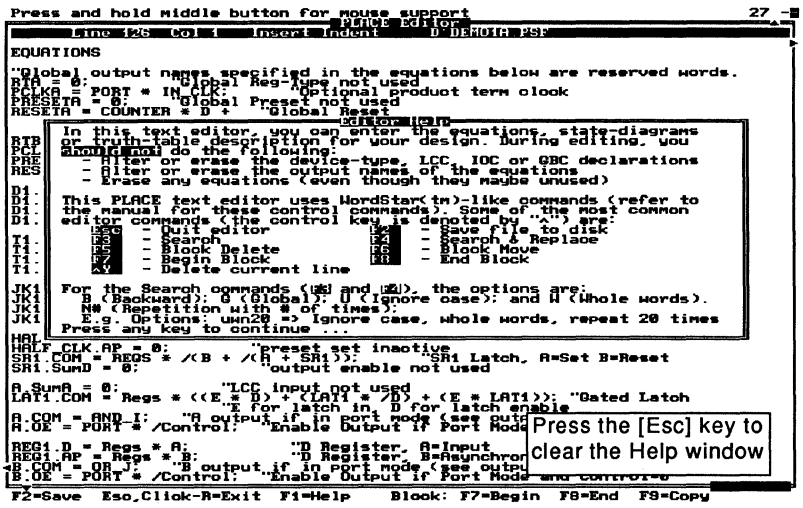


Figure 4-71, Help screen in the editor

## Text Editor Keyboard Commands

### Screen and cursor movement

| Functions | Commands |
|---|---|
| Character left | .^S or Left arrow key |
| Character right | .^D or Right arrow key |
| Word left | .^A or ^-Left-arrow key |
| Word right | .^F or ^-Right arrow key |
| Line up | .^E or Up arrow key |
| Line down | .^X or Down arrow key |
| Scroll up | .^W or ^-Up-arrow key |
| Scroll down | .^Z or ^-Down-arrow key |
| Page up | .^R or [PgUp] key |
| Page down | .^C or [PgDn] key |
| Top of file | .^QR or ^-[PgUp] key |
| End of file | .^QC or ^-[PgDn] key |
| Begin of line | .^QS or [Home] key |
| End of line | .^QD or [End] key |
| Top of screen | .^QE or ^-[Home] key |
| Bottom of screen | .^QX or ^-[End] key |
| Top of block | .^QB |
| Bottom of block | .^QK |
| Previous cursor | .^QP |
| Jump marker 0..3 | .^Q0..^Q3 |
| Set marker 0..3 | .^K0..^K3 |

### Insert and delete

| Functions | Commands |
|---|---|
| New line | ^M or [Enter] key |
| Insert line | ^N |
| Tab | ^I or [Tab] key |
| Delete current character | ^G or [Del] key |
| Delete character left | ^H or [Backspace] key |
| Delete word | ^T |
| Delete to end of line | ^QY |
| Delete line | ^Y |

## Block Functions

In the Design operation, the PLACE software selects and highlights a block of text automatically when the editor is opened via the PSF Text Display windows. If desired, specific text can be manually "blocked" via the [F7] and [F8] function keys. This is done by first moving the editor cursor to the location which marks the beginning of the block and then press the [F7] key. Then, move the cursor to the "end" location of the block and press the [F8] key. A block is selected if it is highlighted.

| Functions | Commands |
|---|---|
| Begin block | ^KB or [F7] key |
| End Block | ^KK or [F8] key |
| Copy block | ^KC |
| Move block | ^KV |
| Delete block | ^KY |
| Hide block | ^KH |
| Mark single word | ^KT |
| Read block from file | ^KR |
| Write block to file | ^KW |
| Print block | ^KP |

### Miscellaneous

| Functions | Commands |
|---|---|
| Exit editor | ^KQ or [Esc] key |
| Save and Open new file | ^KD |
| Toggle insert mode | ^V or [Ins] key |
| Toggle autoindent | ^OI |
| Toggle fixed tabs/smart tabs | ^OF |
| Restore line | ^QL |
| Search string | ^QF |
| Search and replace string | ^QA |
| Repeat last search operation | ^L |

# PLACE Design Language

5

# 5.0 PLACE Design Language

## 5.1 Introduction

To simplify the design entry process, the PLACE software allows control of the architectures graphically. This capability allows the user to better utilize his or her time on the actual design implementation and not on architectural syntax found in most other PLD software tools. Underneath the graphics however,the PLACE software incorporates a powerful design language that provides standard behavioral design methods such as State Diagrams, Truth Tables and Equations.

### PLACE Source File Format

Figure 5-1 shows the format of the PLACE Source File (PSF).

| | |
|---|---|
| ***Design Description:*** | *Title of the design, name of designer, date and detailed description of the design.* |
| ***Device type:*** | *PA7024, PEEL18CV8, PEEL22CV10, and etc.* |
| ***Special features:*** | *Sets Security-bit, Zero-Power or Signature Word.* |
| ***Input or Clock Pins:*** | *Assigns names to the clock and dedicated input pins.* |
| ***Cell Configurations:*** | *PEEL Arrays: IOC and LCC Configurations.*<br>*PEEL Devices: IOC (Macro Cell) Configurations.* |
| ***Global Configurations:*** | *PEEL Array: Group A and B Global Cell Configurations.*<br>*PEEL Devices: Asynchronous and Synchronous node definitions for registered PEEL Devices (e.g. PEEL18CV8, PEEL22CV10, etc.).* |
| **Comments** | Details the description of the design. |
| **Macro Definitons:**<br>**State-diagrams**<br>**Truth-tables**<br>**Equations** | State diagram assignments, and equation and constant declarations. |

Note:
The format categories in ***italics*** are completely controlled and entered via the PLACE architectural software.

Figure 5-1, PLACE Source File Format

Figures 5-2 and 5-3 illustrate the differences between the PSF formats for the PA7024 and PEEL18CV8 devices.

☞ While reading the PSF file, the PLACE software checks the file format for incompatibilities. If any format incompatibilites are found for the selected device type, the PLACE software will display error messages.

```
TITLE ' '
Designer ' '
Date ' '

Description
      Enter description here ...
End_Desc;

PA7024                          "Device type

"Optional Special Features Identifiers
AUTO_SECURE                     "Programs the security bit. If unspecified,
                                "defaults to  Security-bit OFF
SIGNATURE 'ABCDEFGH'            "Programs Signature Word  'ABCDEFGH'

CLK1 PIN 1                      "Input or Clock pin declaration
CLK2 PIN 13

IOC ( 2 "POS IO ) <- 1A         "IOC Declaration
IOC ( 3 " POS IO ) <- 2A
IOC ( 4 " POS IO ) <- 3A
IOC ( 5 " POS IO ) <- 4A
IOC ( 6 " POS IO ) <- 5A
IOC ( 7 " POS IO ) <- 1B
IOC ( 8 " POS IO ) <- 2B
IOC ( 9 " POS IO ) <- 3B
IOC (10 " POS IO ) <- 4B
IOC (11 " POS IO ) <- 5B
IOC (14 " POS IO ) <- 1C
IOC (15 " POS IO ) <- 2C
IOC (16 " POS IO ) <- 3C
IOC (17 " POS IO ) <- 4C
IOC (18 " POS IO ) <- 5C
IOC (19 " POS IO ) <- 1D
IOC (20 " POS IO ) <- 2D
IOC (21 " POS IO ) <- 3D
IOC (22 " POS IO ) <- 4D
IOC (23 " POS IO ) <- 5D
```

Figure 5-2, PA7024 "ANEW7024.PSF" File Template

```
LCC (1A " D  POS  REG  REG )    "LCC Declaration
LCC (2A " D  POS  REG  REG )
LCC (3A " D  POS  REG  REG )
LCC (4A " D  POS  REG  REG )
LCC (5A " D  POS  REG  REG )
LCC (1B " D  POS  REG  REG )
LCC (2B " D  POS  REG  REG )
LCC (3B " D  POS  REG  REG )
LCC (4B " D  POS  REG  REG )
LCC (5B " D  POS  REG  REG )
LCC (1C " D  POS  REG  REG )
LCC (2C " D  POS  REG  REG )
LCC (3C " D  POS  REG  REG )
LCC (4C " D  POS  REG  REG )
LCC (5C " D  POS  REG  REG )
LCC (1D " D  POS  REG  REG )
LCC (2D " D  POS  REG  REG )
LCC (3D " D  POS  REG  REG )
LCC (4D " D  POS  REG  REG )
LCC (5D " D  POS  REG  REG )

Global = 1                      "Number of global cells used
GBC (A Clk1 Clk1)               "Global Cell A configuration
GBC (B Clk1 Clk1)               "Global Cell B configuration

DEFINE                          "Macro Definitions

STATE_DIAGRAM  SD_name          "State diagram design syntax
END;                            "Ends current State diagram syntax

TRUTH TABLE  TT_name            "Truth table design syntax
END;                            "Ends current State diagram syntax

EQUATIONS                       "Logic equation syntax

"Equations for the Global Cell A
RTA = 0;                        "Reg-Type Product Term
PCLKA = 0;                      "IOC Clock Product Term
PRESETA = 0;                    "Preset Sum Term
RESETA = 0;                     "Reset Sum Term

"Equations for the Global Cell B
RTB = 0;                        "Reg-Type Product Term
PCLKB = 0;                      "IOC Clock Product Term
PRESETB = 0;                    "Preset Sum Term
PESETB = 0;                     "Reset Sum Term
```

Figure 5-2, PA7024 "ANEW7024.PSF" File Template (Continued)

```
TITLE ' '
DESIGNER ' '
DATE ' '

Description
     Enter description here ...
End_Desc;

PEEL18CV8                          "Device type

"Optional Special Features Identifiers
AUTO_SECURE                        "Programs Security-bit. If unspecified,
                                   " defaults to security-bit OFF

CLK pin 1                          "Input or Clock pin declaration

IOC (12 " POS COM FEED_PIN )       "I/O  or Macro Cell Configuration
IOC (13 " POS COM FEED_PIN )
IOC (14 " POS COM FEED_PIN )
IOC (15 " POS COM FEED_PIN )
IOC (16 " POS COM FEED_PIN )
IOC (17 " POS COM FEED_PIN )
IOC (18 " POS COM FEED_PIN )
IOC (19 " POS COM FEED_PIN )

AR NODE 21                         "Global Asynchronous Reset  Node
SP NODE 22                         "Global Synchronous Preset Node

DEFINE                             "Macro Definitions

STATE_DIAGRAM  SD_name             "State diagram design syntax
END;                               "Ends current State diagram syntax

TRUTH TABLE  TT_name               "Truth table design syntax
END;                               "Ends current State diagram syntax

EQUATIONS                          "Logic equation syntax

"Equations for the global nodes
AR = 0;                            "Global Asynchronous Reset Equation
SP = 0;                            "Global Synchronous Preset Equation
```

Figure 5-3, PEEL18CV8 "ANEWV8.PSF" Template File

## 5.2 Design Description

The design description section of the PSF format is made up of four fields. The fields include: Title of the design; Designer's name; Date of the design; and a detailed description of the design.

☞ In describing the PSF formats for the following sections (including this one), *italics* will be used to identify fields in which the user would enter identifiers, such as title and date of the design, name of the designer, pin names, and etc. The reserved identifiers will be specified in **bold**. Most of the examples used for illustrating the formats (except for the PEEL device formats) are taken from the Blackjack Machine Application Example (JACK7024.PSF) illustrated in section 6.7. **All reserved identifiers and labels are not case sensitive.**

### Title

**Format:** **Title** *'title of design'*

Example: Title 'Blackjack Machine Example'

Only the characters between the ASCII 32 and 127 can be used in specifying the title of the design. The maximum length of the title is 69 characters.

☞ The characters between the ASCII 32 and 127 are normal characters. These characters include A..Z, a..z, 0..9, space, !, ", $, %, &, ', (, ), *, +, ,, -, ., /, :, ;, <, =, >, ?, @, [, \, ], ^, _, `, {, |, }, and ~.

### Designer

**Format:** **Designer** *'name of the designer'*

Example: Designer 'Joe Peel'

Like the Title identifier, only characters between the ASCII 32 and 127 can be used. The maximum length of the designer's string is 47 characters.

### Date

**Format:** **Date** *'date of design'*

Example: Date 'May 10th, 1991'

Characters valid in the date string are between ASCII 32 and 127. The maximum string length is 47 characters.

### Description

The Description identifier allows the user to specify in detail the description of the design. The user specifies his or her description within the reserved identifiers **"Description"** and **"End_Desc;"**. These identifiers are automatically inserted by the PLACE software.

**Format:** **Description**
*enter description of design here ...*
**End_Desc;**

Example: Description
Blackjack Machine Example

This design example was based on C.R. Clare's design in Designing Logic Systems Using State Machines (McGraw Hill, 1972). The blackjack machine plays ....

All ASCII characters can be used here.

End_Desc;

All PLACE reserved words except "End_Desc" can be used within the "Description" and "End_Desc" identifiers. Each line does not need to begin with a double quotation mark, as required in the Comments field (section 5.9).

## 5.3 Device Type

The target device of the design is declared by simply entering the ICT PEEL device name.

**Format:** *device_type*

The following are the device types supported in Version 2.1 of the PLACE software.

| | | | |
|---|---|---|---|
| **PA7024** | **PEEL18CV8** | **PEEL22CV10A** | **PEEL22CV10** |
| **PA7140** | **PEEL173** | **PEEL22CV10Z** | **PEEL20CG10** |
| **PA7128** | **PEEL273** | **PEEL22CV10A+** | |

## 5.4 Special Features

The special features such as enabling the Security Bit, programming the Signature Word, and setting the Zero Power Bit are available for some of the PEEL devices. These features are optional, meaning that they are not required to be specified in the PSF file. If not specified, the default conditions will be implemented. Refer to the description of each of these features for their default conditions.

### Security Bit

Once the security bit feature is enabled, the programmed data in the device (except for the Signature Word) is prevented from being loaded or read, and hence prevents any unauthorized copying of the design in the PEEL device.

The security bit feature is available for the following devices.

| | | |
|---|---|---|
| **PA7024** | **PEEL18CV8** | **PEEL22CV10A** |
| **PA7140** | **PEEL20CG10** | **PEEL22CV10Z** |
| **PA7128** | **PEEL22CV10** | **PEEL273** |

**Format:** **AUTO_SECURE**

The security bit of the device is enabled via the reserved identifier **AUTO_SECURE**. If this identifier is specified in the PSF file, the PLACE Compiler will create a JEDEC file with the security bit enabled (sets the "G1" field). In most PLD programmers, the "G1" field automatically enables the security bit programming.

**Default condition:** AUTO_SECURE identifier is unspecified. The JEDEC file generated will not have the "G1" field. In most PLD programmers, the user can enable or disable the security bit programming.

## Signature Word

The signature word of the device allows a user to enter a design revision number so that the design can be identifed after the security bit of the PEEL device is enabled. Hence, the signature word data can still be loaded even after the security bit of the device is enabled.

The signature word feature is supported in the following devices. Note that the number of 8-bit bytes in the signature word is specified within the parenthesis.

**PA7024 (8 bytes)**
**PA7128 (1 byte)**
**PEEL22CV10A+ (3 bytes)**
**PA7140 (2 bytes)**
**PEEL273 (2 bytes)**
**PEEL22CV10Z (3 bytes)**

**Format:** **SIGNATURE** *'signature str'*

Example: Signature 'REV. A'

**Default condition:** SIGNATURE identifier is unspecified, which means that the signature word in the device JEDEC file is unused. Note that if the ICT PDS-1 programmer is present, this signature word can be programmed in the Program operation.

## Zero-Power Bit

When the zero-power bit is set, the device can operate at a low standby power condition ("sleep" mode). The device actually senses the inputs or feedbacks for signal transitions. If there are no signal transitions for a certain period, the device automatically goes to "sleep". Please refer to your ICT data book for more information on the AC and DC device parameters.

The device which support the zero-power bit is:

**PEEL22CV10Z**

**Format:** **ZERO_POWER**

The zero-power bit is set when the reserved identifier **ZERO_POWER** is specified.

**Default condition:** The ZERO_POWER identifier is unspecified. Like the signature word feature, the zero-power bit can be set in the Program operation if the ICT PDS-1 programmer is present.

## 5.5 Clock and Input Pins

After labelling a clock or a dedicated input pin (pin that is not associated to an Input Cell or INC) of the device using the **"Label"** command in the Design operation, the PLACE software automatically creates the pin assignment statement.

**Format:** *pin_label* **PIN** pin_number

Example: CLK1 pin 13

Please refer to section 5.6 for the pin label format.

**Default condition:** Unlabeled pin (no pin assignment statement) signifies that the pin is unused.

## 5.6 Pin and Cell Labels

| | | |
|---|---|---|
| **Format:** | First character: | **A..Z, a..z, ~, /, !** |
| | Body of the label: | **A..Z, a..z, 0..9, ~, _** |
| Examples: | Valid labels: | Addr10, ~10, /OUT |
| | Invalid labels: | _Add, 25MHz, /15IN |

The label is not case sensitive. The maximum length of the label is 8 characters (including the / or ! character). **When a / or ! character is added at the beginning of the label, the pin, cell or node becomes an active Low signal path.** Hence, a TRUE logic (logic "1") is resulted when a Low signal is applied.

Example:

```
/A pin 1        "Active Low Input
B pin 2         "Active High Input

IOC (12 'C' Pos COM Feed_pin)      "Output Polarity = Pos
IOC (13 'D' Neg COM Feed_pin)      "Output Polarity = Neg
IOC (14 '/E' Pos COM Feed_pin)     "Output Polarity = Pos
IOC (15 '/F' Neg COM Feed_pin)     "Output Polarity = Neg
```

```
EQUATIONS
C.COM = A;  "C=TRUE or 1 when A=LOW
D.COM = B;  "D=TRUE or 1 when B=HIGH
```

**The / or ! on the pin or cell labels only affect the active level of the inputs or feedback paths** (i.e. variables on the right side of the equal sign in the equations). The polarity of the outputs (i.e. outputs routed to the external pins) are not affected because they are controlled by the IOC configuration statements. In the above example, the feedback active levels and output polarities of cells C, D, E, and F are:

| Cell | Feedback Active Level | Output Polarity |
|---|---|---|
| C | High | High |
| D | High | Low |
| /E | Low | High |
| /F | Low | Low |

## 5.7 Cell Configurations

The cell configuration format statements are used to specify the type of configuration of each cell in the selected device. In most cases, knowledge of the cell configuration formats is not necessary because the configurations of the IOC and LCC are automatically modified by the PLACE architectural software.

Note that all the configuration statements are necessary for the operation of the PLACE software. This means that **you should not delete any of these configuration statements** including the configuration statements for unused cells.

**Format:**

Input Cell in PA7140 and PA7128:

**INC (pin_number *'pin_label'* Input_type)**

Example: INC (3 'A1' Reg)

I/O Cell in PEEL Arrays:

**IOC (pin_number *'pin_label'* output_pol pin_type) <- Assigned_LCC**

Example: IOC ( 4 'V4' Pos IO) <- 3A

Logic Control Cell in PEEL Arrays only:

**LCC (cell_number *'cell_label'* flip-flop_type clock buried_out ext_out)**

Example: LCC (1A 'ADD10' D SumC Reg Reg )

I/O Cell (or Macro Cell) in PEEL devices:

**IOC (pin_number *'pin_label'* output_pol pin_type feedback_type)**

Example: IOC (12 'OUT' POS COM FEED_PIN )

**Default condition:** The default cell configurations are set by the cell configuration statements in the "ANEWxxxx.PSF" files. If the "**New**" function under the File menu command in the Design operation is selected, the PLACE software reads the ANEW file for the selected device (see Table 5-1) and sets the default configurations found in the file.

| ANEW File | Device |
|---|---|
| ANEW7024.PSF | PA7024 |
| ANEW7140.PSF | PA7140 |
| ANEW7128.PSF | PA7128 |
| ANEWV8.PSF | PEEL18CV8 |
| ANEW173.PSF | PEEL173 |
| ANEW273.PSF | PEEL273 |
| ANEWG10.PSF | PEEL20CG10 |
| ANEWV10.PSF | PEEL22CV10 |
| ANEWV10A.PSF | PEEL22CV10A |
| ANEWV10P.PSF | PEEL22CV10A+ |
| ANEWV10Z.PSF | PEEL22CV10Z |

Table 5-1, PLACE ANEW Template Files

## Parameters for the INC Format (PA7140 and PA7128 only)

Pin_Number — The pin number that is assigned to the current Input cell.

| Device | INC Pin Numbers |
|---|---|
| PA7140 (PLCC) | 3-5, 19-21, 25-27, 41-43 |
| PA7128 | 2-6, 8-14 |

*Pin_Label* — See section 5.6 for the format of the pin label.

Input_type — The identifiers for the pin type parameter are:

| Identifier | Function |
|---|---|
| COM | Combinatorial input |
| REG | D-type registered input |
| LAT | D-type latched input |

## Parameters for the IOC Format (PEEL Arrays only)

Pin_Number — The pin number that is assigned to the current I/O cell.

| Device | IOC Pin Numbers |
|---|---|
| PA7024 | 2-11, 14-23 |
| PA7140 (PLCC) | 6-16, 18, 28-38, 40 |
| PA7128 | 15-20, 22-27 |

*Pin_Label* — See section 5.6 for the format of the pin label.

Output_pol — This parameter which refers to the output polarity of the pin is controlled by the following identifiers:

| Identifier | Function |
|---|---|
| POS | Positive Polarity for the Output |
| NEG | Negative Polarity for the Output |

The output polarity "bubble" in the Design operation of the PLACE software controls this parameter. **Inserting the / or ! character in the pin_label does not affect the output (section 5.6).**

Pin_type — The identifiers for the pin type parameter are:

| Identifier | Function |
|---|---|
| IO | I/O |
| REG | I/O with D-type registered input |
| LAT | I/O with D-type latched input |
| OUT | Output only |
| INCOM | Input only |
| INREG | Input only with D-type register |
| INLAT | Input only with D-type latch |
| OUTREG | Output only with D-type registered feedback |
| OUTLAT | Output only with D-type latched feedback |
| DCOM | Output only with feedback from Sum-D |
| DREG | Output only with D-type registered feedback from Sum-D |
| DLAT | Output only with D-type latched feedback from Sum-D |

The parameters DCOM, DREG and DLAT are only applicable for PA7140 and PA7128 devices.

Assigned_LCC — The LCC that is connected to the current IOC.

## Parameters for the LCC Format (PEEL Arrays only)

Cell_number

The cell number that is assigned to the current Logic Control cell. It ranges from 1A-6A, 1B-6B, 1C-6C and 1D-6D. Figure 5-4 illustrates the cell number organization for the PA7024 device.

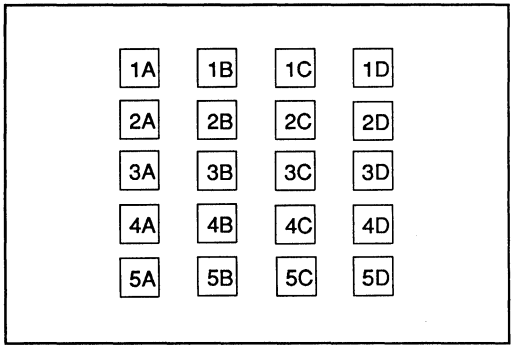


Figure 5-4, LCC numbering system in PA7024

| Device | LCC Assignments |
|---|---|
| PA7024 | 1A-5A, 1B-5B, 1C-5C, 1D-5D |
| PA7140 (PLCC) | 1A-6A, 1B-6B, 1C-6C, 1D-6D |
| PA7128 | 1A-3A, 1B-3B, 1C-3C, 1D-3D |

Refer to the IOC statement described in the previous section for the assigned IOC for each LCC.

*Cell_label*

Refer to section 5.6 for the cell label format.

Flip-flop type

Specifies the type of register in the LCC. The dynamic register type setting (RT signal) is also specified in this parameter. The RT signal which comes from the Global Cell dynamically changes the register type in the LCC during normal (5V) operation.

| Identifier | Function |
|---|---|
| D | D-type register (RT mode is disabled) |
| T | T-type register (RT mode is disabled) |
| JK | JK-type register (RT mode is disabled) |
| DT | D-type register when RT= FALSE,<br>T-type register when RT = TRUE |
| DJK | D-type register when RT = FALSE,<br>JK-type register when RT = TRUE |
| TD | T-type register when RT = FALSE,<br>D-type register when RT = TRUE |
| JKD | JK-type register when RT = FALSE,<br>D-type register when RT = TRUE |

5

Clock — Controls the type of clock for the current LCC.

| Identifier | Function |
|---|---|
| POS | High speed (system) clock from pin 1 or 13 that triggers the register on the rising edge. Note: Global cell controls which pin to use for system clock |
| NEG | Register is triggered on the falling edge of the system clock |
| SumC | Local clock coming from the Sum C term. Register is triggered on the rising edge of the clock signal |
| SumD | Local clock coming from the Sum D term. Register is triggered on the falling edge of the clock signal |

Buried_Out — Output of the LCC that is fed back internally to the array.

| Identifier | Function |
|---|---|
| Reg | Internal output from the output of the register |
| SumA | Internal output from the Sum A term (i.e. the input of the register) |
| SumB | Internal output from the Sum B term |
| SumC | Internal output from the Sum C term |

Ext_Out — Output of the LCC which is connected to the I/O cell. This output sends the signal of the device to the outside world. The final output signal depends on the output polarity of its assigned IOC.

## Parameters for the IOC Format (PEEL Devices)

Pin_Number — The pin number that is assigned to the current I/O cell. Below lists the PEEL I/O pin numbers.

| Device | I/O Pin Numbers |
|---|---|
| PEEL18CV8 | 12 - 19 |
| PEEL173, PEEL273, PEEL20CG10, PEEL22CV10, PEEL22CV10A, PEEL22CV10A+, PEEL22CV10Z | 14 - 23 |

*Pin_Label* — See section 5.6 for the format of the I/O pin label.

Output_pol — This parameter which refers to the output polarity of the pin is controlled by the following identifiers:

| Identifier | Function |
|---|---|
| POS | Positive Polarity for the Output |
| NEG | Negative Polarity for the Output |

The output polarity "bubble" in the PLACE architectural software controls this parameter. Inserting the / or ! character in the pin_label does not affect the output (section 5.6). Hence, only this parameter controls the polarity of the output.

Pin_type

The identifiers for the pin type parameter are:

| Identifier | Function |
|---|---|
| COM | I/O with combinatorial output |
| REG | I/O with D-type registered output |
| OUTCOM | Combinatorial output only |
| OUTREG | Registered output only |
| IN | Output disabled (May or may not be an input depending on the feedback type) |

Note that only the PEEL18CV8, 20CG10, 22CV10, 22CV10A, 22CV10A+ and 22CV10Z have output registers. The REG and OUTREG are not applicable for PEEL173 and 273 devices.

Feedback_type

Specifies the type of feedback for the selected device. This parameter is only applicable for devices such as PEEL18CV8, 20CG10, 22CV10A+ and 22CV10Z. The feedback types of the PEEL22CV10 and 22CV10A are automatically set to FEED_PIN and FEED_REG for COM and REG output types respectively. Only FEED_PIN feedback type is available in the PEEL173 and 273 devices.

| Identifier | Function |
|---|---|
| FEED_PIN | Feedback from the pin |
| FEED_REG | Feedback from the output of the register |
| FEED_OR | Feedback directly from sum term (i.e. prior to the register) |

# 5.8 Global Configurations

## PEEL Arrays

The global configurations for PEEL Arrays are used to set up the global signals for the LCCs, IOCs and INCs.

**Format:**

```
Global = n                                  "n = 1 or 2 cells
GBC (A  LCC_clock  IOC_clock)               "Global Cell A
GBC (B  LCC_clock  IOC_clock)               "Global Cell B
GBC (C  ___  INC_clock)                     "Global Cell C
                                            "(PA7140 and
                                            "PA7128 only)
```

Example:

```
Global = 1
GBC (A  Clk1  Clk2)
GBC (B  Clk1  Clk2)
GBC(C  ___  Clk1)
```

Table 5-2 shows the definitions of the Clk1, Clk2 and PClk terms used in the GBC configuration statements.

**Clk1 and Clk2 terms** - specify the system clock pin to use.

| Device | Clk1 pin | Clk2 pin |
|---|---|---|
| PA7024 | 1 | 13 |
| PA7140 (PLCC) | 2 | 24 |
| PA7128 | 1 | 28 |

**PClk terms** - specify to use the product term for the global clock.

| Device | IOCs by PClkA | IOCs by PClkB | INCs by PClkC |
|---|---|---|---|
| PA7024 | 2 - 11 | 14 - 23 | none |
| PA7140 (PLCC) | 6 - 16, 18 | 28 - 38, 40 | 3-4, 19-21, 25-27, 41-44 |
| PA7128 | 15 - 20, 22 - 27 | | 2-6, 8-16 |

Table 5-2, Definitions of global clock terms

Global = n — The **n** parameter equals 1 or 2. This paramter sets the number of global cells to be used for the LCCs and IOCs. If one global cell is used, then global cell A controls the global signals for all LCCs and IOCs in the device and global cell B configuration statement is ignored . If "Global = 2" is specified, then Global Cell A controls the global signals for the IOCs and LCCs in which the IOCs are on the left side of the device. Global Cell B then controls the global signals for the IOCs and LCCs in which the IOCs are on the right side of the device. See Table 5-2.

Below are the descriptions of each parameter in the GBC (GBC A, B or C) configuration statements.

LCC_clock — Sets the system clock pin for the LCC global clock. The two options available are the **Clk1** and **Clk2** pins. Refer to Table 5-2 for the Clk1 and Clk2 pin numbers for each PEEL Array.

IOC_clock — Sets the system clock pin or product term for the IOC global clock. The options available are **Clk1, Clk2**, and **PCLKA or PCLKB.** See Table 5-2.

INC_clock — Sets the system clock pin or product term for the INC global clock. The options available are **Clk1, Clk2** and **PCLKC**. See Table 5-2.

## PEEL Devices

In the registered PEEL devices such as PEEL18CV8, 20CG10, 22CV10, 22CV10A, 22CV10A+ and 22CV10Z, the global configurations are represented by the global node assignments. These global nodes control the asynchronous reset and synchronous preset product terms.

**Format:** *node_label* **NODE** node_number

Example: AC node 21 "For PEEL18CV8 device

*node_label* — Please refer to section 5.6 for the node label format.

node_number — The node assignment numbers for the selected device are:

| Device | Node Number | Function |
|---|---|---|
| PEEL18CV8 | 21 | Asynchronous Reset |
| | 22 | Synchronouse Preset |
| PEEL20CG10, PEEL22CV10, PEEL22CV10A, PEEL22CV10A+, PEEL22CV10Z | 25 | Asynchronous Reset |
| | 26 | Synchronous Preset |

## 5.9 Comments

In the PLACE software, comments are available so that each component of the design which may not be readily apparent from the source file is explained. Comments do not affect the design itself. Liberal use of comments can make a PSF design file easy to understand.

**Format:** " *Insert comments here ...*

Example: "Enable security bit programming

A comment begins with a double quotation mark (") and ends with the end of line. A comment can be specified anywhere in the PSF design file.

☞ Note that the double quotation marks are not required if the comments are specified within the **"DESCRIPTION"** and **"END_DESC"** reserved identifiers.

## 5.10 Macro Definitions

The macro definitions are used for:

- declaring constants so to make the design easier to understand.
- declaring commonly used equations so that they need not be repeated throughout the design file.
- assigning the state cells and set variables for state diagram designs.
- assigning the pins or cells for truth table designs.

The macro definitions in the PSF design file are located after the reserved identifier **DEFINE** but prior to one of the following

reserved identifiers: **STATE_DIAGRAMS**; **TRUTH_TABLE**; or **EQUATIONS** (whichever is specified first). Macro definitions that are specified via the "Macro" function in the Design operation are automatically inserted into this location.

**Format:** **DEFINE**
*specify macro definitons here...*

**STATE_DIAGRAMS**, **TRUTH_TABLE** or **EQUATIONS**

Example:

```
DEFINE
QSTATE = [ADD10 SUB10 Q2 Q1 Q0]   "State_Diagram  Assignment
Clear      = ^B00000              "Constant Declaration
ShowHit    = ^B00001
AddCard    = ^B11011
Add_10     = ^B10010
Wait       = ^B00010
Test_17    = ^B00110
Test_22    = ^B00111
ShowStand  = ^B00101
ShowBust   = ^B00100

is_Ace = !V4 & !V3 & !V2 & !V1 & V0;   "Equation Declaration

SCORE = [S4 S3 S2 S1 S0]          "Truth table input assignment
BCD2  = [D5 D4]                   "Truth table ouput assignment
BCD1  = [D3 D2 D1 D0]             "Truth table output assignment

STATE_DIAGRAM  QSTATE             "Ends the Macro Definitions
```

## Macro Constants

**Format:** *Const_label* = *constant*

Examples:
```
Clear   = ^B00000
ShowHit = ^B00001
```

*Const_label* The format for the label of the constant is similar to that of the pin or cell label (see section 5.6) with two exceptions, and they are:

1. The length of the label can be up to 20 characters long instead of 8.
2. The / or ! character cannot be used at the beginning of the label.

*Constant*

Specifies the value of the constant in decimal, hexadecimal, octal or binary numbering system.

The format for the constant is:

symbol + number

The symbols for the numbering systems are:

| Numbering system | Symbol |
|---|---|
| Decimal | none (default) |
| Hexadecimal | ^H or ^h |
| Octal | ^O or ^o |
| Binary | ^B or ^b |

Examples: 15 (decimal)
^HF (hexadecimal)
^O17 (octal)
^B1111 (binary)

## Macro Equations

**Format:** *Eqn_label* = *complex_eqn*

Example: Is_ACS = !V4 & !V3 & !V2 & !V1 & !V0;

*Eqn_label*

The label for the equation macro is similar to that for the label for the macro constant. See previous section.

*Complex_eqn*

Macro equation can be specified using the logic operators (), !, &, # and $ (refer to section 5.13).

The input side of a macro equation (i.e. the right side of the "=" symbol) is made up of pin or cell labels, or labels from other macro equations. Below is an example of a macro equation which is a function of other macro equations.

```
DEFINE
  Mac1 = A & B;          "Macro  level 1
  Mac2 = C # D;          "Macro level 1
  Mac3 = Mac1 $ Mac2;    "Macro level 2
```

If the macro equation uses only pin and/or cell labels, then it has one macro level. If it uses **previously defined** macro equation labels in addition to the pin and cell labels, then it has multiple macro levels. The number of macro levels depends on whether the macro equation labels used in the

equation are functions of more macro equation labels themselves.

The number of macro levels is limited by the total number of characters (**maximum of 1024 characters**) in the "flattened" macro equation, i.e. the input side of a flattened macro equation consists of only pin and/or cell labels. Note that the additional spaces between the input variables in the macro equation are automatically deleted by the PLACE Compiler. Example: A maximum of 5 macro levels can be used if each (unflattened) equation level has less than 200 characters. **Typically, the maximum macro level is about ten.**

## Macro State Cell Assignments for STATE DIAGRAMS

The state cell assignment defines the pin or cell labels to be used by the state diagram design syntax.

☞ The **"Allocate"** command in the "Design" menu window of the Design operation automatically generates the state cell assignment definition and STATE_DIAGRAM design syntax. An example is shown below.

```
DEFINE
QSTATE = [ADD10  SUB10  Q2  Q1  Q0]

STATE_DIAGRAM  QSTATE
 "enter design here ...
END;
```

**Format:** *state_label* = [Cell1 Cell2 Cell3 ... Celln]

Example: QSTATE = [ADD10 SUB10 Q2 Q1 Q0]

*State_label* — The state label format is similar to that of the pin or cell label (section 5.6). The only exception is that the state label does not allow the use of the / or ! character at the beginning of the label.

Cell(n) — Specifies the cell labels to be used as state cells by the state diagram. A maximum of 24 cells can be allocated as state cells. Each state cell label must be separated by a space. The most and least significant bit of the state cells are the first and last al-

located cells respectively in the cell assignment definition, i.e. Cell1 is the Most Significant Bit and Celln is the Least Significant Bit.

## Macro Set Variables in State Diagrams

Outputs in a state diagram can be assigned to a set variable so that the logic of these outputs can be specified with a numeric constant. The constant can be specified in a binary, octal, hexadecimal or decimal (default) numbering system.

**Format:** *set_var = [Cell1 Cell2 Cell3 ... Celln]*

Example:

```
DEFINE
TEST = [T2  T1]              "State cell assignment
OUT = [Y3  Y2  Y1  Y0]       "Set variable assignment

STATE_DIAGRAM  TEST
 State 0:    OUT = 0;        "Macro Set variable OUT
                             "Y3-0 = 0000
             Goto 1;
 State 1:    OUT = ^HB;                  "Y3-0 = 1011
             Goto 2;
 State 2:    OUT = ^B1100;               "Y3-0 = 1100
             Goto 3;
 State 3:    Goto 0
END;
```

*Set_var* The format is similar to the state label format used for the state cell assignments.

*Celln* Specifies the assigned pin or cell label.

The macro set variable equation feature is only available within the state diagram design syntax. Also, **only one macro level is available in the macro set variable assignment.**

## Macro Cell Allocation for Truth Tables

The **"Allocate"** command in the PLACE Design operation can also be used to allocate the pins and cells for the truth table design. The pins and cells can be allocated as truth table inputs, truth table outputs or both. If a cell or pin is allocated as the truth table input and output, then it is an I/O. The output of the I/O is then enabled or disabled via the .OE equation.

The following example shows the allocation of the pins and cells for the truth table design "TABLE1".

```
Example:    TRUTH_TABLE  TABLE1
            (I4 I3 I2 I1 I0 -> Y5 Y4 Y3 Y2 Y1 Y0)
            END;
```

Another method of allocating the pins and cells is through the macro set variable method. The inputs and outputs of the truth table can be assigned to the macro set variables in the DEFINE section. The labels of these macro set variables are then used in the truth table design syntax instead of the pin and cell labels.

**Format:** *table_label = [Cell1 Cell2 Cell3 ... Celln]*

```
Example:    DEFINE
            Input = [I4 I3 I2 I1 I0];
            Y_HiBit = [Y5 Y4];
            Y_LoBit = [Y3 Y2 Y1 Y0];

            TRUTH_TABLE TABLE1
            (Input -> Y_HiBit Y_LoBit)
            ^H15 ->   1       ^HA   "I4-0 = 10101, Y5-0 = 011010
            ^H16 ->   1       ^HB   "I4-0 = 10110, Y5-0 = 011011
            END;
```

*Table_label* The format is similar to the state label used for the state cell assignments.

*Celln* Specifies the assigned pin or cell label.

Please refer to section 5.12 on "Truth Table Design Syntax" for more information.

## 5.11 State Diagrams

The state diagram language is used to implement state machine designs. In the PLACE software, the state machine design is specified between the **"STATE_DIAGRAM *state_label*"** and **"END"** identifiers. These identifiers together with the state cell allocation definition (refer to section 5.10) are automatically created when the LCCs or IOCs are allocated for the state machine via the **"Allocate"** command in the Design operation.

**Format:**

```
DEFINE
State_label = [Cell1 Cell2 ... Celln]

STATE_DIAGRAM State_label
  STATE state_0: "usually Reset state
  STATE state_1:
     .
     .
  STATE state_n: "last state
END;
```

*State_label* The state label format is similar to that of the pin or cell label (see section 5.6). The only exception is that the state label does not allow the use of the / or ! character at the beginning of the label.

Celln Specifies the cell labels to be used as state cells by the state diagram. A maximum of 24 cells can be allocated as state cells. Each state cell label must be separated by a space. **The most and least significant bit of the state cells are the first and last allocated cells respectively, i.e. Cell0 and Celln are MSB and LSB respectively.**

*State_n* Specifies the state number which can be in the form of a numeric value or a constant label defined in the DEFINE section. Refer to "Macro Constants" in section 5.10.

The PLACE state diagram syntax includes:

- **GOTO**
- **IF-THEN-ELSE**
- **CASE-ELSE-ENDCASE**
- **WITH-ENDWITH;**
  (used in conjunction with GOTO, IF-THEN-ELSE and CASE-ELSE-ENDCASE)

## GOTO

**Format:** **GOTO** *state_num*;

Examples: GOTO ShowHit; or
GOTO ^B00001;

*State_num* Specifies the state number for the unconditional jump. A numeric representation of the state or a constant label defining the numeric value in the macro definition section can be used to indicate the state number.

The GOTO statement is used to unconditionally jump to a different state on the next clock edge.

### IF-THEN-ELSE

Unlike the GOTO statement, the IF statement provides a conditional jump to the next state. If the condition is satisfied, the logic jumps to the state specified after the THEN identifier. If the condition is not satisfied, the ELSE state will be the next state.

**Format:** **IF** *condition* **THEN** *state_num1*
**ELSE** *state_num2*;

Example: if (!CARDIN) then AddCard
else ShowHit; "^B00001 can be used
"instead of ShowHit.

*Condition* A boolean expression condition which can be in the form of a macro equation label (see "Macro Equations" in section 5.10).

*State_num1* If condition is satisfied, then jump to this state on the next clock edge.

*State_num2* If condition is not satisfied, then jump to the alternate state.

### CASE-ELSE-ENDCASE

**Format:**

```
CASE
        condition_1: state_num;
        condition_2: state_num;
        .
        .
        condition_N: state_num;
ELSE                    "ELSE is optional
        state_num;
END_CASE;
```

Example:
```
case
  !Bust: ShowStand;
  Bust & !Ace: ShowBust;
  Bust & Ace: Sub_10;      "^B01111 can be used
endcase;                   "instead of the constant label
                           "Sub_10.
```

*Condition_N* The condition must be a boolean expression. It can also be in the form of an equation label defined in the macro definition section (see "Equation Declaration" in Macro Definitions).

*State_num* The number represents the state for the conditional jump.

The CASE statement is simply an IF statement with multiple conditions. It lists a sequence of mutually-exclusive conditions and their corresponding state numbers. If a condition in the list is satisfied, the logic jumps to the corresponding state on the next clock edge. If no conditions are satisfied, then it jumps to the state number specified after the ELSE reserved identifier.

Note that the ELSE identifier is optional. If it is not specified and the conditions in the CASE list are not satisfied, then the next state is dependent on the type of flip-flop that is set up in the state cells. For instance, if the state cells have D-type registers, then the next state will reset to state 0. If the state cells have T-type registers, then it will hold at the current state.

## WITH-ENDWITH

The WITH statement is used in conjunction with the GOTO, CASE-ELSE-ENDCASE or IF-THEN-ELSE statements. It allows outputs to be specified so that they use the same clock edge(rising or falling clock edge dependent on the configuration) that triggers the next state. **It is recommended to use only registered outputs with the WITH statement.**

**Format:**
```
WITH
        registered output equations ...
ENDWITH;
```

Example:
```
if (A & B) then 1 with
        C = IN; "C is a D-type registered output
        D = 1;  "D is a T-type registered output
```

```
                    endwith;
                else 2;
```

In the above example, when the expression (A & B) is true jump to state 1 on the next clock edge. Using the same clock edge, the output C latches the data from the input IN. Also, output D will toggle (since it is a T-type register) on same clock edge. If the condition (A & B) is not satisfied, the logic jumps to state 2 without changing the signals on outputs C and D.

## Register Types of the "allocated" state cells

Prior to entering your state diagram design syntax, the outputs of the allocated LCCs and IOCs must be configured as registered outputs. The type of registers used, whether they are D, T or JK type registers, affect the behavior of the state diagram. An example is shown in Figure 5-5.

```
DEFINE
ST_TEST = [S2 S1 S0]

STATE_DIAGRAM  ST_TEST
  state 0: goto 1;
  state 1: case
             A&B&C: 0;
             A&B&/C: 3;
             /A&/B&/C: 4;
           end;
  state 2: goto 5;
    .
    .
  state 7: goto 0;
END:
```

All conditions in the case statement of state 1 failed. Hence, the equations for the state cells S0, S1 and S2 are:
S0 = 0; S1 = 0; S2 = 0;

Question:
What is the next state?

| **If D-type registers are used for S0, S1 and S3 state cells:** | **If T-type registers are used for S0, S1 and S3 state cells:** |
|---|---|
| Answer:<br>Output of a D-type register follows the input on the next clock edge. Hence after clocking the S0, S1 and S2 registers, the outputs equate to 0 which is the condition of state 0. **So, the state 0 is the next state.** | Answer:<br>Output of a T-type register follows the previous state on the next clock edge if the input is FALSE or "0". Hence after clocking the S0, S1 and S2 registers, the outputs follow the previous state of each register. **So, the state 1 is the next state.** |

Figure 5-5, State diagrams with D and T type registers

## Outputs of the State Diagram

The two types of outputs in the PLACE state diagram are the synchronous and asynchronous outputs.

- **Synchronous Outputs:** These are registered outputs which use the same clock as the state machine. The outputs follow the input data on the next clock edge.
- **Asynchronous Outputs:** These are combinatorial outputs. The outputs follow the input data immediately.

Please refer to Figure 5-6 for the synchronous and asynchronous output examples.

Note that the state diagram outputs must first be configured using the PLACE architectural software. For instance if a registered output is required, the type of flip-flop (D,T or JK) and clock (pin or sum term) must be configured in the LCC/IOC or IOC screen in the Design operation.

The two classes of state machine designs that can be created using the PLACE software are the Mealy and Moore machines. Both of these state machine designs can utilize the synchronous and asynchronous outputs.

### Mealy Machine

A Mealy state machine is defined as having outputs which are a function of two sets of variables:

- the present input conditions
- the present state of the machine

```
Examples:   Me_Reg = INPUT;     "Registered output
            Me_Com = INPUT;     "Combinatorial output
```

### Moore machine

A Moore state machine is defined as having outputs which are strictly a function of the state of the machine.

```
Examples:   Mo_Reg = 0;         "Registered output
            Mo_Com = 0;         "Combinatorial output
```

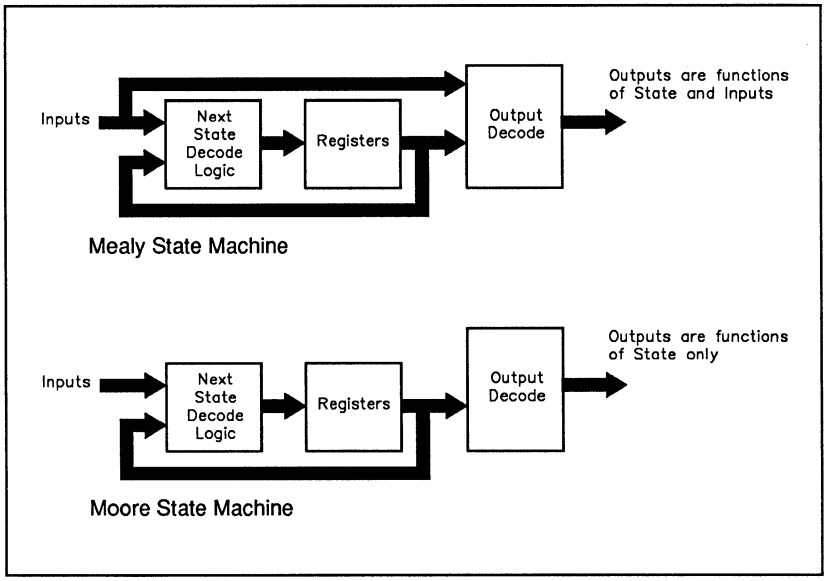


Figure 5-6, Mealy and Moore State Machines

## How the PLACE State Diagram works

Figure 5-7 shows a state diagram example (SDEXAMPL.PSF) using the PLACE state diagram language. This example does not implement any specific application except to illustrate the usage of the state diagram language. The features that are illustrated in the example are:

- GOTO, CASE-ELSE-ENDCASE, IF-THEN-ELSE and WITH-ENDWITH syntax.
- Synchronous and asychronous outputs in Mealy and Moore state machines
- Set Equations for Moore Machine Applications (refer to section 5.10 on "Macro Definitions")

The PLACE Simulate waveforms for the example are shown in Figure 5-8.

5

```
DEFINE

EXAMPLE = [S1 S0]                    "State cell assignment definition
Grp_Out = [OUT3 OUT2 OUT1 OUT0]      "Group outputs assignment

St0 = 0;                             "default - Decimal
St1 = ^H1;                           " ^H   - Hexadecimal
St2 = ^O2;                           " ^O   - Octal
St3 = ^B11;                          " ^B   - Binary

In0 = /I2 & /I1 & /I0                "Input conditions for the State Diagram
In1 = /I2 & /I1 &  I0
In2 = /I2 &  I1 & /I0
In3 = /I2 &  I1 &  I0
In4 =  I2 & /I1 & /I0
In5 =  I2 & /I1 &  I0
In6 =  I2 &  I1 & /I0
In7 =  I2 &  I1 &  I0
In4T06 = In4 # In5 # In6


STATE_DIAGRAM  EXAMPLE
"Goes to STATE St0 upon device power-up (all registers reset on power-up)

   STATE St0:
      Mo_Reg = 0;        "Moore registered output
      Mo_Com = 0;        "Moore combinatorial output
      Grp_Out = 0;       "Moore group combinatorial output, Out3-0 = 0000
      Me_Reg = INPUT;    "Mealy register output
      Me_Com = INPUT;    "Mealy combinatorial output

      IF In1 THEN St1    "If In1=true, then go to STATE St1,
           ELSE St0      "             else remain at STATE St0.

   STATE St1:
      Grp_Out = ^B0110;  "Out3-0 = 0110. These combinational outputs will be valid after the
                         "present state occurs with a single propagation delay (tpd).
      Me_Reg = INPUT;    "This registered output will be valid on the next clock edge,
                         " i.e. clock edge for the NEXT STATE (St0, St1 or St2 depending
                         "on which CASE condition is satisfied).
```

Figure 5-7 PLACE State Diagram Language for SDEXAMPL Design Example

```
    Me_Com = INPUT;   "This combinational output will be valid after the present
                      "state occurs with a single propagation delay (tpd).

    CASE
        /I2 & I1 & /I0: St0          "Go to St0 if (/I2&I1&/I0)=In2=true
                        WITH
                          Mo_Reg = 1; "This output equals to 1 on the next clock edge
                                      "only if the NEXT STATE is St0.
                        ENDWITH;
        In3:            ST2;         "Go to St2 if In3=true
    ELSE
        St1             "If no condition in the CASE list is satisfied, remain at STATE St1.
    ENDCASE;
STATE St2:
    Grp_Out = ^HA;    "Out3-0 = 1010. These combinational outputs will be valid after the
                      "present state occurs with a single propagation delay (tpd).

    IF (In4To6)       THEN St3   "If (In4To6)=true, then go to STATE St3,
        WITH
          Me_Reg = INPUT;        "This registered output will be valid on the next
                                 "clock edge only if the NEXT STATE is St3.
        ENDWITH;
    ELSE
        St2;                     "If (In4To6)=false, then remain at STATE St2.

STATE St3:
    Mo_Reg = 1;       "This output equals to 1 on the next clock edge.
    Mo_Com = 1;       "This combinational output will be valid after the present state
                      "occurs with a single propagation delay (tpd).
    Grp_Out = 0;      "Out3-0 = 0000.
    Me_Reg = 0;       "Reset all Mealy outputs
    Me_Com = 0;

    GOTO St0;         "Go to STATE St0 unconditionally.

END;                  "End of STATE DIAGRAM EXAMPLE
```

Figure 5-7 PLACE State Diagram Language for SDEXAMPL Design Example (Continued)

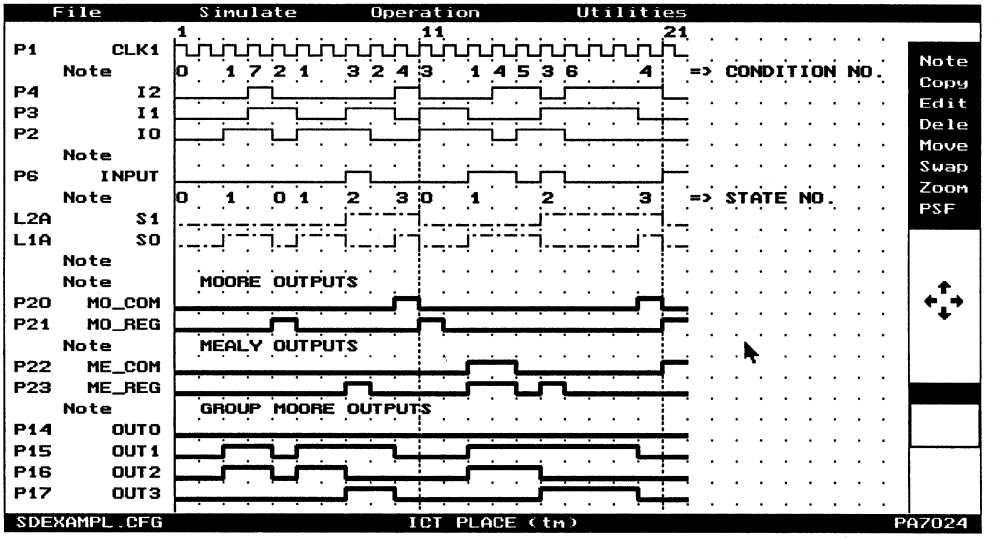


Figure 5-8 Simulate Waveforms for the SDEXAMPL Design Example

## 5.12 Truth Tables

In addition to state diagrams and equations, truth tables can be used to describe the logic designs.

**Format 1:** **TRUTH_TABLE** *table_label*
**(** *In1 In2 ... InN* **->** *Out1 Out2 ... OutN***)** or

**END;**

**Format 2:** **TRUTH_TABLE** *table_label*
**(** *Input* **->** *Output***)**

**END;**

Example 1:

```
TRUTH_TABLE DECODE "3-to-8 Decoder
(C B A -> Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7)
 0 0 0 ->  1  0  0  0  0  0  0  0
 0 0 1 ->  0  1  0  0  0  0  0  0
 0 1 0 ->  0  0  1  0  0  0  0  0
    .
    .
END;
```

```
Example 2: DEFINE
           SCORE = [S4  S3  S2  S1  S0]
           BCD2 = [D5  D4]          "
           BCD1 = [D3  D2  D1  D0]

           TRUTH_TABLE  BIN2BCD  "From JACK7024.PSF
           ( SCORE  ->  BCD2  BCD1)
               0    ->    0     0;
               1    ->    0     1;
               2    ->    0     2;
             .
             .
           END;
```

*Table_label* The format for the label is similar to that for the pin or cell label (section 5.6) with one exception, and that is the / or ! character is not allowed at the beginning of the label.

*InN* (Format 1) Specifies the pin or cell labels to be used as truth table inputs. The inputs can be either registered or combinatorial. **Input data must be in binary (0 or 1) format.**

*OutN* (Format 1) Specifies the pin or cell labels to be used as truth table outputs. Like the inputs, truth table outputs can be either registered or combinatorial. **Output data must be in binary (0 or 1) format.**

*Input*s (Format 2) Specifies a macro defined group of registered or combinatorial pins or cells to be used as truth table inputs. Input data can be in decimal (default), hexadecimal (^H or ^h), octal (^O or ^o) or binary (^B or ^b) numbering system. Only one macro level is available for the macro input set.

*Outputs* (Format 2) Specifies a macro define group of registered or combinatorial pins or cells to be used as truth table outputs. Input data can be in a decimal (default), hexadecimal (^H or ^h), octal (^O or ^o) or binary (^B or ^b) numbering system. Only one macro level is available for the macro output set.

**An additional feature is that both the truth table formats can be used in a single truth table design.**

Alternate truth table description which uses both formats for Example 2 is:

```
TRUTH_TABLE  BIN2BCD
( SCORE ->  D5 D4 BCD1)
    0    ->  0  0   0;
    1    ->  0  0   1;
    2    ->  0  0   2;
   .
   .
END;
```

## 5.13 Equations

The boolean logic equations are the primary methods for specifying logic functions in the PLACE software.

The PLACE architectural software automatically creates the equation for each sum or product term in the cell when it is labeled via the **"Label"** command in the "Design" menu of the Design operation. An example of a newly labeled LCC is shown below.

```
A.D = 0;
A.AP = 0;
A.AR = 0;
A.CLK = 0;
```

**Format:** *Output_label.EXT* = *logic_equation* ;

(The semicolon at the end of the equation is used by the PLACE software to mark the end of the equation when displaying the equation in the Equation Display window. Refer to "PSF Text Display Windows" in section 4.12)

Examples:
```
C1.COM = (V0 & Add10 & Sub10 & S0);
S0.T = (V0 & Add10 & Sub10);
XOR1.COM = A $ B;
XOR2.COM = (!A & B) + (A & !B);
```

*Output_label* This is the pin or cell label that has been entered via the **"Label"** command. Refer to section 5.6 for the format of the label.

*.EXT* The dot extension of the output is automatically appended to the output label by the PLACE software. The type of extension that is appended on each output label depends on the configuration of the pin or cell, the specific function of the product or sum term, and the device type. Refer to Figure 5-9.

*Logic_equation* This is the boolean logic expression that consists of inputs, feedbacks and logic operators. Table 5-3 shows the functions and priorities of the logic operators available in the PLACE software.

| Operator | Logic Function | Priority |
|---|---|---|
| ( ) | Logical organization | 1 |
| ! or / | NOT | 2 |
| & or * | AND | 3 |
| # or + | OR | 4 |
| $ | Exclusive-OR | 5 |

Table 5-3, Priorities of logic operators in PLACE

The output equations can be moved to other locations of the PSF design file as long as they are specified after the reserved identifier **EQUATIONS**. However, the PLACE software operation will be affected if the unused or any other equations generated by the PLACE software are deleted. This means that all equations, whether they are used or unused, are continuously referenced by the PLACE software.

5

### Functions of the Dot Extensions in the equation labels

In the PLACE source file, each of the Dot extensions represents a specific function. Figure 5-9 details the functions of all Dot extensions.

**PEEL Array**

| Sum Term | Dot Extension | LCC Function (unless stated otherwise) |
|---|---|---|
| Sum A | .COM | Combinatorial Internal/External Output |
| | .D | D Input of the Register |
| | .T | T Input of the Register |
| | .J | J Input of the Register |
| | .SumA | Sum A term is unused |
| Sum B | .COM | Combinatorial Internal/External Output |
| | .K | K Input of the Register |
| | .AP | Asynchronous Preset for Register |
| | .SumB | Sum B term is unused |
| Sum C | .COM | Combinatorial Internal/External Output |
| | .CLK | Asynchronous Clock for Register |
| | .AR | Asynchronous Reset for Register |
| | .SumC | Sum C term is unused |
| Sum D | .CLK | Asynchronous Clock for Register |
| | .OE | External Output Enable Control (IOC) |
| | .FB | Buried feedback (PA7140 and PA7128) |
| | .SumD | Sum D term is unused |

**PEEL173/18CV8**
**PEEL20CG10/22CV10/22CV10A/22CV10A+/22CV10Z**
**Devices**

| Prod Term | Dot Extension | Function |
|---|---|---|
| And A | .OE | External Output Enable Control |
| | .AndA or .And | Product (And) A term is unused |
| Sum B | .COM | Combinatorial External Output |
| | .D | D Input of the Register (not applicable for PEEL173 device) |
| | .SumB or .Sum | Sum B term is unused |

**PEEL273 Devices**

| Sum Term | Dot Extension | Function |
|---|---|---|
| Sum A | .OE | External Output Enable Control |
| | .SumA | Sum A term is unused |
| SumB | .COM | Combinatorial External Output |
| | .SumB | Sum B term is unused |

Figure 5-9, Functions of the Dot Extensions in the Equation Labels

## Logic Reduction Compiler Directive (For Equations Only)

A compiler directive is available to prevent redundant terms in the equations from being removed during the logic optimization process. Sometimes redundant terms are intentionally added to avoid race or hazard conditions, especially in asynchronous applications.

**Format:** **@REDUCE ON** or **@R+**

**@REDUCE OFF** or **@R-**

Example:
```
@R-                          "same as @Reduce Off
G_Latch.COM =                "Gated Latch Application
     LAT_EN & LAT_IN
     !LAT_EN & G_Latch
     LAT_IN & G_Latch;       "redundant term to fix hazard
@R+                          "same as @Reduce On
```

@Reduce On — Equations succeeding this directive will be optimized. Redundant terms will be removed from the equations. This is the default condition.

@Reduce Off — All equations specified after this directive will be flattened (i.e. converted to Sum-of-Product equations from complex equations) but not optimized. Redundant terms will be left in the equations.

## Equations of the Outputs used for State Diagrams or Truth Tables

Boolean equations are generated for all pins and cells that are labeled via the **"Label"** command, including those that are specifically used for state diagram or truth table designs. **These equations if they are unmodified do not affect the logic of the state diagrams or truth tables because they always equate to zero.** However, if the equations are modified and they do not equate to zero, then they will be logically ORed with the boolean equations that are transformed from the state diagram or truth table design syntax by the PLACE compiler.

# PLACE Application Examples

6

# 6.0 PLACE Application Examples

## 6.1 Overview

There are several PLACE application examples provided with the PLACE software. All application files included with the PLACE software are listed in Table 6-1.

Some examples provided are to demonstrate the implementation of a variety of standard logic functions such as gates, registers, counters, and etc. To learn the most from these examples, read each file in the Design Operation, review the description and explore the architecture and design entry (equations, state-diagrams or truth-tables) of each file.

For more detailed information on any of the application examples, please select the Document operation to print out the PSF design file or other applicable graphics and text files.

| File Name | Device | Description |
|---|---|---|
| DEMO1A.PSF | PA7024 | Demonstration design for PA7024 which includes Basic Gates and Registers, 8-bit Down Counter, 2-bit State Machine, 4-bit Shift Register and 8-bit Bidirecional I/O Port |
| GATES1.PSF | PA7024 | Basic Gates (part of DEMO1A. |
| REG1.PSF | PA7024 | Basic Registers, 8-bit Down Counter, 2-bit State Machine and 4-bit Shift Register (all are part of the DEMO1A) |
| BI_PORT.PSF | PA7024 | 8-bit Bidirectional I/O Port (part of DEMO1A) |
| COUNTER1.PSF | PA7024 | 8-bit Down Counter with Preset, Reset and Hold (part of DEMO1A) |
| TIMER.PSF | PA7024 | 16-Bit Programmable Clock Generator/Interrupt Timer |
| JACK7024.PSF | PA7024 | Blackjack Machine Example |
| TC7140.PSF | PA7140 | 8-bit Time/Counter |
| ST7128.PSF | PA7128 | 4-Bit State-Machine and 8-Bit Counter |
| V8GATES.PSF | 18CV8 | Basic Logic Gates |
| V8REGS.PSF | 18CV8 | Basic Registers and Latches |
| V8CLKADD.PSF | 18CV8 | Clock Divider Address Decoder |
| V8BUSMUX.PSF | 18CV8 | Bus Programmable 8-to-1 Multiplexer |
| V8FCNTR.PSF | 18CV8 | 8-bit Counter with Function Controls |
| V8CPORT.PSF | 18CV8 | Change-of-State Input Port with Interrupt |
| V8SYNC.PSF | 18CV8 | Synchronization Circuit. |
| PRI173.PSF | 173 | 16-to-4 Priority Encoder |
| V10CNT8.PSF | 22CV10 | 8-bit Up/Down Loadable Counter with Carry-out or Borrow-in |
| PARV10A | 22CV10A | 9-bit Even/Odd Parity Generator/ Checker |
| V10ZPORT | 22CV10Z | Change-of-State Input Port with Interrupt |

Table 6-1, PLACE application examples

## 6.2 DEMO1A.PSF - PA7024

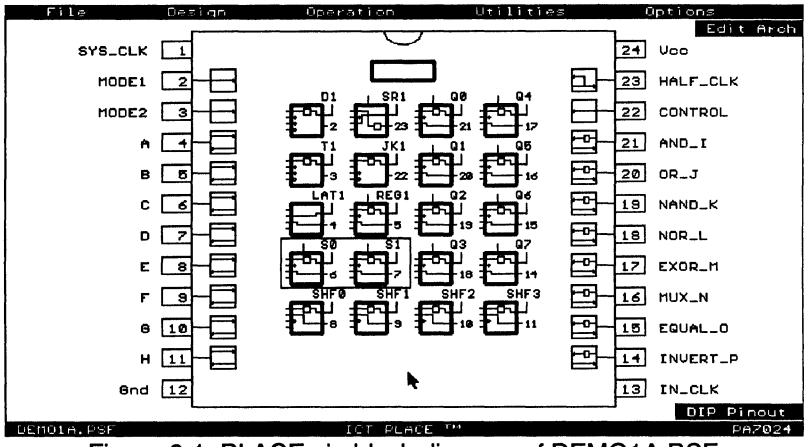


Figure 6-1, PLACE pin block diagram of DEMO1A.PSF

The PLACE design file DEMO1A.PSF incorporates several applications within one design, including: Basic Gates, Basic Registers and Latches, 8-bit Counter, Bi-Directional I/O Port and a Divide-by-2 Clock design. Figures 6-1 and 6-2 show the PLACE pin block and equivalent schematic diagrams.

- **GATES** Basic combinatorial functions including AND, OR, NOR, NAND, EXOR, Inverter, 4-to-1 mux, and 4-bit comparator.
- **REGS** Basic registers including D, T and JK flip-flops with independent clocks, presets and resets, an SR Latch (for debouncing inputs), a gated-latch (LAT1), a basic storage register (REG1), a 2-bit state machine (S0,S1), and a 4-bit shift register (SHF0-3).
- **COUNTER** An 8-bit down counter with Hold, Preset and Reset.
- **PORT** An 8-bit bi-directional I/O port with registered input.

The mode inputs, MODE1 and MODE2, control application selection. Pins names A through H are used as inputs and/or control, pins I through P are used as outputs. The outputs of each application are selected via eight 4-to-1 muxes. Output enable and direction (in PORT mode) are selected by CONTROL. Sections 6.3 through 6.6 describe the individual application in the DEMO1A example.

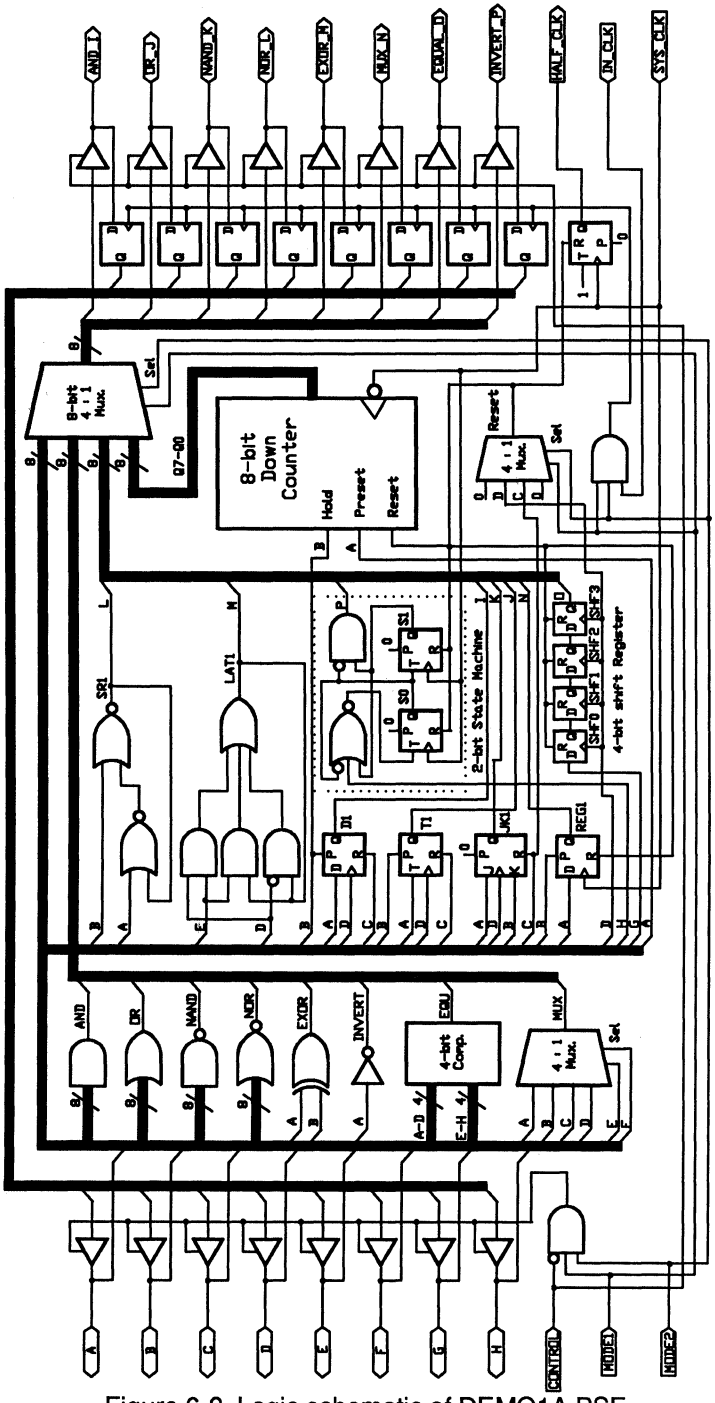


Figure 6-2, Logic schematic of DEMO1A.PSF

## 6.3 GATES1.PSF

This design is one of four main applications that were integrated into a single PA7024 in the DEMO1A application example. As a single application, the basic combinatorial gate functions can be easily reviewed. Included are:

- AND, OR, NOR, NAND gates with 8 inputs (inputs A to H)
- Exclusive-Or gate (inputs A and B)
- 4 to 1 Multiplexor (inputs A,B,C or D selected by E and F)
- 4-bit Comparator (inputs ABCD are compared with EFGH)
- Inverter (input A)

Outputs are labeled with the gate names. The CONTROL pin enables and disables the outputs. Note that very little of the PA7024 is utilized with this example. In fact all 20 buried nodes (with registers), 4 I/0 pins, and 1 input/clock pin, are still available for use.

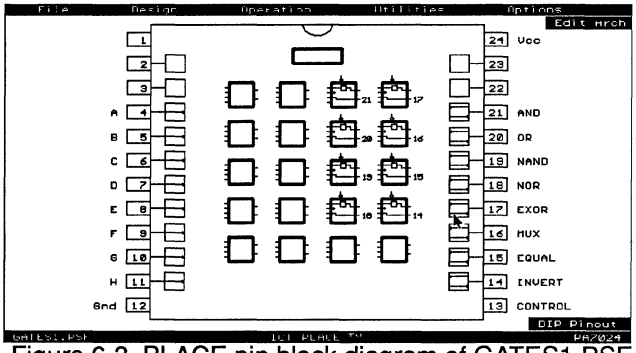


Figure 6-3, PLACE pin block diagram of GATES1.PSF

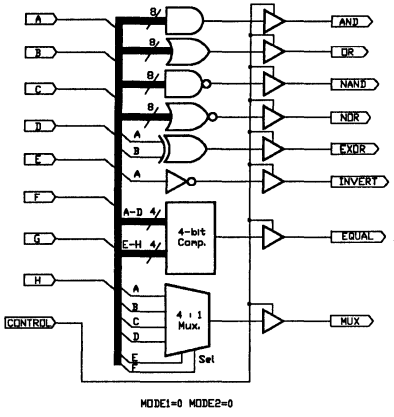


Figure 6-4, Logic schematic of GATES1.PSF

## 6.4 REG1.PSF - PA7024

This design is one of four main applications that were integrated into a single PA7024 in the DEMO1A application example. Basic registers and latches include:

- D, T and JK flip-flops with clock, preset and reset
- SR-latch for debouncing inputs (SR1)
- Gated-latch (LAT1)
- Basic storage register (REG1)
- 2-bit state machine (S0,S1)
- 4-bit shift register (SHF0-3)

In the original DEMO1A application these registers and latches were buried. In this application both the buried path and a direct path have been provided where applicable. The CONTROL input enables and disables all outputs with the exception of the D,T and JK flip-flops.

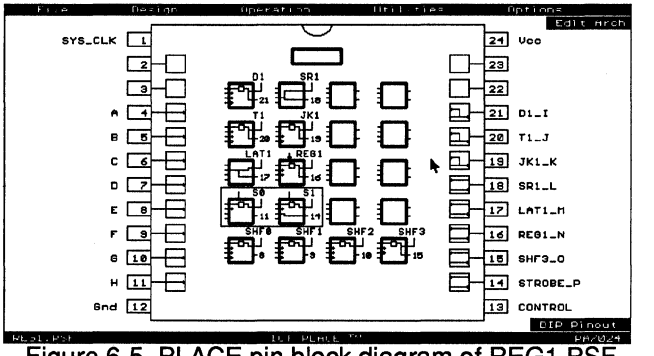


Figure 6-5, PLACE pin block diagram of REG1.PSF

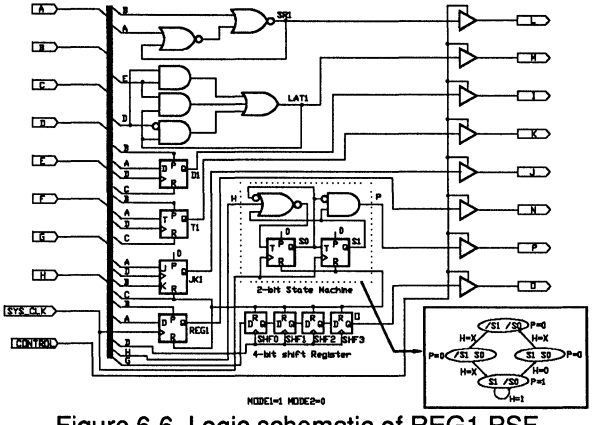


Figure 6-6, Logic schematic of REG1.PSF

## 6.5 BI_PORT.PSF - PA7024

This application example is one of four main applications integrated into a single PA7024 in the DEMO1A example. The bi-directional port application has two eight bit I/O ports grouped as A-H and I-P inputs. The data flow direction of the port is controlled by the CONTROL input. When CONTROL=1, then A-H are inputs and I-P are outputs. When CONTROL=0, I-P are inputs and A-H are outputs. The I-P inputs utilize the transparent input latches which are clocked by the IN_CLK input. Using the many features of the PA7024 there are many alternate ways to design bi-directional I/O ports or dual port interfaces. Note that this application does not use any of the 20 buried nodes or registers, leaving much of the internal PA7024 logic free for use.

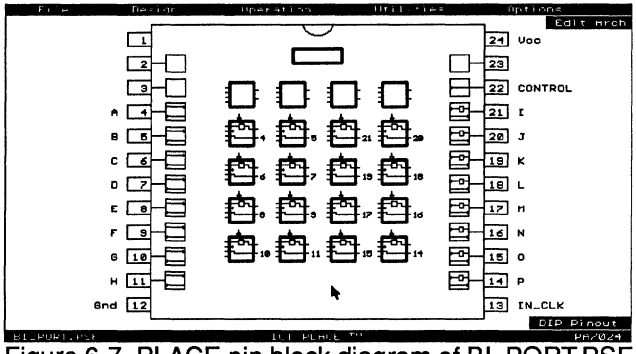


Figure 6-7, PLACE pin block diagram of BI_PORT.PSF

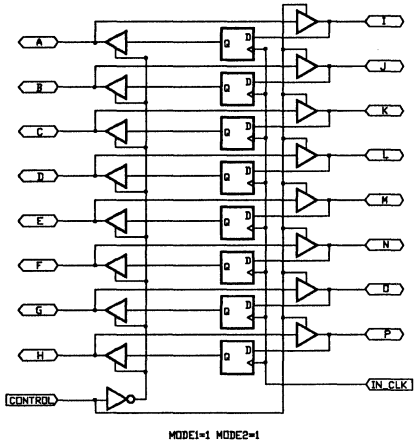


Figure 6-8, Logic schematic of BI_PORT.PSF

## 6.6 COUNTER1.PSF - PA7024

This design is one of four main applications that were integrated into a single PA7024 in the DEMO1A application example. The 8-bit down counter includes preset (A), reset (D) hold (B) and an output enable (Control). The original counter design in DEMO1A is fully buried from I/O pins. In this application both the buried and direct output paths have been provided. Please note that this application uses only a portion of the PA7024. In fact up to a 20-bit buried counter can be implemented.

In addition to the 8-bit counter, a divide-by-2 clock design is also included in the COUNTER1.PSF design file.

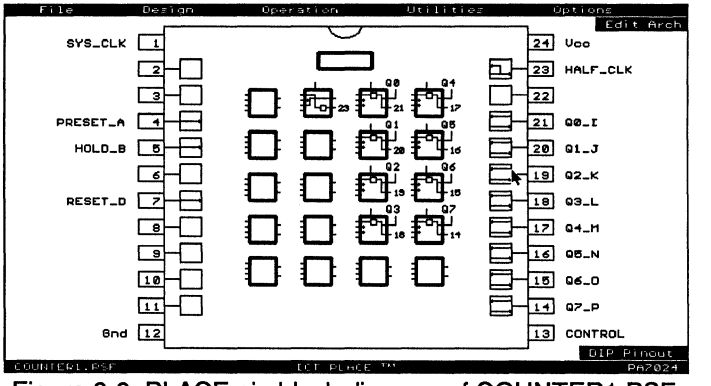


Figure 6-9, PLACE pin block diagram of COUNTER1.PSF

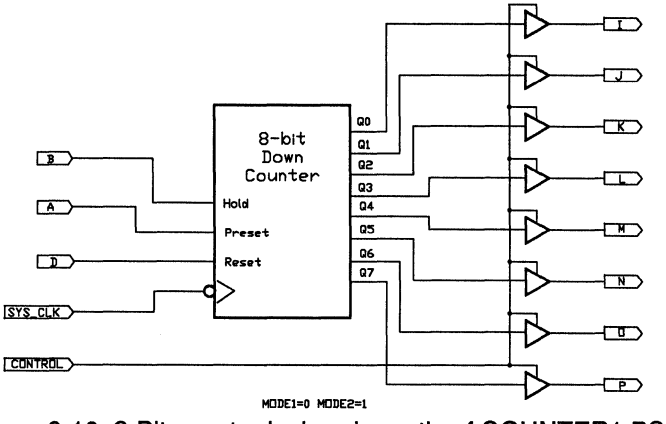


Figure 6-10, 8-Bit counter logic schematic of COUNTER1.PSF

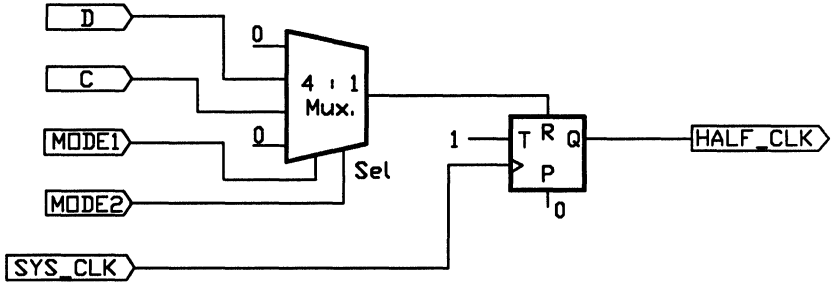


Figure 6-11, Logic schematic of a divide-by-2 clock design in COUNTER1.PSF

## 6.7 TIMER.PSF - PA7024

This application uses the PA7024 to implement a 16-bit programmable clock-generator/interrupt-timer that can be interfaced to a 16-bit microprocessor bus. The CLK input can operate over 50MHz (five times that of conventional programmable counter/timer ICs). A buried 16-bit reloadable down counter is used to divide the high speed input clock.

Upon power-up the counter is disabled. To program the counter, a value must be written into a 16-bit count register from the D0-D15 I/O pins and the counter must be enabled (see Table 6-2 for control). The value in the count register will be loaded into the counter which will count down to 0000 Hex. After reaching 0000 Hex, it will automatically reload the value from the count register. This allows the counter to be free running for clock generation if the value in the count register is maintained. **Note that the "register-type change" feature of the PA7024 global cell is used to dynamically switch the T registers to D registers for loading when the counter reaches the count 0000 Hex.**

If the count register is changed, the new count will be loaded after the count reaches 0000 Hex. One-shot operation for timer controlled interrupts can be implemented by setting the count register to 0000 Hex after the count has been loaded. When this is done, the counter will stop and hold at 0000 Hex.

The OUT pin will toggle (initially low then high and so on) each time the counter reaches 0000 Hex. The counter and OUT pin can be reset, disabled or enabled via a bus command (see table). The count can be read "on the fly" via the D0-D15 pins. The count is temporarily held stable until the read is completed.

| /CS | /RD | /WR | /A0 | Function |
|---|---|---|---|---|
| 1 | X | X | X | Not selected (Don't Care) |
| 0 | 1 | 0 | 0 | Write Count Register from D0-D15 |
| 0 | 0 | 1 | 0 | Read Count Register onto D0-D15 |
| 0 | 1 | 0 | 1 | Reset/Stop Counter and OUT |
| 0 | 0 | 1 | 1 | Enable and Read Counter onto D0-D15 |

Table 6-2, Command table for TIMER.PSF

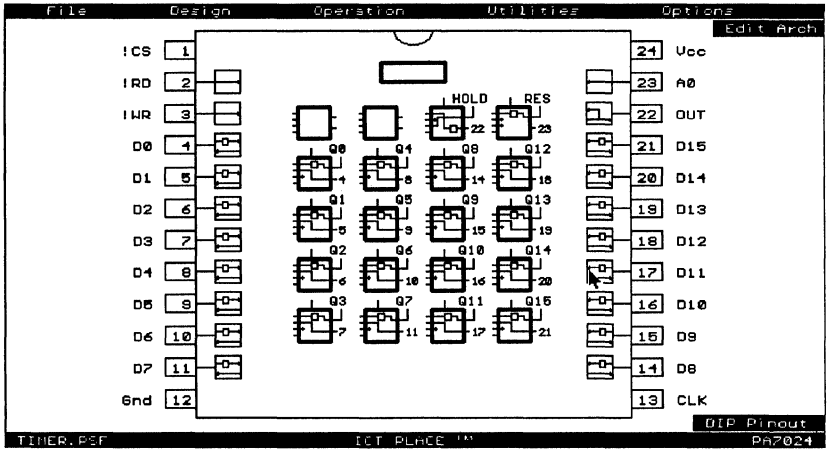


Figure 6-12, PLACE pin block diagram of TIMER.PSF

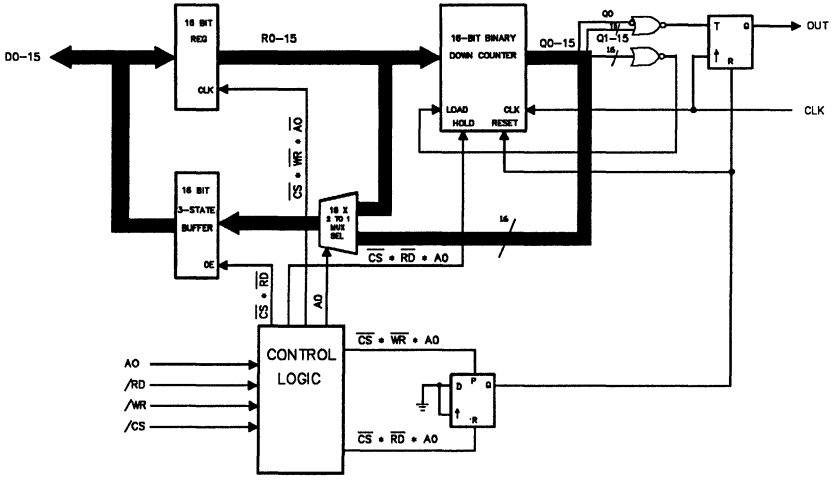


Figure 6-13, Logic schematic of TIMER.PSF

## 6.8 JACK7024.PSF - PA7024

This design example is based on C.R. Clare's design in Designing Logic Systems Using State Machines (McGraw Hill, 1972). The blackjack machine plays the dealer's hand, using typical dealer strategies to decide whether to draw another card (hit) or stand after each round.

The example contains the following logic designs:

- A state machine that controls the game logic which includes:
  - checking the status of the card reader.
  - making the decision of what action to take for a hit, stand or a bust. An example is to draw a card if the hit signal is true.
  - making the decision of when to use the value 1 or 11 for an ace card.
- A Multiplexer/Comparator which compares the point total and sends the hit, stand or bust signal to the state machine. If the point total is greater than 21, it's a bust. If it is equal or less than 16, then hit else stand.
- A 5-Bit Adder that adds the value of the drawn card.
- A Binary-to-BCD converter for converting the 5-bit binary score and converts it to 2-digit BCD for the digital display.

This design example can also be implemented by using three PLDs which include a PAL22V10 for the Multiplexer, Comparator and Adder, a PAL16L8 for the Binary-to-BCD converter, and a PAL16R6 for the state machine.

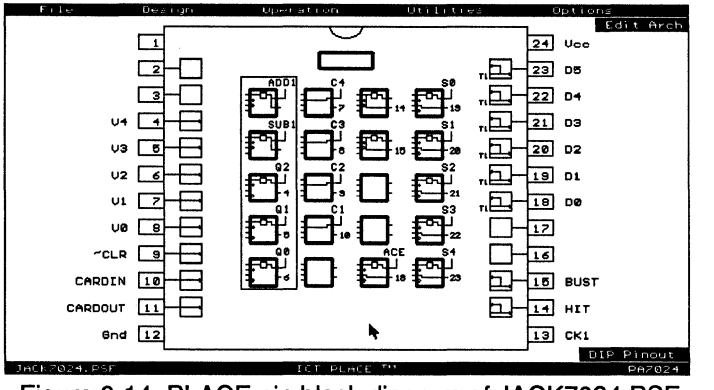


Figure 6-14, PLACE pin block diagram of JACK7024.PSF

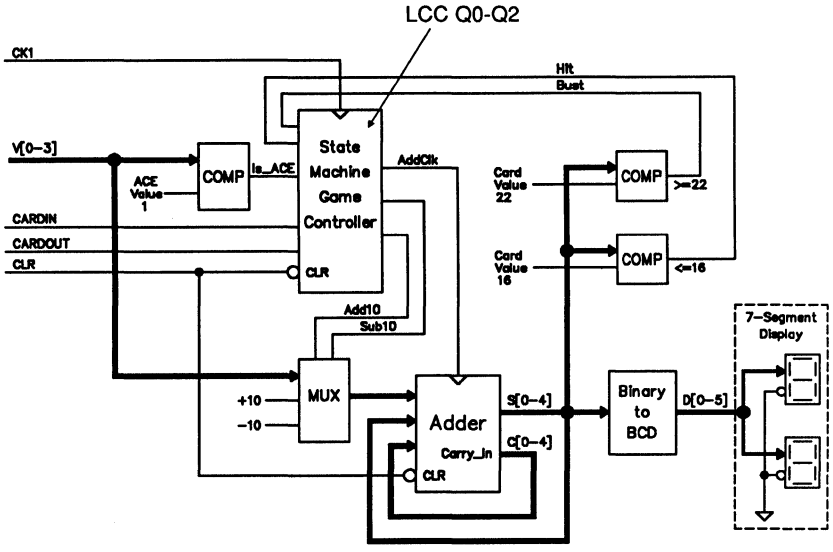


Figure 6-15, Logic block diagram of JACK7024.PSF

## 6.9 TC7140.PSF - PA7140

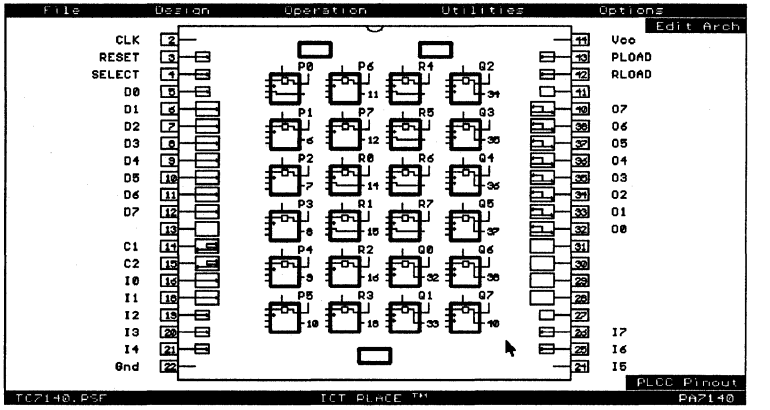


Figure 6-16, PLACE pin block diagram of TC7140.PSF

This example uses a PA7140 device to implement a timer/counter application which is typically used in a microprocessor-based computer system. As shown in Figure 6-17, the circuit employs a multiplexer to allow either the incoming or latched data to be loaded into the counter. The desired data is then loaded into the counter either by reseting the counter and the compare register, or by a match between the counter's state and the value in the compare register.

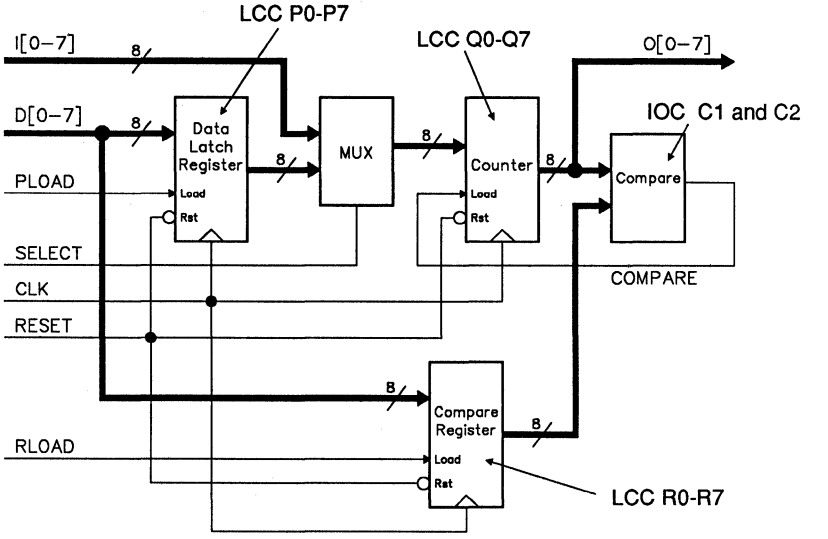


Figure 6-17, Logic block diagram of TC7140.PSF

## 6.10 ST7128.PSF - PA7128

This example implements a 8-bit counter and a 4-bit state machine. The LCCs were allocated for the counter (Q0 - Q7) application. To illustrate the flexibility of the PA7128 I/O Cell (IOC), the state machine (A0 to A3) was implemented by using the buried feedback paths of the IOCs.

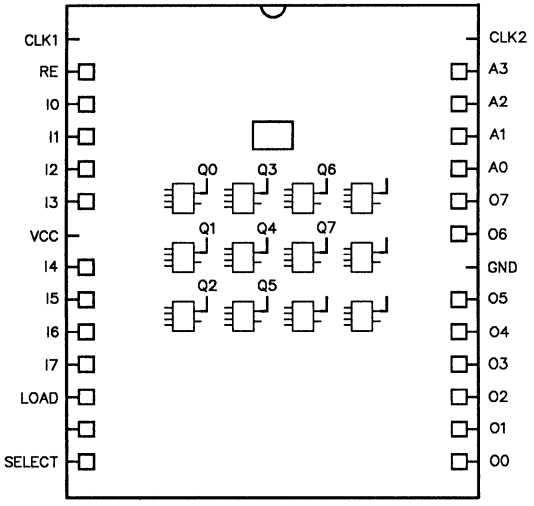


Figure 6-18, Pin block diagram of ST7128.PSF

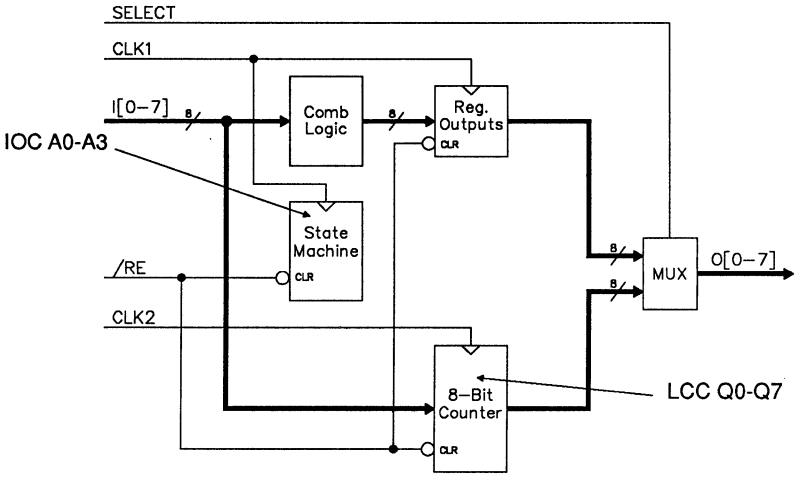


Figure 6-19, Logic block diagram of ST7128.PSF

## 6.11 V8GATES.PSF - PEEL18CV8

This PEEL18CV8 application example implements several basic logic gates. The logic gates include:

- an inverter
- four-input AND, OR, NAND, and NOR gates
- a four-input AND-OR- INVERT gate
- a two- input XOR gate
- a high-impedance buffer.

Each gate uses one or more of the (A,B,C and D) inputs. Additionally, the high-impedance buffer uses the /HZ input for impedance control. The truth table for these gates can be examined in the test vectors. Note, the remaining unused input pins can be used as additional inputs into the gates.

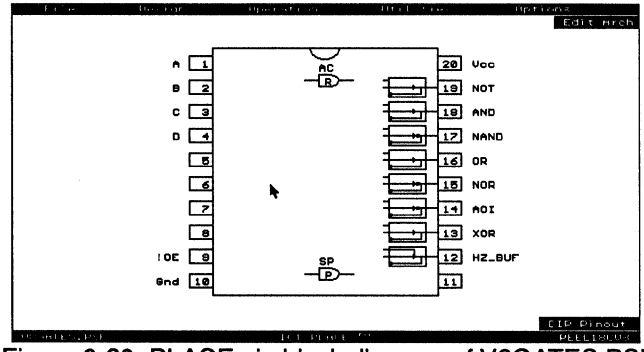


Figure 6-20, PLACE pin block diagram of V8GATES.PSF

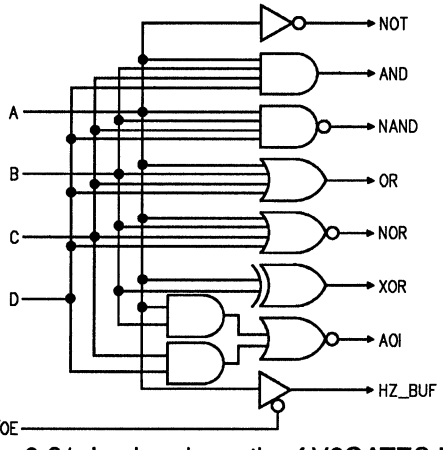


Figure 6-21, Logic schematic of V8GATES.PSF

## 6.12 V8REGS - PEEL18CV8

This application example demonstrates the implementation of several basic registers and latches within a PEEL18CV8. Four register types included are the D, T, JK, and SR, all of which are clocked by the CLK input. All registers can be synchronously reset, set,and asynchronously reset using the SRES, SSET and ARES inputs respectively. Besides the registers, an SR latch and a Gated Latch circuit show how independent asynchronous storage elements can be implemented. Only the Q outputs of these registers and latches are provided at the output pins. The /Q outputs could easily be accessed by inverting the macro cell output polarity. Truth table operation can be referenced via the test vectors.

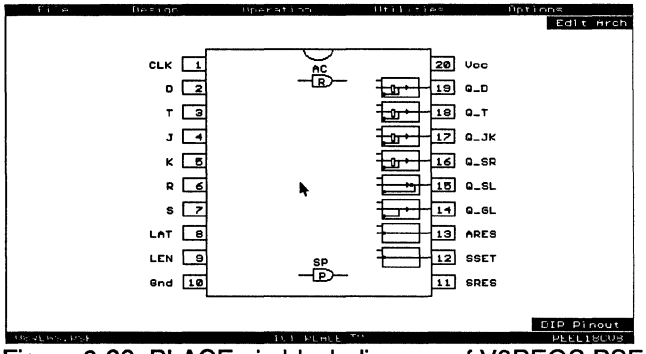


Figure 6-22, PLACE pin block diagram of V8REGS.PSF

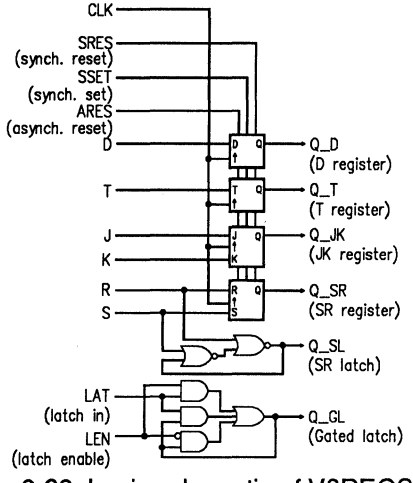


Figure 6-23, Logic schematic of V8REGS.PSF

## 6.13 V8CLKADD.PSF - PEEL18CV8

This application uses the PEEL18CV8 for two common microprocessor system functions: a clock divider and a memory mapped address decoder. The clock divider provides a ÷2, ÷4 and ÷8 clock outputs. The SET input sets all clock outputs high. The address decoder decodes the processor address lines to select one of five memory or I/O devices. The chip select for these devices are active low. The memory map over a 64K boundary is shown below.

Memory Map for Address Decoder

| Function | Address |
|---|---|
| EPROM (32K X 8) | 8000-FFFF Hex |
| EEPROM ( 2K X 8) | 5000-5FFF Hex |
| UART | 4100-41FF Hex |
| PORT | 4000-40FF Hex |
| SRAM ( 8K X 8) | 0000-1FFF Hex |

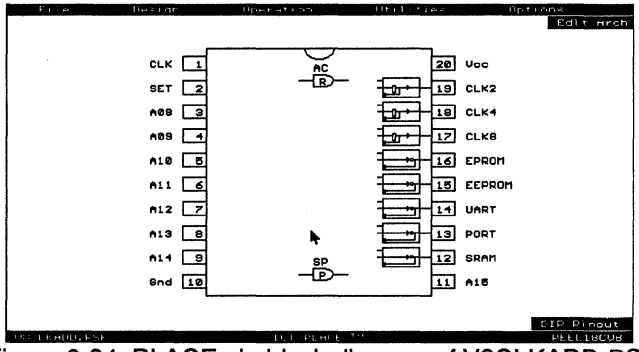


Figure 6-24, PLACE pin block diagram of V8CLKADD.PSF

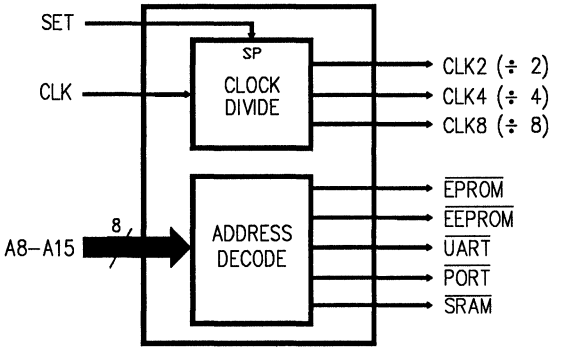


Figure 6-25, Block diagram of V8CLKADD.PSF

## 6.14 V8BUSMUX.PSF - PEEL18CV8

This application implements an 8 to 1 multiplexer that can be interfaced to a µP bus. Any one of the 8 inputs (I0-7) can be selectively routed to the output (OUT) by writing (/WR and /CS =0) a 3-bit binary value to the data inputs (DI0-2). The value is stored into a 3-bit latch that controls the multiplexer selection. Because the latch utilizes internal asynchronous feedback (configuration #8 of the macro cell), the value can also be enabled onto the data outputs DO[0-2]. The DI and DO[0-2] pins should be tied together for write/read bus operation.

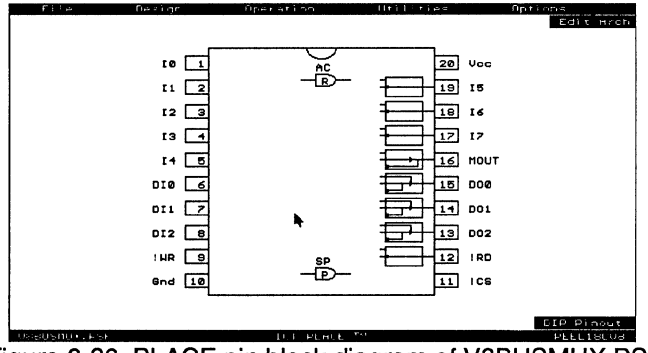


Figure 6-26, PLACE pin block diagram of V8BUSMUX.PSF

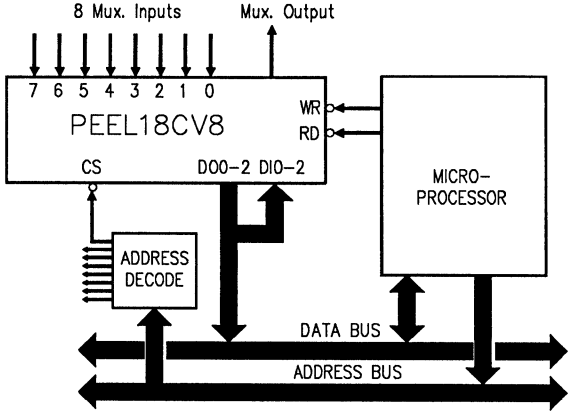


Figure 6-27, Logic schematic of V8BUSMUX.PSF

## 6.15 V8FCNTR.PSF - PEEL18CV8

This application uses the PEEL18CV8 as an 8 bit counter with four control functions: hold, reset, repeat and output enable. The Synchronous Preset term was utilized to free-up a product term from the eighth bit of the counter. This allows the hold function to be implemented.

- SRES (Synchronous Reset): When SRES is set High, the outputs (Q0-7) will go Low after the next clock. When SRES is Low, the counter will start counting up with each clock.
- HOLD (Hold Count): When HOLD is set High the count will hold the present state. When HOLD is Low the counter will resume.
- REP (Repeat Count): When REP is set High, the counter repeats the count after reaching FF Hex. When REP is Low, the counter will stop after one complete count.
- OE (Output Enable): When OE is High, the outputs are disabled (High-Z). When Low, the outputs are enabled.
- (TEST): This input is used to preload the registers to simplify test vector operation.

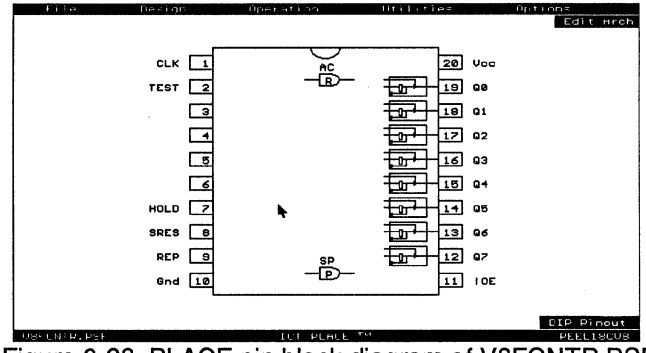


Figure 6-28, PLACE pin block diagram of V8FCNTR.PSF

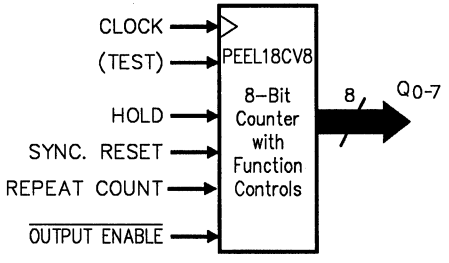


Figure 6-29, Block diagram of V8FCNTR.PSF

## 6.16 V8CPORT.PSF - PEEL18CV8

This application uses the PEEL18CV8 as an 8-bit input port of which 4 of its inputs can detect a change-of-state. When detected, the INTR output is set for interrupting a CPU. The state change is latched by four pseudo-buried registers which can be read by the CPU on D0-D3 as listed in the address table below. Once read, unless another change has occurred, the INTR will be reset. The D4 output can be used for status polling of any remaining state change. The I4-7 inputs do not detect state changes but can be read as a standard input port.

| Address | | | Data Outputs D[0-4] | |
|---|---|---|---|---|
| **A0** | **CS** | **RD** | **D0-3** | **D4** |
| X | 1 | X | Hi-Z | Hi-Z |
| X | X | 1 | Hi-Z | Hi-Z |
| 0 | 0 | 0 | Read I0-I3 Change | I0-I3 Pending Change Status |
| 1 | 0 | 0 | Read I4-I7 Inputs | Don't care |

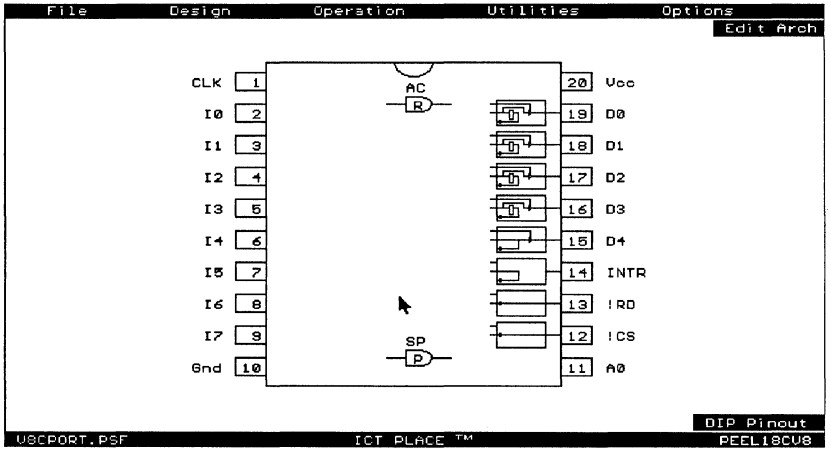


Figure 6-30, PLACE pin block diagram of V8CPORT.PSF

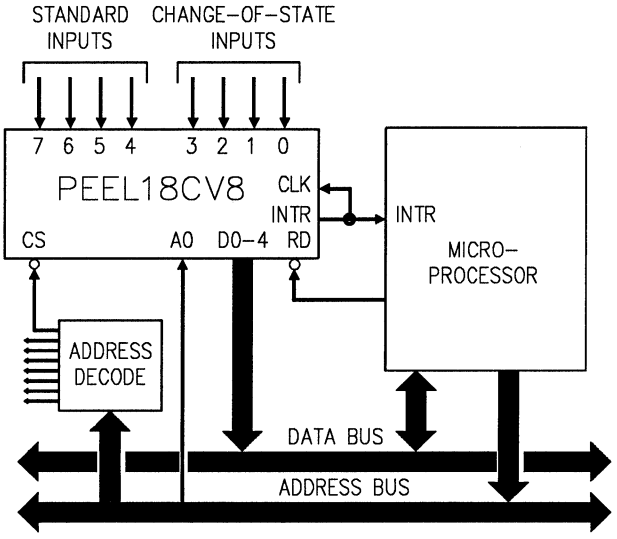


Figure 6-31, System interface block diagram of V8CPORT.PSF

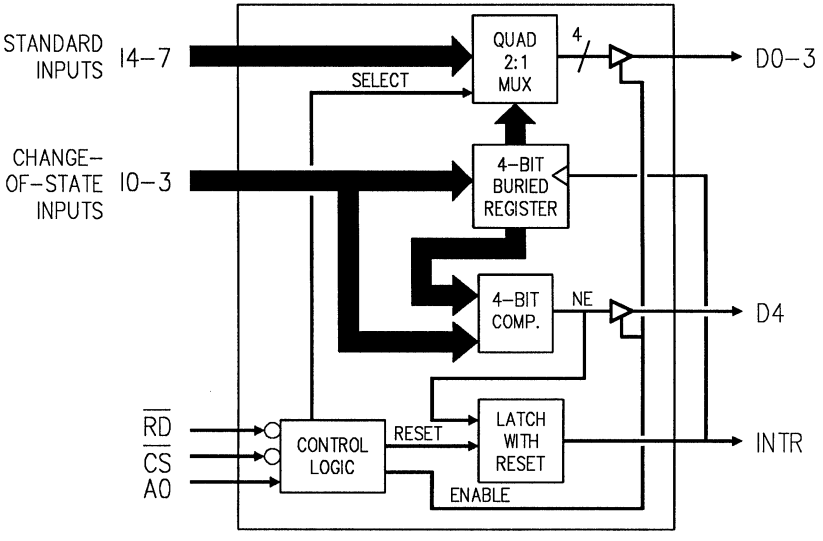


Figure 6-32, Logic schematic of V8CPORT.PSF

## 6.17 V8SYNC.PSF - PEEL18CV8

Digital systems often require synchronization of asynchronous inputs to avoid the potential metastability problems caused by set-up time violation. A common synchronization method uses two rippled 74LS74-type flip-flops (Figure 6-33).

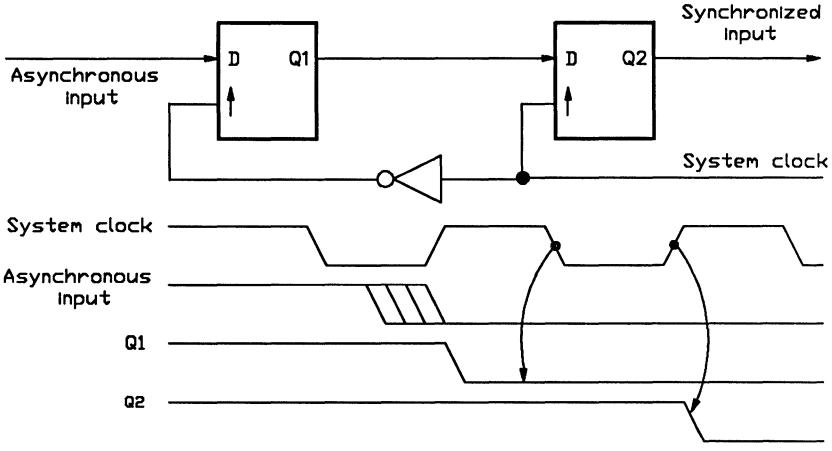


Figure 6-33, A common synchronizer circuit

In this PLACE design example, the PEEL18CV8 utilizes the macro cell configuration #6 (configuration #5 can also be used instead) to implement eight synchronizer circuits as shown in Figure 6-34. In each synchronizer circuit, the gated-latch internally latches the asynchronous input on the falling edge of the clock, generating the signal Q1. ANDing the input Q1 through the internal feedback path eliminates a possible hazard condition during the clock's High-to-Low transition time. The latch then holds Q1 stable to ensure meeting the set-up time requirement of the subsequent D flip-flop which, as before, registers the signal on the next rising edge of the system clock edge. If by chance the input pulse width violates the set-up time of the gated-latch, the clock's Low time will give more time for settling.

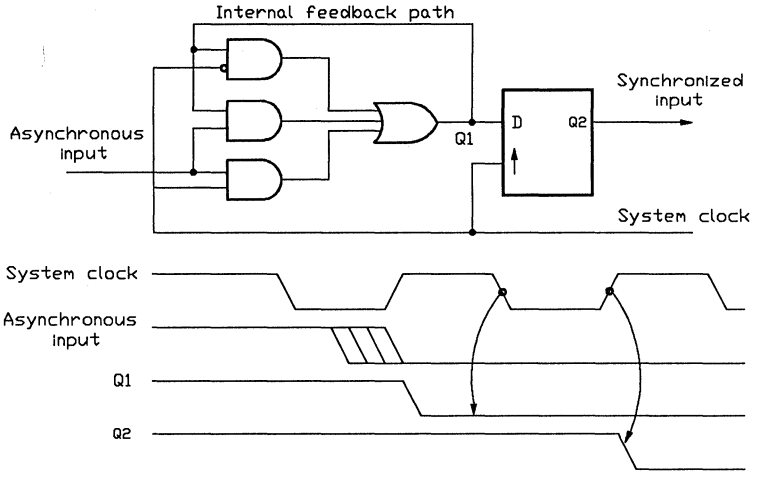


Figure 6-34, Synchronizer circuit in V8SYNC.PSF design

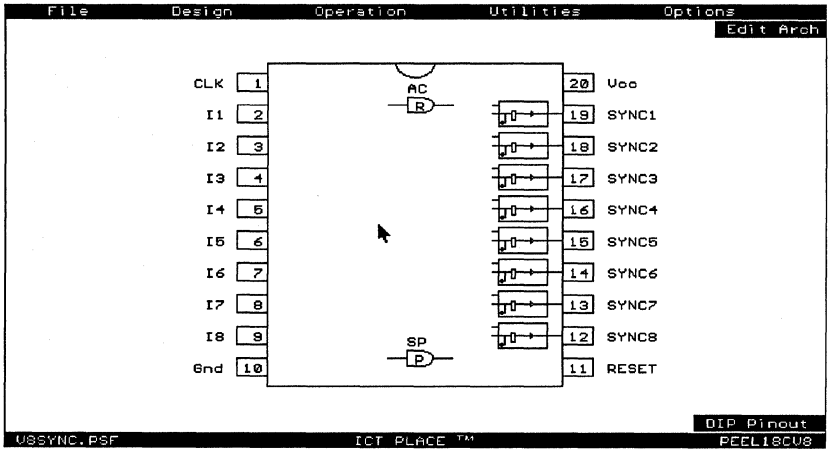


Figure 6-35, PLACE pin block diagram of V8SYNC.PSF

## 6.18 PRI173.PSF - PEEL173

This PEEL173 application implements a 16 to 4 priority encoder with high-impedance outputs. If any D0-DF input goes low, the GS (group strobe) output will go high and the binary value of the highest priority input will be placed on the E0-E3 (Encoded) outputs when enabled by OE (output enable). The D0 input is highest priority and DF lowest. When the E0-E3 outputs are disabled (a function of OE or !GS) they assume a high-impedance state. This makes it possible to interface the encoded outputs onto a system bus where GS might serve as an interrupt line to a uP and OE as the chip select. The high-impedance control also allows multiple PEEL173 priority encoders to be bussed together for creating wider (32, 48 or 64 bit etc.) priority encoders. To add additional encoders, the highest priority OE must be tied low, and the GS must control the next highest priority OE. The multiple GS can be further encoded to identify which device is driving the E0-E3 lines.

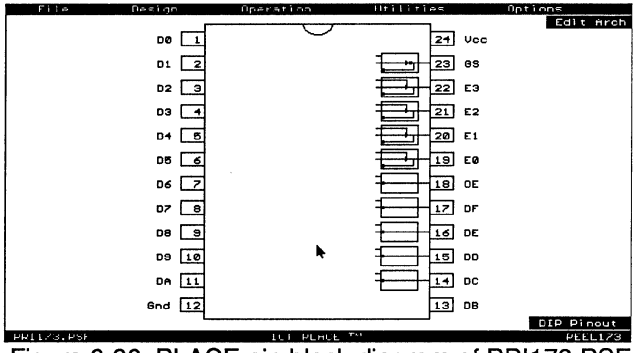


Figure 6-36, PLACE pin block diagram of PRI173.PSF

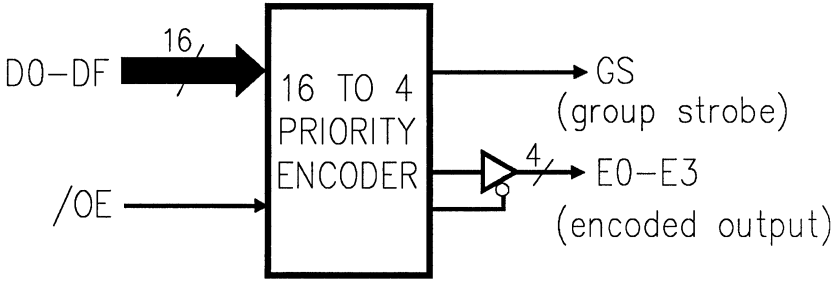


Figure 6-37, Block diagram of PRI173.PSF

## 6.19 V10CNT8.PSF - PEEL22CV10Z

This application uses the PEEL22CV10 as an 8-bit Up/Down Loadable counter. The four controls are:

- CLR (Synchronous Clear)—When CLR is set to High, all outputs (Q7-Q0 and CO_BI) will be set to Low on next clock.
- UP (Up/Down control)—When UP is set to High, outputs Q7-Q0 will count up on each clock. When UP is set to Low, outputs Q7-Q0 will count down.
- LOAD (Load data)—When LOAD is set High, outputs Q7-Q0 will follow the data of D7-D0 on next clock and the output CO_BI will be set to Low.
- !OE (Output Enable)—When OE is set to High, all outputs (Q7-Q0 and CO_BI) will be High Impedance. When OE is set Low, all outputs will be enabled.

Note: After counting up 255, the count will go to 0 and the CO_BI will be set High on next clock. The High will remain on the CO_BI pin until LOAD or CLR goes High.

**Operation Table**

| CLK | CLR | UP | LOAD | !OE | D[7-0] | Q[7-0] | CO_BI |
|---|---|---|---|---|---|---|---|
| C | 1 | X | X | 0 | X | LOW | 0 |
| C | 0 | 1 | 0 | 0 | X | Count up | 0 |
| C | 0 | 1 | 0 | 0 | X | 255 - 0 | 1 carry-out |
| C | 0 | 0 | 0 | 0 | X | Count down | 0 |
| C | 0 | 0 | 0 | 0 | X | 0 - 255 | 1 borrow-in |
| C | 0 | X | 1 | 0 | DATA IN | DATA IN | 0 |
| X | X | X | X | 1 | X | 3-STATE | 0 |

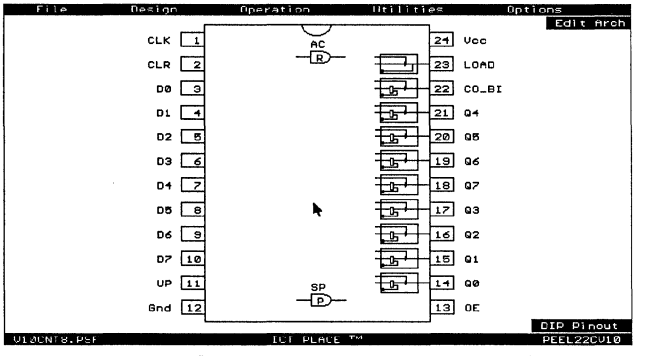


Figure 6-38, PLACE pin block diagram of V10CNT8.PSF

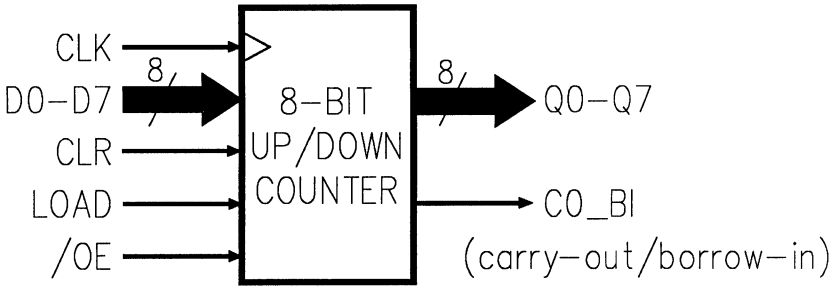


Figure 6-39, Block diagram of V10CNT8.PSF

## 6.20 PARV10A.PSF - PEEL22CV10A

This application uses the PEEL22CV10A as a 9-bit even/odd parity generator/checker.

**Operation Table**

| Number of high inputs A - H | Parity_I | Even_Odd | Parity_O |
|---|---|---|---|
| Even | 1 | 0 | H |
| Odd | 1 | 0 | L |
| Even | 0 | 0 | L |
| Odd | 0 | 0 | H |
| Even | 1 | 1 | L |
| Odd | 1 | 1 | H |
| Even | 0 | 1 | H |
| Odd | 0 | 1 | L |

The parity function is commonly implemented via the utilization of the exclusive-OR operation. To build a N-bit parity generator/checker, the number of 2-input exclusive-OR gates required is N-1. A N-bit parity function can also be implemented via the AND-OR logic operation but it requires $2^{N-1}$ product terms. For instance, a 9-bit parity function will require 256 product terms. Though the PEEL22CV10A device has only 132 product terms, a 9-bit parity function can still be implemented by using two macro cells to implement two 4-bit parity generators. Then, both the outputs of the macro cells are fed back and XORed with the 9th bit (Parity_In). With this method, there is an additional delay due to the feedback of the 4-bit parity generator outputs. If it is implemented in the PEEL22CV10A device, then the delay would be about 3 ns less than if it was implemented in a standard 22V10 device. This is because the outputs in the 22V10 device are fed back from the pin, whereas in the PEEL22CV10A the outputs can be configured to feedback directly from the OR gate (before the output buffer).

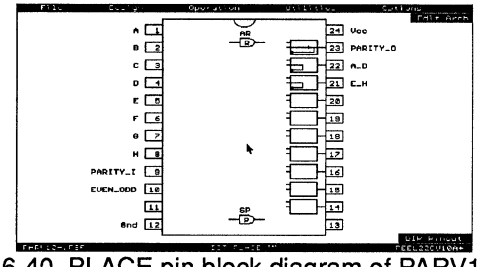


Figure 6-40, PLACE pin block diagram of PARV10A.PSF

## 6.21 V10ZPORT.PSF - PEEL22CV10Z

This application uses the PEEL22CV10Z as an 8-bit input port of which all of its inputs can detect a change-of-state. When detected, the INTR output is set for interrupting a CPU. The state change is latched by eight pseudo-buried registers which can be read by the CPU on D0-D7 as listed in the address table below. Once read, unless another change has occurred, the INTR will be reset. The NEQ output can be used for status polling of any remaining state change. To reduce the average power consumption, the ZERO-POWER mode is used.

| Address | | | Data Outputs | |
|---|---|---|---|---|
| **A0** | **CS** | **RD** | **D0-7** | **NEQ** |
| X | 1 | X | Hi-Z | Hi-Z |
| X | X | 1 | Hi-Z | Hi-Z |
| 0 | 0 | 0 | Read I0-I7 Change | I0-I7 Pending Change Status |

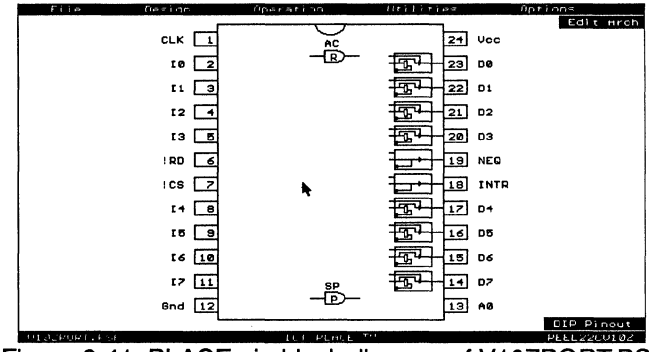


Figure 6-41, PLACE pin block diagram of V10ZPORT.PSF

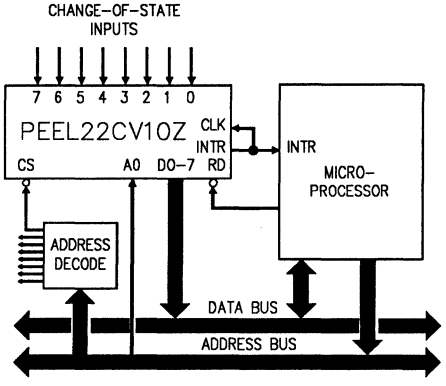


Figure 6-42, System interface block diagram of V10ZPORT.PSF

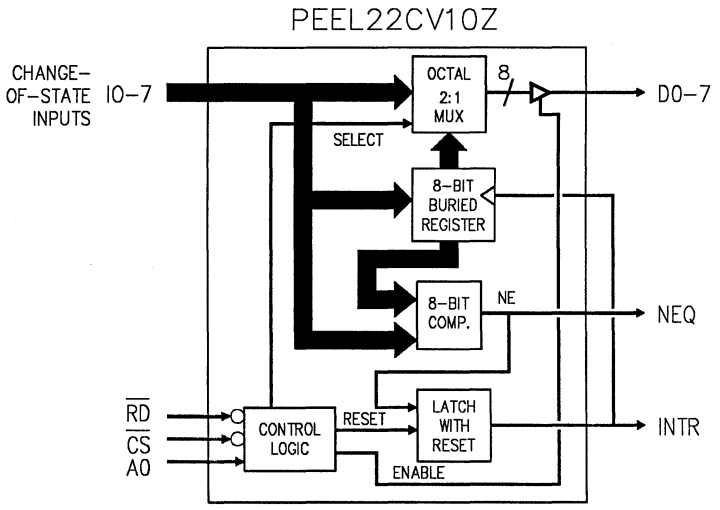


Figure 6-43, Logic schematic of V10ZPORT.PSF

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