5Volt & 3.3Volt

1995 Specialized Memories, FIFOs & Modules Data Book

Integrated Device Technology, Inc.

Integrated Device Technology, Inc.

1995
SPECIALIZED MEMORIES & MODULES DATA BOOK

2975 Stender Way, Santa Clara, California 95054
Telephone: (408) 727-6116 • TWX: 910-338-2070 • FAX: (408) 492-8674
Printed in U.S.A.

GENERAL INFORMATION

CONTENTS OVERVIEW

For ease of use for our customers, Integrated Device Technology provides four separate data books — Logic, Specialized Memories and Modules, RISC and RISC SubSystems, and Static RAM.

IDT's 1995 Specialized Memories and Modules Data Book is comprised of new and revised data sheets for the FIFO, Specialty Memory and Subsystem product groups. Also included is a current packaging section for the products included in this book. This section will be updated in each subsequent data book to reflect packages offered for products included in that book.

The 1995 Specialized Memories and Modules Data Book's Table of Contents contains a listing of the products contained in that data book only. In the past we have included products that appeared in other IDT data books. The numbering scheme for the book is consistent with the 1990-91 data books. The number in the bottom center of the page denotes the section number and the sequence of the data sheet within that section, (i.e. 5.5 would be the fifth data sheet in the fifth section). The number in the lower right hand corner is the page number of that particular data sheet.

Integrated Device Technology, a recognized leader in high-speed CMOS technology, produces a broad line of products. This enables us to provide a complete CMOS solution to designers of high-performance digital systems. Not only do our product lines include industry standard devices, they also feature products with 3.3V technology, faster speed, lower power, and package and/or architectural benefits that allow the designer to achieve significantly improved system performance.

To find ordering information: Ordering Information for all products in this book appears in Section 1, along with the Package Outline Index, Product Selector Guides, and Cross Reference Guides. Reference data on our Technology Capabilities and Quality Commitments is included in separate sections (2 and 3, respectively).

To find product data: Start with the Table of Contents, organized by product line (page 1.2), or with the Numeric Table of Contents (page 1.4). These indexes will direct you to the page on which the complete technical data sheet can be found. Data sheets may be of the following type:

ADVANCE INFORMATION — contain initial descriptions, subject to change, for products that are in development, including features and block diagrams.

PRELIMINARY — contain descriptions for products soon to be, or recently, released to production, including features, pinouts and block diagrams. Timing data are based on simulation or initial characterization and are subject to change upon full characterization.

FINAL — contain minimum and maximum limits specified over the complete supply and temperature range for full production devices.

New products, product performance enhancements, additional package types and new product families are being introduced frequently. Please contact your local IDT sales representative to determine the latest device specifications, package types and product availability.

LIFE SUPPORT POLICY

Integrated Device Technology's products are not authorized for use as critical components in life support devices or systems unless a specific written agreement pertaining to such intended use is executed between the manufacturer and an officer of IDT.

1. **Life support devices or systems are devices or systems which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.**
2. **A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.**

1995 SPECIALIZED MEMORIES & MODULES DATA BOOK
TABLE OF CONTENTS

1

1995 SPECIALIZED MEMORIES & MODULES DATA BOOK (CONTINUED) ..... PAGE

FIFO PRODUCTS (CONTINUED)

1995 SPECIALIZED MEMORIES & MODULES DATA BOOK (CONTINUED) ..... PAGE

FIFO MODULES

Please refer to Subsystems Products listing for FIFO Modules.

SPECIALTY MEMORY PRODUCTS

MULTI-PORT MODULES

Please refer to Subsystems Products listing for Multi-Port Modules

1995 SPECIALIZED MEMORIES & MODULES DATA BOOK (CONTINUED) ..... PAGE

SUBSYSTEMS PRODUCTS

IDT SALES OFFICE, REPRESENTATIVE AND DISTRIBUTOR LOCATIONS

NUMERICAL TABLE OF CONTENTS

ORDERING INFORMATION

When ordering by TWX or Telex, the following format must be used:

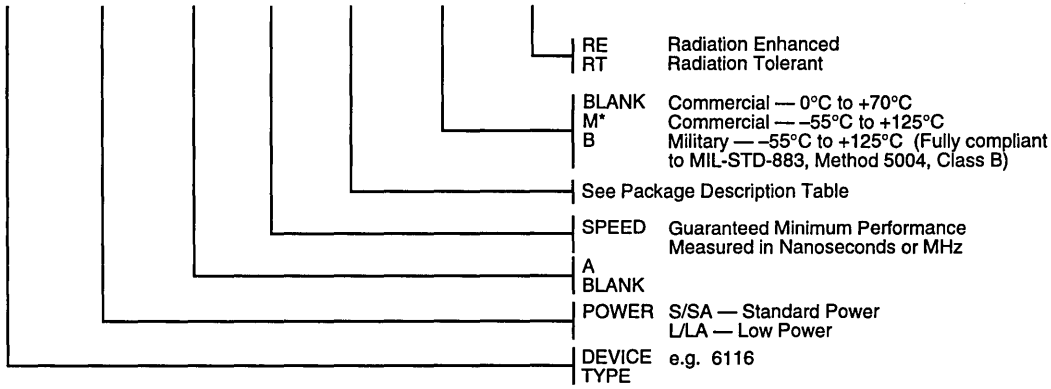
A. Complete Bill To.
B. Complete Ship To.
C. Purchase Order Number.
D. Certificate of Conformance. Y or N.
E. Customer Source Inspection. Y or N.
F. Government Source Inspection. Y or N
G. Government Contract Number and Rating.
H. Requested Routing.
I. IDT Part Number –
   Each item ordered must use the complete part number exactly as listed in the price book.
J. SCD Number — Specification Control Document (Internal Traveller).
K. Customer Part Number/Drawing Number/Revision Level –
   Specify whether part number is for reference only, mark only, or if extended processing to customer specification is required.
L. Customer General Specification Numbers/Other Referenced Drawing Numbers/Revision Levels.
M. Request Date With Exact Quantity.
N. Unit Price.
O. Special Instructions, Including Q.A. Clauses, Special Processing.

Federal Supply Code Number/Cage Number — 61772
Dun & Bradstreet Number — 03-814-2600
Federal Tax I.D. — 94-2669985
TLX# — 887766
FAX# — 408-727-3468

PART NUMBER DESCRIPTION

A = Alpha Character N = Numeric Character

IDT XXXXX (DEVICE TYPE) A (POWER) X (REVISION) 999 (SPEED) AA (PACKAGE) AA (PROCESS/TEMP.) AA (SPECIAL PROCESS)



PACKAGE DESCRIPTION TABLE

C	Ceramic Sidebraze	PF	Plastic Quad Flatpack
D	Cerdip	PZ	TSOP Type 1
F	Flatpack	SO	Plastic Small Outline IC
J	Plastic Leaded Chip Carrier	TC	Sidebraze Thindip (300-MIL)
L	Leadless Chip Carrier	TP	Plastic Thin Dual In-Line
P	Plastic DIP	TY	Thin SOJ
Y	SOJ	XE	Cerpack (F11 Config. only)

*Consult Factory

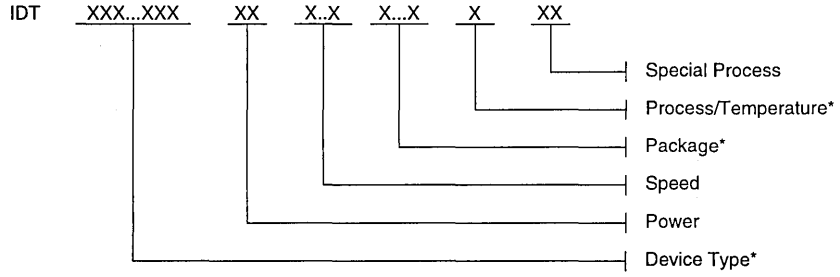
IDT PACKAGE MARKING DESCRIPTION

PART NUMBER DESCRIPTION

IDT's part number identifies the basic product, speed, power, package(s) available, operating temperature and processing grade. Each data sheet has a detailed description, using the part number, for ordering the proper product for the user's application. The part number is comprised of a series of alpha-numeric characters:

1. An "IDT" corporate identifier for Integrated Device Technology, Inc.
2. A basic device part number composed of alpha-numeric characters.
3. A device power identifier, composed of one or two alpha characters, is used to identify the power options. In most cases, the following alpha characters are used:
   "S" or "SA" is used for the standard power product.
   "L" or "LA" is used for lower power than the standard power product.
4. A device speed identifier, when applicable, is either alpha characters, such as "A" or "B", or numbers, such as 20 or 45. The speed units, depending on the product, are in nanoseconds or megahertz.
5. A package identifier, composed of one or two characters. The data sheet should be consulted to determine the packages available and the package identifiers for that particular product.
6. A temperature/process identifier. The product is available in either the commercial or military temperature range, processed to a commercial specification, or the product is available in the military temperature range with full compliance to MIL-STD-883. Many of IDT's products have burn-in included as part of the standard commercial process flow.
7. A special process identifier, composed of alpha characters, is used for products which require radiation enhancement (RE) or radiation tolerance (RT).

Example for Monolithic Devices:



* Field Identifier Applicable To All Products

2507 drw 01

ASSEMBLY LOCATION DESIGNATOR

IDT uses various locations for assembly. These are identified by an alpha character in the last letter of the date code marked on the package. Presently, the assembly location alpha character is as follows:

A = Anam, Korea
I = USA
P = Penang, Malaysia

MIL-STD-883C COMPLIANT DESIGNATOR

IDT ships military products which are compliant to the latest revision of MIL-STD-883C. Such products are identified by a "C" designation on the package. The location of this designator is specified by internal documentation at IDT.

First-In, First-Out Memories (FIFOs)

- Largest and most complete FIFO product line
- Easy to use, highly integrated data buffering solutions
- Represents the culmination of over 11 years of architectural innovation and technical expertise

SUPERSYNCS: NEXT GENERATION CLOCKED FIFOs

- Large density: 8K, 16K, and 32K words (9- and 18-bit wide)
- Ultra high-performance pipelined architecture—100MHz (8ns access time)
- Utilizes less expensive SRAM technology for low cost/bit
- Read, write clocks can be synchronous or simultaneous
- Auto Power Down minimizes external power management logic circuit needs
- Numerous easy to use add ons: partial reset, retransmit, serial loading, programmable flags, standard or first word fall through
  mode, and space saving 64-pin Thin Quad Flat Pack (TQFP)

SYNCHRONOUS (CLOCKED) UNIDIRECTIONAL FIFOs

- Ultra high-performance—83MHz
- 1-,8-, 9-, 18- and 36-bit wide widths
- Various FIFO depths—64 to 4K
- Read, write clocks can be asynchronous or simultaneous
- Programmable depths for Almost-Empty and Almost-Full flags
- Simple word width expansion
- Depth expansion versions available
- Space saving 64-pin Thin Quad Flat Pack (TQFP)

SYNCHRONOUS (CLOCKED) BIDIRECTIONAL FIFOs

- Very high-performance—50MHz
- 18-, and 36-bit wide words
- Read, write clocks can by asynchronous or simultaneous
- Programmable depths for Almost-Empty and Almost-Full flags
- Space saving 64-pin Thin Quad Flat Pack (TQFP)

ASYNCHRONOUS BIDIRECTIONAL FIFOs

- Bus-matching for 18/9-bit, 36/9-bit or 36/18-bit connections
- Bi-directional FIFOs for 9 or 18 bit parallel connections
- Bypass path for direct status/command or data interchange
- Programmable depths for Almost-Empty and Almost- Full flags
- Standard DMA control pins for peripheral interfaces
- Reread/rewrite capabilities

ASYNCHRONOUS UNIDIRECTIONAL FIFOs

- High-performance—12ns data access times
- 3.3V versions for low power consumption
- Various FIFO depths—256 to 16K
- Asynchronous or simultaneous reads and writes
- Simple width and depth expansion
- Surface mount package solutions
- Multiple flags- Full, Empty, and Half-Full
- Configurable Parallel/Serial versions
- Dedicated serial to parallel or parallel to serial versions

Part No.	Description	Max. Speed (ns) Mil.	Com'l.	Max. Power (mW)	Avail.	Fax Doc. No.	Data Book Page
SUPERSYNCS: NEXT GENERATION CLOCKED FIFOs							
IDT72261	16K x 9 (Depth expandable)	15	10	660	NOW	3036	I 5.20■
IDT72271	32K x 9 (Depth expandable)	15	10	660	NOW	3036	I 5.20■
IDT72255	8K x 18 (Depth expandable)	15	10	770	NOW	3037	I 5.21■
IDT72265	16K x 18 (Depth expandable)	15	10	770	NOW	3037	I 5.21■
SYNCHRONOUS (CLOCKED) UNIDIRECTIONAL FIFOs							
IDT72423	64 x 1	15	10	440	NOW	2747	CALL■
IDT72203	256 x 1	15	10	440	NOW	2747	CALL■
IDT72213	512 x 1	15	10	440	NOW	2747	CALL■
IDT72420	64 x 8	20	12	440	NOW	2680	I 5.12
IDT72200	256 x 8	20	12	440	NOW	2680	I 5.12
IDT72210	512 x 8	20	12	440	NOW	2655	I 5.12
IDT72220	1K x 8	25	15	440	NOW	2680	I 5.12
IDT72230	2K x 8	25	15	440	NOW	2680	I 5.12
IDT72240	4K x 8	25	15	440	NOW	2680	I 5.12
IDT72421	64 x 9	20	12	440	NOW	2655	I 5.13
IDT72201	256 x 9	20	12	440	NOW	2655	I 5.13
IDT72211	512 x 9	20	12	440	NOW	2655	I 5.13
IDT72221	1K x 9	25	15	440	NOW	2655	I 5.13
IDT72231	2K x 9	25	15	440	NOW	2655	I 5.13
IDT72241	4K x 9	25	15	440	NOW	2655	I 5.13
IDT72801	Dual 256 x 9 (Configurable)	—	15	700	NOW	3034	I 5.15

Part No.	Description	Max. Speed (ns) Mil.	Com'l.	Max. Power (mW)	Avail.	Fax Doc. No.	Data Book Page
IDT72811	Dual 512 x 9 (Configurable)	—	15	700	NOW	3034	I 5.15
IDT72821	Dual 1K x 9 (Configurable)	—	**15**	700	NOW	3034	I 5.15
IDT72831	Dual 2K x 9 (Configurable)	—	**15**	700	NOW	3034	I 5.15
IDT72841	Dual 4K x 9 (Configurable)	—	**15**	700	NOW	3034	I 5.15
IDT72205LB	256 x 18 (Depth expandable)	25	15	1100	NOW	2766	I 5.14
IDT72215LB	512 x 18 (Depth expandable)	25	15	1100	NOW	2766	I 5.14
IDT72225LB	1K x 18 (Depth expandable)	25	15	1100	NOW	2766	I 5.14
IDT72235LB	2K x 18 (Depth expandable)	25	15	1100	NOW	2766	I 5.14
IDT72245LB	4K x 18 (Depth expandable)	25	15	1100	NOW	2766	I 5.14
IDT72805	Dual 256 x 18 (Configurable)	—	20	1700	2Q'95		CALL■
IDT72815	Dual 512 x 18 (Configurable)	—	20	1700	2Q'95		CALL■
IDT72825	Dual 1K x 18 (Configurable)	—	20	1700	NOW		CALL■
IDT723611	64 x 36	—	15	1100	NOW	3024	I 5.22■
IDT723613	64 x 36 bus matching	—	15	1100	NOW		CALL■
IDT723631	512 x 36	—	15	1200	NOW	3023	I 5.26
IDT723641	1K x 36	—	15	1300	NOW	3023	I 5.26
IDT723651	2K x 36	—	15	1400	2Q'95	3023	I 5.26
SYNCHRONOUS (CLOCKED) BIDIRECTIONAL FIFOs							
IDT72605	256 x 18 x 2 dual memory bank	30	20	1375	NOW	2704	I 5.16
IDT72615	512 x 18 x 2 dual memory bank	30	20	1375	NOW	2704	I 5.16
IDT723612	64 x 36 x 2	—	15	1200	NOW	3025	I 5.23
IDT723614	64 x 36 x 2 bus matching	—	15	1200	NOW		CALL■
IDT723622	256 x 36 x 2	—	15	1250	NOW	3043	I 5.25
IDT723632	512 x 36 x 2	—	15	1300	NOW	3022	I 5.24
IDT723642	1K x 36 x 2	—	15	1400	4Q'95	3043	I 5.25
ASYNCHRONOUS UNIDIRECTIONAL FIFOs							
IDT72401	64 x 4	35MHz	45MHz	192	NOW	2747	I 5.6
IDT72402	64 x 5	35MHz	45MHz	192	NOW	2747	I 5.6
IDT72403	64 x 4 with $\overline{OE}$ (output enable)	35MHz	45MHz	192	NOW	2747	I 5.6
IDT72404	64 x 5 with $\overline{OE}$ (output enable)	35MHz	45MHz	192	NOW	2747	I 5.6
IDT72413	64 x 5 with $\overline{OE}$, Almost-Empty,Almost-Full flags	35MHz	45MHz	192	NOW	2748	I 5.7
IDT7200	256 x 9	20	12	770	NOW	2679	I 5.1
IDT7201	512 x 9	20	12	770	NOW	2679	I 5.1
IDT7202	1K x 9	20	12	770	NOW	2679	I 5.1
IDT7203	2K x 9	20	12	880	NOW	2661	I 5.2
IDT7204	4K x 9	20	12	880	NOW	2661	I 5.2
IDT7205	8K x 9	20	15	770	NOW	2661	I 5.2
IDT7206	16K x 9	20	15	880	NOW	2661	I 5.2
IDT7207	32K x 9	**20**	**15**	880	NOW		CALL■
ASYNCHRONOUS 3.3V FIFOs							
IDT72V01	512 x 9	—	25	180	2Q'95	3033	I 5.3
IDT72V02	1K x 9	—	25	180	NOW	3033	I 5.3
IDT72V03	2K x 9	—	25	180	NOW	3033	I 5.3

Part No.	Description	Max. Speed (ns) Mil.	Com'l.	Max. Power (mW)	Avail.	Fax Doc. No.	Data Book Page
IDT72V04	4K x 9	—	25	180	NOW	3033	I 5.3
IDT72V05	8K x 9	—	25	225	4Q'95		CALL■
ASYNCHRONOUS BIDIRECTIONAL FIFOs							
IDT72510	512 x 18—1K x 9 bus matching	—	25	1210	NOW	2669	I 5.18
IDT72511	512 x 18—512 x 18 (with reread/rewrite)	CALL	25	1210	NOW	2668	I 5.19
IDT72520	1K x 18—2K x 9 bus matching	—	25	1210	NOW	2669	I 5.18
IDT72521	1K x 18—1K x 18 (with reread/rewrite)	40	25	1265	NOW	2668	I 5.19
FLAGGED FIFOs							
IDT72021	1K x 9 with Half-Full, Almost-Empty, Almost-Full flags and $\overline{OE}$	30	25	660	NOW	2677	I 5.5
IDT72031	2K x 9 with Half-Full, Almost-Empty, Almost-Full flags and $\overline{OE}$	**30**	**25**	660	NOW	2677	I 5.5
IDT72041	4K x 9 with Half-Full, Almost-Empty, Almost-Full flags and $\overline{OE}$	**30**	**25**	660	NOW	2677	I 5.5
PARALLEL/SERIAL FIFOs							
IDT72103	2K x 9 configurable Parallel/Serial I/O, multiple flags, 50MHz serial rate and FlexiShift	40	35	770	NOW	2753	I 5.8
IDT72104	4K x 9 configurable Parallel/Serial I/O, multiple flags, 50MHz serial rate and FlexiShift	40	35	770	NOW	2753	I 5.8
IDT72105	256 x 16 dedicated Parallel-to-Serial I/O, 50MHz serial shift rate, multiple flags	—	25	550	NOW	2665	I 5.9
IDT72115	512 x 16 dedicated Parallel-to-Serial I/O, 50MHz serial shift rate, multiple flags	—	25	550	NOW	2665	I 5.9
IDT72125	1K x 16 dedicated Parallel-to-Serial I/O, 50MHz serial shift rate, multiple flags	—	25	550	NOW	2665	I 5.9
IDT72131	2K x 9 dedicated Parallel-to-Serial I/O, 50MHz serial rate, multiple flags and FlexiShift	40	35	770	NOW	2751	I 5.10
IDT72132	2K x 9 dedicated Serial-to-Parallel I/O, 50MHz serial rate, multiple flags and FlexiShift	40	35	770	NOW	2752	I 5.11
IDT72141	4K x 9 dedicated Parallel-to-Serial I/O, 50MHz serial rate, multiple flags and FlexiShift	40	35	770	NOW	2751	I 5.10
IDT72142	4K x 9 dedicated Serial-to-Parallel I/O, 50MHz serial rate, multiple flags and FlexiShift	40	35	770	NOW	2752	I 5.11

High-Speed CMOS/BiCMOS Multi-Port RAMs

- Now offering 12ns Dual-Port RAMs (the world's fastest)
- First synchronous Dual-Port (7099) available allowing for self-timed write cycles.
- Now offering the 70825 Sequential-Access Random-Access Memory (SARAM™).
- 3.3V options available (16K, 64K, 128K, 256K).
- World's first Four-Port™ RAMs.
- x9 Dual-Port RAMs (18K, 36K, 72K, 144K).
- Largest family of Dual-Port RAMs (8K to 512K).
- All Dual-Port RAMs have true dual-ported memory cells allowing simultaneous access from both ports.

Part No.	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Fax Doc. No.	Data Book Page
DUAL-PORT RAMs							
IDT7130	8K (1K x 8) MASTER: Industry's most popular	25	20	325	NOW	2689	I 6.1
IDT7140	8K (1K x 8) SLAVE: Functions with IDT7130 to provide 16-bit words or wider; pin-compatible with IDT7130	35	25	325	NOW	2689	I 6.1
IDT7132	16K (2K x 8) MASTER: Fastest available speeds in this industry standard product	25	20	325	NOW	2692	I 6.2
IDT7142	16K (2K x 8) SLAVE: Functions with IDT7132 to provide 16-bit words or wider; pin-compatible with IDT7132	35	25	325	NOW	2692	I 6.2
IDT71321	16K (2K x 8) MASTER: High-speed Dual-Port with Int.	—	20	325	NOW	2691	I 6.3
IDT71421	16K (2K x 8) SLAVE: Functions with IDT71321 to provide 16-bit words or wider; pin-compatible with IDT71321	—	25	325	NOW	2691	I 6.3
IDT70121	18K (2K x 9) MASTER: High-speed Dual-Port with Busy and Interrupt	—	25	400	NOW	2654	I 6.4
IDT70125	18K (2K x 9) SLAVE: Functions with IDT70121 to provide 18-bit words or wider	—	25	400	NOW	2654	I 6.4
IDT7133	32K (2K x 16) MASTER: High-speed Dual-Port with Busy	35	25	500	NOW	2746	I 6.5
IDT7143	32K (2K x 16) SLAVE: Functions with IDT7133 to provide 32-bit words or wider; pin-compatible with IDT7133	35	25	500	NOW	2746	I 6.5
IDT7134	32K (4K x 8) high-speed Dual-Port operation in systems where on-chip arbitration is not needed	35	25	500	NOW	2720	I 6.6
IDT71342	32K (4K x 8) Dual-Port RAM with Semaphores	35	25	500	NOW	2721	I 6.7
IDT7014	36K (4K x 9) very high-speed Dual-Port using our BiCMOS process	20	12	900	NOW	2528	I 6.8
IDT7015	72K (8K x 9) Dual-Port RAM with Busy, Interrupt, Semaphores and Master/Slave select	25	20	750	NOW	2954	
IDT7016	144K (16K x 9) Dual-Port RAM with Busy, Interrupt, Semaphores and Master/Slave select	25	15	750	Q2C95	2954	
IDT7005	64K (8K x 8) Dual-Port RAM with Busy, Interrupt, Semaphores and Master/Slave select	35	25	750	NOW	2738	I 6.9
IDT7006	128K (16K x 8) Dual-Port RAM with Busy, Interrupt, Semaphores and Master/Slave select	35	25	750	NOW	2739	I 6.11
IDT7007	256K (32K x 8) Dual-Port RAM with Busy, Interrupt, Semaphores and Master/Slave select	35	25	750	NOW	2940	I 6.13
IDT7008	512K (64K x 8) Dual-Port RAM with Busy, Interrupt, Semaphores and Master/Slave select	35	25	750	Q3C95	CALL	
IDT7024	64K (4K x 16) Dual-Port RAM with Busy, Interrupt, Semaphores and Master/Slave select	35	20	750	NOW	2740	I 6.10
IDT7025	128K (8K x 16) Dual-Port RAM with Busy, Interrupt, Semaphores and Master/Slave select	35	20	750	NOW	2683	I 6.12

High-Speed CMOS/BiCMOS Multi-Port RAMs

Part No.	Description	Max. Speed (ns) Mil.	Com'l.	Typical Power (mW)	Avail.	Fax Doc. No.	Data Book Page
DUAL-PORT RAMs (CONTINUED)							
IDT7026	256K (16K x 16) Dual-Port RAM with Busy, Semaphores and Master/Slave select	35	25	750	NOW	2939	I 6.14
IDT70261	256K (16K x 16) Dual-Port RAM with Busy, Interrupt, Semaphores and Master/Slave select	35	25	750	NOW	3039	I 6.15
IDT7027	512K (32K x 16) Industry's Largest Monolithic Dual-Port RAM with Busy, Interrupt, Semaphores and Master/Slave select	35	25	750	Q3C95		
Four-Port RAMs							
IDT7052	16K (2K x 8) Four-Port RAM offers added benefits for high-speed systems in which multiple access is required in the same cycle	30	25	750	NOW	2674	I 6.16
SYNCHRONOUS DUAL-PORT RAM							
IDT7099	36K (4K x 9) synchronous Dual-Port with registered data input, address, and control lines	20	15	900	NOW	3007	I 6.17
SEQUENTIAL ACCESS RANDOM ACCESS MEMORY (SARAM)							
IDT70824	64K (4K x 16) SARAM offers sequentialdata buffering on one port and random access on the other port	35	20	1200	NOW	3099	
IDT70825	128K (8K x 16) SARAM offers sequential data buffering on one port and random access on the other port	35	20	1200	NOW	3016	I 6.18
3.3V DUAL-PORT RAM							
IDT71V321	16K (2K x 8) MASTER: High-speed Dual-Port with Interrupt and 3.3V low power operation	—	25	250	NOW	3026	I 6.19
IDT70V05	64K (8K x 8) Dual-Port RAM with Busy, Interrupt, Semaphores, Master/Slave select and 3.3V low power operation	—	35	350	NOW	2941	I 6.20
IDT70V06	128K (16K x 8) Dual-Port RAM with Busy, Interrupt, Semaphores, Master/Slave select and 3.3V low power operation	—	35	350	NOW	2942	I 6.22
IDT70V07	256K (32K x 8) Dual-Port RAM with Busy, Interrupt, Semaphores, Master/Slave select and 3.3V low power operation	—	35	350	Q3C95	2943	I 6.24
IDT70V24	64K (4K x 16) Dual-Port RAM with Busy, Interrupt, Semaphores, Master/Slave select and 3.3V low power operation	—	35	350	NOW	2911	I 6.21
IDT70V25	128K (8K x 16) Dual-Port RAM with Busy, Interrupt, Semaphores, Master/Slave select and 3.3V low power operation	—	35	350	NOW	2944	I 6.23
IDT70V26	256K (16K x 16) Dual-port RAM with Busy, Semaphores, Master/Slave select and 3.3V low power operation	—	35	350	Q3C95	2945	I 6.25
IDT70V261	256K (16K x 16) Dual-Port RAM with Busy, Interrupt, Semaphores, Master/Slave select and 3.3V low power operation	—	35	350	Q3C95	3040	I 6.26

High-Speed CMOS and BiCMOS Module Products

- High-density, high-performance module products for commercial and military applications
- Standard module products are used in a wide range of applications, such as cache for personal computers and workstations as well as high-speed buffer memories for data communications, telecommunications, video systems, add-on VME- type cards, test systems, DSP-based systems, and intelligent controller systems.
- Fully customized module solutions are available to achieve optimum system integration and performance. Custom modules take advantage of IDT's experienced design, test, and manufacturing teams all working with the highest-performance components available.
- A wide variety of module packages are available offering the optimum combination of pin count and board area. Some of these packages include industry standard SIMMs, Dual read-out SIMMs, CELPs, DIPs, ZIPs and PGAs, in addition to other unique module packaging that use advanced high-density connectors.

Part No.	Description	Max. Speed (ns) Mil.	Com'l.	Avail.	Fax Doc. No.	Data Book Page
CUSTOM MODULES						
Please consult factory or call your local sales representative for more details.						
STATIC RAM MODULES						
IDT7MP4120	1M x 32 Static RAM Module	—	20	NOW	3019	I7.6
IDT7MP4145	256K x 32 Static RAM Module	—	15	NOW	3148	
IDT7MP4045	256K x 32 Static RAM Module	—	10	NOW	2703	I7.7
IDT7MP4095	128K x 32 Static RAM Module	—	20	NOW	3147	
IDT7M4013	128K x 32 Static RAM Module	25	—	NOW	2711	I7.8
IDT7MP4036	64K x 32 Static RAM Module	—	12	NOW	2682	I7.9
IDT7M4003	32K x 32 Static RAM Module	30	—	NOW	2711	I7.8
IDT7M4048	512K x 8 Static RAM Module	—	70	NOW	2675	I7.11
IDT7MB4048	512K x 8 Static RAM Module	—	25	NOW	2675	I7.11
IDT7M4048	512K x 8 Static RAM Module	30	—	NOW	2822	I7.12
PENTIUM MICROPROCESSOR SECONDARY CACHE MODULES						
IDT7MPV6240	3.3V 512KB Cache Module for the Pentium™ CPU and the VLSI Wildcat Core Logic	—	66MHz	NOW	3179	
IDT7MPV6215	512KB Cache Module for the Pentium CPU and the OPTi Viper Core Logic (Write-back)	—	66MHz	NOW	3091	
IDT7MPV6235	512KB Cache Module for the Pentium CPU and the SIS 85C501 Core Logic (Write-back)	—	66MHz	NOW	3178	
IDT7MPV6228	512KB Cache Module for the Pentium CPU including IDT71V280-based cache controller	—	15	3Q'95	3172	
IDT7MP6182	512KB Burst Cache Module for the Pentium CPU and the VLSI 82C590/Intel 82430NX (Neptune) Core Logic	—	9	NOW	3058	
IDT7MPV6200	3.3V 256KB Cache Module for the Pentium CPU and the Intel 82430FX (Triton) Core Logic	—	66MHz	NOW	3150	
IDT7MPV6239	3.3V 256KB Cache Module for the Pentium CPU and the VLSI Wildcat Core Logic	—	66MHz	NOW	3179	
IDT7MPV6214	256KB Cache Module for the Pentium CPU and the OPTi Viper Core Logic (Write-back)	—	66MHz	NOW	3091	
IDT7MPV6234	3.3V 256KB Cache Module for the Pentium CPU and the SIS 85C501 Core Logic	—	66MHz	NOW	3178	
IDT7MPV6229	256KB Burst Cache Module for the Pentium CPU including IDT71V280-based cache controller	—	8.5	3Q'95	3172	
IDT7MPV6227	256KB Cache Module for the Pentium CPU including IDT71V280-based cache controller	—	15	3Q'95	3172	
IDT7MPV6179	3.3V 256KB Cache Module for the Pentium CPU	—	15	NOW	3058	

Part No.	Description	Max. Speed (ns) Mil.	Com'l.	Avail.	Fax Doc. No.	Data Book Page
IDT7MPV6186	3.3V 256KB Cache Module for the Pentium CPU and the VLSI 82C590 Core Logic	—	15	NOW	3082	
IDT7MPV6189	3.3V 256KB Cache Module for the Pentium CPU and the Intel 82430NX (Neptune) Core Logic	—	15	NOW	3058	
IDT7MP6181	256KB Burst Cache Module for the Pentium CPU and the VLSI 82C590/Intel 82430NX (Neptune) Core Logic	—	10	NOW	3058	
486 MICROPROCESSOR SECONDARY CACHE MODULES						
IDT7MP6153	512KB Write-back Secondary Cache Module for the 486 CPU and Intel 82420TX Core Logic (9-bit tag)	—	33MHz	NOW	2929	I7.20
IDT7MP6193	256KB Write-back Secondary Cache Module for the 486 CPU and PicoPower Core Logic (9-bit tag)	—	50MHz	NOW	3066	
IDT7MP6191	256KB Write-back Secondary Cache Module for the 486 CPU and PicoPower Core Logic (8-bit tag)	—	50MHz	NOW	3066	
IDT7MP6184	256KB Write-back Secondary Cache Module for the 486 CPU and Intel 82420EX Core Logic	—	50MHz	NOW	3059	
IDT7MP6175	256KB Write-back Secondary Cache Module for the 486 CPU and VLSI Core Logic (9-bit tag)	—	50MHz	NOW	3057	
IDT7MP6171	256KB Write-back Secondary Cache Module for the 486 CPU and VLSI Core Logic (8-bit tag)	—	50MHz	NOW	3057	
IDT7MP6152	256KB Write-back Secondary Cache Module for the 486 CPU and Intel 82420TX Core Logic (9-bit tag)	—	33MHz	NOW	2929	I7.20
IDT7MP6192	128KB Write-back Secondary Cache Module for the 486 CPU and PicoPower Core Logic (9-bit tag)	—	50MHz	NOW	3066	
IDT7MP6190	128KB Write-back Secondary Cache Module for the 486 CPU and PicoPower Core Logic (8-bit tag)	—	50MHz	NOW	3066	
IDT7MP6183	128KB Write-back Secondary Cache Module for the 486 CPU and Intel 82420EX Core Logic	—	50MHz	NOW	3059	
IDT7MP6174	128KB Write-back Secondary Cache Module for the 486 CPU and VLSI Core Logic (9-bit tag)	—	50MHz	NOW	3057	
IDT7MP6170	128KB Write-back Secondary Cache Module for the 486 CPU and VLSI Core Logic (8-bit tag)	—	50MHz	NOW	3057	
IDT7MP6151	128KB Write-back Secondary Cache Module for the 486 CPU and Intel 82420TX Core Logic (9-bit tag)	—	33MHz	NOW	2929	I7.20
IDT7MP6104	128KB TurboCache SIMM for the 486 CPU	—	33MHz	NOW	2904	I7.17
IDT7MB6098A	128KB TurboCache Module for the 486 CPU	—	33MHz	NOW	2897	I7.16
DUAL-PORT MODULES						
IDT7M1014	4K x 36 Dual-Port Module	25	15	NOW	2819	I7.3
IDT7M1024	4K x 36 Synchronous Dual-Port Module	25	20	NOW	2809	I7.4
IDT7M1002	16K x 32 Dual-Port Module	40	30	NOW	2795	I7.2
IDT7M1001	128K x 8 Dual-Port Module	50	35	NOW	2804	I7.1
IDT7M1003	64K x 8 Dual-Port Module	50	35	NOW	2804	I7.2
FIFO MODULES						
IDT7M209	128K x 9 FIFO Module	30	20	3Q'95	2718	
IDT7M208	64K x 9 FIFO Module	30	20	NOW	2718	I7.5

Integrated Device Technology, Inc.

FIFO CROSS REFERENCE GUIDES

SYNCHRONOUS (CLOCKED) CROSS REFERENCE

PART	NUMBER	PACKAGES	
TI	IDT	TI	IDT
SN74ACT72211L	IDT72211L	RJ	J
SN74ACT72221L	IDT72221L	FN	J
SN74ACT72231L	IDT72231L	PN	PF
SN74ACT72241L	IDT72241L	PH	PF
SN74ACT7882*	IDT72235LB	PM	PF
SN74ACT7884*	IDT72245LB		
SN74ACT7801*	IDT72225LB		
SN74ACT7803*	IDT72215LB		
SN74ACT7805*	IDT72205LB		
SN74ACT7807*	IDT72231L		
SN74ACT7811*	IDT72225LB		
SN74ABT7819*	IDT72615L		
IC WORKS	**IDT**	**ICW**	**IDT**
ICW89C211	IDT72211L	L	J
ICW89C221	IDT72221L		
ICW89C231	IDT72231L		
ICW89C241	IDT72241L		
CYPRESS	**IDT**	**CYP**	**IDT**
CY7C441/451*	IDT72211L	JC	J
CY7C443/453*	IDT72231L	LMB	LB
CY7C445/455*	IDT72215LB	NC	PF
CY7C446/456*	IDT72225LB	PC	TP
CY7C447/457*	IDT72235LB	LC	L
		DC	D
QSI	**IDT**	**QSI**	**IDT**
QS7211*	IDT72211L	LB	LB
QS7212*	IDT72221L	JR	J
QS7223*	IDT72231L		
QS7224*	IDT72241L		
PARADIGM	**IDT**	**PDM**	**IDT**
PDM42205	IDT72205LB	J	J
PDM42215	IDT72215LB	G	G
PDM42225	IDT72225LB		
SHARP	**IDT**		
LH5492*	IDT72241	**SHP**	**IDT**
LH540215*	IDT72215LB	U	J
LH540225*	IDT72225LB		

*** FUNCTIONALLY COMPATIBLE**

ASYNCHRONOUS CROSS REFERENCE

PART	NUMBER	PACKAGES	
AMD	**IDT**	**AMD**	**IDT**
AM7200	IDT7200L	RC	TP
AM7201	IDT7201LA	DC	D
AM7202	IDT7202LA	JC	J
AM7203	IDT7203L	BXA	DB
AM7204	IDT7204L	N	P
AM7205	IDT7205L	PC	P
AM67C401	IDT72401L		
AM67C402	IDT72402L		
AM67C4013	IDT72403L		
AM67C4023	IDT72404L		
AM67C4033	IDT72413L		
MOSEL	**IDT**	**MSL**	**IDT**
MS7200	IDT7200L	NC	TP
MS7201	IDT7201LA	JC	J
MS7202	IDT7202LA	PC	P
MS7203	IDT7203L		
MS7204	IDT7204L		
QSI	**IDT**	**QSI**	**IDT**
QS7201	IDT7201LA	-	TP
QS7202	IDT7202LA	JR	J
QS7203	IDT7203L	P6	P
QS7204	IDT7204L	S3	SO
SAMSUNG	**IDT**	**SAM**	**IDT**
KM75C01	IDT7201LA	AP	P
KM75C02	IDT7202LA	AN	TP
KM75C03	IDT7203L	AJ	J
SHARP	**IDT**	**SHP**	**IDT**
LH5495	IDT7200L	D	TP
LH5496	IDT7201LA	U	J
LH5497	IDT7202LA	-	P
LH5498	IDT7203L		
LH5499	IDT7204L		
LH540205	IDT7205L		
LH540206	IDT7206L		
CYPRESS	**IDT**	**CYP**	**IDT**
CY7C420/421	IDT7201LA	PC	P
CY7C421A	IDT7201LA	DC	D
CY7C424/425	IDT7202LA	DMB	DB
CY7C425A	IDT7202LA	PC	TP
CY7C428/429	IDT7203L	JC	J
CY7C429A	IDT7203L	DC	TC
CY7C432/433	IDT7204L	LMB	LB
CY7C433A	IDT7204L		

*** Functionally Compatible**

ASYNCHRONOUS CROSS REFERENCE

CY7C439*	IDT7272L
CY7C460/(470*)	IDT7205L
CY7C462/(472*)	IDT7206L
CY3341	IDT72401L
CY7C401	IDT72401L
CY7C402	IDT72402L
CY7C403	IDT72403L
CY7C404	IDT72404L

SGS	IDT	SGS	IDT
MK45H01	IDT7201LA	N	P
MK45H02	IDT7202LA	K	J
MK45H03	IDT7203L		
MK45H04	IDT7204L		
MK45H08	IDT7205L		

TI	IDT	TI	IDT
SN74ACT7200L	IDT7200L	NP	TP
SN74ACT7201L	IDT7201LA	RJ	J
SN74ACT7202L	IDT7202LA	DV	SO
SN74ACT7203L	IDT7203L		
SN74ACT7204L	IDT7204L		
SN54/74ALS236	IDT72401L		
SN54/74ALS234	IDT72403L		
SN54/74ALS235	IDT72413L		

MICRON	IDT	MIC	IDT
MT52C9005	IDT7201LA	W	P
MT52C9010	IDT7202LA	C	D
MT52C9020	IDT7203L	EJ	J

NAT. SEMI	IDT	NS	IDT
NMF512X9	IDT7201LA	PC	P
NMF1024X9	IDT7202LA	LCC	J
NMF2048X9	IDT7203L		
NMF4098X9	IDT7204L		

MATRA MHS	IDT	MHS	IDT
xMyy67201A	IDT7201LA	S1	J
xMyy67202A	IDT7202LA	3P	TP
xMyy67203A	IDT7203L	TI	SO
xMyy67204A	IDT7204L	1I	D
xMyy67205A	IDT7205L	4J	L

x=temp range
yy= package

Guidelines for Using the Cross Reference Table

1- Match the part number
2- Match the package type
3- Refer to the Package/Speed availability chart

ORDERING INFORMATION

IDT 72xxxx xx xxx xx x

Device Type Power Speed Package Temp Range

NOTE:
IC WORKS, SAMSUNG, AND MICRON NO LONGER ACTIVELY SELLING FIFOs

CYPRESS	IDT
CY7C130-35PC	IDT7130SA35P
45PC	45P
55PC	55P
35DC	35C
45DC	45C
55DC	55C
25LC	25L48
35LC	35L48
45LC	45L48
55LC	55L48
35DMB	35CB
45DMB	45CB
55DMB	55CB
35LMB	35L48B
45LMB	45L48B
55LMB	55L48B
CY7C131-25JC	IDT7130SA25J
35JC	35J
45JC	45J
55JC	55J
CY7C132-35PC	IDT7132SA35P
45PC	45P
55PC	55P
35DC	35C
45DC	45C
55DC	55C
25LC	25L48
35LC	35L48
45LC	45L48
55LC	55L48
35DMB	35CB
45DMB	45CB
55DMB	55CB
35LMB	35L48B
45LMB	45L48B
55LMB	55L48B
CY7C136-25JC	IDT71321SA25J
35JC	35J
45JC	45J
55JC	55J
CY7B134-35PC	IDT7134SA35P
25DC	25C
35DC	35C
35DMB	35CB
25LC	25L48
35LC	35L48
35LMB	35L48B
CY7B135-25JC	IDT7134SA25J
35JC	35J

CYPRESS	IDT
CY7C140-35PC	IDT7140SA35P
45PC	45P
55PC	55P
35DC	35C
45DC	45C
55DC	55C
25LC	25L48
35LC	35L48
45LC	45L48
55LC	55L48
35DMB	35CB
45DMB	45CB
55DMB	55CB
35LMB	35L48B
45LMB	45L48B
55LMB	55L48B
CY7C141-25JC	IDT7140SA25J
35JC	35J
45JC	45J
55JC	55J
CY7C142-35PC	IDT7142SA35P
45PC	45P
55PC	55P
35DC	35C
45DC	45C
55DC	55C
25LC	25L48
35LC	35L48
45LC	45L48
55LC	55L48
35DMB	35CB
45DMB	45CB
55DMB	55CB
35LMB	35L48B
45LMB	45L48B
55LMB	55L48B
CY7C146-25JC	IDT71421SA25J
35JC	35J
45JC	45J
55JC	55J
CY7B1342-25JC	IDT71342SA25J
35JC	35J
CY7B144-25GC	IDT7005S25G
35GC	35G
25JC	25J
35JC	35J
35GMB	35GB
CY7B145-15JC	IDT7015S15J
25JC	25J
35JC	35J

MHS	IDT
CMS67130L35	IDT7130LA35J
L55	55J
CM367130L35	IDT7130LA35P
L55	55P
MM467130L35	IDT7130LA35L48B
L45	45L48B
L55	55L48B
CMS67140L35	IDT7140LA35J
L55	55J
CM367140L35	IDT7140LA35P
L55	55P
MM467140L35	IDT7140LA35L48B
L45	45L48B
L55	55L48B
CMS67132L35	IDT7132LA35J
L55	55J
CM367132L35	IDT7132LA35P
L55	55P
MM467132L35	IDT7132LA35L48B
L45	45L48B
L55	55L48B
CMS67142L35	IDT7142LA35J
L55	55J
CM367142L35	IDT7142LA35P
L55	55P
MM467142L35	IDT7142LA35L48B
L45	45L48B
L55	55L48B
CMS671321L35	IDT71321LA35J
L45	45J
L55	55J
CMS671421L35	IDT71421LA35J
L45	45J
L55	55J
CMS67005L35	IDT7005L35J
L45	45J
L55	55J
CM867005L35	IDT7005L35G
L45	45G
L55	55G
MM867005L35	IDT7005L35GB
L45	45GB
L55	55GB

MHS	IDT
MG67133H5	IDT7133SA25G
K5	35G
M5	45G
N5	55G
KMB	35GB
MMB	45GB
NMB	55GB
MS67133H	IDT7133SA25J
K5	35J
M5	45J
N5	55J
MG67143H5	IDT7143SA25G
K5	35G
M5	45G
N5	55G
KMB	35GB
MMB	45GB
NMB	55GB
MS67143H	IDT7143SA25J
K5	35J
M5	45J
N5	55J
CMS67024L35	IDT7024L35J
L45	45J
L55	55J
CM867024L35	IDT7024L35G
L45	45G
L55	55G
MM867024L35	IDT7024L35GB
L45	45GB
L55	55GB

Integrated Device Technology, Inc.

SSD PRODUCTS CROSS REFERENCE GUIDE

PART NUMBER	
CYPRESS	IDT
CYM1420HD-xxC	8M824SxxC
CYM1420HD-xxMB	8M824SxxCB
CYM1464PD-xxC	7MB4048SxxP
CYM1465PD-xxC	7M4048LxxN
CYM1620HD-xxC	8M624SxxC
CYM1622HV-xxC	7MP4027SxxV
CYM1828HG-xxC	7M4003SxxCH
CYM1828HG-xxMB	7M4003SxxCHB
CYM1830HD-xxC	7M4017SxxC
CYM1830HD-xxMB	7M4017SxxCB
CYM1831PZ-xxC	7MP4036SxxZ
CYM1831PM-xxC	7MP4036SxxM
CYM1838HG-xxC	7M4013SxxCH
CYM1838HG-xxMB	7M4013SxxCHB
CYM1840PD-xxC	7MB4067SxxP
CYM1841PZ-xxC	7MP4045SxxZ
CYM1841P7-xxC	7MP4145SxxM
CYM1841PM-xxC	7MP4045SxxM
CYM1851PZ-xxC	7MP4120SxxZ
CYM1851PM-xxC	7MP4120SxxM
CYM7485PM-xxC	7MP6104SxxM

PART NUMBER	
EDI	IDT
EDI8F3264CxxMZC	7MP4036SxxZ
EDI8F32256CxxBZC	7MP4045SxxZ
EDI8F32256CxxBMC	7MP4045SxxM
EDI8M8256CxxP6C	7M4068LxxN
EDI8M8512CxxP6C	7M4048LxxN
EDI8F8512CxxM6C	7MB4048SxxP
EDI8M8512CxxM6B	7M4048SxxCB
EDI8M1664CxxC6C	8M624SxxC
EDI8M1664CxxC6B	8M624SxxCB
EDI8F3264CxxM6C	7M4017SxxC
EDI8M3264CxxC6B	7M4017SxxCB
EDI8F32256CxxB6C	7MB4067SxxP

PART NUMBER	
MICRON	IDT
MT8S6432Z-xx	7MP4036SxxZ
MT8S6432M-xx	7MP4036SxxZ
MT8S25632Z-xx	7MP4045SxxZ
MT8S25632M-xx	7MP4045SxxM

PART NUMBER	
MOTOROLA	IDT
MCM32256Z-xx	7MP4045SxxZ
MCM32256SG-xx	7MP4045SxxM
MCM3264AZ-xx	7MP4036SxxZ
MCM32A128SG-xx	7MP6121SxxM
MCM32A256SG-xx	7MP6122SxxM
MCM4464-xx	7MP6084SxxM
MCM44256-xx	7MP6094SxxM

PART NUMBER	
DENSE-PAC	IDT
DPS128X32V3	7M4013SxxCH
DPS512S8-xxC	7M4048LxxN
DPS3232V	7M4003SxxCH
DPS128X32V3-xx	7M4013SxxCH

PART NUMBER	
MOSAIC	IDT
MS8512FKX-xx	7M4048LxxN
MS8512SC-xx	7MB4048SxxP
MS8512SCMB-xx	7M4048SxxCB
MS1664FKX-xx	8M624SxxC
PUMA 2S1000-xx	7M4003SxxCH
PUMA 2S4000-xx	7M4013SxxCH
MS3264FKX-xx	7M4017SxxC
MS32256FKX-xx	7MB4067SxxP

IDT...LEADING THE CMOS FUTURE

A major revolution is taking place in the semiconductor industry today. A new technology is rapidly displacing older NMOS and bipolar technologies as the workhorse of the '80s and beyond. That technology is high-speed CMOS. Integrated Device Technology, a company totally predicated on and dedicated to implementing high-performance CMOS products, is on the leading edge of this dramatic change.

Beginning with the introduction of the industry's fastest CMOS 2K x 8 Static RAM, IDT has grown into a company with multiple divisions producing a wide range of high-speed CMOS circuits that are, in almost every case, the fastest available. These advanced products are produced with IDT's proprietary CMOS technology, a twin-well, dry-etched, stepper-aligned process utilizing progressively smaller dimensions.

From inception, IDT's product strategy has been to apply the advantages of its extremely fast CMOS technology to produce the integrated circuit elements required to implement high-performance digital systems. IDT's goal is to provide the circuits necessary to create systems which are far superior to previous generations in performance, reliability, cost, weight, and size. Many of the company's innovative product designs offer higher levels of integration, advanced architectures, higher density packaging and system enhancement features that are establishing tomorrow's industry standards. The company is committed to providing its customers with an ever-expanding series of these high-speed, lower-power IC solutions to system design needs.

IDT's commitment, however, extends beyond state-of-the-art technology and advanced products to providing the highest level of customer service and satisfaction in the industry. Manufacturing products to exacting quality standards that provide excellent, long-term reliability is given the same level of importance and priority as device performance. IDT is also dedicated to delivering these high-quality advanced products on time. The company would like to be known not only for its technological capabilities, but also for providing its customers with quick, responsive, and courteous service.

IDT's product families are available in both commercial and military grades. As a bonus, commercial customers obtain the benefits of military processing disciplines, established to meet or exceed the stringent criteria of the applicable military specifications.

IDT is the leading U.S. supplier of high-speed CMOS circuits. The company's high-performance fast SRAM , FCT logic, high-density modules, FIFOs, multi-port memories, BiCMOS ECL I/O memories, RISC SubSystems, and the 32- and 64-bit RISC microprocessor families complement each other to provide high-speed CMOS solutions for a wide range of applications and systems.

Dedicated to maintaining its leadership position as a state-of-the-art IC manufacturer, IDT will continue to focus on maintaining its technology edge as well as developing a broader range of innovative products. New products and speed enhancements are continuously being added to each of the existing product families, and additional product families are being introduced. Contact your IDT field representative or factory marketing engineer for information on the most current product offerings. If you're building state-of-the-art equipment, IDT wants to help you solve your design problems.

IDT MILITARY AND DESC-SMD PROGRAM

IDT is a leading supplier of military, high-speed CMOS circuits. The company's high-performance Static RAMs, FCT Logic Family, Complex Logic (CLP), FIFOs, Specialty Memories (SMP), ECL I/O BiCMOS Memories, 32-bit RISC Microprocessor, RISC Subsystems and high-density Subsystems Modules product lines complement each other to provide high-speed CMOS solutions to a wide range of military applications and systems. Most of these product lines offer Class B products which are fully compliant to the latest revision of MIL-STD-883, Paragraph 1.2.1. In addition, IDT offers Radiation Tolerant (RT), as well as Radiation Enhanced (RE), products.

IDT has an active program with the Defense Electronic Supply Center (DESC) to list all of IDT's military compliant devices on Standard Military Drawings (SMD). The SMD program allows standardization of military products and reduction of the proliferation of non-standard source control drawings. This program will go far toward reducing the need for each defense contractor to make separate specification control drawings for purchased parts. IDT plans to have SMDs for many of its product offerings. Presently, IDT has over 140 devices which are listed or pending listing. The devices are from IDT's SRAM, FCT Logic family, Complex Logic (CLP), FIFOs and Specialty Memories (SMP) product families. IDT expects to add another 20 devices to the SMD program in the near future. Users should contact either IDT or DESC for current status of products in the SMD program.

SMD	
SRAM	**IDT**
84036	6116
5962-88740	6116LA
84132	6167
5962-86015	7187
5962-86859	6198/7198/7188
5962-86705	6168
5962-85525	7164
5962-88552	71256L
5962-88662	71256S
5962-88611	71682L
5962-89891	7198
5962-89892	6198
5962-89690	6116
5962-38294	7164
5962-89692	7188
5962-89790	71682
5962-92344	71B74
SMP	**IDT**
5962-86875	7130/7140
5962-87002	7132/7142
5962-88610	7133SA/7143SA
5962-88665	7133LA/7143LA
5962-89764	7134
5962-91508	7006
5962-91617	7025
5962-91662	7024
5962-93153	7014S
FIFO	**IDT**
5962-87531	7201LA
5962-86846	72404L
5962-88669	7203S
5962-89568	7204L
5962-89536	7202LA
5962-89863	7201SA
5962-89523	72403L/72401L
5962-89666	7200L
5962-89942	72103L
5962-89943	72104L
5962-89567	7203L
5962-90715	7204S
5962-91677	7205L
5962-93177	7206L
5962-92069	72141L
5962-92101	72215LB
5962-93138	72220L
5962-92057	72225LB
5962-93189	72245LB
5962-95506	72240L
5962-91585	7202SA
5962-91757	72200L
5962-91618	72031L
5962-94707	72231L
5962-94511	72241L

SMD	
CLP	**IDT**
5962-88533	49C460A/B/C
5962-86873	7216L
5962-87686	7217L
5962-88733	7210L
5962-92122	49C465/A
LOGIC	**IDT**
5962-87630	54FCT244/A
5962-87629	54FCT245/A
5962-86862	54FCT299/A
5962-87644	54FCT373/A
5962-87628	54FCT374/A
5962-87627	54FCT377/A
5962-87654	54FCT138/A
5962-87655	54FCT240/A
5962-87656	54FCT273/A
5962-89533	54FCT861A/B
5962-89506	54FCT827A/B
5962-88575	54FCT841A/B
5962-88608	54FCT821A/B
5962-88543	54FCT521/A
5962-88640	54FCT161/A
5962-88639	54FCT573/A
5962-88656	54FCT823A/B
5962-88657	54FCT163/A
5962-88674	54FCT825A/B
5962-88661	54FCT863A/B
5962-88736	29FCT520A/B
5962-88775	54FCT646/A
5962-89508	54FCT139/A
5962-89665	54FCT824A/B
5962-88651	54FCT533/A
5962-88653	54FCT645/A
5962-88654	54FCT640/A
5962-88655	54FCT534/A
5962-89767	54FCT540/A
5962-89766	54FCT541/A
5962-89733	54FCT191/A
5962-89652	54FCT399/A
5962-89513	54FCT574/A
5962-89731	54FCT833A/B
5962-89730	54FCT543/A
5962-90901	29FCT52A/B/C
5962-92204	29FCT52AT/BT/CT
5962-92205	29FCT520AT/BT/CT
5962-92206	54FCT151T/ATCT
5962-92242	54FCT623T/AT/CT
5962-92228	54CT841AT/BT/CT
5962-92259	54CT16373T/AT/CT
5962-92260	54FCT16374T/AT/CT
5962-92263	54FCT16543T/AT/CT
5962-92264	54FCT16646T/AT/CT
5962-92267	54FCT16827AT/BT/CT
5962-92268	54FCT16841AT/BT/CT

SMD	
5962-92270	54FCT162240T/AT/CT
5962-94744	54FCT162511AT/CT
5962-92278	54FCT162646T/AT/CT
5962-92283	54FCT162952AT/BT/CT
5962-92157	49FCT805/A/806/A
5962-92233	54FCT138T/AT/CT
5962-92202	54FCT139T/AT/CT
5962-92208	54FCT157T/AT/CT
5962-92209	54FCT161T/AT/CT
5962-92210	54FCT163T/AT/CT
5962-90669	54FCT193/A
5962-92213	54FCT240T/AT/CT
5962-92203	54FCT244T/AT/CT
5962-92214	54FCT245T/AT/CT
5962-92211	54FCT257T/AT/CT
5962-92215	54FCT273T/AT/CT
5962-92216	54FCT299T/AT/CT
5962-92217	54FCT373T/AT/CT
5962-92218	54FCT374T/AT/CT
5962-92219	54FCT377T/AT/CT
5962-92212	54FCT399T/AT/CT
5962-92234	54FCT521T/AT/BT/CT
5962-92236	54FCT534T/AT/CT
5962-92220	54FCT540T/AT/CT
5962-92237	54FCT541T/AT/CT
5962-92221	54FCT543T/AT/CT
5962-92238	54FCT573T/AT/CT
5962-92222	54FCT574T/AT/CT
5962-92240	54FCT621T/AT
5962-92243	54FCT640T/AT/CT
5962-92244	54FCT645T/AT/CT
5962-92223	54FCT646T/AT/CT
5962-92246	54FCT652T/AT/CT
5962-92225	54FCT821AT/BT/CT
5962-92229	54FCT823AT/BT/CT
5962-92230	54FCT825AT/BT/CT
5962-92247	54FCT827AT/BT/CT
5962-92257	54FCT16244T/AT/CT
5962-92258	54FCT16245T/AT/CT
5962-92271	54FCT162244T/AT/CT
5962-92272	54FCT162245T/AT/CT
5962-92273	54FCT162373T/AT/CT
5962-92274	54FCT162374T/AT/CT
5962-92276	54FCT162501AT/CT
5962-92280	54FCT162823AT/BT/CT

RADIATION HARDENED TECHNOLOGY

IDT manufactures and supplies radiation hardened products for military/aerospace applications. Utilizing special processing and starting materials, IDT's radiation hardened devices survive in hostile radiation environments. In Total Dose, Dose Rate, and environments where single event upset is of concern, IDT products are designed to continue functioning without loss of performance. IDT can supply all its products on these processes. Total Dose radiation testing is performed in-house on an ARACOR X-Ray system. External facilities are utilized for device research on gamma cell, LINAC and other radiation equipment. IDT has an on-going research and development program for improving radiation handling capabilities (See "IDT Radiation Tolerant/Enhanced Products for Radiation Environments" in Section 3) of IDT products/processes.

KNOWN GOOD DIE

Emerging high performance electronic systems require smaller and smaller form-factors. IDT is meeting these design challenges by offering Known Good Die (KGD) in addition to its broad array of small form-factor packages. The IDT KGD manufacturing process enables IDT to offer die that have received the same electrical tests, burn-in, and speed sorting at elevated temperatures as shipped packaged products. Via IDT KGD, users are able to manufacture cost-efficient and reliable multi-chip modules (MCMs), hybrids, and other high-density interconnect products. All IDT KGD, at the completion of their test flow, receive 100% die visual inspection and are packed within Gel-Pak™ containers. The Gel-Pak™ containers are then placed in vacuum sealed ESD wrappers prior to shipping. Delivered KGD products have superior yield, quality, and reliability over standard raw die offerings. Most IDT products can be offered as "KGD", and commercial, industrial or military temperatures can be considered.

IDT LEADING EDGE CEMOS TECHNOLOGY

HIGH-PERFORMANCE CEMOS

From IDT's beginnings in 1980, it has had a belief in and a commitment to CMOS. The company developed a high-performance version of CMOS, called enhanced CMOS (CEMOS), that allows the design and manufacture of leading-edge components. It incorporates the best characteristics of traditional CMOS, including low power, high noise immunity and wide operating temperature range; it also achieves speed and output drive equal or superior to bipolar Schottky TTL. The last decade has seen development and production of four "generations" of IDT's CEMOS technology with process improvements which have reduced IDT's electrical effective (L_{eff}) gate lengths by more than 50 percent from 1.3 microns (millionths of a meter) in 1981 to 0.6 microns in 1989.

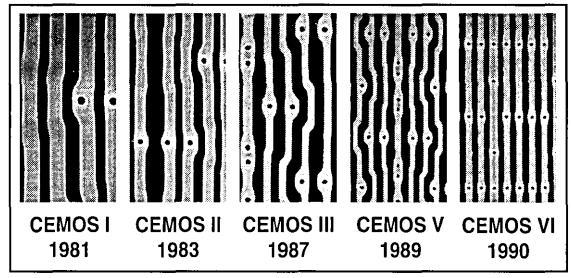
	CEMOS I	CEMOS II A	CEMOS II C	CEMOS III	CEMOS V	CEMOS VI
Calendar Year	**1981**	**1983**	**1985**	**1987**	**1989**	**1990**
Drawn Feature Size	2.5μ	1.7μ	1.3μ	1.2μ	1.0μ	0.8μ
Leff	1.3μ	1.1μ	0.9μ	0.8μ	0.6μ	0.45μ
Basic Proces Enhancements	Dual-well, Wet Etch, Projection Aligned	Dry Etch, Stepper	Shrink, Spacer	Silicide, BPSG, BiCEMOS I	BiCEMOS II	BiCEMOS III

2514 drw 01

CEMOS IV = CEMOS III – scaled process optimized for high-speed logic.

Figure 1.

Continual advancement of CEMOS technology allows IDT to implement progressively higher levels of integration and achieve increasingly faster speeds maintaining the company's established position as the leader in high-speed CMOS integrated circuits. In addition, the fundamental process technology has been extended to add bipolar elements to the CEMOS platform. IDT's BiCEMOS process combines the ultra-high speeds of bipolar devices with the lower power and cost of CMOS, allowing us to build even faster components than straight CMOS at a slightly higher cost.



SEM photos (miniaturization)

Figure 2. Fifteen-Hundred-Power Magnification Scanning Electron Microscope (SEM) Photos of the Four Generations of IDT's CEMOS Technology

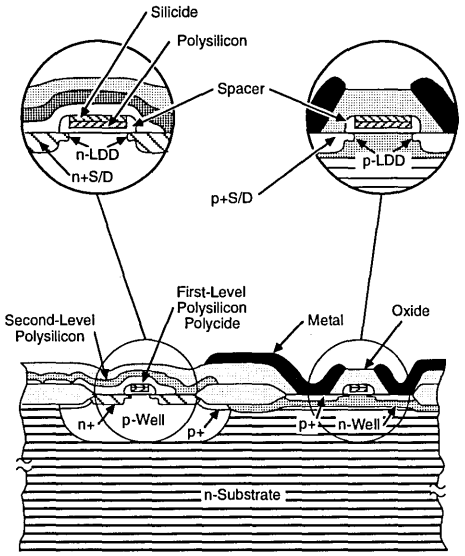


Figure 3. IDT CEMOS Device Cross Section

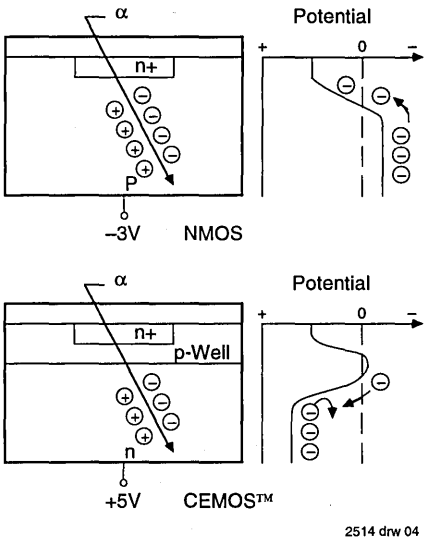


Figure 4. IDT CEMOS Built-In High Alpha Particle Immunity

ALPHA PARTICLES

Random alpha particles can cause memory cells to temporarily lose their contents or suffer a "soft error." Traveling with high energy levels, alpha particles penetrate deep into an integrated chip. As they burrow into the silicon, they leave a trail of free electron-hole pairs in their wake.

The cause of alpha particles is well documented and understood in the industry. IDT has considered various techniques to protect the cells from this hazardous occurrence. These techniques include dual-well structures (Figures 3 and 4) and a polymeric compound for die coating. Presently, a polymeric compound is used in many of IDT's SRAMs; however, the specific techniques used may vary and change from one device generation to the next as the industry and IDT improve the alpha particle protection technology.

LATCHUP IMMUNITY

A combination of careful design layout, selective use of guard rings and proprietary techniques have resulted in virtual elimination of latchup problems often associated with older CMOS processes (Figure 5). The use of NPN and N-channel I/O devices eliminates hole injection latchup. Double guard ring structures are utilized on all input and output circuits to absorb injected electrons. These effectively cut off the current paths into the internal circuits to essentially isolate I/O circuits. Compared to older CMOS processes which exhibit latchup characteristics with trigger currents from 10-20mA, IDT products inhibit latchup at trigger currents substantially greater than this.

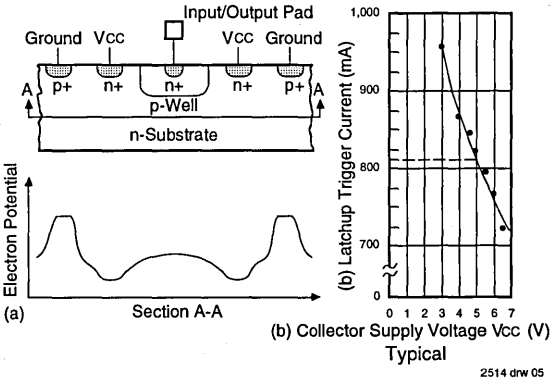


Figure 5. IDT CEMOS Latchup Suppression

STATE-OF-THE-ART FACILITIES AND CAPABILITIES

Integrated Device Technology is headquartered in Santa Clara, California—the heart of "Silicon Valley." The company's operations are housed in six facilities totaling over 500,000 square feet. These facilities house all aspects of business from research and development to design, wafer fabrication, assembly, environmental screening, test, and administration. In-house capabilities include scanning electron microscope (SEM) evaluation, particle impact noise detection (PIND), plastic and hermetic packaging, military and commercial testing, burn-in, life test, and a full complement of environmental screening equipment.

The over-200,000-square-foot corporate headquarters campus is composed of three buildings. The largest facility on this site is a 100,000 square foot, two-building complex. The first building, a 60,000-square-foot facility, is dedicated to the Standard Logic and RISC Microprocessor product lines, as well as hermetic and plastic package assembly, logic products' test, burn-in, mark, QA, and a reliability/failure analysis lab.

IDT's Packaging and Assembly Process Development teams are located here. To keep pace with the development of new products and to enhance the IDT philosophy of "innovation," these teams have ultra-modern, integrated and correspondingly sophisticated equipment and environments at their disposal. All manufacturing is completed in dedicated clean room areas (Class 10K minimum), with all preseal operations accomplished under Class 100 laminar flow hoods.

Development of assembly materials, processes and equipment is accomplished under a fully operational production environment to ensure reliability and repeatable product. The Hermetic Manufacturing and Process Development team is currently producing custom products to the strict requirements of MIL-STD-883. The fully automated plastic facility is currently producing high volumes of USA-manufactured product, while developing state-of-the-art surfac- mount technology patterned after MIL-STD-883.

The second building of the complex houses sales, marketing, finance, MIS, and Northwest Area Sales.

The RISC Subsystems Division is located across from the two-building complex in a 50,000-square-foot facility. Also located at this facility are Quality Assurance and wafer fabrication services. Administrative services, , Human Resources, International Planning, Shipping and Receiving departments are also housed in this facility.

IDT's largest and newest facility, opened in 1990 in San Jose, California, is a multi-purpose 150,000-square-foot, ultra-modern technology development center. This facility houses a 25,000 square foot, combined Class 1 (a maximum of one particle-per-cubic-foot of 0.2 micron or larger), sub-half-micron R&D fabrication facility and a wafer fabrication area. This fab supports both production volumes of IDT products, including some next-generation SRAMs, and the R&D efforts of the technology development staff. Technology development efforts targeted for the center include advanced silicon processing and wafer fabrication techniques. A test area to support both production and research is located on-site. The building is also the home of the FIFO, ECL, and Subsystems product lines.

IDT's second largest facility is located in Salinas, California, about an hour south of Santa Clara. This 95,000-square-foot facility, located on 14 acres, houses the Static RAM Division and Specialty Memory product line. Constructed in 1985, this facility contains an ultra-modern 25,000-square-foot high-volume wafer fabrication area measured at Class 2-to-3 (a maximum of 2 to 3 particles-per-cubic-foot of 0.2 micron or larger) clean room conditions. Careful design and construction of this fabrication area created a clean room environment far beyond the 1985 average for U.S. fab areas. This made possible the production of large volumes of high-density submicron geometry, fast static RAMs. This facility also houses shipping areas for IDT's leadership family of CMOS static RAMs. This site can expand to accommodate a 250,000-square-foot complex.

To extend our capabilities while maintaining strict control of our processes, IDT has an operational Assembly and Test facility located in Penang, Malaysia. This facility assembles product to U.S. standards, with all assemblies done under laminar flow conditions (Class 100) until the silicon is encased in its final packaging. All products in this facility are manufactured to the quality control requirements of MIL-STD-883.

All of IDT's facilities are aimed at increasing our manufacturing productivity to supply ever-larger volumes of high-performance, cost-effective, leadership CMOS products.

SUPERIOR QUALITY AND RELIABILITY

Maintaining the highest standards of quality in the industry on all products is the basis of Integrated Device Technology's manufacturing systems and procedures. From inception, quality and reliability are built into all of IDT's products. Quality is "designed in" at every stage of manufacturing – as opposed to being "tested-in" later – in order to ensure impeccable performance.

Dedicated commitment to fine workmanship, along with development of rigid controls throughout wafer fab, device assembly and electrical test, create inherently reliable products. Incoming materials are subjected to careful inspections. Quality monitors, or inspections, are performed throughout the manufacturing flow.

IDT military grade monolithic hermetic products are designed to meet or exceed the demanding Class B reliability levels of MIL-STD-883 and MIL-I-38535, as defined by Paragraph 1.2.1 of MIL-STD-883.

Product flow and test procedures for all monolithic hermetic military grade products are in accordance with the latest revision and notice of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with tight controls and inspections to ensure that products meet the requirements for 100% screening. Routine quality conformance lot testing is performed as defined in MIL-STD-883, Methods 5004 and 5005.

For IDT module products, screening of the fully assembled substrates is performed, in addition to the monolithic level screening, to assure package integrity and mechanical reliability. All modules receive 100% electrical tests (DC, functional and dynamic switching) to ensure compliance with the "subsystem" specifications.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that commercial, industrial and military grade products consistently meet customer requirements for quality, reliability and performance.

SPECIAL PROGRAMS

Class S. IDT also has all manufacturing, screening and test capabilities in-house (except X-ray and some Group D tests) to perform complete Class S processing per MIL-STD-883 on all IDT products and has supplied Class S products on several programs.

Radiation Hardened. IDT has developed and supplied several levels of radiation hardened products for military/aerospace applications to perform at various levels of dose rate, total dose, single event upset (SEU), upset and latchup. IDT products maintain nearly their same high-performance levels built to these special process requirements. The company has in-house radiation testing capability used both in process development and testing of deliverable product. IDT also has a separate group within the company dedicated to supplying products for radiation hardened applications and to continue research and development of process and products to further improve radiation hardening capabilities.

QSP–QUALITY, SERVICE AND PERFORMANCE

Quality from the beginning, is the foundation for IDT's commitment to supply consistently high-quality products to our customers. IDT's quality commitment is embodied in its all pervasive Continuous Quality Improvement (CQI) process. Everyone who influences the quality of the product–from the designer to the shipping clerk–is committed to constantly improving the quality of their actions.

IDT QUALITY PHILOSOPHY

"To make quantitative constant improvement in the quality of our actions that result in the supply of leadership products in conformance to the requirements of our customers."

IDT's ASSURANCE STRATEGY FOR CQI

Measurable standards are essential to the success of CQI. All the processes contributing to the final quality of the product need to be monitored, measured and improved upon through the use of statistical tools.

PRODUCT FLOW

DEVELOPMENT
|
FAB
|
ASSEMBLY
|
TEST
|
SHIP

Our customers receive the benefit of our optimized systems. Installed to enhance quality and reliability, these systems provide accurate and timely reporting on the effectiveness of manufacturing controls and the reliability and quality performance of IDT products and services.

SERVICE FLOW

ORDER ENTRY
|
PRODUCTION CONTROL
|
SHIPPING
|
CUSTOMER SUPPORT

These systems and controls concentrate on CQI by focusing on the following key elements:

Statistical Techniques
Using statistical techniques, including Statistical Process Control (SPC) to determine whether the product/ processes are under control.

Standardization
Implementing policies, procedures and measurement techniques that are common across different operational areas.

Documentation
Documenting and training in policies, procedures, measurement techniques and updating through characterization/ capability studies.

Productivity Improvement
Using constant improvement teams made up from employees at all levels of the organization.

Leadership
Focusing on quality as a key business parameter and strategic strength.

Total Employee Participation
Incorporating the CQI process into the IDT Corporate Culture.

Customer Service
Supporting the customer, as a partner, through performance review and pro-active problem solving.

People Excellence
Committing to growing, motivating and retaining people through training, goal setting, performance measurement and review.

PRODUCT FLOW

Product quality starts here. IDT has mechanisms and procedures in place that monitor and control the quality of our development activities. From the calibration of design capture libraries through process technology and product characterization that establish whether the performance, ratings and reliability criteria have been met. This includes failure analysis of parts that will improve the prototype product.

At the pre-production stage once again in-house qualification tests assure the quality and reliability of the product. All specifications and manufacturing flows are established and personnel trained before the product is placed into production.

Manufacturing
To accomplish CQI during the manufacturing stage, control items are determined for major manufacturing conditions. Data is gathered and statistical techniques are used to control specific manufacturing processes that affect the quality of the product.

In-process and final inspections are fed back to earlier processes to improve product quality. All product is burned-in (where applicable) before 100% inspection of electrical characteristics takes place.

Products which pass final inspection are then subject to Quality Assurance and Reliability Tests. This data is used to improve manufacturing processes and provide reliability predictions of field applications.

Inventory and Shipping

Controls in shipping focus on ensuring parts are identified and packaged correctly. Care is also taken to see that the correct paperwork is present and the product being shipped was processed correctly.

SERVICE FLOW

Quality not only applies to the product but to the quality -of -service we give our customers. Services is also constantly monitored for improvement.

Order Procedures

Checks are made at the order entry stage to ensure the correct processing of the Customer's product. After verification and data entry the Acknowledgements (sent to Customers) are again checked to ensure details are correct. As part of the CQI process, the results of these verifications are analyzed using statistical techniques and corrective actions are taken.

Production Control

Production Control (P.C.) is responsible for the flow and logistics of material as it moves through the manufacturing processes. The quality of the actions taken by P.C. greatly impinges on the quality of service the customer receives. Because many of our customers have implemented Just-in-Time (JIT) manufacturing practices, IDT as a supplier also has to adopt these same disciplines. As a result, employees receive extensive training and the performance level of key actions are kept under constant review. These key actions include:

Quotation response and accuracy.
Scheduling response and accuracy.
Response and accuracy of Expedites.
Inventory, management, and effectiveness.
On time delivery.

Customer Support

IDT has a worldwide network of sales offices and Technical Development Centers. These provide local customer support on business transactions, and in addition, support customers on applications information, technical services, benchmarking of hardware solutions, and demonstration of various Development Workstations.

The key to CQI is the timely resolution of defects and implementation of the corrective actions. This is no more important than when product failures are found by a customer.When failures are found at the customer's incoming inspection, in the production line, or the field application, the Division Quality Assurance group is the focal point for the investigation of the cause of failure and implementation of the corrective action. IDT constantly improves the level of support we give our customers by monitoring the response time to customers that have detected a product failure. Providing the customer with an analysis of the failure, including corrective actions and the statistical analysis of defects, brings CQI full circle–full support of our customers and their designs with high-quality products.

SUMMARY

In 1990, IDT made the commitment to *"Leadership through Quality, Service, and Performance Products"*.

We believe by following that credo IDT and our cusotmers will be successful in the coming decade.With the implementation of the CQI strategy within the company, we will satisfy our goal...

"Leadership through Quality, Service and Performance Products".

IDT QUALITY CONFORMANCE PROGRAM

A COMMITMENT TO QUALITY

Integrated Device Technology's monolithic assembly products are designed, manufactured and tested in accordance with the strict controls and procedures required by Military Standards. The documentation, design and manufacturing criteria of the Quality and Reliability Assurance Program were developed and are being maintained to the most current revisions of MIL-38510 as defined by paragraph 1.2.1 of MIL-STD-883 and MIL-STD-883 requirements.

Product flow and test procedures for all Class B *monolithic* hermetic Military Grade microcircuits are in full compliance with paragraph 1.2.1 of MIL-STD-883. State-of-the-art production techniques and computer-based test procedures are coupled with stringent controls and inspections to ensure that products meet the requirements for 100% screening and quality conformance tests as defined in MIL-STD-883, Methods 5004 and 5005.

Product flow and test procedures for all *plastic* and *commercial hermetic* products are in accordance with industry practices for producing highly reliable microcircuits to ensure that products meet the IDT requirements for 100% screening and quality conformance tests.

By maintaining these high standards and rigid controls throughout every step of the manufacturing process, IDT ensures that our products consistently meet customer requirements for quality, reliability and performance.

SUMMARY

Monolithic Hermetic Package Processing Flow[1]

Refer to the Monolithic Hermetic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are cut and separated and the individual die are 100% visually inspected to strict IDT-defined internal criteria.

3. **Die Shear Monitor:** To ensure die attach integrity, product samples are routinely subjected to a shear strength test per Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to a strength test per Method 2011, Condition D, to ensure the integrity of the lead bond process.

5. **Pre-Cap Visual:** Before the completed package is sealed, 100% of the product is visually inspected to Method 2010, Condition B criteria.

6. **Environmental Conditioning:** 100% of the sealed product is subjected to environmental stress tests. These thermal and mechanical tests are designed to eliminate units with marginal seal, die attach or lead bond integrity.

7. **Hermetic Testing:** 100% of the hermetic packages are subjected to fine and gross leak seal tests to eliminate marginally sealed units or units whose seals may have become defective as a result of environmental conditioning tests.

8. **Pre-Burn-In Electrical Test:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

9. **Burn-In:** 100% of the Military Grade product is burned-in under dynamic electrical conditions to the time and temperature requirements of Method 1015, Condition D. Except for the time, Commercial Grade product is burned-in as applicable to the same conditions as Military Grade devices.

10. **Post-Burn-In Electrical:** After burn-in, 100% of the Class B Military Grade product is electrically tested to IDT data sheet or customer specifications over the –55°C to +125°C temperature range. Commercial Grade products are sample tested to the applicable temperature extremes.

11. **Mark:** All product is marked with product type and lot code identifiers. MIL-STD-883 compliant Military Grade products are identified with the required compliant code letter.

12. **Quality Conformance Tests:** Samples of the Military Grade product which have been processed to the 100% screening tests of Method 5004 are routinely subjected to the quality conformance requirements of Method 5005.

NOTE:

1. For quality requirements beyond Class B levels such as SEM analysis, X-Ray inspection, Particle Impact Noise Reduction (PIND) test, Class S screening or other customer specified screening flows, please contact your Integrated Device Technology sales representative.

SUMMARY

Monolithic Plastic Package Processing Flow

Refer to the Monolithic Plastic Package Processing Flow diagram. All test methods refer to MIL-STD-883 unless otherwise stated.

1. **Wafer Fabrication:** Humidity, temperature and particulate contamination levels are controlled and maintained according to criteria patterned after Federal Standard 209, Clean Room and Workstation Requirements. All critical workstations are maintained at Class 100 levels or better.

   Topside silicon nitride passivation is all applied to all wafers for better moisture barrier characteristics.

   Wafers from each wafer fabrication area are subjected to Scanning Electron Microscope analysis on a periodic basis.

2. **Die Visual Inspection:** Wafers are 100% visually inspected to strict IDT defined internal criteria.

3. **Die Push Test:** To ensure die attach integrity, product samples are routinely subjected to die push tests, patterned after MIL-STD-883, Method 2019.

4. **Wire Bond Monitor:** Product samples are routinely subjected to wire bond pull and ball shear tests to ensure the integrity of the wire bond process, patterned after MIL-STD-883, Method 2011, Condition D.

5. **Pre-Cap Visual:** Before encapsulation, all product lots are visually inspected (using LTPD 5 sampling plan) to criteria patterned after MIL-STD-883, Method 2010, Condition B.

6. **Post Mold Cure:** Plastic encapsulated devices are baked to ensure an optimum polymerization of the epoxy mold compound so as to enhance moisture resistance characteristics.

7. **Pre-Burn-In Electrical:** Each product is 100% electrically tested at an ambient temperature of +25°C to IDT data sheet or the customer specification.

8. **Burn-In:** Except for MSI Logic family devices where it may be obtained as an option, all Commercial Grade plastic package products are burned-in for 16 hours at +125°C minimum (or equivalent), utilizing the same burn-in conditions as the Military Grade product.

9. **Post-Burn-In Electrical:** After burn-in, 100% of the plastic product is electrically tested to IDT data sheet or customer specifications at the maximum temperature extreme. The minimum temperature extreme is tested periodically on an audit basis.

10. **Mark:** All product is marked with product type and lot code identifiers. Products are identified with the assembly and test locations.

11. **Quality Conformance Inspection:** Samples of the plastic product which have been processed to the 100% screening requirements are subjected to the Periodic Quality Conformance Inspection Program. Where indicated, the test methods are patterned after MIL-STD-883 criteria.

TABLE 1

This table defines the device class screening procedures for IDT's high reliability products in conformance with MIL-STD-883C.

Monolithic Hermetic Package Final Processing Flow

	CLASS-S		CLASS-B		CLASS-C [1]	
OPERATION	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**	**TEST METHOD**	**RQMT**
BURN-IN	1015 Cond. D, 240 Hrs @ 125°C or equivalent	100%	1015 Cond. D, 160 Hrs. @ 125°C min or equivalent	100%	Per applicable device specification	100%
POST BURN-IN ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification +25, -55 and 125°C	100%	Per applicable device specification +25, -55 and 125°C	100%	Per applicable [2] device specification	100%
Group A ELECTRICAL: Static (DC), Functional and Switching (AC)	Per applicable device specification and 5005	Sample	Per applicable device specification and 5005	Sample	Per applicable [2] device specification	Sample
MARK/LEAD STRAIGHTENING	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
FINAL ELECTRICAL TEST	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%	Per applicable device specification +25°C	100%
FINAL VISUAL/PACK	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%
QUALITY CONFORMANCE INSPECTION	5005 Group B, C, D.	Sample	5005 Group B,C,D.	Sample	IDT Spec	Sample
QUALITY SHIPPING INSPECTION (Visual/Plant Clearance)	IDT Spec	100%	IDT Spec	100%	IDT Spec	100%

NOTES:
1. Class-C = IDT commercial spec. for hermetic and plastic packages
2. Typical 0°C, 70°C, Extended -55°C +125°C

RADIATION TOLERANT/ENHANCED/HARDENED PRODUCTS FOR RADIATION ENVIRONMENTS

INTRODUCTION

The need for high-performance CMOS integrated circuits in military and space systems is more critical today than ever before. The low power dissipation that is achieved using CMOS technology, along with the high complexity and density levels, makes CMOS the nearly ideal component for all types of applications.

Systems designed for military or space applications are intended for environments where high levels of radiation may be encountered. The implication of a device failure within a military or space system clearly is critical. IDT has made a significant contribution toward providing reliable radiation-tolerant systems by offering integrated circuits with enhanced radiation tolerance. Radiation environments, IDT process enhancements and device tolerance levels achieved are described below.

THE RADIATION ENVIRONMENT

There are four different types of radiation environments that are of concern to builders of military and space systems. These environments and their effects on the device operation, summarized in Figure 1, are as follows:

Total Dose Accumulation refers to the total amount of accumulated gamma rays experienced by the devices in the system, and is measured in RADS (SI) for radiation units experienced at the silicon level. The physical effect of gamma rays on semiconductor devices is to cause threshold shifts (Vt shifts) of both the active transistors as well as the parasitic field transistors. Threshold voltages decrease as total dose is accumulated; at some point, the device will begin to exhibit parametric failures as the input/output and supply currents increase. At higher radiation accumulation levels, functional failures occur. In memory circuits, however, functional failures due to memory cell failure often occur first.

Burst Radiation or Dose Rate refers to the amount of radiation, usually photons or electrons, experienced by the devices in the system due to a pulse event, and is measured in RADS (Si) per second. The effect of a high dose rate or burst of radiation on CMOS integrated circuits is to cause temporary upset of logic states and/or CMOS latch-up. Latch-up can cause permanent damage to the device.

Single Event Upset (SEU) is a transient logic state change caused by high-energy ions, such as energetic cosmic rays, striking the integrated circuits. As the ion passes through the silicon, charge is either created through ionization or direct nuclear collision. If collected by a circuit node, this excess charge can cause a change in logic state of the circuit. Dynamic nodes that are not actively held at a particular logic state (dynamic RAM cells for example) are the most susceptible. These upsets are transient, but can cause system failures known as "soft errors."

Neutron Irradiation will cause structural damage to the silicon lattice which may lead to device leakage and, ultimately, functional failure.

DEVICE ENHANCEMENTS

Of the four radiation environments above, IDT has taken considerable data on the first two, Total Dose Accumulation and Dose Rate. IDT has developed a process that significantly improves the radiation tolerance of its devices within these environments. Prevention of SEU failures is usually accomplished by system-level considerations, such as Error Detection and Correction (EDC) circuitry, since the occurrence of SEUs is not particularly dependent on process technology. Through IDT's customer contracts, SEU has been gathered on some devices. Little is yet known about the effects of neutron-induced damage. For more information on SEU testing, contact IDT's Radiation Hardened Product Group.

Radiation Category	Primary Particle	Source	Effect
Total Dose	Gamma	Space or Nuclear Event	Permanent
Dose Rate	Photons	Nuclear Event	Temporary Upset of Logic State or Latch-up
SEU	Cosmic Rays	Space	Temporary Upset of Logic State
Neutron	Neutrons	Nuclear Event	Device Leakage Due to Silicon Lattice Damage

2510 drw 01

Figure 1.

Enhancements to IDT's standard process are used to create radiation enhanced and tolerant processes. Field and gate oxides are "hardened" to make the device less susceptible to radiation damage by modifying the process architecture to allow lower temperature processing. Device implants and Vts adjustments allow more Vt margin. In addition to process changes, IDT's radiation enhanced process utilizes epitaxial substrate material. The use of epi substrate material provides a lower substrate resistance environment to create latch-up free CMOS structures.

RADIATION HARDNESS CATEGORIES

Radiation Enhanced (RE) or Radiation Tolerant ('RT) versions of IDT products follow IDT's military product data sheets whenever possible (consult factory). IDT's Total Dose Test plan exposes a sample of die on a wafer to a particular Total Dose level via ARACOR X-Ray radiation. This Total Dose Test plan qualifies each 'RE or 'RT wafer to a Total Dose level. Only wafers with sampled die that pass Total Dose level

tests are assembled and used for orders (consult factory for more details on Total Dose sample testing). With regard to Total Dose testing, clarifications/exceptions to MIL-STD-883, Methods 5005 and 1019 are required. Consult factory for more details.

The 'RE and 'RT process enhancements enable IDT to offer integrated circuits with varying grades of radiation tolerance or radiation "hardness".

- Radiation Enhanced process uses Epi wafers and is able to provide devices that can be Total Dose qualified to 10K RADs (Si) or greater by IDT's ARACOR X-Ray Total Dose sample die test plan (Total Dose levels require negotiation, consult factory for more details).
- Radiation Tolerant product uses standard wafer/process material that is qualified to 10K RADs (Si) Total Dose by IDT's ARACOR X-Ray Total Dose sample die test plan.

Integrated Device Technology can provide Radiation Tolerant/Enhanced versions of all product types (some speed grades may not be available as 'RE).

Please contact your IDT sales representative or factory marketing to determine availability and price of any IDT product processed in accordance with one of these levels of radiation hardness.

CONCLUSION

There has been widespread interest within the military and space community in IDT's CMOS product line for its radiation hardness levels, as well as its high-performance and low power dissipation. To serve this growing need for CMOS circuits that must operate in a radiation environment, IDT has created a separate group within the company to concentrate on supplying products for these applications.Continuing research and development of process and products, including the use of in-house radiation testing capability, will allow Integrated Device Technology to offer continuously increasing levels of radiation-tolerant solutions.

THERMAL PERFORMANCE CALCULATIONS FOR IDT'S PACKAGES

Since most of the electrical energy consumed by microelectronic devices eventually appears as heat, poor thermal performance of the device or lack of management of this thermal energy can cause a variety of deleterious effects. This device temperature increase can exhibit itself as one of the key variables in establishing device performance and long term reliability; on the other hand, effective dissipation of internally generated thermal energy can, if properly managed, reduce the deleterious effects and improve component reliability.

A few key benefits of IDT's enhanced CMOS process are: low power dissipation, high speed, increased levels of integration, wider operating temperature ranges and lower quiescent power dissipation. Because the reliability of an integrated circuit is largely dependent on the maximum temperature the device attains during operation, and as the junction stability declines with increases in junction temperature (T_J), it becomes increasingly important to maintain a low (T_J).

CMOS devices stabilize more quickly and at greatly lower temperature than bipolar devices under normal operation. The accelerated aging of an integrated circuit can be expressed as an exponential function of the junction temperature as:

$$t_A = t_o \exp\left[\frac{E_a}{k}\left(\frac{1}{T_O} - \frac{1}{T_J}\right)\right]$$

where

- t_A = lifetime at elevated junction (T_J) temperature
- t_O = normal lifetime at normal junction (T_O) temperature
- E_a = activation energy (ev)
- k = Boltzmann's constant (8.617×10^{-5}ev/k)

i.e. the lifetime of a device could be decreased by a factor of 2 for every 10°C increase temperature.

To minimize the deleterious effects associated with this potential increase, IDT has:

1. Optimized our proprietary low-power CMOS fabrication process to ensure the active junction temperature rise is minimal.
2. Selected only packaging materials that optimize heat dissipation, which encourages a cooler running device.
3. Physically designed all package components to enhance the inherent material properties and to take full advantage of heat transfer and radiation due to case geometries.
4. Tightly controlled the assembly procedures to meet or exceed the stringent criteria of MIL-STD-883_ to ensure maximum heat transfer between die and packaging materials.

The following figures graphically illustrate the thermal values of IDT's current package families. Each envelop (shaded area) depicts a typical spread of values due to the influence of a number of factors which include: circuit size, package materials and package geometry. The following range of values are to be used as a comprehensive characterization of the major variables rather than single point of reference.

When calculating junction temperature (T_J), it is necessary to know the thermal resistance of the package (θ_{JA}) as measured in "degree celsius per watt". With the accompanying data, the following equation can be used to establish thermal performance, enhance device reliability and ultimately provide you, the user, with a continuing series of high-speed, low-power CMOS solutions to your system design needs.

4

$$\theta_{JA} = [T_J - T_A]/P$$
$$T_J = T_A + P[\theta_{JA}] = T_A + P[\theta_{JC} + \theta_{CA}]$$

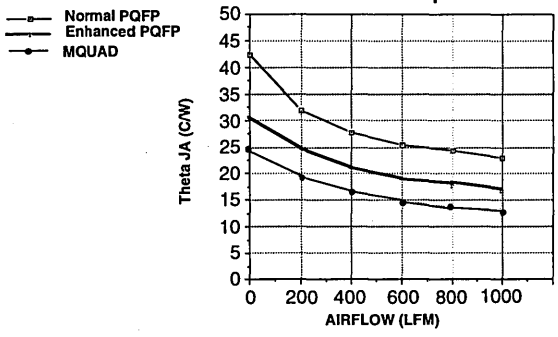
where

$$\frac{\theta_{JC} = T_J - T_C}{P} \qquad \frac{\theta_{CA} = T_C - T_A}{P}$$

- θ = Thermal resistance
- J = Junction
- P = Operational power of device (dissipated)
- T_A = Ambient temperature in degree celsius
- T_J = Temperature of the junction
- T_C = Temperature of case/package
- θ_{CA} = Case to Ambient, thermal resistance—usually a measure of the heat dissipation due to natural or forced convection, radiation and mounting techniques.
- θ_{JC} = Junction to Case, thermal resistance—usually measured with reference to the temperature at a specific point on the package (case) surface. (Dependent on the package material properties and package geometry.)
- θ_{JA} = Junction to Ambient, thermal resistance—usually measured with respect to the temperature of a specified volume of still air. (Dependent on θ_{JC} + θ_{JA} which includes the influence of area and environmental condition.)

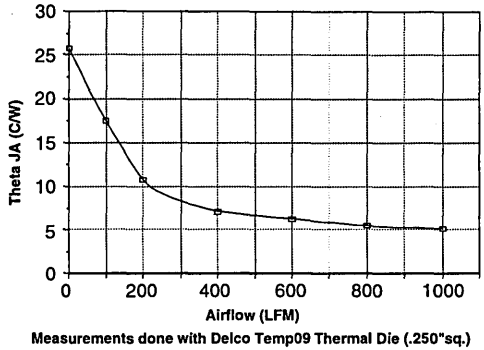
Ref. MIL-STD-883C, Method 1012.1
JEDEC ENG. Bulletin No. 20, January 1975
1986 Semi. Std., Vol. 4, Test Methods G30–86, G32–86.

Theta JA vs. Airflow
160 Pin Quad Flatpacks



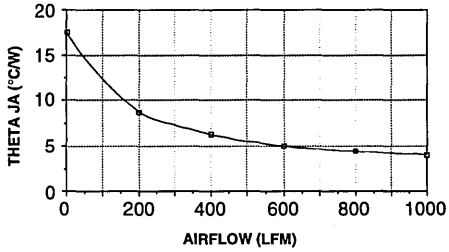
Delco Temp 09 Thermal Die (.250"sq.)
Parts mounted to standard 3" sq. test board.

Theta JA vs. Airflow
144 pin PGA - Cavity Down w/ CuW heatsink



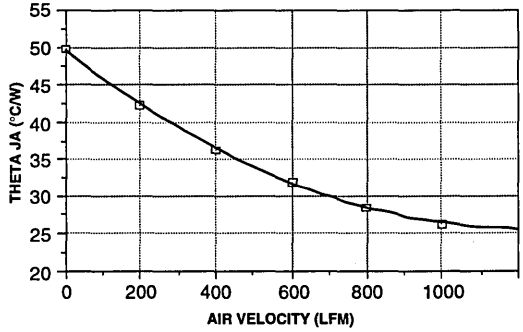
Measurements done with Delco Temp09 Thermal Die (.250"sq.)

THETA JA vs. AIRFLOW
179 PIN PGA - R4000 PACKAGE
INTEGRAL CuW HEATSINK - NO FIN ATTACHED



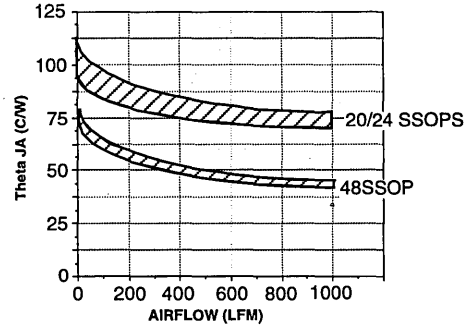
Delco Temp09 Thermal Die Array (.500"sq.)
applied power = 3W

THETA JA vs. AIR FLOW
32 pin J-bend SOIC



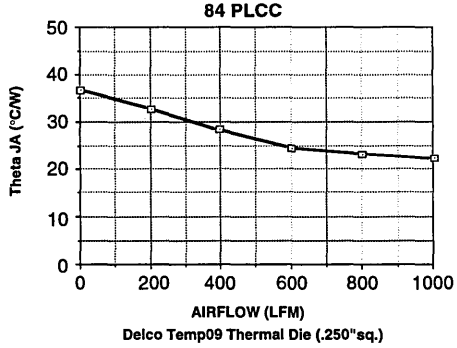
Theta JC was measured to be 17°C/W - Die size (.150"x.250")

Theta JA vs. Airflow
PLASTIC SSOP PACKAGES



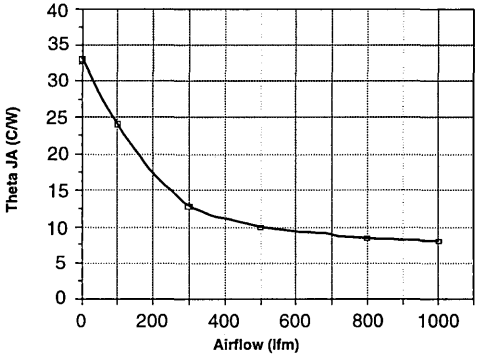
THETA JC : 20/24 PIN = 35-40 °C/W
48 PIN = 16-20 °C/W

THETA JA VS. AIRFLOW
84 PLCC



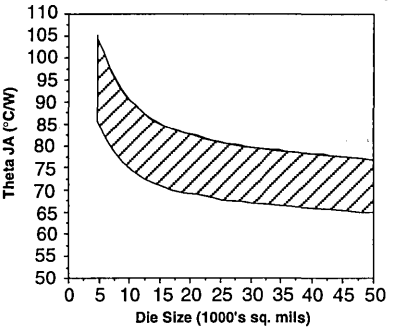
Delco Temp09 Thermal Die (.250"sq.)

Theta JA vs. Airflow
84 pin PGA - Cavity Down w/CuW heatsink



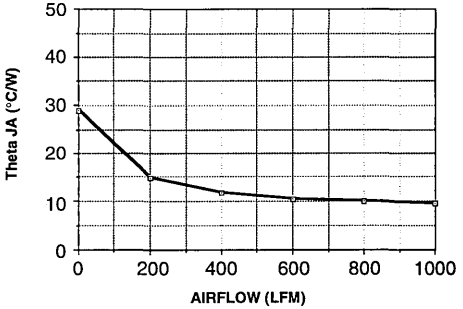
Measurements were done using Temp09 Delco Thermal Die (.250sq.)

Theta JA - Still Air 16-20 Lead Ceramic Dips



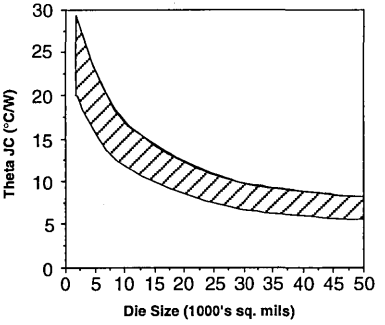
4

GD 208 THETA JA VS. AIRFLOW

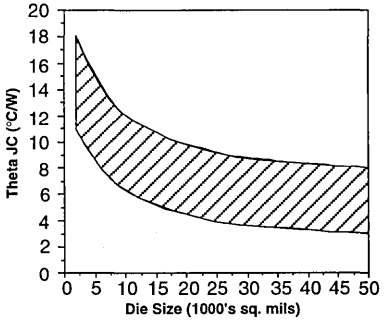


Delco Temp09 Thermal Die (.250"sq.)

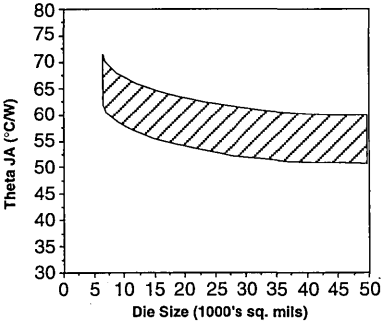
Theta JC 16-20 Lead Ceramic Dip



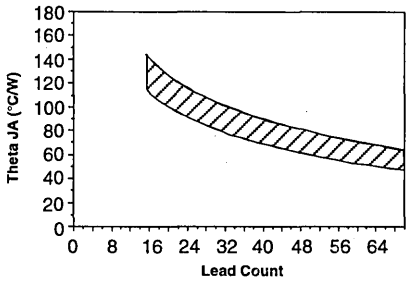
Theta JC 22-40 Lead Ceramic Dips



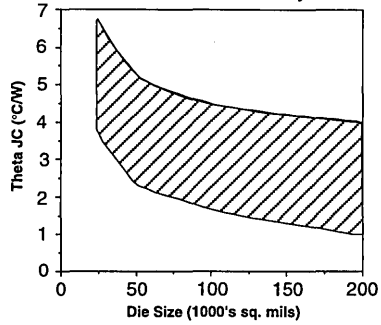
Theta JA - Still Air 22-40 Ceramic Dips



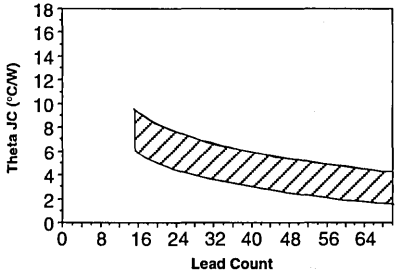
Theta JA Ceramic Flatpacks/Cerpacks



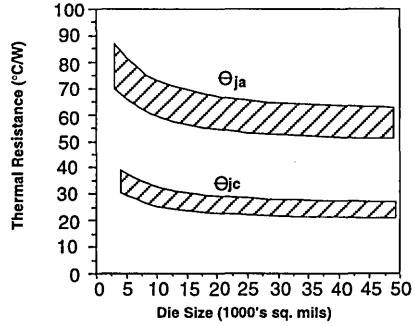
Theta JC Pin Grid Arrays



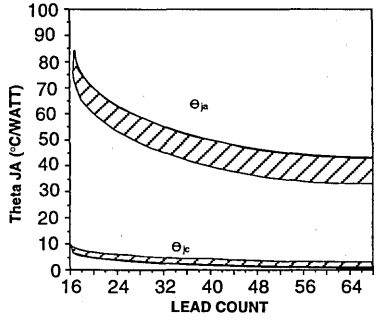
Theta JC Ceramic Flatpacks/Cerpacks



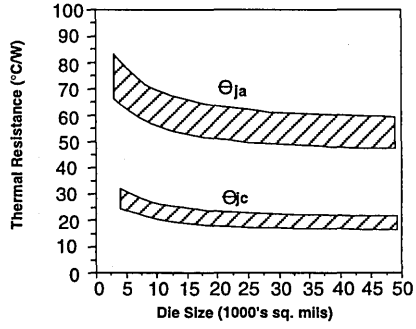
PLASTIC DIPS: 16,18 & 20 PINS



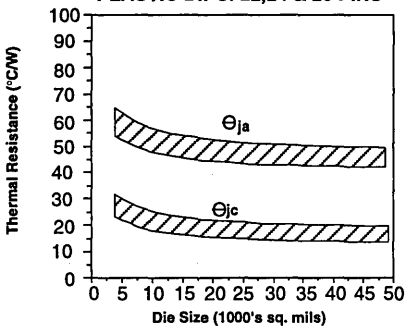
Thermal Resistance of Ceramic LCC's



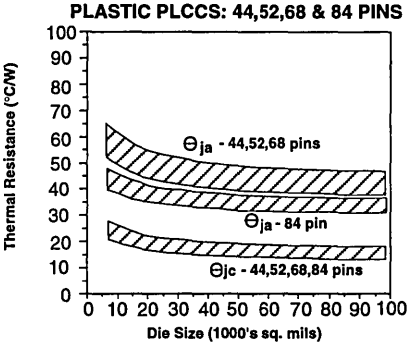
PLASTIC SOICS: 24,28 & 32 PINS



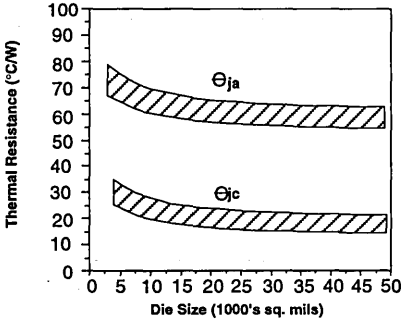
PLASTIC DIPS: 22,24 & 28 PINS



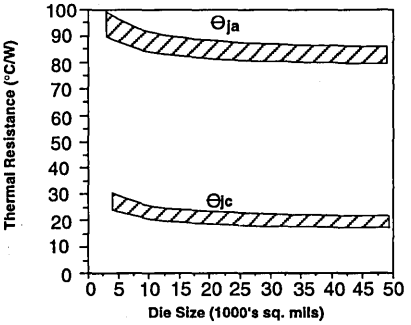
PLASTIC PLCCS: 44,52,68 & 84 PINS



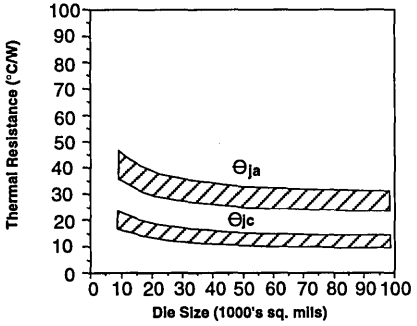
PLASTIC PLCCS: 28 & 32 PINS



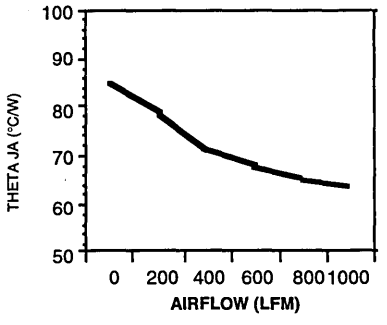
PLASTIC SOICS: 16 & 20 PINS



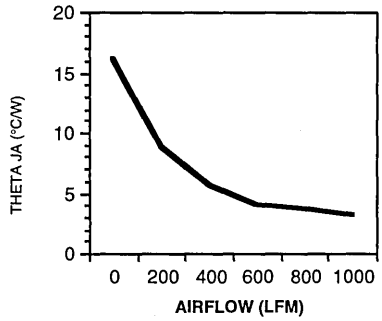
PLASTIC DIPS: 40,48 & 64 PINS



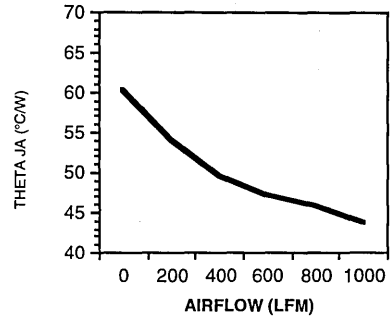
PA 56 THETA JA VS. AIRFLOW



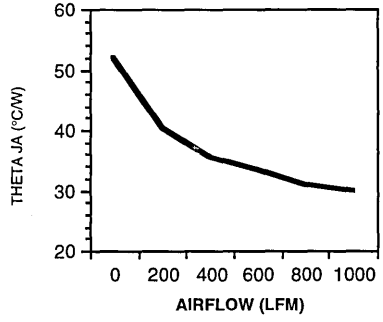
GD 447 THETA JA VS. AIRFLOW



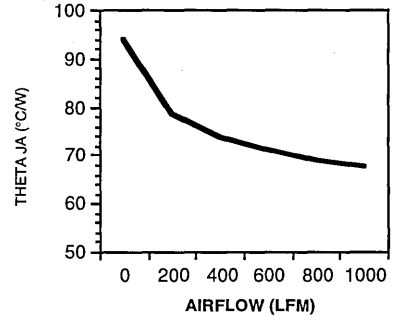
PV 56 THETA JA VS. AIRFLOW



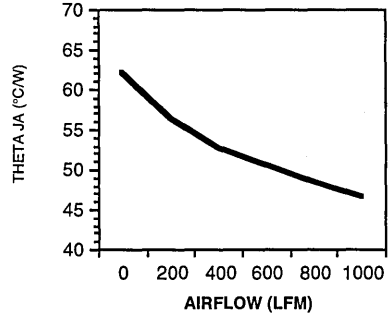
TQFP 64 THETA JA VS. AIRFLOW



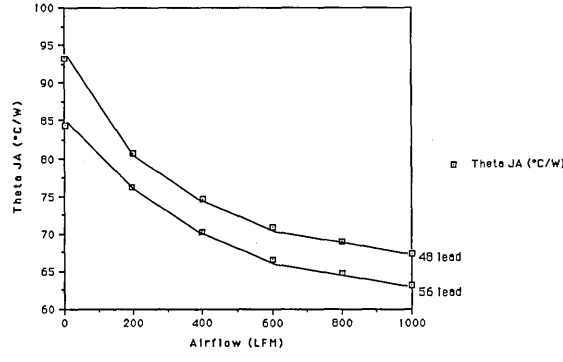
PA 48 THETA JA VS. AIRFLOW



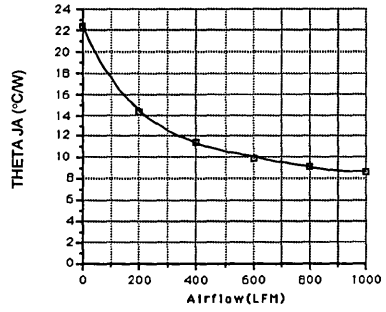
PV 48 THETA JA VS. AIRFLOW



Theta JA vs. Airflow
48/56 lead (.150 body) SSOP

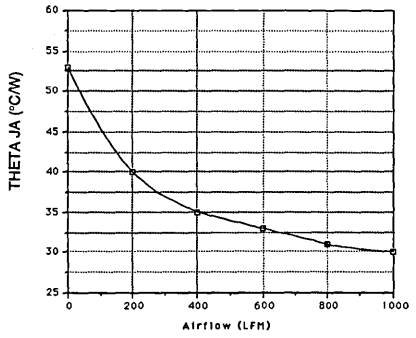


Theta JA vs. Airflow
84/160/208 lead MQUAD flatpack
28mm body

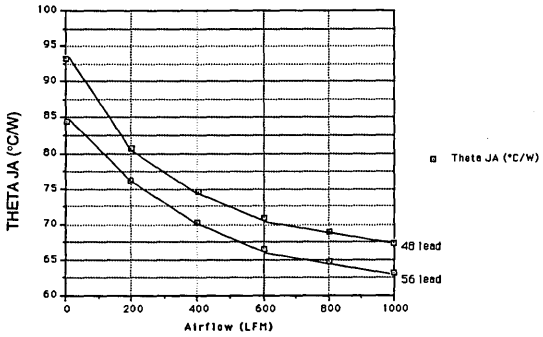


This data is with all leads soldered. .250"sq. Delco Temp09 thermal die.

Theta JA vs. Airflow
64/80/100 lead Thin Quad Flatpack
(14mm body)



Theta JA vs. Airflow
48/56 lead (.150 body) SSOP



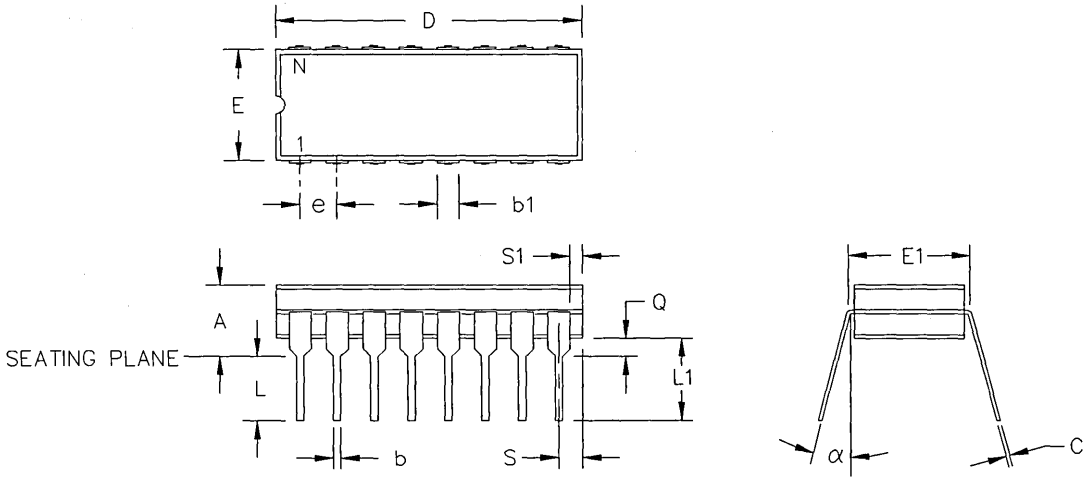
4

PACKAGE DIAGRAM OUTLINE INDEX

Integrated Device Technology, Inc.

PACKAGE DIAGRAM OUTLINES

DUAL IN-LINE PACKAGES



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. THE MINIMUM LIMIT FOR DIMENSION b1 MAY BE .023 FOR CORNER LEADS.

16-28 LEAD CERDIP (300 MIL)

DWG #	D16-1		D18-1		D20-1		D22-1		D24-1		D28-3	
# OF LDS (N)	16		18		20		22		24		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200	.140	.200
b	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021	.015	.021
b1	.045	.060	.045	.060	.045	.060	.045	.060	.045	.065	.045	.065
C	.009	.012	.009	.012	.009	.012	.009	.012	.009	.014	.009	.014
D	.750	.830	.880	.930	.935	1.060	1.050	1.080	1.240	1.280	1.440	1.485
E	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310	.285	.310
E1	.290	.320	.290	.320	.290	.320	.300	.320	.300	.320	.300	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175	.125	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.055	.015	.055	.015	.060	.015	.060	.015	.060	.015	.060
S	.020	.080	.020	.080	.020	.080	.020	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°

DUAL IN-LINE PACKAGES (Continued)

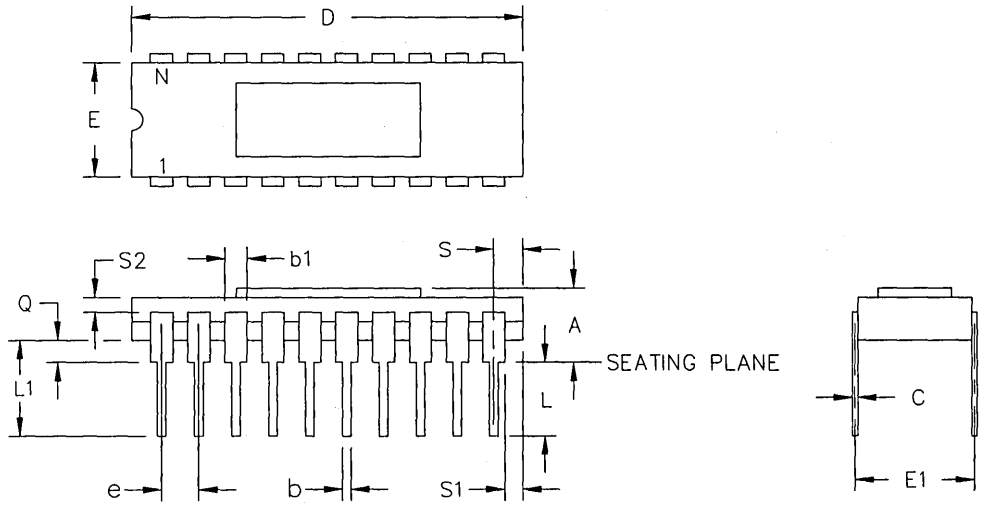
24-40 LEAD CERDIP (400 & 600 MIL)

DWG #	D24-3		D24-2		D28-1		D40-1	
# OF LDS (N)	24		24		28		40	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.130	.175	.090	.190	.090	.200	.160	.220
b	.015	.021	.014	.023	.014	.023	.014	.023
b1	.045	.065	.045	.060	.045	.065	.045	.065
C	.009	.014	.008	.012	.008	.014	.008	.014
D	1.180	1.250	1.230	1.290	1.440	1.490	2.020	2.070
E	.350	.410	.500	.610	.510	.600	.510	.600
E1	.380	.420	.590	.620	.590	.620	.590	.620
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.175	.125	.200	.125	.200	.125	.200
L1	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.020	.060	.020	.060
S	.030	.070	.030	.080	.030	.080	.030	.080
S1	.005	–	.005	–	.005	–	.005	–
α	0°	15°	0°	15°	0°	15°	0°	15°

32 LEAD CERDIP (WIDE BODY)

DWG #	D32-1	
# OF LDS (N)	32	
SYMBOL	MIN	MAX
A	.120	.210
b	.014	.023
b1	.045	.065
C	.008	.014
D	1.625	1.675
E	.570	.600
E1	.590	.620
e	.100 BSC	
L	.125	.200
L1	.150	–
Q	.020	.060
S	.030	.080
S1	.005	–
α	0°	15°

DUAL IN-LINE PACKAGES (Continued)

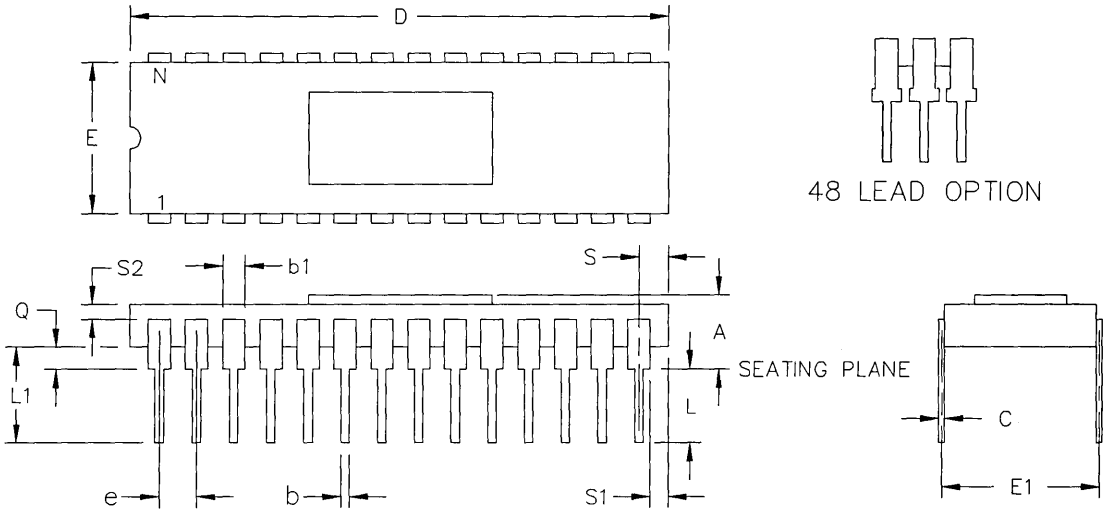


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20-32 LEAD SIDE BRAZE DIP (300 MIL)

DWG #	C20-1		C22-1		C24-1		C28-1		C32-3	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.100	.200	.090	.200	.090	.200	.090	.200
b	.014	.023	.014	.023	.015	.023	.014	.023	.014	.023
b1	.045	.060	.045	.060	.045	.060	.045	.060	.045	.060
C	.008	.015	.008	.015	.008	.015	.008	.015	.008	.014
D	.970	1.060	1.040	1.120	1.180	1.230	1.380	1.420	1.580	1.640
E	.260	.310	.260	.310	.220	.310	.220	.310	.280	.310
E1	.290	.320	.290	.320	.290	.320	.290	.320	.290	.320
e	.100 BSC		.100 BSC		.100 BSC		.100 BSC		.100 BSC	
L	.125	.200	.125	.200	.125	.200	.125	.200	.100	.175
L1	.150	–	.150	–	.150	–	.150	–	.150	–
Q	.015	.060	.015	.060	.015	.060	.015	.060	.030	.060
S	.030	.065	.030	.065	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)

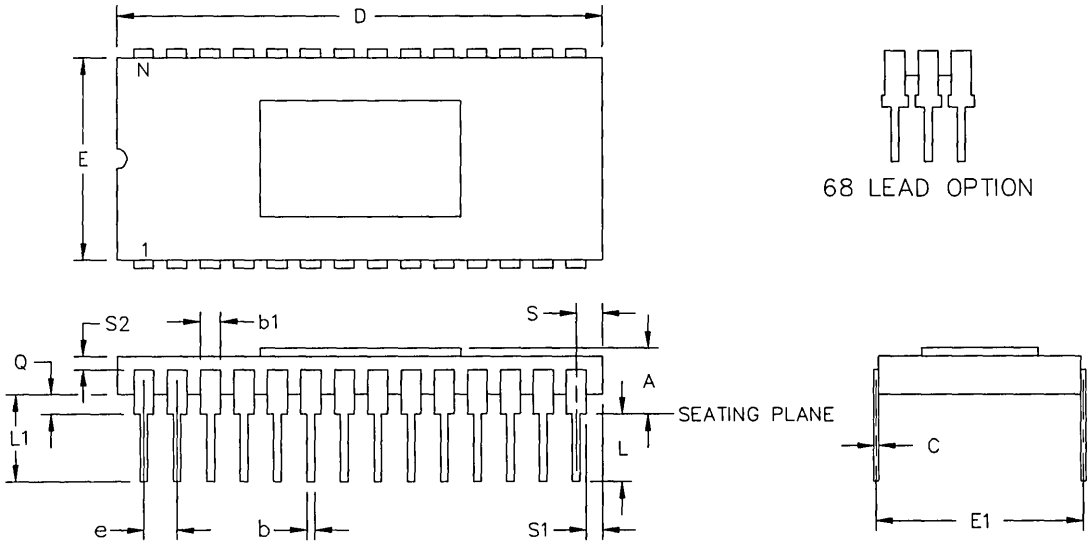


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

28-48 LEAD SIDE BRAZE DIP (400 MIL)

DWG #	C28-2		C32-2		C48-1	
# OF LDS (N)	28		32		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX
A	.090	.200	.090	.200	.085	.190
b	.014	.023	.014	.023	.014	.023
b1	.045	.060	.045	.060	.045	.060
C	.008	.014	.008	.014	.008	.014
D	1.380	1.420	1.580	1.640	1.690	1.730
E	.380	.420	.380	.410	.380	.410
E1	.390	.420	.390	.420	.390	.420
e	.100 BSC		.100 BSC		.070 BSC	
L	.100	.175	.100	.175	.125	.175
L1	.150	–	.150	–	.150	–
Q	.030	.060	.030	.060	.020	.070
S	.030	.065	.030	.065	.030	.065
S1	.005	–	.005	–	.005	–
S2	.005	–	.005	–	.005	–

DUAL IN-LINE PACKAGES (Continued)



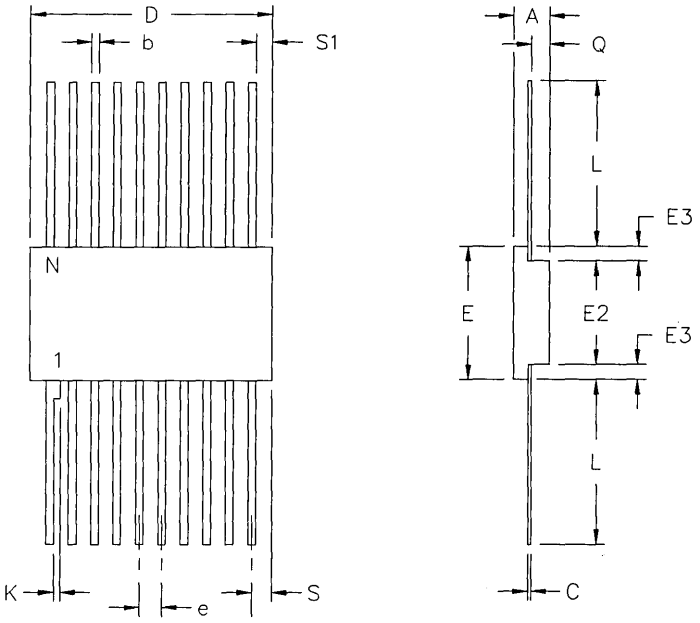
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

48 & 68 LD SIDE BRAZE (600 MIL)

DWG #	C48-2		C68-1	
# OF LDS (N)	48		68	
SYMBOL	MIN	MAX	MIN	MAX
A	.100	.190	.085	.190
b	.015	.023	.015	.023
b1	.045	.060	.045	.060
C	.008	.012	.008	.012
D	2.370	2.430	2.380	2.440
E	.550	.610	.580	.610
E1	.595	.620	.590	.620
e	.100 BSC		.070 BSC	
L	.125	.175	.125	.175
L1	.150	–	.150	–
Q	.020	.060	.020	.070
S	.030	.065	.030	.065
S1	.005	–	.005	–
S2	.005	–	.005	–

FLATPACKS

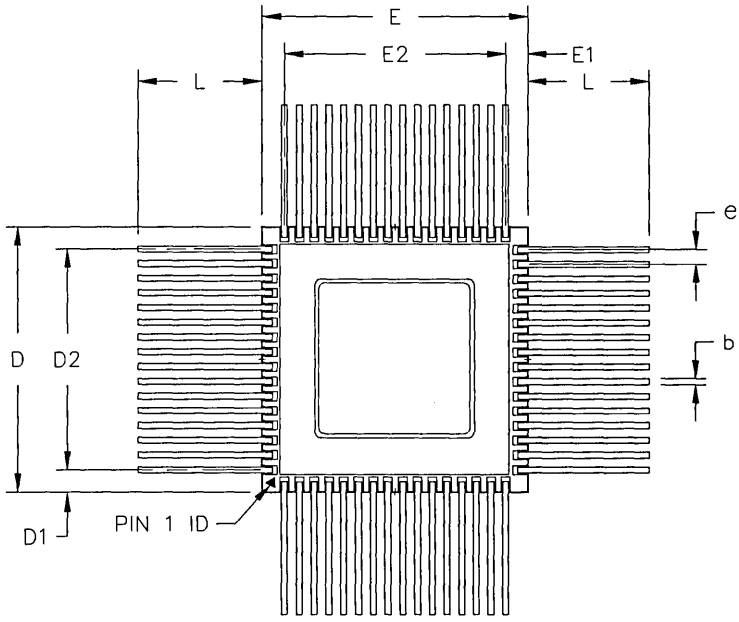
20–28 LEAD FLATPACK

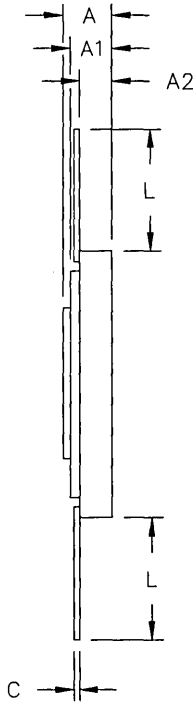


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

DWG #	F20–1		F20–2		F24–1		F28–1		F28–2	
# OF LDS (N)	20		20 (.295 BODY)		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.045	.092	.045	.092	.045	.090	.045	.090	.045	.115
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.004	.007	.004	.007	.004	.007	.004	.007	.004	.007
D	–	.540	–	.540	–	.640	.710	.740	.710	.740
E	.340	.360	.245	.303	.360	.420	.480	.520	.480	.520
E2	.130	–	.130	–	.180	–	.180	–	.180	–
E3	.030	–	.030	–	.030	–	.040	–	.040	–
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.006	.015	.008	.015	–	–	–	–	–	–
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.010	.040	.010	.040	.010	.040	.010	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.000	–	.005	–	.005	–	.005	–	.005	–

FLATPACKS (Continued)





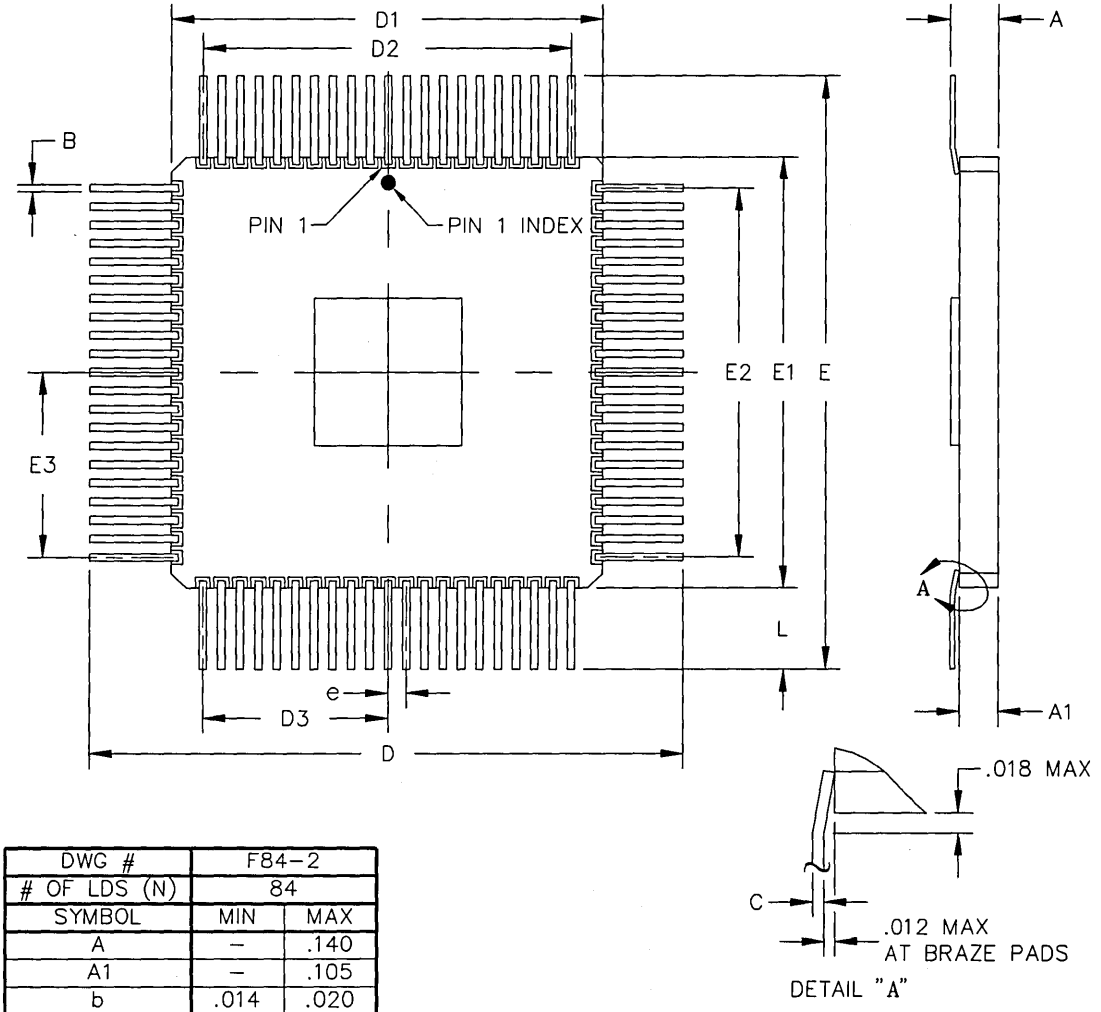
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

48–64 LEAD QUAD FLATPACK

DWG #	F48–1		F64–1	
# OF LDS (N)	48		64	
SYMBOL	MIN	MAX	MIN	MAX
A	.089	.108	.070	.090
A1	.079	.096	.054	.078
A2	.058	.073	.030	.045
b	.018	.022	.016	.020
C	.008	.010	.009	.012
D/E	–	.750	.885	.915
D1/E1	.100 REF		.075 REF	
D2/E2	.550 BSC		.750 BSC	
e	.050 BSC		.050 BSC	
L	.350	.450	.350	.450
ND/NE	12		16	

FLATPACKS (Continued)

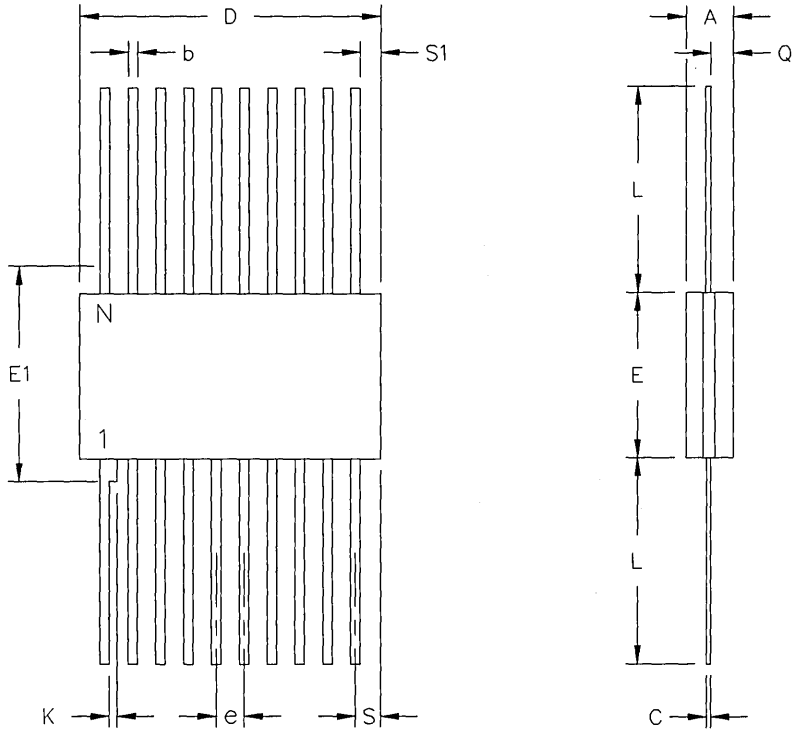
84 LEAD QUAD FLATPACK (CAVITY UP)



DWG #	F84-2	
# OF LDS (N)	84	
SYMBOL	MIN	MAX
A	–	.140
A1	–	.105
b	.014	.020
C	.007	.013
D/E	1.940	1.960
D1/E1	1.130	1.170
D2/E2	1.000 BSC	
D3/E3	.500 BSC	
e	.050 BSC	
L	.350	.450
ND/NE	21	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

CERPACKS

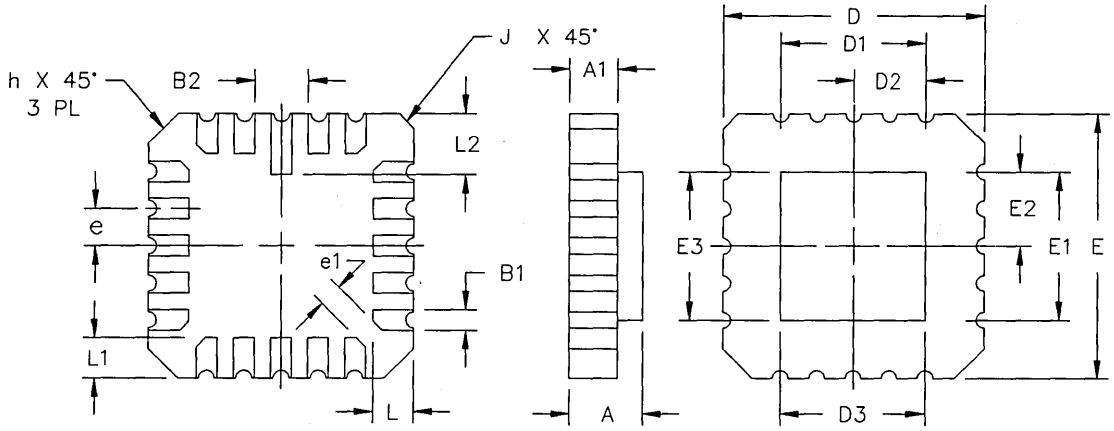


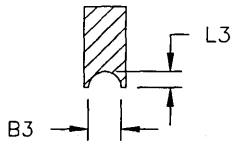
NOTES:
1. ALL DIMENSION ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

16–28 LEAD CERPACK

DWG #	E16–1		E20–1		E24–1		E28–1		E28–2	
# OF LDS (N)	16		20		24		28		28	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.085	.045	.092	.045	.090	.045	.115	.045	.090
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.0045	.006	.0045	.006	.0045	.006	.0045	.006	.0045	.006
D	.370	.430	–	.540	–	.640	–	.740	–	.740
E	.245	.285	.245	.300	.300	.420	.460	.520	.340	.380
E1	–	.305	–	.305	–	.440	–	.550	–	.400
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
Q	.026	.040	.026	.040	.026	.040	.026	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.005	–	.005	–	.005	–	.000	–	.005	–

LEADLESS CHIP CARRIERS





NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

20–48 LEAD LCC (SQUARE)

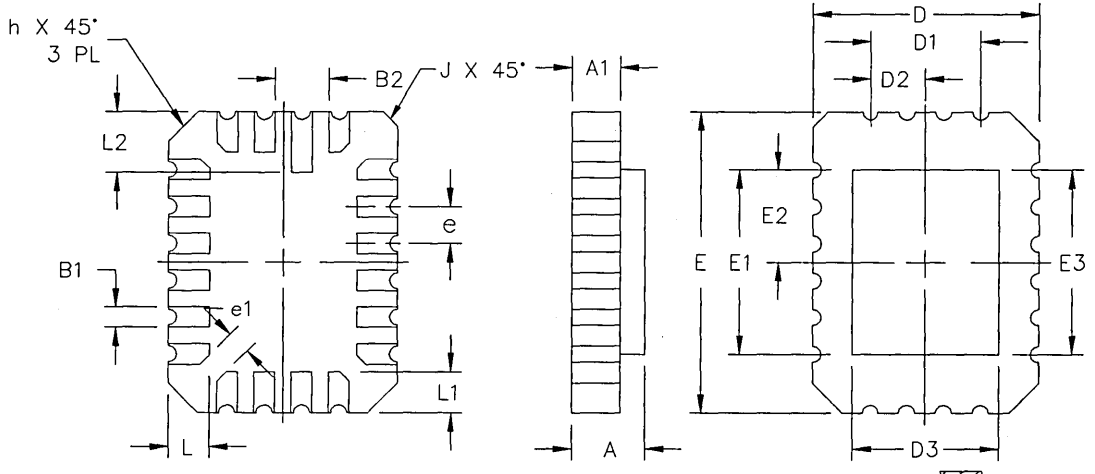
DWG #	L20–2		L28–1		L44–1		L48–1	
# OF LDS (N)	20		28		44		48	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.064	.100	.064	.100	.064	.120	.055	.120
A1	.054	.066	.050	.088	.054	.088	.045	.090
B1	.022	.028	.022	.028	.022	.028	.017	.023
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.342	.358	.442	.460	.640	.660	.554	.572
D1/E1	.200 BSC		.300 BSC		.500 BSC		.440 BSC	
D2/E2	.100 BSC		.150 BSC		.250 BSC		.220 BSC	
D3/E3	–	.358	–	.460	–	.560	.500	.535
e	.050 BSC		.050 BSC		.050 BSC		.040 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.012 RADIUS	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.033	.047
L1	.045	.055	.045	.055	.045	.055	.033	.047
L2	.077	.093	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	5		7		11		12	

LEADLESS CHIP CARRIERS (Continued)

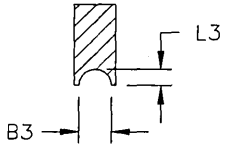
52–68 LEAD LCC (SQUARE)

DWG #	L52–1		L52–2		L68–2		L68–1	
# OF LDS (N)	52		52		68		68	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.061	.087	.082	.120	.082	.120	.065	.120
A1	.051	.077	.072	.088	.072	.088	.055	.075
B1	.022	.028	.022	.028	.022	.028	.008	.014
B2	.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022
D/E	.739	.761	.739	.761	.938	.962	.554	.566
D1/E1	.600 BSC		.600 BSC		.800 BSC		.400 BSC	
D2/E2	.300 BSC		.300 BSC		.400 BSC		.200 BSC	
D3/E3	–	.661	–	.661	–	.862	–	.535
e	.050 BSC		.050 BSC		.050 BSC		.025 BSC	
e1	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.040 REF		.040 REF		.040 REF	
J	.020 REF		.020 REF		.020 REF		.020 REF	
L	.045	.055	.045	.055	.045	.055	.045	.055
L1	.045	.055	.045	.055	.045	.055	.045	.055
L2	.077	.093	.075	.093	.075	.095	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015
ND/NE	13		13		17		17	

LEADLESS CHIP CARRIERS (Continued)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.

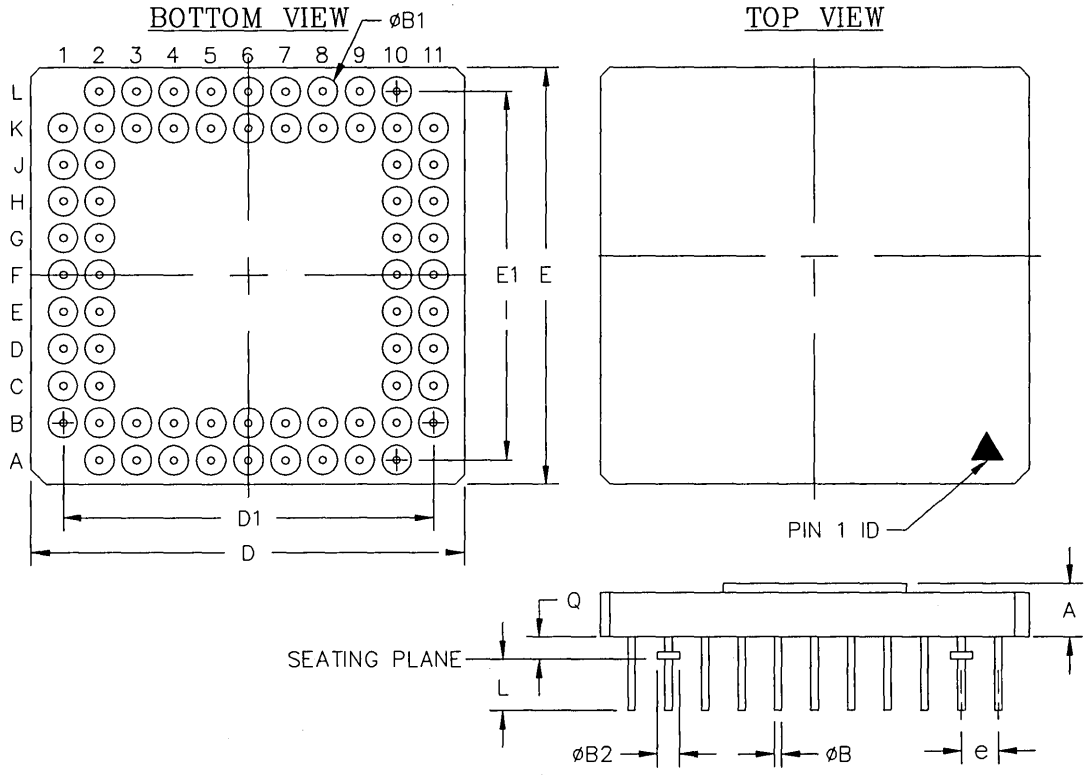


20–32 LEAD LCC (RECTANGULAR)

DWG #	L20–1		L22–1		L24–1		L28–2		L32–1	
# OF LDS (N)	20		22		24		28		32	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.060	.075	.064	.100	.064	.120	.060	.120	.060	.120
A1	.050	.065	.054	.063	.054	.066	.050	.088	.050	.088
B1	.022	.028	.022	.028	.022	.028	.022	.028	.022	.028
B2	.072 REF		.072 REF		.072 REF		.072 REF		.072 REF	
B3	.006	.022	.006	.022	.006	.022	.006	.022	.006	.022
D	.284	.296	.284	.296	.292	.308	.342	.358	.442	.458
D1	.150 BSC		.150 BSC		.200 BSC		.200 BSC		.300 BSC	
D2	.075 BSC		.075 BSC		.100 BSC		.100 BSC		.150 BSC	
D3	–	.280	–	.280	–	.308	–	.358	–	.458
E	.420	.435	.480	.496	.392	.408	.540	.560	.540	.560
E1	.250 BSC		.300 BSC		.300 BSC		.400 BSC		.400 BSC	
E2	.125 BSC		.150 BSC		.150 BSC		.200 BSC		.200 BSC	
E3	–	.410	–	.480	–	.408	–	.558	–	.558
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
e1	.015	–	.015	–	.015	–	.015	–	.015	–
h	.040 REF		.012 RADIUS		.025 REF		.040 REF		.040 REF	
J	.020 REF		.012 RADIUS		.015 REF		.020 REF		.020 REF	
L	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L1	.045	.055	.039	.051	.040	.050	.045	.055	.045	.055
L2	.080	.095	.083	.097	.077	.093	.077	.093	.077	.093
L3	.003	.015	.003	.015	.003	.015	.003	.015	.003	.015
ND	4		4		5		5		7	
NE	6		7		7		9		9	

PIN GRID ARRAYS

68 PIN PGA (CAVITY UP)

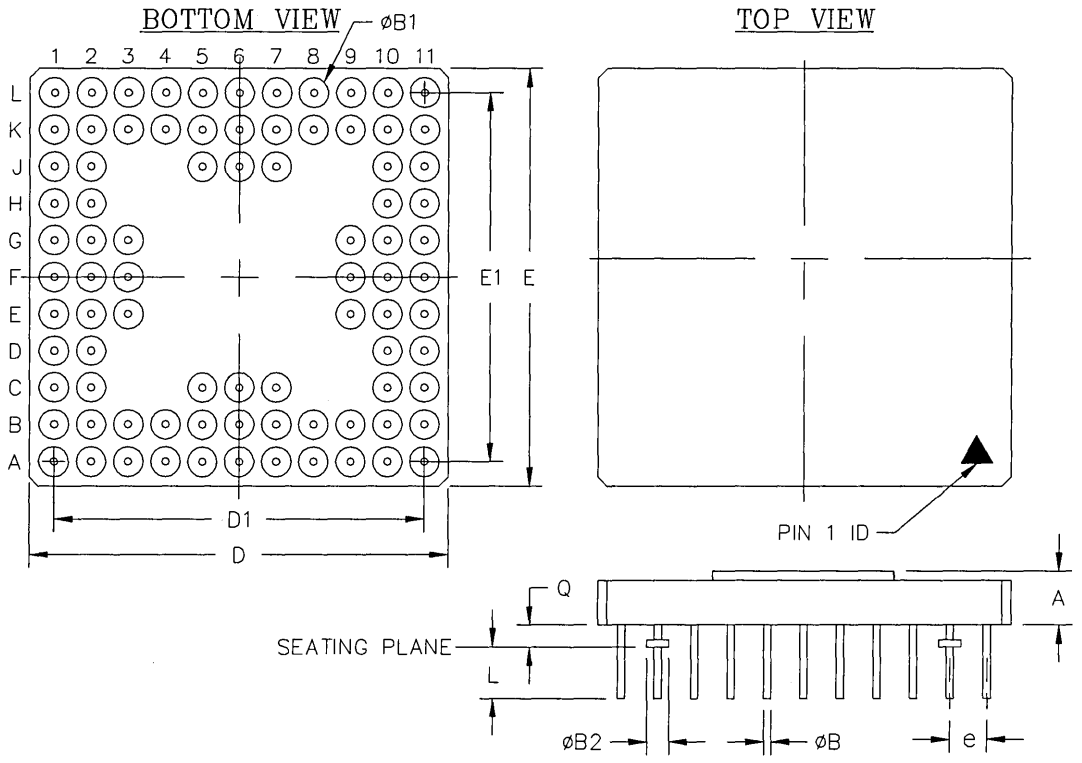


DWG #	G68-1	
# OF PINS (N)	68	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1	–	.080
øB2	.040	.060
D/E	1.140	1.180
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

84 PIN PGA (CAVITY UP – 11 X 11 GRID)

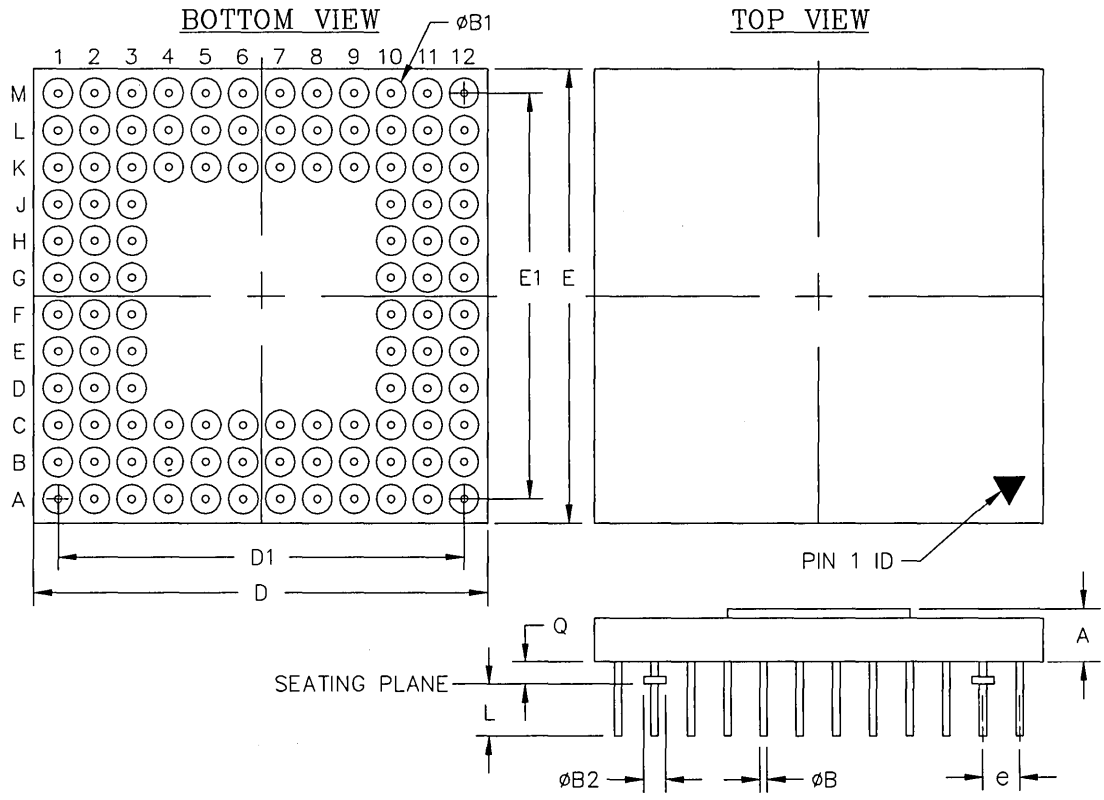


DWG #	G84-3	
# OF PINS (N)	84	
SYMBOL	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1	–	.080
ØB2	.040	.060
D/E	1.080	1.120
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PIN GRID ARRAYS (Continued)

108 PIN PGA (CAVITY UP)

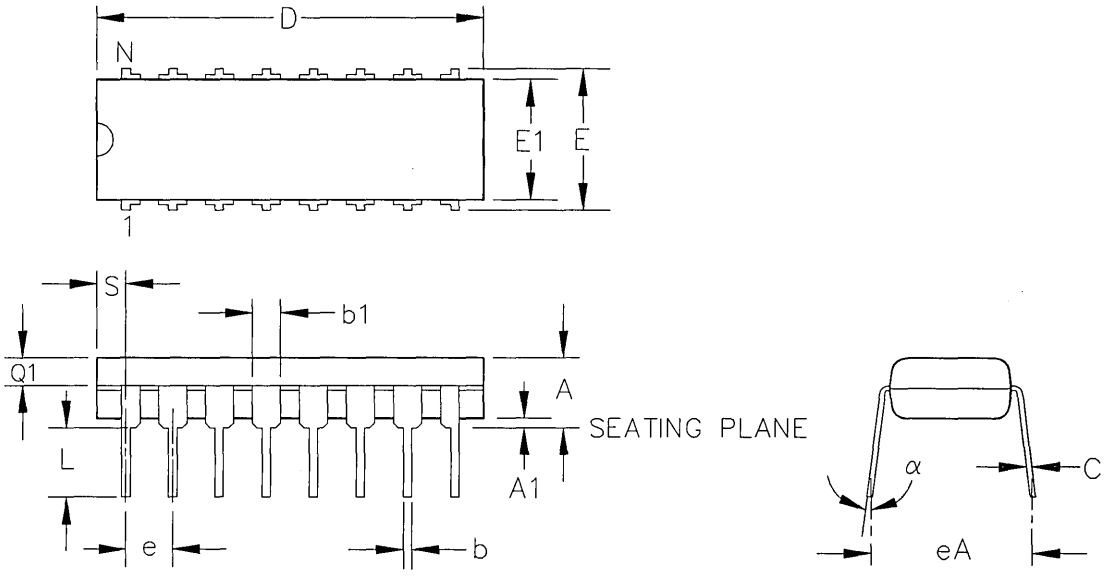


DWG #	G108-1	
# OF PINS (N)	108	
SYMBOL	MIN	MAX
A	.070	.145
ØB	.016	.020
ØB1	–	.080
ØB2	.040	.060
D/E	1.188	1.212
D1/E1	1.100 BSC	
e	.100 BSC	
L	.120	.140
M	12	
Q	.040	.060

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS
5. CHAMFERED CORNERS ARE IDT'S OPTION.

PLASTIC DUAL IN-LINE PACKAGES

16-32 LEAD PLASTIC DIP (300 MIL)

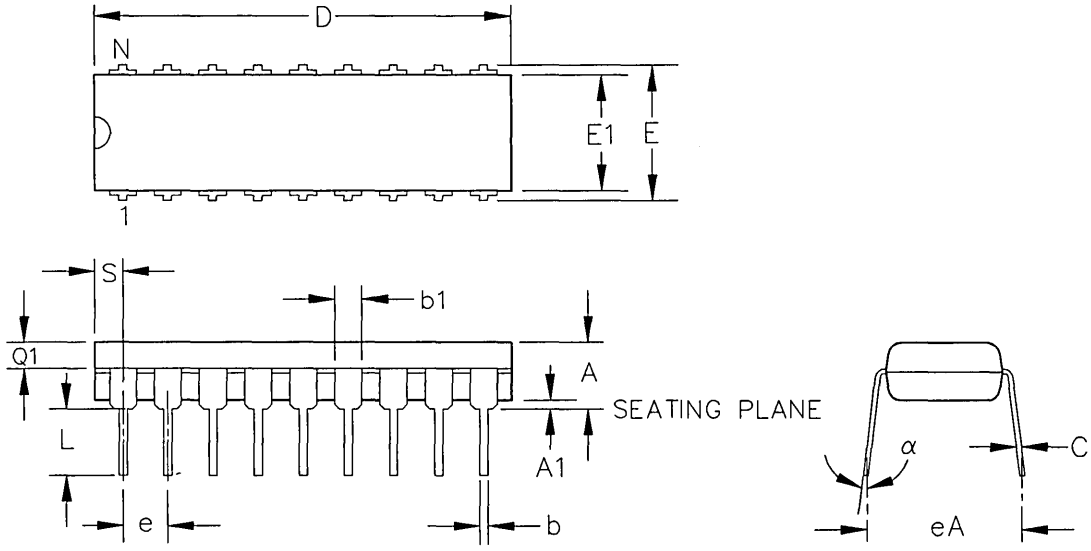


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P16-1		P22-1		P28-2		P32-2	
# OF LDS (N)	16		22		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.180	.145	.180
A1	.015	.035	.015	.035	.015	.030	.015	.030
b	.015	.022	.015	.022	.015	.022	.016	.022
b1	.050	.070	.050	.065	.045	.060	.045	.060
C	.008	.012	.008	.012	.008	.015	.008	.015
D	.745	.760	1.050	1.060	1.345	1.385	1.545	1.585
E	.300	.325	.300	.320	.300	.325	.300	.325
E1	.247	.260	.240	.270	.270	.295	.275	.295
e	.090	.110	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.400	.310	.400
L	.120	.150	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°
S	.015	.035	.020	.040	.020	.042	.020	.060
Q1	.050	.070	.055	.075	.055	.065	.055	.065

PLASTIC DUAL IN-LINE PACKAGES (Continued)

18-24 LEAD PLASTIC DIP (300 MIL - FULL LEAD)

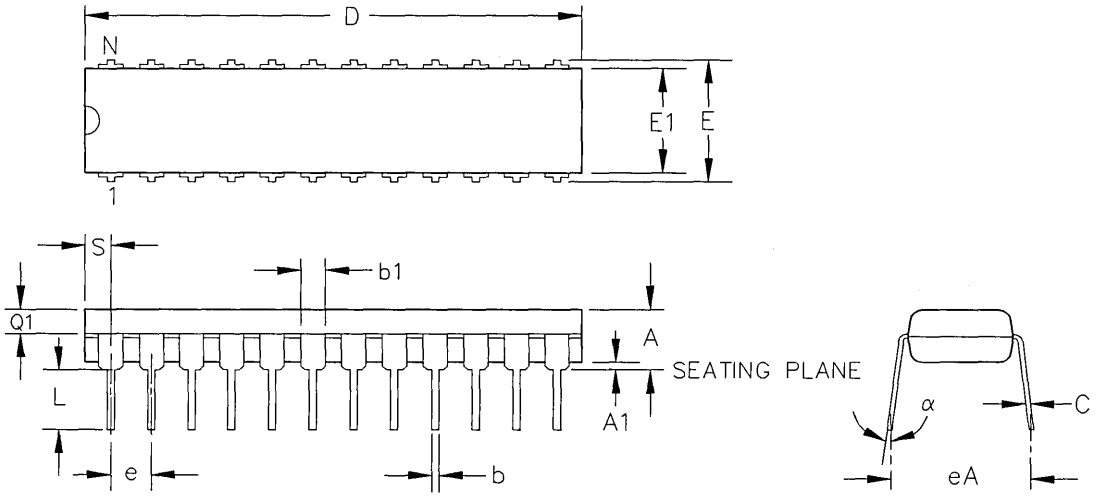


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DWG #	P18-1		P20-1		P24-1	
# OF LDS (N)	18		20		24	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX
A	.140	.165	.145	.165	.145	.165
A1	.015	.035	.015	.035	.015	.035
b	.015	.020	.015	.020	.015	.020
b1	.050	.070	.050	.070	.050	.065
C	.008	.012	.008	.012	.008	.012
D	.885	.910	1.022	1.040	1.240	1.255
E	.300	.325	.300	.325	.300	.320
E1	.247	.260	.240	.280	.250	.275
e	.090	.110	.090	.110	.090	.110
eA	.310	.370	.310	.370	.310	.370
L	.120	.150	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°
S	.040	.060	.025	.070	.055	.075
Q1	.050	.070	.055	.075	.055	.070

PLASTIC DUAL IN-LINE PACKAGES (Continued)

24-48 LEAD PLASTIC DIP (600 MIL)

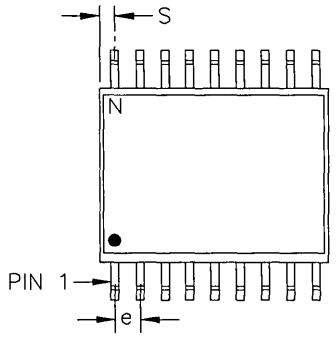


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. D & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

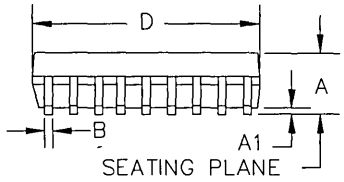
DWG #	P24-2		P28-1		P32-1		P40-1		P48-1	
# OF LEADS (N)	24		28		32		40		48	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.160	.185	.160	.185	.170	.190	.160	.185	.170	.200
A1	.015	.035	.015	.035	.015	.050	.015	.035	.015	.035
b	.015	.020	.015	.020	.016	.020	.015	.020	.015	.020
b1	.050	.065	.050	.065	.045	.055	.050	.065	.050	.065
C	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	1.240	1.260	1.420	1.460	1.645	1.655	2.050	2.070	2.420	2.450
E	.600	.620	.600	.620	.600	.625	.600	.620	.600	.620
E1	.530	.550	.530	.550	.530	.550	.530	.550	.530	.560
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
eA	.610	.670	.610	.670	.610	.670	.610	.670	.610	.670
L	.120	.150	.120	.150	.125	.135	.120	.150	.120	.150
α	0°	15°	0°	15°	0°	15°	0°	15°	0°	15°
S	.060	.080	.055	.080	.070	.080	.070	.085	.060	.075
Q1	.060	.080	.060	.080	.065	.075	.060	.080	.060	.080

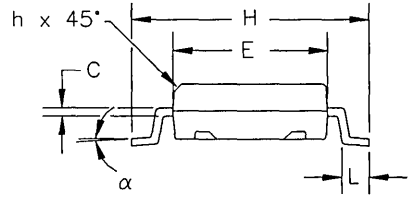
SMALL OUTLINE IC

16-24 LEAD SOIC (GULL WING - JEDEC)



NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC - BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.

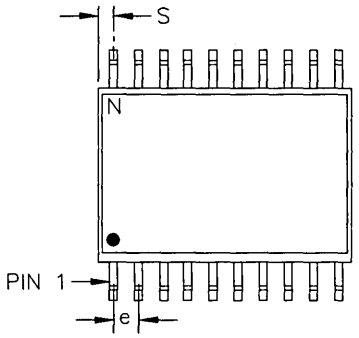




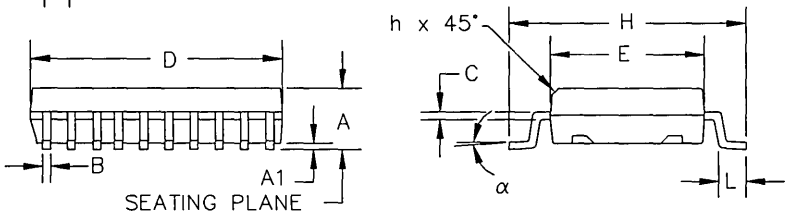
DWG #	SO16-1		SO18-1		SO20-2		SO24-2	
# OF LDS (N)	16 (.300)		18 (.300)		20 (.300")		24 (.300")	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.095	.1043	.095	.1043	.095	.1043	.095	.1043
A1	.005	.0118	.005	.0118	.005	.0118	.005	.0118
B	.014	.020	.014	.020	.014	.020	.014	.020
C	.0091	.0125	.0091	.0125	.0091	0125	.0091	.0125
D	.403	.413	.447	.462	.497	.511	.600	.614
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC	
E	.292	.2992	.292	.2992	.292	.2992	.292	.2992
h	.010	.020	.010	.020	.010	.020	.010	.020
H	.400	.419	.400	.419	.400	.419	.400	.419
L	.018	.045	.018	.045	.018	.045	.018	.045
α	0°	8°	0°	8°	0°	8°	0°	8°
S	.023	.035	.023	.035	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)

28 LEAD SOIC (GULL WING – JEDEC)



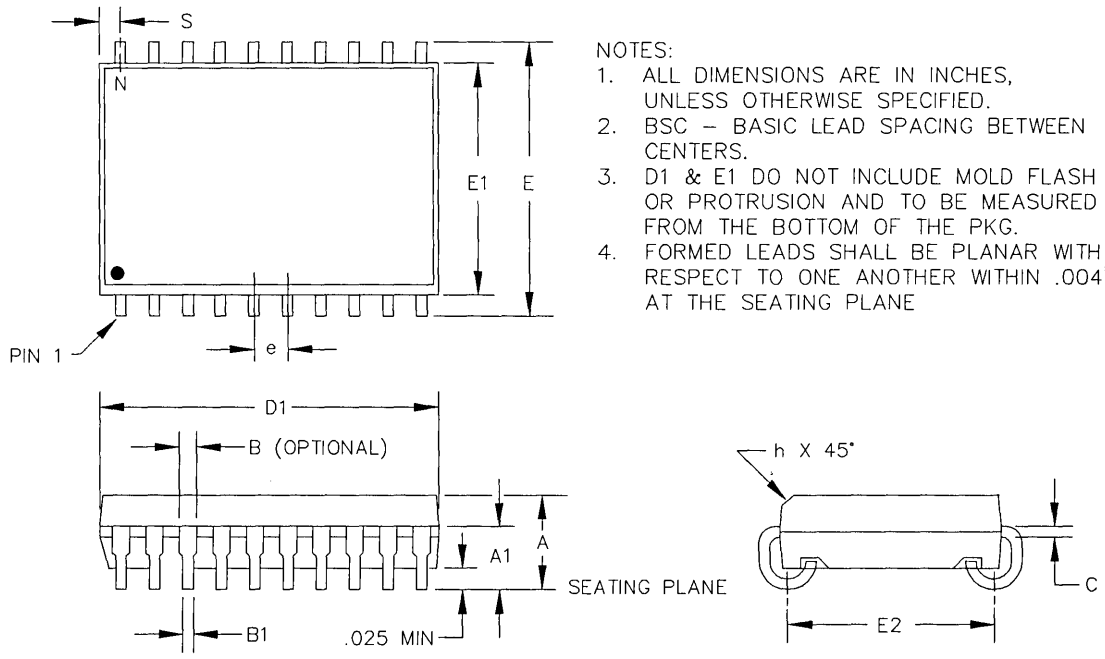
NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.



DWG #	SO28-2		SO28-3	
# OF LDS (N)	28 (.300")		28 (.330")	
SYMBOL	MIN	MAX	MIN	MAX
A	.095	.1043	.110	.120
A1	.005	.0118	.005	.014
B	.014	.020	.014	.019
C	.0091	.0125	.006	.010
D	.700	.712	.718	.728
e	.050 BSC		.050 BSC	
E	.292	.2992	.340	.350
h	.010	.020	.012	.020
H	.400	.419	.462	.478
L	.018	.045	.028	.045
α	0°	8°	0°	8°
S	.023	.035	.023	.035

SMALL OUTLINE IC (Continued)

20-32 LEAD SOIC (J-BEND, 300 MIL)

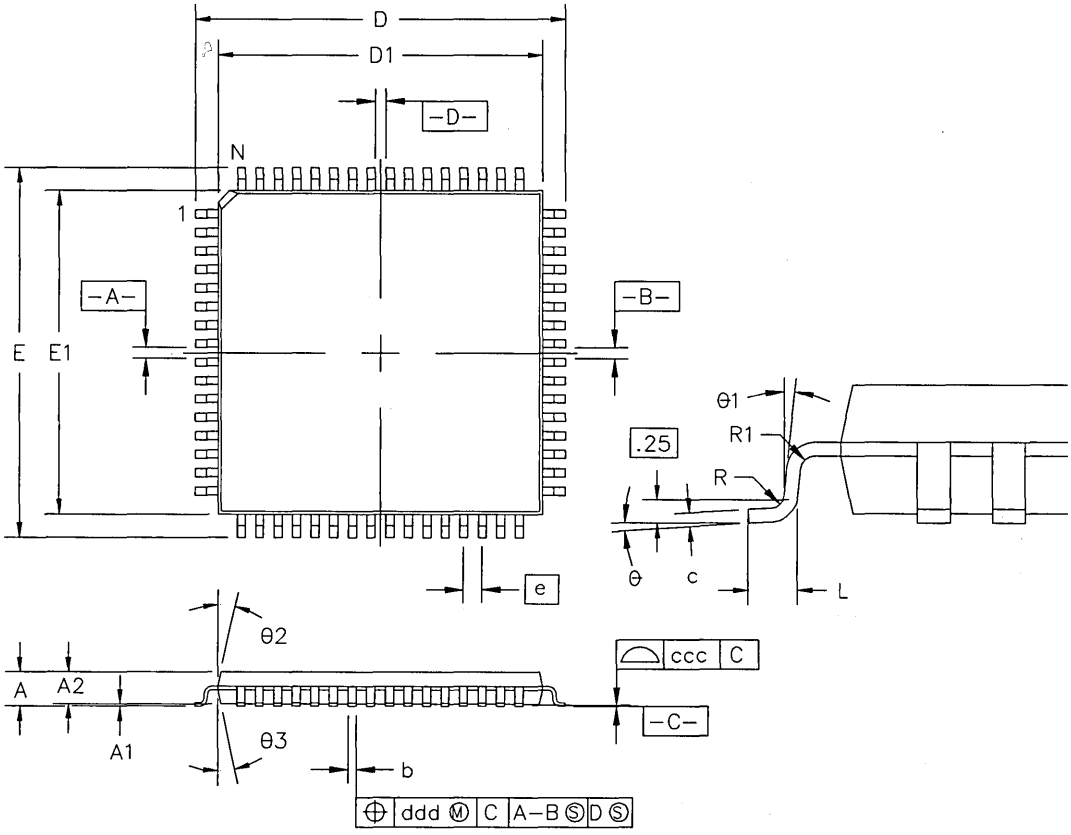


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PKG.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE

DWG #	SO20-1		SO24-4		SO24-8		SO28-5		SO32-2	
# OF LDS (N)	20		24		24		28		32	
SYMBOLS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.120	.140	.130	.148	.120	.140	.120	.140	.130	.148
A1	.078	.095	.082	.095	.078	.091	.078	.095	.082	.095
B	–	–	.026	.032	–	–	–	–	.026	.032
B1	.014	.020	.015	.020	.014	.019	.014	.020	.016	.020
C	.008	.013	.007	.011	.0091	.0125	.008	.013	.008	.013
D1	.500	.512	.620	.630	.602	.612	.700	.712	.820	.830
E	.335	.347	.335	.345	.335	.347	.335	.347	.330	.340
E1	.292	.300	.295	.305	.292	.299	.292	.300	.295	.305
E2	.262	.272	.260	.280	.262	.272	.262	.272	.260	.275
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
h	.010	.020	.010	.020	.010	.016	.012	.020	.012	.020
S	.023	.035	.032	.043	.032	.043	.023	.035	.032	.043

PLASTIC QUAD FLATPACKS

TQFP



NOTES:
1. ALL DIMENSIONS ARE IN MELLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD PROTRUSION AND TO BE MEASURED FROM THE BOTTOM OF THE PACKAGE. ALLOWABLE PROTRUSION TO BE .254 PER SIDE.

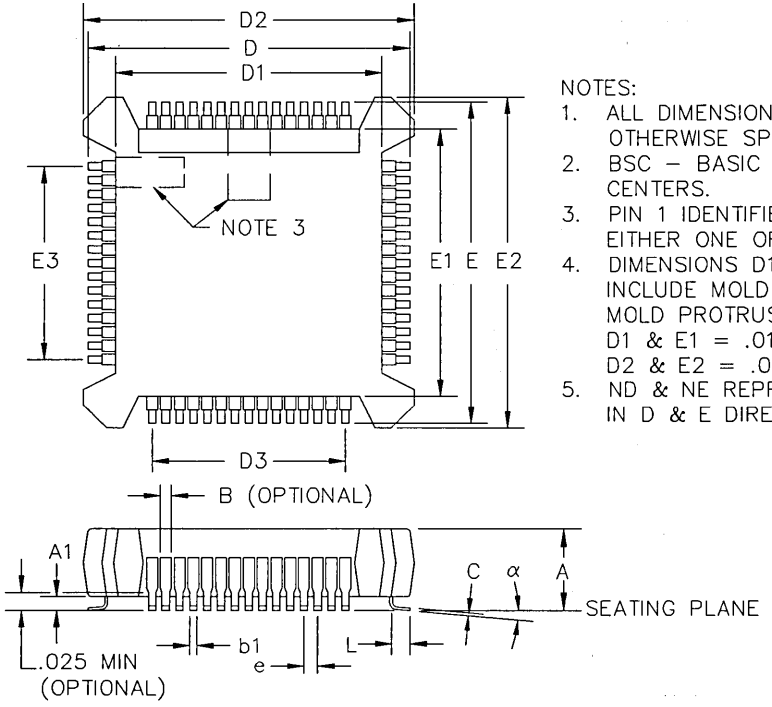
PLASTIC QUAD FLATPACKS (Continued)

64–120 LEAD TQFP

DWG #	PN 64–1		PN 80–1		PN 100–1		PN 120–1	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	–	1.60	–	1.60	–	1.60	–	1.60
A1	.05	.15	.05	.15	.05	.15	.05	.15
A2	1.35	1.45	1.35	1.45	1.35	1.45	1.35	1.45
D	15.75	16.25	15.75	16.25	15.75	16.25	15.75	16.25
D1	13.95	14.05	13.95	14.05	13.95	14.05	13.95	14.05
E	15.75	16.25	15.75	16.25	15.75	16.25	15.75	16.25
E1	13.95	14.05	13.95	14.05	13.95	14.05	13.95	14.05
L	.45	.70	.45	.70	.45	.70	.45	.70
N	64		80		100		120	
e	.80 BSC		.65 BSC		.50 BSC		.40 BSC	
b	.30	.40	.25	.35	.17	.27	.13	.23
ccc	–	.10	–	.10	–	.08	–	.08
ddd	–	.20	–	.13	–	.08	–	.07
R	.08	.20	.08	.20	.08	.20	.08	.20
R1	.08	–	.08	–	.08	–	.08	–
θ	0°	7°	0°	7°	0°	7°	0°	7°
θ1	2°	10°	2°	10°	2°	10°	2°	10°
θ2	11°	13°	11°	13°	11°	13°	11°	13°
θ3	11°	13°	11°	13°	11°	13°	11°	13°
c	.09	.16	.09	.16	.09	.16	.09	.16

PLATIC QUAD FLATPACKS (Continued)

100–132 LEAD PLASTIC QUAD FLATPACK (JEDEC)

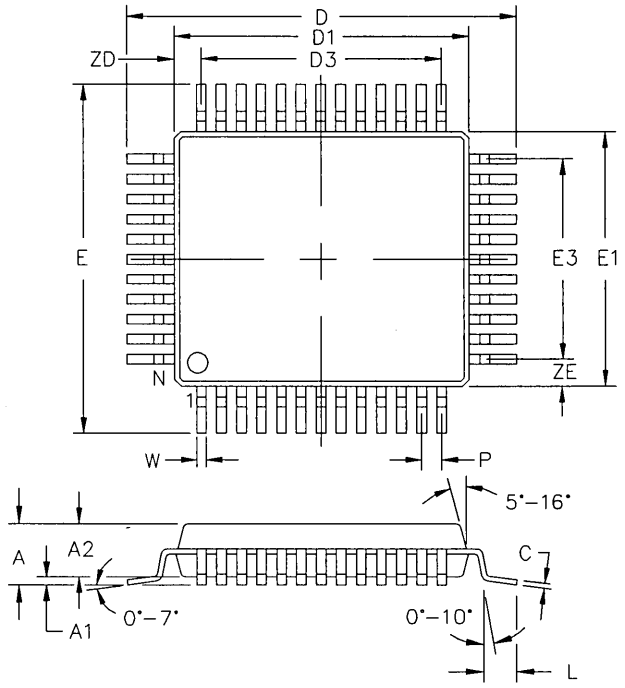


NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. PIN 1 IDENTIFIER CAN BE POSITIONED AT EITHER ONE OF THESE TWO LOCATIONS.
4. DIMENSIONS D1, D2, E1, AND E2 DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE MOLD PROTRUSIONS ARE AS FOLLOWS:
   D1 & E1 = .010 MAX.
   D2 & E2 = .007 MAX.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

DWG #	PQ100–1		PQ132–1	
# OF LDS (N)	100		132	
SYMBOLS	MIN	MAX	MIN	MAX
A	.160	.180	.160	.180
A1	.020	.040	.020	.040
B	.008	.016	.008	.016
b1	.008	.012	.008	.012
C	.0055	.008	.0055	.008
D	.875	.885	1.075	1.085
D1	.747	.753	.947	.953
D2	.897	.903	1.097	1.103
D3	.600 REF		.800 REF	
e	.025 BSC		.025 BSC	
E	.875	.885	1.075	1.085
E1	.747	.753	.947	.953
E2	.897	.903	1.097	1.103
E3	.600 REF		.800 REF	
L	.020	.030	.020	.030
α	0°	8°	0°	8°
ND/NE	25/25		33/33	

PLASTIC QUAD FLATPACKS (Continued)

80 & 100 LEAD RECTANGULAR PLASTIC QUAD FLATPACK (EIAJ)

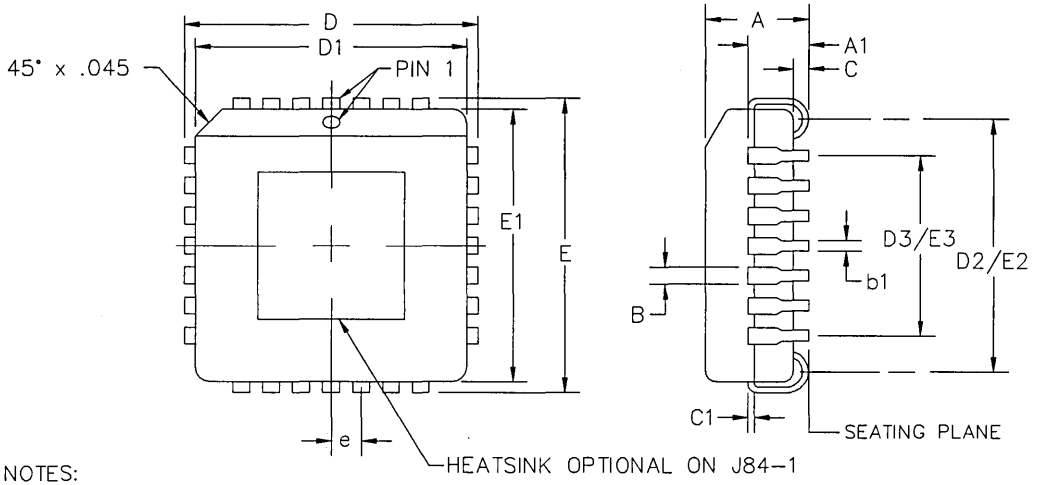


DWG #	PQ80–2		PQ100–2	
# OF LDS (N)	80		100	
SYMBOLS	MIN	MAX	MIN	MAX
A	2.80	3.40	2.80	3.40
A1	.25	–	.25	–
A2	2.54	3.05	2.54	3.05
C	.13	.20	.13	.20
D	23.65	24.15	23.65	24.15
D1	19.90	20.10	19.90	20.10
D3	18.40 REF		18.85 REF	
E	17.65	18.15	17.65	18.15
E1	13.90	14.10	13.90	14.10
E3	12.00 REF		12.35 REF	
L	.65	.95	.65	.95
ND/NE	16/24		20/30	
P	.80 BSC		.65 BSC	
W	.30	.45	.25	.40
ZD	.80		.575	
ZE	1.00		.825	

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D1 & E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .254 PER SIDE.
4. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.

PLASTIC LEADED CHIP CARRIERS

20–84 LEAD PLCC (SQUARE)



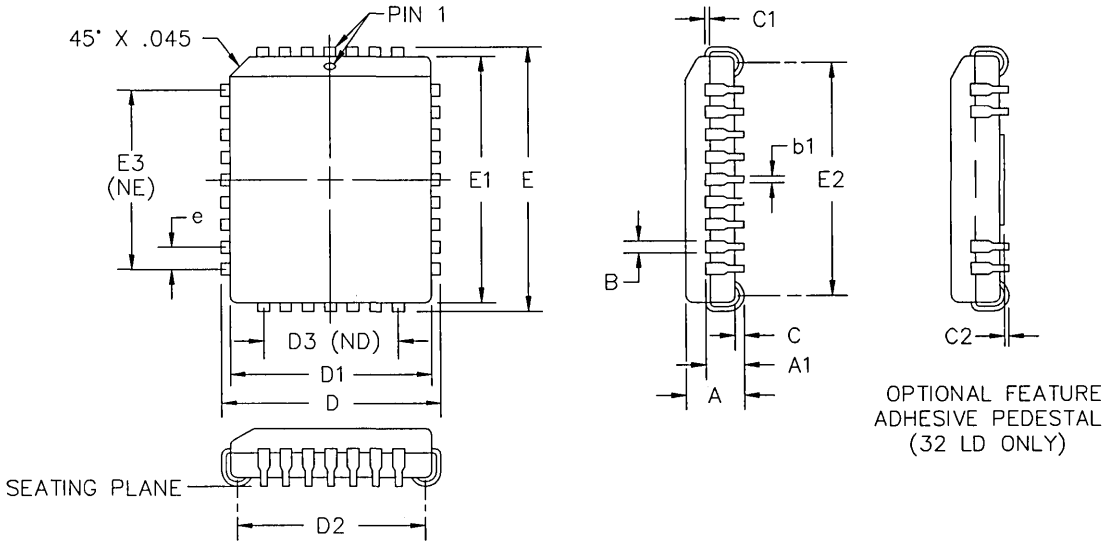
NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBER OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PKG.

DWG #	J20–1		J28–1		J44–1		J52–1		J68–1		J84–1	
# OF LDS	20		28		44		52		68		84	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180	.165	.180
A1	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115	.095	.115
B	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032	.026	.032
b1	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021	.013	.021
C	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040	.020	.040
C1	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012	.008	.012
D	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
D1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
D2/E2	.290	.330	.390	.430	.590	.630	.690	.730	.890	.930	1.090	1.130
D3/E3	.200 REF		.300 REF		.500 REF		.600 REF		.800 REF		1.000 REF	
E	.385	.395	.485	.495	.685	.695	.785	.795	.985	.995	1.185	1.195
E1	.350	.356	.450	.456	.650	.656	.750	.756	.950	.956	1.150	1.156
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
ND/NE	5		7		11		13		17		21	

PLASTIC LEADED CHIP CARRIERS (Continued)

18–32 LEAD PLCC (RECTANGULAR)



DWG #	J18–1		J32–1	
# OF LDS	18		32	
SYMBOL	MIN	MAX	MIN	MAX
A	.120	.140	.120	.140
A1	.075	.095	.075	.095
B	.026	.032	.026	.032
b1	.013	.021	.013	.021
C	.015	.040	.015	.040
C1	.008	.012	.008	.012
C2	–	–	.005	.015
D	.320	.335	.485	.495
D1	.289	.293	.449	.453
D2	.225	.265	.390	.430
D3	.150 REF		.300 REF	
E	.520	.535	.585	.595
E1	.489	.493	.549	.553
E2	.422	.465	.490	.530
E3	.200 REF		.400 REF	
e	.050 BSC		.050 BSC	
ND/NE	4 / 5		7 / 9	

NOTES:
1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE SPECIFIED.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004" AT THE SEATING PLANE.
5. ND & NE REPRESENT NUMBERS OF LEADS IN D & E DIRECTIONS RESPECTIVELY.
6. D1 & E1 SHOULD BE MEASURED FROM THE BOTTOM OF THE PACKAGE.

FIFO MEMORIES

Integration of IDT high-speed static RAM technology with internal support logic yields high-performance, high-density FIFO memories. A FIFO is used as a memory buffer between two asynchronous systems with simultaneous read/write access. The data rate between the two systems can be regulated by monitoring the status flags and throttling the read and write accesses. Since these FIFOs are built with an internal RAM pointer architecture, there is no fall-through time between a write to a memory location and a read from that memory location. System performance is significantly improved over the shift register-based architecture of previous FIFO designs which are handicapped with long fall-through times.

IDT offers the widest selection of monolithic FIFOs, ranging from shallow 64 x 4 and 64 x 5 to the high-density 32K x 9. Shallow FIFOs regulate data flow in tightly coupled computational engines. High-density FIFOs store large blocks in networking, telecommunication and data storage systems. The IDT7200 FIFO family (256 x 9 through the 32K x 9. FIFOs) are all pin and function compatible, making density upgrades simple. All IDT FIFOs can be cascaded to greater word depths and expanded to greater word widths with no external support logic.

IDT's high-speed SyncFIFO™ is ideal for multiprocessor systems, workstations and high-end graphics. The innovative architecture of the SyncFIFO (internal I/O registers with separate clock and enable inputs), along with wider data bus, simplifies design and reduces interface logic.

The Parallel-Serial FIFOs incorporate a serial input or a serial output shifter for serial-to-parallel or parallel-to-serial bus interface. The Parallel-Serial FIFOs also offer six status flags for flexible data throttling.

New product offerings include:

1) a new family of deep, high speed, low cost per bit "Supersyncs" available in x9 (16K-32K) and x18 (8K-16K).
2) a new line of x36-bit wide SyncFIFOs with added functionality including bidirectional data flow, parity generation/check, mailbox capability, and dynamic bus matching.
3) a new family of x1-bit SyncFIFOs for serial data buffering in telecom applications such as Token Ring Networks and Modems.
4) a family of DualSync FIFOs which function as 2 independent FIFOs in space saving 64-pin TQFP (x9) and 121-pin BGA (x18) packages.

A variety of packages are available: standard plastic DIP and CERDIP, surface mount ceramic LCC, PLCC and SOIC, and high-reliability flatpack. Increasing board density is the overwhelming goal of IDT's package development efforts, as demonstrated by the introduction of the 300-mil ThinDIP, the 64-pin Thin Quad Flatpack (TQFP), the 121-pin Ball Grid Array (BGA) and our latest new package offering—the 64-pin Slim Thin Quad Flatpack (STQFP) which allows us to offer x18 SyncFIFOs and our SuperSyncs in a 144 square mil surface mount package..

FIFO modules, composed of four LCC devices mounted on a multi-layer co-fired ceramic substrate, increase densities to 32K x 18 which are pin-compatible with current monolithic versions.

IDT is committed to offering FIFOs of increasing density, speed and enhanced architectural innovations, such as Flexishift™ and the BiFIFO, for easier system interface.

TABLE OF CONTENTS

FIFO MODULES

Please refer to Subsystems Products listing for FIFO Modules.

Integrated Device Technology, Inc.

155 Mbps ATM SAR CONTROLLER FOR PCI-BASED NETWORKING APPLICATIONS

ADVANCED INFORMATION
IDT77201

KEY FEATURES

- Full-duplex Segmentation and Reassembly (SAR) at 155 Mbps "wire-speed" (310 Mbps aggregate speed).
- Performs ATM layer protocol functions.
- Supports AAL5, AAL3/4, "AAL0" and "Raw Cell" formats.
- Supports Constant Bit Rate (CBR), Available Bit Rate (ABR), Variable Bit Rate (VBR) and Unassigned Bit Rate (UBR) service classes.
- Reassembles received CS-PDUs directly into host memory.
- Segments CS-PDUs ready for transmission directly from host memory.
- PCI bus master interface for efficient, low latency DMA transfers with host system.
- Operates with ATM networks up to 155.52 Mbps.
- Up to 16 million open transmit connections.
- Up to 16K simultaneous receive connections.
- Glue-less integration to host system's PCI bus.
- UTOPIA Interface to PHY.
- Utility & Management Interface to PHY.
- Standalone controller: embedded processor not required.
- Supports high-performance, lowest-cost ATM NIC solution.
- Programming Manual available upon request.

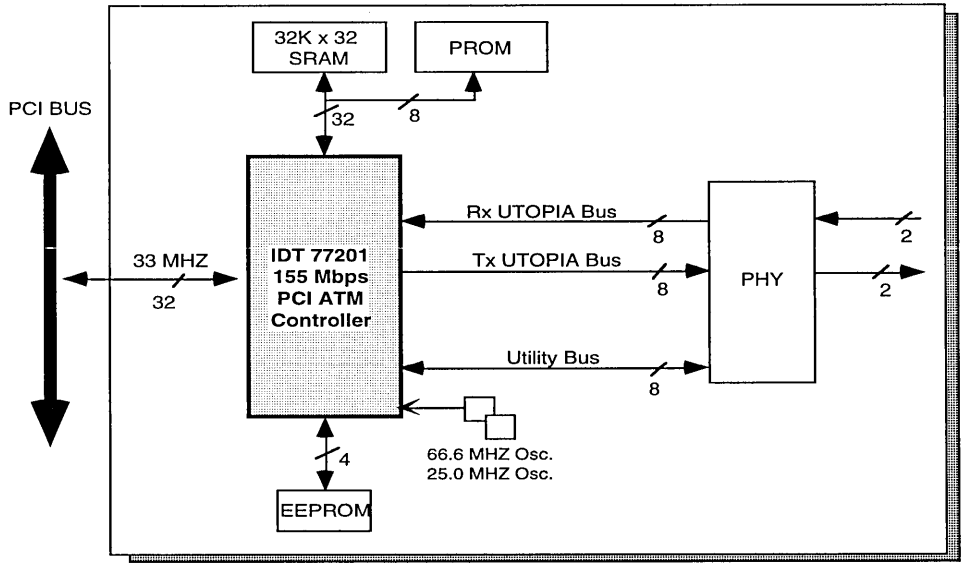
DESCRIPTION

The IDT77201 NICStAR™ is a member of IDT's family of products for Asynchronous Transfer Mode (ATM) networks. The NICStAR performs both the ATM Adaption Layer (AAL) Segmentation and Reassembly (SAR) function and the ATM layer protocol functions.

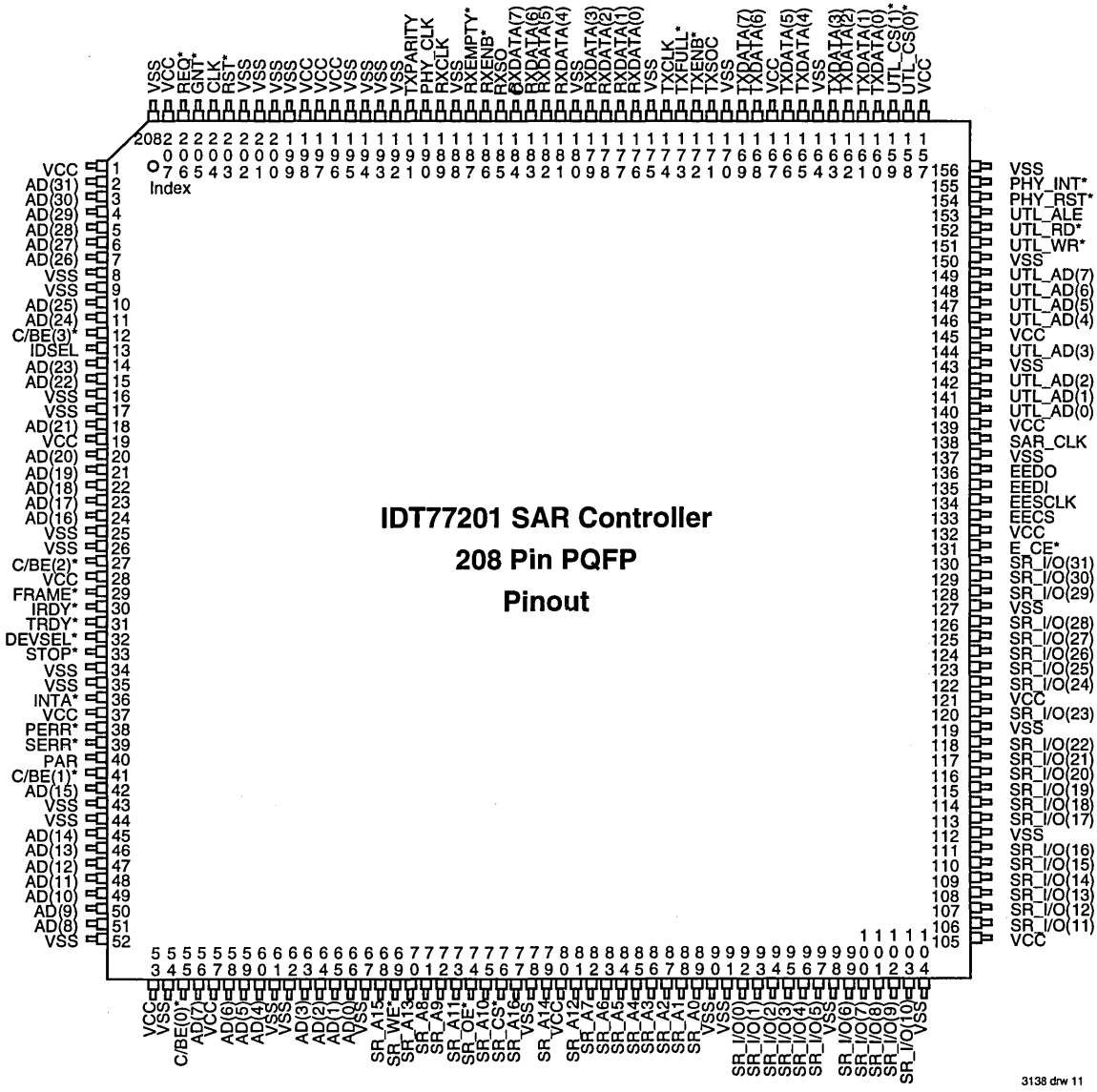
A Network Interface Card (NIC) or internetworking product based on the NICStAR uses host memory, rather than local memory, to reassemble Convergence Sublayer Protocol Data Units (CS-PDUs) from ATM cell payloads received from the network. When transmitting, as CS-PDUs become ready, they are queued in host memory and segmented by the NICStAR into ATM cell payloads. From this, the NICStAR then creates complete 53-byte ATM cells which are sent through the network. The NICStAR's on-chip PCI bus master interface provides efficient, low latency DMA transfers with the host system, while it's UTOPIA interface provides direct connection to PHY components used in 25.6 Mbps to 155 Mbps ATM networks.

The IDT77201 is fabricated using state-of-the-art CMOS technology, providing the highest levels of integration, performance and reliability, with the low-power consumption characteristics of CMOS.

SYSTEM-LEVEL FUNCTIONAL BLOCK DIAGRAM

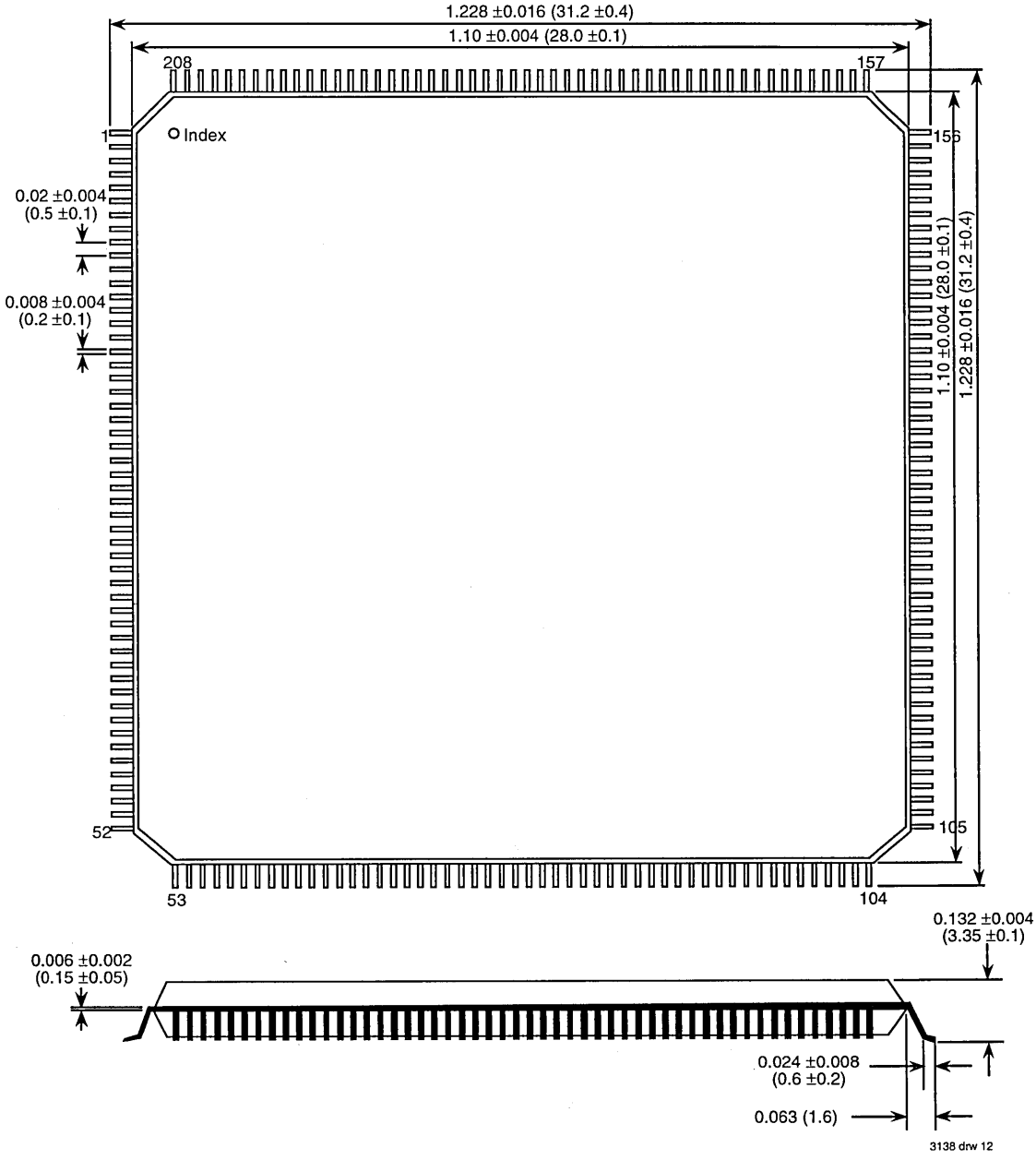


PACKAGE PINOUT



3138 drw 11

PACKAGE DRAWING



PIN DEFINITIONS

Symbol	Name	I/O	# Pins	Description
AD[31-0]	Addess/Data	I/O	32	PCI Bus multiplexed address/data bus
C/BE[3-0]#	Command	I/O	4	PCI Bus Command
PAR	Parity	I/O	1	Even parity across AD31-0 and C/BE3-0
FRAME#	Cycle Frame	I/O	1	Cycle frame. Beginning and duration of an access.
TRDY#	Target Ready	I/O	1	Target ready
IRDY#	Init. Ready	I/O	1	Initiator ready
STOP#	Stop	I/O	1	Target requesting master to stop current transaction
DEVSEL#	Device Select	I/O	1	Target indicating address decode
IDSEL	Init. Device Select	I	1	Initialization device select
PERR#	Parity Error	I/O	1	Parity error on data
SERR#	System Error	O	1	System error
REQ#	Request	O	1	Bus request. SAR requests PCI bus using this signal
GNT#	Grant	I	1	PCI bus arbiter grants bus using this signal
INTA#	Interrupt Request	O	1	SAR uses this to drive one of the PCI bus INTx# signals
CLK	Clock	I	1	PCI bus clock
RST#	Reset	I	1	PCI bus system reset
SR_I/O[31-0]	SRAM Data	I/O	32	Read/write data for external SRAM
SR_ADRS[16-0]	SRAM Address	O	17	SRAM word address
SR_WE#	SRAM Write	O	1	SRAM read/write control
SR_OE#	Output Enable	O	1	SRAM output enable control
SR_CS#	Chip Select	O	1	SRAM chip select control.
E_CS#	ROM Select	O	1	External ROM chip select.
TxData[7-0]	Transmit Data	O	8	UTOPIA Tx data bus
TxSOC	Tx Start of Cell	O	1	UTOPIA start of cell indicator
TxEnb#	Tx Enable	O	1	UTOPIA Tx enable signal
TxFull#	Tx Full	I	1	UTOPIA flow control from PHY indicating input buffer is full
TXClk	Tx Clock	O	1	UTOPIA Tx transfer/synchronization clock from ATM layer to PHY layer
TxParity	Tx Parity	O	1	Parity on Tx data bytes.
RxClk	Rx Clock	O	1	UTOPIA Rx transfer/synchronization clock from ATM layer to PHY layer
RxData[7-0]	Rx Data	I	8	Receive data bus from PHY
RxSOC	Rx Start of Cell	I	1	Start of Rx cell indicator
RxEnb#	Receive Enable	O	1	Receive enable signal from SAR
RxEmpty#	Rx Empty	I	1	Indicates that current cycle does not contain valid data on RxData
PHY_Int#	PHY Interrupt	I	1	Interrupt input from PHY
PHY_RST#	PHY Reset	O	1	Output to PHY for reset.
PHY_Clk	PHY Clock	I	1	Input from external 25 MHz crystal clock osciallator
UTL_AD[7-0]	Address/Data	I/O	8	Utility Bus multiplexed address and data
UTL_RD#	Read	O	1	Utility Bus read control signal
UTL_WR#	Write	O	1	Utility Bus write control signal
UTL_ALE	Address Latch	O	1	Utility Bus address latch enable signal to latch UTL_AD[7-0]
UTL_CS[1-0]#	Chip Select	O	2	Utility Bus chip select controls
EEDO	EEPROM Data Out	O	1	EEPROM serial write data
EEDI	EEPROM Data In	I	1	EEPROM serial read data
EECS	EEPROM Chip Select	O	1	EEPROM device select (selectable input polarity via SAR register)
SAR_CLK	SAR Clock	I	1	SAR 66 MHz clock input
VCC	Power	I	18	Power
VSS	Ground	I	41	Ground

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply voltage	-0.3	6.5	V
Vin	InputVoltage	VSS-0.3	VCC+0.3	V
Vout	Output Voltage	VSS-0.3	VCC+0.3	V
Tstg	Storage Temperature	0	125	deg. C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply voltage	4.75	5.25	V
Vi	Input Voltage	0	VCC	V
Ta	Operating temperature	0	70	deg. C
titr	Input TTL rise time	-	2	ns
titf	Input TTL fall time	-	2	ns

CAPACITANCE

Symbol	Parameter	Condition	Min.	Max.	Typical	Unit
Cin	Input Capacitance	except PCI Bus	-	-	4	pF
Cout	Output Capacitance	all outputs	-	-	6	pF
Cbid	Bi-Direactional Capacitance	all bi-directional pins	-	-	10	pF
Cinpci	PCI Bus Input Capacitance	PCI Bus inputs	-	10	-	pF
Cclkpci	PCI Bus Clock Input	-	5	12	-	pF
Cidsel	PCI Bus ID Select Input	-	-	8	-	pF

DC OPERATING CONDIONS

Symbol	Parameter	Condition	Min.	Max.	Typical	Unit
Vil	Low-level TTL input voltage	-	-	0.8	-	V
Vih	High-level TTL input voltate	-	2	-	-	V
Vol	Low-level TTL Output voltage	except PCI Bus	-	0 4	-	V
Vol	PCI Bus Low-level TTL output	PCI Bus voltage	-	0.55	-	V
Voh	High-level TTL output voltage	-	2.4	-	-	V
Iol	Low-level TTL output current: SR_A16-0	VSS+0.4V	-	-	12	mA
Ioh	High-level TTL output current: SR_A16-0	Vdd-0.4V	-	-	-4	mA
Iol	Low-level TTL output current: RxEnb#, RxClk, TxSOC, TxData 7-0, TxEnb#, TxParity, TxClk, WE#, OE#, CS#, SR_D31-0	VSS+0.4V	-	-	6	mA
Ioh	High-level TTL output current: RxEnb#, RxClk, TxSoc, TxData7-0, TxEnb#, TxPariety, TxClk, WE#, OE#, CS#, SR_D31-0	Vdd-0.4V	-	-	-2	mA
Iol	Low-level TTL output current: UTL_AD7-0, UTL_RD#, UTL_WR#, UTL_ALE#, UTL_CS1/2#, EESCLK, EECS, EEDO, PHY_RST#	Vss+0.4V	-	-	3	mA
Ioh	High-level TTL output current: UTL_AD7-0, UTL_RD#, UTL_WR#, UTL_ALE#, UTL_CS1/2#, EESCLK, EECS, EEDO, PHY_RST#	Vss+0.4V	-	-	-1	mA
Iil	Input leakage current	-	-1	1	-	uA
Ityp	Dynamic Supply Current	-	-	-	TBD	mA

5

PCI BUS

Symbol	Parameter	Min.	Max.	Units
tval	CLK to Output Signal Valid Delay: AD31-0, C/BE3-0, PAR, FRAME#, IRDY#, DEVSE;#. TRDU#. STOP#. PERR#. SERR#	-	11	ns
tval(ptp)	CLK to Output Signal Valid Delay: REQ#	-	12	ns
ton	Float to Signal Active Delay: AD31-0, C/BE3-0, PAR, FRAME#, IRDY#, DEVSEL#, TRDY#, STOP#, RERR#, SERR#	2	-	ns
toff	Signal Active to Float Delay: AD31-0, C/BE3-0, PAR, FRAME#, IRDY#, DEVSEL#, TRDY#, STOP#, RERR#, SERR#	-	28	ns
tsu	Input Setup Time to CLK: AD31-0, C/BE3-0, PAR, FRAME#, IRDY#, DEVSEL#, TRDY#, STOP#, RERR#, SERR#, GNT#, IDSEL#	7	-	ns
tsu(ptp)	Input Setup Time to CLK: GNT#	10	-	ns
th	Input Hold Time from CLK: AD31-0,C/BE3-0, PAR, FRAME#, IRDY#, DEVSEL#, TRDY#, STOP#, PERR#, SERR#, GNT#, IDSEL#	0	-	ns
trst-pwr	Reset Active Time After Power Stable	1	-	ms
trst-clk	Reset Active Time After CLK Stable	100	-	ns
trst-off	Reset Active to Output Float Delay:AD31-0, C/B3-0, PAR, FRAME#, IRDY#, DEVSEL#, TRDYU#, STOP#, PERR#, SERR#	-	40	ns

UTOPIA BUS

Symbol	Parameter	Min.	Max.	Units
tl	TxClk, RxClk Delay from PHY_CLK	-	15	ns
t2	TxData7-0, TxSOC, TAxEnb#, TxParity Output Valid from TxClk	-	20	ns
t3	TxFull#/TAxCLAV Setup Time to ExClk	10	-	ns
t4	TxFull#/TxCLAV Hold Time from TxClk	0	-	ns
t5	RxEnb# Output Valid from RxClk	-	20	ns
t6	RxData7-0, RxSOC Setup Time to RxClk	10	-	ns
t7	RxData7-0, RxSOC Hold Time from RxClk	0	-	ns
t8	RxEmpty# Setup Time to RxClk	10	-	ns
t9	RxEmpty# Hold Time from RxClk	0	-	ns

UTILITY BUS WRITE CYCLE

Symbol	Parameter	Min.	Max.	Units
twl	UTL_ALE Pulse Width	25	-	ns
tw2	UTL_CS1/2# Output Valid to UTL_ALE falling edge	25	-	ns
tw3	UTL_WR# Output Valid from UTL_ALE falling edge	-	80	ns
tw4	UTL_CS1/2# Pulse Width	275	-	ns
tw5	UTL_WR# Pulse Width	185	-	ns
tw6	UTL_ALE falling edge to UTL_CS1/2#2,UTL_WR# rising edge	245	-	ns
tw7	UTL_AD7-0 Address Setup Time to UTL_ALE falling edge	30	-	ns
tw8	UTL_AD7-0 Address Hold Time from UTL_ALE falling edge	10	-	ns
tw9	UTL_AD7-0 Data Setup Time to UTL_CS1/2#, UTL_WR# rising edge	185	-	ns
tw10	UTL_AD7-0 Data Hold Time from UTL_CS1/2#, UTL_WR# rising edge	10	-	ns

UTILITY BUS READ CYCLE

Symbol	Parameter	Min.	Max.	Units
trl	UTL_ALE Pulse Width	25	-	ns
tr2	UTL_CS1/2# Output Valid to UTL_ALE falling edge	25	-	ns
tr3	UTL_RD# Output Valid from UTL_ALE falling edge	-	80	ns
tr4	UTL_CS1/2# Pulse Width	275	-	ns
tr5	UTL_RD# Pulse Width	185	-	ns
tr6	UTL_ALE falling edge to UTL_CS1/2#, UTL_RD# rising edge	270	-	ns
tr7	UTL_AD7-0 Address Setup Time to UTL_ALE falling edge	30	-	ns
tr8	UTL_AD7-0 Address Hold Time from UTL_ALE falling edge	10	-	ns
tr9	UTL_AD7-0 Data Setup Time to UTL_CS1/2#, UTL_RD# rising edge	80	-	ns
tr10	UTL_AD7-0 Data Hold Time from UTL_CS1/2#, UTL_RD# rising edge	10	-	ns

SRAM BUS WRITE CYCLE

Symbol	Parameter	Min.	Max.	Units
t1	SR_CS# falling edge to SR_WR# falling edge	0	-	ns
t2	SR_WE# rising edge to SR_CS# rising edge	0	-	ns
t3	SR_A16-0 Setup Time to SR_WE# falling edge	2	-	ns
t4	SR_A16-0 Hold Time from SR_CS# rising edge	0	-	ns
t5	SR_D31-0 Setup Time to SR_CS# rising edge	11	-	ns
t6	SR_D31-0 Setup Time to SR_WR# rising edge	11	-	ns
t7	SR_D31-0 Hold Time from SR_CS# rising edge	0	-	ns
t8	SR_D31-0 Hold Time from SR_WR# rising edge	0	-	ns

SRAM BUS READ CYCLE

Symbol	Parameter	Min.	Max.	Units
t1	SR_CS# falling edge to SR_OE# falling edge	0	-	ns
t2	SR_OE# rising edge to SR_CS# rising edge	0	-	ns
t3	SR_D31-0 Setup Time to SR_)E# rising edge	15	-	ns
t4	SR_D31-0 Setup Time from SR_CS# rising edge	15	-	ns
t5	SR_D31-0 Hold Time to SR_OE# rising edge	10	-	ns
t6	SR_D31-0 Hold Time to SR_SC# rising edge	10	-	ns
t7	SR_CS#0 falling edge to SR_ADR16-0 Valide	0	-	ns
t8	SR_A16-0 to SR_D31-0 Valid	15	-	ns

EPROM

Symbol	Parameter	Min.	Max.	Units
t1	SR_D7-0 Hold Time fromROM_CS# rising edge	0	-	ns
t2	ROM_CS# falling edge to SR_A16-0 Valid	0	-	ns
t3	ROM_CS# rising edge to SR_A16-0 Delay	0	-	ns
t4	ROM_CS# Pulse Width	345	-	ns
t5	SR_A16--0 Change to SR_D7-0 Valid	-	70	ns
t6	SR_A16-0 to SR_A16-0 Change	75	-	ns

EEPROM

Symbol	Parameter	Min.	Max.	Units	Comments
t1	SAR_CLK to Output Signal Valid Delay: EECS, EED0, EECLK	100	-	ns	software controlled
t2	EEDI Input Setup Time to SAR_CLK	10	-	ns	software controlled
t3	EDDI Input Hold Time from SAR_CLK	0	-	ns	software controlled

NICStAR OVERVIEW

A NIC or internetworking product based on the NICStAR includes:

- IDT77201 NICStAR
- 32K x 32 - 15 ns SRAM
  (expandable to 128K x 32):
  - Receive Small/Large Free Buffer Queues
  - 315-cell Receive FIFO Buffer
  - Receive Connection Table
  - Transmit Buffer Descriptors
  - Transmit Schedule Table
  - Intermediate AAL5 CS-PDU CRC storage
- 32K x 8 - 100 ns (optional) PROM
  (expandable to 128Kx 8)
  - Host driver storage (loaded at boot time).
- EEPROM, serial I/O (optional)
  Non-volatile configuration data storage.
- Crystal Clock Oscillators
  - 66.67 MHz for NICStAR clock
  - 25.00 MHz for UTOPIA interface

Local SRAM

A small amount of external SRAM is used by the NICStAR for various key functions, as shown below. As the table at the right illustrates, the size of the local SRAM determines the maximum number of simultaneously open receive and transmit connections; 32K x 32 SRAM should be sufficient for most applications.

Rx Large Free Buffer Queue (up to 512 entries @ 2 words/entry)
Rx Small Free Buffer Queue (up to 512 entries @ 2 words/entry)
315-cell Rx FIFO Buffer (up to 315 52-byte cells)
ABR SCD0 ABR SCD1 ABR SCD2 (12 words/SCD with 2 TBDS/SCD)
Tx Schedule Table & CBR SCDs (up to 2430 64Kbps CBR VCs @ 1 word/TST entry) (12 words/SCD with 2 TBDS/SCD)
Rx Connection Table (up to 16K VCs @ 4 words/entry)

Options for Max. # of Receive VC Connections:

	32K x 32	128K x 32
4K VCs	Yes	Yes
8K VCs	-	Yes
16K VCs	-	Yes

Max. # of Transmit VC Connections:

	32K x 32	128K x 32
CBR VCs*	647	2430*
ABR/VBR/UBR VCs	= Rx VCs	= Rx VCs

*Specifies the # of simultaneously open Tx CBR VCs.
The theoretical maximum # is 2430 with 155.52 Mbps ATM.

PCI Interface

The NICStAR includes a PCI DMA master interface, which requires no glue logic to interface to the host system's PCI bus. This interface provides efficient, low latency transfers to and from the host memory. Further, the DMA master transfer method relieves the host system processor from most of the activities involved in ATM communication. The device driver only needs to write and maintain small descriptors in the host memory and to update pointers in local SRAM for the NICStAR. All ATM cell payload transfers, as well as all key descriptor transfers, are controlled by the NICStAR.

To achieve optimum performance, other devices and interface cards in the host system which have PCI bus master capability should have their Latency Timers set to values < 30 (representing the number of PCI clocks a bus master may use for transfer purposes). This should allow a NICStAR-based device to obtain access to the PCI bus in ~ 1 us, low enough that isochoronous data will not be affected in 155 Mbps ATM networks.

PHY Interface

For connecting to PHY components, the NICStAR provides a UTOPIA (Universal Test and Operations PHY Interface for ATM) interface. UTOPIA is a standard data path handshake protocol which eases PHY and other product integration and interchange.

5

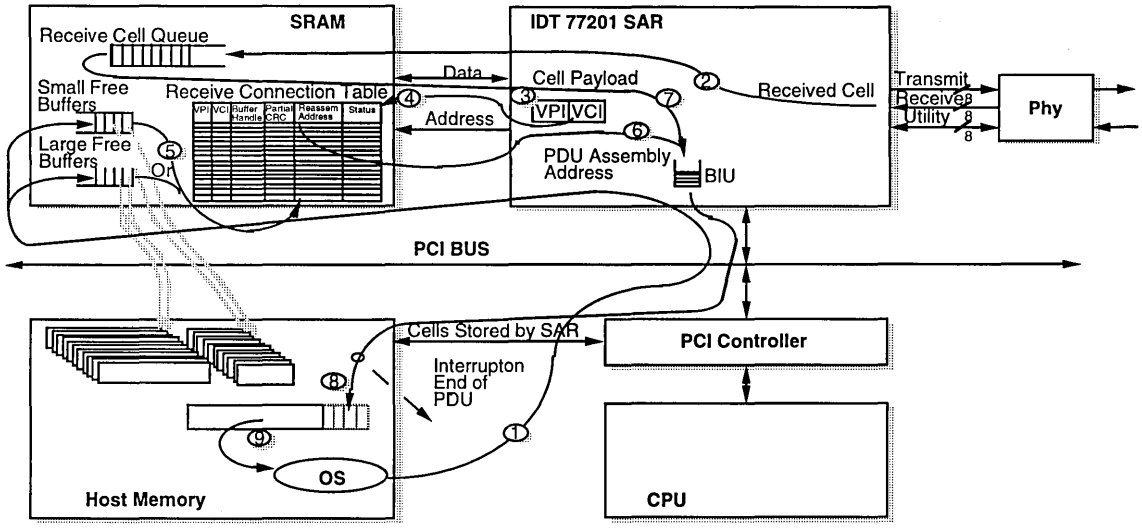
SAR Function Implementation

The NICStAR implements the Segmentation and Reassembly (SAR) function as described in the ATM User-Network Interface Specification, Version 3.1, and other documents published by the "ATM Forum".

Host Driver Operation

The NICStAR operates under the control of a software device driver running on a host system. In receive, the device driver generates lists of host memory buffer addresses which constitute reassembled CS=PDUs in host memory buffers. Once reassembly is complete, a list of addresses is provided to the application program(s) for conversion of the CS-PDU back to user data.

When transmitting, CS-PDUs are queued in host memory as they become ready. The device driver creates descriptors of the host memory buffer addresses which contain the PDU, and then writes these descriptors into a descriptor queue (located in host memory), for processing by the NICStAR. The device driver initiates the transmit process by incrementing a pointer to the descriptor queue (located in local SRAM).



IDT 77201 SAR Controller Receive Data Flow 3138 drw 03

NICStAR Receive Operation

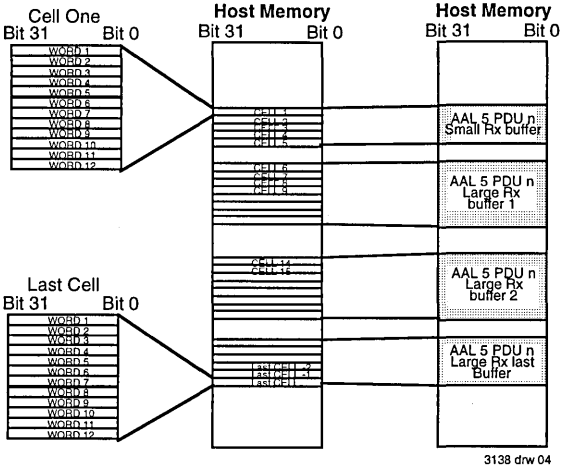
The NICStAR may simultaneously receive AAL5, AAL3/4, OAM, "AAL0" and "Raw Cell" formats. This section provides a description of the overall receive operation, followed by an overview of how each AAL format is supported.

Following the above diagram by the numbers:

1. Before reassembly may begin, the device driver must provide the NICStAR with a supply of host memory locations (buffers) which may be used for reassembly of ATM cell payloads into CS-PDUs. The start address of each buffer allocated for reassembly, called Small Free Buffers and Large Free Buffers, must be programmed into the local SRAM's Small Free Buffer Queue and Large Free Buffer Queue, respectively. The size of both types is programmed at initialization; Small Free Buffers default to 64 bytes (carriage returns, message receipt acknowledgements, etc), while Large Free Buffers default to 2 Kbytes. The NICStAR accomodates up to 512 Small and 512 Large Free Buffers at any one time.
2. A 53-byte ATM cell received from the PHY is immediately written by the NICStAR into the local SRAM's Receive Cell Queue (315 cell FIFO). The NICStAR writes the ATM cell header without the HEC byte, since the HEC byte was calculated and compared within the PHY prior to being received by the NICStAR.
3. The ATM cell header is read by the NICStAR.
4. The NICStAR uses the VPI/VCI field of the ATM cell header to index into the Receive Connection Table, which contains the following information:
   - VPI/VCI (unique for each virtual connection)
   - Buffer Handle (virtual start address of a free buffer)
   - Partial CRC value (for AAL5 PDU)
   - Reassembly Address (from Free Buffer Queues)
   - Status (AAL format, etc.)
5. Assuming this is the first ATM cell received for this CS-PDU, the first free buffer address in the Small Free Buffer Queue is copied into the Receive Connection Table entry for the specified virtual channel (VC). As additional cells are received for this CS-PDU, cell payloads are deposited into host memory at remaining addresses pointed to by this Small Free Buffer. Once the Small Free Buffer memory area is exhausted, subsequent free buffers (as

needed) are copied from the Large Free Buffer Queue to finish reassembly of the PDU. The first ATM cell payload of a new CS-PDU is always stored into a memory location addressed by a Small Free Buffer.

6. The NICStAR writes the start address for the Small Free Buffer to it's Bus Interface Unit (BIU).
7. The NICStAR writes the 12 word ATM cell payload to it's BIU.
8. The NICStAR performs a PCI DMA-master transfer of the 48-byte ATM cell payload to the specified Small Free Buffer in host memory. After completely filling any Small or Large Free Buffer in host memory, the NICStAR writes the start address of the buffer to the Receive Status Queue, located in host memory. As additional Large Free Buffers are filled with ATM cell payloads, the NICStAR writes the start addresses of the Large Free Buffers to the Receive Status Queue for the specified VC. After the NICStAR detects an end of PDU, it may (optionally) generate an interrupt, informing the host system to service the Receive Status Queue.



3138 drw 04

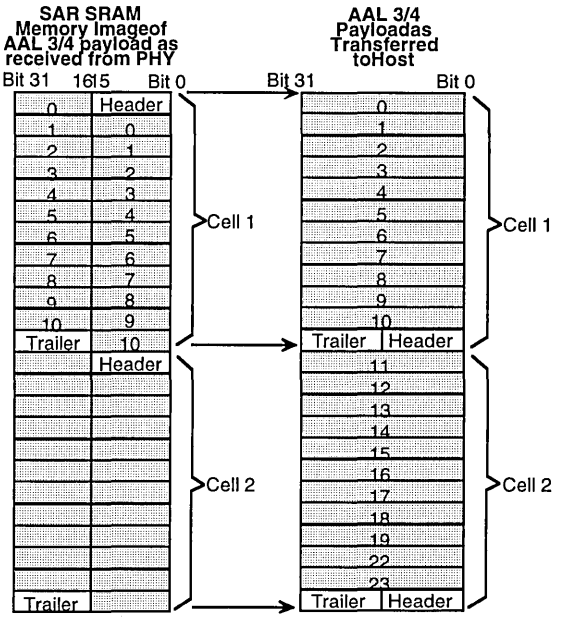
9. After an "end of PDU" is detected, the device driver reads the Receive Status Queue, generates a list of host memory buffer addresses which constitute the received CS-PDU and then provides the list of addresses to the application program(s) for converting back to user data.

• ATM Adaptation Layer (AAL) Support

As a VC connection is being established, the NICStAR assigns it a specific AAL format identifier, which is maintained in the local SRAM's Receive Connection Table. The following are descriptions of how each AAL format is supported:

• AAL5

AAL5 cells are reassembled by the NICStAR and stored directly to the appropriate host memory buffers. As each



3138 drw 05

AAL5 cell contains a 48 byte payload (with the possible exception of the last cell), the cell payload is mapped directly into 12 32-bit words and transferred as shown below.

The above diagram illustrates a Small Free Buffer for storing the first ATM cell payload, followed by successive Large Free Buffers. The NICStAR accumulates a CRC-32 value for all AAL5 cells from a VC, and stores the running total in the Receive Connection Table. When the last AAL5 cell is received from a specific VC, the NICStAR compares it's final calculated CRC-32 value to the CRC-32 value contained within the last AAL5 cell's payload.

• AAL3/4

As the first byte (header) and the last two bytes (trailer) of an AAL3/4 payload contain overhead information, AAL3/4 cells receive special processing.

As illustrated in drawing 5, the NICStAR shifts the header to payload byte positions 47 and 48, and leaves the AAL3/4 trailer in it's original location (payload bytes 45 and 46). In addition, payload data is all shifted to an even word boundary. Transferring the cell payload in this format to the host system supports subsequent data processing effiiciency. On receiving the cell payload, the device driver merely decodes the AAL3/4 header and trailer, followed by a simple word-aligned reassembly into a complete CS-PDU. The NICStAR calculates a payload CRC-10 value and stores it in the trailer. If the NICStAR detects a CRC error, it will set an error bit in the Receive Status Queue for the host memory buffers associated with this CS-PDU.

5

• OAM Cells

Operations and Management (OAM) cells are identified by several reserved (ATM Forum specification) VPI/VCI addresses, as well as several of the possible states contained in the Payload Type Identifier (PTI) field of the cell header. Since the header of OAM cells contains useful information, the entire cell is transferred to host memory; specifically stored in the Raw Cell Queue (see Raw Cell below). There are three possible OAM cell states:

1. Currently established VPI/VCI connections which may be passing application data; these connections may also pass OAM cells (ie, without application data) by setting certain PTI bits in the cell header. OAM cells of this type are detected by the NICStAR and transferred to the Raw Cell Queue in host memory. The NICStAR may optionally generate an interrupt upon completion of the transfer.

• "AAL0"

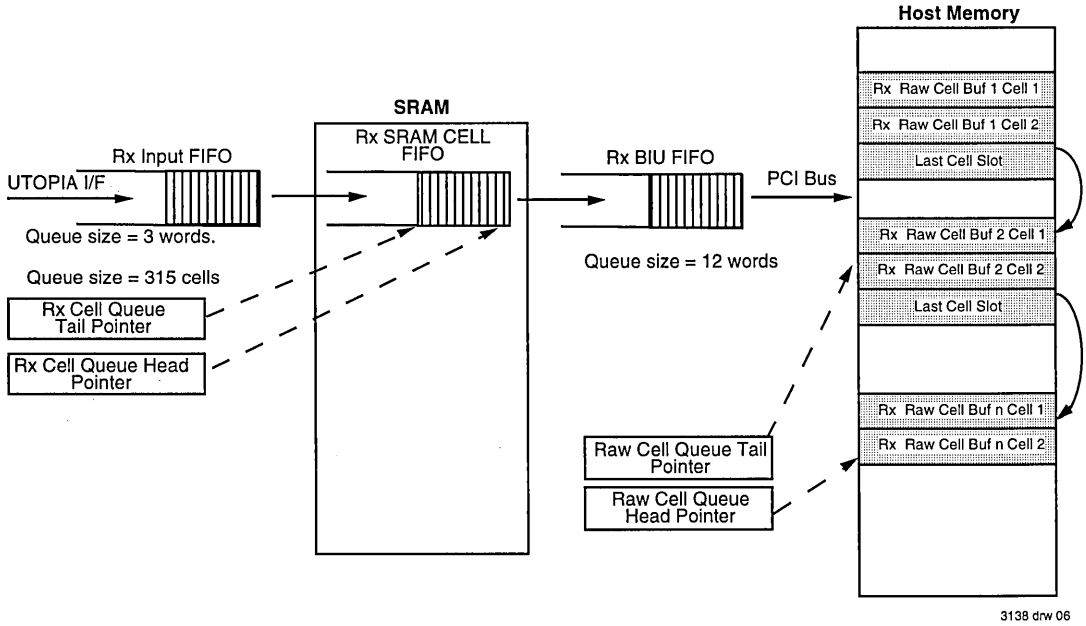
"AAL0" cells are ATM cells which conform to the 5 byte header, 48 byte payload structure of "general" ATM cells, but which do not fit within the requirements of other AAL formats. These "AAL0" cells are treated identical to AAL5 format cells, but without CRC processing and checking.

Using "AAL0", the NICStAR provides a means to support future AAL definitions. The device driver, on receipt of an AAL0 CS-PDU could perform additional payload (or PDU) processing as required by the newly defined AAL.

• "Raw Cells"

"Raw Cells" are defined as follows:

1. Identified as "Raw Cell" in the Receive Connection Table, by a particular VC.



2. 'Special' VPI/VCI connections which may be assigned for OAM cell communication. These are assembled according to their AAL format (created on establishment of connection). Operation continues as 'normal'; the device driver is interrupted as each CS-PDU is reassembled.

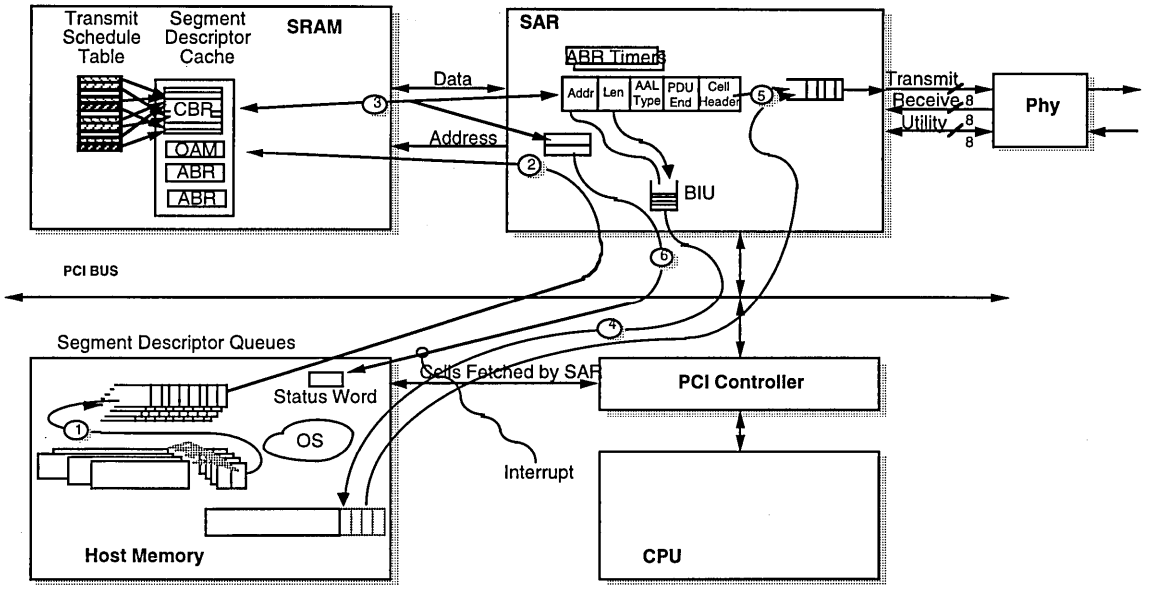
3. 'Unidentified' VPI/VCI combinations are those ATM cells which are received, but which do not have a corresponding entry in the Receive Connection Table. These cells are passed on to the "Raw Cell Queue" (described in the AAL0 section below) for identification processing.

2. Unknown VPI/VCI (entry not found in Receive Connection Table). This is selectable via the host driver: "Unknown" traffic may either be discarded, or placed in a Raw Cell Queue.

3. OAM cells (defined either by specific VC or PTI bits).

The diagram below illustrates the path flow of an incoming "Raw Cell" arriving via the UTOPIA interface, and its deposition into a Raw Cell Queue.

Note that Raw Cells are transferred in their entirety (payload and header) to the Raw Cell Buffer Queue for processing within the host.NICStAR Transmit Operation.



IDT 77201 SAR Controller Transmission Data Flow

3138 drw 07

5

As CS-PDUs are available, the NICStAR continuously segments and transmit ATM cells at the full 155 Mbps "wire speed". It simultaneously accomodates Constant Bit Rate (CBR), Unassigned Bit Rate (UBR), Available Bit Rate (ABR), and Variable Bit Rate (VBR) traffic types. Depending on the amount of external SRAM, the NICStAR supports up to 16K open CBR connections; independent of the size of the SRAM, it always supports the maximum of 16,000,000 VC connections (the full 24 bit VPI/VCI address space).

This section describes the overall transmission portion of the NICStAR. Following sections describe the Transmit Buffer Descriptors (TBDs) and the Transmit Cell Schedule Table (TCST), which manages the overall channel bandwidth and provides CBR connections with "guaranteed" bandwidth allocation.

Following the above diagram by the numbers:

1. As a CS-PDU becomes available for transmit, the device driver creates Transmit Buffer Descriptors (TBDs) for the sequence of buffers in host memory which constitute the CS-PDU, and then writes the TBDs into a TBD queue, located in host memory.
2. The device driver then causes the NICStAR to copy the first one or two TBDs to local SRAM.
3. The NICStAR reads the first TBD. The ATM cell header, also part of this buffer descriptor, is loaded into the output FIFO. During this process, a HEC byte place holder (00h) is added as the fifth byte of the header.
4. The PCI bus is arbitrated using the address and length taken from the TBD.
5. The ATM cell payload is transferred from host memory to the output FIFO via DMA. On completion, the 53-byte ATM cell is transferred out of the NICStAR via the UTOPIA interface.
6. Status information is returned to the host system to communicate transmission state, error conditions, etc.

• Transmit Buffer Descriptors

A Transmit Buffer Descriptor (TBD) is a four word descriptor which contains information such as the base address of a buffer in host memory, the number of words in the buffer, the AAL format of the information in the buffer (used when segmenting the buffer into ATM cells) and the ATM cell header (all TBDs in the same queue have identical cell headers; that of the first ATM cell of the CS-PDU).

The device driver writes the TBDs into a TBD Queue in host memory, and then increments a pointer to the queue in local SRAM, which causes the NICStAR to copy the first one or two TBDs to local SRAM. The NICStAR then reads the TBD and begins it's transmits process. The information contained in a

TBD is dependent upon which traffic type is stored in the corresponding Tx buffer:

CBR Traffic:
- Control Information (e.g. interrupt at end, etc)
- Cell Header
- Buffer Size, Base FIFO Address

UBR/ABR/VBR Traffic:
- Timer mantissa and exponent
- Interrupt at EOB
- Buffer Address, Size
- Status
- Segment Length
- Cell Header

The NICStAR maintains 3 types of transmit descriptor caches (queues):

1. CBR

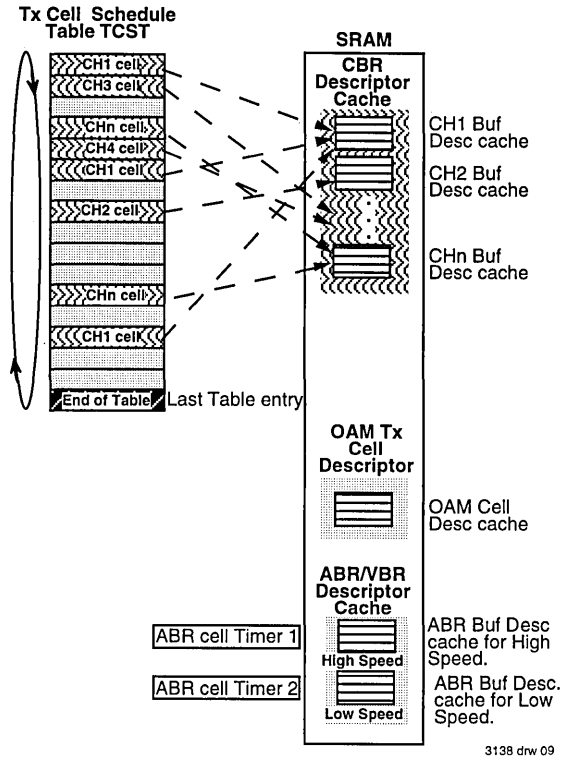
This cache holds two entries from each open CBR connection. This ensures that an entry is always immediately available for each connection, under schedule control of the NICStAR's Transmit Cell Schedule Table.

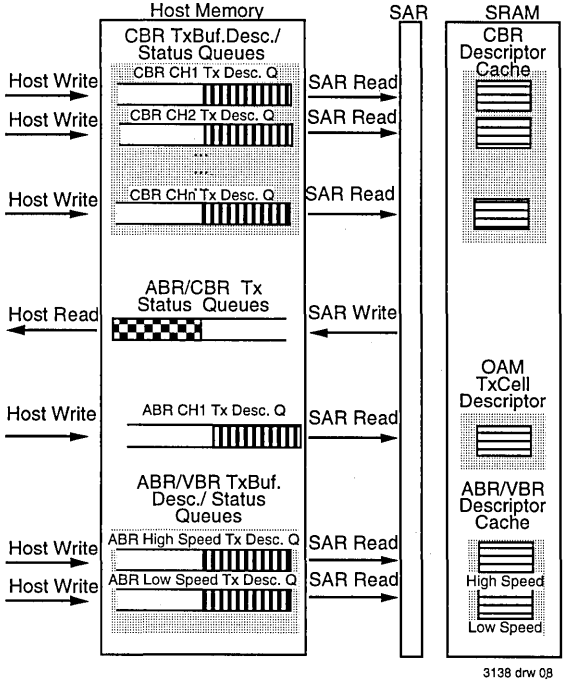
2. OAM

This cache is reserved for OAM cells which are considered higher priority than UBR/VBR traffic, but are to be sent only during time slots not reserved for CBR connections.

3. UBR/ABR/VBR

This cache consists of two sections a "high speed" cache and "low speed" cache. This separation provides a 'passing





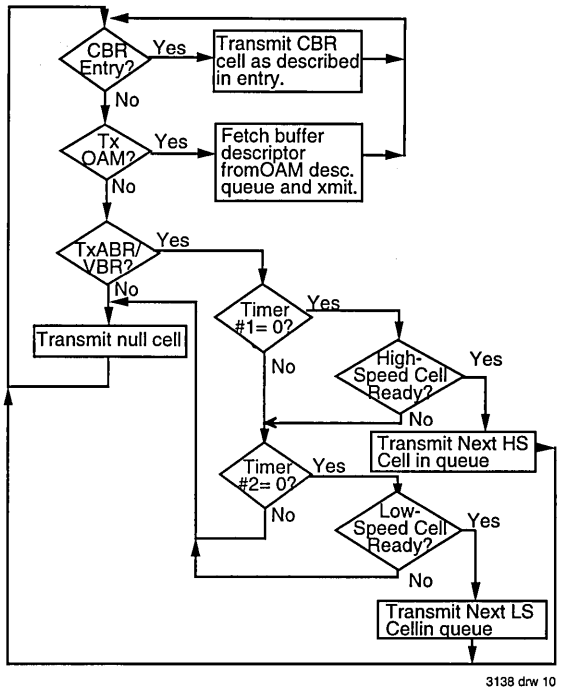
lane' for higher-speed/higher-priority traffic. Descriptors in the "Low Speed" queue are serviced only after the "High Speed" queue is empty, ensuring that higher-speed traffic is shipped at the highest data rate possible without exceeding its negotiated bandwidth. The facility operates under software control such that it can be tailored for specific applications and/or current operating conditions.

• Transmit Schedule Table (TST)

The Transmit Schedule Table is used to guarantee CBR transmission at fixed data rates and specific timing intervals within the system bandwidth. The TST is a circular table, in local SRAM, which the NICStAR continually scans to allocate bandwidth and control which connection is serviced. The number of entries in the table is equivalent to the line speed divided by the desired bandwidth resolution.

As an example, a 155Mb/s line would support 2430 64Kb/ CBR conneactions. Since the TST is scanned many times each second, any CBR channel may be allocated bandwidth in multiples of 64Kb/s. Each 64Kb/s entry 'contains' one line-speed cell time, which at 155Mb/s equals 2.7.µs. I It contains

TCST Entry Control Flow Chart



3138 drw 10

It contains three entry types:

1. CBR
2. OAM
3. ABR
4. VBR

CBR entries are VC-specific: it tells the SAR exactly which connection is to be serviced at that time. All other entry types designate available opportunities to transmit these data types.

Each TCST entry is either CBR, OAM, or ABR/VBR. If the entry is not defined, or cells are not available for transmission, a null cell is generated and transmitted. This feature is provided to assist users in integrating the 77201 SAR with PHY transceivers which may not have automatic null cell generation.

Each ABR/VBR entry has associated with it, a timer value which is used to throttle its transmission speed based upon the bandwidth allocated to it when the connection was established. Thus, if the TCST is servicing an ABR/VBR entry, the entry can point to one of two possible states:

1. A new buffer descriptor. In this case, the 'timer' is set to zero, since this connection has not been serviced yet. Once a cell has been transmitted, the timer is set for countdown.
2. A buffer descriptor whose transmission is 'in progress'. Data remains in the buffer. If the bandwidth-timer has timed out, a cell from this buffer is transmitted. Otherwise, flow control is transferred to check the "Low Speed" timer (Timer #2), which operates in the same way for entries in the "Low Speed" buffer descriptor cache.

5

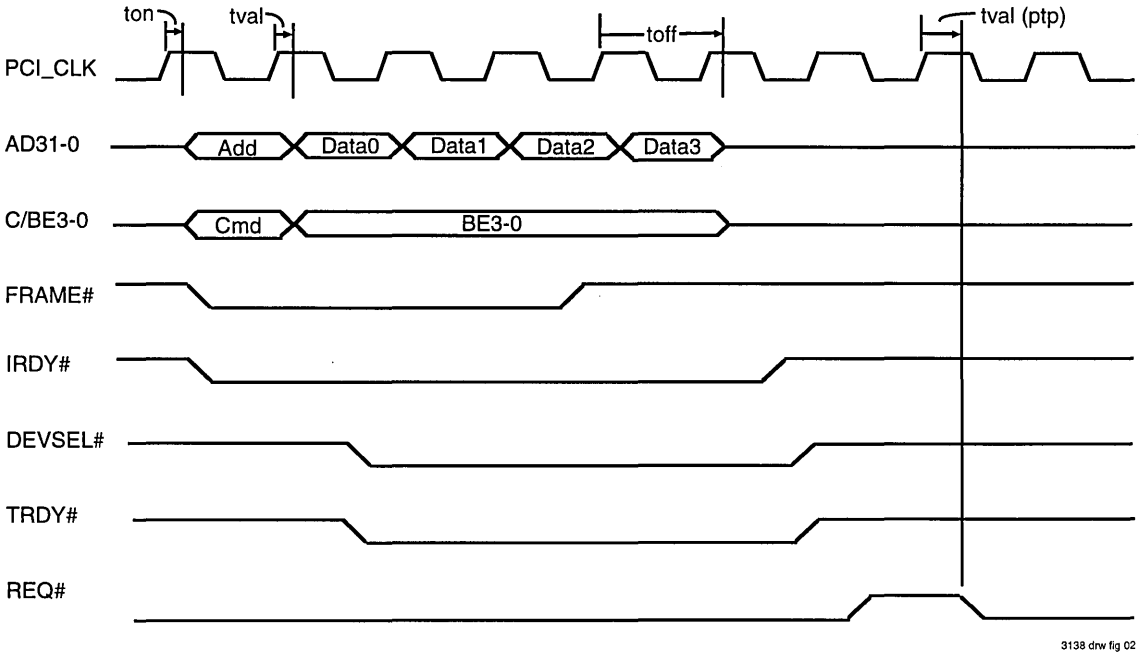


Figure 1. The NICStAR as a PCI master (illustrates a 4-word write by the NICStAR to host memory)

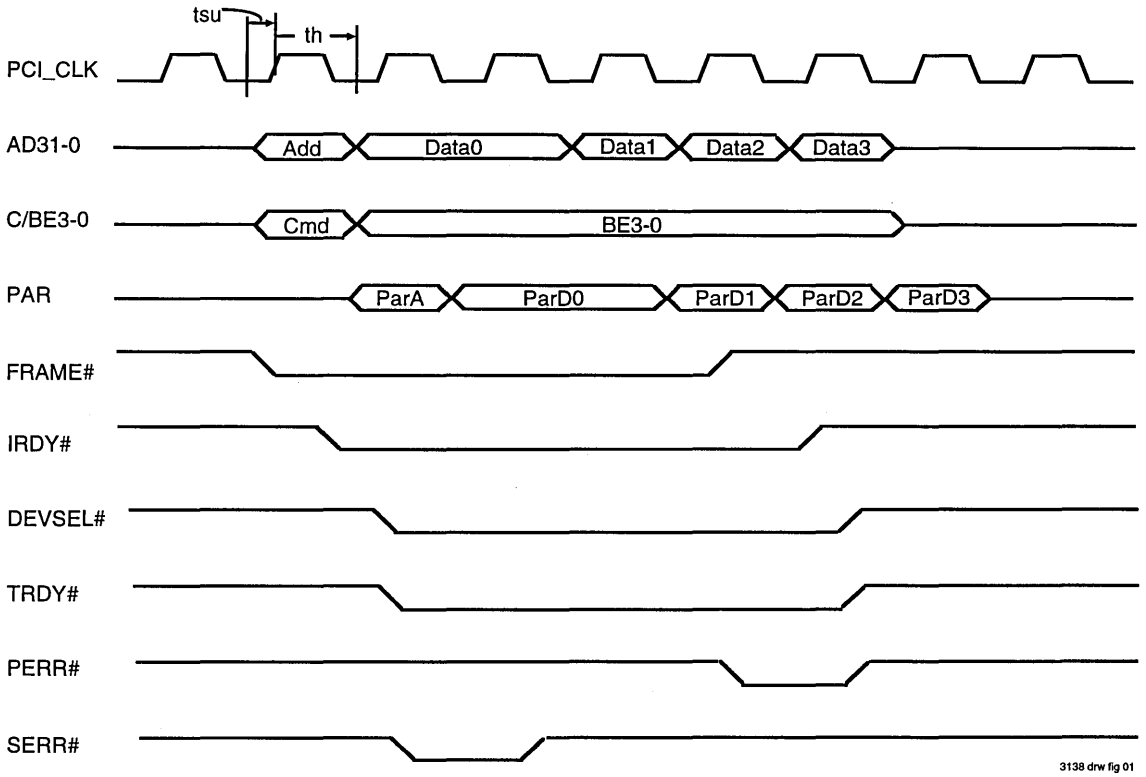


Figure 2. The NICStAR as a PCI target (illustrates a 4-word write operation by the host device driver to the NICStAR)

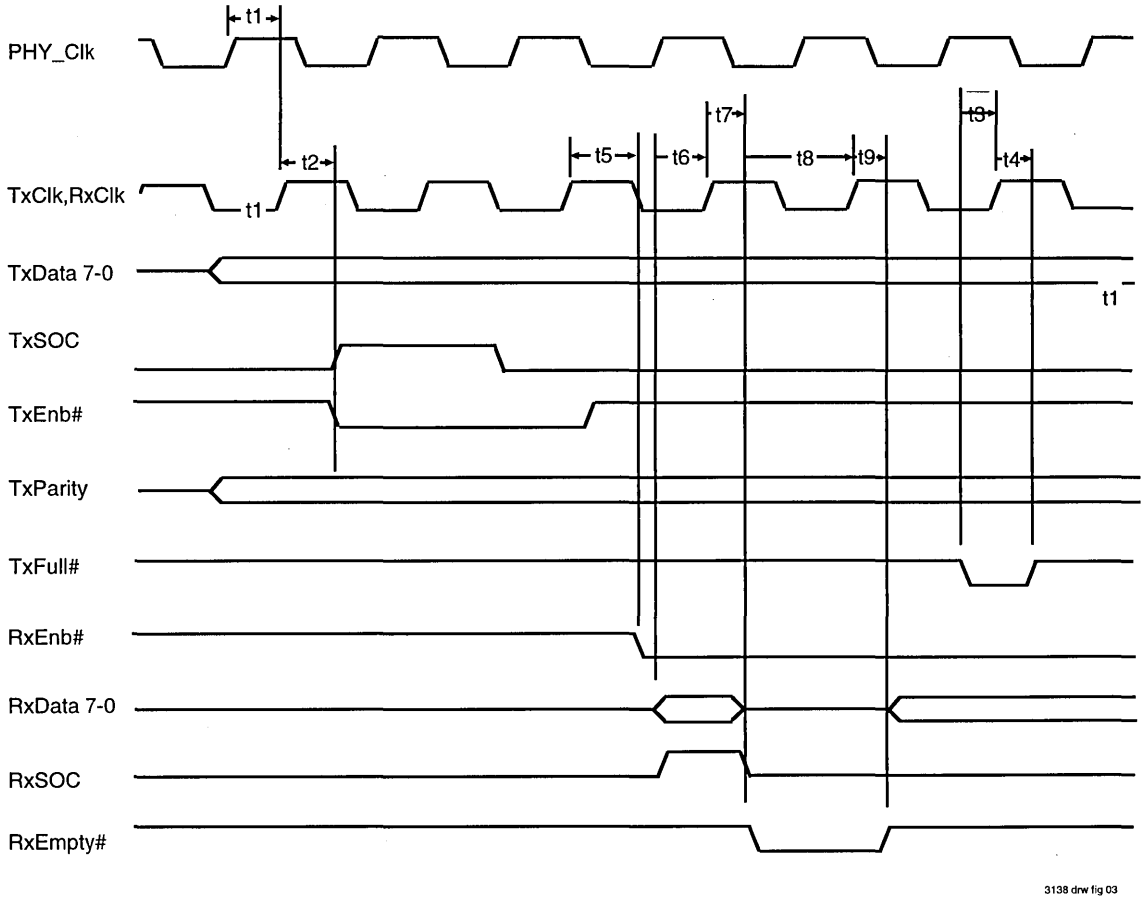


Figure 3. UTOPIA Bus Timing

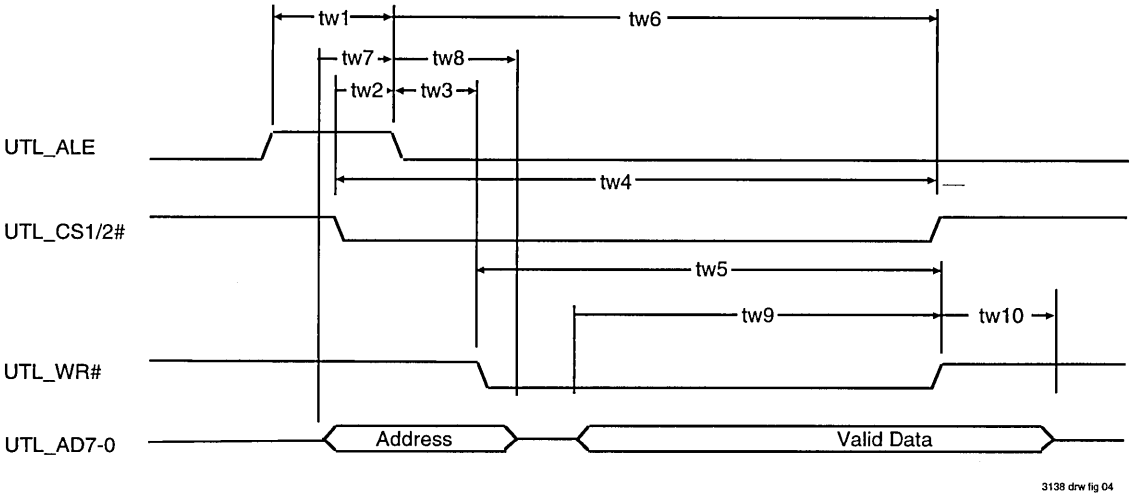


Figure 4. Utility Bus Write Cycle

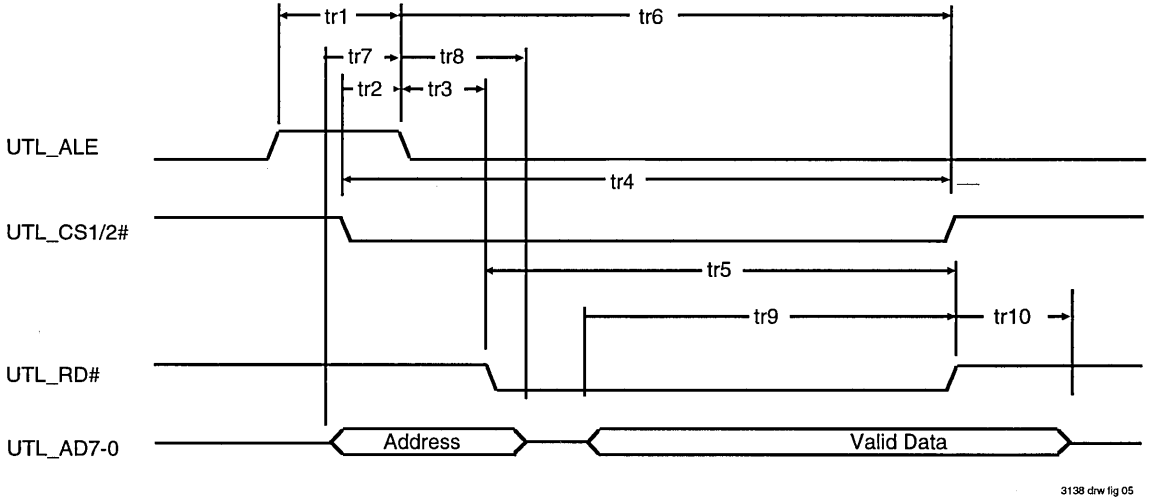


Figure 5. Utility Bus Read Cycle

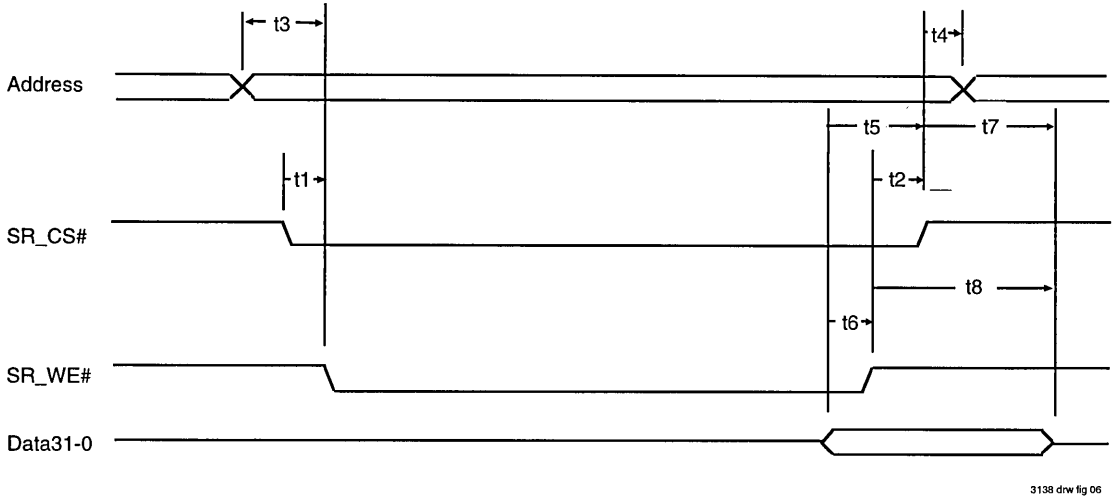


Figure 6. SRAM Bus Write Cycle Timing

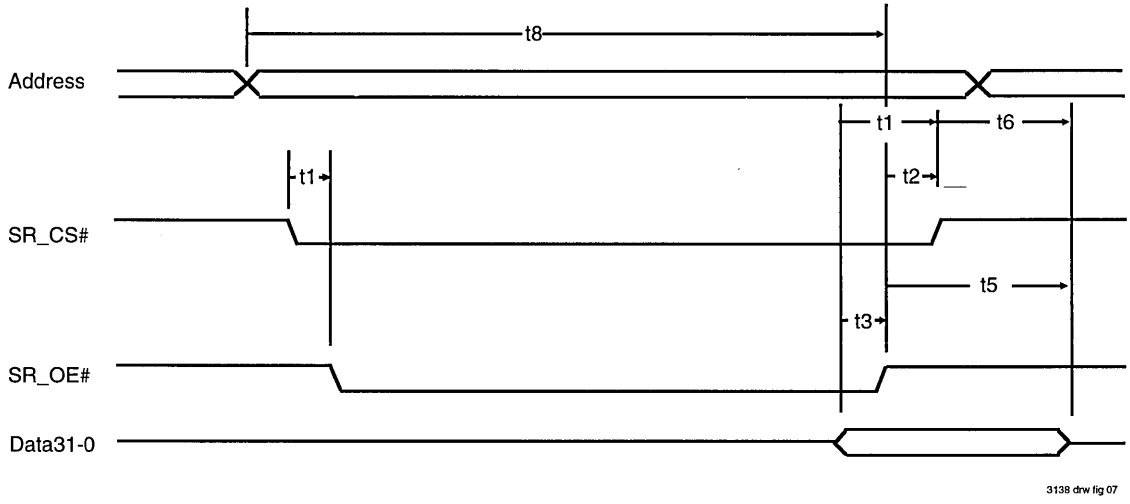


Figure 7. SRAM Bus Read Cycle Timing

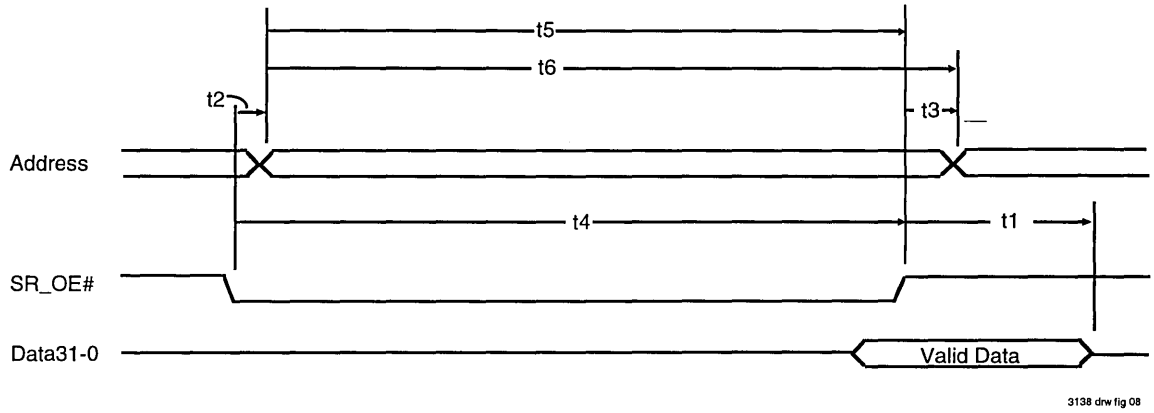


Figure 8. EPROM Timing

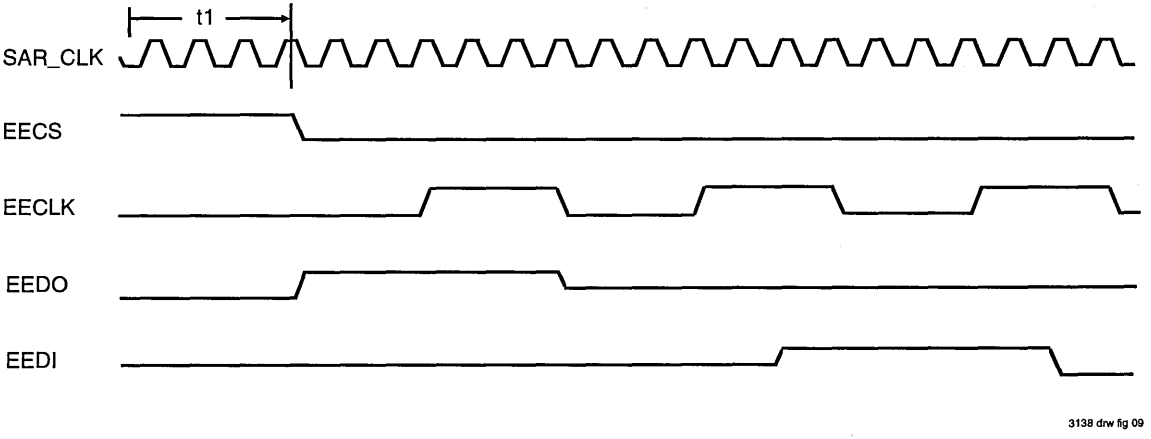
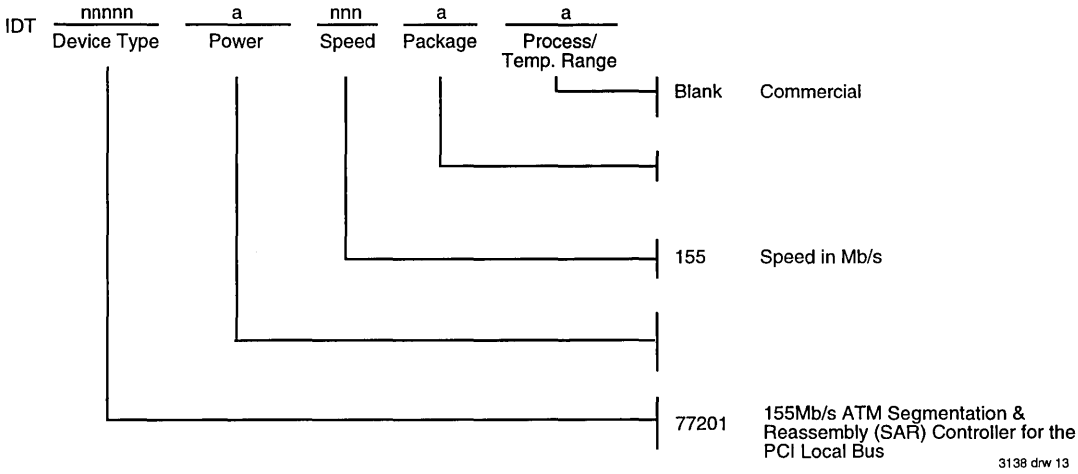


Figure 9. EEPROM Timing

ORDERING INFORMATION



ADVANCE INFORMATION DATASHEET: DEFINITION

"Advance Information" datasheets contain initial descriptions, subject to change, for products that are in development, including features and block diagrams.

Datasheet Document History

8/11/94: Initial Public Release
9/28/94: Pinout and Pin Definitions updated.
12/8/94: Pinout revised to final.
12/21/94: Pin 133 changed from EECS* to EECS with input polarity selectable via command register.

Integrated Device Technology, Inc.

CMOS SUPERSYNC FIFO™
16,384 x 9, 32,768 x 9

PRELIMINARY
IDT72261
IDT72271

FEATURES:

- 16,384 x 9-bit storage capacity (IDT72261)
- 32,768 x 9-bit storage capacity (IDT72271)
- 10ns read/write cycle time (8ns access time)
- Retransmit Capability
- Auto power down reduces power consumption
- Master Reset clears entire FIFO, Partial Reset clears data, but retains programmable settings
- Empty, Full and Half-full flags signal FIFO status
- Programmable Almost Empty and Almost Full flags, each flag can default to one of two preselected offsets
- Program partial flags by either serial or parallel means
- Select IDT Standard timing (using $\overline{EF}$ and $\overline{FF}$ flags) or First Word Fall Through timing (using $\overline{OR}$ and $\overline{IR}$ flags)
- Easily expandable in depth and width
- Independent read and write clocks (permit simultaneous reading and writing with one clock signal
- Available in the 64-pin Thin Quad Flat Pack (TQFP), 64-pin Slim Thin Quad Flat Pack (STQFP) and the 68-pin Pin Grid Array (PGA)
- Output enable puts data outputs into high impedance
- High-performance submicron CMOS technology

DESCRIPTION:

The IDT72261/72271 are monolithic, CMOS, high capacity, high speed, low power first-in, first-out (FIFO) memories with clocked read and write controls. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, local area networks (LANs), and interprocessor communication.

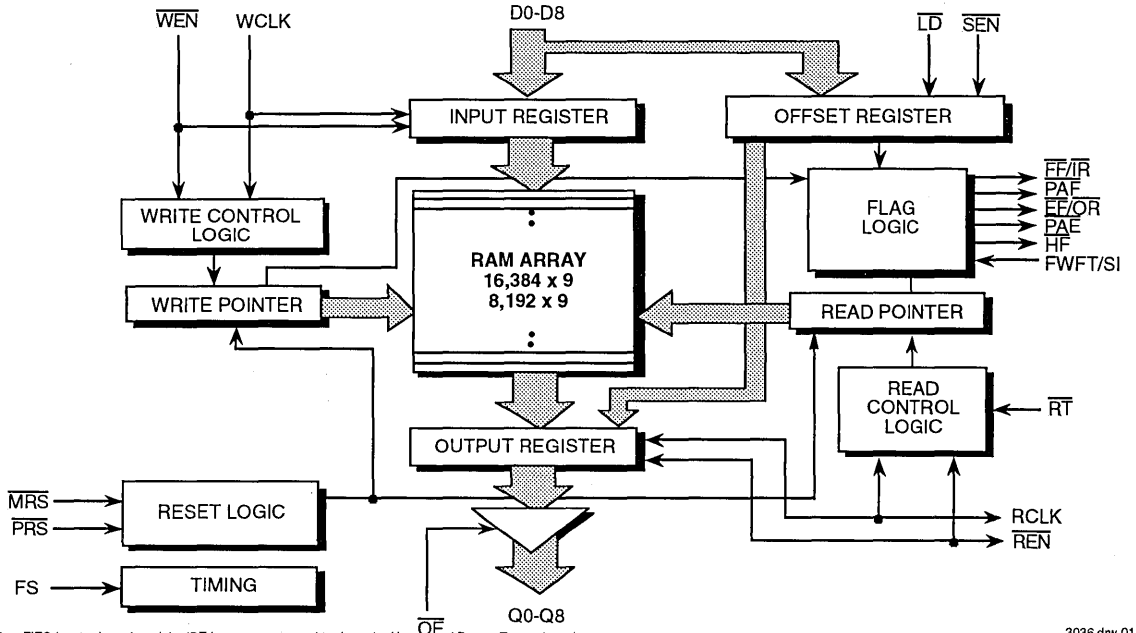
Both FIFOs have a 9-bit input port (Dn) and a 9-bit output port (Qn). The input port is controlled by a free-running clock (WCLK) and a data input enable pin ($\overline{WEN}$). Data is written into the synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronously for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the outputs.

The IDT72261/72271 have two modes of operation: In the *IDT Standard Mode*, the first word written to the FIFO is deposited into the memory array. A read operation is required to access that word. In the *First Word Fall Through Mode* (FWFT), the first word written to an empty FIFO appears automatically on the outputs, no read operation required. The state of the FWFT/SI pin during Master Reset determines the mode in use.

The IDT72261/72271 FIFOs have five flag functions, $\overline{EF}$/

5

FUNCTIONAL BLOCK DIAGRAM



SyncFIFO is a trademark and the IDT logo is a registered trademark of Integrated Device Technology, Inc.

3036 drw 01

$\overline{OR}$ (Empty Flag or Output Ready), $\overline{FF}$/$\overline{IR}$ (Full Flag or Input Ready), and $\overline{HF}$ (Half-full Flag). The $\overline{EF}$ and $\overline{FF}$ functions are selected in the IDT Standard Mode.

The $\overline{IR}$ and $\overline{OR}$ functions are selected in the First Word Fall Through Mode. $\overline{IR}$ indicates that the FIFO has free space to receive data. $\overline{OR}$ indicates that data contained in the FIFO is available for reading.

$\overline{HF}$ is a flag whose threshold is fixed at the half-way point in memory. This flag can always be used irrespective of mode.

$\overline{PAE}$, $\overline{PAF}$ can be programmed independantly to any point in memory. They, also, can be used irrespective of mode. Programmable offsets determine the flag threshold and can be loaded by two methods: parallel or serial. Two default offset settings are also provided, such that $\overline{PAE}$ can be set at 127 or 1023 locations from the empty boundary and the $\overline{PAF}$ threshold can be set at 127 or 1023 locations from the full boundary. All these choices are made with $\overline{LD}$ during Master Reset.

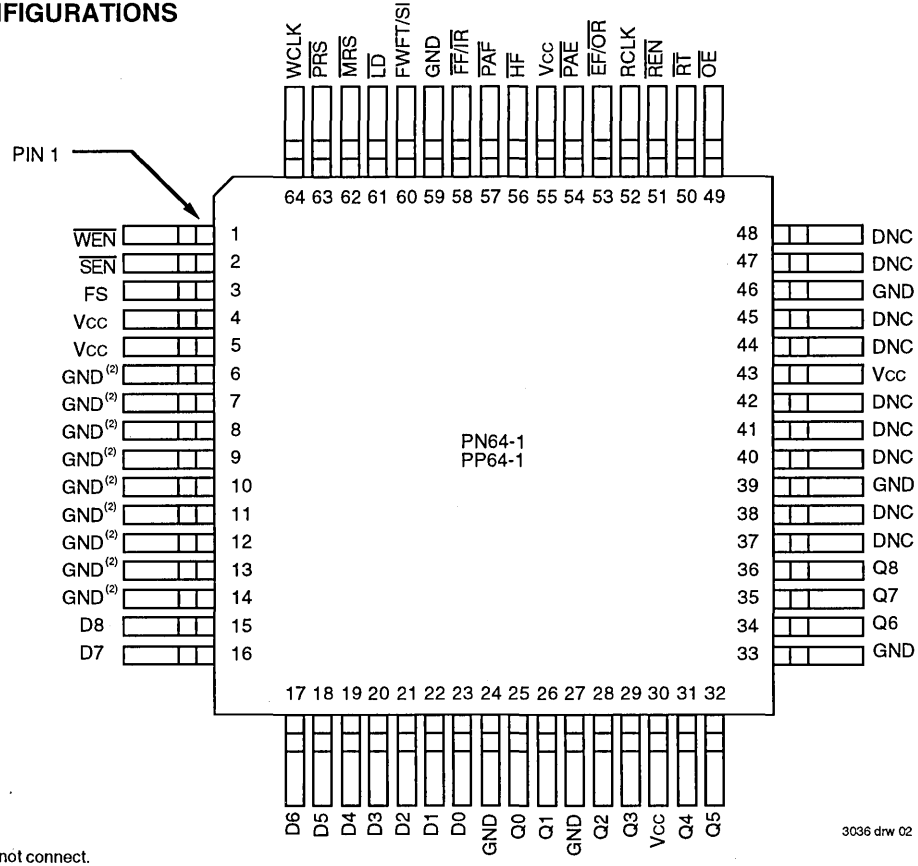
In the serial method, $\overline{SEN}$ together with $\overline{LD}$ are used to load the offset registers via the Serial Input (SI). In the parallel method, $\overline{WEN}$ together with $\overline{LD}$ can be used to load the offset registers via Dn. $\overline{REN}$ together with $\overline{LD}$ can be used to read the offsets in parallel from Qn regardless of whether serial or parallel offset loading is selected.

During Master Reset ($\overline{MRS}$), the read and write pointers are set to the first location of the FIFO. The FWFT line selects IDT Standard Mode or FWFT Mode. The $\overline{LD}$ pin selects one of two partial flag default settings (127 or 1023) and, also, serial or parallel programming. The flags are updated accordingly.

The Partial Reset ($\overline{PRS}$) also sets the read and write pointers to the first location of the memory. However, the mode setting, programming method, and partial flag offsets are not altered. The flags are updated accordingly. $\overline{PRS}$ is useful for resetting a device in mid-operation, when reprogramming offset registers may not be convenient.

The Retransmit function allows the read pointer to be reset to the first location in the RAM array. It is synchronized to RCLK when $\overline{RT}$ is LOW. This feature is convenient for

PIN CONFIGURATIONS



3036 drw 02

NOTES:
1. DNC = Do not connect.
2. This pin may either be tied to ground or left open.

TQFP
STQFP
TOP VIEW

sending the same data more than once.

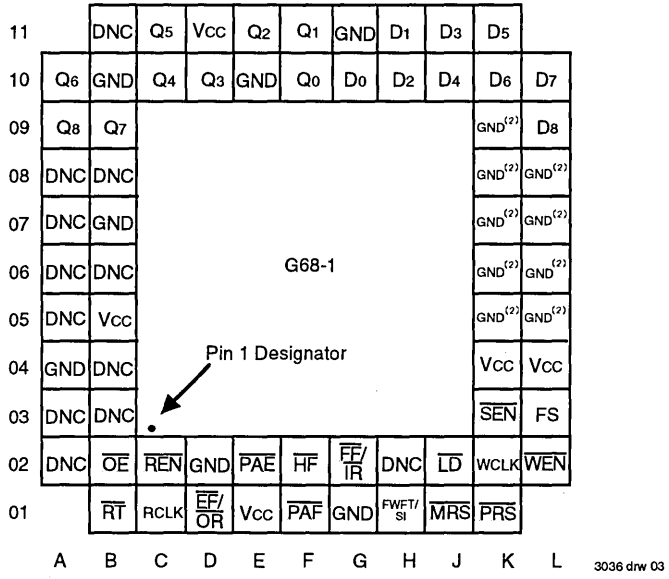
If, at any time, the FIFO is not actively performing a function, the chip will automatically power down. This occurs if neither a read nor a write occurs within 10 cycles of the faster clock, RCLK or WCLK. During the Power Down state, supply current consumption (I_{CC2}) is at a minimum. Initiating any operation (by activating control inputs) will immediately take the device out of the Power Down state.

The IDT72261/72271 are depth expandable. The addition of external components is unnecessary. The $\overline{IR}$ and $\overline{OR}$ functions, together with $\overline{REN}$ and $\overline{WEN}$, are used to extend the total FIFO memory capacity.

The FS line ensures optimal data flow through the FIFO. It is tied to GND if the RCLK frequency is higher than the WCLK frequency or to Vcc if the RCLK frequency is lower than the WCLK frequency

The IDT72261/72271 is fabricated using IDT's high speed submicron CMOS technology.

PIN CONFIGURATIONS (CONT.)



PGA
TOP VIEW

NOTES:
1. DNC = Do not connect.
2. This pin may either be tied to ground or left open.

PIN DESCRIPTION

Symbol	Name	I/O	Description
D_0–D_8	Data Inputs	I	Data inputs for a 9-bit bus.
$\overline{MRS}$	Master Reset	I	$\overline{MRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Master Reset, the FIFO is configured for either FWFT or IDT Standard Mode, one of two programmable flag default settings, and serial or parallel programming of the offset settings.
$\overline{PRS}$	Partial Reset	I	$\overline{PRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Partial Reset,the existing mode (IDT or FWFT), programming method (serial or parallel), and programmable flag settings are all retained.
$\overline{RT}$	Retransmit	I	Allows data to be resent starting with the first location of FIFO memory.
FWFT/SI	First Word Fall Through/Serial In	I	During Master Reset, selects First Word Fall Through or IDT Standard mode. After Master Reset, this pin functions as a serial input for loading offset registers
WCLK	Write Clock	I	When enabled by $\overline{WEN}$, the rising edge of WCLK writes data into the FIFO and offsets into the programmable registers.
$\overline{WEN}$	Write Enable	I	$\overline{WEN}$ enables WCLK for writing data into the FIFO memory and offset registers.
RCLK	Read Clock	I	When enabled by $\overline{REN}$, the rising edge of RCLK reads data from the FIFO memory and offsets from the programmable registers.
$\overline{REN}$	Read Enable	I	$\overline{REN}$ enables RCLK for reading data from the FIFO memory and offset registers.
$\overline{OE}$	Output Enable	I	$\overline{OE}$ controls the output impedance of Q_n
$\overline{SEN}$	Serial Enable	I	$\overline{SEN}$ enables serial loading of programmable flag offsets
$\overline{LD}$	Load	I	During Master Reset, $\overline{LD}$ selects one of two partial flag default offsets (127 and 1023) and determines programming method, serial or parallel. After Master Reset, this pin enables writing to and reading from the offset registers.
FS	Frequency Select	I	The FS setting optimizes data flow through the FIFO.
$\overline{FF}/\overline{IR}$	Full Flag/ Input Ready	O	In the IDT Standard Mode, the $\overline{FF}$ function is selected. $\overline{FF}$ indicates whether or not the FIFO memory is full. In the FWFT mode, the $\overline{IR}$ function is selected. $\overline{IR}$ indicates whether or not there is space available for writing to the FIFO memory.
$\overline{EF}/\overline{OR}$	Empty Flag/ Output Ready	O	In the IDT Standard Mode, the $\overline{EF}$ function is selected. $\overline{EF}$ indicates whether or not the FIFO memory is empty. In FWFT mode, the $\overline{OR}$ function is selected. $\overline{OR}$ indicates whether or not there is valid data available at the outputs.
$\overline{PAF}$	Programmable Almost Full Flag	O	$\overline{PAF}$ goes HIGH if the number of free locations in the FIFO memory is more than offset m which is store in Almost Full which is stored in the Full Offset register. $\overline{PAF}$ goes LOW if the number of free locations in the FIFO memory is less than m.
$\overline{PAE}$	Programmable Almost Empty Flag	O	$\overline{PAE}$ goes LOW if the number of words in the FIFO memory is less than offset n which is stored in theEmpty Offset register. $\overline{PAE}$ goes HIGH if the number of words in the FIFO memory is greater than offset n.
$\overline{HF}$	Half-full Flag	O	$\overline{HF}$ indicates whether the FIFO memory is more or less than half-full.
Q_0–Q_8	Data Outputs	O	Data outputs for a 9-bit bus.
V_{CC}	Power		+5 volt power supply pins.
GND	Ground		Ground pins.

3097 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
IOUT	DC Output Current	50	50	mA

3097 tbl 02

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maimum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIH	Input High Voltage Military	2.2	—	—	V
VIL(1)	Input Low Voltage Commercial & Military	—	—	0.8	V

3097 tbl 03

NOTE:

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Military: VCC = 5V ± 10%, TA = –55°C to +125°C)

Symbol	Parameter	DT72261L IDT72271L Commercial tCLK = 10, 12,15, 20ns			IDT72261L IDT72271L Military tCLK = 15, 25ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
ILI(1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
ILO(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = –2 mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8 mA	—	—	0.4	—	—	0.4	V
ICC1(3)	Active Power Supply Current	—	—	150	—	—	200	mA
ICC2(3,4)	Power Down Current (All inputs = VCC - 0.2V or GND + 0.2V, RCLK and WCLK are free-running)	—	—	15	—	—	25	mA

3097 tbl 04

NOTES:

1. Measurements with 0.4 ≤ VIN ≤ VCC.
2. $\overline{OE}$ = VIH
3. Tested at f = 20 MHz with outputs unloaded.
4. No data written or read for more than 10 cycles

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN(2)	Input Capacitance	VIN = 0V	10	pF
COUT(1,2)	Output Capacitance	VOUT = 0V	10	pF

3097 tbl 05

NOTES:

1. With output deselected, ($\overline{OE}$=HIGH).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = −55°C to +125°C)

		Commercial				Com'l & Mil.		Commercial		Military		
		72261L10 72271L10		72261L12 72271L12		72261L15 72271L15		72261L20 72271L20		72261L25 72271L25		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_S	Clock Cycle Frequency	—	100	—	83.3	—	66.7	—	50	—	40	MHz
t_A	Data Access Time	2	8	2	9	2	10	2	12	3	15	ns
t_{CLK}	Clock Cycle Time	10	—	12	—	15	—	20	—	25	—	ns
t_{CLKH}	Clock High Time	4.5	—	5	—	6	—	8	—	10	—	ns
t_{CLKL}	Clock Low Time	4.5[2]	—	5[2]	—	6[2]	—	8	—	10	—	ns
t_{DS}	Data Set-up Time	3.5	—	3.5	—	4	—	5	—	6	—	ns
t_{DH}	Data Hold Time	0	—	0	—	1	—	1	—	1	—	ns
t_{ENS}	Enable Set-up Time	3.5	—	3.5	—	4	—	5	—	6	—	ns
t_{ENH}	Enable Hold Time	0	—	0	—	1	—	1	—	1	—	ns
t_{LDS}	Load Set-up Time	3.5	—	3.5	—	4	—	5	—	6	—	ns
t_{LDH}	Load Hold Time	6.5	—	8.5	—	10	—	10	—	10	—	ns
t_{RS}	Reset Pulse Width[3]	10	—	12	—	15	—	20	—	25	—	ns
t_{RSS}	Reset Set-up Time	10	—	12	—	15	—	20	—	25	—	ns
t_{RSR}	Reset Recovery Time	10	—	12	—	15	—	20	—	25	—	ns
t_{RSF}	Reset to Flag and Output Time	—	10	—	12	—	15	—	20	—	25	ns
t_{FWFT}	Mode Select Time	0	—	0	—	0	—	0	—	0	—	ns
t_{RTS}	Retransmit Set-Up Time	3.5	—	3.5	—	4	—	5	—	6	—	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	0	—	0	—	0	—	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid	3	7	3	7.5	3	8	3	10	3	13	ns
t_{OHZ}	Output Enable to Output in High Z[4]	3	7	3	7.5	3	8	3	10	3	13	ns
t_{WFF}	Write Clock to $\overline{FF}$ or $\overline{IR}$	—	8	—	9	—	10	—	12	—	15	ns
t_{REF}	Read Clock to $\overline{EF}$ or $\overline{OR}$	—	8	—	9	—	10	—	12	—	15	ns
t_{PAF}	Write Clock to $\overline{PAF}$	–	8	—	9	—	10	—	12	—	15	ns
t_{PAE}	Read Clock to $\overline{PAE}$	—	8	—	9	—	10	—	12	—	15	ns
t_{HF}	Clock to $\overline{HF}$	—	16	—	18	—	20	—	22	—	25	ns
t_{SKEW1}	Skew time between RCLK and WCLK for $\overline{FF}$ and $\overline{IR}$	8	—	10	—	12	—	15	—	20	—	ns
t_{SKEW2}	Skew time between RCLK and WCLK for $\overline{PAE}$ and $\overline{PAF}$	15	—	18	—	21	—	25	—	35	—	ns

3097 tbl 06

NOTES:

1. All AC timings apply to both Standard IDT Mode and First Word Fall Through Mode.
2. For the RCLK line: t_{CLKL} (min.) = 7 ns only when reading the offsets from the programmable flag registers; otherwise, use the table value. For the WCLK line, use the t_{CLKL} (min.) value given in the table.
3. Pulse widths less than minimum values are not allowed.
4. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

3097 tbl 08

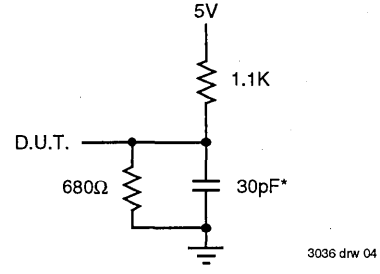


Figure 1. Output Load
* Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0 - D_8)
Data inputs for 9-bit wide data.

CONTROLS:

MASTER RESET ($\overline{MRS}$)
A Master Reset is accomplished whenever the Master Reset ($\overline{MRS}$) input is taken to a LOW state. This operation sets the internal read and write pointers to the first location of the RAM array. $\overline{PAE}$ will go LOW, $\overline{PAF}$ will go HIGH, and $\overline{HF}$ will go HIGH.

If FWFT is LOW during Master Reset then the IDT Standard Mode, along with $\overline{EF}$ and $\overline{FF}$ are selected. $\overline{EF}$ will go LOW and $\overline{FF}$ will go HIGH. If FWFT is HIGH, then the First Word Fall through Mode (FWFT), along with $\overline{IR}$ and $\overline{OR}$, are selected. $\overline{OR}$ will go HIGH and $\overline{IR}$ will go LOW.

If $\overline{LD}$ is LOW during Master Reset, then $\overline{PAE}$ is assigned a threshold 127 words from the empty boundary and $\overline{PAF}$ is assigned a threshold 127 words from the full boundary; 127 words corresponds to an offset value of 07FH. Following Master Reset, parallel loading of the offsets is permitted, but not serial loading.

If $\overline{LD}$ is HIGH during Master Reset, then $\overline{PAE}$ is assigned a threshold 1023 words from the empty boundary and $\overline{PAF}$ is assigned a threshold 1023 words from the full boundary; 1023 words corresponds to an offset value of 3FFH. Following Master Reset, serial loading of the offsets is permitted, but not parallel loading.

Regardless of whether serial or parallel offset loading has been selected, parallel reading of the registers is always permitted. (See section describing the $\overline{LD}$ line for further details).

During a Master Reset, the output register is initialized to all zeroes. A Master Reset is required after power up, before a write operation can take place. $\overline{MRS}$ is asynchronous.

PARTIAL RESET ($\overline{PRS}$)
A Partial Reset is accomplished whenever the Partial Reset ($\overline{PRS}$) input is taken to a LOW state. As in the case of the Master Reset, the internal read and write pointers are set to the first location of the RAM array, $\overline{PAE}$ goes LOW, $\overline{PAF}$ goes HIGH, and $\overline{HF}$ goes HIGH.

Whichever mode is active at the time of partial reset, IDT Standard Mode or First Word Fall-through, that mode will remain selected. If the IDT Standard Mode is active, then $\overline{FF}$ will go HIGH and $\overline{EF}$ will go LOW. If the First word Fall-through Mode is active, then $\overline{OR}$ will go HIGH, and $\overline{IR}$ will go LOW.

Following Partial Reset, all values held in the offset registers remain unchanged. The programming method (parallel or serial) currently active at the time of Partial Reset is also retained. The output register is initialized to all zeroes. $\overline{PRS}$ is asynchronous.

A Partial Reset is useful for resetting the device during the course of operation, when reprogramming flag settings may not be convenient.

RETRANSMIT ($\overline{RT}$)
The Retransmit operation allows data that has already been read to be accessed again. There are two stages: first, a setup procedure that resets the read pointer to the first location of memory, then the actual retransmit, which consists of reading out the memory contents, starting at the beginning of memory.

Retransmit Setup is initiated by holding $\overline{RT}$ LOW during a rising RCLK edge. $\overline{REN}$ and $\overline{WEN}$ must be HIGH before bringing $\overline{RT}$ LOW. At least one word, but no more than Full - 2 words should have been written into the FIFO between Reset (Master or Partial) and the time of Retransmit Setup (Full = 16,384 words for the 72261, 32,768 words for the 72271).

If IDT Standard mode is selected, the FIFO will mark the beginning of the Retransmit Setup by setting $\overline{EF}$ LOW. The change in level will only be noticeable if $\overline{EF}$ was HIGH before setup. During this period, the internal read pointer is initialized to the first location of the RAM array.

When $\overline{EF}$ goes HIGH, Retransmit Setup is complete and read operations may begin starting with the first location in memory. Since IDT Standard Mode is selected, every word read including the first word following Retransmit Setup requires a LOW on $\overline{REN}$ to enable the rising edge of RCLK. Writing operations can begin after one of two conditions have been met: $\overline{EF}$ is HIGH or 14 cycles of the faster clock (RCLK or WCLK) have elapsed since the RCLK rising edge enabled by the $\overline{RT}$ pulse.

The deassertion time of $\overline{EF}$ during Retransmit Setup is variable. The parameter t_{RTF1}, which is measured from the rising RCLK edge enabled by $\overline{RT}$ to the rising edge of $\overline{EF}$ is described by the following equation:

$$t_{RTF1}\ \text{max.} = 14*T_f + 3*T_{RCLK}\ \text{(in ns)}$$

where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period.

Regarding $\overline{FF}$: Note that since no more than Full - 2 writes are allowed between a Reset and a Retransmit Setup, $\overline{FF}$ will remain HIGH throughout the setup procedure.

For IDT Standard mode, updating the $\overline{PAE}$, $\overline{HF}$, and $\overline{PAF}$ flags begins with the "first" $\overline{REN}$-enabled rising RCLK edge following the end of Retransmit Setup (the point at which $\overline{EF}$ goes HIGH). This same RCLK rising edge is used to access the "first" memory location. $\overline{HF}$ is updated on the first RCLK rising edge. $\overline{PAE}$ is updated after two more rising RCLK edges. $\overline{PAF}$ is updated after the "first" rising RCLK edge, followed by the next two rising WCLK edges. (If the t_{skew2} specification is not met, add one more WCLK cycle.)

If FWFT mode is selected, the FIFO will mark the beginning of the Retransmit Setup by setting $\overline{OR}$ HIGH. The change in level will only be noticeable if $\overline{OR}$ was LOW before setup. During this period, the internal read pointer is set to the first location of the RAM array.

5

When $\overline{OR}$ goes LOW, Retransmit Setup is complete; at the same time, the contents of the first location are automatically displayed on the outputs. Since FWFT Mode is selected, the first word appears on the outputs, no read request necessary. Reading all subsequent words requires a LOW on $\overline{REN}$ to enable the rising edge of RCLK. Writing operations can begin after one of two conditions have been met: $\overline{OR}$ is LOW or 14 cycles of the faster clock (RCLK or WCLK) have elapsed since the RCLK rising edge enabled by the $\overline{RT}$ pulse.

The assertion time of $\overline{OR}$ during Retransmit Setup is variable. The parameter t_{RTF2}, which is measured from the rising RCLK edge enabled by $\overline{RT}$ to the falling edge of $\overline{OR}$ is described by the following equation:

$$t_{RTF2}\ max. = 14*Tf + 4*T_{RCLK}\ (in\ ns)$$

where Tf is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period. Note that a Retransmit Setup in FWFT mode requires one more RCLK cycle than in IDT Standard mode.

Regarding $\overline{IR}$: Note that since no more than Full - 2 writes are allowed between a Reset and a Retransmit Setup, $\overline{IR}$ will remain LOW throughout the setup procedure.

For FWFT mode, updating the $\overline{PAE}$, $\overline{HF}$, and $\overline{PAF}$ flags begins with the "last" rising edge of RCLK before the end of Retransmit Setup. This is the same edge that asserts $\overline{OR}$ and automatically accesses the first memory location. Note that, in this case, $\overline{REN}$ is not required to initiate flag updating. $\overline{HF}$ is updated on the "last" RCLK rising edge. $\overline{PAE}$ is updated after two more rising RCLK edges. $\overline{PAF}$ is updated after the "last" rising RCLK edge, followed by the next two rising WCLK edges. (If the t_{SKEW2} specification is not met, add one more WCLK cycle.)

$\overline{RT}$ is synchronized to RCLK. The Retransmit operation is useful in the event of a transmission error on a network, since it allows a data packet to be resent.

FIRST WORD FALL THROUGH/SERIAL IN (FWFT/SI)

This is a dual purpose pin. During Master Reset, the state of the FWFT/SI helps determine whether the device will operate in IDT Standard mode or First Word Fall Through (FWFT) mode.

If, at the time of Master Reset, FWFT/SI is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}$) to indicate whether or not there are any words present in the FIFO memory. It also uses the Full Flag function ($\overline{FF}$) to indicate whether or not the FIFO memory has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable ($\overline{REN}$) line.

If, at the time of Master Reset, FWFT/SI is HIGH, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}$) to indicate whether or not there is valid data at the data outputs (Q_n). It also uses Input Ready ($\overline{IR}$) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Q_n, no read request necessary. Subsequent words must be accessed using the Read Enable ($\overline{REN}$) line.

After Master Reset, FWFT/SI acts as a serial input for loading $\overline{PAE}$ and $\overline{PAF}$ offsets into the programmable registers. The serial input function can only be used when the serial loading method has been selected during Master Reset. FWFT/SI functions the same way in both IDT Standard and FWFT modes.

WRITE CLOCK (WCLK)

A write cycle is initiated on the rising edge of the write clock (WCLK). Data set-up and hold times must be met with respect to the LOW-to-HIGH transition of the WCLK. The write and read clocks lines can either be asynchronous or coincident.

WRITE ENABLE ($\overline{WEN}$)

When Write Enable ($\overline{WEN}$) is LOW, data can be loaded into the input register on the rising edge of every WCLK cycle. Data is stored in the RAM array sequentially and independently of any on-going read operation.

When $\overline{WEN}$ is HIGH, the input register holds the previous data and no new data is loaded into the FIFO.

To prevent data overflow in the IDT Standard Mode, $\overline{FF}$ will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{FF}$ will go HIGH allowing a write to occur. $\overline{WEN}$ is ignored when the FIFO is full.

To prevent data overflow in the FWFT mode, $\overline{IR}$ will go HIGH, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{IR}$ will go LOW allowing a write to occur. $\overline{WEN}$ is ignored when the FIFO is full.

READ CLOCK (RCLK)

Data can be read on the outputs, on the rising edge of the read clock (RCLK), when Output Enable ($\overline{OE}$) is set LOW. The write and read clocks can be asynchronous or coincident.

READ ENABLE ($\overline{REN}$)

When Read Enable ($\overline{REN}$) is LOW, data is loaded from the RAM array into the output register on the rising edge of the RCLK.

When $\overline{REN}$ is HIGH, the output register holds the previous data and no new data is loaded into the output register.

In the IDT Standard Mode, every word accessed at Q_n, including the first word written to an empty FIFO, must be requested using $\overline{REN}$. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty. Once a write is performed, $\overline{EF}$ will go HIGH after $t_{FWL1} + t_{REF}$ and a read is permitted.

In the FWFT Mode, the first word written to an empty FIFO automatically goes to the outputs Q_n, no need for any read request. In order to access all other words, a read must be executed using $\overline{REN}$. When all the data has been read from the FIFO, Output Ready ($\overline{OR}$) will go HIGH, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty. Once a write is performed, $\overline{OR}$ will go LOW after $t_{FWL2} + t_{REF}$, when the first word appears at Q_n; if a second word is written into the FIFO, then $\overline{REN}$ can be used to read it out.

SERIAL ENABLE ($\overline{SEN}$)

Serial Enable is ($\overline{SEN}$) is an enable used only for serial programming of the offset registers. The serial programming method must be selected during Master Reset. $\overline{SEN}$ is always used in conjunction with $\overline{LD}$. When these lines are both LOW, data at the SI input can be loaded into the input register one bit for each LOW-to-HIGH transition of WCLK.

When $\overline{SEN}$ is HIGH, the programmable registers retains the previous settings and no offsets are loaded.

$\overline{SEN}$ functions the same way in both IDT Standard and FWFT modes.

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable ($\overline{OE}$) is enabled (LOW), the parallel output buffers receive data from the output register. When $\overline{OE}$ is HIGH, the output data bus (Q_n) goes into a high impedance state.

LOAD ($\overline{LD}$)

This is a dual purpose pin. During Master Reset, the state of the Load line ($\overline{LD}$) determines one of two default values (127 or 1023) for the $\overline{PAE}$ and $\overline{PAF}$ flags, along with the method by which these flags can be programmed, parallel or serial. After Master Reset, $\overline{LD}$ enables write operations to and read operations from the registers. Only the offset loading method currently selected can be used to write to the registers. Aside from Master Reset, there is no other way change the loading method. Registers can be read only in parallel; this can be accomplished regardless of whether serial or the parallel loading has been selected.

Associated with each of the programmable flags, $\overline{PAE}$ and $\overline{PAF}$, are two registers which can either be written to or read from. Offset values contained in these registers determine how many words need to be in the FIFO memory to switch a partial flag. A LOW on $\overline{LD}$ during Master Reset selects a default $\overline{PAE}$ offset value of 07FH (a threshold 127 words from the empty boundary), a default $\overline{PAF}$ offset value of 07FH (a threshold 127 words from the full boundary), and parallel loading of other offset values. A HIGH on $\overline{LD}$ during Master Reset selects a default $\overline{PAE}$ offset value of 3FFH (a threshold 1023 words from the empty boundary), a default $\overline{PAF}$ offset value of 3FFH (a threshold 1023 words form the full boundary), and serial loading of other offset values.

The act of writing offsets (in parallel or serial) employs a dedicated write offset register pointer. The act of reading offsets employs a dedicated read offset register pointer. The

5

$\overline{LD}$	$\overline{WEN}$	$\overline{REN}$	$\overline{SEN}$	WCLK	RCLK	Selection
0	0	1	1	↑	X	Parallel write to registers: Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	0	1	X	↑	Parallel read from registers: Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	1	0	↑	X	Serial shift into registers: 28 bits for the 72261 30 bits for the 72271 1 bit for each rising WCLK edge Starting with Empty Offset (LSB) Ending with Full Offset (MSB)
0	1	1	1	X	X	No Operation
1	0	X	X	↑	X	Write Memory
1	X	0	X	X	↑	Read Memory
1	1	1	X	X	X	No Operation

3097 tbl 01

NOTES:
1. Only one of the two offset programming methods, serial or parallel, is available for use at any given time.
2. The programming method can only be selected at Master Reset.
3. Parallel reading of the offset registers is always permitted regardless of which programming method has been selected.
4. The programming sequence applies to both IDT Standard and FWFT modes.

Figure 2. Partial Flag Programming Sequence

two pointers operate independently; however, a read and a write should not be performed simultaneously to the offset registers. A Master Reset initializes both pointers to the Empty Offset (LSB) register. A Partial Reset has no effect on the position of these pointers.

Once serial offset loading has been selected, then programming $\overline{PAE}$ and $\overline{PAF}$ procedes as follows: When $\overline{LD}$ and $\overline{SEN}$ are set LOW, data on the SI input are written, one bit for each WCLK rising edge, starting with the Empty Offset LSB (8 bits for both the 72261 and 72271), then the Empty Offset MSB (6 bits for the 72261, 7 bits for the 72271) , then the Full Offset LSB (8 bits for both the 72261 and 72271), ending with the Full Offset MSB (6 bits for the 72261, 7 bits for the 72271). A total of 28 bits are necessary to program the 72261; a total of 30 bits are necessary to program the 72271. Individual registers cannot be loaded serially; rather, all four must be programmed in sequence, no padding allowed. $\overline{PAE}$ and $\overline{PAF}$ can show a valid status only after the the full set of bits have been entered. The registers can be re-programmed, as long as all four offsets are loaded. When $\overline{LD}$ is LOW and $\overline{SEN}$ is HIGH, no serial write to the registers can occur.

Once parallel offset loading has been selected, then programming $\overline{PAE}$ and $\overline{PAF}$ procedes as follows: When $\overline{LD}$ and $\overline{WEN}$ are set LOW, data on the inputs D_n are written into the LSB Empty Offset Register on the first LOW-to-HIGH transition of WCLK. Upon the second LOW-to-HIGH transition of WCLK, data at the inputs are written into the MSB Empty Offset Register. Upon the third LOW-to-HIGH transition of WCLK, data at the inputs are written into the LSB Full Offset Register. Upon the fourth LOW-to-HIGH transition of WCLK, data at the inputs are written into the MSB Full Offset Register. The fifth transition of WCLK writes, once again, to the LSB Empty Offset Register.

To ensure proper programming (serial or parallel) of the offset registers, no read operation is permitted from the time of reset (master or partial) to the time of programming. (During this period, the read pointer must be pointing to the first location of the memory array.) After the programming has been accomplished, read operations may begin.

Write operations to memory are allowed before and during the parallel programming sequence. In this case, the programming of all offset registers does not have to occur at one time. One or two offset registers can be written to and then, by bringing $\overline{LD}$ HIGH, write operations can be redirected to the FIFO memory. When $\overline{LD}$ is set LOW again, and $\overline{WEN}$ is LOW, the next offset register in sequence is written to. As an alternative to holding $\overline{WEN}$ LOW and toggling $\overline{LD}$, parallel programming can also be interrupted by setting $\overline{LD}$ LOW and toggling $\overline{WEN}$.

Write operations to memory are allowed before and during the serial programming sequence. In this case, the programming of all offset bits does not have to occur at once. A select number of bits can be written to the SI input and then, by bringing $\overline{LD}$ and $\overline{SEN}$ HIGH, data can be written to FIFO memory via D_n by toggling $\overline{WEN}$. When $\overline{WEN}$ is brought HIGH with $\overline{LD}$ and $\overline{SEN}$ restored to a LOW, the next offset bit in sequence is written to the registers via SI. If a mere interuption of serial programming is desired, it is sufficient either to set $\overline{LD}$ LOW and deactivate $\overline{SEN}$ or to set $\overline{SEN}$ LOW and deactivate $\overline{LD}$. Once $\overline{LD}$ and $\overline{SEN}$ are both restored to a LOW level, serial offset programming continues from where it left off.

Note that the status of a partial flag ($\overline{PAE}$ or $\overline{PAF}$) output is invalid during the programming process. From the time parallel programming has begun, a partial flag output will not be valid until the appropriate offset words have been written to the LSB and MSB registers pertaining to that flag. From the time serial programming has begun, neither partial flag will be valid until the full set of bits required to fill all the offset registers has been written. Measuring from the rising WCLK edge that achieves either of the above criteria; $\overline{PAF}$ will be valid after two more rising WCLK edges plus t_{PAF}, $\overline{PAE}$ will will be valid after the next two rising RCLK edges plus t_{PAE} (Add one more RCLK cycle if t_{SKEW2} is not met.)

The act of reading the offset registers employs a dedicated read offset register pointer. The contents of the offset registers can be read on the output lines when $\overline{LD}$ is set LOW and $\overline{REN}$ is set LOW; then, data are read via Q_n from the LSB Empty Offset Register on the first LOW-to-HIGH transition of RCLK. Upon the second LOW-to-HIGH transition of RCLK, data are read from the MSB Empty Offset Register. Upon the third LOW-to-HIGH transition of RCLK, data are read from the LSB Full Offset Register. Upon the fourth LOW-to-HIGH transition of RCLK, data are read from the MSB Full Offset Register. The fifth transition of RCLK reads, once again, from the LSB Empty Offset Register.

It is permissable to interrupt the the offset register access sequence with reads or writes to memory . The interruption is accomplished by deasserting $\overline{REN}$, $\overline{LD}$, or both together. When $\overline{REN}$ and $\overline{LD}$ are restored to a LOW level, access of the registers continues where it left off.

$\overline{LD}$ functions the same way in both IDT Standard and FWFT modes.

FREQUENCY SELECT INPUT (FS)

An internal state machine manages the movement of data through the Supersync FIFO. The FS line determines whether RCLK or WCLK will synchronize the state machine. Tie FS to V_{CC} if the RCLK line is running at a lower frequency than the WCLK line. In this case, the state machine will be synchronized to WCLK. Tie FS to GND if the RCLK line is running at a higher frequency than the WCLK line. In this case, the state machine will be synchronized to RCLK. Note that FS must be set so the clock line running at the higher frequency drives the state machine; this ensures efficient handling of the data within the FIFO. If the same clock signal drives both the WCLK and the RCLK pins, then tie FS to GND.

The frequency of the clock tied to the state machine (referred to as the "selected clock") may be changed at any time, so long as it is always greater than or equal to the frequency of the clock that is not tied to the state machine (referred to as the "non-selected clock"). The frequency of the non-selected clock can also be varied with time, so long as it never exceeds the frequency of the selected clock. To be more specific, the frequencies of both RCLK and WCLK may be varied during FIFO operation, provided that, at any given point in time, the cycle period of the selected clock is

equal to or less than the cycle period of the non-selected clock.

The selected clock must be continuous. It is, however, permissible to stop the non-selected clock. Note, so long as RCLK is idle, $\overline{EF}/\overline{OR}$ and $\overline{PAE}$ will not be updated. Likewise, as long as WCLK is idle, $\overline{FF}/\overline{IR}$ and $\overline{PAF}$ will not be updated.

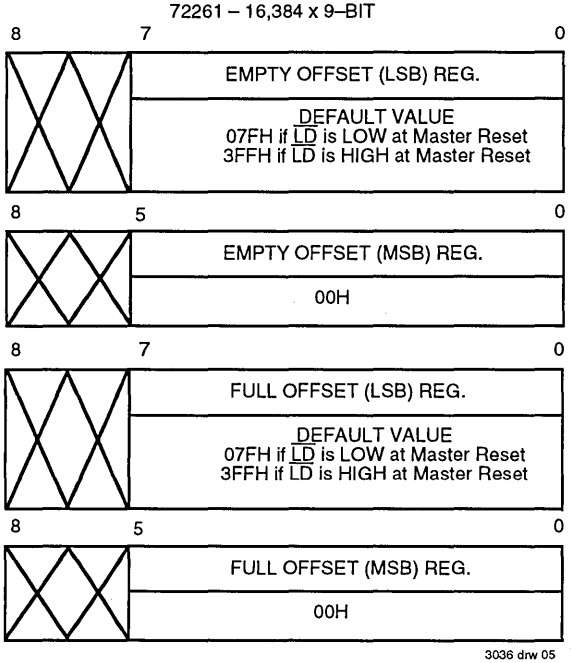
Changing the FS setting during FIFO operation (i.e. reading or writing) is not permitted; however, such a change at the time of Master Reset or Partial Reset is all right. FS is an asynchronous input.

OUTPUTS:

FULL FLAG ($\overline{FF}/\overline{IR}$)

This is a dual purpose pin. In IDT Standard Mode, the Full Flag ($\overline{FF}$) function is selected. When the FIFO is full (i.e. the write pointer catches up to the read pointer), $\overline{FF}$ will go LOW, inhibiting further write operation. When $\overline{FF}$ is HIGH, the FIFO is not full. If no reads are performed after a reset (either $\overline{MRS}$ or $\overline{PRS}$), $\overline{FF}$ will go LOW after 16,384 writes tor the IDT72261 and 32,768 writes to the IDT72271.

In FWFT Mode, the Input Ready ($\overline{IR}$) function is selected. $\overline{IR}$ goes LOW when memory space is available for writing in data. When there is no longer any free space left, $\overline{IR}$ goes HIGH, inhibiting further write operation. If no reads are performed after a reset (either $\overline{MRS}$ or $\overline{PRS}$), $\overline{IR}$ will go HIGH after 16,385 writes for the IDT72261 and 32,769 writes for the IDT72271.



The $\overline{IR}$ status not only measures the contents of the FIFO memory, but also counts the presence of a word in the output register. Thus, in FWFT mode, the total number of writes necessary to deassert $\overline{IR}$ is one greater than needed to assert $\overline{FF}$ in IDT Standard mode.

$\overline{FF}/\overline{IR}$ is synchronized to WCLK. It is double-registered to enhance metastable immunity.

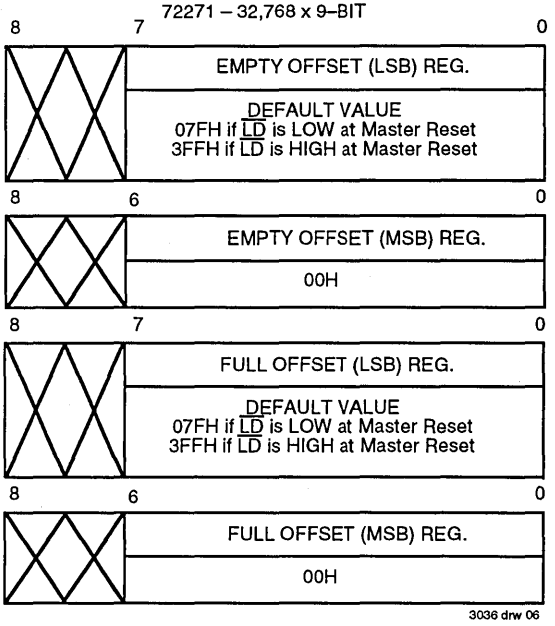
EMPTY FLAG ($\overline{EF}/\overline{OR}$)

This is a dual purpose pin. In the IDT Standard Mode, the Empty Flag ($\overline{EF}$) function is selected. When the FIFO is empty (i.e. the read pointer catches up to the write pointer), $\overline{EF}$ will go LOW, inhibiting further read operations. When $\overline{EF}$ is HIGH, the FIFO is not empty.

When writing the first word to an empty FIFO, the deassertion time of $\overline{EF}$ is variable, and can be represent by the First Word Latency parameter, t_{FWL1}, which is measured from the rising WCLK edge that writes the first word to the rising RCLK edge that updates the flag. t_{FWL1} includes any delays due to clock skew and can be expressed as follows:

$$t_{FWL1} \text{ max.} = 10*T_f + 2*T_{RCLK} \text{ (in ns)}$$

where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period. Since no read can take place until $\overline{EF}$ goes HIGH, the t_{FWL1} delay determines how early the first word can be available at Q_n. This delay has no effect on the reading of subsequent words.



NOTE:
1. Any bits of the offset register not being programmed should be set to zero.

Figure 3. Offset Register Location and Default Values

In FWFT Mode, the Ouput Ready ($\overline{OR}$) function is selected. $\overline{OR}$ goes LOW at the same time that the first word written to an empty FIFO appears valid on the outputs. $\overline{OR}$ goes HIGH one cycle after RCLK shifts the last word from the FIFO memory to the outputs. Then further data reads are inhibited until $\overline{OR}$ goes LOW again.

When writing the first word to an empty FIFO, the assertion time of $\overline{OR}$ is variable, and can be represented by the First Word Latency parameter, t_{FWL2}, which is measured from the rising WCLK edge that writes the first word to the rising RCLK edge that updates the flag. t_{FWL2} includes any delay due to clock skew and can be expressed as follows:

$$t_{FWL2} \text{ max.} = 10*T_f + 3*T_{RCLK} \text{ (in ns)}$$

where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period. Note that the First Word Latency in FWFT mode is one RCLK cycle longer than in IDT Standard mode. The t_{FWL2} delay determines how early the first word can be available at Q_n. This delay has no effect on the reading of subsequent words.

$\overline{EF}/\overline{OR}$ is sychronized to the RCLK. It is double-registered to enhance metastable immunity.

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

The Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW when the FIFO reaches the Almost-Full condition as specified by the offset m stored in the Full Offset register.

At the time of Master Reset, depending on the state of $\overline{LD}$, one of two possible default offset values are chosen. If $\overline{LD}$ is

TABLE I — STATUS FLAGS FOR IDT STANDARD MODE

Number of Words in FIFO Memory (1)						
72261	72271	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	H	H	H	L	L
1 to n(2)	1 to n(2)	H	H	H	L	H
(n+1) to 8,192	(n+1) to16,384	H	H	H	H	H
8,193 to (16,384-(m+1))	16,385 to (32,768-(m+1))	H	H	L	H	H
(16,384-m)(3) to 16,383	(32,768-m)(3) to 32,767	H	L	L	H	H
16,384	32,768	L	L	L	H	H

3097 tbl 03

NOTES:
1. Data in the output register does not count as a "word in FIFO memory". Since, in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
2. n = Empty Offset, Default Values: n = 127 when parallel offset loading is selected or n=1023 when serial offset loading is selected.
3. m = Full Offset, Default Values: m = 127 when parallel offset loading is selected or n=1023 when serial offset loading is selected.

TABLE II — STATUS FLAGS FOR FWFT MODE

Number of Words in FIFO Memory (1)						
72261	72271	$\overline{IR}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{OR}$
0	0	L	H	H	L	H(4)
1 to n(2)	1 to n(2)	L	H	H	L	L
(n+1) to 8,192	(n+1) to16,384	L	H	H	H	L
8,193 to (16,384-(m+1))	16,385 to (32,768-(m+1))	L	H	L	H	L
(16,384-m)(3) to 16,383	(32,768-m)(3) to 32,767	L	L	L	H	L
16,384	32,768	H	L	L	H	L

3097 tbl 04

NOTES:
1. Data in the output register does not count as a "word in FIFO memory". Since, in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
2. n = Empty Offset, Default Values: n = 127 when parallel offset loading is selected or n=1023 when serial offset loading is selected.
3. m = Full Offset, Default Values: m = 127 when parallel offset loading is selected or n=1023 when serial offset loading is selected.
4. Following a reset (Master or Partial), the FIFO memory is empty and $\overline{OR}$ = HIGH. After writing the first word, the FIFO memory remains empty, the data is placed into the output register, and $\overline{OR}$ goes LOW. In this case, or any time the last word in the FIFO memory has been read into the output register; a rising RCLK edge, enabled by $\overline{REN}$, will set $\overline{OR}$ HIGH.

LOW, then m = 07FH and the $\overline{PAF}$ switching threshold is 127 words from the Full boundary, if $\overline{LD}$ is HIGH, then m = 3FFH and the $\overline{PAF}$ switching threshold is 1023 words away from the Full boundary.

Any integral value of m from 0 to the maximum FIFO depth minus 1 (16,383 words for the 72261, 32,767 words for the 72271) can be programmed into the Full Offset register.

In IDT Standard Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{PAF}$ will go LOW after (16,384-m) writes to the IDT72261, and (32,768-m) writes to the IDT72271.

In FWFT Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{PAF}$ will go LOW after (16,385-m) writes to the IDT72261, and (32,769-m) writes to the IDT72271. In this case, the first word written to an empty FIFO does not stay in memory, but goes unrequested to the output register; therefore, it has no effect on determining the state of $\overline{PAF}$.

Note that even though $\overline{PAF}$ is programmed to switch LOW during the first word latency period (tFWL), attempts to read data will be ignored until $\overline{EF}$ goes HIGH indicating that data is available at the output port. This is true for both timing modes.

$\overline{PAF}$ is synchronous and updated on the rising edge of WCLK. It is double-registered to enhance metastable immunity.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

The Programmable Almost-Empty Flag ($\overline{PAE}$) will go LOW when the FIFO reaches the Almost-Empty condition as specified by the offset n stored in the Empty Offset register.

At the time of Master Reset, depending on the state of $\overline{LD}$, one of two possible default offset values are chosen. If $\overline{LD}$ is LOW, then n = 07FH and the $\overline{PAE}$ switching threshold is 127 words from the Empty boundary, if $\overline{LD}$ is HIGH, then n = 3FFH and the $\overline{PAE}$ switching threshold is 1023 words away from the Empty boundary.

Any integral value of n from 0 to the maximum FIFO depth minus 1 (16,383 words for the 72261, 32,767 words for the 72271) can be programmed into the Empty Offset register.

In IDT Standard Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{PAE}$ will go HIGH after (n + 1) writes to the IDT72261/72271.

In FWFT Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{PAE}$ will go HIGH after (n+2) writes to the IDT72261/72271. In this case, the first word written to an empty FIFO does not stay in memory, but goes unrequested to the output register; therefore, it has no effect on determining the state of $\overline{PAE}$.

Note that even though $\overline{PAE}$ is programmed to switch HIGH during the first word latency period (tFWL), attempts to read data will be ignored until $\overline{EF}$ goes HIGH indicating that data is available at the output port. This is true for both timing modes.

$\overline{PAE}$ is synchronous and updated on the rising edge of RCLK. It is double-registered to enhance metastable immunity.

HALF-FULL FLAG ($\overline{HF}$)

This output indicates a half-full memory. The rising WCLK edge that fills the memory beyond half-full sets $\overline{HF}$ LOW. The flag remains LOW until the difference between the write and read pointers becomes less than or equal to one half of the total depth of the device, the rising RCLK edge that accomplishes this condition also sets $\overline{HF}$ HIGH.

In IDT Standard Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{HF}$ will go LOW after (D/2 + 1) writes, where D is the maximum FIFO depth (16,384 words for the IDT72261, 32,768 words for the IDT72271).

In FWFT Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{HF}$ will go LOW after (D/2+2) writes to the IDT72261/72271. In this case, the first word written to an empty FIFO does not stay in memory, but goes unrequested to the output register; therefore, it has no effect on determining the state of $\overline{HF}$.

Because $\overline{HF}$ uses both RCLK and WCLK for synchronization purposes, it is asynchronous.

DATA OUTPUTS (Q_0-Q_8)

Q_0-Q_8 are data outputs for 9-bit wide data.

5

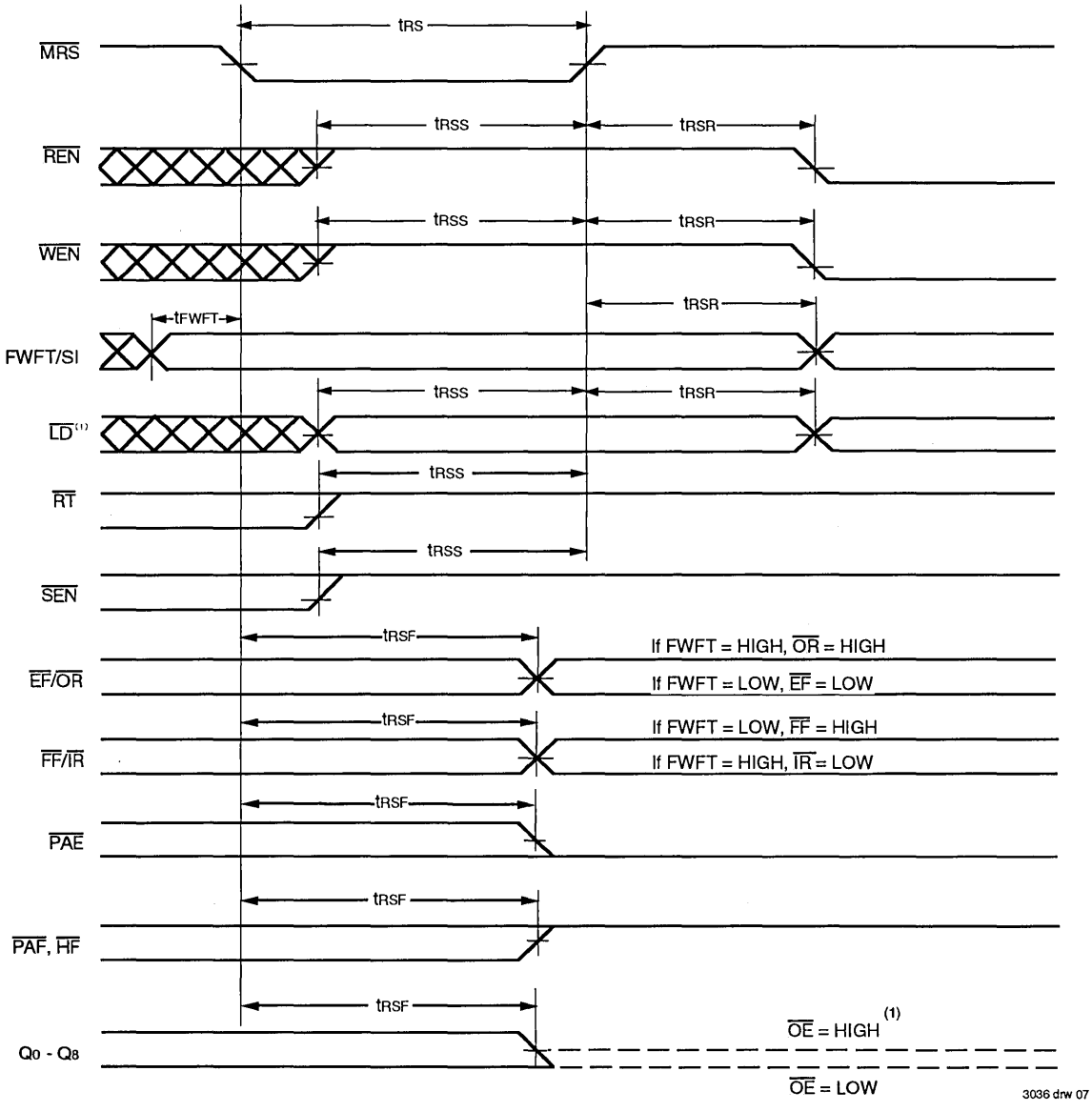


Figure 4. Master Reset Timing

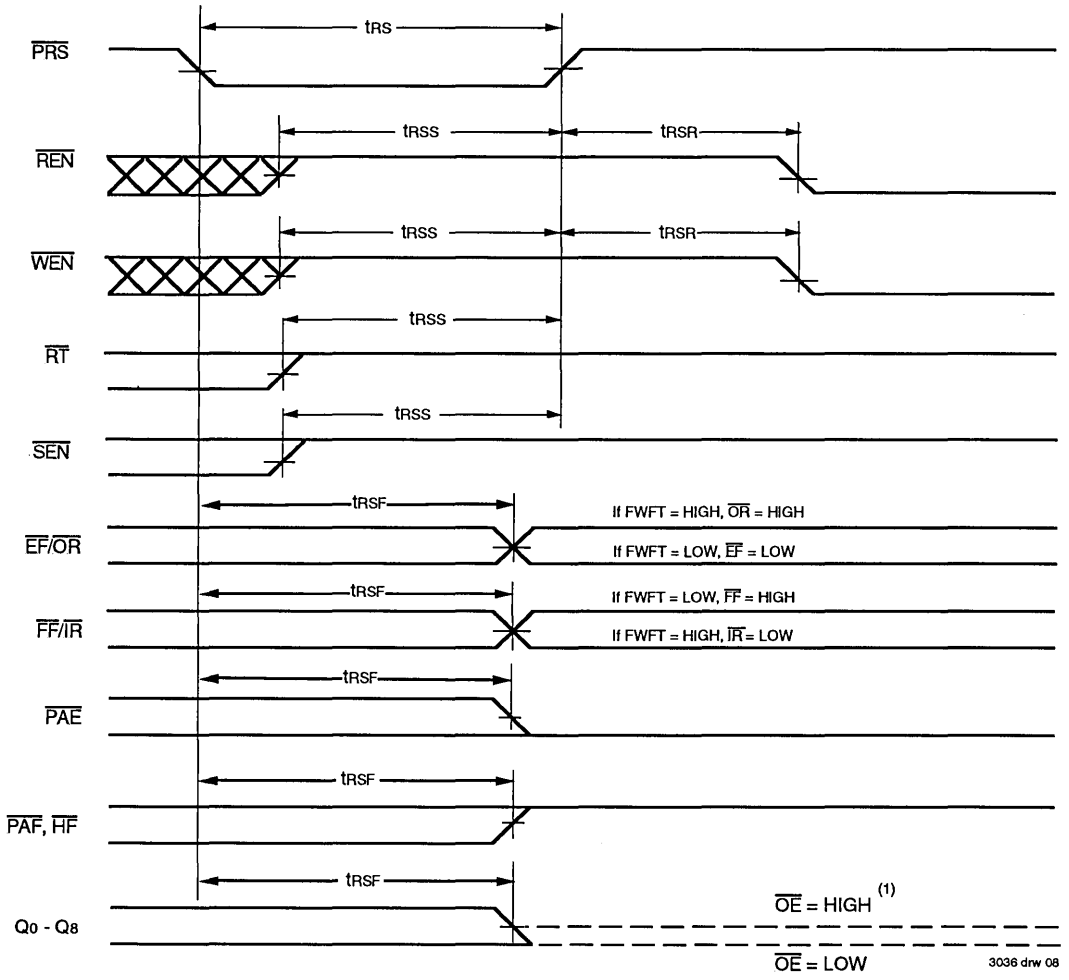
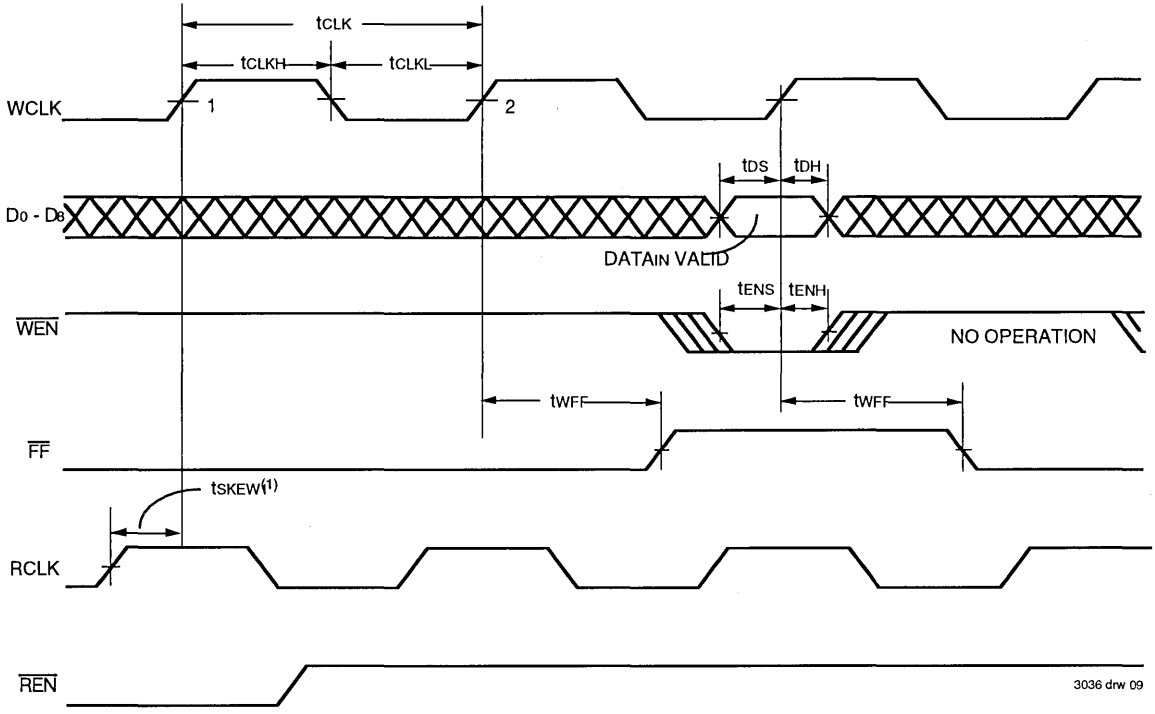
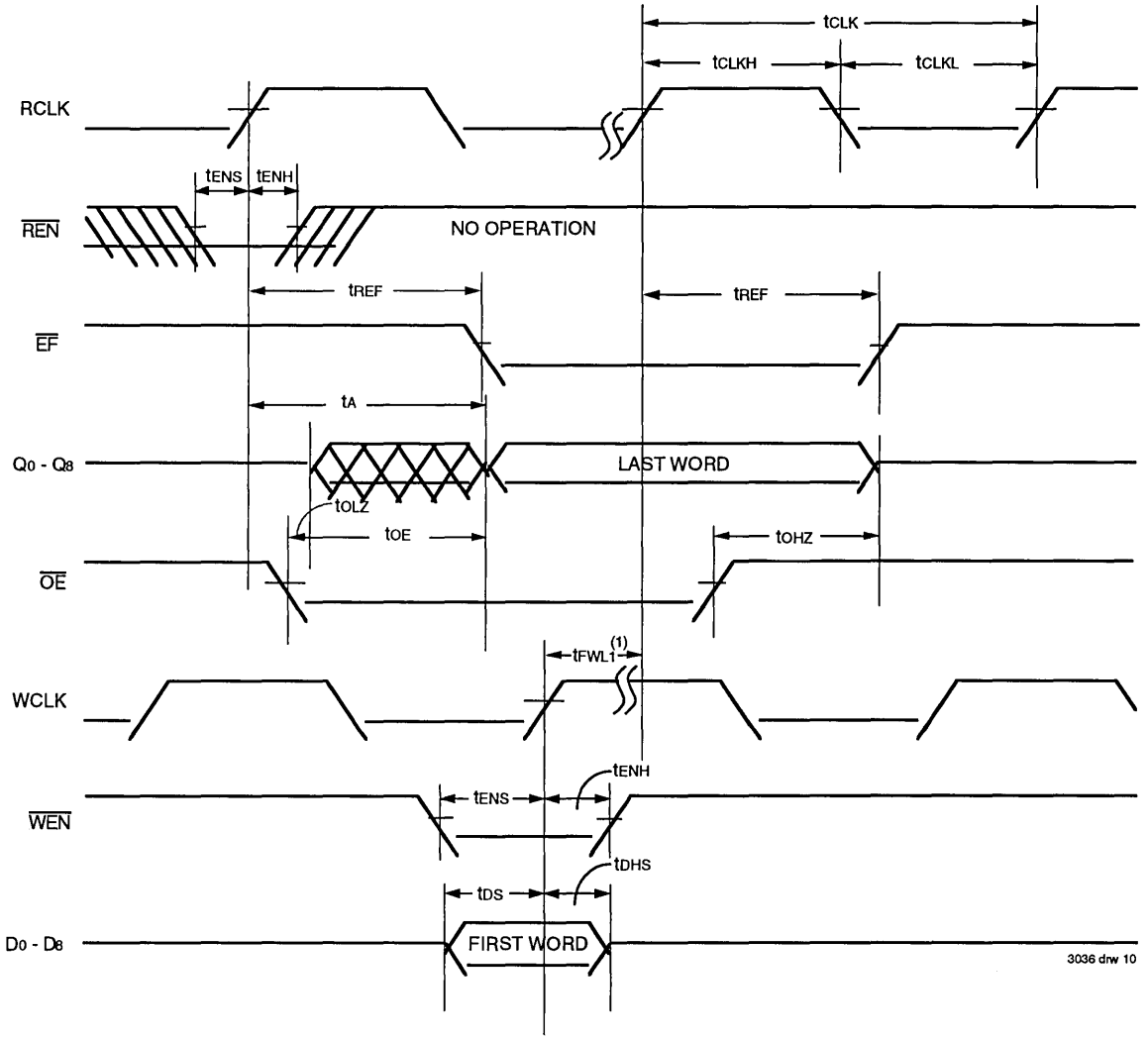


Figure 5. Partial Reset Timing



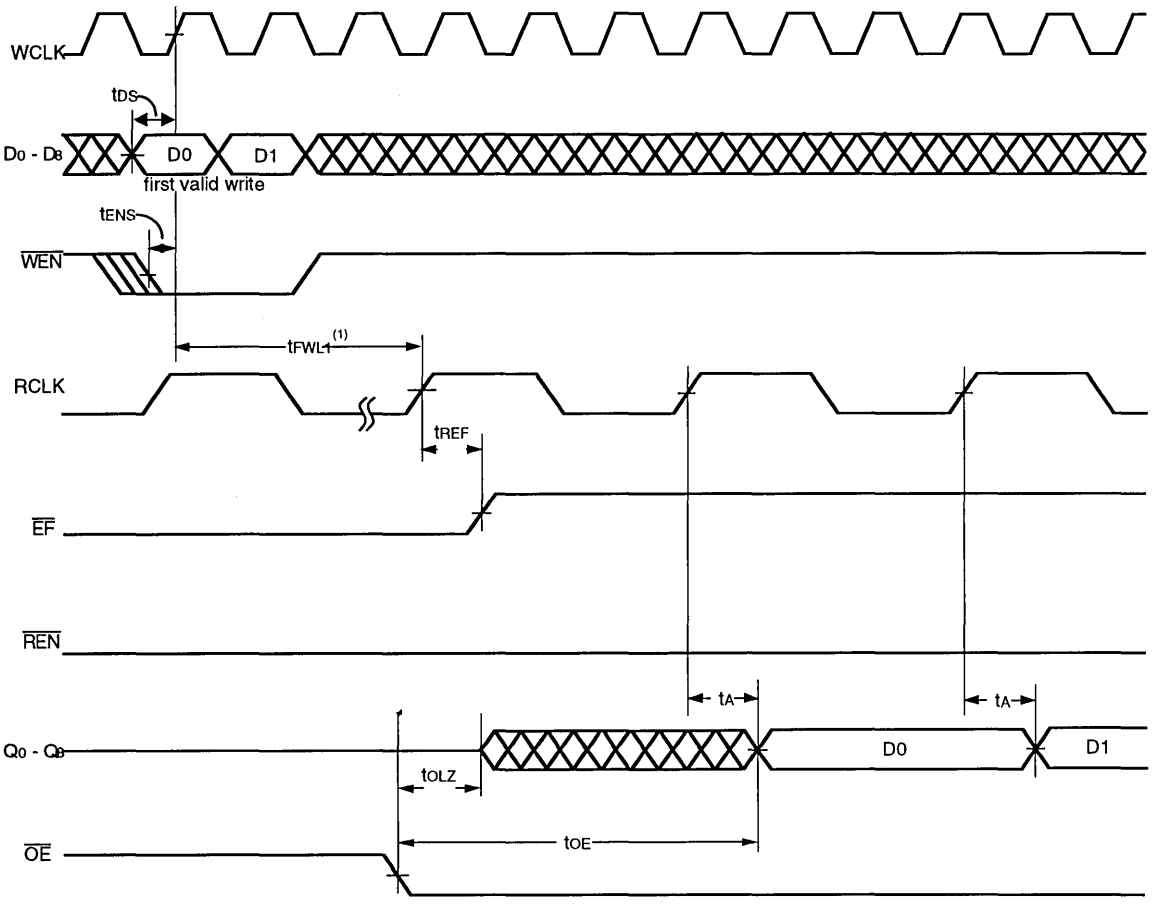
NOTES:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH (after one WCLK cycle plus t_{WFF}). If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then the $\overline{FF}$ deassertion may be delayed an extra WCLK cycle.
2. $\overline{LD}$ = HIGH

Figure 6. Write Cycle Timing (IDT Standard Mode)



NOTES:
1. t_{FWL1} contributes a variable delay to the overall first word latency (this parameter includes delays due to skew):
   t_{FWL1} max. (in ns) = 10*T_f + 2* T_{RCLK}
   where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period
2. $\overline{LD}$ = HIGH

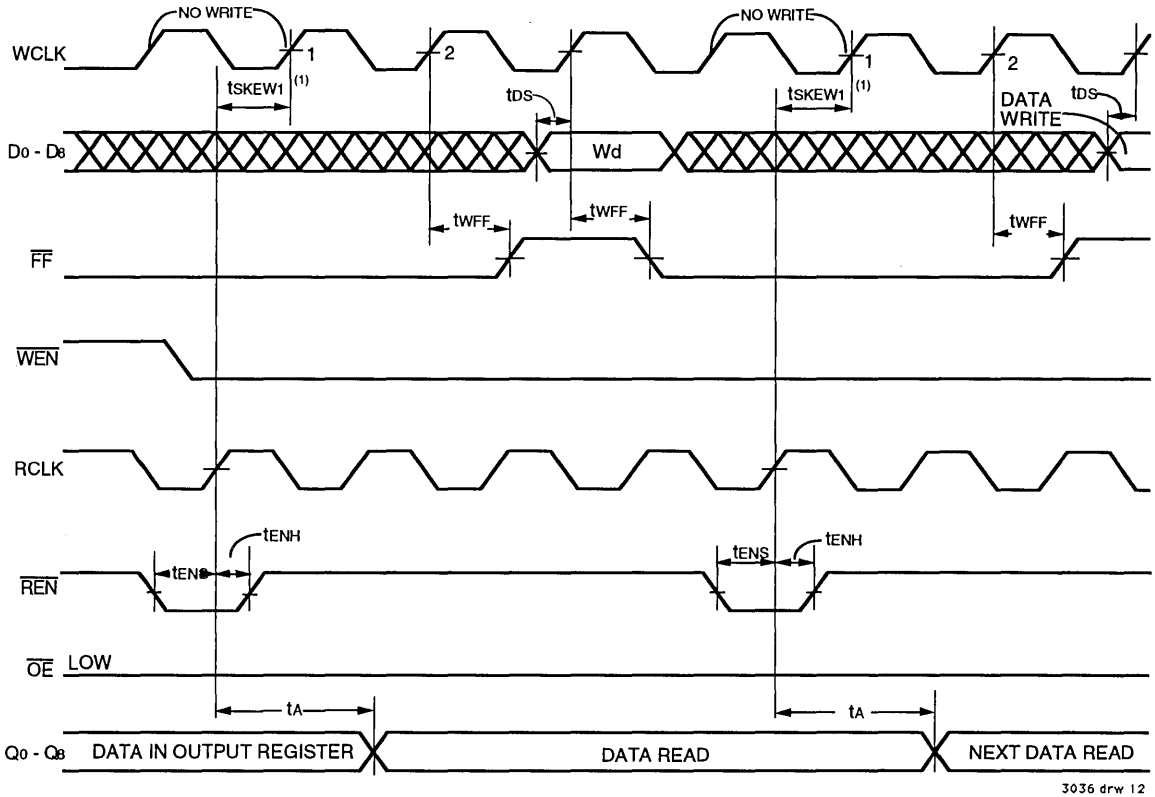
Figure 7. Read Cycle Timing (IDT Standard Mode)



3036 drw 11

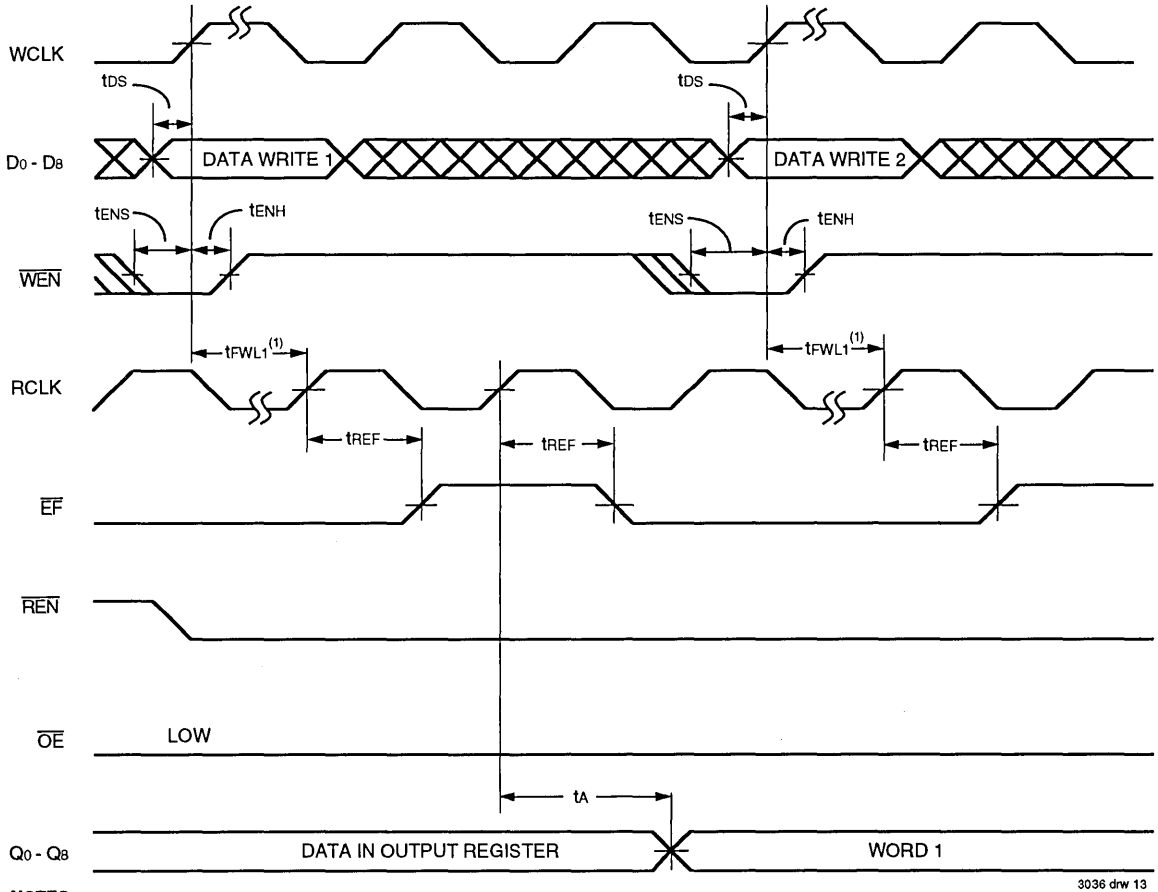
NOTES:
1. t_{FWL1} max. (in ns) = 10* T_f + 2* T_{RCLK}
   Where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period
2. $\overline{LD}$ = HIGH

Figure 8. First Data Word Latency (IDT Standard Mode)



NOTES:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go high (after one WCLK cycle pus t_{WFF}). If the time between the rising edge of the RCLK and the rising edge of the WCLK is less than t_{SKEW1}, then the $\overline{FF}$ deassertion may be delayed an extra WCLK cycle.
2. $\overline{LD}$ = HIGH

Figure 9. Full Flag Timing (IDT Standard Mode)



NOTES:
1. t_{FWL1} max. (in ns) = 10*T_f + 2*T_{RCLK}
   Where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the period.
2. $\overline{LD}$ = HIGH

Figure 10. Empty Flag Timing (IDT Standard Mode)

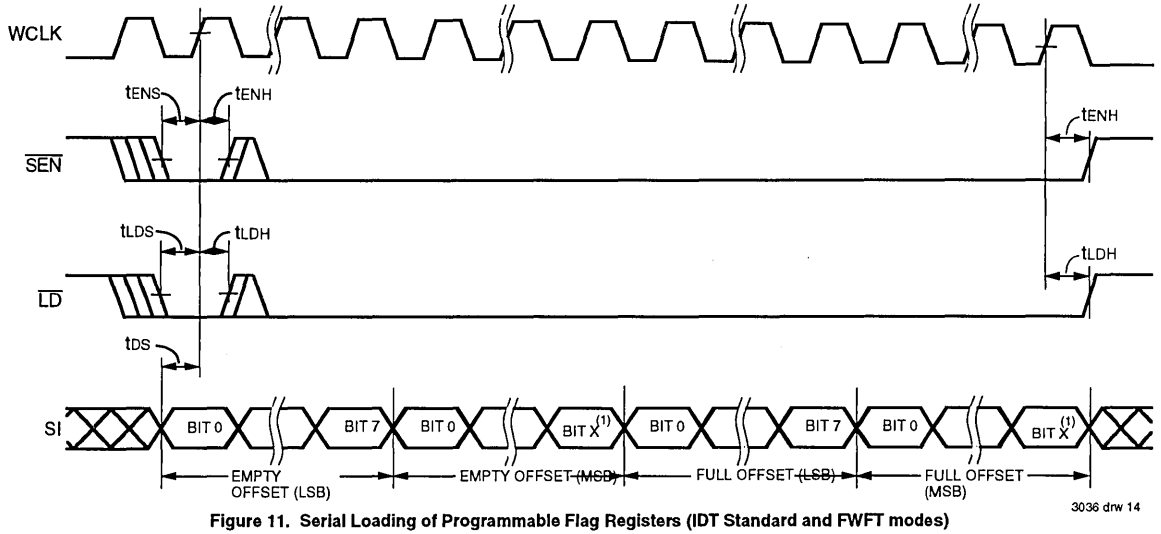


Figure 11. Serial Loading of Programmable Flag Registers (IDT Standard and FWFT modes)

NOTE:
1. For the 72261, X = 5.
   For the 72271, X = 6.

5

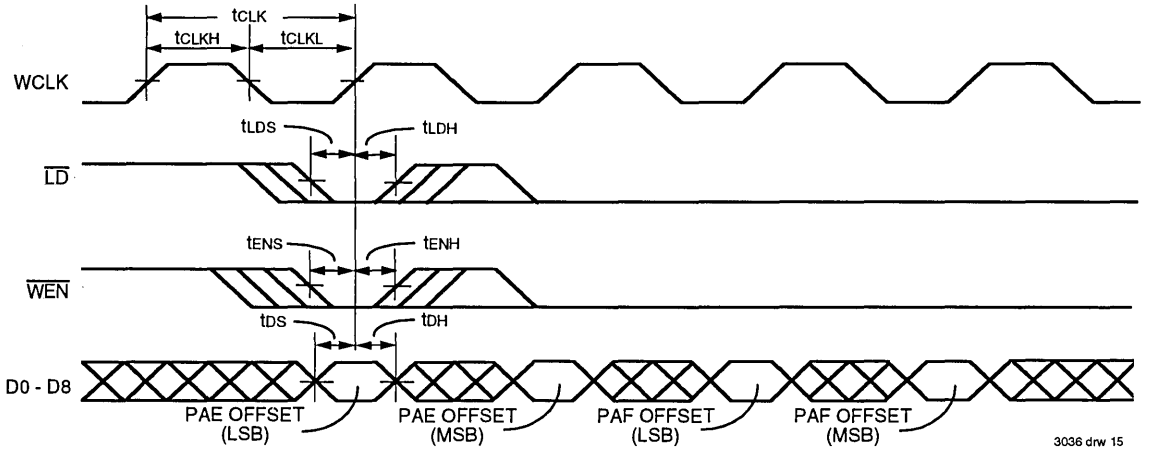


Figure 12. Parallel Loading of Programmable Flag Registers (IDT Standard and FWFT modes)

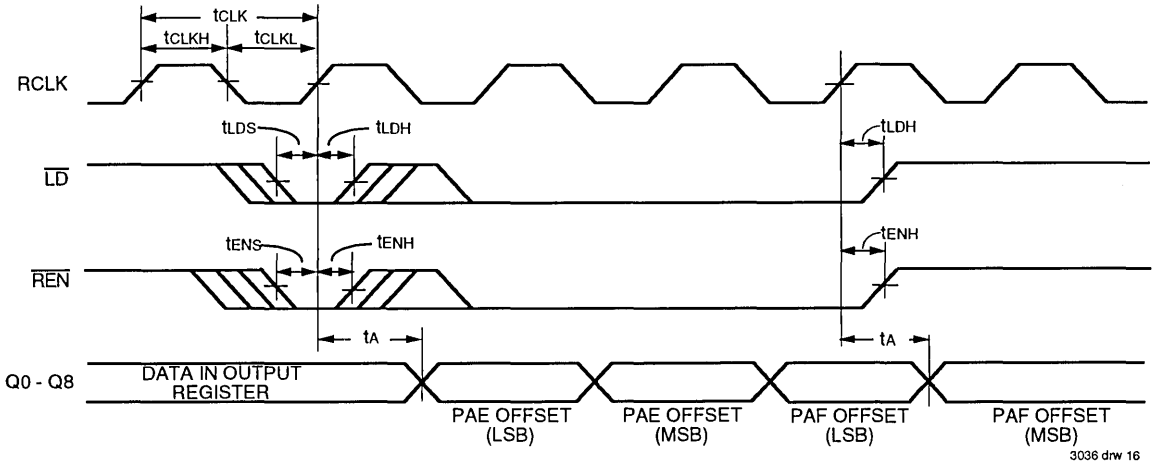
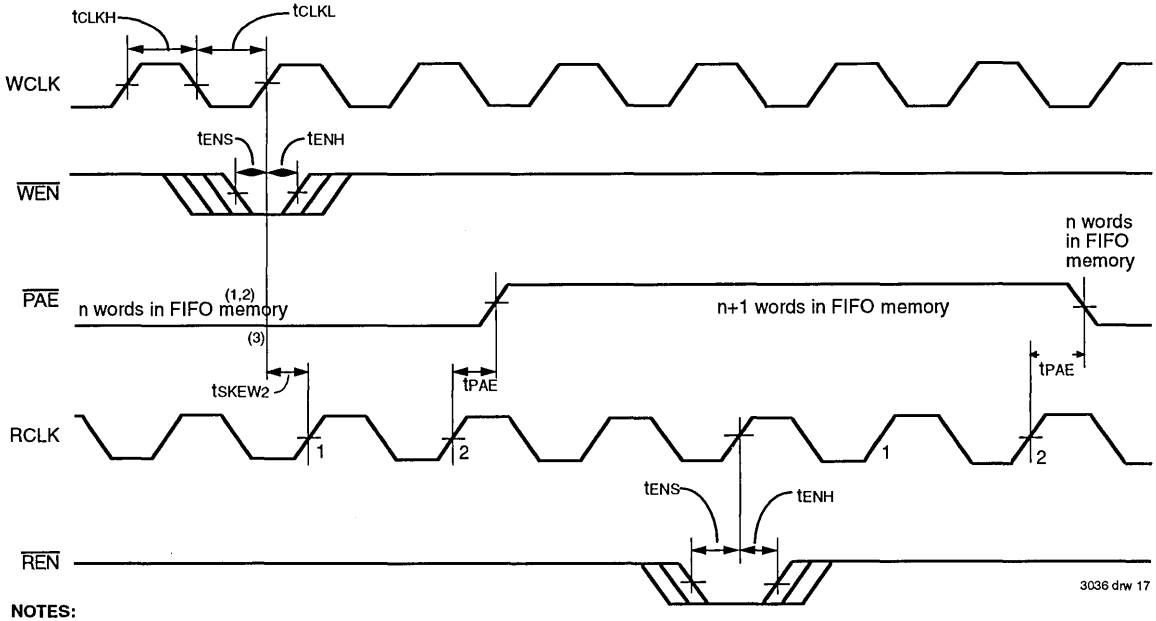


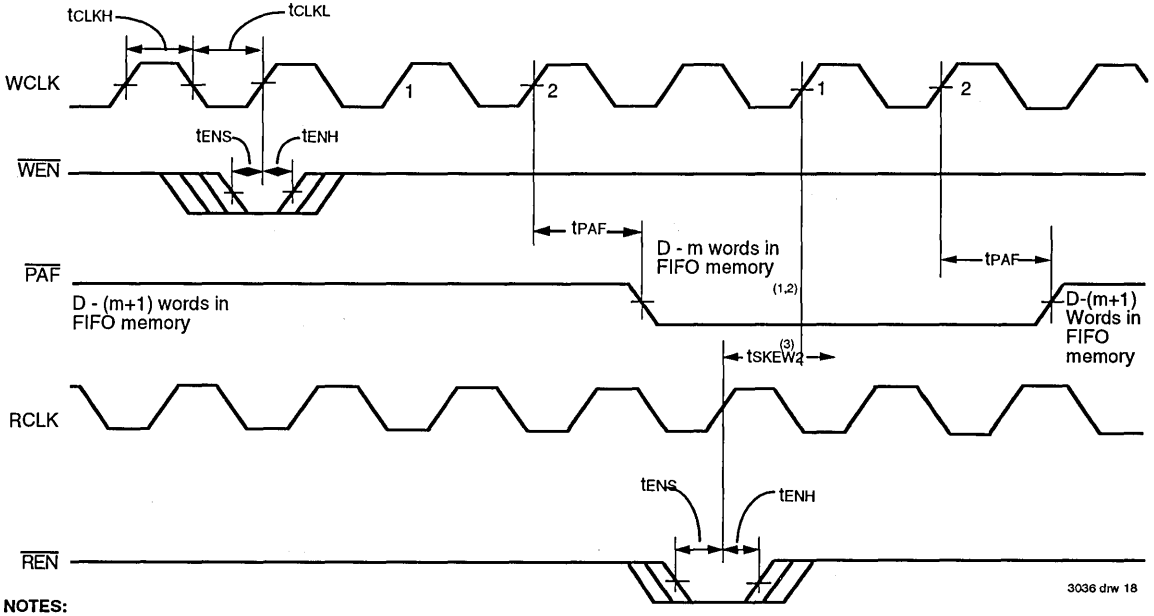
Figure 13. Parallel Read of Programmable Flag Registers (IDT Standard and FWFT modes)

NOTES:
1. $\overline{OE}$ = LOW



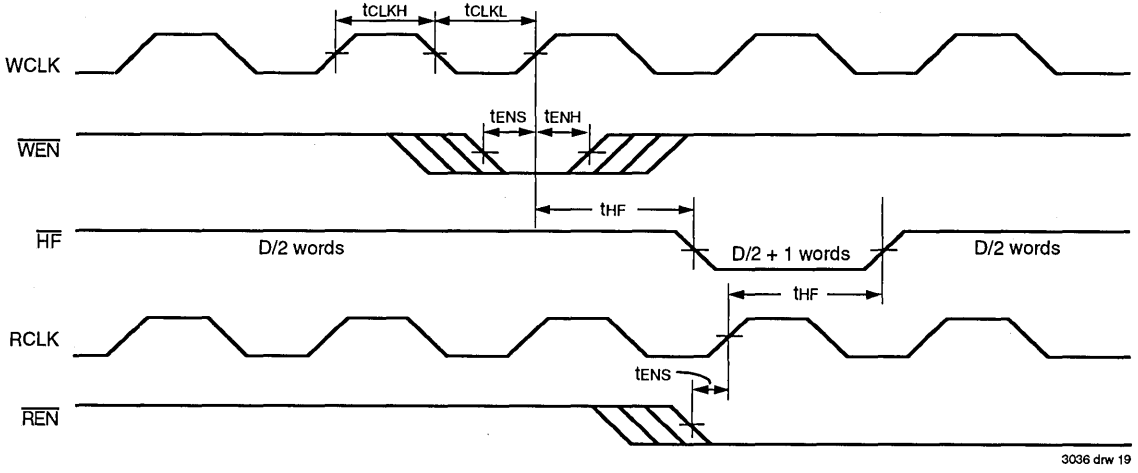
NOTES:
1. $\overline{PAE}$ offset = n
2. Data in the output register does not count as a "word in FIFO memory". Since, in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
3. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to go HIGH (after one RCLK cycle plus t_{PAE}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then the $\overline{PAE}$ deassertion may be delayed one extra RCLK cycle.

Figure 14. Programmable Almost Empty Flag Timing (IDT Standard and FWFT modes)



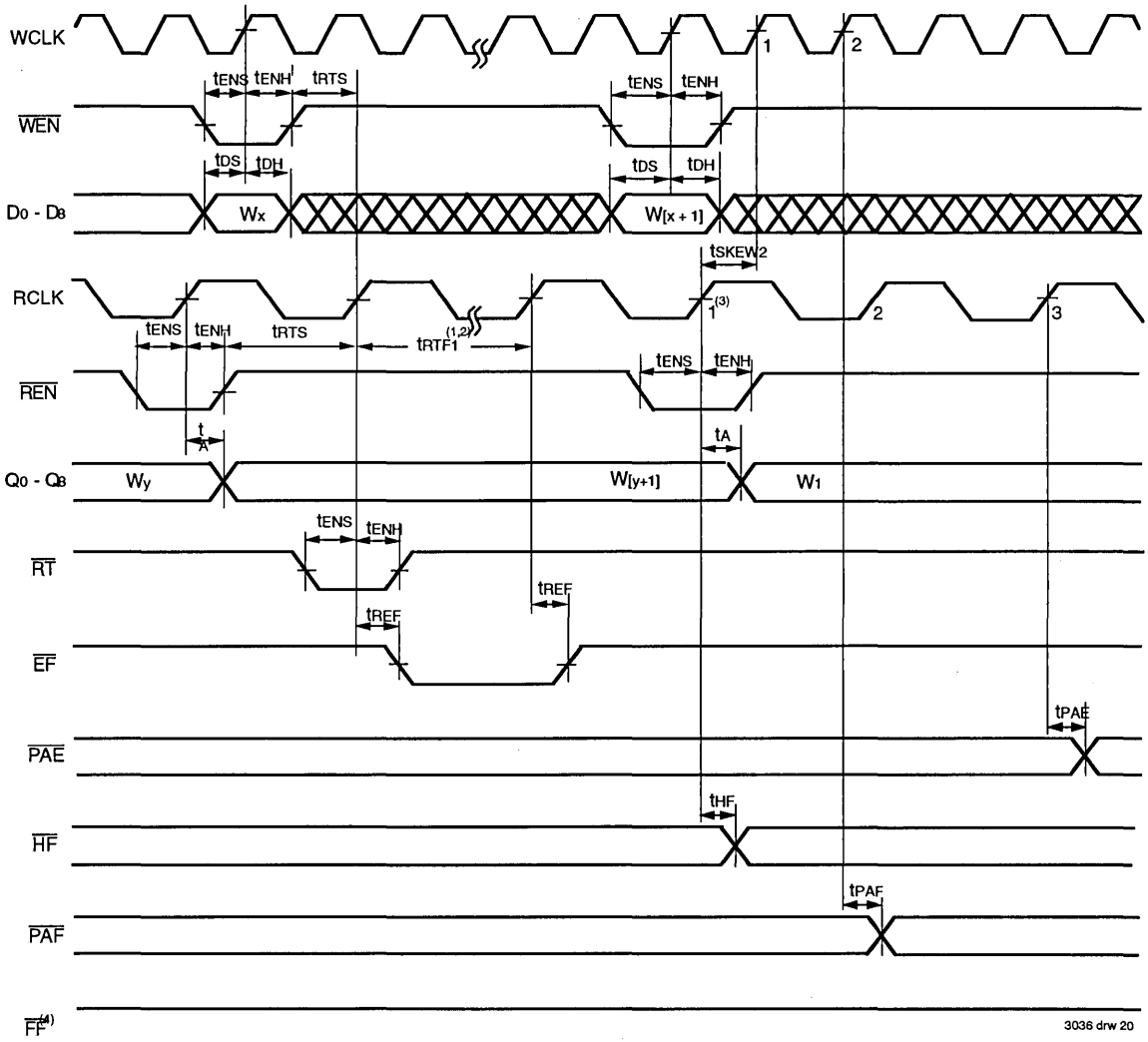
NOTES:
1. $\overline{PAF}$ offset = m, D = 16,384 for IDT72261, 32,768 words for IDT72271.
2. Data in the output register does not count as a "word in FIFO memory". Since, in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to go HIGH (after one WCLK cycle plus t_{PAF}). If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then the $\overline{PAF}$ deassertion time may be delayed an extra WCLK cycle.

Figure 15. Programmable Almost Full Flag Timing (IDT Standard and FWFT modes)



NOTES:
1. D = maximum FIFO depth = 16,384 for IDT72261, 32,768 words for IDT72271.

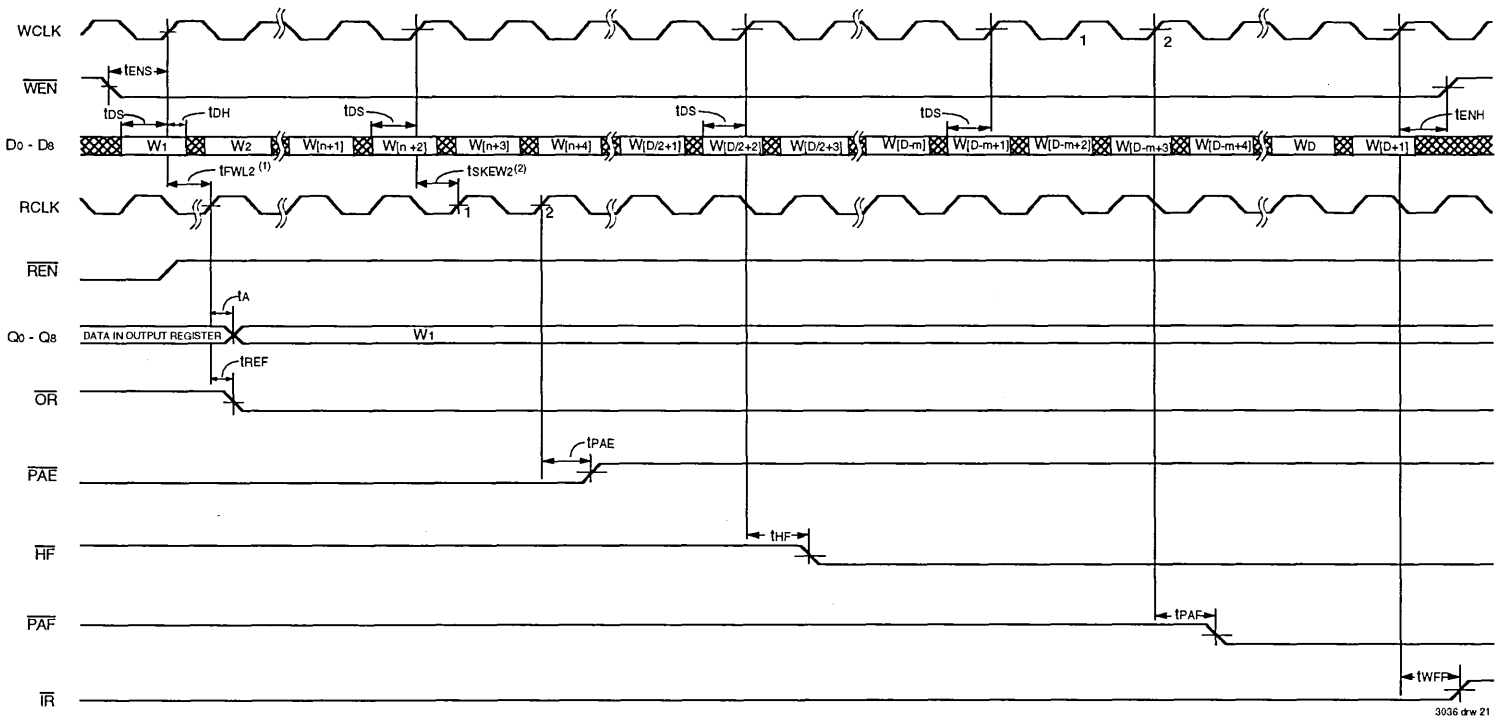
Figure 16. Half - Full Flag Timing (IDT Standard and FWFT modes)



NOTES:

1. t_{RTF1} contributes a variable delay to the overall retransmit recovery time:
   t_{RFTF1} max = 14*T_f + 3*T_{RCLK} (in ns)
   Where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period.
2. Retransmit Setup is complete after $\overline{EF}$ returns HIGH, only then can a read operation begin. Write operations are permitted after one of two conditions have been met: $\overline{EF}$ is HIGH or 14 cycles of the faster clock (RCLK or WCLK) have elapsed since the RCLK rising edge enabled by the $\overline{RT}$ pulse.
3. Following Retransmit Setup, the rising edge of RCLK that accesses the first memory location also initiates the updating of $\overline{HF}$, $\overline{PAE}$, and $\overline{PAF}$.
4. No more than D - 2 words (D = 16,384 words for the 72261, 32,768 words for the 72271) should have been written to the FIFO between Reset (Master or Partial) and Retransmit Setup. Therefore, $\overline{FF}$ will be HIGH throughout the Retransmit Setup procedure.
5. $\overline{OE}$ = LOW

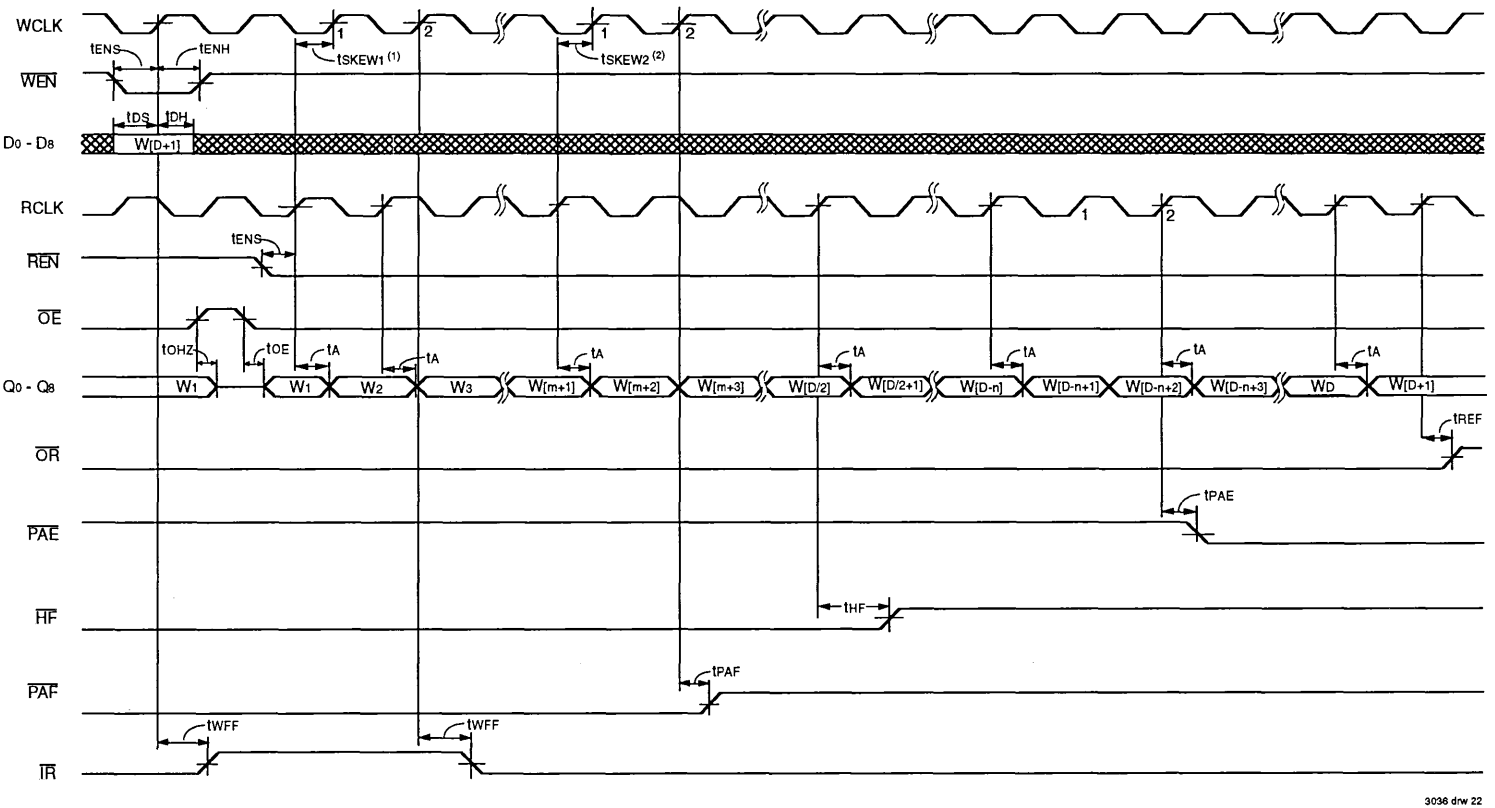
Figure 17. Retransmit Timing (IDT Standard mode)



NOTES:

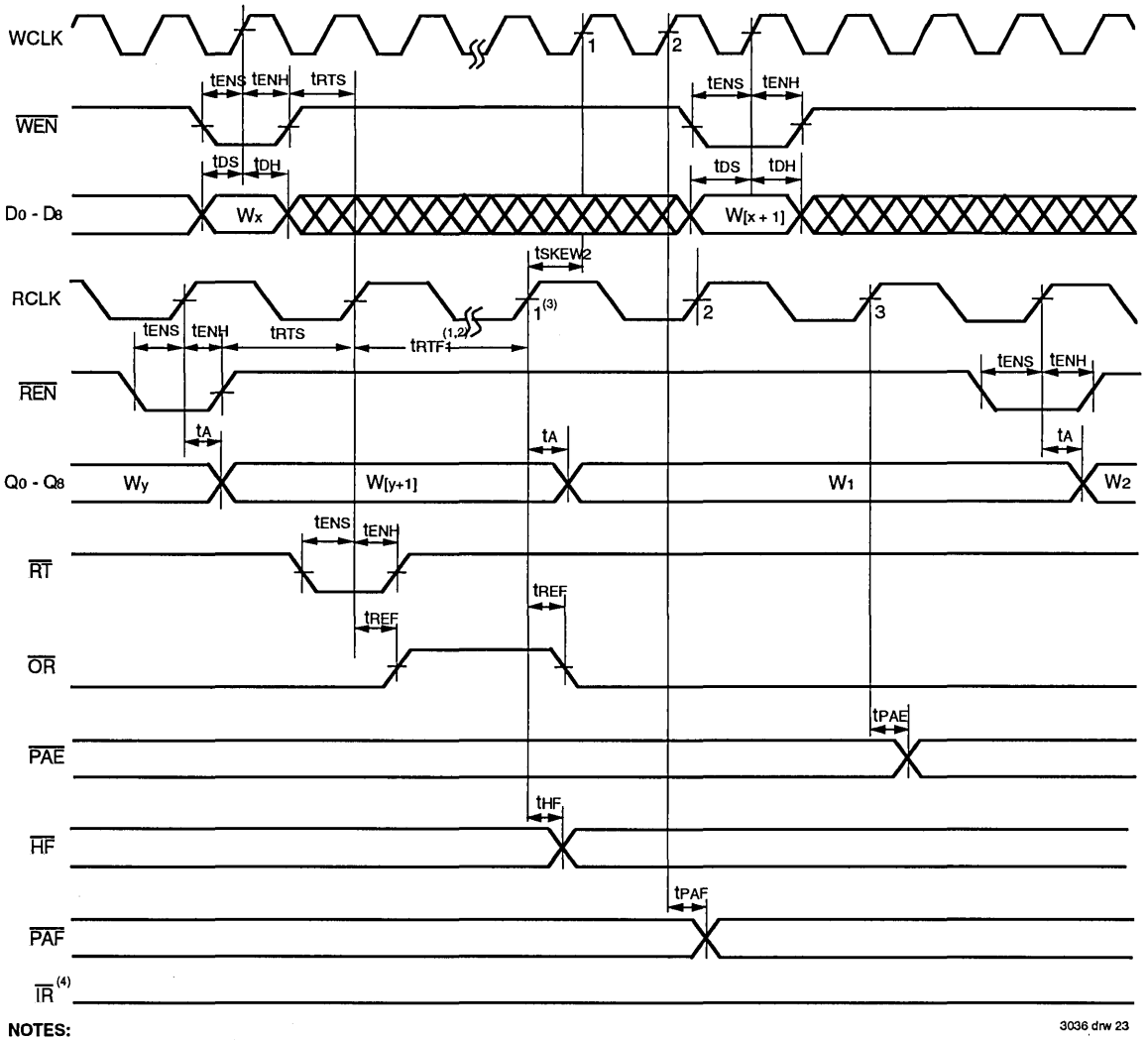
1. t_{FWL2} max. (in ns) = 10*Tf + 3*T_{RCLK}
   where Tf is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to go HIGH (after one RCLK cycle plus t_{PAE}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then the $\overline{PAE}$ deassertion may be delayed one extra RCLK cycle.
3. $\overline{LD}$ = HIGH, $\overline{OE}$ = LOW
4. $\overline{PAE}$ offset = n, $\overline{PAF}$ offset = m, D = maximum FIFO depth = 16,384 words for the IDT 72261, 32,768 words for the IDT72271

Figure 18. Write Timing (First Word Fall Through Mode)



NOTES:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{IR}$ will go LOW (after one WCLK cycle plus t_{WFF}). If the time between the rising ege of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then the $\overline{IR}$ assertion may be delayed an extra WCLK cycle.
2. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to go HIGH (after one WCLK cycle plus t_{PAF}). If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then the $\overline{PAF}$ deassertion may be delayed an extra WCLK cycle.
3. $\overline{LD}$ = HIGH
4. $\overline{PAE}$ offset = n, $\overline{PAF}$ offset = m, D = maximum FIFO depth = 16,384 words for the IDT 72261, 32,768 words for the IDT72271

Figure 19. Read Timing (First Word Fall Through Mode)



NOTES:

1. t_{RTF2} contribute a variable delay to the overall retransmit time:
   t_{RTF2} max = 14*T_f + 4*T_{RCLK} (in ns)
   Where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period.
2. Retransmit Setup is complete after $\overline{OR}$ returns LOW, only then can a read operation begin. Write operations are permitted after one of two conditions have been met: $\overline{OR}$ is LOW or 14 cycles of the faster clock (RCLK or WCLK) have elapsed since the RCLK rising edge enabled by the $\overline{RT}$ pulse.
3. Following Retransmit Setup, the rising edge of RCLK that accesses the first memory location also initiates the updating of $\overline{HF}$, $\overline{PAE}$, and $\overline{PAF}$.
4. No more than D - 2 words (D = 16,384 words for the 72261, 32,768 words for the 72271) should have been written to the FIFO between Reset (Master or Partial) and Retransmit Setup. Therefore, $\overline{IR}$ will be LOW throughout the Retransmit Setup procedure.
5. $\overline{OE}$ = LOW

Figure 20. Retransmit Timing (FWFT mode)

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

A single IDT72261/722171 may be used when the application requirements are for 16,384/32,768 words or less. The IDT72261/72271 can always be used in Single Device Configuration, whether IDT Standard Mode or FWFT Mode has been selected. No special set up procedure is necessary.

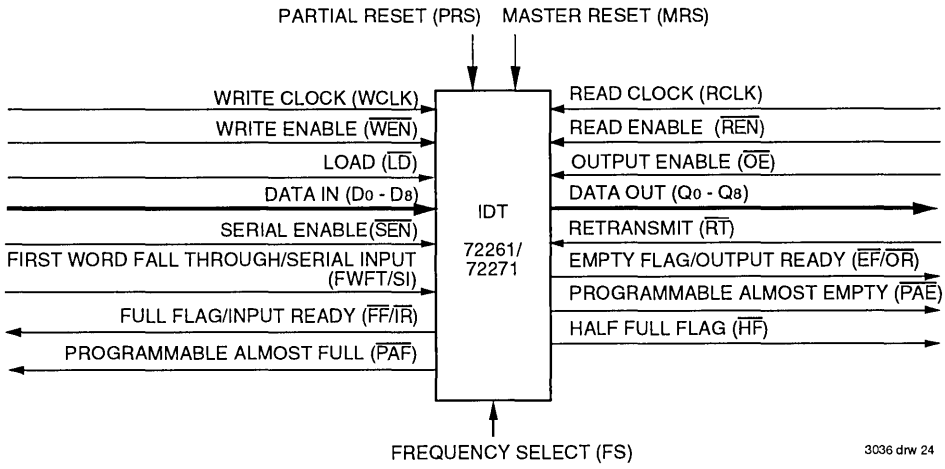
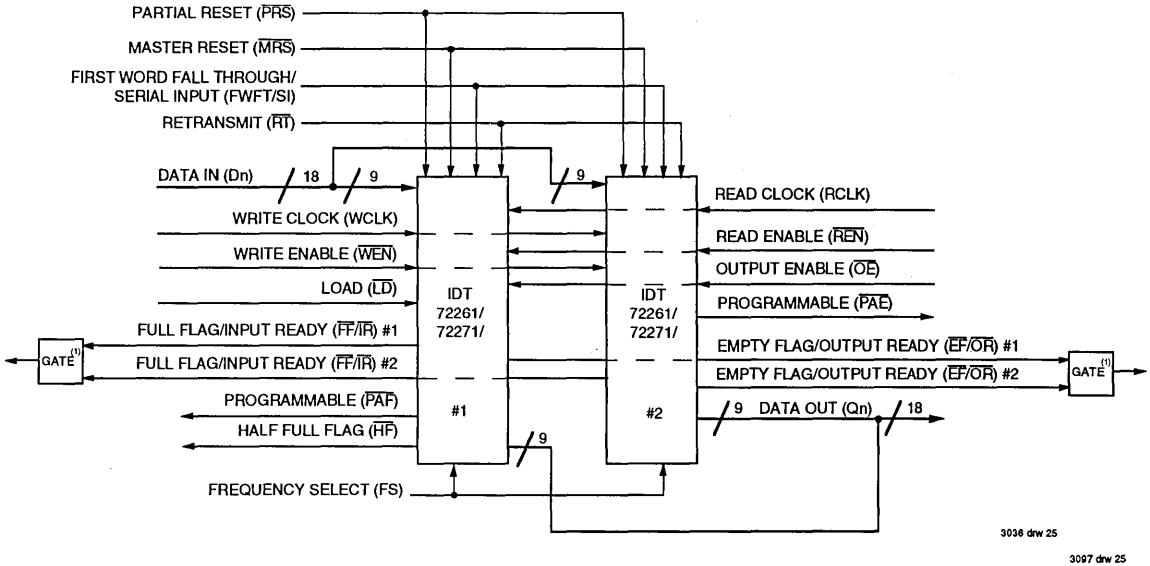


Figure 21. Block Diagram of Single 16,384x9/32,768x9 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting together the control signals of multiple devices. Status flags can be detected from any one device. The exceptions are the $\overline{EF}$ and $\overline{FF}$ functions in IDT Standard mode and the $\overline{IR}$ and $\overline{OR}$ functions in FWFT mode. Because of variations in skew between RCLK and WCLK, it is possible for $\overline{EF}$/$\overline{FF}$ deassertion and $\overline{IR}$/$\overline{OR}$ assertion to vary by one cycle between FIFOs. In IDT Standard mode, such problems can be avoided by creating composite flags, that is, ANDing $\overline{EF}$ of every FIFO, and separately ANDing $\overline{FF}$ of every FIFO. In FWFT mode, composite flags can be created by ORing $\overline{OR}$ of every FIFO, and separately ORing $\overline{IR}$ of every FIFO. Figure 22 demonstrates an 18-word width by using two IDT72261/72271s. Any word width can be attained by adding additional IDT7226172271s.



NOTE:
1. Use an AND gate in IDT Standard mode, an OR gate in FWFT mode.
2. Do not connect any output control signals directly together.

Figure 22. Block Diagram of 16,384x18/32,768x18 72261/71 Width Expansion

5

DEPTH EXPANSION CONFIGURATION

The IDT72261/72271 can easily be adapted to applications requiring more than 16,384/32,768 words of buffering. In FWFT mode, the FIFOs can be arranged in series (the data outputs of one FIFO connected to the data inputs of the next)–no external logic necessary. The resulting configuration provides a total depth equivalent to the sum of the depths associated with each single FIFO. Figure 23 shows a depth expansion using two IDT72261/72271s.

Care should be taken to select FWFT mode during Master Reset for all FIFOs in the depth expansion configuration. The first word written to an empty configuration will pass from one FIFO to the next ("ripple down") until it finally appears at the outputs of the last FIFO in the chain–no read operation is necessary. Each time the data word appears at the outputs of one FIFO, that device's $\overline{OR}$ line goes LOW, enabling a write to the next FIFO in line.

The $\overline{OR}$ assertion time is variable and is described with the help of the t_{FWL2} parameter, which includes including delay caused by clock skew:

$$t_{FWL2}\ max.= 10*T_f + 3*T_{RCLK}$$

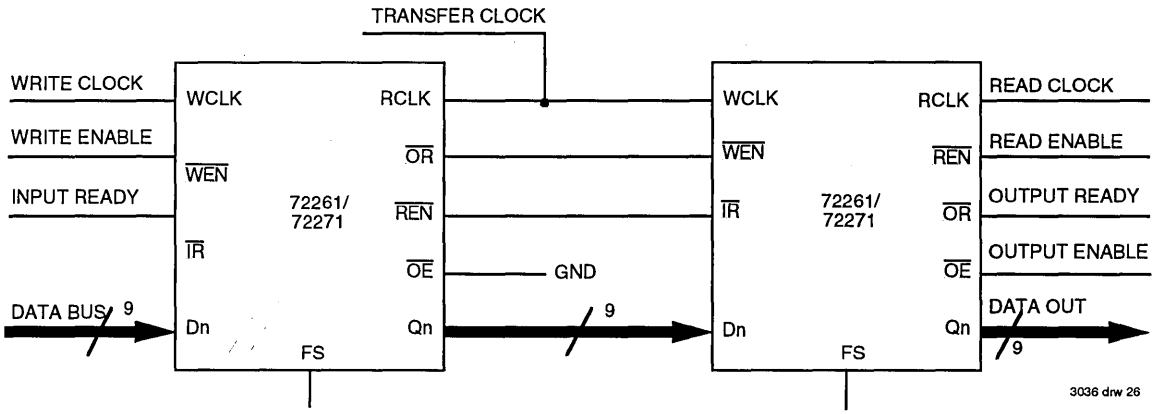


Figure 23. Block Diagram of 32,768x9/65,536x9 Synchronous FIFO Memory With Programmable Flags used in Depth Expansion Configuration

where T_{RCLK} is the RCLK period and T_f is either the RCLK or the WCLK period, whichever is shorter.

The maximum amount of time it takes for a word to pass from the inputs of the first FIFO to the outputs of the last FIFO in the chain is the sum of the delays for each individual FIFO:

$$t_{FWL2(1)} + t_{FWL2(2)} + \ldots + t_{FWL2(N)} + N^*T_{RCLK}$$

where N is the number of FIFOs in the expansion.

Note that the additional RCLK term accounts for the time it takes to pass data between FIFOs.

The ripple down delay is only noticeable for the first word written to an empty depth expansion configuration. There will be no delay evident for subsequent words written to the configuration.

The first free location created by reading from a full depth expansion configuration will "bubble up" from the last FIFO to the previous one until it finally moves into the first FIFO of the chain. Each time a free location is created in one FIFO of the chain, that FIFO's $\overline{IR}$ line goes LOW, enabling the preceding FIFO to write a word to fill it.

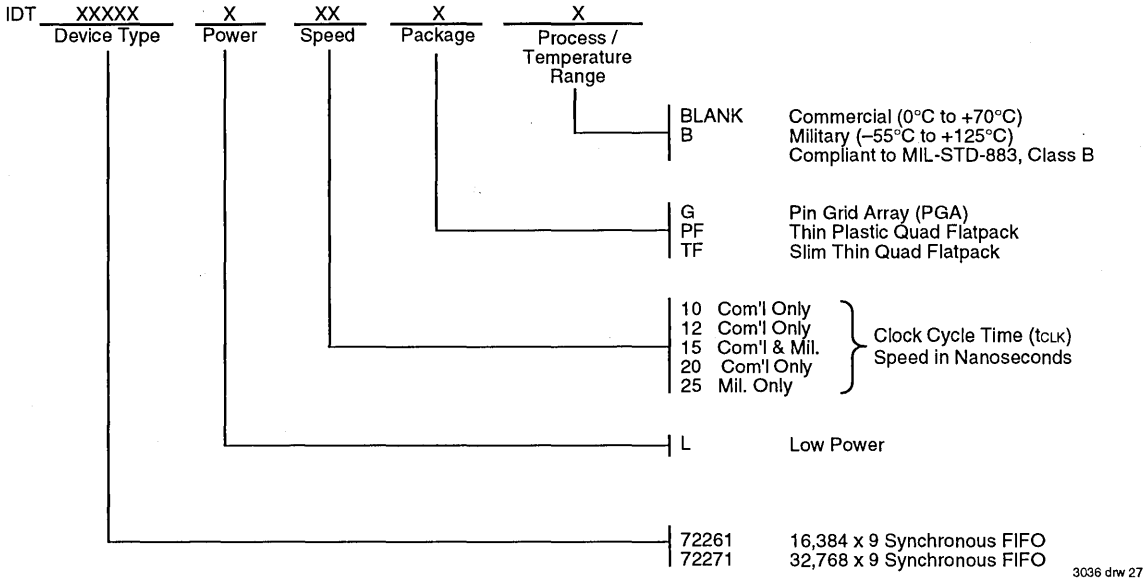
The amount of time it takes for $\overline{IR}$ of the first FIFO in the chain to assert after a word is read from the last FIFO is the sum of the delays for each individual FIFO:

$$N^*(3^*T_{WCLK})$$

where N is the number of FIFOs in the expansion and T_{WCLK} is the WCLK period. Note that one of the three WCLK cycle accounts for T_{SKEW1} delays.

In a Supersync depth expansion, set FS individually for each FIFO in the chain. The Transfer Clock line should be tied to either WCLK or RCLK, whichever is faster. Both these actions result in moving, as quickly as possible, data to the end of the chain and free locations to the beginning of the chain.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS SUPERSYNC FIFO™ 8,192 x 18, 16,384 x 18

PRELIMINARY
IDT72255
IDT72265

FEATURES:

- 8,192 x 18-bit storage capacity (IDT72255)
- 16,384 x 18-bit storage capacity (IDT72265)
- 10ns read/write cycle time (8ns access time)
- Retransmit Capability
- Auto power down reduces power consumption
- Master Reset clears entire FIFO, Partial Reset clears data, but retains programmable settings
- Empty, Full and Half-full flags signal FIFO status
- Programmable Almost Empty and Almost Full flags, each flag can default to one of two preselected offsets
- Program partial flags by either serial or parallel means
- Select IDT Standard timing (using $\overline{EF}$ and $\overline{FF}$ flags) or First Word Fall Through timing (using $\overline{OR}$ and $\overline{IR}$ flags)
- Easily expandable in depth and width
- Independent read and write clocks (permit simultaneous reading and writing with one clock signal)
- Available in the 64-pin Thin Quad Flat Pack (TQFP), 64-pin Slim Thin Quad Flat Pack (STQFP) and the 68-pin Pin Grid Array (PGA)
- Output enable puts data outputs into high impedance
- High-performance submicron CMOS technology

DESCRIPTION:

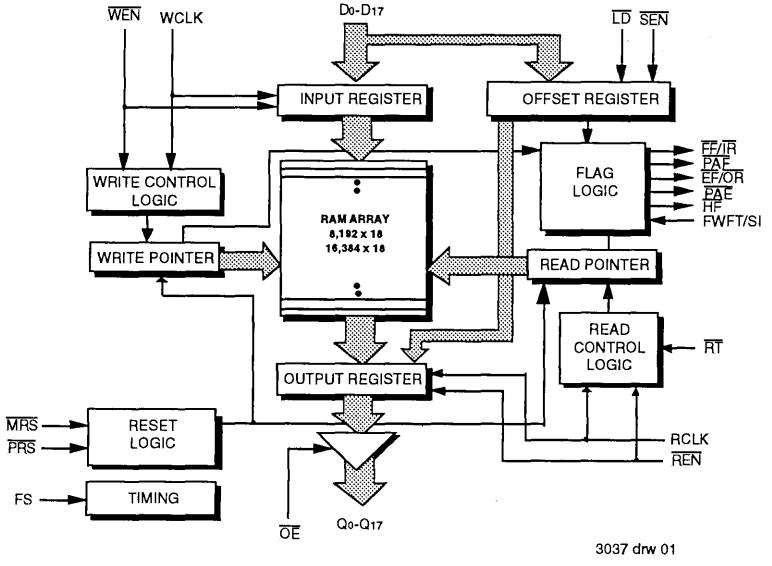
The IDT72255/72265 are monolithic, CMOS, high capacity, high speed, low power first-in, first-out (FIFO) memories with clocked read and write controls. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, local area networks (LANs), and interprocessor communication.

Both FIFOs have an 18-bit input port (Dn) and an 18-bit output port (Qn). The input port is controlled by a free-running clock (WCLK) and a data input enable pin ($\overline{WEN}$). Data is written into the synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronously for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the outputs.

The IDT72255/72265 have two modes of operation: In the *IDT Standard Mode*, the first word written to the FIFO is deposited into the memory array. A read operation is required to access that word. In the *First Word Fall Through Mode*

5

FUNCTIONAL BLOCK DIAGRAM



3037 drw 01

SyncFIFO is a trademark and the IDT logo is a registered trademark of Integrated Device Technology, Inc.

(FWFT), the first word written to an empty FIFO appears automatically on the outputs, no read operation required. The state of the FWFT/SI pin during Master Reset determines the mode in use.

The IDT72255/72265 FIFOs have five flag functions, $\overline{EF}$/$\overline{OR}$ (Empty Flag or Output Ready), $\overline{FF}$/$\overline{IR}$ (Full Flag or Input Ready), and $\overline{HF}$ (Half-full Flag). The $\overline{EF}$ and $\overline{FF}$ functions are selected in the IDT Standard Mode.

The $\overline{IR}$ and $\overline{OR}$ functions are selected in the First Word Fall Through Mode. $\overline{IR}$ indicates that the FIFO has free space to receive data. $\overline{OR}$ indicates that data contained in the FIFO is available for reading.

$\overline{HF}$ is a flag whose threshold is fixed at the half-way point in memory. This flag can always be used irrespective of mode.

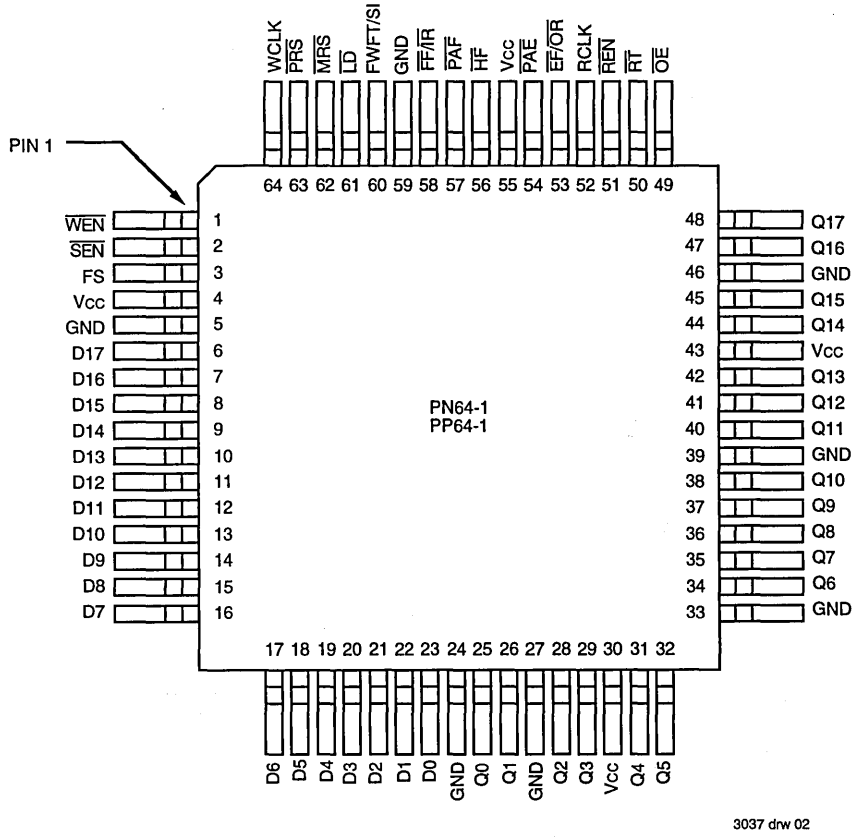
$\overline{PAE}$, $\overline{PAF}$ can be programmed independantly to any point in memory. They, also, can be used irrespective of mode. Programmable offsets determine the flag threshold and can be loaded by two methods: parallel or serial. Two default offset settings are also provided, such that $\overline{PAE}$ can be set at 127 or 1023 locations from the empty boundary and the $\overline{PAF}$ threshold can be set at 127 or 1023 locations from the full boundary. All these choices are made with $\overline{LD}$ during Master Reset.

In the serial method, $\overline{SEN}$ together with $\overline{LD}$ are used to load the offset registers via the Serial Input (SI). In the parallel method, $\overline{WEN}$ together with $\overline{LD}$ can be used to load the offset registers via D_n. $\overline{REN}$ together with $\overline{LD}$ can be used to read the offsets in parallel from Q_n regardless of whether serial or parallel offset loading is selected.

During Master Reset ($\overline{MRS}$), the read and write pointers are set to the first location of the FIFO. The FWFT line selects IDT Standard Mode or FWFT Mode. The $\overline{LD}$ pin selects one of two partial flag default settings (127 or 1023) and, also, serial or parallel programming. The flags are updated accordingly.

The Partial Reset ($\overline{PRS}$) also sets the read and write pointers to the first location of the memory. However, the mode setting, programming method, and partial flag offsets are not altered. The flags are updated accordingly. $\overline{PRS}$ is

PIN CONFIGURATIONS



3037 drw 02

TQFP
STQFP
TOP VIEW

useful for resetting a device in mid-operation, when reprogramming offset registers may not be convenient.

The Retransmit function allows the read pointer to be reset to the first location in the RAM array. It is synchronized to RCLK when $\overline{RT}$ is LOW. This feature is convenient for sending the same data more than once.

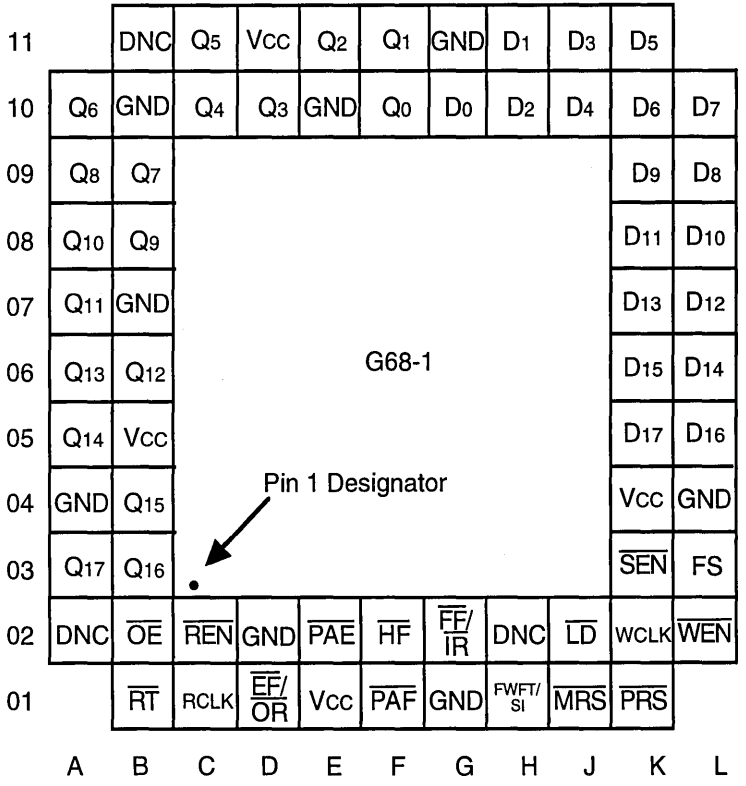
If, at any time, the FIFO is not actively performing a function, the chip will automatically power down. This occurs if neither a read nor a write occurs within 10 cycles of the faster clock, RCLK or WCLK. During the Power Down state, supply current consumption (I_{CC2}) is at a minimum. Initiating any operation (by activating control inputs) will immediately take the device out of the Power Down state.

The IDT72255/72265 are depth expandable. The addition of external components is unnecessary. The $\overline{IR}$ and $\overline{OR}$ functions, together with $\overline{REN}$ and $\overline{WEN}$, are used to extend the total FIFO memory capacity.

The FS line ensures optimal data flow through the FIFO. It is tied to GND if the RCLK frequency is higher than the WCLK frequency or to Vcc if the RCLK frequency is lower than the WCLK frequency

The IDT72255/72265 is fabricated using IDT's high speed submicron CMOS technology.

PIN CONFIGURATIONS (CONT.)



3037 drw 03

PGA
TOP VIEW

NOTES:
1. DNC = Do not connect

PIN DESCRIPTION

Symbol	Name	I/O	Description
D_0–D_{17}	Data Inputs	I	Data inputs for a 18-bit bus.
$\overline{MRS}$	Master Reset	I	$\overline{MRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Master Reset, the FIFO is configured for either FWFT or IDT Standard Mode, one of two programmable flag default settings, and serial or parallel programming of the offset settings.
$\overline{PRS}$	Partial Reset	I	$\overline{PRS}$ initializes the read and write pointers to zero and sets the output register to all zeroes. During Partial Reset,the existing mode (IDT or FWFT), programming method (serial or parallel), and programmable flag settings are all retained.
$\overline{RT}$	Retransmit	I	Allows data to be resent starting with the first location of FIFO memory.
FWFT/SI	First Word Fall Through/Serial In	I	During Master Reset, selects First Word Fall Through or IDT Standard mode. After Master Reset, this pin functions as a serial input for loading offset registers
WCLK	Write Clock	I	When enabled by $\overline{WEN}$, the rising edge of WCLK writes data into the FIFO and offsets into the programmable registers.
$\overline{WEN}$	Write Enable	I	$\overline{WEN}$ enables WCLK for writing data into the FIFO memory and offset registers.
RCLK	Read Clock	I	When enabled by $\overline{REN}$, the rising edge of RCLK reads data from the FIFO memory and offsets from the programmable registers.
$\overline{REN}$	Read Enable	I	$\overline{REN}$ enables RCLK for reading data from the FIFO memory and offset registers.
$\overline{OE}$	Output Enable	I	$\overline{OE}$ controls the output impedance of Q_n
$\overline{SEN}$	Serial Enable	I	$\overline{SEN}$ enables serial loading of programmable flag offsets
$\overline{LD}$	Load	I	During Master Reset, $\overline{LD}$ selects one of two partial flag default offsets (127 and 1023) and determines programming method, serial or parallel. After Master Reset, this pin enables writing to and reading from the offset registers.
FS	Frequency Select	I	The FS setting optimizes data flow through the FIFO.
$\overline{FF}/\overline{IR}$	Full Flag/ Input Ready	O	In the IDT Standard Mode, the $\overline{FF}$ function is selected. $\overline{FF}$ indicates whether or not the FIFO memory is full. In the FWFT mode, the $\overline{IR}$ function is selected. $\overline{IR}$ indicates whether or not there is space available for writing to the FIFO memory.
$\overline{EF}/\overline{OR}$	Empty Flag/ Output Ready	O	In the IDT Standard Mode, the $\overline{EF}$ function is selected. $\overline{EF}$ indicates whether or not the FIFO memory is empty. In FWFT mode, the $\overline{OR}$ function is selected. $\overline{OR}$ indicates whether or not there is valid data available at the outputs.
$\overline{PAF}$	Programmable Almost Full Flag	O	$\overline{PAF}$ goes HIGH if the number of free locations in the FIFO memory is more than offset m which is store in Almost Full which is stored in the Full Offset register. $\overline{PAF}$ goes LOW if the number of free locations in the FIFO memory is less than m.
$\overline{PAE}$	Programmable Almost Empty Flag	O	$\overline{PAE}$ goes LOW if the number of words in the FIFO memory is less than offset n which is stored in theEmpty Offset register. $\overline{PAE}$ goes HIGH if the number of words in the FIFO memory is greater than offset n.
$\overline{HF}$	Half-full Flag	O	$\overline{HF}$ indicates whether the FIFO memory is more or less than half-full.
Q_0–Q_{17}	Data Outputs	O	Data outputs for a 18-bit bus.
Vcc	Power		+5 volt power supply pins.
GND	Ground		Ground pins.

3037 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Mlilitary	Unit
VTERM	Terminal Voltage with respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
IOUT	DC Output Current	50	50	mA

NOTE: 3037 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maimum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIH	Input High Voltage Military	2.2	—	—	V
VIL(1)	Input Low Voltage Commercial & Military	—	—	0.8	V

NOTE: 3037 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Military: VCC = 5V ± 10%, TA = –55°C to +125°C)

Symbol	Parameter	DT72255L IDT72265L Commercial tCLK = 10, 12,15, 20ns			IDT72255L IDT72265L Military tCLK = 15, 25ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
ILI(1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
ILO(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = –2 mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8 mA	—	—	0.4	—	—	0.4	V
ICC1(3)	Active Power Supply Current	—	—	180	—	—	250	mA
ICC2(3,4)	Power Down Current (All inputs = VCC - 0.2V or GND + 0.2V, RCLK and WCLK are free-running)	—	—	15	—	—	25	mA

NOTES: 3037 tbl 04

1. Measurements with 0.4 ≤ VIN ≤ VCC.
2. $\overline{OE}$ = VIH
3. Tested at f = 20 MHz with outputs unloaded.
4. No data written or read for more than 10 cycles

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN(2)	Input Capacitance	VIN = 0V	10	pF
COUT(1,2)	Output Capacitance	VOUT = 0V	10	pF

NOTES: 3037 tbl 05

1. With output deselected, ($\overline{OE}$=HIGH).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Commercial				Com'l & Mil.		Commercial		Military		
		72255L10 72265L10		72255L12 72265L12		72255L15 72265L15		72255L20 72265L20		72255L25 72265L25		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Clock Cycle Frequency	—	100	—	83.3	—	66.7	—	50	—	40	MHz
tA	Data Access Time	2	8	2	9	2	10	2	12	3	15	ns
tCLK	Clock Cycle Time	10	—	12	—	15	—	20	—	25	—	ns
tCLKH	Clock High Time	4.5	—	5	—	6	—	8	—	10	—	ns
tCLKL	Clock Low Time	4.5[2]	—	5[2]	—	6[2]	—	8	—	10	—	ns
tDS	Data Set-up Time	3.5	—	3.5	—	4	—	5	—	6	—	ns
tDH	Data Hold Time	0	—	0	—	1	—	1	—	1	—	ns
tENS	Enable Set-up Time	3.5	—	3.5	—	4	—	5	—	6	—	ns
tENH	Enable Hold Time	0	—	0	—	1	—	1	—	1	—	ns
tLDS	Load Set-up Time	3.5	—	3.5	—	4	—	5	—	6	—	ns
tLDH	Load Hold Time	6.5	—	8.5	—	10	—	10	—	10	—	ns
tRS	Reset Pulse Width[3]	10	—	12	—	15	—	20	—	25	—	ns
tRSS	Reset Set-up Time	10	—	12	—	15	—	20	—	25	—	ns
tRSR	Reset Recovery Time	10	—	12	—	15	—	20	—	25	—	ns
tRSF	Reset to Flag and Output Time	—	10	—	12	—	15	—	20	—	25	ns
tFWFT	Mode Select Time	0	—	0	—	0	—	0	—	0	—	ns
tRTS	Retransmit Set-Up Time	3.5	—	3.5	—	4	—	5	—	6	—	ns
tOLZ	Output Enable to Output in Low Z[4]	0	—	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	7	3	7.5	3	8	3	10	3	13	ns
tOHZ	Output Enable to Output in High Z[4]	3	7	3	7.5	3	8	3	10	3	13	ns
tWFF	Write Clock to $\overline{FF}$ or $\overline{IR}$	—	8	—	9	—	10	—	12	—	15	ns
tREF	Read Clock to $\overline{EF}$ or $\overline{OR}$	—	8	—	9	—	10	—	12	—	15	ns
tPAF	Write Clock to $\overline{PAF}$	–	8	—	9	—	10	—	12	—	15	ns
tPAE	Read Clock to $\overline{PAE}$	—	8	—	9	—	10	—	12	—	15	ns
tHF	Clock to $\overline{HF}$	—	16	—	18	—	20	—	22	—	25	ns
tSKEW1	Skew time between RCLK and WCLK for $\overline{FF}$ and $\overline{IR}$	8	—	10	—	12	—	15	—	20	—	ns
tSKEW2	Skew time between RCLK and WCLK for $\overline{PAE}$ and $\overline{PAF}$	15	—	18	—	21	—	25	—	35	—	ns

3037 tbl 06

NOTES:

1. All AC timings apply to both Standard IDT Mode and First Word Fall Through Mode.
2. For the RCLK line: t_{CLKL} (min.) = 7 ns only when reading the offsets from the programmable flag registers; otherwise, use the table value. For the WCLK line, use the t_{CLKL} (min.) value given in the table.
3. Pulse widths less than minimum values are not allowed.
4. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

3037 tbl 08

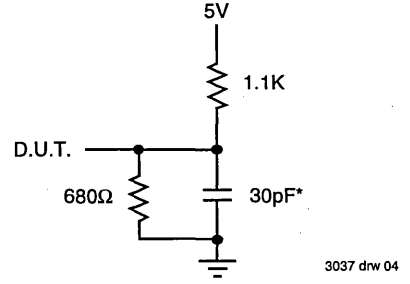


Figure 1. Output Load
* Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0 - D_{17})
Data inputs for 18-bit wide data.

CONTROLS:

MASTER RESET ($\overline{MRS}$)
A Master Reset is accomplished whenever the Master Reset ($\overline{MRS}$) input is taken to a LOW state. This operation sets the internal read and write pointers to the first location of the RAM array. $\overline{PAE}$ will go LOW, $\overline{PAF}$ will go HIGH, and $\overline{HF}$ will go HIGH.

If FWFT is LOW during Master Reset then the IDT Standard Mode, along with $\overline{EF}$ and $\overline{FF}$ are selected. $\overline{EF}$ will go LOW and $\overline{FF}$ will go HIGH. If FWFT is HIGH, then the First Word Fall through Mode (FWFT), along with $\overline{IR}$ and $\overline{OR}$, are selected. $\overline{OR}$ will go HIGH and $\overline{IR}$ will go LOW.

If $\overline{LD}$ is LOW during Master Reset, then $\overline{PAE}$ is assigned a threshold 127 words from the empty boundary and $\overline{PAF}$ is assigned a threshold 127 words from the full boundary; 127 words corresponds to an offset value of 07FH. Following Master Reset, parallel loading of the offsets is permitted, but not serial loading.

If $\overline{LD}$ is HIGH during Master Reset, then $\overline{PAE}$ is assigned a threshold 1023 words from the empty boundary and $\overline{PAF}$ is assigned a threshold 1023 words from the full boundary; 1023 words corresponds to an offset value of 3FFH. Following Master Reset, serial loading of the offsets is permitted, but not parallel loading.

Regardless of whether serial or parallel offset loading has been selected, parallel reading of the registers is always permitted. (See section describing the $\overline{LD}$ line for further details).

During a Master Reset, the output register is initialized to all zeroes. A Master Reset is required after power up, before a write operation can take place. $\overline{MRS}$ is asynchronous.

PARTIAL RESET ($\overline{PRS}$)
A Partial Reset is accomplished whenever the Partial Reset ($\overline{PRS}$) input is taken to a LOW state. As in the case of the Master Reset, the internal read and write pointers are set to the first location of the RAM array, $\overline{PAE}$ goes LOW, $\overline{PAF}$ goes HIGH, and $\overline{HF}$ goes HIGH.

Whichever mode is active at the time of partial reset, IDT Standard Mode or First Word Fall-through, that mode will remain selected. If the IDT Standard Mode is active, then $\overline{FF}$ will go HIGH and $\overline{EF}$ will go LOW. If the First word Fall-through Mode is active, then $\overline{OR}$ will go HIGH, and $\overline{IR}$ will go LOW.

Following Partial Reset, all values held in the offset registers remain unchanged. The programming method (parallel or serial) currently active at the time of Partial Reset is also retained. The output register is initialized to all zeroes. $\overline{PRS}$ is asynchronous.

A Partial Reset is useful for resetting the device during the course of operation, when reprogramming flag settings may not be convenient.

RETRANSMIT ($\overline{RT}$)
The Retransmit operation allows data that has already been read to be accessed again. There are two stages: first, a setup procedure that resets the read pointer to the first location of memory, then the actual retransmit, which consists of reading out the memory contents, starting at the beginning of memory.

Retransmit Setup is initiated by holding $\overline{RT}$ LOW during a rising RCLK edge. $\overline{REN}$ and $\overline{WEN}$ must be HIGH before bringing $\overline{RT}$ LOW. At least one word, but no more than Full - 2 words should have been written into the FIFO between Reset (Master or Partial) and the time of Retransmit Setup (Full = 8,192 words for the 72255, 16,384 words for the 72265).

If IDT Standard mode is selected, the FIFO will mark the beginning of the Retransmit Setup by setting $\overline{EF}$ LOW. The change in level will only be noticeable if $\overline{EF}$ was HIGH before setup. During this period, the internal read pointer is initialized to the first location of the RAM array.

When $\overline{EF}$ goes HIGH, Retransmit Setup is complete and read operations may begin starting with the first location in memory. Since IDT Standard Mode is selected, every word read including the first word following Retransmit Setup requires a LOW on $\overline{REN}$ to enable the rising edge of RCLK. Writing operations can begin after one of two conditions have been met: $\overline{EF}$ is HIGH or 14 cycles of the faster clock (RCLK or WCLK) have elapsed since the RCLK rising edge enabled by the $\overline{RT}$ pulse.

The deassertion time of $\overline{EF}$ during Retransmit Setup is variable. The parameter t_{RTF1}, which is measured from the rising RCLK edge enabled by $\overline{RT}$ to the rising edge of $\overline{EF}$ is described by the following equation:

$$t_{RTF1} \text{ max.} = 14*T_f + 3*T_{RCLK} \text{ (in ns)}$$

where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period.

Regarding $\overline{FF}$: Note that since no more than Full - 2 writes are allowed between a Reset and a Retransmit Setup, $\overline{FF}$ will remain HIGH throughout the setup procedure.

For IDT Standard mode, updating the $\overline{PAE}$, $\overline{HF}$, and $\overline{PAF}$ flags begins with the "first" $\overline{REN}$-enabled rising RCLK edge following the end of Retransmit Setup (the point at which $\overline{EF}$ goes HIGH). This same RCLK rising edge is used to access the "first" memory location. $\overline{HF}$ is updated on the first RCLK rising edge. $\overline{PAE}$ is updated after two more rising RCLK edges. $\overline{PAF}$ is updated after the "first" rising RCLK edge, followed by the next two rising WCLK edges. (If the t_{skew2} specification is not met, add one more WCLK cycle.)

If FWFT mode is selected, the FIFO will mark the beginning of the Retransmit Setup by setting $\overline{OR}$ HIGH. The change in level will only be noticeable if $\overline{OR}$ was LOW before setup. During this period, the internal read pointer is set to the first location of the RAM array.

5

When $\overline{OR}$ goes LOW, Retransmit Setup is complete; at the same time, the contents of the first location are automatically displayed on the outputs. Since FWFT Mode is selected, the first word appears on the outputs, no read request necessary. Reading all subsequent words requires a LOW on $\overline{REN}$ to enable the rising edge of RCLK. Writing operations can begin after one of two conditions have been met: $\overline{OR}$ is LOW or 14 cycles of the faster clock (RCLK or WCLK) have elapsed since the RCLK rising edge enabled by the $\overline{RT}$ pulse.

The assertion time of $\overline{OR}$ during Retransmit Setup is variable. The parameter t_{RTF2}, which is measured from the rising RCLK edge enabled by $\overline{RT}$ to the falling edge of $\overline{OR}$ is described by the following equation:

$$t_{RTF2}\ \text{max.} = 14*T_f + 4*T_{RCLK}\ \text{(in ns)}$$

where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period. Note that a Retransmit Setup in FWFT mode requires one more RCLK cycle than in IDT Standard mode.

Regarding $\overline{IR}$: Note that since no more than Full - 2 writes are allowed between a Reset and a Retransmit Setup, $\overline{IR}$ will remain LOW throughout the setup procedure.

For FWFT mode, updating the $\overline{PAE}$, $\overline{HF}$, and $\overline{PAF}$ flags begins with the "last" rising edge of RCLK before the end of Retransmit Setup. This is the same edge that asserts $\overline{OR}$ and automatically accesses the first memory location. Note that, in this case, $\overline{REN}$ is not required to initiate flag updating. $\overline{HF}$ is updated on the "last" RCLK rising edge. $\overline{PAE}$ is updated after two more rising RCLK edges. $\overline{PAF}$ is updated after the "last" rising RCLK edge, followed by the next two rising WCLK edges. (If the t_{skew2} specification is not met, add one more WCLK cycle.)

$\overline{RT}$ is synchronized to RCLK. The Retransmit operation is useful in the event of a transmission error on a network, since it allows a data packet to be resent.

FIRST WORD FALL THROUGH/SERIAL IN (FWFT/SI)

This is a dual purpose pin. During Master Reset, the state of the FWFT/SI helps determine whether the device will operate in IDT Standard mode or First Word Fall Through (FWFT) mode.

If, at the time of Master Reset, FWFT/SI is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag ($\overline{EF}$) to indicate whether or not there are any words present in the FIFO memory. It also uses the Full Flag function ($\overline{FF}$) to indicate whether or not the FIFO memory has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable ($\overline{REN}$) line.

If, at the time of Master Reset, FWFT/SI is HIGH, then FWFT mode will be selected. This mode uses Output Ready ($\overline{OR}$) to indicate whether or not there is valid data at the data outputs (Q_n). It also uses Input Ready ($\overline{IR}$) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Q_n, no read request necessary. Subsequent words must be accessed using the Read Enable ($\overline{REN}$) line.

After Master Reset, FWFT/SI acts as a serial input for loading $\overline{PAE}$ and $\overline{PAF}$ offsets into the programmable registers. The serial input function can only be used when the serial loading method has been selected during Master Reset. FWFT/SI functions the same way in both IDT Standard and FWFT modes.

WRITE CLOCK (WCLK)

A write cycle is initiated on the rising edge of the write clock (WCLK). Data set-up and hold times must be met with respect to the LOW-to-HIGH transition of the WCLK. The write and read clocks can either be asynchronous or coincident.

WRITE ENABLE ($\overline{WEN}$)

When Write Enable ($\overline{WEN}$) is LOW, data can be loaded into the input register on the rising edge of every WCLK cycle. Data is stored in the RAM array sequentially and independently of any on-going read operation.

When $\overline{WEN}$ is HIGH, the input register holds the previous data and no new data is loaded into the FIFO.

To prevent data overflow in the IDT Standard Mode, $\overline{FF}$ will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{FF}$ will go HIGH allowing a write to occur. $\overline{WEN}$ is ignored when the FIFO is full.

To prevent data overflow in the FWFT mode, $\overline{IR}$ will go HIGH, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{IR}$ will go LOW allowing a write to occur. $\overline{WEN}$ is ignored when the FIFO is full.

READ CLOCK (RCLK)

Data can be read on the outputs, on the rising edge of the read clock (RCLK), when Output Enable ($\overline{OE}$) is set LOW. The write and read clocks can be asynchronous or coincident.

READ ENABLE ($\overline{REN}$)

When Read Enable ($\overline{REN}$) is LOW, data is loaded from the RAM array into the output register on the rising edge of the RCLK.

When $\overline{REN}$ is HIGH, the output register holds the previous data and no new data is loaded into the output register.

In the IDT Standard Mode, every word accessed at Q_n, including the first word written to an empty FIFO, must be requested using $\overline{REN}$. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty. Once a write is performed, $\overline{EF}$ will go HIGH after $t_{FWL1} + t_{REF}$ and a read is permitted.

In the FWFT Mode, the first word written to an empty FIFO automatically goes to the outputs Q_n, no need for any read request. In order to access all other words, a read must be executed using $\overline{REN}$. When all the data has been read from the FIFO, Output Ready ($\overline{OR}$) will go HIGH, inhibiting further read operations. $\overline{REN}$ is ignored when the FIFO is empty. Once a write is performed, $\overline{OR}$ will go LOW after $t_{FWL2} + t_{REF}$, when the first word appears at Q_n; if a second word is written into the FIFO, then $\overline{REN}$ can be used to read it out.

when the first word appears at Q_n; if a second word is written into the FIFO, then $\overline{REN}$ can be used to read it out.

SERIAL ENABLE ($\overline{SEN}$)

Serial Enable is ($\overline{SEN}$) is an enable used only for serial programming of the offset registers. The serial programming method must be selected during Master Reset. $\overline{SEN}$ is always used in conjunction with $\overline{LD}$. When these lines are both LOW, data at the SI input can be loaded into the input register one bit for each LOW-to-HIGH transition of WCLK.

When $\overline{SEN}$ is HIGH, the programmable registers retains the previous settings and no offsets are loaded.

$\overline{SEN}$ functions the same way in both IDT Standard and FWFT modes.

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable ($\overline{OE}$) is enabled (LOW), the parallel output buffers receive data from the output register. When $\overline{OE}$ is HIGH, the output data bus (Q_n) goes into a high impedance state.

LOAD ($\overline{LD}$)

This is a dual purpose pin. During Master Reset, the state of the Load line ($\overline{LD}$) determines one of two default values (127 or 1023) for the $\overline{PAE}$ and $\overline{PAF}$ flags, along with the method by which these flags can be programmed, parallel or serial. After Master Reset, $\overline{LD}$ enables write operations to and read operations from the registers. Only the offset loading method currently selected can be used to write to the registers. Aside from Master Reset, there is no other way change the loading method. Registers can be read only in parallel; this can be accomplished regardless of whether serial or the parallel loading has been selected.

Associated with each of the programmable flags, $\overline{PAE}$ and $\overline{PAF}$, is one register which can either be written to or read from. Offset values contained in these registers determine how many words need to be in the FIFO memory to switch a partial flag. A LOW on $\overline{LD}$ during Master Reset selects a default $\overline{PAE}$ offset value of 07FH (a threshold 127 words from the empty boundary), a default $\overline{PAF}$ offset value of 07FH (a threshold 127 words from the full boundary), and parallel loading of other offset values. A HIGH on $\overline{LD}$ during Master Reset selects a default $\overline{PAE}$ offset value of 3FFH (a threshold 1023 words from the empty boundary), a default $\overline{PAF}$ offset value of 3FFH (a threshold 1023 words form the full boundary), and serial loading of other offset values.

5

$\overline{LD}$	$\overline{WEN}$	$\overline{REN}$	$\overline{SEN}$	WCLK	RCLK	Selection
0	0	1	1	↑	X	Parallel write to registers: Empty Offset Full Offset
0	1	0	1	X	↑	Parallel read from registers: Empty Offset Full Offset
0	1	1	0	↑	X	Serial shift into registers: 26 bits for the 72255 28 bits for the 72265 1 bit for each rising WCLK edge Starting with Empty Offset (LSB) Ending with Full Offset (MSB)
0	1	1	1	X	X	No Operation
1	0	X	X	↑	X	Write Memory
1	X	0	X	X	↑	Read Memory
1	1	1	X	X	X	No Operation

3037 tbl 02

NOTES:
1. Only one of the two offset programming methods, serial or parallel, is available for use at any given time.
2. The programming method can only be selected at Master Reset.
3. Parallel reading of the offset registers is always permitted regardless of which programming method has been selected.
4. The programming sequence applies to both IDT Standard and FWFT modes.

Figure 2. Partial Flag Programming Sequence

two pointers operate independently; however, a read and a write should not be performed simultaneously to the offset registers. A Master Reset initializes both pointers to the Empty Offset (LSB) register. A Partial Reset has no effect on the position of these pointers.

Once serial offset loading has been selected, then programming $\overline{PAE}$ and $\overline{PAF}$ procedes as follows: When $\overline{LD}$ and $\overline{SEN}$ are set LOW, data on the SI input are written, one bit for each WCLK rising edge, starting with the Empty Offset (13 bits for the 72255, 14 bits for the 72265), ending with the Full Offset (13 bits for the 72255, 14 bits for the 72265). A total of 26 bits are necessary to program the 72255; a total of 28 bits are necessary to program the 72265. Individual registers cannot be loaded serially; rather, both must be programmed in sequence, no padding allowed. $\overline{PAE}$ and $\overline{PAF}$ can show a valid status only after the the full set of bits have been entered. The registers can be re-programmed, as long as both offsets are loaded. When $\overline{LD}$ is LOW and $\overline{SEN}$ is HIGH, no serial write to the registers can occur.

Once parallel offset loading has been selected, then programming $\overline{PAE}$ and $\overline{PAF}$ procedes as follows: When $\overline{LD}$ and $\overline{WEN}$ are set LOW, data on the inputs D_n are written into the Empty Offset Register on the first LOW-to-HIGH transition of WCLK. Upon the second LOW-to-HIGH transition of WCLK, data at the inputs are written into the Full Register. The third transition of WCLK writes, once again, to the Empty Offset Register.

To ensure proper programming (serial or parallel) of the offset registers, no read operation is permitted from the time of reset (master or partial) to the time of programming. (During this period, the read pointer must be pointing to the first location of the memory array.) After the programming has been accomplished, read operations may begin.

Write operations to memory are allowed before and during the parallel programming sequence. In this case, the programming of all offset registers does not have to occur at one time. One or two offset registers can be written to and then, by bringing $\overline{LD}$ HIGH, write operations can be redirected to the FIFO memory. When $\overline{LD}$ is set LOW again, and $\overline{WEN}$ is LOW, the next offset register in sequence is written to. As an alternative to holding $\overline{WEN}$ LOW and toggling $\overline{LD}$, parallel programming can also be interrupted by setting $\overline{LD}$ LOW and toggling $\overline{WEN}$.

Write operations to memory are allowed before and during the serial programming sequence. In this case, the programming of all offset bits does not have to occur at once. A select number of bits can be written to the SI input and then, by bringing $\overline{LD}$ and $\overline{SEN}$ HIGH, data can be written to FIFO memory via D_n by toggling $\overline{WEN}$. When $\overline{WEN}$ is brought HIGH with $\overline{LD}$ and $\overline{SEN}$ restored to a LOW, the next offset bit in sequence is written to the registers via SI. If a mere interuption of serial programming is desired, it is sufficient either to set $\overline{LD}$ LOW and deactivate $\overline{SEN}$ or to set $\overline{SEN}$ LOW and deactivate $\overline{LD}$. Once $\overline{LD}$ and $\overline{SEN}$ are both restored to a LOW level, serial offset programming continues from where it left off.

Note that the status of a partial flag ($\overline{PAE}$ or $\overline{PAF}$) output is invalid during the programming process. From the time parallel programming has begun, a partial flag output will not be valid until the appropriate offset word has been written to the register pertaining to that flag. From the time serial programming has begun, neither partial flag will be valid until the full set of bits required to fill all the offset registers has been written. Measuring from the rising WCLK edge that achieves either of the above criteria; $\overline{PAF}$ will be valid after two more rising WCLK edges plus t_{PAF}, $\overline{PAE}$ will will be valid after the next two rising RCLK edges plus t_{PAE} (Add one more RCLK cycle if t_{SKEW2} is not met.)

The act of reading the offset registers employs a dedicated read offset register pointer. The contents of the offset registers can be read on the output lines when $\overline{LD}$ is set LOW and $\overline{REN}$ is set LOW; then, data are read via Q_n from the LSB Empty Offset Register on the first LOW-to-HIGH transition of RCLK. Upon the second LOW-to-HIGH transition of RCLK, data are read from the MSB Empty Offset Register. Upon the third LOW-to-HIGH transition of RCLK, data are read from the LSB Full Offset Register. Upon the fourth LOW-to-HIGH transition of RCLK, data are read from the MSB Full Offset Register. The fifth transition of RCLK reads, once again, from the LSB Empty Offset Register.

It is permissable to interrupt the the offset register access sequence with reads or writes to memory. The interruption is accomplished by deasserting $\overline{REN}$, $\overline{LD}$, or both together. When $\overline{REN}$ and $\overline{LD}$ are restored to a LOW level, access of the registers continues where it left off.

$\overline{LD}$ functions the same way in both IDT Standard and FWFT modes.

FREQUENCY SELECT INPUT (FS)

An internal state machine manages the movement of data through the Supersync FIFO. The FS line determines whether RCLK or WCLK will synchronize the state machine. Tie FS to V_{CC} if the RCLK line is running at a lower frequency than the WCLK line. In this case, the state machine will be synchronized to WCLK. Tie FS to GND if the RCLK line is running at a higher frequency than the WCLK line. In this case, the state machine will be synchronized to RCLK. Note that FS must be set so the clock line running at the higher frequency drives the state machine; this ensures efficient handling of the data within the FIFO. If the same clock signal drives both the WCLK and the RCLK pins, then tie FS to GND.

The frequency of the clock tied to the state machine (referred to as the "selected clock") may be changed at any time, so long as it is always greater than or equal to the frequency of the clock that is not tied to the state machine (referred to as the "non-selected clock"). The frequency of the non-selected clock can also be varied with time, so long as it never exceeds the frequency of the selected clock. To be more specific, the frequencies of both RCLK and WCLK may be varied during FIFO operation, provided that, at any given point in time, the cycle period of the selected clock is equal to or less than the cycle period of the non-selected clock.

The selected clock must be continuous. It is, however, permissible to stop the non-selected clock. Note, so long as RCLK is idle, $\overline{EF}/\overline{OR}$ and $\overline{PAE}$ will not be updated. Likewise, as long as WCLK is idle, $\overline{FF}/\overline{IR}$ and $\overline{PAF}$ will not be updated.

Changing the FS setting during FIFO operation (i.e. read-

ing or writing) is not permitted; however, such a change at the time of Master Reset or Partial Reset is all right. FS is an asynchronous input.

OUTPUTS:

FULL FLAG ($\overline{FF}/\overline{IR}$)

This is a dual purpose pin. In IDT Standard Mode, the Full Flag ($\overline{FF}$) function is selected. When the FIFO is full (i.e. the write pointer catches up to the read pointer), $\overline{FF}$ will go LOW, inhibiting further write operation. When $\overline{FF}$ is HIGH, the FIFO is not full. If no reads are performed after a reset (either MRS or PRS), $\overline{FF}$ will go LOW after 8,192 writes tor the IDT72255 and 16,384 writes to the IDT72265.

In FWFT Mode, the Input Ready ($\overline{IR}$) function is selected. $\overline{IR}$ goes LOW when memory space is available for writing in data. When there is no longer any free space left, $\overline{IR}$ goes HIGH, inhibiting further write operation. If no reads are performed after a reset (either MRS or PRS), $\overline{IR}$ will go HIGH after 8,193 writes for the IDT72255 and 16,385 writes for the IDT72265.

The $\overline{IR}$ status not only measures the contents of the FIFO memory, but also counts the presence of a word in the output register. Thus, in FWFT mode, the total number of writes necessary to deassert $\overline{IR}$ is one greater than needed to assert $\overline{FF}$ in IDT Standard mode.

$\overline{FF}/\overline{IR}$ is synchronized to WCLK. It is double-registered to enhance metastable immunity.

EMPTY FLAG ($\overline{EF}/\overline{OR}$)

This is a dual purpose pin. In the IDT Standard Mode, the Empty Flag ($\overline{EF}$) function is selected. When the FIFO is empty (i.e. the read pointer catches up to the write pointer), $\overline{EF}$ will go LOW, inhibiting further read operations. When $\overline{EF}$ is HIGH, the FIFO is not empty.

When writing the first word to an empty FIFO, the deassertion time of $\overline{EF}$ is variable, and can be represent by the First Word Latency parameter, t_{FWL1}, which is measured from the rising WCLK edge that writes the first word to the rising RCLK edge that updates the flag. t_{FWL1} includes any delays due to clock skew and can be expressed as follows:

$$t_{FWL1} \text{ max.} = 10*T_f + 2*T_{RCLK} \text{ (in ns)}$$

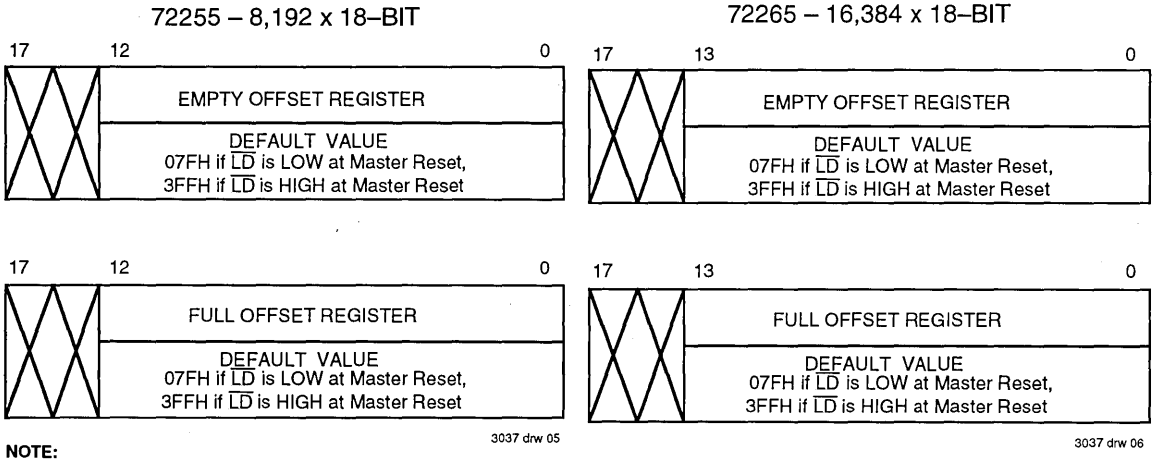
where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period. Since no read can take place until $\overline{EF}$ goes HIGH, the t_{FWL1} delay determines how early the first word can be available at Q_n. This delay has no effect on the reading of subsequent words.

In FWFT Mode, the Ouput Ready ($\overline{OR}$) function is selected. $\overline{OR}$ goes LOW at the same time that the first word written to an empty FIFO appears valid on the outputs. $\overline{OR}$ goes HIGH one cycle after RCLK shifts the last word from the FIFO memory to the outputs. Then further data reads are inhibited until $\overline{OR}$ goes LOW again.

When writing the first word to an empty FIFO, the assertion time of $\overline{OR}$ is variable, and can be represented by the First Word Latency parameter, t_{FWL2}, which is measured from the rising WCLK edge that writes the first word to the rising RCLK edge that updates the flag. t_{FWL2} includes any delay due to clock skew and can be expressed as follows:

$$t_{FWL2} \text{ max.} = 10*T_f + 3*T_{RCLK} \text{ (in ns)}$$

where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period. Note that the First Word Latency in FWFT mode is one RCLK cycle longer than in IDT Standard mode. The t_{FWL2} delay determines how early the first word can be available at Q_n. This delay has no effect



NOTE:
1. Any bits of the offset register not being programmed should be set to zero.

Figure 3. Offset Register Location and Default Values

on the reading of subsequent words.

$\overline{EF}/\overline{OR}$ is sychronized to the RCLK. It is double-registered to enhance metastable immunity.

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

The Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW when the FIFO reaches the Almost-Full condition as specified by the offset m stored in the Full Offset register.

At the time of Master Reset, depending on the state of $\overline{LD}$, one of two possible default offset values are chosen. If $\overline{LD}$ is LOW, then m = 07FH and the $\overline{PAF}$ switching threshold is 127 words from the Full boundary, if $\overline{LD}$ is HIGH, then m = 3FFH and the $\overline{PAF}$ switching threshold is 1023 words away from the Full boundary.

Any integral value of m from 0 to the maximum FIFO depth minus 1 (8,191 words for the 72255, 16,383 words for the 72265) can be programmed into the Full Offset register.

In IDT Standard Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{PAF}$ will go LOW after (8,192-m) writes to the IDT72255, and (16,384-m) writes to the IDT72265.

In FWFT Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{PAF}$ will go LOW after (8,193-m) writes to the IDT72255, and (16,385-m) writes to the IDT72265. In this case, the first word written to an empty FIFO does not stay in memory, but goes unrequested to the output register; therefore, it has no effect on determining the state of $\overline{PAF}$.

Note that even though $\overline{PAF}$ is programmed to switch LOW during the first word latency period (tFWL), attempts to read data will be ignored until $\overline{EF}$ goes HIGH indicating that data is available at the output port. This is true for both timing modes.

$\overline{PAF}$ is synchronous and updated on the rising edge of WCLK. It is double-registered to enhance metastable immunity.

TABLE I — STATUS FLAGS FOR IDT STANDARD MODE

Number of Words in FIFO Memory (1)						
72255	72265	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	H	H	H	L	L
1 to n (2)	1 to n (2)	H	H	H	L	H
(n+1) to 4,096	(n+1) to 8,192	H	H	H	H	H
4,097 to (8192-(m+1))	8,193 to (16,384-(m+1))	H	H	L	H	H
(8,192-m) (3) to 8,191	(16,384-m) (3) to 16,383	H	L	L	H	H
8,192	16,384	L	L	L	H	H

3037 tbl 03

NOTES:
1. Data in the output register does not count as a 'word in FIFO memory". Since in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
2. n = Empty Offset, Default Values: n = 127 when parallel offset loading is selected or n=1023 when serial offset loading is selected.
3. m = Full Offset, Default Values: m = 127 when parallel offset loading is selected or n=1023 when serial offset loading is selected.

TABLE II — STATUS FLAGS FOR FWFT MODE

Number of Words in FIFO Memory (1)						
72255	72265	$\overline{IR}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{OR}$
0	0	L	H	H	L	H (4)
1 to n (2)	1 to n (2)	L	H	H	L	L
(n+1) to 4,096	(n+1) to 8,192	L	H	H	H	L
4,097 to (8192-(m+1))	8,193 to (16,384-(m+1))	L	H	L	H	L
(8,192-m) (3) to 8,191	(16,384-m) (3) to 16,383	L	L	L	H	L
8,192	16,384	H	L	L	H	L

3037 tbl 04

NOTES:
1. Data in the output register does not count as a 'word in FIFO memory". Since in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
2. n = Empty Offset, Default Values: n = 127 when parallel offset loading is selected or n=1023 when serial offset loading is selected.
3. m = Full Offset, Default Values: m = 127 when parallel offset loading is selected or n=1023 when serial offset loading is selected.
4. Following a reset (Master or Partial), the FIFO memory is empty and $\overline{OR}$ = HIGH. After writing the first word, the FIFO memory remains empty, the data is placed into the output register, and $\overline{OR}$ goes LOW. In this case, or any time the last word in the FIFO memory has been read into the output register; a rising RCLK edge, enabled by $\overline{REN}$, will set $\overline{OR}$ HIGH.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

The Programmable Almost-Empty Flag ($\overline{PAE}$) will go LOW when the FIFO reaches the Almost-Empty condition as specified by the offset n stored in the Empty Offset register.

At the time of Master Reset, depending on the state of $\overline{LD}$, one of two possible default offset values are chosen. If $\overline{LD}$ is LOW, then n = 07FH and the $\overline{PAE}$ switching threshold is 127 words from the Empty boundary, if $\overline{LD}$ is HIGH, then n = 3FFH and the $\overline{PAE}$ switching threshold is 1023 words away from the Empty boundary.

Any integral value of n from 0 to the maximum FIFO depth minus 1 (8,191 words for the 72255, 16,383 words for the 72265) can be programmed into the Empty Offset register.

In IDT Standard Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), the $\overline{PAE}$ will go HIGH after (n + 1) writes to the IDT72255/72265.

In FWFT Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), the $\overline{PAE}$ will go HIGH after (n+2) writes to the IDT72255/72265. In this case, the first word written to an empty FIFO does not stay in memory, but goes unrequested to the output register; therefore, it has no effect on determining the state of $\overline{PAE}$.

Note that even though $\overline{PAE}$ is programmed to switch HIGH during the first word latency period (t_{FWL}), attempts to read data will be ignored until $\overline{EF}$ goes HIGH indicating that data is available at the output port. This is true for both timing modes.

$\overline{PAE}$ is synchronous and updated on the rising edge of RCLK. It is double-registered to enhance metastable immunity.

HALF-FULL FLAG ($\overline{HF}$)

This output indicates a half-full memory. The rising WCLK edge that fills the memory beyond half-full sets $\overline{HF}$ LOW. The flag remains LOW until the difference between the write and read pointers becomes less than or equal to half of the total depth of the device; the rising RCLK edge that accomplishes this condition also sets $\overline{HF}$ HIGH.

In IDT Standard Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{HF}$ will go LOW after (D/2 + 1) writes, where D is the maximum FIFO depth (8,192 words for the IDT72255, 16,384 words for the IDT72265).

In FWFT Mode, if no reads are performed after reset ($\overline{MRS}$ or $\overline{PRS}$), $\overline{HF}$ will go LOW after (D/2+2) writes to the IDT72255/72265. In this case, the first word written to an empty FIFO does not stay in memory, but goes unrequested to the output register; therefore, it has no effect on determining the state of $\overline{HF}$.

Because $\overline{HF}$ uses both RCLK and WCLK for synchronization purposes, it is asynchronous.

DATA OUTPUTS (Q_0-Q_{17})

Q_0-Q_{17} are data outputs for 18-bit wide data.

5

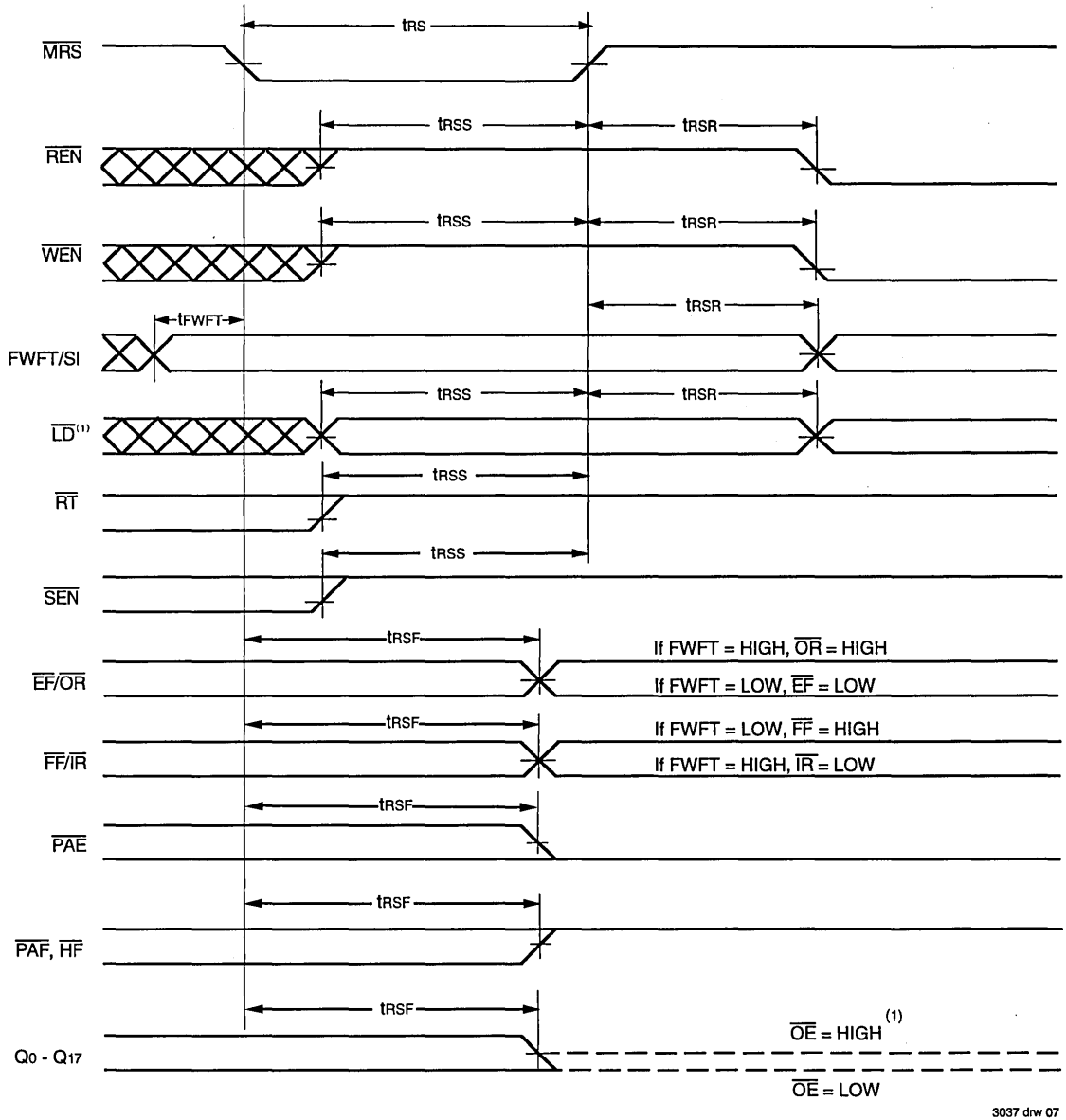


Figure 4. Master Reset Timing

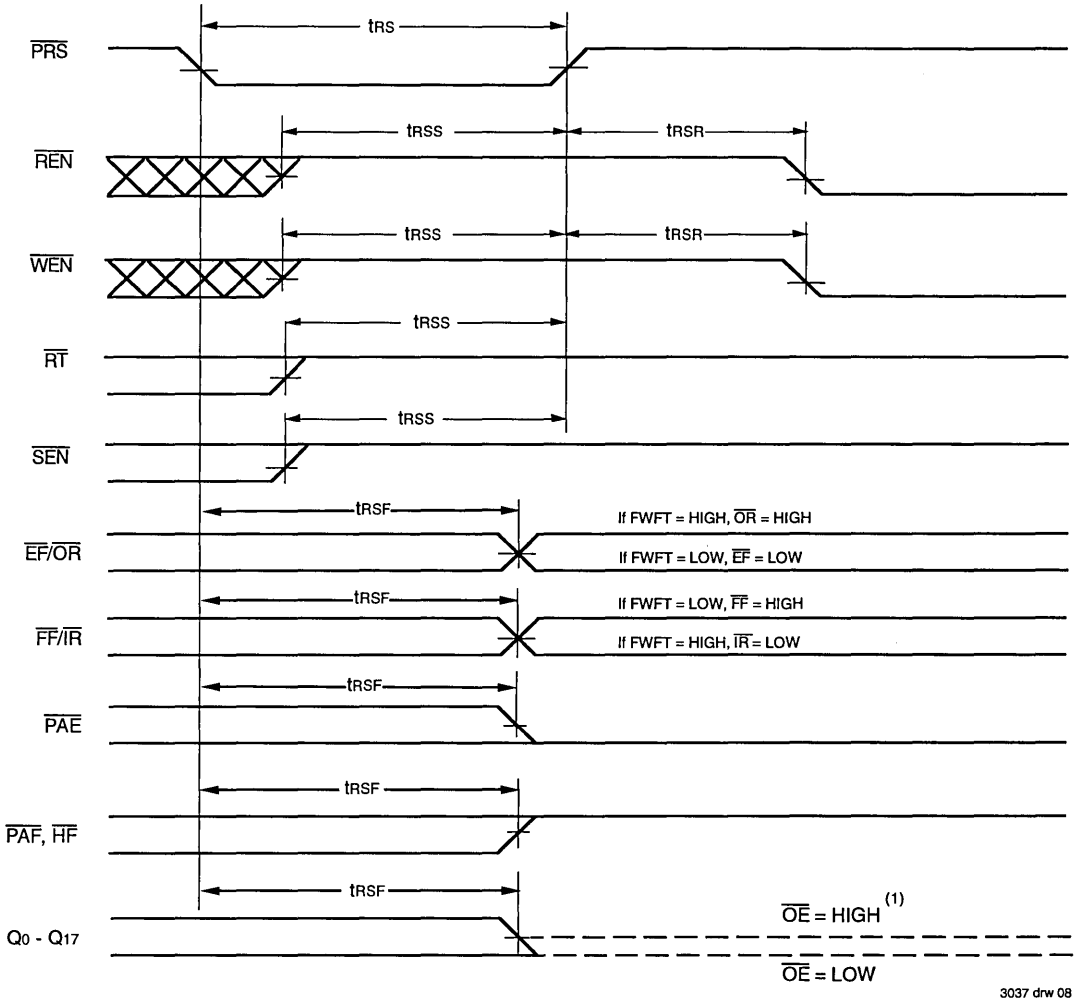
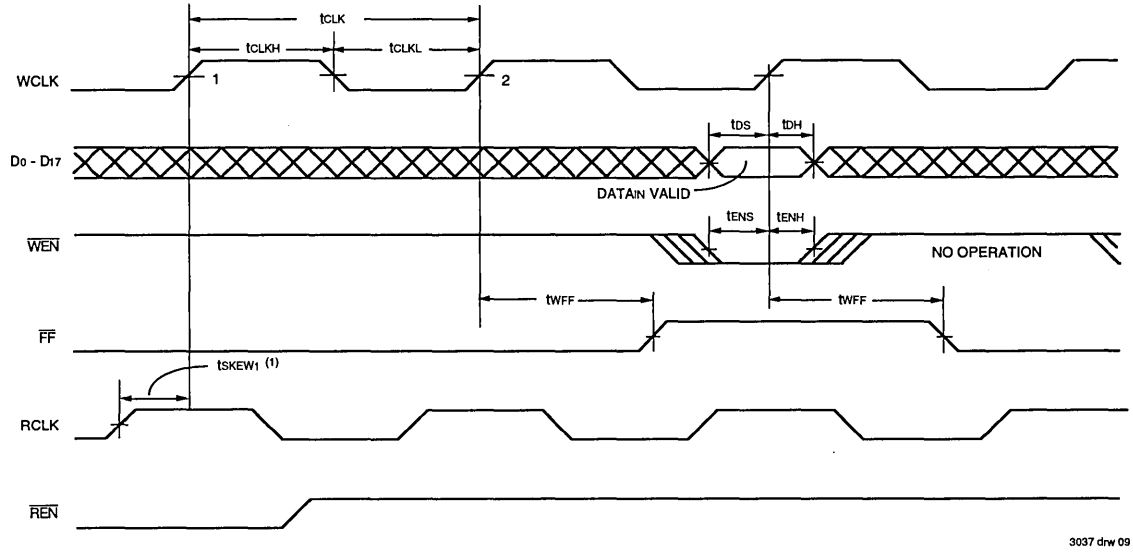
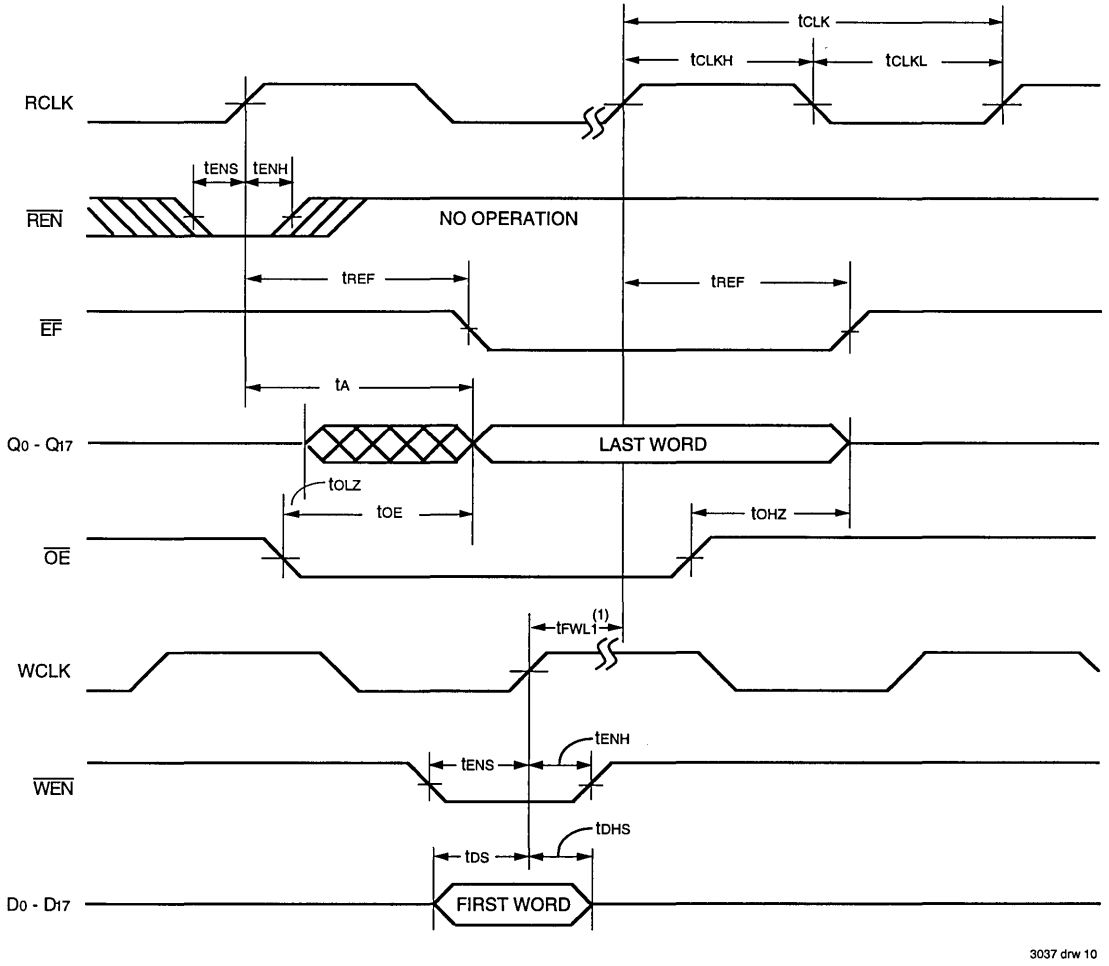


Figure 5. Partial Reset Timing



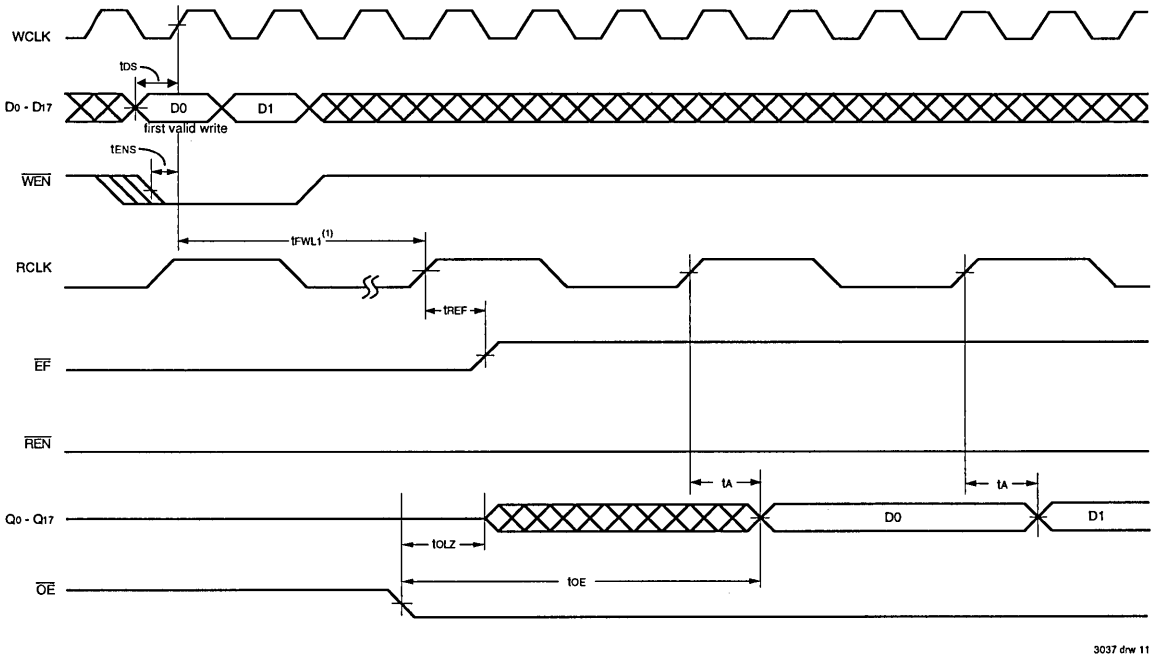
NOTES:
1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH (after one WCLK cycle plus tWFF). If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then the $\overline{FF}$ deassertion may be delayed an extra WCLK cycle.
2. $\overline{LD}$ = HIGH

Figure 6. Write Cycle Timing (IDT Standard Mode)



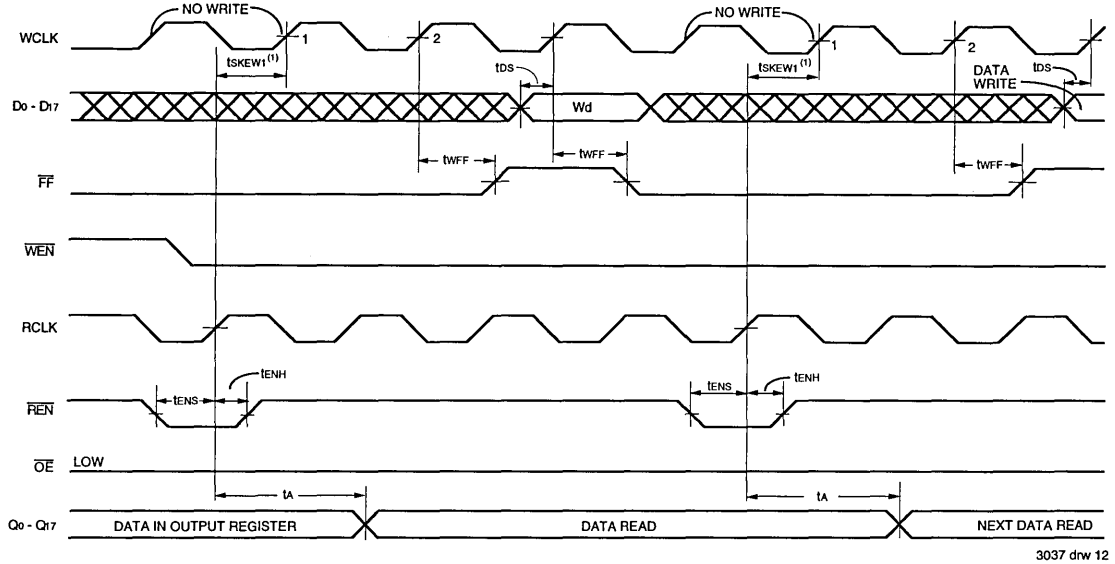
NOTES:
1. t_{FWL1} contributes a variable delay to the overall first word latency (this parameter includes delays due to skew):
   t_{FWL1} max. (in ns) = 10*Tf + 2* T_{RCLK}
   where Tf is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period
2. $\overline{LD}$ = HIGH

Figure 7. Read Cycle Timing (IDT Standard Mode)



NOTES:
1. t_{FWL1} max. (in ns) = 10* Tf + 2* T_{RCLK}
   Where Tf is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period
2. $\overline{LD}$ = HIGH

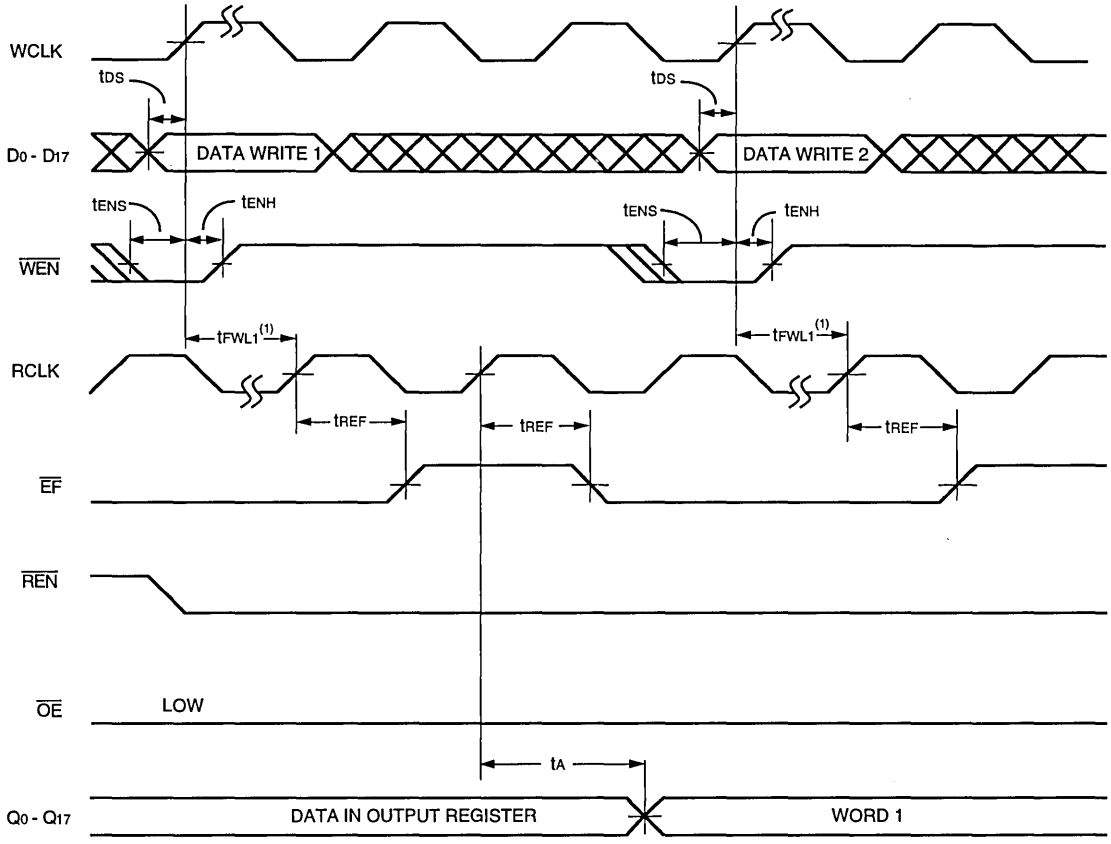
Figure 8. First Data Word Latency (IDT Standard Mode)



NOTES:
1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go high (after one WCLK cycle pus tWFF). If the time between the rising edge of the RCLK and the rising edge of the WCLK is less than tSKEW1, then the $\overline{FF}$ deassertion may be delayed an extra WCLK cycle.
2. $\overline{LD}$ = HIGH

Figure 9. Full Flag Timing (IDT Standard Mode)

5



3037 drw 13

NOTES:
1. t_{FWL1} max. (in ns) = 10*T_f + 2*T_{RCLK}
   Where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the period.
2. $\overline{LD}$ = HIGH

Figure 10. Empty Flag Timing (IDT Standard Mode)

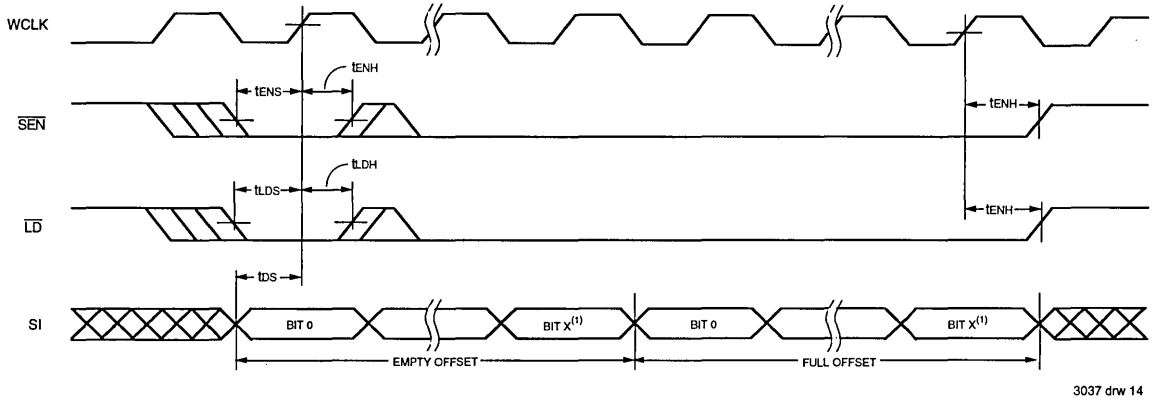


Figure 11. Serial Loading of Programmable Flag Registers (IDT Standard and FWFT modes)

NOTE:
1. For the 72255, X = 12.
   For the 72265, X = 13.

5

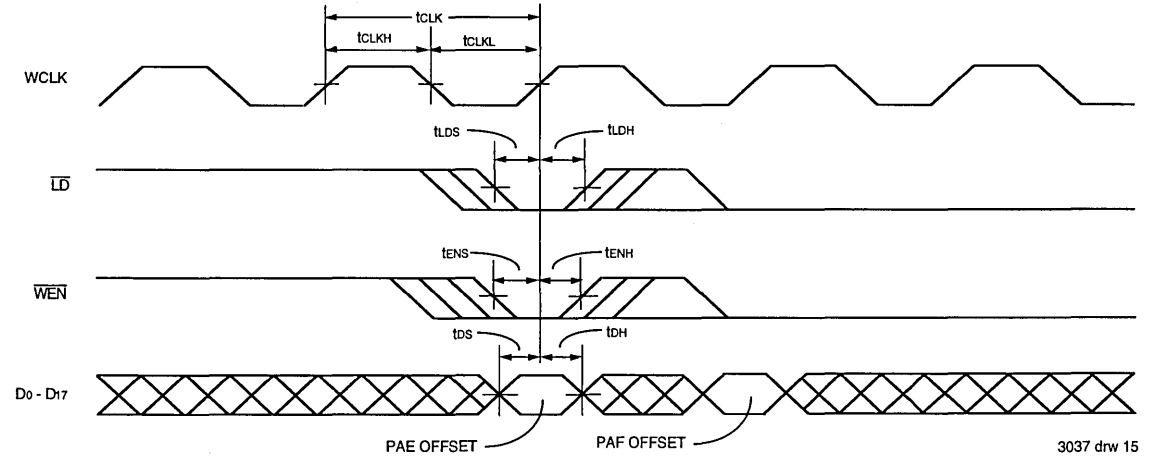


Figure 12. Parallel Loading of Programmable Flag Registers (IDT Standard and FWFT modes)

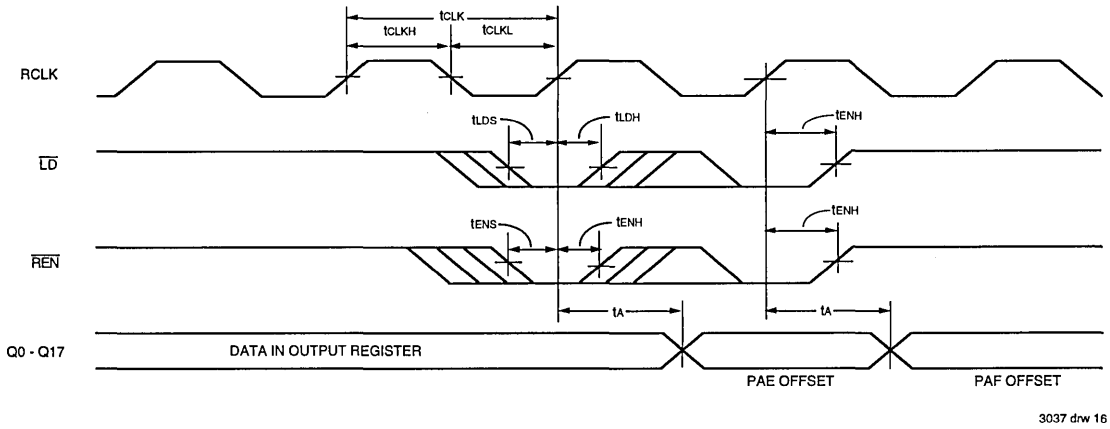
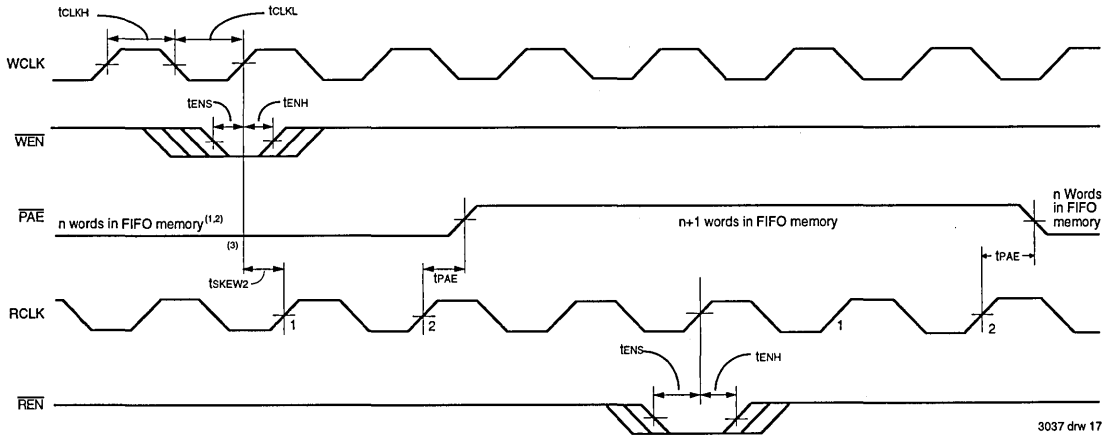


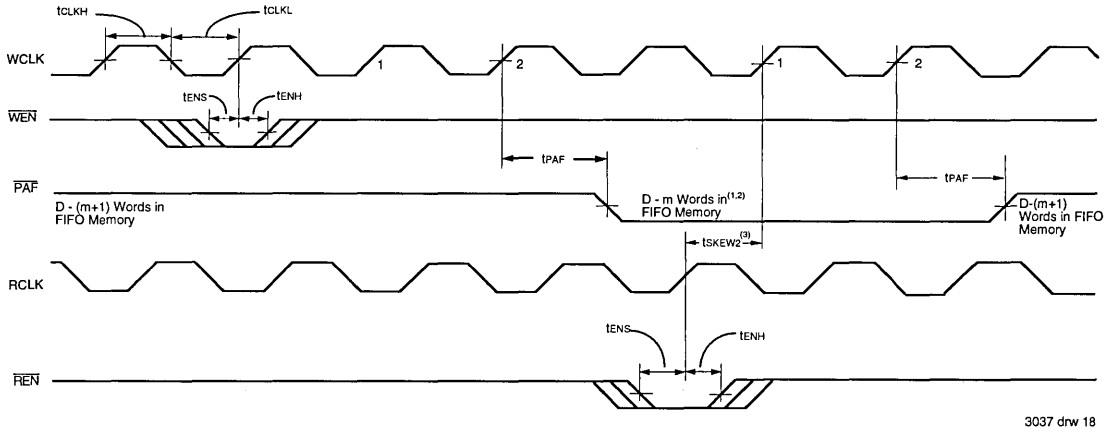
Figure 13. Parallel Read of Programmable Flag Registers (IDT Standard and FWFT modes)

NOTE:
1. $\overline{OE}$=LOW



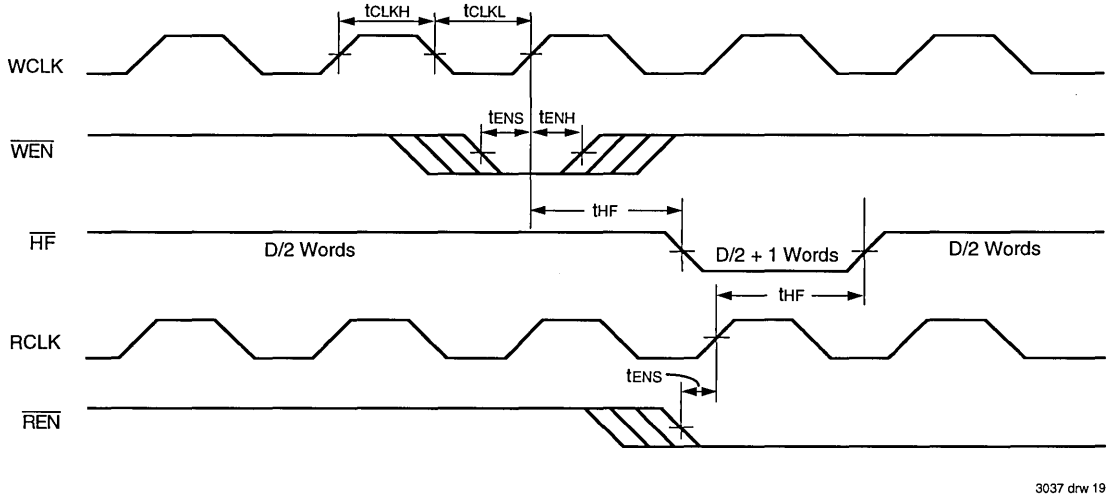
NOTES:
1. $\overline{PAE}$ offset = n
2. Data in the output register does not count as a "word in FIFO memory". Since, in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
3. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to go HIGH (after one RCLK cycle plus t_{PAE}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then the $\overline{PAE}$ deassertion may be delayed one extra RCLK cycle.

Figure 14. Programmable Almost Empty Flag Timing (IDT Standard and FWFT modes)



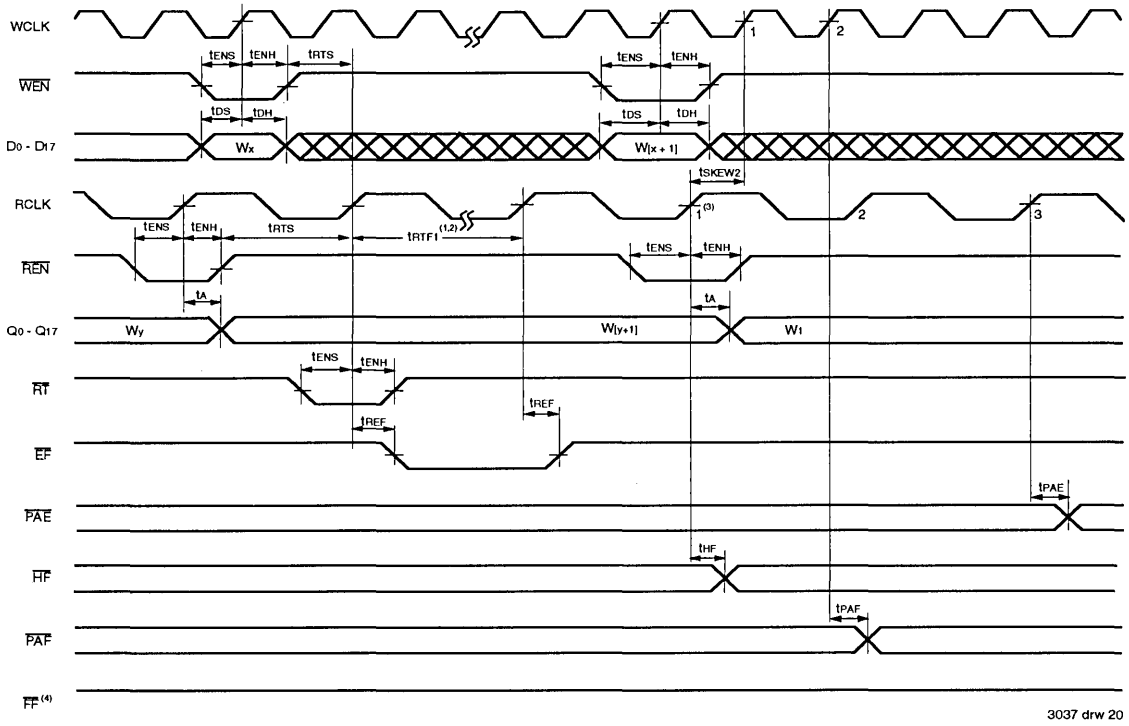
NOTES:
1. $\overline{PAF}$ offset = m, D = 8,192 for IDT 72255, 16,384 word for IDT 72265.
2. Data in the output register does not count as a "word in FIFO memory". Since, in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
3. tSKEW2 is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to go HIGH (after one WCLK cycle plus tPAF). If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW2, then the $\overline{PAF}$ deassertion time may be delayed an extra WCLK cycle.

Figure 15. Programmable Almost Full Flag Timing (IDT Standard and FWFT modes)



NOTE:
1. D = maximum FIFO depth = 8,192 for IDT 72255, 16,384 word for IDT 72265.

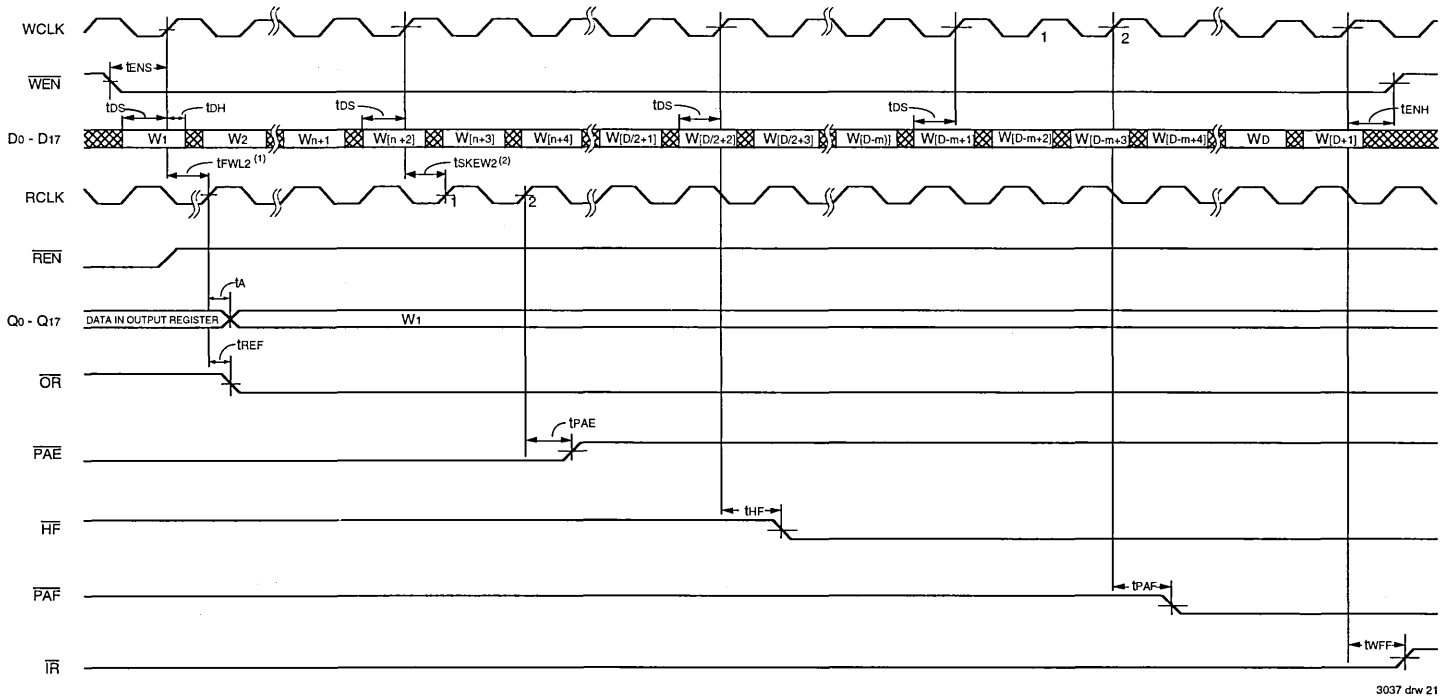
Figure 16. Half - Full Flag Timing (IDT Standard and FWFT modes)



NOTES:

1. t_{RTF1} contributes a variable delay to the overall retransmit recovery time:
   t_{RFTF1} max = 14*T_f + 3*T_{RCLK} (in ns)
   Where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period.
2. Retransmit set up is complete after $\overline{EF}$ returns HIGH, only then can a read operation begin. Write operations are permitted after one of two conditions have been met: $\overline{EF}$ is HIGH or 14 cycles of the faster clock (RCLK or WCLK) have elapsed since the RCLK rising edge enabled by the $\overline{RT}$ pulse.
3. Following Retransmit Setup, the rising edge of RCLK that accesses the first memory location also initiates the updating of $\overline{HF}$, $\overline{PAE}$, and $\overline{PAF}$.
4. No more than D-2 words (D = 8,192 words for the 72255, 16,384 words for the 72265) should have been written to the FIFO between Reset (Master or Partial) and Retransmit Setup. Therefore, $\overline{FF}$ will be HIGH throughout the Restransmit Setup procedure.
5. $\overline{OE}$=LOW

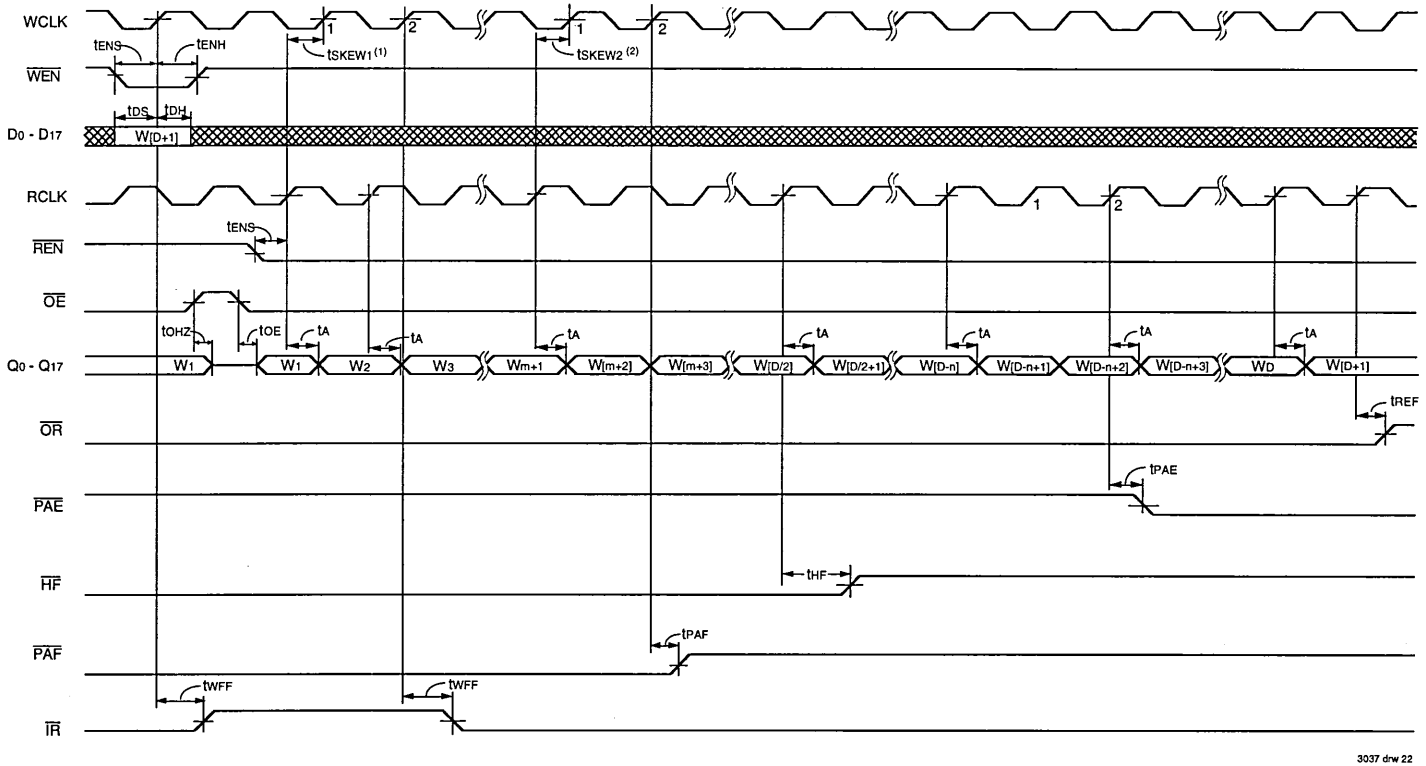
Figure 17. Retransmit Timing (IDT Standard mode)



NOTES:

1. t_{FWL2} max. (in ns) = 10*Tf + 3*T_{RCLK}
   where Tf is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to go HIGH (after one RCLK cycle plus t_{PAE}). If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then the $\overline{PAE}$ deassertion may be delayed one extra RCLK cycle.
3. $\overline{LD}$ = HIGH, $\overline{OE}$ = LOW
4. $\overline{PAE}$ offset = n, $\overline{PAF}$ offset = m, D = maximum FIFO depth = 8,192 words for the IDT72255, 16,384 words for the IDT72265.

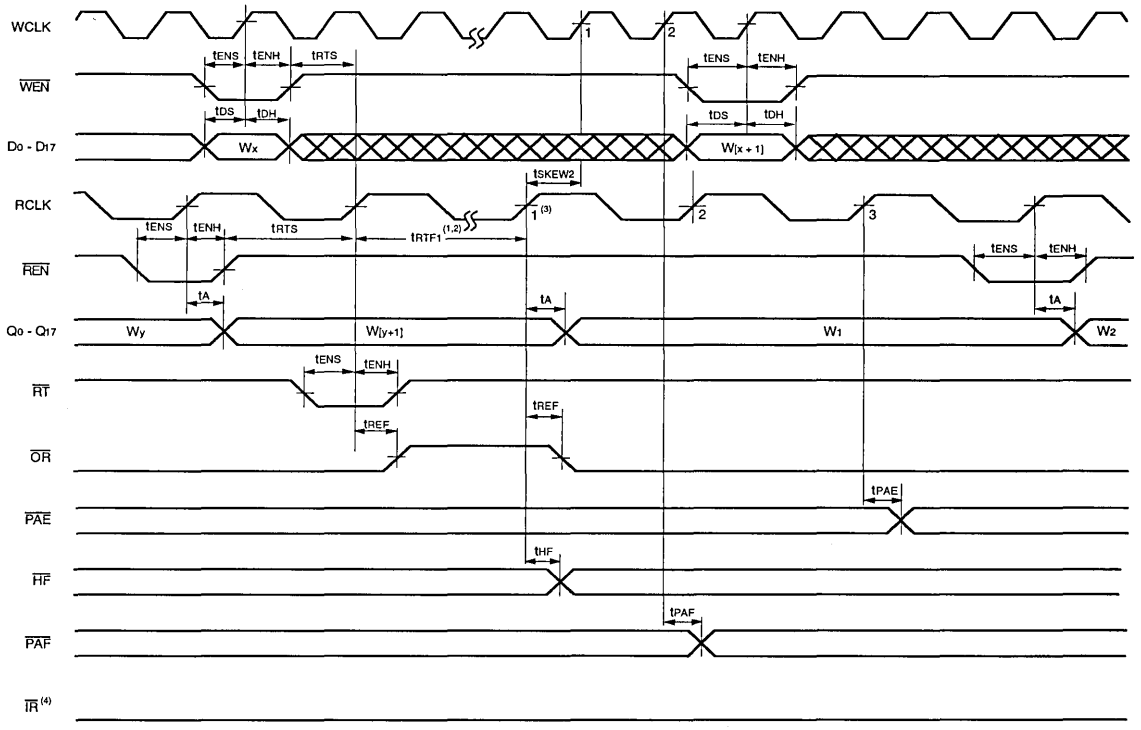
Figure 18. Write Timing (First Word Fall Through Mode)



NOTES:

1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{IR}$ will go LOW (after one WCLK cycle plus tWFF). If the time between the rising ege of RCLK and the rising edge of WCLK is less than tSKEW1, then the $\overline{IR}$ assertion may be delayed an extra WCLK cycle.
2. tSKEW2 is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to go HIGH (after one WCLK cycle plus tPAF). If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW2, then the $\overline{PAF}$ deassertion may be delayed an extra WCLK cycle.
3. $\overline{LD}$ = HIGH
4. $\overline{PAE}$ Offset = n, $\overline{PAF}$ offset = m, D = maximum FIFO depth = 8,192 words for the IDT72255, 16,384 words for the IDT72265.

Figure 19. Read Timing (First Word Fall Through Mode)



NOTES:

1. t_{RTF2} contribute a variable delay to the overall retransmit time:
   t_{RTF2} max = 13*T_f + 4*T_{RCLK} (in ns)
   Where T_f is either the RCLK or the WCLK period, whichever is shorter, and T_{RCLK} is the RCLK period.
2. Retransmit set up is complete after $\overline{OR}$ returns LOW, only then can a read operation begin. Write operations are permitted after one of two conditions have been met: $\overline{OR}$ is LOW or 14 cycles of the faster clock (RCLK or WCLK) have elapsed since the RCLK rising edge enabled by the $\overline{RT}$ pulse.
3. Following Retransmit Setup, the rising edge of RCLK that accesses the first memory location also initiates the updating of $\overline{HF}$, $\overline{PAE}$, and $\overline{PAF}$.
4. No more than D-2 words (D = 8,192 words for the 72255, 16,384 words for the 72265) should have been written to the FIFO between Reset (Master or Partial) and Retransmit Setup. Therefore, $\overline{IR}$ will be LOW throughout the Retransmit Setup procedure.
5. $\overline{OE}$=LOW

Figure 20. Retransmit Timing (FWFT mode)

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

A single IDT72255/72265 may be used when the application requirements are for 8,192/16,384 words or less. The IDT72255/72265 can always be used in Single Device Configuration, whether IDT Standard Mode or FWFT Mode has been selected. No special set up procedure is necessary.

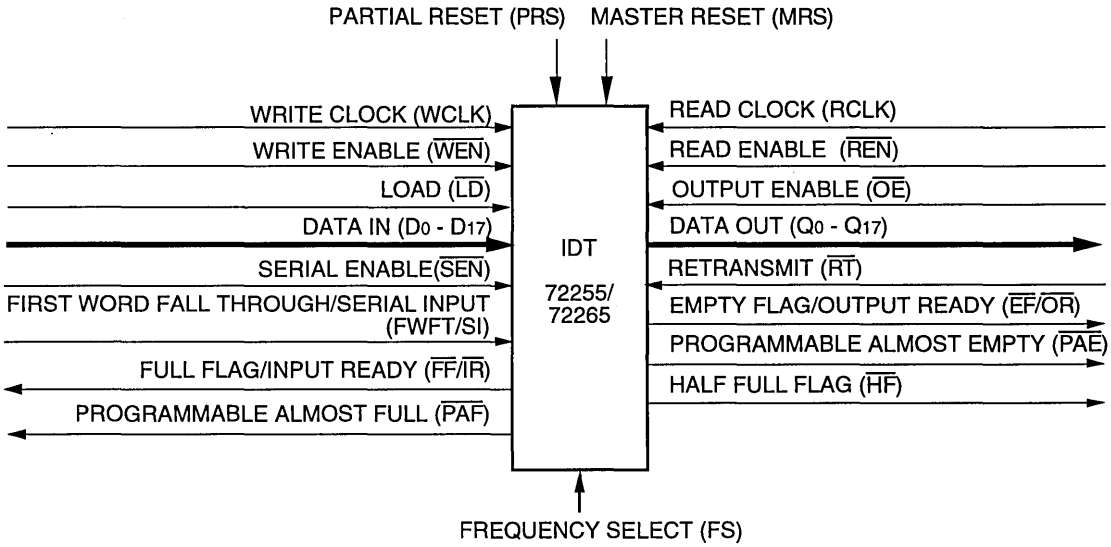
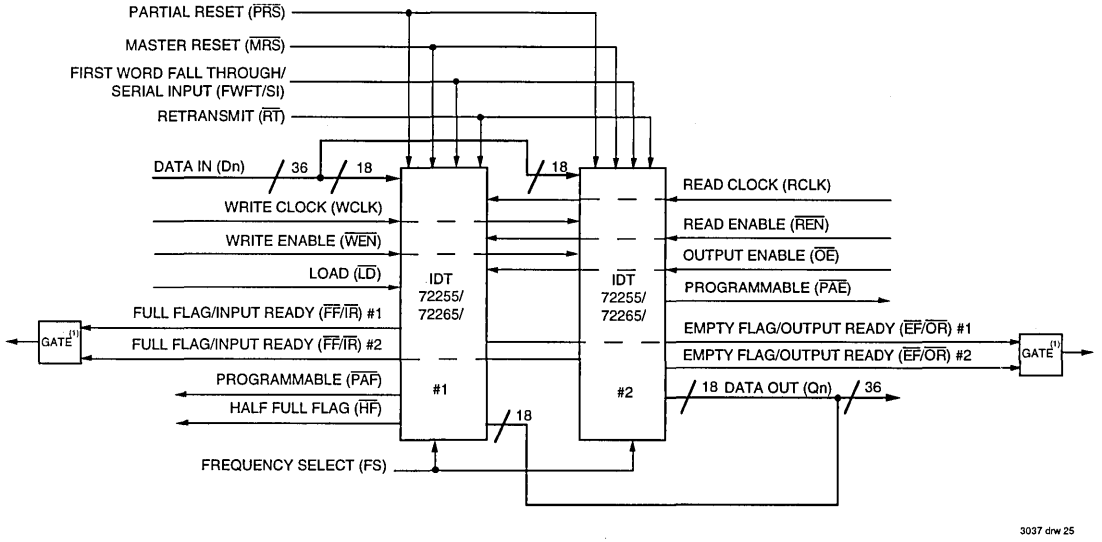


Figure 21. Block Diagram of Single 8,192x18/16,384x18 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting together the control signals of multiple devices. Status flags can be detected from any one device. The exceptions are the $\overline{EF}$ and $\overline{FF}$ functions in IDT Standard mode and the $\overline{IR}$ and $\overline{OR}$ functions in FWFT mode. Because of variations in skew between RCLK and WCLK, it is possible for $\overline{EF}$/$\overline{FF}$ deassertion and $\overline{IR}$/$\overline{OR}$ assertion to vary by one cycle between FIFOs. In IDT Standard mode, such problems can be avoided by creating composite flags, that is, ANDing $\overline{EF}$ of every FIFO, and separately ANDing $\overline{FF}$ of every FIFO. In FWFT mode, composite flags can be created by ORing $\overline{OR}$ of every FIFO, and separately ORing $\overline{IR}$ of every FIFO. Figure 22 demonstrates an 36-word width by using two IDT72255/72265s. Any word width can be attained by adding additional IDT72255/72265s.



3037 drw 25

NOTE:
1. Use an AND gate in IDT Standard mode, an OR gate in FWFT mode.
2. Do not connect any output control signals directly together.

Figure 22. Block Diagram of 8,192x36/16,384x36 72255/65 Width Expansion

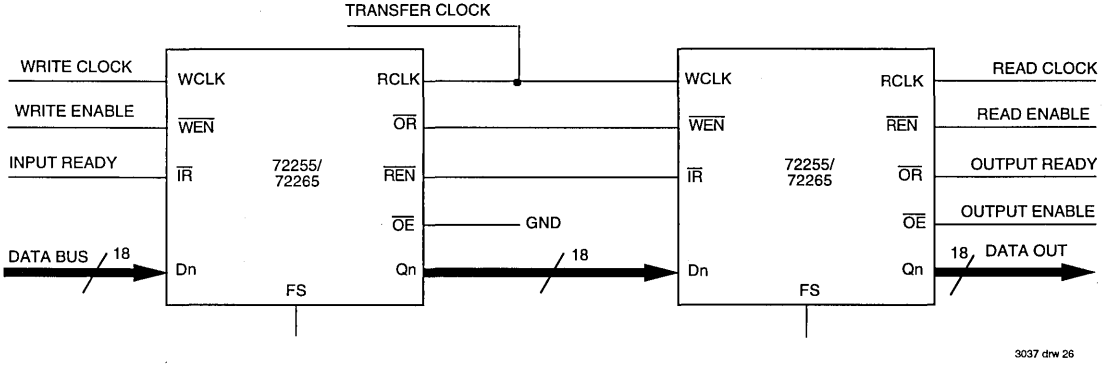
DEPTH EXPANSION CONFIGURATION

The IDT72255/72265 can easily be adapted to applications requiring more than 8,192/16,384 words of buffering. In FWFT mode, the FIFOs can be arranged in series (the data outputs of one FIFO connected to the data inputs of the next)–no external logic necessary. The resulting configuration provides a total depth equivalent to the sum of the depths associated with each single FIFO. Figure 23 shows a depth expansion using two IDT72255/72265s.

Care should be taken to select FWFT mode during Master Reset for all FIFOs in the depth expansion configuration. The first word written to an empty configuration will pass from one FIFO to the next ("ripple down") until it finally appears at the outputs of the last FIFO in the chain–no read operation is necessary. Each time the data word appears at the outputs of one FIFO, that device's $\overline{OR}$ line goes LOW, enabling a write to the next FIFO in line.

The $\overline{OR}$ assertion time is variable and is described with the help of the t_{FWL2} parameter, which includes including delay caused by clock skew:

$$t_{FWL2}\ max.= 10*T_f + 3*T_{RCLK}$$



3037 drw 26

Figure 23. Block Diagram of 16,384x18/32,768x18 Synchronous FIFO Memory With Programmable Flags used in Depth Expansion Configuration

where T_{RCLK} is the RCLK period and Tf is either the RCLK or the WCLK period, whichever is shorter.

The maximum amount of time it takes for a word to pass from the inputs of the first FIFO to the outputs of the last FIFO in the chain is the sum of the delays for each individual FIFO:

$$t_{FWL2(1)} + t_{FWL2(2)} + \ldots + t_{FWL2(N)} + N*T_{RCLK}$$

where N is the number of FIFOs in the expansion.

Note that the additional RCLK term accounts for the time it takes to pass data between FIFOs.

The ripple down delay is only noticeable for the first word written to an empty depth expansion configuration. There will be no delay evident for subsequent words written to the configuration.

The first free location created by reading from a full depth expansion configuration will "bubble up" from the last FIFO to the previous one until it finally moves into the first FIFO of the chain. Each time a free location is created in one FIFO of the chain, that FIFO's $\overline{IR}$ line goes LOW, enabling the preceding FIFO to write a word to fill it.

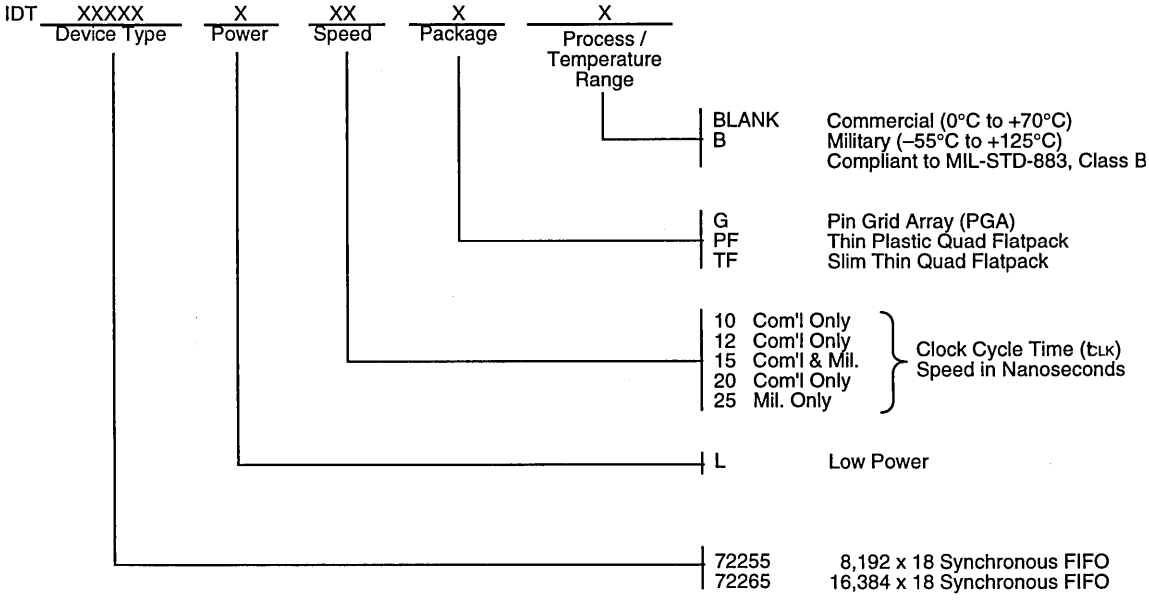
The amount of time it takes for $\overline{IR}$ of the first FIFO in the chain to assert after a word is read from the last FIFO is the sum of the delays for each individual FIFO:

$$N*(3*T_{WCLK})$$

where N is the number of FIFOs in the expansion and T_{WCLK} is the WCLK period. Note that one of the three WCLK cycle accounts for T_{SKEW1} delays.

In a Supersync depth expansion, set FS individually for each FIFO in the chain. The Transfer Clock line should be tied to either WCLK or RCLK, whichever is faster. Both these actions result in moving, as quickly as possible, data to the end of the chain and free locations to the beginning of the chain.

ORDERING INFORMATION



3037 drw 27

Integrated Device Technology, Inc.

CMOS SINGLE BIT SyncFIFO™ 64 X 1, 256 x 1, 512 x 1

PRELIMINARY
IDT72423
IDT72203
IDT72213

FEATURES:

- 64 x 1-bit organization (IDT72423)
- 256 x 1-bit organization (IDT72203)
- 512 x 1-bit organization (IDT72213)
- 10 ns read/write cycle time (IDT72423/72203/72213)
- Independent read and write clock lines
- Empty and Full flags signal FIFO status
- Programmable Almost-Empty and Almost-Full flags can be programmed to any depth via a dedicated port (Pn). These flags default to Empty+7 and Full-7, respectively.
- Output enable puts output data bus in high impedance state
- Available in 24-pin SOIC, 24-pin plastic DIP (300 mil.), and 24-pin ceramic DIP (300 mil.)
- Military product compliant to MIL-STD-883, Class B Advanced submicron CMOS technology

DESCRIPTION:

The IDT72423/72203/72213 SyncFIFO™ are very high-speed, low-power First-In, First-Out (FIFO) memories with a word width of 1 and clocked read and write controls. The IDT72423/72203/72213 have a 64, 256, and 512 x 1-bit memory arrays, respectively. These FIFOs are appropriate for a wide variety of serial data buffering needs, especially telecommunications applications such as networks, modems, signal processing, and serial interfaces.

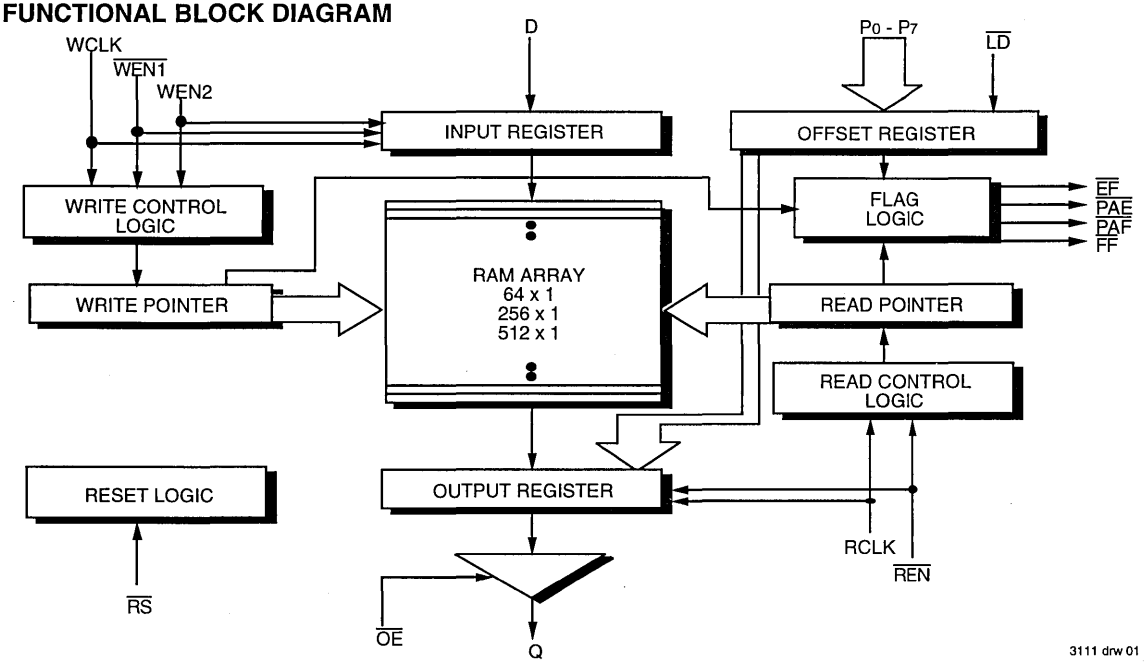
These single-bit FIFOs have 1-bit input (D) and output ports (Q). The input port is controlled by a free-running clock (WCLK), and two write enable pins ($\overline{WEN1}$, WEN2). Data is written into the Synchronous FIFO on every rising clock edge when the write enable pins are asserted. The output port is controlled by another clock pin (RCLK) and a read enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

The Synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$). Two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$), are provided for improved system control. The programmable flags default to Empty+7 and Full-7 for $\overline{PAE}$ and $\overline{PAF}$, respectively. The programmable flag offset is loaded via the Program Inputs (P0 - P7), on the rising WCLK when the load pin ($\overline{LD}$) is asserted.

The IDT72423/72203/72213/ are fabricated using IDT's high-speed submicron CMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

5

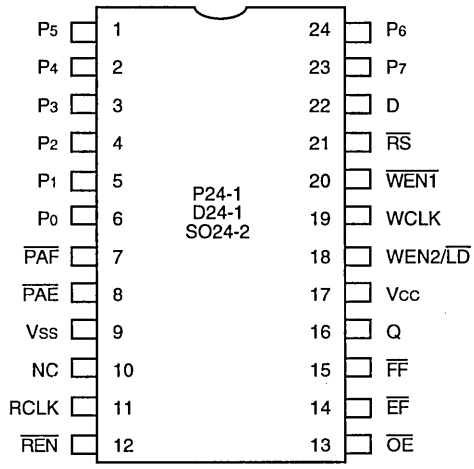
FUNCTIONAL BLOCK DIAGRAM



3111 drw 01

The IDT logo is a registered trademark and SyncFIFO is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



DIP/SOIC
TOP VIEW

3111 drw 02

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D	Data Input	I	Input for serial data.
RS	Reset	I	When RS is set LOW, internal read and write pointers are set to the first location of the RAM array, FF and PAF go HIGH, and PAE and EF go LOW. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when the Write Enable(s) are asserted.
WEN1	Write Enable 1	I	If the FIFO is configured to have programmable flags, WEN1 is the only write enable pin. When WEN1 is LOW, data is written into the FIFO on every LOW-to-HIGH transition WCLK. If the FIFO is configured to have two write enables, WEN1 must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the FF is LOW.
WEN2/LD	Write Enable 2/ Load	I	The FIFO is configured at reset to have either two write enables or programmable flags. If WEN2/LD is HIGH at reset, this pin operates as a second write enable. If WEN2/LD is LOW at reset, this pin operates as a control to load and read the programmable flag offsets. If the FIFO is configured to have two write enables, WEN1 must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the FF is LOW. If the FIFO is configured to have programmable flags, WEN2/LD is held LOW to write or read the programmable flag offsets.
P0-P7	Program Inputs	I	Offsets for the programmable flag registers are entered at these inputs on the rising edge of WCLK when LD and WEN are LOW
Q	Data Output	O	Output for serial data.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when REN is asserted.
REN	Read Enable 1	I	When REN is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the EF is LOW.
OE	Output Enable	I	When OE is LOW, the data output bus is active. If OE is HIGH, the output data bus will be in a high impedance state.
EF	Empty Flag	O	When EF is LOW, the FIFO is empty and further data reads from the output are inhibited. When EF is HIGH, the FIFO is not empty. EF is synchronized to RCLK.
PAE	Programmable Almost-Empty Flag	O	When PAE is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is Empty+7. PAE is synchronized to RCLK.
PAF	Programmable Almost-Full Flag	O	When PAF is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is Full-7. PAF is synchronized to WCLK.
FF	Full Flag	O	When FF is LOW, the FIFO is full and further data writes into the input are inhibited. When FF is HIGH, the FIFO is not full. FF is synchronized to WCLK.
Vcc	Power		One +5Volt power supply pin.
GND	Ground		One 0Volt ground pin.

3111 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +135	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 3111 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}	Input Low Voltage Commercial & Military	—	—	0.8	V

3111 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES: 3111 tbl 04

1. With output deselected ($\overline{OE}$ = HIGH).
2. Characterized values, not currently tested.

5

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72423 IDT72203 IDT72213 Commercial t_{CLK} = 10, 12, 15ns Min.	Typ.	Max.	IDT72423 IDT72203 IDT72213 Military t_{CLK} = 15, 25ns Min.	Typ.	Max.	Unit
I_{LI}(1)	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = -2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC}(3)	Active Power Supply Current	—	—	80	—	—	100	mA

3111 tbl 05

NOTES:

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Measurements are made with outputs unloaded. Tested at f_{CLK} = 20MHz.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Commmercial				Com'l & Mil.		Military		
		72423L10 72203L10 72213L10		72423L12 72203L12 72213L12		72423L15 72203L15 72213L15		72423L25 72203L25 72213L25		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
fS	Clock Cycle Frequency	100	—	—	83.3	—	66.7	—	40	Mhz
tA	Data Access Time	2	7.5	2	8	2	10	3	15	ns
tCLK	Clock Cycle Time	10	—	12	—	15	—	25	—	ns
tCLKH	Clock High Time	4.5	—	5	—	6	—	10	—	ns
tCLKL	Clock Low Time	4.5	—	5	—	6	—	10	—	ns
tDS	Data Set-up Time	3	—	3	—	4	—	6	—	ns
tDH	Data Hold Time	0	—	0	—	1	—	1	—	ns
tENS	Enable Set-up Time	3	—	3	—	4	—	6	—	ns
tENH	Enable Hold Time	0	—	0.2	—	1	—	1	—	ns
tRS	Reset Pulse Width[1]	10	—	12	—	15	—	25	—	ns
tRSS	Reset Set-up Time	10	—	12	—	15	—	25	—	ns
tRSR	Reset Recovery Time	10	—	12	—	15	—	25	—	ns
tRSF	Reset to Flag and Output Time	10	—	—	12	—	15	—	25	ns
tOLZ	Output Enable to Output in Low-Z[2]	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	6.5	3	7	3	8	3	13	ns
tOHZ	Output Enable to Output in High-Z[2]	3	6.5	3	7	3	8	3	13	ns
tWFF	Write Clock to Full Flag	7.5	—	—	8	—	10	—	15	ns
tREF	Read Clock to Empty Flag	7.5	—	—	8	—	10	—	15	ns
tAF	Write Clock to Almost-Full Flag	7.5	—	—	8	—	10	—	15	ns
tAE	Read Clock to Almost-Empty Flag	7.5	—	—	8	—	10	—	15	ns
tSKEW1	Skew time between Read Clock & Write Clock for Empty Flag &Full Flag	5	—	5	—	6	—	10	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Almost-Full Flag	22	—	22	—	28	—	40	—	ns

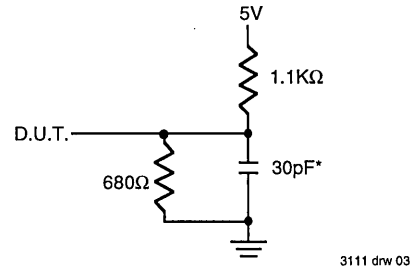
NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

3111 tbl 06

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

3111 tbl 07



3111 drw 03

or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

Data In (D) — Input for serial data.

CONTROLS:

Reset ($\overline{RS}$)—Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) will be reset to HIGH after t_{RSF}. The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) will be reset to low after t_{RSF}. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

Write Clock (WCLK)—A write cycle is initiated on the LOW-to-HIGH transition of the write clock (WCLK). Data set-up and hold times must be met in respect to the LOW-to-HIGH transition of the write clock (WCLK). The Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) are synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

Write Enable 1 ($\overline{WEN1}$)—If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable 1 ($\overline{WEN1}$) is HIGH, the input register holds the previous data and no new data is allowed to be loaded into the register.

If the FIFO is configured to have two write enables, which allows for depth expansion, there are two enable control pins. See Write Enable 2 paragraph below for operation in this configuration.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go high after t_{WFF}, allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) is ignored when the FIFO is full.

Read Clock (RCLK) — Data can be read on the outputs on the LOW-to-HIGH transition of the read clock (RCLK). The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) are synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

The write and read clocks can be asynchronous or coincident.

Read Enables ($\overline{REN}$)—When the Read Enable ($\overline{REN}$) is LOW, data is read from the RAM array to the output register on the LOW-to-HIGH transition of the read clock (RCLK).

When the Read Enable ($\overline{REN}$) is HIGH, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{REF} and a valid read can begin. The Read Enable ($\overline{REN}$) is ignored when the FIFO is empty.

Output Enable ($\overline{OE}$)—When Output Enable ($\overline{OE}$) is enabled (LOW), the output buffer receives data from the output register. When Output Enable ($\overline{OE}$) is disabled (HIGH), the Q data output is in a high-impedance state.

Write Enable 2/Load (WEN2/$\overline{LD}$)—This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows depth expansion. If Write Enable 2/Load (WEN2/$\overline{LD}$) is set HIGH at Reset ($\overline{RS}$ = LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{WEN1}$) is LOW and Write Enable 2/Load (WEN2/$\overline{LD}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable ($\overline{WEN1}$) is HIGH and/or Write Enable 2/Load (WEN2/$\overline{LD}$) is LOW, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go HIGH after t_{WFF}, allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load (WEN2/$\overline{LD}$) are ignored when the FIFO is full.

The FIFO is configured to have programmable flags when the Write Enable 2/Load (WEN2/$\overline{LD}$) is set LOW at Reset ($\overline{RS}$ = LOW). The IDT72423/72203/72213 devices contain four 8-bit offset registers which can be loaded with data on the Program Inputs (P_0 - P_7). See Figure 3 for details of the size of the registers and the default values.

If the FIFO is configured to have programmable flags when the Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load (WEN2/$\overline{LD}$) are set LOW, data on the Program Inputs (P_0 - P_7) are written into the Empty (Least Significant Bit) offset register on the first LOW-to-HIGH transition of the write clock (WCLK). Data is written into the Empty (Most Significant Bit) offset register on the second LOW-to-HIGH transition of the write clock (WCLK), into the Full (Least Significant Bit) offset register on the third transition, and into the Full (Most Significant Bit) offset register on the fourth transition. The fifth transition of the write clock (WCLK) again writes to the Empty (Least Significant Bit) offset register.

5

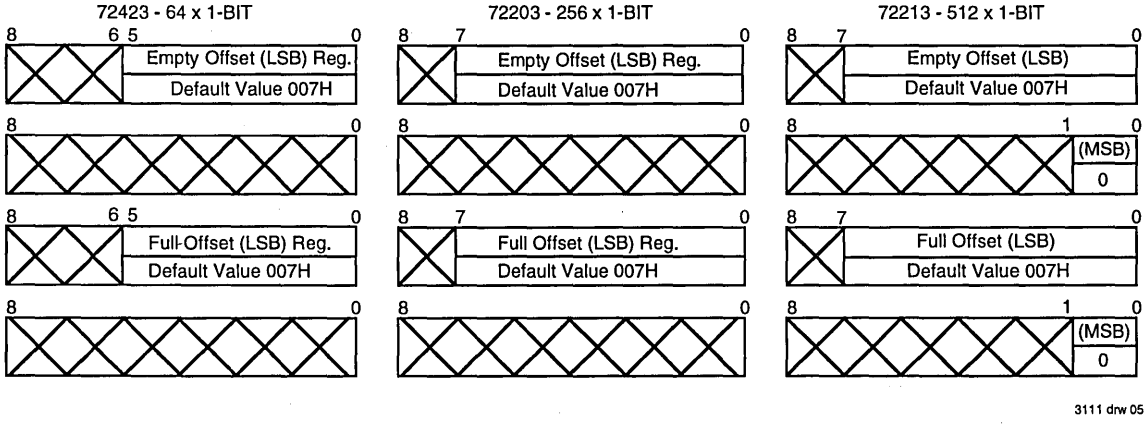
However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the Write Enable 2/Load (WEN2/$\overline{LD}$) pin HIGH, the FIFO is returned to normal read/write operation. When the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set LOW, and Write Enable 1 ($\overline{WEN1}$) is LOW, the next offset register in sequence is written.

Program Inputs (P_0 - P_7)—Flag offsets on these inputs are entered into the programmable offset registers on the rising edge of WCLK when $\overline{LD}$ and $\overline{WEN}$ are LOW.

LD	WEN1	WCLK[1]	Selection
0	0	↑	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	↑	No Operation
1	0	↑	Write into FIFO
1	1	↑	No Operation

3111 tbl 08

Figure 2. Write Offset Register



3111 drw 05

Figure 3. Offset Register Location and Default Values

OUTPUTS:

Full Flag ($\overline{FF}$)—The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operation, when the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 64 writes for the IDT72423, 256 writes for the IDT72203, 512 writes for the IDT72213.

The Full Flag ($\overline{FF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Empty Flag ($\overline{EF}$)—The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Programmable Almost-Full Flag ($\overline{PAF}$)—The Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW when the FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW after (64-m) writes for the IDT72423, (256-m) writes for the IDT72203, (512-m) writes for the IDT72213. The offset "m" is defined in the Full offset registers.

If there is no Full offset specified, the Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW at Full-7 words.

The Programmable Almost-Full Flag ($\overline{PAF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Programmable Almost-Empty Flag ($\overline{PAE}$)—The Programmable Almost-Empty Flag ($\overline{PAE}$) will go LOW when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the Empty offset registers. If no reads are performed after Reset the Programmable Almost-Empty Flag ($\overline{PAE}$) will go HIGH after "n+1" for the IDT72423/72203/72213. If there is no Empty offset specified, the Programmable Almost-Empty Flag ($\overline{PAE}$) will go LOW at Empty+7 words.

The Programmable Almost-Empty Flag ($\overline{PAE}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

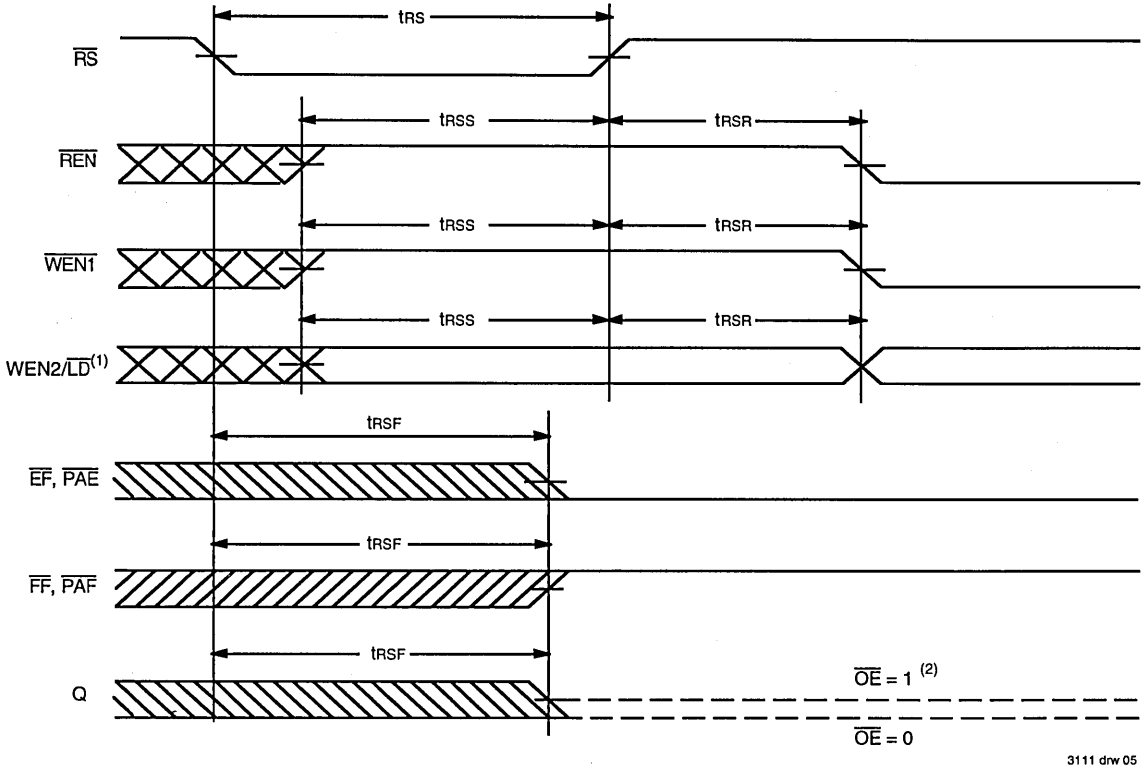
Data Outputs (Q) — Output for serial data.

TABLE 1: STATUS FLAGS

NUMBER OF WORDS IN FIFO						
72423	72203	72213	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	L	H
(n+1) to (64-(m+1))	(n+1) to (256-(m+1))	(n+1) to (512-(m+1))	H	H	H	H
(64-m)[2] to 63	(256-m)[2] to 255	(512-m)[2] to 511	H	L	H	H
64	256	512	L	L	H	H

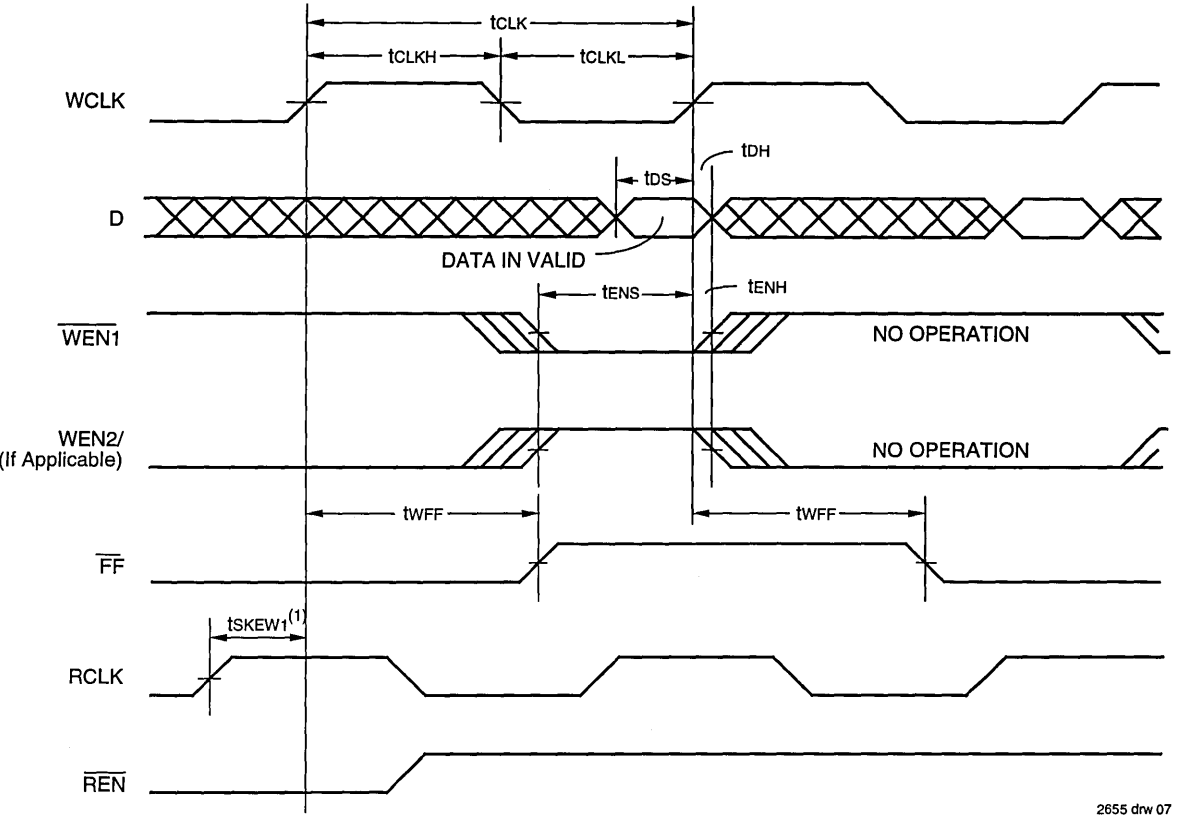
3111 tbl 09

NOTES:
1. n = Empty Offset (n = 7 default value)
2. m = Full Offset (m = 7 default value)



NOTES:
1. Holding WEN2/$\overline{LD}$ HIGH during reset will make the pin act as a second write enable pin. Holding WEN2/$\overline{LD}$ LOW during reset will make the pin act as a load enable for the programmable flag offset registers.
2. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
3. The clocks (RCLK, WCLK) can be free-running during reset.

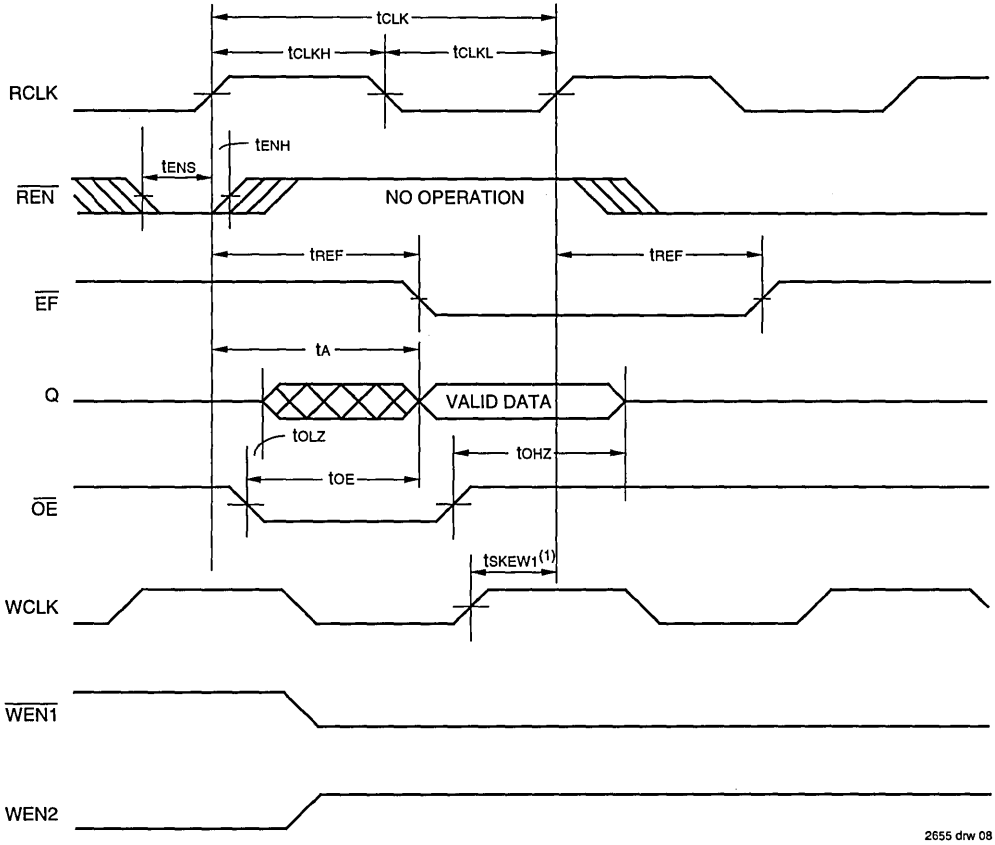
Figure 4. Reset Timing



NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 5. Write Cycle Timing

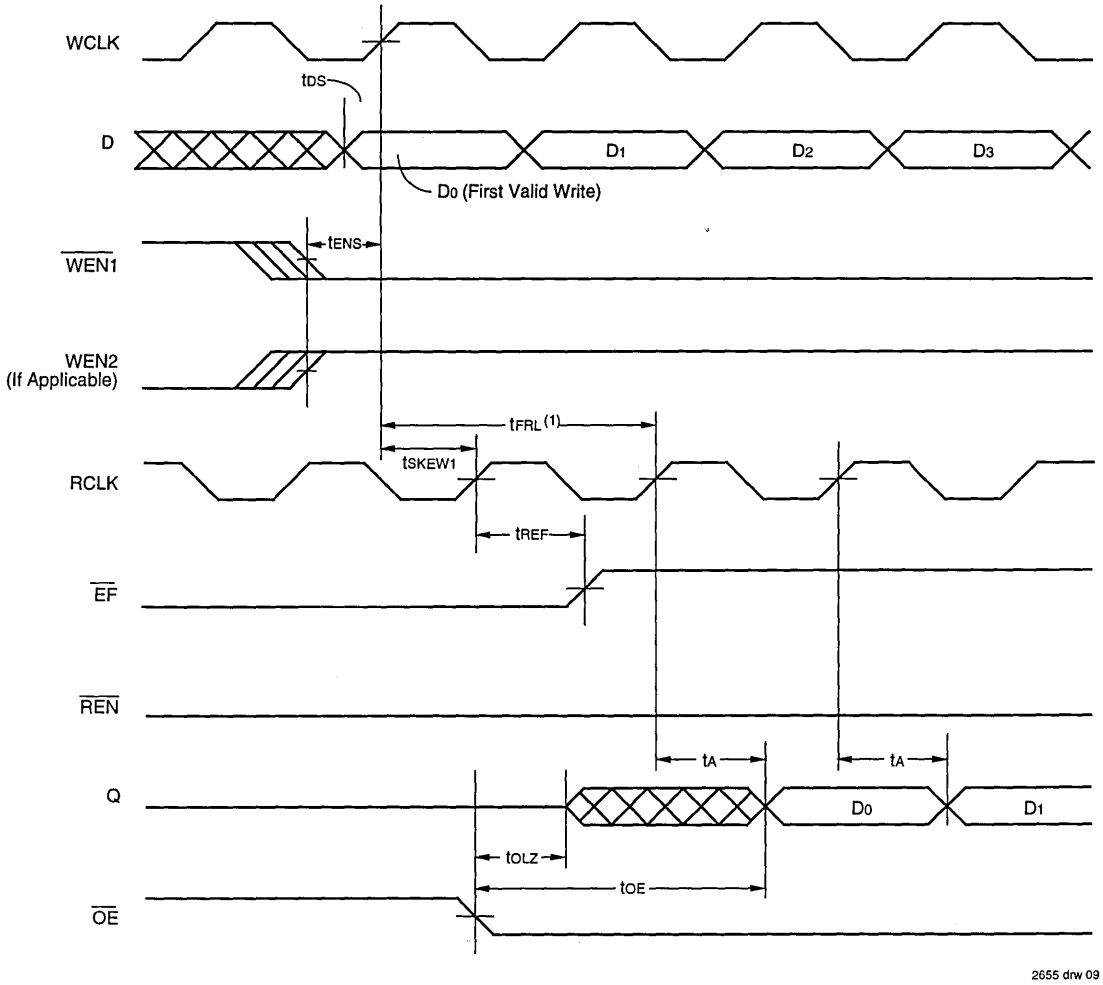
5



Note:

1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge. Figure 6. Read Cycle - Timing

Figure 6. Read Cycle Timing



Note:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = t_{CLK} + t_{SKEW1}$
   When $t_{SKEW1} <$ minimum specification, $t_{FRL} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 7. First Data Word Latency Timing

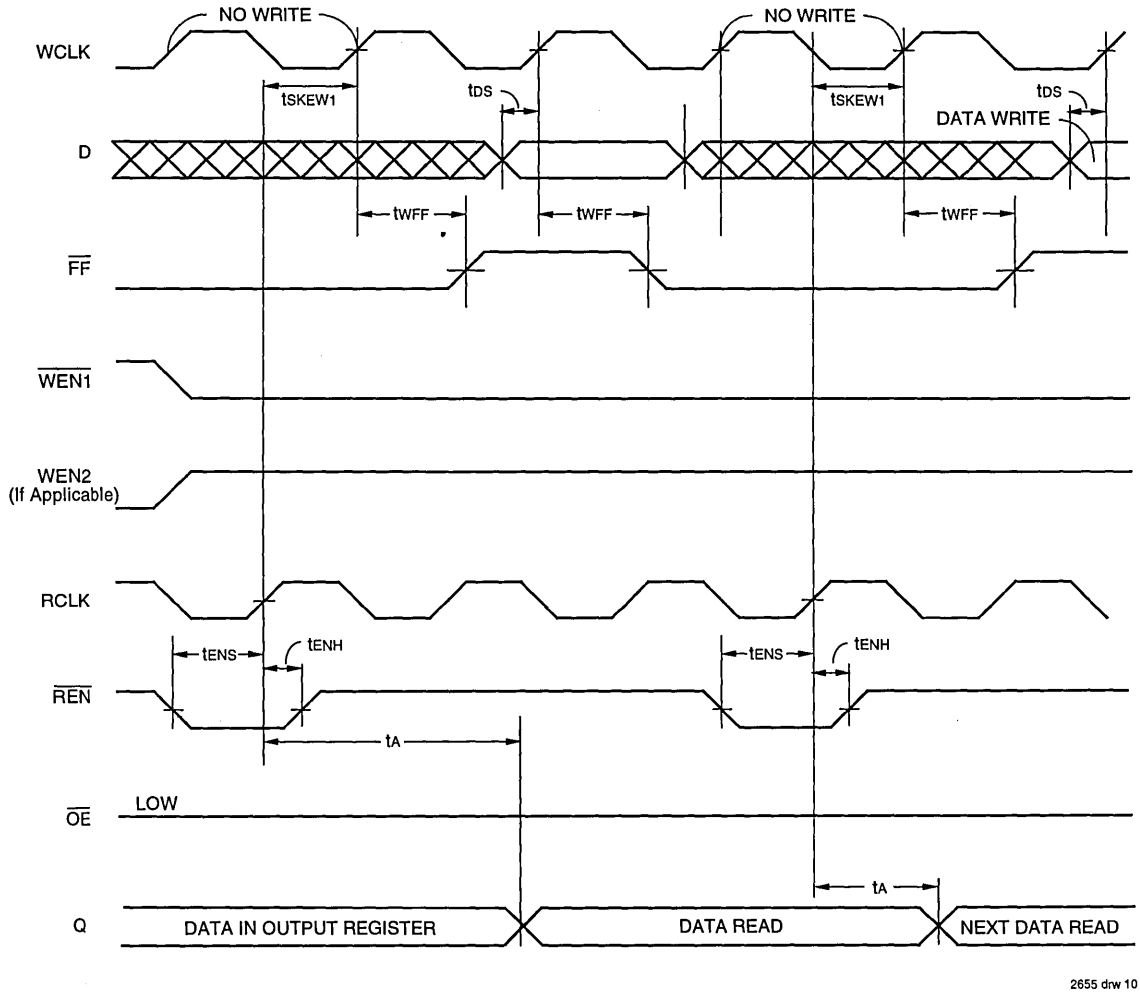
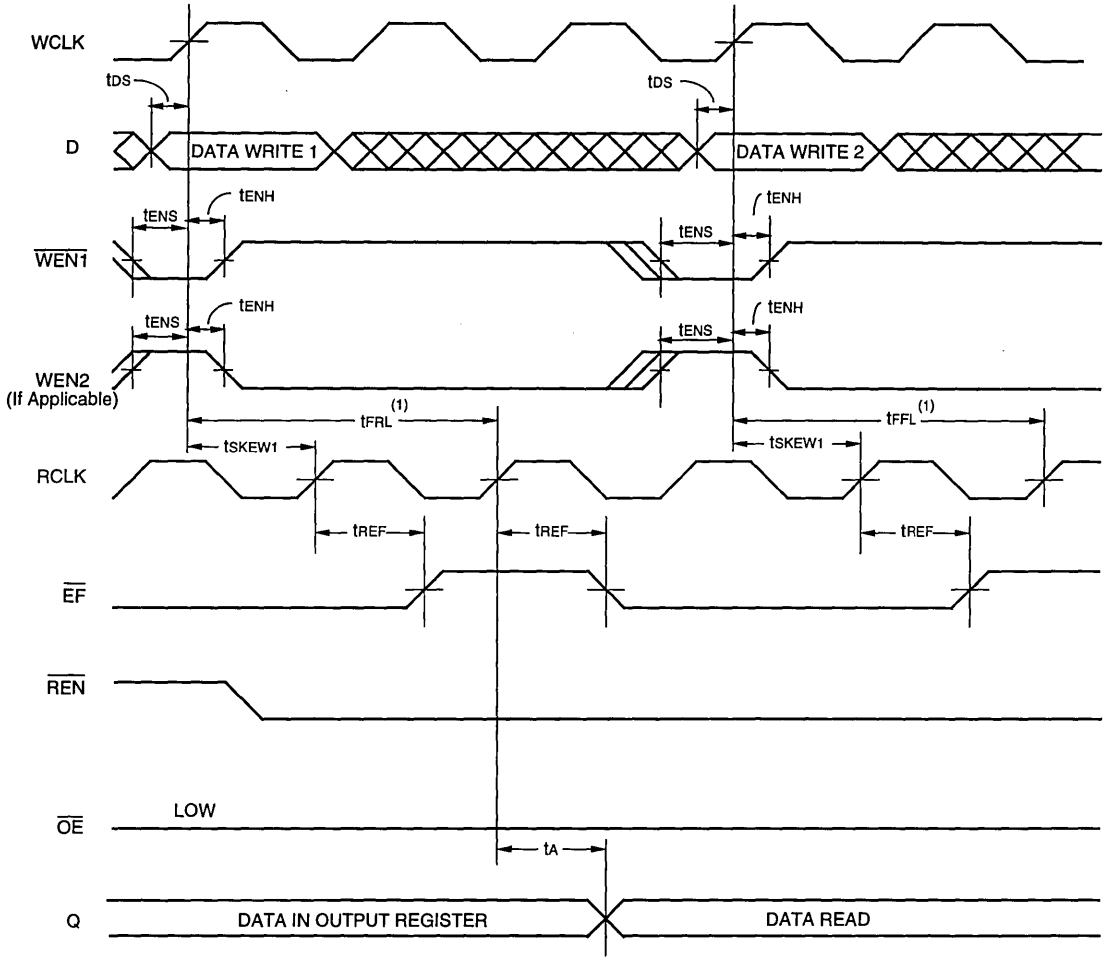


Figure 8. Full Flag Timing

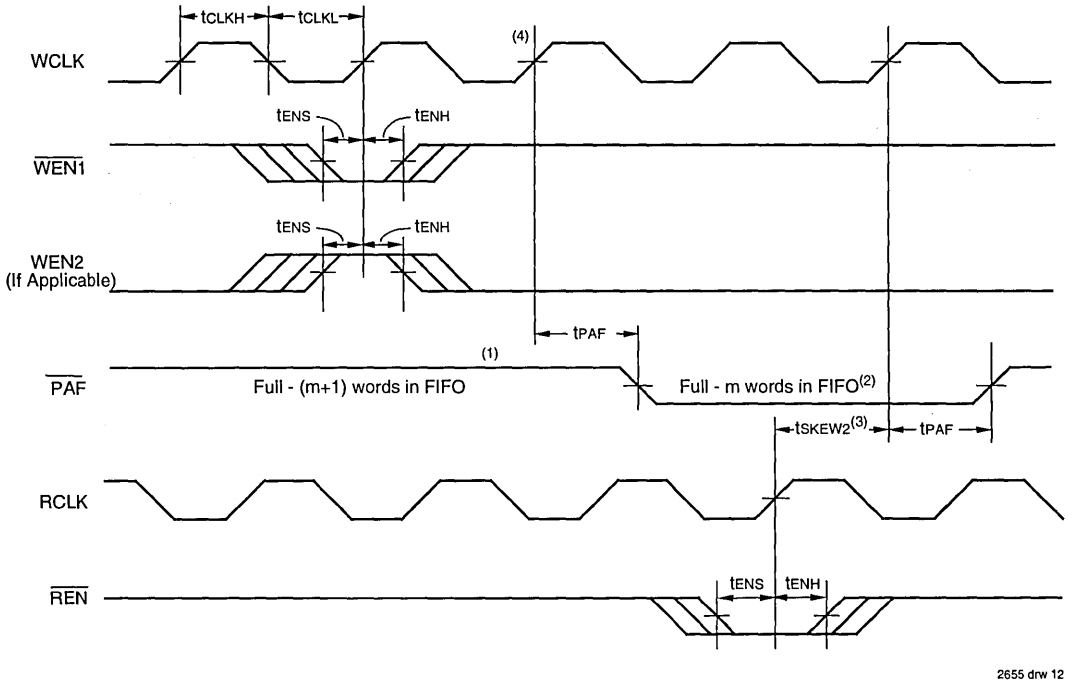


2655 drw 11

Note:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   When $t_{SKEW1} <$ minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at at the Empty Boundary ($\overline{EF}$ = LOW).

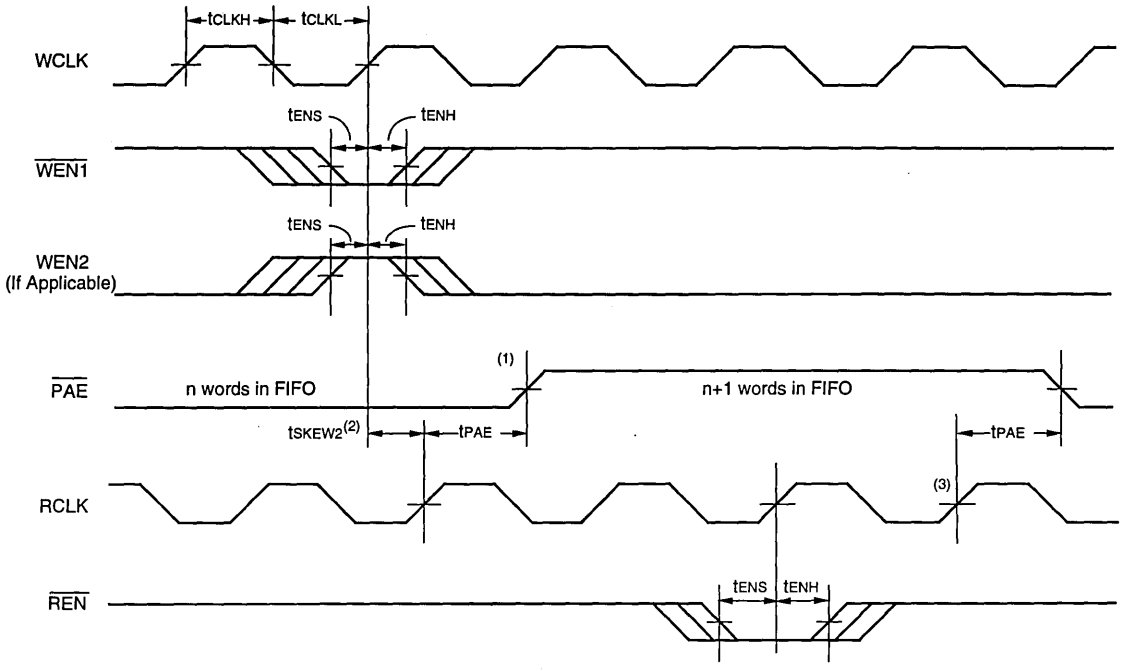
Figure 9. Empty Flag Timing

5



NOTES:
1. PAF offset = m.
2. 64 - m words in for IDT72423, 256 - m words in FIFO for IDT72203, 512 - m words for IDT72213.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK rising edge.
4. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words in the FIFO when $\overline{PAF}$ goes LOW.

Figure 10. Programmable Full Flag Timing



NOTES:
1. PAE offset = n.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to change during that clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK rising edge.
3. If a read is performed on this rising edge of the read clock, there will be Empty + (n-1) words in the FIFO when $\overline{PAE}$ goes LOW.

Figure 11. Programmable Empty Flag Timing

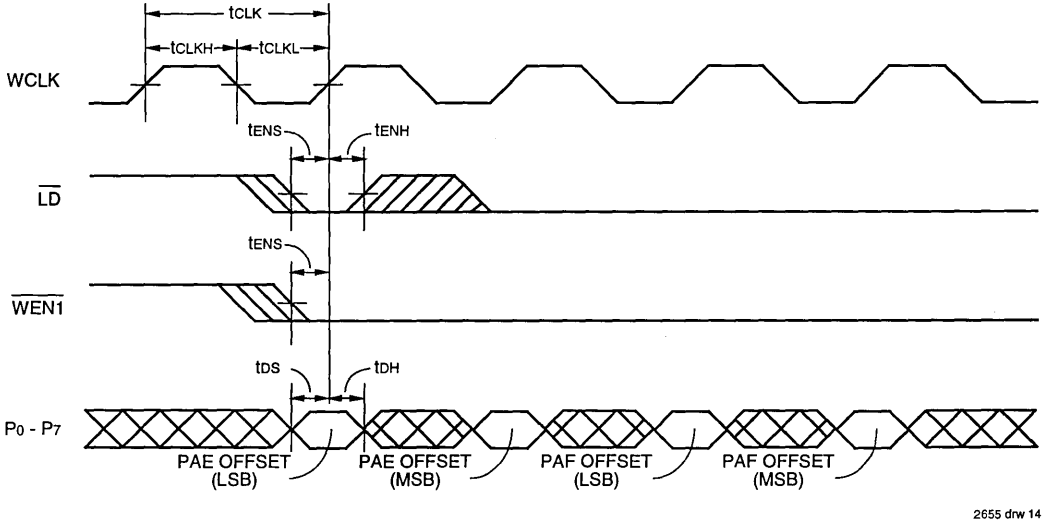


Figure 12. Write Offset Registers Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION—A single IDT72423/72203/72213 may be used when the application requirements are for 64/256/512 bits or less. In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

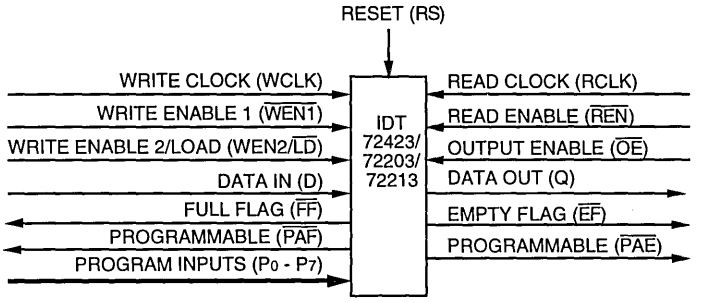


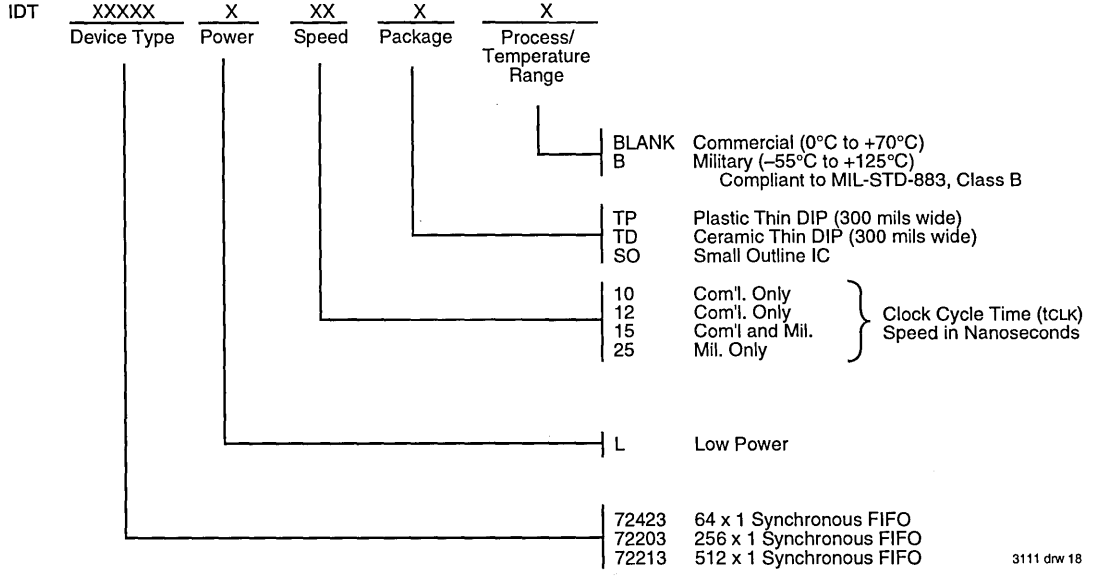
Figure 14. Block Diagram of Single 64 x 1/256 x 1/512 x 1 Synchronous FIFO

DEPTH EXPANSION—The IDT72423/72203/72213 can be adapted to applications when the requirements are for greater than 64/256/512 words. The existence of two enable pins on the write port facilitates depth expansion. The Write Enable 2/Load pin is used as a second write enable in a depth expansion configuration thus the Programmable flags are set to the default values. Two read enables can be created by adding a two-input AND gate to the $\overline{REN}$ line of the FIFO. Depth expansion is possible by using one enable input for system control while the other enable input is controlled by expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data access from one device to the next in a sequential manner. The IDT72423/72203/72213 operates in the Depth Expansion configuration when the following conditions are met:

1. The WEN2/$\overline{LD}$ pin is held HIGH during Reset so that this pin operates a second Write Enable.
2. An external two-input AND gate is used to create two read enables, $\overline{REN1}$ and $\overline{REN2}$. The output of the AND gate is tied to the $\overline{REN}$ pin of the FIFO device, one input of the AND gate is designated $\overline{REN1}$, the other $\overline{REN2}$.
3. External logic is used to control the flow of data.

Please see the Application Note "Depth Expansion of IDT's Synchronous FIFOs Using the Ring Counter Approach" for details of this configuration.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS SyncFIFO™ 64 x 8, 256 x 8, 512 x 8, 1024 x 8, 2048 x 8 and 4096 x 8

IDT72420 IDT72200 IDT72210 IDT72220 IDT72230 IDT72240

FEATURES:

- 64 x 8-bit organization (IDT72420)
- 256 x 8-bit organization (IDT72200)
- 512 x 8-bit organization (IDT72210)
- 1024 x 8-bit organization (IDT72220)
- 2048 x 8-bit organization (IDT72230)
- 4096 x 8-bit organization (IDT72240)
- 12 ns read/write cycle time (IDT72420/72200/72210)
- 15 ns read/write cycle time (IDT72220/72230/72240)
- Read and write clocks can be asynchronous or coincidental
- Dual-Ported zero fall-through time architecture
- Empty and Full flags signal FIFO status
- Almost-empty and almost-full flags set to Empty+7 and Full-7, respectively
- Output enable puts output data bus in high-impedance state
- Produced with advanced submicron CMOS technology
- Available in 28-pin 300 mil plastic DIP and 300 mil ceramic DIP
- For surface mount product please see the IDT72421/72201/72211/72221/72231/72241 data sheet
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72420/72200/72210/72220/72230/72240 SyncFIFO™ are very high-speed, low-power First-In, First-Out (FIFO) memories with clocked read and write controls. The IDT72420/72200/72210/72220/72230/72240 have a 64, 256, 512, 1024, 2048, and 4096 x 8-bit memory array, respectively. These FIFOs are applicable for a wide variety of data buffering needs, such as graphics, Local Area Networks (LANs), and interprocessor communication.

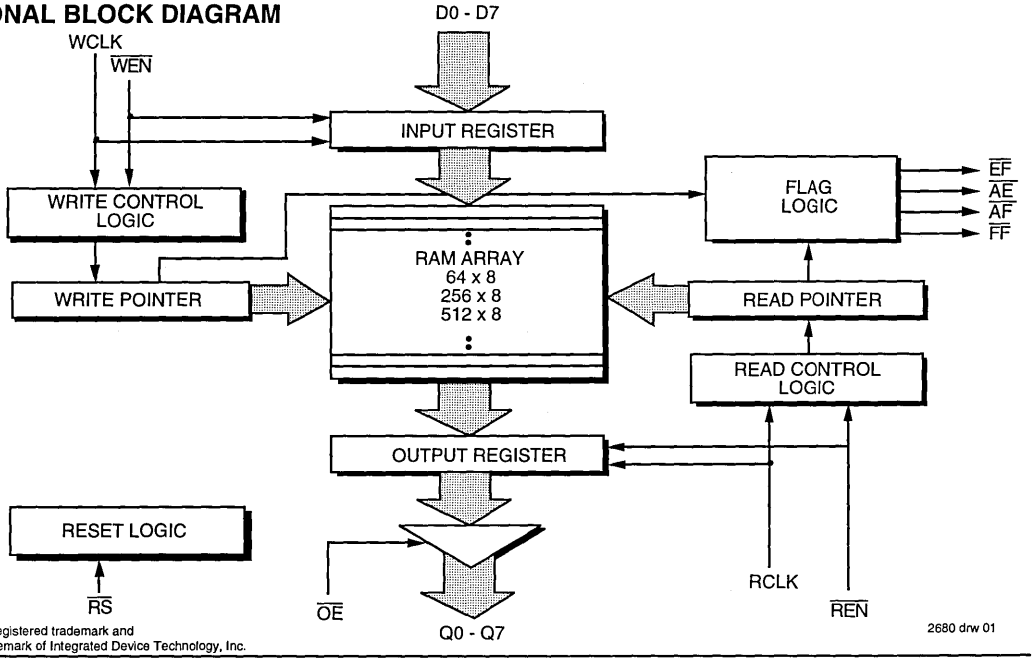
These FIFOs have 8-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and a write enable pin ($\overline{WEN}$). Data is written into the Synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and a read enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

These Synchronous FIFOs have two end-point flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$). Two partial flags, Almost-Empty ($\overline{AE}$) and Almost-Full ($\overline{AF}$), are provided for improved system control. The partial ($\overline{AE}$) flags are set to Empty+7 and Full-7 for $\overline{AE}$ and $\overline{AF}$ respectively.

The IDT72420/72200/72210/72220/72230/72240 are fabricated using IDT's high-speed submicron CMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

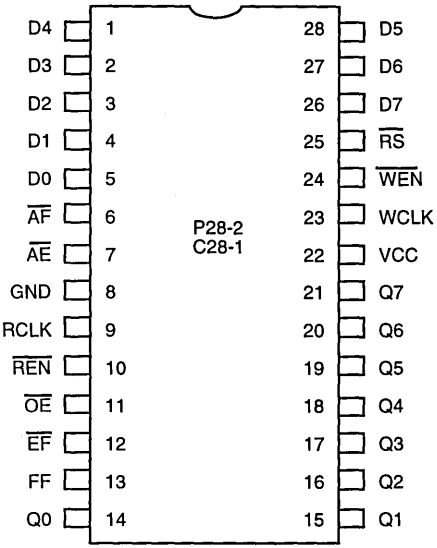
5

FUNCTIONAL BLOCK DIAGRAM



2680 drw 01

PIN CONFIGURATION



DIP TOP VIEW

2680 drw 02

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_0 - D_7	Data Inputs	I	Data inputs for a 8-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{AF}$ go HIGH, and $\overline{AE}$ and $\overline{EF}$ go LOW. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when $\overline{WEN}$ is asserted.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
Q_0 - Q_7	Data Outputs	O	Data outputs for a 8-bit bus.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when $\overline{REN}$ is asserted.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high-impedance state.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited., When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{AE}$	Almost-Empty Flag	O	When $\overline{AE}$ is LOW, the FIFO is almost empty based on the offset Empty+7. $\overline{AE}$ is synchronized to RCLK.
$\overline{AF}$	Almost-Full Flag	O	When $\overline{AF}$ is LOW, the FIFO is almost full based on the offset Full-7. $\overline{AF}$ is synchronized to WCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
Vcc	Power		One +5 volt power supply pin.
GND	Ground		One 0 volt ground pin.

2680 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to + 7.0	–0.5 to + 7.0	V
T_A	Operating Temperature	0 to + 70	–55 to + 125	°C
T_{BIAS}	Temperature Under Bias	–55 to + 125	–65 to + 135	°C
T_{STG}	Storage Temperature	–55 to + 125	–65 to + 135	°C
I_{OUT}	DC Output Current	50	50	mA

2680 tbl 02

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}	Input Low Voltage Commercial & Military	—	—	0.8	V

2680 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1, 2)	Output Capacitance	V_{OUT} = 0V	10	pF

2680 tbl 04

NOTES:

1. With output deselected. ($\overline{OE}$ = HIGH)
2. Characterized values, not currently tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72420 IDT72200 IDT72210 Commercial t_{CLK} = 12, 15, 20, 25, 35, 50 ns Min.	Typ.	Max.	IDT72420 IDT72200 IDT72210 Military t_{CLK} = 20, 25,35, 50 ns Min.	Typ.	Max.	Units
I_{LI}(1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	—	140	—	—	160	mA

2680 tbl 05

Symbol	Parameter	IDT72220 IDT72230 IDT72240 Commercial t_{CLK} = 15, 20, 25, 35, 50 ns Min.	Typ.	Max.	IDT72220 IDT72230 IDT72240 Military t_{CLK} = 25, 35, 50 ns Min.	Typ.	Max.	Units
I_{LI}(1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1}(4)	Active Power Supply Current	—	—	160	—	—	180	mA

2680 tbl 06

NOTES:

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.

3 & 4. Measurements are made with outputs open. Tested at f_{CLK} = 20 MHz.
(3) Typical I_{CC1} = 65 + (f_{CLK} * 1.1/MHz) + (f_{CLK} * C_L * 0.03/MHz-pF) mA
(4) Typical I_{CC1} = 80 + (f_{CLK} * 2.1/MHz) + (f_{CLK} * C_L * 0.03/MHz-pF) mA
f_{CLK} = 1 / t_{CLK}
C_L = external capacitive load (30 pF typical)

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Commercial				Commercial & Military										
		72200L12 72210L12 72420L12		72200L15 72210L15 72420L15		72200L20 72210L20 72420L20		72200L25 72210L25 72420L25		72200L35 72210L35 72420L35		72200L50 72210L50 72420L50		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
fS	Clock Cycle Frequency	—	83.3	—	66.7	—	50	—	40	—	28.6	—	20	MHz
tA	Data Access Time	2	8	2	10	2	12	3	15	3	20	3	25	ns
tCLK	Clock Cycle Time	12	—	15	—	20	—	25	—	35	—	50	—	ns
tCLKH	Clock High Time	5	—	6	—	8	—	10	—	14	—	20	—	ns
tCLKL	Clock Low Time	5	—	6	—	8	—	10	—	14	—	20	—	ns
tDS	Data Set-up Time	3	—	4	—	5	—	6	—	8	—	10	—	ns
tDH	Data Hold Time	0.5	—	1	—	1	—	1	—	2	—	2	—	ns
tENS	Enable Set-up Time	3	—	4	—	5	—	6	—	8	—	10	—	ns
tENH	Enable Hold Time	0.5	—	1	—	1	—	1	—	2	—	2	—	ns
tRS	Reset Pulse Width[1]	12	—	15	—	20	—	25	—	35	—	50	—	ns
tRSS	Reset Set-up Time	12	—	15	—	20	—	25	—	35	—	50	—	ns
tRSR	Reset Recovery Time	12	—	15	—	20	—	25	—	35	—	50	—	ns
tRSF	Reset to Flag and Output Time	—	12	—	15	—	20	—	25	—	35	—	50	ns
tOLZ	Output Enable to Output in Low-Z[2]	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	7	3	8	3	10	3	13	3	15	3	28	ns
tOHZ	Output Enable to Output in High-Z[2]	3	7	3	8	3	10	3	13	3	15	3	28	ns
tWFF	Write Clock to Full Flag	—	8	—	10	—	12	—	15	—	20	—	30	ns
tREF	Read Clock to Empty Flag	—	8	—	10	—	12	—	15	—	20	—	30	ns
tAF	Write Clock to Almost-Full Flag	—	8	—	10	—	12	—	15	—	20	—	30	ns
tAE	Read Clock to Almost-Empty Flag	—	8	—	10	—	12	—	15	—	20	—	30	ns
tSKEW1	Skew time between Read Clock & Write Clock for Empty Flag & Full Flag	5	—	6	—	8	—	10	—	12	—	15	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Almost-Full Flag	22	—	28	—	35	—	40	—	42	—	45	—	ns

NOTES:

1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

2680 tbl 07

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	Commercial				Commercial & Military						Unit
		72220L15 72230L15 72240L15		72220L20 72230L20 72240L20		72220L25 72230L25 72240L25		72220L35 72230L35 72240L35		72220L50 72230L50 72240L50		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Clock Cycle Frequency	—	66.7	—	50	—	40	—	28.6	—	20	MHz
t_A	Data Access Time	2	10	2	12	3	15	3	20	3	25	ns
t_{CLK}	Clock Cycle Time	15	—	20	—	25	—	35	—	50	—	ns
t_{CLKH}	Clock High Time	6	—	8	—	10	—	14	—	20	—	ns
t_{CLKL}	Clock Low Time	6	—	8	—	10	—	14	—	20	—	ns
t_{DS}	Data Set-up Time	4	—	5	—	6	—	8	—	10	—	ns
t_{DH}	Data Hold Time	1	—	1	—	1	—	2	—	2	—	ns
t_{ENS}	Enable Set-up Time	4	—	5	—	6	—	8	—	10	—	ns
t_{ENH}	Enable Hold Time	1	—	1	—	1	—	2	—	2	—	ns
t_{RS}	Reset Pulse Width[1]	15	—	20	—	25	—	35	—	50	—	ns
t_{RSS}	Reset Set-up Time	15	—	20	—	25	—	35	—	50	—	ns
t_{RSR}	Reset Recovery Time	15	—	20	—	25	—	35	—	50	—	ns
t_{RSF}	Reset to Flag and Output Time	—	15	—	20	—	25	—	35	—	50	ns
t_{OLZ}	Output Enable to Output in Low-Z[2]	0	—	0	—	0	—	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid	3	8	3	10	3	13	3	15	3	23	ns
t_{OHZ}	Output Enable to Output in High-Z[2]	3	8	3	10	3	13	3	15	3	23	ns
t_{WFF}	Write Clock to Full Flag	—	10	—	12	—	15	—	20	—	30	ns
t_{REF}	Read Clock to Empty Flag	—	10	—	12	—	15	—	20	—	30	ns
t_{AF}	Write Clock to Almost-Full Flag	—	10	—	12	—	15	—	20	—	30	ns
t_{AE}	Read Clock to Almost-Empty Flag	—	10	—	12	—	15	—	20	—	30	ns
t_{SKEW1}	Skew time between Read Clock & Write Clock for Empty Flag & Full Flag	6	—	8	—	10	—	12	—	15	—	ns
t_{SKEW2}	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Almost-Full Flag	28	—	35	—	40	—	42	—	45	—	ns

NOTES:

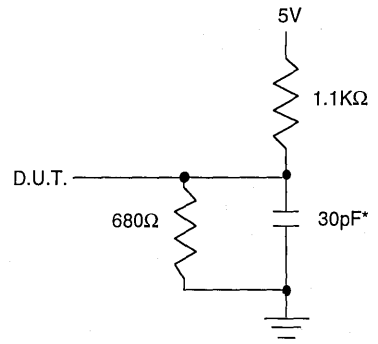
2680 tbl 08

1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2680 tbl 09



2680 drw 03

or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

Data In (D_0–D_7) — Data inputs for 8-bit wide data.

CONTROLS:

Reset ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The Full Flag ($\overline{FF}$) and Almost Full Flag ($\overline{AF}$) will be reset to HIGH after t_{RSF}. The Empty Flag ($\overline{EF}$) and Almost Empty Flag ($\overline{AE}$) will be reset to LOW after t_{RSF}. During reset, the output register is initialized to all zeros.

Write Clock (WCLK) — A write cycle is initiated on the LOW-to-HIGH transition of the write clock (WCLK). Data set-up and hold times must be met in respect to the LOW-to-HIGH transition of the write clock (WCLK). The Full Flag ($\overline{FF}$) and Almost Full Flag ($\overline{AF}$) are synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

Write Enable ($\overline{WEN}$) — When Write Enable ($\overline{WEN}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

When Write Enable ($\overline{WEN}$) is HIGH, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go HIGH after t_{WFF}, allowing a valid write to begin. Write Enable ($\overline{WEN}$) is ignored when the FIFO is full.

Read Clock (RCLK) — Data can be read on the outputs on the LOW-to-HIGH transition of the read clock (RCLK). The Empty Flag ($\overline{EF}$) and Almost-Empty Flag ($\overline{AE}$) are synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

The write and read clocks can be asynchronous or coincident.

Read Enable ($\overline{REN}$) — When Read Enable ($\overline{REN}$) is LOW, data is read from the RAM array to the output register on the LOW-to-HIGH transition of the read clock (RCLK).

When Read Enable ($\overline{REN}$) is HIGH, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{REF} and a valid read can begin. Read Enable ($\overline{REN}$) is ignored when the FIFO is empty.

Output Enable ($\overline{OE}$) — When Output Enable ($\overline{OE}$) is enabled (LOW), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (HIGH), the Q output data bus is in a high-impedance state.

OUTPUTS:

Full Flag ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operation, when the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 64 writes for the IDT72420, 256 writes for the IDT72200, 512 writes for the IDT72210, 1024 writes for the IDT72220, 2048 writes for the IDT72230, and 4096 writes for the IDT72240.

The Full Flag ($\overline{FF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Empty Flag ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Almost Full Flag ($\overline{AF}$) — The Almost Full Flag ($\overline{AF}$) will go LOW when the FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the Almost Full Flag ($\overline{AF}$) will go LOW after 57 writes for the IDT72420, 249 writes for the IDT72200, 505 writes for the IDT72210, 1017 writes for the IDT72220, 2041 writes for the IDT72230 and 4089 writes for the IDT72240.

The Almost Full Flag ($\overline{AF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Almost Empty Flag ($\overline{AE}$) — The Almost Empty Flag ($\overline{AE}$) will go LOW when the FIFO reaches the Almost-Empty condition. If no reads are performed after Reset ($\overline{RS}$), the Almost Empty Flag ($\overline{AE}$) will go HIGH after 8 writes for the IDT72420, IDT72200, IDT72210, IDT72220, IDT72230 and IDT72240.

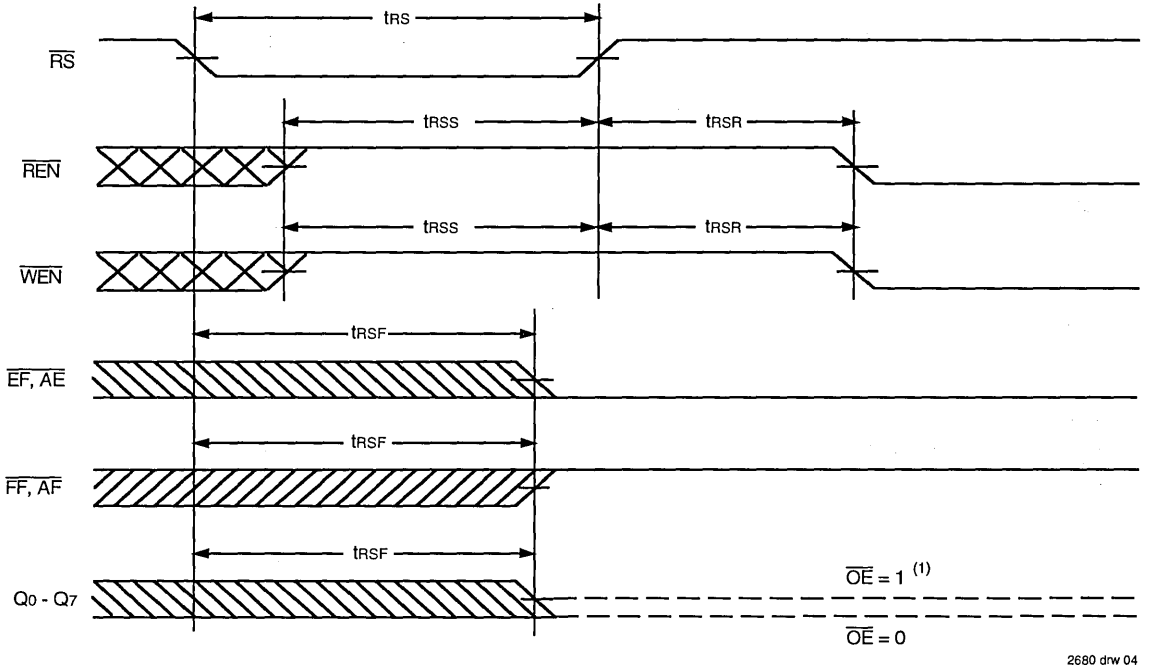
The Almost Empty Flag ($\overline{AE}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Data Outputs (Q_0–Q_7) — Data outputs for a 8-bit wide data.

TABLE 1: STATUS FLAGS

Number of Words in FIFO						$\overline{FF}$	$\overline{AF}$	$\overline{AE}$	$\overline{EF}$
IDT72420	IDT72200	IDT72210	IDT72220	IDT72230	IDT72240				
0	0	0	0	0	0	H	H	L	L
1 to 7	1 to 7	1 to 7	1 to 7	1 to 7	1 to 7	H	H	L	H
8 to 56	8 to 248	8 to 504	8 to 1016	8 to 2040	8 to 4088	H	H	H	H
57 to 63	249 to 255	505 to 511	1017 to 1023	2041 to 2047	4089 to 4095	H	L	H	H
64	256	512	1024	2048	4096	L	L	H	H

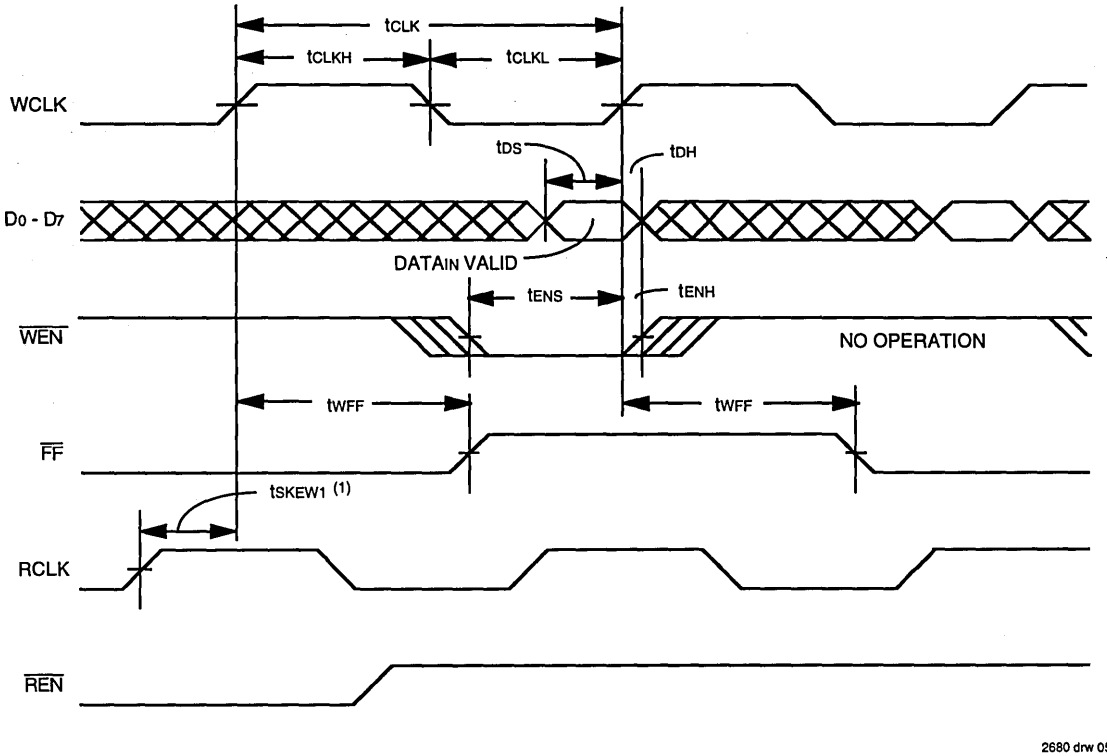
2680 tbl 10



2680 drw 04

NOTE:
1. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

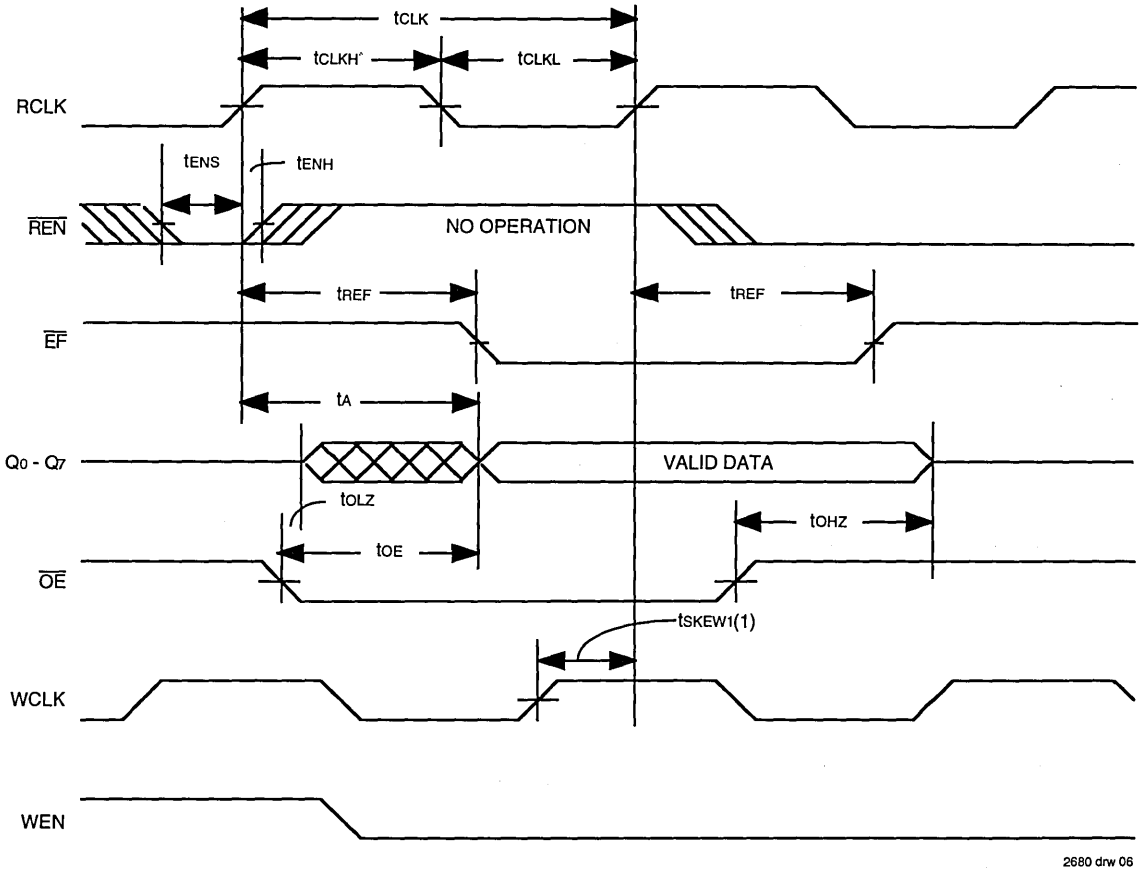
Figure 2. Reset Timing



2680 drw 05

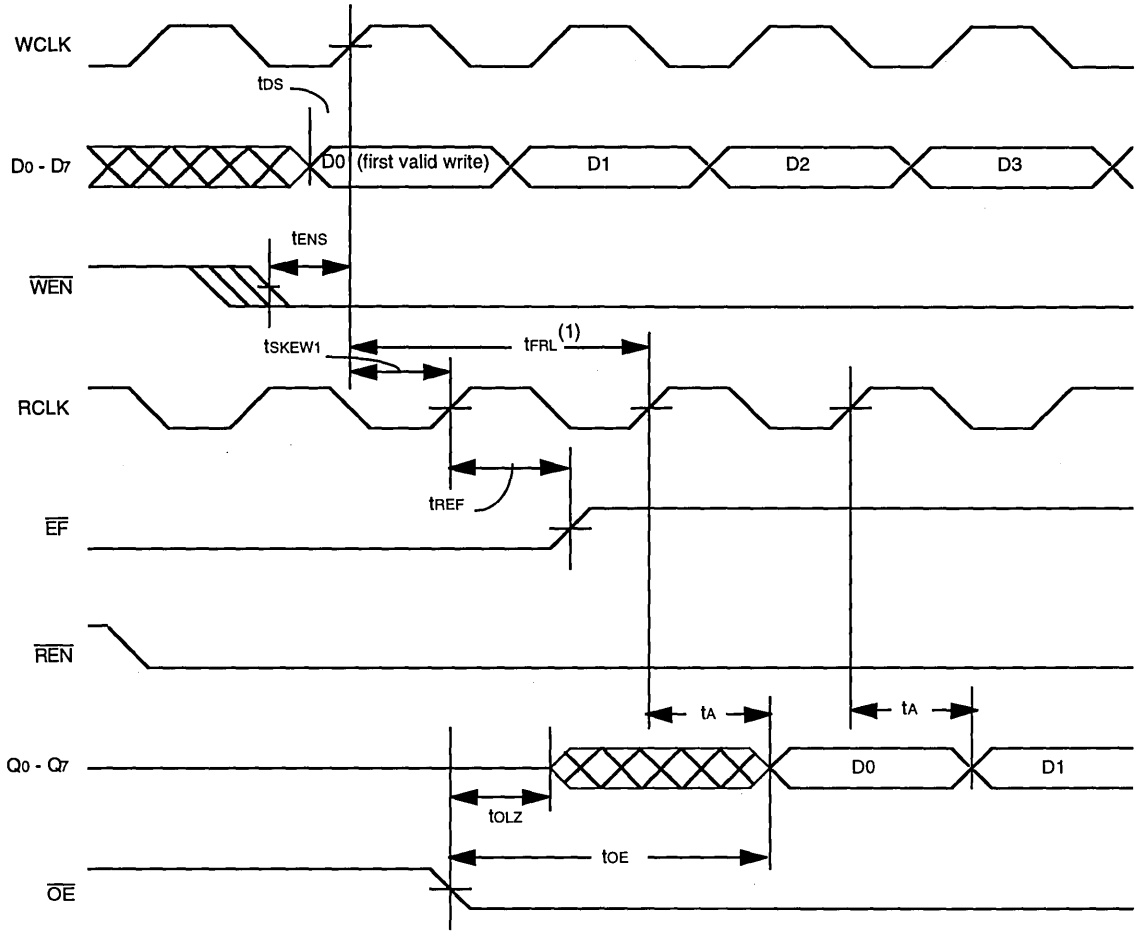
NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the curent clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

Figure 3. Write Cycle Timing



NOTE:
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change during the curent clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 4. Read Cycle Timing



NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timing apply only at the Empty Boundry ($\overline{EF}$ = LOW).

2680 drw 07

Figure 5. First Data Word Latency Timing

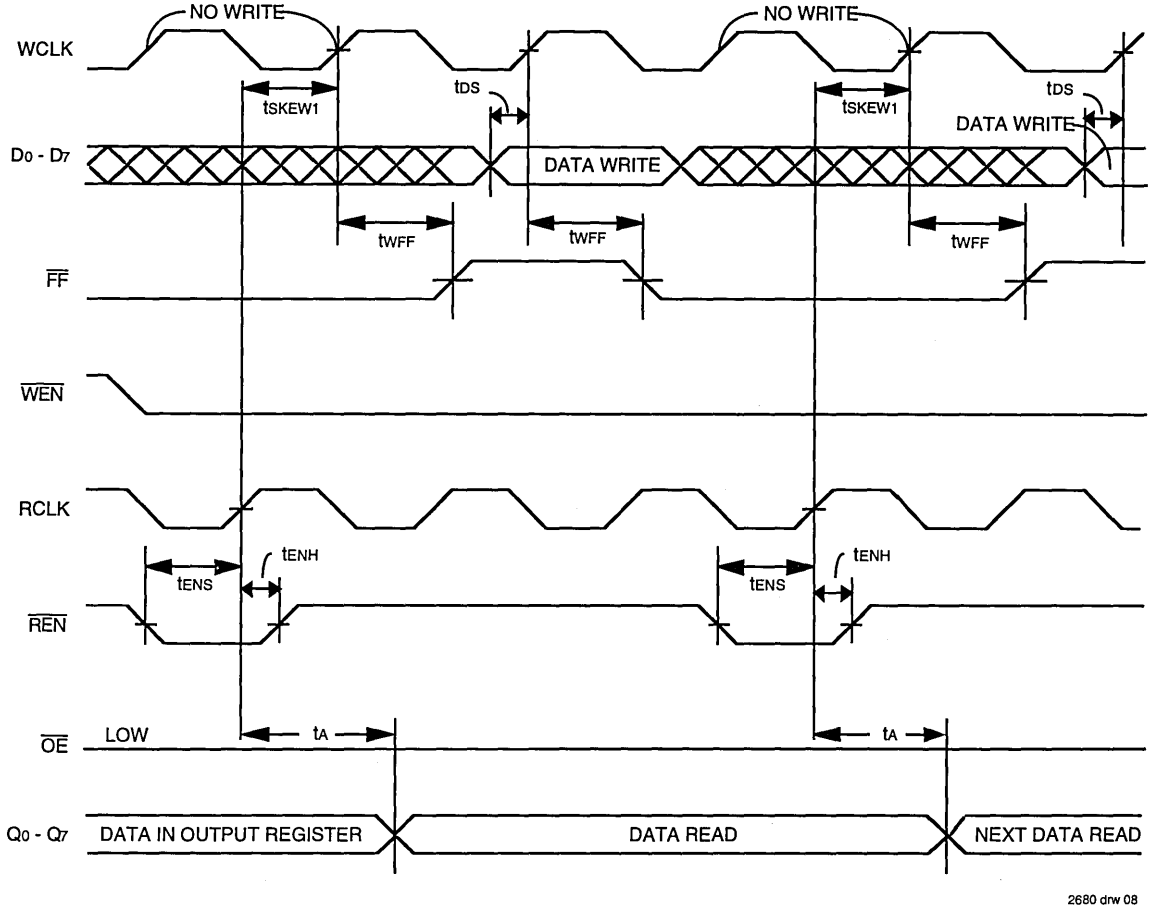
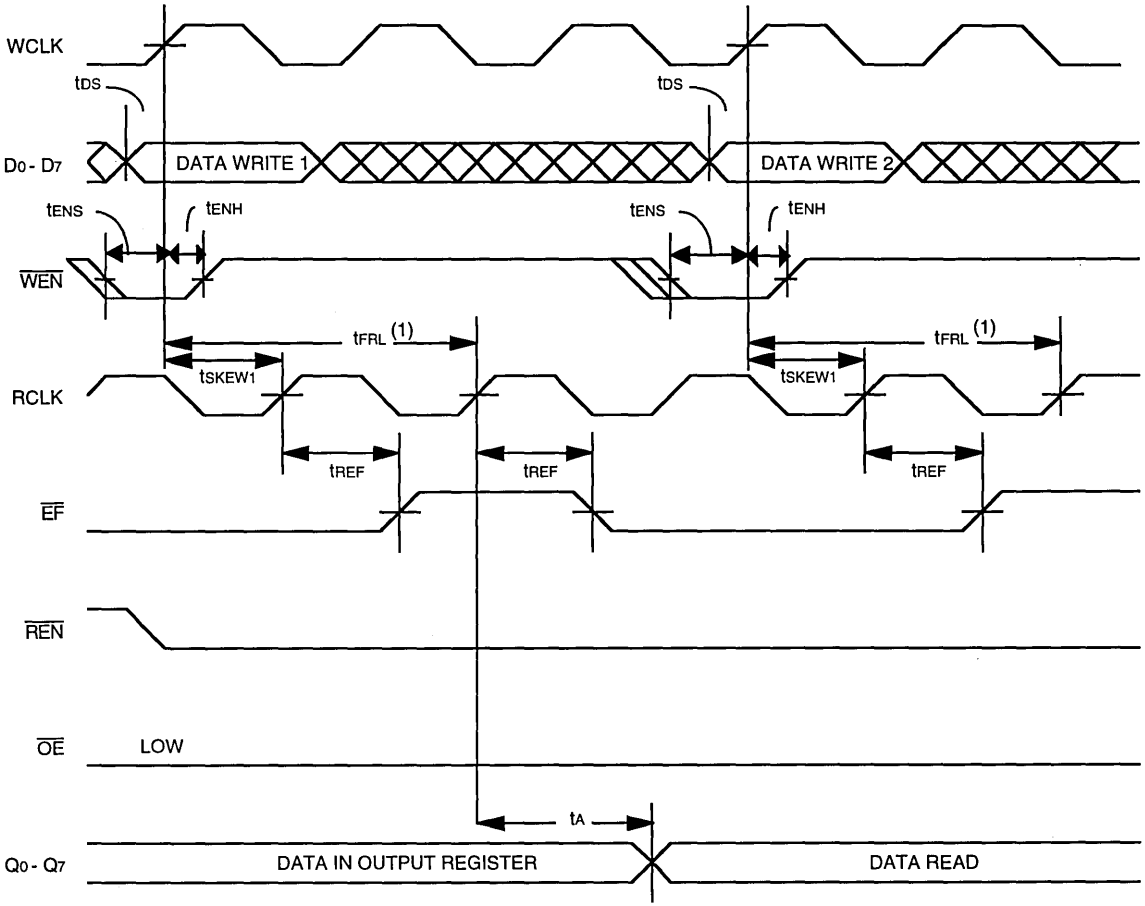


Figure 6. Full Flag Timing

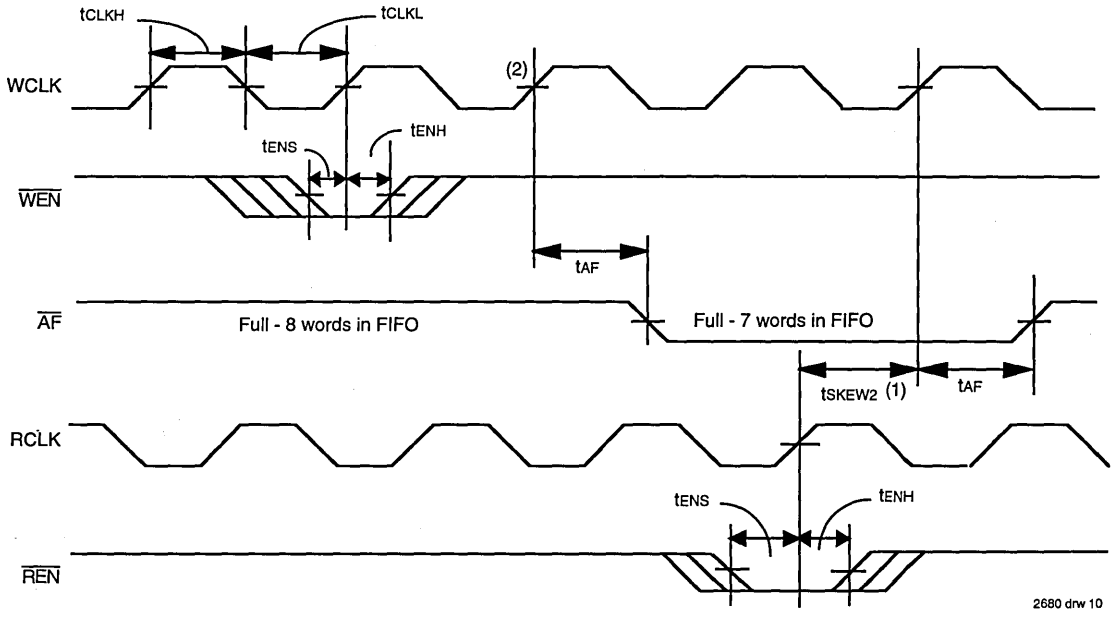


NOTE:

1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timing apply only at the Empty Boundry ($\overline{EF}$ = LOW).

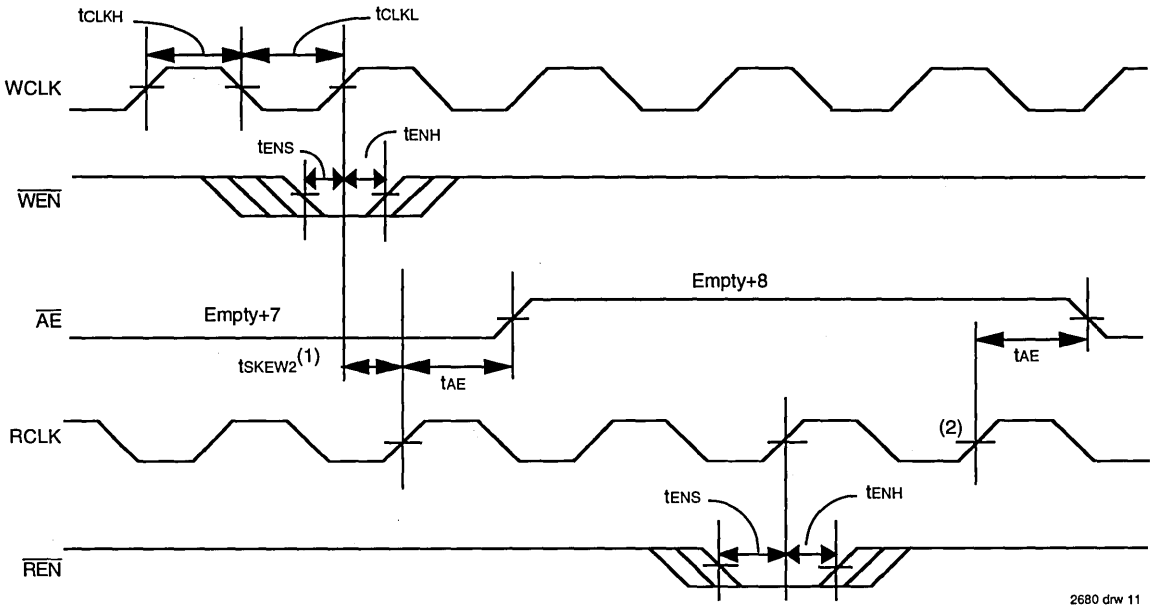
2680 drw 09

Figure 7. Empty Flag Timing



NOTES:
1. tSKEW2 is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{AF}$ to change during the curent clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW2, then $\overline{AF}$ may not change state until the next WCLK edge.
2. If a write is performed on this rising edge of the write clock, there will be Full - 6 words in the FIFO when $\overline{AF}$ goes LOW.

Figure 8. Almost Full Flag Timing



NOTES:
1. tSKEW2 is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{AE}$ to change during the curent clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than tSKEW2, then $\overline{AE}$ may not change state until the next RCLK edge.
2. If a read is performed on this rising edge of the read clock, there will be Empty - 6 words in the FIFO when $\overline{AE}$ goes LOW.

Figure 9. Almost Empty Flag Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION - A single IDT72420/72200/72210/72220/72230/72240 may be used when the application requirements are for 64/256/512/1024/2048/4096 words or less. See Figure 10.

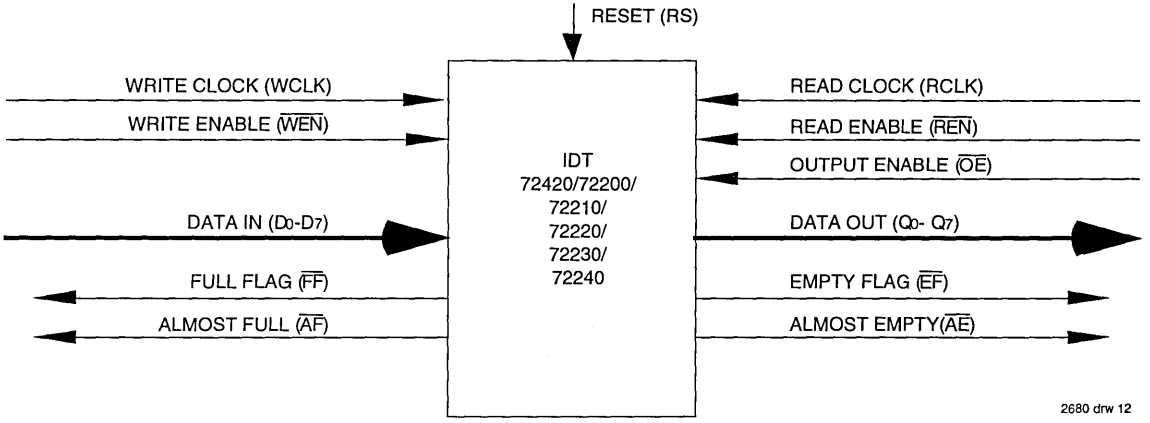


Figure 10. Block Diagram of Single 64 x 8/256 x 8/512 x 8/1024 x 8/2048 x 8/4096 x 8 Synchronous FIFO

5

WIDTH EXPANSION CONFIGURATION - Word width may be increased simply by connecting the corresponding input control signals of multiple devices. A composite flag should be created for each of the end-point status flags (EF and FF) The partial status flags (AE and AF) can be detected from any one device. Figure 11 demonstrates a 16-bit word width by using two IDT72420/72200/72210/72220/72230/72240s. Any word width can be attained by adding additional IDT72420/72200/72210/72220/72230/72240s.

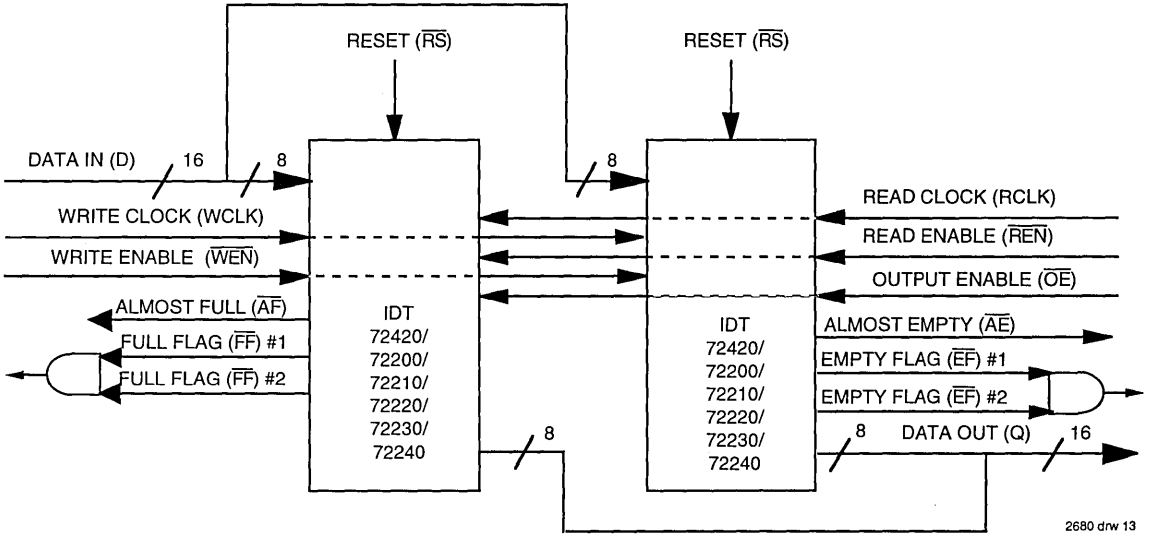
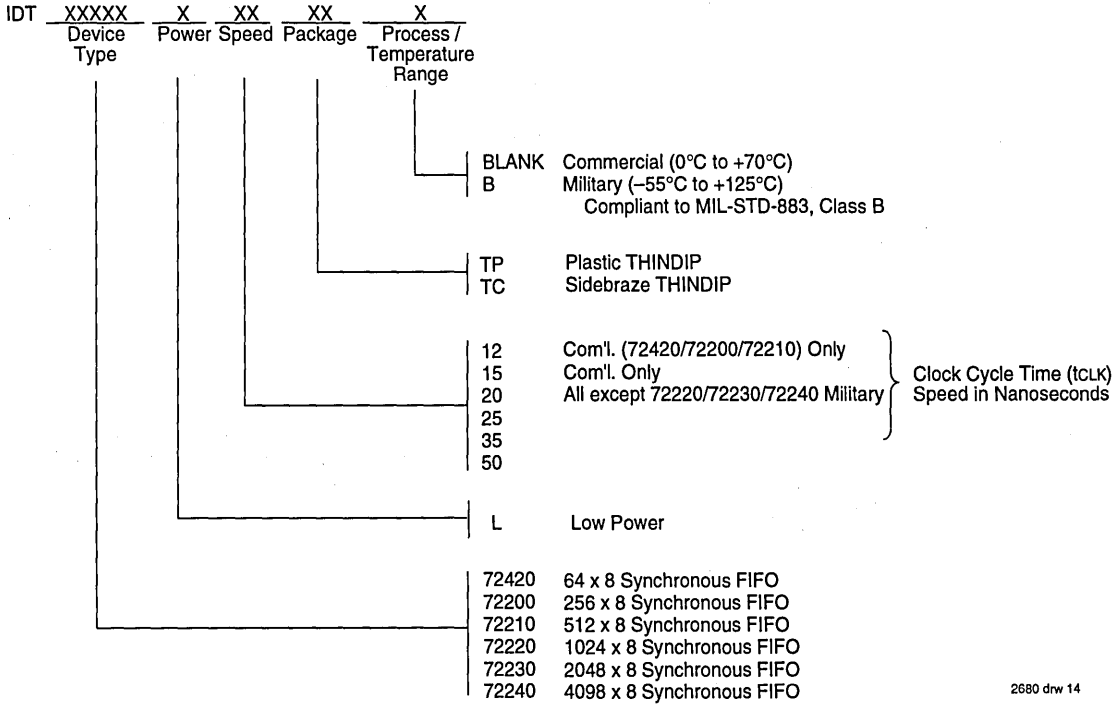


Figure 11. Block Diagram of 64 x 16/256 x 16/512 x 16/1024 x 16/2048 x 16/4096 x 16 Synchronous FIFO Used in a Width Expansion Configuration

DEPTH EXPANSION - The IDT72420/72200/72210/72220/72230/72240 can be adapted to applications when the requirements are for greater than 64/256/512/1024/2048/4096 words. Depth expansion is possible by using expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data accesses from one device to the next in a sequential manner.

Please see the Application Note "DEPTH EXPANSION IDT'S SYNCHRONOUS FIFOs USING RING COUNTER APPROACH" for details of this configuration.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS SyncFIFO™ 64 X 9, 256 x 9, 512 x 9, 1024 X 9, 2048 X 9 and 4096 x 9

IDT72421
IDT72201
IDT72211
IDT72221
IDT72231
IDT72241

FEATURES:

- 64 x 9-bit organization (IDT72421)
- 256 x 9-bit organization (IDT72201)
- 512 x 9-bit organization (IDT72211)
- 1024 x 9-bit organization (IDT72221)
- 2048 x 9-bit organization (IDT72231)
- 4096 x 9-bit organization (IDT72241)
- 12 ns read/write cycle time (IDT72421/72201/72211)
- 15 ns read/write cycle time (IDT72221/72231/72241)
- Read and write clocks can be independent
- Dual-Ported zero fall-through time architecture
- Empty and Full flags signal FIFO status
- Programmable Almost-Empty and Almost-Full flags can be set to any depth
- Programmable Almost-Empty and Almost-Full flags default to Empty+7, and Full-7, respectively
- Output enable puts output data bus in high-impedance state
- Advanced submicron CMOS technology
- Available in 32-pin plastic leaded chip carrier (PLCC) and ceramic leadless chip carrier (LCC)
- For Through-Hole product please see the IDT72420/72200/72210/72220/72230/72240 data sheet
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72421/72201/72211/72221/72231/72241 SyncFIFO™ are very high-speed, low-power First-In, First-Out (FIFO) memories with clocked read and write controls. The IDT72421/72201/72211/72221/72231/72241 have a 64, 256, 512, 1024, 2048, and 4096 x 9-bit memory array, respectively. These FIFOs are applicable for a wide variety of data buffering needs such as graphics, local area networks and interprocessor communication.

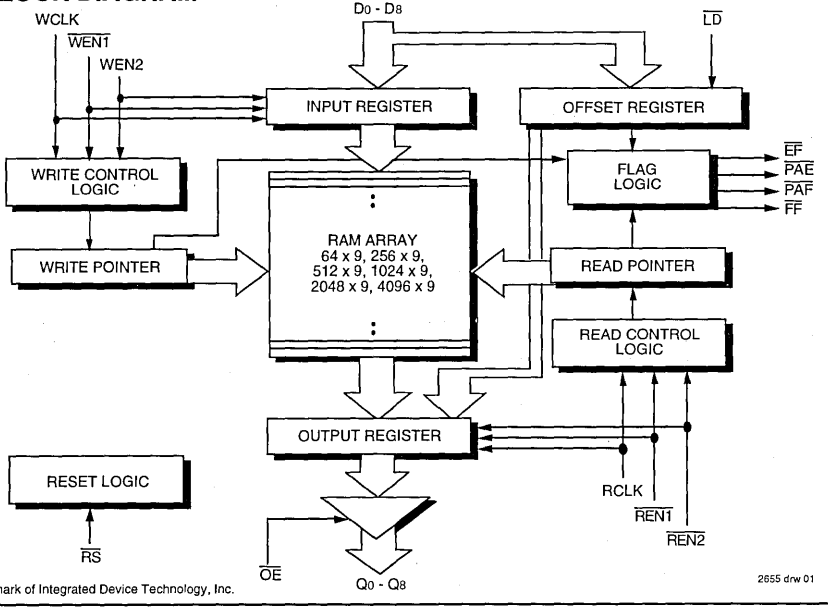
These FIFOs have 9-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and two write enable pins ($\overline{WEN1}$, WEN2). Data is written into the Synchronous FIFO on every rising clock edge when the write enable pins are asserted. The output port is controlled by another clock pin (RCLK) and two read enable pins ($\overline{REN1}$, $\overline{REN2}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual-clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

The Synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$). Two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$), are provided for improved system control. The programmable flags default to Empty+7 and Full-7 for $\overline{PAE}$ and $\overline{PAF}$, respectively. The programmable flag offset loading is controlled by a simple state machine and is initiated by asserting the load pin ($\overline{LD}$).

The IDT72421/72201/72211/72221/72231/72241 are fabricated using IDT's high-speed submicron CMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

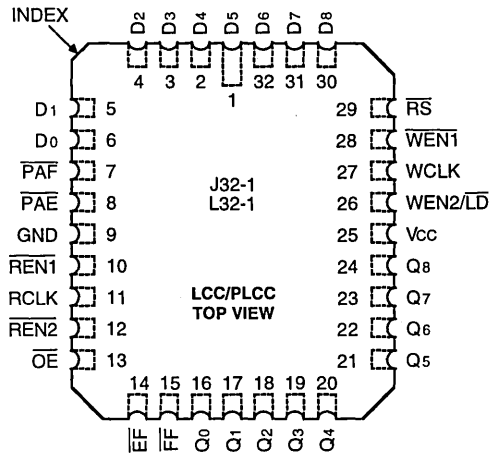
5

FUNCTIONAL BLOCK DIAGRAM



SyncFIFO is a trademark and the IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATION



2655 drw 02

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0-D8	Data Inputs	I	Data inputs for a 9-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go HIGH, and $\overline{PAE}$ and $\overline{EF}$ go LOW. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when the Write Enable(s) are asserted.
$\overline{WEN1}$	Write Enable 1	I	If the FIFO is configured to have programmable flags, $\overline{WEN1}$ is the only write enable pin. When $\overline{WEN1}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition WCLK. If the FIFO is configured to have two write enables, $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
WEN2/$\overline{LD}$	Write Enable 2/ Load	I	The FIFO is configured at reset to have either two write enables or programmable flags. If WEN2/$\overline{LD}$ is HIGH at reset, this pin operates as a second write enable. If WEN2/$\overline{LD}$ is LOW at reset, this pin operates as a control to load and read the programmable flag offsets. If the FIFO is configured to have two write enables, $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held LOW to write or read the programmable flag offsets.
Q0-Q8	Data Outputs	O	Data outputs for a 9-bit bus.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when $\overline{REN1}$ and $\overline{REN2}$ are asserted.
$\overline{REN1}$	Read Enable 1	I	When $\overline{REN1}$ and $\overline{REN2}$ are LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{REN2}$	Read Enable 2	I	When $\overline{REN1}$ and $\overline{REN2}$ are LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high-impedance state.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is Empty+7. $\overline{PAE}$ is synchronized to RCLK.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is Full-7. $\overline{PAF}$ is synchronized to WCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
Vcc	Power		One +5 volt power supply pin.
GND	Ground		One 0 volt ground pin.

2655 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +135	°C
IOUT	DC Output Current	50	50	mA

2655 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIH	Input High Voltage Military	2.2	—	—	V
VIL	Input Low Voltage Commercial & Military	—	—	0.8	V

2655 tbl 03

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN(2)	Input Capacitance	VIN = 0V	10	pF
COUT(1,2)	Output Capacitance	VOUT = 0V	10	pF

2655 tbl 04

NOTES:
1. With output deselected ($\overline{OE}$ = HIGH).
2. Characterized values, not currently tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	IDT72421 IDT72201 IDT72211 Commercial tCLK = 12, 15, 20, 25,35, 50ns Min.	Typ.	Max.	IDT72421 IDT72201 IDT72211 Military tCLK = 20, 25,35, 50ns Min.	Typ.	Max.	Unit
ILI(1)	Input Leakage Current (Any Input)	–1	—	–1	–10	—	10	µA
ILO(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = –2mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8mA	—	—	0.4	—	—	0.4	V
ICC(3)	Active Power Supply Current	—	—	140	—	—	160	mA

2655 tbl 05

Symbol	Parameter	IDT72221 IDT72231 IDT72241 Commercial tCLK = 15, 20, 25, 35, 50ns Min.	Typ.	Max.	IDT72221 IDT72231 IDT72241 Military tCLK = 25, 35, 50ns Min.	Typ.	Max.	Unit
ILI(1)	Input Leakage Current (Any Input)	–1	—	–1	–10	—	10	µA
ILO(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = –2mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8mA	—	—	0.4	—	—	0.4	V
ICC1(4)	Active Power Supply Current	—	—	160	—	—	180	mA

2655 tbl 06

NOTES:
1. Measurements with 0.4 ≤ VIN ≤ VCC.
2. $\overline{OE}$ ≥ VIH, 0.4 ≤ VOUT ≤ VCC.

3 & 4. Measurements are made with outputs open. Tested at fCLK = 20MHz.
(3) Typical ICC1 = 65 + (fCLK * 1.1/MHz) + (fCLK * CL * 0.03/MHz-pF) mA
(4) Typical ICC1 = 80 + (fCLK * 2.1/MHz) + (fCLK * CL * 0.03/MHz-pF) mA
fCLK = 1/tCLK.
CL = external capacitive load (30pF typical)

5

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Com'l.				Commercial & Military								
		72421L12 72201L12 72211L12		72421L15 72201L15 72211L15		72421L20 72201L20 72211L20		72421L25 72201L25 72211L25		72421L35 72201L35 72211L35		72421L50 72201L50 72211L50		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
fS	Clock Cycle Frequency	—	83.3	—	66.7	—	50	—	40	—	28.6	—	20	MHz
tA	Data Access Time	2	8	2	10	2	12	3	15	3	20	3	25	ns
tCLK	Clock Cycle Time	12[1]	—	15[2]	—	20	—	25	—	35	—	50	—	ns
tCLKH	Clock High Time	5	—	6	—	8	—	10	—	14	—	20	—	ns
tCLKL	Clock Low Time	5	—	6	—	8	—	10	—	14	—	20	—	ns
tDS	Data Set-up Time	3	—	4	—	5	—	6	—	8	—	10	—	ns
tDH	Data Hold Time	0.5	—	1	—	1	—	1	—	2	—	2	—	ns
tENS	Enable Set-up Time	3	—	4	—	5	—	6	—	8	—	10	—	ns
tENH	Enable Hold Time	0.5	—	1	—	1	—	1	—	2	—	2	—	ns
tRS	Reset Pulse Width[3]	12	—	15	—	20	—	25	—	35	—	50	—	ns
tRSS	Reset Set-up Time	12	—	15	—	20	—	25	—	35	—	50	—	ns
tRSR	Reset Recovery Time	12	—	15	—	20	—	25	—	35	—	50	—	ns
tRSF	Reset to Flag and Output Time	—	12	—	15	—	20	—	25	—	35	—	50	ns
tOLZ	Output Enable to Output in Low-Z[4]	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	7	3	8	3	10	3	13	3	15	3	28	ns
tOHZ	Output Enable to Output in High-Z[4]	3	7	3	8	3	10	3	13	3	15	3	28	ns
tWFF	Write Clock to Full Flag	—	8	—	10	—	12	—	15	—	20	—	30	ns
tREF	Read Clock to Empty Flag	—	8	—	10	—	12	—	15	—	20	—	30	ns
tAF	Write Clock to Almost-Full Flag	—	8	—	10	—	12	—	15	—	20	—	30	ns
tAE	Read Clock to Almost-Empty Flag	—	8	—	10	—	12	—	15	—	20	—	30	ns
tSKEW1	Skew time between Read Clock & Write Clock for Empty Flag &Full Flag	5	—	6	—	8	—	10	—	12	—	15	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Almost-Full Flag	22	—	28	—	35	—	40	—	42	—	45	—	ns

NOTES:

2655 tbl 07

1. Valid for programmable $\overline{PAE}$ or $\overline{PAF}$ offset values ≤ 7 bytes from respective boundary. With programmable $\overline{PAE}$ or $\overline{PAF}$ offset values such that 7 bytes < offset ≤ 63 bytes, t_{CLK} = 15ns. With programmable $\overline{PAE}$ or $\overline{PAF}$ offset values > 63 bytes, t_{CLK} = 20ns.
2. Valid for programmable $\overline{PAE}$ or $\overline{PAF}$ values ≤ 63 bytes from respective boundary. With programmable $\overline{PAE}$ or $\overline{PAF}$ values > 63 bytes, t_{CLK}= 20ns.
3. Pulse widths less than minimum values are not allowed.
4. Values guaranteed by design, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Commercial				Commercial and Military						
		72221L15 72231L15 72241L15		72221L20 72231L20 72241L20		72221L25 72231L25 72241L25		72221L35 72231L35 72241L35		72221L50 72231L50 72241L50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Clock Cycle Frequency	—	66.7	—	50	—	40	—	28.6	—	20	MHz
tA	Data Access Time	2	10	2	12	3	15	3	20	3	25	ns
tCLK	Clock Cycle Time	15[1]	—	20	—	25	—	35	—	50	—	ns
tCLKH	Clock HIGH Time	6	—	8	—	10	—	14	—	20	—	ns
tCLKL	Clock LOW Time	6	—	8	—	10	—	14	—	20	—	ns
tDS	Data Set-up Time	4	—	5	—	6	—	8	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	2	—	2	—	ns
tENS	Enable Set-up Time	4	—	5	—	6	—	8	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	2	—	2	—	ns
tRS	Reset Pulse Width[2]	15	—	20	—	25	—	35	—	50	—	ns
tRSS	Reset Set-up Time	15	—	20	—	25	—	35	—	50	—	ns
tRSR	Reset Recovery Time	15	—	20	—	25	—	35	—	50	—	ns
tRSF	Reset to Flag Time and Output Time	—	15	—	20	—	25	—	35	—	50	ns
tOLZ	Output Enable to Output in Low-Z[3]	0	—	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	8	3	10	3	13	3	15	3	28	ns
tOHZ	Output Enable to Output in High-Z[3]	3	8	3	10	3	13	3	15	3	28	ns
tWFF	Write Clock to Full Flag	—	10	—	12	—	15	—	20	—	30	ns
tREF	Read Clock to Empty Flag	—	10	—	12	—	15	—	20	—	30	ns
tPAF	Write Clock to Programmable Almost-Full Flag	—	10	—	12	—	15	—	20	—	30	ns
tPAE	Read Clock to Programmable Almost-Empty Flag	—	10	—	12	—	15	—	20	—	30	ns
tSKEW1	Skew Time Between Read Clock and Write Clock for Empty Flag and Full Flag	6	—	8	—	10	—	12	—	15	—	ns
tSKEW2	Skew Time Between Read Clock and Write Clock for Programmable Almost-Empty Flag and Programmable Almost-Full Flag	28	—	35	—	40	—	42	—	45	—	ns

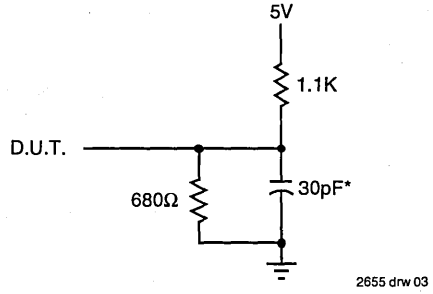
2655 tbl 08

NOTES:
1. Valid for programmable $\overline{PAE}$ or $\overline{PAF}$ offset values ≤ 511 bytes from respective boundary.
   With programmable $\overline{PAE}$ or $\overline{PAF}$ offset values > 511 bytes, t_{CLK} = 20ns.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2655 tbl 09



2655 drw 03

or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

Data In (D_0 - D_8) — Data inputs for 9-bit wide data.

CONTROLS:

Reset ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) will be reset to HIGH after t_{RSF}. The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) will be reset to LOW after t_{RSF}. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

Write Clock (WCLK) — A write cycle is initiated on the LOW-to-HIGH transition of the write clock (WCLK). Data set-up and hold times must be met in respect to the LOW-to-HIGH transition of the write clock (WCLK). The Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) are synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

Write Enable 1 ($\overline{WEN1}$) — If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is low, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable 1 ($\overline{WEN1}$) is HIGH, the input register holds the previous data and no new data is allowed to be loaded into the register.

If the FIFO is configured to have two write enables, which allows for depth expansion, there are two enable control pins. See Write Enable 2 paragraph below for operation in this configuration.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go HIGH after t_{WFF}, allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) is ignored when the FIFO is full.

Read Clock (RCLK) — Data can be read on the outputs on the LOW-to-HIGH transition of the read clock (RCLK). The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) are synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

The write and read clocks can be asynchronous or coincident.

Read Enables ($\overline{REN1}$, $\overline{REN2}$) — When both Read Enables ($\overline{REN1}$, $\overline{REN2}$) are LOW, data is read from the RAM array to the output register on the LOW-to-HIGH transition of the read clock (RCLK).

When either Read Enable ($\overline{REN1}$, $\overline{REN2}$) is HIGH, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{REF} and a valid read can begin. The Read Enables ($\overline{REN1}$, $\overline{REN2}$) are ignored when the FIFO is empty.

Output Enable ($\overline{OE}$) — When Output Enable ($\overline{OE}$) is enabled (LOW), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (HIGH), the Q output data bus is in a high-impedance state.

Write Enable 2/Load (WEN2/$\overline{LD}$) — This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows depth expansion. If Write Enable 2/Load (WEN2/$\overline{LD}$) is set high at Reset ($\overline{RS}$ = LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{WEN1}$) is LOW and Write Enable 2/Load (WEN2/$\overline{LD}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable ($\overline{WEN1}$) is HIGH and/or Write Enable 2/Load (WEN2/$\overline{LD}$) is LOW, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go HIGH after t_{WFF}, allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load (WEN2/$\overline{LD}$) are ignored when the FIFO is full.

The FIFO is configured to have programmable flags when the Write Enable 2/Load (WEN2/$\overline{LD}$) is set LOW at Reset ($\overline{RS}$=low). The IDT72421/72201/72211/72221/72231/72241 devices contain four 8-bit offset registers which can be loaded with data on the inputs, or read on the outputs. See Figure 3 for details of the size of the registers and the default values.

If the FIFO is configured to have programmable flags when the Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load (WEN2/$\overline{LD}$) are set low, data on the inputs D is written into the Empty (Least Significant Bit) offset register on the first LOW-to-HIGH transition of the write clock (WCLK). Data is written into the Empty (Most Significant Bit) offset register on the second LOW-to-HIGH transition of the write clock (WCLK), into the Full (Least Significant Bit) offset register on the third transition, and into the Full (Most Significant Bit) offset register on the fourth transition. The fifth transition of the write clock (WCLK) again writes to the Empty (Least Significant Bit) offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the Write Enable 2/Load (WEN2/$\overline{LD}$) pin HIGH, the FIFO is returned to normal read/write operation. When the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set LOW, and Write Enable 1 ($\overline{WEN1}$) is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set low and both Read Enables ($\overline{REN1}$, $\overline{REN2}$) are set LOW. Data can be read on the LOW-to-HIGH transition of the read clock (RCLK).

A read and write should not be performed simultaneously to the offset registers.

LD	WEN1	WCLK[1]	Selection
0	0	↑	Empty Offset (LSB)
			Empty Offset (MSB)
			Full Offset (LSB)
			Full Offset (MSB)
0	1	↑	No Operation
1	0	↑	Write Into FIFO
1	1	↑	No Operation

NOTE: 2655 drw 04

1. The same selection sequence applies to reading from the registers. $\overline{REN1}$ and $\overline{REN2}$ are enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Figure 2. Write Offset Register

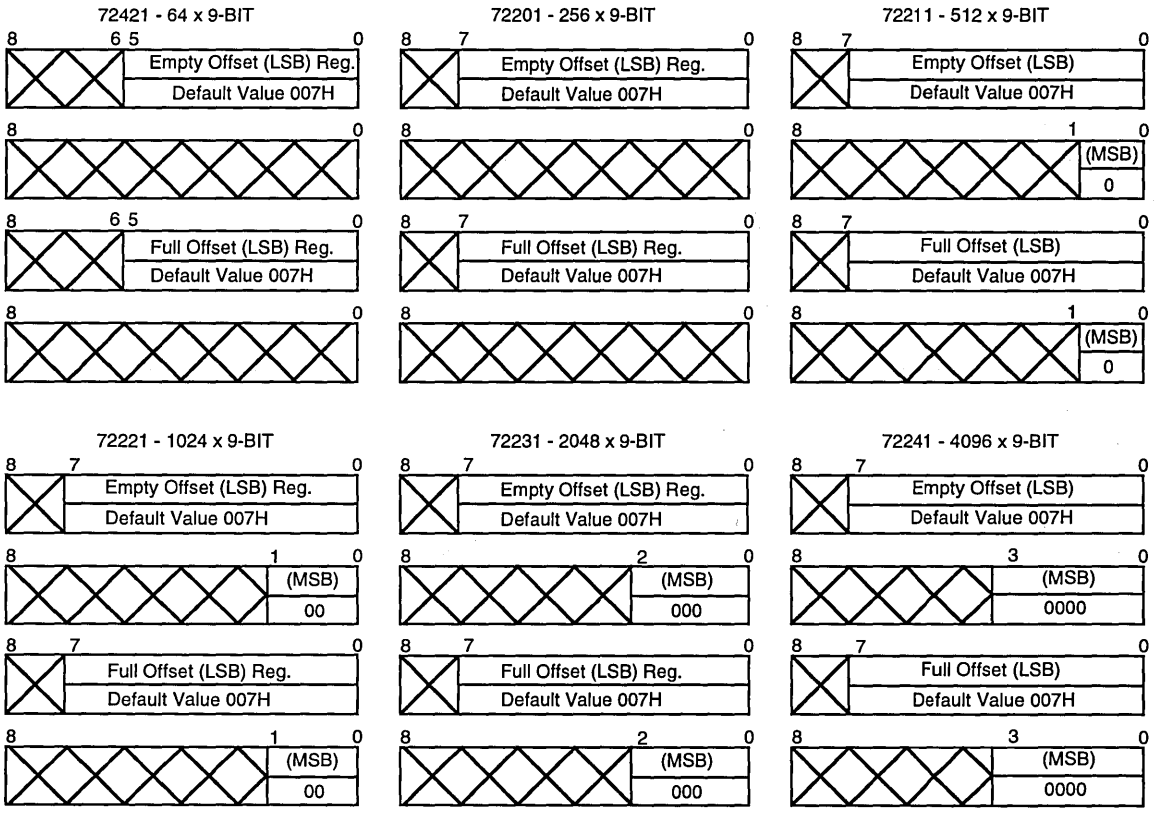


Figure 3. Offset Register Location and Default Values

2655 drw 05

OUTPUTS:

Full Flag ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operation, when the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 64 writes for the IDT72421, 256 writes for the IDT72201, 512 writes for the IDT72211, 1024 writes for the IDT72221, 2048 writes for the IDT72231, and 4096 writes for the IDT72241.

The Full Flag ($\overline{FF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Empty Flag ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Programmable Almost-Full Flag ($\overline{PAF}$) — The Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW when the FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW after (64-m) writes for the IDT72421, (256-m) writes for the IDT72201, (512-m) writes for the IDT72211, (1024-m) writes for the IDT72221, (2048-m) writes for the IDT72231, and (4096-m) writes for the IDT72241. The offset "m" is defined in the Full offset registers.

If there is no Full offset specified, the Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW at Full-7 words.

The Programmable Almost-Full Flag ($\overline{PAF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Programmable Almost-Empty Flag ($\overline{PAE}$) — The Programmable Almost-Empty Flag ($\overline{PAE}$) will go LOW when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the Empty offset registers. If no reads are performed after Reset the Programmable Almost-Empty Flag ($\overline{PAE}$) will go HIGH after "n+1" for the IDT72421/72201/72211/72221/72231/72241.

If there is no Empty offset specified, the Programmable Almost-Empty Flag ($\overline{PAE}$) will go LOW at Empty+7 words.

The Programmable Almost-Empty Flag ($\overline{PAE}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Data Outputs (Q_0 - Q_8) — Data outputs for a 9-bit wide data.

TABLE 1: STATUS FLAGS

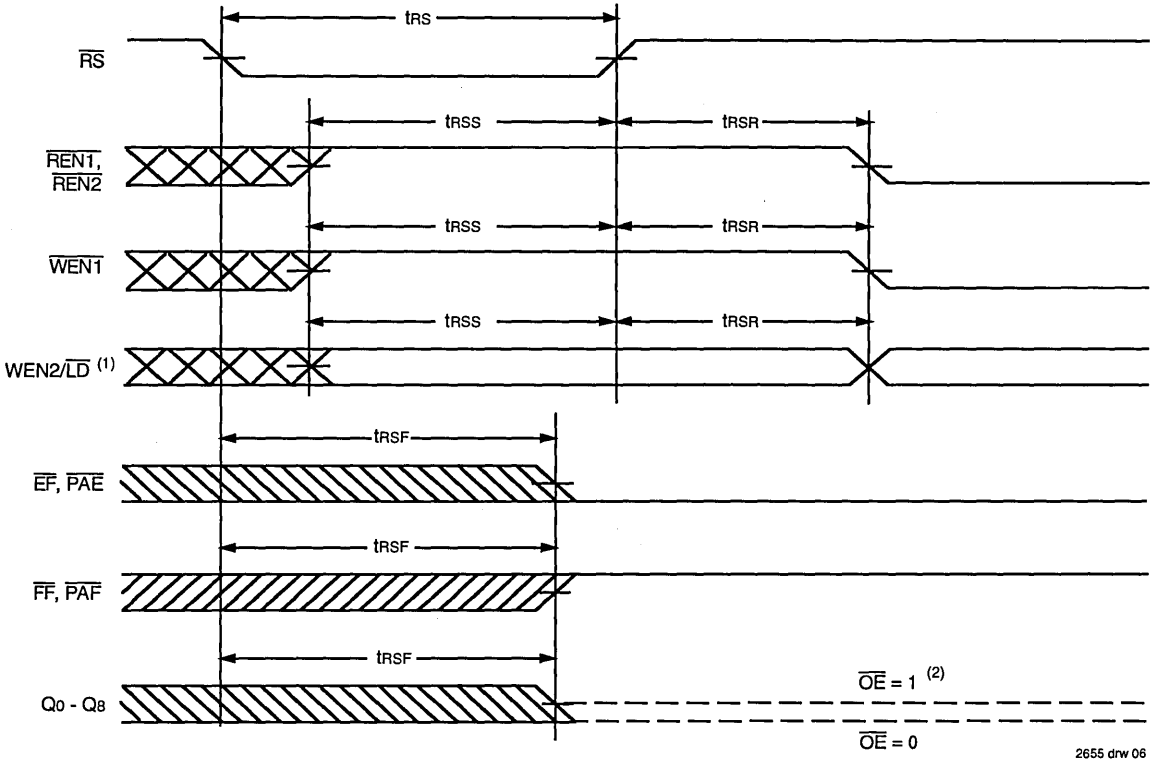
NUMBER OF WORDS IN FIFO						
72421	72201	72211	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	L	H
(n+1) to (64-(m+1))	(n+1) to (256-(m+1))	(n+1) to (512-(m+1))	H	H	H	H
(64-m)[2] to 63	(256-m)[2] to 255	(512-m)[2] to 511	H	L	H	H
64	256	512	L	L	H	H

2655 tbl 10

NUMBER OF WORDS IN FIFO						
72221	72231	72241	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	L	H
(n+1) to (1024-(m+1))	(n+1) to (2048-(m+1))	(n+1) to (4096-(m+1))	H	H	H	H
(1024-m)[2] to 1023	(2048-m)[2] to 2047	(4096-m)[2] to 4095	H	L	H	H
1024	2048	4096	L	L	H	H

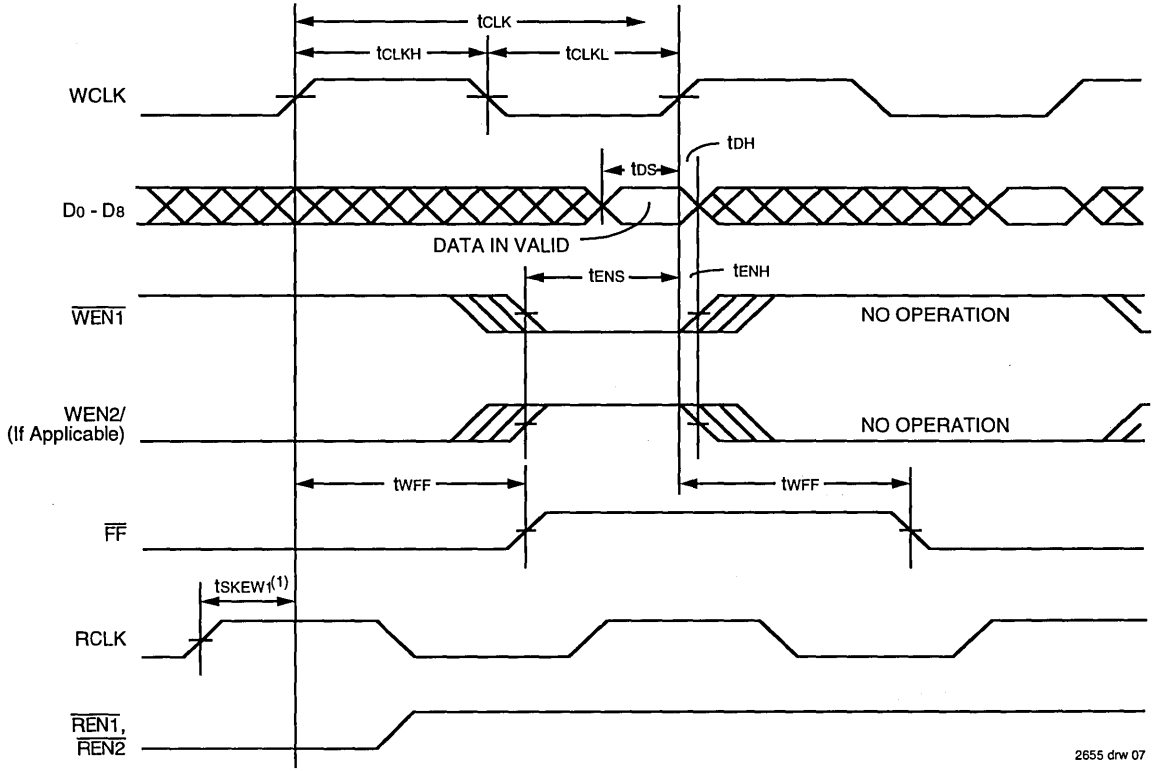
NOTES:
1. n = Empty Offset (n = 7 default value)
2. m = Full Offset (m = 7 default value)

2655 tbl 11



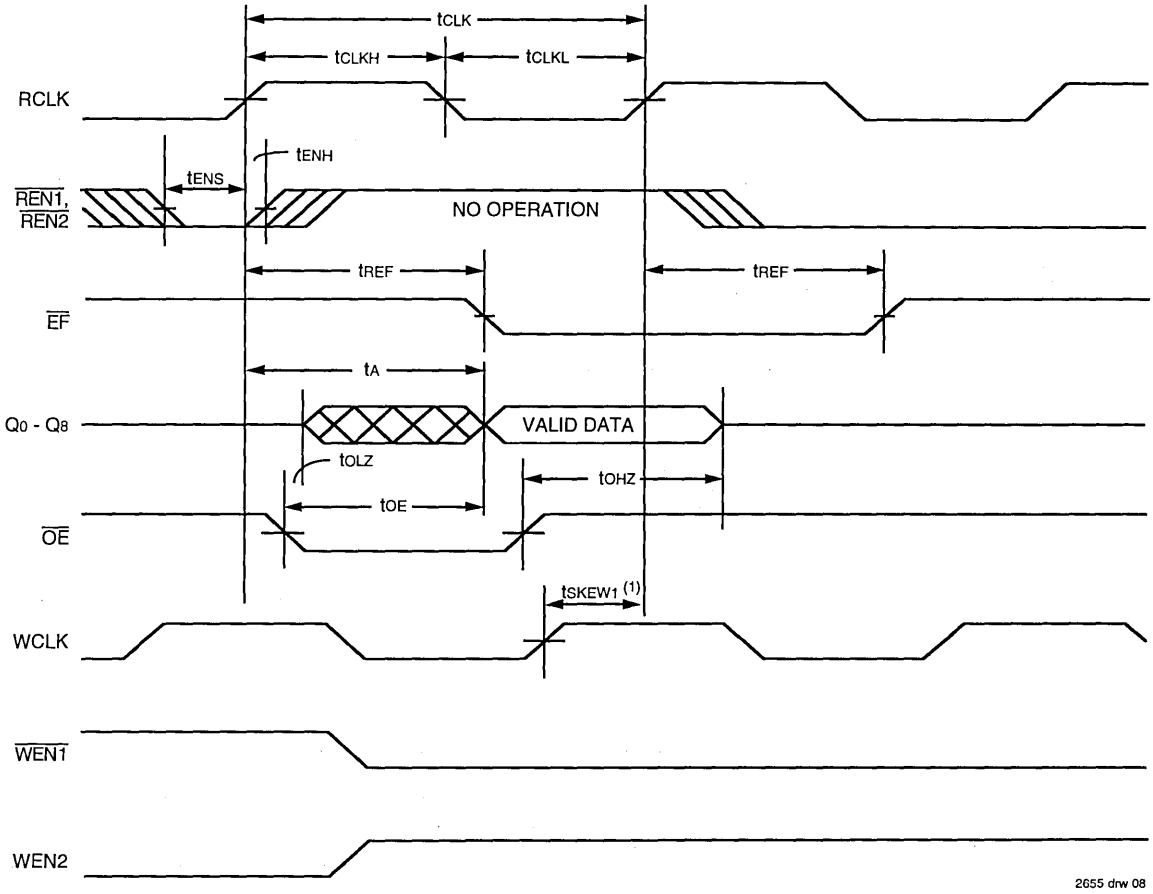
NOTES:
1. Holding WEN2/$\overline{LD}$ HIGH during reset will make the pin act as a second write enable pin. Holding WEN2/$\overline{LD}$ LOW during reset will make the pin act as a load enable for the programmable flag offset registers.
2. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
3. The clocks (RCLK, WCLK) can be free-running during reset.

Figure 4. Reset Timing



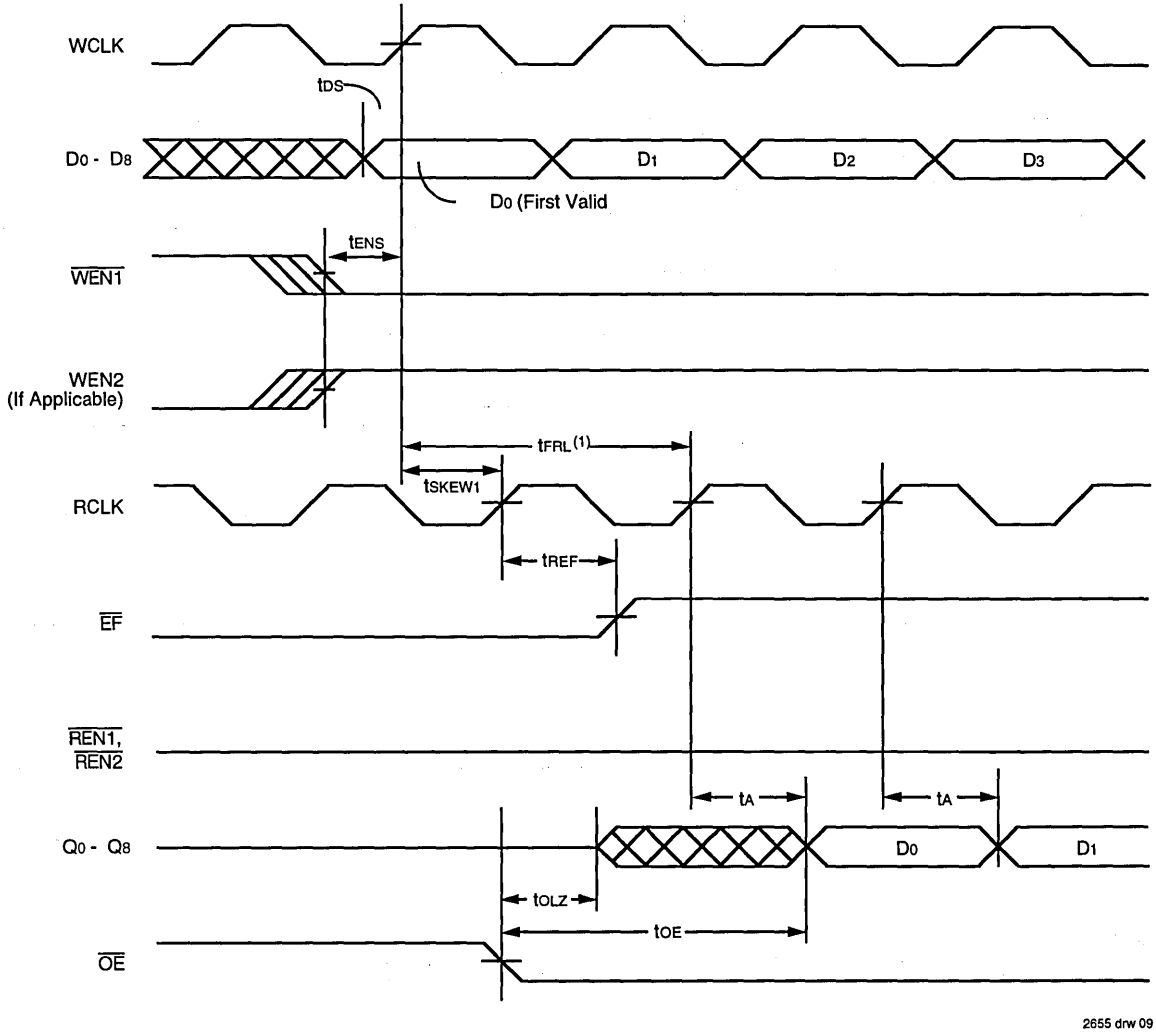
NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 5. Write Cycle Timing



NOTE:
1. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{EF}$ may not change state until the next RCLK edge. Figure 6. Read Cycle Timing

Figure 6. Read Cycle Timing



NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, $t_{FRL} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 7. First Data Word Latency Timing

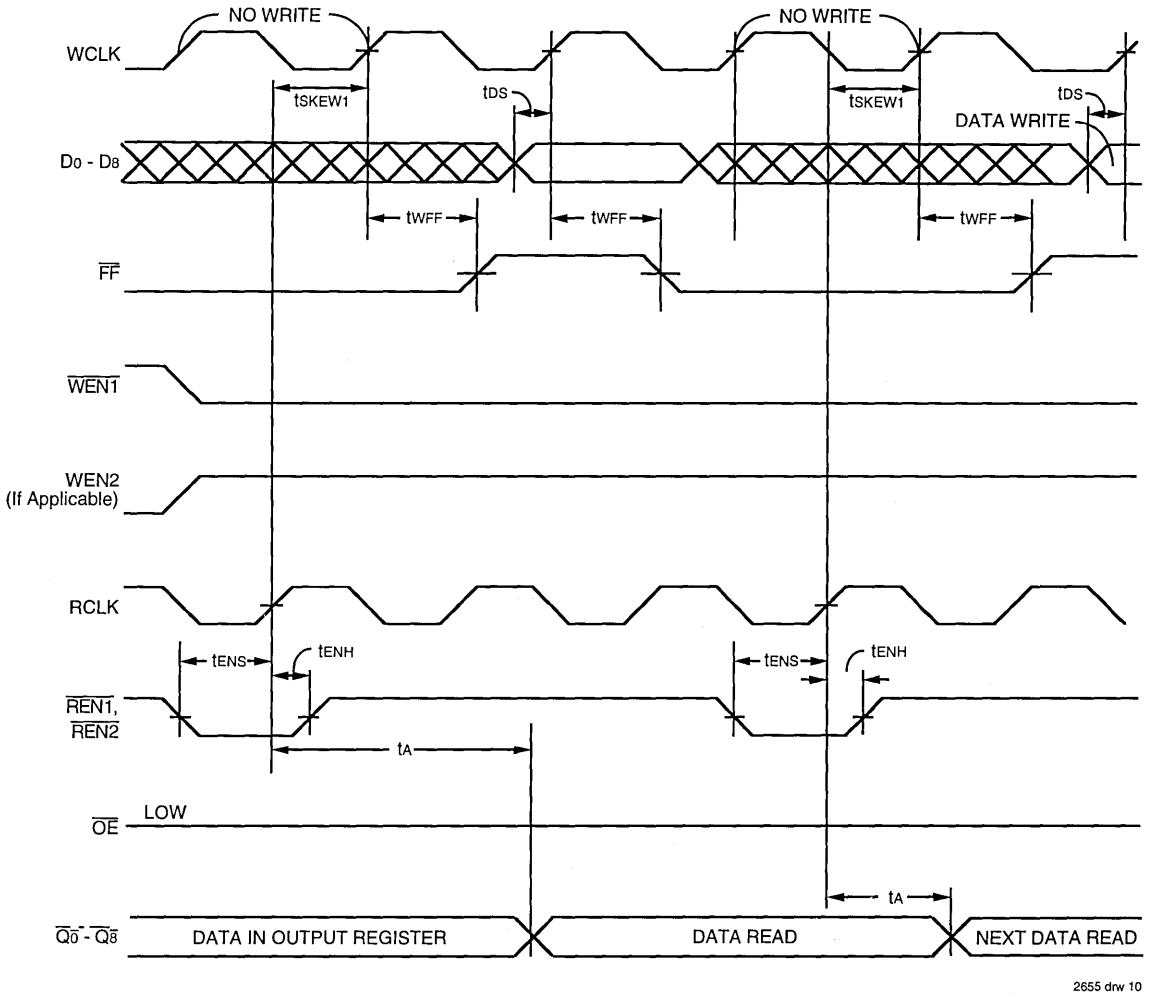
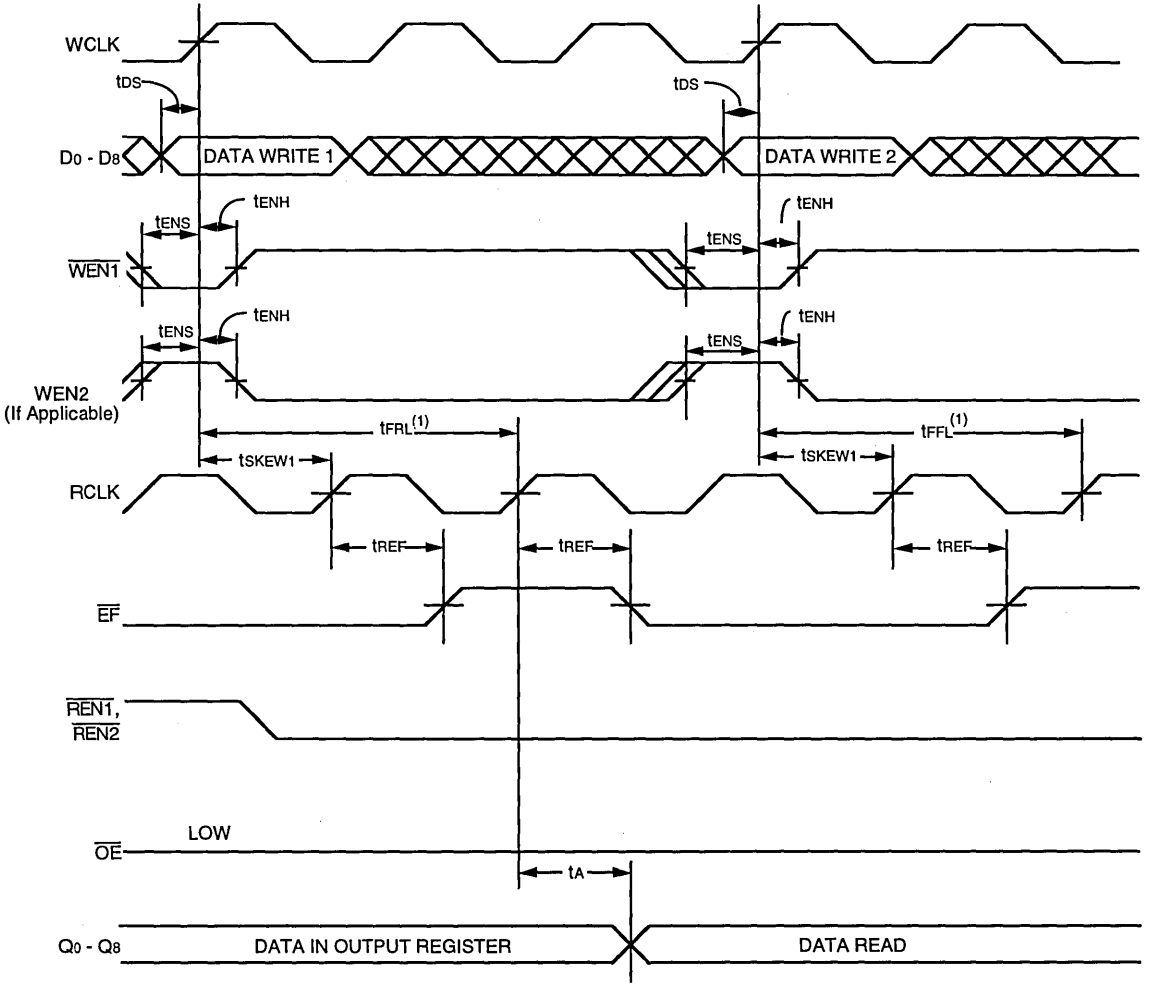


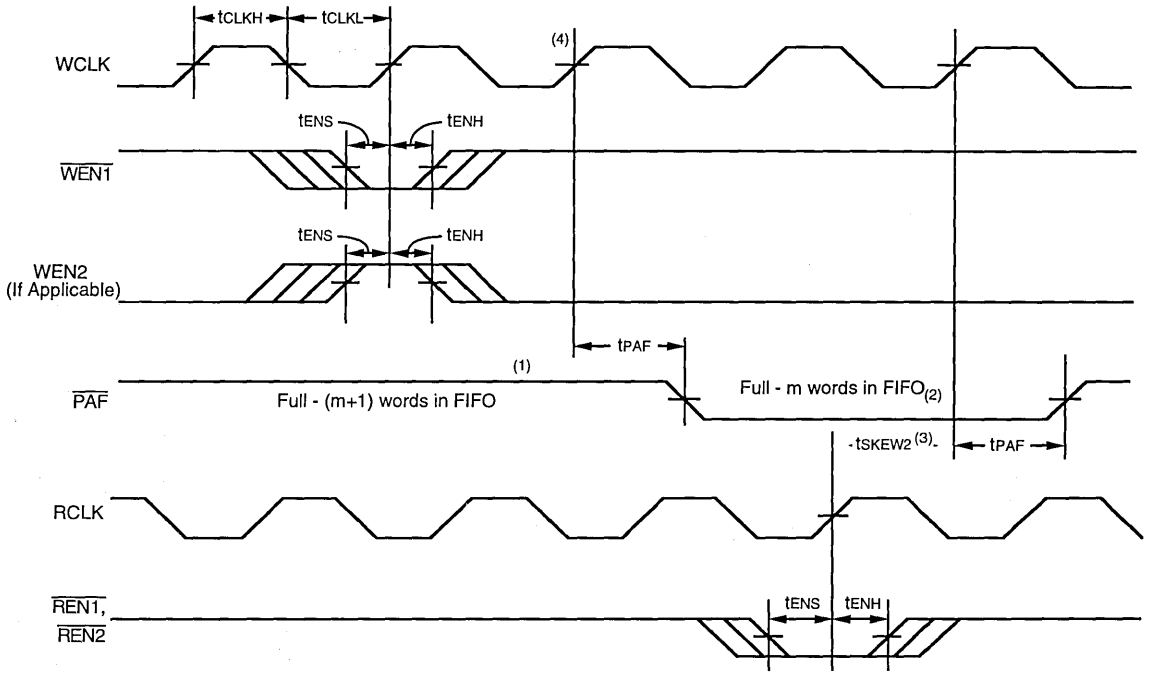
Figure 8. Full Flag Timing



2655 drw 11

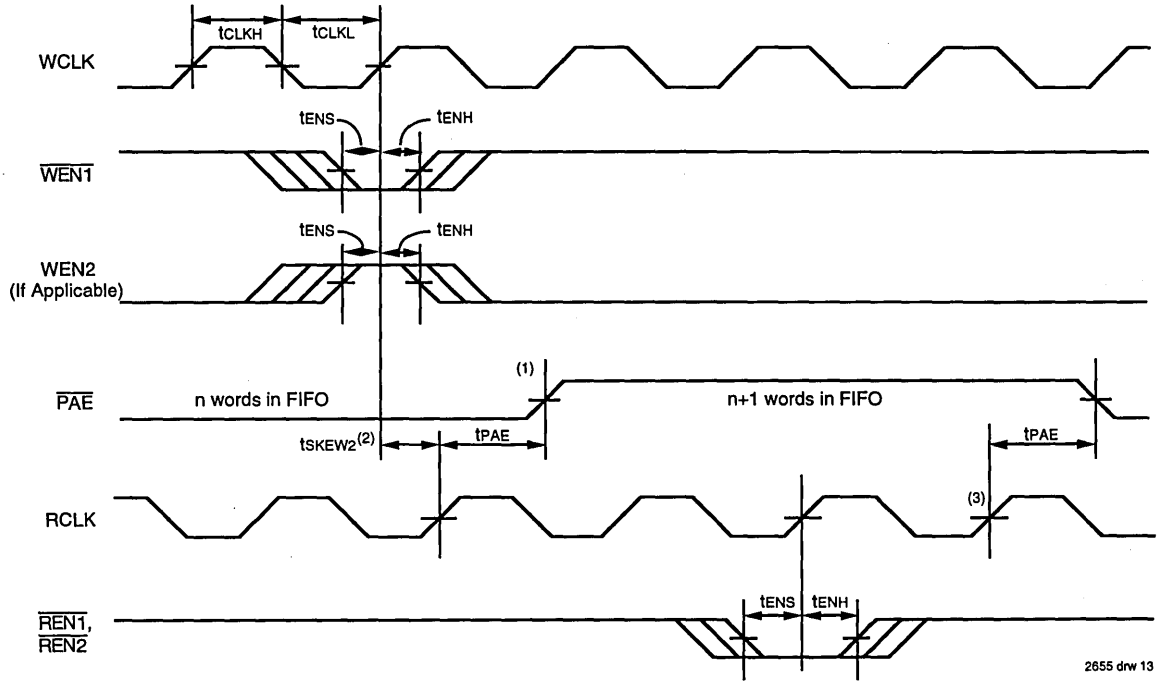
NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 9. Empty Flag Timing



NOTES:
1. PAF offset = m.
2. 64 - m words in for IDT72421, 256 - m words in FIFO for IDT72201, 512 - m words for IDT72211, 1024 - m words for IDT72221, 2048 - m words for IDT72231, 4096 - m words for IDT72241.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK rising edge.
4. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words in the FIFO when $\overline{PAF}$ goes LOW.

Figure 10. Programmable Full Flag Timing



NOTES:
1. PAE offset = n.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to change during that clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK rising edge.
3. If a read is performed on this rising edge of the read clock, there will be Empty + (n-1) words in the FIFO when $\overline{PAE}$ goes LOW.

Figure 11. Programmable Empty Flag Timing

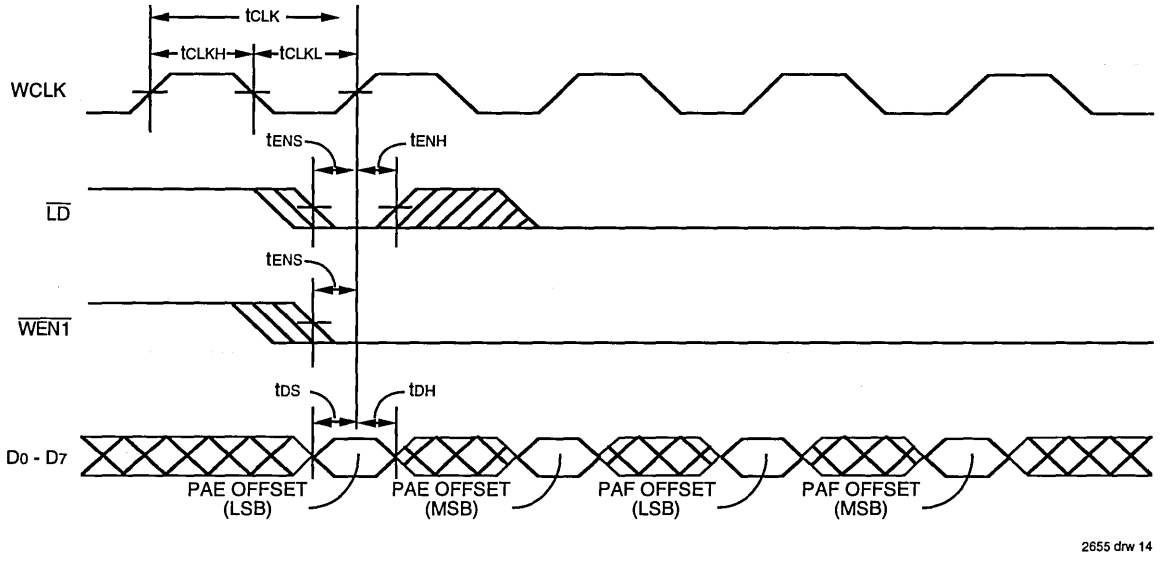


Figure 12. Write Offset Registers Timing

5

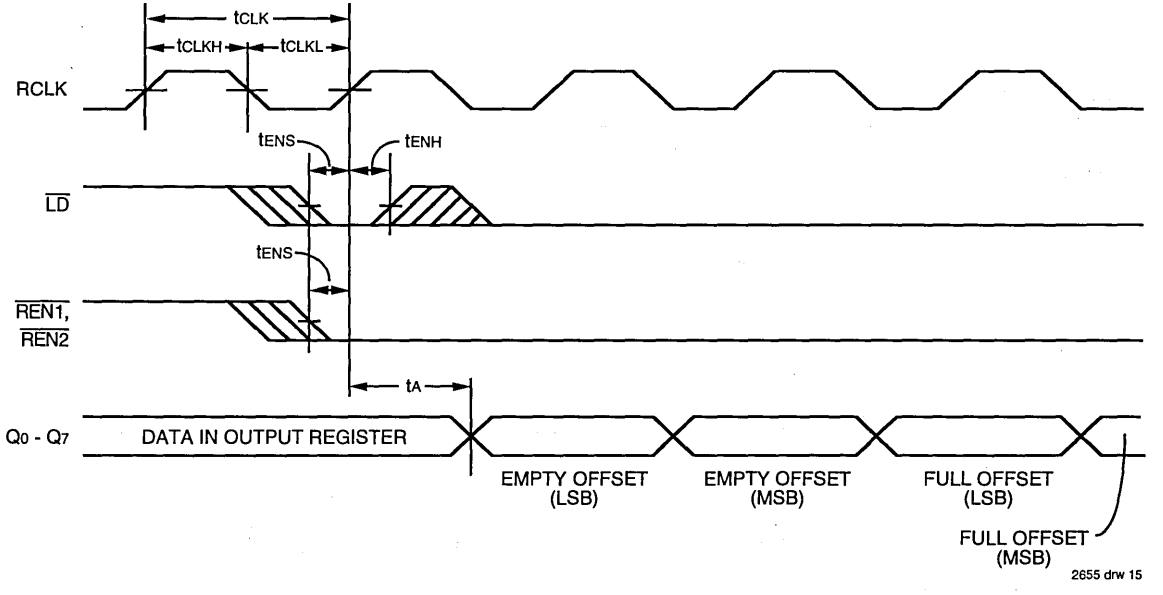


Figure 13. Read Offset Registers Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION - A single IDT72421/72201/72211/72221/72231/72241 may be used when the application requirements are for 64/256/512/1024/2048/4096 words or less. When the IDT72421/72201/72211/72221/72231/72241 are in a Single Device Configuration, the Read Enable 2 ($\overline{REN2}$) control input can be grounded (see Figure 14). In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

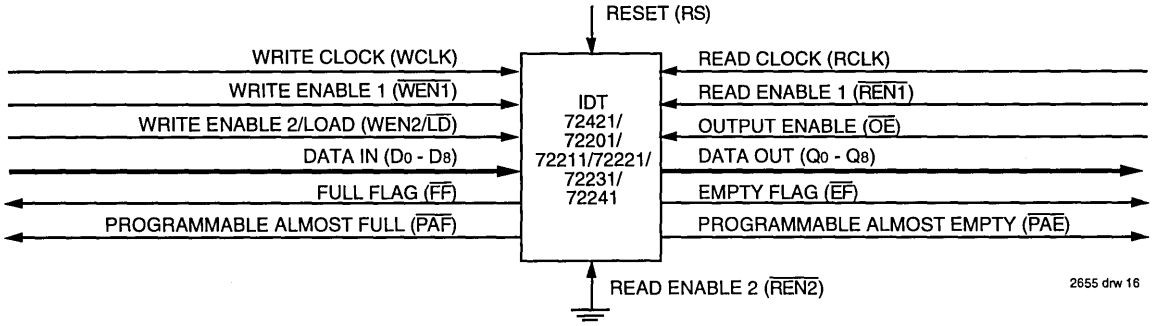


Figure 14. Block Diagram of Single 64 x 9/256 x 9/512 x 9/1024 x 9/2048 x 9/4096 x 9 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION - Word width may be increased simply by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags ($\overline{EF}$ and $\overline{FF}$). The partial status flags ($\overline{AE}$ and $\overline{AF}$) can be detected from any one device. Figure 15 demonstrates a 18-bit word width by using two IDT72421/72201/72211/72221/72231/72241s. Any word width can be attained by adding additional IDT72421/72201/72211/72221/72231/72241s.

When the IDT72421/72201/72211/72221/72231/72241 are in a Width Expansion Configuration, the Read Enable 2 ($\overline{REN2}$) control input can be grounded (see Figure 15). In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

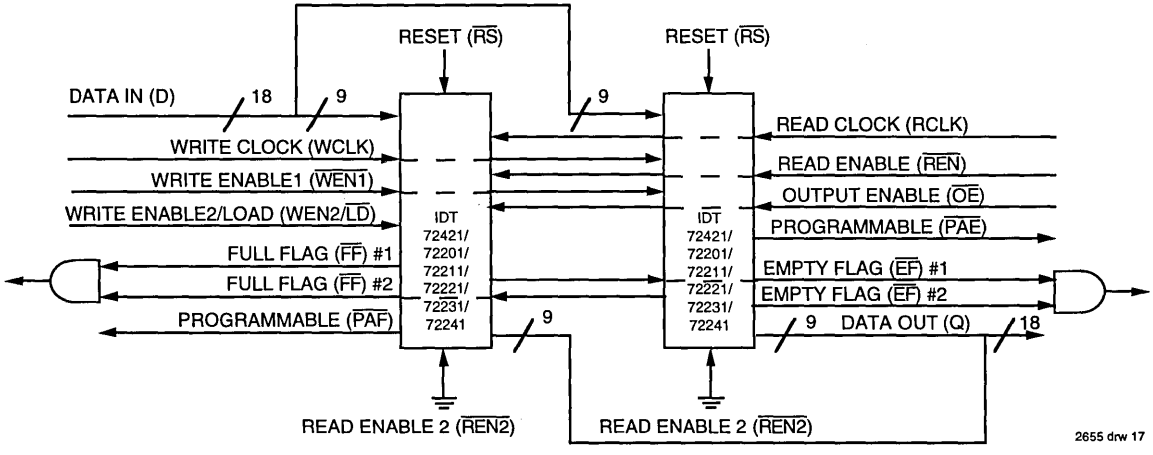


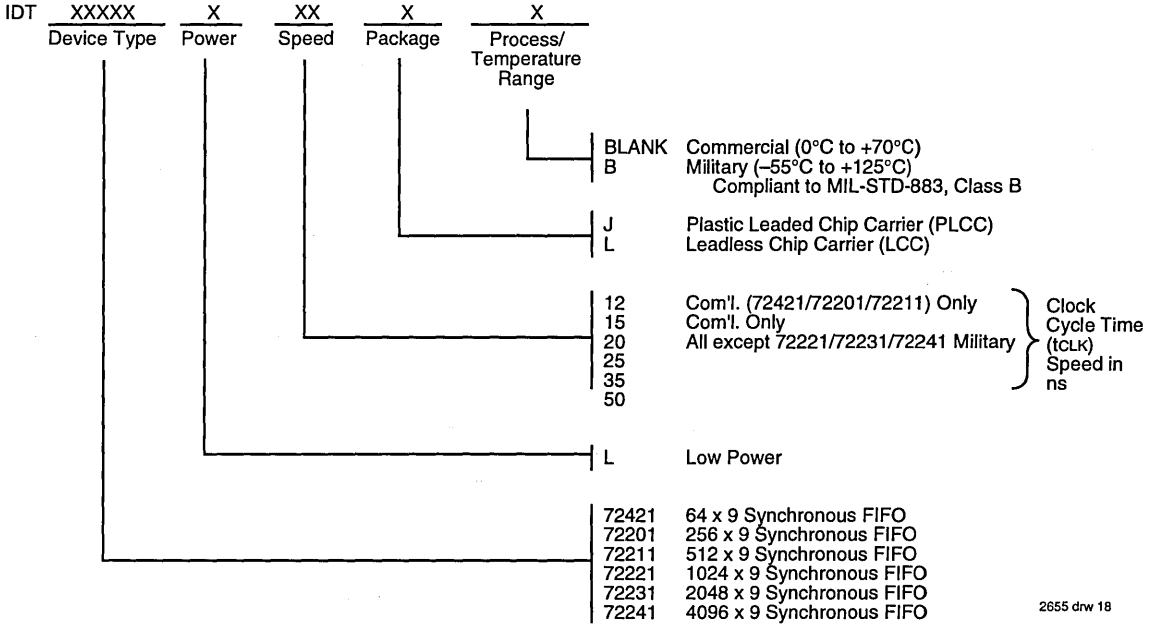
Figure 15. Block Diagram of 64 x 18/256 x 18/512 x 18/1024 x 18/2048 x 18/4096 x 18 Synchronous FIFO Used in a Width Expansion Configuration

DEPTH EXPANSION - The IDT72421/7221/72211/72221/72231/72241 can be adapted to applications when the requirements are for greater than 64/256/512/1024/2048/4096 words. The existence of two enable pins on the read and write port allow depth expansion. The Write Enable 2/Load pin is used as a second write enable in a depth expansion configuration thus the Programmable flags are set to the default values. Depth expansion is possible by using one enable input for system control while the other enable input is controlled by expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data access from one device to the next in a sequential manner. The IDT72421/7221/72211/72221/72231/72241 operates in the Depth Expansion configuration when the following conditions are met:

1. The WEN2/$\overline{LD}$ pin is held HIGH during Reset so that this pin operates a second Write Enable.
2. External logic is used to control the flow of data.

Please see the Applicatioin Note" DEPTH EXPANSION OF IDT'S SYNCHRONOUS FIFOs USING THE RING COUNTER APPROACH" for details of this configuration.

ORDERING INFORMATION



2655 drw 18

5

Integrated Device Technology, Inc.

DUAL CMOS SyncFIFO™

PRELIMINARY
IDT72801
IDT72811
IDT72821
IDT72831
IDT72841

FEATURES:

- The 72801 is equivalent to two 72201 256 x 9 FIFOs
- The 72811 is equivalent to two 72211 512 x 9 FIFOs
- The 72821 is equivalent to two 72221 1024 x 9 FIFOs
- The 72831 is equivalent to two 72231 2048 x 9 FIFOs
- The 72841 is equivalent to two 72241 4096 x 9 FIFOs
- Offers optimal combination of large capacity, high speed, design flexibility and small footprint
- Ideal for prioritization, bidirectional, and width expansion applications
- 15 ns read/write cycle time FOR THE 72801/72811
- 20 ns read/write cycle time FOR THE 72821/72831/72841
- Separate control lines and data lines for each FIFO
- Separate empty, full, programmable almost-empty and almost-full flags for each FIFO
- Enable puts output data lines in high-impedance state
- Space-saving 64-pin Thin Quad Flat Pack (TQFP)

DESCRIPTION:

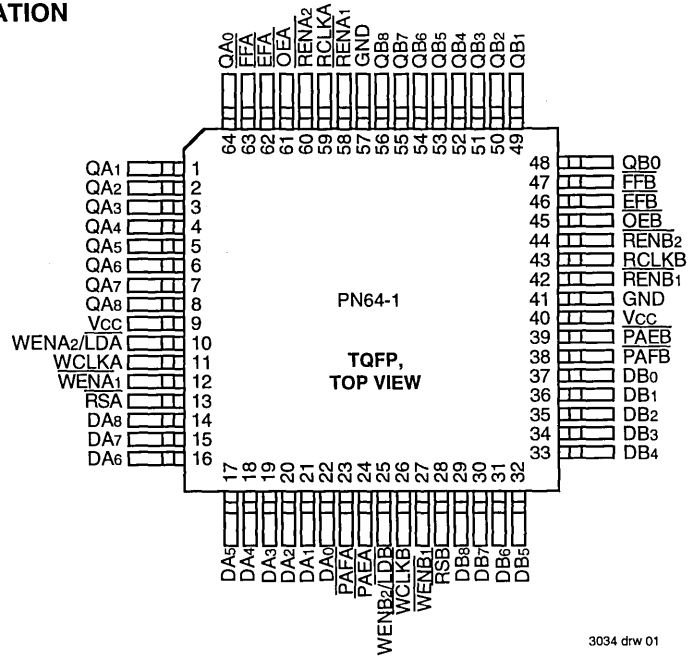
72801/72811/72821/72831/72841 are dual synchronous (clocked) FIFOs. The device is functionally equivalent to two 72201/72211/72221/72231/72241 FIFOs in a single package with all associated control, data, and flag lines assigned to separate pins.

Each of the two FIFOs (designated FIFO A and FIFO B) contained in the 72801/72811/72821/72831/72841 has a 9-bit input data port (DA0 - DA8), DB0 - DB8) and a 9-bit output data port (QA0 - QA8, QB0 - QB8). Each input port is controlled by a free-running clock(WCLKA, WCLKB), and two write enable pins ($\overline{WENA1}$, WENA2, $\overline{WENB1}$, WENB2). Data is written into each of the two arrays on every rising clock edge of the write clock (WCLKA WCLKB) when the appropriate write enable pins are asserted.

The output port of each FIFO bank is controlled by its associated clock pin (RCLKA, RCLKB) and two read enable pins ($\overline{RENA1}$, $\overline{RENA2}$, $\overline{RENB1}$, $\overline{RENB2}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OEA}$, $\overline{OEB}$) is provided on the read port of each FIFO for three-state output control .

Each of the two FIFOs has two fixed flags, empty ($\overline{EFA}$, $\overline{EFB}$) and full ($\overline{FFA}$, $\overline{FFB}$). Two programmable flags, almost-empty ($\overline{PAEA}$, $\overline{PAEB}$) and almost-full ($\overline{PAFA}$, $\overline{PAFB}$), are provided for each FIFO bank to improve memory utilization. If not programmed, the programmable flags default to empty+7 for $\overline{PAEA}$

PIN CONFIGURATION



3034 drw 01

SyncFIFO is a trademark and the IDT logo is a registered trademark of Integrated Device Technology, Inc.

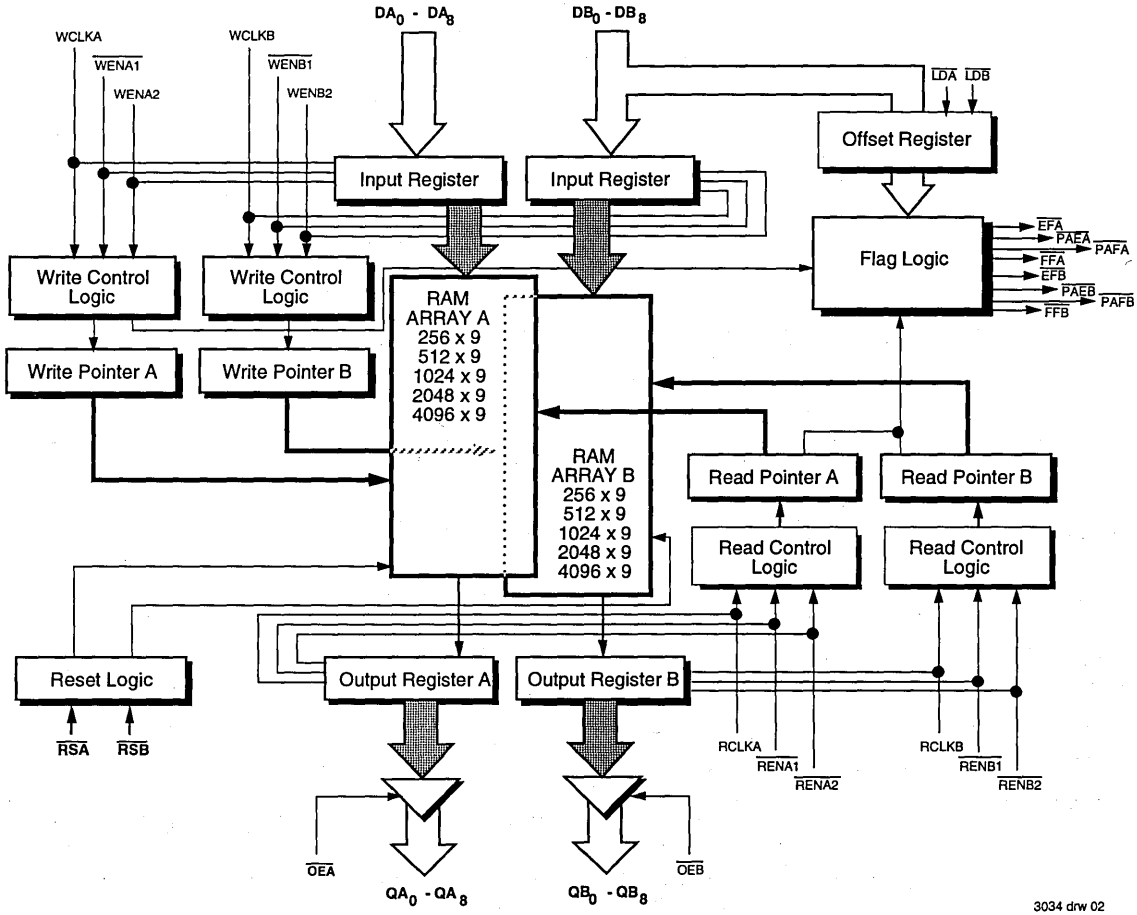
and $\overline{PAEB}$, and full-7 for $\overline{PAFA}$ and $\overline{PAFB}$.

The 72801/72811/72821/72831/72841 architecture lends itself to many flexible configurations such as:

- 2-level priority data buffering
- Bidirectional operation
- Width expansion
- Depth expansion

This FIFO is fabricated using IDTs high-performance sub-micron CMOS technology.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

The 72801/72811/72821/72831/72841 s two FIFOs, referred to as FIFO A and FIFO B, are identical in every respect. The following description defines the input and output signals for FIFO A. The corresponding signal names for FIFO B are provided in parentheses.

Symbol	Name I/O		Description
DA0-DA8	A Data Inputs	I	9-bit data inputs to RAM array A.
DB0-DB8	B Data Inputs	I	9-bit data inputs to RAM array B.
$\overline{RSA}$, $\overline{RSB}$	Reset	I	When $\overline{RSA}$ ($\overline{RSB}$) is set LOW, the associated internal read and write pointers of array A (B) are set to the first location; $\overline{FFA}$ ($\overline{FFB}$) and $\overline{PAFA}$ ($\overline{PAFB}$) go HIGH, and $\overline{PAEA}$ ($\overline{PAEB}$) and $\overline{EFA}$ ($\overline{EFB}$) go LOW. After power-up, a reset of both FIFOs A and B is required before an initial WRITE.
WCLKA WCLKB	Write Clock	I	Data is written into the FIFO A (B) on a LOW-to-HIGH transition of WCLKA (WCLKB) when the write enable(s) are asserted.
$\overline{WENA1}$ $\overline{WENB1}$	Write Enable 1	I	If FIFO A (B) is configured to have programmable flags, $\overline{WENA1}$ ($\overline{WENB1}$) is the only write enable pin that can be used. When $\overline{WENA1}$ ($\overline{WENB1}$) is LOW, data A (B) is written into the FIFO on every LOW-to-HIGH transition WCLKA (WCLKB). If the FIFO is configured to have two write enables, $\overline{WENA1}$ ($\overline{WENB1}$) must be LOW and WENA2 (WENB2) must be HIGH to write data into the FIFO. Data will not be written into the FIFO if $\overline{FFA}$ ($\overline{FFB}$) is LOW.
WENA2/$\overline{LDA}$ WENB2/$\overline{LDB}$	Write Enable 2/ Load	I	FIFO A (B) is configured at reset to have either two write enables or programmable flags. If $\overline{LDA}$ ($\overline{LDB}$) is HIGH at reset, this pin operates as a second write enable. If WENA2/$\overline{LDA}$ (WENB2/$\overline{LDB}$) is LOW at reset this pin operates as a control to load and read the program mable flag offsets for its respective array. If the FIFO is configured to have two write enables, $\overline{WENA1}$ ($\overline{WENB1}$) must be LOW and WENA2 (WENB2) must be HIGH to write data into FIFO A (B). Data will not be written into FIFO A (B) if $\overline{FFA}$ ($\overline{FFB}$) is LOW. If the FIFO is configured to have programmable flags, $\overline{LDA}$($\overline{LDB}$) is held LOW to write or read the programmable flag offsets.
QA0-QA8	A Data Outputs	O	9-bit data outputs from RAM array A.
QB0-QB8	B Data Outputs	O	9-bit data outputs from RAM array B.
RCLKA RCLKB	Read Clock	I	Data is read from FIFO A (B) on a LOW-to-HIGH transition of RCLKA (RCLKB) when $\overline{RENA1}$ ($\overline{RENB1}$) and $\overline{RENA2}$ ($\overline{RENB2}$) are asserted.
$\overline{RENA1}$ $\overline{RENB1}$	Read Enable 1	I	When $\overline{RENA1}$ ($\overline{RENB1}$) and $\overline{RENA2}$ ($\overline{RENB2}$) are LOW, data is read from FIFO A (B) on every LOW-to-HIGH transition of RCLKA (RCLKB). Data will not be read from Array A (B) if $\overline{EFA}$ ($\overline{EFB}$) is LOW.
$\overline{RENA2}$ $\overline{RENB2}$	Read Enable 2	I	When $\overline{RENA1}$ ($\overline{RENB1}$) and $\overline{RENA2}$ ($\overline{RENB2}$) are LOW, data is read from the FIFO A (B) on every LOW-to-HIGH transition of RCLKA (RCLKB). Data will not be read from array A (B) if the $\overline{EFA}$ (EFB) is LOW.
$\overline{OEA}$ $\overline{OEB}$	Output Enable	I	When $\overline{OEA}$ ($\overline{OEB}$) is LOW, outputs DA0-DA8 (DB0-DB8) are active. If $\overline{OEA}$ ($\overline{OEB}$) is HIGH, the outputs DA0-DA8 (DB0-DB8) will be in a high-impedance state.
$\overline{EFA}$ $\overline{EFB}$	Empty Flag	O	When $\overline{EFA}$ ($\overline{EFB}$) is LOW, FIFO A (B) is empty and further data reads from the output are inhibited. When $\overline{EFA}$ ($\overline{EFB}$) is HIGH, FIFO A (B) is not empty. $\overline{EFA}$ ($\overline{EFB}$) is synchronized to RCLKA (RCLKB).
$\overline{PAEA}$ $\overline{PAEB}$	Programmable Almost-Empty Flag	O	When $\overline{PAEA}$ ($\overline{PAEB}$) is LOW, FIFO A (B) is almost empty based on the offset programmed into the appropriate offset register. The default offset at reset is Empty+7. $\overline{PAEA}$ ($\overline{PAEB}$) is synchro nized to RCLKA (RCLKB).
$\overline{PAFA}$ $\overline{PAFB}$	Programmable Almost-Full Flag	O	When $\overline{PAFA}$ ($\overline{PAFB}$) is LOW, FIFO A (B) is almost full based on the offset programmed into the appropriate offset register. The default offset at reset is Full-7. $\overline{PAFA}$ ($\overline{PAFB}$) is synchronized to WCLKA (WCLKB).
$\overline{FFA}$ $\overline{FFB}$	Full Flag	O	When $\overline{FFA}$ ($\overline{FFB}$) is LOW, FIFO A (B) is full and further data writes into the input are inhibited. When $\overline{FFA}$ ($\overline{FFB}$) is HIGH, FIFO A (B) is not full. $\overline{FFA}$ ($\overline{FFB}$) is synchronized to WCLKA (WCLKB).
VCC	Power		+5V power supply pin.
GND	Ground		0V ground pin.

3034 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

3034 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	—	V
VIL	Input Low Voltage	—	—	0.8	V

3034 tbl 03

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN(2)	Input Capacitance	VIN = 0V	10	pF
COUT(1,2)	Output Capacitance	VOUT = 0V	10	pF

3034 tbl 04

NOTE:
1. With output deselected ($\overline{OEA}$, $\overline{OEB}$ = HIGH).

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	IDT72801 IDT72811 Commercial tCLK = 15, 20, 25, 35ns Min.	Typ.	Max.	Unit
ILI(1)	Input Leakage Current (Any Input)	–1	—	–1	µA
ILO(2)	Output Leakage Current	–10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = –2 mA	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8 mA	—	—	0.4	V
ICC(3)	Active Power Supply Current	—	—	270	mA

3034 tbl 05

Symbol	Parameter	IDT72821 IDT72831 IDT72841 Commercial tCLK = 20, 25, 35 ns Min.	Typ.	Max.	Unit
ILI(1)	Input Leakage Current (Any Input)	–1	—	–1	µA
ILO(2)	Output Leakage Current	–10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = –2 mA	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8 mA	—	—	0.4	V
ICC(3)	Active Power Supply Current	—	—	300	mA

3034 tbl 06

NOTES:
1. Measurements with 0.4 ≤ VIN ≤ VCC.
2. OEA, OEB ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. Measurements are made with outputs open. Tested at fCLK = 20MHz. ICC limits applicable when using both banks of FIFO's

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		Commercial								
		IDT72801L15 IDT72811L15		IDT72801L20 IDT72811L20 IDT72821L20 IDT72831L20 IDT72841L20		IDT72801L25 IDT72811L25 IDT72821L25 IDT72831L25 IDT72841L25		IDT72801L35 IDT72811L35 IDT72821L35 IDT72831L35 IDT72841L35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Clock Cycle Frequency	—	66.7	—	50	—	40	—	28.6	MHz
tA	Data Access Time	2	10	2	12	3	15	3	20	ns
tCLK	Clock Cycle Time	15[1]	—	20	—	25	—	35	—	ns
tCLKH	Clock High Time	6	—	8	—	10	—	14	—	ns
tCLKL	Clock Low Time	6	—	8	—	10	—	14	—	ns
tDS	Data Set-up Time	4	—	5	—	6	—	8	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	2	—	ns
tENS	Enable Set-up Time	4	—	5	—	6	—	8	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	2	—	ns
tRS	Reset Pulse Width[2]	15	—	20	—	25	—	35	—	ns
tRSS	Reset Set-up Time	15	—	20	—	25	—	35	—	ns
tRSR	Reset Recovery Time	15	—	20	—	25	—	35	—	ns
tRSF	Reset to Flag Time and Output Time	—	15	—	20	—	25	—	35	ns
tOLZ	Output Enable to Output in Low-Z[3]	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	8	3	10	3	13	3	15	ns
tOHZ	Output Enable to Output in High-Z[3]	3	8	3	10	3	13	3	15	ns
tWFF	Write Clock to Full Flag	—	10	—	12	—	15	—	20	ns
tREF	Read Clock to Empty Flag	—	10	—	12	—	15	—	20	ns
tPAF	Write Clock to Programmable Almost-Full Flag	—	10	—	12	—	15	—	20	ns
tPAE	Read Clock to Programmable Almost-Empty Flag	—	10	—	12	—	15	—	20	ns
tSKEW1	Skew Time Between Read Clock and Write Clock for Empty Flag and Full Flag	6	—	8	—	10	—	12	—	ns
tSKEW2	Skew Time Between Read Clock and Write Clock for Programmable Almost-Empty Flag and Programmable Almost-Full Flag	28	—	35	—	40	—	42	—	ns

NOTES:

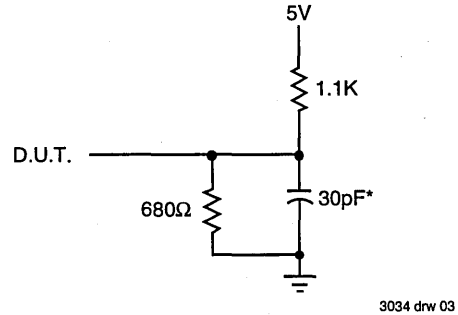
3034 tbl 07

1. Regarding the 72801/72811: this spec is valid for programmable $\overline{PAE}$ or $\overline{PAF}$ offset values ≤ 63. For offset values ≥ 63, t_{CLK} = 20 ns.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

3034 tbl 08



3034 drw 03

or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

FIFO A and FIFO B are identical in every respect. The following description explains the interaction of input and output signals for FIFO A. The corresponding signal names for FIFO B are provided in parentheses.

INPUTS:

Data In ($D_{A0} - D_{A8}$, $D_{B0} - D_{B8}$) — D_{A0} - D_{A8} are the nine data inputs for memory array A. D_{B0} - D_{B8} are the nine data inputs for memory array B.

CONTROLS:

Reset ($\overline{RSA}$, $\overline{RSB}$) — Reset of FIFO A (B) is accomplished whenever $\overline{RSA}$ ($\overline{RSB}$) input is taken to a LOW state. During reset, the internal read and write pointers associated with the FIFO are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag $\overline{FFA}$ ($\overline{FFB}$) and Programmable Almost-Full Flag $\overline{PAFA}$ ($\overline{PAFB}$) will be reset to HIGH after t_{RSF}. The Empty Flag $\overline{EFA}$ ($\overline{EFB}$) and Programmable Almost-Empty Flag $\overline{PAEA}$ ($\overline{PAEB}$) will be reset to LOW after t_{RSF}. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

Write Clock (WCLKA, WCLKB) — A write cycle to Array A (B) is initiated on the LOW-to-HIGH transition of WCLKA (WCLKB). Data set-up and hold times must be met with respect to the LOW-to-HIGH transition of WCLKA (WCLKB). The Full Flag $\overline{FFA}$ ($\overline{FFB}$) and Programmable Almost-Full Flag $\overline{PAFA}$ ($\overline{PAFB}$) are synchronized with respect to the LOW-to-HIGH transition of the write clock WCLKA (WCLKB).

The write and read clocks can be asynchronous or coincident.

Write Enable 1 ($\overline{WENA1}$, $\overline{WENB1}$) — If FIFO A (B) is configured for programmable flags, $\overline{WENA1}$ ($\overline{WENB1}$) is the only enable control pin. In this configuration, when $\overline{WENA1}$ ($\overline{WENB1}$) is LOW, data can be loaded into the input register of RAM Array A (B) on the LOW-to-HIGH transition of every write clock WCLKA (WCLKB). Data is stored in Array A (B) sequentially and independently of any on-going read operation.

In this configuration, when $\overline{WENA1}$ ($\overline{WENB1}$) is HIGH, the input register holds the previous data and no new data is allowed to be loaded into the register.

If the FIFO is configured to have two write enables, which allows for depth expansion. See Write Enable 2 paragraph below for operation in this configuration.

To prevent data overflow, $\overline{FFA}$ ($\overline{FFB}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the $\overline{FFA}$ ($\overline{FFB}$) will go HIGH after t_{WFF}, allowing a valid write to begin. $\overline{WENA1}$ ($\overline{WENB1}$) is ignored when FIFO A (B) is full.

Read Clock (RCLKA, RCLKB) — Data can be read from Array A (B) on the the LOW-to-HIGH transition of RCLKA (RCLKB). The Empty Flag $\overline{EFA}$ ($\overline{EFB}$) and Programmable Almost-Empty Flag $\overline{PAEA}$ ($\overline{PAEB}$) are synchronized with respect to the LOW-to-HIGH transition of RCLKA (RCLKB).

The write and read clock can be asynchronous or coincident.

Read Enables ($\overline{RENA1}$, $\overline{RENA2}$, $\overline{RENB1}$, $\overline{RENB2}$) — When both Read Enables $\overline{RENA1}$, $\overline{RENA2}$ ($\overline{RENB1}$, $\overline{RENB2}$) are LOW, data is read from Array A (B) to the output register on the LOW-to-HIGH transition of the read clock RCLKA (RCLKB).

When either of the two Read Enable $\overline{RENA1}$, $\overline{RENA2}$ ($\overline{RENB1}$, $\overline{RENB2}$) associated with FIFO A (B) is HIGH, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from FIFO A (B), the Empty Flag $\overline{EFA}$ ($\overline{EFB}$) will go LOW, inhibiting further read operations. Once a valid write operation has been accomplished, $\overline{EFA}$ ($\overline{EFB}$) will go HIGH after t_{REF} and a valid read can begin. The Read Enables $\overline{RENA1}$, $\overline{RENA2}$ ($\overline{RENB1}$, $\overline{RENB2}$) are ignored when FIFO A (B) is empty.

Output Enable ($\overline{OEA}$, $\overline{OEB}$) — When Output Enable $\overline{OEA}$ ($\overline{OEB}$) is enabled (LOW), the parallel output buffers of FIFO A (B) receive data from their respective output register. When Output Enable $\overline{OEA}$ ($\overline{OEB}$) is disabled (HIGH), the QA (QB) output data bus is in a high-impedance state.

Write Enable 2/Load ($\overline{WENA2/LDA}$, $\overline{WENB2/LDB}$) — This is a dual-purpose pin. FIFO A (B) is configured at Reset to have programmable flags or to have two write enables, which allows depth expansion. If $\overline{WENA2/LDA}$ ($\overline{WENB2/LDB}$) is set HIGH at Reset $\overline{RSA}$ = LOW ($\overline{RSB}$ = LOW), this pin operates as a second write enable pin.

If FIFO A (B) is configured to have two write enables, when Write Enable 1 $\overline{WENA1}$ ($\overline{WENB1}$) is LOW and $\overline{WENA2/LDA}$ ($\overline{WENB2/LDB}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock WCLKA (WCLKB). Data is stored in the array sequentially and independently of any on-going read operation.

In this configuration, when $\overline{WENA1}$ ($\overline{WENB1}$) is HIGH and/or $\overline{WENA2/LDA}$ ($\overline{WENB2/LDB}$) is LOW, the input register of Array A holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag $\overline{FFA}$ ($\overline{FFB}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, $\overline{FFA}$ ($\overline{FFB}$) will go HIGH after t_{WFF}, allowing a valid write to begin. $\overline{WENA1}$, ($\overline{WENB1}$) and $\overline{WENA2/LDA}$ ($\overline{WENB2/LDB}$) are ignored when the FIFO is full.

FIFO A (B) is configured to have programmable flags when the $\overline{WENA2/LDA}$ ($\overline{WENB2/LDB}$) is set LOW at Reset $\overline{RSA}$ = LOW ($\overline{RSB}$ = LOW). Each FIFO contains four 8-bit offset registers which can be loaded with data on the inputs, or read on the outputs. See Figure 3 for details of the size of the registers and the default values.

5

$\overline{LDA}$	$\overline{WENA1}$	WCLKA(1)	OPERATION ON FIFO A
$\overline{LDB}$	$\overline{WENB1}$	WCLKB(1)	OPERATION ON FIFO B
0	0		Empty Offset (LSB)
			Empty Offset (MSB)
			Full Offset (LSB)
			Full Offset (MSB)
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

3034 drw 04

NOTE:
1. The same selection sequence applies to reading from the registers. $\overline{RENA1}$ and $\overline{RENA2}$ ($\overline{RENB1}$ and $\overline{RENB2}$) are enabled and read is performed on the LOW-to-HIGH transition of RCLKA (RCLKB).

Figure 2. Writing to Offset Registers for FIFOs A and B

If FIFO A (B) is configured to have programmable flags, when the $\overline{WENA1}$ ($\overline{WENB1}$) and WENA2/$\overline{LDA}$ (WENB2/$\overline{LDB}$) are set LOW, data on the DA (DB) inputs are written into the Empty (Least Significant Bit) offset register on the first LOW-to-HIGH transition of the WCLKA (WCLKB). Data are written into the Empty (Most Significant Bit) offset register on the second LOW-to-HIGH transition of WCLKA (WCLKB), into the Full (Least Significant Bit) offset register on the third transition, and into the Full (Most Significant Bit) offset register on the fourth transition. The fifth transition of WCLKA (WCLKB) again writes to the Empty (Least Significant Bit) offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing $\overline{LDA}$ ($\overline{LDB}$) HIGH, FIFO A (B) is returned to normal read/write operation. When $\overline{LDA}$ ($\overline{LDB}$) is set LOW, and $\overline{WENA1}$ ($\overline{WENB1}$) is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the QA (QB) outputs when WENA2/$\overline{LDA}$ (WENB2/$\overline{LDB}$) is set LOW and both Read Enables $\overline{RENA1}$, $\overline{RENA2}$ ($\overline{RENB1}$, $\overline{RENB2}$) are set LOW. Data can be read on the LOW-to-HIGH transition of the read clock RCLKA (RCLKB).

A read and write should not be performed simultaneously to the offset registers.

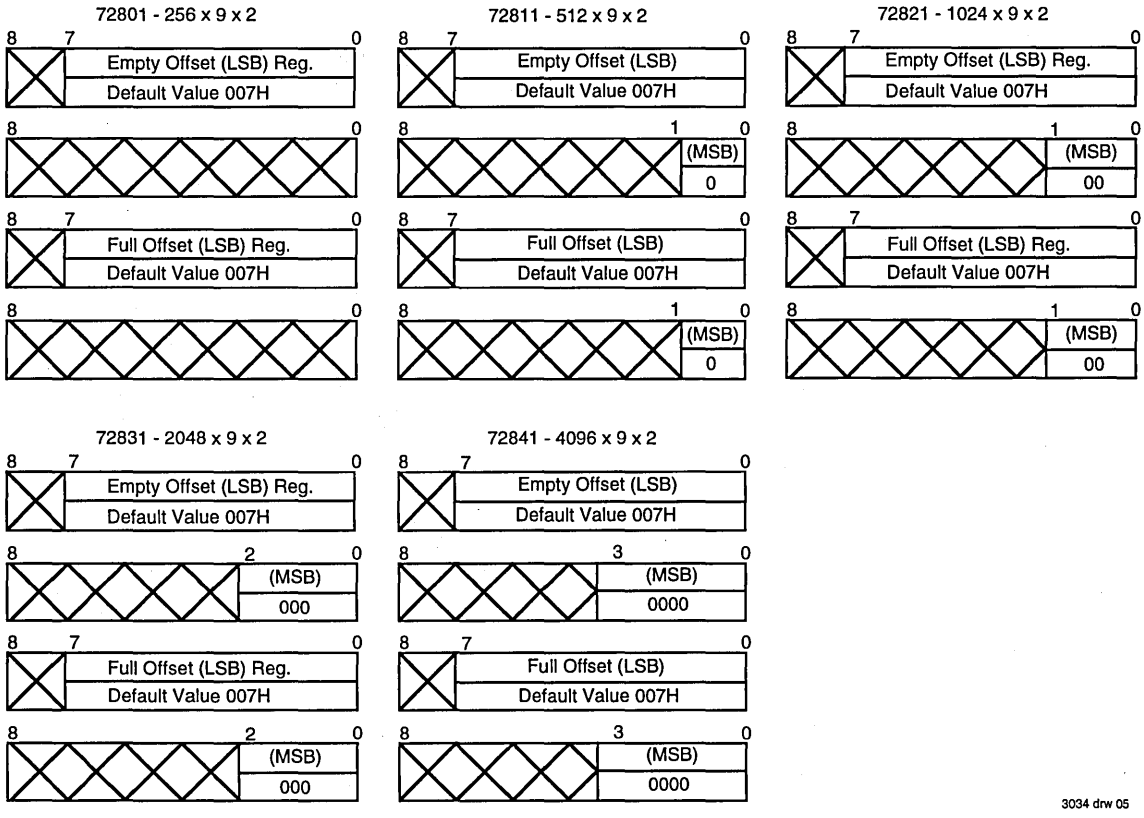


Figure 3. Offset Register Formats and Default Values for the A and B FIFOs

OUTPUTS:

Full Flag ($\overline{FFA}$, $\overline{FFB}$) — $\overline{FFA}$ ($\overline{FFB}$) will go LOW, inhibiting further write operations, when Array A (B) is full. If no reads are performed after reset, $\overline{FFA}$ ($\overline{FFB}$) will go LOW after 256 writes to the 72801's FIFO A (B), 512 writes to the 72811's FIFO A (B), 1024 writes to the 72821's FIFO A (B), 2048 writes to the 72831's FIFO A (B), or 4096 writes to the 72841's FIFO A (B).

$\overline{FFA}$ ($\overline{FFB}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock WCLKA (WCLKB).

Empty Flag ($\overline{EFA}$, $\overline{EFB}$) — $\overline{EFA}$ ($\overline{EFB}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that Array A (B) is empty.

$\overline{EFA}$ ($\overline{EFB}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock RCLKA (RCLKB).

Programmable Almost-Full Flag ($\overline{PAFA}$, $\overline{PAFB}$) — $\overline{PAFA}$ ($\overline{PAFB}$) will go LOW when the amount of data in Array A (B) reaches the Almost-Full condition. If no reads are performed after reset, $\overline{PAFA}$ ($\overline{PAFB}$) will go LOW after (256-m) writes to the 72801's FIFO A (B), (512-m) writes to the 72811's FIFO A (B), (1024-m) writes to the 72821's FIFO A (B), (2048-m) writes to the 72831's FIFO A (B), or (4096-m) writes to the 72841's FIFO A (B).

$\overline{FFA}$ ($\overline{FFB}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock WCLKA (WCLKB). The offset "m" is defined in the Full Offset Registers.

If there is no Full offset specified, $\overline{PAFA}$ ($\overline{PAFB}$) will go LOW at Full-7 words.

$\overline{PAFA}$ ($\overline{PAFB}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock WCLKA (WCLKB).

Programmable Almost-Empty Flag ($\overline{PAEA}$, $\overline{PAEB}$) — $\overline{PAEA}$ ($\overline{PAEB}$) will go LOW when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the Empty Offset Registers. If no reads are performed after reset, $\overline{PAEA}$ ($\overline{PAEB}$) will go HIGH after "n+1" writes to FIFO A (B).

If there is no Empty offset specified, $\overline{PAEA}$ ($\overline{PAEB}$) will go LOW at Empty+7 words.

$\overline{PAEA}$ ($\overline{PAEB}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock RCLKA (RCLKB).

Data Outputs ($QA_0 - QA_8$, $QB_0 - QB_8$) — QA_0 - QA_8 are the nine data outputs for memory array A, QB_0 - QB_8 are the nine data outputs for memory array B.

5

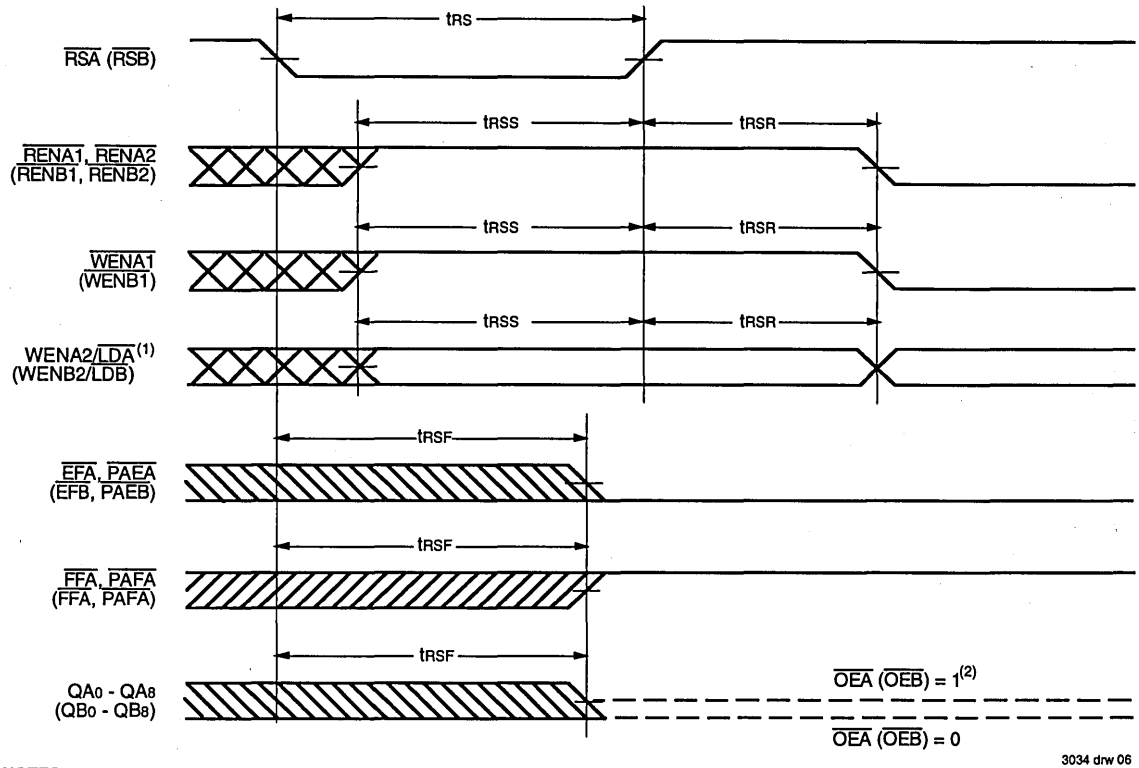
TABLE 1: STATUS FLAGS FOR A AND B FIFOS

NUMBER OF WORDS IN ARRAY A			$\overline{FFA}$	$\overline{PAFA}$	$\overline{PAEA}$	$\overline{EFA}$
NUMBER OF WORDS IN ARRAY B			$\overline{FFB}$	$\overline{PAFB}$	$\overline{PAEB}$	$\overline{EFB}$
72801	**72811**	**72821**				
0	0	0	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	L	H
(n+1) to (256-(m+1))	(n+1) to (512-(m+1))	(n+1) to (1024-(m+1))	H	H	H	H
(256-m)[2] to 255	(512-m)[2] to 511	(1024-m)[2] to 1023	H	L	H	H
256	512	1024	L	L	H	H

NUMBER OF WORDS IN ARRAY A		$\overline{FFA}$	$\overline{PAFA}$	$\overline{PAEA}$	$\overline{EFA}$
NUMBER OF WORDS IN ARRAY B		$\overline{FFB}$	$\overline{PAFB}$	$\overline{PAEB}$	$\overline{EFB}$
72831	**72841**				
0	0	H	H	L	L
1 to n[1]	1 to n[1]	H	H	L	H
(n+1) to (2048-(m+1))	(n+1) to (4096-(m+1))	H	H	H	H
(2048-m)[2] to 2047	(4096-m)[2] to 4095	H	L	H	H
2048	4096	L	L	H	H

NOTES:
1. n = Empty Offset (n = 7 default value)
2. m = Full Offset (m = 7 default value)

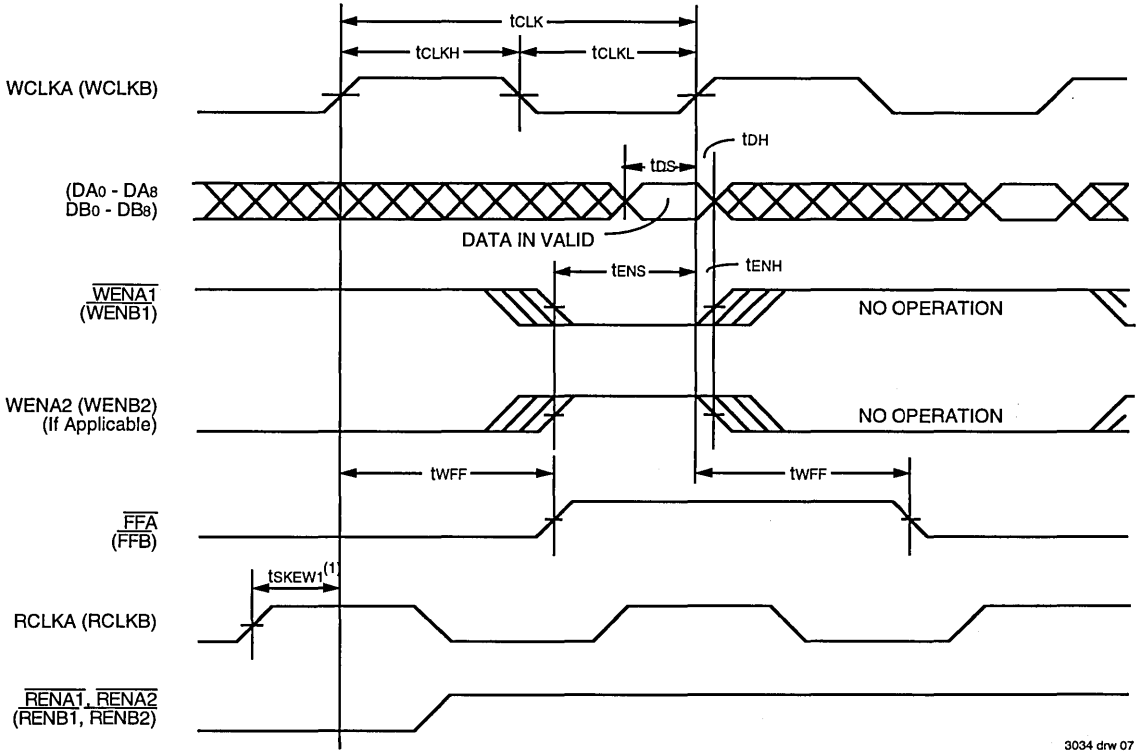
3034 tbl 09



NOTES:

1. Holding WENA2/LDA (WENB2/LDB) HIGH during reset will make the pin act as a second write enable pin. Holding WEN2/LDA (WENB2/LDB) LOW during reset will make the pin act as a load enable for the programmable flag offset registers.
2. After reset, QA0 - QA8 (QB0 - QB8) will be LOW if OEA (OEB) = 0 and tri-state if OEA (OEB) = 1.
3. The clocks RCLKA, WCLKA (RCLKB, WCLKB) can be free-running during reset.

Figure 4. Reset Timing

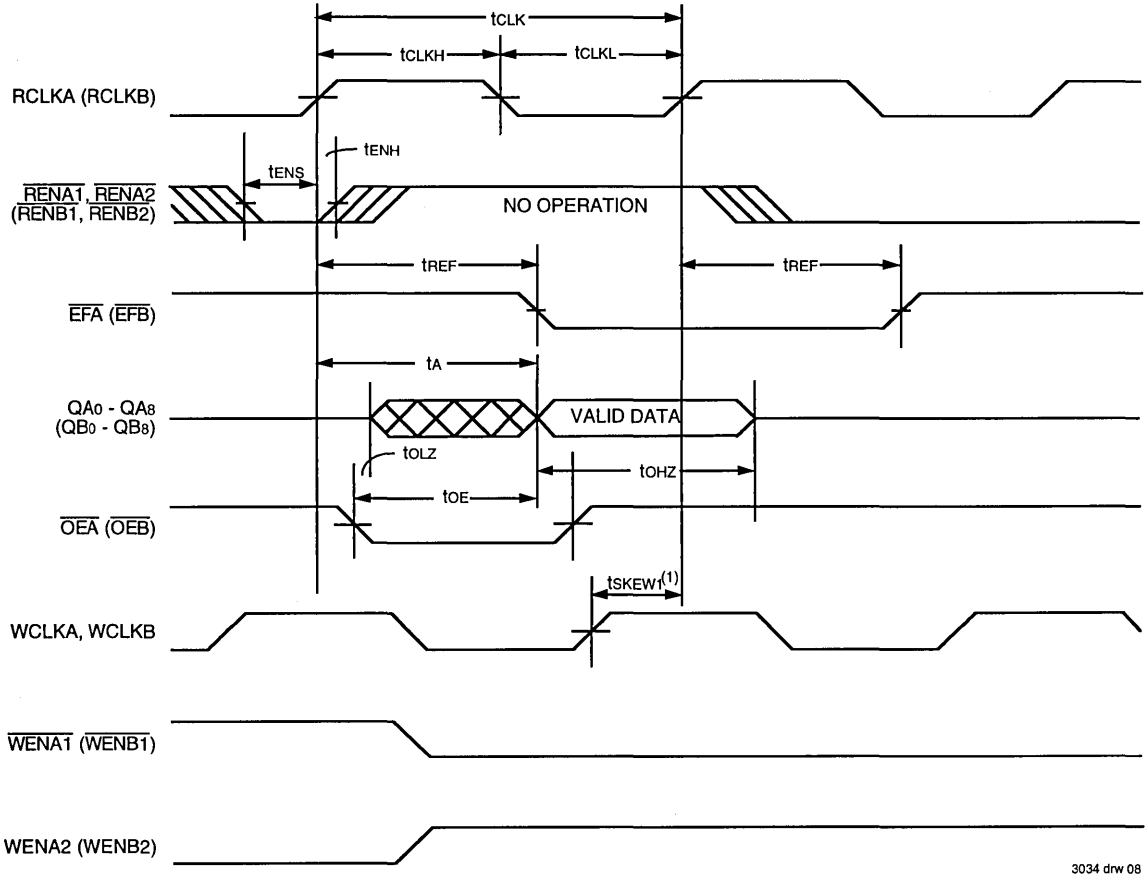


NOTE:

1. t_{SKEW1} is the minimum time between a rising RCLKA (RCLKB) edge and a rising WCLKA (WCLKB) edge for $\overline{FFA}$ ($\overline{FFB}$) to change during the current clock cycle. If the time between the rising edge of RCLKA (RCLKB) and the rising edge of WCLKA (WCLKB) is less than t_{SKEW1}, then $\overline{FFA}$ ($\overline{FFB}$) may not change state until the next RCLKA (RCLKB) edge.

Figure 5. Write Cycle Timing

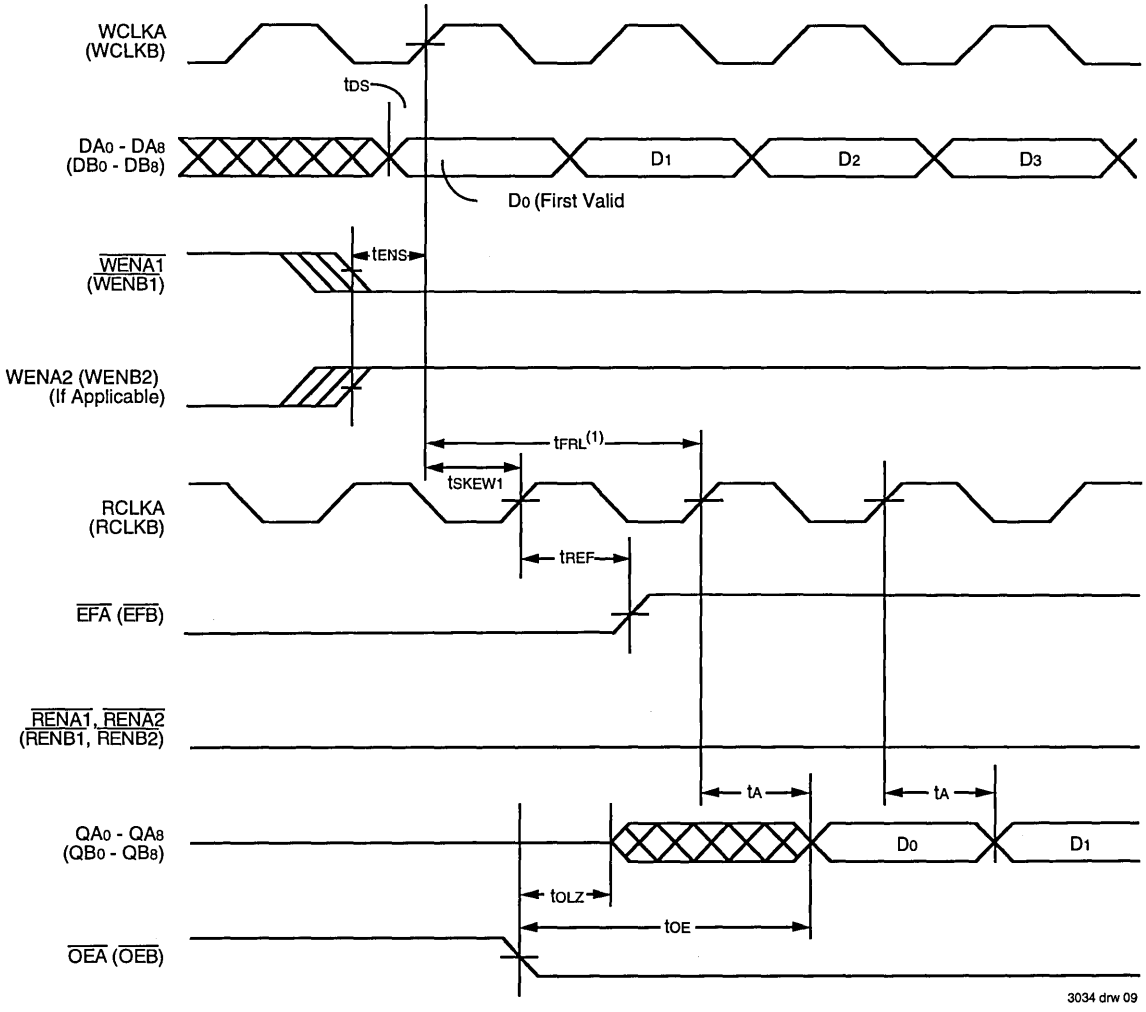
5



NOTE:

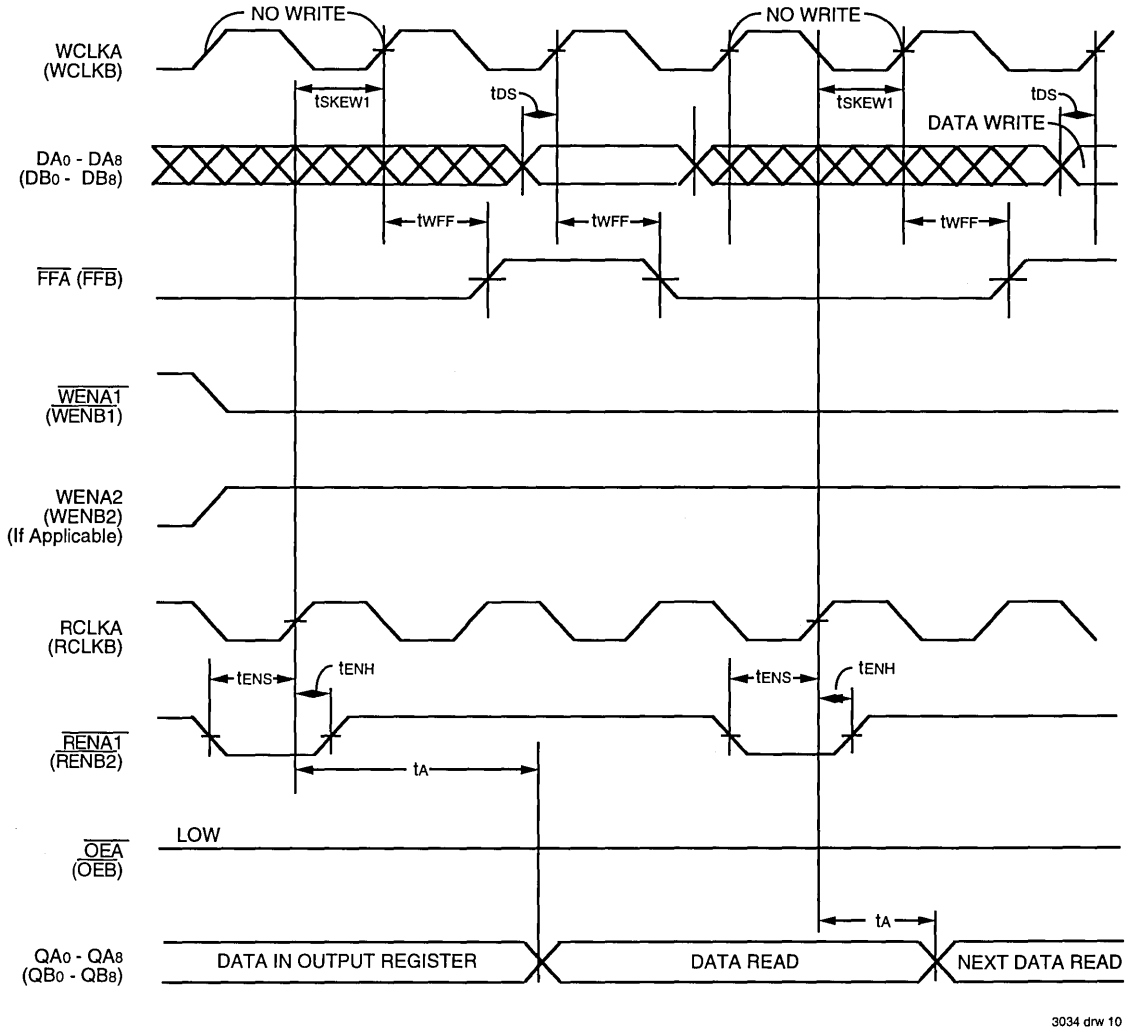
1. t_{SKEW1} is the minimum time between a rising WCLKA (WCLKB) edge and a rising RCLKA (RCLKB) edge for $\overline{EFA}$ ($\overline{EFB}$) to change during the current clock cycle. If the time between the rising edge of RCLKA (RCLKB) and the rising edge of WCLKA (WCLKB) is less than t_{SKEW1}, then $\overline{EFA}$ ($\overline{EFB}$) may not change state until the next RCLKA (RCLKB) edge.

Figure 6. Read Cycle Timing



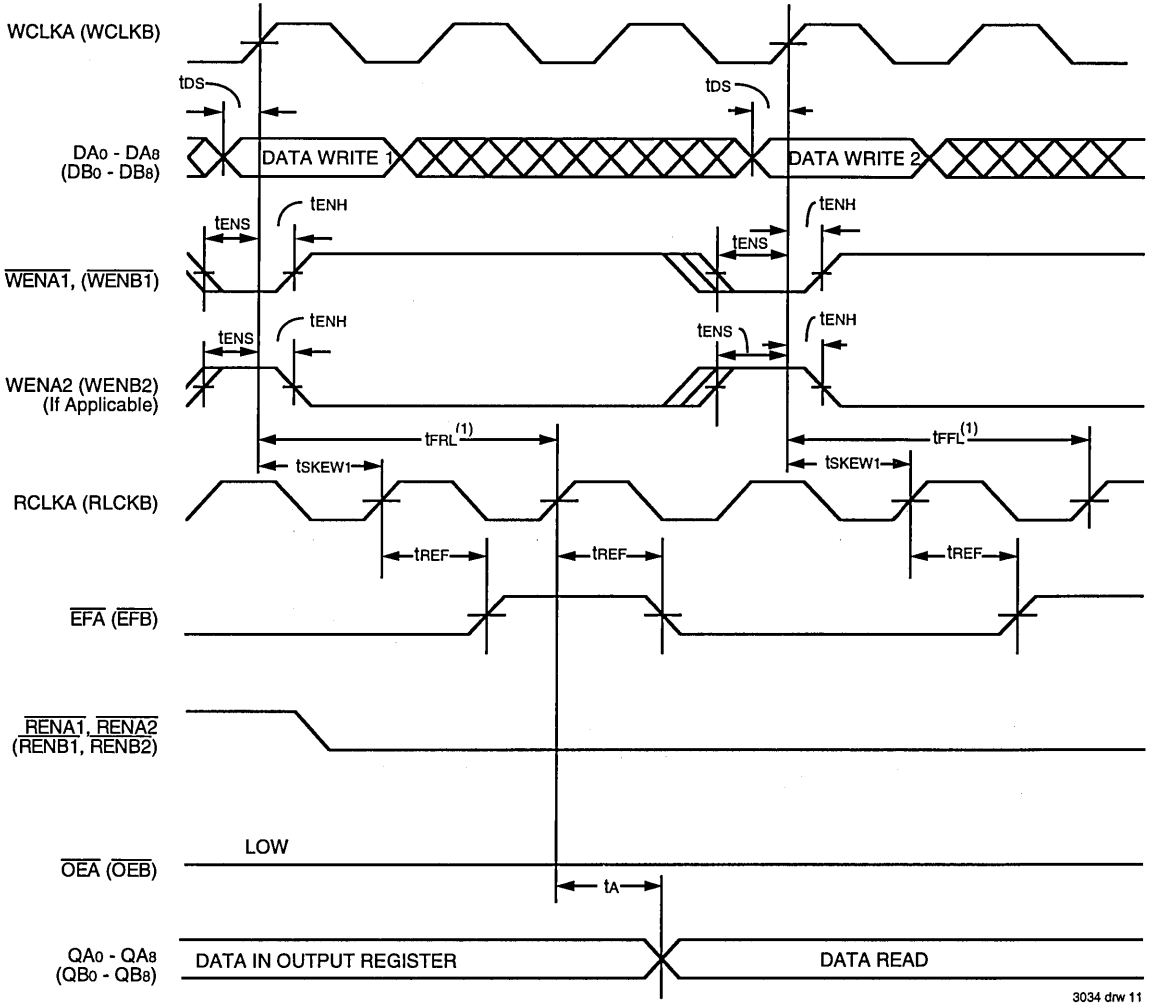
NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, $t_{FRL} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EFA}$, $\overline{EFB}$ = LOW).

Figure 7. First Data Word Latency Timing



3034 drw 10

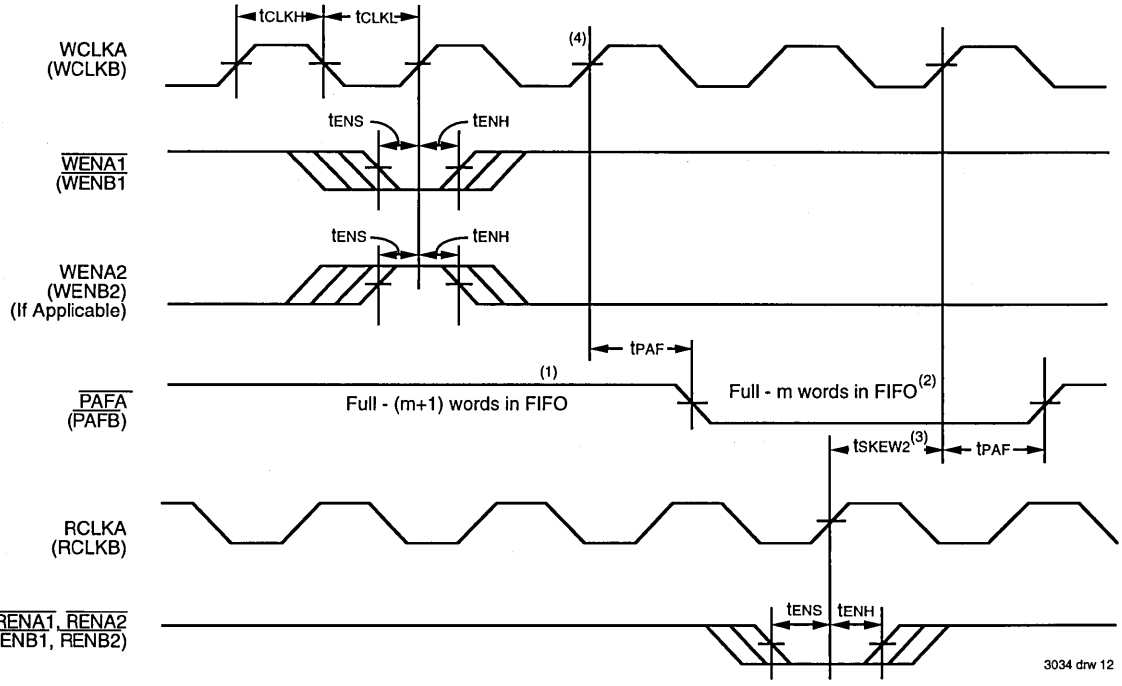
Figure 8. Full Flag Timing



NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at at the Empty Boundary ($\overline{EFA}$, $\overline{EFB}$ = LOW).

Figure 9. Empty Flag Timing

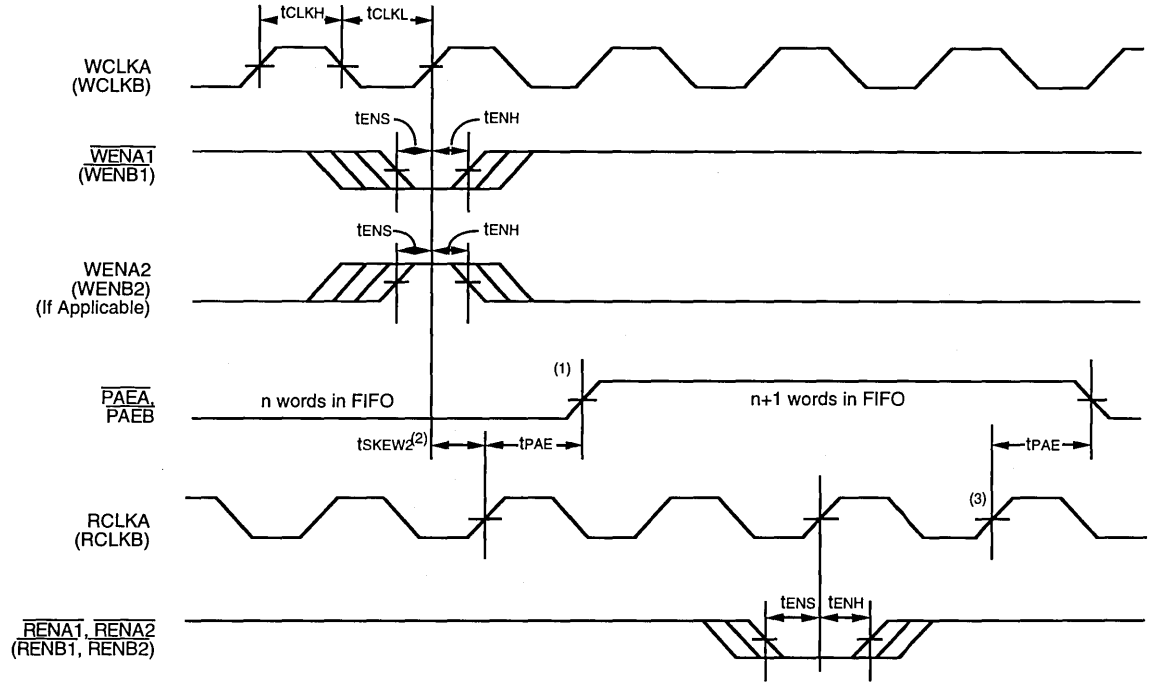
5



Notes:

1. PAF offset = m.
2. (256-m) words for the 72801, (512-m) words the 72811, (1024-m) words for the 72821, (2048-m) words for the 72831, or (4096-m) words for the 72841.
3. t_{SKEW2} is the minimum time between a rising RCLKA (RCLKB) edge and a rising WCLKA (WCLKB) edge for $\overline{PAFA}$ ($\overline{PAFB}$) to change during that clock cycle. If the time between the rising edge of RCLKA (RCLKB) and the rising edge of WCLKA (WCLKB) is less than t_{SKEW2}, then $\overline{PAFA}$ ($\overline{PAFB}$) may not change state until the next WCLKA (WCLKB) rising edge.
4. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words in FIFO A (B) when $\overline{PAFA}$ ($\overline{PAFB}$) goes LOW.

Figure 10. Programmable Full Flag Timing



3034 drw 13

NOTES:
1. PAE offset = n.
2. t_{SKEW2} is the minimum time between a rising WCLKA (WCLKB) edge and a rising RCLKA (RCLKB) edge for $\overline{PAEA}$ ($\overline{PAEB}$) to change during that clock cycle. If the time between the rising edge of WCLKA (WCLKB) and the rising edge of RCLKA (RCLKB) is less than t_{SKEW2}, then $\overline{PAEA}$ ($\overline{PAEB}$) may not change state until the next RCLKA (RCLKB) rising edge.
3. If a read is performed on this rising edge of the read clock, there will be Empty + (n-1) words in FIFO A (B) when $\overline{PAEA}$ ($\overline{PAEB}$) goes LOW.

Figure 11. Programmable Empty Flag Timing

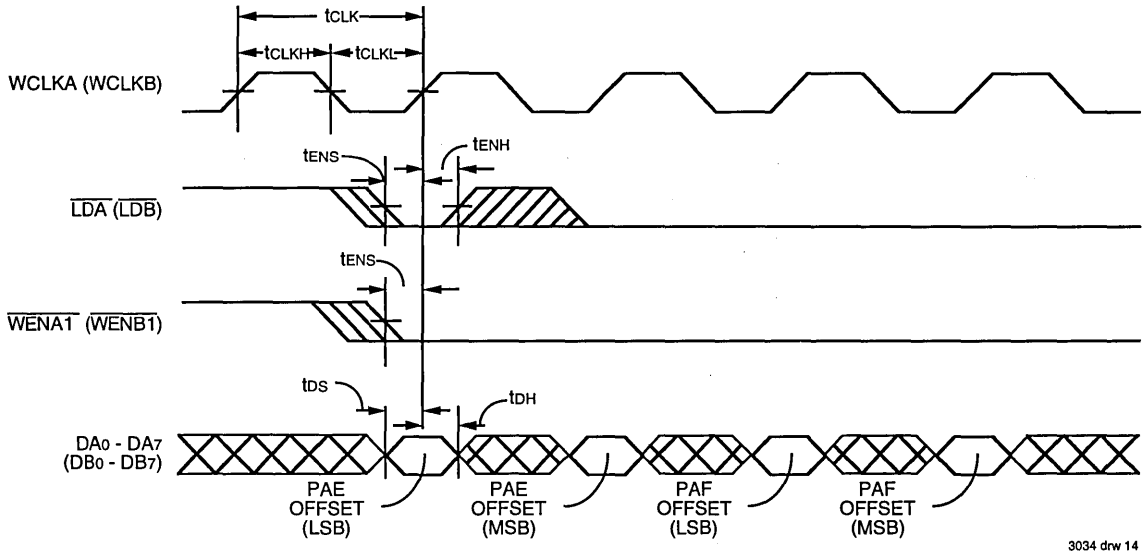


Figure 12. Write Offset Register Timing

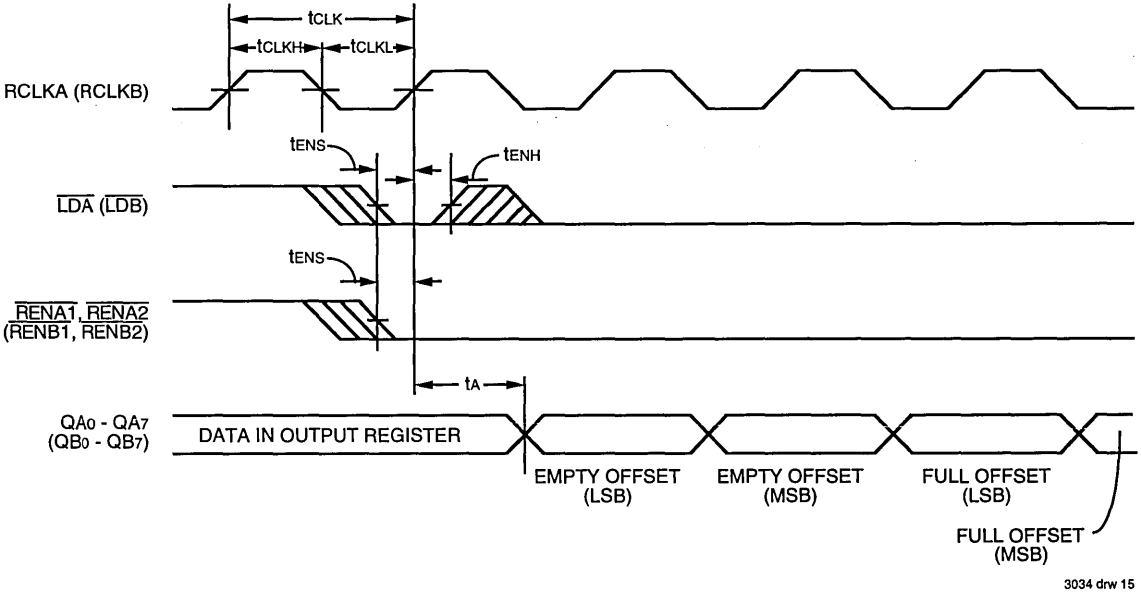


Figure 13. Read Offset Register Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION — When FIFO A (B) is in a Single Device Configuration, the Read Enable 2 $\overline{RENA2}$ ($\overline{RENB2}$) control input can be grounded (see Figure 14). In this configuration, the Write Enable 2/Load WENA2/$\overline{LDA}$ (WENB2/$\overline{LDB}$) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

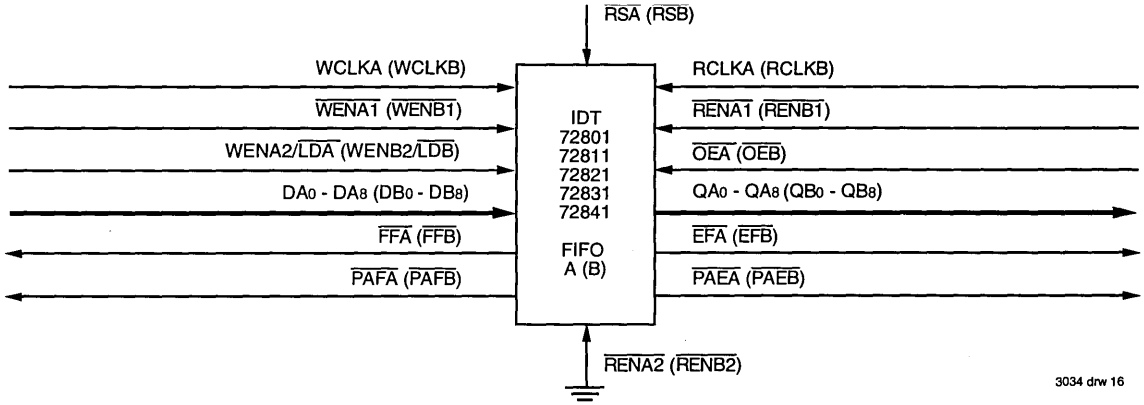


Figure 14. Block Diagram of One of the 72801/72811/72821/72831/72841's two FIFOs configured as a single device

WIDTH EXPANSION CONFIGURATION — Word width may be increased simply by connecting the corresponding input control signals of FIFOs A and B. A composite flag should be created for each of the end-point status flags $\overline{EFA}$ and $\overline{EFB}$, also $\overline{FFA}$ and $\overline{FFB}$). The partial status flags $\overline{PAEA}$, $\overline{PAFB}$, $\overline{PAEA}$ and $\overline{PAFB}$ can be detected from any one device. Figure 15 demonstrates an 18-bit word width using the two FIFOs contained in one IDT72801/72811/72821/72831/72841. Any word width can be attained by adding additional IDT2801/72811/72821/72831/72841s.

When the IDT2801/72811/72821/72831/72841 is in a Width Expansion Configuration, the Read Enable 2 ($\overline{RENA2}$ and $\overline{RENB2}$) control inputs can be grounded (see Figure 15). In this configuration, the Write Enable 2/Load (WENA2/$\overline{LDA}$, WENB2/$\overline{LDB}$) pins are set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

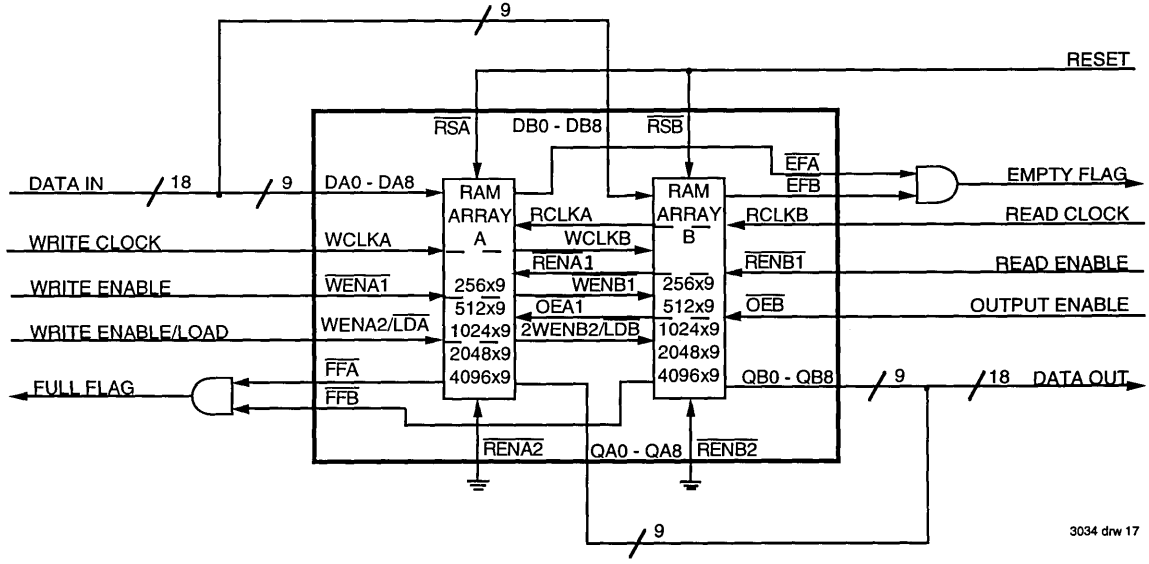


Figure 15. Block diagram of the two FIFOs contained in one 72801/72811/72821/72831/72841configured for an 18-bit width-expansion

TWO PRIORITY DATA BUFFER CONFIGURATION

The two FIFOs contained in the IDT2801/72811/72821/72831/72841 can be used to prioritize two different types of data shared on a system bus. When writing from the bus to the FIFO, control logic sorts the intermixed data according to type, sending one kind to FIFO A and the other kind to FIFO B. Then, at the outputs, each data type is transferred to its appropriate destination. Additional IDT2801/72811/72821/72831/72841s permit more than two priority levels. Priority buffering is particularly useful in network applications.

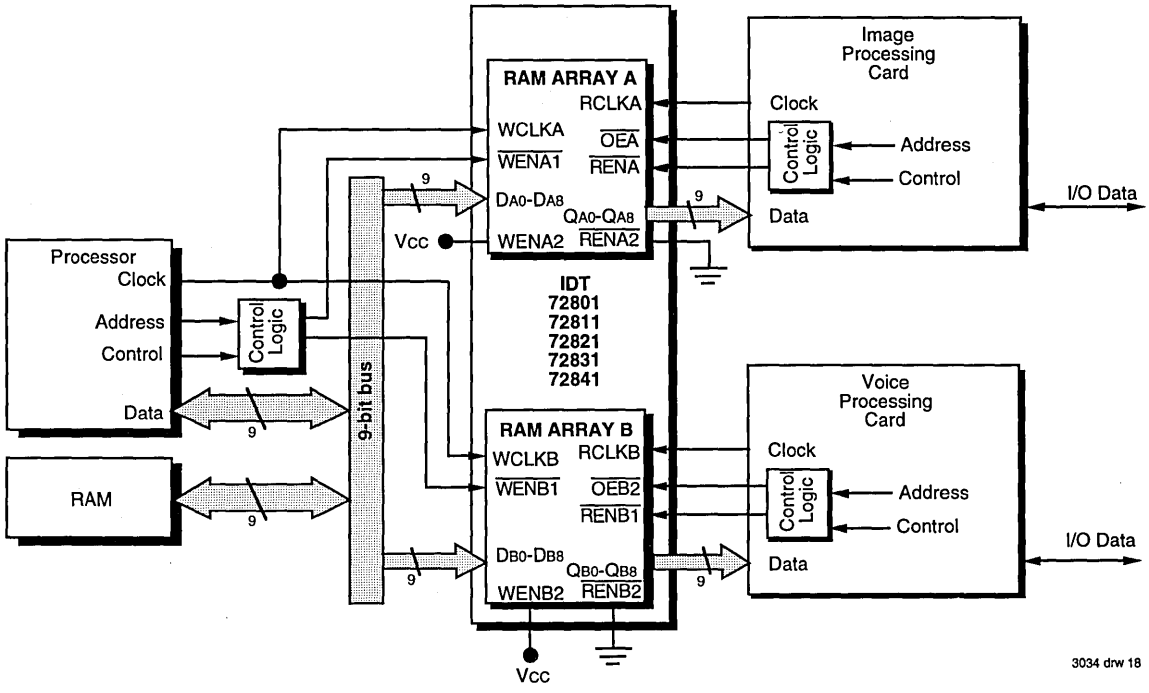


Figure 16. Block Diagram of Two Priority Configuration

BIDIRECTIONAL CONFIGURATION

The two FIFOs of the IDT2801/72811/72821/72831/72841 can be used to buffer data flow in two directions. In the example that follows, a processor can write data to a peripheral controller via FIFO A, and, in turn, the peripheral controller can write the processor via FIFO B.

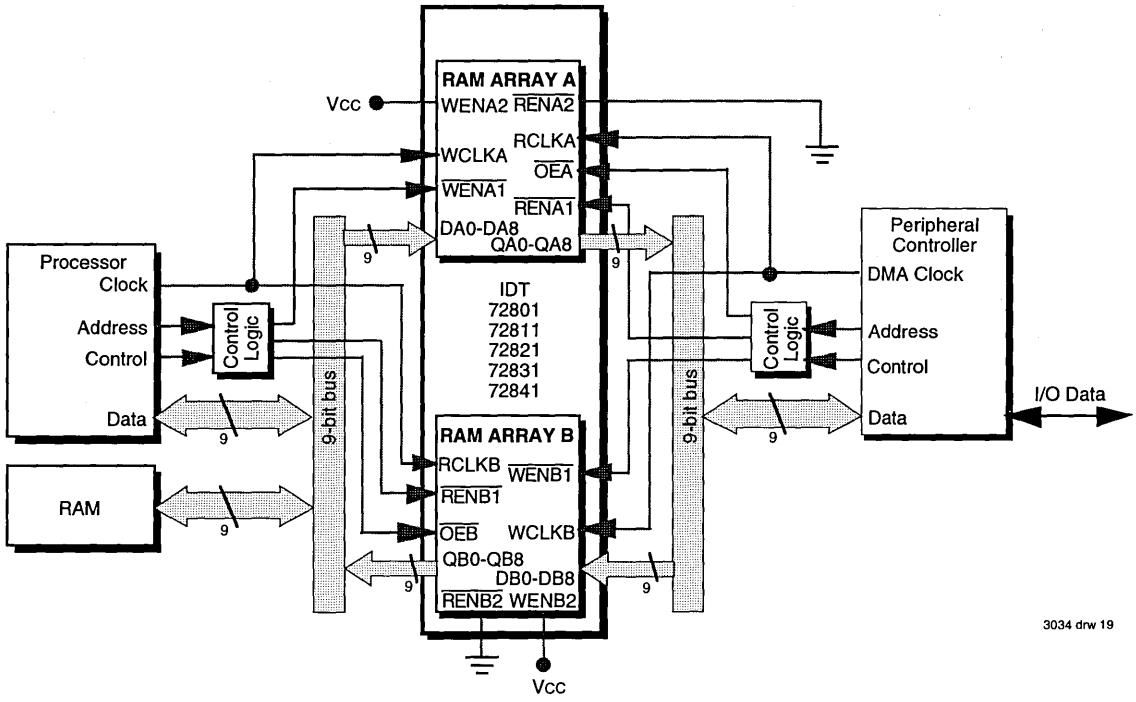


Figure 17. Block Diagram of Bidirectional Configuration

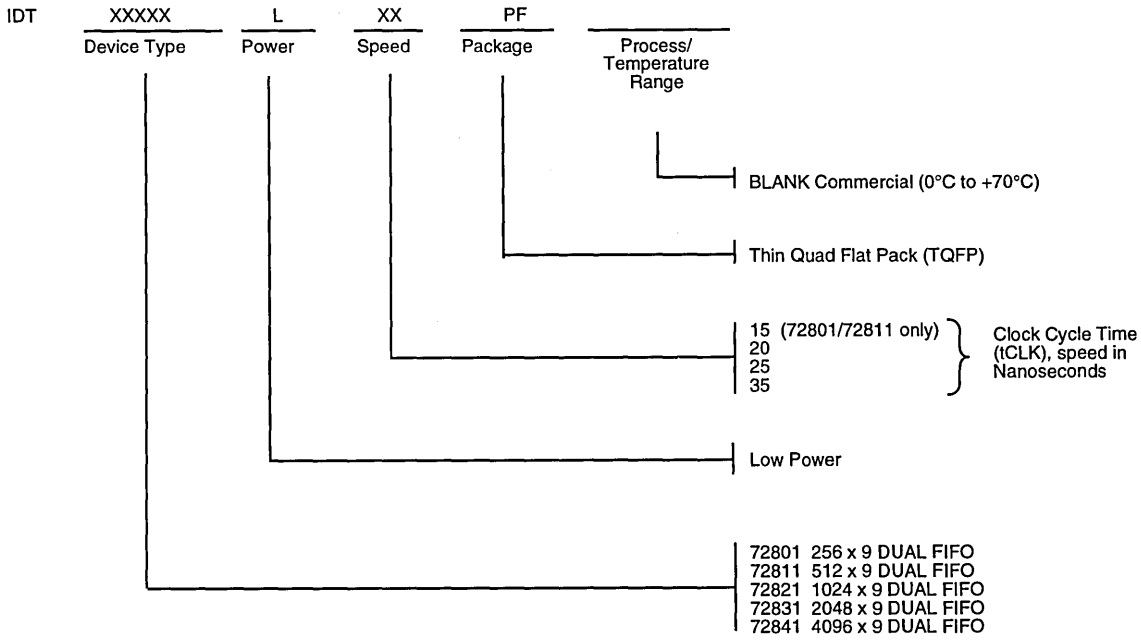
5

DEPTH EXPANSION — IDT2801/72811/72821/72831/72841 can be adapted to applications that require greater than 256/512/1024/2048/4096 words. The existence of double enable pins on the read and write ports allow depth expansion. The Write Enable 2/Load (WENA2, WENB2) pins are used as a second write enables in a depth expansion configuration, thus the Programmable flags are set to the default values. Depth expansion is possible by using one enable input for system control while the other enable input is controlled by expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data access from one device to the next in a sequential manner. The IDT2801/72811/72821/72831/72841 operates in the Depth Expansion configuration when the following conditions are met:

1. WENA2/$\overline{LDA}$ and WENB2/$\overline{LDB}$ pins are held HIGH during Reset so that these pins operate as second Write Enables.
2. External logic is used to control the flow of data.

Please see the Application Note" DEPTH EXPANSION OF IDT'S SYNCHRONOUS FIFOs USING THE RING COUNTER APPROACH" for details of this configuration.

ORDERING INFORMATION



3034 drw 20

Integrated Device Technology, Inc.

CMOS SyncFIFO™ 256 x 18, 512 x 18, 1024 x 18, 2048 x 18 and 4096 x 18

IDT72205LB
IDT72215LB
IDT72225LB
IDT72235LB
IDT72245LB

FEATURES:

- 256 x 18-bit organization array (72205LB)
- 512 x 18-bit organization array (72215LB)
- 1024 x 18-bit organization array (72225LB)
- 2048 x 18-bit organization array (72235LB)
- 4096 x 18-bit organization array (72245LB)
- 15 ns read/write cycle time
- Easily expandable in depth and width
- Read and write clocks can be asynchronous or coincident
- Dual-Port zero fall-through time architecture
- Programmable almost-empty and almost-full flags
- Empty and Full flags signal FIFO status
- Half-Full flag capability in a single device configuration
- Output enable puts output data bus in high-impedance state
- High-performance submicron CMOS technology
- Available in a 64-lead thin quad flatpack (TQFP), pin grid array (PGA), and plastic leaded chip carrier (PLCC)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72205LB/72215LB/72225LB/72235LB/72245LB are very high-speed, low-power First-In, First-Out (FIFO) memories with clocked read and write controls. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, Local Area Networks (LANs), and interprocessor communication.

Both FIFOs have 18-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and a data input enable pin ($\overline{WEN}$). Data is read into the synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and another enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual-clock operation. An Output Enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

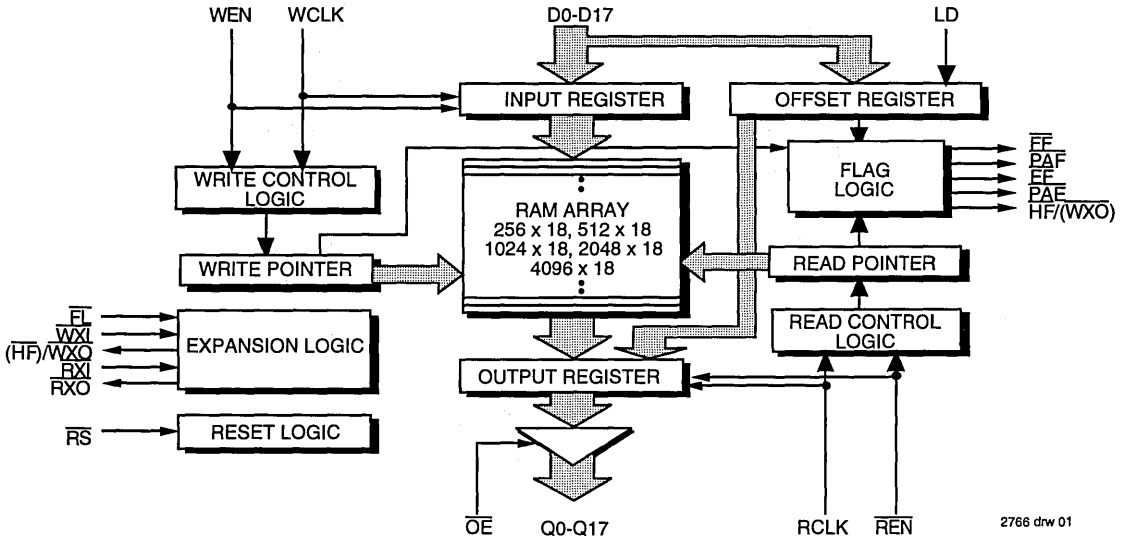
The synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$), and two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$). The offset loading of the programmable flags is controlled by a simple state machine, and is initiated by asserting the Load pin ($\overline{LD}$). A Half-Full flag ($\overline{HF}$) is available when the FIFO is used in a single device configuration.

The IDT72205LB/72215LB/72225LB/72235LB/72245LB are depth expandable using a daisy-chain technique. The XI and $\overline{XO}$ pins are used to expand the FIFOs. In depth expansion configuration, FL is grounded on the first device and set to HIGH for all other devices in the daisy chain.

The IDT72205LB/72215LB/72225LB/72235LB/72245LB is fabricated using IDT's high-speed submicron CMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

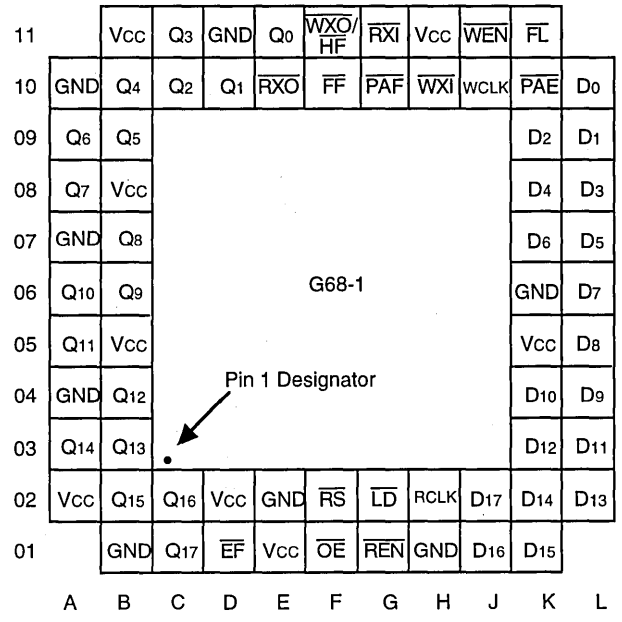
5

FUNCTIONAL BLOCK DIAGRAM

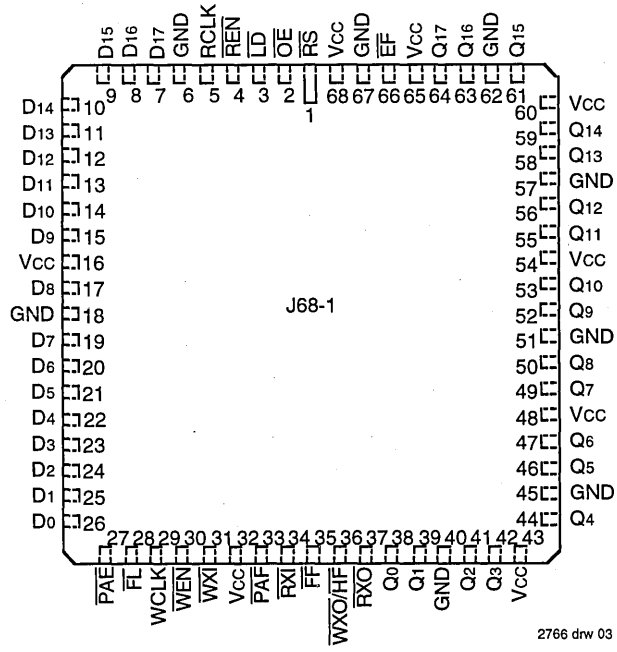


SyncFIFO is a trademark and the IDT logo is a registered trademark of Integrated Device Technology, Inc

PIN CONFIGURATIONS

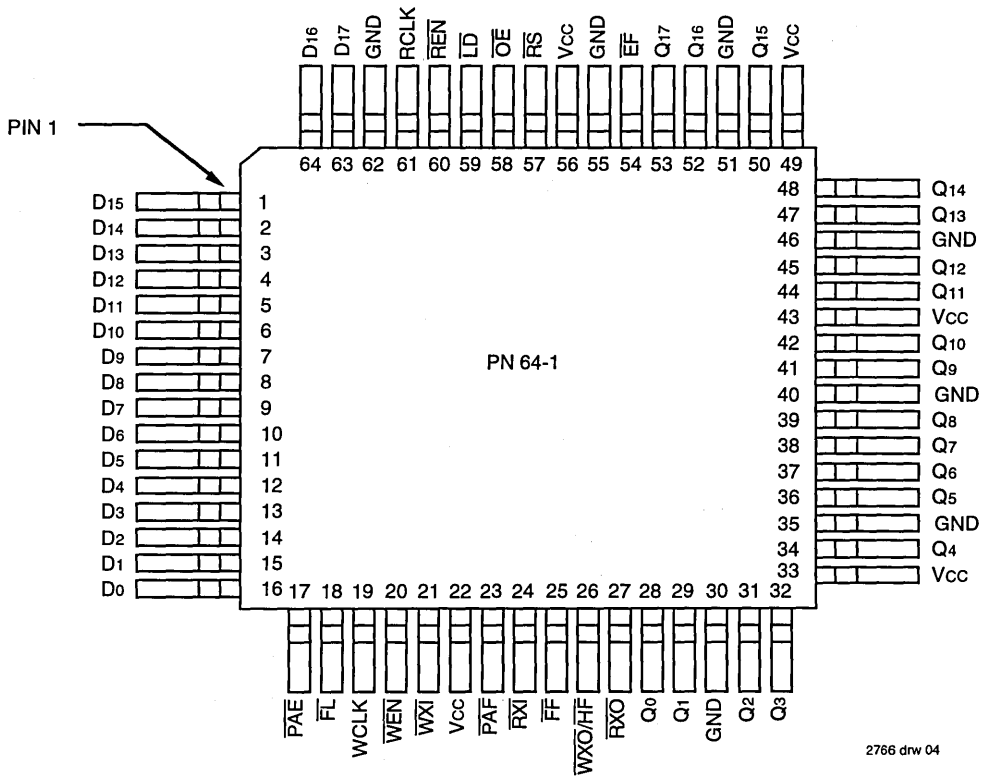


PGA
TOP VIEW



PLCC
TOP VIEW

PIN CONFIGURATIONS



TQFP
TOP VIEW

NOTE:
1. For information on the flatpack (F68-1), contact factory.

5

PIN DESCRIPTION

Symbol	Name	I/O	Description
D0–D17	Data Inputs	I	Data inputs for a 18-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go HIGH, and $\overline{PAE}$ and $\overline{EF}$ go LOW. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on a LOW-to-HIGH transition of WCLK, if the FIFO is not full.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is HIGH, the FIFO holds the previous data. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
RCLK	Read Clock	I	When $\overline{REN}$ is LOW, data is read from the FIFO on a LOW-to-HIGH transition of RCLK, if the FIFO is not empty.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is HIGH, the output register holds the previous data. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high-impedance state.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, data on the inputs D0–D11 is written to the offset and depth registers on the LOW-to-HIGH transition of the WCLK, when $\overline{WEN}$ is LOW. When $\overline{LD}$ is LOW, data on the outputs Q0–Q11 is read from the offset and depth registers on the LOW-to-HIGH transition of the RCLK, when $\overline{REN}$ is LOW.
$\overline{FL}$	First Load	I	In the single device or width expansion configuration, $\overline{FL}$ is grounded. In the depth expansion configuration, $\overline{FL}$ is grounded on the first device (first load device) and set to HIGH for all other devices in the daisy chain.
$\overline{WXI}$	Write Expansion Input	I	In the single device or width expansion configuration, $\overline{WXI}$ is grounded. In the depth expansion configuration, $\overline{WXI}$ is connected to $\overline{WXO}$ (Write Expansion Out) of the previous device.
$\overline{RXI}$	Read Expansion Input	I	In the single device or width expansion configuration, RXI is grounded. In the depth expansion configuration, $\overline{RXI}$ is connected to $\overline{RXO}$ (Read Expansion Out) of the previous device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is 31 from empty for 72205LB, 63 from empty for 72215LB, and 127 from empty for 72225LB/72235LB/72245LB.
$\overline{PAF}$	Programmable	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is 31 from full for 72205LB, 63 from full for 72215LB, and 127 from full for 72225LB/72235LB/72245LB.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{WXO}/\overline{HF}$	Write Expansion Out/Half-Full Flag	O	In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is LOW. In the depth expansion configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device when the last location in the FIFO is written.
$\overline{RXO}$	Read Expansion Out	O	In the depth expansion configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next device when the last location in the FIFO is read.
Q0–Q17	Data Outputs	O	Data outputs for a 18-bit bus.
VCC	Power		Eight +5V power supply pins for the PLCC and PGA, five pins for the TQFP.
GND	Ground		Eight ground pins for the PLCC and PGA, seven pins for the TQFP.

2766 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Mlilitary	Unit
VTERM	Terminal Voltage with respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2766 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maimum rating conditions for extended

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIH	Input High Voltage Military	2.2	—	—	V
VIL(1)	Input Low Voltage Commercial & Military	—	—	0.8	V

NOTE: 2766 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Military: VCC = 5V ± 10%, TA = –55°C to +125°C)

		IDT72205LB IDT72215LB IDT72225LB IDT72235LB IDT72245LB Commercial tCLK = 15, 20, 25, 35, 50ns			IDT72205LB IDT72215LB IDT72225LB IDT72235LB IDT72245LB Military tCLK = 25, 35, 50ns			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
ILI(1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
ILO(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = –2 mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8 mA	—	—	0.4	—	—	0.4	V
ICC1(3)	Active Power Supply Current	—	—	200	—	—	250	mA
ICC2(3)	Average Standby Current (All Input = VCC – 0.2V, except RCLK and WCLK which are free-running)	—	—	70	—	—	85	mA

NOTES: 2766 tbl 04

1. Measurements with 0.4 ≤ VIN ≤ VCC.
2. $\overline{OE}$ ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. Tested at f = 20MHz with outputs open.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN(2)	Input Capacitance	VIN = 0V	10	pF
COUT(1,2)	Output Capacitance	VOUT = 0V	10	pF

NOTES: 2766 tbl 05

1. With output deselected, ($\overline{OE}$ = HIGH).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = −55°C to +125°C)

		Commercial				Commercial and Military						
		72205LB15 72215LB15 72225LB15 72235LB15 72245LB15		72205LB20 72215LB20 72225LB20 72235LB20 72245LB20		72205LB25 72215LB25 72225LB25 72235LB25 72245LB25		72205LB35 72215LB35 72225LB35 72235LB35 72245LB35		72205LB50 72215LB50 72225LB50 72235LB50 72245LB50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Clock Cycle Frequency	—	66.7	—	50	—	40	—	28.6	—	20	MHz
tA	Data Access Time	2	10	2	12	3	15	3	20	3	25	ns
tCLK	Clock Cycle Time	15	—	20	—	25	—	35	—	50	—	ns
tCLKH	Clock HIGH Time	6.5	—	8	—	10	—	14	—	20	—	ns
tCLKL	Clock LOW Time	6.5	—	8	—	10	—	14	—	20	—	ns
tDS	Data Set-up Time	4	—	5	—	6	—	7	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	2	—	2	—	ns
tENS	Enable Set-up Time	4	—	5	—	6	—	7	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	2	—	2	—	ns
tRS	Reset Pulse Width[1]	15	—	20	—	25	—	35	—	50	—	ns
tRSS	Reset Set-up Time	10	—	12	—	15	—	20	—	30	—	ns
tRSR	Reset Recovery Time	10	—	12	—	15	—	20	—	30	—	ns
tRSF	Reset to Flag and Output Time	—	35	—	35	—	40	—	45	—	50	ns
tOLZ	Output Enable to Output in Low-Z[2]	0	—	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	—	8	—	9	—	12	—	15	—	20	ns
tOHZ	Output Enable to Output in High-Z[2]	1	8	1	9	1	12	1	15	1	20	ns
tWFF	Write Clock to Full Flag	—	10	—	12	—	15	—	20	—	30	ns
tREF	Read Clock to Empty Flag	—	10	—	12	—	15	—	20	—	30	ns
tPAF	Clock to Programmable Almost-Full Flag	—	28	—	30	—	35	—	40	—	40	ns
tPAE	Clock to Programmable Almost-Empty Flag	—	28	—	30	—	35	—	40	—	40	ns
tHF	Clock to Half-Full Flag	—	28	—	30	—	35	—	40	—	40	ns
tXO	Clock to Expansion Out	—	10	—	12	—	15	—	20	—	30	ns
tXI	Expansion In Pulse Width	6.5	—	8	—	10	—	14	—	20	—	ns
tXIS	Expansion In Set-Up Time	5	—	8	—	10	—	15	—	20	—	ns
tSKEW1	Skew time between Read Clock & Write Clock for Full Flag	10	—	14	—	16	—	18	—	20	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Empty Flag	10	—	14	—	16	—	18	—	20	—	ns

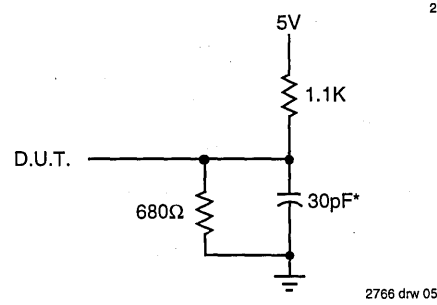
NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

2766 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2766 tbl 07



2766 drw 05

Figure 1. Output Load
* Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0 - D_{17})

Data inputs for 18-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag ($\overline{FF}$), Half-Full Flag ($\overline{HF}$), and Programmable Almost-Full Flag ($\overline{PAF}$) will be reset to HIGH after t_{RSF}. The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) will be reset to LOW after t_{RSF}. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

WRITE CLOCK (WCLK)

A write cycle is initiated on the LOW-to-HIGH transition of the write clock (WCLK). Data set-up and hold times must be met with respect to the LOW-to-HIGH transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

WRITE ENABLE ($\overline{WEN}$)

When Write Enable ($\overline{WEN}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

When $\overline{WEN}$ is HIGH, the input register holds the previous data and no new data is loaded into the FIFO.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the $\overline{FF}$ will go HIGH after t_{WFF} allowing a write to begin. $\overline{WEN}$ is ignored when the FIFO is full.

READ CLOCK (RCLK)

Data can be read on the outputs on the LOW-to-HIGH transition of the read clock (RCLK), when Output Enable ($\overline{OE}$) is set LOW.

The write and read clocks can be asynchronous or coincident.

READ ENABLE ($\overline{REN}$)

When Read Enable ($\overline{REN}$) is LOW, data is loaded into the RAM array to the output register on the LOW-to-HIGH transition of the read clock (RCLK).

When $\overline{REN}$ is HIGH, the output register holds the previous data and no new data is loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. Once a write is performed, the $\overline{EF}$ will go HIGH after t_{REF} and a read can begin. $\overline{REN}$ is ignored when the FIFO is empty.

OUTPUT ENABLE ($\overline{OE}$)

When Output Enable ($\overline{OE}$) is enabled (LOW), the parallel output buffers receive data from the output register. When $\overline{OE}$ is disabled (HIGH), the Q output data bus is in a high-impedance state.

LOAD ($\overline{LD}$)

The IDT72205LB/72215LB/72225LB/72235LB/72245LB devices contain two 12-bit offset registers with data on the inputs, or read on the outputs. When the Load ($\overline{LD}$) pin is set LOW and $\overline{WEN}$ is set LOW, data on the inputs D0-D11 is written into the Empty offset register on the first LOW-to-HIGH transition of the write clock (WCLK). When the $\overline{LD}$ pin and ($\overline{WEN}$) are held LOW then data is written into the Full offset register on the second LOW-to-HIGH transition of the write clock (WCLK). The third transition of the write clock (WCLK) again writes to the Empty offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the $\overline{LD}$ pin HIGH, the FIFO is returned to normal read/write operation. When the LD pin is set LOW, and $\overline{WEN}$ is LOW, the next offset register in sequence is written.

When the $\overline{LD}$ pin is LOW and $\overline{WEN}$ is HIGH, the WCLK input is disabled; then a signal at this input can neither increment the write offset register pointer, nor execute a write.

The contents of the offset registers can be read on the output lines when the $\overline{LD}$ pin is set LOW and $\overline{REN}$ is set LOW; then, data can be read on the LOW-to-HIGH transition of the read clock (RCLK). The act of reading the control registers employs a dedicated read offset register pointer. (The read and write pointers operate independently).

A read and a write should not be performed simultaneously to the offset registers.

LD	WEN	WCLK[1]	Selection
0	0		Writing to offset registers: Empty Offset Full Offset 
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

NOTE: 2766 tbl 08

1. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Figure 2. Write Offset Register

First Load (FL)

First Load ($\overline{FL}$) is grounded to indicate operation in the Single Device or Width Expansion mode. In the Depth Expansion configuration, $\overline{FL}$ is grounded to indicate it is the first device loaded and is set to HIGH for all other devices in the daisy chain. (See Operating Configurations for further details.)

WRITE EXPANSION INPUT ($\overline{WXI}$)

This is a dual purpose pin. Write Expansion In ($\overline{WXI}$) is grounded to indicate operation in the Single Device or Width Expansion mode. $\overline{WXI}$ is connected to Write Expansion Out ($\overline{WXO}$) of the previous device in the Depth Expansion or Daisy Chain mode.

READ EXPANSION INPUT (RXI)

This is a dual purpose pin. Read Expansion In ($\overline{RXI}$) is grounded to indicate operation in the Single Device or Width Expansion mode. $\overline{RXI}$ is connected to Read Expansion Out ($\overline{RXO}$) of the previous device in the Depth Expansion or Daisy Chain mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

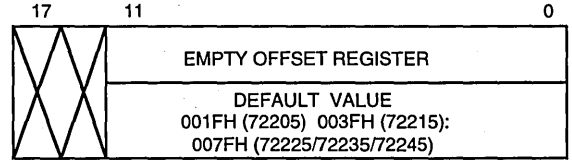
The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operation, indicating that the device is full. If no reads are performed after Reset (RS), the Full Flag ($\overline{FF}$) will go LOW after 256 writes for the IDT72205LB, 512 writes for the IDT72215LB, 1024 writes for the IDT72225LB, 2048 writes for the IDT72235LB and 4096 writes for the IDT72245LB.

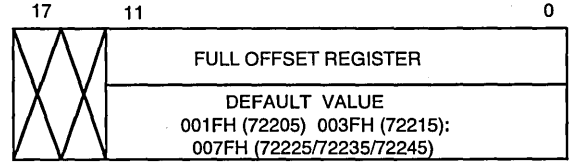
The Full Flag ($\overline{FF}$) is updated on the LOW-to-HIGH transition of the write clock (WCLK).

EMPTY FLAG (EF)

The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The $\overline{EF}$ is updated on the LOW-to-HIGH transition the read clock (RCLK).





NOTE: 2766 drw 06
1. Any bits of the offset register not being programmed should be set to zero.

Figure 3. Offset Register Location and Default Values

TABLE I — STATUS FLAGS

Number of Words in FIFO									
72205	72215	72225	72235	72245	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	0	0	H	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	1 to n[1]	1 to n[1]	H	H	H	L	H
(n + 1) to 128	(n + 1) to 256	(n + 1) to 512	(n + 1) to 1024	(n + 1) to 2048	H	H	H	H	H
129 to (256-(m+1))	257 to (512-(m+1))	513 to (1024-(m+1))	1025 to (2048-(m+1))	2049 to (4096-(m+1))	H	H	L	H	H
(256-m)[2] to 255	(512-m)[2] to 511	(1024-m)[2] to 1023	(2048-m)[2] to 2047	(4096-m)[2] to 4095	H	L	L	H	H
256	512	1024	2048	4096	L	L	L	H	H

NOTES: 2766 tbl 09
1. n = Empty Offset (Default Values : 72205 n=31, 72215 n = 63, 72225/72235/72245 n = 127)
2. m = Full Offset (Default Values : 72205 n=31, 72215 n = 63, 72225/72235/72245 n = 127)

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

The Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW when FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the $\overline{PAF}$ will go LOW after (256-m) writes for the IDT72205LB, (512-m) writes for the IDT72215LB, (1024-m) writes for the IDT72225LB, (2048–m) writes for the IDT72235LB and (4096–m) writes for the IDT72245LB. The offset "m" is defined in the FULL offset register.

If there is no Full offset specified, the $\overline{PAF}$ will be LOW when the device is 31 away from completely full for 72205LB, 63 away from completely full for 72215LB, and 127 away from completely full for 72225LB/72235LB/72245LB.

The $\overline{PAF}$ is asserted LOW on the LOW-to-HIGH transition of the write clock (WCLK). $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of the read clock (RCLK). Thus $\overline{PAF}$ is asychronous.

PROGRAMMABLE ALMOST-EMPTY FLAG (PAE)

The Programmable Almost-Empty Flag ($\overline{PAE}$) will go LOW when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the EMPTY offset register.

If there is no Empty offset specified, the Programmable Almost Empty Flag ($\overline{PAE}$) will be LOW when the device is 31 away from completely empty for 72205LB, 63 away from completely empty for 72215LB, and 127 away from completely empty for 72225LB/72235LB/72245LB.

The $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of the read clock (RCLK). $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of the write clock (WCLK). Thus $\overline{PAE}$ is asychronous.

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXO/HF}$)

This is a dual-purpose output. In the Single Device and Width Expansion mode, when Write Expansion In ($\overline{WXI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the LOW-to-HIGH transition of the next write cycle, the Half-Full Flag goes LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset to HIGH by the LOW-to-HIGH transition of the read clock (RCLK). The $\overline{HF}$ is asychronous.

In the Depth Expansion or Daisy Chain mode, $\overline{WXI}$ is connected to $\overline{WXO}$ of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device writes to the last location of memory.

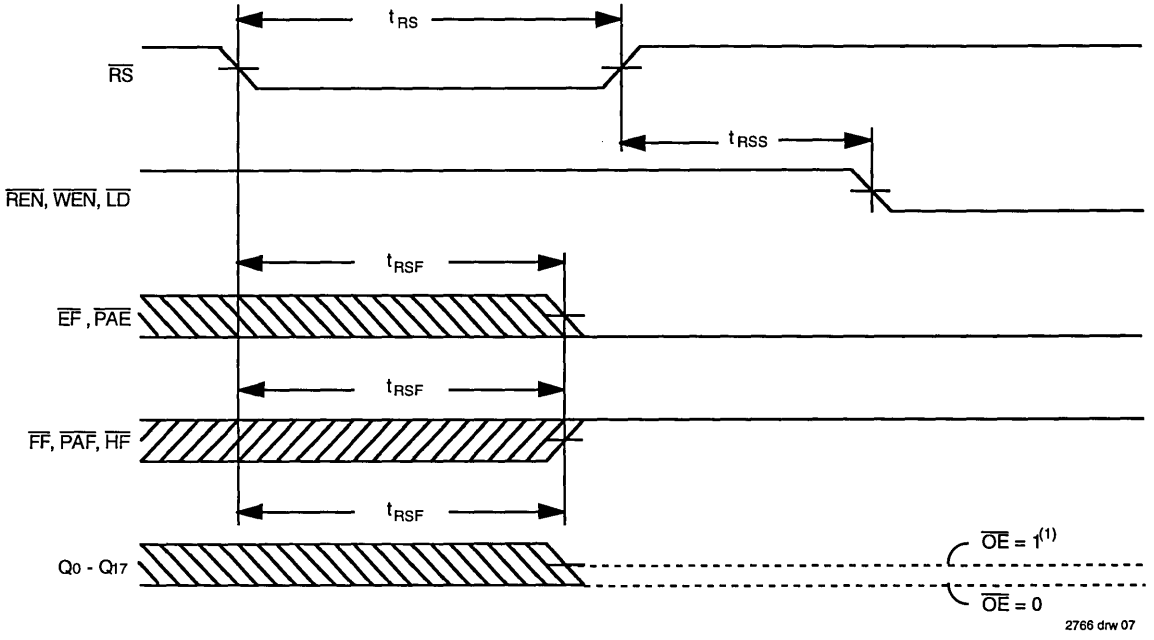
READ EXPANSION OUT ($\overline{RXO}$)

In the Depth Expansion or Daisy Chain configuration, Read Expansion In ($\overline{RXI}$) is connected to Read Expansion Out ($\overline{RXO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device reads from the last location of memory.

DATA OUTPUTS (Q0-Q17)

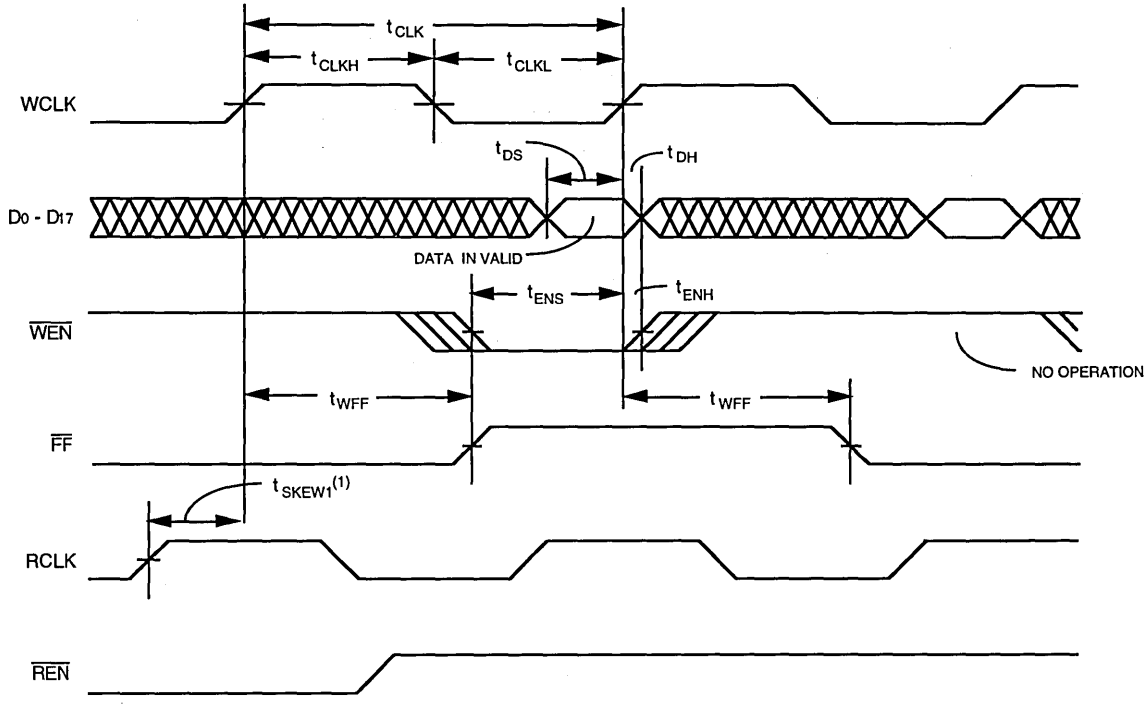
Q0-Q17 are data outputs for 18-bit wide data.

5



NOTES:
1. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

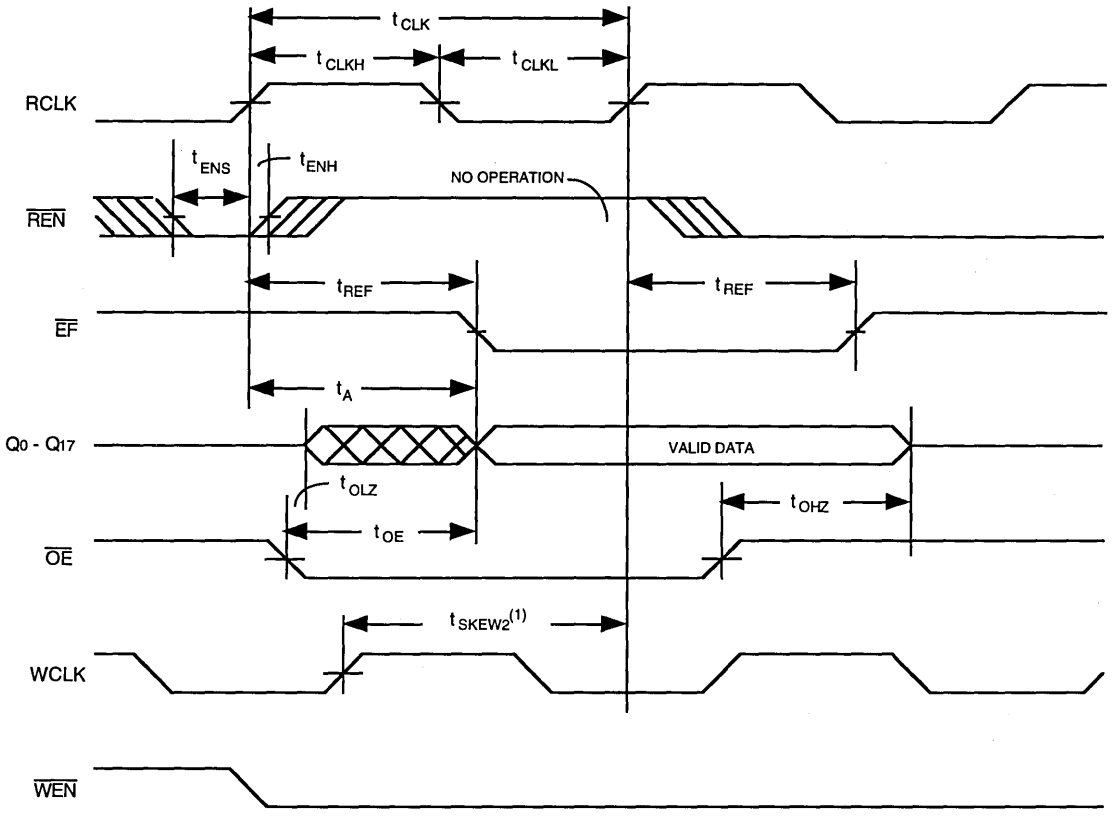
Figure 5. Reset Timing(2)



2766 drw 08

NOTE:
1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then $\overline{FF}$ may not change state until the next WCLK edge.

Figure 6. Write Cycle Timing

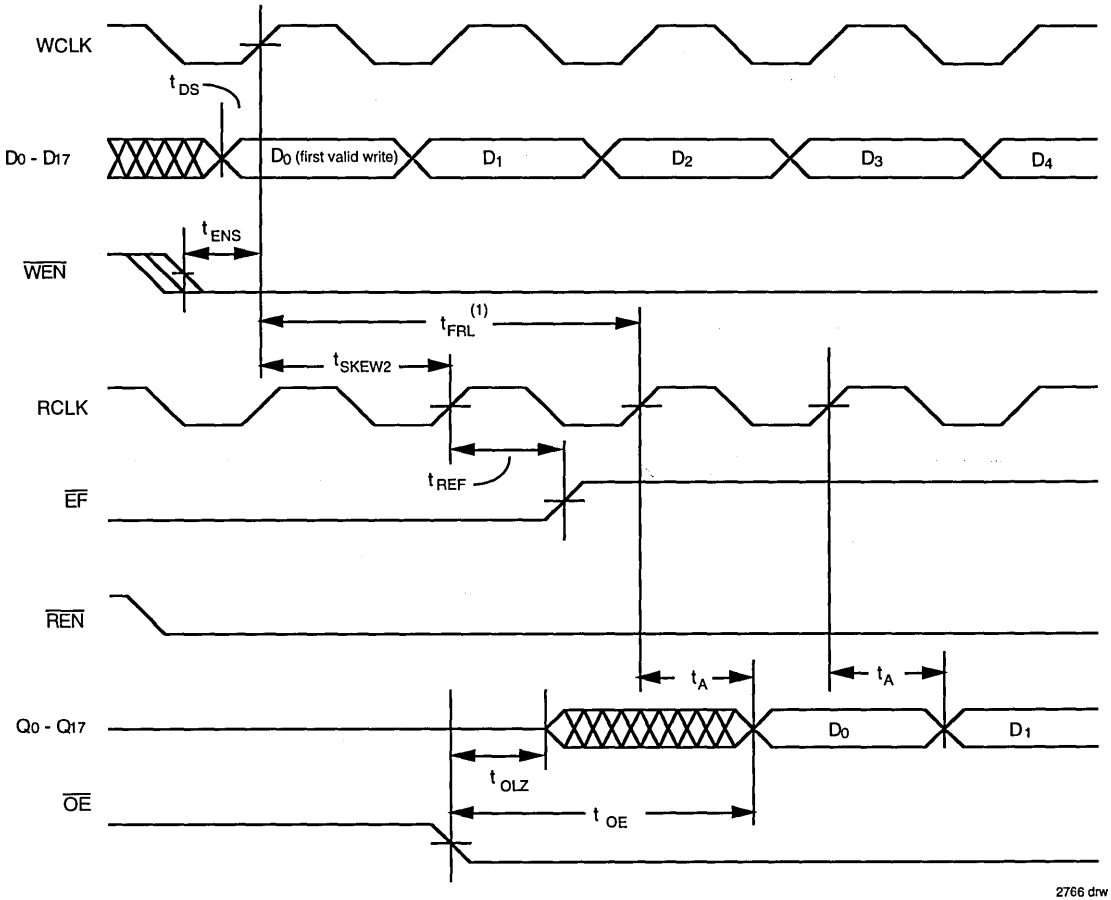


2766 drw 09

NOTE:
1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 7. Read Cycle Timing

5



NOTES:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2 * t_{CLK} + t_{SKEW2} or t_{CLK} + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
2. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

Figure 8. First Data Word Latency after Reset with Simultaneous Read and Write

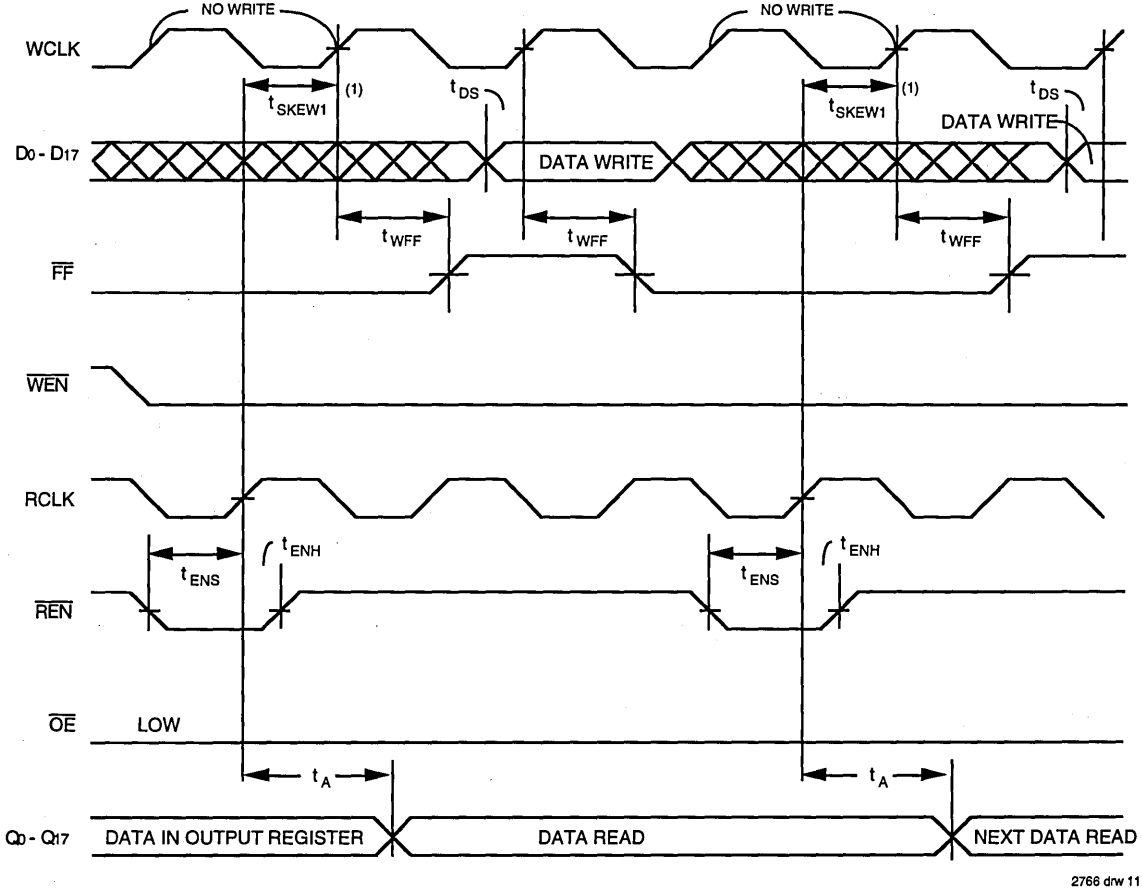


Figure 9. Full Flag Timing

NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

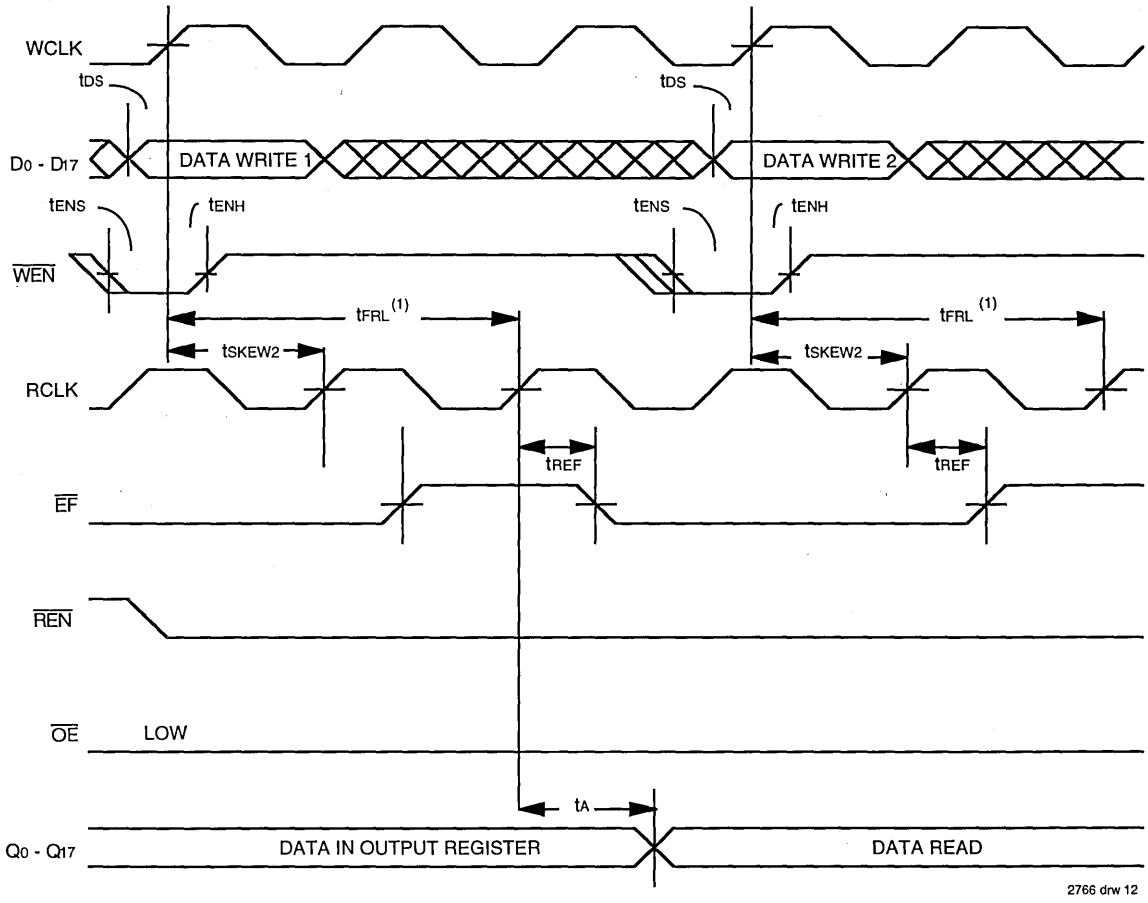


Figure 10. Empty Flag Timing

NOTE:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2 * t_{CLK} + t_{SKEW2}. or t_{CLK} + t_{SKEW2}. The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = LOW).

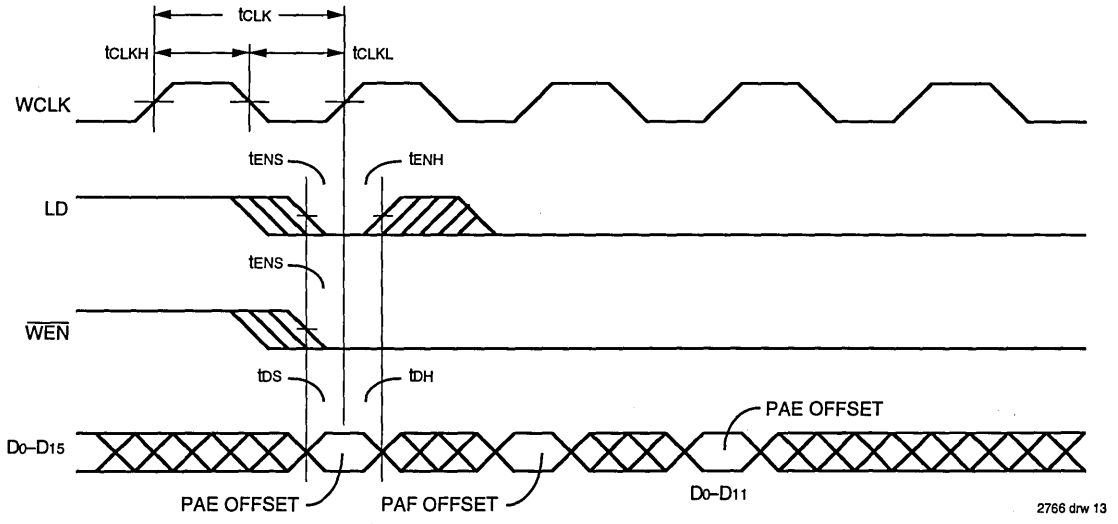


Figure 11. Write Programmable Registers

5

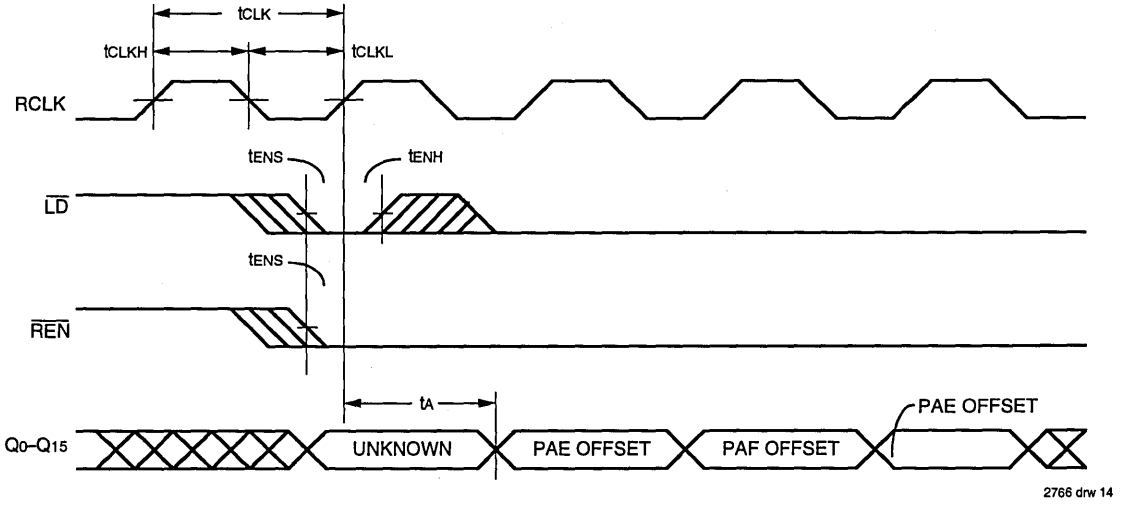
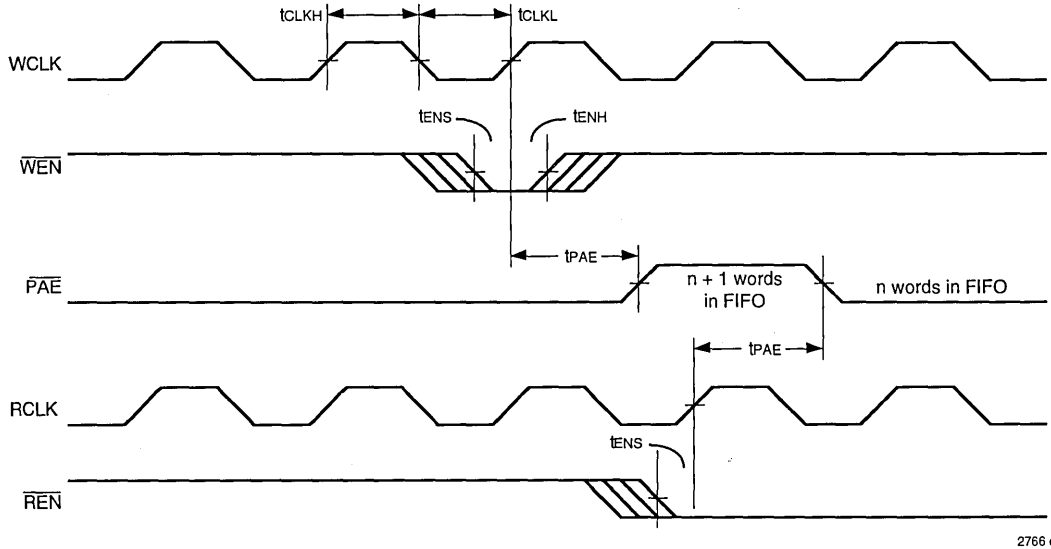
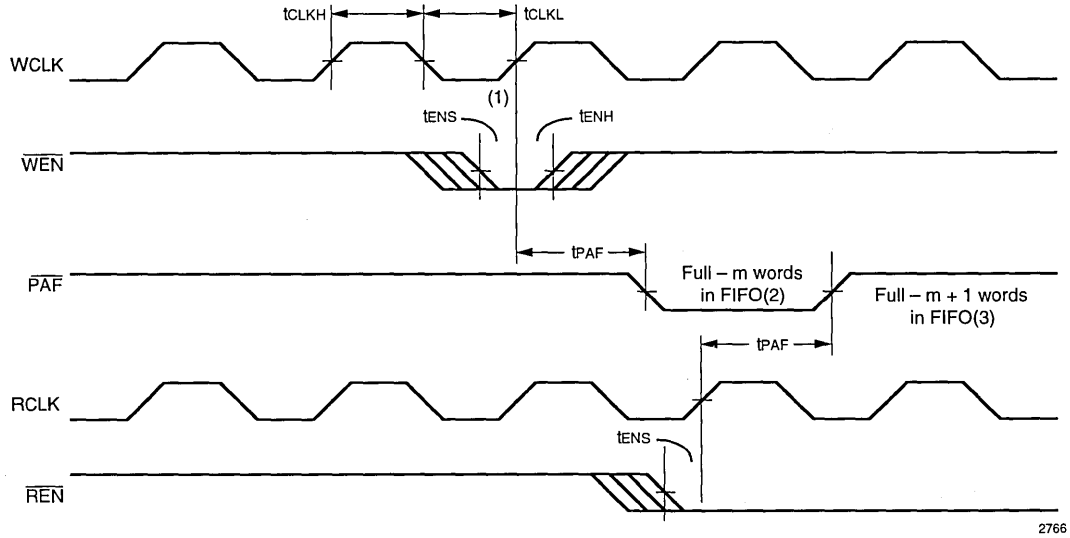


Figure 12. Read Programmable Registers



NOTE:
1. PAE is offset = n. Number of data words written into FIFO already = n.

Figure 13. Programmable Almost Empty Flag Timing



NOTES:
1. PAF offset = m. Number of data words written into FIFO already = 256 - m + 1 for the IDT72205B, 512 - m + 1 for the IDT72215B, 1024 - m + 1 for the IDT72225B, 2048 – m + 1 for the IDT72235B and 4096 – m +1 for the IDT72245B.
2. 256 - m words in IDT72205B, 512 - m words in IDT72215B, 1024 - m words in IDT72225B, 2048 – m words in IDT72235B and 4096 – m words in IDT72245B.
3. 256 - m + 1 words in IDT72205B, 512 - m + 1 words in IDT72215B, 1024 - m + 1 words in IDT72225B, 2048 – m + 1 words in IDT72235B and 4096 – m + 1 words in IDT72245B.

Figure 14. Programmable Almost-Full Flag Timing

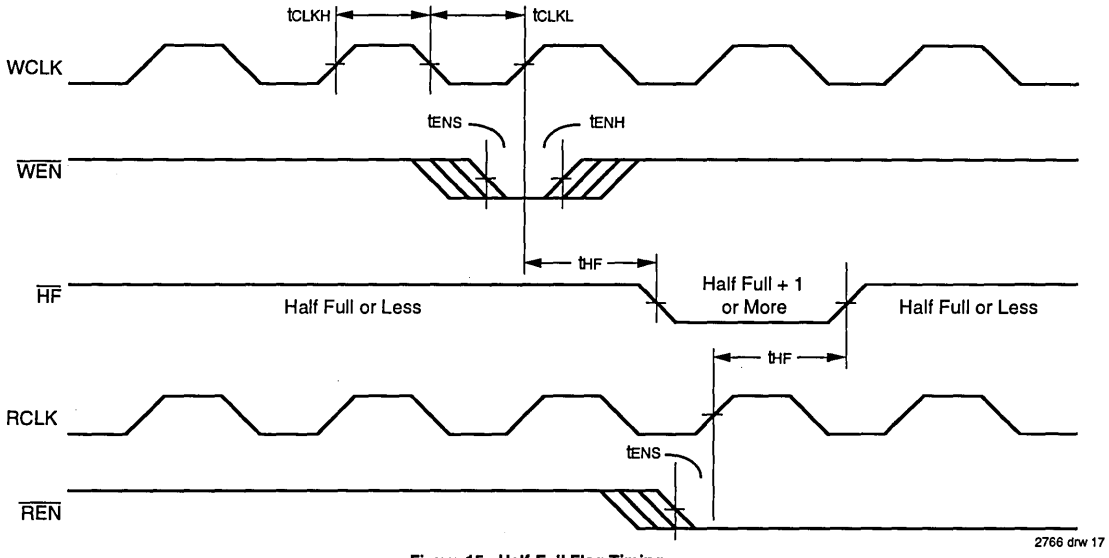
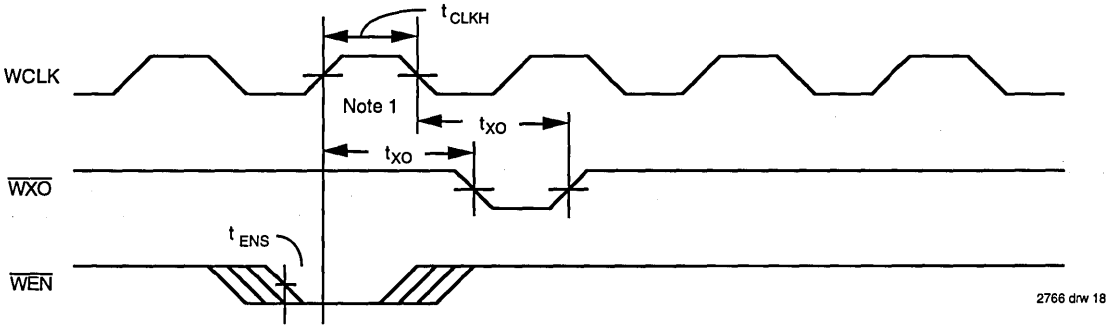
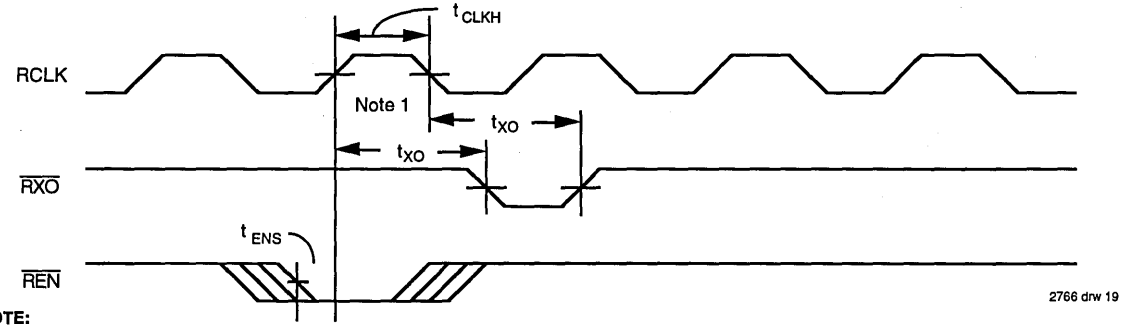


Figure 15. Half-Full Flag Timing



NOTE:
1. Write to Last Physical Location.

Figure 16. Write Expansion Out Timing



NOTE:
1. Read from Last Physical Location.

Figure 17. Read Expansion Out Timing

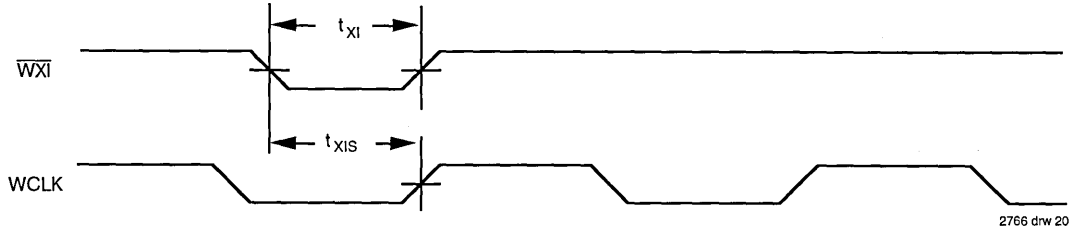


Figure 18. Write Expansion In Timing

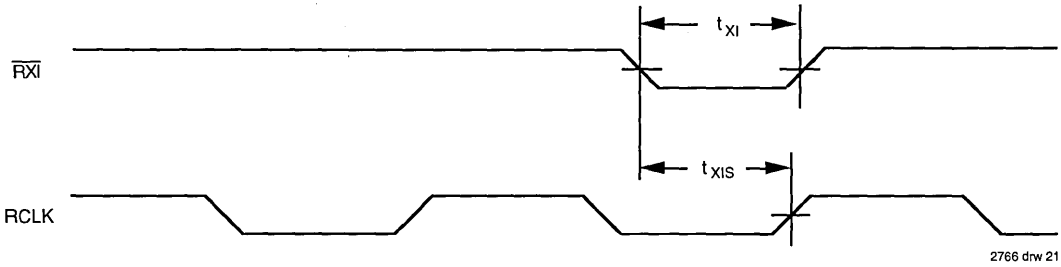


Figure 19. Read Expansion In Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

A single IDT72205LB/72215LB/72225LB/72235LB/72245LB may be used when the application requirements are for 256/512/1024/2048/4096 words or less. The IDT72205LB/72215LB/72225LB/72235LB/72245LB are in a single Device Configuration when the Write Exansion In ($\overline{WXI}$), Read Expansion In ($\overline{RXI}$), and First Load ($\overline{FL}$) control inputs are grounded (Figure 20).

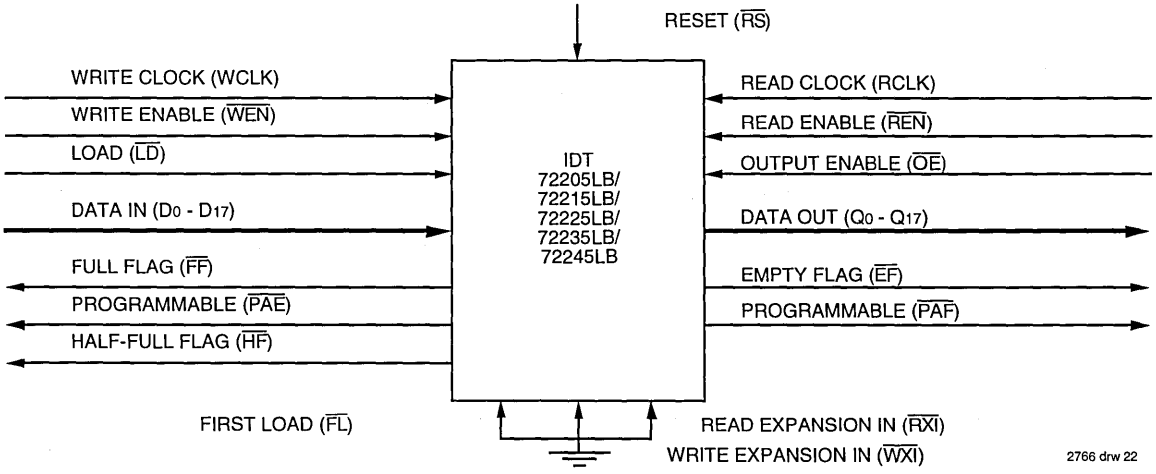
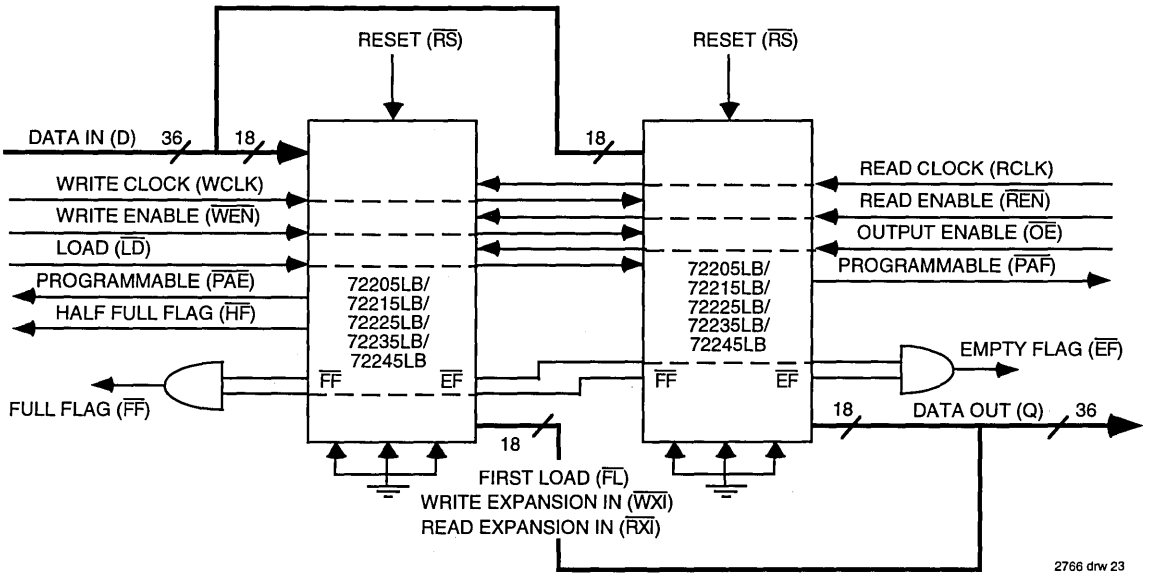


Figure 20. Block Diagram of Single 256 x 18/512 x 18/1024 x 18/2048 x 18/4096 x 18 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting together the control signals of multiple devices. Status flags can be detected from any one device. The exceptions are the Empty Flag and Full Flag. Because of variations in skew between RCLK and WCLK, it is possible for flag assertion and deassertion to vary by one cycle between FIFOs. To avoid problems the user must create composite flags by ANDing the Empty Flags of every FIFO, and separately ANDing all Full Flags. Figure 21 demonstrates a 36-word width by using two IDT72205B/72215B/72225B/72235B/72245Bs. Any word width can be attained by adding additional IDT72205B/72215B/72225B/72235B/72245Bs. Please see the Application Note AN-83.



NOTE:
1. Do not connect any output control signals directly together.

Figure 21. Block Diagram of 256 x 36/512 x 36/1024 x 36/2048 x 36/4096 x 36 Synchronous FIFO Memory Used in a Width Expansion Configuration

DEPTH EXPANSION CONFIGURATION (WITH PROGRAMMABLE FLAGS)

The IDT72205LB/72215LB/72225LB/72235LB/72245LB can easily be adapted to applications requiring more than 256/512/1024/2048/4096 words of buffering. Figure 22 shows Depth Expansion using three IDT72205LB/72215LB/72225LB/72235LB/72245LBs. Maximum depth is limited only by signal loading. Follow these steps:

1. The first device must be designated by grounding the First Load (FL) control input.
2. All other devices must have FL in the HIGH state.
3. The Write Expansion Out (WXO) pin of each device must be tied to the Write Expansion In (WXI) pin of the next device. See Figure 24.
4. The Read Expansion Out (RXO) pin of each device must be tied to the Read Expansion In (RXI) pin of the next device. See Figure 24.
5. All Load (LD) pins are tied together.
6. The Half-Full Flag (HF) is not available in the Depth Expansion Configuration.
7. EF, FF, PAE, and PAF are created with composite flags by ORing together every respective flags for monitoring. The composite PAE and PAF flags are not precise.

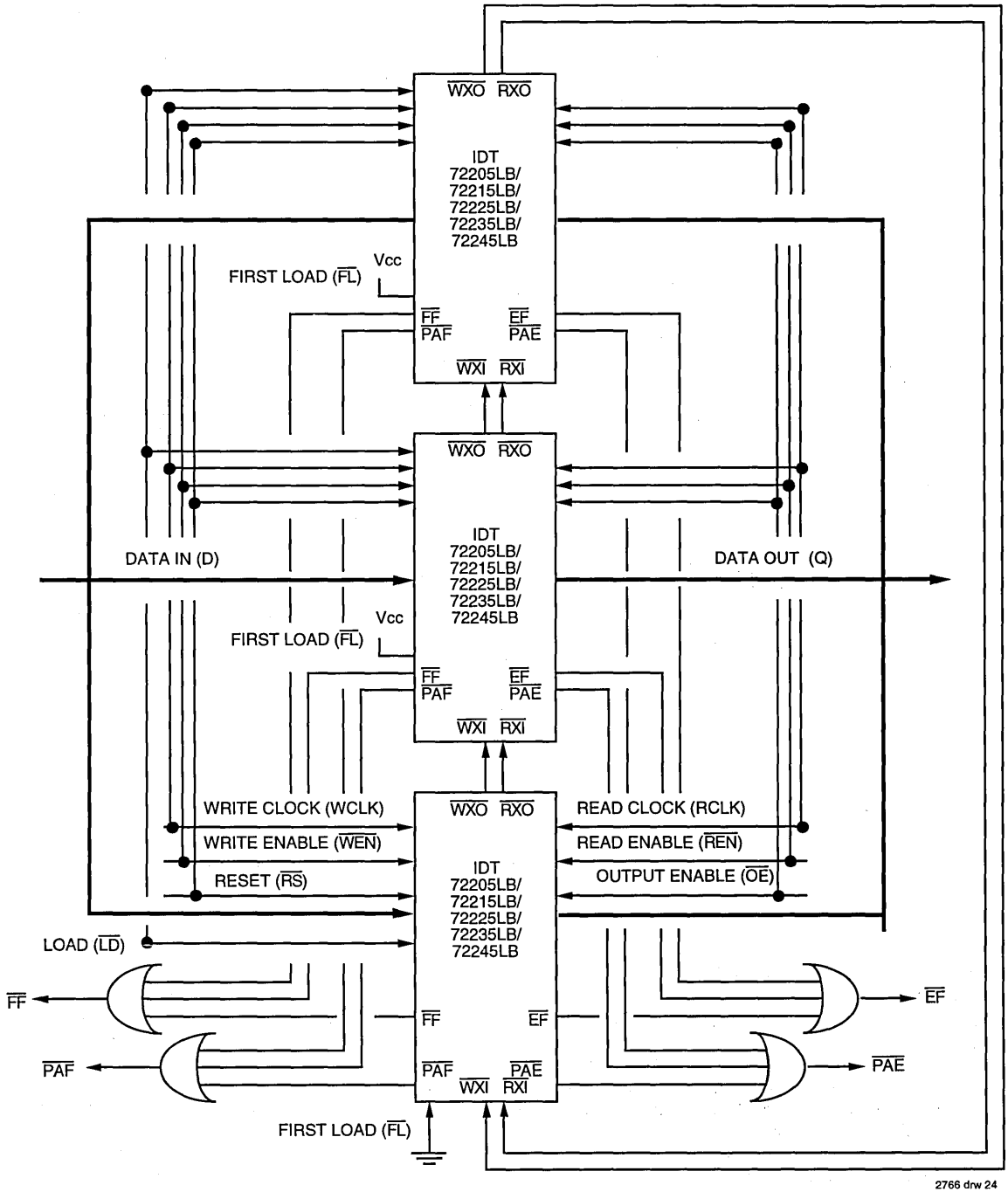
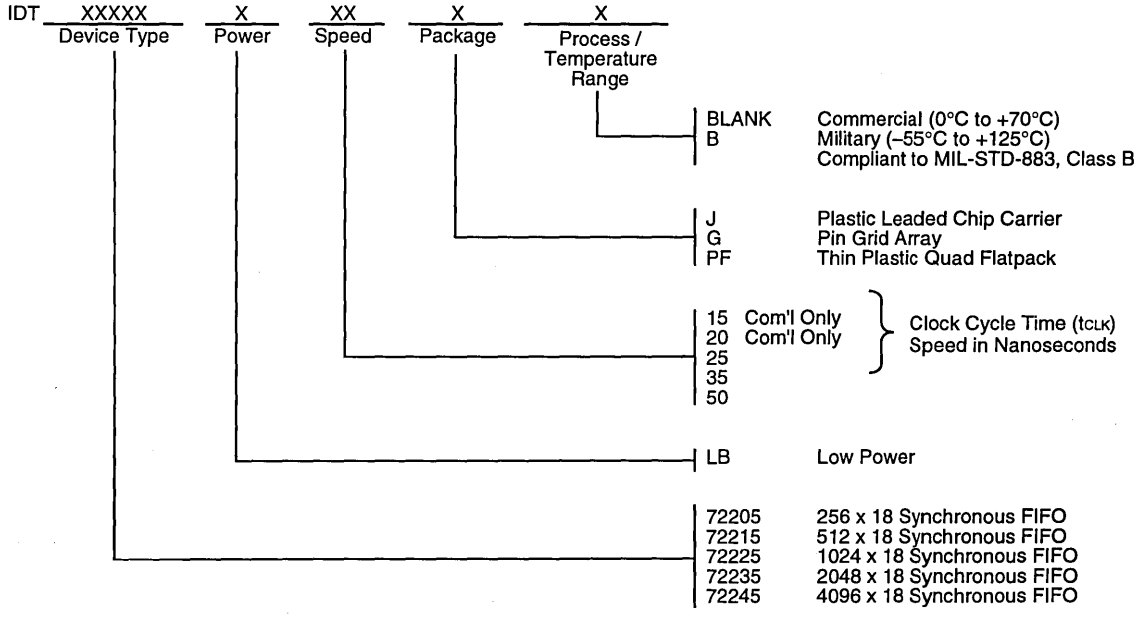


Figure 22. Block Diagram of 768 x 18/1536 x 18/3072 x 18/6144 x 18/12288 x 18 Synchronous FIFO Memory With Programmable Flags used in Depth Expansion Configuration

ORDERING INFORMATION



2766 drw 25

5

Integrated Device Technology, Inc.

CMOS DUAL SyncFIFO™ DUAL 256 x 18, DUAL 512 x 18, DUAL 1024 x 18

PRELIMINARY
IDT72805LB
IDT72815LB
IDT72825LB

FEATURES:

- The 72805 is equivalent to two 72205LB 256 x 18 FIFOs
- The 72815 is equivalent to two 72215LB 512 x 18 FIFOs
- The 72825 is equivalent to two 72225LB 1024 x 18 FIFOs
- Offers optimal combination of large capacity (2K), high speed, design flexibility, and small footprint
- Ideal for the following applications:
  - Network switching
  - Two level prioritization of parallel data
  - Bidirectional data transfer
  - Busmatching between 18-bit and 36-bit data paths
  - Width expansion to 36-bit per package
  - Depth expansion to 2048 words per package
- 20ns read/write cycle time, 12ns access time
- Read and write clocks can be asynchronous or coincident (permits simultaneous reading and writing of data on a single clock edge)
- Programmable almost-empty and almost-full flags
- Empty and Full flags signal FIFO status
- Half-Full flag capability in single device configuration
- Enable puts output data bus in high impedance state
- High-performance submicron CMOS technology
- Available in a 121-lead, 16 x 16 mm plastic Ball Grid Array (BGA)

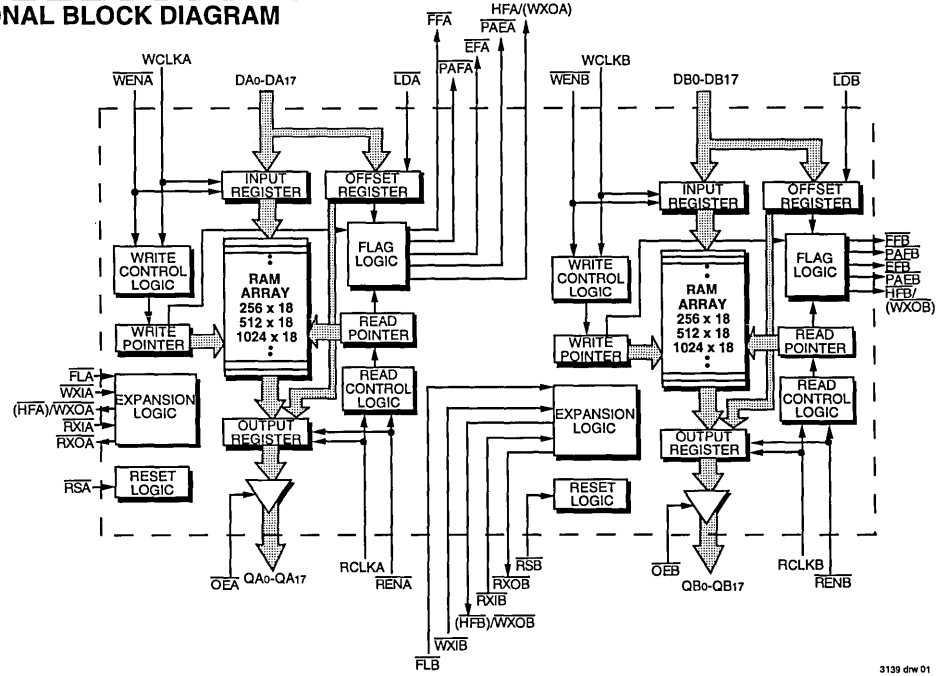
DESCRIPTION:

The IDT72805LB/72815LB/72825LB are dual 18-bit-wide synchronous (clocked) first-in, first-out (FIFO) memories. These devices are functionally equivalent to two IDT72205LB/72215LB/72225LB FIFOs in a single package with all associated control, data, and flag lines assigned to independent pins. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, local area networks (LANs), and interprocessor communication.

Each of the two FIFOs contained in the IDT72805LB/72815LB/72825LB has an 18-bit input data port (D0 - D17) and an 18-bit output data port (Q0 - Q17). Each input port is controlled by a free-running Write Clock (WCLK) and a data input Write Enable pin ($\overline{WEN}$). Data is written into each array on every rising clock edge of the appropriate Write Clock (WCLK) when its corresponding Write Enable line ($\overline{WEN}$) is asserted.

The output port of each FIFO bank is controlled by a Read Clock pin (RCLK) and a Read Enable pin ($\overline{REN}$). The Read

FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark, and SyncFIFO is a trademark of Integrated Device Technology, Inc

DESCRIPTION (CONTINUED)

Clock can be tied to the Write Clock for single clock operation or the two clock lines can run asynchronously to one another for dual clock operation. An Output Enable pin ($\overline{OE}$) is provided on the read port of each FIFO for three-state output control.

Each of the two FIFOs has fixed flags, an Empty ($\overline{EF}$) and a Full ($\overline{FF}$). Two kinds of programmable flags, an Almost-Empty ($\overline{PAE}$) and an Almost-Full ($\overline{PAF}$), are provided to improve the utilization of each FIFO memory bank. The offset loading of the programmable flags is controlled by a simple state machine and is initiated by asserting the load pin ($\overline{LD}$). A Half-Full flag ($\overline{HF}$) is available for each FIFO that is implemented as a single device.

The IDT72805LB/72815LB/72825LB are depth expandable using a daisy-chain technique. A set of expansion pins (XI and XO) are provided for each FIFO. In depth expansion configuration, FL is grounded on the first device and set high for all other devices in the daisy-chain.

The IDT72805LB/72815LB/72825LB is fabricated using IDT's high speed submicron CMOS technology.

PIN CONFIGURATION

PIN 1

	1	2	3	4	5	6	7	8	9	10	11
A	WCLKA	DA3	DA1	DA0	DB13	DB16	RCLKB	$\overline{LDB}$	$\overline{RSB}$	QB17	QB16
B	$\overline{PAFA}$	DA4	$\overline{WENA}$	DA2	DB12	DB15	$\overline{RENB}$	$\overline{OEB}$	$\overline{EFB}$	QB15	QB14
C	$\overline{FFA}$	$\overline{RXIA}$	$\overline{WXIA}$	DA5	DB14	DB11	GND	DB17	GND	QB13	QB11
D	$\overline{RXOA}$	QA0	QA2	$\overline{FLA}$	DB8	DB10	DB7	VCC	QB12	QB10	QB8
E	QA1	QA4	QA3	$\overline{WXOA}$/$\overline{HFA}$	$\overline{PAEA}$	DB9	DB6	VCC	VCC	QB9	QB7
F	QA5	QA6	GND	VCC	GND	GND	GND	VCC	GND	QB6	QB5
G	QA7	QA9	VCC	VCC	DA6	DA9	$\overline{PAEB}$	$\overline{WXOB}$/$\overline{HFB}$	QB3	QB4	QB1
H	QA8	QA10	QA12	VCC	DA7	DA10	DA8	$\overline{FLB}$	QB2	QB0	$\overline{RXOB}$
J	QA11	QA13	GND	DA17	GND	DA11	DA14	DB5	$\overline{WXIB}$	$\overline{RXIB}$	$\overline{FFB}$
K	QA14	QA15	$\overline{EFA}$	$\overline{OEA}$	$\overline{RENA}$	DA15	DA12	DB2	$\overline{WENB}$	DB4	$\overline{PAFB}$
L	QA16	QA17	$\overline{RSA}$	$\overline{LDA}$	RCKLA	DA16	DA13	DB0	DB1	DB3	WCLKB

BGA
(BG 121-1)
TOP VIEW

3139 drw 02

PIN DESCRIPTION

Symbol	Name	I/O	Description
DA0–DA17 DB0–DB17	Data Inputs	I	Data inputs for a 18-bit bus.
$\overline{RSA}$ $\overline{RSB}$	Reset	I	When $\overline{RS}$ is set LOW, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go HIGH, and $\overline{PAE}$ and $\overline{EF}$ go LOW. A reset is required before an initial WRITE after power-up.
WCLKA WCLKB	Write Clock	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on a LOW-to-HIGH transition of WCLK, if the FIFO is not full.
$\overline{WENA}$ $\overline{WENB}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is HIGH, the FIFO holds the previous data. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
RCLKA RCLKB	Read Clock	I	When $\overline{REN}$ is LOW, data is read from the FIFO on a LOW-to-HIGH transition of RCLK, if the FIFO is not empty.
$\overline{RENA}$ $\overline{RENB}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is HIGH, the output register holds the previous data. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OEA}$ $\overline{OEB}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high-impedance state.
$\overline{LDA}$ $\overline{LDB}$	Load	I	When $\overline{LD}$ is LOW, data on the inputs D0–D9 is written to the offset and depth registers on the LOW-to-HIGH transition of the WCLK, when $\overline{WEN}$ is LOW. When $\overline{LD}$ is LOW, data on the outputs Q0–Q9 is read from the offset and depth registers on the LOW-to-HIGH transition of the RCLK, when $\overline{REN}$ is LOW.
$\overline{FLA}$ $\overline{FLB}$	First Load	I	In the single device or width expansion configuration, $\overline{FL}$ is grounded. In the depth expansion configuration, $\overline{FL}$ is grounded on the first device (first load device) and set to HIGH for all other devices in the daisy chain.
$\overline{WXIA}$ $\overline{WXIB}$	Write Expansion Input	I	In the single device or width expansion configuration, $\overline{WXI}$ is grounded. In the depth expansion configuration, $\overline{WXI}$ is connected to $\overline{WXO}$ (Write Expansion Out) of the previous device.
$\overline{RXIA}$ $\overline{RXIB}$	Read Expansion Input	I	In the single device or width expansion configuration, RXI is grounded. In the depth expansion configuration, $\overline{RXI}$ is connected to $\overline{RXO}$ (Read Expansion Out) of the previous device.
$\overline{EFA}$ $\overline{EFB}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAEA}$ $\overline{PAEB}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is 31 from empty for 72805LB, 63 from empty for 72815LB, and 127 from empty for 72825LB.
$\overline{PAFA}$ $\overline{PAFB}$	Programmable	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is 31 from full for 72805LB, 63 from full for 72815LB, and 127 from full for 72825LB.
$\overline{FFA}$ $\overline{FFB}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{WXOA/HFA}$ $\overline{WXOB/HFB}$	Write Expansion Out/Half-Full Flag	O	In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is LOW. In the depth expansion configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device when the last location in the FIFO is written.
$\overline{RXOA}$ $\overline{RXOB}$	Read Expansion Out	O	In the depth expansion configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next device when the last location in the FIFO is read.
QA0–QA17 QB0–QB17	Data Outputs	O	Data outputs for a 18-bit bus.
VCC	Power		8 Vcc pins
GND	Ground		9 GND pins

3139 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 3139 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maimum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	—	V
VIL(1)	Input Low Voltage	—	—	0.8	V

NOTE: 3139 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	IDT72805LB IDT72815LB IDT72825LB Commercial tCLK = 20, 25, 35ns			Unit
		Min.	Typ.	Max	
ILI(1)	Input Leakage Current (any input)	–1	—	1	µA
ILO(2)	Output Leakage Current	–10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = –2 mA	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8 mA	—	—	0.4	V
ICC1(3)	Active Power Supply Current	—	—	250	mA
ICC2(3)	Average Standby Current (All Input = VCC – 0.2V, except RCLK and WCLK which are free-running)	—	—	80	mA

NOTES: 3139 tbl 04

1. Measurements with 0.4 ≤ VIN ≤ VCC.
2. $\overline{OE}$ ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. Tested at f = 20MHz with outputs unloaded.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN(2)	Input Capacitance	VIN = 0V	10	pF
COUT(1,2)	Output Capacitance	VOUT = 0V	10	pF

NOTES: 3139 tbl 05

1. With output deselected, ($\overline{OE}$ = HIGH).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

		Commercial						
		72805LB20 72815LB20 72825LB20		72805LB25 72815LB25 72825LB25		72805LB35 72815LB35 72825LB35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Clock Cycle Frequency	—	50	—	40	—	28.6	MHz
tA	Data Access Time	2	12	3	15	3	20	ns
tCLK	Clock Cycle Time	20	—	25	—	35	—	ns
tCLKH	Clock HIGH Time	8	—	10	—	14	—	ns
tCLKL	Clock LOW Time	8	—	10	—	14	—	ns
tDS	Data Set-up Time	5	—	6	—	7	—	ns
tDH	Data Hold Time	1	—	1	—	2	—	ns
tENS	Enable Set-up Time	5	—	6	—	7	—	ns
tENH	Enable Hold Time	1	—	1	—	2	—	ns
tRS	Reset Pulse Width(1)	20	—	25	—	35	—	ns
tRSS	Reset Set-up Time	12	—	15	—	20	—	ns
tRSR	Reset Recovery Time	12	—	15	—	20	—	ns
tRSF	Reset to Flag and Output Time	—	35	—	40	—	45	ns
tOLZ	Output Enable to Output in Low-Z(2)	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	—	9	—	12	—	15	ns
tOHZ	Output Enable to Output in High-Z(2)	1	9	1	12	1	15	ns
tWFF	Write Clock to Full Flag	—	12	—	15	—	20	ns
tREF	Read Clock to Empty Flag	—	12	—	15	—	20	ns
tPAF	Clock to Programmable Almost-Full Flag	—	30	—	35	—	40	ns
tPAE	Clock to Programmable Almost-Empty Flag	—	30	—	35	—	40	ns
tHF	Clock to Half-Full Flag	—	30	—	35	—	40	ns
tXO	Clock to Expansion Out	—	12	—	15	—	20	ns
tXI	Expansion In Pulse Width	8	—	10	—	14	—	ns
tXIS	Expansion In Set-Up Time	8	—	10	—	15	—	ns
tSKEW1	Skew time between Read Clock & Write Clock for Full Flag	14	—	16	—	18	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Empty Flag	14	—	16	—	18	—	ns

3139 tbl 06

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

3139 tbl 07

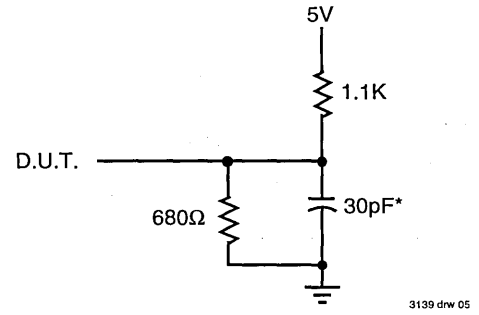


Figure 1. Output Load

* Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (DA_0 - DA_{17}, DB_0 - DB_{17})

Data inputs for 18-bit wide data.

CONTROLS:

RESET ($\overline{RSA}$, $\overline{RSB}$)

Reset is accomplished whenever the Reset ($\overline{RSA}$, $\overline{RSB}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag ($\overline{FFA}$, $\overline{FFB}$), Half-Full Flag ($\overline{HFA}$, $\overline{HFB}$), and Programmable Almost-Full Flag ($\overline{PAFA}$, $\overline{PAFB}$) will be reset to HIGH after t_{RSF}. The Empty Flag ($\overline{EFA}$, $\overline{EFB}$) and Programmable Almost-Empty Flag ($\overline{PAEA}$, $\overline{PAEB}$) will be reset to LOW after t_{RSF}. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

WRITE CLOCK (WCLKA, WCLKB)

A write cycle is initiated on the LOW-to-HIGH transition of the write clock (WCLKA, WCLKB). Data set-up and hold times must be met with respect to the LOW-to-HIGH transition of WCLK.

The write and read clocks can be asynchronous or coincident.

WRITE ENABLE ($\overline{WENA}$, $\overline{WENB}$)

When Write Enable ($\overline{WENA}$, $\overline{WENB}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every WCLK. Data is stored in the RAM array sequentially and independently of any on-going read operation.

When $\overline{WEN}$ is HIGH, the input register holds the previous data and no new data is loaded into the FIFO.

To prevent data overflow, $\overline{FF}$ will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the $\overline{FF}$ will go HIGH after t_{WFF} allowing a write to begin. $\overline{WEN}$ is ignored when the FIFO is full.

READ CLOCK (RCLKA, RCLKB)

Data can be read on the outputs on the LOW-to-HIGH transition of the read clock (RCLKA, RCLKB), when the Output Enable ($\overline{OEA}$, $\overline{OEB}$) is set LOW.

The write and read clocks can be asynchronous or coincident.

READ ENABLE ($\overline{RENA}$, $\overline{RENB}$)

When Read Enable ($\overline{RENA}$, $\overline{RENB}$) is LOW, data is loaded into the RAM array to the output register on the LOW-to-HIGH transition of the RCLK.

When $\overline{REN}$ is HIGH, the output register holds the previous data and no new data is loaded into the register.

When all the data has been read from the FIFO, $\overline{EF}$ will go LOW, inhibiting further read operations. Once a write is performed, the $\overline{EF}$ will go HIGH after t_{REF} and a read can begin. $\overline{REN}$ is ignored when the FIFO is empty.

OUTPUT ENABLE ($\overline{OEA}$, $\overline{OEB}$)

When Output Enable ($\overline{OEA}$, $\overline{OEB}$) is enabled (LOW), the parallel output buffers receive data from the output register. When $\overline{OE}$ is disabled (HIGH), the Q output data bus is in a high-impedance state.

LOAD ($\overline{LDA}$, $\overline{LDB}$)

The IDT72805LB/72815LB/72825LB devices contain two 10-bit offset registers with data on the inputs, or read on the outputs. When the Load ($\overline{LDA}$, $\overline{LDB}$) pin is set LOW and $\overline{WEN}$ is set LOW, data on the inputs D0-D19 is written into the Empty offset register on the first LOW-to-HIGH transition of WCLK. When $\overline{LD}$ and $\overline{WEN}$ are held LOW then data is written into the Full offset register on the second LOW-to-HIGH transition of WCLK. The third transition of WCLK again writes to the Empty offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing $\overline{LD}$ HIGH, the FIFO is returned to normal read/write operation. When $\overline{LD}$ is set LOW, and $\overline{WEN}$ is LOW, the next offset register in sequence is written.

When $\overline{LD}$ is LOW and $\overline{WEN}$ is HIGH, the WCLK input is disabled; then a signal at this input can neither increment the write offset register pointer, nor execute a write.

The contents of the offset registers can be read on the output lines when $\overline{LD}$ is set LOW and $\overline{REN}$ is set LOW; then, data can be read on the LOW-to-HIGH transition of RCLK. The act of reading the control registers employs a dedicated read offset register pointer. (The read and write pointers operate independently).

A read and a write should not be performed simultaneously to the offset registers.

$\overline{LDA}$ $\overline{LDB}$	$\overline{WENA}$ $\overline{WENB}$	$\overline{WCLKA}$[1] $\overline{WCLKB}$[1]	Selection
0	0	↑	Writing to offset registers: Empty Offset Full Offset
0	1	↑	No Operation
1	0	↑	Write Into FIFO
1	1	↑	No Operation

NOTE: 3139 tbl 08

1. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Figure 2. Write Offset Register

5

FIRST LOAD ($\overline{FLA}$, $\overline{FLB}$)

First Load ($\overline{FLA}$, $\overline{FLB}$) is grounded to indicate operation in the Single Device or Width Expansion mode. In the Depth Expansion configuration, $\overline{FL}$ is grounded to indicate it is the first deBvice loaded and is set to HIGH for all other devices in the daisy chain. (See Operating Configurations for further details.)

WRITE EXPANSION INPUT ($\overline{WXIA}$, $\overline{WXIB}$)

This is a dual purpose pin. Write Expansion In ($\overline{WXIA}$, $\overline{WXIB}$) is grounded to indicate operation in the Single Device or Width Expansion mode. $\overline{WXI}$ is connected to Write Expansion Out ($\overline{WXOA}$, $\overline{WXOB}$) of the previous device in the Depth Expansion or Daisy Chain mode.

READ EXPANSION INPUT ($\overline{RXIA}$, $\overline{RXIB}$)

This is a dual purpose pin. Read Expansion In ($\overline{RXIA}$, $\overline{RXIB}$) is grounded to indicate operation in the Single Device or Width Expansion mode. $\overline{RXI}$ is connected to Read Expansion Out ($\overline{RXOA}$, $\overline{RXOB}$) of the previous device in the Depth Expansion or Daisy Chain mode.

OUTPUTS:

FULL FLAG ($\overline{FFA}$, $\overline{FFB}$)

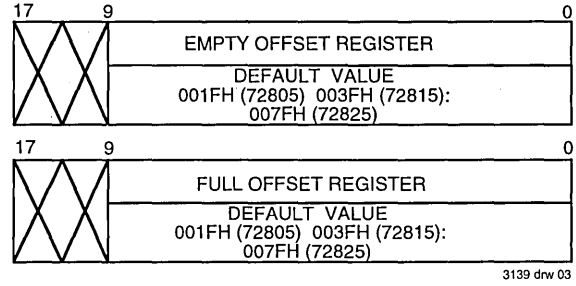
The Full Flag ($\overline{FFA}$, $\overline{FFB}$) will go LOW, inhibiting further write operation, indicating that the device is full. If no reads are performed after $\overline{RS}$, $\overline{FF}$ will go LOW after 256 writes for the IDT72805LB, 512 writes for the IDT72815LB, 1024 writes for the IDT72825LB.

$\overline{FF}$ is updated on the LOW-to-HIGH transition of WCLK.

EMPTY FLAG ($\overline{EFA}$, $\overline{EFB}$)

The Empty Flag ($\overline{EFA}$, $\overline{EFB}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The $\overline{EF}$ is updated on the LOW-to-HIGH transition of RCLK.



3139 drw 03

NOTE:
1. Any bits of the offset register not being programmed should be set to zero.

Figure 3. Offset Register Location and Default Values

TABLE I — STATUS FLAGS

Number of Words in FIFO			$\overline{FFA}$	$\overline{PAFA}$	$\overline{HFA}$	$\overline{PAEA}$	$\overline{EFA}$
72805	72815	72825	$\overline{FFB}$	$\overline{PAFB}$	$\overline{HFB}$	$\overline{PAEB}$	$\overline{EFB}$
0	0	0	H	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	H	L	H
(n + 1) to 128	(n + 1) to 256	(n + 1) to 512	H	H	H	H	H
129 to (256-(m+1))	257 to (512-(m+1))	513 to (1024-(m+1))	H	H	L	H	H
(256-m)[2] to 255	(512-m)[2] to 511	(1024-m)[2] to 1023	H	L	L	H	H
256	512	1024	L	L	L	H	H

NOTES:
1. n = Empty Offset (Default Values : 72805 n=31, 72815 n = 63, 72825 n = 127)
2. m = Full Offset (Default Values : 72805 n=31, 72815 n = 63, 722825 n = 127)

3139 tbl 09

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAFA}$, $\overline{PAFB}$)

The Programmable Almost-Full Flag ($\overline{PAFA}$, $\overline{PAFB}$) will go LOW when FIFO reaches the Almost-Full condition. If no reads are performed after $\overline{RS}$, the $\overline{PAF}$ will go LOW after (256-m) writes for the IDT72805LB, (512-m) writes for the IDT72815LB, (1024-m) writes for the IDT72825LB. The offset "m" is defined in the FULL offset register.

If there is no Full offset specified, the $\overline{PAF}$ will be LOW when the device is 31 away from completely full for 72805LB, 63 away from completely full for 72815LB, and 127 away from completely full for 72825LB.

The $\overline{PAF}$ is asserted LOW on the LOW-to-HIGH transition of the WCLK. $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of RCLK. Thus $\overline{PAF}$ is asychronous.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAEA}$, $\overline{PAEB}$)

The Programmable Almost-Empty Flag ($\overline{PAEA}$, $\overline{PAEB}$) will go LOW when the read pointer is "n" locations less than the write pointer. The offset "n" is defined in the EMPTY offset register.

If there is no Empty offset specified, $\overline{PAE}$ will be LOW when the device is 31 away from completely empty for 72805LB, 63 away from completely empty for 72815LB, and 127 away from completely empty for 72825LB.

The $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of RCLK. $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of WCLK. Thus $\overline{PAF}$ is asychronous.

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXOA/HFA}$, $\overline{WXOB/HFB}$)

This is a dual-purpose output. In the Single Device and Width Expansion mode, when $\overline{WXI}$ is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the LOW-to-HIGH transition of the next write cycle, the Half-Full Flag goes LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HFA}$, $\overline{HFB}$) is then reset to HIGH by the LOW-to-HIGH transition of the read clock (RCLK). The $\overline{HF}$ is asychronous.

In the Depth Expansion or Daisy Chain mode, $\overline{WXI}$ is connected to $\overline{WXO}$ of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device writes to the last location of memory.

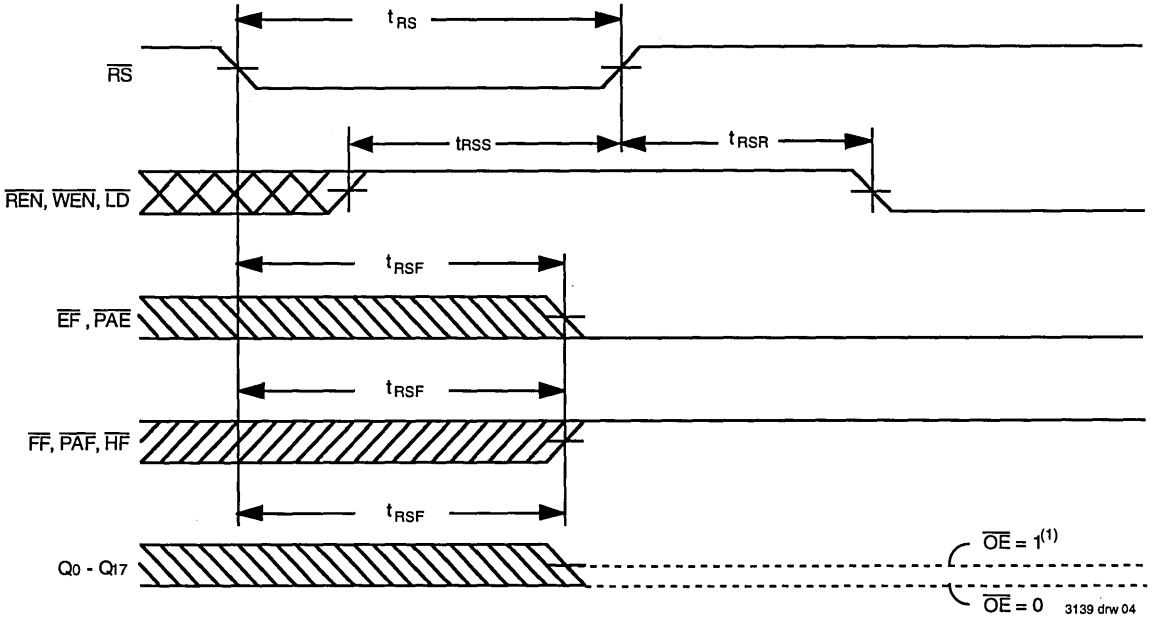
READ EXPANSION OUT ($\overline{RXOA}$, $\overline{RXOB}$)

In the Depth Expansion or Daisy Chain configuration, Read Expansion In ($\overline{RXIA}$, $\overline{RXIB}$) is connected to Read Expansion Out ($\overline{RXOA}$, $\overline{RXOB}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device reads from the last location of memory.

DATA OUTPUTS (Q0A-QA17, QB0-QB17)

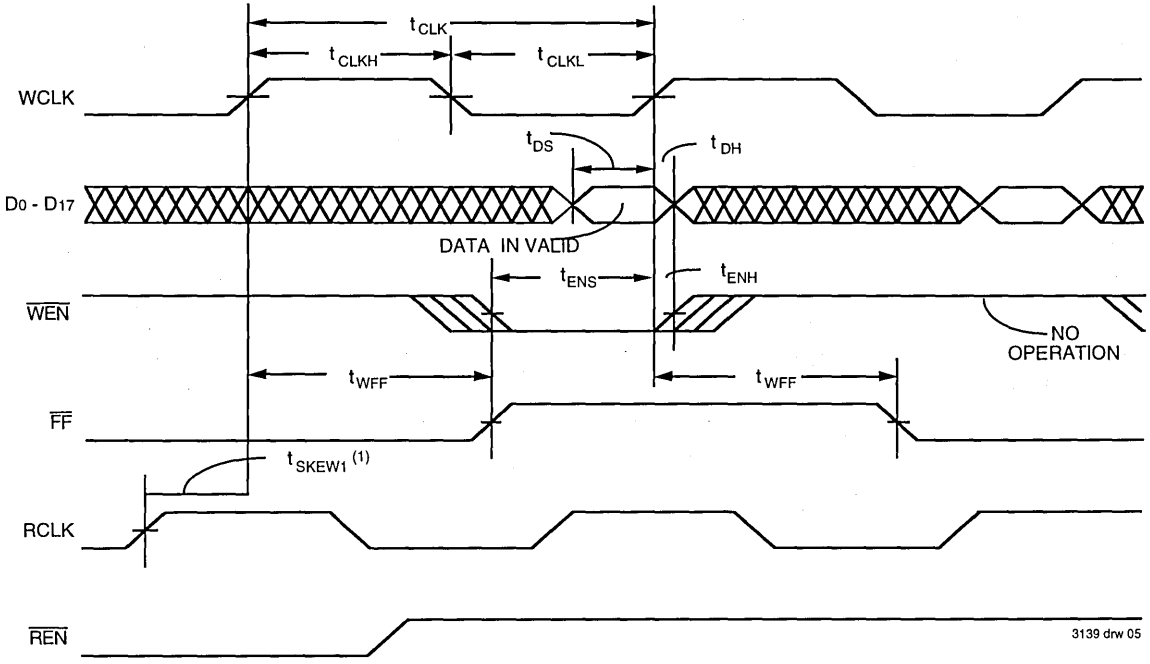
Q0-Q17 are data outputs for 18-bit wide data.

5



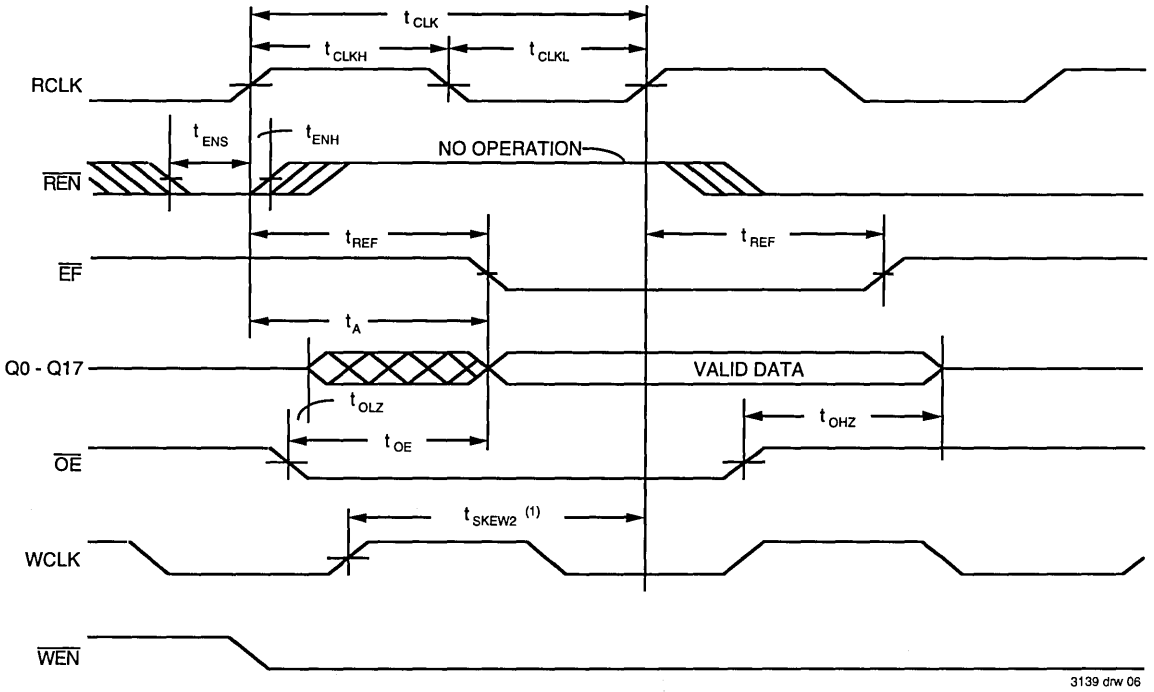
NOTES:
1. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

Figure 4. Reset Timing(2)



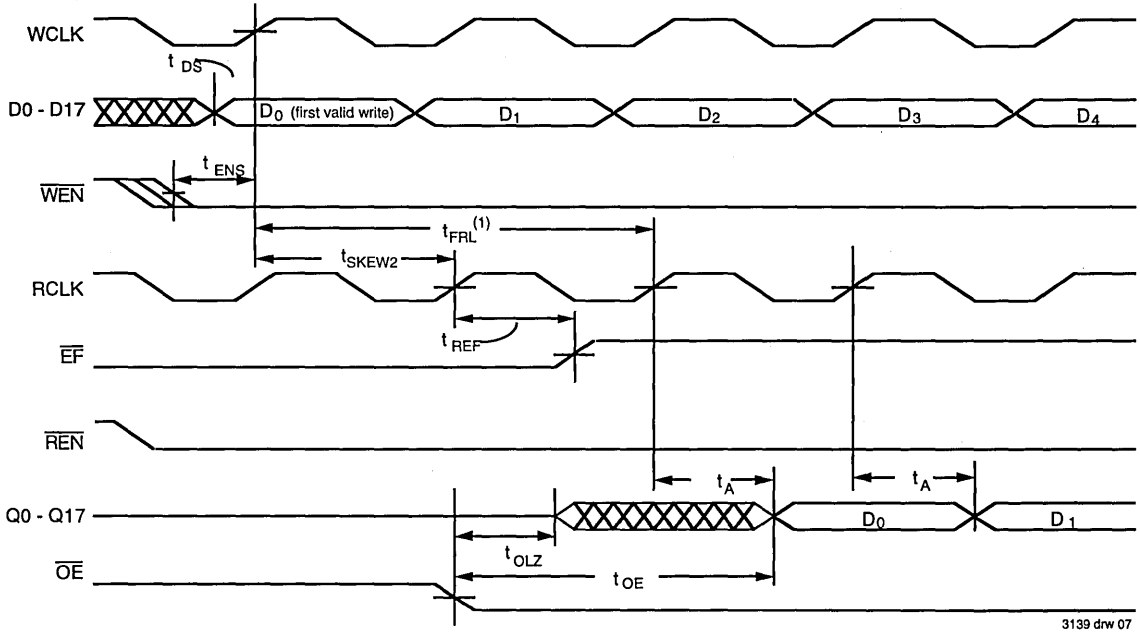
NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

Figure 5. Write Cycle Timing



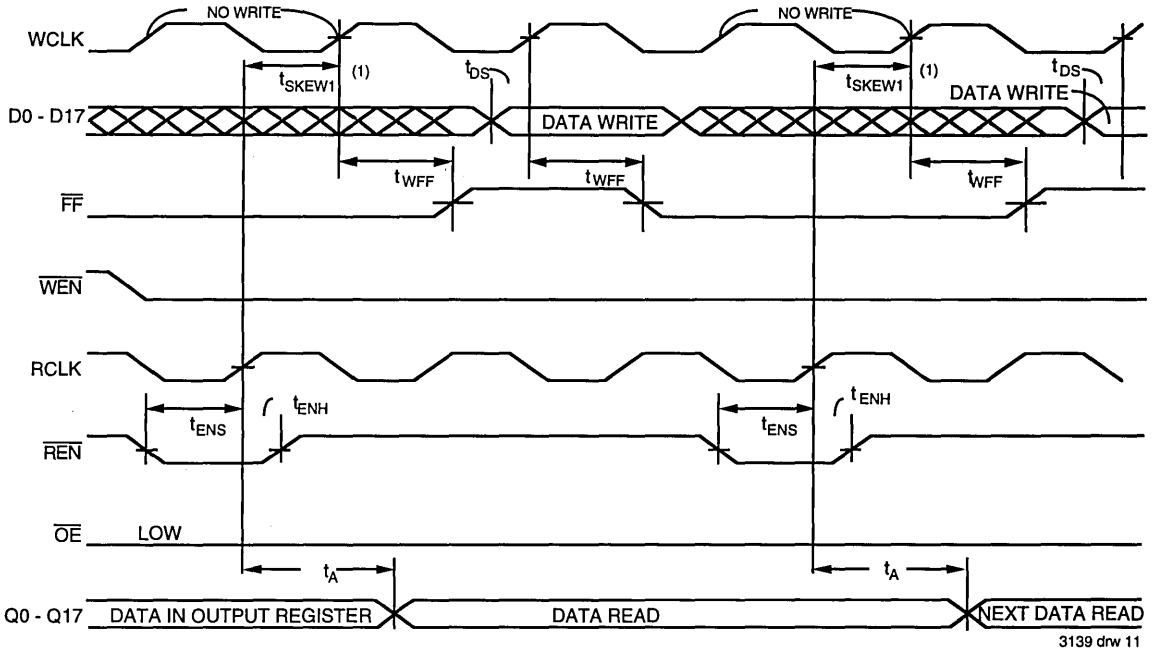
NOTE:
1. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 6. Read Cycle Timing



NOTES:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2 * t_{CLK} + t_{SKEW2} or t_{CLK} + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
2. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

Figure 7. First Data Word Latency after Reset with Simultaneous Read and Write



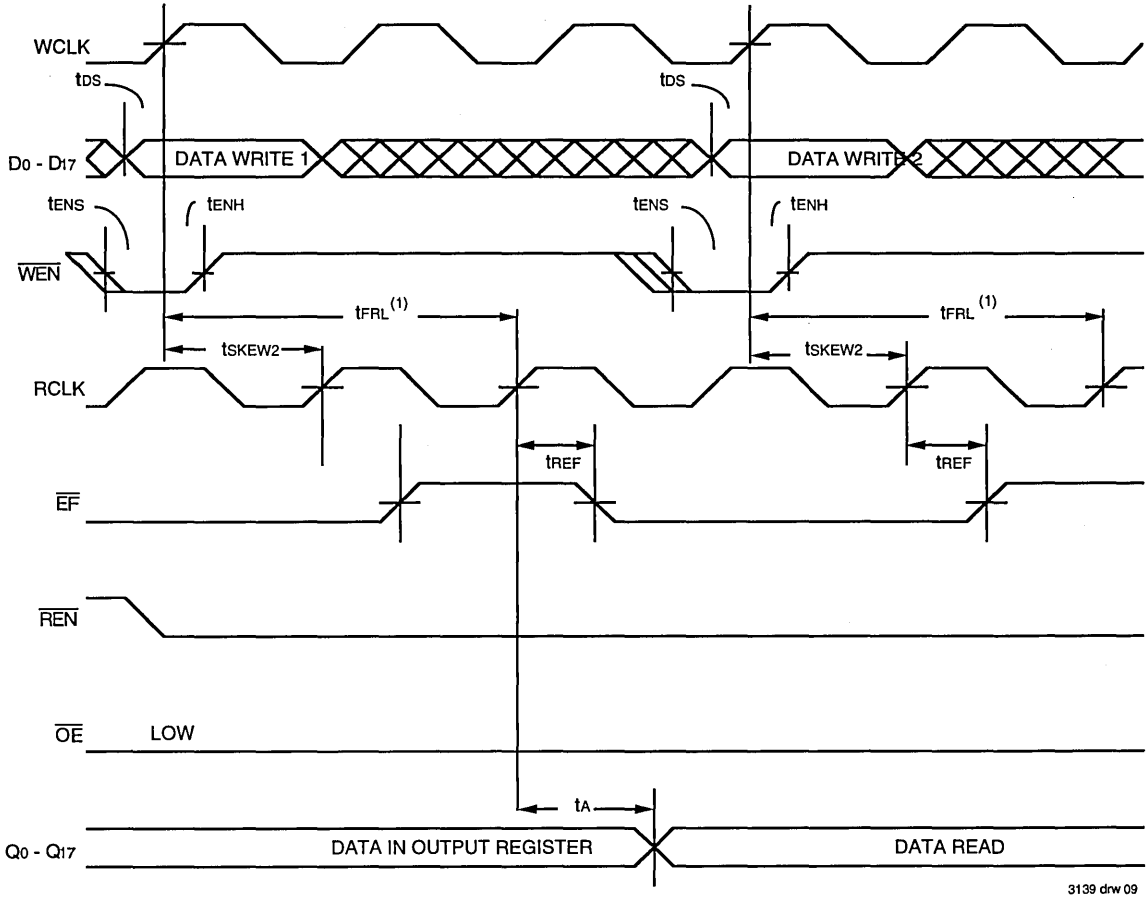
3139 drw 11

NOTE:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

Figure 8. Full Flag Timing

5



NOTE:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2 * t_{CLK} + t_{SKEW2}. or t_{CLK} + t_{SKEW2}. The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 9. Empty Flag Timing

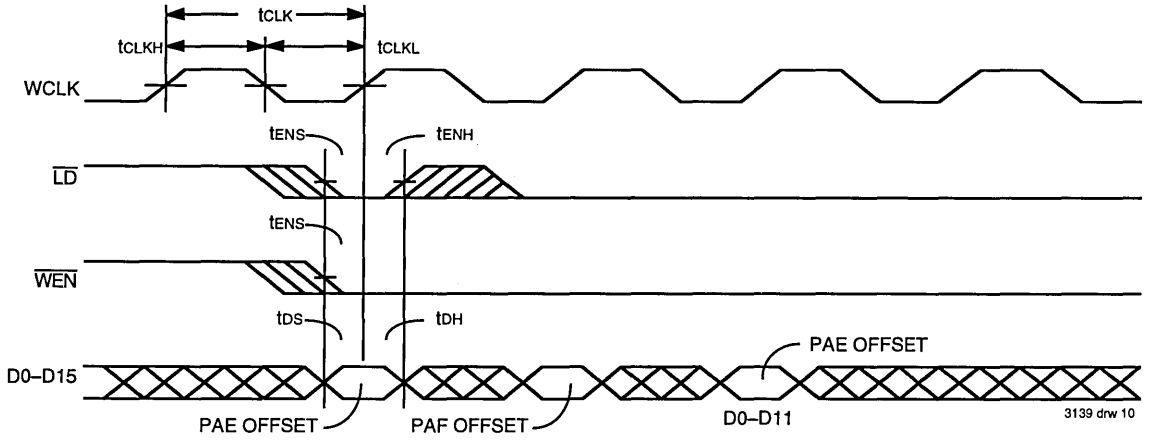


Figure 10. Write Programmable Registers

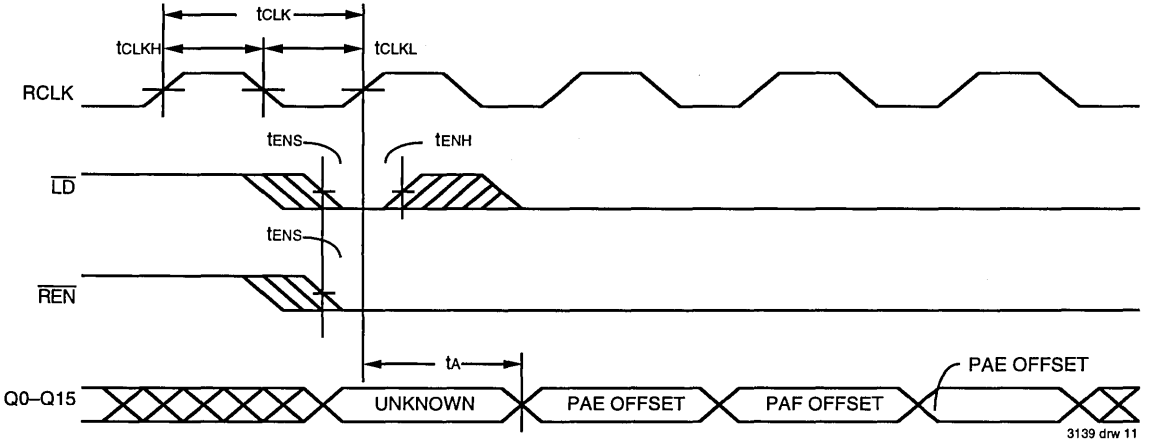
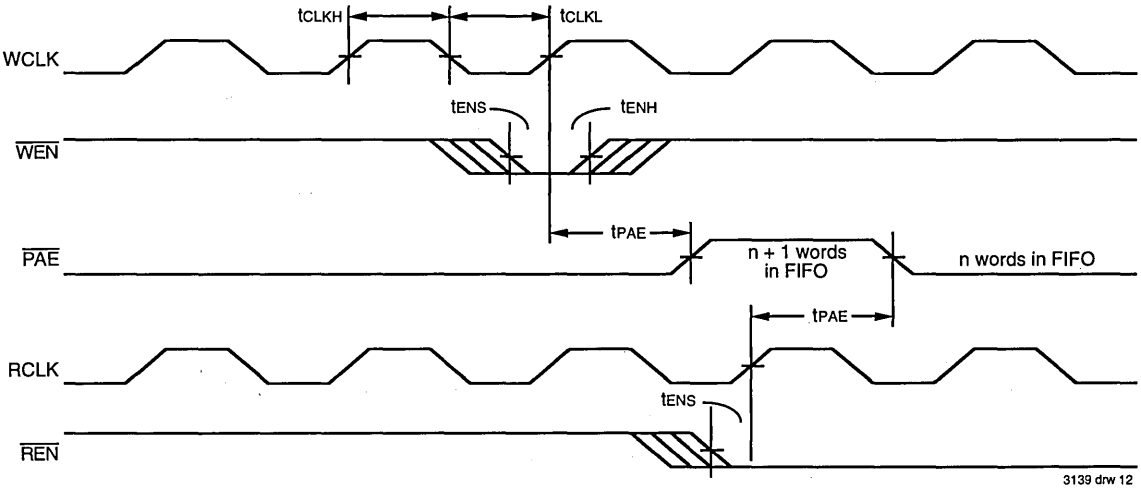
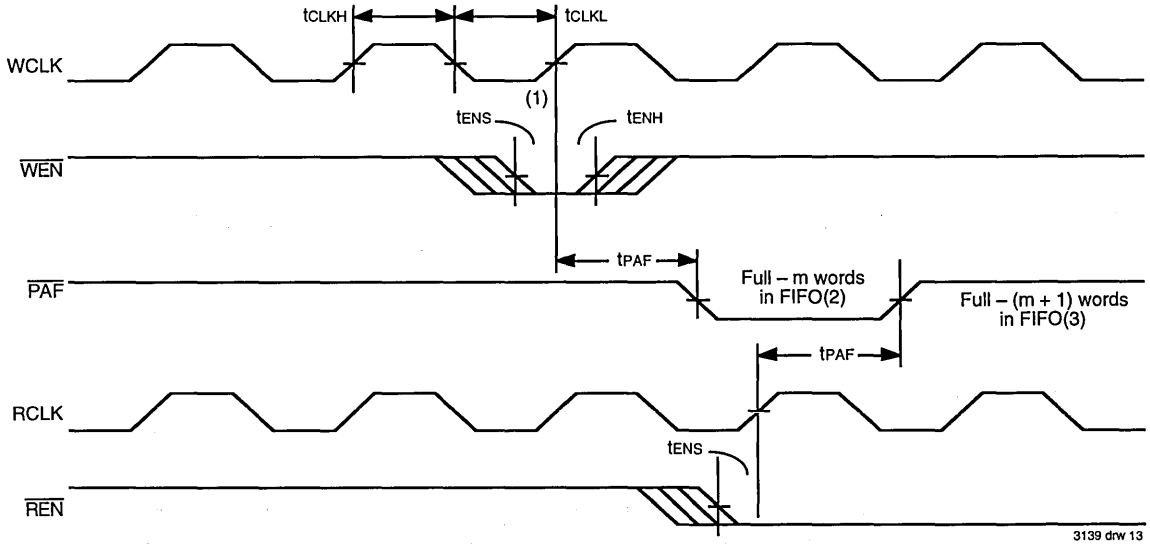


Figure 11. Read Programmable Registers



NOTE:
1. PAE is offset = n. Number of data words written into FIFO already = n.

Figure 12. Programmable Almost Empty Flag Timing



NOTES:
1. PAF offset = m. Number of data words written into FIFO already = 256 - (m + 1) for the IDT72805LB, 512 - (m + 1) for the IDT72815LB, 1024 - (m + 1) for the IDT72825LB.
2. 256 - m words in IDT72805LB, 512 - m words in IDT72815LB, 1024 - m words in IDT72825LB.
3. 256 - (m + 1) words in IDT72805LB, 512 - (m + 1) words in IDT72815LB, 1024 - (m + 1) words in IDT72825LB.

Figure 13. Programmable Almost-Full Flag Timing

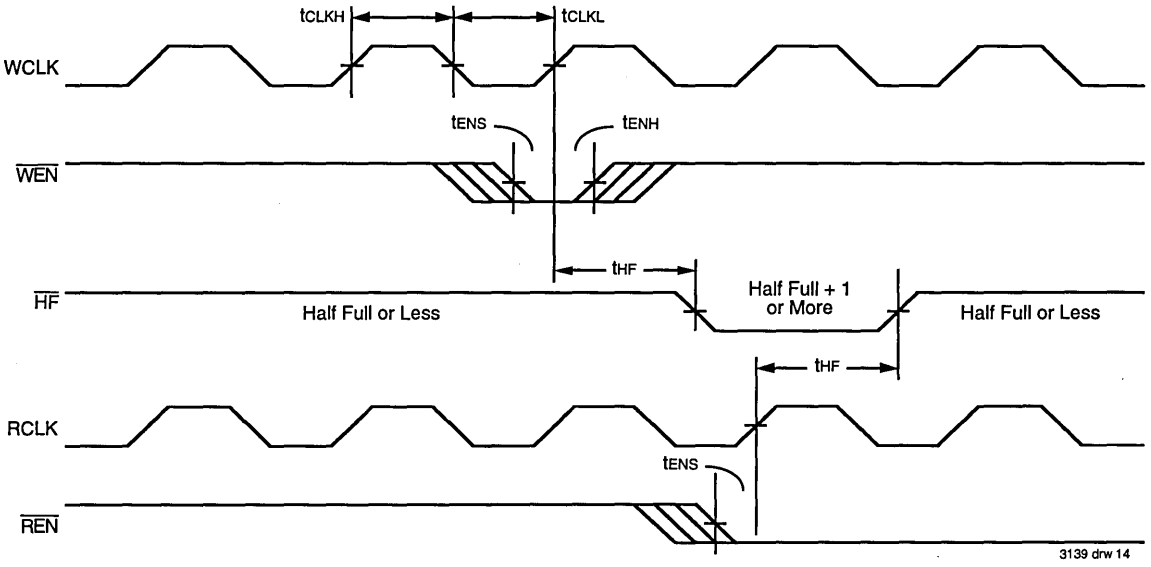
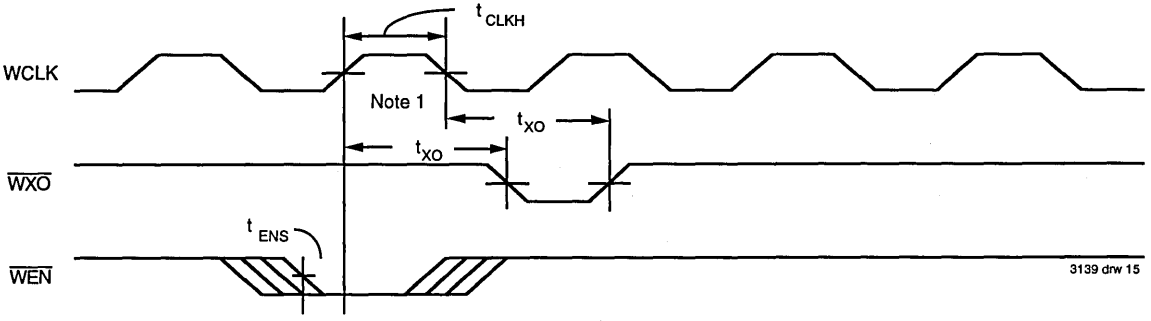
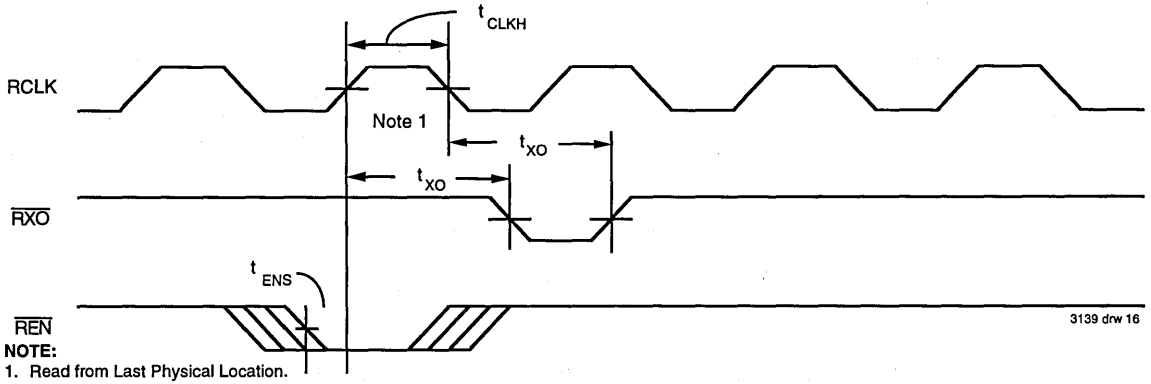


Figure 14. Half-Full Flag Timing



NOTE:
1. Write to Last Physical Location.

Figure 15. Write Expansion Out Timing



NOTE:
1. Read from Last Physical Location.

Figure 16. Read Expansion Out Timing

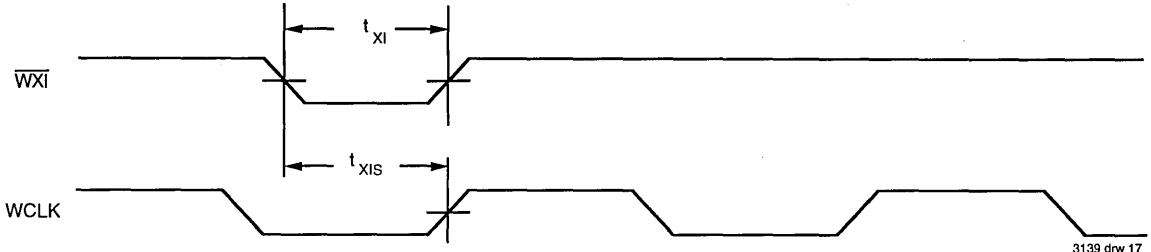


Figure 17. Write Expansion In Timing

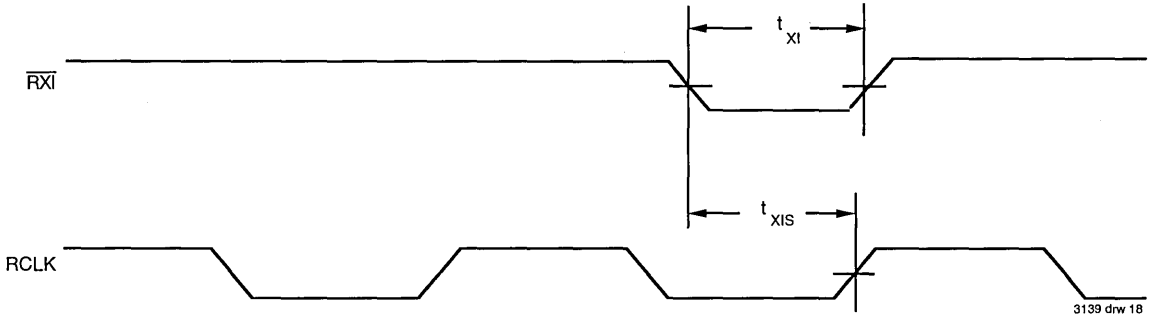


Figure 18. Read Expansion In Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

Each of the two FIFOs contained in a single IDT72805LB/72815LB/72825LB may be operated as a stand-alone device when the application requirements are for 256/512/1024 words or less. The IDT72805LB/72815LB/72825LB are in a single Device Configuration when the Write Exansion In ($\overline{WXI}$), Read Expansion In ($\overline{RXI}$), and First Load ($\overline{FL}$) control inputs are grounded (Figure 19).

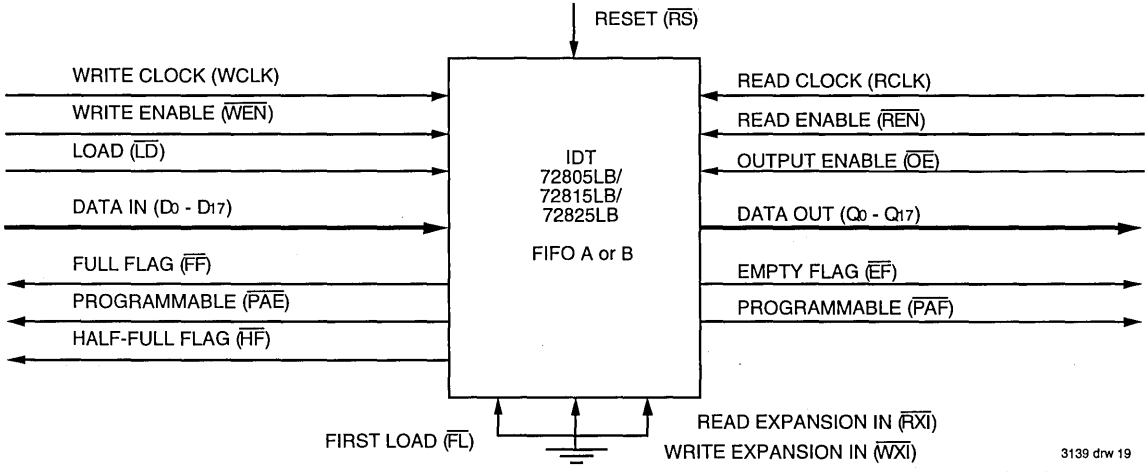
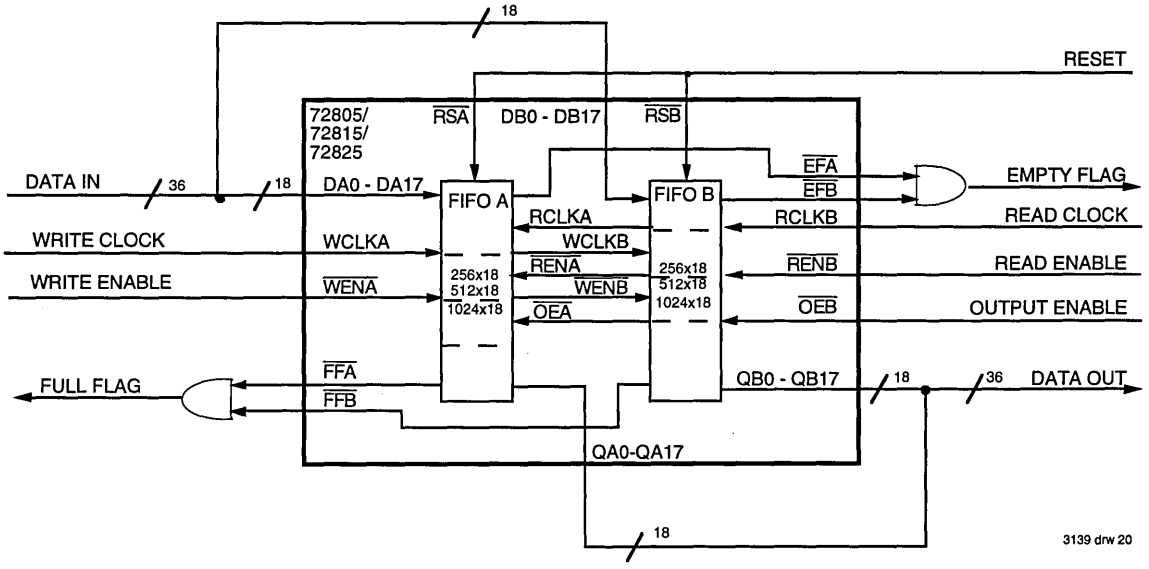


Figure 19. Block Diagram of Single 256 x 18/512 x 18/1024 x 18 Synchronous FIFO
(One of the Two FIFOs contained in the 72805/72815/72825)

WIDTH EXPANSION CONFIGURATION — Word width may be increased simply by connecting together the control signals of FIFOs A and B. A composite flag should be created for each of the end-point status flags ($\overline{EFA}$ and $\overline{EFB}$, also $\overline{FFA}$ and $\overline{FFB}$). The partial status flags ($\overline{PAEA}$ and $\overline{PAEB}$, also $\overline{PAFA}$ and $\overline{PAFB}$) can be detected from any one device. Figure 20 demonstrates a 36-bit word width using the two FIFOs contained in one IDT72805/72815/72825. Any word width can be attained by adding additional IDT2805/72815/72825.



NOTE:
1. Do not tie any output control signals directly together.
2. Tie $\overline{FLA}$, $\overline{FLB}$, $\overline{WXIA}$, $\overline{WXIB}$, $\overline{RXIA}$ and $\overline{RXIB}$ to GND.

Figure 20. Block Diagram of the two FIFOs contained in one 72805/72815/72825 configured for a 36-bit Width Expansion

DEPTH EXPANSION CONFIGURATION (WITH PROGRAMMABLE FLAGS)

The IDT72805LB/72815LB/72825LB can easily be adapted to applications requiring more than 256/512/1024 words of buffering. Figure 21 shows a Depth Expansion using the two FIFOs contained in one IDT72805LB/72815LB/72825LB. Maximum depth is limited only by signal loading. Follow these steps:

1. The first FIFO must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other FIFOs must have $\overline{FL}$ in the HIGH state.
3. The Write Expansion Out ($\overline{WXO}$) pin of each device must be tied to the Write Expansion In ($\overline{WXI}$) pin of the next FIFO.
4. The Read Expansion Out ($\overline{RXO}$) pin of each device must be tied to the Read Expansion In ($\overline{RXI}$) pin of the next FIFO.
5. All Load ($\overline{LD}$) pins are tied together.
6. The Half-Full Flag ($\overline{HF}$) is not available in the Depth Expansion Configuration.
7. $\overline{EF}$, $\overline{FF}$, $\overline{PAE}$, and $\overline{PAF}$ are created with composite flags by ORing together every respective flags for monitoring. The composite $\overline{PAE}$ and $\overline{PAF}$ flags are not precise.

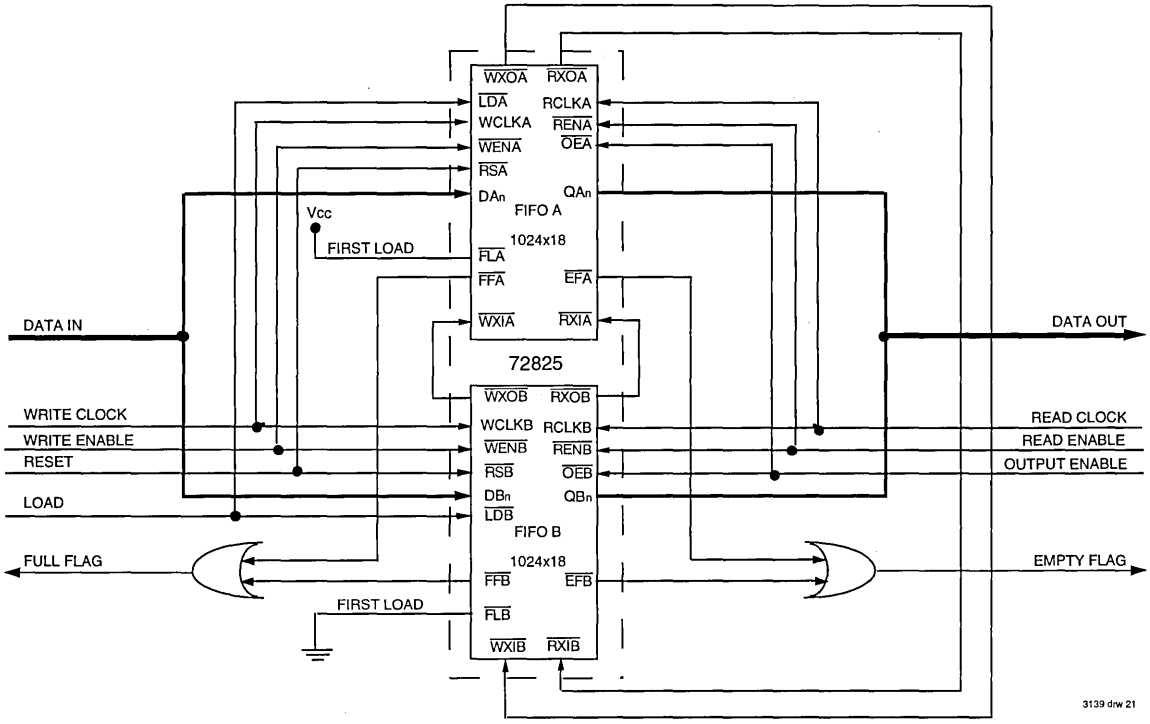
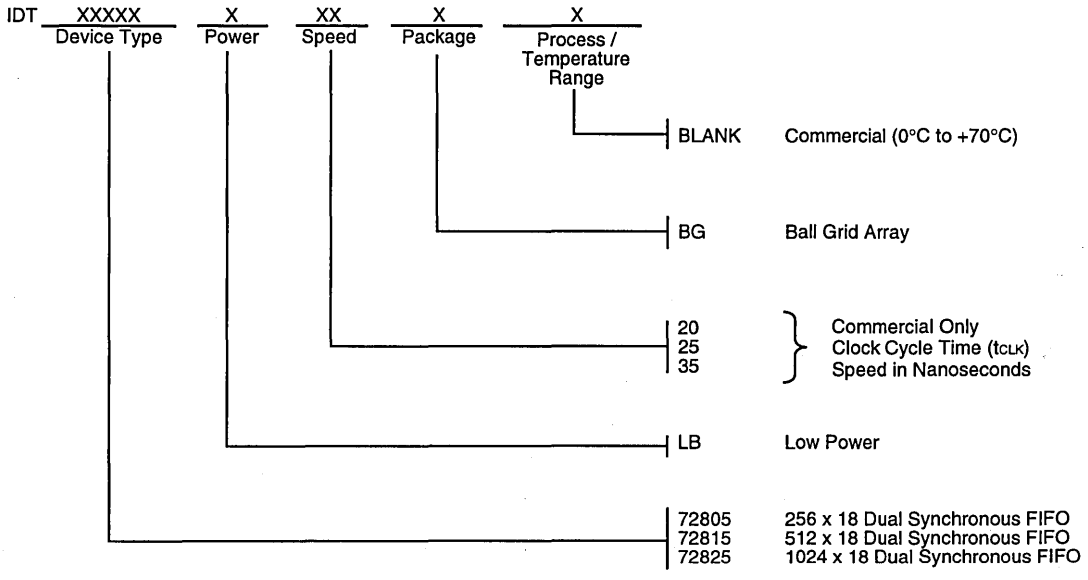


Figure 21. Block Diagram of 2048 x 18 Synchronous FIFO Memory With Programmable Flags used in Depth Expansion Configuration

ORDERING INFORMATION



3139 drw 22

5

Integrated Device Technology, Inc.

BiCMOSClocked FIFO 64 x 36

IDT723611

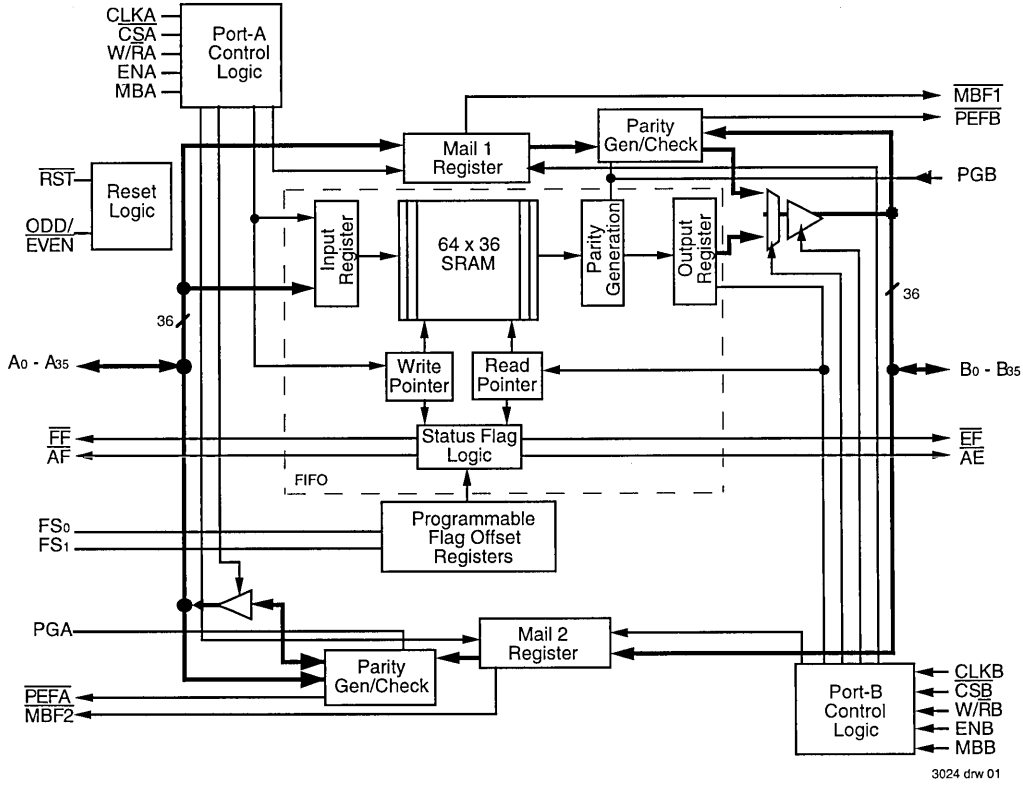
FEATURES:

- Free-running CLKA and CLKB may be asynchronous or coincident (permits simultaneous reading and writing of data on a single clock edge)
- 64 x 36 storage capacity
- Synchronous data buffering from Port A to Port B
- Mailbox bypass register in each direction
- Programmable Almost-Full ($\overline{AF}$) and Almost-Empty ($\overline{AE}$) flags
- Microprocessor Interface Control Logic
- Full Flag ($\overline{FF}$) and Almost-Full ($\overline{AF}$) flags synchronized by CLKA
- Empty Flag ($\overline{EF}$) and Almost-Empty ($\overline{AE}$) flags synchronized by CLKB
- Passive parity checking on each Port
- Parity Generation can be selected for each Port
- Supports clock frequencies up to 67MHz
- Fast access times of 10ns
- Available in 132-pin Plastic Quad Flatpack (PQF) or space-saving 120-pin Thin Quad Flatpack (PF)
- Low-power advanced BiCMOS technology

DESCRIPTION:

The IDT723611 is a monolithic, high-speed, low-power, BiCMOS Synchronous (clocked) FIFO memory which supports clock frequencies up to 67MHz and has read access times as fast as 10ns. The 64 x 36 dual-port FIFO buffers data from Port A to Port B. The FIFO has flags to indicate empty and full conditions, and two programmable flags, Almost-Full ($\overline{AF}$) and Almost-Empty ($\overline{AE}$), to indicate when a selected number of words is stored in memory. Communication between each port can take place through two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be

FUNCTIONAL BLOCK DIAGRAM



SyncFIFO is a trademark and the IDT logo is a registered trademark of Integrated Device Technology, Inc.

DESCRIPTION (CONTINUED)

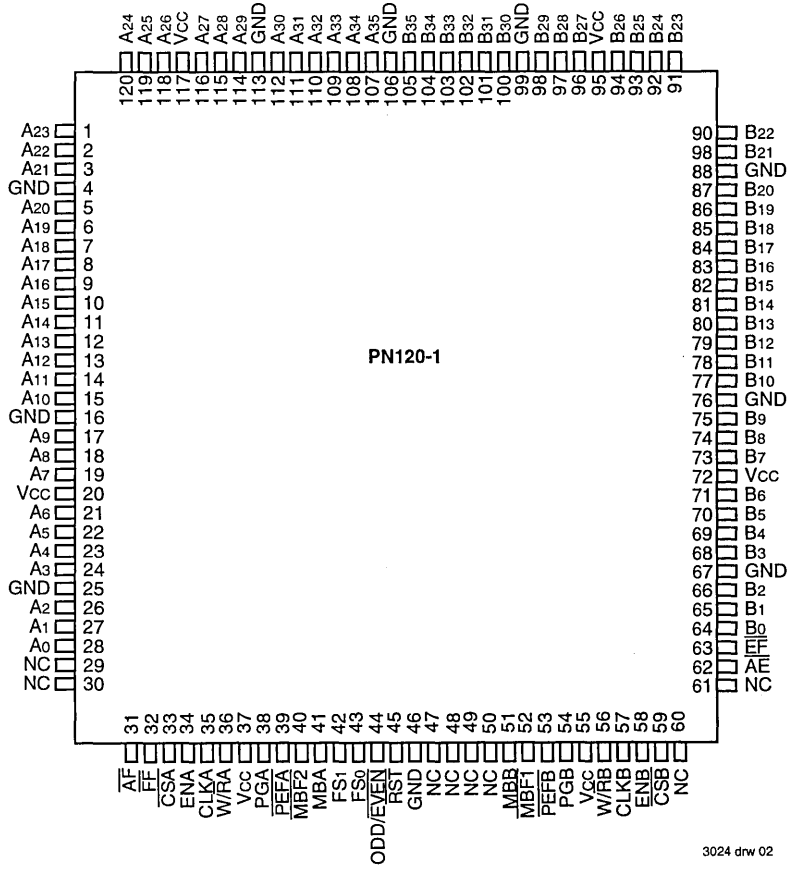
ignored if not desired. Parity generation can be selected for data read from each port. Two or more devices may be used in parallel to create wider data paths.

The IDT723611 is a synchronous (clocked) FIFO, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The Full-Flag ($\overline{FF}$) and Almost-Full ($\overline{AF}$) flag of the FIFO are two-stage synchronized to the port clock that writes data into its array (CLKA). The Empty Flag ($\overline{EF}$) and Almost-Empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to the port clock that reads data from its array.

The IDT723611 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATION

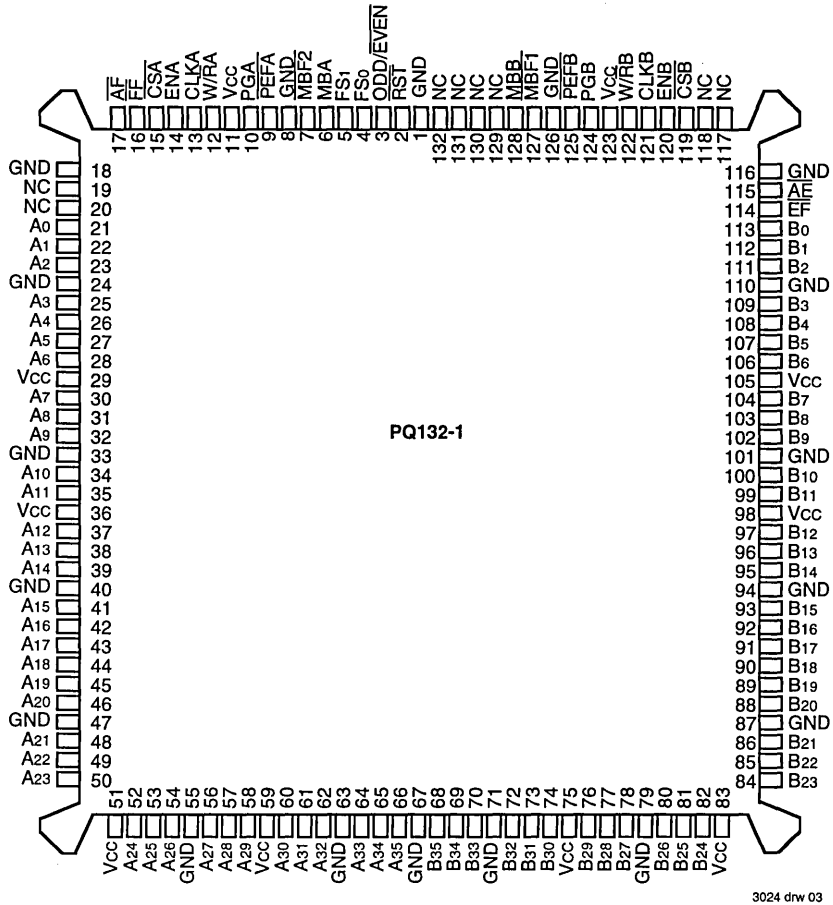


3024 drw 02

TQFP
TOP VIEW

Note:
1. NC = No internal connection

PIN CONFIGURATION (CONTINUED)



PQF PACKAGE
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
A0-A35	Port-A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AE}$	Almost-Empty Flag	O	Programmable almost-empty flag synchronized to CLKB. It is LOW when the number of words in the FIFO is less than or equal to the value in the offset register, X.
$\overline{AF}$	Almost-Full Flag.	O	Programmable almost-full flag synchronized to CLKA. It is LOW when the number of empty locations in the FIFO is less than or equal to the value in the offset register, X.
B0-B35	Port-B Data.	I/O	36-bit bidirectional data port for side B.
CLKA	Port-A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port-A and can be aynchronous or coincident to CLKB. $\overline{FF}$ and $\overline{AF}$ are synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port-B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through port-B and can be asynchronous or coincident to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port-A Chip Select	I	$\overline{CSA}$ must be LOW to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port-B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EF}$	Empty Flag	O	$\overline{EF}$ is synchronized to the LOW-to-HIGH transition of CLKB. When $\overline{EF}$ is LOW, the FIFO is empty, and reads from its memory are disabled. Data can be read from the FIFO to its output register when $\overline{EF}$ is HIGH. $\overline{EF}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after data is loaded into empty FIFO memory.
ENA	Port-A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A.
ENB	Port-B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B.
$\overline{FF}$	Full Flag	O	$\overline{FF}$ is synchronized to the LOW-to-HIGH transition of CLKA. When $\overline{FF}$ is LOW, the FIFO is full, and writes to its memory are disabled. $\overline{FF}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after reset.
FS1, FS0	Flag-Offset Selects	I	The LOW-to-HIGH transition of $\overline{RST}$ latches the values of FS0 and FS1, which loads one of four preset values into the almost-full and almost-empty offset register (X).
MBA	Port-A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a port-A read or write operation.
MBB	Port-B Mailbox Select	I	A HIGH level on MBB chooses a mailbox register for a port-B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register for output, and a LOW level selects the FIFO output register data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is set LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a port-B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH when the device is reset.

5

PIN DESCRIPTION (CONTINUED)

Symbol	Name	I/O	Description
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a port-A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH when the device is reset.
ODD/$\overline{EVEN}$	Odd/Even Parity Select	I	Odd parity is checked on each port when ODD/$\overline{EVEN}$ is HIGH, and even parity is checked when ODD/$\overline{EVEN}$ is LOW. ODD/$\overline{EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{PEFA}$	Port-A Parity Error Flag	O (Port A)	When any byte applied to terminals A0-A35 fails parity, $\overline{PEFA}$ is LOW. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the A0-A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is setup by having $\overline{CSA}$ LOW, ENA HIGH, W/$\overline{RA}$ LOW, MBA HIGH, and PGA HIGH, the $\overline{PEFA}$ flag is forced HIGH regardless of the state of A0-A35 inputs.
$\overline{PEFB}$	Port-B Parity Error Flag	O (Port B)	When any byte applied to terminals B0-B35 fails parity, $\overline{PEFB}$ is LOW. Bytes are organized as B0-B8, B9-B17, B18-B26, B27-B35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the B0-B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having $\overline{CSB}$ LOW, ENB HIGH, W/$\overline{RB}$ LOW, MBB HIGH, and PGB HIGH, the $\overline{PEFB}$ flag is forced HIGH regardless of the state of the B0-B35 inputs
PGA	Port-A Parity Generation	I	Parity is generated for mail2 register reads from port A when PGA is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35. The generated parity bits are output in the most significant bit of each byte.
PGB	Port-B Parity Generation	I	Parity is generated for data reads from port B when PGB is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as B0-B8, B9-B17, B18-B26, and B27-B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{RST}$	Reset	I	To reset the device, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST}$ is LOW. This sets the $\overline{AF}$, $\overline{MBF1}$, and $\overline{MBF2}$ flags HIGH and the $\overline{EF}$, $\overline{AE}$, and $\overline{FF}$ flags LOW. The LOW-to-HIGH transition of $\overline{RST}$ latches the status of the FS1 and FS0 inputs to select almost-full and almost-empty flag offset.
W/$\overline{RA}$	Port-A Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the high-impedance state when W/$\overline{RA}$ is HIGH.
W/$\overline{RB}$	Port-B Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the high-impedance state when W/$\overline{RB}$ is HIGH.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)(1)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	-0.5 to 7	V
V_I(2)	Input Voltage Range	-0.5 to V_{CC}+0.5	V
V_O(2)	Output Voltage Range	-0.5 to V_{CC}+0.5	V
I_{IK}	Input Clamp Current, (V_I < 0 or V_I > V_{CC})	±20	mA
I_{OK}	Output Clamp Current, (V_O = < 0 or V_O > V_{CC})	±50	mA
I_{OUT}	Continuous Output Current, (V_O = 0 to V_{CC})	±50	mA
I_{CC}	Continuous Current Through V_{CC} or GND	±500	mA
T_A	Operating Free Air Temperature Range	0 to 70	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C

Notes:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

5

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IH}	High-Level Input Voltage	2		V
V_{IL}	Low-Level Input Voltage		0.8	V
I_{OH}	High-Level Output Current		-4	mA
I_{OL}	Low-Level Output Current		8	mA
T_A	Operating Free-Air Temperature	0	70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Parameter	Test Conditions			Min.	Typ.(1)	Max.	Unit
V_{OH}	V_{CC} = 4.5V,	I_{OH} = -4 mA		2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA				0.5	V
I_{LI}	V_{CC} = 5.5 V,	V_I = V_{CC} or 0				±50	µA
I_{LO}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0				±50	µA
I_{CC}	V_{CC} = 5.5 V,	I_O = 0 mA, V_I = V_{CC} or GND	Outputs HIGH			60	mA
			Outputs LOW			130	
			Outputs Disabled			60	
C_{IN}	V_I = 0,	f = 1 MHz			4		pF
C_{OUT}	V_O = 0,	f = 1 MHZ			8		pF

Notes:
1. All typical values are at V_{CC} = 5 V, T_A = 25°C.

TIMING REQUIREMENTS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURES

Symbol	Parameter	IDT723611L15		IDT723611L20		IDT723611L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fS	Clock Frequency, CLKA or CLKB	–	66.7	–	50	–	33.4	Mhz
tCLK	Clock Cycle Time, CLKA or CLKB	15	–	20	–	30	–	Mhz
tCLKH	Pulse Duration, CLKA or CLKB HIGH	6	–	8	–	12	–	ns
tCLKL	Pulse Duration, CLKA or CLKB LOW	6	–	8	–	12	–	ns
tDS	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	4	–	5	–	6	–	ns
tENS1	$\overline{CSA}$, W/$\overline{RA}$, before CLKA↑; $\overline{CSB}$, W/$\overline{RB}$ before CLKB↑	6	–	6	–	7	–	ns
tENS2	ENA before CLKA↑; ENB before CLKB↑	4	–	5	–	6	–	ns
tENS3	MBA before CLKA↑; $\overline{ENB}$ before CLKB↑	4	–	5	–	6	–	ns
tPGS	Setup Time, ODD/$\overline{EVEN}$ and PGB before CLKB↑[1]	4	–	5	–	6	–	ns
tRSTS	Setup Time, $\overline{RST}$ LOW before CLKA↑ or CLKB↑[2]	5	–	6	–	7	–	ns
tFSS	Setup Time, FS0 and FS1 before $\overline{RST}$ HIGH	5	–	6	–	7	–	ns
tDH	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	1	–	1	–	1	–	ns
tENH1	$\overline{CSA}$, W/$\overline{RA}$ after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$ after CLKB↑	1	–	1	–	1	–	ns
tENH2	ENA after CLKA↑; ENB after CLKB↑	1		1		1		ns
tENH3	MBA after CLKA↑; MBB after CLKB↑	1		1		1		ns
tPGH	Hold TIme, ODD/$\overline{EVEN}$ and PGB after CLKB↑[1]	0	–	0	–	0	–	ns
tRSTH	Hold Time, $\overline{RST}$ LOW after CLKA↑ or CLKB↑[2]	6	–	6	–	7	–	ns
tFSH	Hold Time, FS0 and FS1 after $\overline{RST}$ HIGH	4	–	4	–	4	–	ns
tSKEW1[3]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{EF}$, $\overline{FF}$	8	–	8	–	10	–	ns
tSKEW2[3]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{AE}$, $\overline{AF}$	9	–	16	–	20	–	ns

Notes:
1. Only applies for a rising edge of CLKB that does a FIFO read.
2. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
3. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 30 pF

Symbol	Parameter	IDT723611L15		IDT723611L20		IDT723611L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fS	Clock Frequency, CLKA or CLKB	–	66.7	–	50	–	33.4	MHz
tA	Access Time, CLKB↑ to B0-B35	2	10	2	12	2	15	ns
tWFF	Propagation Delay Time, CLKA↑ to $\overline{FF}$	2	10	2	12	2	15	ns
tREF	Propagation Delay Time, CLKB↑ to $\overline{EF}$	2	10	2	12	2	15	ns
tPAE	Propagation Delay Time, CLKB↑ to $\overline{AE}$	2	10	2	12	2	15	ns
tPAF	Propagation Delay Time, CLKA↑ to $\overline{AF}$	2	10	2	12	2	15	ns
tPMF	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	1	9	1	12	1	15	ns
tPMR	Propagation Delay Time, CLKA↑ to B0-B35[1] and CLKB↑ to A0-A35[2]	3	12	3	14	3	16	ns
tMDV	Propagation Delay Time, MBB to B0-B35 Valid	1	11	1	11.5	1	12	ns
tPDPE	Propagation Delay Time, A0-A35 Valid to $\overline{PEFA}$ Valid; B0-B35 Valid to $\overline{PEFB}$ Valid	3	12	3	13	3	14	ns
tPOPE	Propagation Delay Time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	3	11	3	12	3	14	ns
tPOPB[3]	Propagation Delay Time, ODD/$\overline{EVEN}$ to Parity Bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	12	2	13	2	15	ns
tPEPE	Propagation Delay Time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGAto $\overline{PEFA}$; $\overline{CSB}$, ENB, W/$\overline{RB}$, MBB, or PGB to $\overline{PEFB}$	1	12	1	13	1	15	ns
tPEPB[3]	Propagation Delay Time, $\overline{CSA}$, ENA W/$\overline{RA}$, MBA, or PGA to Parity Bits (A8, A17, A26, A35); $\overline{CSB}$, ENB, W/$\overline{RB}$, MBB, or PGB to Parity Bits (B8, B17, B26, B35)	3	14	3	15	3	16	ns
tRSF	Propagation Delay Time, $\overline{RST}$ to $\overline{AE}$ LOW and ($\overline{AF}$, $\overline{MBF1}$, $\overline{MBF2}$) HIGH	1	15	1	20	1	30	ns
tEN	Enable Time, $\overline{CSA}$ and W/$\overline{RA}$ LOW to A0-A35 Active and $\overline{CSB}$ LOW and $\overline{W}$/RB HIGH to B0-B35 Active	2	10	2	12	2	14	ns
tDIS	Disable Time, $\overline{CSA}$ or W/$\overline{RA}$ HIGH to A0-A35 at high impedance and $\overline{CSB}$ HIGH or $\overline{W}$/RB LOW to B0-B35 at high impedance	1	9	1	10	1	11	ns

Notes:
1. Writing data to the mail1 register when the B0-B35 outputs are active and MBB is HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.
3. Only applies when reading data from a mail register.

5

SIGNAL DESCRIPTION

RESET ($\overline{RST}$)

The IDT723611 is reset by taking the reset ($\overline{RST}$) input LOW for at least four port-A clock (CLKA) and four port-B clock (CLKB) LOW-to-HIGH transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of the FIFO and forces the full-flag ($\overline{FF}$) LOW, the empty flag ($\overline{EF}$) LOW, the almost-empty flag ($\overline{AE}$) LOW, and the almost-full flag ($\overline{AF}$) HIGH. A reset also forces the mailbox flags ($\overline{MBF1}$, $\overline{MBF2}$) HIGH. After a reset, $\overline{FF}$ is set HIGH after two LOW-to-HIGH transitions of CLKA.

Almost-Full and Almost-Empty Flag Offset Register (X)	FS1	FS0	$\overline{RST}$
16	H	H	↑
12	H	L	↑
8	L	H	↑
4	L	L	↑

Table 1. Flag Programming

The device must be reset after power up before data is written to its memory.

A LOW-to-HIGH transition on the $\overline{RST}$ input loads the almost-full and almost-empty offset register (X) with the value selected by the flag select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1.

FIFO WRITE/READ OPERATION

The state of the port-A data (A0-A35) outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{RA}$). The A0-A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW. Data is loaded into the FIFO from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH, MBA is LOW, and $\overline{FF}$ is HIGH (see Table 2).

The port-B control signals are identical to those of port A. The state of the port-B data (B0-B35) outputs is controlled by the port-B chip select ($\overline{CSB}$) and the port-B write/read select (W/$\overline{RB}$). The B0-B35 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is HIGH. The B0-B35 outputs are active when both $\overline{CSB}$ and W/$\overline{RB}$ are LOW. Data is read from the FIFO to the B0-B35 outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, W/$\overline{RB}$ is LOW, ENB is HIGH, MBB is LOW, and $\overline{EF}$ is HIGH (see Table 3).

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0-A35 Outputs	Port Functions
H	X	X	X	X	In High-Impedance State	None
L	H	L	X	X	In High-Impedance State	None
L	H	H	L	↑	In High-Impedance State	FIFO Write
L	H	H	H	↑	In High-Impedance State	Mail1 Write
L	L	L	L	X	Active, Mail2 Register	None
L	L	H	L	↑	Active, Mail2 Register	None
L	L	L	H	X	Active, Mail2 Register	None
L	L	H	H	↑	Active, Mail2 Register	Mail2 Read (set $\overline{MBF2}$ HIGH)

Table 2. Port-A Enable Function Table

$\overline{CSB}$	W/$\overline{RB}$	ENB	MBB	CLKB	B0-B35 Outputs	Port Functions
H	X	X	X	X	In High-Impedance State	None
L	H	L	X	X	In High-Impedance State	None
L	H	H	L	↑	In High-Impedance State	None
L	H	H	H	↑	In High-Impedance State	Mail2 Write
L	L	L	L	X	Active, FIFO Output Register	None
L	L	H	L	↑	Active, FIFO Output Register	FIFO Read
L	L	L	H	X	Active, Mail1 Register	None
L	L	H	H	↑	Active, Mail1 Register	Mail1 Read (set $\overline{MBF1}$ HIGH)

Table 3. Port-B Enable Function Table

The setup and hold-time constraints to the port clocks for the port chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, W/$\overline{RB}$) are only for enabling write and read operations and are not related to HIGH-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port's chip select and write/read select can change states during the setup and hold-time window of the cycle.

SYNCHRONIZED FIFO FLAGS

Each FIFO flag is synchronized to its port clock through two flip-flop stages. This is done to improve the flags' reliability by reducing the probability of mestastable events on their outputs when CLKA and CLKB operate asynchronously to one another. $\overline{FF}$ and $\overline{AF}$ are synchronized to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to CLKB. Table 4 shows the relationship to the flags to the FIFO.

EMPTY FLAG ($\overline{EF}$)

The FIFO empty flag is synchronized to the port clock that reads data from its array (CLKB). When the empty flag is HIGH, new data can be read to the FIFO output register. When the empty flag is LOW, the FIFO is empty and attempted FIFO reads are ignored.

The FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to the FIFO can be read to the FIFO output register in a minimum of three port-B clock (CLKB) cycles. Therefore, an empty flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two CLKB cycles have not elapsed since the time the word was written. The empty flag of the FIFO is set HIGH by the second LOW-to-HIGH transition of CLKB, and the new data word can be read to the FIFO output register in the following cycle.

A LOW-to-HIGH transition on CLKB begins the first synchronized cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see figure 4).

Number of Words in the FIFO	Synchronized to CLKB		Synchronized to CLKA	
	$\overline{EF}$	$\overline{AE}$	$\overline{AF}$	$\overline{FF}$
0	L	L	H	H
1 to X	H	L	H	H
(X+1) to [64-(X+1)]	H	H	H	H
(64-X) to 63	H	H	L	H
64	H	H	L	L

Table 4. FIFO Flag Operation

Note:
X is the value in the almost-empty flag and almost-full flag register.

FULL FLAG ($\overline{FF}$)

The FIFO full flag is synchronized to the port clock that writes data to its array (CLKA). When the full flag is HIGH, an SRAM location is free to receive new data. No memory locations are free when the full flag is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to the FIFO, its write pointer is incremented. The state machine that controls the full flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full-1, or full-2. From the time a word is read from the FIFO, its previous memory location is ready to be written in a minimum of three port-A clock cycles. Therefore, a full flag is LOW if less than two CLKA cycles have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on CLKA after the read sets the full flag HIGH and data can be written in the following clock cycle.

A LOW-to-HIGH transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see figure 5).

ALMOST-EMPTY FLAG ($\overline{AE}$)

The FIFO almost empty-flag is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls the almost-empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset above). The almost-empty flag is LOW when the FIFO contains X or less words in memory and is HIGH when the FIFO contains (X+1) or more words.

Two LOW-to-HIGH transitions on the port-B clock (CLKB) are required after a FIFO write for the almost-empty flag to reflect the new level of fill. Therefore, the almost-empty flag of a FIFO containing (X+1) or more words remains LOW if two CLKB cycles have not elapsed since the write that filled the memory to the (X+1) level. The almost-empty flag is set HIGH by the second CLKB LOW-to-HIGH transition after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition on CLKB begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see figure 6).

ALMOST FULL FLAG ($\overline{AF}$)

The FIFO almost-full flag is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an almost-full flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost full, almost full-1, or almost full-2. The almost-full state is defined by the value of the almost-full and almost-

empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset above). The almost-full flag is LOW when the FIFO contains (64-X) or more words in memory and is HIGH when the FIFO contains [64-(X+1)] or less words.

Two LOW-to-HIGH transitions on the port-A clock (CLKA) are required after a FIFO read for the almost-full flag to reflect the new level of fill. Therefore, the almost-full flag of a FIFO containing [64-(X+1)] or less words remains LOW if two CLKA cycles have not elapsed since the read that reduced the number of words in memory to [64-(X+1)]. The almost-full flag is set HIGH by the second CLKA LOW-to-HIGH transition after the FIFO read that reduces the number of words in memory to [64-(X+1)]. A LOW-to-HIGH transition on CLKA begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [64-(X+1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see figure 7).

MAILBOX REGISTERS

Two 36-bit bypass registers are on the IDT723611 to pass command and control information between port A and port B. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A LOW-to-HIGH transition on CLKA writes A0-A35 data to the mail1 register when port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH. A LOW-to-HIGH transition on CLKB writes B0-B35 data to the mail2 register when port-B write is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB with MBB HIGH. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while its mail flag is LOW.

When the port-B data (B0-B35) outputs are active, the data on the bus comes from the FIFO output register when the port-B mailbox select (MBB) input is LOW and from the mail1 register when MBB is HIGH. Mail2 data is always present on the port-A data (A0-A35) outputs when they are active. The mail1 register flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a port-B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB with MBB HIGH. The mail2 register flag ($\overline{MBF2}$) is set HIGH by a LOW-to-HIGH transition on CLKA when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

PARITY CHECKING

The port-A (A0-A35) inputs and port-B (B0-B35) inputs each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the input bus is reported by a LOW level on the port parity error flag ($\overline{PEFA}$, $\overline{PEFB}$). Odd or even parity checking can be selected, and the parity error flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/$\overline{EVEN}$) select input. A parity error on one or more bytes of a port is reported by a LOW level on the corresponding port parity error flag ($\overline{PEFA}$, $\overline{PEFB}$) output. Port-A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35, and port-B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35. When odd/even parity is selected, a port parity error flag ($\overline{PEFA}$, $\overline{PEFB}$) is LOW if any byte on the port has an odd/even number of LOW levels applied to its bits.

The four parity trees used to check the A0-A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA=HIGH). When port-A read from the mail2 register with parity generation is selected with $\overline{CSA}$ LOW, ENA HIGH, W/$\overline{RA}$ LOW, MBA HIGH, and PGA HIGH, the port-A parity error flag ($\overline{PEFA}$) is held HIGH regardless of the levels applied to the A0-A35 inputs. Likewise, the parity trees used to check the B0-B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB=HIGH). When a port-B read from the mail1 register with parity generation is selected with $\overline{CSB}$ LOW, ENB HIGH, W/$\overline{RB}$ LOW, MBB HIGH, and PGB HIGH, the port-B parity error flag ($\overline{PEFB}$) is held HIGH regardless of the levels applied to the B0-B35 inputs.

PARITY GENERATION

A HIGH level on the port-A parity generate select (PGA) or port-B generate select (PGB) enables the IDT723611 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all thirty-six inputs regardless of the state of the parity generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{EVEN}$ select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port-B parity generate select (PGB) and ODD/$\overline{EVEN}$ have setup and hold time constraints to the port-B clock (CLKB) for a rising edge of CLKB used to read a new word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0-B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0-A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port write/read select (W/$\overline{RA}$, W/$\overline{RB}$) input is LOW, the port mail select (MBA, MBB) input is HIGH, chip select ($\overline{CSA}$, $\overline{CSB}$) is LOW, enable ENA, ENB) is HIGH, and the port parity generate select (PGA, PGB) is HIGH. Generating parity for mail register data does not change the contents of the register.

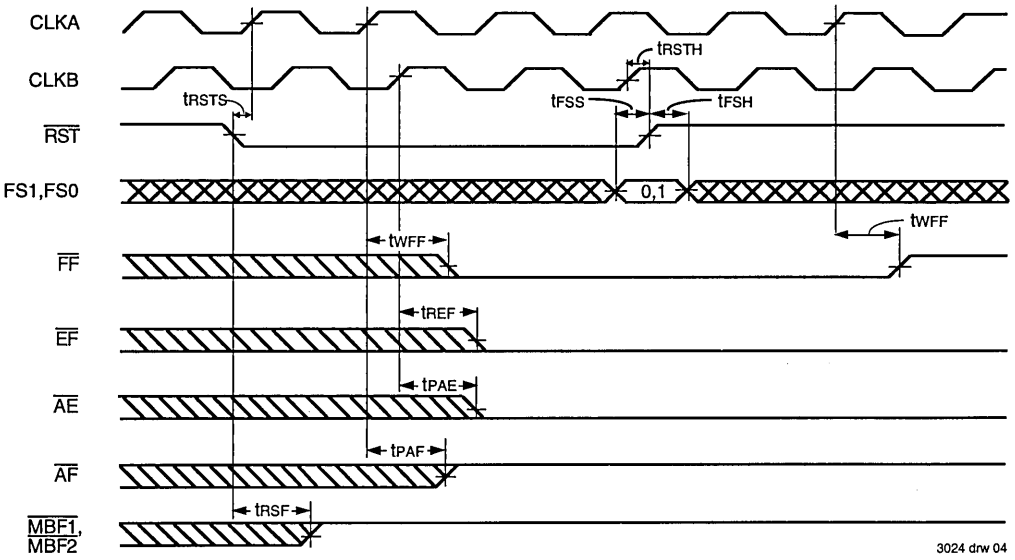


Figure 1. Device Reset Loading the X Register with the Value of Eight

5

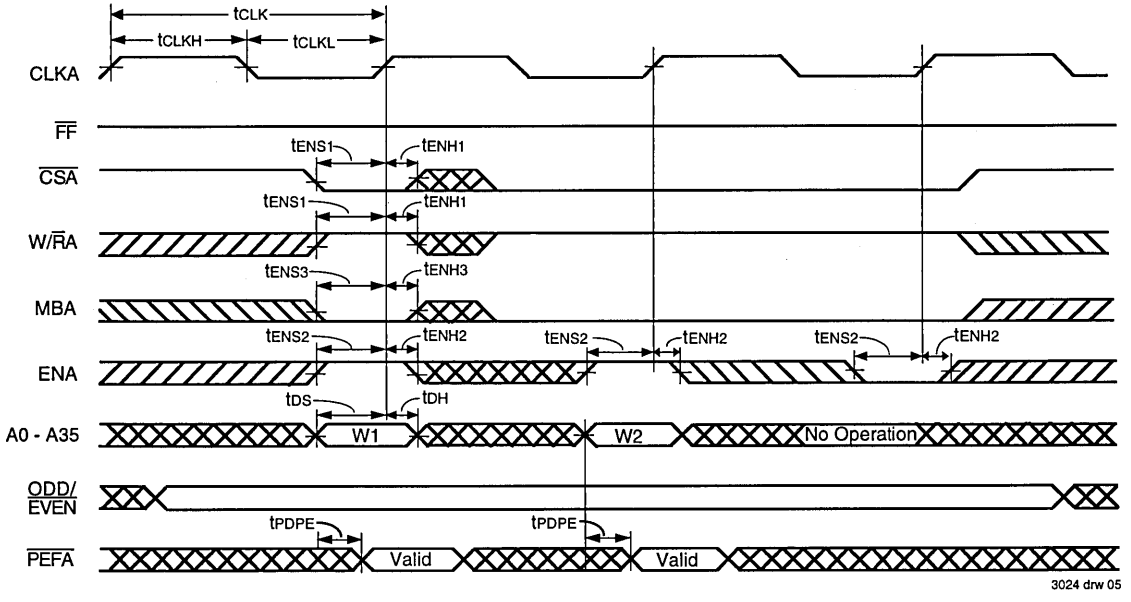


Figure 2. FIFO Write Cycle Timing

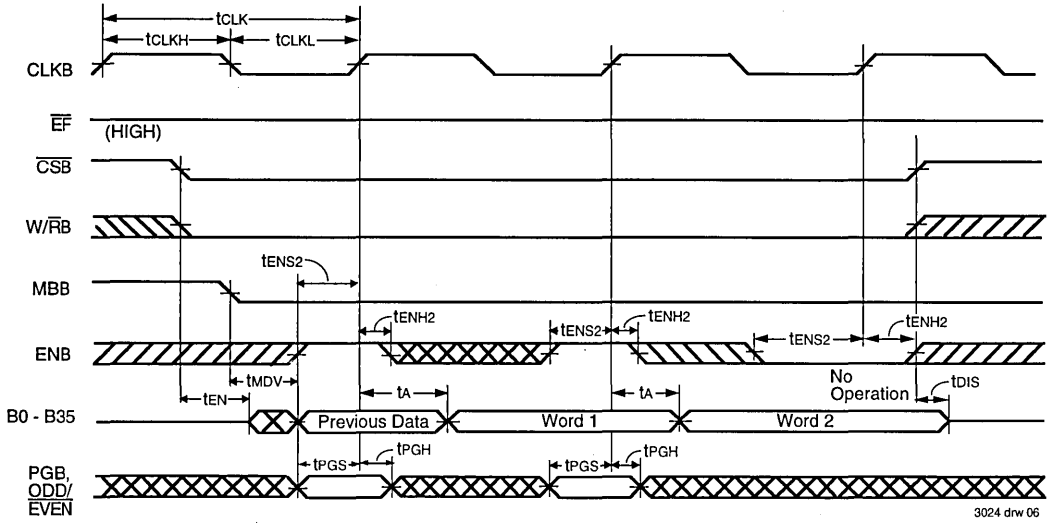
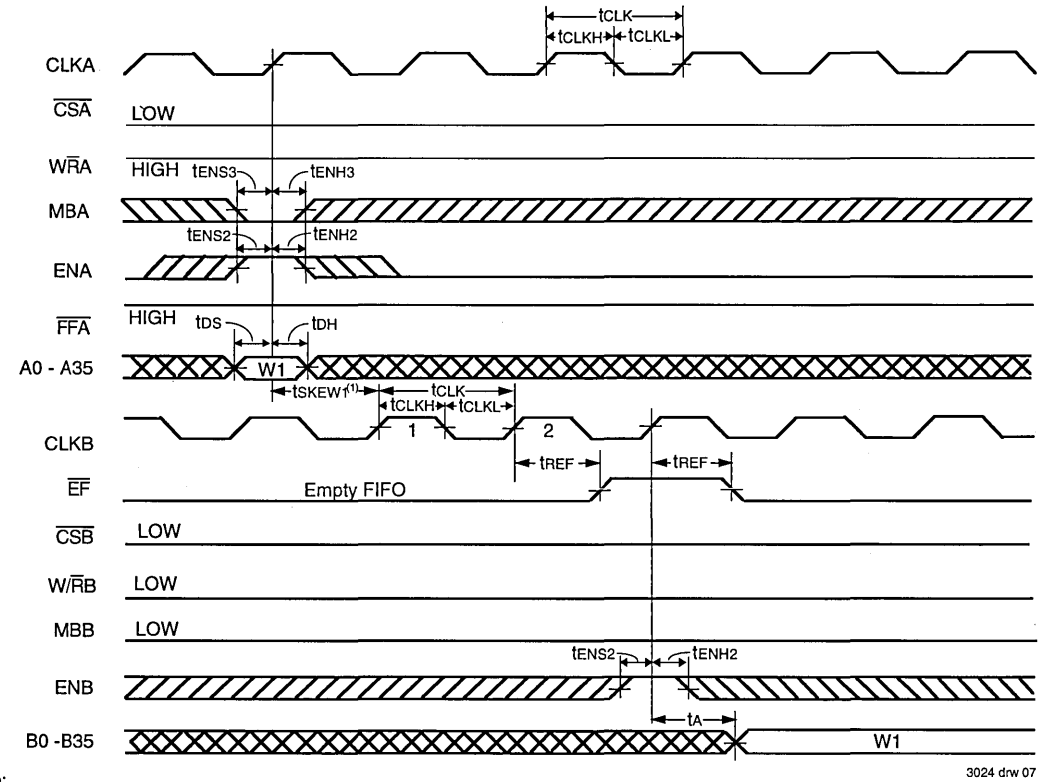
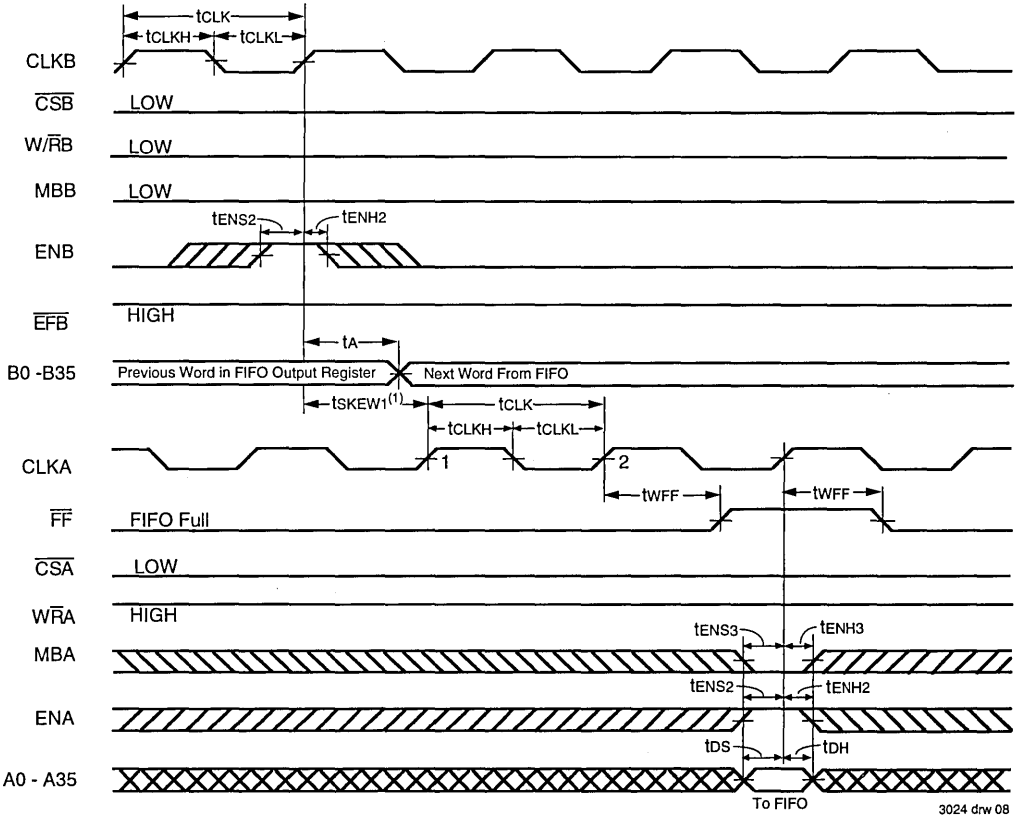


Figure 3. FIFO Read Cycle Timing



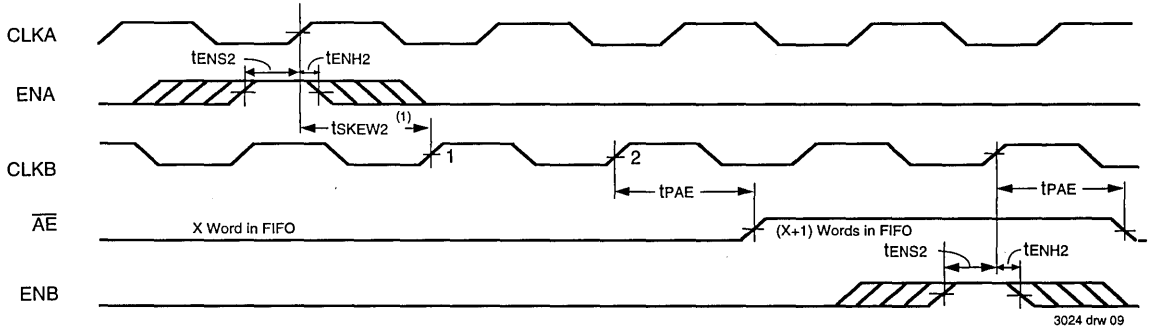
Note:
1. tSKEW1 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EF}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW1, then the transition of $\overline{EF}$ HIGH may occur one CLKB cycle later than shown.

Figure 4. $\overline{EF}$ Flag Timing and First Data Read when the FIFO is Empty



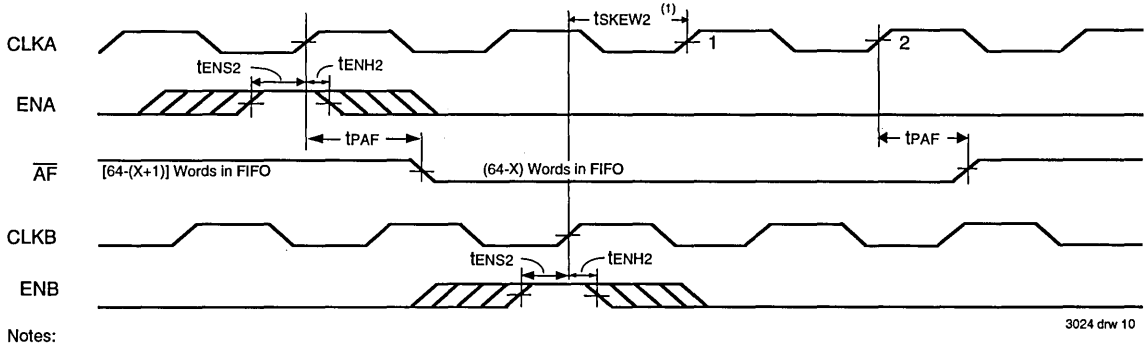
Note:
1. tSKEW1 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW1, then the transition of $\overline{FF}$ HIGH may occur one CLKA cycle later than shown.

Figure 5. $\overline{FF}$ Flag Timing and First Available Write when the FIFO is Full



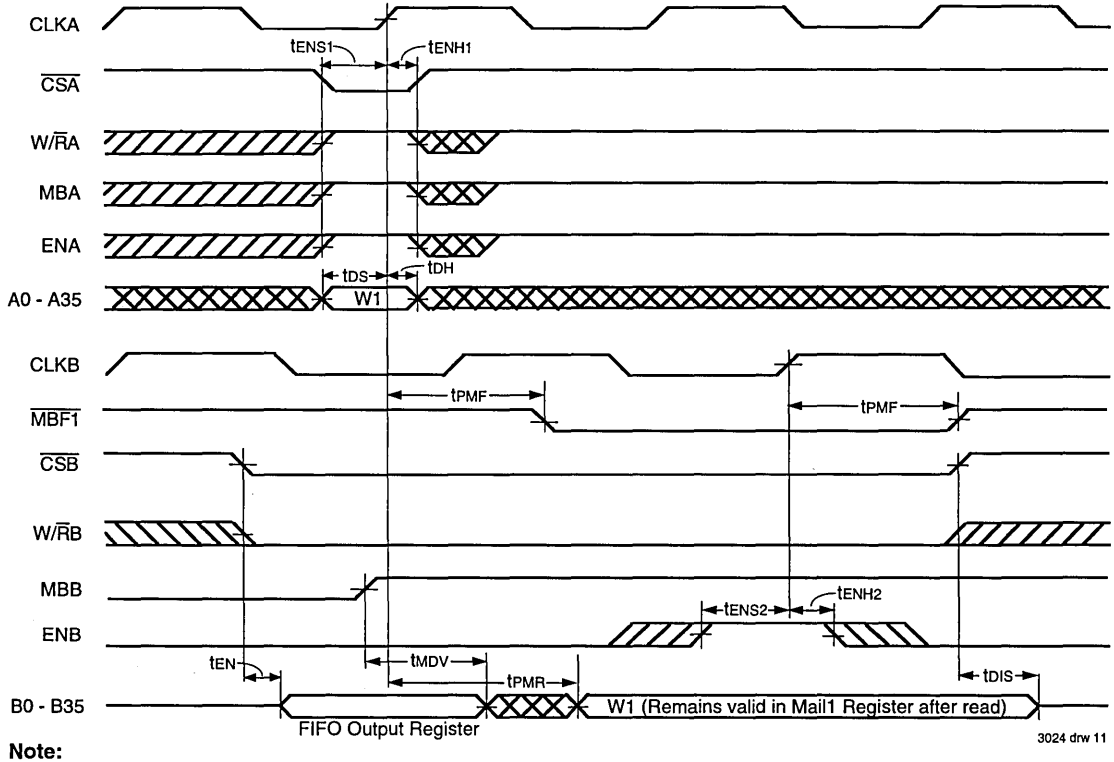
Notes:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then $\overline{AE}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

Figure 6. Timing for $\overline{AE}$ when the FIFO is Almost Empty



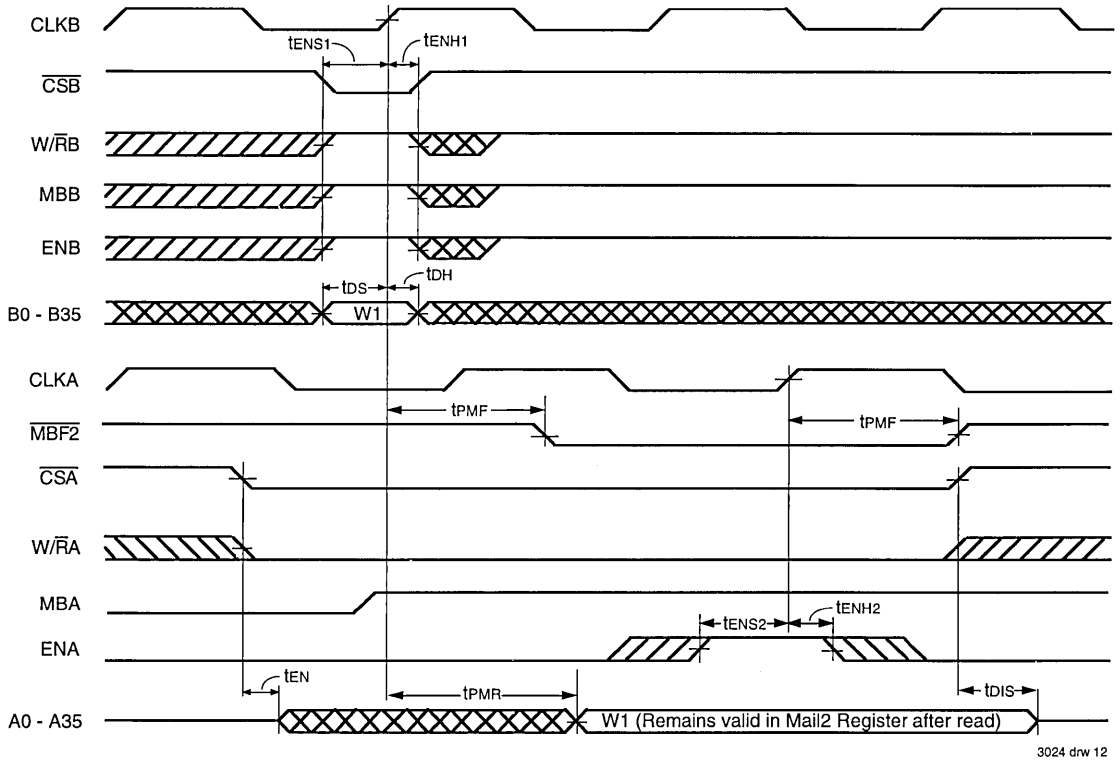
Notes:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then $\overline{AF}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO write ($\overline{CSA}$ = L, W/$\overline{RA}$ = H, MBA = L), FIFO read ($\overline{CSB}$ = L, W/$\overline{RB}$ = L, MBB = L).

Figure 7. Timing for $\overline{AF}$ when the FIFO is Almost Full



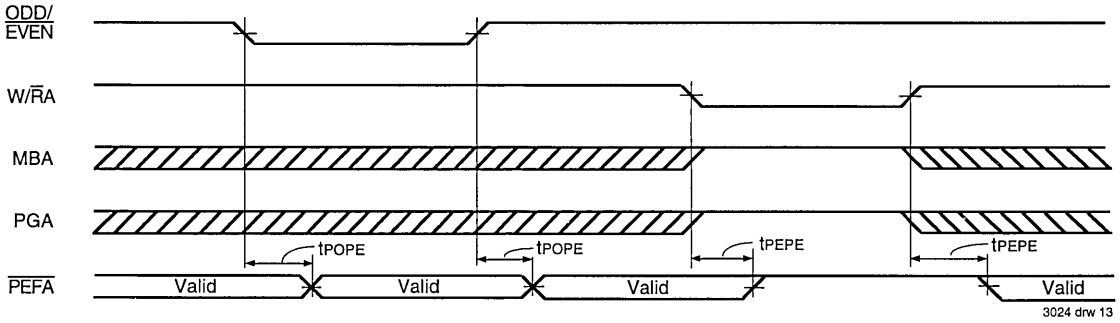
Note:
1. Port-B parity generation off (PGB = L)

Figure 8. Timing for Mail1 Register and $\overline{MBF1}$ Flag



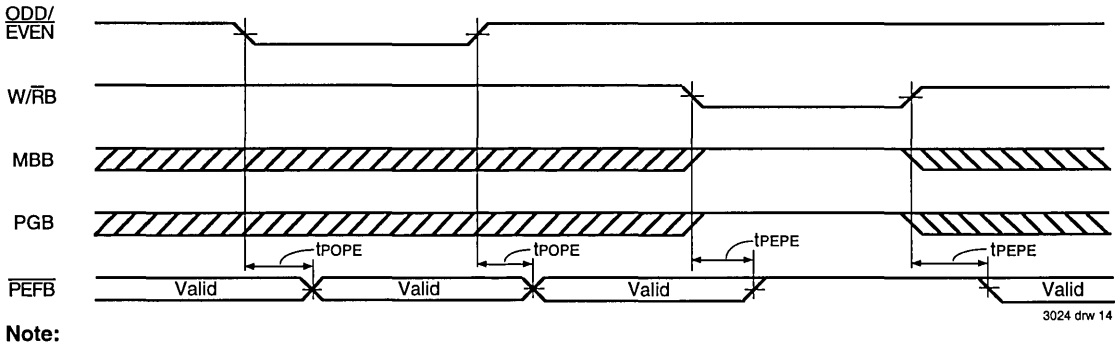
Note:
1. Port-A parity generation off (PGA = L)

Figure 9. Timing for Mail2 Register and $\overline{MBF2}$ Flag



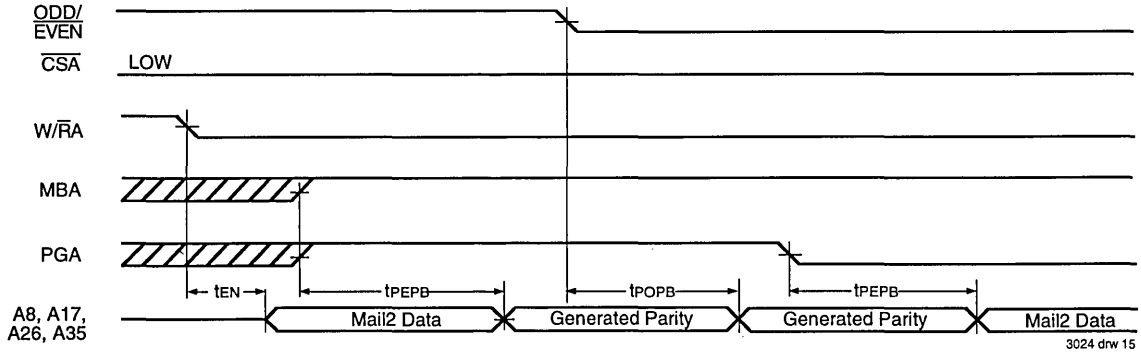
Note:
1. $\overline{CSA}$ = L and ENA = H.

Figure 10. ODD/$\overline{EVEN}$, W/RA, MBA, and PGA to $\overline{PEFA}$ Timing



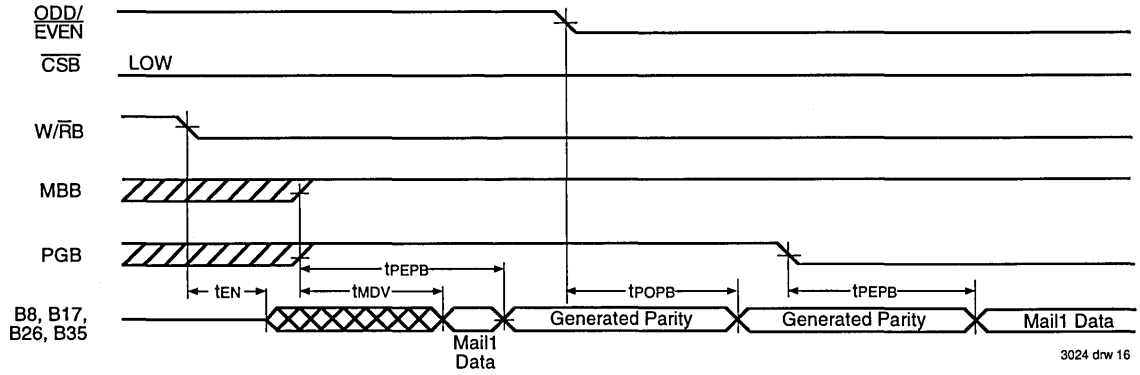
Note:
1. $\overline{CSB}$ = L and ENB = H.

Figure 11. ODD/$\overline{EVEN}$, W/RB, MBB, and PGB to $\overline{PEFB}$ Timing



Note:
1. ENA = H.

Figure 12. Parity Generation Timing when reading from the Mail2 Register



Note:
1. ENB = H.

Figure 13. Parity Generation Timing when reading from the Mail1 Register

TYPICAL CHARACTERISTICS

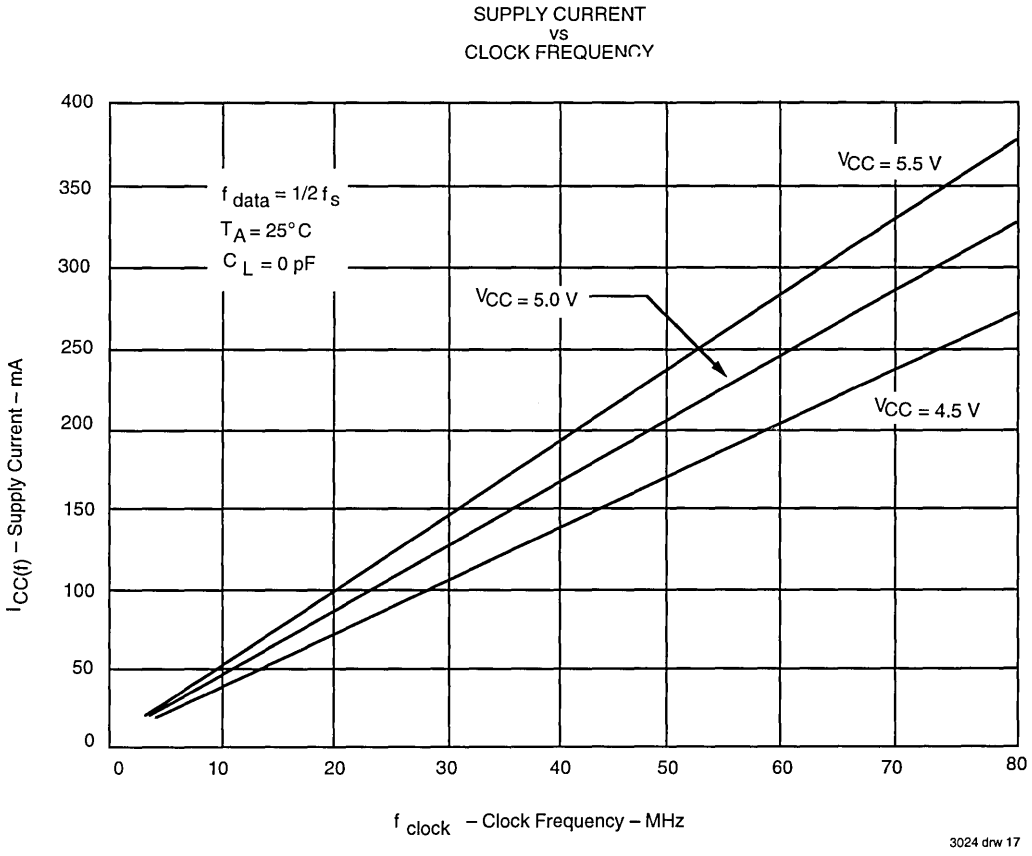


Figure 14.

CALCULATING POWER DISSIPATION

The $I_{CC(f)}$ data for the graph was taken while simultaneously reading and writing the FIFO on the IDT723611 with CLKA and CLKB operating at frequency fs. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitance load per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from FIgure 14, the maximum power dissipation (PT) of the IDT723611 may be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times V_{OH} - V_{OL})^2 \times f_O)$$

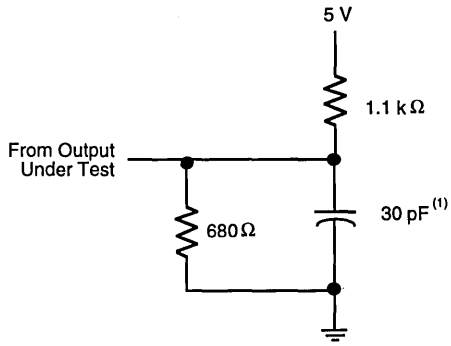
where:

C_L	=	output capacitance load
f_O	=	switching frequency of an output
V_{OH}	=	output high-level voltage
V_{OL}	=	output low-level voltage

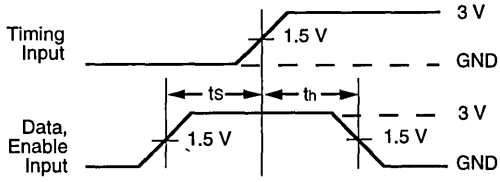
When no read or writes are occurring on the IDT723611, the power dissipated by a single clock (CLKA or CLKB) input running at frequency fs is calculated by:

$$P_T = V_{CC} \times f_s \times 0.290 \text{ mA/MHz}$$

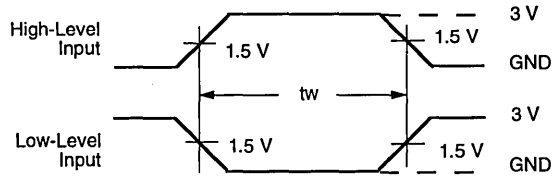
PARAMETER MEASUREMENT INFORMATION



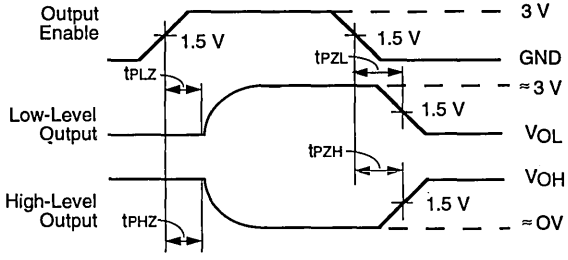
PROPAGATION DELAY LOAD CIRCUIT



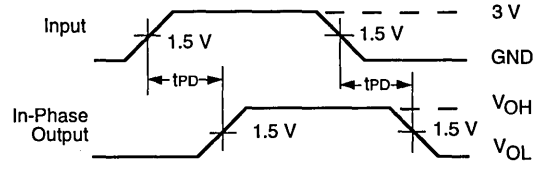
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES



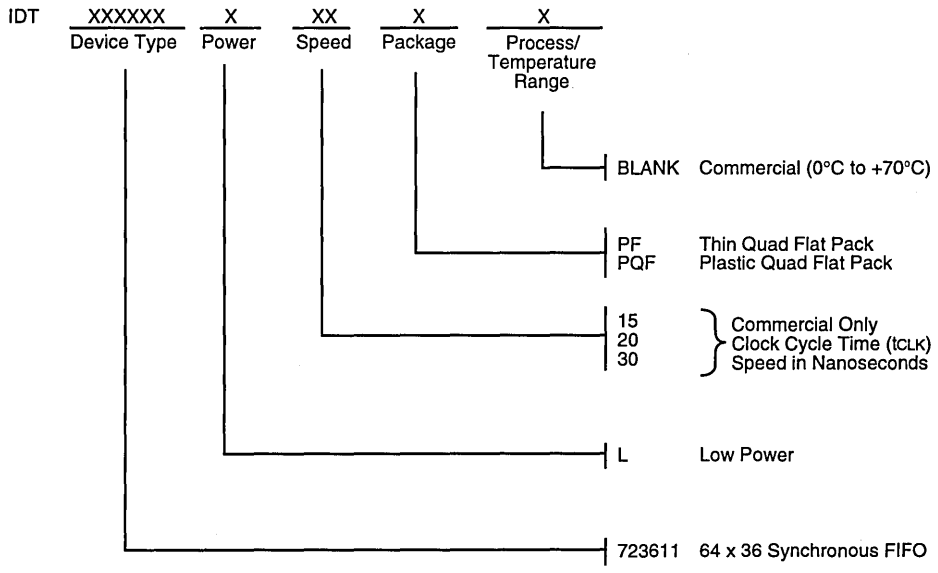
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

3024 drw 18

Note:
1. Includes probe and jig capacitance.

Figure 15. Load Circuit and Voltage Waveforms

ORDERING INFORMATION



3024 drw 19

5

Integrated Device Technology, Inc.

CMOS Clocked FIFO With Bus Matching and Byte Swapping 64 x 36

PRELIMINARY
IDT723613

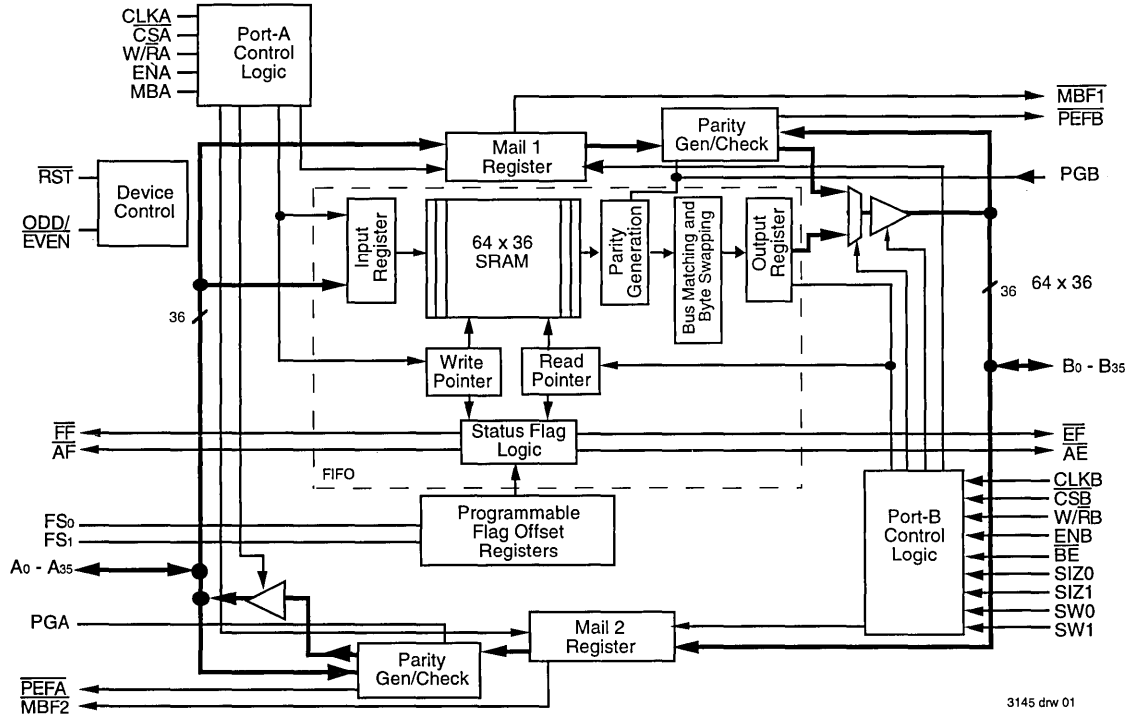
FEATURES:

- Free-running CLKA and CLKB may be asynchronous or coincident (permits simultaneous reading and writing of data on a single clock edge)
- 64 x 36 storage capacity FIFO buffering data from Port A to Port B
- Mailbox bypass registers in each direction
- Dynamic Port B bus sizing of 36-bits (long word), 18-bits (word), and 9-bits (byte)
- Selection of Big- or Little-Endian format for word and byte bus sizes
- Three modes of byte-order swapping on Port B
- Programmable Almost-Full and Almost-Empty flags
- Microprocessor interface control logic
- $\overline{FF}$, $\overline{AF}$ flags synchronized by CLKA
- $\overline{EF}$, $\overline{AE}$ flags synchronized by CLKB
- Passive parity checking on each Port
- Parity Generation can be selected for each Port
- Low-power advanced BiCMOS technology
- Supports clock frequencies up to 67 MHz
- Fast access times of 10 ns
- Available in 132-pin quad flatpack (PQF) or space-saving 120-pin thin quad flatpack (TQFP)

DESCRIPTION:

The IDT723613 is a monolithic, high-speed, low-power, BiCMOS synchronous (clocked) FIFO memory which supports clock frequencies up to 67 MHz and has read-access times as fast as 10 ns. The 64 x 36 dual-port SRAM FIFO buffers data from port A to port B. The FIFO has flags to indicate empty and full conditions, and two programmable flags, Almost-Full ($\overline{AF}$) and Almost-Empty ($\overline{AE}$), to indicate when a selected number of words is stored in memory. FIFO data on port B can be output in 36-bit, 18-bit, and 9-bit formats

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION (CONTINUED)

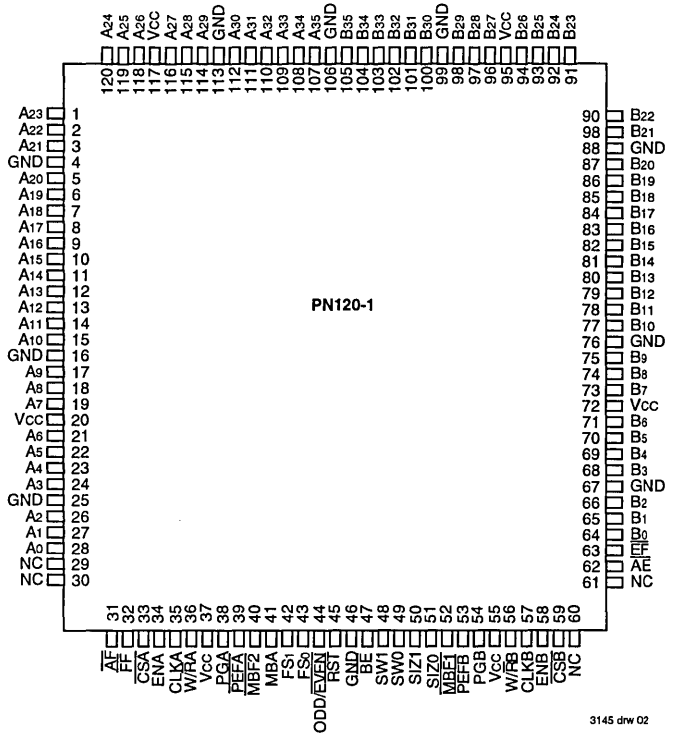
with a choice of big- or little-endian configurations. Three modes of byte-order swapping are possible with any bus-size selection. Communication between each port can bypass the FIFO via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if not desired. Parity generation can be selected for data read from each port. Two or more devices may be used in parallel to create wider data paths.

The IDT723613 is a synchronous (clocked) FIFO, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple interface between microprocessors and/or buses with synchronous interfaces.

The Full Flag ($\overline{FF}$) and Almost-Full ($\overline{AF}$) flag of the FIFO are two-stage synchronized to the port clock (CLKA) that writes data into its array. The Empty Flag ($\overline{EF}$) and Almost-Empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to the port clock (CLKB) that reads data from its array.

The IDT723613 is characterized for operation from 0°C to 70°C.

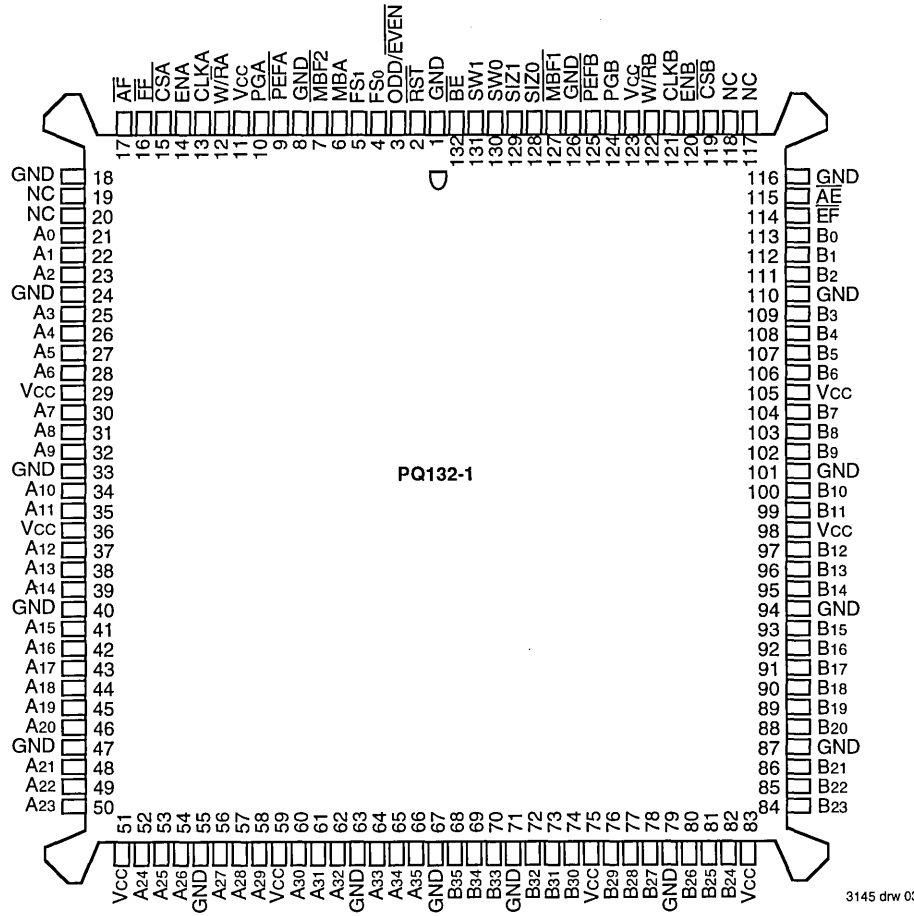
PIN CONFIGURATION



NOTE:
1. NC = No internal connection

TQFP
TOP VIEW

PIN CONFIGURATION (CONTINUED)



NOTES:
1. NC = No internal connection.
2. Uses Yamaichi socket IC51-1324-828.

PQF PACKAGE (2)
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
A0-A35	Port A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AE}$	Almost-Empty Flag	O Port B	Programmable almost-empty flag synchronized to CLKB. It is LOW when Port B the number of 36-bit words in the FIFO is less than or equal to the value in the offset register, X.
$\overline{AF}$	Almost-Full Flag	O Port A	Programmable almost-full flag synchronized to CLKA. It is LOW when the number of 36-bit empty locations in the FIFO is less than or equal to the value in the offset register, X.
B0-B35	Port B Data	I/O	36-bit bidirectional data port for side B
$\overline{BE}$	Big-Endian Select	I	Selects the bytes on port B used during byte or word FIFO reads. A LOW on $\overline{BE}$ selects the most significant bytes on B0-B35 for use, and a HIGH selects the least significant bytes.
CLKA	Port A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{FF}$ and $\overline{AF}$ are synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. Port-B byte swapping and data port sizing operations are also synchronous to the LOW-to-HIGH transition of CLKB. $\overline{EF}$ and $\overline{AE}$ are synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port A Chip Select	I	$\overline{CSA}$ must be LOW to enable a LOW-to-HIGH transition of CLKA to read or write data on port A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on port B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EF}$	Empty Flag	O Port B	$\overline{EF}$ is synchronized to the LOW-to-HIGH transition of CLKB. When $\overline{EF}$ is LOW, the FIFO is empty, and reads from its memory are disabled. Data can be read from the FIFO to its output register when $\overline{EF}$ is HIGH. $\overline{EF}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after data is loaded into empty FIFO memory.
ENA	Port A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port A.
ENB	Port B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on port B.
$\overline{FF}$	Full Flag	O Port A	$\overline{FF}$ is synchronized to the LOW-to-HIGH transition of CLKA. When $\overline{FF}$ is LOW, the FIFO is full, and writes to its memory are disabled. $\overline{FF}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after reset.
FS1, FS0	Flag Offset Selects	I	The LOW-to-HIGH transition of $\overline{RST}$ latches the values of FS0 and FS1, which loads one of four preset values into the almost-full flag and almost-empty flag offsets.
MBA	Port A Mailbox Select	I	A high level on MBA chooses a mailbox register for a port A read or write operation. When the A0-A35 outputs are active, mail2 register data is output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is set LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a port B read is selected and both SIZ1 and SIZ0 are HIGH. $\overline{MBF1}$ is set HIGH when the device is reset.
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is set LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a port A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH when the device is reset.

5

PIN DESCRIPTION (CONTINUED)

Symbol	Name	I/O	Description
ODD/$\overline{\text{EVEN}}$	Odd/Even Parity Select	I	Odd parity is checked on each port when ODD/$\overline{\text{EVEN}}$ is HIGH, and even parity is checked when ODD/$\overline{\text{EVEN}}$ is LOW. ODD/$\overline{\text{EVEN}}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{\text{PEFA}}$	Port A Parity Error Flag	O (Port A)	When any byte applied to terminals A0-A35 fails parity, $\overline{\text{PEFA}}$ is LOW. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{\text{EVEN}}$ input. The parity trees used to check the A0-A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is set up by having $\overline{\text{CSA}}$ LOW, ENA HIGH, W/$\overline{\text{RA}}$ LOW, MBA HIGH and PGA HIGH, the $\overline{\text{PEFA}}$ flag is forced HIGH regardless of the state of the A0-A35 inputs.
$\overline{\text{PEFB}}$	Port B Parity Error Flag	O (Port B)	When any valid byte applied to terminals B0-B35 fails parity, $\overline{\text{PEFB}}$ is LOW. Bytes are organized as B0-B8, B9-B17, B-18-B26, and B27-B35, with the most significant bit of each byte serving as the parity bit. A byte is valid when it is used by the bus size selected for port B. The type of parity checked is determined by the state of the ODD/$\overline{\text{EVEN}}$ input. The parity trees used to check the B0-B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is set up by having $\overline{\text{CSB}}$ LOW, ENB HIGH, W/$\overline{\text{RB}}$ LOW, SIZ1 and SIZ0 HIGH and PGB HIGH, the $\overline{\text{PEFB}}$ flag is forced HIGH regardless of the state of the B0-B35 inputs.
PGA	Port A Parity Generation	I	Parity is generated for data reads from the mail2 register when PGA is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{\text{EVEN}}$ input. Bytes are organized at A0-A8, A9-A17, A18-A26, and A27-A35. The generated parity bits are output in the most significant bit of each byte.
PGB	Port B Parity	I	Parity is generated for data reads from port B when PGB is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{\text{EVEN}}$ input. Bytes are organized as B0-B8, B9-B17, B18-B26, and B27-B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{\text{RST}}$	Reset	I	To reset the device, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{\text{RST}}$ is LOW. This sets the $\overline{\text{AF}}$, $\overline{\text{MBF1}}$, and $\overline{\text{MBF2}}$ flags HIGH and the $\overline{\text{EF}}$, $\overline{\text{AE}}$, and $\overline{\text{FF}}$ flags LOW. The LOW-to-HIGH transition of $\overline{\text{RST}}$ latches the status of the FS1 and FS0 inputs to select almost-full flag and almost-empty flag offset.
SIZ0, SIZ1	Port B Bus Size Selects	I (Port B)	A LOW-to-HIGH transition of CLKB latches the states of SIZ0, SIZ1, and $\overline{\text{BE}}$, and the following LOW-to-HIGH transition of CLKB implements the latched states as a port B bus size. Port B bus sizes can be long word, word, or byte. A HIGH on both SIZ0 and SIZ1 accesses the mailbox registers for a port B 36-bit write or read.
SW0, SW1	Port B Byte Swap Selects	I (Port B)	At the beginning of each long word FIFO read, one of four modes of byte-order swapping is selected by SW0 and SW1. The four modes are no swap, byte swap, word swap, and byte-word swap. Byte-order swapping is possible with any bus-size selection.
W/$\overline{\text{RA}}$	Port A Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the high-impedance state when W/$\overline{\text{RA}}$ is HIGH.
W/$\overline{\text{RB}}$	Port B Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the high-impedance state when W/$\overline{\text{RB}}$ is HIGH.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)(1)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	-0.5 to 7	V
V_I(2)	Input Voltage Range	-0.5 to V_{CC}+0.5	V
V_O(2)	Output Voltage Range	-0.5 to V_{CC}+0.5	V
I_{IK}	Input Clamp Current, (V_I < 0 or V_I > V_{CC})	±20	mA
I_{OK}	Output Clamp Current, (V_O < 0 or V_O > V_{CC})	±50	mA
I_{OUT}	Continuous Output Current, (V_O = 0 to V_{CC})	±50	mA
I_{CC}	Continuous Current Through V_{CC} or GND	±500	mA
T_A	Operating Free-Air Temperature Range	0 to 70	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

5

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IH}	High-Level Input Voltage	2		V
V_{IL}	Low-Level Input Voltage		0.8	V
I_{OH}	High-Level Output Current		-4	mA
I_{OL}	Low-Level Output Current		8	mA
T_A	Operating Free-Air Temperature	0	70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Parameter	Test Conditions				Min.	Typ.(1)	Max.	Unit
V_{OH}	V_{CC} = 4.5V,	I_{OH} = -4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or 0					±50	µA
I_{OZ}	V_{CC} = 5.5 V,	V_O = V_{CC} or 0					±50	µA
I_{CC}	V_{CC} = 5.5 V,	I_O = 0 mA,	V_I = V_{CC} or GND	Outputs HIGH			60	mA
				Outputs LOW			130	
				Outputs Disabled			60	
C_i	V_I = 0,	f = 1 MHz				4		pF
C_o	V_O = 0,	f = 1 MHz				8		pF

NOTE:
1. All typical values are at VCC = 5 V, TA = 25°C.

AC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE (SEE FIGURE 4 THROUGH 18)

Symbol	Parameter	IDT723613L15		IDT723613L20		IDT723613L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Clock Frequency, CLKA or CLKB	–	66.7	–	50	–	33.4	MHz
t_{CLK}	Clock Cycle Time, CLKA or CLKB	15	–	20	–	30	–	ns
t_{CLKH}	Pulse Duration, CLKA and CLKB HIGH	6	–	8	–	12	–	ns
t_{CLKL}	Pulse Duration, CLKA and CLKB LOW	6	–	8	–	12	–	ns
t_{DS}	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	4	–	5	–	6	–	ns
t_{ENS}	Setup Time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$,W/$\overline{RB}$, and ENB before CLKB↑	5	–	5	–	6	–	ns
t_{SZS}	Setup Time, SIZ0, SIZ1,and $\overline{BE}$ before CLKB↑	4	–	5	–	6	–	ns
t_{SWS}	Setup Time, SW0 and SW1 before CLKB↑	5	–	7	–	8	–	ns
t_{PGS}	Setup Time, ODD/$\overline{EVEN}$ and PGB before CLKB↑[1]	4	–	5	–	6	–	
t_{RSTS}	Setup Time, $\overline{RST}$ LOW before CLKA↑ or CLKB↑[2]	5	–	6	–	7	–	ns
t_{FSS}	Setup Time, FS0 and FS1 before $\overline{RST}$ HIGH	5	–	6	–	7	–	ns
t_{DH}	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	1	–	1	–	1	–	ns
t_{ENH}	Hold Time, $\overline{CSA}$ W/$\overline{RA}$, ENA and MBA after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, and ENB after CLKB↑	1	–	1	–	1	–	ns
t_{SZH}	Hold Time, SIZ0, SIZ1, and $\overline{BE}$ after CLKB↑	2	–	2	–	2	–	ns
t_{SWH}	Hold Time, SW0 and SW1 after CLKB↑	0	–	0	–	0	–	ns
t_{PGH}	Hold Time, ODD/$\overline{EVEN}$ and PGB after CLKB↑[1]	0	–	0	–	0	–	ns
t_{RSTH}	Hold Time, $\overline{RST}$ LOW after CLKA↑ or CLKB↑[2]	5	–	6	–	7	–	ns
t_{FSH}	Hold Time, FS0 and FS1 after $\overline{RST}$ HIGH	4	–	4	–	4	–	ns
t_{SKEW1}[3]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{EF}$ and $\overline{FF}$	8	–	8	–	10	–	ns
t_{SKEW2}[3]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{AE}$ and $\overline{AF}$	9	–	16	–	20	–	ns

NOTES:
1. Only applies for a clock edge that does a FIFO read.
2. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
3. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 30pF (SEE FIGURE 4 THROUGH 18)

Symbol	Parameter	IDT723613L15		IDT723613L20		IDT723613L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_A	Access Time, CLKA↑ to A0-A35 and CLKB↑ to B0-B35	2	10	2	12	2	15	ns
t_{WFF}	Propagation Delay Time, CLKA↑ to $\overline{FF}$	2	10	2	12	2	15	ns
t_{REF}	Propagation Delay Time, CLKB↑ to $\overline{EF}$	2	10	2	12	2	15	ns
t_{PAE}	Propagation Delay Time, CLKB↑ to $\overline{AE}$	2	10	2	12	2	15	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AF}$	2	10	2	12	2	15	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	1	9	1	12	1	15	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to B0-B35[1] and CLKB↑ to A0-A35[2]	3	11	3	12	3	15	ns
t_{PPE}[3]	Propagation delay time, CLKB↑ to $\overline{PEFB}$	2	11	2	12	2	13	ns
t_{MDV}	Propagation Delay Time, SIZ1, SIZ0 to B0-B35 valid	1	11	1	11.5	1	12	ns
t_{PDPE}	Propagation Delay Time, A0-A35 valid to $\overline{PEFA}$ valid; B0-B35 valid to $\overline{PEFB}$ valid	3	10	3	11	3	13	ns
t_{POPE}	Propagation Delay Time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	3	11	3	12	3	14	ns
t_{POPB}[4]	Propagation Delay Time, ODD/$\overline{EVEN}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	12	2	13	2	15	ns
t_{PEPE}	Propagation Delay Time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to $\overline{PEFA}$; $\overline{CSB}$, ENB, W/$\overline{RB}$, SIZ1, SIZ0, or PGB to $\overline{PEFB}$	1	11	1	12	1	14	ns
t_{PEPB}[4]	Propagation Delay Time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to parity bits (A8, A17, A26, A35); $\overline{CSB}$, ENB, W/$\overline{RB}$, SIZ1, SIZ0, or PGB to parity bits (B8, B17, B26, B35)	3	12	3	13	3	14	ns
t_{RSF}	Propagation Delay Time, $\overline{RST}$ to $\overline{AE}$, $\overline{EF}$ LOW and $\overline{AF}$, $\overline{MBF1}$, $\overline{MBF2}$ HIGH	1	15	1	20	1	25	ns
t_{EN}	Enable Time, $\overline{CSA}$ and W/$\overline{RA}$ LOW to A0-A35 active and $\overline{CSB}$ LOW and W/$\overline{RB}$ HIGH to B0-B35 active	2	10	2	12	2	14	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{RA}$ HIGH to A0-A35 at high impedance and $\overline{CSB}$ HIGH or W/$\overline{RB}$ LOW to B0-B35 at high impedance	1	8	1	9	1	11	ns

NOTES:
1. Writing data to the mail1 register when the B0-B35 outputs are active and SIZ1 and SIZ0 are HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active.
3. Only applies when a new port-B bus size is implemented by the rising CLKB edge.
4. Only applies when reading data from a mail register.

5

FUNCTIONAL DESCRIPTION

RESET (RST)

The IDT723613 is reset by taking the reset ($\overline{RST}$) input LOW for at least four port A clock (CLKA) and four port B clock (CLKB) LOW-to-HIGH transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of the FIFO and forces the full-flag ($\overline{FF}$) LOW, the empty flag ($\overline{EF}$) LOW, the almost-empty flag ($\overline{AE}$) LOW, and the almost-full flag ($\overline{AF}$) HIGH. A reset also forces the mailbox flags ($\overline{MBF1}$, $\overline{MBF2}$) HIGH. After a reset, $\overline{FF}$ is set HIGH after two LOW-to-HIGH transitions of CLKA. The device must be reset after power up before data is written to its memory.

A LOW-to-HIGH transition on the $\overline{RST}$ input loads the almost-full and almost-empty offset register (X) with the value selected by the flag select (FS0, FS1) inputs. The values that can be loaded into the register are shown in Table 1.

TABLE 1: FLAG PROGRAMMING

FS1	FS0	$\overline{RST}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FIFO WRITE/READ OPERATION

The state of the port A data (A0-A35) outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{RA}$). The A0-A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW.

Data is loaded into the FIFO from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH, MBA is LOW, and $\overline{FFA}$ is HIGH (see Table 2).

The state of the port B data (B0-B35) outputs is controlled by the port B chip select ($\overline{CSB}$) and the port B write/read select (W/$\overline{RB}$). The B0-B35 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is HIGH. The B0-B35 outputs are active when both $\overline{CSB}$ and W/$\overline{RB}$ are LOW. Data is read from the FIFO to the B0-B35 outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, W/$\overline{RB}$ is LOW, ENB is HIGH, $\overline{EFB}$ is HIGH, and either SIZ0 or SIZ1 is LOW (see Table 3).

The setup and hold-time constraints to the port clocks for the port chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, W/$\overline{RB}$) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port's chip select and write/read select can change states during the setup and hold time window of the cycle.

SYNCHRONIZED FIFO FLAGS

Each FIFO flag is synchronized to its port clock through two flip-flop stages. This is done to improve the flags' reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another. $\overline{FF}$ and $\overline{AF}$ are synchronized to CLKA. $\overline{EF}$ and $\overline{AE}$ are synchronized to CLKB. Table 4 shows the relationship of each port flag to the level of FIFO fill.

TABLE 2: PORT A ENABLE FUNCTION TABLE

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0-A35 OUPTUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO write
L	H	H	H	↑	In high impedence state	Mail1 write
L	L	L	L	X	Active, mail2 register	None
L	L	H	L	↑	Active, mail2 register	None
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{MBF2}$ HIGH)

TABLE 3: PORT B ENABLE FUNCTION TABLE

$\overline{CSB}$	W/$\overline{RB}$	ENB	SIZ1, SIZ0	CLKB	B0-B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	One, both LOW	↑	In high-impedance state	None
L	H	H	Both HIGH	↑	In high-impedance state	Mail2 write
L	L	L	One, both LOW	X	Active, FIFO output regisger	None
L	L	H	One, both LOW	↑	Active, FIFO output register	FIFO read
L	L	L	Both HIGH	X	Active, mail1 register	None
L	L	H	Both HIGH	↑	Active mail1 register	Mail1 read (set $\overline{MBF1}$ HIGH)

EMPTY FLAG ($\overline{EF}$)

The FIFO empty flag is synchronized to the port clock that reads data from its array (CLKB). When the empty flag is HIGH, new data can be read to the FIFO output register. When the empty flag is LOW, the FIFO is empty and attempted FIFO reads are ignored. When reading the FIFO with a byte or word size on port B, $\overline{EF}$ is set LOW when the fourth byte or second word of the last long word is read.

The FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls the empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to the FIFO can be read to the FIFO output register in a minimum of three port B clock (CLKB) cycles. Therefore, an empty flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two CLKB cycles have not elapsed since the time the word was written. The empty flag of the FIFO is set HIGH by the second LOW-to-HIGH transition of CLKB, and the new data word can be read to the FIFO output register in the following cycle.

A LOW-to-HIGH transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 9).

TABLE 4: FIFO FLAG OPERATION

NUMBER OF 36-BIT WORDS IN THE FIFO [1]	SYNCHRONIZED TO CLKB		SYNCHRONIZED TO CLKA	
	$\overline{EF}$	$\overline{AE}$	$\overline{AF}$	$\overline{FF}$
0	L	L	H	H
1 to X	H	L	H	H
(X+ 1) to [64 - (X + 1)]	H	H	H	H
(64 - X) to 63	H	H	L	H
64	H	H	L	L

NOTE:
1. X is the value in the almost-empty flag and almost-full flag offset register

FULL FLAG ($\overline{FF}$)

The FIFO full flag is synchronized to the port clock that writes data to its array (CLKA). When the full flag is HIGH, a SRAM location is free to receive new data. No memory locations are free when the full flag is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to the FIFO, its write-pointer is incremented. The state machine that controls the full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full-1, or full-2. From the time a word is read from the FIFO, its previous memory location is ready to be written in a minimum of three CLKA cycles. Therefore, a full flag is LOW if less than two CLKA cycles have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the full flag synchronizing clock after the read sets the full flag HIGH and data can be written in the following clock cycle.

A LOW-to-HIGH transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 10).

ALMOST-EMPTY FLAG ($\overline{AE}$)

The FIFO almost empty-flag is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls the almost-empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost

empty+2. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset above). The almost-empty flag is LOW when the FIFO contains X or less long words in memory and is HIGH when the FIFO contains (X+1) or more long words.

Two LOW-to-HIGH transitions on the port B clock (CLKB) are required after a FIFO write for the almost-empty flag to reflect the new level of fill. Therefore, the almost-empty flag of a FIFO containing (X+1) or more long words remains LOW if two CLKB cycles have not elapsed since the write that filled the memory to the (X+1) level. The almost-empty flag is set HIGH by the second CLKB LOW-to-HIGH transition after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of CLKB begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) long words. Otherwise, the subsequent CLKB cycle can be the first synchronization cycle (see Figure 11).

ALMOST FULL FLAG ($\overline{AF}$)

The FIFO almost-full flag is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full-1, or almost full-2. The almost-full state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see reset above). The almost-full flag is LOW when the FIFO contains (64-X) or more long words in memory and is HIGH when the FIFO contains [64-(X+1)] or less long words.

Two LOW-to-HIGH transitions on the port A clock (CLKA) are required after a FIFO read for the almost-full flag to reflect the new level of fill. Therefore, the almost-full flag of a FIFO containing [64-(X+1)] or less words remains LOW if two CLKA cycles have not elapsed since the read that reduced the number of long words in memory to [64-(X+1)]. The almost-full flag is set HIGH by the second CLKA LOW-to-HIGH transition after the FIFO read that reduces the number of long words in memory to [64-(X+1)]. A LOW-to-HIGH transition on CLKA begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of long words in memory to [64-(X+1)]. Otherwise, the subsequent CLKA cycle can be the first synchronization cycle (see Figure 12).

MAILBOX REGISTERS

Two 36-bit bypass registers (mail1, mail2) are on the IDT723613 to pass command and control information between port A and port B without putting it in queue. A LOW-to-HIGH transition on CLKA writes A0-A35 data to the mail1 register when a port A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA (with MBA HIGH). A LOW-to-HIGH transition on CLKB writes B0-B35 data to the mail2 register when a port B write is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB (and both SIZ0 and SIZ1 are HIGH). Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while its mail flag is LOW.

When the port B data (B0-B35) outputs are active, the data on the bus comes from the FIFO output register when either one or both SIZ1 and SIZ0 are LOW and from the mail1 register when both SIZ1 and SIZ0 are HIGH. The mail1 register flag ($\overline{MBF1}$) is set HIGH by a rising CLKB edge when a port B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB, (and both SIZ1 and SIZ0 HIGH). The mail2 register flag ($\overline{MBF2}$) is set HIGH by a rising CLKA edge when a port A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA (with MBA HIGH). The data in a mail register remains intact after it is read and changes only when new data is written to the register.

DYNAMIC BUS SIZING

The port B bus can be configured in a 36-bit long word, 18-bit word, or 9-bit byte format for data read from the FIFO. Word- and byte-size bus selections can utilize the most significant bytes of the bus (big endian) or least significant bytes of the bus (little endian). Port B bus-size can be changed dynamically and synchronous to CLKB to communicate with peripherals of various bus widths.

The levels applied to the port B bus-size select (SIZ0, SIZ1) inputs and the big-endian select ($\overline{BE}$) input are stored on each CLKB LOW-to-HIGH transition. The stored port B bus-size selection is implemented by the next rising edge on CLKB according to Figure 1.

Only 36-bit long-word data is written to or read from the FIFO memory on the IDT723613. Bus-matching operations are done after data is read from the FIFO RAM. Port B bus sizing does not apply to mail register operations.

BUS-MATCHING FIFO READS

Data is read from the FIFO RAM in 36-bit long-word increments. If a long-word bus-size is implemented, the entire long word immediately shifts to the FIFO output register upon a read. If byte or word size is implemented on port B, only the first one or two bytes appear on the selected portion of the FIFO output register, with the rest of the long word stored in auxiliary registers. In this case, subsequent FIFO reads with the same bus-size implementation output the rest of the long word to the FIFO output register in the order shown by Figure 1.

Each FIFO read with a new bus-size implementation automatically unloads data from the FIFO RAM to its output register and auxiliary registers. Therefore, implementing a new port B bus-size and performing a FIFO read before all bytes or words stored in the auxiliary registers have been read results in a loss of the unread data in these registers.

When reading data from FIFO in byte or word format, the unused B0-B35 outputs remain inactive but static, with the unused FIFO output register bits holding the last data value to decrease power consumption.

BYTE SWAPPING

The byte-order arrangement of data read from the FIFO can be changed synchronous to the rising edge of CLKB. Byte-order swapping is not available for mail register data. Four modes of byte-order swapping (including no swap) can be done with any data port size selection. The order of the bytes are rearranged within the long word, but the bit order within the bytes remaines constant.

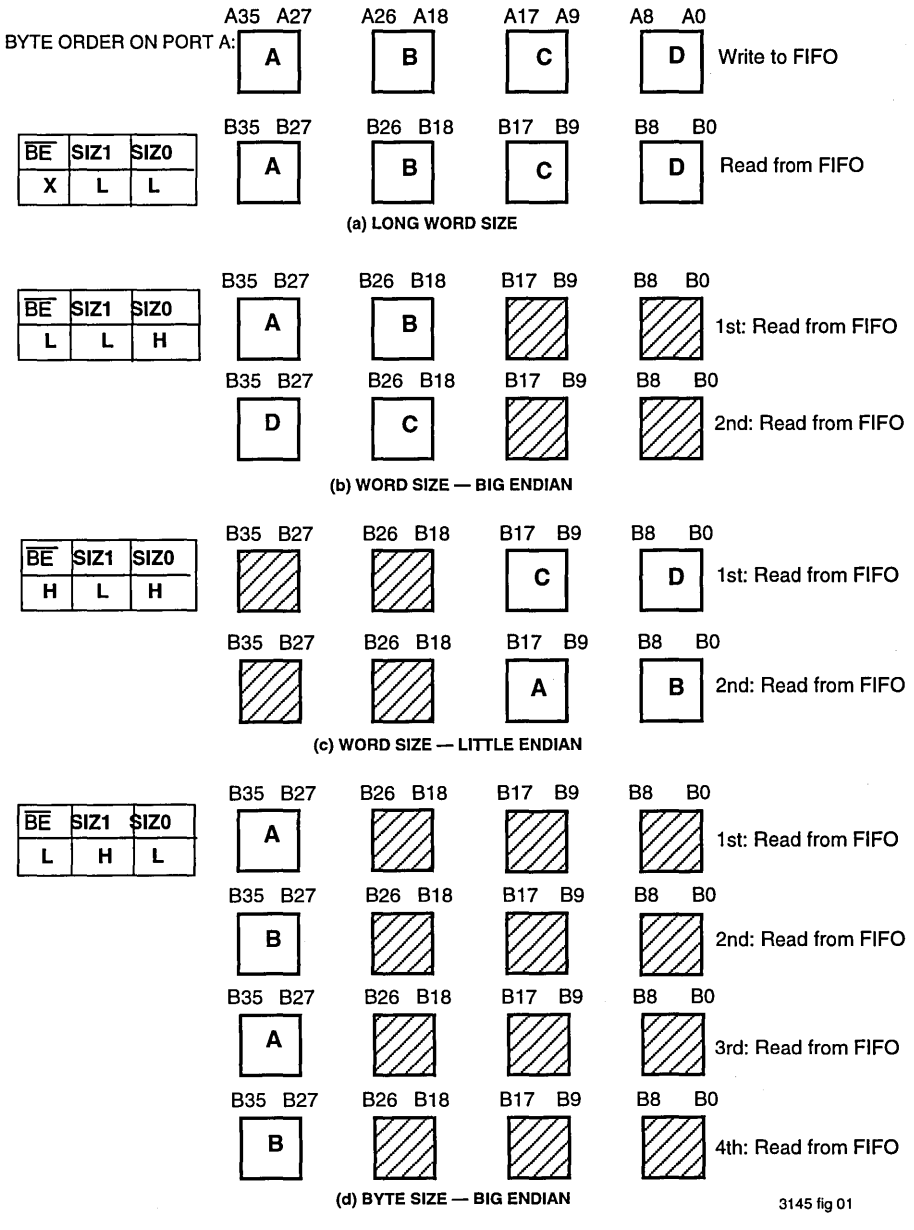


Figure 1. Dynamic Bus Sizing

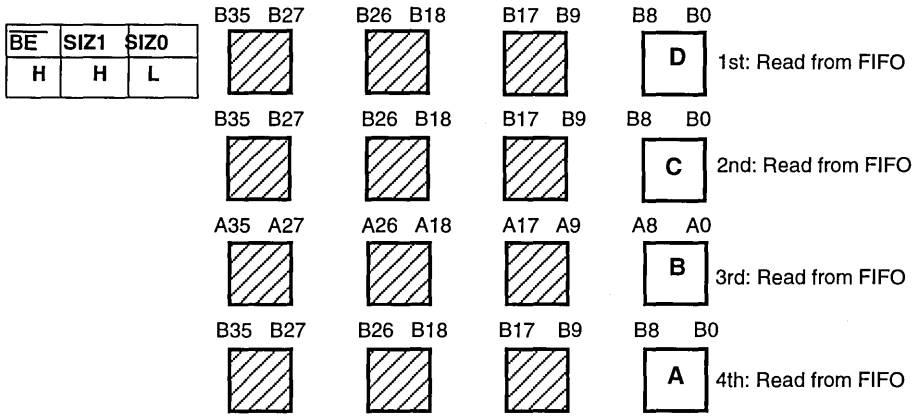


Figure 1. Dynamic Bus Sizing (continued)

Byte arrangement is chosen by the port B swap select (SW0, SW1) inputs on a CLKB rising edge that reads a new long word from the FIFO. The byte order chosen on the first byte or first word of a new long word read from the FIFO is maintained until the entire long word is transferred, regardless of the SW0 and SW1 states during subsequent reads. Figure 3 is an example of the byte-order swapping available for long word reads. Performing a byte swap and bus-size simulationeously for a FIFO read first rearranges the bytes as shown in Figure 3, then outputs the bytes as shown in Figure 1.

PORT-B MAIL REGISTER ACCESS

In addition to selecting port B bus sizes for FIFO reads, the port B bus size select (SIZ0, SIZ1) inputs also access the mail registers. When both SIZ0 and SIZ1 are HIGH, the mail1 register is accessed for a port B long-word read and the mail2 register is accessed for a port B long-word write. The mail register is accessed immediately and any bus-sizing operation that can be underway is unaffected by the mail register access. After the mail register access is complete, the previous FIFO access can resume in the next

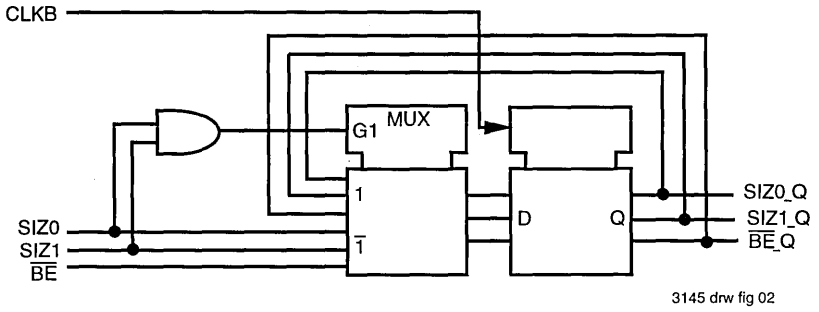


Figure 2. Logic Diagram for SIZ0, SIZ1, and BE Register

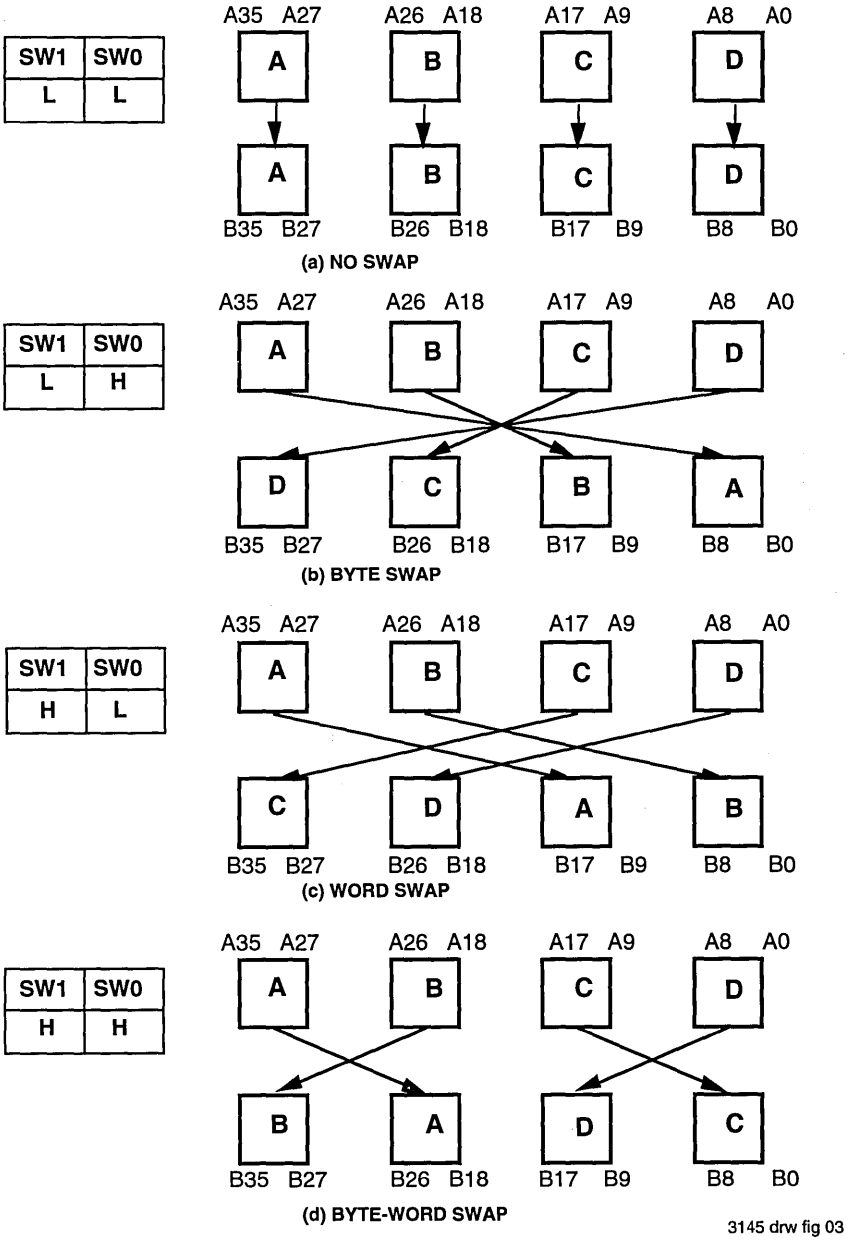


Figure 3. Byte Swapping for FIFO Reads (Long-Word Size Example)

CLKB cycle. The logic diagram in Figure 2 shows the previous bus-size selection is preserved when the mail registers are accessed from port B. A port B bus-size is implemented on each rising CLKB edge according to the states of SIZ0_Q, SIZ1_Q, and $\overline{BE}$_Q.

PARITY CHECKING

The port A data inputs (A0-A35) and port B data inputs (B0-B35) each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the port A data bus is reported by a low level on the port A parity error flag ($\overline{PEFA}$). A parity failure on one or more bytes of the port B data inputs that are valid for the bus-size implementation is reported by a low level on the port B parity error flag ($\overline{PEFB}$). Odd or even parity checking can be selected, and the parity error flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/$\overline{EVEN}$) select input. A parity error on one or more valid bytes of a port is reported by a LOW level on the corresponding port-parity-error flag ($\overline{PEFA}$, $\overline{PEFB}$) output. Port A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35, and port B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, and its valid bytes are those used in a port B bus size implementation. When odd/even parity is selected, a port-parity-error flag ($\overline{PEFA}$, $\overline{PEFB}$) is LOW if any byte on the port has an odd/even number of LOW levels applied to its bits.

The four parity trees used to check the A0-A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = HIGH). When a port A read from the mail2 register with parity generation is selected with $\overline{CSA}$ LOW, ENA HIGH, W/$\overline{RA}$ LOW, MBA HIGH, and PGA HIGH, the port A parity error flag ($\overline{PEFA}$) is held HIGH regardless of the levels applied to the A0-A35 inputs. Likewise, the parity trees used to check the B0-B35 inputs are shared by the mail1 register when parity generation is selected for port B reads (PGB = HIGH). When a port B read from the mail1 register with parity generation is selected with $\overline{CSB}$ LOW, ENB HIGH, W/$\overline{RB}$ LOW, both SIZ0 and SIZ1 HIGH, and PGB HIGH, the port B parity error flag ($\overline{PEFB}$) is held HIGH regardless of the levels applied to the B0-B35 inputs.

PARITY GENERATION

A HIGH level on the port A parity generate select (PGA) or port B generate select (PGB) enables the IDT723613 to generate parity bits for port reads from a FIFO or mailbox register. Port A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte used as the parity bit. Port B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all nine inputs of a byte regardless of the state of the parity generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{EVEN}$ select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port A parity generate select (PGA) and odd/even parity select (ODD/$\overline{EVEN}$) have setup and hold time constraints to the port A clock (CLKA) and the port B parity generate select (PGB) and ODD/$\overline{EVEN}$ select have setup and hold time constraints to the port B clock (CLKB). These timing constraints only apply for a rising clock edge used to read a new long word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port B bus (B0-B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port A bus (A0-A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port chip select ($\overline{CSA}$, $\overline{CSB}$) is LOW, enable (ENA, ENB) is HIGH, and write/read select (W/$\overline{RA}$, W/$\overline{RB}$) input is LOW, the mail register is selected (MBA HIGH for port A; both SIZ0 and SIZ1 are HIGH for port B), and port parity generate select (PGA, PGB) is HIGH. Generating parity for mail register data does not change the contents of the register.

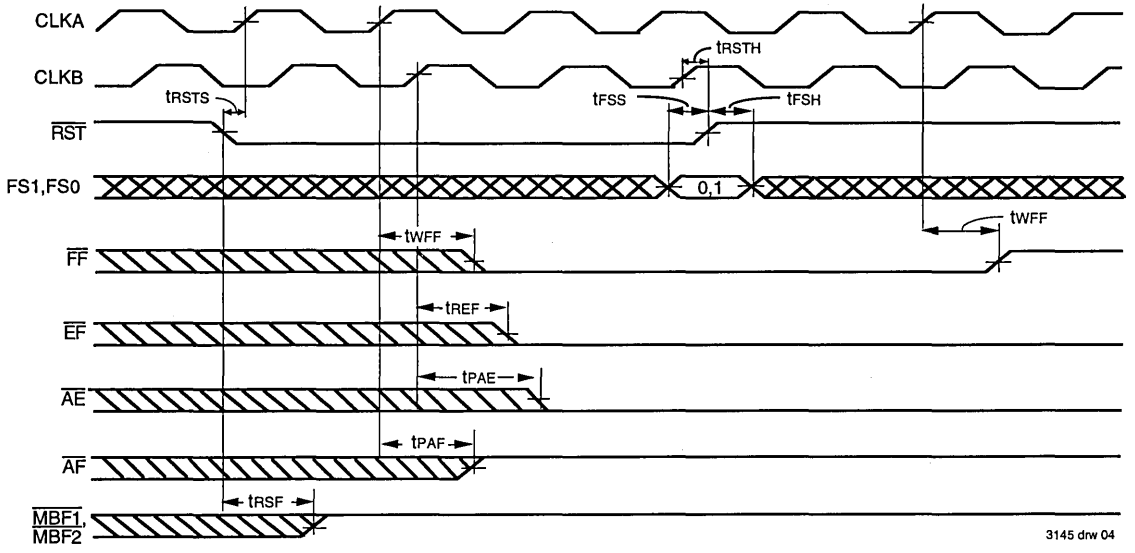
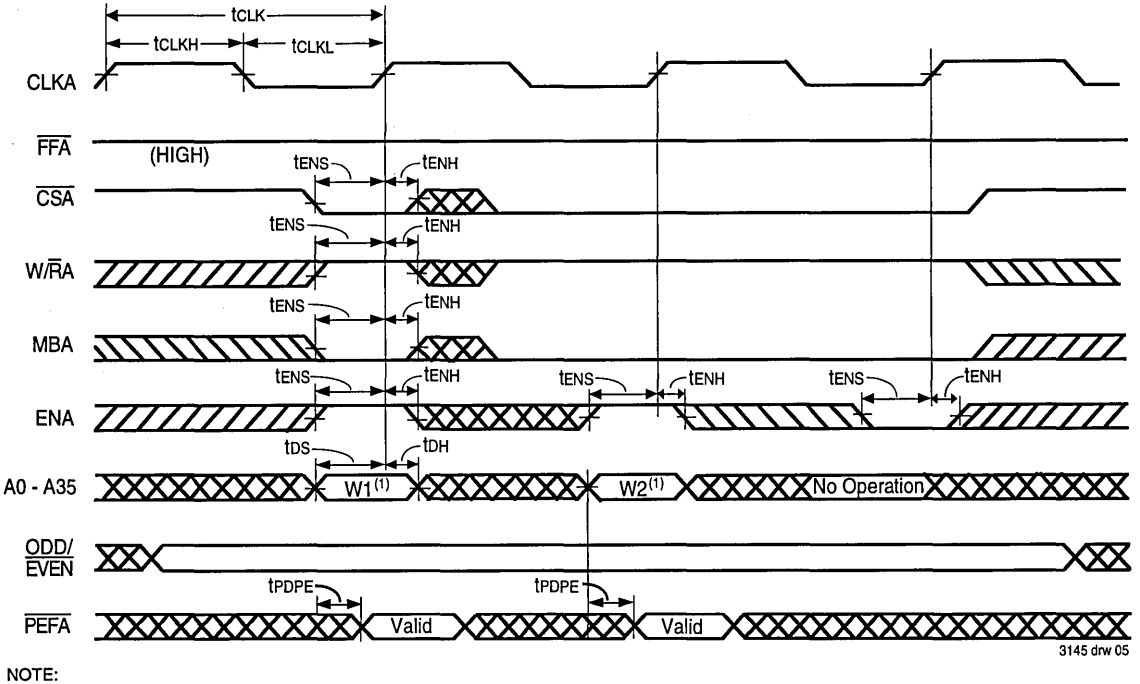


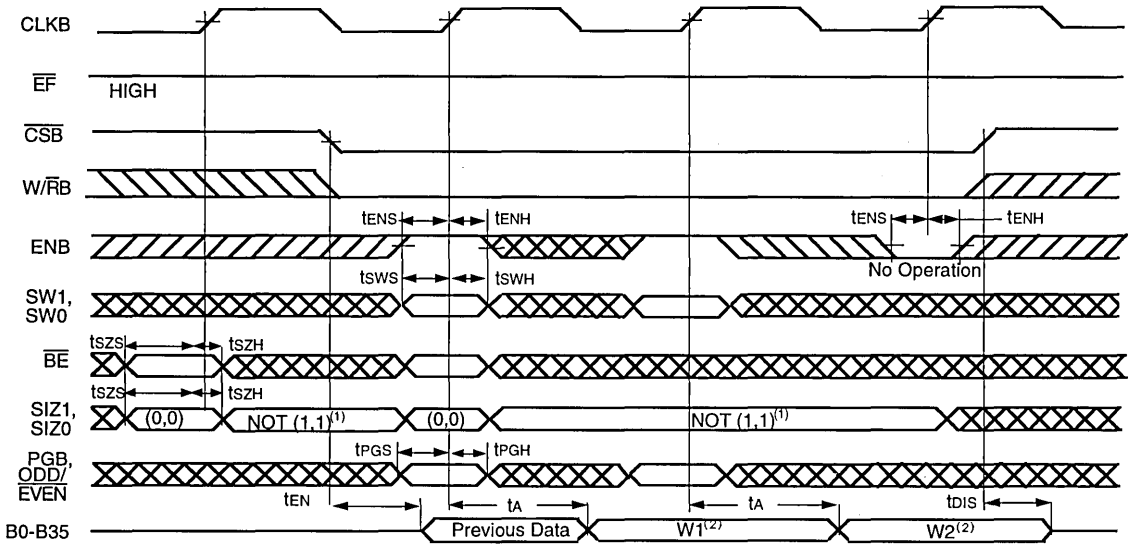
Figure 4. Device Reset Loading the X Register with the Value of Eight

5



NOTE:
1. Written to the FIFO.

Figure 5. FIFO Write Cycle Timing



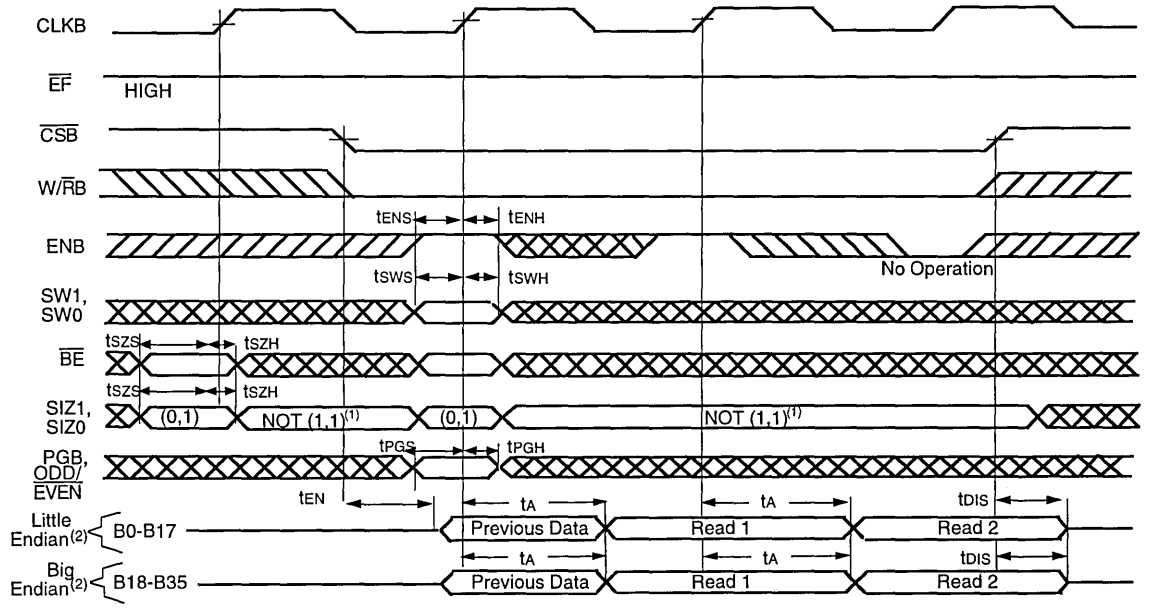
3146 drw 06

NOTES:
1. SIZ0 = HIGH and SIZ1 = HIGH selects the mail1 register for output on B0-B35.
2. Data read from FIFO1.

DATA SWAP TABLE FOR FIFO LONG-WORD READS

FIFO DATA WRITE				SWAP MODE		FIFO DATA READ			
A35-A27	A26-A18	A17-A9	A8-A0	SW1	SW0	B35-B27	B26-B18	B17-B9	B8-B0
A	B	C	D	L	L	A	B	C	D
A	B	C	D	L	H	D	C	B	A
A	B	C	D	H	L	C	D	A	B
A	B	C	D	H	H	B	A	D	C

Figure 6. FIFO Long-Word Read Cycle Timing



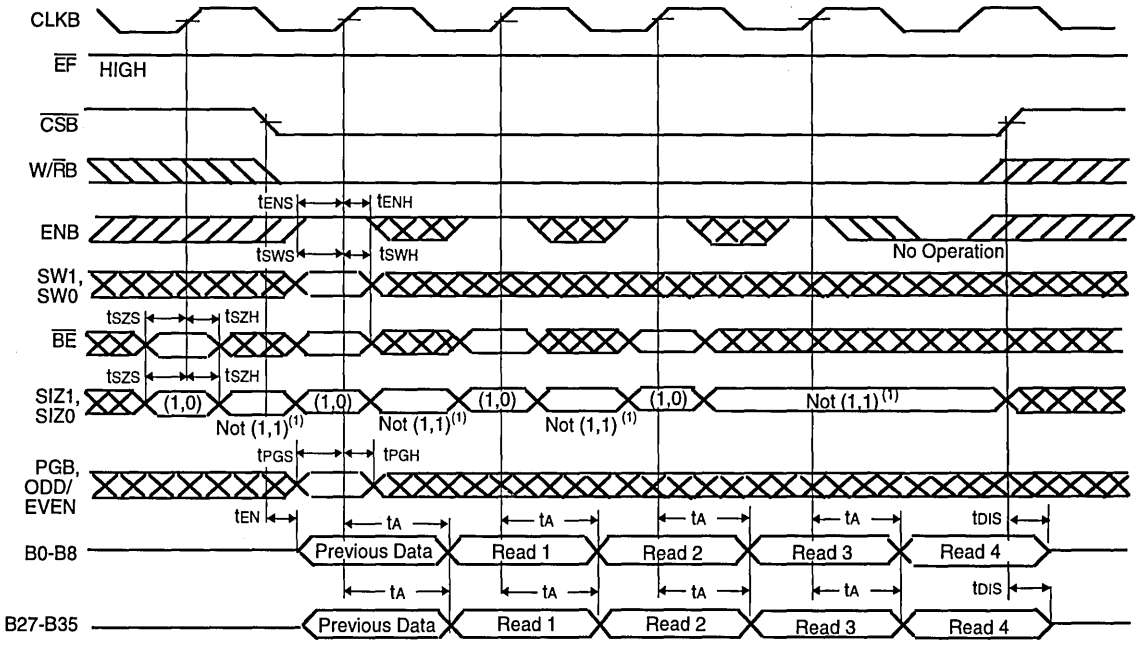
3145 drw 07

NOTES;
1. SIZ0 = HIGH and SIZ1 = HIGH selects the mail1 register for output on B0-B35.
2. Unused word B0-B17 or B18-B35 holds last FIFO1 output register data for word-size reads.

DATA SWAP TABLE FOR FIFO WORD READS

FIFO DATA WRITE				SWAP MODE		READ NO.	FIFO DATA READ			
							BIG ENDIAN		LITTLE ENDIAN	
A35-A27	A26-A18	A17-A9	A8-A0	SW1	SW0		B35-B27	B26-B18	B17-B9	B8-B0
						1	A	B	C	D
A	B	C	D	L	L	2	C	D	A	B
						1	D	C	B	A
A	B	C	D	L	H	2	B	A	D	C
						1	C	D	A	B
A	B	C	D	H	L	2	A	B	C	D
						1	B	A	D	C
A	B	C	D	H	H	2	D	C	B	A

Figure 7. FIFO Word Read-Cycle Timing



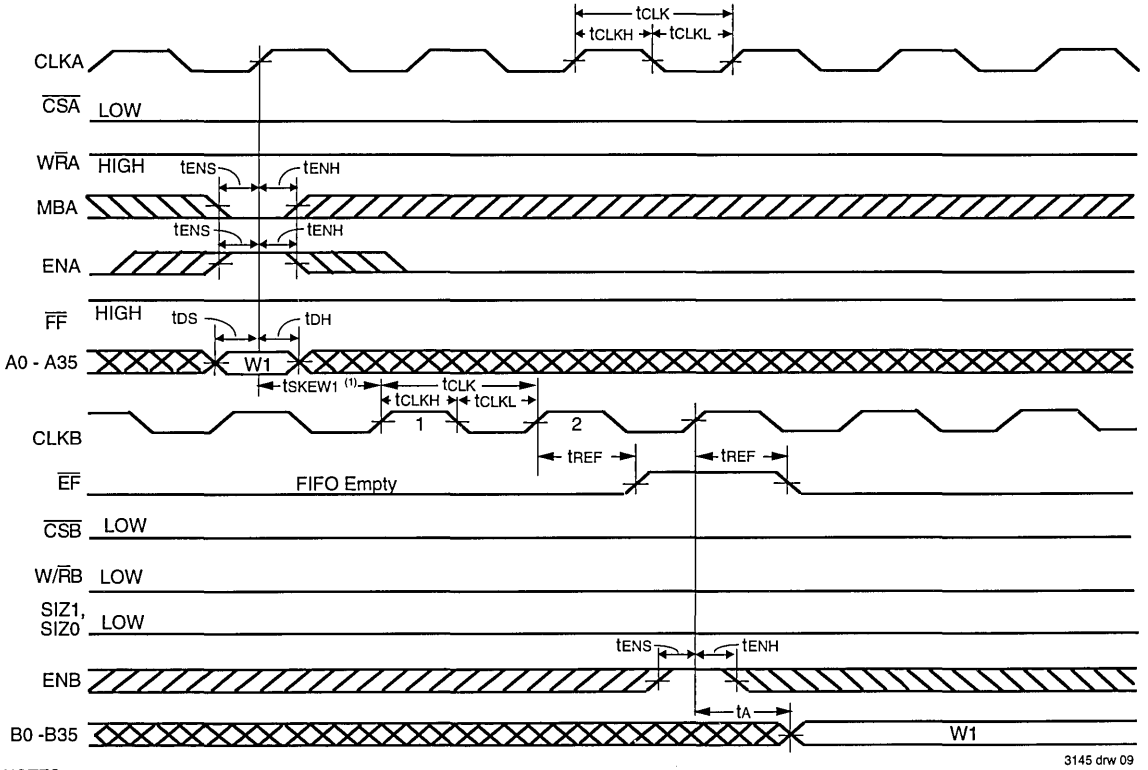
NOTES:
1. SIZ0 = HIGH and SIZ1 = HIGH selects the mail1 register for output on B0-B35.
2. Unused bytes hold last FIFO output register data for byte-size reads.

3145 drw 08

DATA SWAP TABLE FOR FIFO BYTE READS

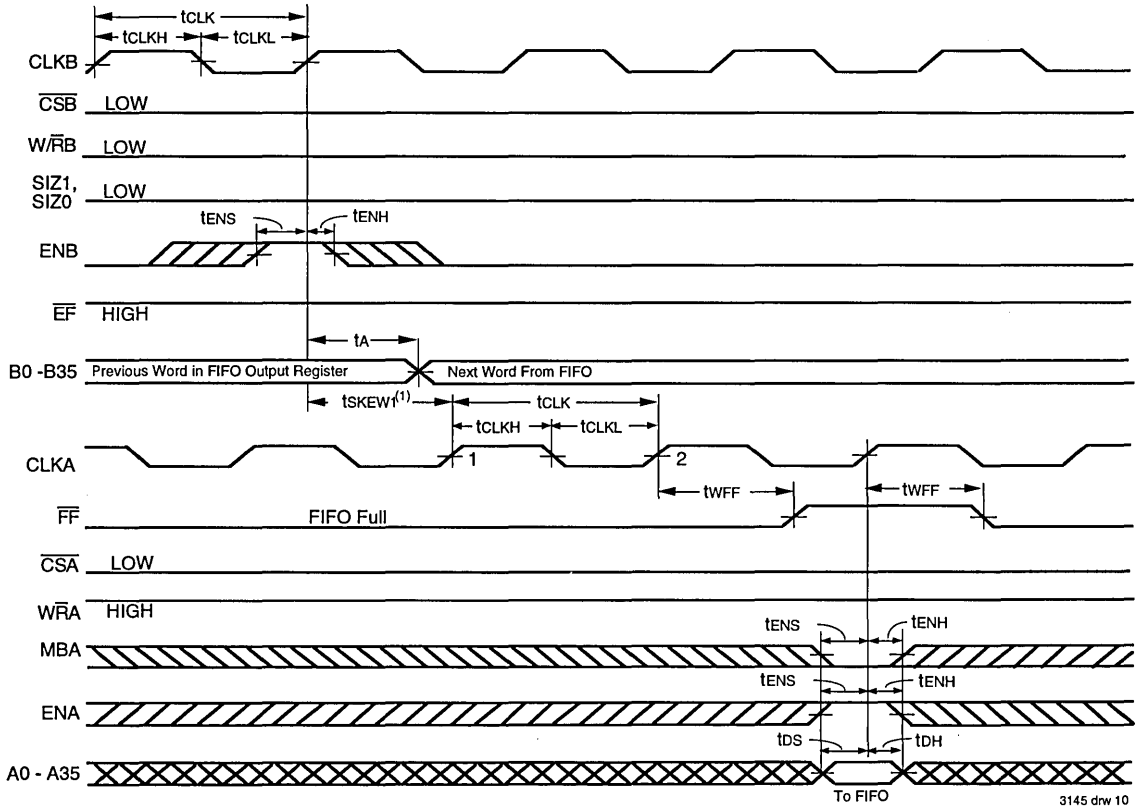
FIFO DATA WRITE				SWAP MODE		READ NO.	FIFO DATA READ	
							BIG ENDIAN	LITTLE ENDIAN
A35-A27	A26-A18	A17-A9	A8-A0	SW1	SW0		B35-B27	B8-B0
A	B	C	D	L	L	1 2 3 4	A B C D	D C B A
A	B	C	D	L	H	1 2 3 4	D C B A	A B C D
A	B	C	D	H	L	1 2 3 4	C D A B	B A D C
A	B	C	D	H	H	1 2 3 4	B A D C	C D A B

Figure 8. FIFO Byte Read-Cycle Timing



NOTES:
1. tSKEW1 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EF}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW1, then the transition of $\overline{EF}$ HIGH may occur one CLKB cycle later than shown.
2. Port B size of long word is selected for the FIFO read by SIZ1 = LOW, SIZ0 = LOW. If port-B size is word or byte, $\overline{EF}$ is set LOW by the last word or byte read from the FIFO, respectively.

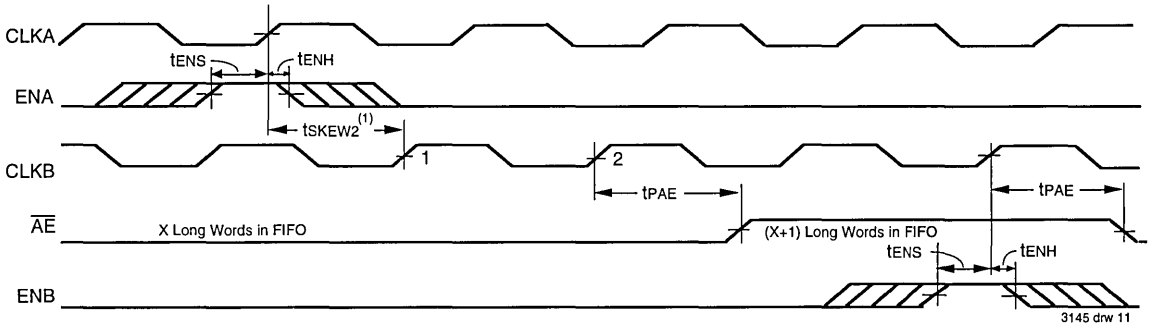
Figure 9. EF Flag Timing and First Data Read when the FIFO is Empty



NOTES:

1. tSKEW1 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{EF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW1, then the transition of $\overline{EF}$ HIGH may occur one CLKA cycle later than shown.
2. Port B size of long word is selected for the FIFO read by SIZ1 = LOW, SIZ0 = LOW. If port B size is word or byte, tSKEW1 is referenced from the rising CLKB edge that reads the first word or byte of the long word, respectively.

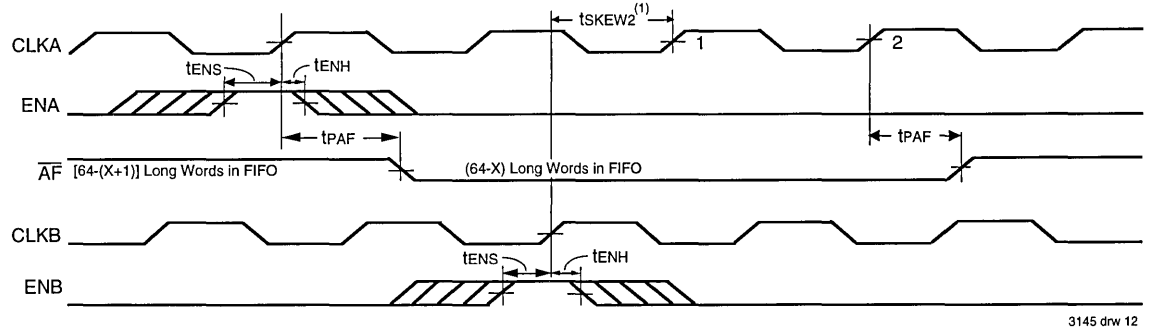
Figure 10. FF Flag Timing and First Available Write when the FIFO is Full



NOTES:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AE}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then AE may transition HIGH one CLKB cycle later than shown.
2. FIFO write ($\overline{CSA}$ = LOW, W/RA = HIGH, MBA = LOW), FIFO read ($\overline{CSB}$ = LOW, W/RB = LOW, MBB = LOW).
3. Port B size of long word is selected for the FIFO read by SIZ1 = LOW, SIZ0 = LOW. If port B size is word or byte, tSKEW2 is referenced to the first word or byte of the long word, respectively.

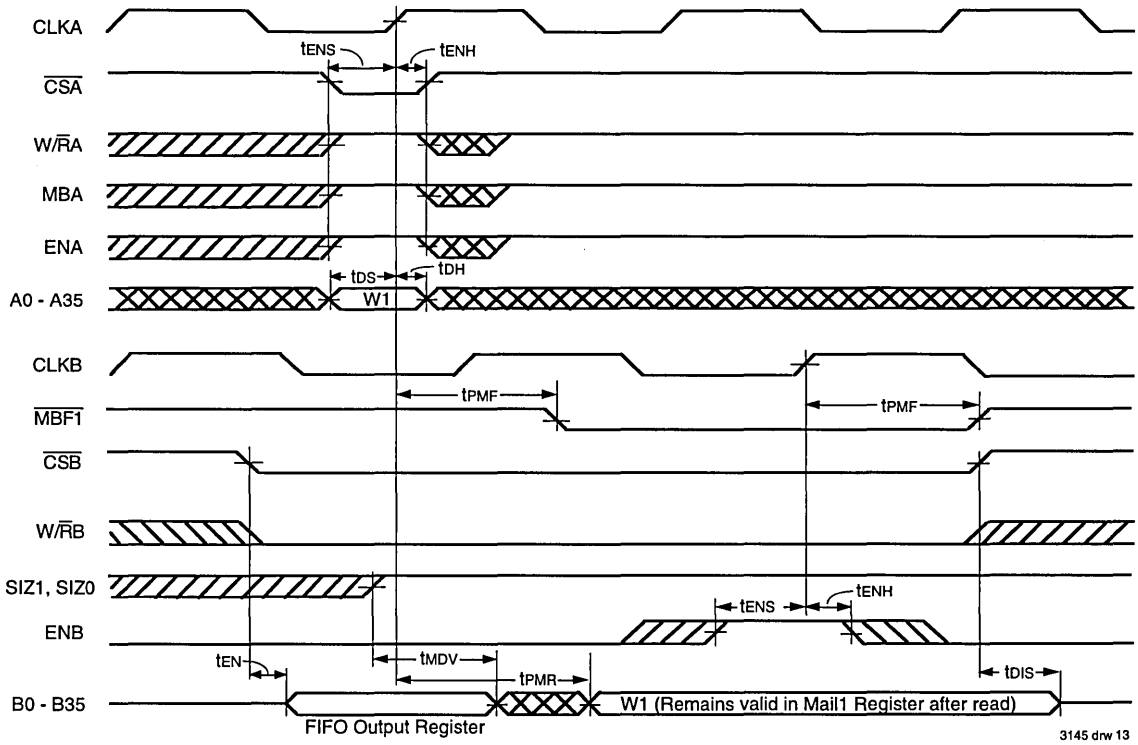
Figure 11. Timing for $\overline{AE}$ when the FIFO is Almost Empty

5



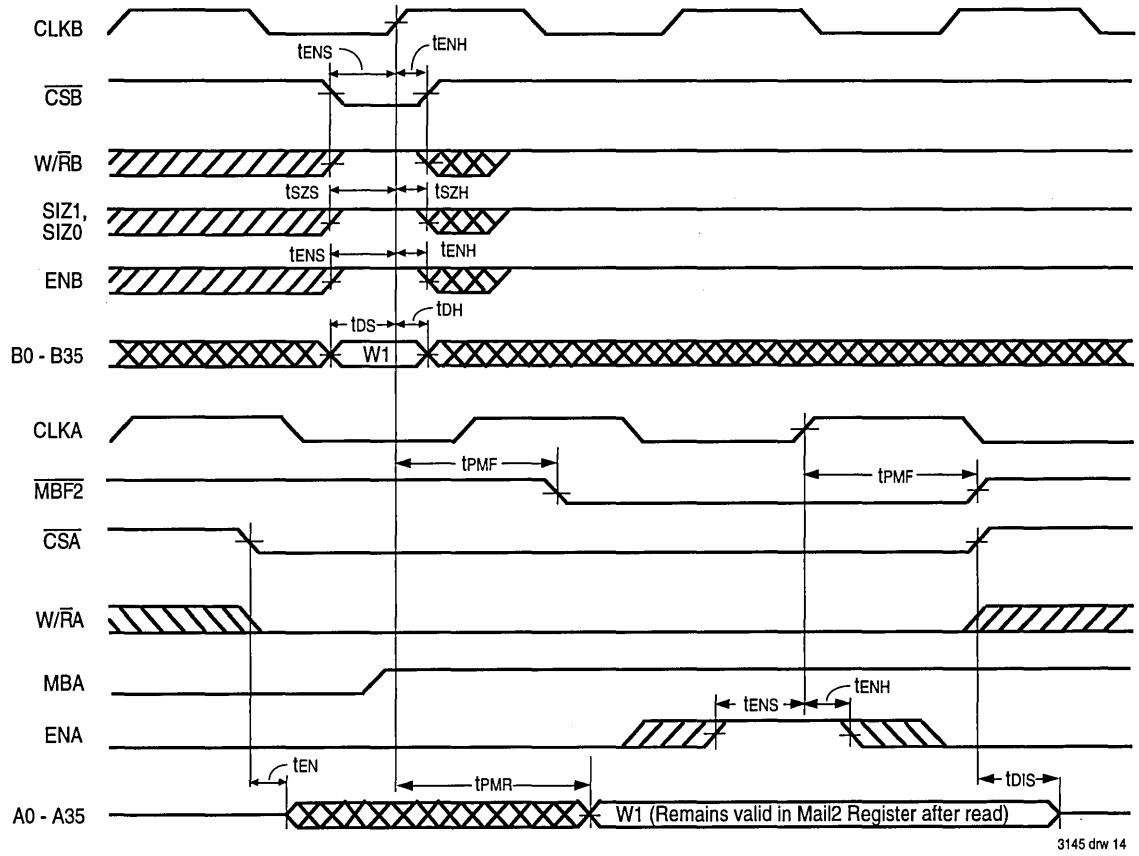
NOTES:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then $\overline{AF}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO read ($\overline{CSB}$ = LOW, $\overline{W}$/RB = LOW, MBB = LOW).
3. Port-B size of long word is selected for FIFO read by SIZ1 = LOW, SIZ0 = LOW. If port B size is word or byte, tSKEW2 is referenced from the first word or byte read of the long word, respectively.

Figure 12. Timing for $\overline{AF}$ when the FIFO is Almost Full



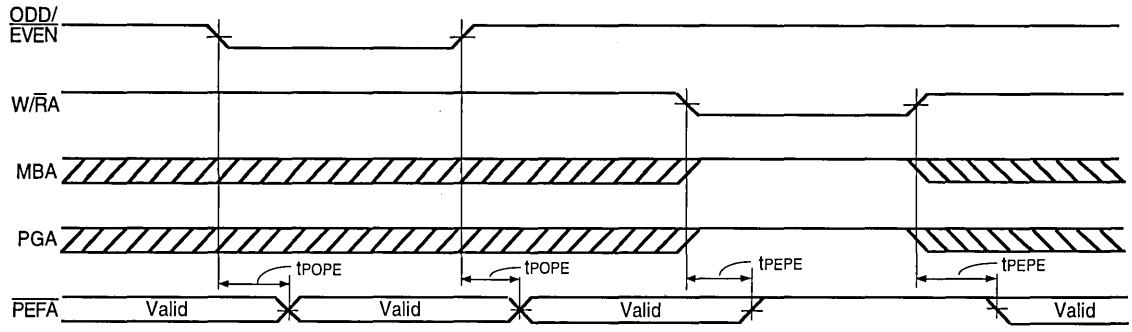
NOTE:
1. Port-B parity generation off (PGB = LOW).

Figure 13. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag



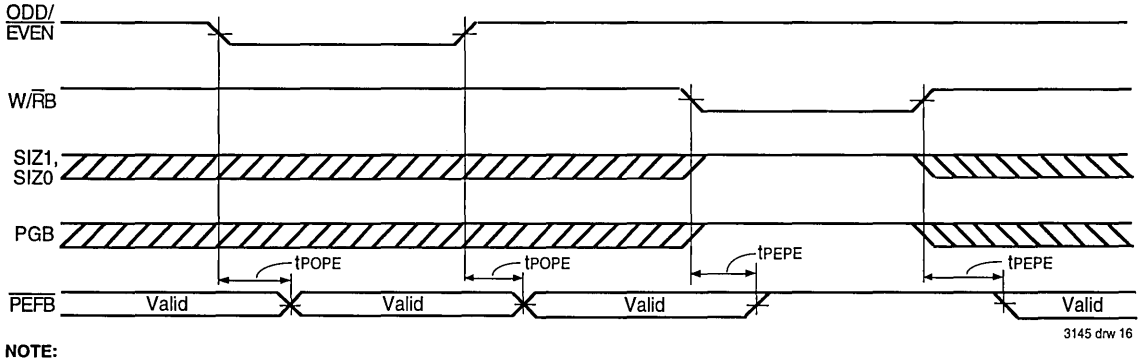
NOTE:
1. Port-A parity generation off (PGA = LOW).

Figure 14. Timing for Mail2 Register and $\overline{MBF2}$ Flag



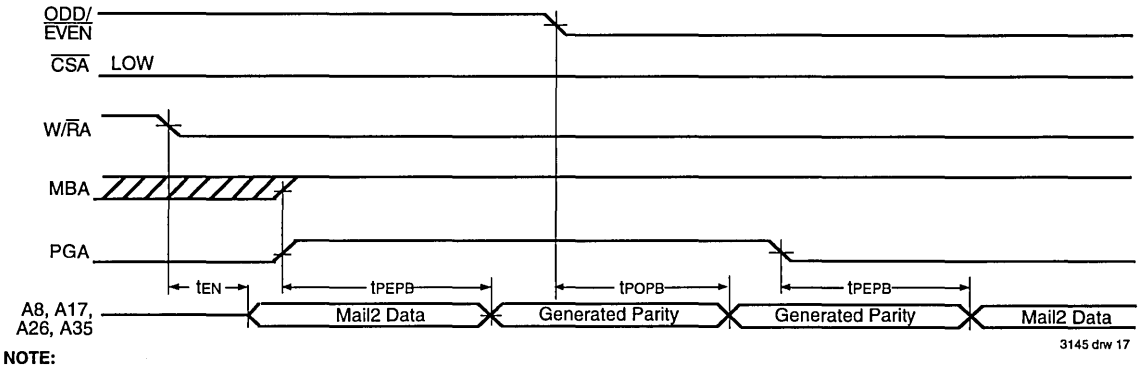
NOTE:
1. $\overline{CSA}$ = LOW and ENA = HIGH.

Figure 15. ODD/$\overline{EVEN}$, W/$\overline{RA}$, MBA, and PGA to $\overline{PEFA}$ Timing



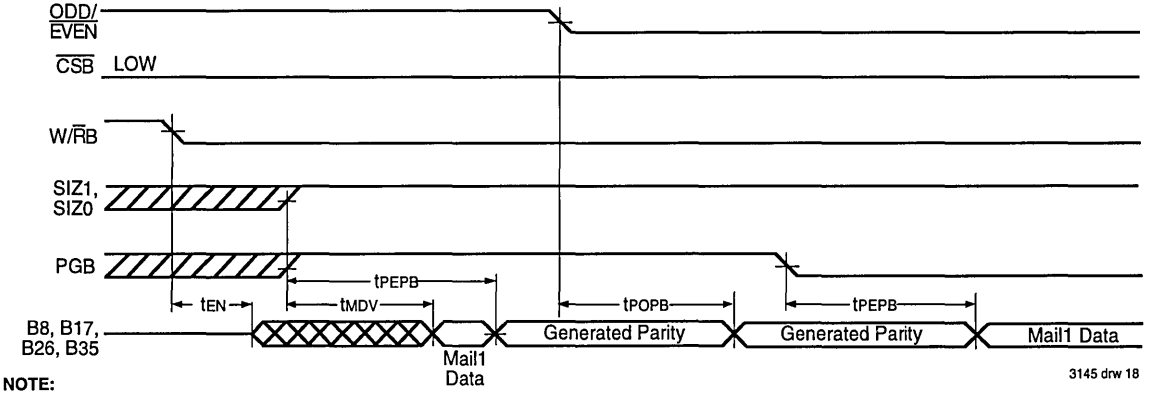
NOTE:
1. $\overline{CSB}$ = LOW and ENB = HIGH.

Figure 16. ODD/$\overline{EVEN}$, W/$\overline{RB}$, SIZ1, SIZ0, and PGB to $\overline{PEFB}$ Timing



NOTE:
1. ENA = HIGH.

Figure 17. Parity Generation Timing when Reading from the Mail2 Register



NOTE:
1. ENB = HIGH.

Figure 18. Parity Generation Timing when Reading from the Mail1 Register

5

TYPICAL CHARACTERISTICS

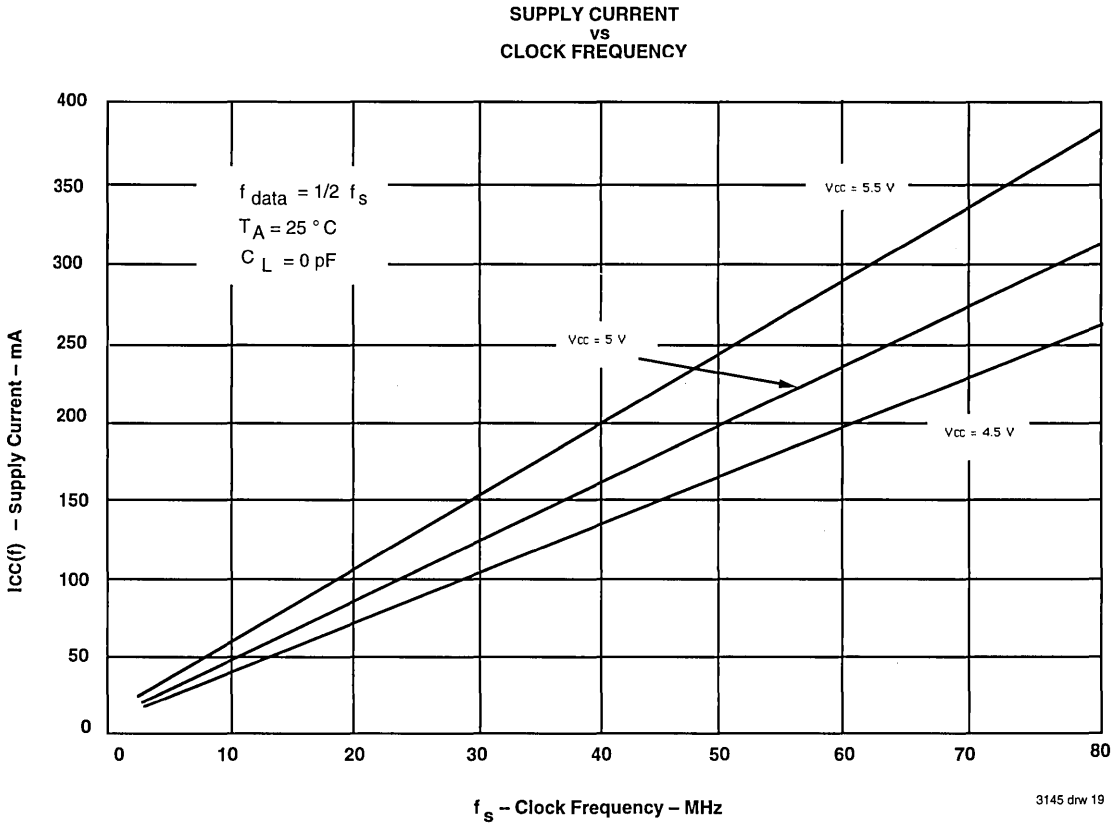


FIGURE 19

CALCULATING POWER DISSIPATION

The ICC_f current for the graph in Figure 19 was taken while simultaneously reading and writing the FIFO on the IDT723613 with CLKA and CLKB set to f_s. All date inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-copacitance load. Once the capacitive lead per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 19, the maximum power dissipation (P_T) of the IDT723613 may be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma[C_L \times (V_{OH} - V_{OL})^2 \times f_o)$$

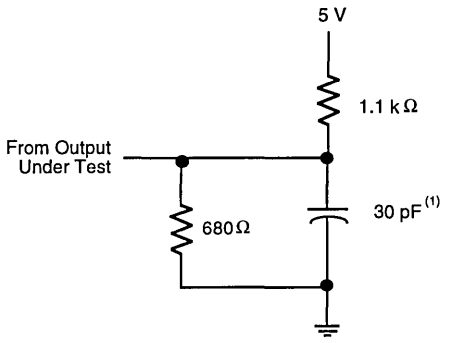
where:

C_L	=	output capacitive load
f_o	=	switching frequency of an output
V_{OH}	=	output high-level voltage
V_{OL}	=	output high-level voltage

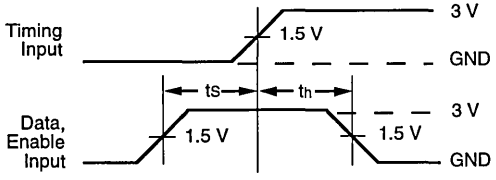
When no reads or writes are occurring on the IDT723613, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_s is calculated by:

$P_T = VCC \times f_s \times 0.29ma/MHz$

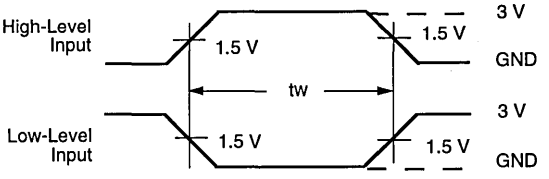
PARAMETER MEASUREMENT INFORMATION



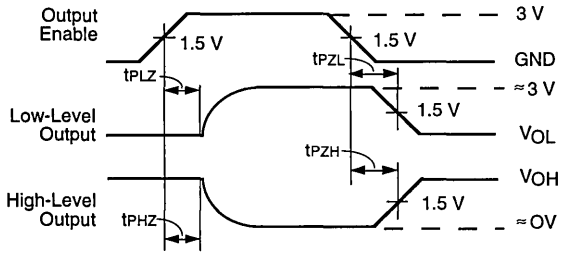
PROPAGATION DELAY
LOAD CIRCUIT



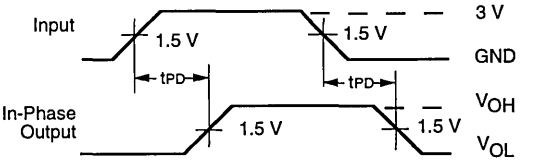
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



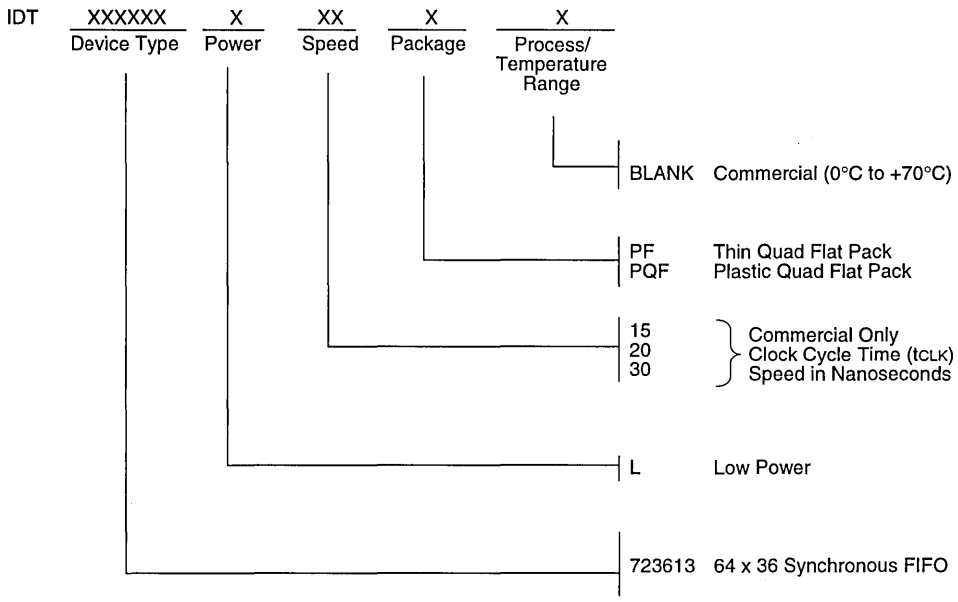
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

3145 drw 20

NOTE:
1. Includes probe and jig capacitance.

Figure 20. Load Circuit and Voltage Waveforms

ORDERING INFORMATION



3145 drw 21

Integrated Device Technology, Inc.

CMOS SyncFIFO™ 512 x 36, 1024 x 36, 2048 x 36

IDT723631
IDT723641
IDT723651

Advance information for the IDT723631
Final information for the IDT723641
Advance information for the IDT723651

FEATURES:

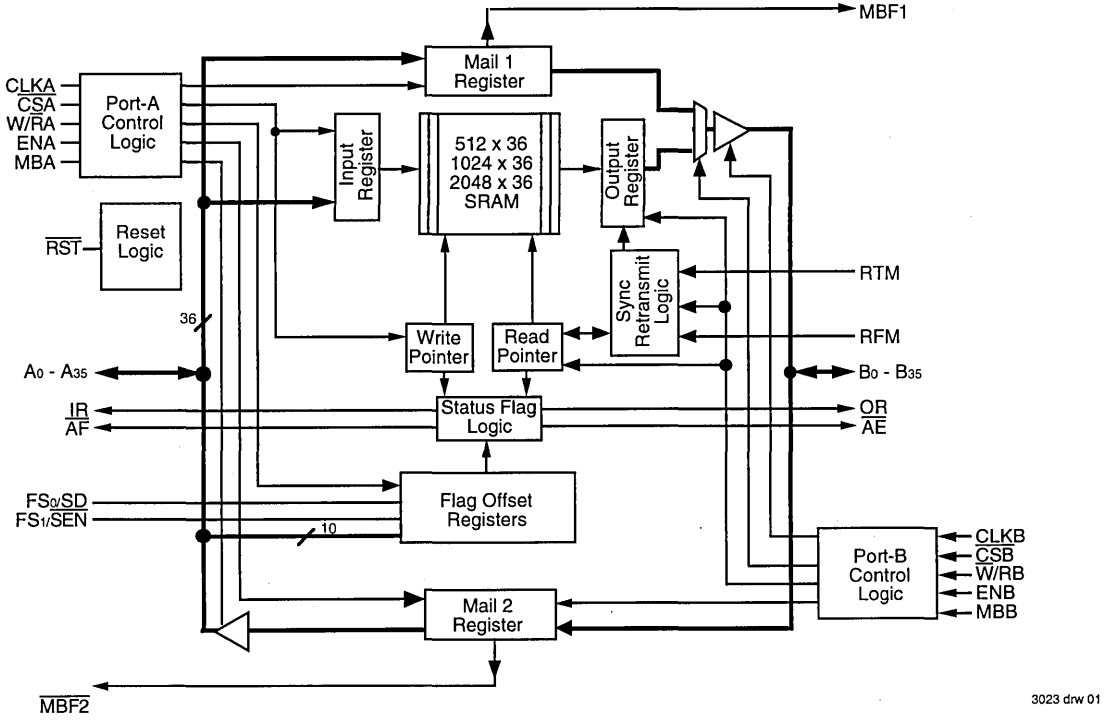
- Free-running CLKA and CLKB can be asynchronous or coincident (permits simultaneous reading and writing of data on a single clock edge)
- Clocked FIFO buffering data from Port A to Port B
- Storage capacity: IDT723631 - 512 x 36
  IDT723641 - 1024 x 36
  IDT723651 - 2048 x 36
- Synchronous read retransmit capability
- Mailbox register in each direction
- Programmable Almost-Full and Almost-Empty flags
- Microprocessor interface control logic
- Input-Ready (IR) and Almost-Full ($\overline{AF}$) flags synchronized by CLKA
- Output-Ready (OR) and Almost-Empty ($\overline{AE}$) flags synchronized by CLKB
- Low-power 0.8-micron advanced CMOS technology
- Supports clock frequencies up to 67 Mhz
- Fast access times of 11 ns
- Available in 132-pin plastic quad flat package (PQF) or space-saving 120-pin thin quad flat package (TQFP)

DESCRIPTION:

The IDT723631/723641/723651 is a monolithic high-speed, low-power, CMOS clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 12ns. The 512/1024/2048 x 36 dual-port SRAM FIFO buffers data from port A to Port B. The FIFO memory has retransmit capability, which allows previously read data to be accessed again. The FIFO has flags to indicate empty and full conditions and two programmable flags (almost full and al-

5

FUNCTIONAL BLOCK DIAGRAM



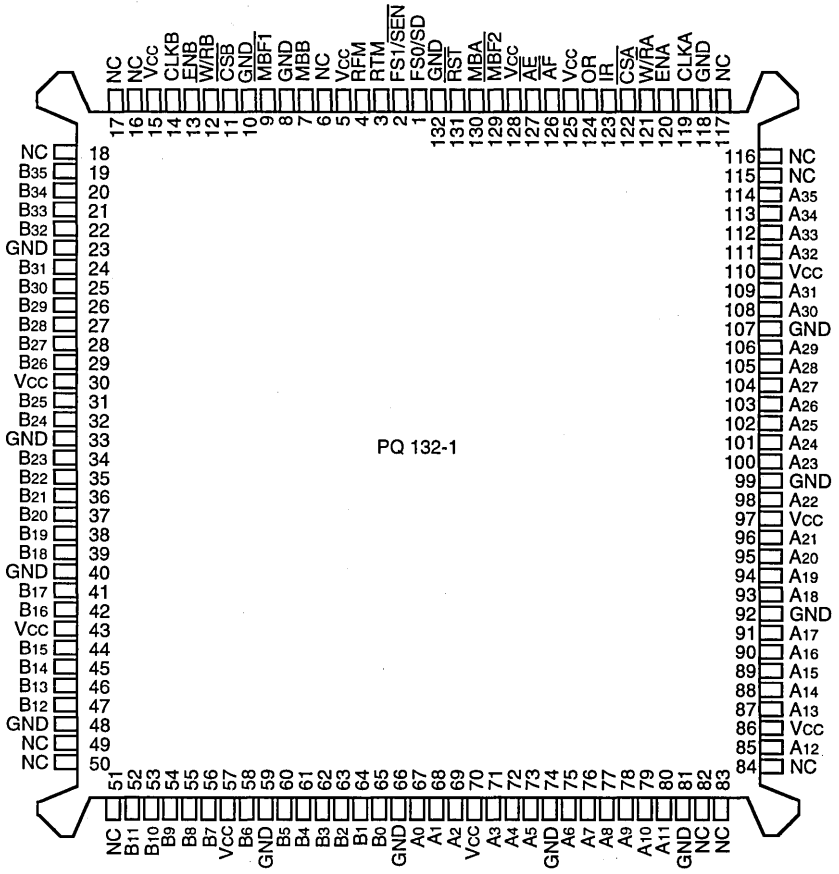
DESCRIPTION (CONTINUED)

most empty) to indicate when a selected number of words is stored in memory. Communication between each port may take place with two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices may be used in parallel to create wider data paths. Expansion is also possible in word depth.

The IDT723631/723641/723651 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple interface between microprocessors and/or buses with synchronous control.

The input-ready (IR) flag and almost-full ($\overline{AF}$) flag of the FIFO are two-stage synchronized to CLKA. The output-ready (OR) flag and almost-empty ($\overline{AE}$) flag of the FIFO are two-stage synchronized to CLKB. Offset values for the almost-full and almost empty flags of the FIFO can be programmed from port A or through a serial input.

PIN CONFIGURATION

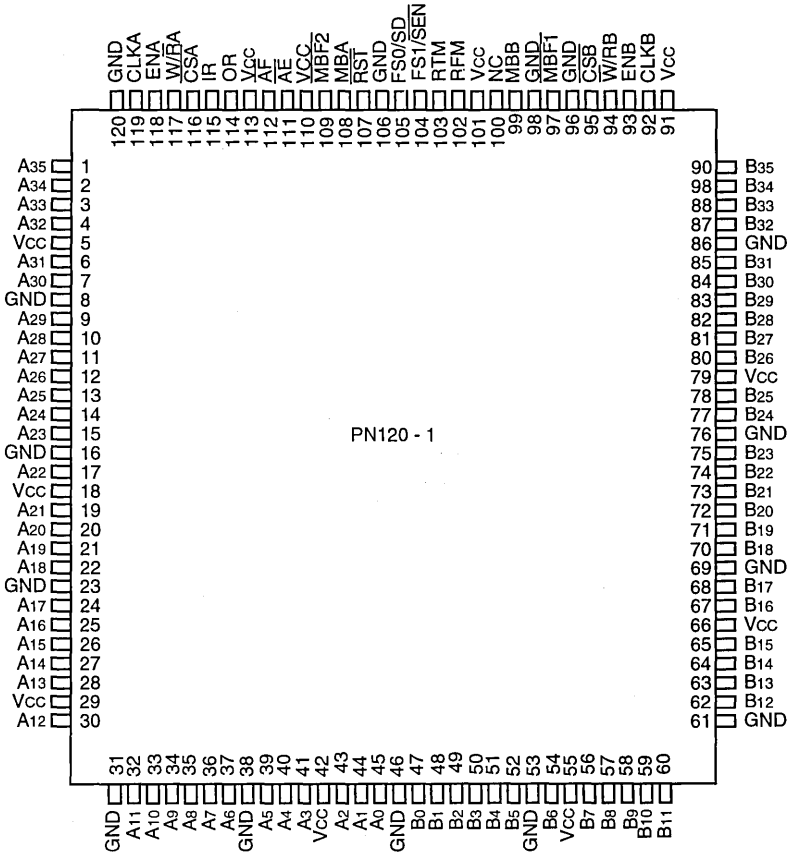


3023 drw 02

Notes:
1. NC – No internal connection
2. Uses Yamaichi socket IC51-1324-828

PQF PACKAGE
TOP VIEW

PIN CONFIGURATION (CONTINUED)



3023 drw 02a

Note:
1. NC – No internal connection

TQFP
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
A0-A35	Port-A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AE}$	Almost-Empty Flag	O	Programmable flag synchronized to CLKB. It is LOW when the number of words in the FIFO is less than or equal to the value in the almost-empty register (X).
$\overline{AF}$	Almost-Full Flag.	O	Programmable flag synchronized to CLKA. It is LOW when the number of empty locations in the FIFO is less than or equal to the value in the almost-full offset register (Y).
B0-B35	Port-B Data.	I/O	36-bit bidirectional data port for side B.
CLKA	Port-A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port-A and may be aynchronous or coincident to CLKB. IR and $\overline{AF}$ are synchronous to the LOW-to-HIGH transition of CLKA.
CLKB	Port-B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through port-B and may be asynchronous or coincident to CLKA. OR and $\overline{AE}$ are synchro nous to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port-A Chip Select	I	$\overline{CSA}$ must be LOW to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port-B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
ENA	Port-A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A.
ENB	Port-B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B.
FS1/$\overline{SEN}$, FS0/SD	Flag-Offset Select 1/ Serial Enable, Flag Offset 0/ Serial Data	I	FS1/$\overline{SEN}$ and FS0/SD are dual-purpose inputs used for flag offset register programming. During a device reset, FS1/$\overline{SEN}$ and FS0/SD selects the flag offset programming method. Three offset register programming methods are available: automatically load one of two preset values, parallel load from port A, and serial load. When serial load is selected for flag offset register programming, FS1/$\overline{SEN}$ is used as an enable synchronous to the LOW-to-HIGH transition of CLKA. When FS1/$\overline{SEN}$ is LOW, a rising edge on CLKA load the bit present on FS0/SD into the X and Y registers. The number of bit writes required to program the offset registers is 18/20/22. The first bit write stores the Y-register MSB and the last bit write stores the X-register LSB.
IR	Input-Ready Flag	O	IR is synchronized to the LOW-to-HIGH transition of CLKA. When IR is LOW, the FIFO is full and writes to its array are disabled. When the FIFO is in retransmit mode, IR indicates when the memory has been filled to the point of the retransmit data and prevents further writes. IR is set LOW during reset and is set HIGH after reset.
MBA	Port-A Mailbox Select	I	A HIGH level chooses a mailbox register for a port-A read or write operation.
MBB	Port-B Mailbox Select	I	A HIGH level chooses a mailbox register for a port-B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register for output and a LOW level selects FIFO data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by the LOW-to-HIGH transition of CLKA that writes data to the mail1 register. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a port-B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH by a reset.

3023 tbl 01

PIN DESCRIPTION (CONTINUED)

Symbol	Name	I/O	Description
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by the LOW-to-HIGH transition of CLKB that writes data to the mail2 register. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a port-A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH by a reset.
OR	Output-Ready Flag	O	OR is synchronized to the LOW-to-HIGH transition of CLKB. When OR is LOW, the FIFO is empty and reads are disabled. Ready data is present in the output register of the FIFO when OR is HIGH. OR is forced LOW during the reset and goes HIGH on the third LOW-to-HIGH transition of CLKB after a word is loaded to empty memory.
RFM	Read From Mark	I	When the FIFO is in retransmit mode, a HIGH on RFM enables a LOW-to-HIGH transition of CLKB to reset the read pointer to the beginning retransmit location and output the first selected retransmit data.
$\overline{RST}$	Reset	I	To reset the device, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST}$ is LOW. The LOW-to-HIGH transition of $\overline{RST}$ latches the status of FS0 and FS1 for $\overline{AF}$ and $\overline{AE}$ offset selection.
RTM	Retransmit Mode	I	When RTM is HIGH and valid data is present in the FIFO output register (OR is HIGH), a LOW-to-HIGH transition of CLKB selects the data for the beginning of a retransmit and puts the FIFO in retransmit mode. The selected word remains the initial retransmit point until a LOW-to-HIGH transition of CLKB occurs while RTM is LOW, taking the FIFO out of retransmit mode.
W/$\overline{RA}$	Port-A Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the high-impedance state when W/$\overline{RA}$ is HIGH.
$\overline{W}$/RB	Port-B Write/Read Select	I	A LOW selects a write operation and a HIGH selects a read operation on port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the high-impedance state when $\overline{W}$/RB is HIGH.

3023 tbl 02

5

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)(2)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	-0.5 to 7	V
V_I(2)	Input Voltage Range	-0.5 to Vcc+0.5	V
V_O(2)	Output Voltage Range	-0.5 to Vcc+0.5	V
I_{IK}	Input Clamp Current, (V_I < 0 or V_I > Vcc)	±20	mA
I_{OK}	Output Clamp Current, (V_O = < 0 or V_O > Vcc)	±50	mA
I_{OUT}	Continuous Output Current, (V_O = 0 to Vcc)	±50	mA
I_{CC}	Continuous Current Through Vcc or GND	±400	mA
T_A	Operating Free Air Temperature Range	0 to 70	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C

3023 tbl 03

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply Voltage	4.5	5.5	V
VIH	HIGH Level Input Voltage	2	–	V
VIL	LOW-Level Input Voltage	–	0.8	V
IOH	HIGH-Level Output Current	–	-4	mA
IOL	LOW-Level Output Current	–	8	mA
TA	Operating Free-air Temperature	0	70	°C

3023 tbl 04

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Parameter	Test Conditions				Min.	Typ.(1)	Max.	Unit
V_{OH}	V_{CC} = 4.5V,	I_{OH} = -4 mA			2.4			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.5	V
I_{LI}	V_{CC} = 5.5 V,	V_I = Vcc or 0					±5	µA
I_{LO}	V_{CC} = 5.5 V,	V_O = Vcc or 0					±5	µA
I_{CC}	V_{CC} = 5.5 V,	V_I = Vcc -0.2 V or 0					400	µA
ΔI_{CC}(2)	V_{CC} = 5.5 V,	One Input at 3.4 V,	$\overline{CSA}$ = V_{IH}	A0-A35		0		mA
	Other Inputs at Vcc or GND		$\overline{CSB}$ = V_{IH}	B0-B35		0		
			$\overline{CSA}$ = V_{IL}	A0-A35			1	
			$\overline{CSB}$ = V_{IL}	B0-35			1	
			All Other Inputs				1	
C_{IN}	V_I = 0,	f = 1 MHz				4		pF
C_{OUT}	V_O = 0,	f = 1 MHZ				8		pF

3023 tbl 05

NOTES:
1. All typical values are at VCC = 5 V, TA = 25°C.
2. This is the supply current when each input is at least one of the specified TTL voltage levels rather than 0 V or VCC.

DC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

Symbol	Parameter	IDT723631L15 IDT723641L15 IDT723651L15		IDT723631L20 IDT723641L20 IDT723651L20		IDT723631L30 IDT723641L30 IDT723651L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fS	Clock Frequency, CLKA or CLKB	–	66.7	–	50	–	33.4	MHz
tCLK	Clock Cycle Time, CLKA or CLKB	15	–	20	–	30	–	ns
tCLKH	Pulse Duration, CLKA or CLKB HIGH	6	–	8	–	12	–	ns
tCLKL	Pulse Duration, CLKA or CLKB LOW	6	–	8	–	12	–	ns
tDS	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	5	–	6	–	7	–	ns
tENS1	Setup Time, ENA to CLKA↑; ENB to CLKB↑	5	–	6	–	7	–	ns
tENS2	Setup Time, $\overline{CSA}$, W/$\overline{RA}$, and MBA to CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, and MBB to CLKB↑	7	–	7.5	–	8	–	ns
tRMS	Setup Time, RTM and RFM to CLKB↑	6	–	6.5	–	7	–	ns
tRSTS	Setup Time, $\overline{RST}$ LOW before CLKA↑ or CLKB↑[1]	5	–	6	–	7	–	ns
tFSS	Setup Time, FS0 and FS1 before $\overline{RST}$ HIGH	9	–	10	–	11	–	ns
tSDS[2]	Setup Time, FS0/SD before CLKA↑	5	–	6	–	7	–	ns
tSENS[2]	Setup Time, FS1/$\overline{SEN}$ before CLKA↑	5	–	6	–	7	–	ns
tDH	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	0	–	0	–	0	–	ns
tENH1	Hold Time, ENA after CLKA↑; ENB after CLKB↑	0	–	0	–	0	–	ns
tENH2	Hold Time, $\overline{CSA}$, W/$\overline{RA}$, and MBA after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, and MBB after CLKB↑	0	–	0	–	0	–	ns
tRMH	Hold Time, RTM and RFM after CLKB↑	0	–	0	–	0	–	ns
tRSTH	Hold Time, $\overline{RST}$ LOW after CLKA↑ or CLKB↑[1]	5	–	6	–	7	–	ns
tFSH	Hold Time, FS0 and FS1 after $\overline{RST}$ HIGH	0	–	0	–	0	–	ns
tSPH[2]	Hold Time, FS1/$\overline{SEN}$ HIGH after $\overline{RST}$ HIGH	0	–	0	–	0	–	ns
tSDH[2]	Hold Time, FS0/SD after CLKA↑	0	–	0	–	0	–	ns
tSENH[2]	Hold Time, FS1/$\overline{SEN}$ after CLKA↑	0	–	0	–	0	–	ns
tSKEW1[3]	Skew Time, between CLKA↑ and CLKB↑ for OR and IR	9	–	11	–	13	–	ns
tSKEW2[3]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{AE}$ and $\overline{AF}$	12	–	16	–	20	–	ns

3023 tbl 06

NOTES:
1. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
2. Only applies when serial load method is used to program flag offset registers.
3. Skew time is not a timimg constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	IDT723631L15 IDT723641L15 IDT723651L15		IDT723631L20 IDT723641L20 IDT723651L20		IDT723631L30 IDT723641L30 IDT723651L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Clock Frequency, CLKA or CLKB	–	66.7	–	50	–	33.4	MHz
t_A	Access Time, CLKB↑ to B0-B35	3	11	3	13	3	15	ns
t_{PIR}	Propagation Delay Time, CLKA↑ to $\overline{IR}$	1	8	1	10	1	12	ns
t_{POR}	Propagation Delay Time, CLKB↑ to $\overline{OR}$	1	8	1	10	1	12	ns
t_{PAE}	Propagation Delay Time, CLKB↑ to $\overline{AE}$	1	8	1	10	1	12	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AF}$	1	8	1	10	1	12	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	0	8	0	10	0	12	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to B0-B35[1] and CLKB↑ to A0-A35[2]	3	13.5	3	15	3	17	ns
t_{MDV}	Propagation Delay Time, MBB to B0-B35 Valid	3	13	3	15	3	17	ns
t_{RSF}	Propagation Delay Time, $\overline{RST}$ LOW to $\overline{AE}$ LOW and $\overline{AF}$ HIGH	1	15	1	20	1	30	ns
t_{EN}	Enable Time, $\overline{CSA}$ and W/$\overline{RA}$ LOW to A0-A35 Active and $\overline{CSB}$ LOW and $\overline{W}$/RB HIGH to B0-B35 Active	2	12	2	13	2	14	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{RA}$ HIGH to A0-A35 at high impedance and $\overline{CSB}$ HIGH or $\overline{W}$/RB LOW to B0-B35 at high impedance	1	8	1	10	1	11	ns

3023 tbl 07

NOTES:
1. Writing data to the mail1 register when the B0-B35 outputs are active and MBB is HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.

SIGNAL DESCRIPTION

RESET

The IDT723631/723641/723651 is reset by taking the reset ($\overline{RST}$) input LOW for at least four port-A clock (CLKA) and four port-B (CLKB) LOW-to-HIGH transitions. The reset input may switch asynchronously to the clocks. A reset initializes the memory read and write pointers and forces the input-ready (IR) flag LOW, the output-ready (OR) flag HIGH, the almost-empty ($\overline{AE}$) flag LOW, and the almost-full ($\overline{AF}$) flag HIGH. Resetting the device also forces the mailbox flags ($\overline{MBF1}$, $\overline{MBF2}$) HIGH. After a FIFO is reset, its input-ready flag is set HIGH after at least two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory.

ALMOST-EMPTY FLAG AND ALMOST-FULL FLAG OFFSET PROGRAMMING

Two registers in the IDT723631/723641/723651 are used to hold the offset values for the almost-empty and almost full flags. The almost-empty ($\overline{AE}$) flag offset register is labeled X, and the almost-full ($\overline{AF}$) flag offset register is labeled Y. The offset register can be loaded with a value in three ways: one of two preset values are loaded into the offset registers, parallel load from port A, or serial load. The offset register programming mode is chosen by the flag select (FS1, FS0) inputs during a LOW-to-HIGH transition on the $\overline{RST}$ input (See Table 1).

PRESET VALUES

If the preset value of 8 or 64 is chosen by the FS1 and FS0 inputs at the time of a $\overline{RST}$ LOW-to-HIGH transition according to Table 1, the preset value is automatically loaded into the X and Y registers. No other device initialization is necessary to begin normal operation, and the IR flag is set HIGH after two LOW-to-HIGH transitions on CLKA.

PARALLEL LOAD FROM PORT A

To program the X and Y registers from port A, the device is reset with FS0 and FS1 LOW during the LOW-to-HIGH transition of $\overline{RST}$. After this reset is complete, the IR flag is set HIGH after two LOW-to-HIGH transitions on CLKA. The first two writes to the FIFO do not store data in its memory but load the offset registers in the order Y, X. Each offset register of the IDT723631, IDT723641, and IDT723651 uses port-A inputs (A8-A0), (A9-A0), and (A10-A0), respectively. The highest number input is used as the most significant bit of the binary number in each case. Each register value can be programmed from 1 to 508 (IDT723631), 1 to 1020 (IDT723641), and 1 to 2044 (IDT723651). After both offset registers are programmed from port A, subsequent FIFO writes store data in the SRAM.

SERIAL LOAD

To program the X and Y registers serially, the device is reset with FS0/SD and FS1/$\overline{SEN}$ HIGH during the LOW-to-HIGH transition of $\overline{RST}$. After this reset is complete, the X and Y register values are loaded bitwise through the FS0/SD input on each LOW-to-HIGH transition of CLKA that the FS1/$\overline{SEN}$ input is LOW. Eighteen-, 20-, or 22-bit writes are needed to complete the programming for the IDT723631, IDT723641, or IDT723651, repsectively. The first-bit write stores the most significant bit of the Y register, and the last-bit write stores the least significant bit of the X register. Each register value can be programmed from 1 to 508 (IDT723631), 1 to 1020 (IDT723641), or 1 to 2044 (IDT723651).

When the option to program the offset registers serially is chosen, the input-ready (IR) flag remains LOW until all register bits are written. The IR flag is set HIGH by the LOW-to-HIGH transition of CLKA after the last bit is loaded to allow normal FIFO operation.

FIFO WRITE/READ OPERATION

The state of the port-A data (A0-A35) outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{RA}$). The A0-A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW.

Data is loaded into the FIFO from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ and the port-A mailbox select (MBA) are LOW, W/$\overline{RA}$, the port-A enable (ENA), and the input-ready (IR) flag are HIGH (see Table 2). Writes to the FIFO are independent of any concurrent FIFO read.

The port-B control signals are identical to those of port-A with the exception that the port-B write/read select ($\overline{W}$/RB) is the inverse of the port-A write/read select (W/$\overline{RA}$). The state of the port-B data (B0-B35) outputs is controlled by the port-B chip select ($\overline{CSB}$) and the port-B write/read select ($\overline{W}$/RB). The B0-B35 outputs are in the high-impedance state when either $\overline{CSB}$ is HIGH or $\overline{W}$/RB is LOW. The B0-B35 outputs are active when $\overline{CSB}$ is LOW and $\overline{W}$/RB is HIGH.

Data is read from the FIFO to its output register on a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ and the port-B mailbox select (MBB) are LOW, $\overline{W}$/RB, the port-B enable (ENB), and the output-ready (OR) flag are HIGH (see Table 3). Reads from the FIFO are independent of any concurrent FIFO writes.

The setup- and hold-time constraints to the port clocks for the port-chip selects and write/read selects are only for enabling write and read operations and are not related to high-

FS1	FS0	$\overline{RST}$	X and Y Registers (1)
H	H	↑	Serial Load
H	L	↑	64
L	H	↑	8
L	L	↑	Parallel Load From Port A

3023 tbl 08

NOTE:
1. X register holds the offset for AE; Y register holds the offset for AF.

Table 1. Flag Programming

5

impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port chip select and write/read select may change states during the setup- and hold time window of the cycle.

When the output-ready (OR) flag is LOW, the next data word is sent to the FIFO output register automatically by the CLKB LOW-to-HIGH transition that sets the output-ready flag HIGH. When OR is HIGH, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port-B chip select ($\overline{CSB}$), write/read select ($\overline{W}$/RB), enable (ENB), and mailbox select (MBB).

SYNCHRONIZED FIFO FLAGS

Each IDT723631/723641/723651 FIFO flag is synchronized to its port clock through at least two flip-flop stages. This is done to improve the flags' reliability by reducing the probability of metastable events on their outputs when CLKA and CLKB operate asynchronously to one another. OR and $\overline{AE}$ are synchronized to CLKB. IR and $\overline{AF}$ are synchronized to CLKA. Table 4 shows the relationship of each flag to the number of words stored in memory.

OUTPUT-READY FLAG (OR)

The output-ready flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). When the output-ready flag is HIGH, new data is present in the FIFO output register. When the output-ready flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an output-ready flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of CLKB. Therefore, an output-ready flag is LOW if a word in memory is the next data to be sent to the FIFO output register and three CLKB cycles have not elapsed since the time the word was written. The output-ready flag of the FIFO remains LOW until the third LOW-to-HIGH transition of CLKB occurs, simultaneously forcing the output-ready flag HIGH and shifting the word to the FIFO output register.

A LOW-to-HIGH transition on CLKB begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent CLKB cycle may be the first synchronization cycle (see Figure 6).

INPUT READY FLAG (IR)

The input ready flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). When the input-

$\overline{CSA}$	W/$\overline{R}$A	ENA	MBA	CLKA	A0-A35 Outputs	Port Functions
H	X	X	X	X	In High-Impedance State	None
L	H	L	X	X	In High-Impedance State	None
L	H	H	L	↑	In High-Impedance State	FIFO Write
L	H	H	H	↑	In High-Impedance State	Mail1 Write
L	L	L	L	X	Active, Mail2 Register	None
L	L	H	L	↑	Active, Mail2 Register	None
L	L	L	H	X	Active, Mail2 Register	None
L	L	H	H	↑	Active, Mail2 Register	Mail2 Read (Set $\overline{MBF2}$ HIGH)

3023 tbl 09

Table 2. Port-A Enable Function Table

$\overline{CSB}$	$\overline{W}$/RB	ENB	MBB	CLKB	B0-A35 Outputs	Port Functions
H	X	X	X	X	In High-Impedance State	None
L	L	L	X	X	In High-Impedance State	None
L	L	H	L	↑	In High-Impedance State	None
L	L	H	H	↑	In High-Impedance State	Mail2 Write
L	H	L	L	X	Active, FIFO Output Register	None
L	H	H	L	↑	Active, FIFO Output Register	FIFO read
L	H	L	H	X	Active, Mail1 Register	None
L	H	H	H	↑	Active, Mail1 Register	Mail1 Read (Set $\overline{MBF1}$ HIGH)

3023 tbl 10

Table 3. Port-B Enable Function Table

ready flag is HIGH, a memory location is free in the SRAM to write new data. No memory locations are free when the input-ready flag is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an input-ready flag monitors a write-pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full-1, or full-2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of three cycles of CLKA. Therefore, an input-ready flag is LOW if less than two cycles of CLKA have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on CLKA after the read sets the input-ready flag HIGH, and data can be written in the following cycle.

A LOW-to-HIGH transition on CLKA begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent CLKA cycle may be the first synchronization cycle (see Figure 7).

ALMOST-EMPTY FLAG ($\overline{AE}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls an almost-empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the contents of register X. This register is loaded with a preset value during a FIFO reset,programmed from port A, or programmed serially (see almost-empty flag and almost-full flag offset programming above). The almost-empty flag is LOW when the FIFO contains X or less words and is HIGH when the FIFO contains (X+1) or more words. A data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of CLKB are required after a FIFO write for the almost-empty flag to reflect the new level of fill; therefore, the almost-empty flag of a FIFO containing (X+1) or more words remains LOW if two cycles of CLKB have not elapsed since the write that filled the memory to the (X+1) level. An almost-empty flag is set HIGH by the second LOW-to-HIGH transition of CLKB after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of CLKB begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent CLKB cycle may be the first synchronization cycle (see Figure 8).

ALMOST-FULL FLAG ($\overline{AF}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full-1, or almost full-2. The almost-full state is defined by the contents of register Y. This register is loaded with a preset value during a FIFO reset, programmed from port A, or programmed serially (see almost-empty flag and almost-full flag offset programming). The almost-full flag is LOW when the number of words in the FIFO is greater than or equal to (512-Y), (1024-Y), OR (2048-Y) for the IDT723631, IDT723641, or IDT723651, respectively. The almost-full flag is HIGH when the number of words in the FIFO is less than or equal to [512-(Y+1)], [1024-(Y+1)], or [2048-(Y+1)] for the IDT723631, IDT723641, or IDT723651, respectively. A data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of CLKA are required after a FIFO read for its almost-full flag to reflect the new level of fill. Therefore, the almost-full flag of a FIFO containing [512/1024/2048-(Y+1)] or less words remains LOW if two cycles of CLKA have not elapsed since the read that reduced the number of words in memory to [512/1024/2048-(Y+1)]. An almost-full flag is set HIGH by the second LOW-to-HIGH transition of CLKA after the FIFO read that reduces the number of words in memory to [512/1024/2048-(Y+1)]. A LOW-to-HIGH transition of CLKA begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [512/1024/2048-(Y+1)]. Otherwise, the subsequent CLKA cycle may be the first synchronization cycle (see Figure 9).

Number of Words in the FIFO[1,2]			Synchronized to CLKB		Synchronized to CLKA	
IDT723631	IDT723641	IDT723651	OR	$\overline{AE}$	$\overline{AF}$	IR
0	0	0	L	L	H	H
1 to X	1 to X	1 to X	H	L	H	H
(X+1) to [512-(Y+1)]	(X+1) to [1024-(Y+1)]	(X+1) to [2048-(Y+1)]	H	H	H	H
(512-Y) to 511	(1024-Y) to 1023	(2048-Y) to 2047	H	H	L	H
512	1024	2048	H	H	L	L

3023 tbl 11

NOTES:
1. X is the almost-empty offset for $\overline{AE}$. Y is the almost-full offset for $\overline{AF}$.
2. When a word is present in the FIFO output register, its previous memory location is free.

Table 4. FIFO Flag Operation

SYNCHRONOUS RETRANSMIT

The synchronous retransmit feature of the IDT723631/723641/723651 allows FIFO data to be read repeatedly starting at a user-selected position. The FIFO is first put into retransmit mode to select a beginning word and prevent ongoing FIFO write operations from destroying retransmit data. Data vectors with a minimum length of three words can retransmit repeatedly starting at the selected word. The FIFO can be taken out of retransmit mode at any time and allow normal device operation.

The FIFO is put in retransmit mode by a LOW-to-HIGH transition on CLKB when the retransmit mode (RTM) input is HIGH and OR is HIGH. The rising CLKB edge marks the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a LOW-to-HIGH transition occurs while RTM is LOW.

When two or more reads have been done past the initial retransmit word, a retransmit is initiated by a LOW-to-HIGH transition on CLKB when the read-from-mark (RFM) input is HIGH. This rising CLKB edge shifts the first retransmit word to the FIFO output register and subsequent reads can begin immediately. Retransmit loops can be done endlessly while the FIFO is in retransmit mode. RFM must be LOW during the CLKB rising edge that takes the FIFO out of retransmit mode.

When the FIFO is put into retransmit mode, it operates with two read pointers. The current read pointer operates normally, incrementing each time a new word is shifted to the FIFO output register and used by the OR and $\overline{AE}$ flags. The shadow read pointer stores the SRAM location at the time the device is put into retransmit mode and does not change until the device is taken out of retransmit mode. The shadow read pointer is used by the IR and $\overline{AF}$ flags. Data writes can proceed while the FIFO is in retransmit mode, but $\overline{AF}$ is set LOW by the write that stores (512 - Y), (1024 - Y), or (2048 - Y) words after the first retransmit word for the IDT723631, IDT723641, or IDT723651, respectively. The IR flag is set LOW by the 512th, 1024th, or 2048th write after the first retransmit word for the IDT723631, IDT723641, or IDT723651, respectively.

SYNCHRONOUS TRANSMIT

When the FIFO is in retransmit mode and RFM is HIGH, a rising CLKB edge loads the current read pointer with the shadow read-pointer value and the OR flag reflect the new level of fill immediately. If the retransmit changes the FIFO status out of the almost-empty range, up to two CLKB rising edges after the retransmit cycle are needed to switch $\overline{AE}$ high (see Figure 11).The rising CLKB edge that takes the FIFO out of retransmit mode shifts the read pointer used by the IR and $\overline{AF}$ flags from the shadow to the current read pointer. If the change of read pointer used by IR and $\overline{AF}$ should cause one or both flags to transmit HIGH, at least two CLKA synchronizing cycles are needed before the flags reflect the change. A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of IR if it occurs at time t_{SKEW1} or greater after the rising CLKB edge (see Figure 12). A rising CLKA edge after the FIFO is taken out of retransmit mode is the first synchronizing cycle of $\overline{AF}$ if it occurs at time t_{SKEW2} or greater after the rising CLKB edge (see Figure 14).

MAILBOX REGISTERS

Two 36-bit bypass registers are on the IDT723631/723641/723651 to pass command and control information between port A and port B. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A LOW-to-HIGH transition on CLKA writes A0-A35 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH. A LOW-to-HIGH transition on CLKB writes B0-B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB HIGH. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while its mail flag is LOW.

When the port-B data (B0-B35) outputs are active, the data on the bus comes from the FIFO output register when the port-B mailbox select (MBB) input is LOW and from the mail1 register when MBB is HIGH. Mail2 data is always present on the port-A data (A0-A35) outputs when they are active. The mail1 register flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a port-B read is selected by $\overline{CSB}$, $\overline{W}$/RB, and ENB with MBB HIGH. The mail2 register flag (MBF2) is set HIGH by a LOW-to-HIGH transition on CLKA when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

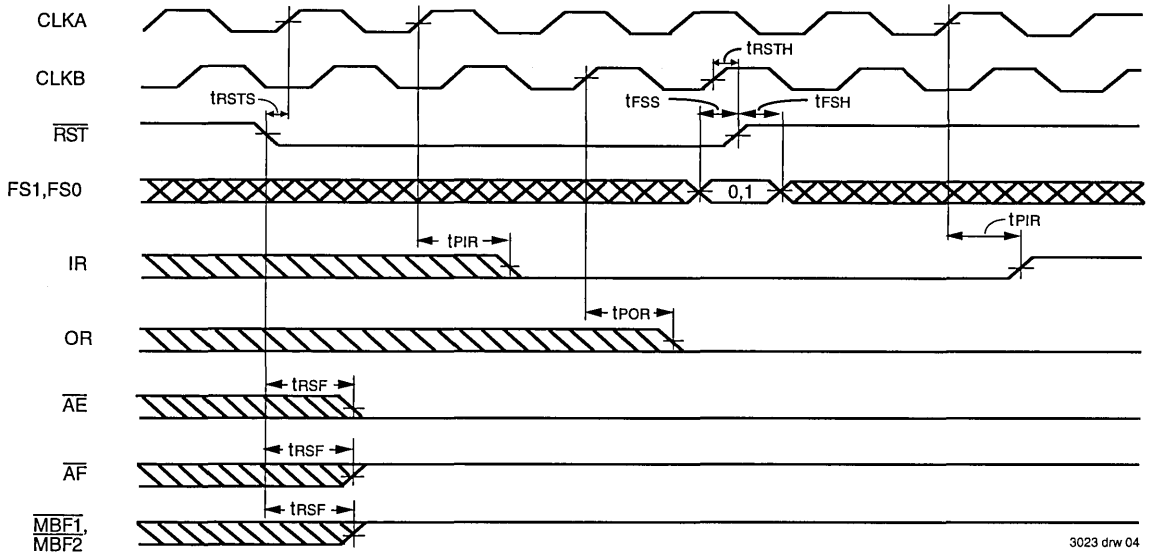
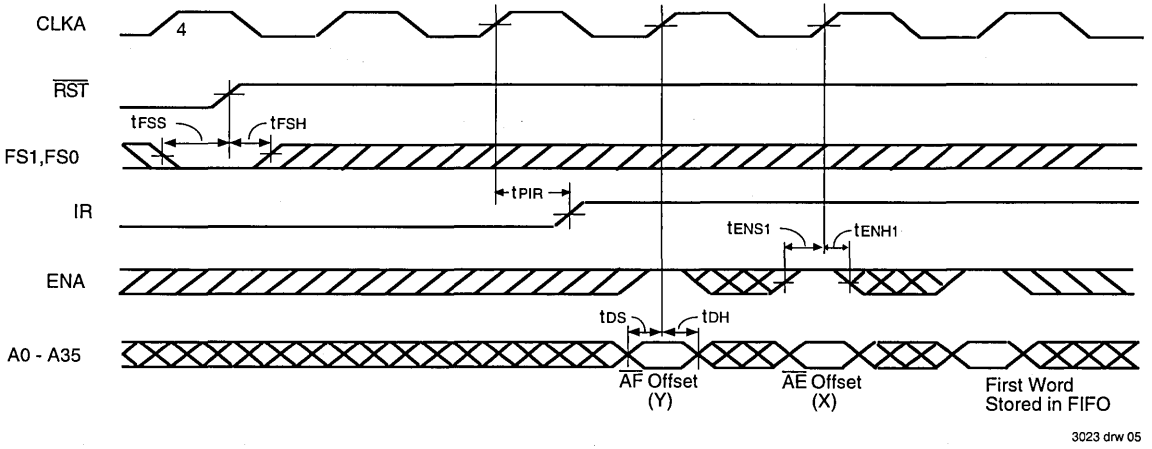


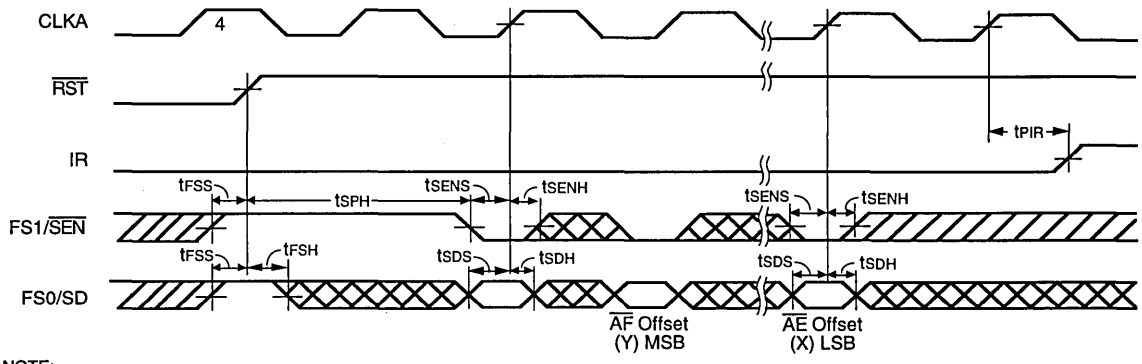
Figure 1. FIFO Reset Loading X and Y with a Preset Value of Eight

5



NOTE:
1. $\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW. It is not necessary to program offset register on consecutive clock cycles.

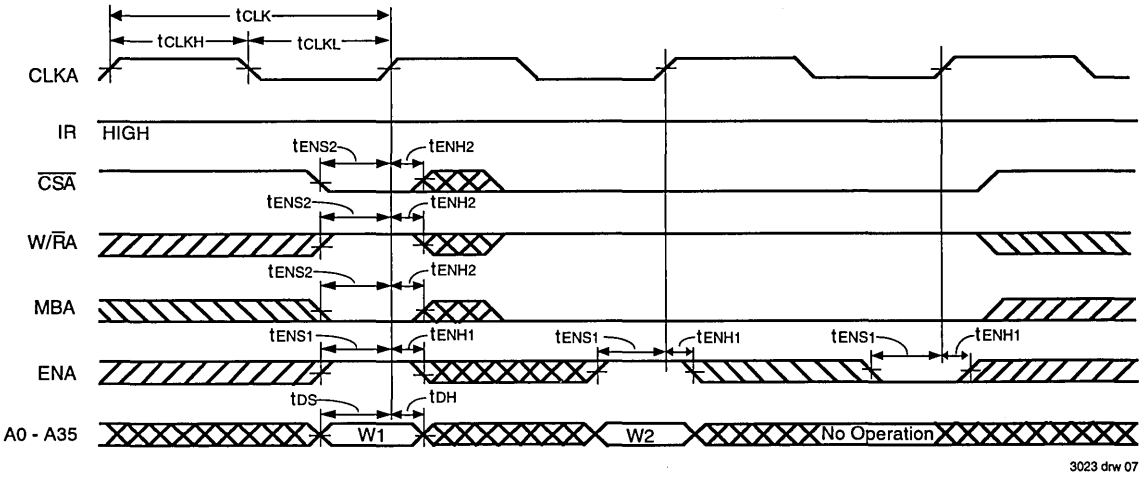
Figure 2. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values from Port A



NOTE:
1. It is not necessary to program offset register bits on consecutive clock cycles. FIFO write attempts are ignored until IR is set HIGH.

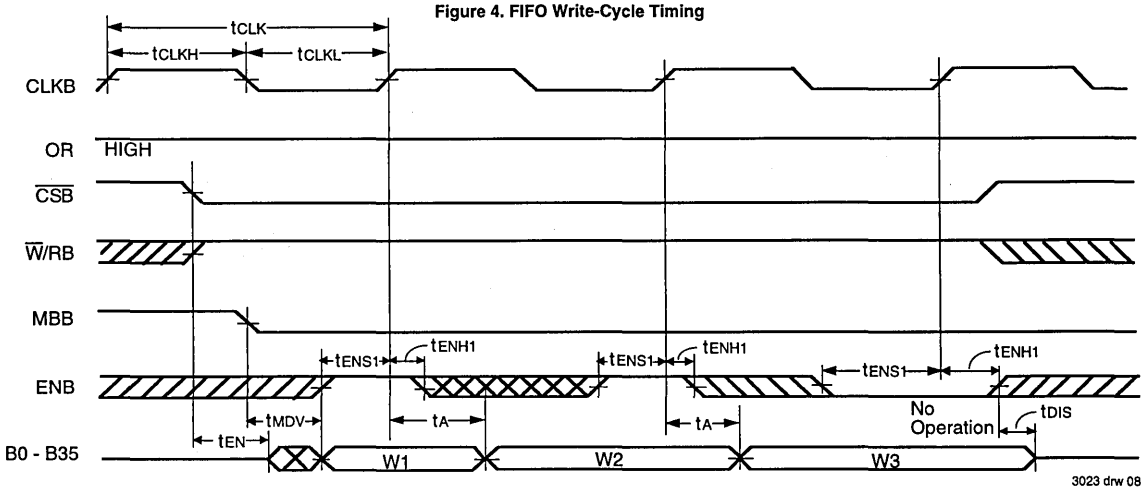
3023 drw 06

Figure 3. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values Serially



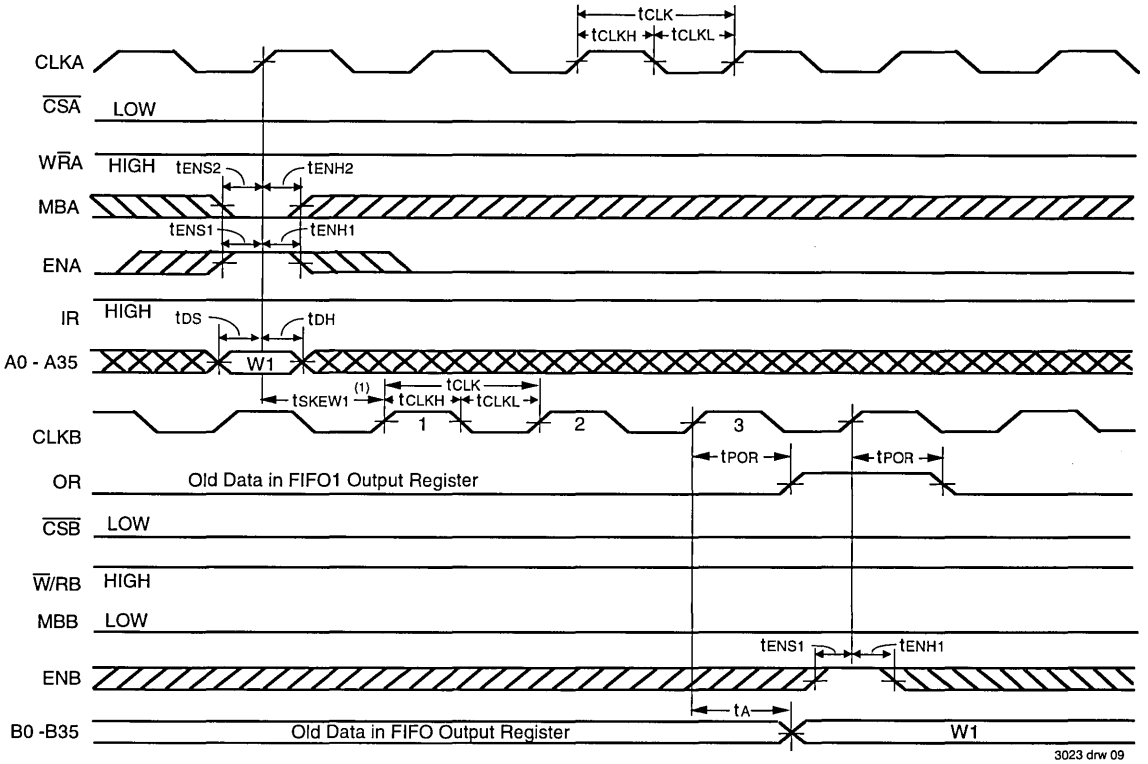
3023 drw 07

Figure 4. FIFO Write-Cycle Timing



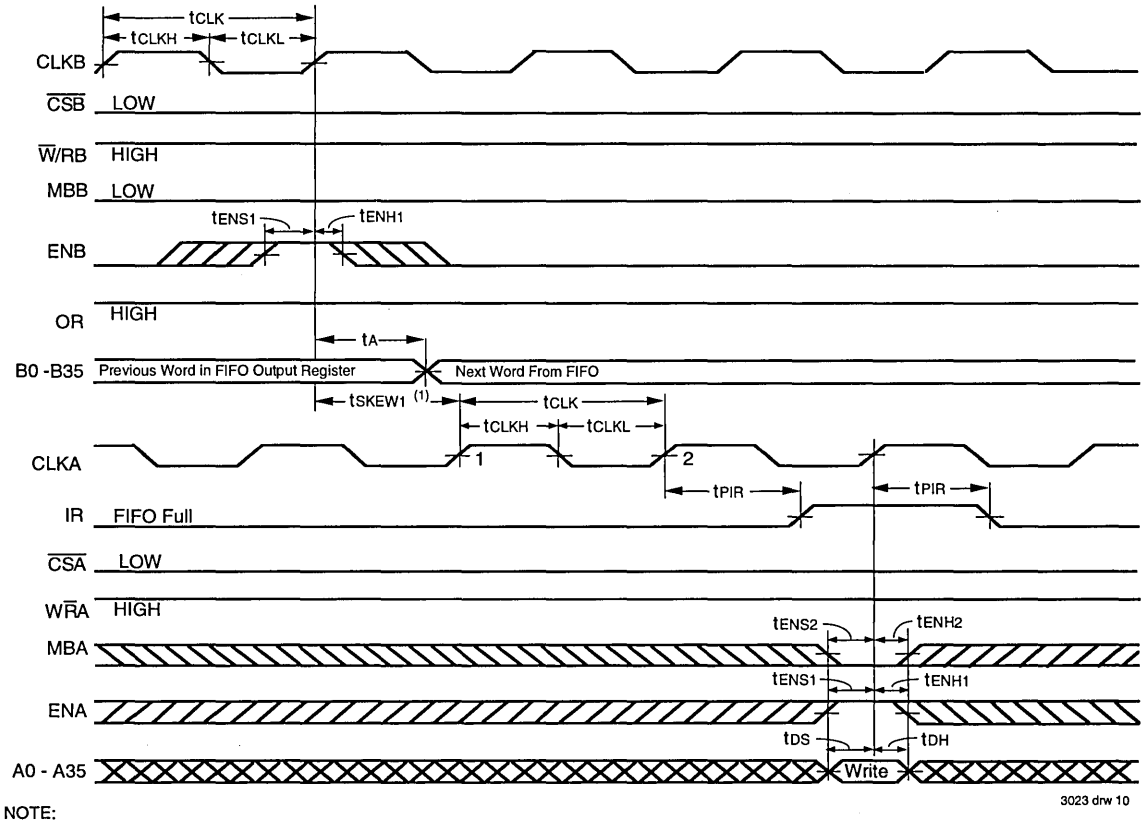
3023 drw 08

Figure 5. FIFO Read-Cycle Timing



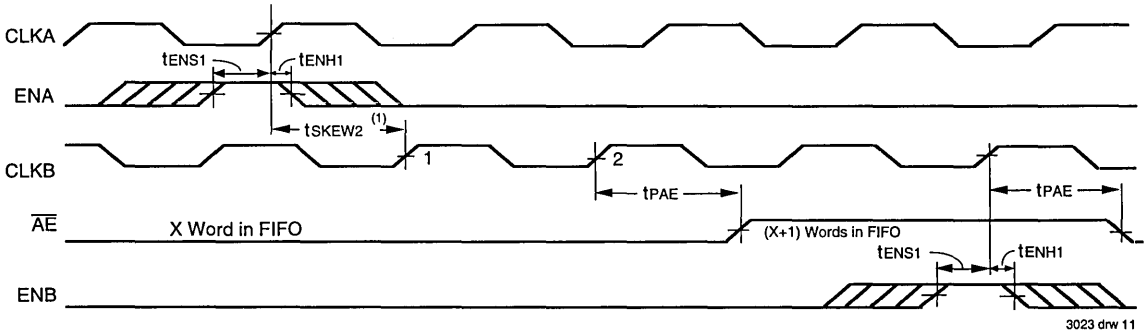
NOTE:
1. tSKEW1 is the minimum time between a rising CLKA edge and a rising CLKB edge for OR to transition HIGH and to clock the next word to the FIFO output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW1, then the transition of OR HIGH and the first word load to the output register may occur one CLKB cycle later than shown.

Figure 6. OR Flag Timing and First Data Word Fallthrough when the FIFO is Empty



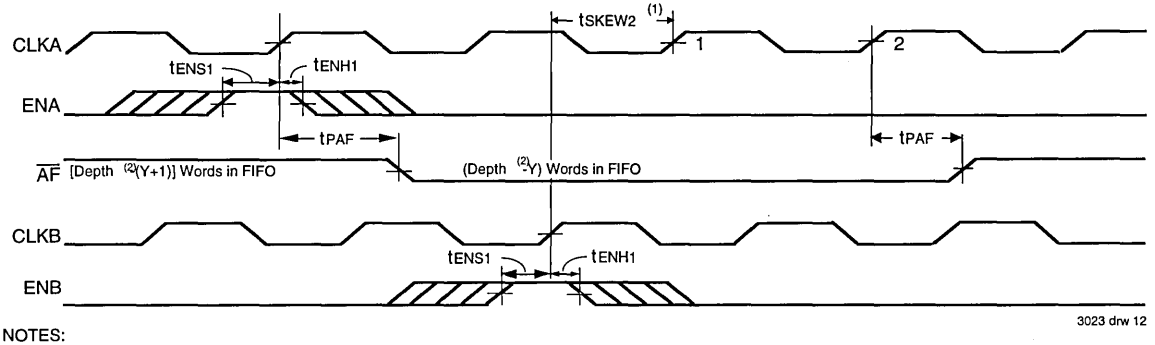
NOTE:
1. tSKEW1 is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW1, then IR may transition HIGH one CLKA cycle later than shown.

Figure 7. IR Flag Timing and First Available Write when the FIFO is Full



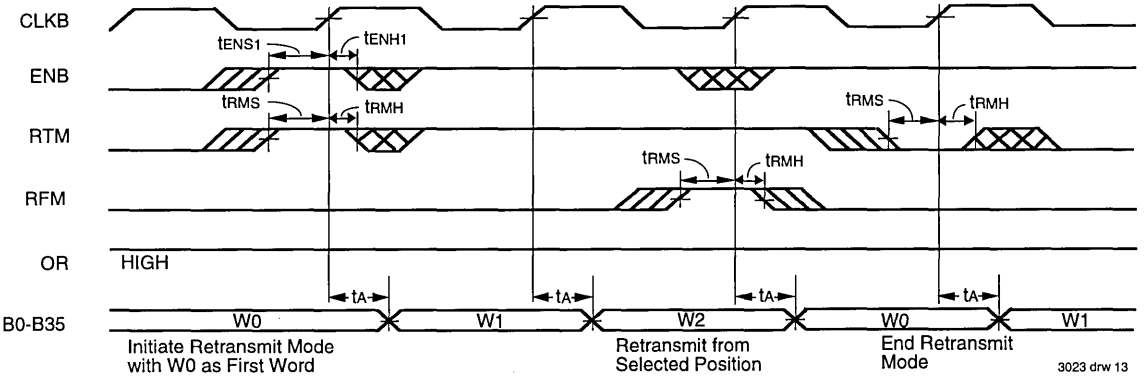
NOTES:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for AE to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then AE may transition HIGH one CLKB cycle later than shown.
2. FIFO write (CSA = LOW, W/RA = HIGH, MBA = LOW), FIFO read (CSB = LOW, W/RB = HIGH, MBB = LOW).

Figure 8. Timing for AE when FIFO is Almost Empty



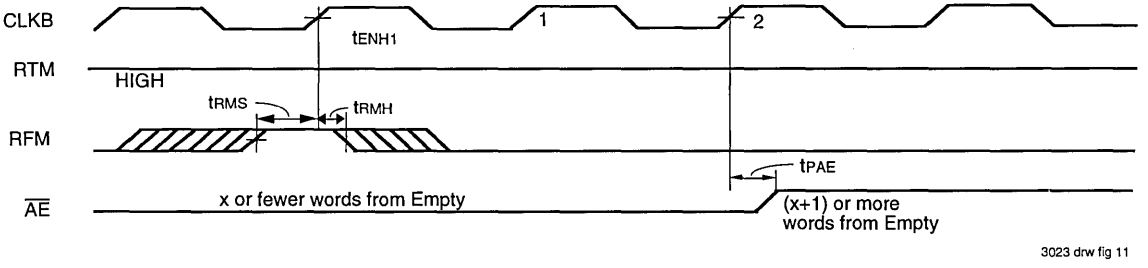
NOTES:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AF}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW2, then $\overline{AF}$ may transition HIGH one CLKA cycle later than shown.
2. Depth is 512 for the IDT723631, 1024 for the IDT723641, and 2048 for the IDT723651.
3. FIFO write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO read ($\overline{CSB}$ = LOW, $\overline{W}$/RB = HIGH, MBB = LOW).

Figure 9. Timing for $\overline{AF}$ when FIFO is Almost Full



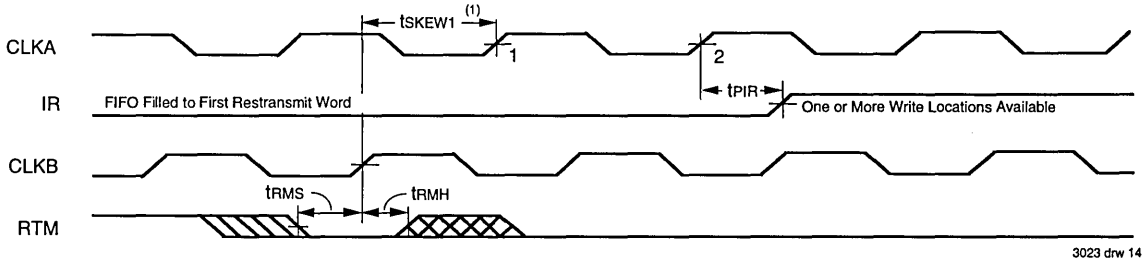
NOTE:
1. CSB = LOW, W/RB = HIGH, MBB = LOW. No input enables other than RTM and RFM are needed to control retransmit mode or begin a retransmit. Other enables are shown only to relate retransmit operations to the FIFO output register.

Figure 10. Retransmit Timing Showing Minimum Retransmit Length



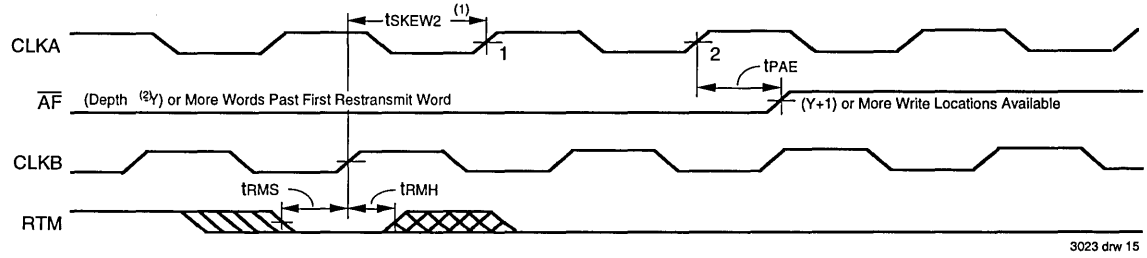
NOTE:
1. X is the value loaded in the almost empgy flag offset register.

Figure 11. $\overline{AE}$ Maximum Latency When Retransmit Increases the Number of Stored Words Above X.



NOTE:
1. tSKEW1 is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW1, then IR may transition HIGH one CLKA cycle later than shown.

Figure 12. IR Timing from the End of Retransmit Mode when One or More Write Locations are Available



NOTES:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for AF to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW2, then AF may transition HIGH one CLKA cycle later than shown.
2. Depth is 512 for the IDT723631, 1024 for the IDT723641, and 2048 for the IDT723651.
3. Y is the value loaded in the almost-full flag offset register.

Figure 13. $\overline{AF}$ Timing from the End of Retransmit Mode when (Y+1) or More Write Locations are Available

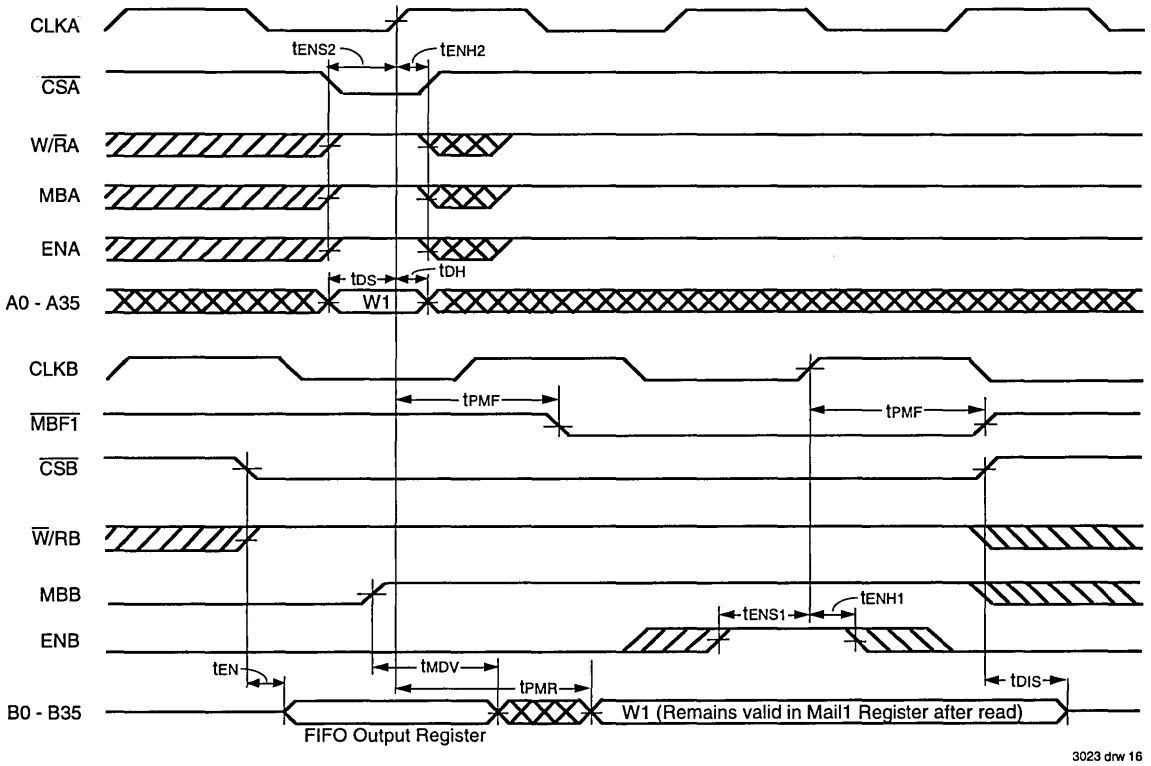


Figure 14. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag

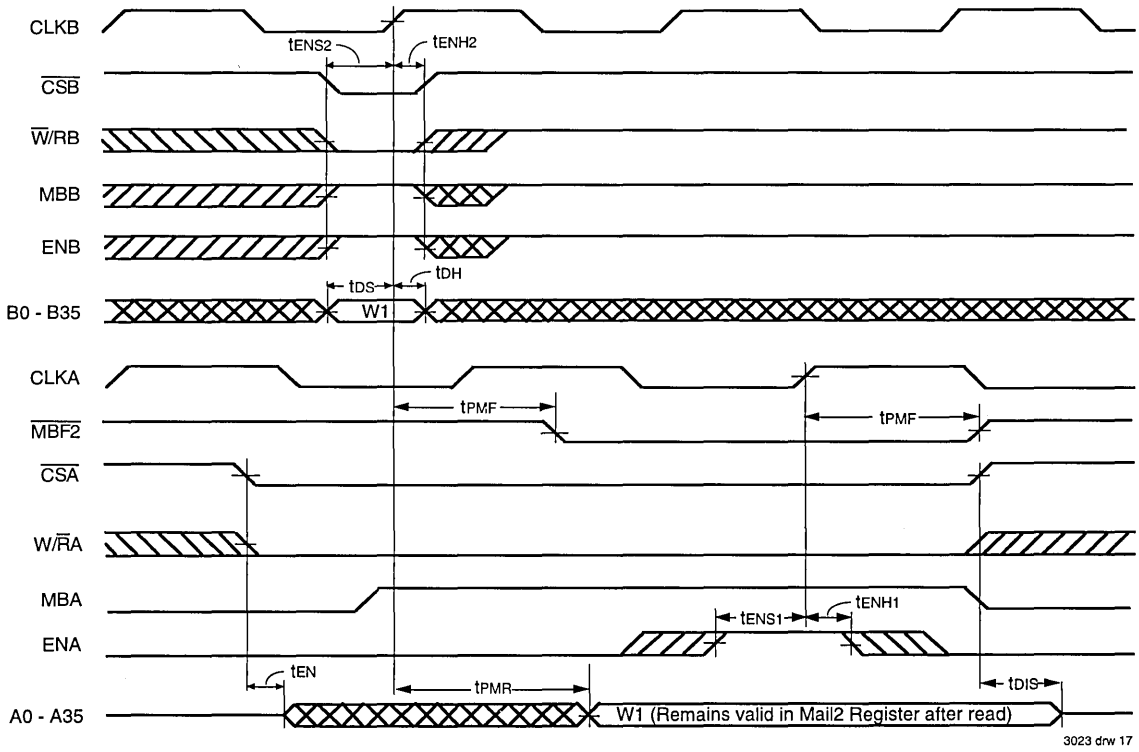


Figure 15. Timing for Mail2 Register and MBF2 Flag

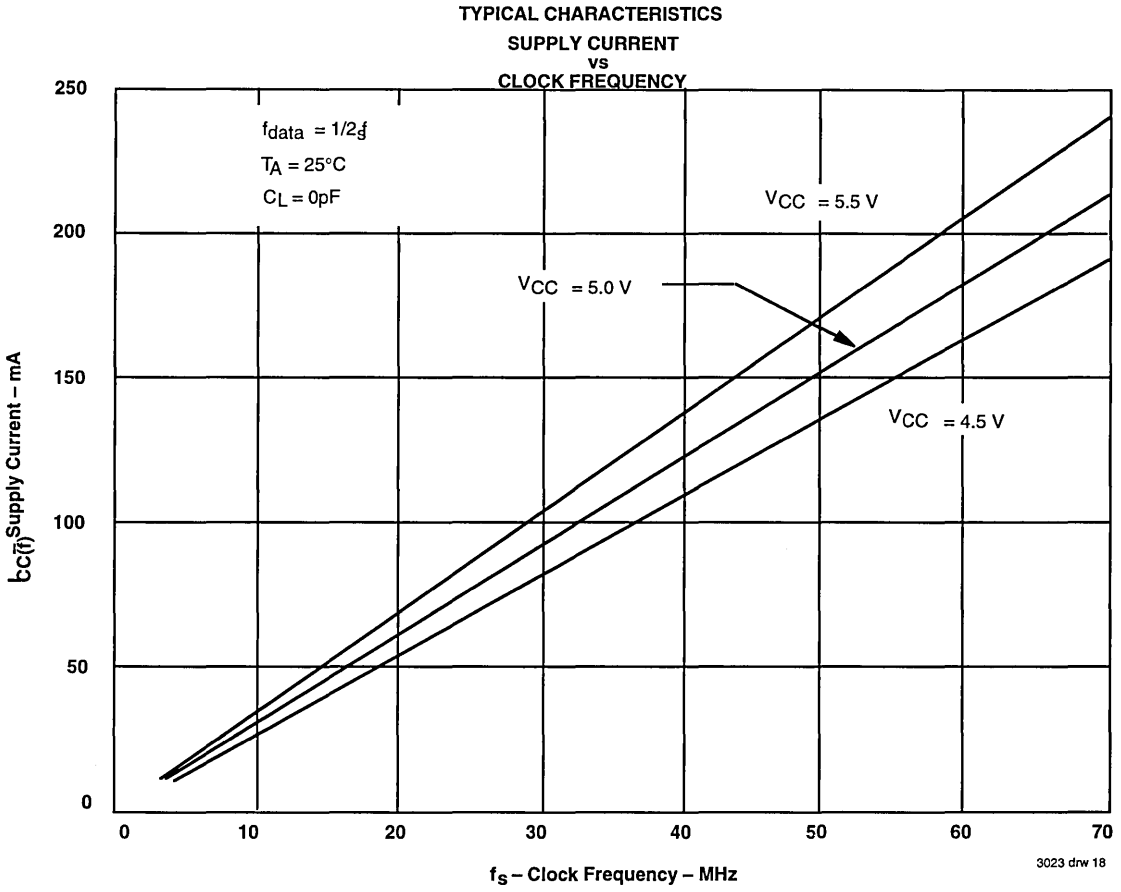


Figure 16

CALCULATING POWER DISSIPATION

The Icc(f) current for the graph in Figure 16 was taken while simultaneously reading and writing the FIFO on the IDT723641 with CLKA and CLKB set to fS. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitance load per data-output channel and the number of IDT723631/723641/723651 inputs driven by TTL HIGH levels are known, the power dissipation can be calculated with the equation below.

With Icc(f) taken from Figure 16, the maximum power dissipation (PT) of the IDT723631/723641/723651 may be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \Sigma(C_L \times V_{CC}^2 \times f_O)$$

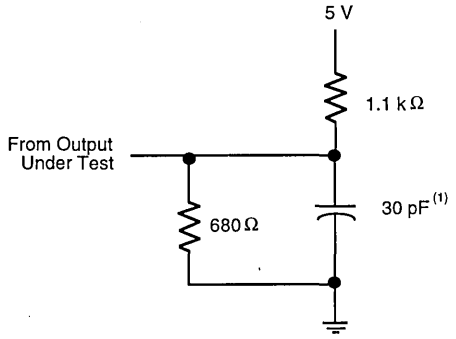
where:

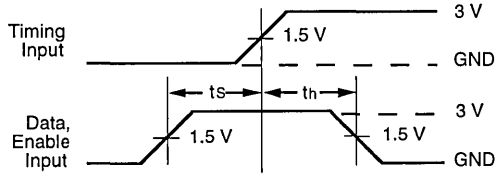
N	=	number of inputs driven by TTL levels
ΔIcc	=	increase in power supply current for each input at a TTL HIGH level
dc	=	duty cycle of inputs at a TTL HIGH level of 3.4
CL	=	output capacitance load
fo	=	switching frequency of an output

When no reads or writes are occurring on the IDT723631/723641/723651, the power dissipated by a single clock (CLKA or CLKB) input running at frequency fS is calculated by:

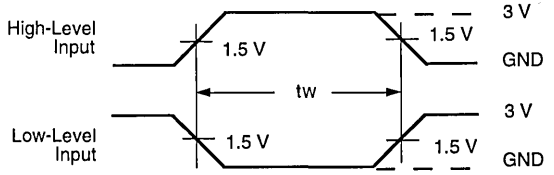
$$P_T = V_{CC} \times f_S \times 0.209\ mA/MHz$$

PARAMETER MEASUREMENT INFORMATION

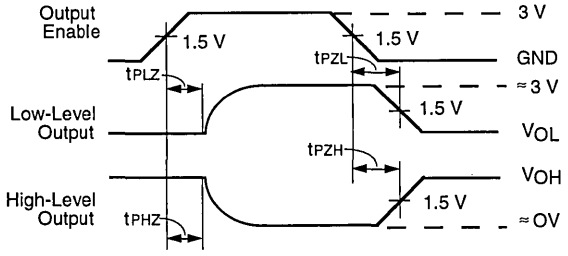




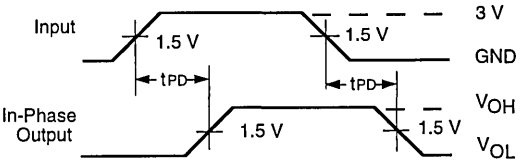
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



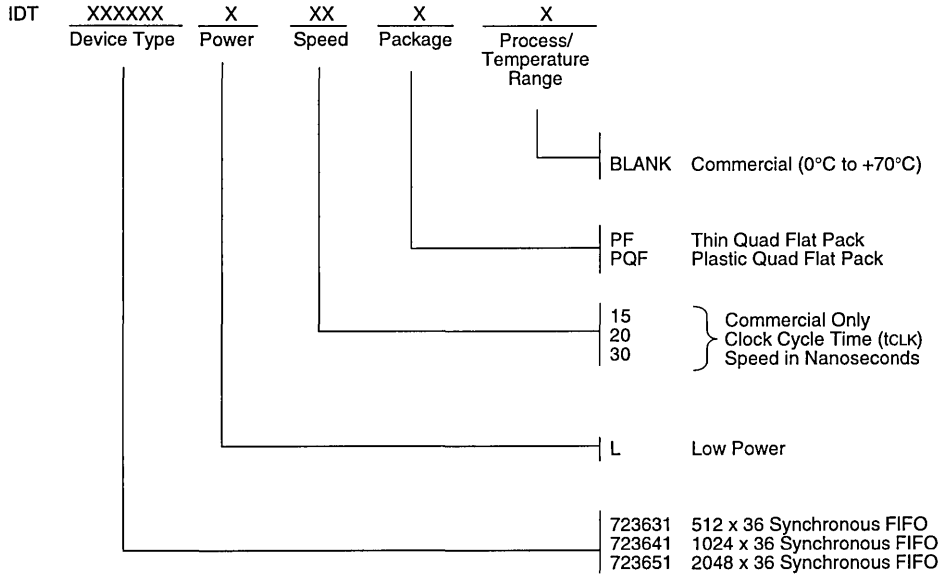
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

3023 drw 19

NOTE:
1. Includes probe and jig capacitance

Figure 17. Load Circuit and Voltage Waveforms

ORDERING INFORMATION



3023 drw 20

5

Integrated Device Technology, Inc.

CMOS SyncBiFIFO™ 256 x 18 x 2 and 512 x 18 x 2

IDT72605
IDT72615

FEATURES:

- Two independent FIFO memories for fully bidirectional data transfers
- 256 x 18 x 2 organization (IDT 72605)
- 512 x 18 x 2 organization (IDT 72615)
- Synchronous interface for fast (20ns) read and write cycle times
- Each data port has an independent clock and read/write control
- Output enable is provided on each port as a three-state control of the data bus
- Built-in bypass path for direct data transfer between two ports
- Two fixed flags, Empty and Full, for both the A-to-B and the B-to-A FIFO
- Programmable flag offset can be set to any depth in the FIFO
- The synchronous BiFIFO is packaged in a 64-pin TQFP (Thin Quad Flatpack), 68-pin PGA and 68-pin PLCC

DESCRIPTION:

The IDT72605 and IDT72615 are very high-speed, low-power bidirectional First-In, First-Out (FIFO) memories, with synchronous interface for fast read and write cycle times. The SyncBiFIFO™ is a data buffer that can store or retrieve information from two sources simultaneously. Two Dual-Port FIFO memory arrays are contained in the SyncBiFIFO; one data buffer for each direction.

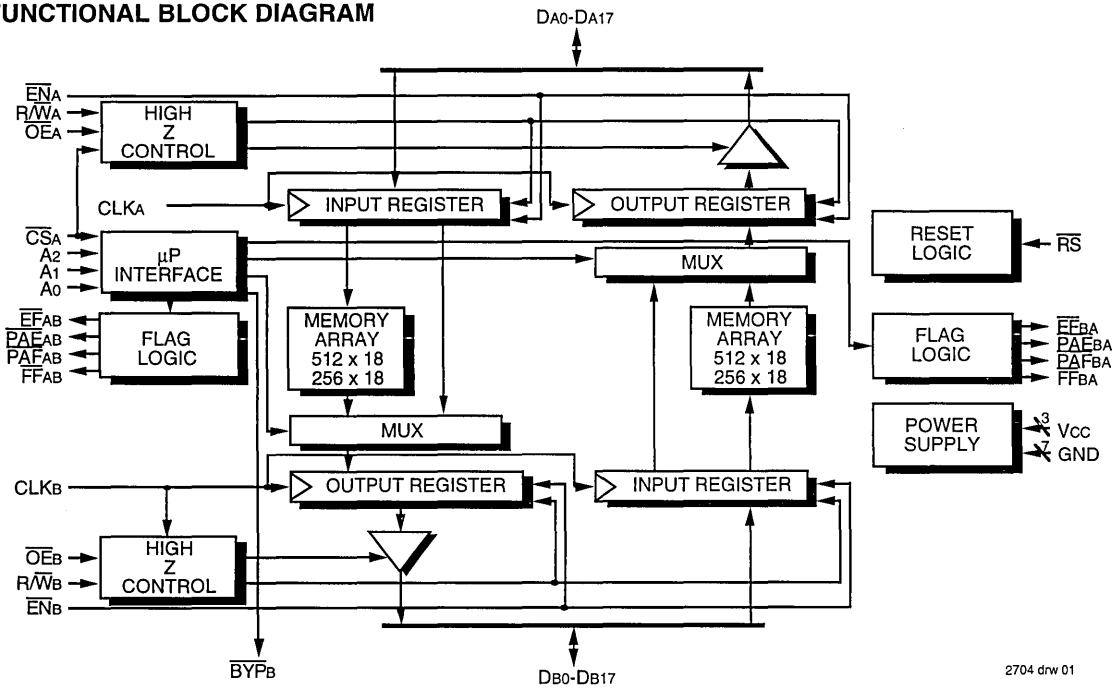
The SyncBiFIFO has registers on all inputs and outputs. Data is only transferred into the I/O registers on clock edges, hence the interfaces are synchronous. Each Port has its own independent clock. Data transfers to the I/O registers are gated by the enable signals. The transfer direction for each port is controlled independently by a read/write signal. Individual output enable signals control whether the SyncBiFIFO is driving the data lines of a port or whether those data lines are in a high-impedance state.

Bypass control allows data to be directly transferred from input to output register in either direction.

The SyncBiFIFO has eight flags. The flag pins are full, empty, almost-full, and almost-empty for both FIFO memories. The offset depths of the almost-full and almost-empty flags can be programmed to any location.

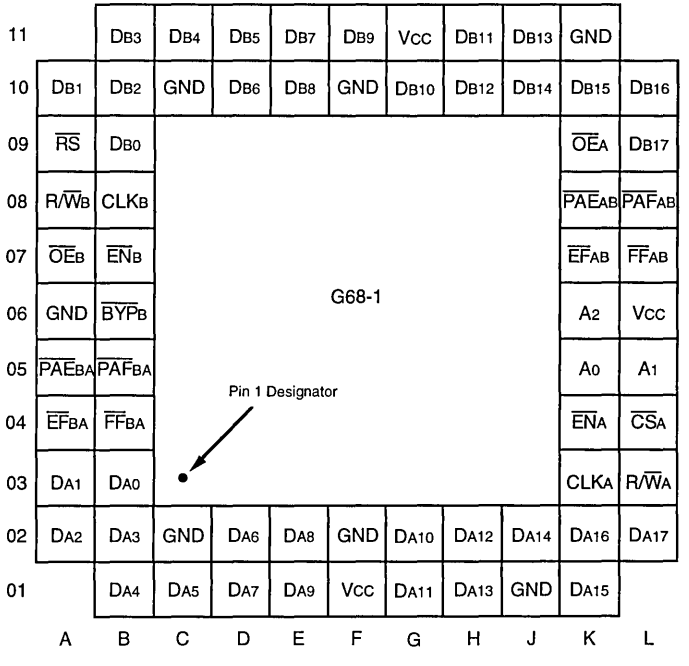
The SyncBiFIFO is fabricated using IDT's high-speed, submicron CMOS technology.

FUNCTIONAL BLOCK DIAGRAM

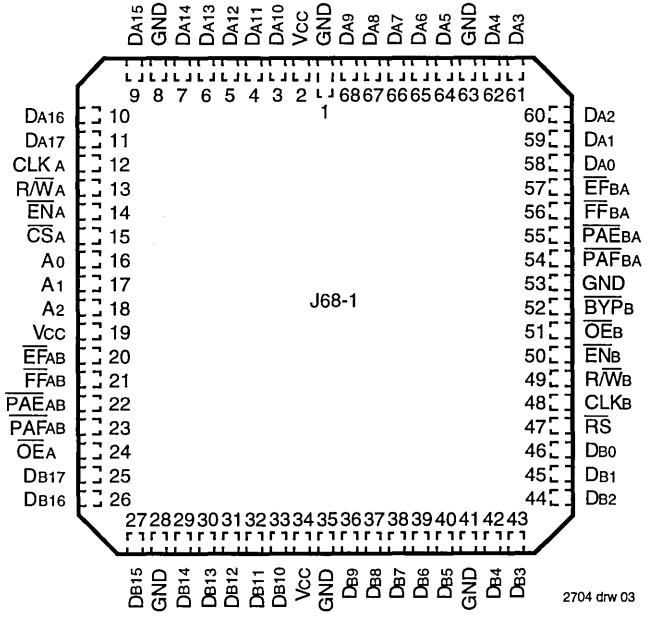


SyncBiFIFO is a trademark and the IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS

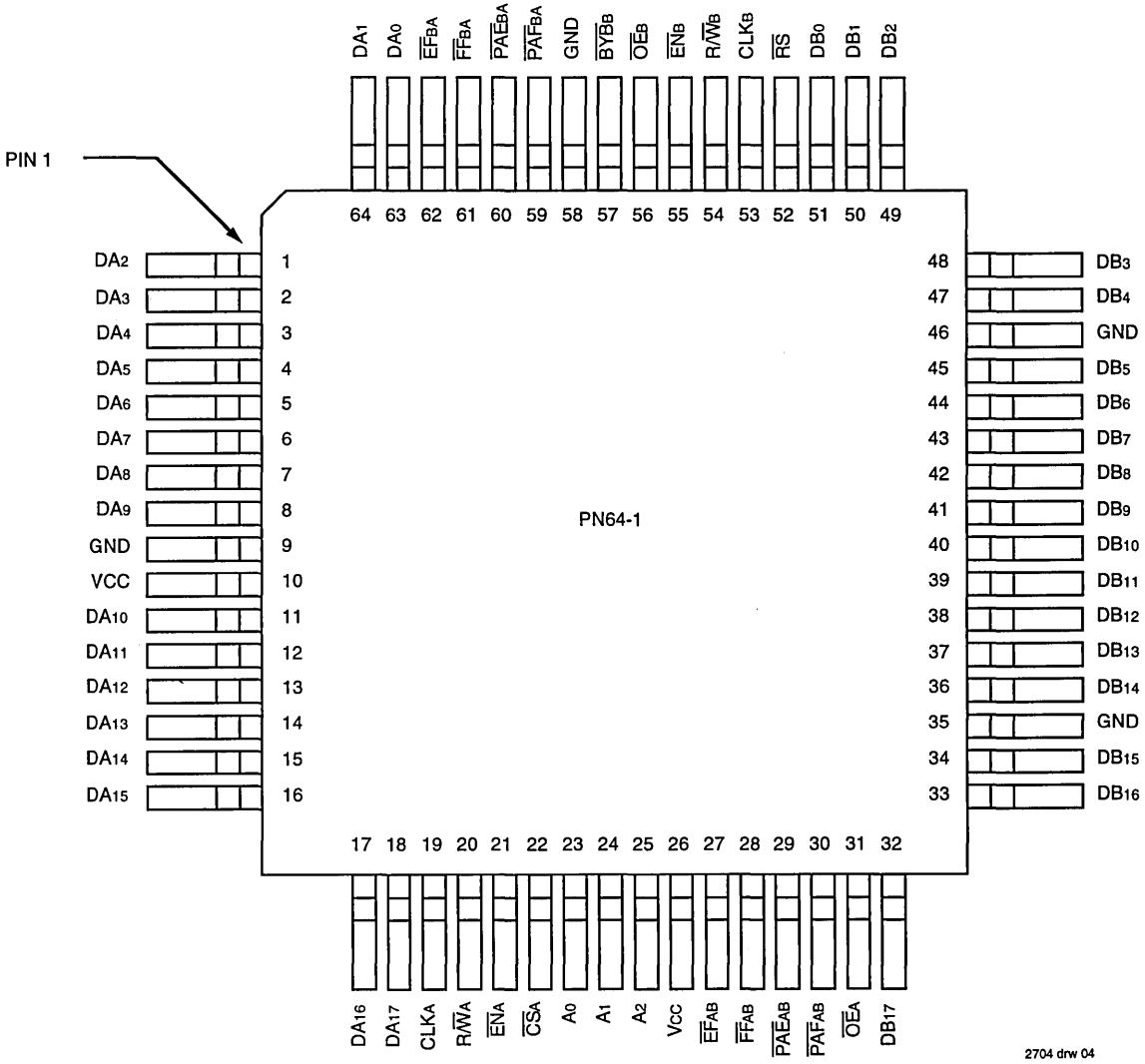


PGA
Top View



PLCC
Top View

PIN CONFIGURATIONS



TQFP
Top View

PIN DESCRIPTION

Symbol	Name	I/O	Description
D_{A0}-D_{A17}	Data A	I/O	Data inputs & outputs for the 18-bit Port A bus.
$\overline{CS}_A$	Chip Select A	I	Port A is accessed when $\overline{CS}_A$ is LOW. Port A is inactive if $\overline{CS}_A$ is HIGH.
R/$\overline{W}_A$	Read/Write A	I	This pin controls the read or write direction of Port A. If R/$\overline{W}_A$ is LOW, Data A input data is written into Port A. If R/$\overline{W}_A$ is HIGH, Data A output data is read from Port A. In bypass mode, when R/$\overline{W}_A$ is LOW, message is written into A→B output register. If R/$\overline{W}_A$ is HIGH, message is read from B→A output register.
CLK_A	Clock A	I	CLK_A is typically a free running clock. Data is read or written into Port A on the rising edge of CLK_A.
$\overline{EN}_A$	Enable A	I	When $\overline{EN}_A$ is LOW, data can be read or written to Port A. When $\overline{EN}_A$ is HIGH, no data transfers occur.
$\overline{OE}_A$	Output Enable A	I	When R/$\overline{W}_A$ is HIGH , Port A is an output bus and $\overline{OE}_A$ controls the high-impedance state of D_{A0}-D_{A17}. If $\overline{OE}_A$ is HIGH, Port A is in a high-impedance state. If $\overline{OE}_A$ is LOW while $\overline{CS}_A$ is LOW and R/$\overline{W}_A$ is HIGH, Port A is in an active (low-impedance) state.
A_0, A_1, A_2	Addresses	I	When $\overline{CS}_A$ is asserted, A_0, A_1, A_2 and R/$\overline{W}_A$ are used to select one of six internal resources.
D_{B0}-D_{B17}	Data B	I/O	Data inputs & outputs for the 18-bit Port B bus.
R/$\overline{W}_B$	Read/Write B	I	This pin controls the read or write direction of Port B. If R/$\overline{W}_B$ is LOW, Data B input data is written into Port B. If R/$\overline{W}_B$ is HIGH, Data B output data is read from Port B. In bypass mode, when R/$\overline{W}_B$ is LOW, message is written into B→A output register. If R/$\overline{W}_B$ is HIGH, message is read from A→B output register.
CLK_B	Clock B	I	Clock B is typically a free running clock. Data is read or written into Port B on the rising edge of CLK_B.
$\overline{EN}_B$	Enable B	I	When $\overline{EN}_B$ is LOW, data can be read or written to Port B. When $\overline{EN}_B$ is HIGH, no data transfers occur.
$\overline{OE}_B$	Output Enable B	I	When R/$\overline{W}_B$ is HIGH , Port B is an output bus and $\overline{OE}_B$ controls the high-impedance state of D_{B0}-D_{B17}. If OEB is HIGH, Port B is in a high-impedance state. If $\overline{OE}_B$ is LOW while R/$\overline{W}_B$ is HIGH, Port B is in an active (low-impedance) state.
$\overline{EF}_{AB}$	A→B Empty Flag	O	When $\overline{EF}_{AB}$ is LOW, the A→B FIFO is empty and further data reads from Port B are inhibited. When $\overline{EF}_{AB}$ is HIGH, the FIFO is not empty. $\overline{EF}_{AB}$ is synchronized to CLK_B. In the bypass mode, $\overline{EF}_{AB}$ HIGH indicates that data D_{A0}-D_{A17} is available for passing through. After the data D_{B0}-D_{B17} has been read, $\overline{EF}_{AB}$ goes LOW.
$\overline{PAE}_{AB}$	A→B Programmable Almost-Empty Flag	O	When $\overline{PAE}_{AB}$ is LOW, the A→B FIFO is almost empty. An almost empty FIFO contains less than or equal to the offset programmed into $\overline{PAE}_{AB}$ Register. When $\overline{PAE}_{AB}$ is HIGH, the A→B FIFO contains more than offset in $\overline{PAE}_{AB}$ Register. The default offset value for $\overline{PAE}_{AB}$ Register is 8. $\overline{PAE}_{AB}$ is synchronized to CLK_B.
$\overline{PAF}_{AB}$	A→B Programmable Almost-Full Flag	O	When $\overline{PAF}_{AB}$ is LOW, the A→B FIFO is almost full. An almost full FIFO contains greater than the FIFO depth minus the offset programmed into $\overline{PAF}_{AB}$ Register. When PAF_{AB} is HIGH, the A→B FIFO contains less than or equal to the depth minus the offset in PAF_{AB} Register. The default offset value for PAF_{AB} Register is 8. $\overline{PAF}_{AB}$ is synchronized to CLK_A.
$\overline{FF}_{AB}$	A→B Full Flag	O	When $\overline{FF}_{AB}$ is LOW, the A→B FIFO is full and further data writes into Port A are inhibited. When $\overline{FF}_{AB}$ is HIGH, the FIFO is not full. $\overline{FF}_{AB}$ is synchronized to CLK_A. In bypass mode, $\overline{FF}_{AB}$ tells Port A that a message is waiting in Port B's output register. If $\overline{FF}_{AB}$ is LOW, a bypass message is in the register. If $\overline{FF}_{AB}$ is HIGH, Port B has read the message and another message can be written into Port A.
$\overline{EF}_{BA}$	B→A Empty Flag	O	When $\overline{EF}_{BA}$ is LOW, the B→A FIFO is empty and further data reads from Port A are inhibited. When $\overline{EF}_{BA}$ is HIGH, the FIFO is not empty. $\overline{EF}_{BA}$ is synchronized to CLK_A. In the bypass mode, $\overline{EF}_{BA}$ HIGH indicates that data D_{B0}-D_{B17} is available for passing through. After the data D_{A0}-D_{A17} has been read, $\overline{EF}_{BA}$ goes LOW on the following cycle.
$\overline{PAE}_{BA}$	B→A Programmable Almost-Empty Flag	O	When $\overline{PAE}_{BA}$ is LOW, the B→A FIFO is almost empty. An almost empty FIFO contains less than or equal to the offset programmed into $\overline{PAE}_{BA}$ Register. When $\overline{PAE}_{BA}$ is HIGH, the B→A FIFO contains more than offset in $\overline{PAE}_{BA}$ Register. The default offset value for $\overline{PAE}_{BA}$ Register is 8. $\overline{PAE}_{BA}$ is synchronized to CLK_A.
$\overline{PAF}_{BA}$	B→A Programmable Almost-Full Flag	O	When $\overline{PAF}_{BA}$ is LOW, the B→A FIFO is almost full. An almost full FIFO contains greater than the FIFO depth minus the offset programmed into $\overline{PAF}_{BA}$ Register. When $\overline{PAF}_{BA}$ is HIGH, the B→A FIFO contains less than or equal to the depth minus the offset in $\overline{PAF}_{BA}$ Register. The default offset value for $\overline{PAF}_{BA}$ Register is 8. $\overline{PAF}_{BA}$ is synchronized to CLK_B.

2704 tbl 01

PIN DESCRIPTION (Continued)

Symbol	Name	I/O	Description
$\overline{FF}_{BA}$	B→A Full Flag	O	When $\overline{FF}_{BA}$ is LOW, the B→A FIFO is full and further data writes into Port B are inhibited. When $\overline{FF}_{BA}$ is HIGH, the FIFO is not full. $\overline{FF}_{BA}$ is synchronized to CLK_B. In bypass mode, $\overline{FF}_{BA}$ tells Port B that a message is waiting in Port A's output register. If $\overline{FF}_{BA}$ is LOW, a bypass message is in the register. If $\overline{FF}_{BA}$ is HIGH, Port A has read the message and another message can be written into Port B.
$\overline{BYP}_B$	Port B Bypass Flag	O	This flag informs Port B that the Synchronous BiFIFO is in bypass mode. When BYP_B is LOW, Port A has placed the FIFO into bypass mode. If $\overline{BYP}_B$ is HIGH, the Synchronous BiFIFO passes data into memory. $\overline{BYP}_B$ is synchronized to CLK_B.
$\overline{RS}$	Reset	I	A LOW on this pin will perform a reset of all Synchronous BiFIFO functions.
V_{CC}	Power		There are three +5V power pins for the PLCC and PGA packages and two for the TQFP.
GND	Ground		There are seven ground pins for the PLCC and PGA packages and four for the TQFP.

2704 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2704 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	—	V
V_{IL}(1)	Input Low Voltage	—	—	0.8	V

NOTE: 2704 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES: 2704 tbl 05

1. With output deselected.
2. Characterized values, not currently tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT72615L IDT72605L Commercial t_{CLK} = 20, 25, 35, 50ns			Unit
		Min.	Typ.	Max.	
I_{IL}(1)	Input Leakage Current (Any Input)	–1	—	1	µA
I_{OL}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	—	0.4	V
I_{CC}(3)	Average Vcc Power Supply Current	—	—	230	mA

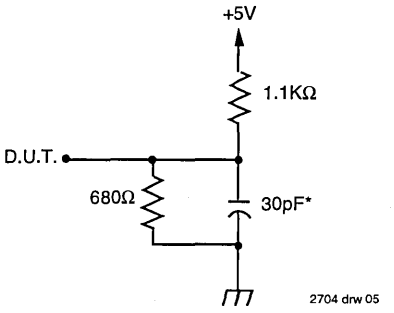
NOTES: 2704 tbl 06

1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OEA}$, $\overline{OEB}$ ≥ V_{IH}; 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested with outputs open. Testing frequency f=20MHz

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 2

2704 tbl 07



or equivalent circuit
Figure 2. Output Load
* Includes jig and scope capacitances.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C)

		Commercial									
		72615L20 72605L20		72615L25 72605L25		72615L35 72605L35		72615L50 72605L50			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Timing Figures
f_{CLK}	Clock frequency	—	50	—	40	—	28	—	20	MHz	—
t_{CLK}	Clock cycle time	20	—	25	—	35	—	50	—	ns	4,5,6,7
t_{CLKH}	Clock HIGH time	8	—	10	—	14	—	20	—	ns	4,5,6,7,12,13,14,15
t_{CLKL}	Clock LOW time	8	—	10	—	14	—	20	—	ns	4,5,6,7,12,13,14,15
t_{RS}	Reset pulse width	20	—	25	—	35	—	50	—	ns	3
t_{RSS}	Reset set-up time	12	—	15	—	21	—	30	—	ns	3
t_{RSR}	Reset recovery time	12	—	15	—	21	—	30	—	ns	3
t_{RSF}	Reset to flags in intial state	—	27	—	28	—	35	—	50	ns	3
t_A	Data access time	3	10	3	15	3	21	3	25	ns	5,7,8,9,10,11
t_{CS}	Control signal set-up time(1)	6	—	6	—	8	—	10	—	ns	4,5,6,7,8,9,10,11, 12, 13,14,15
t_{CH}	Control signal hold time(1)	1	—	1	—	1	—	1	—	ns	4,5,6,7,10,11,12, 13, 14,15
t_{DS}	Data set-up time	6	—	6	—	8	—	10	—	ns	4,6,8,9,10,11
t_{DH}	Data hold time	1	—	1	—	1	—	1	—	ns	4,6
t_{OE}	Output Enable LOW to output data valid(2)	3	10	3	13	3	20	3	28	ns	5,7,8,9,10,11
t_{OLZ}	Output Enable LOW to data bus at Low-Z(2)	0	—	0	—	0	—	0	—	ns	5,7,8,9,10,11
t_{OHZ}	Output Enable HIGH to data bus at High-Z(2)	3	10	3	13	3	20	3	28	ns	5,7,10,11
t_{FF}	Clock to Full Flag time	—	10	—	15	—	21	—	30	ns	4,6,10,11
t_{EF}	Clock to Empty Flag time	—	10	—	15	—	21	—	30	ns	5,7,8,9,10,11
t_{PAE}	Clock to Programmable Almost Empty Flag time	—	12	—	15	—	21	—	30	ns	12,14
t_{PAF}	Clock to Programmable Almost Full Flag time	—	12	—	15	—	21	—	30	ns	13,15
t_{SKEW1}	Skew between CLK_A & CLK_B for Empty/Full Flags(2)	10	—	12	—	17	—	20	—	ns	4,5,6,7,8,9,10,11
t_{SKEW2}	Skew between CLK_A & CLK_B for Programmable Flags(2)	17	—	19	—	25	—	34	—	ns	4, 7,12,13,14,15

NOTES:
1. Control signals refer to $\overline{CS}_A$, $R/\overline{W}_A$, $\overline{EN}_A$, A_2, A_1, A_0, $R/\overline{W}_B$, $\overline{EN}_B$.
2. Minimum values are guaranteed by design.

2704 tbl 08

FUNCTIONAL DESCRIPTION

IDTs SyncBiFIFO is versatile for both multiprocessor and peripheral applications. Data can be stored or retrieved from two sources simultaneously.

The SyncBiFIFO has registers on all inputs and outputs. Data is only transferred into the I/O registers on clock edges, hence the interfaces are synchronous. Two Dual-Port FIFO memory arrays are contained in the SyncBiFIFO; one data buffer for each direction. Each port has its own independent clock. Data transfers to the I/O registers are gated by the enable signals. The transfer direction for each port is controlled independently by a read/write signal. Individual output enable signals control whether the SyncBiFIFO is driving the data lines of a port or whether those data lines are in a high-impedance state. The processor connected to Port A of the BiFIFO can send or receive messages directly to the Port B device using the 18-bit bypass path.

The SyncBiFIFO can be used in multiples of 18-bits. In a 36- to 36-bit configuration, two SyncBiFIFOs operate in parallel. Both devices are programmed simultaneously, 18 data bits to each device. This configuration can be extended to wider bus widths (54- to 54-bits, 72- to 72-bits, etc.) by adding more SyncBiFIFOs to the configuration. Figure 1 shows multiple SyncBiFIFOs configured for multiprocessor communication.

The microprocessor or microcontroller connected to Port A controls all operations of the SyncBiFIFO. Thus, all Port A interface pins are inputs driven by the controlling processor. Port B interfaces with a second processor. The Port B control pins are inputs driven by the second processor.

RESET

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state with $\overline{CS}_A$, $\overline{EN}_A$ and $\overline{EN}_B$ HIGH. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The A→B and B→A FIFO Empty Flags ($\overline{EF}_{AB}$, $\overline{EF}_{BA}$) and Programmable Almost Empty Flags ($\overline{PAE}_{AB}$, $\overline{PAE}_{BA}$) will be set to LOW after t_{RSF}. The A→B and B→A FIFO Full Flags ($\overline{FF}_{AB}$, $\overline{FF}_{BA}$) and Programmable Almost Full Flags ($\overline{PAF}_{AB}$, $\overline{PAF}_{BA}$) will be set to HIGH after t_{RSF}. After the reset, the offsets of the Almost-Empty Flags and Almost-Full Flags for the A→B and B→A FIFO offset default to 8.

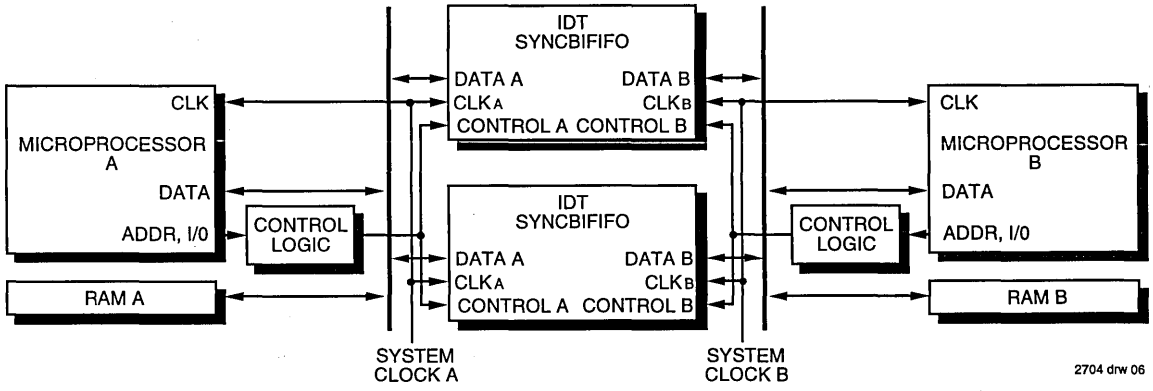
PORT A INTERFACE

The SyncBiFIFO is straightforward to use in micro-processor-based systems because each port has a standard microprocessor control set. Port A interfaces with microprocessor through the three address pins (A_2-A_0) and a Chip Select $\overline{CS}_A$ pins. When $\overline{CS}_A$ is asserted, A_2,A_1,A_0 and $R/\overline{W}_A$ are used to select one of six internal resources (Table 1).

With A_2=0 and A_1=0, A_0 determines whether data can be read out of output register or be written into the FIFO (A_0=0), or the data can pass through the FIFO through the bypass path (A_0=1).

With A_2=1, four programmable flags (two A→B FIFO programmable flags and two B→A FIFO programmable flags) can be selected: the A→B FIFO Almost-Empty Flag Offset (A_1=0, A_0=0), A→B FIFO Almost-Full Flag Offset (A_1=0, A_0=1), B→A FIFO Almost-Empty Flag Offset (A_1=1, A_0=0), B→A FIFO Almost-Full Flag Offset (A_1=1, A_0=1).

Port A is disabled when CSA is deasserted and data A is in high-impedance state.



NOTES:
1. Upper SyncBiFIFO only is used in 18- to 18-bit configuration.
2. Control A Consists of $R/\overline{W}_A$, $\overline{EN}_A$, $\overline{OE}_A$, $\overline{CS}_A$, A_2, A_1, A_0. Control B consists of $R/\overline{W}_B$, $\overline{EN}_B$, $\overline{OE}_B$.

Figure 1. 36- to 36-bit Processor Interface Configuration.

$\overline{CS_A}$	R/$\overline{W}_A$	$\overline{EN}_A$	$\overline{OE}_A$	Data A I/O	Port A Operation
0	0	0	0	I	Data A is written on CLKA ≠. This write cycle immediately following low-impedance cycle is prohibited. Note that even though OE_A = 0, a LOW logic level on R/W_A, once qualified by a rising edge on CLK_A, will put Data A into a high-impedance state.
0	0	0	1	I	Data A is written on CLKA ≠
0	0	1	X	I	Data A is ignored
0	1	0	0	O	Data is read[1] from RAM array to output register on CLKA ≠, Data A is low-impedance
0	1	0	1	O	Data is read[1] from RAM array to output register on CLKA ≠, Data A is high-impedance
0	1	1	0	O	Output register does not change[2], Data A is low-impedance
0	1	1	1	O	Output register does not change[2], Data A is high-impedance
1	0	X	X	I	Data A is ignored[3]
1	1	X	X	O	Data A is high-impedance[3]

NOTES: 2704 tbl 09

1. When $A_2A_1A_0$ = 000, the next B→A FIFO value is read out of the output register and the read pointer advances. If $A_2A_1A_0$ = 001, the bypass path is selected and bypass data from the Port B input register is read from the Port A output register. If $A_2A_1A_0$ = 1XX, a flag offset register is selected and its offset is read out through Port A output register.
2. Regardless of the condition of $A_2A_1A_0$, the data in the Port A output register does not change and the B→A read pointer does not advance.
3. If $CS_{A\#}$ is HIGH, then BYP_B is HIGH. No bypass occur under this condition.

Table 1. Port A Operation Control Signals

5

BYPASS PATH

The bypass paths provide direct communication between Port A and Port B. There are two full 18-bit bypass paths, one in each direction. During a bypass operation, data is passed directly between the input and output registers, and the FIFO memory is undisturbed.

Port A initiates and terminates all bypass operations. The bypass flag, $\overline{BYP}_B$, is asserted to inform Port B that a bypass operation is beginning. The bypass flag state is controlled by the Port A controls, although the $\overline{BYP}_B$ signal is synchronized to $\overline{CLK}_B$. So, $\overline{BYP}_B$ is asserted on the next rising edge of $\overline{CLK}_B$ when $A_2A_1A_0$=001and CS_A is LOW. When Port A returns to normal FIFO mode ($A_2A_1A_0$=000 or CS_A is HIGH), $\overline{BYP}_B$ is deasserted on the next $\overline{CLK}_B$ rising edge.

Once the SyncBiFIFO is in bypass mode, all data transfers are controlled by the standard Port A (R/$\overline{W}_A$, $\overline{CLK}_A$, $\overline{EN}_A$, $\overline{OE}_A$) and Port B (R/$\overline{W}_B$, $\overline{CLK}_B$, $\overline{EN}_B$, $\overline{OE}_B$) interface pins. Each bypass path can be considered as a one word deep FIFO. Data is held in each input register until it is read. Since the controls of each port operate independently, Port A can be reading bypass data at the same time Port B is reading bypass data.

When R/$\overline{W}_A$ and $\overline{EN}_A$ is LOW, data on pins D_{A0}-D_{A17} is written into Port A input register. Following the rising edge of $\overline{CLK}_A$ for this write, the A→B Full Flag ($\overline{FF}_{AB}$) goes LOW. Subsequent writes into Port A are blocked by internal logic until $\overline{FF}_{AB}$ goes HIGH again. On the next CLKB rising edge, the A→B Empty Flag ($\overline{EF}_{AB}$) goes HIGH indicating to Port B that data is available. Once R/$\overline{W}_B$ is HIGH and $\overline{EN}_B$ is LOW, data is read into the Port B output register. $\overline{OE}_B$ still controls whether Port B is in a high-impedance state. When $\overline{OE}_B$ is LOW, the output register data appears at D_{B0}-D_{B17}. $\overline{EF}_{AB}$ goes LOW following the $\overline{CLK}_B$ rising edge for this read. FFAB goes HIGH on the next $\overline{CLK}_A$ rising edge, letting Port A know that another word can be written through the bypass path.

Bypass data transfers from Port B to Port A work in a similar manner with $\overline{EFB}_A$ and $\overline{FFB}_A$ indicating the Port A output register state.

When the Port A address changes from bypass mode ($A_2A_1A_0$=001) to FIFO mode ($A_2A_1A_0$=000) on the rising edge of $\overline{CLK}_A$, the data held in the Port B output register may be overwritten. Unless Port A monitors the $\overline{BYP}_B$ pin and waits for Port B to clock out the last bypass word, data from the A→B FIFO will overwrite data in the Port B output register. $\overline{BYP}_B$ will go HIGH on the rising edge of $\overline{CLK}_B$ signifying that Port B has finished its last bypass operation. Port B must read any bypass data in the output register on this last $\overline{CLK}_B$ clock or it is lost and the SyncBiFIFO returns to FIFO operations. It is especially important to monitor $\overline{BYP}_B$ when $\overline{CLK}_B$ is much slower than $\overline{CLK}_A$ to avoid this condition. $\overline{BYP}_B$ will also go HIGH after $\overline{CS}_A$ is brought HIGH; in this manner the Port B bypass data may also be lost.

Since the Port A processor controls $\overline{CS}_A$ and the bypass mode, this scenario can be handled for B→A bypass data. The Port A processor must be set up to read the last bypass word before leaving bypass mode.

$\overline{CS}_A$	A_2	A_1	A_0	Read	Write
0	0	0	0	B→A FIFO	A→B FIFO
0	0	0	1	18-bit Bypass Path	
0	1	0	0	A→B FIFO Almost-Empty Flag Offset	
0	1	0	1	A→B FIFO Almost-Full Flag Offset	
0	1	1	0	B→A FIFO Almost-Empty Flag Offset	
0	1	1	1	B→A FIFO Almost-Full Flag Offset	
1	X	X	X	Port A Disabled	

2704 tbl 10

Table 2. Accessing Port A Resources Using $\overline{CS}_A$, A_2, A_1, and A_0.

PORT A CONTROL SIGNALS

The Port A control signals pins dictate the various operations shown in Table 2. Port A is accessed when $\overline{CS}_A$ is LOW, and is inactive if $\overline{CS}_A$ is HIGH. $R/\overline{W}_A$ and $\overline{EN}_A$ lines determine when Data A can be written or read. If $R/\overline{W}_A$ and $\overline{EN}_A$ are LOW, data is written into input register on the LOW-to-HIGH transition of $\overline{CLK}_A$. If $R/\overline{W}_A$ is HIGH and $\overline{OE}_A$ is LOW, data comes out of bus and is read from output register into three-state buffer. Refer to pin descriptions for more information.

PROGRAMMABLE FLAGS

The IDT SyncBiFIFO has eight flags: four flags for A→B FIFO ($\overline{EF}_{AB}$, $\overline{PAE}_{AB}$, $\overline{PAF}_{AB}$, $\overline{FF}_{AB}$), and four flags for B→A FIFO ($\overline{EF}_{BA}$, $\overline{PAE}_{BA}$, $\overline{PAF}_{BA}$, $\overline{FF}_{BA}$). The Empty and Full flags are fixed, while the Almost Empty and Almost Full offsets can be set to any depth through the Flag Offset Registers (see Table 3). The flags are asserted at the depths shown in the Flag Truth Table (Table 4). After reset, the programmable flag offsets are set to 8. This means the Almost Empty flags are asserted at Empty +8 words deep, and the Almost Full flags are asserted at Full -8 words deep.

The $\overline{PAE}_{AB}$ is synchronized to $\overline{CLK}_B$, while $\overline{PAE}_{AB}$ is synchronized to $\overline{CLK}_A$; and $\overline{PAE}_{BA}$ is synchronized to $\overline{CLK}_A$, while $\overline{PAE}_{BA}$ is synchronized to $\overline{CLK}_B$. If the minimum time (t_{SKEW2}) between a rising $\overline{CLK}_B$ and a rising $\overline{CLK}_A$ is met, the flag will change state on the current clock; otherwise, the flag may not change state until the next clock rising edge. For the specific flag timings, refer to Figures 12-15.

PORT B CONTROL SIGNALS

The Port B control signal pins dictate the various operations shown in Table 5. Port B is independent of $\overline{CS}_A$. $R/\overline{W}_B$ and $\overline{EN}_B$ lines determine when Data can be written or read in Port B. If $R/\overline{W}_B$ and $\overline{EN}_B$ are LOW, data is written into input register, and on LOW-to-HIGH transition of $\overline{CLK}_B$ data is written into

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{PAE}_{AB}$ Register	X	X	X	X	X	X	X	X	X	A→B FIFO Almost-Empty Flag Offset								
$\overline{PAF}_{AB}$ Register	X	X	X	X	X	X	X	X	X	A→B FIFO Almost-Full Flag Offset								
$\overline{PAE}_{BA}$ Register	X	X	X	X	X	X	X	X	X	B→A FIFO Almost-Empty Flag Offset								
$\overline{PAF}_{BA}$ Register	X	X	X	X	X	X	X	X	X	B→A FIFO Almost-Full Flag Offset								

2704 tbl 11

NOTE:
1. Bit 8 must be set to 0 for the IDT72605 (256 x 18) Synchronous BiFIFO.

Table 3. Flag Offset Register Format.

Number of Words in FIFO					
From	To	$\overline{EF}$	$\overline{PAE}$	$\overline{PAF}$	$\overline{FF}$
0	0	LOW	LOW	HIGH	HIGH
1	n	HIGH	LOW	HIGH	HIGH
n+1	D-(m+1)	HIGH	HIGH	HIGH	HIGH
D-m	D-1	HIGH	HIGH	LOW	HIGH
D	D	HIGH	HIGH	LOW	LOW

NOTES:
n = Programmable Empty Offset ($\overline{PAE}_{AB}$ Register or $\overline{PAE}_{BA}$ Register)
m = Programmable Full Offset ($\overline{PAF}_{AB}$ Register or $\overline{PAF}_{BA}$ Register)
D = FIFO Depth (IDT72605 = 256 words, IDT72615= 512 words)

2704 tbl 12

Table 4. Internal Flag Truth Table.

input register and the FIFO memory. If $R/\overline{W}_B$ is HIGH and $\overline{OE}_B$ is LOW, data comes out of bus and is read from output register into three-state buffer. In bypass mode, if $R/\overline{W}_B$ is LOW, bypass messages are transferred into B→A output register. If $R/\overline{W}_A$ is HIGH, bypass messages are transferred into A→B output register. Refer to pin descriptions for more information.

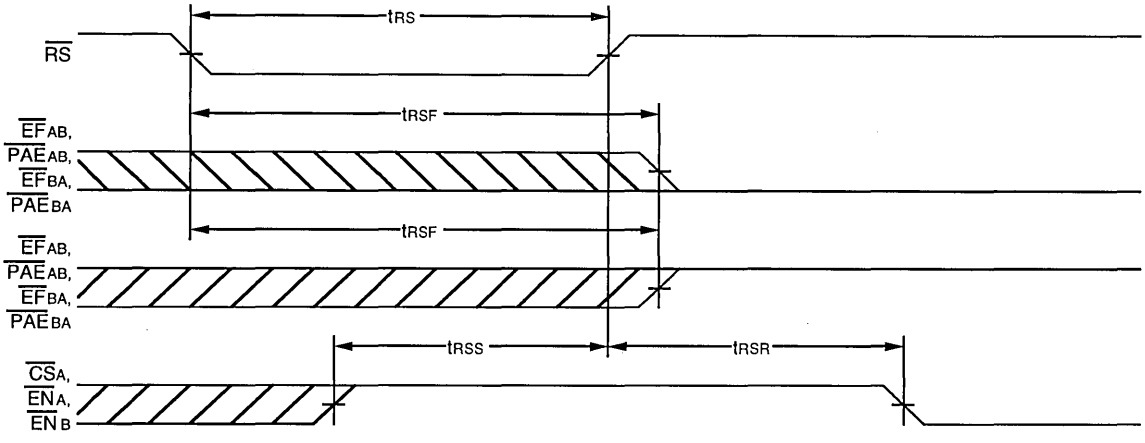
$R/\overline{W}_B$	$\overline{EN}_B$	$\overline{OE}_B$	Data B I/O	Port B Operation
0	0	0	I	Data B is written on CLKB ↑. This write cycle immediately following output low-impedance cycle is prohibited. Note that even though $\overline{OE}_B$ = 0, a LOW logic level on $R/\overline{W}_B$, once qualified by a rising edge on CLK_B, will put Data B into a high-impedance state.
0	0	1	I	Data B is written on CLKB ↑.
0	1	X	I	Data B is ignored
1	0	0	O	Data is read(1) from RAM array to output register on CLKB ≠, Data B is LOW impedance
1	0	1	O	Data is read(1) from RAM array to output register on CLKB ≠, Data B is HIGH impedance
1	1	0	O	Output register does not change(2), Data B is low-impedance
1	1	1	O	Output register does not change(2), Data B is high-impedance

NOTES:
2704 tbl 13

1. When $A_2A_1A_0$ = 000 or 1XX, the next A→B FIFO value is read out of the output register and the read pointer advances. If $A_2A_1A_0$ = 001, the bypass path is selected and bypass data is read from the Port B output register.
2. Regardless of the condition of $A_2A_1A_0$, the data in the Port B output register does not change and the A→B read pointer does not advance.

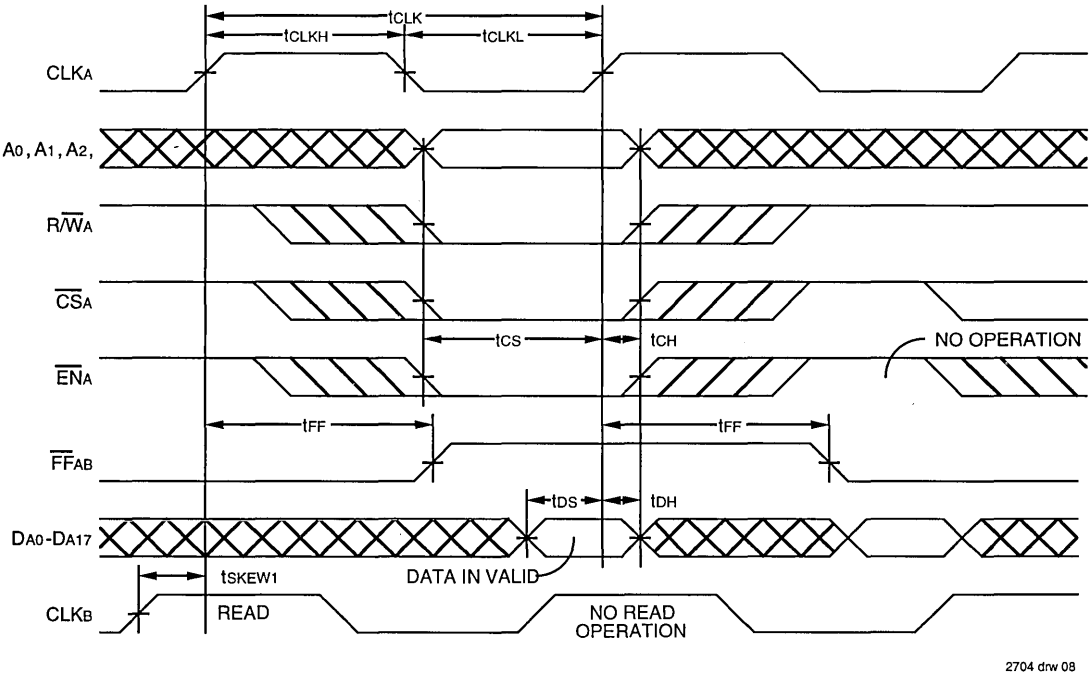
Table 5. Port B Operation Control Signals.

5



2704 drw 07

Figure 3. Reset Timing



2704 drw 08

Figure 4. Port A (A→B) Write Timing

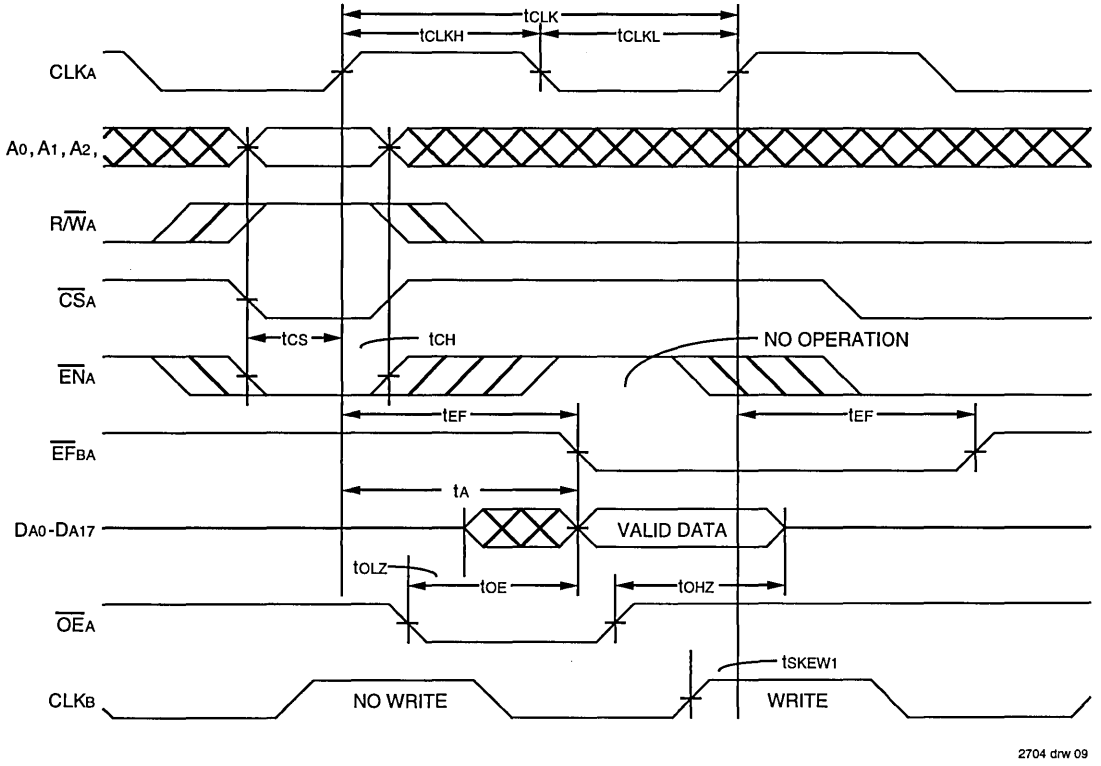


Figure 5. Port A (B→A) Read Timing

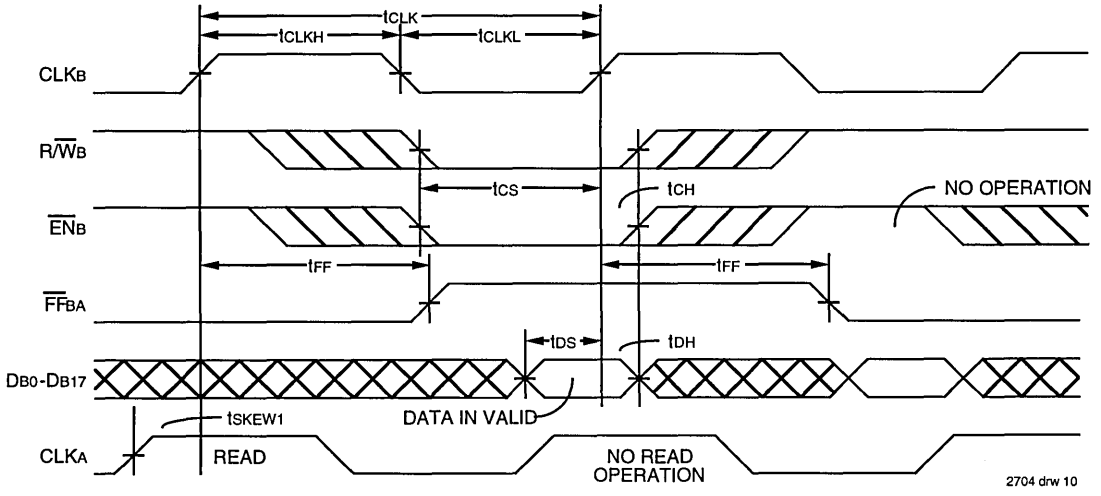


Figure 6. Port B (B→A) Write Timing

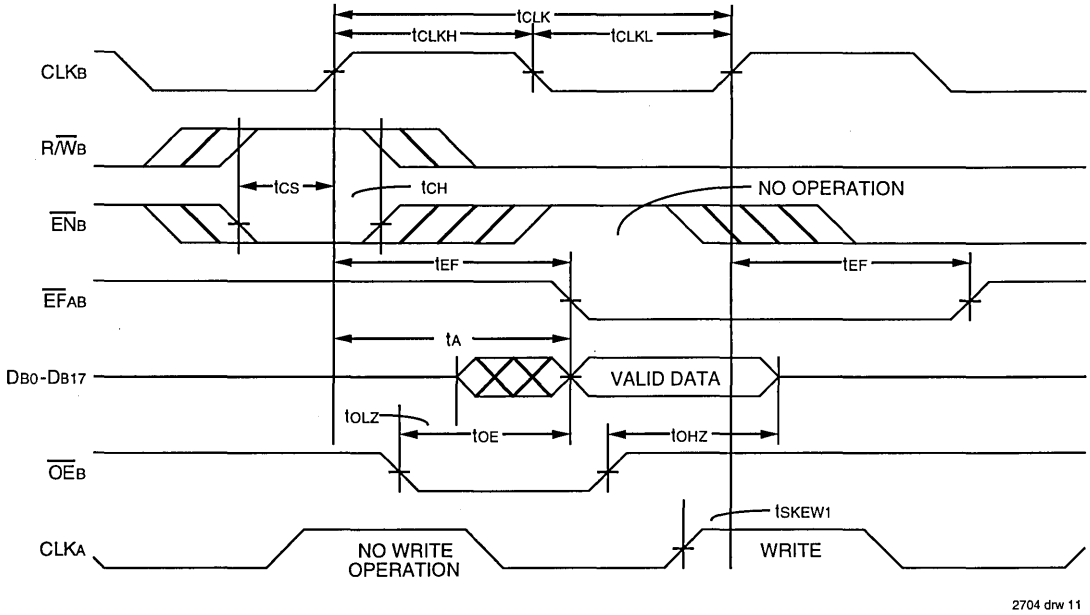
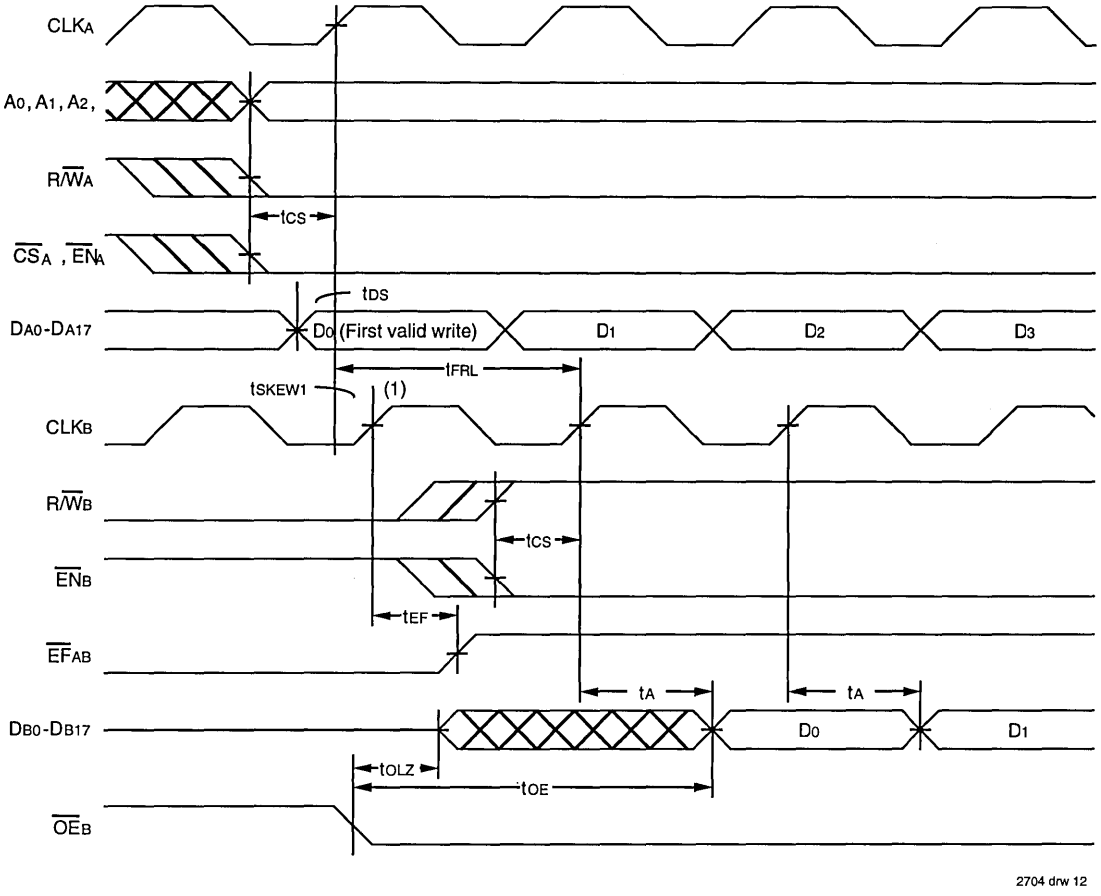
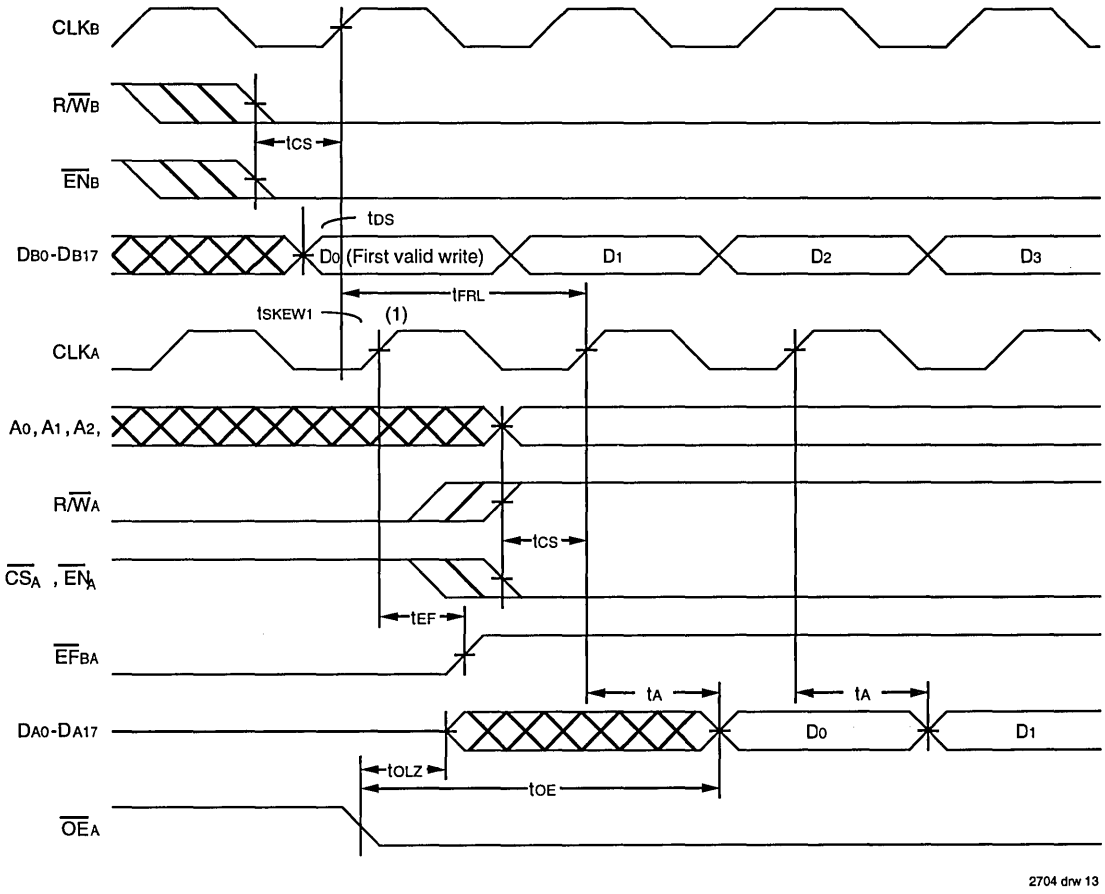


Figure 7. Port B (A→B) Read Timing



NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL(Max.)} = t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, $t_{FRL(Max.)} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).

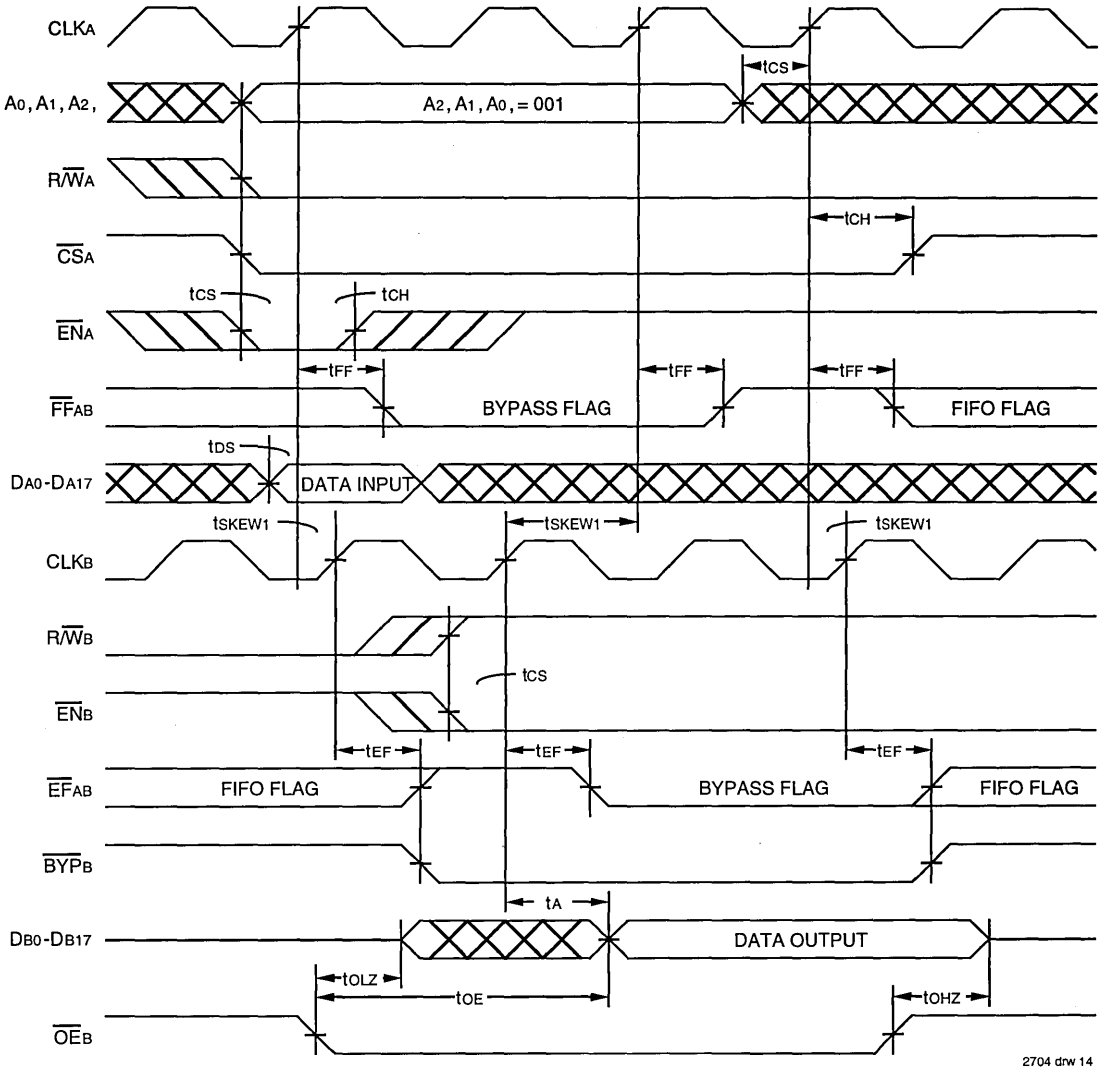
Figure 8. A→B First Data Word Latency after Reset for Simultaneous Read and Write



2704 drw 13

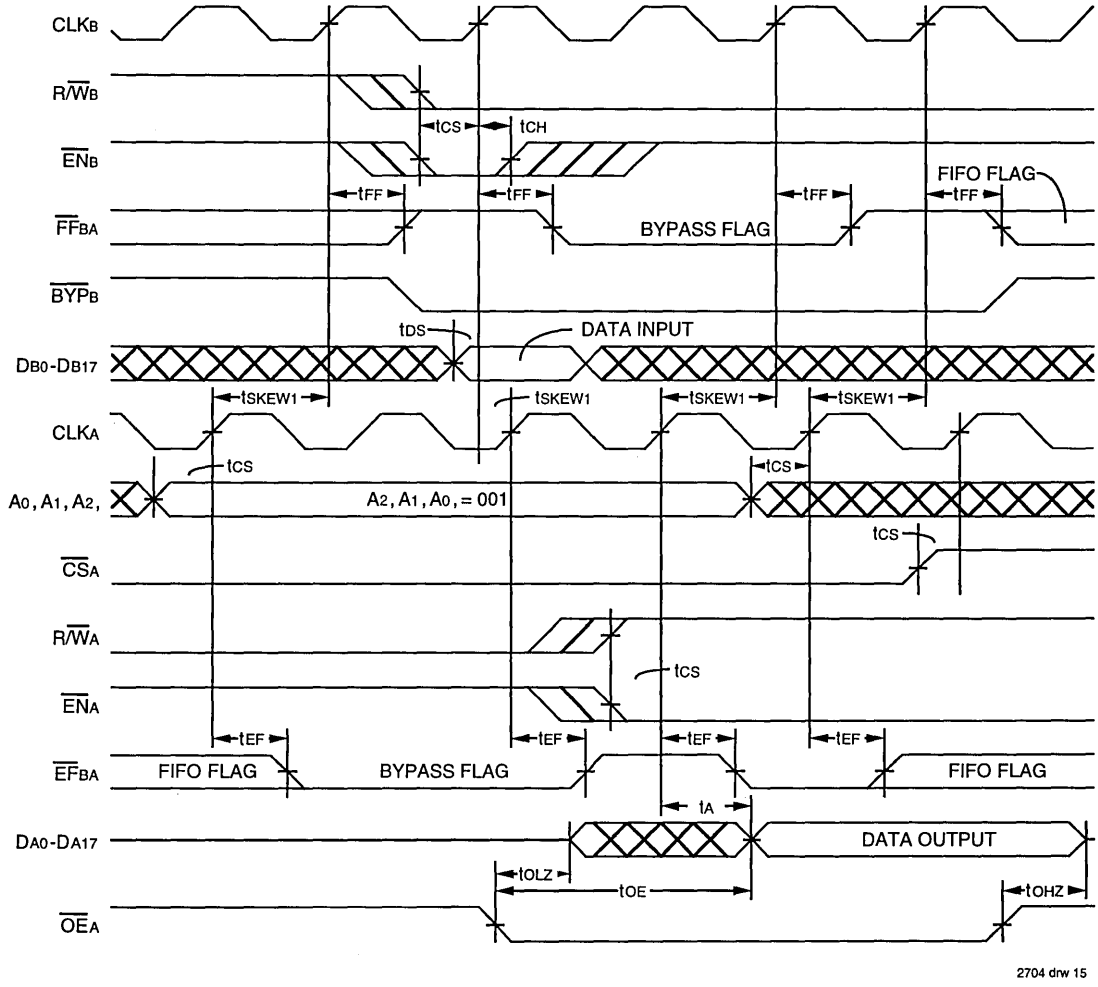
NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL(Max.)} = t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, $t_{FRL(Max.)} = 2t_{CLK} + t_{SKEW1}$
   The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 9. B→A First Data Word Latency after Reset for Simultaneous Read and Write



NOTES:
1. When $\overline{CS}_A$ is brought HIGH, A→B Bypass mode will switch to FIFO mode on the following CLKA LOW-to-HIGH transition.
2. After the bypass operation is completed, the $\overline{BYP}_B$ goes from LOW-to-HIGH; this will reset all bypass flags. The bypass path becomes available for the next bypass operation.
3. When A-side changed from bypass mode into FIFO mode, B-side only has one cycle to read the bypass data. On the next cycle, B-side will be forced back to FIFO mode.

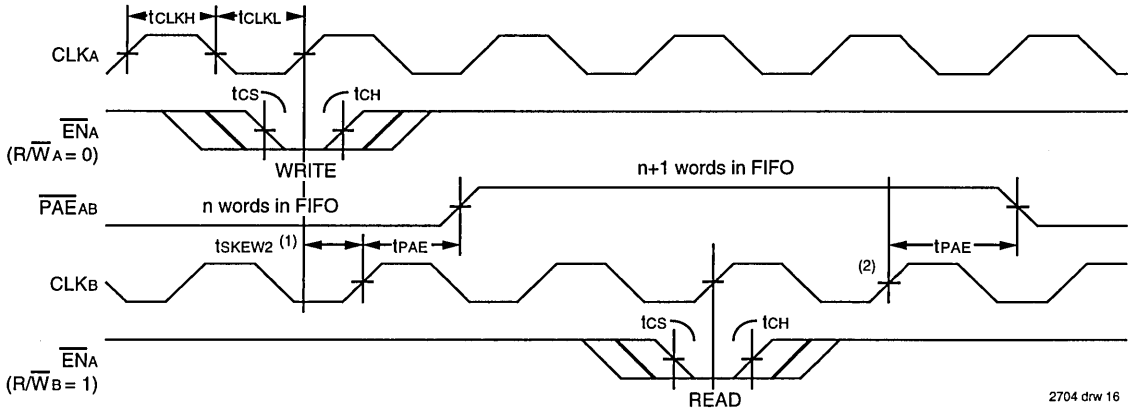
Figure 10. A→B Bypass Timing



2704 drw 15

NOTES:
1. When $\overline{CS}_A$ is brought HIGH, A→B Bypass mode will switch to FIFO mode on the following CLKA going LOW-to-HIGH.
2. After the bypass operation is completed, the $\overline{BYP}_B$ goes from LOW-to-HIGH; this will reset all bypass flags. The bypass path becomes available for the next bypass operation.
3. When A-side changed from bypass mode into FIFO mode, B-side only has one cycle to read the bypass data. On the next cycle, B-side will be forced back to FIFO mode.

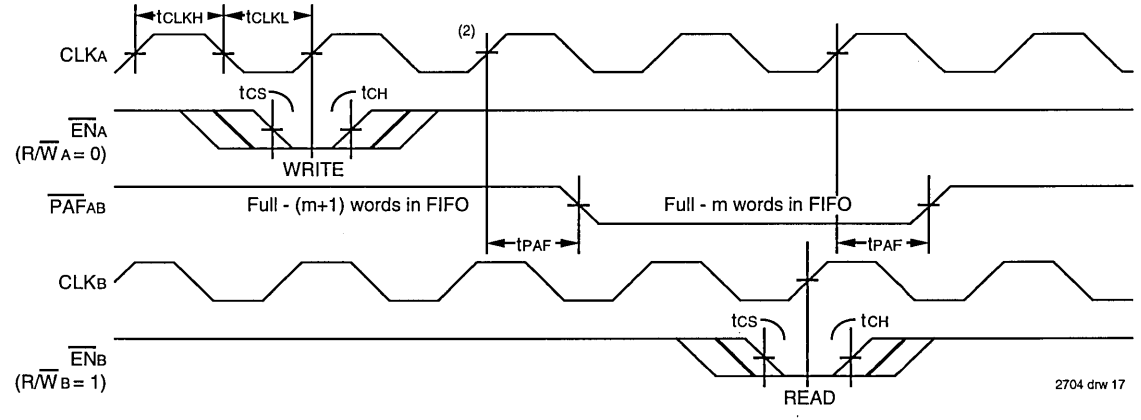
Figure 11. B→A Bypass Timing



NOTES:
1. tSKEW2 the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{PAE}_{AB}$ to change during that clock cycle. If the time between the rising edge of CLKA and the rising edge of CLKB is less than tSKEW, then $\overline{PAE}_{AB}$ may not go HIGH until the next CLKB rising edge.
2. If a read is performed on this rising edge of the read clock, there will be Empty + (n + 1) words in the FIFO when $\overline{PAE}$ goes LOW.

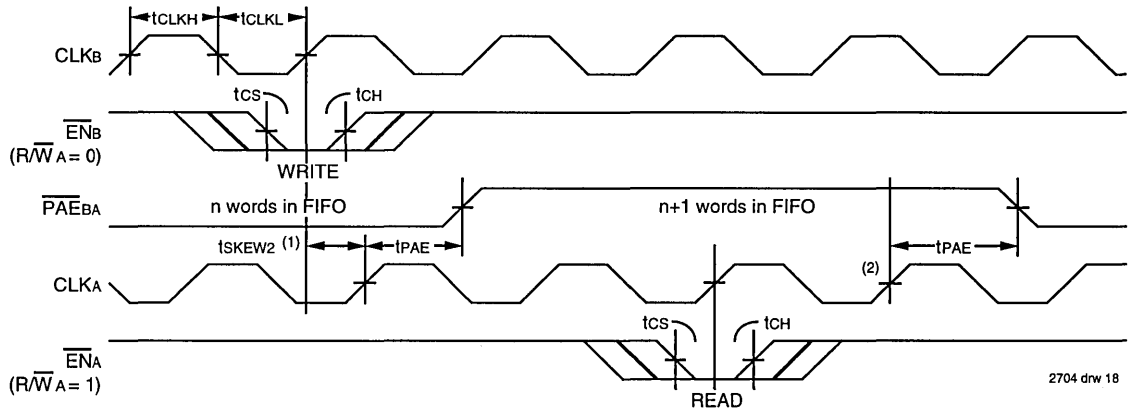
Figure 12. A→B Programmable Almost-Empty Flag Timing

5



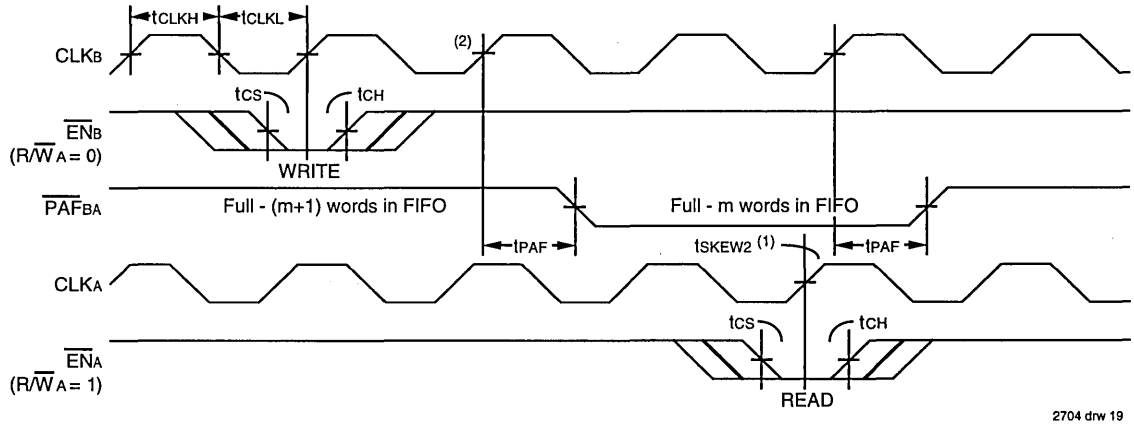
NOTES:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{PAF}_{AB}$ to change during that clock cycle. If the time between the rising edge of CLKB and the rising edge of CLKA is less than tSKEW2, then $\overline{PAF}_{AB}$ may not go HIGH until the next CLKA rising edge.
2. If a write is performed on this rising edge of the write clock, there will be Full - (m + 1) words in the FIFO when $\overline{PAF}$ goes LOW.

Figure 13. A→B Programmable Almost-Full Flag Timing



NOTES:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{PAE}_{BA}$ to change during that clock cycle. If the time between the rising edge of CLKB and the rising edge of CLKA is less than tSKEW2, then $\overline{PAE}_{BA}$ may not go HIGH until the next CLKA rising edge.
2. If a read is performed on this rising edge of the read clock, there will be Empty + (n - 1) words in the FIFO when $\overline{PAE}$ goes LOW.

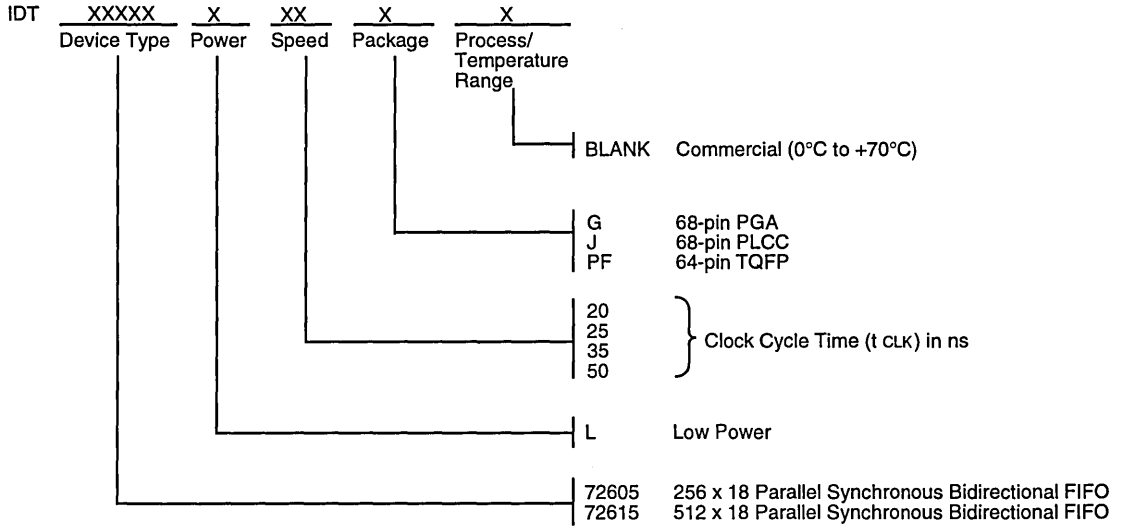
Figure 14. B→A Programmable Almost-Empty Flag Timing



NOTES:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{PAF}_{BA}$ to change during that clock cycle. If the time between the rising edge of CLKB and the rising edge of CLKA is less than tSKEW2, then $\overline{PAF}_{BA}$ may not go HIGH until the next CLKA rising edge.
2. If a write is performed on this rising edge of the write clock, there will be Full - (m + 1) words in the FIFO when $\overline{PAF}$ goes LOW.

Figure 15. B→A Programmable Almost-Full Flag Timing

ORDERING INFORMATION



2704 drw 20

5

Integrated Device Technology, Inc.

BiCMOS SyncBiFIFO™ 64 x 36 x 2

IDT723612

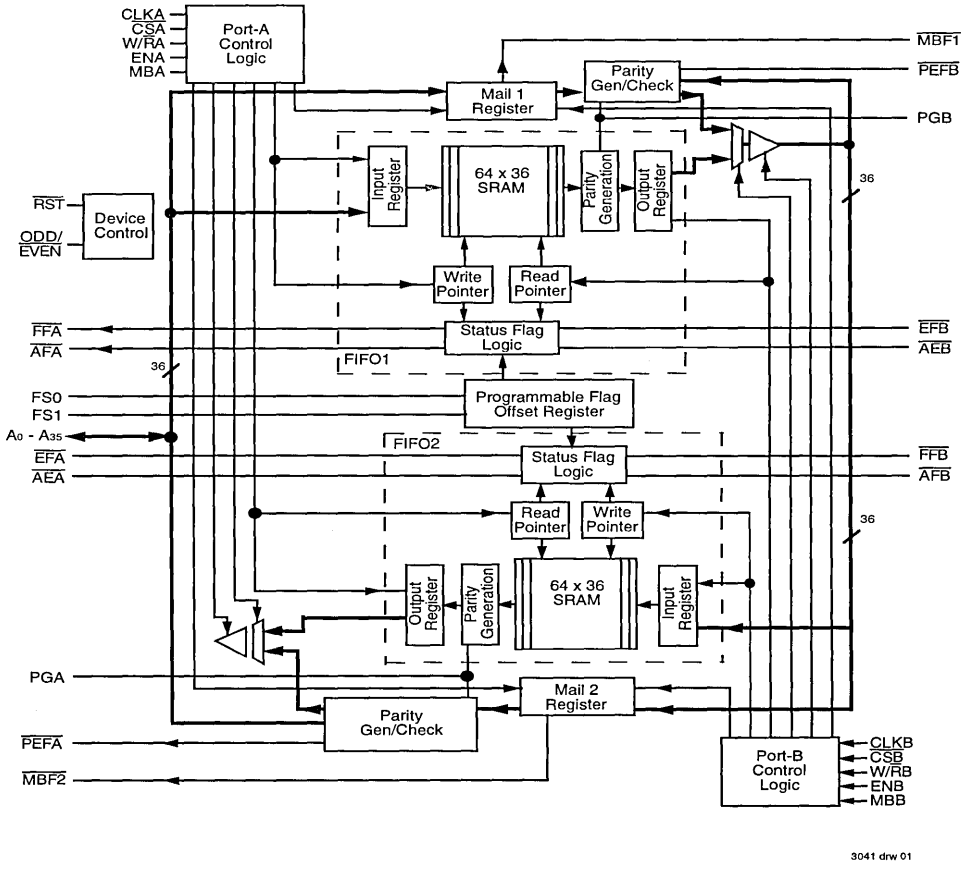
FEATURES:

- Free-running CLKA and CLKB can be asynchronous or coincident (simultaneous reading and writing of data on a single clock edge is permitted)
- Two independent clocked FIFOs (64 x 36 storage capacity each) buffering data in opposite directions
- Mailbox bypass Register for each FIFO
- Programmable Almost-Full and Almost-Empty Flags
- Microprocessor interface control logic
- $\overline{EFA}$, $\overline{FFA}$, $\overline{AEA}$, and $\overline{AFA}$ flags synchronized by CLKA
- $\overline{EFB}$, $\overline{FFB}$, $\overline{AEB}$, and $\overline{AFB}$ flags synchronized by CLKB
- Passive parity checking on each port
- Parity generation can be selected for each port
- Low-power advanced BiCMOS technology
- Supports clock frequencies up to 67 MHz
- Fast access times of 10ns
- Available in 132-pin plastic quad flat package (PQF) or space-saving 120-pin thin quad flat package (TQFP)

DESCRIPTION:

The IDT723612 is a monolithic high-speed, low-power BiCMOS bi-directional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 10ns. Two independent 64 x 36 dual-port SRAM FIFOs

FUNCTIONAL BLOCK DIAGRAM



3041 drw 01

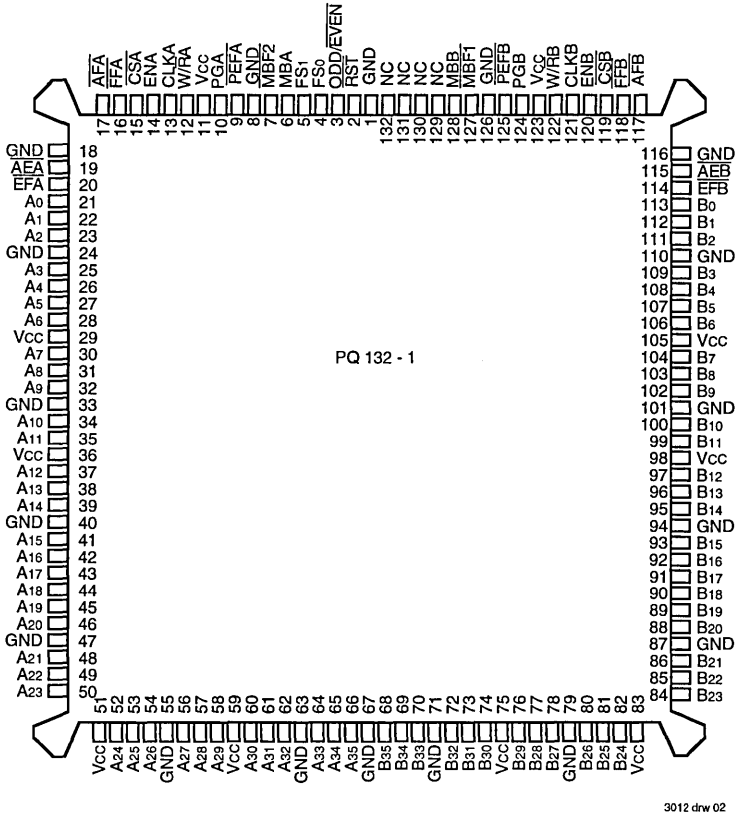
on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost-full and almost-empty) to indicate when a selected number of words is stored in memory. Communication between each port can bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if not desired. Parity generation can be selected for data read from each port. Two or more devices can be used in parallel to create wider data paths.

The IDT723612 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bi-directional interface between microprocessors and/or buses with synchronous control.

The full flag ($\overline{FFA}$, $\overline{FFB}$) and almost-full ($\overline{AFA}$, $\overline{AFB}$) flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The empty flag ($\overline{EFA}$, $\overline{EFB}$) and almost-empty ($\overline{AEA}$, $\overline{AEB}$) flag of a FIFO are two stage synchronized to the port clock that reads data from its array.

The IDT723612 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS

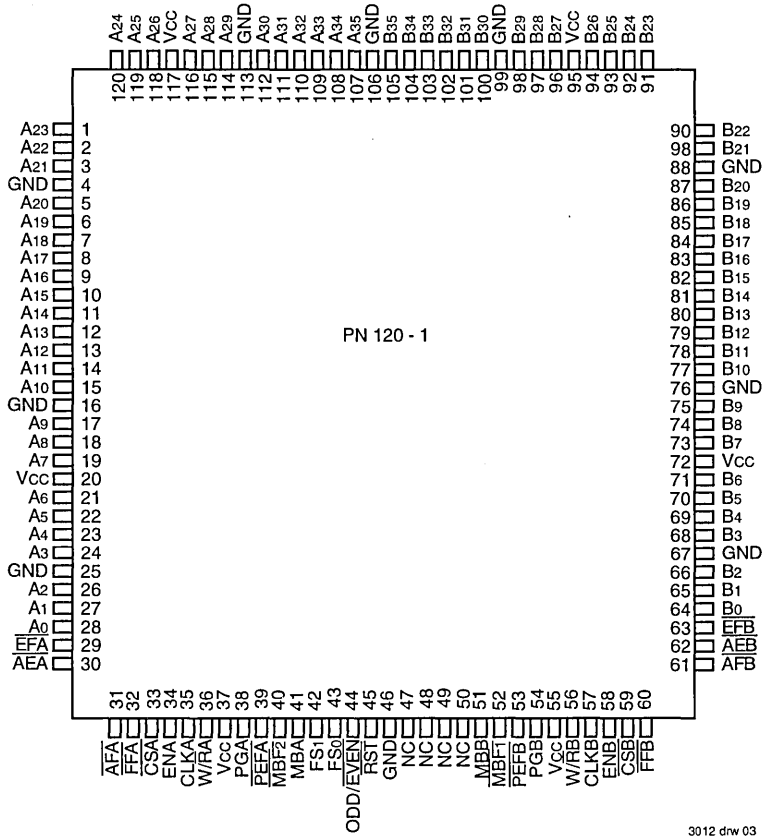


3012 drw 02

PQF PACKAGE
TOP VIEW

Note:
1. NC - No internal connection
2. Uses Yamaichi socket IC51-1324-828

PIN CONFIGURATIONS (CONT.)



3012 drw 03

TQFP
TOP VIEW

Note:
1. NC - No internal connection

PIN DESCRIPTION

Symbol	Name	I/O	Description
A0-A35	Port-A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AEA}$	Almost-Empty Flag	O (Port A)	Programmable almost-empty flag synchronized to CLKA. It is LOW when the number of words in the FIFO2 is less than or equal to the value in the offset register, X.
AEB	Port-B Almost-Empty Flag	O (PortB)	Programmable almost-full flag synchronized to CLKB. It is LOW when the number of words in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFA}$	Port-A Almost-Full Flag	O (Port A)	Programmable almost-full flag synchronized to CLKA. It is LOW when the number of empty locations in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFB}$	Port-B Almost-Empty Flag	O (Port B)	Programmable almost-full flag synchronized to CLKB. It is LOW when the number of empty locations in FIFO2 is less than or equal to the value in the offset register, X.
B0-B35	Port-B Data.	I/O	36-bit bidirectional data port for side B.
CLKA	Port-A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port-A and can be aynchronous or coincident to CLKB. $\overline{EFA}$, $\overline{FFA}$, $\overline{AFA}$, and $\overline{AEA}$ are synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port-B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through port-B and can be asynchronous or coincident to CLKA. $\overline{EFB}$, $\overline{FFB}$, $\overline{AFB}$, and $\overline{AEB}$ are synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port-A Chip Select	I	$\overline{CSA}$ must be LOW to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port-B Chip Select	I	$\overline{B}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EFA}$	Port-A Empty Flag	O (Port A)	$\overline{EFA}$ is synchronized to the LOW-to-HIGH transition of CLKA. When $\overline{EFA}$ is LOW, FIFO2 is empty, and reads from its memory are disabled. Data can be read from FIFO2 to the output register when $\overline{EFA}$ is HIGH. $\overline{EFA}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after data is loaded into empty FIFO2 memory.
$\overline{EFB}$	Port-B Empty Flag	O (Port B)	$\overline{EFB}$ is synchronized to the LOW-to-HIGH transition of CLKB. When $\overline{EFB}$ is LOW, the FIFO1 is empty, and reads from its memory are disabled. Data can be read from FIFO1 to the output register when $\overline{EFB}$ is HIGH. $\overline{EFB}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after data is loaded into empty FIFO1 memory.
ENA	Port-A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A.
ENB	Port-B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B.
$\overline{FFA}$	Port-A Full Flag	O (Port A)	$\overline{FFA}$ is synchronized to the LOW-to-HIGH transition of CLKA. When $\overline{FFA}$ is LOW, FIFO1 is full, and writes to its memory are disabled. $\overline{FFA}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after reset.
$\overline{FFB}$	Port-B Full Flag	O (Port B)	$\overline{FFB}$ is synchronized to the LOW-to-HIGH transition of CLKB. When $\overline{FFB}$ is LOW, FIFO2 is full, and writes to its memory are disabled. $\overline{FFB}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after reset.
FS1, FS0	Flag-Offset Selects	I	The LOW-to-HIGH transition of $\overline{RST}$ latches the values of FS0 and FS1, which selects one of four preset values for the almost-full flag and almost-empty flag.
MBA	Port-A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a port-A read or write operation. When the A0-A35 outputs are active, a HIGH level on MBA selects data from the mail2 register for output, and a LOW level selects FIFO2 output register data for output.

5

PIN DESCRIPTION (CONTINUED)

SYMBOL	NAME	I/O	DESCRIPTION
MBB	Port-B Mailbox Select	I	A HIGH level on MBB chooses a mailbox register for a port-B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register for output, and a LOW level selects FIFO1 output register data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is set LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a port-B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH when the device is reset.
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is set LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a port-A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH when the device is reset.
ODD/$\overline{EVEN}$	Odd/Even Parity Select	I	Odd parity is checked on each port when ODD/$\overline{EVEN}$ is HIGH, and even parity is checked when ODD/$\overline{EVEN}$ is LOW. ODD/$\overline{EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for a read operation.
$\overline{PEFA}$	Port-A Parity Error Flag	O (Port A)	When any byte applied to terminals A0-A35 fails parity, $\overline{PEFA}$ is LOW. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the A0-A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is setup by having W/$\overline{RA}$ LOW, MBA HIGH, and PGA HIGH, the $\overline{PEFA}$ flag is forcedHIGH regardless of the A0-A35 inputs.
$\overline{PEFB}$	Port-B Parity Error Flag	O (Port B)	When any byte applied to terminals B0-B35 fails parity, $\overline{PEFB}$ is LOW. Bytes are organized as B0-B8, B9-B17, B18-B26, B27-B35 with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the B0-B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having W/$\overline{RB}$ LOW, MBB HIGH, and PGB HIGH, the $\overline{PEFB}$ flag is forced HIGH regardless of the state of the B0-B35 inputs.
PGA	Port-A Parity	I	Parity is generated for data reads from port A when PGA is HIGH. Generation The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35. The generated parity bits are output in the most significant bit of each byte.
PGB	Port-B Parity Generation	I	Parity is generated for data reads from port B when PGB s HIGH. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as B0-B8, B9-B17, B18-B26, and B27-B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{RST}$	Reset	I	To reset the device, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST}$ is LOW. This sets the $\overline{AFA}$, $\overline{AFB}$, $\overline{MBF1}$, and $\overline{MBF2}$ flags HIGH and the $\overline{EFA}$, $\overline{EFB}$, $\overline{AEA}$, $\overline{AEB}$, $\overline{FFA}$, and $\overline{FFB}$ flags LOW. The LOW-to-HIGH transition of $\overline{RST}$ latches the status of the FS1 and FS0 inouts to select almost-full and almost-empty flag offset.
W/$\overline{RA}$	Port-A Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the high-impedance state when W/$\overline{RA}$ is HIGH.
W/$\overline{RB}$	Port-B Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the high-impedance state when W/$\overline{RB}$ is HIGH.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)(2)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	-0.5 to 7	V
V_I(2)	Input Voltage Range	-0.5 to Vcc+0.5	V
V_O(2)	Output Voltage Range	-0.5 to Vcc+0.5	V
I_{IK}	Input Clamp Current, (V_I < 0 or V_I > Vcc)	±20	mA
I_{OK}	Output Clamp Current, (V_O < 0 or V_O > Vcc)	±50	mA
I_{OUT}	Continuous Output Current, (V_O = 0 to Vcc)	±50	mA
I_{CC}	Continuous Current Through Vcc or GND	±500	mA
T_A	Operating Free Air Temperature Range	0 to 70	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C

Notes:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

5

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply Voltage	4.5	5.5	V
VIH	HIGH Level Input Voltage	2	–	V
VIL	LOW-Level Input Voltage	–	0.8	V
IOH	HIGH-Level Output Current	–	-4	mA
IOL	LOW-Level Output Current	–	8	mA
TA	Operating Free-air Temperature	0	70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Parameter	Test Conditions			Min. Typ.(1) Max.	Unit
V_{OH}	Vcc = 4.5V,	I_{OH} = -4 mA		2.4	V
V_{OL}	Vcc = 4.5 V,	I_{OL} = 8 mA		0.5	V
I_{LI}	Vcc = 5.5 V,	V_I = Vcc or 0		±50	µA
I_{LO}	Vcc = 5.5 V,	V_O = Vcc or 0		±50	µA
I_{CC}	Vcc = 5.5 V,	I_O = 0 mA, V_I = Vcc or GND	Outputs HIGH	60	mA
			Outputs LOW	130	mA
			Outputs Disabled	60	mA
C_{IN}	V_I = 0,	f = 1 MHz		4	pF
C_{OUT}	V_O = 0,	f = 1 MHZ		8	pF

Note:
1. All typical values are at Vcc = 5 V, T_A = 25°C.

DC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

Symbol	Parameter	IDT723612L15		IDT723612L20		IDT723612L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Clock Frequency, CLKA or CLKB	–	66.7	–	50	–	33.4	MHz
t_{CLK}	Clock Cycle Time, CLKA or CLKB	15	–	20	–	30	–	ns
t_{CLKH}	Pulse Duration, CLKA and CLKB HIGH	6	–	8	–	12	–	ns
t_{CLKL}	Pulse Duration, CLKA and CLKB LOW	6	–	8	–	12	–	ns
t_{DS}	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	4	–	5	–	6	–	ns
t_{ENS1}	Setup Time, $\overline{CSA}$, W/$\overline{RA}$ before CLKA↑; $\overline{CSB}$, W/$\overline{RB}$ before CLKB↑	6	–	6	–	7	–	ns
t_{ENS2}	Setup Time, ENA, before CLKA↑; ENB before CLKB↑	4	–	5	–	6	–	ns
t_{ENS3}	Setup Time, MBA before CLKA↑: MBB before CLKB↑	4	–	5	–	6	–	ns
t_{PGS}	Setup Time, ODD/$\overline{EVEN}$ and PGA before CLKA↑; ODD/$\overline{EVEN}$ and PGB before CLKB↑[1]	4	–	5	–	6	–	ns
t_{RSTS}	Setup Time, $\overline{RST}$ LOW before CLKA↑ or CLKB↑[2]	5	–	6	–	7	–	ns
t_{FSS}	Setup Time, FS0/FS1 before $\overline{RST}$ HIGH	5	–	6	–	7	–	ns
t_{DH}	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	2.5	–	2.5	–	2.5	–	ns
t_{ENH1}	Hold Time, $\overline{CSA}$ W/$\overline{RA}$ after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$ after CLKB↑	2	–	2	–	2	–	ns
t_{ENH2}	Hold Time, ENA, after CLKA↑; ENB after CLKB↑	2.5	–	2.5	–	2.5	–	ns
t_{ENH3}	Hold Time, MBA after CLKA↑; MBB after CLKB↑	1	–	1	–	1	–	ns
t_{PGH}	Hold Time, ODD/$\overline{EVEN}$ and PGA after CLKA↑; ODD/$\overline{EVEN}$ and PGB after CLKB↑[1]	1	–	1	–	1	–	ns
t_{RSTH}	Hold Time, $\overline{RST}$ LOW after CLKA↑ or CLKB↑[2]	5	–	6	–	7	–	ns
t_{FSH}	Hold Time, FS0 and FS1 after $\overline{RST}$ HIGH	4	–	4	–	4	–	ns
t_{SKEW1}[3]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{EFA}$, $\overline{EFB}$, $\overline{FFA}$, and $\overline{FFB}$	8	–	8	–	10	–	ns
t_{SKEW2}[3]	Skew Time, between CLKA↑ and CLKB↑ For $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	9	–	16	–	20	–	ns

Notes:
1. Only applies for a clock edge that does a FIFO read.
2. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
3. Skew time is not a timimg constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 30pF

Symbol	Parameter	IDT723612L15		IDT723612L20		IDT723612L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_A	Access Time, CLKA↑ to A0-A35 and CLKB↑ to B0-B35	2	10	2	12	2	15	ns
t_{WFF}	Propagation Delay Time, CLKA↑ to $\overline{FFA}$ and CLKB↑ to $\overline{FFB}$	2	10	2	12	2	15	ns
t_{REF}	Propagation Delay Time, CLKA↑ to $\overline{EFA}$ and and CLKB↑ to $\overline{EFB}$	2	10	2	12	2	15	ns
t_{PAE}	Propagation Delay Time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	2	10	2	12	2	15	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	2	10	2	12	2	15	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	1	9	1	12	1	15	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to B0-B35[1] and CLKB↑ to A0-A35[2]	3	11	3	13	3	15	ns
t_{MDV}	Propagation Delay Time, MBA to A0-A35 valid and MBB to B0-B35 valid	1	11	1	11.5	1	12	ns
t_{PDPE}	Propagation Delay Time, A0-A35 valid to $\overline{PEFA}$ valid; B0-B35 valid to $\overline{PEFB}$ valid	3	10	3	11	3	13	ns
t_{POPE}	Propagation Delay Time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	3	11	3	12	3	14	ns
t_{POPB}[3]	Propagation Delay Time, ODD/$\overline{EVEN}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	11	2	12	2	14	ns
t_{PEPE}	Propagation Delay Time, W/$\overline{RA}$, $\overline{CSA}$, ENA, MBA or PGA to $\overline{PEFA}$; W/$\overline{RB}$, $\overline{CSB}$, ENB. MBB, PGB to $\overline{PEFB}$	1	11	1	12	1	14	ns
t_{PEPB}[3]	Propagation Delay Time, W/$\overline{RA}$, $\overline{CSA}$, ENA, MBA or PGA to parity bits (A8, A17, A26, A35); W/$\overline{RB}$, $\overline{CSB}$, ENB. MBB or PGB to parity bits (B8, B17, B26, B35)	3	12	3	13	3	14	ns
t_{RSF}	Propagation Delay Time, $\overline{RST}$ to ($\overline{AEA}$, $\overline{AEB}$) LOW and ($\overline{AFA}$, $\overline{AFB}$, $\overline{MBF1}$, $\overline{MBF2}$) HIGH	1	15	1	20	1	30	ns
t_{EN}	Enable Time, $\overline{CSA}$ and W/$\overline{RA}$ LOW to A0-A35 active and $\overline{CSB}$ LOW and W/$\overline{RB}$ HIGH to B0-B35 active	2	10	2	12	2	14	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{RA}$ HIGH to A0-A35 at high impedance and $\overline{CSB}$ HIGH or W/$\overline{RB}$ LOW to B0-B35 at high impedance	1	8	1	9	1	11	ns

Notes:
1. Writing data to the mail1 register when the B0-B35 outputs are active and MBB is HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.
3. Only applies when reading data from a mail register.

5

SIGNAL DESCRIPTIONS

RESET

The IDT723612 is reset by taking the reset ($\overline{RST}$) input LOW for at least four port-A clock (CLKA) and four port-B clock (CLKB) LOW-to-HIGH transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of each FIFO and forces the full flags ($\overline{FFA}$, $\overline{FFB}$) LOW, the empty flags ($\overline{EFA}$, $\overline{EFB}$) LOW, the almost-empty flags ($\overline{AEA}$, $\overline{AEB}$) LOW and the almost-full flags ($\overline{AFA}$, $\overline{AFB}$) HIGH. A reset also forces the mailbox flags ($\overline{MBF1}$, $\overline{MBF2}$) HIGH. After a reset, $\overline{FFA}$ is set HIGH after two LOW-to-HIGH transitions of CLKA and $\overline{FFB}$ is set HIGH after two LOW-to-HIGH transitions of CLKB. The device must be reset after power up before data is written to its memory.

FS1	FS0	$\overline{RST}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

Table 1. Flag Programming

A LOW-to-HIGH transition on the $\overline{RST}$ input loads the almost-full and almost-empty registers (X) with the values selected by the flag-select (FS0, FS1) inputs. The values that can be loaded into the registers are shown in Table 1.

FIFO WRITE/READ OPERATION

The state of port-A data A0-A35 outputs is controlled by the port-A chip select ($\overline{CSA}$) and the port-A write/read select (W/$\overline{RA}$). The A0-A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW.

Data is loaded into FIFO1 from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH, MBA is LOW, and $\overline{FFA}$ is HIGH. Data is read from FIFO2 to the A0-A35 outputs by a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is LOW, ENA is HIGH, MBA is LOW, and $\overline{EFA}$ is HIGH (see Table 2).

The port-B control signals are identical to those of port A. The state of the port-B data (B0-B35) outputs is controlled by the port-B chip select ($\overline{CSB}$) and the port-B write/read select (W/$\overline{RB}$). The B0-B35 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is HIGH. The B0-B35 outputs are active when both $\overline{CSB}$ and W/$\overline{RB}$ are LOW.

Data is loaded into FIFO2 from the B0-B35 inputs on a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, W/$\overline{RB}$ is HIGH, ENB is HIGH, MBB is LOW, and $\overline{FFB}$ is HIGH. Data is read from FIFO1 to the B0-B35 outputs by a LOW-to-HIGH

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0-A35 Outputs	Port Functions
H	X	X	X	X	In High-Impedance State	None
L	H	L	X	X	In High-Impedance State	None
L	H	H	L	↑	In High-Impedance State	FIFO1 Write
L	H	H	H	↑	In High-Impedance State	Mail1 Write
L	L	L	L	X	Active, FIFO2 Output Register	None
L	L	H	L	↑	Active, FIFO2 Output Register	FIFO2 Read
L	L	L	H	X	Active, Mail2 Register	None
L	L	H	H	↑	Active, Mail2 Register	Mail2 Read (Set $\overline{MBF2}$ HIGH)

Table 2. Port-A Enable Function Table

$\overline{CSB}$	W/$\overline{RB}$	ENB	MBB	CLKB	B0-B35 Outputs	Port Functions
H	X	X	X	X	In High-Impedance State	None
L	H	L	X	X	In High-Impedance State	None
L	H	H	L	↑	In High-Impedance State	FIFO2 Write
L	H	H	H	↑	In High-Impedance State	Mail2 Write
L	L	L	L	X	Active, FIFO1 Output Register	None
L	L	H	L	↑	Active, FIFO1 Output Register	FIFO1 read
L	L	L	H	X	Active, Mail1 Register	None
L	L	H	H	↑	Active, Mail1 Register	Mail1 Read (Set $\overline{MBF1}$ HIGH)

Table 3. Port-B Enable Function Table

transition of CLKB when $\overline{CSB}$ is LOW, W/$\overline{RB}$ is LOW, ENB is HIGH, MBB is LOW, and $\overline{EFB}$ is HIGH (see Table 3).

The setup and hold time constraints to the port clocks for the port chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{RA}$, W/$\overline{RB}$) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port chip select and write/read select may change states during the setup and hold time window of the cycle.

SYNCHRONIZED FIFO FLAGS

Each FIFO is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on the output when CLKA and CLKB operate asynchronously to one another. $\overline{EFA}$, $\overline{AEA}$, $\overline{FFA}$, and $\overline{AFA}$ are synchronized by CLKA. $\overline{EFB}$, $\overline{AEB}$, $\overline{FFB}$, and $\overline{AFB}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

EMPTY FLAGS ($\overline{EFA}$, $\overline{EFB}$)

The empty flag of a FIFO is synchronized to the port clock that reads data from its array. When the empty flag is HIGH, new data can be read to the FIFO output register. When the empty flag is LOW, the FIFO is empty and attempted FIFO reads are ignored.

The read pointer of a FIFO is incremented each time a new word is clocked to the output register. The state machine that controls an empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to a FIFO can be read to the FIFO output register in a minimum of three cycles of the empty flag synchronizing clock. Therefore, an empty flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The empty flag of the FIFO is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock, and the new data word can be read to the FIFO output register in the following cycle.

A LOW-to-HIGH transition on an empty flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle.

FULL FLAG ($\overline{FFA}$, $\overline{FFB}$)

The full flag of a FIFO is synchronized to the port clock that writes data to its array. When the full flag is HIGH, a memory location is free in the SRAM to receive new data. No memory locations are free when the full flag is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, the write pointer is incremented. The state machine that controls a full flag monitors a write-pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full-1, or full-2. From the time a word is read from a FIFO, the previous memory location is ready to be written in a minimum of three cycles of the full flag synchronizing clock. Therefore, a full flag is LOW if less than two cycles of the full flag synchronizing clock have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the full flag synchronization clock after the read sets the full flag HIGH and the data can be written in the following clock cycle.

A LOW-to-HIGH transition on a full flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle.

ALMOST EMPTY FLAGS ($\overline{AEA}$, $\overline{AEB}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an almost-empty flag monitors a write-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see Reset above). An almost-empty flag is LOW when the FIFO contains

Number of Words in the FIFO1[1]	Synchronized to CLKB		Synchronized to CLKA	
	$\overline{EFB}$	$\overline{AEB}$	$\overline{AFA}$	$\overline{FFA}$
0	L	L	H	H
1 to X	H	L	H	H
(X+1) to [64-(X+1)]	H	H	H	H
(64-X) to 63	H	H	L	H
64	H	H	L	L

Table 4. FIFO1 Flag Operation

Number of Words in the FIFO[1]	Synchronized to CLKB		Synchronized to CLKA	
	$\overline{EFA}$	$\overline{AEA}$	$\overline{AFB}$	$\overline{FFB}$
0	L	L	H	H
1 to X	H	L	H	H
(X+1) to [64-(X+1)]	H	H	H	H
(64-X) to 63	H	H	L	H
64	H	H	L	L

Table 5. FIFO2 Flag Operation

Note:
1. X is the value in the almost-empty flag and almost-full flag offset register.

X or less words in memory and is HIGH when the FIFO contains (X+1) or more words.

Two LOW-to-HIGH transitions of the almost-empty flag synchronizing clocks are required after a FIFO write for the almost-empty flag to reflect the new level of fill. Therefore, the almost-empty flag of a FIFO containing (X+1) or more words remains LOW if two cycles of the synchronizing clock have not elapsed since the write that filled the memory to the (X+1) level. An almost-empty flag is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of an almost-empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figure 6 and 7).

ALMOST FULL FLAGS ($\overline{AFA}$, $\overline{AFB}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full-1, or almost full-2. The almost-full state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see Reset above). An almost-full flag is LOW when the FIFO contains (64-X) or more words in memory and is HIGH when the FIFO contains [64-(X+1)] or less words.

Two LOW-to-HIGH transitions of the almost-full flag synchronizing clock are required after a FIFO read for the almost-full flag to reflect the new level of fill. Therefore, the almost-full flag of a FIFO containing [64-(X+1)]or less words remains LOW if two cycles of the synchronizing clock have not elapsed since the read that reduced the number of words in memory to [64-(X+1)]. An almost-full flag is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock after the FIFO read that reduces the number of words in memory to [64-(X+1)]. A second LOW-to-HIGH transition of an almost-full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [64-(X+1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figure 13 and 14).

MAILBOX REGISTERS

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A LOW-to-HIGH transition on CLKA writes A0-A35 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and MBA HIGH. A LOW-to-HIGH transition on CLKB writes B0-B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and MBB is HIGH. Writing data to a mail register sets the corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while the mail flag is LOW.

When a port's data outputs are active, the data on the bus comes from the FIFO output register when the port mailbox-select input (MBA, MBB) is LOW and from the mail register when the port mailbox-select input is HIGH. The mail1 register flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a port-B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and MBB is HIGH. The mail2 register flag ($\overline{MBF2}$) is set HIGH by a LOW-to-HIGH transition on CLKA when port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and MBA is HIGH. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

PARITY CHECKING

The port-A inputs (A0-A35) and port-B inputs (B0-B35) each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the input bus is reported by a LOW level on the port parity error flag ($\overline{PEFA}$, $\overline{PEFB}$). Odd or even parity checking can be selected, and the parity error flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/EVEN) select input. A parity error on one or more bytes of a port is reported by a LOW level on the corresponding port parity error flag ($\overline{PEFA}$, $\overline{PEFB}$) output. Port-A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35 with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, with the most significant bit of each byte used as the parity bit. When odd/even parity is selected, a port parity error flag ($\overline{PEFA}$, $\overline{PEFB}$) is LOW if any byte on the port has an odd/even number of LOW levels applied to the bits.

The four parity trees used to check the A0-A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = HIGH). When a port-A read from the mail2 register with parity generation is selected with W/$\overline{RA}$ LOW, $\overline{CSA}$ LOW, ENA HIGH, MBA HIGH, and PGA HIGH, the port-A parity error flag ($\overline{PEFA}$) is held HIGH regardless of the levels applied to the A0-A35 inputs. Likewise, the parity trees used to check the B0-B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB = HIGH). When a port-B read from the mail1 register with parity generation is selected with W/$\overline{RB}$ LOW, $\overline{CSB}$ LOW, ENB HIGH, MBB HIGH, and PGB HIGH, the port-B parity error flag ($\overline{PEFB}$) is held HIGH regardless of the levels applied to the B0-B35 inputs.

PARITY GENERATION

A HIGH level on the port-A parity generate select (PGA) or port-B parity generate select (PGB) enables the IDT723612 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0-A8, A9-A17, A18-26, and A27-A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all thirty-six inputs regardless of the state of the parity generate select (PGA, PGB)

inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{\text{EVEN}}$ select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port-A parity generate select (PGA) and odd/even parity select (ODD/$\overline{\text{EVEN}}$) have setup and hold time constraints to the port-A clock (CLKA) and the port-B parity generate select (PGB) and ODD/$\overline{\text{EVEN}}$ have setup and hold-time constraints to the port-B clock (CLKB). These timing constraints only apply for a rising clock edge used to read a new word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0-B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0-A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port write/read select (W/$\overline{\text{R}}$A, W/$\overline{\text{R}}$B) input is LOW, the port mail select (MBA, MBB) input is HIGH, chip select ($\overline{\text{CSA}}$, $\overline{\text{CSB}}$) is LOW, enable (ENA, ENB) is HIGH, and port parity generate select (PGA, PGB) is HIGH. Generating parity for mail register data does not change the contents of the register.

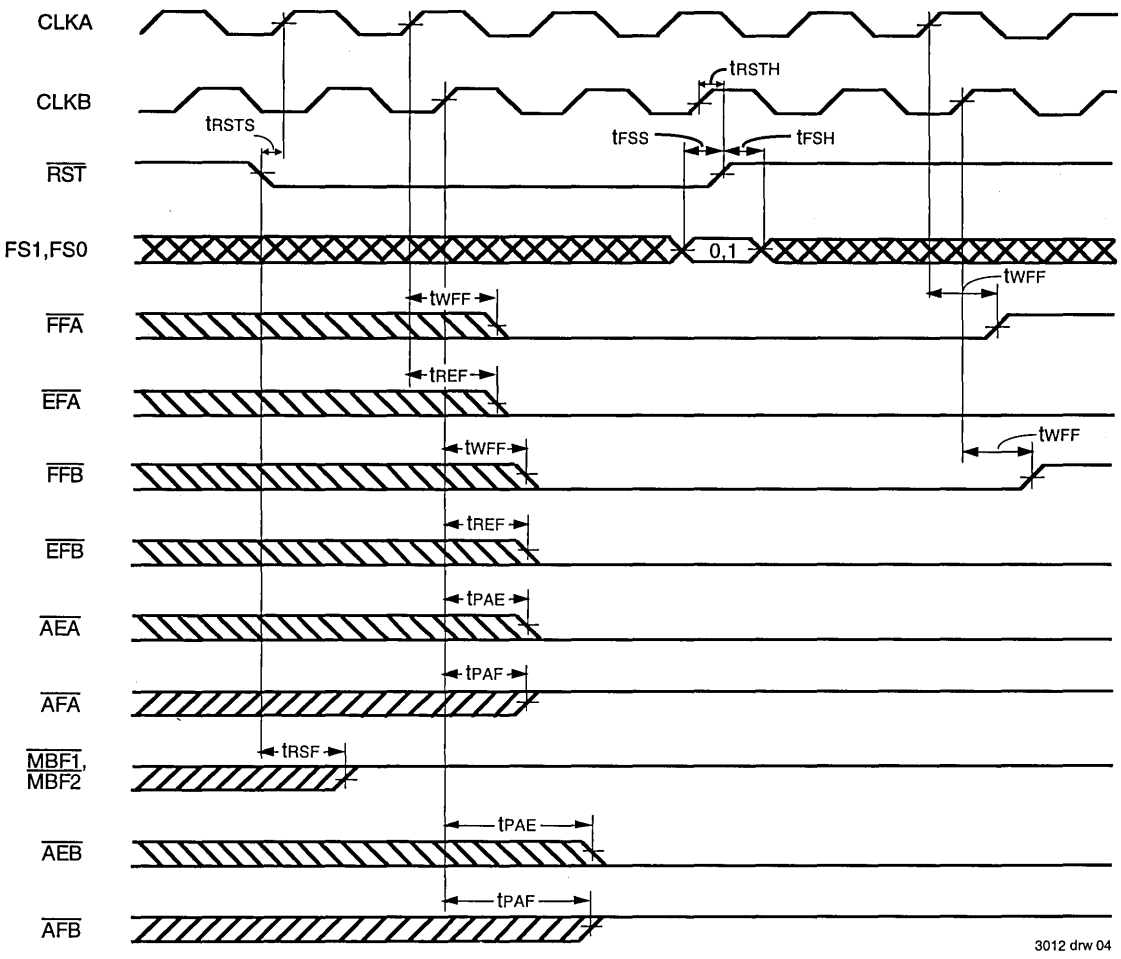
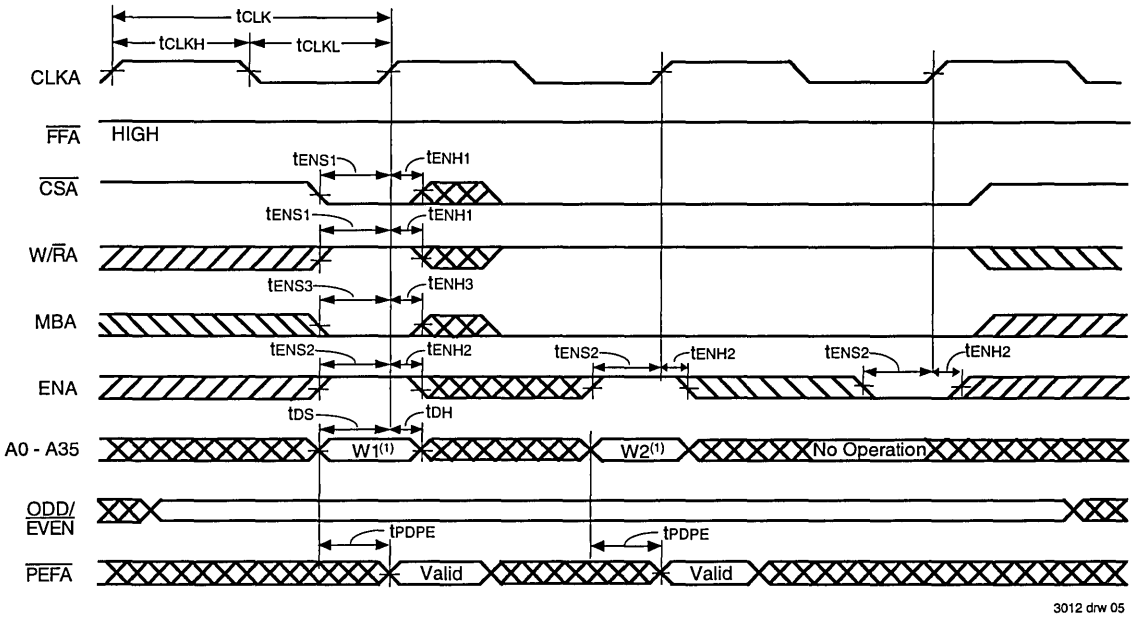


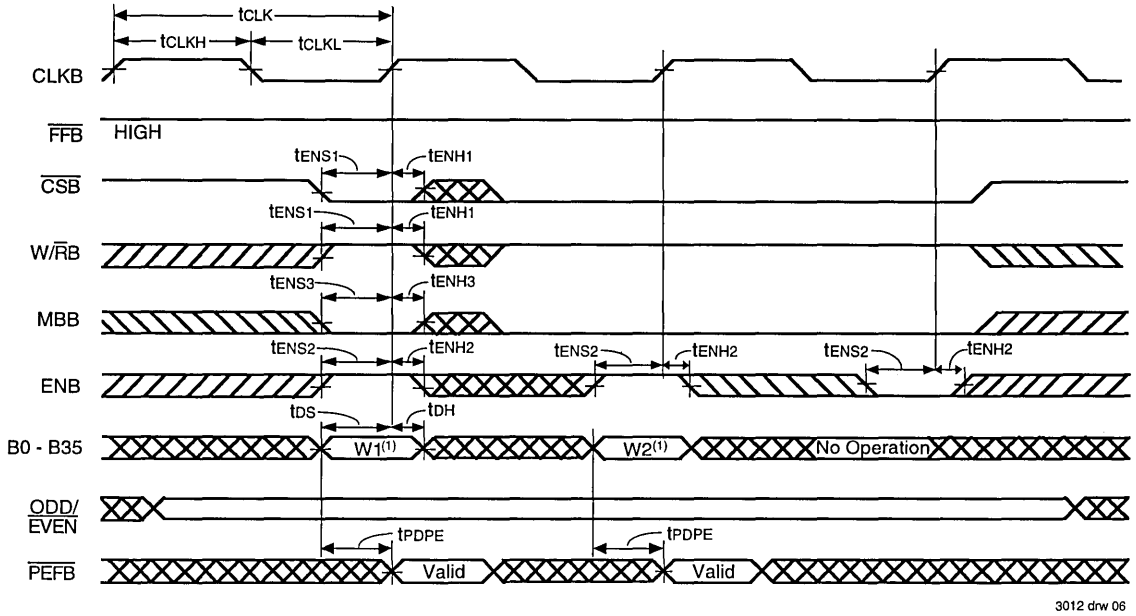
Figure 1. Device Reset Loading the X Register with the Value of Eight



Note:
1. Written to FIFO1

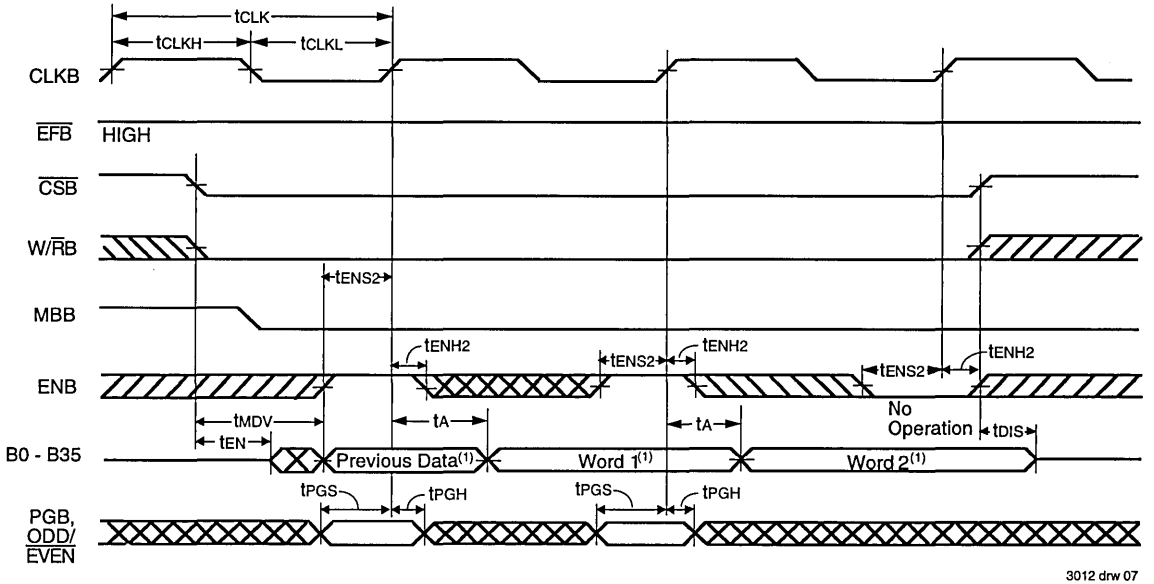
Figure 2. Port-A Write Cycle Timing for FIFO1

5



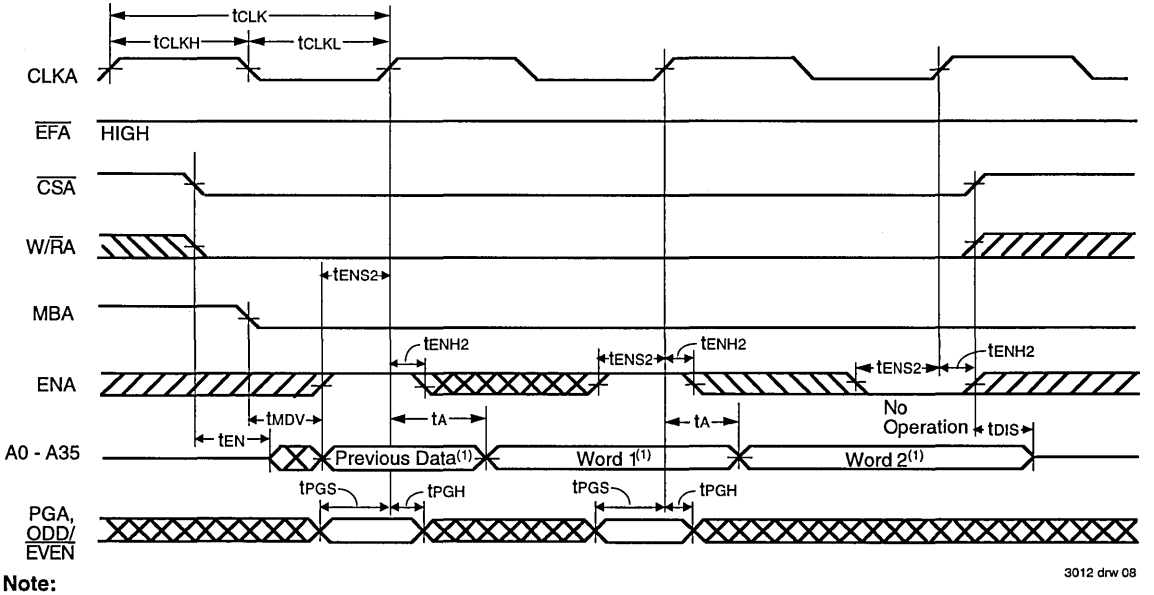
Note:
1. Written to FIFO2

Figure 3. Port-B Write Cycle Timing for FIFO2



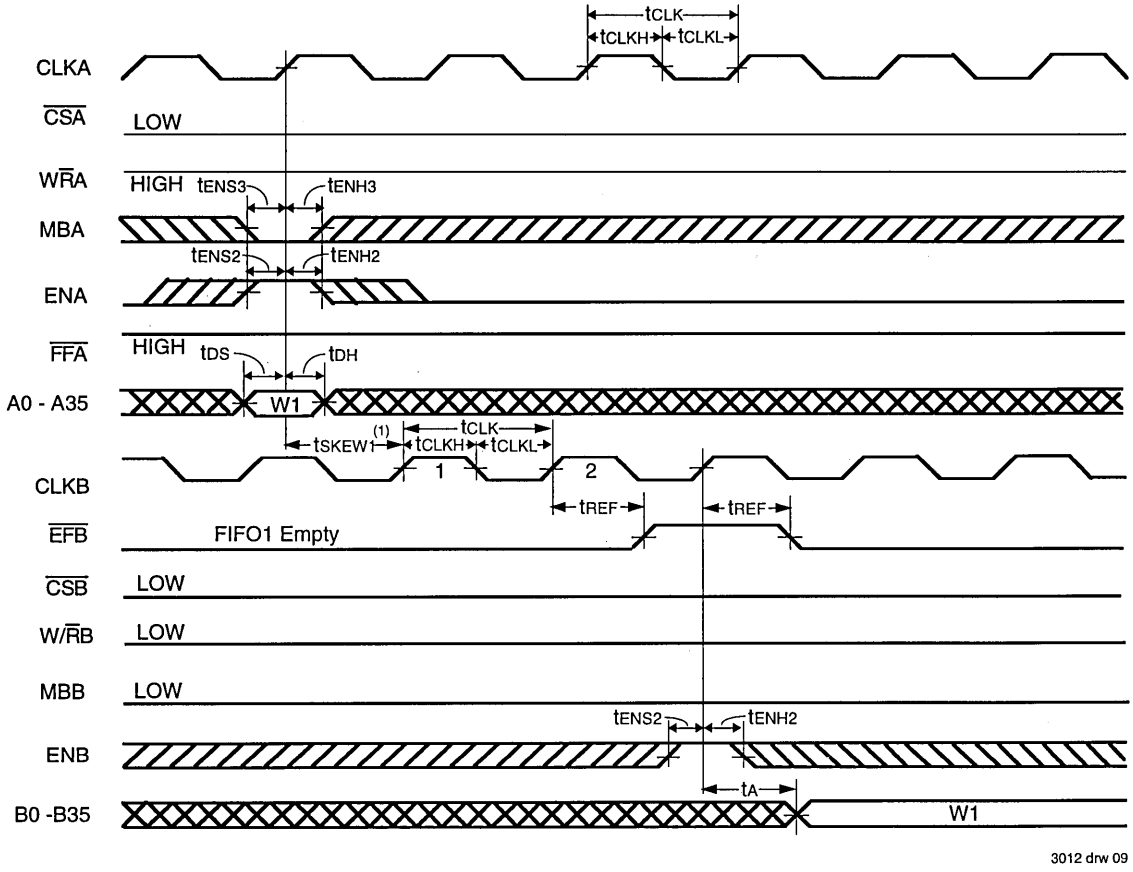
Note:
1. Read from FIFO1

Figure 4. Port-B Read Cycle Timing for FIFO1



Note:
1. Read from FIFO2

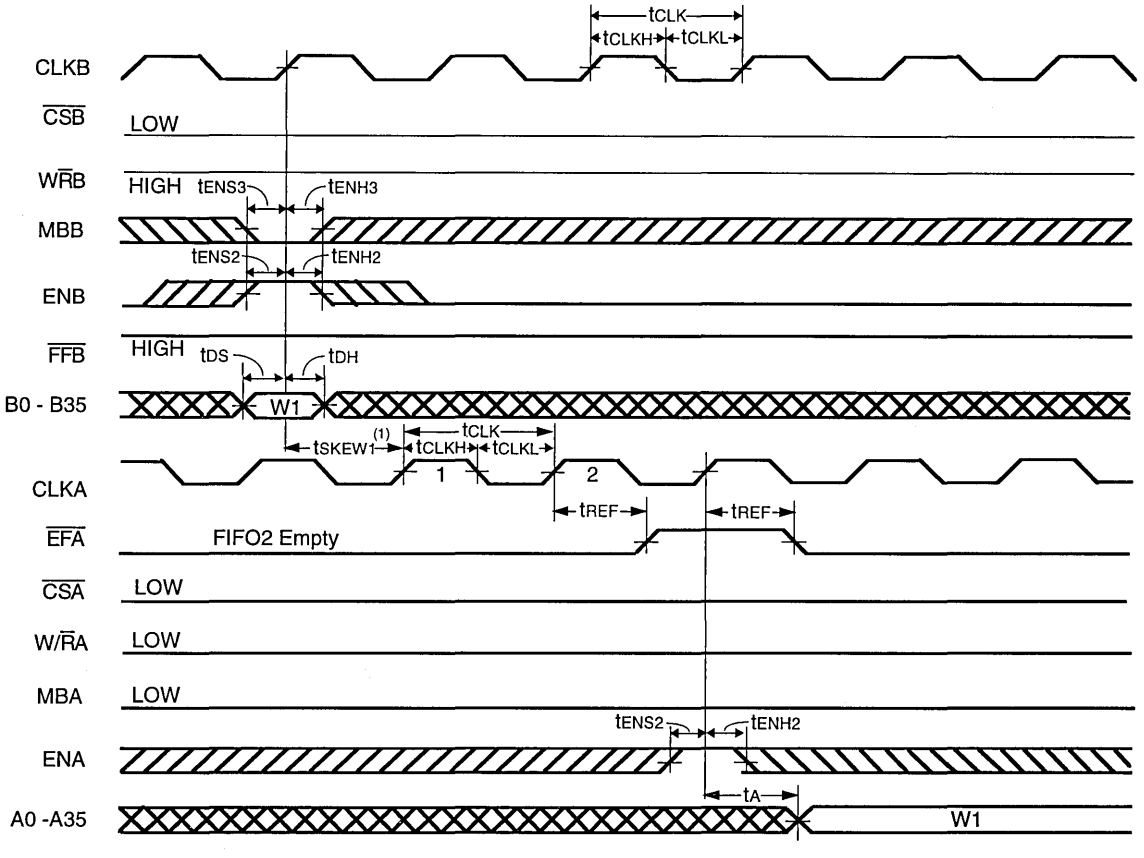
Figure 5. Port-A Read Cycle Timing for FIFO2



Note:

1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of $\overline{EFB}$ HIGH may occur one CLKB cycle later than shown.

Figure 6. $\overline{EFB}$ Flag Timing and First Data Read when FIFO1 is Empty

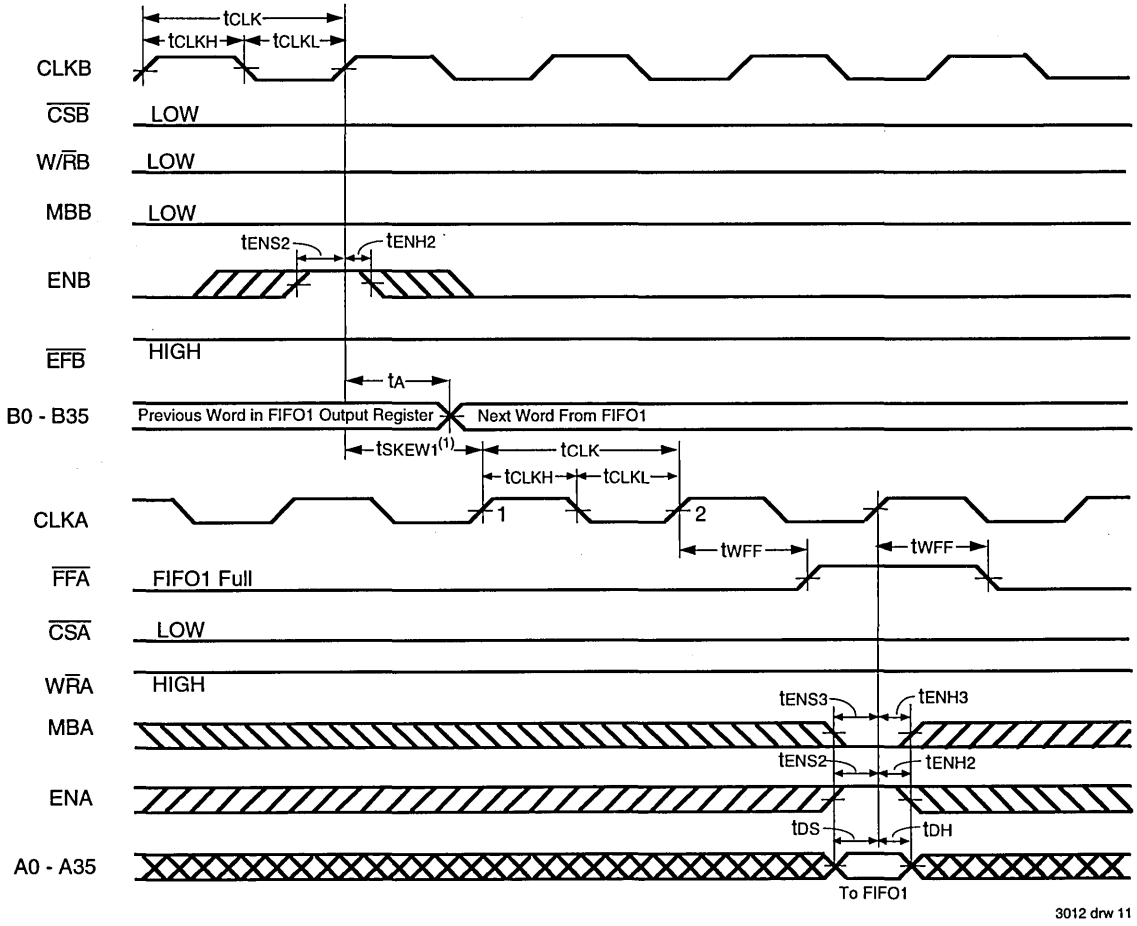


3012 drw 10

Note:

1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{EFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of $\overline{EFA}$ HIGH may occur one CLKA cycle later than shown.

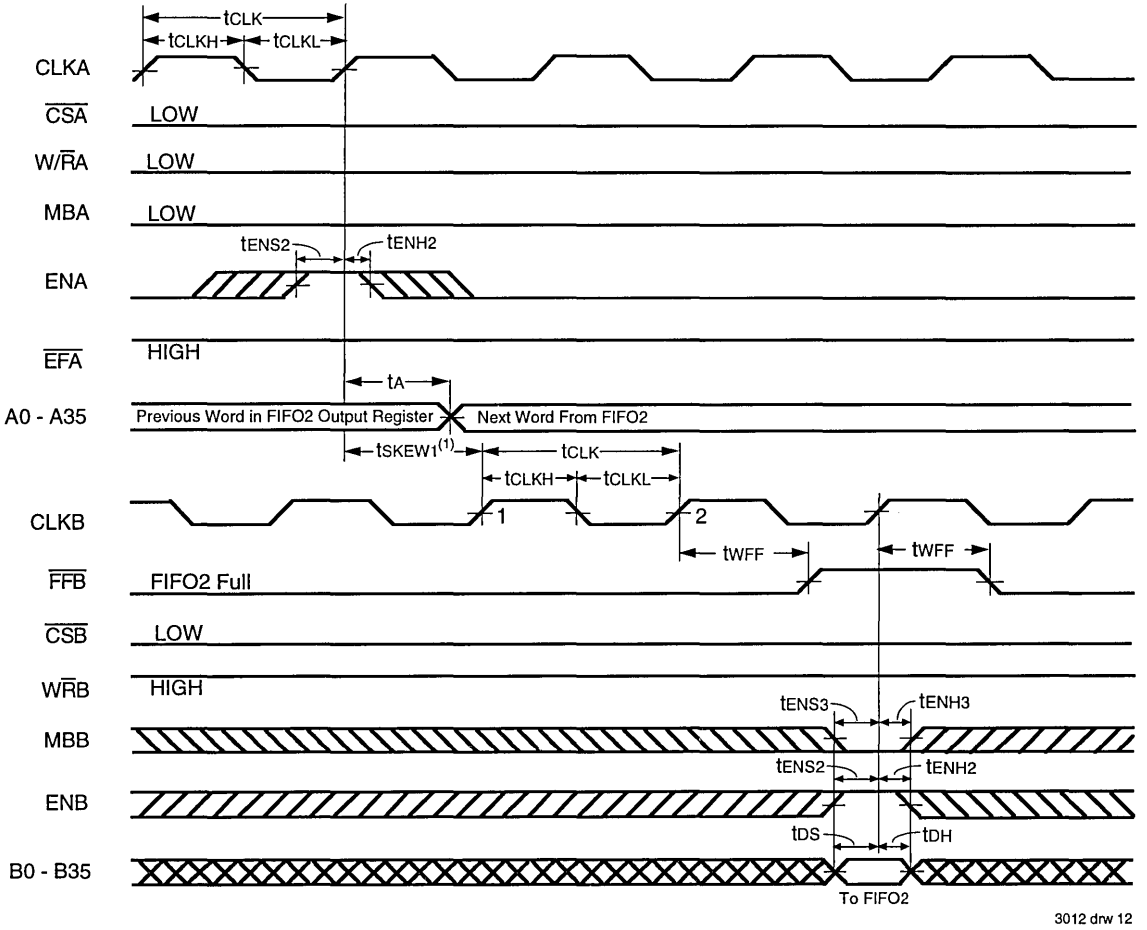
Figure 7. $\overline{EFA}$ Flag Timing and First Data Read when FIFO2 is Empty



Note:

1. tSKEW1 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW1, then $\overline{FFA}$ may transition HIGH one CLKA cycle later than shown.

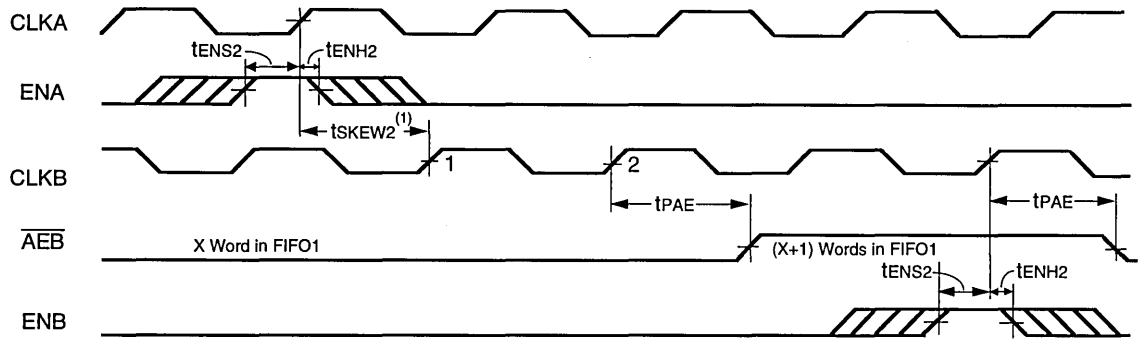
Figure 8. $\overline{FFA}$ Flag Timing and First Available Write when FIFO1 is Full.



Note:

1. tSKEW1 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{FFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW1, then $\overline{FFB}$ may transition HIGH one CLKB cycle later than shown.

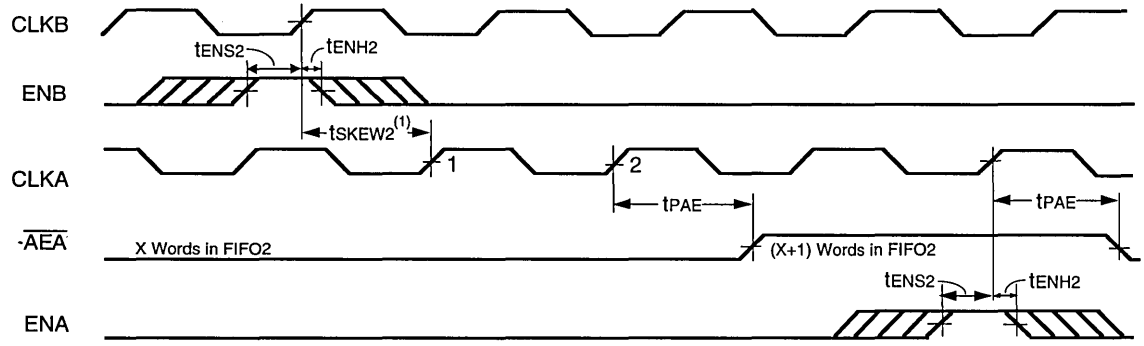
Figure 9. $\overline{FFB}$ Flag Timing and First Available Write when FIFO2 is Full



3012 drw 13

Notes:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then $\overline{AEB}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO1 read ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = LOW, MBB = LOW).

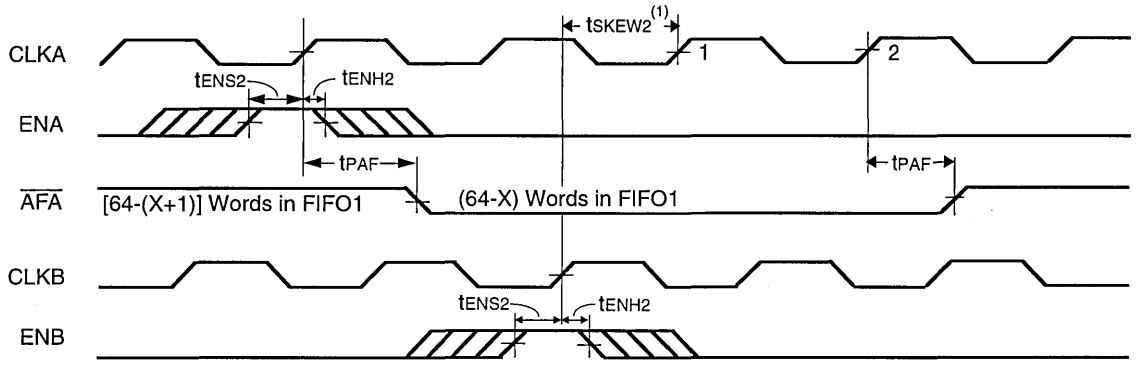
Figure 10. Timing for $\overline{AEB}$ when FIFO1 is Almost Empty



3012 drw 14

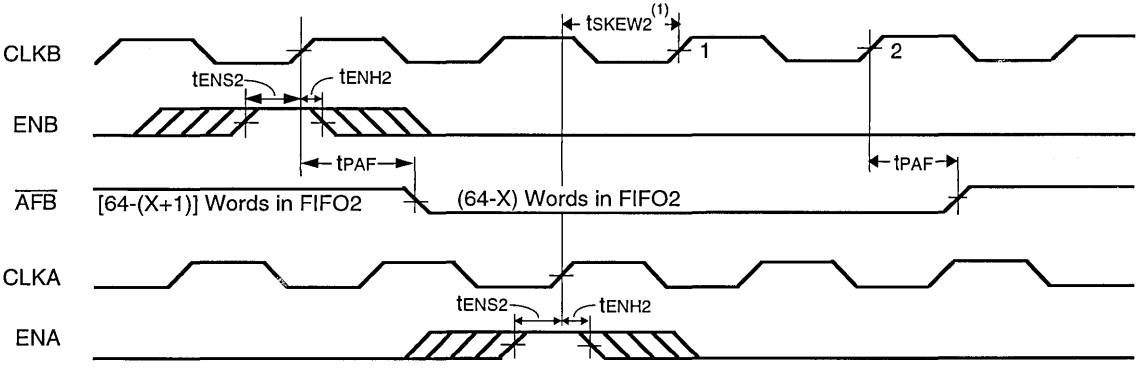
Notes:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW2, then $\overline{AEA}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO2 Write ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = HIGH, MBB = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW).

Figure 11. Timing for $\overline{AEA}$ when FIFO2 is Almost Empty



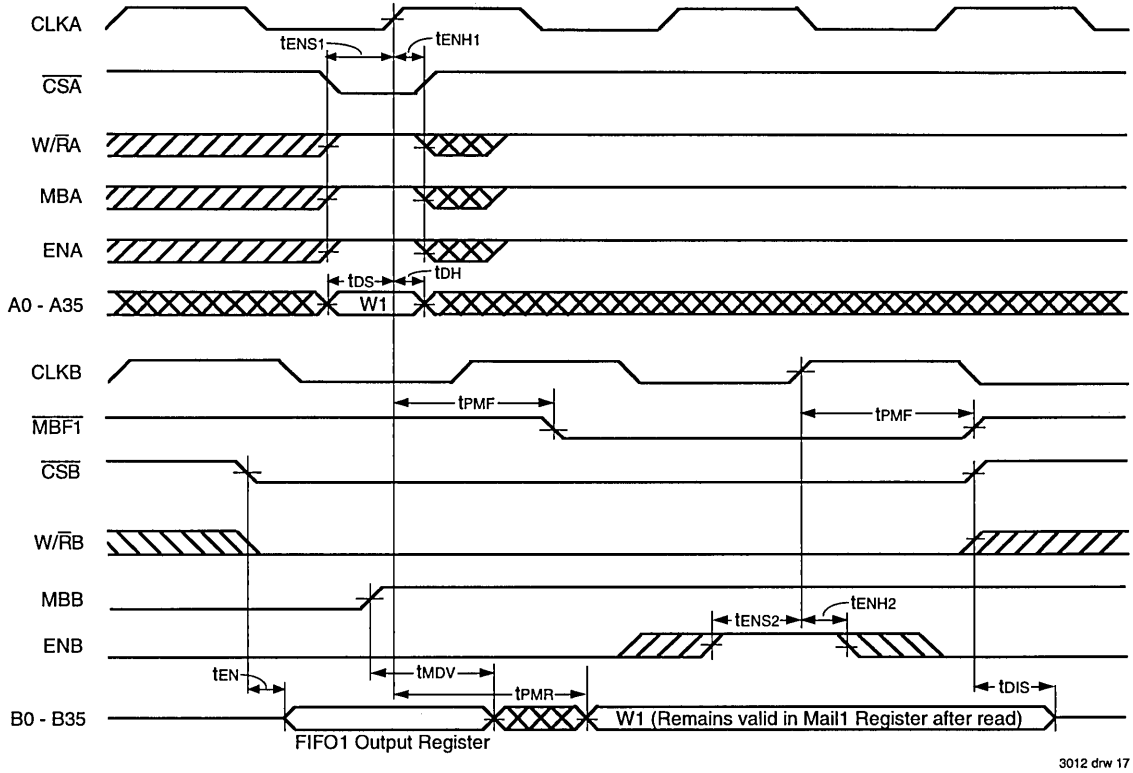
Notes:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then $\overline{AFA}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO1 read ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = LOW, MBB = LOW).

Figure 12. Timing for $\overline{AFA}$ when FIFO1 is Almost Full



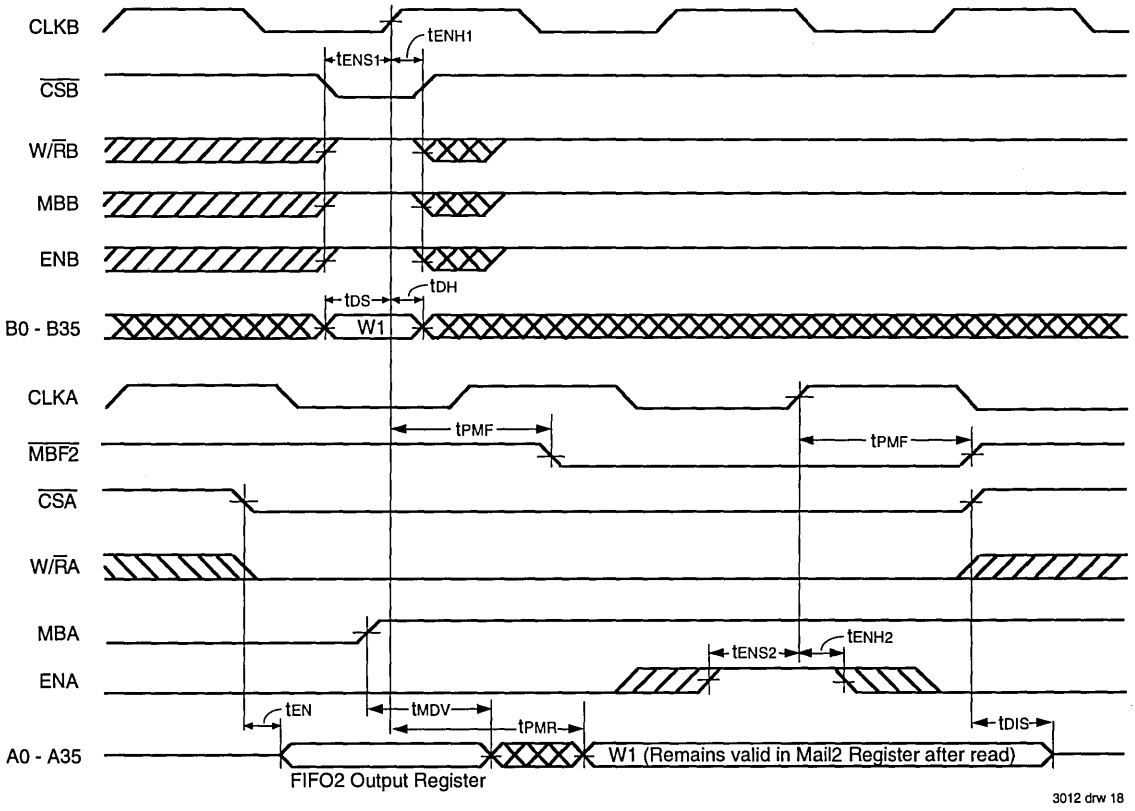
Notes:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW2, then $\overline{AFB}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO2 Write ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = HIGH, MBB = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW).

Figure 13. Timing for $\overline{AFB}$ when FIFO2 is Almost Full



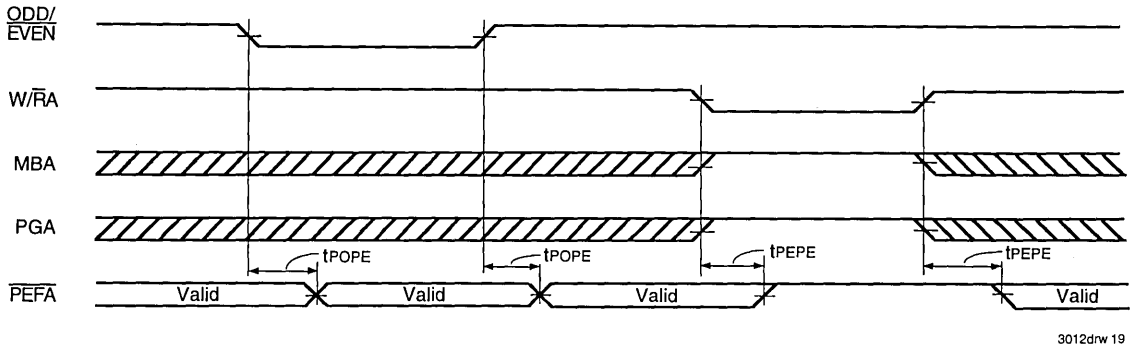
Note:
1. Port-B parity generation off (PGB = LOW)

Figure 14. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag



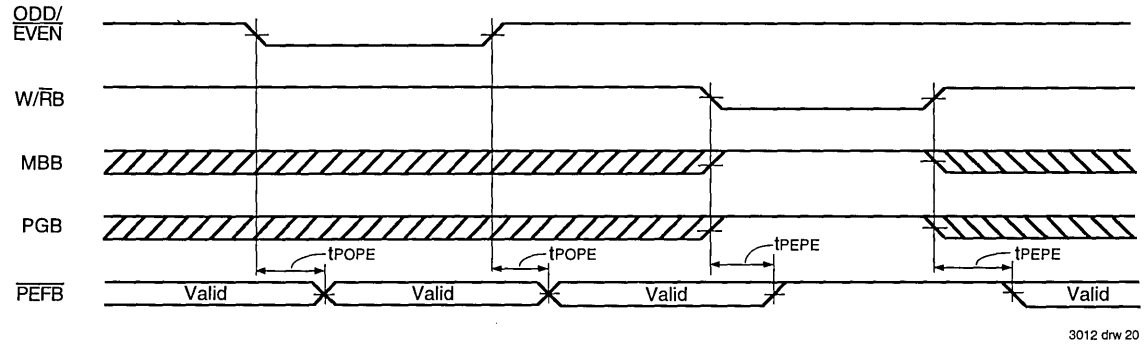
Note:
1. Port-A parity generation off (PGA = LOW)

Figure 15. Timing for Mail2 Register and $\overline{MBF2}$ Flag



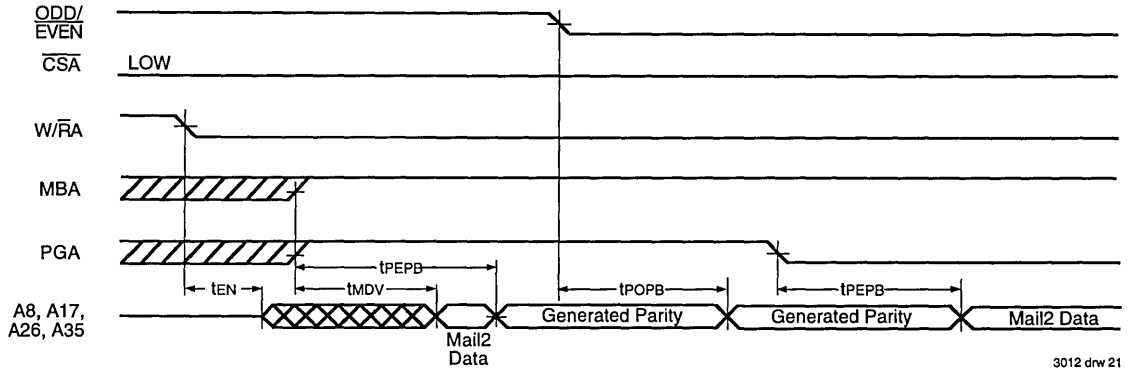
Note:
1. ENA is HIGH, and $\overline{CSA}$ is LOW

Figure 16. ODD/$\overline{EVEN}$ W/$\overline{RA}$, MBA, and PGA to $\overline{PEFA}$ Timing



Note:
1. ENB is HIGH, and $\overline{CSB}$ is LOW

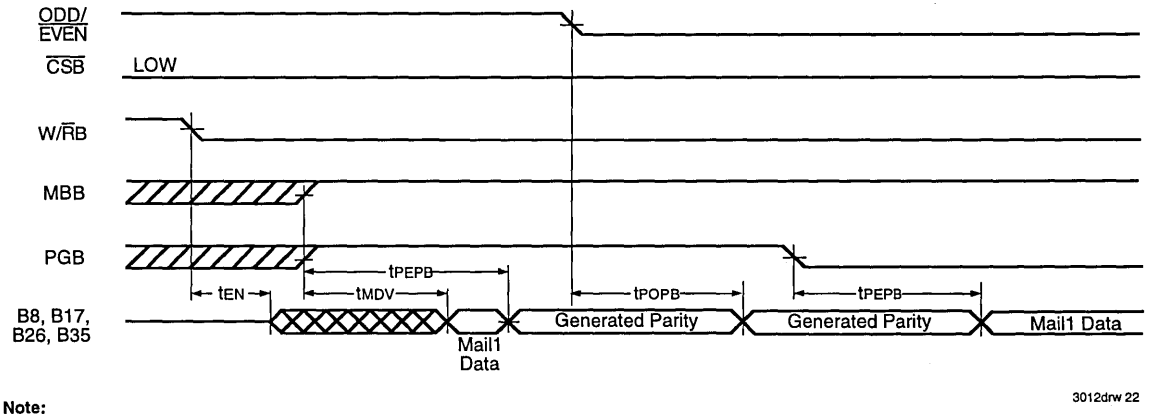
Figure 17. ODD/$\overline{EVEN}$ W/$\overline{RB}$, MBB, and PGB to $\overline{PEFB}$ Timing



Note:
1. ENA is HIGH

Figure 18. Parity Generation Timing when Reading from Mail2 Register

5



Note:
1. ENB is HIGH

Figure 19. Parity Generation Timing when Reading from Mail1 Register

TYPICAL CHARACTERISTICS

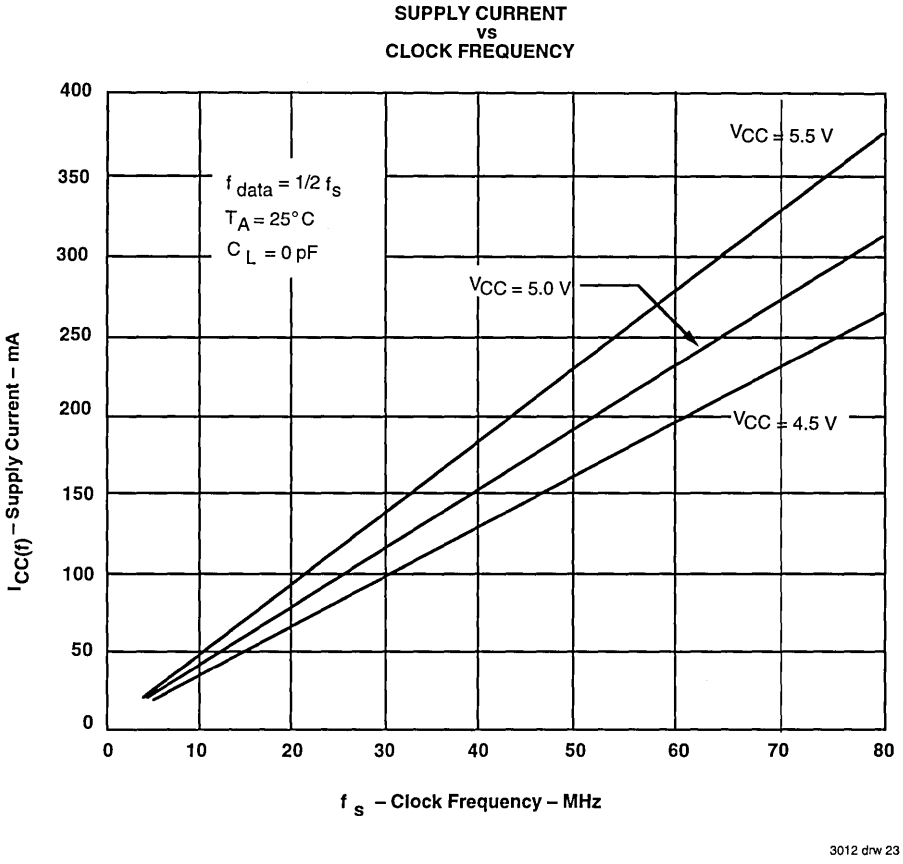


Figure 20

CALCULATING POWER DISSIPATION

The $I_{CC(f)}$ current for the graph in Figure 20 was taken while simultaneously reading and writing the FIFO on the IDT723612 with CLKA and CLKB set to fs. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitance load per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 28, the maximum power dissipation (P_D) of the IDT723612 may be calculated by:

$$P_D = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times V_{CC} \times (V_{OH} - V_{OL}) \times f_o)$$

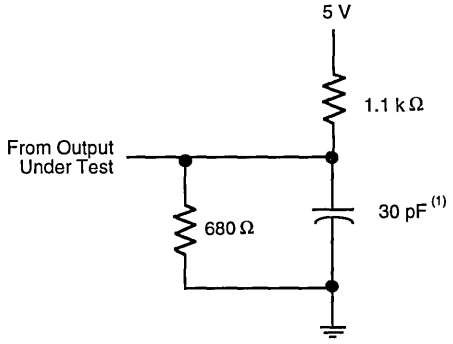
where:

C_L	=	output capacitance load
f_o	=	switching frequency of an output
V_{OH}	=	output HIGH level voltage
V_{OL}	=	output LOW level voltage

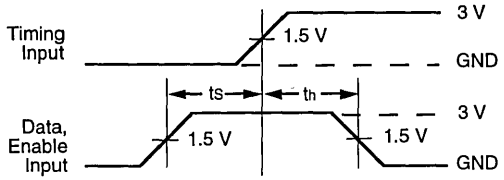
When no reads or writes are occurring on the IDT723612, the power dissipated by a single clock (CLKA or CLKB) input running at frequency fs is calculated by:

$$P_T = V_{CC} \times f_S \times 0.290 \text{ mA/MHz}$$

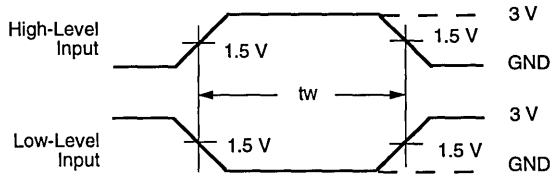
PARAMETER MEASUREMENT INFORMATION



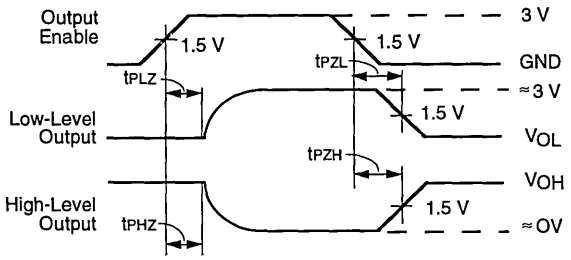
LOAD CIRCUIT



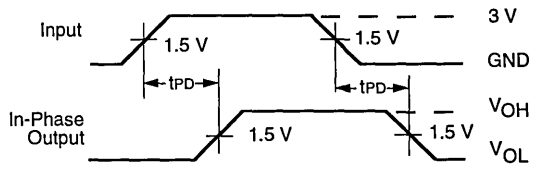
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



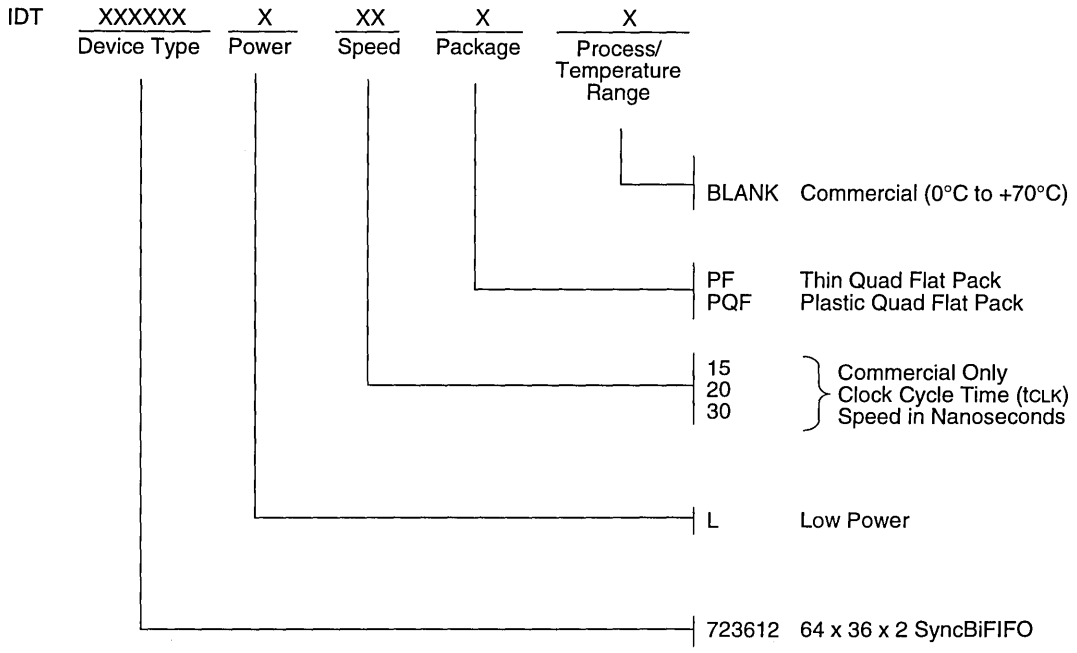
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

3012 drw 24

Note:
1. Includes probe and jig capacitance

Figure 21. Load Circuit and Voltage Waveforms

ORDERING INFORMATION



3012 drw 25

Integrated Device Technology, Inc.

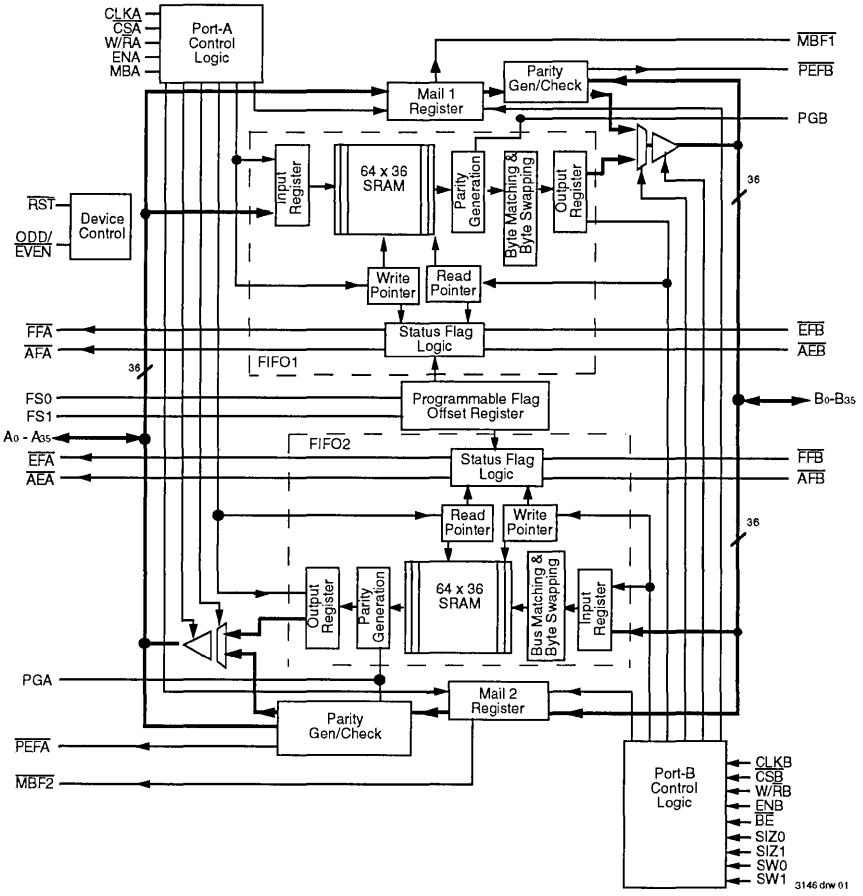
CMOS SyncBiFIFO™ WITH BUS MATCHING AND BYTE SWAPPING 64 x 36 x 2

IDT723614

FEATURES:

- Free-running CLKA and CLKB can be asynchronous or coincident (simultaneous reading and writing of data on a single clock edge is permitted)
- Two independent clocked FIFOs (64 x 36 storage capacity each) buffering data in opposite directions
- Mailbox bypass Register for each FIFO
- Dynamic Port B bus sizing of 36-bits (long word), 18-bits (word), and 9-bits (byte)
- Selection of Big- or Little-Endian format for word and byte bus sizes
- Three modes of byte-order swapping on port B
- Programmable Almost-Full and Almost-Empty Flags
- Microprocessor interface control logic
- $\overline{EFA}$, $\overline{FFA}$, $\overline{AEA}$, and $\overline{AFA}$ flags synchronized by CLKA
- $\overline{EFB}$, $\overline{FFB}$, $\overline{AEB}$, and $\overline{AFB}$ flags synchronized by CLKB
- Passive parity checking on each port
- Parity generation can be selected for each port
- Low-power advanced BiCMOS technology
- Supports clock frequencies up to 67 MHz
- Fast access times of 10 ns
- Available in 132-pin plastic quad flat package (PQF) or space-saving 120-pin thin quad flat package (TQFP)

FUNCTIONAL BLOCK DIAGRAM

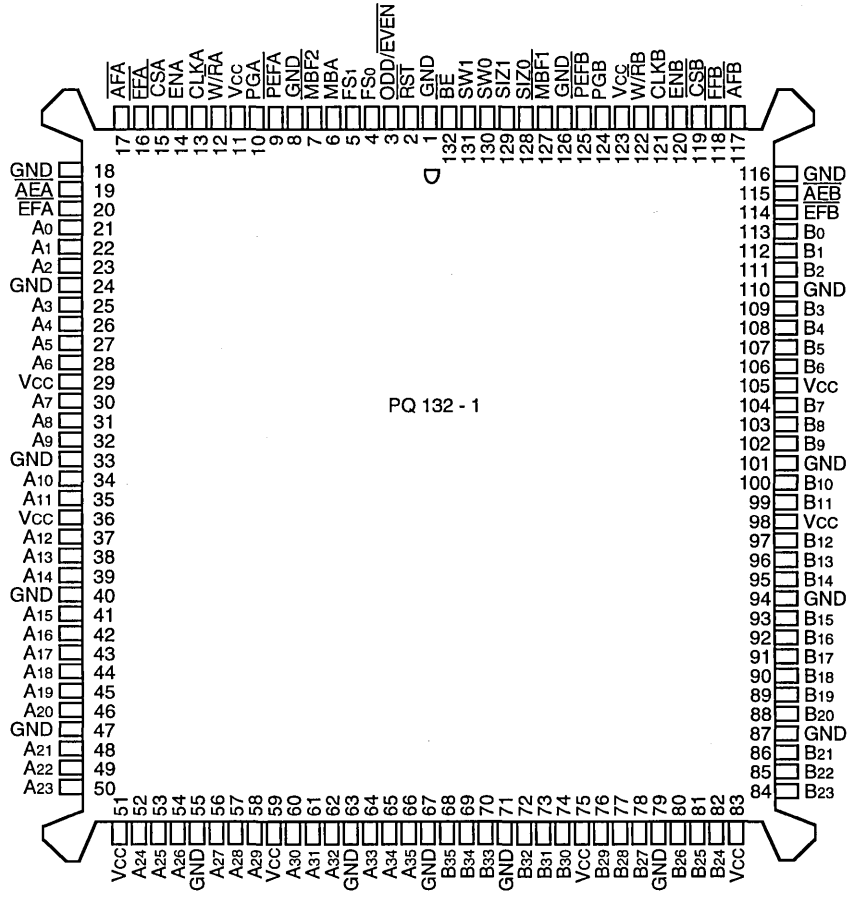


DESCRIPTION:

The IDT723614 is a monolithic, high-speed, low-power BiCMOS bidirectional clocked FIFO memory. It supports clock frequencies up to 67MHz and has read access times as fast as 10ns. Two independent 64 x 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (almost-full and almost-empty) to indicate when a selected number of words is stored in memory. FIFO data on port B can be input and output in 36-bit, 18-bit, and 9-bit formats with a choice of big- or little-endian configurations. Three modes of byte-order swapping are possible with any bus size selection. Communication between each port can bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if not desired. Parity generation can be selected for data read from each port. Two or more devices can be used in parallel to create wider data paths.

The IDT723614 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a continuous (free-running) port clock by enable signals. The clocks for

PIN CONFIGURATIONS



3146 drw 02

PQF PACKAGE
TOP VIEW

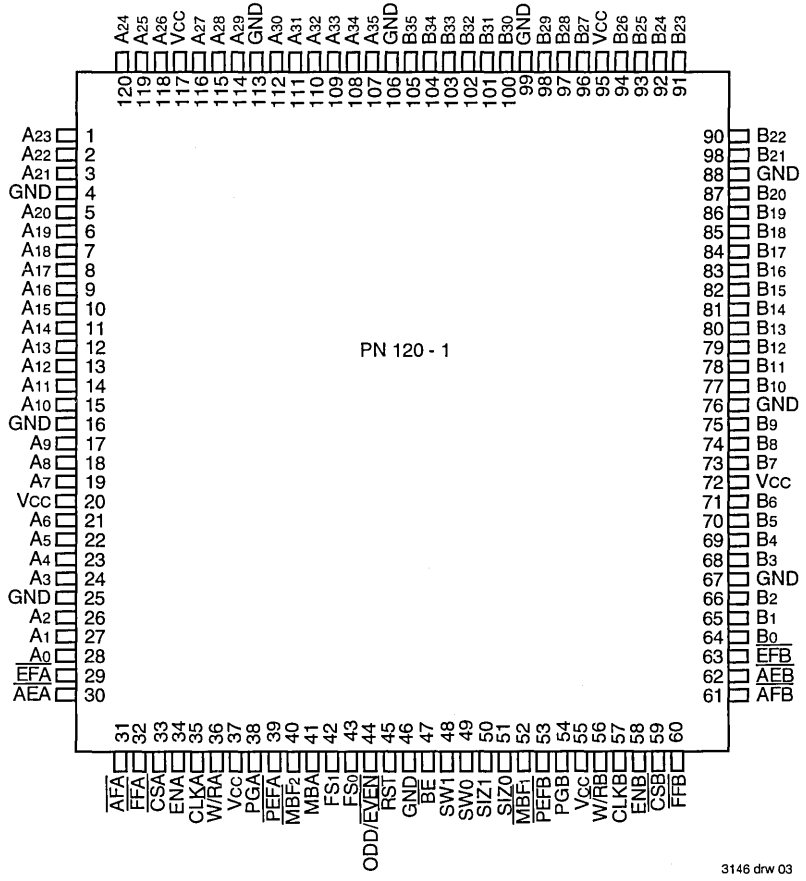
NOTES:
1. NC - No internal connection.
2. Uses Yamaichi socket IC51-1324-828.

each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses controlled by a synchronous interface.

The full flag ($\overline{FFA}$, $\overline{FFB}$) and almost-full flag ($\overline{AFA}$, $\overline{AFB}$) of a FIFO are two-stage synchronized to the port clock that writes data to its array. The empty flag ($\overline{EFA}$, $\overline{EFB}$) and almost-empty ($\overline{AEA}$, $\overline{AEB}$) flag of a FIFO are two stage synchronized to the port clock that reads data from its array.

The IDT723614 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS (CONT.)



3146 drw 03

TQFP
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
A0-A35	Port A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AEA}$	Port A Almost-Empty Flag	O (Port A)	Programmable almost-empty flag synchronized to CLKA. It is LOW when the number of 36-bit words in FIFO2 is less than or equal to the value in the offset register, X.
$\overline{AEB}$	Port B Almost-Empty Flag	O (Port B)	Programmable almost-empty flag synchronized to CLKB. It is LOW when the number of 36-bit words in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFA}$	Port A Almost-Full Flag	O (Port A)	Programmable almost-full flag synchronized to CLKA. It is LOW when the number of 36-bit empty locations in FIFO1 is less than or equal to the value in the offset register, X.
$\overline{AFB}$	Port B Almost-Full Flag	O (Port B)	Programmable almost-full flag synchronized to CLKB. It is LOW when the number of 36-bit empty locations in FIFO2 is less than or equal to the value in the offset register, X.
B0-B35	Port B Data.	I/O	36-bit bidirectional data port for side B.
$\overline{BE}$	Big-endian select	I	Selects the bytes on port B used during byte or word data transfer. A LOW on $\overline{BE}$ selects the most significant bytes on B0-B35 for use, and a HIGH selects the least significant bytes
CLKA	Port A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. $\overline{EFA}$, $\overline{FFA}$, $\overline{AFA}$, and $\overline{AEA}$ are synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. Port B byte swapping and data port sizing operations are also synchronous to the LOW-to-HIGH transition of CLKB. $\overline{EFB}$, $\overline{FFB}$, $\overline{AFB}$, and $\overline{AEB}$ are synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port A Chip Select	I	$\overline{CSA}$ must be LOW to enable a LOW-to-HIGH transition of CLKA to read or write data on port A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on port B. The B0-B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EFA}$	Port A Empty Flag	O (Port A)	$\overline{EFA}$ is synchronized to the LOW-to-HIGH transition of CLKA. When $\overline{EFA}$ is LOW, FIFO2 is empty, and reads from its memory are disabled. Data can be read from FIFO2 to the output register when $\overline{EFA}$ is HIGH. $\overline{EFA}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after data is loaded into empty FIFO2 memory.
$\overline{EFB}$	Port B Empty Flag	O (Port B)	$\overline{EFB}$ is synchronized to the LOW-to-HIGH transition of CLKB. When $\overline{EFB}$ is LOW, the FIFO1 is empty, and reads from its memory are disabled. Data can be read from FIFO1 to the output register when $\overline{EFB}$ is HIGH. $\overline{EFB}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after data is loaded into empty FIFO1 memory.
ENA	Port A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port A.
ENB	Port B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on port B.
$\overline{FFA}$	Port A Full Flag	O (Port A)	$\overline{FFA}$ is synchronized to the LOW-to-HIGH transition of CLKA. When $\overline{FFA}$ is LOW, FIFO1 is full, and writes to its memory are disabled. $\overline{FFA}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after reset.
$\overline{FFB}$	Port B Full Flag	O (Port B)	$\overline{FFB}$ is synchronized to the LOW-to-HIGH transition of CLKB. When $\overline{FFB}$ is LOW, FIFO2 is full, and writes to its memory are disabled. $\overline{FFB}$ is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after reset.

PIN DESCRIPTION (CONTINUED)

Symbol	Name	I/O	Description
FS1, FS0	Flag-Offset Selects	I	The LOW-to-HIGH transition of $\overline{RST}$ latches the values of FS0 and FS1, which selects one of four preset values for the almost-full flag and almost-empty flag offset.
MBA	Port A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a port A read or write operation. When the A0-A35 outputs are active, a HIGH level on MBA selects data from the mail2 register for output, and a LOW level selects FIFO2 output register data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is set LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a port B read is selected and both SIZ1 and SIZ0 are HIGH. $\overline{MBF1}$ is set HIGH when the device is reset.
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is set LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a port A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH when the device is reset.
ODD/ $\overline{EVEN}$	Odd/Even Parity Select	I	Odd parity is checked on each port when ODD/$\overline{EVEN}$ is HIGH, and even parity is checked when ODD/$\overline{EVEN}$ is LOW. ODD/$\overline{EVEN}$ also selects the type of parity generated for each port if parity generation is enabled for a readoperation.
$\overline{PEFA}$	Port A Parity Error Flag	O (Port A)	When any byte applied to terminals A0-A35 fails parity, $\overline{PEFA}$ is LOW. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is deter mined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the A0-A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read parity generation is setup by having W/$\overline{RA}$ LOW, MBA HIGH, and PGA HIGH, the $\overline{PEFA}$ flag is forced HIGH regardless of the A0-A35 inputs.
$\overline{PEFB}$	Port B Parity Error Flag	O (Port B)	When any valid byte applied to terminals B0-B35 fails parity, $\overline{PEFB}$ is LOW. Bytes are organized as B0-B8, B9-B17, B18-B26, B27-B35 with the most significant bit of each byte serving as the parity bit. A byte is valid when it is used by the bus size selected for Port B. The type of parity checked is determined by the state of the ODD/$\overline{EVEN}$ input. The parity trees used to check the B0-B35 inputs are sharedby the mail 1 register to generate parity if parity generation isselected by PGB. Therefore, if a mail1 read with parity generation is setup by having W/$\overline{RB}$ LOW, SIZ1 and SIZ0 HIGH, and PGB HIGH, the $\overline{PEFB}$ flag is forced HIGH regardless of the state of the B0-B35 inputs.
PGA	Port A Parity Generation	I	Parity is generated for data reads from port A when PGA is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35. The generated parity bits are output in the most significant bit of each byte.
PGB	Port B Parity Generation	I	Parity is generated for data reads from port B when PGB is HIGH. The type of parity generated is selected by the state of the ODD/$\overline{EVEN}$ input. Bytes are organized as B0-B8, B9-B17, B18-B26, and B27-B35. The generated parity bits are output in the most significant bit of each byte.
$\overline{RST}$	Reset	I	To reset the device, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST}$ is LOW. This sets the $\overline{AFA}$, $\overline{AFB}$, $\overline{MBF1}$, and $\overline{MBF2}$ flags HIGH and the $\overline{EFA}$, $\overline{EFB}$, $\overline{AEA}$, $\overline{AEB}$, $\overline{FFA}$, and $\overline{FFB}$ flags LOW. The LOW-to-HIGH transition of $\overline{RST}$ latches the status of the FS1 and FS0 inputs to select almost-full and almost-empty flag offsets
SIZ0, SIZ1	Port B bus size selects	I (Port B)	A LOW-to-HIGH transition of CLKB latches the states of SIZ0, SIZ1, and $\overline{BE}$, and the following LOW-to-HIGH transition of CLKB implements the latched states as a port B bus size. Port B bus sizes can be long word, word, or byte. A high on both SIZ0 and SIZ1 accesses the mailbox reegisters for a port B 36-bit write or read.

PIN DESCRIPTION (CONTINUED)

Symbol	Name	I/O	Description
SW0, SW1	Port B byte swap Select	I (Port B)	At the beginning of each long word transfer, one of four modes of byte-order swapping is selected by SW0 and SW1. The four modes are no swap, byte swap, word swap, and byte-word swap. Byte-order swapping is possible with any bus-size selection.
W/$\overline{RA}$	Port A Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the high-impedance state when W/$\overline{RA}$ is HIGH.
W/$\overline{RB}$	Port B Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the high-impedance state when W/$\overline{RB}$ is HIGH.

SIGNAL DESCRIPTIONS

RESET

The IDT723614 is reset by taking the reset ($\overline{RST}$) input LOW for at least four port A clock (CLKA) and four port B clock (CLKB) LOW-to-HIGH transitions. The reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of each FIFO and forces the full flags ($\overline{FFA}$, $\overline{FFB}$) LOW, the empty flags ($\overline{EFA}$, $\overline{EFB}$) LOW, the almost-empty flags ($\overline{AEA}$, $\overline{AEB}$) LOW and the almost-full flags ($\overline{AFA}$, $\overline{AFB}$) HIGH. A reset also forces the mailbox flags ($\overline{MBF1}$, $\overline{MBF2}$) HIGH. After a reset, $\overline{FFA}$ is set HIGH after two LOW-to-HIGH transitions of CLKA and $\overline{FFB}$ is set HIGH after two LOW-to-HIGH transitions of CLKB. The device must be reset after power up before data is written to its memory.

A LOW-to-HIGH transition on the $\overline{RST}$ input loads the almost-full and almost-empty offset register (X) with the values selected by the flag-select (FS0, FS1) inputs. The values that can be loaded into the registers are shown in Table 1.

FIFO WRITE/READ OPERATION

The state of port A data A0-A35 outputs is controlled by the port A chip select ($\overline{CSA}$) and the port A write/read select (W/$\overline{RA}$). The A0-A35 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW. Data is loaded into FIFO1 from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH, MBA is LOW, and $\overline{FFA}$ is HIGH. Data is read from FIFO2 to the A0-A35 outputs by a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is LOW, ENA is HIGH, MBA is LOW, and $\overline{EFA}$ is HIGH (see Table 2).

The port B control signals are identical to those of port A. The state of the port B data (B0-B35) outputs is controlled by the port B chip select ($\overline{CSB}$) and the port B write/read select (W/$\overline{RB}$). The B0-B35 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{RB}$ is HIGH. The B0-B35 outputs are active when both $\overline{CSB}$ and W/$\overline{RB}$ are LOW. Data is loaded into FIFO2 from the B0-B35 inputs on a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, W/$\overline{RB}$ is HIGH, ENB is HIGH, $\overline{EFB}$ is HIGH, and either SIZ0 or SIZ1 is LOW. Data is read from FIFO1 to the B0-B35 outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, W/$\overline{RB}$ is LOW, ENB is HIGH, $\overline{EFB}$ is HIGH, and either SIZ0 or SIZ1 is LOW (see Table 3).

The setup and hold time constraints to the port clocks for the port chip selects (CSA, CSB) and write/read selects (W/RA, W/RB) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port chip select and write/read select can change states during the setup and hold time window of the cycle.

SYNCHRONIZED FIFO FLAGS

Each FIFO is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on the output when CLKA and CLKB operate asynchronously to one another. $\overline{EFA}$, $\overline{AEA}$, $\overline{FFA}$, and $\overline{AFA}$ are synchronized to CLKA. $\overline{EFB}$, $\overline{AEB}$, $\overline{FFB}$, and $\overline{AFB}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

EMPTY FLAGS ($\overline{EFA}$, $\overline{EFB}$)

The empty flag of a FIFO is synchronized to the port clock that reads data from its array. When the empty flag is HIGH, new data can be read to the FIFO output register. When the empty flag is LOW, the FIFO is empty and attempted FIFO reads are ignored. When reading FIFO1 with a byte or word size on port B, $\overline{EFB}$ is set LOW when the fourth byte or second word of the last long word is read.

The read pointer of a FIFO is incremented each time a new word is clocked to the output register. The state machine that controls an empty flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to a FIFO can be read to the FIFO output register in a minimum of three cycles of the empty flag synchronizing clock. Therefore, an empty flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port

clock that reads data from the FIFO have not elapsed since the time the word was written. The empty flag of the FIFO is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock, and the new data word can be read to the FIFO output register in the following cycle.

A LOW-to-HIGH transition on an empty flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 13 and 14).

TABLE 1: FLAG PROGRAMMING

FS1	FS0	$\overline{RST}$	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

FULL FLAG ($\overline{FFA}$, $\overline{FFB}$)

The full flag of a FIFO is synchronized to the port clock that writes data to its array. When the full flag is HIGH, a memory location is free in the SRAM to receive new data. No memory locations are free when the full flag is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, the write pointer is incremented. The state machine that controls a full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is full, full-1, or full-2. From the time a word is read from a FIFO, the previous memory location is ready to be written in a minimum of three cycles of the full flag synchronizing clock. Therefore, a full flag is LOW if less than two cycles of the full flag synchronizing clock have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the full flag synchronization clock after the read sets the full flag HIGH and the data can be written in the following clock cycle.

A LOW-to-HIGH transition on a full flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figure 15 and 16).

5

TABLE 2: PORT-A ENABLE FUNCTION TABLE

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	A0-A35 Outputs	Port Functions
H	X	X	X	X	In High-Impedance State	None
L	H	L	X	X	In High-Impedance State	None
L	H	H	L	↑	In High-Impedance State	FIFO1 Write
L	H	H	H	↑	In High-Impedance State	Mail1 Write
L	L	L	L	X	Active, FIFO2 Output Register	None
L	L	H	L	↑	Active, FIFO2 Output Register	FIFO2 Read
L	L	L	H	X	Active, Mail2 Register	None
L	L	H	H	↑	Active, Mail2 Register	Mail2 Read (Set $\overline{MBF2}$ HIGH)

TABLE 3: PORT-B ENABLE FUNCTION TABLE

$\overline{CSB}$	W/$\overline{RB}$	ENB	SIZ1, SIZ0	CLKB	B0-B35 Outputs	Port Functions
H	X	X	X	X	In High-Impedance State	None
L	H	L	X	X	In High-Impedance State	None
L	H	H	One, both LOW	↑	In High-Impedance State	FIFO2 Write
L	H	H	Both HIGH	↑	In High-Impedance State	Mail2 Write
L	L	L	One, both LOW	X	Active, FIFO1 Output Register	None
L	L	H	One, both LOW	↑	Active, FIFO1 Output Register	FIFO1 read
L	L	L	Both HIGH	X	Active, Mail1 Register	None
L	L	H	Both HIGH	↑	Active, Mail1 Register	Mail1 Read (Set $\overline{MBF1}$ HIGH)

ALMOST EMPTY FLAGS ($\overline{AEA}$, $\overline{AEB}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an almost-empty flag monitors a write-pointer and a read-pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see Reset above). An almost-empty flag is LOW when the FIFO contains X or less long words in memory and is HIGH when the FIFO contains (X+1) or more long words.

Two LOW-to-HIGH transitions of the almost-empty flag synchronizing clock are required after a FIFO write for the almost-empty flag to reflect the new level of fill. Therefore, the almost-empty flag of a FIFO containing (X+1) or more long words remains LOW if two cycles of the synchronizing clock have not elapsed since the write that filled the memory to the (X+1) level. An almost-empty flag is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of an almost-empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) long words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figure 17 and 18).

ALMOST FULL FLAGS ($\overline{AFA}$, $\overline{AFB}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an almost-full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is almost full, almost full-1, or almost full-2. The almost-full state is defined by the value of the almost-full and almost-empty offset register (X). This register is loaded with one of four preset values during a device reset (see Reset above). An almost-full flag is LOW when the FIFO contains (64-X) or more long words in memory and is HIGH when the FIFO contains [64-(X+1)] or less long words.

Two LOW-to-HIGH transitions of the almost-full flag synchronizing clock are required after a FIFO read for the almost-full flag to reflect the new level of fill. Therefore, the almost-full flag of a FIFO containing [64-(X+1)] or less words remains LOW if two cycles of the synchronizing clock have not elapsed since the read that reduced the number of long words in memory to [64-(X+1)]. An almost-full flag is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock after the FIFO read that reduces the number of long words in memory to [64-(X+1)]. A LOW-to-HIGH transition of an almost-full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of long words in memory to [64-(X+1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figure 19 and 20).

MAILBOX REGISTERS

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A LOW-to-HIGH transition on CLKA writes A0-A35 data to the mail1 register when a port A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA with MBA HIGH. A LOW-to-HIGH transition on CLKB writes B0-B35 data to the mail2 register when a port B write is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB with both SIZ1 and SIZ0 HIGH. Writing data to a mail register sets the corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while the mail flag is LOW.

When the port A data outputs (A0-A35) are active, the data on the bus comes from the FIFO2 output register when MBA is LOW and from the mail2 register when MBA is HIGH. When the port B data outputs (B0-B35) are active, the data on the bus comes from the FIFO1 output register when either one

TABLE 4: FIFO1 FLAG OPERATION

Number of 36-Bit Words in the FIFO1[1]	Synchronized to CLKB		Synchronized to CLKA	
	$\overline{EFB}$	$\overline{AEB}$	$\overline{AFA}$	$\overline{FFA}$
0	L	L	H	H
1 to X	H	L	H	H
(X+1) to [64-(X+1)]	H	H	H	H
(64-X) to 63	H	H	L	H
64	H	H	L	L

TABLE 5: FIFO2 FLAG OPERATION

Number of 36-Bit Words in the FIFO2[1]	Synchronized to CLKB		Synchronized to CLKA	
	$\overline{EFA}$	$\overline{AEA}$	$\overline{AFB}$	$\overline{FFB}$
0	L	L	H	H
1 to X	H	L	H	H
(X+1) to [64-(X+1)]	H	H	H	H
(64-X) to 63	H	H	L	H
64	H	H	L	L

NOTE:
1. X is the value in the almost-empty flag and almost-full flag offset register.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)(1)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	-0.5 to 7	V
V_I(2)	Input Voltage Range	-0.5 to Vcc+0.5	V
V_O(2)	Output Voltage Range	-0.5 to Vcc+0.5	V
I_{IK}	Input Clamp Current, (V_I < 0 or V_I > Vcc)	±20	mA
I_{OK}	Output Clamp Current, (V_O < 0 or V_O > Vcc)	±50	mA
I_{OUT}	Continuous Output Current, (V_O = 0 to Vcc)	±50	mA
I_{CC}	Continuous Current Through Vcc or GND	±500	mA
T_A	Operating Free Air Temperature Range	0 to 70	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

5

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply Voltage	4.5	5.5	V
VIH	HIGH Level Input Voltage	2	–	V
VIL	LOW-Level Input Voltage	–	0.8	V
IOH	HIGH-Level Output Current	–	-4	mA
IOL	LOW-Level Output Current	–	8	mA
TA	Operating Free-air Temperature	0	70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Parameter	Test Conditions		Min. Typ.(1) Max.	Unit
V_{OH}	V_{CC} = 4.5V, I_{OH} = -4 mA		2.4	V
V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8 mA		0.5	V
I_I	V_{CC} = 5.5 V, V_I = Vcc or 0		±50	µA
I_{OZ}	V_{CC} = 5.5 V, V_O = Vcc or 0		±50	µA
I_{CC}	V_{CC} = 5.5 V, I_O = 0 mA, V_I = Vcc or GND	Outputs HIGH	30	mA
		Outputs LOW	130	mA
		Outputs Disabled	30	mA
C_{IN}	V_I = 0, f = 1 MHz		4	pF
C_{OUT}	V_O = 0, f = 1 MHZ		8	pF

NOTE:
1 . All typical values are at VCC = 5 V, TA = 25°C.

DC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE (See Figures 4 through 26)

Symbol	Parameter	IDT723614L15		IDT723614L20		IDT723614L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fS	Clock Frequency, CLKA or CLKB	–	66.7	–	50	–	33.4	MHz
tCLK	Clock Cycle Time, CLKA or CLKB	15	–	20	–	30	–	ns
tCLKH	Pulse Duration, CLKA and CLKB HIGH	6	–	8	–	12	–	ns
tCLKL	Pulse Duration, CLKA and CLKB LOW	6	–	8	–	12	–	ns
tDS	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	4	–	5	–	6	–	ns
tENS	Setup Time, $\overline{CSA}$, W/$\overline{RA}$, ENA and MBA before CLKA↑; $\overline{CSB}$,W/$\overline{RB}$ and ENB before CLKB↑	5	–	5	–	6	–	ns
tSZS	Setup Time, SIZ0, SIZ1,and $\overline{BE}$ before CLKB↑	4	–	5	–	6	–	ns
tSWS	Setup Time, SW0 and SW1 before CLKB↑	5	–	7	–	8	–	ns
tPGS	Setup Time, ODD/$\overline{EVEN}$ and PGA before CLKA↑; ODD/$\overline{EVEN}$ and PGB before CLKB↑[1]	4	–	5	–	6	–	ns
tRSTS	Setup Time, $\overline{RST}$ LOW before CLKA↑ or CLKB↑[2]	5	–	6	–	7	–	ns
tFSS	Setup Time, FS0 and FS1 before $\overline{RST}$ HIGH	5	–	6	–	7	–	ns
tDH	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	1	–	1	–	1	–	ns
tENH	Hold Time, $\overline{CSA}$, W/$\overline{RA}$, ENA and MBA after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, and ENB after CLKB↑	1	–	1	–	1	–	ns
tSZH	Hold Time, SIZ0, SIZ1, and $\overline{BE}$ after CLKB↑	2	–	2	–	2	–	ns
tSWH	Hold Time, SW0 and SW1 after CLKB↑	0	–	0	–	0	–	ns
tPGH	Hold Time, ODD/$\overline{EVEN}$ and PGA after CLKA↑; ODD/$\overline{EVEN}$ and PGB after CLKB↑[1]	0	–	0	–	0	–	ns
tRSTH	Hold Time, $\overline{RST}$ LOW after CLKA↑ or CLKB↑[2]	5	–	6	–	7	–	ns
tFSH	Hold Time, FS0 and FS1 after $\overline{RST}$ HIGH	4	–	4	–	4	–	ns
tSKEW1[3]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{EFA}$, $\overline{EFB}$, $\overline{FFA}$, and $\overline{FFB}$	8	–	8	–	10	–	ns
tSKEW2[3]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	9	–	16	–	20	–	ns

NOTES:
1. Only applies for a clock edge that does a FIFO read.
2. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
3. Skew time is not a timimg constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 30pF (See Figures 4 through 26)

Symbol	Parameter	IDT723614L15		IDT723614L20		IDT723614L30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
tA	Access Time, CLKA↑ to A0-A35 and CLKB↑ to B0-B35	2	10	2	12	2	15	ns
tWFF	Propagation Delay Time, CLKA↑ to $\overline{FFA}$ and CLKB↑ to $\overline{FFB}$	2	10	2	12	2	15	ns
tREF	Propagation Delay Time, CLKA↑ to $\overline{EFA}$ and and CLKB↑ to $\overline{EFB}$	2	10	2	12	2	15	ns
tPAE	Propagation Delay Time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	2	10	2	12	2	15	ns
tPAF	Propagation Delay Time, CLKA↑ to $\overline{AFA}$ and CLKB↑ to $\overline{AFB}$	2	10	2	12	2	15	ns
tPMF	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	1	9	1	12	1	15	ns
tPMR	Propagation Delay Time, CLKA↑ to B0-B35[1] and CLKB↑ to A0-A35[2]	3	11	3	13	3	15	ns
tPPE[3]	Propagation delay time, CLKB↑ to $\overline{PEFB}$	2	11	2	12	2	13	ns
tMDV	Propagation Delay Time, MBA to A0-A35 valid and SIZ1, SIZ0 to B0-B35 valid	1	11	1	11. 5	1	12	ns
tPDPE	Propagation Delay Time, A0-A35 valid to $\overline{PEFA}$ valid; B0-B35 valid to $\overline{PEFB}$ valid	3	10	3	11	3	13	ns
tPOPE	Propagation Delay Time, ODD/$\overline{EVEN}$ to $\overline{PEFA}$ and $\overline{PEFB}$	3	11	3	12	3	14	ns
tPOPB[4]	Propagation Delay Time, ODD/$\overline{EVEN}$ to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	11	2	12	2	14	ns
tPEPE	Propagation Delay Time, $\overline{CSA}$, ENA,W/$\overline{RA}$, MBA, or PGA to $\overline{PEFA}$; $\overline{CSB}$, ENB, W/$\overline{RB}$, SIZ1, SIZ0, or PGB to $\overline{PEFB}$	1	11	1	12	1	14	ns
tPEPB[4]	Propagation Delay Time, $\overline{CSA}$, ENA, W/$\overline{RA}$, MBA, or PGA to parity bits (A8, A17, A26, A35); $\overline{CSB}$, ENB, W/$\overline{RB}$,SIZ1, SIZ0, or PGB to parity bits (B8, B17, B26, B35)	3	12	3	13	3	14	ns
tRSF	Propagation Delay Time, $\overline{RST}$ to ($\overline{MBF1}$, $\overline{MBF2}$) HIGH	1	15	1	20	1	30	ns
tEN	Enable Time, $\overline{CSA}$ and W/$\overline{RA}$ LOW to A0-A35 active and $\overline{CSB}$ LOW and $\overline{W}$/RB HIGH to B0-B35 active	2	10	2	12	2	14	ns
tDIS	Disable Time, $\overline{CSA}$ or W/$\overline{RA}$ HIGH to A0-A35 at high impedance and $\overline{CSB}$ HIGH or $\overline{W}$/RB LOW to B0-B35 at high impedance	1	8	1	9	1	11	ns

NOTES:
1. Writing data to the mail1 register when the B0-B35 outputs are active and SIZ1, SIZ0 are HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.
3. Only applies when a new port B bus size is implemented by the rising CLKB edge.
4. Only applies when reading data from a mail register.

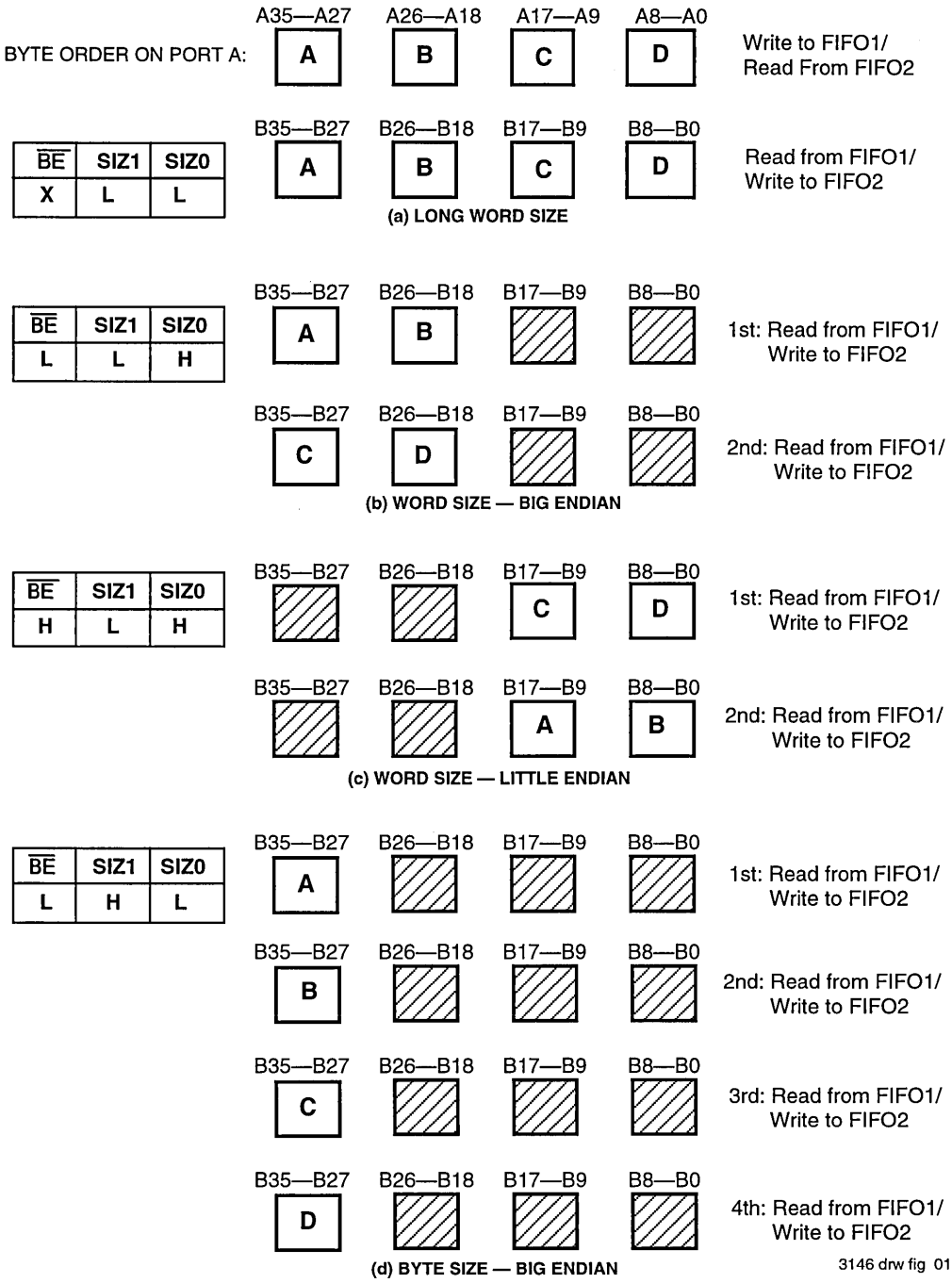
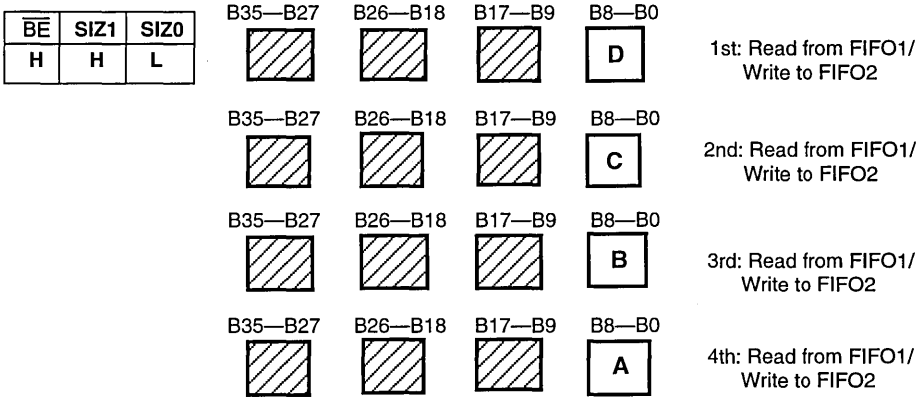


Figure 1. Dynamic Bus Sizing



(d) BYTE SIZE — LITTLE ENDIAN

3146 drw fig 01a

Figure 1. Dynamic Bus Sizing (continued)

DESCRIPTION (CONTINUED)

or both SIZ1 and SIZ0 are LOW and from the mail2 register when both SIZ1 and SIZ0 are HIGH.The mail1 register flag ($\overline{MBF1}$) is set HIGH by a rising CLKB edge when a port B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB with both SIZ1 and SIZ0 HIGH. The mail2 register flag ($\overline{MBF2}$) is set HIGH by a LOW-to-HIGH transition on CLKA when port A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and MBA is HIGH. The data in the mail register remains intact after it is read and changes only when new data is written to the register.

DYNAMIC BUS SIZING

The port B bus can be configured in a 36-bit long word, 18-bit word, or 9-bit byte format for data read from FIFO1 or written to FIFO2. Word- and byte-size bus selections can utilize the most significant bytes of the bus (big endian) or least significant bytes of the bus (little endian). Port B bus size can be changed dynamically and synchronous to CLKB to communicate with peripherals of various bus widths.

The levels applied to the port B bus size select (SIZ0, SIZ1) inputs and the big-endian select ($\overline{BE}$) input are stored on each CLKB LOW-to-HIGH transition. The stored port B bus size selection is implemented by the next rising edge on CLKB according to Figure 1.

Only 36-bit long-word data is written to or read from the two FIFO memories on the IDT723614. Bus-matching operations are done after data is read from the FIFO1 RAM and before data is written to the FIFO2 RAM. Port B bus sizing does not apply to mail register operations.

BUS-MATCHING FIFO1 READS

Data is read from the FIFO1 RAM in 36-bit long word increments. If a long word bus size is implemented, the entire long word immediately shifts to the FIFO1 output register. If byte or word size is implemented on port B, only the first one or two bytes appear on the selected portion of the FIFO1 output register, with the rest of the long word stored in auxiliary registers. In this case, subsequent FIFO1 reads with the same bus-size implementation output the rest of the long word to the FIFO1 output register in the order shown by Figure1.

Each FIFO1 read with a new bus-size implementation automatically unloads data from the FIFO1 RAM to its output register and auxiliary registers. Therefore, implementing a new port B bus size and performing a FIFO1 read before all bytes or words stored in the auxiliary registers have been read results in a loss of the unread long word data.

When reading data from FIFO1 in byte or word format, the unused B0-B35 outputs remain inactive but static, with the unused FIFO1 output register bits holding the last data value to decrease power consumption.

BUS-MATCHING FIFO2 WRITES

Data is written to the FIFO2 RAM in 36-bit long word increments. FIFO2 writes, with a long-word bus size, immediately store each long word in FIFO2 RAM. Data written to FIFO2 with a byte or word bus size stores the initial bytes or words in auxiliary registers. The CLKB rising edge that writes the fourth byte or the second word of long word to FIFO2 also stores the entire long word in FIFO2 RAM. The bytes are arranged in the manner shown in Figure 1.

Each FIFO2 write with a new bus-size implementation resets the state machine that controls the data flow from the auxiliary registers to the FIFO2 RAM. Therefore, implementing a new bus size and performing a FIFO2 write before bytes or words stored in the auxiliary registers have been loaded to FIFO2 RAM results in a loss of data.

PORT-B MAIL REGISTER ACCESS

In addition to selecting port-B bus sizes for FIFO reads and writes, the port B bus size select (SIZ0, SIZ1) inputs also access the mail registers. When both SIZ0 and SIZ1 are HIGH, the mail1 register is accessed for a port B long word read and the mail2 register is accessed for a port B long word write. The mail register is accessed immediately and any bus-sizing operation that may be underway is unaffected by the mail register access. After the mail register access is complete, the previous FIFO access can resume in the next CLKB cycle. The logic diagram in Figure 2 shows the previous bus-size selection is preserved when the mail registers are accessed from port B. A port B bus size is implemented on each rising CLKB edge according to the states of SIZ0_Q, SIZ1_Q, and $\overline{BE}$_Q.

BYTE SWAPPING

The byte-order arrangement of data read from FIFO1 or data written to FIFO2 can be changed synchronous to the rising edge of CLKB. Byte-order swapping is not available for mail register data. Four modes of byte-order swapping (including no swap) can be done with any data port size selection. The order of the bytes are rearranged within the long word, but the bit order within the bytes remains constant.

Byte arrangement is chosen by the port B swap select (SW0, SW1) inputs on a CLKB rising edge that reads a new long word from FIFO1 or writes a new long word to FIFO2. The byte order chosen on the first byte or first word of a new long word read from FIFO1 or written to FIFO2 is maintained until the entire long word is transferred, regardless of the SW0 and SW1 states during subsequent writes or reads. Figure 3 is an example of the byte-order swapping available for long words. Performing a byte swap and bus size simultaneously for a FIFO1 read first rearranges the bytes as shown in Figure 3, then outputs the bytes as shown in Figure 1. Simultaneous bus-sizing and byte-swapping operations for FIFO2 writes, first loads the data according to Figure 1, then swaps the bytes as shown in Figure 3 when the long word is loaded to FIFO2 RAM.

PARITY CHECKING

The port A inputs (A0-A35) and port B inputs (B0-B35) each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the port A data bus is reported by a LOW level on the port parity error flag ($\overline{PEFA}$). A parity failure on one or more bytes of the port B data input that are valid for the bus-size implementation is reported by a LOW level on the port B parity error flag ($\overline{PEFB}$).Odd or even parity checking can be selected, and the parity error flags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the odd/even parity (ODD/$\overline{EVEN}$) select input. A parity error on one or more valid bytes of a port is reported by a LOW level on the corresponding port parity error flag ($\overline{PEFA}$, $\overline{PEFB}$) output. Port A bytes are arranged as A0-A8, A9-A17,

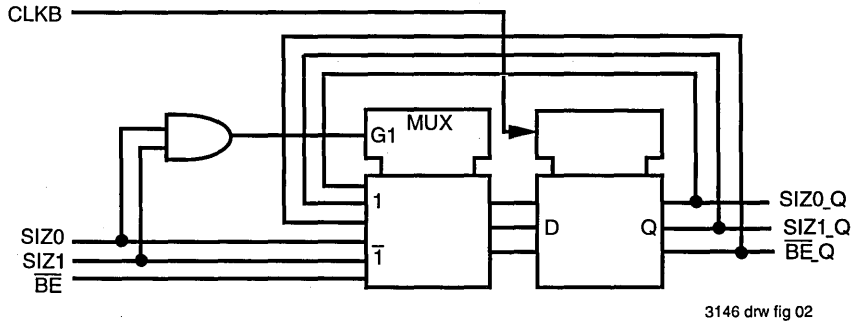
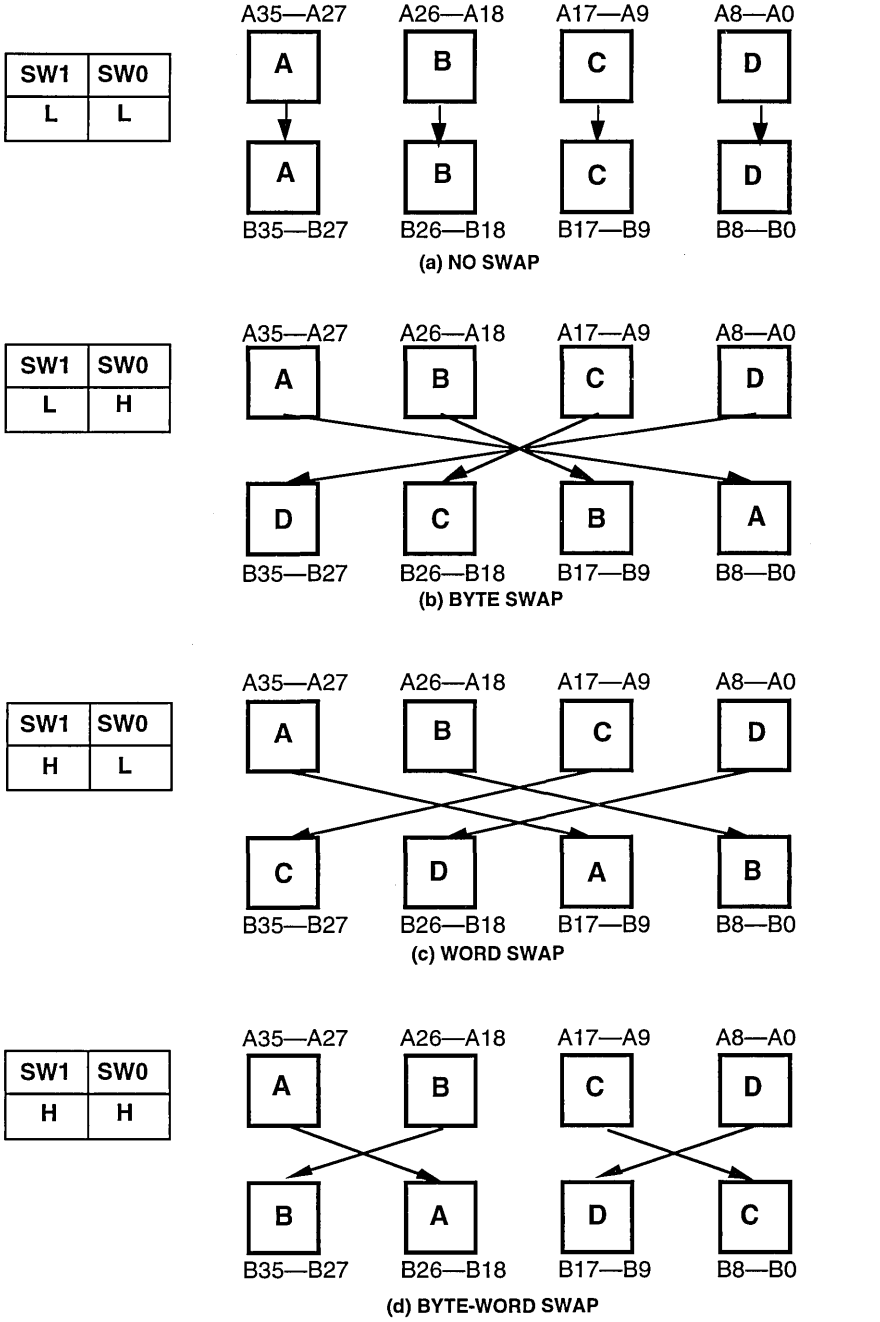


Figure 2. Logic Diagrams for SIZ0, SIZ1, and $\overline{BE}$ Register



3146 drw fig 03

Figure 3. Byte Swapping (Long Word Size Example)

5

A18-A26, and A27-A35. Port B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, and its valid bytes are those used in a port B bus-size implementation. When odd/even parity is selected, a port parity error flag ($\overline{PEFA}$, $\overline{PEFB}$) is LOW if any byte on the port has an odd/even number of LOW levels applied to the bits.

The four parity trees used to check the A0-A35 inputs are shared by the mail2 register when parity generation is selected for port A reads (PGA = HIGH). When a port A read from the mail2 register with parity generation is selected with $\overline{CSA}$ LOW, ENA HIGH, W/$\overline{RA}$ LOW, MBA HIGH, and PGA HIGH, the port A parity error flag ($\overline{PEFA}$) is held HIGH regardless of the levels applied to the A0-A35 inputs. Likewise, the parity trees used to check the B0-B35 inputs are shared by the mail1 register when parity generation is selected for port B reads (PGB = HIGH). When a port B read from the mail1 register with parity generation is selected with $\overline{CSB}$ LOW, ENB HIGH, W/$\overline{RB}$ LOW, both SIZ0 and SIZ1 HIGH, and PGB HIGH, the port B parity error flag ($\overline{PEFB}$) is held HIGH regardless of the levels applied to the B0-B35 inputs.

PARITY GENERATION

A HIGH level on the port A parity generate select (PGA) or port B parity generate select (PGB) enables the IDT723614 to generate parity bits for port reads from a FIFO or mailbox register. Port A bytes are arranged as A0-A8, A9-A17, A18-26, and A27-A35, with the most significant bit of each byte used as the parity bit. Port B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all nine inputs of a byte regardless of the state of the parity generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/$\overline{EVEN}$ select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port A parity generate select (PGA) and odd/even parity select (ODD/$\overline{EVEN}$) have setup and hold time constraints to the port A clock (CLKA) and the port B parity generate select (PGB) and ODD/$\overline{EVEN}$ have setup and hold-time constraints to the port B clock (CLKB). These timing constraints only apply for a rising clock edge used to read a new long word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port B bus (B0-B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port A bus (A0-A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port chip select ($\overline{CSA}$, $\overline{CSB}$) is LOW, enable (ENA, ENB) is HIGH, write/read select (W/$\overline{RA}$, W/$\overline{RB}$) input is LOW, the mail register is selected (MBA is HIGH for port A; both SIZ0 and SIZ1 are HIGH for port B), and port parity generate select (PGA, PGB) is HIGH. Generating parity for mail register data does not change the contents of the register.

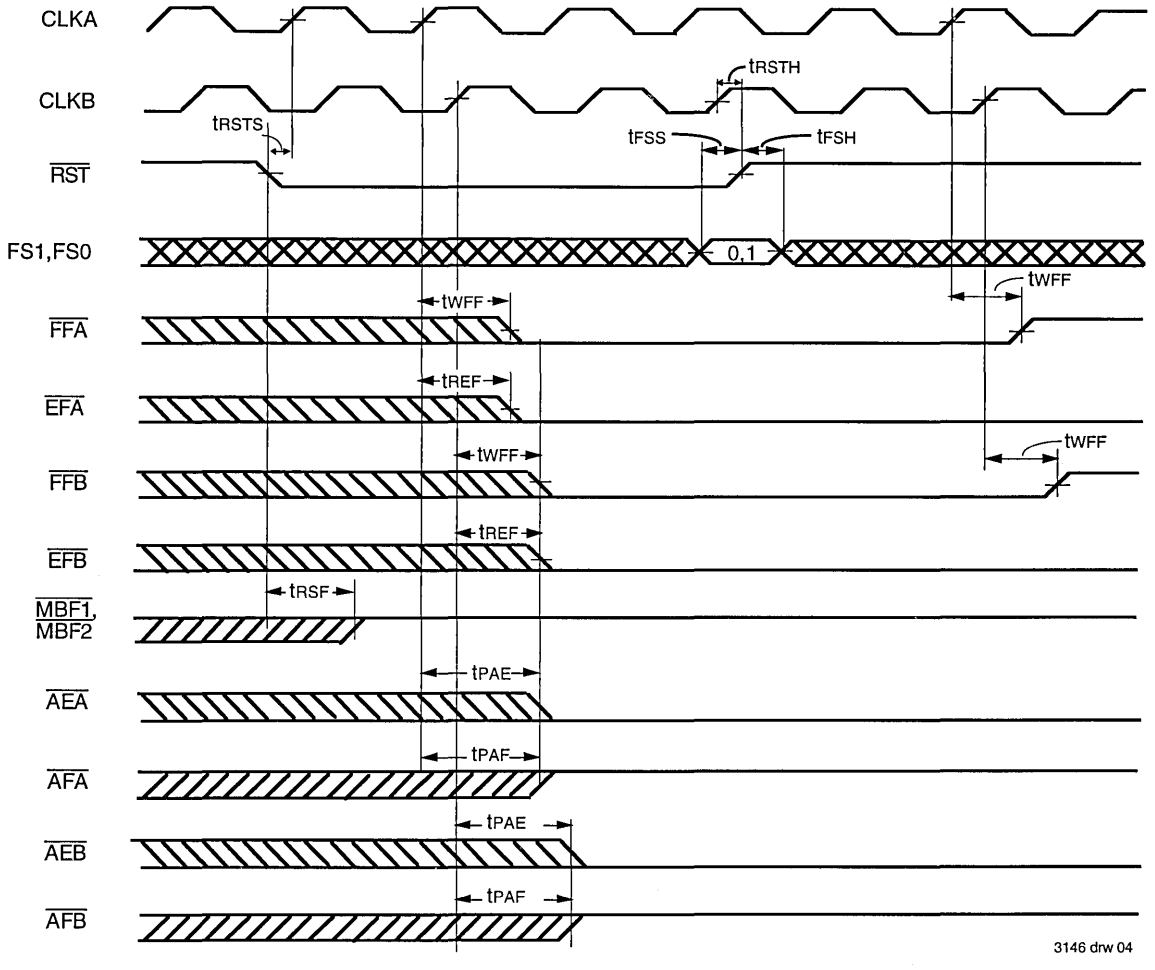
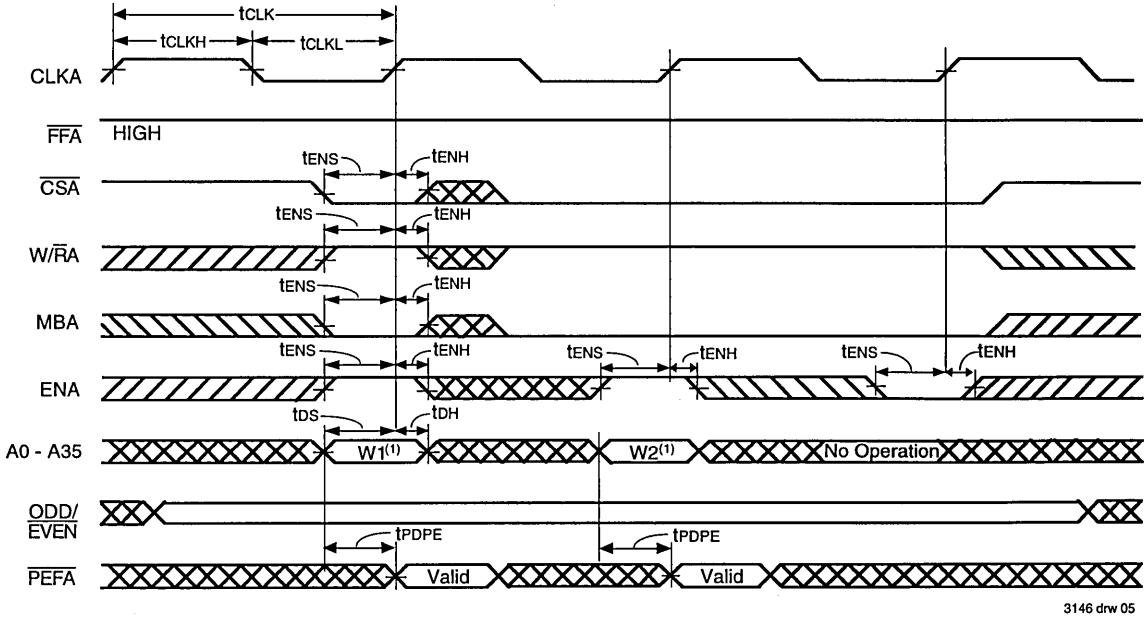
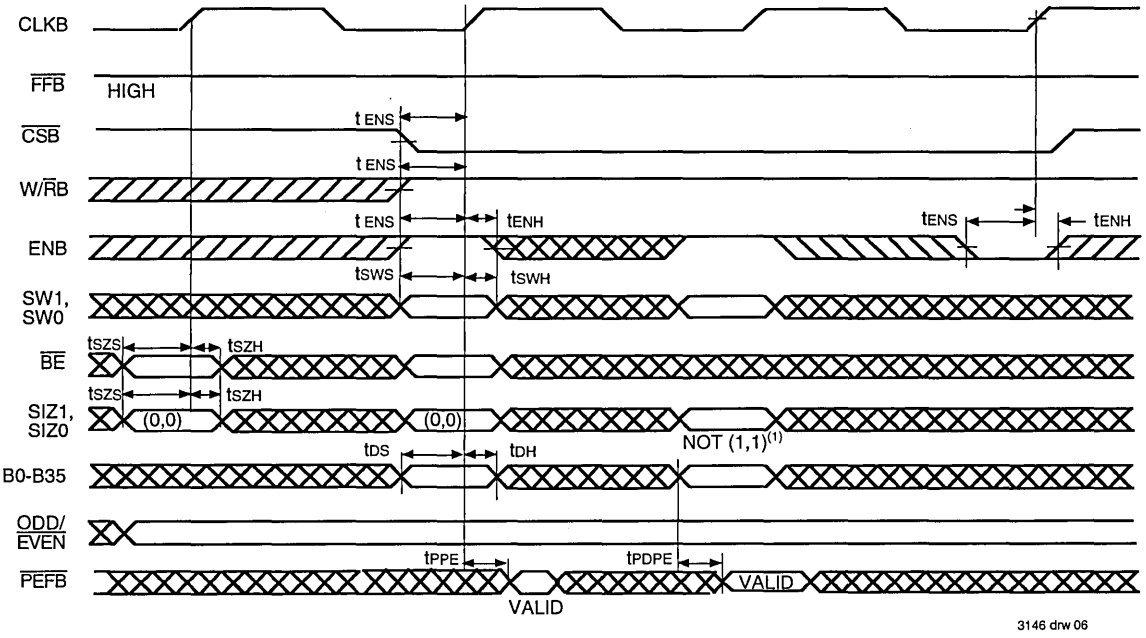


Figure 4. Device Reset Loading the X Register with the Value of Eight



NOTE:
1. Written to FIFO1.

Figure 5. Port-A Write Cycle Timing for FIFO1

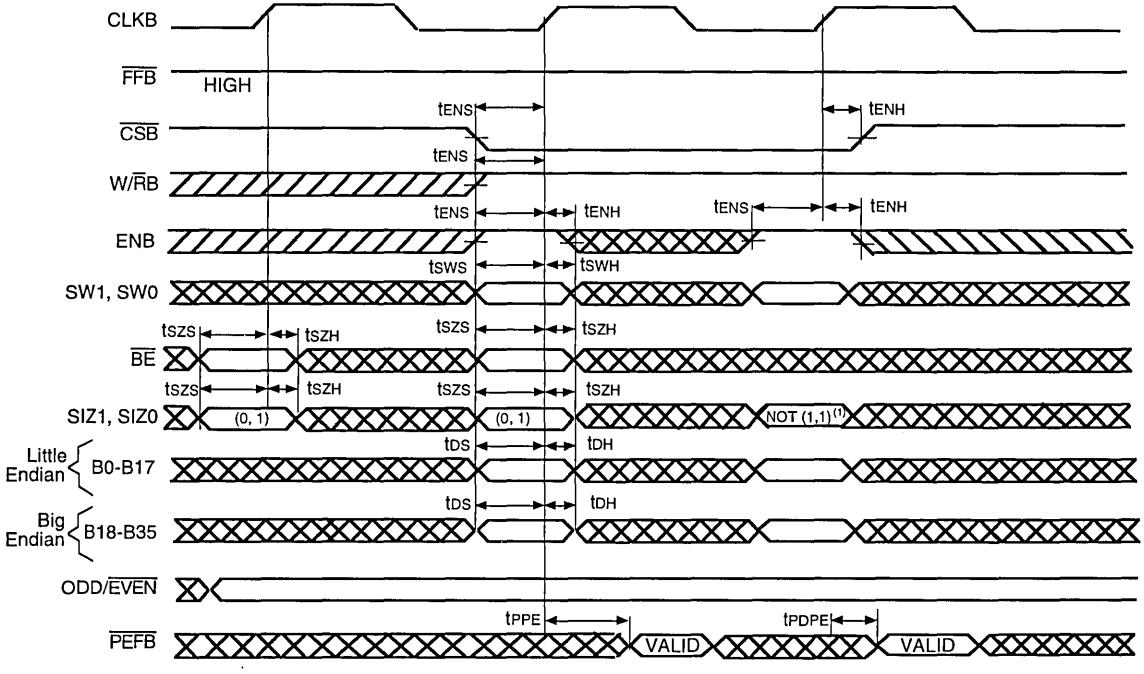


NOTE:
1. SIZ0 = HIGH and SIZ1 = HIGH writes data to the mail2 register

DATA SWAP TABLE FOR LONG-WORD WRITES TO FIFO2

SWAP MODE		DATA WRITTEN TO FIFO2				DATA READ FROM FIFO2			
SW1	SW0	B35-27	B26-18	B17-B9	B8-B0	A35-27	A26-A18	A17-A9	A8-A0
L	L	A	B	C	D	A	B	C	D
L	H	D	C	B	A	A	B	C	D
H	L	C	D	A	B	A	B	C	D
H	H	B	A	D	C	A	B	C	D

Figure 6. Port-B Long-Word Write Cycle Timing for FIFO2



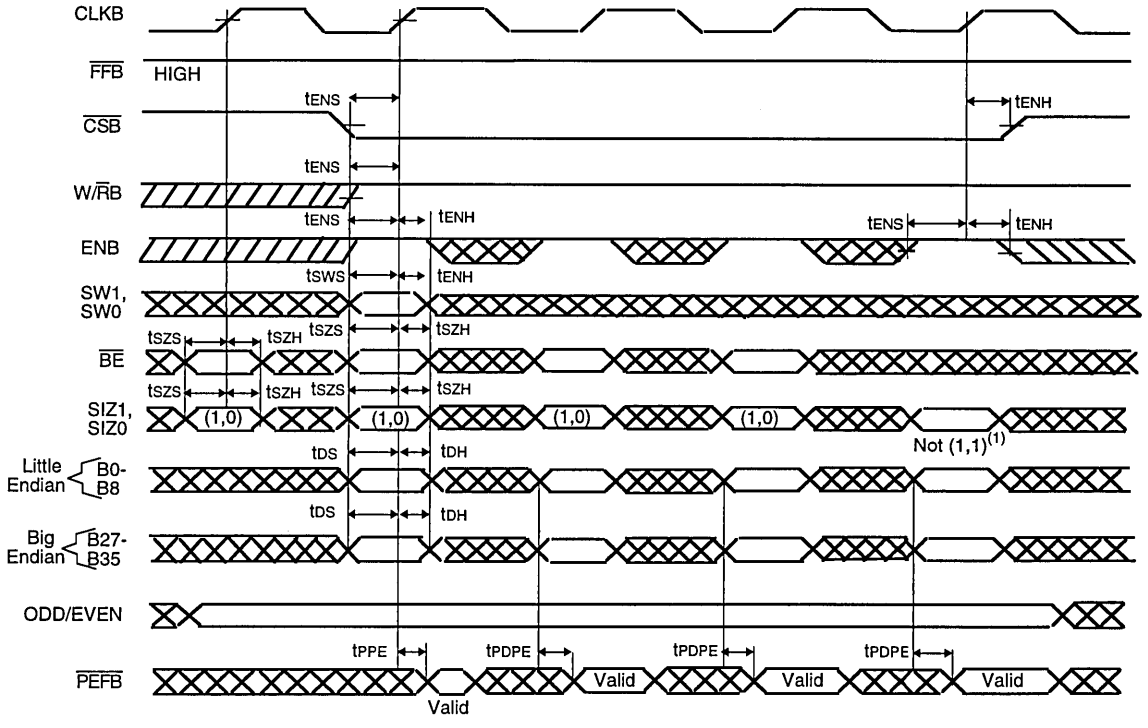
3146 drw 07

NOTES:
1. SIZ0 = HIGH and SIZ1 = HIGH writes data to the mail2 register.
2. $\overline{PEFB}$ indicates parity error for the following bytes: B35-B27 and B26-B18 for big-endian bus, and B17-B9 and B-8-B0 for little-endian bus.

DATA SWAP TABLE FOR WORD WRITES TO FIFO2

SWAP MODE		WRITE NO.	DATA WRITTEN TO FIFO2				DATA READ FROM FIFO2			
			BIG ENDIAN		LITTLE ENDIAN					
SW1	SW0		B35-27	B26-18	B17-B9	B8-B0	A35-27	A26-A18	A17-A9	A8-A0
L	L	1	A	B	C	D	A	B	C	D
		2	C	D	A	B				
L	H	1	D	C	B	A	A	B	C	D
		2	B	A	D	C				
H	L	1	C	D	A	B	A	B	C	D
		2	A	B	C	D				
H	H	1	B	A	D	C	A	B	C	D
		2	D	C	B	A				

Figure 7. Port-B Word Write Cycle Timing for FIFO2



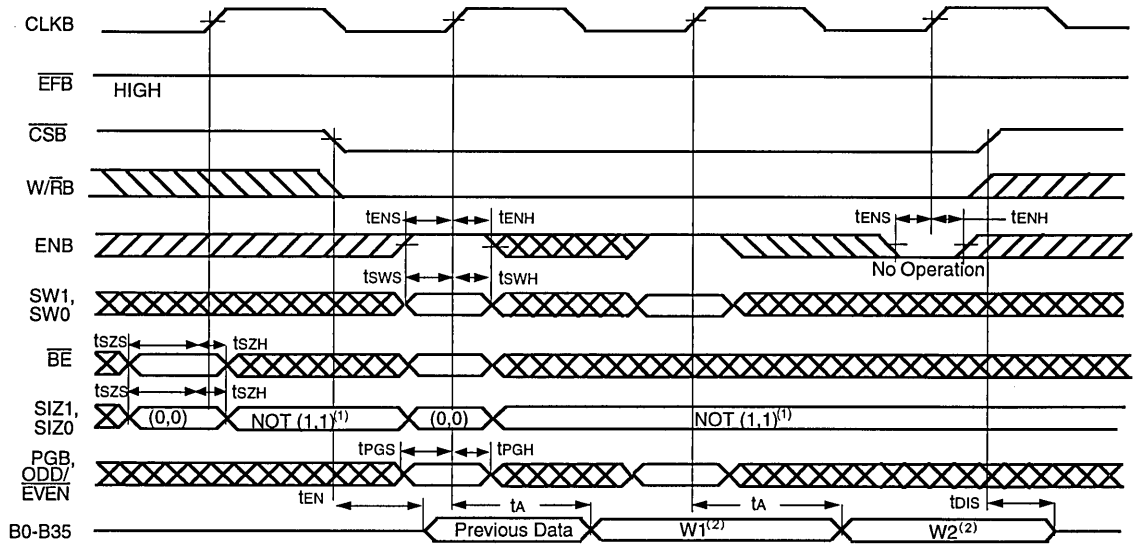
NOTES:
1. SIZ0 = HIGH amd SIZ1 = HIGH writes data to the mail2 register.
2. PEFB indicates parity error for the following bytes: B35—B27 for big-endian bus and B17—B9 for little-endian bus.

Figure 8. Port-B Byte Write Cycle Timing for FIFO2

DATA SWAP TABLE FOR BYTE WRITES TO FIFO2

SWAP MODE		WRITE NO.	DATA WRITTEN TO FIFO2		DATA READ FROM FIFO2			
			BIG ENDIAN	LITTLE ENDIAN				
SW1	SW0		B35-B27	B8-80	A35-A27	A26-A18	A17-A9	A8-A0
L	L	1	A	D	A	B	C	D
		2	B	C				
		3	C	B				
		4	D	A				
L	H	1	D	A	A	B	C	D
		2	C	B				
		3	B	C				
		4	A	D				
H	L	1	C	B	A	B	C	D
		2	D	A				
		3	A	D				
		4	B	C				
H	H	1	B	C	A	B	C	D
		2	A	D				
		3	D	A				
		4	C	B				

Figure 8. Port-B Byte Write Cycle Timing for FIFO2 (continued)



3146 drw 09

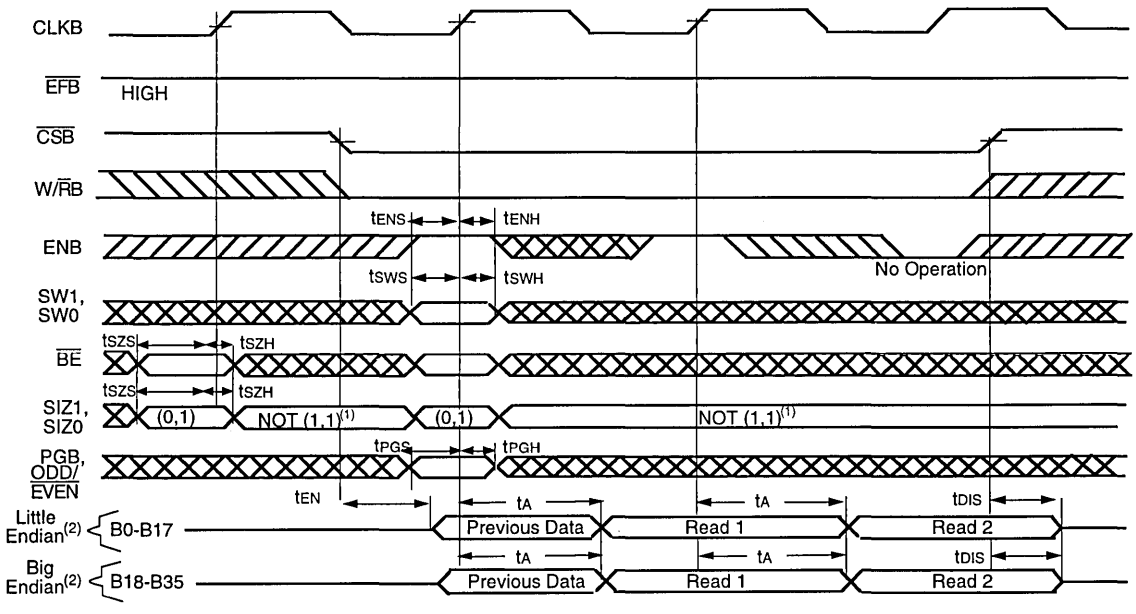
NOTES:
1. SIZ0 = HIGH and SIZ1 = HIGH selects the mail1 register for output on B0-B35.
2. Data read from FIFO1.

5

DATA SWAP TABLE FOR FIFO LONG-WORD READS FROM FIFO1

DATA WRITTEN TO FIFO1				SWAP MODE		DATA READ FROM FIFO1			
A35-A27	A26-A18	A17-A9	A8-A0	SW1	SW0	B35-B27	B26-B18	B17-B9	B8-B0
A	B	C	D	L	L	A	B	C	D
A	B	C	D	L	H	D	C	B	A
A	B	C	D	H	L	C	D	A	B
A	B	C	D	H	H	B	A	D	C

Figure 9. Port-B Long-Word Read Cycle Timing for FIFO1



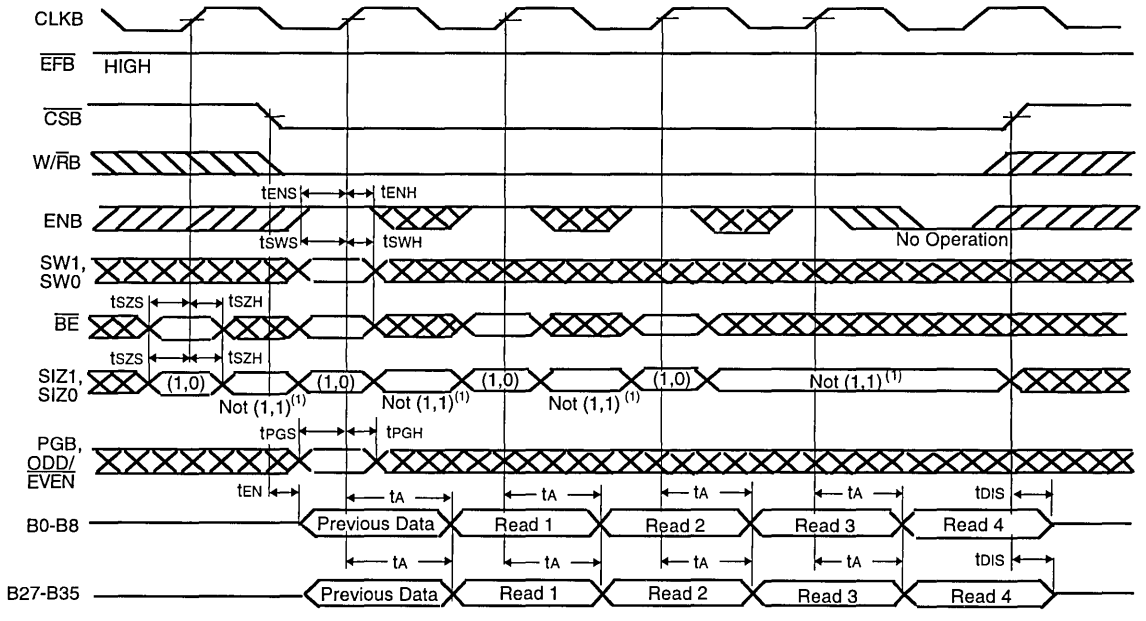
3146 drw 10

NOTES:
1. SIZ0 = HIGH and SIZ1 = HIGH selects the mail1 register for output on B0-B35.
2. Unused word B0-B17 or B18-B35 holds last FIFO1 output register data for word-size reads.

DATA SWAP TABLE FOR WORD READS FROM FIFO1

DATA WRITTEN TO FIFO1				SWAP MODE		READ NO.	DATA READ FROM FIFO1			
							BIG ENDIAN		LITTLE ENDIAN	
A35-A27	A26-A18	A17-A9	A8-A0	SW1	SW0		B35-B27	B26-B18	B17-B9	B8-B0
A	B	C	D	L	L	1 2	A C	B D	C A	D B
A	B	C	D	L	H	1 2	D B	C A	B D	A C
A	B	C	D	H	L	1 2	C A	D B	A C	B D
A	B	C	D	H	H	1 2	B D	A C	D B	C A

Figure 10. Port-B Word Read Cycle Timing for FIFO1



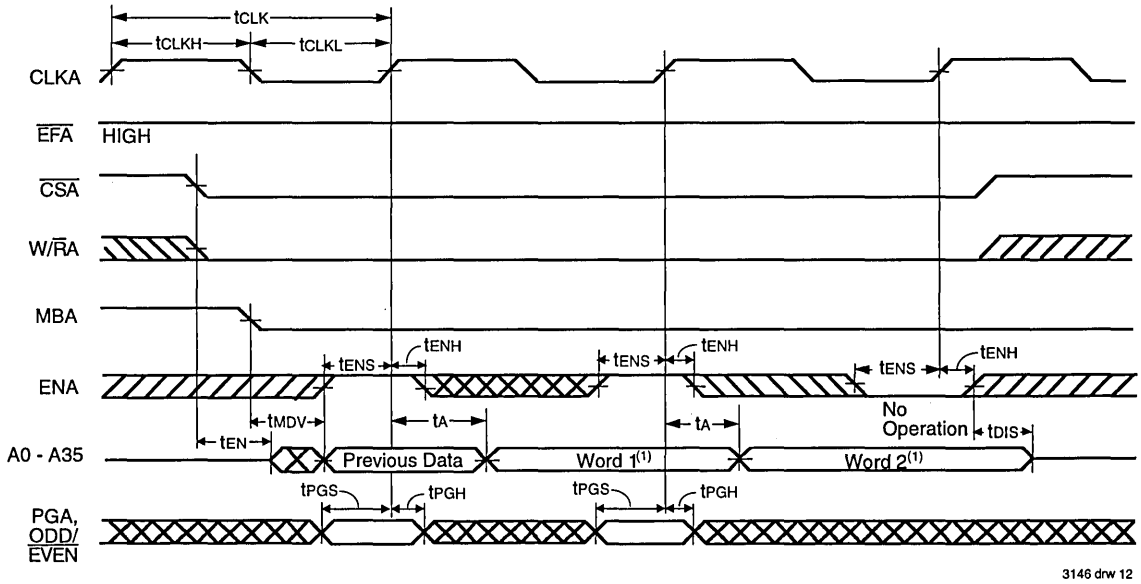
NOTES:
1. SIZ0 = HIGH and SIZ1 = HIGH selects the mail1 register for output on B0-B35.
2. Unused bytes hold last FIFO1 output regisger data for byte-size reads.

3146 drw 11

DATA SWAP TABLE FOR BYTE READS FROM FIFO1

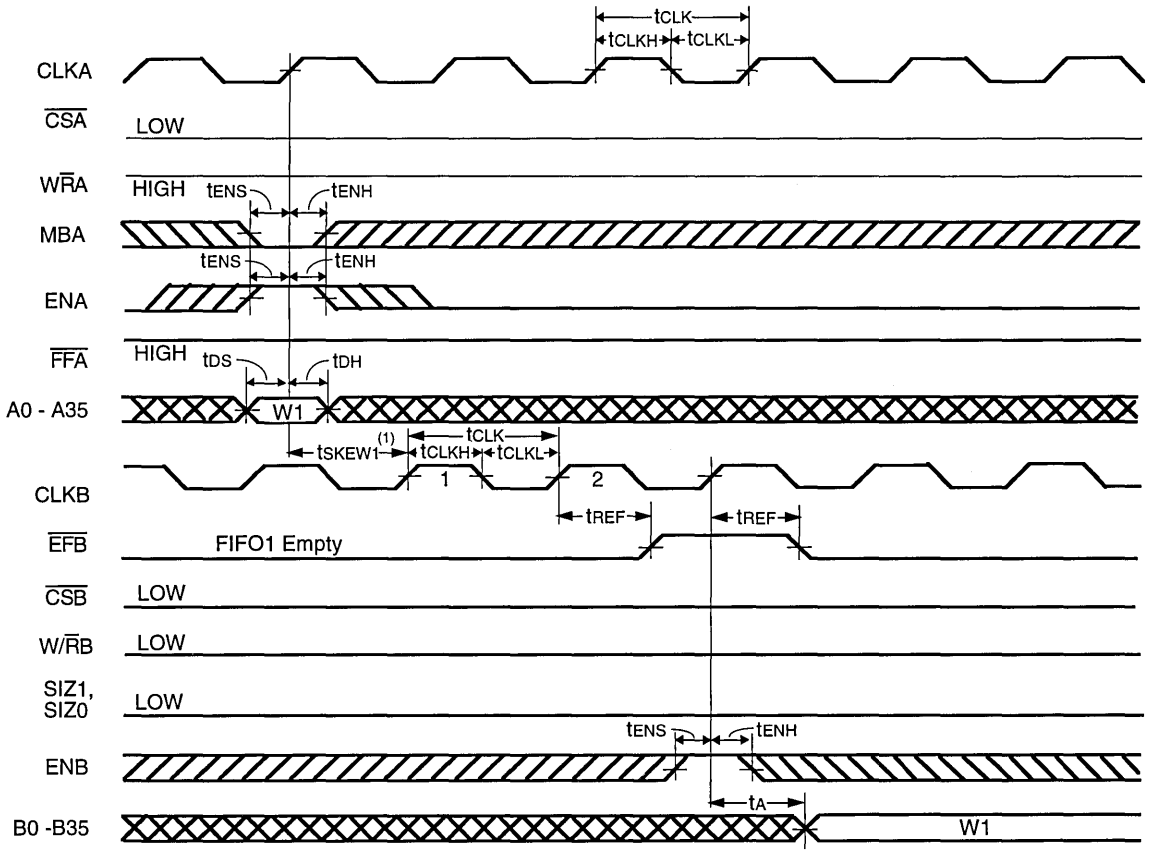
DATA WRITTEN TO FIFO 1				SWAP MODE		READ NO.	DATA READ FROM FIFO 1	
							BIG ENDIAN	LITTLE ENDIAN
A35-A27	A26-A18	A17-A9	A8-A0	SW1	SW0		B35-B27	B8-B0
A	B	C	D	L	L	1 2 3 4	A B C D	D C B A
A	B	C	D	L	H	1 2 3 4	D C B A	A B C D
A	B	C	D	H	L	1 2 3 4	C D A B	B A D C
A	B	C	D	H	H	1 2 3 4	B A D C	C D A B

Figure 11. Port-B Byte Read Cycle Timing for FIFO1



NOTE:
1. Read from FIFO2..

Figure 12. Port-A Read Cycle Timing for FIFO2

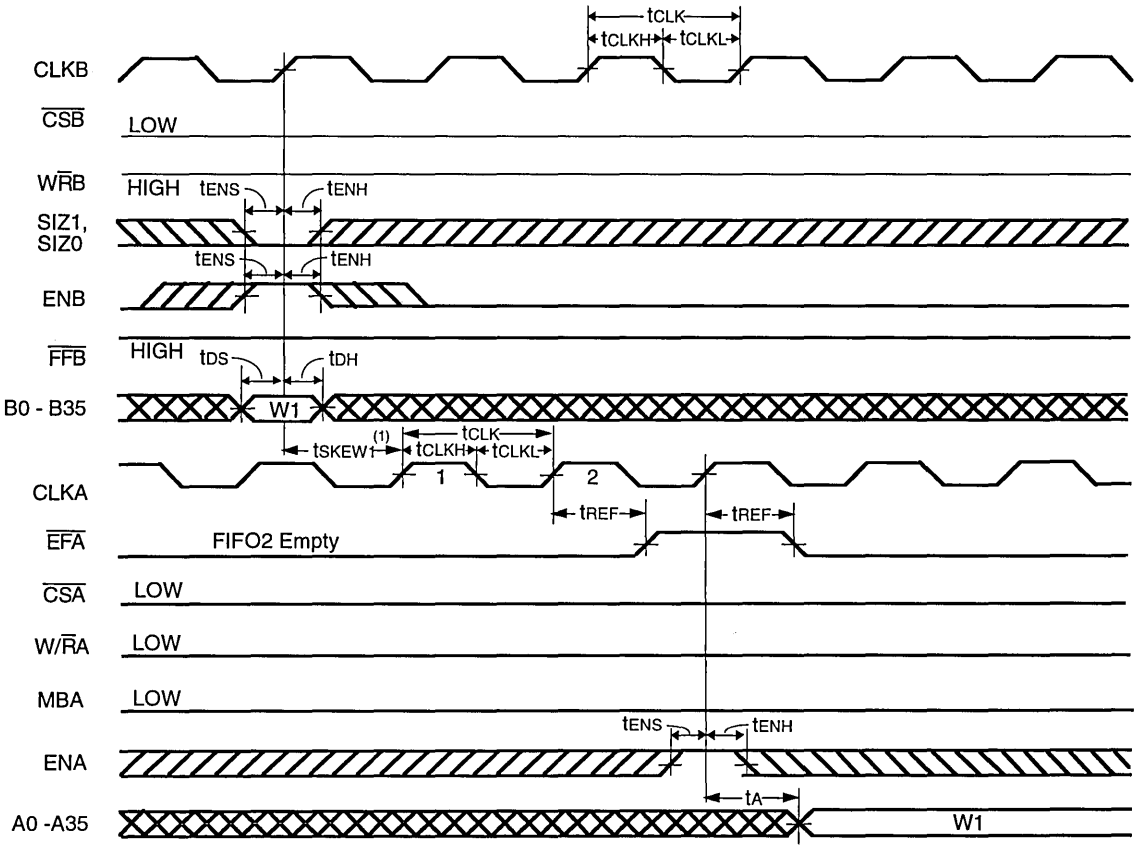


3146 drw 13

NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of $\overline{EFB}$ HIGH may occur one CLKB cycle later than shown.
2. Port-B size of long word is selected for FIFO1 read by SIZ1 = LOW, SIZ0 = LOW. If port-B size is word or byte, $\overline{EFB}$ is set LOW by the last word or byte read from FIFO1, respectively.

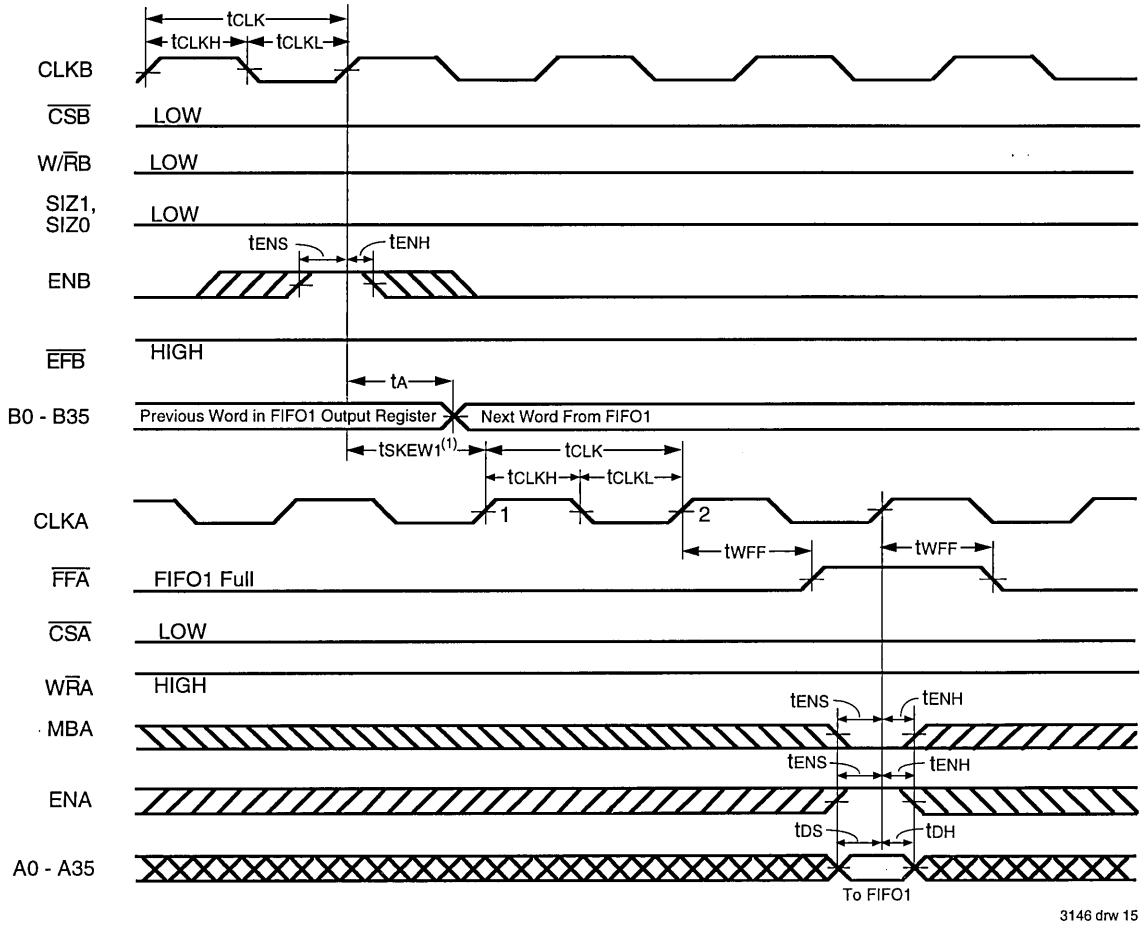
Figure13. $\overline{EFB}$ Flag Timing and First Data Read when FIFO1 is Empty



3146 drw 14

NOTES:
1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{EFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of $\overline{EFA}$ HIGH may occur one CLKA cycle later than shown.
2. Port B size of long word is selected for FIFO2 write by SIZ1 = LOW, SIZ0 = LOW. If port B size is word or byte t_{SKEW1} is referenced to the rising CLKB edge that writes the last word or byte of the long word, respectively.

Figure 14. $\overline{EFA}$ Flag Timing and First Data Read when FIFO2 is Empty

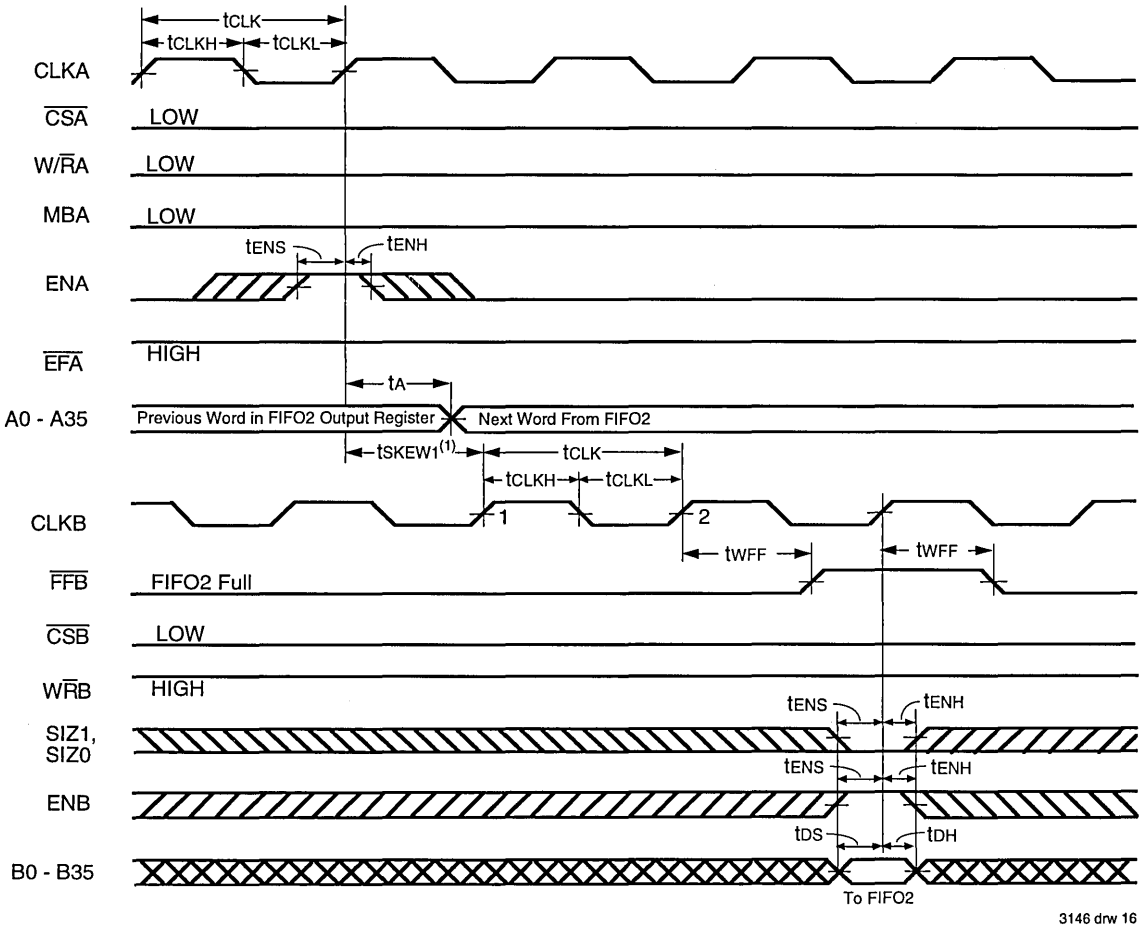


3146 drw 15

NOTES:

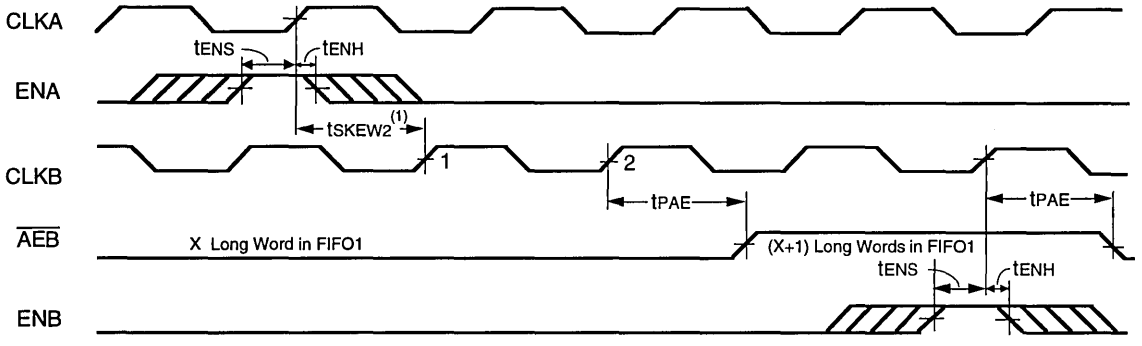
1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then $\overline{FFA}$ may transition HIGH one CLKA cycle later than shown.
2. Port B size of long word is selected for FIFO1 read by SIZ1 = LOW, SIZ0 = LOW. If port B size is word or byte, t_{SKEW1} is referenced from the rising CLKB edge that reads the last word or byte of the long word, respectively.

Figure 15. $\overline{FFA}$ Flag Timing and First Available Write when FIFO1 is Full.



NOTES:
1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{FFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then $\overline{FFB}$ may transition HIGH one CLKB cycle later than shown.
2. Port B size of long word is selected for FIFO2 write by SIZ1 = LOW, SIZ0 = LOW. If port B size is word or byte, $\overline{FFB}$ is set LOW by the last word or byte write of the long word, respectively.

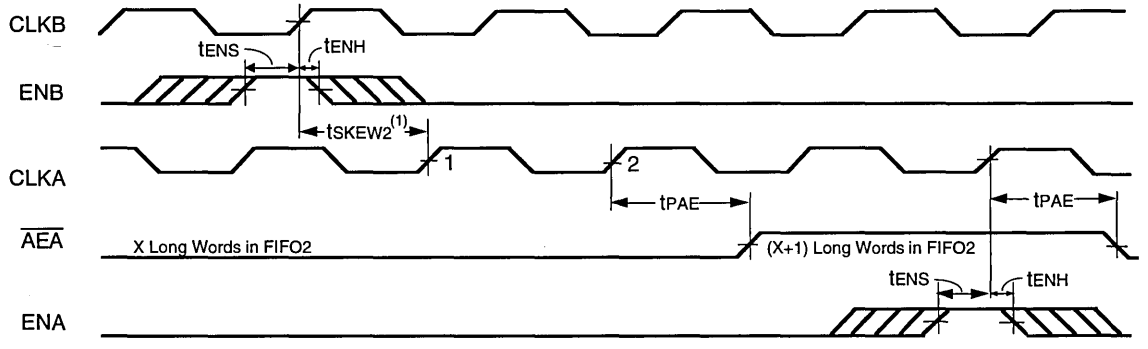
Figure 16. $\overline{FFB}$ Flag Timing and First Available Write when FIFO2 is Full



3146 drw 17

NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AEB}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO1 read ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = LOW, MBB = LOW).
3. Port B size of long word is selected for FIFO1 read by SIZ1 = LOW, SIZ0 = LOW. If port B size is word or byte, $\overline{AEB}$ is set LOW by the first word or byte read of the long word, respectively.

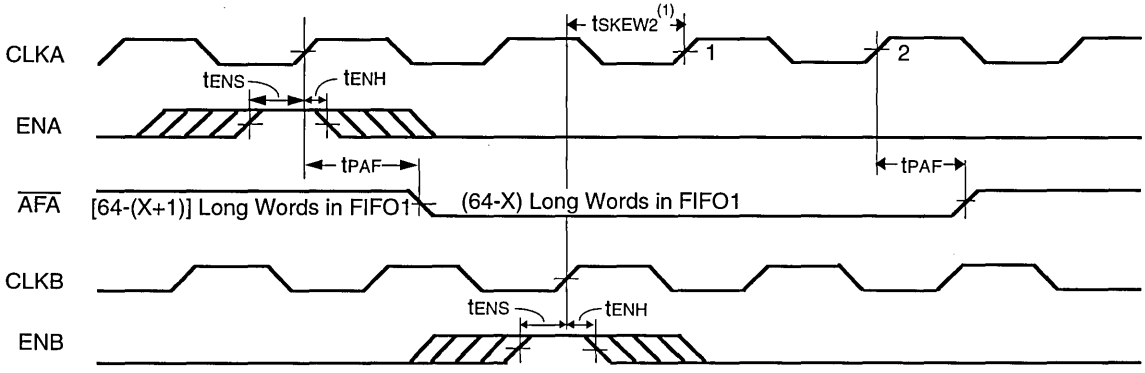
Figure 17. Timing for $\overline{AEB}$ when FIFO1 is Almost Empty



3146 drw 18

NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW2}, then $\overline{AEA}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO2 Write ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = HIGH, MBB = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW).
3. Port B size of long word is selected for FIFO2 write by SIZ1 = LOW, SIZ0 = LOW. If port B size is word or byte, t_{SKEW2} is referenced from the rising CLKB edge that writes the last word or byte of the long word, respectively.

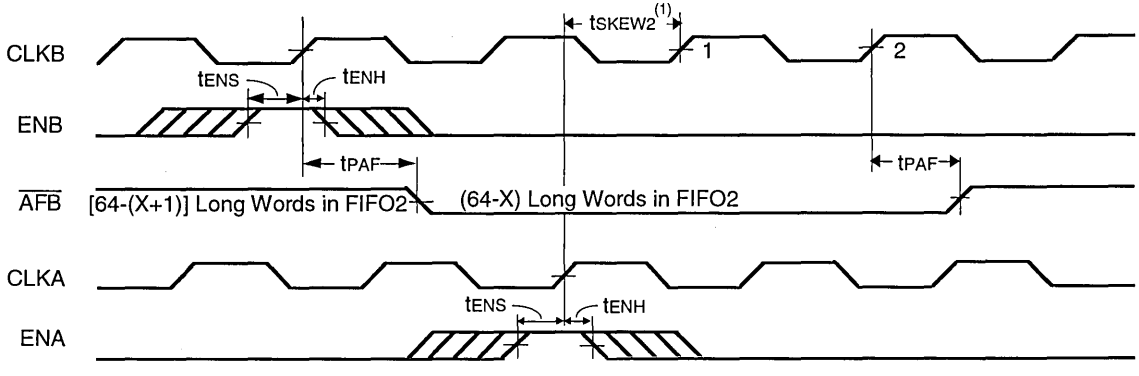
Figure 18. Timing for $\overline{AEA}$ when FIFO2 is Almost Empty



3146 drw 19

NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AFA}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO1 read ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = LOW, MBB = LOW).
3. Port B size of long word is selected for FIFO1 read by SIZ1 = LOW, SIZ0 = LOW. If port B size is word or byte, t_{SKEW2} is referenced from the first word or byte read of the long word, respectively.

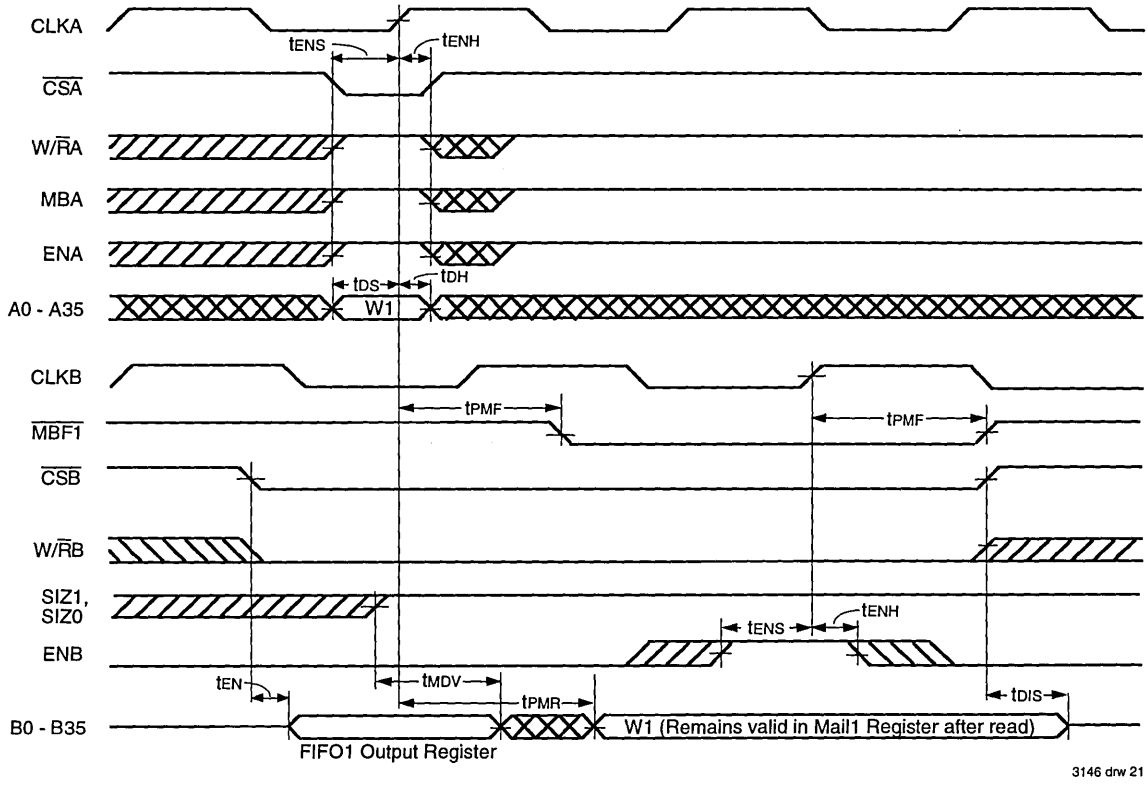
Figure 19. Timing for $\overline{AFA}$ when FIFO1 is Almost Full



3146 drw 20

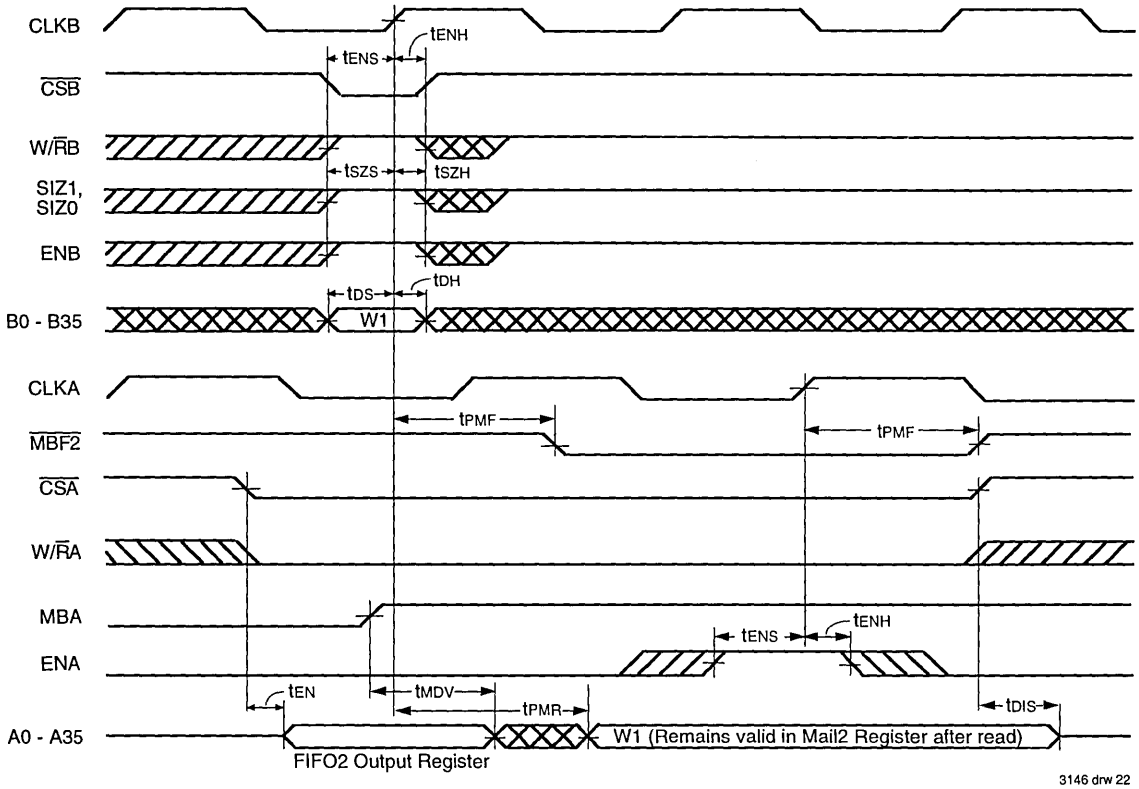
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW2}, then $\overline{AFB}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO2 Write ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = HIGH, MBB = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW).
3. Port B size of long word is selected for FIFO2 write by SIZ1 = LOW, SIZ0 = LOW. If port B size is word or byte, $\overline{AFB}$ is set LOW by the last word or byte read of the long word, respectively.

Figure 20. Timing for $\overline{AFB}$ when FIFO2 is Almost Full



NOTE:
1. Port B parity generation off (PGB = LOW).

Figure 21. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag



NOTE:
1. Port-A parity generation off (PGA = LOW).

Figure 22. Timing for Mail2 Register and $\overline{MBF2}$ Flag

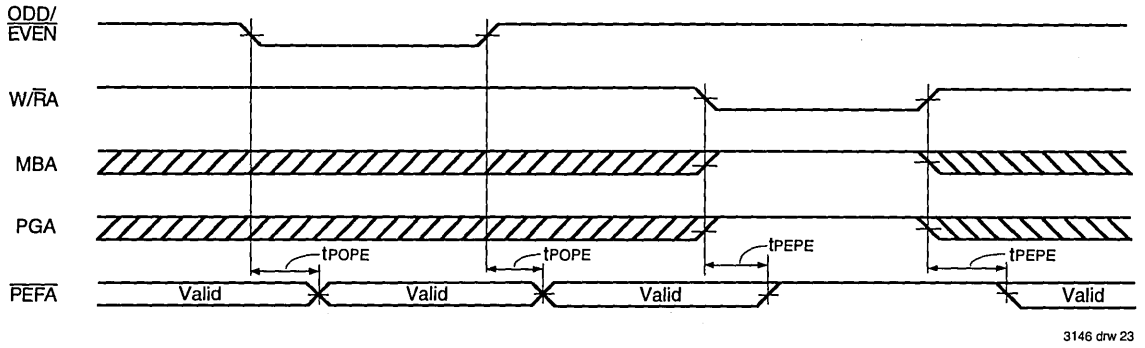


Figure 23. ODD/EVEN. W/RA, MBA, and PGA to PEFA Timing

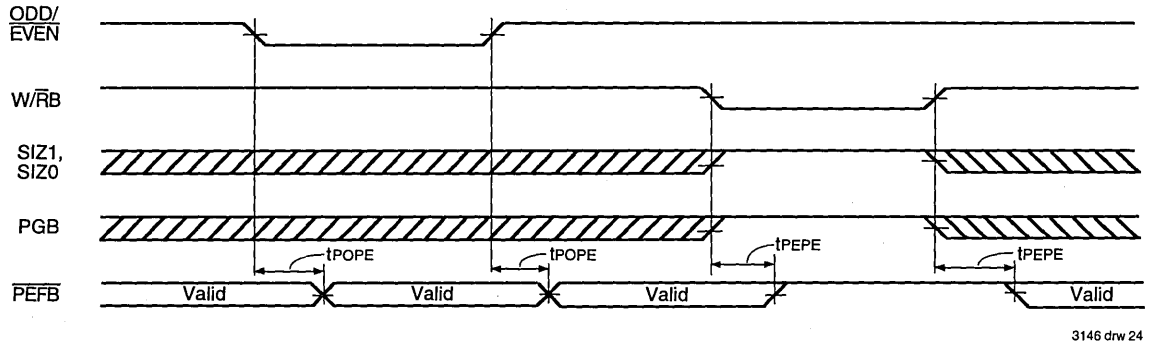
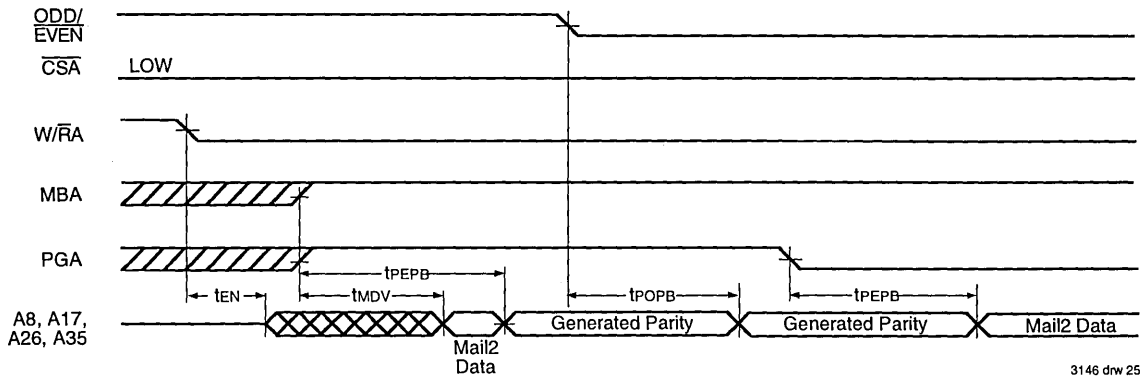
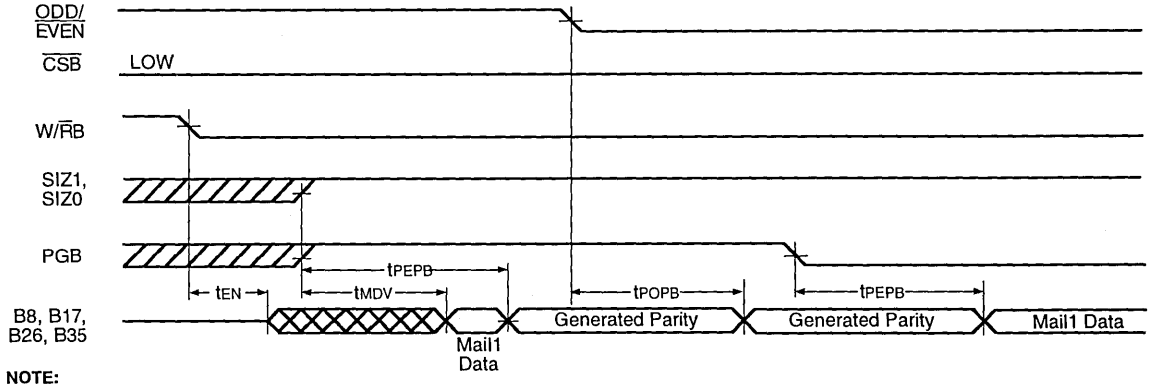


Figure 24. ODD/EVEN. W/RB, SIZ1, SIZ0, and PGB to PEFB Timing



NOTE:
1. ENA is HIGH.

Figure 25. Parity Generation Timing when Reading from the Mail2 Register



NOTE:
1. ENB is HIGH.

Figure 26. Parity Generation Timing when Reading from the Mail1 Register

TYPICAL CHARACTERISTICS

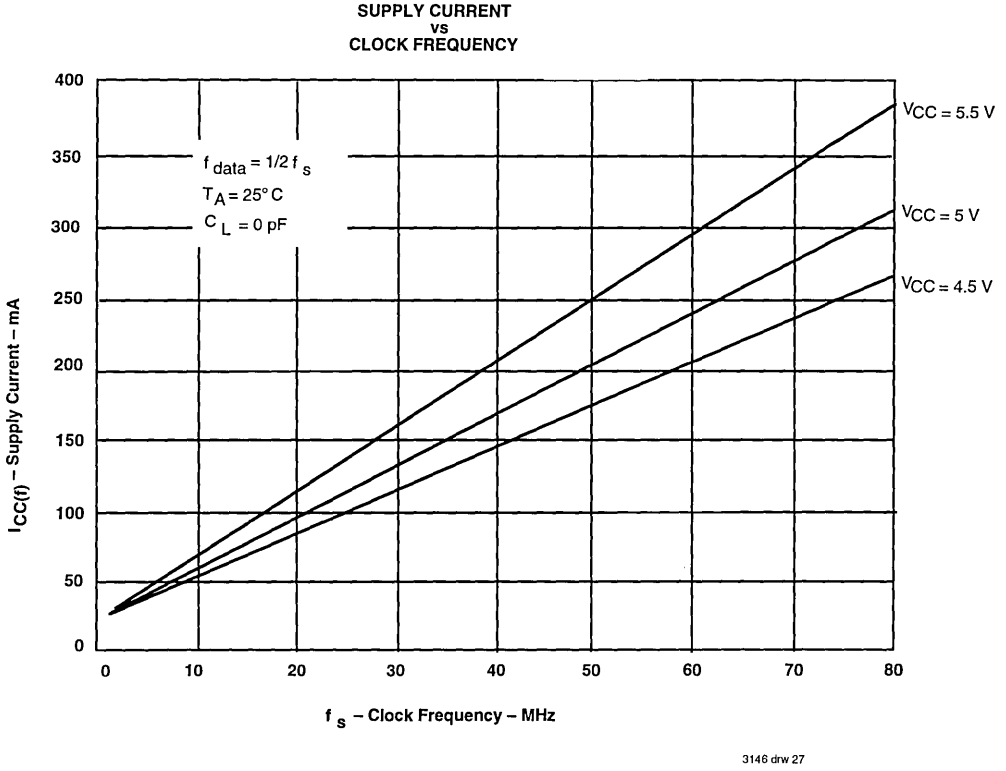


Figure 27

CALCULATING POWER DISSIPATION

The $I_{CC(f)}$ current for the graph in Figure 27 was taken while simultaneously reading and writing the FIFO on the IDT723614 with CLKA and CLKB set to fs. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitive lead per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from Figure 28, the maximum power dissipation (P_T) of the IDT723614 can be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times V_{OH}^2 \times f_o)$$

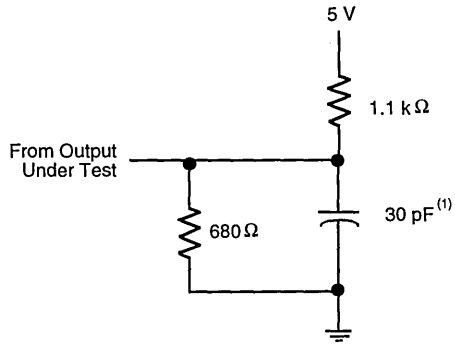
where:

C_L	=	output capacitance load
f_o	=	switching frequency of an output
V_{OH}	=	output high level voltage

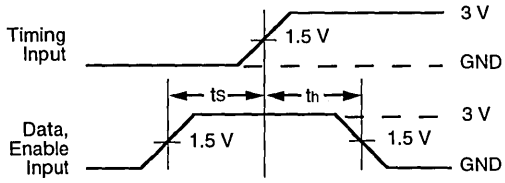
When no reads or writes are occurring on the IDT723614, the power dissipated by a single clock (CLKA or CLKB) input running at frequency fs is calculated by:

$$P_T = V_{CC} \times f_s \times 0.290\ mA/MHz$$

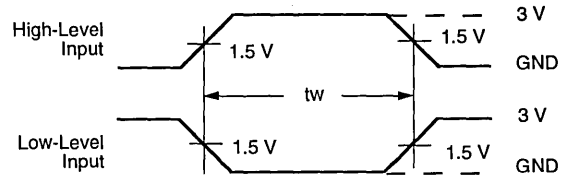
PARAMETER MEASUREMENT INFORMATION



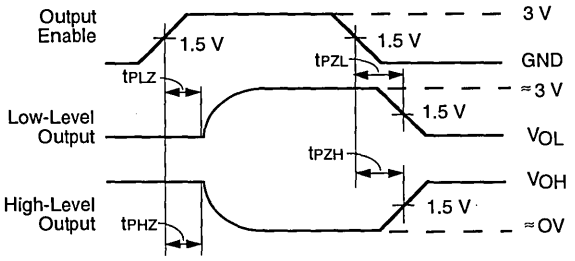
LOAD CIRCUIT



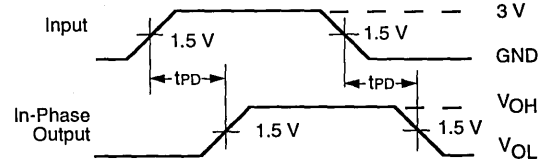
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



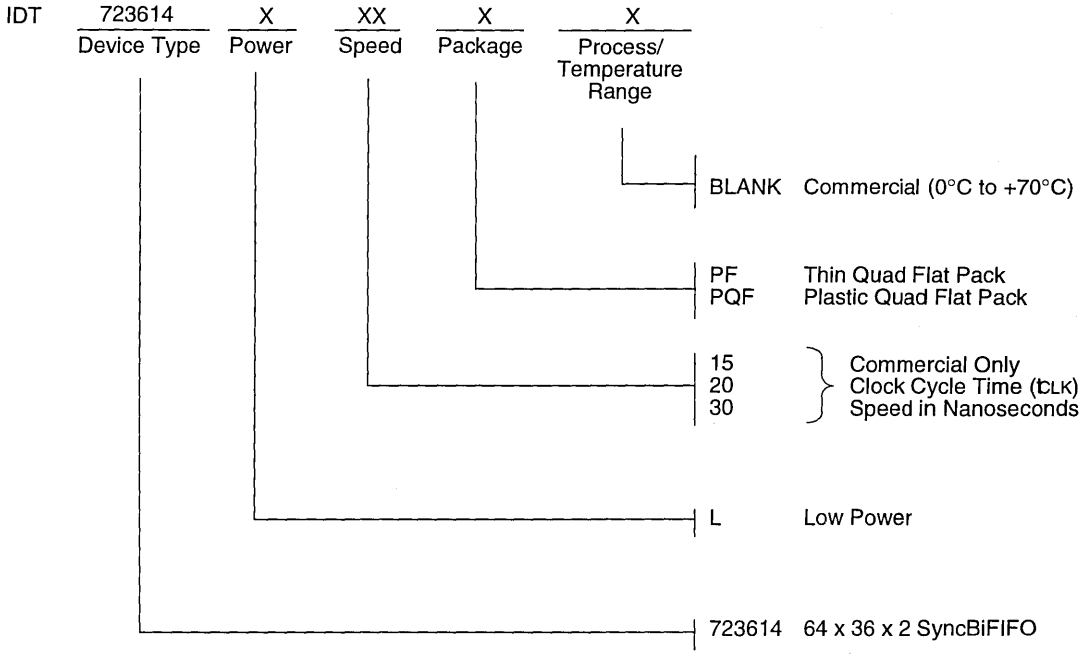
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

3146 drw 28

NOTE:
1. Includes probe and jig capacitance.

Figure 28. Load Circuit and Voltage Waveforms

ORDERING INFORMATION



3146 drw 29

5

Integrated Device Technology, Inc.

CMOS SyncBiFIFO™ 256 x 36 x 2, 512 x 36 x 2, 1024 x 36 x 2

IDT723622
IDT723632
IDT723642

Advance information for the IDT723622
Final for the IDT723632
Advance information for the IDT723642

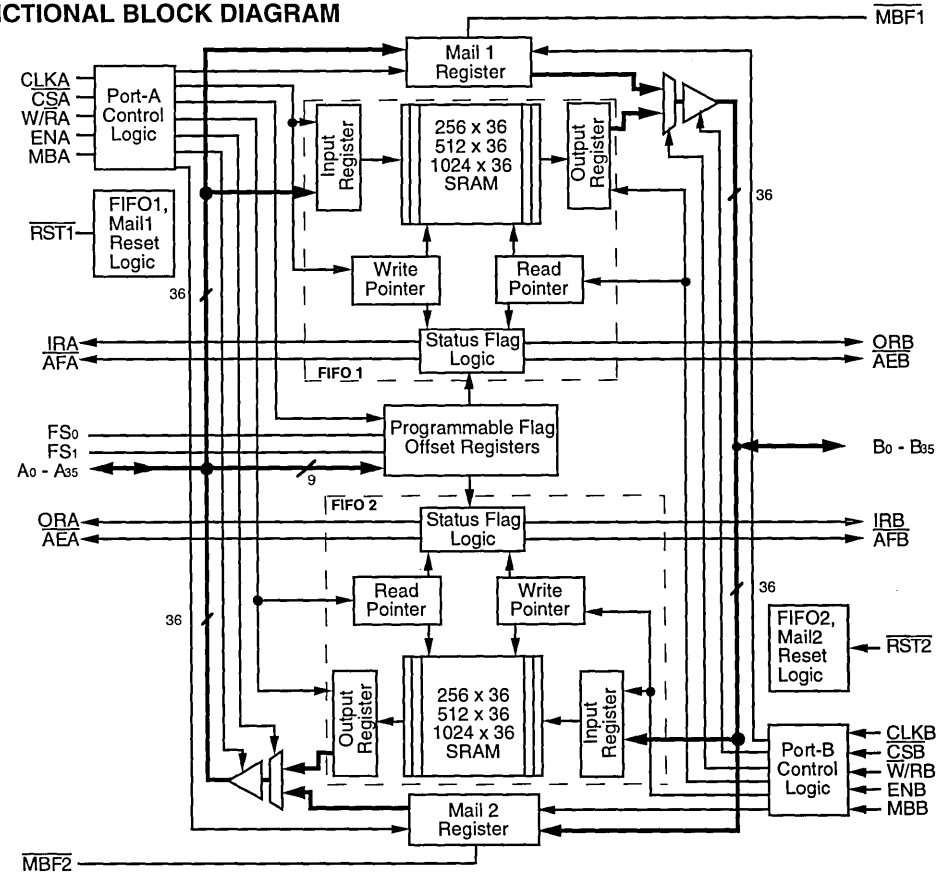
FEATURES:

- Free-running CLKA and CLKB may be asynchronous or coincident (simultaneous reading and writing of data on a single clock edge is permitted)
- Two independent clocked FIFOs buffering data in opposite directions
- Memory storage capacity:
  - IDT723622–256 x 36 x 2
  - IDT723632–512 x 36 x 2
  - IDT723642–1024 x 36 x 2
- Mailbox bypass register for each FIFO
- Programmable Almost-Full and Almost-Empty flags
- Microprocessor Interface Control Logic
- IRA, ORA, $\overline{AEA}$, and $\overline{AFA}$ flags synchronized by CLKA
- IRB, ORB, $\overline{AEB}$, and $\overline{AFB}$ flags synchronized by CLKB
- Supports clock frequencies up to 67MHz
- Fast access times of 11ns
- Available in 132-pin Plastic Quad Flatpack (PQF) or space-saving 120-pin Thin Quad Flatpack (PF)
- Low-power 0.8-Micron Advanced CMOS technology

DESCRIPTION:

The IDT723622/723632/723642 is a monolithic, high-speed, low-power, CMOS Bidirectional Synchronous (clocked) FIFO memory which supports clock frequencies up to 67MHz and have read access times as fast as 11ns. Two independent

FUNCTIONAL BLOCK DIAGRAM



3022 drw 01

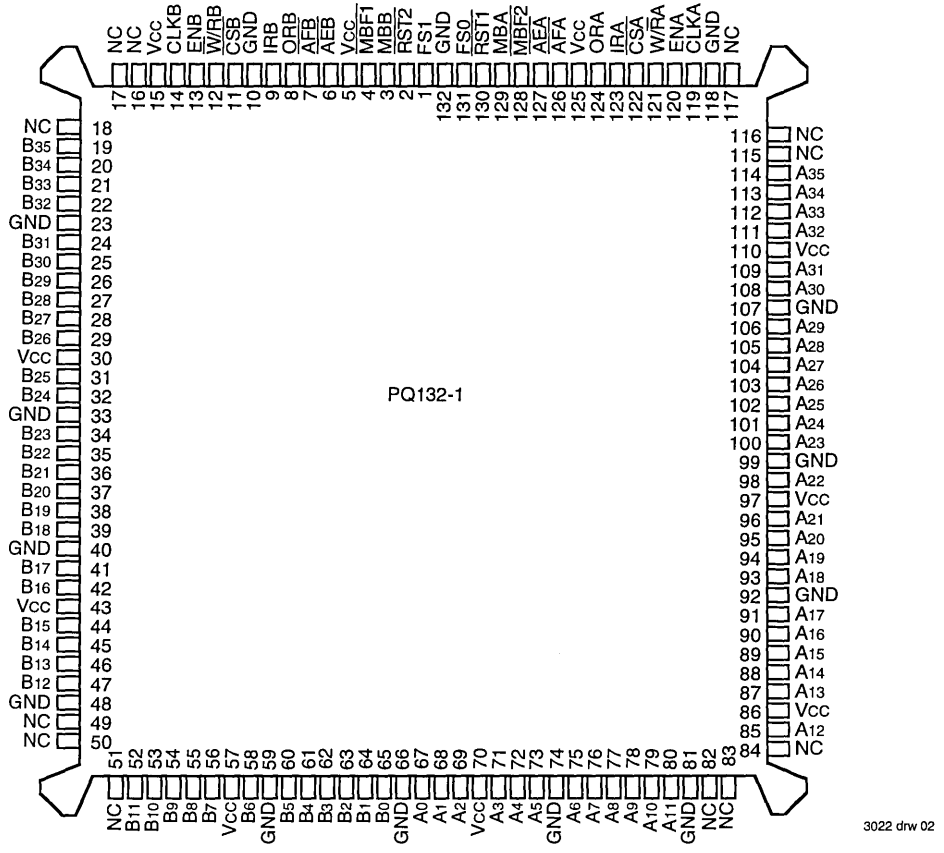
DESCRIPTION (CONTINUED)

256/512/1024x36 dual-port SRAM FIFOs on board each chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programable flags (almost Full and almost Empty) to indicate when a selected number of words is stored in memory. Communication between each port may bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Two or more devices may be used in parallel to create wider data paths.

The IDT723622/723632/723642 is a synchronous (clocked) FIFO, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The Input Ready (IRA, IRB) and Almost-Full ($\overline{AFA}$, $\overline{AFB}$) flags of a FIFO are two-stage synchronized to the port clock that writes data into its array. The Output Ready (ORA, ORB) and Almost-Empty ($\overline{AEA}$, $\overline{AEB}$) flags of a FIFO are two-stage synchronized to the port clock that reads data from its array. Offset values for the Almost-Full and Almost-Empty flags of both FIFOs can be programmed from Port A.

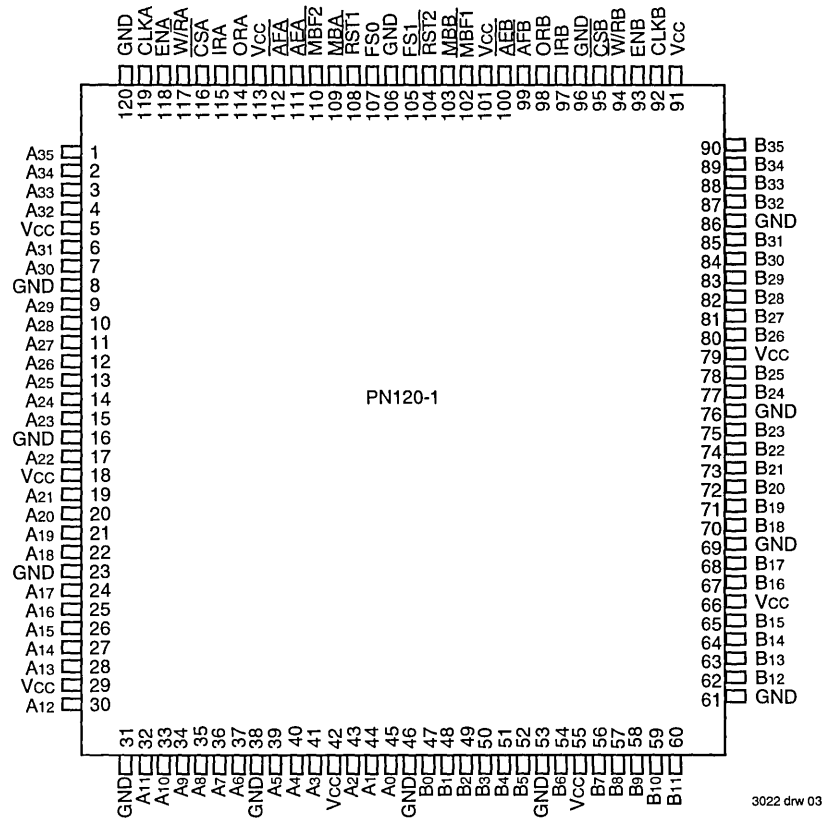
PIN CONFIGURATION



PQF Package
TOP VIEW

NOTES:
1. NC – no internal connection
2. Uses Yamaichi socket IC51-1324-828

PIN CONFIGURATION



3022 drw 03

TQFP
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
A0-A35	Port-A Data	I/0	36-bit bidirectional data port for side A.
$\overline{AEA}$	Port-A Almost -Empty Flag	O (Port A)	Programmable almost-empty flag synchronized to CLKA. It is LOW when the number of words in FIF02 is less than or equal to the value in the almost-empty A offset register, X2.
$\overline{AEB}$	Port-B Almost -Empty Flag	O (Port B)	Programmable almost-empty flag synchronzed to CLKB. It is LOW when the number of words in FIF01 is less than or equal to the value in the almost-empty B offset register, X1.
$\overline{AFA}$	Port-A Almost -Full Flag	O (Port A)	Programmable almost-full flag synchronized to CLKA. It is LOW when the number of empty locations in FIF01 is less than or equal to the value in the almost-full A offset register, Y1.
$\overline{AFB}$	Port-B Almost -Full Flag	O (Port B)	Programmable almost-full flag synchronized to CLKB. It is LOW when the number of empty locations in FIF02 is less than or equal to the value in the almost-full B offset register, Y2.
B0 - B35	Port-B Data	I/O	36-bit bidirectional data port for side B.
CLKA	Port-A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port A and can be asynchronous or coincident to CLKB. IRA, ORA, $\overline{AFA}$, and $\overline{AEA}$ are all synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port-B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through port B and can be asynchronous or coincident to CLKA. IRB, ORB, $\overline{AFB}$, and $\overline{AEB}$ are synchronized to the LOW-to-HIGH transition of CLKB.
$\overline{CSA}$	Port-A Chip Select	I	$\overline{CSA}$ must be LOW to enable to LOW-to-HIGH transition of CLKA to read or write on port A. The AO-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port-B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on port B. The BO- B35 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
ENA	Port-A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port A.
ENB	Port-B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on port B.
FS1, FS0	Flag Offset Selects	I	The LOW-to-HIGH transition of a FIFO's reset input latches the values of FSO and FS1. If either FSO or FS1 is HIGH when a reset input goes HIGH, one of the three preset values is selected as the offset for the FIFOs almost-full and almost-empty flags. If both FIFOs are reset simultaneously and both FSO and FS1 are LOW when RST1 and RST2 go HIGH, the first four writes to FIFO1 almost empty offsets for both FIFOs.
IRA	Input-Ready Flag	O (Port A)	IRA is synchronized to the LOW-to-HIGH transition of CLKA. When IRA is LOW, FIFO1 is full and writes to its array are disabled. IRA is set LOW when FIFO1 is reset and is set HIGH on the second LOW-to-HIGH transition of CLKA after reset.
IRB	Input-Ready Flag	O (Port B)	IRB is synchronized to the LOW-to-HIGH transition of CLKB. When IRB is LOW, FIFO2 is full and writes to its array are disabled. IRB is set LOW when FIFO2 is reset and is set HIGH on the second LOW-to-HIGH transition of CLKB after reset.
MBA	Port-A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a port-A read or write operation. When the AO-A35 outputs are active, a HIGH level on MBA selects data from the mail2 register for output and a LOW level selects FIF02 output-register data for output.

5

PIN DESCRIPTIONS (CONT.)

Symbol	Name	I/O	Description
MBB	Port-B Mailbox Select	I	A HIGH level on MBB chooses a mailbox register for a port-B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register or output and a LOW level selects FIFO1 output-register data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a port-B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH when FIFO1 is reset.
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a port-A read is selected and MBA is HIGH. $\overline{MBF2}$ is also set HIGH when FIFO2 is reset.
ORA	Output-Ready Flag	O (Port A)	ORA is synchronized to the LOW-to-HIGH transition of CLKA. When ORA is LOW, FIFO2 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO2 when ORA is HIGH. ORA is forced LOW when FIFO2 is reset and goes HIGH on the third LOW-to-HIGH transition of CLKA after a word is loaded to empty memory.
ORB	Output-Ready Flag	O (Port B)	ORB is synchronized to the LOW-to-HIGH transition of CLKB. When ORB is LOW, FIFO1 is empty and reads from its memory are disabled. Ready data is present on the output register of FIFO1 when ORB is HIGH. ORB is forced LOW when FIFO1 is reset and goes HIGH on the third LOW-to-HIGH transition of CLKB after a word is loaded to empty memory.
$\overline{RST1}$	FIFO1 Reset	I	To reset FIFO1, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST1}$ is LOW. The LOW-to-HIGH transition of $\overline{RST1}$ latches the status of FSO and FS1 for $\overline{AFA}$ and $\overline{AEB}$ offset selection. FIFO1 must be reset upon power up before data is written to its RAM.
$\overline{RST2}$	FIFO2 Reset	I	To reset FIFO2, four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{RST2}$ is LOW. The LOW-to-HIGH transition of $\overline{RST2}$ latches the status of FSO and FS1 for $\overline{AFB}$ and $\overline{AEA}$ offset selection. FIFO2 must be reset upon power up before data is written to its RAM.
W/$\overline{RA}$	Port-A Write/ Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of CLKA. The AO-A35 outputs are in the HIGH impedance state when W/$\overline{RA}$ is HIGH.
$\overline{W}$/RB	Port-B Write/ Read Select	I	A LOW selects a write operation and a HIGH selects a read operation on port B for a LOW-to-HIGH transition of CLKB. The BO-B35 outputs are in the HIGH impedance state when $\overline{W}$/RB is LOW.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)(1)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	-0.5 to 7	V
V_I(2)	Input Voltage Range	-0.5 to Vcc+0.5	V
V_O(2)	Output Voltage Range	-0.5 to Vcc+0.5	V
I_{IK}	Input Clamp Current (V_I < 0 or V_I > Vcc)	±20	mA
I_{OK}	Output Clamp Current (V_O = < 0 or V_O > Vcc)	±50	mA
I_{OUT}	Continuous Output Current (V_O = 0 to Vcc)	±50	mA
I_{CC}	Continuous Current Through Vcc or GND	±400	mA
T_A	Operating Free Air Temperature Range	0 to 70	°C
T_{STG}	Storage Temperature Range	-65 to 150	°C

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IH}	High-Level Input Voltage	2		V
V_{IL}	Low-Level Input Voltage		0.8	V
I_{OH}	High-Level Output Current		-4	mA
I_{OL}	Low-Level Output Current		8	mA
T_A	Operating Free-Air Temperature	0	70	°C

5

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Parameter	Test Conditions				IDT723622 IDT723632 IDT723642 Commerical tA = 15, 20, 30 ns Min.	Typ.(1)	Max.	Unit
VOH	VCC = 4.5V,	IOH = -4 mA			2.4			V
VOL	VCC = 4.5 V,	IOL = 8 mA					0.5	V
ILI	VCC = 5.5 V,	VI = VCC or 0					±5	µA
ILO	VCC = 5.5 V,	VO = VCC or 0					±5	µA
ICC	VCC = 5.5 V,	VI = VCC -0.2 V or 0					400	µA
ΔICC(2)	VCC = 5.5 V,	One Input at 3.4 V,	$\overline{CSA}$ = VIH	A0-A35		0		mA
	Other Inputs at VCC or GND		$\overline{CSB}$ = VIH	B0-B35		0		
			$\overline{CSA}$ = VIL	A0-A35			1	
			$\overline{CSB}$ = VIL	B0-35			1	
			All Other Inputs				1	
CIN	VI = 0,	f = 1 MHz				4		pF
COUT	VO = 0,	f = 1 MHZ				8		pF

NOTES:
1. All typical values are at VCC = 5V, TA = 25°C.
2. This is the supply current when each input is at least one of the specified TTL voltage levels rather than 0V or VCC.

TIMING REQUIREMENTS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

Symbol	Parameter	723622-15 723632-15 723642-15		723622-20 723632-20 723642-20		723622-30 723632-30 723642-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fS	Clock Frequency, CLKA or CLKB		66.7		50		33.4	MHz
tCLK	Clock Cycle Time, CLKA or CLKB	15		20		30		ns
tCLKH	Pulse Duration, CLKA or CLKB HIGH	6		8		10		ns
tCLKL	Pulse Duration, CLKA and CLKB LOW	6		8		10		ns
tDS	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	4		5		6		ns
tENS	Setup Time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA before CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, ENB, and MBB before CLKB↑	4.5		5		6		ns
tRSTS	Setup Time, $\overline{RST1}$ or $\overline{RST2}$ LOW before CLKA↑ or CLKB↑[1]	5		6		7		ns
tFSS	Setup Time, FS0 and FS1 before $\overline{RST1}$ and $\overline{RST2}$ HIGH	7.5		8.5		9.5		ns
tDH	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	1		1		1		ns
tENH	Hold Time, $\overline{CSA}$, W/$\overline{RA}$, ENA, and MBA after CLKA↑; $\overline{CSB}$, W/$\overline{RB}$, ENB, and MBB after CLKB↑	1		1		1		ns
tRSTH	Hold Time, $\overline{RST1}$ or $\overline{RST2}$ LOW after CLKA↑ or CLKB↑[1]	4		4		5		ns
tFSH	Hold Time, FS0 and FS1 after $\overline{RST1}$ and $\overline{RST2}$ HIGH	2		3		3		ns
tSKEW1[2]	Skew Time, between CLKA↑ and CLKB↑ for ORA, ORB, IRA, and IRB	7.5		9		11		ns
tSKEW2[2]	Skew Time, between CLKA↑ and CLKB↑ for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, and $\overline{AFB}$	12		16		20		ns

NOTES:
1. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
2. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

5

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, C_L = 30 pF

Symbol	Parameter	723632-15		723632-20		723632-30		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_A	Access Time, CLKA↑ to A0-A35 and CLKB↑ to B0-B35	3	11	3	13	3	15	ns
t_{PIR}	Propagation Delay Time, CLKA↑ to IRA and CLKB↑ to IRB	2	8	2	10	2	12	ns
t_{POR}	Propagation Delay Time, CLKA↑ to ORA and CLKB↑ to ORB	1	8	1	10	1	12	ns
t_{PAE}	Propagation Delay Time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	1	8	1	10	1	12	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AFA}$ and and CLKB↑ to $\overline{AFB}$	1	8	1	10	1	12	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	0	8	0	10	0	12	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to B0-B35[1] and CLKB↑ to A0-A35[2]	3	13.5	3	15	3	17	ns
t_{MDV}	Propagation Delay Time, MBA to A0-A35 valid and MBB to B0-B35 Valid	3	11	3	13	3	15	ns
t_{PRF}	Propagation Delay Time, $\overline{RST1}$ LOW to $\overline{AEB}$ LOW, $\overline{AFA}$ HIGH, and $\overline{MBF1}$ HIGH, and $\overline{RST2}$ LOW to $\overline{AEA}$ LOW, $\overline{AFB}$ HIGH, and $\overline{MBF2}$ HIGH	1	15	1	20	1	30	ns
t_{EN}	Enable Time, $\overline{CSA}$ and W/$\overline{RA}$ LOW to A0-A35 Active and $\overline{CSB}$ LOW and $\overline{W}$/RB HIGH to B0-B35 Active	2	12	2	13	2	14	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{RA}$ HIGH to A0-A35 at high impedance and $\overline{CSB}$ HIGH or $\overline{W}$/RB LOW to B0-B35 at HIGH impedance	1	8	1	12	1	11	ns

NOTES:
1. Writing data to the mail1 register when the B0-B35 outputs are active and MBB is HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.

SIGNAL DESCRIPTION

RESET

The FIFO memories of the IDT723622/723632/723642 are reset separately by taking their reset ($\overline{RST1}$, $\overline{RST2}$) inputs LOW for at least four port-A clock (CLKA) and four port-B clock (CLKB) LOW-to-HIGH transitions. The reset inputs can switch asynchronously to the clocks. A FIFO reset initializes the internal read and write pointers and forces the input-ready flag (IRA, IRB) LOW, the output-ready flag (ORA, ORB) LOW, the almost-empty flag ($\overline{AEA}$, $\overline{AEB}$) LOW, and the almost-full flag ($\overline{AFA}$, $\overline{AFB}$) HIGH. Resetting a FIFO also forces the mailbox flag ($\overline{MBF1}$, $\overline{MBF2}$) of the parallel mailbox register HIGH. After a FIFO is reset, its input-ready flag is set HIGH after two clock cycles to begin normal operation. A FIFO must be reset after power up before data is written to its memory.

A LOW-to HIGH transition on a FIFO reset ($\overline{RST1}$, $\overline{RST2}$) input latches the value of the flag-select (FS0, FS1) inputs for choosing the almost-full and almost-empty offset programming method (see *almost-empty and almost-full flag offset programming* below).

ALMOST-EMPTY FLAG AND ALMOST-FULL FLAG OFFSET PROGRAMMING

Four registers in the IDT723622/723632/723642 are used to hold the offset values for the almost-empty and almost-full flags. The port-B almost-empty flag ($\overline{AEB}$) offset register is labeled X1 and the port-A almost-empty flag ($\overline{AEA}$) offset register is labeled X2. The port-A almost-full flag ($\overline{AFA}$) offset register is labeled Y1 and the port-B almost-full flag ($\overline{AFB}$) offset register is labeled Y2. The index of each register name corresponds to its FIFO number. The offset registers can be loaded with preset values during the reset of a FIFO or they can be programmed from port A (see Table 1) .

To load a FIFO almost-empty flag and almost-full flag offset registers with one of the three preset values listed in Table1, at least one of the flag-select inputs must be HIGH during the LOW-to-HIGH transition of its reset input. For example, to load the preset value of 64 into X1 and Y1, FS0 and FS1 must be HIGH when FIFO1 reset ($\overline{RST1}$) returns HIGH. Flag-offset registers associated with FIFO2 are loaded with one of the preset values in the same way with FIFO2 reset ($\overline{RST2}$). When using one of the preset values for the flag offsets, the FIFOs can be reset simultaneously or at different times.

To program the X1, X2, Y1, and Y2 registers from port A, both FIFOs should be reset simultaneously with FS0 and FS1 LOW during the LOW-to-HIGH transition of the reset inputs. After this reset is complete, the first four writes to FIFO1 do not store data in RAM but load the offset registers in the order Y1, X1, Y2, X2. The port A data inputs used by the offset registers are (A7-A0), (A8-A0), or (A9-A0) for the IDT723622, IDT723632, or IDT723642, respectively. The highest numbered input is used as the most significant bit of the binary number in each case. Valid programming values for the registers ranges from 1 to 252 for the IDT723622; 1 to 508 for the IDT723632; and 1 to 1020 for the IDT723642. After all the offset registers are programmed from port A, the port-B input-ready flag (IRB) is set HIGH, and both FIFOs begin normal operation.

FIFO WRITE/READ OPERATION

The state of the port-A data (A0-A35) outputs is controlled by port-A chip select ($\overline{CSA}$) and port-A write/read select (W/$\overline{RA}$). The A0-A35 outputs are in the High-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW.

Data is loaded into FIFO1 from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH , MBA is LOW, and IRA is HIGH. Data is read from FIFO2 to the A0-A35 outputs by a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is LOW, ENA is HIGH, MBA is LOW, and ORA is HIGH (see Table 2). FIFO reads and writes on port A are independent of any concurrent

FS1	FS0	$\overline{RST1}$	$\overline{RST2}$	X1 AND Y1 REGISTERS[1]	X2 AND Y2 REGISTERS[2]
H	H	↑	X	64	X
H	H	X	↑	X	64
H	L	↑	X	16	X
H	L	X	↑	X	16
L	H	↑	X	8	X
L	H	X	↑	X	8
L	L	↑	↑	Programmed from port A	Programmed from port A

NOTES:
1. X1 register holds the offset for $\overline{AEB}$; Y1 register holds the offset for $\overline{AFA}$.
2. X2 register holds the offset tor $\overline{AEA}$; Y2 register holds the offset for $\overline{AFB}$.

Table 1. Flag Programming

port-B operation.

The port-B control signals are identical to those of port A with the exception that the port-B write/read select ($\overline{W}$/RB) is the inverse of the port-A write/read select (W/$\overline{R}$A). The state of the port-B data (B0-B35) outputs is controlled by the port-B chip select ($\overline{CSB}$) and port-B write/read select ($\overline{W}$/RB). The B0-B35 outputs are in the high-impedance state when either $\overline{CSB}$ is HIGH or $\overline{W}$/RB is LOW. The B0-B35 outputs are active when $\overline{CSB}$ is LOW and $\overline{W}$/RB is HIGH.

Data is loaded into FIFO2 from the B0-B35 inputs on a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, $\overline{W}$/RB is LOW, ENB is HIGH, MBB is LOW, and IRB is HIGH. Data is read from FIFO1 to the B0-B35 outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, $\overline{W}$/RB is HIGH, ENB is HIGH, MBB is LOW, and ORB is HIGH (see Table 3) . FIFO reads and writes on port B are independent of any concurrent port-A operation.

The setup and hold time constraints to the port clocks for the port chip selects and write/read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port's chip select and write/read select may change states during the setup and hold time window of the cycle.

When a FIFO output-ready flag is LOW, the next data word is sent to the FIFO output register automatically by the LOW-to-HIGH transition of the port clock that sets the output-ready flag HIGH. When the output-ready flag is HIGH, an available data word is clocked to the FIFO output register only when a FIFO read is selected by the port's chip select, write/read select, enable, and mailbox select.

SYNCHRONIZED FIFO FLAGS

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of metastable events when CLKA and CLKB operate asynchronously to one another. ORA, $\overline{AEA}$, IRA, and $\overline{AFA}$ are synchronized to CLKA. ORB, $\overline{AEB}$, IRB, and $\overline{AFB}$ are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIF02.

$\overline{CSA}$	W/$\overline{R}$A	ENA	MBA	CLKA	A0-A35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	H	L	X	X	In high-impedance state	None
L	H	H	L	↑	In high-impedance state	FIFO1 write
L	H	H	H	↑	In high-impedance state	Mail1 write
L	L	L	L	X	Active, FIFO2 output register	None
L	L	H	L	↑	Active, FIFO2 output register	FIFO2 read
L	L	L	H	X	Active, mail2 register	None
L	L	H	H	↑	Active, mail2 register	Mail2 read (set $\overline{MBF2}$ HIGH)

Table 2. Port-A Enable Function Table

$\overline{CSB}$	$\overline{W}$/RB	ENB	MBB	CLKB	B0-B35 OUTPUTS	PORT FUNCTION
H	X	X	X	X	In high-impedance state	None
L	L	L	X	X	In high-impedance state	None
L	L	H	L	↑	In high-impedance state	FIFO2 write
L	L	H	H	↑	In high-impedance state	Mail2 write
L	H	L	L	X	Active, FIFO1 output register	None
L	H	H	L	↑	Active, FIFO1 output register	FIFO1 read
L	H	L	H	X	Active, mail1 register	None
L	H	H	H	↑	Active, mail1 register	Mail1 read (set $\overline{MBF1}$ HIGH)

Table 3. Port-B Enable Function Table

OUTPUT-READY FLAGS (ORA, ORB)

The output-ready flag of a FIFO is synchronized to the port clock that reads data from its array. When the output-ready flag is HIGH, new data is present in the FIFO output register. When the output-ready flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

A FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an output-ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. From the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the output-ready flag synchronizing clock. Therefore, an output-ready flag is LOW if a word in memory is the next data to be sent to the FIFO output register and three cycles of the port Clock that reads data from the FIFO have not elapsed since the time the word was written. The output-ready flag of the FIFO remains LOW until the third LOW-to-HIGH transition of the synchronizing clock occurs, simultaneously forcing the output-ready flag HIGH and shifting the word to the FIFO output register.

A LOW-to-HIGH transition on an output-ready flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 7 and 8).

INPUT-READY FLAGS (IRA, IRB)

The input-ready flag of a FIFO is synchronized to the port clock that writes data to its array. When the input-ready flag is HIGH, a memory location is free in the SRAM to receive new data. No memory locations are free when the input-ready flag is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls an input-ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full-1, or full-2. From the time a word is read from a FIFO, its previous memory location is ready to be written in a minimum of two cycles of the

5

Number of Words in FIFO			Synchronized to CLKB		Synchronized to CLKA	
IDT723622[1,2]	IDT723632[1,2]	IDT723642[1,2]	ORB	$\overline{AEB}$	$\overline{AFA}$	IRA
0	0	0	L	L	H	H
1 to X1	1 to X1	1 to X1	H	L	H	H
(X1+1) to [256-(Y1+1)]	(X1+1) to [512-(Y1+1)]	(X1+1) to [1024-(Y1+1)]	H	H	H	H
(256-Y1) to 255	(512-Y1) to 511	(1024-Y1) to 1023	H	H	L	H
256	512	1024	H	H	L	L

Table 4. FIF01 Flag Operation

Notes:
1. X1 is the almost-empty offset for FIFO1 used by $\overline{AEB}$. Y1 is the almost-full offset for FIFO1 used by $\overline{AFA}$. Both X1 and Y1 are selected during a reset of FIFO1 or programmed from port A.
2. When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

Number of Words in FIFO			Synchronized to CLKA		Synchronized to CLKB	
IDT723622[1,2]	IDT723632[1,2]	IDT723642[1,2]	ORA	$\overline{AEA}$	$\overline{AFB}$	IRB
0	0	0	L	L	H	H
1 to X2	1 to X2	1 to X2	H	L	H	H
(X2+1) to [256-(Y2+1)]	(X2+1) to [512-(Y2+1)]	(X2+1) to [1024-(Y2+1)]	H	H	H	H
(256-Y2) to 255	(512-Y2) to 511	(1024-Y2) to 1023	H	H	L	H
256	512	1024	H	H	L	L

Table 5. FIF02 Flag Operation

Notes:
1. X2 is the almost-empty offset for FIFO2 used by $\overline{AEA}$. Y2 is the almost-full offset for FIFO2 used by $\overline{AFB}$. Both X2 and Y2 are selected during a reset of FIFO2 or programmed from port A.
2. When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.

input-ready flag synchronizing clock. Therefore, an input-ready flag is LOW if less than two cycles of the input-ready flag synchronizing clock have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the input-ready flag synchronizing Clock after the read sets the input-ready flag HIGH.

A LOW-to-HIGH transition on an input-ready flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 9 and 10).

ALMOST-EMPTY FLAGS ($\overline{AEA}$, $\overline{AEB}$)

The almost-empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an almost-empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost empty, almost empty+1, or almost empty+2. The almost-empty state is defined by the contents of register X1 for $\overline{AEB}$ and register X2 for $\overline{AEA}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming* above). An almost empty Flag is LOW when its FIFO contains X or less words and is HIGH when its FIFO contains (X+1) or more words. A data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the almost-empty flag synchronizing clock are required after a FIFO write for its almost-empty flag to reflect the new level of fill. Therefore, the almost-full flag of a FIFO containing (X+1) or more words remains LOW if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the (X+1) level. An almost-empty flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of an almost-empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle.

ALMOST-FULL FLAGS ($\overline{AFA}$, $\overline{AFB}$)

The almost-full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an almost-full flag monitors a write pointer and read pointer comparator that indicates when the FIFO SRAM status is almost full, almost full-1, or almost full-2. The almost-full state is defined by the contents of register Y1 for $\overline{AFA}$ and register Y2 for $\overline{AFB}$. These registers are loaded with preset values during a FIFO reset or programmed from port A (see *almost-empty flag and almost-full flag offset programming* above). An almost-full flag is LOW when the number of words in its FIFO is greater than or equal to (256-Y), (512-Y), or (1024-Y) for the IDT723622, IDT723632, or IDT723642 respectively. An almost-full flag is HIGH when the number of words in its FIFO is less than or equal to [256-(Y+1)], [512-(Y+1)], or [1024-(Y+1)] for the IDT723622, IDT723632, or IDT723642 respectively. Note that a data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the almost-full flag synchronizing clock are required after a FIFO read for its almost-full flag to reflect the new level of fill. Therefore, the almost-full flag of a FIFO containing [256/512/1024-(Y+1)] or less words remains LOW if two cycles of its synchronizing clock have not elapsed since the read that reduced the number of words in memory to [256/512/1024-(Y+1)]. An almost-full flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO read that reduces the number of words in memory to [256/512/1024-(Y+1)]. A LOW-to-HIGH transition of an almost-full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [256/512/1024-(Y+1)]. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle (see Figures 13 and 14).

MAILBOX REGISTERS

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The mailbox-select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A LOW-to-HIGH transition on CLKA writes A0-A35 data to the mail1 register when a port-A write is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and with MBA HIGH. A LOW-to-HIGH transition on CLKB writes BO-B35 data to the mail2 register when a port-B write is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and with MBB HIGH. Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while the mail flag is LOW.

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port mailbox select input is LOW and from the mail register when the port-mailbox select input is HIGH. The mail1 register flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a port-B read is selected by $\overline{CSB}$, W/$\overline{RB}$, and ENB and with MBB HIGH. The mail2 register flag ($\overline{MBF2}$) is set HIGH by a LOW-to-HIGH transition on CLKA when a port-A read is selected by $\overline{CSA}$, W/$\overline{RA}$, and ENA and with MBA HIGH. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

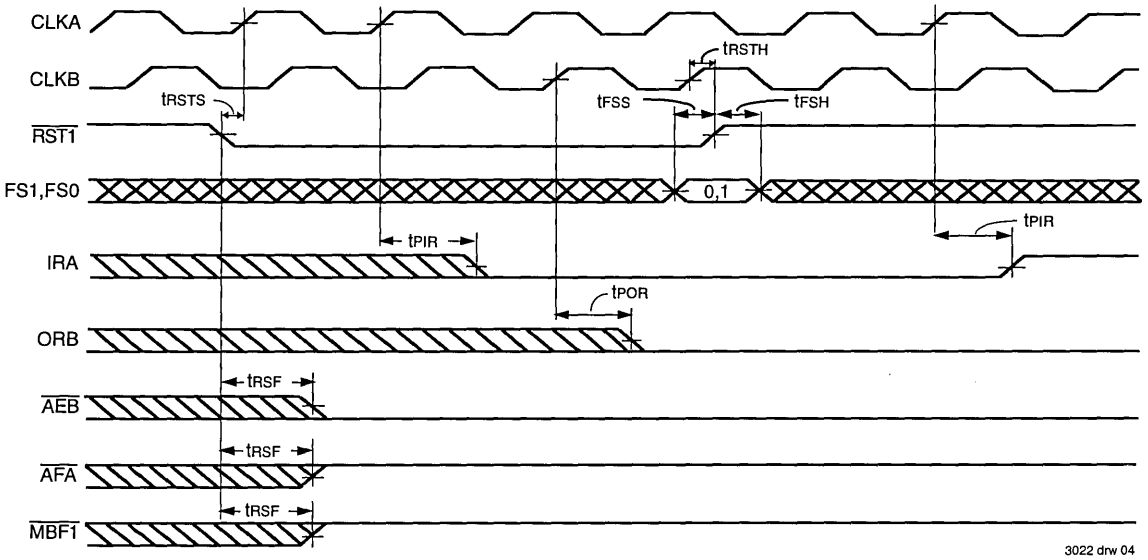
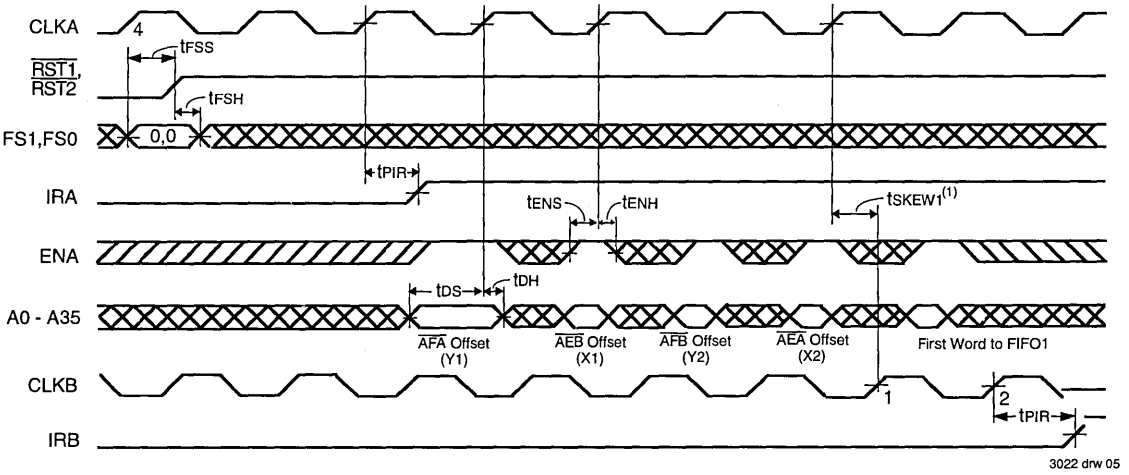


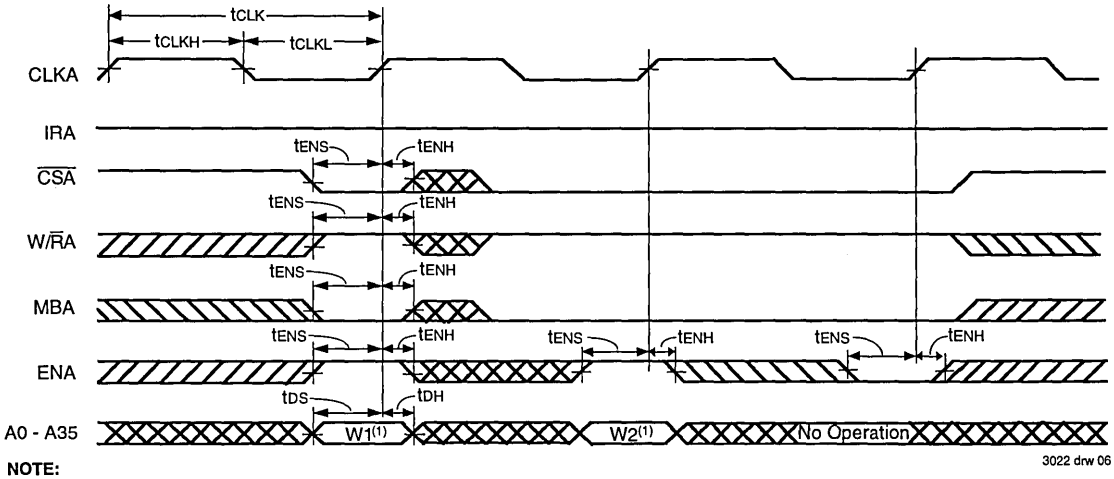
Figure 1. FIFO1 Reset Loading X1 and Y1 with a Preset Value of Eight(1).

NOTE:
1. FIFO2 is reset in the same manner to load X2 and Y2 with a preset value.



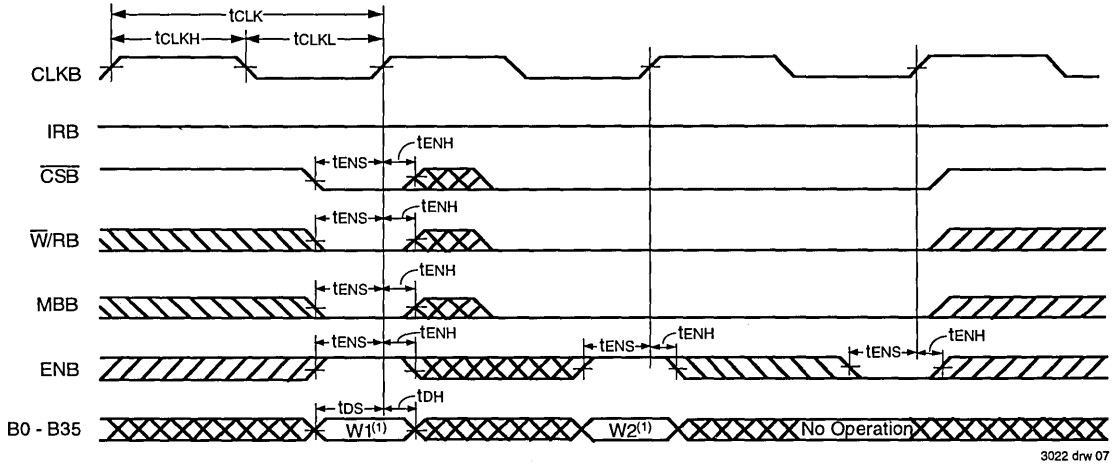
NOTES:
1. tSKEW1 is the minimum time between the rising CLKA edge and a rising CLKB edge for $\overline{IRB}$ to transition HIGH in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKB is less than tSKEW1, then $\overline{IRB}$ may transition HIGH one cycle later than shown.
2. $\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW. It is not necessary to program offset register on consecutive clock cycles.

Figure 2. Programming the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset.



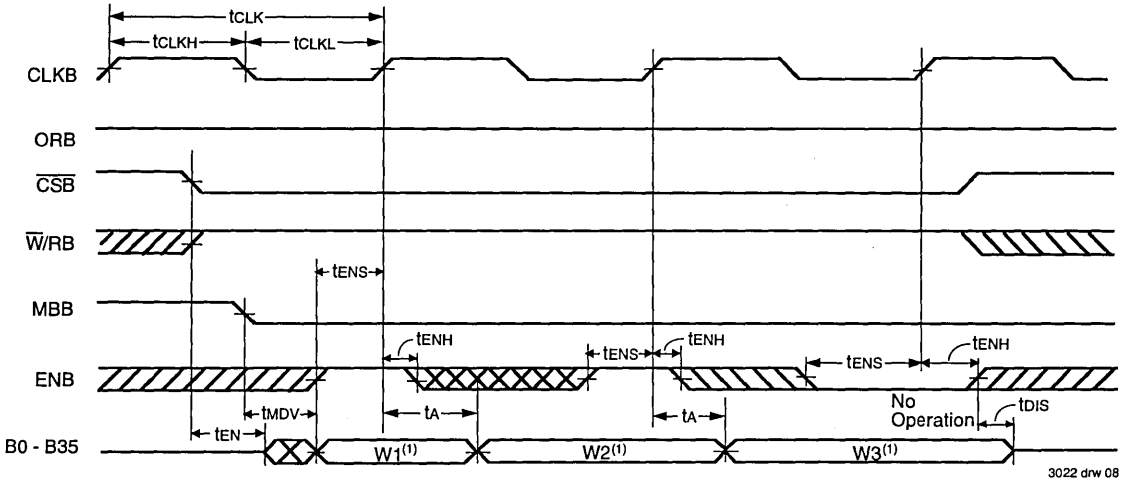
NOTE:
1. Written to FIFO1.

Figure 3. Port-A Write Cycle Timing for FIFO1



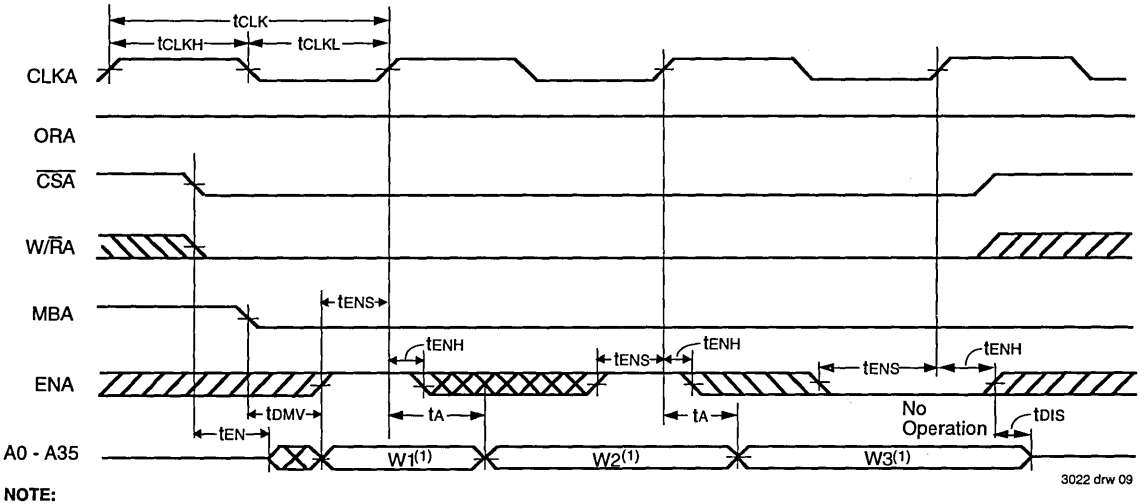
NOTE:
1. Written to FIFO2.

Figure 4. Port-B Write Cycle Timing for FIFO2.



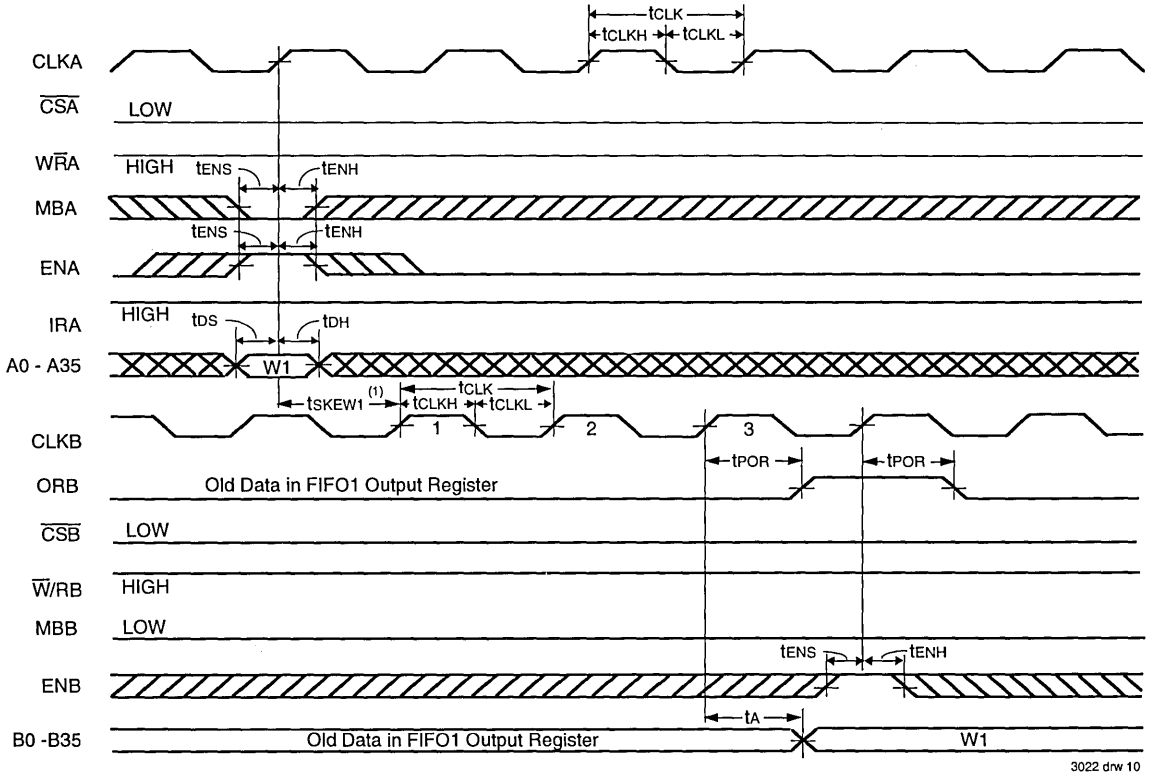
NOTE:
1. Read From FIFO1.

Figure 5. Port-B Read Cycle Timing for FIFO1.



NOTE:
1. Read From FIFO2.

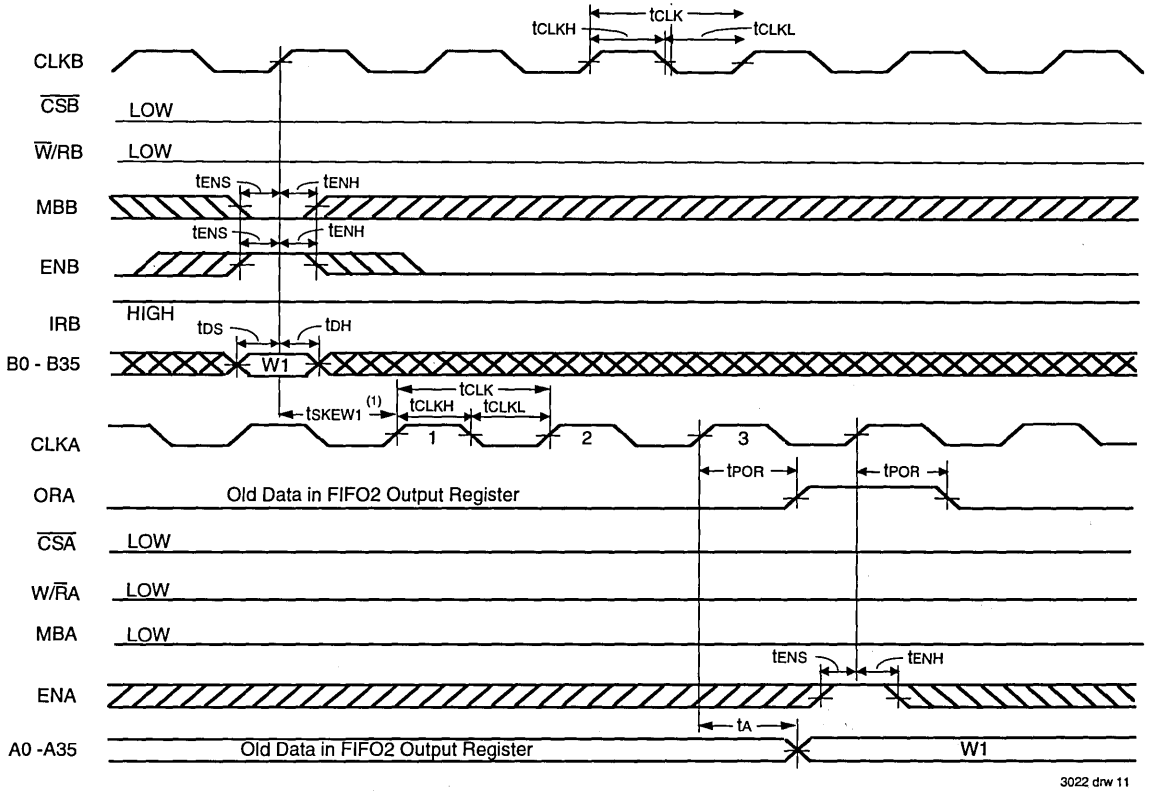
Figure 6. Port-A Read Cycle Timing for FIFO2.



NOTE:

1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for ORB to transition HIGH and to clock the next word to the FIFO1 output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of ORB HIGH and load of the first word to the output register may occur one CLKB cycle later than shown.

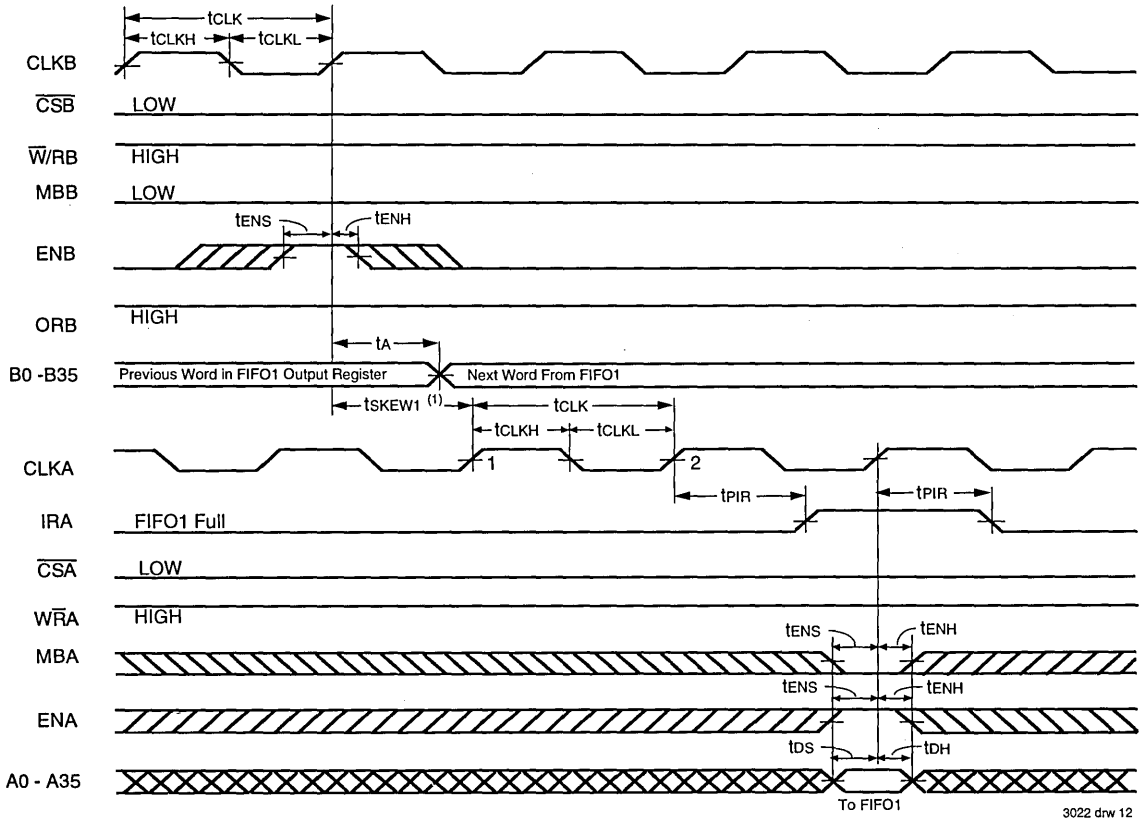
Figure 7. ORB Flag Timing and First Data Word Fallthrough when FIFO1 is Empty.



NOTE:

1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for ORA to transition HIGH and to clock the next word to the FIFO2 output register in three CLKA cycles. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then the transition of ORA HIGH and load of the first word to the output register may occur one CLKA cycle later than shown.

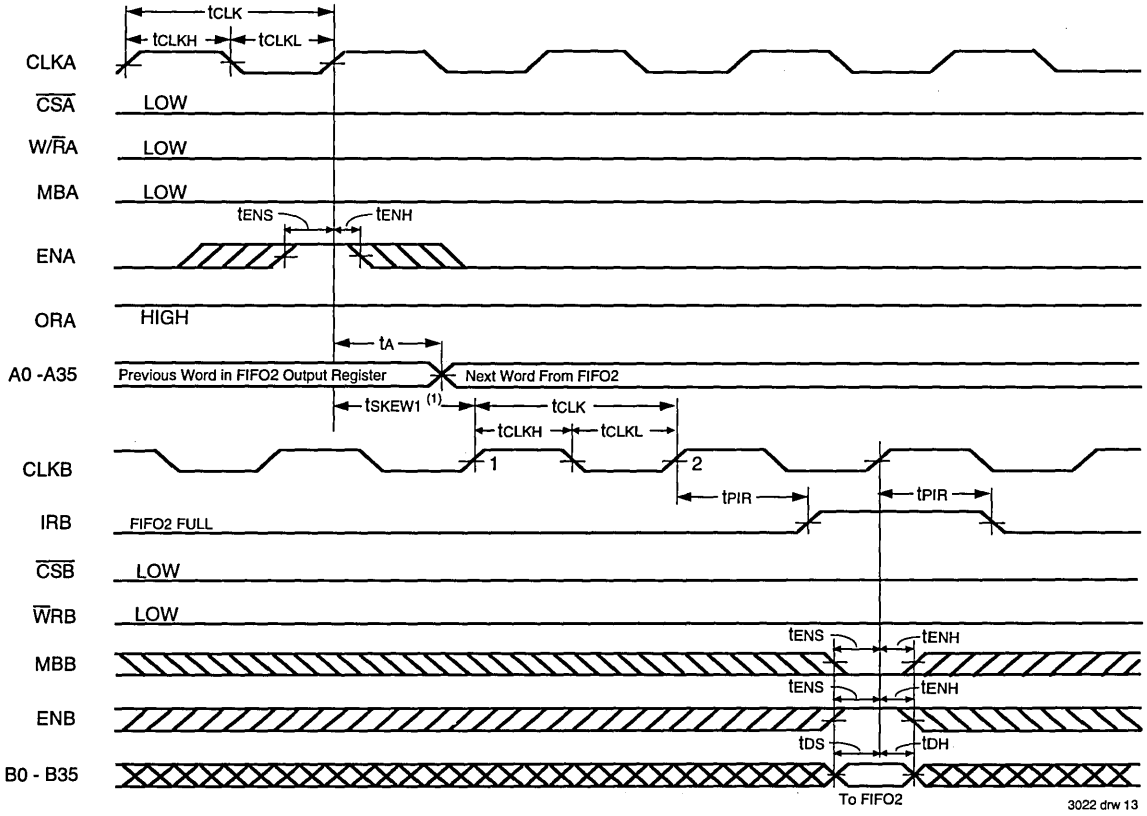
Figure 8. ORA Flag Timing and First Data Word Fallthrough when FIFO2 is Empty.



NOTE:

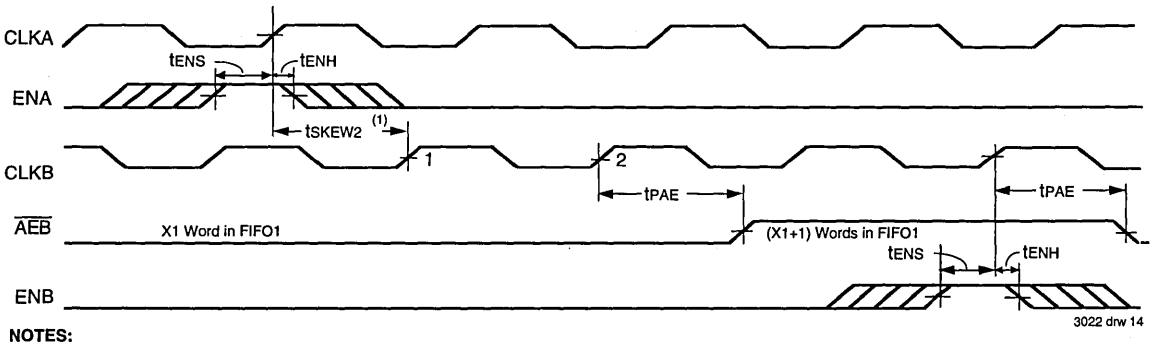
1. tSKEW1 is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW1, then IRA may transition HIGH one CLKA cycle later than shown.

Figure 9. IRA Flag Timing and First Available Write when FIFO1 is Full.



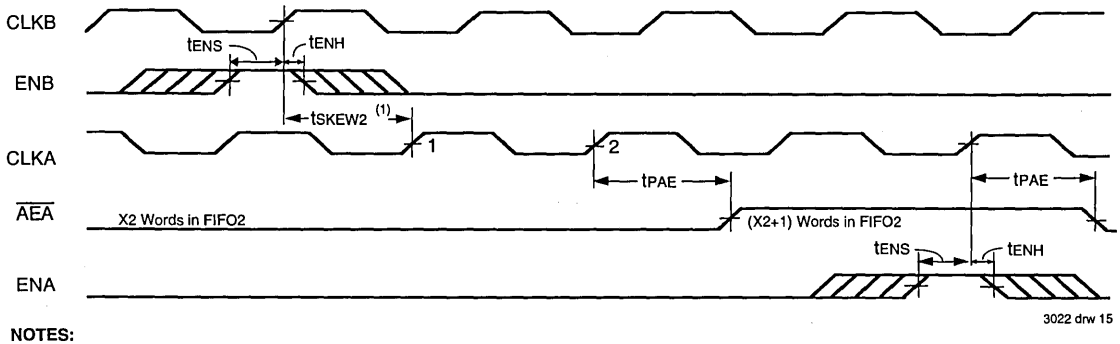
NOTE:
1. tSKEW1 is the minimum time between a rising CLKA edge and a rising CLKB edge for IRB to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW1, then IRB may transition HIGH one CLKB cycle later than shown.

Figure 10. IRB Flag Timing and First Available Write when FIFO2 is Full.



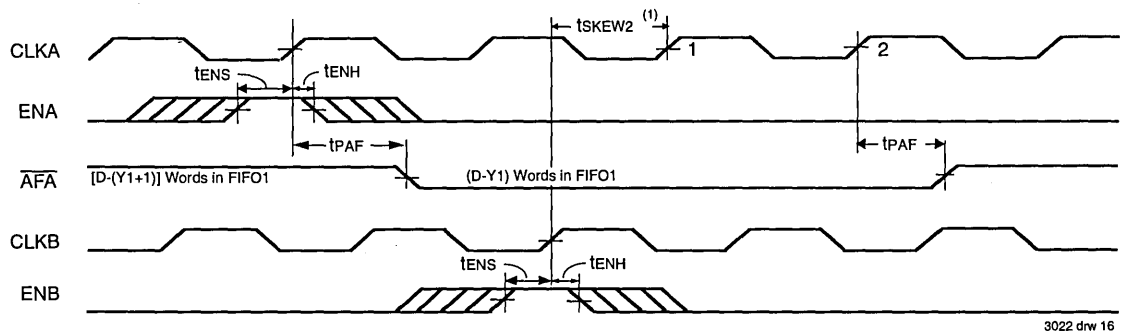
NOTES:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for AEB to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then AEB may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write (CSA = LOW, W/RA = LOW, MBA = LOW), FIFO1 read (CSB = LOW, W/RB = HIGH, MBB = LOW). Data in the FIFO1 output register has been read from the FIFO.

Figure 11. Timing for AEB when FIFO2 is Almost Empty.



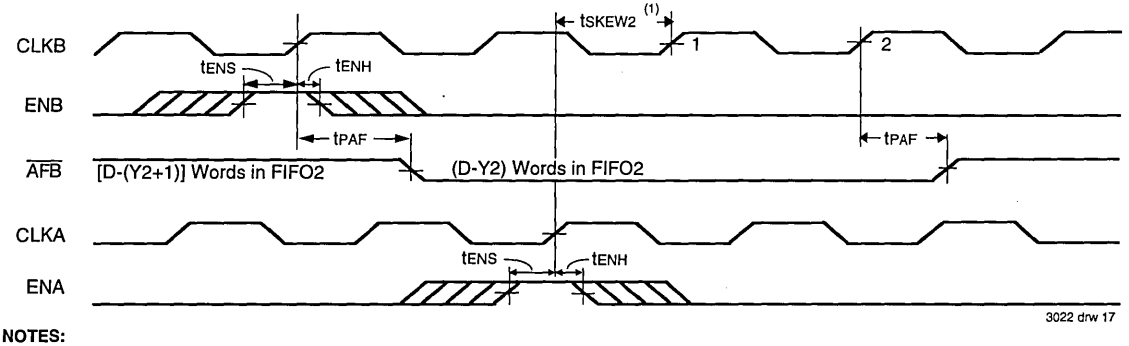
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AEA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW2}, then $\overline{AEA}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO2 Write ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = LOW, MBB = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW). Data in the FIFO2 output register has been read from the FIFO.

Figure 12. Timing for $\overline{AEA}$ when FIFO2 is Almost Empty.



NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AFA}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO1 read ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = HIGH, MBB = LOW). Data in the FIFO1 output register has been read from the FIFO.
3. D = Maximum FIFO Depth = 256 for the 723622, 512 for the 723632, 1024 for the 723642.

Figure 13. Timing for $\overline{AFA}$ when FIFO1 is Almost Full.



NOTES:
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{AFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW2, then $\overline{AFB}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO2 write ($\overline{CSB}$ = LOW, W/$\overline{RB}$ = LOW, MBB = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW). Data in the FIFO2 output register has been read from the FIFO.
3. D = Maximum FIFO Depth = 256 for the 723622, 512 for the 723632, 1024 for the 723642.

Figure 14. Timing for $\overline{AFB}$ when FIFO2 is Almost Full.

5

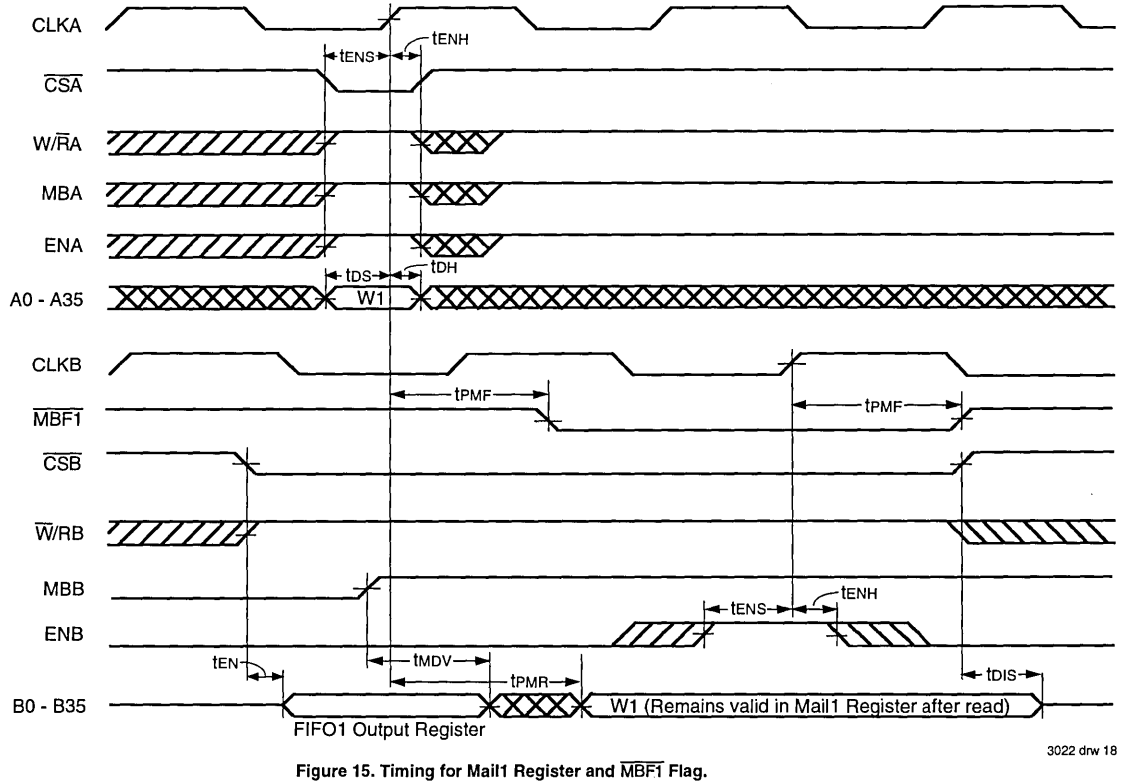


Figure 15. Timing for Mail1 Register and $\overline{MBF1}$ Flag.

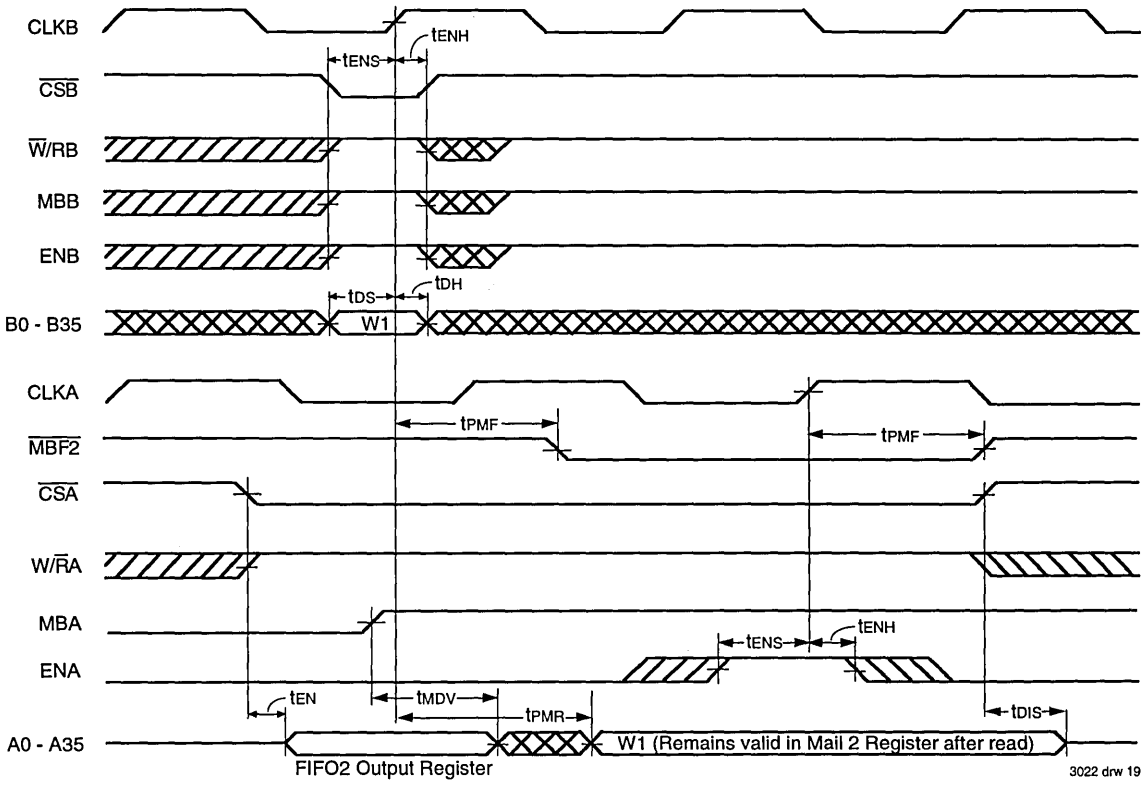


Figure 16. Timing for Mail2 Register and $\overline{MBF2}$ Flag.

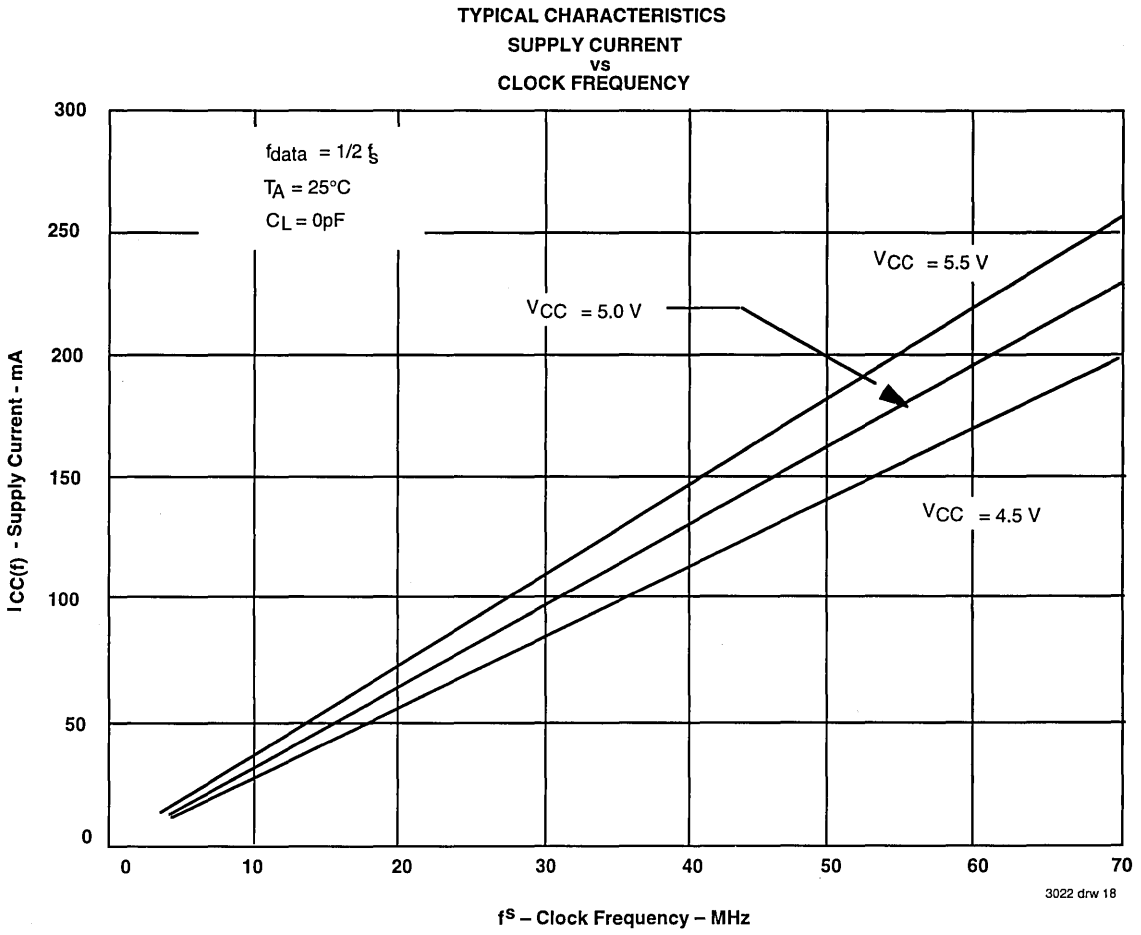


Figure 17.

CALCULATING POWER DISSIPATION

The $I_{CC(f)}$ current for the graph in Figure 17 was taken while simultaneously reading and writing a FIFO on the IDT723622/IDT723632/IDT723642 with CLKA and CLKB set to fs. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero capacitance load. Once the capacitance load per data-output channel and the number of IDT723622/IDT723632/IDT62342 inputs driven by TTL HIGH levels are known, the power dissipation can be calculated with the equation below.

With $I_{CC(f)}$ taken from FIgure 17, the maximum power dissipation (PT) of the IDT723622/IDT723632/IDT723642 may be calculated by:

$$PT = VCC \times [ICC(f) + (N \times \Delta ICC \times dc)] + \Sigma(CL \times VCC^2 \times fO)$$

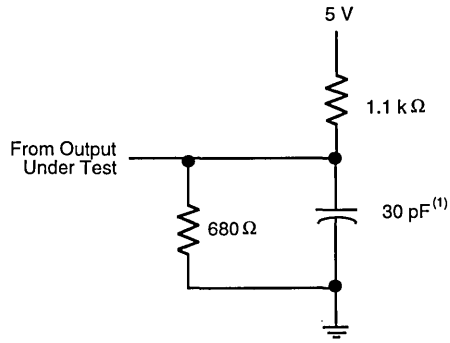
where:

N	=	number of inputs driven by TTL levels
ΔICC	=	increase in power supply current for each input at a TTL HIGH level
dc	=	duty cycle of inputs at a TTL HIGH level of 3.4 V
CL	=	output capacitance load
fO	=	switching frequency of an output

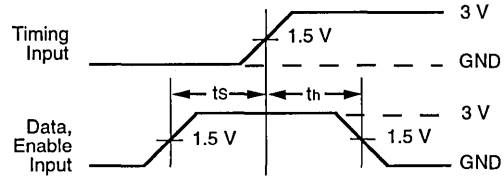
When no read or writes are occurring on the IDT723632, the power dissipated by a single clock (CLKA or CLKB) input running at frequency fS is calculated by:

$$PT = Vcc \times fs \times 0.184\ mA/MHz$$

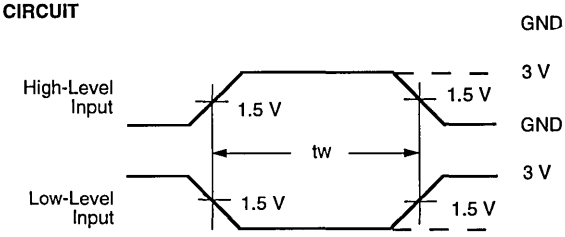
PARAMETER MEASUREMENT INFORMATION



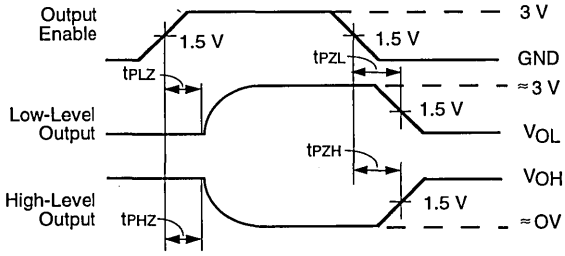
PROPAGATION DELAY
LOAD CIRCUIT



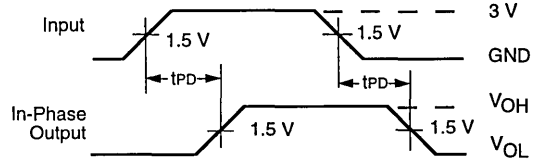
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES



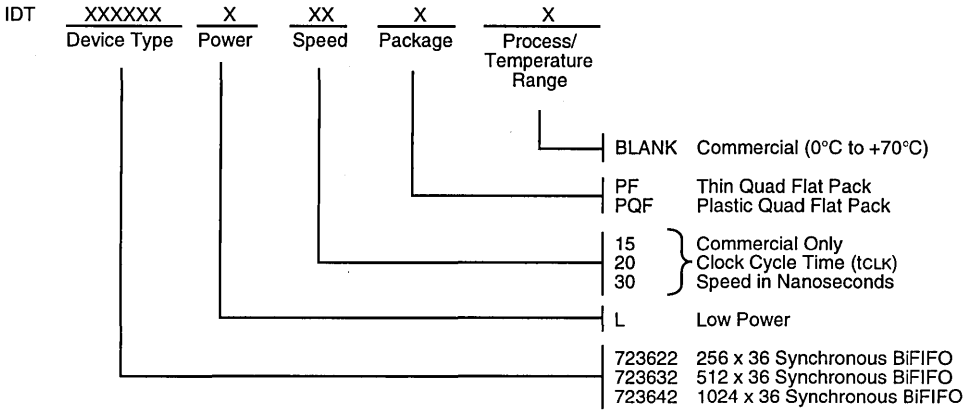
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

3022 drw 20

NOTE:
1. Includes probe and jig capacitance.

Figure 18. Load Circuit and Voltage Waveforms.

ORDERING INFORMATION



3022 drw 22

5

Integrated Device Technology, Inc.

CMOS PARALLEL FIFO 64 x 4-BIT AND 64 x 5-BIT

IDT72401
IDT72402
IDT72403
IDT72404

FEATURES:

- First-In/First-Out Dual-Port memory
- 64 x 4 organization (IDT72401/03)
- 64 x 5 organization (IDT72402/04)
- IDT72401/02 pin and functionally compatible with MMI67401/02
- RAM-based FIFO with low fall-through time
- Low-power consumption
  — Active: 175mW (typ.)
- Maximum shift rate — 45MHz
- High data output drive capability
- Asynchronous and simultaneous read and write
- Fully expandable by bit width
- Fully expandable by word depth
- IDT72403/04 have Output Enable pin to enable output data
- High-speed data communications applications
- High-performance CMOS technology
- Available in CERDIP, plastic DIP and SOIC
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86846 and 5962-89523 is listed on this function.

DESCRIPTION:

The IDT72401 and IDT72403 are asynchronous high-performance First-In/First-Out memories organized 64 words by 4 bits. The IDT72402 and IDT72404 are asynchronous high-performance First-In/First-Out memories organized as 64 words by 5 bits. The IDT72403 and IDT72404 also have an Output Enable ($\overline{OE}$) pin. The FIFOs accept 4-bit or 5-bit data at the data input ($D_{0-3,4}$). The stored data stack up on a first-in/first-out basis.

A Shift Out (SO) signal causes the data at the next to last word to be shifted to the output while all other data shifts down one location in the stack. The Input Ready (IR) signal acts like a flag to indicate when the input is ready for new data (IR = HIGH) or to signal when the FIFO is full (IR = LOW). The Input Ready signal can also be used to cascade multiple devices together. The Output Ready (OR) signal is a flag to indicate that the output remains valid data (OR = HIGH) or to indicate that the FIFO is empty (OR = LOW). The Output Ready can also be used to cascade multiple devices together.

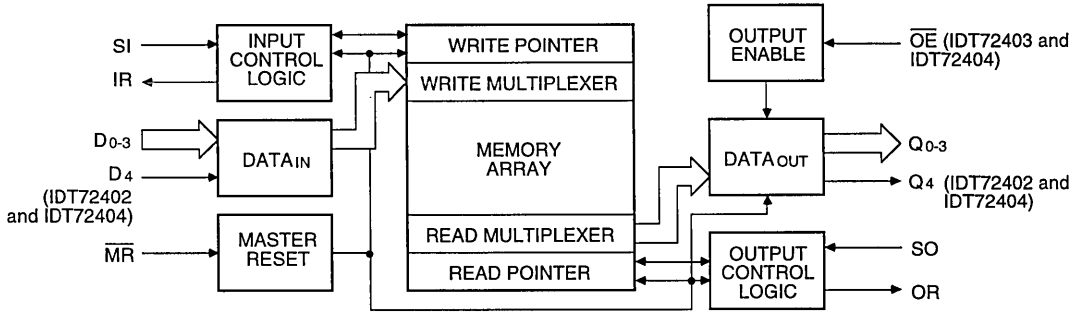
Width expansion is accomplished by logically ANDing the Input Ready (IR) and Output Ready (OR) signals to form composite signals.

Depth expansion is accomplished by tying the data inputs of one device to the data outputs of the previous device. The Input Ready pin of the receiving device is connected to the Shift Out pin of the sending device and the Output Ready pin of the sending device is connected to the Shift In pin of the receiving device.

Reading and writing operations are completely asynchronous allowing the FIFO to be used as a buffer between two digital machines of widely varying operating frequencies. The 45MHz speed makes these FIFOs ideal for high-speed communication and controller applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

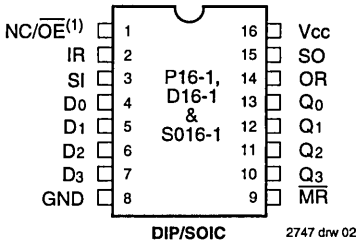


2747 drw 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.
FAST is a trademark of National Semiconductor, Inc.

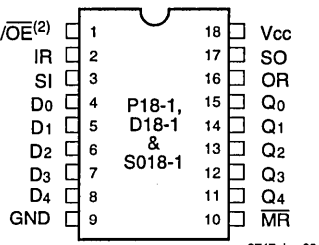
PIN CONFIGURATIONS

IDT72401/IDT72403



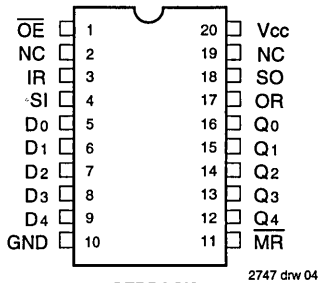
DIP/SOIC TOP VIEW 2747 drw 02

IDT72402/IDT72404



DIP/SOIC TOP VIEW 2747 drw 03

(IDT72404 Only)



2747 drw 04

CERPACK TOP VIEW

NOTES:
1. Pin 1: NC - No Connection IDT72401, OE - IDT72403
2. Pin 1: NC - No Connection IDT72402,OE - IDT72404

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temp.	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temp.	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2747 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Mil. Supply Voltage	4.5	5.0	5.5	V
VCC	Com'l. Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.0	—	—	V
VIL(1)	Input High Voltage	—	—	0.8	V

NOTE: 2747 tbl 02
1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	5	pF
COUT	Output Capacitance	VOUT = 0V	7	pF

NOTE: 2747 tbl 03
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 5.0V ± 10%, TA = 0°C to +70°C; Military: VCC = 5.0V ± 10%, TA = –55°C to +125°C)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
IIL	Low-Level Input Current	VCC = Max., GND ≤ VI ≤ VCC		–10	—	µA
IIH	High-Level Input Current	VCC = Max., GND ≤ VI ≤ VCC		—	10	µA
VOL	Low-Level Output Voltage	VCC = Min., IOL = 8mA		—	0.4	V
VOH	High-Level Output Voltage	VCC = Min., IOH = -4mA		2.4	—	V
IOS(1)	Output Short-Circuit Current	VCC = Max., VO = GND		–20	–110	mA
IHZ	Off-State Output Current	VCC = Max., VO = 2.4V		—	20	µA
ILZ	(IDT72403 and IDT72404)	VCC = Max., VO = 0.4V		–20	—	µA
ICC(2,3)	Supply Current	VCC = Max., f = 10MHz	Com'l.	—	35	mA
			Military	—	45	mA

NOTES: 2747 tbl 04
1. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. Guaranteed but not tested.
2. Icc measurements are made with outputs open. OE is HIGH for IDT72403/72404.
3 For frequencies greater than 10MHZ, Icc = 35mA + (1.5mA x [f - 10MHz]) commercial, and Icc = 45mA + (1.5mA x [f - 10MHz]) military.

OPERATING CONDITIONS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = –55°C to +125°C)

			Commercial		Military and Commercial								
			IDT72401L45 IDT72402L45 IDT72403L45 IDT72404L45		IDT72401L35 IDT72402L35 IDT72403L35 IDT72404L35		IDT72401L25 IDT72402L25 IDT72403L25 IDT72404L25		IDT72401L15 IDT72402L15 IDT72403L15 IDT72404L15		IDT72401L10 IDT72402L10 IDT72403L10 IDT72404L10		
Symbol	Parameters	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{SIH}[1]	Shift in HIGH Time	2	9	—	9	—	11	—	11	—	11	—	ns
t_{SIL}	Shift in LOW TIme	2	11	—	17	—	24	—	25	—	30	—	ns
t_{IDS}	Input Data Set-up	2	0	—	0	—	0	—	0	—	0	—	ns
t_{IDH}	Input Data Hold Time	2	13	—	15	—	20	—	30	—	40	—	ns
t_{SOH}[1]	Shift Out HIGH Time	5	9	—	9	—	11	—	11	—	11	—	ns
t_{SOL}	Shift Out LOW Time	5	11	—	17	—	24	—	25	—	25	—	ns
t_{MRW}	Master Reset Pulse	8	20	—	25	—	25	—	25	—	30	—	ns
t_{MRS}	Master Reset Pulse to SI	8	10	—	10	—	10	—	25	—	35	—	ns
t_{SIR}	Data Set-up to IR	4	3	—	3	—	5	—	5	—	5	—	ns
t_{HIR}	Data Hold from IR	4	13	—	15	—	20	—	30	—	30	—	ns
t_{SOR}[4]	Data Set-up to OR HIGH	7	0	—	0	—	0	—	0	—	0	—	ns

2747 tbl 05

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = –55°C to +125°C)

			Commercial		Military and Commercial								
			IDT72401L45 IDT72402L45 IDT72403L45 IDT72404L45		IDT72401L35 IDT72402L35 IDT72403L35 IDT72404L35		IDT72401L25 IDT72402L25 IDT72403L25 IDT72404L25		IDT72401L15 IDT72402L15 IDT72403L15 IDT72404L15		IDT72401L10 IDT72402L10 IDT72403L10 IDT72404L10		
Symbol	Parameters	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{IN}	Shift In Rate	2	—	45	—	35	—	25	—	15	—	10	MHz
t_{IRL}[1]	Shift In to Input Ready LOW	2	—	18	—	18	—	21	—	35	—	40	ns
t_{IRH}[1]	Shift In to Input Ready HIGH	2	—	18	—	20	—	28	—	40	—	45	ns
t_{OUT}	Shift Out Rate	5	—	45	—	35	—	25	—	15	—	10	MHz
t_{ORL}[1]	Shift Out to Output Ready LOW	5	—	18	—	18	—	19	—	35	—	40	ns
t_{ORH}[1]	Shift Out to Output Ready HIGH	5	—	19	—	20	—	34	—	40	—	55	ns
t_{ODH}	Output Data Hold (Previous Word)	5	5	—	5	—	5	—	5	—	5	—	ns
t_{ODS}	Output Data Shift (Next Word)	5	—	19	—	20	—	34	—	40	—	55	ns
t_{PT}	Data Throughput or "Fall-Through"	4, 7	—	30	—	34	—	40	—	65	—	65	ns
t_{MRORL}	Master Reset to OR LOW	8	—	25	—	28	—	35	—	35	—	40	ns
t_{MRIRH}	Master Reset to IR HIGH	8	—	25	—	28	—	35	—	35	—	40	ns
t_{MRQ}	Master Reset to Data Output LOW	8	—	20	—	20	—	25	—	35	—	40	ns
t_{OOE}[3]	Output Valid from $\overline{OE}$ LOW	9	—	12	—	15	—	20	—	30	—	35	ns
t_{HZOE}[3,4]	Output High-Z from $\overline{OE}$ HIGH	9	—	12	—	12	—	15	—	25	—	30	ns
t_{IPH}[2,4]	Input Ready Pulse HIGH	4	9	—	9	—	11	—	11	—	11	—	ns
t_{OPH}[2,4]	Ouput Ready Pulse HIGH	7	9	—	9	—	11	—	11	—	11	—	ns

NOTES:

2747 tbl 06

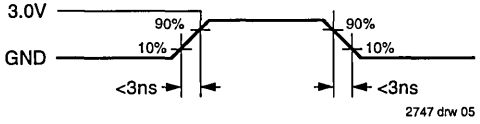
1. Since the FIFO is a very high-speed device, care must be excercised in the design of the hardware and timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between V_{CC} and GND with very short lead length is recommended.
2. This parameter applies to FIFOs communicating with each other in a cascaded mode. IDT FIFOs are guaranteed to cascade with other IDT FIFOs of like speed grades.
3. IDT72403 and IDT72404 only.
4. Guaranteed by design but not currently tested.

AC TEST CONDITIONS

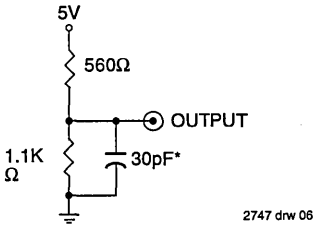
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2747 tbl 07

ALL INPUT PULSES:



2747 drw 05



2747 drw 06

or equivalent circuit

Figure 1. AC Test Load

*Including scope and jig

SIGNAL DESCRIPTIONS

INPUTS:

DATA INPUT ($D_{0-3, 4}$)

Data input lines. The IDT72401 and IDT72403 have a 4-bit data input. The IDT72402 and IDT72404 have a 5-bit data input.

CONTROLS:

SHIFT IN (SI)

Shift In controls the input of the data into the FIFO. When SI is HIGH, data can be written to the FIFO via the $D_{0-3, 4}$ lines.

SHIFT OUT (SO)

Shift Out controls the output of data of the FIFO. When SO is HIGH, data can be read from the FIFO via the Data Output ($Q_{0-3, 4}$) lines.

MASTER RESET (MR)

Master Reset clears the FIFO of any data stored within. Upon power up, the FIFO should be cleared with a Master Reset. Master Reset is active LOW.

INPUT READY (IR)

When Input Ready is HIGH, the FIFO is ready for new input data to be written to it. When IR is LOW the FIFO is unavailable for new input data. Input Ready is also used to cascade many FIFOs together, as shown in Figures 10 and 11 in the Applications section.

OUTPUT READY (OR)

When Output Ready is HIGH, the output ($Q_{0-3, 4}$) contains valid data. When OR is LOW, the FIFO is unavailable for new output data. Output Ready is also used to cascade many FIFOs together, as shown in Figures 10 and 11.

OUTPUT ENABLE (OE) (IDT72403 AND IDT72404 ONLY)

Output enable is used to read FIFO data onto a bus. Output Enable is active LOW.

OUTPUTS:

DATA OUTPUT ($Q_{0-3, 4}$)

Data Output lines. The IDT72401 and IDT72403 have a 4-bit data output. The IDT72402 and IDT72404 have a 5-bit data output.

FUNCTIONAL DESCRIPTION

These 64 x 4 and 64 x 5 FIFOs are designed using a dual port RAM architecture as opposed to the traditional shift register approach. This FIFO architecture has a write pointer, a read pointer and control logic, which allow simultaneous read and write operations. The write pointer is incremented by the falling edge of the Shift In (SI) control; the read pointer is incremented by the falling edge of the Shift Out (SO). The Input Ready (IR) signals when the FIFO has an available memory location; Output Ready (OR) signals when there is valid data on the output. Output Enable (OE) provides the capability of three-stating the FIFO outputs.

FIFO Reset

The FIFO must be reset upon power up using the Master Reset (MR) signal. This causes the FIFO to enter an empty state, signified by Output Ready (OR) being LOW and Input Ready (IR) being HIGH. In this state, the data outputs ($Q_{0-3, 4}$) will be LOW.

Data Input

Data is shifted in on the LOW-to-HIGH transition of Shift In (SI). This loads input data into the first word location of the FIFO and causes Input Ready to go LOW. On the HIGH-to-LOW transition of Shift In, the write pointer is moved to the next word position and Input Ready (IR) goes HIGH, indicating the readiness to accept new data. If the FIFO is full, Input Ready will remain LOW until a word of data is shifted out.

5

Data Output

Data is shifted out on the HIGH-to-LOW transition of Shift Out (SO). This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and Output Ready (OR) will go HIGH. If data is not present, Output Ready will stay LOW indicating the FIFO is empty. The last valid word read from the FIFO will remain at the FIFOs output when it is empty. When the FIFO is not empty, Output Ready (OR) goes LOW on the LOW-to-HIGH transition of Shift Out. Previous data remains on the output until the HIGH-to-LOW transition of Shift Out (SO).

Fall-Through Mode

The FIFO operates in a fall-through mode when data gets shifted into an empty FIFO. After a fall-through delay the data propagates to the output. When the data reaches the output, the Output Ready (OR) goes HIGH. Fall-through mode also occurs when the FIFO is completely full. When data is shifted out of the full FIFO, a location is available for new data. After a fall-through delay, the Input Ready goes HIGH. If Shift In is HIGH, the new data can be written to the FIFO.

Since these FIFOs are based on an internal dual-port RAM architecture with separate read and write pointers, the fall-through time (tPT) is one cycle long. A word may be written into the FIFO on a clock cycle and can be accessed on the next clock cycle.

TIMING DIAGRAMS

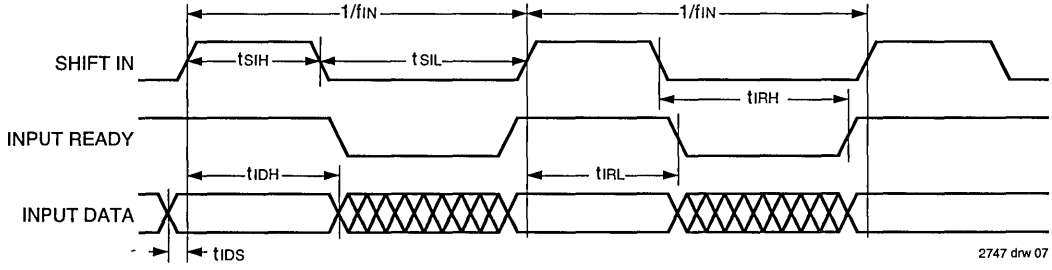
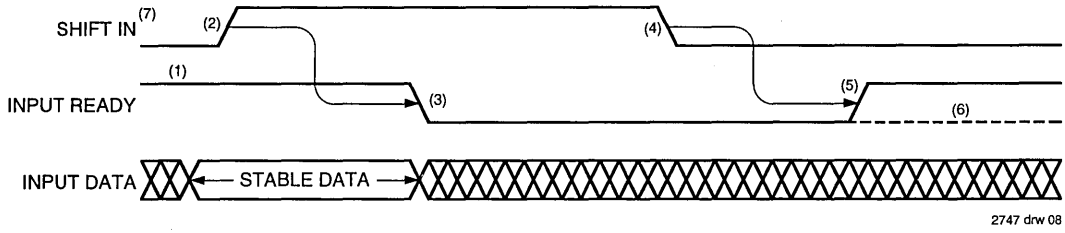


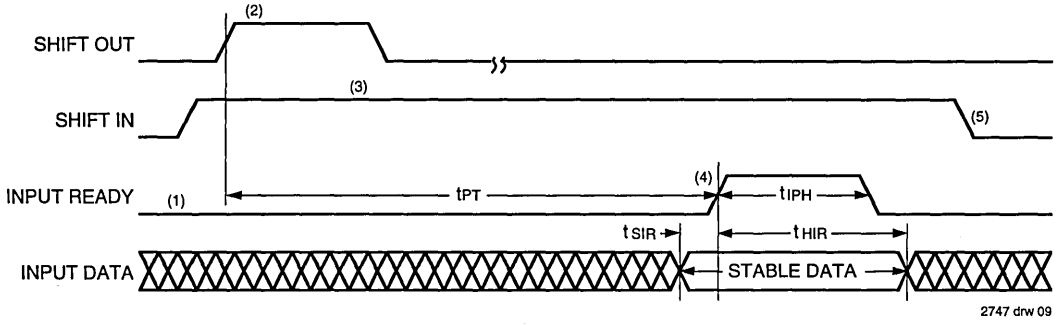
Figure 2. Input Timing



NOTES:
1. Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
2. Input Data is loaded into the first word.
3. Input Ready goes LOW indicating the first word is full.
4. The write pointer is incremented.
5. The FIFO is ready for the next word.
6. If the FIFO is full then the Input Ready remains LOW.
7. Shift In pulses applied while Input Ready is LOW will be ignored (see Figure 4).

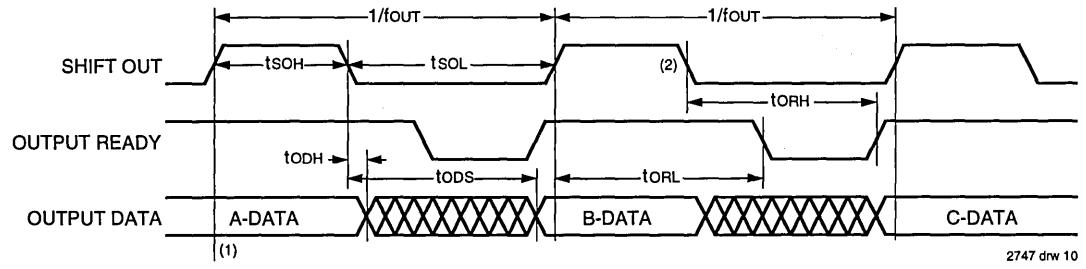
Figure 3. The Mechanism of Shifting Data Into the FIFO

TIMING DIAGRAMS (Continued)



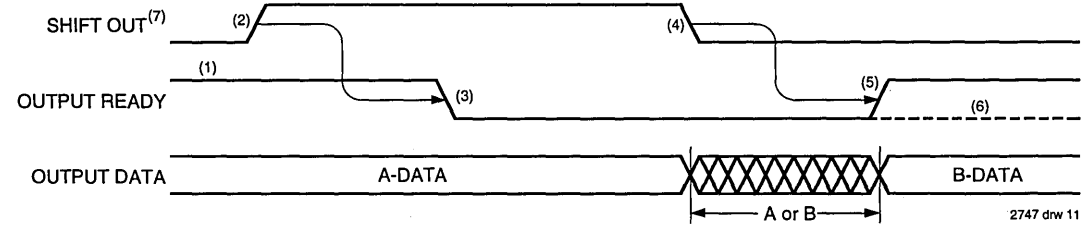
NOTES:
1. FIFO is initially full.
2. Shift Out pulse is applied.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the FIFO.
5. The write pointer is incremented. Shift In should not go LOW until (t_{PT} + t_{IPH}).

Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH



NOTES:
1. This data is loaded consecutively A, B, C.
2. Data is shifted out when Shift Out makes a HIGH to LOW transition.

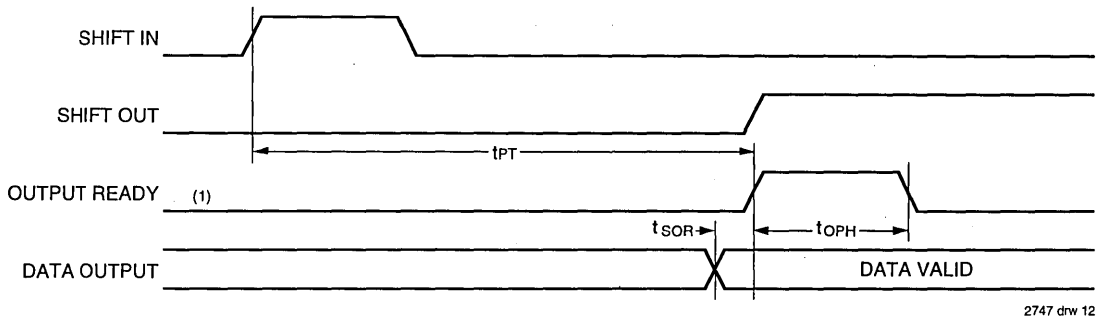
Figure 5. Output Timing



NOTES:
1. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
2. Shift Out goes HIGH causing the next step.
3. Output Ready goes LOW.
4. The read pointer is incremented.
5. Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
6. If the FIFO has only one word loaded (A DATA) then Output Ready stays LOW and the A DATA remains unchanged at the outputs.
7. Shift Out pulses applied when Output Ready is LOW will be ignored.

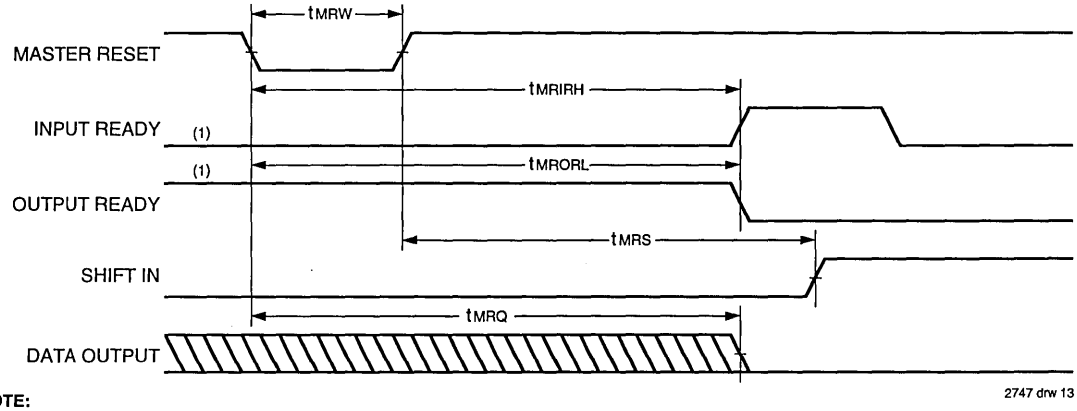
Figure 6. The Mechanism of Shifting Data Out of the FIFO

TIMING DIAGRAMS (Continued)



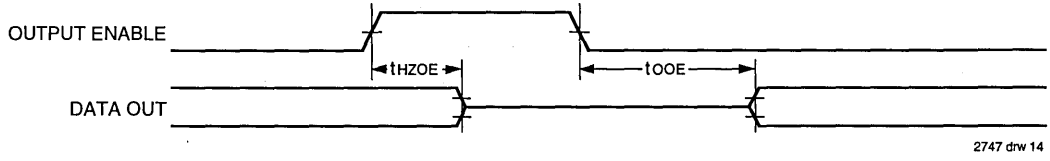
NOTE:
1. FIFO initially empty.

Figure 7. tPT and tOPH Specification



NOTE:
1. Worst case, FIFO initially full..

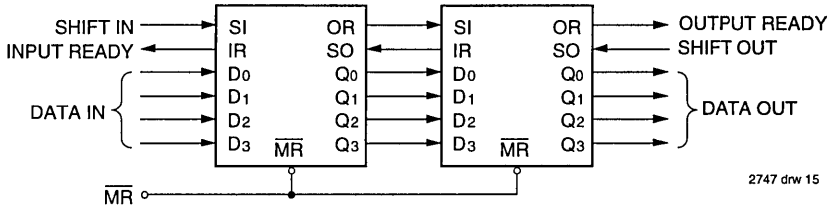
Figure 8. Master Reset Timing



NOTE:
1. High-Z transitions are referenced to the steady-state VOH -500mV and VOL +500mV levels on the output. tHZOE is tested with 5pF load capacitance instead of 30pF as shown in Figure 1.

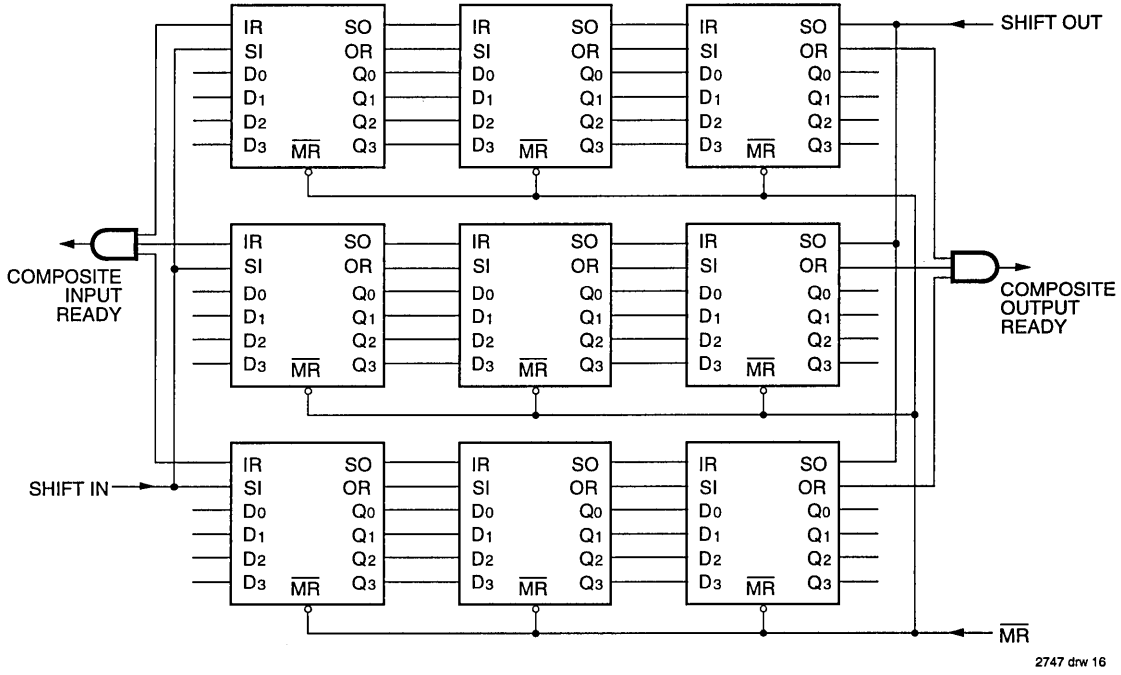
Figure 9. Output Enable Timing, IDT72403 and IDT72404 Only

APPLICATIONS



NOTE:
1. FIFOs can be easily cascaded to any desired path. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

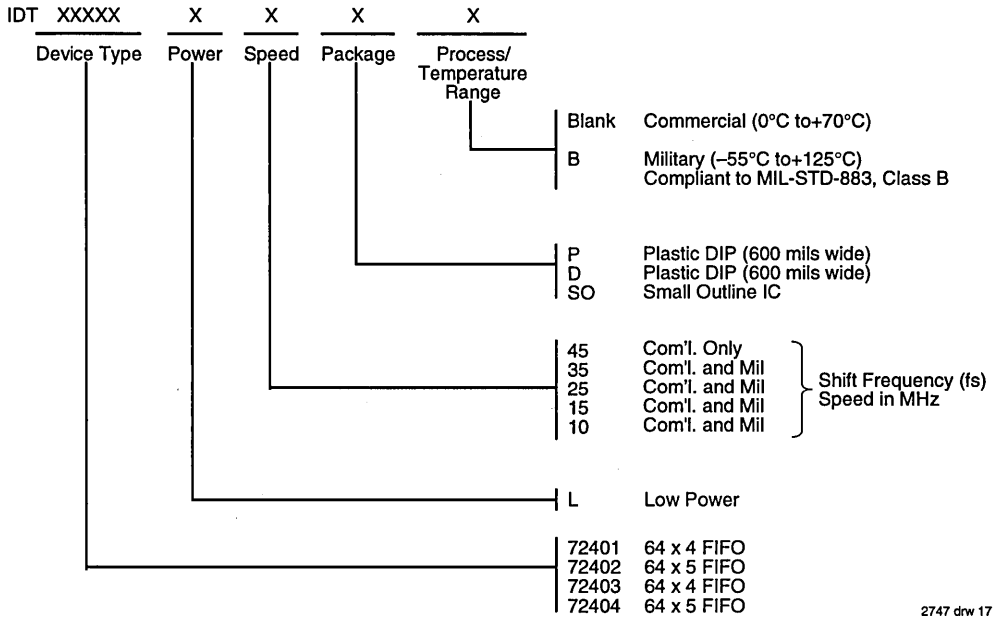
Figure 10. 128 x 4 Depth Expansion



NOTES:
1. When the memory is empty, the last word will remain on the outputs until the Master Reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data and stays LOW until the new data has appeared on the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will appear at the output after a fall-through time. OR will go HIGH for one internal cycle (at least t_{ORL}) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the Master Reset is brought Low, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the Master Reset goes HIGH, the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the Master Reset is ended, IR will go HIGH, but the data in the inputs will not enter the memory until SI goes HIGH.
5. FIFOs are expandable on depth and width. However, in forming wider words, two external gates are required to generate composite Input and Output Ready flags. This is due to the variation of delays of the FIFOs.

Figure 11. 192 x 12 Depth and Width Expansion

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS PARALLEL 64 x 5-BIT FIFO WITH FLAGS

IDT72413

FEATURES:

- First-In/First-Out Dual-Port memory—45MHz
- 64 x 5 organization
- Low-power consumption
  — Active: 200mW (typical)
- RAM-based internal structure allows for fast fall-through time
- Asynchronous and simultaneous read and write
- Expandable by bit width
- Cascadable by word depth
- Half-Full and Almost-Full/Empty status flags
- IDT72413 is pin and functionally compatible with the MMI67413
- High-speed data communications applications
- Bidirectional and rate buffer applications
- High-performance CMOS technology
- Available in plastic DIP, CERDIP and SOIC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72413 is a 64 x 5, high-speed First-In/First-Out (FIFO) that loads and empties data on a first-in-first-out basis. It is expandable in bit width. All speed versions are cascadable in depth.

The FIFO has a Half-Full Flag, which signals when it has 32 or more words in memory. The Almost-Full/Empty Flag is active when there are 56 or more words in memory or when there are 8 or less words in memory.

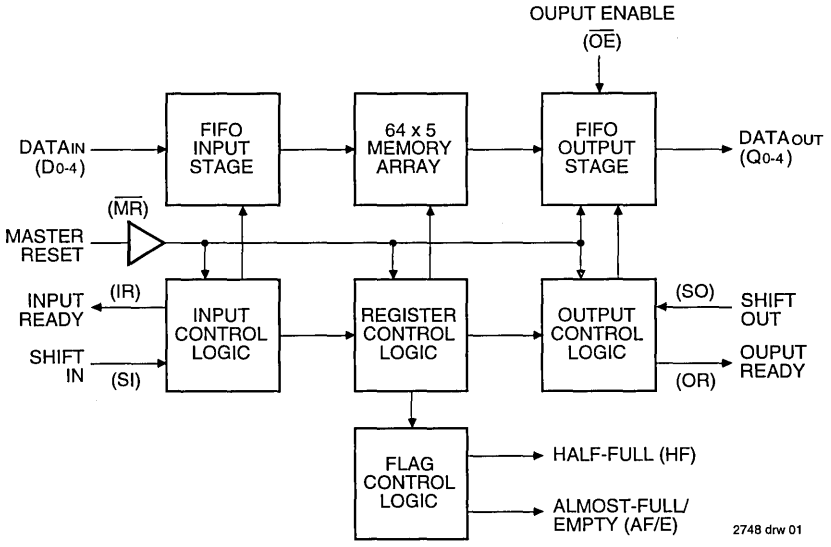
The IDT72413 is pin and functionally compatible to the MMI67413. It operates at a shift rate of 45MHz. This makes it ideal for use in high-speed data buffering applications. The IDT72413 can be used as a rate buffer, between two digital systems of varying data rates, in high-speed tape drivers, hard disk controllers, data communications controllers and graphics controllers.

The IDT72413 is fabricated using IDTs high-performance CMOS process. This process maintains the speed and high output drive capability of TTL circuits in low-power CMOS.

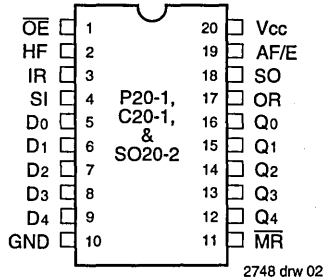
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

5

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP/SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2748 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2748 tbl 02

1. This parameter is sampled and not 100% tested.
2. Characterized values, not currently listed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Military Supply Voltage	4.5	5.0	5.5	V
Vcc	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}(1)	Input Low Voltage	—	—	0.8	V

NOTE: 2748 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	Test Conditions				Min.	Max.	Unit
I_{IL}	Low-Level Input Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}				-10	—	µA
I_{IH}	High-Level Input Current	V_{CC} = Max., GND ≤ V_I ≤ V_{CC}				—	10	µA
V_{OL}	Low-Level Output Current	V_{CC} = Min.	I_{OL} (Q_{0-4})	Mil.	12mA	—	0.4	V
				Com'l.	24mA			
			I_{OL} (IR, OR)[1]		8mA			
			I_{OL} (HF, AF/E)		8mA			
V_{OH}	High-Level Output Current	V_{CC} = Min.	I_{OH} (Q_{0-4})		–4mA	2.4	—	V
			I_{OH} (IR, OR)		–4mA			
			I_{OH} (HF, AF/E)		–4mA			
I_{OS}[2]	Output Short-Circuit Current	V_{CC} = Max.	V_O = 0V			-20	-110	mA
I_{HZ}	Off-State Output Current	V_{CC} = Max.	V_O = 2.4V			—	20	µA
I_{LZ}		V_{CC} = Max.	V_O = 0.4V			-20	—	
I_{CC}[3]	Supply Current	V_{CC} = Max., OE=HIGH		Mil.		—	70	mA
		Inputs LOW, f=25MHz		Com'l.		—	60	

NOTES: 2748 tbl 04

1. Care should be taken to minimize as much as possible the DC and capactive load on IR and OR when operating at frequencies above 25mHz.
2. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. Guaranteed by design, but not currently tested.
3. For frequencies greater than 25MHz, Icc = 60mA + (1.5mA x [f - 25MHz]) commercial and Icc = 70mA + (1.5mA x [f - 25MHz]) military.

5

OPERATING CONDITIONS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = –55°C to +125°C)

			Military		Military & Commercial		Commercial		
			IDT72413L45		IDT72413L35		IDT72413L25		
Symbol	Parameters	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_{SIH}[1]	Shift in HIGH Time	2	9	—	9	—	16	—	ns
t_{SIL}[1]	Shift in LOW TIme	2	11	—	17	—	20	—	ns
t_{IDS}	Input Data Set-up	2	0	—	0	—	0	—	ns
t_{IDH}	Input Data Hold Time	2	13	—	15	—	25	—	ns
t_{SOH}[1]	Shift Out HIGH Time	5	9	—	9	—	16	—	ns
t_{SOL}	Shift Out LOW Time	5	11	—	17	—	20	—	ns
t_{MRW}	Master Reset Pulse	8	20	—	30	—	35	—	ns
t_{MRS}	Master Reset Pulse to SI	8	20	—	35	—	35	—	ns

NOTE: 2748 tbl 05

1. Since the FIFO is a very high-speed device, care must be excercised in the design of the hardware and timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between VCC and GND with very short lead length is recommended.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = –55°C to +125°C)

			Military		Military & Commercial				
			IDT72413L45		IDT72413L35		IDT72413L25		
Symbol	Parameters	Figure	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_{IN}	Shift In Rate	2	—	45	—	35	—	25	MHz
t_{IRL}[1]	Shift In ↑ to Input Ready LOW	2	—	18	—	18	—	28	ns
t_{IRH}[1]	Shift In ↓ to Input Ready HIGH	2	—	18	—	20	—	25	ns
f_{OUT}	Shift Out Rate	5	—	45	—	35	—	25	MHz
t_{ORL}[1]	Shift Out ↓ to Output Ready LOW	5	—	18	—	18	—	28	ns
t_{ORH}[1]	Shift Out ↓ to Output Ready HIGH	5	—	19	—	20	—	25	ns
t_{ODH}[1]	Output Data Hold Previous Word	5	5	—	5	—	5	—	ns
t_{ODS}	Output Data Shift Next Word	5	—	19	—	20	—	20	ns
t_{PT}	Data Throughput or "Fall-Through"	4, 7	—	25	—	28	—	40	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8	—	25	—	28	—	30	ns
t_{MRIRH}[3]	Master Reset ↑ to Input Ready HIGH	8	—	25	—	28	—	30	ns
t_{MRIRL}[2]	Master Reset ↓ to Input Ready LOW	8	—	25	—	28	—	30	ns
t_{MRQ}	Master Reset ↓ to Outputs LOW	8	—	20	—	25	—	35	ns
t_{MRHF}	Master Reset ↓ to Half-Full Flag	8	—	25	—	28	—	40	ns
t_{MRAFE}	Master Reset ↓ to AF/E Flag	8	—	25	—	28	—	40	ns
t_{IPH}[3]	Input Ready Pulse HIGH	4	5	—	5	—	5	—	ns
t_{OPH}[3]	Ouput Ready Pulse HIGH	7	5	—	5	—	5	—	ns
t_{ORD}[3]	Output Ready ↑ HIGH to Valid Data	5	—	5	—	5	—	7	ns
t_{AEH}	Shift Out ↑ to AF/E HIGH	9	—	28	—	28	—	40	ns
t_{AEL}	Shift In ↑ to AF/E	9	—	28	—	28	—	40	ns
t_{AFL}	Shift Out ↑ to AF/E LOW	10	—	28	—	28	—	40	ns
t_{AFH}	Shift In ↑ to AF/E HIGH	10	—	28	—	28	—	40	ns
t_{HFH}	Shift In ↑ to HF HIGH	11	—	28	—	28	—	40	ns
t_{HFL}	Shif Out ↑ to HF LOW	11	—	28	—	28	—	40	ns
t_{PHZ}[3]	Output Disable Delay	12	—	12	—	12	—	15	ns
t_{PLZ}[3]		12	—	12	—	12	—	15	
t_{PLZ}[3]	Output Enable Delay	12	—	15	—	15	—	20	ns
t_{PHZ}[3]		12	—	15	—	15	—	20	

NOTES:

2748 tbl 06

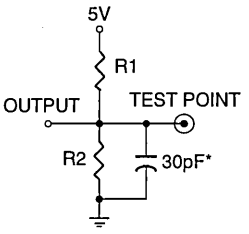
1. Since the FIFO is a very high-speed device, care must be taken in the design of the hardware and the timing utilized within the design. Device grounding and decoupling are crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. A monolithic ceramic capacitor of 0.1µF directly between VCC and GND with very short lead length is recommended.
2. If the FIFO is full, (IR = HIGH), $\overline{MR}$ ↓ forces IR to go LOW, and $\overline{MR}$ ↑ causes IR to go HIGH.
3. Guaranteed by design but not currently tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

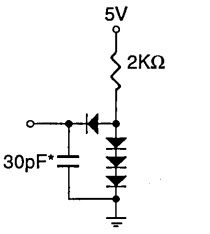
2748 tbl 07

STANDARD TEST LOAD



or equivalent circuit

DESIGN TEST LOAD



2748 drw 03

*Including scope and jig

RESISTOR VALUES FOR STANDARD TEST LOAD

I_{OL}	R1	R2
24mA	200Ω	300Ω
12mA	390Ω	760Ω
8mA	600Ω	1200Ω

2748 tbl 08

Figure 1. Output Load

5

FUNCTIONAL DESCRIPTION:

The IDT72413, 65 x 5 FIFO is designed using a dual-port RAM architecture as opposed to the traditional shift register approach. This FIFO architecture has a write pointer, a read pointer and control logic, which allow simultaneous read and write operations. The write pointer is incremented by the falling edge of the Shift In (SI) control; the read pointer is incremented by the falling edge of the Shift Out (SO). The Input Ready (IR) signals when the FIFO has an available memory location; Output Ready (OR) signals when there is valid data on the output. Output Enable ($\overline{OE}$) provides the capability of three-stating the FIFO outputs.

FIFO RESET

The FIFO must be reset upon power up using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state signified by Output Ready (OR) being LOW and Input Ready (IR) being HIGH. In this state, the data outputs (Q_{0-4}) will be LOW.

DATA INPUT

Data is shifted in on the LOW-to-HIGH transition of Shift In (SI). This loads input data into the first word location of the FIFO and causes the Input Ready to go LOW. On the HIGH-to-LOW transition of Shift In, the write pointer is moved to the next word position and Input Ready (IR) goes HIGH indicating the readiness to accept new data. If the FIFO is full, Input Ready will remain LOW until a word of data is shifted out.

DATA OUTPUT

Data is shifted out on the HIGH-to-LOW transition of Shift Out (SO). This causes the internal read pointer to be advanced to the next word location. If data is present, valid data will appear on the outputs and Output Ready (OR) will go HIGH. If data is not present, Output Ready will stay LOW indicating the FIFO is empty. The last valid word read from the FIFO will remain at the FIFOs output when it is empty. When the FIFO is not empty Output Ready (OR) goes LOW on the LOW-to-HIGH transition of Shift Out.

FALL-THROUGH MODE

The FIFO operates in a Fall-Through Mode when data gets shifted into an empty FIFO. After the fall-through delay the data propagates to the output. When the data reaches the output, the Output Ready (OR) goes HIGH.

A Fall-Through Mode also occurs when the FIFO is completely full. When data is shifted out of the full FIFO a location is available for new data. After a fall-through delay, the Input Ready goes HIGH. If Shift In is HIGH, the new data can be written to the FIFO. The fall-through delay of a RAM-based FIFO (one clock cycle) is far less than the delay of a Shift register-based FIFO.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA INPUT (D_{0-4})

Data input lines. The IDT72413 has a 5-bit data input.

CONTROLS:

SHIFT IN (SI)

Shift In controls the input of the data into the FIFO. When SI is HIGH, data can be written to the FIFO via the D0-4 lines. The data has to meet set-up and hold time requirements with respect to the rising edge of SI.

SHIFT OUT (SO)

Shift Out controls the outputs data from the FIFO.

MASTER RESET (MR)

Master Reset clears the FIFO of any data stored within. Upon power up, the FIFO should be cleared with a Master Reset. Master Reset is active LOW.

HALF-FULL FLAG (HF)

Half-Full Flag signals when the FIFO has 32 or more words in it.

INPUT READY(IR)

When Input Ready is HIGH, the FIFO is ready for new input data to be written to it. When IR is LOW, the FIFO is unavailable for new input data, Input Ready is also used to cascade many FIFOs together, as shown in Figure 13 in the Applications section.

OUTPUT READY (OR)

When Output Ready is HIGH, the output (Q_{0-4}) contains valid data. When OR is LOW, the FIFO is unavailable for new output data. Output Ready is also used to cascade many FIFOs together, as shown in Figure 13 in the Applications section.

OUTPUT ENABLE (OE)

Output Enable is used to enable the FIFO outputs onto a bus. Output Enable is active LOW.

ALMOST-FULL/EMPTY FLAG (AFE)

Almost-Full/Empty Flag signals when the FIFO is 7/8 full (56 or more words) or 1/8 from empty (8 or less words).

OUTPUTS:

DATA OUTPUT (Q_{0-4})

Data output lines, three-state. The IDT72413 has a 5-bit output.

TIMING DIAGRAMS

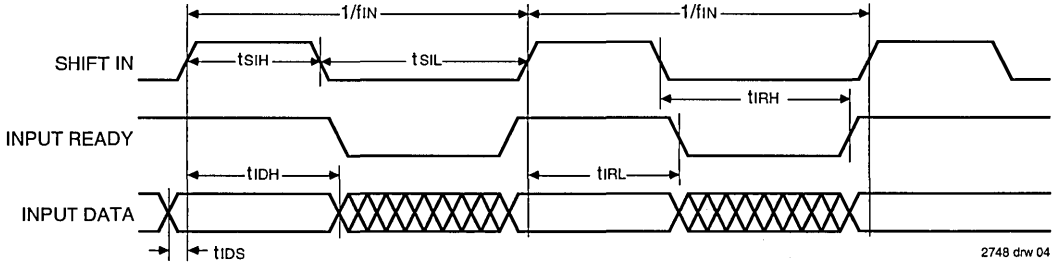


Figure 2. Input Timing

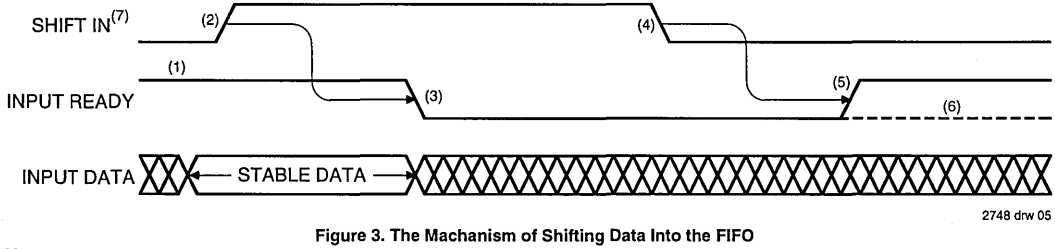
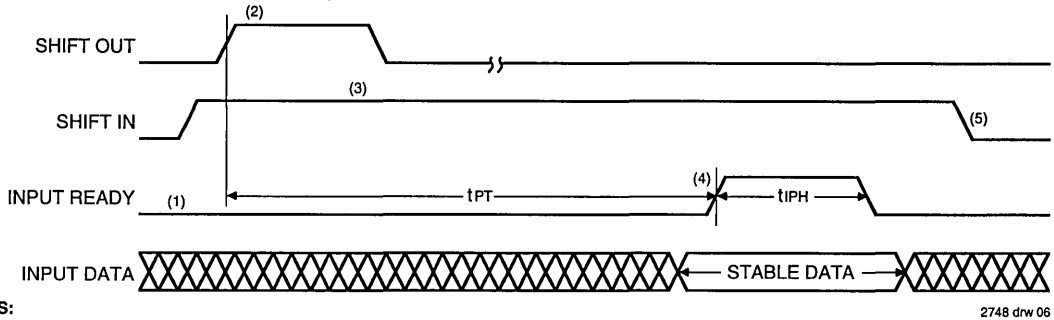


Figure 3. The Machanism of Shifting Data Into the FIFO

NOTES:

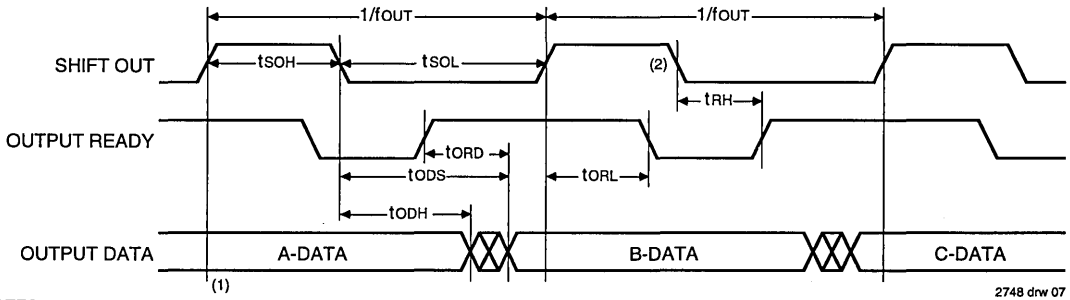
1. Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
2. Input Data is loaded into the FIFO.
3. Input Ready goes LOW indicating the FIFO is unavailable for new data.
4. The write pointer is incremented.
5. The FIFO is ready for the next word.
6. If the FIFO is full, then the Input Ready remains LOW.
7. **Shift In pulses applied while Input Ready is LOW will be ignored (see Figure 4).**

TIMING DIAGRAMS (Continued)



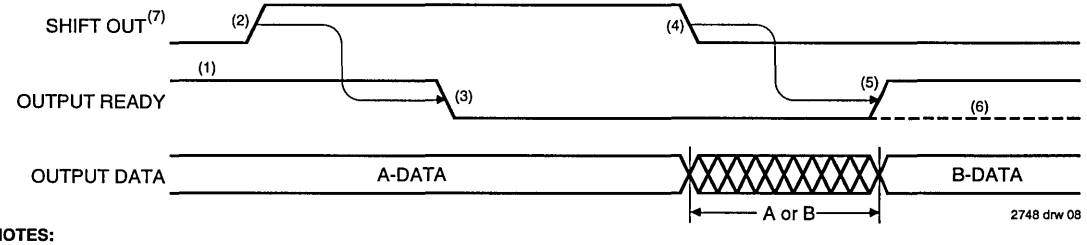
NOTES:
1. FIFO is initially full.
2. Shift Out pulse is applied.
3. Shift In is held HIGH.
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the FIFO.
5. The write pointer is incremented. Shift In should not go LOW until (tPT + tIPH).

Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH



NOTES:
1. This data is loaded consecutively A, B, C.
2. Output data changes on the falling edge of SO after a valid Shift Out sequence, i.e., OR and SO are both high together.

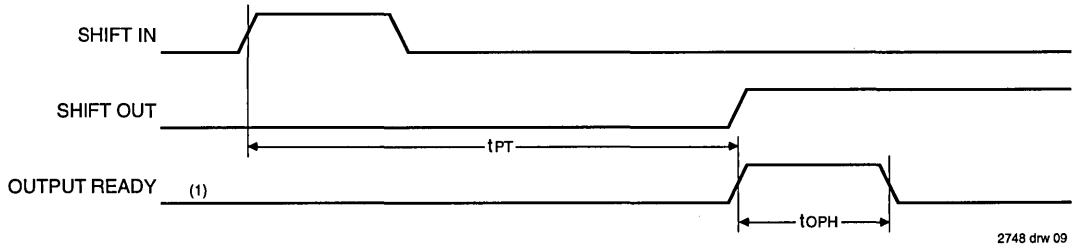
Figure 5. Output Timing



NOTES:
1. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
2. Shift Out goes HIGH causing the next step.
3. Output Ready goes LOW.
4. Read pointer is incremented.
5. Output Ready goes HIGH indicating that new data (B) will be available at the FIFO outputs after tORD ns.
6. If the FIFO has only one word loaded (A DATA) , Output Ready stays LOW and the A-DATA remains unchanged at the outputs.
7. Shift Out pulses applied when Output Ready is LOW will be ignored.

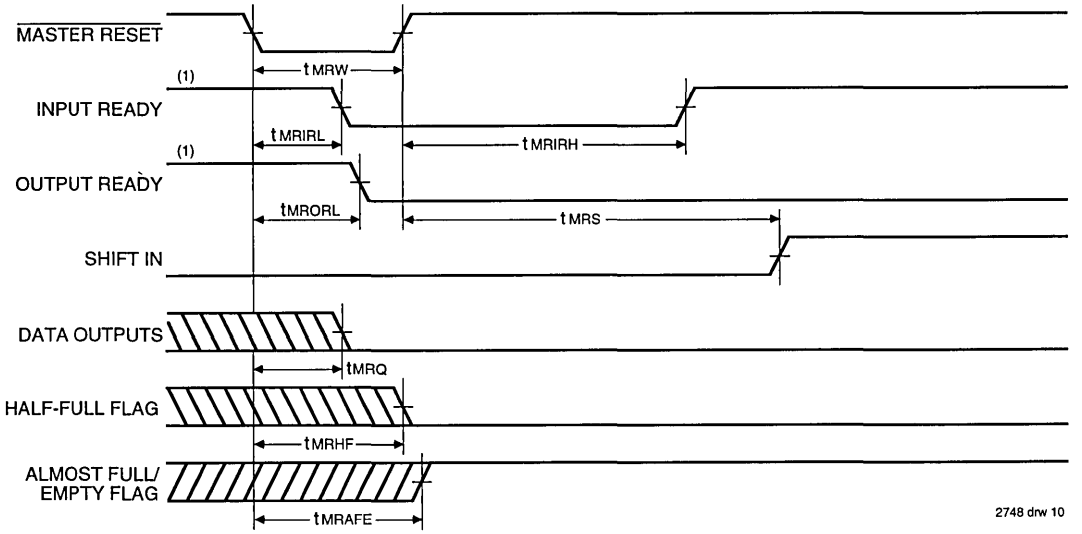
Figure 6. The Mechanism of Shifting Data Out of the FIFO

TIMING DIAGRAMS (Continued)



NOTE:
1. FIFO initailly empty.

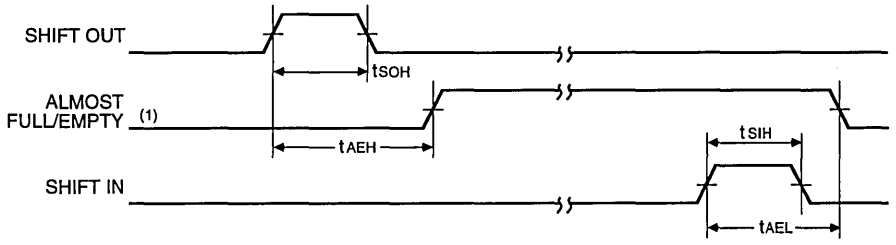
Figure 7. tPT and tOPH Specification



NOTE:
1. FIFO is partially full..

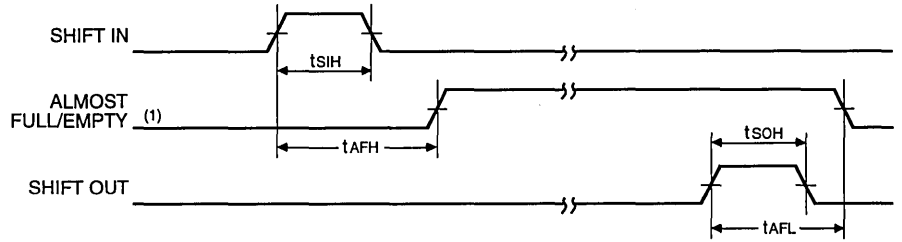
Figure 8. Master Reset Timing

TIMING DIAGRAMS (Continued)



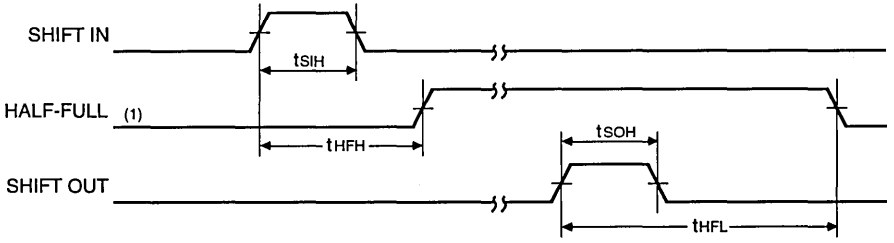
NOTE:
1. FIFO contains 9 words (one more than Almost-Empty).

Figure 9. t_{AEH} and t_{AEL} Specifications



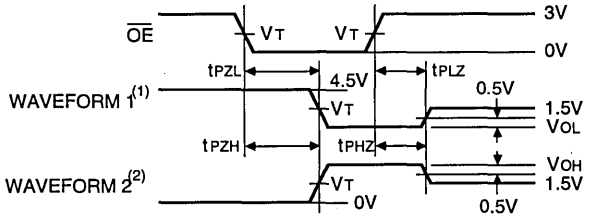
NOTE:
1. FIFO contains 55 words (one short of Almost-Full).

Figure 10. t_{AFH} and t_{AFL} Specifications



NOTE:
1. FIFO contains 31 words (one short of Half-Full).

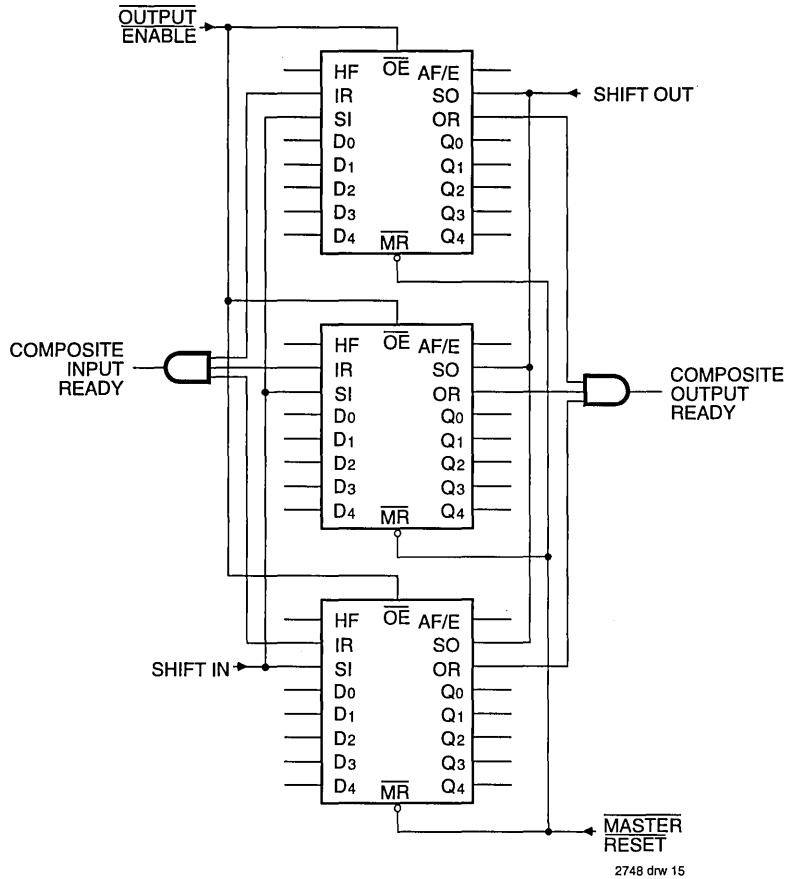
Figure 11. t_{HFL} and t_{HFH} Specifications



NOTES:
1. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.

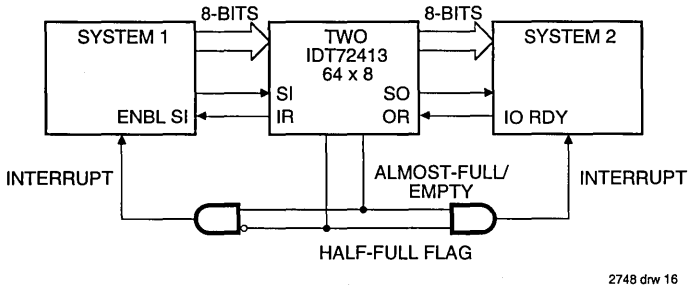
Figure 12. Enable and Disable

APPLICATIONS



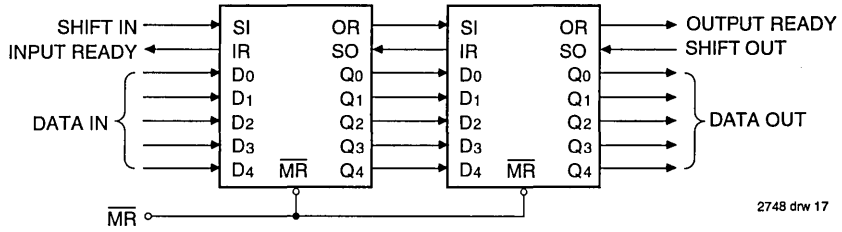
NOTE:
1. FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This requirement is due to the different fall-through times of the FIFOs.

Figure 13. 64 x 15 FIFO with IDT72413



NOTE:
1. Cascading the FIFOs in word width is done by ANDing the IR and OR as shown in Figure 13.

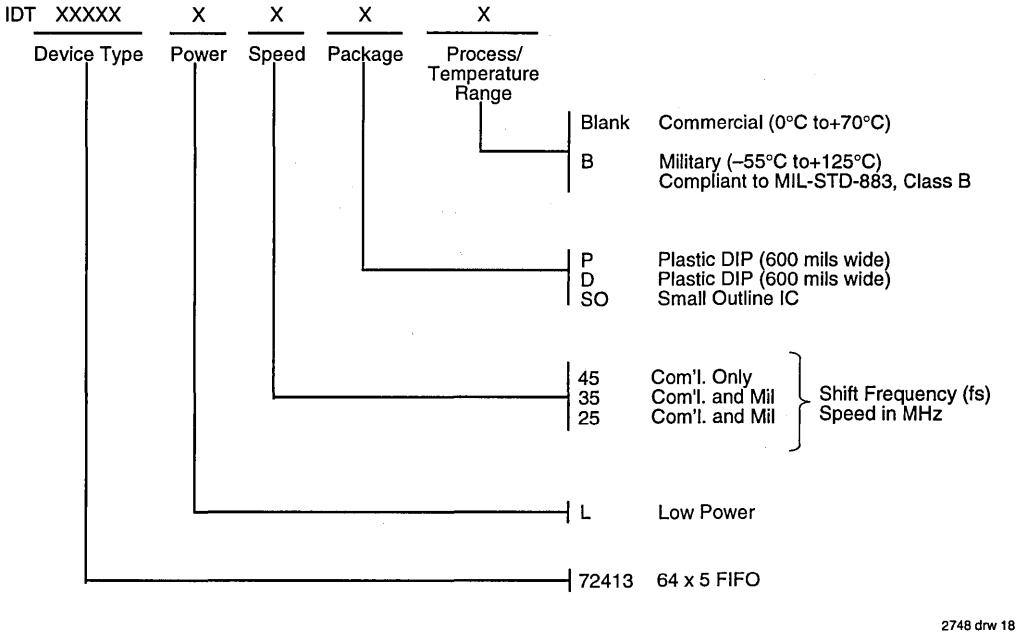
Figure 14. Application for IDT72413 for Two Asynchronous Systems



NOTE:
1. FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

Figure 15. 128 x 5 Depth Expansion

ORDERING INFORMATION



5

Integrated Device Technology, Inc.

CMOS ASYNCHRONOUS FIFO 256 x 9, 512 x 9, 1K x 9

IDT7200L
IDT7201LA
IDT7202LA

FEATURES:

- First-In/First-Out dual-port memory
- 256 x 9 organization (IDT7200)
- 512 x 9 organization (IDT7201)
- 1K x 9 organization (IDT7202)
- Low power consumption
  - — Active: 770mW (max.)
  - —Power-down: 2.75mW (max.)
- Ultra high speed—12ns access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Pin and functionally compatible with 720X family
- Status Flags: Empty, Half-Full, Full
- Auto-retransmit capability
- High-performance CEMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-87531, 5962-89666, 5962-89863 and 5962-89536 are listed on this function.

DESCRIPTION:

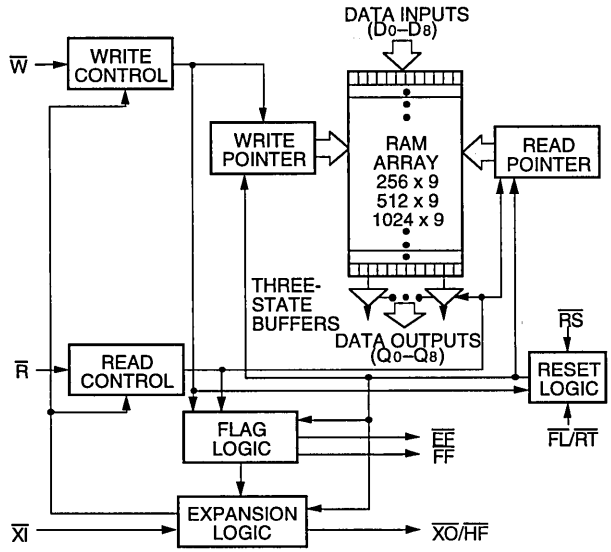
The IDT7200/7201/7202 are dual-port memories that load and empty data on a first-in/first-out basis. The devices use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins.

The devices utilizes a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

The IDT7200/7201/7202 are fabricated using IDT's high-speed CMOS technology. They are designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

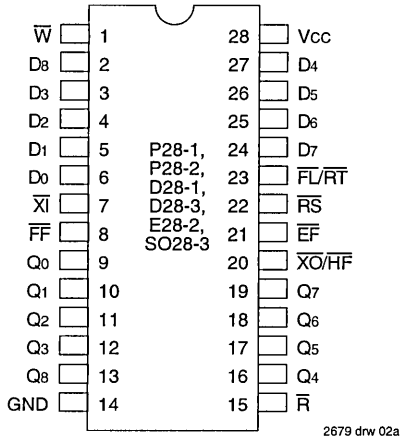
FUNCTIONAL BLOCK DIAGRAM



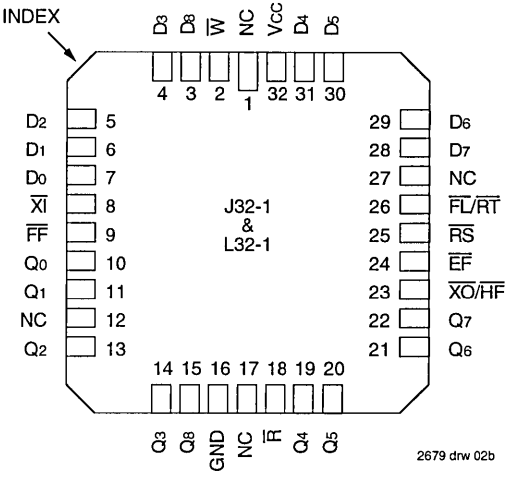
2679 drw 01

The IDT logo is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC/PLCC
TOP VIEW

NOTE:
1. CERPACK (E28-2) and 600-mil-wide DIP (P28-1 and D28-1) not available for 7200.

NOTE:
1. LCC (L32-1) not available for 7200.

5

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
IOUT	DC Output Current	50	50	mA

2679 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIH(1)	Input High Voltage Military	2.2	—	—	V
VIL(2)	Input Low Voltage Commercial and Military	—	—	0.8	V

2679 tbl 03

NOTE:
1. VIH = 2.6V for XI input (commercial).
   VIH = 2.8V for XI input (military).
2. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

2679 tbl 02

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT7200L IDT7201LA IDT7202LA Commercial t_A = 12, 15, 20 ns			IDT7200L IDT7201LA IDT7202LA Military t_A = 20 ns			IDT7200L IDT7201LA IDT7202LA Commercial t_A = 25, 35 ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[1]	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	–1	—	1	µA
I_{LO}[2]	Output Leakage Current	–10	—	10	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	—	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	V
I_{CC1}[3]	Active Power Supply Current	—	—	125[4]	—	—	140[4]	—	—	125[4]	mA
I_{CC2}[3]	Standby Current ($\overline{R}$=W=RS=FL/RT=V_{IH})	—	—	15	—	—	20	—	—	15	mA
$I_{CC3(L)}$[3]	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	0.5	—	—	0.9	—	—	0.5	mA

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open (only capacitive loading).
4. Tested at f = 20MHz.

2679 tbl 04

DC ELECTRICAL CHARACTERISTICS (Continued)

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT7200L IDT7201LA IDT7202LA Military t_A = 30, 40 ns			IDT7200L IDT7201LA IDT7202LA Commercial t_A = 50 ns			IDT7200L IDT7201LA IDT7202LA Military t_A = 50, 65, 80, 120 ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[1]	Input Leakage Current (Any Input)	–10	—	10	–1	—	1	–10	—	10	µA
I_{LO}[2]	Output Leakage Current	–10	—	10	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	—	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	V
I_{CC1}[3]	Active Power Supply Current	—	—	140[4]	—	50	80	—	70	100	mA
I_{CC2}[3]	Standby Current ($\overline{R}$=W=RS=FL/RT=V_{IH})	—	—	20	—	5	8	—	8	15	mA
$I_{CC3(L)}$[3]	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	0.9	—	—	0.5	—	—	0.9	mA

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open (only capacitive loading).
4. Tested at f = 20MHz.

2679 tbl 05

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = –55°C to +125°C)

		Commercial				Com'l & Mil.		Com'l		Military		Com'l		
		7200L12 7201LA12 7202LA12		7200L15 7201LA15 7202LA15		7200L20 7201LA20 7202LA20		7200L25 7201LA25 7202LA25		7200L30 7201LA30 7202LA30		7200L35 7201LA35 7202LA35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Shift Frequency	—	50	—	40	—	33.3	—	28.5	—	25	—	22.2	MHz
t_{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_A	Access Time	—	12	—	15	—	20	—	25	—	30	—	35	ns
t_{RR}	Read Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[3]	3	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[3, 4]	3	—	5	—	5	—	5	—	5	—	10	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[3]	—	12	—	15	—	15	—	18	—	20	—	20	ns
t_{WC}	Write Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_{WPW}	Write Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	9	—	11	—	12	—	15	—	18	—	18	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_{RS}	Reset Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RSS}	Reset Set-up Time[3]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RSR}	Reset Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{RTC}	Retransmit Cycle Time	20	12	—	25	—	30	—	35	—	40	—	45	ns
t_{RT}	Retransmit Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RTS}	Retransmit Set-up Time[3]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RTR}	Retransmit Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to Empty Flag Low	—	12	—	25	—	30	—	35	—	40	—	45	ns
$t_{HFH,FFH}$	Reset to Half-Full and Full Flag High	—	17	—	25	—	30	—	35	—	40	—	45	ns
t_{RTF}	Retransmit Low to Flags Valid	—	20	—	25	—	30	—	35	—	40	—	45	ns
t_{REF}	Read Low to Empty Flag Low	—	12	—	15	—	20	—	25	—	30	—	30	ns
t_{RFF}	Read High to Full Flag High	—	14	—	15	—	20	—	25	—	30	—	30	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{WEF}	Write High to Empty Flag High	—	12	—	15	—	20	—	25	—	30	—	30	ns
t_{WFF}	Write Low to Full Flag Low	—	14	—	15	—	20	—	25	—	30	—	30	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	17	—	25	—	30	—	35	—	40	—	45	ns
t_{RHF}	Read High to Half-Full Flag High	—	17	—	25	—	30	—	35	—	40	—	45	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	12	—	15	—	20	—	25	—	30	—	35	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	12	—	15	—	20	—	25	—	30	—	35	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	8	—	10	—	10	—	10	—	10	—	10	—	ns

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

2679 tbl 06

AC ELECTRICAL CHARACTERISTICS[1] (Continued)

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = –55°C to +125°C)

		Military		Com'l & Mil.		Military[2]						
		7200 L40 7201LA40 7202LA40		7200L50 7201LA50 7202LA50		7200L65 7201LA65 7202LA65		7200L80 7201LA80 7202LA80		7200L120 7201LA120 7202LA120		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_S	Shift Frequency	—	20	—	15	—	12.5	—	10	—	7	MHz
t_{RC}	Read Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_A	Access Time	—	40	—	50	—	65	—	80	—	120	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{RPW}	Read Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z[4]	5	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}	Write Pulse High to Data Bus at Low Z[4, 5]	10	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z[4]	—	25	—	30	—	30	—	30	—	35	ns
t_{WC}	Write Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{WPW}	Write Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Set-up Time	20	—	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	5	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{RS}	Reset Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RSS}	Reset Set-up Time[4]	40	—	50	—	65	—	80	—	120	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{RT}	Retransmit Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RTS}	Retransmit Set-up Time[4]	40	—	50	—	65	—	80	—	120	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to Empty Flag Low	—	50	—	65	—	80	—	100	—	140	ns
$t_{HFH,FFH}$	Reset to Half-Full and Full Flag High	—	50	—	65	—	80	—	100	—	140	ns
t_{RTF}	Retransmit Low to Flags Valid	—	50	—	65	—	80	—	100	—	140	ns
t_{REF}	Read Low to Empty Flag Low	—	30	—	45	—	60	—	60	—	60	ns
t_{RFF}	Read High to Full Flag High	—	35	—	45	—	60	—	60	—	60	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ High	40	—	50	—	65	—	80	—	120	—	ns
t_{WEF}	Write High to Empty Flag High	—	35	—	45	—	60	—	60	—	60	ns
t_{WFF}	Write Low to Full Flag Low	—	35	—	45	—	60	—	60	—	60	ns
t_{WHF}	Write Low to Half-Full Flag Low	—	50	—	65	—	80	—	100	—	140	ns
t_{RHF}	Read High to Half-Full Flag High	—	50	—	65	—	80	—	100	—	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ High	40	—	50	—	65	—	80	—	120	—	ns
t_{XOL}	Read/Write to $\overline{XO}$ Low	—	40	—	50	—	65	—	80	—	120	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	—	40	—	50	—	65	—	80	—	120	ns
t_{XI}	$\overline{XI}$ Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	10	—	15	—	15	—	15	—	15	—	ns

NOTES:

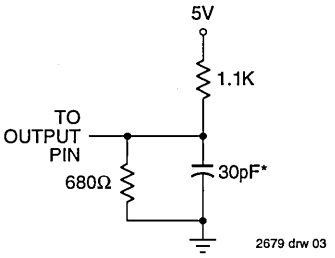
1. Timings referenced as in AC Test Conditions
2. Speed grades 65, 80 and 120 not available in the CERPACK
3. Pulse widths less than minimum value are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode.

2679 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2679 tbl 08



or equivalent circuit

Figure 1. Output Load

* Includes scope and jig capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN ($D_0 - D_8$)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the high state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to high after Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes high, the Data Outputs ($Q_0 - Q_8$) will return to a high impedance condition until the next Read operation. When all data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go high after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the restransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7200/7201A/7202A can be made to retransmit data when the Retransmit Enable control ($\overline{RT}$) input is pulsed low. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the high state during retransmit. This feature is useful when less than 256/512/1024 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-Flag ($\overline{FF}$) will go low after 256 writes for IDT7200, 512 writes for the IDT7201A and 1024 writes for the IDT7202A.

5

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by using rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS ($Q_0 - Q_8$)

Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read ($\overline{R}$) is in a high state.

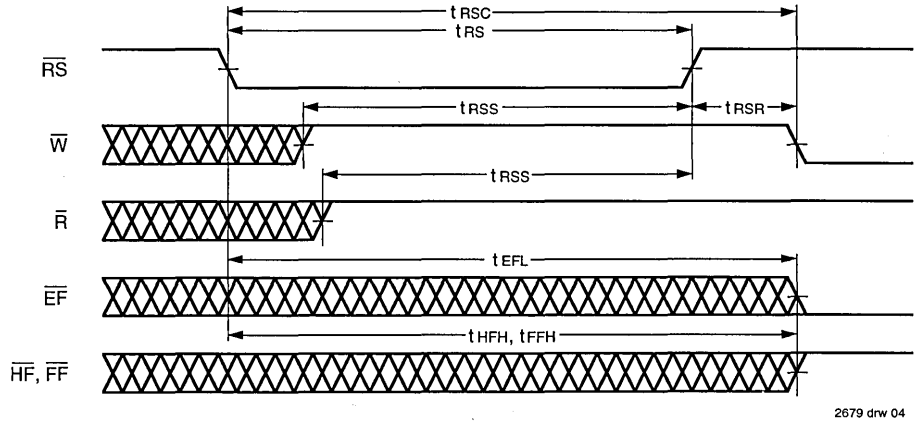


Figure 2. Reset

NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

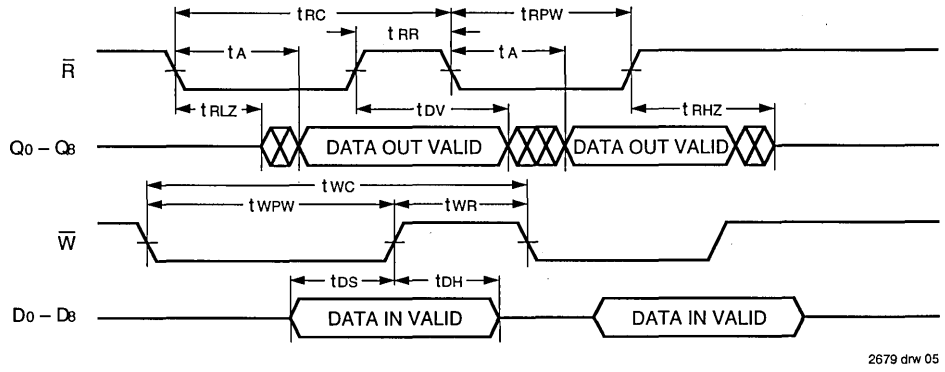


Figure 3. Asynchronous Write and Read Operation

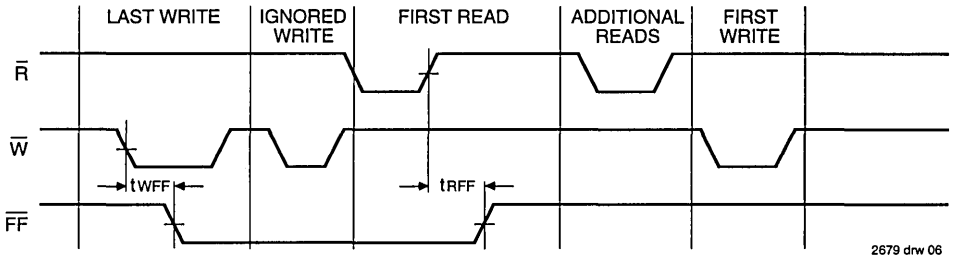


Figure 4. Full Flag From Last Write to First Read

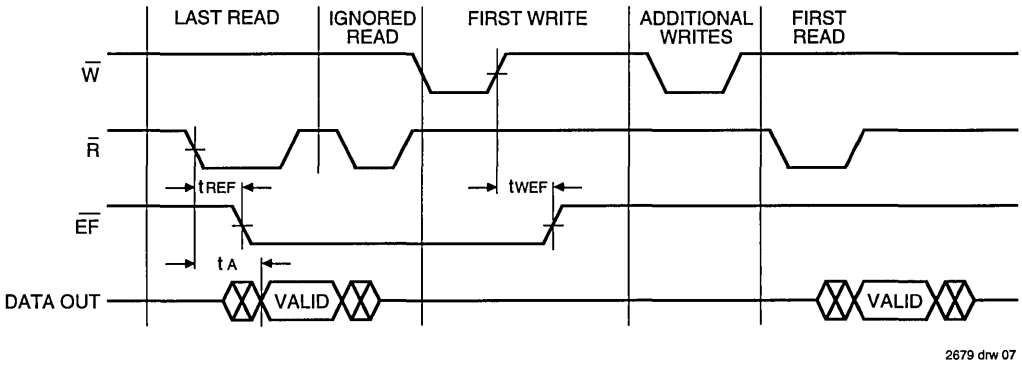


Figure 5. Empty Flag From Last Read to First Write

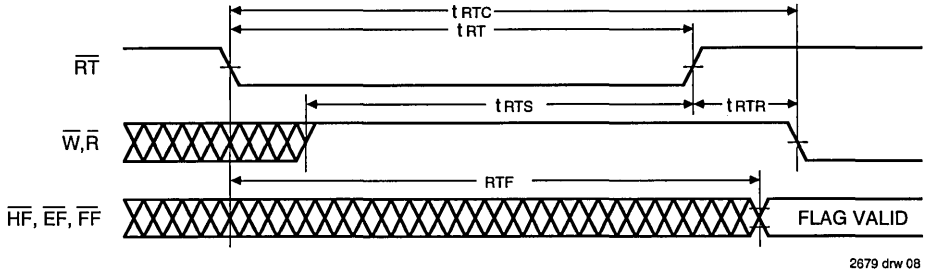


Figure 6. Retransmit

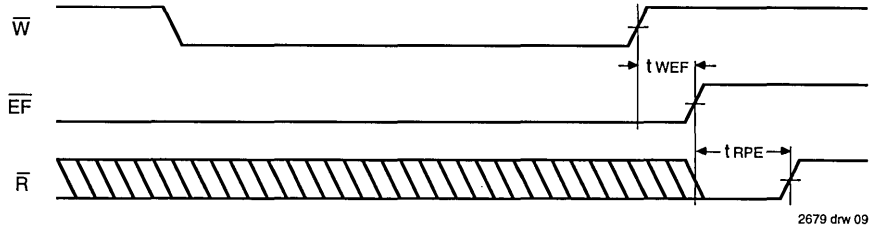


Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse

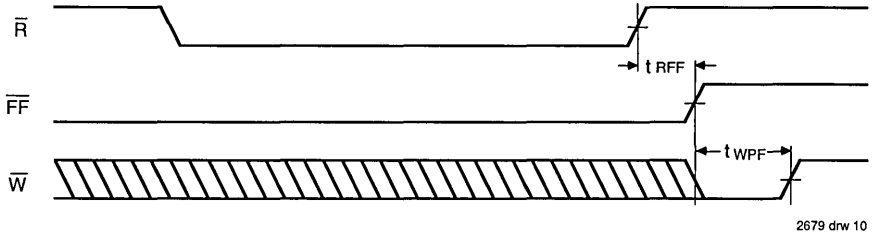


Figure 8. Minimum Timing for an Full Flag Coincident Write Pulse

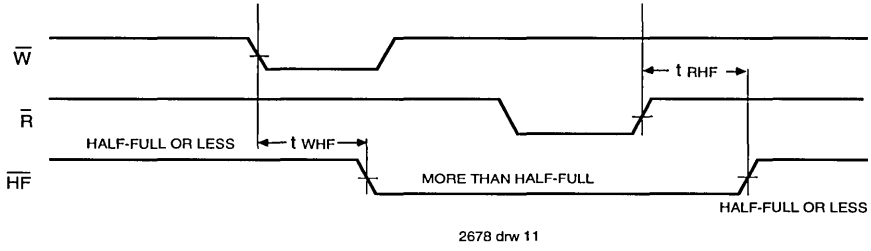


Figure 9. Half-Full Flag Timing

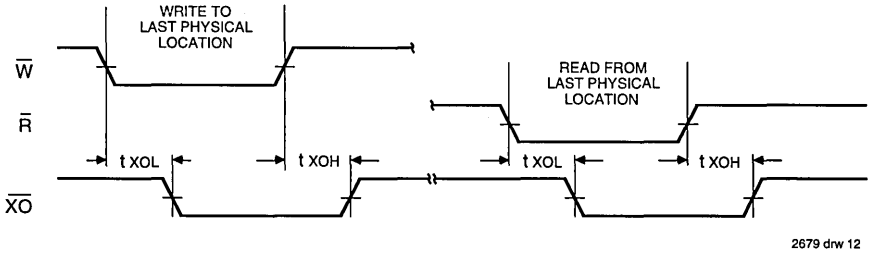


Figure 10. Expansion Out

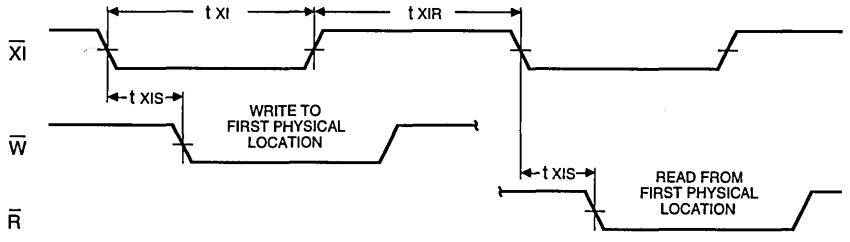


Figure 11. Expansion In

OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

Single Device Mode

A single IDT7200/7201A/7202A may be used when the application requirements are for 256/512/1024 words or less. The IDT7200/7201A/7202A is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

Depth Expansion

The IDT7200/7201A/7202A can easily be adapted to applications when the requirements are for greater than 256/512/1024 words. Figure 14 demonstrates Depth Expansion using three IDT7200/7201A/7202As. Any depth can be attained by adding additional IDT7200/7201A/7202As. The IDT7200/7201A/7202A operates in the Depth Expansion mode when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

USAGE MODES:

Width Expansion

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7200/7201A/7202As. Any word width can be attained by adding additional IDT7200/7201A/7202As (Figure 13).

Bidirectional Operation

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7200/7201A/7202As as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

Compound Expansion

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

5

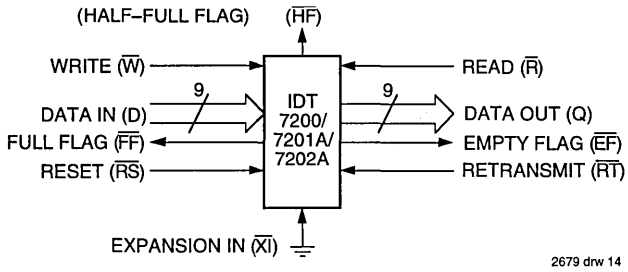


Figure 12. Block Diagram of Single 256/512/1024 x 9 FIFO

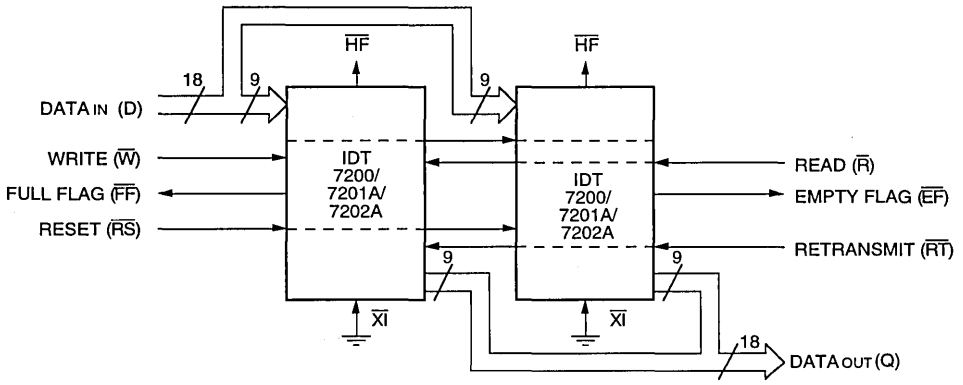


Figure 13. Block Diagram of 256/512/1024 x 18 FIFO Memory Used in Width Expansion Mode

TABLE I—RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if flag is High.

2679 tbl 09

TABLE II—RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Flag Full Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

2679 tbl 10

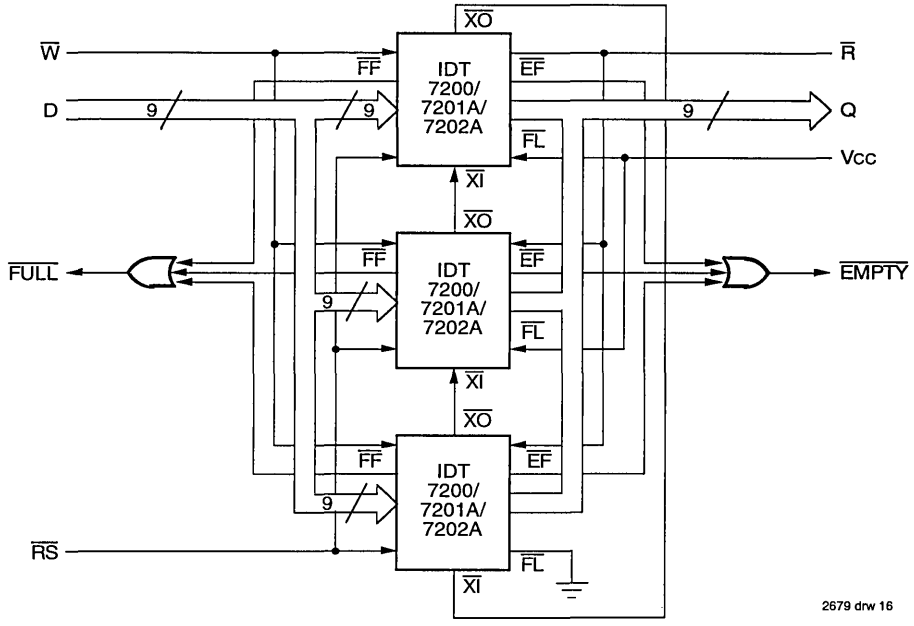


Figure 14. Block Diagram of 768 x 9/1536 x 9/3072 x 9 FIFO Memory (Depth Expansion)

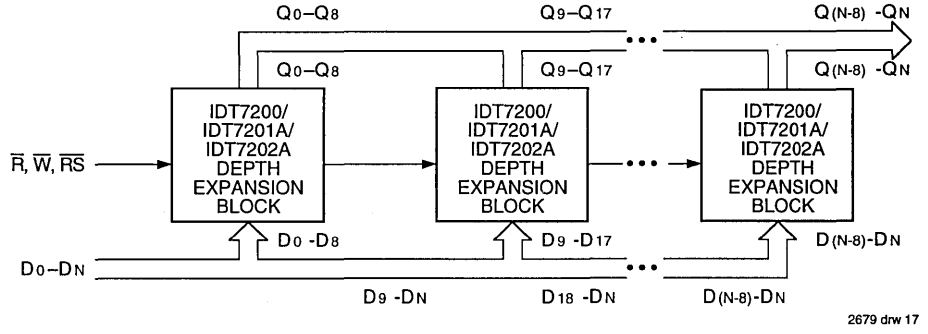


Figure 15. Compound FIFO Expansion

NOTES:
1. For depth expsansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

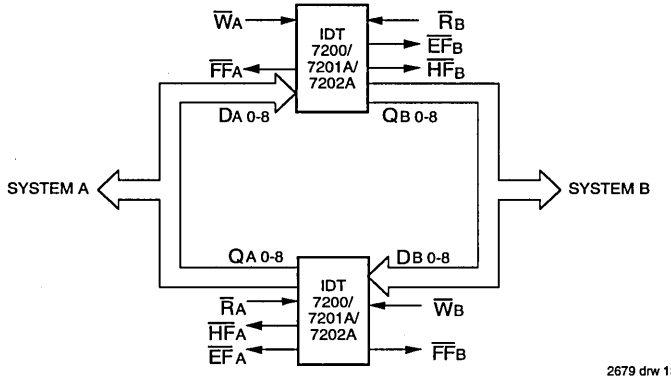


Figure 16. Bidirectional FIFO Mode

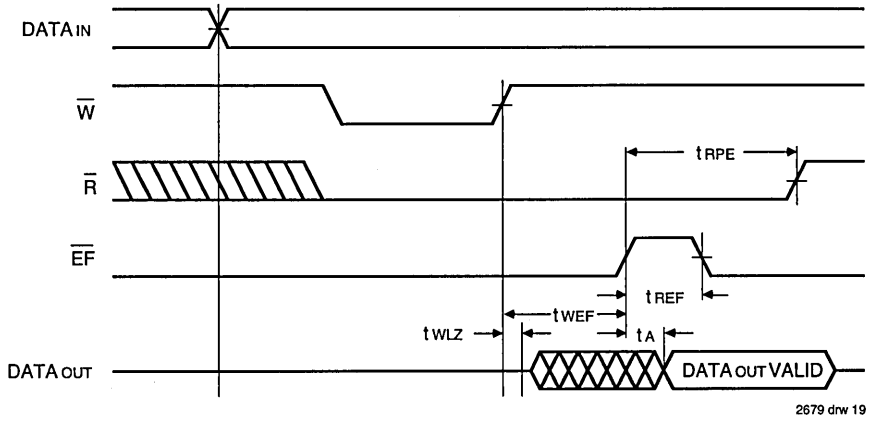


Figure 17. Read Data Flow-Through Mode

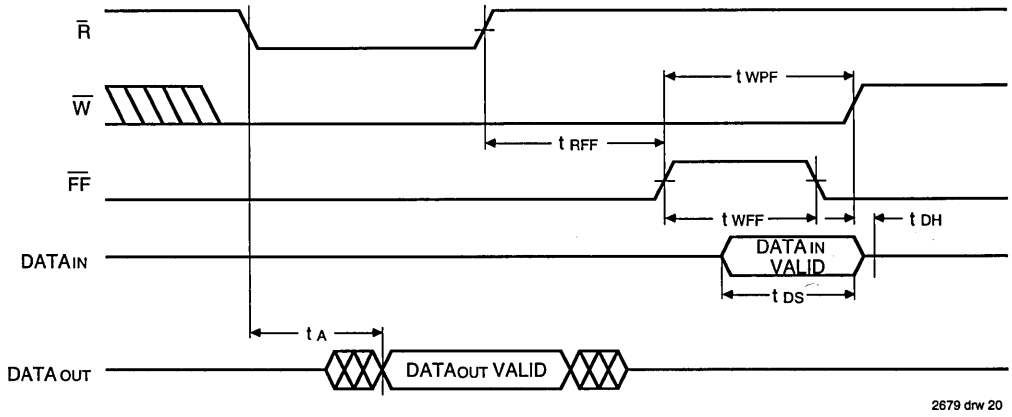
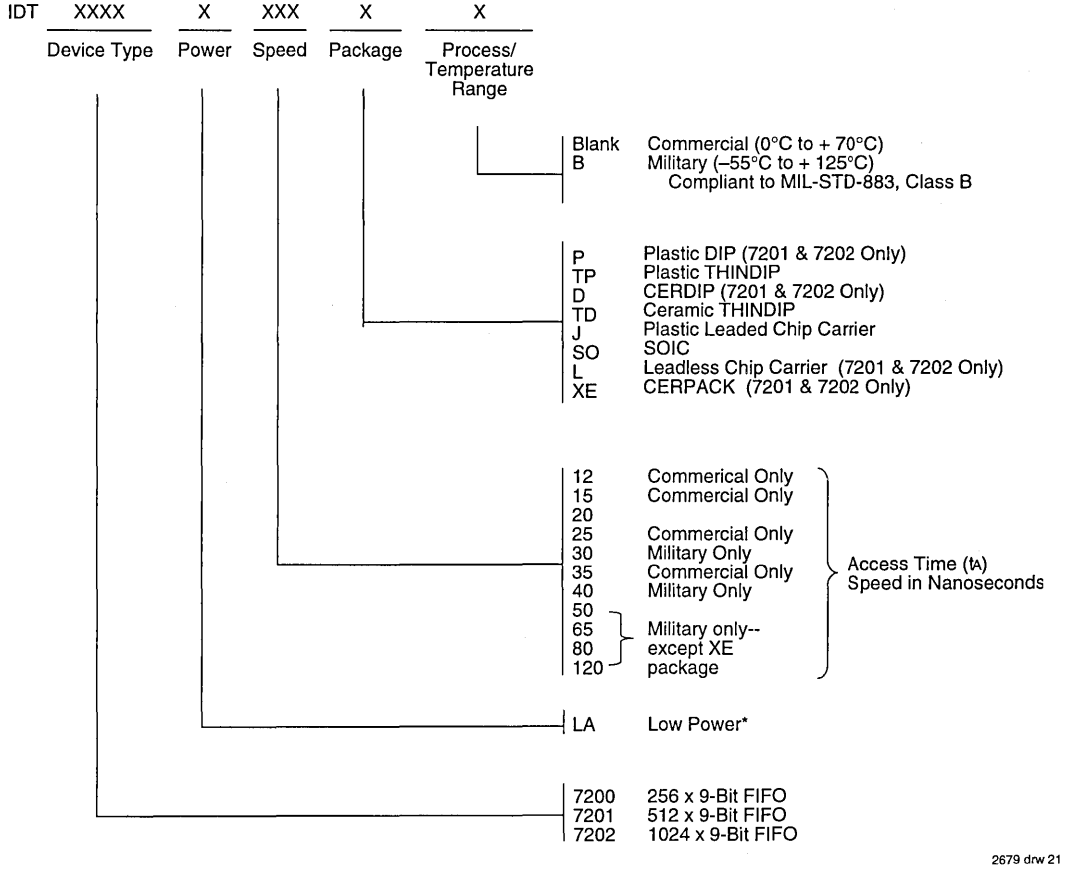


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION



2679 drw 21

* "A" to be included for 7201 and 7202 ordering part number.

5

Integrated Device Technology, Inc.

CMOS ASYNCHRONOUS FIFO 2048 x 9, 4096 x 9, 8192 x 9 and 16384 x 9

IDT7203
IDT7204
IDT7205
IDT7206

FEATURES:

- First-In/First-Out Dual-Port memory
- 2048 x 9 organization (IDT7203)
- 4096 x 9 organization (IDT7204)
- 8192 x 9 organization (IDT7205)
- 16384 x 9 organization (IDT7206)
- High-speed: 12ns access time
- Low power consumption
  - — Active: 770mW (max.)
  - — Power-down: 44mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable in both word depth and width
- Pin and functionally compatible with IDT720X family
- Status Flags: Empty, Half-Full, Full
- Retransmit capability
- High-performance CMOS technology
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing for #5962-88669 (IDT7203), 5962-89567 (IDT7203), and 5962-89568 (IDT7204) are listed on this function.

DESCRIPTION:

The IDT7203/7204/7205/7206 are dual-port memory buffers with internal pointers that load and empty data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

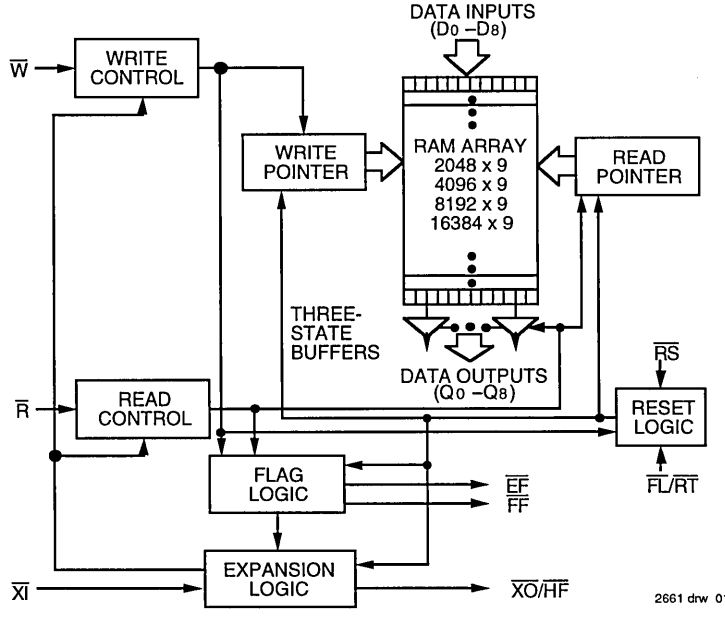
Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins.

The devices 9-bit width provides a bit for a control or parity at the user's option. It also features a Retransmit ($\overline{RT}$) capability that allows the read pointer to be reset to its initial position when $\overline{RT}$ is pulsed LOW. A Half-Full Flag is available in the single device and width expansion modes.

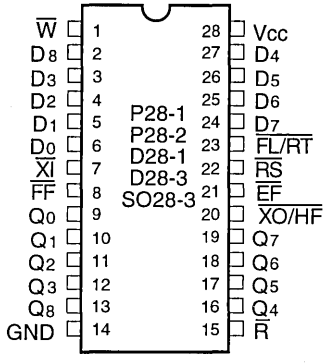
The IDT7203/7204/7205/7206 are fabricated using IDT's high-speed CMOS technology. They are designed for applications requiring asynchronous and simultaneous read/writes in multiprocessing, rate buffering, and other applications.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

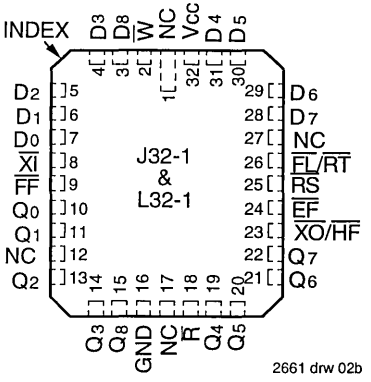


PIN CONFIGURATIONS



2661 drw 02a

DIP
TOP VIEW



2661 drw 02b

PLCC/LCC
TOP VIEW

NOTES:
1. The THINDIPs P28-2 and D28-3 are only available for the 7203/7204/7205.
2. The small outline package SO28-3 is only available for the 7204.
3. Consult factory for CERPACK pinout.

5

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to + 7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	° C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	° C
TSTG	Storage Temperature	–55 to + 125	–65 to +155	° C
IOUT	DC Output Current	50	50	mA

NOTE: 2661 tbl 01
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIH(1)	Input High Voltage Military	2.2	—	—	V
VIL(1)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTE: 2661 tbl 02
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS FOR THE 7203 AND 7204

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

		IDT7203/7204 Commercial t_A = 12, 15, 20, 25, 35, 50 ns			IDT7203/7204 Military(1) t_A = 20, 30, 40, 50, 65, 80, 120 ns			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LI}(2)	Input Leakage Current (Any Input)	−1	—	1	−1	—	1	µA
I_{LO}(3)	Output Leakage Current	−10	—	10	−10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = −2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}(4)	Active Power Supply Current	—	—	120(5)	—	—	150(5)	mA
I_{CC2}(4)	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL}$/$\overline{RT}$=V_{IH})	—	—	12	—	—	25	mA
$I_{CC3(L)}$(4)	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	2	—	—	4	mA
$I_{CC3(S)}$(4)	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	8	—	—	12	mA

NOTES:
2661 tbl 03

1. Speed grades 65, 80, and 120ns are only available in the ceramic DIP.
2. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
3. R ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
4. Icc measurements are made with outputs open (only capacitive loading).
5. Tested at f = 20MHz.

DC ELECTRICAL CHARACTERISTICS FOR THE 7205 AND 7206

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V±10%, T_A = −55°C to +125°C)

		IDT7205/7206 Commercial t_A = 15, 20, 25, 35, 50 ns			IDT7205/7206 Military t_A = 20, 30, 50 ns			
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**	**Unit**
I_{LI}(1)	Input Leakage Current (Any Input)	−1	—	1	−1	—	1	µA
I_{LO}(2)	Output Leakage Current	−10	—	10	−10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = −2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	—	120(4)	—	—	150(4)	mA
I_{CC2}(3)	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL}$/$\overline{RT}$=V_{IH})	—	—	12	—	—	25	mA
$I_{CC3(L)}$(3)	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	8	—	—	12	mA

NOTES:
2661 tbl 04

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. R ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open (only capacitive loading).
4. Tested at f = 20MHz.

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = −55°C to +125°C)

		Commercial				Com'l & Mil.		Com'l		Military		Com'l		
		7203S/L12 7204S/L12		7203S/L15 7204S/L15 7205L15 7206L15		7203S/L20 7204S/L20 7205L20 7206L20		7203S/L25 7204S/L25 7205L25 7206L25		7203S/L30 7204S/L30 7205L30 7206L30		7203S/L35 7204S/L35 7205L35 7206L35		
Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_S	Shift Frequency	—	50	—	40	—	33.3	—	28.5	—	25	—	22.2	MHz
t_{RC}	Read Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_A	Access Time	—	12	—	15	—	20	—	25	—	30	—	35	ns
t_{RR}	Read Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{RPW}	Read Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RLZ}	Read LOW to Data Bus LOW[3]	3	—	5	—	5	—	5	—	5	—	5	—	ns
t_{WLZ}	Write HIGH to Data Bus Low-Z[3, 4]	3	—	5	—	5	—	5	—	5	—	10	—	ns
t_{DV}	Data Valid from Read HIGH	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read HIGH to Data Bus High-Z[3]	—	12	—	15	—	15	—	18	—	20	—	20	ns
t_{WC}	Write Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_{WPW}	Write Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	9	—	11	—	12	—	15	—	18	—	18	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_{RS}	Reset Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RSS}	Reset Set-up Time[3]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RTR}	Reset Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{RTC}	Retransmit Cycle Time	20	—	25	—	30	—	35	—	40	—	45	—	ns
t_{RT}	Retransmit Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RTS}	Retransmit Set-up Time[3]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{RSR}	Retransmit Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to $\overline{EF}$ LOW	—	12	—	25	—	30	—	35	—	40	—	45	ns
t_{HFH}, t_{FFH}	Reset to $\overline{HF}$ and $\overline{FF}$ HIGH	—	17	—	25	—	30	—	35	—	40	—	45	ns
t_{RTF}	Retransmit LOW to Flags Valid	—	20	—	25	—	30	—	35	—	40	—	45	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW	—	12	—	15	—	20	—	25	—	30	—	30	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH	—	14	—	15	—	20	—	25	—	30	—	30	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ HIGH	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH	—	12	—	15	—	20	—	25	—	30	—	30	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW	—	14	—	15	—	20	—	25	—	30	—	30	ns
t_{WHF}	Write LOW to $\overline{HF}$ Flag LOW	—	17	—	25	—	30	—	35	—	40	—	45	ns
t_{RHF}	Read HIGH to $\overline{HF}$ Flag HIGH	—	17	—	25	—	30	—	35	—	40	—	45	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ HIGH	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{XOL}	Read/Write LOW to $\overline{XO}$ LOW	—	12	—	15	—	20	—	25	—	30	—	35	ns
t_{XOH}	Read/Write HIGH to $\overline{XO}$ HIGH	—	12	—	15	—	20	—	25	—	30	—	35	ns
t_{XI}	$\overline{XI}$ Pulse Width[2]	12	—	15	—	20	—	25	—	30	—	35	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	8	—	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	8	—	10	—	10	—	10	—	10	—	15	—	ns

NOTES:
1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

2661 tbl 05

5

AC ELECTRICAL CHARACTERISTICS[1] (Continued)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Military		Com'l & Mil.		Military[2]						
		7203S/L40 7204S/L40		7203S/L50 7204S/L50 7205L50 7206L50		7203S/L65 7204S/L65		7203S/L80 7204S/L80		7203S/L120 7204S/L120		
Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_S	Shift Frequency	—	20	—	15	—	12.5	—	10	—	7	MHz
t_{RC}	Read Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_A	Access Time	—	40	—	50	—	65	—	80	—	120	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{RPW}	Read Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RLZ}	Read LOW to Data Bus LOW[4]	5	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}	Write HIGH to Data Bus Low-Z[4, 5]	10	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read HIGH	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}	Read HIGH to Data Bus High-Z[4]	—	25	—	30	—	30	—	30	—	35	ns
t_{WC}	Write Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{WPW}	Write Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Set-up Time	20	—	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	5	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{RS}	Reset Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RSS}	Reset Set-up Time[4]	40	—	50	—	65	—	80	—	120	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{RTC}	Retransmit Cycle Time	50	—	65	—	80	—	100	—	140	—	ns
t_{RT}	Retransmit Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{RTS}	Retransmit Set-up Time[4]	40	—	50	—	65	—	80	—	120	—	ns
t_{RSR}	Retransmit Recovery Time	10	—	15	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to $\overline{EF}$ LOW	—	50	—	65	—	80	—	100	—	140	ns
t_{HFH}, t_{FFH}	Reset to $\overline{HF}$ and $\overline{FF}$ HIGH	—	50	—	65	—	80	—	100	—	140	ns
t_{RTF}	Retransmit LOW to Flags Valid	—	50	—	65	—	80	—	100	—	140	ns
t_{REF}	Read LOW to $\overline{EF}$ Flag LOW	—	35	—	45	—	60	—	60	—	60	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH	—	35	—	45	—	60	—	60	—	60	ns
t_{RPE}	Read Pulse Width after $\overline{EF}$ HIGH	40	—	50	—	65	—	80	—	120	—	ns
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH	—	35	—	45	—	60	—	60	—	60	ns
t_{WFF}	Write LOW to $\overline{FF}$ LOW	—	35	—	45	—	60	—	60	—	60	ns
t_{WHF}	Write LOW to $\overline{HF}$ LOW	—	50	—	65	—	80	—	100	—	140	ns
t_{RHF}	Read HIGH to $\overline{HF}$ HIGH	—	50	—	65	—	80	—	100	—	140	ns
t_{WPF}	Write Pulse Width after $\overline{FF}$ HIGH	40	—	50	—	65	—	80	—	120	—	ns
t_{XOL}	Read/Write LOW to $\overline{XO}$ LOW	—	40	—	50	—	65	—	80	—	120	ns
t_{XOH}	Read/Write HIGH to $\overline{XO}$ HIGH	—	40	—	50	—	65	—	80	—	120	ns
t_{XI}	$\overline{XI}$ Pulse Width[3]	40	—	50	—	65	—	80	—	120	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	15	—	15	—	ns

NOTES:

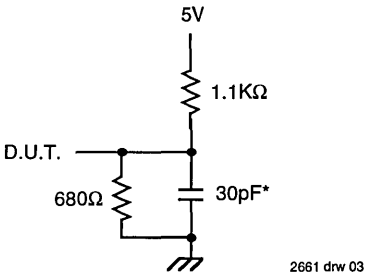
2661 tbl 06

1. Timings referenced as in AC Test Conditions.
2. Speed grades 65, 80, and 120ns are only available in the ceramic DIP.
3. Pulse widths less than minimum are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2661 tbl 07



OR EQUIVALENT CIRCUIT

Figure 1. Output Load

*Includes jig and scope capacitances.

CAPACITANCE[1] (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

2661 tbl 08

NOTES:
1. This parameter is sampled and not 100% tested.
2. With output deselected.

SIGNAL DESCRIPTIONS

Inputs:

DATA IN (D_0–D_8) — Data inputs for 9-bit wide data.

Controls:

RESET ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the HIGH state during the window shown in Figure 2 (i.e. t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$.**

WRITE ENABLE ($\overline{W}$) — A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered-to, with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW, and will remain set until the difference between the write pointer and read pointer is less-than or equal to one-half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW on the falling edge of the last write signal, which inhibits further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after t_{RFF}, allowing a new valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$) — A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$), provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes HIGH, the Data Outputs (Q_0 through Q_8) will return to a high-impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, allowing the "final" read cycle but inhibiting further read operations, with the data outputs remaining in a high-impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$) — This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first device loaded (see Operating Modes). The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7203/7204/7205/7206 can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. The status of the Flags will change depending on the relative locations of the read and write pointers. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the HIGH state during retransmit. This feature is useful when less than 2048/4096/8192/16384 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode.

EXPANSION IN ($\overline{XI}$) — This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy-Chain Mode.

5

Outputs:

FULL FLAG ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations, when the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 2048/4096/8192/16384 writes.

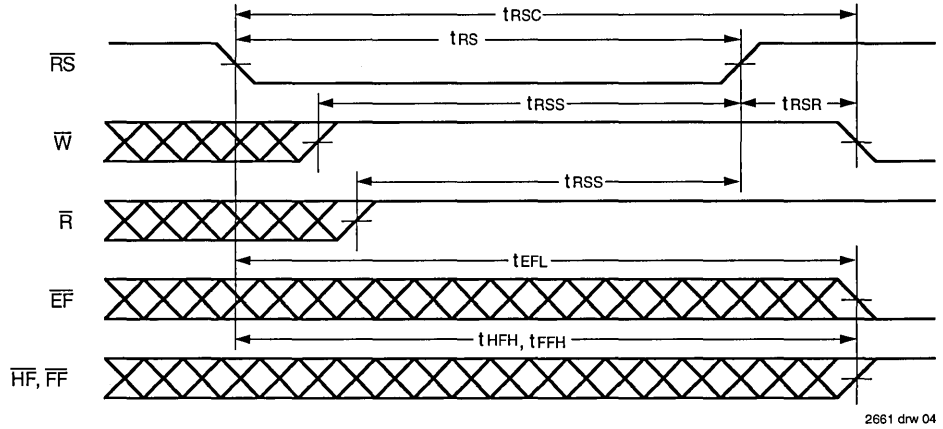
EMPTY FLAG ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$) — This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory. There will be an $\overline{XO}$ pulse when the Write pointer reaches the last location of memory, and an additional $\overline{XO}$ pulse when the Read pointer reaches the last location of memory.

DATA OUTPUTS (Q_0-Q_8) — Q_0-Q_8 are data outputs for 9-bit wide data. These outputs are in a high-impedance condition whenever Read ($\overline{R}$) is in a HIGH state.



NOTE:
1. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

Figure 2. Reset

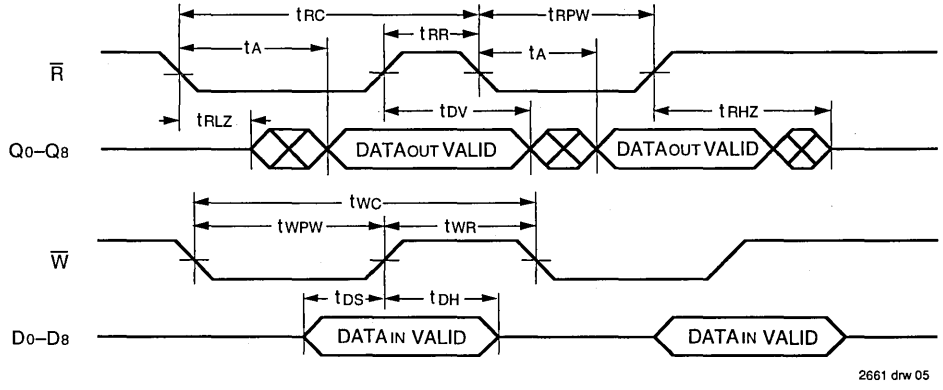


Figure 3. Asynchronous Write and Read Operation

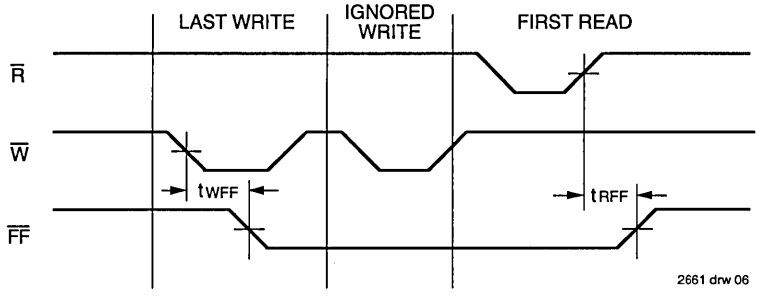


Figure 4. Full FlagTiming From Last Write to First Read

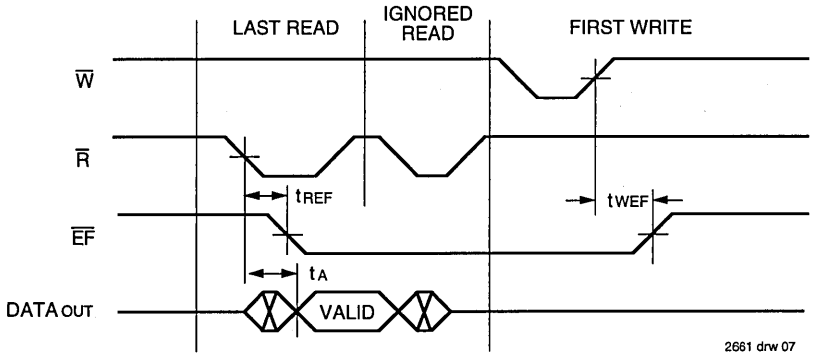
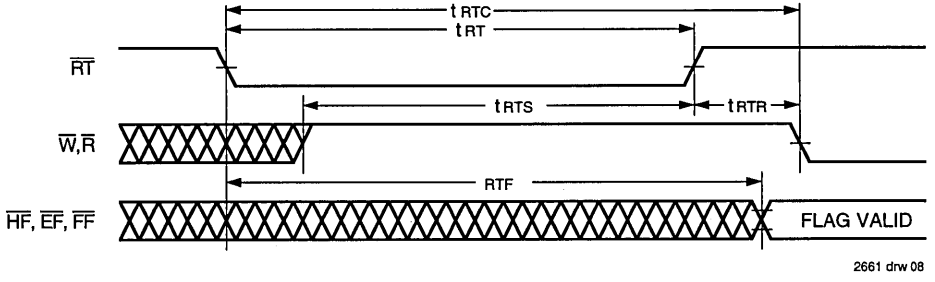


Figure 5. Empty Flag Timing From Last Read to First Write



NOTE:
1. EF, FF and HF may change status during Retransmit, but flags will be valid at tRTC.

Figure 6. Retransmit

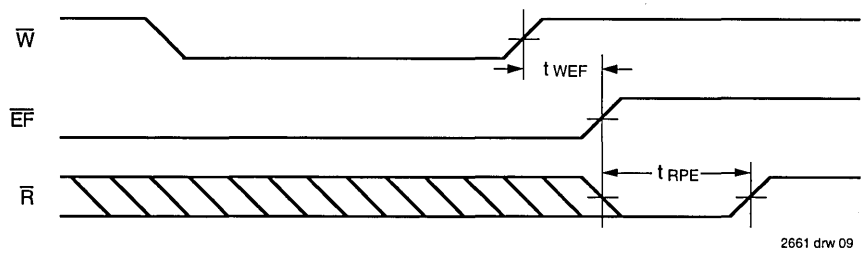


Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse.

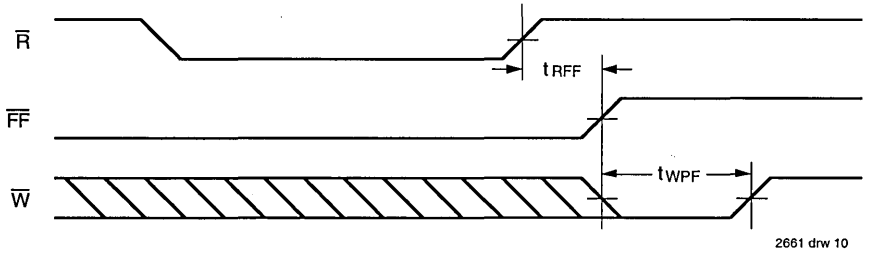


Figure 8. Minimum Timing for an Full Flag Coincident Write Pulse.

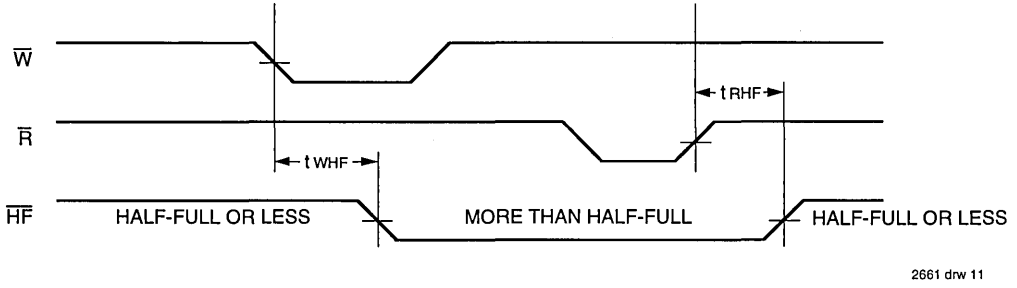


Figure 9. Half-Full Flag Timing

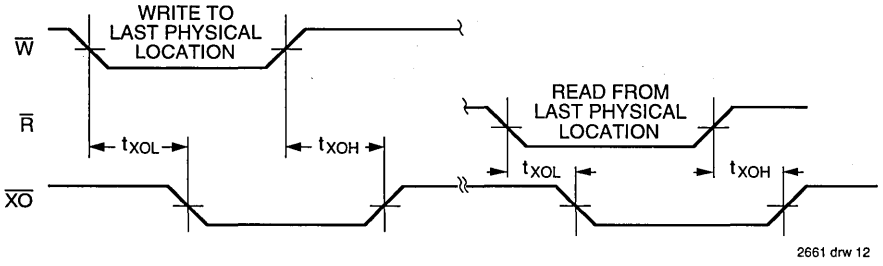


Figure 10. Expansion Out

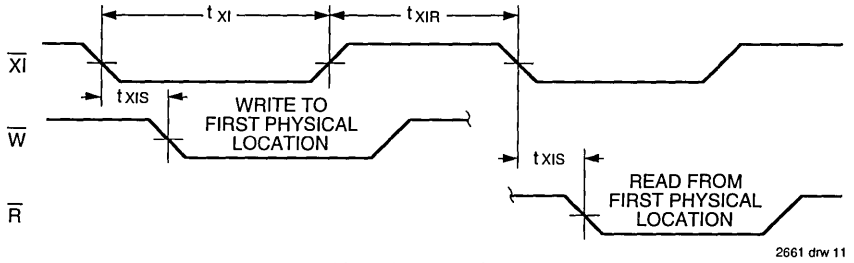


Figure 11. Expansion In

OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

Single Device Mode

A single IDT7203/7204/7205/7206 may be used when the application requirements are for 2048/4096/8192/16384 words or less. The IDT7203/7204/7205/7206 is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

Depth Expansion

The IDT7203/7204/7205/7206 can easily be adapted to applications when the requirements are for greater than 2048/4096/8192/16384 words. Figure 14 demonstrates Depth Expansion using three IDT7203/7204/7205/7206s. Any depth can be attained by adding additional IDT7203/7204/7205/7206s. The IDT7203/7204/7205/7206 operates in the Depth Expansion mode when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

USAGE MODES:

Width Expansion

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7203/7204/7205/7206s. Any word width can be attained by adding additional IDT7203/7204/7205/7206s (Figure 13).

Bidirectional Operation

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7203/7204/7205/7206s as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

Compound Expansion

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

5

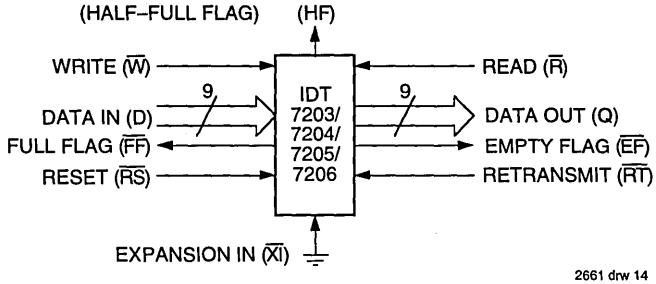
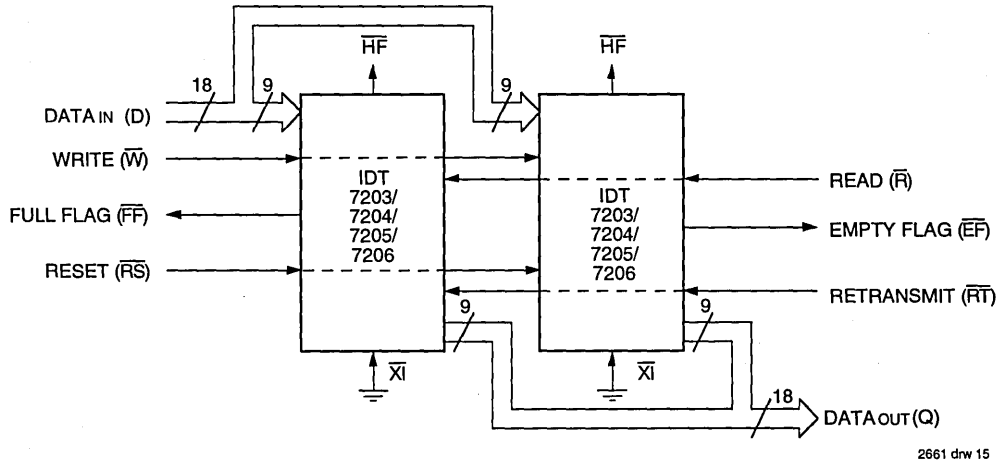


Figure 12. Block Diagram of 2048 x 9/4096 x 9/8192 x 9/16384 x 9 FIFO Used in Single Device Mode



NOTE:
1. Flag detection is accomplished by monitoring the FF, EF and HF signals on either (any) device used in the width expansion configuration. Do not connect any output signals together.

Figure 13. Block Diagram of 2048 x 18/4096 x 18/8192 x 18/16384 x 18 FIFO Memory Used in Width Expansion Mode

TRUTH TABLES

TABLE I – RESET AND RETRANSMIT

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will Increment if flag is HIGH.

2661 tbl 09

TABLE II – RESET AND FIRST LOAD

DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
2. $\overline{RS}$ = Reset Input, $\overline{FL/RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

2661 tbl 10

5

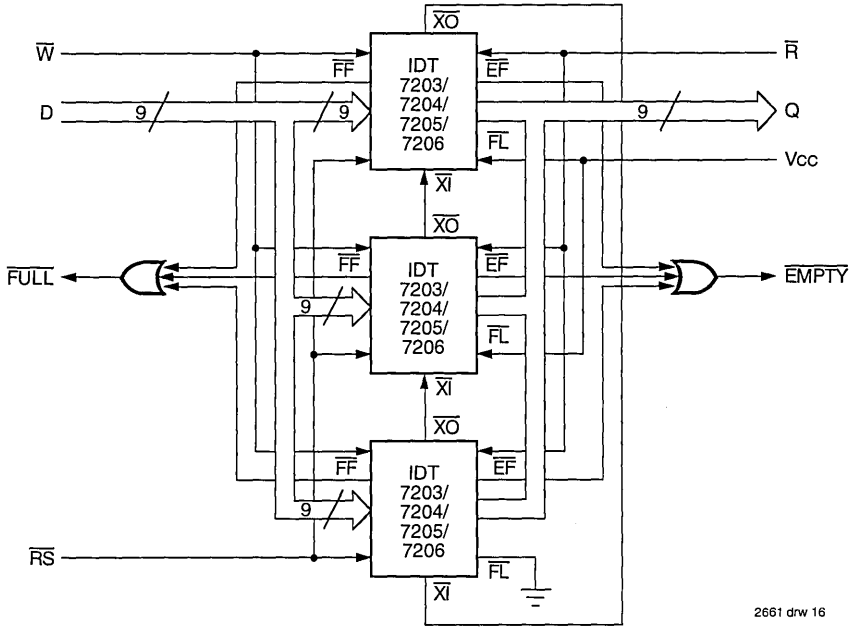
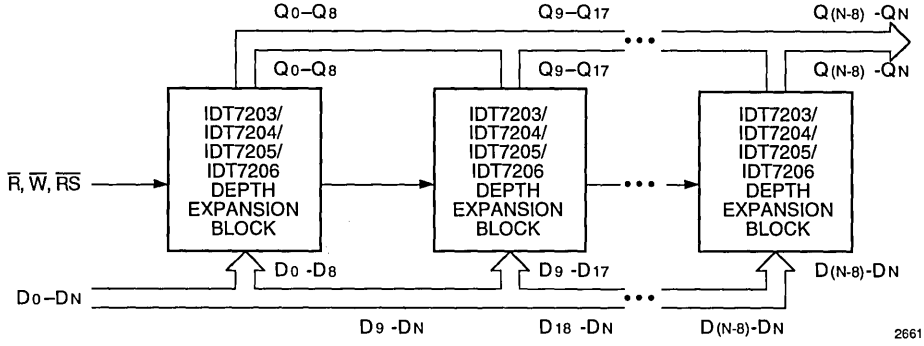


Figure 14. Block Diagram of 6149 x 9/12298 x 9/24596 x 9/49152 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

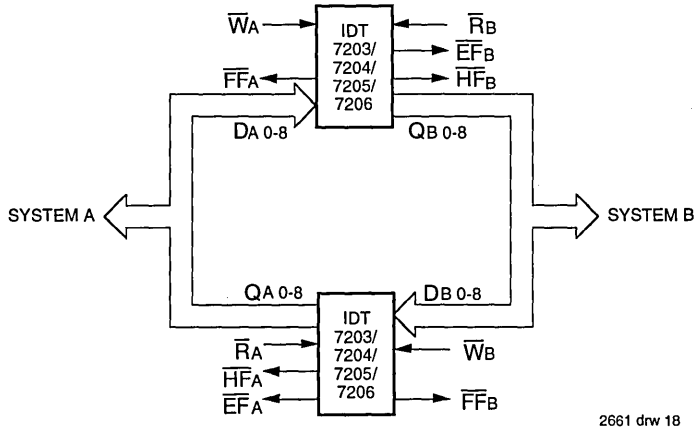


Figure 16. Bidirectional FIFO Operation

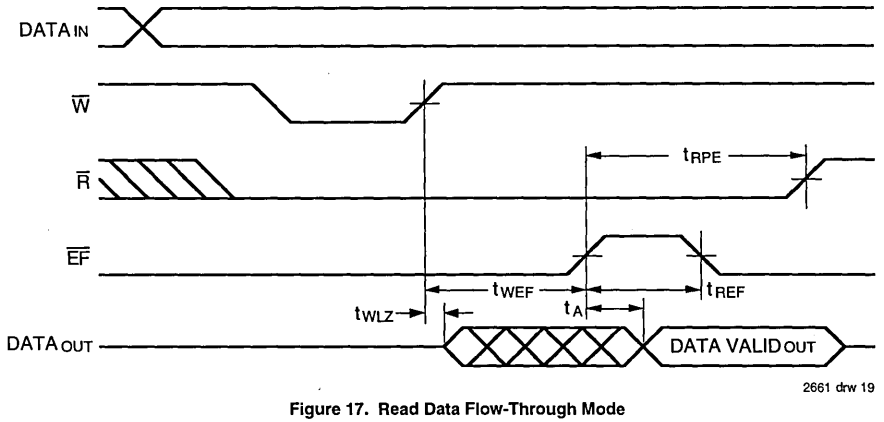


Figure 17. Read Data Flow-Through Mode

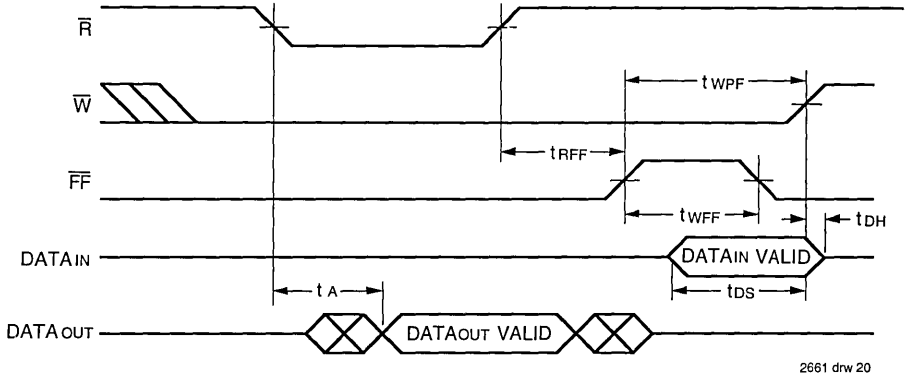
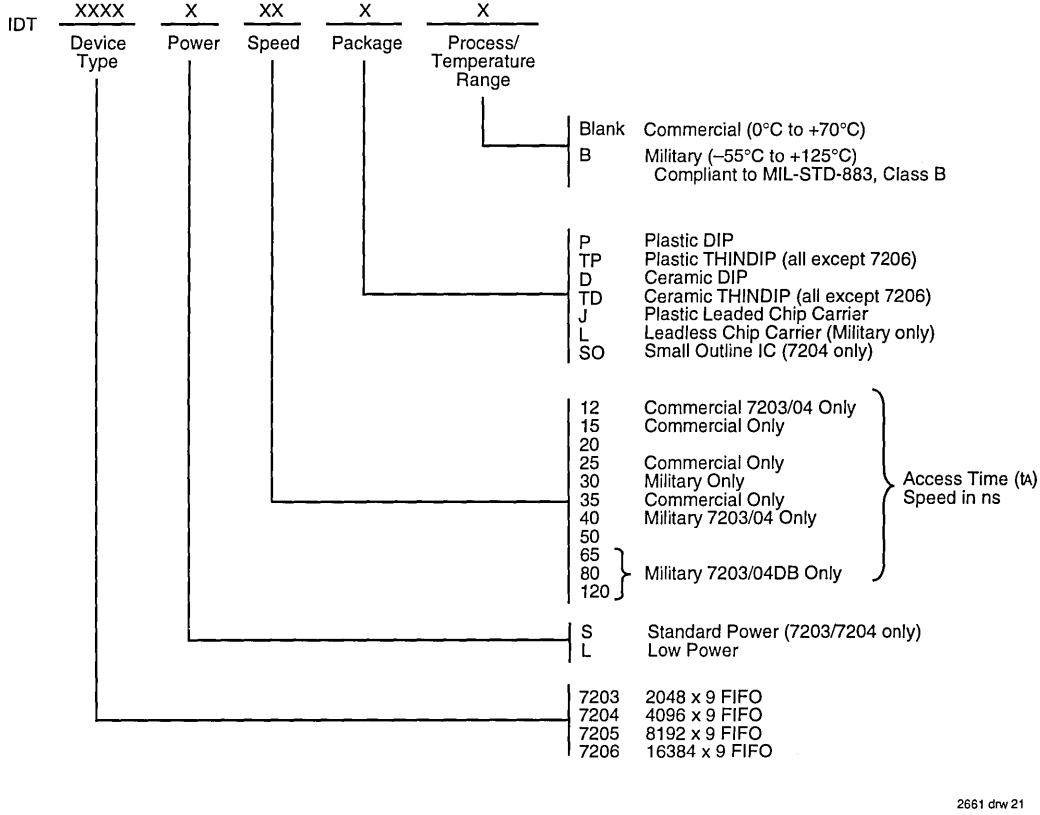


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS ASYNCHRONOUS FIFO 32,768 x 9

PRELIMINARY
IDT7207

FEATURES:

- 32768 x 9 storage capacity
- High-speed: 15ns access time
- Low power consumption
  - — Active: 660mW (max.)
  - — Power-down: 44mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable in both word depth and width
- Pin and functionally compatible with IDT720x family
- Status Flags: Empty, Half-Full, Full
- Retransmit capability
- High-performance CMOS technology
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7207 is a monolithic dual-port memory buffer with internal pointers that load and empty data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

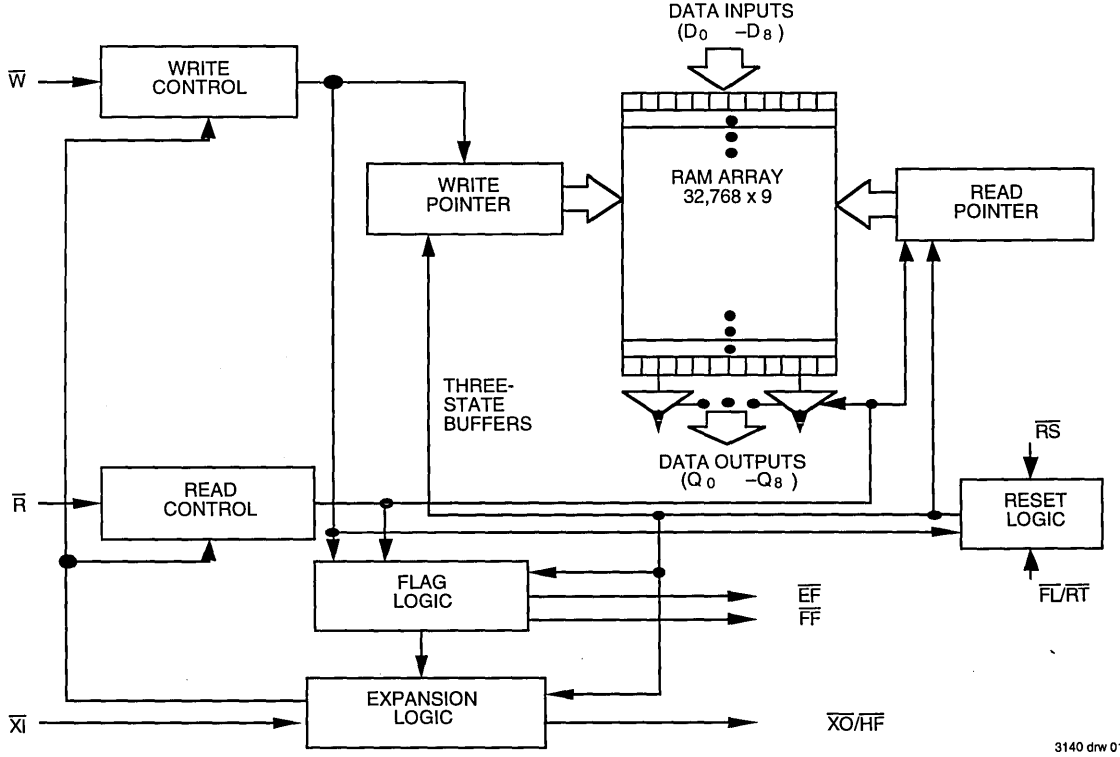
Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins.

The devices 9-bit width provides a bit for a control or parity at the user's option. It also features a Retransmit ($\overline{RT}$) capability that allows the read pointer to be reset to its initial position when $\overline{RT}$ is pulsed LOW. A Half-Full Flag is available in the single device and width expansion modes.

The IDT7207 is fabricated using IDT's high-speed CMOS technology. It is designed for applications requiring asynchronous and simultaneous read/writes in multiprocessing, rate buffering, and other applications.

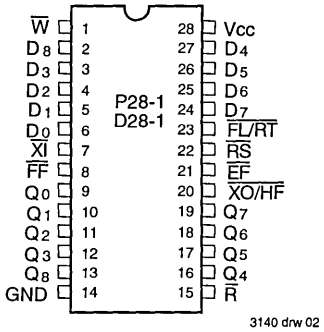
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

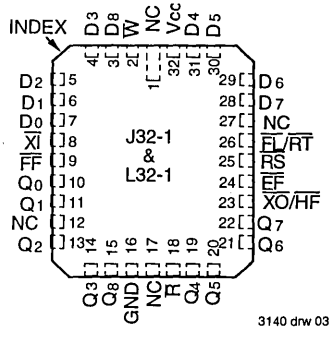


3140 drw 01

PIN CONFIGURATIONS



DIP
TOP VIEW



PLCC/LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to + 7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	° C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	° C
TSTG	Storage Temperature	–55 to + 125	–65 to +155	° C
IOUT	DC Output Current	50	50	mA

NOTE: 3140 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIH(1)	Input High Voltage Military	2.2	—	—	V
VIL(1)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTE: 3140 tbl 02

1. 1.5V undershoots are allowed for 10ns once per cycle.

5

DC ELECTRICAL CHARACTERISTICS FOR THE 7207

(Commercial: VCC = 5.0V±10%, TA = 0°C to +70°C; Military: VCC = 5.0V±10%, TA = –55°C to +125°C)

Symbol	Parameter	IDT7207 Commercial tA = 15, 20, 25, 35, 50 ns			IDT7207 Military tA = 20, 30, 50 ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
ILI(1)	Input Leakage Current (Any Input)	–1	—	1	–1	—	1	µA
ILO(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
VOH	Output Logic "1" Voltage IOH = –2mA	2.4	—	—	2.4	—	—	V
VOL	Output Logic "0" Voltage IOL = 8mA	—	—	0.4	—	—	0.4	V
ICC1(3)	Active Power Supply Current	—	—	120(4)	—	—	150(4)	mA
ICC2(3)	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL/RT}$=VIH)	—	—	12	—	—	25	mA
ICC3(L)(3)	Power Down Current (All Input = VCC - 0.2V)	—	—	8	—	—	12	mA

NOTES: 3140 tbl 04

1. Measurements with 0.4 ≤ VIN ≤ VCC.
2. R ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. Icc measurements are made with outputs open (only capacitive loading).
4. Tested at f = 20MHz.

AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: Vcc = 5V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5V ± 10%, TA = –55°C to +125°C)

		Com'l		Com'l & Mil.		Com'l		Military		Com'l		Com'l & Mil.		
		7207L15		7207L20		7207L25		7207L30		7207L35		7207L50		
Symbol	Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Shift Frequency	—	40	—	33.3	—	28.5	—	25	—	22.2	—	15	MHz
tRC	Read Cycle Time	25	—	30	—	35	—	40	—	45	—	65	—	ns
tA	Access Time	—	15	—	20	—	25	—	30	—	35	—	50	ns
tRR	Read Recovery Time	10	—	10	—	10	—	10	—	10	—	15	—	ns
tRPW	Read Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	50	—	ns
tRLZ	Read LOW to Data Bus LOW[3]	5	—	5	—	5	—	5	—	5	—	10	—	ns
tWLZ	Write HIGH to Data Bus Low-Z[3,4]	5	—	5	—	5	—	5	—	10	—	15	—	ns
tDV	Data Valid from Read HIGH	5	—	5	—	5	—	5	—	5	—	5	—	ns
tRHZ	Read HIGH to Data Bus High-Z[3]	—	15	—	15	—	18	—	20	—	20	—	30	ns
tWC	Write Cycle Time	25	—	30	—	35	—	40	—	45	—	65	—	ns
tWPW	Write Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	50	—	ns
tWR	Write Recovery Time	10	—	10	—	10	—	10	—	10	—	15	—	ns
tDS	Data Set-up Time	11	—	12	—	15	—	18	—	18	—	30	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	5	—	ns
tRSC	Reset Cycle Time	25	—	30	—	35	—	40	—	45	—	65	—	ns
tRS	Reset Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	50	—	ns
tRSS	Reset Set-up Time[3]	15	—	20	—	25	—	30	—	35	—	50	—	ns
tRTR	Reset Recovery Time	10	—	10	—	10	—	10	—	10	—	15	—	ns
tRTC	Retransmit Cycle Time	25	—	30	—	35	—	40	—	45	—	65	—	ns
tRT	Retransmit Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	50	—	ns
tRTS	Retransmit Set-up Time[3]	15	—	20	—	25	—	30	—	35	—	50	—	ns
tRSR	Retransmit Recovery Time	10	—	10	—	10	—	10	—	10	—	15	—	ns
tEFL	Reset to EF LOW	—	25	—	30	—	35	—	40	—	45	—	65	ns
tHFH, tFFH	Reset to HF and FF HIGH	—	25	—	30	—	35	—	40	—	45	—	65	ns
tRTF	Retransmit LOW to Flags Valid	—	25	—	30	—	35	—	40	—	45	—	65	ns
tREF	Read LOW to EF LOW	—	15	—	20	—	25	—	30	—	30	—	45	ns
tRFF	Read HIGH to FF HIGH	—	15	—	20	—	25	—	30	—	30	—	45	ns
tRPE	Read Pulse Width after EF HIGH	15	—	20	—	25	—	30	—	35	—	50	—	ns
tWEF	Write HIGH to EF HIGH	—	15	—	20	—	25	—	30	—	30	—	45	ns
tWFF	Write LOW to FF LOW	—	15	—	20	—	25	—	30	—	30	—	45	ns
tWHF	Write LOW to HF Flag LOW	—	25	—	30	—	35	—	40	—	45	—	65	ns
tRHF	Read HIGH to HF Flag HIGH	—	25	—	30	—	35	—	40	—	45	—	65	ns
tWPF	Write Pulse Width after FF HIGH	15	—	20	—	25	—	30	—	35	—	50	—	ns
tXOL	Read/Write LOW to XO LOW	—	15	—	20	—	25	—	30	—	35	—	50	ns
tXOH	Read/Write HIGH to XO HIGH	—	15	—	20	—	25	—	30	—	35	—	50	ns
tXI	XI Pulse Width[2]	15	—	20	—	25	—	30	—	35	—	50	—	ns
tXIR	XI Recovery Time	10	—	10	—	10	—	10	—	10	—	10	—	ns
tXIS	XI Set-up Time	10	—	10	—	10	—	10	—	15	—	15	—	ns

NOTES:

3140 tbl 05

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

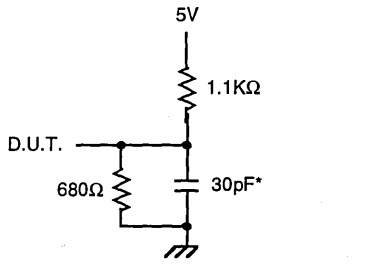
3140 tbl 07

CAPACITANCE[1] (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES:
1. This parameter is sampled and not 100% tested.
2. With output deselected.

3140 tbl 08



OR EQUIVALENT CIRCUIT 3140 drw 04

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

Inputs:

DATA IN (D_0–D_8) — Data inputs for 9-bit wide data.

Controls:

RESET ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the HIGH state during the window shown in Figure 2 (i.e. t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$.**

WRITE ENABLE ($\overline{W}$) — A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered-to, with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW, and will remain set until the difference between the write pointer and read pointer is less-than or equal to one-half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW on the falling edge of the last write signal, which inhibits further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after t_{RFF}, allowing a new valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$) — A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$), provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes HIGH, the Data Outputs (Q_0 through Q_8) will return to a high-impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, allowing the "final" read cycle but inhibiting further read operations, with the data outputs remaining in a high-impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$) — This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first device loaded (see Operating Modes). The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7207 can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. The status of the Flags will change depending on the relative locations of the read and write pointers. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the HIGH state during retransmit. This feature is useful when less than 32,768 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode.

EXPANSION IN ($\overline{XI}$) — This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy-Chain Mode.

5

Outputs:

FULL FLAG ($\overline{FF}$) — The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations, when the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 32,768 writes.

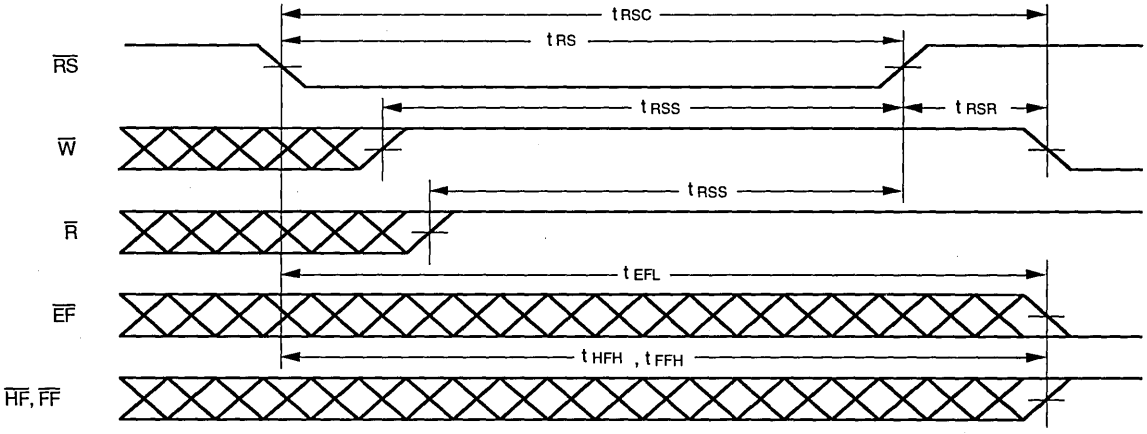
EMPTY FLAG ($\overline{EF}$) — The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$) — This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory. There will be an $\overline{XO}$ pulse when the Write pointer reaches the last location of memory, and an additional $\overline{XO}$ pulse when the Read pointer reaches the last location of memory.

DATA OUTPUTS (Q_0-Q_8) — Q_0-Q_8 are data outputs for 9-bit wide data. These outputs are in a high-impedance condition whenever Read ($\overline{R}$) is in a HIGH state.



NOTE:
1. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

Figure 2. Reset

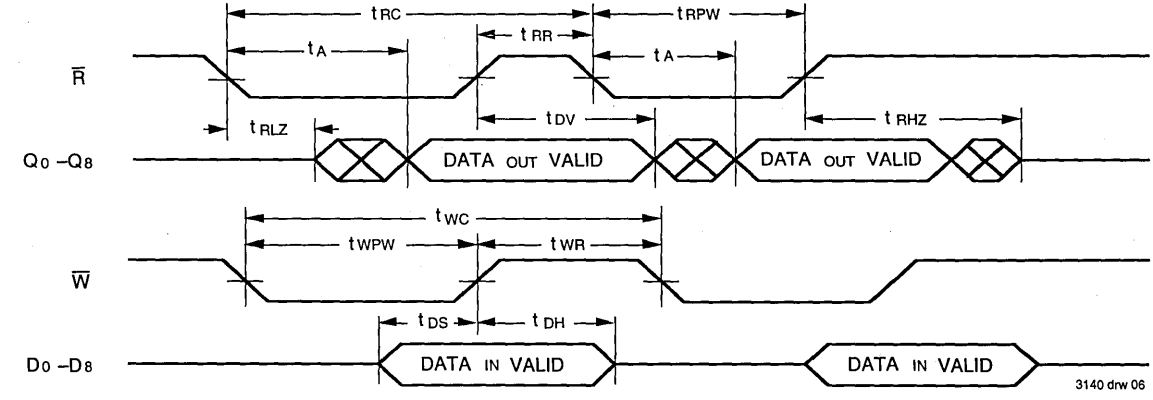


Figure 3. Asynchronous Write and Read Operation

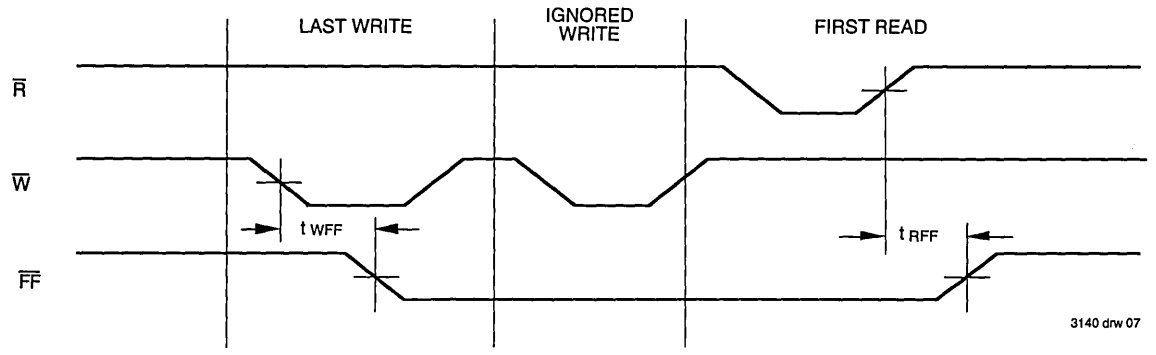


Figure 4. Full FlagTiming From Last Write to First Read

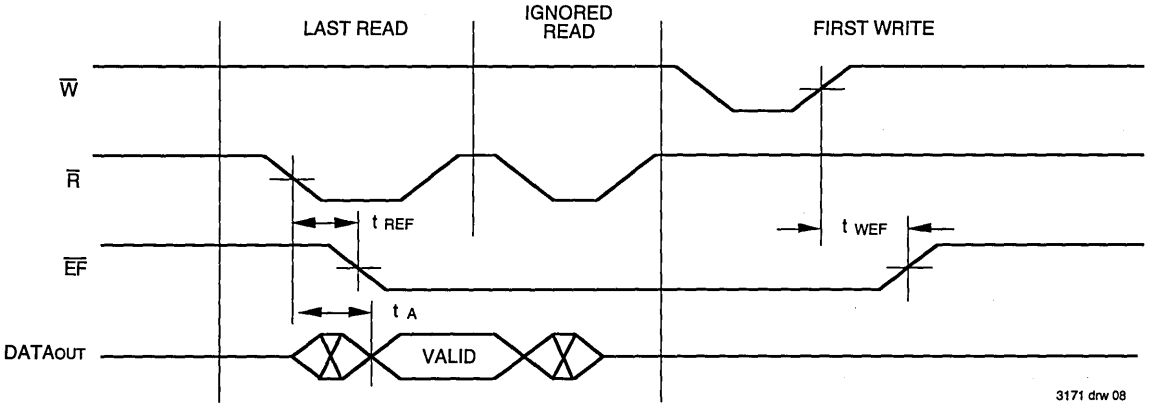
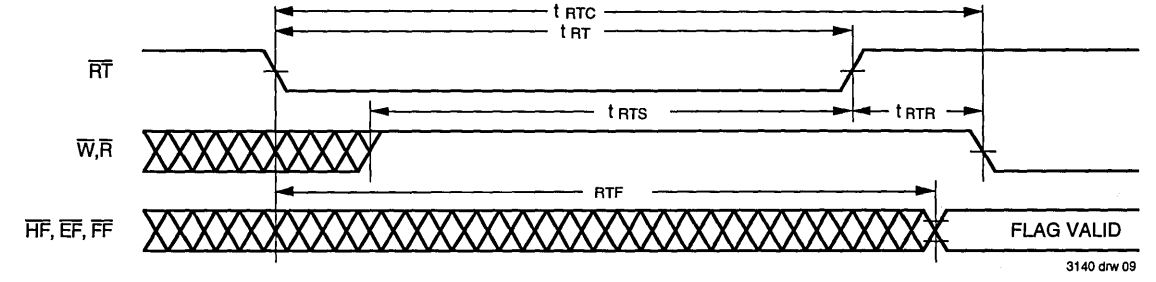


Figure 5. Empty Flag Timing From Last Read to First Write



NOTE:
1. $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

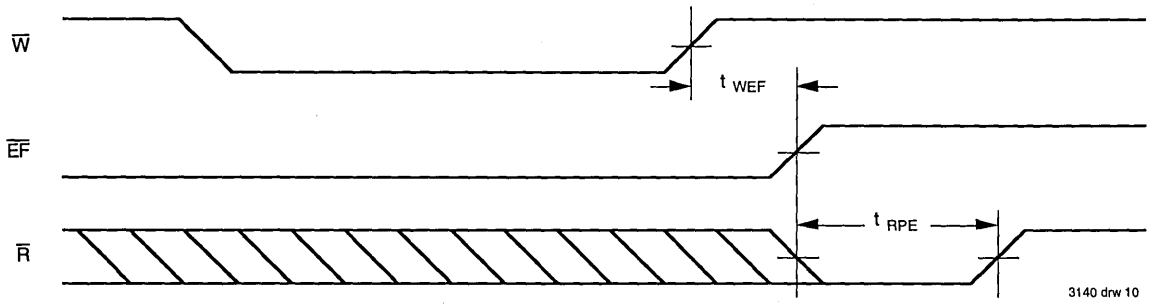


Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse.

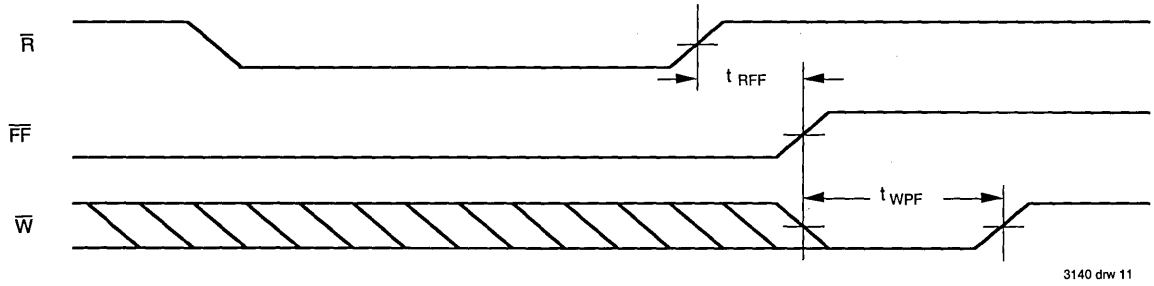


Figure 8. Minimum Timing for an Full Flag Coincident Write Pulse.

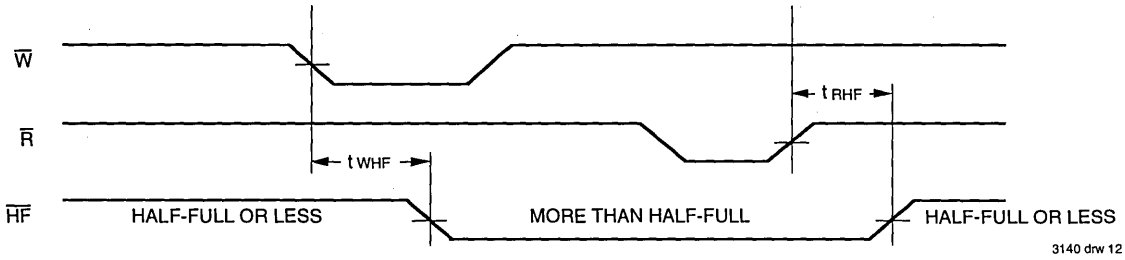


Figure 9. Half-Full Flag Timing

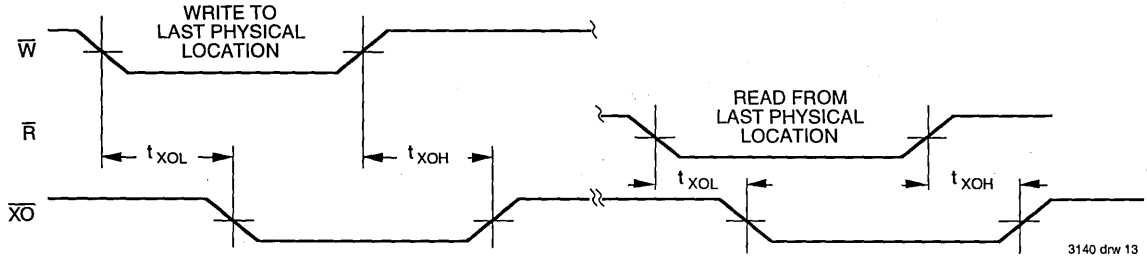


Figure 10. Expansion Out

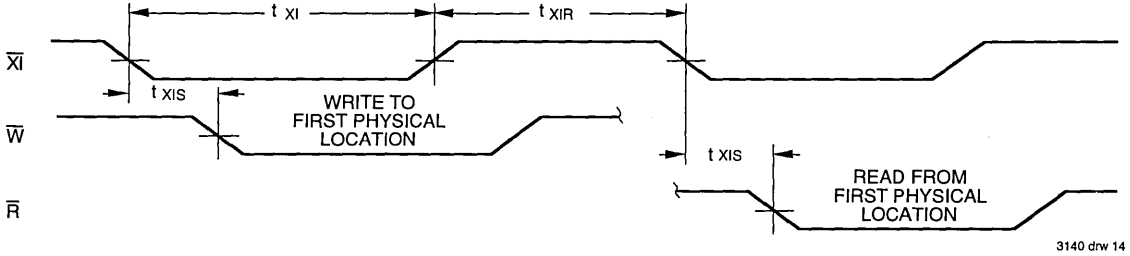


Figure 11. Expansion In

OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

Single Device Mode

A single IDT7207 may be used when the application requirements are for 32,768 words or less. The IDT7207 is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

Depth Expansion

The IDT7207 can easily be adapted to applications when the requirements are for greater than 32,768 words. Figure 14 demonstrates Depth Expansion using three IDT7207s. Any depth can be attained by adding additional IDT7207s. The IDT7207 operates in the Depth Expansion mode when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

USAGE MODES:

Width Expansion

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7207s. Any word width can be attained by adding additional IDT7207s (Figure 13).

Bidirectional Operation

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7207s as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

Compound Expansion

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

5

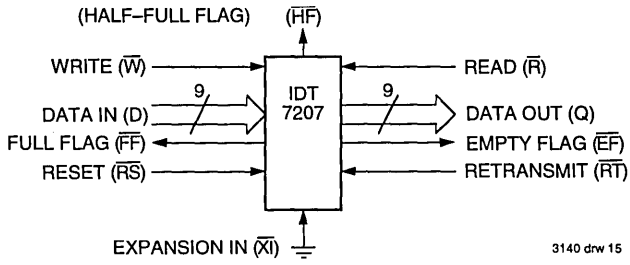
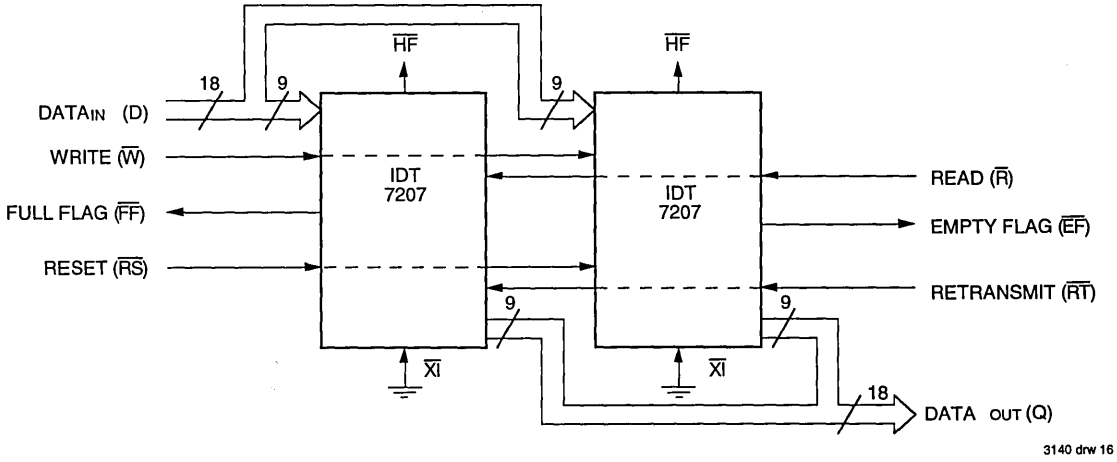


Figure 12. Block Diagram of 32,768 x 9 FIFO Used in Single Device Mode



NOTE:
1. Flag detection is accomplished by monitoring the FF, EF and HF signals on either (any) device used in the width expansion configuration. Do not connect any output signals together.

Figure 13. Block Diagram of 32,768 x 18 FIFO Memory Used in Width Expansion Mode

TRUTH TABLES

TABLE I – RESET AND RETRANSMIT

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will Increment if flag is HIGH.

3140 tbl 09

TABLE II – RESET AND FIRST LOAD

DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
2. $\overline{RS}$ = Reset Input, $\overline{FL/RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

3140 tbl 10

5

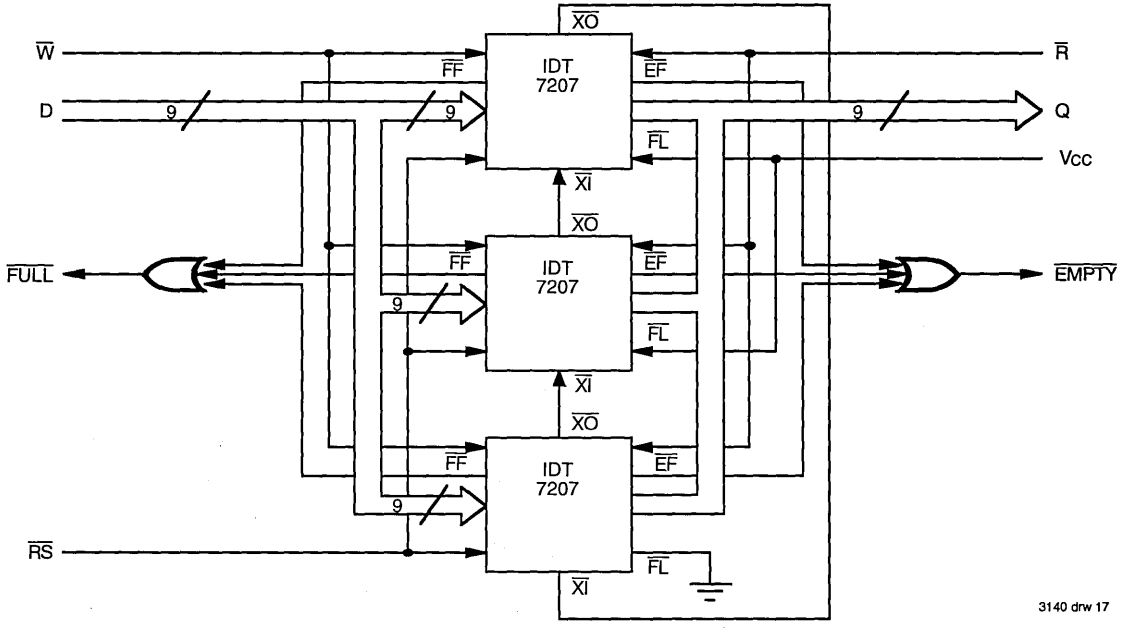
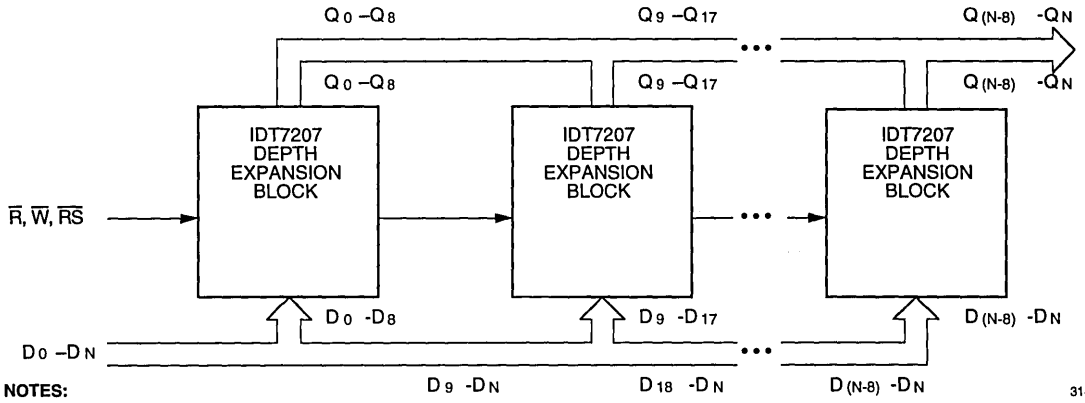


Figure 14. Block Diagram of 98,304 x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

Figure 15. Compound FIFO Expansion

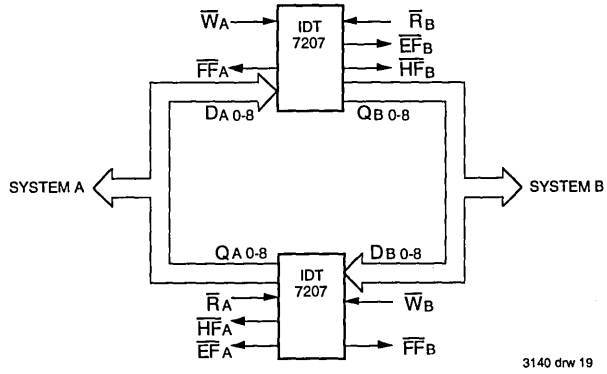


Figure 16. Bidirectional FIFO Operation

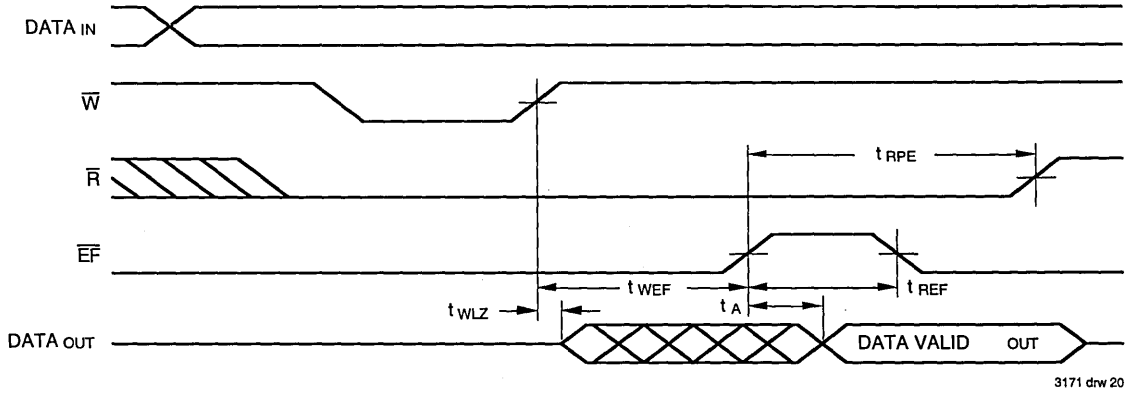


Figure 17. Read Data Flow-Through Mode

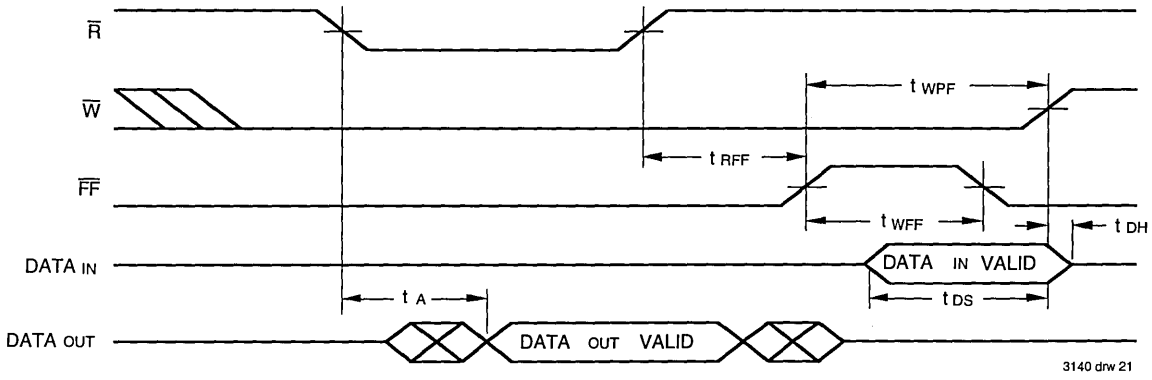
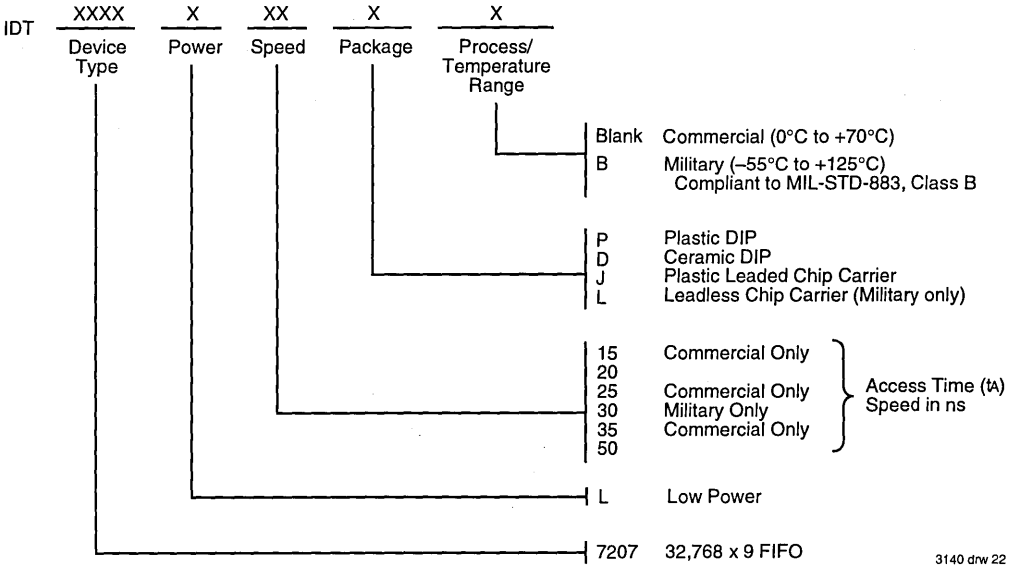


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION



5

Integrated Device Technology, Inc.

3.3 VOLT CMOS ASYNCHRONOUS FIFO 512 x 9, 1024 x 9, 2048 x 9, 4096 X 9

PRELIMINARY
IDT72V01
IDT72V02
IDT72V03
IDT72V04

FEATURES:

- 3.3V family uses 70% less power than the 5 Volt 7201/02/03/04 family
- 512 x 9 organization (72V01)
- 1024 x 9 organization (72V02)
- 2048 x 9 organization (72V03)
- 4096 X 9 organization (72V04)
- Functionally compatible with 720x family
- 25 ns access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Status Flags: Empty, Half-Full, Full
- Auto-retransmit capability
- Available in 32-pin PLCC and 28-pin SOIC Package (to be determined)

DESCRIPTION:

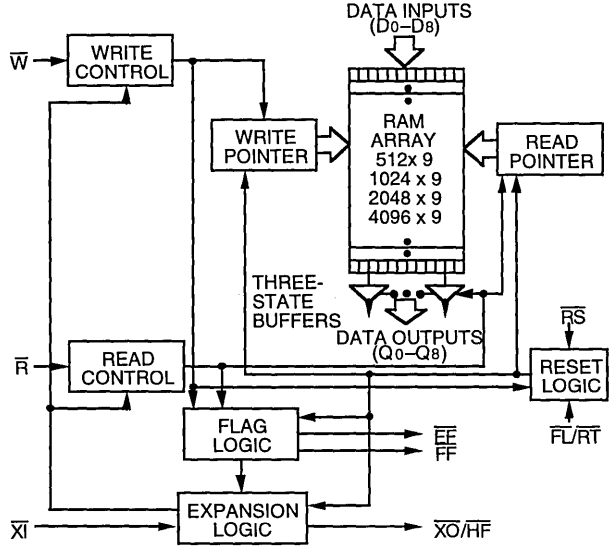
The IDT72V01/72V02/72V03/72V04 are dual-port FIFO memories that operate at a power supply voltage (Vcc) between 3.0V and 3.6V. Their architecture, functional operation and pin assignments are identical to those of the IDT7201/7202/7203/7204. These devices load and empty data on a first-in/first-out basis. They use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins. The devices have a maximum data access time as fast as 25 ns.

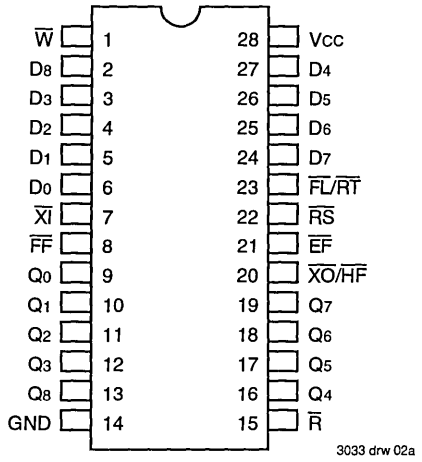
The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. They also feature a Retransmit ($\overline{RT}$) capability that allows for reset of the read pointer to its initial position when $\overline{RT}$ is pulsed low to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

The IDT72V01/72V02/72V03/72V04 is fabricated using IDT's high-speed CMOS technology. It has been designed for those applications requiring asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

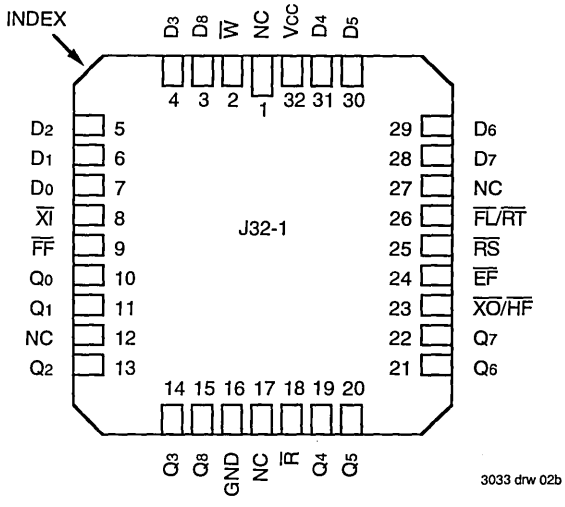
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



SMALL OUTLINE PACKAGE TO BE DETERMINED



PLCC
TOP VIEW

5

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 3033 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

CAPACITANCE (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 3033 tbl 02

1. This parameter is sampled and not 100% tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Rating	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage	2.0	—	Vcc+0.5	V
VIL(2)	Input Low Voltage	—	—	0.8	V

NOTES: 3033 tbl 03

1. VIH = 2.6V for XI input (commercial).
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 3.3 V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT72V01/72V02/ 72V03/72V04 Commercial t_A = 25 ns			IDT72V01/72V02/ 72V03/72V04 Commercial t_A = 35 ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[1]	Input Leakage Current (Any Input)	–1	—	1	–1	—	1	µA
I_{LO}[2]	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}[3,4]	Active Power Supply Current	—	35	50	—	35	50	mA
I_{CC2}[3]	Standby Current ($\overline{R}$=$\overline{W}$=$\overline{RS}$=$\overline{FL}$/$\overline{RT}$=V_{IH})	—	5	8	—	5	8	mA
$I_{CC3(L)}$[3]	Power Down Current (All Input = V_{CC} - 0.2V)	—	—	0.3	—	—	0.3	mA

3033 tbl 04

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. I_{CC} measurements are made with outputs open (only capacitive loading).
4. Tested at f = 20MHz.

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 3.3V±10%, TA = 0°C to +70°C)

		Commercial		Commercial		
		72V01L25/72V02L25 72V03L25/72V04L25		72V01L35/72V02L35 72V03L35/72V04L35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
fs	Shift Frequency	—	28.5	—	22.2	MHz
tRC	Read Cycle Time	35	—	45	—	ns
tA	Access Time	—	25	—	35	ns
tRR	Read Recovery Time	10	—	10	—	ns
tRPW	Read Pulse Width[2]	25	—	35	—	ns
tRLZ	Read Pulse LOW to Data Bus at Low-Z[3]	5	—	5	—	ns
tWLZ	Write Pulse HIGH to Data Bus at Low-Z[3,4]	5	—	10	—	ns
tDV	Data Valid from Read Pulse HIGH	5	—	5	—	ns
tRHZ	Read Pulse HIGH to Data Bus at High-Z[3]	—	18	—	20	ns
tWC	Write Cycle Time	35	—	45	—	ns
tWPW	Write Pulse Width[2]	25	—	35	—	ns
tWR	Write Recovery Time	10	—	10	—	ns
tDS	Data Set-up Time	15	—	18	—	ns
tDH	Data Hold Time	0	—	0	—	ns
tRSC	Reset Cycle Time	35	—	45	—	ns
tRS	Reset Pulse Width[2]	25	—	35	—	ns
tRSS	Reset Set-up Time[3]	25	—	35	—	ns
tRSR	Reset Recovery Time	10	—	10	—	ns
tRTC	Retransmit Cycle Time	35	—	45	—	ns
tRT	Retransmit Pulse Width[2]	25	—	35	—	ns
tRTS	Retransmit Set-up Time[3]	25	—	35	—	ns
tRTR	Retransmit Recovery Time	10	—	10	—	ns
tEFL	Reset to Empty Flag LOW	—	35	—	45	ns
tHFH,FFH	Reset to Half-Full and Full Flag HIGH	—	35	—	45	ns
tRTF	Retransmit LOW to Flags Valid	—	35	—	45	ns
tREF	Read LOW to Empty Flag LOW	—	25	—	30	ns
tRFF	Read HIGH to Full Flag HIGH	—	25	—	30	ns
tRPE	Read Pulse Width after $\overline{EF}$ HIGH	25	—	35	—	ns
tWEF	Write HIGH to Empty Flag HIGH	—	25	—	30	ns
tWFF	Write LOW to Full Flag LOW	—	25	—	30	ns
tWHF	Write LOW to Half-Full Flag LOW	—	35	—	45	ns
tRHF	Read HIGH to Half-Full Flag HIGH	—	35	—	45	ns
tWPF	Write Pulse Width after $\overline{FF}$ HIGH	25	—	35	—	ns
tXOL	Read/Write to $\overline{XO}$ LOW	—	25	—	35	ns
tXOH	Read/Write to $\overline{XO}$ HIGH	—	25	—	35	ns
tXI	$\overline{XI}$ Pulse Width[2]	25	—	35	—	ns
tXIR	$\overline{XI}$ Recovery Time	10	—	10	—	ns
tXIS	$\overline{XI}$ Set-up Time	10	—	10	—	ns

NOTES:

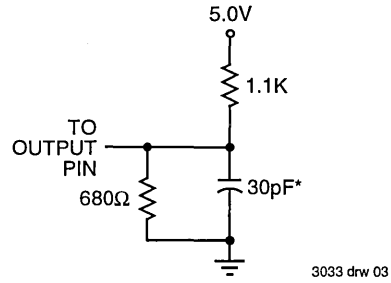
3033 tbl 05

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

3033 tbl 06



or equivalent circuit

Figure 1. Output Load

* Includes scope and jig capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN ($D_0 - D_8$)

Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the HIGH state during the window shown in Figure 2, (i.e., t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$. Half-Full Flag ($\overline{HF}$) will be reset to HIGH after Reset ($\overline{RS}$).**

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after t_{RFF}, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$) provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes HIGH, the Data Outputs ($Q_0 - Q_8$) will return to a high impedance condition until the next Read operation. When all data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, allowing the "final" read cycle but inhibiting further read operations with the data outputs remaining in a HIGH impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes in $\overline{R}$ will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the restransmit input. The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT72V01/72V02/72V03/72V04 can be made to retransmit data when the Retransmit Enable control ($\overline{RT}$) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be in the HIGH state during retransmit. This feature is useful when less than 512/1024/2048/4096 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag ($\overline{HF}$), depending on the relative locations of the read and write pointers.

EXPANSION IN ($\overline{XI}$)

This input is a dual-purpose pin. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset ($\overline{RS}$), the Full-Flag ($\overline{FF}$) will go LOW after 512/1024/2048/4096 writes to the IDT72V01/72V02/72V03/72V04.

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG ($\overline{XO}/\overline{HF}$)

This is a dual-purpose output. In the single device mode, when Expansion In ($\overline{XI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by using rising edge of the read operation.

In the Depth Expansion Mode, Expansion In ($\overline{XI}$) is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

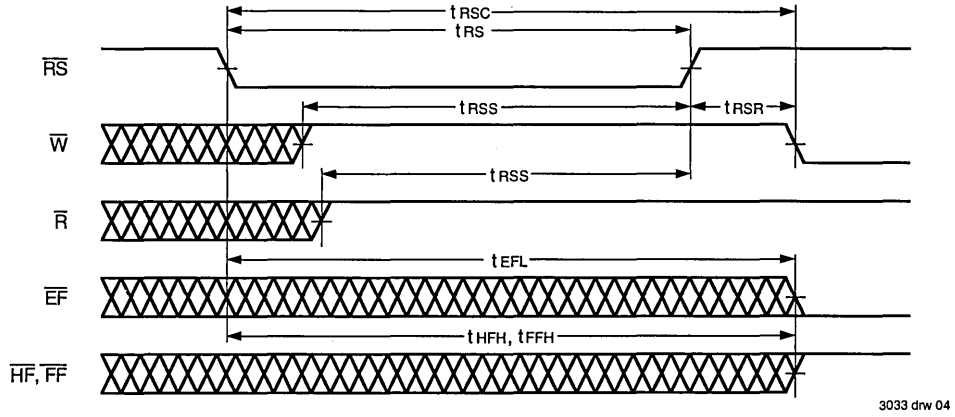


Figure 2. Reset

NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

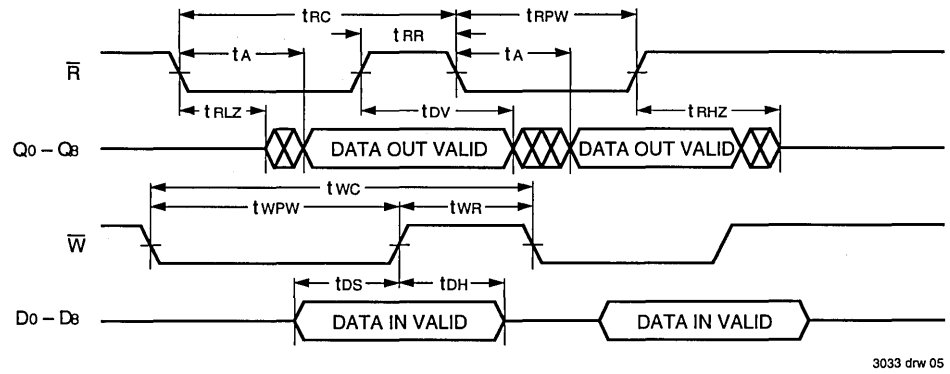


Figure 3. Asynchronous Write and Read Operation

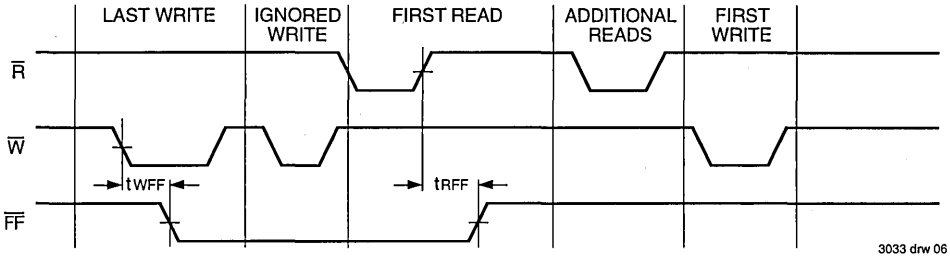


Figure 4. Full Flag From Last Write to First Read

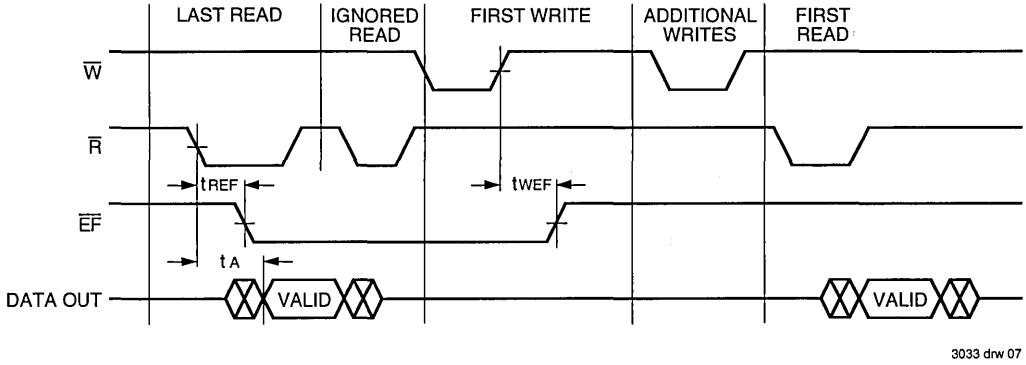


Figure 5. Empty Flag From Last Read to First Write

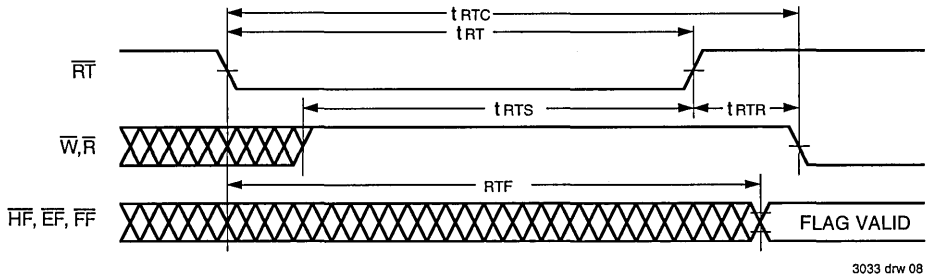


Figure 6. Retransmit

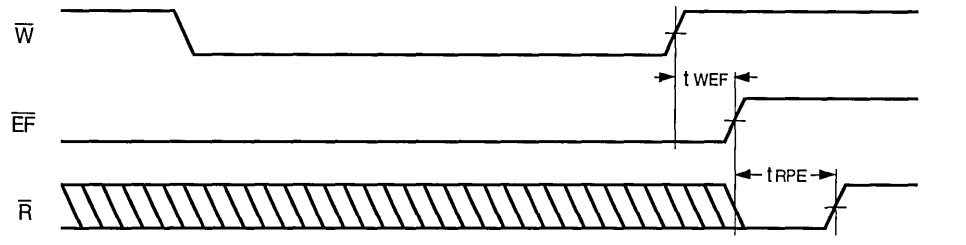


Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse

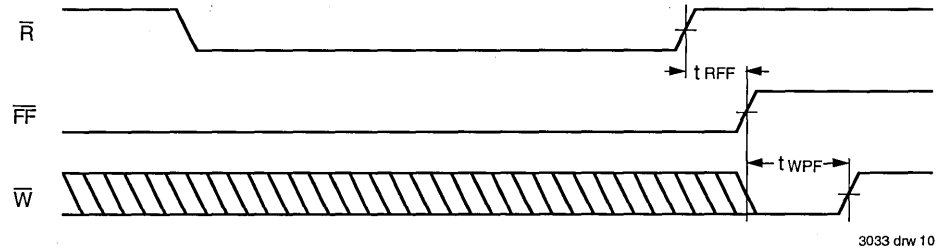


Figure 8. Minimum Timing for an Full Flag Coincident Write Pulse

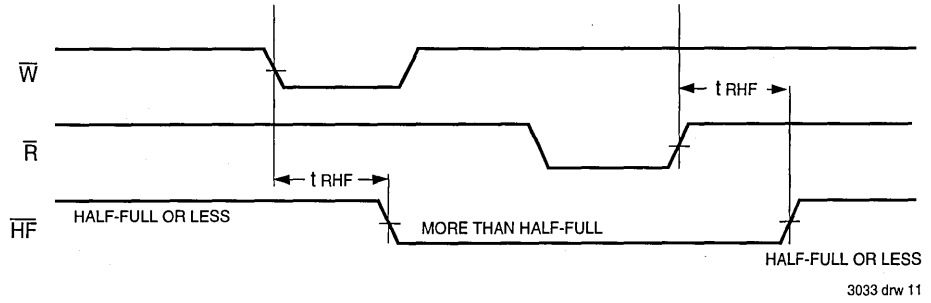


Figure 9. Half-Full Flag Timing

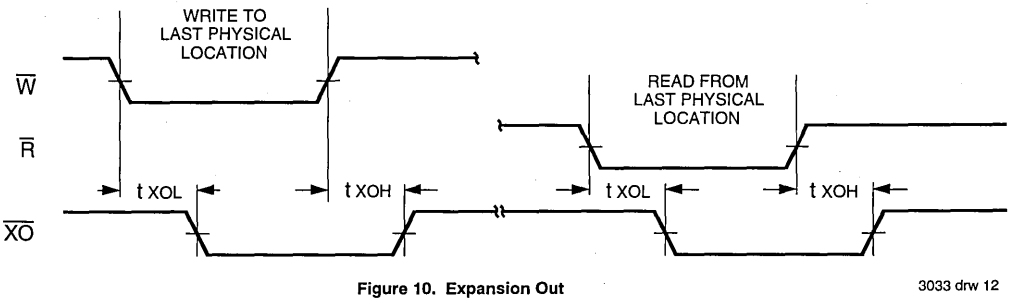


Figure 10. Expansion Out

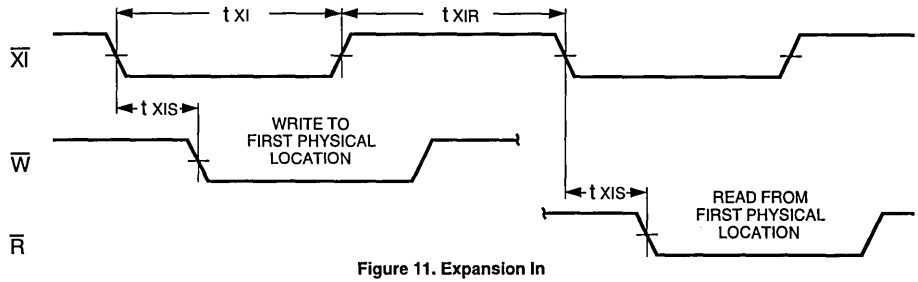


Figure 11. Expansion In

3033 drw 13

OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). For additional information, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs.*

Single Device Mode

A single IDT72V01/72V02/72V03/72V04 may be used when the application requirements are for 512/1024/2048/4096 words or less. IDT72V01/72V02/72V03/72V04 is in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

Depth Expansion

The IDT72V01/72V02/72V03/72V04 can easily be adapted to applications when the requirements are for greater than 512/1,024/2,048/4,096 words. Figure 14 demonstrates Depth Expansion using three IDT72V01/72V02/72V03/72V04s. Any depth can be attained by adding additional IDT72V01/72V02/72V03/72V04s. The IDT72V01/72V02/72V03/72V04 operates in the Depth Expansion mode when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 14.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: *Cascading FIFOs or FIFO Modules.*

USAGE MODES:

Width Expansion

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT72V01/72V02/72V03/72V04s. Any word width can be attained by adding additional IDT72V01/72V02/72V03/72V04s (Figure 13).

Bidirectional Operation

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72V01/72V02/72V03/72V04s as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

Compound Expansion

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).

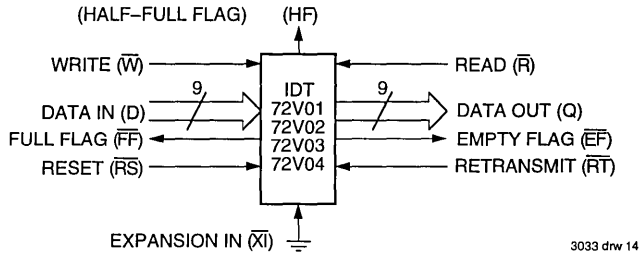


Figure 12. Block Diagram of Single 1024 x 9 FIFO

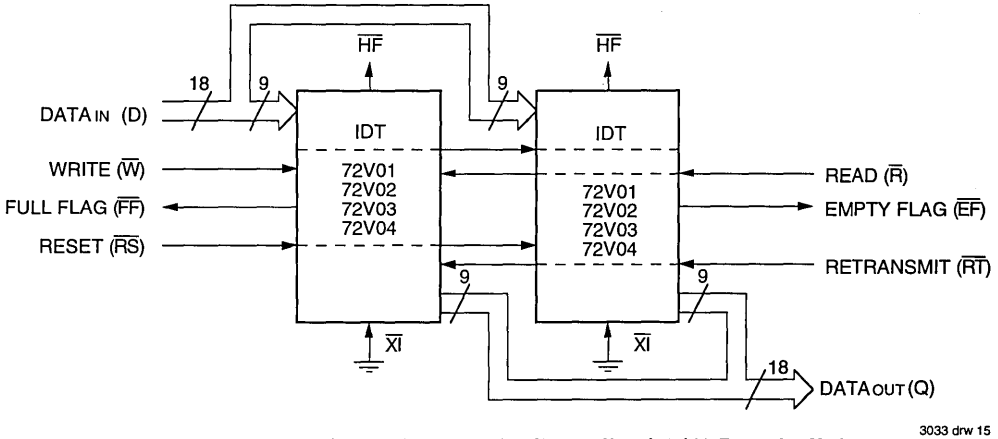


Figure 13. Block Diagram of 1024 x 18 FIFO Memory Used in Width Expansion Mode

TABLE I—RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if flag is HIGH.

3033 tbl 07

TABLE II—RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Flag Full Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output

3033 tbl 08

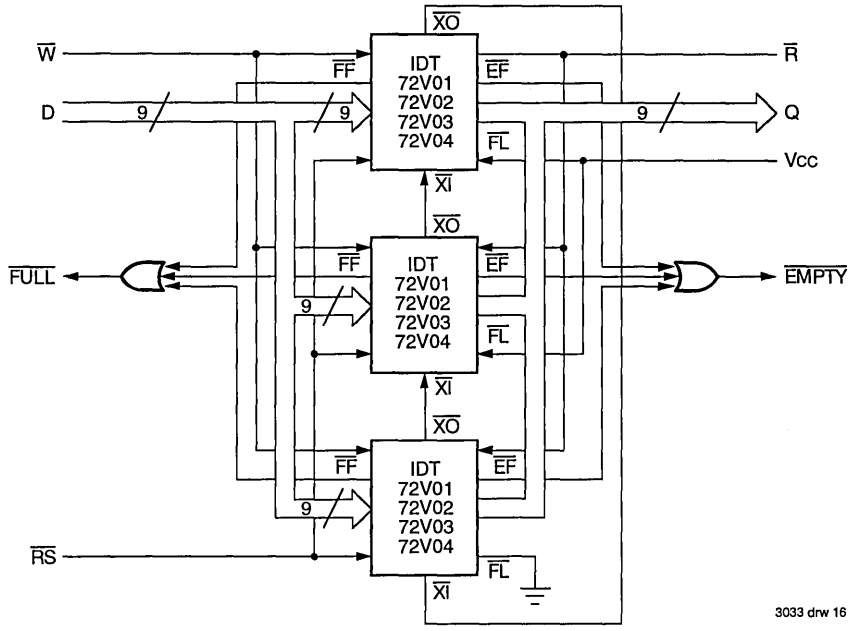


Figure 14. Block Diagram of 3072 x 9 FIFO Memory (Depth Expansion)

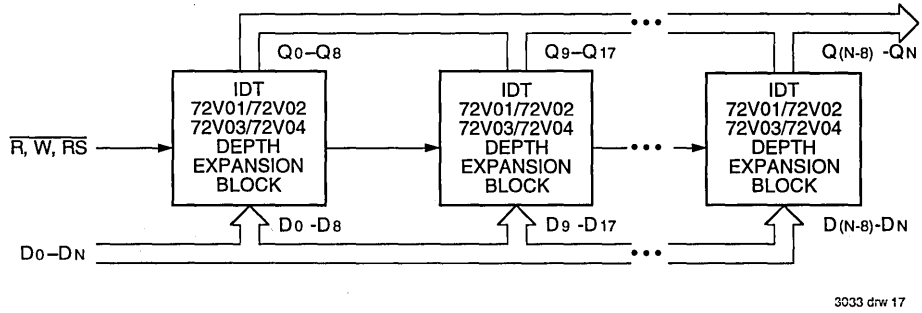


Figure 15. Compound FIFO Expansion

NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

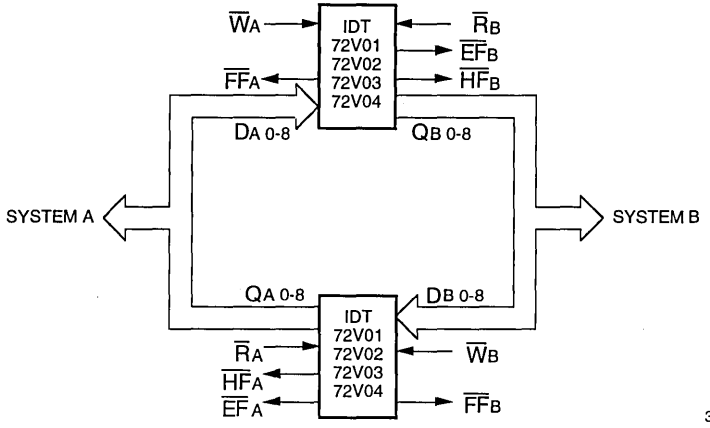


Figure 16. Bidirectional FIFO Mode

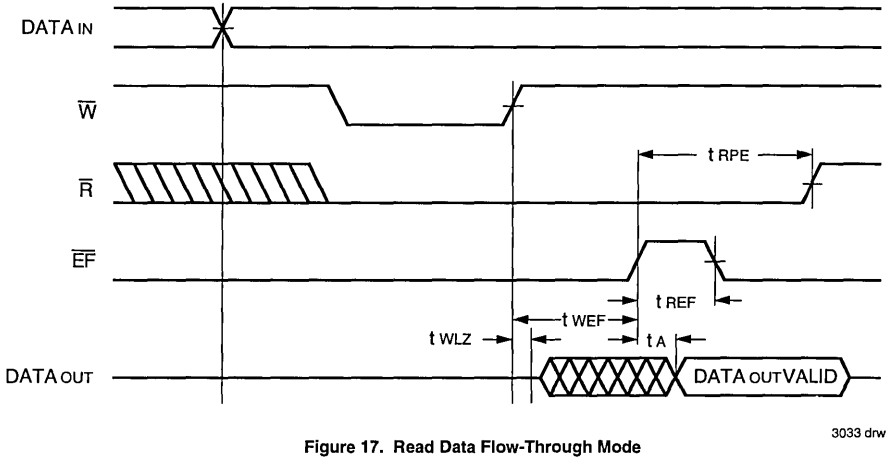


Figure 17. Read Data Flow-Through Mode

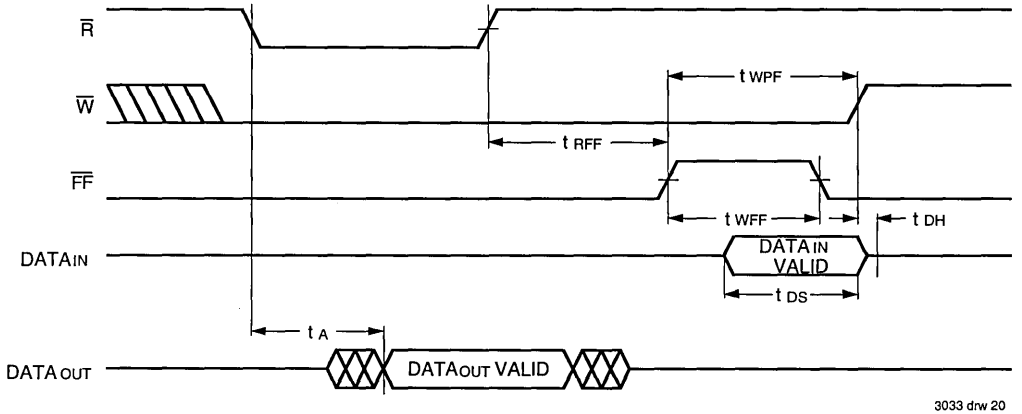
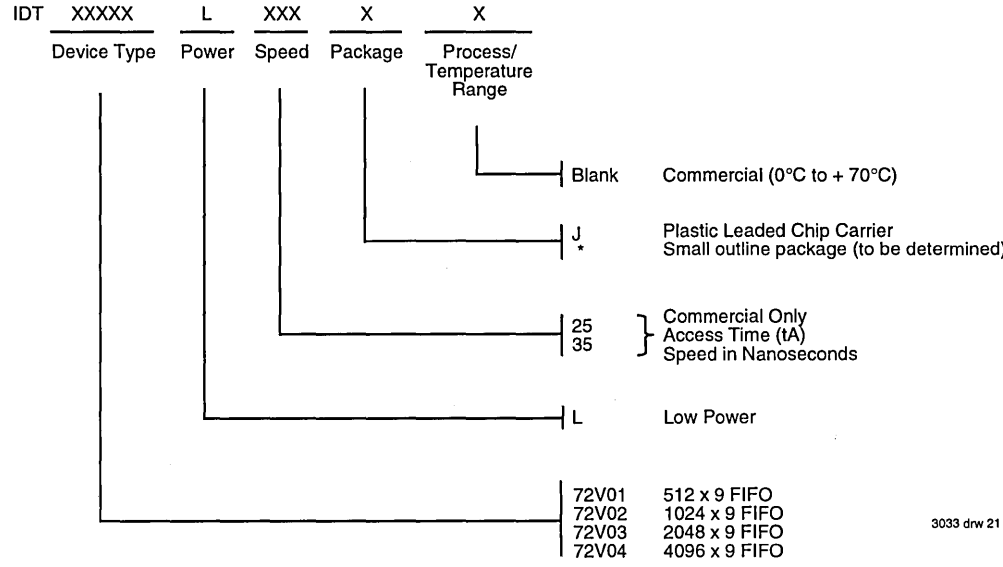


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION



Integrated Device Technology, Inc.

BUS-MATCHING BIDIRECTIONAL FIFO 512 x 18-BIT – 1024 x 9-BIT 1024 x 18-BIT – 2048 x 9-BIT

IDT72510
IDT72520

FEATURES:

- Two side-by-side FIFO memory arrays for bidirectional data transfers
- 512 x 18-Bit – 1024 x 9-Bit (IDT72510)
- 1024 x 18-Bit – 2048 x 9-Bit (IDT72520)
- 18-bit data bus on Port A side and 9-bit data bus on Port B side
- Can be configured for 18-to-9-bit, 36-to-9-bit, or 36-to-18-bit communication
- Fast 25ns access time
- Fully programmable standard microprocessor interface
- Built-in bypass path for direct data transfer between two ports
- Two fixed flags, Empty and Full, for both the A-to-B and the B-to-A FIFO
- Two programmable flags, Almost-Empty and Almost-Full for each FIFO
- Programmable flag offset can be set to any depth in the FIFO
- Any of the eight internal flags can be assigned to four external flag pins
- Flexible reread/rewrite capabilities.
- On-chip parity checking and generation
- Standard DMA control pins for data exchange with peripherals
- IDT72510 and IDT72520 available in the the 52-pin PLCC package

DESCRIPTION:

The IDT72510 and IDT72520 are highly integrated first-in, first-out memories that enhance processor-to-processor and processor-to-peripheral communications. IDT BiFIFOs integrate two side-by-side memory arrays for data transfers in two directions.

The BiFIFOs have two ports, A and B, that both have standard microprocessor interfaces. All BiFIFO operations are controlled from the 18-bit wide Port A. The BiFIFOs incorporate bus matching logic to convert the 18-bit wide memory data paths to the 9-bit wide Port B data bus. The BiFIFOs have a bypass path that allows the device connected to Port A to pass messages directly to the Port B device.

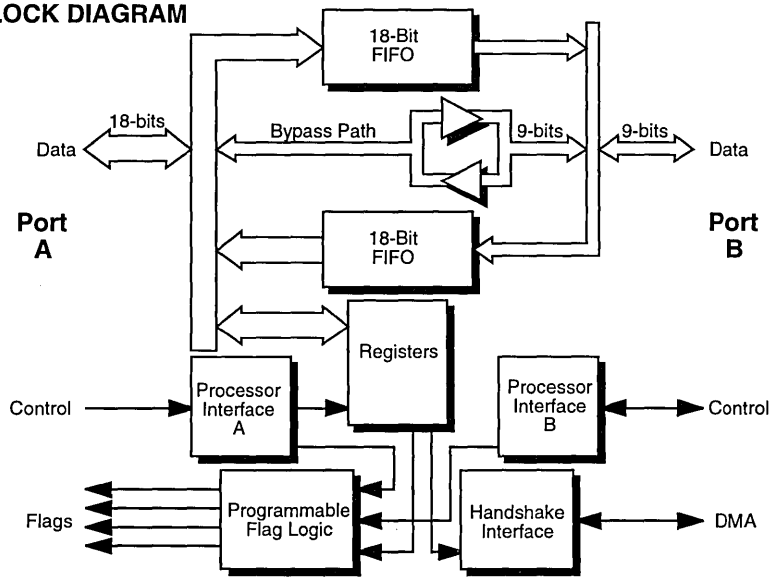
Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

The IDT BiFIFOs have programmable flags. Each FIFO memory array has four internal flags, Empty, Almost-Empty, Almost-Full and Full, for a total of eight internal flags. The Almost-Empty and Almost-Full flag offsets can be set to any depth through the Configuration Registers. These eight internal flags can be assigned to any of four external flag pins (FLGA-FLGD) through one Configuration Register.

Port B has parity, reread/rewrite and DMA functions. Parity generation and checking can be done by the BiFIFO on data passing through Port B. The Reread and Rewrite con-

5

SIMPLIFIED BLOCK DIAGRAM

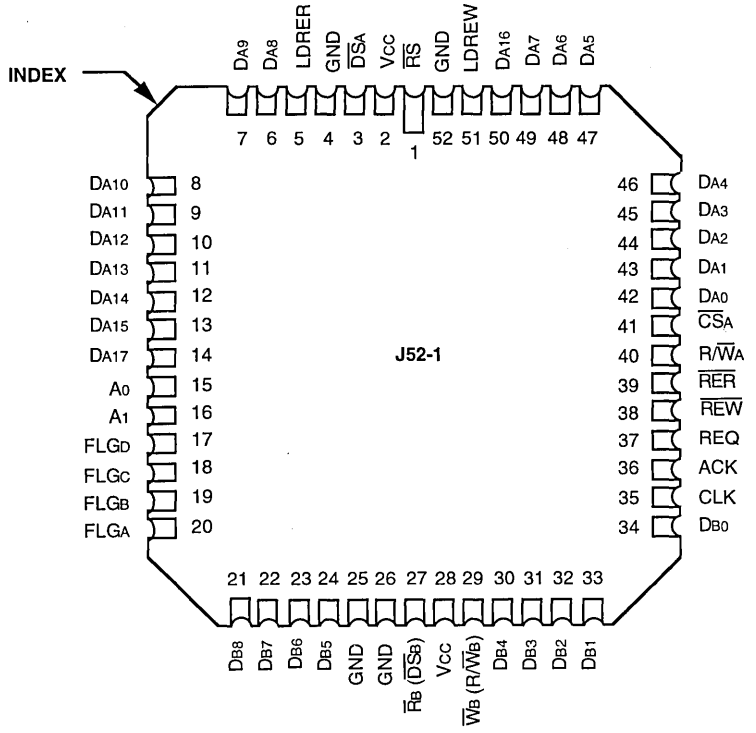


The IDT logo is a registered trademark of Integrated Device Techology, Inc.

2669 drw 01

trols will read or write Port B data blocks multiple times. The BiFIFOs have three pins, REQ, ACK and CLK, to control DMA transfers from Port B devices.

PIN CONFIGURATION



PLCC
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
DA0-DA15	Data A	I/O	Data inputs and outputs for 16 bits of the 18-bit Port A bus.
DA16-DA17	Parity A	I/O	DA16 is the parity bit for DA0-DA7. DA17 is the parity bit for DA8-DA15. DA16 and DA17 can be used as two extra data bits if the parity generate function is disabled.
$\overline{CSA}$	Chip Select A	I	Port A is accessed when Chip Select A is LOW.
$\overline{DSA}$	Data Strobe A	I	Data is written into Port A on the rising edge of Data Strobe when Chip Select is LOW. Data is read out of Port A on the falling edge of Data Strobe when Chip Select is LOW.
R/$\overline{WA}$	Read/Write A	I	This pin controls the read or write direction of Port A. When $\overline{CSA}$ is LOW and R/$\overline{WA}$ is HIGH, data is read from Port A on the falling edge of $\overline{DSA}$. When $\overline{CSA}$ is LOW and R/$\overline{WA}$ is LOW, data is written into Port A on the rising edge of $\overline{DSA}$.
A0, A1	Addresses	I	When Chip Select A is asserted, A0, A1, and Read/Write A are used to select one of six internal resources.
DB0-DB7	Data B	I / O	Data inputs and outputs for 8 bits of the 9-bit Port B bus.
DB8	Parity B	I / O	DB8 is the parity bit for DB0-DB7. DB8 can be used as a data bit if the parity generate function is disabled.
$\overline{RB}$ ($\overline{DSB}$)	Read B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{RB}$) or as part of a Motorola-style interface ($\overline{DSB}$). As an Intel-style interface, data is read from Port B on a falling edge of $\overline{RB}$. As a Motorola-style interface, data is read on the falling edge of $\overline{DSB}$ or written on the rising edge of $\overline{DSB}$ through Port B. The Default is Intel-style processor mode ($\overline{RB}$ as an input).
$\overline{WB}$ (R/$\overline{WB}$)	Write B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{WB}$) or as part of a Motorola-style interface (R/$\overline{WB}$). As an Intel style interface, data is written to Port B on a rising edge of $\overline{WB}$. As a Motorola-style interface, data is read (R/$\overline{WB}$ = HIGH) or written (R/$\overline{WB}$ = LOW) to Port B in conjunction with a Data Strobe B falling or rising edge. The Default is Intel-style processor mode ($\overline{WB}$ as input).
$\overline{RER}$	Reread	I	Loads A-to-B FIFO Read Pointer with the value of the Reread Pointer when LOW.
$\overline{REW}$	Rewrite	I	Loads B-to-A FIFO Write Pointer with the value of the Rewrite Pointer when LOW.
LDRER	Load Reread	I	Loads the Reread Pointer with the value of the A-to-B FIFO Read Pointer when HIGH. This signal is accessible through the Command Register.
LDREW	Load Rewrite	I	Loads the Rewrite Pointer with the value of the B-to-A FIFO Write Pointer when HIGH. This signal is accessible through the Command Register.
REQ	Request	I	When Port B is programmed in peripheral mode, asserting this pin begins a data transfer. Request can be programmed either active HIGH or active LOW.

2669 tbl 01

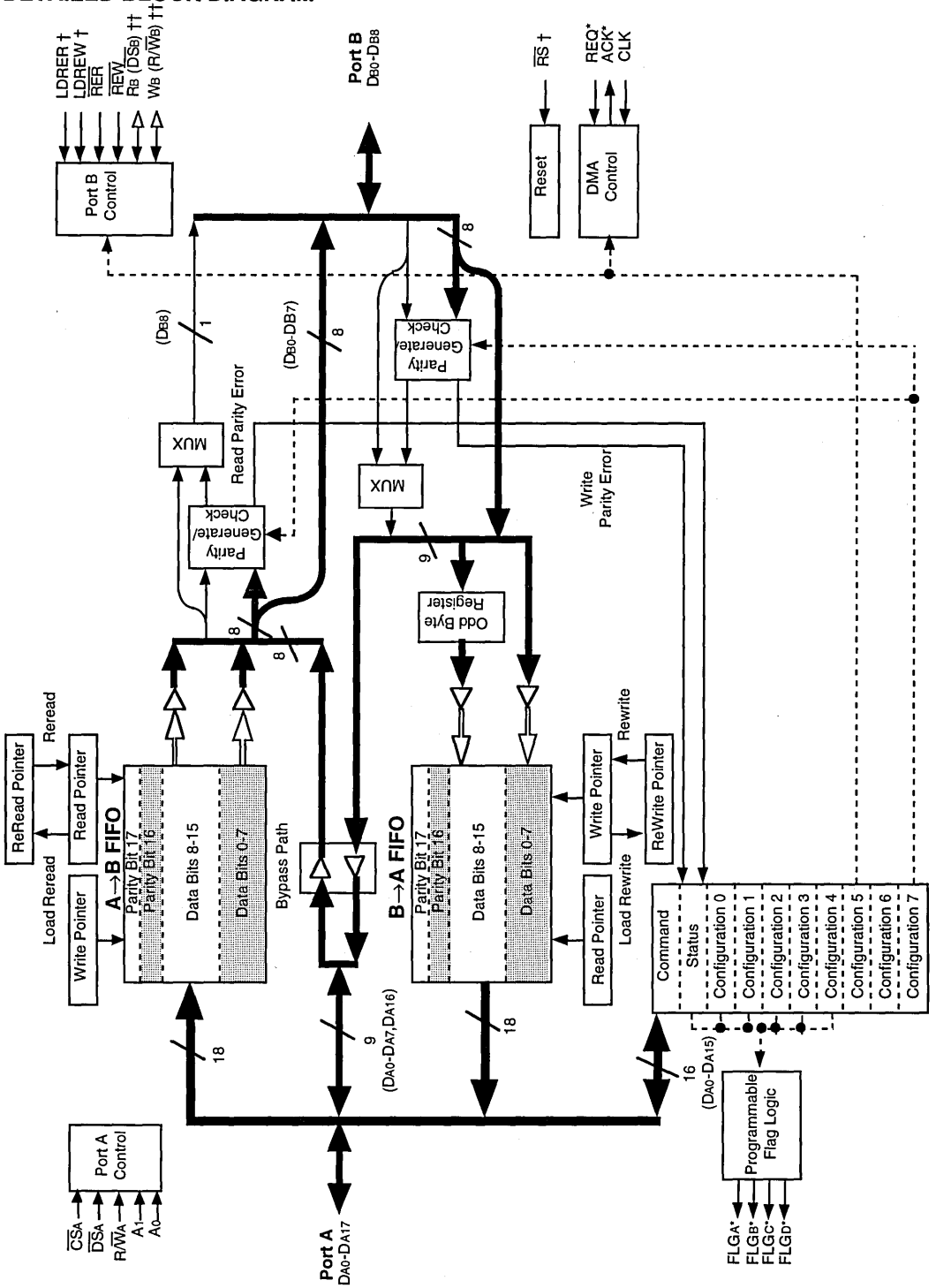
5

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
ACK	Acknowledge	O	When Port B is programmed in peripheral mode, Acknowledge is asserted in response to a Request signal. This confirms that a data transfer may begin. Acknowledge can be programmed either active HIGH or active LOW.
CLK	Clock	I	This pin is used to generate timing for ACK, $\overline{RB}$, $\overline{WB}$, $\overline{DS}$B and R/$\overline{W}$B when Port B is in the peripheral mode.
FLGA-FLGD	Flags	O	These four outputs pins can be assigned to any one of the eight internal flags in the BiFIFO. Each of the two internal FIFOs (A-to-B and B-to-A) has four internal flags: Empty, Almost-Empty, Almost-Full, and Full. If parity checking is enabled, the FLGA pin can also be assigned as a parity error output.
$\overline{RS}$	Reset	I	A LOW on this pin will perform a reset of all BiFIFO functions. Software reset can be achieved through command register.
VCC	Power		There are two +5V power pins on all four devices.
GND	Ground		There are four ground pins

2669 tbl 02

DETAILED BLOCK DIAGRAM



NOTES:
(*) Can be programmed either active high or active low in internal configuration registers.
(†) Accessible through internal registers.
(††) Can be programmed through an internal configuration register to be either an input or an output.

2669 drw 03

FUNCTIONAL DESCRIPTION

IDT's BiFIFO family is versatile for both multiprocessor and peripheral applications. Data can be sent through both FIFO memories concurrently, thus freeing both processors from laborious direct memory access (DMA) protocols and frequent interrupts.

Two full 18-bit wide FIFOs are integrated into the IDT BiFIFO, making simultaneous data exchange possible. Each FIFO is monitored by separate internal read and write pointers, so communication is not only bidirectional, it is also totally independent in each direction. The processor connected to Port A of the BiFIFO can send or receive messages directly to the Port B device using the BiFIFO's 9-bit bypass path.

The BiFIFOs can be used in three different bus configurations: 18 bits to 9 bits, 36 bits to 9 bits and 36 bits to 18 bits. One BiFIFO can be used for the 18- to 9-bit configuration, and two BiFIFOs are required for 36- to 9-bit or 36- to 18-bit configurations. Bits 11 and 12 of Configuration Register 5 determine the BiFIFO configuration (see Table 11 for Configuration Register 5 format).

The microprocessor or microcontroller connected to Port A controls all operations of the BiFIFOs. Thus, all Port A interface pins are inputs driven by the controlling processor. Port B can be programmed to interface either with a second processor or a peripheral device. When Port B is programmed in processor interface mode, the Port B interface pins are inputs driven by the second processor. If a peripheral device is connected to the BiFIFOs, Port B is programmed to peripheral interface mode and the interface pins are outputs.

18- to 9-bit Configurations

A single BiFIFO can be configured to connect an 18-bit processor to another 9-bit processor or a 9-bit peripheral. Bits 11 and 12 of Configuration Register 5 should be set to **00** for a stand-alone configuration. Figures 1 and 2 show the BiFIFO in 18- to 9-bit configurations for processor and peripheral interface modes respectively.

36- to 9-bit Configurations

Two BiFIFOs can be hooked together to create a 36-bit to 9-bit configuration. This means that a 36-bit processor can

36-BIT PROCESSOR to 18-BIT PROCESSOR CONFIGURATION

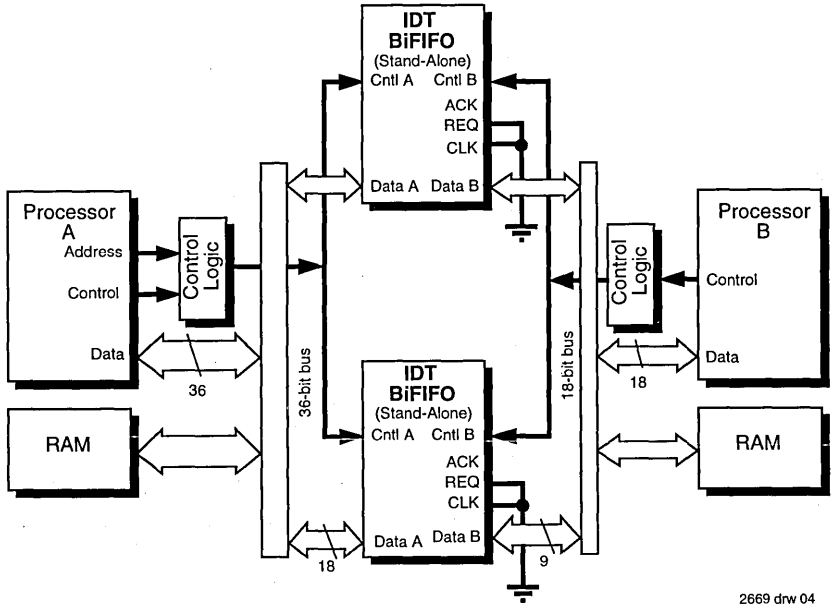


Figure 1. 36- to 18-Bit Processor Interface Configuration

NOTE:

1. Upper BiFIFO only is used in 18- to 9-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, $R/\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to $R/\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

36-BIT PROCESSOR to 18-BIT PERIPHERAL CONFIGURATION

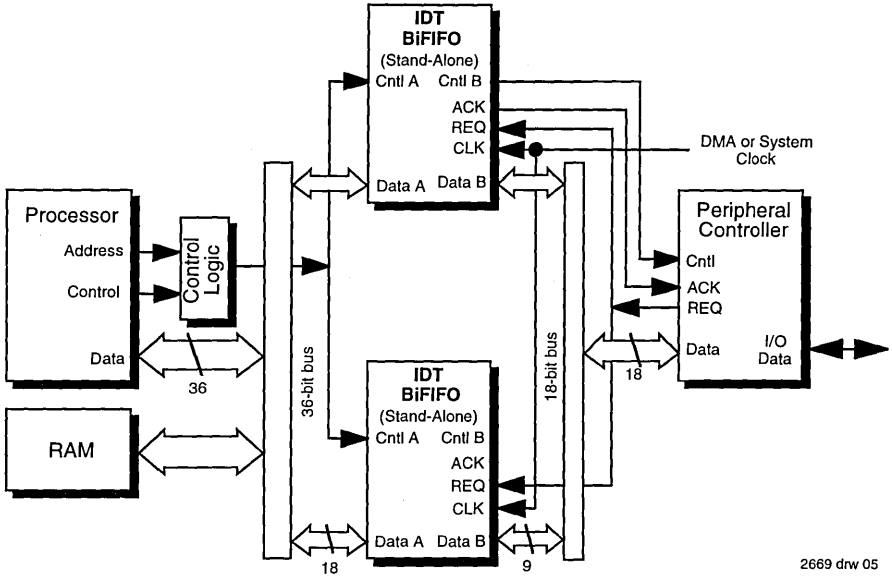


Figure 2. 36- to 18-Bit Peripheral Interface Configuration

NOTE:

1. Upper BiFIFO only is used in 18- to 9-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, $R/\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to $R/\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

talk to a 9-bit processor or a 9-bit peripheral. Both BiFIFOs are programmed simultaneously through Port A by placing one command word on the most significant 16 data bits and one command word on the least significant 16 data bits (parity bits should be ignored).

One BiFIFO must be programmed as the master device and the other BiFIFO is the slave device. Bits 11 and 12 of Configuration Register 5 are set to **10** for the slave device and **11** for the master device. The first two 9-bit words on Port B are read from or written to the slave device and the next two 9-bit words go to the master device.

When both BiFIFOs are in peripheral interface mode, the Port B interface pins of the master device are outputs and this BiFIFO controls the bus. The Port B interface pins of the slave device are inputs driven by the master BiFIFO. Two BiFIFOs are connected in Figure 4 to create a 36- to 9-bit peripheral interface.

The two BiFIFOs shown in Figure 3 are configured to connect a 36-bit processor to a 9-bit processor.

36- to 18-bit Configurations

In a 36- to 18-bit configuration, two BiFIFOs operate in parallel. Both BiFIFOs are programmed simultaneously, 16 data bits to each device with the 4 parity bits ignored.

Both BiFIFOs must be programmed into stand-alone mode for a 36-bit processor to communicate with an 18-bit processor or an 18-bit peripheral. This means that bits 11 and 12 of Configuration Register 5 must be set to **00**.

This configuration can be extended to wider bus widths (54- to 27-bits, 72- to 36-bits, ...) by adding more BiFIFOs to the configuration. Figures 1 and 2 show multiple BiFIFOs configured for processor and peripheral interface modes respectively.

Processor Interface Mode

When a microprocessor or microcontroller is connected to Port B, all BiFIFOs in the configuration must be programmed to processor interface mode. In this mode, all Port B interface controls are inputs. Both REQ and CLK pins should be pulled LOW to ensure that the set-up and hold time requirements for these pins are met during reset. Figures 1 and 3 show BiFIFOs in processor interface mode.

Peripheral Interface Mode

If Port B is connected to a peripheral controller, all BiFIFOs in the configuration must be programmed in the peripheral interface mode. To assure fixed high states for $\overline{R}_B$ and $\overline{W}_B$ before they are programmed into an output, both pins should be pulled-up to Vcc with 10K resistors.

If the BiFIFOs are in stand-alone configuration mode (18-to 9-bit, 36- to 18-bit, ...), then the Port B interface pins are all outputs. Of course, only one set of Port B interface pins should be used to control a single peripheral device, while the other interface pins are all ignored. Figure 2 shows stand-

alone configuration BiFIFOs connected to a peripheral.

In a 36- to 9-bit configuration, the master device controls the bus. The Port B interface pins of the master device are outputs and the interface pins of the slave device are inputs. A 36- to 9-bit configuration of two BiFIFOs connected to a peripheral is shown in Figure 4.

Port A Interface

The BiFIFO is straightforward to use in microprocessor-based systems because each BiFIFO port has a standard microprocessor control set. Port A has access to six resources: the A→B FIFO, the B→A FIFO, the 9-bit direct data bus (bypass path), the configuration registers, status and command registers. The Port A Address and Read/Write pins determine the resource being accessed as shown in Table 1. Data Strobe is used to move data in and out of the BiFIFO.

When either of the internal FIFOs are accessed 18 bits of data are transferred across Port A. Since the bypass path is only 9 bits wide, the least significant byte with parity (D_{A0}-D_{A7}, D_{A16}) is used on Port A. All of the registers are 16 bits wide which means only the data bits (D_{A0}-D_{A15}) are passed by Port A.

36-BIT PROCESSOR to 9-BIT PROCESSOR CONFIGURATION

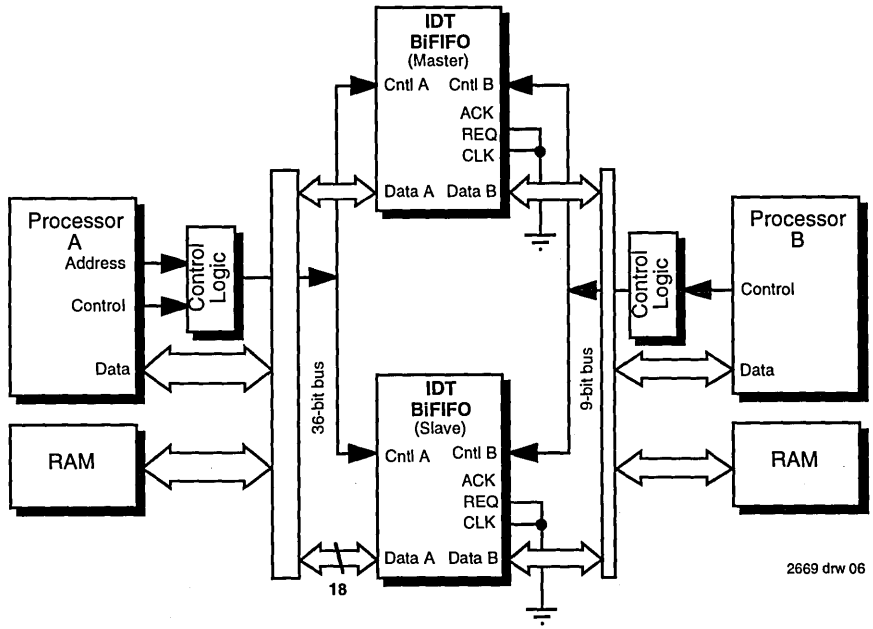


Figure 3. 36- to 9-Bit Processor Interface Configuration

NOTE:

1. *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, $R/\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to $R/\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

36-BIT PROCESSOR to 9-BIT PERIPHERAL CONFIGURATION

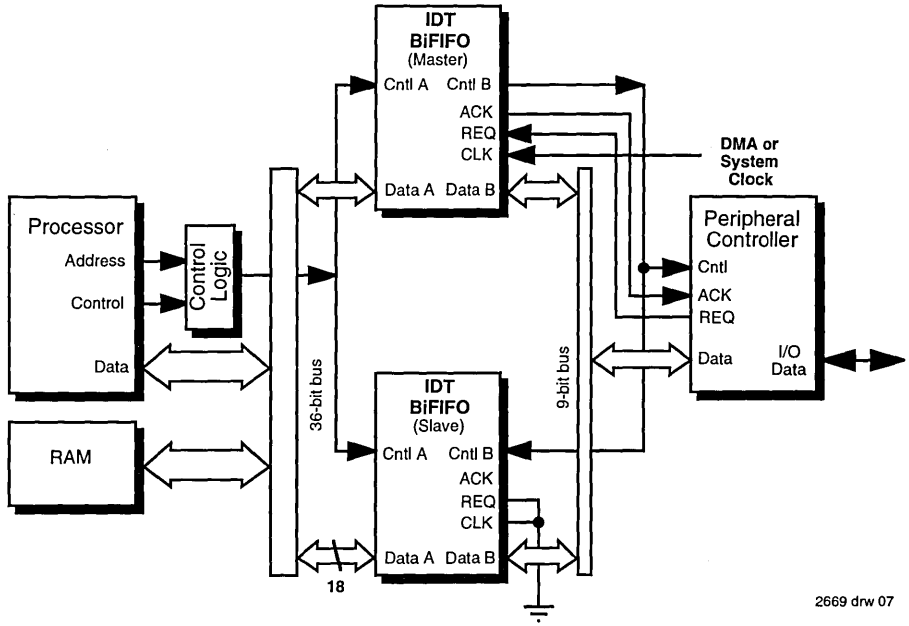


Figure 4. 36- to 9-Bit Peripheral Interface Configuration

NOTE:
1. *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, $R/\overline{W}_A$ and $\overline{DS}_A$; *Cntl B* refers to $R/\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

5

PORT A RESOURCES

$\overline{CS}_A$	A_1	A_0	Read	Write
0	0	0	B→A FIFO	A→B FIFO
0	0	1	9-bit Bypass Path	9-bit Bypass Path
0	1	0	Configuration Registers	Configuration Registers
0	1	1	Status Register	Command Register
1	X	X	Disabled	Disabled

2669 tbl 03

Table 1. Accessing Port A Resources Using $\overline{CS}_A$, A_0, and A_1

Bypass Path

The bypass path acts as a bidirectional bus transceiver directly between Port A and Port B. The direct connection requires that the Port A interface pins are inputs and the Port B interface pins are outputs. The bypass path is 9 bits wide in an 18- to 9-bit configuration or in a 36- to 9-bit configuration. Only in the 36- to 18-bit configuration is the bypass path 18 bits wide.

During bypass operations, the BiFIFOs must be programmed into peripheral interface mode. Bit 10 of Configuration Register 5 (see Table 11) is set to **1** for peripheral interface mode. In a 36- to 9-bit configuration, both Port B data buses will be active. Data written into Port A will appear on both master and slave Port B buses concurrently. To avoid Port B bus contention, the data on D_{A0}-D_{A7} and D_{A16} of both BiFIFOs should be exactly the same. Data read from Port A will appear on pins D_{A0}-D_{A7} and D_{A16} of both BiFIFOs within the same 36-bit word.

Command Register

Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

The Command Register is written by setting $\overline{CS}_A = 0$, $A_1 = 1$, $A_0 = 1$. Commands written into the BiFIFO have a 4-bit opcode (bit 8 – bit 11) and a 3-bit operand (bit 0 – bit 2) as shown in Figure 5. The commands can be used to reset the BiFIFO, to select the Configuration Register, to perform intelligent reread/rewrite, to set the Port B DMA direction, to set the Status Register format, to modify the Port B Read and Write Pointers, and to clear Port B parity errors. The command opcodes are shown in Table 2.

The reset command initializes different portions of the BiFIFO depending on the command operand. Table 3 shows the reset command operands.

The Configuration Register address is set directly by the command operands shown in Table 4.

Intelligent reread/rewrite is performed by changing the Port B Read Pointer with the Reread Pointer or by changing the Port B Write Pointer with the Rewrite Pointer. No command operands are required to perform a reread/rewrite operation.

When Port B of the BiFIFO is in peripheral mode, the DMA direction is controlled by the Command Register. Table 5 shows the Port B read/write DMA direction operands.

The BiFIFO supports two Status Register formats. Status Register format 1 gives all the internal flag status, while Status Register format 0 provides the data in the Odd Byte Register. Table 6 gives the operands for selecting the appropriate Status Register format. See Table 8 for the details of the two Status Register formats.

Two commands are provided to increment the Port B Read and Write Pointers in case reread/rewrite is performed. Incrementing the pointers guarantees that pointers will be on a word boundary when an odd number of bytes is transmitted through Port B. No operands are required for these commands.

When parity check errors occur on Port B, a clear parity error command is needed to remove the parity error. There are no operands for these commands.

COMMAND OPERATIONS

Command Opcode	Function
0000	Reset BiFIFO (see Table 3)
0001	Select Configuration Register (see Table 4)
0010	Load Reread Pointer with Read Pointer Value
0011	Load Rewrite Pointer with Write Pointer Value
0100	Load Read Pointer with Reread Pointer Value
0101	Load Write Pointer with Rewrite Pointer Value
0110	Set DMA Transfer Direction (see Table 5)
0111	Set Status Register Format (see Table 6)
1000	Increment in byte for A→B FIFO Read Pointer (Port B)
1001	Increment in byte for B→A FIFO Write Pointer (Port B)
1010	Clear Write Parity Error Flag
1011	Clear Read Parity Error Flag

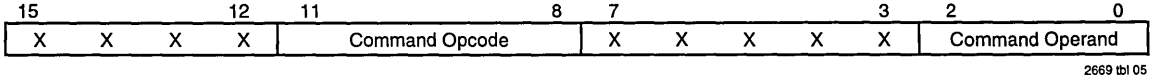
2669 tbl 04

Table 2. Functions Performed by Port A Commands

Reset

The IDT72510 and IDT72520 have a hardware reset pin ($\overline{RS}$) that resets all BiFIFO functions. A hardware reset requires the following four conditions: $\overline{R}_B$ and $\overline{W}_B$ must be HIGH, $\overline{RER}$ and $\overline{REW}$ must be HIGH, LDRER and LDREW must be LOW, and $\overline{DS}_A$ must be HIGH (Figure 9). After a hardware reset, the BiFIFO is in the following state: Configuration Registers 0-3 are **0000H**, Configuration Register 4 is set to

COMMAND FORMAT



2669 tbl 05

Figure 5. Format for Commands Written into Port A

RESET COMMAND FUNCTIONS

Reset Operands	Function
000	No Operation
001	Reset B→A FIFO (Read, Write, and Rewrite Pointers = 0)
010	Reset A→B FIFO (Read, Write, and Reread Pointers = 0)
011	Reset B→A and A→B FIFO
100	Reset Internal DMA Request Circuitry
101	No Operation
110	No Operation
111	Reset All

2669 tbl 06

Table 3. Reset Command Functions

6420H, and Configuration Registers 5 and 7 are **0000H**. Additionally, Status Register format 0 is selected, all the pointers including the Reread and Rewrite Pointers are set to **0**, the odd byte register valid bit is cleared, the DMA direction is set to B→A write, the internal DMA request circuitry is cleared (set to its initial state), and all parity errors are cleared.

A software reset command can reset A→B pointers and the B→A pointers to **0** independently or together. The request (REQ) DMA circuitry can also be reset independently. A software Reset All command resets all the pointers, the DMA request circuitry, and sets all the Configuration Registers to their default condition. Note that a hardware reset is **NOT** the same as a software Reset All command. Table 7 shows the BiFIFO state after the different hardware and software resets.

SELECT CONFIGURATION REGISTER COMMAND FUNCTIONS

Operands	Function
000	Select Configuration Register 0
001	Select Configuration Register 1
010	Select Configuration Register 2
011	Select Configuration Register 3
100	Select Configuration Register 4
101	Select Configuration Register 5
110	Select Configuration Register 6
111	Select Configuration Register 7

2669 tbl 07

Table 4. Select Configuration Register Command Functions.

DMA DIRECTION COMMAND FUNCTIONS

Operands	Function
XX0	Write B→A FIFO
XX1	Read A→B FIFO

2669 tbl 08

Table 5. Set DMA Direction Command Functions. Command Only Operates in Peripheral Interface Mode

STATUS REGISTER FORMAT COMMAND FUNCTIONS

Operands	Function
XX0	Status Register Format 0
XX1	Status Register Format 1

2669 tbl 09

Table 6. Command Functions to Set the Status Register Format

STATE AFTER RESET

	Hardware Reset	Software Reset				
	($\overline{RS}$ asserted)	B→A (001)	A→B (010)	B→A and A→B (011)	Internal Request (100)	All (111)
Configuration Registers 0-3	0000H	—	—	—	—	0000H
Configuration Register 4	6420H	—	—	—	—	6420H
Configuration Register 5	0000H	—	—	—	—	0000H
Configuration Register 7	0000H	—	—	—	—	0000H
Status Register format	0	—	—	—	—	—
B→A Read, Write, Rewrite Pointers	0	0	—	0	—	0
A→B Read, Write, Reread Pointers	0	—	0	0	—	0
Odd byte register valid bit	clear	clear	—	clear	—	clear
DMA direction	B→A write	—	—	—	—	—
DMA internal request	clear	—	—	—	clear	clear
Parity errors	clear	—	—	—	—	—

2669 tbl 10

Table 7. The BiFIFO State After a Reset Command

Status Register

The Status Register reports the state of the programmable flags, the DMA read/write direction, the Odd Byte Register valid bit, and parity errors. The Status Register is read by setting $\overline{CS}_A$ = 0, A_1 = 1, A_0 = 1 (see Table 1).

There are two Status Register formats that are set by a Status Register format command. Format **0** stores the Odd Byte Register data in the lower eight bits of the Status Register, while format **1** reports the flag states and the DMA read/write direction in the lower eight bits. The upper eight bits are identical for both formats. The flag states, the parity errors, the Odd Byte Register valid bit, and the Status Register format are all in the upper eight bits of the Status Register. See Table 8 for both Status Register formats.

Configuration Registers

The eight Configuration Register formats are shown in Table 9. Configuration Registers 0-3 contain the programmable flag offsets for the Almost Empty and Almost Full flags. These offsets are set to **0** when a hardware reset or a software reset all is applied. Note that Table 9 shows that Configuration Registers 0-3 are 10 bits wide to accommodate the 1024 locations in each FIFO memory of the IDT72520. Only 9 least significant bits are used for the 512 locations of the IDT72510; the most significant bit, bit 9, must be set to **0**.

Configuration Register 4 is used to assign the internal flags to the external flag pins (FLG_A-FLG_D). Each external flag pin is assigned an internal flag based on the four bit codes shown in Table 10. The default condition for Configuration Register 4 is **6420H** as shown in Table 7. The default flag assignments are: FLG_D is assigned B→A $\overline{Full}$, FLG_C is assigned B→A $\overline{Empty}$, FLG_B is assigned A→B $\overline{Full}$, FLG_A is assigned A→B $\overline{Empty}$.

Configuration Register 5 is a general control register. The format of Configuration Register 5 is shown in Table 11. Bit 0 sets the Intel-style interface ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style interface ($\overline{DS}_B$, R/$\overline{W}_B$) for Port B. Bit 1 changes the byte order for data coming through Port B. Bits 2 and 3 redefine Full and Empty Flags for reread/rewrite data protection.

Bits 4-9 control the DMA interface and are only applicable in peripheral interface mode. In processor interface mode, these bits are don't care states. Bits 4 and 5 set the polarity of the DMA control pins REQ and ACK, respectively. An internal clock controls all DMA operations. This internal clock is derived from the external clock (CLK). Bit 9 determines the internal clock frequency: the internal clock = CLK or the internal clock = CLK divided by 2. Bit 8 sets whether $\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for either one or two internal clocks. Bits 6 and 7 set the number of internal clocks between REQ assertion and ACK assertion. The timing can be from 2 to 5 cycles as shown in Figure 17.

Bit 10 controls Port B processor or peripheral interface mode. In processor mode, the Port B control pins ($\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$, R/$\overline{W}_B$) are inputs and the DMA controls are ignored. In peripheral mode, the Port B control pins are outputs and the DMA controls are active.

Bits 11 and 12 set the width expansion mode. For 18- to 9-bit configurations or 36- to 18-bit configurations, the BiFIFO should be set in stand-alone mode. For a 36- to 9-bit configuration, one BiFIFO must be in slave mode and the other BiFIFO must be in master mode. The master BiFIFO allows the first two bytes transferred across Port B to go to the slave BiFIFO, then the next two bytes go to the master BiFIFO.

Configuration Register 7 controls the parity functions of Port B as shown in Table 12. Either parity generation or parity

STATUS REGISTER FORMAT 0

Bit	Signal
0	Odd Byte Register
1	
2	
3	
4	
5	
6	
7	
8	Valid Bit
9	Write Parity Error
10	Read Parity Error
11	Status Register Format = 0
12	A→B Full Flag
13	A→B Almost-Full Flag
14	B→A Empty Flag
15	B→A Almost-Empty Flag

2669 tbl 11

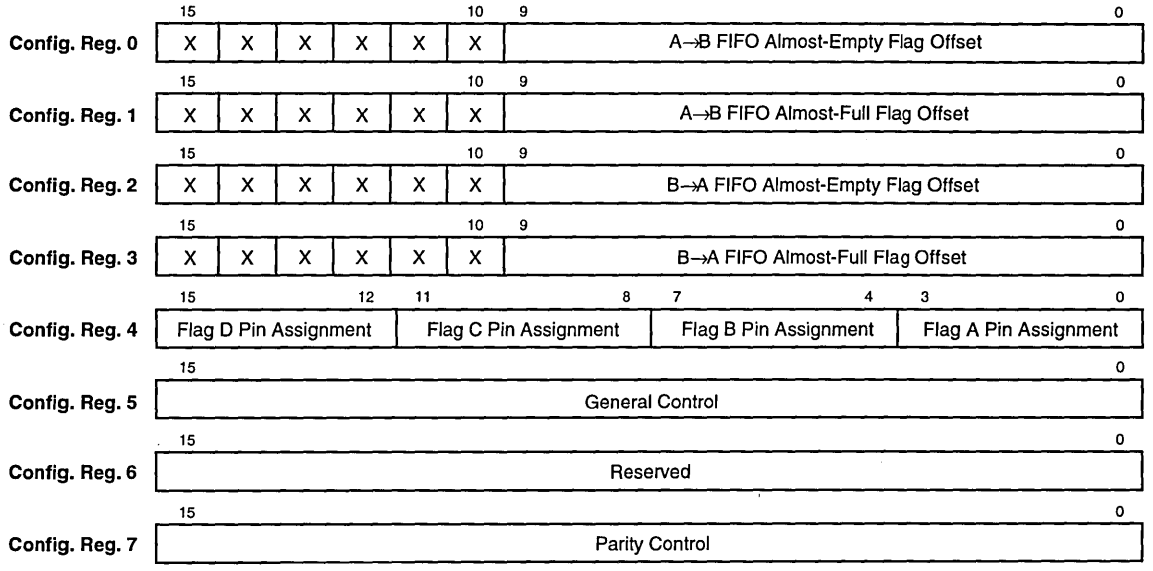
STATUS REGISTER FORMAT 1

Bit	Signal
0	Reserved
1	Reserved
2	Reserved
3	DMA Direction
4	A→B Empty Flag
5	A→B Almost-Empty Flag
6	B→A Full Flag
7	B→A Almost-Full Flag
8	Valid Bit
9	Write Parity Error
10	Read Parity Error
11	Status Register Format = 1
12	A→B Full Flag
13	A→B Almost-Full Flag
14	B→A Empty Flag
15	B→A Almost-Empty Flag

2669 tbl 12

Table 8. The Two Status Register Formats

CONFIGURATION REGISTER FORMATS



NOTE:

1. Bit 9 of Configuration Registers 0-3 must be set to 0 on the IDT72510.

2669 tbl 13

Table 9. The BiFIFO Configuration Register Formats

checking is enabled for data read and written through Port B. Bit 8 controls parity checking and generation for B→A write data. Bit 9 controls parity checking and generation for A→B read data. Bit 10 controls whether the parity is odd or even. Bit 11 is used to assign the internal parity checking error to the FLGA pin. When the parity error is assigned to FLGA, the Configuration Register 4 flag assignment for FLGA is ignored.

Programmable Flags

The IDT BiFIFO has eight internal flags; four of these flags have programmable offsets, the other four are empty or full. Associated with each FIFO memory array are four internal flags, Empty, Almost-Empty, Almost-Full and Full, for the total of eight internal flags. The Almost-Empty and Almost-Full offsets can be set to any depth through the Configuration Registers 0-3 (see Table 9). The offset (or depth) of FIFO RAM array is based on the unit of an 18-bit word. The flags are asserted at the depths shown in Table 13. After a hardware reset or a software reset all, the almost flag offsets are set to **0**. Even though the offsets are equivalent, the Empty and Almost-Empty flags have different timing which means that the flags are not coincident. Similarly, the Full and Almost-Full flags are not coincident because of timing.

These eight internal flags can be assigned to any of four external flag pins (FLGA-FLGD) through Configuration Register 4 (see Table 10). For the specific flag timings, see Figures 20-23.

The current state of all eight flags is available in the Status Register in Status Register format 1. In Status Register format 0, only four flags can be found in the Status Register (see Table 8).

EXTERNAL FLAG ASSIGNMENT CODES

Assignment Code	Internal Flag Assigned to Flag Pin
0000	A→B $\overline{\text{Empty}}$
0001	A→B $\overline{\text{Almost-Empty}}$
0010	A→B $\overline{\text{Full}}$
0011	A→B $\overline{\text{Almost-Full}}$
0100	B→A $\overline{\text{Empty}}$
0101	B→A $\overline{\text{Almost-Empty}}$
0110	B→A $\overline{\text{Full}}$
0111	B→A $\overline{\text{Almost-Full}}$
1000	A→B Empty
1001	A→B Almost-Empty
1010	A→B Full
1011	A→B Almost-Full
1100	B→A Empty
1101	B→A Almost-Empty
1110	B→A Full
1111	B→A Almost-Full

2669 tbl 14

Table 10. Configuration Register 4 Internal Flag Assignments to External Flag Pins.

5

Port B Interface

Port B also has parity, reread/rewrite and DMA functions. Port B can be configured to interface to either Intel-style ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style ($\overline{DS}_B$, R/$\overline{W}_B$) devices in Configuration Register 5 (see Table 11). Port B can also be configured to talk to a processor or a peripheral device through Configuration Register 5. In processor interface mode, the Port B interface controls are inputs. In peripheral interface mode, the Port B interface controls are outputs. After a hardware reset or a software Reset All command, Port B defaults to an Intel-style processor interface; the controls are inputs.

Two 9-bit words are put together to create each 18-bit word stored in the internal FIFOs. The first 9-bit word written to Port B goes into the Odd Byte Register shown in the detailed block diagram. The Odd Byte Register valid bit (Bit 8) in the Status Register is **1** when this first 9-bit word is written. The data bits from Port B (D_{B0}-D_{B7}) are also stored in the lower 8 bits of the Status Register when Status Register format 0 is selected (see Table 8). The second write on Port B moves the 9-bits from Port B and the 9-bits in the Odd Byte Register into the B→A FIFO and advances the B→A Write Pointer. The Status Register valid bit is set to **0** after the second write.

When Port B reads data from the A→B FIFO, two buffers choose which 9 of the 18 memory bits are sent to Port B. These buffers alternate between the upper 9 bits (D_{A8}-D_{A15}, D_{A17}) and the lower 9 bits (D_{A0}-D_{A7}, D_{A16}). The A→B Read Pointer is advanced after every two Port B reads.

The BiFIFO can be set to order the 9-bit data so the first 9-

CONFIGURATION REGISTER 5 FORMAT

Bit	Function		
0	Select Port B Interface $\overline{R}_B$ & $\overline{W}_B$ or $\overline{DS}_B$ & R/$\overline{W}_B$	0	Pins are $\overline{R}_B$ and $\overline{W}_B$ (Intel-style interface)
		1	Pins are $\overline{DS}_B$ and R/$\overline{W}_B$ (Motorola-style interface)
1	Byte Order of 18-bit Word	0	Lower byte D_{A7}-D_{A0} and parity D_{A16} are read or written first on Port B
		1	Upper byte D_{A15}-D_{A8} and parity D_{A17} are read or written first on Port B
2	Full Flag Definition	0	Full Flag is asserted when write pointer meets read pointer
		1	Full Flag is asserted when write pointer meets reread pointer
3	Empty Flag Definition	0	Empty Flag is asserted when read pointer meets write pointer
		1	Empty Flag is asserted when read pointer meets rewrite pointer
4	REQ Pin Polarity	0	REQ pin active HIGH
		1	REQ pin active LOW
5	ACK Pin Polarity	0	ACK pin active LOW
		1	ACK pin active HIGH
7-6	REQ / ACK Timing	00	2 internal clocks between REQ assertion and ACK assertion
		01	3 internal clocks between REQ assertion and ACK assertion
		10	4 internal clocks between REQ assertion and ACK assertion
		11	5 internal clocks between REQ assertion and ACK assertion
8	Port B Read and Write Timing Control for Peripheral Mode	0	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 1 internal clock
		1	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 2 internal clocks
9	Internal Clock Frequency Control	0	internal clock = CLK
		1	internal clock = CLK divided by 2
10	Port B Interface Mode Control	0	Processor interface mode (Port B controls are inputs)
		1	Peripheral interface mode (Port B controls are outputs)
12-11	Width Expansion Mode Control	00	Stand-alone mode (18- to 9-bits, 36- to 18-bits)
		01	Reserved
		10	Slave width expansion mode (36- to 9-bits)
		11	Master width expansion mode (36- to 9-bits)
13	Unused		
14	Unused		
15	Unused		

2669 tbl 15

Table 11. BiFIFO Configuration Register 5 Format

CONFIGURATION REGISTER 7 FORMAT

BIT	FUNCTION		
0-7	Unused		
8	Parity Input Control B→A	0	Disable Parity Generate, Enable Parity Check
		1	Enable Parity Generate, Disable Parity Check
9	Parity Output Control A→B	0	Disable Parity Generate, Enable Parity Check
		1	Enable Parity Generate, Disable Parity Check
10	Parity Odd/Even Control	0	Odd
		1	Even
11	Assign Parity Error to Flag A Pin	0	No Parity Error Output
		1	Parity Error on Flag A Pin
12-15	Unused		

2669 tbl 16

Table 12. BiFIFO Configuration Register 7 Format

bits go to the LSB (D_{A0}-D_{A7}, D_{A16}) or the MSB (D_{A8}-D_{A15}, D_{A17}) of Port A. This data ordering is controlled by bit 1 of Configuration Register 5 (see Table 11).

DMA Control Interface

The BiFIFO has DMA control to simplify data transfers with peripherals. For the BiFIFO DMA controls (REQ, ACK and CLK) to operate, the BiFIFO must be in peripheral interface mode (Configuration Register 5, Table 11).

DMA timing is controlled by the external clock input, CLK. An internal clock is derived from this CLK signal to generate the $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and R/$\overline{W}_B$ output signals. The internal clock also determines the timing between REQ assertion and ACK assertion. Bit 9 of Configuration Register 5 determines whether the internal clock is the same as CLK or whether the internal clock is CLK divided by 2.

Bit 8 of Configuration Register 5 sets whether $\overline{R}_B$, $\overline{W}_B$ and $\overline{DS}_B$ are asserted for 1 or 2 internal clocks. Bits 6 and 7 of Configuration Register 5 set the number of clocks between REQ assertion and ACK assertion. The clocks between REQ assertion and ACK assertion can be 2, 3, 4 or 5.

Bits 4 and 5 of Configuration Register 5 set the polarity of the REQ and ACK pins, respectively.

A DMA transfer command sets the Port B read/write direction (see Table 5). The timing diagram for DMA transfers is shown in Figure 17. The basic DMA transfer starts with REQ assertion. After 2 to 5 internal clocks, ACK is asserted by the BiFIFO. ACK will not be asserted if a read is attempted on an Empty A→B FIFO or if a write is attempted on a Full B→A FIFO. If the BiFIFO is in Motorola-style interface mode, R/$\overline{W}_B$ is set at the same time that ACK is asserted. One internal clock later, $\overline{DS}_B$ is asserted. If the BiFIFO is in Intel-style interface mode, either $\overline{R}_B$ or $\overline{W}_B$ is asserted one internal clock after ACK assertion. These read/write controls stay asserted for 1 or 2 internal clocks, then ACK, $\overline{DS}_B$, $\overline{R}_B$ and $\overline{W}_B$ are made inactive. This completes the transfer of one 9-bit word.

On the next rising edge of CLK, REQ is sampled. If REQ is still asserted, another DMA transfer starts with the assertion of ACK. Data transfers will continue as long as REQ is asserted.

Parity Checking and Generation

Parity generation or checking is performed by the BiFIFO on data passing through Port B. Parity can either be odd or even as determined by Bit 10 of Configuration Register 7.

When parity checking is enabled, D_{B8} is treated as a data bit. D_{B8} data will be passed to D_{A16} (bypass operation) or stored in the RAM array (FIFO operation) for B->A operation; similarly, D_{A16} or parity bits from the RAM array will be passed to D_{B8} for A->B operations. A->B read parity errors and B->A write parity errors are shown in Bit 9 and 10 in the Status Register. If an external parity error signal is required, a logical OR of the

INTERNAL FLAG TRUTH TABLE

Number of Words in FIFO					
From	To	Empty Flag	Almost-Empty Flag	Almost-Full Flag	Full Flag
0	0	Asserted	Asserted	Not Asserted	Not Asserted
1	n	Not Asserted	Asserted	Not Asserted	Not Asserted
n + 1	D - (m + 1)	Not Asserted	Not Asserted	Not Asserted	Not Asserted
D - m	D - 1	Not Asserted	Not Asserted	Asserted	Not Asserted
D	D	Not Asserted	Not Asserted	Asserted	Asserted

NOTE: 2669 tbl 17

1. BiFIFO flags can be assigned to external flag pins to be observed. D = FIFO depth (IDT72510 = 512, IDT72520 = 1024), n = Almost-Empty flag offset, m = Almost-Full flag offset.

Table 13. Internal Flag Truth Table.

two parity error bits is brought out to FLGA pin by setting Bit 11 of Configuration Register 7.

Parity generation creates the ninth bit. This ninth bit is placed on DB8 for A->B read operation, and on DA16 or RAM array for B->A write operation.

It is recommended that if the parity pins (DB8, DA16, and DA17) are not used, they should be pulled down with 10K resistors for noise immunity.

Intelligent Reread/Rewrite

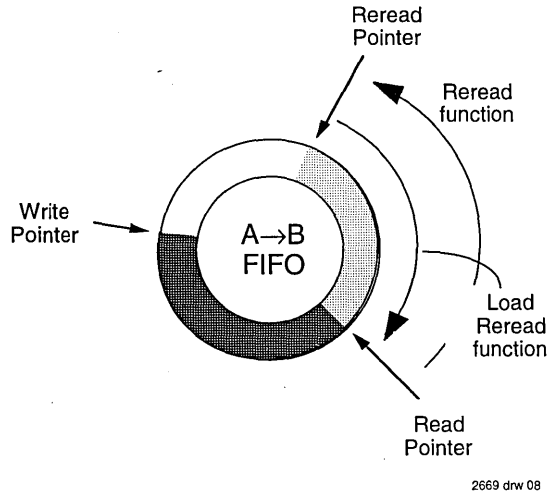
Intelligent reread/rewrite is a method the BiFIFO uses to help assure data integrity. Port B of the BiFIFO has two extra pointers, the Reread Pointer and the Rewrite Pointer. The Reread Pointer is associated with the A->B FIFO Read Pointer, while the Rewrite Pointer is associated with the B->A FIFO Write Pointer. The Reread Pointer holds the start address of a data block in the A->B FIFO RAM, and the Read Pointer is the current address of the same FIFO RAM array. By loading the Read Pointer with the value held in the Reread Pointer (RER asserted), reads will start over at the beginning of the data block. In order to mark the beginning of a data block, the Reread Pointer should be loaded with the Read Pointer value (LDRER asserted) before the first read is performed on this data block. Figure 6 shows a Reread operation.

Similarly, the Rewrite Pointer holds the start address of a data block in the B->A FIFO RAM, while the Write Pointer is the current address within the RAM array. The operation of the REW and LDREW is identical to the RER and LDRER discussed above. Figure 7 shows a Rewrite operation.

For the reread data protection, Bit 2 of Configuration Register 5 can be set to 1 to prevent the data block form being overwritten. In this way, the assertion of A->B full flag will occur when the write pointer meets the reread pointer instead of the read pointer as in the normal definition. For the rewrite data protection, Bit 3 of Configuration Register 5 can be set to 1 to prevent the data block from being read. In this case, the assertion of B->A empty flag will occur when the read pointer meets the rewrite pointer instead of the write pointer.

In conclusion, Bit 2 and 3 of Configuration Register 5 are used to redefine Full & Empty flags for data block partition. Although it can serve the purpose of data protection, the setting of these 2 bits is independent of the functions caused by RER/REW, or LDRER/LDREW assertions.

REREAD OPERATIONS (1,2)

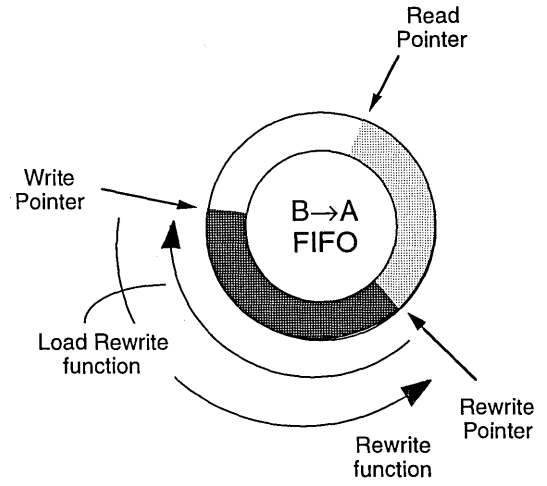


2669 drw 08

NOTES:
1. If bit 2 is set to 1,
   Empty flag asserted if Read = Write
   Full flag asserted if Reread + FIFO size = Write
2. If bit 2 is set to 0,
   Empty flag asserted if Read = Write
   Full flag asserted if Read + FIFO size = Write

Figure 6. BiFIFO Reread Operations

REWRITE OPERATIONS (3,4)



2669 drw 09

NOTES:
1. If bit 3 is set to 1,
   Empty flag asserted if Read = Rewrite
   Full flag asserted if Read + FIFO size = Write
2. If bit 3 is set to 0,
   Empty flag asserted if Read = Write
   Full flag asserted if Read + FIFO size = Write

Figure 7. BiFIFO Rewrite Operations

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2669 tbl 18

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage	2.0	—	—	V
V_{IL}(1)	Input LOW Voltage	—	—	0.8	V

NOTE: 2669 tbl 19

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT72510L IDT72520L Commercial t_A = 25, 35, 50 ns Min.	Typ.	Max.	Unit
I_{IL}(1)	Input Leakage Current (Any Input)	–1	—	1	µA
I_{OL}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -1mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA	—	—	0.4	V
I_{CC1}(3)	Average Vcc Power Supply Current	—	150	220	mA
I_{CC2}(3)	Average Standby Current ($\overline{R}_B$ = $\overline{W}_B$ = $\overline{DS}_A$ = V_{IH})	—	16	30	mA

NOTES: 2669 tbl 20

1. Measurements with 0.4V ≤ VIN ≤ VCC, DSA = DSB ≥ VIH.
2. Measurements with 0.4V ≤ VOUT ≤ VCC, DSA = DSB ≥ VIH.
3. Measurements are made with outputs open. Tested at f = 20 MHz.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 8

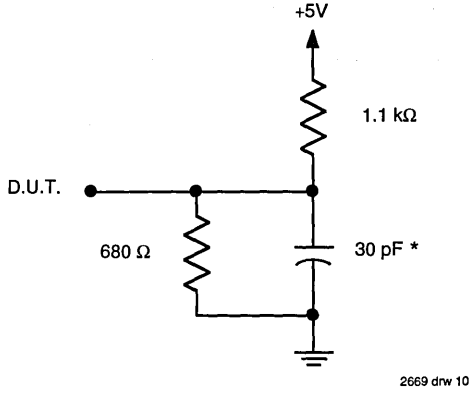
2669 tbl 21

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	12	pF

NOTES: 2669 tbl 22

1. With output deselected.
2. Characterized values, not currently tested.



2669 drw 10

or equivalent circuit

Figure 8. Output Load

* Includes jig and scope capacitances

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Commercial IDT72510L25 IDT72520L25 Min.	Max.	IDT72510L35 IDT72520L35 Min.	Max.	IDT72510L50 IDT72520L50 Min.	Max.	Unit	Timing Figure
RESET TIMING (Port A and Port B)									
t_{RSC}	Reset cycle time	35	—	45	—	65	—	ns	9
t_{RS}	Reset pulse width	25	—	35	—	50	—	ns	9
t_{RSS}	Reset set-up time	25	—	35	—	50	—	ns	9
t_{RSR}	Reset recovery time	10	—	10	—	15	—	ns	9
t_{RSF}	Flag reset pulse width	—	35	—	45	—	65	ns	9
PORT A TIMING									
t_{aA}	Port A access time	—	25	—	35	—	50	ns	12, 14, 15
t_{aLZ}	Read or write pulse LOW to data bus at Low-Z	5	—	5	—	5	—	ns	12, 15, 16
t_{aHZ}	Read or write pulse HIGH to data bus at High-Z	—	15	—	20	—	30	ns	12, 14, 15, 16
t_{aDV}	Data valid from read pulse HIGH	5	—	5	—	5	—	ns	12, 14, 16
t_{aRC}	Read cycle time	35	—	45	—	65	—	ns	12
t_{aRPW}	Read pulse width	25	—	35	—	50	—	ns	12, 14, 15
t_{aRR}	Read recovery time	10	—	10	—	15	—	ns	12
t_{aS}	$\overline{CS}_A$, A_0, A_1, $R/\overline{W}_A$ set-up time	5	—	5	—	5	—	ns	10, 12, 16
t_{aH}	$\overline{CS}_A$, A_0, A_1, $R/\overline{W}_A$ hold time	5	—	5	—	5	—	ns	10, 12
t_{aDS}	Data set-up time	15	—	18	—	30	—	ns	11, 12, 14, 15
t_{aDH} (1)	Data hold time	0	—	0	—	5	—	ns	11, 12, 14, 15
t_{aWC}	Write cycle time	35	—	45	—	65	—	ns	12
t_{aWPW}	Write pulse width	25	—	35	—	50	—	ns	11, 12, 14
t_{aWR}	Write recovery time	10	—	10	—	15	—	ns	12
t_{aWRCOM}	Write recovery time after a command	25	—	35	—	50	—	ns	11

NOTE:

2669 tbl 23

1. The minimum data hold time is 5ns (10ns for the 80ns speed grade) when writing to the Command or Configuration registers.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Commercial						Unit	Timing Figure
		IDT72510L25 IDT72520L25		IDT72510L35 IDT72520L35		IDT72510L50 IDT72520L50			
		Min.	Max.	Min.	Max.	Min.	Max.		
PORT B PROCESSOR INTERFACE TIMING									
t_{bA1}	Port B access time with no parity	—	25	—	35	—	50	ns	13, 14, 15
t_{bA2}	Port B access time with parity	—	30	—	42	—	60	ns	13, 14, 15
t_{bLZ}	Read or write pulse LOW to data bus at Low-Z	5	—	5	—	5	—	ns	13, 14, 15
t_{bHZ}	Read or write pulse HIGH to data bus at High-Z	—	15	—	20	—	30	ns	13, 14, 15
t_{bDV}	Data valid from read pulse HIGH	5	—	5	—	5	—	ns	13, 14, 15, 16
t_{bRC}	Read cycle time	35	—	45	—	65	—	ns	13
t_{bRPW}	Read pulse width	25	—	35	—	50	—	ns	13
t_{bRR}	Read recovery time	10	—	10	—	15	—	ns	13
t_{bS}	R/$\overline{W}_B$ set-up time	5	—	5	—	5	—	ns	13
t_{bH}	R/$\overline{W}_B$ hold time	5	—	5	—	5	—	ns	13
t_{bDS1}	Data set-up time with no parity	15	—	18	—	30	—	ns	13, 14, 15
t_{bDH1}	Data hold time with no parity	0	—	0	—	5	—	ns	13, 14, 15
t_{bDS2}	Data set-up time with parity	18	—	22	—	35	—	ns	13, 14, 15
t_{bDH2}	Data hold time with parity	0	—	0	—	5	—	ns	13, 14, 15
t_{bWC}	Write cycle time	35	—	45	—	65	—	ns	13
t_{bWPW}	Write pulse width	25	—	35	—	50	—	ns	13, 15
t_{bWR}	Write recovery time	10	—	10	—	15	—	ns	13
PORT B PERIPHERAL INTERFACE TIMING									
t_{bA1}	Port B access time with no parity	—	25	—	40	—	55	ns	17
t_{bA2}	Port B access time with parity	—	30	—	42	—	60	ns	17
t_{bCKC}	Clock cycle time	15	—	20	—	25	—	ns	17
t_{bCKH}	Clock pulse HIGH time	6	—	6	—	10	—	ns	17
t_{bCKL}	Clock pulse LOW time	6	—	6	—	10	—	ns	17
t_{bREQS}	Request set-up time	5	—	5	—	10	—	ns	17
t_{bREQH}	Request hold time	5	—	5	—	5	—	ns	17
t_{bACKL}	Delay from a rising clock edge to ACK switching	—	15	—	18	—	25	ns	17

2669 tbl 24

5

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Commercial						Unit	Timing Figure
		IDT72510L25 IDT72520L25		IDT72510L35 IDT72520L35		IDT72510L50 IDT72520L50			
		Min.	Max.	Min.	Max.	Min.	Max.		
PORT B RETRANSMIT and PARITY TIMING									
t_{DSBH}	$\overline{RER}$, $\overline{REW}$, LDRER, LDREW set-up and recovery time	10	—	10	—	15	—	ns	9, 18
t_{PER}	Parity error time	20	—	25	—	30	—	ns	19
BYPASS TIMING									
t_{BYA}	Bypass access time	—	15	—	20	—	30	ns	16
t_{BYD}	Bypass delay	—	10	—	15	—	20	ns	16
t_{ABYDV}	Bypass data valid time from $\overline{DS}_A$	15	—	15	—	15	—	ns	16
t_{BBYDV} (3)	Bypass data valid time from $\overline{DS}_B$	3	—	3	—	3	—	ns	16
FLAG TIMING									
t_{REF}	Read clock edge to Empty Flag asserted	—	25	—	35	—	45	ns	14, 15, 20, 22
t_{WEF}	Write clock edge to Empty Flag not asserted	—	25	—	35	—	45	ns	14, 15, 20, 22
t_{RFF}	Read clock edge to Full Flag not asserted	—	25	—	35	—	45	ns	14, 15, 21, 23
t_{WFF}	Write clock edge to Full Flag asserted	—	25	—	35	—	45	ns	14, 15, 21, 23
t_{RAEF}	Read clock edge to Almost-Empty Flag asserted	—	40	—	50	—	60	ns	20, 22
t_{WAEF}	Write clock edge to Almost-Empty Flag not asserted	—	40	—	50	—	60	ns	20, 22
t_{RAFF}	Read clock edge to Almost-Full Flag not asserted	—	40	—	50	—	60	ns	21, 23
t_{WAFF}	Write clock edge to Almost-Full Flag asserted	—	40	—	50	—	60	ns	21, 23

NOTES:

2669 tbl 25

1. Read and Write are internal signals derived from $\overline{DS}_A$, $R/\overline{W}_A$, $\overline{DS}_B$, $R/\overline{W}_B$, $\overline{R}_B$, and $\overline{W}_B$.
2. Although the flags, Empty, Almost-Empty, Almost-Full, and Full Flags are internal flags, the timing given is for those assigned to external pins.
3. Values guaranteed by design, not currently tested.

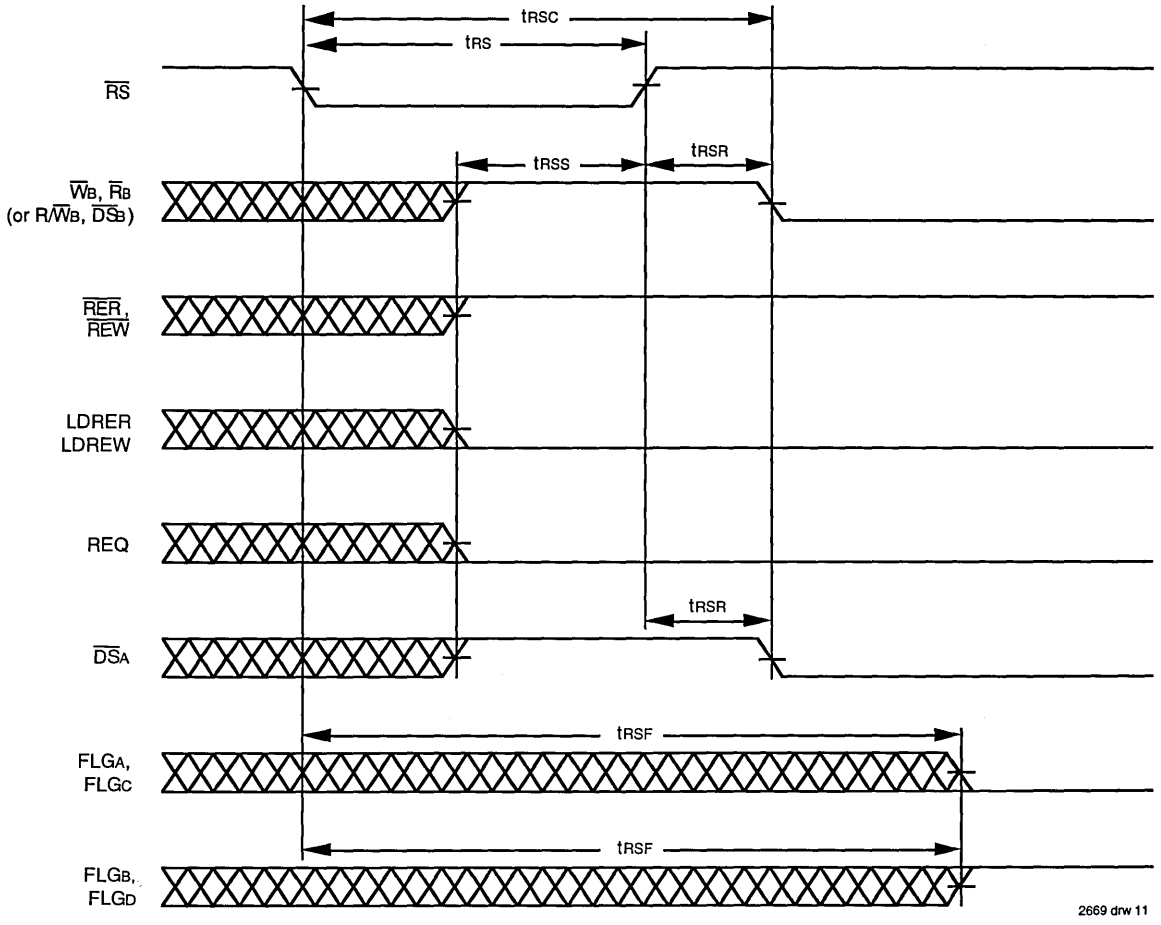


Figure 9. Hardware Reset Timing for IDT72510/520

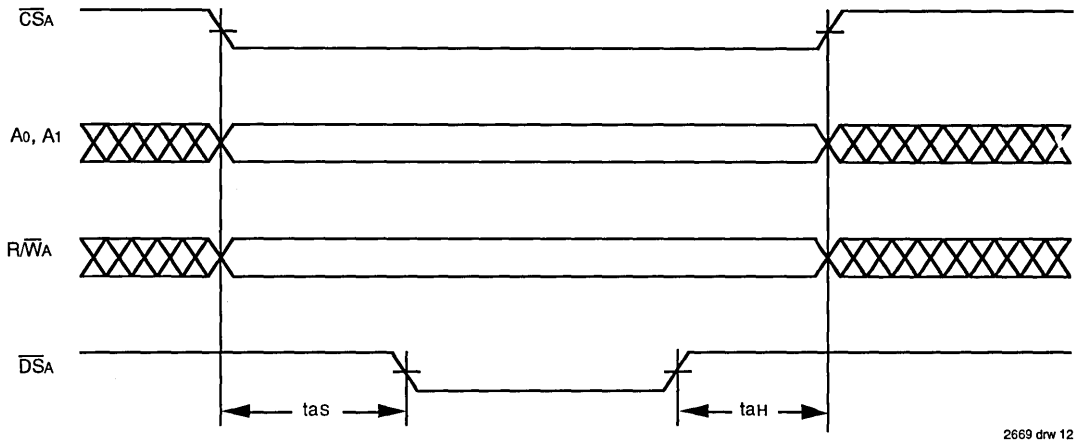


Figure 10. Basic Port A Control Signal Timing (Applies to All Port A Timing)

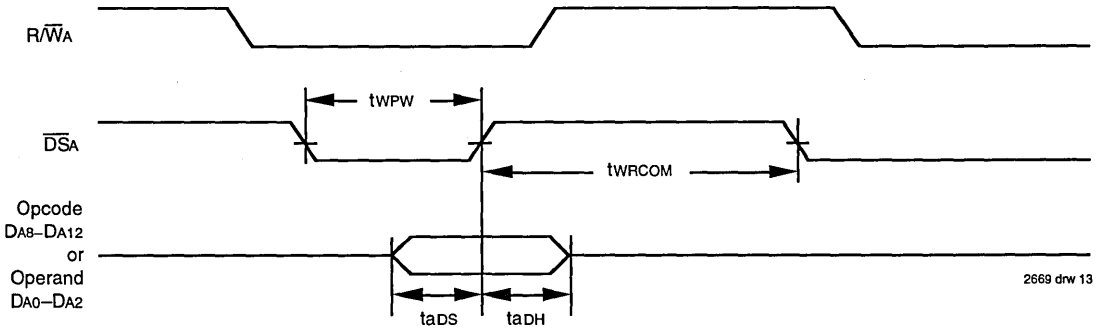
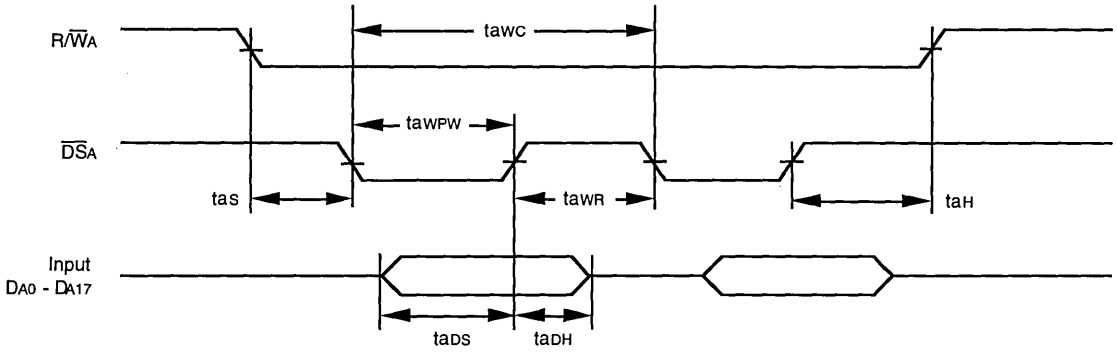


Figure 11. Port A Command Timing (Write)

WRITE



READ

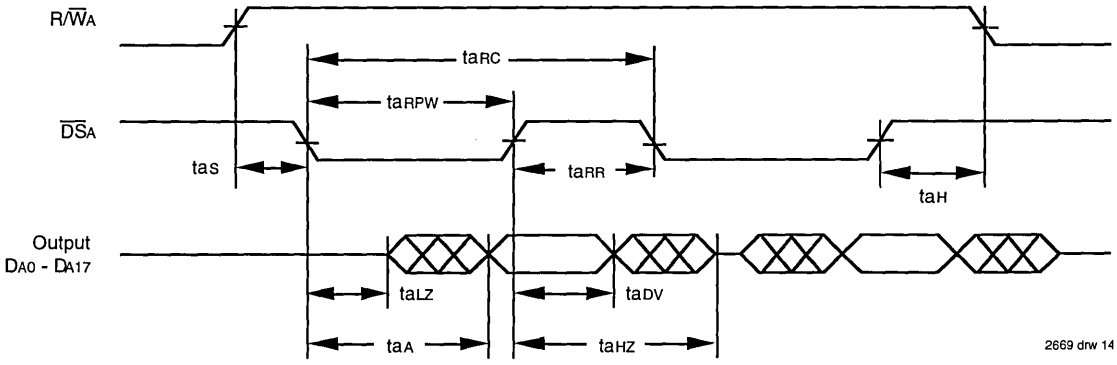
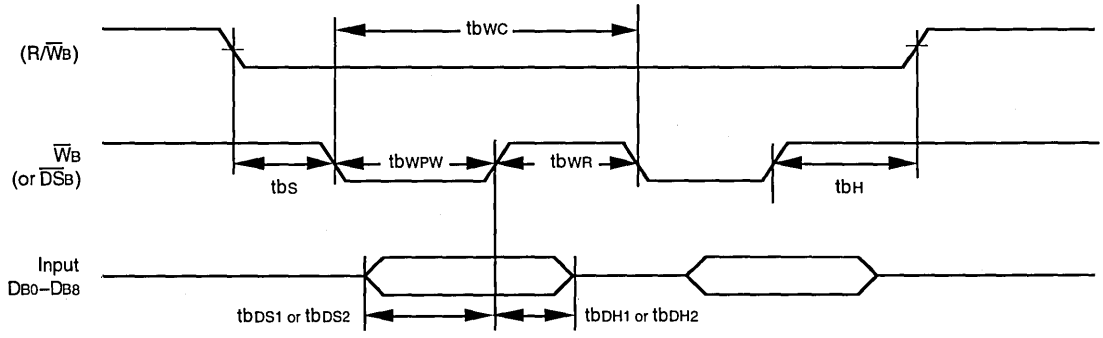
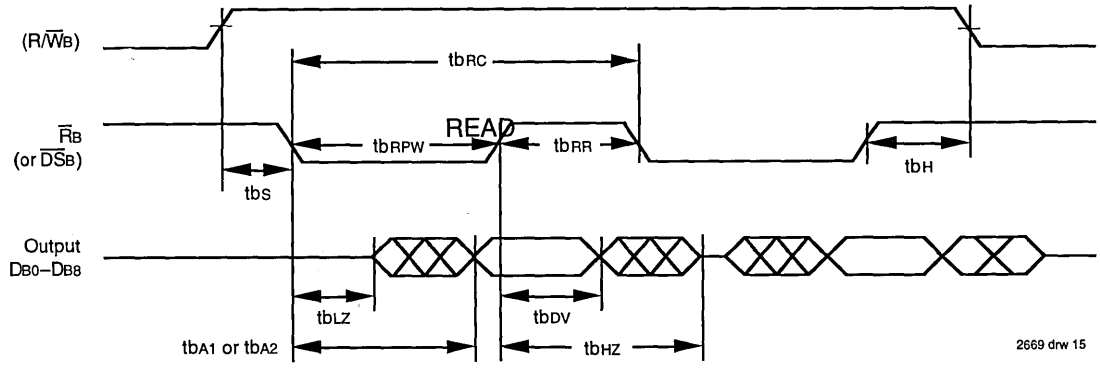


Figure 12. Read and Write Timing for Port A

WRITE



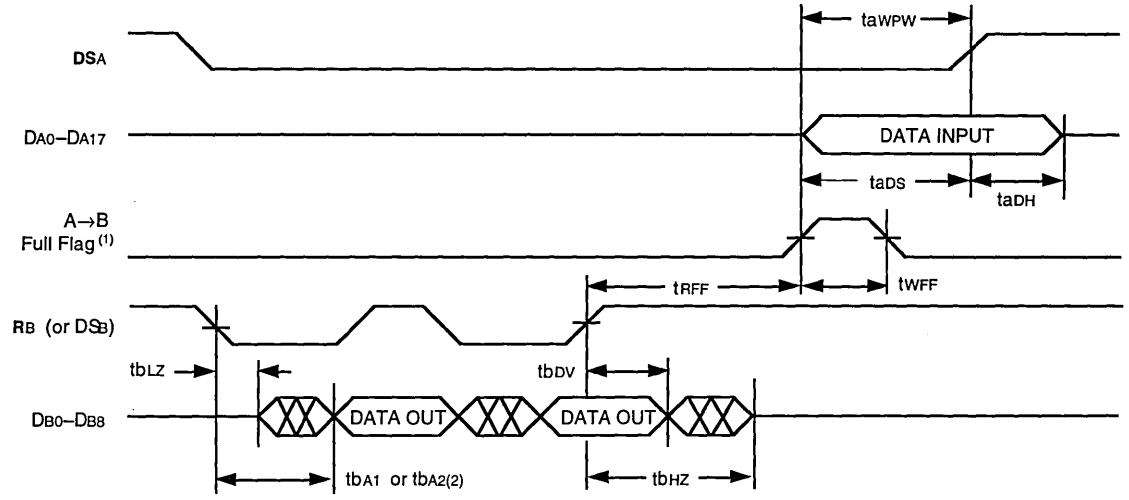
NOTES:
1. tbDS1 and tbDH1 are with parity checking or if parity is ignored, tbDS2 and tbDH2 are with parity generation.
2. RB = 1



NOTES:
1. tbA1 is with parity checking or if parity is ignored, tbA2 is with parity generation.
2. RB = 1

Figure 13. Port B Read and Write Timing. Processor Interface Mode Only

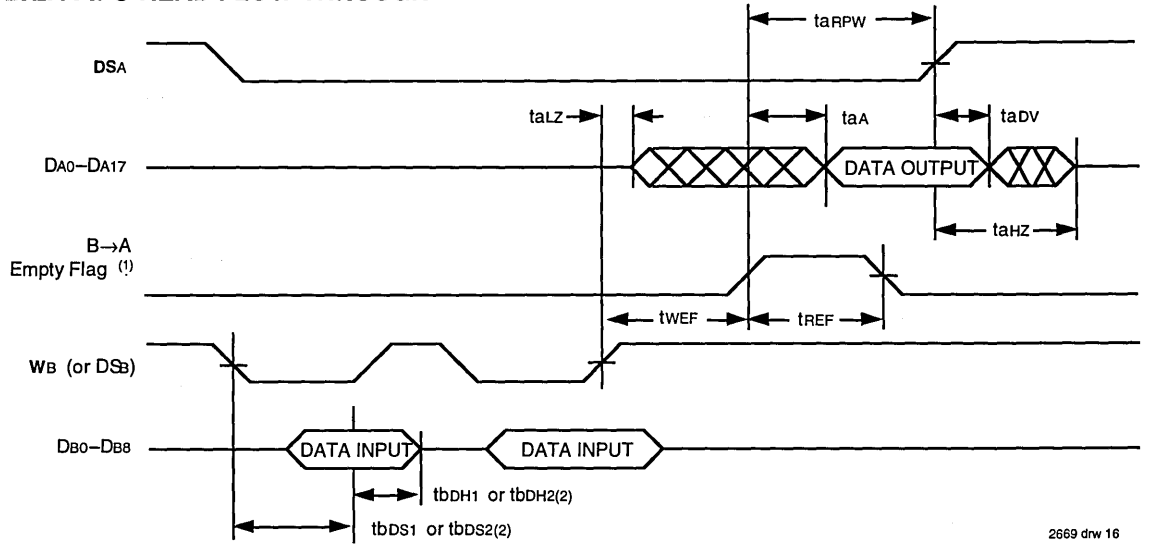
AÆB FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. tbA1 is with parity checking or if parity is ignored, tbA2 is with parity generation.
3. R/WA = 0

5

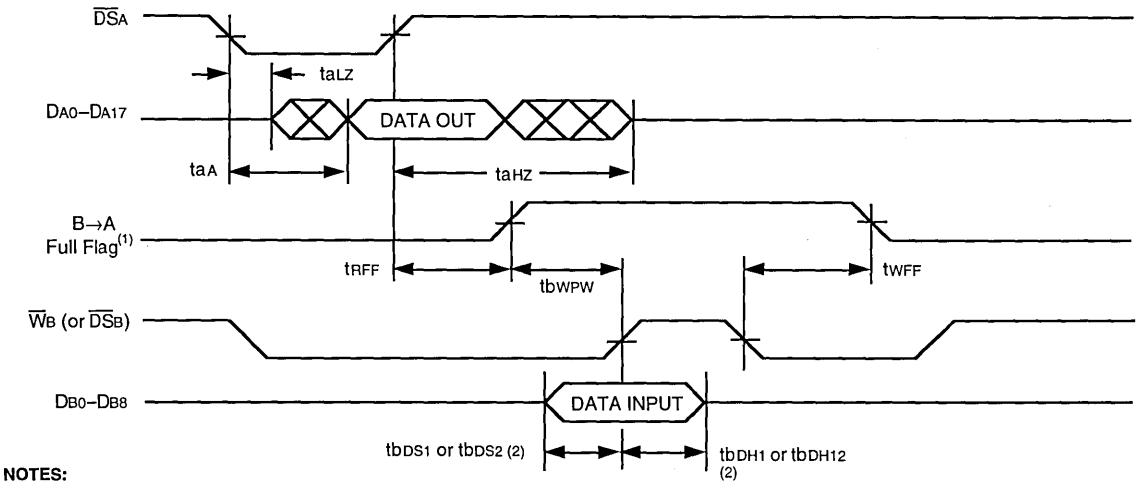
BÆA FIFO READ FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. tbDS1 & tbDH1 are with parity checking or if parity is ignored, tbDS2 & tbDH2 is with parity generation.
3. R/WA = 1

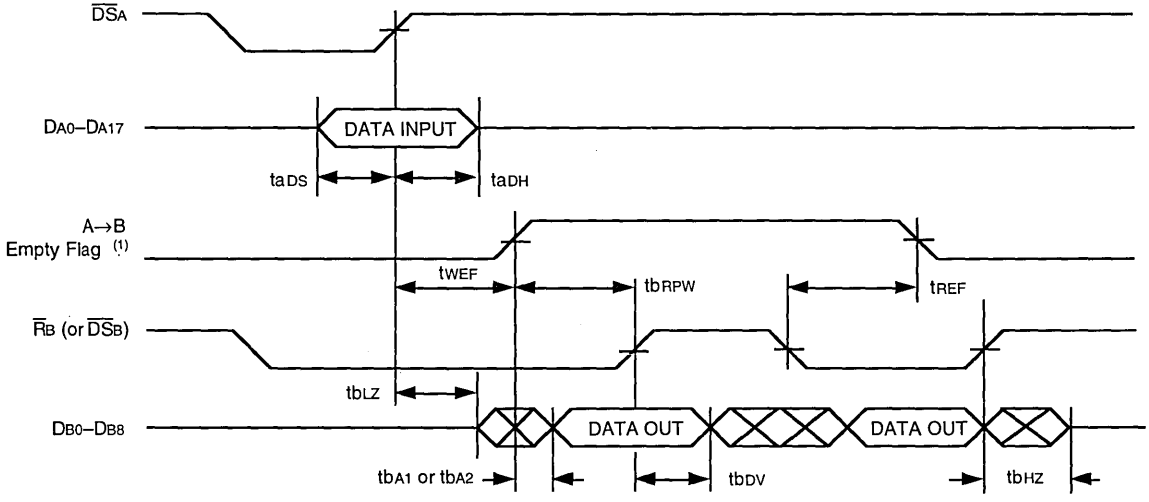
Figure 14. Port A Read and Write Flow-Through Timing. Processor Interface Mode Only

BÆA FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. tbDS1 & tbDH1 are with parity checking or if parity is ignored, tbDS2 & tbDH2 are with parity generation.
3. R/WA = 1

AÆB FIFO READ FLOW-THROUGH

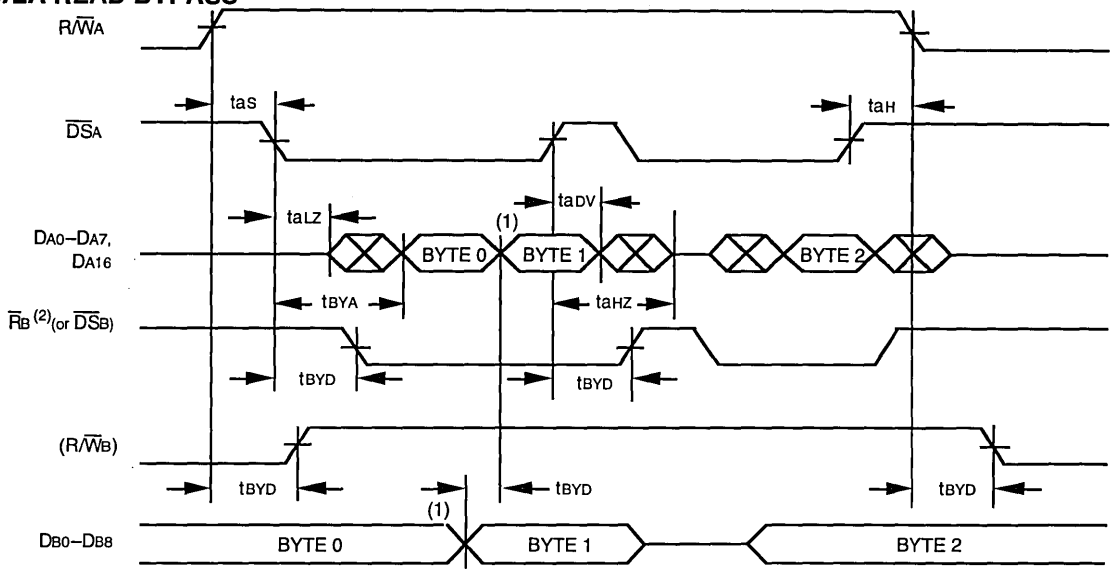


NOTES:
1. Assume the flag pin is programmed active LOW.
2. tbA1 is with parity checking or if parity is ignored, tbA2 is with parity generation.
3. R/WA = 0

2669 drw 17

Figure 15. Port B Read and Write Flow-Through Timing

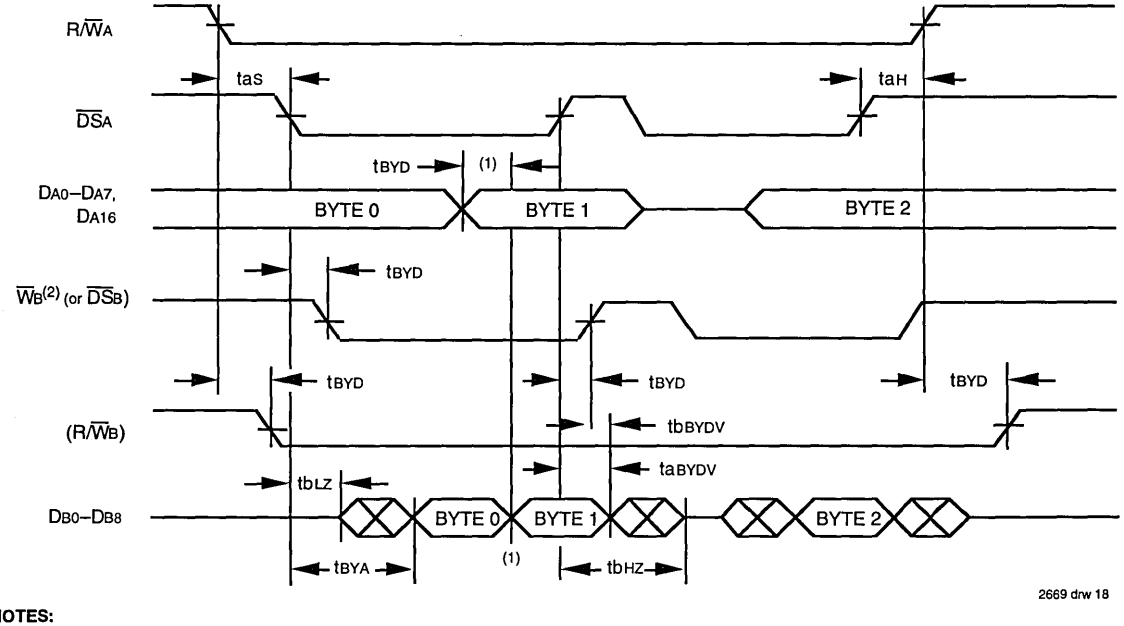
BÆA READ BYPASS



NOTES:
1. Once the bypass starts, any data changes on Port B bus (Byte 0 ÆByte 1) will be passed to Port A bus.
2. WB = 1.

5

AÆB WRITE BYPASS

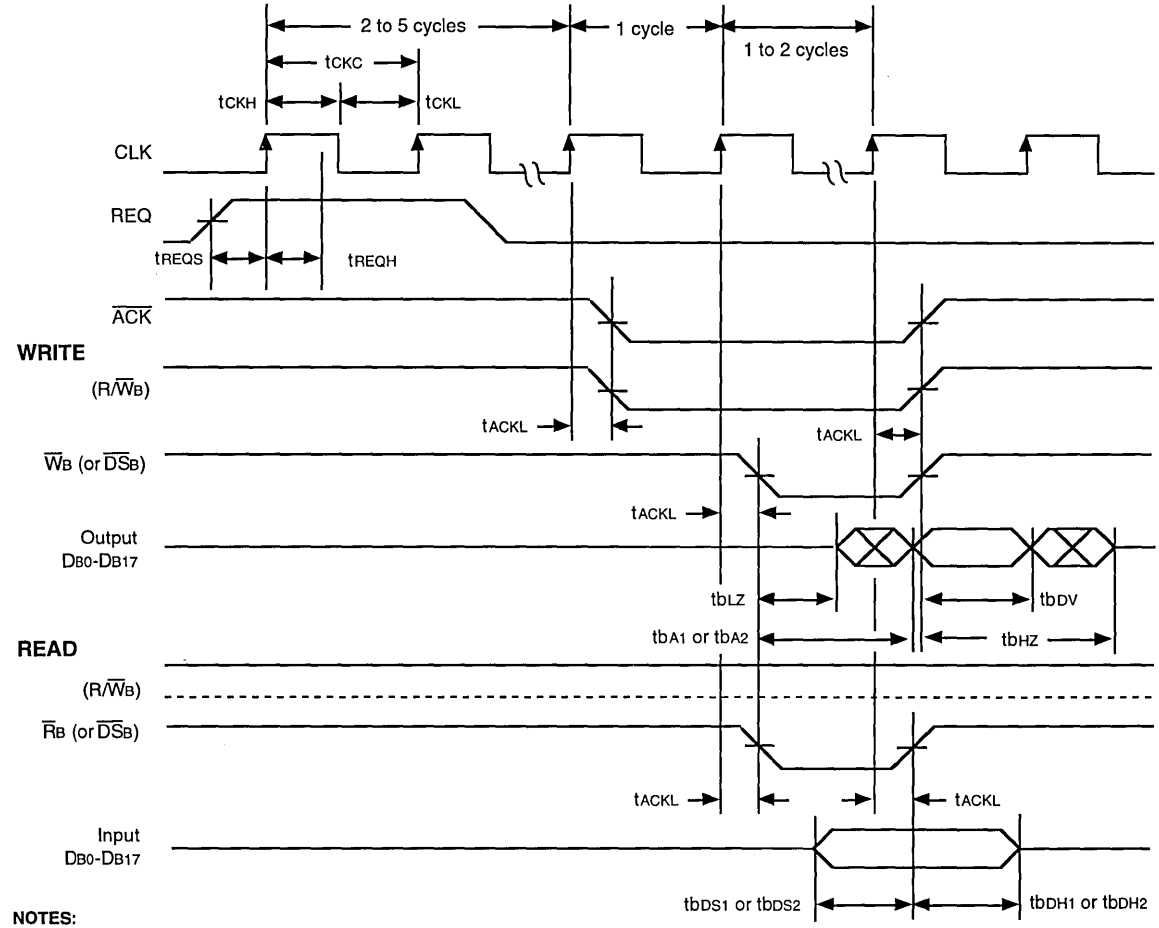


2669 drw 18

NOTES:
1. Once the bypass starts, any data changes on Port A bus (Byte 0 ÆByte 1) will be passed to Port B bus.
2. RB = 1.

Figure 16. Bypass Path Timing. BiFIFO Must be in Peripheral Interface Mode

SINGLE WORD DMA TRANSFER



NOTES:
1. tbA1, tbDS1 and tbDH1 are with parity checking or if parity is ignored, tbA2 & tbDS2 and tbDH2 are with parity.

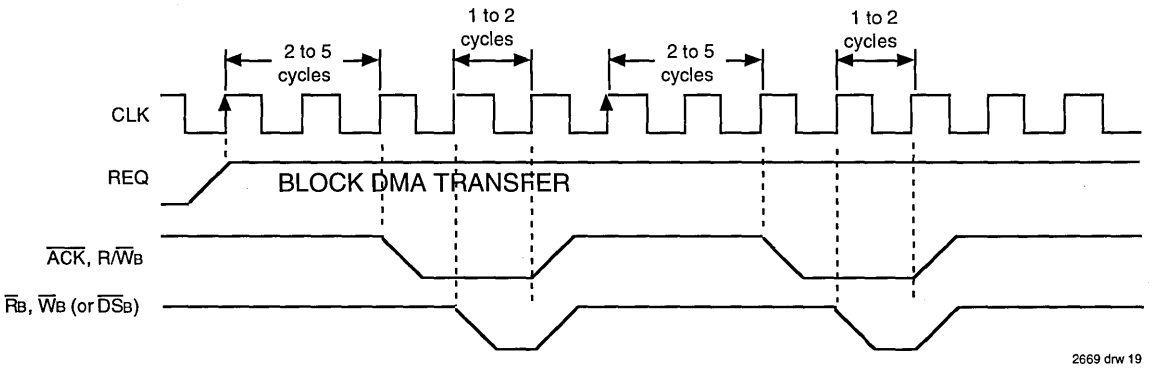


Figure 17. Port B Read and Write DMA Timing. Peripheral Interface Mode Only

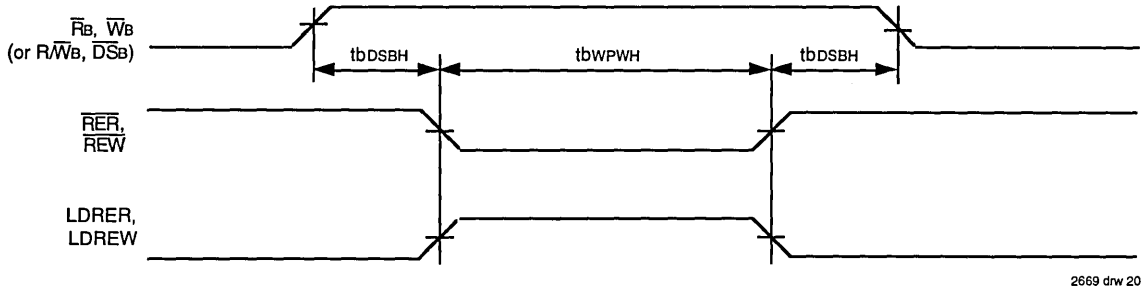
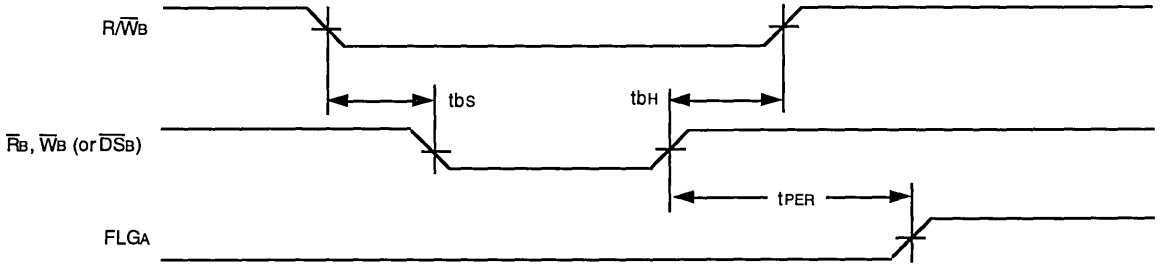
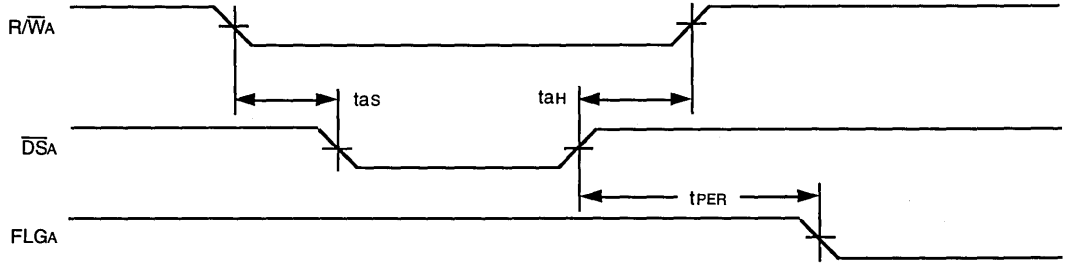


Figure 18. Port B Reread and Rewrite Timing for Intelligent Retransmit

SET PARITY ERROR: FLGA IS ASSIGNED AS THE PARITY ERROR PIN



CLEAR PARITY ERROR: COMMAND WRITTEN INTO PORT A CLEARS PARITY ERROR ON FLGA PIN



NOTE:
1. FLGA is the only pin that can be assigned as a parity error output.

Figure 19. Port B Parity Error Timing

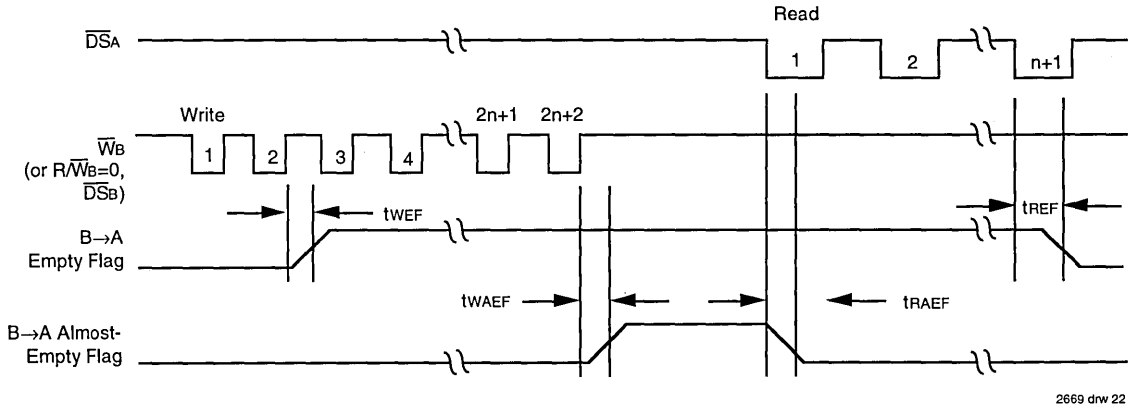


Figure 20. Empty and Almost-Empty Flag Timing for BÆA FIFO. (n = Programmed Offset)

NOTES:
1. BÆA FIFO is initially empty.
2. Assume the flag pins are programmed active LOW.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/WA = 1

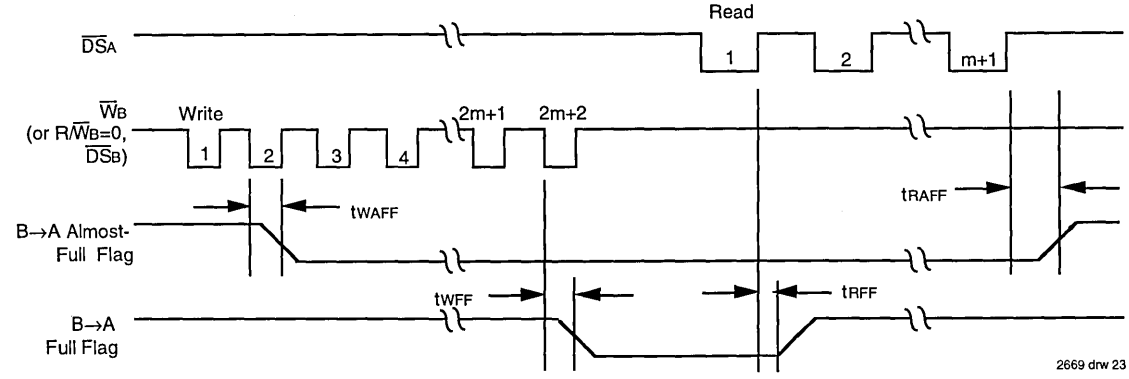


Figure 21. Full and Almost-Full Flag Timing for BÆA FIFO. (m = Programmed Offset)

NOTES:
1. BÆA FIFO initially contains D–(M+1) data words. D = 512 for IDT 72510; D = 1024 for IDT72520.
2. Assume the flag pins are programmed active LOW.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/WA = 1

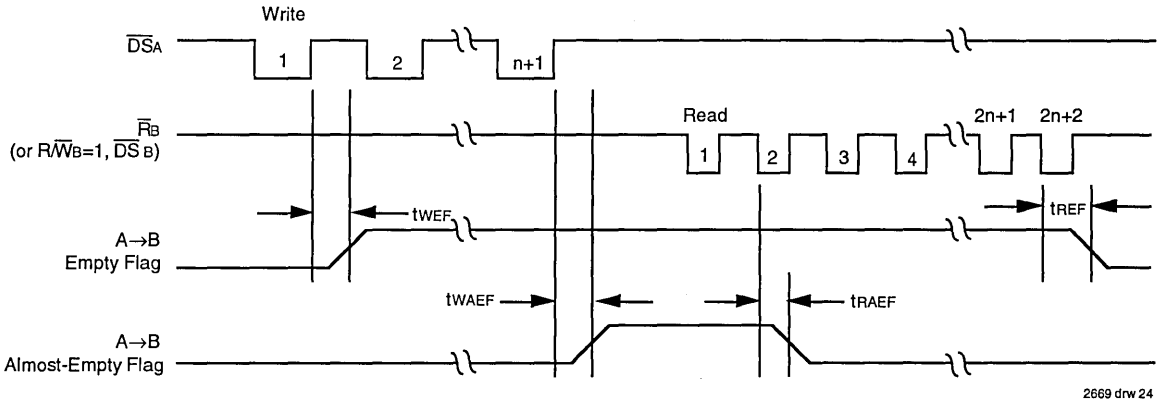


Figure 22. Empty and Almost-Empty Flag Timing for AÆB FIFO. (n = Programmed Offset)

NOTES:
1. AÆB FIFO is initially empty.
2. Assume the flag pins are programmed active LOW.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/WA = 1

5

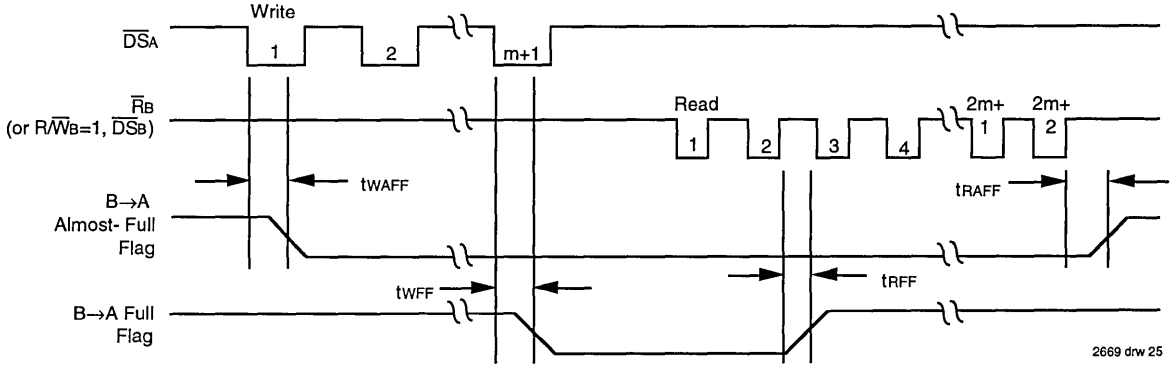
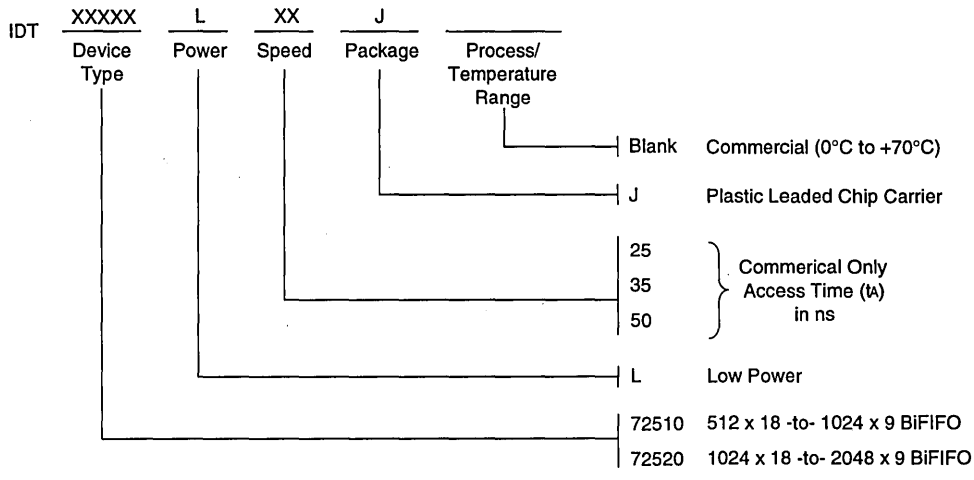


Figure 23. Full and Almost-Full Flag Timing for AÆB FIFO. (m = Programmed Offset)

NOTES:
1. AÆB FIFO initially contains D–(M+1) data words. D = 512 for IDT 72510; D = 1024 for IDT72520.
2. Assume the flag pins are programmed active LOW.
3. For stand-alone mode only; in a 36- to 9-bit configuration, Port B reads must be doubled.
4. R/WA = 0


IDT
XXXXX
Device Type
L
Power
XX
Speed
J
Package
Process/ Temperature Range
Blank
Commercial (0°C to +70°C)
J
Plastic Leaded Chip Carrier
25
35
50
Commerical Only Access Time (tA) in ns
L
Low Power
72510
512 x 18 -to- 1024 x 9 BiFIFO
72520
1024 x 18 -to- 2048 x 9 BiFIFO

2669 drw 26

Integrated Device Technology, Inc.

PARALLEL BIDIRECTIONAL FIFO 512 x 18 & 1024 x 18

IDT72511
IDT72521

FEATURES:

- Two side-by-side FIFO memory arrays for bidirectional data transfers
- 512 x 18-Bit - 512 x 18-Bit (IDT72511)
- 1024 x 18-Bit - 1024 x 18-Bit (IDT72521)
- 18-bit data buses on Port A side and Port B side
- Can be configured for 18-to-18-bit or 36-to-36-bit communication
- Fast 35ns access time
- Fully programmable standard microprocessor interface
- Built-in bypass path for direct data transfer between two ports
- Two fixed flags, Empty and Full, for both the A-to-B and the B-to-A FIFO
- Two programmable flags, Almost-Empty and Almost-Full for each FIFO
- Programmable flag offset can be set to any depth in the FIFO
- Any of the eight flags can be assigned to four external flag pins
- Flexible reread/rewrite capabilities
- Six general-purpose programmable I/O pins
- Standard DMA control pins for data exchange with peripherals
- 68-pin PGA and PLCC packages

DESCRIPTION:

The IDT72511 and IDT72521 are highly integrated first-in, first-out memories that enhance processor-to-processor and processor-to-peripheral communications. IDT BiFIFOs integrate two side-by-side memory arrays for data transfers in two directions.

The BiFIFOs have two ports, A and B, that both have standard microprocessor interfaces. All BiFIFO operations are controlled from the 18-bit wide Port A. Port B is also 18 bits wide and can be connected to another processor or a peripheral controller. The BiFIFOs have a 9-bit bypass path that allows the device connected to Port A to pass messages directly to the Port B device.

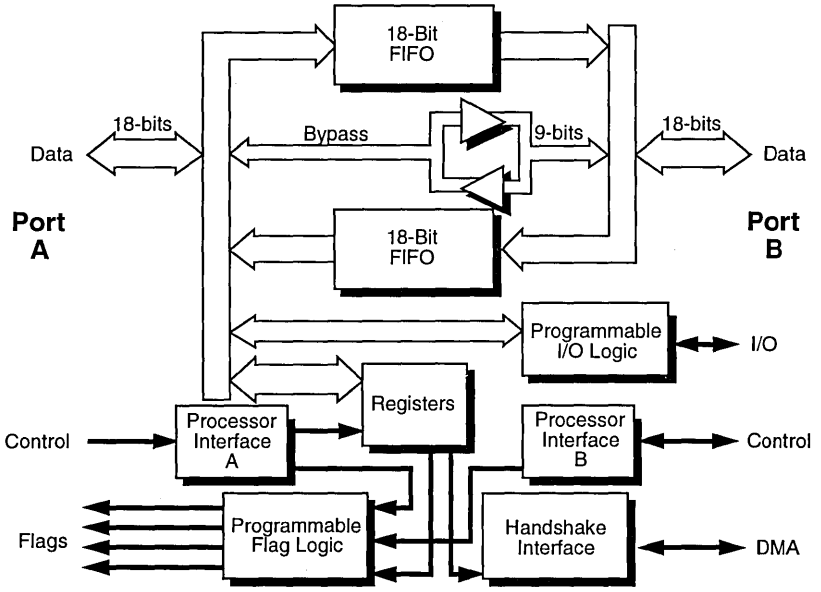
Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

The IDT BiFIFO has programmable flags. Each FIFO memory array has four internal flags, Empty, Almost-Empty, Almost-Full and Full, for a total of eight internal flags. The Almost-Empty and Almost-Full flag offsets can be set to any depth through the Configuration Registers. These eight internal flags can be assigned to any of four external flag pins (FLGA-FLGD) through one Configuration Register.

Port B has programmable I/O, reread/rewrite and DMA functions. Six programmable I/O pins are manipulated through

5

SIMPLIFIED BLOCK DIAGRAM

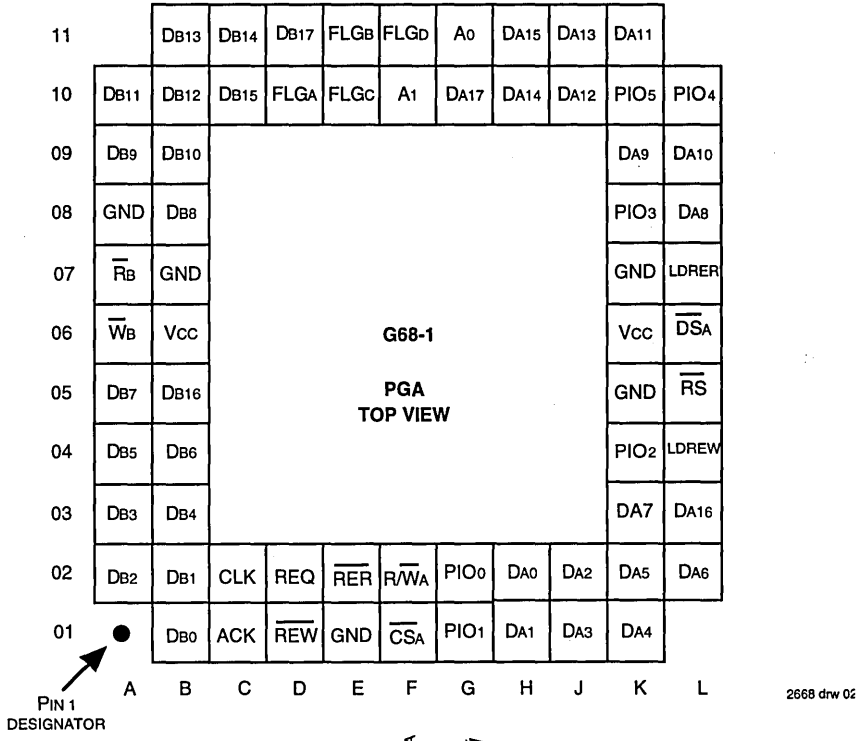


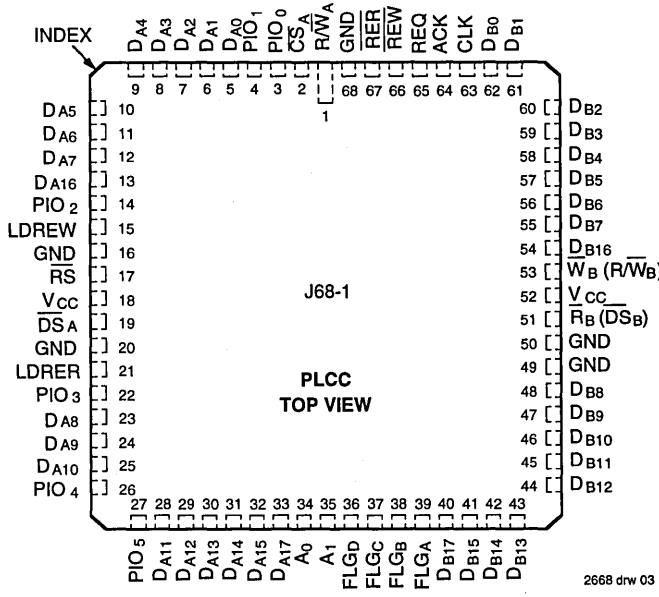
2668 drw 01

The IDT logo is a registered trademark of Integrated Device Techology, Inc.

two Configuration Registers. The Reread and Rewrite controls will read or write Port B data blocks multiple times. The BiFIFO has three pins, REQ, ACK and CLK, to control DMA transfers from Port B devices.

PIN CONFIGURATIONS





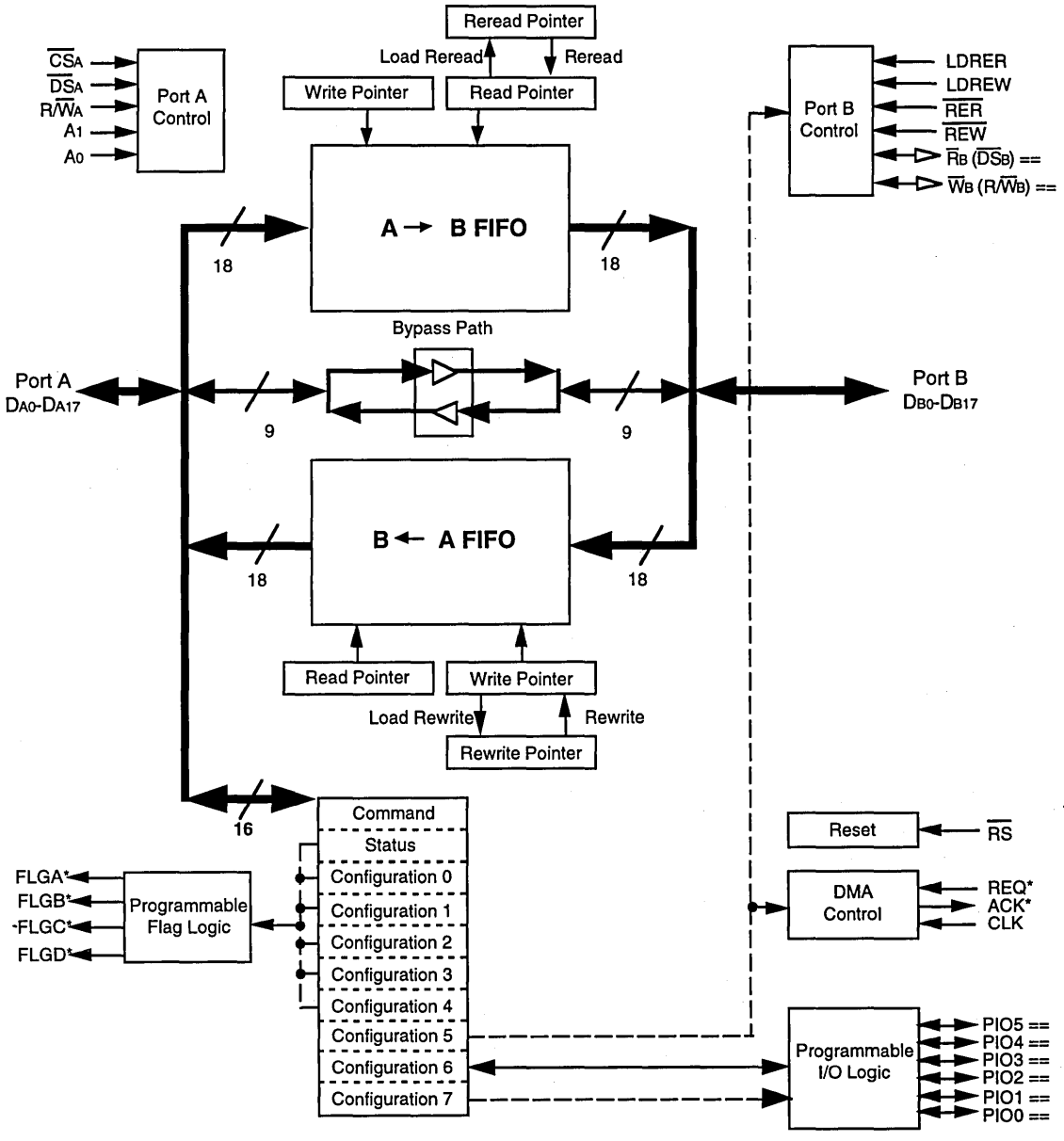
PIN DESCRIPTION

Symbol	Name	I/O	Description
D_{A0}-D_{A17}	Data A	I/O	Data inputs and outputs for the 18-bit Port A bus.
$\overline{CS}_A$	Chip Select A	I	Port A is accessed when Chip Select A is LOW.
$\overline{DS}_A$	Data Strobe A	I	Data is written into Port A on the rising edge of Data Strobe when Chip Select is LOW. Data is read out of Port A on the falling edge of Data Strobe when Chip Select is LOW.
R/$\overline{W}_A$	Read/Write A	I	This pin controls the read or write direction of Port A. When $\overline{CS}_A$ is LOW and R/$\overline{W}_A$ is HIGH, data is read from Port A on the falling edge of $\overline{DS}_A$. When $\overline{CS}_A$ is LOW and R/$\overline{W}_A$ is LOW, data is written into Port A on the rising edge of $\overline{DS}_A$.
A_0, A_1	Addresses	I	When Chip Select A is asserted, A_0, A_1, and Read/Write A are used to select one of six internal resources.
D_{B0}-D_{B17}	Data B	I/O	Data inputs and outputs for the 18-bit Port B bus.
$\overline{R}_B$ ($\overline{DS}_B$)	Read B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{R}_B$) or as part of a Motorola-style interface ($\overline{DS}_B$). As an Intel-style interface, data is read from Port B on a falling edge of $\overline{R}_B$. As a Motorola-style interface, data is read on the falling edge of $\overline{DS}_B$ or written on the rising edge of $\overline{DS}_B$ through Port B. The default is Intel-style processor mode. ($\overline{R}_B$ as an input).
$\overline{W}_B$ (R/$\overline{W}_B$)	Write B	I or O	If Port B is programmed to processor mode, this pin functions as an input. If Port B is programmed to peripheral mode this pin functions as an output. This pin can function as part of an Intel-style interface ($\overline{W}_B$) or as part of a Motorola-style interface (R/$\overline{W}_B$). As an Intel-style interface, data is written to Port B on a rising edge of $\overline{W}_B$. As a Motorola-style interface, data is read (R/$\overline{W}_B$ = HIGH) or written (R/$\overline{W}_B$ = LOW) to Port B in conjunction with a Data Strobe B falling or rising edge. The default is Intel-style processor mode ($\overline{W}_B$ as an input.)
$\overline{RER}$	Reread	I	Loads A→B FIFO Read Pointer with the value of the Reread Pointer when LOW.
$\overline{REW}$	Rewrite	I	Loads B→A FIFO Write Pointer with the value of the Rewrite Pointer when LOW.
LDRER	Load Reread	I	Loads the Reread Pointer with the value of the A→B FIFO Read Pointer when HIGH.
LDREW	Load Rewrite	I	Loads the Rewrite Pointer with the value of the B→A FIFO Write Pointer when HIGH.
REQ	Request	I	When Port B is programmed in peripheral mode, asserting this pin begins a data transfer. Request can be programmed either active HIGH or active LOW.
ACK	Acknowledge	O	When Port B is programmed in peripheral mode, Acknowledge is asserted in response to a Request signal. This confirms that a data transfer may begin. Acknowledge can be programmed either active HIGH or active LOW.
CLK	Clock	I	This pin is used to generate timing for ACK, $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and R/$\overline{W}_B$ when Port B is in the peripheral mode.
FLG_A-FLG_D	Flags	O	These four outputs pins can be assigned any one of the eight internal flags in the BiFIFO. Each of the two internal FIFOs (A→B and B→A) has four internal flags: Empty, Almost-Empty, Almost-Full and Full.
PIO_0-PIO_5	Programmable Inputs/ Outputs	I/O	Six general purpose I/O pins. The input or output direction of each pin can be set independently.
$\overline{RS}$	Reset	I	A LOW on this pin will perform a reset of all BiFIFO functions.
V_{CC}	Power		There are two +5V power pins.
GND	Ground		There are five Ground pins at 0V.

2668 tbl 01

5

DETAILED BLOCK DIAGRAM



NOTES:

2668 drw 04

(*) Can be programmed either active high or active low in internal configuration registerers.

(††) Can be programmed through an internal configuration register to be either an input or an output.

FUNCTIONAL DESCRIPTION

IDT's BiFIFO family is versatile for both multiprocessor and peripheral applications. Data can be sent through both FIFO memories concurrently, thus freeing both processors from laborious direct memory access (DMA) protocols and frequent interrupts.

Two full 18-bit wide FIFOs are integrated into the IDT BiFIFO, making simultaneous data exchange possible. Each FIFO is monitored by separate internal read and write pointers, so communication is not only bidirectional, it is also totally independent in each direction. The processor connected to Port A of the BiFIFO can send or receive messages directly to the Port B device using the BiFIFO's 9-bit bypass path.

The BiFIFO can be used in different bus configurations: 18 bits to 18 bits and 36 bits to 36 bits. One BiFIFO can be used for the 18- to 18-bit configuration, and two BiFIFOs are required for 36- to 36-bit configuration. This configuration can be extended to wider bus widths (54- to 54-bits, 72- to 72-bits, ...) by adding more BiFIFOs to the configuration.

The microprocessor or microcontroller connected to Port A controls all operations of the BiFIFO. Thus, all Port A interface pins are inputs driven by the controlling processor. Port B can be programmed to interface either with a second processor or a peripheral device. When Port B is programmed in processor interface mode, the Port B interface pins are inputs driven by the second processor. If a peripheral device is connected to the BiFIFO, Port B is programmed to peripheral interface mode and the interface pins are outputs.

18- to 18-bit Configurations

A single BiFIFO can be configured to connect an 18-bit processor to another 18-bit processor or an 18-bit peripheral. The upper BiFIFO shown in each of the Figures 1 and 2 can be used in 18- to 18-bit configurations for processor and peripheral interface modes respectively.

36- to 36-bit Configurations

In a 36- to 36-bit configuration, two BiFIFOs operate in parallel. Both BiFIFOs are programmed simultaneously, 18 data bits to each device. Figures 1 and 2 show multiple BiFIFOs configured for processor and peripheral interface modes respectively.

Processor Interface Mode

When a microprocessor or microcontroller is connected to Port B, all BiFIFOs in the configuration must be programmed to processor interface mode. In this mode, all Port B interface controls are inputs. Both REQ and CLK pins should be pulled LOW to ensure that the setup and hold time requirements for these pins are met during reset. Figure 1 shows the BiFIFO in processor interface mode.

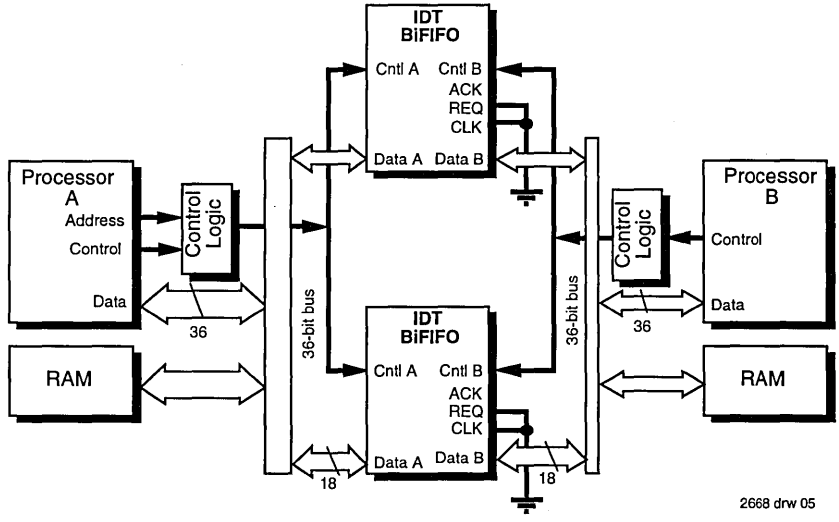


Figure 1. 36-Bit Processor to 36-Bit Processor Configuration

NOTE:

1. 36- to 36-bit processor interface configuration. Upper BiFIFO only is used in 18- to 18-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, R/$\overline{W}_A$, and $\overline{DS}_A$; *Cntl B* refers to R/$\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

Peripheral Interface Mode

If Port B is connected to a peripheral controller, all BiFIFOs in the configuration must be programmed in peripheral interface mode. In this mode, all the Port B interface pins are all outputs. To assure fixed high states for $\overline{R}_B$ and $\overline{W}_B$ before they are programmed into an output, these two pins should be pulled up to Vcc with 10K resistors. Of course, only one set of Port B interface pins should be used to control a single peripheral device, while the other interface pins are all ignored. Figure 2 shows a BiFIFO configuration connected to a peripheral.

Port A Interface

The BiFIFO is straightforward to use in microprocessor-based systems because each BiFIFO port has a standard microprocessor control set. Port A has access to six resources: the A→B FIFO, the B→A FIFO, the 9-bit direct data bus (bypass path), the configuration registers, status and command registers. The Port A Address and Read/Write pins determine the resource being accessed as shown in Table 1. Data Strobe is used to move data in and out of the BiFIFO.

When either of the internal FIFOs are accessed, 18 bits of data are transferred across Port A. Since the bypass path is only 9 bits wide, the least significant byte (D_{A0}-D_{A7}, D_{A16}) is used on Port A. All of the registers are 16 bits wide which means only the data bits (D_{A0}-D_{A15}) are passed by Port A.

Bypass Path

The bypass path acts as a bidirectional bus transceiver directly between Port A and Port B. The direct connection requires that the Port A interface pins are inputs and the Port B interface pins are outputs. The bypass path is 9 bits wide in an 18- to 18-bit configuration or 18 bits wide in a 36- to 36-bit configuration.

During bypass operations, the BiFIFOs must be programmed into peripheral interface mode. Bit 10 of Configuration Register 5 (see Table 10) is set to 1 for peripheral interface mode.

Command Register

Ten registers are accessible through Port A, a Command Register, a Status Register, and eight Configuration Registers.

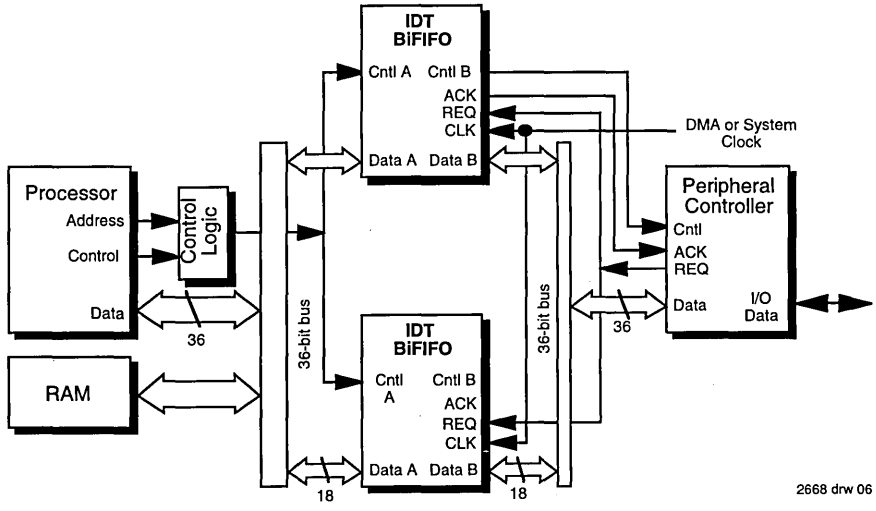


Figure 2. 36-Bit Processor to 36-Bit Peripheral Configuration

NOTE:

1. 36- to 36-bit peripheral interface configuration. Upper BiFIFO only is used in 18- to 18-bit configuration. Note that *Cntl A* refers to $\overline{CS}_A$, A_1, A_0, R/$\overline{W}_A$, and $\overline{DS}_A$; *Cntl B* refers to R/$\overline{W}_B$ and $\overline{DS}_B$ or $\overline{R}_B$ and $\overline{W}_B$.

The Command Register is written by setting $\overline{CS}_A = 0$, $A_1 = 1$, $A_0 = 1$. Commands written into the BiFIFO have a 4-bit opcode (bit8 – bit 11) and a 3-bit operand (bit 0 – bit 2) as shown in Figure 3. The commands can be used to reset the BiFIFO, to select the Configuration Register, to perform intelligent reread/rewrite, to set the Port B DMA direction, to set the Status Register format, and to modify the Port B Read and Write Pointers. The command opcodes are shown in Table 2.

The reset command initializes different portions of the BiFIFO depending on the command operand. Table 3 shows the reset command operands.

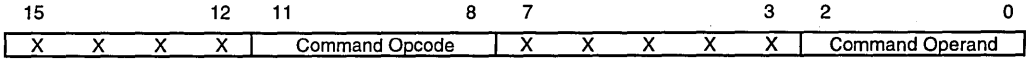
The configuration Register address is set directly by the command operands shown in Table 4.

Intelligent reread/rewrite is performed by interchanging the Port B Read Pointer with the Reread Pointer or by interchanging the Port B Write Pointer with the Rewrite Pointer. No command operands are required to perform a reread/rewrite operation.

When Port B of the BiFIFO is in peripheral mode, the DMA direction is controlled by the Command Register. Table 5 shows the Port B read/write DMA direction operands.

Two commands are provided to increment the Port B Read and Write Pointers. No operands are required for these commands.

COMMAND FORMAT



2668 tbl 02

Figure 3. Format for Commands Written into Port A

5

Reset

The IDT72511 and IDT72521 have a hardware reset pin ($\overline{RS}$) that resets all BiFIFO functions. A hardware reset requires the following four conditions: $\overline{R}_B$ and $\overline{W}_B$ must be HIGH, $\overline{RER}$ and $\overline{REW}$ must be HIGH, LDRER and LDREW must be LOW, and $\overline{DS}_A$ must be HIGH (Figure 9). After a hardware reset, the BiFIFO is in the following state: Configuration Registers 0-3 are **0000H**, Configuration Register 4 is set to **6420H**, and Configuration Registers 5, 6 and 7 are **0000H**. Additionally, all the pointers including the Reread and Rewrite Pointers are set to **0**, the DMA direction is set to B→A write, and the internal DMA request circuitry is cleared (set to its initial state).

A software reset command can reset A→B pointers and the B→A pointers to **0** independently or together. The internal request DMA circuitry can also be reset independently. A software Reset All command resets all the pointers, the DMA request circuitry, and sets all the Configuration Registers to their default condition. Note that a hardware reset is **NOT** the same as a software Reset All command. Table 6 shows the BiFIFO state after the different hardware and software resets

Status Register

The Status Register reports the state of the programmable flags and the DMA read/write direction. The Status Register is read by setting $\overline{CS}_A = 0$, $A_1 = 1$, $A_0 = 1$ (see Table 1). See Table 7 for the Status Register format.

Configuration Registers

The eight Configuration Register formats are shown in

PORT A RESOURCE SELECTION

$\overline{CS}_A$	A_1	A_0	Read	Write
0	0	0	B→A FIFO	A→B FIFO
0	0	1	9-bit Bypass Path	9-bit Bypass Path
0	1	0	Configuration Registers	Configuration Registers
0	1	1	Status Register	Command Register
1	X	X	Disabled	Disabled

2668 tbl 03

Table 1. Accessing Port A Resources Using $\overline{CS}_A$, A_0 and A_1

COMMAND OPERATIONS

Command Opcode	Function
0000	Reset BiFIFO (see Table 3)
0001	Select Configuration Register (see Table 4)
0010	Load Reread Pointer with Read Pointer Value
0011	Load Rewrite Pointer with Write Pointer Value
0100	Load Read Pointer with Reread Pointer Value
0101	Load Write Pointer with Rewrite Pointer Value
0110	Set DMA Transfer Direction (see Table 5)
0111	Reserved
1000	Increment A→B FIFO Read Pointer (Port B)
1001	Increment B→A FIFO Write Pointer (Port B)
1010	Reserved
1011	Reserved

2668 tbl 05

Table 2. Functions Performed by Port A Commands

RESET COMMAND FUNCTIONS

Reset Operands	Function
000	No Operation
001	Reset B→A FIFO (Read, Write, and Rewrite Pointers = 0)
010	Reset A→B FIFO (Read, Write, and Reread Pointers = 0)
011	Reset B→A and A→B FIFO
100	Reset Internal DMA Request Circuitry
101	No Operation
110	No Operation
111	Reset All

2668 tbl 04

Table 3. Reset Command Functions

SELECT CONFIGURATION REGISTER/ COMMAND FUNCTIONS

Operands	Function
000	Select Configuration Register 0
001	Select Configuration Register 1
010	Select Configuration Register 2
011	Select Configuration Register 3
100	Select Configuration Register 4
101	Select Configuration Register 5
110	Select Configuration Register 6
111	Select Configuration Register 7

2668 tbl 06

Table 4. Select Configuration Register Functions.

DMA DIRECTION COMMAND FUNCTIONS

Operands	Function
XX0	Write B→A FIFO
XX1	Read A→B FIFO

2668 tbl 07

Table 5. Set DMA Direction Command Functions. Command Only Operates in Peripheral Interface Mode

STATE AFTER RESET

	Hardware Reset (*RS* asserted)	Software Reset				
		B→A(001)	A→B(010)	B→A and A→B(011)	Internal Request (100)	All(111)
Configuration Registers 0-3	0000H	—	—	—	—	0000H
Configuration Register 4	6420H	—	—	—	—	6420H
Configuration Register 5	0000H	—	—	—	—	0000H
Configuration Register 6-7	0000H	—	—	—	—	0000H
Status Register format	0	—	—	—	—	—
B→A Read, Write, Rewrite Pointers	0	0	—	0	—	0
A→B Read, Write, Reread Pointers	0	—	0	0	—	0
DMA direction	B→A write	—	—	—	—	—
DMA internal request	clear	—	—	—	clear	clear

2668 tbl 08

Table 6. The BiFIFO State After a Reset Command

Table 8. Configuration Registers 0-3 contain the programmable flag offsets for the Almost-Empty and Almost-Full flags. These offsets are set to **0** when a hardware reset or a software Reset All is applied. Note that Table 8 shows that Configuration Registers 0-3 are 10 bits wide to accommodate the 1024 locations in each FIFO memory of the IDT7252/520. Only 9 least significant bits are used for the 512 locations of the IDT7251/510; the most significant bit, bit 9, must be set to **0**.

Configuration Register 4 is used to assign the internal flags to the external flag pins (FLG_A-FLG_D). Each external flag pin is assigned an internal flag based on the four bit codes shown in Table 9. The default condition for Configuration Register 4 is **6420H** as shown in Table 6. The default flag assignments are: FLG_D is assigned B→A $\overline{Full}$, FLG_C is assigned B→A $\overline{Empty}$, FLG_B is assigned A→B $\overline{Full}$, FLG_A is assigned A→B $\overline{Empty}$.

Configuration Register 5 is a general control register. The format of Configuration Register 5 is shown in Table 10.

Bit 0 sets the Intel-style interface ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style interface ($\overline{DS}_B$, R/$\overline{W}_B$) for Port B. Bits 2 and 3 redefine Full and Empty Flags for reread/rewrite data protection.

Bits 4-9 control the DMA interface and are only applicable in peripheral interface mode. In processor interface mode, these bits are don't care states. Bits 4 and 5 set the polarity of the DMA control pins REQ and ACK respectively. An internal clock controls all DMA operations. This internal clock is derived from the external clock (CLK). Bit 9 determines the internal clock frequency: the internal clock = CLK or the internal clock = CLK divided by 2. Bit 8 sets whether $\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for either one or two internal clocks. Bits 6 and 7 set the number of internal clocks between REQ assertion and ACK assertion. The timing can be from 2 to 5 cycles as shown in Figure 17.

Bit 10 controls Port B processor or peripheral interface mode. In processor mode, the Port B control pins ($\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$, R/$\overline{W}_B$) are inputs and the DMA controls are ignored. In peripheral mode, the Port B control pins are outputs and the DMA controls are active.

Six PIO pins can be programmed as an input or output by the corresponding mask bits in Configuration Register 7. The format of Configuration Register 7 is shown in Figure 5. Each bit of the register set the I/O direction independently. A logic **1** indicates that the corresponding PIO pin is an output, while a logic **0** indicates that the PIO pin is an input. This I/O mask register can be read or written.

A programmed output PIO_i pin (i = 0, 1, . . . 5) displays the data latched in Bit i of Configuration Register 6. A programmed input PIO_i pin allows Port A bus to sample the data on DA_i by reading Configuration Register 6.

STATUS REGISTER FORMAT

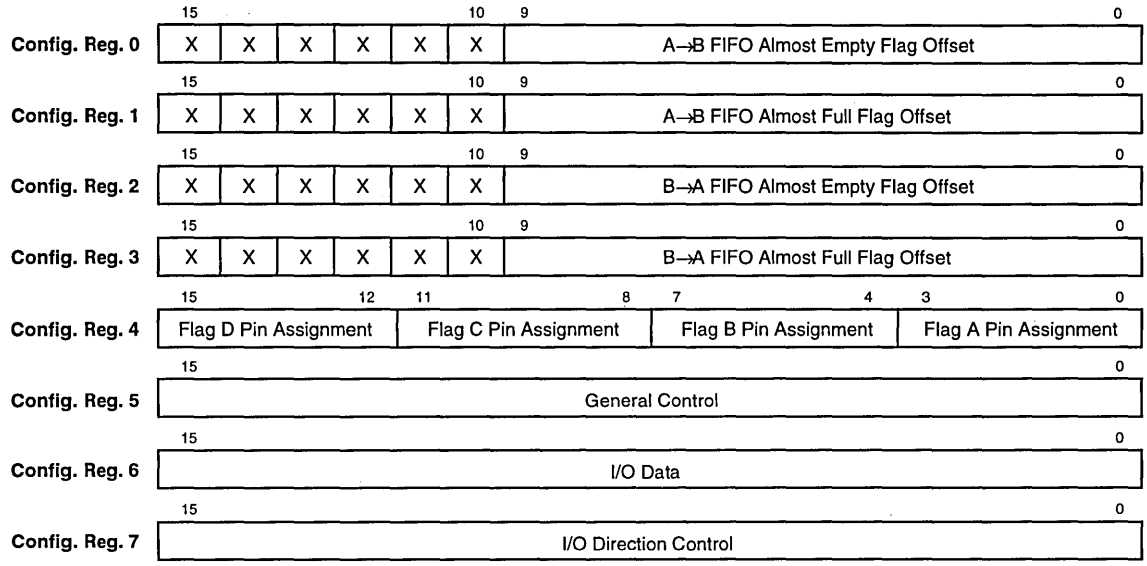
Bit	Signal
0	Reserved
1	Reserved
2	Reserved
3	DMA Direction
4	A→B Empty Flag
5	A→B Almost-Empty Flag
6	B→A Full Flag
7	B→A Almost-Full Flag
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	A→B Full Flag
13	A→B Almost-Full Flag
14	B→A Empty Flag
15	B→A Almost-Empty Flag

2668 tbl 09

Table 7. The Status Register Format

5

CONFIGURATION REGISTER FORMATS



NOTE:

1. Bit 9 of Configuration Registers 0-3 must be set to 0 on the IDT72511.

2668 tbl 10

Table 8. The BiFIFO Configuration Register Formats

Programmable Flags

The IDT BiFIFO has eight internal flags. Associated with each FIFO memory array are four internal flags, Empty, Almost-Empty, Almost-Full and Full, for the total of eight internal flags. The Almost-Empty and Almost-Full offsets can be set to any depth through the Configuration Registers 0-3 (see Table 8). The flags are asserted at the depths shown in Table 11. After a hardware reset or a software Reset All, the almost flag offsets are set to 0. Even though the offsets are equivalent, the Empty and Almost-Empty flags have different timing which means that the flags are not coincident. Similarly, the Full and Almost-Full flags are not coincident after reset because of timing.

These eight internal flags can be assigned to any of four external flag pins (FLGA-FLGD) through Configuration Register 4 (see Table 9). For the specific flag timings, see Figures 20-23.

The current state of all eight flags is available in the Status Register.

EXTERNAL FLAG ASSIGNMENT CODES

Assignment Code	Internal Flag Assigned to Flag Pin
0000	A→B $\overline{\text{Empty}}$
0001	A→B $\overline{\text{Almost-Empty}}$
0010	A→B $\overline{\text{Full}}$
0011	A→B $\overline{\text{Almost-Full}}$
0100	B→A $\overline{\text{Empty}}$
0101	B→A $\overline{\text{Almost-Empty}}$
0110	B→A $\overline{\text{Full}}$
0111	B→A $\overline{\text{Almost-Full}}$
1000	A→B Empty
1001	A→B Almost-Empty
1010	A→B Full
1011	A→B Almost-Full
1100	B→A Empty
1101	B→A Almost-Empty
1110	B→A Full
1111	B→A Almost-Full

2668 tbl 11

Table 9. Configuration Register 4 Internal Flag Assignments to External Flag Pins

CONFIGURATION REGISTER 5 FORMAT

Bit	Function		
0	Select Port B Interface $\overline{R}_B$ and $\overline{W}_B$ or $\overline{DS}_B$ and R/$\overline{W}_B$	0	Pins are $\overline{R}_B$ and $\overline{W}_B$ (Intel-style interface)
		1	Pins are $\overline{DS}_B$ and R/$\overline{W}_B$ (Motorola-style interface)
1	Unused		
2	Full Flag Definition	0	Write pointer meets read pointer
		1	Write pointer meets reread pointer
3	Empty Flag Definition	0	Read pointer meets write pointer
		1	Read pointer meets rewrite pointer
4	REQ Pin Polarity	0	REQ pin active HIGH
		1	REQ pin active LOW
5	ACK Pin Polarity	0	ACK pin active LOW
		1	ACK pin active HIGH
7-6	REQ / ACK Timing	00	2 internal clocks between REQ assertion and ACK assertion
		01	3 internal clocks between REQ assertion and ACK assertion
		10	4 internal clocks between REQ assertion and ACK assertion
		11	5 internal clocks between REQ assertion and ACK assertion
8	Port B Read & Write Timing Control for Peripheral Mode	0	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 1 internal clock
		1	$\overline{R}_B$, $\overline{W}_B$, and $\overline{DS}_B$ are asserted for 2 internal clocks
9	Internal Clock Frequency Control	0	Internal clock = CLK
		1	Internal clock = CLK divided by 2
10	Port B Interface Mode Control	0	Processor interface mode (Port B controls are inputs)
		1	Peripheral interface mode (Port B controls are outputs)
11	Unused		
12	Unused		
13	Unused		
14	Unused		
15	Unused		

2668 tbl 12

Table 10. BiFIFO Configuration Register 5 Format

CONFIGURATION REGISTER 6 FORMAT

15 ... 6	5	4	3	2	1	0
Unused	PIO5	PIO4	PIO3	PIO2	PIO1	PIO0

2668 tbl 13

Figure 4. BiFIFO Configuration Register 6 Format for Programmable I/O Data

CONFIGURATION REGISTER 7 FORMAT

15 ... 6	5	4	3	2	1	0
Unused	MIO5	MIO4	MIO3	MIO2	MIO1	MIO0

2668 tbl 14

Figure 5. BiFIFO Configuration Register 7 Format for Programmable I/O Direction Mask

Port B Interface

Port B has reread/rewrite and DMA functions. Port B can be configured to interface to either Intel-style ($\overline{R}_B$, $\overline{W}_B$) or Motorola-style ($\overline{DS}_B$, R/$\overline{W}_B$) devices in Configuration Register 5 (see Table 10). Port B can also be configured to talk to a processor or a peripheral device through Configuration Register 5. In processor interface mode, the Port B interface controls are inputs. In peripheral interface mode, the Port B interface controls are outputs. After a hardware reset or a software Reset All command, Port B defaults to an Intel-style processor interface; the controls are inputs.

DMA Control Interface

The BiFIFO has DMA control to simplify data transfers with peripherals. For the BiFIFO DMA controls (REQ, ACK and CLK) to operate, the BiFIFO must be in peripheral interface mode (Configuration Register 5, Table 10).

DMA timing is controlled by the external clock input, CLK. An internal clock is derived from this CLK signal to generate the $\overline{R}_B$, $\overline{W}_B$, $\overline{DS}_B$ and R/$\overline{W}_B$ output signals. The internal clock also determines the timing between REQ assertion and ACK assertion. Bit 9 of Configuration Register 5 determines whether the internal clock is the same as CLK or whether the internal clock is CLK divided by 2.

Bit 8 of Configuration Register 5 set whether $\overline{R}_B$, $\overline{W}_B$ and $\overline{DS}_B$ are asserted for 1 or 2 internal clocks. Bits 6 and 7 of Configuration Register 5 set the number of clocks between REQ assertion and ACK assertion. The clocks between REQ assertion and ACK assertion can be 2, 3, 4 or 5.

Bits 4 and 5 of Configuration Register 5 set the polarity of the REQ and ACK pins respectively.

A DMA transfer command sets the Port B read/write direction (see Table 5). The timing diagram for DMA transfers is shown in Figure 17. The basic DMA transfer starts with REQ assertion. After 2 to 5 internal clocks, ACK is asserted by the BiFIFO. ACK will not be asserted if a read is attempted on an empty A→B FIFO or if a write is attempted on a full B→A FIFO. If the BiFIFO is in Motorola-style interface mode, R/$\overline{W}_B$ is set at the same time that ACK is asserted. One internal clock later, $\overline{DS}_B$ is asserted. If the BiFIFO is in Intel-style interface mode, either $\overline{R}_B$ or $\overline{W}_B$ is asserted one internal clock after ACK assertion. These read/write controls stay asserted for 1 or 2 internal clocks, then ACK, $\overline{DS}_B$, $\overline{R}_B$ and $\overline{W}_B$ are made inactive. This completes the transfer of one 9-bit word.

On the next rising edge of CLK, REQ is sampled. If REQ is still asserted, another DMA transfer starts with the assertion of ACK. Data transfers will continue as long as REQ is asserted.

Intelligent Reread/Rewrite

Intelligent reread/rewrite is a method the BiFIFO uses to help assure data integrity. Port B of the BiFIFO has two extra pointers, the Reread Pointer and the Rewrite Pointer.The Reread Pointer is associated with the A->B FIFO Read Pointer, while the Rewrite Pointer is associated with the B->A FIFO Write Pointer. The Reread Pointer holds the start address of a data block in the A->B FIFO RAM, and the Read Pointer is the current address of the same FIFO RAM array. By loading the Read Pointer with the value held in the Reread Pointer (RER asserted), reads will start over at the beginning of the data block. In order to mark the beginning of a data block, the Reread Pointer should be loaded with the Read Pointer value (LDRER asserted) before the first read is performed on this data block. Figure 6 shows a Reread operation.

Similarly, the Rewrite Pointer holds the start address of a data block in the B->A FIFO RAM, while the Write Pointer is the current address within the RAM array. The operation of the REW and LDREW is identical to the RER and LDRER discussed above. Figure 7 shows a Rewrite operation.

For the reread data protection, Bit 2 of Configuration Register 5 can be set to 1 to prevent the data block from being overwritten. In this way, the assertion of A->B full flag will occur when the write pointer meets the reread pointer instead of the read pointer as in the normal definition. For the rewrite data protection, Bit 3 of Configuration Register 5 can be set to 1 to

INTERNAL FLAG TRUTH TABLE

Number of Words in FIFO					
From	To	Empty Flag	Almost-Empty Flag	Almost-Full Flag	Full Flag
0	0	Asserted	Asserted	Not Asserted	Not Asserted
1	n	Not Asserted	Asserted	Not Asserted	Not Asserted
n + 1	D – (m + 1)	Not Asserted	Not Asserted	Not Asserted	Not Asserted
D – m	D – 1	Not Asserted	Not Asserted	Asserted	Not Asserted
D	D	Not Asserted	Not Asserted	Asserted	Asserted

NOTE: 2668 tbl 15

1. BiFIFO flags must be assigned to external flag pins to be observed. D = FIFO depth (IDT72511 = 512, IDT72521 = 1024), n = Almost-Empty flag offset, m = Almost-Full flag offset.

Table 11. Internal Flag Truth Table

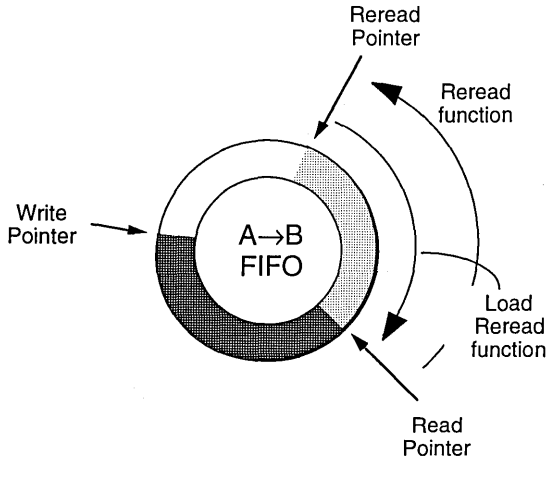
prevent the data block from being read. In this case the assertion of B->A empty flag will occur when the read pointer meets the rewrite pointer instead of the write pointer.

In conclusion, Bit 2 and 3 of Configuration Register 5 are used to redefine Full & Empty flags for data block partition. Although it can serve the purpose of data protection, the setting of these 2 bits is independent of the functions caused by RER/REW, or LDRER/LDREW assertions.

Programmable Input/Output

The BiFIFO has six programmable I/0 pins (PIO_0 - PIO_5) which are controlled by Port A through Configuration Registers 6 and 7. Data from the programmable I/O pins is mapped directly to the six least significant bits of Configuration Register 6. Figure 4 shows the format of Configuration Register 6. This data is read or written by Port A on the data pins (DA_0- DA_5). A programmed output PIO_i pin (i = 0, 1, . . . , 5) displays the data latched in Bit i of Configuration Register 6. A programmed input PIO_i pin allows Port A bus to sample its data on DA_i by reading Configuration Register 6. The read and write timing for the programmable I/O pins is shown in Figure 19. The direction of each programmable I/O pin can be set independently by programming the mask in Configuration Register 7. Each P10 pin has a corresponding input/output direction mask bit in Configuration Register 7. Figure 5 shows the format of Configuration Register 7. Setting a mask bit to a logic 1 makes the corresponding I/O pin an output. Mask bits set to logic 0 force the corresponding I/O pin to an input.

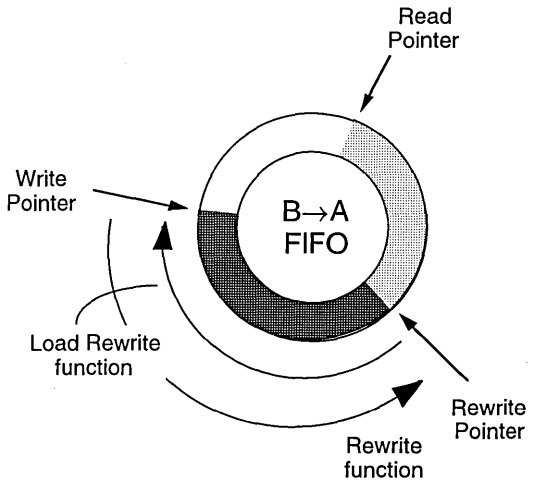
REREAD OPERATIONS (1,2)



NOTES:
1. If bit 2 is set to 1,
   Empty flag asserted if Read = Write
   Full flag asserted if Reread + FIFO size = Write
2. If bit 2 is set to 0,
   Empty flag asserted if Read = Write
   Full flag asserted if Read + FIFO size = Write

Figure 6. BiFIFO Reread Operations

REWRITE OPERATIONS (3,4)



NOTES:
1. If bit 3 is set to 1,
   Empty flag asserted if Read = Rewrite
   Full flag asserted if Read + FIFO size = Write
2. If bit 3 is set to 0,
   Empty flag asserted if Read = Write
   Full flag asserted if Read + FIFO size = Write

Figure 7. BiFIFO Rewrite Operations

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage With Respect To Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2668 tbl 16

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage Commercial	2.0	—	—	V
V_{IH}	Input HIGH Voltage Military	2.2	—	—	V
V_{IL}(1)	Input LOW Voltage Commercial and Military	—	—	0.8	V

NOTE: 2668 tbl 17

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72511L IDT72521L Commercial t_A = 25, 35, 50ns Min.	Typ.	Max.	IDT72521L Military t_A = 40, 50ns Min.	Typ.	Max.	Unit
I_{IL}(1)	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	µA
I_{OL}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –1mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 4mA	—	—	0.4	—	—	0.4	V
I_{CC1} (3)(4)	Average VCC Power Supply Current	—	150	230	—	180	250	mA
I_{CC2} (3)	Average Standby Current ($\overline{R_B}$ = $\overline{W_B}$ = $\overline{DS_A}$ = V_{IH})	—	16	30	—	24	50	mA

NOTES: 2668 tbl 18

1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}, $\overline{DS_A}$ = $\overline{DS_B}$ ≥ V_{IH}
2. Measurements with 0.4V ≤ V_{OUT} ≤ V_{CC}, $\overline{DS_A}$ = $\overline{DS_B}$ ≥ V_{IH}
3. Measurements are made with outputs open.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 8

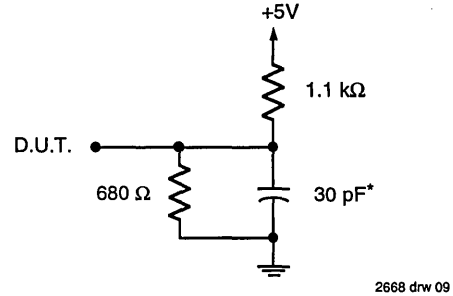
2668 tbl 19

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN} (2)	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT} (1,2)	Output Capacitance	V_{OUT} = 0V	12	pF

NOTES: 2668 tbl 20

1. With output deselected.
2. Characterized values, not currently tested.



2668 drw 09

or equivalent circuit

Figure 8. Output Load
*Includes jig and scope capacitances

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to + 125°C)

Symbol	Parameter	Commercial				Military		Com'l & Mil.[2]		Unit	Timing Figure
		IDT72511L25 IDT72521L25		IDT72511L35 IDT72521L35		IDT72521L40		IDT72511L50 IDT72521L50			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
RESET TIMING (Port A and Port B)											
t_{RSC}	Reset cycle time	35	—	45	—	50	—	65	—	ns	9
t_{RS}	Reset pulse width	25	—	35	—	40	—	50	—	ns	9
t_{RSS}	Reset set-up time	25	—	35	—	40	—	50	—	ns	9
t_{RSR}	Reset recovery time	10	—	10	—	10	—	15	—	ns	9
t_{RSF}	Reset to flag time	—	35	—	45	—	50	—	65	ns	9
PORT A TIMING											
t_{AA}	Port A access time	—	25	—	35	—	40	—	50	ns	12, 14, 15
t_{ALZ}	Read or write pulse LOW to data bus at Low-Z	5	—	5	—	5	—	5	—	ns	12, 15, 16
t_{AHZ}	Read or write pulse HIGH to data bus at High- Z	—	15	—	20	—	25	—	30	ns	12, 14, 15, 16
t_{ADV}	Data valid from read pulse HIGH	5	—	5	—	5	—	5	—	ns	12, 14, 16
t_{ARC}	Read cycle time	35	—	45	—	50	—	65	—	ns	12
t_{ARPW}	Read pulse width	25	—	35	—	40	—	50	—	ns	12, 14, 15
t_{ARR}	Read recovery time	10	—	10	—	10	—	15	—	ns	12
t_{AS}	$\overline{CS}_A$, A_0, A_1, $R/\overline{W}_A$ set-up time	5	—	5	—	5	—	5	—	ns	10, 12, 16
t_{AH}	$\overline{CS}_A$, A_0, A_1, $R/\overline{W}_A$ hold time	5	—	5	—	5	—	5	—	ns	10, 12
t_{ADS}	Data set-up time	15	—	18	—	20	—	30	—	ns	11, 12, 14, 15
t_{ADH}[1]	Data hold time	0	—	2	—	5	—	5	—	ns	11, 12, 14, 15
t_{AWC}	Write cycle time	35	—	45	—	50	—	65	—	ns	12
t_{AWPW}	Write pulse width	25	—	35	—	40	—	50	—	ns	11, 12, 14
t_{AWR}	Write recovery time	10	—	10	—	10	—	15	—	ns	12
t_{AWRCOM}	Write recovery time after a command	25	—	35	—	40	—	50	—	ns	11

NOTE:

2668 tbl 21

1. The minimum data hold time is 5ns (10ns for the 80ns speed grade) when writing to the Command or Configuration registers.
2. IDT72511 not available in military.

5

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to + 125°C)

		Commercial				Military		Com'l & Mil.[1]			
		IDT72511L25 IDT72521L25		IDT72511L35 IDT72521L35		IDT72521L40		IDT72511L50 IDT72521L50			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
PORT B PROCESSOR INTERFACE TIMING											
t_{BA}	Port B access time	—	25	—	35	—	40	—	50	ns	13, 14, 15
t_{BLZ}	Read or write pulse LOW to data bus at Low-Z	5	—	5	—	5	—	5	—	ns	13, 14, 15
t_{BHZ}	Read or write pulse HIGH to data bus at High-Z	—	15	—	20	—	25	—	30	ns	14, 13, 15
t_{BDV}	Data valid from read pulse HIGH	5	—	5	—	5	—	5	—	ns	13, 14, 15, 16
t_{BRC}	Read cycle time	35	—	45	—	50	—	65	—	ns	13
t_{BRPW}	Read pulse width	25	—	35	—	40	—	50	—	ns	13
t_{BRR}	Read recovery time	10	—	10	—	10	—	15	—	ns	13
t_{BS}	$R/\overline{W}_B$ set-up time	5	—	5	—	5	—	5	—	ns	13
t_{BH}	$R/\overline{W}_B$ hold time	5	—	5	—	5	—	5	—	ns	13
t_{BDS}	Data set-up time	15	—	18	—	20	—	30	—	ns	13, 14, 15
t_{BDH}	Data hold time	0	—	2	—	5	—	5	—	ns	13, 14, 15
t_{BWC}	Write cycle time	35	—	45	—	50	—	65	—	ns	13
t_{BWPW}	Write pulse width	25	—	35	—	40	—	50	—	ns	13, 15
t_{BWR}	Write recovery time	10	—	10	—	10	—	15	—	ns	13
PORT B PERIPHERAL INTERFACE TIMING											
t_{BA}	Port B access time	—	25	—	40	—	45	—	55	ns	17
t_{BCKC}	Clock cycle time	15	—	20	—	20	—	25	—	ns	17
t_{BCKH}	Clock pulse HIGH time	6	—	6	—	8	—	10	—	ns	17
t_{BCKL}	Clock pulse LOW time	6	—	6	—	8	—	10	—	ns	17
t_{BREQS}	Request set-up time	5	—	5	—	5	—	10	—	ns	17
t_{BREQH}	Request hold time	5	—	5	—	5	—	5	—	ns	17
t_{BACKL}	Delay from a rising clock edge to ACK switching	—	15	—	18	—	20	—	25	ns	17

NOTE:

1. IDT72511 not available in military.

2668 tbl 22

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to + 125°C)

		Commercial				Military		Com'l & Mil.[4]			
		IDT72511L25 IDT72521L25		IDT72511L35 IDT72521L35		IDT72521L40		IDT72511L50 IDT72521L50			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
PORT B RETRANSMIT TIMING											
t_{BDSBH}	$\overline{RER}$, $\overline{REW}$, LDRER, LDREW set-up and recovery time	10	—	10	—	10	—	15	—	ns	9, 18
PROGRAMMABLE I/O TIMING											
t_{PIOA}	Programmable I/O access time	—	20	—	25	—	25	—	30	ns	19
t_{PIOS}	Programmable I/O set-up time	8	—	10	—	10	—	15	—	ns	19
t_{PIOH}	Programmable I/O hold time	8	—	10	—	10	—	15	—	ns	19
BYPASS TIMING											
t_{BYA}	Bypass access time	—	18	—	20	—	25	—	30	ns	16
t_{BYD}	Bypass delay	—	10	—	15	—	20	—	20	ns	16
t_{aBYDV}	Bypass data valid time from $\overline{DS_A}$	15	—	15	—	15	—	15	—	ns	16
t_{bBYDV} [3]	Bypass data valid time from $\overline{DS_B}$	3	—	3	—	3	—	3	—	ns	16
FLAG TIMING [1] [2]											
t_{REF}	Read clock edge to Empty Flag asserted	—	25	—	35	—	40	—	45	ns	14, 15, 20, 22
t_{WEF}	Write clock edge to Empty Flag not asserted	—	25	—	35	—	40	—	45	ns	14, 15, 20, 22
t_{RFF}	Read clock edge to Full Flag not asserted	—	25	—	35	—	40	—	45	ns	14, 15, 21, 23
t_{WFF}	Write clock edge to Full Flag asserted	—	25	—	35	—	40	—	45	ns	14, 15, 21, 23
t_{RAEF}	Read clock edge to Almost-Empty Flag asserted	—	40	—	50	—	55	—	60	ns	20, 22
t_{WAEF}	Write clock edge to Almost-Empty Flag not asserted	—	40	—	50	—	55	—	60	ns	20, 22
t_{RAFF}	Read clock edge to Almost-Full Flag not asserted	—	40	—	50	—	55	—	60	ns	21, 23
t_{WAFF}	Write clock edge to Almost-Full Flag asserted	—	40	—	50	—	55	—	60	ns	21, 23

NOTES:

2668 tbl 23

1. Read and write are internal signals derived from $\overline{DS_A}$, $R/\overline{W_A}$, $\overline{DS_B}$, $R/\overline{W_B}$, $\overline{R_B}$, and $\overline{W_B}$.
2. Although the flags, Empty, Almost-Empty, Almost-Full, and Full Flags are internal flags, the timing given is for those assigned to external pins.
3. Values guaranteed by design, not currently tested.
4. IDT72511 not available in military.

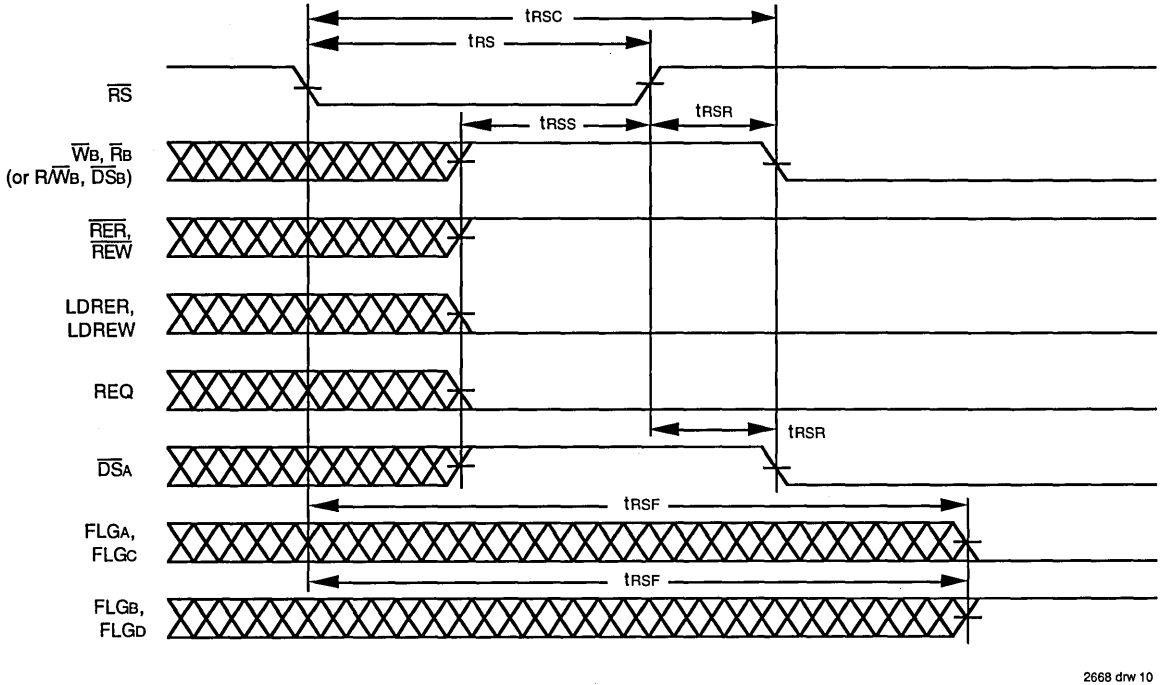


Figure 9. Hardware Reset Timing

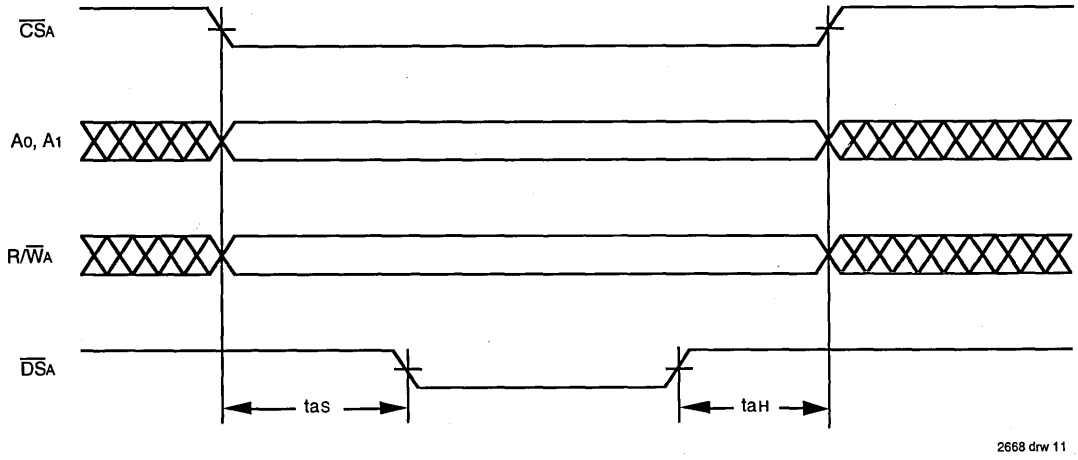


Figure 10. Basic Port A Control Signal Timing (Applies to All Port A Timing)

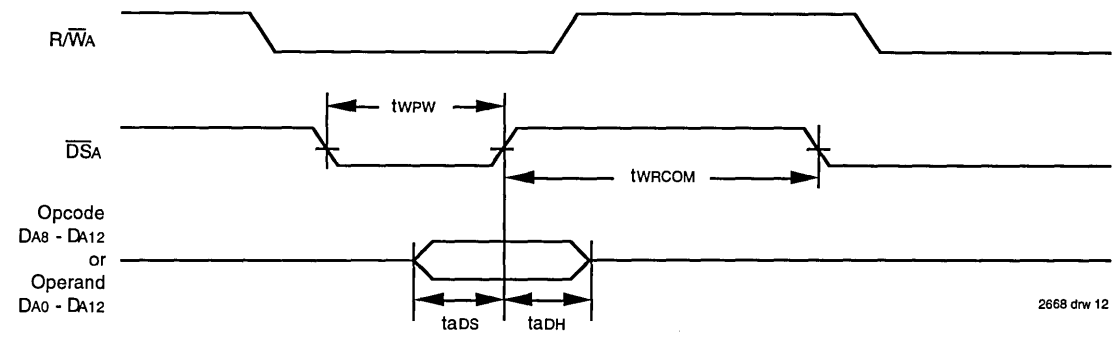
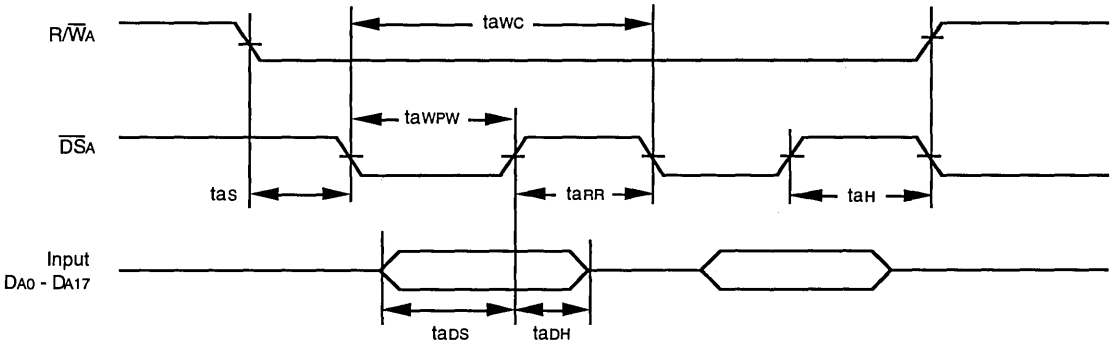


Figure 11. Port A Command Timing (write).

WRITE



READ

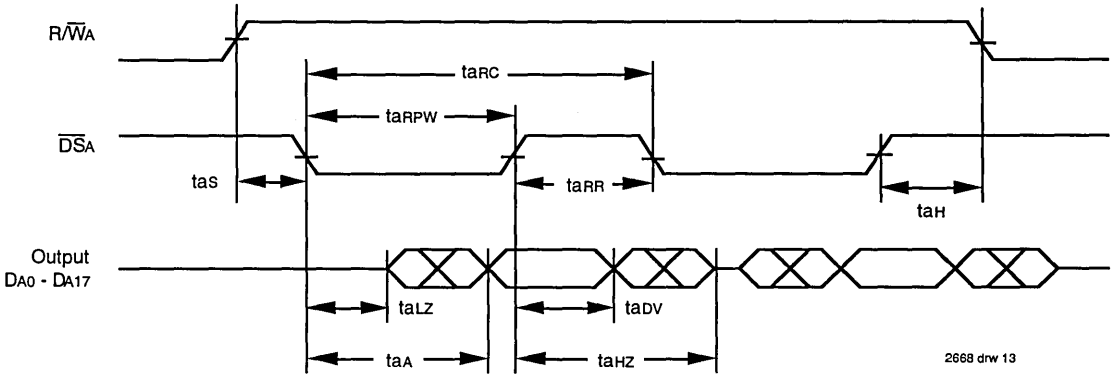
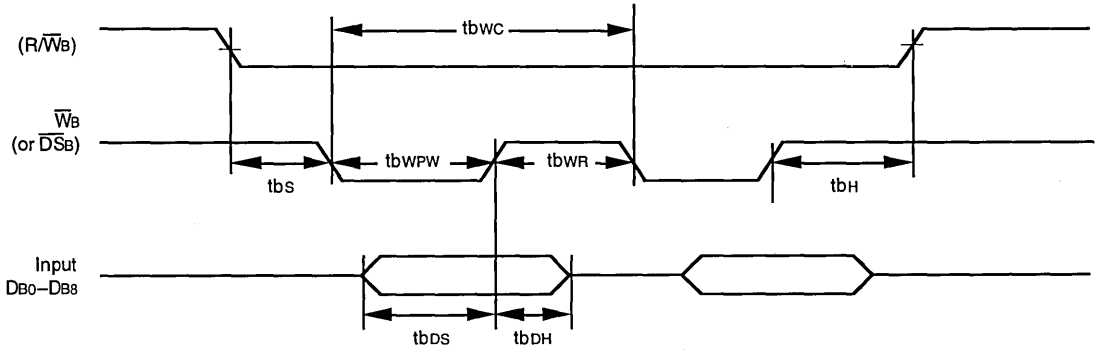


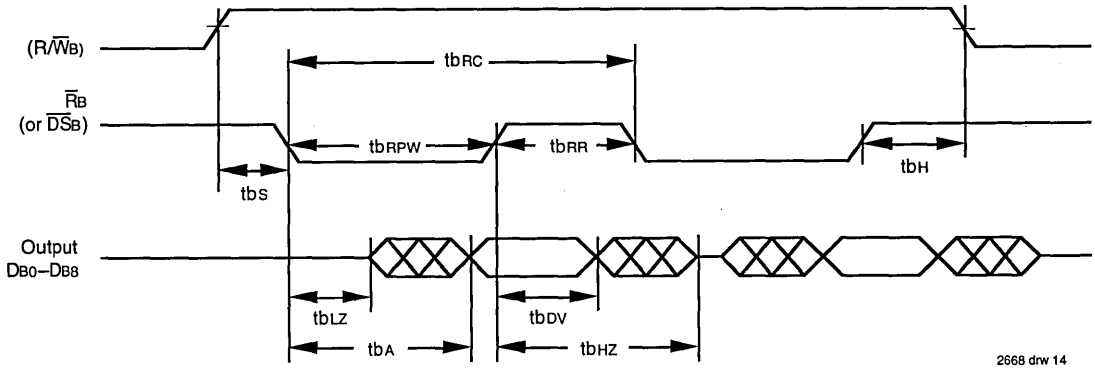
Figure 12. Read and Write Timing for Port A

WRITE



NOTE:
1. $\overline{R}_B$ = 1

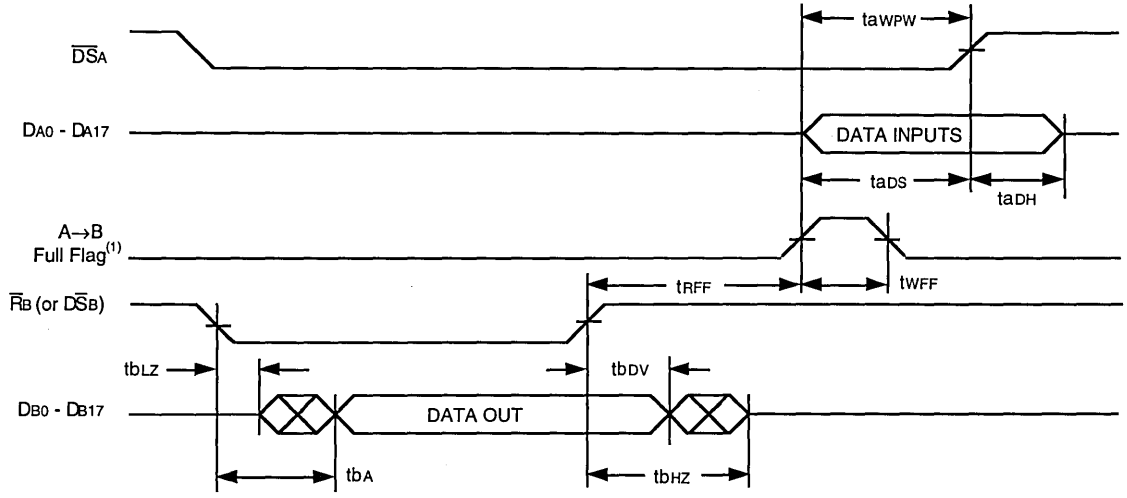
READ



NOTE:
1. $\overline{W}_B$ = 1

Figure 13. Port B Read and Write Timing, Processor Interface Mode Only

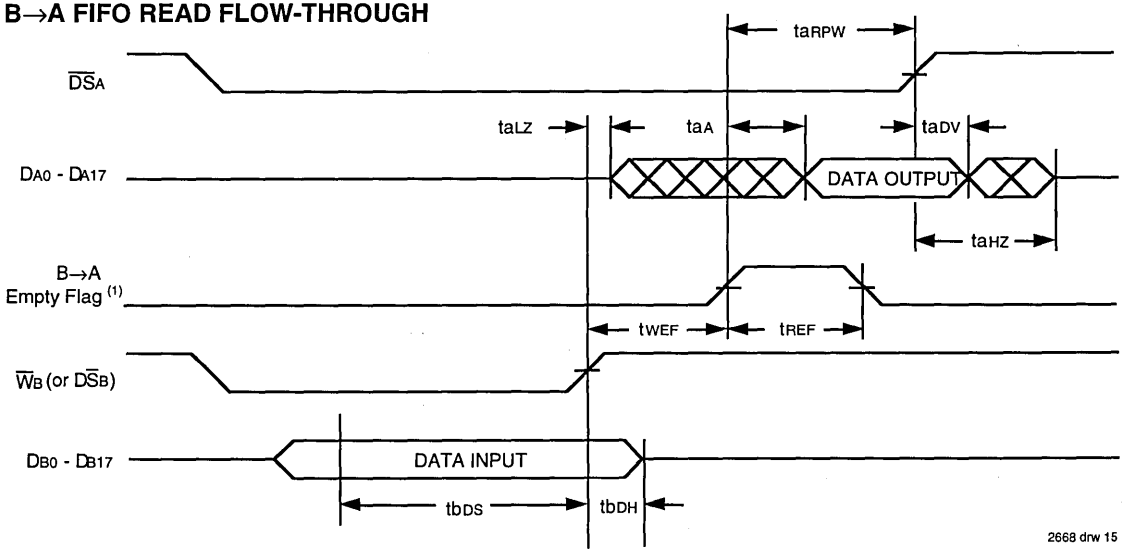
A→B FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. R/$\overline{W}$A = 0

5

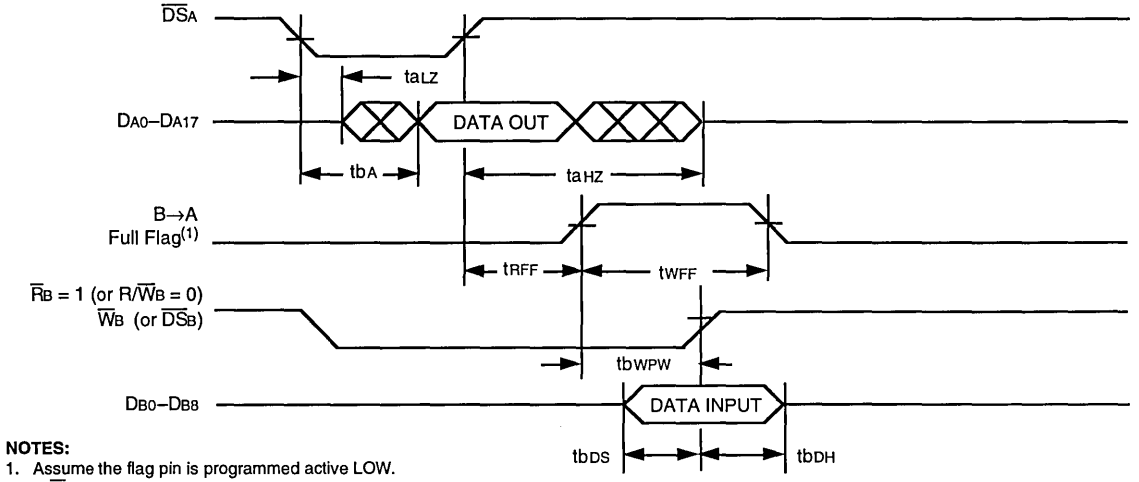
B→A FIFO READ FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. R/$\overline{W}$A = 1

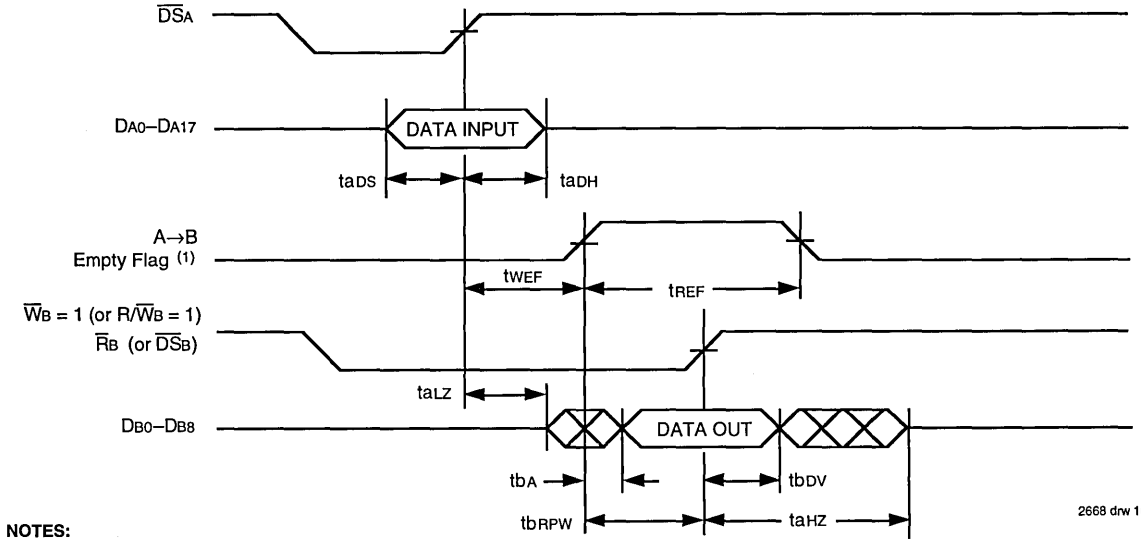
Figure 14. Port A Read and Write Flow-Through Timing, Processor Interface Mode Only

A→B FIFO WRITE FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. R/$\overline{W}_A$ = 1

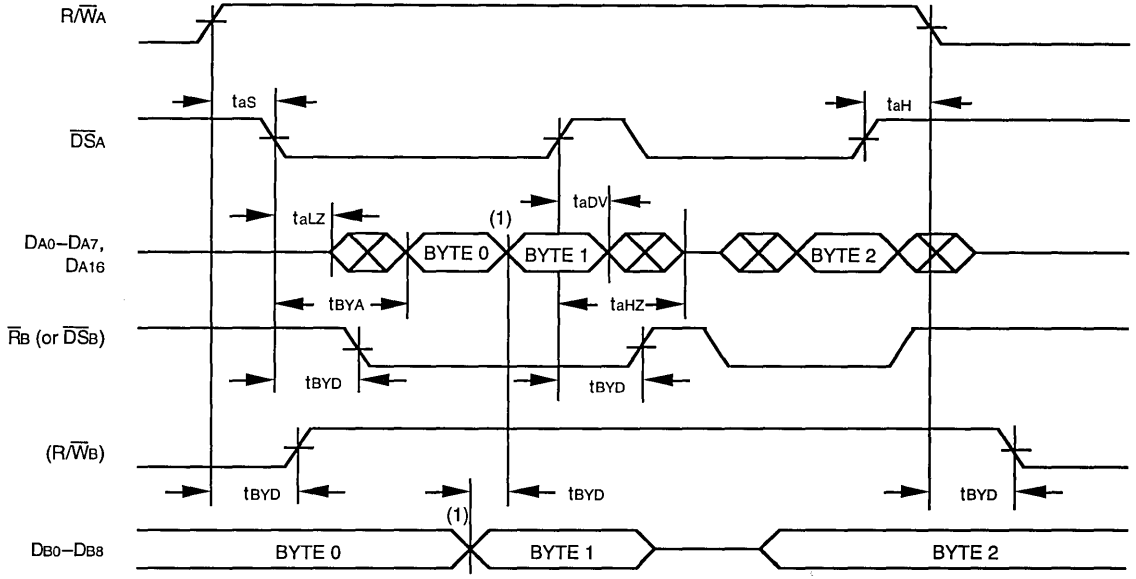
A→B FIFO READ FLOW-THROUGH



NOTES:
1. Assume the flag pin is programmed active LOW.
2. R/$\overline{W}_A$ = 0

Figure 15. Port B Read and Write Flow-Through Timing, Processor Interface Mode Only

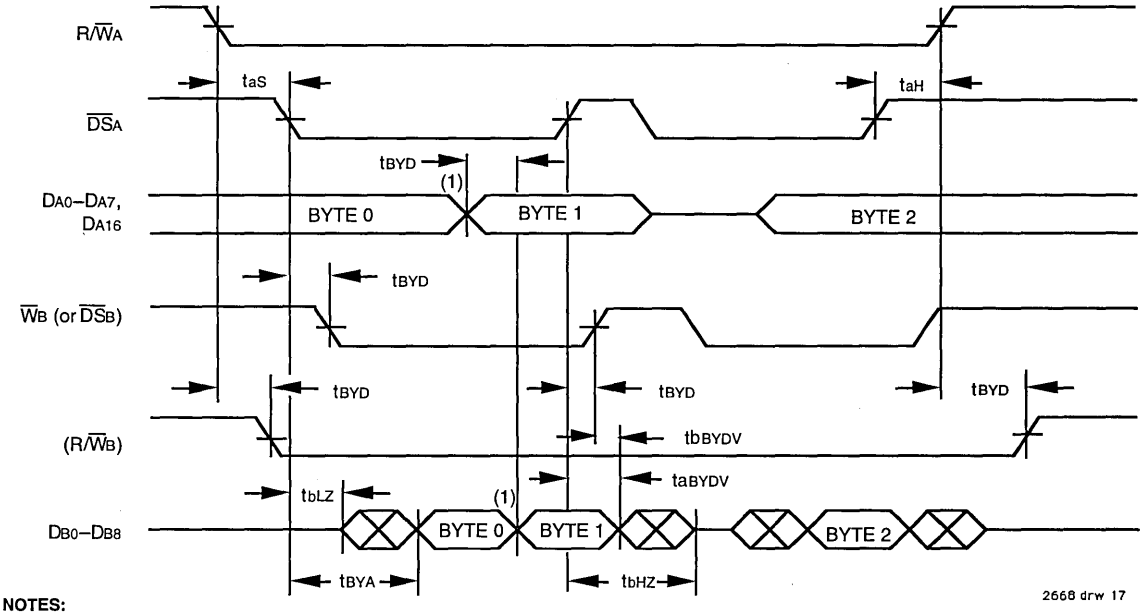
B→A READ BYPASS



NOTES:

1. Once the bypass mode starts, any data change on Port B bus (Byte 0→Byte 1) will be passed to Port A bus.
2. $\overline{W}$B = 1

A→B WRITE BYPASS



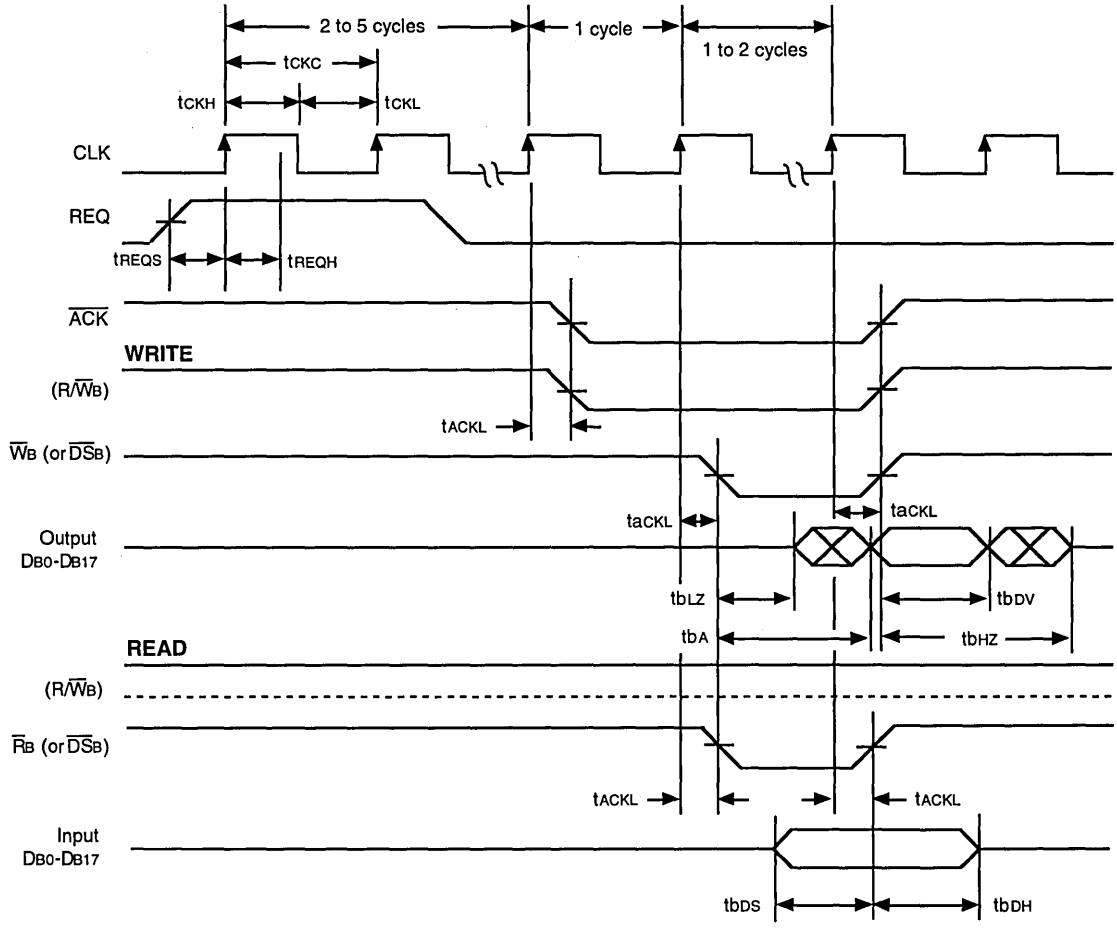
2668 drw 17

NOTES:

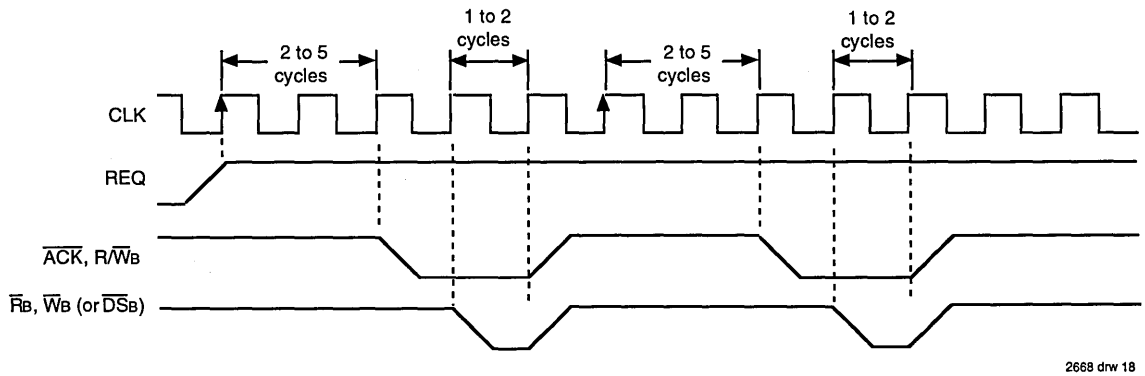
1. Once the bypass mode starts, any data change on Port A bus (Byte 0→Byte 1) will be passed to Port B bus.
2. $\overline{R}$B = 1

Figure 16. Bypass Path Timing, BiFIFO Must Be in Peripheral Interface Mode

SINGLE WORD DMA TRANSFER



BLOCK DMA TRANSFER



2668 drw 18

Figure 17. Port B Read and Write DMA timing. Peripheral Interface Mode Only

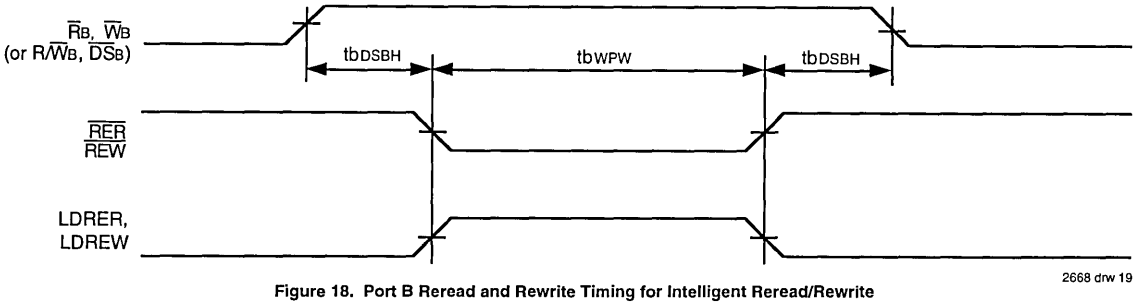
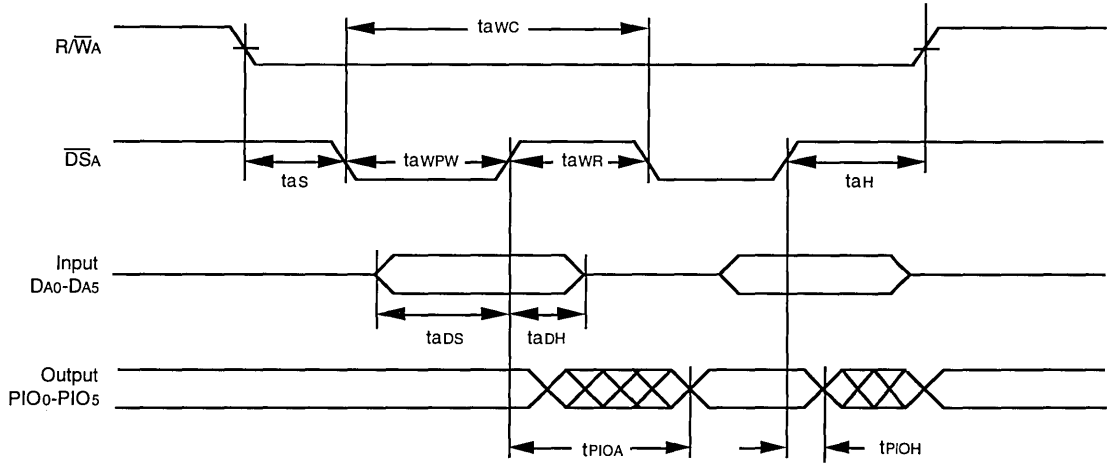


Figure 18. Port B Reread and Rewrite Timing for Intelligent Reread/Rewrite

Port A → PIO WRITE



PIO → Port A READ

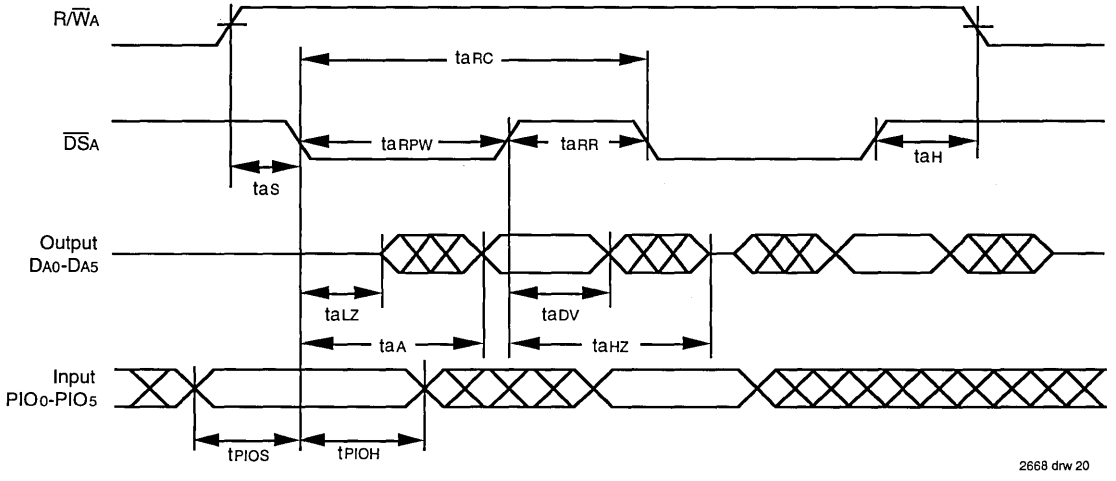
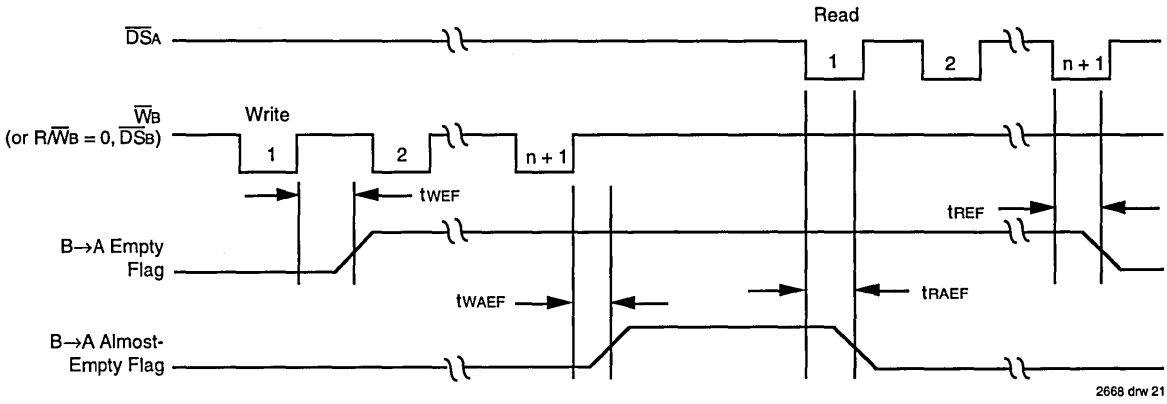
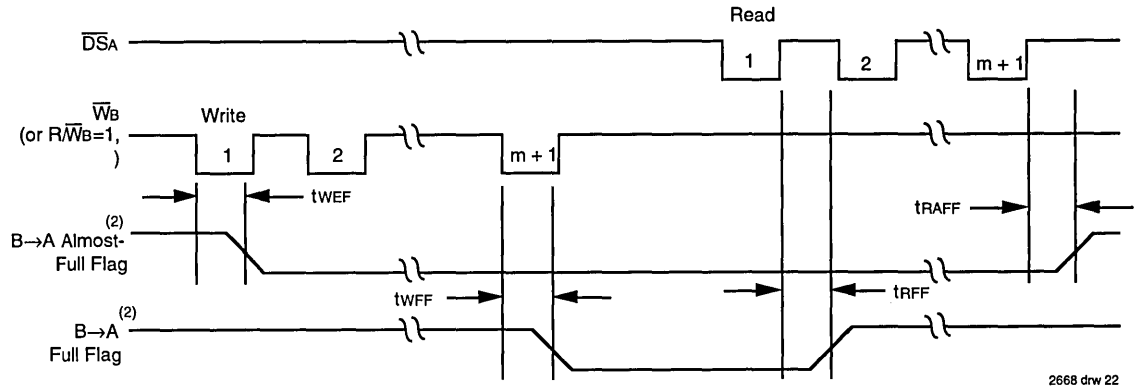


Figure 19. Programmable I/O Timing



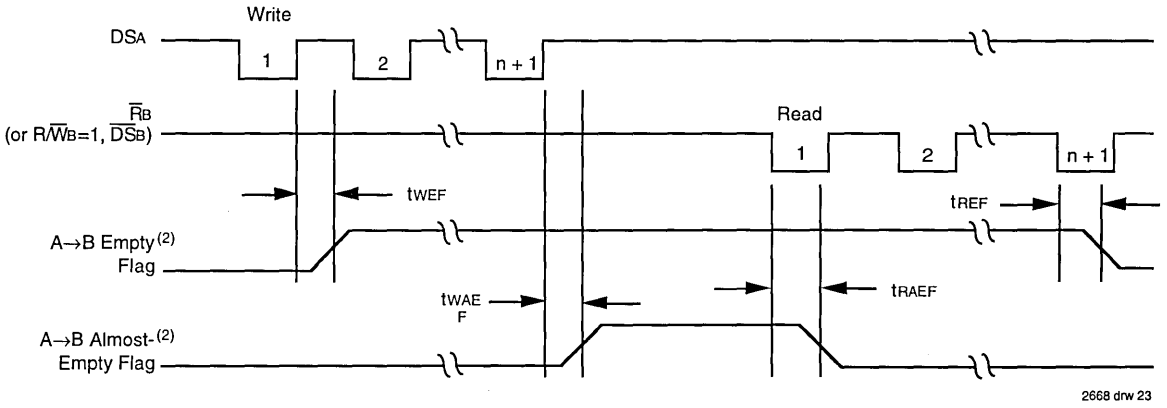
NOTES:
1. B→A FIFO is initially empty.
2. Assume the flag pins are programmed active LOW.
3. R/$\overline{W_A}$ = 1.

Figure 20. Empty and Almost-Empty Flag Timing for B→A FIFO, (n = programmed offset)



NOTES:
1. B→A FIFO initially contains D – (M + 1) data words. D = 512 for IDT72511; D = 1024 for IDT72521.
2. Assume the flag pins are programmed active LOW.
3. R/$\overline{W_A}$ = 1.

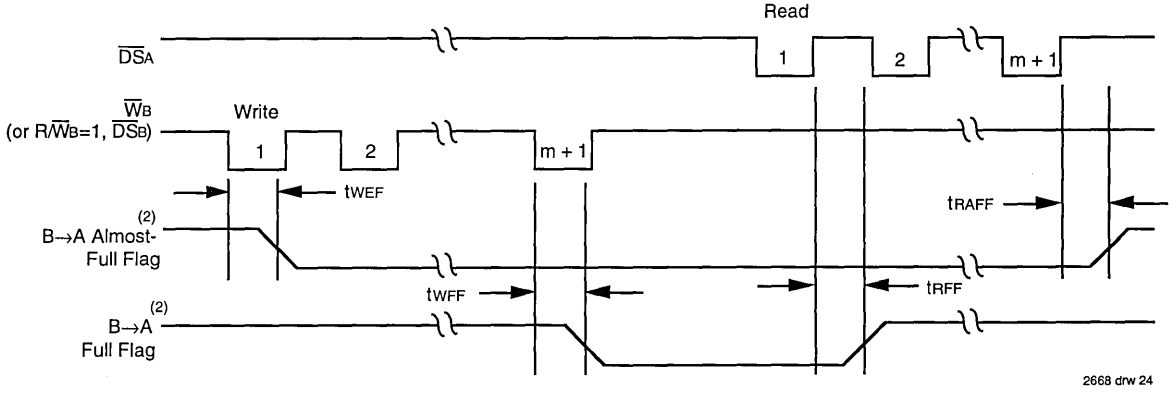
Figure 21. Full and Almost-Full Flag Timing for B→A FIFO, (m = programmed offset)



NOTES:
1. A→B FIFO is initially empty.
2. Assume the flag pins are programmed active LOW.
3. R/WA = 1.

Figure 22. Empty and Almost-Empty Flag Timing for A→B FIFO, (n = programmed offset)

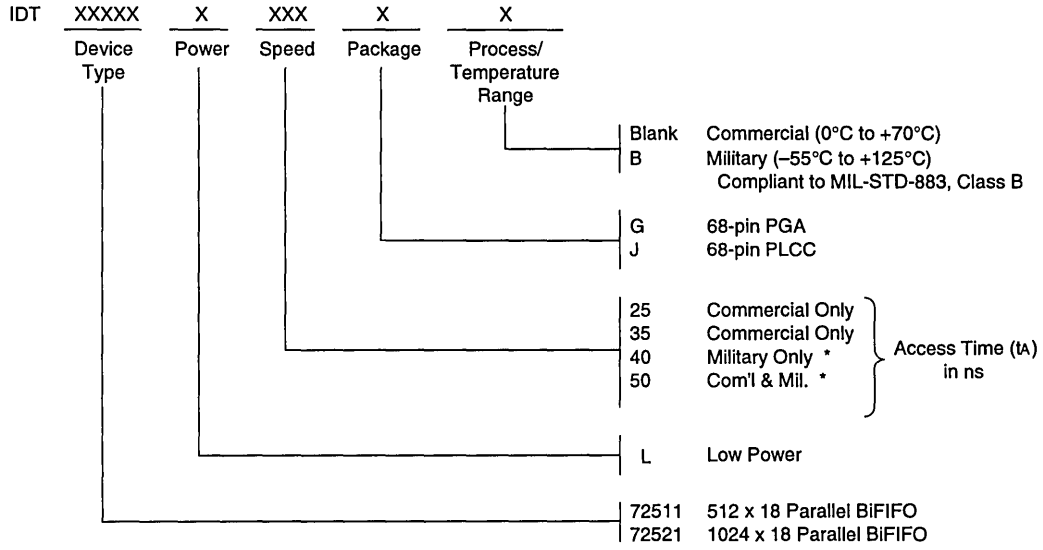
5



NOTES:
1. B→A FIFO initially contains D – (M + 1) data words. D = 512 for IDT72511; D = 1024 for IDT72521.
2. Assume the flag pins are programmed active LOW.
3. R/WA = 1.

Figure 23. Full and Almost-Full Flag Timing for A→B FIFO, (m = programmed offset)

ORDERING INFORMATION



2668 drw 25

* 40 Military Only, IDT72521
* 50 Commercial and Military, IDT72511 available in commercial only

Integrated Device Technology, Inc.

CMOS ASYNCHRONOUS FIFO WITH RETRANSMIT 1K x 9, 2K x 9, 4K x 9

IDT72021
IDT72031
IDT72041

FEATURES:

- First-In/First-Out Dual-Port memory
- Bit organization
  - IDT72021—1K x 9
  - IDT72031—2K x 9
  - IDT72041—4K x 9
- Ultra high speed
  - IDT72021—25ns access time
  - IDT72031—35ns access time
  - IDT72041—35ns access time
- Easily expandable in word depth and/or width
- Asynchronous and simultaneous read and write
- Functionally equivalent to IDT7202/03/04 with Output Enable ($\overline{OE}$) and Almost Empty/Almost Full Flag ($\overline{AEF}$)
- Four status flags: Full, Empty, Half-Full (single device mode), and Almost Empty/Almost Full (7/8 empty or 7/8 full in single device mode)
- Output Enable controls the data output port
- Auto-retransmit capability
- Available in 32-pin DIP and PLCC
- Military product compliant to MIL-STD-883, Class B

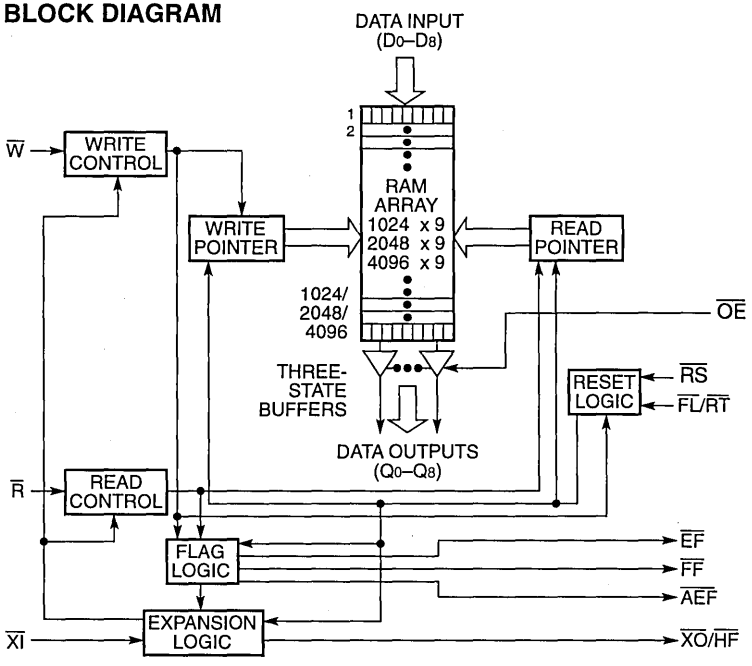
DESCRIPTION:

IDT72021/031/041s are high-speed, low-power, dual-port memory devices commonly known as FIFOs (First-In/First-Out). Data can be written into and read from the memory at independent rates. The order of information stored and extracted does not change, but the rate of data entering the FIFO might be different than the rate leaving the FIFO. Unlike a Static RAM, no address information is required because the read and write pointers advance sequentially. The IDT72021/031/041s can perform asynchronous and simultaneous read and write operations. There are four status flags, ($\overline{HF}$, $\overline{FF}$, $\overline{EF}$, $\overline{AEF}$) to monitor data overflow and underflow. Output Enable ($\overline{OE}$) is provided to control the flow of data through the output port. Additional key features are Write ($\overline{W}$), Read ($\overline{R}$), Retransmit ($\overline{RT}$), First Load ($\overline{FL}$), Expansion In ($\overline{XI}$) and Expansion Out ($\overline{XO}$). The IDT72021/031/041s are designed for those applications requiring data control flags and Output Enable ($\overline{OE}$) in multiprocessing and rate buffer applications.

The IDT72021/031/041s are fabricated using IDT's CMOS technology. Military grade product is manufactured in compliance with the latest version of MIL-STD-883, Class B, for high reliability systems.

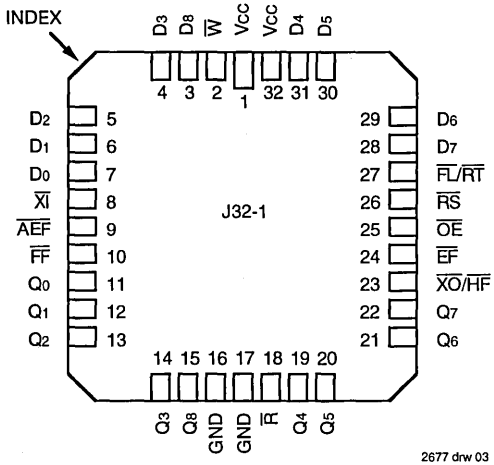
5

FUNCTIONAL BLOCK DIAGRAM

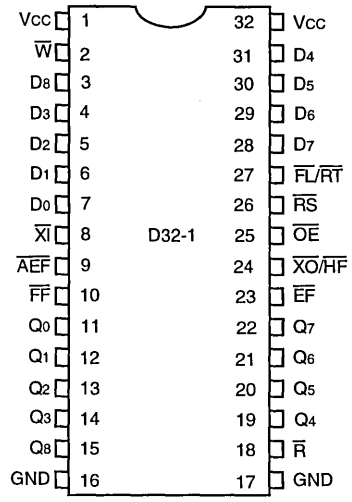


2677 drw 01

PIN CONFIGURATIONS



PLCC TOP VIEW



DIP TOP VIEW

2677 drw 02

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0–D8	Inputs	I	Data inputs for 9-bit wide data.
RS	Reset	I	When RS is set LOW, internal READ and WRITE pointers are set to the first location of the RAM array. HF and FF go HIGH, and AEF and EF go LOW. A reset is required before an initial WRITE after power-up. R and W must be HIGH during RS cycle.
W	Write	I	When WRITE is LOW, data can be written into the RAM array sequentially, independent of READ. In order for WRITE to be active, FF must be HIGH. When the FIFO is full (FF-LOW), the internal WRITE operation is blocked.
R	Read	I	When READ is LOW, data can be read from the RAM array sequentially, independent of WRITE. In order for READ to be active, EF must be HIGH. When the FIFO is empty (EF-LOW), the internal READ operation is blocked. The three-state output buffer is controlled by the read signal and the external output control (OE).
FL/RT	First Load/ Retransmit	I	This is a dual-purpose input. In the single device configuration (XI grounded), activating retransmit (FL/RT-LOW) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. R and W must be HIGH before setting FL/RT LOW. Retransmit is not compatible with depth expansion. In the depth expansion configuration, FL/RT-LOW indicates the first activated device.
XI	Expansion In	I	In the single device configuration, XI is grounded. In depth expansion or daisy chain expansion, XI is connected to XO (expansion out) of the previous device.
OE	Output Enable	I	When OE is set HIGH, the data flow through the three-state output buffer is inhibited regardless of an active READ operation. A read operation does increment the read pointer in this situation. When OE is set LOW, Q0-Q8 are still in a HIGH impedance condition if no READ occurs. For a complete READ operation with data appearing on Q0-Q8, both R and OE should be asserted LOW.
FF	Full Flag	O	When FF goes LOW, the device is full and further WRITE operations are inhibited. When FF is HIGH, the device is not full.
EF	Empty Flag	O	When EF goes LOW, the device is empty and further READ operations are inhibited. When EF is HIGH, the device is not empty.
AEF	Almost-Empty/ Almost-Full Flag	O	When AEF is LOW, the device is empty to 1/8 full or 7/8 to completely full. When AEF is HIGH, the device is greater than 1/8 full, but less than 7/8 full.
XO/HF	Expansion Out/ Half-Full Flag	O	This is a dual purpose output. In the single device configuration (XI grounded), the device is more than half full when HF is LOW. In the depth expansion configuration (XO connected to XI of the next device), a pulse is sent from XO to XI when the last location in the RAM array is filled.
Q0–Q8	Outputs	O	Data outputs for 9-bit wide data.

2677 tbl 01

STATUS FLAG

Number of Words in FIFO						
1K	2K	4K	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	0	H	L	H	L
1-127	1-255	1-511	H	L	H	H
128-512	256-1024	512-2048	H	H	H	H
513-896	1025-1792	2049-3584	H	H	L	H
897-1023	1793-2047	3585-4095	H	L	L	H
1024	2048	4096	L	L	L	H

2677 tbl I 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2677 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE: 2677 tbl 03

1. These parameters are sampled and not 100% tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTE: 2677 tbl 05

1. 1.5V undershoots are allowed for 10ns once per cycle.

5

DC ELECTRICAL CHARACTERISTICS — IDT72021

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72021 Commercial t_A =25,35ns			IDT72021 Military t_A =30,40ns			IDT72021 Commercial t_A =50ns			IDT72021 Military t_A =50ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[1]	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	–1	—	1	–10	—	10	µA
I_{LO}[2]	Output Leakage Current	–10	—	10	–10	—	10	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = –2mA	2.4	—	—	2.4	—	—	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	—	—	0.4	—	—	0.4	—	—	0.4	—	—	0.4	V
I_{CC1}[3,4]	Active Power Supply Current	—	—	120	—	—	140	—	50	80	—	70	100	mA
I_{CC2}[3]	Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})	—	—	12	—	—	20	—	5	8	—	8	15	mA
I_{CC3}[3]	Power Down Current (All Input = V_{CC} – 0.2V)	—	—	500	—	—	900	—	—	500	—	—	900	µA

2677 tbl 06

DC ELECTRICAL CHARACTERISTICS — IDT72031, IDT72041

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72031 IDT72041 Commercial t_A =35,50ns			IDT72031 IDT72041 Military t_A =40,50ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}[1]	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	µA
I_{LO}[2]	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}[3,5]	Active Power Supply Current	—	75	120	—	100	150	mA
I_{CC2}[3]	Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH})	—	8	12	—	12	25	mA
I_{CC3}[3]	Power Down Current (All Input = V_{CC} – 0.2V)	—	—	2	—	—	4	mA

2677 tbl 07

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. I_{CC} measurements are made with $\overline{OE}$ = HIGH.
4. Tested at f = 20MHz.
5. Tested at f = 15.3 MHz.

AC ELECTRICAL CHARACTERISTICS — IDT72021[1]

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = –55°C to +125°C)

		Com'l		Mil.		Com'l		Mil.		Com'l & Mil.		
		72021L25		72021L30		72021L35		72021L40		72021L50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Shift Frequency	—	28.5	—	25	—	22.2	—	20	—	15	MHz
tRC	$\overline{R}$ Cycle Time	35	—	40	—	45	—	50	—	65	—	ns
tA	Access Time	—	25	—	30	—	35	—	40	—	50	ns
tRR	$\overline{R}$ Recovery Time	10	—	10	—	10	—	10	—	15	—	ns
tRPW	$\overline{R}$ Pulse Width[2]	25	—	30	—	35	—	40	—	50	—	ns
tRLZ	$\overline{R}$ Pulse LOW to Data Bus at Low-Z[3]	5	—	5	—	5	—	5	—	10	—	ns
tWLZ	$\overline{W}$ Pulse HIGH to Data Bus at Low-Z[3,4]	5	—	5	—	5	—	5	—	5	—	ns
tDV	Data Valid from $\overline{R}$ Pulse HIGH	5	—	5	—	5	—	5	—	5	—	ns
tRHZ	$\overline{R}$ Pulse HIGH to Data Bus at High-Z[3]	—	18	—	20	—	20	—	25	—	30	ns
tWC	$\overline{W}$ Cycle Time	35	—	40	—	45	—	50	—	65	—	ns
tWPW	$\overline{W}$ Pulse Width[2]	25	—	30	—	35	—	40	—	50	—	ns
tWR	$\overline{W}$ Recovery Time	10	—	10	—	10	—	10	—	15	—	ns
tDS	Data Set-up Time	15	—	18	—	18	—	20	—	30	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	5	—	ns
tRSC	$\overline{RS}$ Cycle Time	35	—	40	—	45	—	50	—	65	—	ns
tRS	$\overline{RS}$ Pulse Width[2]	25	—	30	—	35	—	40	—	50	—	ns
tRSS	$\overline{RS}$ Set-up Time	25	—	30	—	35	—	40	—	50	—	ns
tRSR	$\overline{RS}$ Recovery Time	10	—	10	—	10	—	10	—	15	—	ns
tRTC	$\overline{RT}$ Cycle Time	35	—	40	—	45	—	50	—	65	—	ns
tRT	$\overline{RT}$ Pulse Width[2]	25	—	30	—	35	—	40	—	50	—	ns
tRTR	$\overline{RT}$ Recovery Time	10	—	10	—	10	—	10	—	15	—	ns
tRSF1	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ LOW	—	35	—	40	—	45	—	50	—	65	ns
tRSF2	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ HIGH	—	35	—	40	—	45	—	50	—	65	ns
tREF	$\overline{R}$ LOW to $\overline{EF}$ LOW	—	25	—	30	—	30	—	35	—	45	ns
tRFF	$\overline{R}$ HIGH to $\overline{FF}$ HIGH	—	25	—	30	—	30	—	35	—	45	ns
tRPE	$\overline{R}$ Pulse Width After $\overline{EF}$ HIGH	25	—	30	—	35	—	40	—	50	—	ns
tWEF	$\overline{W}$ HIGH to $\overline{EF}$ HIGH	—	25	—	30	—	30	—	35	—	45	ns
tWFF	$\overline{W}$ LOW to $\overline{EF}$ LOW	—	25	—	30	—	30	—	35	—	45	ns
tWHF	$\overline{W}$ LOW to $\overline{HF}$ LOW	—	35	—	40	—	45	—	50	—	65	ns
tRHF	$\overline{R}$ HIGH to $\overline{HF}$ HIGH	—	35	—	40	—	45	—	50	—	65	ns
tWPF	$\overline{W}$ Pulse Width after $\overline{FF}$ HIGH	25	—	30	—	35	—	40	—	50	—	ns
tRF	$\overline{R}$ HIGH to Transitioning $\overline{AEF}$	—	35	—	40	—	45	—	50	—	65	ns
tWF	$\overline{W}$ LOW to Transitioning $\overline{AEF}$	—	35	—	40	—	45	—	50	—	65	ns
tOEHZ	$\overline{OE}$ HIGH to High-Z (Disable)[3]	0	12	0	15	0	17	0	20	0	25	ns
tOELZ	$\overline{OE}$ LOW to Low-Z (Enable)[3]	0	12	0	15	0	17	0	20	0	25	ns
tAOE	$\overline{OE}$ LOW Data Valid (Q_0–Q_8)	—	15	—	18	—	20	—	25	—	30	ns

NOTES:

2677 tbl 08

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC ELECTRICAL CHARACTERISTICS — IDT72031, IDT72041[1]

(Commercial: V_{CC} = 5.0V±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V±10%, T_A = –55°C to +125°C)

		Com'l		Mil.		Com'l and Mil.		
		72031L35 72041L35		72031L40 72041L40		72031L50 72041L50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_S	Shift Frequency	—	22.2	—	20	—	15	MHz
t_{RC}	$\overline{R}$ Cycle Time	45	—	50	—	65	—	ns
t_A	Access Time	—	35	—	40	—	50	ns
t_{RR}	$\overline{R}$ Recovery Time	10	—	10	—	15	—	ns
t_{RPW}	$\overline{R}$ Pulse Width[2]	35	—	40	—	50	—	ns
t_{RLZ}	$\overline{R}$ Pulse LOW to Data Bus at Low-Z[3]	5	—	5	—	10	—	ns
t_{WLZ}	$\overline{W}$ Pulse HIGH to Data Bus at Low-Z[3,4]	5	—	5	—	5	—	ns
t_{DV}	Data Valid from $\overline{R}$ Pulse HIGH	5	—	5	—	5	—	ns
t_{RHZ}	$\overline{R}$ Pulse HIGH to Data Bus at High-Z[3]	—	20	—	25	—	30	ns
t_{WC}	$\overline{W}$ Cycle Time	45	—	50	—	65	—	ns
t_{WPW}	$\overline{W}$ Pulse Width[2]	35	—	40	—	50	—	ns
t_{WR}	$\overline{W}$ Recovery Time	10	—	10	—	15	—	ns
t_{DS}	Data Set-up Time	18	—	20	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	5	—	ns
t_{RSC}	$\overline{RS}$ Cycle Time	45	—	50	—	65	—	ns
t_{RS}	$\overline{RS}$ Pulse Width[2]	35	—	40	—	50	—	ns
t_{RSS}	$\overline{RS}$ Set-up Time	35	—	40	—	50	—	ns
t_{RSR}	$\overline{RS}$ Recovery Time	10	—	10	—	15	—	ns
t_{RTC}	$\overline{RT}$ Cycle Time	45	—	50	—	65	—	ns
t_{RT}	$\overline{RT}$ Pulse Width[2]	35	—	40	—	50	—	ns
t_{RTR}	$\overline{RT}$ Recovery Time	10	—	10	—	15	—	ns
t_{RSF1}	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ LOW	—	45	—	50	—	65	ns
t_{RSF2}	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ HIGH	—	45	—	50	—	65	ns
t_{REF}	$\overline{R}$ LOW to $\overline{EF}$ LOW	—	30	—	35	—	45	ns
t_{RFF}	$\overline{R}$ HIGH to $\overline{FF}$ HIGH	—	30	—	35	—	45	ns
t_{RPE}	$\overline{R}$ Pulse Width After $\overline{EF}$ HIGH	35	—	40	—	50	—	ns
t_{WEF}	$\overline{W}$ HIGH to $\overline{EF}$ HIGH	—	30	—	35	—	45	ns
t_{WFF}	$\overline{W}$ LOW to $\overline{EF}$ LOW	—	30	—	35	—	45	ns
t_{WHF}	$\overline{W}$ LOW to $\overline{HF}$ LOW	—	45	—	50	—	65	ns
t_{RHF}	$\overline{R}$ HIGH to $\overline{HF}$ HIGH	—	45	—	50	—	65	ns
t_{WPF}	$\overline{W}$ Pulse Width after $\overline{FF}$ HIGH	35	—	40	—	50	—	ns
t_{RF}	$\overline{R}$ HIGH to Transitioning $\overline{AEF}$	—	45	—	50	—	65	ns
t_{WF}	$\overline{W}$ LOW to Transitioning $\overline{AEF}$	—	45	—	50	—	65	ns
t_{OEHZ}	$\overline{OE}$ HIGH to High-Z (Disable)[3]	0	17	0	20	0	25	ns
t_{OELZ}	$\overline{OE}$ LOW to Low-Z (Enable)[3]	0	17	0	20	0	25	ns
t_{AOE}	$\overline{OE}$ LOW Data Valid (Q_0–Q_8)	—	20	—	25	—	30	ns

NOTES:

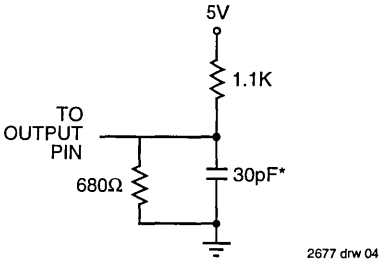
2677 tbl 09

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2677 tbl 10



or equivalent circuit

Figure 1. Output Load

* Includes scope and jig capacitances.

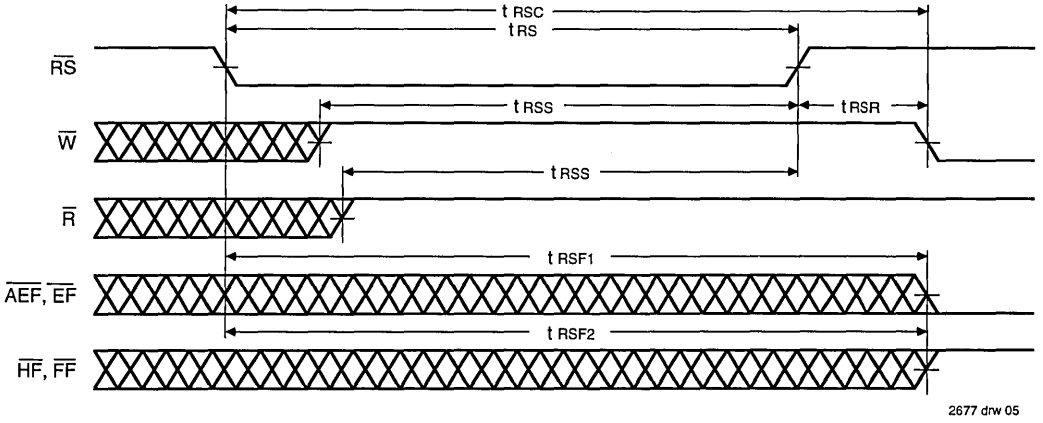


Figure 2. Reset

NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$, and $\overline{AEF}$ may change status during Reset, but flags will be valid at tRSC.
2. $\overline{W}$ and $\overline{R}$ = VIH around the rising edge of $\overline{RS}$.

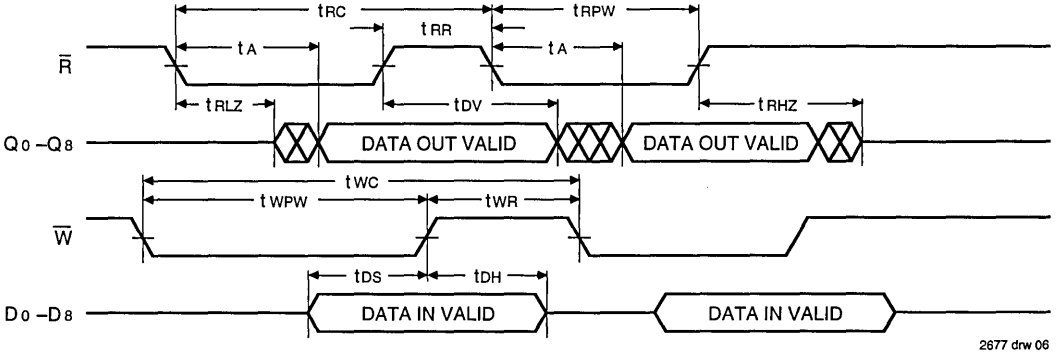


Figure 3. Asynchronous Write and Read Operation

NOTE:
1. Assume $\overline{OE}$ is asserted LOW.

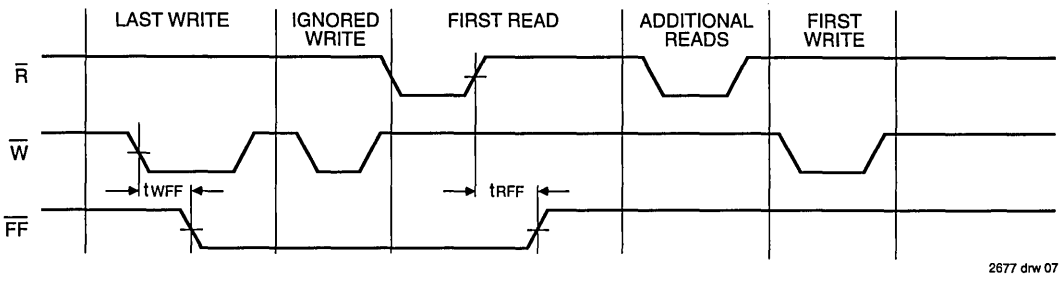


Figure 4. Full Flag From Last Write to First Read

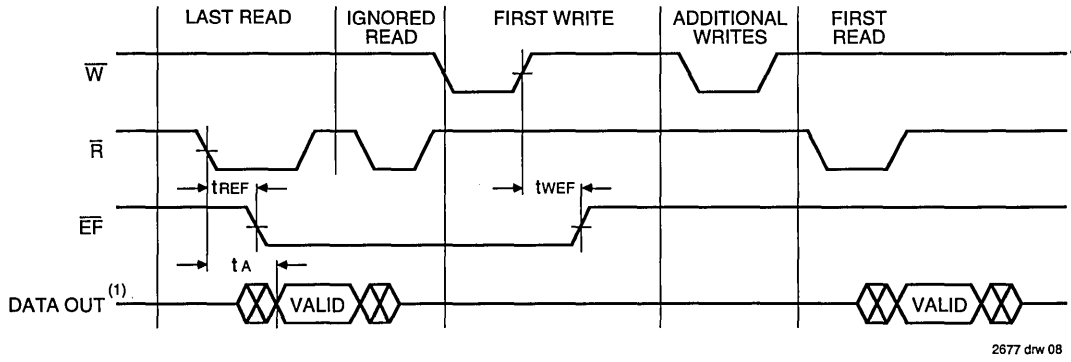


Figure 5. Empty Flag From Last Read to First Write

NOTE:
1. Assume $\overline{OE}$ is asserted LOW.

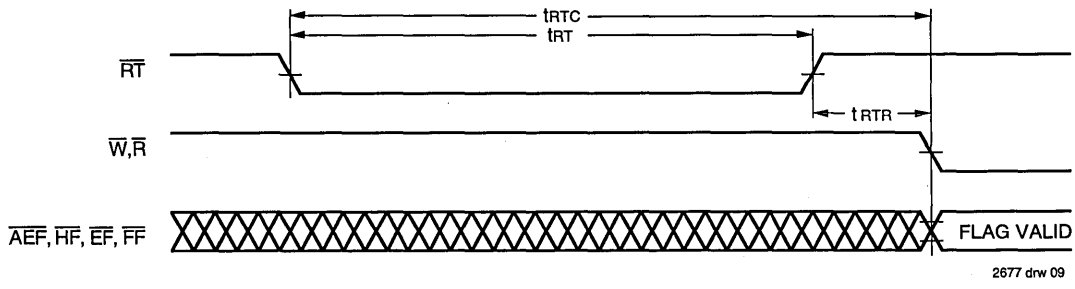


Figure 6. Retransmit

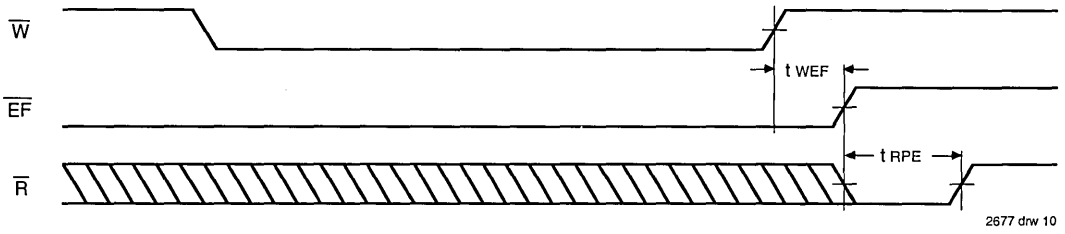


Figure 7. Empty Flag Timing
Figure 9. Almost-Empty/Almost-Full Flag and Half-Full Timings

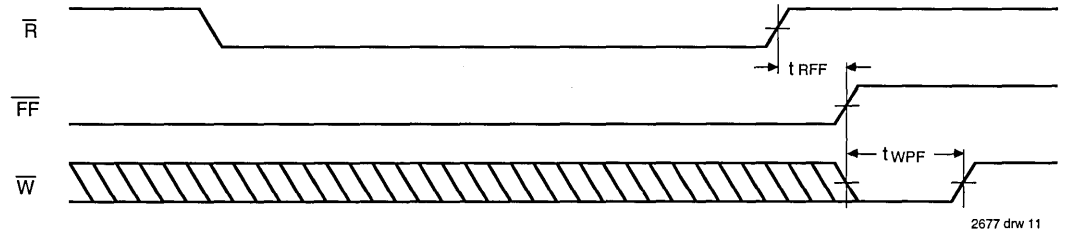


Figure 8. Full Flag Timing

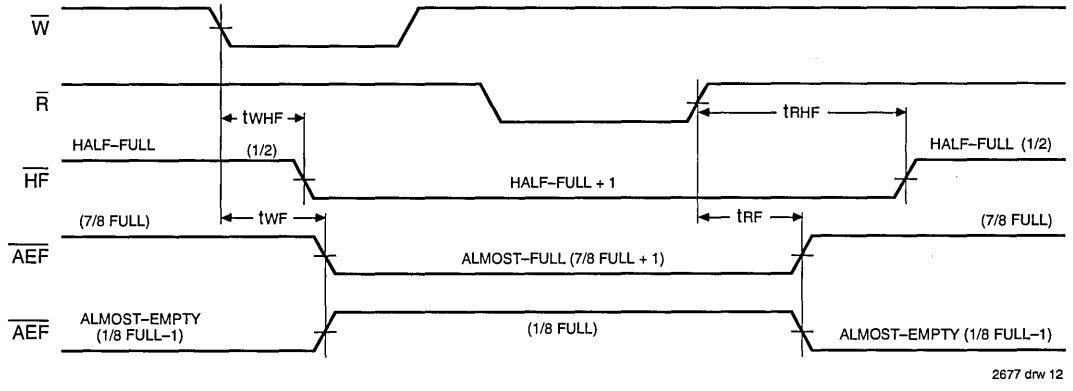


Figure 9. Almost-Empty/Almost-Full Flag and Half-Full Timings

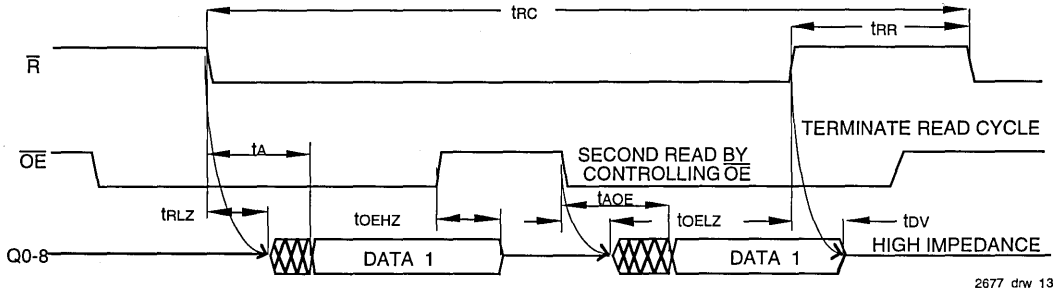


Figure 10. Output Enable and Read Operation Timings

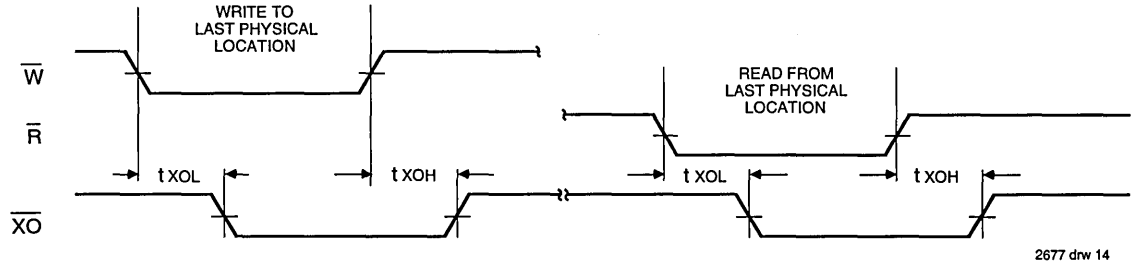


Figure 11. Expansion Out

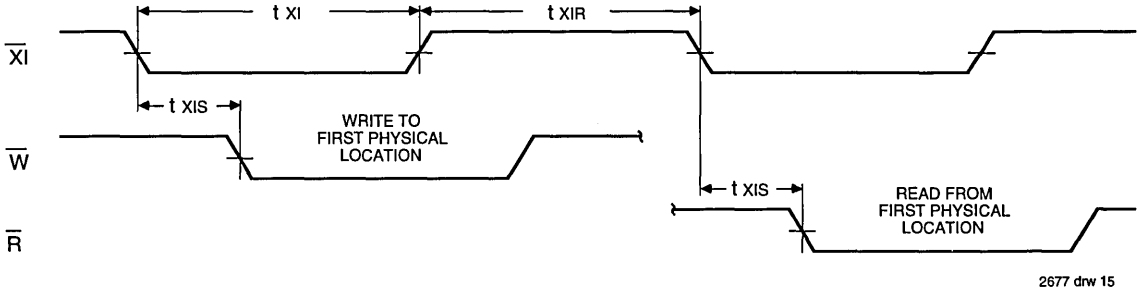


Figure 12. Expansion In

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

The IDT72021/031/041 is in the Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 13).

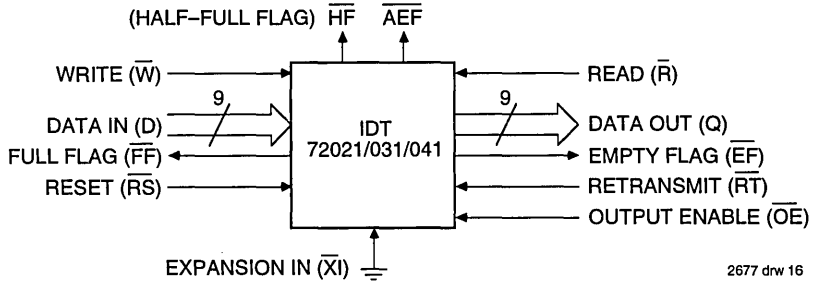


Figure 13. Block Diagram of Single 1K/2K/4K x 9 FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$, $\overline{HF}$, and $\overline{AEF}$) can be detected from any one device. Figure 14 demonstrates an 18-bit word width by using two IDT72021/031/041 devices. Any word width can be attained by adding additional IDT72021/031/041s.

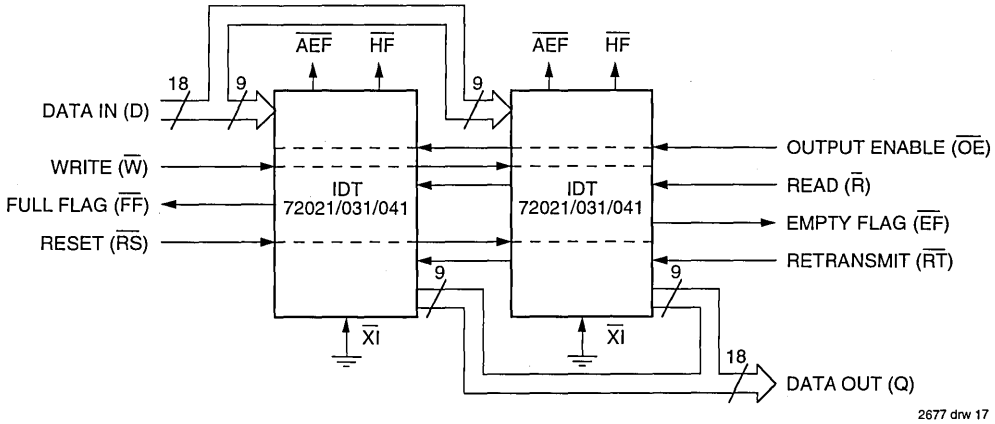


Figure 14. Block Diagram of 1K/2K/4K x 18 FIFO Memory Used in Width Expansion Configuration

NOTE:
1. Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, $\overline{HF}$ and $\overline{AEF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output signals together.

5

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT72021/031/041 can easily be adapted to applications when the requirements are for greater than 1K/2K/4K words. Figure 15 demonstrates Depth Expansion using three IDT72021/031/041s. Any depth can be attained by adding additional devices. The IDT72021/031/041 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designed by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 15.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 15.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode. For additional information refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays (see Figure 16).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72021/031/041s as shown in Figure 17. Care must be taken to assure that the appropriate flag is monitored by each system (i.e., $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 18), the FIFO permits the reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge. It remains on the bus until the $\overline{R}$ line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that $\overline{R}$ was LOW, more words can be written to the FIFO (the subsequent writes after the first write edge will be deassert the Empty Flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ was LOW. On toggling $\overline{R}$, the other words that are written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line, being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

TRUTH TABLES
TABLE I—RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs			
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$	$\overline{AEF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1	0
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X	X

NOTE:
1. Pointer will increment if flag is HIGH.

2677 tbl 11

TABLE II—RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 15. $\overline{RS}$ = Reset Input $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Flag Full Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output, $\overline{AEF}$ = Almost Empty/Almost Full Flag.

2677 tbl 12

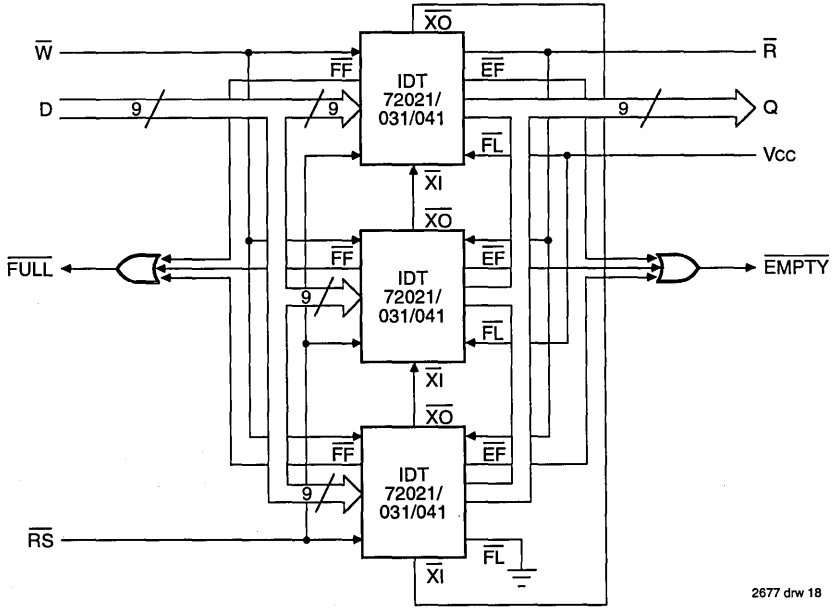


Figure 15. Block Diagram of 3K/6K/12K x 9 FIFO Memory (Depth Expansion)

NOTE:
1. IDT only guarantees depth expansion with identical IDT part numbers and speed.

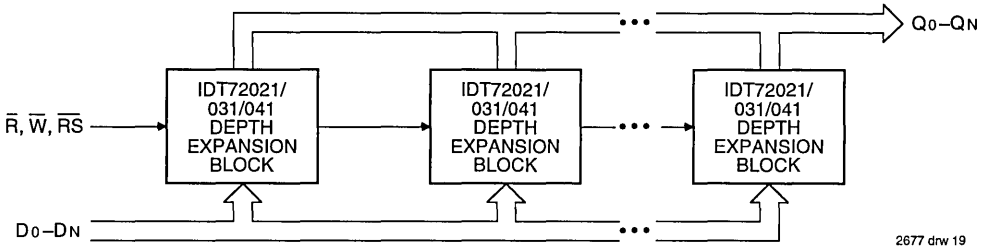


Figure 16. Compound FIFO Expansion

NOTES:
1. For depth expansion block see section od Depth Expansion and Figure 15.
2. For Flag detection see section on Width Expansion and Figure 14.

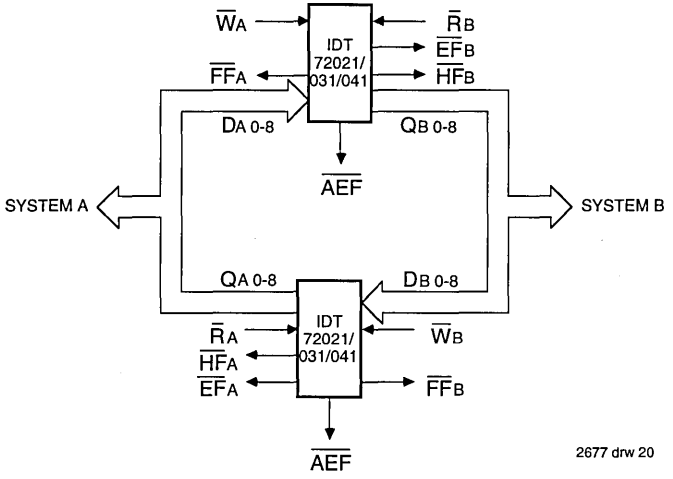


Figure 17. Bidirectional FIFO Mode

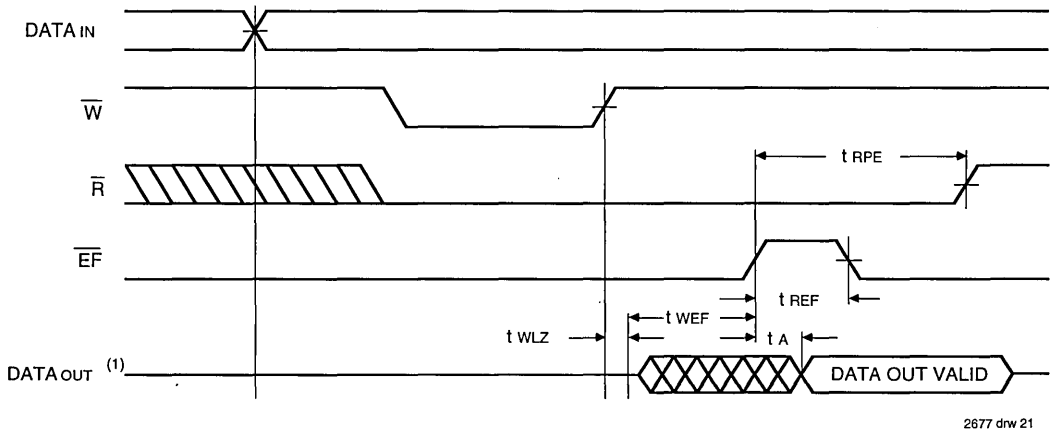


Figure 18. Read Data Flow-Through Mode

NOTE:
1. Assume $\overline{OE}$ is asserted LOW.

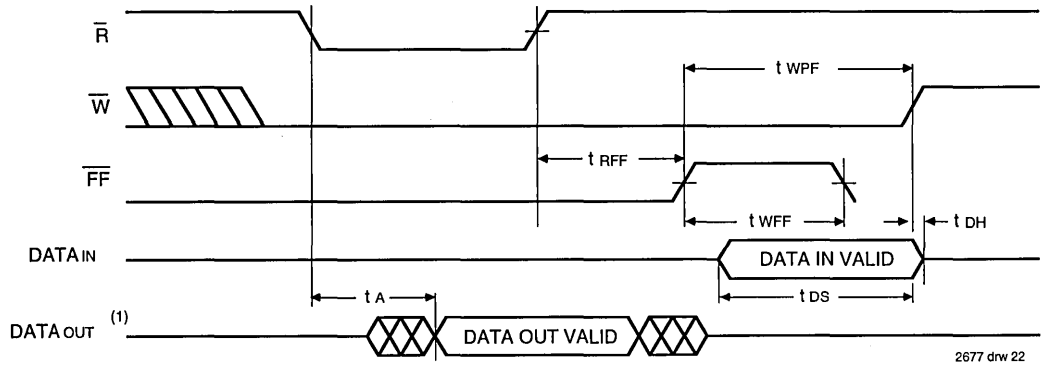
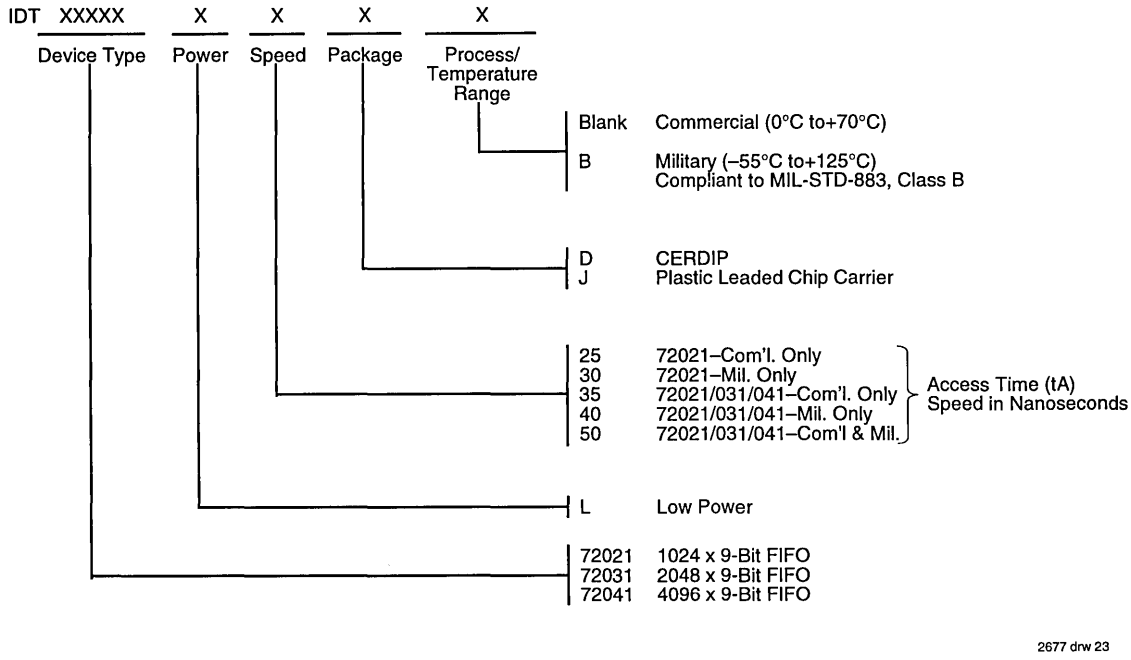


Figure 19. Write Data Flow-Through Mode

NOTE:
1. Assume $\overline{OE}$ is asserted LOW.

ORDERING INFORMATION



Integrated Device Technology, Inc.

CMOS PARALLEL-SERIAL FIFO 2048 x 9, 4096 x 9

IDT72103
IDT72104

FEATURES:

- 35ns parallel port access time, 45ns cycle time
- 50MHz serial input/output frequency
- Serial-to-parallel, parallel-to-serial, serial-to-serial, and parallel-to-parallel operations
- Expandable in both depth and width with no external components
- Flexishift™ — Sets programmable serial word width from 4 bits to any width with no external components
- Multiple flags: Full, Almost-Full (Full-1/8),Full-Minus-One, Empty, Almost-Empty (Empty + 1/8), Empty-Plus One, and Half-Full
- Asynchronous and simultaneous read or write operations
- Dual-Port, zero fall-through time architecture
- Retransmit capability in single-device mode
- Packaged in 40-pin ceramic and plastic DIP, 44-pin PLCC
- Military product compliant to MIL-STD-883, Class B

APPLICATIONS:

- High-speed data acquisition systems
- Local area network (LAN) buffer
- High-speed modem data buffer
- Remote telemetry data buffer
- FAX raster video data buffer
- Laser printer engine data buffer
- High-speed parallel bus-to-bus communications
- Magnetic media controllers
- Serial link buffer

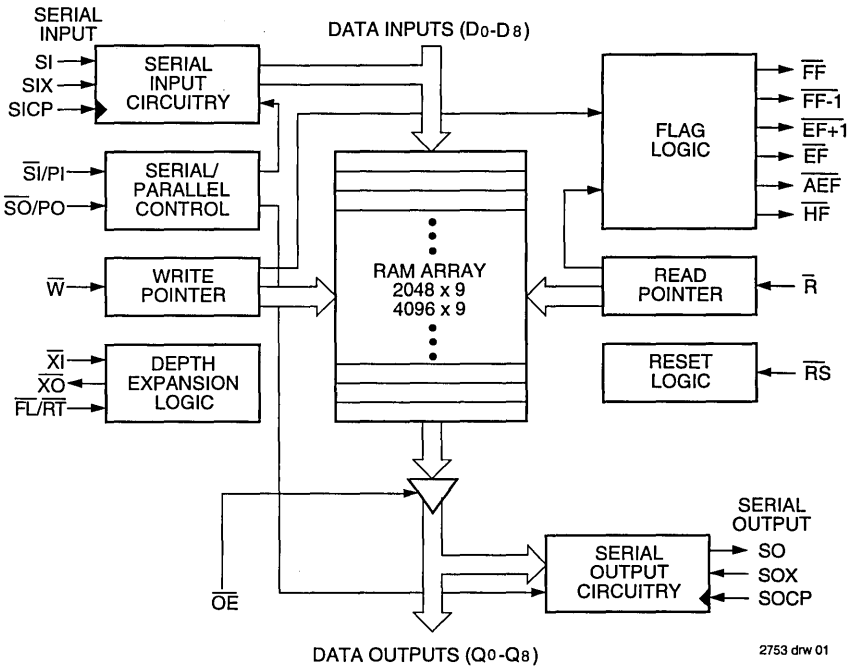
DESCRIPTION:

The IDT72103/72104 are high-speed Parallel-Serial FIFOs to be used with high-performance systems for functions such as serial communications, laser printer engine control and local area networks.

A serial input, a serial output and two 9-bit parallel ports make four modes of data transfer possible: serial-to-parallel, parallel-to-serial, serial-to-serial, and parallel-to-parallel. The IDT72103/72104 are expandable in both depth and width for all of these operational configurations.

5

FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark of Integrated Device Technology,Inc.

DESCRIPTION (CONTINUED)

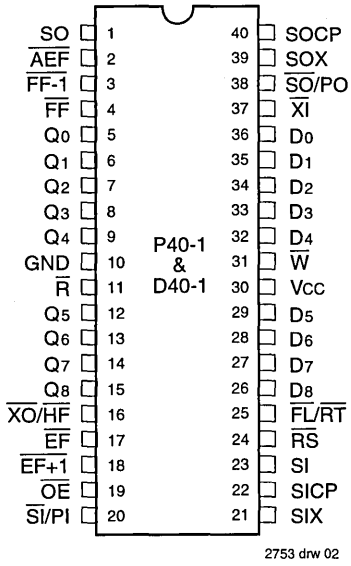
The IDT72103/72104 may be configured to handle serial word widths of four or greater using IDT's unique Flexishift feature. Flexishift allows serial width and depth expansion without external components. For example, you may configure a 4K x 24 FIFO using three IDT72104s in a serial width expansion configuration.

Seven flags are provided to signal memory status of the FIFO. The flags are $\overline{FF}$ (Full), $\overline{AF}$ (7/8 full), $\overline{FF-1}$ (Full-minus-one), $\overline{EF}$ (Empty), $\overline{AE}$ (1/8 full), $\overline{EF+1}$ (Empty-plus-one), and $\overline{HF}$ (Half-full).

Read ($\overline{R}$) and Write ($\overline{W}$) control pins are provided for asynchronous and simultaneous operations. An output enable ($\overline{OE}$) control pin is available on the parallel output port for high-impedance control. The depth expansion control pins $\overline{XO}$ and $\overline{XI}$ are provided to allow cascading for deeper FIFOs.

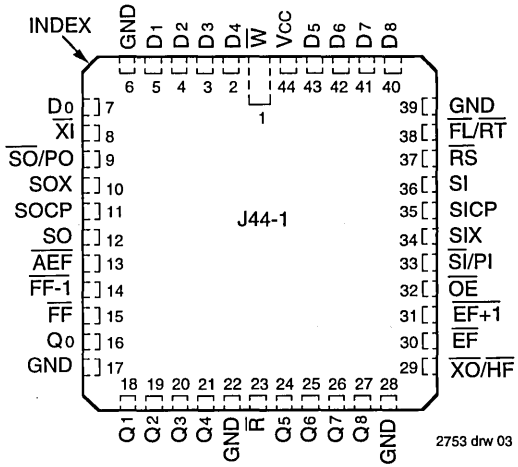
The IDT72103/72104 are manufactured using IDT's CMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

PIN CONFIGURATIONS



2753 drw 02

DIP
TOP VIEW



2753 drw 03

PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +155	°C
IOUT	DC Output Current	50	50	mA

NOTE: 2753 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	12	pF

NOTE: 2753 tbl 02

1. This parameter is sampled and not 100% tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial	2.0	—	—	V
VIH	Input High Voltage Military	2.2	—	—	V
VIL(1)	Input Low Voltage	—	—	0.8	V

NOTE: 2753 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

5

PIN DESCRIPTION

Symbol	Name	I/O	Description
D0-D8	Data Inputs Serial Input Word Width Select	I/O	In a parallel input configuration – data inputs for 9-bit wide data. In a serial input configuration – one of the nine output pins is used to select the serial input word width.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{EF}$, $\overline{EF+1}$, $\overline{AEF}$ are all LOW after a reset, while $\overline{FF}$, $\overline{FF-1}$, $\overline{HF}$ are HIGH after a reset.
$\overline{W}$	Write	I	A parallel word write cycle is initiated on the falling edge of $\overline{W}$ if the $\overline{FF}$ is high. When the FIFO is full, FF will go low inhibiting further write operations to prevent data overflow. In a serial input configuration, data bits are clocked into the input shift register and the write pointer does not advance until a full parallel word is assembled. One of the pins, Di, is connected to $\overline{W}$ and advances the write pointer every i-th serial input clock.
$\overline{R}$	Read	I	A read cycle is initiated on the falling edge of $\overline{R}$ if the $\overline{EF}$ is HIGH. After all the data from the FIFO has been read $\overline{EF}$ will go LOW inhibiting further read operations. In a serial output configuration, a data word is read from memory into the output shift register. One of the pins, Qj, is connected to $\overline{R}$ and advances the read pointer every j-th serial output clock.
$\overline{FL/RT}$	First Load/ Retransmit	I	This is a dual-purpose pin. In multiple-device mode, $\overline{FL/RT}$ is grounded to indicate the first device loaded. In single-device mode, $\overline{FL/RT}$ acts as the retransmit input. Single-device mode is initiated by grounding the $\overline{XI}$ pin.
$\overline{XI}$	Expansion In	I	In single-device mode, $\overline{XI}$ is grounded.In depth expansion or daisy chain mode, $\overline{XI}$ is connected to the $\overline{XO}$ pin of the previous device.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, both parallel and serial outputs are enabled. When $\overline{OE}$ is HIGH, the parallel output buffers are placed in a high-impedance state.
Q0-Q8	Data Outputs / Serial Output Word Width Select	O	In a parallel output configuration - data outputs for 9-bit wide data. In a serial output configuration - one of nine output pins used to select the serial output word width.
$\overline{FF}$	Full Flag	O	$\overline{FF}$ is asserted LOW when the FIFO is full and further write operations are inhibited. When the $\overline{FF}$ is HIGH, the FIFO is not full and data can be written into the FIFO.
$\overline{FF-1}$	Full-1 Flag	O	$\overline{FF-1}$ goes LOW when the FIFO memory array is one word away from being full. It will remain LOW when every memory location is filled.

2753 tbl 04

PIN DESCRIPTION (Continued)

Symbol	Name	I/O	Description
$\overline{XO}/\overline{HF}$	Expansion Out/ Half-Full Flag	O	$\overline{HF}$ is LOW when the FIFO is more than half-full in the single device or width expansion modes. The $\overline{HF}$ will remain LOW until the difference between the write and read pointers is less than or equal to one-half of the FIFO memory. In depth expansion mode, a pulse is written from $\overline{XO}$ to $\overline{XI}$ of the next device when the last location in the FIFO is filled. Another pulse is sent from $\overline{XO}$ to $\overline{XI}$ of the next device when the last FIFO location is read.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is LOW, the FIFO is empty to 1/8 full or 7/8 full to completely full. If $\overline{AEF}$ is HIGH, then the FIFO is greater than 1/8 full, but less than 7/8 full.
$\overline{EF+1}$	Empty+1 Flag	O	$\overline{EF+1}$ is LOW when there is zero or one word word in the FIFO memory array.
$\overline{EF}$	Empty Flag	O	$\overline{EF}$ goes LOW when the FIFO is empty and further read operations are inhibited. $\overline{FF}$ is HIGH when the FIFO is not empty and data reads are permitted.
SI	Serial Input	I	Data input for serial data.
SO	Serial Output	O	Data output for serial data.
SICP	Serial Input Clock	I	This pin is the serial input clock. On the rising edge of the SICP signal, new serial data bits are read into the serial input shift register.
SOCP	Serial Output Clock	I	This pin is the serial output clock. On the rising edge of the SOCP signal, new serial data bits are read from the serial output shift register.
SIX	Serial Input Expansion	I	SIX controls the serial input expansion for word widths greater than 9 bits. In a serial input configuration, the SIX pin of the least significant device is tied HIGH. The SIX pin of all other devices is connected to the D_8 pin of the previous device. In parallel input configurations or serial input configurations of 9 bits or less, SIX is tied HIGH.
SOX	Serial Output Expansion	I	SOX controls the serial output expansion for word widths greater than 9 bits. In a serial output configuration, the SOX pin of the least significant device is tied HIGH. The SOX pin of all other devices is connected to the Q_8 pin of the previous device. In parallel output configurations or serial output configurations of 9 bits or less, SOX is tied HIGH.
$\overline{SI}$/PI	Serial/Parallel Input	I	When this pin is HIGH, the FIFO is in a parallel input configuration and accepts input data through D_0-D_8. When $\overline{SI}$/PI is LOW, the FIFO is in a serial input configuration and data is input through SI.
$\overline{SO}$/PO	Serial/Parallel Output	I	When this pin is HIGH, the FIFO is in a parallel output configuration and sends output data through Q_0-Q_8. When $\overline{SO}$/PO is LOW the FIFO is in a serial output configuration and data is input through SO.
GND	Ground		One ground pin for the DIP package and five ground pins for the LCC/PLCC packages.
Vcc	Power		One + 5V power pin.

2753 tbl 05

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = −55°C to +125°C)

Symbol	Parameter	IDT72103/72104 Commercial t_A = 35, 50ns			IDT72103/72104 Military t_A = 40, 50ns			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}[1]	Input Leakage Current (Any Input)	−1	—	1	−10	—	10	µA
I_{OL}[2]	Output Leakage Current	−10	—	10	−10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OUT} = -2mA[4]	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OUT} = 8mA[5]	—	—	0.4	—	—	0.4	V
I_{CC1}[3]	Average Vcc Power Supply Current	—	90	140	—	100	160	mA
I_{CC2}[3]	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (SOCP = SICP = V_{IL})	—	8	12	—	12	25	mA
$I_{CC3(L)}$[3,6]	Power Down Current	—	—	2	—	—	4	mA

NOTES:

2753 tbl 06

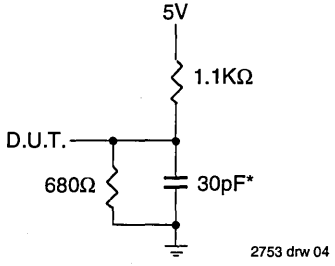
1. Measurements with 0.4 ≤ V_{IN} ≤ Vcc.
2. $\overline{R}$ ≥ V_{IH}, SOCP ≤ V_{IL}, 0.4 ≤ V_{OUT} ≤ Vcc.
3. Icc measurements are made with outputs open.
4. For SO, I_{OUT} = -8mA.
5. For SO, I_{OUT} =16mA.
6. SOCP = SICP ≤ 0.2V; other Inputs = Vcc -0.2V.

5

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2753 tbl 07



2753 drw 04

or equivalent circuit

Figure 1. Ouput Load

*Including jig and scope capacitances

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = –55°C to +125°C)

		Commercial		Military		Mil. and Com'l.			
		IDT72103L35 IDT72104L35		IDT72103L40 IDT72104L40		IDT72103L50 IDT72104L50			Timing
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Figure
f_S	Parallel Shift Frequency	—	22.2	—	20	—	15	MHz	—
f_{SOCP}	Serial-Out Shift Frequency	—	50	—	50	—	40	MHz	—
f_{SICP}	Serial-In Shift Frequency	—	50	—	50	—	40	MHz	—
PARALLEL-OUTPUT MODE TIMINGS									
t_A	Access Time	—	35	—	40	—	50	ns	4
t_{RR}	Read Recovery Time	10	—	10	—	15	—	ns	4
t_{RPW}	Read Pulse Width	35	—	40	—	50	—	ns	4
t_{RC}	Read Cycle Time	45	—	50	—	65	—	ns	4
t_{WLZ}	Write Pulse LOW to Data Bus at Low-Z[1]	5	—	5	—	15	—	ns	15
t_{RLZ}	Read Pulse LOW to Data Bus at Low-Z[1]	5	—	5	—	10	—	ns	4
t_{RHZ}	Read Pulse HIGH to Data Bus at High-Z[1]	—	20	—	25	—	30	ns	4
t_{DV}	Data Valid from Read Pulse HIGH	5	—	5	—	5	—	ns	4
PARALLEL-INPUT MODE TIMINGS									
t_{DS}	Data Set-up Time	18	—	20	—	30	—	ns	3
t_{DH}	Data Hold Time	0	—	0	—	5	—	ns	3
t_{WC}	Write Cycle Time	45	—	50	—	65	—	ns	3
t_{WPW}	Write Pulse Width	35	—	40	—	50	—	ns	3
t_{WR}	Write Recovery Time	10	—	10	—	15	—	ns	3
RESET TIMINGS									
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	ns	2,18
t_{RS}	Reset Pulse Width	35	—	40	—	50	—	ns	2,18
t_{RSS}	Reset Set-up Time	35	—	40	—	50	—	ns	2,18
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	ns	2,17,18
RESET TO FLAG TIMINGS									
t_{RSF1}	Reset to $\overline{EF}$, $\overline{AEF}$, and $\overline{EF+1}$ LOW	—	45	—	50	—	65	ns	2
t_{RSF2}	Reset to $\overline{HF}$, $\overline{FF}$, and $\overline{FF-1}$ LOW	—	45	—	50	—	65	ns	2
RESET TO OUTPUT TIMINGS – SERIAL MODE ONLY									
t_{RSQL}	Reset Going LOW to Q_{0-8} LOW	20	—	20	—	35	—	ns	18
t_{RSQH}	Reset Going HIGH to Q_{0-8} HIGH	20	—	20	—	35	—	ns	18
t_{RSDL}	Reset Going LOW to D_{0-8} LOW	20	—	20	—	35	—	ns	17
RETRANSMIT TIMINGS									
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	ns	5
t_{RT}	Retransmit Pulse Width	35	—	40	—	50	—	ns	5
t_{RTS}	Retransmit Set-up Time	35	—	40	—	50	—	ns	5
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	ns	5
t_{RTF}	Retransmit to Flags	—	35	—	40	—	50	ns	5
PARALLEL MODE FLAG TIMINGS									
t_{REF}	Read LOW to $\overline{EF}$ LOW	—	30	—	35	—	45	ns	6
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH	—	30	—	35	—	45	ns	7
t_{RF}	Read HIGH to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	—	45	—	50	—	65	ns	8,9,10
t_{RE}	Read LOW to $\overline{EF+1}$ LOW	—	45	—	45	—	65	ns	11
t_{RPE}	Read Pulse Width after $\overline{EF}$ HIGH	35	—	40	—	50	—	ns	15
t_{WEF}	Write HIGH to $\overline{EF}$ HIGH	—	30	—	35	—	45	ns	6
t_{WFF}	Write LOW to $\overline{FF}$ LOW	—	30	—	35	—	45	ns	7
t_{WF}	Write LOW to Transitioning $\overline{HF}$, $\overline{AEF}$ and $\overline{FF-1}$	—	45	—	50	—	65	ns	8,9,10
t_{WE}	Write HIGH to $\overline{EF+1}$ HIGH	—	45	—	50	—	65	ns	11
t_{WPF}	Write Pulse Width after $\overline{FF}$ HIGH	35	—	40	—	50	—	ns	16

NOTE:
1. Values guaranteed by design, not tested.

2753 tbl 08

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	Commercial IDT72103L35 IDT72104L35 Min.	Commercial IDT72103L35 IDT72104L35 Max.	Military IDT72103L40 IDT72104L40 Min.	Military IDT72103L40 IDT72104L40 Max.	Mil. and Com'l. IDT72103L50 IDT72104L50 Min.	Mil. and Com'l. IDT72103L50 IDT72104L50 Max.	Unit	Timing Figure
DEPTH EXPANSION MODE TIMINGS									
t_{XOL}	Read/Write to $\overline{XO}$ LOW	—	35	—	40	—	50	ns	13
t_{XOH}	Read/Write to $\overline{XO}$ HIGH	—	35	—	40	—	50	ns	13
t_{XI}	$\overline{XI}$ Pulse Width	35	—	40	—	50	—	ns	14
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns	14
t_{XIS}	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns	14
SERIAL-INPUT MODE TIMINGS									
t_{S2}	Serial Data In Set-up Time to SICP Rising Edge	12	—	12	—	15	—	ns	19
t_{H2}	Serial Data In Hold Time to SICP Rising Edge	0	—	0	—	0	—	ns	19
t_{S3}	SIX Set-up Time to SICP Rising Edge	5	—	5	—	5	—	ns	19
t_{S4}	$\overline{W}$ Set-up Time to SICP Rising Edge	5	—	5	—	5	—	ns	19
t_{H4}	$\overline{W}$ Hold Time to SICP Rising Edge	7	—	7	—	7	—	ns	19
t_{SICW}	Serial In Clock Width High/Low	8	—	8	—	10	—	ns	19
t_{S5}	SI/PI Set-up Time to SICP Rising Edge	35	—	40	—	50	—	ns	19
SERIAL-OUTPUT MODE TIMINGS									
t_{S6}	SO/PO Set-up Time to SOCP Rising Edge	35	—	40	—	50	—	ns	20
t_{S7}	SOX Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns	20
t_{S8}	$\overline{R}$ Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns	20
t_{H8}	$\overline{R}$ Hold Time to SOCP Rising Edge	7	—	7	—	7	—	ns	20
t_{SOCW}	Serial Out Clock Width HIGH/LOW	8	—	8	—	10	—	ns	20
SERIAL MODE RECOVERY TIMINGS									
t_{REFSO}	Recovery Time SOCP after $\overline{EF}$ Goes HIGH	35	—	40	—	80	—	ns	22
t_{RFFSI}	Recovery Time SICP after $\overline{FF}$ Goes HIGH	15	—	15	—	15	—	ns	23
SERIAL MODE FLAG TIMINGS									
t_{SOCEF}	SOCP Rising Edge (Bit 0- Last Word) to $\overline{EF}$ LOW	—	20	—	25	—	25	ns	22
t_{SOCFF}	SOCP Rising Edge (Bit 0- First Word) to $\overline{FF}$ HIGH	—	30	—	35	—	40	ns	24
t_{SOCF}	SOCP Rising Edge to $\overline{FF-1}$, $\overline{HF}$, $\overline{AEF}$ HIGH	—	30	—	35	—	40	ns	24,26
t_{SOCF}	SOCP Rising Edge to $\overline{AEF}$, $\overline{EF}$, $\overline{EF+1}$ LOW	—	30	—	35	—	40	ns	22,26
t_{SICEF}	SICP Rising Edge (Last Bit-First Word) to $\overline{EF}$ HIGH	—	45	—	50	—	65	ns	21
t_{SICFF}	SICP Rising Edge (Bit 1-Last Word) to $\overline{FF}$ LOW	—	30	—	35	—	40	ns	23
t_{SICF}	SICP Rising Edge to $\overline{EF+1}$, $\overline{AEF}$ HIGH	—	45	—	50	—	65	ns	21,25
t_{SICF}	SICP Rising Edge to $\overline{FF-1}$, $\overline{HF}$, $\overline{AEF}$ HIGH	—	45	—	50	—	65	ns	23,25
SERIAL-INPUT MODE TIMINGS									
t_{PD1}	SICP Rising Edge to D[1]	5	17	5	17	5	20	ns	17,19
SERIAL-OUTPUT MODE TIMINGS									
t_{PD2}	SOCP Rising Edge to Q[1]	5	17	5	17	5	20	ns	20
t_{SOHZ}	SOCP Rising Edge to SO at High-Z[1]	5	16	5	16	5	16	ns	20
t_{SOLZ}	SOCP Rising Edge to SO at Low-Z[1]	5	22	5	22	5	22	ns	20
t_{SOPD}	SOCP Rising Edge to Valid Data on SO	—	18	—	18	—	18	ns	20
OUTPUT ENABLE/DISABLE TIMINGS									
t_{OEHZ}	Output Enable to High-Z (Disable)[1]	—	16	—	16	—	16	ns	12
t_{OELZ}	Output Enable to Low-Z (Enable)[1]	5	—	5	—	5	—	ns	12
t_{AOE}	Output Enable to Data Valid (Q_{0-8})	—	20	—	20	—	22	ns	12

NOTE:
1. Values guaranteed by design, not tested.

2753 tbl 09

5

GENERAL SIGNAL DESCRIPTION

INPUTS:

Data Inputs (D_0-D_8)

The parallel-in mode is selected by connecting the $\overline{SI}$/PI pin to Vcc. D_0-D_8 are the data input lines.

The serial-input mode is selected by grounding the $\overline{SI}$/PI pin. The D_0-D_8 lines are control output pins used to program the serial word width.

Reset ($\overline{RS}$)

Reset is accomplished whenever the $\overline{RS}$ input is taken to a low state. Both internal read and write pointers are set to the first location during reset. A reset is required after power up before a write operation can take place. Both Read ($\overline{R}$) and Write ($\overline{W}$) inputs must be HIGH during reset.

Write ($\overline{W}$)

A write cycle is initiated on the falling edge of $\overline{W}$ provided the Full Flag ($\overline{FF}$) is not asserted. Data set-up and hold times must be met with respect to the rising edge of $\overline{W}$. Data is stored in the RAM array sequentially and independently of any on going read operation.

When the FIFO is full, the $\overline{FF}$ will go LOW inhibiting further write operations to prevent data overflow. After a valid read operation is completed, the $\overline{FF}$ will go HIGH after t_{RFF} allowing a valid write to begin.

Read ($\overline{R}$)

A read cycle is initiated on the falling edge of $\overline{R}$, provided the $\overline{EF}$ is not set. Data is accessed on a first-in/first out basis independent of any on going write operations. After $\overline{R}$ goes HIGH, the Data Outputs (Q_0-Q_8) go to a high-impedance condition until the next read operation. When all the data has been read from the FIFO, the $\overline{EF}$ will go LOW, and Q_0-Q_8 will go to a high-impedance state inhibiting further read operations. After the completion of a valid write operation, the $\overline{EF}$ will go HIGH after t_{WEF} allowing a valid read to begin.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

In the depth-expansion mode, the $\overline{FL}/\overline{RT}$ pin is grounded to indicate that it is the first device loaded. In the single-device mode, the $\overline{FL}/\overline{RT}$ pin acts as the retransmit input. The single-device mode is initiated by grounding the Expansion-In ($\overline{XI}$) pin.

The IDT72103/72104 can be made to retransmit data when the $\overline{RT}$ input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. During retransmit, $\overline{R}$ and $\overline{W}$ must be set HIGH and the $\overline{FF}$ will be affected depending on the relative locations of the read and write pointers. This feature is useful when less than 2048/4096 writes are performed between resets. The retransmit feature is not available in the depth expansion mode.

Expansion In ($\overline{XI}$)

The $\overline{XI}$ pin is grounded to indicate an operation in the the single-device mode. In the depth expansion or daisy-chain mode, the $\overline{XI}$ pin is connected to the $\overline{XO}$ pin of the previous device.

Output Enable ($\overline{OE}$)

When $\overline{OE}$ is HIGH, the parallel output buffers are tristated. When $\overline{OE}$ is LOW, both parallel and serial outputs are enabled.

Serial Input (SI)

Serial data is read into the serial input register via the SI pin. In both depth and serial width expansion modes, the serial-input signals of the different FIFOs in the expansion array are connected together.

Serial Input Clock (SICP)

Serial data is read into the serial input register on the rising edge of the SICP signal. In both depth and serial width expansion modes, the SICP signals of the different FIFOs in the expansion array are connected together.

Serial Output Clock (SOCP)

New serial data bits are read from the serial output register on the rising edge of the SOCP signal. In both depth and serial width expansion modes, the SOCP signals of the different FIFOs in the expansion array are connected together.

Serial Input Expansion (SIX)

The SIX pin is tied HIGH for single-device serial or parallel input operation. In a serial input configuration, the SIX pin of the least significant device is tied HIGH. The SIX pin of all other devices is connected to the D_8 pin of the previous device.

Serial Output Expansion (SOX)

The SOX pin is tied HIGH for single-device serial or parallel output operation. In a serial output configuration, the SOX pin of the least significant device is tied HIGH. The SOX pin of all other devices is connected to the Q_8 pin of the previous device.

Serial/Parallel Input ($\overline{SI}$/PI)

The $\overline{SI}$/PI pin programs whether the IDT72103/72104 accepts parallel or serial data as input. When this pin is LOW, the FIFO expects serial data and the D_0-D_8 pins become output pins used to program the write signal and the serial input word width. For instance, connecting D_8 to $\overline{W}$ will program a serial word width of 9 bits; connecting D_7 to $\overline{W}$ will program a serial word width of 8 bits and so on.

Serial/Parallel Output ($\overline{SO}$/PO)

The $\overline{SO}$/PO pin programs whether the IDT72103/72104 outputs parallel or serial data. When this pin is LOW, the FIFO expects serial data and the Q_0-Q_8 pins output signals used to

program the read signal and the serial output word width.

OUTPUTS:

Data Outputs (Q_0–Q_8)

Data outputs for 9-bit wide data. These output lines are in a high-impedance condition whenever $\overline{R}$ is in a high state. The serial output mode is selected by grounding the $\overline{SO}$/PO pin. The Q_0-Q_8 lines are control pins used to program the serial word width.

Serial Output (SO)

Serial data is output on the SO pin. In both depth and serial width expansion modes the serial output signals of the different FIFOs in the expansion array are connected together. Following reset, SO is tristated until the first rising edge of the Serial Out Clock (SOCP) signal. Data is clocked out least significant bit first. In the serial width expansion mode, SO is tristated again after the ninth bit is output.

Full Flag ($\overline{FF}$)

$\overline{FF}$ is asserted LOW when the FIFO is full. When the FIFO is full, the internal write pointer will not be incremented by any additional write pulses.

Full Flag — Serial In Mode

When the FIFO is loaded serially, the Serial In Clock (SICP) asserts the $\overline{FF}$. On the second rising edge of the SICP for the last word in the FIFO, the $\overline{FF}$ will assert LOW, and it will remain asserted until the next read operation. Note that when the $\overline{FF}$ is asserted, the last SICP for that word will have to be stretched as shown in Figure 23.

Full Flag — Parallel-In Mode

When the FIFO is in the Parallel-In mode, the falling edge of $\overline{W}$ asserts the $\overline{FF}$ (LOW). The $\overline{FF}$ is then de-asserted (HIGH) by subsequent read operations - either serial or parallel.

Full–Minus — One Flag ($\overline{FF-1}$)

The $\overline{FF-1}$ flag is asserted low when the FIFO is one word away from being full. It will remain asserted when the FIFO is full.

Expansion Out/Half–Full Flag ($\overline{XO}/\overline{HF}$)

In the single-device mode, the $\overline{XO}/\overline{HF}$ pin operates as a $\overline{HF}$ pin when the $\overline{XI}$ pin is grounded. After half of the memory is filled, the $\overline{HF}$ will be set to LOW at the falling edge of the next write operation. It will remain set until the difference between the write pointer and read pointer is less than or equal to one-half of the FIFO total memory. The $\overline{HF}$ is then reset by the rising edge of the read operation.

In the multiple-device mode, the $\overline{XI}$ pin is connected to the $\overline{XO}$ pin of the previous device. The $\overline{XO}$ pin signals a pulse to the next device when the previous device reaches the best location of memory in the daisy chain configuration.

Almost–Empty or Almost–Full Flag ($\overline{AEF}$)

The $\overline{AEF}$ asserts LOW if there are 0-255 or 1793-2048 bytes in the IDT72103, 2K x 9 FIFO. The $\overline{AEF}$ asserts LOW if there are 0-511 or 3585-4096 bytes in the IDT72104, 4K x 9 FIFO.

Empty–Plus–One Flag ($\overline{EF+1}$)

In the parallel-output mode, the $\overline{EF+1}$ flag is asserted LOW when there is one word or less in the FIFO. It will remain LOW when the FIFO is empty.

In the serial-output mode, the $\overline{EF+1}$ flag operates as an $\overline{EF+2}$ flag. It goes LOW when the second to the last word is read from the RAM array and is ready to be shifted out.

Empty Flag ($\overline{EF}$) — Parallel–Out Mode

When the FIFO is in the parallel out mode and there is only one word in the FIFO, the falling edge of the $\overline{R}$ line will cause the $\overline{EF}$ line to be asserted LOW. This is shown in Figure 6. The $\overline{EF}$ is then de-asserted HIGH by either the rising edge of $\overline{W}$ or the rising edge of SICP, as shown in Figure 6.

Empty Flag — Serial–Out Mode

The use of the $\overline{EF}$ is important for proper serial-out operation when the FIFO is almost empty. The $\overline{EF}$ flag is asserted LOW after the first bit of the last word is shifted out. This is shown in Figure 22.

TABLE 1 — STATUS FLAGS

Number of Words in FIFO IDT72103	Number of Words in FIFO IDT72104	$\overline{FF}$	$\overline{FF-1}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF+1}$ (1)	$\overline{EF}$
0	0	H	H	L	H	L	L
1	1	H	H	L	H	L	H
2-255	2-511	H	H	L	H	H	H
256-1024	512-2048	H	H	H	H	H	H
1025-1792	2049-3584	H	H	H	L	H	H
1793-2046	3585-4094	H	H	L	L	H	H
2047	4095	H	L	L	L	H	H
2048	4096	L	L	L	L	H	H

NOTE: 2753 tbl 10

1. $\overline{EF+1}$ acts as $\overline{EF+2}$ in the serial out mode.

PARALLEL TIMINGS:

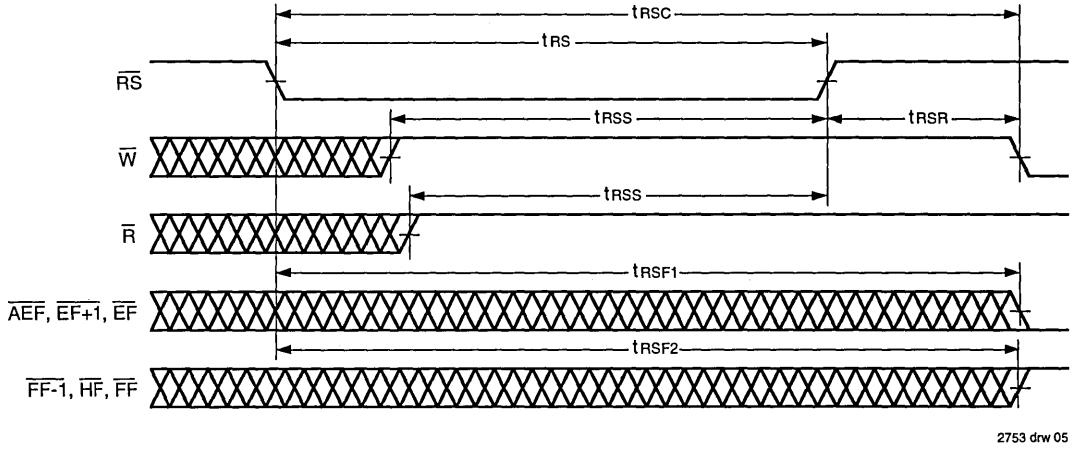


Figure 2. Reset

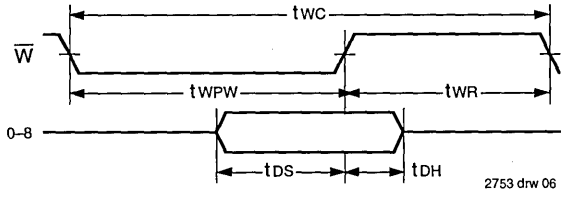


Figure 3. Write Operation in Parallel Data In Mode

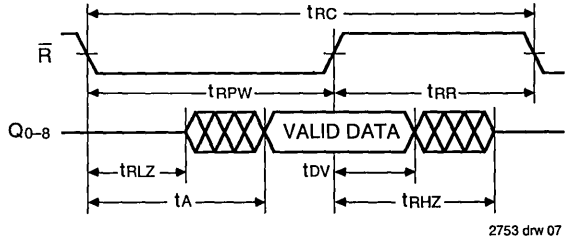


Figure 4. Read Operation in Parallel Data Out Mode

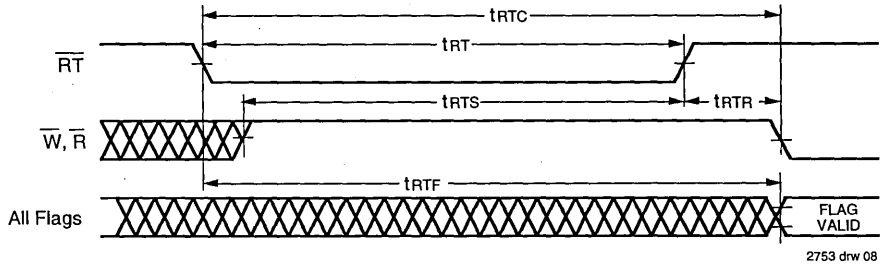
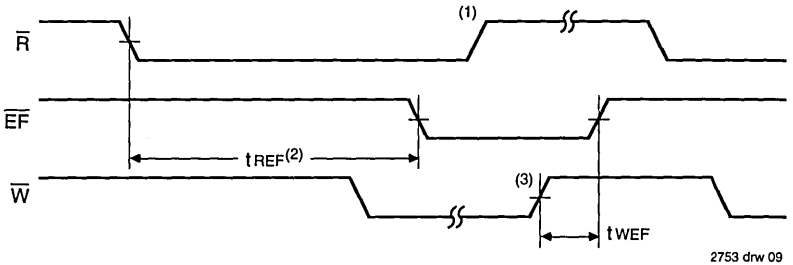
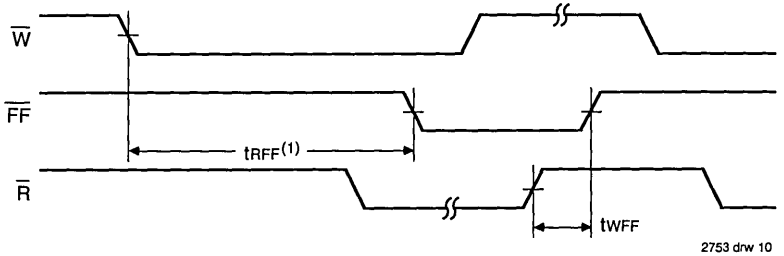


Figure 5. Retransmit



NOTES:
1. Data is valid on this edge.
2. The Empty Flag is asserted by R in the Parallel-Out mode and is specified by tREF. The EF flag is deasserted by the rising edge of W.
3. First rising edge of Write after EF is set.

Figure 6. Empty Flag Timings in Parallel Out Mode



NOTE:
1. For the assertion time, tWFF is used when data is written in the Parallel mode. The FF is de-asserted by the rising edge of R.

Figure 7. Full Flag Timings in Parallel-In Mode

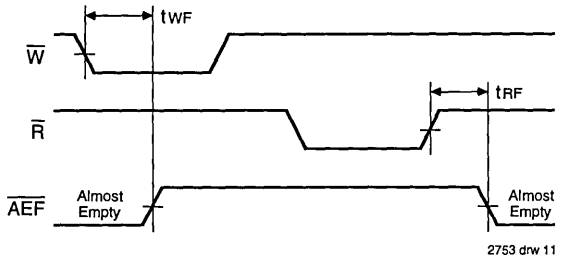


Figure 8. Almost-Empty Flag Region

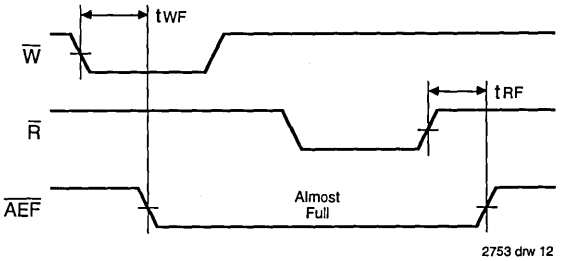


Figure 9. Almost-Full Flag Region

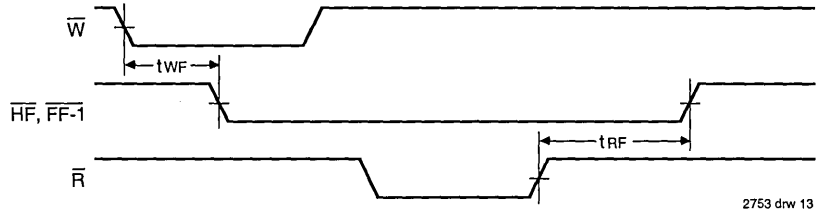


Figure 10. Half-Full and Full-minus-1 Flag Timings

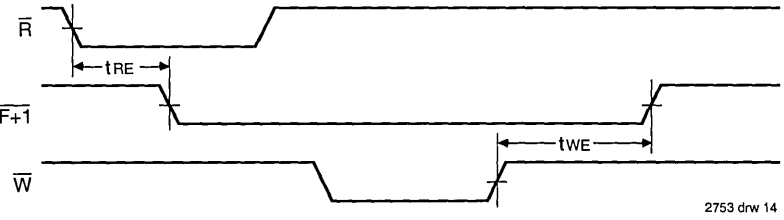


Figure 11. Empty+1 Flag Timings

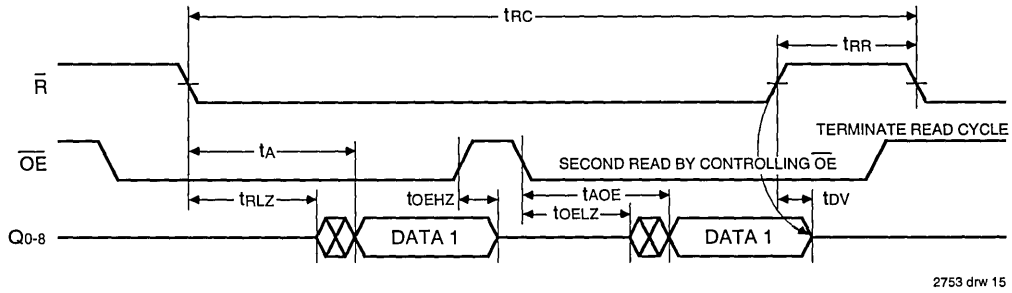


Figure 12. Output Enable Timings

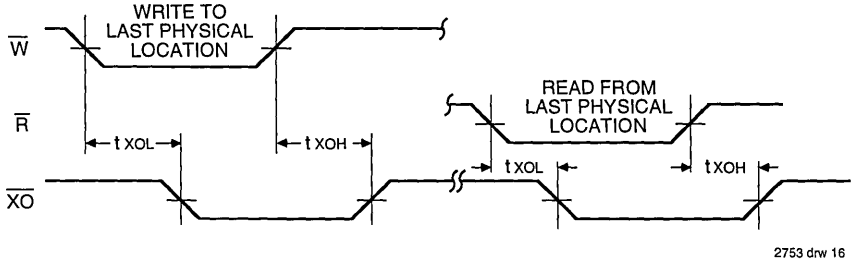


Figure 13. Expansion-Out

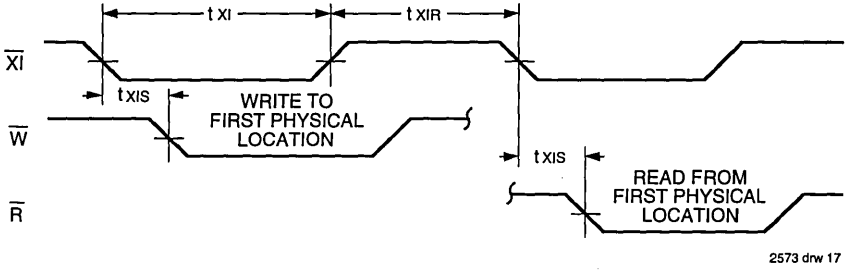


Figure 14. Expansion-In

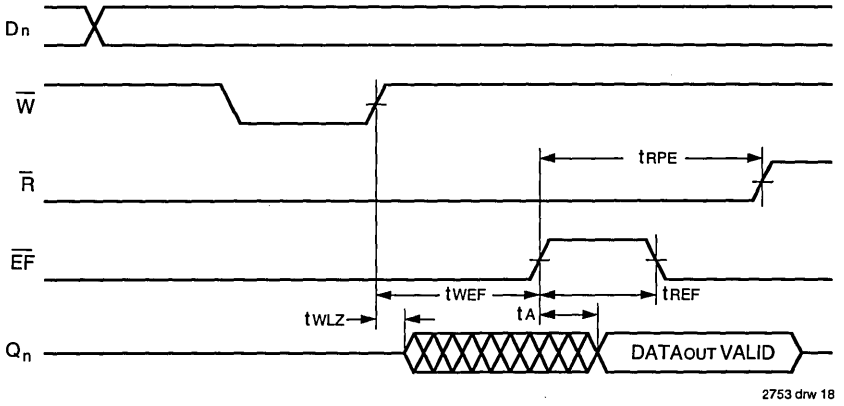


Figure 15. Read Data Flow-Through Mode

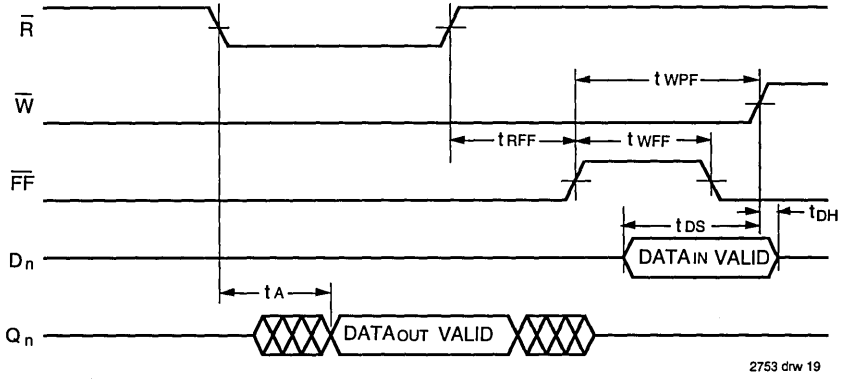
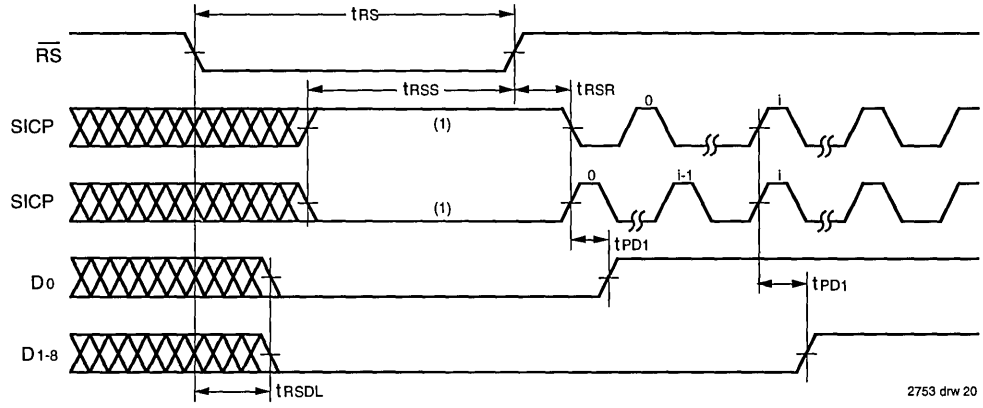


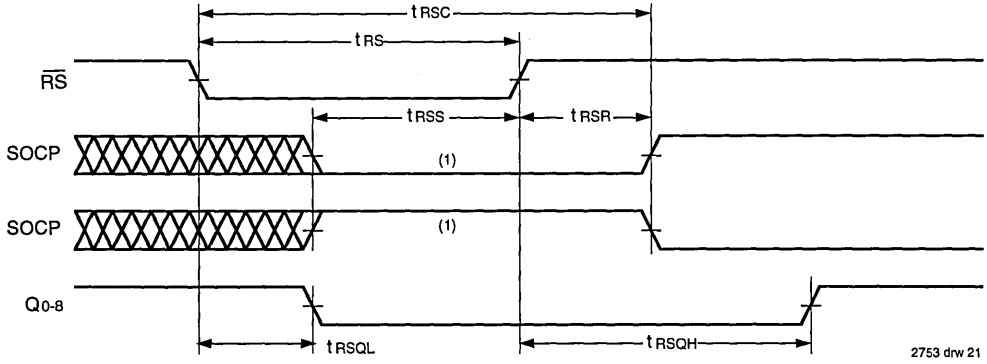
Figure 16. Write Data Flow-Through Mode

serial timings:



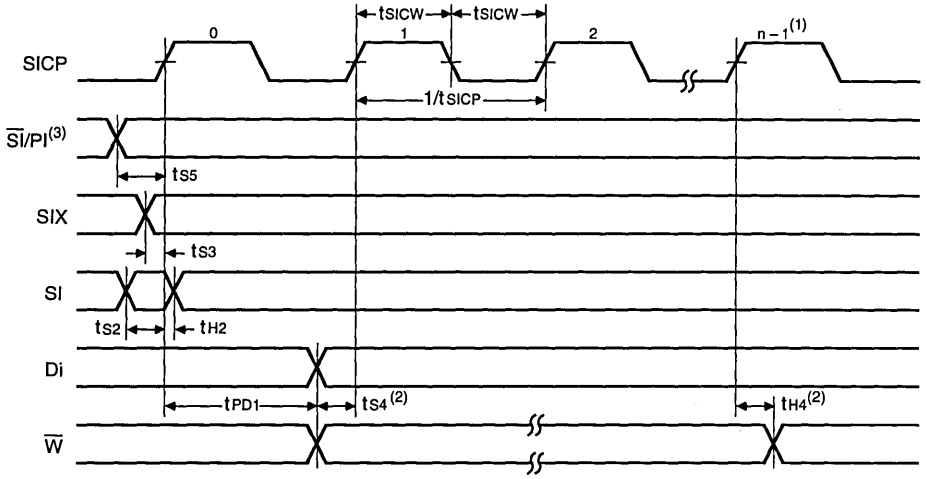
NOTE:
1. SICP should be in the steady LOW or HIGH during tRSS. The first LOW-HIGH (or HIGH-LOW) transition can begin after tRSR.

Figure 17. Reset Timings for Serial-In Mode



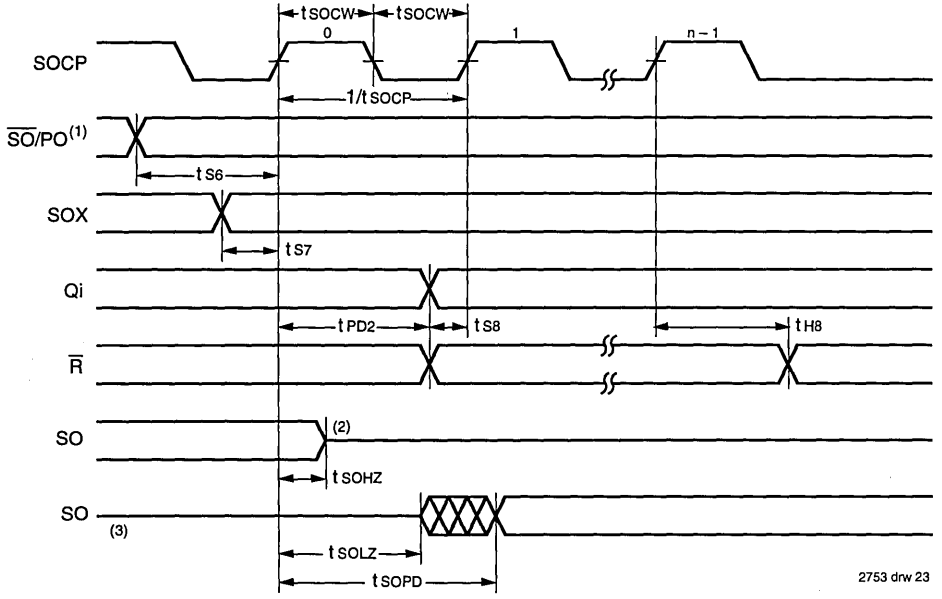
NOTE:
1. SOCP should be in the steady LOW or HIGH during tRSS. The first LOW-HIGH (or HIGH-LOW) transition can begin after tRSR.

igure 18. Reset Timings for Serial-Out Mode



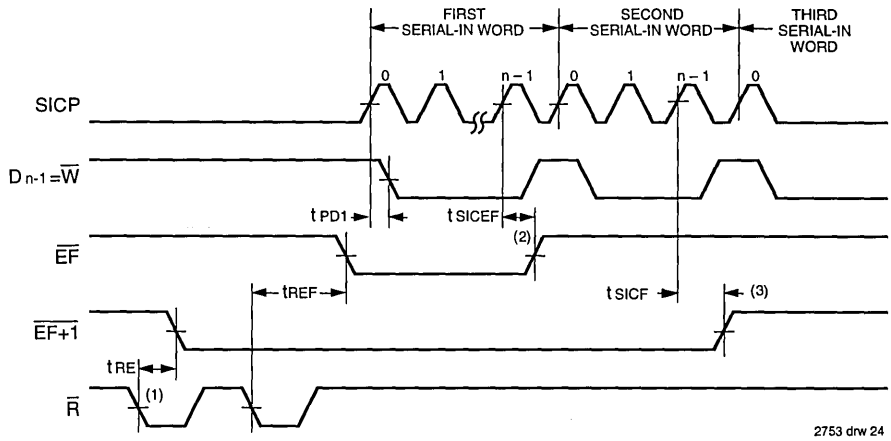
NOTES:
1. For the stand alone mode, n ≥ 4 and the input bits are numbered 0 to n-1.
2. For the recommended interconnections, Di is to be directly tied to W and the tS4 and tH4 requirements will be satisfied. For users that modify W externally, tS4 and tH4 requirements have to be met.
3. After SI/PI has been set up, it cannot be dynamically changed; it can only be changed after a reset operation.

Figure 19. Write Operation In Serial-In Mode



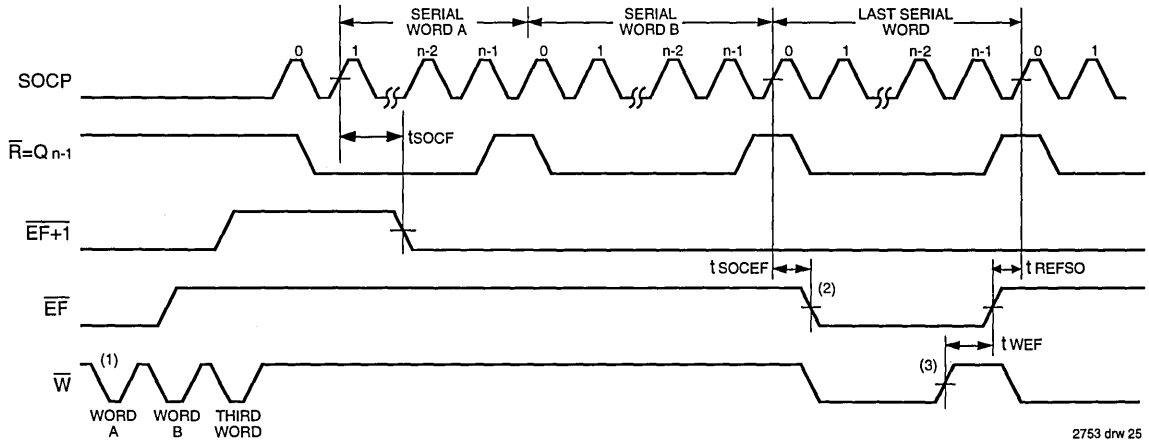
NOTES:
1. After SO/PO has been set up, it cannot be dynamically changed; it can only be changed after a reset operation.
2. For single device: Read out the last bit after EF is asserted.
   For Serial Width Expansion mode: Read out the last bit of the current memory location from the active device.
3. For single device: The operation starts after Reset.
   For Serial Width Expansion mode: Read the first bit of the current memory location from the active device.

Figure 20. Read Operation In Serial-Out Mode



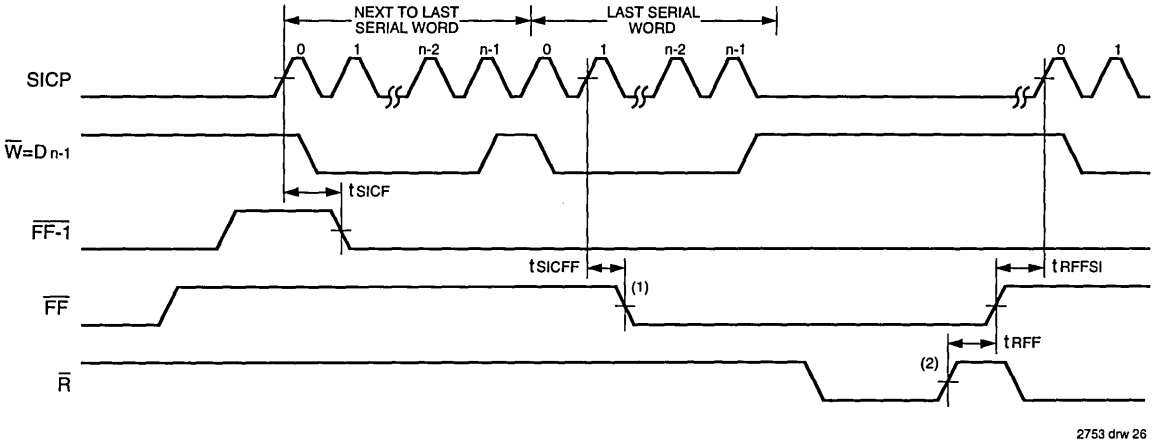
NOTES:
1. Parallel Read shown for reference only. Can also use serial output mode.
2. The Empty Flag is de-asserted after the N–1 rising edge of SICP of the first serial-in word. In the Serial-Out mode, a new read operation can begin tREFSO after EF goes HIGH. In the Parallel-Out mode, a new read operation can occur immedately after FF goes HIGH.
3. The EF+1 Flag is de-asserted after the N–1 rising edge of SICP of the second serial-in word.

Figure 21. Empty Flag and Empty+1 Flag De-assertion in the Serial-In Mode



NOTES:
1. Parallel write shown for reference only. Can also use serial input mode.
2. The Empty Flag (EF) is asserted in Serial-Out mode by using the tSOCEF parameter. This parameter is measured in the worst case condition from the rising edge of the SOCP used to clock data bit 0. Whenever EF goes LOW, there is only one word to be shifted out. In the Parallel-In mode, the EF flag is de-asserted by the rising edge of W. In the Serial-In mode, the EF flag is de-asserted by the rising edge of W.
3. First Write rising edge after EF is set.
4. Once EF has gone LOW and the last bit of the final word has been shifted out, SOCP should not be clocked until EF goes HIGH.

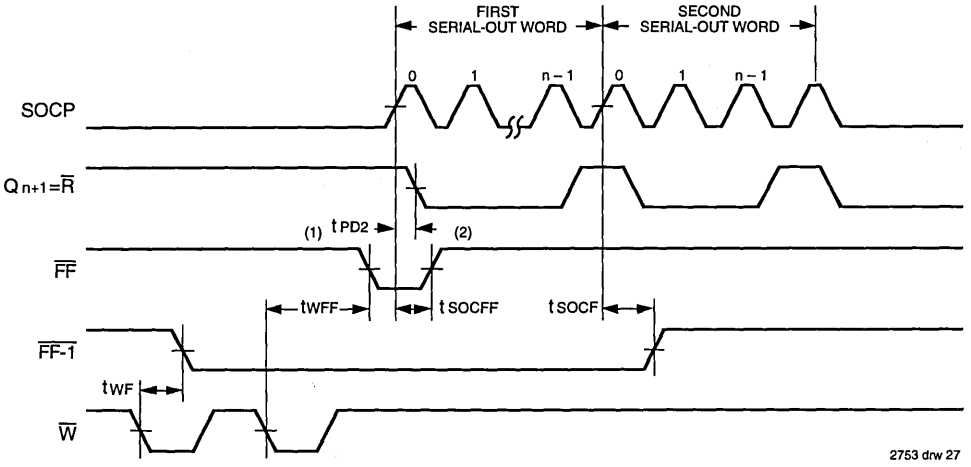
Figure 22. Empty Flag and Empty+1 Flag Assertion in the Serial-Out Mode (FIFO Being Emptied)



NOTES:
1. The Full Flag is asserted in the Serial-In mode by using the tSICFF parameter. This parameter is measured in the worst case condition from the rising edge of SICP following a (tPD1+tWFF) delay from the first SICP rising edge of the last word.
2. First Read rising edge after FF is set.
3. After FF goes LOW and the last bit of the final word has been clocked in, SICP should not be clocked until FF goes HIGH.

Figure 23. Full Flag and Full-1 Flag Assertion in the Serial-In Mode (FIFO Being Filled)

5



NOTES:
1. The FIFO is full and a new read sequence is started.
2. On the first rising edge of SOCP, the FF is de-asserted. In the Serial-In mode, a new write operation can begin following tRFFS1 after FF, goes HIGH. In the Parallel-In mode, a new write operation can occur immediately after FF goes HIGH.
3. The FF-1 flag is de-asserted after the first SOCP of the second serial word.

Figure 24. Full Flag and Full-1 Flag De-assertion in the Serial-Out Mode

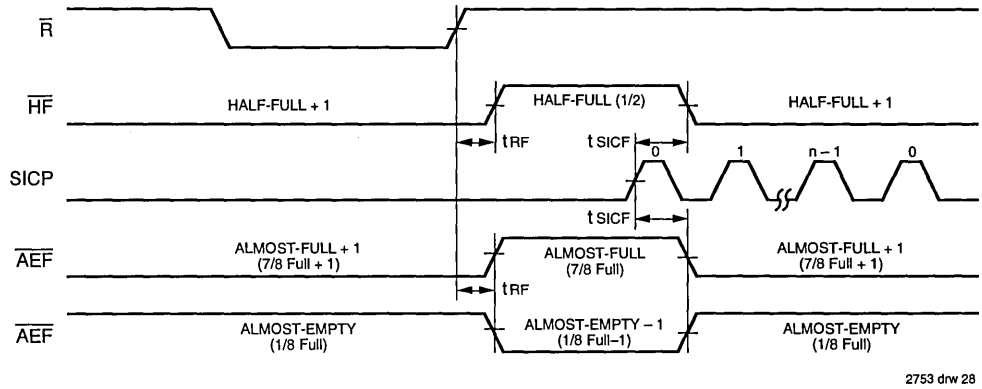


Figure 25. Half-Full, Almost-Full and Almost-Empty Timings for Serial-In Mode

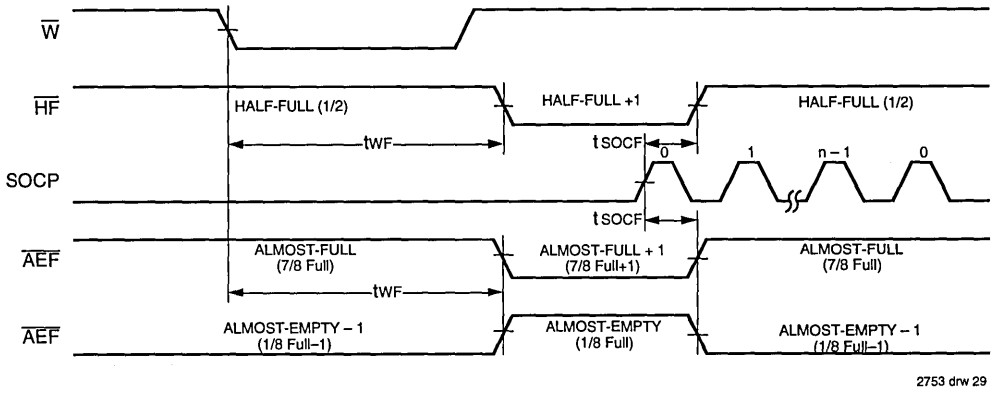


Figure 26. Half-Full, Almost-Full and Almost-Empty Timings for Serial-Out Mode

OPERATING DESCRIPTION

PARALLEL OPERATING MODES:

Parallel Data Input

By setting SI/PI HIGH, data is written into the FIFO in parallel through the D0-D8 input data lines.

Parallel Data Output

By setting SO/PO HIGH, the parallel-out mode is chosen. In the parallel-out mode, as shown in Figure 4, data is available tA after the falling edge of R and the output bus Q goes into high-impedance after R goes HIGH.

Alternately, the user can access the FIFO by keeping R LOW and enabling data on the bus by asserting OE. When R is LOW, the OE is HIGH and the output bus is tri-stated. When R is HIGH, the output bus is disabled irrespective of OE. The enable and disable timings for OE are shown in Figure 12.

Single Device Mode

A single IDT172103/72104 may be used when application requirements are for 2048/4096 words or less. The IDT72103/72104 is in the Single Device Configuration when the Expansion In (XI) control input is grounded (See Figure 27). In this mode, the HF/XO is used as a Half-Full flag.

Width Expansion Mode

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags can be detected from any one of the connected devices. Figure 28 demonstrates an 18-bit word width by using two IDT72103/72104s. Any word width can be attained by adding additional IDT72103/72104.

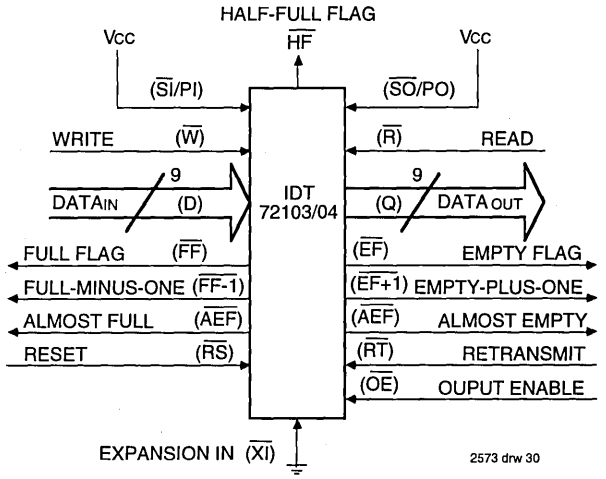


Figure 27. Block Diagram of Single 2048 x 9/4096 x 9 FIFO in Parallel Mode

INPUT CONFIGURATION TABLE

Pin	Parallel Input	Serial Input			
			Width Expansion		
		Single Device	Least Significant Device	All Other Devices	Most Significant Device
$\overline{SI}$/PI	HIGH	LOW	LOW	LOW	LOW
SI	HIGH or LOW	Input Data	Input Data	Input Data	Input Data
SICP	HIGH or LOW	Input Clock	Input Clock	Input Clock	Input Clock
SIX	HIGH	HIGH	HIGH	D_8 of next least significant device	D_8 of next least significant device
$\overline{W}$	Write Control	Di	Di of most significant device	Di of most significant device	Di of most significant device
D_0-D_8	Input Data	No connect except Di	No connect except D_8	No connect except D_8	No connect except Di
$Di^{(1)}$	—	$\overline{W}$	—	—	$\overline{W}$ of all devices
D_8	—	—	SIX of next most significant device	SIX of next most significant device	—

NOTE: 2753 tbl 11

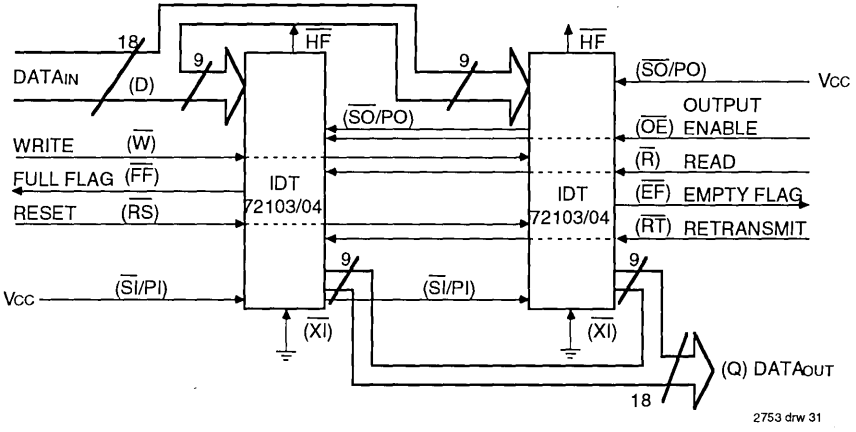
1. Di refers to the most significant bit of the serial word. If multiple devices are width cascaded, Di is the most significant bit from the most signifi device.

OUTPUT CONFIGURATION TABLE

Pin	Parallel Output	Serial Output			
			Width Expansion		
		Single Device	Least Significant Device	All Other Devices	Most Significant Device
$\overline{SO}$/PO	HIGH	LOW	LOW	LOW	LOW
SO	—	Output Data	Output Data	Output Data	Output Data
SOCP	HIGH or LOW	Output Clock	Output Clock	Output Clock	Output Clock
SOX	HIGH	HIGH	HIGH	Q_8 of next least significant device	Q_8 of next least significant device
$\overline{R}$	Read Control	Qi	Qi of most significant device	Qi of most significant device	Qi of most significant device
Q_0-Q_8	Output Data	No connect except Di	No connect except Q_8	No connect except Q_8	No connect except Qi
$Qi^{(1)}$	—	$\overline{R}$	—	—	$\overline{R}$ of all devices
Q_8	—	—	SOX of next most significant device	SOX of next most significant device	—

NOTE: 2753 tbl 12

1. Qi refers to the most significant bit of the serial word. If multiple devices are width cascaded, Qi is the most significant bit from the most signifi device.



NOTE:
1. Flag detection is accomplished by monitoring all the flag signals of either (any) device used in the width expansion configuration. Do not connect any flag signals together.

Figure 28. Block Diagram of 2048 x 18/4096 x 18 FIFO Memory Used in Width Expansion in Parallel Mode

5

TRUTH TABLES
TABLE 2: RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION IN PARALLEL MODE

Mode	Inputs[2]			Internal Status[1]		Outputs		
	RS	FL	XI	Read Pointer	Write Pointer	AEF, EF	FF	HF
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

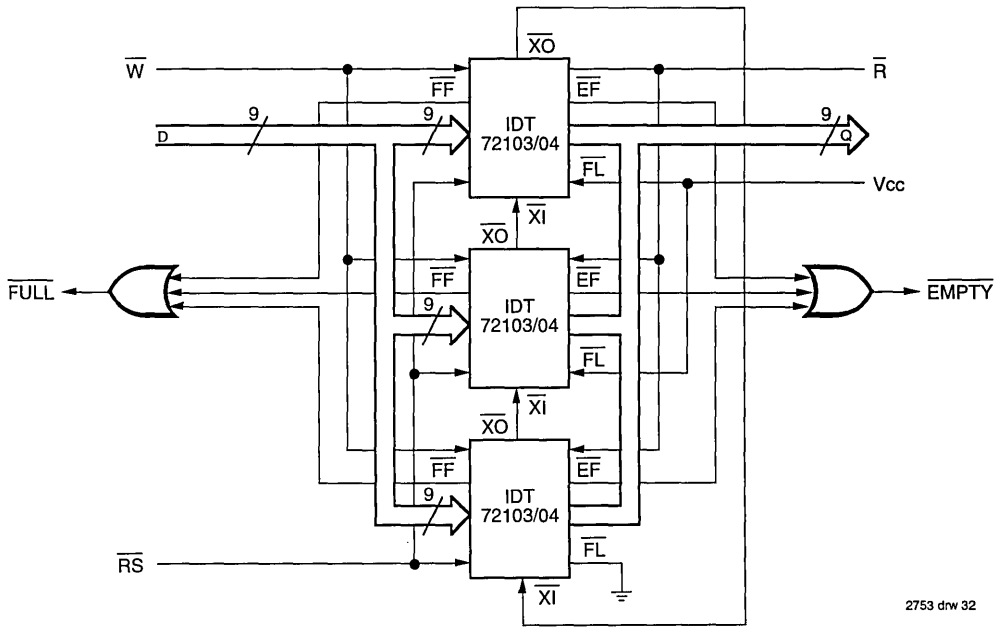
2753 tbl 13

NOTES:
1. Pointer will increment if appropriate flag is HIGH.
2. RS = Reset Input, FL/RT = First Load/Retransmit, EF = Empty Flag Output, FF = Full Flag Output, XI = Expansion Input.

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT72103/4 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 29 demonstrates Depth Expansion using three IDT72103/4s. Any memory depth can be attained by adding additional IDT72103/4s. The IDT72103/4 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load (FL) control input pin.
2. All other devices must have the FL pin in the high state.
3. The Expansion Out (XO) pin of each device must be tied to the Expansion In (XI) pin of the next device. See Figure 29.
4. External logic is needed to generate a composite Full Flag (FF) and Empty Flag (EF). This requires the OR-ing of all EFs and OR-ing of all FFs (i.e., all must be set to generate the correct composite FF or EF). See Figure 29.
5. The Retransmit (RT) function and Half-Full Flag (HF) are not available in the Depth Expansion mode.

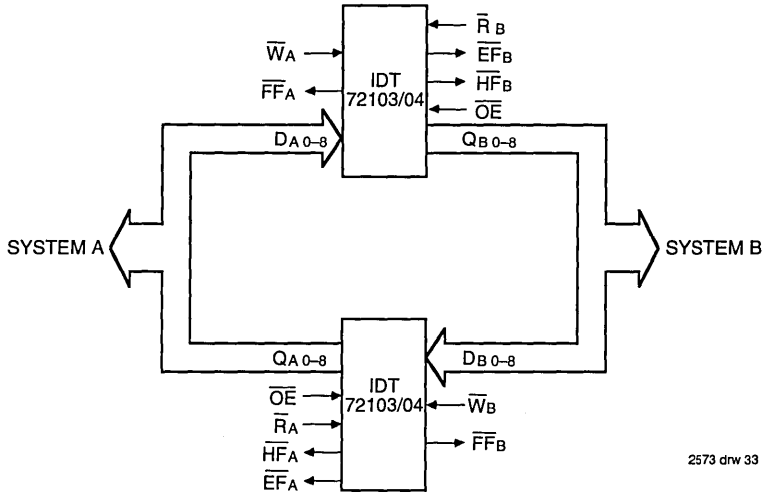


NOTE:
1. SI/PI and SO/PO pins are tied to VCC.

Figure 29. Block Diagram of 6,144 x 9/12,288 x 9-FIFO Memory, Depth Expansion in Parallel Mode

BIDIRECTIONAL MODE

Applications requiring data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72103/4 as shown in Figure 30. Both Depth Expansion and Width Expansion may be used in this mode.

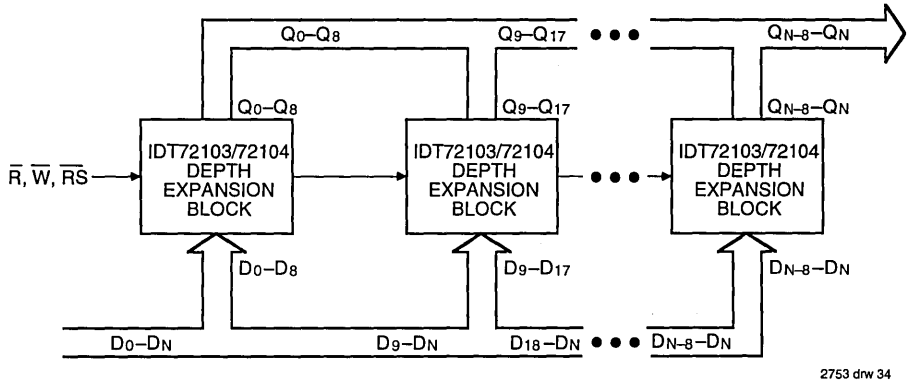


NOTE:
1. SI/PI and SO/PO pins are tied to VCC.

Figure 30. Bidirectional FIFO Mode

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 31).



NOTE:
1. SI/PI and SO/PO pins are tied to VCC.
2. For depth expansion block see DEPTH EXPANSION Section and Figure 29.
3. For Flag Detection see WIDTH EXPANSION SECTION and Figure 28.

Figure 31. Compound FIFO Expansion

TABLE 3: RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs[2]			Internal Status		Outputs	
	RS	FL	XI	Read Pointer	Write Pointer	EF	FF
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Retransmit all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input, FL/$\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Ouput, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

2753 tbl 14

SERIAL OPERATING MODES:

Serial Data Input

The Serial Input mode is selected by grounding the SI/PI line. The D0-8 lines are then outputs which are used to program the width of the serial word. They are taps off a digital delay line which are meant for connection to the W input. For instance, connecting D6 to W will program a serial word width of 7 bits, connecting D7 to W will program a serial word width of 8 bits and so on.

By programming the serial word width, an economy of clock cycles is achieved. As an example, if the word width is 6 bits, then on every 6th clock cycle the serial data register is written in parallel into the FIFO RAM array. Thus, the possible clock cycles for an extra 3 bits of width in the RAM array are not required.

The SIX signal is used for Serial-In Expansion. When the serial word width is 9 or less, the SIX input must be tied HIGH. When more than 9 bits of serial word width is required, more than one device is required. The SIX input of the least significant device must be tied HIGH. The D8 pin of the least significant device must be tied to SIX of the next significant device. In other words, the SIX input of the most significant and intermediate devices must always be connected to the D8 of the next least significant device.

Figure 32 shows the relationship of the SIX, SICP and D0-8 lines. In the stand alone case (Figure 32), on the first LOW-to-HIGH of SICP, the D1-8 lines go LOW and the D0 line remains HIGH. On the next SICP clock edge, the D1 goes HIGH, then D2 and so on. This continues until the D line, which is connected to W, goes HIGH. On the next clock cycle, after W is HIGH, all of the D lines go LOW again and a new serial word input starts.

In the cascaded case, the first LOW-to-HIGH SICP clock edge for a serial word will cause all timed outputs (D) to go LOW except for D0 of the least significant device. The D outputs of the least significant device will go high on consecutive clock cycles until D8. When D8 goes HIGH, the SIX of the next device goes HIGH. On the next cycle after the SIX input is brought HIGH, the D0 goes HIGH; then on the next cycle D1 and so on. A Di output from the most significant device is issued to create the W for all cascaded devices.

The minimum serial word width is 4 bits and the maximum is virtually unlimited.

When in the Serial mode, the Least Significant Bit of a serial stream is shifted in first. If the FIFO output is in the Parallel mode, the first serial bit will come out on Q0. The second bit shifted in is on Q1 and so on.

In the Serial Cascade mode, the serial input (SI) pins must be connected together. Each of the devices then receives serial information together and uses the SIX and D0-8 lines to determine whether to store it or not.

The example shown in Figure 34 shows the interconnections for a serializing FIFO that transfers data to the internal RAM in 16-bit quantities (i.e. every 16 SICP cycles). This corresponds to incrementing the write pointer every 16 SICP cycles.

Once W goes HIGH with the last serial bit in, SICP should not be clocked again until FF goes HIGH.

SINGLE DEVICE SERIAL INPUT CONFIGURATION

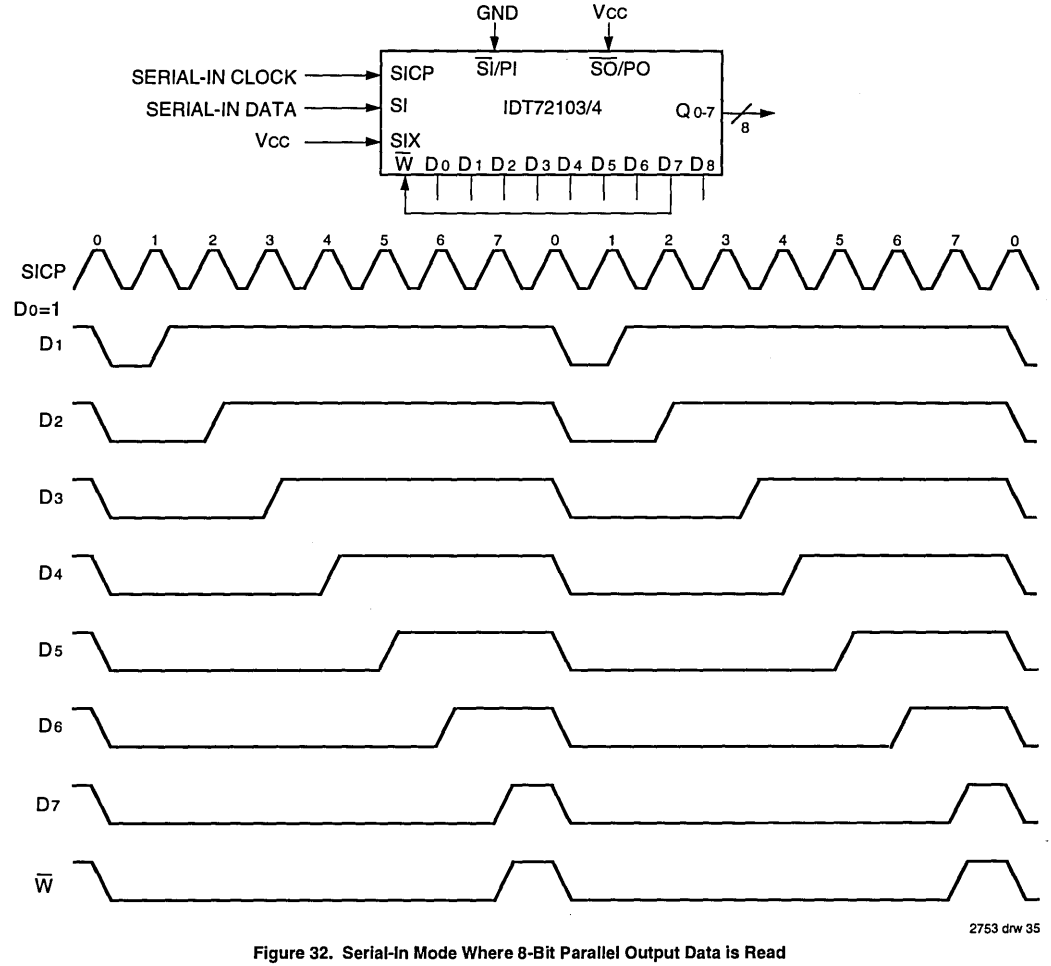


Figure 32. Serial-In Mode Where 8-Bit Parallel Output Data is Read

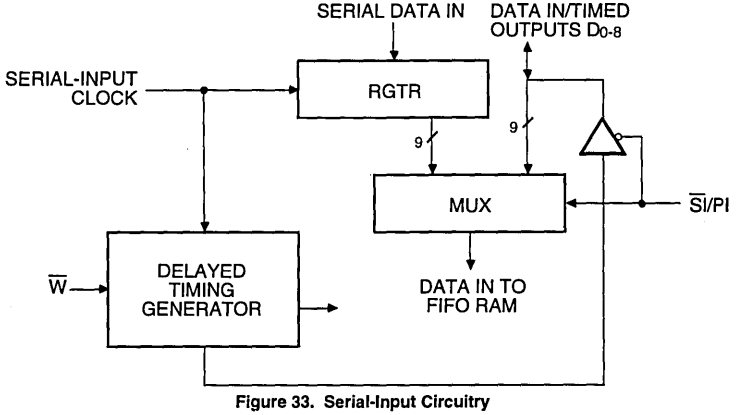


Figure 33. Serial-Input Circuitry

SERIAL INPUT WIDTH EXPANSION

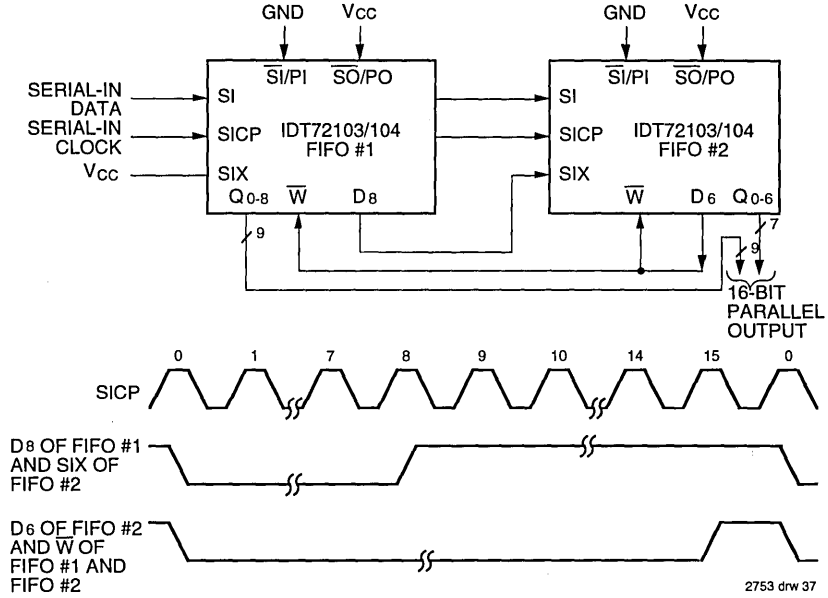
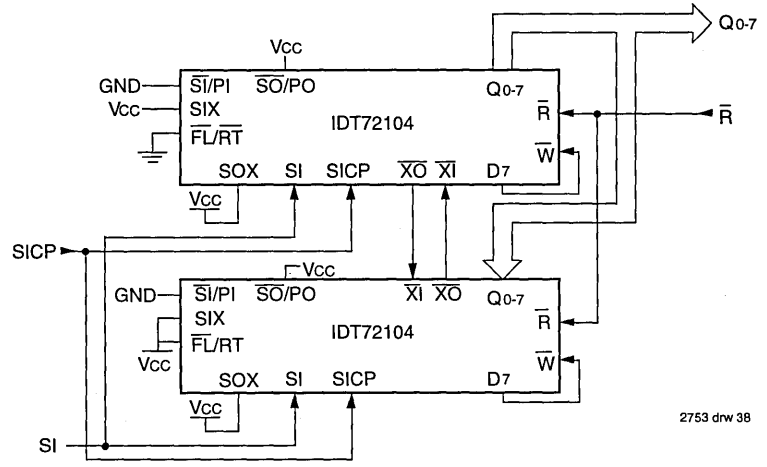


Figure 34. Serial-In Configuration for Serial-In to Parallel-Out Data of 16 bits

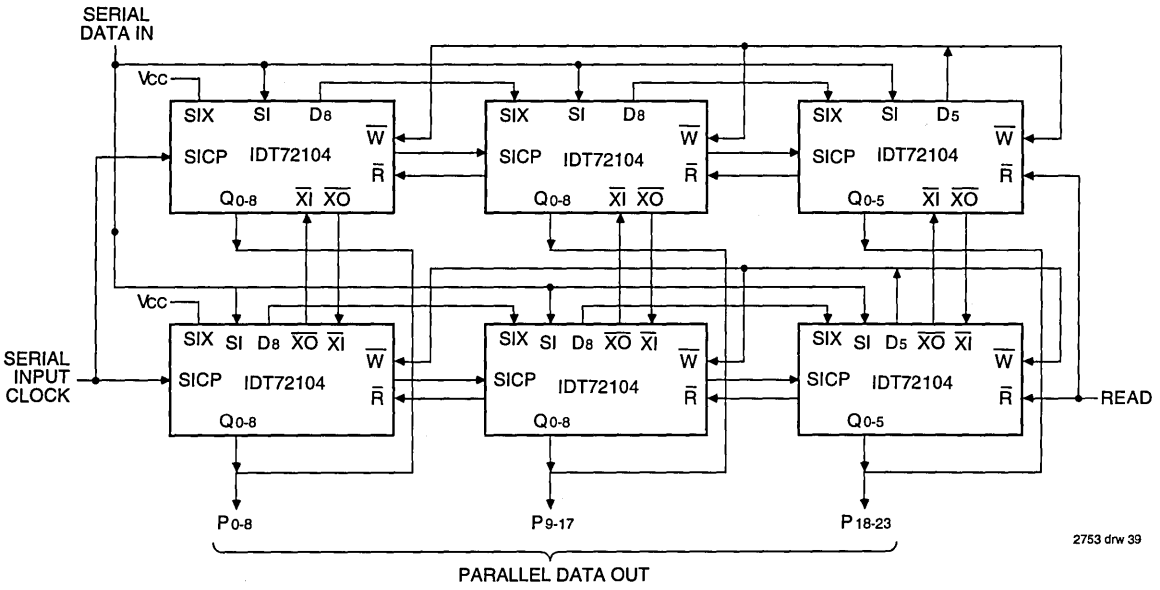
SERIAL INPUT WITH DEPTH EXPANSION



NOTE:
1. All SI/PI pins are tied to GND and SO/PO pins are tied to VCC. OE is tied LOW. For FF and EF connections see Figure 29.

Figure 35. An 8K x 8 Serial-In, Parallel-Out FIFO

SERIAL INPUT WITH WIDTH AND DEPTH EXPANSION



NOTE:
1. All SI/PI pins are tied to GND. SO/PO pins are tied to VCC. For FL/RT, FF and EF connections see Figure 29.

Figure 36. An 8K x 24 Serial-In, Parallel-Out FIFO Using Six IDT72104s

SERIAL DATA OUTPUT

The Serial Output mode is selected by setting the SO/PO line LOW. When in the Serial-Out mode, one of the Q1-8 lines should be used to control the R signal. In the Serial-Out mode, the Q0-8 are taps off a digital delay line. By selecting one of these taps and connecting it to R, the width of the serial word to be read and shifted is programmed. For instance, if the Q5 line is connected to the R input, on every sixth clock cycle a new word is read from the FIFO RAM array and begins to be shifted out. The serial word is shifted out Least Significant Bit first. If the input mode of the FIFO is parallel, the information that was written into the D0 bit will come out as the first bit of the serial word. The second bit of the serial stream will be the D1 bit and so on.

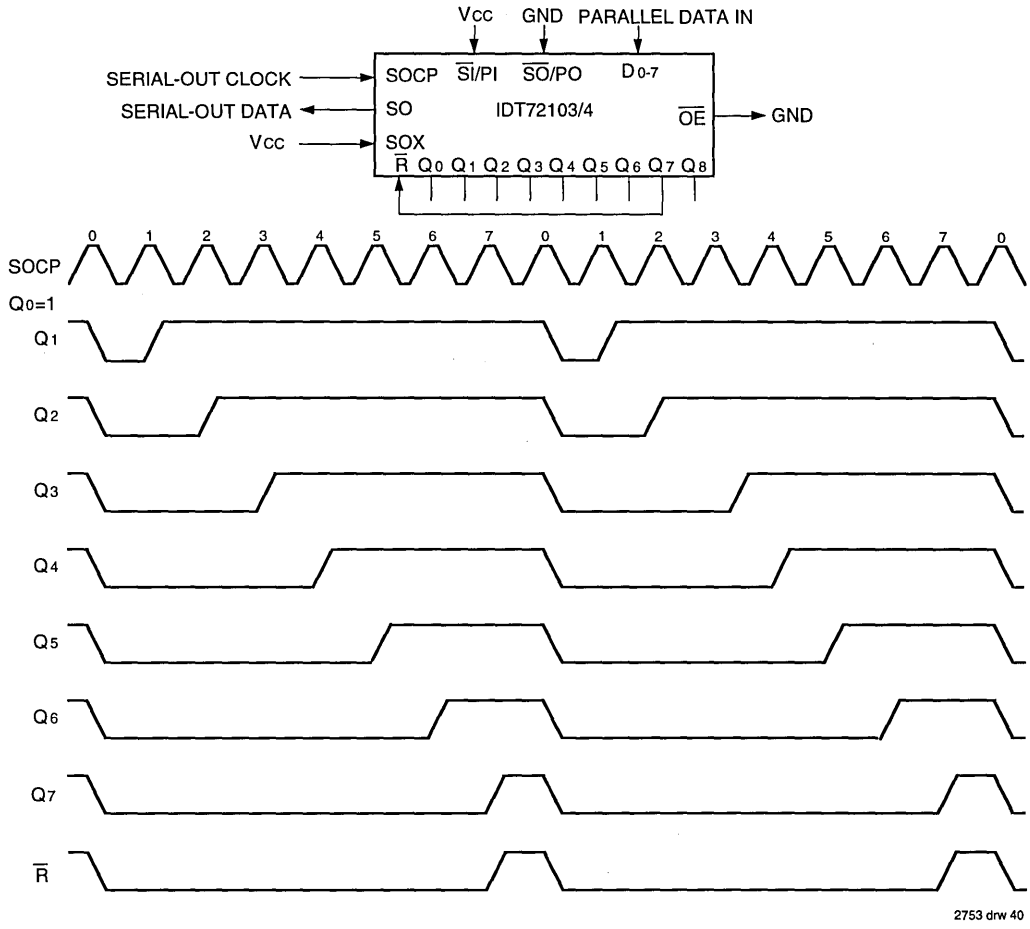
In the stand alone case, the SOX line is tied HIGH and not used. On the first LOW-to-HIGH of the SOCP clock, all of the Q outputs except for Q0 go LOW and a new serial word is started. On the next clock cycle, Q1 will go HIGH, Q2 on the next clock cycle and so on, as shown in Figure 37. This continues until the Q line, which is connected to R, goes HIGH at which point all of the Q lines go LOW on the next clock and a new word is started.

In the cascaded case, word width of more than 9 bits can be achieved by using more than one device. By tying the SOX line of the least significant device HIGH and the SOX of the subsequent devices to Q8 of the previous device, a cascaded serial word is achieved. On the first LOW-to-HIGH clock edge of SOCP, all the Q lines go low except for Q0. Just as in the stand alone case, on each consecutive clock cycle, each Q line goes HIGH in the order of least to most significant. When Q8 (which is connected to the SOX input of the next device) goes HIGH, the D0 of that device goes HIGH, thus cascading from one device to the next. The Q line of the most significant device, which programs the serial word width, is connected to all R inputs.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is tri-stated, only the device which is currently shifting out is enabled and driving the 1-bit bus.

Figure 39 shows an example of the interconnections for a 16-bit serialized FIFO.

Once R goes HIGH with the last serial bit out, SOCP should not be clocked again until EF goes HIGH.



NOTE:
1. Input data is loaded in 8-bit quantities and read out serially.

Figure 37. Serial-Out Configuration

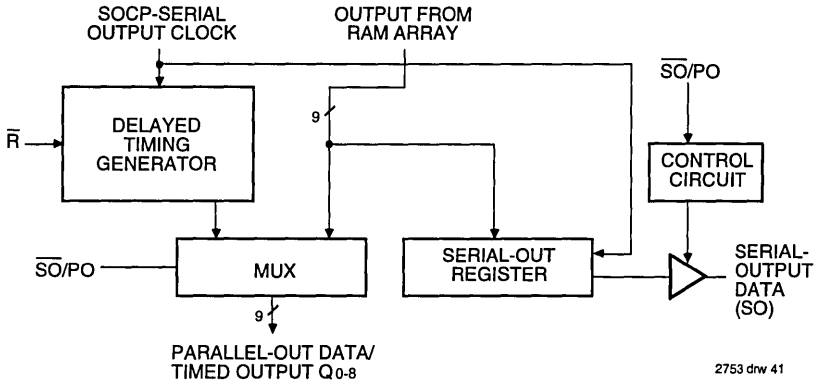
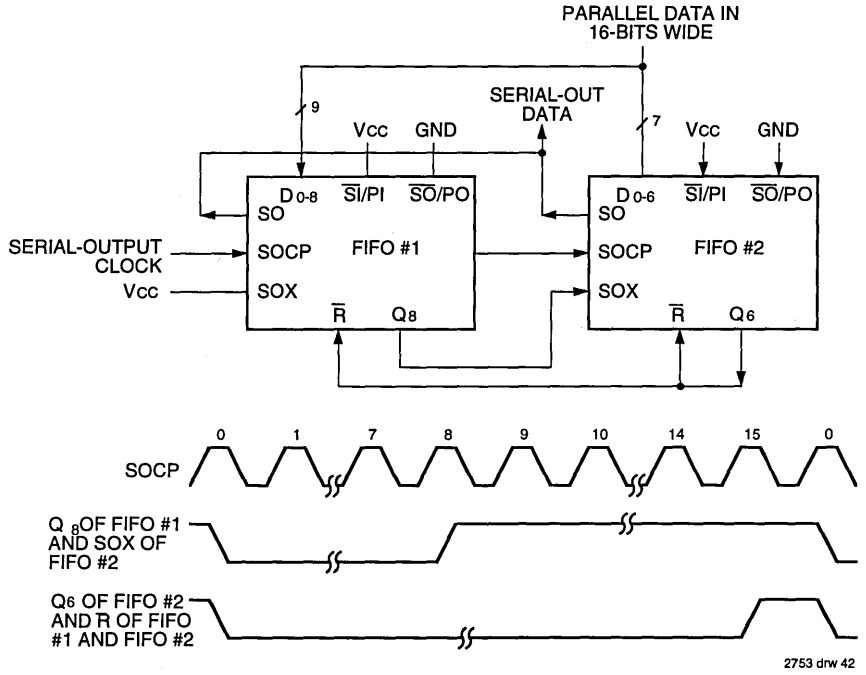


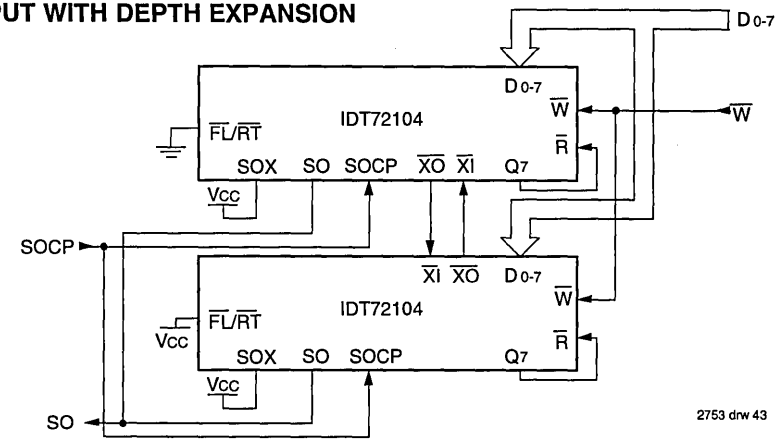
Figure 38. Serial-Output Circuitry



NOTE:
1. The parallel Data In is tied to D0-8 of FIFO #1 and D0-6 of FIFO #2.

Figure 39. Serial-Output for 16-Bit Parallel Data In

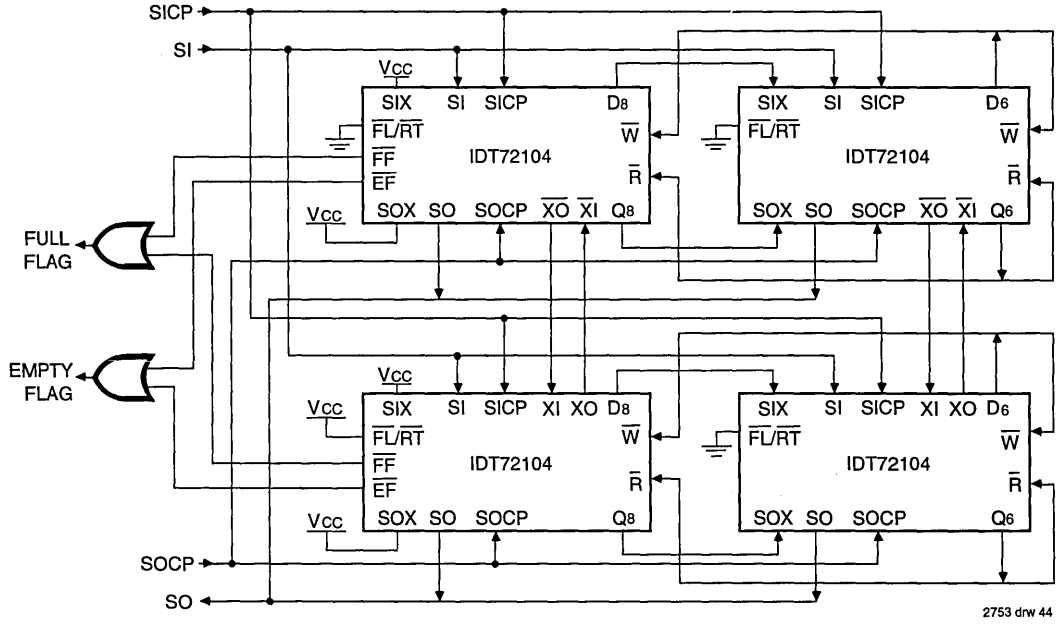
SERIAL OUTPUT WITH DEPTH EXPANSION



NOTE:
1. All SI/PI pins are tied to VCC and SO/PO pins are tied to GND. OE is tied LOW. For FF and EF connections see Figure 17.

Figure 40. An 8K x 8 Parallel-In Serial-Out FIFO

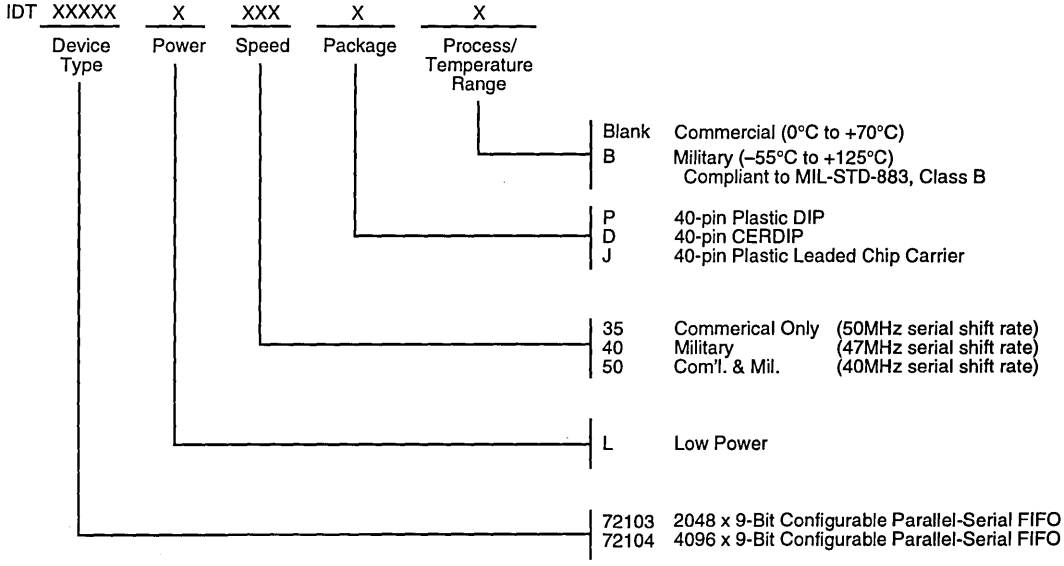
SERIAL IN AND SERIAL OUT WITH WIDTH AND DEPTH EXPANSION



NOTE:
1. All RS pins are connected together. All OE pins are connected LOW. All SI/PI and SO/PO pins are grounded.

Figure 41. 128K x 1 Serial-In Serial-Out FIFO

ORDERING INFORMATION



2753 drw 45

5

Integrated Device Technology, Inc.

CMOS PARALLEL-TO-SERIAL FIFO 256 x 16, 512 x 16, 1024 x 16

IDT72105
IDT72115
IDT72125

FEATURES:

- 25ns parallel port access time, 35ns cycle time
- 45MHz serial output shift rate
- Wide x16 organization offering easy expansion
- Low power consumption (50mA typical)
- Least/Most Significant Bit first read selected by asserting the FL/DIR pin
- Four memory status flags: Empty, Full, Half-Full, and Almost-Empty/Almost-Full
- Dual-Port zero fall-through architecture
- Available in 28-pin 300 mil plastic DIP, 28-pin SOIC, and 32-pin PLCC

DESCRIPTION:

The IDT72105/72115/72125s are very high-speed, low-power,dedicated, parallel-to-serial FIFOs. These FIFOs possess a 16-bit parallel input port and a serial output port with 256, 512 and 1K word depths, respectively.

The ability to buffer wide word widths (x16) make these FIFOs ideal for laser printers, FAX machines, local area networks (LANs), video storage and disk/tape controller applications.

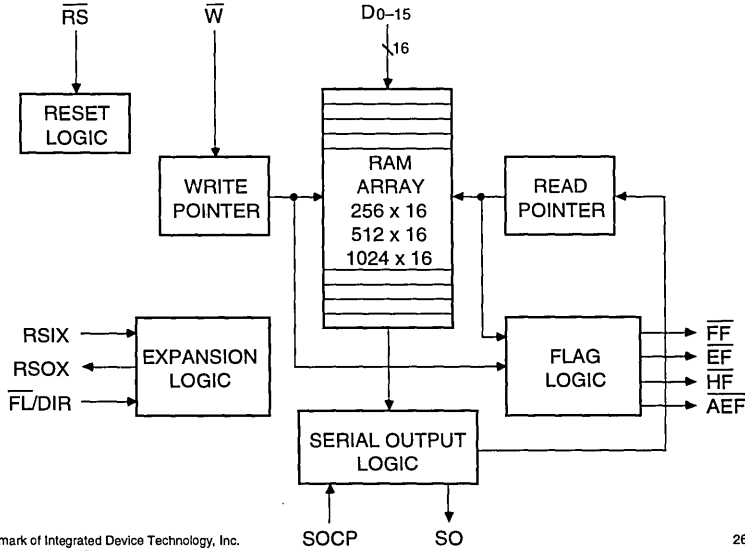
Expansion in width and depth can be achieved using multiple chips. IDT's unique serial expansion logic makes this possible using a minimum of pins.

The unique serial output port is driven by one data pin (SO) and one clock pin (SOCP). The Least Significant or Most Significant Bit can be read first by programming the DIR pin after a reset.

Monitoring the FIFO is eased by the availability of four status flags: Empty, Full, Half-Full and Almost-Empty/Almost-Full. The Full and Empty flags prevent any FIFO data overflow or underflow conditions. The Half-Full Flag is available in both single and expansion mode configurations. The Almost-Empty/Almost-Full Flag is available only in a single device mode.

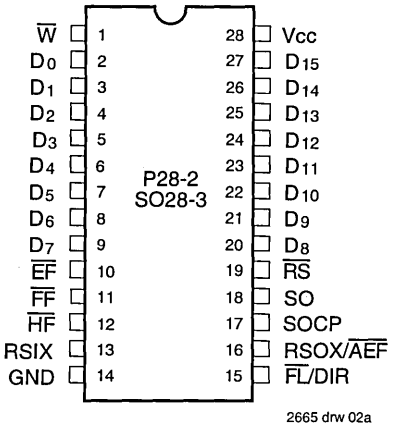
The IDT72105/15/25 are fabricated using IDT's leading edge, submicron CMOS technology. Military grade product is manufactured in compliance with the latest revision of Mil-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



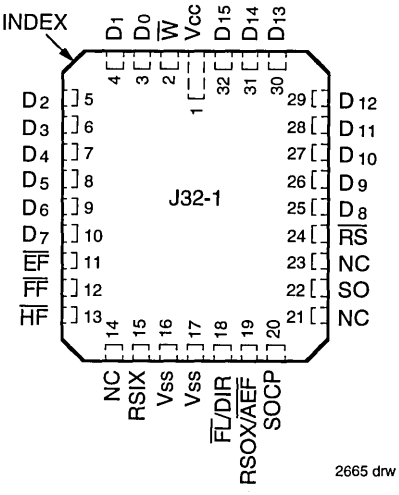
2665 drw 01

PIN CONFIGURATIONS



2665 drw 02a

DIP/SOIC
TOP VIEW



2665 drw 02b

PLCC
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D0–D15	Inputs	I	Data inputs for 16-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{FF}$ and $\overline{HF}$ go HIGH. $\overline{EF}$ and $\overline{AEF}$ go LOW. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be high during the $\overline{RS}$ cycle. Also the First Load pin ($\overline{FL}$) is programmed only during Reset.
$\overline{W}$	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
$\overline{FL}$/DIR	First Load/ Direction	I	This is a dual purpose input used in the width and depth expansion configurations. The First Load ($\overline{FL}$) function is programmed only during Reset ($\overline{RS}$) and a LOW on $\overline{FL}$ indicates the first device to be loaded with a byte of data. All other devices should be programmed HIGH. The Direction (DIR) pin controls shift direction after Reset and tells the device whether to read out the Least Significant or Most Significant bit first.
RSIX	Read Serial In Expansion	I	In the single device configuration, RSIX is set HIGH. In depth expansion or daisy chain expansion, RSIX is connected to RSOX (expansion out) of the previous device.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out LSB or MSB depending on the Direction pin programming. During Expansion the SO pins are tied together.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes LOW, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is HIGH, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes LOW, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is HIGH, the device is not empty.
$\overline{HF}$	Half-Full Flag	O	When $\overline{HF}$ is LOW, the device is more than half-full. When $\overline{HF}$ is HIGH, the device is empty to half-full.
RSOX/$\overline{AEF}$	Read Serial Out Expansion Almost-Empty, Almost-Full Flag	O	This is a dual purpose output. In the single device configuration (RSIX HIGH), this is an $\overline{AEF}$ output pin. When $\overline{AEF}$ is LOW, the device is empty-to-(1/8 full -1) or (7/8 full +1)-to-full. When $\overline{AEF}$ is HIGH, the device is 1/8-full up to 7/8-full. In the Expansion configuration (RSOX connected to RSIX of the next device) a pulse is sent from RSOX to RSIX to coordinate the width, depth or daisy chain expansion.
Vcc	Power Supply		Single power supply of 5V.
GND	Ground		Single ground of 0V.

2665 tbl 01

STATUS FLAGS

Number of Words in FIFO						
IDT72105	IDT72115	IDT72125	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	0	H	L	H	L
1–31	1–63	1–127	H	L	H	H
32–128	64–256	128–512	H	H	H	H
129–224	257–448	513–896	H	H	L	H
225–255	449–511	897–1023	H	L	L	H
256	512	1024	L	L	L	H

2665 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to + 7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to + 125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2665 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}(1)	Input Low Voltage	—	—	0.8	V

NOTE: 2665 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial Vcc = 5.0V ± 10%, T_A = 0°C to +70°C)

		IDT72105/IDT72115/ IDT72125 Commercial			
Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{IL}(1)	Input Leakage Current (Any Input)	–1	—	1	µA
I_{OL}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA(5)	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA(6)	—	—	0.4	V
I_{CC1} (3)	Power Supply Current	—	50	100	mA
I_{CC2} (3)	Average Standby Current ($\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/DIR = V_{IH})(SOCP = V_{IL})	—	4	8	mA
I_{CC3} (3,4,7)	Power Down Current	—	1	6	mA

NOTES: 2665 tbl 05

1. Measurements with 0.4V ≤ V_{IN} ≤ Vcc.
2. SOCP = V_{IL}, 0.4 ≤ V_{OUT} ≤ Vcc.
3. Icc measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL}$/DIR = $\overline{W}$ = Vcc - 0.2V; SOCP = 0.2V; all other inputs ≥ Vcc - 0.2 or ≤ 0.2V.
5. For SO, I_{OUT} = -4mA.
6. For SO, I_{OUT} = 16mA.
7. Measurements are made after reset.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Figure	COM'L 72105L25 72115L25 72125L25 Min.	Max.	COM'L 72105L50 72115L50 72125L50 Min.	Max.	Unit
t_S	Parallel Shift Frequency	—	—	28.5	—	15	MHz
t_{SOCP}	Serial Shift Frequency	—	—	50	—	40	MHz
PARALLEL INPUT TIMINGS							
t_{WC}	Write Cycle Time	2	35	—	65	—	ns
t_{WPW}	Write Pulse Width	2	25	—	50	—	ns
t_{WR}	Write Recovery Time	2	10	—	15	—	ns
t_{DS}	Data Set-up Time	2	12	—	15	—	ns
t_{DH}	Data Hold Time	2	0	—	2	—	ns
t_{WEF}	Write High to $\overline{EF}$ HIGH	5, 6	—	35	—	45	ns
t_{WFF}	Write Low to $\overline{FF}$ LOW	4, 7	—	35	—	45	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	8	—	35	—	45	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ HIGH	7	25	—	50	—	ns
SERIAL OUTPUT TIMINGS							
t_{SOCP}	Serial Clock Cycle Time	3	20	—	25	—	ns
t_{SOCW}	Serial Clock Width HIGH/LOW	3	8	—	10	—	ns
t_{SOPD}	SOCP Rising Edge to SO Valid Data	3	—	14	—	15	ns
t_{SOHZ}	SOCP Rising Edge to SO at High-Z[1]	3	3	14	3	15	ns
t_{SOLZ}	SOCP Rising Edge to SO at Low-Z[1]	3	3	14	3	15	ns
t_{SOCEF}	SOCP Rising Edge to $\overline{EF}$ LOW	5, 6	—	35	—	45	ns
t_{SOCFF}	SOCP Rising Edge to $\overline{FF}$ HIGH	4, 7	—	35	—	45	ns
t_{SOCF}	SOCP Rising Edge to Transitioning $\overline{HF}$, $\overline{AEF}$	8	—	35	—	45	ns
t_{REFSO}	SOCP Delay After $\overline{EF}$ HIGH	6	35	—	65	—	ns
RESET TIMINGS							
t_{RSC}	Reset Cycle Time	1	35	—	65	—	ns
t_{RS}	Reset Pulse Width	1	25	—	50	—	ns
t_{RSS}	Reset Set-up Time	1	25	—	50	—	ns
t_{RSR}	Reset Recovery Time	1	10	—	15	—	ns
EXPANSION MODE TIMINGS							
t_{FLS}	$\overline{FL}$ Set-up Time to $\overline{RS}$ Rising Edge	9	7	—	8	—	ns
t_{FLH}	$\overline{FL}$ Hold Time to $\overline{RS}$ Rising Edge	9	0	—	2	—	ns
t_{DIRS}	DIR Set-up Time to SOCP Rising Edge	9	10	—	12	—	ns
t_{DIRH}	DIR Hold Time from SOCP Rising Edge	9	5	—	5	—	ns
t_{SOXD1}	SOCP Rising Edge to RSOX Rising Edge	9	—	15	—	17	ns
t_{SOXD2}	SOCP Rising Edge to RSOX Falling Edge	9	—	15	—	17	ns
t_{SIXS}	RSIX Set-up Time to SOCP Rising Edge	9	5	—	8	—	ns
t_{SIXPW}	RSIX Pulse Width	9	10	—	15	—	ns

NOTE:
1. Values guaranteed by design.

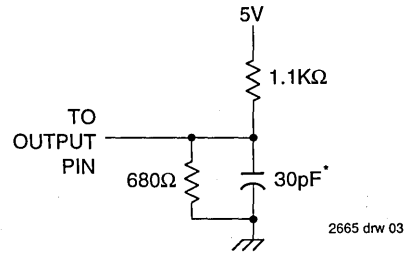
2665 tbl 06

5

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2665 tbl 07



or equivalent circuit

Figure A. Output Load

*Includes jig and scope capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:
1. This parameter is sampled and not 100% tested.

2665 tbl 08

FUNCTIONAL DESCRIPTION

Parallel Data Input

The device must be reset before beginning operation so that all flags are set to their initial state. In width or depth expansion the First Load pin ($\overline{FL}$) must be programmed to indicate the first device.

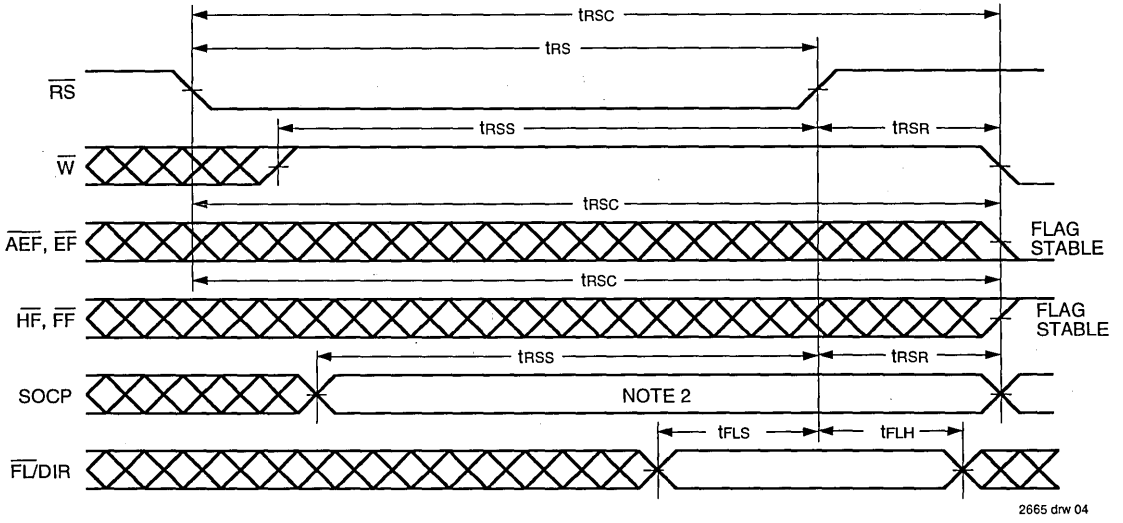
The data is written into the FIFO in parallel through the D0-15 input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full Flag ($\overline{FF}$) is already set, the write line is internally inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP.

The serial word is shifted out Least Significant Bit or Most Significant Bit first, depending on the $\overline{FL}$/DIR level during operation. A LOW on DIR will cause the Least Significant Bit to be read out first. A HIGH on DIR will cause the Most Significant Bit to be read out first.



NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ and $\overline{AEF}$ may change status during Reset, but flags will be valid at tRSC.
2. SOCP should be in the steady LOW or HIGH during tRSS. The first LOW-HIGH (or HIGH-LOW) transition can begin after tRSR.

Figure 1. Reset

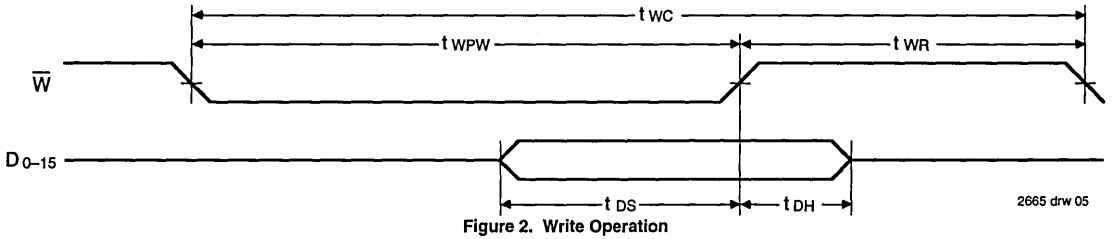
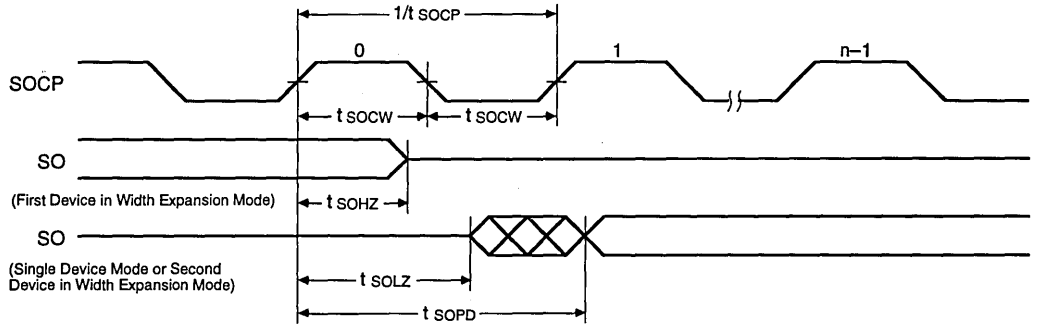


Figure 2. Write Operation



NOTE:
1. In Single Device Mode, SO will not tri-state except after reset.

Figure 3. Read Operation

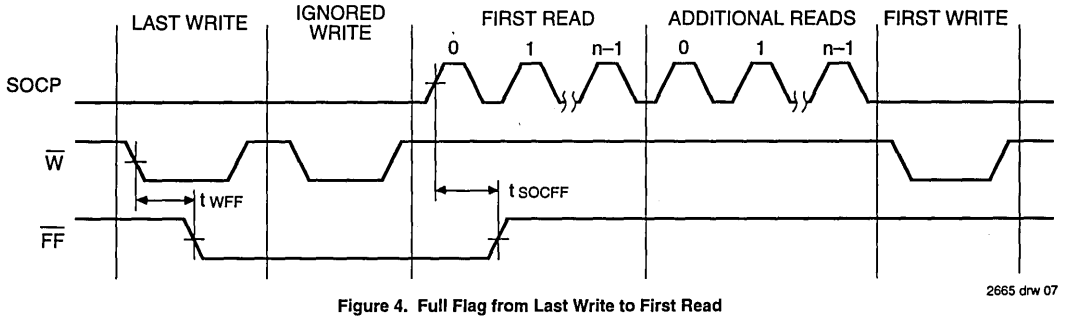
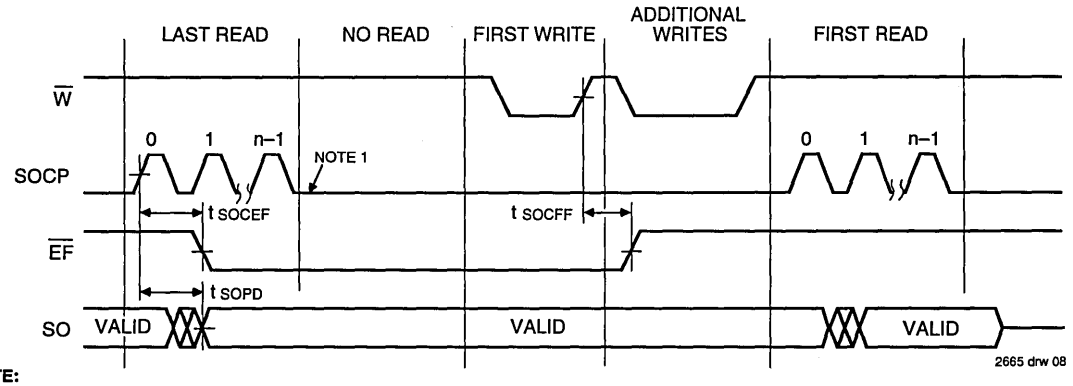
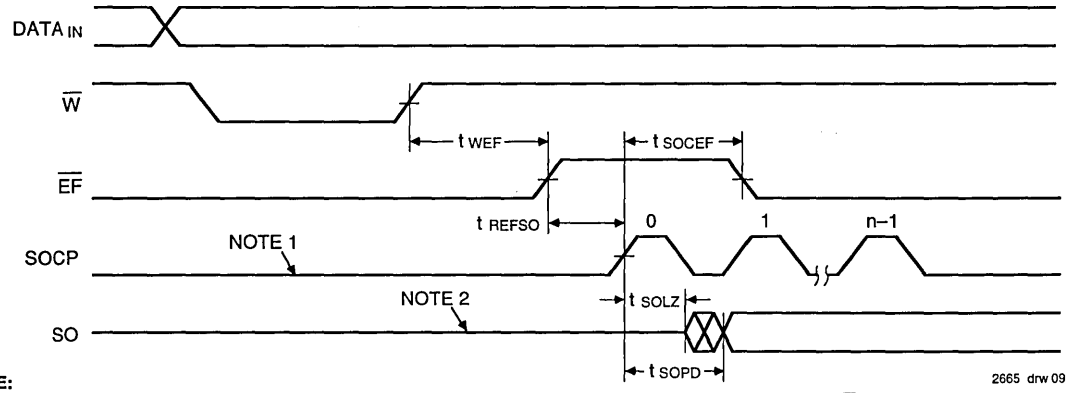


Figure 4. Full Flag from Last Write to First Read



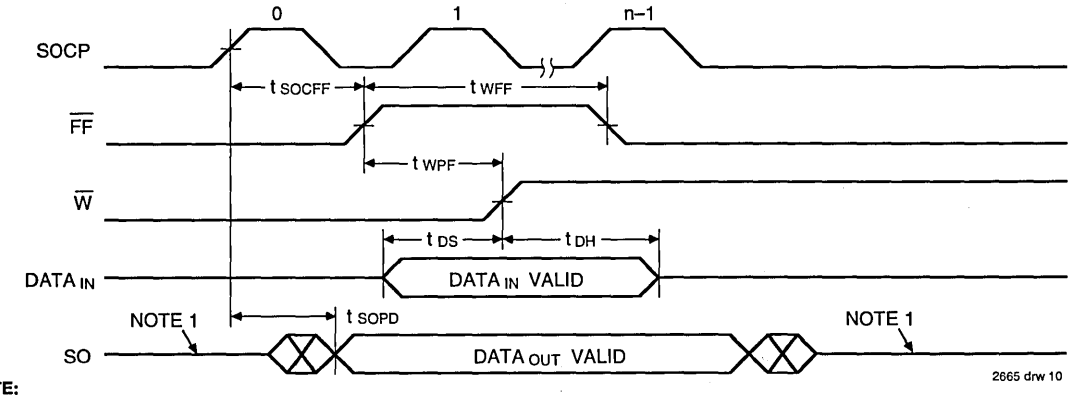
NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes HIGH.

Figure 5. Empty Flag from Last Read to First Write



NOTE:
1. Once $\overline{EF}$ has gone LOW and the last bit of the final word has been shifted out, SOCP should not be clocked until $\overline{EF}$ goes HIGH.
2. In Single Device Mode, SO will not tri-state except after Reset. It will retain the last valid data.

Figure 6. Empty Boundary Condition Timing



NOTE:
1. Single Device Mode will not tri-state but will retain the last valid data.

Figure 7. Full Boundary Condition Timing

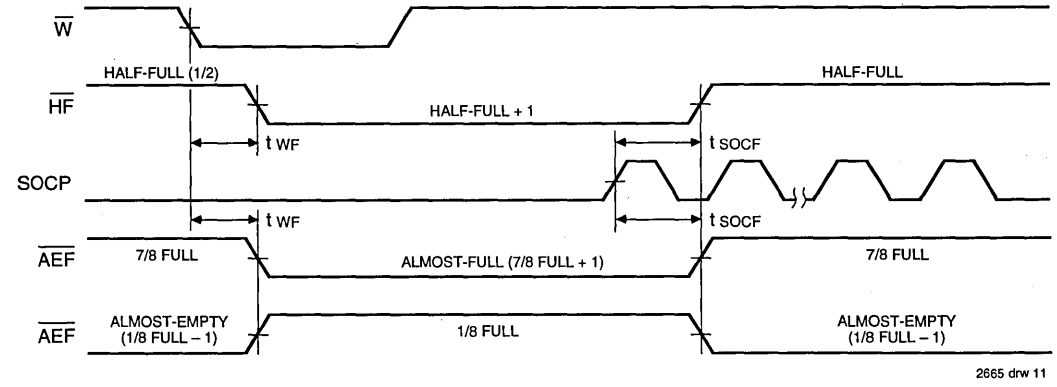


Figure 8. Half-Full, Almost-Full and Almost-Empty Timings

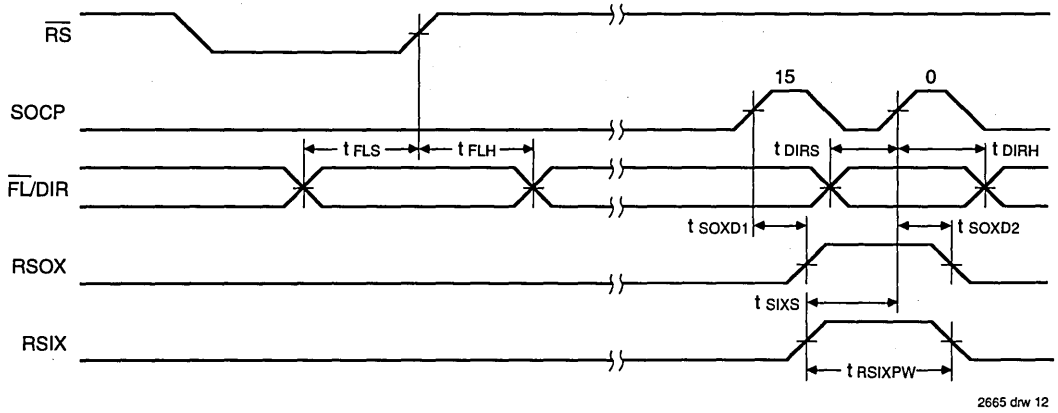


Figure 9. Serial Read Expansion

OPERATING CONFIGURATIONS

Single Device Mode

The device must be reset before beginning operation so that all flags are set to location zero. In the standalone case, the RSIX line is tied HIGH and indicates single device operation to the device. The RSOX/$\overline{AEF}$ pin defaults to $\overline{AEF}$ and outputs the Almost-Empty and Almost-Full Flag.

Width Expansion Mode

In the cascaded case, word widths of more than 16 bits can be achieved by using more than one device. By tying the RSOX and RSIX pins together, as shown in Figure 11, and programming which is the Least Significant Device, a cascaded serial word is achieved. The Least Significant Device is programmed by a LOW on the $\overline{FL}$/DIR pin during reset. All other devices should be programmed HIGH on the $\overline{FL}$/DIR pin at reset.

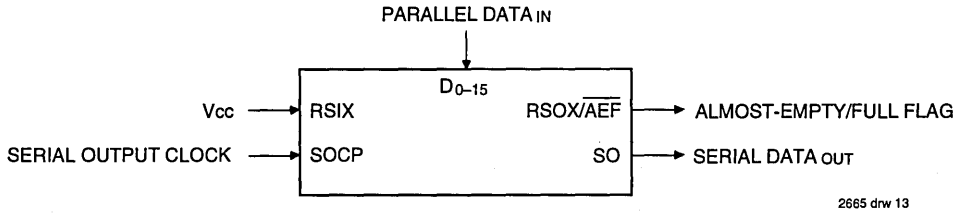


Figure 10. Single Device Configuration

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}$	DIR	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	X	Location Zero	Location Zero	0	1	1
Read/Write	1	X	0,1	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

2665 tbl 09

Table 1. Reset and First Load Truth Table–Single Device Configuration

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit bus. NOTE: After reset, the level on the $\overline{FL}$/DIR pin decides if the Least Significant or Most Significant Bit is read first out of each device.

The three flag outputs, Empty ($\overline{EF}$), Half-Full ($\overline{HF}$) and Full ($\overline{FF}$), should be taken from the Most Significant Device (in the example, FIFO #2). The Almost-Empty/Almost-Full flag is not available. The RSOX pin is used for expansion.

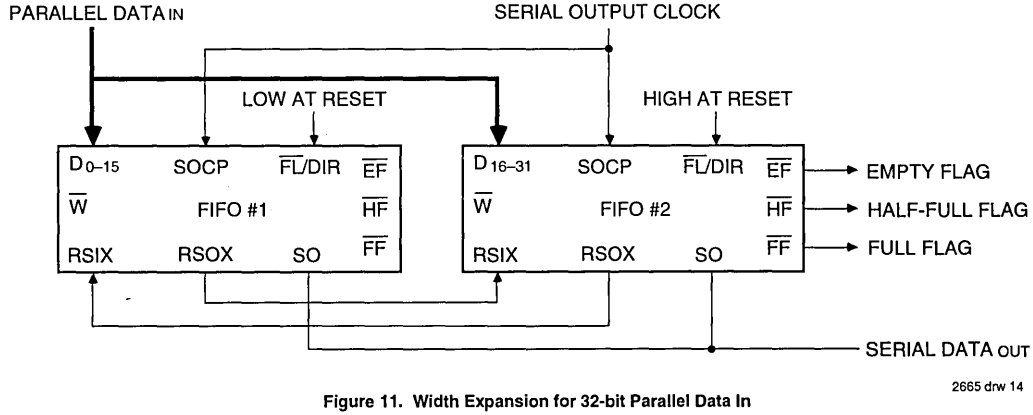


Figure 11. Width Expansion for 32-bit Parallel Data In

Depth Expansion (Daisy Chain) Mode

The IDT72105/15/25 can easily be adapted to applications requiring greater than 1024 words. Figure 12 demonstrates Depth Expansion using three IDT72105/15/25s and an IDT74FCT138 Address Decoder. Any depth can be attained by adding additional devices. The Address Decoder is necessary to determine which FIFO is being written. A word of data must be written sequentially into each FIFO so that the data will be read in the correct sequence. The IDT72105/15/25 operates in the Depth Expansion Mode when the following conditions are met:

1. The first device must be programmed by holding $\overline{FL}$ LOW at Reset. All other devices must be programmed by holding $\overline{FL}$ HIGH at reset.
2. The Read Serial Out Expansion pin (RSOX) of each device must be tied to the Read Serial In Expansion pin (RSIX) of the next device (see Figure 12).
3. External logic is needed to generate composite Empty, Half-Full and Full Flags. This requires the OR-ing of all $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ Flags.
4. The Almost-Empty and Almost-Full Flag is not available due to using the RSOX pin for expansion.

Compound Expansion (Daisy Chain) Mode

The IDT72105/15/25 can be expanded in both depth and width as Figure 13 indicates:

1. The RSOX-to-RSIX expansion signals are wrapped around sequentially.
2. The write ($\overline{W}$) signal is expanded in width.
3. Flag signals are only taken from the Most Significant Devices.
4. The Least Significant Device in the array must be programmed with a LOW on $\overline{FL}$/DIR during reset.

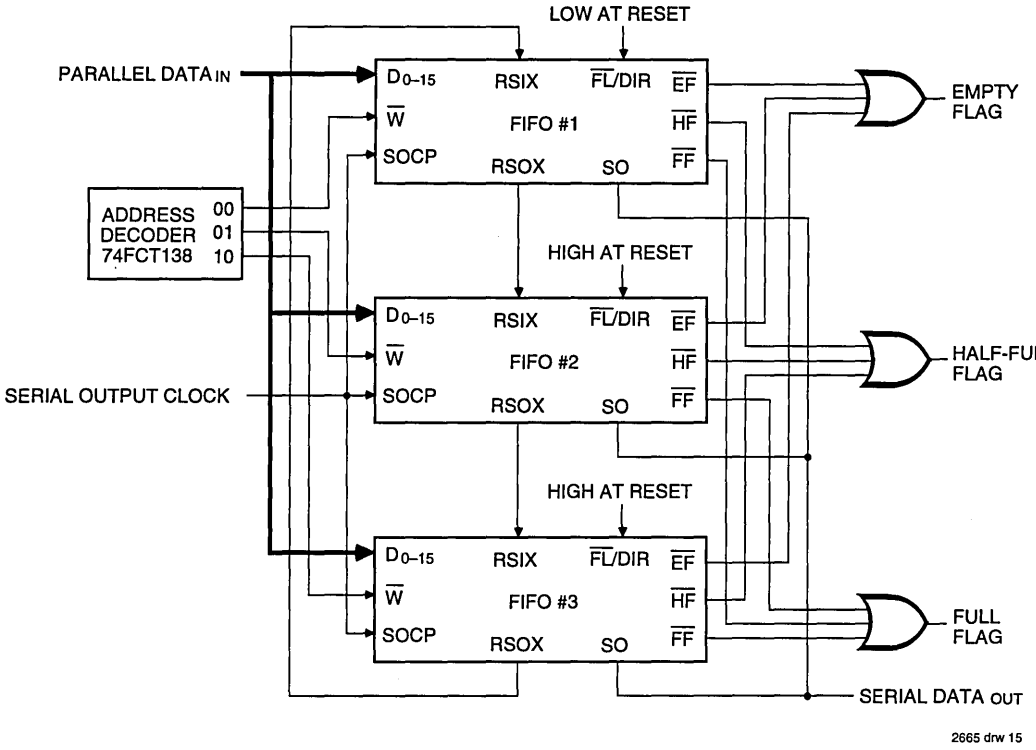


Figure 12. A 3K x 16 Parallel-to-Serial FIFO using the IDT72125

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	DIR	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{HF}$, $\overline{FF}$
Reset-First Device	0	0	X	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	X	Location Zero	Location Zero	0	1
Read/Write	1	X	0,1	X	X	X	X

NOTE: 2665 tbl 10
1. $\overline{RS}$ = Reset Input, $\overline{FL}$/FIR = First Load/Direction, $\overline{EF}$ = Empty Flag Output, $\overline{HF}$ = Half- Full Flag Output, $\overline{FF}$ = Full Flag Output.

Table 2. Reset and First Load Truth Table–Width/Depth Compound Expansion Mode

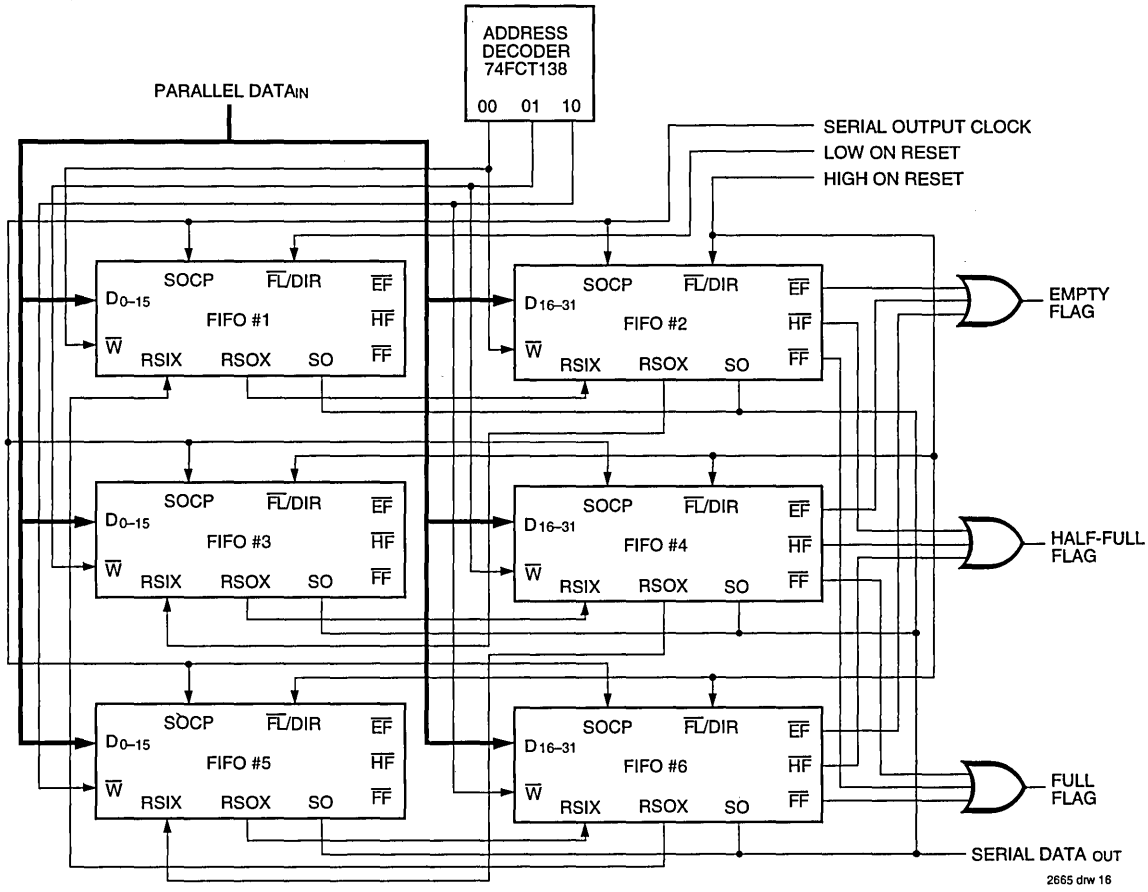
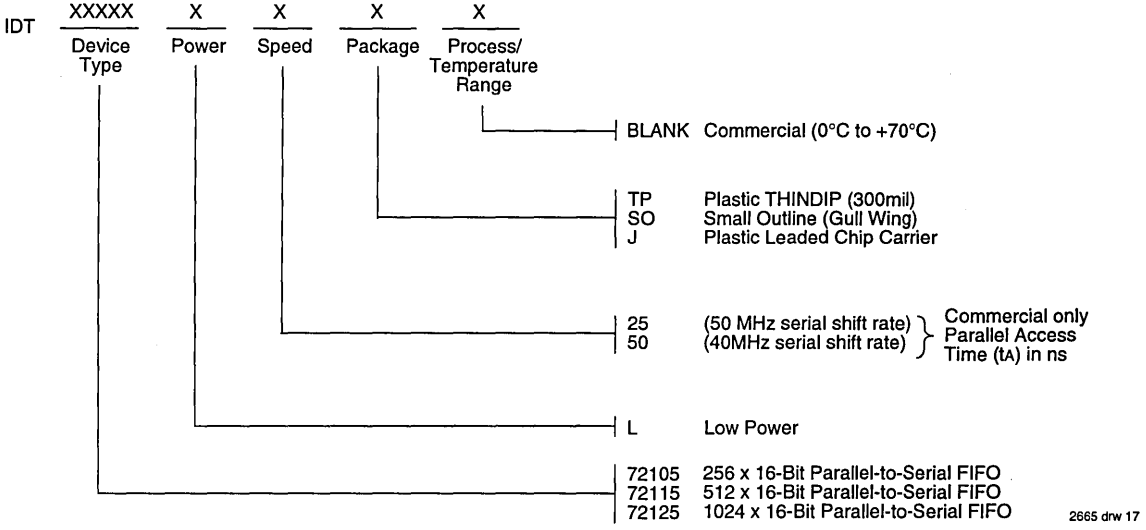


Figure 13. A 3K x 32 Parallel-to-Serial FIFO using the IDT72125

ORDERING INFORMATION



2665 drw 17

5

Integrated Device Technology, Inc.

CMOS PARALLEL-TO-SERIAL FIFO
2048 x 9
4096 x 9

IDT72131
IDT72141

FEATURES:

- 35ns parallel port access time, 45ns cycle time
- 50MHz serial port shift rate
- Expandable in depth and width with no external components
- Programmable word lengths including 7-9, 16-18, 32-36 bit using Flexishift™ serial output without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-Port zero fall-through architecture
- Retransmit capability in single device mode
- Produced with high-performance, low power CMOS technology
- Available in 28-pin ceramic and plastic DIP.
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

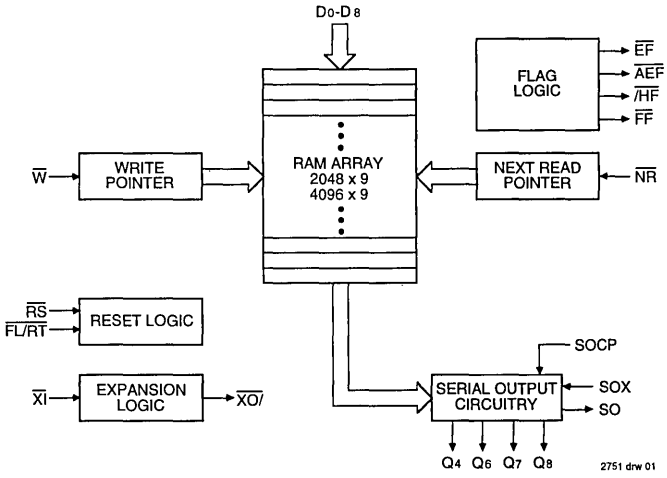
The IDT72131/72141 are high-speed, low power parallel-to-serial FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). The IDT72131/72141 can be configured with the IDTs serial-to-parallel FIFOs (IDT72132/72142) for bidirectional serial data buffering.

The FIFO has a 9-bit parallel input port and a serial output port. Wider and deeper parallel-to-serial data buffers can be built using multiple IDT72131/72141 chips. IDTs unique Flexishift serial expansion logic (SOX, $\overline{NR}$) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. The IDT72131/141 can also be directly connected for depth expansion.

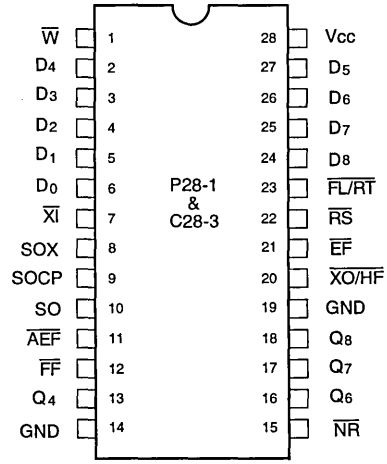
Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The almost-full (7/8), half-full, and almost empty (1/8) flags signal memory utilization within the FIFO.

The IDT72131/72141 is fabricated using IDTs high-speed submicron CMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP
TOP VIEW

2751 drw 02a

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_0–D_8	Inputs	I	Data inputs for 9-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go HIGH, and $\overline{AEF}$ and $\overline{EF}$ go LOW. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be HIGH and SOCP must be LOW during $\overline{RS}$ cycle.
$\overline{W}$	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
$\overline{NR}$	Next Read	I	To program the Serial Out data word width , connect $\overline{NR}$ with one of the Data Set pins (Q_4, Q_6, Q_7 and Q_8). For example, $\overline{NR}$ - Q_7 programs for a 8-bit Serial Out word width.
$\overline{FL}/\overline{RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL}/\overline{RT}$-LOW) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{W}$ must be high and SOCP must be low before setting $\overline{FL}/\overline{RT}$ LOW. Retransmit is not compatible with depth expansion. In the depth expansion configuration, $\overline{FL}/\overline{RT}$ grounded indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
SOX	Serial Output Expansion	I	In the Serial Output Expansion mode, the SOX pin of the least significant device is tied HIGH. The SOX pin of all other devices is connected to the Q_8 pin of the previous device. Data is then clocked out least significant bit first. For single device operation, SOX is tied HIGH.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out Least Significant Bit first. In the Serial Width Expansion mode the SO pins are tied together and each SO pin is tristated at the end of the byte.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes LOW, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is HIGH, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes LOW, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is HIGH, the device is not empty. See the description on page 6 for more details.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is LOW, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is HIGH, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO}/\overline{HF}$	Expansion Out/ Half-Full Flag	O	This is a dual-purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when HF is LOW. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
Q_4, Q_6, Q_7 and Q_8	Data Set	O	The appropriate Data Set pin (Q_4, Q_6, Q_7 and Q_8) is connected to $\overline{NR}$ to program the Serial Out data word width. For example: Q_6 - $\overline{NR}$ programs a 7-bit word width, Q_8 - $\overline{NR}$ programs a 9-bit word width, etc.
Vcc	Power Supply		Single Power Supply of 5V.
GND	Ground		Single ground at 0V.

2751 tbl 01

STATUS FLAGS

Number of Words in FIFO					
IDT72131	IDT72141	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	H	L	H	L
1-255	1-511	H	L	H	H
256-1024	512-2048	H	H	H	H
1025-1792	2049-3584	H	H	L	H
1793-2047	3585-4095	H	L	L	H
2048	4096	L	L	L	H

2751 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2751 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage	—	—	0.8	V

NOTE: 2751 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2751 tbl 05

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = –55°C to +125°C)

Symbol	Parameter	IDT72131/IDT72141 Commercial			IDT72131/IDT72141 Military			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}(1)	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	µA
I_{OL}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OUT} = -8mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 16mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Power Supply Current	—	90	140	—	100	160	mA
I_{CC2}(3)	Average Standby Current ($\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (SOCP = V_{IL})	—	8	12	—	12	25	mA
$I_{CC3(L)}$(3,4)	Power Down Current	—	—	2	—	—	4	mA

NOTES: 2751 tbl 06

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. SOCP ≤ V_{IL}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. I_{CC} measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL/RT}$ = $\overline{W}$ = V_{CC} -0.2V; SOCP ≤ 0.2V; all other inputs ≥ V_{CC} -0.2V or ≤ 0.2V.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)

		Commercial		Military		Mil. and Com'l.		
		IDT72131L35 IDT72141L35		IDT72131L40 IDT72141L40		IDT72131L50 IDT72141L50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Parallel Shift Frequency	—	22.2	—	20	—	15	MHz
t_{SOCP}	Serial-Out Shift Frequency	—	50	—	50	—	40	MHz
PARALLEL INPUT TIMINGS								
t_{DS}	Data Set-up Time	18	—	20	—	30	—	ns
t_{DH}	Data Hold Time	0	—	0	—	5	—	ns
t_{WC}	Write Cycle Time	45	—	50	—	65	—	ns
t_{WPW}	Write Pulse Width	35	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	15	—	ns
t_{WEF}	Write High to $\overline{EF}$ HIGH	—	30	—	35	—	45	ns
t_{WFF}	Write Low to $\overline{FF}$ LOW	—	30	—	35	—	45	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	—	45	—	50	—	65	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ HIGH	35	—	40	—	50	—	ns
SERIAL OUTPUT TIMINGS								
t_{SOHZ}	SOCP Rising Edge to SO at High-Z[1]	5	16	5	16	5	26	ns
t_{SOLZ}	SOCP Rising Edge to SO at Low-Z[1]	5	22	5	22	5	22	ns
t_{SOPD}	SOCP Rising Edge to Valid Data on SO	—	18	—	18	—	18	ns
t_{SOX}	SOX Set-up Time to SOCP Rising Edge	5	—	5	—	5	—	ns
t_{SOCW}	Serial In Clock Width HIGH/LOW	8	—	8	—	10	—	ns
t_{SOCEF}	SOCP Rising Edge (Bit 0 - Last Word) to $\overline{EF}$ LOW	—	20	—	25	—	25	ns
t_{SOCFF}	SOCP Rising Edge to $\overline{FF}$ HIGH	—	30	—	35	—	40	ns
t_{SOCF}	SOCP Rising Edge to $\overline{HF}$, $\overline{AEF}$, HIGH	—	30	—	35	—	40	ns
t_{REFSO}	Recovery Time SOCP After $\overline{EF}$ HIGH	35	—	40	—	50	—	ns
RESET TIMINGS								
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	ns
t_{RS}	Reset Pulse Width	35	—	40	—	50	—	ns
t_{RSS}	Reset Set-up Time	35	—	40	—	50	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	ns
t_{RSF1}	Reset to $\overline{EF}$ and $\overline{AEF}$ LOW	—	45	—	50	—	65	ns
t_{RSF2}	Reset to $\overline{HF}$ and $\overline{FF}$ HIGH	—	45	—	50	—	65	ns
t_{RSQL}	Reset to Q LOW	20	—	20	—	35	—	ns
t_{RSQH}	Reset to Q HIGH	20	—	20	—	35	—	ns
RETRANSMIT TIMINGS								
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	ns
t_{RT}	Retransmit Pulse Width	35	—	40	—	50	—	ns
t_{RTS}	Retransmit Set-up Time	35	—	40	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	ns
DEPTH EXPANSION MODE TIMINGS								
t_{XOL}	Read/Write to $\overline{XO}$ LOW	—	35	—	40	—	50	ns
t_{XOH}	Read/Write to $\overline{XO}$ HIGH	—	35	—	40	—	50	ns
t_{XI}	$\overline{XI}$ Pulse Width	35	—	40	—	50	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	—	15	—	15	—	ns

NOTE:
1. Guaranteed by design minimum times, not tested.

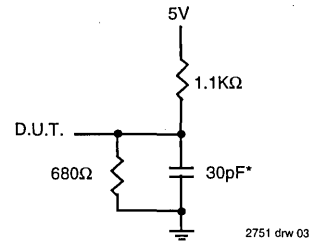
2751 tbl 07

5

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2751 tbl 08



or equivalent circuit

Figure A. Ouput Load
*Including jig and scope capacitances

FUNCTIONAL DESCRIPTION

Parallel Data Input

The data is written into the FIFO in parallel through the D_{0-8} input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full-Flag ($\overline{FF}$) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. The data is written to the RAM at the write pointer. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP. NOTE: SOCP should not be clocked once the last bit of the last word has been clocked out. If it is, then two things will occur. One, the SO pin will go High-Z and two, SOCP will be out of sync with Next Read ($\overline{NR}$).

The serial word is shifted out Least Significant Bit first, that is the first bit will be D0, then D1 and so on up to the serial word width. The serial word width must be programmed by connecting the appropriate Data Set line (Q4, Q6, Q7 or Q8) to the $\overline{NR}$ input. The Data Set lines are taps off a digital delay line. Selecting one of these taps, programs the width of the serial word to be read and shifted out.

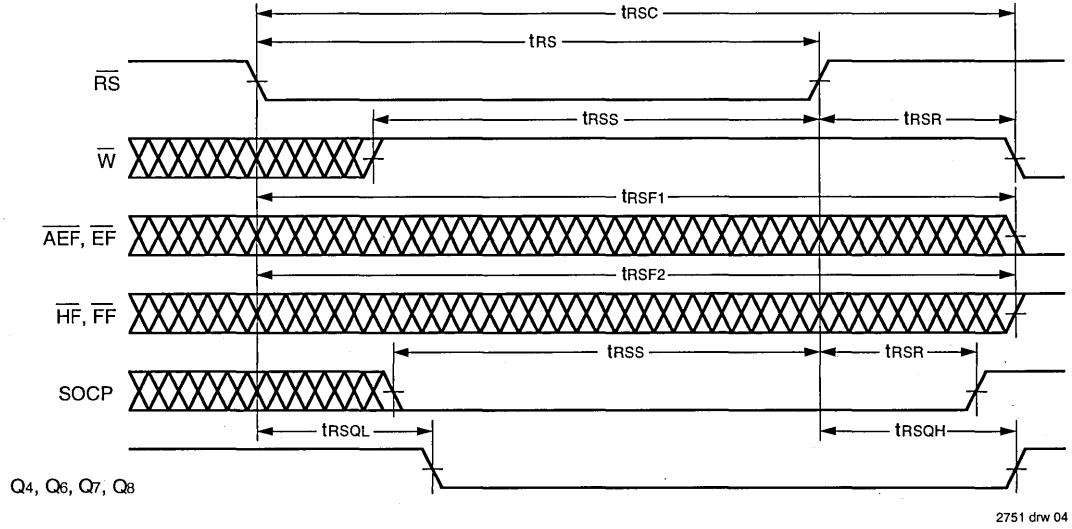


Figure 1. Reset

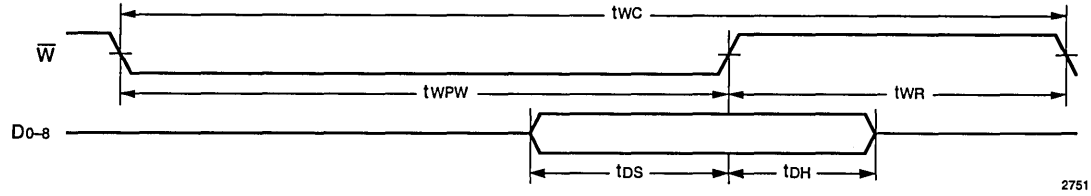


Figure 2. Write Operation

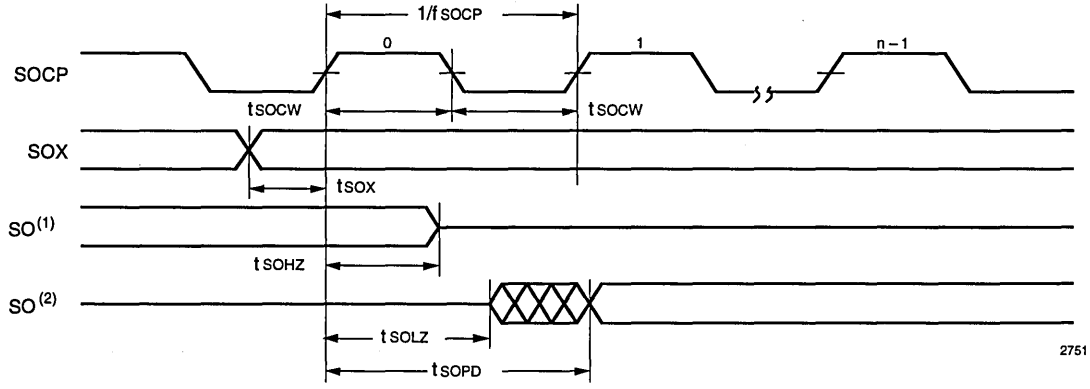


Figure 3. Read Operation

NOTES:
1. This timing applies to the Active Device in Width Expansion Mode.
2. This timing applies to Single Device Mode at Empty Boundary ($\overline{EF}$ = LOW) and the Next Active Device in Width Expansion Mode.

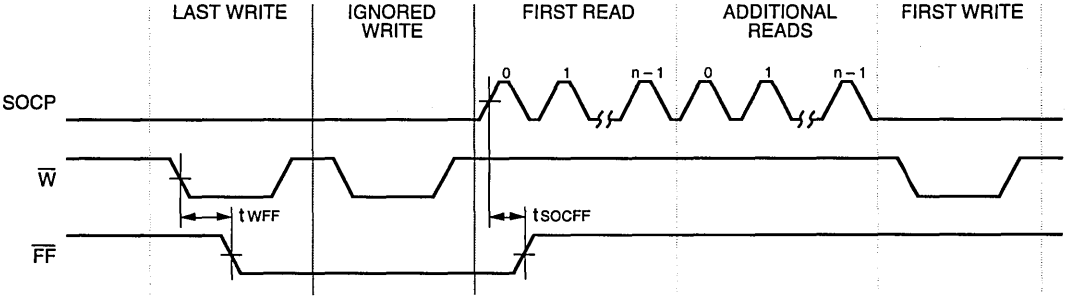
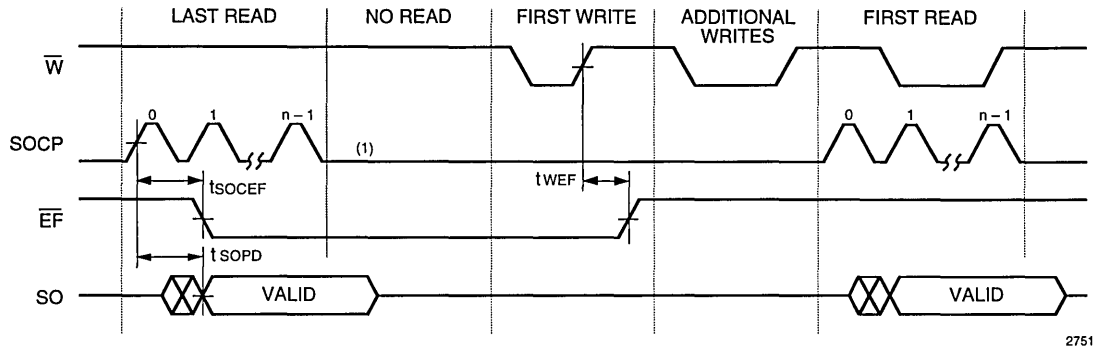
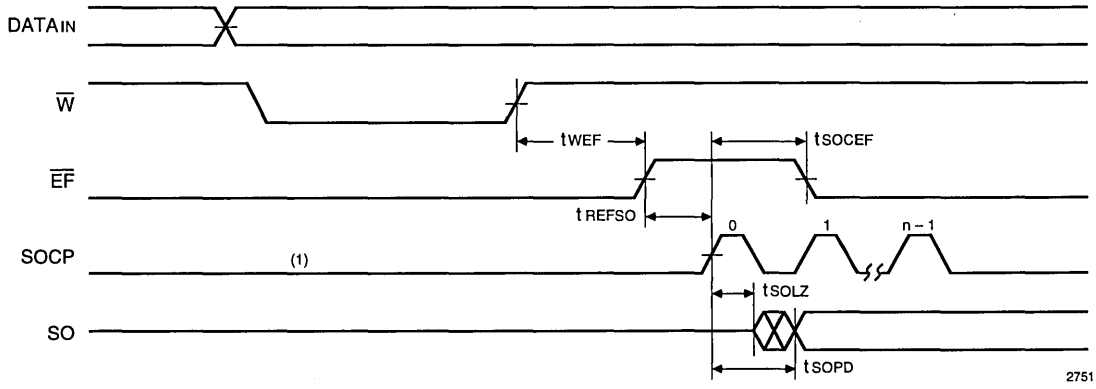


Figure 4. Full Flag from Last Write to First Read



NOTE:
1. Once $\overline{EF}$ has gone LOW and the last bit of the final word has been shifted out, SOCP should not be clocked until $\overline{EF}$ goes HIGH.

Figure 5. Empty Flag from Last Read to First Write



NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes HIGH.

Figure 6. Empty Boundary Condition Timing

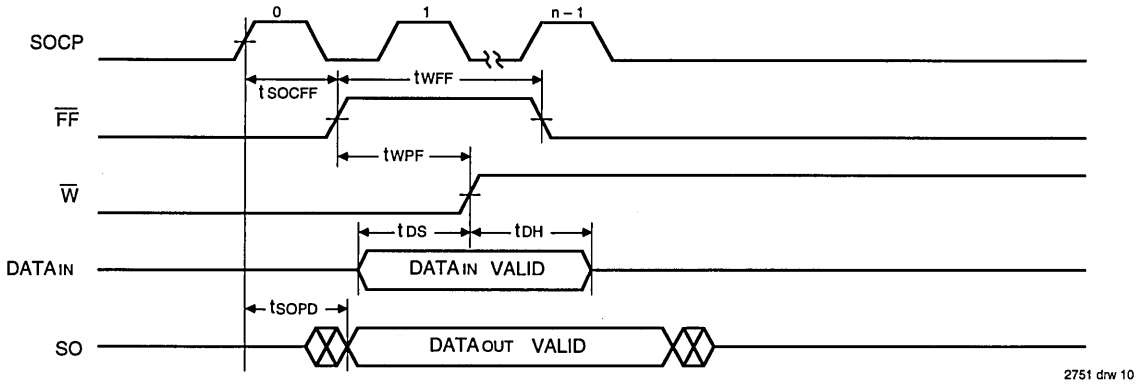


Figure 7. Full Boundry Condition Timing

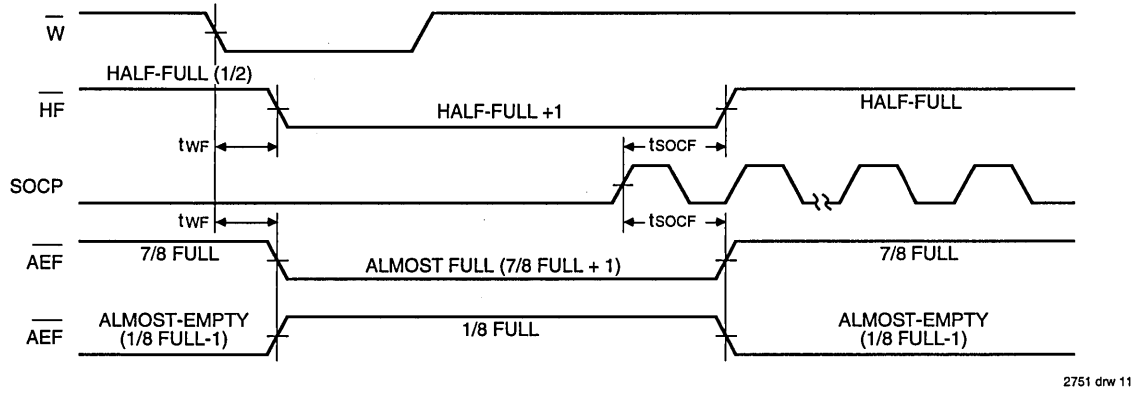
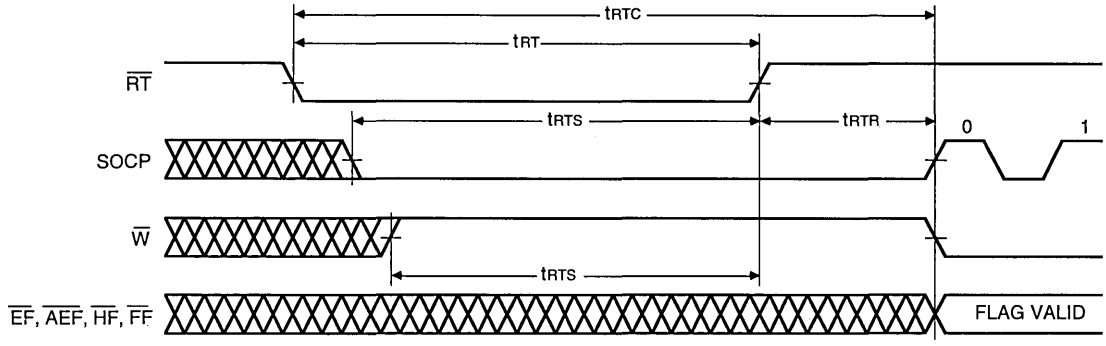


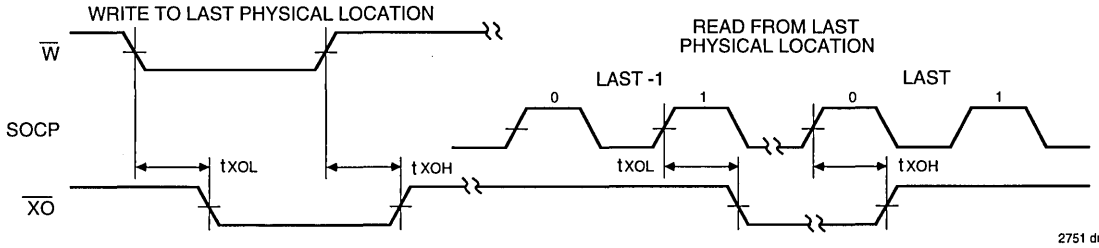
Figure 8. Half Full, Almost Full and Almost Empty Timings



2751 drw 12

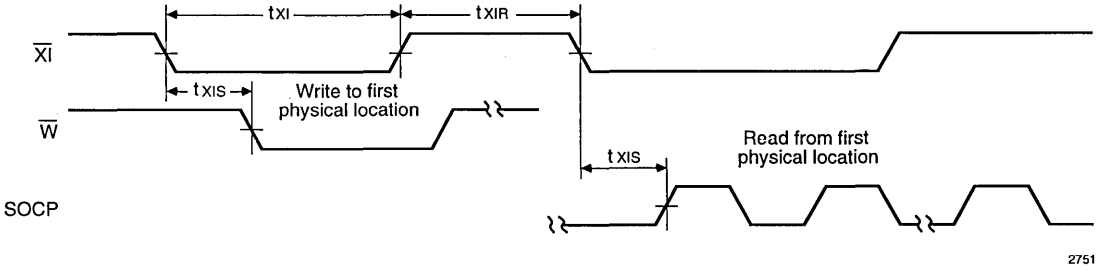
NOTE:
1. EF, AEF, HF and FF may change status during Retransmit, but flags will be valid at tRTC.

Figure 9. Retransmit



2751 drw 13

Figure 10. Expansion-Out



2751 drw 14

Figure 11. Expansion-In

OPERATING CONFIGURATIONS

Single Device Configuration

In the standalone case, the SOX line is tied HIGH and not used. On the first LOW-to-HIGH of the SOCP clock, all of the Data Set lines (Q4, Q6, Q7, Q8) go LOW and a new serial word is started. The Data Set lines then go HIGH on the equivalent SOCP clock pulse. This continues until the Q line connected to $\overline{NR}$ goes HIGH completing the serial word. The cycle is then repeated with the next LOW-to-HIGH transition of SOCP.

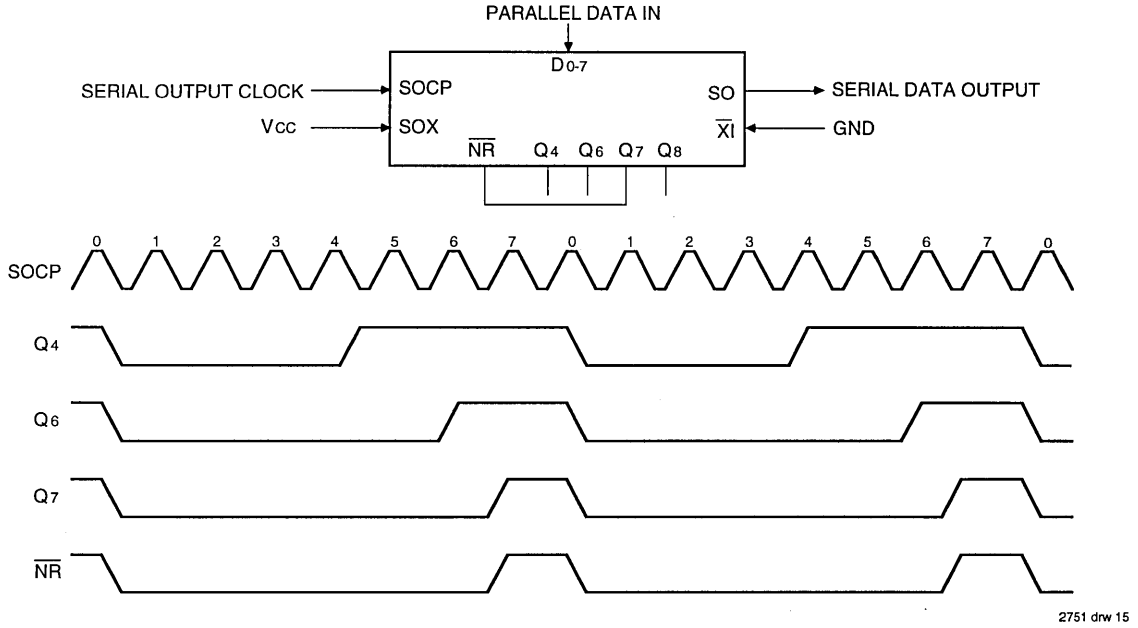


Figure 12. Eight-Bit Word Single Device Configuration

TRUTH TABLES
TABLE 1: RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

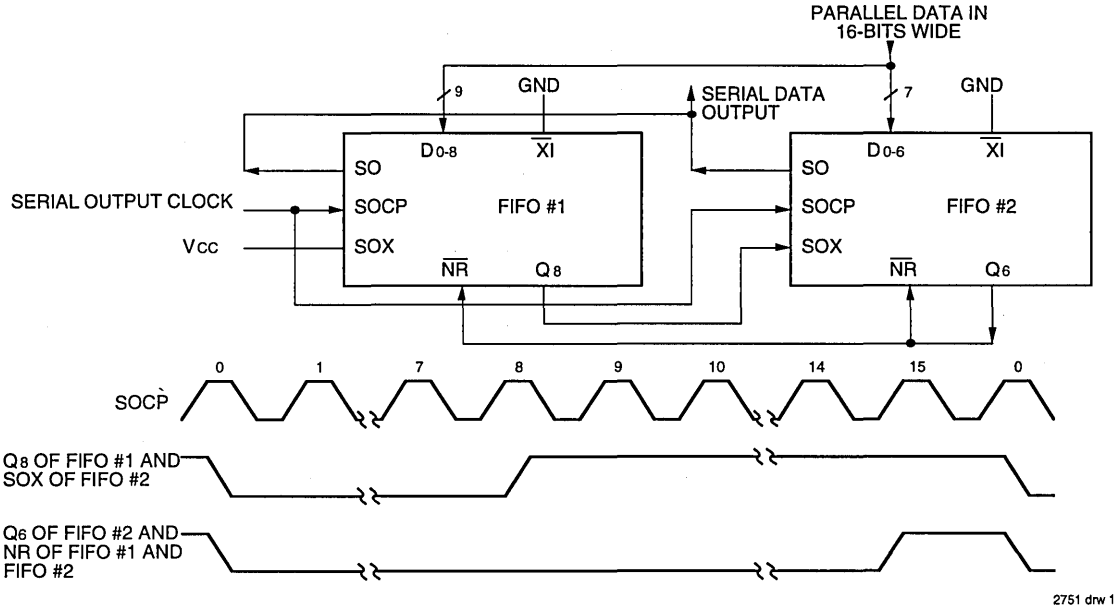
2751 tbl 09

Width Expansion Configuration

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SOX line of the least significant device HIGH and the SOX of the subsequent devices to the appropriate Data Set lines of the previous devices, a cascaded serial word is achieved.

On the first LOW-to-HIGH clock edge of SOCP, all lines go LOW. Just as in the standalone case, on each corresponding clock cycle, the equivalent Data Set line goes HIGH in order of least to most significant. When the Data Set line which is connected to the SOX input of the next device goes HIGH, the D_0 of that device goes HIGH, the cascading from one device to the next. The Data Set line of the most significant bit programs the serial word width by being connected to all NR inputs.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit-bus.



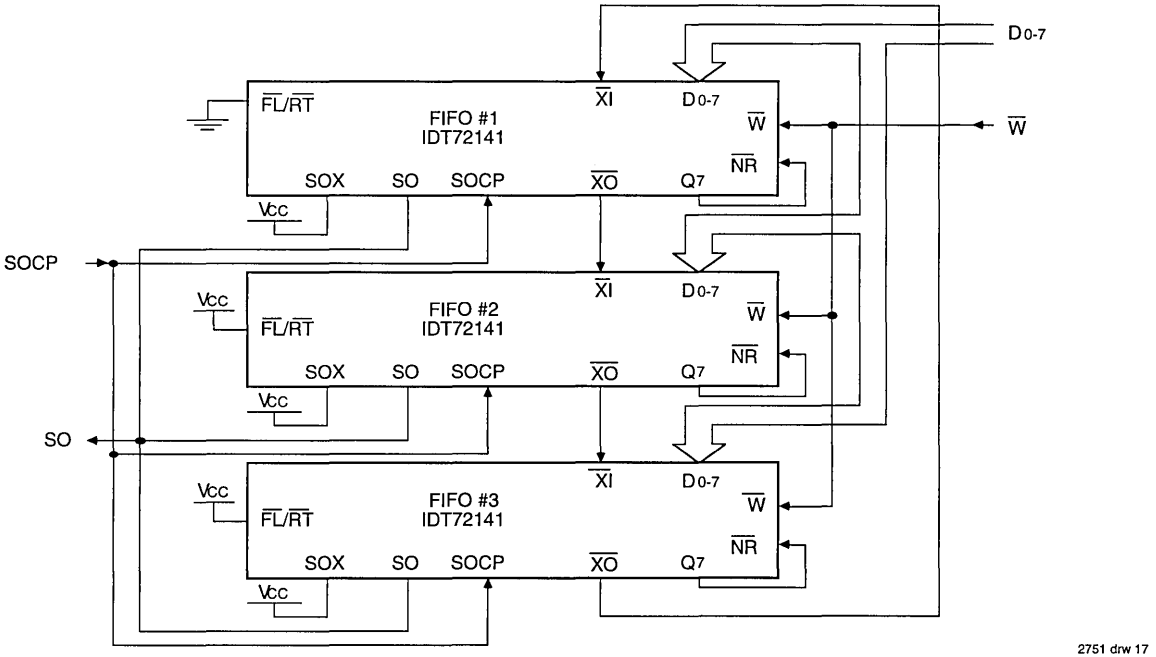
2751 drw 16

Figure 13. Width Wxpansion for 16-bit Parallel Data In. The Parallel Data In is tied to D_{0-8} of FIFO #1 and D_{0-6} of FIFO #2.

Depth Expansion (Daisy Chain) Mode

The IDT72131/41 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 14 demonstrates Depth Expansion using three IDT72131/41. Any depth can be attained by adding additional IDT72131/41 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.



2751 drw 17

Figure 14. A 12K x 8 Parallel-In Serial-Out FIFO

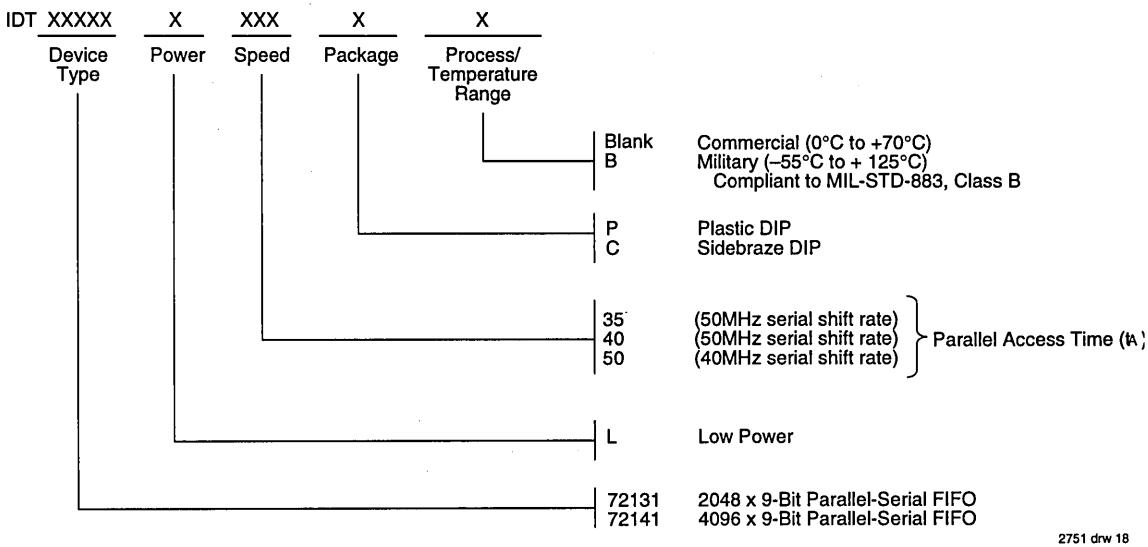
TABLE 2: RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset-All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES: 2751 tbl 10

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Ouput, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

ORDERING INFORMATION



2751 drw 18

Integrated Device Technology, Inc.

CMOS SERIAL-TO-PARALLEL FIFO 2048 x 9 4096 x 9

IDT72132
IDT72142

FEATURES:

- 35ns parallel-port access time, 45ns cycle time
- 50MHz serial port shift rate
- Expandable in depth and width with no external components
- Programmable word lengths including 8, 9, 16-18, and 32-36 bit using Flexshift™ serial input without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-Port zero fall-through architecture
- Retransmit capability in single device mode
- Produced with high-performance, low-power CMOS technology
- Available in the 28-pin ceramic and plastic DIPs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72132/72142 are high-speed, low-power serial-to-parallel FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). The IDT72132/72142 can be configured with the IDTs parallel-to-serial FIFOs (IDT72131/72141) for bidirectional serial data buffering.

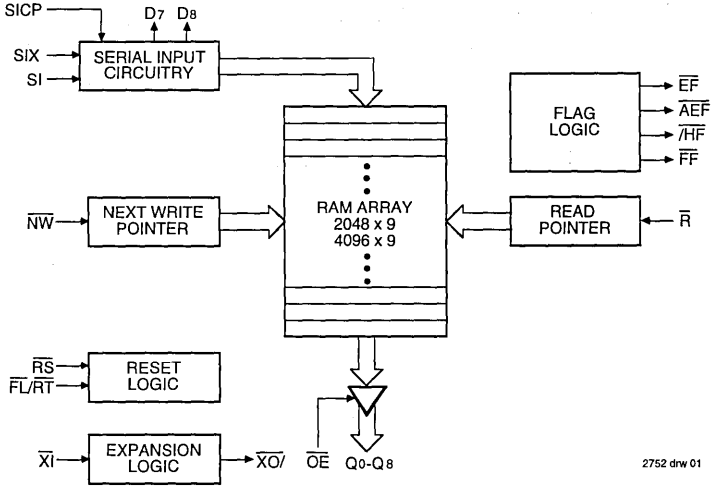
The FIFO has a serial input port and a 9-bit parallel output port. Wider and deeper serial-to-parallel data buffers can be built using multiple IDT72132/72142 chips. IDTs unique Flexshift serial expansion logic (SIX, $\overline{NW}$) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. The IDT72132/142 can also be directly connected for depth expansion.

Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The Almost-Full (7/8), Half-Full, and Almost Empty (1/8) flags signal memory utilization within the FIFO.

The IDT72132/72142 is fabricated using IDTs high-speed submicron CMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

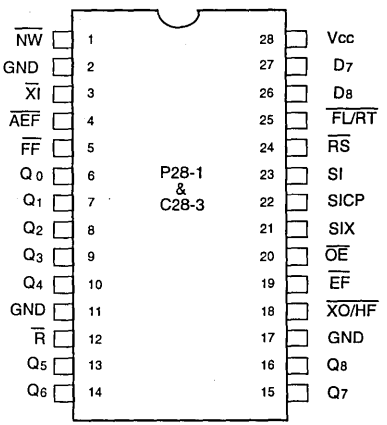
5

FUNCTIONAL BLOCK DIAGRAM



2752 drw 01

PIN CONFIGURATION



DIP
TOP VIEW

2752 drw 02

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
SI	Serial Input	I	Serial data is shifted in least significant bit first. In the serial cascade mode, the Serial Input (SI) pins are tied together and SIX plus D7, D8 determine which device stores the data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go HIGH, and $\overline{AEF}$, and $\overline{EF}$ go LOW. A reset is required before an initial WRITE after power-up. $\overline{R}$ must be HIGH during an $\overline{RS}$ cycle.
$\overline{NW}$	Next Write	I	To program the Serial In word width , connect $\overline{NW}$ with one of the Data Set pins (D7, D8).
SICP	Serial Input Clock	I	Serial data is read into the serial input register on the rising edge of SICP. In both Depth and Serial Word Width Expansion modes, all of the SICP pins are tied together.
$\overline{R}$	Read	I	When READ is LOW, data can be read from the RAM array sequentially, independent of SICP. In order for READ to be active, $\overline{EF}$ must be HIGH. When the FIFO is empty ($\overline{EF}$-LOW), the internal READ operation is blocked and Q0-Q8 are in a high impedance condition.
$\overline{FL}/\overline{RT}$	First Load/ Retransmit	I	This is a dual-purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL}/\overline{RT}$-LOW) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{R}$ must be HIGH and SICP must be LOW before setting $\overline{FL}/\overline{RT}$ LOW. Retransmit is not possible in depth expansion. In the depth expansion configuration, $\overline{FL}/\overline{RT}$ grounded indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
SIX	Serial Input Expansion	I	In the Expansion mode, the SIX pin of the least significant device is tied HIGH. The SIX pin of all other devices is connected to the D7 or D8 pin of the previous device. For single device operation, SIX is tied HIGH.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is set LOW, the parallel output buffers receive data from the RAM array. When $\overline{OE}$ is set HIGH, parallel three state buffers inhibit data flow.
Q0–Q8	Output Data	O	Data outputs for 9-bit wide data.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes LOW, the device is full and data must not be clocked by SICP. When $\overline{FF}$ is HIGH, the device is not full. See the diagram on page 7 for more details.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes LOW, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is HIGH, the device is not empty.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is LOW, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is HIGH, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO}/\overline{HF}$	Expansion Out/ Half-Full Flag	O	This is a dual-purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when $\overline{HF}$ is LOW. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
D7, D8	Data Set	O	The appropriate Data Set pin (D7, D8) is connected to $\overline{NW}$ to program the Serial In data word width. For example: D7 - $\overline{NW}$ programs a 8-bit word width, D8 - $\overline{NW}$ programs a 9-bit word width, etc.
Vcc	Power Supply		Single Power Supply of 5V.
GND	Ground		Three grounds at 0V.

2752 tbl 01

STATUS FLAGS

Number of Words in FIFO					
IDT72132	IDT72142	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	H	L	H	L
1-255	1-511	H	L	H	H
256-1024	512-2048	H	H	H	H
1025-1792	2049-3584	H	H	L	H
1793-2047	3585-4095	H	L	L	H
2048	4096	L	L	L	H

2752 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2752 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage	—	—	0.8	V

NOTE: 2752 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2752 tbl 05

1. This parameter is sampled and not 100% tested.

5

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = –55°C to +125°C)

		IDT72132/IDT72142 Commercial			IDT72132/IDT72142 Military			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
I_{IL}(1)	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	µA
I_{OL}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OUT} = -2mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OUT} = 8mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Power Supply Current	—	90	140	—	100	160	mA
I_{CC2}(3)	Average Standby Current ($\overline{R}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (SICP = V_{IL})	—	8	12	—	12	25	mA
$I_{CC3(L)}$(3,4)	Power Down Current	—	—	2	—	—	4	mA

NOTES: 2752 tbl 06

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. R ≤ V_{IL}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Icc measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL/RT}$ = $\overline{R}$ = V_{CC} -0.2V; SICP ≤ 0.2V; all other inputs ≥ V_{CC} -0.2V or ≤ 0.2V.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = –55°C to +125°C)

		Commercial		Military		Mil. and Com'l.		
		IDT72132L35 IDT72142L35		IDT72132L40 IDT72142L40		IDT72132L50 IDT72142L50		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t_S	Parallel Shift Frequency	—	22.2	—	20	—	15	MHz
t_{SICP}	Serial-InShift Frequency	—	50	—	50	—	40	MHz
PARALLEL OUTPUT TIMINGS								
t_A	Access Time	—	35	—	40	—	50	ns
t_{RR}	Read Recovery Time	10	—	10	—	15	—	ns
t_{RPW}	Read Pulse Width	35	—	40	—	50	—	ns
t_{RC}	Read Cycle Time	45	—	50	—	65	—	ns
t_{RLZ}	Read Pulse LOW to Data Bus at Low-Z[1]	5	—	5	—	10	—	ns
t_{RHZ}	Read Pulse HIGH to Data Bus at High-Z[1]	—	20	—	25	—	30	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	—	5	—	5	—	ns
t_{OEHZ}	Output Enable to High-Z (Disable)[1]	—	15	—	15	—	15	ns
t_{OELZ}	Output Enable to Low-Z (Enable)[1]	5	—	5	—	5	—	ns
t_{AOE}	Output Enable to Data Valid (Q_{0-8})	—	20	—	20	—	22	ns
SERIAL INPUT TIMINGS								
t_{SIS}	Serial Data in Set-Up Time to SICP Rising Edge	12	—	12	—	15	—	ns
t_{SIH}	Serial Data in Hold Time to SICP Rising Edge	0	—	0	—	0	—	ns
t_{SIX}	SIX Set-Up Time to SICP Rising Edge	5	—	5	—	5	—	ns
t_{SICW}	Serial-In Clock Width HIGH/LOW	8	—	8	—	10	—	ns
FLAG TIMINGS								
t_{SICEF}	SICP Rising Edge (Last Bit - First Word) to $\overline{EF}$ HIGH	—	45	—	50	—	65	ns
t_{SICFF}	SICP Rising Edge (Bit 1 - Last Word) to $\overline{FF}$ LOW	—	30	—	35	—	40	ns
t_{SICF}	SICP Rising Edge to $\overline{HF}$, $\overline{AEF}$	—	45	—	50	—	65	ns
t_{RFFSI}	Recovery Time SICP After $\overline{FF}$ Goes HIGH	15	—	15	—	15	—	ns
t_{REF}	Read LOW to $\overline{EF}$ LOW	—	30	—	35	—	45	ns
t_{RFF}	Read HIGH to $\overline{FF}$ HIGH	—	30	—	35	—	45	ns
t_{RF}	Read HIGH to Transitioning $\overline{HF}$ and $\overline{AEF}$	—	45	—	50	—	65	ns
t_{RPE}	Read Pulse Width After $\overline{EF}$ HIGH	35	—	40	—	50	—	ns
RESET TIMINGS								
t_{RSC}	Reset Cycle Time	45	—	50	—	65	—	ns
t_{RS}	Reset Pulse Width	35	—	40	—	50	—	ns
t_{RSS}	Reset Set-up Time	35	—	40	—	50	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	15	—	ns
t_{RSF1}	Reset to $\overline{EF}$ and $\overline{AEF}$ LOW	—	45	—	50	—	65	ns
t_{RSF2}	Reset to $\overline{HF}$ and $\overline{FF}$ HIGH	—	45	—	50	—	65	ns
t_{RSDL}	Reset to D LOW	20	—	20	—	35	—	ns
t_{POI}	SICP Rising Edge to D	5	17	5	17	5	20	ns
RETRANSMIT TIMINGS								
t_{RTC}	Retransmit Cycle Time	45	—	50	—	65	—	ns
t_{RT}	Retransmit Pulse Width	35	—	40	—	50	—	ns
t_{RTS}	Retransmit Set-up Time	35	—	40	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	10	—	15	—	ns
DEPTH EXPANSION MODE TIMINGS								
t_{XOL}	Read/Write to $\overline{XO}$ LOW	—	40	—	45	—	50	ns
t_{XOH}	Read/Write to $\overline{XO}$ HIGH	—	40	—	45	—	50	ns
t_{XI}	$\overline{XI}$ Pulse Width	35	—	40	—	50	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	16	—	15	—	15	—	ns

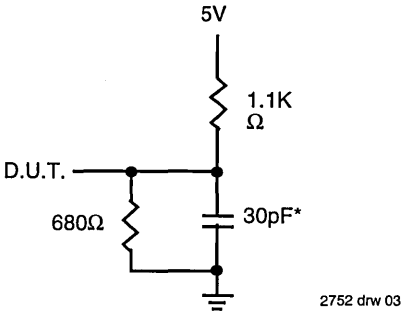
NOTE:
1. Guaranteed by design minimum times, not tested

2752 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2752 tbl 08



or equivalent circuit

Figure A. Output Load
*Includies jig and scope capacitances

FUNCTIONAL DESCRIPTION

Serial Data Input

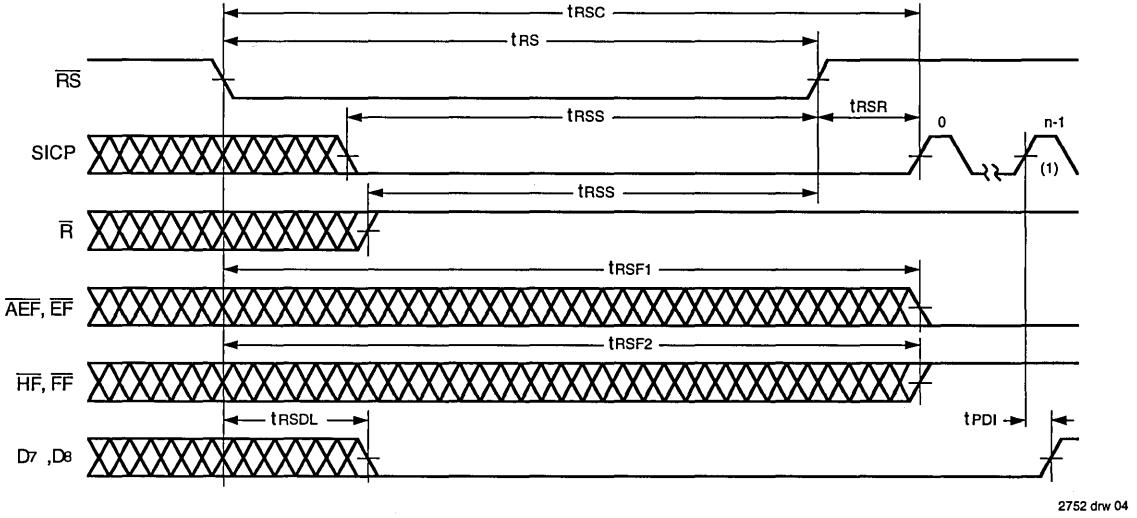
The serial data is input on the SI pin. The data is clocked in on the rising edge of SICP providing the Full Flag ($\overline{FF}$) is not asserted. If the Full Flag is asserted then the next parallel data word is inhibited from moving into the RAM array. NOTE: SICP should not be clocked once the last bit of the last word has been shifted in, as indicated by $\overline{NW}$ HIGH and $\overline{FF}$ LOW. If it is, then the input data will be lost.

The serial word is shifted in Least Significant Bit first. Thus, when the FIFO is read, the Least Significant Bit will come out on Q_0 and the second bit is on Q_1 and so on. The serial word width must be programmed by connecting the appropriate Data Set line (D_7, D_8) to the $\overline{NW}$ input. The data set lines are taps off a digital delay line. Selecting one of these taps programs the width of the serial word to be written in.

Parallel Data Output

A read cycle is initiated on the falling edge of Read ($\overline{R}$) provided the Empty Flag is not set. The output data is accessed on a first-in/first-out basis, independent of the ongoing write operations. The data is available t_A after the falling edge of $\overline{R}$ and the output bus Q goes into high impedance after $\overline{R}$ goes HIGH.

Alternately, the user can access the FIFO by keeping $\overline{R}$ LOW and enabling data on the bus by asserting Output Enable ($\overline{OE}$). When $\overline{R}$ is LOW, the $\overline{OE}$ signal enables data on the output bus. When $\overline{R}$ is LOW and $\overline{OE}$ is HIGH, the output bus is three-stated. When $\overline{R}$ is HIGH, the output bus is disabled irrespective of $\overline{OE}$.



NOTE:
1. Input bits are numbered 0 to n-1. D_7 and D_8 correspond to n=8 and n=9 respectively

Figure 1. Reset

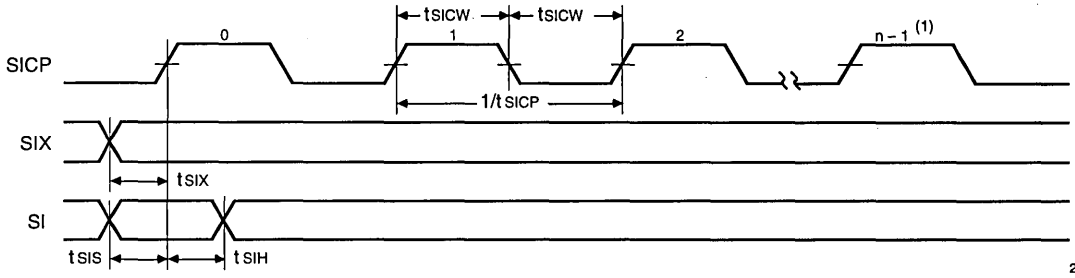


Figure 2. Write Operation

NOTE:
1. Input bits are numbered 0 to n-1.

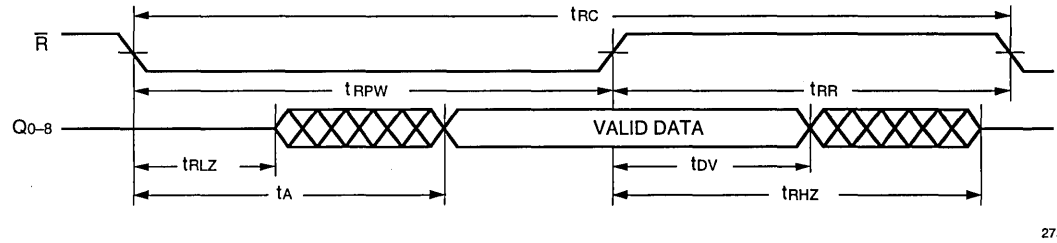


Figure 3. Read Operation

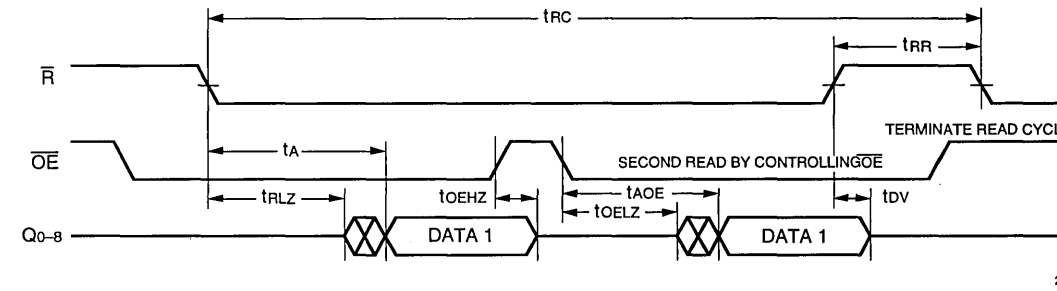
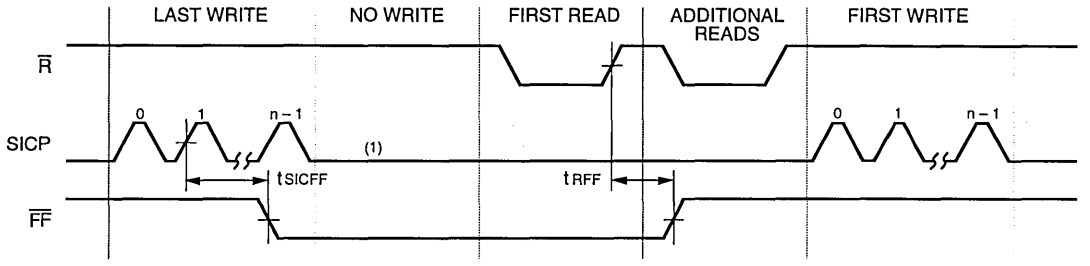


Figure 4. Output Enable Timings



NOTE:
1. After $\overline{FF}$ goes LOW and the last bit of the final word has been clocked in, SICP should not be clocked until $\overline{FF}$ goes HIGH.

Figure 5. Full Flag from Last Write to First Read

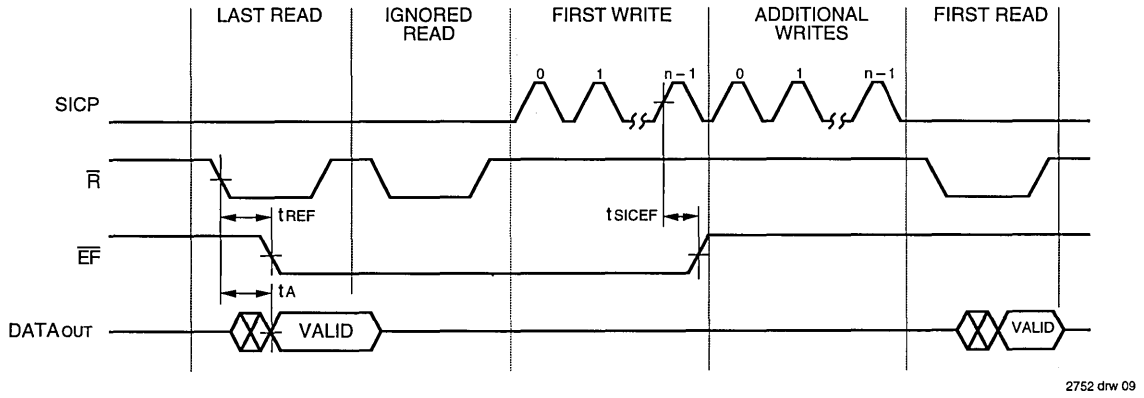


Figure 6. Empty Flag from Last Read to First Write

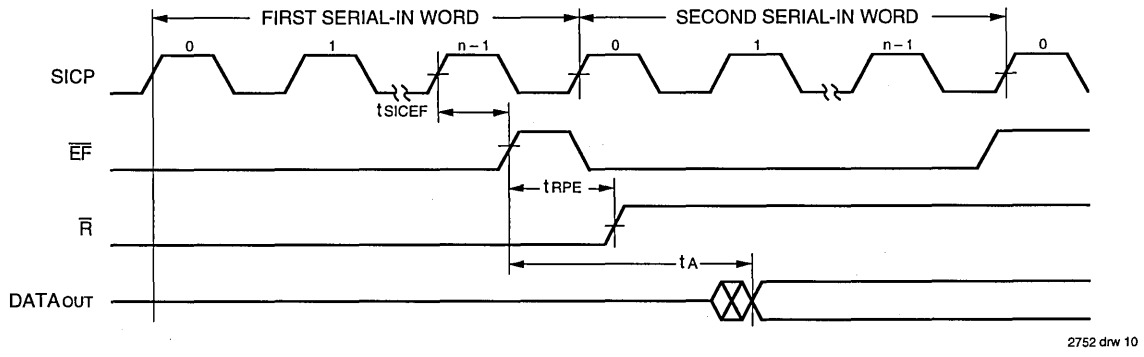
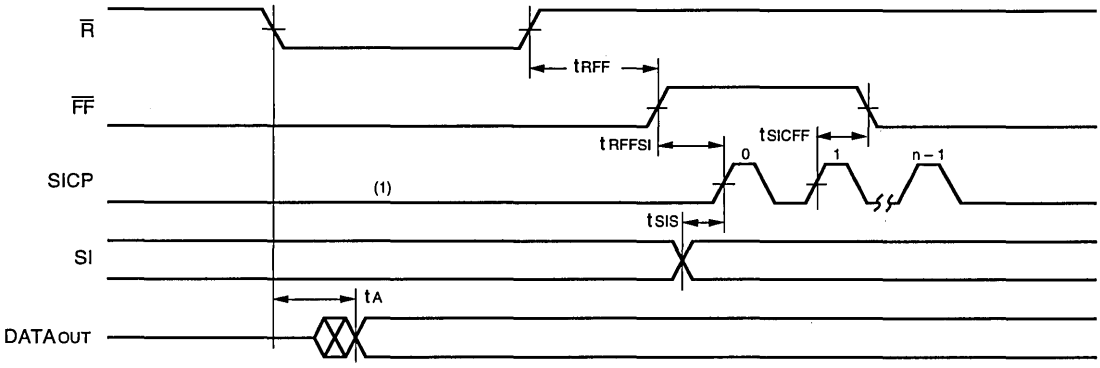


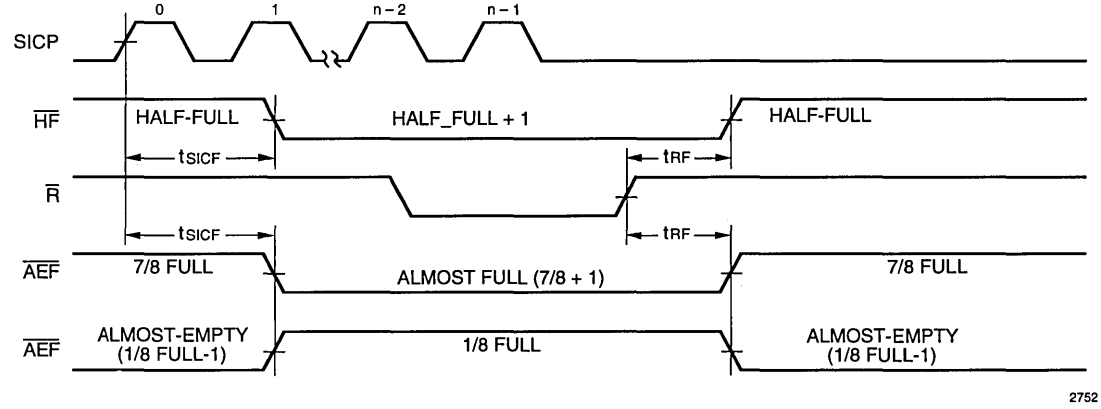
Figure 7. Empty Boundry Condition Timing



NOTE:
1. After $\overline{FF}$ goes LOW and the last bit of the final word has been clocked in, SICP should not be clocked until $\overline{FF}$ goes HIGH.

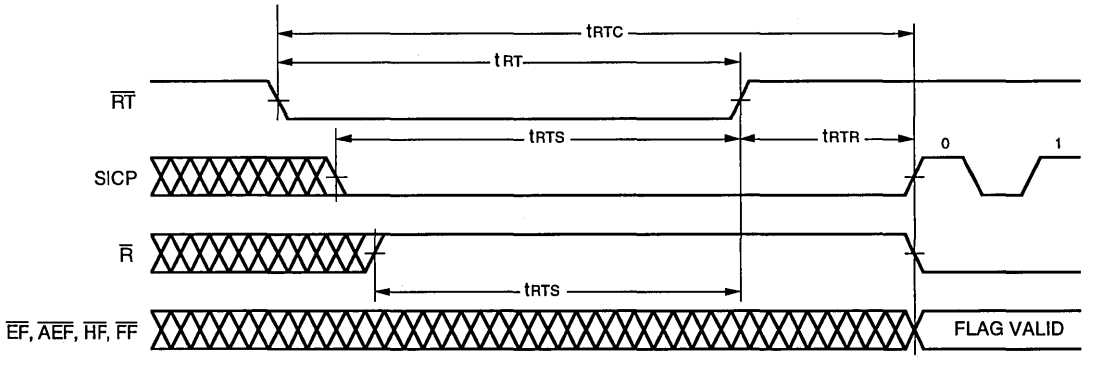
2752 drw 11

Figure 8. Full Boundry Condition Timing



2752 drw 12

Figure 9. Half Full, Almost Full and Almost Empty Timings



2752 drw 13

NOTE:
1. $\overline{EF}$, $\overline{AEF}$, $\overline{HF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at tRTC.

Figure 10. Retransmit

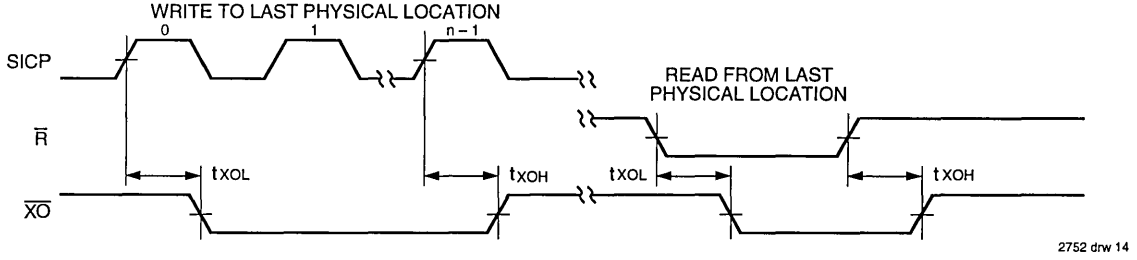


Figure 11. Expansion-Out

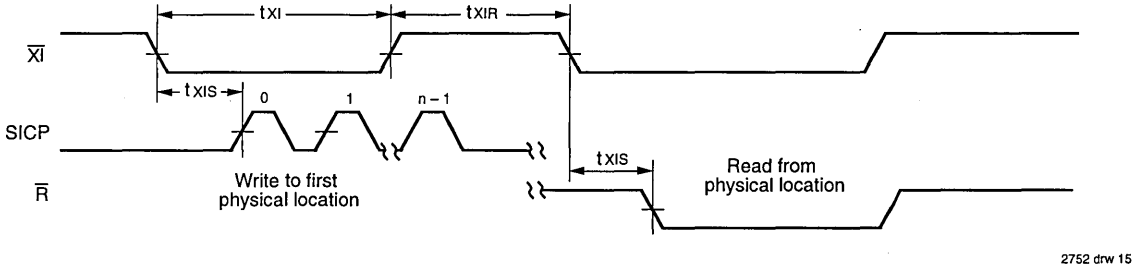


Figure 12. Expansion-In

5

OPERATING CONFIGURATIONS

Single Device Configuration

In the standalone case, the SIX line is tied HIGH and not used. On the first LOW-to-HIGH of the SICP clock, both of the Data Set lines (D_7, D_8) go LOW and a new serial word is started. The Data Set lines then go HIGH on the equivalent SICP clock pulse. This continues until the D line connected to $\overline{NW}$ goes HIGH completing the serial word. The cycle is then repeated with the next LOW-to-HIGH transition of SICP.

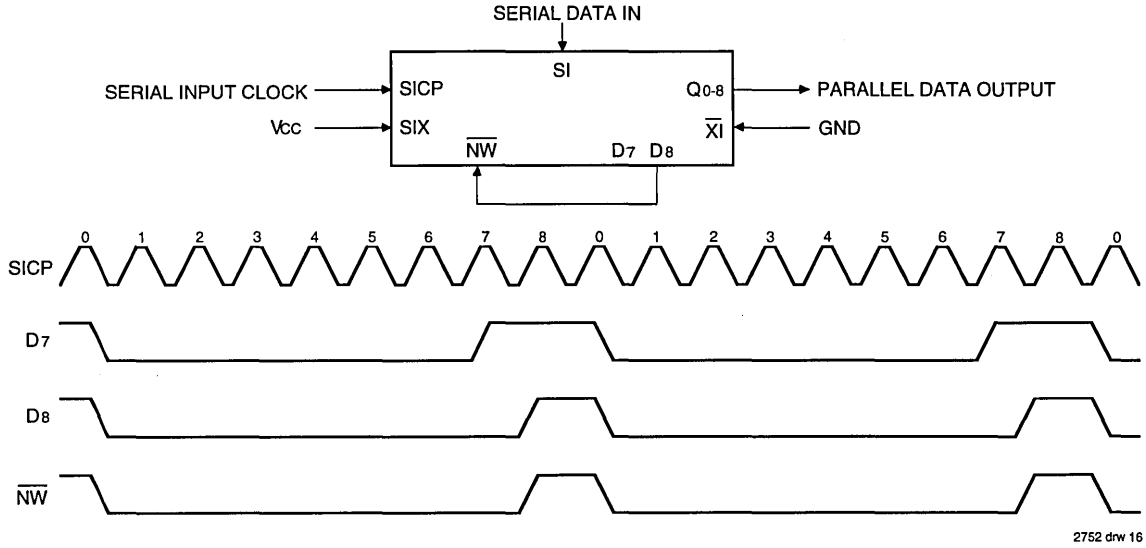


Figure 13. Nine-Bit Word Single Device Configuration

TRUTH TABLES
TABLE 1: RESET AND RETRANSMIT SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

2752 tbl 09

Width Expansion Configuration

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SIX line of the least significant device HIGH and the SIX of the subsequent devices to the appropriate Data Set lines of the previous devices, a cascaded serial word is achieved.

On the first LOW-to-HIGH clock edge of SICP, both the Data Set lines go LOW. Just as in the standalone case, on each corresponding clock cycle, the equivalent Data Set line goes HIGH in order of least to most significant.

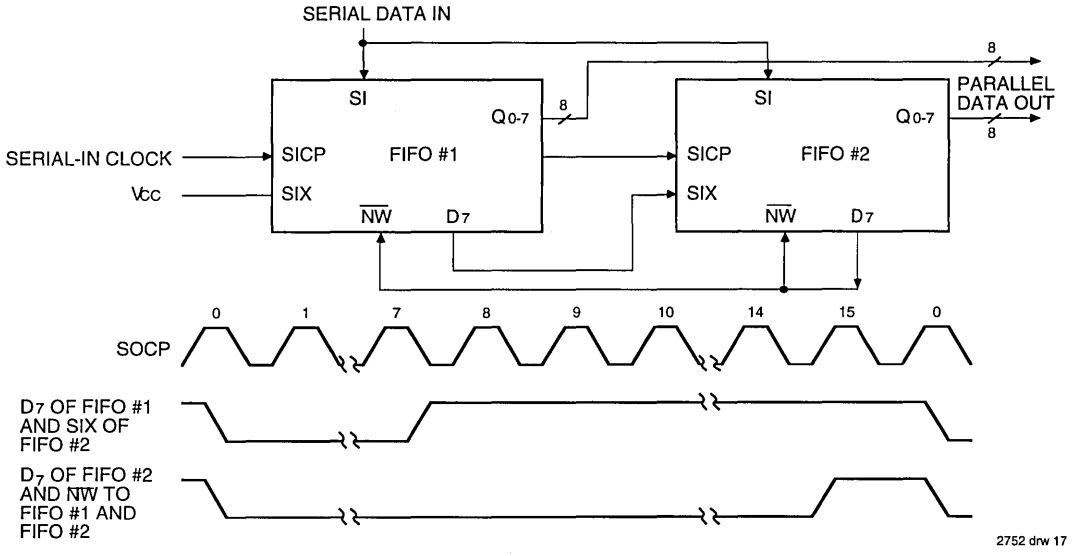


Figure 14. Serial-In to Parallel-Out Data of 16 Bits

Depth Expansion (Daisy Chain) Mode

The IDT72132/42 can be easily adapted to applications where the requirements are for greater than 2048/4096 words. Figure 15 demonstrates Depth Expansion using three IDT72132/42. Any depth can be attained by adding additional IDT72132/42 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin and Expansion In ($\overline{XI}$) pin of each device must be tied together.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite ($\overline{FF}$) or ($\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.

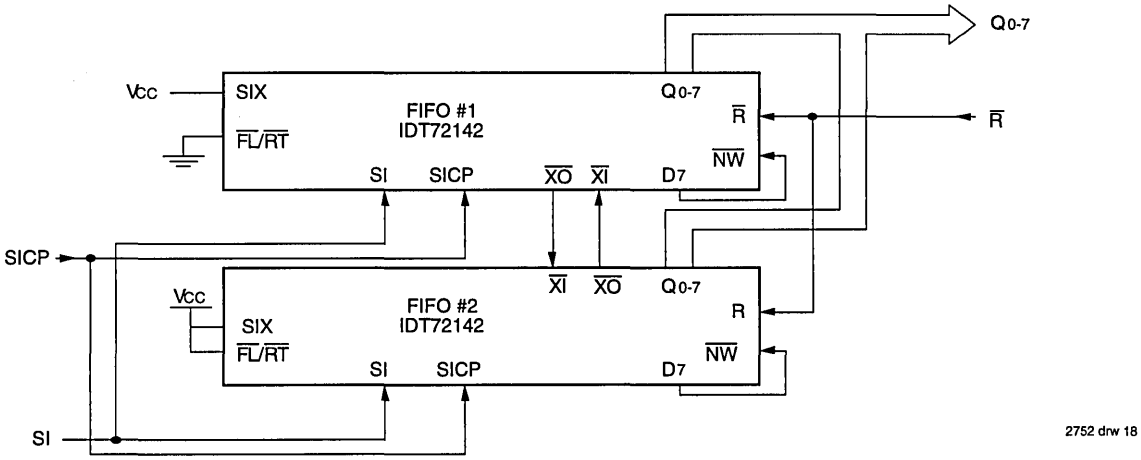


Figure 15. An 8K x 8 Serial-In Parallel-Out FIFO

TABLE 2: RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES: 2752 tbl 10

1. $\overline{XI}$ is connected to $\overline{XO}$ of the previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL/RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Ouput, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

SERIAL INPUT WITH WIDTH AND DEPTH EXPANSION

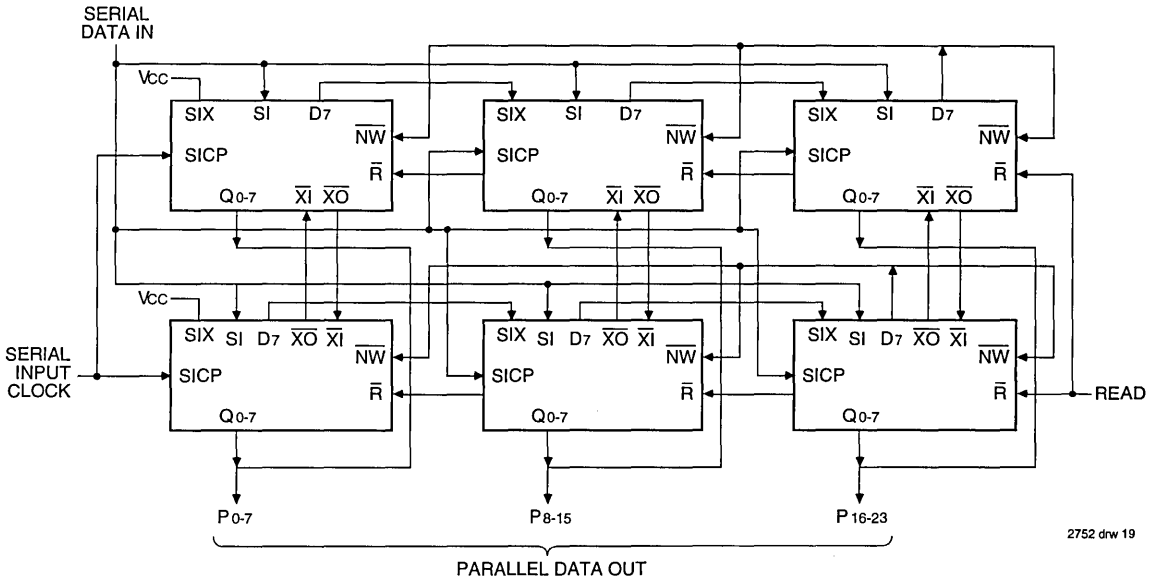
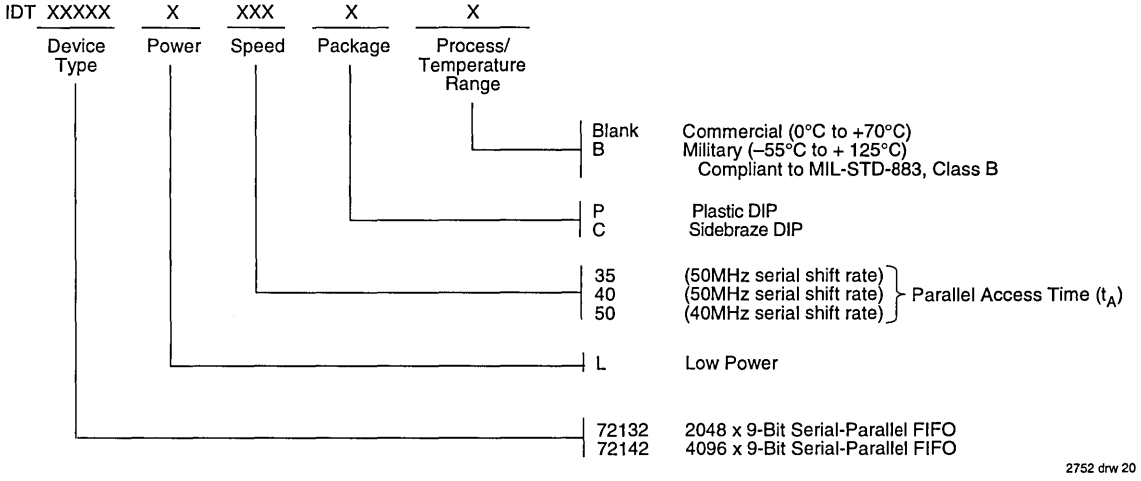


Figure 16. An 8K x 24 Serial-In, Parallel-Out FIFO Using Six IDT72142s

ORDERING INFORMATION



MULTI-PORT RAMS

Integrated Device Technology has emerged as the leading multi-port RAM supplier by combining CMOS/BiCMOS technology with innovative circuit design. With system performance advantages as a goal, we have brought system design expertise together with circuit and technology expertise in defining dual-port and four-port RAM products. Our dual-port memories are now industry standards. The synergistic relationship between advanced process technology, system expertise and unique design capability add value beyond that normally achieved. As an example, our dual-port memories provide arbitration along with a completely tested solution to the metastability problem. Various arbitration techniques are available to the designer to prevent contention and system wait states. On-chip hardware arbitration, "semaphore" token passing or software arbitration allow the most efficient memory to be selected for each application. At IDT, innovation counts only when it provides system advantages to the user.

IDT offers the largest selection of Multi-Port RAMS in the industry with offerings in x8, x9 and x16 configurations. We also offer a wide variety of packaging option with most product available in plastic DIP, Ceramic DIP, ceramic flat pack, PGA, PLCC, LCC as well as our latest innovation the space-saving TQFP(Thin Quad Flat Pack).

IDT has embarked on a mission to reduce the cost of a shared memory solutions We will accomplish this though the introduction of higher density products offered at a much lower cost per bit as well as continuing to cost reduce existing products by upgrading them to our latest technology. The combination of these will continue to drive down the cost of a "True Dual-Port" shared memory solution no matter what the size or configuration that is needed.

Both commercial and military versions of all IDT memories are available. Our military devices are manufactured and processed strictly in conformance with all the administrative processing and performance requirements of MIL-STD-883. Because we anticipated increased military radiation resistance requirements, all devices are also offered with special radiation resistant processing and guarantees. As the leading supplier of military specialty RAMs, IDT provides performance and quality levels second to none.

Our commercial dual-port and four-port memories, in fact, share most processing steps with military devices.

TABLE OF CONTENTS

SPECIALTY MEMORY PRODUCTS

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 8K (1K x 8-BIT)

IDT7130SA/LA
IDT7140SA/LA

FEATURES

- High-speed access
  - —Military: 25/35/55/100ns (max.)
  - —Commercial: 25/35/55/100ns (max.)
  - —Commercial: 20ns in PLCC only for 7130
- Low-power operation
  - —IDT7130/IDT7140SA
    - Active: 550mW (typ.)
    - Standby: 5mW (typ.)
  - —IDT7130/IDT7140LA
    - Active: 550mW (typ.)
    - Standby: 1mW (typ.)
- MASTER IDT7130 easily expands data bus width to 16-or-more-bits using SLAVE IDT7140
- On-chip port arbitration logic (IDT7130 Only)
- $\overline{BUSY}$ output flag on IDT7130; $\overline{BUSY}$ input on IDT7140
- $\overline{INT}$ flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention (LA only)
- TTL-compatible, single 5V ±10% power supply
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-86875
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION

The IDT7130/IDT7140 are high-speed 1K x 8 Dual-Port Static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7140 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

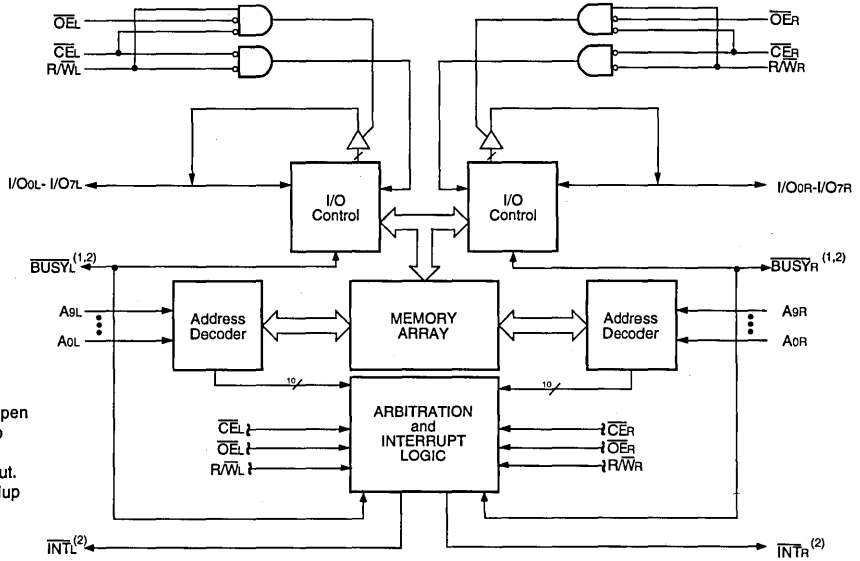
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 550mW of power. Low-power (LA) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200μW from a 2V battery.

The IDT7130/IDT7140 devices are packaged in 48-pin sidebraze or plastic DIPs, LCCs, or flatpacks, 52-pin PLCCs and 64-pin TQFPs. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

6

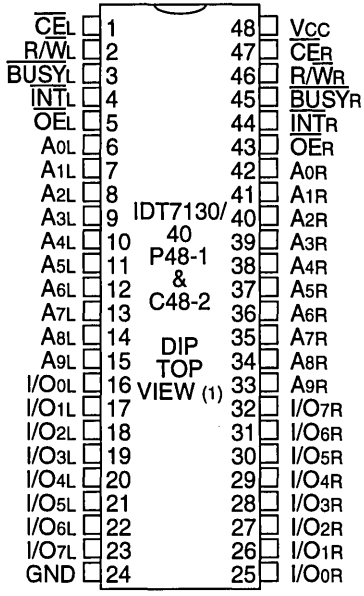
FUNCTIONAL BLOCK DIAGRAM

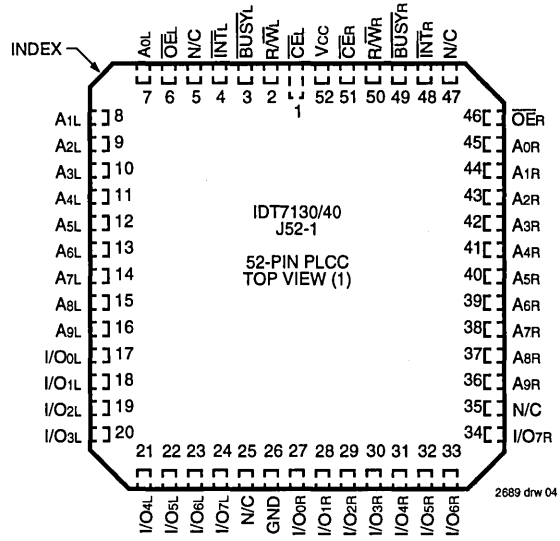


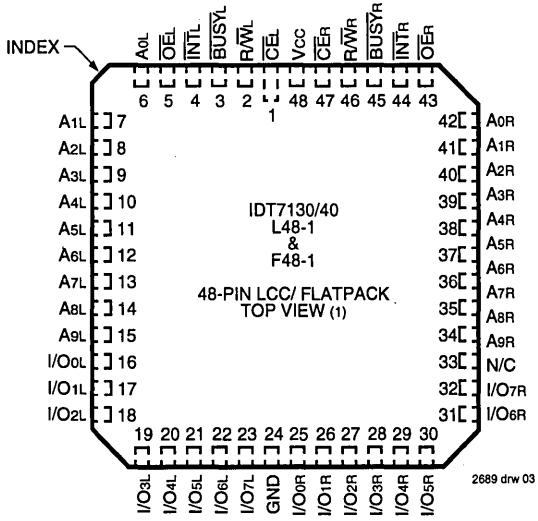
NOTES:
1. IDT7130 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7140 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

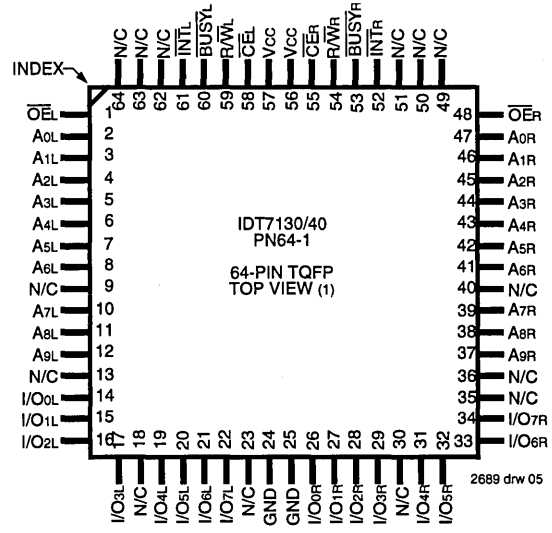
2689 drw 01

PIN CONFIGURATIONS









NOTE:
1. This text does not indicate orientation of the actual part-marking.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2689 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5 for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE:
1. V_{IL} (min.) ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

2689 tbl 02

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2689 tbl 03

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7130SA 7140SA Min.	7130SA 7140SA Max.	7130LA 7140LA Max.	7130LA 7140LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[1]	Vcc = 5.5V, VIN = 0V to Vcc	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current[1]	Vcc = 5.5V, $\overline{CE}$ = VIH, VOUT = 0V to Vcc	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O0-I/O7)	IOL = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$ $\overline{INT}$)	IOL = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	IOH = -4mA	2.4	—	2.4	—	V

NOTES:
1. At Vcc<2.0V leakages are undefined.

2689 tbl 04

CAPACITANCE (T_A = +25°C, f = 1.0MHz) TQFP Package Only

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	VIN = 3dV	9	pF
C_{OUT}	Output Capacitance	VIN = 3dV	10	pF

2689 tbl 05

NOTE:
1. This parameter is determined by device characterization but is not production tested.
2. 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version	7130X20[2] Typ.	7130X20[2] Max.	7130X25[3] 7140X25[3] Typ.	7130X25[3] 7140X25[3] Max.	7130X35 7140X35 Typ.	7130X35 7140X35 Max.	7130X55 7140X55 Typ.	7130X55 7140X55 Max.	7130X100 7140X100 Typ.	7130X100 7140X100 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs open, f = f_{MAX}[4]	MIL. SA	—	—	110	280	80	230	65	190	65	190	mA
			LA	—	—	110	220	80	170	65	140	65	140	
			COM'L. SA	110	250	110	220	80	165	65	155	65	155	
			LA	110	200	110	170	80	120	65	110	65	110	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH}, f = f_{MAX}[4]	MIL. SA	—	—	30	80	25	80	20	65	20	65	mA
			LA	—	—	30	60	25	60	20	45	20	45	
			COM'L. SA	30	65	30	65	25	65	20	65	20	55	
			LA	30	45	30	45	25	45	20	35	20	35	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{\cdot A\cdot}$ = V_{IL} and $\overline{CE}_{\cdot B\cdot}$ = V_{IH}[7] Active Port Outputs Open, f = f_{MAX}[4]	MIL. SA	—	—	65	160	50	150	40	125	40	125	mA
			LA	—	—	65	125	50	115	40	90	40	90	
			COM'L. SA	65	165	65	150	50	125	40	110	40	110	
			LA	65	125	65	115	50	90	40	75	40	75	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, f = 0[5]	MIL. SA	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
			LA	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
			COM'L. SA	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
			LA	0.2	5	0.2	5	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{\cdot A\cdot}$ ≤ 0.2V and $\overline{CE}_{\cdot B\cdot}$ ≥ V_{CC} -0.2V[7] V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[4]	MIL. SA	—	—	60	155	45	145	40	110	40	110	mA
			LA	—	—	60	115	45	105	40	85	40	80	
			COM'L. SA	60	155	60	145	45	110	40	100	40	95	
			LA	60	115	60	105	45	85	40	70	40	70	

NOTES:

2689 tbl 06

1. 'X' in part numbers indicates power rating (SA or LA).
2. Com'l Only, 0°C to +70°C temperature range. PLCC package only.
3. Not available in DIP packages..
4. At f = f_{Max}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. V_{CC} = 5V, T_A=+25°C for Typ and is not production tested. $V_{CC\,DC}$ = 100mA (Typ)
7. Port "A" may be either left or right port. Port "B" is opposite from port "A".

DATA RETENTION CHARACTERISTICS (LA Version Only)

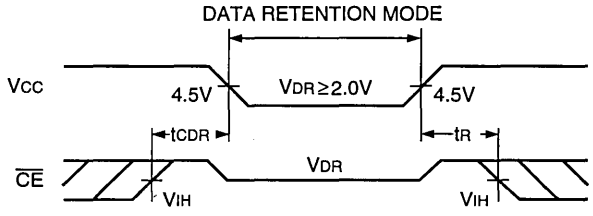
Symbol	Parameter	Test Conditions		IDT7130LA/IDT7140LA Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V, $\overline{CE}$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V		2.0	—	—	V
I_{CCDR}	Data Retention Current		Mil.	—	100	4000	µA
			Com'l.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:

2689 tbl 07

1. V_{CC} = 2V, T_A = +25°C, and is not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not production tested.

DATA RETENTION WAVEFORM



2692 drw 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

2689 tbl 08

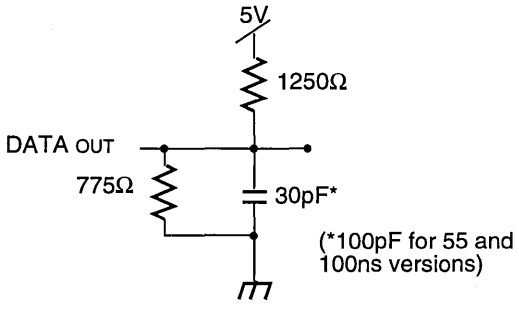


Figure 1. Output Test Load

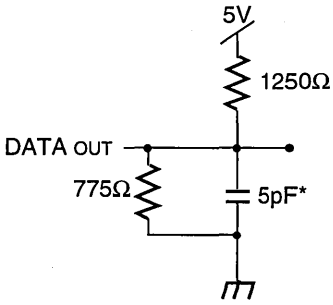
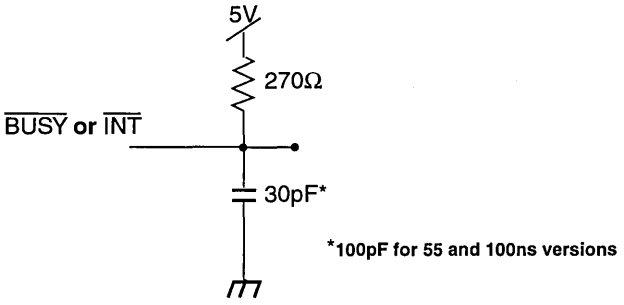


Figure 2. Output Test Load
(for tHZ, tLZ, twz, and tow)
*** including scope and jig**



2689 drw 07

Figure 3. BUSY and INT
AC Output Test Load

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3]

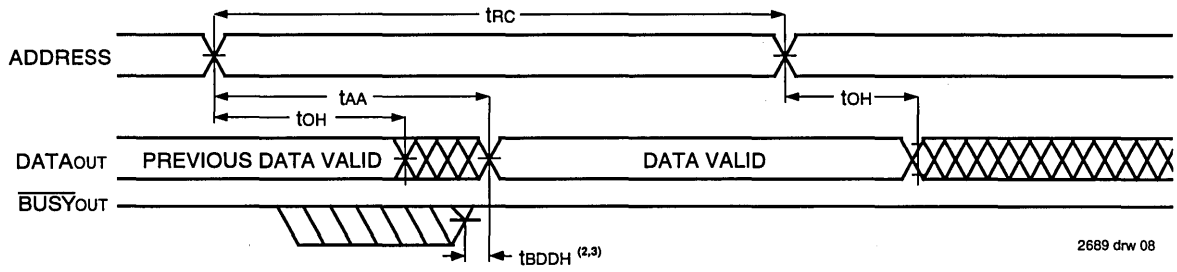
Symbol	Parameter	7130X20[2] Min.	7130X20[2] Max.	7130X25[5] 7140X25[5] Min.	7130X25[5] 7140X25[5] Max.	7130X35 7140X35 Min.	7130X35 7140X35 Max.	7130X55 7140X55 Min.	7130X55 7140X55 Max.	7130X100 7140X100 Min.	7130X100 7140X100 Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	35	—	55	—	100	—	ns
tAA	Address Access Time	—	20	—	25	—	35	—	55	—	100	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	—	55	—	100	ns
tAOE	Output Enable Access Time		11	—	12	—	20	—	25	—	40	ns
tOH	Output Hold From Address Change	3	—	3	—	3	—	3	—	10	—	ns
tLZ	Output Low-Z Time[1,4]	0	—	0	—	0	—	5	—	5	—	ns
tHZ	Output High-Z Time[1,4]	—	10	—	10	—	15	—	25	—	40	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	20	—	25	—	35	—	50	—	50	ns

NOTES:

2689 tbl 09

1. Transition is measured ±500mV from Low or High impedance voltage Output Test Load (Figure 2).
2. Com'l Only, 0°C to +70°C temperature range. PLCC package only.
3. "X" in part numbers indicates power rating (SA or LA).
4. This parameter is guaranteed by device characterization, but is not production tested.
5. Not available in DIP packages.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1]

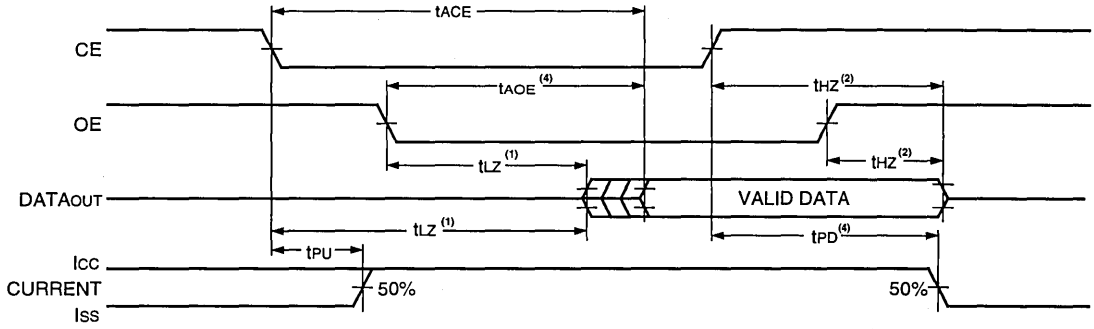


2689 drw 08

NOTES:

1. R/W = VIH, CE = VIL, and is OE = VIL. Address is valid prior to the coincidental with CE transition Low.
2. tBDD delay is required only in case where the opposite is port is completing a write operation to same the address location. For simultanious read operations BUSY has no relationship to valid output data.
3. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[3]



2689 drw 09

NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is deasserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = VIH, and the address is valid prior to other coincidental with $\overline{CE}$ transition Low.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

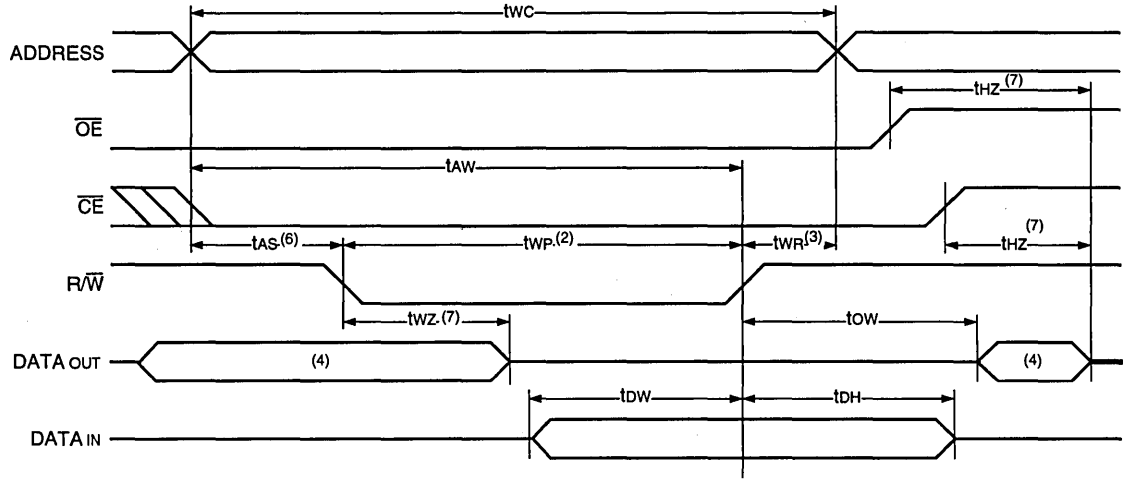
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	7130X20[2] Min.	7130X20[2] Max.	7130X25[6] 7140X25[6] Min.	7130X25[6] 7140X25[6] Max.	7130X35 7140X35 Min.	7130X35 7140X35 Max.	7130X55 7140X55 Min.	7130X55 7140X55 Max.	7130X100 7140X100 Min.	7130X100 7140X100 Max.	Unit
Write Cycle												
tWC	Write Cycle Time[3]	20	—	25	—	35	—	55	—	100	—	ns
tEW	Chip Enable to End-of-Write	15	—	20	—	30	—	40	—	90	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	30	—	40	—	90	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[4]	15	—	15	—	25	—	30	—	55	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	10	—	12	—	15	—	20	—	40	—	ns
tHZ	Output High-Z Time[1]	—	10	—	10	—	15	—	25	—	40	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High-Z[1]	—	10	—	10	—	15	—	25	—	40	ns
tOW	Output Active From End-of-Write[1]	0	—	0	—	0	—	0	—	0	—	ns

2689 tbl 10

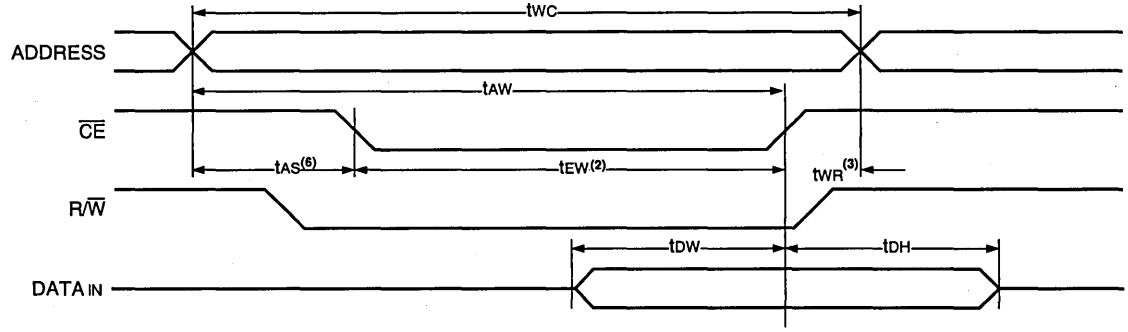
NOTES:
1. Transition is measured ±500mV from Low or High impedance voltage with Output Test Load (Figure 2). This parameter guaranteed device characterization but is not production tested.
2. 0°C to +70°C temperature range only, PLCC package only.
3. For MASTER/SLAVE combination, tWC = tBAA + tWP, since R/$\overline{W}$ = VIL must occur after tBAA.
4. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
5. "X" in part numbers indicates power rating (SA or LA).
6. Not available in DIP packages.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,5,8)



2689 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,5)



2689 drw 11

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be High during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of $\overline{CE}$ = VIL and R/$\overline{W}$ = VIL.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going High to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ Low transition occurs simultaneously with or after the R/$\overline{W}$ Low transition, the outputs remain in the High impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined be device characterization, but is not production tested. Transition is measured +/- 500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7]

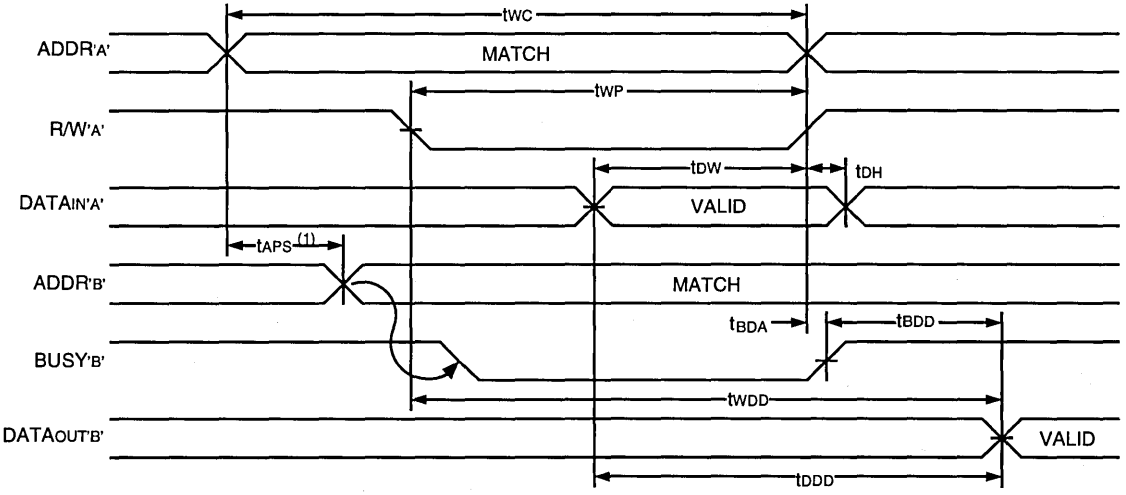
Symbol	Parameter	7130X20[1] Min.	7130X20[1] Max.	7130X25[9] 7140X25[9] Min.	7130X25[9] 7140X25[9] Max.	7130X35 7140X35 Min.	7130X35 7140X35 Max.	7130X55 7140X55 Min.	7130X55 7140X55 Max.	7130X100 7140X100 Min.	7130X100 7140X100 Max.	Unit
Busy Timing (For Master IDT7130 Only)												
tBAA	$\overline{BUSY}$ Access Time from Address	—	20	—	20	—	20	—	30	—	50	ns
tBDA	$\overline{BUSY}$ Disable Time from Address	—	20	—	20	—	20	—	30	—	50	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	20	—	20	—	30	—	50	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	20	—	20	—	30	—	50	ns
tWDD	Write Pulse to Data Delay[2]	—	50	—	50	—	60	—	80	—	120	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	35	—	35	—	35	—	55	—	100	ns
tAPS	Arbitration Priority Set-up Time[3]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[4]	—	20	—	25	—	35	—	55	—	100	ns
Busy Timing (For Slave IDT7140 Only)												
tWB	Write to $\overline{BUSY}$ Input[5]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	12	—	15	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay[2]	—	40	—	50	—	60	—	80	—	120	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	30	—	35	—	35	—	55	—	100	ns

NOTES: 2689 tbl 11

1. Com'l Only, 0°C to +70°C temperature range. PLCC package only.
2. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port -to-Port Read and $\overline{BUSY}$.
3. To ensure that the earlier of the two ports wins.
4. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
5. To ensure that a write cycle is inhibited on port 'B' during contention on port 'A'..
6. To ensure that a write cycle is completed on port 'B' after contention on port 'A'.
7. "X" in part numbers indicates power rating (S or L).
8. Not available in DIP package

6

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$[2,3,4]

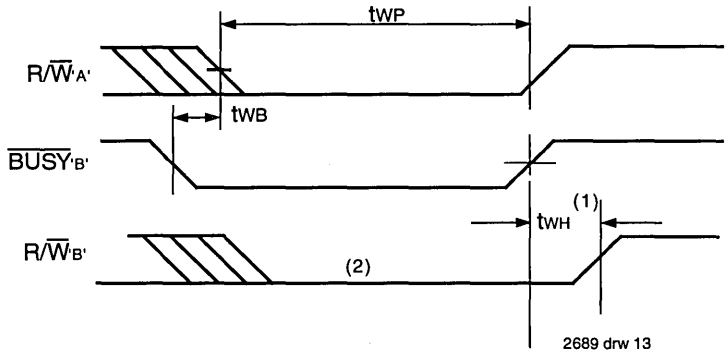


NOTES:

1. To ensure that the earlier of the two ports wins. tBDD is ignored for slave (IDT7140).
2. $\overline{CE_L}$ = $\overline{CE_R}$ = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is oppsite from port "A".

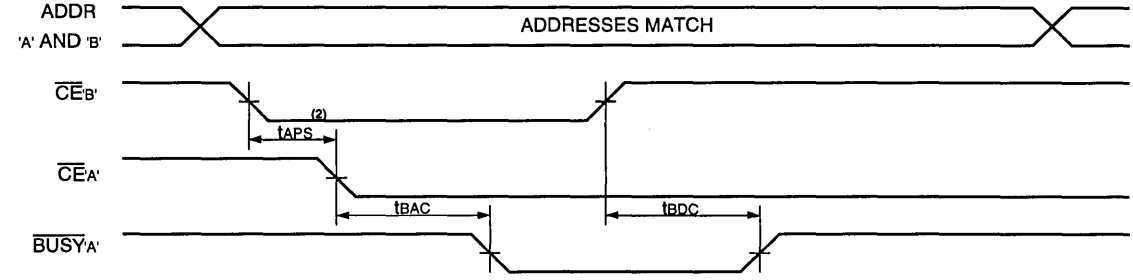
2689 drw 12

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$[3]

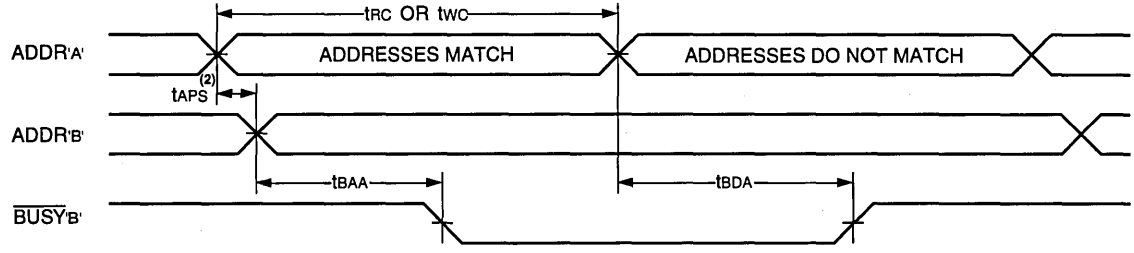


NOTES:
1. tBDD must be met for both BUSY Input (IDT7140, slave) or Output (IDT7130 master).
2. BUSY is asserted on port 'B' blocking R/W'B', until BUSY'B' goes High.
3. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is oppsite from port "A".

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING [1]



TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESS MATCH TIMING [1]



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If tAPS is not satisified, the BUSY will be asserted on one side or the other, but there is no guarantee on which side BUSY will be asserted (7130 only).

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[2]

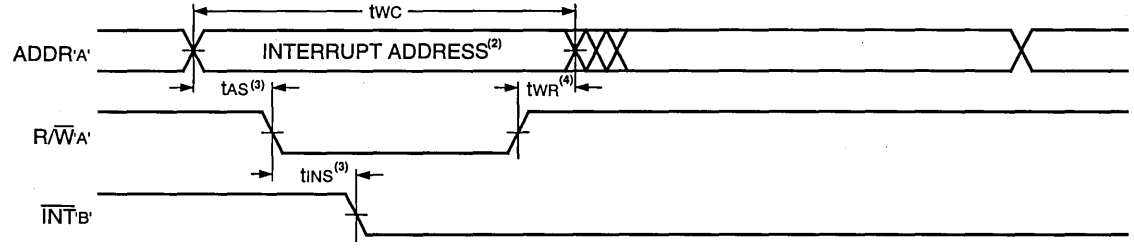
Symbol	Parameter	7130X20[1] Min.	7130X20[1] Max.	7130X25[3] 7140X25[3] Min.	7130X25[3] 7140X25[3] Max.	7130X35 7140X35 Min.	7130X35 7140X35 Max.	7130X55 7140X55 Min.	7130X55 7140X55 Max.	7130X100 7140X100 Min.	7130X100 7140X100 Max.	Unit
Interrupt Timing												
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	25	—	25	—	45	—	60	ns
tINR	Interrupt Reset Time	—	20	—	25	—	25	—	45	—	60	ns

2689 tbl 12

NOTES:
1. 0°C to +70°C temperature range only, PLCC package only.
2. "X" in part numbers indicates power rating (SA or LA).
3. Not available in DIP packages .

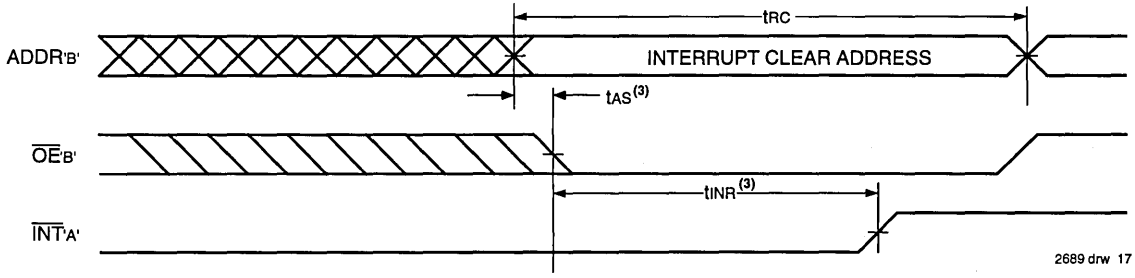
TIMING WAVEFORM OF INTERRUPT MODE

$\overline{INT}$ SET:



2689 drw 16

$\overline{INT}$ CLEAR:



2689 drw 17

NOTES:.
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. See Interrupt Truth Table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TABLE I. NON-CONTENTION READ/WRITE CONTROL[4]

Left or Right Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = V_{IH}$, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written Into Memory[2]
H	L	L	DATAOUT	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

NOTES: 2689 tbl 13

1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. 'H' = V_{IH}, 'L' = V_{IL}, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

TABLE II. INTERRUPT FLAG[1,4]

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{9L} - A_{0L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{9L} - A_{0R}$	$\overline{INT}_R$	Function
L	L	X	3FF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES: 2689 tbl 14

1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$
2. If $\overline{BUSY}_L = V_{IL}$, then No Change.
3. If $\overline{BUSY}_R = V_{IL}$, then No Change.
4. 'H' = HIGH,' L' = LOW,' X' = DON'T CARE

TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{9L} A_{0R}-A_{9R}	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

NOTES: 2689 tbl 15

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs for IDT7130 (master). Both are inputs for IDT7140 (slave). $\overline{BUSY}x$ outputs on the IDT7130 are open drain, not push-pull outputs. On slaves the $\overline{BUSY}x$ input internally inhibits writes.
2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving Low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving Low regardless of actual logic level on the pin.

FUNCTIONAL DESCRIPTION

The IDT7130/IDT7140 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7130/IDT7140 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = V_{IH}). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 3FE (HEX), where a write is defined as the $\overline{CE}$ = R/$\overline{W}$ = V_{IL} per the Truth Table. The left port clears the interrupt by access address location FFE access when $\overline{CE}_R$ = $\overline{OE}_R$ = V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must access the memory location 3FF. The message (8 bits) at 3FE or 3FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FE and 3FF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The Busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. In slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins High. If desired, unintended write operations can be prevented to a port by tying the Busy pin for that port Low.

The Busy outputs on the IDT7130 RAM (Master) are open drain type outputs and require open drain resistors to operate. If these RAMs are being expanded in depth, then the Busy indication for the resulting array does not require the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7130/IDT7140 RAMs the Busy pin is an output if the part is Master (IDT7031), and the Busy pin is an input if the part is a Slave (IDT7140) as shown in Figure 3.

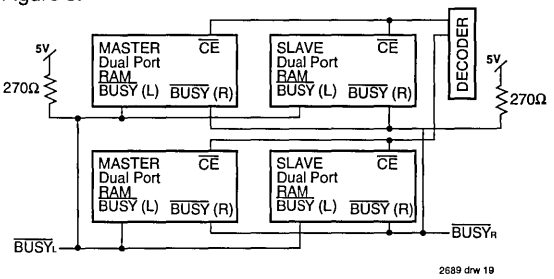


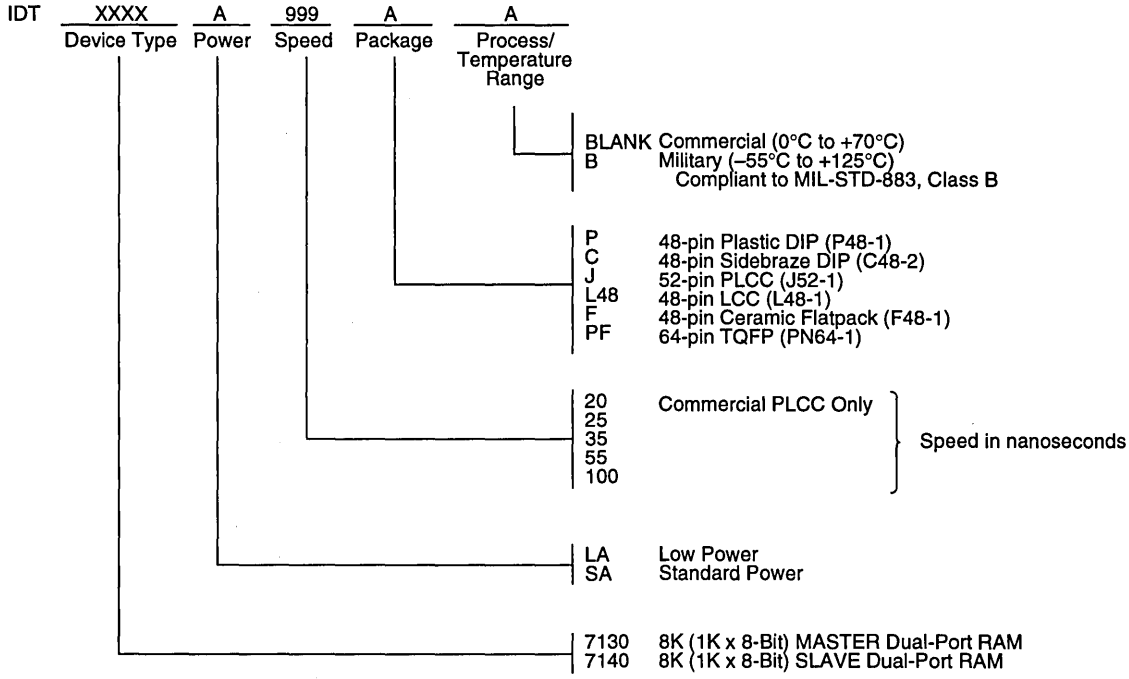
Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7030 (Master) and IDT7140 (Slave)RAMs.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The Busy arbitration, on a Master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

6

ORDERING INFORMATION



2689 drw 19

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT)

IDT7132SA/LA
IDT7142SA/LA

FEATURES:

- High-speed access
  - — Military: 25/35/55/100ns (max.)
  - — Commercial: 25/35/55/100ns (max.)
  - — Commercial: 20ns only in PLCC for 7132
- Low-power operation
  - — IDT7132/42SA
    Active: 550mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7132/42LA
    Active: 550mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- MASTER IDT7132 easily expands data bus width to 16-or-more bits using SLAVE IDT7142
- On-chip port arbitration logic (IDT7132 only)
- $\overline{BUSY}$ output flag on IDT7132; $\overline{BUSY}$ input on IDT7142
- Battery backup operation —2V data retention
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD, Class B
- Standard Military Drawing # 5962-87002
- Industrial temperature range (–40°C to +85°C) is available, tested to miliary electrical specifications

DESCRIPTION:

The IDT7132/IDT7142 are high-speed 2K x 8 Dual-Port Static RAMs. The IDT7132 is designed to be used as a stand-alone 8-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7142 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

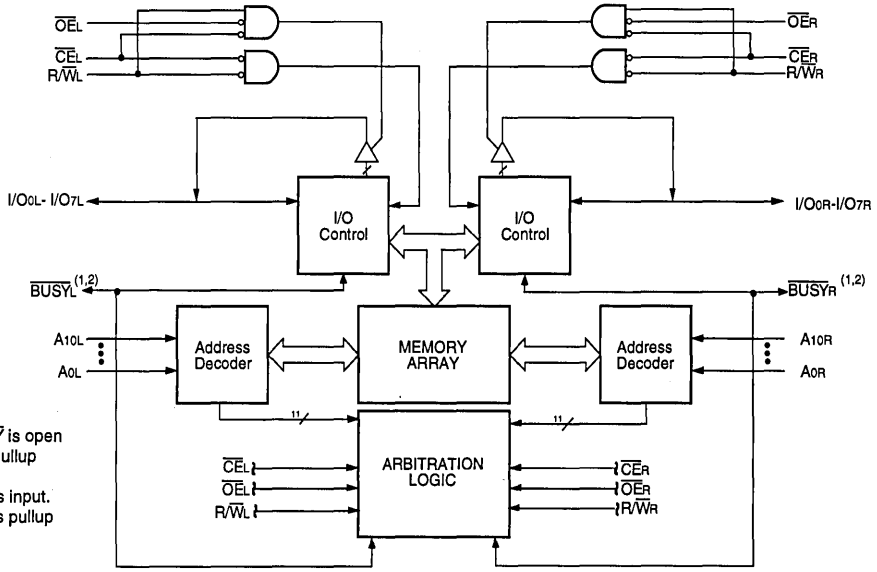
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 550mW of power. Low-power (LA) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

The IDT7132/7142 devices are packaged in a 48-pin sidebraze or plastic DIPs, 48-pin LCCs, 52-pin PLCCs, and 48-lead flatpacks. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

6

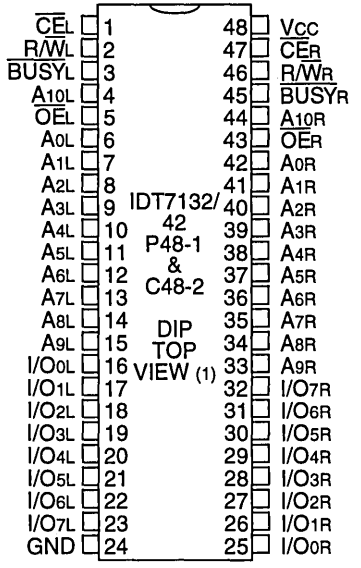
FUNCTIONAL BLOCK DIAGRAM



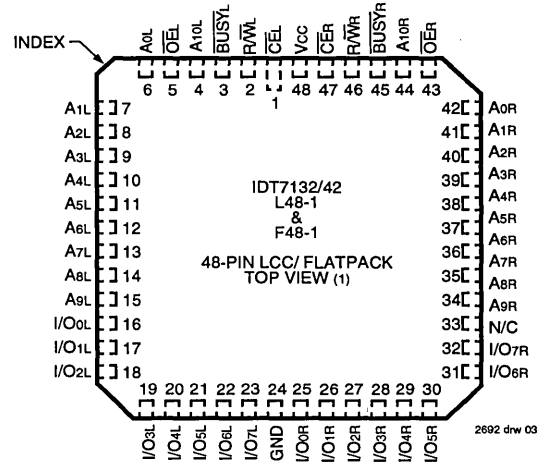
NOTES:
1. IDT7132 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor.
   IDT7142 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

2692 drw 01

PIN CONFIGUARATIONS



2692 drw 02



2692 drw 03

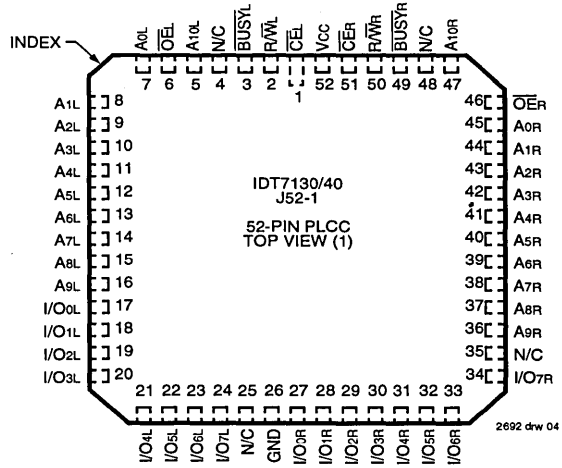
NOTE:
1. This text does not indicate orientation of the actual part-marking.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2692 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.



2692 drw 04

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2692 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0(2)	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

2692 tbl 03

NOTE:
1. VIL (min.) = -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version	7132X20[2] Typ.	7132X20[2] Max.	7132X25[3] 7142X25[3] Typ.	7132X25[3] 7142X25[3] Max.	7132X35 7142X35 Typ.	7132X35 7142X35 Max.	7132X55 7142X55 Typ.	7132X55 7142X55 Max.	7132X100 7142X100 Typ.	7132X100 7142X100 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs open, f = f_{MAX}[4]	MIL. SA	—	—	110	280	80	230	65	190	65	190	mA
			LA	—	—	110	220	80	170	65	140	65	140	
			COM'L. SA	110	250	110	220	80	165	65	155	65	155	
			LA	110	200	110	170	80	120	65	110	65	110	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH}, f = f_{MAX}[4]	MIL. SA	—	—	30	80	25	80	20	65	20	65	mA
			LA	—	—	30	60	25	60	20	45	20	45	
			COM'L. SA	30	65	30	65	25	65	20	65	20	55	
			LA	30	45	30	45	25	45	20	35	20	35	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{*A}$ = V_{IL} and $\overline{CE}_{*B}$ = V_{IH}[7] Active Port Outputs Open, f = f_{MAX}[4]	MIL. SA	—	—	65	160	50	150	40	125	40	125	mA
			LA	—	—	65	125	50	115	40	90	40	90	
			COM'L. SA	65	165	65	150	50	125	40	110	40	110	
			LA	65	125	65	115	50	90	40	75	40	75	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$, f = 0[5]	MIL. SA	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
			LA	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
			COM'L. SA	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
			LA	0.2	5	0.2	5	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{*A} \leq 0.2V$ and $\overline{CE}_{*B} \geq V_{CC}$ -0.2V[7] $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq 0.2V$, Active Port Outputs Open, f = f_{MAX}[4]	MIL. SA	—	—	60	155	45	145	40	110	40	110	mA
			LA	—	—	60	115	45	105	40	85	40	80	
			COM'L. SA	60	155	60	145	45	110	40	100	40	95	
			LA	60	115	60	105	45	85	40	70	40	70	

NOTES:

2689 tbl 04

1. 'X' in part numbers indicates power rating (SA or LA).
2. Com'l Only, 0°C to +70°C temperature range. PLCC package only.
3. Not available in DIP packages..
4. At f = f_{Max}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. V_{CC} = 5V, T_A=+25°C for Typ and is not production tested. $V_{CC\,DC}$ = 100mA (Typ)
7. Port "A" may be either left or right port. Port "B" is opposite from port "A".

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7132SA 7142SA Min.	7132SA 7142SA Max.	7132LA 7142LA Max.	7132LA 7142LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current[1]	V_{CC} = 5.5V, $\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O0-I/O7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$ $\overline{INT}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

NOTES:

2689 tbl 05

1. At Vcc<2.0V leakages are undefined.

6

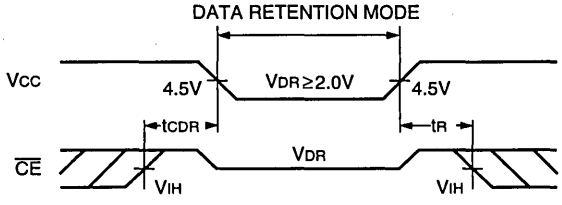
DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Conditions		IDT7132LA/IDT7142LA Min.	Typ.	Max.	Unit
V_{DR}	Vcc for Data Retention			2.0	—	—	V
I_{CCDR}	Data Retention Current	Vcc = 2.0V, $\overline{CE} \geq$ Vcc -0.2V	Mil.	—	100	4000	µA
		$V_{IN} \geq$ Vcc -0.2V or $V_{IN} \leq$ 0.2V	Com'l.	—	100	1500	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

NOTES:
1. Vcc = 2V, TA = +25°C, and is not production tested.
2. tRC = Read Cycle Time
3. This parameter is guaranteed but not production tested.

2692 tbl 06

DATA RETENTION WAVEFORM



2692 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND TO 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, & 3

2692 tbl 07

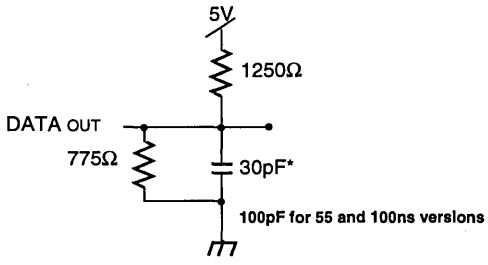


Figure 1. Output Test

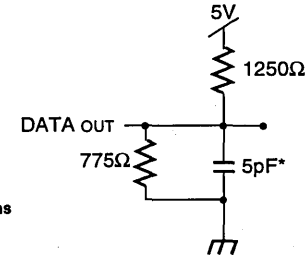


Figure 2. Output Test Load (for tHZ, tLZ, twz, and tow)
* Including scope and jig

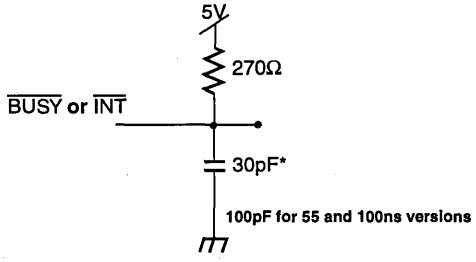


Figure 3. $\overline{Busy}$ AC Output TestLoad (IDT7132 only)

2692 drw 06

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3]

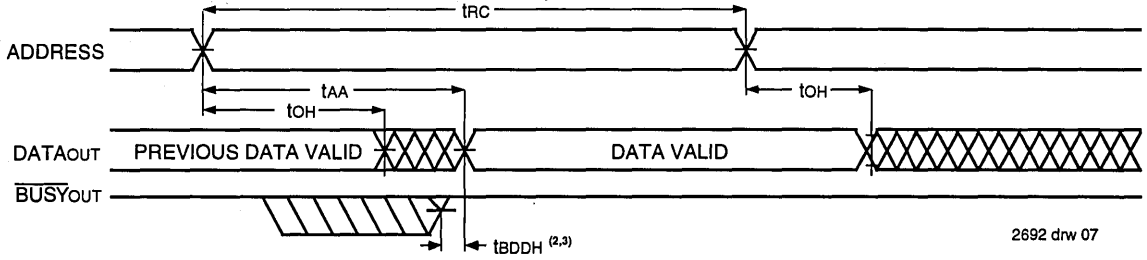
Symbol	Parameter	7132X20[2] Min.	7132X20[2] Max.	7132X25[5] 7142X25[5] Min.	7132X25[5] 7142X25[5] Max.	7132X35 7142X35 Min.	7132X35 7142X35 Max.	7132X55 7142X55 Min.	7132X55 7142X55 Max.	7132X100 7142X100 Min.	7132X100 7142X100 Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	35	—	55	—	100	—	ns
tAA	Address Access Time	—	20	—	25	—	35	—	55	—	100	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	—	55	—	100	ns
tAOE	Output Enable Access Time		11	—	12	—	20	—	25	—	40	ns
tOH	Output Hold From Address Change	3	—	3	—	3	—	3	—	10	—	ns
tLZ	Output Low-Z Time[1,4]	0	—	0	—	0	—	5	—	5	—	ns
tHZ	Output High-Z Time[1,4]	—	10	—	10	—	15	—	25	—	40	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	20	—	25	—	35	—	50	—	50	ns

NOTES:

2689 tbl 08

1. Transition is measured ±500mV from Low or High impedance voltage Output Test Load (Figure 2).
2. Com'l Only, 0°C to +70°C temperature range. PLCC package only.
3. "X" in part numbers indicates power rating (SA or LA).
4. This parameter is guaranteed by device characterization, but is not production tested.
5. Not available in DIP packages.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1]

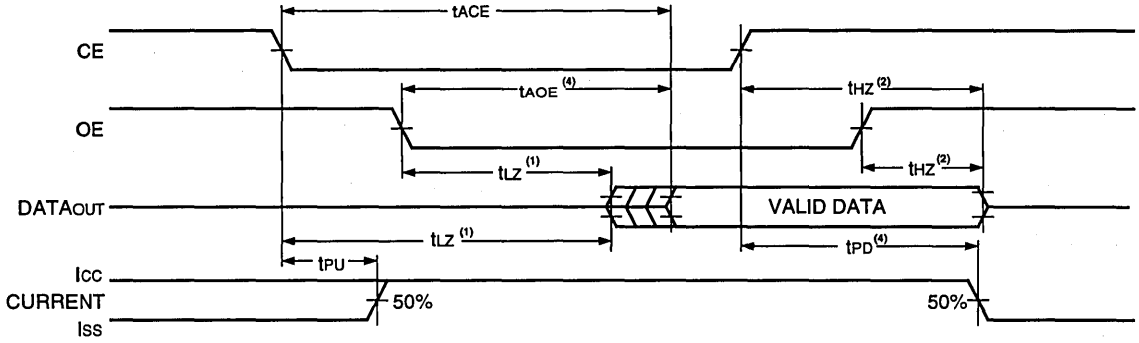


2692 drw 07

NOTES:

1. R/$\overline{W}$ = VIH, $\overline{CE}$ = VIL, and is $\overline{OE}$ = VIL. Address is valid prior to the coincidental with $\overline{CE}$ transition Low.
2. tBDD delay is required only in case where the opposite is port is completing a write operation to same the address location. For simultanious read operations $\overline{BUSY}$ has no relationship to valid output data.
3. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE [1,3]



2692 drw 08

NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is deasserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = VIH, and the address is valid prior to other coincidental with $\overline{CE}$ transition Low.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[5]

Symbol	Parameter	7132X20[2] Min.	7132X20[2] Max.	7132X25[6] 7142X25[6] Min.	7132X25[6] 7142X25[6] Max.	7132X35 7142X35 Min.	7132X35 7142X35 Max.	7132X55 7142X55 Min.	7132X55 7142X55 Max.	7132X100 7142X100 Min.	7132X100 7142X100 Max.	Unit
Write Cycle												
tWC	Write Cycle Time[3]	20	—	25	—	35	—	55	—	100	—	ns
tEW	Chip Enable to End of Write	15	—	20	—	30	—	40	—	90	—	ns
tAW	Address Valid to End of Write	15	—	20	—	30	—	40	—	90	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width[4]	15	—	15	—	25	—	30	—	55	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12	—	15	—	20	—	40	—	ns
tHZ	Output High Z Time[1]	—	10	—	10	—	15	—	25	—	40	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z[1]	—	10	—	10	—	15	—	30	—	40	ns
tOW	Output Active From End of Write[1]	0	—	0	—	0	—	0	—	0	—	ns

NOTES:

2692 tbl 09

1. Transition is measured ±500mV from Low or High impedance voltage with Output Test Load (Figure 2). This parameter guaranteed device characterization but is not production tested.
2. 0°C to +70°C temperature range only, PLCC package only.
3. For Master/Slave combination, tWC = tBAA + tWP, since R/$\overline{W}$ = VIL must occur after tBAA.
4. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
5. "X" in part numbers indicates power rating (SA or LA).
6. Not available in DIP packages.

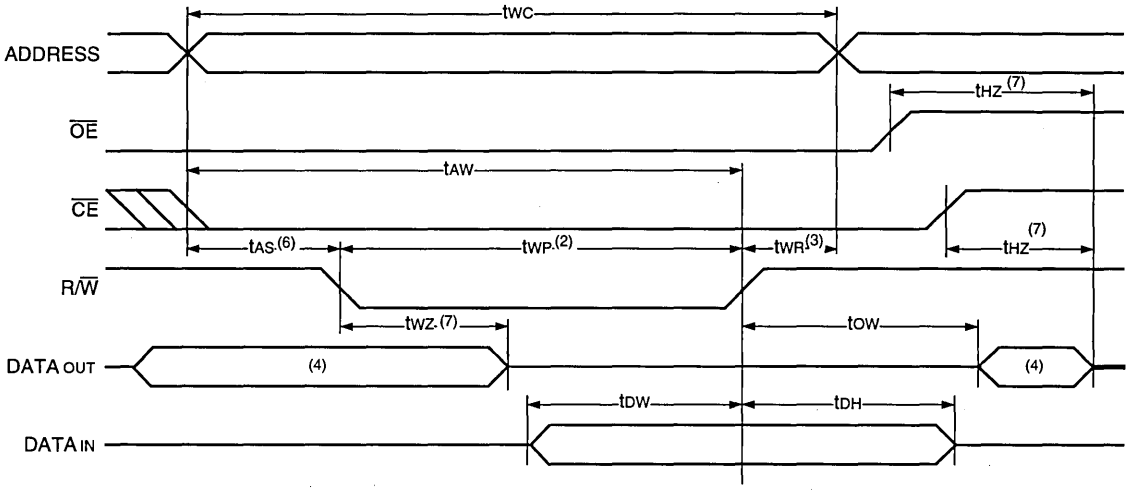
CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter [1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	11	pF
COUT	Output Capacitance	VIN = 0V	11	pF

2692 tbl 10

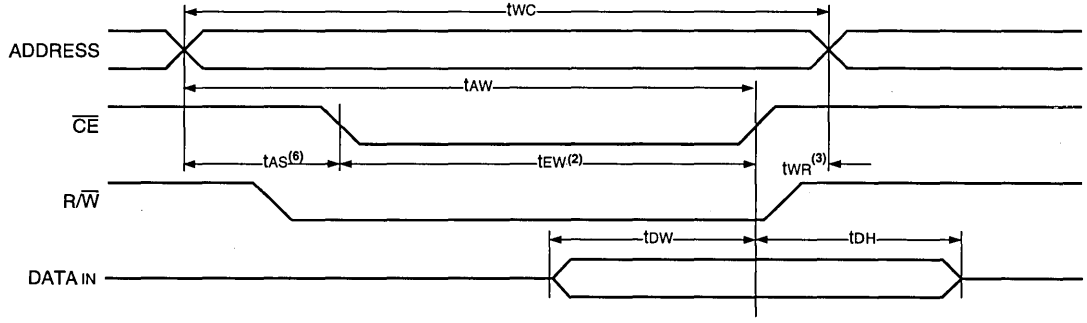
NOTE:
1. This parameter is sampled and not 100% tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,5,8))



2692 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,5)



2692 drw 11

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be High during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of $\overline{CE}$ = VIL and R/$\overline{W}$= VIL.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going High to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ Low transition occurs simultaneously with or after the R/$\overline{W}$ Low transition, the outputs remain in the High impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined be device characterization, but is not production tested. Transition is measured +/- 500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7]

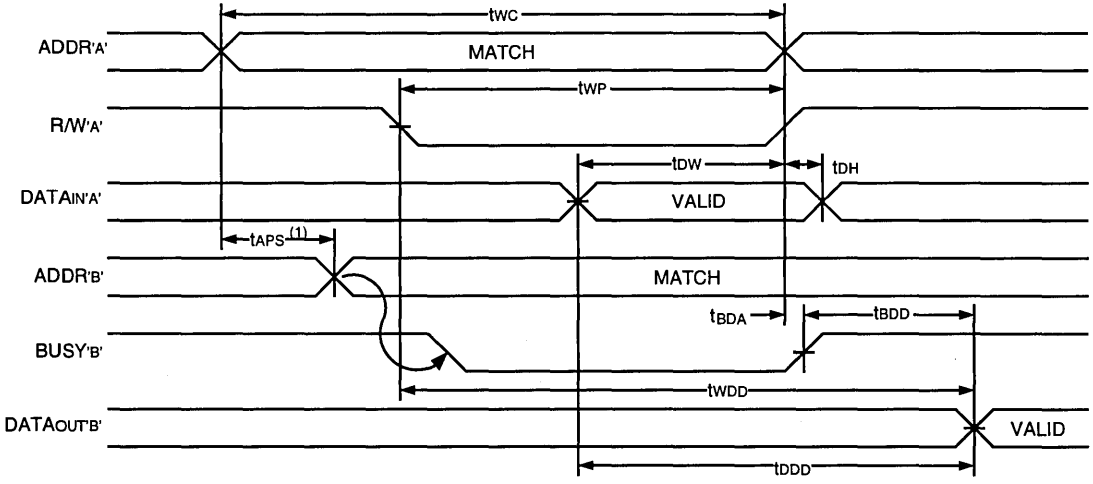
Symbol	Parameter	7132X20[1] Min.	7132X20[1] Max.	7132X25[9] 7142X25[9] Min.	7132X25[9] 7142X25[9] Max.	7132X35 7142X35 Min.	7132X35 7142X35 Max.	7132X55 7142X55 Min.	7132X55 7142X55 Max.	7132X100 7142X100 Min.	7132X100 7142X100 Max.	Unit
Busy Timing (For Master IDT7130 Only)												
tBAA	$\overline{BUSY}$ Access Time from Address	—	20	—	20	—	20	—	30	—	50	ns
tBDA	$\overline{BUSY}$ Disable Time from Address	—	20	—	20	—	20	—	30	—	50	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	20	—	20	—	30	—	50	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	20	—	20	—	30	—	50	ns
tWDD	Write Pulse to Data Delay[2]	—	50	—	50	—	60	—	80	—	120	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	35	—	35	—	35	—	55	—	100	ns
tAPS	Arbitration Priority Set-up Time[3]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[4]	—	20	—	25	—	35	—	55	—	100	ns
Busy Timing (For Slave IDT7140 Only)												
tWB	Write to $\overline{BUSY}$ Input[5]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	12	—	15	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay[2]	—	40	—	50	—	60	—	80	—	120	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	30	—	35	—	35	—	55	—	100	ns

NOTES:

2689 tbl 11

1.Com'l Only, 0°C to +70°C temperature range. PLCC package only.
2. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port -to-Port Read and $\overline{BUSY}$.
3. To ensure that the earlier of the two ports wins.
4. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
5. To ensure that a write cycle is inhibited on port 'B' during contention on port 'A'..
6. To ensure that a write cycle is completed on port 'B' after contention on port 'A'.
7. "X" in part numbers indicates power rating (S or L).
8. Not available in DIP package

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$ (1,2,3,6)

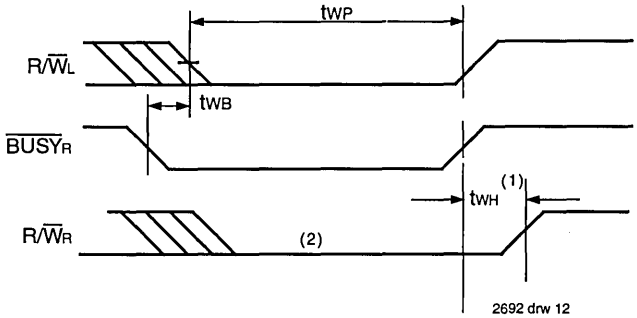


2692 drw 12

NOTES:

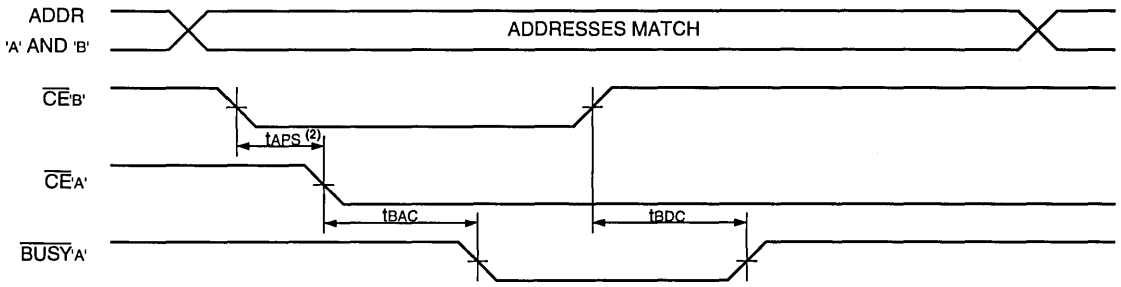
1. To ensure that the earlier of the two ports wins. tAPS is ignored for Slave (IDT7142).
2. $\overline{CE_L}$ = $\overline{CE_R}$ = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is opposite from port "A".

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$[3]

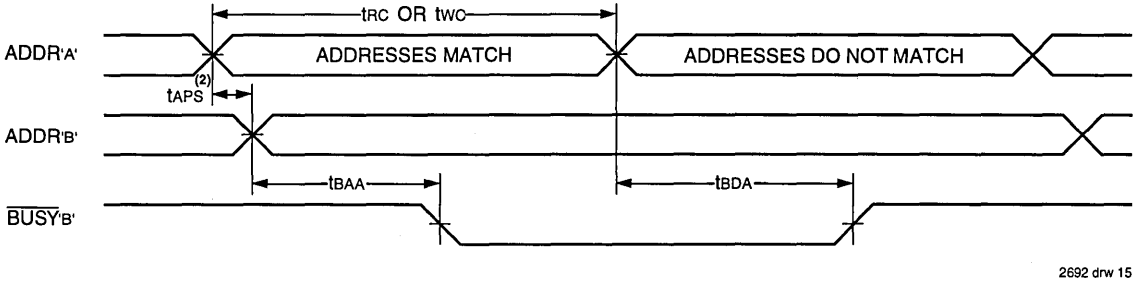


NOTES:
1. tBDD must be met for both BUSY Input (IDT7140, slave) or Output (IDT7130 master).
2. BUSY is asserted on port 'B' blocking R/W'B', until BUSY'B' goes High.
3. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is oppsite from port "A".

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING [1]



TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESS MATCH TIMING [1]



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If tAPS is not satisified, the BUSY will be asserted on one side or the other, but there is no guarantee on which side BUSY will be asserted (7032 only).

TRUTH TABLES

TABLE I. NON-CONTENTION READ/WRITE CONTROL[4]

Left or Right Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D0-7	Function
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = V_{IH}$, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written Into Memory[2]
H	L	L	DATAOUT	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

2654 tbl 12

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. 'H' = V_{IH}, 'L' = V_{IL}, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

TABLE II. INTERRUPT FLAG[1,4]

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{10L} - A_{0L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{10L} - A_{0R}$	$\overline{INT}_R$	Function
L	L	X	7FF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2654 tbl 13

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$
2. If $\overline{BUSY}_L = V_{IL}$, then No Change.
3. If $\overline{BUSY}_R = V_{IL}$, then No Change.
4. 'H' = HIGH,' L' = LOW,' X' = DON'T CARE

TABLE III — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{10L} A_{0R}-A_{10R}	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

2654 tbl 13

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs for IDT7130 (master). Both are inputs for IDT7140 (slave). $\overline{BUSY}x$ outputs on the IDT7130 are open drain, not push-pull outputs. On slaves the $\overline{BUSY}x$ input internally inhibits writes.
2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If tAPS is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving Low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving Low regardless of actual logic level on the pin.

FUNCTIONAL DESCRIPTION

The IDT7132/IDT7142 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7132/IDT7142 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = VIL). When a port is enabled, access to the entire memory array is permitted.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT7132/IDT7142 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7130/IDT7140 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

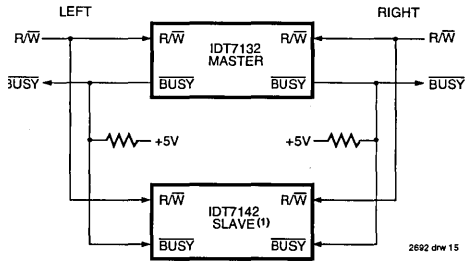
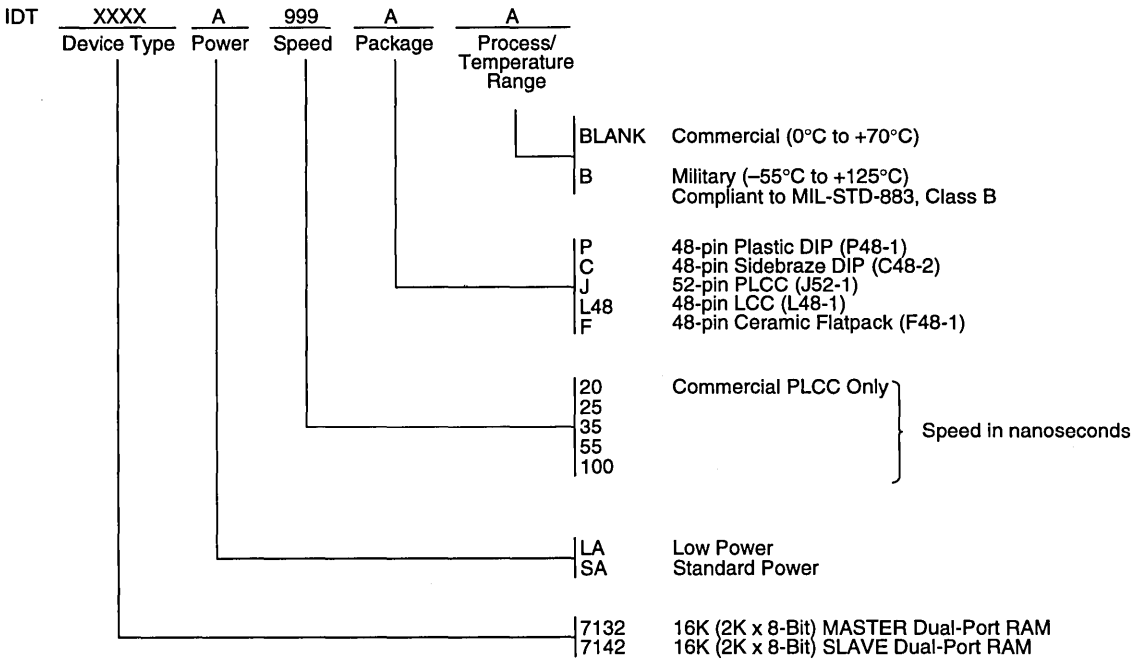


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7032 (Master) and (Slave) IDT7142 RAMs.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

6


IDT
XXXX
Device Type
A
Power
999
Speed
A
Package
A
Process/
Temperature
Range
BLANK
Commercial (0°C to +70°C)
B
Military (–55°C to +125°C)
Compliant to MIL-STD-883, Class B
P
48-pin Plastic DIP (P48-1)
C
48-pin Sidebraze DIP (C48-2)
J
52-pin PLCC (J52-1)
L48
48-pin LCC (L48-1)
F
48-pin Ceramic Flatpack (F48-1)
20
Commercial PLCC Only
25
35
55
100
Speed in nanoseconds
LA
Low Power
SA
Standard Power
7132
16K (2K x 8-Bit) MASTER Dual-Port RAM
7142
16K (2K x 8-Bit) SLAVE Dual-Port RAM

2692 drw 16

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 16K (2K x 8-BIT) WITH INTERRUPTS

IDT71321SA/LA
IDT71421SA/LA

FEATURES:

- High-speed access
  —Commercial: 20/25/35/45/55ns (max.)
- Low-power operation
  —IDT71321/IDT71421SA
  Active: 550mW (typ.)
  Standby: 5mW (typ.)
  —IDT71321/421LA
  Active: 550mW (typ.)
  Standby: 1mW (typ.)
- Two $\overline{INT}$ flags for port-to-port communications
- MASTER IDT71321 easily expands data bus width to 16-or-more-bits using SLAVE IDT71421
- On-chip port arbitration logic (IDT71321 only)
- $\overline{BUSY}$ output flag on IDT71321; $\overline{BUSY}$ input on IDT71421
- Fully asynchronous operation from either port
- Battery backup operation —2V data retention (LA Only)
- TTL-compatible, single 5V ±10% power supply
- Available in popular hermetic and plastic packages

DESCRIPTION:

The IDT71321/IDT71421 are high-speed 2K x 8 Dual-Port Static RAMs with internal interrupt logic for interprocessor communications. The IDT71321 is designed to be used as a stand-alone 8-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT71421 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-or-more-bit memory system applications results in full speed, error-free operation without the need for additional discrete logic.

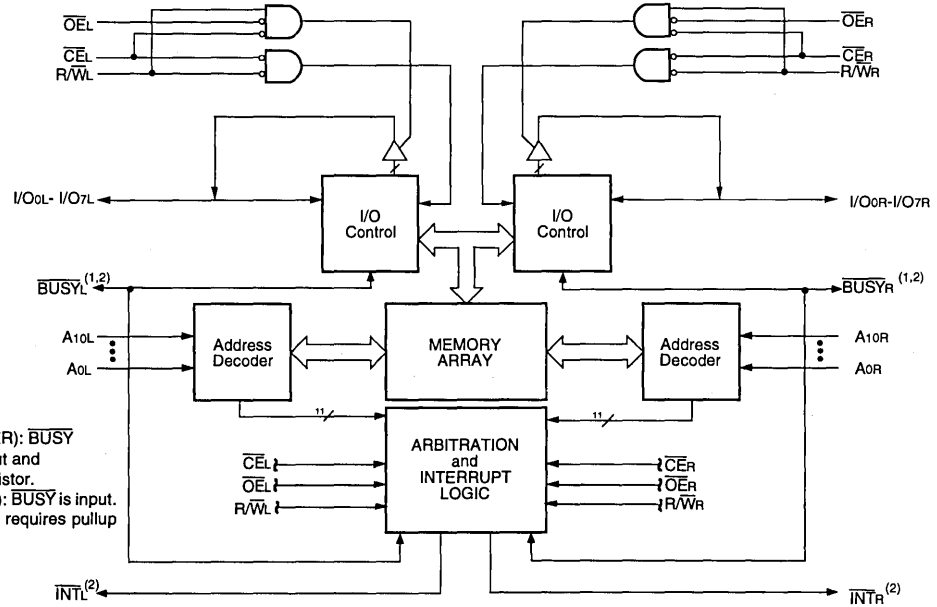
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 550mW of power. Low-power (LA) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

The IDT71321/IDT71421 devices are packaged in 52-pin PLCCs and 64-pin TQFPs.

6

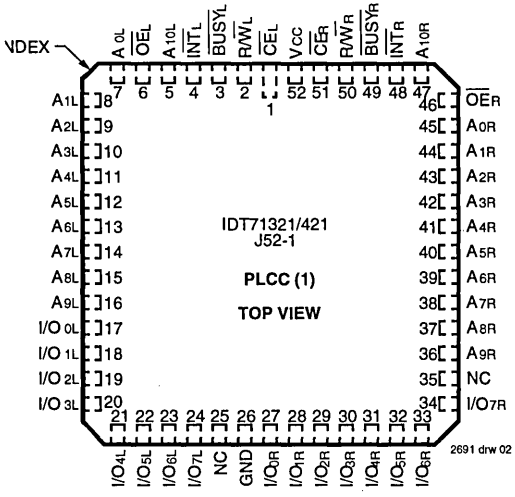
FUNCTIONAL BLOCK DIAGRAM

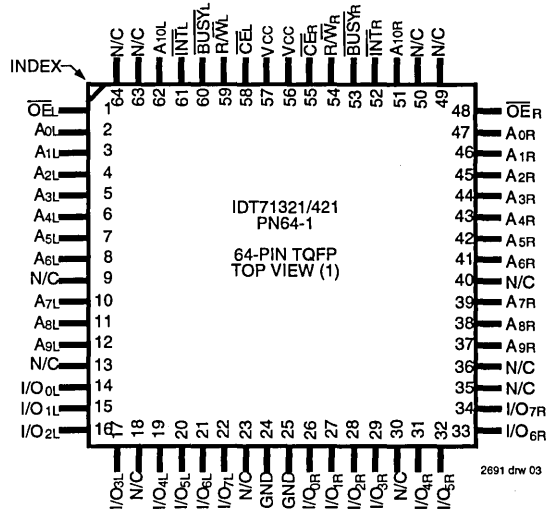


NOTES:
1. IDT71321 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor. IDT71421 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor.

2691 drw 01

PIN CONFIGURATIONS





NOTES:
1. This text does not indicate orientation of the actual part-marking.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2691 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5 for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2691 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.
2. VTERM must not exceed Vcc + 0.5V.

2691 tbl 03

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,6] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version	71321X20[2] Typ.	71321X20[2] Max.	71321X25[3] 71421X25[3] Typ.	71321X25[3] 71421X25[3] Max.	71321X35 71421X35 Typ.	71321X35 71421X35 Max.	71321X55 71421X55 Typ.	71321X55 71421X55 Max.	71321X100 71421X100 Typ.	71321X100 71421X100 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs open, f = f_{MAX}[4]	MIL. SA	—	—	110	280	80	230	65	190	65	190	mA
			LA	—	—	110	220	80	170	65	140	65	140	
			COM'L. SA	110	250	110	220	80	165	65	155	65	155	
			LA	110	200	110	170	80	120	65	110	65	110	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH}, f = f_{MAX}[4]	MIL. SA	—	—	30	80	25	80	20	65	20	65	mA
			LA	—	—	30	60	25	60	20	45	20	45	
			COM'L. SA	30	65	30	65	25	65	20	65	20	55	
			LA	30	45	30	45	25	45	20	35	20	35	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{\cdot A\cdot}$ = V_{IL} and $\overline{CE}_{\cdot B\cdot}$ = V_{IH}[7] Active Port Outputs Open, f = f_{MAX}[4]	MIL. SA	—	—	65	160	50	150	40	125	40	125	mA
			LA	—	—	65	125	50	115	40	90	40	90	
			COM'L. SA	65	165	65	150	50	125	40	110	40	110	
			LA	65	125	65	115	50	90	40	75	40	75	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, f = 0[5]	MIL. SA	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
			LA	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
			COM'L. SA	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
			LA	0.2	5	0.2	5	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{\cdot A\cdot} \leq$ 0.2V and $\overline{CE}_{\cdot B\cdot} \geq V_{CC}$ -0.2V[7] $V_{IN} \geq V_{CC}$ -0.2V or $V_{IN} \leq$ 0.2V, Active Port Outputs Open, f = f_{MAX}[4]	MIL. SA	—	—	60	155	45	145	40	110	40	110	mA
			LA	—	—	60	115	45	105	40	85	40	80	
			COM'L. SA	60	155	60	145	45	110	40	100	40	95	
			LA	60	115	60	105	45	85	40	70	40	70	

NOTES:

2689 tbl 04

1. 'X' in part numbers indicates power rating (SA or LA).
2. Com'l Only, 0°C to +70°C temperature range. PLCC package only.
3. Not available in DIP packages..
4. At f = f_{Max}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. V_{CC} = 5V, T_A=+25°C for Typ and is not production tested. $V_{CC\,DC}$ = 100mA (Typ)
7. Port "A" may be either left or right port. Port "B" is opposite from port "A".

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT71321SA IDT71421SA Min.	IDT71321SA IDT71421SA Max.	IDT71321LA IDT71421LA Min.	IDT71321LA IDT71421LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current[1]	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC} V_{CC} = 5.5V	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}/\overline{INT}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

NOTE: 1. At V_{CC} < 2.0V leakages are undefined.

2691 tbl 05

6

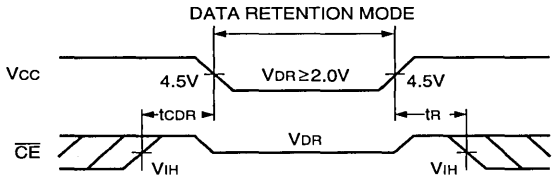
DATA RETENTION CHARACTERISTICS (LA Version Only)

Symbol	Parameter	Test Conditions		71321LA/71421LA Min.	Typ.[1]	Max.	Unit
VDR	VCC for Data Retention			2.0	—	0	V
ICCDR	Data Retention Current	VCC = 2.0V, $\overline{CE}$ ≥ VCC - 0.2V	COM'L.	—	100	1500	µA
tCDR[3]	Chip Deselect to Data Retention Time	VIN ≥ VCC - 0.2V or VIN≤ 0.2V		0	—	—	ns
tR[3]	Operation Recovery Time			tRC[2]	—	—	ns

2691 tbl 06

NOTES:
1. VCC = 2V, TA = +25°C, and is not production tested.
2. tRC = Read Cycle Time
3. This parameter is guaranteed but not production tested.

DATA RETENTION WAVEFORM



2691 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2691 tbl 07

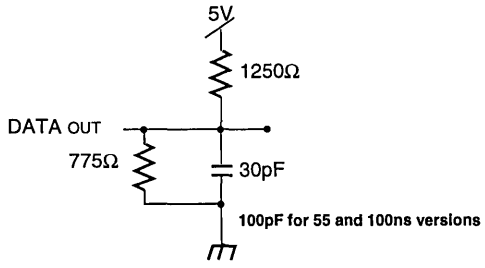


Figure 1. AC Output Test Load

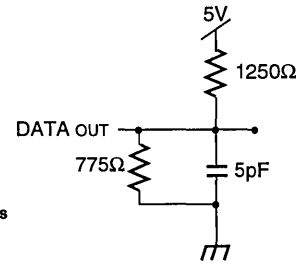
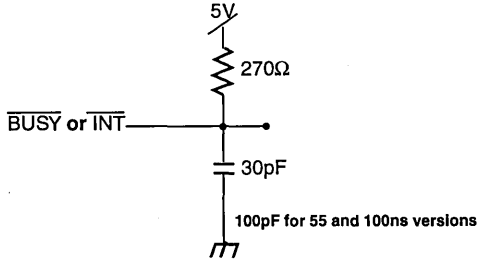


Figure 2. Output Test Load
(for tHZ, tLZ, twz, and tow)
* Including scope and jig.



2691 drw 05

Figure 3. $\overline{BUSY}$ and $\overline{INT}$ AC Output Test Load

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3]

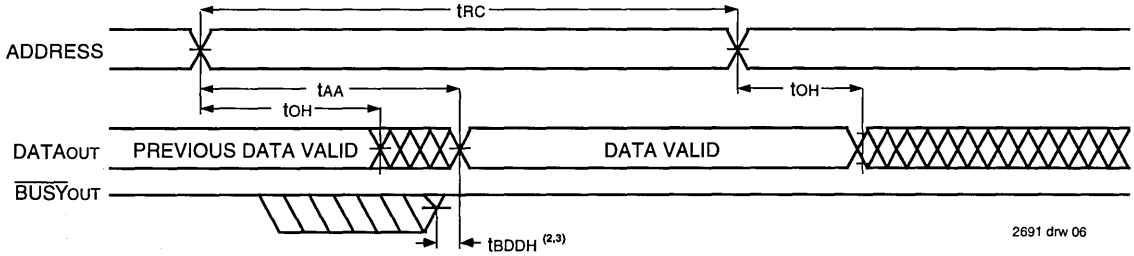
Symbol	Parameter	71321X20[2] Min.	71321X20[2] Max.	71321X25[5] 71421X25[5] Min.	71321X25[5] 71421X25[5] Max.	71321X35 71421X35 Min.	71321X35 71421X35 Max.	71321X55 71421X55 Min.	71321X55 71421X55 Max.	71321X100 71421X100 Min.	71321X100 71421X100 Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	35	—	55	—	100	—	ns
tAA	Address Access Time	—	20	—	25	—	35	—	55	—	100	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	—	55	—	100	ns
tAOE	Output Enable Access Time		11	—	12	—	20	—	25	—	40	ns
tOH	Output Hold From Address Change	3	—	3	—	3	—	3	—	10	—	ns
tLZ	Output Low-Z Time[1,4]	0	—	0	—	0	—	5	—	5	—	ns
tHZ	Output High-Z Time[1,4]	—	10	—	10	—	15	—	25	—	40	ns
tPU	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[4]	—	20	—	25	—	35	—	50	—	50	ns

NOTES:

2689 tbl 08

1. Transition is measured ±500mV from Low or High impedance voltage Output Test Load (Figure 2).
2. Com'l Only, 0°C to +70°C temperature range. PLCC package only.
3. "X" in part numbers indicates power rating (SA or LA).
4. This parameter is guaranteed by device characterization, but is not production tested.
5. Not available in DIP packages.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE [1]



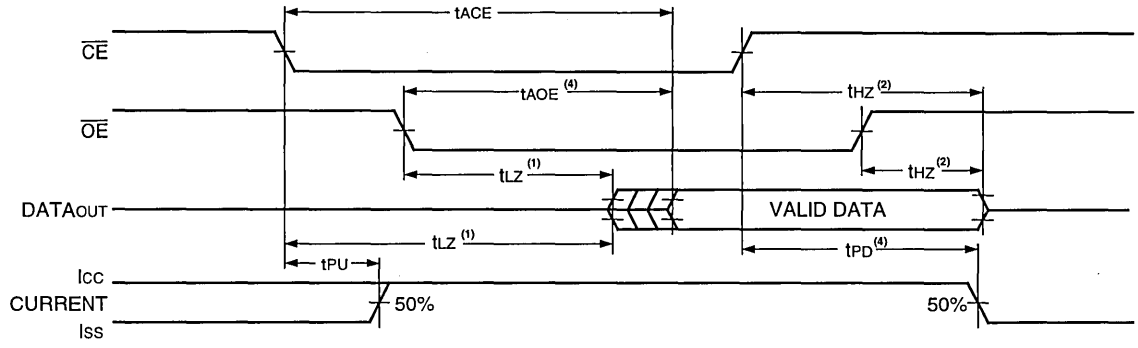
2691 drw 06

NOTES:

1. R/W = VIH, CE = VIL, and is OE = VIL. Address is valid prior to the coincidental with CE transition Low.
2. tBDD delay is required only in case where the opposite is port is completing a write operation to same the address location. For simultanious read operations BUSY has no relationship to valid output data.
3. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

6

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (3)



2691 drw 07

NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is deasserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = VIH, and the address is valid prior to other coincidental with $\overline{CE}$ transition Low.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

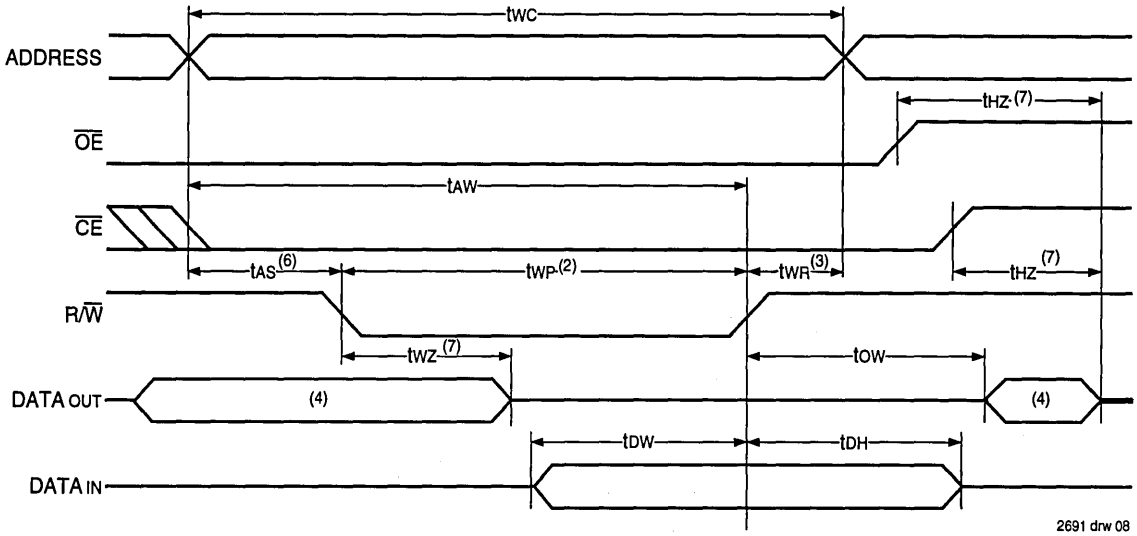
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(5)

Symbol	Parameter	71321X20(2) Min.	71321X20(2) Max.	71321X25(6) 71421X25(6) Min.	71321X25(6) 71421X25(6) Max.	71321X35 71421X35 Min.	71321X35 71421X35 Max.	71321X55 71421X55 Min.	71321X55 71421X55 Max.	71321X100 71421X100 Min.	71321X100 71421X100 Max.	Unit
Write Cycle												
tWC	Write Cycle Time(3)	20	—	25	—	35	—	55	—	100	—	ns
tEW	Chip Enable to End of Write	15	—	20	—	30	—	40	—	90	—	ns
tAW	Address Valid to End of Write	15	—	20	—	30	—	40	—	90	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width(4)	15	—	15	—	25	—	30	—	55	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	10	—	12	—	15	—	20	—	40	—	ns
tHZ	Output High Z Time(1)	—	10	—	10	—	15	—	25	—	40	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z(1)	—	10	—	10	—	15	—	30	—	40	ns
tOW	Output Active From End of Write(1)	0	—	0	—	0	—	0	—	0	—	ns

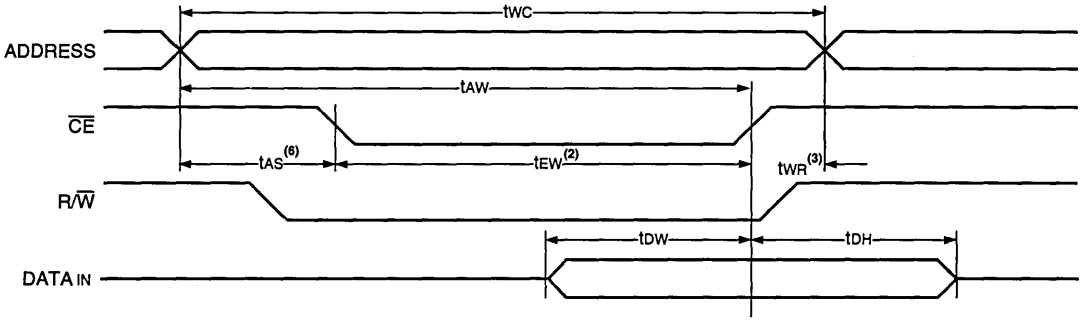
2692 tbl 09

NOTES:
1. Transition is measured ±500mV from Low or High impedance voltage with Output Test Load (Figure 2). This parameter guaranteed device characterization but is not production tested.
2. 0°C to +70°C temperature range only, PLCC package only.
3. For Master/Slave combination, tWC = tBAA + tWP, since R/$\overline{W}$ = VIL must occur after tBAA.
4. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
5. "X" in part numbers indicates power rating (SA or LA).
6. Not available in DIP packages.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/$\overline{W}$ CONTROLLED TIMING)(1,5,8)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CE}$ CONTROLLED TIMING)(1,5)



NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be High during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of $\overline{CE}$ = VIL and R/$\overline{W}$= VIL.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going High to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ Low transition occurs simultaneously with or after the R/$\overline{W}$ Low transition, the outputs remain in the High impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined be device characterization, but is not production tested. Transition is measured +/- 500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

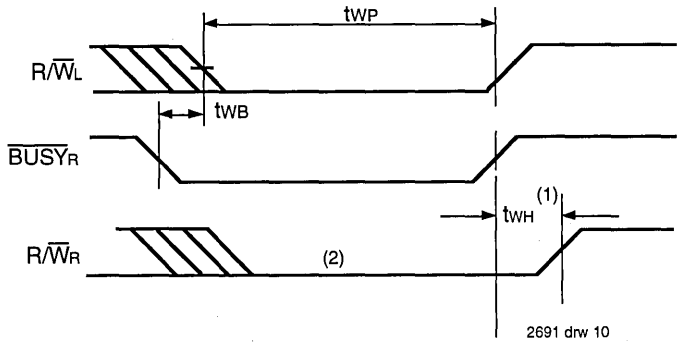
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[7]

Symbol	Parameter	71321X20[1] Min.	71321X20[1] Max.	71321X25[9] 71421X25[9] Min.	71321X25[9] 71421X25[9] Max.	71321X35 71421X35 Min.	71321X35 71421X35 Max.	71321X55 71421X55 Min.	71321X55 71421X55 Max.	71321X100 71421X100 Min.	71321X100 71421X100 Max.	Unit
Busy Timing (For Master IDT71321 Only)												
tBAA	$\overline{BUSY}$ Access Time from Address	—	20	—	20	—	20	—	30	—	50	ns
tBDA	$\overline{BUSY}$ Disable Time from Address	—	20	—	20	—	20	—	30	—	50	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	20	—	20	—	30	—	50	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	20	—	20	—	30	—	50	ns
tWDD	Write Pulse to Data Delay[2]	—	50	—	50	—	60	—	80	—	120	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	35	—	35	—	35	—	55	—	100	ns
tAPS	Arbitration Priority Set-up Time[3]	5	—	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[4]	—	20	—	25	—	35	—	55	—	100	ns
Busy Timing (For Slave IDT71421 Only)												
tWB	Write to $\overline{BUSY}$ Input[5]	0	—	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[6]	12	—	15	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay[2]	—	40	—	50	—	60	—	80	—	120	ns
tDDD	Write Data Valid to Read Data Delay[2]	—	30	—	35	—	35	—	55	—	100	ns

2689 tbl 10

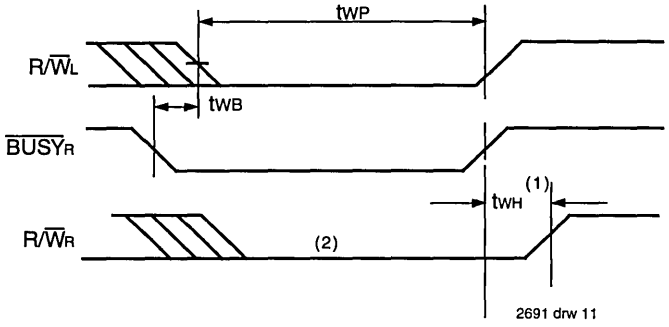
NOTES:
1. Com'l Only, 0°C to +70°C temperature range. PLCC package only.
2. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port -to-Port Read and $\overline{BUSY}$.
3. To ensure that the earlier of the two ports wins.
4. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
5. To ensure that a write cycle is inhibited on port 'B' during contention on port 'A'..
6. To ensure that a write cycle is completed on port 'B' after contention on port 'A'.
7. "X" in part numbers indicates power rating (S or L).
8. Not available in DIP package

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$[2,3,4]



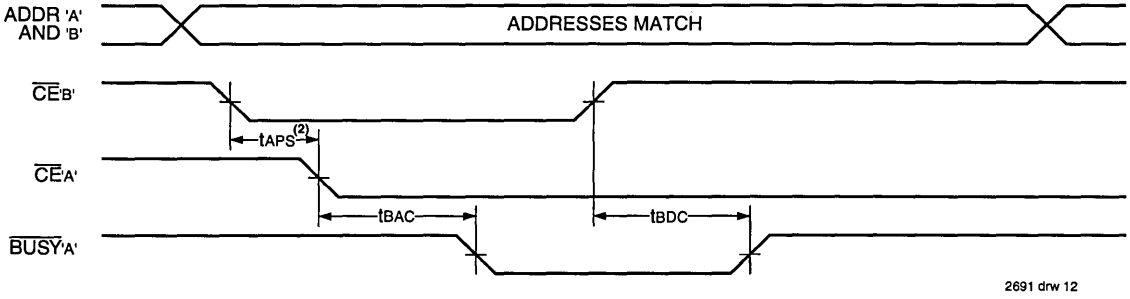
NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for Slave (IDT7142).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
3. $\overline{OE} = V_{IL}$ for the reading port.
4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is opposite from port "A".

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$[3]

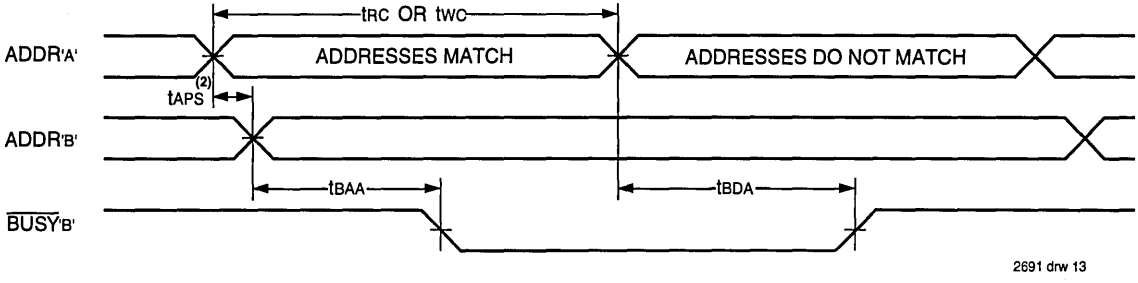


NOTES:
1. tWH must be met for both $\overline{BUSY}$ Input (IDT71421, slave) or Output (IDT71321 master).
2. $\overline{BUSY}$ is asserted on port 'B' blocking R/W'B', until $\overline{BUSY}$'B' goes High.
3. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is oppsite from port "A".

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING [1]



TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESS MATCH TIMING [1]



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If tAPS is not satisified, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted (71321 only).

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

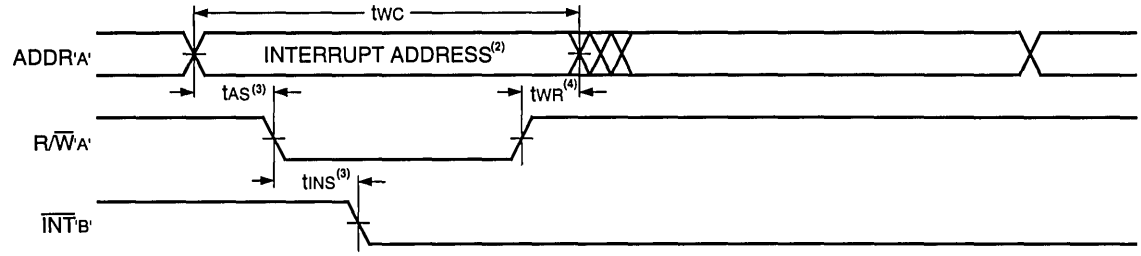
Symbol	Parameter	71321X25[3] 71421X25 Min.	Max.	71321X35 71421X35 Min.	Max.	71321X45 71421X45 Min.	Max.	71321X55 71421X55 Min.	Max.	Unit
Interrupt Timing										
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	25	—	35	—	45	ns
t_{INR}	Interrupt Reset Time	—	25	—	25	—	35	—	45	ns

2689 tbl 11

NOTES:
1. 0°C to +70°C temperature range only, PLCC package only.
2. "X" in part numbers indicates power rating (SA or LA).
3. Not available in DIP packages .

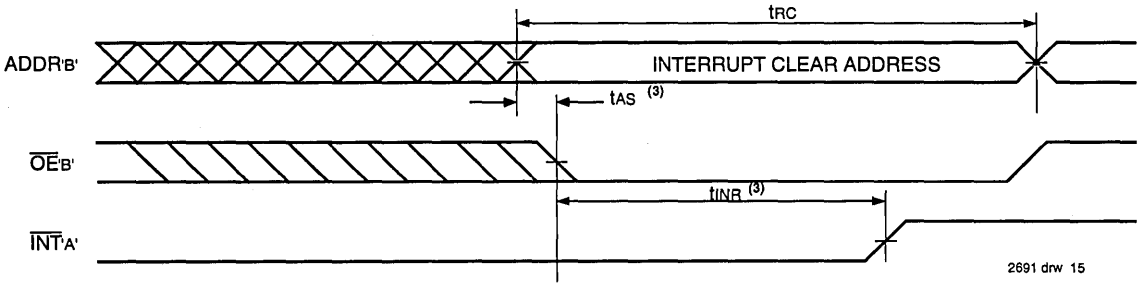
TIMING WAVEFORM OF INTERRUPT MODE

SET $\overline{INT}$



2691 drw 14

CLEAR $\overline{INT}$



2691 drw 15

NOTES:.
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. See Interrupt Truth Table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TABLE I. NON-CONTENTION READ/WRITE CONTROL[4]

Left or Right Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = V_{IH}$, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written Into Memory[2]
H	L	L	DATAOUT	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

NOTES: 2654 tbl 12

1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. 'H' = V_{IH}, 'L' = V_{IL}, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

TABLE II. INTERRUPT FLAG[1,4]

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{10L} - A_{0L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{10L} - A_{0R}$	$\overline{INT}_R$	Function
L	L	X	3FF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES: 2654 tbl 13

1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$
2. If $\overline{BUSY}_L = V_{IL}$, then No Change.
3. If $\overline{BUSY}_R = V_{IL}$, then No Change.
4. 'H' = HIGH,' L' = LOW,' X' = DON'T CARE

TABLE III — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{10L} A_{0R}-A_{10R}	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

2689 tbl 14

NOTE:

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs for IDT71321 (master). Both are inputs for IDT71421 (slave). $\overline{BUSY}_X$ outputs on the IDT71321 are open drain, not push-pull outputs. On slaves the $\overline{BUSY}_X$ input internally inhibits writes.
2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be low simultaneously.
3. Writes to the left port are internally ignored when BUSYL outputs are driving Low regardless of actual logic level on the pin. Writes to the right port are internally ignored when BUSYR outputs are driving Low regardless of actual logic level on the pin.

6

FUNCTIONAL DESCRIPTION

The IDT71321/IDT71421 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT71321/IDT71421 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = V_{IH}). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FE (HEX), where a write is defined as the $\overline{CE}$ = R/$\overline{W}$ = V_{IL} per the Truth Table. The left port clears the interrupt by access address location 7FE access when $\overline{CE}_R$ = $\overline{OE}_R$ = V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must access the memory location 7FF. The message (8 bits) at 7FE or 7FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The Busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. In slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins High. If desired, unintended write operations can be prevented to a port by tying the Busy pin for that port Low.

The Busy outputs on the IDT71321 RAM (Master) are open drain type outputs and require open drain resistors to operate. If these RAMs are being expanded in depth, then the Busy indication for the resulting array does not require the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT71321/IDT71421 RAMs the Busy pin is an output if the part is Master (IDT71321), and the Busy pin is an input if the part is a Slave (IDT71421) as shown in Figure 3.

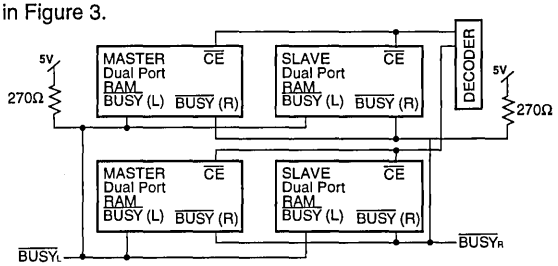
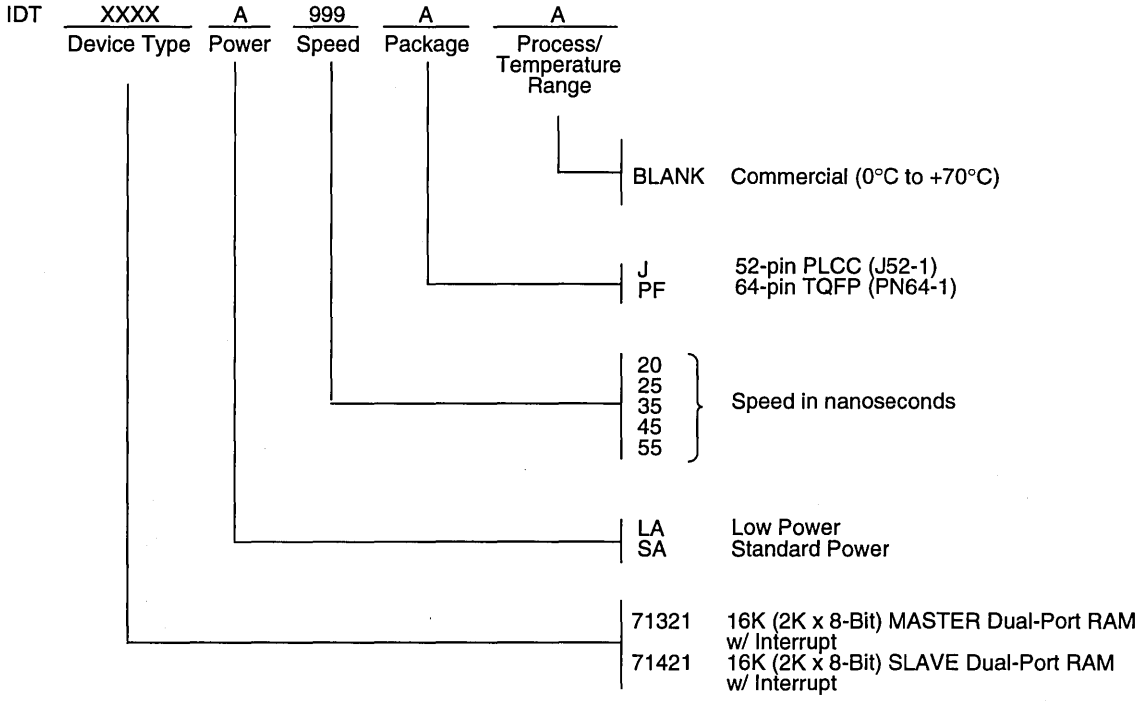


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT71321 (Master) and (Slave) IDT71421 RAMs.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The Busy arbitration, on a Master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

ORDERING INFORMATION



2691 drw 17

6

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT)

IDT7134SA
IDT7134LA

FEATURES:

- High-speed access
  - — Military: 25/35/45/55/70ns (max.)
  - — Commercial: 20/25/35/45/55/70ns (max.)
- Low-power operation
  - — IDT7134SA
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7134LA
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

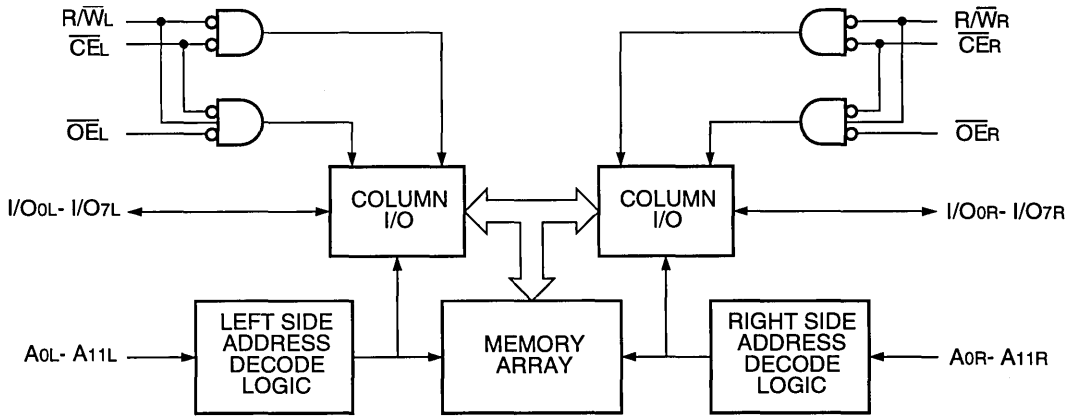
The IDT7134 is an extremely high-speed 4K x 8 Dual-Port Static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same Dual-Port RAM location.

The IDT7134 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these Dual-Port typically on only 500mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery.

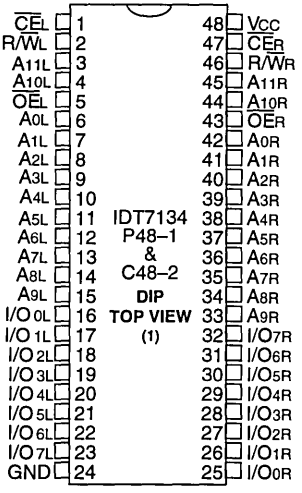
The IDT7134 is packaged on either a sidebraze or plastic 48-pin DIP, 48-pin LCC, 52-pin PLCC and 48-pin Ceramic Flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

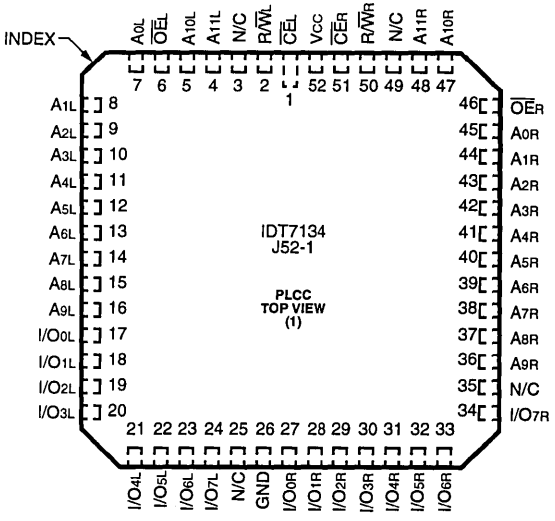


2720 drw 01

PIN CONFIGURATIONS[1]



2720 drw 02



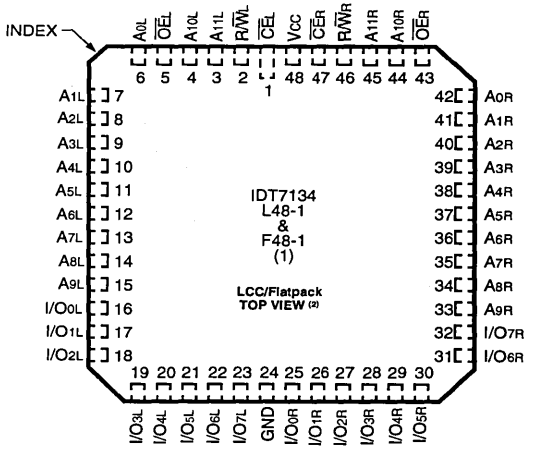
2720 drw 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
VTERM[2]	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
PT[3]	Power Dissipation	1.5	1.5	W
IOUT	DC Output Current	50	50	mA

2720 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10 ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc +0.5V.



2720 drw 04

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dv[2]	9	pF
COUT	Output Capacitance	VOUT = 3dv[2]	10	pF

2720 tbl 02

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V and from 3V to 0V.

NOTE:
1. This text does not indicate orientation of actual part-marking.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2720 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0(2)	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

NOTES:
1. VIL (min.) ≥ –1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 0.5V.

2720 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (Vcc = 5V ± 10%)

Symbol	Parameter	Test Conditions	IDT7134SA		IDT7134LA		Unit
			Min.	Max.	Min.	Max.	
|ILI|	Input Leakage Current(1)	Vcc = 5.5V, VIN = 0V to Vcc	—	10	—	5	µA
|ILO|	Output Leakage Current	$\overline{CE}$ = VIH, VOUT = 0V to Vcc	—	10	—	5	µA
VOL	Output Low Voltage	IOL = 6mA	—	0.4	—	0.4	V
		IOL = 8mA	—	0.5	—	0.5	V
VOH	Output High Voltage	IOH = –4mA	2.4	—	2.4	—	V

1. At Vcc < 2.0V input leakages are undefined.

2720 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1) (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version		7134X20(4)		7134X25		7134X35		7134X45		7134X55		7134X70		Unit
					Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	Typ.(2)	Max.	
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = VIL Outputs Open f = fMAX(3)	MIL.	S	—	—	160	310	150	300	140	280	140	270	140	270	mA
				L	—	—	160	260	150	250	140	240	140	220	140	220	
			COM'L.	S	170	280	160	280	150	260	140	240	140	240	140	240	
				L	170	240	160	220	150	210	140	200	140	200	140	200	
ISB1	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R}$ = VIH f = fMAX(3)	MIL.	S	—	—	25	100	25	75	25	70	25	70	25	70	mA
				L	—	—	25	80	25	55	25	50	25	50	25	50	
			COM'L.	S	25	110	25	80	25	75	25	70	25	70	25	70	
				L	25	80	25	50	25	45	25	40	25	40	25	40	
ISB2	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_{A'}$ = V_{IL} and $\overline{CE}_{B'}$ = V_{IH} Active Port Outputs Open, f = fMAX(3)	MIL.	S	—	—	95	210	85	200	75	190	75	180	75	180	mA
				L	—	—	95	170	85	160	75	150	75	150	75	150	
			COM'L.	S	105	180	95	180	85	170	75	160	75	160	75	160	
				L	105	150	95	140	85	130	75	130	75	130	75	130	
ISB3	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ Vcc - 0.2V	MIL.	S	—	—	1.0	30	1.0	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
		VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V, f = 0(3)	COM'L.	S	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	
				L	0.2	4.5	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	
ISB4	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}_{A'}$ or $\overline{CE}_{B'}$ ≥ Vcc - 0.2V	MIL.	S	—	—	95	210	85	190	75	180	75	170	75	170	mA
				L	—	—	95	150	85	130	75	120	75	120	75	120	
		VIN ≥ Vcc - 0.2V or VIN ≤ 0.2V Active Port Outputs Open, f = fMAX(3)	COM'L.	S	105	170	95	170	85	160	75	150	75	150	75	150	
				L	105	130	95	120	85	110	75	100	75	100	75	100	

NOTES:
1. "X" in part number indicates power rating (SA or LA).
2. Vcc = 5V, TA = +25°C for typical, and parameters are not production tested.
3. fMAX = 1/tRC = All inputs cycling at f = 1/tRC (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby ISB3.
4. (Commercial only) 0°C to +70°C temperature range.

2720 tbl 06

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

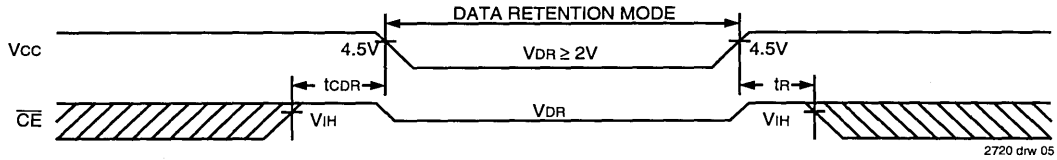
(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.(1)	Max.	Unit
V_{DR}	VCC for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	100	1500	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

NOTES:
2720 tbl 07

1. V_{CC} = 2V, T_A = +25°C, and are not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but not production tested.

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2720 tbl 08

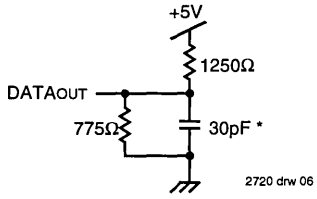


Figure 1. AC Output Test Load

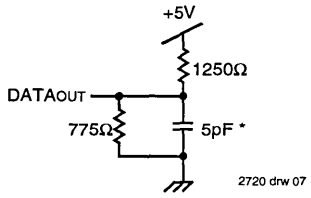


Figure 2. Output Test Load
(for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
*Including scope and jig

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[4]

Symbol	Parameter	7134X20[3] Min.	7134X20[3] Max.	7134X25 Min.	7134X25 Max.	7134X35 Min.	7134X35 Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACE}	Chip Enable Access Time	—	20	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	15	—	15	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1, 2]	3	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	15	—	15	—	20	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	20	—	25	—	35	ns

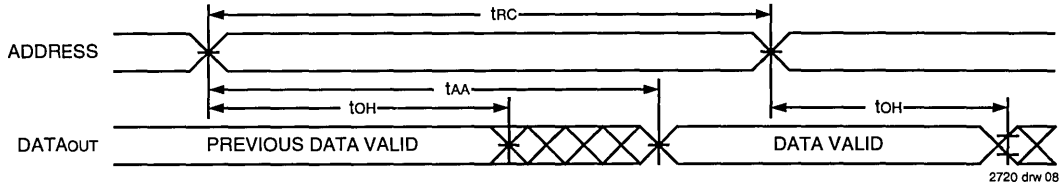
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[4] (CONT'D)

Symbol	Parameter	7134X45 Min.	7134X45 Max.	7134X55 Min.	7134X55 Max.	7134X70 Min.	7134X70 Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{ACE}	Chip Enable Access Time	—	45	—	55	—	70	ns
t_{AOE}	Output Enable Access Time	—	25	—	30	—	40	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1, 2]	5	—	5	—	5	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	20	—	25	—	30	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	45	—	50	—	50	ns

2720 tbl 09

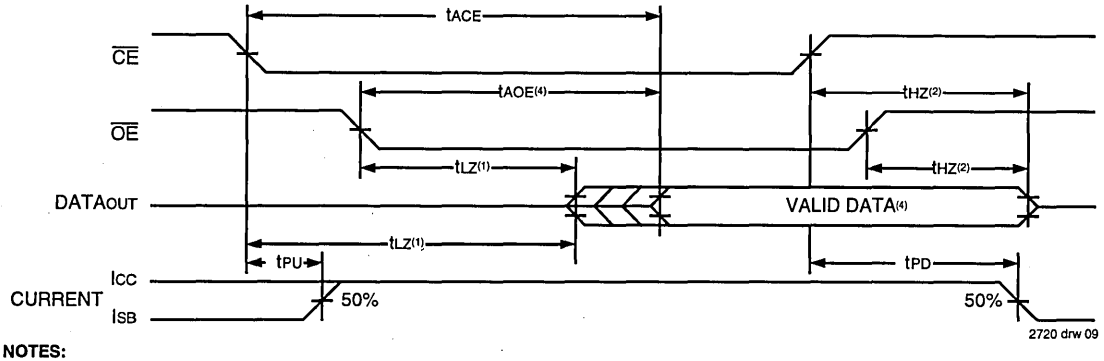
NOTES:
1. Transition is measured ±500mV fromLow or High impedance voltage with the Output Test Load (Figures 1 and 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. (Commercial only) 0°C to +70°C temperature range only.
4. "X" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



2720 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(1, 3)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/W = V_{IH} and $\overline{OE}$ = V_{IL}, unless otherwise noted.
4. Start of valid data depends on which timing becomes effective , tAOE, tACE or tAA
5. tAA for RAM Address Access and tSAA for Semaphore Address Access.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE(6)

Symbol	Parameter	7134X20(5) Min.	7134X20(5) Max.	7134X25 Min.	7134X25 Max.	7134X35 Min.	7134X35 Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time	20	—	25	—	35	—	ns
tEW	Chip Enable to End-of-Write	15	—	20	—	30	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	30	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	ns
tWR	Write RecoveryTime	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	15	—	20	—	ns
tHZ	Output High-Z Time(1, 2)	—	15	—	15	—	20	ns
tDH	Data Hold Time(3)	0	—	0	—	3	—	ns
tWZ	Write Enabled to Output in High-Z(1, 2)	—	15	—	15	—	20	ns
tOW	Output Active from End-of-Write(1, 2, 3)	3	—	3	—	3	—	ns
tWDD	Write Pulse to Data Delay(4)	—	40	—	50	—	60	ns
tDDD	Write Data Valid to Read Data Delay(4)(7)	—	30	—	30	—	35	ns

NOTES: 2720 tbl 10

1. Transition is measured ±500mV from Low or High impedance voltage with Output Test Load (Figures 1 and 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tow values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tow.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port - to - Port Read".
5. (Commercial only), 0°C to +70°C temperature range .
6. "X" in part number indicates power rating (SA or LA).
7. tDDD = 35ns for military temperature range.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[6] (CONT'D)

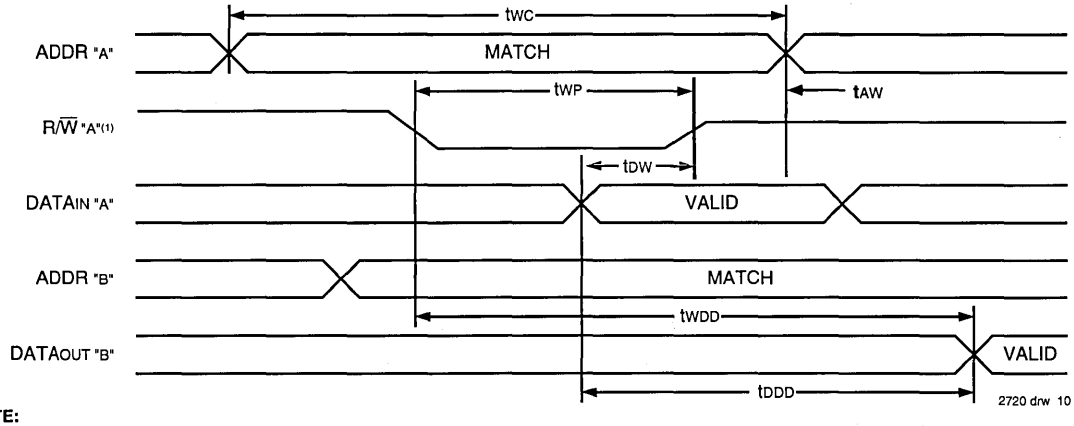
Symbol	Parameter	7134X45		7134X55		7134X70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{EW}	Chip Enable to End-of-Write	40	—	50	—	60	—	ns
t_{AW}	Address Valid to End-of-Write	40	—	50	—	60	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	60	—	ns
t_{WR}	Write RecoveryTime	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	20	—	25	—	30	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	20	—	25	—	30	ns
t_{DH}	Data Hold Time[3]	3	—	3	—	3	—	ns
t_{WZ}	Write Enabled to Output in High-Z[1, 2]	—	20	—	25	—	30	ns
t_{OW}	Output Active from End-of-Write[1, 2, 3]	3	—	3	—	3	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	70	—	80	—	90	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	—	45	—	55	—	70	ns

2720 tbl 10

NOTES:

1. Transition is measured ±500mV fromLow orHigh impedance voltage with Output Test Load (Figures 1 and 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and tow values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual tow.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port - to - Port Read".
5. (Commercial only), 0°C to +70°C temperature range .
6. "X" in part number indicates power rating (SA or LA).

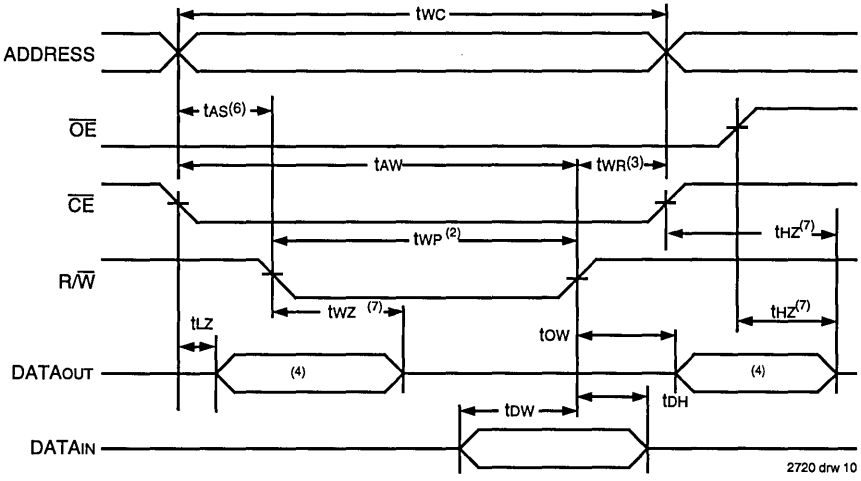
TIMING WAVEFORM OF WRITE WITH PORT - TO - PORT READ [1]



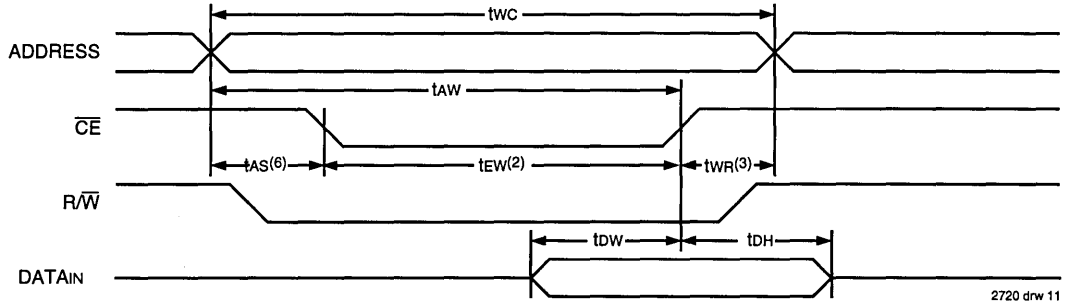
NOTE:

1. Write cycle parameters should be adhered to, in order to ensure proper writing.
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$. $\overline{OE}_{"B"} = V_{IL}$.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 5, 8)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 5)



NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be High during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a $\overline{CE}$ = VIL and R/$\overline{W}$ = VIL.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going high to the end-of-write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$)is asserted last.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured ± 500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

FUNCTIONAL DESCRIPTION

The IDT7134 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/WRITE conditions are illustrated in the table below.

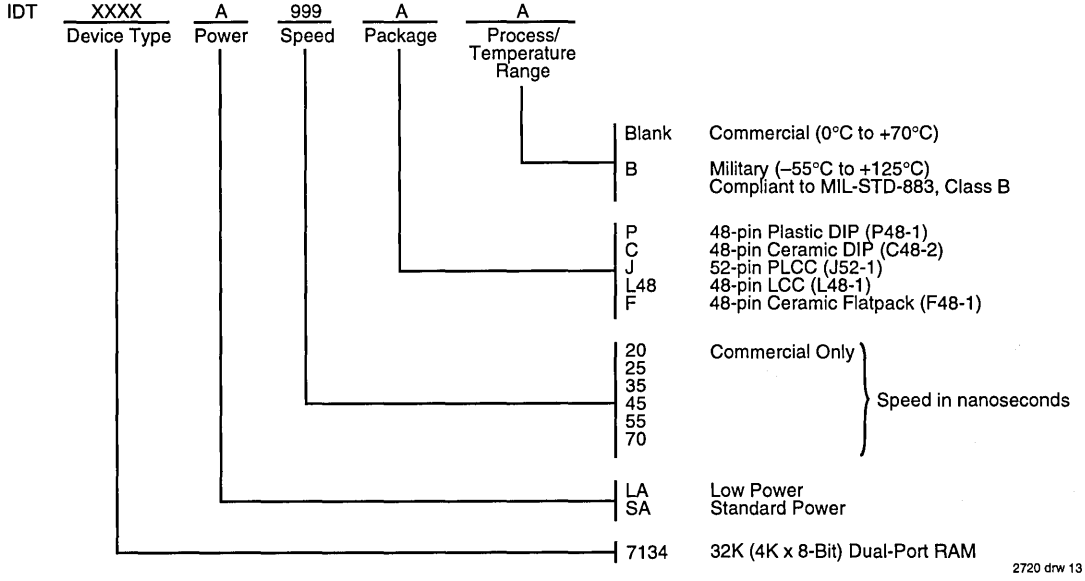
TABLE I – READ/WRITE CONTROL

Left or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D0-7	Function
X	H	X	Z	Port Disabled and in Power Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R$ = $\overline{CE}_L$ = H, Power Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on port written into memory
H	L	L	DATAOUT	Data in memory output on port
X	X	H	Z	High impedance outputs

2720 tbl 11

NOTE:
1. A_{OL} - $A_{11L} \neq A_{OR}$ - A_{11R}
"H" = HIGH, "L" = LOW, "X" = Don't Care, and "Z" = High Impedance

ORDERING INFORMATION



2720 drw 13

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 32K (4K x 8-BIT) WITH SEMAPHORE

IDT71342SA
IDT71342LA

FEATURES:

- High-speed access
  - — Commercial: 20/25/35/45/55/70ns (max.)
- Low-power opera(7) tion
  - — IDT71342SA
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - — IDT71342LA
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asynchronous operation from either port
- Full on-chip hardware support of semaphore signalling between ports
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in plastic packages

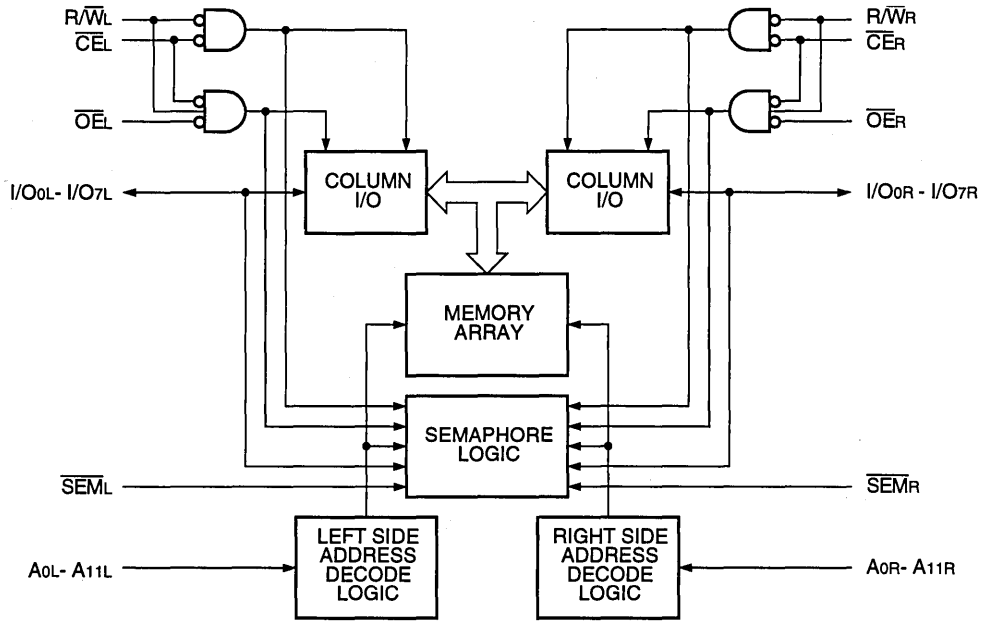
DESCRIPTION:

The IDT71342 is an extremely high-speed 4K x 8 Dual-Port Static RAM with full on-chip hardware support of semaphore signalling between the two ports.

The IDT71342 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. To assist in arbitrating between ports, a fully independent semaphore logic block is provided. This block contains unassigned flags which can be accessed by either side; however, only one side can control the flag at any time. An automatic power down feature, controlled by $\overline{CE}$ and $\overline{SEM}$, permits the on-chip circuitry of each port to enter a very low standby power mode (both $\overline{CE}$ and $\overline{SEM}$ high).

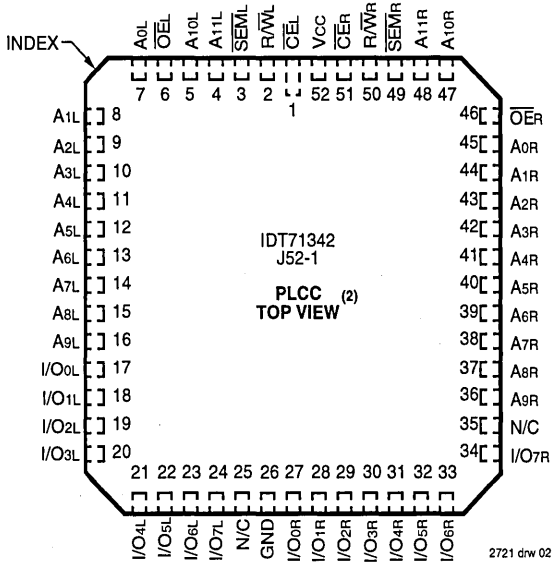
Fabricated using IDT's CMOS high-performance technology, this device typically operates on only 500mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200µW from a 2V battery. The device is packaged in either a 64-pin TQFP, thin quad plastic flatpack, or a 52-pin PLCC.

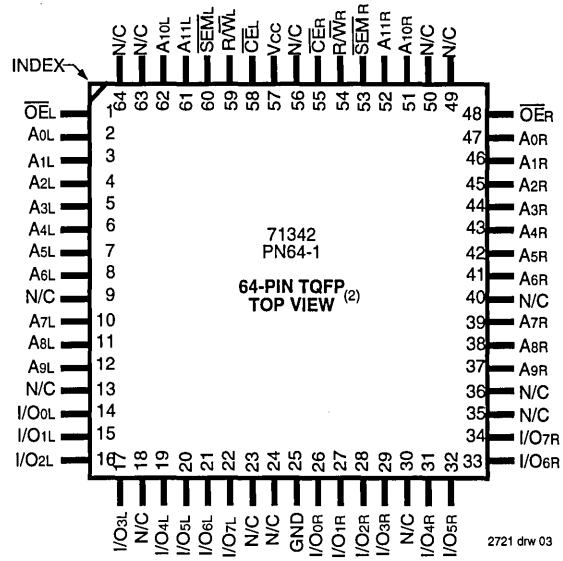
FUNCTIONAL BLOCK DIAGRAM



2721 drw 01

PIN CONFIGURATIONS[1]





NOTE:
1. Index indicator is Pin 1 ID in package outline.
2. This text does not indicate orientation of actual part-marking.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}[2]	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T[3]	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

2721 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25%of the cycle time or 10 ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc +0.5V.

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

2721 tbl 02

NOTE:
1. This parameter is determined by device characterization but is not production tested.
2. 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V and from 3V to 0V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2721 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

2721 tbl 04

NOTE:
1. V_{IL} (min.) ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Conditions	IDT71342SA		IDT71342LA		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 6mA	—	0.4	—	0.4	V
		I_{OL} = 8mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V

2721 tbl 05

NOTES:

1. At V_{CC} ≤ 2.0V input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Version	71342X20		71342X25		71342X35		71342X45		71342X55		71342X70		Unit
				Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open $\overline{SEM}$ = Don't Care f = f_{MAX}[3]	COM'L. S	—	280	—	280	—	260	—	240	—	240	—	240	mA
			L	—	240	—	240	—	220	—	200	—	200	—	200	
ICC1	Dynamic Operating Current (Semaphores Both Sides)	$\overline{CE}$ = V_{IH} Outputs Open $\overline{SEM}$ ≤ V_{IL} f = f_{MAX}[3]	COM'L. S	—	280	—	200	—	185	—	170	—	170	—	170	mA
			L	—	240	—	170	—	155	—	140	—	140	—	140	
ISB1	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} $\overline{SEM}_L$ = $\overline{SEM}_R$ ≥ V_{IH} f = f_{MAX}[3]	COM'L. S	25	80	25	80	25	75	25	70	25	70	25	70	mA
			L	25	80	25	50	25	45	25	40	25	40	25	40	
ISB2	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_{A*}$ = V_{IL} and $\overline{CE}_{B*}$ = V_{IH} Active Port Outputs Open, f = f_{MAX}[3]	COM'L. S	—	180	—	180	—	170	—	160	—	160	—	160	mA
			L	—	150	—	150	—	140	—	130	—	130	—	130	
ISB3	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V $\overline{SEM}_L$ = $\overline{SEM}_R$ ≥ V_{CC} - 0.2V, f = 0[3]	COM'L. S	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	1.0	15	mA
			L	0.2	4.5	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	0.2	4.0	
ISB4	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}_{A*}$ or $\overline{CE}_{B*}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V $\overline{SEM}_L$ = $\overline{SEM}_R$ ≥ V_{CC} - 0.2V Active Port Outputs Open, f = f_{MAX}[3]	COM'L. S	—	170	—	170	—	150	—	150	—	150	—	150	mA
			L	—	140	—	140	—	130	—	120	—	120	—	120	

2721 tbl 06

NOTES:

1. "X" in part number indicates power rating (SA or LA).
2. V_{CC} = 5V, T_A = +25°C for typical, and parameters are not production tested.
3. f_{MAX} = 1/t_{RC} = All inputs cycling at f = 1/t_{RC} (except Output Enable). f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby I_{SB3}.

6

DATA RETENTION CHARACTERISTICS

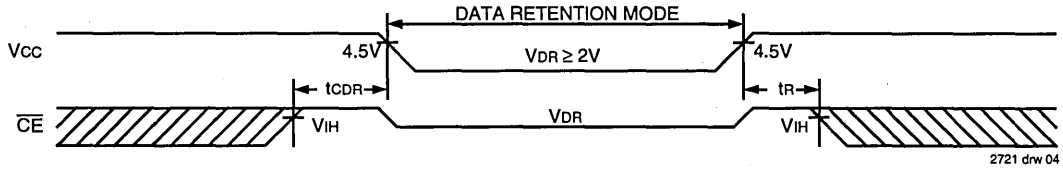
(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition	Min.	Typ.[1]	Max.	Unit
V_{DR}	VCC for Data Retention	—	2.0	—	—	V
I_{CCDR}	Data Retention Current	V_{CC} = 2V, $\overline{CE} \geq V_{HC}$ COM'L. $\overline{SEM} \geq V_{HC}$	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	0	—	—	ns
t_R[3]	Operation Recovery Time		t_{RC}[2]	—	—	ns

2721 tbl 07

NOTES:
1. V_{CC} = 2V, T_A = +25°C, and are not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2721 tbl 08

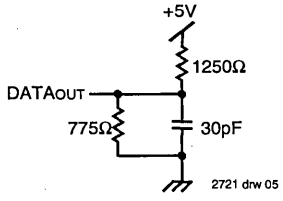


Figure 1. AC Output Test Load

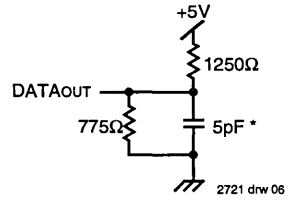


Figure 2. Output Test Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
*Including scope and jig

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[5]

Symbol	Parameter	71342X20		71342X25		71342X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACE}	Chip Enable Access Time[3]	—	20	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	15	—	15	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1, 2]	3	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	15	—	15	—	20	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	—	—	10	—	15	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	40	—	50	—	60	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	—	30	—	30	—	35	ns
t_{SAA}	Semaphore Address Access Time	—	—	—	25	—	35	ns

2721 tbl 09

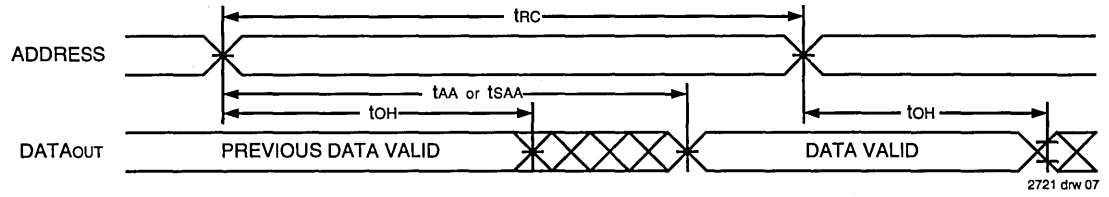
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[5] (CONT'D)

Symbol	Parameter	71342X45		71342X55		71342X70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70	ns
t_{ACE}	Chip Enable Access Time[3]	—	45	—	55	—	70	ns
t_{AOE}	Output Enable Access Time	—	25	—	30	—	40	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1, 2]	5	—	5	—	5	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	20	—	25	—	30	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	50	—	50	—	50	ns
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	20	—	20	—	ns
t_{WDD}	Write Pulse to Data Delay[4]	—	70	—	80	—	90	ns
t_{DDD}	Write Data Valid to Read Data Delay[4]	—	45	—	55	—	70	ns
t_{SAA}	Semaphore Address Access Time	—	45	—	55	—	70	ns

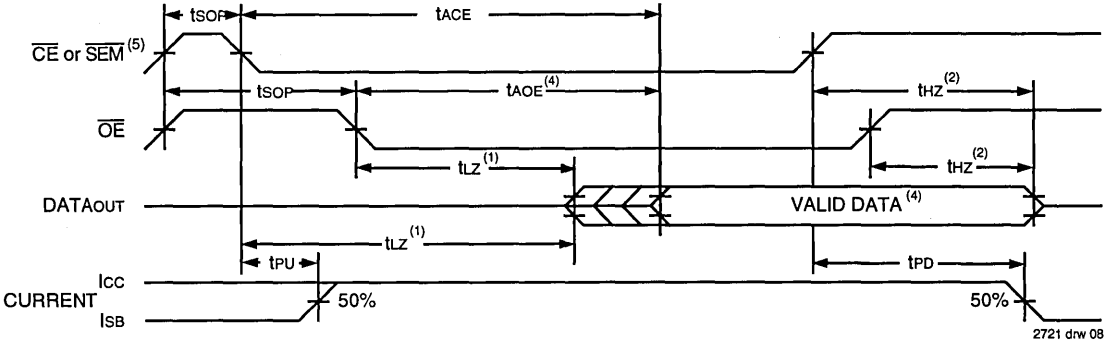
2721 tbl 10

NOTES:
1. Transition is measured ±500mV from Low or High impedance voltage with the Ouput Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, and $\overline{SEM}$ = V_{IL}.
4. "X" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE(1, 2, 4)

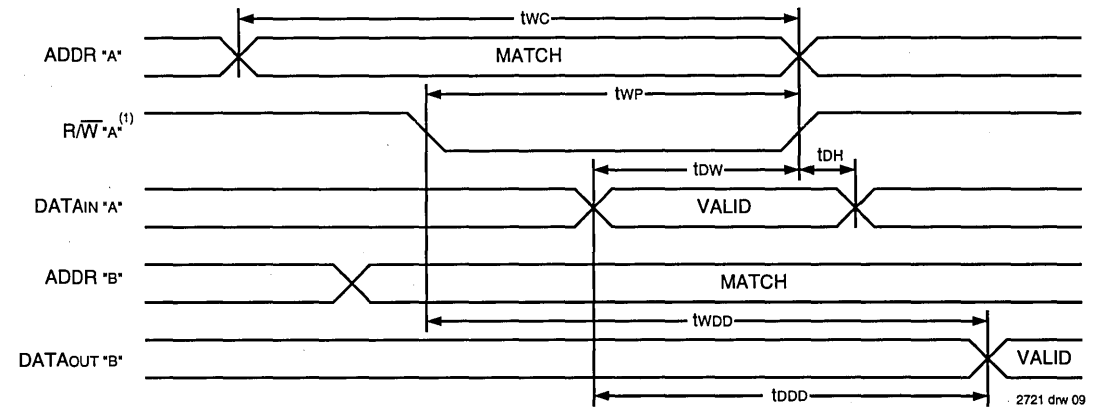


TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(1, 3)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/W = VIH and $\overline{OE}$ = VIL, unless otherwise noted.
4. Start of valid data depends on which timing becomes effective last; tAOE, tACE, or tAA
5. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. tAA is for RAM Address Access and tSAA is for Semaphore Address Access.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ (1, 2)



NOTE:
1. Write cycle parameters should be adhered to, in order to ensure proper writing.
2. $\overline{CE}_L = \overline{CE}_R$ = VIL. $\overline{CE}$"B" = VIL.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[6]

Symbol	Parameter	71342X20		71342X25		71342X35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t_{EW}	Chip Enable to End-of-Write[3]	15	—	20	—	30	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	15	—	20	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	15	—	15	—	20	ns
t_{DH}	Data Hold Time[4]	0	—	0	—	3	—	ns
t_{WZ}	Write Enabled to Output in High-Z[1, 2]	—	15	—	15	—	20	ns
t_{OW}	Output Active from End-of-Write[1, 2, 4]	3	—	3	—	3	—	ns
t_{SWR}	SEM Flag Write to Read Time	10	—	10	—	10	—	ns
t_{SPS}	SEM Flag Contention Window	10	—	10	—	10	—	ns

2721 tbl 11

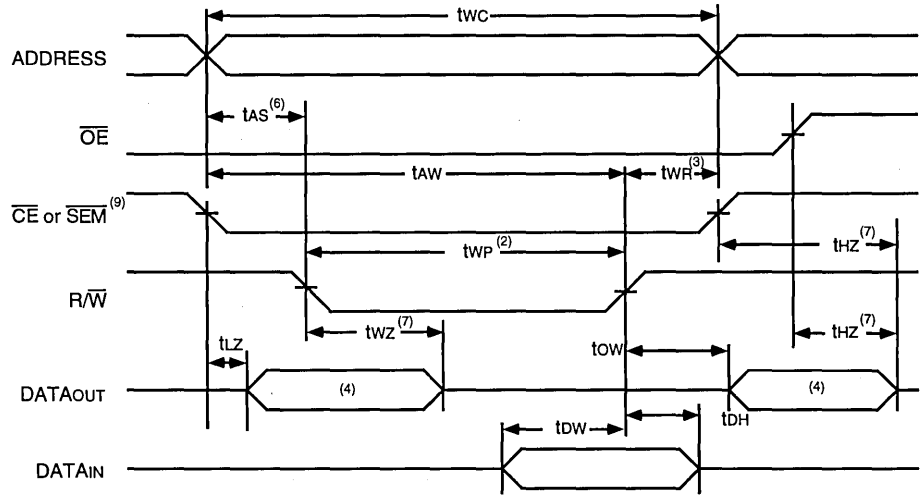
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[6](CONT'D)

Symbol	Parameter	71342X45		71342X55		71342X70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	45	—	55	—	70	—	ns
t_{EW}	Chip Enable to End-of-Write[3]	40	—	50	—	60	—	ns
t_{AW}	Address Valid to End-of-Write	40	—	50	—	60	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	40	—	50	—	60	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	20	—	25	—	30	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	20	—	25	—	30	ns
t_{DH}	Data Hold Time[4]	3	—	3	—	3	—	ns
t_{WZ}	Write Enabled to Output in High-Z[1, 2]	—	20	—	25	—	30	ns
t_{OW}	Output Active from End-of-Write[1, 2, 4]	3	—	3	—	3	—	ns
t_{SWR}	SEM Flag Write to Read Time	10	—	10	—	10	—	ns
t_{SPS}	SEM Flag Contention Window	10	—	10	—	10	—	ns

2721 tbl 12

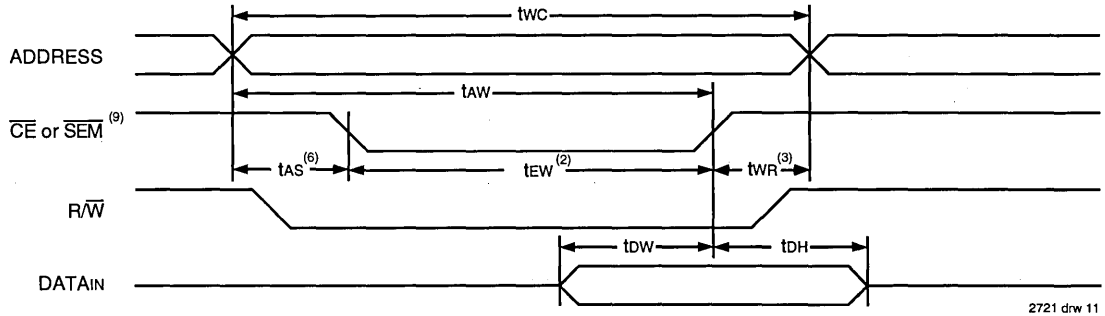
NOTES:
1. Transition is measured ±500mV from Low or High impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. "X" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1, 5,8)



2721 drw 10

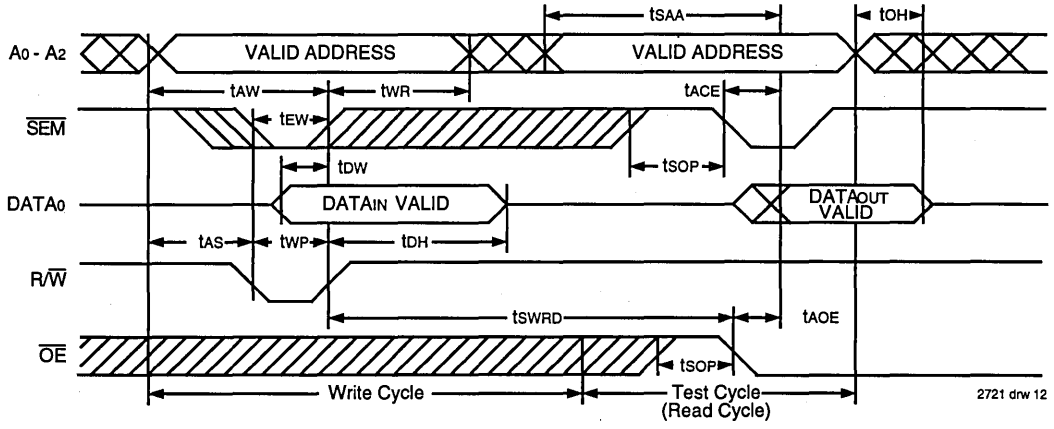
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 5)



2721 drw 11

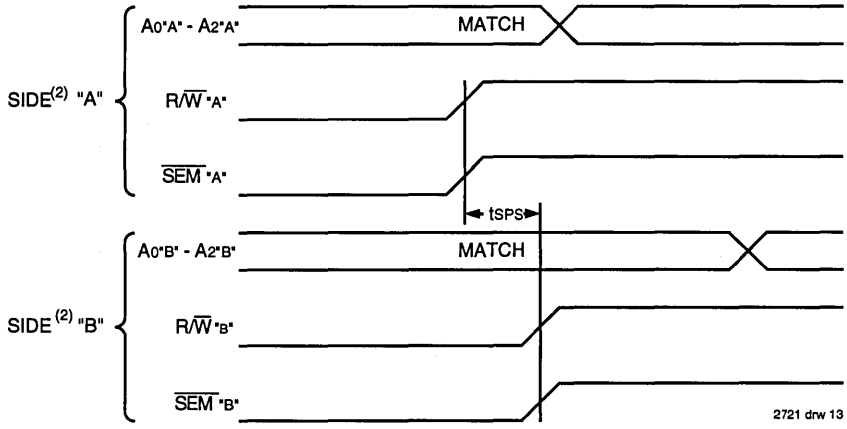
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be High during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of either $\overline{CE}$ or $\overline{SEM}$ = VIL and R/$\overline{W}$ = VIL.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going High to the end-of-write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ Low transition occurs simultaneously with or after the R/$\overline{W}$ Low transition, the outputs remain in the High - impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured ±500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ =VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE CONTENTION[1, 3, 4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}_R$ = $\overline{CE}_L$ = VIH, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from the point where R/$\overline{W}$ "A" or $\overline{SEM}$ "A" goes High until R/$\overline{W}$ "B" or $\overline{SEM}$ "B" goes High.
4. If tSPS is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

FUNCTIONAL DESCRIPTION

The IDT71342 is an extremely fast Dual-Port 4K x 8 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAMs and can be read from or written to at the same time, with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Table 1 where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT71342 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT71342's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT71342 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor had set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT71342 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through the address pins A_0–A_2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other (see Table II). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence of WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as a one, a fact which the processor will verify by the subsequent read (see Table II). As an example, assume a

processor writes a zero in the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during a subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 3. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first

TABLE I — NON-CONTENTION READ/WRITE CONTROL

Left or Right Port[1]					
R/$\overline{W}$	$\overline{CE}$	$\overline{SEM}$	$\overline{OE}$	D_{0-7}	Function
X	H	H	X	Z	Port Disabled and in Power Down Mode
H	H	L	L	DATAOUT	Data in Semaphore Flag Output on Port
X	X	X	H	Z	Output Disabled
↑	H	L	X	DATAIN	Port Data Bit D0 Written Into Semaphore Flag
H	L	H	L	DATAOUT	Data in Memory Output on Port
L	L	H	X	DATAIN	Data on Port Written Into Memory
X	L	L	X	—	Not Allowed

2721 tbl 13

NOTE:
1. $A_{OL} = A_{10L} \neq A_{0R} - A_{10R}$.
"H" = HIGH, "L" = LOW, "X" = Don't Care, "Z" = High Impedance, and
"↑" = Low-to-High transition.

TABLE II — EXAMPLE SEMAPHORE PROCUREMENT SEQUENCE[1]

Function	$D_0 - D_7$ Left	$D_0 - D_7$ Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left side has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

2721 tbl 14

NOTE:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT71342.

side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen. Code integrity is of the utmost importance when semaphores are used instead of slower, more restrictive hardware intensive schemes.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES–Some examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT71342's Dual-Port RAM. Say the 4K x 8 RAM was to be divided into two 2K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of the memory.

To take a resource, in this example the lower 2K of Dual-Port RAM, the processor on the left port could write and then read a zero into Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 2K. Meanwhile, the right processor would attempt to perform the same function. Since this processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 2K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 2K blocks of Dual-Port RAM with each other.

The blocks do not have to by any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices had determined which memory area was "off limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

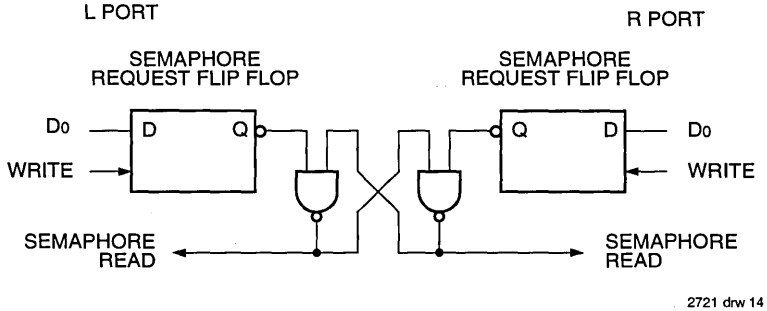
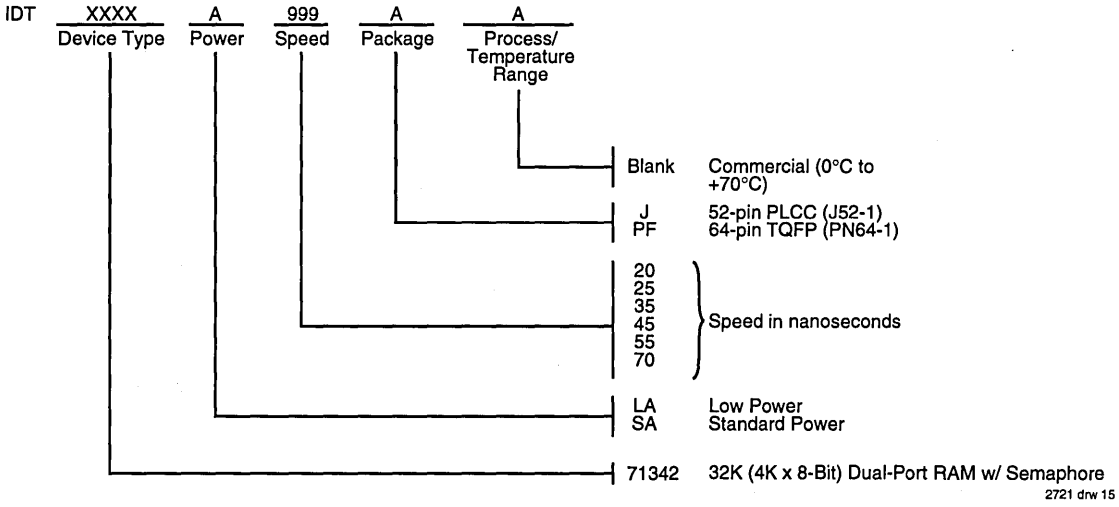


Figure 3. IDT71342 Semaphore Logic

ORDERING INFORMATION



2721 drw 15

6

Integrated Device Technology, Inc.

HIGH-SPEED 8K x 8 DUAL-PORT STATIC RAM

IDT7005S/L

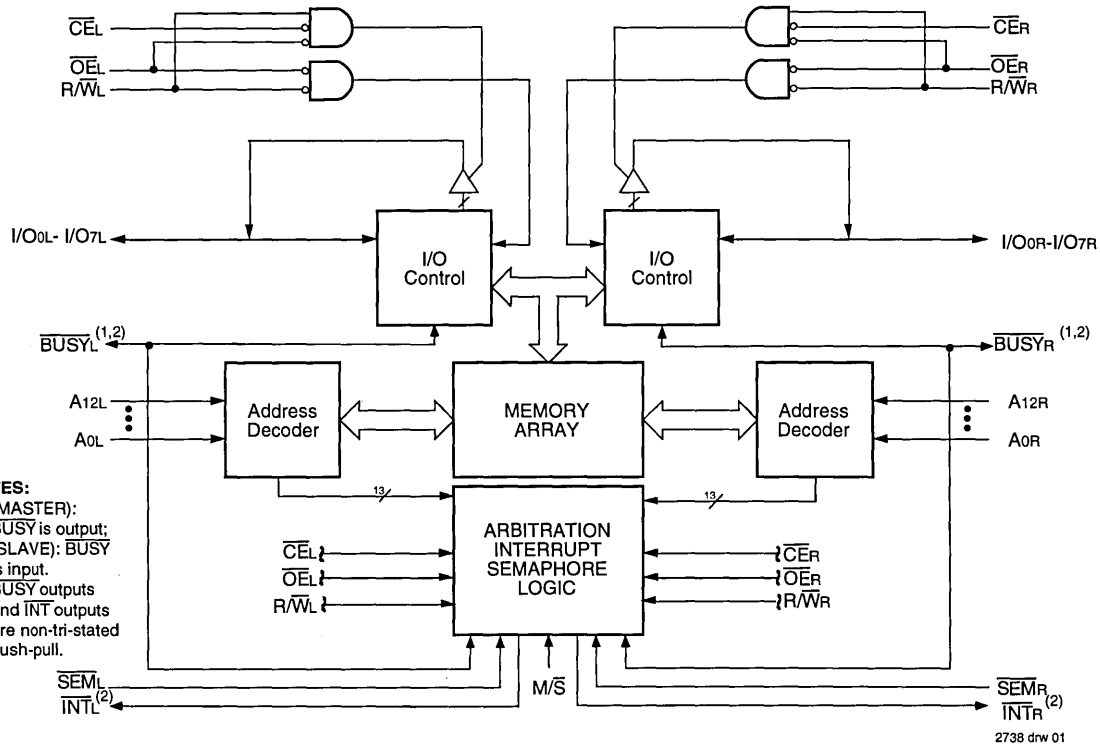
FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 25/35/55/70ns (max.)
  - — Commercial:17/20/25/35/55ns (max.)
- Low-power operation
  - — IDT7005S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7005L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- IDT7005 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master, M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Devices are capable of withstanding greater than 2001V electrostatic discharge
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Available in 68-pin PGA, quad flatpack, and PLCC, and a 64-pin TQFP
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7005 is a high-speed 8K x 8 Dual-Port Static RAM. The IDT7005 is designed to be used as a stand-alone 64K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.

2738 drw 01

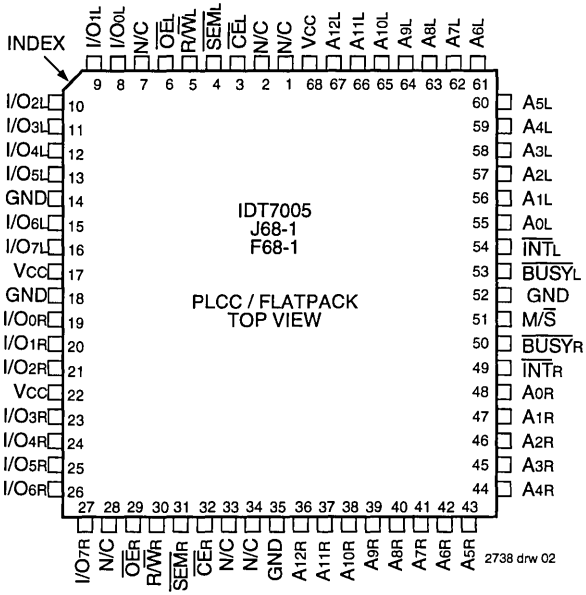
Port RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

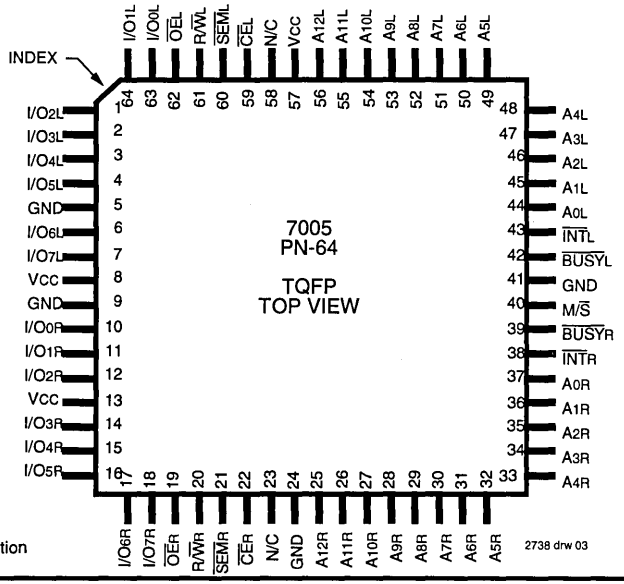
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500µW from a 2V battery.

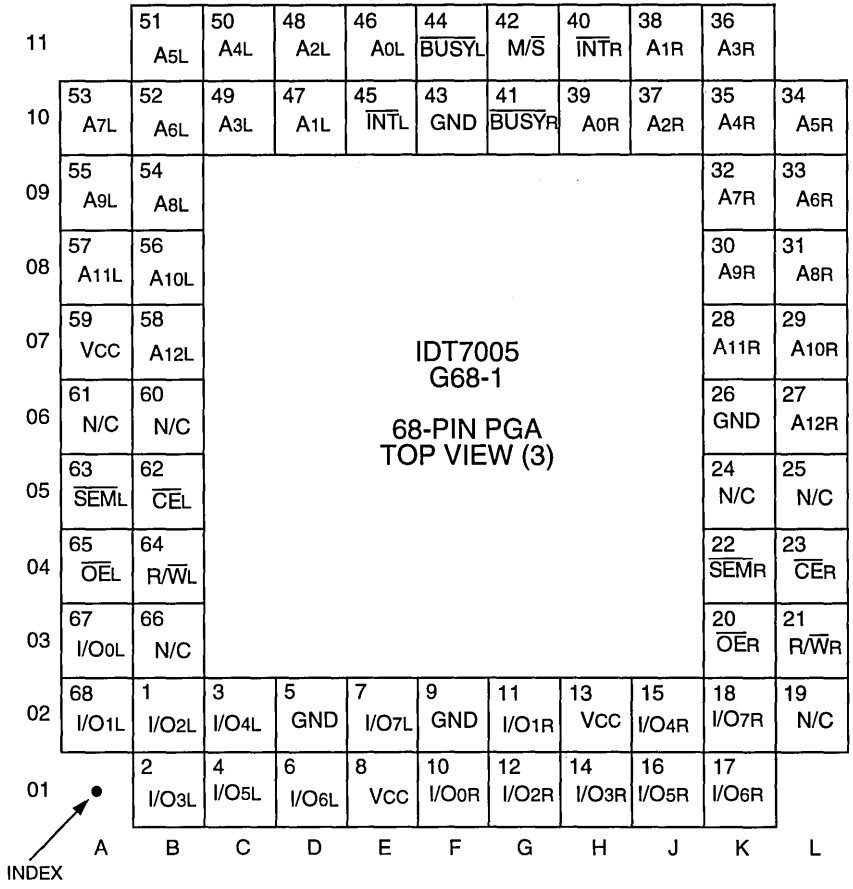
The IDT7005 is packaged in a ceramic 68-pin PGA, an 68-pin quad flatpack, a PLCC and a 64-pin thin plastic quad flatpack, (TQFP). Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS





NOTE:
This text does not indicate orientation of the the actual part-marking.



2738 drw 04

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{12L}$	$A_{0R} - A_{12R}$	Address
$I/O_{0L} - I/O_{7L}$	$I/O_{0R} - I/O_{7R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2738 tbl 01

NOTES:
1. All V_{CC} pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	X	X	H	High-Z	Deselected: Power-Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read Memory
X	X	H	X	High-Z	Outputs Disabled

NOTE:
1. A_{0L} — A_{12L} IS NOT EQUAL TO A_{0R} — A_{12R}

2738 tbl 02

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL(1)

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	H	L	L	DATAOUT	Read in Semaphore Flag Data 0ut
H	↑	X	L	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	—	Not Allowed

2738 tbl 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10% maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 0.5V.

2738 tbl 04

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2738 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTES:
1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

2738 tbl 06

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dvV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dvV	10	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested. TQFP Package only.
2. 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

2738 tbl 07

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7005S		IDT7005L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

NOTE:
1. At V_{CC} = 2.0V input leakages are undefined.

2738 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7005X17 Com'l Only		7005X20 Com'l Only		7005X25		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \leq V_{IL}$, Outputs Open $\overline{SEM} \geq V_{IH}$ f = f_{MAX}[3]	MIL.	S	—	—	—	—	155	340	mA
				L	—	—	—	—	155	280	
			COM'L.	S	170	310	160	290	155	265	
				L	170	260	160	240	155	220	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE_L} = \overline{CE_R} \geq V_{IH}$ $\overline{SEM_R} = \overline{SEM_L} \geq V_{IH}$ f = f_{MAX}[3]	MIL.	S	—	—	—	—	16	80	mA
				L	—	—	—	—	16	65	
			COM'L.	S	25	60	20	60	16	60	
				L	25	50	20	50	16	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A"=V_{IL} and $\overline{CE}$"B"=V_{IH}[5] Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM_R} = \overline{SEM_L} \geq V_{IH}$	MIL.	S	—	—	—	—	90	215	mA
				L	—	—	—	—	90	180	
			COM'L.	S	105	190	95	180	90	170	
				L	105	160	95	150	90	140	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R} \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[4] $\overline{SEM_R} = \overline{SEM_L} \geq V_{CC}$ - 0.2V	MIL.	S	—	—	—	—	1.0	30	mA
				L	—	—	—	—	0.2	10	
			COM'L.	S	1.0	15	1.0	15	1.0	15	
				L	0.2	5	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE_R} \geq V_{CC}$ - 0.2v $\overline{SEM_R} = \overline{SEM_L} \geq V_{CC}$ - 0.2V	MIL.	S	—	—	—	—	85	200	mA
				L	—	—	—	—	85	170	
		$V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2v Active Port Outputs Open, f = f_{MAX}[3]	COM'L.	S	100	170	90	155	85	145	
				L	100	140	90	130	85	120	

NOTES:
1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. $I_{CC\,DC}$ = 120mA (TYP)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A"may be either left or right port. Port "B" is the port opposite port "A".

2738 tbl 09

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7005X35 Typ.[2]	7005X35 Max.	7005X55 Typ.[2]	7005X55 Max.	7005X70 MIL ONLY Typ.[2]	7005X70 MIL ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open, $\overline{SEM}$ = V_{IH}, f = f_{MAX}[3]	MIL.	S	150	300	150	300	140	300	mA
				L	150	250	150	250	140	250	
			COM'L.	S	150	250	150	250	—	—	
				L	150	210	150	210	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE_L}$ = $\overline{CE_R}$ = V_{IH}, $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH}, f = f_{MAX}[3]	MIL.	S	13	80	13	80	10	80	mA
				L	13	65	13	65	10	65	
			COM'L.	S	13	60	13	60	—	—	
				L	13	50	13	50	—	—	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A"=V_{IL} and $\overline{CE}$"B"=V_{IL}[5], Active Port Outputs Open, f = f_{MAX}[3], $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH}	MIL.	S	85	190	85	190	80	190	mA
				L	85	160	85	160	80	160	
			COM'L.	S	85	155	85	155	—	—	
				L	85	130	85	130	—	—	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{CC} - 0.2V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4], $\overline{SEM_R}$ = $\overline{SEM_L}$ ≥ V_{CC} - 0.2V	MIL.	S	1.0	30	1.0	30	1.0	30	mA
				L	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	—	—	
				L	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}$"A" ≤ 0.2V, $\overline{CE}$"B" ≥ V_{CC} - 0.2V[5], $\overline{SEM_R}$ = $\overline{SEM_L}$ ≥ V_{CC} - 0.2V	MIL.	S	80	175	80	175	75	175	mA
				L	80	150	80	150	75	150	
		V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V	COM'L.	S	80	135	80	135	—	—	
		Active Port Outputs Open, f = f_{MAX}[3]		L	80	110	80	110	—	—	

NOTES:
1. 'X' in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C and are not production tested. $I_{CC\,DC}$ = 120mA (TYP)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the port opposite port "A".

2738 tbl 10

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

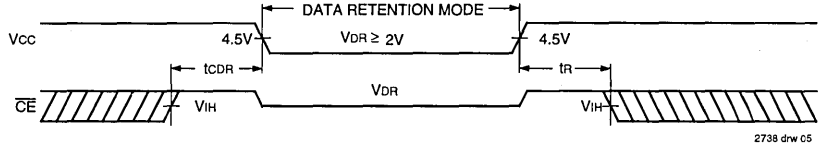
(V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)[4]

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ ≥ V_{HC}	MIL.	—	100	4000	µA
		V_{IN} ≥ V_{HC} or ≤ V_{LC}	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time	$\overline{SEM}$ ≥ V_{HC}		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. T_A = +25°C, V_{CC} = 2V
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

2738 tbl 11

DATA RETENTION WAVEFORM



2738 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1 & 2

2738 tbl 12

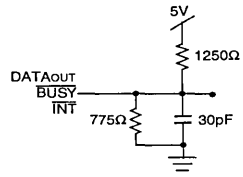
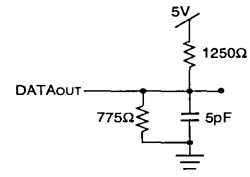


Figure 1. AC Output Test Load



2738 drw 06

Figure 2. Output Load
(For tLZ, tHZ, tWZ, tOW)
Including scope and jig

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

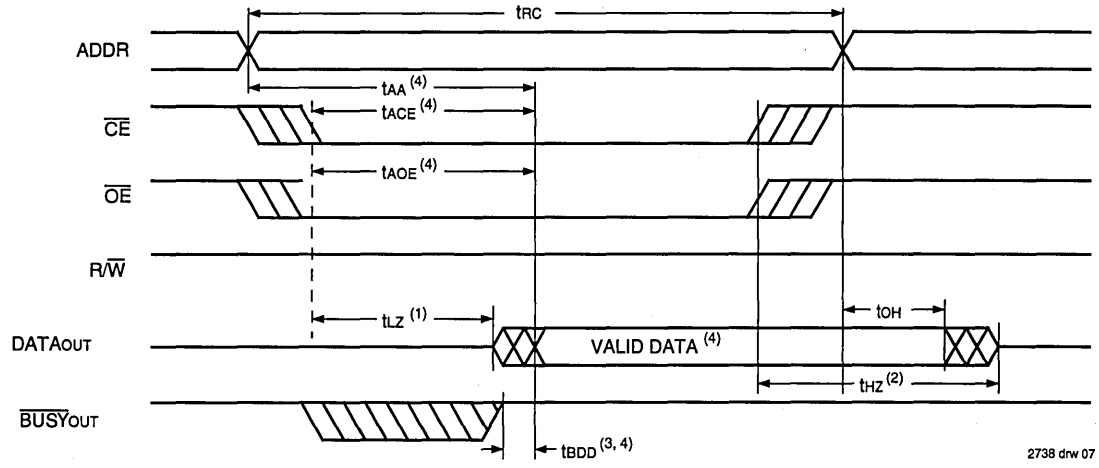
Symbol	Parameter	IDT7005X17 Com'l Only Min.	IDT7005X17 Com'l Only Max.	IDT7005X20 Com'l Only Min.	IDT7005X20 Com'l Only Max.	IDT7005X25 Min.	IDT7005X25 Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	17	—	20	—	25	—	ns
tAA	Address Access Time	—	17	—	20	—	25	ns
tACE	Chip Enable Access Time[3]	—	17	—	20	—	25	ns
tAOE	Output Enable Access Time	—	10	—	12	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time[1, 2]	3	—	3	—	3	—	ns
tHZ	Output High-Z Time[1, 2]	—	10	—	12	—	15	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	17	—	20	—	25	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	10	—	ns
tSAA	Semaphore Address Access Time	—	17	—	20	—	25	ns

Symbol	Parameter	IDT7005X35 Min.	IDT7005X35 Max.	IDT7005X55 Min.	IDT7005X55 Max.	IDT7005X70 MIL ONLY Min.	IDT7005X70 MIL ONLY Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	35	—	55	—	70	—	ns
tAA	Address Access Time	—	35	—	55	—	70	ns
tACE	Chip Enable Access Time[3]	—	35	—	55	—	70	ns
tAOE	Output Enable Access Time	—	20	—	30	—	35	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time[1, 2]	3	—	3	—	3	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	35	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns
tSAA	Semaphore Address Access Time	—	35	—	55	—	70	ns

2738 tbl 13

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIN and $\overline{SEM}$ = VIL.
4. 'X' in part numbers indicates power rating (S or L).

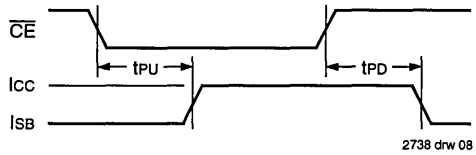
WAVEFORM OF READ CYCLES[5]



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$ or $\overline{OE}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

6

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE [5]

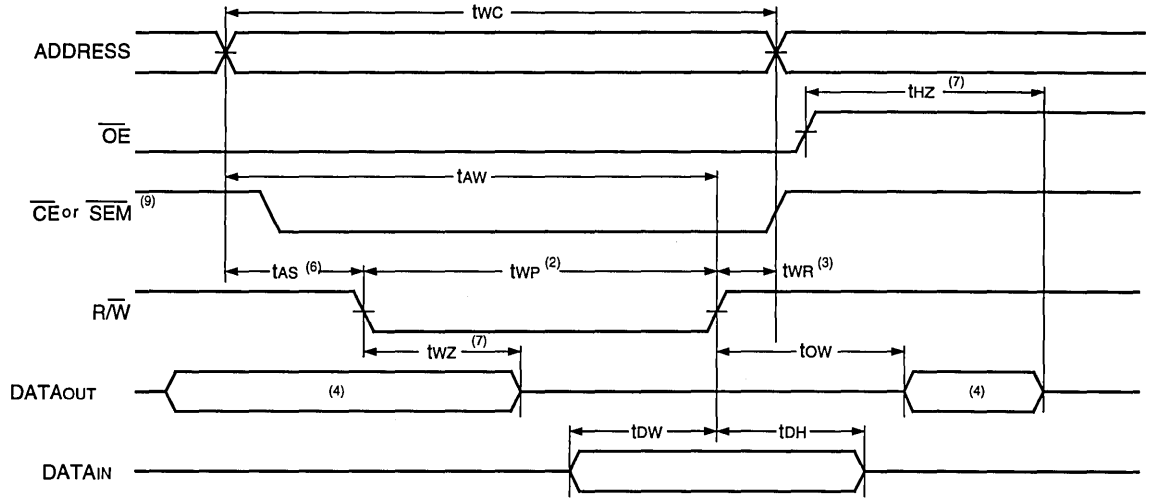
Symbol	Parameter	IDT7005X17 Com'l Only Min.	IDT7005X17 Com'l Only Max.	IDT7005X20 Com'l Only Min.	IDT7005X20 Com'l Only Max.	IDT7005X25 Min.	IDT7005X25 Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time	17	—	20	—	25	—	ns
tEW	Chip Enable to End-of-Write[3]	12	—	15	—	20	—	ns
tAW	Address Valid to End-of-Write	12	—	15	—	20	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	10	—	15	—	15	—	ns
tHZ	Output High-Z Time[1, 2]	—	10	—	12	—	15	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	10	—	12	—	15	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

Symbol	Parameter	IDT7005X35 Max	IDT7005X35 Min.	IDT7005X55 Max.	IDT7005X55 Min	IDT7005X70 MIL. Only Max	IDT7005X70 MIL. Only Min	Unit
WRITE CYCLE								
tWC	Write Cycle Time	35	—	55	—	70	—	ns
tEW	Chip Enable to End-of-Write[3]	30	—	45	—	50	—	ns
tAW	Address Valid to End-of-Write	30	—	45	—	50	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	25	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	30	—	40	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	25	—	30	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	15	—	25	—	30	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

NOTES: 2738 tbl 14

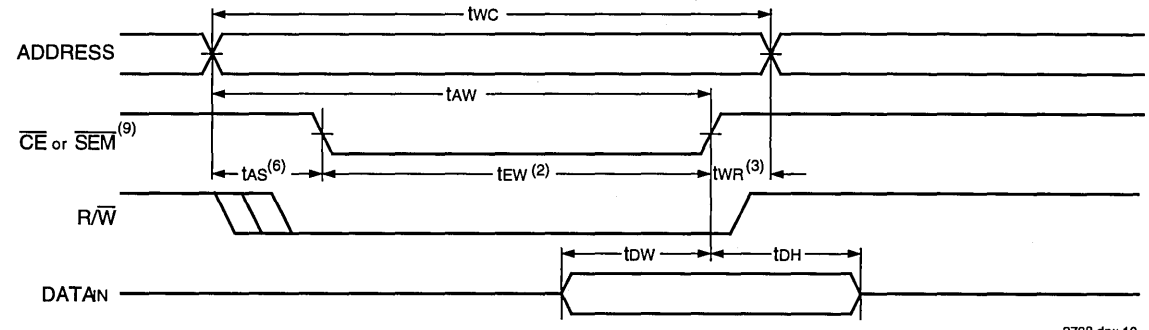
1. Transition is measured ±500mV from low or high impedance voltage with load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. 'X' in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,5,8)



2738 drw 09

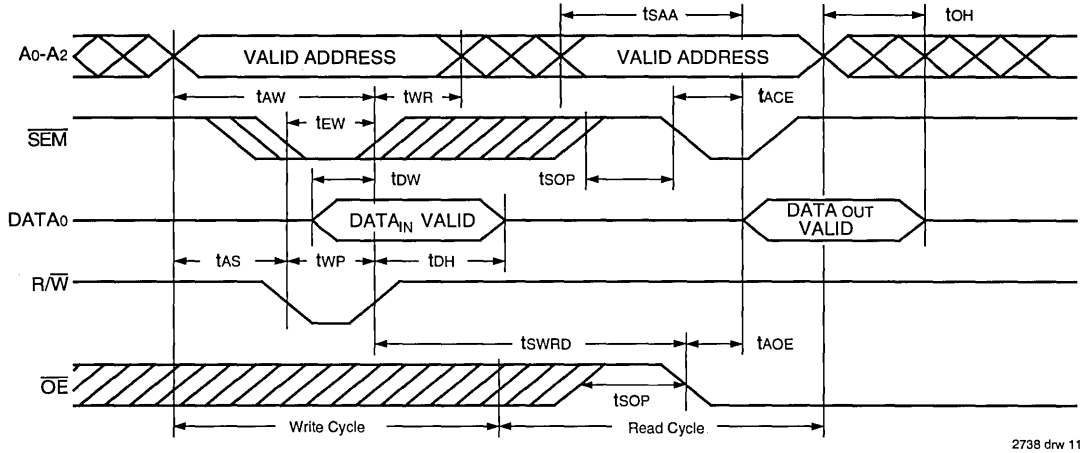
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,5)



2738 drw 10

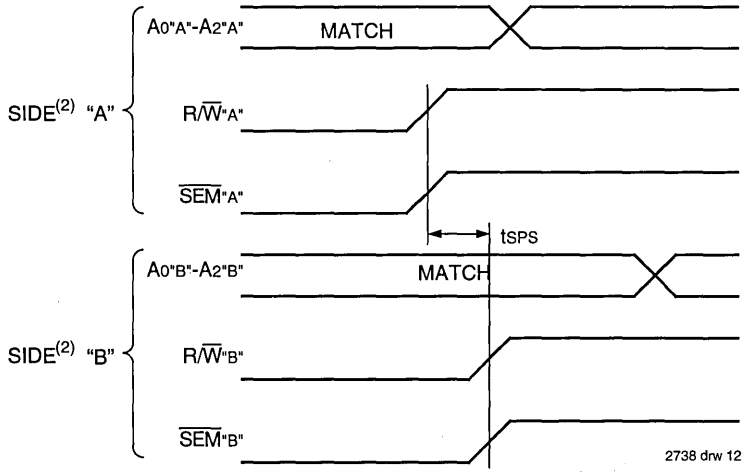
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured +/- 500mv from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. tEW must be met for either condition.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}_R$ = $\overline{CE}_L$ = VIH.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}_A$ or $\overline{SEM}_A$ going High to R/$\overline{W}_B$ or $\overline{SEM}_B$ going High.
4. If tSPS is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

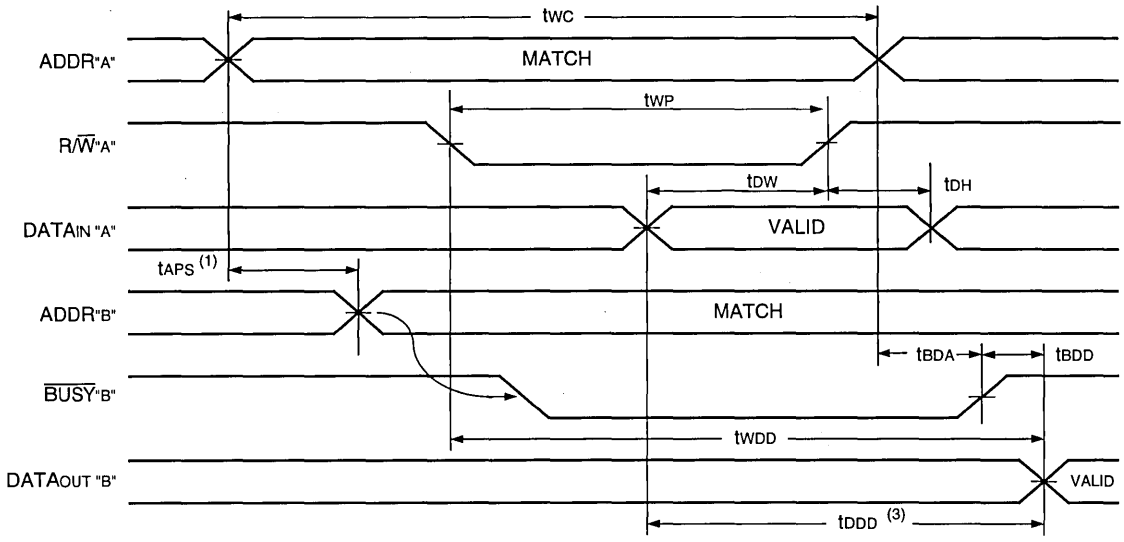
Symbol	Parameter	IDT7005X17 Com'l Only Min.	IDT7005X17 Com'l Only Max.	IDT7005X20 Com'l Only Min.	IDT7005X20 Com'l Only Max.	IDT7005X25 Min.	IDT7005X25 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	17	—	20	—	20	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	17	—	20	—	20	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable	—	17	—	20	—	20	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable	—	17	—	17	—	17	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	17	—	20	—	25	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	13	—	15	—	17	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	30	—	45	—	50	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	25	—	35	—	35	ns

Symbol	Parameter	IDT7005X35 Min.	IDT7005X35 Max.	IDT7005X55 Min.	IDT7005X55 Max.	IDT7005X70 MIL. ONLY Min.	IDT7005X70 MIL. ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	20	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	40	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	35	—	35	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	35	—	55	—	70	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	60	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	45	—	65	—	80	ns

2738 tbl 15

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention with port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. "X" in part numbers indicates power rating (S or L).

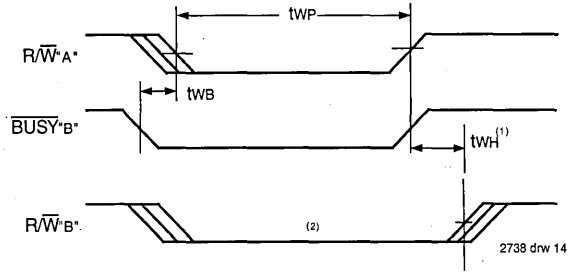
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ WITH $\overline{BUSY}$ (2,5) (M/S = V_{IH})



2738 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for for M/$\overline{S}$ = VIL (slave).
2. $\overline{CE}_L$ = $\overline{CE}_R$ = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. If M/$\overline{S}$ = VIL (slave), then $\overline{BUSY}$ is an input ($\overline{BUSY}$"A" =VIH), and $\overline{BUSY}$"B" = "don't care", for this example.
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite port "A".

TIMING WAVEFORM OF WITH WRITE $\overline{BUSY}$

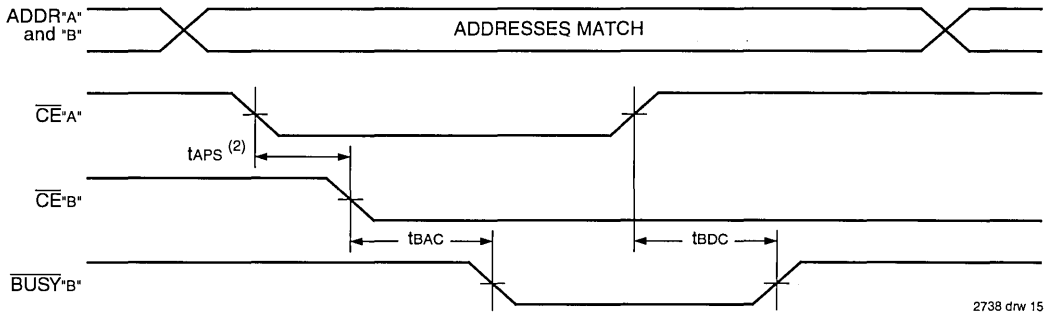


2738 drw 14

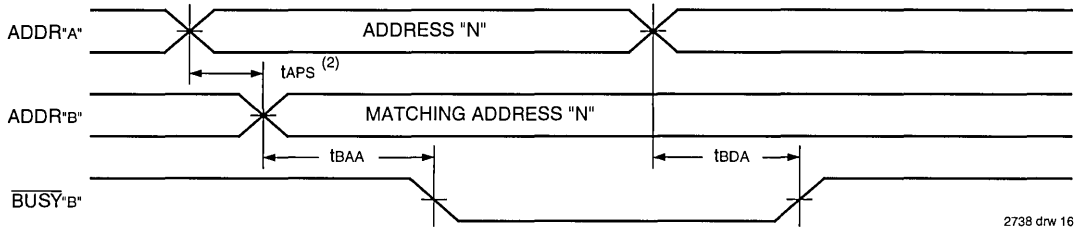
NOTE:

1. tWH must be met for both $\overline{BUSY}$ input (slave) and output (master).
2. $\overline{BUSY}$ is asserted on Port "B" Blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes High.

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1) (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)(M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1)

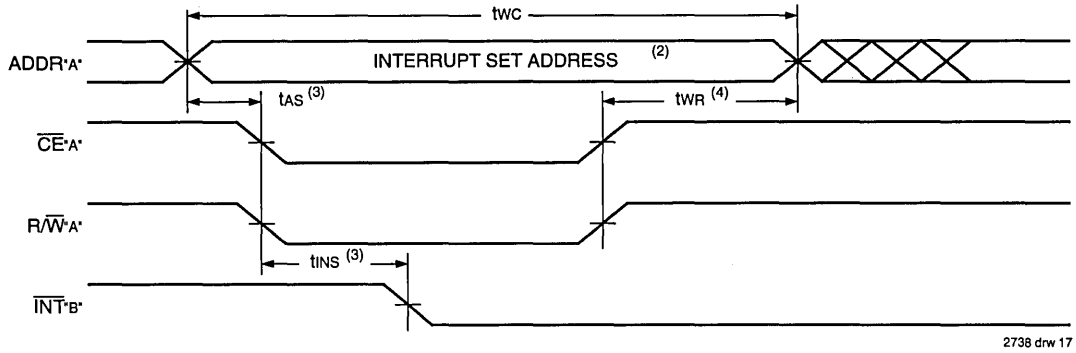
Symbol	Parameter	IDT7005X17 Com'l Only Min.	IDT7005X17 Com'l Only Max.	IDT7005X20 Com'l Only Min.	IDT7005X20 Com'l Only Max.	IDT7005X25 Min.	IDT7005X25 Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	15	—	20	—	20	ns
tINR	Interrupt Reset Time	—	15	—	20	—	20	ns

Symbol	Parameter	IDT7005X35 Min.	IDT7005X35 Max.	IDT7005X55 Min.	IDT7005X55 Max.	IDT7005X70 MIL. ONLY Min.	IDT7005X70 MIL. ONLY Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	40	—	50	ns
tINR	Interrupt Reset Time	—	25	—	40	—	50	ns

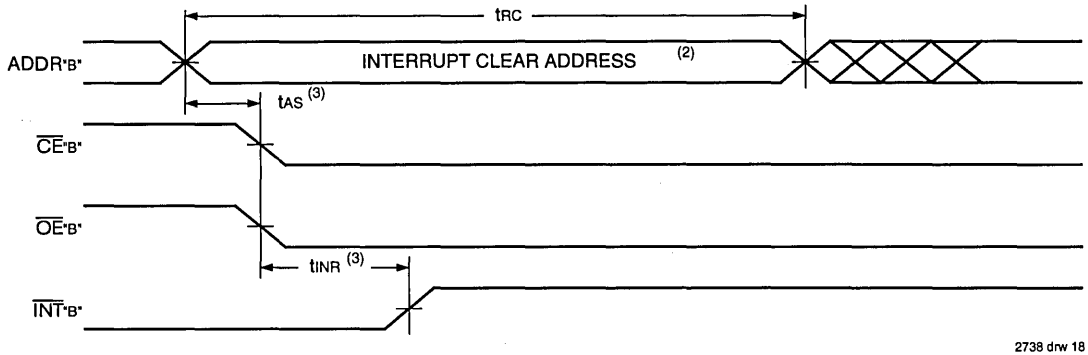
NOTE:
1. "X" in part numbers indicates power rating (S or L).

2738 tbl 16

WAVEFORM OF INTERRUPT TIMING[1]



2738 drw 17



2738 drw 18

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{12L}-A_{0L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{12R}-A_{0R}	$\overline{INT}_R$	Function
L	L	X	1FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	1FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	1FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	1FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2738 tbl 17

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$.
2. If $\overline{BUSY}_L = V_{IL}$, then no change.
3. If $\overline{BUSY}_R = V_{IL}$, then no change.

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{12L} A_{0R}-A_{12R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

2738 tbl 18

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$x outputs on the IDT7005 are push-pull, not open drain outputs. On slaves the $\overline{BUSY}$x input internally inhibits writes.
2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_7 Left	D_0 - D_7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

2738 tbl 19

NOTE:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7005.

FUNCTIONAL DESCRIPTION

The IDT7005 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7005 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 1FFE (HEX), where a write is defined as $\overline{CE}$ = R/$\overline{W}$= V_{IL} per the Truth Table. The left port clears the interrupt through access of address location 1FFE when $\overline{CE}$ = $\overline{OE}$ = V_{IL}. For this example, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 1FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 1FFF. The message (8 bits) at 1FFE or 1FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all

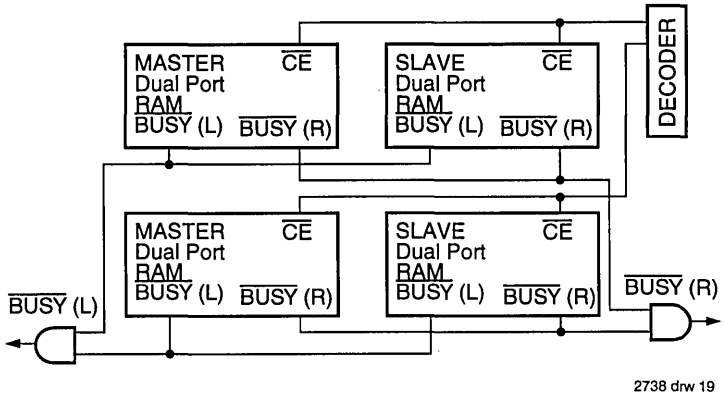


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7005 RAMs.

applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 7005 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7005 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7005 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with the R/$\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7005 is an extremely fast Dual-Port 8K x 8 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7005 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7005's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the

maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7005 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7005 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming

6

technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7005's Dual-Port RAM. Say the 8K x 8 RAM was to be divided into two 4K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

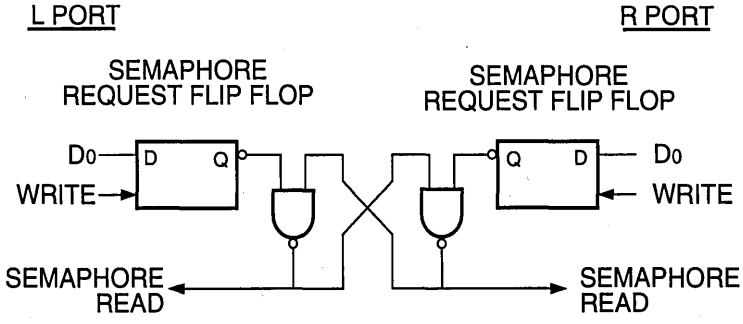
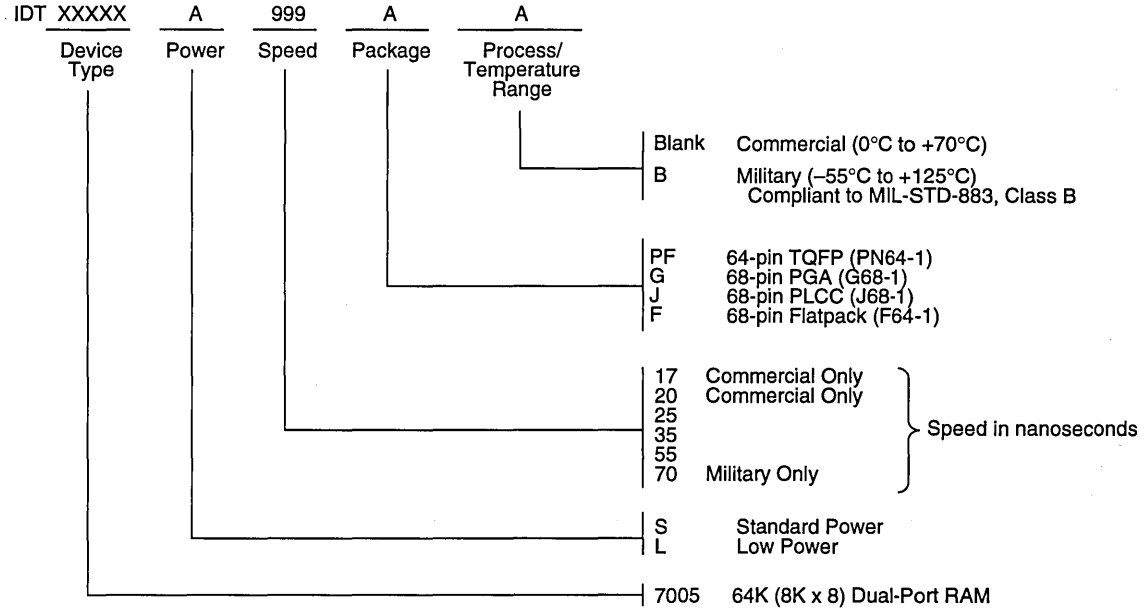


Figure 4. IDT7005 Semaphore Logic

2738 drw 20

ORDERING INFORMATION



2738 drw 21

6

Integrated Device Technology, Inc.

HIGH-SPEED 16K x 8 DUAL-PORT STATIC RAM

IDT7006S/L

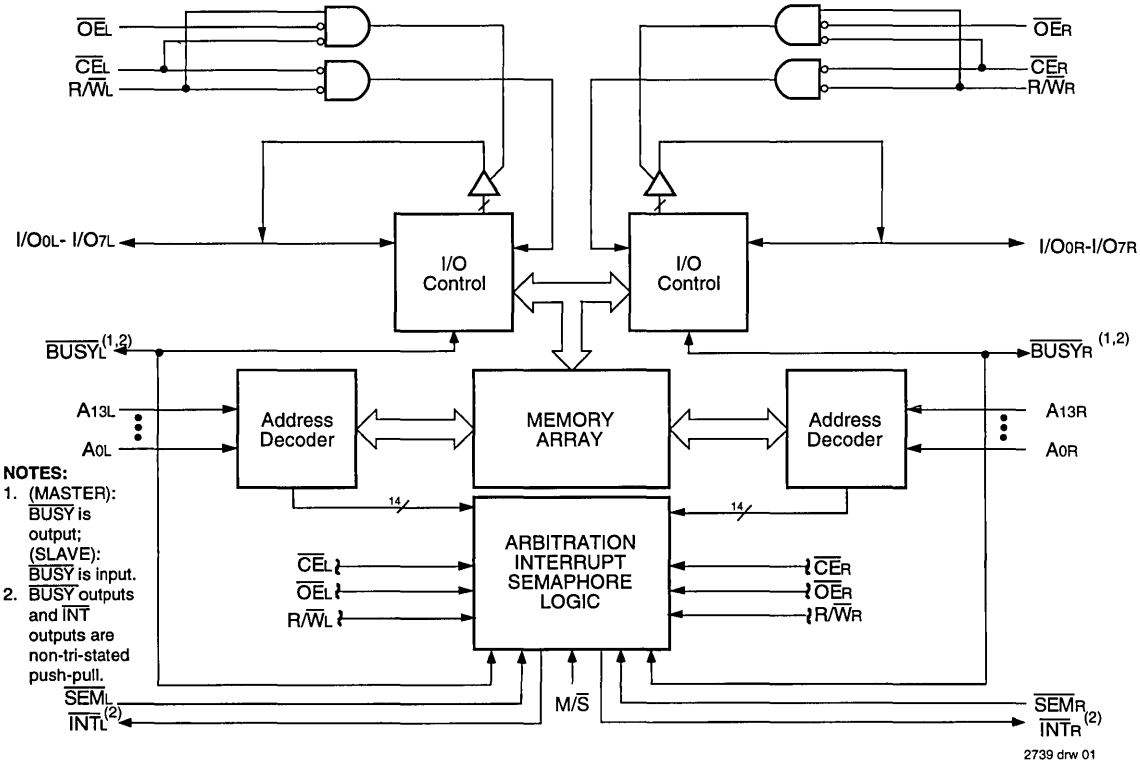
FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 25/35/55/70ns (max.)
  - — Commercial: 17/20/25/35/55ns (max.)
- Low-power operation
  - — IDT7006S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7006L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- IDT7006 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master, M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Devices are capable of withstanding greater than 2001V electrostatic discharge
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Available in 68-pin PGA, quad flatpack, PLCC, and a 64-pin TQFP
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7006 is a high-speed 16K x 8 Dual-Port Static

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.

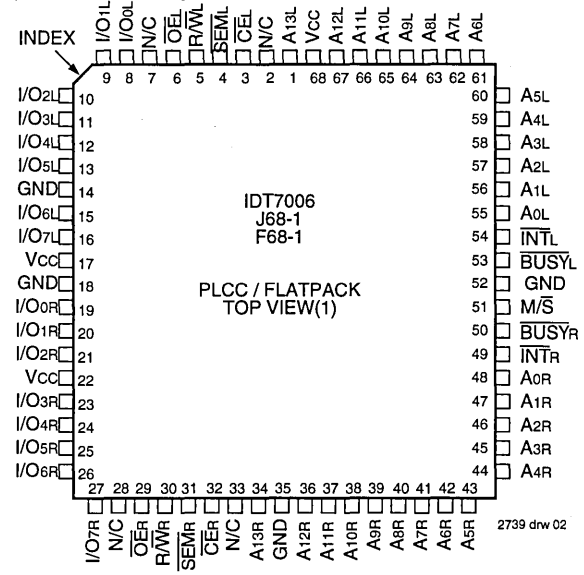
RAM. The IDT7006 is designed to be used as a stand-alone 128K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

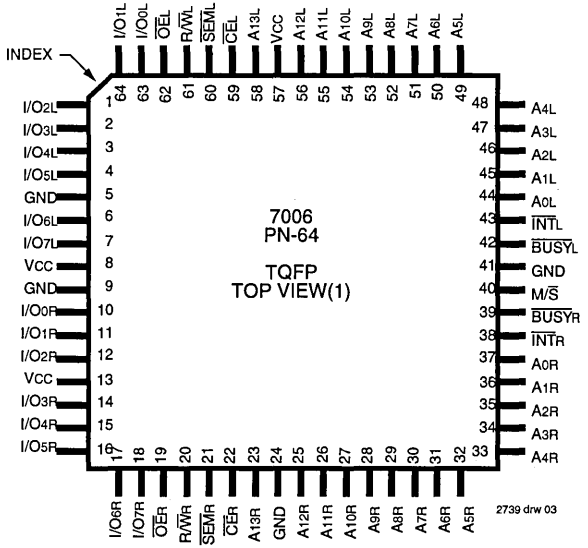
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500µW from a 2V battery.

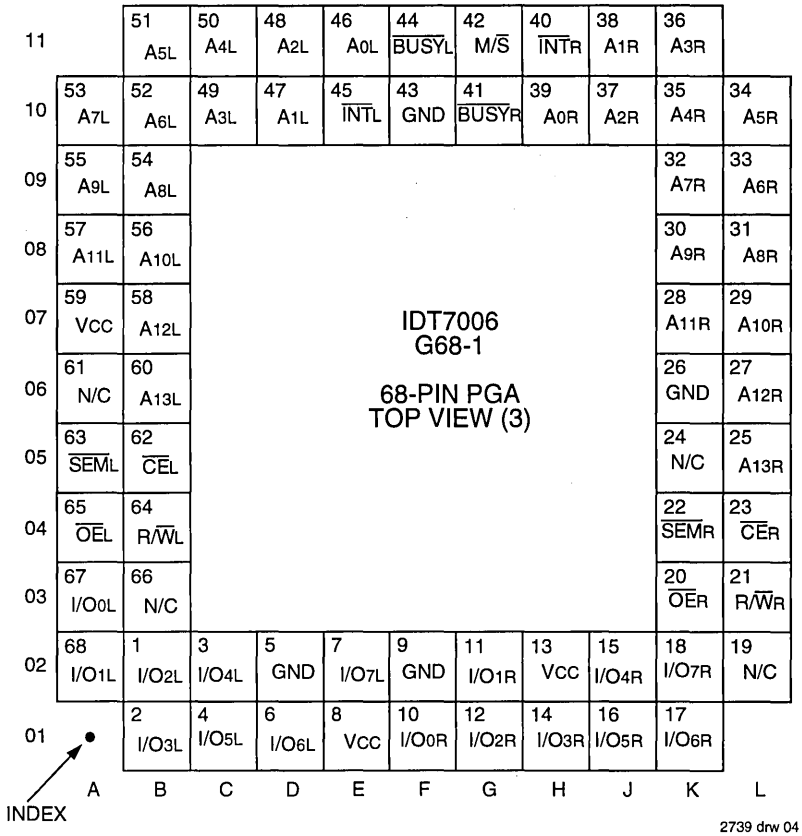
The IDT7006 is packaged in a ceramic 68-pin PGA, an 68-pin quad flatpack, a PLCC, and a 64-pin thin plastic quad flatpack, TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS





NOTE:
1. This text is does not indicate the actual part-marking



2739 drw 04

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{13L}$	$A_{0R} - A_{13R}$	Address
$I/O_{0L} - I/O_{7L}$	$I/O_{0R} - I/O_{7R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2739 tbl 01

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	X	X	H	High-Z	Deselected: Power-Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read Memory
X	X	H	X	High-Z	Outputs Disabled

NOTE: 2739 tbl 02
1. A_{0L} — A_{13L} is not equal to A_{0R} — A_{13R}

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag Data Out
H	↑	X	L	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	—	Not Allowed

2739 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTES: 2739 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \leq$ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2739 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTES: 2739 tbl 06
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

NOTE: 2739 tbl 07
1. This parameter is determined by device characterization, but is not production tested (TQFP Package Only).
2. 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7006S		IDT7006L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2739 tbl 08

NOTE:
1. At Vcc = 2.0V input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7006X17 Com'l Only		7006X20 Com'l Only		7006X25		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	—	—	155	340	mA
				L	—	—	—	—	155	280	
			COM'L.	S	170	310	160	290	155	265	
				L	170	260	160	240	155	220	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	—	—	16	80	mA
				L	—	—	—	—	16	65	
			COM'L.	S	25	60	20	60	16	60	
				L	25	50	20	50	16	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A"=V_{IL} and $\overline{CE}$"B"=V_{IH}[5] Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{IH}	MIL.	S	—	—	—	—	90	215	mA
				L	—	—	—	—	80	180	
			COM'L.	S	105	190	95	180	90	170	
				L	105	160	95	150	90	140	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	MIL.	S	—	—	—	—	1.0	30	mA
				L	—	—	—	—	0.2	10	
			COM'L.	S	1.0	15	1.0	15	1.0	15	
				L	0.2	5	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{CC} - 0.2V [5] $\overline{SEM}_R$ = $\overline{SEM}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	—	—	85	200	mA
				L	—	—	—	—	85	170	
			COM'L.	S	100	170	90	155	85	145	
				L	100	140	90	130	85	120	

NOTES:
2739 tbl 09

1. 'X' in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. ICC DC =120mA (TYP)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or comtrol lines change.
5. Port "A" may be either left of right port. Port "B" is the opposite from port "A".

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7006X35 Typ.[2]	7006X35 Max.	7006X55 Typ.[2]	7006X55 Max.	7006X70 MIL ONLY Typ.[2]	7006X70 MIL ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open, $\overline{SEM}$ = V_{IH}, f = f_{MAX}[3]	MIL.	S	150	300	150	300	140	300	mA
				L	150	250	150	250	140	250	
			COM'L.	S	150	250	150	250	—	—	
				L	150	210	150	210	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE_L}$ = $\overline{CE_R}$ = V_{IH}, $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH}, f = f_{MAX}[3]	MIL.	S	13	80	13	80	10	80	mA
				L	13	65	13	65	10	65	
			COM'L.	S	13	60	13	60	—	—	
				L	13	50	13	50	—	—	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A"=V_{IL} and $\overline{CE}$"B"=V_{IH}[5], Active Port Outputs Open, f = f_{MAX}[3], $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH}	MIL.	S	85	190	85	190	80	190	mA
				L	85	160	85	160	80	160	
			COM'L.	S	85	155	85	155	—	—	
				L	85	130	85	130	—	—	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs) $\overline{SEM_R}$ = $\overline{SEM_L}$ ≥ Vcc - 0.2V	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ Vcc - 0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ 0.2V, f = 0[4]	MIL.	S	1.0	30	1.0	30	1.0	30	mA
				L	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	—	—	
				L	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ Vcc - 0.2V[5], $\overline{SEM_R}$ = $\overline{SEM_L}$ ≥ Vcc - 0.2V	MIL.	S	80	175	80	175	75	175	mA
				L	80	150	80	150	75	150	
		V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ 0.2V	COM'L.	S	80	135	80	135	—	—	
		Active Port Outputs Open, f = f_{MAX}[3]		L	80	110	80	110	—	—	

NOTES:
1. 'X' in part numbers indicates power rating (S or L)
2. Vcc = 5V, TA = +25°C, and are not production tested. $I_{CC\ DC}$ =120ma (TYP)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or comtrol lines change.
5. Port "A" may be either left or right port. Port "B"is the opposite from port "A".

2739 tbl 10

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

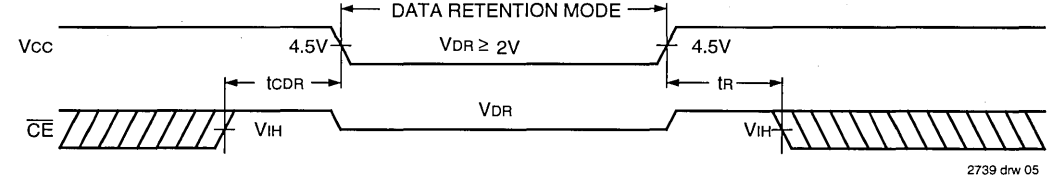
(V_{LC} = 0.2V, V_{HC} = Vcc - 0.2V)[4]

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	Vcc for Data Retention	Vcc = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ ≥ V_{HC}	MIL.	—	100	4000	µA
		V_{IN} ≥ V_{HC} or ≤ V_{LC}	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time	$\overline{SEM}$ ≥ V_{HC}		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. TA = +25°C, Vcc = 2V, and are not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.
4. At Vcc = 2V input leakages are undefined

2739 tbl 11

DATA RETENTION WAVEFORM



2739 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2739 tbl 12

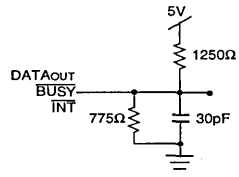
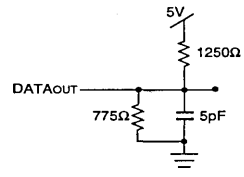


Figure 1. AC Output Test Load



2739 drw 06

Figure 2. Output Load (5pF for tLZ, tHZ, twz, tow) Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

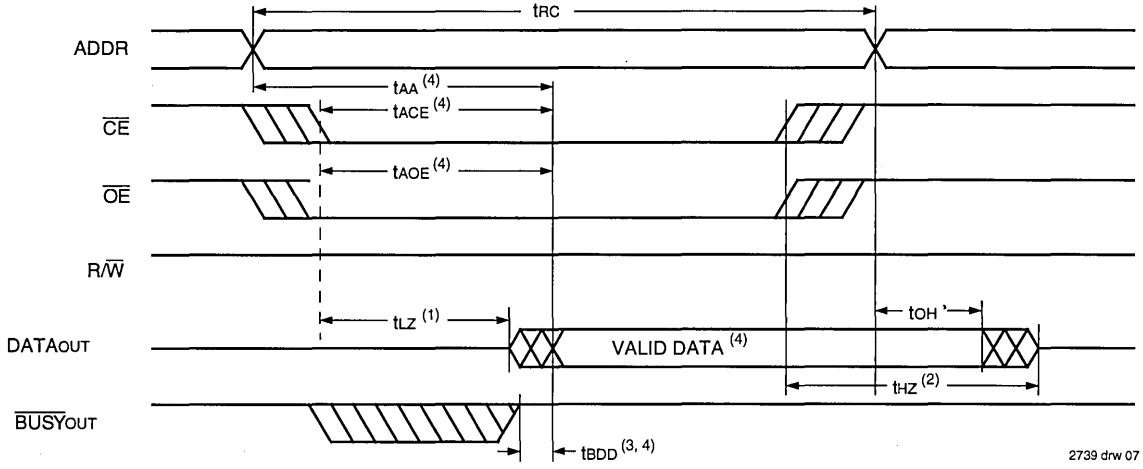
Symbol	Parameter	IDT7006X17 Com'l Only Min.	IDT7006X17 Com'l Only Max.	IDT7006X20 Com'l Only Min.	IDT7006X20 Com'l Only Max.	IDT7006X25 Min.	IDT7006X25 Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	17	—	20	—	25	—	ns
tAA	Address Access Time	—	17	—	20	—	25	ns
tACE	Chip Enable Access Time[3]	—	17	—	20	—	25	ns
tAOE	Output Enable Access Time	—	10	—	12	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time[1, 2]	3	—	3	—	3	—	ns
tHZ	Output High-Z Time[1, 2]	—	10	—	12	—	15	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	17	—	20	—	25	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	10	—	ns
tSAA	Semaphore Address Access Time	—	17	—	20	—	25	ns

Symbol	Parameter	IDT7006X35 Min.	IDT7006X35 Max.	IDT7006X55 Min.	IDT7006X55 Max.	IDT7006X70 MIL ONLY Min.	IDT7006X70 MIL ONLY Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	35	—	55	—	70	—	ns
tAA	Address Access Time	—	35	—	55	—	70	ns
tACE	Chip Enable Access Time[3]	—	35	—	55	—	70	ns
tAOE	Output Enable Access Time	—	20	—	30	—	35	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time[1, 2]	3	—	3	—	3	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	35	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns
tSAA	Semaphore Address Access Time	—	35	—	55	—	70	ns

2739 tbl 13

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL
4. 'X' in part numbers indicates power rating (S or L).

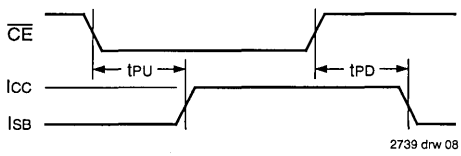
WAVEFORM OF READ CYCLES[5]



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$ or $\overline{OE}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations BUSY has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

6

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[5]

Symbol	Parameter	IDT7006X17 Com'l Only		IDT7006X20 Com'l Only		IDT7006X25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	17	—	20	—	25	—	ns
tEW	Chip Enable to End-of-Write[3]	12	—	15	—	20	—	ns
tAW	Address Valid to End-of-Write	12	—	15	—	20	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	10	—	15	—	15	—	ns
tHZ	Output High-Z Time[1, 2]	—	10	—	12	—	15	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	10	—	12	—	15	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

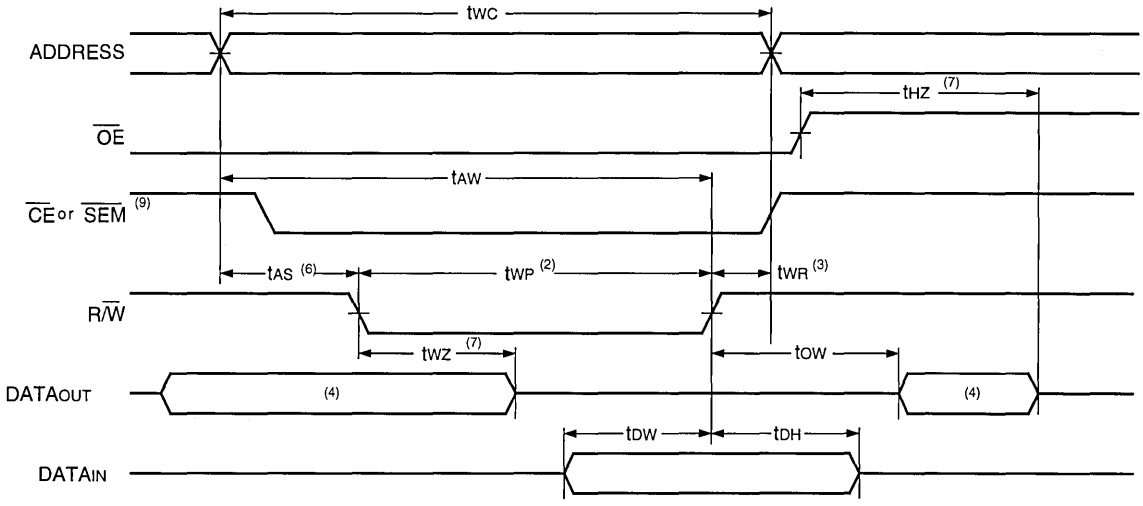
Symbol	Parameter	IDT7006X35		IDT7006X55		IDT7006X70 MIL. ONLY		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	35	—	55	—	70	—	ns
tEW	Chip Enable to End-of-Write[3]	30	—	45	—	50	—	ns
tAW	Address Valid to End-of-Write	30	—	45	—	50	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	25	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	30	—	40	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	25	—	30	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	15	—	25	—	30	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

NOTES:

2739 tbl 14

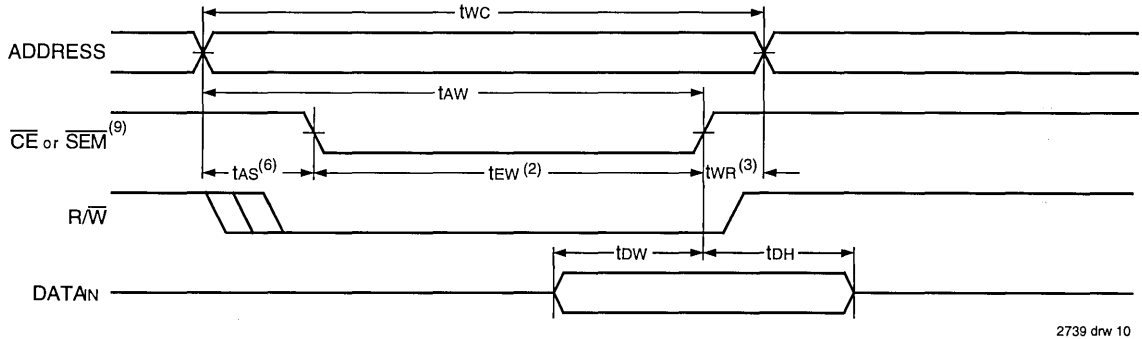
1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 2).
2. This parameter is guaranteed by device characterization, but is not production tested but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. 'X' in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,5,8)



2739 drw 09

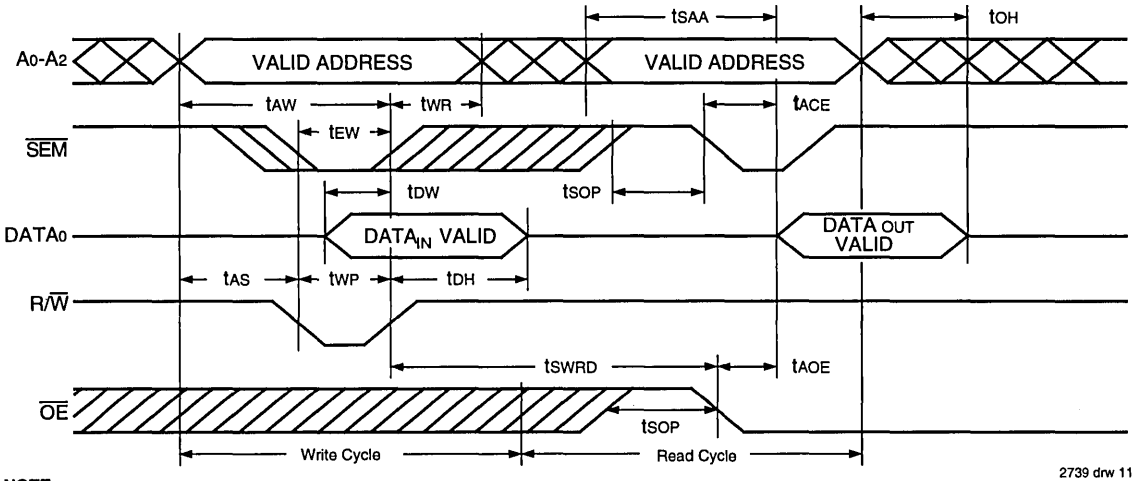
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,5)



2739 drw 10

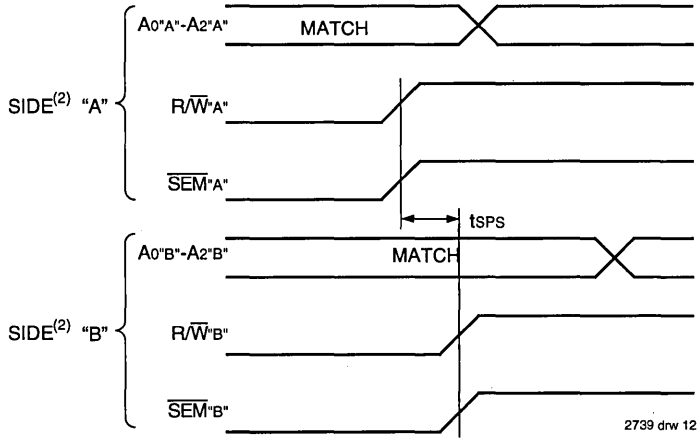
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured by +/- 500mV from steady state with the Output Test Load (Figure 2)
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. tEW must be met for either condition.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}_R$ = $\overline{CE}_L$ = VIH, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}$"A" or $\overline{SEM}$"A" going High to R/$\overline{W}$"B" or $\overline{SEM}$"B" going High.
4. If tSPS is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

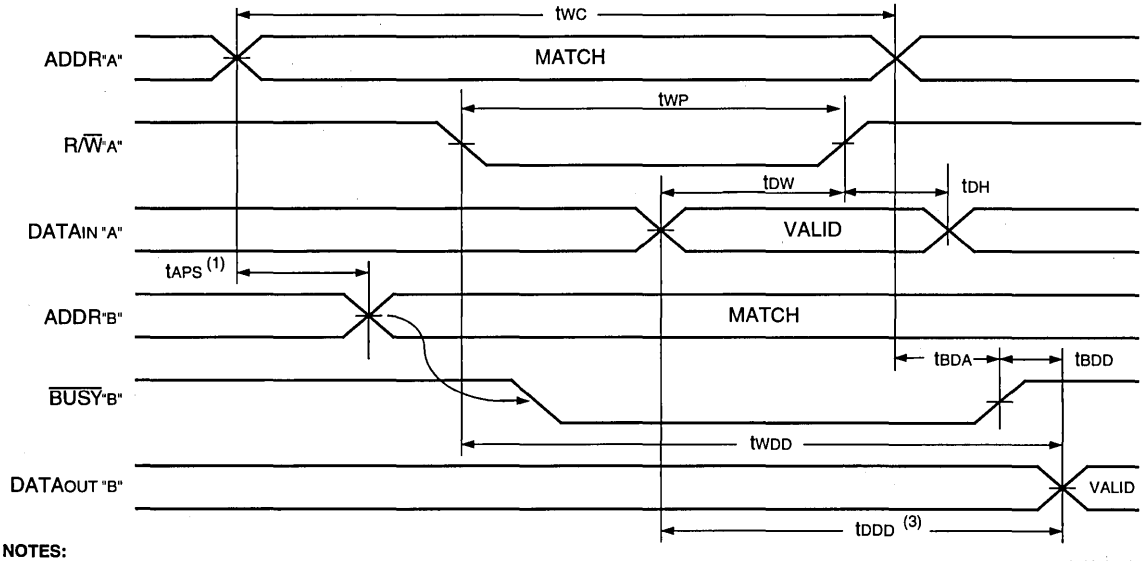
Symbol	Parameter	IDT7006X17 Com'l Only Min.	IDT7006X17 Com'l Only Max.	IDT7006X20 Com'l Only Min.	IDT7006X20 Com'l Only Max.	IDT7006X25 Min.	IDT7006X25 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	17	—	20	—	20	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	17	—	20	—	20	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	17	—	20	—	20	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	17	—	17	—	17	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	17	—	20	—	25	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	13	—	15	—	17	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	30	—	45	—	50	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	25	—	30	—	35	ns

Symbol	Parameter	IDT7006X35 Min.	IDT7006X35 Max.	IDT7006X55 Min.	IDT7006X55 Max.	IDT7006X70 MIL. ONLY Min.	IDT7006X70 MIL. ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	20	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	40	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	20	—	35	—	35	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	35	—	55	—	70	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	60	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	45	—	65	—	80	ns

NOTES: 2739 tbl 15

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited with port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention with port "A".
6. "X" is part numbers indicates power rating (S or L).

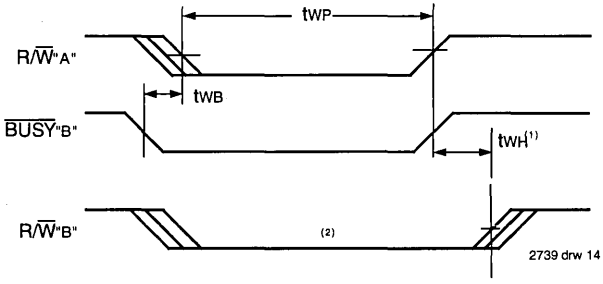
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}^{(2,5)}$ ($M/\overline{S}$ = V_{IH})



2739 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for $M/\overline{S}$ = VIL (SLAVE).
2. $\overline{CE}_L = \overline{CE}_R$ = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. If $M/\overline{S}$ = VIL(slave) then BUSY is input ($\overline{BUSY}$"A" = VIH and $\overline{BUSY}$"B" = "don't care", for this example.
5. All timing is the same for left and right port. Port "A' may be either left or right port. Port "B" is the port opposite from Port "A".

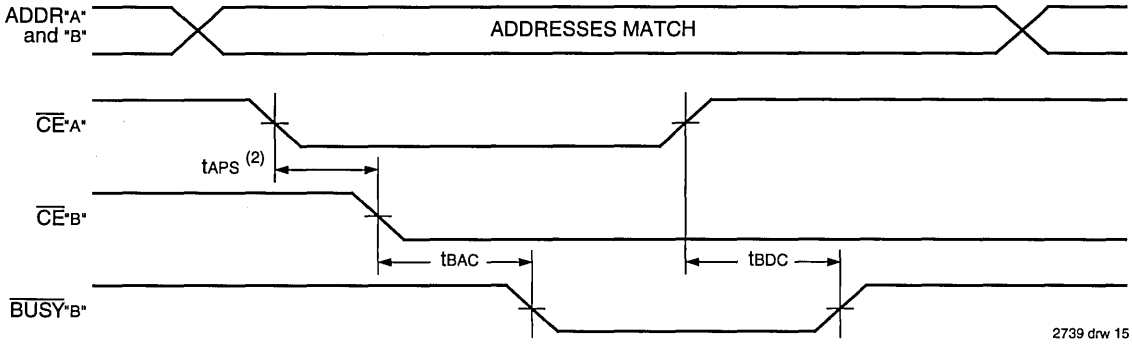
TIMING WAVEFORM OF WRITE WITH BUSY



2739 drw 14

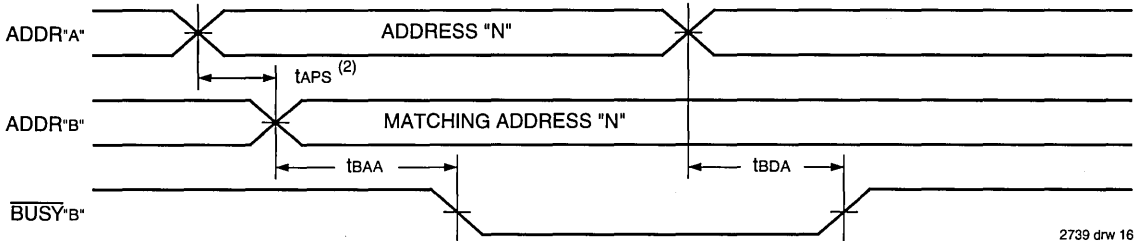
NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (slave) and output (master).
2. $\overline{BUSY}$ is asserted on Port "B" Blocking R/W"B", until $\overline{BUSY}$"B" goes High.

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1) (M/$\overline{S}$ = H)



2739 drw 15

WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)(M/$\overline{S}$ = H)



2739 drw 16

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1)

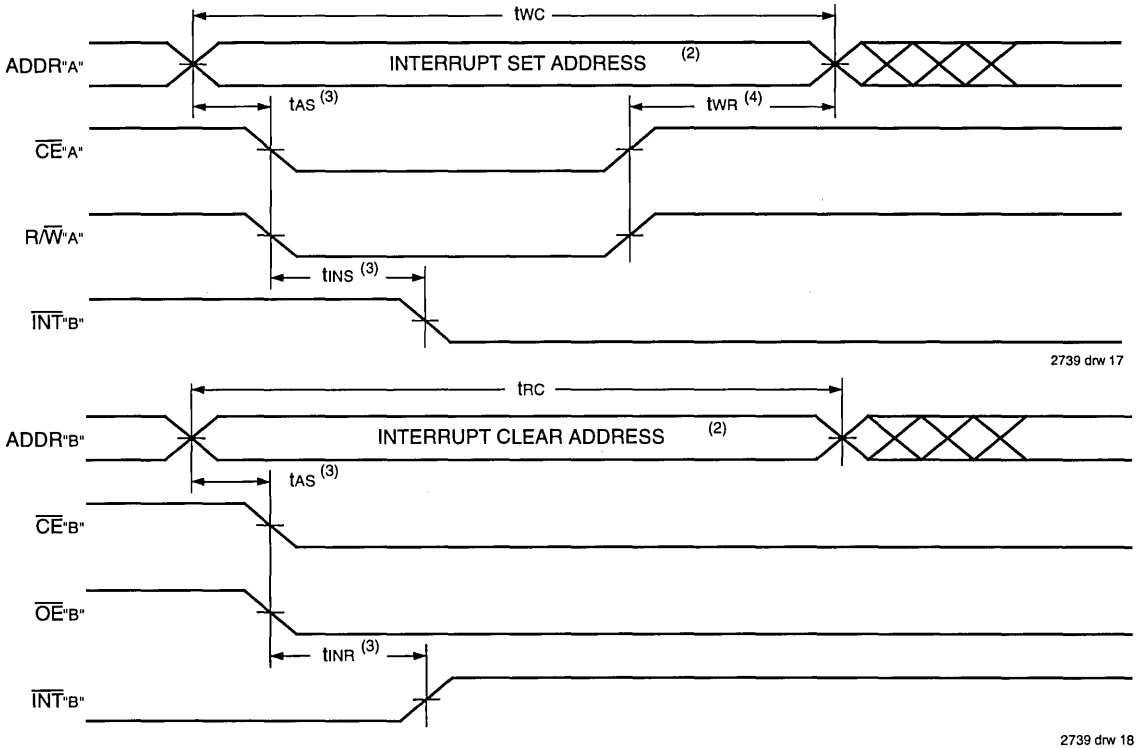
Symbol	Parameter	IDT7006X17 Com'l Only Min.	IDT7006X17 Com'l Only Max.	IDT7006X20 Com'l Only Min.	IDT7006X20 Com'l Only Max.	IDT7006X25 Min.	IDT7006X25 Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	15	—	20	—	20	ns
tINR	Interrupt Reset Time	—	15	—	20	—	20	ns

Symbol	Parameter	IDT7006X35 Min.	IDT7006X35 Max.	IDT7006X55 Min.	IDT7006X55 Max.	IDT7006X70 MIL. ONLY Min.	IDT7006X70 MIL. ONLY Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	40	—	50	ns
tINR	Interrupt Reset Time	—	25	—	40	—	50	ns

NOTE:
1. "X" in part numbers indicates power rating (S or L).

2739 tbl 16

WAVEFORM OF INTERRUPT TIMING(1)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG(1)

Left Port					Right Port					
R/$\overline{W}$L	$\overline{CE}$L	$\overline{OE}$L	A13L-A0L	$\overline{INT}$L	R/$\overline{W}$R	$\overline{CE}$R	$\overline{OE}$R	A13R-A0R	$\overline{INT}$R	Function
L	L	X	1FFF	X	X	X	X	X	L(2)	Set Right $\overline{INT}$R Flag
X	X	X	X	X	X	L	L	1FFF	H(3)	Reset Right $\overline{INT}$R Flag
X	X	X	X	L(3)	L	L	X	1FFE	X	Set Left $\overline{INT}$L Flag
X	L	L	1FFE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}$L Flag

NOTES:
1. Assumes $\overline{BUSY}$L = $\overline{BUSY}$R = VIH.
2. If $\overline{BUSY}$L = VIL, then no change.
3. If $\overline{BUSY}$R = VIL, then no change.

2739 tbl 17

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE_L}$	$\overline{CE_R}$	A_{0L}-A_{13L} A_{0R}-A_{13R}	$\overline{BUSY_L}$(1)	$\overline{BUSY_R}$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

NOTES: 2739 tbl 18

1. Pins $\overline{BUSY_L}$ and $\overline{BUSY_R}$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$x outputs on the IDT7006 are push pull, not open drain outputs. On slaves the $\overline{BUSY}$x input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY_L}$ or $\overline{BUSY_R}$ = Low will result. $\overline{BUSY_L}$ and $\overline{BUSY_R}$ outputs cannot be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY_L}$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY_R}$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_7 Left	D_0 - D_7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2739 tbl 19

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7006.

FUNCTIONAL DESCRIPTION

The IDT7006 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7006 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT_L}$) is asserted when the right port writes to memory location 3FFE (HEX) where a write is defined as $\overline{CE} = R/\overline{W} = V_{IL}$ per the Truth Table. The left port clears the interrupt by reading address location 3FFE access when $CE_R = OE_R = V_{IL}$, $R/\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT_R}$) is asserted when the left port writes to memory location 3FFF (HEX) and to clear the interrupt flag ($\overline{INT_R}$), the right port must read the memory location 3FFF. The message (8 bits) at 3FFE or 3FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FFE and 3FFF are not used as mail boxes, but as part of the random access memory. Refer to Table 1 for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all

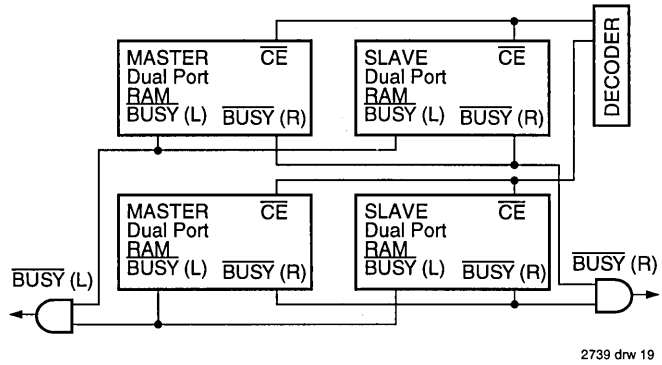


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7006 RAMs.

applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 7006 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7006 RAM array in width while using busy logic, one master part is used to decide which side of the RAMs array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7006 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with the R/$\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7006 is an extremely fast Dual-Port 16K x 8 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7006 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7006s hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources

to be allocated in varying configurations. The IDT7006 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7006 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a

6

resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7006's Dual-Port RAM. Say the 16K x 8 RAM was to be divided into two 8K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 8K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

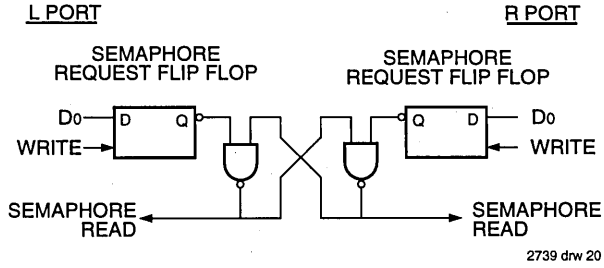
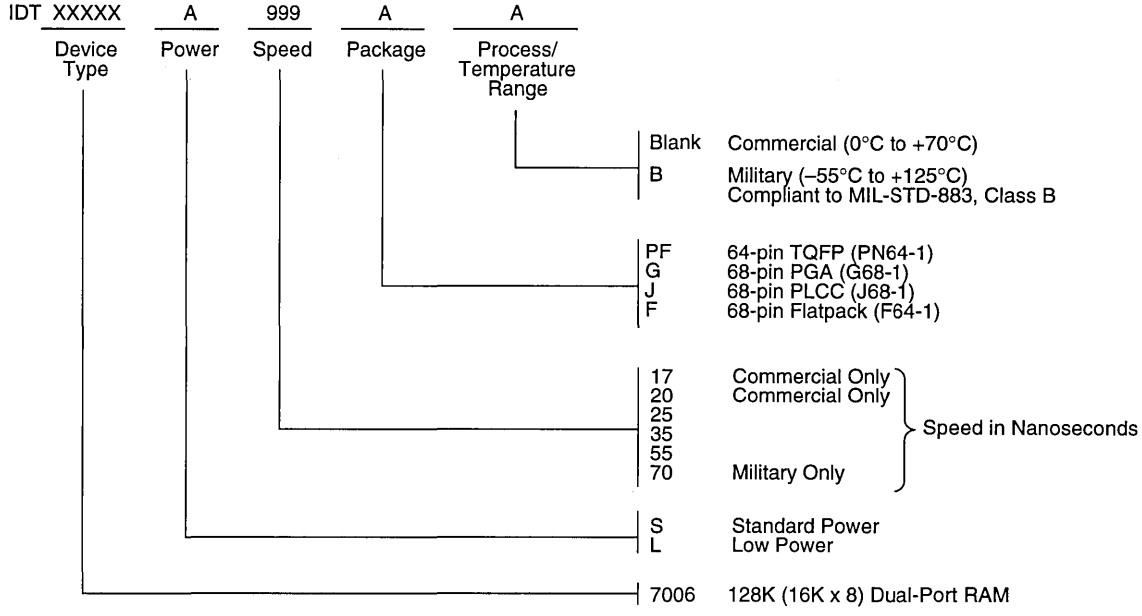


Figure 4. IDT7006 Semaphore Logic

ORDERING INFORMATION



2739 drw 21

6

Integrated Device Technology, Inc.

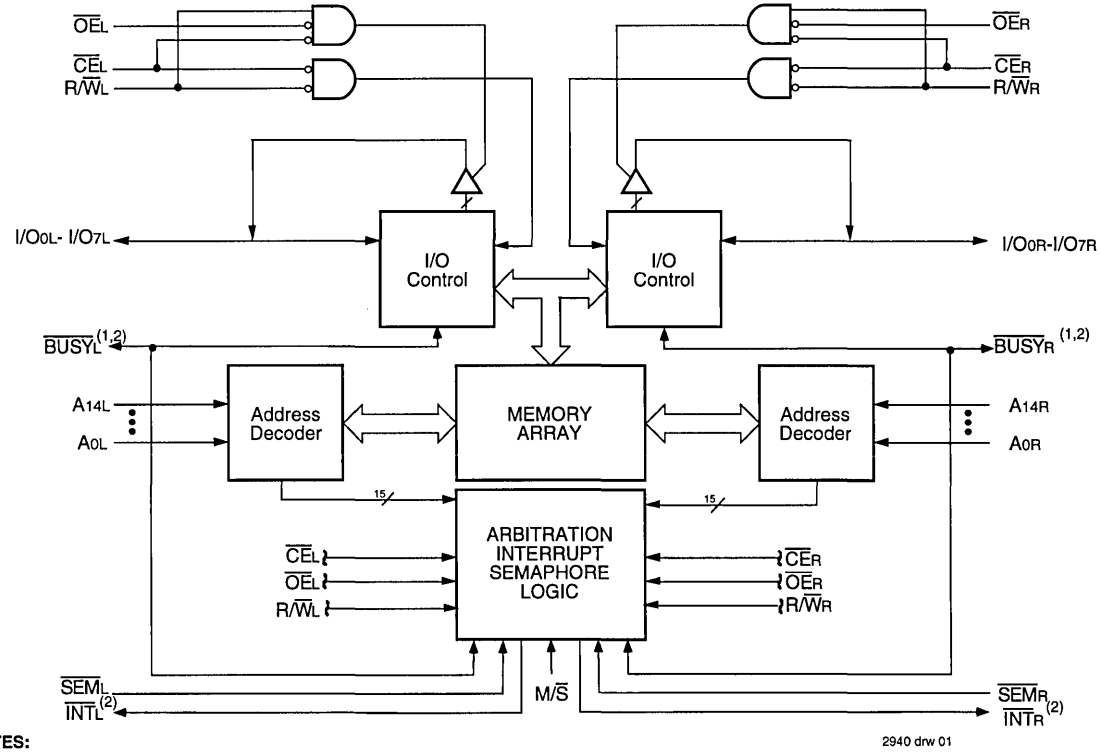
HIGH-SPEED 32K x 8 DUAL-PORT STATIC RAM

IDT7007S/L

FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 25/35/55ns (max.)
  - — Commercial: 20/25/35/55ns (max.)
- Low-power operation
  - — IDT7007S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7007L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- IDT7007 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master,
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Devices are capable of withstanding greater than 2001V electrostatic discharge
- TTL-compatible, single 5V (±10%) power supply
- Available in 68-pin PGA and PLCC and a 64-pin TQFP
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

FUNCTIONAL BLOCK DIAGRAM



2940 drw 01

NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ and $\overline{INT}$ outputs are non-tri-stated push-pull.

DESCRIPTION:

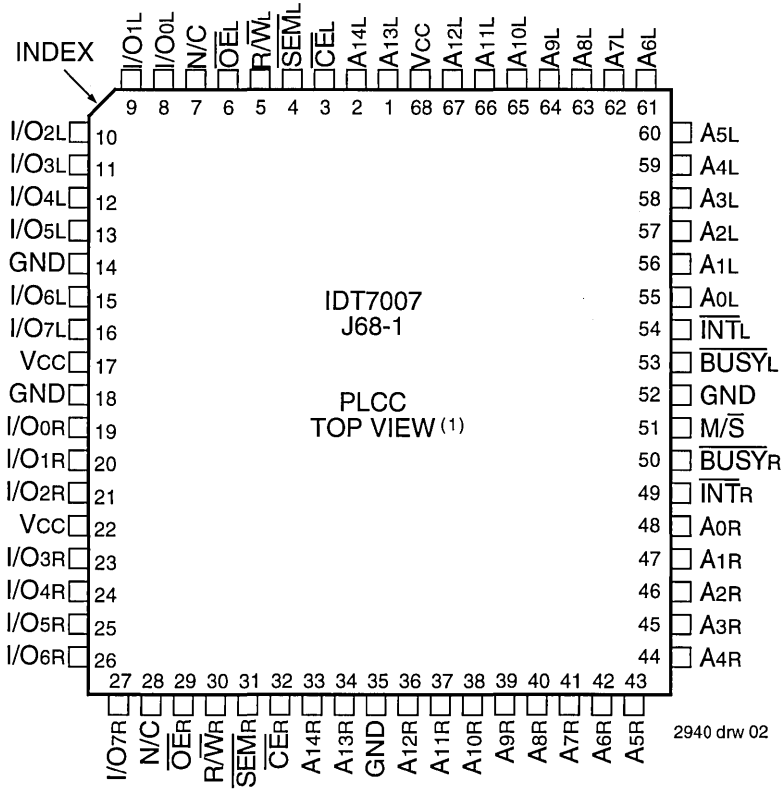
The IDT7007 is a high-speed 32K x 8 Dual-Port Static RAM. The IDT7007 is designed to be used as a stand-alone 256K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power.

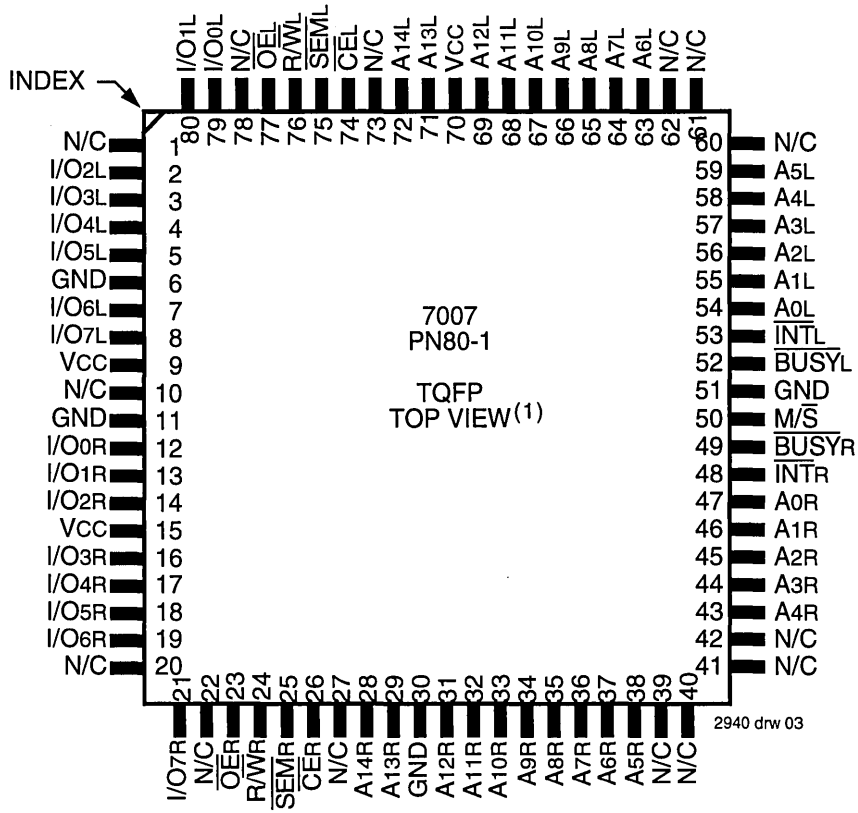
The IDT7007 is packaged in a 68-pin pin PGA, a 68-pin PLCC, and a 80-pin thin plastic quad flatpack, TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS

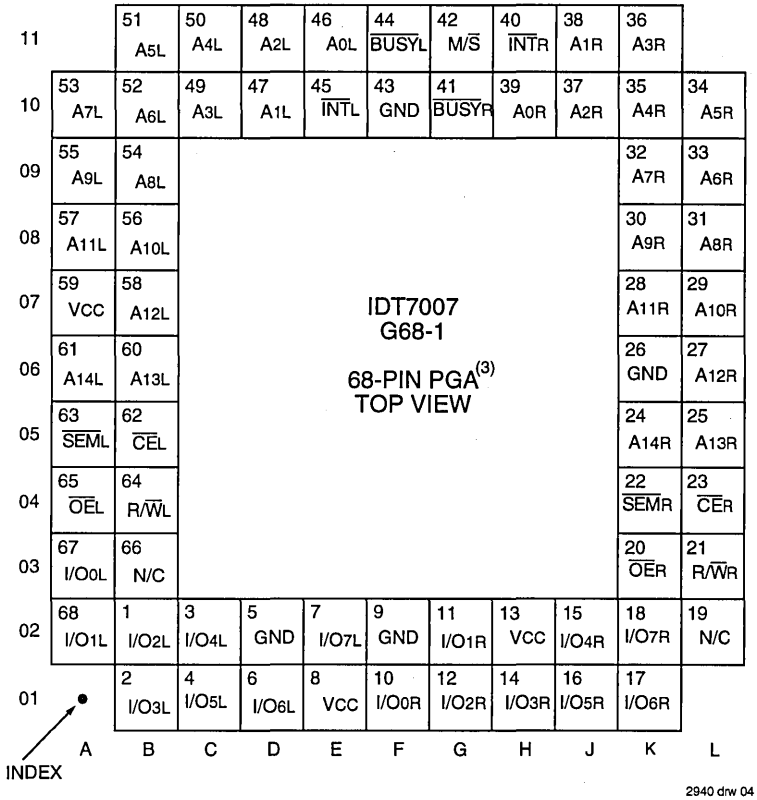


NOTE:
1. This text does not indicate orientation of the actual part marking.

PIN CONFIGURATIONS (Continued)



NOTE:
1. This text does not indicate orientation of the actual part-marking.



2940 drw 04

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{14L}$	$A_{0R} - A_{14R}$	Address
$I/O_{0L} - I/O_{7L}$	$I/O_{0R} - I/O_{7R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2940 tbl 01

NOTES:
1. All V_{CC} pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part marking.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	X	X	H	High-Z	Deselected: Power-Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read Memory
X	X	H	X	High-Z	Outputs Disabled

NOTE: 2940 tbl 02
1. $A_{0L} - A_{14L} \neq A_{0R} - A_{14R}$

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL[1]

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	H	L	L	DATAOUT	Read Semaphore Flag Data Out
H	↑	X	L	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	—	Not Allowed

2940 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2940 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq$ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2940 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTES: 2940 tbl 06
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

NOTE: 2940 tbl 07
1. This parameter is determined by device characterization but is not production tested. TQFP package only.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7007S		IDT7007L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = – 4mA	2.4	—	2.4	—	V

NOTE:

1. At V_{CC} = 2.0V, input leakages are undefined.

2940 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7007X20 COM'L ONLY Typ.[2]	7007X20 COM'L ONLY Max.	7007X25 Typ.[2]	7007X25 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	170	345	mA
				L	—	—	170	305	
			COM'L.	S	180	315	170	305	
				L	180	275	170	265	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	25	100	mA
				L	—	—	25	80	
			COM'L.	S	30	85	25	85	
				L	30	60	25	60	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	MIL.	S	—	—	105	230	mA
				L	—	—	105	200	
			COM'L.	S	115	210	105	200	
				L	115	180	105	170	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V	MIL.	S	—	—	1.0	30	mA
				L	—	—	0.2	10	
			COM'L.	S	1.0	15	1.0	15	
				L	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	100	200	mA
				L	—	—	100	175	
			COM'L.	S	110	185	100	170	
				L	110	160	100	145	

NOTES:

1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1 / t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

2940 tbl 09

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7007X35 Typ.[2]	7007X35 Max.	7007X55 Typ.[2]	7007X55 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	335	150	310	mA
				L	—	295	150	270	
			COM'L.	S	160	295	150	270	
				L	160	255	150	230	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	100	13	100	mA
				L	—	80	13	80	
			COM'L.	S	20	85	13	85	
				L	20	60	13	60	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	MIL.	S	—	215	85	195	mA
				L	—	185	85	165	
			COM'L.	S	95	185	85	165	
				L	95	155	85	135	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	MIL.	S	—	30	1.0	30	mA
				L	—	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	
				L	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{CC} - 0.2V[5] $\overline{CE}_R$ ≥ V_{CC} - 0.2V $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	190	80	165	mA
				L	—	165	80	140	
			COM'L.	S	90	160	80	135	
				L	90	135	80	110	

NOTES:

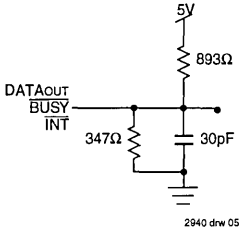
2940 tbl 10

1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/ tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

AC TEST CONDITIONS

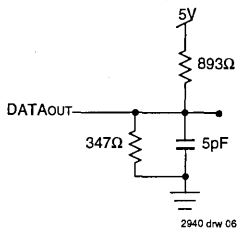
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2940 tbl 11



2940 drw 05

Figure 1. AC Output Load



2940 drw 06

Figure 2. Output Test Load
(for tLZ, tHZ, twz, tow)
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(4)

Symbol	Parameter	IDT7007X20 COM'L ONLY Min.	IDT7007X20 COM'L ONLY Max.	IDT7007X25 Min.	IDT7007X25 Max.	Unit
READ CYCLE						
tRC	Read Cycle Time	20	—	25	—	ns
tAA	Address Access Time	—	20	—	25	ns
tACE	Chip Enable Access Time(3)	—	20	—	25	ns
tAOE	Output Enable Access Time	—	12	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	3	—	3	—	ns
tHZ	Output High-Z Time(1, 2)	—	12	—	15	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	20	—	25	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	12	—	ns
tSAA	Semaphore Address Access Time	—	20	—	25	ns

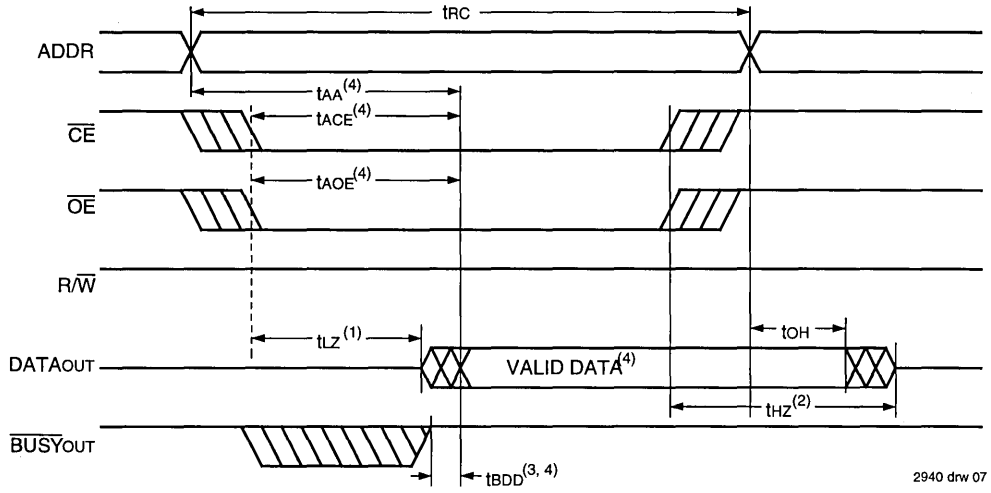
Symbol	Parameter	IDT7007X35 Min.	IDT7007X35 Max.	IDT7007X55 Min.	IDT7007X55 Max.	Unit
READ CYCLE						
tRC	Read Cycle Time	35	—	55	—	ns
tAA	Address Access Time	—	35	—	55	ns
tACE	Chip Enable Access Time(3)	—	35	—	55	ns
tAOE	Output Enable Access Time	—	20	—	30	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	3	—	3	—	ns
tHZ	Output High-Z Time(1, 2)	—	15	—	25	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	35	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	ns
tSAA	Semaphore Address Access Time	—	35	—	55	ns

NOTES:

2940 tbl 12

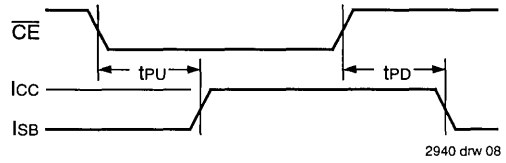
1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL.
4. "X" in part numbers indicates power rating (S or L).

WAVEFORM OF READ CYCLES[5]



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$ or $\overline{OE}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[5]

Symbol	Parameter	IDT7007X20 COM'L ONLY Min.	IDT7007X20 COM'L ONLY Max	IDT7007X25 Min.	IDT7007X25 Max.	Unit
WRITE CYCLE						
t_{WC}	Write Cycle Time	20	—	25	—	ns
t_{EW}	Chip Enable to End-of-Write[3]	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	ns
t_{AS}	Address Set-up Time[3]	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	15	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	12	—	15	ns
t_{DH}	Data Hold Time[4]	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1, 2]	—	12	—	15	ns
t_{OW}	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	ns

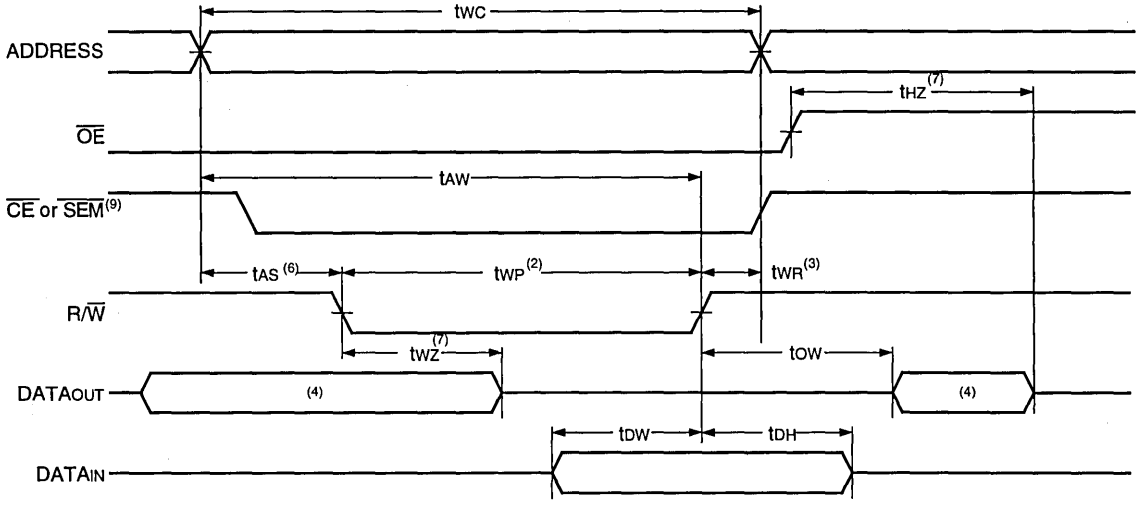
Symbol	Parameter	IDT7007X35 Min.	IDT7007X35 Max	IDT7007X55 Min.	IDT7007X55 Max.	Unit
WRITE CYCLE						
t_{WC}	Write Cycle Time	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write[3]	30	—	45	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	45	—	ns
t_{AS}	Address Set-up Time[3]	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	30	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	15	—	25	ns
t_{DH}	Data Hold Time[4]	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1, 2]	—	15	—	25	ns
t_{OW}	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	ns

NOTES:

2940 tbl 13

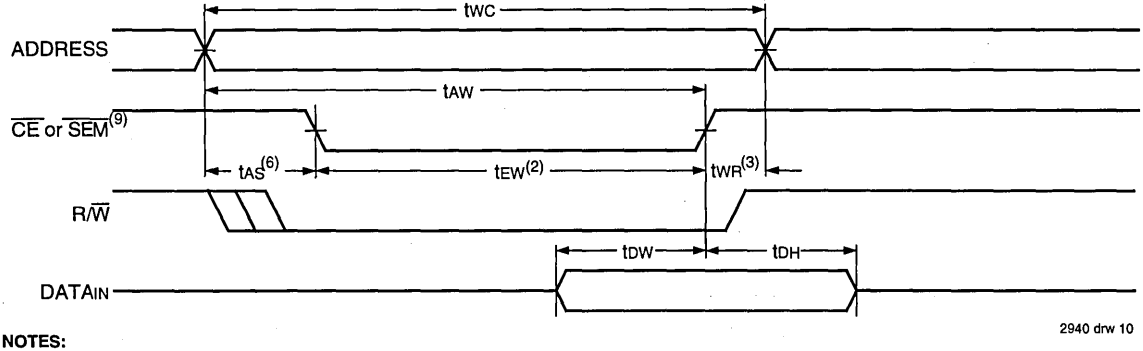
1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,5,8)



2940 drw 09

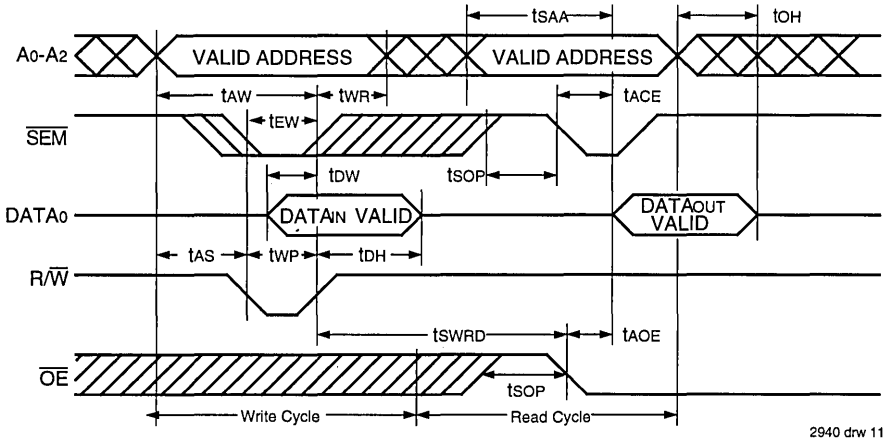
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,5,)



2940 drw 10

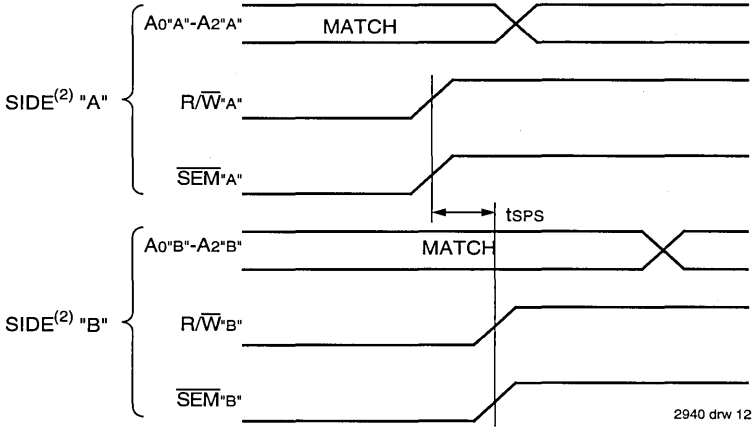
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a LOW $\overline{CE}$ and a LOW R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured ± 200mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. tEW must be met for either condition.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}_R$ = $\overline{CE}_L$ = VIH.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}_A$ or $\overline{SEM}_A$ going HIGH to R/$\overline{W}_B$ or $\overline{SEM}_B$ going HIGH.
4. If tSPS is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

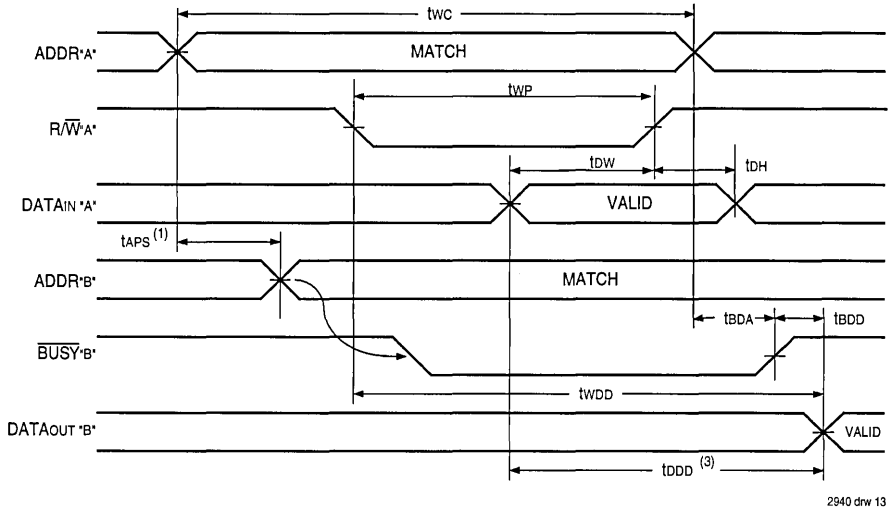
Symbol	Parameter	IDT7007X20 COM'L ONLY		IDT7007X25		Unit
		Min.	Max.	Min.	Max.	
BUSY TIMING (M/$\overline{S}$ = H)						
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	20	—	20	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	20	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	20	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	17	—	17	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	20	—	25	ns
BUSY TIMING (M/$\overline{S}$ = L)						
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	15	—	17	—	ns
PORT-TO-PORT DELAY TIMING						
tWDD	Write Pulse to Data Delay[1]	—	45	—	50	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	30	—	35	ns

Symbol	Parameter	IDT7007X35		IDT7007X55		Unit
		Min.	Max.	Min.	Max.	
BUSY TIMING (M/$\overline{S}$ = H)						
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	20	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	40	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	20	—	35	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	35	—	55	ns
BUSY TIMING (M/$\overline{S}$ = L)						
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING						
tWDD	Write Pulse to Data Delay[1]	—	60	—	80	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	45	—	65	ns

NOTES:
2940 tbl 14

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = VIH)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$ (2,5) (M/$\overline{S}$ = VIH)

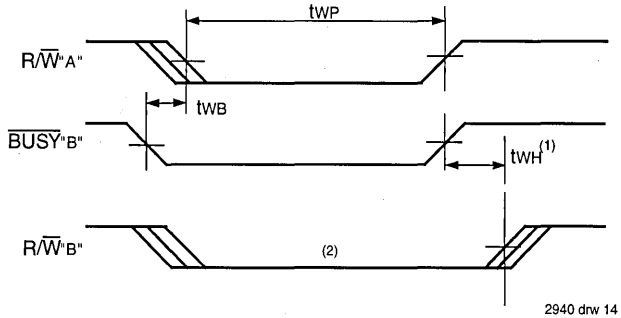


2940 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for M/$\overline{S}$ = VIL (SLAVE).
2. $\overline{CE}_L$ = $\overline{CE}_R$ = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. If M/$\overline{S}$ = VIL (SLAVE), then $\overline{BUSY}$ is an input ($\overline{BUSY}$"A" = VIH and $\overline{BUSY}$"B" = "don't care", for this example).
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

6

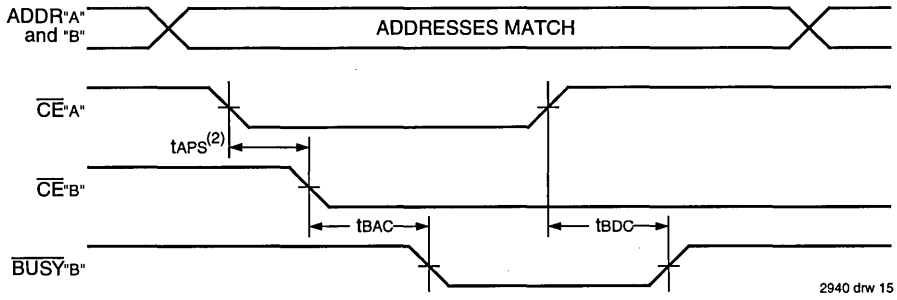
TIMING WAVEFORM OF WRITE WITH BUSY (M/$\overline{S}$ = VIL)



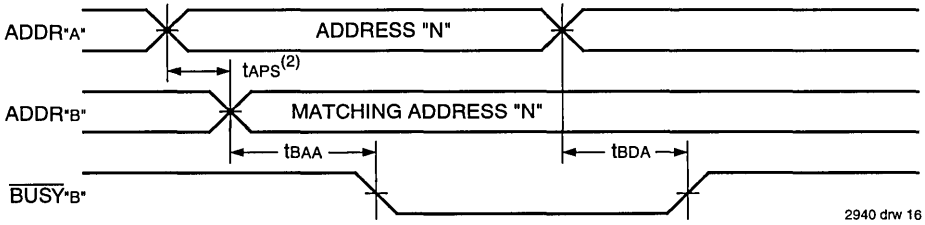
2940 drw 14

NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (SLAVE) and output (MASTER).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes High.

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING[1] (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING[1](M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

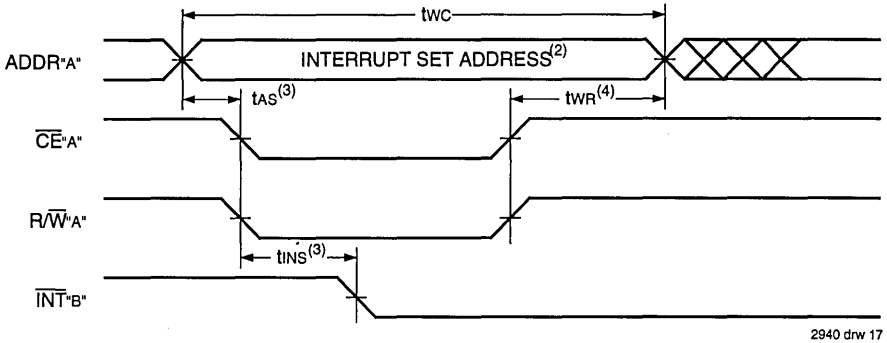
Symbol	Parameter	IDT7007X20 COM'L ONLY Min.	IDT7007X20 COM'L ONLY Max.	IDT7007X25 Min	IDT7007X25 Max.	Unit
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	20	ns
tINR	Interrupt Reset Time	—	20	—	20	ns

Symbol	Parameter	IDT7007X35 Min.	IDT7007X35 Max.	IDT7007X55 Min	IDT7007X55 Max.	Unit
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	40	ns
tINR	Interrupt Reset Time	—	25	—	40	ns

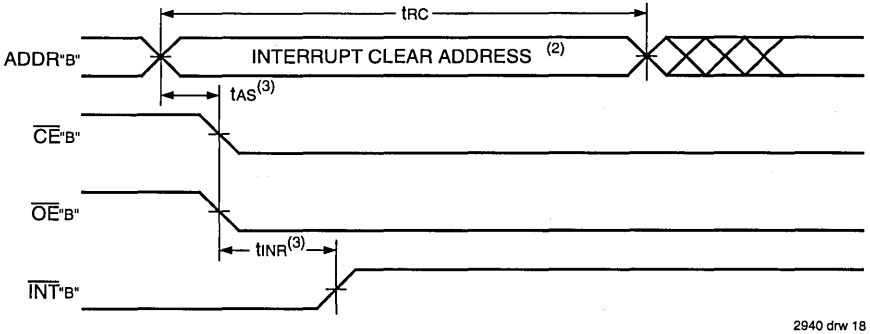
NOTE:
1. "X" in part numbers indicates power rating (S or L).

2739 tbl 15

WAVEFORM OF INTERRUPT TIMING[1]



2940 drw 17



2940 drw 18

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

6

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
R/$\overline{W}$L	$\overline{CE}$L	$\overline{OE}$L	A14L-A0L	$\overline{INT}$L	R/$\overline{W}$R	$\overline{CE}$R	$\overline{OE}$R	A14R-A0R	$\overline{INT}$R	Function
L	L	X	7FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}$R Flag
X	X	X	X	X	X	L	L	7FFF	H[3]	Reset Right $\overline{INT}$R Flag
X	X	X	X	L[3]	L	L	X	7FFE	X	Set Left $\overline{INT}$L Flag
X	L	L	7FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}$L Flag

NOTES:
1. Assumes $\overline{BUSY}$L = $\overline{BUSY}$R = VIH.
2. If $\overline{BUSY}$L = VIL, then no change.
3. If $\overline{BUSY}$R = VIL, then no change.

2739 tbl 16

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{14L} A_{0R}-A_{14R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

NOTES: 2940 tbl 17

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$ outputs on the IDT7007 are push-pull, not open drain outputs. On slaves the $\overline{BUSY}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_7 Left	D_0 - D_7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2940 tbl 18

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7007.

FUNCTIONAL DESCRIPTION

The IDT7007 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7007 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ HIGH). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FFE (HEX), where a write is defined as $\overline{CE}$ = R/$\overline{W}$ = V_{IL} per the Truth Table. The left port clears the interrupt through access of address location 7FFE when $\overline{CE}_R$ = $\overline{OE}_R$ = V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 7FFF. The message (8 bits) at 7FFE or 7FFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FFE and 7FFF are not used as mail boxes, but as part of the random access memory. Refer to Table 1 for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not

desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins HIGH. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port LOW.

The busy outputs on the IDT 7007 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7007 RAM array in width while using busy logic, one master part is used to decide which side of the RAMs array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7007 RAM the busy pin is

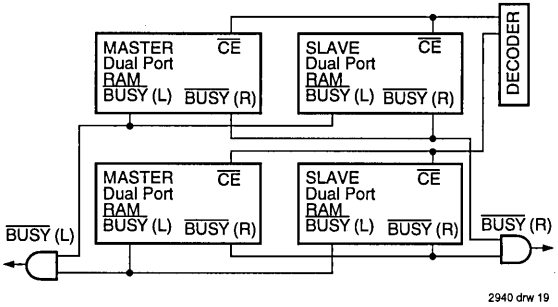


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7007 RAMs.

an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with the R/$\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7007 is an extremely fast Dual-Port 16K x 8 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both HIGH.

Systems which can best use the IDT7007 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7007s hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7007 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to

gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7007 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

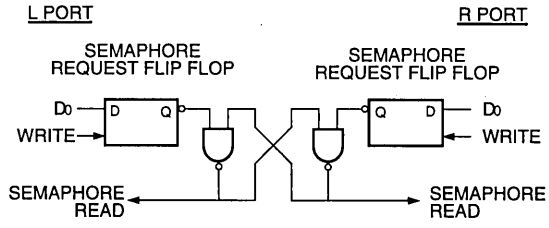


Figure 4. IDT7007 Semaphore Logic

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7007's Dual-Port RAM. Say the 32K x 8 RAM was to be divided into two 16K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the

indicator for the upper section of memory.

To take a resource, in this example the lower 16K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 16K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 16K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 16K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

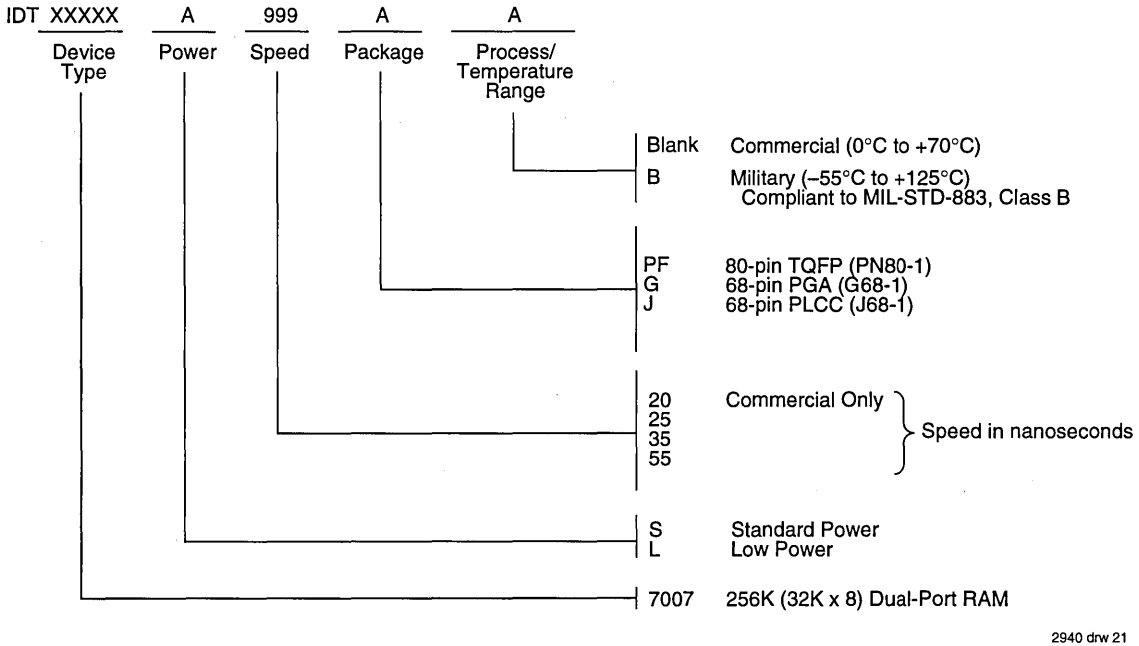
Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

6

ORDERING INFORMATION



2940 drw 21

Integrated Device Technology, Inc.

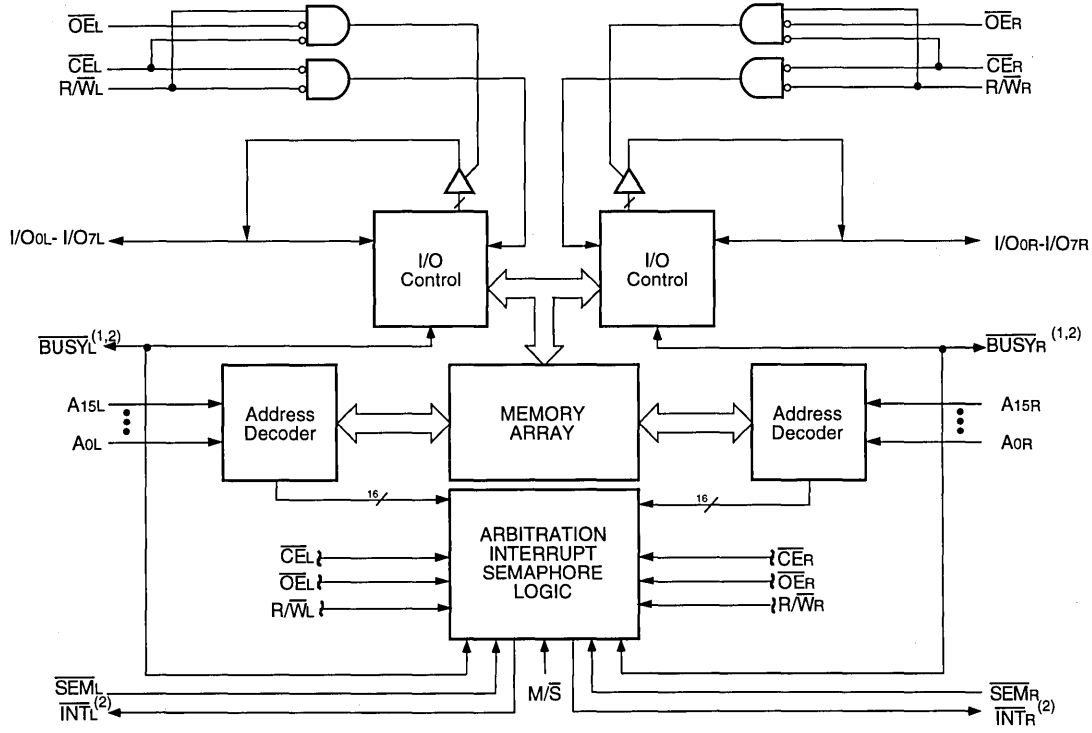
HIGH-SPEED 64K x 8 DUAL-PORT STATIC RAM

ADVANCED IDT7008S/L

FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 35/55ns (max.)
  - — Commercial: 25/35/55ns (max.)
- Low-power operation
  - — IDT7008S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7008L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- IDT7008 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master,
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Devices are capable of withstanding greater than 2001V electrostatic discharge
- TTL-compatible, single 5V (±10%) power supply
- Available in 84-pin PGA and PLCC and a 100-pin TQFP
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

FUNCTIONAL BLOCK DIAGRAM



3198 drw 01

NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ and $\overline{INT}$ outputs are non-tri-stated push-pull.

DESCRIPTION:

The IDT7008 is a high-speed 64K x 8 Dual-Port Static RAM. The IDT7008 is designed to be used as a stand-alone 512K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power.

The IDT7008 is packaged in an 84-pin pin PGA, an 84-pin PLCC, and a 1000-pin thin plastic quad flatpack, TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

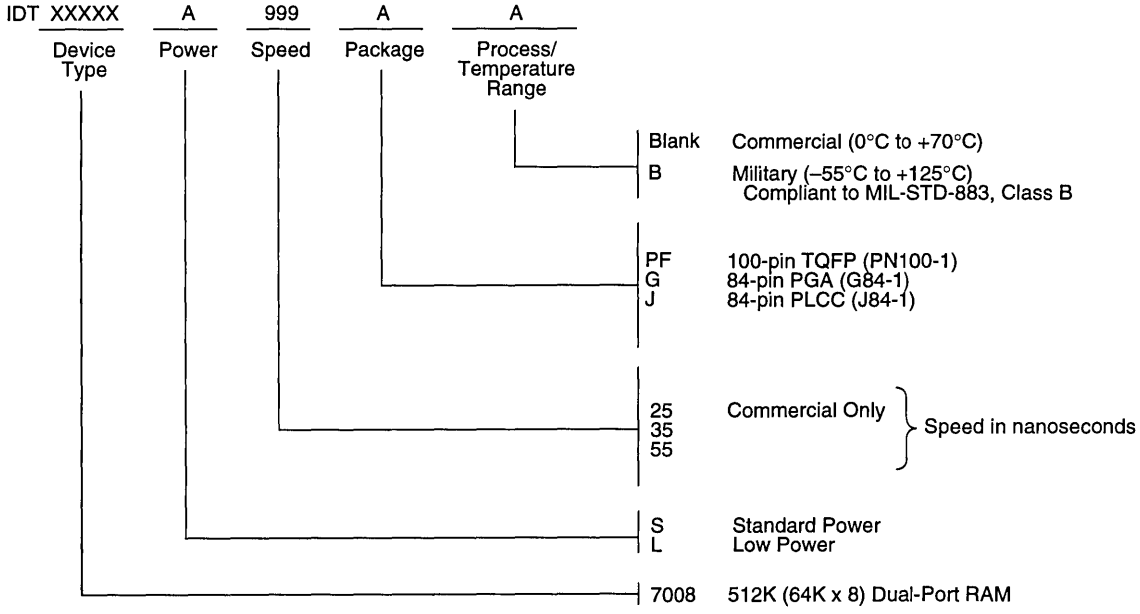
PIN NAMES

Left Port	Right Port	Names
$\overline{CE_L}$	$\overline{CE_R}$	Chip Enable
$R/\overline{W_L}$	$R/\overline{W_R}$	Read/Write Enable
$\overline{OE_L}$	$\overline{OE_R}$	Output Enable
$A_{0L} - A_{15L}$	$A_{0R} - A_{15R}$	Address
$I/O_{0L} - I/O_{7L}$	$I/O_{0R} - I/O_{7R}$	Data Input/Output
$\overline{SEM_L}$	$\overline{SEM_R}$	Semaphore Enable
$\overline{INT_L}$	$\overline{INT_R}$	Interrupt Flag
$\overline{BUSY_L}$	$\overline{BUSY_R}$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

3198 tbl 01

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part marking.

ORDERING INFORMATION



3198 drw 21

6

Integrated Device Technology, Inc.

HIGH-SPEED 2K x 9 DUAL-PORT STATIC RAM WITH BUSY & INTERRUPT

IDT70121S/L
IDT70125S/L

FEATURES:

- High-speed access
  - Commercial: 25/35/45/55ns (max.)
- Low-power operation
  - IDT70121/70125S
    Active: 500mW (typ.)
    Standby: 5mW (typ.)
  - IDT70121/70125L
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Fully asychronous operation from either port
- MASTER IDT70121 easily expands data bus width to 18 bits or more using SLAVE IDT70125 chip
- On-chip port arbitration logic (IDT70121 only)
- $\overline{BUSY}$ output flag on Master; $\overline{BUSY}$ input on Slave
- $\overline{INT}$ flag for port-to-port communication
- Battery backup operation—2V data retention
- TTL-compatible, signal 5V (±10%) power supply
- Available in 52-pin PLCC

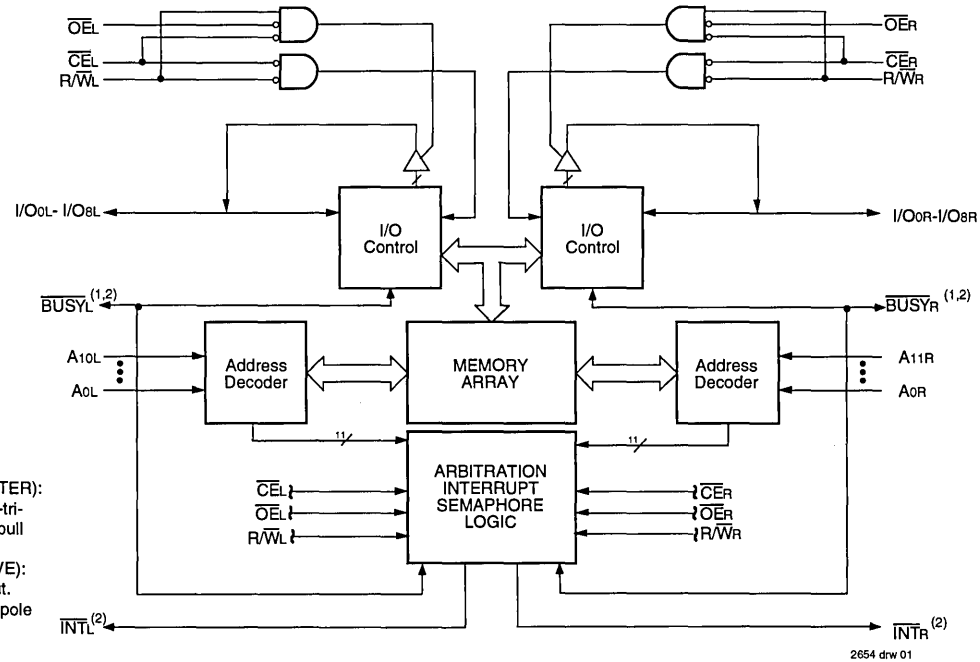
DESCRIPTION:

The IDT70121/IDT70125 are high-speed 2K x 9 Dual-Port Static RAMs. The IDT70121 is designed to be used as a stand-alone 9-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT70125 "SLAVE" Dual-Port in 18-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 18-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power-down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70121/IDT70125 utilizes a 9-bit wide data path to allow for Data/Control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

FUNCTIONAL BLOCK DIAGRAM



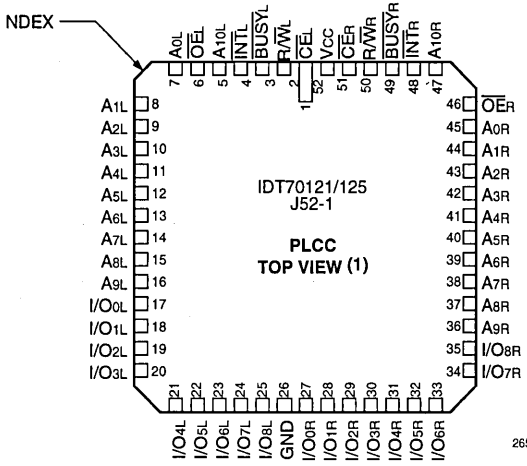
NOTES:
1. 70121 (MASTER): $\overline{BUSY}$ is non-tri-stated push-pull output.
   70125 (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{INT}$ is totem-pole output.

DESCRIPTION (Continued):

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 400mW of power. Low-power (L) versions offer battery backup data retention capability with each port typically consuming 200µW from a 2V battery.

The IDT70121/IDT70125 devices are packaged in a 52-pin PLCC.

PIN CONFIGURATIONS



2654 drw 02

NOTE:
1. This text does not indicate the orientation of the actual part-marking.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

2654 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2654 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0.0	V
V_{IH}	Input High Voltage	2.2	–	6.0(2)	V
V_{IL}	Input Low Voltage	–0.5(1)	–	0.8	V

2654 tbl 03

NOTE:
1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

2654 tbl 13

NOTE:
1. This parameter is determined by device characterization but is not production tested.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	70121S 70125S Min.	70121S 70125S Max.	70121L 70125L Min.	70121L 70125L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current[5]	V_{CC} = 5.5V, $\overline{CE}$ = V_{IH} V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V

NOTE:
1. At Vcc < 2.0V leakages are undefined.

2654 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1,4] (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version		70121 X 25 70125 X 25 Typ.	70121 X 25 70125 X 25 Max.	70121 X 35 70125 X 35 Typ.	70121 X 35 70125 X 35 Max.	70121 X 45 70125 X 45 Typ.	70121 X 45 70125 X 45 Max.	70121 X 55 70125 X 55 Typ.	70121 X 55 70125 X 55 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[2]	Com'l.	S	125	260	125	250	125	245	125	240	mA
				L	125	220	125	210	125	205	125	200	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_A$ and $\overline{CE}_B$ = V_{IH}, f = f_{MAX}[2]	Com'l.	S	30	65	30	65	30	65	30	65	mA
				L	30	45	30	45	30	45	30	45	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_A$ = V_{IL} and $\overline{CE}_B$ = V_{IH}[5] Active Port Outputs Open, f = f_{MAX}[2]	Com'l.	S	80	175	80	165	80	160	80	155	mA
				L	80	145	80	135	80	130	80	125	
I_{SB3}	Full Standby Current (Both Ports CMOS Level Inputs)	$\overline{CE}_A$ and $\overline{CE}_B$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[3]	Com'l.	S	1.0	15	1.0	15	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port CMOS Level Inputs)	$\overline{CE}_A$ ≤ 0.2V and $\overline{CE}_B$ ≥ V_{CC}-0.2V[5] V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[2]	Com'l.	S	70	170	70	160	70	155	70	150	mA
				L	70	140	70	130	70	125	70	120	

NOTES:
1. "X" in part numbers indicates power rating (S or L).
2. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
3. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
4. Vcc=5V, T_A=+25°C for Typ, and is not production tested.
5. Port "A" may be either left or right port. Port "B" is opposite from port "A".

2654 tbl 05

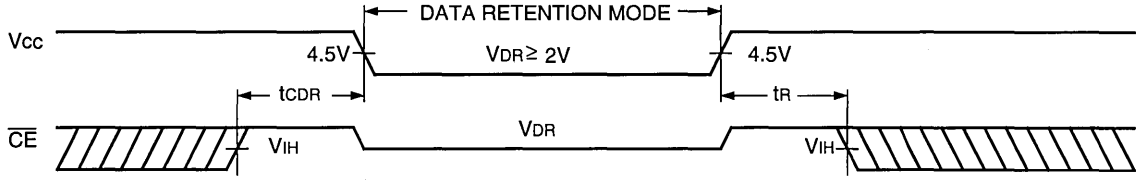
DATA RETENTION CHARACTERISTICS (L Version Only)

Symbol	Parameter	Test Condition		70121L/70125L Min.	Typ.[1]	Max.	Unit
V_{DR}	Vcc for Data Retention	V_{CC} = 2.0V, $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		2	—	—	V
I_{CCDR}	Data Retention Current		Com'l.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C, and are not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but is not production tested.

2654 tbl 06

DATA RETENTION WAVEFORM

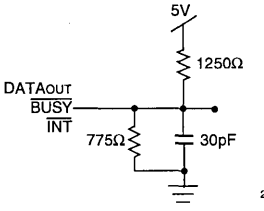


2654 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1 and 2

2654 tbl 07



2654 drw 04

Figure 1. AC Output Test Load

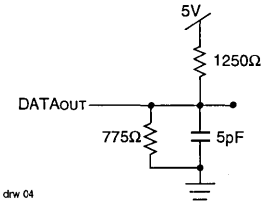


Figure 2. Output Test Load
(For tLZ, tHZ, tWZ, tOW)
Including scope and jig.

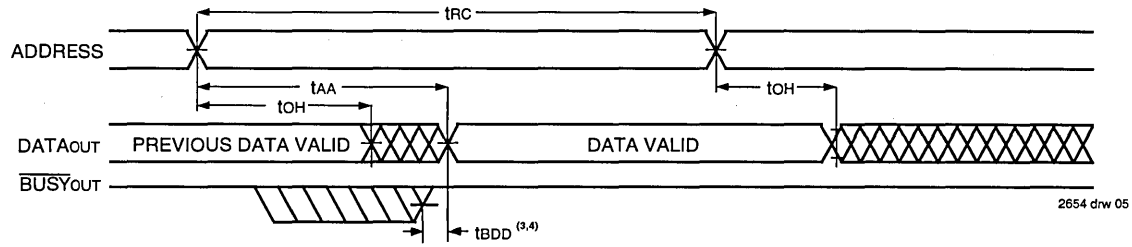
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3]

Symbol	Parameter	70121 X 25 70125 X 25 Min.	Max.	70121 X 35 70125 X 35 Min.	Max.	70121 X 45 70125 X 45 Min.	Max.	70121 X 55 70125 X 55 Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	25	—	35	—	45	—	55	—	ns
t_{AA}	Address Access Time	—	25	—	35	—	45	—	55	ns
t_{ACE}	Chip Enable Access Time	—	25	—	35	—	45	—	55	ns
t_{AOE}	Output Enable Access Time	—	12	—	25	—	30	—	35	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1,2]	0	—	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	10	—	15	—	20	—	30	ns
t_{PU}	Chip Enable to Power-Up Time[2]	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power-Down Time[2]	—	50	—	50	—	50	—	50	ns

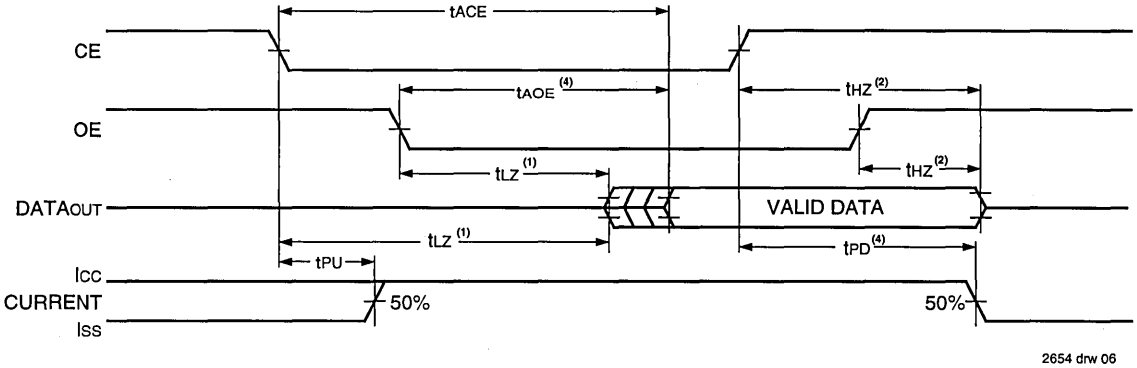
NOTES:
1. Transition is measured ±500mV from Low or High impedance voltage with the Output Test Load (Figure 2).
2. This parameter guaranteed by device characterization, but is not production tested.
3. "X" in part numbers indicates power rating (S or L).

2654 tbl 08

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2,4]



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[5]



NOTES:
1. Timing depends on which signal is aserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is deaserted first, $\overline{OE}$ or $\overline{CE}$.
3. tBDD delay is required only in a case where the opposite port is completing a write operation to the same address location. For simultanious read operations $\overline{BUSY}$ has no relationship to valid output data.
4. Start of valid data depends on which timing becomes effective last, tAOE, tACE, tAA, or tBDD.
5. R/$\overline{W}$ = VIH, and the address is valid prior to other coincidental with $\overline{CE}$ transition Low.

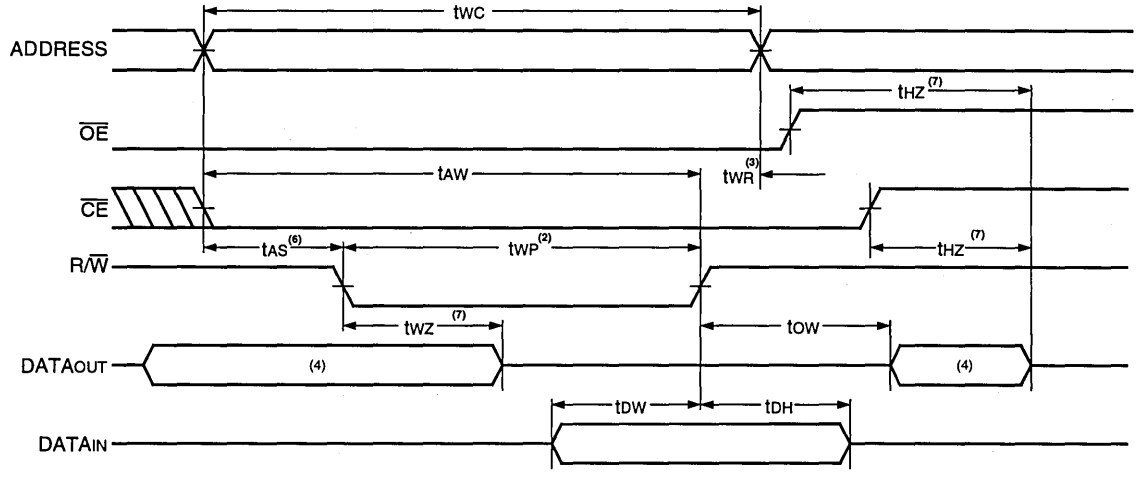
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

Symbol	Parameter	70121 X 25 70125 X 25		70121 X 35 70125 X 35		70121 X 45 70125 X 45		70121 X 55 70125 X 55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
twc	Write Cycle Time[3]	25	—	35	—	45	—	55	—	ns
tew	Chip Enable to End-of-Write	20	—	30	—	35	—	40	—	ns
taw	Address Valid to End-of-Write	20	—	30	—	35	—	40	—	ns
tas	Address Set-up Time	0	—	0	—	0	—	0	—	ns
twp	Write Pulse Width[6]	20	—	30	—	35	—	40	—	ns
twr	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tdw	Data Valid to End-of-Write	12	—	20	—	20	—	20	—	ns
thz	Output High-Z Time[1,2]	—	10	—	15	—	20	—	30	ns
tdh	Data Hold Time[5]	0	—	0	—	0	—	0	—	ns
twz	Write Enabled to Output in High-Z[1,2]	—	10	—	15	—	20	—	30	ns
tow	Output Active from End-of-Write[1,2]	0	—	0	—	0	—	0	—	ns

NOTES:
2654 tbl 09

1. Transition is measured ±500mV from low or high impedance voltage with Output Test Load (Figure 2).
2. This parameter guaranteed by device characterization, but is not production tested.
3. For MASTER/SLAVE combination, twc = tBAA + twp, since R/$\overline{W}$ = VIL must occur after tBAA .
4. "X" in part numbers indicates power rating (S or L).
5. The specified tdh must be met by the device supplying write date to the RAM under all operating conditions. Although tdh and tow values will vary over voltage nad temperature. The actual tdh will always be smaller than the actual tow.
6. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of twp or (twz + tdw) to allow the I/O drivers to turn off\ data to be placed on the bus for the required tdw. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.

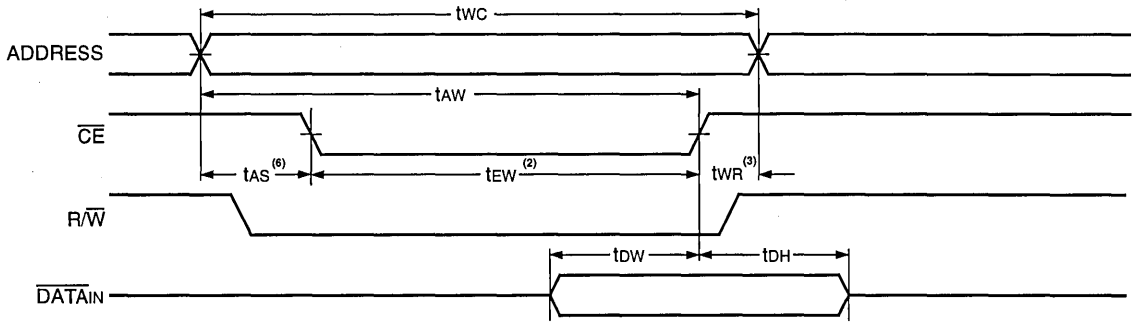
TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING[1,5,8]



2654 drw 07

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be High during all address transitions.
2. A write occurs during the overlap (tew or twp) of a $\overline{CE}$ = VIL and a R/$\overline{W}$ = VIL
3. twr is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going High to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ Low transition occurs simultaneously with or after the R/$\overline{W}$ Low transition, the outputs remain in the high-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined be device characterization, but is not production tested. Transition is measured +/- 500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of twp or (twz + tdw) to allow the I/O drivers to turn off data to be placed on the bus for the required tdw. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.

TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,5)



2654 drw 08

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be High during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a $\overline{CE}$ = VIL and a R/$\overline{W}$ = VIL
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going High to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ Low transition occurs simultaneously with or after the R/$\overline{W}$ Low transition, the outputs remain in the high-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined be device characterization, but is not production tested. Transition is measured +/- 500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

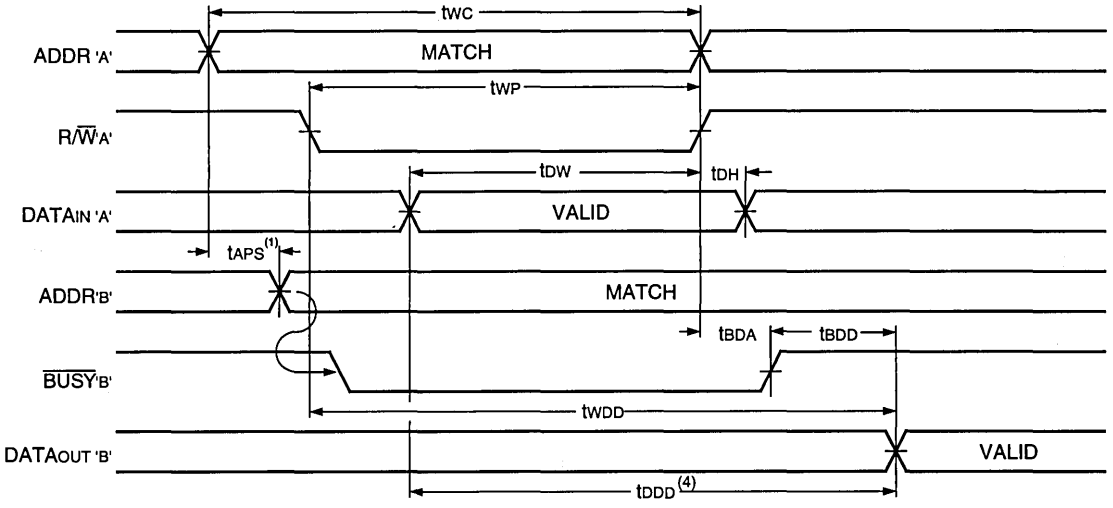
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(6)

Symbol	Parameter	70121 X 25 70125 X 25 Min.	70121 X 25 70125 X 25 Max.	70121 X 35 70125 X 35 Min.	70121 X 35 70125 X 35 Max.	70121 X 45 70125 X 45 Min.	70121 X 45 70125 X 45 Max.	70121 X 55 70125 X 55 Min.	70121 X 55 70125 X 55 Max.	Unit
Busy Timing (For Master IDT70121 Only)										
tBAA	$\overline{BUSY}$ Access Time from Address	—	20	—	20	—	20	—	30	ns
tBDA	$\overline{BUSY}$ Disable Time from Address	—	20	—	20	—	20	—	30	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	20	—	20	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	20	—	20	—	30	ns
tWDD	Write Pulse to Data Delay(1)	—	50	—	60	—	70	—	80	ns
tDDD	Write Data Valid to Read Data Delay(1)	—	35	—	45	—	55	—	65	ns
tAPS	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data(3)	—	25	—	35	—	45	—	55	ns
Busy Timing (For Slave IDT70125 Only)										
tWB	Write to $\overline{BUSY}$ Input(4)	0	—	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$(5)	15	—	20	—	20	—	20	—	ns
tWDD	Write Pulse to Data Delay(1)	—	50	—	60	—	70	—	80	ns
tDDD	Write Data Valid to Read Data Delay(1)	—	35	—	45	—	55	—	65	ns

2654 tbl 10

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port -to-Port Read and $\overline{BUSY}$.
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that a write cycle is inhibited on port 'B' during contention on port 'A'..
5. To ensure that a write cycle is completed on port 'B' after contention on port 'A'.
6. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$ (1,2,3)

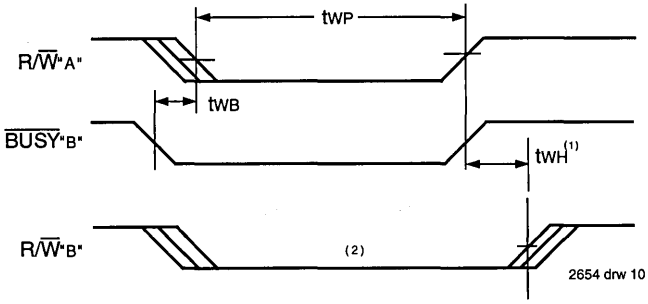


2654 drw 09

NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for Slave (IDT 70125).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
3. $\overline{OE} = V_{IL}$ for the reading port.
4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is oppsite from port "A".

6

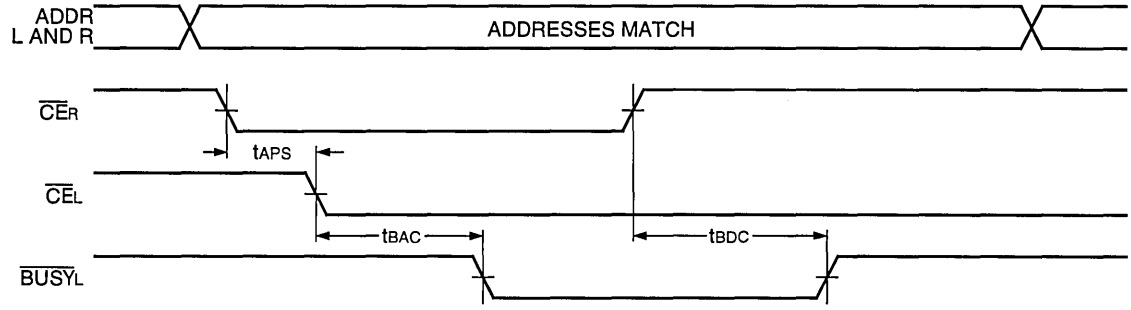
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$



2654 drw 10

NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (slave) and output (master).
2. $\overline{BUSY}$ is asserted on port 'B' blocking R/$\overline{W}_B$, until $\overline{BUSY}_B$ goes High.
3. All timing is the same for left and right ports. Port"A" may be either left or right port. Port "B" is the opposite from port "A".

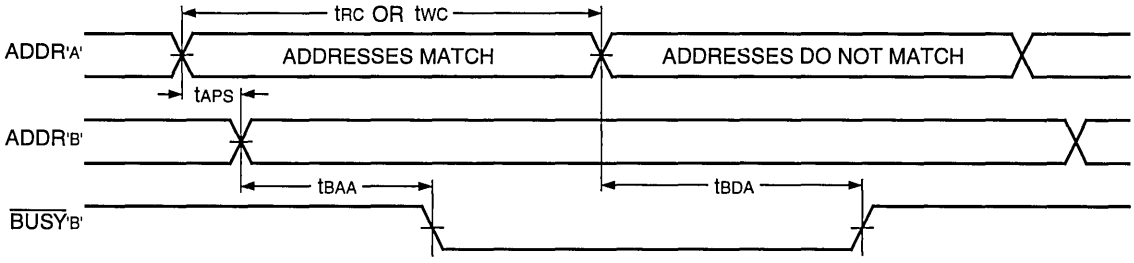
TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMIING(1)



2654 drw 12

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If tAPS is not satisified, the BUSY will be asserted on one side or the other, but there is no guarantee on which side BUSY will be asserted (70121 only).

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESS (1)



2654 drw 13

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If tAPS is not satisified, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted (70121 only).

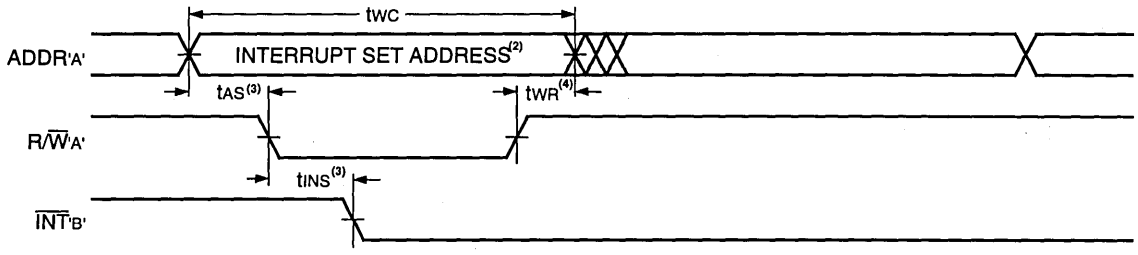
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1)

Symbol	Parameter	70121 X 25 70125 X 25 Min.	Max.	70121 X 35 70125 X 35 Min.	Max.	70121 X 45 70125 X 45 Min.	Max.	70121 X 55 70125 X 55 Min.	Max.	Unit
Interrupt Timing										
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	25	—	40	—	45	ns
tINR	Interrupt Reset Time	—	25	—	35	—	40	—	45	ns

NOTES:
1. "X" in part numbers indicates power rating (S or L).

2654 tbl 11

TIMING WAVEFORM OF INTERRUPT MODE



2654 drw 14

NOTES:.
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. See Interupt Truth Table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TABLE I. NON-CONTENTION READ/WRITE CONTROL(4)

Left or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-8}	Function
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R$ = $\overline{CE}_L$ = H, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written Into Memory(2)
H	L	L	DATAOUT	Data in Memory Output on Port(3)
H	L	H	Z	High Impedance Outputs

NOTES:
2654 tbl 12
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. 'H' = V_{IH}, 'L' = V_{IL}, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

TABLE II. INTERRUPT FLAG(1,4)

Left Port					Right Port					Function
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L} - A_{10L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0L} - A_{10R}$	$\overline{INT}_R$	
L	L	X	7FF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
2654 tbl 13
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = V_{IH}
2. If $\overline{BUSY}_L$ = V_{IL}, then No Change.
3. If $\overline{BUSY}_R$ = V_{IL}, then No Change.
4. 'H' = HIGH,' L' = LOW,' X' = DON'T CARE

FUNCTIONAL DESCRIPTION

The IDT70121/125 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70121/125 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FE (HEX), where a write is defined as the $\overline{CE} = R/\overline{W} = V_{IL}$ per the Truth Table. The left port clears the interrupt by access address location 7FE access when $\overline{CE}_R = \overline{OE}_R = V_{IL}$, $R/\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must access the memory location 7FF. The message (9 bits) at 7FE or 7FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the $M/\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT70121/125 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT70121/125 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT70121 RAM the busy pin is an output of the part, and the busy pin is an input of the IDT70125 as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the $R/\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

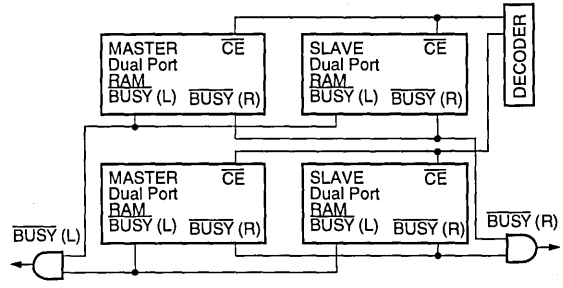
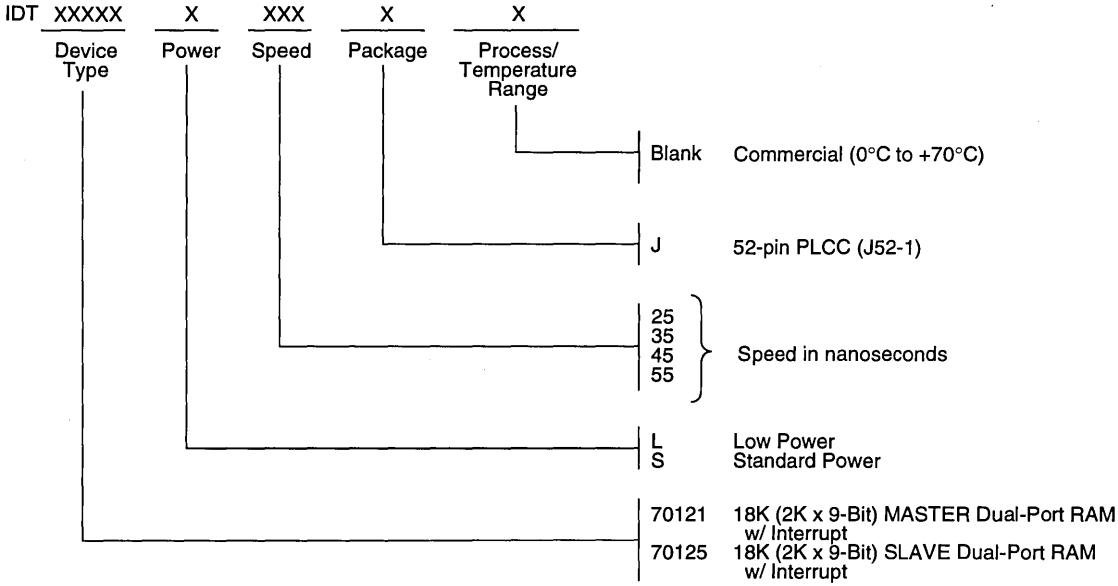


Figure 3. Busy and chip enable routing for both width and depth expansion with 70121 (Master) and 70125 (Slave) RAMs.

ORDERING INFORMATION



2654 drw 16

6

Integrated Device Technology, Inc.

HIGH-SPEED 36K (4K x 9-BIT) DUAL-PORT RAM

IDT7014S

FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Commercial: 12/15/20/25ns (max.)
- Low-power operation
  - — IDT7014S
    Active: 900mW (typ.)
- Fully asynchronous operation from either port
- TTL-compatible; single 5V (±10%) power supply
- Available in 52-pin PLCC and a 64-pin TQFP

DESCRIPTION:

The IDT7014 is an extremely high-speed 4K x 9 Dual-Port Static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to high-speed applications which do not rely on $\overline{BUSY}$ signals to manage simultaneous access.

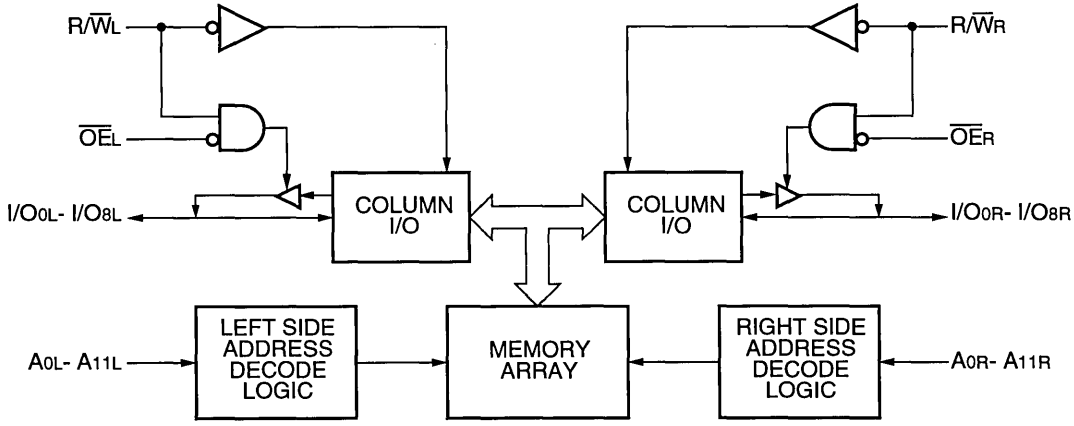
The IDT7014 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. See functional description.

The IDT7014 utilitizes a 9-bit wide data path to allow for parity at the user's option. This feature is especially useful in data communication applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's BiCMOS high-performance technology, these Dual-Ports typically operate on only 900mW of power at maximum access times as fast as 12ns.

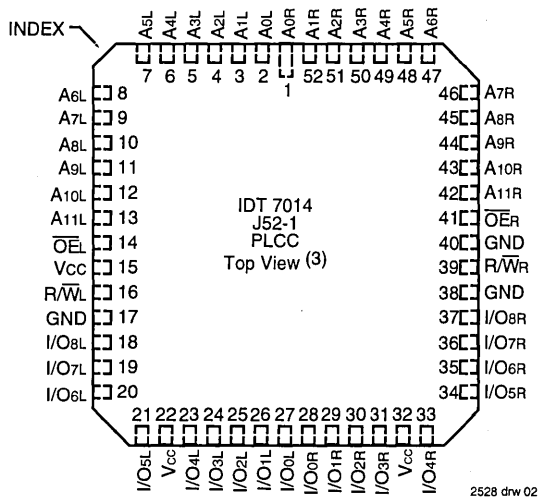
The IDT7014 is packaged in a 52-pin PLCC and a 64-pin thin plastic quad flatpack, (TQFP).

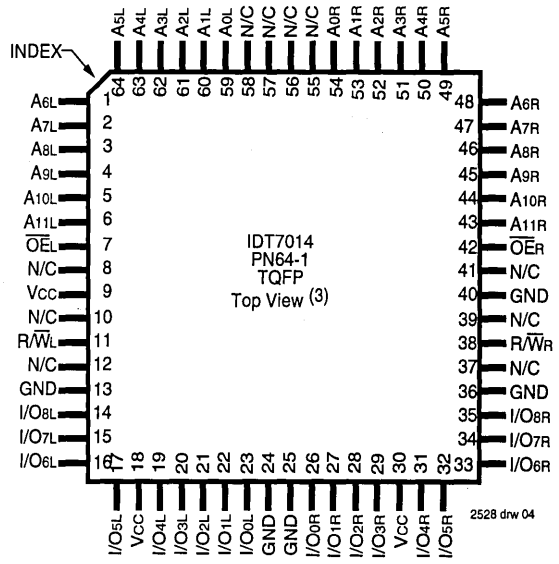
FUNCTIONAL BLOCK DIAGRAM



2528 drw 01

PIN CONFIGURATION





NOTES:
1. All Vcc pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. This text does not indicate the orentation of the actual part-marking

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
VTERM(3)	Terminal Voltage	–0.5 to Vcc	–0.5 to Vcc	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

2528 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2528 tbl 02

RECOMMENDED DC OPERATING CONDTIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0(2)	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

2528 tbl 03

NOTE:
1. VIL ≥ -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 0.5V.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT7014S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	V

2528 tbl 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version	IDT7014S12 Com'l Only		IDT7014S15 Com'l Only		IDT7014S20		IDT7014S25		DT7014S35 Mil Only		Unit
				Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	Outputs Open f = f_{MAX}(1)	Mil.	—	—	160	260	155	260	150	255	150	250	mA
			Com'l.	160	250	160	250	155	245	150	240	—	—	

NOTES:
1. At f = fmax, address inputs are cycling at the maximum read cycle of 1/tRC using the "AC Test Conditions" input levels of GND to 3V.

2528 tbl 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

2528 tbl 06

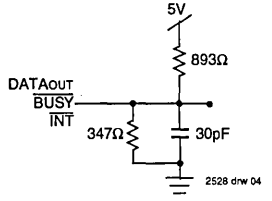


Figure 1. AC Output Test Load.

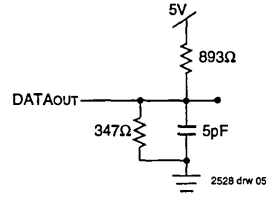


Figure 2. Output Test Load (for tHZ, tWZ, and tOW) Including scope and jig.

CAPACITANCE (T_A = +25°C, f = 1.0MHz) TQFP Package Only

Symbol	Parameter(1)	Condition(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

2528 tbl 07

NOTES:
1. This parameter is determined by device characteristics but is not tested.
2. 3dv references the interperlated capacitance when the input and output signals swith from OV to 3V or from 3V to 0v.

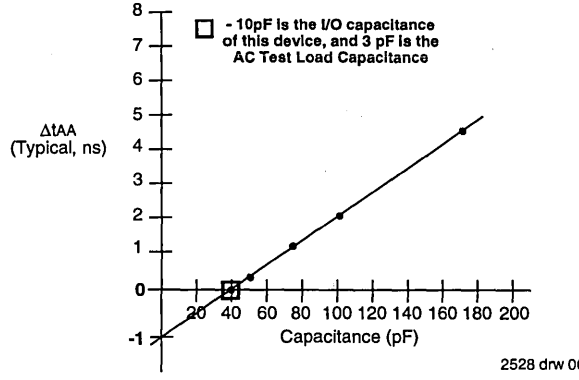


Figure 1. Typical Output Derating (Lumped Capacitive Load).

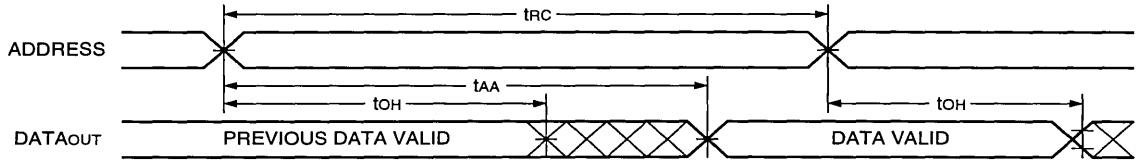
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

		7014Sx12		7014Sx15		7014Sx20		7014Sx25		7014Sx35		
		COM'L ONL		COM'L ONL						MIL ONLY		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE												
t_{RC}	Read Cycle Time	12	—	15	—	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	8	—	8	—	10	—	12	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1, 2]	3	—	3	—	3	—	3	—	3	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	7	—	7	—	9	—	11	—	15	ns

NOTES:
2528 tbl 08

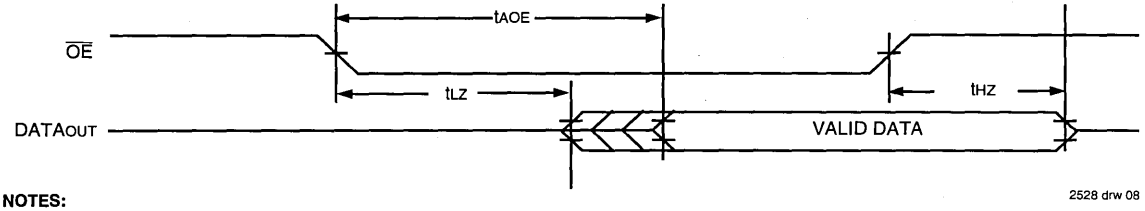
1. Transition is measured ±200mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is determined by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1,2]



2528 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



2528 drw 08

NOTES:
1. R/$\overline{W}$ = VIH for Read Cycles.
2. $\overline{OE}$ = VIL.
3. Addresses valid prior to $\overline{OE}$ transition LOW.

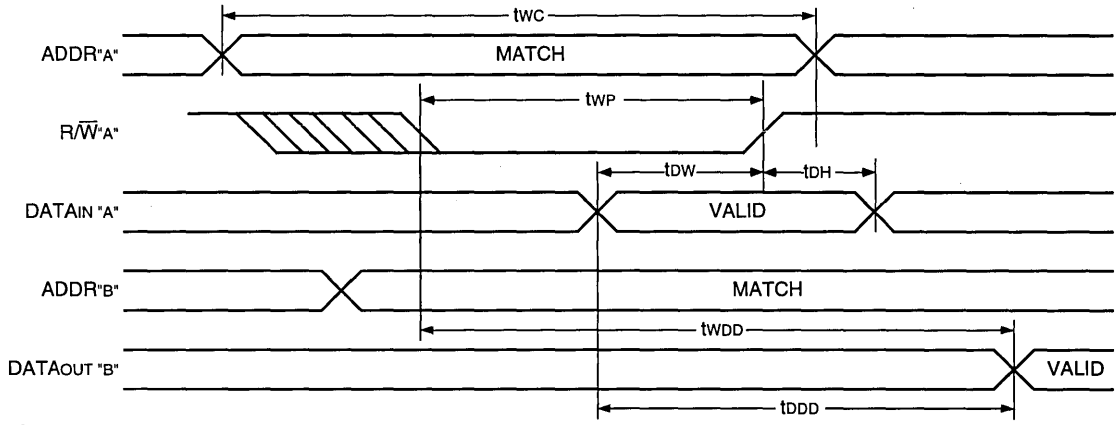
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

		7014S12		7014S15		7014S20		7014S25		7014S35		
		Com'l Only		Com'l Only						Mil Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
WRITE CYCLE												
tWC	Write Cycle Time	12	—	15	—	20	—	25	—	35	—	ns
tAW	Address Valid to End-of-Write	10	—	14	—	15	—	20	—	30	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	12	—	15	—	20	—	30	—	ns
tWR	Write Recovery Time	1	—	1	—	2	—	2	—	2	—	ns
tDW	Data Valid to End-of-Write	8	—	10	—	12	—	15	—	25	—	ns
tHZ	Output High-Z Time[1, 2]	—	7	—	7	—	9	—	11	—	15	ns
tDH	Data Hold Time[3]	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High-Z[1, 2]	—	7	—	7	—	9	—	11	—	15	ns
tOW	Output Active from End-of-Write[1, 2, 3]	0	—	0	—	0	—	0	—	0	—	ns
tWDD	Write Pulse to Data Delay[4]	—	25	—	30	—	40	—	45	—	55	ns
tDDD	Write Data Valid to Read Data Delay[4]	—	22	—	25	—	30	—	35	—	45	ns

NOTES:
2528 tbl 09

1. Transition is measured ±200mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tow values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tow.
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write With Port-to-Port Read".

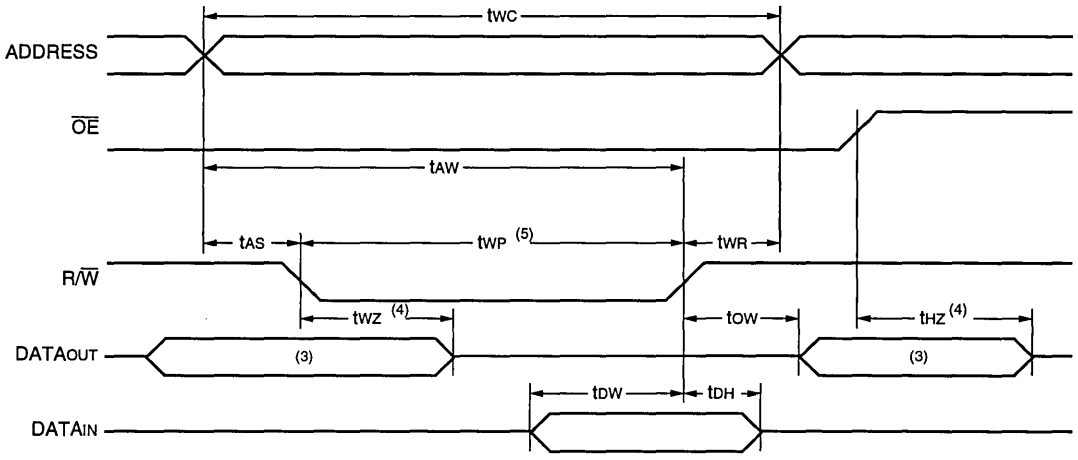
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ [1,2]



NOTES:
2528 drw 09

1. R/W"B" = VIH, Read cycle pass through.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is opposite from port "A".

TIMING WAVEFORM OF WRITE CYCLE(1, 2, 3, 4, 5)



2528 drw 10

NOTES:
1. R/W must be HIGH during all address transitions.
2. tWR is measured from R/W going HIGH to the end of write cycle.
3. During this period, the I/O pins are in the output state, and input signals must not be applied.
4. Transition is measured ±200mV from the Low or High-impedance voltage with the Output Test Load (Figure 2).
5. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If OE is HIGH during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

6

FUNCTIONAL DESCRIPTION

The IDT7014 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. It lacks the chip enable feature of CMOS Dual Ports, thus it operates in active mode as soon as power is applied. Each port has its own Output Enable control (OE). In the read mode, the port's OE turns on the output drivers when set LOW. The user application should avoid simultaneous write operations to the same memory location. There is no on-chip arbitration circuitry to resolve write priority and partial data from both ports may be written. READ/WRITE conditions are illustrated in table 1.

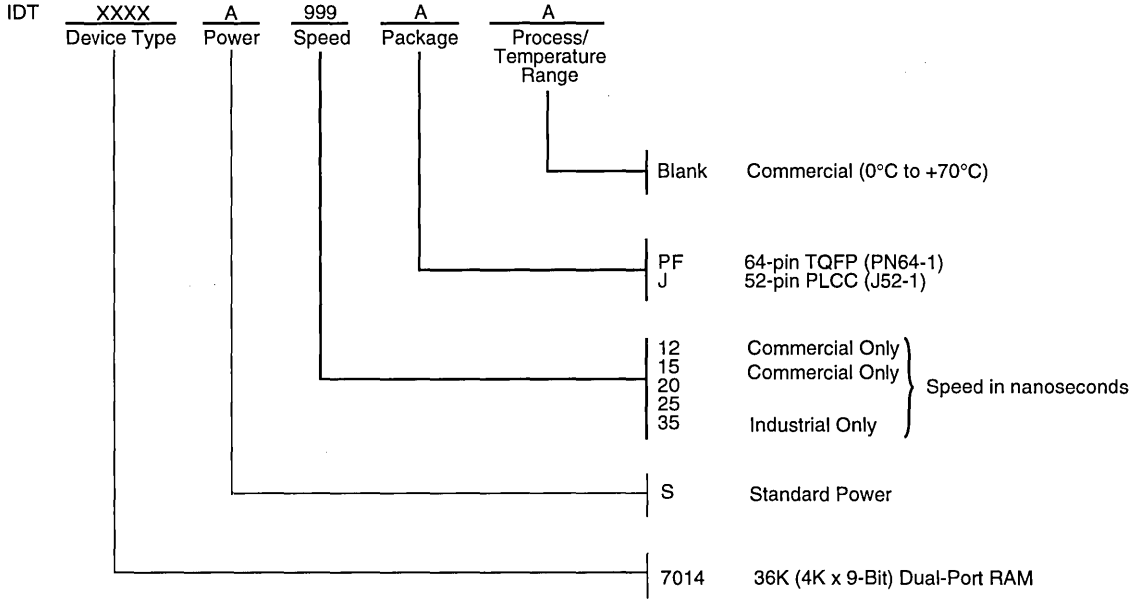
TABLE I – READ/WRITE CONTROL

Left or Right Port(1)			
R/W	OE	D0-8	Function
L	X	DATAIN	Data on port written into memory
H	L	DATAOUT	Data in memory output on port
X	H	Z	High-impedance outputs

2528 tbl 10

NOTE:
1. AOL - A11L is not equal to AOR - A11R.
'H' = HIGH,'L' = LOW, 'X' = Don't Care, and 'Z' = High Impedance.

ORDERING INFORMATION



2528 drw 11

Integrated Device Technology, Inc.

HIGH-SPEED 8K x 9 DUAL-PORT STATIC RAM

IDT7015S/L

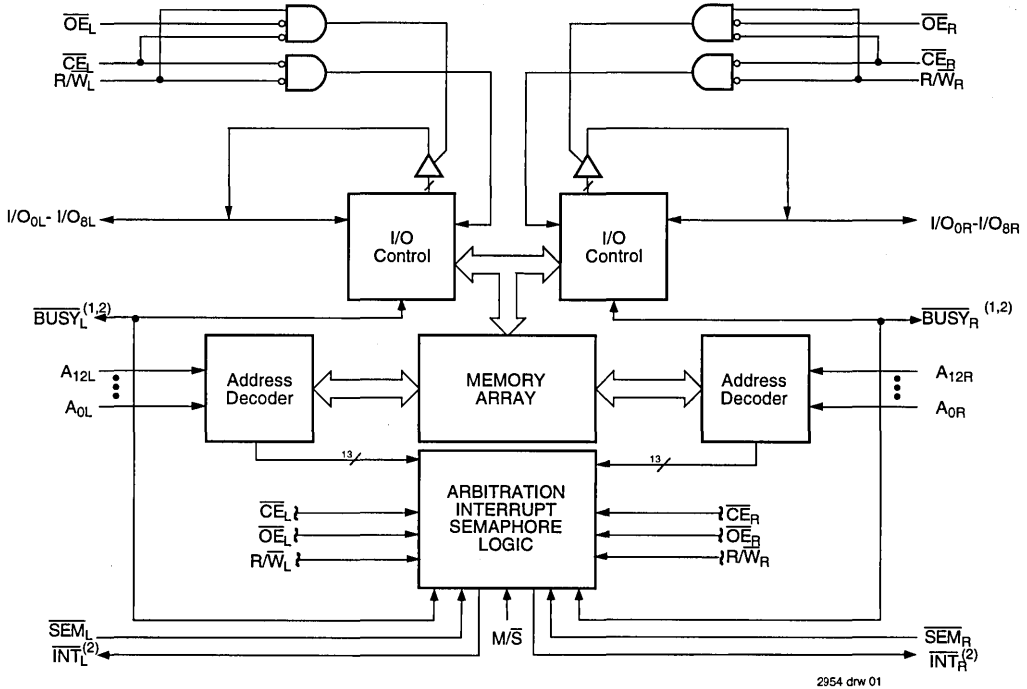
FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 25/35ns (max.)
  - — Commercial:15/17/20/25/35ns (max.)
- Low-power operation
  - — IDT7015S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7015L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- IDT7015 easily expands data bus width to 18 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Devices are capable of withstanding greater than 2001V electrostatic discharge
- TTL-compatible, single 5V (±10%) power supply
- Available in ceramic 68-pin PGA, 68-pin PLCC, and an 80-pin TQFP
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7015 is a high-speed 8K x 9 Dual-Port Static RAMs. The IDT7015 is designed to be used as stand-alone 72K bit Dual-Port RAMs or as a combination MASTER/SLAVE Dual-Port RAM for 18-bit-or-more word systems.

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. In MASTER mode: $\overline{BUSY}$ is an output and is a push-pull driver
   In SLAVE mode: $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ outputs and $\overline{INT}$ outputs are non-tristated push-pull drivers.
3. A$_{12L}$ and A$_{12R}$

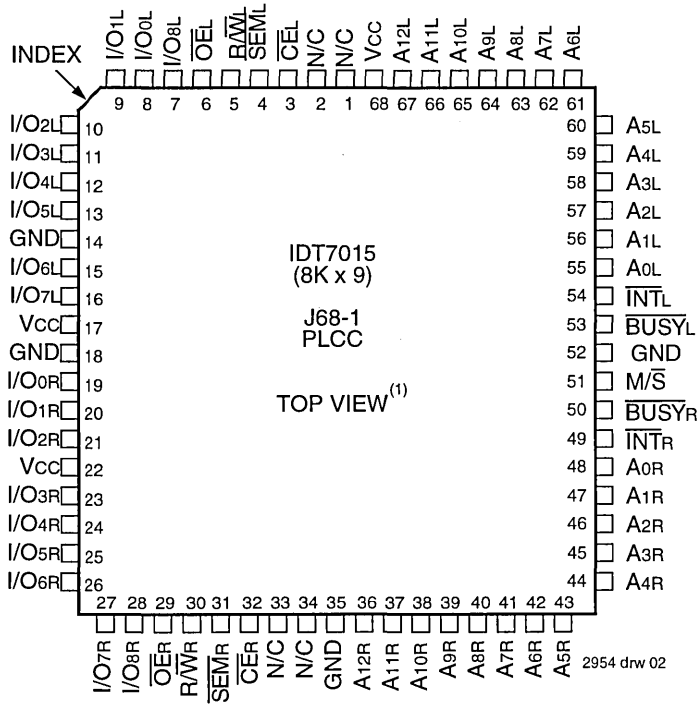
Using the IDT MASTER/SLAVE Dual-Port RAM approach in 18-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power.

The IDT7015 is packaged in a ceramic 68-pin PGA, a 64-pin PLCC and an 80-pinTQFP (Thin Quad FlatPack). Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



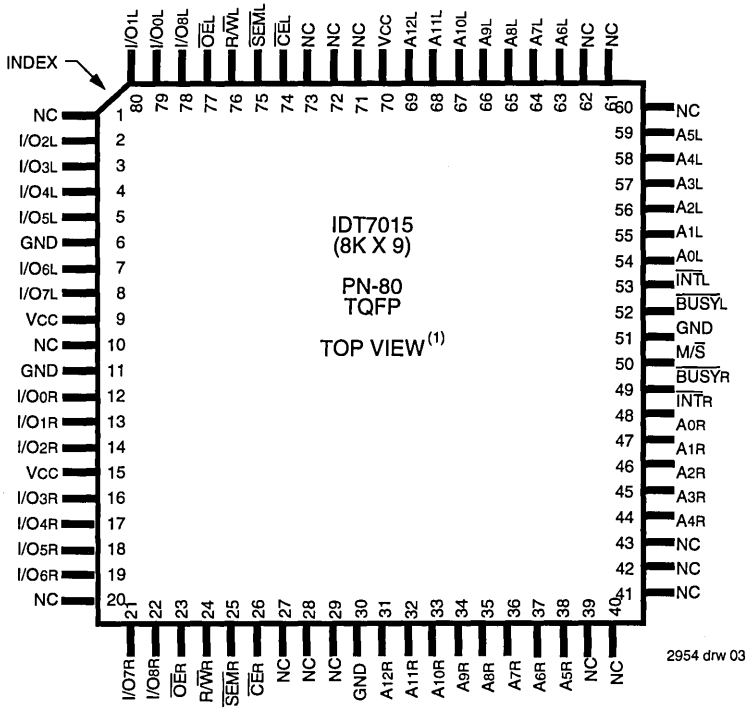
PIN NAMES (7015)

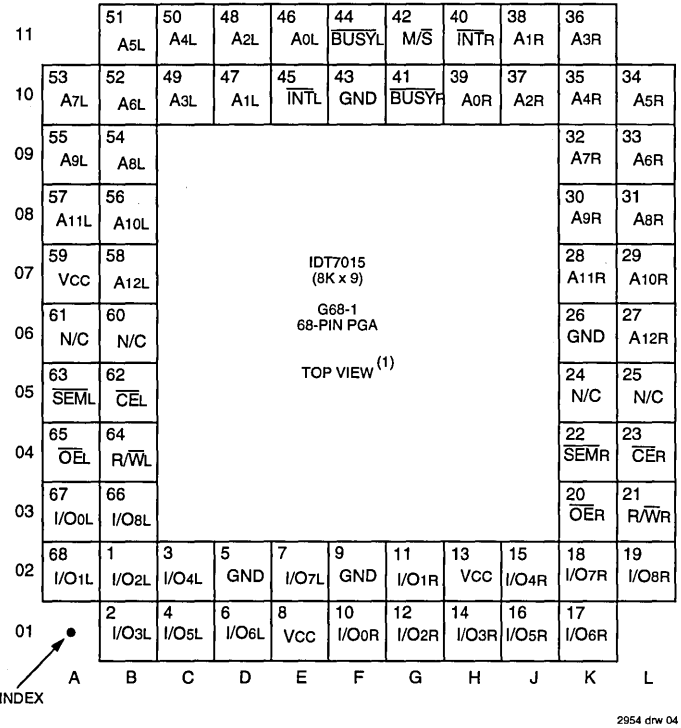
Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{12L}$	$A_{0R} - A_{12R}$	Address
$I/O_{0L} - I/O_{8L}$	$I/O_{0R} - I/O_{8R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}(1)		Power
GND(2)		Ground

2954 tbl 01

NOTES:
1. This text does not imply orientation of Part-Mark.

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.





NOTES:
1. This text does not imply orientation of Part-Mark.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-8	Mode
H	X	X	H	High-Z	Deselected: Power-Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read Memory
X	X	H	X	High-Z	Outputs Disabled

NOTE:
1. Condition: A0L — A12L is not equal to A0R — A12R

2954 tbl 02

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-8	Mode
H	H	L	L	DATAOUT	Read Semaphore Flag Data Out
H	↑	X	L	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	—	Not Allowed

2954 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTES:
2954 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2954 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0[2]	V
VIL	Input Low Voltage	–0.5[1]	—	0.8	V

NOTES:
2954 tbl 06
1. VIL ≥ -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 0.5V.

CAPACITANCE (TA = +25°C, f = 1.0MHz, for TQFP Package)[1]

Symbol	Parameter	Conditions[2]	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	9	pF
COUT	Output Capacitance	VOUT = 3dV	10	pF

2954 tbl 07

NOTES:
1. This parameter is determined by device characteristics but is not production tested.
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V .

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7015 S		7015 L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

NOTES:
At V_{CC} = 2.0V, Input leakages are undefined.

2954 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7015X15 COM'L ONLY Typ.[2]	7015X15 COM'L ONLY Max.	7015X17 COM'L ONLY Typ.[2]	7015X17 COM'L ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	—	—	mA
				L	—	—	—	—	
			COM'L.	S	170	310	170	310	
				L	170	260	170	260	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	—	—	mA
				L	—	—	—	—	
			COM'L.	S	25	60	25	60	
				L	25	50	25	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A"=V_{IL} and $\overline{CE}$"B" = V_{IH}[5] Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	MIL.	S	—	—	—	—	mA
				L	—	—	—	—	
			COM'L.	S	105	190	105	190	
				L	105	160	109	160	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V	MIL.	S	—	—	—	—	mA
				L	—	—	—	—	
			COM'L.	S	1.0	15	1.0	15	
				L	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{CC} - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	—	—	mA
				L	—	—	—	—	
			COM'L.	S	100	170	100	170	
				L	100	140	100	140	

NOTES:
1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA(typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite of port "A".

2954 tbl 09

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7015X20 Typ.[2]	7015X20 Max.	7015X25 Typ.[2]	7015X25 Max.	7015X35 Typ.[2]	7015X35 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ = V_{IL}, Outputs Open; $\overline{SEM}$ = V_{IH}; f = f_{MAX}[3]	MIL.	S	—	—	155	340	150	300	mA
				L	—	—	155	280	150	250	
			COM'L.	S	160	290	155	265	150	250	
				L	160	240	155	220	150	210	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH}; $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}; f = f_{MAX}[3]	MIL.	S	—	—	16	80	13	80	mA
				L	—	—	16	65	13	65	
			COM'L.	S	20	60	16	60	13	60	
				L	20	50	16	50	13	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_{"A"}$=V_{IL} and $\overline{CE}_{"B"}$=V_{IH}[5]; Active Port Outputs Open; f = f_{MAX}[3]; $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	MIL.	S	—	—	90	215	85	190	mA
				L	—	—	90	180	85	160	
			COM'L.	S	95	180	90	170	85	155	
				L	95	150	90	140	85	130	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V; V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4]; $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	MIL.	S	—	—	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	1.0	15	
				L	0.2	5	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{CC} - 0.2V[5]; $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	MIL.	S	—	—	85	200	80	175	mA
				L	—	—	85	170	80	150	
		V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V; Active Port Outputs Open, f = f_{MAX}[3]	COM'L.	S	90	155	85	145	80	135	
				L	90	130	85	120	80	110	

NOTES:

2954 tbl 10

1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA(typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/ tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite of port "A".

OUTPUT LOADS AND AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figure 1 & 2

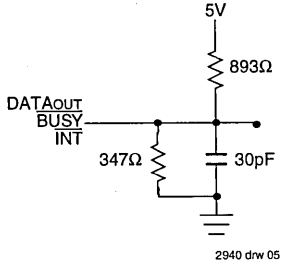


Figure 1. AC Output Test Load

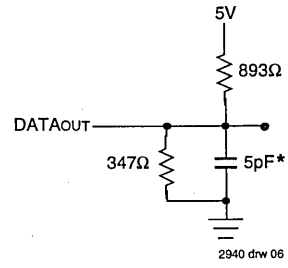


Figure 2. Output Test Load (For t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}) Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

Symbol	Parameter	IDT7015X15 COM'L ONLY Min.	IDT7015X15 COM'L ONLY Max.	IDT7015X17 COM'L ONLY Min.	IDT7015X17 COM'L ONLY Max.	Unit
READ CYCLE						
tRC	Read Cycle Time	15	—	17	—	ns
tAA	Address Access Time	—	15	—	17	ns
tACE	Chip Enable Access Time[3]	—	15	—	17	ns
tAOE	Output Enable Access Time	—	10	—	10	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
tLZ	Output Low-Z Time[1, 2]	3	—	3	—	ns
tHZ	Output High-Z Time[1, 2]	—	10	—	10	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	15	—	17	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	ns
tSAA	Semaphore Address Access Time	—	15	—	17	ns

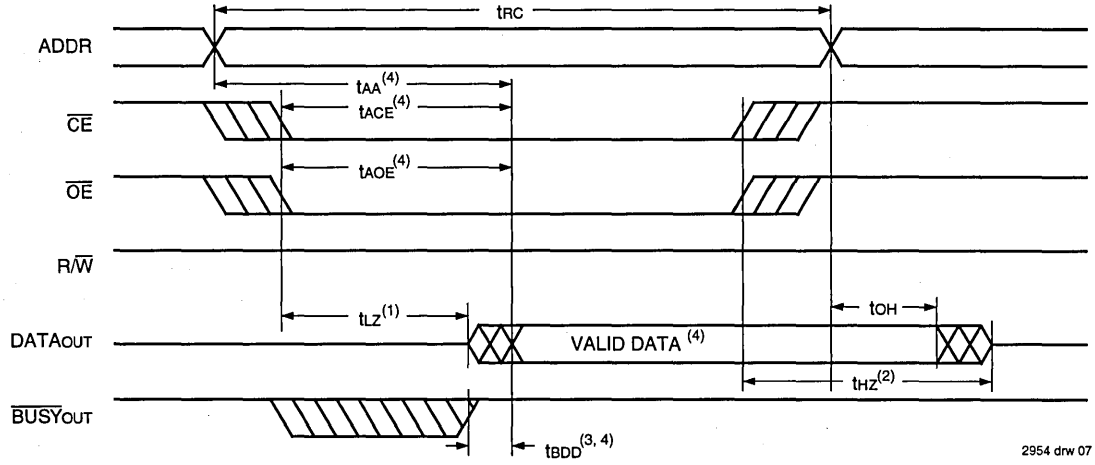
Symbol	Parameter	IDT7015X20 Min.	IDT7015X20 Max.	IDT7015X25 Min.	IDT7015X25 Max.	IDT7015X35 Min.	IDT7015X35 Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	20	—	25	—	35	—	ns
tAA	Address Access Time	—	20	—	25	—	35	ns
tACE	Chip Enable Access Time[3]	—	20	—	25	—	35	ns
tAOE	Output Enable Access Time	—	12	—	13	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time[1, 2]	3	—	3	—	3	—	ns
tHZ	Output High-Z Time[1, 2]	—	12	—	15	—	20	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	20	—	25	—	35	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	15	—	ns
tSAA	Semaphore Address Access Time	—	20	—	25	—	35	ns

NOTES:
1. Transition is measured ±500mV from low- or high-impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIN and $\overline{SEM}$ = VIL.
4. "X" in part numbers indicates power rating (S or L).

2954 tbl 11

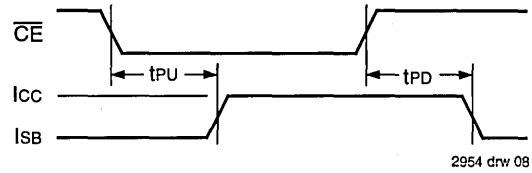
6

WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{CE}$ or $\overline{OE}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

TIMING OF POWER-UP / POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[5]

Symbol	Parameter	IDT7015X15 COM'L ONLY Min.	IDT7015X15 COM'L ONLY Max	IDT7015X17 COM'L ONLY Min.	IDT7015X17 COM'L ONLY Max.	Unit
WRITE CYCLE						
t_{WC}	Write Cycle Time	15	—	17	—	ns
t_{EW}	Chip Enable to End-of-Write[3]	12	—	12	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	12	—	ns
t_{AS}	Address Set-up Time[3]	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	12	—	ns
t_{WR}	Write Recovery Time	2	—	2	—	ns
t_{DW}	Data Valid to End-of-Write	12	—	10	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	10	—	10	ns
t_{DH}	Data Hold Time[4]	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1, 2]	—	10	—	10	ns
t_{OW}	Output Active from End-of-Write[1, 2, 4]	3	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	ns

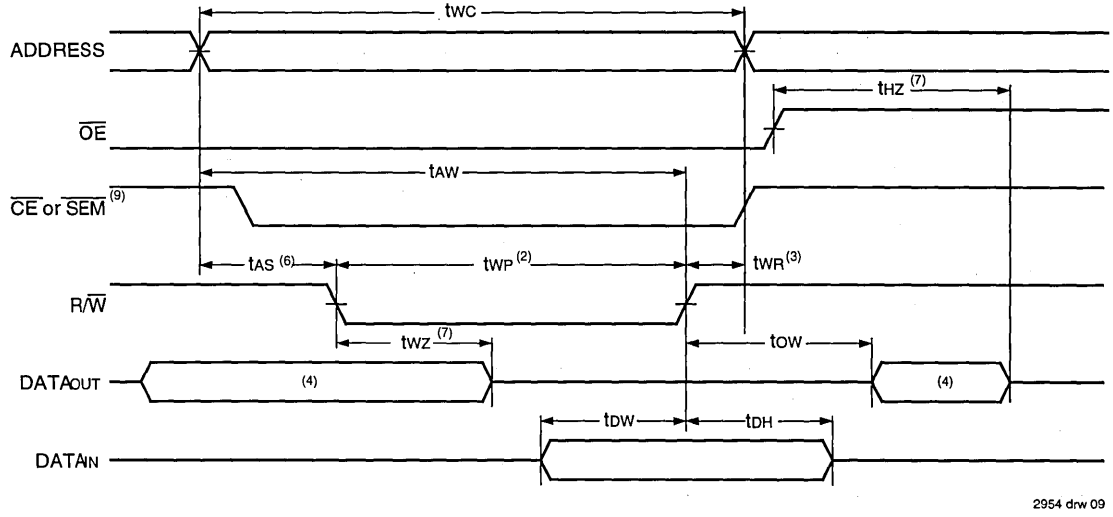
Symbol	Parameter	IDT7015X20 Min.	IDT7015X20 Max.	IDT7015X25 Min.	IDT7015X25 Max.	IDT7015X35 Min.	IDT7015X35 Max.	Unit
WRITE CYCLE								
t_{WC}	Write Cycle Time	20	—	25	—	35	—	ns
t_{EW}	Chip Enable to End-of-Write[3]	15	—	20	—	30	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	30	—	ns
t_{AS}	Address Set-up Time[3]	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	25	—	ns
t_{WR}	Write Recovery Time	2	—	2	—	2	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	15	—	15	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	12	—	15	—	20	ns
t_{DH}	Data Hold Time[4]	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1, 2]	—	12	—	15	—	20	ns
t_{OW}	Output Active from End-of-Write[1, 2, 4]	3	—	3	—	3	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

NOTES:

2954 tbl 12

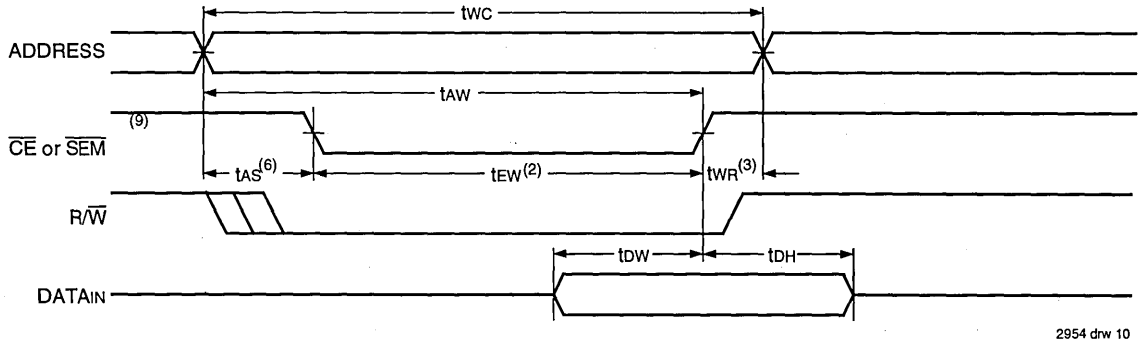
1. Transition is measured ±500mV from low - or high-impedance voltage with the output test load (Figure 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,5,8)



2954 drw 09

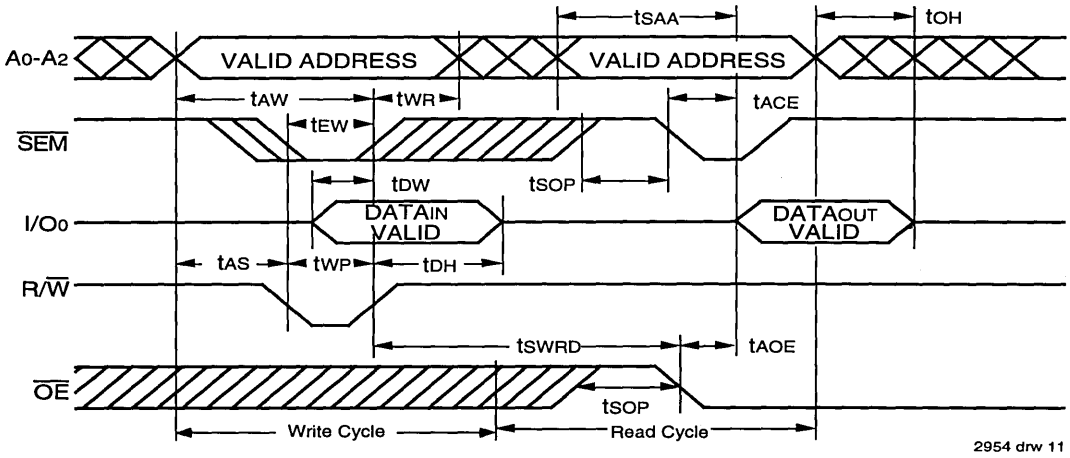
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,5)



2954 drw 10

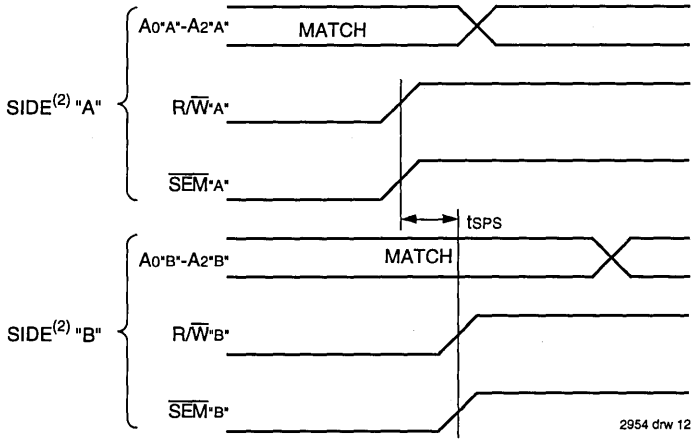
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization but is not production tested, transition is measured +/-200mV from steady state with the Output Test load (Figure 2).
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t WP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t WP.
9. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access Semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. tEW must be met for either condition.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL =VIH, $\overline{CE}_R$ = $\overline{CE}_L$ =VIH.
2. All timing is the same for left and right ports. Port"A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/$\overline{W}_A$ or $\overline{SEM}_A$ going high to R/$\overline{W}_B$ or $\overline{SEM}_B$ going High.
4. If tSPS is not satisfied, there is no guarantee which side will obtain the semaphore flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(6)

Symbol	Parameter	IDT7015X15 COM'L ONLY Min.	IDT7015X15 COM'L ONLY Max.	IDT7015X17 COM'L ONLY Min.	IDT7015X17 COM'L ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)						
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	15	—	17	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	15	—	17	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	15	—	17	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	15	—	17	ns
tAPS	Arbitration Priority Set-up Time(2)	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data(3)	—	15	—	17	ns
BUSY TIMING (M/$\overline{S}$ = L)						
tWB	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$(5)	13	—	13	—	ns
PORT-TO-PORT DELAY TIMING						
tWDD	Write Pulse to Data Delay(1)	—	30	—	30	ns
tDDD	Write Data Valid to Read Data Delay(1)	—	25	—	25	ns

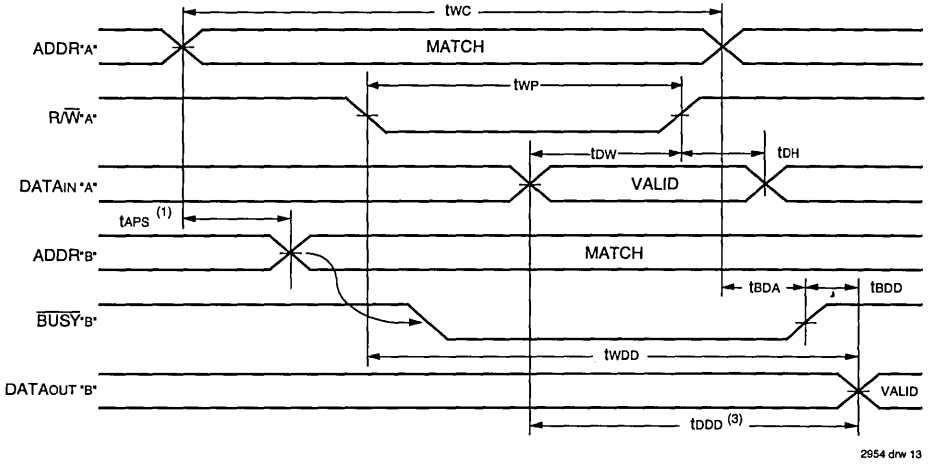
Symbol	Parameter	IDT7015X20 Min.	IDT7015X20 Max.	IDT7015X25 Min.	IDT7015X25 Max.	IDT7015X35 Min.	IDT7015X35 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	20	—	20	—	20	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	20	—	20	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	20	—	20	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	17	—	17	—	20	ns
tAPS	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data(3)	—	20	—	25	—	35	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$(5)	15	—	17	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay(1)	—	45	—	50	—	60	ns
tDDD	Write Data Valid to Read Data Delay(1)	—	30	—	35	—	45	ns

NOTES:

2940 tbl 13

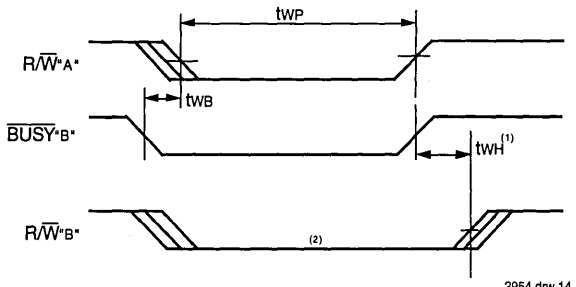
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Wave form of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = VIH)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[2] (M/$\overline{S}$ = V_{IH})



NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for M/$\overline{S}$=VIL
2. $\overline{CE}_L$ = $\overline{CE}_R$ = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. If M/$\overline{S}$=VIL (SLAVE), the $\overline{BUSY}$ is an input ($\overline{BUSY}$=VIH). For this example, $\overline{BUSY}$="don't care".
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

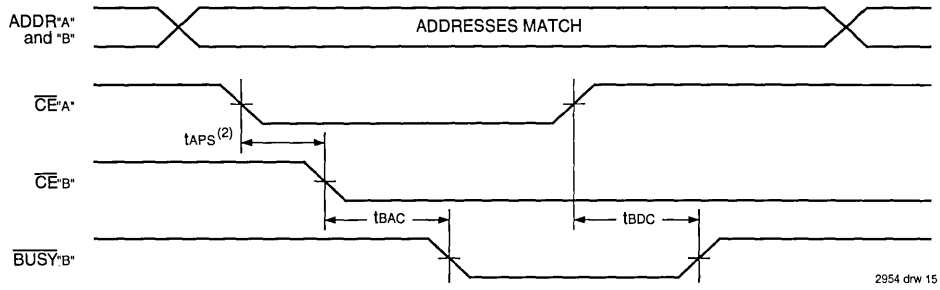
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$



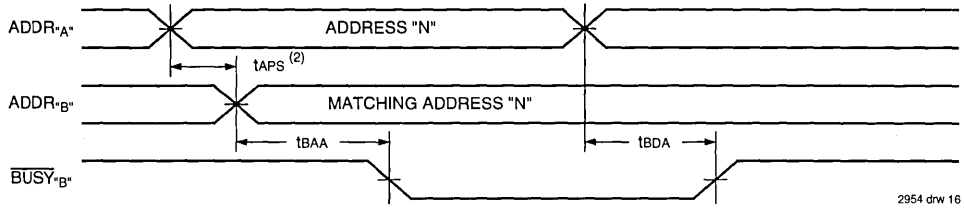
NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (SLAVE) and output (MASTER).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes High.

6

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING[1] ($M/\overline{S}$ = V_{IH})



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING[1] ($M/\overline{S}$ = V_{IH})



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

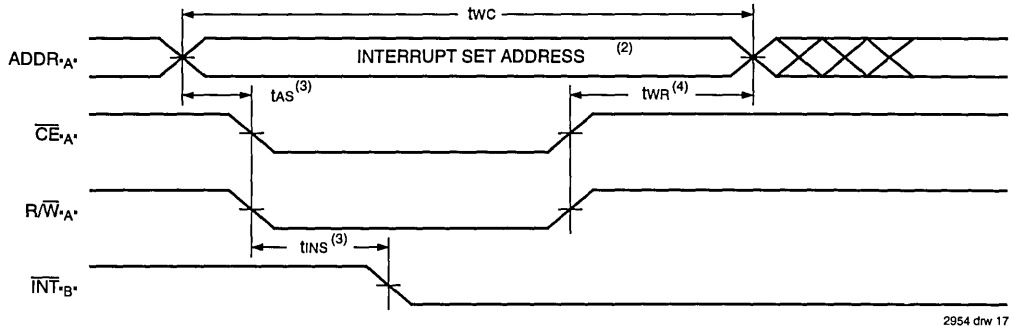
Symbol	Parameter	IDT7015X15 COM'L ONLY Min.	IDT7015X15 COM'L ONLY Max.	IDT7015X17 COM'L ONLY Min	IDT7015X17 COM'L ONLY Max.	Unit
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	15	—	17	ns
tINR	Interrupt Reset Time	—	15	—	17	ns

Symbol	Parameter	IDT7015X20 Min.	IDT7015X20 Max.	IDT7015X25 Min.	IDT7015X25 Max.	IDT7015X35 Min.	IDT7015X35 Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	20	—	25	ns
tINR	Interrupt Reset Time	—	20	—	20	—	25	ns

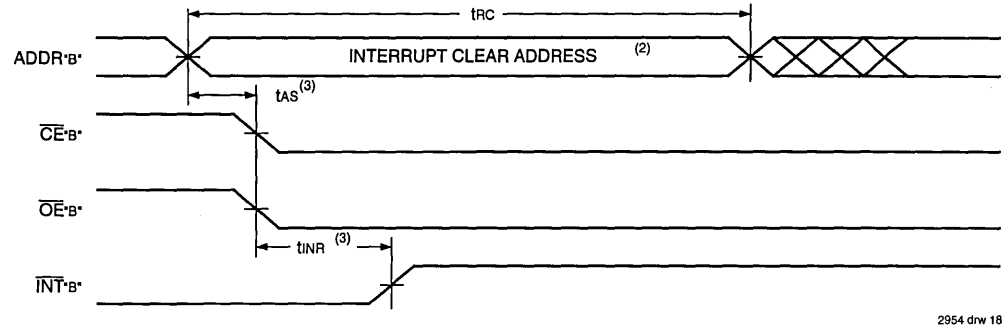
NOTE:
1. "X" in part numbers indicates power rating (S or L).

2739 tbl 14

WAVEFORM OF INTERRUPT TIMING[1]



2954 drw 17



2954 drw 18

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

6

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
R/$\overline{W}$L	$\overline{CE}$L	$\overline{OE}$L	A12L-A0L	$\overline{INT}$L	R/$\overline{W}$R	$\overline{CE}$R	$\overline{OE}$R	A12R-A0R	$\overline{INT}$R	Function
L	L	X	1FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}$R Flag
X	X	X	X	X	X	L	L	1FFF	H[3]	Reset Right $\overline{INT}$R Flag
X	X	X	X	L[3]	L	L	X	1FFE	X	Set Left $\overline{INT}$L Flag
X	L	L	1FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}$L Flag

NOTES:
1. Assumes $\overline{BUSY}$L = $\overline{BUSY}$R = VIH.
2. If $\overline{BUSY}$L = VIL, then no change.
3. If $\overline{BUSY}$R = VIL, then no change.

2954 tbl 15

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{12L} A_{0R}-A_{12R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

NOTES: 2954 tbl 16

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}_X$ outputs on the IDT7015 are push-pull, not open drain outputs. On slaves the $\overline{BUSY}_X$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_8 Left	D_0 - D_8 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2954 tbl 17

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7015.

FUNCTIONAL DESCRIPTION

The IDT7015 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7015 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ High). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 1FFE where a write is defined as the $\overline{CE}$ = R/$\overline{W}$ = V_{IL} per the Truth Table. The left port clears the interrupt by an address location 1FFE access when $\overline{CE}_R$ =$\overline{OE}_R$ =V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 1FFF and to clear the interrupt flag ($\overline{INT}_R$), the right port must access memory location 1FFF. The message (9 bits) at 1FFE or 1FFF isuser-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes but are still part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all

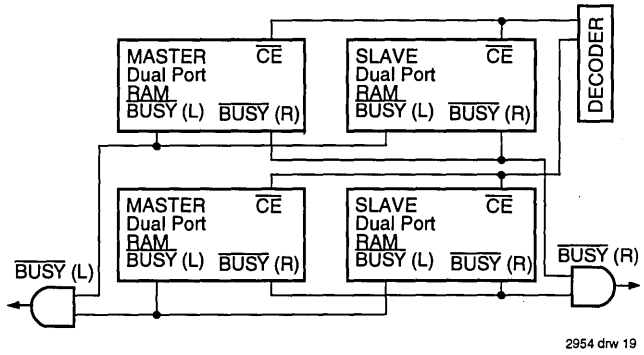


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7015 RAMs.

applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT7015 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7015 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7015 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with the R/$\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7015 are extremely fast Dual-Port 8Kx9 Static RAMs with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7015 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7015's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

6

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7015 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7015 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a

resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7015's Dual-Port RAM. Say the 8K x 9 RAM was to be divided into two 4K x 9 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

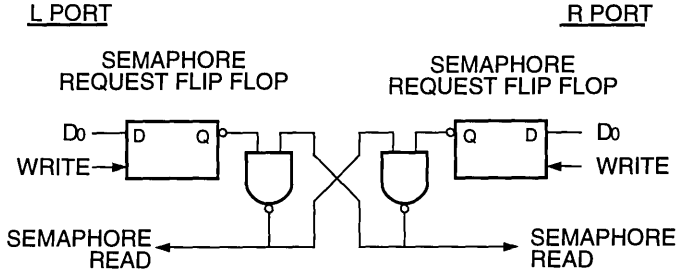
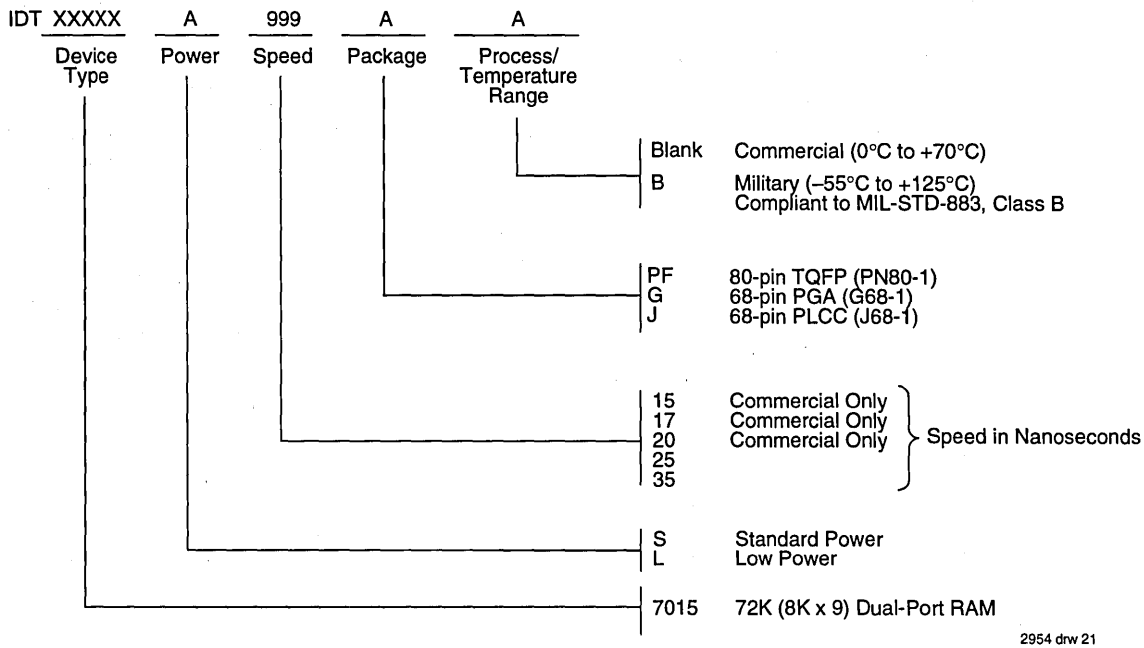


Figure 4. IDT7015/7016 Semaphore Logic

ORDERING INFORMATION



2954 drw 21

Integrated Device Technology, Inc.

HIGH-SPEED 16K x 9 DUAL-PORT STATIC RAM

PRELIMINARY IDT7016S/L

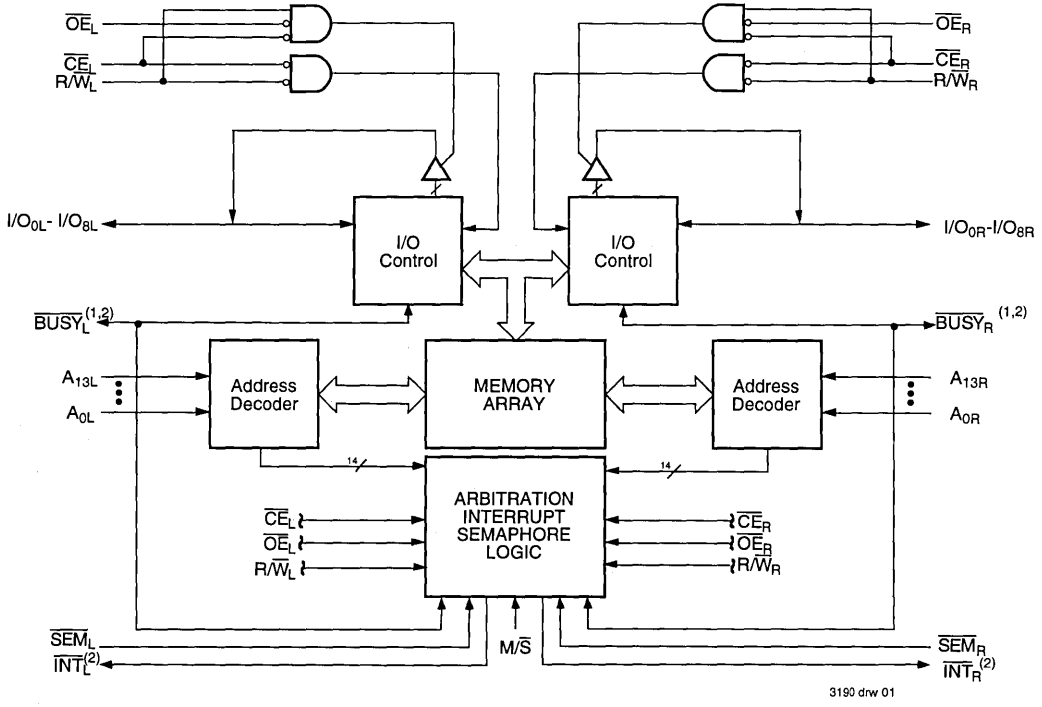
FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 25/35ns (max.)
  - — Commercial:15/17/20/25/35ns (max.)
- Low-power operation
  - — IDT7016S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7016L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- IDT7016 easily expands data bus width to 18 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Devices are capable of withstanding greater than 2001V electrostatic discharge
- TTL-compatible, single 5V (±10%) power supply
- Available in ceramic 68-pin PGA, 68-pin PLCC, and an 80-pin TQFP
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7016 is a high-speed 16K x 9 Dual-Port Static RAMs. The IDT7016 is designed to be used as stand-alone 144K bit Dual-Port RAMs or as a combination MASTER/SLAVE Dual-Port RAM for 18-bit-or-more word systems.

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. In MASTER mode: $\overline{BUSY}$ is an output and is a push-pull driver
   In SLAVE mode: $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ outputs and $\overline{INT}$ outputs are non-tristated push-pull drivers.

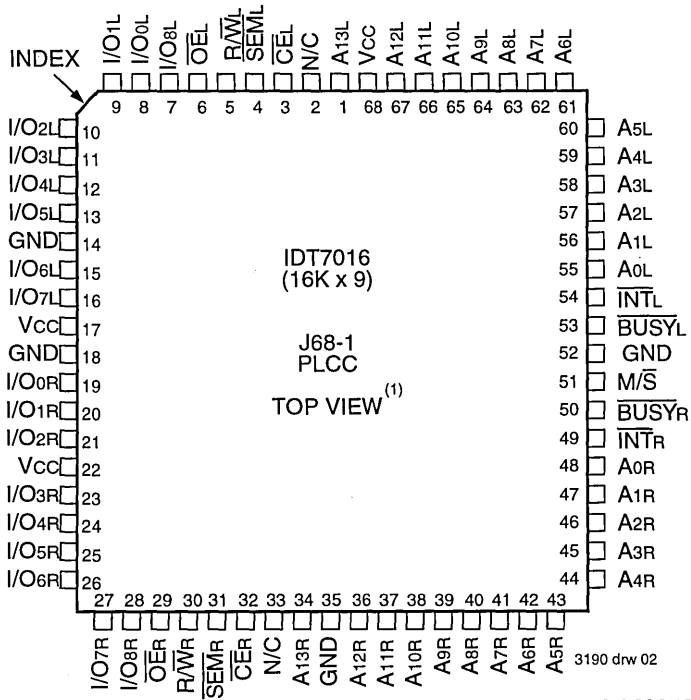
Using the IDT MASTER/SLAVE Dual-Port RAM approach in 18-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power.

The IDT7016 is packaged in a ceramic 68-pin PGA, a 64-pin PLCC and an 80-pinTQFP (Thin Quad FlatPack). Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



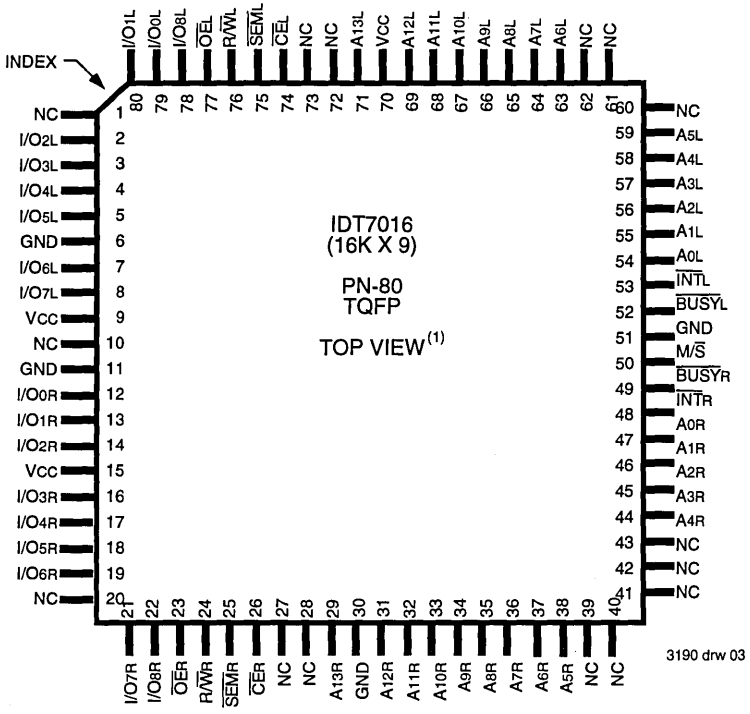
PIN NAMES (7016)

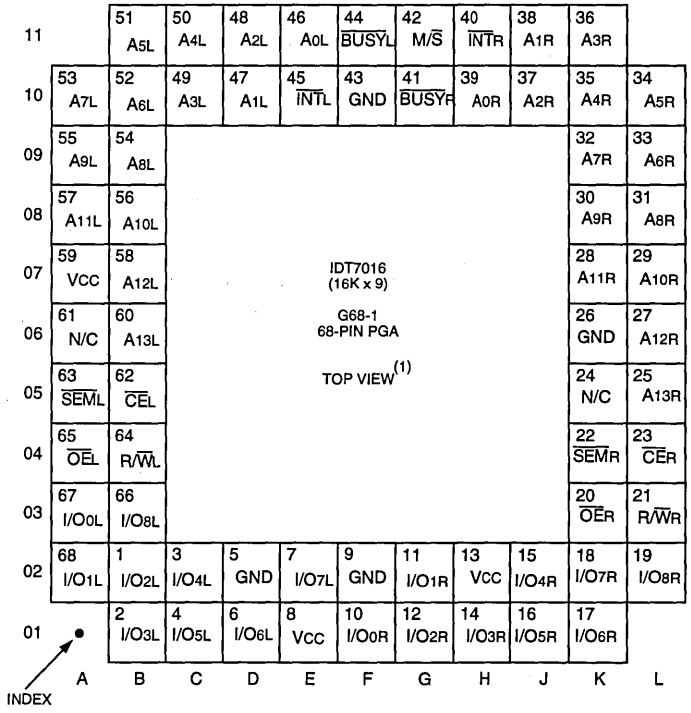
Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{13L}$	$A_{0R} - A_{13R}$	Address
$I/O_{0L} - I/O_{8L}$	$I/O_{0R} - I/O_{8R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}(1)		Power
GND(2)		Ground

3190 tbl 01

NOTES:
1. This text does not imply orientation of Part-Mark.

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.





NOTES:
1. This text does not imply orientation of Part-Mark.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-8	Mode
H	X	X	H	High-Z	Deselected: Power-Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read Memory
X	X	H	X	High-Z	Outputs Disabled

NOTE:
1. Condition: A0L — A13L is not equal to A0R — A13R

3190 tbl 02

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-8	Mode
H	H	L	L	DATAOUT	Read Semaphore Flag Data Out
H	↑	X	L	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	—	Not Allowed

3190 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 0.5V.

3190 tbl 04

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

3190 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTES:
1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

3190 tbl 06

CAPACITANCE (T_A = +25°C, f = 1.0MHz, for TQFP Package)[1]

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

3190 tbl 07

NOTES:
1. This parameter is determined by device characteristics but is not production tested.
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V .

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7016 S		7016 L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

NOTES:
At V_{CC} = 2.0V, Input leakages are undefined.

3190 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7016X15 COM'L ONLY Typ.[2]	7016X15 COM'L ONLY Max.	7016X17 COM'L ONLY Typ.[2]	7016X17 COM'L ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	—	—	mA
				L	—	—	—	—	
			COM'L.	S	170	310	170	310	
				L	170	260	170	260	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	—	—	mA
				L	—	—	—	—	
			COM'L.	S	25	60	25	60	
				L	25	50	25	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_{"A"}$=V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	MIL.	S	—	—	—	—	mA
				L	—	—	—	—	
			COM'L.	S	105	190	105	190	
				L	105	160	109	160	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	MIL.	S	—	—	—	—	mA
				L	—	—	—	—	
			COM'L.	S	1.0	15	1.0	15	
				L	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{CC} - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	—	—	mA
				L	—	—	—	—	
			COM'L.	S	100	170	100	170	
				L	100	140	100	140	

NOTES:
1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA(typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite of port "A".

3190 tbl 09

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7016X20 Typ.[2]	7016X20 Max.	7016X25 Typ.[2]	7016X25 Max.	7016X35 Typ.[2]	7016X35 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	155	340	150	300	mA
				L	—	—	155	280	150	250	
			COM'L.	S	160	290	155	265	150	250	
				L	160	240	155	220	150	210	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE_L}$ = $\overline{CE_R}$ = V_{IH} $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	16	80	13	80	mA
				L	—	—	16	65	13	65	
			COM'L.	S	20	60	16	60	13	60	
				L	20	50	16	50	13	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A"=V_{IL} and $\overline{CE}$"B"=V_{IH}[5] Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH}	MIL.	S	—	—	90	215	85	190	mA
				L	—	—	90	180	85	160	
			COM'L.	S	95	180	90	170	85	155	
				L	95	150	90	140	85	130	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM_R}$ = $\overline{SEM_L}$ ≥ V_{CC} - 0.2V	MIL.	S	—	—	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	1.0	15	
				L	0.2	5	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A"≤ 0.2V and $\overline{CE}$"B" ≥ V_{CC} - 0.2V[5] $\overline{SEM_R}$ = $\overline{SEM_L}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	85	200	80	175	mA
				L	—	—	85	170	80	150	
			COM'L.	S	90	155	85	145	80	135	
				L	90	130	85	120	80	110	

NOTES:

3190 tbl 10

1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA(typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite of port "A".

OUTPUT LOADS AND AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figure 1 & 2

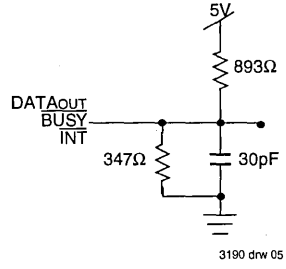


Figure 1. AC Output Test Load

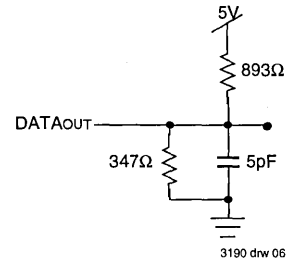


Figure 2. Output Test Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW}) Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

Symbol	Parameter	IDT7016X15 COM'L ONLY Min.	IDT7016X15 COM'L ONLY Max.	IDT7016X17 COM'L ONLY Min.	IDT7016X17 COM'L ONLY Max.	Unit
READ CYCLE						
t_{RC}	Read Cycle Time	15	—	17	—	ns
t_{AA}	Address Access Time	—	15	—	17	ns
t_{ACE}	Chip Enable Access Time[3]	—	15	—	17	ns
t_{AOE}	Output Enable Access Time	—	10	—	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1, 2]	3	—	3	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	10	—	10	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	15	—	17	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	ns
t_{SAA}	Semaphore Address Access Time	—	15	—	17	ns

Symbol	Parameter	IDT7016X20 Min.	IDT7016X20 Max.	IDT7016X25 Min.	IDT7016X25 Max.	IDT7016X35 Min.	IDT7016X35 Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACE}	Chip Enable Access Time[3]	—	20	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	12	—	13	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1, 2]	3	—	3	—	3	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	12	—	15	—	20	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	20	—	25	—	35	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	15	—	ns
t_{SAA}	Semaphore Address Access Time	—	20	—	25	—	35	ns

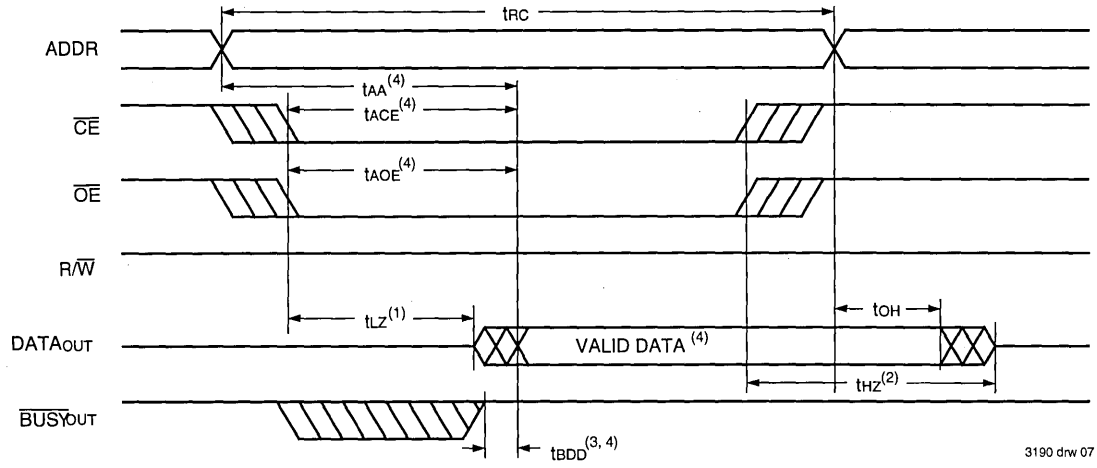
NOTES:

3190 tbl 11

1. Transition is measured ±500mV from low- or high-impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IN} and $\overline{SEM}$ = V_{IL}.
4. "X" in part numbers indicates power rating (S or L).

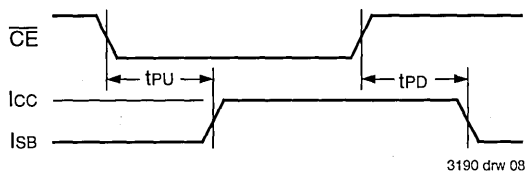
6

WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{CE}$ or $\overline{OE}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

TIMING OF POWER-UP / POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[5]

Symbol	Parameter	IDT7016X15 COM'L ONLY Min.	IDT7016X15 COM'L ONLY Max	IDT7016X17 COM'L ONLY Min.	IDT7016X17 COM'L ONLY Max.	Unit
WRITE CYCLE						
tWC	Write Cycle Time	15	—	17	—	ns
tEW	Chip Enable to End-of-Write[3]	12	—	12	—	ns
tAW	Address Valid to End-of-Write	12	—	12	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	ns
tWP	Write Pulse Width	12	—	12	—	ns
tWR	Write Recovery Time	2	—	2	—	ns
tDW	Data Valid to End-of-Write	12	—	10	—	ns
tHZ	Output High-Z Time[1, 2]	—	10	—	10	ns
tDH	Data Hold Time[4]	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	10	—	10	ns
tOW	Output Active from End-of-Write[1, 2, 4]	3	—	3	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	ns

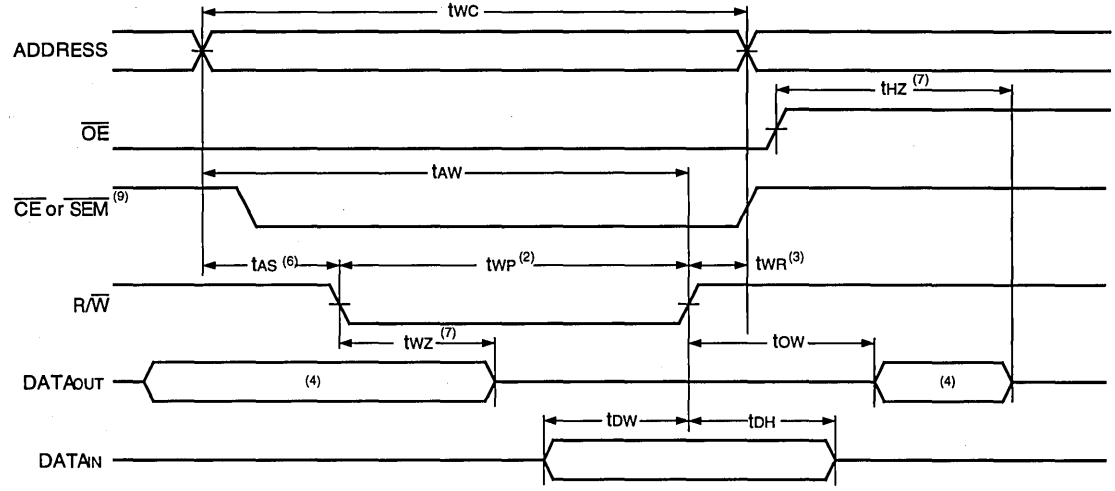
Symbol	Parameter	IDT7016X20 Min.	IDT7016X20 Max.	IDT7016X25 Min.	IDT7016X25 Max.	IDT7016X35 Min.	IDT7016X35 Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time	20	—	25	—	35	—	ns
tEW	Chip Enable to End-of-Write[3]	15	—	20	—	30	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	30	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	ns
tWR	Write Recovery Time	2	—	2	—	2	—	ns
tDW	Data Valid to End-of-Write	15	—	15	—	15	—	ns
tHZ	Output High-Z Time[1, 2]	—	12	—	15	—	20	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	12	—	15	—	20	ns
tOW	Output Active from End-of-Write[1, 2, 4]	3	—	3	—	3	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

3190 tbl 12

NOTES:

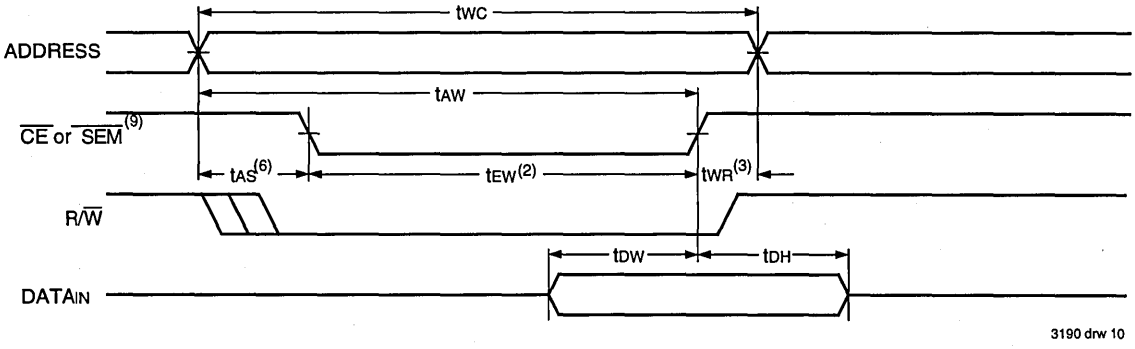
1. Transition is measured ±500mV from low - or high-impedance voltage with the output test load (Figure 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,5,8)



3190 drw 09

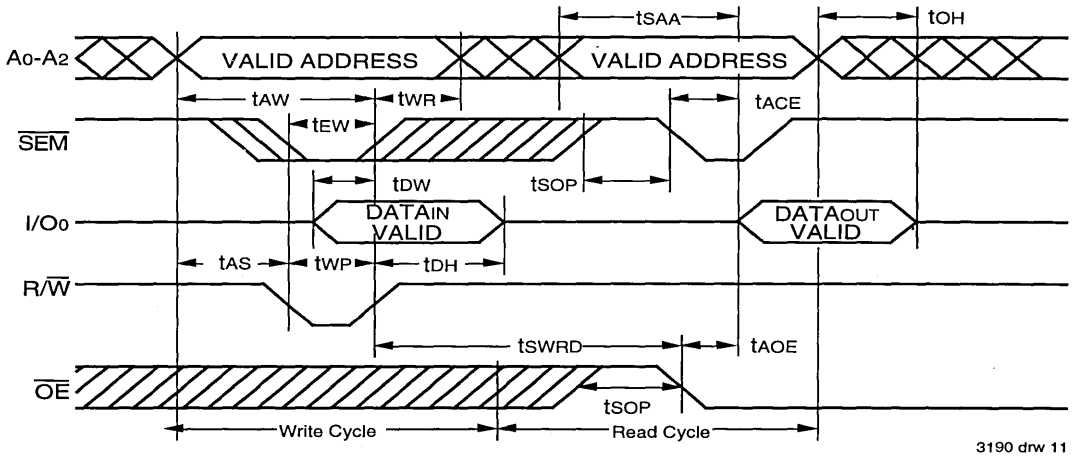
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,5)



3190 drw 10

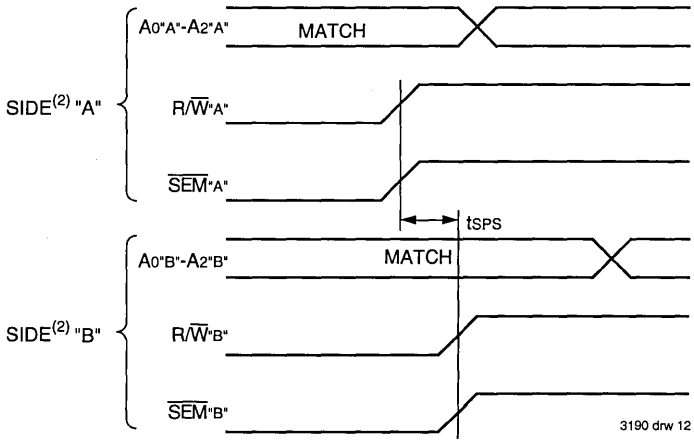
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization but is not production tested, transition is measured +/-200mV from steady state with the Output Test load (Figure 2).
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t WP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t WP.
9. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access Semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. tEW must be met for either condition.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL =VIH, $\overline{CE}_R$ = $\overline{CE}_L$ =VIH.
2. All timing is the same for left and right ports. Port"A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/$\overline{W}_A$ or $\overline{SEM}_A$ going high to R/$\overline{W}_B$ or $\overline{SEM}_B$ going High.
4. If tSPS is not satisfied, there is no guarantee which side will obtain the semaphore flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

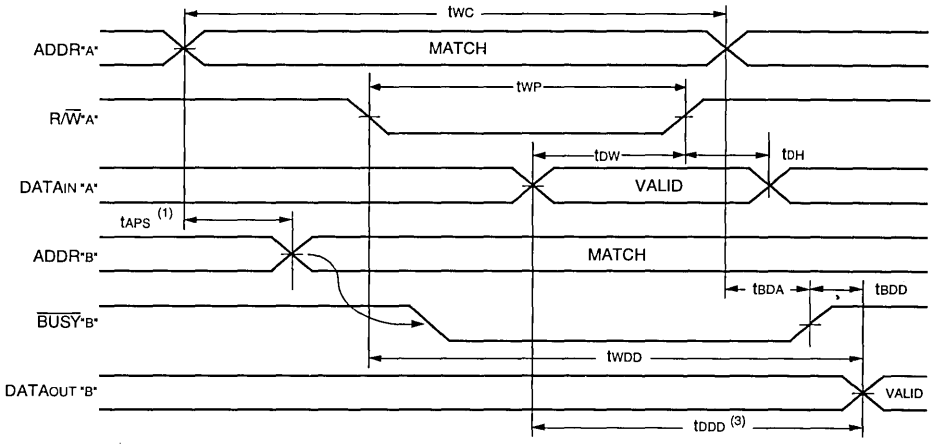
Symbol	Parameter	IDT7016X15 COM'L ONLY Min.	IDT7016X15 COM'L ONLY Max.	IDT7016X17 COM'L ONLY Min.	IDT7016X17 COM'L ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)						
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	15	—	17	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	15	—	17	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	15	—	17	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	15	—	17	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	15	—	17	ns
BUSY TIMING (M/$\overline{S}$ = L)						
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	13	—	13	—	ns
PORT-TO-PORT DELAY TIMING						
tWDD	Write Pulse to Data Delay[1]	—	30	—	30	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	25	—	25	ns

Symbol	Parameter	IDT7016X20 Min.	IDT7016X20 Max.	IDT7016X25 Min.	IDT7016X25 Max.	IDT7016X35 Min.	IDT7016X35 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	20	—	20	—	20	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	20	—	20	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	20	—	20	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	17	—	17	—	20	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	20	—	25	—	35	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	15	—	17	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	45	—	50	—	60	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	30	—	30	—	35	ns

2940 tbl 13

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveformof Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = VIH)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. "X" in part numbers indicates power rating (S or L).

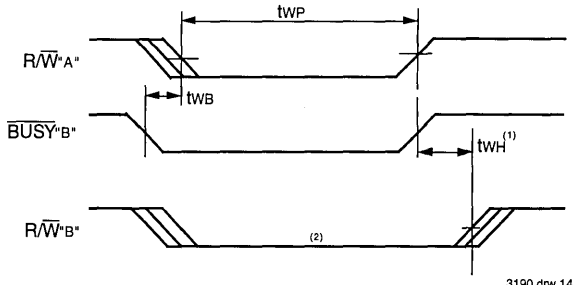
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$(2) (M/$\overline{S}$ = V_{IH})



3190 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for M/$\overline{S}$=VIL
2. $\overline{CE}_L$ = $\overline{CE}_R$ = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. If M/$\overline{S}$=VIL (SLAVE), the $\overline{BUSY}$ is an input ($\overline{BUSY}$=VIH). For this example, $\overline{BUSY}$="don't care".
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$

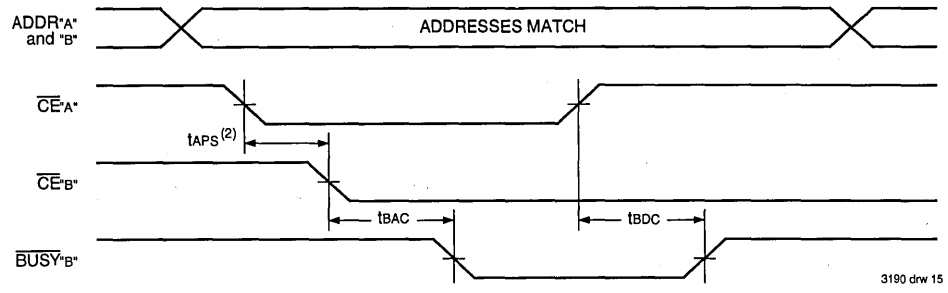


3190 drw 14

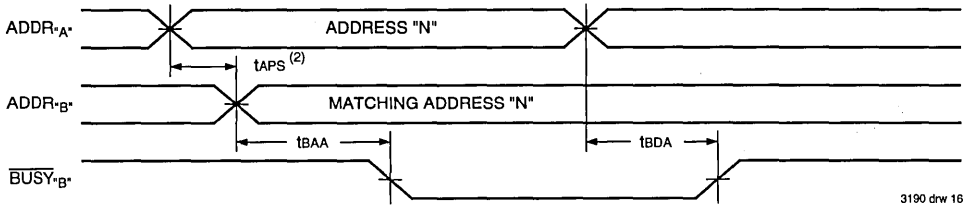
NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (SLAVE) and output (MASTER).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes High.

6

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING[1] ($M/\overline{S}$ = V_{IH})



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING[1] ($M/\overline{S}$ = V_{IH})



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

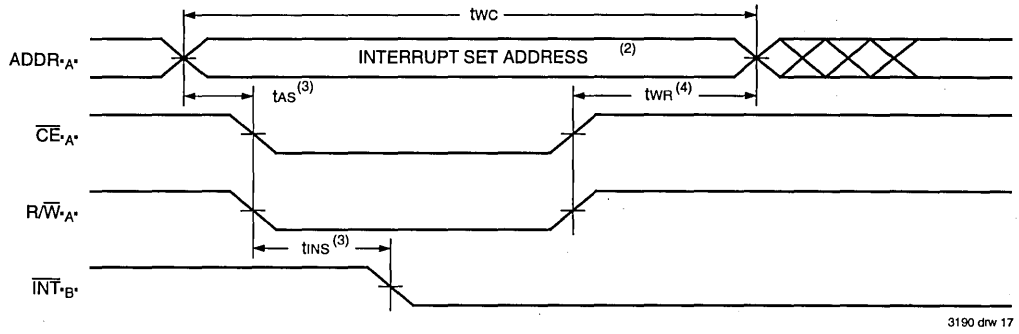
Symbol	Parameter	IDT7016X15 COM'L ONLY Min.	IDT7016X15 COM'L ONLY Max.	IDT7016X17 COM'L ONLY Min	IDT7016X17 COM'L ONLY Max.	Unit
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	15	—	17	ns
tINR	Interrupt Reset Time	—	15	—	17	ns

Symbol	Parameter	IDT7016X20 Min.	IDT7016X20 Max.	IDT7016X25 Min.	IDT7016X25 Max.	IDT7016X35 Min.	IDT7016X35 Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	20	—	25	ns
tINR	Interrupt Reset Time	—	20	—	20	—	25	ns

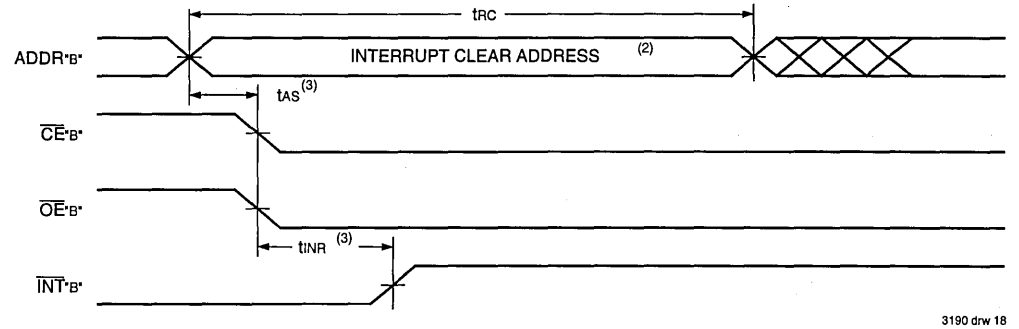
NOTE:
1. "X" in part numbers indicates power rating (S or L).

2739 tbl 14

WAVEFORM OF INTERRUPT TIMING[1]



3190 drw 17



3190 drw 18

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{13L}-A_{0L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{13R}-A_{0R}	$\overline{INT}_R$	Function
L	L	X	3FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	3FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

3190 tbl 15

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = VIH.
2. If $\overline{BUSY}_L$ = VIL, then no change.
3. If $\overline{BUSY}_R$ = VIL, then no change.

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{13L} A_{0R}-A_{13R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

3190 tbl 16

NOTES:

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}x$ outputs on the IDT7016 are push-pull, not open drain outputs. On slaves the $\overline{BUSY}x$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_8 Left	D_0 - D_8 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

3190 tbl 17

NOTE:

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7016.

FUNCTIONAL DESCRIPTION

The IDT7016 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7016 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ High). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 3FFE where a write is defined as the $\overline{CE}$ = R/$\overline{W}$ = V_{IL} per the Truth Table. The left port clears the interrupt by an address location 3FFE access when $\overline{CE}_R$ =$\overline{OE}_R$ =V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 3FFF and to clear the interrupt flag ($\overline{INT}_R$), the right port must access memory location 3FFF. The message (9 bits) at 3FFE or 3FFF is user-defined since it is in an addressable SRAM location. If the interrupt function is not used, address locations 3FFE and 3FFF are not used as mail boxes but are still part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all

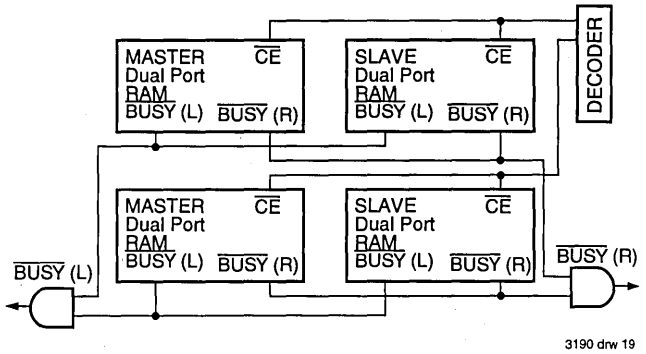


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7016 RAMs.

applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT7016 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7016 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7016 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with the R/$\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7016 are extremely fast Dual-Port 16Kx9 Static RAMs with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7016 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7016's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

6

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7016 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7016 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a

resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7016's Dual-Port RAM. Say the 16K x 9 RAM was to be divided into two 8K x 9 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 8K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

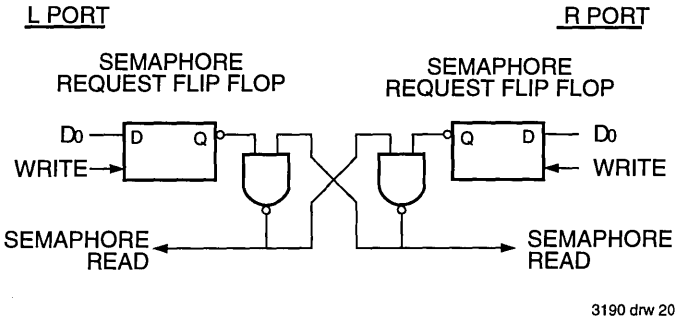
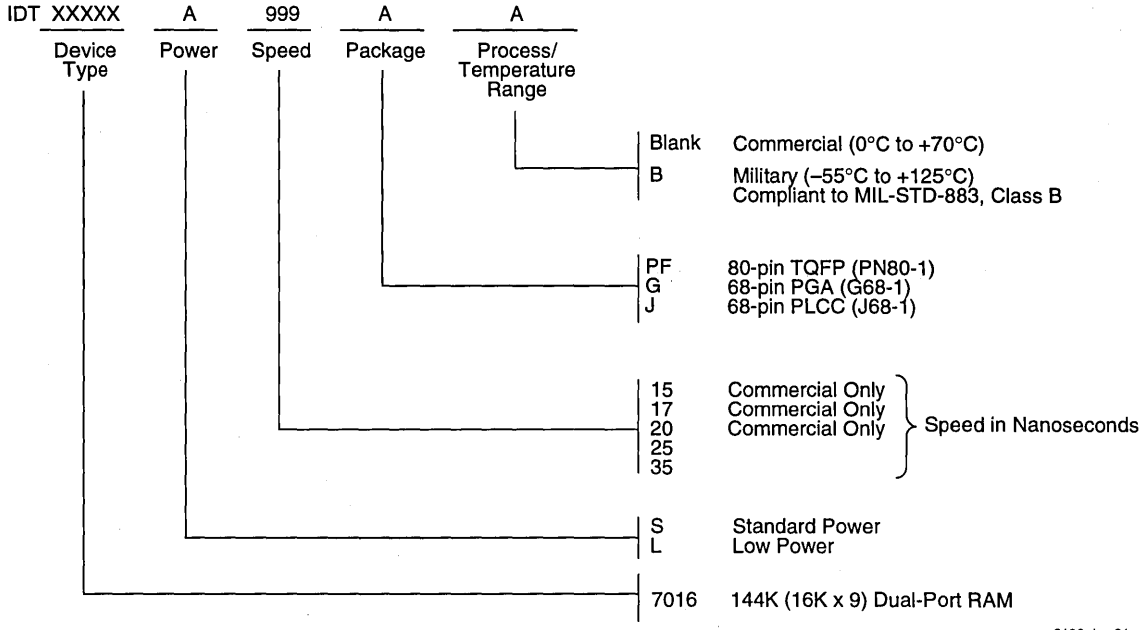


Figure 4. IDT7016 Semaphore Logic

ORDERING INFORMATION



3190 drw 21

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAMS 32K (2K x 16-BIT)

IDT7133SA/LA
IDT7143SA/LA

FEATURES:

- High-speed access
  - — Military: 35/45/55/70/90ns (max.)
  - — Commercial: 25/35/45/55/70/90ns (max.)
- Low-power operation
  - — IDT7133/43SA
    Active: 500 mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7133/43LA
    Active: 500mW (typ.)
    Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)
- $\overline{BUSY}$ output flag on IDT7133; $\overline{BUSY}$ input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in 68-pin ceramic PGA, Flatpack, and PLCC
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7133/7143 are high-speed 2K x 16 Dual-Port Static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7143 "SLAVE" Dual-Port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit-or-wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

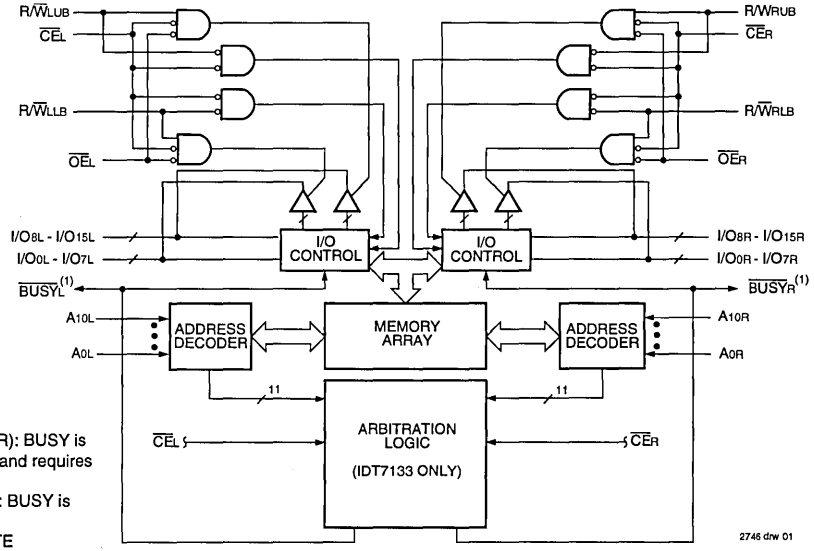
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 500mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200µW for a 2V battery.

The IDT7133/7143 devices have identical pinouts. Each is packed in a 68-pin ceramic PGA, 68-pin flatpack, and 68-pin PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

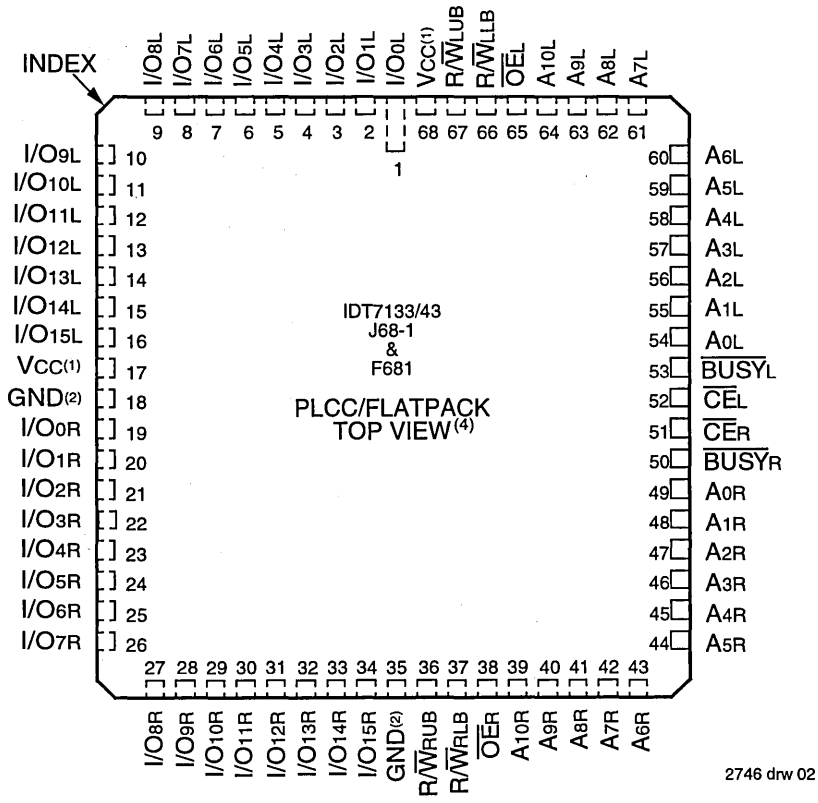
6

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. IDT7133 (MASTER): BUSY is open drain output and requires pull-up resistor.
   IDT7143 (SLAVE): BUSY is input.
2. LB = LOWER BYTE
3. UB = UPPER BYTE

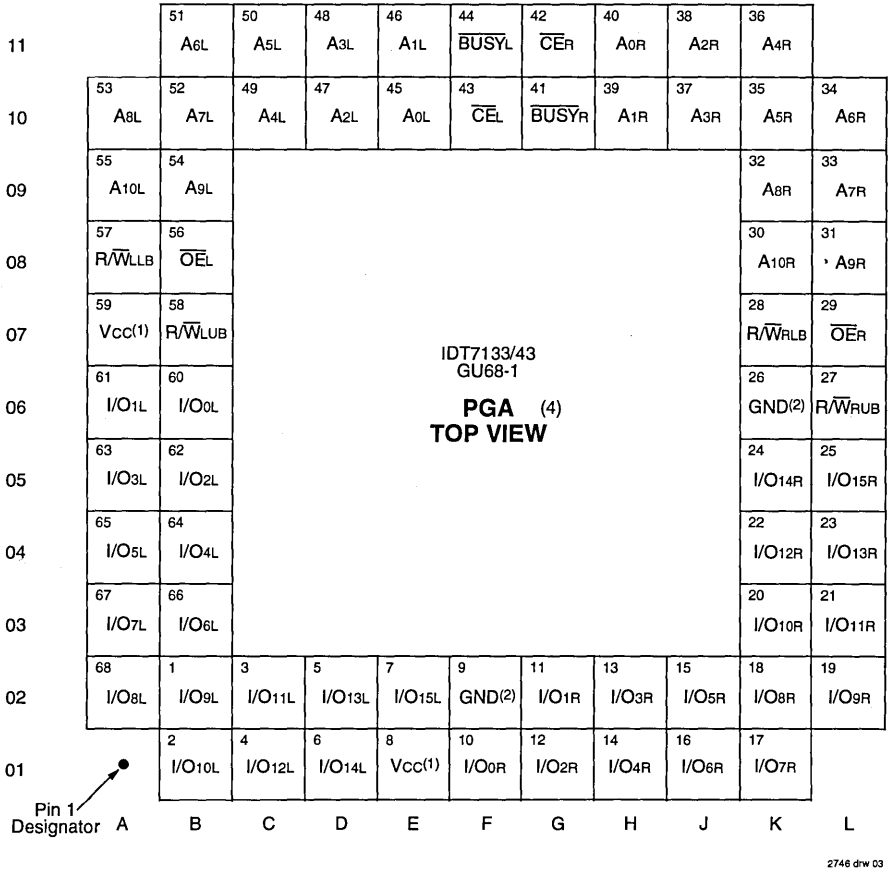
PIN CONFIGURATIONS[1,2,3]



2746 drw 02

NOTES:
1. Both Vcc pins must be connected to the supply to assure reliable operation.
2. Both GND pins must be connected to the supply to assure reliable operation.
3. UB = Upper Byte, LB = Lower Byte
4. - This text does not indicate orientation of the actual part-marking.

PIN CONFIGURATIONS (CONTINUED)[1,2,3]



	A	B	C	D	E	F	G	H	J	K	L
11		51 A6L	50 A5L	48 A3L	46 A1L	44 BUSYL	42 CER	40 A0R	38 A2R	36 A4R	
10	53 A8L	52 A7L	49 A4L	47 A2L	45 A0L	43 CEL	41 BUSYR	39 A1R	37 A3R	35 A5R	34 A6R
09	55 A10L	54 A9L								32 A8R	33 A7R
08	57 R/WLLB	56 OEL								30 A10R	31 A9R
07	59 VCC(1)	58 R/WLUB								28 R/WRLB	29 OER
06	61 I/O1L	60 I/O0L								26 GND(2)	27 R/WRUB
05	63 I/O3L	62 I/O2L								24 I/O14R	25 I/O15R
04	65 I/O5L	64 I/O4L								22 I/O12R	23 I/O13R
03	67 I/O7L	66 I/O6L								20 I/O10R	21 I/O11R
02	68 I/O8L	1 I/O9L	3 I/O11L	5 I/O13L	7 I/O15L	9 GND(2)	11 I/O1R	13 I/O3R	15 I/O5R	18 I/O8R	19 I/O9R
01		2 I/O10L	4 I/O12L	6 I/O14L	8 VCC(1)	10 I/O0R	12 I/O2R	14 I/O4R	16 I/O6R	17 I/O7R	

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_{LUB}$	$R/\overline{W}_{RUB}$	Upper Byte Read/Write Enable
$R/\overline{W}_{LLB}$	$R/\overline{W}_{RLB}$	Lower Byte Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{10L}$	$A_{0R} - A_{10R}$	Address
$I/O_{0L} - I/O_{15L}$	$I/O_{0R} - I/O_{15R}$	Data Input/Output
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
V_{CC}		Power
GND		Ground

2746 tbl 01

NOTES:
1. Both Vcc pins must be connected to the supply to assure reliable operation.
2. Both GND pins must be connected to the supply to assure reliable operation.
3. UB = Upper Byte, LB = Lower Byte
4. This text does not indicate orientation of the actual part-marking.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T[3]	Power Dissipation	2.0	2.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTES: 2746 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \geq$ Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2746 tbl 03

1. This parameter is determined by device characterization but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2746 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTES: 2746 tbl 05

1. V_{IL} (min.) = -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Either port, V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7133SA IDT7143SA		IDT7133LA IDT7143LA		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_{15})	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

NOTES:
1. At V_{CC} < 2.0V, input leakages are undefined.

2746 tbl 06

DC ELECTRICAL CHARACTERISTICS OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[3] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7133X25[1] 7143X25[1]		7133X35 7143X35		7133X45 7143X45		7133X55 7143X55		7133X70/90 7143X70/90		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[4]	MIL.	S	250	330	240	325	230	320	230	315	230	310	mA
				L	230	300	220	295	210	290	210	285	210	280	
			COM'L.	S	250	300	240	295	230	290	230	285	230	280	
				L	230	270	220	265	210	260	210	255	210	250	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE_L}$ and $\overline{CE_R}$ = V_{IH} f = f_{MAX}[4]	MIL.	S	25	90	25	85	25	80	25	80	25	75	mA
				L	25	80	25	75	25	70	25	70	25	65	
			COM'L.	S	25	80	25	75	25	75	25	70	25	70	
				L	25	70	25	65	25	65	25	60	25	60	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5], f = f_{MAX}[4], Active Port Outputs Open	MIL.	S	140	230	130	220	120	210	120	210	120	200	mA
				L	120	210	110	200	100	190	100	190	100	180	
			COM'L.	S	140	200	130	190	120	190	120	180	120	180	
				L	120	180	110	170	100	170	100	160	100	160	
I_{SB3}	Full Standby Current (Both Ports — CMOS Level Inputs)	Both Ports $\overline{CE_L}$ & $\overline{CE_R}$ ≥ V_{CC} - 0.2V	MIL.	S	1	30	1	30	1	30	1	30	1	30	mA
				L	0.2	10	0.2	10	0.2	10	0.2	10	0.2	10	
		V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[5]	COM'L.	S	1	15	1	15	1	15	1	15	1	15	
				L	0.2	4	0.2	4	0.2	4	0.2	4	0.2	4	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{CC} - 0.2V[6] V_{IN} ≥ V_{CC} - 0.2V or	MIL.	S	140	220	130	210	120	200	120	200	120	190	mA
				L	120	200	110	190	100	180	100	180	100	170	
		V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[4]	COM'L.	S	140	190	130	180	120	180	120	170	120	170	
				L	120	170	110	160	100	160	100	150	100	150	

NOTES:
1. Commercial only, 0°C to +70°C temperature range.
2. V_{CC} = 5V, T_A = +25°C for Typ., and are not production tested. I_{CCDC} = 180mA (Typ.)
3. "X" in part numbers indicates power rating (SA or LA)
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1 / t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
5. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
6. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

2746 tbl 07

6

DATA RETENTION CHARACTERISTICS

(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

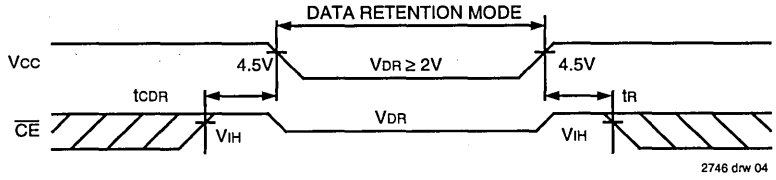
Symbol	Parameter	Test Condition		IDT7133LA/IDT7143LA Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	100	1500	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	ns

NOTES:

2746 tbl 08

1. V_{CC} = 2V, T_A = +25°C, and are not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but is not production tested.

DATA RETENTION WAVEFORM



2746 drw 04

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 & 3

2746 tbl 09

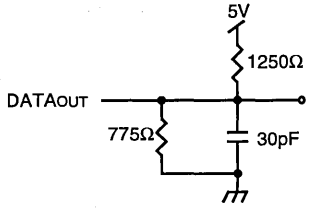


Figure 1. Output Load

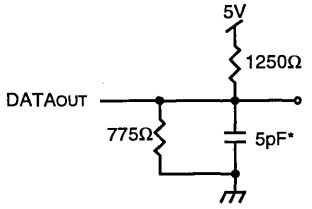
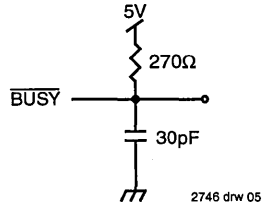


Figure 2. Output Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
*Including scope and jig



2746 drw 05

Figure 3. $\overline{BUSY}$ Output Load (IDT7133 only)

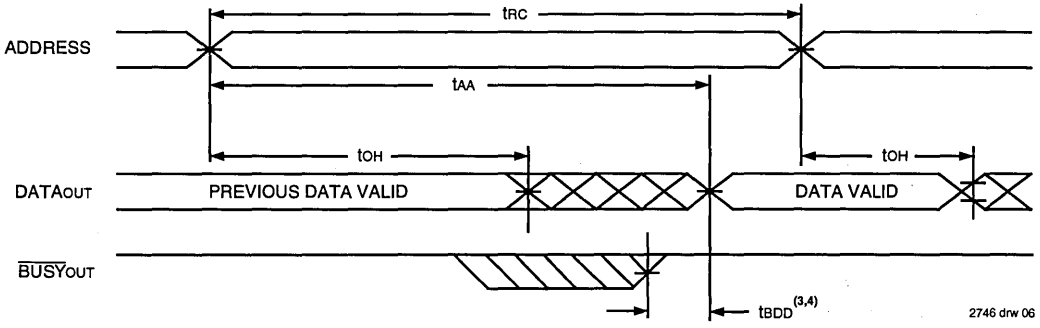
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[4]

Symbol	Parameter	IDT7133X25[2] IDT7143X25[2] Min.	Max.	IDT7133X35 IDT7143X35 Min.	Max.	IDT7133X45 IDT7143X45 Min.	Max.	IDT7133X55 IDT7143X55 Min.	Max.	IDT7133X70/90 IDT7143X70/90 Min.	Max.	Unit
READ CYCLE												
tRC	Read Cycle Time	25	—	35	—	45	—	55	—	70/90	—	ns
tAA	Address Access Time	—	25	—	35	—	45	—	55	—	70/90	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70/90	ns
tAOE	Output Enable Access Time	—	15	—	20	—	25	—	30	—	40/40	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	0	—	0/0	—	ns
tLZ	Output Low-Z Time[1, 3]	0	—	0	—	0	—	5	—	5/5	—	ns
tHZ	Output High-Z Time[1, 3]	—	15	—	20	—	20	—	20	—	25/25	ns
tPU	Chip Enable to Power Up Time[3]	0	—	0	—	0	—	0	—	0/0	—	ns
tPD	Chip Disable to Power Down Time[3]	—	50	—	50	—	50	—	50	—	50/50	ns

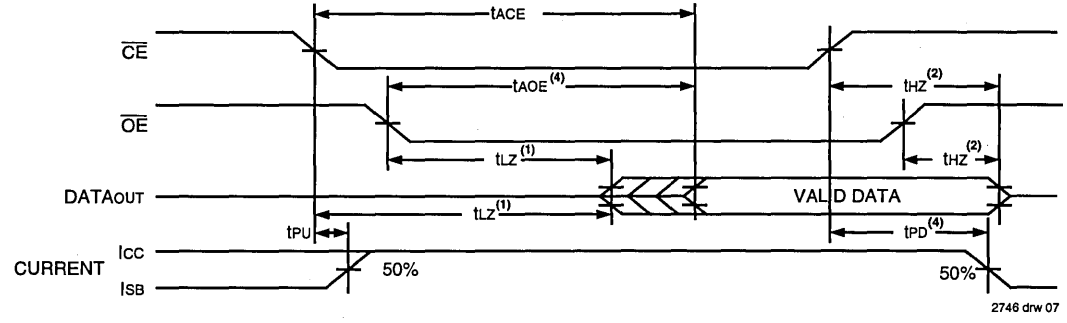
NOTES:
2746 tbl 10

1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1, 2, and 3).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed by device characterization, but is not production tested.
4. "X" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE[1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE[1, 3]



NOTES:

1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is deasserted last, $\overline{OE}$ or $\overline{CE}$.
3. tBDD delay is required only in a case where the opposite port is completing a write operation to the same address location. For simultaneous read operations, $\overline{BUSY}$ has no relationship to valid output data.
4. Start of valid data depends on which timing becomes effective last, tAOE, tACE, tAA, or tBDD.
5. R/$\overline{W}$ = VIH, and the address is valid prior to others coincidental with $\overline{CE}$ transition Low.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[7]

Symbol	Parameter	IDT7133x25[2] IDT7143x25[2] Min.	Max.	IDT7133x35 IDT7143x35 Min.	Max.	IDT7133x45 IDT7143x45 Min.	Max.	IDT7133x55 IDT7143x55 Min.	Max.	IDT7133x70/90 IDT7143x70/90 Min.	Max.	Unit
WRITE CYCLE												
t_{WC}	Write Cycle Time[4]	25	—	35	—	45	—	55	—	70/90	—	ns
t_{EW}	Chip Enable to End-of-Write	20	—	25	—	30	—	40	—	50/50	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	25	—	30	—	40	—	50/50	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	0/0	—	ns
t_{WP}	Write Pulse Width[6]	20	—	25	—	30	—	40	—	50/50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0/0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	20	—	20	—	25	—	30/30	—	ns
t_{HZ}	Output High-Z Time[1, 3]	—	15	—	20	—	20	—	20	—	25/25	ns
t_{DH}	Data Hold Time[5]	0	—	0	—	5	—	5	—	5/5	—	ns
t_{WZ}	Write Enable to Output in High-Z[1, 3]	—	15	—	20	—	20	—	20	—	25/25	ns
t_{OW}	Output Active from End-of-Write[1, 3, 5]	0	—	0	—	5	—	5	—	5/5	—	ns

NOTES: 2746 tbl 11

1. Transition is measured ±500mV from Low- or High-impedance voltage with the Output Test Load (Figures 2).
2. 0°C to +70°C temperature range only.
3. This parameter is guaranteed but not tested.
4. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WR} + t_{WP}$, since $R/\overline{W} = V_{IL}$ must occur after t_{BAA}.
5. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operation conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
6. This parameter is determined by device characterization, but is not production tested. Transition is measured ± 200mV from steady state with the Output Test Load (Figure 2).
7. "X" in part number indicates power rating (SA or LA).

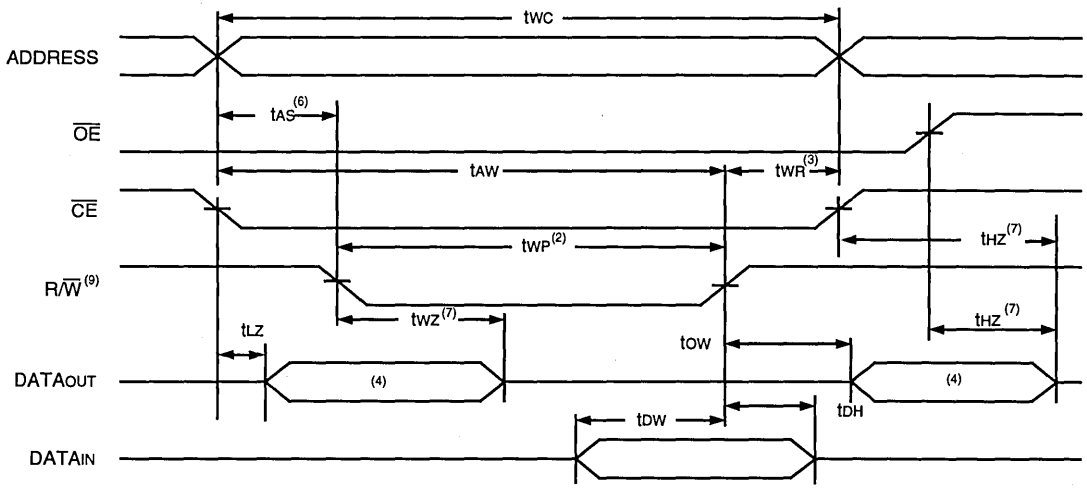
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[7]

Symbol	Parameter	IDT7133x25[1] IDT7143x25[1] Min.	Max.	IDT7133x35 IDT7143x35 Min.	Max.	IDT7133x45 IDT7143x45 Min.	Max.	IDT7133x55 IDT7143x55 Min.	Max.	IDT7133x70/90 IDT7143x70/90 Min.	Max.	Unit
BUSY TIMING (For MASTER IDT7133)												
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	25	—	35	—	45	—	50	—	55/55	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	20	—	30	—	40	—	40	—	45/45	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	25	—	30	—	35	—	35/35	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	20	—	25	—	30	—	30/30	ns
t_{WDD}	Write Pulse to Data Delay[2]	—	50	—	60	—	80	—	80	—	90/90	ns
t_{DDD}	Write Data Valid to Read Data Delay[2]	—	35	—	45	—	55	—	55	—	70/70	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[3]	—	Note 3	—	Note 3	—	Note 3	—	Note 3	—	Note 3	ns
t_{APS}	Arbitration Priority Set Up Time[4]	5	—	5	—	5	—	5	—	5/5	—	ns
BUSY INPUT TIMING (For SLAVE IDT7143)												
t_{WB}	Write to $\overline{BUSY}$[5]	0	—	0	—	0	—	0	—	0/0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$[6]	20	—	25	—	30	—	30	—	30/30	—	ns
t_{WDD}	Write Pulse to Data Delay[2]	—	50	—	60	—	80	—	80	—	90/90	ns
t_{DDD}	Write Data Valid to Read Data Delay[2]	—	35	—	45	—	55	—	55	—	70/70	ns

NOTES: 2746 tbl 12

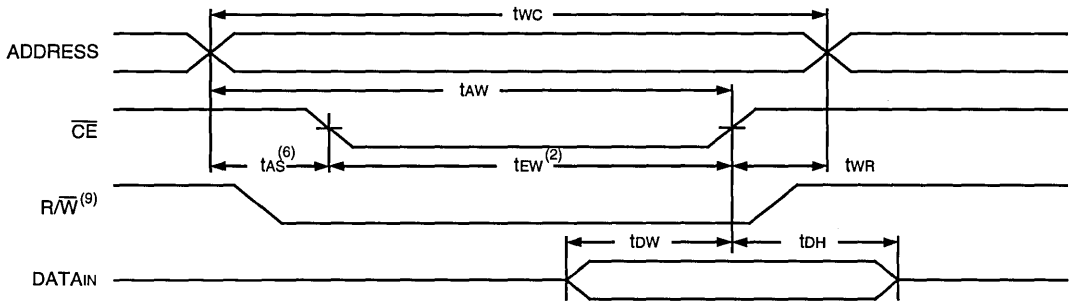
1. 0°C to +70°C temperature range only.
2. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and Busy".
3. t_{BDD} is calculated parameter and is greater of 0, t_{WDD} - t_{WP} (actual) or t_{DDD} - t_{DW} (actual).
4. To ensure that the earlier of the two ports wins.
5. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
6. To ensure that a write cycle is completed on port "B" after contention on port "A".
7. "X" in part number indicates power rating (SA or LA).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1, 5, 8)



2746 drw 08

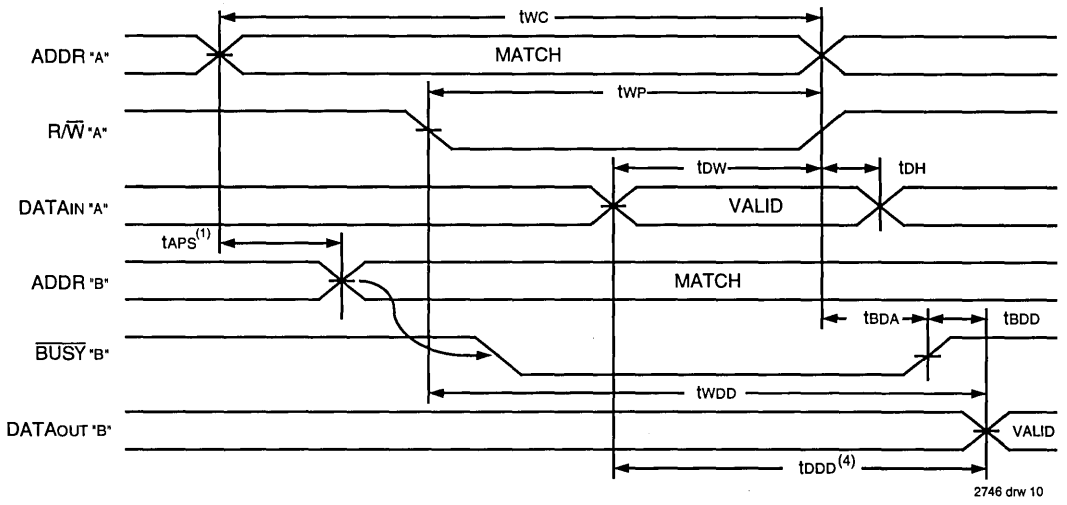
WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED TIMING)(1, 5)



2746 drw 09

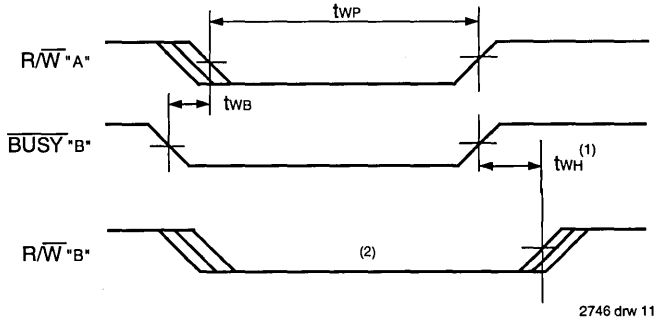
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a $\overline{CE}$ = VIL and a R/$\overline{W}$ = VIL.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going High to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined by device characterization, but is not production tested. Transition is measured ± 200mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. R/$\overline{W}$ for either upper or lower byte.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$ (1, 2, 3)



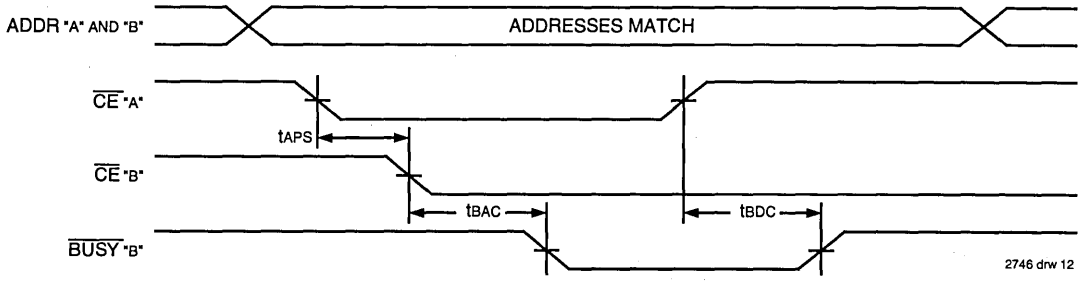
NOTES:
1. To ensure that the earlier of the two ports wins, tAPS is ignored for Slave (IDT7143).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
3. $\overline{OE} = V_{IL}$ for the reading port.
4. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ (M/$\overline{S}$ = VIL)

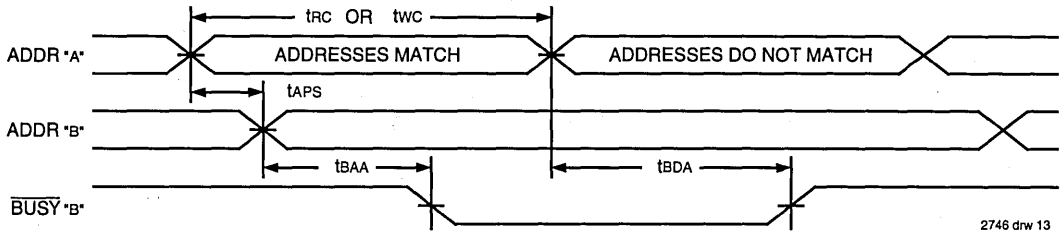


NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (SLAVE) and output (MASTER).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/$\overline{W}$ "B", until $\overline{BUSY}$ "B" goes High.
3. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING (1)



TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESSES (1)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted (IDT7133 only).

6

FUNCTIONAL DESCRIPTION:

The IDT7133/43 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7133/43 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Non-contention READ/WRITE conditions are illustrated in Table 1.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by using the IDT7143 (SLAVE). In the IDT7143, the busy pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low. The busy outputs on the IDT 7133 RAM are open drain and require pull-up resistors.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7133/43 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7133 RAM the busy pin is an output and on the IDT7143 RAM, the busy pin is an input (see Figure 3).

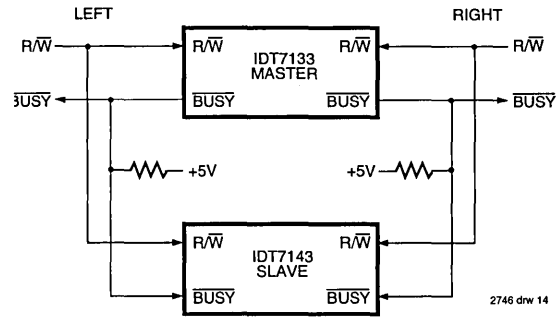


Figure 4. Busy and chip enable routing for both width and depth expansion with the IDT7133 (MASTER) and the IDT7143 (SLAVE).

Expanding the data bus width to 32 bits or more in a Dual-Port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now busy and the CPUs will await indefinately for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding Dual-Port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all Dual-Port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

TRUTH TABLE I – NON-CONTENTION READ/WRITE CONTROL[4]

LEFT OR RIGHT PORT[1]						
$R/\overline{W}_{LB}$	$R/\overline{W}_{UB}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	I/O_{8-15}	Function
X	X	H	X	Z	Z	Port Disabled and in Power Down Mode, I_{SB2}, I_{SB4}
X	X	H	X	Z	Z	$\overline{CE}_R = \overline{CE}_L = V_{IH}$, Power Down Mode, I_{SB1} or I_{SB3}
L	L	L	X	DATAIN	DATAIN	Data on Lower Byte and Upper Byte Written into Memory[2]
L	H	L	L	DATAIN	DATAOUT	Data on Lower Byte Written into Memory[2], Data in Memory Output on Upper Byte[3]
H	L	L	L	DATAOUT	DATAIN	Data in Memory Output on Lower Byte[3], Data on Upper Byte Written into Memory[2]
L	H	L	H	DATAIN	Z	Data on Lower Byte Written into Memory[2]
H	L	L	H	Z	DATAIN	Data on Upper Byte Written into Memory[2]
H	H	L	L	DATAOUT	DATAOUT	Data in Memory Output on Lower Byte and Upper Byte
H	H	L	H	Z	Z	High Impedance Outputs

NOTES: 2746 tbl 13

1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$
2. If $\overline{BUSY}$ = LOW, data is not written.
3. If $\overline{BUSY}$ = LOW, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. "H" = HIGH, "L" = LOW, "X" = Don't Care, "Z" = High Impedance, "LB" = Lower Byte, "UB" = Upper Byte

TRUTH TABLE I I — ADDRESS BUSY ARBITRATION

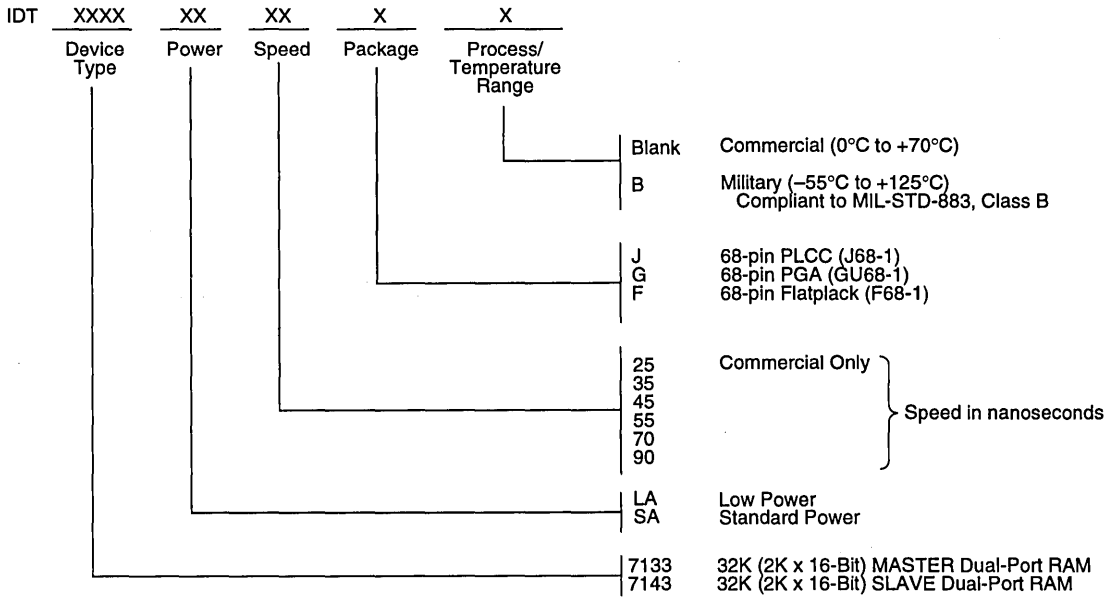
Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{10L} A_{0R}-A_{10R}	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

NOTES: 2746 tbl 14

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs on the IDT7133 (MASTER). Both are inputs on the IDT7143 (SLAVE). On Slaves the $\overline{BUSY}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

6

ORDERING INFORMATION



2746 drw 15

Integrated Device Technology, Inc.

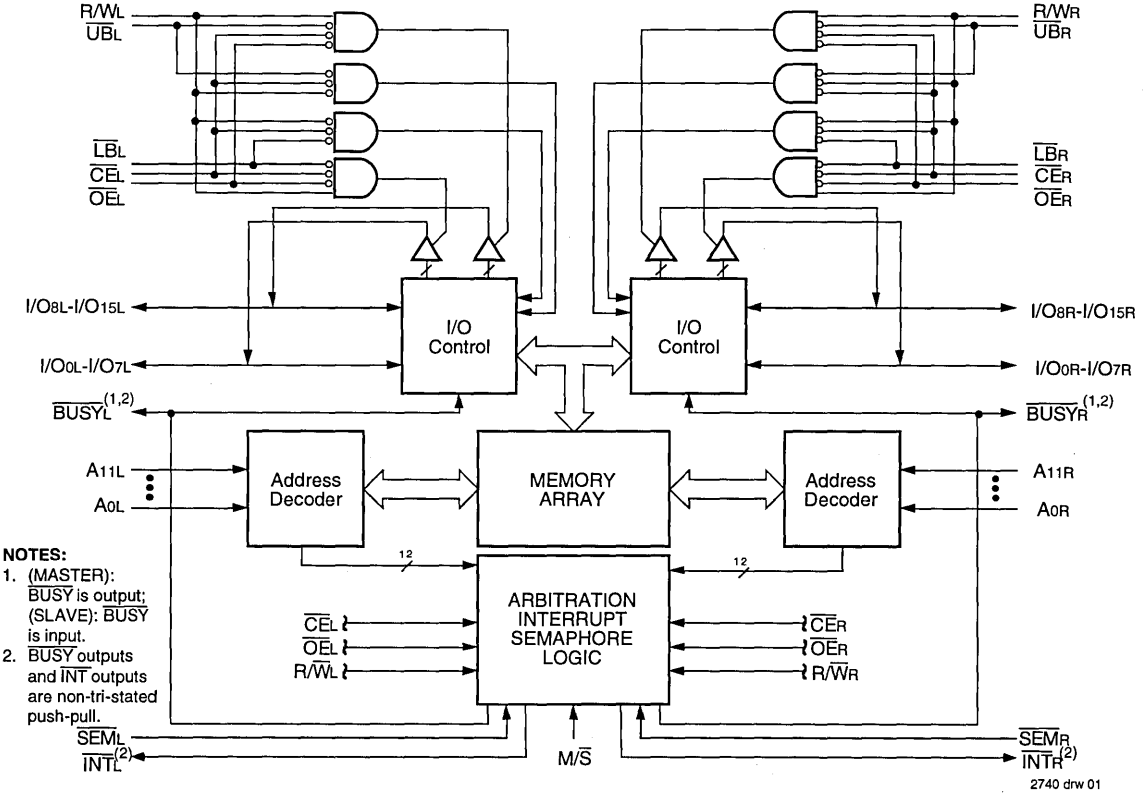
HIGH-SPEED 4K x 16 DUAL-PORT STATIC RAM

IDT7024S/L

FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 25/35/55/70ns (max.)
  - — Commercial: 17/20/25/35/55ns (max.)
- Low-power operation
  - — IDT7024S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7024L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT7024 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Devices are capable of withstanding greater than 2001V electrostatic discharge.
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Available in 84-pin PGA, quad flatpack, PLCC, and 100-pin Thin Quad Plastic Flatpack
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.

2740 drw 01

DESCRIPTION:

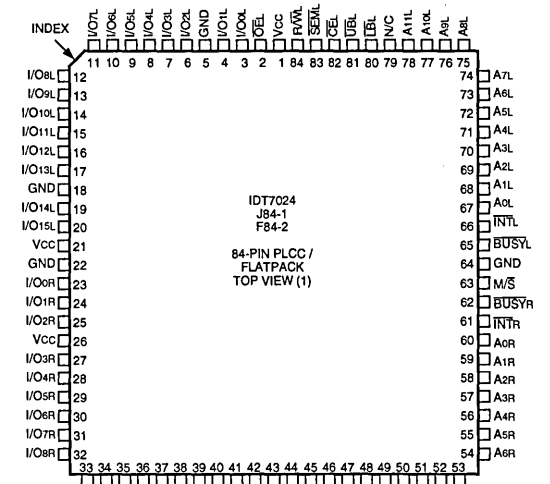
The IDT7024 is a high-speed 4K x 16 Dual-Port Static RAM. The IDT7024 is designed to be used as a stand-alone 64K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit or more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

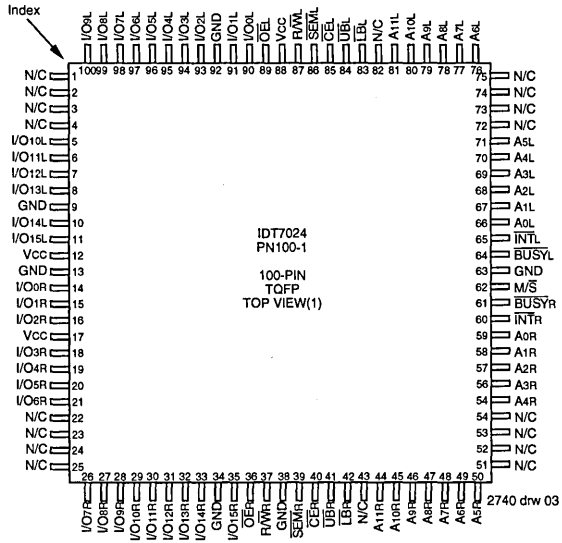
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by chip enable ($\overline{CE}$) permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500µW from a 2V battery.

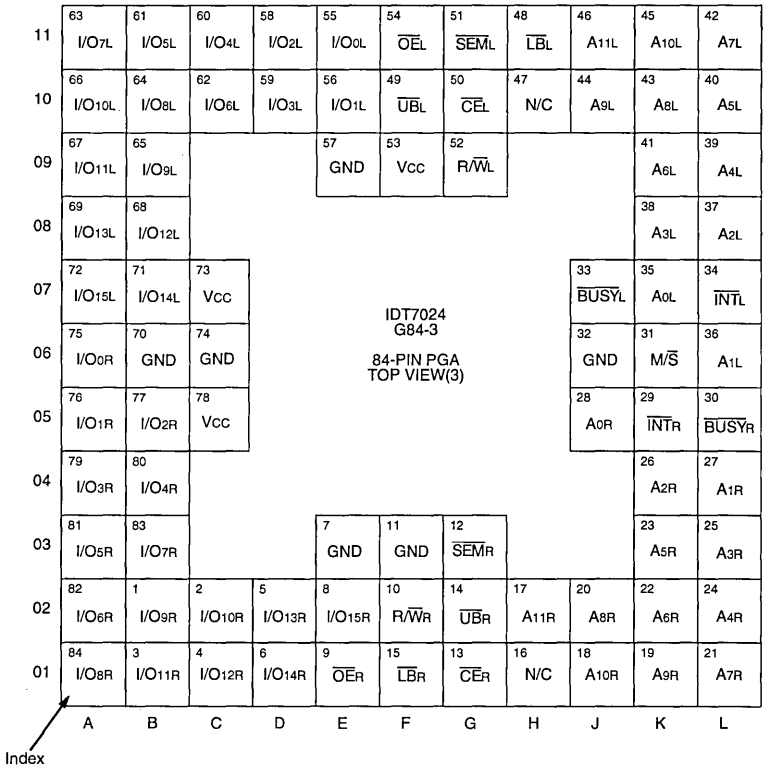
The IDT7024 is packaged in a ceramic 84-pin PGA, an 84-pin quad flatpack and PLCC, and a 100-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS





NOTE:
1. This text does not indicate orientation of the actual part-marking.



PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{11L}$	$A_{0R} - A_{11R}$	Address
$I/O_{0L} - I/O_{15L}$	$I/O_{0R} - I/O_{15R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2740 tbl 1

NOTES:
1. All V_{CC} pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power-Down
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	H	DATAIN	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

NOTE: 2740 tbl 02

1. A_{0L} — A_{11L} are not equal to A_{0R} — A_{11R}

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Semaphore Flag Data Out
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Semaphore Flag Data Out
H	↑	X	X	X	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
X	↑	X	H	H	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

2740 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2740 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc +0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20ma for the period over V_{TERM} ≥ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2740 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2740 tbl 06

1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, F = 1.0MHZ)[1]

Symbol	Parameter	Condition[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

Note: 2740 tbl 07

1. This parameter are determined by device characterization, but is not production tested. TQFP Package only.
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7024S		IDT7024L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2740 tbl 08

NOTE:
1. At V_{CC} = 2.0V input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7024X17 COM'L ONLY		7024X20 COM'L ONLY		7024X25		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	MIL	S	—	—	—	—	155	340	mA
				L	—	—	—	—	155	280	
			COM	S	170	310	160	290	155	265	
				L	170	260	160	240	155	220	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	MIL	S	—	—	—	—	16	80	mA
				L	—	—	—	—	16	65	
			COM	S	20	60	20	60	16	60	
				L	20	50	20	50	16	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_{"A"}$=V_{IL} and $\overline{CE}_{"B"}$=V_{IH}[5] Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	MIL	S	—	—	—	—	90	215	mA
				L	—	—	—	—	90	180	
			COM	S	105	190	95	180	90	170	
				L	105	160	95	150	90	140	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$-0.2V	MIL	S	—	—	—	—	1.0	30	mA
				L	—	—	—	—	0.2	10	
			COM	S	1.0	15	1.0	15	1.0	15	
				L	0.2	5	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2 and $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$-0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, Active Port Outputs Open, f = f_{MAX}[3]	MIL	S	—	—	—	—	85	200	mA
				L	—	—	—	—	85	170	
			COM	S	100	170	90	155	85	145	
				L	100	140	90	130	85	120	

NOTES:
2740 tbl 09
1. 'X' in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. $I_{CC\,DC}$ = 120mA (TYP.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the oppOsite from port "A".

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7024X35 Typ.[2]	7024X35 Max.	7024X55 Typ.[2]	7024X55 Max.	7024X70 MIL ONLY Typ.[2]	7024X70 MIL ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open; $\overline{SEM}$ = V_{IH}; f = f_{MAX}[3]	MIL.	S	150	300	150	300	140	300	mA
				L	150	250	150	250	140	250	
			COM'L.	S	150	250	150	250	—	—	
				L	150	210	150	210	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH}; $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}; f = f_{MAX}[3]	MIL.	S	13	80	13	80	10	80	mA
				L	13	65	13	65	10	65	
			COM'L.	S	13	60	13	60	—	—	
				L	13	50	13	50	—	—	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_{"A"}$=V_{IL} and $\overline{CE}_{"B"}$=V_{IH}[5]; Active Port Outputs Open; f = f_{MAX}[3]; $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	MIL.	S	85	190	85	190	80	190	mA
				L	85	160	85	160	80	160	
			COM'L.	S	85	155	85	155	—	—	
				L	85	130	85	130	—	—	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V; V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4]; $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	MIL.	S	1.0	30	1.0	30	1.0	30	mA
				L	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	—	—	
				L	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2 and $\overline{CE}_{"B"}$ ≥ V_{CC} - 0.2V[5]; $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V; V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	80	175	80	175	75	175	mA
				L	80	150	80	150	75	150	
			COM'L.	S	80	135	80	135	—	—	
				L	80	110	80	110	—	—	

NOTES:
2740 tbl 10

1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested.
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

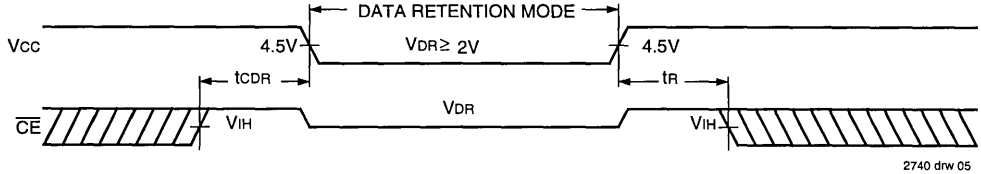
(V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)[4]

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ ≥ V_{HC}	MIL.	—	100	4000	µA
		V_{IN} ≥ V_{HC} or ≤ V_{LC}	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time	$\overline{SEM}$ ≥ V_{HC}		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
2740 tbl 11

1. T_A = +25°C, V_{CC} = 2V, and are guaranted by characterization but are not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.
4. At V_{CC} = 2.0V, input leakages are not defined.

DATA RETENTION WAVEFORM



2740 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2740 tbl 12

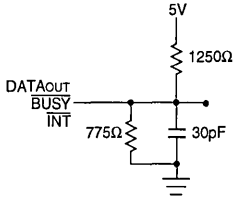
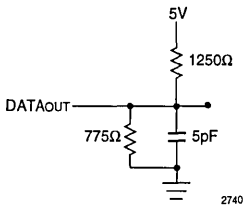


Figure 1. AC Output Test Load



2740 drw 06

Figure 2. Output Test Load
(for tLZ, tHZ, tWZ, tOW)
Including scope and Jig

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

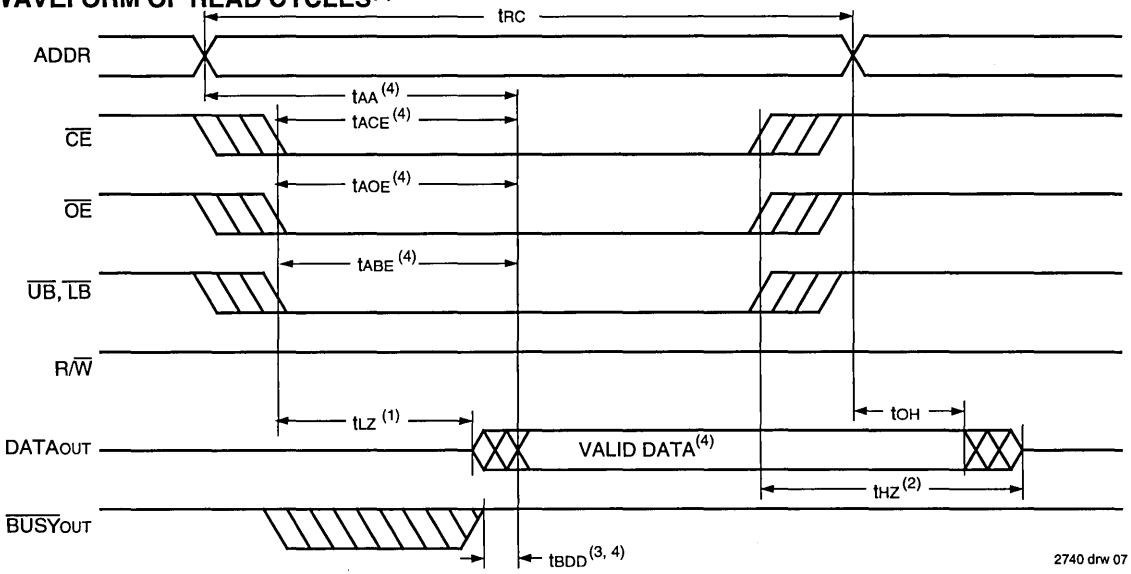
Symbol	Parameter	IDT7024X17 COM'L ONLY Min.	IDT7024X17 COM'L ONLY Max.	IDT7024X20 COM'L ONLY Min.	IDT7024X20 COM'L ONLY Max.	IDT7024X25 Min.	IDT7024X25 Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	17	—	20	—	25	—	ns
tAA	Address Access Time	—	17	—	20	—	25	ns
tACE	Chip Enable Access Time[3]	—	17	—	20	—	25	ns
tABE	Byte Enable Access Time[3]	—	17	—	20	—	25	ns
tAOE	Output Enable Access Time	—	10	—	12	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time[1, 2]	3	—	3	—	3	—	ns
tHZ	Output High-Z Time[1, 2]	—	10	—	12	—	15	ns
tPU	Chip Enable to Power Up Time[1,2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[1,2]	—	17	—	20	—	25	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	10	—	ns
tSAA	Semaphore Address Access[3]	—	17	—	20	—	25	ns

Symbol	Parameter	IDT7024X35 Min.	IDT7024X35 Max.	IDT7024X55 Min.	IDT7024X55 Max.	IDT7024X70 MIL ONLY Min.	IDT7024X70 MIL ONLY Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	35	—	55	—	70	—	ns
tAA	Address Access Time	—	35	—	55	—	70	ns
tACE	Chip Enable Access Time[3]	—	35	—	55	—	70	ns
tABE	Byte Enable Access Time[3]	—	35	—	55	—	70	ns
tAOE	Output Enable Access Time	—	20	—	30	—	35	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time[1, 2]	3	—	3	—	3	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	25	—	30	ns
tPU	Chip Enable to Power Up Time[1,2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[1,2]	—	35	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns
tSAA	Semaphore Address Access[3]	—	35	—	55	—	70	ns

2740 tbl 13

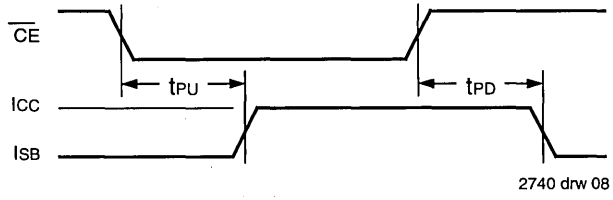
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{UB}$ or $\overline{LB}$ = VIL, and $\overline{SEM}$ =VIH. To access semaphore, $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIH, and $\overline{SEM}$ =VIL.
4. "X" in part numbers indicates power rating (S or L).

WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first, $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. tBDD delay is required only in cases where opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tABE, tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE [5]

Symbol	Parameter	IDT7024X17 COM'L ONLY Min.	IDT7024X17 COM'L ONLY Max.	IDT7024X20 COM'L ONLY Min.	IDT7024X20 COM'L ONLY Max.	IDT7024X25 Min.	IDT7024X25 Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time	17	—	20	—	25	—	ns
tEW	Chip Enable to End-of-Write[3]	12	—	15	—	20	—	ns
tAW	Address Valid to End-of-Write	12	—	15	—	20	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	10	—	15	—	15	—	ns
tHZ	Output High-Z Time[1, 2]	—	10	—	12	—	15	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	10	—	12	—	15	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

Symbol	Parameter	IDT7024X35 Min.	IDT7024X35 Max.	IDT7024X55 Min.	IDT7024X55 Max.	IDT7024X70 MIL. ONLY Min.	IDT7024X70 MIL. ONLY Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time	35	—	55	—	70	—	ns
tEW	Chip Enable to End-of-Write[3]	30	—	45	—	50	—	ns
tAW	Address Valid to End-of-Write	30	—	45	—	50	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	25	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	30	—	40	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	25	—	30	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	15	—	25	—	30	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

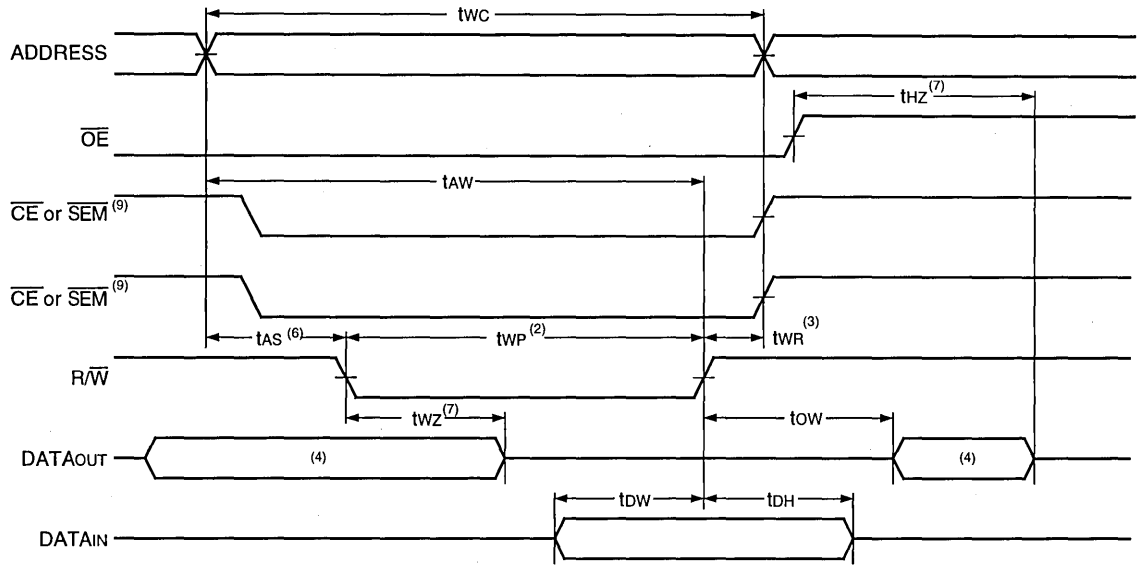
NOTES:

2740 tbl 14

1. Transition is measured ±500mV from low or high impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{UB}$ or $\overline{LB}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIH, and $\overline{SEM}$ = VIL. Either condition must be valid for the entire t EW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. "X" in part numbers indicates power rating (S or L).

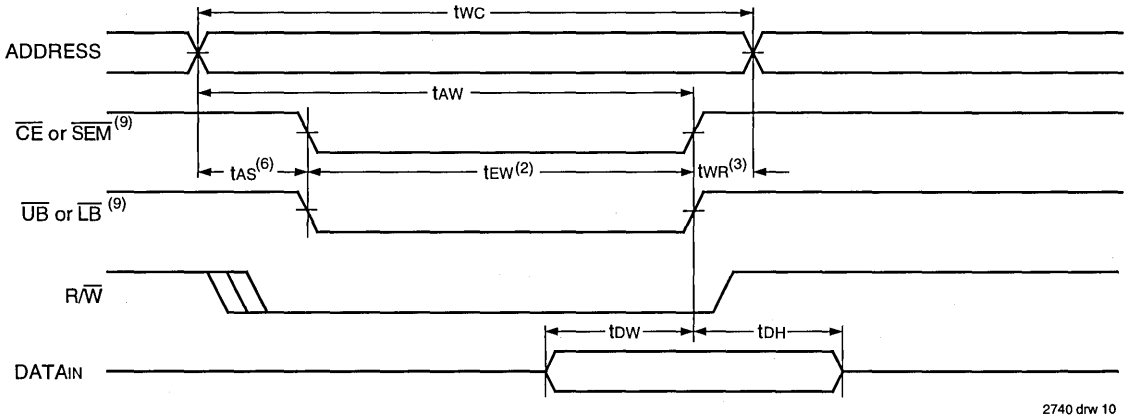
6

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,5,8)



2740 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING(1,5)

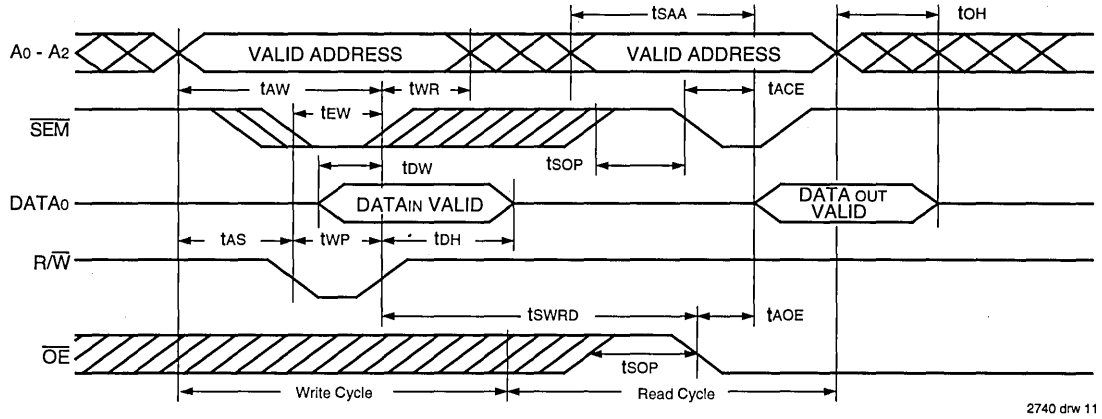


2740 drw 10

NOTES:

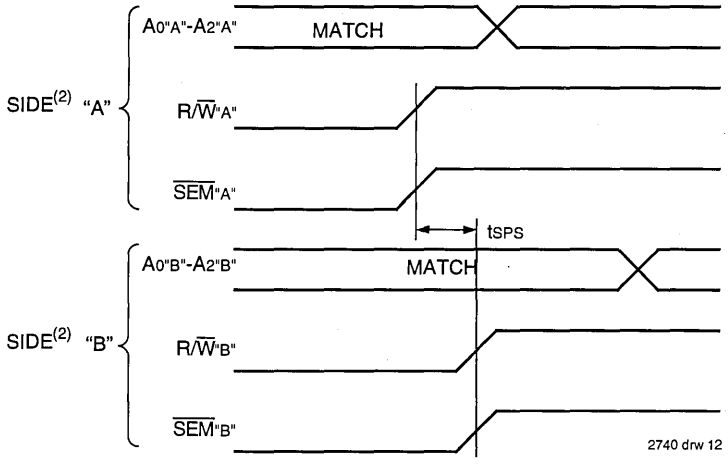
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ & $\overline{LB}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{UB}$ or $\overline{LB}$ and a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end-of-write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, R/$\overline{W}$, $\overline{UB}$, or $\overline{LB}$.
7. This parameter is guaranted by device characterization, but is not production tested.Transition is measured +/- 500mV steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP for (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .
9. To access RAM, $\overline{CE}$ = VIL, $\overline{UB}$ or $\overline{LB}$ = VIL, and $\overline{SEM}$ = VIH. To access Semephore, $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIH, and $\overline{SEM}$ = VIL. tEW must be met for either condition.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}$R = $\overline{CE}$L = VIH, or both $\overline{UB}$ & $\overline{LB}$ = VIH, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. All timing is the same for left and rift ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}$A or $\overline{SEM}$A going High to R/$\overline{W}$B or $\overline{SEM}$B going High.
4. If tSPS is not satisfied, there is no guarantee which side will obtain the Semephore flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	IDT7024X17 COM'L ONLY Min.	IDT7024X17 COM'L ONLY Max.	IDT7024X20 COM'L ONLY Min.	IDT7024X20 COM'L ONLY Max.	IDT7024X25 Min.	IDT7024X25 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	17	—	20	—	20	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	17	—	20	—	20	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	17	—	20	—	20	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	17	—	17	—	17	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	17	—	20	—	25	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	13	—	15	—	17	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	30	—	45	—	50	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	25	—	30	—	35	ns

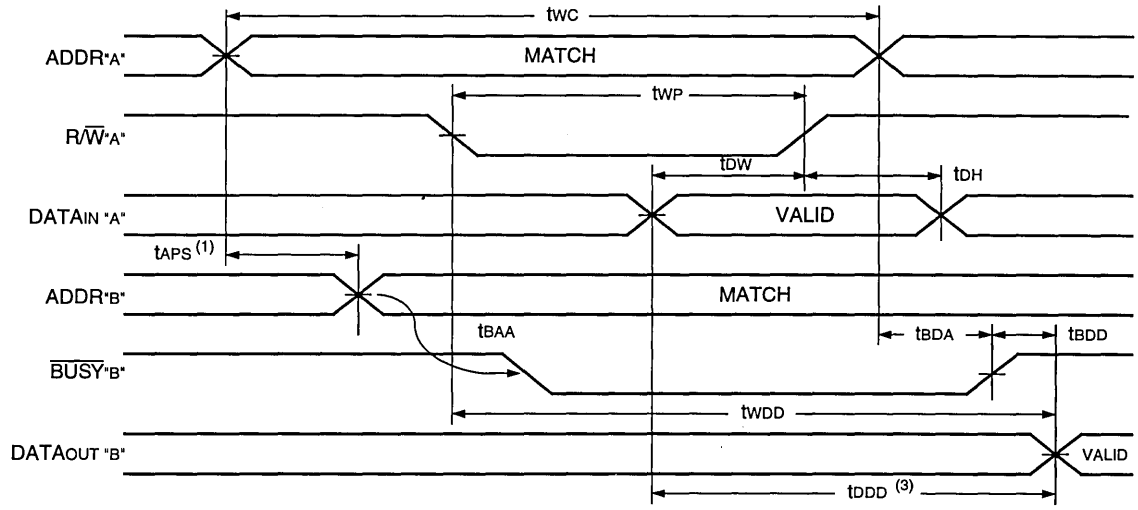
Symbol	Parameter	IDT7024X35 Min.	IDT7024X35 Max.	IDT7024X55 Min.	IDT7024X55 Max.	IDT7024X70 MIL. ONLY Min.	IDT7024X70 MIL. ONLY Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	20	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	40	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	20	—	35	—	35	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	35	—	55	—	70	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	60	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	45	—	65	—	80	ns

NOTES:

2740 tbl 15

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M / $\overline{S}$ = H)" or "Timing Waveform of Write With Port-To-Port Delay (M / $\overline{S}$ = L)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0ns, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port 'B' during contention with port 'A'.
5. To ensure that a write cycle is completed on port 'B' after contention with port 'A'.
6. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$ (2,5) (M/$\overline{S}$ = V_{IH})

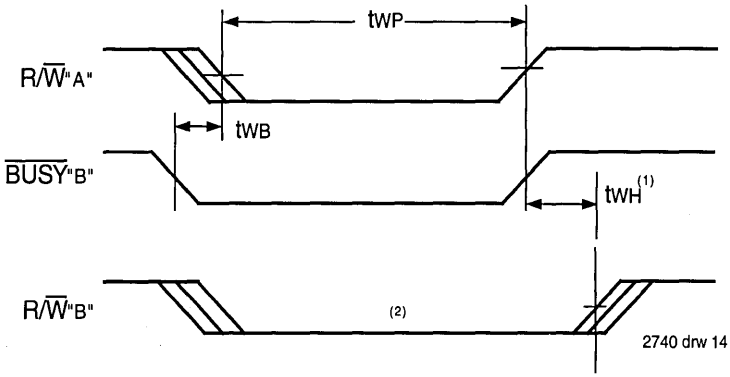


2740 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for M/$\overline{S}$ = VIL (SLAVE).
2. $\overline{CE}$L = $\overline{CE}$R = VIL.
3. $\overline{OE}$ = VIL for the reading port.
4. If M/$\overline{S}$ = VIL(slave) then $\overline{BUSY}$ is an input $\overline{BUSY}$"A" = VIL and $\overline{BUSY}$"B" = don't care, for this example.
5. All timing is the same for both left and right ports. Port "A" may be either the left or right Port. Port "B" is the port opposite from port "A".

6

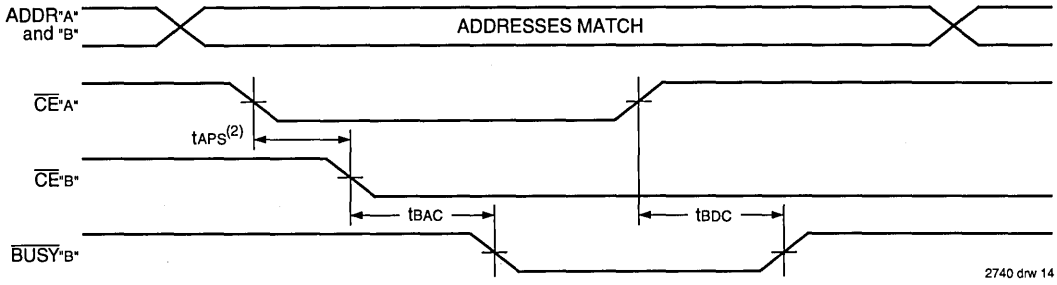
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$



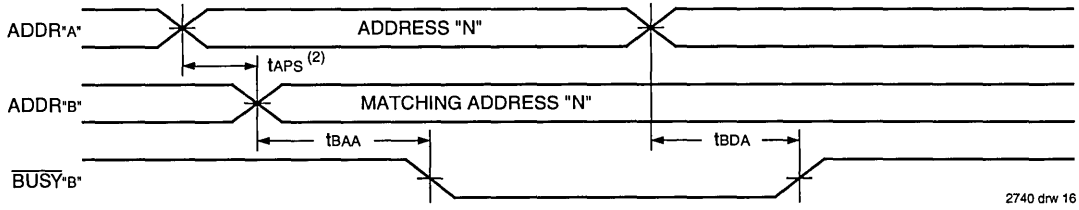
2740 drw 14

Note:
1. tWH must be met for both $\overline{BUSY}$ input (slave) and output (master).
2. Busy is asserted on port "B" Blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes High.

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1) (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)(M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1)

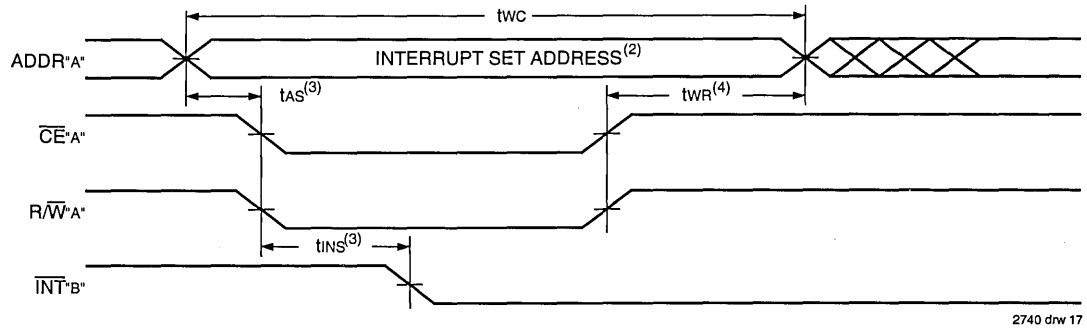
Symbol	Parameter	IDT7024X17 COM'L ONLY Min.	IDT7024X17 COM'L ONLY Max.	IDT7024X20 COM'L ONLY Min.	IDT7024X20 COM'L ONLY Max.	IDT7024X25 Min.	IDT7024X25 Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	15	—	20	—	20	ns
tINR	Interrupt Reset Time	—	15	—	20	—	20	ns20

Symbol	Parameter	IDT7024X35 Min.	IDT7024X35 Max.	IDT7024X55 Min.	IDT7024X55 Max.	IDT7024X70 MIL. ONLY Min.	IDT7024X70 MIL. ONLY Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	40	—	50	ns
tINR	Interrupt Reset Time	—	25	—	40	—	50	ns

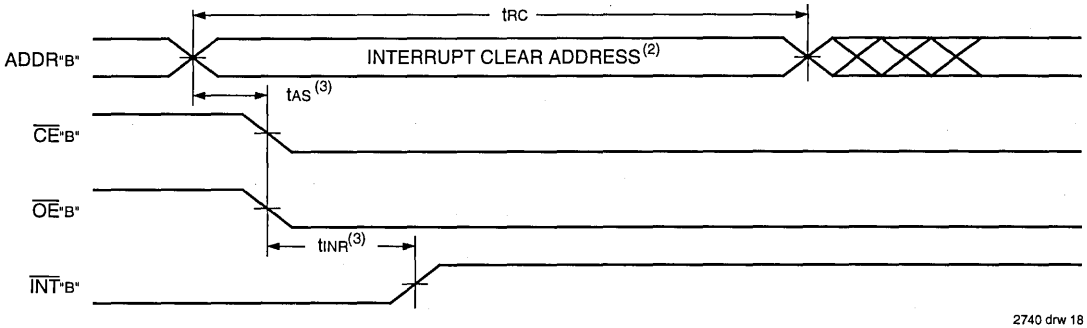
NOTE:
1. "X" in part numbers indicates power rating (S or L).

2740 tbl 16

WAVEFORM OF INTERRUPT TIMING[1]



2740 drw 17



2740 drw 18

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

6

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{11L}-A_{0L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{11R}-A_{0R}	$\overline{INT}_R$	Function
L	L	X	FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = VIH.
2. If $\overline{BUSY}_L$ = VIL, then no change.
3. If $\overline{BUSY}_R$ = VIL, then no change.

2740 tbl 17

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{11L} A_{0R}-A_{11R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

2740 tbl 16

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}_X$ outputs on the IDT7024 are push pull, not open drain outputs. On slaves, the $\overline{BUSY}$ asserted input internally inhibits write.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If tAPS is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_{15} Left	D_0 - D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

2740 tbl 19

NOTE:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7024.

FUNCTIONAL DESCRIPTION

The IDT7024 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7024 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location FFE (HEX), where a write is defined as the $\overline{CE} = R/\overline{W} = V_{IL}$ per the Truth Table. The left port clears the interrupt by access address location FFE access when $\overline{CE}_R = \overline{OE}_R = V_{IL}$, $R/\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must access the memory location FFF. The message (16 bits) at FFE or FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations FFE and FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all

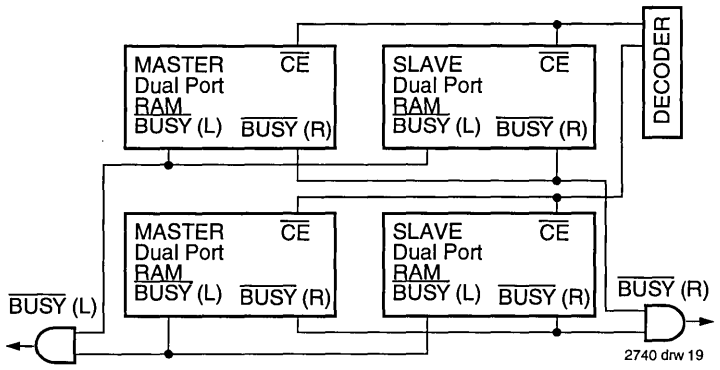


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7024 RAMs.

applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 7024 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7024 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7024 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7024 is an extremely fast Dual-Port 4K x 16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7024 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7024's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the

6

maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7024 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7024 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a

resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7024's Dual-Port RAM. Say the 4K x 16 RAM was to be divided into two 2K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 2K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 2K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 2K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

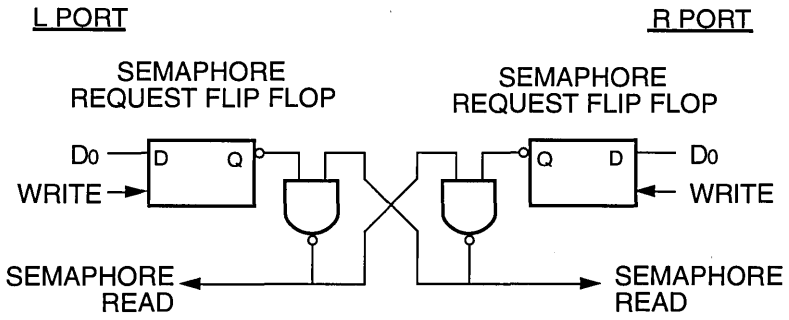
Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 2K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

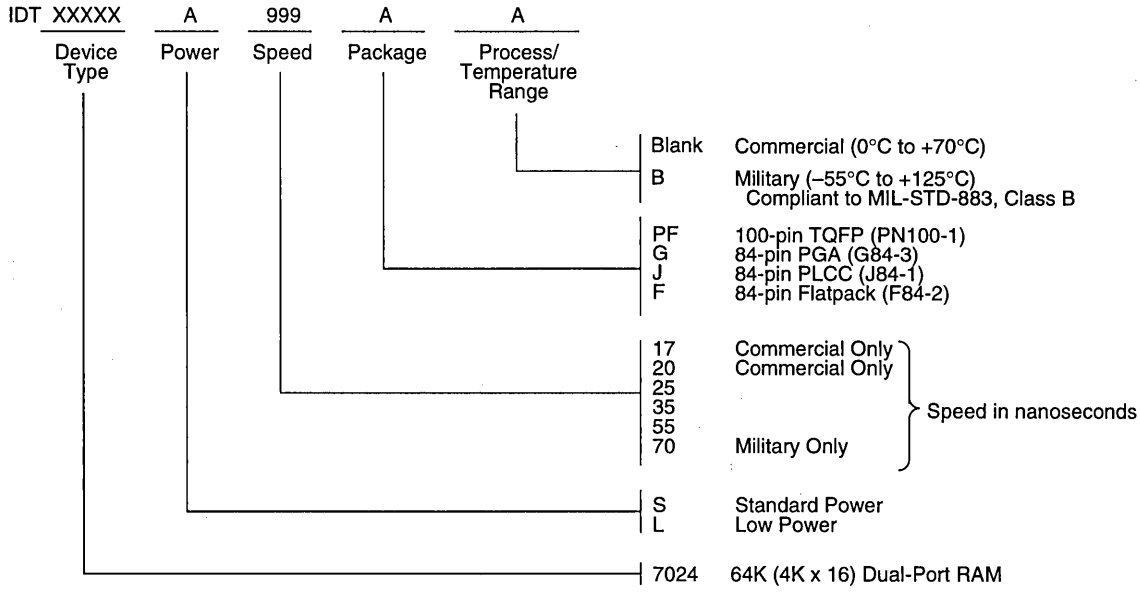
Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.



2740 drw 20

Figure 4. IDT7024 Semaphore Logic

ORDERING INFORMATION



2740 drw 21

Integrated Device Technology, Inc.

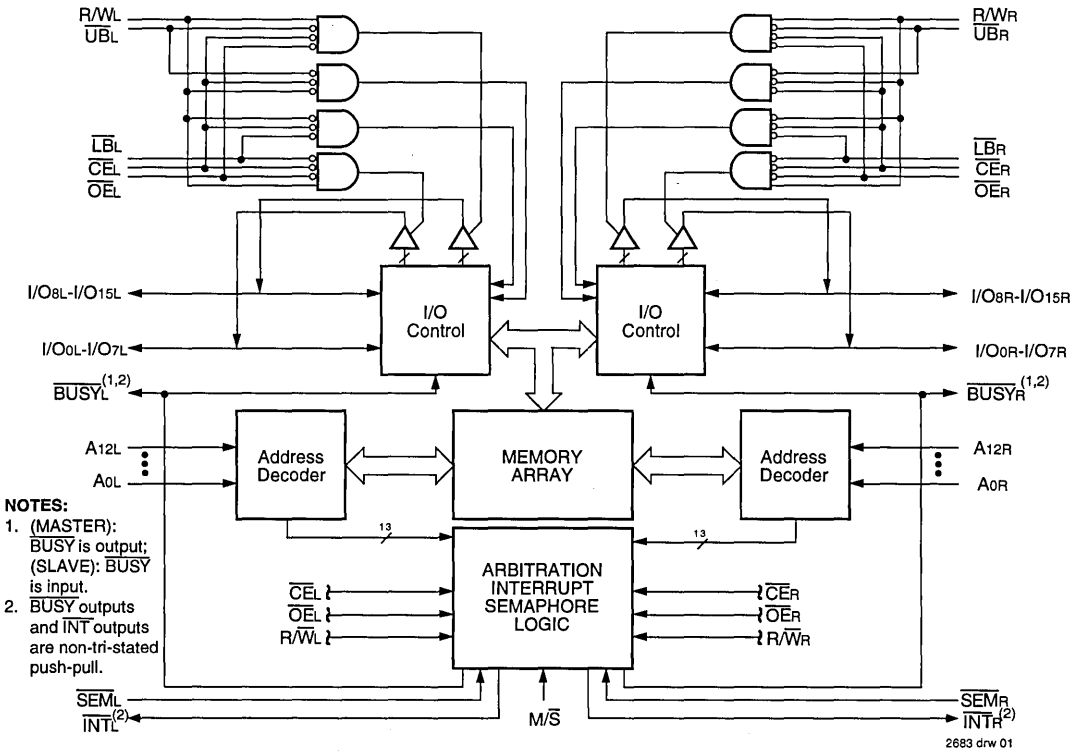
HIGH-SPEED 8K x 16 DUAL-PORT STATIC RAM

IDT7025S/L

FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 25/35/55/70ns (max.)
  - — Commercial: 17/20/25/35/55ns (max.)
- Low-power operation
  - — IDT7025S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7025L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT7025 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Devices are capable of withstanding greater than 2001V electrostatic discharge
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Available in 84-pin PGA, quad flatpack, PLCC, and 100-pin Thin Quad Plastic Flatpack
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.

DESCRIPTION:

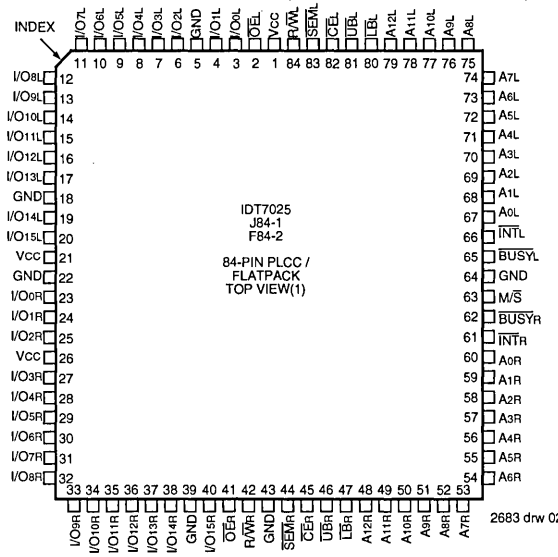
The IDT7025 is a high-speed 8K x 16 Dual-Port Static RAM. The IDT7025 is designed to be used as a stand-alone 128K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit or more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

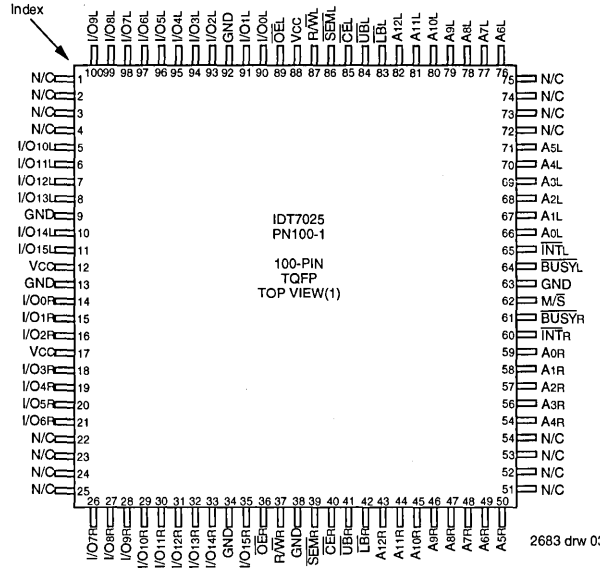
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by Chip Enable ($\overline{CE}$) permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500µW from a 2V battery.

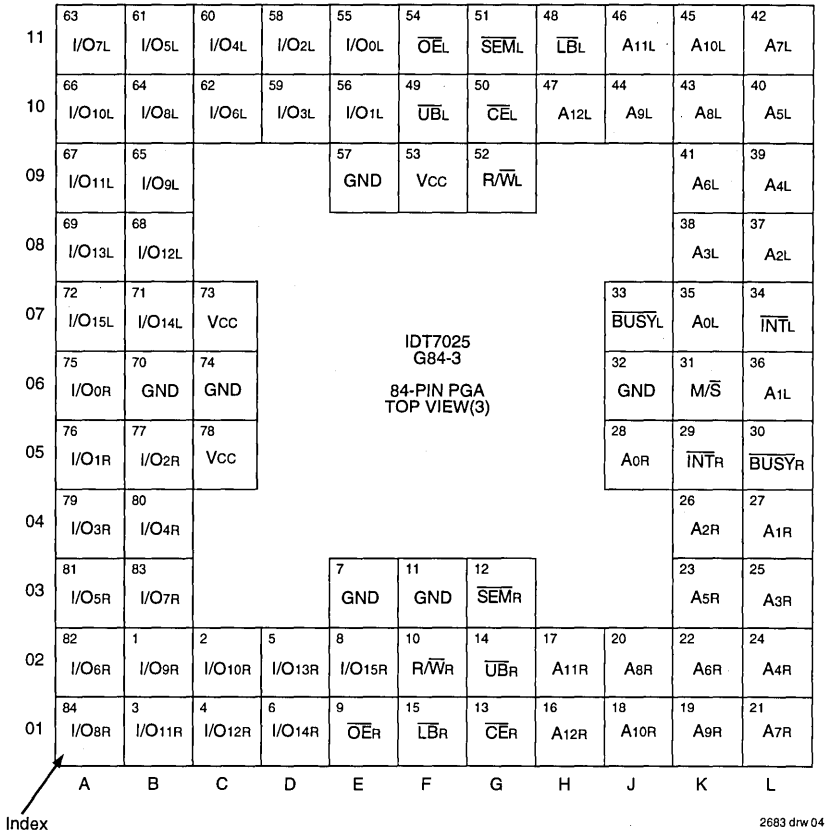
The IDT7025 is packaged in a ceramic 84-pin PGA, an 84-pin quad flatpack, PLCC, and a 100-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS





NOTE:
1. This text does not indicate orientation of the actual part- marking



	A	B	C	D	E	F	G	H	J	K	L
11	63 I/O7L	61 I/O5L	60 I/O4L	58 I/O2L	55 I/O0L	54 $\overline{OE}_L$	51 $\overline{SEM}_L$	48 $\overline{LB}_L$	46 A11L	45 A10L	42 A7L
10	66 I/O10L	64 I/O8L	62 I/O6L	59 I/O3L	56 I/O1L	49 $\overline{UB}_L$	50 $\overline{CE}_L$	47 A12L	44 A9L	43 A8L	40 A5L
09	67 I/O11L	65 I/O9L			57 GND	53 VCC	52 R/$\overline{W}_L$			41 A6L	39 A4L
08	69 I/O13L	68 I/O12L								38 A3L	37 A2L
07	72 I/O15L	71 I/O14L	73 VCC						33 $\overline{BUSY}_L$	35 A0L	34 $\overline{INT}_L$
06	75 I/O0R	70 GND	74 GND						32 GND	31 M/$\overline{S}$	36 A1L
05	76 I/O1R	77 I/O2R	78 VCC						28 A0R	29 $\overline{INT}_R$	30 $\overline{BUSY}_R$
04	79 I/O3R	80 I/O4R								26 A2R	27 A1R
03	81 I/O5R	83 I/O7R			7 GND	11 GND	12 $\overline{SEM}_R$			23 A5R	25 A3R
02	82 I/O6R	1 I/O9R	2 I/O10R	5 I/O13R	8 I/O15R	10 R/$\overline{W}_R$	14 $\overline{UB}_R$	17 A11R	20 A8R	22 A6R	24 A4R
01	84 I/O8R	3 I/O11R	4 I/O12R	6 I/O14R	9 $\overline{OE}_R$	15 $\overline{LB}_R$	13 $\overline{CE}_R$	16 A12R	18 A10R	19 A9R	21 A7R

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A0L – A12L	A0R – A12R	Address
I/O0L – I/O15L	I/O0R – I/O15R	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
M/$\overline{S}$		Master or Slave Select
VCC		Power
GND		Ground

2683 tbl 01

NOTES:
1. All VCC pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	X	X	X	X	H	High-Z	High-Z	Deselected:
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	H	DATAIN	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

NOTE:
1. A_{0L} — A_{12L} are not equal to A_{0R} — A_{12R}

2683 tbl 02

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Semaphore Flag Data Out
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Semaphore Flag Data Out
H	↑	X	X	X	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
X	↑	X	H	H	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

2683 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTES:
2683 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20 mA for the period over V_{TERM} ≥ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2683 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTES:
2683 tbl 06

1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz) [1]

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

NOTE:
2683 tbl 07

1. This parameter is determined by device characterization but is not production tested. For TQFP Package Only.
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7025S		IDT7025L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2683 tbl 08

NOTE:
1. At Vcc = 2.0V input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7025X17 COM'L ONLY		7025X20 COM'L ONLY		7025X25		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	—	—	155	340	mA
				L	—	—	—	—	155	280	
			COM.	S	170	310	160	290	155	265	
				L	170	260	160	240	155	220	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	MIL	S	—	—	—	—	16	80	mA
				L	—	—	—	—	16	65	
			COM	S	20	60	20	60	16	60	
				L	20	50	20	50	16	50	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_{"A"}$=V_{IL} and $\overline{CE}_{"B"}$=V_{IH}[5,] Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	MIL	S	—	—	—	—	90	215	mA
				L	—	—	—	—	90	180	
			COM	S	105	190	95	180	90	170	
				L	105	160	95	150	90	140	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ Vcc-0.2V	MIL	S	—	—	—	—	1.0	30	mA
				L	—	—	—	—	0.2	10	
			COM	S	1.0	15	1.0	15	1.0	15	
				L	0.2	5	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_{"A"}$ ≤ 0.2 and $\overline{CE}_{"B"}$ ≥ V_{CC} - 0.2V $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ Vcc-0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs f = f_{MAX}[3]	MIL	S	—	—	—	—	85	200	mA
				L	—	—	—	—	85	170	
			COM	S	100	170	90	155	85	145	
				L	100	140	90	130	85	120	

NOTES:
2683 tbl 09

1. 'X' in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. Icc dc = 120mA (TYP)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/ RC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7024X35 Typ.[2]	7024X35 Max.	7024X55 Typ.[2]	7024X55 Max.	7024X70 MIL ONLY Typ.[2]	7024X70 MIL ONLY Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open; $\overline{SEM}$ = V_{IH}; f = f_{MAX}[3]	MIL.	S	150	300	150	300	140	300	mA
				L	150	250	150	250	140	250	
			COM'L.	S	150	250	150	250	—	—	
				L	150	210	150	210	—	—	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE_L}$ = $\overline{CE_R}$ = V_{IH}; $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH}; f = f_{MAX}[3]	MIL.	S	13	80	13	80	10	80	mA
				L	13	65	13	65	10	65	
			COM'L.	S	13	60	13	60	—	—	
				L	13	50	13	50	—	—	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A"=V_{IL} and $\overline{CE}$"B"=V_{IH}[5]; Active Port Outputs Open; f = f_{MAX}[3]; $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH}	MIL.	S	85	190	85	190	80	190	mA
				L	85	160	85	160	80	160	
			COM'L.	S	85	155	85	155	—	—	
				L	85	130	85	130	—	—	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{CC} - 0.2V; V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4]; $\overline{SEM_R}$ = $\overline{SEM_L}$ ≥ V_{CC} - 0.2V	MIL.	S	1.0	30	1.0	30	1.0	30	mA
				L	0.2	10	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	—	—	
				L	0.2	5	0.2	5	—	—	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2 and $\overline{CE}$"B" ≥ V_{CC} - 0.2V[5]; $\overline{SEM_R}$ = $\overline{SEM_L}$ ≥ V_{CC} - 0.2V; V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	80	175	80	175	75	175	mA
				L	80	150	80	150	75	150	
			COM'L.	S	80	135	80	135	—	—	
				L	80	110	80	110	—	—	

NOTES:
2683 tbl 10

1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested.
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L Version Only)

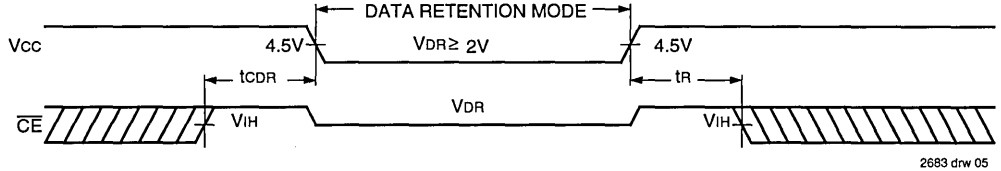
(V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)[4]

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	Vcc for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ ≥ V_{HC}	MIL.	—	100	4000	µA
		V_{IN} ≥ V_{HC} or ≤ V_{LC}	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time	$\overline{SEM}$ ≥ V_{HC}		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
2683 tbl 11

1. T_A = +25°C, V_{CC} = 2V, and are guaranted by characterization, but are not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.
4. At Vcc = 2.0V input leakages are undefined.

DATA RETENTION WAVEFORM



2683 drw 05

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2683 tbl 12

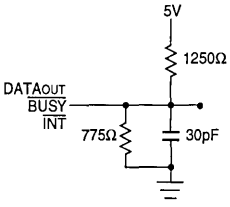


Figure 1. AC Output Test Load

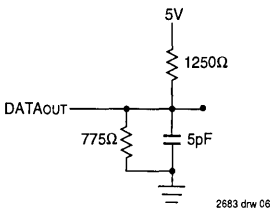


Figure 2. Output Test Load
(for tLZ, tHZ, tWZ, tOW)
* including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(4)

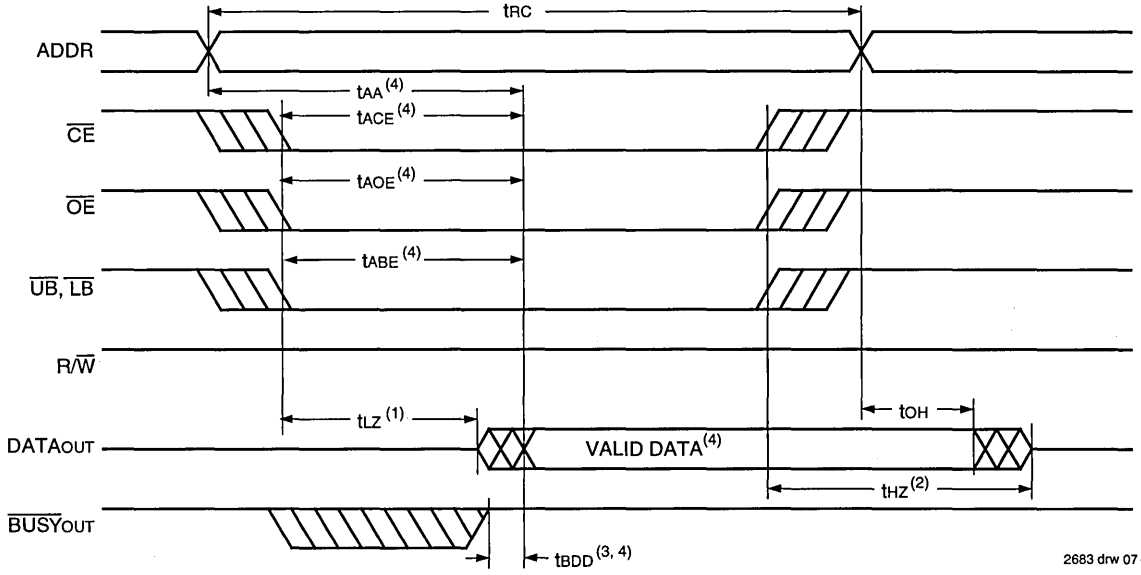
Symbol	Parameter	IDT7025X17 COM'L ONLY Min.	IDT7025X17 COM'L ONLY Max.	IDT7025X20 COM'L ONLY Min.	IDT7025X20 COM'L ONLY Max.	IDT7025X25 Min.	IDT7025X25 Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	17	—	20	—	25	—	ns
tAA	Address Access Time	—	17	—	20	—	25	ns
tACE	Chip Enable Access Time(3)	—	17	—	20	—	25	ns
tABE	Byte Enable Access Time(3)	—	17	—	20	—	25	ns
tAOE	Output Enable Access Time	—	10	—	12	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	3	—	3	—	3	—	ns
tHZ	Output High-Z Time(1, 2)	—	10	—	12	—	15	ns
tPU	Chip Enable to Power Up Time(1,2)	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(1,2)	—	17	—	20	—	25	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	10	—	ns
tSAA	Semaphore Address Access Time(3)	—	17	—	20	—	25	ns

Symbol	Parameter	IDT7025X35 Min.	IDT7025X35 Max.	IDT7025X55 Min.	IDT7025X55 Max.	IDT7025X70 MIL ONLY Min.	IDT7025X70 MIL ONLY Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	35	—	55	—	70	—	ns
tAA	Address Access Time	—	35	—	55	—	70	ns
tACE	Chip Enable Access Time(3)	—	35	—	55	—	70	ns
tABE	Byte Enable Access Time(3)	—	35	—	55	—	70	ns
tAOE	Output Enable Access Time	—	20	—	30	—	35	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	3	—	3	—	3	—	ns
tHZ	Output High-Z Time(1, 2)	—	15	—	25	—	30	ns
tPU	Chip Enable to Power Up Time(1,2)	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(1,2)	—	35	—	50	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns
tSAA	Semaphore Address Access Time(3)	—	35	—	55	—	70	ns

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterazation, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{UB}$ or $\overline{LB}$ = VIL, and $\overline{SEM}$ = VIH. To access semephore, $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIH, and $\overline{SEM}$ = VIL.
4. "X" in part numbers indicates power rating (S or L).

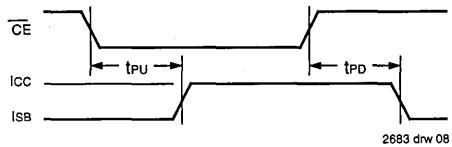
2683 tbl 13

WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first, $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. tBDD delay is required only in case where opposite port is completing a write operation to the same address location for simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tABE, tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[5]

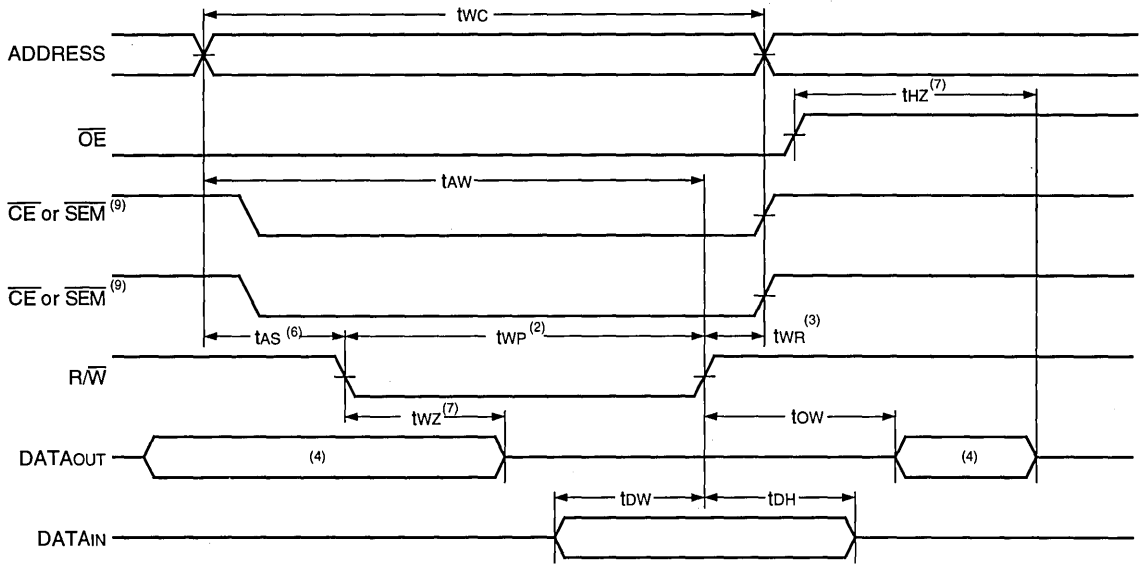
Symbol	Parameter	IDT7025X17 COM'L ONLY		IDT7025X20 COM'L ONLY		IDT7025X25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	17	—	20	—	25	—	ns
tEW	Chip Enable to End-of-Write[3]	12	—	15	—	20	—	ns
tAW	Address Valid to End-of-Write	12	—	15	—	20	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	10	—	15	—	15	—	ns
tHZ	Output High-Z Time[1, 2]	—	10	—	12	—	15	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	10	—	12	—	15	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

Symbol	Parameter	IDT7025X35		IDT7025X55		IDT7025X70 MIL. ONLY		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	35	—	55	—	70	—	ns
tEW	Chip Enable to End-of-Write[3]	30	—	45	—	50	—	ns
tAW	Address Valid to End-of-Write	30	—	45	—	50	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	25	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	30	—	40	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	25	—	30	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	15	—	25	—	30	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

NOTES: 2683 tbl 14

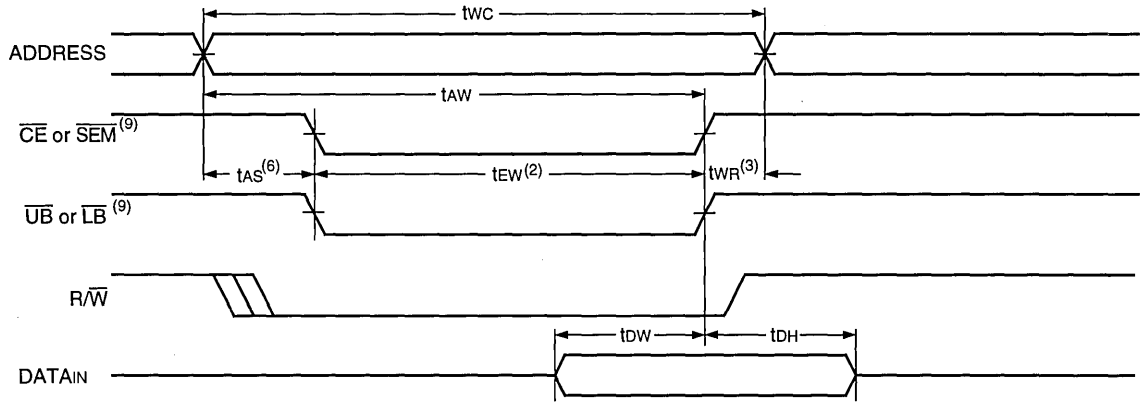
1. Transition is measured ±500mV from low or high impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{UB}$ or $\overline{LB}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIH, and $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,5,8)



2683 drw 09

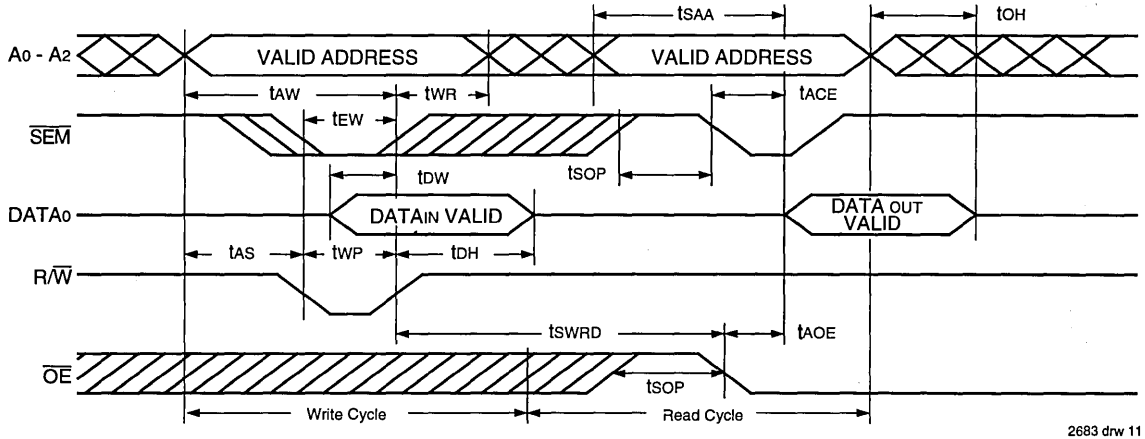
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING(1,5)



2683 drw 10

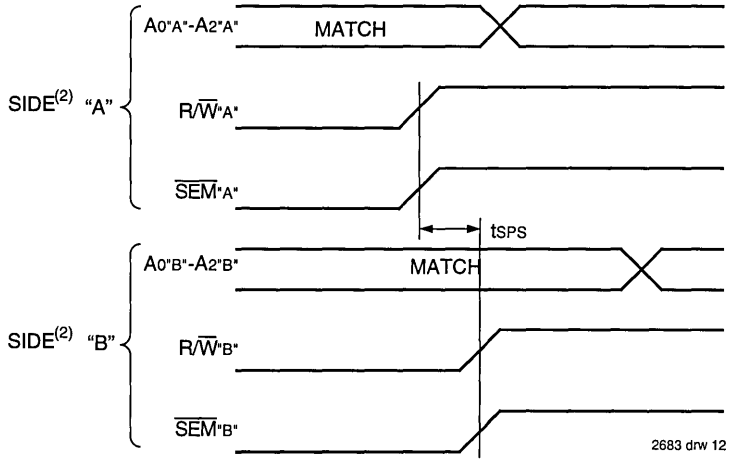
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ & $\overline{LB}$ must be High during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{UB}$ or $\overline{LB}$ and a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end-of-write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, R/$\overline{W}$, or byte control.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured +/- 500mV from steady state with Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ = VIL, $\overline{UB}$ or $\overline{LB}$ = VIL, and $\overline{SEM}$ = VIH. To access Semephore, $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIL, and $\overline{SEM}$ = VIL. tEW must be met for either condition.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}_R$ = $\overline{CE}_L$ = VIH, or both $\overline{UB}$ & $\overline{LB}$ = VIH.
2. All timing is the same for left and right port. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}$"A" or $\overline{SEM}$"A" going High to R/$\overline{W}$"B" or $\overline{SEM}$"B" going High.
4. If tSPS is not satisfied, there is no guarantee which side will obtain the semaphore flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	IDT7025X17 COM'L ONLY		IDT7025X20 COM'L ONLY		IDT7025X25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	17	—	20	—	20	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	17	—	20	—	20	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	17	—	20	—	20	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	17	—	17	—	17	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	17	—	20	—	25	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	13	—	15	—	17	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	30	—	45	—	50	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	25	—	30	—	35	ns

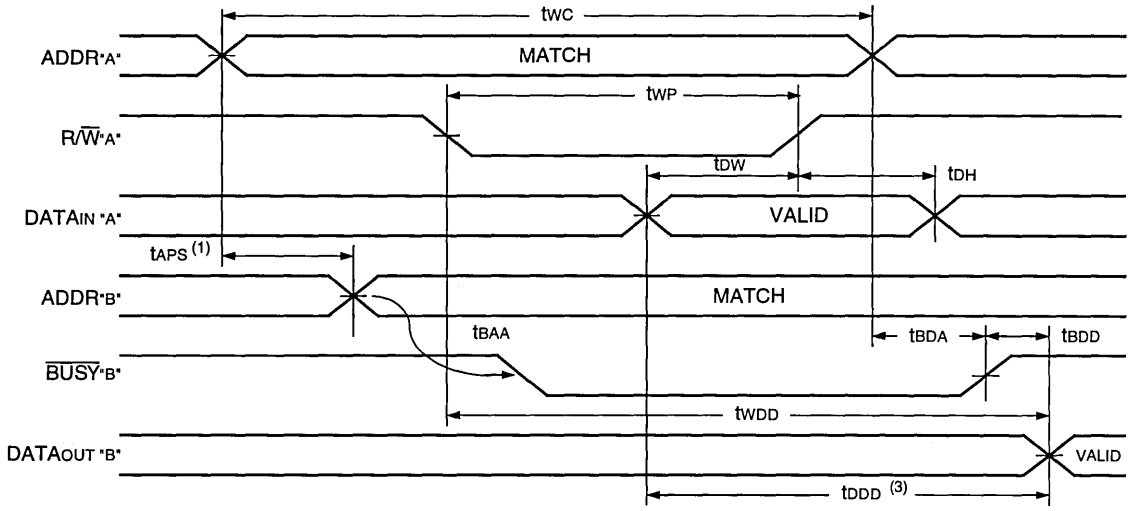
Symbol	Parameter	IDT7025X35		IDT7025X55		IDT7025X70 MIL. ONLY		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	20	—	45	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	40	—	40	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	40	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	20	—	35	—	35	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	35	—	55	—	70	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	60	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	45	—	65	—	80	ns

NOTES:

2683 tbl 15

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = H)" or "Timing Waveform of Write With Port-To-Port Delay (M/$\overline{S}$ = H)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0ns, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited pn Port "B" during contention with Port "A".
5. To ensure that a write cycle is completed on Port "B" after contention with Port "A".
6. "X" in part numbers indicates power rating (S or L).

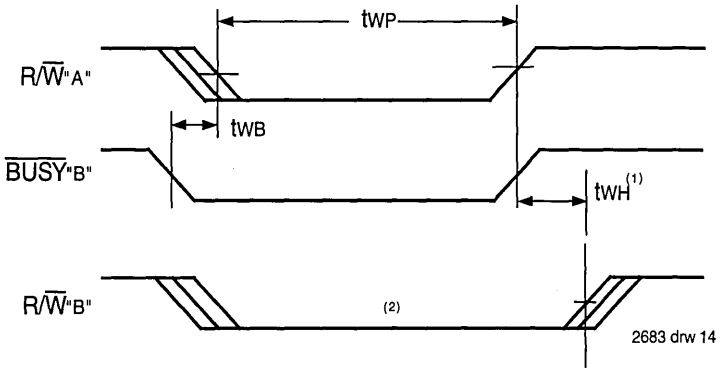
TIMING WAVEFORM OF WRITE PORT-TO-PORT READ AND $\overline{BUSY}^{(2,5)}$ ($M/\overline{S}$ = VIH)



NOTES:
1. To ensure that the earlier of the two ports wins. tAPSis ignored for M/S = VIL (slave).
2. $\overline{CE}L$ = $\overline{CE}R$ = VIL.
3. $\overline{OE}$ = VIL for the reading port.
4. If $M/\overline{S}$ = VIL (SLAVE) then $\overline{BUSY}$ is an input $\overline{BUSY}$"A" = VIL and $\overline{BUSY}$"B" = 'don't care'
5. All timing is the same for left and right ports. Port "A" may be either the left of right port. Port "B" is the opposite Port from Port "A".

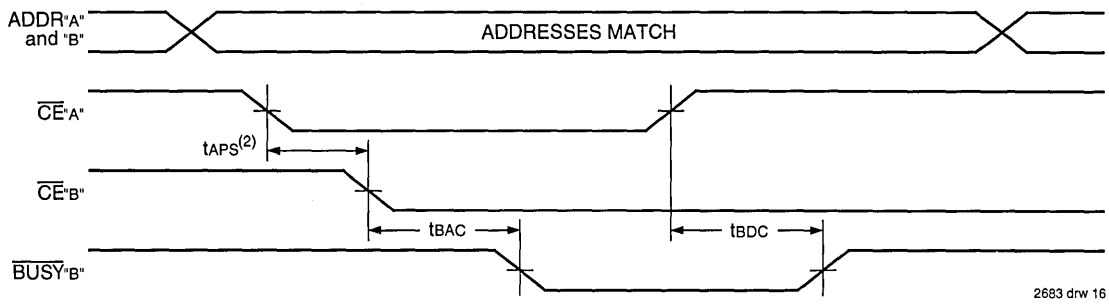
6

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$



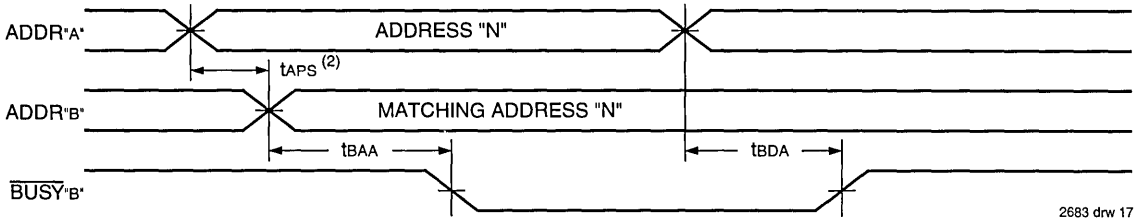
NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (slave) output master.
2. Busy is asserted on port "B" Blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes High

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING[1] (M/$\overline{S}$ = H)



2683 drw 16

WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING[1](M/$\overline{S}$ = H)



2683 drw 17

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

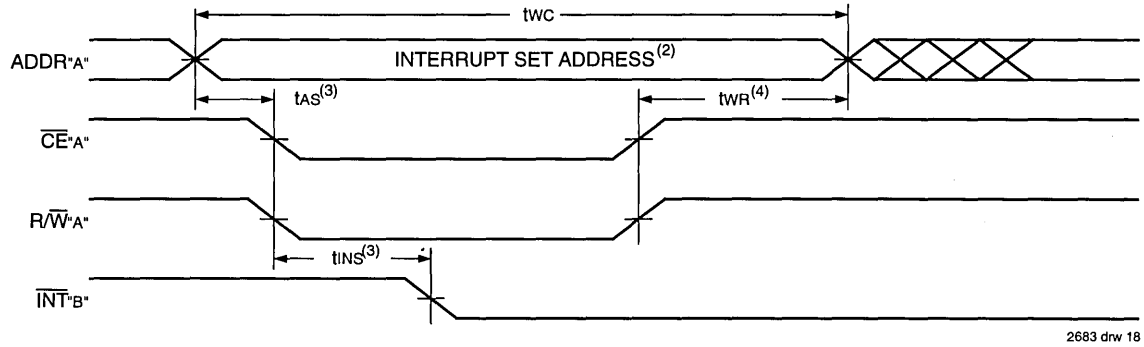
Symbol	Parameter	IDT7025X17 COM'L ONLY Min.	IDT7025X17 COM'L ONLY Max.	IDT7025X20 COM'L ONLY Min.	IDT7025X20 COM'L ONLY Max.	IDT7025X25 Min.	IDT7025X25 Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	15	—	20	—	20	ns
tINR	Interrupt Reset Time	—	15	—	20	—	20	ns

Symbol	Parameter	IDT7025X35 Min.	IDT7025X35 Max.	IDT7025X55 Min.	IDT7025X55 Max.	IDT7025X70 MIL. ONLY Min.	IDT7025X70 MIL. ONLY Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	40	—	50	ns
tINR	Interrupt Reset Time	—	25	—	40	—	50	ns

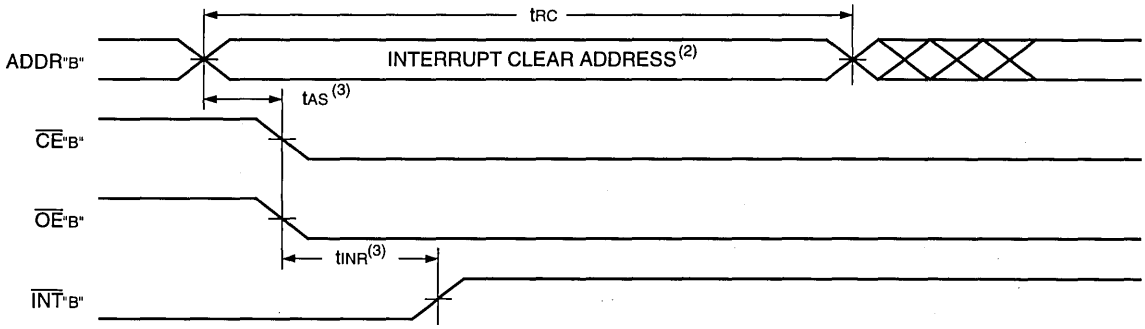
NOTE:
1. "X" in part numbers indicates power rating (S or L).

2683 tbl 16

WAVEFORM OF INTERRUPT TIMING[1]



2683 drw 18



2683 drw 19

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt Flag truth table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{12L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{12R}	$\overline{INT}_R$	Function
L	L	X	1FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	1FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	1FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	1FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = VIH.
2. If $\overline{BUSY}_L$ = VIL, then no change.
3. If $\overline{BUSY}_R$ = VIL, then no change.

2683 tbl 17

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{12L} A_{0R}-A_{12R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

NOTES: 2683 tbl 18

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. $\overline{BUSY}$ are inputs when configured as a slave. $\overline{BUSY}_X$ outputs on the IDT7025 are push pull, not open drain outputs. On slaves the $\overline{BUSY}$ asserted internally inhibits write.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If tAPS is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_{15} Left	D_0 - D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2683 tbl 19

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7025.

FUNCTIONAL DESCRIPTION

The IDT7025 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7025 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location FFE (HEX), where a write is defined as the $\overline{CE}_R$ = R/$\overline{W}_R$ = V_{IL} per the Truth Table. The left port clears the interrupt by an address location FFE access when $\overline{CE}_L$ = $\overline{OE}_L$ = V_{IL}, R/$\overline{W}_L$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must access the memory location FFF, The message (16 bits) at FFE or FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all

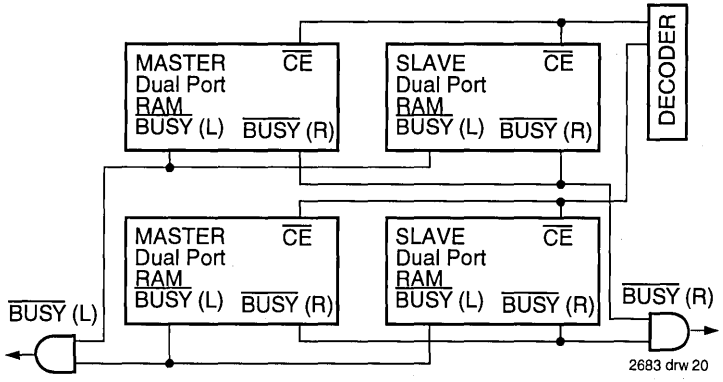


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7025 RAMs.

applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 7025 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7025 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7025 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7025 is an extremely fast Dual-Port 8K x 16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT7025 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7025's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources

6

to be allocated in varying configurations. The IDT7025 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7025 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a

resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7025's Dual-Port RAM. Say the 8K x 16 RAM was to be divided into two 4K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

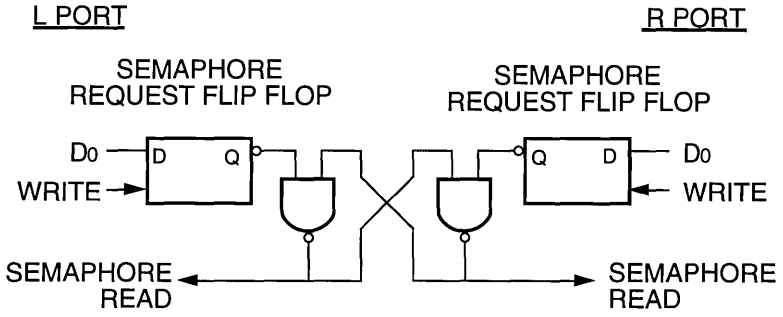
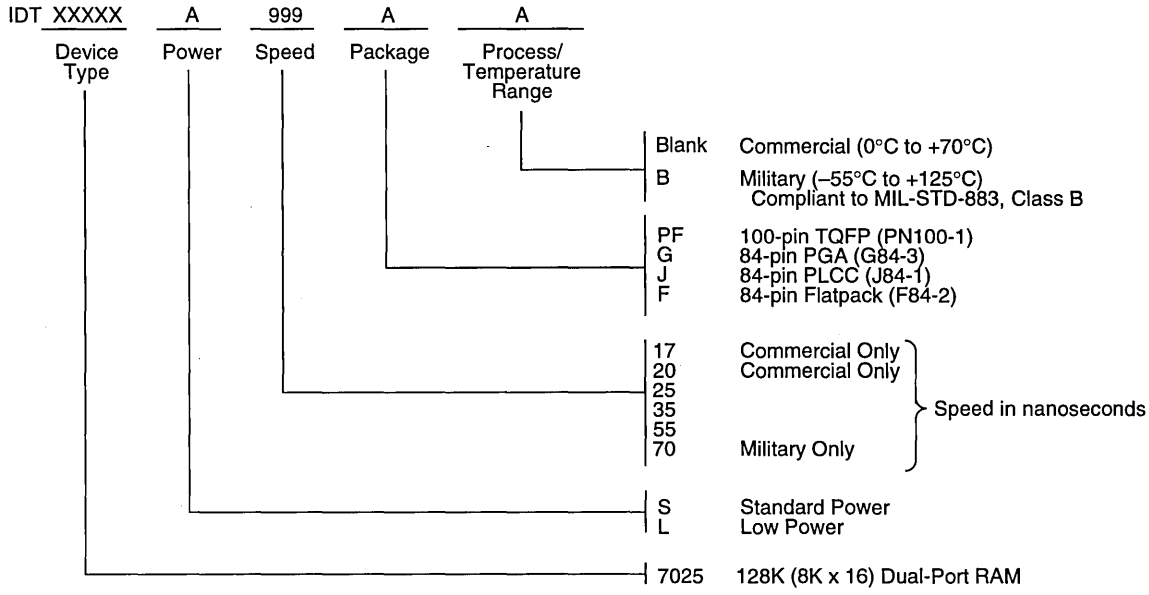


Figure 4. IDT7025 Semaphore Logic

ORDERING INFORMATION



2683 drw 21

Integrated Device Technology, Inc.

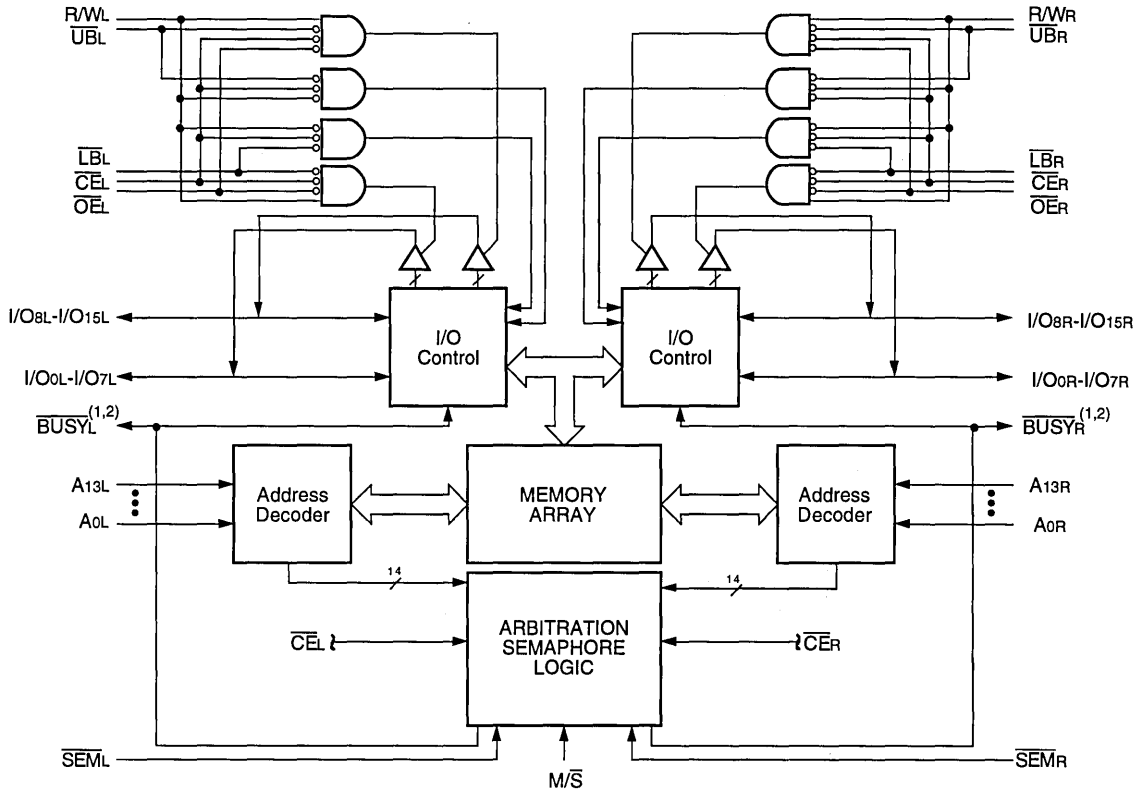
HIGH-SPEED 16K x 16 DUAL-PORT STATIC RAM

IDT7026S/L

FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 25/35/55ns (max.)
  - — Commercial: 20/25/35/55ns (max.)
- Low-power operation
  - — IDT7026S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7026L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT7026 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master,
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- TTL-compatible, single 5V (±10%) power supply
- Available in 84-pin PGA, and PLCC
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ outputs are non-tri-stated push-pull.

DESCRIPTION:

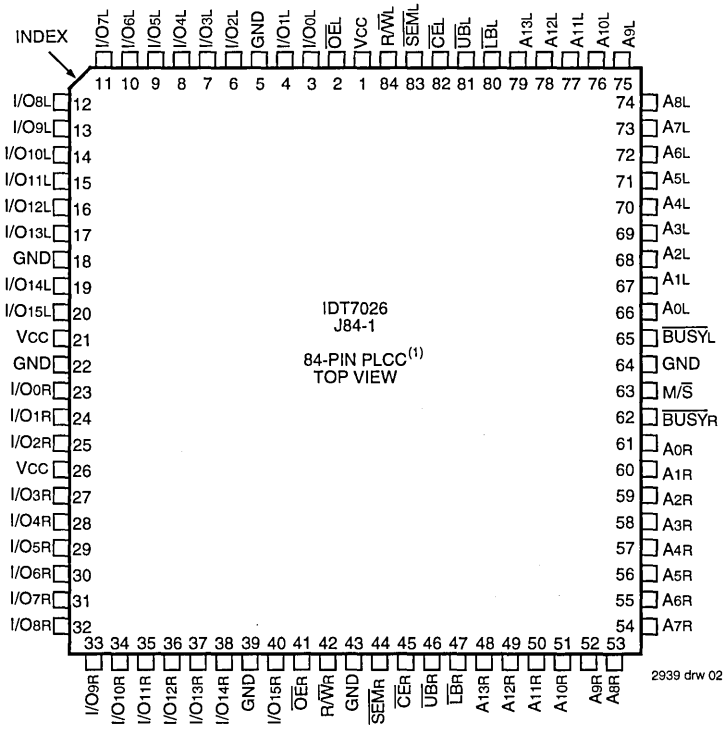
The IDT7026 is a high-speed 16K x 16 Dual-Port Static RAM. The IDT7026 is designed to be used as a stand-alone 256K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

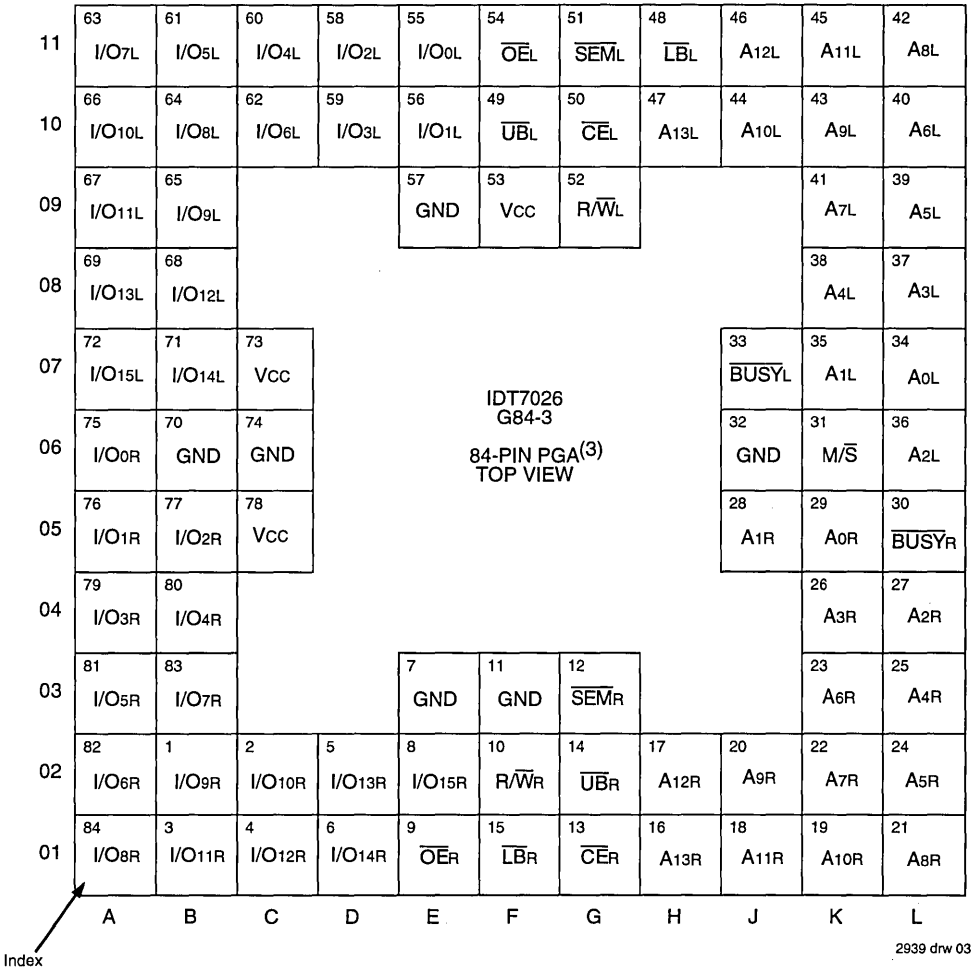
Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power.

The IDT7026 is packaged in a ceramic 84-pin PGA, an 84-pin quad flatpack, and PLCC. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



NOTE:
1. This text does not indicate orientation of the actual part-marking.



	A	B	C	D	E	F	G	H	J	K	L
11	63 I/O7L	61 I/O5L	60 I/O4L	58 I/O2L	55 I/O0L	54 $\overline{OE}_L$	51 $\overline{SEM}_L$	48 $\overline{LB}_L$	46 A12L	45 A11L	42 A8L
10	66 I/O10L	64 I/O8L	62 I/O6L	59 I/O3L	56 I/O1L	49 $\overline{UB}_L$	50 $\overline{CE}_L$	47 A13L	44 A10L	43 A9L	40 A6L
09	67 I/O11L	65 I/O9L			57 GND	53 VCC	52 R/$\overline{W}_L$			41 A7L	39 A5L
08	69 I/O13L	68 I/O12L								38 A4L	37 A3L
07	72 I/O15L	71 I/O14L	73 VCC						33 $\overline{BUSY}_L$	35 A1L	34 A0L
06	75 I/O0R	70 GND	74 GND						32 GND	31 M/$\overline{S}$	36 A2L
05	76 I/O1R	77 I/O2R	78 VCC						28 A1R	29 A0R	30 $\overline{BUSY}_R$
04	79 I/O3R	80 I/O4R								26 A3R	27 A2R
03	81 I/O5R	83 I/O7R			7 GND	11 GND	12 $\overline{SEM}_R$			23 A6R	25 A4R
02	82 I/O6R	1 I/O9R	2 I/O10R	5 I/O13R	8 I/O15R	10 R/$\overline{W}_R$	14 $\overline{UB}_R$	17 A12R	20 A9R	22 A7R	24 A5R
01	84 I/O8R	3 I/O11R	4 I/O12R	6 I/O14R	9 $\overline{OE}_R$	15 $\overline{LB}_R$	13 $\overline{CE}_R$	16 A13R	18 A11R	19 A10R	21 A8R

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A0L – A13L	A0R – A13R	Address
I/O0L – I/O15L	I/O0R – I/O15R	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
M/$\overline{S}$		Master or Slave Select
VCC		Power
GND		Ground

2939 tbl 01

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power-Down
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	H	DATAIN	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

NOTE: 2939 tbl 02
1. $A_{0L} — A_{13L} \neq A_{0R} — A_{13R}$

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
H	↓	X	X	X	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
X	↓	X	H	H	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

2939 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2939 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq$ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2939 tbl 05

RECOMMENDED DC OPERATING CONDTIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2939 tbl 06
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dv	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dv	10	pF

NOTE: 2939 tbl 07
1. This parameter is determined by device characterization but is not production tested.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7026S		IDT7026L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA	2.4	—	2.4	—	V

NOTE:
1. At V_{CC} = 2.0V, input leakages are undefined.

2939 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7026X20 COM'L ONLY		7026X25		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	170	345	mA
				L	—	—	170	305	
			COM'L.	S	180	315	170	305	
				L	180	275	170	265	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	MIL.	S	—	—	25	100	mA
				L	—	—	25	80	
			COM'L.	S	30	85	25	85	
				L	30	60	25	60	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	MIL.	S	—	—	105	230	mA
				L	—	—	105	200	
			COM'L.	S	115	210	105	200	
				L	115	180	105	170	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V	MIL.	S	—	—	1.0	30	mA
				L	—	—	0.2	10	
			COM'L.	S	1.0	15	1.0	15	
				L	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	MIL.	S	—	—	100	200	mA
				L	—	—	100	175	
			COM'L.	S	110	185	100	170	
				L	110	160	100	145	

NOTES:
1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1 / t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

2939 tbl 09

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1](Continued) (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7026X35 Typ.[2]	7026X35 Max.	7026X55 Typ.[2]	7026X55 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	MIL.	S	160	335	150	310	mA
				L	160	295	150	270	
			COM'L.	S	160	295	150	270	
				L	160	255	150	230	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE_L}$ = $\overline{CE_R}$ = V_{IH} $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH} f = f_{MAX}[3]	MIL.	S	20	100	13	100	mA
				L	20	80	13	80	
			COM'L.	S	20	85	13	85	
				L	20	60	13	60	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A"=V_{IL} and $\overline{CE}$"B"=V_{IH}[5] Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH}	MIL.	S	95	215	85	195	mA
				L	95	185	85	165	
			COM'L.	S	95	185	85	165	
				L	95	155	85	135	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ V_{CC} - 0.2V	MIL.	S	1.0	30	1.0	30	mA
				L	0.2	10	0.2	10	
		V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM_R}$ = $\overline{SEM_L}$ ≥V_{CC} - 0.2V	COM'L.	S	1.0	15	1.0	15	
				L	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{CC} - 0.2V[5] $\overline{SEM_R}$ = $\overline{SEM_L}$ ≥V_{CC} - 0.2V	MIL.	S	90	190	80	165	mA
				L	90	165	80	140	
		V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	COM'L.	S	90	160	80	135	mA
				L	90	135	80	110	

NOTES: 2939 tbl 10

1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/ tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2939 tbl 11

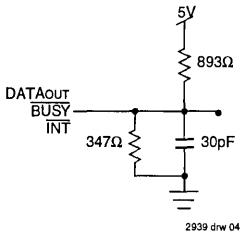


Figure 1. AC Output Load

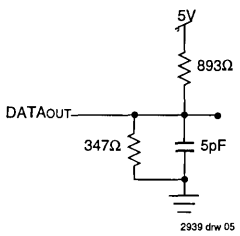


Figure 2. Output Test Load
(for tLZ, tHZ, twz, tow)
* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(4)

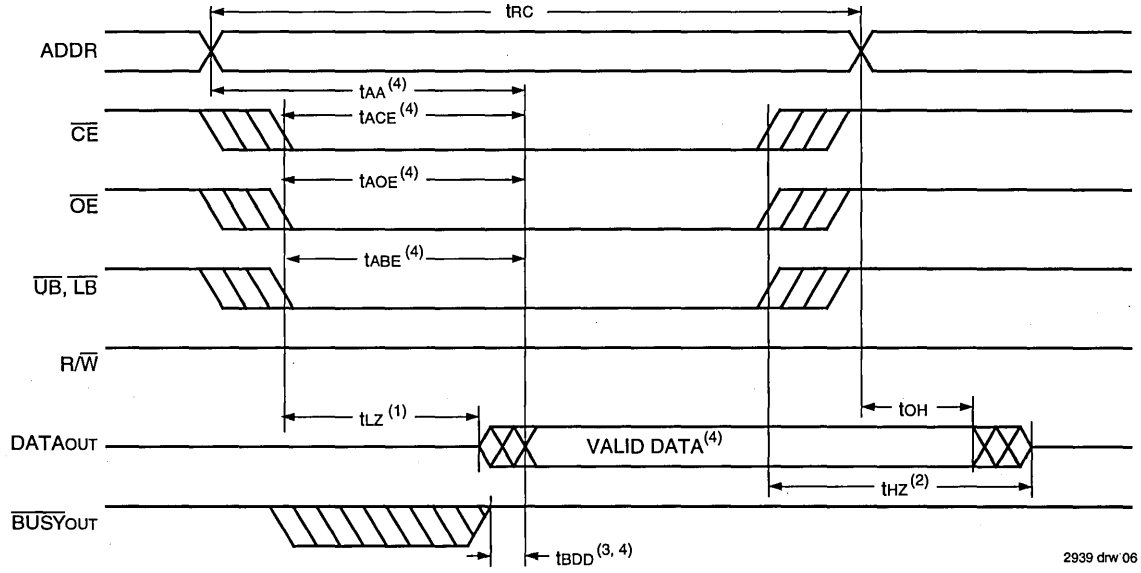
Symbol	Parameter	IDT7026X20 COM'L ONLY Min.	IDT7026X20 COM'L ONLY Max.	IDT7026X25 Min.	IDT7026X25 Max.	Unit
READ CYCLE						
tRC	Read Cycle Time	20	—	25	—	ns
tAA	Address Access Time	—	20	—	25	ns
tACE	Chip Enable Access Time(3)	—	20	—	25	ns
tABE	Byte Enable Access Time(3)	—	20	—	25	ns
tAOE	Output Enable Access Time	—	12	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	3	—	3	—	ns
tHZ	Output High-Z Time(1, 2)	—	12	—	15	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	20	—	25	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	12	—	ns
tSAA	Semaphore Address Access Time	—	20	—	25	ns

Symbol	Parameter	IDT7026X35 Min.	IDT7026X35 Max.	IDT7026X55 Min.	IDT7026X55 Max.	Unit
READ CYCLE						
tRC	Read Cycle Time	35	—	55	—	ns
tAA	Address Access Time	—	35	—	55	ns
tACE	Chip Enable Access Time(3)	—	35	—	55	ns
tABE	Byte Enable Access Time(3)	—	35	—	55	ns
tAOE	Output Enable Access Time	—	20	—	30	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	3	—	3	—	ns
tHZ	Output High-Z Time(1, 2)	—	15	—	25	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	35	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	ns
tSAA	Semaphore Address Access Time	—	35	—	55	ns

2939 tbl 12

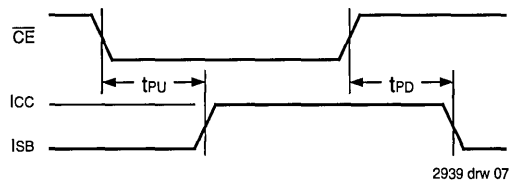
NOTES:
1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL.
4. "X" in part numbers indicates power rating (S or L).

WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (5)

Symbol	Parameter	IDT7026X20 COM'L ONLY Min.	IDT7026X20 COM'L ONLY Max.	IDT7026X05 Min.	IDT7026X05 Max.	Unit
WRITE CYCLE						
tWC	Write Cycle Time	20	—	25	—	ns
tEW	Chip Enable to End-of-Write(3)	15	—	20	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	ns
tAS	Address Set-up Time(3)	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	15	—	ns
tHZ	Output High-Z Time(1, 2)	—	12	—	15	ns
tDH	Data Hold Time(4)	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z(1, 2)	—	12	—	15	ns
tOW	Output Active from End-of-Write(1, 2, 4)	0	—	0	—	ns
tSWRD	SEM Flag Write to Read Time	5	—	5	—	ns
tSPS	SEM Flag Contention Window	5	—	5	—	ns

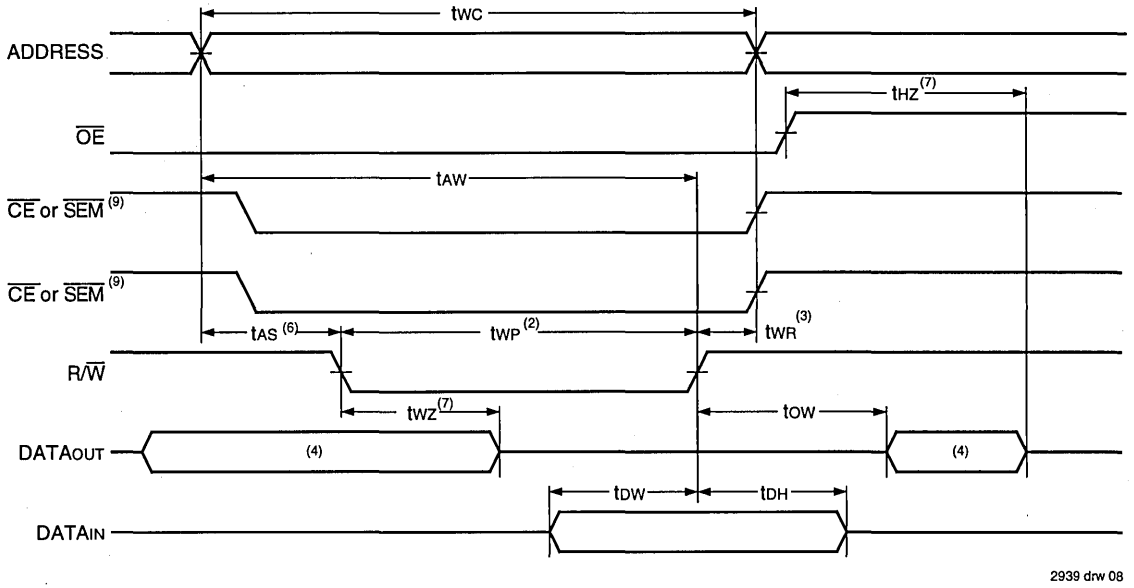
Symbol	Parameter	IDT7026X35 Min.	IDT7026X35 Max.	IDT7026X55 Min.	IDT7026X55 Max.	Unit
WRITE CYCLE						
tWC	Write Cycle Time	35	—	55	—	ns
tEW	Chip Enable to End-of-Write(3)	30	—	45	—	ns
tAW	Address Valid to End-of-Write	30	—	45	—	ns
tAS	Address Set-up Time(3)	0	—	0	—	ns
tWP	Write Pulse Width	25	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	30	—	ns
tHZ	Output High-Z Time(1, 2)	—	15	—	25	ns
tDH	Data Hold Time(4)	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z(1, 2)	—	15	—	25	ns
tOW	Output Active from End-of-Write(1, 2, 4)	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	ns

NOTES: 2939 tbl 13

1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. "X" in part numbers indicates power rating (S or L).

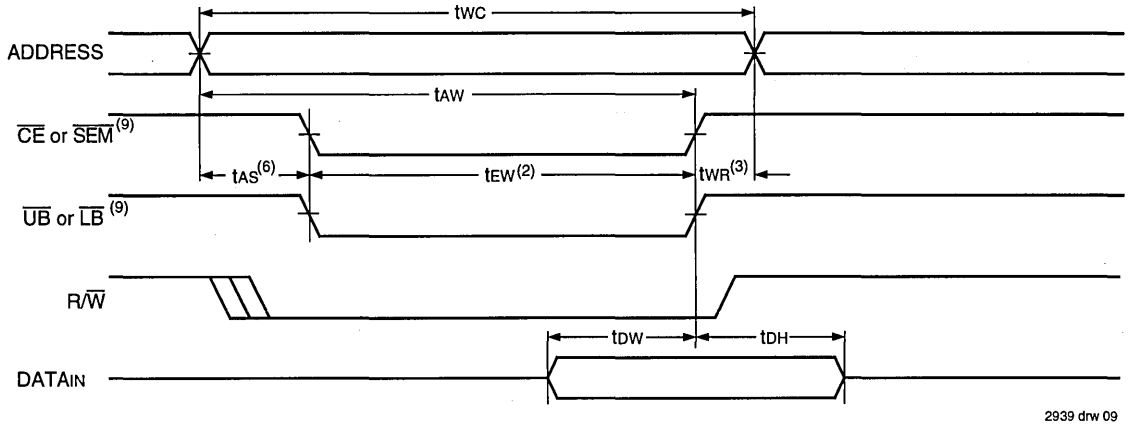
6

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING[1,5,8]



2939 drw 08

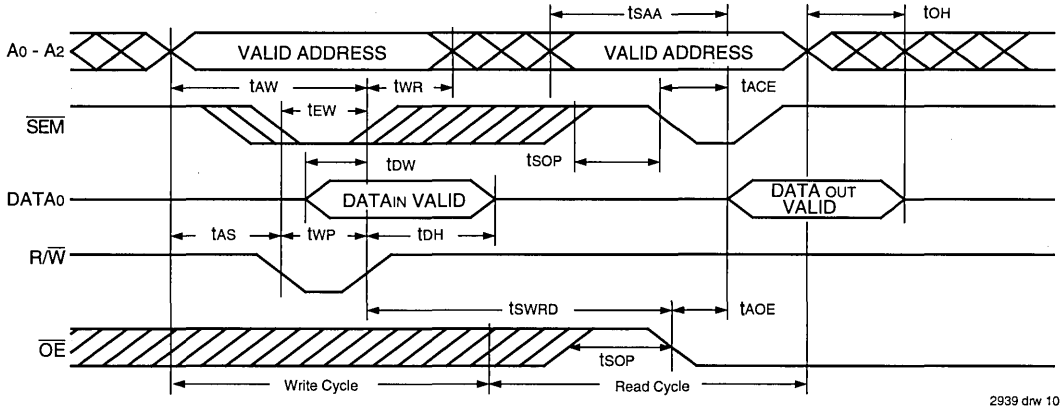
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING[1,5]



2939 drw 09

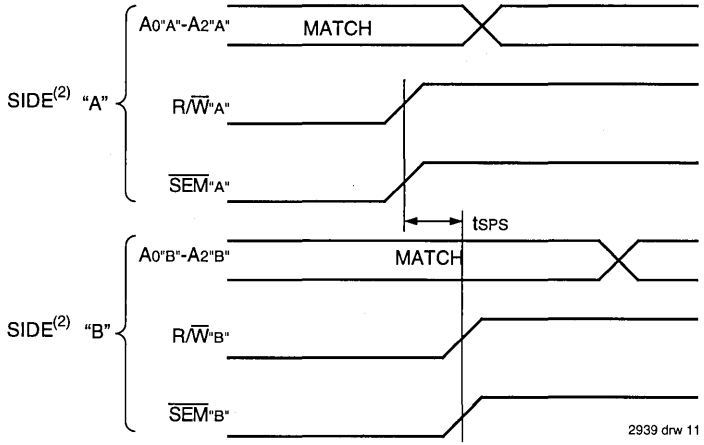
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ and $\overline{LB}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a LOW $\overline{CE}$ and a LOW R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured ± 200mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. tEW must be met for either condition.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH or $\overline{UB}$ and $\overline{LB}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}$R = $\overline{CE}$L = VIH, or both $\overline{UB}$ & $\overline{LB}$ = VIH.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}$"A" or $\overline{SEM}$"A" going HIGH to R/$\overline{W}$"B" or $\overline{SEM}$"B" going HIGH.
4. If tSPS is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

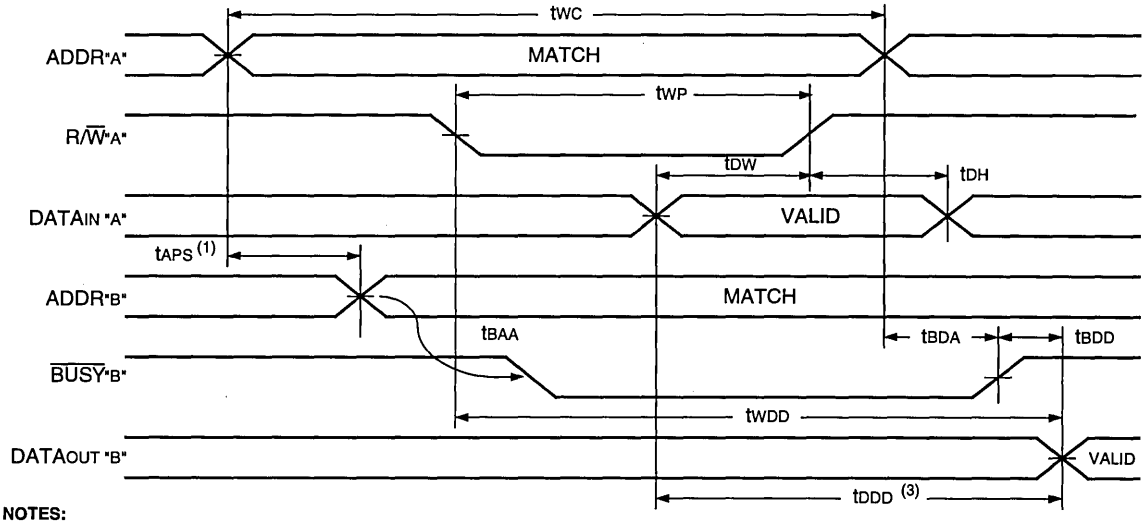
Symbol	Parameter	IDT7026X20 COM'L ONLY Min.	IDT7026X20 COM'L ONLY Max.	IDT7026X25 Min.	IDT7026X25 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)						
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	20	—	20	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	20	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	20	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	17	—	17	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	20	—	25	ns
BUSY TIMING (M/$\overline{S}$ = L)						
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	15	—	17	—	ns
PORT-TO-PORT DELAY TIMING						
tWDD	Write Pulse to Data Delay[1]	—	45	—	50	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	30	—	35	ns

Symbol	Parameter	IDT7026X35 Min.	IDT7026X35 Max.	IDT7026X55 Min.	IDT7026X55 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)						
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	20	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	40	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	20	—	35	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	35	—	55	ns
BUSY TIMING (M/$\overline{S}$ = L)						
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING						
tWDD	Write Pulse to Data Delay[1]	—	60	—	80	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	45	—	65	ns

NOTES: 2939 tbl 15

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = VIH)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$ (2,5) (M/$\overline{S}$ = VIH)

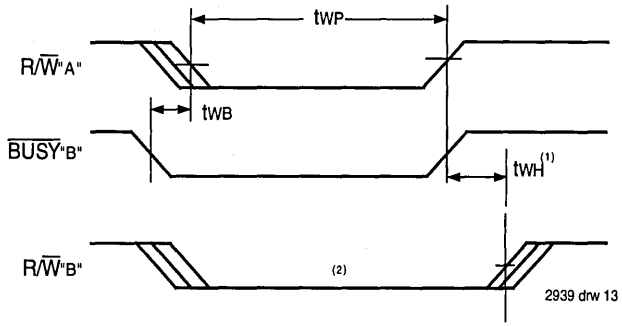


2939 drw 12

NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for M/$\overline{S}$ = VIL (SLAVE).
2. $\overline{CE}_L$ = $\overline{CE}_R$ = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. If M/$\overline{S}$ = VIL (SLAVE), then $\overline{BUSY}$ is an input ($\overline{BUSY}$"A" = VIH and $\overline{BUSY}$"B" = "don't care", for this example).
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

6

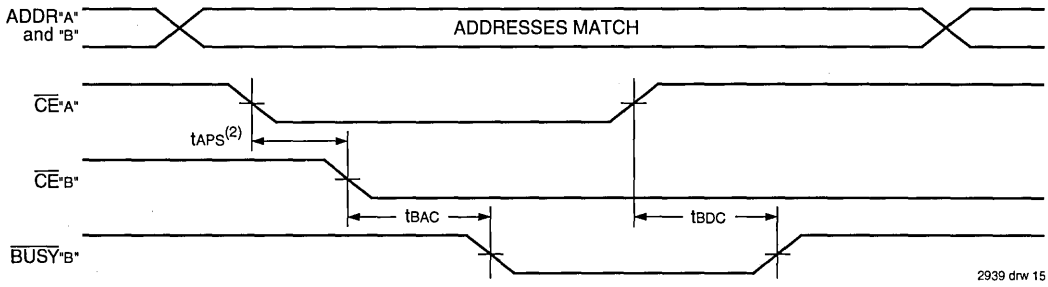
TIMING WAVEFORM OF WRITE WITH BUSY (M/$\overline{S}$ = VIL)



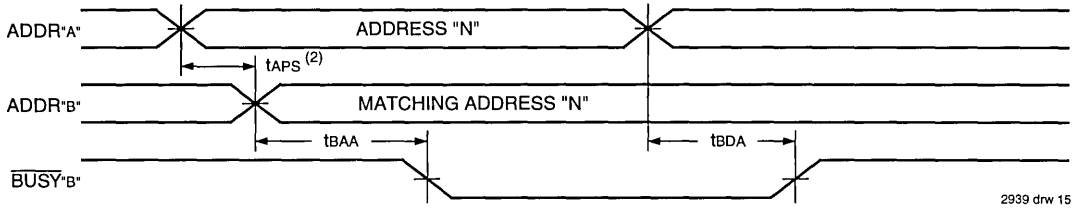
2939 drw 13

NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (SLAVE) and output (MASTER).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes High.

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1) (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)(M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

TRUTH TABLE I — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D0 - D15 Left	D0 - D15 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7026.

2683 tbl 16

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{13L} A_{0R}-A_{13R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

NOTES: 2683 tbl 17

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$x outputs on the IDT7026 are push pull, not open drain outputs. On slaves the $\overline{BUSY}$x input internally inhibits writes.
2. LOW if the inputs to the opposite port were stable prior to the address and enable inputs of this port. HIGH if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

FUNCTIONAL DESCRIPTION

The IDT7026 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7026 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ HIGH). When a port is enabled, access to the entire memory array is permitted.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins HIGH. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port LOW.

The busy outputs on the IDT 7026 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT7026 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7026 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

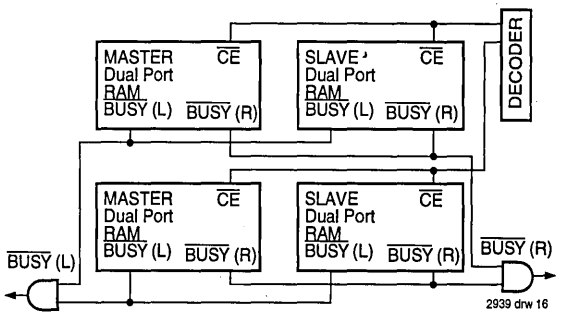


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7026 RAMs.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT7026 is an extremely fast Dual-Port 16K x 16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard

6

CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both HIGH.

Systems which can best use the IDT7026 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7026's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7026 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7026 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a

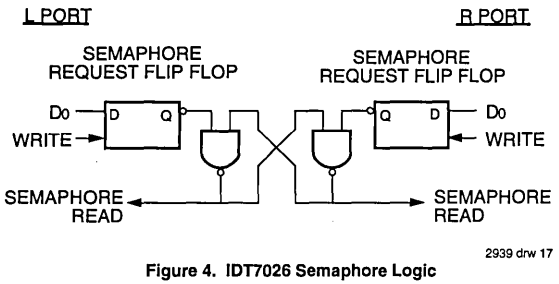


Figure 4. IDT7026 Semaphore Logic

one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7026's Dual-Port RAM. Say the 16K x 16 RAM was to be divided into two 8K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 8K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of Dual-Port RAM with each other.

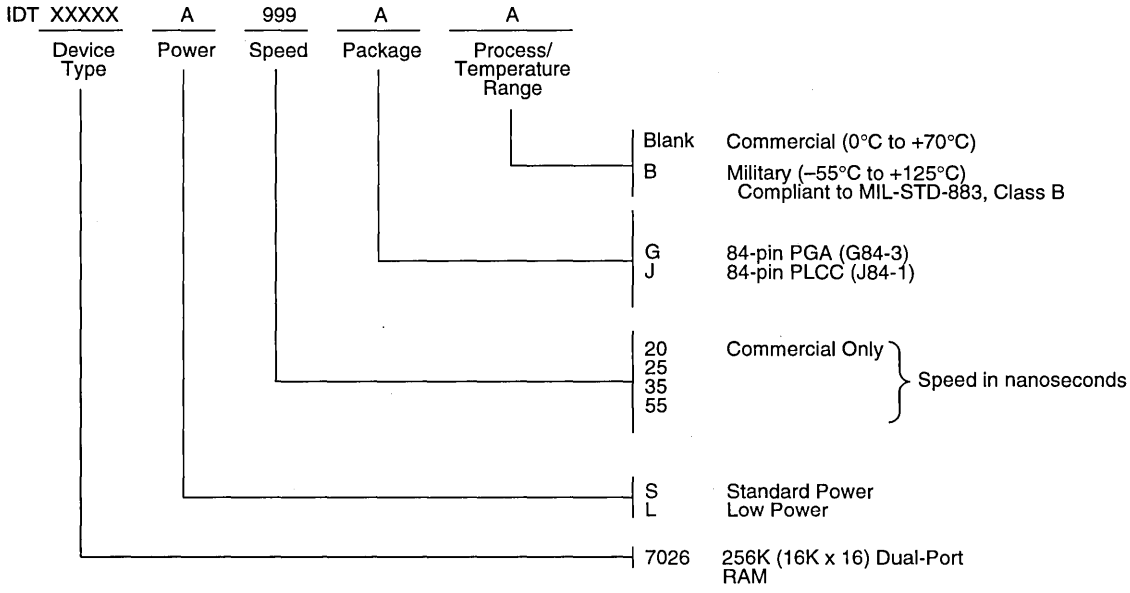
The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

ORDERING INFORMATION



2939 drw 18

Integrated Device Technology, Inc.

HIGH-SPEED 16K x 16 DUAL-PORT STATIC RAM

IDT70261S/L

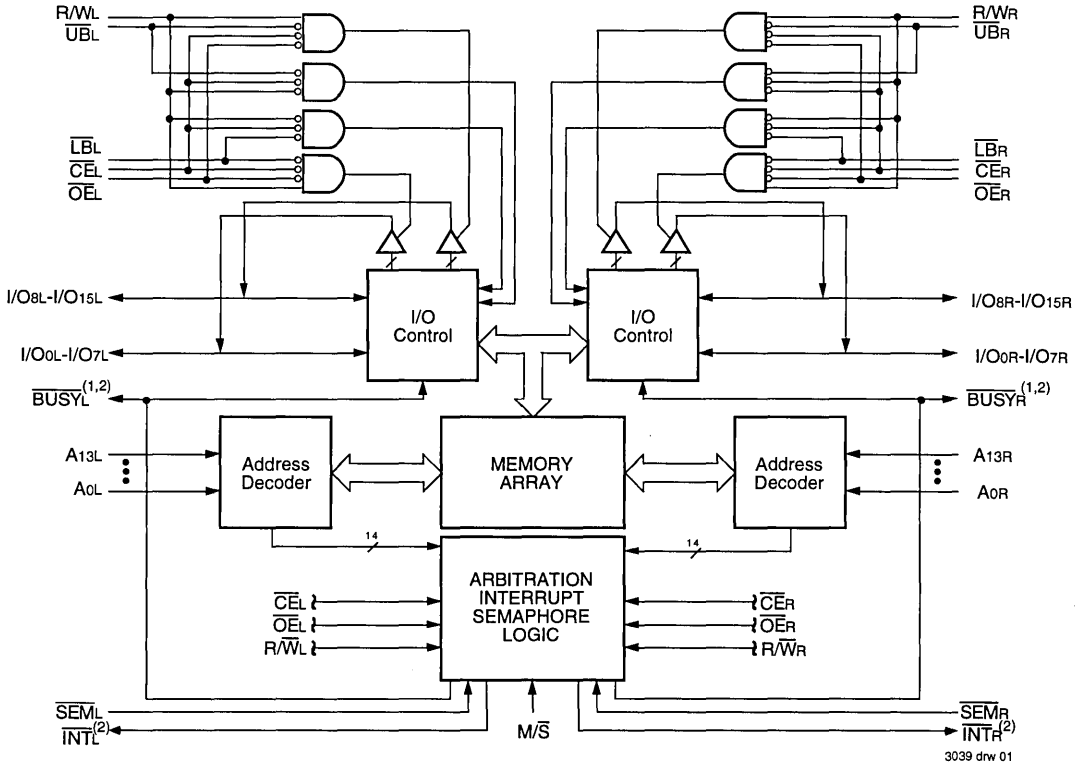
FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Commercial: 20/25/35/55ns (max.)
- Low-power operation
  - — IDT70261S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT70261L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT70261 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master,
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- TTL-compatible, single 5V (±10%) power supply
- Available in 100-pin Thin Quad Plastic Flatpack

DESCRIPTION:

The IDT70261 is a high-speed 16K x 16 Dual-Port Static RAM. The IDT70261 is designed to be used as a stand-alone 256K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ and $\overline{INT}$ outputs are non-tri-stated push-pull.

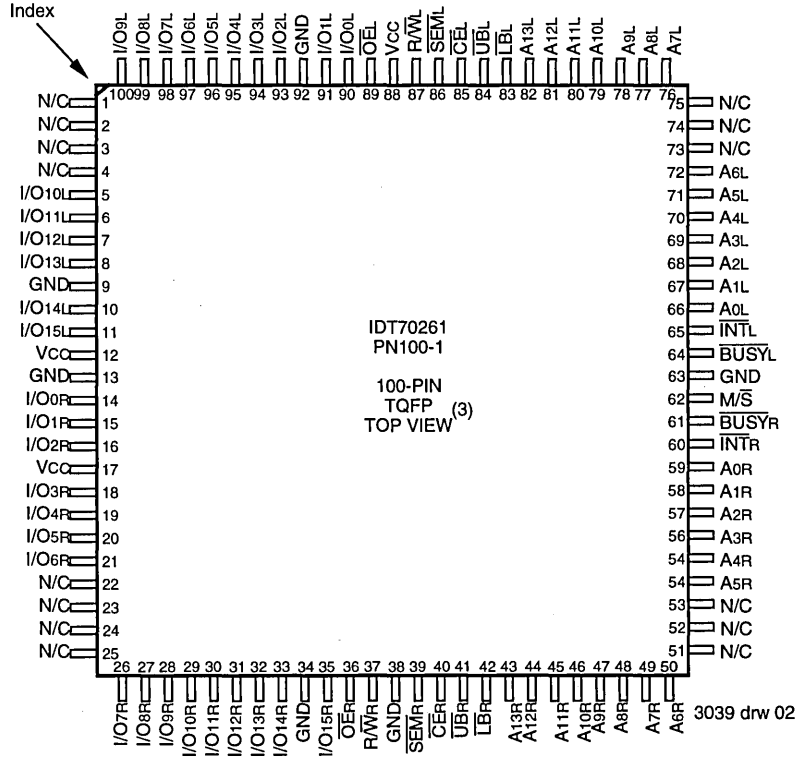
speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power.

The IDT70261 is packaged in a 100-pin TQFP.

PIN CONFIGURATIONS



PIN NAMES (1,2)

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{13L}$	$A_{0R} - A_{13R}$	Address
$I/O_{0L} - I/O_{15L}$	$I/O_{0R} - I/O_{15R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

3039 tbl 01

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power-Down
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	H	DATAIN	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

NOTE: 3039 tbl 02
1. $A_{0L} — A_{13L} \neq A_{0R} — A_{13R}$

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
H	↑	X	X	X	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
X	↑	X	H	H	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

3039 tbl 03

6

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 3039 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq$ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

3039 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 3039 tbl 06
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

NOTE: 3039 tbl 07
1. This parameter is determined by device characterization but is not production tested. TQFP package only.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT70261S		IDT70261L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

NOTE:
1. At V_{CC} = 2.0V, input leakages are undefined.

3039 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		70261X20		70261X25		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L.	S	180	315	170	305	mA
				L	180	275	170	265	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L.	S	30	85	25	85	mA
				L	30	60	25	60	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5] Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L.	S	115	210	105	200	mA
				L	115	180	105	170	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	COM'L.	S	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{CC} - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	COM'L.	S	110	185	100	170	mA
				L	110	160	100	145	

NOTES:
1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1 / t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

3039 tbl 09

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		70261X35 Typ.[2]	70261X35 Max.	70261X55 Typ.[2]	70261X55 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L.	S	160	295	150	270	mA
				L	160	255	150	230	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L.	S	20	85	13	85	mA
				L	20	60	13	60	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5] Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L.	S	95	185	85	165	mA
				L	95	155	85	135	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	COM'L.	S	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{CC} - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ Vc 265 V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	COM'L.	S	90	160	90	135	mA
				L	90	135	80	110	

NOTES:

3039 tbl 10

1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CCDC} = 120mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/ tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

6

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

3039 tbl 11

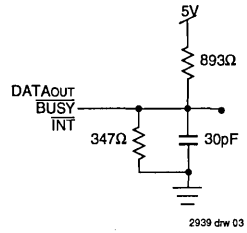


Figure 1. AC Output Load

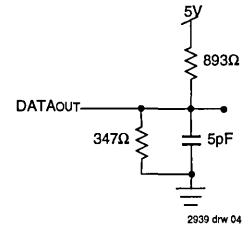


Figure 2. Output Test Load
(for tLZ, tHZ, twz, tow)
Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(4)

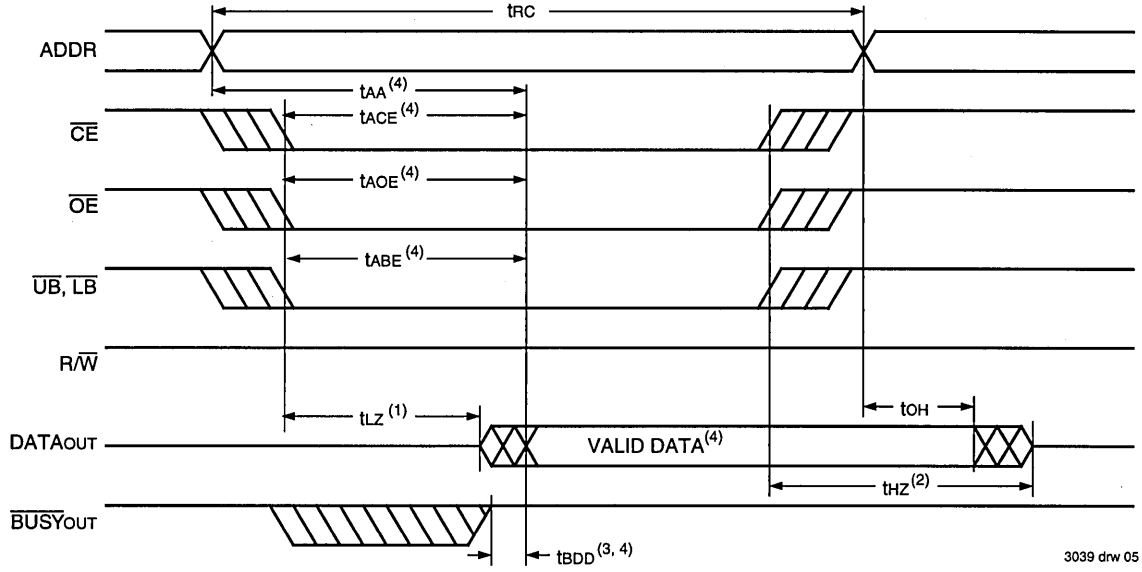
Symbol	Parameter	IDT70261X20 Min.	IDT70261X20 Max.	IDT70261X25 Min.	IDT70261X25 Max.	Unit
READ CYCLE						
tRC	Read Cycle Time	20	—	25	—	ns
tAA	Address Access Time	—	20	—	25	ns
tACE	Chip Enable Access Time(3)	—	20	—	25	ns
tABE	Byte Enable Access Time(3)	—	20	—	25	ns
tAOE	Output Enable Access Time	—	12	—	13	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	3	—	3	—	ns
tHZ	Output High-Z Time(1, 2)	—	12	—	15	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	20	—	25	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	12	—	ns
tSAA	Semaphore Address Access Time	—	20	—	25	ns

Symbol	Parameter	IDT70261X35 Min.	IDT70261X35 Max.	IDT70261X55 Min.	IDT70261X55 Max.	Unit
READ CYCLE						
tRC	Read Cycle Time	35	—	55	—	ns
tAA	Address Access Time	—	35	—	55	ns
tACE	Chip Enable Access Time(3)	—	35	—	55	ns
tABE	Byte Enable Access Time(3)	—	35	—	55	ns
tAOE	Output Enable Access Time	—	20	—	30	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	3	—	3	—	ns
tHZ	Output High-Z Time(1, 2)	—	15	—	25	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	35	—	55	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	ns
tSAA	Semaphore Address Access Time	—	35	—	55	ns

3039 tbl 12

NOTES:
1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL.
4. "X" in part numbers indicates power rating (S or L).

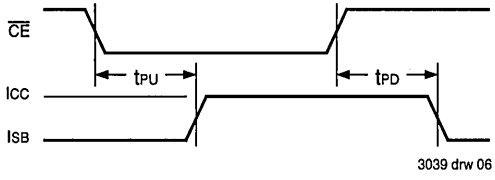
WAVEFORM OF READ CYCLES(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

6

TIMING OF POWER-UP POWER-DOWN



AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE [5]

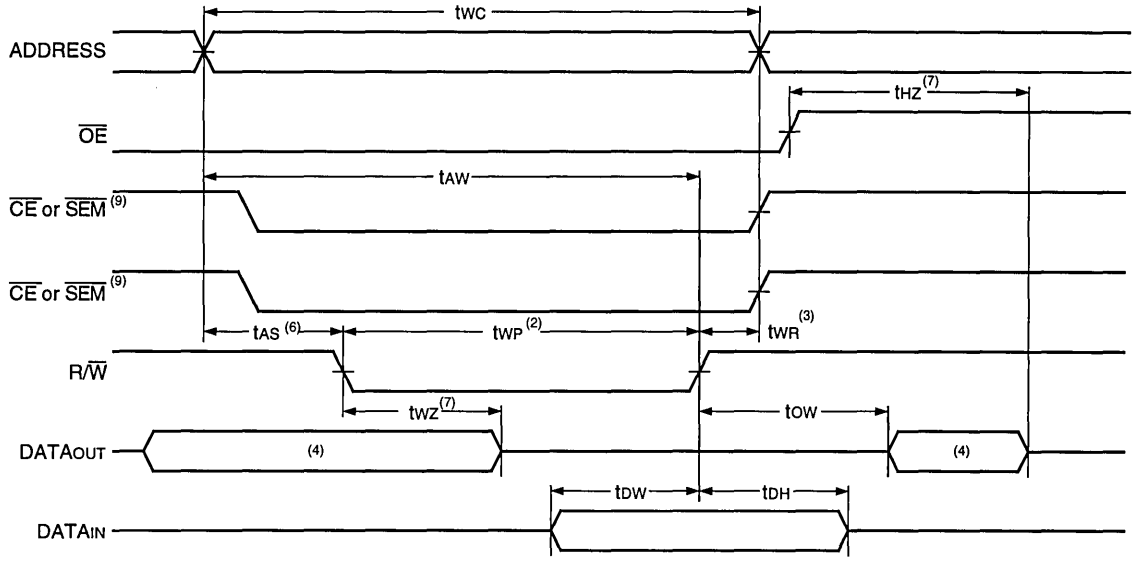
Symbol	Parameter	IDT70261X20 Min.	IDT70261X20 Max.	IDT70261X25 Min.	IDT70261X25 Max.	Unit
WRITE CYCLE						
tWC	Write Cycle Time	20	—	25	—	ns
tEW	Chip Enable to End-of-Write[3]	15	—	20	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	15	—	ns
tHZ	Output High-Z Time[1, 2]	—	12	—	15	ns
tDH	Data Hold Time[4]	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	12	—	15	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	ns

Symbol	Parameter	IDT70261X35 Min.	IDT70261X35 Max.	IDT70261X55 Min.	IDT70261X55 Max.	Unit
WRITE CYCLE						
tWC	Write Cycle Time	35	—	55	—	ns
tEW	Chip Enable to End-of-Write[3]	30	—	45	—	ns
tAW	Address Valid to End-of-Write	30	—	45	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	ns
tWP	Write Pulse Width	25	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	30	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	25	ns
tDH	Data Hold Time[4]	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	15	—	25	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	ns

NOTES: 3039 tbl 13

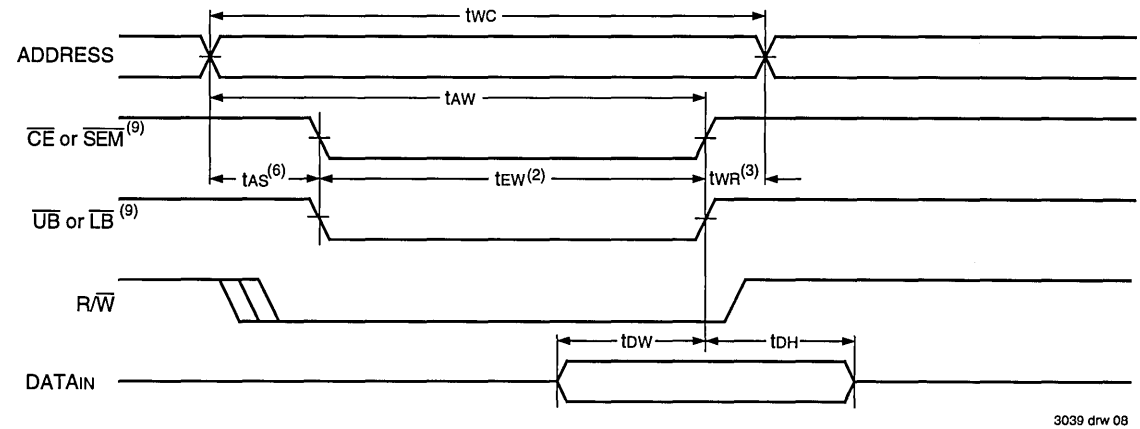
1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,5,8)



3039 drw 07

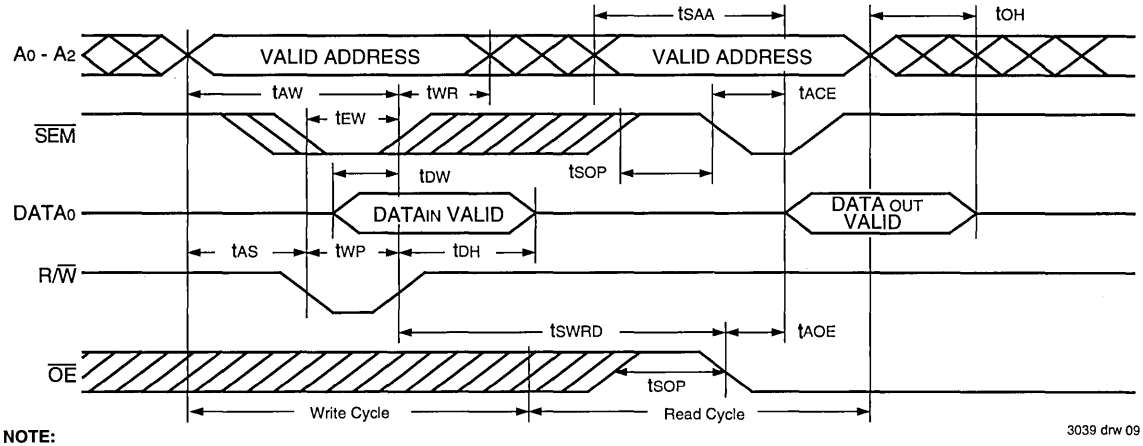
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING(1,5)



3039 drw 08

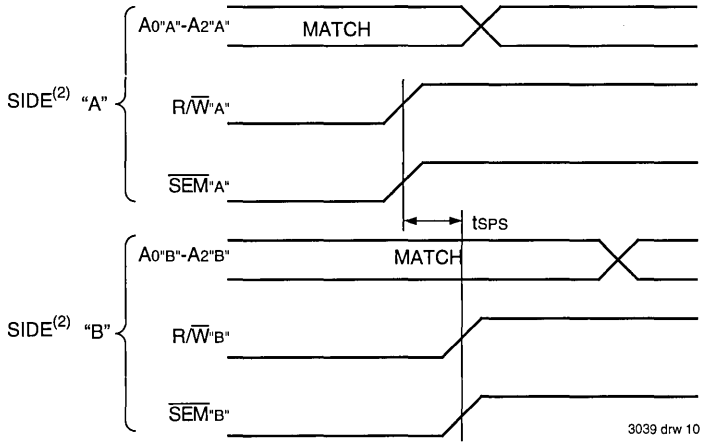
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ and $\overline{LB}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a LOW $\overline{CE}$ and a LOW R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured ± 200mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. tEW must be met for either condition.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH or $\overline{UB}$ and $\overline{LB}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}_R$ = $\overline{CE}_L$ = VIH, or both $\overline{UB}$ & $\overline{LB}$ = VIH.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}$"A" or $\overline{SEM}$"A" going HIGH to R/$\overline{W}$"B" or $\overline{SEM}$"B" going HIGH.
4. If tSPS is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	IDT70261X20 Min.	IDT70261X20 Max.	IDT70261X25 Min.	IDT70261X25 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)						
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	20	—	20	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	20	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	20	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	17	—	17	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	20	—	25	ns
BUSY TIMING (M/$\overline{S}$ = L)						
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	15	—	17	—	ns
PORT-TO-PORT DELAY TIMING						
tWDD	Write Pulse to Data Delay[1]	—	45	—	50	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	30	—	30	ns

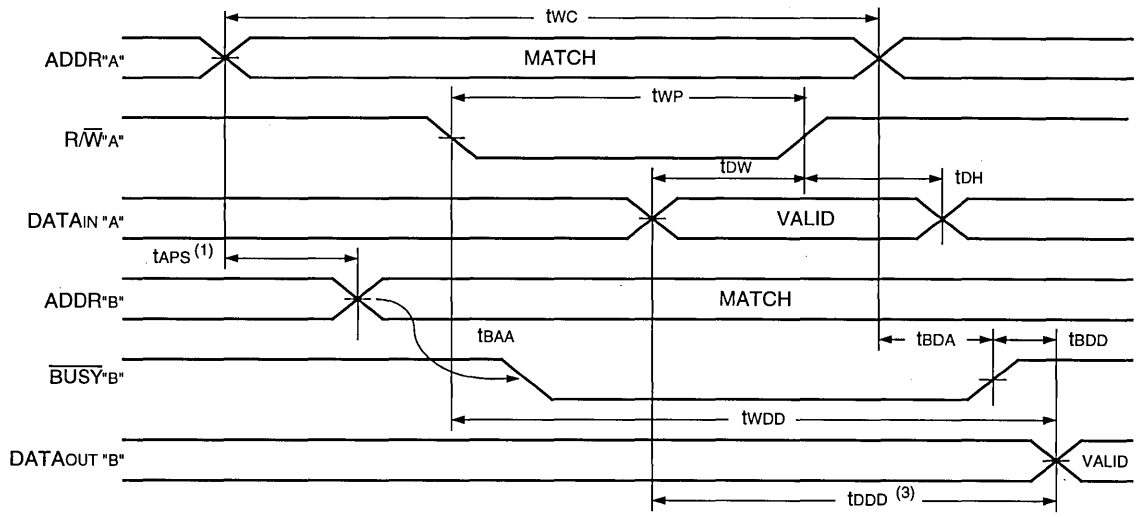
Symbol	Parameter	IDT70261X35 Min.	IDT70261X35 Max.	IDT70261X55 Min.	IDT70261X55 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)						
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	20	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	40	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	40	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	20	—	35	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	35	—	55	ns
BUSY TIMING (M/$\overline{S}$ = L)						
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING						
tWDD	Write Pulse to Data Delay[1]	—	60	—	80	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	35	—	55	ns

3039 tbl 14

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Wave form of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = VIH)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. "X" in part numbers indicates power rating (S or L).

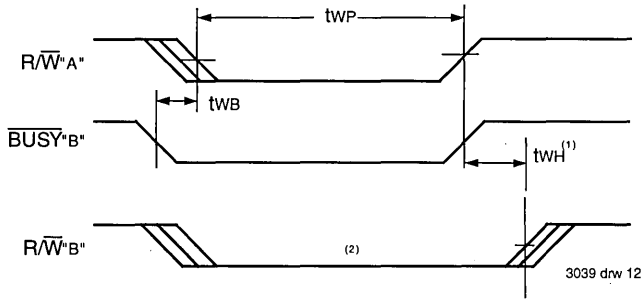
6

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$ (2,5) ($M/\overline{S}$ = VIH)



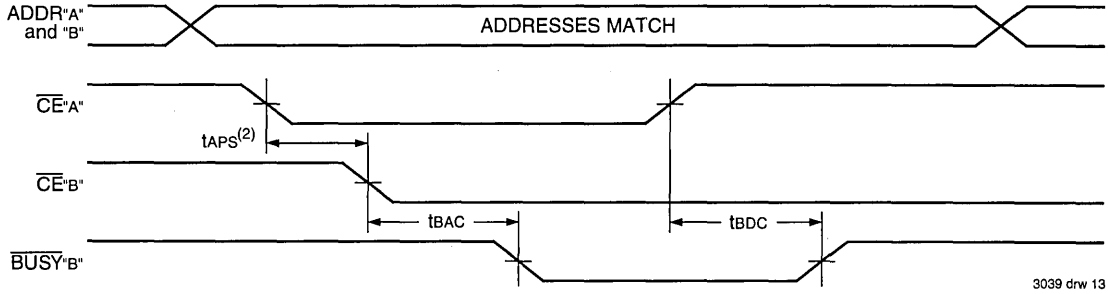
NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for $M/\overline{S}$ = VIL (SLAVE).
2. $\overline{CE}_L = \overline{CE}_R$ = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. If $M/\overline{S}$ = VIL (SLAVE), then $\overline{BUSY}$ is an input ($\overline{BUSY}$"A" = VIH and $\overline{BUSY}$"B" = "don't care", for this example).
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

TIMING WAVEFORM OF WRITE WITH BUSY ($M/\overline{S}$ = VIL)

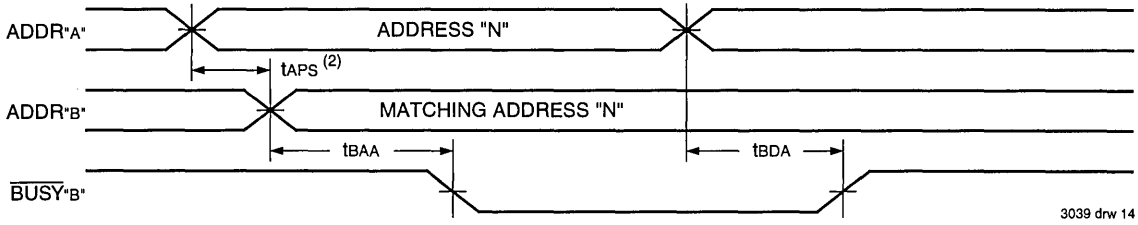


NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (SLAVE) and output (MASTER).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/W"B", until $\overline{BUSY}$"B" goes High.

WAVEFORM OF $\overline{BUSY}$ ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1) (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)(M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

6

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1)

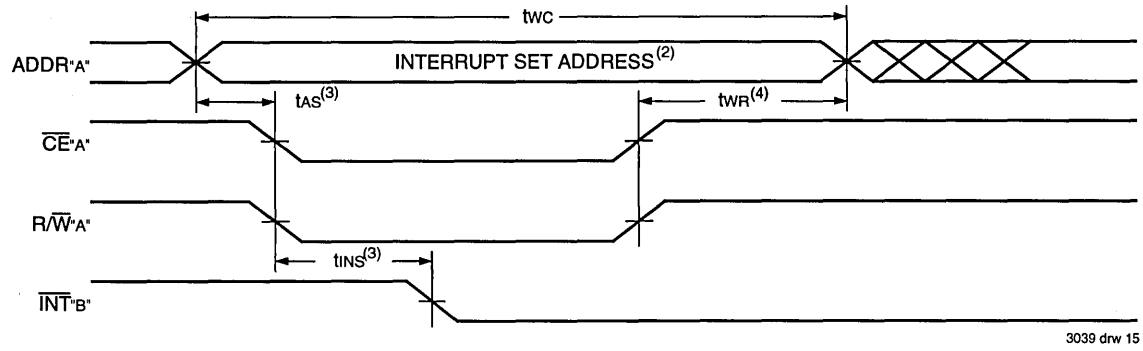
Symbol	Parameter	IDT7025X20 Min.	IDT7025X20 Max.	IDT7025X25 Min.	IDT7025X25 Max.	Unit
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	20	—	20	ns
tINR	Interrupt Reset Time	—	20	—	20	ns

Symbol	Parameter	IDT7025X35 Min.	IDT7025X35 Max.	IDT7025X55 Min.	IDT7025X55 Max.	Unit
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	40	ns
tINR	Interrupt Reset Time	—	25	—	40	ns

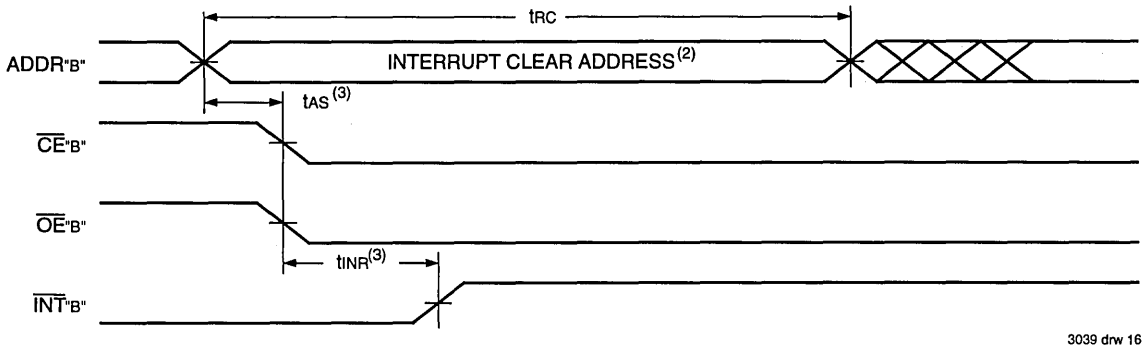
NOTE:
1. "X" in part numbers indicates power rating (S or L).

2683 tbl 14

WAVEFORM OF INTERRUPT TIMING(1)



3039 drw 15



3039 drw 16

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG(1)

Left Port					Right Port					
R/$\overline{W}$L	$\overline{CE}$L	$\overline{OE}$L	A13L-A0L	$\overline{INT}$L	R/$\overline{W}$R	$\overline{CE}$R	$\overline{OE}$R	A13R-A0R	$\overline{INT}$R	Function
L	L	X	3FFF	X	X	X	X	X	L(2)	Set Right $\overline{INT}$R Flag
X	X	X	X	X	X	L	L	3FFF	H(3)	Reset Right $\overline{INT}$R Flag
X	X	X	X	L(3)	L	L	X	3FFE	X	Set Left $\overline{INT}$L Flag
X	L	L	3FFE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}$L Flag

2683 tbl 16

NOTES:
1. Assumes $\overline{BUSY}$L = $\overline{BUSY}$R = VIH.
2. If $\overline{BUSY}$L = VIL, then no change.
3. If $\overline{BUSY}$R = VIL, then no change.

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{13L} A_{0R}-A_{13R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

NOTES: 2683 tbl 17

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$ outputs on the IDT70261 are push-pull, not open drain outputs. On slaves the $\overline{BUSY}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_{15} Left	D_0 - D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2683 tbl 18

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70261.

FUNCTIONAL DESCRIPTION

The IDT70261 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70261 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ HIGH). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 3FFE (HEX), where a write is defined as $\overline{CE} = R/\overline{W} = V_{IL}$ per the Truth Table. The left port clears the interrupt through access of address location 3FFE when $\overline{CE}_R = \overline{OE}_R = V_{IL}$, $R/\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 3FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 3FFF. The message (16 bits) at 3FFE or 3FFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FFE and 3FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not

desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 70261 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT70261 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT70261 RAM the busy pin

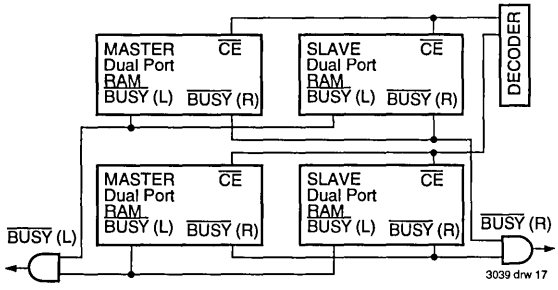


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70261 RAMs.

is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT70261 is an extremely fast Dual-Port 16K x 16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT70261 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70261's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70261 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that

semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70261 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into

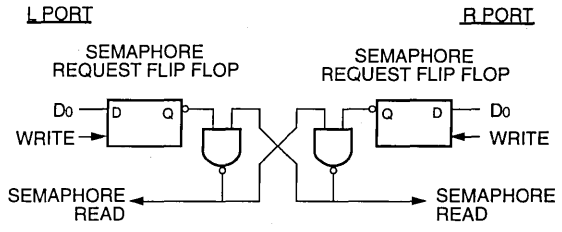


Figure 4. IDT70261 Semaphore Logic

the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT70261's Dual-Port RAM. Say the 16K x 16 RAM was to be divided into two 8K

x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 8K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of Dual-Port RAM with each other.

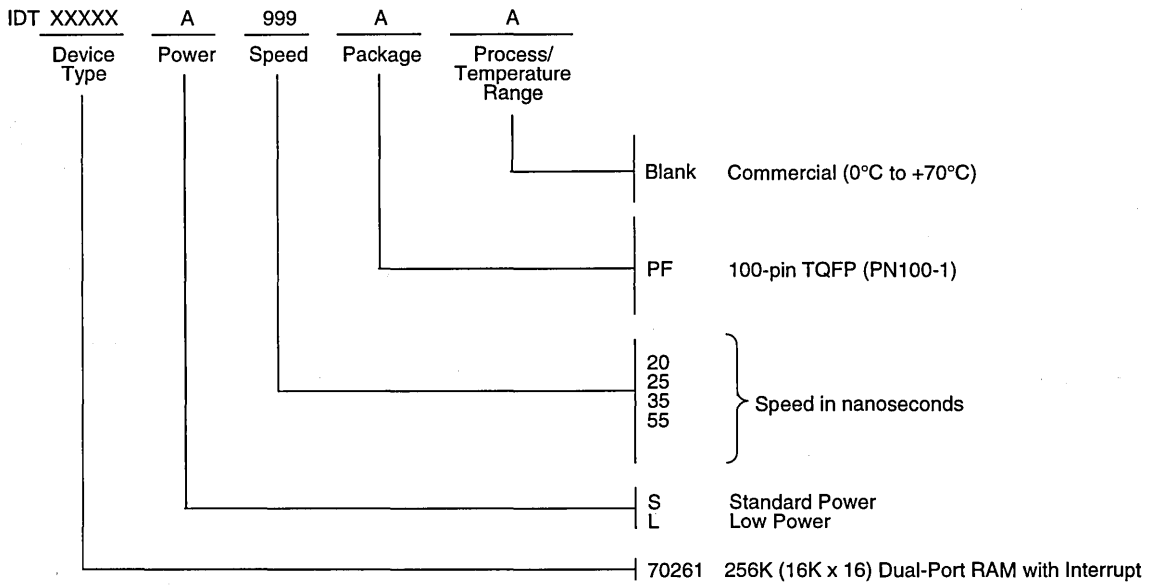
The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

ORDERING INFORMATION



3039 drw 19

Integrated Device Technology, Inc.

HIGH-SPEED 32K x 16 DUAL-PORT STATIC RAM

ADVANCED IDT7027S/L

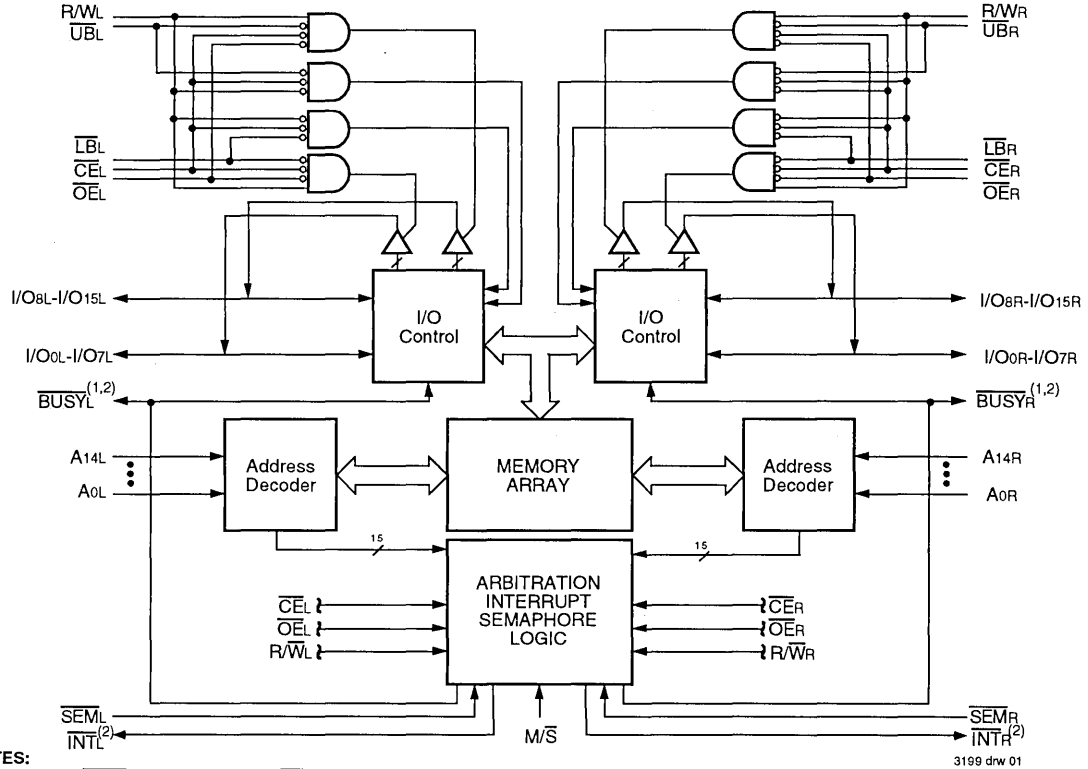
FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Military: 35/55ns (max.)
  - — Commercial: 25/35/55ns (max.)
- Low-power operation
  - — IDT7027S
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - — IDT7027L
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT7027 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master,
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- TTL-compatible, single 5V (±10%) power supply
  Available in an 108-pin PGA and a 100-pin Thin Quad Plastic Flatpack TQFP
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7027 is a high-speed 32K x 16 Dual-Port Static RAM. The IDT7027 is designed to be used as a stand-alone 512K-bit Dual-Port RAM or as a combination MASTER/SLAVE

FUNCTIONAL BLOCK DIAGRAM



NOTES:

1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ and $\overline{INT}$ outputs are non-tri-stated push-pull.

Dual-Port RAM for 32-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power.

The IDT7027 is packaged in a 100-pin TQFP and a 108-pin PGA. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Clas B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

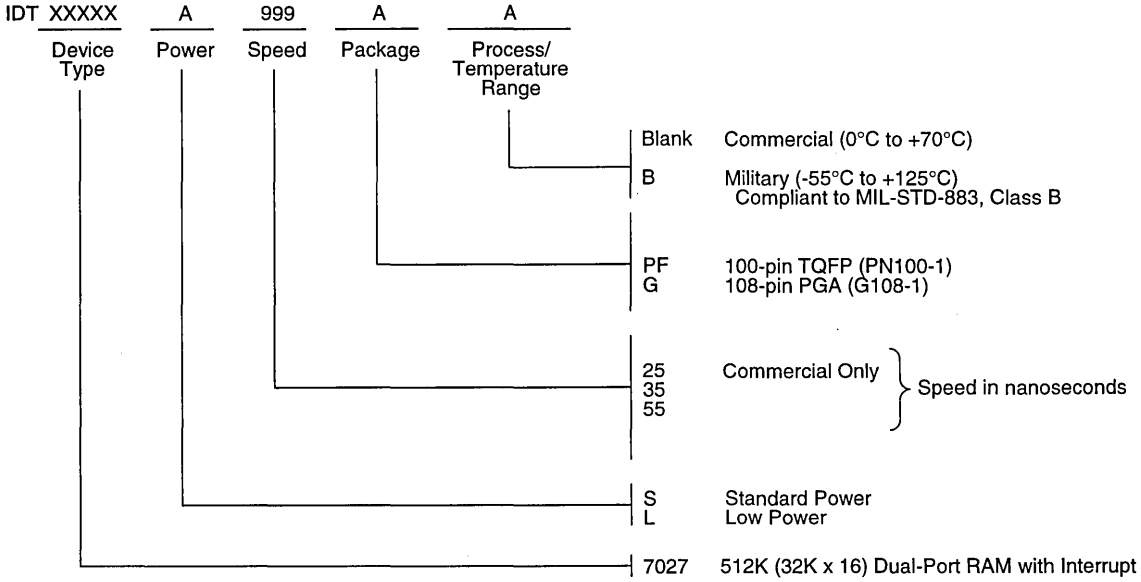
PIN NAMES (1,2)

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{13L}$	$A_{0R} - A_{13R}$	Address
$I/O_{0L} - I/O_{15L}$	$I/O_{0R} - I/O_{15R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

3199 tbl 01

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

ORDERING INFORMATION



3199 drw 19

Integrated Device Technology, Inc.

HIGH-SPEED 36K (4K x 9-BIT) SYNCHRONOUS DUAL-PORT RAM

IDT7099S

FEATURES:

- High-speed clock-to-data output times
  - — Military: 20/25/30ns (max.)
  - — Commercial: 15/20/25ns (max.)
- Low-power operation
  - — IDT7099S
    Active: 900 mW (typ.)
    Standby: 50 mW (typ.)
- 4K X 9 bits
- Architecture based on Dual-Port RAM cells
  - — Allows full simultaneous access from both ports
  - — Independent bit/byte Read and Write inputs for control functions
- Synchronous operation
  - — 4ns setup to clock, 1ns hold on all control, data, and address inputs
  - — Data input, address, and control registers
  - — Fast 15ns clock to data out
  - — Self-timed write allows fast write cycle
  - — 20ns cycle times, 50MHz operation
- Clock enable feature
- Guaranteed data output hold times
- Available in 68-pin PGA, PLCC, and 80-pin TQFP
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

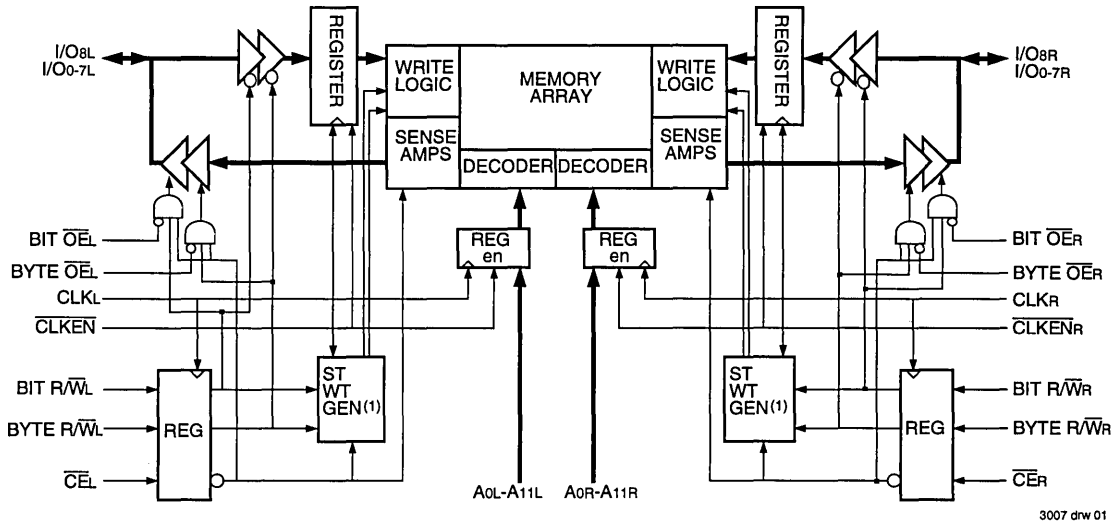
The IDT7099 is a high-speed 4K x 9 bit synchronous Dual-Port RAM. The memory array is based on Dual-Port memory cells to allow simultaneous access from both ports. Registers on control, data, and address inputs provide low set-up and hold times. The timing latitude provided by this approach allow systems to be designed with very short realized cycle times. With an input data register, thjs device has been optimized for applications having unidirectional data flow or bi-directional data flow in bursts. Changing data direction from reading to writing normally requires one dead cycle.

Fabricated using IDT's BiCMOS high-performance technology, these Dual-Ports typically operate on only 900mW of power at maximum high-speed clock-to-data output times as fast as 15ns. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT7099 is packaged in a 68-pin PGA, 68-pin PLCC, and a 80-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

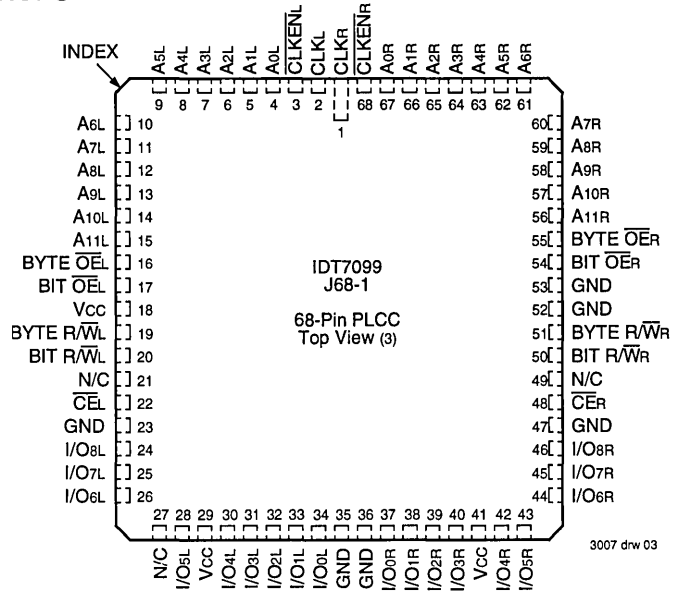
6

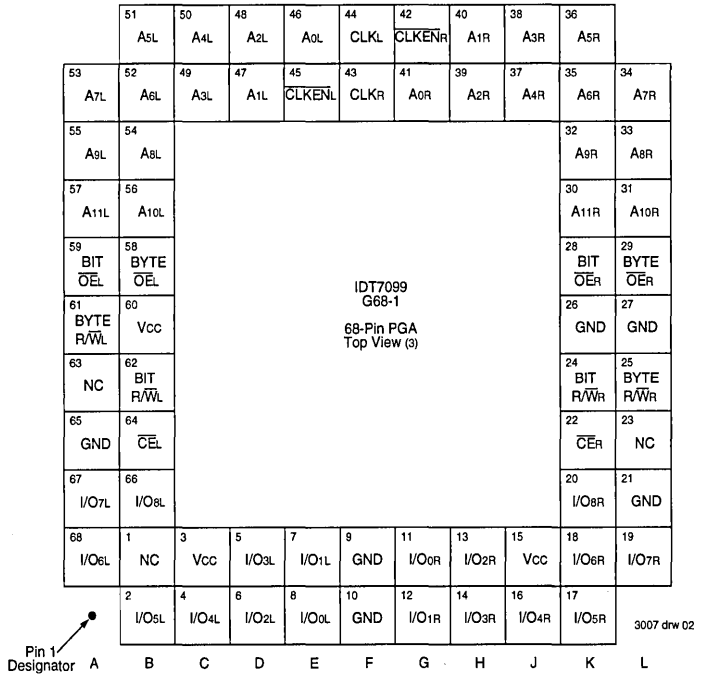
FUNCTIONAL BLOCK DIAGRAM



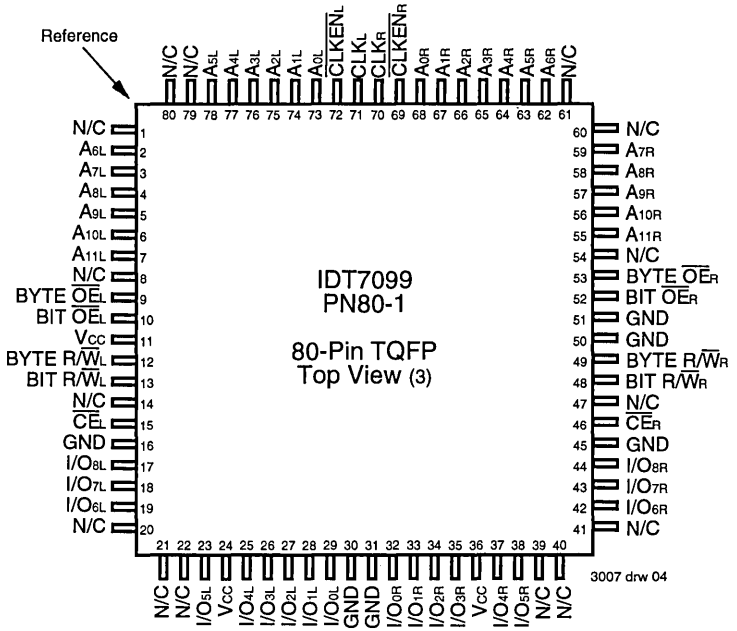
NOTE:
1. Self-timed write generator.

PIN CONFIGURATIONS





NOTES:
1. All VCC pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.



NOTES:
1. All VCC pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. This text does not indicate the orientaion of the actual part-marking.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
VTERM(3)	Terminal Voltage	–0.5 to VCC	–0.5 to VCC	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

3007 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

3007 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0 (2)	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

3007 tbl 03

NOTE:
1. VIL ≥ -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 0.5V.

CAPACITANCE (TA = +25°C, F = 1.0MHz) TQFP ONLY

Symbol	Parameter(1)	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	9	pF
COUT	Output Capacitance	VOUT = 3dV	10	pF

3007 tbl 04

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT7099S Min.	IDT7099S Max.	Unit
$\|I_{LI}\|$	Input Leakage Current [1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, VOUT = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OL} = –4mA	2.4	—	V

3007 tbl 05

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4] (V_{CC} = 5V ± 10%)

				IDT7099S15		IDT7099S20		IDT7099S25		IDT7099S30		
				Com'l Only						Mil Only		
Symbol	Parameter	Test Conditions	Version	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL} Outputs Open f = f_{MAX}[1]	Mil.	—	—	170	310	160	290	160	270	mA
			Com'l.	180	300	170	290	160	270	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} f = f_{MAX}[1]	Mil.	—	—	85	140	80	130	80	110	mA
			Com'l.	90	140	85	130	80	110	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_{A'}$ = V_{IL} and $\overline{CE}_{B'}$ = V_{IH} [3] Active Port Outputs Open, f = f_{MAX}[1]	Mil.	—	—	150	210	140	200	140	180	mA
			Com'l.	160	210	150	200	140	180	—	—	
I_{SB3}	Full Standby Current (Both Ports—CMOS Level Inputs)	Both Ports $\overline{CE}_R$ and $\overline{CE}_L$ ≥ V_{CC} – 0.2V V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0[2]	Mil.	—	—	10	20	10	20	10	20	mA
			Com'l.	10	15	10	—	10	—	—		
I_{SB4}	Full Standby Current (One Port—CMOS Level Inputs)	$\overline{CE}_{A'}$≤0.2V and $\overline{CE}_{B'}$ ≥ V_{CC} -0.2V[3], V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[1]	Mil.	—	—	145	200	135	190	135	170	mA
			Com'l.	155	200	145	190	135	170	—	—	

3007 tbl 06

NOTES:
1. At f = fmax, address and control lines (except Output Enable) are cycleing at the maximum frequency clock cycle of the 1/tCLK, using "AC TEST CONDITIONS" of input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{CC} = 5V, TA = 25°C for Typ, and are not production tested. $I_{CC\,DC}$ = 150mA (Typ).

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2, and 3

3007 tbl 07

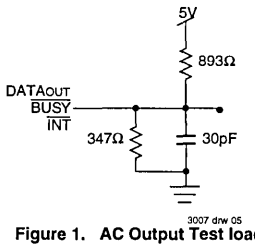


Figure 1. AC Output Test load.

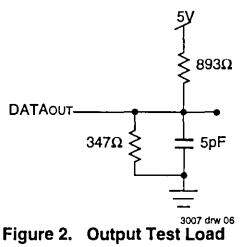


Figure 2. Output Test Load (For tCLZ, tCHZ, tOLZ, and tOHZ). Including scope and jig.

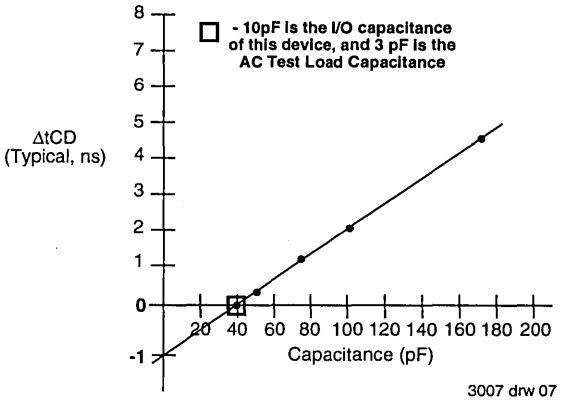


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGE — (READ AND WRITE CYCLE TIMING)

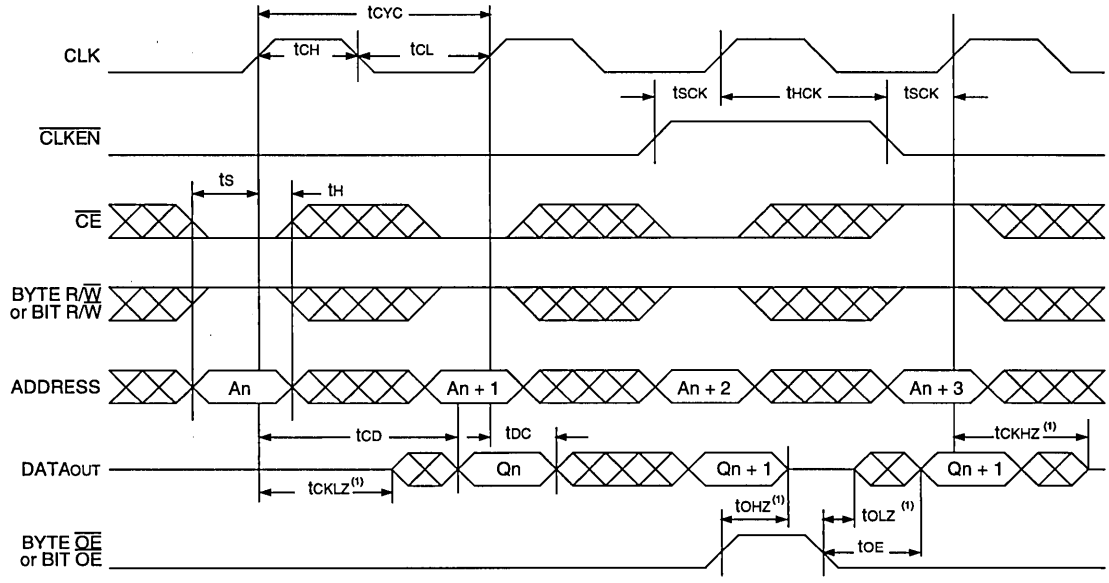
(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

		Commercial						Military						
		7099S15		7099S20		7099S25		7099S20		7099S25		7099S30		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tCYC	Clock Cycle Time	20	—	20	—	25	—	20	—	25	—	30	—	ns
tCH	Clock High Time	6	—	8	—	10	—	8	—	10	—	12	—	ns
tCL	Clock Low Time	6	—	8	—	10	—	8	—	10	—	12	—	ns
tCD	Clock High to Output Valid	—	15	—	20	—	25	—	20	—	25	—	30	ns
tS	Registered Signal Set-up Time	4	—	5	—	6	—	5	—	6	—	7	—	ns
tH	Registered Signal Hold Time	1	—	1	—	1	—	2	—	2	—	2	—	ns
tDC	Data Output Hold After Clock High	3	—	3	—	3	—	3	—	3	—	3	—	ns
tCKLZ	Clock High to Output Low-Z[1,2]	2	—	2	—	2	—	2	—	2	—	2	—	ns
tCKHZ	Clock High to Output High-Z[1,2]	—	7	—	9	—	12	—	9	—	12	—	15	ns
tOE	Output Enable to Output Valid	—	8	—	10	—	12	—	10	—	12	—	15	ns
tOLZ	Output Enable to Output Low-Z[1,2]	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOHZ	Output Disable to Output High-Z[1,2]	—	7	—	9	—	11	—	9	—	11	—	14	ns
tSCK	Clock Enable, Disable Set-up Time	4	—	5	—	6	—	5	—	6	—	7	—	ns
tHCK	Clock Enable, Disable Hold Time	2	—	2	—	2	—	3	—	3	—	3	—	ns
Port-to-Port Delay														
tCWDD	Write Port Clock High to Read Data Delay	—	30	—	35	—	45	—	35	—	45	—	55	ns

3007 tbl 08

NOTES:
1. Transition is measured +/-200mV from Low or High impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.

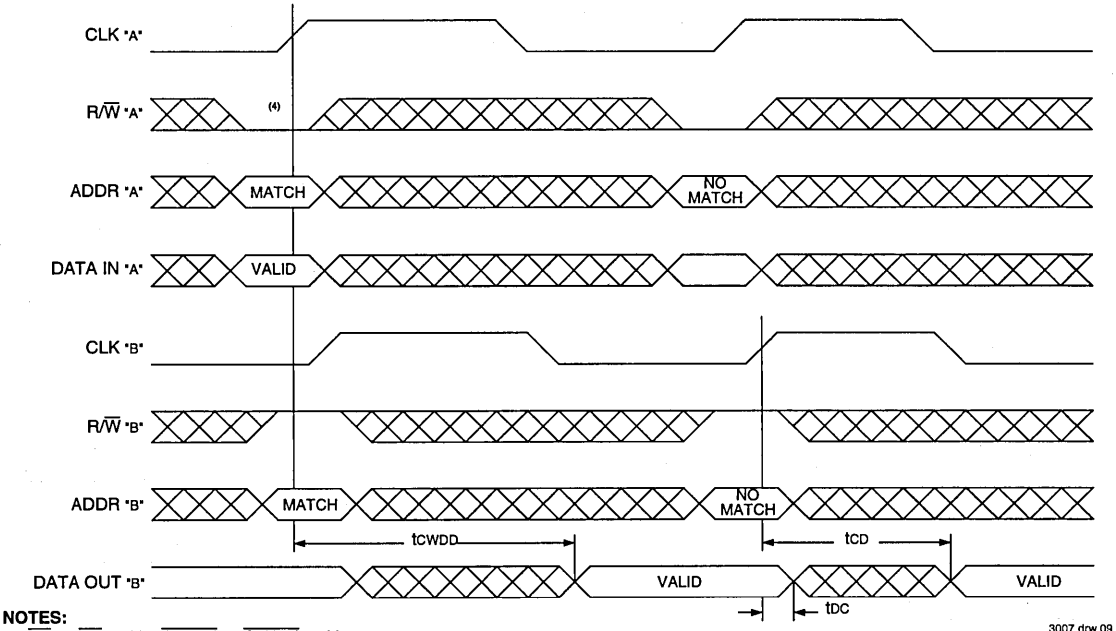
TIMING WAVEFORM OF READ CYCLE, EITHER SIDE



NOTES:
1. Transition is measured +/-200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).

3007 drw 08

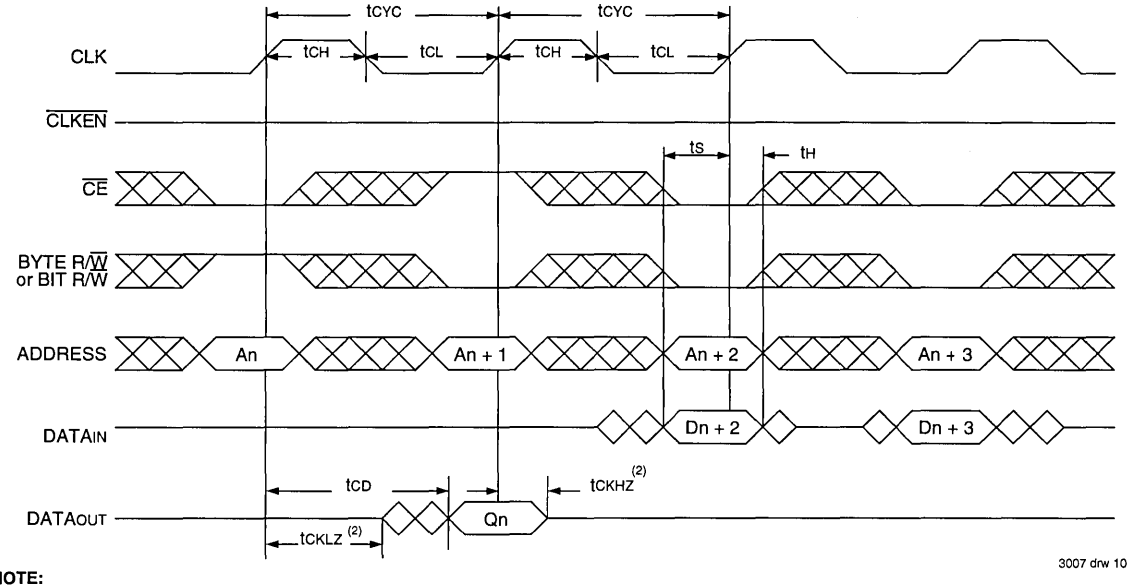
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ (1,2,3)



NOTES:
1. $\overline{CEL} = \overline{CER} = V_{IL}$, $\overline{CLKEN}_L = \overline{CLKEN}_R = V_{IL}$
2. $\overline{OE} = V_{IL}$ for the reading port, port 'B'.
3. All timing is the same for left and right ports. Ports "A" may be either the left or right port. Port "B" is opposite from port "A".
4. $R/\overline{W}_{A'}$ was active (V_{IL}) during the previous $CLK_{A'}$, when enabled the write path.

3007 drw 09

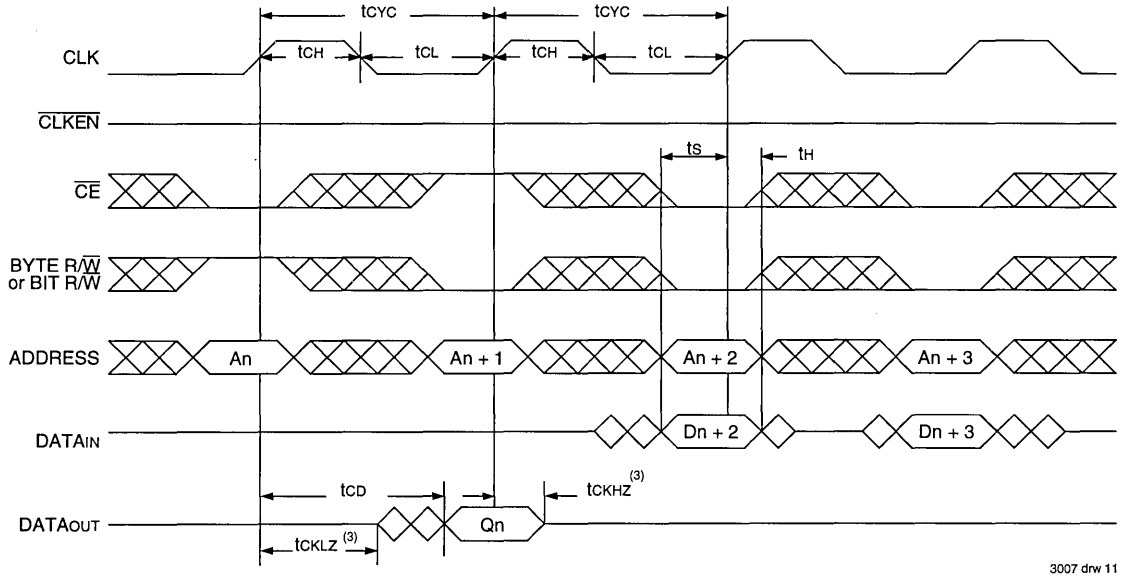
TIMING WAVEFORM OF READ-TO-WRITE CYCLE NO. 1, $\overline{CE}$ = VIH (1)



3007 drw 10

NOTE:
1. $\overline{OE}$ low throughout.
2. Transition is measured +/-200mV from Low or High impedance voltage with the Output Test Load (Figure 2).

TIMING WAVEFORM OF READ-TO-WRITE CYCLE NO. 2, $\overline{CE}$ = VIL(2)



3007 drw 11

NOTES:
1. During dead cycle, if $\overline{CE}$ = VIL, then invalid data will be written into array. The An+1 is rewritten on the following cycle.
2. $\overline{OE}$ low throughout.
3. Transition is measured +/-200mV from Low or High impedance voltage with the Output Test Load (Figure 2).

6

FUNCTIONAL DESCRIPTION

The IDT7099 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide very short set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. An asynchronous output enable is provided to ease asynchronous bus interfacing.

The internal write pulse width is independent of the high and low periods of the clock. This allows the shortest possible realized cycle times. Clock enable inputs are provided to stall the operation of the address and data input registers without introducing clock skew for very fast interleaved memory applications.

The data inputs are gated to control on-chip noise in bussed applications. The user must guarantee that the BYTE R/$\overline{W}$ and BIT R/$\overline{W}$ pins are low for at least one clock cycle before any write is attempted. A high on the $\overline{CE}$ input for one clock cycle will power down the internal circuitry to reduce static power consumption.

The device has separate bit write, byte write, bit enable, and byte enable pins to allow for independent control.

TRUTH TABLE I: READ/WRITE CONTROL(1)

Inputs						Outputs		
Synchronous				Asynchronous				
CLK	$\overline{CE}$	Byte R/$\overline{W}$	Bit R/$\overline{W}$	Byte $\overline{OE}$	Bit $\overline{OE}$	I/O0-7	I/O8	Mode
↑	h	h	h	X	X	High-Z	High-Z	Deselected, Power Down, Data I/O Disabled
↑	h	l	h	X	X	DATAIN	High-Z	Deselected, Power Down, Byte Data Input Enabled
↑	h	h	l	X	X	High-Z	DATAIN	Deselected, Power Down, Bit Data Input Enabled
↑	h	l	l	X	X	DATAIN	DATAIN	Deselected, Power Down, Data Input Enabled
↑	l	l	h	X	L	DATAIN	DATAOUT	Write Byte, Read Bit
↑	l	l	h	X	H	DATAIN	High-Z	Write Byte Only
↑	l	h	l	L	X	DATAOUT	DATAIN	Read Byte, Write Bit
↑	l	h	l	H	X	High-Z	DATAIN	Write Bit Only
↑	l	l	l	X	X	DATAIN	DATAIN	Write Byte, Write Bit
↑	l	h	h	L	L	DATAOUT	DATAOUT	Read Byte, Read Bit
↑	l	h	h	H	L	High-Z	DATAOUT	Read Bit Only
↑	l	h	h	L	H	DATAOUT	High-Z	Read Byte Only
↑	l	h	h	H	H	High-Z	High-Z	Data I/O Disabled

3007 tbl 09

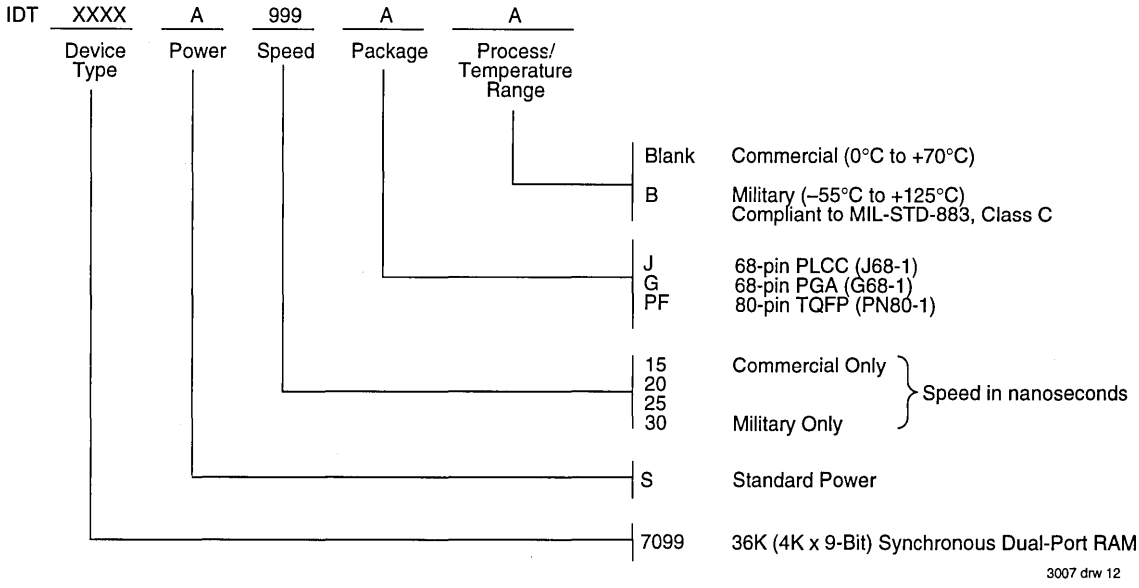
TRUTH TABLE II: CLOCK ENABLE FUNCTION TABLE(1)

	Inputs		Register Inputs		Register Outputs	
Operating Mode	CLK	$\overline{CLKEN}$(2)	ADDR	DATAIN	ADDR	DATAOUT
Load "1"	↑	l	h	h	H	H
Load "0"	↑	l	l	l	L	L
Hold (do nothing)	↑	h	X	X	NC	NC
	X	H	X	X	NC	NC

NOTE: 3007 tbl 10

1. 'H' = High voltage level steady state, 'h' = High voltage level one set-up time prior to the low-to-high clock transition, 'L' = Low voltage level steady state 'l' = Low voltage level one set-up time prior to the Low-to-High clock transition, 'X' = Don't care, 'NC' = No change
2. $\overline{CLKEN}$ = VIL must be clocked in during Power-Up.

ORDERING INFORMATION



3007 drw 12

6

Integrated Device Technology, Inc.

HIGH-SPEED 512K (64K x 8) SYNCHRONOUS DUAL-PORT RAM

ADVANCED
IDT70908S/L

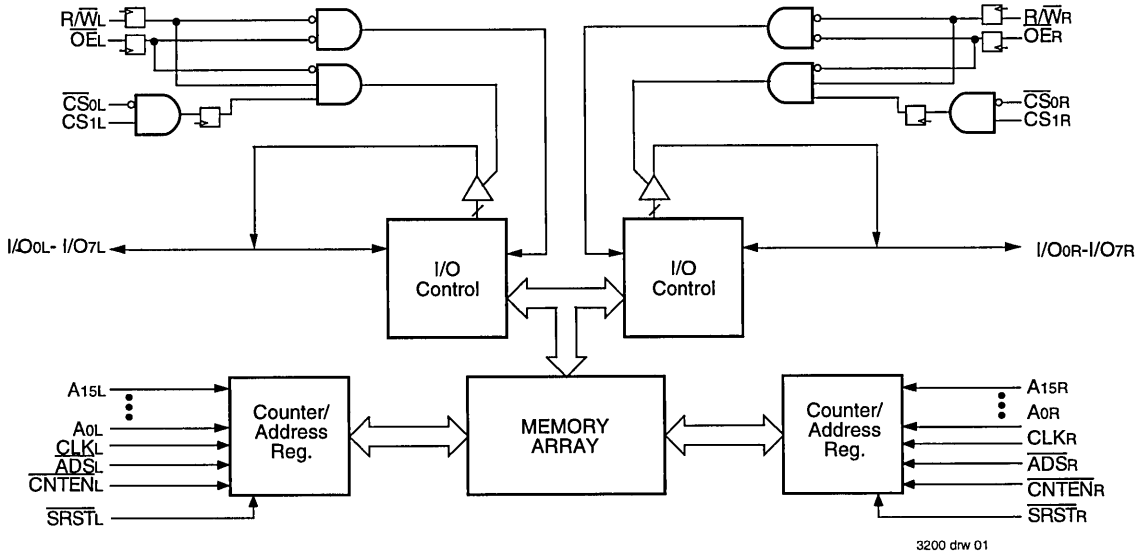
FEATURES:

- High-speed clock-to-data output times
  - — Military: 35/55ns (max.)
  - — Commercial: 25/35/55ns (max.)
- Low-power operation
  - — IDT70908S
    Active: 900mW (typ.)
    Standby: 5mW (typ.)
  - — IDT70908L
    Active: 900mW (typ.)
    Standby: 1mW (typ.)
- 64K X 8 bits Synchronous Operation
- Architecture based on Dual-Port RAM cells
  - — Allows full simultaneous access from both ports
- Synchronous operation
  - — Data input, address, and control registers
  - — Fast 25ns clock to data out
  - — Self-timed write allows fast write cycle
  - — 30ns cycle times, 33MHz operation
- On-Chip counter provides burst capability for any size burst or direct address access controlled by $\overline{ADS}$
- This part is available in a Flow-Through mode, with a Pipe-lined version available soon
- Clock enable feature
- Chip Select Feature allows power savings by allowing control of the memory array's power usage
- Two Chip Select pins allows for either high or low activation of the memory array
- Guaranteed data output hold times
- Available in 84-pin PGA, PLCC, and 100-pin TQFP
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT70908 is a high-speed 64K x 8 bit synchronous Dual-Port RAM. The memory array is based on Dual-Port memory cells to allow simultaneous access from both ports. Registers on control, data, and address inputs provide low setup and hold times. The timing latitude provided by this approach allow systems to be designed with very short realized cycle times. With an input data register, this device has been optimized for applications having unidirectional data flow or bidirectional data flow in bursts.

FUNCTIONAL BLOCK DIAGRAM



Fabricated using IDT's CMOS high-performance technology, these Dual-Ports typically operate on only 900mW of power at maximum high-speed clock-to-data output times as fast as 25ns. An automatic power down feature, controlled by $\overline{CS}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

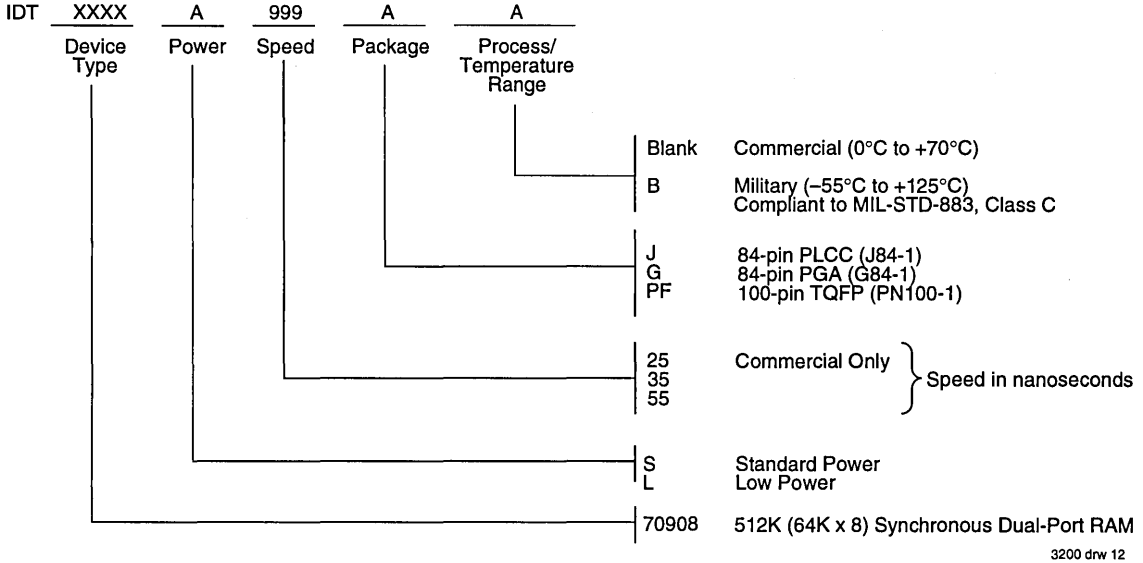
The IDT70908 is packaged in a 84-pin PGA, 84-pin PLCC, and a 100-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN NAMES AND FUNCTIONS

Left Port	Right Port	Names	Usage
A_{0L} — A_{15L}	A_{0R} — A_{15R}	Address	Separate Address and Data lines allow for parallel Address and Data use.
I/O_{0L} — I/O_{7L}	I/O_{0R} — I/O_{7R}	Data Input/Output	Data that is read and written via these lines.
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Contol	Clocked control for Reading and Writing to Memory.
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable	Internally disables output, removing Data from the Bus.
$\overline{CS}_{0L}$ CS_{1L}	$\overline{CS}_{0R}$ CS_{1R}	Chip Select	Selects or "powers up" the memory array. is active low and CS is active high. The unused pin should be tied to the active mode.
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Input Strobe	When Low, loads the current address into the register, used to access the array. When high, isolates the address bus from the register using the value in the register to access the array.
CLK_L	CLK_R	Clock	Clock or strobe for synchronous operation.
$\overline{SRST}_L$	$\overline{SRST}_R$	Counter Reset	Sets Counter=0 in the read mode, with CS active.
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Count Advance Enable	Synchronously advances the counter when active low.
Vcc		Power	Common Power.
GND		Ground	Common Ground.

6

ORDERING INFORMATION



3200 drw 12

Integrated Device Technology, Inc.

HIGH-SPEED 512K (32K x 16) SYNCHRONOUS DUAL-PORT RAM

ADVANCED IDT70927S/L

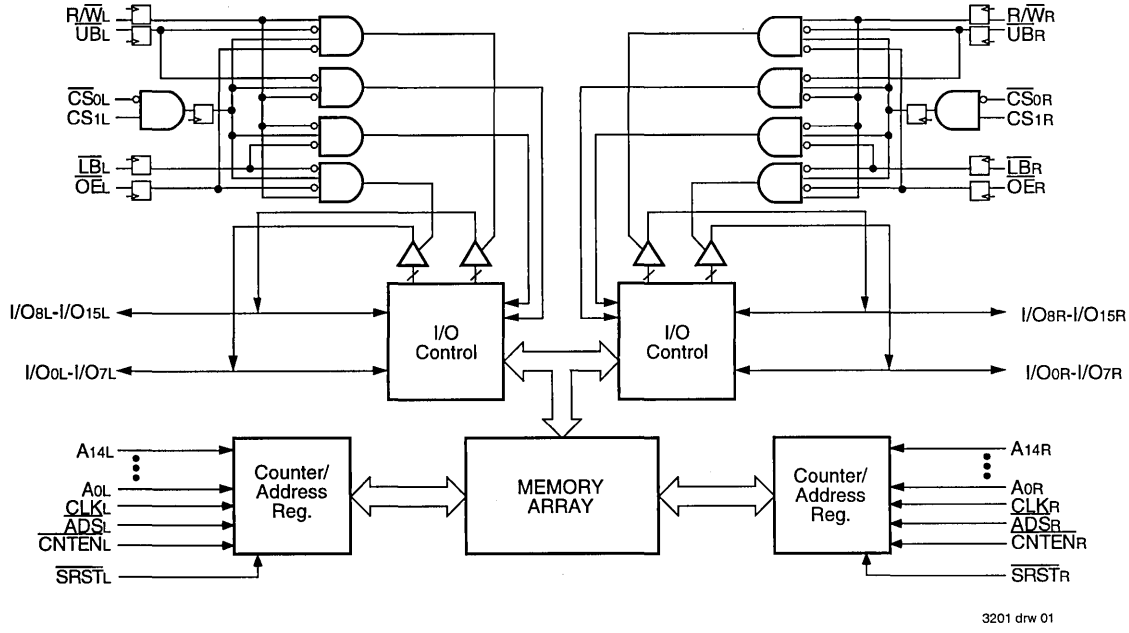
FEATURES:

- High-speed clock-to-data output times
  - — Military: 35/55ns (max.)
  - — Commercial: 25/35/55ns (max.)
- Low-power operation
  - — IDT70927S
    Active: 900mW (typ.)
    Standby: 5mW (typ.)
  - — IDT70927L
    Active: 900mW (typ.)
    Standby: 1mW (typ.)
- 32K X 16 bits Synchronous Operation
- Architecture based on Dual-Port RAM cells
  - — Allows full simultaneous access from both ports
- Synchronous operation
  - — Data input, address, and control registers
  - — Fast 25ns clock to data out
  - — Self-timed write allows fast write cycle
  - — 30ns cycle times, 33MHz operation
- On-Chip counter provides burst capability for any size burst or direct address access controlled by $\overline{ADS}$
- This part is available in a Flow-Through mode, with a Pipe-lined version available soon
- Upper and lower byte accessability
- Clock enable feature
- Chip Select Feature allows power savings by allowing control of the memory array's power usage
- Two Chip Select pins allows for either high or low activation of the memory array
- Guaranteed data output hold times
- Available in 108-pin PGA and 100-pin TQFP
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT70927 is a high-speed 32K x 16 bit synchronous Dual-Port RAM. The memory array is based on Dual-Port memory cells to allow simultaneous access from both ports. Registers on control, data, and address inputs provide low setup and hold times. The timing latitude provided by this approach allow systems to be designed with very short realized cycle times. With an input data register, this device has been optimized for applications having unidirectional data flow or bidirectional data flow in bursts.

FUNCTIONAL BLOCK DIAGRAM



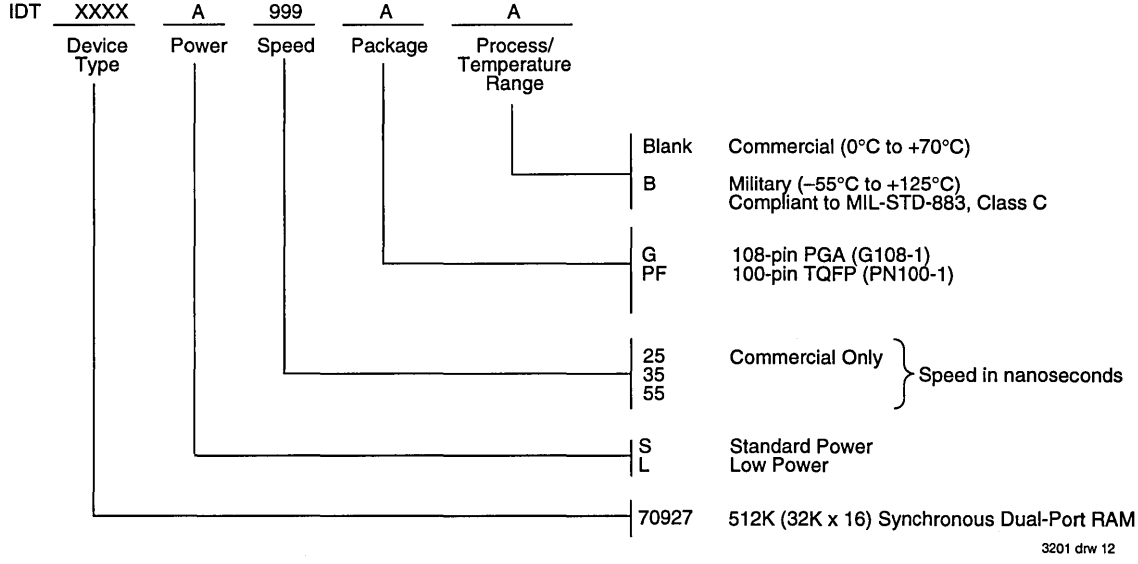
Fabricated using IDT's CMOS high-performance technology, these Dual-Ports typically operate on only 900mW of power at maximum high-speed clock-to-data output times as fast as 25ns. An automatic power down feature, controlled by $\overline{CS}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70927 is packaged in a 108-pin PGA and a 100-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN NAMES AND FUNCTIONS

Left Port	Right Port	Names	Usage
A_{0L} — A_{14L}	A_{0R} — A_{14R}	Address	Separate Address and Data lines allow for parallel Address and Data use.
I/O_{0L} — I/O_{15L}	I/O_{0R} — I/O_{15R}	Data Input/Output	Data that is read and written via these lines.
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Contol	Clocked control for Reading and Writing to Memory.
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable	Internally disables output, removing Data from the Bus.
$\overline{CS}_{0L}$ CS_{1L}	$\overline{CS}_{0R}$ CS_{1R}	Chip Select	Selects or "powers up" the memory array. is active low and CS is active high. The unused pin should be tied to the active mode.
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Input Strobe	When Low, loads the current address into the register, used to access the array. When high, isolates the address bus from the register using the value in the register to access the array.
CLK_L	CLK_R	Clock	Clock or strobe for synchronous operation.
$\overline{SRST}_L$	$\overline{SRST}_R$	Counter Reset	Sets Counter=0 in the read mode, with CS active.
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Count Advance Enable	Synchronously advances the counter when active low.
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select	Selects the high order byte at the given address.
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select	Selects the Low order byte at the given address.
Vcc		Power	Common Power.
GND		Ground	Common Ground.

ORDERING INFORMATION



3201 drw 12

Integrated Device Technology, Inc.

HIGH-SPEED 2K X 8 FOURPORT™ STATIC RAM

IDT7052S/L

FEATURES:

- High-speed access
  - — Military: 35/45ns (max.)
  - — Commercial: 25/35/45ns (max.)
- Low-power operation
  - — IDT7052S
    Active: 750mW (typ.)
    Standby: 10mW (typ.)
  - — IDT7052L
    Active: 750mW (typ.)
    Standby: 1.5mW (typ.)
- True Four-Port memory cells which allow simultaneous reads of the same memory locations
- Fully asynchronous operation from each of the four ports: P1, P2, P3, P4
- Versatile control for write-inhibit: separate $\overline{BUSY}$ input to control write-inhibit for each of the four ports
- Battery backup operation—2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in several popular hermetic and plastic packages for both through-hole and surface mount
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications

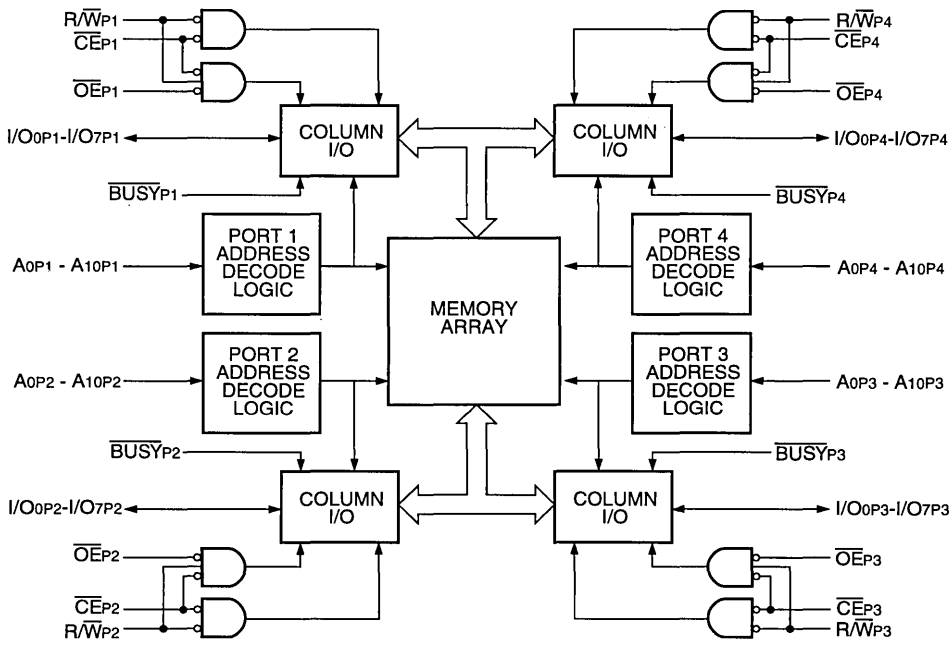
DESCRIPTION:

The IDT7052 is a high-speed 2K x 8 FourPort Static RAM designed to be used in systems where multiple access into a common RAM is required. This FourPort Static RAM offers increased system performance in multiprocessor systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

The IDT7052 is also designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when all ports simultaneously access the same FourPort RAM location.

The IDT7052 provides four independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location

FUNCTIONAL BLOCK DIAGRAM



2674 drw 01

from all ports. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using IDT's CMOS high-performance technology, this four port RAM typically operates on only 750mW of power. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 50µW from a 2V battery.

The IDT7052 is packaged in a ceramic 108-pin PGA, a plastic 132-pin quad flatpack, and a 120-pin thin quad flatpack. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS

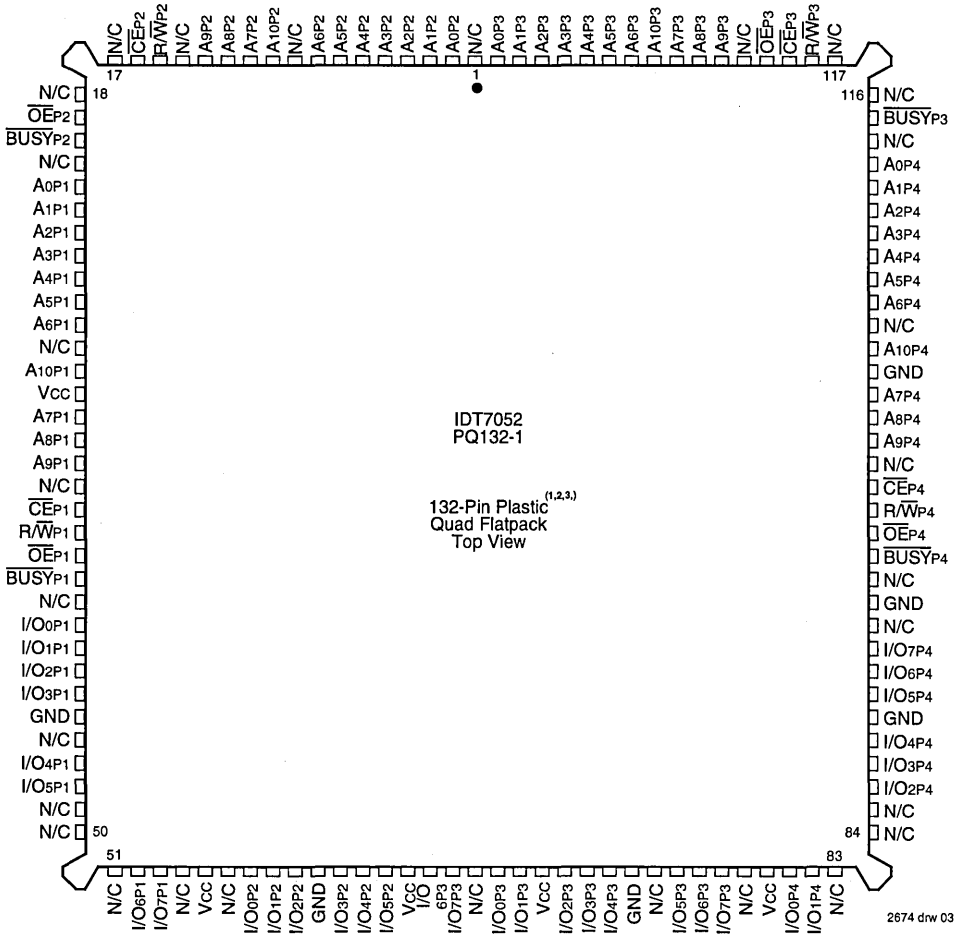
	A	B	C	D	E	F	G	H	J	K	L	M	
12	81 R/$\overline{W}$ P2	80 NC	77 A_7 P2	74 A_5 P2	72 A_3 P2	69 A_0 P2	68 A_0 P3	65 A_3 P3	63 A_5 P3	60 A_7 P3	57 NC	54 R/$\overline{W}$ P3	12
11	84 $\overline{BUSY}$ P2	83 $\overline{OE}$ P2	78 A_8 P2	76 A_{10} P2	73 A_4 P2	70 A_1 P2	67 A_1 P3	64 A_4 P3	61 A_{10} P3	59 A_8 P3	56 $\overline{OE}$ P3	53 $\overline{BUSY}$ P3	11
10	87 A_2 P1	86 A_1 P1	82 $\overline{CE}$ P2	79 A_9 P2	75 A_6 P2	71 A_2 P2	66 A_2 P3	62 A_6 P3	58 A_9 P3	55 $\overline{CE}$ P3	51 A_1 P4	50 A_2 P4	10
09	90 A_5 P1	88 A_3 P1	85 A_0 P1							52 A_0 P4	49 A_3 P4	47 A_5 P4	09
08	92 A_{10} P1	91 A_6 P1	89 A_4 P1							48 A_4 P4	46 A_6 P4	45 A_{10} P4	08
07	95 A_8 P1	94 A_7 P1	93 V_{CC}			IDT7052 G108-1				44 GND	43 A_7 P4	42 A_8 P4	07
06	96 A_9 P1	97 NC	98 $\overline{CE}$ P1			108-Pin PGA[1,2,3] Top View				39 $\overline{CE}$ P4	40 NC	41 A_9 P4	06
05	99 R/$\overline{W}$ P1	100 $\overline{OE}$ P1	102 I/O_0 P1							35 GND	37 $\overline{OE}$ P4	38 R/$\overline{W}$ P4	05
04	101 $\overline{BUSY}$ P1	103 I/O_1 P1	106 GND							31 GND	34 I/O_7 P4	36 $\overline{BUSY}$ P4	04
03	104 I/O_2 P1	105 I/O_3 P1	1 I/O_6 P1	4 V_{CC}	8 GND	12 V_{CC}	17 V_{CC}	21 GND	25 V_{CC}	28 I/O_2 P4	32 I/O_5 P4	33 I/O_6 P4	03
02	107 I/O_4 P1	2 I/O_7 P1	5 I/O_0 P2	7 I/O_2 P2	10 I/O_4 P2	13 I/O_6 P2	16 I/O_1 P3	19 I/O_3 P3	22 I/O_5 P3	24 I/O_7 P3	29 I/O_3 P4	30 I/O_4 P4	02
01	108 I/O_5 P1	3 NC	6 I/O_1 P2	9 I/O_3 P2	11 I/O_5 P2	14 I/O_7 P2	15 I/O_0 P3	18 I/O_2 P3	20 I/O_4 P3	23 I/O_6 P3	26 I/O_0 P4	27 I/O_1 P4	01

Index

2674 drw 02

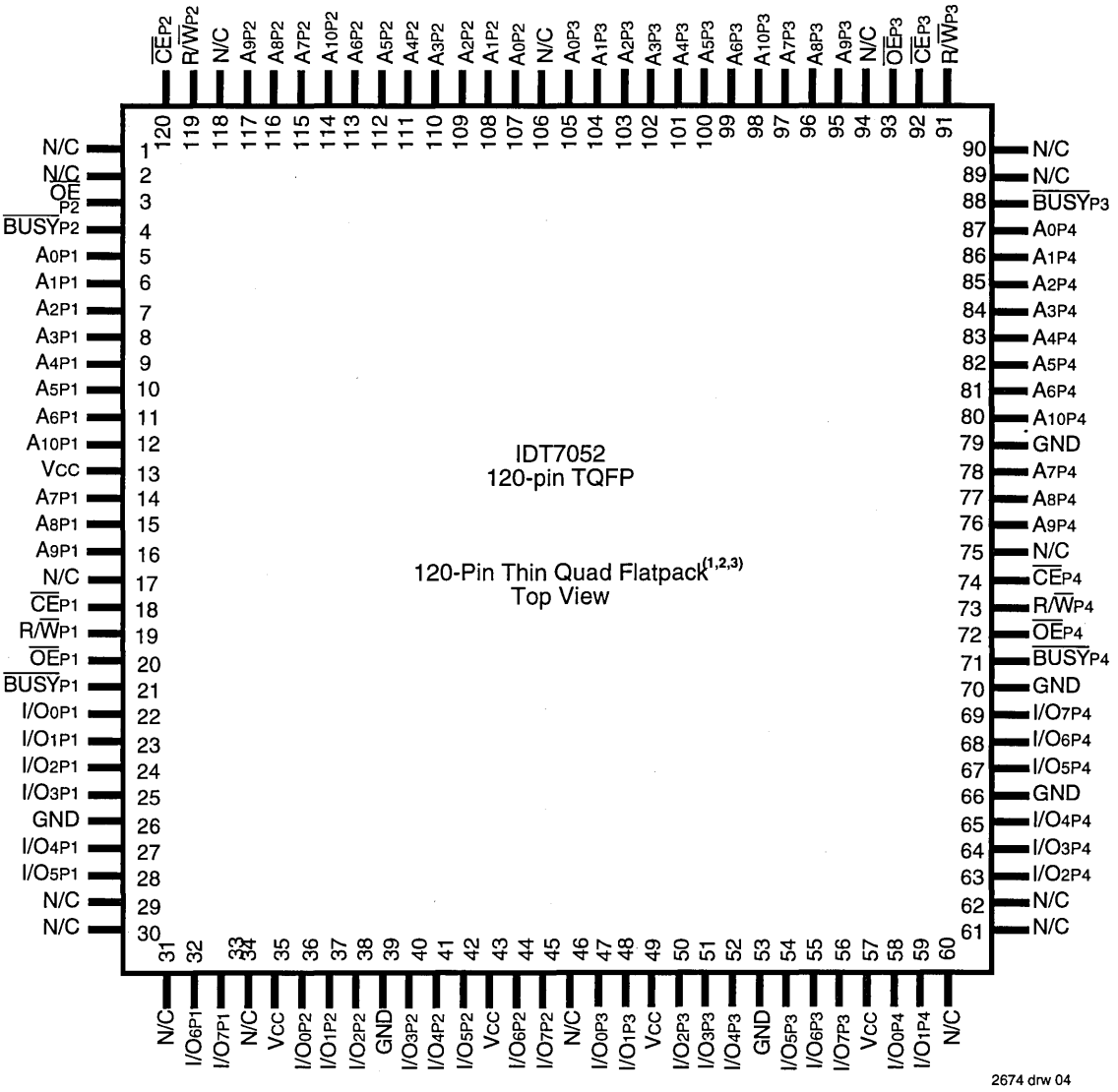
NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. This text does not indicate orientation of the actual part-marking.

PIN CONFIGURATIONS (CONT'D.)



NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. This text does not indicate orientation of the actual part-marking.

PIN CONFIGURATIONS (CONT'D.)



2674 drw 04

NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. This text does not indicate orientation of the actual part-marking.

PIN CONFIGURATIONS[1,2]

Symbol	Pin Name
A_0 P1 – A_{10} P1	Address Lines – Port 1
A_0 P2 – A_{10} P2	Address Lines – Port 2
A_0 P3 – A_{10} P3	Address Lines – Port 3
A_0 P4 – A_{10} P4	Address Lines – Port 4
I/O_0 P1 – I/O_7 P1	Data I/O – Port 1
I/O_0 P2 – I/O_7 P2	Data I/O – Port 2
I/O_0 P3 – I/O_7 P3	Data I/O – Port 3
I/O_0 P4 – I/O_7 P4	Data I/O – Port 4
$R/\overline{W}$ P1	Read/Write – Port 1
$R/\overline{W}$ P2	Read/Write – Port 2
$R/\overline{W}$ P3	Read/Write – Port 3
$R/\overline{W}$ P4	Read/Write – Port 4
GND	Ground
$\overline{CE}$ P1	Chip Enable – Port 1
$\overline{CE}$ P2	Chip Enable – Port 2
$\overline{CE}$ P3	Chip Enable – Port 3
$\overline{CE}$ P4	Chip Enable – Port 4
$\overline{OE}$ P1	Output Enable – Port 1
$\overline{OE}$ P2	Output Enable – Port 2
$\overline{OE}$ P3	Output Enable – Port 3
$\overline{OE}$ P4	Output Enable – Port 4
$\overline{BUSY}$ P1	Write Disable – Port 1
$\overline{BUSY}$ P2	Write Disable – Port 2
$\overline{BUSY}$ P3	Write Disable – Port 3
$\overline{BUSY}$ P4	Write Disable – Port 4
Vcc	Power

NOTES: 2674 tbl 01
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2674 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 0.5V.

CAPACITANCE (TQFP Package Only)

(T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE: 2674 tbl 03
1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and the output signals switch from 0V to 3V or from 3V to 0V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2674 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0[2]	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2674 tbl 05
1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT7052S		IDT7052L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

NOTES:
1. At Vcc≤2.0V input leakages are undefined.

2674 tbl 06

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1, 5] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Condition	Version		IDT7052X25 COM'L. ONLY		IDT7052X35		IDT7052X45		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC1}	Operating Power Supply Current (All Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open, f = 0[4]	MIL.	S	—	—	150	360	150	360	mA
				L	—	—	150	300	150	300	
			COM'L.	S	150	300	150	300	150	300	
				L	150	250	150	250	150	250	
I_{CC2}	Dynamic Operating Current (All Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[5]	MIL.	S	—	—	210	395	195	390	mA
				L	—	—	180	330	170	325	
			COM'L.	S	225	350	210	335	195	330	
				L	195	305	180	290	170	285	
I_{SB}	Standby Current (All Ports — TTL Level Inputs)	$\overline{CE}$ = V_{IH}, f = f_{MAX}[5]	MIL.	S	—	—	40	110	35	105	mA
				L	—	—	35	80	30	75	
			COM'L.	S	60	85	40	75	35	70	
				L	50	70	35	60	30	55	
I_{SB1}	Full Standby Current (All Ports — All CMOS Level Inputs)	All Ports, $\overline{CE}$ ≥ V_{CC} - 0.2V	MIL.	S	—	—	1.5	30	1.5	30	mA
				L	—	—	.3	4.5	.3	4.5	
		V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4]	COM'L.	S	1.5	15	1.5	15	1.5	15	
				L	.3	1.5	.3	1.5	.3	1.5	

NOTES:
1. "X" in part number indicates power rating (S or L).
2. V_{CC} = 5V, T_A = +25°C and are not production tested.
3. f = 0 means no address or control lines change.
4. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
5. For the case of one port, divide the appropriate current above by four.

2674 tbl 07

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

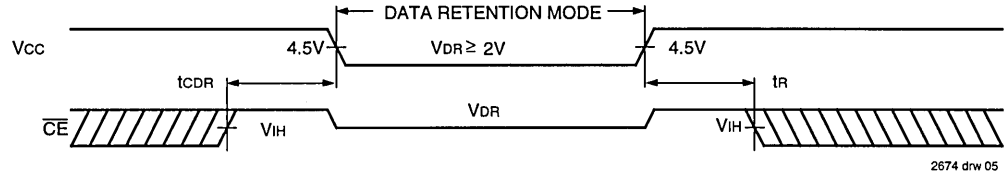
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	Vcc for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ ≥ V_{HC}	MIL.	—	25	1800	µA
		V_{IN} ≥ V_{HC} or ≤ V_{LC}	COM'L.	—	25	600	
t_{CDR}[3]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not production tested.

2674 tbl 08

LOW Vcc DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2674 tbl 09

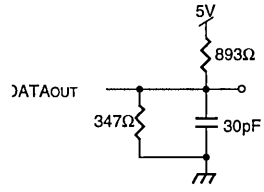


Figure 1. Output Test Load (for tLZ, tHZ, twz, tow)

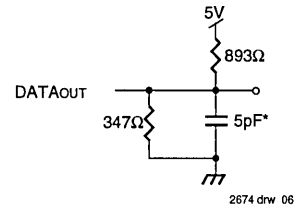


Figure 2. Output Test Load (for tLZ, tHZ, twz, tow)
*Including scope and jig

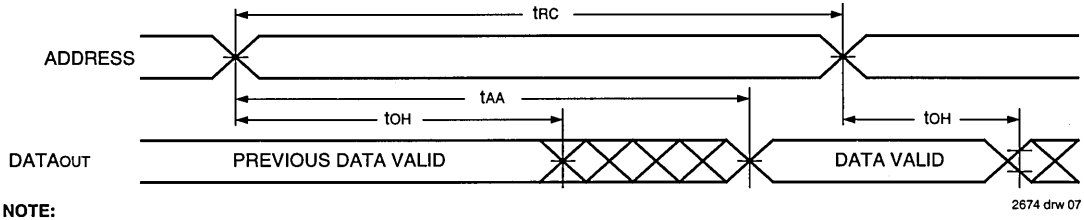
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE(3)

Symbol	Parameter	IDT7052X25 Commercial Min.	IDT7052X25 Commercial Max.	IDT7052X35 Min.	IDT7052X35 Max.	IDT7052X45 Min.	IDT7052X45 Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	25	—	35	—	45	—	ns
tAA	Address Access Time	—	25	—	35	—	45	ns
tACE	Chip Enable Access Time	—	25	—	35	—	45	ns
tAOE	Output Enable Access Time	—	15	—	25	—	30	ns
tOH	Output Hold from Address Change	0	—	0	—	0	—	ns
tLZ	Output Low-Z Time(1, 2)	5	—	5	—	5	—	ns
tHZ	Output High-Z Time(1, 2)	—	15	—	15	—	20	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	25	—	35	—	45	ns

2674 tbl 10

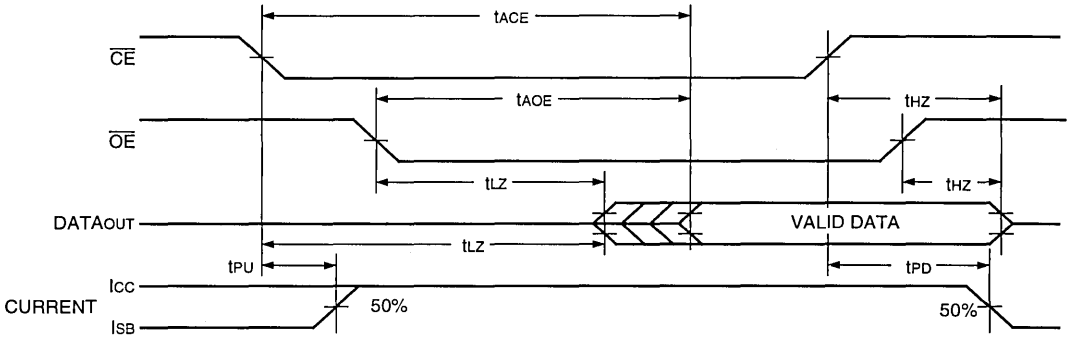
NOTES:
1. Transition is measured ±200mV from low or high impedance voltage with the Output Test Load (Figures 1 and 2).
2. This parameter is guaranteed but is not production tested.
3. "X" in part number indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, ANY PORT(1)



NOTE:
1. R/W = VIH, OE = VIL, and CC = VIL.

TIMING WAVEFORM OF READ CYCLE NO. 2, ANY PORT(1, 3)



2674 drw 08

NOTES:
1. R/$\overline{W}$ = VIH for Read Cycles.
2. Addresses valid prior to or coincident with $\overline{CE}$ transition LOW.

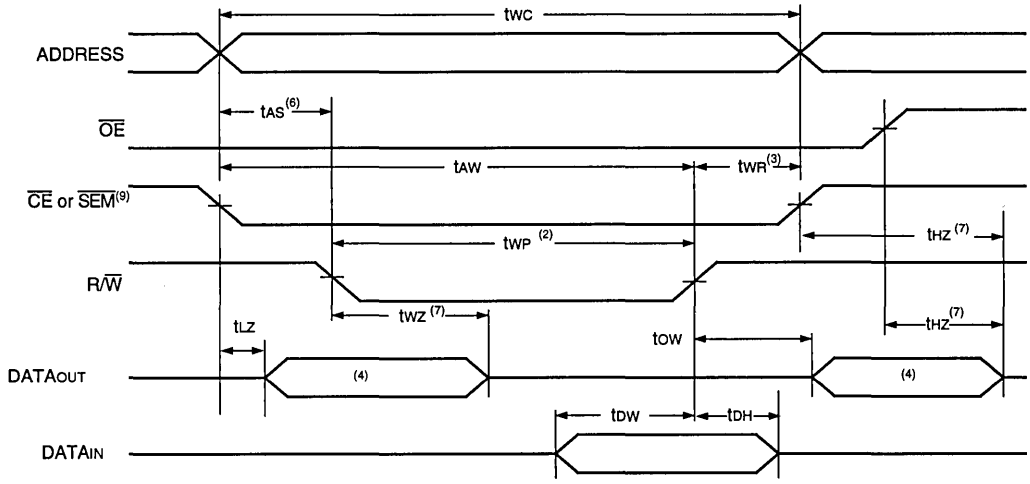
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Symbol	Parameter	IDT7052X25 COM'L. ONLY Min.	IDT7052X25 COM'L. ONLY Max.	IDT7052X35 Min.	IDT7052X35 Max.	IDT7052X45 Min.	IDT7052X45 Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time	25	—	35	—	45	—	ns
tEW	Chip Enable to End-of-Write	20	—	30	—	35	—	ns
tAW	Address Valid to End-of-Write	20	—	30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width(3)	20	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	20	—	20	—	ns
tHZ	Output High-Z Time(1, 2)	—	15	—	15	—	20	ns
tDH	Data Hold Time	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High-Z(1, 2)	—	15	—	15	—	20	ns
tOW	Output Active from End-of-Write(1, 2)	0	—	0	—	0	—	ns
tWDD	Write Pulse to Data Delay(4)	—	45	—	55	—	65	ns
tDDD	Write Data Valid to Read Data Delay(4)	—	35	—	45	—	55	ns
BUSY INPUT TIMING								
tWB	Write to $\overline{BUSY}$(5)	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$(6)	15	—	20	—	20	—	ns

2674 tbl 11

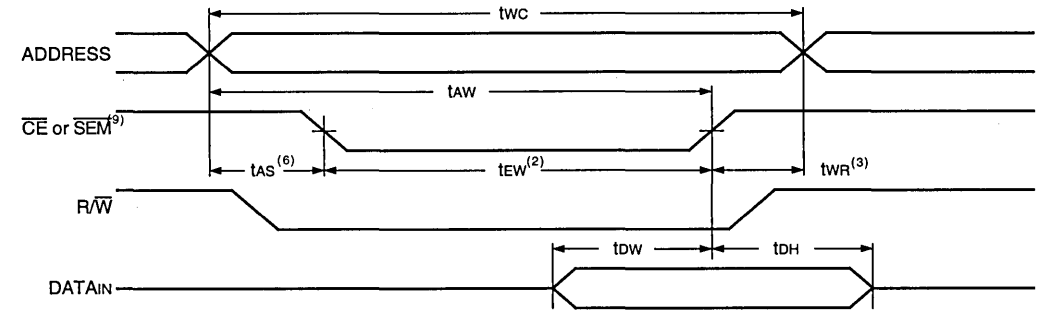
NOTES:
1. Transition is measured ±200mV from low or high impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed but is not production tested.
3. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP .Specified for $\overline{OE}$ at high (refer to "Timing Waveform of Write Cycle", Note 7).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read".
5. To ensure that the write cycle is inhibited on port "A" during contention from Port "B". Port "A" may be any of the four ports and Port "B" is any other port.
6. To ensure that a write cycle is completed on port "A" after contention from Port "B". Port "A" may be any of the four ports and Port "B" is any other port.
7. "X" in part number indicates power rating.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(5,8)



2674 drw 09

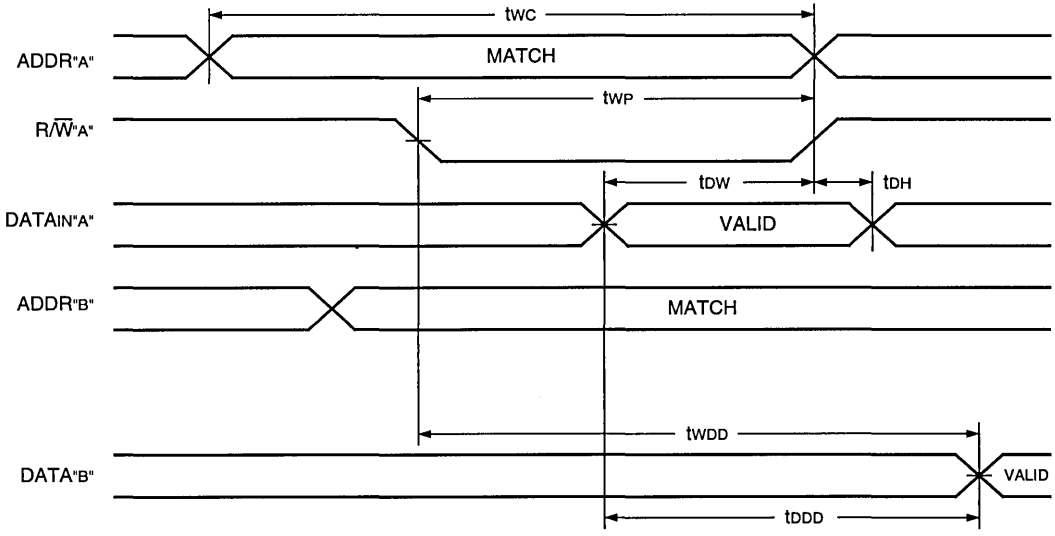
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1, 5)



2674 drw 10

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. Transition is measured ±200mV from low or high impedance voltage with the Output Test Load (Figure 2).This parameter is guaranteed but is not production tested.
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. tEW must be met for either condition.

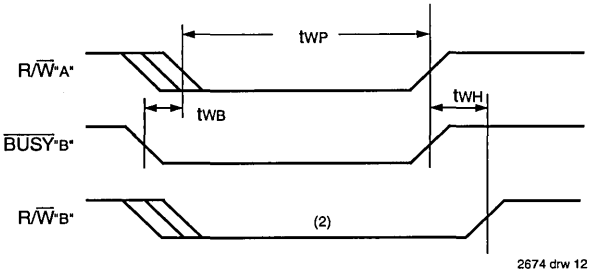
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ(1, 2, 3)



2674 drw 11

NOTES:
1. Assume $\overline{BUSY}$ input = VIH and $\overline{CE}$ = VIL for the writing port.
2. $\overline{OE}$ = VIL for the reading ports.
3. All timing is the same for left and right ports. Port "A" may be either of the four ports and Port "B" is any other port.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT



2674 drw 12

NOTES:
1. $\overline{BUSY}$ is aserted on Port "B" blocking R/$\overline{W}$"B" until $\overline{BUSY}$ "B" goes HIGH.

FUNCTIONAL DESCRIPTION

The IDT7052 provides four ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE}$ HIGH). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. READ/WRITE conditions are illustrated in the table below.

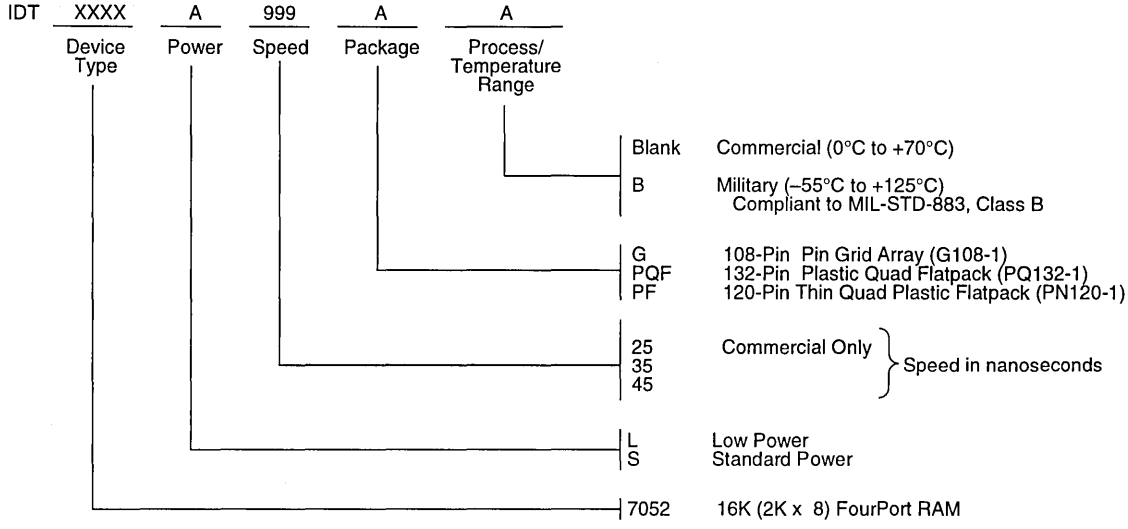
TABLE I – READ/WRITE CONTROL

Any Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D0-7	Function
X	H	X	Z	Port Deselected: Power-Down
X	H	X	Z	$\overline{CE}_{P1}$ = $\overline{CE}_{P2}$ = $\overline{CE}_{P3}$ = $\overline{CE}_{P4}$ =VIH Power Down Mode, ISB or ISB1
L	L	X	DATAIN	Data on port written into memory(2, 3)
H	L	L	DATAOUT	Data in memory output on port
X	X	H	Z	Outputs Disabled

2698 tbl 12

NOTES:
1. "H" = VIH, "L" = VIL, "X" = Don't Care, "Z "= High Impedance
2. If $\overline{BUSY}$ = VIL, write is blocked.
3. For valid write operation, no more than one port can write to the same address location at the same time.

ORDERING INFORMATION



2674 drw 13

Integrated Device Technology, Inc.

HIGH SPEED 64K (4K X 16 BIT) SEQUENTIAL ACCESS RANDOM ACCESS MEMORY (SARAM™)

IDT70824S/L

FEATURES:

- 4K x 16 Sequential Access Random Access Memory (SARAM™)
  - Sequential Access from one port and standard Random Access from the other port
  - Separate upper-byte and lower-byte control of the Random Access Port
- High speed operation
  - 20ns t_{AA} for random access port
  - 20ns t_{CD} for sequential port
  - 25ns clock cycle time
- Architecture based on Dual-Port RAM cells
- Electrostatic discharge ≥ 2001V, Class II
- Compatible with Intel BMIC and 82430 PCI Set
- Width and Depth Expandable
- Sequential side
  - Address based flags for buffer control
  - Pointer logic supports up to two internal buffers
- Battery backup operation - 2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Available in 80-pin TQFP and 84-pin PGA
- Military product compliant to MIL-STD-883.
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications.

DESCRIPTION:

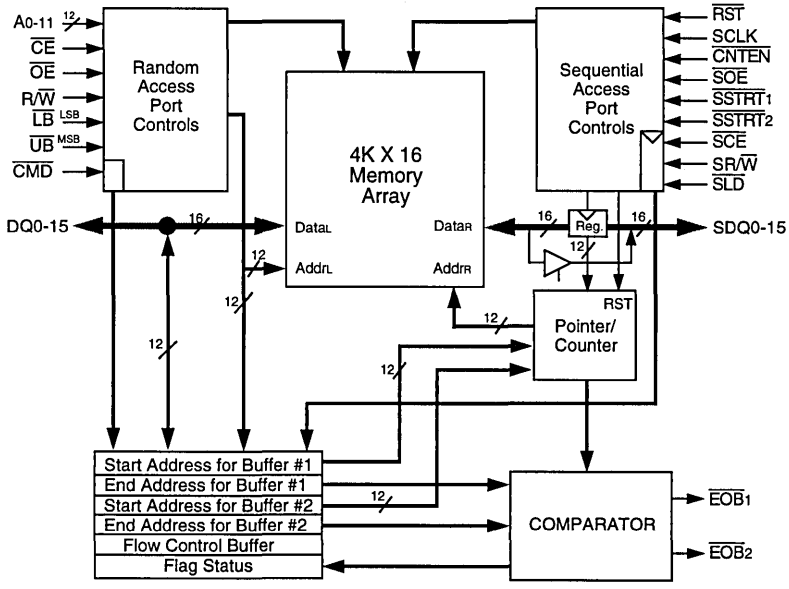
The IDT70824 is a high-speed 4K x 16-bit Sequential Access Random Access Memory (SARAM). The SARAM offers a single-chip solution to buffer data sequentially on one port, and be accessed randomly (asynchronously) through the other port. The device has a Dual-Port RAM based architecture with a standard SRAM interface for the random (asynchronous) access port, and a clocked interface with counter sequencing for the sequential (synchronous) access port.

Fabricated using CMOS high-performance technology, this memory device typically operates on less than 900mW of power at maximum high-speed clock-to-data and Random Access. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70824 is packaged in a 80-pin Thin Plastic Quad Flatpack (TQFP) or 84-pin Ceramic Pin Grid Array (PGA). Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

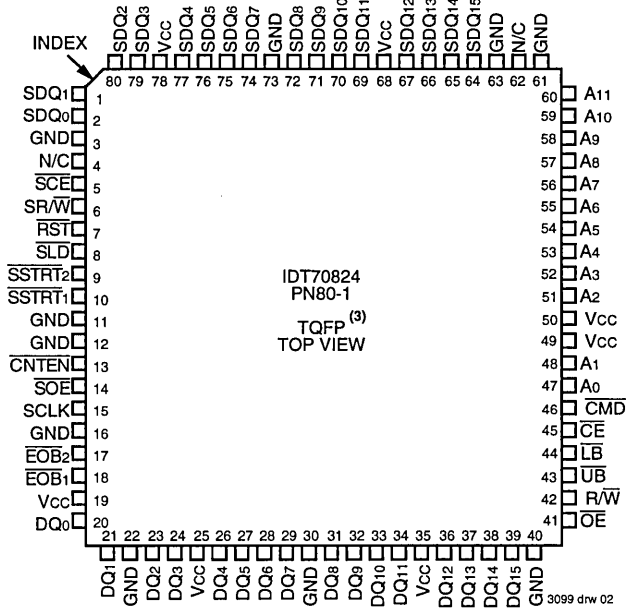
6

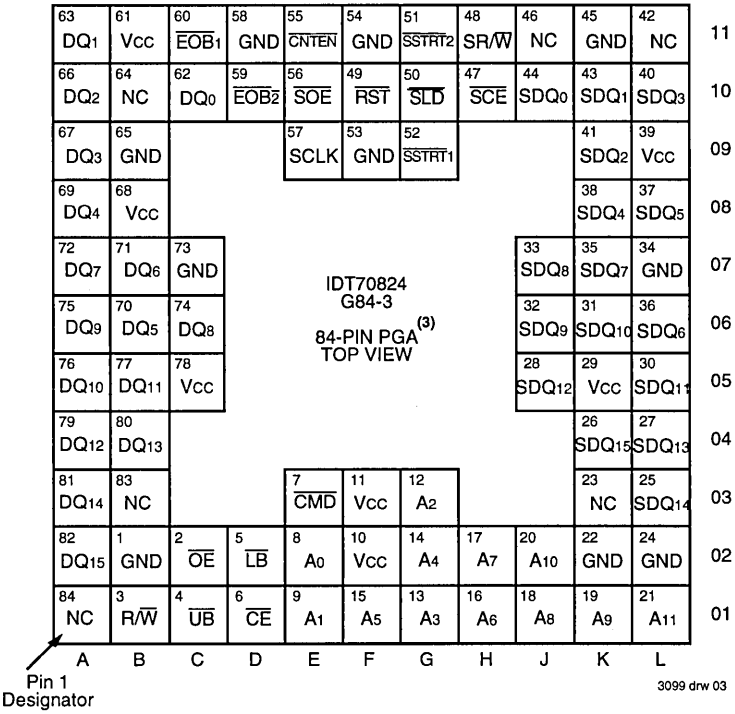
FUNCTIONAL BLOCK DIAGRAM



3099 drw 01

PIN CONFIGURATIONS





NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

PIN DESCRIPTIONS: RANDOM ACCESS PORT

SYMBOL	NAME	I/O	DESCRIPTION
A0-A11	Address Lines	I	Address inputs to access the 4096-word (16 bit) memory array.
DQ0-DQ15	Inputs/Outputs	I	Random access data inputs/outputs for 16-bit wide data.
$\overline{CE}$	Chip Enable	I	When $\overline{CE}$ is LOW, the random access port is enabled. When $\overline{CE}$ is HIGH, the random access port is disabled into power-down mode and the DQ outputs are in the high-impedance state. All data is retained during $\overline{CE}$ = VIH, unless it is altered by the sequential port. $\overline{CE}$ and $\overline{CMD}$ may not be LOW at the same time.
$\overline{CMD}$	Control Register Enable	I	When $\overline{CMD}$ is LOW, Address lines A0-A2, R/$\overline{W}$, and inputs/outputs DQ0-DQ11, are used to access the control register, the flag register, and the start and end of buffer registers. $\overline{CMD}$ and $\overline{CE}$ may not be LOW at the same time.
R/$\overline{W}$	Read/Write Enable	I	If $\overline{CE}$ is LOW and $\overline{CMD}$ is HIGH, data is written into the array when R/$\overline{W}$ is LOW and read out of the array when R/$\overline{W}$ is HIGH. If $\overline{CE}$ is HIGH and $\overline{CMD}$ is LOW, R/$\overline{W}$ is used to access the buffer command registers. $\overline{CE}$ and $\overline{CMD}$ may not be LOW at the same time.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW and R/$\overline{W}$ is HIGH, DQ0-DQ15 outputs are enabled. When $\overline{OE}$ is HIGH, the DQ outputs are in the high-impedance state.
$\overline{LB}$,$\overline{UB}$	Lower Byte, Upper Byte Enables	I	When $\overline{LB}$ is LOW, DQ0-DQ7 are accessible for read and write operations. When $\overline{LB}$ is HIGH, DQ0-DQ7 are tri-stated and blocked during read and write operations. $\overline{UB}$ controls access for DQ8-DQ15 in the same manner and is asynchronous from $\overline{LB}$.
VCC	Power Supply		Seven +5V power supply pins. All Vcc pins must be connected to the same +5V VCC supply.
GND	Ground		Ten Ground pins. All Ground pins must be connected to the same Ground supply.

3099 tbl 01

PIN DESCRIPTIONS: SEQUENTIAL ACCESS PORT

SYMBOL	NAME	I/O	DESCRIPTION
SDQ0-SDQ15	Inputs	I/O	Sequential data inputs/outputs for 16-bit wide data.
SCLK	Clock	I	SDQ0-SDQ15, $\overline{SCE}$, SR/$\overline{W}$, and $\overline{SLD}$ are registered on the LOW-to-HIGH transition of SCLK. Also, the sequential access port address pointer increments by 1 on each LOW-to-HIGH transition of SCLK when $\overline{CNTEN}$ is LOW.
$\overline{SCE}$	Chip Enable	I	When $\overline{SCE}$ is LOW, the sequential access port is enabled on the LOW-to-HIGH transition of SCLK. When $\overline{SCE}$ is HIGH, the sequential access port is disabled into powered-down mode on the LOW-to-HIGH transition of SCLK, and the SDQ outputs are in the high-impedance state. All data is retained, unless altered by the random access port.
$\overline{CNTEN}$	Counter Enable	I	When $\overline{CNTEN}$ is LOW, the address pointer increments on the LOW-to-HIGH transition of SCLK.
SR/$\overline{W}$	Read/Write Enable	I	When SR/$\overline{W}$ and SCE are LOW, a write cycle is initiated on the LOW-to-HIGH transition of SCLK. When SR/$\overline{W}$ is HIGH, and $\overline{SCE}$ and $\overline{SOE}$ are LOW, a read cycle is initiated on the LOW-to-HIGH transition of SCLK.
$\overline{SLD}$	Address Pointer Load Control	I	When $\overline{SLD}$ is sampled LOW, there is an internal delay of one cycle before the address pointer changes. When $\overline{SLD}$ is LOW, data on the inputs SDQ0-SDQ11 is loaded into a data-in register on the LOW-to-HIGH transition of SCLK. On the cycle following $\overline{SLD}$, the address pointer changes to the address location contained in the data-in register. $\overline{SSTRT1}$ and $\overline{SSTRT2}$ may not be LOW while $\overline{SLD}$ is LOW or during the cycle following $\overline{SLD}$.
$\overline{SSTRT1}$, $\overline{SSTRT2}$	Load Start of Address Register	I	When $\overline{SSTRT1}$ or $\overline{SSTRT2}$ is LOW, the start of address register #1 or #2 is loaded into the address pointer on the LOW-to-HIGH transition of SCLK. The start addresses are stored in internal registers. $\overline{SSTRT1}$ and $\overline{SSTRT2}$ may not be LOW while $\overline{SLD}$ is LOW or during the cycle following $\overline{SLD}$.
$\overline{EOB1}$, $\overline{EOB2}$	End of Buffer Flag	O	$\overline{EOB1}$ or $\overline{EOB2}$ is output LOW when the address pointer is incremented to match the address stored in the end of buffer registers. The flags can be cleared by either asserting $\overline{RST}$ LOW or by writing zero into bit 0 and/or bit 1 of the control register at address 101. $\overline{EOB1}$ and $\overline{EOB2}$ are dependent on separate internal registers, and therefore separate match addresses.
$\overline{SOE}$	Output Enable	I	$\overline{SOE}$ controls the data outputs and is independent of SCLK. When $\overline{SOE}$ is LOW, output buffers and the sequentially addressed data is output. When $\overline{SOE}$ is HIGH, the SDQ output bus is in the high-impedance state. $\overline{SOE}$ is asynchronous to SCLK.
$\overline{RST}$	Reset	I	When $\overline{RST}$ is LOW, all internal registers are set to their default state, the address pointer is set to zero and the $\overline{EOB1}$ and $\overline{EOB2}$ flags are set HIGH. $\overline{RST}$ is asynchronous to SCLK.

Note: "I/O" is bidirectional Input and Output. "I" is Input and "O" is Output.

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTES: 3099 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

3099 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0(2)	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 3099 tbl 05

1. VIL ≥ –1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 0.5V.

CAPACITANCE (TA = +25°C, F = 1.0MHz, TQFP only)

Symbol	Parameter(1)	Conditions(2)	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	9	pF
COUT	Output Capacitance	VOUT = 3dV	10	pF

NOTE: 3099 tbl 06

1. This parameter is determined by device characterization, but is not production tested.
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (VCC = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT70824S		IDT70824L		Unit
			Min.	Max.	Min.	Max.	
|ILI|	Input Leakage Current	VCC = Max. VIN = GND to VCC	—	5.0	—	1.0	µA
|ILO|	Output Leakage Current	VCC = Max. $\overline{CE}$ and $\overline{SCE}$ = VIH VOUT = GND to VCC	—	5.0	—	1.0	µA
VOL	Output Low Voltage	IOL = 4mA, VCC = Min.	—	0.4	—	0.4	V
VOH	Output High Voltage	IOH = –4mA, VCC = Min.	2.4	—	2.4	—	V

3099 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		70824X20 COM'L ONLY Typ.[2]	70824X20 COM'L ONLY Max.	70824X25 COM'L ONLY Typ.[2]	70824X25 COM'L ONLY Max.	70824X35 Typ.[2]	70824X35 Max.	70824X45 Typ.[2]	70824X45 Max.	Unit
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = VIL, Outputs Open, $\overline{SCE}$ = VIL[5] f = fMAX[3]	MIL.	S	—	—	—	—	160	400	155	400	mA
				L	—	—	—	—	160	340	155	340	
			COM'L.	S	180	380	170	360	160	340	155	340	
				L	180	330	170	310	160	290	155	290	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{SCE}$ and $\overline{CE} \geq$ VIH[7] $\overline{CMD}$ = VIH f = fMAX[3]	MIL.	S	—	—	—	—	20	85	16	85	mA
				L	—	—	—	—	20	65	16	65	
			COM'L.	S	25	70	25	70	20	70	16	70	
				L	25	50	25	50	20	50	16	50	
ISB2	Standby Current (One Port - TTL Level Input)	$\overline{CE}$ or $\overline{SCE}$ = VIH Active Port Outputs Open, f = fMAX[3]	MIL.	S	—	—	—	—	95	290	90	290	mA
				L		—	—	—	95	250	90	250	
			COM'L.	S	115	260	105	250	95	240	90	240	
				L	115	230	105	220	95	210	90	210	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}$ and $\overline{SCE} \geq$ VCC - 0.2V[6] VIN ≥ VCC - 0.2V or VIN ≤ 0.2V, f = 0[4]	MIL.	S	—	—	—	—	1.0	30	1.0	30	mA
				L	—	—	—	—	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	1.0	15	1.0	15	
				L	0.2	5	0.2	5	0.2	5	0.2	5	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	One Port $\overline{CE}$ or $\overline{SCE} \geq$ VCC - 0.2V[6,7] Outputs Open (Active port), f = fMAX[3] VIN ≥ VCC - 0.2V or VIN ≤ 0.2V	MIL.	S	—	—	—	—	90	260	85	260	mA
				L	—	—	—	—	90	215	85	215	
			COM'L.	S	110	240	100	230	90	220	85	220	
				L	110	200	100	190	90	180	85	180	

NOTES:
1. 'X' in part number indicates power rating (S or L).
2. Vcc = 5V, Ta = +25°C; guaranteed by device characterization but not production tested.
3. At f = fMAX, address, control lines (except Output Enable), and SCLK are cycling at the maximum frequency read cycle of 1/tRC.
4. f = 0 means no address or control lines change.
5. $\overline{SCE}$ may transition, but is Low ($\overline{SCE}$=VIL) when clocked in by SCLK.
6. $\overline{SCE}$ may be ≤ 0.2V, after it is clocked in, since SCLK=VIH must be clocked in prior to powerdown.
7. If one port is enabled (either $\overline{CE}$ or $\overline{SCE}$ = Low) then the other port is disabled (SCE or CE = High, respectively). CMOS High ≥ Vcc - 0.2V and Low ≤ 0.2V, and TTL High = VIH and Low = VIL.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L VERSION ONLY) ($V_{LC} \leq 0.2V$, $V_{HC} \geq V_{CC} - 0.2V$)

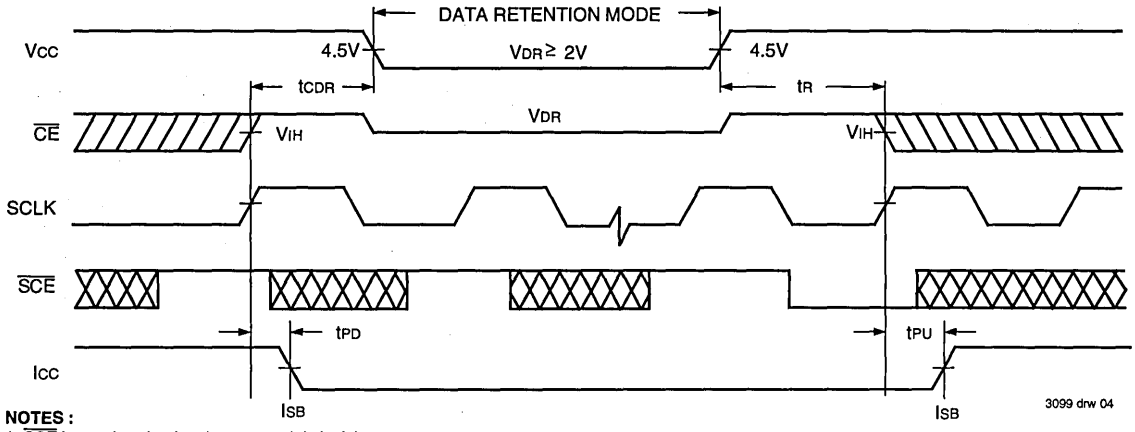
Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
VDR	VCC for Data Retention	VCC = 2V		2.0	—	—	V
ICCDR	Data Retention Current	$\overline{CE}$ = VHC	MIL.	—	100	4000	µA
		VIN = VHC or = VLC	COM'L.	—	100	1500	
tCDR[3]	Chip Deselect to Data Retention Time	$\overline{SCE}$ = VHC[4] when SCLK= ↓		0	—	—	ns
tR[3]	Operation Recovery Time	$\overline{CMD} \geq$ VHC		tRC[2]	—	—	ns

NOTES :
1. TA = +25°C, Vcc = 2V; guaranteed by device characterization but not production tested.
2. tRC = Read Cycle Time
3. This parameter is guaranteed by device characterization, but is not production tested.
4. To initiate data retention, $\overline{SCE}$ = VIH must be clocked in.

3099 tbl 09

6

DATA RETENTION POWER DOWN/UP WAVEFORM (RANDOM AND SEQUENTIAL PORT)[1, 2]



NOTES :
1. $\overline{SCE}$ is synchronized to the sequential clock input.
2. $\overline{CMD} \geq$ Vcc - 0.2V.

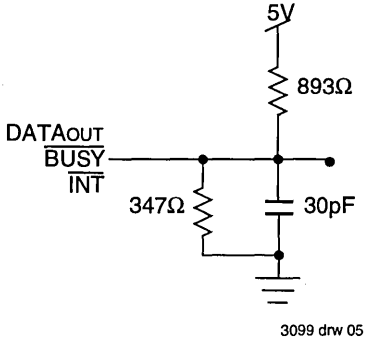


Figure 1. AC Output Test Load

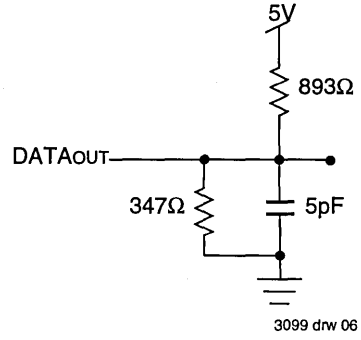


Figure 2. Output Test Load (for tCLZ, tBLZ, tOLZ, tCHZ, tBHZ,tOHZ,tWHZ, tCKHZ, and tCKLZ)
Including scope and jig.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 & 2

3099 tbl 10

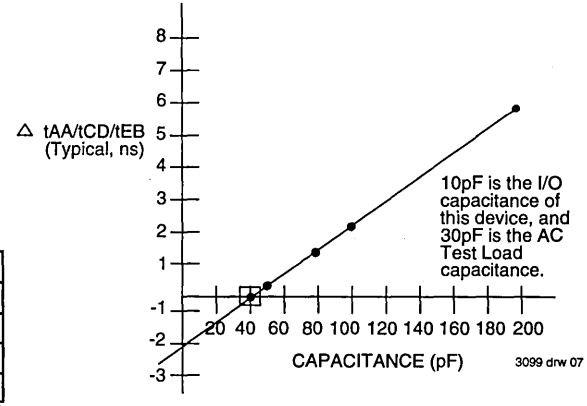


Figure 1A. Lumped Capacitance Load Typical Derating Curve

TRUTH TABLE: RANDOM ACCESS READ AND WRITE (1,2)

Inputs/Outputs								MODE
$\overline{CE}$	$\overline{CMD}$	R/$\overline{W}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	DQ0-DQ7	DQ8-DQ15	
L	H	H	L	L	L	DATAOUT	DATAOUT	Read both Bytes.
L	H	H	L	L	H	DATAOUT	High-Z	Read lower Byte only.
L	H	H	L	H	L	High-Z	DATAOUT	Read upper Byte only.
L	H	L	H(3)	L	L	DATAIN	DATAIN	Write to both Bytes.
L	H	L	H(3)	L	H	DATAIN	High-Z	Write to lower Byte only.
L	H	L	H(3)	H	L	High-Z	DATAIN	Write to upper Byte only.
H	H	X	X	X	X	High-Z	High-Z	Both Bytes deselected and powered down.
L	H	H	H	X	X	High-Z	High-Z	Outputs disabled but not powered down.
L	H	X	X	H	H	High-Z	High-Z	Both Bytes deselected but not powered down.
H	L	L	H(3)	L(4)	L(4)	DATAIN	DATAIN	Write DQ0-DQ11 to the Buffer Command Register.
H	L	H	L	L(4)	L(4)	DATAOUT	DATAOUT	Read contents of the Buffer Command Register via DQ0-DQ12.

3099 tbl 11

NOTE:
1. H = VIH, L = VIL, X = Don't Care, and High-Z = High-impedance.
2. $\overline{RST}$, $\overline{SCE}$, $\overline{CNTEN}$, SR/$\overline{W}$, $\overline{SLD}$, $\overline{SSTRT1}$, $\overline{SSTRT2}$, SCLK, SDQ0-SDQ15, $\overline{EOB1}$, $\overline{EOB2}$, and $\overline{SOE}$ are unrelated to the random access port control and operation.
3. If $\overline{OE}$ = VIL during write, tWHZ must be added to the tWP or tCW write pulse width to allow the bus to float prior to being driven.
4. Byte operations to control register using $\overline{UB}$ and $\overline{LB}$ separately are also allowed.

TRUTH TABLE: SEQUENTIAL READ (1,2,3,4,5)

Inputs/Outputs								MODE
SCLK	$\overline{SCE}$	$\overline{CNTEN}$	SR/$\overline{W}$	$\overline{EOB1}$	$\overline{EOB2}$	$\overline{SOE}$	SDQ	
↓	L	L	H	LOW	LAST	L	[EOB1]	Counter Advanced Sequential Read with $\overline{EOB1}$ reached.
↓	L	H	H	LAST	LAST	L	[EOB1 - 1]	Non-Counter Advanced Sequential Read, without $\overline{EOB1}$ reached.
↓	L	L	H	LAST	LOW	L	[EOB2]	Counter Advanced Sequential Read with $\overline{EOB2}$ reached.
↓	L	H	H	LAST	LAST	L	[EOB2 - 1]	Non-Counter Advanced Sequential Read without $\overline{EOB2}$ reached.
↓	L	L	H	LOW	LOW	H	HIGH-Z	Counter Advanced Sequential Non-Read with $\overline{EOB1}$ and $\overline{EOB2}$ reached.

3099 tbl 12

NOTES:
1. H = VIH, L = VIL, X = Don't Care, High-Z = High impedance, and LOW = VOL.
2. $\overline{RST}$, $\overline{SLD}$, $\overline{SSTRT1}$, $\overline{SSTRT2}$ are continuously HIGH during sequential access, other than pointer access operations.
3. '[X]' refers to the contents of address 'X'.
4. $\overline{CE}$, $\overline{OE}$, R/$\overline{W}$, $\overline{CMD}$, $\overline{LB}$, $\overline{UB}$, and DQ0-DQ15 are unrelated to the sequential port control and operation except for $\overline{CMD}$ which must not be used concurrently with the sequential port operation (due to the counter and register control). $\overline{CMD}$ should be HIGH ($\overline{CMD}$ = VIH) during sequential port access.
5. "LAST" refers to the previous value still being output, no change.

TRUTH TABLE: SEQUENTIAL WRITE (1,2,3,4,5,6)

Inputs/Outputs								MODE
SCLK	$\overline{SCE}$	$\overline{CNTEN}$	SR/$\overline{W}$	$\overline{EOB1}$	$\overline{EOB2}$	$\overline{SOE}$	SDQ	
↓	L	H	L	LAST	LAST	H	SDQIN	Non-Counter Advanced Sequential Write, without $\overline{EOB1}$ or $\overline{EOB2}$ reached
↓	L	L	L	LOW	LOW	H	SDQIN	Counter Advanced Sequential Write with $\overline{EOB1}$ and $\overline{EOB2}$ reached.
↓	H	X	X	LAST	LAST	X	High-Z	No Write or Read due to Sequential port Deselect.

3099 tbl 13

NOTES:
1. H = VIH, L = VIL, X = Don't Care, and High-Z = High-impedance. LOW = VOL.
2. $\overline{RST}$, $\overline{SLD}$, $\overline{SSTRT1}$, $\overline{SSTRT2}$ are continuously HIGH during a sequential write access, other than pointer access operations.
3. $\overline{CE}$, $\overline{OE}$, R/$\overline{W}$, $\overline{CMD}$, $\overline{LB}$, $\overline{UB}$, and DQ0-DQ15 are unrelated to the sequential port control and operation except for $\overline{CMD}$ which must not be used concurrently with the sequential port operation (due to the counter and register control). $\overline{CMD}$ should be HIGH ($\overline{CMD}$ = VIH) during sequential port access.
4. $\overline{SOE}$ must be HIGH ($\overline{SOE}$=VIH) prior to write conditions only if the previous cycle is a read cycle, since the data being written must be an input at the rising edge of the clock during the cycle in which SR/$\overline{W}$ = VIL.
5. SDQIN refers to SDQ0-SDQ15 inputs.
6. "LAST" refers to the previous value still being output, no change.

TRUTH TABLE: SEQUENTIAL ADDRESS POINTER OPERATIONS (1,2,3,4,5)

Inputs/Outputs					
SCLK	$\overline{SLD}$	$\overline{SSTRT1}$	$\overline{SSTRT2}$	$\overline{SOE}$	MODE
↑	H	L	H	X	Start address for Buffer #1 loaded into Address Pointer.
↑	H	H	L	X	Start address for Buffer #2 loaded into Address Pointer.
↑	L	H	H	H(6)	Data on SDQ0-SDQ12 loaded into Address Pointer .

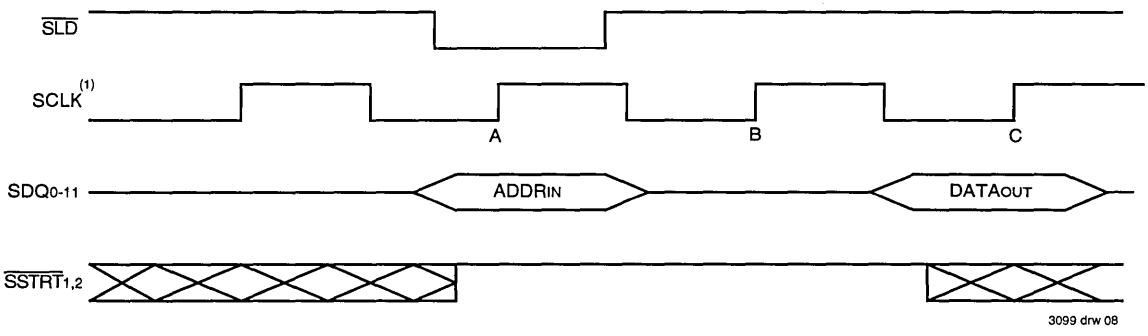
3099 tbl 14

NOTES:
1. H = V_{IH}, L = V_{IL}, X = Don't Care, and High-Z = High-impedance.
2. $\overline{RST}$ is continuously HIGH. The conditions of $\overline{SCE}$, $\overline{CNTEN}$, and SR/$\overline{W}$ are unrelated to the sequential address pointer operations.
3. $\overline{CE}$, $\overline{OE}$, R/$\overline{W}$, $\overline{LB}$, $\overline{UB}$, and DQ0-DQ15 are unrelated to the sequential port control and operation, except for $\overline{CMD}$ which must not be used concurrently with the sequential port operation (due to the counter and register control). $\overline{CMD}$ should be HIGH (CMD = V_{IH}) during sequential port access.
4. Address pointer can also change when it reaches an end of buffer address. See Flow Control Bits table.
5. When $\overline{SLD}$ is sampled LOW, there is an internal delay of one cycle before the address pointer changes. The state of $\overline{CNTEN}$ is ignored and the address is not incremented during the two cycles.
6. $\overline{SOE}$ may be LOW with $\overline{SCE}$ deselect or in the write mode using SR/$\overline{W}$.

ADDRESS POINTER LOAD CONTROL (SLD)

In $\overline{SLD}$ mode, there is an internal delay of one cycle before the address pointer changes in the cycle following $\overline{SLD}$. When $\overline{SLD}$ is LOW, data on the inputs SDQ0-SDQ11 is loaded into a data-in register on the LOW-to-HIGH transition of $\overline{SCLK}$. On the cycle following $\overline{SLD}$, the address pointer changes to the address location contained in the data-in register. $\overline{SSTRT1}$, $\overline{SSTRT2}$ may not be low while $\overline{SLD}$ is LOW, or during the cycle following $\overline{SLD}$. The $\overline{SSTRT1}$ and $\overline{SSTRT2}$ require only one clock cycle, since these addresses are pre-loaded in the registers already.

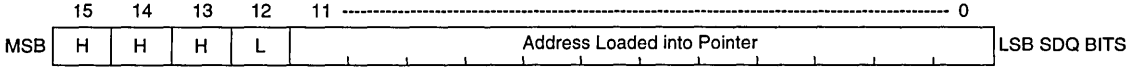
$\overline{SLD}$ MODE (1)



3099 drw 08

NOTE:
1. At SCLK edge (A), SDQ0-SDQ11 data is loaded into a data-in register. At edge (B), contents of the data-in register are loaded into the address pointer (i.e. address pointer changes). At SCLK edge (A), $\overline{SSTRT1}$ and $\overline{SSTRT2}$ must be high to ensure for proper sequential address pointer loading. At SCLK edge (B), $\overline{SLD}$ and $\overline{SSTRT1,2}$ must be high to ensure for proper sequential address pointer loading. For $\overline{SSTRT1}$ or $\overline{SSTRT2}$, the data to be read will be ready for edge (B), while data will not be ready at edge (B) when $\overline{SLD}$ is used, but will be ready at edge (C).

SEQUENTIAL LOAD OF ADDRESS INTO POINTER/COUNTER (1)



3099 drw 09

NOTE:
1. "H" = V_{IH} and "L" = V_{IL} for the SDQ intput state.

Reset ($\overline{RST}$)

Setting $\overline{RST}$ LOW resets the control state of the SARAM. $\overline{RST}$ functions asynchronously of SCLK (i.e. not registered). The default states after a reset operation are displayed in the adjacent chart.

Register	Contents
Address Pointer	0
$\overline{EOB}$ Flags	Cleared to High state
Buffer Flow Mode	BUFFER CHAINING
Start Address Buffer #1	0 (1)
End Address Buffer #1	4095 (4K)
Start Address Buffer #2(1)	Cleared (set at invalid points)
End Address Buffer #2(1)	Cleared (set at invalid points)
Registered State	$\overline{SCE}$ = VIH, SR/$\overline{W}$ = VIL

3099 tbl 15

Notes:
1. Start address and End of address for Buffer #2 and the Flow Control for both Buffer #1 and #2, must be programmed as described in the "Buffer Command Mode" section.

BUFFER COMMAND MODE ($\overline{CMD}$)

Buffer Command Mode ($\overline{CMD}$) allows the random access port to control the state of the two buffers. Address pins A0-A2 and I/O pins DQ0-DQ11 are used to access the start of buffer and the end of buffer addresses and to set the flow control mode of each buffer. The Buffer Command Mode also allows reading and clearing the status of the EOB flags. Seven different CMD cases are available depending on the conditions of A0-A2 and R/W. Address bits A3-A11 and data I/O bits DQ12-DQ15 are not used during this operation.

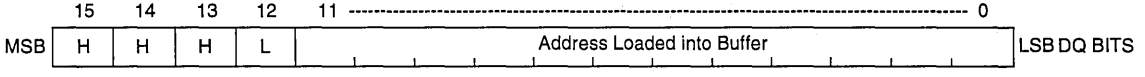
RANDOM ACCESS PORT $\overline{CMD}$ MODE(1)

Case #	A2-A0	R/$\overline{W}$	DESCRIPTIONS
1	000	0 (1)	Write (read) the start address of Buffer #1 through DQ0-DQ11.
2	001	0 (1)	Write (read) the end address of Buffer #1 through DQ0-DQ11.
3	010	0 (1)	Write (read) the start address of Buffer #2 through DQ0-DQ11.
4	011	0 (1)	Write (read) the end address of Buffer #2 through DQ0-DQ11.
5	100	0 (1)	Write (read) flow control register
6	101	0	Write only – clear EOB1 and/or EOB2 flag
7	101	1	Read only – flag status register
8	110/111	(X)	(Reserved)

3099 tbl 16

NOTES:
1. R/$\overline{W}$ input "0(1)" indicates a write(0) or read(1) occurring with the same address input.

CASES 1 THROUGH 4: START AND END OF BUFFER REGISTER DESCRIPTION (1,2)



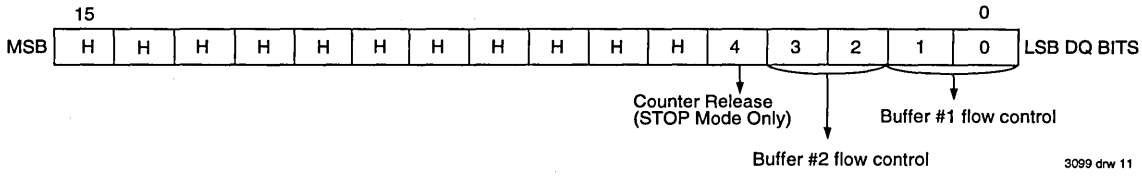
3099 drw 10

NOTES:
1. "H" = VOH for DQ in the output state and "Don't Cares" for DQ in the input state. "L" = VIL for DQ in the input state.
2. A write into the buffer occurs when R/$\overline{W}$ = VIL and a read when R/$\overline{W}$ = VIH. $\overline{EOB1}$/$\overline{SOB1}$ and $\overline{EOB2}$/$\overline{SOB2}$ are chosen through address A0-A2 while $\overline{CMD}$ = VIL and $\overline{CE}$ = VIH.

CASE 5: BUFFER FLOW MODES

Within the SARAM, the user can designate one of two buffer flow modes for each buffer. Each buffer flow mode defines a unique set of actions for the sequential port address pointer and EOB flags. In BUFFER CHAINING mode, after the address pointer reaches the end of the buffer, it sets the corresponding EOB flag and continues from the start address of the other buffer. In STOP mode, the address pointer stops incrementing after it reaches the end of the buffer. There is no linear or mask mode available.

FLOW CONTROL REGISTER DESCRIPTION[1,2]



NOTES:
1. "H" = VOH for DQ in the output state and "Don't Cares" for DQ in the input state.
2. Writing a 0 into bit 4 releases the address pointer after it is stopped due to the STOP mode and allows sequential write operations to resume. This occurs asynchronously of SCLK, and therefore caution should be taken. The pointer will be at address EOB+2 on the next rising edge of SCLK that is enabled by $\overline{CNTEN}$. The pointer is also released by $\overline{RST}$, $\overline{SLD}$, $\overline{SSTRT1}$ and $\overline{SSTRT2}$ operations.

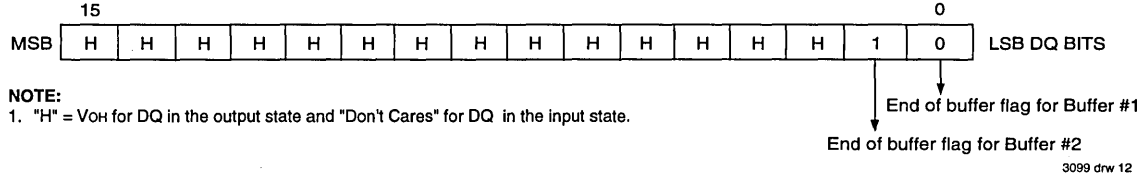
FLOW CONTROL BITS[5]

Flow Control Bits		
Bit 1 & Bit 0 (Bit 3 & Bit 2)	Mode	Functional Description
00	BUFFER CHAINING	$\overline{EOB1}$ ($\overline{EOB2}$) is asserted (Active Low output) when the pointer matches the end address of Buffer #1 (Buffer #2). The pointer value is changed to the start address of Buffer #2 (Buffer #1).[1,3]
01	STOP	$\overline{EOB1}$ ($\overline{EOB2}$) is asserted when the pointer matches the end address of Buffer #1 (Buffer #2). The address pointer will stop incrementing when it reaches the next address ($\overline{EOB}$ address + 1), if $\overline{CNTEN}$ is Low on the next clock's rising edge. Otherwise, the address pointer will stop incrementing on $\overline{EOB}$. Sequential write operations are inhibited after the address pointer is stopped. The pointer can be released by bit 4 of the flow control register. [1,2,4]

3099 tbl 17

NOTES:
1. $\overline{EOB1}$ and $\overline{EOB2}$ may be asserted (set) at the same time, if both end addresses have been loaded with the same value.
2. $\overline{CMD}$ Flow Control bits are unchanged, the count does not continue advancement.
3. If $\overline{EOB1}$ and $\overline{EOB2}$ are equal, then the pointer will jump to the start of Buffer #1.
4. If the counter has stopped at EOBx and was released by bit 4 of the flow control register, $\overline{CNTEN}$ must be LOW on the next rising edge of SCLK; otherwise the flow control will remain in the stop mode.
5. Flow Control Bit settings of '10' and '11' are reserved.
6. Start address and End of address for Buffer #2 and the Flow Control for both Buffer #1 and #2, must be programmed as described in the "Buffer Command Mode" section. $\overline{RST}$ conditions are not set to valid addresses.

CASES 6 AND 7: FLAG STATUS REGISTER BIT DESCRIPTION[1]



NOTE:
1. "H" = VOH for DQ in the output state and "Don't Cares" for DQ in the input state.

CASES 6: FLAG STATUS REGISTER WRITE CONDITIONS[1]

Flag Status Bit 0, (Bit 1)	Functional Description
0	Clears Buffer Flag $\overline{EOB1}$, ($\overline{EOB2}$).
1	No change to the Buffer Flag.[2]

3099 tbl 18

NOTE:
1. Either bit 0 or bit 1, or both bits, may be changed simultaneously. One may be cleared while the second is left alone, or both may be cleared.
2. Remains as it was prior to the $\overline{CMD}$ operation, either HIGH (1) or LOW (0).

CASE 7: FLAG STATUS REGISTER READ CONDITIONS

Flag Status Bit 0, (Bit 1)	Functional Description
0	$\overline{EOB1}$ ($\overline{EOB2}$) flag has not been set, the Pointer has not reached the End of the Buffer.
1	$\overline{EOB1}$ ($\overline{EOB2}$) flag has been set, the Pointer has reached the End of the Buffer.

3099 tbl 19

CASES 8 AND 9: (RESERVED)

Illegal operations. All outputs will be HIGH on the DQ bus during a READ.

RANDOM ACCESS PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (2,3)

Symbol	Parameter	IDT70824X20 COM'L ONLY		IDT70824X25 COM'L ONLY		IDT70824X35		IDT70824X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tRC	Read Cycle Time	20	—	25	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	35	—	45	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	—	45	ns
tBE	Byte Enable Access Time	—	20	—	25	—	35	—	45	ns
tOE	Output Enable Access Time	—	10	—	10	—	15	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tCLZ	Chip Select Low-Z Time(1)	3	—	3	—	3	—	3	—	ns
tBLZ	Byte Enable Low-Z Time(1)	3	—	3	—	3	—	3	—	ns
tOLZ	Output Enable Low-Z Time(1)	2	—	2	—	2	—	2	—	ns
tCHZ	Chip Select High-Z Time(1)	—	10	—	12	—	15	—	15	ns
tBHZ	Byte Enable High-Z Time(1)	—	10	—	12	—	15	—	15	ns
tOHZ	Output Enable High-Z Time(1)	—	9	—	11	—	15	—	15	ns
tPU	Chip Select Power-Up Time	0	—	0	—	0	—	0	—	ns
tPD	Chip Select Power-Down Time	—	20	—	25	—	35	—	45	ns

NOTES:

3099 tbl 20

1. Transition measured at ±200mV from steady state. This parameter is guaranteed with the AC Test Load (Figure 2) by device characterization, but is not production tested.
2. "X" in part number indicates power rating (S or L).
3. $\overline{CMD}$ access follows standard timing listed for both read and write accesses, ($\overline{CE}$ = VIH when $\overline{CMD}$ = VIL) or ($\overline{CMD}$ = VIH when $\overline{CE}$ = VIL).

RANDOM ACCESS PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (2,4)

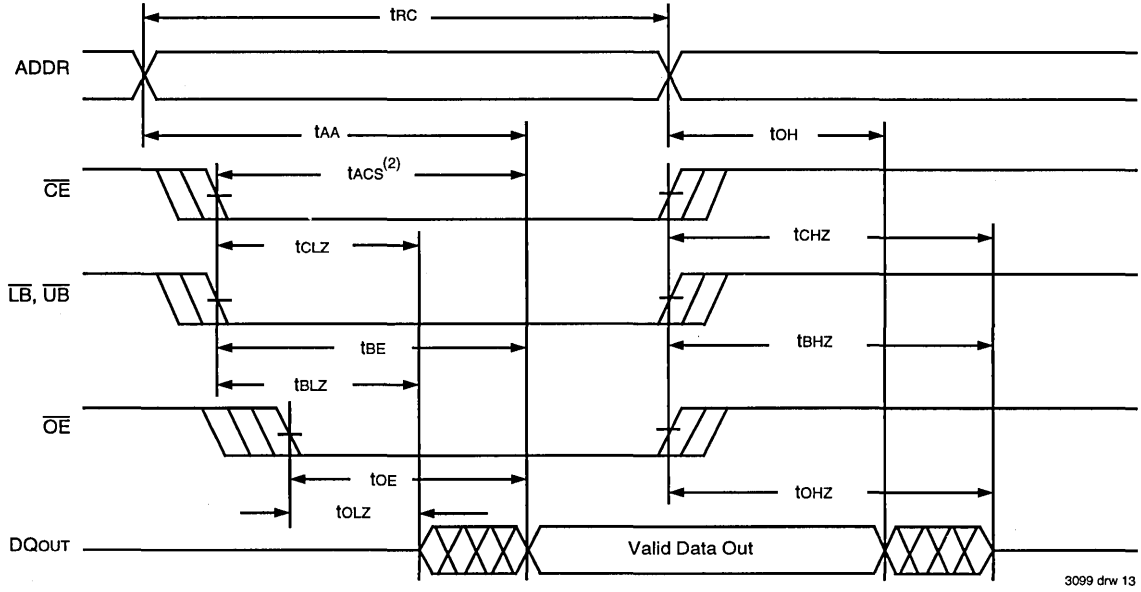
Symbol	Parameter	IDT70824X20 COM'L ONLY		IDT70824X25 COM'L ONLY		IDT70824X35		IDT70824X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	20	—	25	—	35	—	45	—	ns
tCW	Chip Select to End-of-Write	15	—	20	—	25	—	30	—	ns
tAW	Address Valid to End-of-Write(3)	15	—	20	—	25	—	30	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width(3)	13	—	20	—	25	—	30	—	ns
tBP	Byte Enable Pulse Width(3)	15	—	20	—	25	—	30	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable Output High-Z Time(1)	—	10	—	12	—	15	—	15	ns
tDW	Data Set-up Time	13	—	15	—	20	—	25	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End-of-Write	3	—	3	—	3	—	3	—	ns

NOTES:

3099 tbl 21

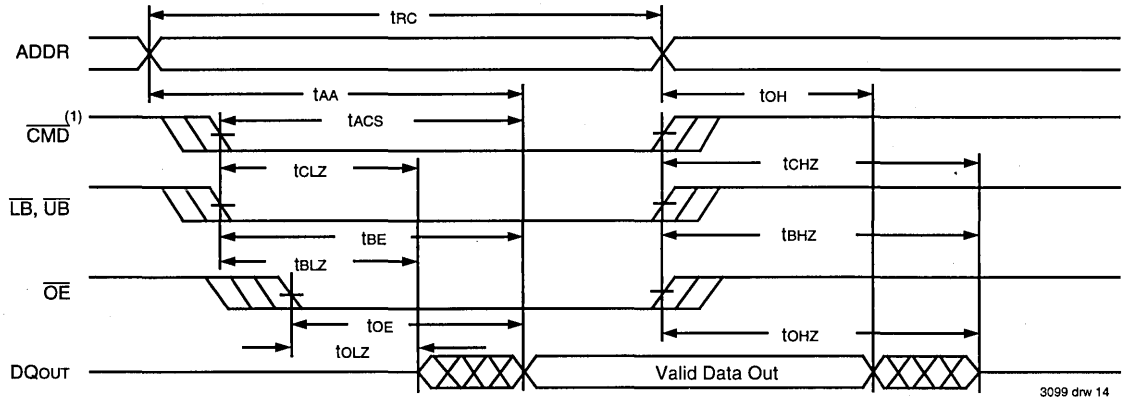
1. Transition measured at ±200mV from steady state. This parameter is guaranteed with the AC Test Load (Figure 2) by device characterization, but is not production tested.
2. "X" in part number indicates power rating (S or L).
3. $\overline{OE}$ is continuously HIGH, $\overline{OE}$ = VIH. If during the R/$\overline{W}$ controlled write cycle the $\overline{OE}$ is LOW, tWP must be greater or equal to tWHZ + tDW to allow the DQ drivers to turn off and on the data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during the R/$\overline{W}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified tWP. For the $\overline{CE}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to tCW timing.
4. $\overline{CMD}$ access follows standard timing listed for both read and write accesses, ($\overline{CE}$ = VIH when $\overline{CMD}$ = VIL) or ($\overline{CMD}$ = VIH when $\overline{CE}$ = VIL).

WAVEFORM OF READ CYCLES: RANDOM ACCESS PORT[1,2,3,4,5]



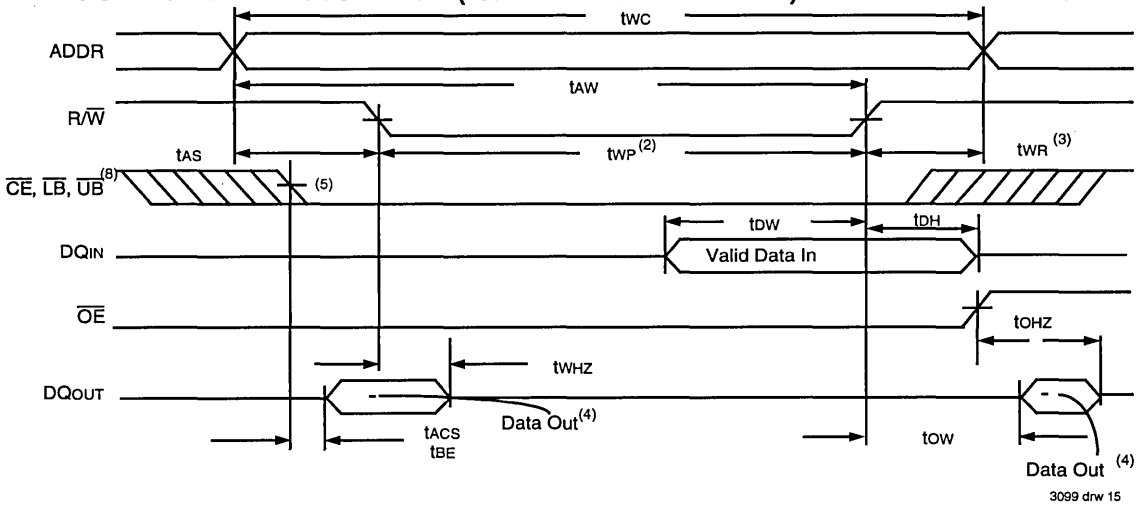
NOTES:
1. R/W is HIGH for Read cycle.
2. Address valid prior to or coincident with CE transition LOW; otherwise t_{AA} is the limiting parameter.

WAVEFORM OF READ CYCLES: BUFFER COMMAND MODE



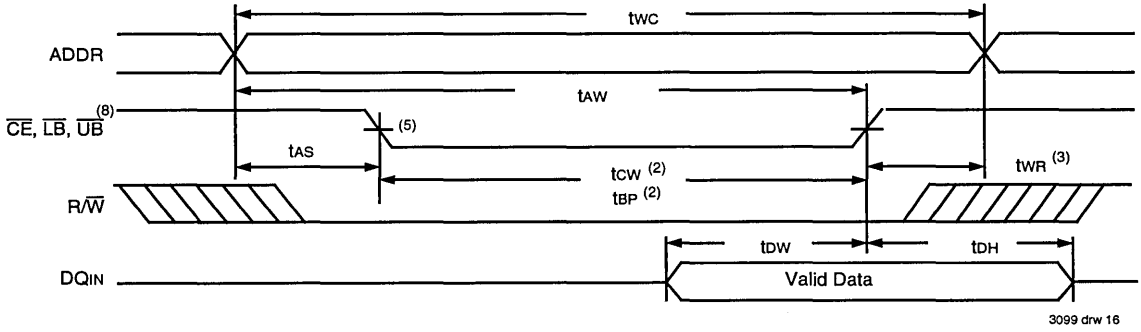
NOTES:
1. CE = V_{IH} when CMD = V_{IL}.

WAVEFORM OF WRITE CYCLE NO.1 (R/$\overline{W}$ CONTROLLED TIMING) RANDOM ACCESS PORT[1,6]



3099 drw 15

WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CE}$, $\overline{LB}$, AND/OR $\overline{UB}$ CONTROLLED TIMING) RANDOM ACCESS PORT[1,6,7]



3099 drw 16

NOTES:
1. R/$\overline{W}$, $\overline{CE}$, or $\overline{LB}$ and $\overline{UB}$ must be inactive during all address transitions.
2. A write occurs during the overlap of R/$\overline{W}$ = VIL, $\overline{CE}$ = VIL and $\overline{LB}$ = VIL and/or $\overline{UB}$ = VIL.
3. tWR is measured from the earlier of $\overline{CE}$ (and $\overline{LB}$ and/or $\overline{UB}$) or R/$\overline{W}$ going HIGH to the end of the write cycle.
4. During this period, DQ pins are in the output state and the input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.
6. $\overline{OE}$ is continuously HIGH, $\overline{OE}$ = VIH. If during the R/$\overline{W}$ controlled write cycle the $\overline{OE}$ is LOW, tWP must be greater or equal to tWHZ + tDW to allow the DQ drivers to turn off and on the data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during the R/$\overline{W}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified tWP. For the $\overline{CE}$ controlled write cycle, $\overline{OE}$ may be LOW with no degregation to tcw timing.
7. DQOUT is never enabled, therefore the output is in High-Z state during the entire write cycle.
8. $\overline{CMD}$ access follows the standard $\overline{CE}$ access described above. If $\overline{CMD}$ = VIL, then $\overline{CE}$ must = VIH or, when $\overline{CE}$ = VIL, $\overline{CMD}$ must = VIH.

SEQUENTIAL PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[2]

Symbol	Parameter	IDT70824X20 COM'L ONLY		IDT70824X25 COM'L ONLY		IDT70824X35		IDT70824X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tCYC	Sequential Clock Cycle Time	25	—	30	—	40	—	50	—	ns
tCH	Clock Pulse HIGH	12	—	12	—	15	—	18	—	ns
tCL	Clock Pulse LOW	12	—	12	—	15	—	18	—	ns
tES	Count Enable and Address Pointer Set-up Time	5	—	5	—	6	—	6	—	ns
tEH	Count Enable and Address Pointer Hold Time	2	—	2	—	2	—	2	—	ns
tSOE	Output Enable to Data Valid	—	8	—	10	—	15	—	20	ns
tOLZ	Output Enable Low-Z Time[1]	2	—	2	—	2	—	2	—	ns
tOHZ	Output Enable High-Z Time[1]	—	9	—	11	—	15	—	15	ns
tCD	Clock to Valid Data	—	20	—	25	—	35	—	45	ns
tCKHZ	Clock High-Z Time[1]	—	12	—	14	—	17	—	20	ns
tCKLZ	Clock Low-Z Time[1]	3	—	3	—	3	—	3	—	ns
tEB	Clock to EOB	13	—	—	15	—	18	—	23	ns

NOTES:
3099 tbl 22

1. Transition measured at ±200mV from steady state. This parameter is guaranteed with the AC Test Load (Figure 2) by device characterization, but is not production tested.
2. "X" in part numbers indicates power rating (S or L).

SEQUENTIAL PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[1]

Symbol	Parameter	IDT70824X20 COM'L ONLY		IDT70824X25 COM'L ONLY		IDT70824X35		IDT70824X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tCYC	Sequential Clock Cycle Time	25	—	30	—	40	—	50	—	ns
tFS	Flow Restart Time	—	13	—	15	—	20	—	20	ns
tWS	Chip Select and Read/Write Set-up Time	5	—	5	—	6	—	6	—	ns
tWH	Chip Select and Read/Write Hold Time	2	—	2	—	2	—	2	—	ns
tDS	Input Data Set-up Time	5	—	5	—	6	—	6	—	ns
tDH	Input Data Hold Time	2	—	2	—	2	—	2	—	ns

NOTE:
3099 tbl 23

1. "X" in part numbers indicates power rating (S or L).

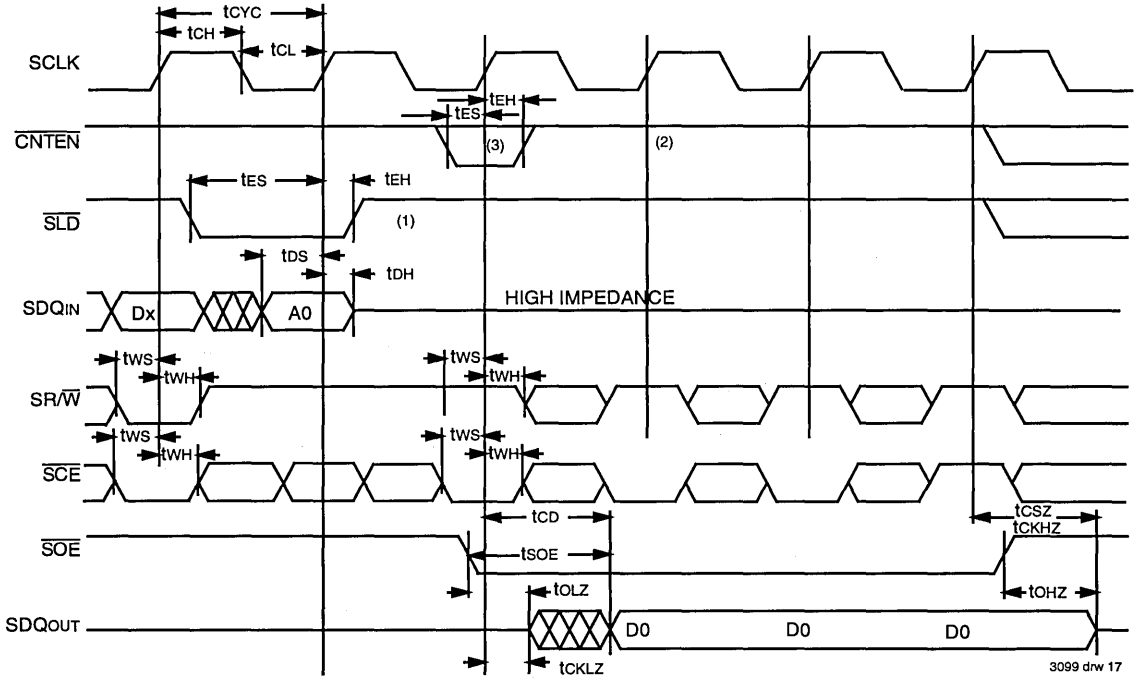
SEQUENTIAL PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[1]

Symbol	Parameter	IDT70824X20 COM'L ONLY Min.	IDT70824X20 COM'L ONLY Max.	IDT70824X25 COM'L ONLY Min.	IDT70824X25 COM'L ONLY Max.	IDT70824X35 Min.	IDT70824X35 Max.	IDT70824X45 Min.	IDT70824X45 Max.	Unit
RESET CYCLE										
tRSPW	Reset Pulse Width	13	—	15	—	20	—	20	—	ns
tWERS	Write Enable HIGH to Reset HIGH	10	—	10	—	10	—	10	—	ns
tRSRC	Reset HIGH to Write Enable LOW	10	—	10	—	10	—	10	—	ns
tRSFV	Reset HIGH to Flag Valid	15	—	20	—	25	—	25	—	ns

NOTE:
1. "X" in part numbers indicates power rating (S or L).

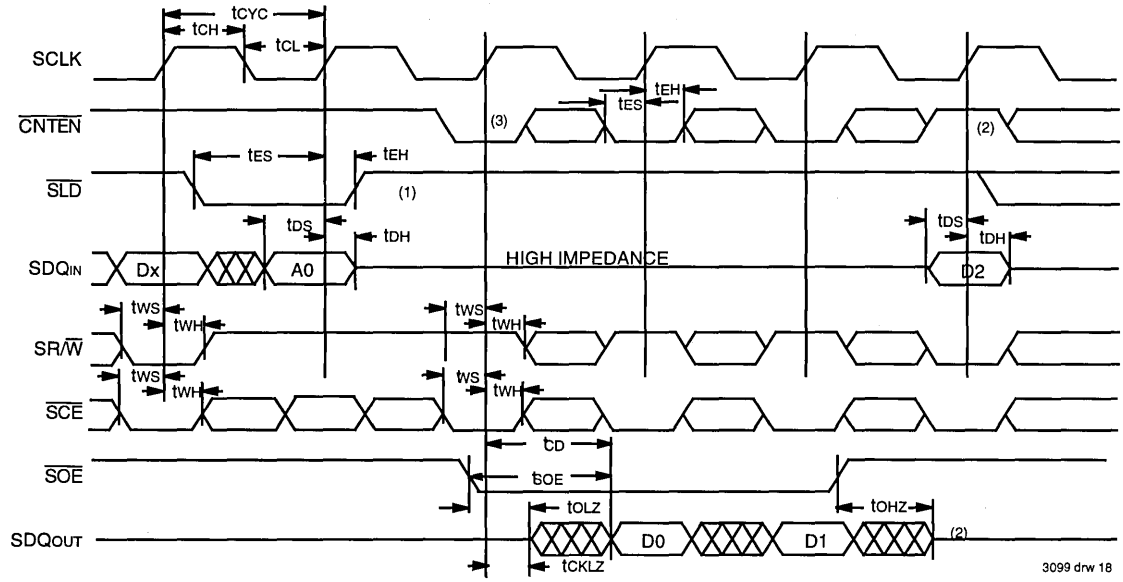
3099 tbl 24

SEQUENTIAL PORT: WRITE, POINTER LOAD NON-INCREMENTING READ



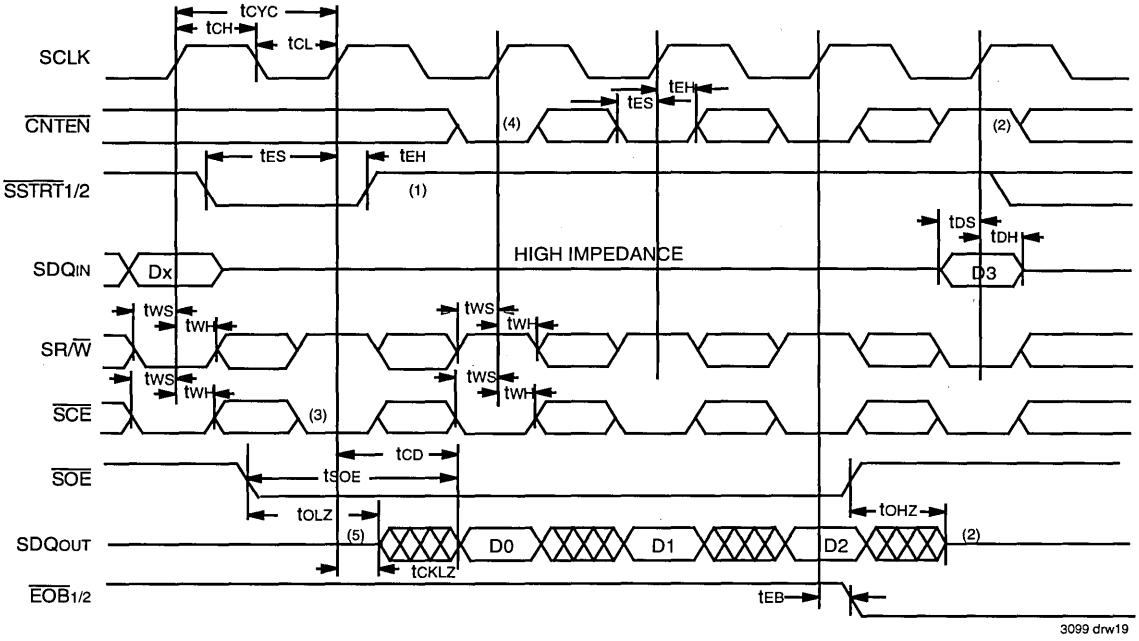
NOTE:
See notes in Figure "Sequential Port: Write, Pointer Load, Burst Read".

SEQUENTIAL PORT: WRITE, POINTER LOAD, BURST READ



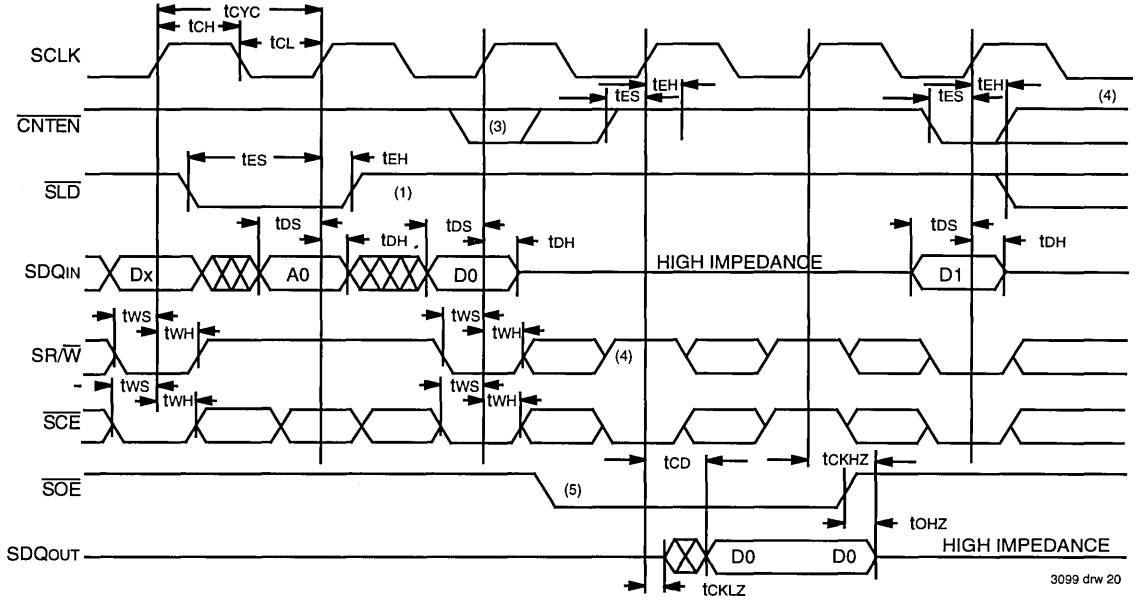
NOTES:
1. If $\overline{SLD}$ = VIL, then address will be clocked in on the SCLK's rising edge.
2. If $\overline{CNTEN}$ = VIH for the SCLK's rising edge, the internal address counter will not advance.
3. Pointer is not incremented on cycle immediately following $\overline{SLD}$ even if $\overline{CNTEN}$ is LOW.

READ STRT/EOB FLAG TIMING - SEQUENTIAL PORT

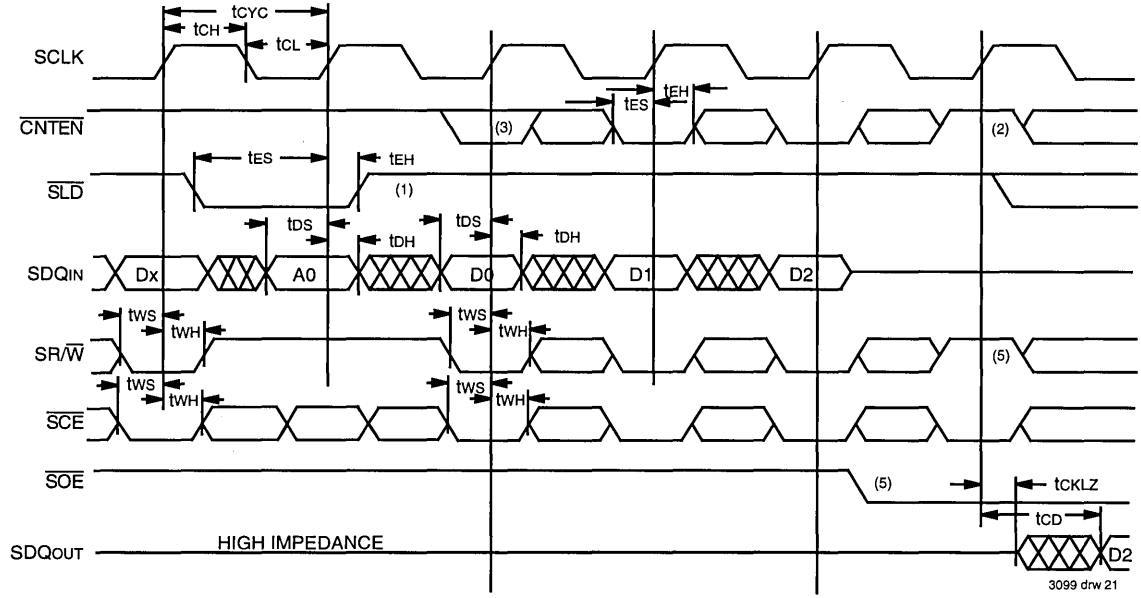


NOTES:
See notes in Figure "STRT/EOB Sequential Port Write Cycle".

WAVEFORM OF WRITE CYCLES: SEQUENTIAL PORT

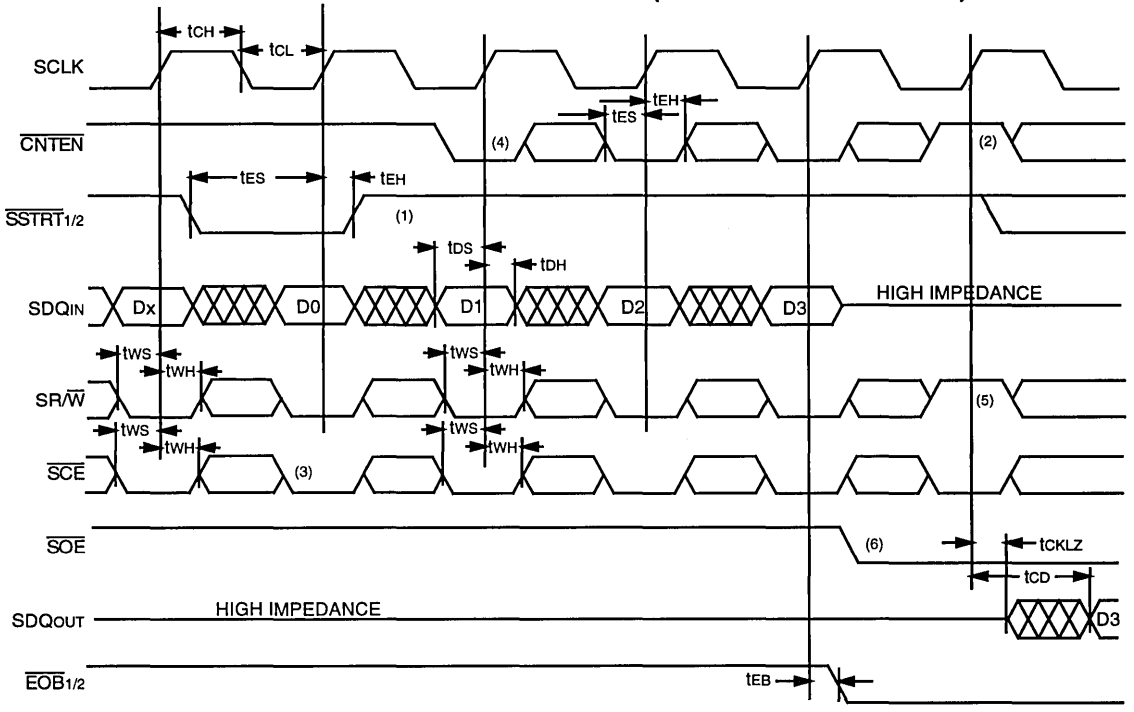


WAVEFORM OF BURST WRITE CYCLES: SEQUENTIAL PORT



NOTES :
1. If $\overline{SLD}$ = VIL, then address will be clocked in on the SCLK's rising edge.
2. If $\overline{CNTEN}$ = VIH for the SCLK's rising edge, the internal address counter will not advance.
3. Pointer is not incrementing on cycle immediately following $\overline{SLD}$ even if $\overline{CNTEN}$ is Low.
4. If SR/$\overline{W}$ = VIL, data would be written to D0 again since $\overline{CNTEN}$ = VIH.
5. $\overline{SOE}$ = VIL makes no difference at this point since the SR/$\overline{W}$ = VIL disables the output until SR/$\overline{W}$ = VIH is clocked in on the next rising clock edge.

WAVEFORM OF WRITE CYCLES: SEQUENTIAL PORT (STRT/EOB FLAG TIMING)

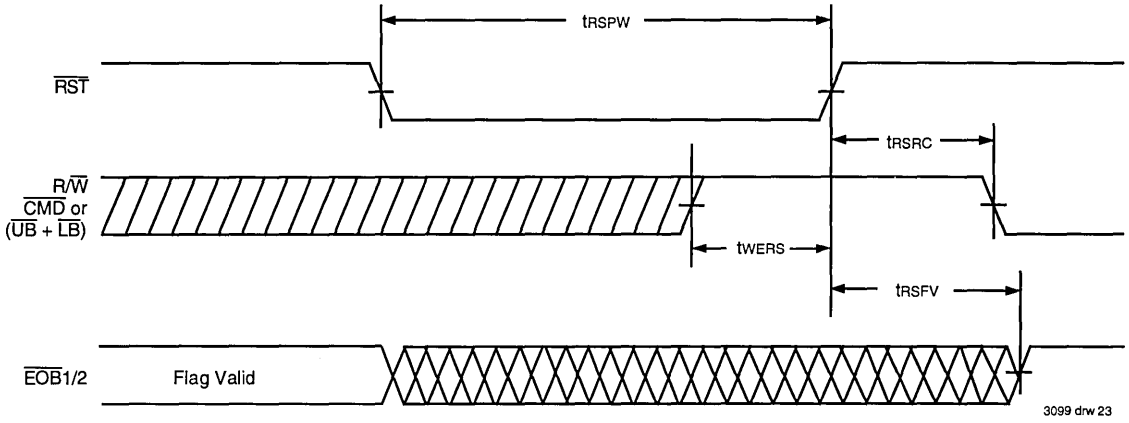


3099 drw 22

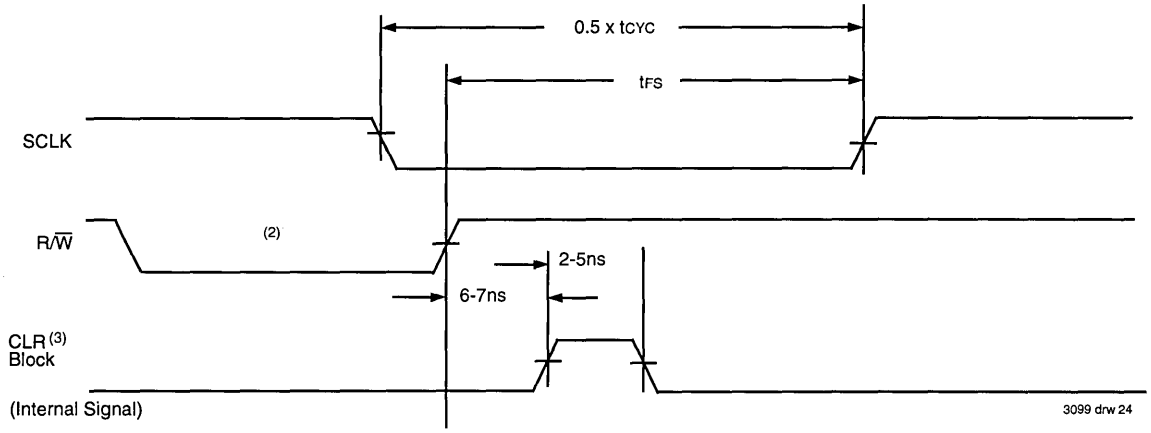
NOTES: (Also used in Figure "Read STRT/EOB Flag Timing")

1. If $\overline{SSTRT_1}$ or $\overline{SSTRT_2}$ = VIL, then address will be clocked in on the SCLK's rising edge.
2. If $\overline{CNTEN}$ = VIH for the SCLK's rising edge, the internal address counter will not advance.
3. $\overline{SOE}$ will control the output and should be High on Power-Up. If $\overline{SCE}$ = VIL and is clocked in while SR/$\overline{W}$ = VIH, the data addressed will be read out within that cycle. If $\overline{SCE}$ = VIL and is clocked in while SR/$\overline{W}$ = VIL, the data addressed will be written to if the last cycle was a Read. $\overline{SOE}$ may be used to control the bus contention and permit a Write on this cycle.
4. Unlike $\overline{SLD}$ case, $\overline{CNTEN}$ is not disabled on cycle immediately following $\overline{SSTRT}$.
5. If SR/$\overline{W}$ = VIL, data would be written to D0 again since $\overline{CNTEN}$ = VIH.
6. $\overline{SOE}$ = VIL makes no difference at this point since the SR/$\overline{W}$ = VIL disables the output until SR/$\overline{W}$ = VIH is clocked in on the next rising clock edge.

RANDOM ACCESS PORT - RESET TIMING

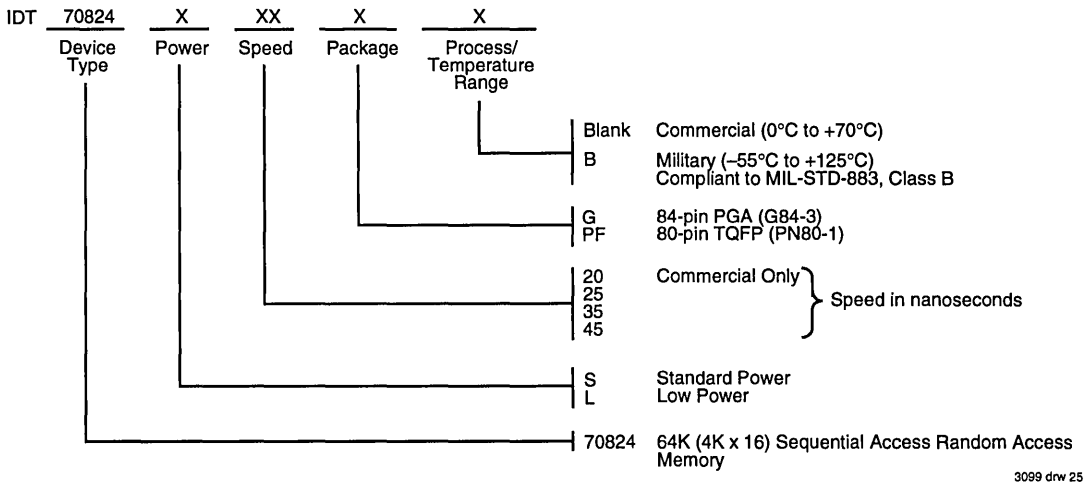


RANDOM ACCESS PORT RESTART TIMING OF SEQUENTIAL PORT (1)



NOTE:
1. The sequential port is in the STOP mode and is being restarted from the random port by the Bit 4 Counter Release (see Case 5).
2. "0" is written to Bit 4 from the random port at address [A2 - A0] = 100, when $\overline{CMD}$ = VIL and $\overline{CE}$ = VIH. The device is in the Buffer Command Mode (see Case 5).
3. CLR is an internal signal only and is shown for reference only.

ORDERING INFORMATION



Integrated Device Technology, Inc.

HIGH SPEED 128K (8K X 16 BIT) SEQUENTIAL ACCESS RANDOM ACCESS MEMORY (SARAM™)

IDT70825S/L

FEATURES:

- 8K x 16 Sequential Access Random Access Memory (SARAM™)
  - Sequential Access from one port and standard Random Access from the other port
  - Separate upper-byte and lower-byte control of the Random Access Port
- High-speed operation
  - 20ns t_{AA} for random access port
  - 20ns t_{CD} for sequential port
  - 25ns clock cycle time
- Architecture based on Dual-Port RAM cells
- Electrostatic discharge ≥ 2001V, Class II
- Compatible with Intel BMIC and 82430 PCI Set
- Width and Depth Expandable
- Sequential side
  - Address based flags for buffer control
  - Pointer logic supports two internal buffers
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Available in 80-pin TQFP and 84-pin PGA
- Military product compliant to MIL-STD-883.
- Industrial temperature range (–40°C to +85°C) is available, tested to military electrical specifications.

DESCRIPTION:

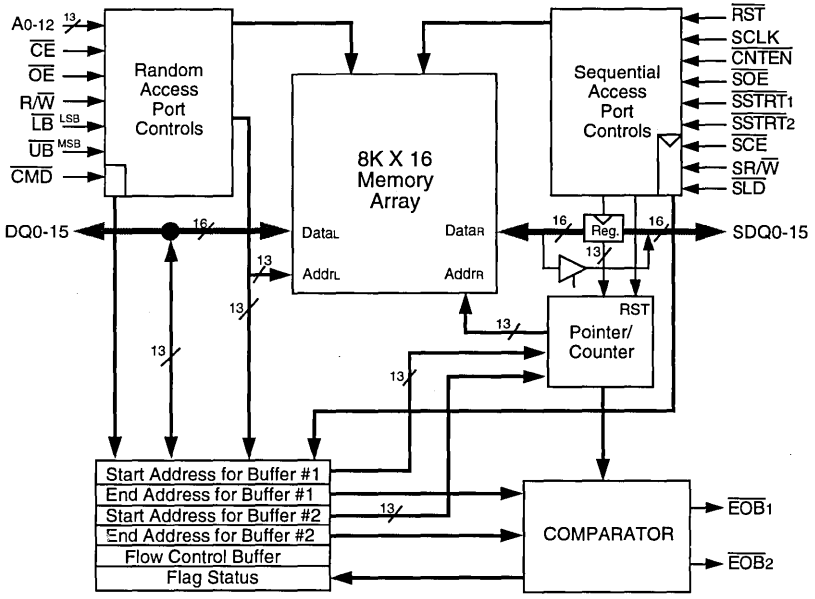
The IDT70825 is a high-speed 8K x 16bit Sequential Access Random Access Memory (SARAM). The SARAM offers a single-chip solution to buffer data sequentially on one port, and be accessed randomly (asynchronously) through the other port. The device has a Dual-Port RAM based architecture with a standard SRAM interface for the random (asynchronous) access port, and a clocked interface with counter sequencing for the sequential (synchronous) access port.

Fabricated using CMOS high-performance technology, this memory device typically operates on less than 900mW of power at maximum high-speed clock-to-data and Random Access. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70825 is packaged in a 80-pin Thin Plastic Quad Flatpack (TQFP) or 84-pin Ceramic Pin Grid Array (PGA). Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

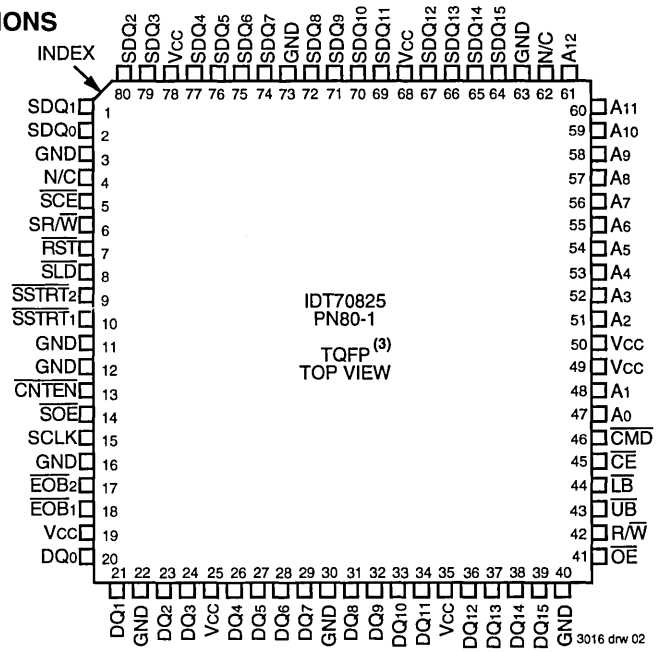
6

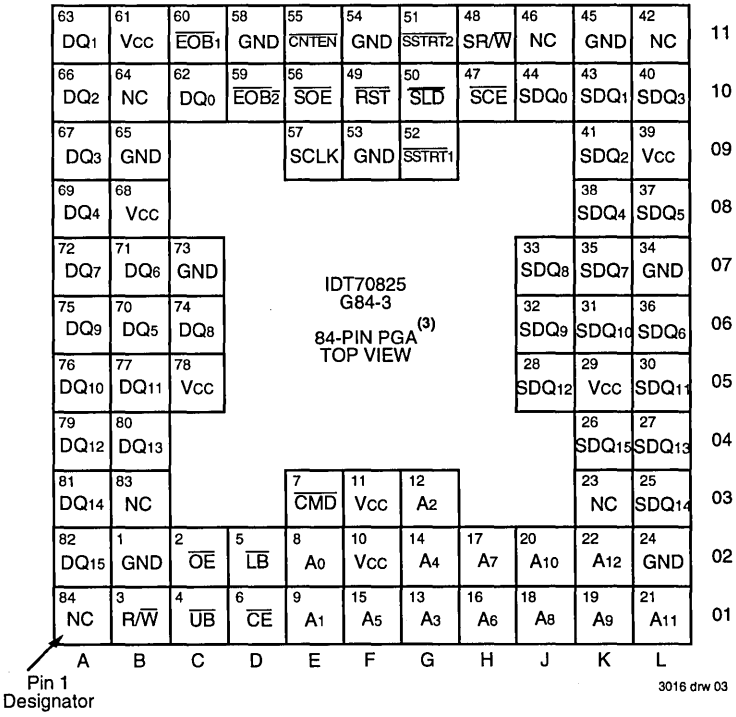
FUNCTIONAL BLOCK DIAGRAM



3016 drw 01

PIN CONFIGURATIONS





NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

PIN DESCRIPTIONS: RANDOM ACCESS PORT

SYMBOL	NAME	I/O	DESCRIPTION
A0-A12	Address Lines	I	Address inputs to access the 8192-word (16 bit) memory array.
DQ0-DQ15	Inputs/Outputs	I	Random access data inputs/outputs for 16-bit wide data.
$\overline{CE}$	Chip Enable	I	When $\overline{CE}$ is LOW, the random access port is enabled. When $\overline{CE}$ is HIGH, the random access port is disabled into power-down mode and the DQ outputs are in the high-impedance state. All data is retained during $\overline{CE}$ = VIH, unless it is altered by the sequential port. $\overline{CE}$ and $\overline{CMD}$ may not be LOW at the same time.
$\overline{CMD}$	Control Register Enable	I	When $\overline{CMD}$ is LOW, Address lines A0-A2, R/$\overline{W}$, and inputs/outputs DQ0-DQ12, are used to access the control register, the flag register, and the start and end of buffer registers. $\overline{CMD}$ and $\overline{CE}$ may not be LOW at the same time.
R/$\overline{W}$	Read/Write Enable	I	If $\overline{CE}$ is LOW and $\overline{CMD}$ is HIGH, data is written into the array when R/$\overline{W}$ is LOW and read out of the array when R/$\overline{W}$ is HIGH. If $\overline{CE}$ is HIGH and $\overline{CMD}$ is LOW, R/$\overline{W}$ is used to access the buffer command registers. $\overline{CE}$ and $\overline{CMD}$ may not be LOW at the same time.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW and R/$\overline{W}$ is HIGH, DQ0-DQ15 outputs are enabled. When $\overline{OE}$ is HIGH, the DQ outputs are in the high-impedance state.
$\overline{LB}$,$\overline{UB}$	Lower Byte, Upper Byte Enables	I	When $\overline{LB}$ is LOW, DQ0-DQ7 are accessible for read and write operations. When $\overline{LB}$ is HIGH, DQ0-DQ7 are tri-stated and blocked during read and write operations. $\overline{UB}$ controls access for DQ8-DQ15 in the same manner and is asynchronous from $\overline{LB}$.
VCC	Power Supply		Seven +5V power supply pins. All Vcc pins must be connected to the same +5V VCC supply.
GND	Ground		Nine Ground pins. All Ground pins must be connected to the same Ground supply.

3016 tbl 01

PIN DESCRIPTIONS: SEQUENTIAL ACCESS PORT

SYMBOL	NAME	I/O	DESCRIPTION
SDQ0-SDQ15	Inputs	I/O	Sequential data inputs/outputs for 16-bit wide data.
SCLK	Clock	I	SDQ0-SDQ15, $\overline{SCE}$, SR/$\overline{W}$, and $\overline{SLD}$ are registered on the LOW-to-HIGH transition of SCLK. Also, the sequential access port address pointer increments by 1 on each LOW-to-HIGH transition of SCLK when $\overline{CNTEN}$ is LOW.
$\overline{SCE}$	Chip Enable	I	When $\overline{SCE}$ is LOW, the sequential access port is enabled on the LOW-to-HIGH transition of SCLK. When $\overline{SCE}$ is HIGH, the sequential access port is disabled into powered-down mode on the LOW-to-HIGH transition of SCLK, and the SDQ outputs are in the high-impedance state. All data is retained, unless altered by the random access port.
$\overline{CNTEN}$	Counter Enable	I	When $\overline{CNTEN}$ is LOW, the address pointer increments on the LOW-to-HIGH transition of SCLK.
SR/$\overline{W}$	Read/Write Enable	I	When SR/$\overline{W}$ and SCE are LOW, a write cycle is initiated on the LOW-to-HIGH transition of SCLK. When SR/$\overline{W}$ is HIGH, and $\overline{SCE}$ and $\overline{SOE}$ are LOW, a read cycle is initiated on the LOW-to-HIGH transition of SCLK.
$\overline{SLD}$	Address Pointer Load Control	I	When $\overline{SLD}$ is sampled LOW, there is an internal delay of one cycle before the address pointer changes. When $\overline{SLD}$ is LOW, data on the inputs SDQ0-SDQ12 is loaded into a data-in register on the LOW-to-HIGH transition of SCLK. On the cycle following $\overline{SLD}$, the address pointer changes to the address location contained in the data-in register. $\overline{SSTRT1}$ and $\overline{SSTRT2}$ may not be LOW while $\overline{SLD}$ is LOW or during the cycle following $\overline{SLD}$.
$\overline{SSTRT1}$, $\overline{SSTRT2}$	Load Start of Address Register	I	When $\overline{SSTRT1}$ or $\overline{SSTRT2}$ is LOW, the start of address register #1 or #2 is loaded into the address pointer on the LOW-to-HIGH transition of SCLK. The start addresses are stored in internal registers. $\overline{SSTRT1}$ and $\overline{SSTRT2}$ may not be LOW while $\overline{SLD}$ is LOW or during the cycle following $\overline{SLD}$.
$\overline{EOB1}$, $\overline{EOB2}$	End of Buffer Flag	O	$\overline{EOB1}$ or $\overline{EOB2}$ is output LOW when the address pointer is incremented to match the address stored in the end of buffer registers. The flags can be cleared by either asserting $\overline{RST}$ LOW or by writing zero into bit 0 and/or bit 1 of the control register at address 101. $\overline{EOB1}$ and $\overline{EOB2}$ are dependent on separate internal registers, and therefore separate match addresses.
$\overline{SOE}$	Output Enable	I	$\overline{SOE}$ controls the data outputs and is independent of SCLK. When $\overline{SOE}$ is LOW, output buffers and the sequentially addressed data is output. When $\overline{SOE}$ is HIGH, the SDQ output bus is in the high-impedance state. $\overline{SOE}$ is asynchronous to SCLK.
$\overline{RST}$	Reset	I	When $\overline{RST}$ is LOW, all internal registers are set to their default state. The address pointer is set to zero and the $\overline{EOB1}$ and $\overline{EOB2}$ flags are set HIGH. $\overline{RST}$ is asynchronous to SCLK.

Note: "I/O" is bidirectional Input and Output. "I" is Input and "O" is Output.

3016 tbl 02

6

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

3016 tbl 03

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

3016 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0(2)	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

3016 tbl 05

NOTE:
1. VIL ≥ –1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 0.5V.

CAPACITANCE (TA = +25°C, F = 1.0MHz, TQFP only)

Symbol	Parameter(1)	Conditions(2)	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	9	pF
COUT	Output Capacitance	VOUT = 3dV	10	pF

3016 tbl 06

NOTE:
1. This parameter is determined by device characterization, but is not production tested.
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	IDT70825S		IDT70825L		Unit
			Min.	Max.	Min.	Max.	
|ILI|	Input Leakage Current	VCC = Max. VIN = GND to VCC	—	5.0	—	1.0	µA
|ILO|	Output Leakage Current	VCC = Max. $\overline{CE}$ and $\overline{SCE}$ = VIH VOUT = GND to VCC	—	5.0	—	1.0	µA
VOL	Output Low Voltage	IOL = 4mA, VCC = Min.	—	0.4	—	0.4	V
VOH	Output High Voltage	IOH = –4mA, VCC = Min.	2.4	—	2.4	—	V

3016 tbl 07

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		70825X20 COM'L ONLY Typ.[2]	70825X20 COM'L ONLY Max.	70825X25 COM'L ONLY Typ.[2]	70825X25 COM'L ONLY Max.	70825X35 Typ.[2]	70825X35 Max.	70825X45 Typ.[2]	70825X45 Max.	Unit
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = VIL, Outputs Open, $\overline{SCE}$ = VIL[5] f = fMAX[3]	MIL.	S	—	—	—	—	160	400	155	400	mA
				L	—	—	—	—	160	340	155	340	
			COM'L.	S	180	380	170	360	160	340	155	340	
				L	180	330	170	310	160	290	155	290	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{SCE}$ and $\overline{CE}$ ≥ VIH[7] $\overline{CMD}$ = VIH f = fMAX[3]	MIL.	S	—	—	—	—	20	85	16	85	mA
				L	—	—	—	—	20	65	16	65	
			COM'L.	S	25	70	25	70	20	70	16	70	
				L	25	50	25	50	20	50	16	50	
ISB2	Standby Current (One Port - TTL Level Input)	$\overline{CE}$ or $\overline{SCE}$ = VIH Active Port Outputs Open, f = fMAX[3]	MIL.	S	—	—	—	—	95	290	90	290	mA
				L		——	—	—	95	250	90	250	
			COM'L.	S	115	260	105	250	95	240	90	240	
				L	115	230	105	220	95	210	90	210	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}$ and $\overline{SCE}$ ≥ VCC - 0.2V[6,7] VIN ≥ VCC - 0.2V or VIN ≤ 0.2V, f = 0[4]	MIL.	S	—	—	—	—	1.0	30	1.0	30	mA
				L	—	—	—	—	0.2	10	0.2	10	
			COM'L.	S	1.0	15	1.0	15	1.0	15	1.0	15	
				L	0.2	5	0.2	5	0.2	5	0.2	5	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	One Port $\overline{CE}$ or $\overline{SCE}$ ≥ VCC - 0.2V[6] Outputs Open (Active port), f = fMAX[3] VIN ≥ VCC - 0.2V or VIN ≤ 0.2V	MIL.	S	—	—	—	—	90	260	85	260	mA
				L	—	—	—	—	90	215	85	215	
			COM'L.	S	110	240	100	230	90	220	85	220	
				L	110	200	100	190	90	180	85	180	

NOTES:
3016 tbl 08

1. 'X' in part number indicates power rating (S or L).
2. Vcc = 5V, Ta = +25°C; guaranteed by device characterization but not production tested.
3. At f = fMAX, address, control lines (except Output Enable), and SCLK are cycling at the maximum frequency read cycle of 1/tRC.
4. f = 0 means no address or control lines change.
5. $\overline{SCE}$ may transition, but is Low ($\overline{SCE}$=VIL) when clocked in by SCLK.
6. $\overline{SCE}$ may be ≤ 0.2V, after it is clocked in, since SCLK=VIH must be clocked in prior to powerdown.
7. If one port is enabled (either $\overline{CE}$ or $\overline{SCE}$ = Low) then the other port is disabled (SCE or CE = High, respectively). CMOS High ≥ Vcc - 0.2V and Low ≤ 0.2V, and TTL High = VIH and Low = VIL.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES (L VERSION ONLY) (V_{LC} ≤ 0.2V, V_{HC} ≥ VCC - 0.2V)

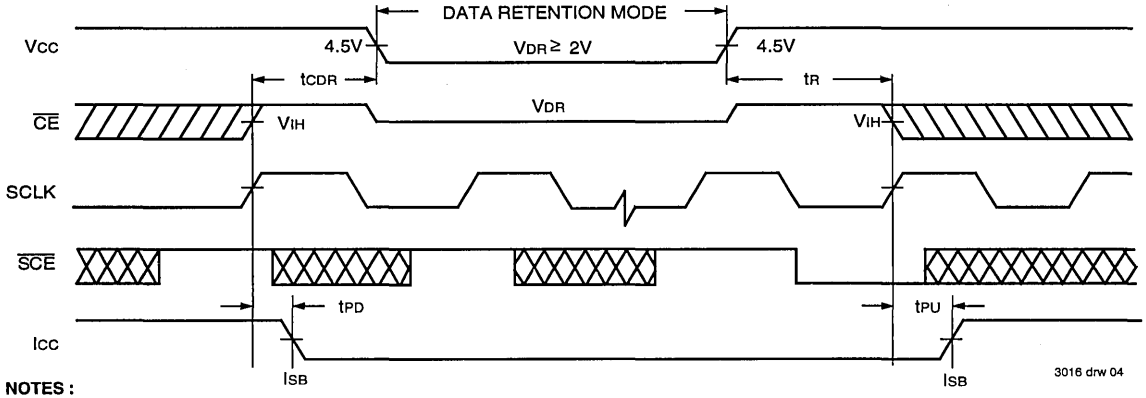
Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
VDR	VCC for Data Retention	VCC = 2V		2.0	—	—	V
ICCDR	Data Retention Current	$\overline{CE}$ = VHC	MIL.	—	100	4000	µA
		VIN = VHC or = VLC	COM'L.	—	100	1500	
tCDR[3]	Chip Deselect to Data Retention Time	$\overline{SCE}$ = VHC[4] when SCLK= ↓		0	—	—	ns
tR[3]	Operation Recovery Time	$\overline{CMD}$ = VHC		tRC[2]	—	—	ns

NOTES :
3016 tbl 09

1. TA = +25°C, Vcc = 2V; guaranteed by device characterization but not production tested.
2. tRC = Read Cycle Time
3. This parameter is guaranteed by device characterization, but is not production tested.
4. To initiate data retention, $\overline{SCE}$ = VIH must be clocked in.

6

DATA RETENTION AND POWER DOWN/UP WAVEFORM (RANDOM AND SEQUENTIAL PORT)[1,2]



NOTES :
1. $\overline{SCE}$ is synchronized to the sequential clock input.
2. $\overline{CMD}$ ≥ Vcc - 0.2V.

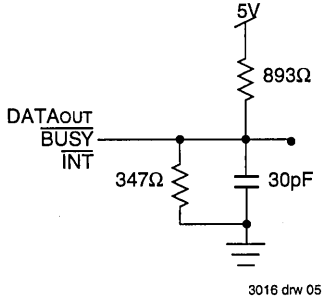


Figure 1. AC Output Test Load

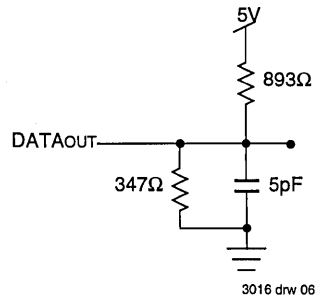


Figure 2. Output Test Load (for tCLZ, tBLZ, tOLZ, tCHZ, tBHZ, tOHZ, tWHZ, tCKHZ, and tCKLZ)
Including scope and jig.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 & 2

3016 tbl 10

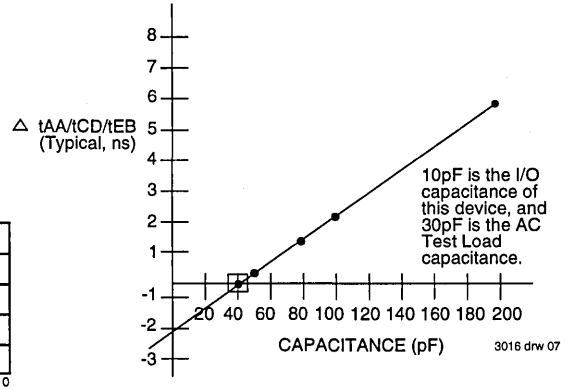


Figure 1A. Lumped Capacitance Load Typical Derating Curve

TRUTH TABLE: RANDOM ACCESS READ AND WRITE (1,2)

Inputs/Outputs								MODE
$\overline{CE}$	$\overline{CMD}$	R/$\overline{W}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	DQ0-DQ7	DQ8-DQ15	
L	H	H	L	L	L	DATAOUT	DATAOUT	Read both Bytes.
L	H	H	L	L	H	DATAOUT	High-Z	Read lower Byte only.
L	H	H	L	H	L	High-Z	DATAOUT	Read upper Byte only.
L	H	L	H(3)	L	L	DATAIN	DATAIN	Write to both Bytes.
L	H	L	H(3)	L	H	DATAIN	High-Z	Write to lower Byte only.
L	H	L	H(3)	H	L	High-Z	DATAIN	Write to upper Byte only.
H	H	X	X	X	X	High-Z	High-Z	Both Bytes deselected and powered down.
L	H	H	H	X	X	High-Z	High-Z	Outputs disabled but not powered down.
L	H	X	X	H	H	High-Z	High-Z	Both Bytes deselected but not powered down.
H	L	L	H(3)	L(4)	L(4)	DATAIN	DATAIN	Write DQ0-DQ12 to the Buffer Command Register.
H	L	H	L	L(4)	L(4)	DATAOUT	DATAOUT	Read contents of the Buffer Command Register via DQ0-DQ12.

3016 tbl 11

NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't Care, and High-Z = High-impedance.
2. $\overline{RST}$, $\overline{SCE}$, $\overline{CNTEN}$, SR/$\overline{W}$, $\overline{SLD}$, $\overline{SSTRT1}$, $\overline{SSTRT2}$, SCLK, SDQ0-SDQ15, $\overline{EOB1}$, $\overline{EOB2}$, and $\overline{SOE}$ are unrelated to the random access port control and operation.
3. If $\overline{OE}$ = V_{IL} during write, t_{WHZ} must be added to the t_{WP} or t_{CW} write pulse width to allow the bus to float prior to being driven.
4. Byte operations to control register using $\overline{UB}$ and $\overline{LB}$ separately are also allowed.

TRUTH TABLE: SEQUENTIAL READ (1,2,3,4,5)

Inputs/Outputs								MODE
SCLK	$\overline{SCE}$	$\overline{CNTEN}$	SR/$\overline{W}$	$\overline{EOB1}$	$\overline{EOB2}$	$\overline{SOE}$	SDQ	
↓	L	L	H	LOW	LAST	L	[EOB1]	Counter Advanced Sequential Read with $\overline{EOB1}$ reached.
↓	L	H	H	LAST	LAST	L	[EOB1 - 1]	Non-Counter Advanced Sequential Read, without $\overline{EOB1}$ reached.
↓	L	L	H	LAST	LOW	L	[EOB2]	Counter Advanced Sequential Read with $\overline{EOB2}$ reached.
↓	L	H	H	LAST	LAST	L	[EOB2 - 1]	Non-Counter Advanced Sequential Read without $\overline{EOB2}$ reached.
↓	L	L	H	LOW	LOW	H	HIGH-Z	Counter Advanced Sequential Non-Read with $\overline{EOB1}$ and $\overline{EOB2}$ reached.

3016 tbl 12

NOTES:
1. H = V_{IH}, L = V_{IL}, X = Don't Care, High-Z = High impedance, and Low = V_{OL}.
2. $\overline{RST}$, $\overline{SLD}$, $\overline{SSTRT1}$, $\overline{SSTRT2}$ are continuously HIGH during sequential access, other than pointer access operations.
3. '[X]' refers to the contents of address 'X'.
4. $\overline{CE}$, $\overline{OE}$, R/$\overline{W}$, $\overline{CMD}$, $\overline{LB}$, $\overline{UB}$, and DQ0-DQ15 are unrelated to the sequential port control and operation except for $\overline{CMD}$ which must not be used concurrently with the sequential port operation (due to the counter and register control). $\overline{CMD}$ should be HIGH ($\overline{CMD}$ = V_{IH}) during sequential port access.
5. "LAST" refers to the previous value still being output, no change.

TRUTH TABLE: SEQUENTIAL WRITE (1,2,3,4,5,6)

Inputs/Outputs								MODE
SCLK	$\overline{SCE}$	$\overline{CNTEN}$	SR/$\overline{W}$	$\overline{EOB1}$	$\overline{EOB2}$	$\overline{SOE}$	SDQ	
↓	L	H	L	LAST	LAST	H	SDQIN	Non-Counter Advanced Sequential Write, without $\overline{EOB1}$ or $\overline{EOB2}$ reached
↓	L	L	L	LOW	LOW	H	SDQIN	Counter Advanced Sequential Write with $\overline{EOB1}$ and $\overline{EOB2}$ reached.
↓	H	X	X	LAST	LAST	X	High-Z	No Write or Read due to Sequential port Deselect.

3016 tbl 13

NOTES:
1. H = V_{IH}, L = V_{IL}, X = Don't Care, and High-Z = High-impedance. LOW = V_{OL}.
2. $\overline{RST}$, $\overline{SLD}$, $\overline{SSTRT1}$, $\overline{SSTRT2}$ are continuously HIGH during a sequential write access, other than pointer access operations.
3. $\overline{CE}$, $\overline{OE}$, R/$\overline{W}$, $\overline{CMD}$, $\overline{LB}$, $\overline{UB}$, and DQ0-DQ15 are unrelated to the sequential port control and operation except for $\overline{CMD}$ which must not be used concurrently with the sequential port operation (due to the counter and register control). $\overline{CMD}$ should be HIGH ($\overline{CMD}$ = V_{IH}) during sequential port access.
4. $\overline{SOE}$ must be HIGH ($\overline{SOE}$=V_{IH}) prior to write conditions only if the previous cycle is a read cycle, since the data being written must be an input at the rising edge of the clock during the cycle in which SR/$\overline{W}$ = V_{IL}.
5. SDQ_{IN} refers to SDQ0-SDQ15 inputs.
6. "LAST" refers to the previous value still being output, no change.

TRUTH TABLE: SEQUENTIAL ADDRESS POINTER OPERATIONS (1,2,3,4,5)

Inputs/Outputs					
SCLK	$\overline{SLD}$	$\overline{SSTRT1}$	$\overline{SSTRT2}$	$\overline{SOE}$	MODE
↑	H	L	H	X	Start address for Buffer #1 loaded into Address Pointer.
↑	H	H	L	X	Start address for Buffer #2 loaded into Address Pointer.
↑	L	H	H	H(6)	Data on SDQ0-SDQ12 loaded into Address Pointer .

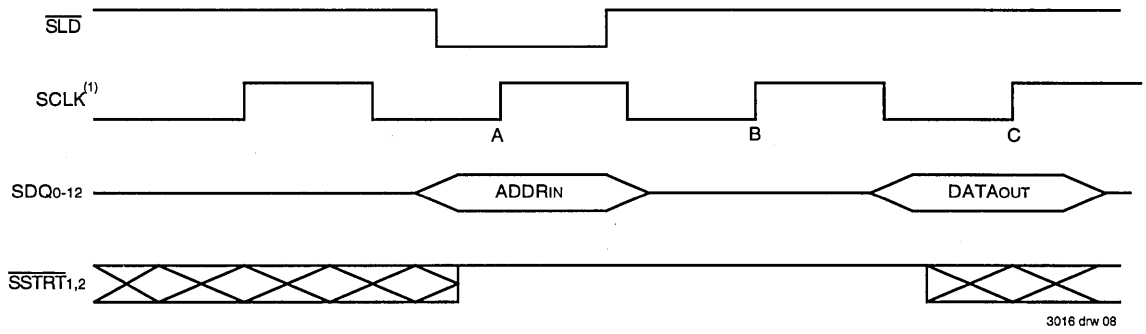
3016 tbl 14

NOTES:
1. H = V_{IH}, L = V_{IL}, X = Don't Care, and High-Z = High-impedance.
2. $\overline{RST}$ is continuously HIGH. The conditions of $\overline{SCE}$, $\overline{CNTEN}$, and SR/$\overline{W}$ are unrelated to the sequential address pointer operations.
3. $\overline{CE}$, $\overline{OE}$, R/$\overline{W}$, $\overline{LB}$, $\overline{UB}$, and DQ_0-DQ_{15} are unrelated to the sequential port control and operation, except for $\overline{CMD}$ which must not be used concurrently with the sequential port operation (due to the counter and register control). $\overline{CMD}$ should be HIGH (CMD = V_{IH}) during sequential port access.
4. Address pointer can also change when it reaches an end of buffer address. See Flow Control Bits table.
5. When $\overline{SLD}$ is sampled LOW, there is an internal delay of one cycle before the address pointer changes. The state of $\overline{CNTEN}$ is ignored and the address is not incremented during the two cycles.
6. $\overline{SOE}$ may be LOW with $\overline{SCE}$ deselect or in the write mode using SR/$\overline{W}$.

ADDRESS POINTER LOAD CONTROL (SLD)

In $\overline{SLD}$ mode, there is an internal delay of one cycle before the address pointer changes in the cycle following $\overline{SLD}$. When $\overline{SLD}$ is LOW, data on the inputs SDQ_0-SDQ_{12} is loaded into a data-in register on the LOW-to-HIGH transition of $\overline{SCLK}$. On the cycle following $\overline{SLD}$, the address pointer changes to the address location contained in the data-in register. $\overline{SSTRT1}$, $\overline{SSTRT2}$ may not be low while $\overline{SLD}$ is LOW, or during the cycle following $\overline{SLD}$. The $\overline{SSTRT1}$ and $\overline{SSTRT2}$ require only one clock cycle, since these addresses are pre-loaded in the registers already.

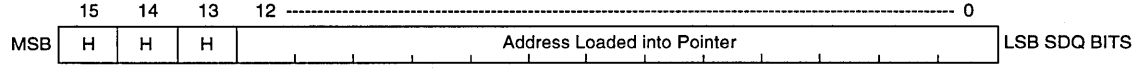
$\overline{SLD}$ MODE (1)



3016 drw 08

NOTE:
1. At SCLK edge (A), SDQ0-SDQ12 data is loaded into a data-in register. At edge (B), contents of the data-in register are loaded into the address pointer (i.e. address pointer changes). At SCLK edge (A), $\overline{SSTRT1}$ and $\overline{SSTRT2}$ must be high to ensure for proper sequential address pointer loading. At SCLK edge (B), $\overline{SLD}$ and $\overline{SSTRT1,2}$ must be high to ensure for proper sequential address pointer loading. For $\overline{SSTRT1}$ or $\overline{SSTRT2}$, the data to be read will be ready for edge (B), while data will not be ready at edge (B) when $\overline{SLD}$ is used, but will be ready at edge (C).

SEQUENTIAL LOAD OF ADDRESS INTO POINTER/COUNTER (1)



3016 drw 09

NOTE:
1. "H" = V_{IH} for the SDQ intput state.

Reset ($\overline{RST}$)

Setting $\overline{RST}$ LOW resets the control state of the SARAM. $\overline{RST}$ functions asynchronously of SCLK, (i.e. not registered). The default states after a reset operation are as follows:

Register	Contents
Address Pointer	0
EOB Flags	Cleared to High state
Buffer Flow Mode	BUFFER CHAINING
Start Address Buffer #1	0 (1)
End Address Buffer #1	4095 (4K)
Start Address Buffer #2	4096 (4K+1)
End Address Buffer #2	8191 (8K)
Registered State	$\overline{SCE}$ = VIH, SR/$\overline{W}$ = VIL

3016 tbl 15

BUFFER COMMAND MODE ($\overline{CMD}$)

Buffer Command Mode ($\overline{CMD}$) allows the random access port to control the state of the two buffers. Address pins A_0-A_2 and I/O pins DQ_0-DQ_{12} are used to access the start of buffer and the end of buffer addresses and to set the flow control mode of each buffer. The Buffer Command Mode also allows reading and clearing the status of the EOB flags. Seven different CMD cases are available depending on the conditions of A_0-A_2 and R/W. Address bits A_3-A_{12} and data I/O bits DQ_{13}-DQ_{15} are not used during this operation.

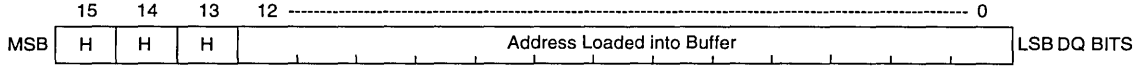
RANDOM ACCESS PORT $\overline{CMD}$ MODE(1)

Case #	A2-A0	R/$\overline{W}$	DESCRIPTIONS
1	000	0 (1)	Write (read) the start address of Buffer #1 through DQ_0-DQ_{12}.
2	001	0 (1)	Write (read) the end address of Buffer #1 through DQ_0-DQ_{12}.
3	010	0 (1)	Write (read) the start address of Buffer #2 through DQ_0-DQ_{12}.
4	011	0 (1)	Write (read) the end address of Buffer #2 through DQ_0-DQ_{12}.
5	100	0 (1)	Write (read) flow control register
6	101	0	Write only – clear EOB1 and/or EOB2 flag
7	101	1	Read only – flag status register
8	110/111	(X)	(Reserved)

NOTES:
1. R/$\overline{W}$ input "0(1)" indicates a write(0) or read(1) occurring with the same address input.

3016 tbl 16

CASES 1 THROUGH 4: START AND END OF BUFFER REGISTER DESCRIPTION(1,2)



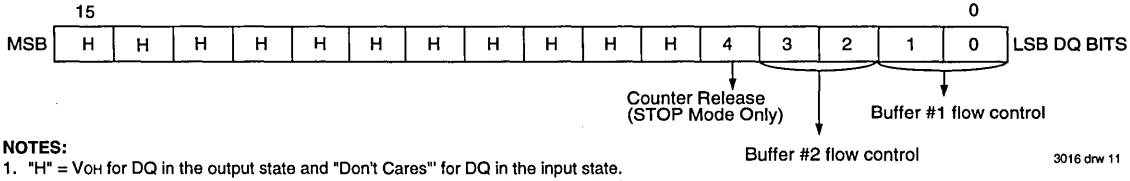
NOTES:
1. "H" = VOH for DQ in the output state and "Don't Cares" for DQ in the input state.
2. A write into the buffer occurs when R/$\overline{W}$ = VIL and a read when R/$\overline{W}$ = VIH. $\overline{EOB1}$/$\overline{SOB1}$ and $\overline{EOB2}$/$\overline{SOB2}$ are chosen through address A0-A2 while $\overline{CMD}$ = VIL and $\overline{CE}$ = VIH.

3016 drw 10

CASE 5: BUFFER FLOW MODES

Within the SARAM, the user can designate one of four buffer flow modes for each buffer. Each buffer flow mode defines a unique set of actions for the sequential port address pointer and EOB flags. In BUFFER CHAINING mode, after the address pointer reaches the end of the buffer, it sets the corresponding EOB flag and continues from the start address of the other buffer. In STOP mode, the address pointer stops incrementing after it reaches the end of the buffer. In LINEAR mode, the address pointer ignores the end of buffer address and increments past it, but sets the EOB flag. MASK mode is the same as LINEAR mode except EOB flags are not set.

FLOW CONTROL REGISTER DESCRIPTION[1,2]



3016 drw 11

NOTES:
1. "H" = V_{OH} for DQ in the output state and "Don't Cares"' for DQ in the input state.
2. Writing a 0 into bit 4 releases the address pointer after it is stopped due to the STOP mode and allows sequential write operations to resume. This occurs asynchronously of SCLK, and therefore caution should be taken. The pointer will be at address EOB+2 on the next rising edge of SCLK that is enabled by $\overline{CNTEN}$. The pointer is also released by $\overline{RST}$, $\overline{SLD}$, $\overline{SSTRT1}$ and $\overline{SSTRT2}$ operations.

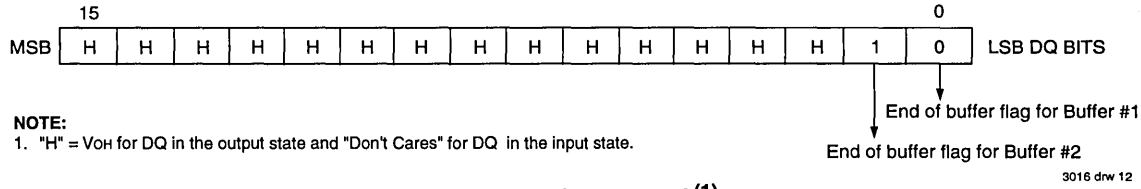
FLOW CONTROL BITS

Flow Control Bits		Functional Description
Bit 1 & Bit 0 (Bit 3 & Bit 2)	Mode	
00	BUFFER CHAINING	$\overline{EOB1}$ ($\overline{EOB2}$) is asserted (Active Low output) when the pointer matches the end address of Buffer #1 (Buffer #2). The pointer value is changed to the start address of Buffer #2 (Buffer #1).[1,3]
01	STOP	$\overline{EOB1}$ ($\overline{EOB2}$) is asserted when the pointer matches the end address of Buffer #1 (Buffer #2). The address pointer will stop incrementing when it reaches the next address ($\overline{EOB}$ address + 1), if $\overline{CNTEN}$ is Low on the next clock's rising edge. Otherwise, the address pointer will stop incrementing on $\overline{EOB}$. Sequential write operations are inhibited after the address pointer is stopped. The pointer can be released by bit 4 of the flow control register. [1,2,4]
10	LINEAR	$\overline{EOB1}$ ($\overline{EOB2}$) is asserted when the pointer matches the end address of Buffer #1 (Buffer #2). The pointer keeps incrementing for further operations.[1]
11	MASK	$\overline{EOB1}$ ($\overline{EOB2}$) is not asserted when the pointer reaches the end address of Buffer #1 (Buffer #2), although the flag status bits will be set. The pointer keeps incrementing for further operations.

3016 tbl 17

NOTES:
1. $\overline{EOB1}$ and $\overline{EOB2}$ may be asserted (set) at the same time, if both end addresses have been loaded with the same value.
2. $\overline{CMD}$ Flow Control bits are unchanged, the count does not continue advancement.
3. If $\overline{EOB1}$ and $\overline{EOB2}$ are equal, then the pointer will jump to the start of Buffer #1.
4. If counter has stopped at EOBx and was released by bit 4 of the flow control register, $\overline{CNTEN}$ must be LOW on the next rising edge of SCLK otherwise the flow control will remain in the STOP mode.

CASES 6 AND 7: FLAG STATUS REGISTER BIT DESCRIPTION[1]



3016 drw 12

NOTE:
1. "H" = V_{OH} for DQ in the output state and "Don't Cares" for DQ in the input state.

CASES 6: FLAG STATUS REGISTER WRITE CONDITIONS[1]

Flag Status Bit 0, (Bit 1)	Functional Description
0	Clears Buffer Flag $\overline{EOB1}$, ($\overline{EOB2}$).
1	No change to the Buffer Flag.[2]

3016 tbl 18

NOTE:
1. Either bit 0 or bit 1, or both bits, may be changed simultaneously. One may be cleared while the second is left alone or cleared.
2. Remains as it was prior to the $\overline{CMD}$ operation, either HIGH (1) or LOW (0).

CASE 7: FLAG STATUS REGISTER READ CONDITIONS

Flag Status Bit 0, (Bit 1)	Functional Description
0	$\overline{EOB1}$ ($\overline{EOB2}$) flag has not been set, the Pointer has not reached the End of the Buffer.
1	$\overline{EOB1}$ ($\overline{EOB2}$) flag has been set, the Pointer has reached the End of the Buffer.

3016 tbl 19

CASES 8 AND 9: (RESERVED)

Illegal operations. All outputs will be HIGH on the DQ bus during a READ.

RANDOM ACCESS PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (2,3)

Symbol	Parameter	IDT70825X20 COM'L ONLY		IDT70825X25 COM'L ONLY		IDT70825X35		IDT70825X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tRC	Read Cycle Time	20	—	25	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	35	—	45	ns
tACE	Chip Enable Access Time	—	20	—	25	—	35	—	45	ns
tBE	Byte Enable Access Time	—	20	—	25	—	35	—	45	ns
tOE	Output Enable Access Time	—	10	—	10	—	15	—	20	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
tCLZ	Chip Select Low-Z Time(1)	3	—	3	—	3	—	3	—	ns
tBLZ	Byte Enable Low-Z Time(1)	3	—	3	—	3	—	3	—	ns
tOLZ	Output Enable Low-Z Time(1)	2	—	2	—	2	—	2	—	ns
tCHZ	Chip Select High-Z Time(1)	—	10	—	12	—	15	—	15	ns
tBHZ	Byte Enable High-Z Time(1)	—	10	—	12	—	15	—	15	ns
tOHZ	Output Enable High-Z Time(1)	—	9	—	11	—	15	—	15	ns
tPU	Chip Select Power-Up Time	0	—	0	—	0	—	0	—	ns
tPD	Chip Select Power-Down Time	—	20	—	25	—	35	—	45	ns

NOTES: 3016 tbl 20

1. Transition measured at ±200mV from steady state. This parameter is guaranteed with the AC Test Load (Figure 2) by device characterization, but is not production tested.
2. "X" in part number indicates power rating (S or L).
3. $\overline{CMD}$ access follows standard timing listed for both read and write accesses, ($\overline{CE}$ = VIH when $\overline{CMD}$ = VIL) or ($\overline{CMD}$ = VIH when $\overline{CE}$ = VIL).

RANDOM ACCESS PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (2,4)

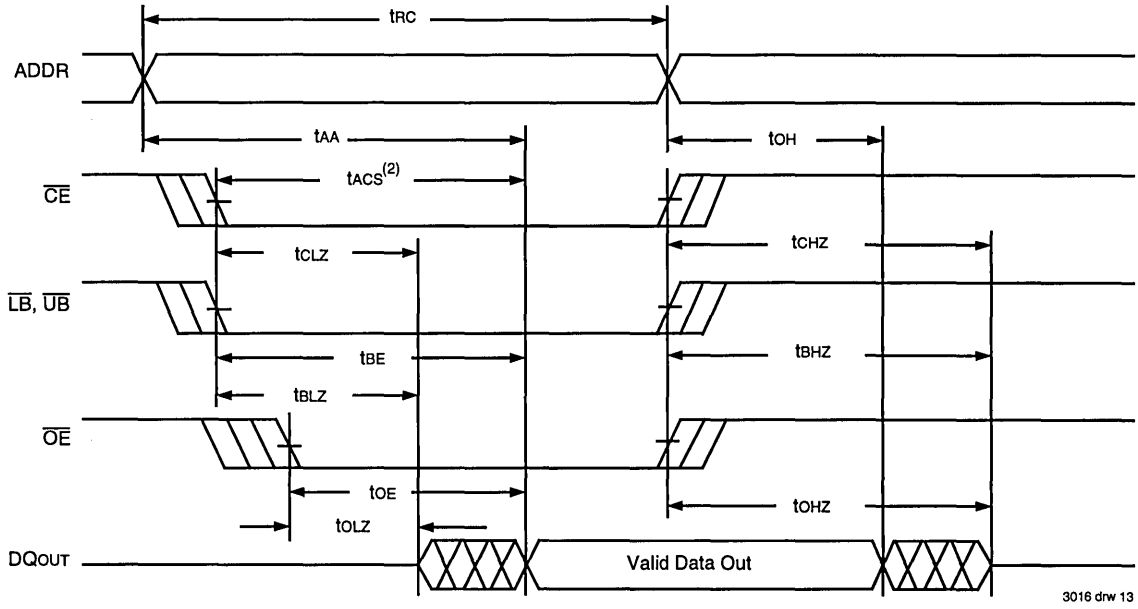
Symbol	Parameter	IDT70825X20 COM'L ONLY		IDT70825X25 COM'L ONLY		IDT70825X35		IDT70825X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tWC	Write Cycle Time	20	—	25	—	35	—	45	—	ns
tCW	Chip Select to End-of-Write	15	—	20	—	25	—	30	—	ns
tAW	Address Valid to End-of-Write(3)	15	—	20	—	25	—	30	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width(3)	13	—	20	—	25	—	30	—	ns
tBP	Byte Enable Pulse Width(3)	15	—	20	—	25	—	30	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable Output High-Z Time(1)	—	10	—	12	—	15	—	15	ns
tDW	Data Set-up Time	13	—	15	—	20	—	25	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End-of-Write	3	—	3	—	3	—	3	—	ns

NOTES: 3016 tbl 21

1. Transition measured at ±200mV from steady state. This parameter is guaranteed with the AC Test Load (Figure 2) by device characterization, but is not production tested.
2. "X" in part number indicates power rating (S or L).
3. $\overline{OE}$ is continuously HIGH, $\overline{OE}$ = VIH. If during the R/$\overline{W}$ controlled write cycle the $\overline{OE}$ is LOW, tWP must be greater or equal to tWHZ + tDW to allow the DQ drivers to turn off and on the data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during the R/$\overline{W}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified tWP. For the $\overline{CE}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to tCW timing.
4. $\overline{CMD}$ access follows standard timing listed for both read and write accesses, ($\overline{CE}$ = VIH when $\overline{CMD}$ = VIL) or ($\overline{CMD}$ = VIH when $\overline{CE}$ = VIL).

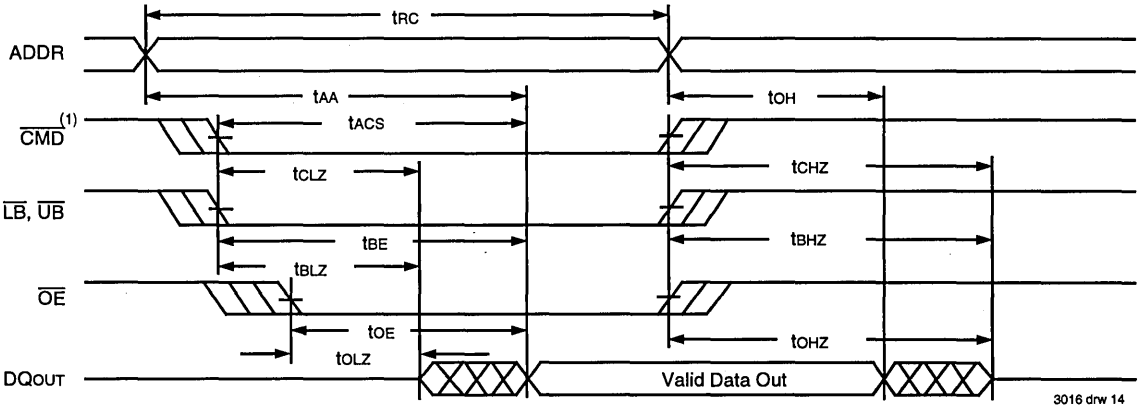
6

WAVEFORM OF READ CYCLES: RANDOM ACCESS PORT[1,2]



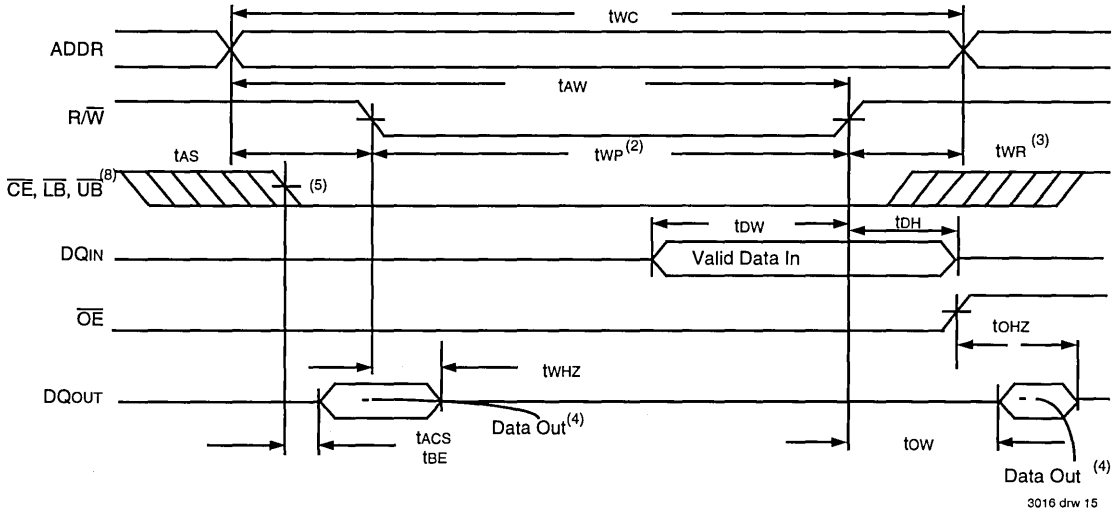
NOTES:
1. R/$\overline{W}$ is HIGH for Read cycle.
2. Address valid prior to or coincident with $\overline{CE}$ transition LOW; otherwise t_{AA} is the limiting parameter.

WAVEFORM OF READ CYCLES: BUFFER COMMAND MODE

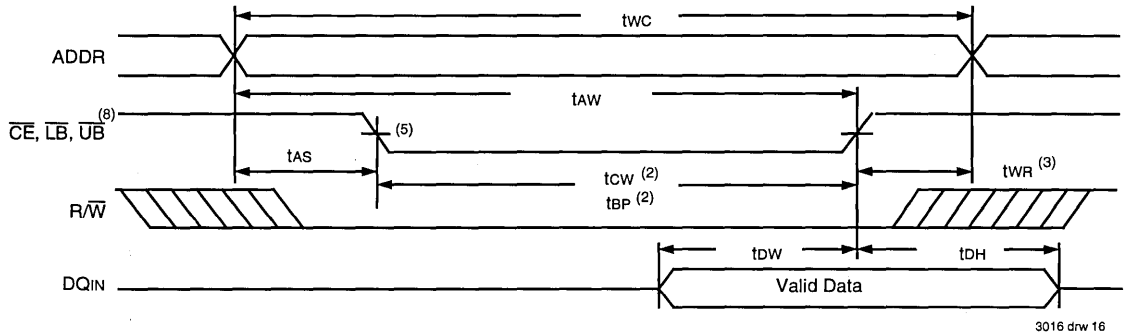


NOTES:
1. $\overline{CE}$ = V_{IH} when $\overline{CMD}$ = V_{IL}.

WAVEFORM OF WRITE CYCLE NO.1 (R/$\overline{W}$ CONTROLLED TIMING) RANDOM ACCESS PORT[1,6]



WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CE}$, $\overline{LB}$, AND/OR $\overline{UB}$ CONTROLLED TIMING) RANDOM ACCESS PORT[1,6,7]



NOTES:
1. R/$\overline{W}$, $\overline{CE}$, or $\overline{LB}$ and $\overline{UB}$ must be inactive during all address transitions.
2. A write occurs during the overlap of R/$\overline{W}$ = VIL, $\overline{CE}$ = VIL and $\overline{LB}$ = VIL and/or $\overline{UB}$ = VIL.
3. tWR is measured from the earlier of $\overline{CE}$ (and $\overline{LB}$ and/or $\overline{UB}$) or R/$\overline{W}$ going HIGH to the end of the write cycle.
4. During this period, DQ pins are in the output state and the input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.
6. $\overline{OE}$ is continuously HIGH, $\overline{OE}$ = VIH. If during the R/$\overline{W}$ controlled write cycle the $\overline{OE}$ is LOW, tWP must be greater or equal to tWHZ + tDW to allow the DQ drivers to turn off and on the data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during the R/$\overline{W}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified tWP. For the $\overline{CE}$ controlled write cycle, $\overline{OE}$ may be LOW with no degregation to tcw timing.
7. DQOUT is never enabled, therefore the output is in High-Z state during the entire write cycle.
8. $\overline{CMD}$ access follows the standard $\overline{CE}$ access described above. If $\overline{CMD}$ = VIL, then $\overline{CE}$ must = VIH or, when $\overline{CE}$ = VIL, $\overline{CMD}$ must = VIH.

SEQUENTIAL PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[2]

Symbol	Parameter	IDT70825X20 COM'L ONLY		IDT70825X25 COM'L ONLY		IDT70825X35		IDT70825X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
tCYC	Sequential Clock Cycle Time	25	—	30	—	40	—	50	—	ns
tCH	Clock Pulse HIGH	12	—	12	—	15	—	18	—	ns
tCL	Clock Pulse LOW	12	—	12	—	15	—	18	—	ns
tES	Count Enable and Address Pointer Set-up Time	5	—	5	—	6	—	6	—	ns
tEH	Count Enable and Address Pointer Hold Time	2	—	2	—	2	—	2	—	ns
tSOE	Output Enable to Data Valid	—	8	—	10	—	15	—	20	ns
tOLZ	Output Enable Low-Z Time[1]	2	—	2	—	2	—	2	—	ns
tOHZ	Output Enable High-Z Time[1]	—	9	—	11	—	15	—	15	ns
tCD	Clock to Valid Data	—	20	—	25	—	35	—	45	ns
tCKHZ	Clock High-Z Time[1]	—	12	—	14	—	17	—	20	ns
tCKLZ	Clock Low-Z Time[1]	3	—	3	—	3	—	3	—	ns
tEB	Clock to EOB	13	—	—	15	—	18	—	23	ns

NOTES: 3016 tbl 22
1. Transition measured at ±200mV from steady state. This parameter is guaranteed with the AC Test Load (Figure 2) by device characterization, but is not production tested.
2. "X" in part numbers indicates power rating (S or L).

SEQUENTIAL PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[1]

Symbol	Parameter	IDT70825X20 COM'L ONLY		IDT70825X25 COM'L ONLY		IDT70825X35		IDT70825X45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
tCYC	Sequential Clock Cycle Time	25	—	30	—	40	—	50	—	ns
tFS	Flow Restart Time	—	13	—	15	—	20	—	20	ns
tWS	Chip Select and Read/Write Set-up Time	5	—	5	—	6	—	6	—	ns
tWH	Chip Select and Read/Write Hold Time	2	—	2	—	2	—	2	—	ns
tDS	Input Data Set-up Time	5	—	5	—	6	—	6	—	ns
tDH	Input Data Hold Time	2	—	2	—	2	—	2	—	ns

NOTE:
1. "X" in part numbers indicates power rating (S or L). 3016 tbl 23

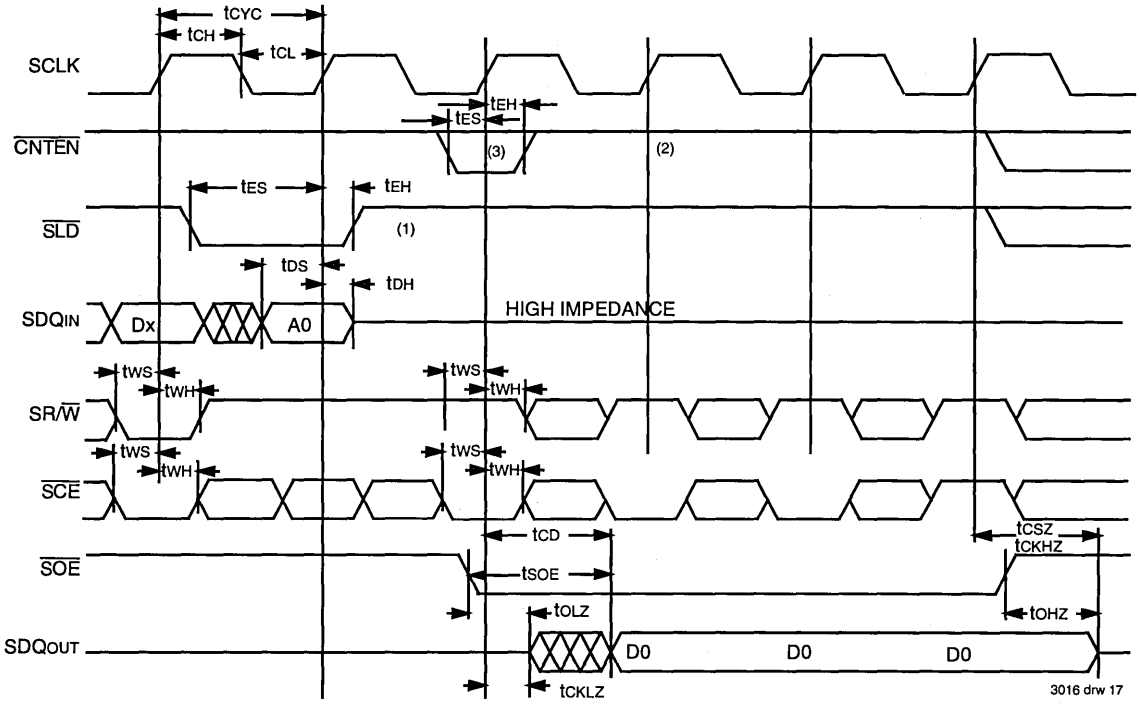
SEQUENTIAL PORT: AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[1]

Symbol	Parameter	IDT70825X20 COM'L ONLY Min.	IDT70825X20 COM'L ONLY Max.	IDT70825X25 COM'L ONLY Min.	IDT70825X25 COM'L ONLY Max.	IDT70825X35 Min.	IDT70825X35 Max.	IDT70825X45 Min.	IDT70825X45 Max.	Unit
RESET CYCLE										
tRSPW	Reset Pulse Width	13	—	15	—	20	—	20	—	ns
tWERS	Write Enable HIGH to Reset HIGH	10	—	10	—	10	—	10	—	ns
tRSRC	Reset HIGH to Write Enable LOW	10	—	10	—	10	—	10	—	ns
tRSFV	Reset HIGH to Flag Valid	15	—	20	—	25	—	25	—	ns

NOTE:
1. "X" in part numbers indicates power rating (S or L).

3016 tbl 24

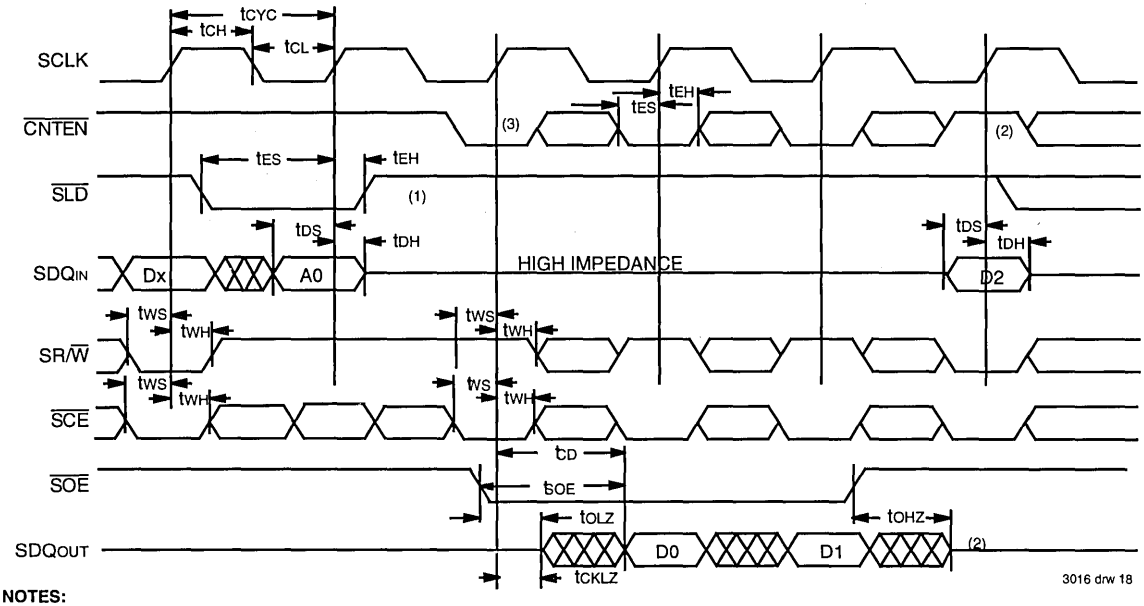
SEQUENTIAL PORT: WRITE, POINTER LOAD NON-INCREMENTING READ



3016 drw 17

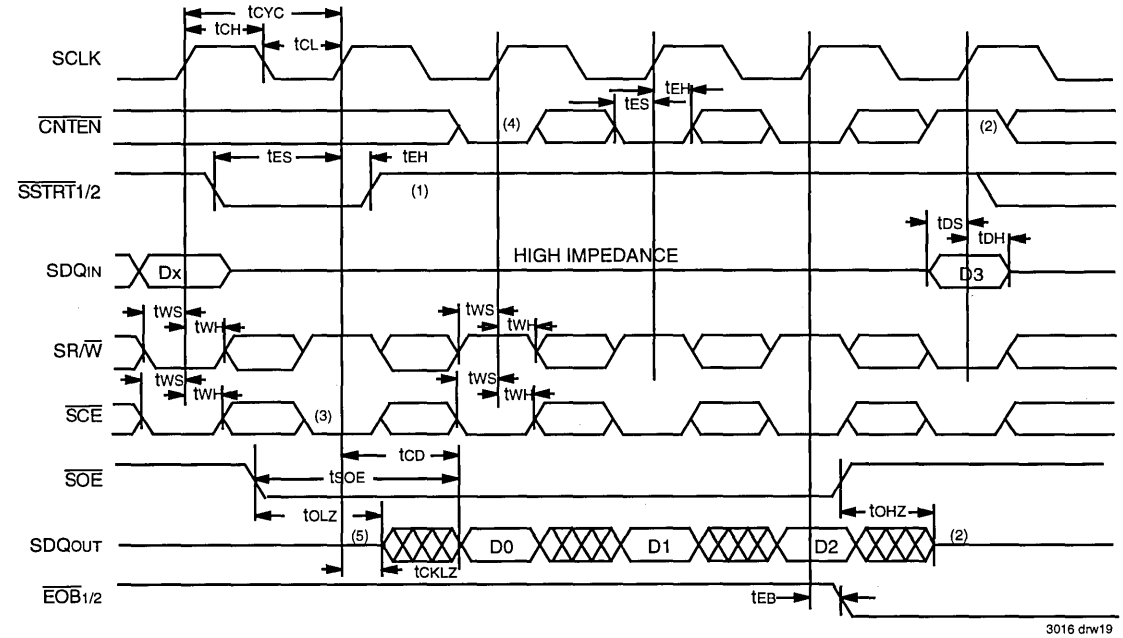
NOTE:
See notes in Figure "Sequential Port: Write, Pointer Load, Burst Read".

SEQUENTIAL PORT: WRITE, POINTER LOAD, BURST READ



NOTES:
1. If $\overline{SLD}$ = VIL, then address will be clocked in on the SCLK's rising edge.
2. If $\overline{CNTEN}$ = VIH for the SCLK's rising edge, the internal address counter will not advance.
3. Pointer is not incremented on cycle immediately following $\overline{SLD}$ even if $\overline{CNTEN}$ is LOW.

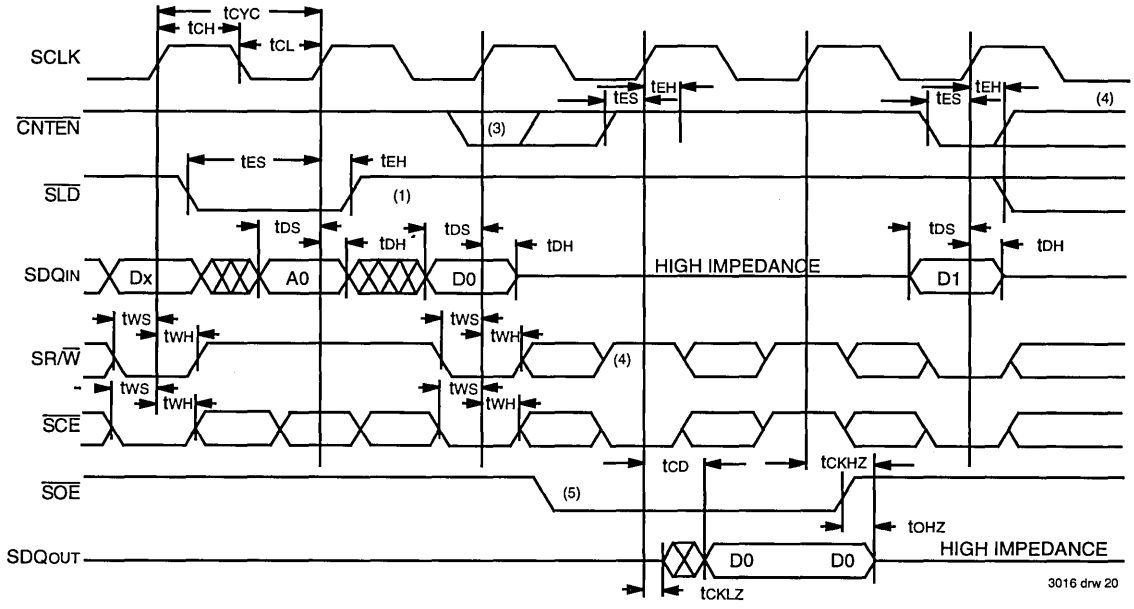
READ STRT/EOB FLAG TIMING - SEQUENTIAL PORT



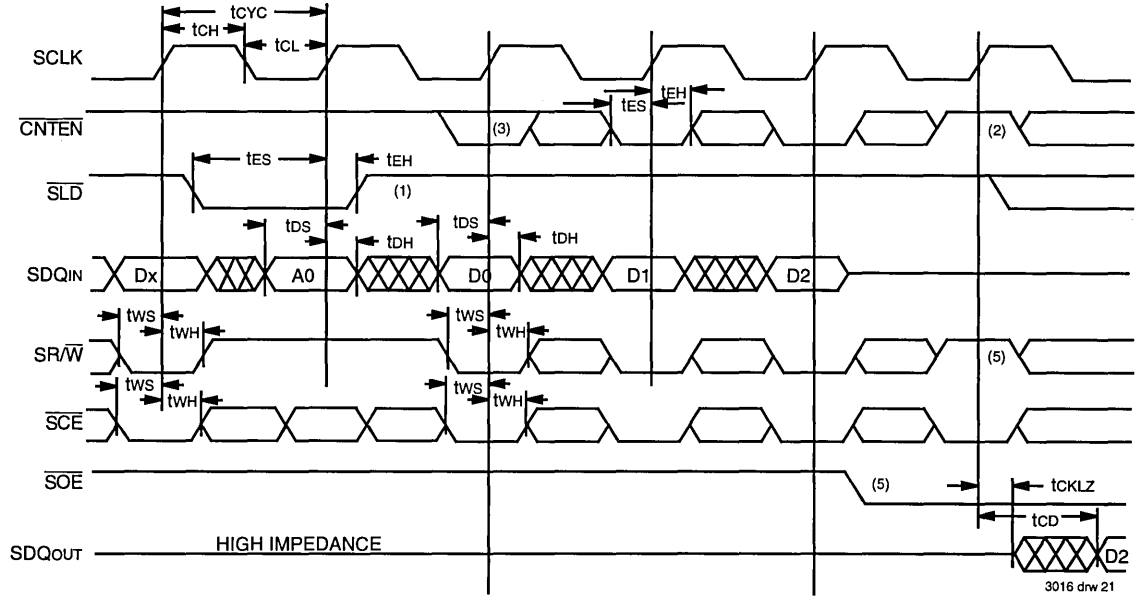
NOTES:

See notes in Figure "STRT/EOB Sequential Port Write Cycle".

WAVEFORM OF WRITE CYCLES: SEQUENTIAL PORT

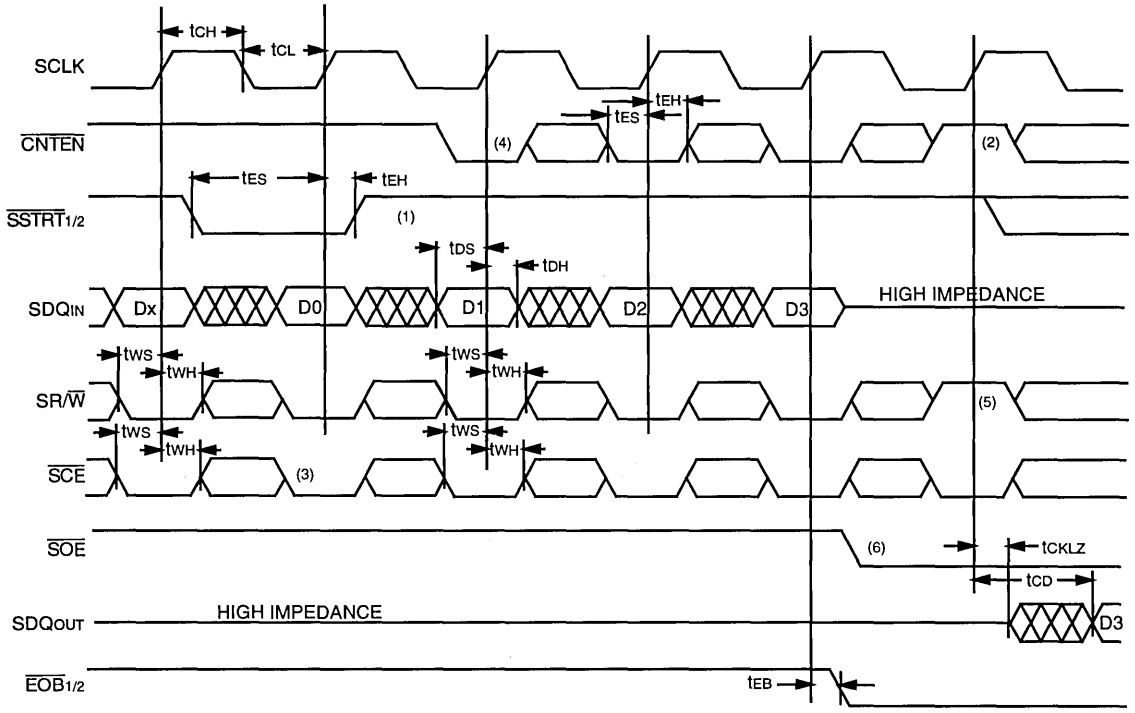


WAVEFORM OF BURST WRITE CYCLES: SEQUENTIAL PORT



NOTES :
1. If $\overline{SLD}$ = VIL, then address will be clocked in on the SCLK's rising edge.
2. If $\overline{CNTEN}$ = VIH for the SCLK's rising edge, the internal address counter will not advance.
3. Pointer is not incrementing on cycle immediately following $\overline{SLD}$ even if $\overline{CNTEN}$ is Low.
4. If SR/$\overline{W}$ = VIL, data would be written to D0 again since $\overline{CNTEN}$ = VIH.
5. $\overline{SOE}$ = VIL makes no difference at this point since the SR/$\overline{W}$ = VIL disables the output until SR/$\overline{W}$ = VIH is clocked in on the next rising clock edge.

WAVEFORM OF WRITE CYCLES: SEQUENTIAL PORT (STRT/EOB FLAG TIMING)

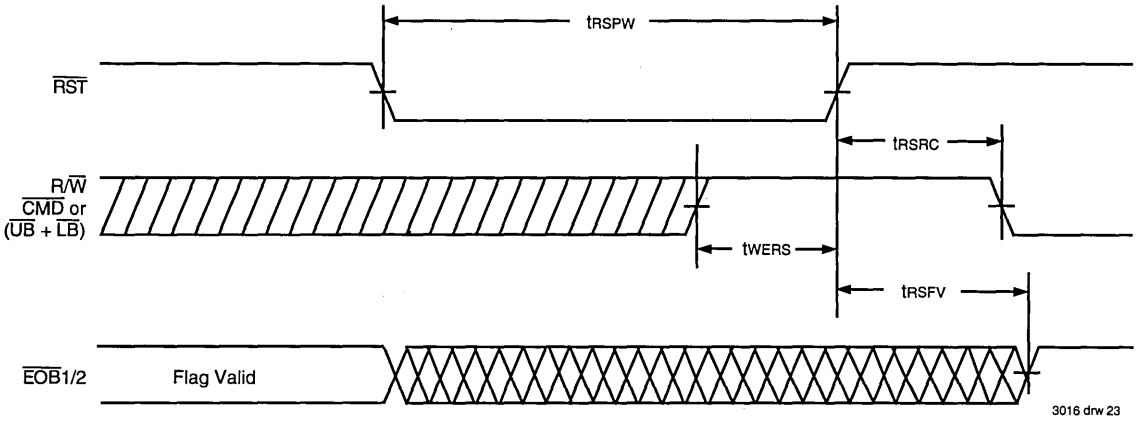


3016 drw 22

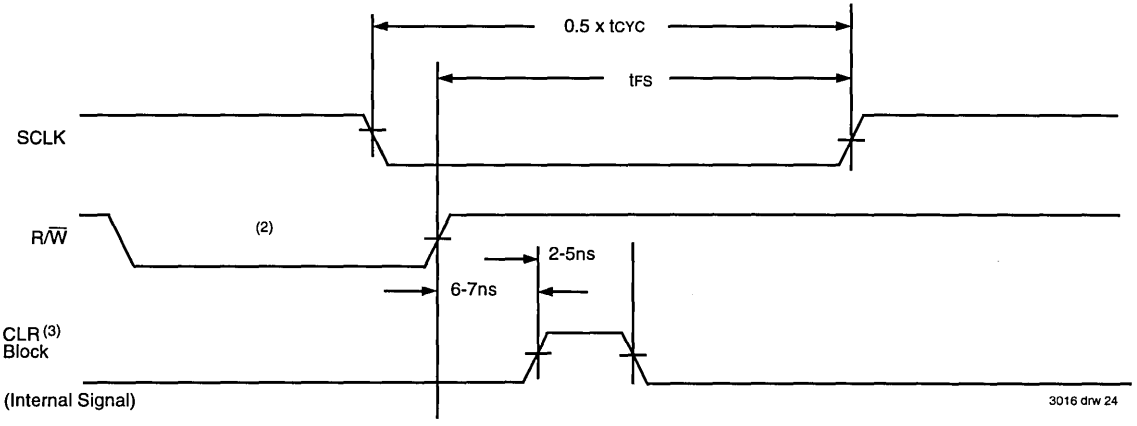
NOTES: (Also used in the Figure "Read STRT/EOB Flag Timing")

1. If $\overline{SSTRT_1}$ or $\overline{SSTRT_2}$ = VIL, then address will be clocked in on the SCLK's rising edge.
2. If $\overline{CNTEN}$ = VIH for the SCLK's rising edge, the internal address counter will not advance.
3. $\overline{SOE}$ will control the output and should be High on Power-Up. If $\overline{SCE}$ = VIL and is clocked in while SR/$\overline{W}$ = VIH, the data addressed will be read out within that cycle. If $\overline{SCE}$ = VIL and is clocked in while SR/$\overline{W}$ = VIL, the data addressed will be written to if the last cycle was a Read. $\overline{SOE}$ may be used to control the bus contention and permit a Write on this cycle.
4. Unlike $\overline{SLD}$ case, $\overline{CNTEN}$ is not disabled on cycle immediately following $\overline{SSTRT}$.
5. If SR/$\overline{W}$ = VIL, data would be written to D0 again since $\overline{CNTEN}$ = VIH.
6. $\overline{SOE}$ = VIL makes no difference at this point since the SR/$\overline{W}$ = VIL disables the output until SR/$\overline{W}$ = VIH is clocked in on the next rising clock edge.

RANDOM ACCESS PORT - RESET TIMING

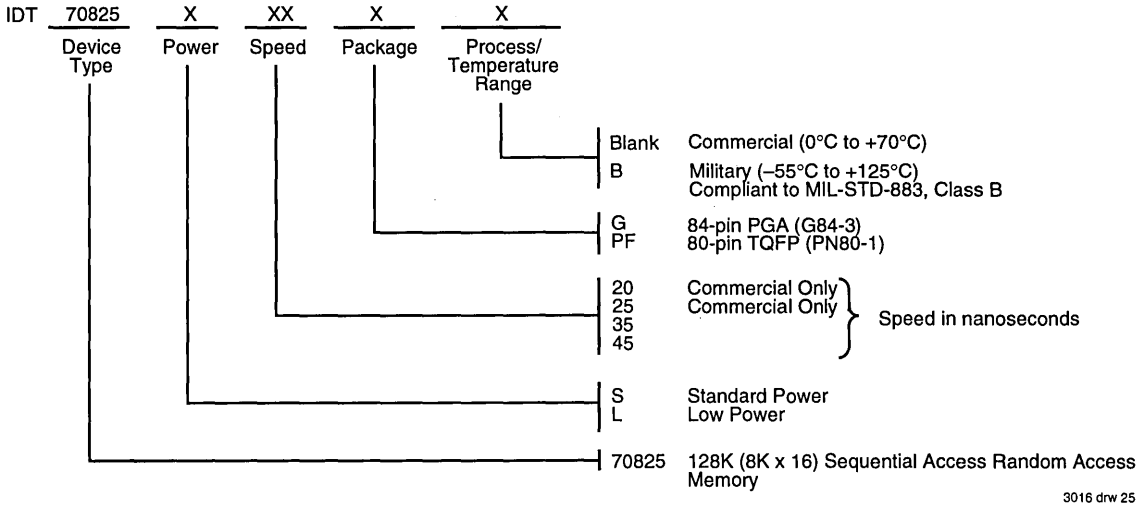


RANDOM ACCESS PORT RESTART TIMING OF SEQUENTIAL PORT (1)



NOTE:
1. The sequential port is in the STOP mode and is being restarted from the random port by the Bit 4 Counter Release (see Case 5).
2. "0" is written to Bit 4 from the random port at address [A2 - A0] = 100, when $\overline{CMD}$ = VIL and $\overline{CE}$ = VIH. The device is in the Buffer Command Mode (see Case 5).
3. CLR is an internal signal only and is shown for reference only.

ORDERING INFORMATION



3016 drw 25

Integrated Device Technology, Inc.

CMOS DUAL-PORT RAM 3.3V, 16K (2K x 8-BIT) WITH INTERRUPTS

PRELIMINARY
IDT71V321S/L

FEATURES:

- High-speed access
  - —Commercial: 25/35/55ns (max.)
- Low-power operation
  - —IDT71V321S
    - Active: 250mW (typ.)
    - Standby: 3.3mW (typ.)
  - —IDT71V321L
    - Active: 250mW (typ.)
    - Standby: 660µW (typ.)
- Two $\overline{INT}$ flags for port-to-port communications
- On-chip port arbitration logic
- $\overline{BUSY}$ output flag
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 3.3V ±0.3V power supply
- Available in popular plastic packages

DESCRIPTION:

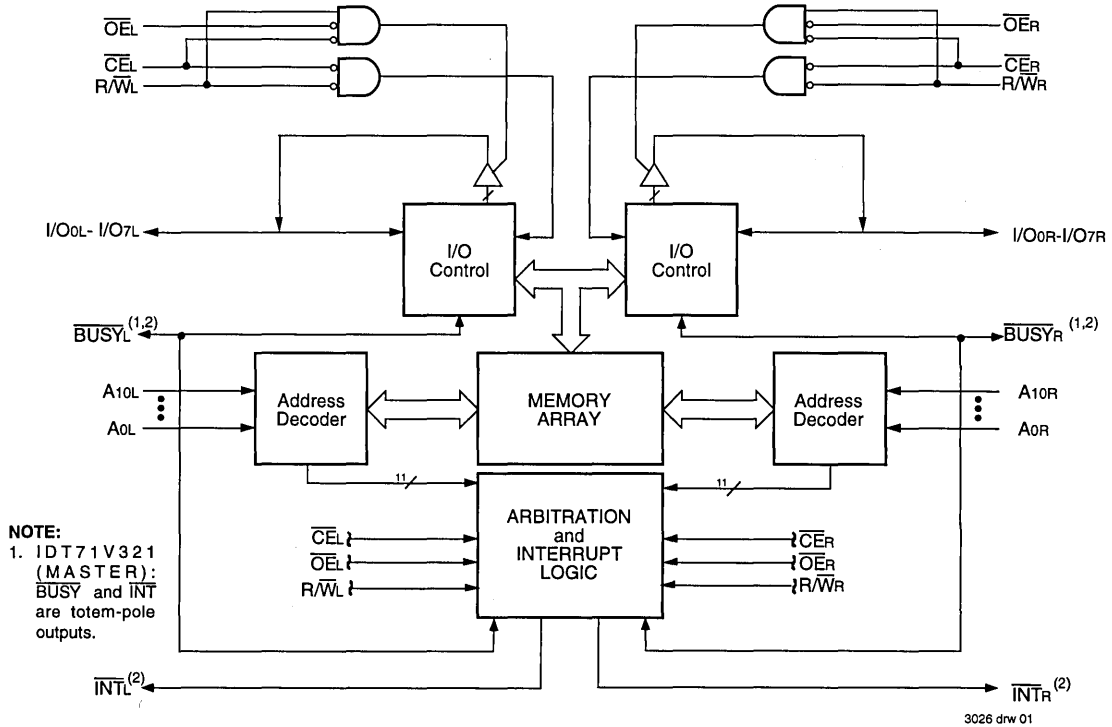
The IDT71V321 is a high-speed 2K x 8 Dual-Port Static RAMs with internal interrupt logic for interprocessor communications. The IDT71V321 is designed to be used as a stand-alone 8-bit Dual-Port RAM.

The device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

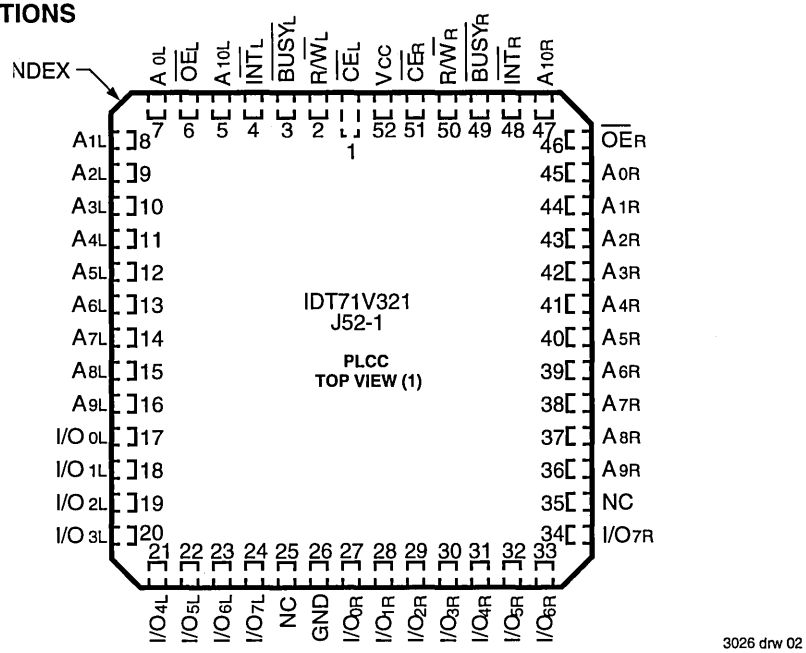
Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 250mW of power. Low-power (L) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

The IDT71V321 devices are packaged in 52-pin PLCCs and 64-pin TQFPs.

FUNCTIONAL BLOCK DIAGRAM

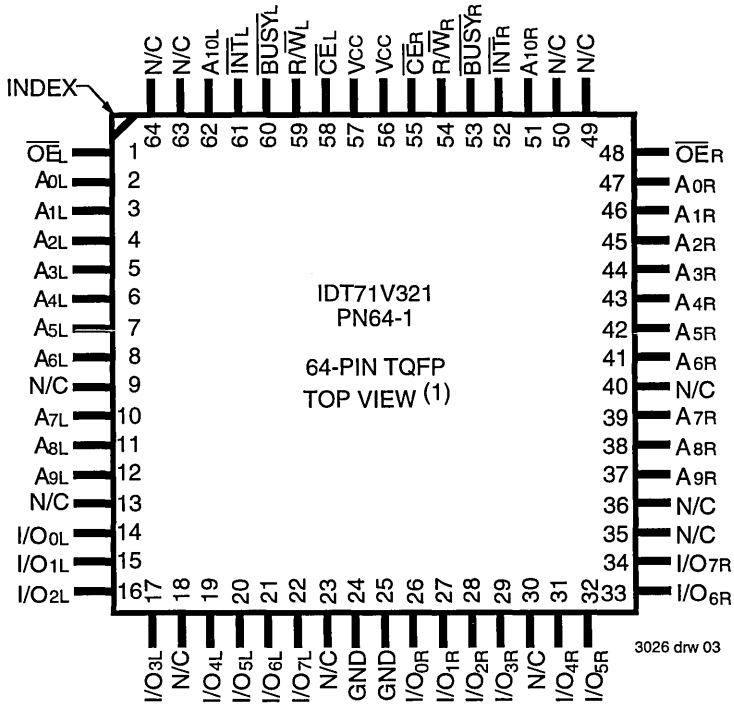


PIN CONFIGURATIONS



3026 drw 02

NOTE: 1. This text does not indicate the orientation of the actusl part-marking.



3026 drw 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

3026 tbl 01

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5 for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V

3026 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	Vcc+0.3	V
V_{IL}	Input Low Voltage	–0.3(1)	—	0.8	V

3026 tbl 03

NOTE:
1. V_{IL} (min.) = -1.5V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Vcc = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	IDT71V321S		IDT71V321L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	Vcc = 3.6V V_{IN} = 0V to Vcc	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to Vcc Vcc = 3.6V	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O0-I/O7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

NOTE:
1. At Vcc<2.0V input leakages are undefined.

3026 tbl 04

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		71V321X25 Typ.[2]	71V321X25 Max.	71V321X35 Typ.[2]	71V321X35 Max.	71V321X55 Typ.[2]	71V321X55 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L	S L	75 75	150 120	75 75	145 115	75 75	135 105	mA
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L.	S L	20 20	50 35	20 20	50 35	20 20	50 35	mA
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5] Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L.	S L	30 30	105 75	30 30	100 70	30 30	90 60	mA
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V	COM'L.	S L	1.0 0.2	5.0 3.0	1.0 0.2	5.0 3.0	1.0 0.2	5.0 3.0	mA
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{CC} - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open f = f_{MAX}[3]	COM'L.	S L	30 30	90 75	30 30	85 70	30 30	75 60	mA

NOTES: 2943 tbl 05

1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 3.3V, T_A = +25°C, and are not production tested. I_{CCDC} = 80mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1 / t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

DATA RETENTION CHARACTERISTICS (L Version Only)

Symbol	Parameter	Test Conditions		71V321L Min.	71V321L Typ.[1]	71V321L Max.	Unit
VDR	VCC for Data Retention	VCC = 2.0V, $\overline{CE} \geq$ VCC - 0.2V VIN ≥ VCC - 0.2V or VIN ≤ 0.2V	COM'L.	2.0	—	0	V
ICCDR	Data Retention Current			—	100	1500	µA
tCDR[3]	Chip Deselect to Data Retention Time			0	—	—	ns
tR[3]	Operation Recovery Time			tRC[2]	—	—	ns

NOTES: 3026 tbl 06

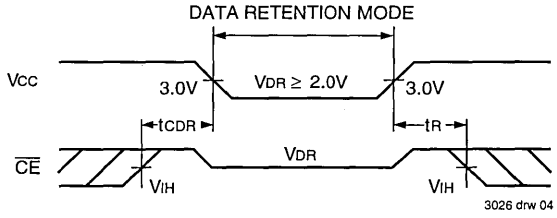
1. V_{CC} = 2V, T_A = +25°C, and is not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed but not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

3026 tbl 07

DATA RETENTION WAVEFORM



3026 drw 04

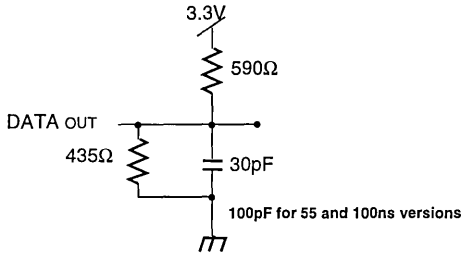


Figure 1. AC Output Test Load

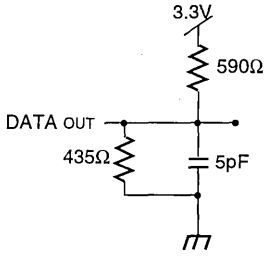
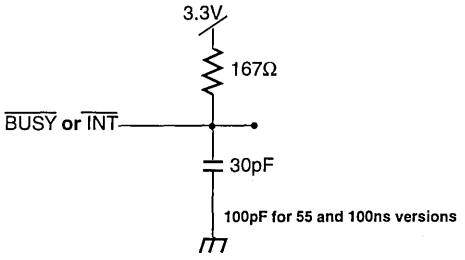


Figure 2. Output Test Load
(For tHZ, tLZ, twz and tow)
* Including scope and jig.



3026 drw 05

Figure 3. BUSY and INT
AC Output Test Load

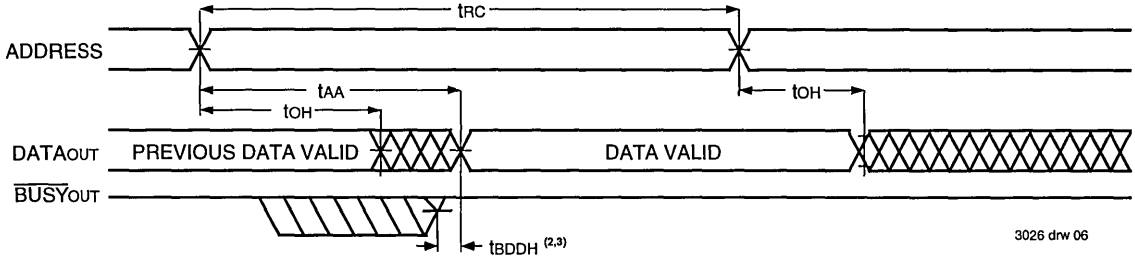
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(4)

Symbol	Parameter	71V321X25 Min.	71V321X25 Max.	71V321X35 Min.	71V321X35 Max.	71V321X55 Min.	71V321X55 Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	25	—	35	—	55	—	ns
tAA	Address Access Time	—	25	—	35	—	55	ns
tACE	Chip Enable Access Time(3)	—	25	—	35	—	55	ns
tAOE	Output Enable Access Time	—	12	—	20	—	25	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	0	—	0	—	0	—	ns
tHZ	Output High-Z Time(1, 2)	—	12	—	15	—	30	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	50	—	50	—	50	ns

2943 tbl 08

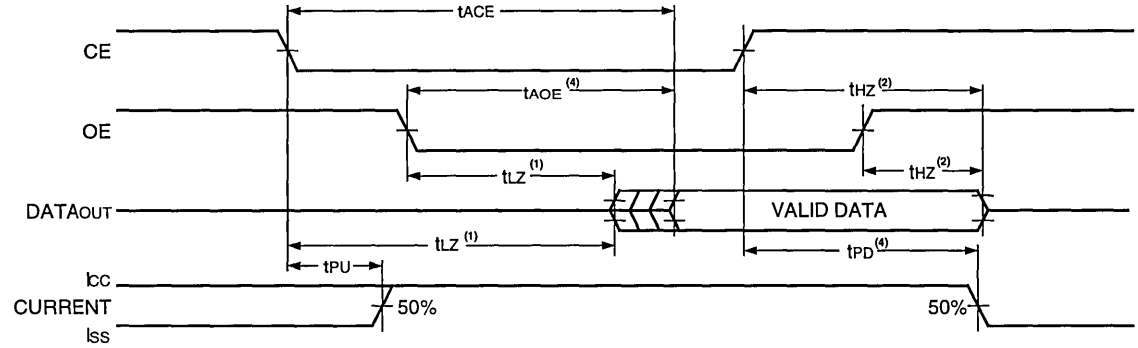
NOTES:
1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL.
4. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE(1)



NOTES:
1. R/$\overline{W}$ = VIH, $\overline{CE}$ = VIL, and is $\overline{OE}$ = VIL. Address is valid prior to the coincidental with $\overline{CE}$ transition Low.
2. t$\overline{BDD}$ delay is required only in case where the opposite is port is completing a write operation to same the address location. For simultanious read operations $\overline{BUSY}$ has no relationship to valid output data.
3. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(3)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is deaserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = VIH, and the address is valid prior to other coincidental with $\overline{CE}$ transition Low.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[5]

Symbol	Parameter	71V321X25		71V321X35		71V321X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	25	—	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write[3]	20	—	30	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	30	—	40	—	ns
t_{AS}	Address Set-up Time[3]	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	30	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	12	—	20	—	20	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	12	—	15	—	30	ns
t_{DH}	Data Hold Time[4]	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1, 2]	—	15	—	15	—	30	ns
t_{OW}	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns

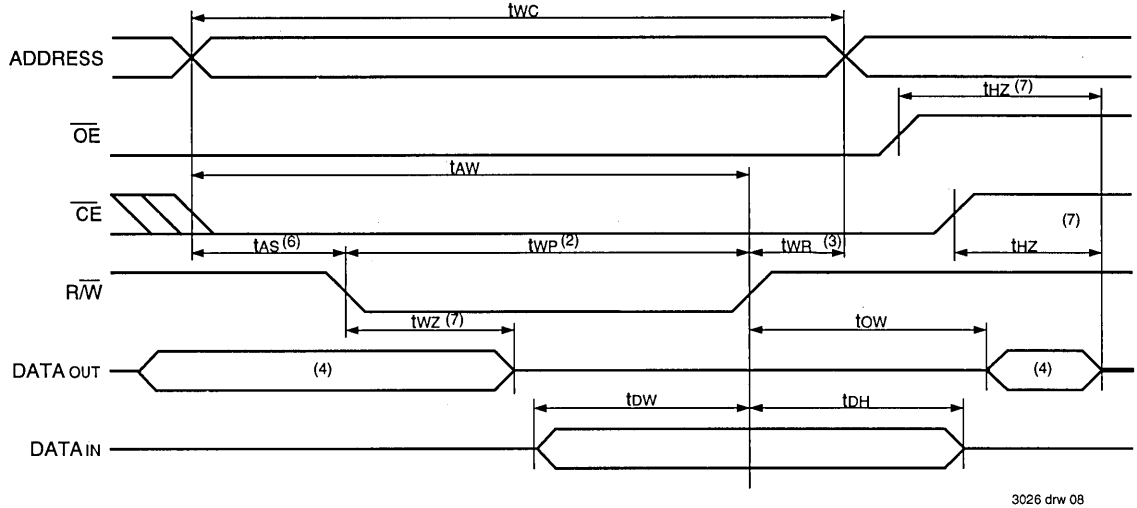
2943 tbl 09

NOTES:

1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. "X" in part numbers indicates power rating (S or L).

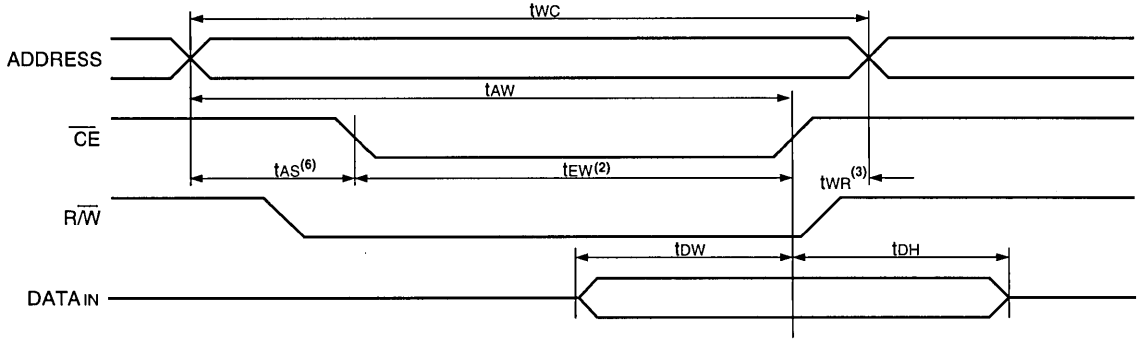
6

TIMING WAVEFORM OF WRITE CYCLE NO. 1,(R/$\overline{W}$ CONTROLLED TIMING) (1,5,8)



3026 drw 08

TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,5)



3026 drw 09

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be High during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of $\overline{CE}$ = VIL and R/$\overline{W}$= VIL.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going High to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ Low transition occurs simultaneously with or after the R/$\overline{W}$ Low transition, the outputs remain in the High impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined be device characterization, but is not production tested. Transition is measured +/- 500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off data to be placed on the bus for the required tDW. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

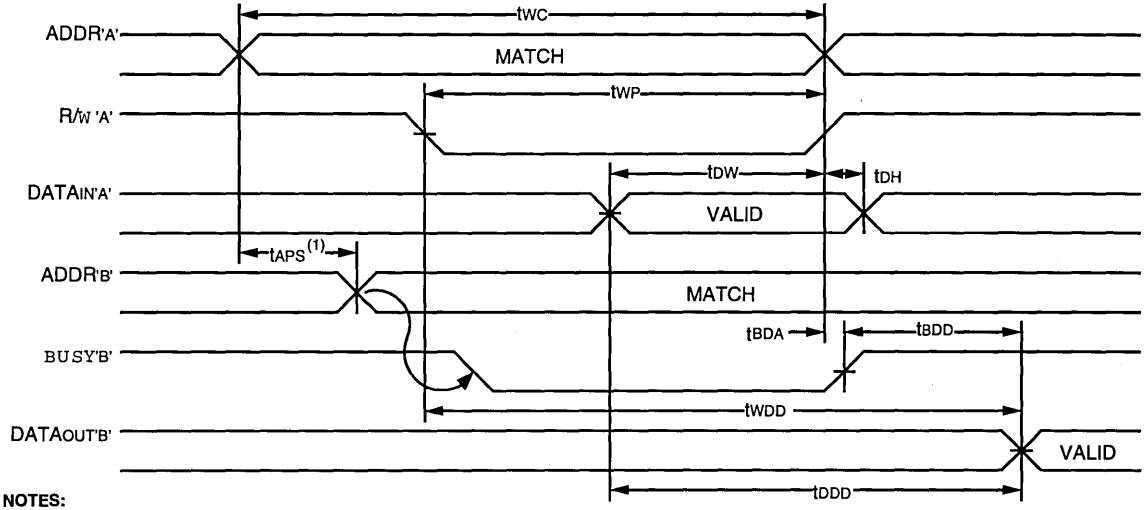
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	71V321X25		71V321X35		71V321X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING ($M/\overline{S}$ = VIH)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	20	—	20	—	30	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	20	—	30	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	20	—	30	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	20	—	20	—	30	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	25	—	35	—	55	ns
tWDD	Write Pulse to Delay Data[1]	—	50	—	60	—	80	ns
tDDD	Write Pulse to Delay Data[1]	—	35	—	45	—	65	ns

NOTES:
2943 tbl 10

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. "X" in part numbers indicates power rating (S or L).

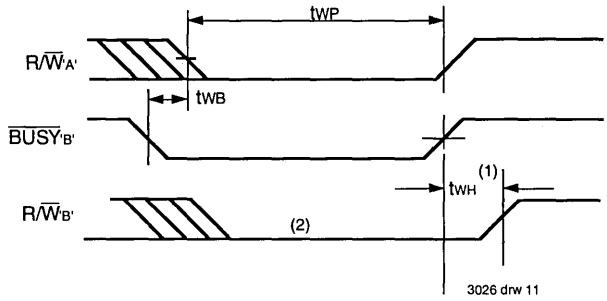
TIMING WAVE FORM OF WRITE WITH PORT-TO-PORT READ WITH $\overline{BUSY}$[1,2,3]



NOTES:
3026 drw 10

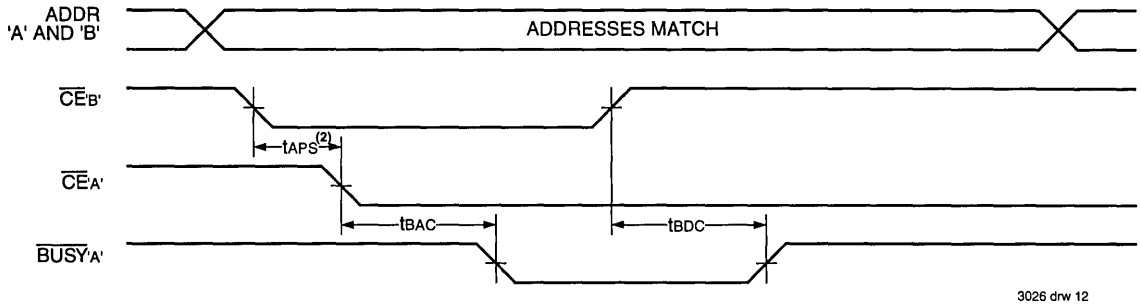
1. To ensure that the earlier of the two ports wins. tAPS is ignored for Slave (IDT7142).
2. $\overline{CE}_L = \overline{CE}_R$ = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is opposite from port "A".

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$[3]

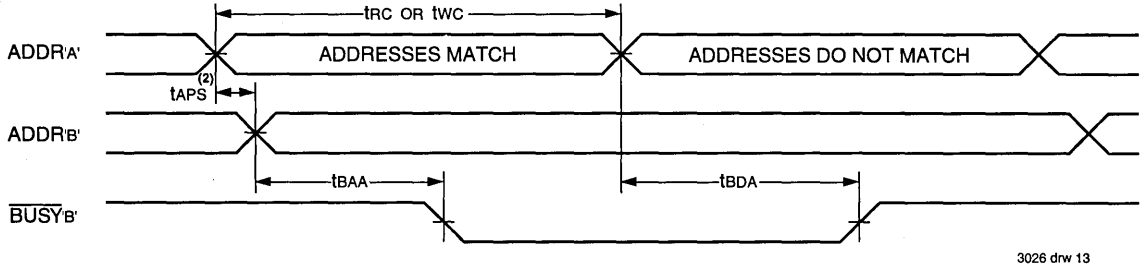


NOTES:
1. tWH must be met for $\overline{BUSY}$.
2. $\overline{BUSY}$ is asserted on port 'B' blocking R/W'B', until $\overline{BUSY}$'B' goes High.
3. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is oppsite from port "A".

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING [1]



TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESS MATCH TIMING [1]



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If tAPS is not satisified, the BUSY will be asserted on one side or the other, but there is no guarantee on which side BUSY will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

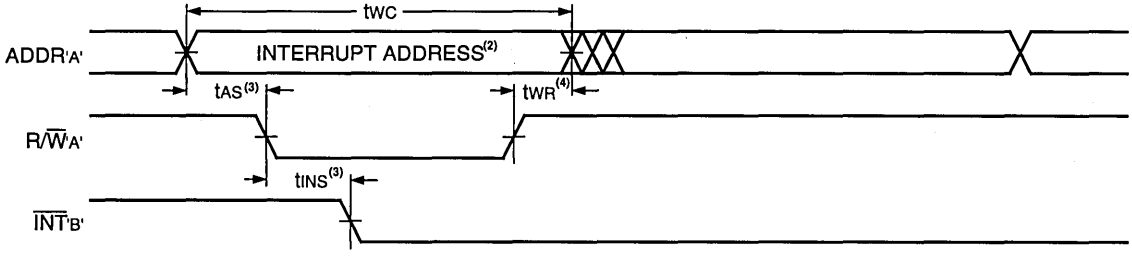
Symbol	Parameter	71V321X25 Min.	71V321X25 Max.	71V321X35 Min.	71V321X35 Max.	71V321X55 Min.	71V321X55 Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	25	—	45	ns
tINR	Interrupt Reset Time	—	25	—	25	—	45	ns

NOTE:
1. "X" in part numbers indicates power rating (S or L).

2942 tbl 11

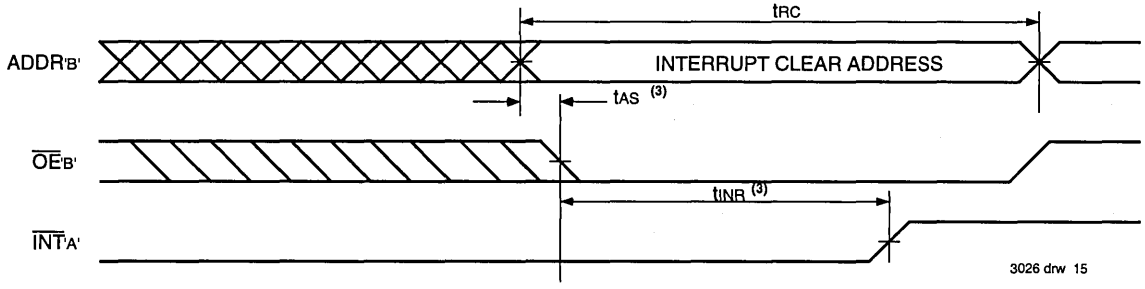
TIMING WAVEFORM OF INTERRUPT MODE

$\overline{INT}$ SETS



3026 drw 14

$\overline{INT}$ CLEARS



3026 drw 15

NOTES:.
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. See Interrupt Truth Table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TABLE I. NON-CONTENTION READ/WRITE CONTROL[4]

Left or Right Port[1]				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = V_{IH}$, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	DATAIN	Data on Port Written Into Memory[2]
H	L	L	DATAOUT	Data in Memory Output on Port[3]
H	L	H	Z	High Impedance Outputs

2654 tbl 12

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY}$ = L, data is not written.
3. If $\overline{BUSY}$ = L, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. 'H' = V_{IH}, 'L' = V_{IL}, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

TABLE II. INTERRUPT FLAG[1,4]

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{10L} - A_{0L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{10L} - A_{0R}$	$\overline{INT}_R$	Function
L	L	X	3FF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	3FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2654 tbl 13

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$
2. If $\overline{BUSY}_L = V_{IL}$, then No Change.
3. If $\overline{BUSY}_R = V_{IL}$, then No Change.
4. 'H' = HIGH,' L' = LOW,' X' = DON'T CARE

TABLE III — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{10L} A_{0R}-A_{10R}	$\overline{BUSY}_L$[1]	$\overline{BUSY}_R$[1]	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit[3]

2654 tbl 14

NOTE:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs for IDT71V321 (master). $\overline{BUSY}_X$ outputs on the IDT71V321 are open drain, not push-pull outputs.
2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be low simultaneously.

FUNCTIONAL DESCRIPTION

The IDT71V321 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT71V321 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = V_{IH}). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FE (HEX), where a write is defined as the $\overline{CE}$ = R/$\overline{W}$ = V_{IL} per the Truth Table. The left port clears the interrupt by access address location 7FE access when $\overline{CE}_R$ = $\overline{OE}_R$ = V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must access the memory location 7FF. The message (8 bits) at 7FE or 7FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

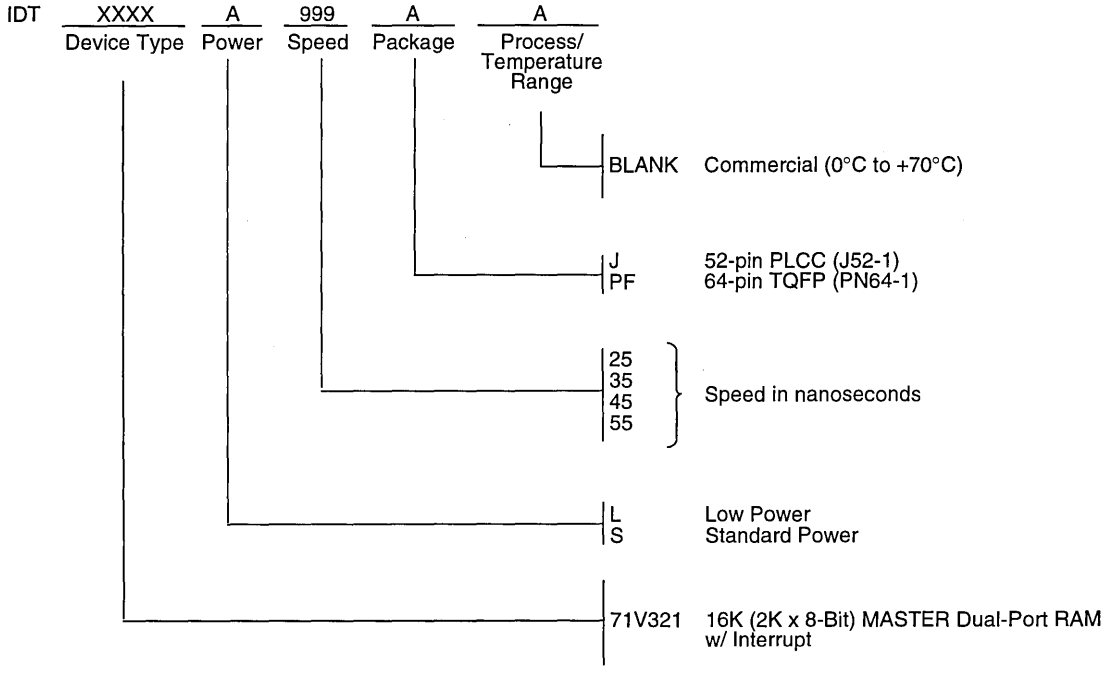
BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The Busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation.

The Busy outputs on the IDT71V321 RAM are open drain type outputs and require open drain resistors to operate. If these RAMs are being expanded in depth, then the Busy indication for the resulting array does not require the use of an external AND gate.

ORDERING INFORMATION



3026 drw 17

Integrated Device Technology, Inc.

HIGH-SPEED 3.3V 8K x 8 DUAL-PORT STATIC RAM

PRELIMINARY
IDT70V05S/L

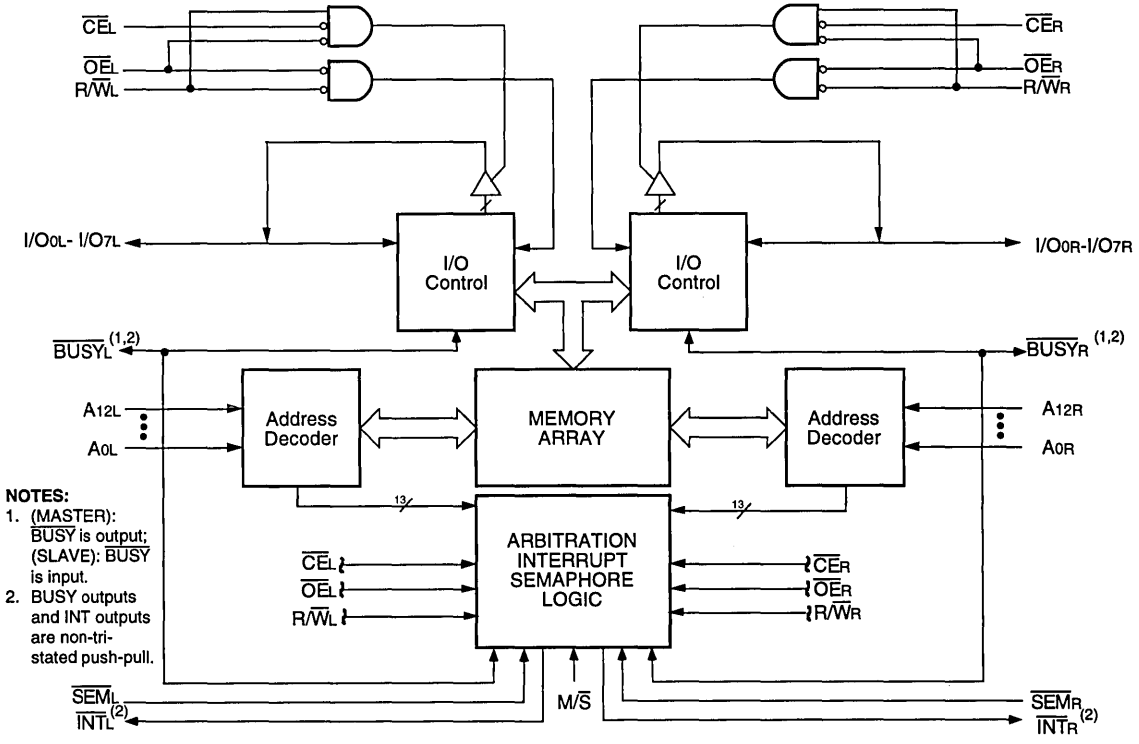
FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Commercial: 25/35/55ns (max.)
- Low-power operation
  - — IDT70V05S
    Active: 350mW (typ.)
    Standby: 3.5mW (typ.)
  - — IDT70V05L
    Active: 350mW (typ.)
    Standby: 1mW (typ.)
- IDT70V05 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Devices are capable of withstanding greater than 2001V electrostatic discharge
- Battery backup operation—2V data retention
- TTL-compatible, single 3.3V (±0.3V) power supply
- Available in 68-pin PGA and PLCC, and a 64-pin TQFP

DESCRIPTION:

The IDT70V05 is a high-speed 8K x 8 Dual-Port Static RAM. The IDT70V05 is designed to be used as a stand-alone 64K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

FUNCTIONAL BLOCK DIAGRAM



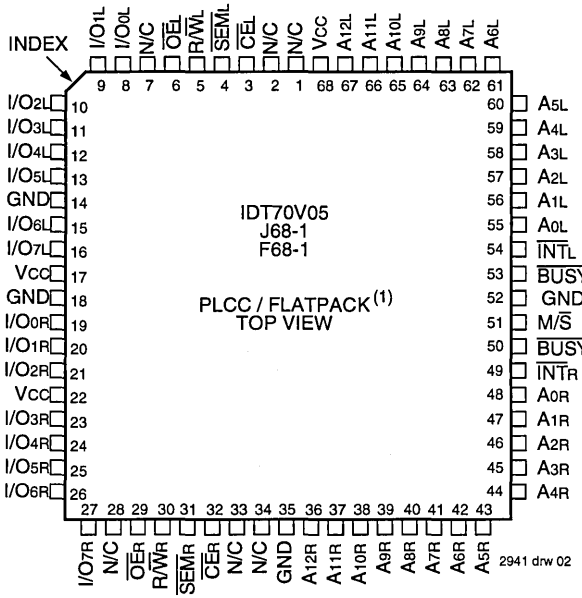
NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. BUSY outputs and INT outputs are non-tri-stated push-pull.

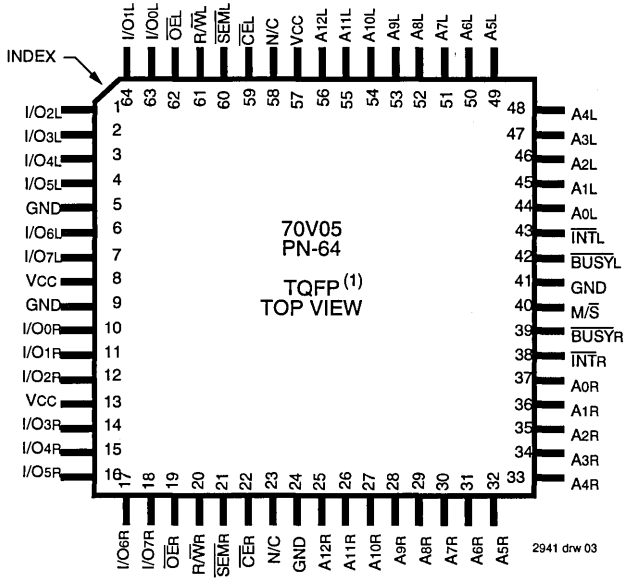
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 350mW of power. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500µW from a 2V battery.

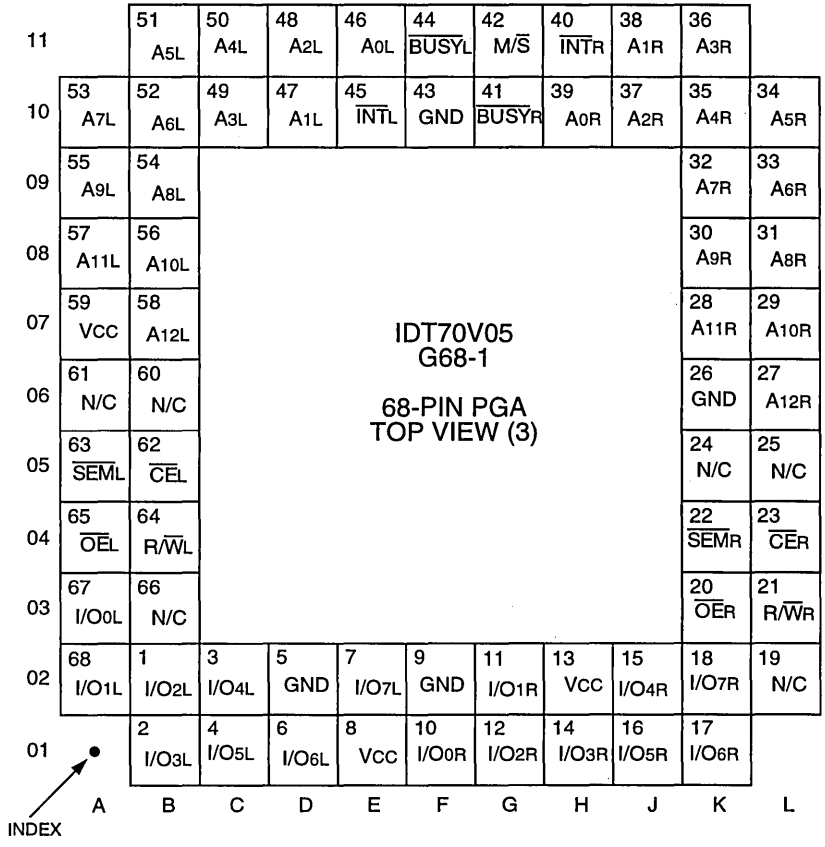
The IDT70V05 is packaged in a ceramic 68-pin PGA and PLCC and a 64-pin thin plastic quad flatpack (TQFP).

PIN CONFIGURATIONS





NOTE:
1. This text does not indicate the actual part-marking



2941 drw 04

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{12L}$	$A_{0R} - A_{12R}$	Address
$I/O_{0L} - I/O_{7L}$	$I/O_{0R} - I/O_{7R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2941 tbl 01

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	X	X	H	High-Z	Deselected: Power Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read Memory
X	X	H	X	High-Z	Outputs Disabled

NOTE: 2941 tbl 02
1. $A_{0L} - A_{12L} \neq A_{0R} - A_{12R}$

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
H	↑	X	L	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	—	Not Allowed

2941 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTES: 2941 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.3V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V

2941 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	Vcc+0.3	V
V_{IL}	Input Low Voltage	–0.3[1]	—	0.8	V

NOTES: 2941 tbl 06
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2941 tbl 07
1. This parameter is determined by device characterization but is not production tested.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	IDT70V05S		IDT70V05L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2941 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V05X25		70V05X35		70V05X55		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L	S	80	140	70	115	70	115	mA
				L	80	120	70	100	70	100	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L.	S	12	25	10	25	10	25	mA
				L	10	20	8	20	8	20	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R$ = V_{IH} Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L.	S	40	82	35	72	35	72	mA
				L	40	72	35	62	35	62	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	COM'L.	S	1.0	5	1.0	5	1.0	5	mA
				L	0.2	2.5	0.2	2.5	0.2	2.5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} - 0.2V $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open f = f_{MAX}[3]	COM'L.	S	50	81	45	71	45	71	mA
				L	50	71	45	61	45	61	

2941 tbl 09

NOTES:
1. X in part numbers indicates power rating (S or L)
2. VCC = 3.3V, TA = +25°C.
3. At f = fMAX, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At Vcc≤2.0V input leakages are undefined.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2941 tbl 10

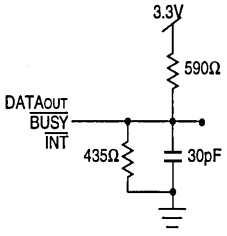


Figure 1. AC Output Test Load

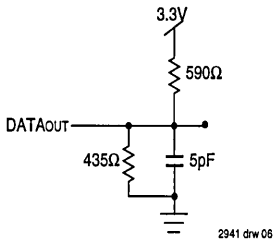


Figure 2. Output Load (For tLZ, tHZ, twz, tow) Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(4)

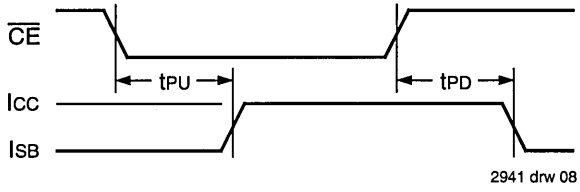
Symbol	Parameter	IDT70V05X25		IDT70V05X35		IDT70V05X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	25	—	35	—	55	—	ns
tAA	Address Access Time	—	25	—	35	—	55	ns
tACE	Chip Enable Access Time(3)	—	25	—	35	—	55	ns
tAOE	Output Enable Access Time	—	15	—	20	—	30	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	3	—	3	—	3	—	ns
tHZ	Output High-Z Time(1, 2)	—	15	—	20	—	25	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	25	—	35	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns
tSAA	Semaphore Address Access Time	—	35	—	45	—	65	ns

NOTES:

2941 tbl 11

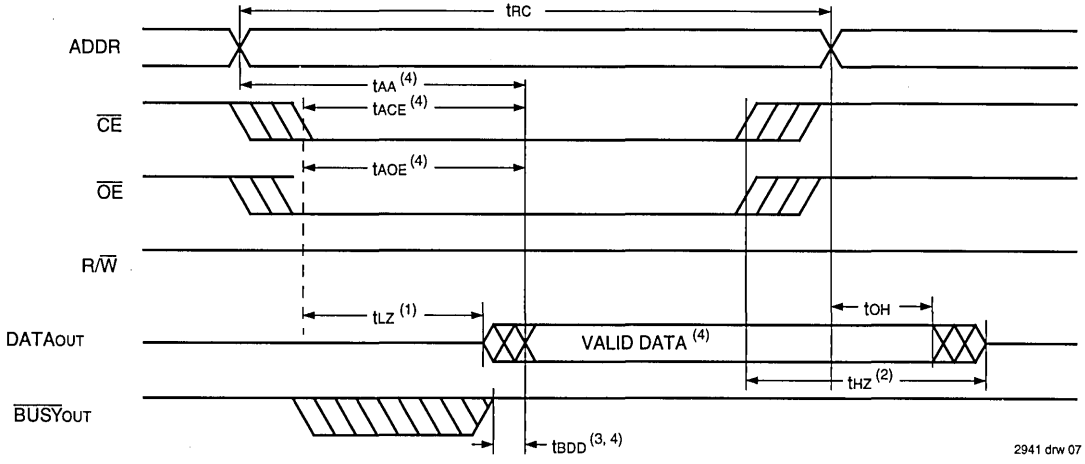
1. Transition is measured ±200mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H.
4. X in part numbers indicates power rating (S or L).

TIMING OF POWER-UP POWER-DOWN



2941 drw 08

WAVEFORM OF READ CYCLES(5)



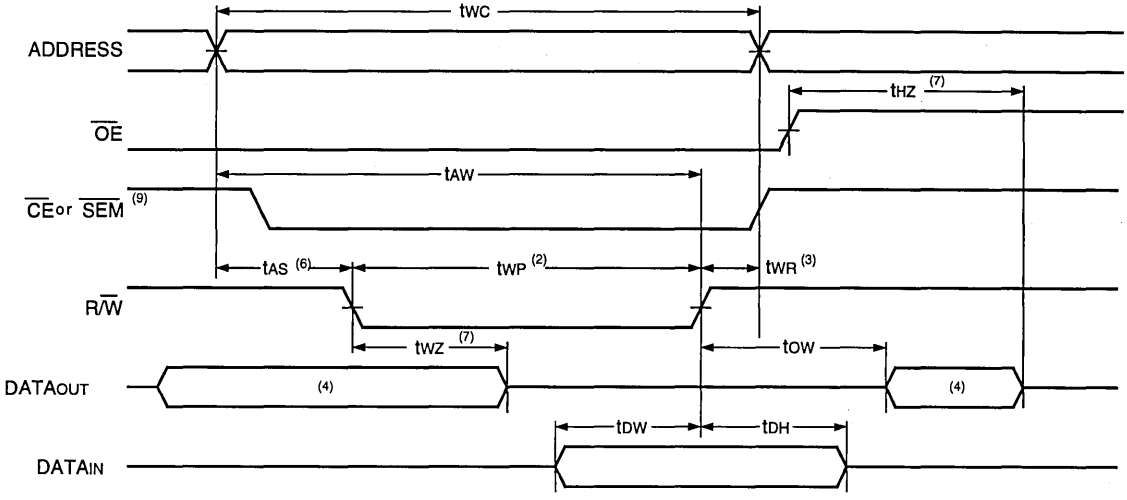
NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$ or $\overline{OE}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = H.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE(5)

Symbol	Parameter	IDT70V05X25 Min.	IDT70V05X25 Max.	IDT70V05X35 Min.	IDT70V05X35 Max.	IDT70V05X55 Min.	IDT70V05X55 Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time	25	—.	35	—	55	—	ns
tEW	Chip Enable to End-of-Write(3)	20	—	30	—	45	—	ns
tAW	Address Valid to End-of-Write	20	—	30	—	45	—	ns
tAS	Address Set-up Time(3)	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	20	—	30	—	ns5
tHZ	Output High-Z Time(1, 2)	—	15	—	20	—	25	ns
tDH	Data Hold Time(4)	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z(1, 2)	—	15	—	20	—	25	ns
tOW	Output Active from End-of-Write(1, 2, 4)	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

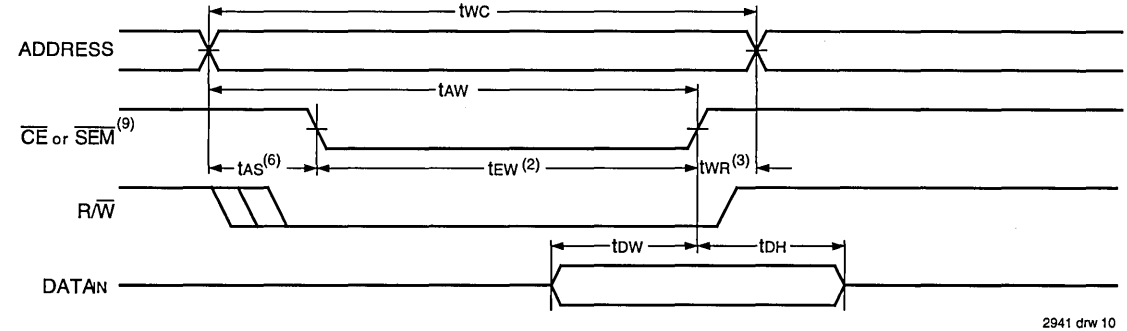
NOTES:
2941 tbl 12
1. Transition is measured ±200mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. X in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,3,5,8)



2941 drw 09

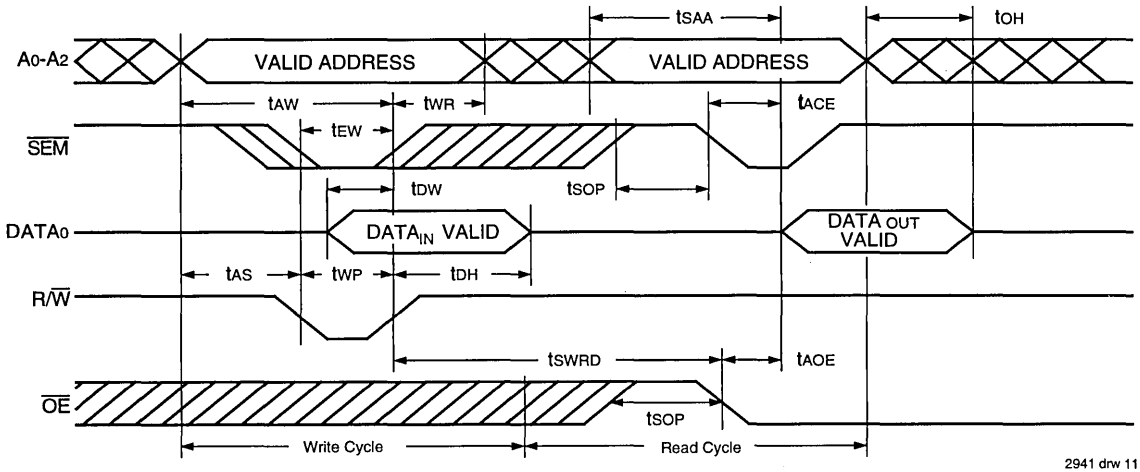
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,3,5,8)



2941 drw 10

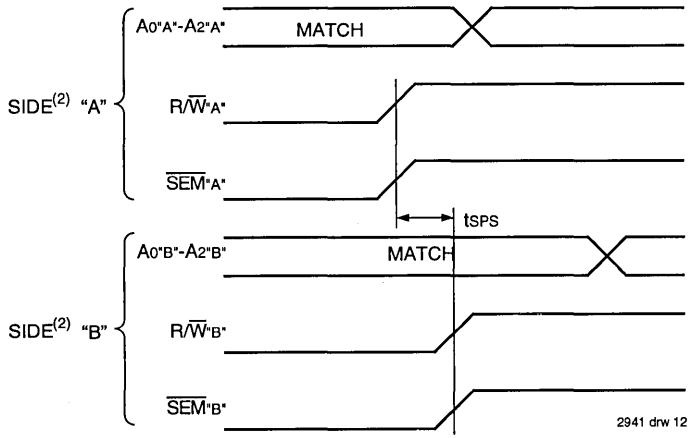
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, or R/$\overline{W}$.
7. Timing depends on which enable signal is de-asserted first, $\overline{CE}$, or R/$\overline{W}$.
8. If $\overline{OE}$ is LOW during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = H for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. $D_{OR} = D_{OL}$ = L, $\overline{CE}_R = \overline{CE}_L$ = H, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going high to $R/\overline{W}_B$ or $\overline{SEM}_B$ going HIGH.
4. If t_{SPS} is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

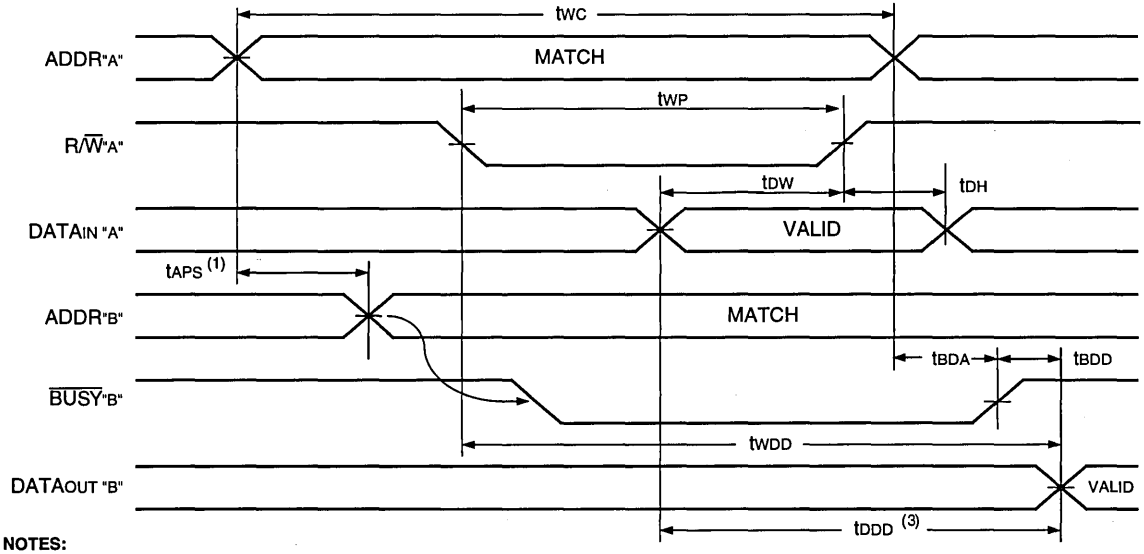
Symbol	Parameter	IDT70V05X25		IDT70V05X35		IDT70V05X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	25	—	35	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	25	—	35	—	45	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	25	—	35	—	45	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	25	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	25	—	35	—	35	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	20	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	55	—	65	—	85	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	50	—	60	—	80	ns

NOTES: 2941 tbl 13

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = H) or "Timing Waveform of Write With Port-To-Port Delay (M/$\overline{S}$=L)"".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. "x" is part numbers indicates power rating (S or L).

6

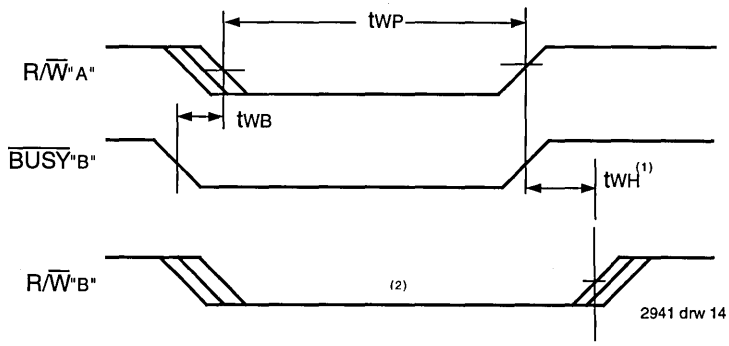
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ WITH $\overline{BUSY}$[2] (M/$\overline{S}$ = V_{IH})



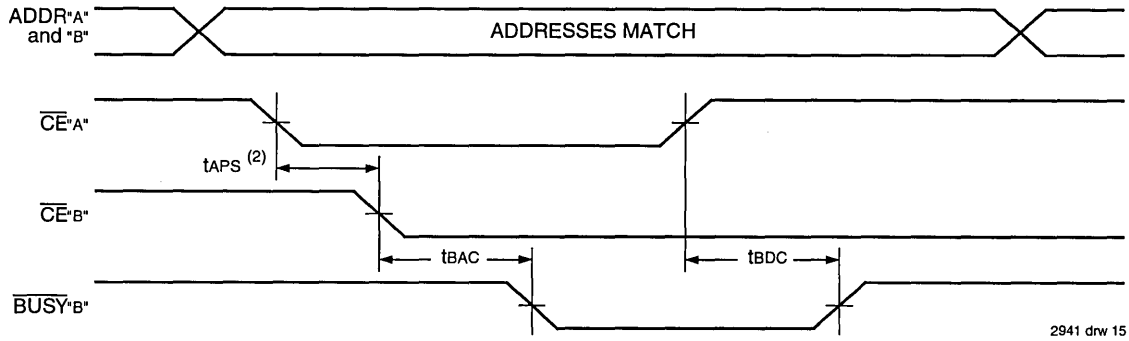
NOTES:

1. To ensure that the earlier of the two ports wins. 2941 drw 13
2. $\overline{CE_L}$ = $\overline{CE_R}$ = L
3. $\overline{OE}$ = L for the reading port.

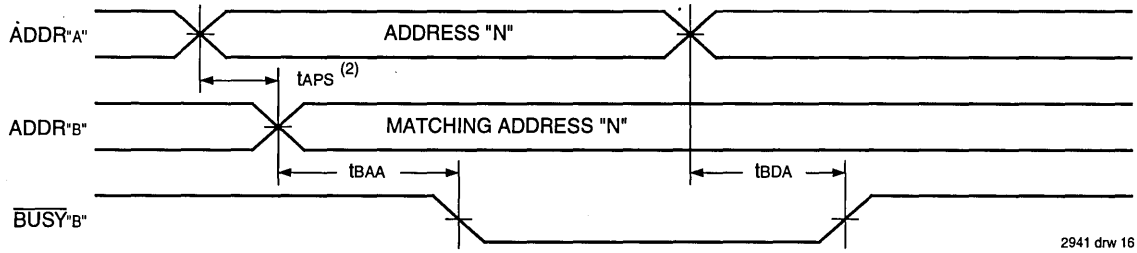
TIMING WAVEFORM OF SLAVE WRITE (M/$\overline{S}$ = L)



WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1) (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)(M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

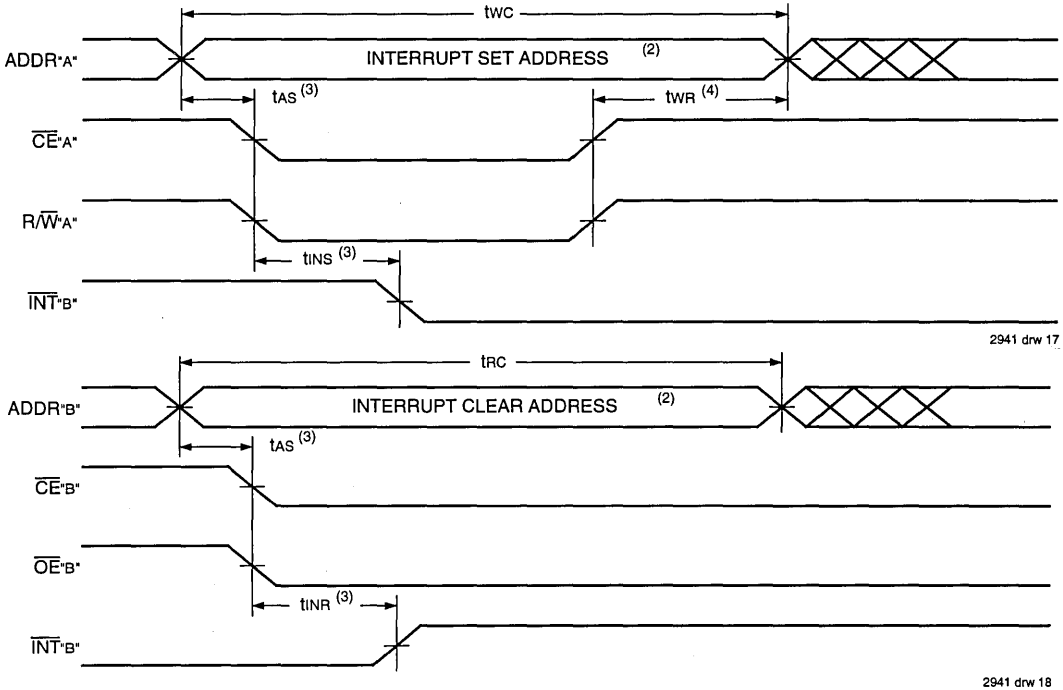
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

Symbol	Parameter	IDT70V05X25 Min.	IDT70V05X25 Max.	IDT70V05X35 Min.	IDT70V05X35 Max.	IDT70V05X55 Min	IDT70V05X55 Max.	Unit
INTERRUPT TIMING								
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	30	—	40	ns
t_{INR}	Interrupt Reset Time	—	30	—	35	—	45	ns

NOTE:
1. "x" in part numbers indicates power rating (S or L).

2941 tbl 14

WAVEFORM OF INTERRUPT TIMING[1]



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					Function
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{12L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{12R}	$\overline{INT}_R$	
L	L	X	1FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	1FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	1FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	1FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then no change.
3. If $\overline{BUSY}_R$ = L, then no change.

2941 tbl 15

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{12L} A_{0R}-A_{12R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

2941 tbl 16

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}_X$ outputs on the IDT70V05 are push pull, not open drain outputs. On slaves the $\overline{BUSY}_X$ input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_7 Left	D_0 - D_7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

2941 tbl 17

NOTE:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V05.

FUNCTIONAL DESCRIPTION

The IDT70V05 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V05 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is set when the right port writes to memory location 1FFE (HEX). The left port clears the interrupt by reading address location 1FFE. Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 1FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 1FFF. The message (8 bits) at 1FFE or 1FFF is user-defined. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical

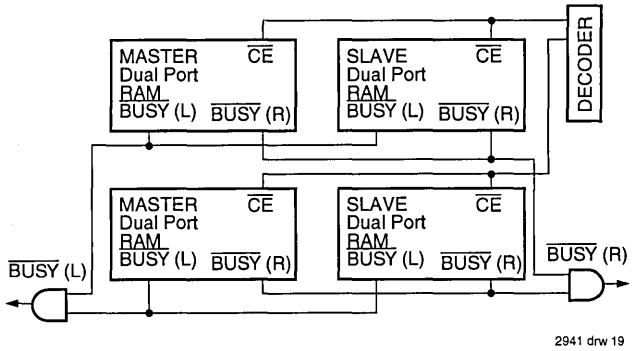


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70V05 RAMs.

operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 70V05 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT70V05 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT70V05 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with the R/$\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT70V05 is an extremely fast Dual-Port 8K x 8 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT70V05 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70V05's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70V05 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in

6

system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70V05 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT70V05's Dual-Port RAM. Say the 8K x 8 RAM was to be divided into two 4K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

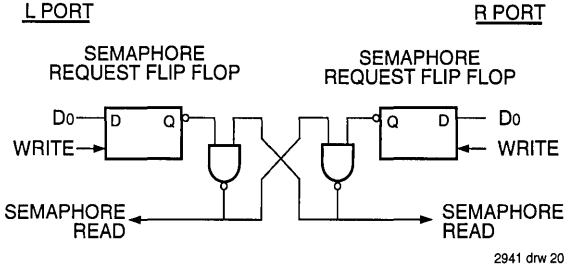
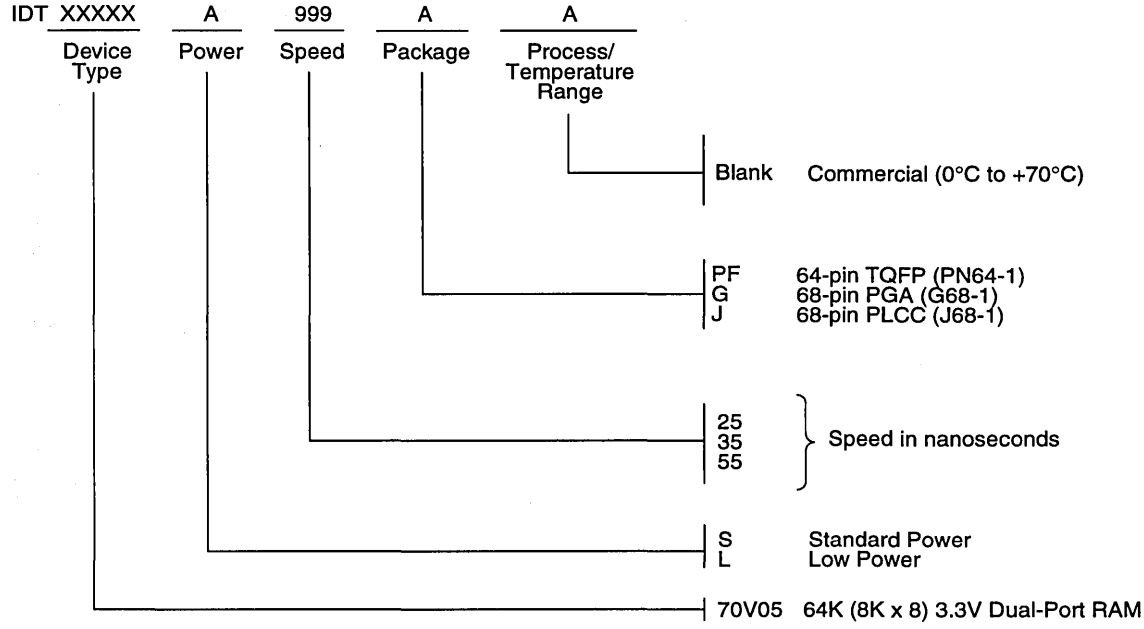


Figure 4. IDT70V05 Semaphore Logic

ORDERING INFORMATION



2941 drw 21

Integrated Device Technology, Inc.

HIGH-SPEED 3.3V 16K x 8 DUAL-PORT STATIC RAM

PRELIMINARY
IDT70V06S/L

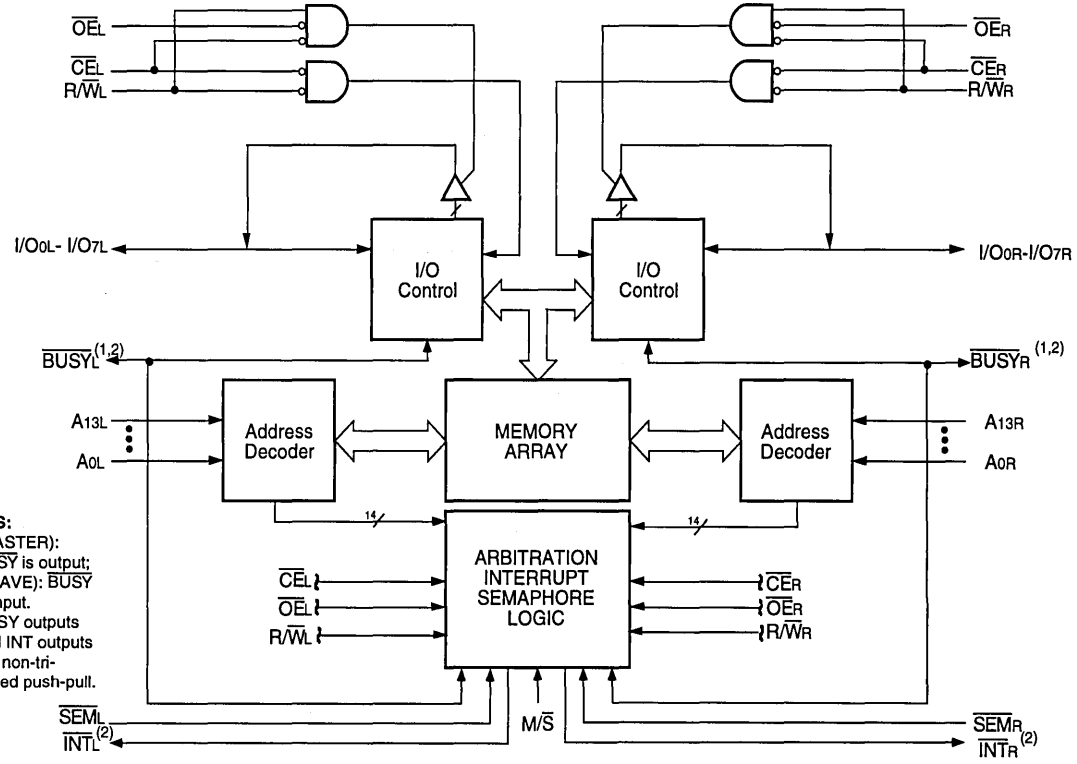
FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Commercial:25/35/55ns (max.)
- Low-power operation
  - — IDT70V06S
    Active: 350mW (typ.)
    Standby: 3.5mW (typ.)
  - — IDT70V06L
    Active: 350mW (typ.)
    Standby: 1mW (typ.)
- IDT70V06 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Devices are capable of withstanding greater than 2001V electrostatic discharge
- Battery backup operation—2V data retention
- TTL-compatible, single 3.3V (±0.3V) power supply
- Available in 68-pin PGA and PLCC, and a 64-pin TQFP

DESCRIPTION:

The IDT70V06 is a high-speed 16K x 8 Dual-Port Static RAM. The IDT70V06 is designed to be used as a stand-alone 128K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free operation without the need for additional

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. BUSY outputs and INT outputs are non-tri-stated push-pull.

2942 drw 01

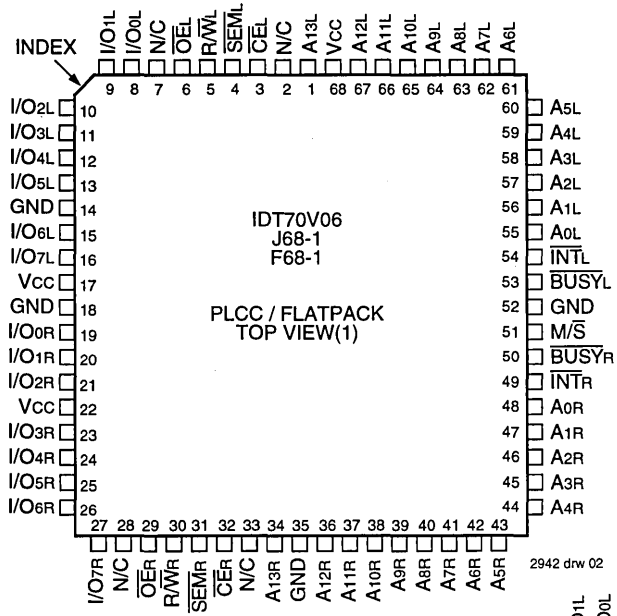
discrete logic.

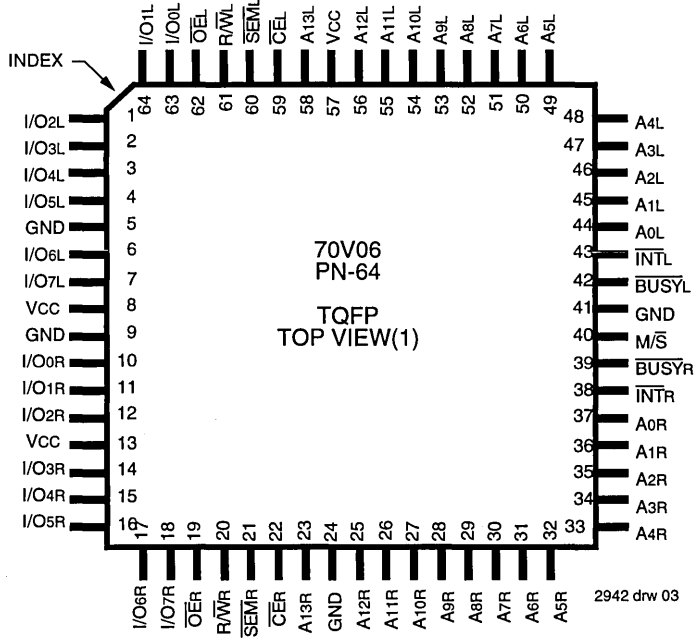
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 350mW of power. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500µW from a 2V battery.

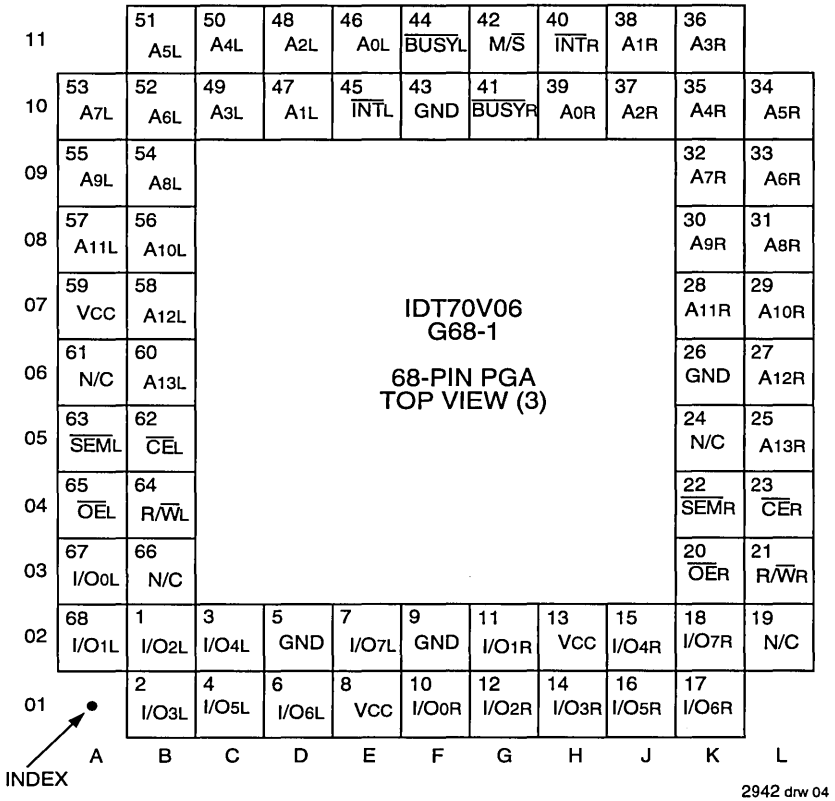
The IDT70V06 is packaged in a ceramic 68-pin PGA and PLCC and a 64-pin thin plastic quad flatpack (TQFP).

PIN CONFIGURATIONS





NOTE:
1. This text does not indicate the actual part marking.



2942 drw 04

PIN NAMES

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{13L}$	$A_{0R} - A_{13R}$	Address
$I/O_{0L} - I/O_{7L}$	$I/O_{0R} - I/O_{7R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2942 tbl 01

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate the actual part marking.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	X	X	H	High-Z	Deselected: Power Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read Memory
X	X	H	X	High-Z	Outputs Disabled

NOTE:
1. $A_{0L} — A_{13L} \neq A_{0R} — A_{13R}$

2942 tbl 02

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
H	↑	X	L	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	—	Not Allowed

2942 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	−0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	°C
T_{STG}	Storage Temperature	−55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTES:
2942 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.3V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V

2942 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	Vcc+0.3	V
V_{IL}	Input Low Voltage	−0.3[1]	—	0.8	V

NOTES:
2942 tbl 06

1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
2942 tbl 07

1. This parameter is determined by device characterization but is not production tested.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	IDT70V06S		IDT70V06L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[5]	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2942 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version	70V06X25		70V06X35		70V06X55		Unit
				Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L. S L	80 80	140 120	70 70	115 100	70 70	115 100	mA
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L. S L	12 10	25 20	10 8	25 20	10 8	25 20	mA
I_{SB2}	Standby Current (One Port — TTL Level Inputs) $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	$\overline{CE}_L$ or $\overline{CE}_R$ = V_{IH} Active Port Outputs Open f = f_{MAX}[3]	COM'L. S L	40 40	82 72	35 35	72 62	35 35	72 62	mA
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	COM'L. S L	1.0 0.2	5 2.5	1.0 0.2	5 2.5	1.0 0.2	5 2.5	mA
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} - 0.2V $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open f = f_{MAX}[3]	COM'L. S L	50 50	81 71	45 45	71 61	45 45	71 61	mA

2942 tbl 09

NOTES:
1. X in part numbers indicates power rating (S or L)
2. V_{CC} = 3.3V, T_A = +25°C.
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. At Vcc≤2.0V input leakages are undefined.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2942 tbl 10

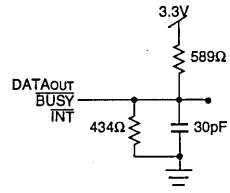


Figure 1. AC Output Test Load

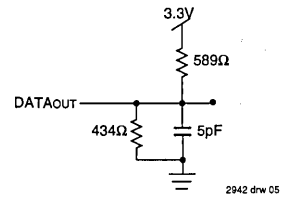


Figure 2. Output Load (5pF for tLZ, tHZ, tWZ, tOW) Including scope and jig.

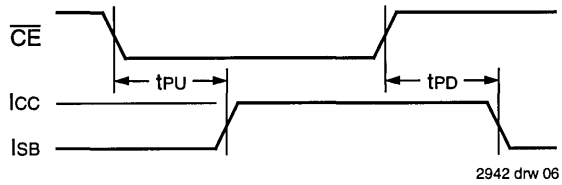
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(4)

Symbol	Parameter	IDT70V06X25 Min.	IDT70V06X25 Max.	IDT70V06X35 Min.	IDT70V06X35 Max.	IDT70V06X55 Min.	IDT70V06X55 Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	25	—	35	—	55	—	ns
tAA	Address Access Time	—	25	—	35	—	55	ns
tACE	Chip Enable Access Time(3)	—	25	—	35	—	55	ns
tAOE	Output Enable Access Time	—	15	—	20	—	30	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	3	—	3	—	3	—	ns
tHZ	Output High-Z Time(1, 2)	—	15	—	20	—	25	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	25	—	35	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns
tSAA	Semaphore Address Access Time	—	35	—	45	—	65	ns

2942 tbl 11

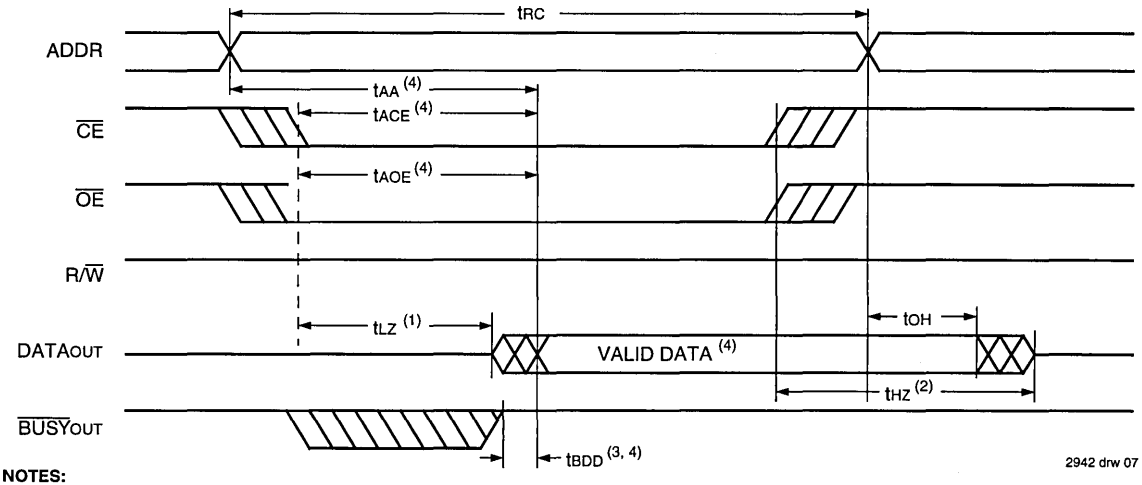
NOTES:
1. Transition is measured ±200mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H.
4. X in part numbers indicates power rating (S or L).

TIMING OF POWER-UP POWER-DOWN



2942 drw 06

WAVEFORM OF READ CYCLES[5]



2942 drw 07

NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$ or $\overline{OE}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

6

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE [5]

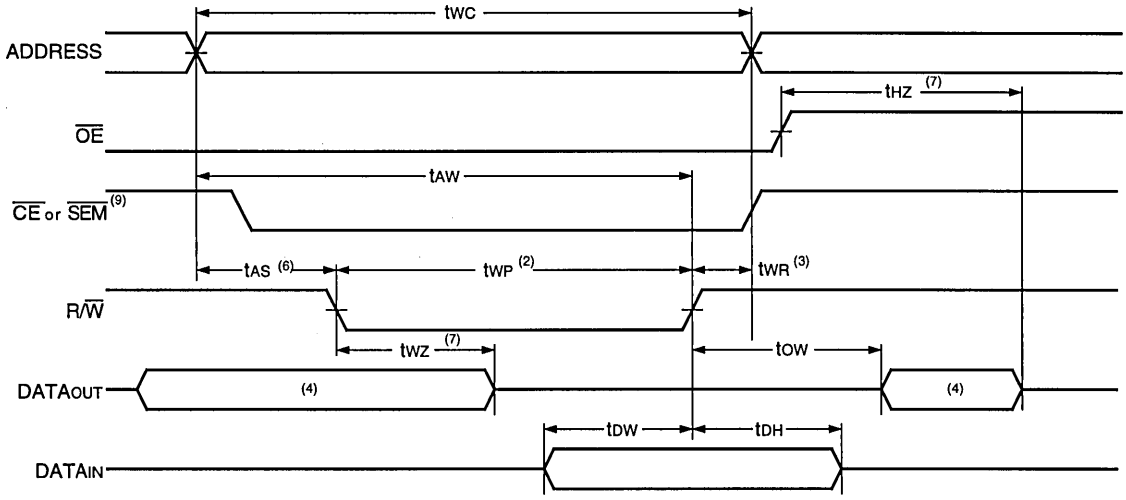
Symbol	Parameter	IDT70V06X25		IDT70V06X35		IDT70V06X55		Unit
		Min.	Max	Min.	Max	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	25	—	35	—	55	—	ns
tEW	Chip Enable to End-of-Write[3]	20	—	30	—	45	—	ns
tAW	Address Valid to End-of-Write	20	—	30	—	45	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	20	—	30	—	ns5
tHZ	Output High-Z Time[1, 2]	—	15	—	20	—	25	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	15	—	20	—	25	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

NOTES:

2942 tbl 12

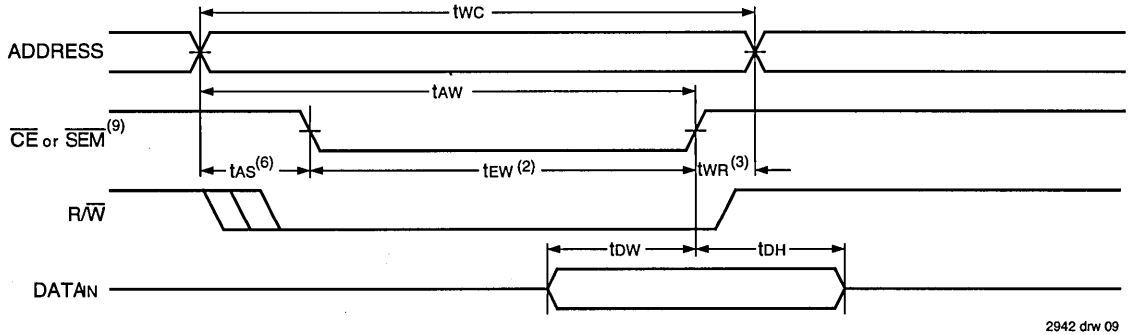
1. Transition is measured ±200mV from low or high impedance voltage with load (Figures 1 and 2).
2. This parameter is guaranteed but not tested.
3. To access RAM, $\overline{CE}$ = L, $\overline{SEM}$ = H. To access semaphore, $\overline{CE}$ = H and $\overline{SEM}$ = L. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. X in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,3,5,8)



2942 drw 08

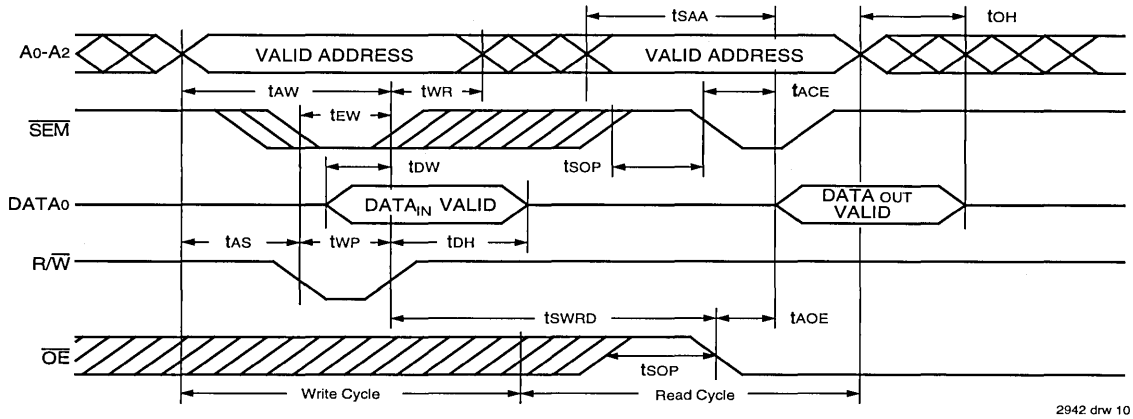
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,3,5,8)



2942 drw 09

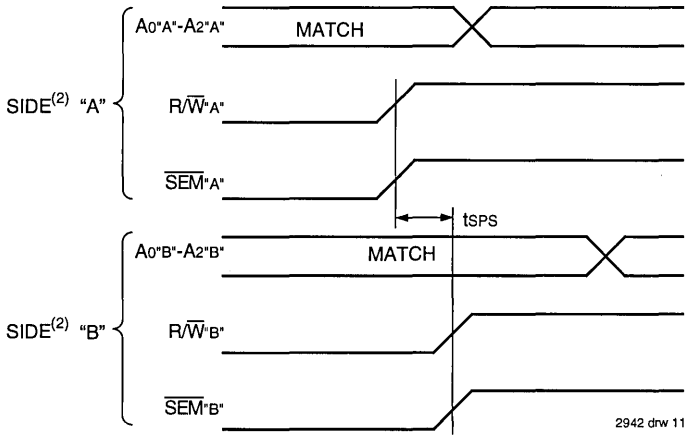
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, or R/$\overline{W}$.
7. Timing depends on which enable signal is de-asserted first, $\overline{CE}$, or R/$\overline{W}$.
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = H for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. $D_{OR} = D_{OL}$ = L, $\overline{CE}_R = \overline{CE}_L$ = H, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going high to $R/\overline{W}_B$ or $\overline{SEM}_B$ going high.
4. If t_{SPS} is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

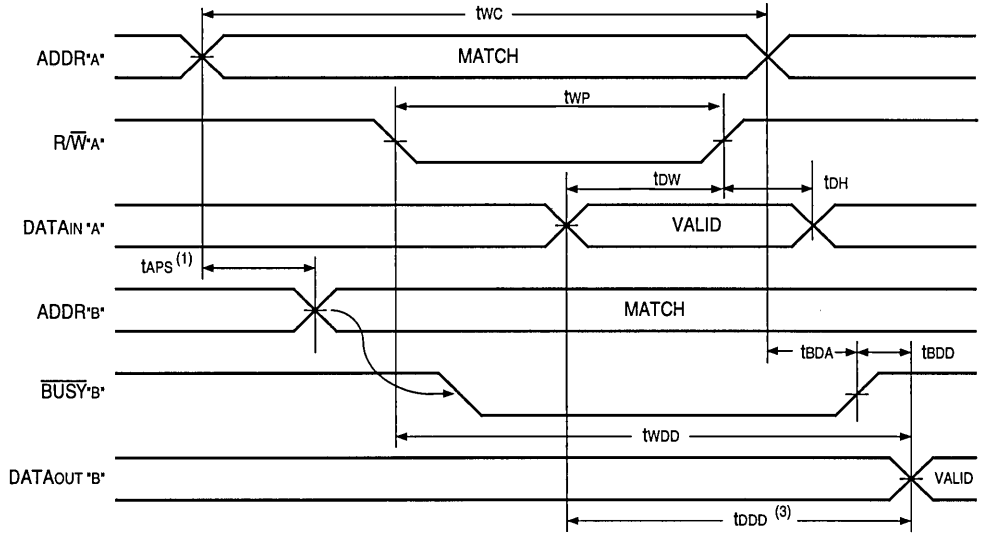
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	IDT70V06X25		IDT70V06X35		IDT70V06X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	25	—	35	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	25	—	35	—	45	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	25	—	35	—	45	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	25	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	25	—	35	—	55	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	20	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	55	—	65	—	85	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	50	—	60	—	80	ns

NOTES: 2942 tbl 12

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M/$\overline{S}$ = H) or "Timing Waveform of Write With Port-To-Port Delay (M/$\overline{S}$=L)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. "x" is part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$[2] (M/$\overline{S}$ = H)

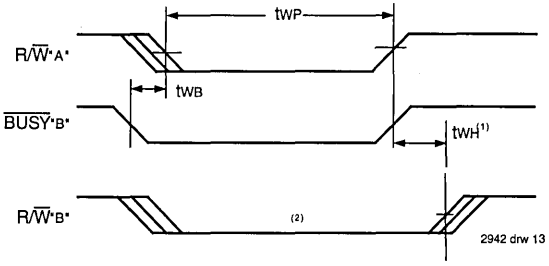


2942 drw 12

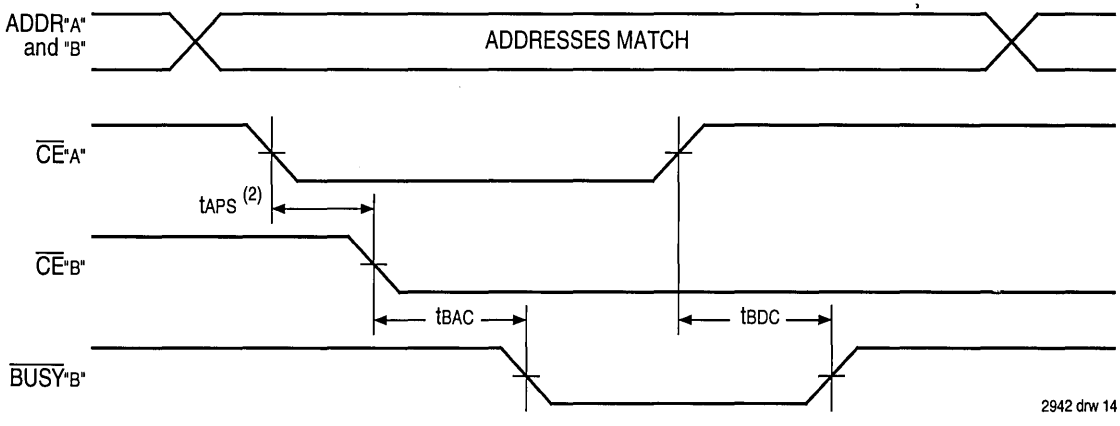
NOTES:

1. To ensure that the earlier of the two ports wins. tAPS is ignored for M/$\overline{S}$ = VIL (SLAVE).
2. $\overline{CE}_L$ = $\overline{CE}_R$ = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. If M/$\overline{S}$ = VIL(slave) then BUSY is input ($\overline{BUSY}$"A" = VIH and $\overline{BUSY}$"B" = "don't care", for this example.
5. All timing is the same for left and right port. Port "A' may be either left or right port. Port "B" is the port opposite from Port "A".

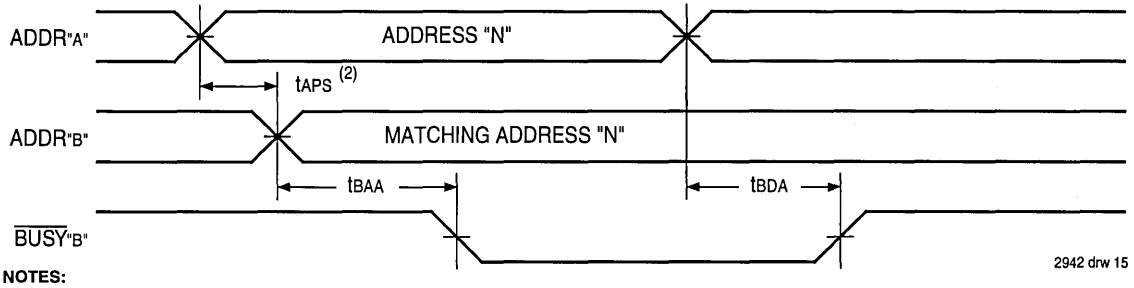
TIMING WAVEFORM OF SLAVE WRITE (M/$\overline{S}$ = L)



WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1) (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)(M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

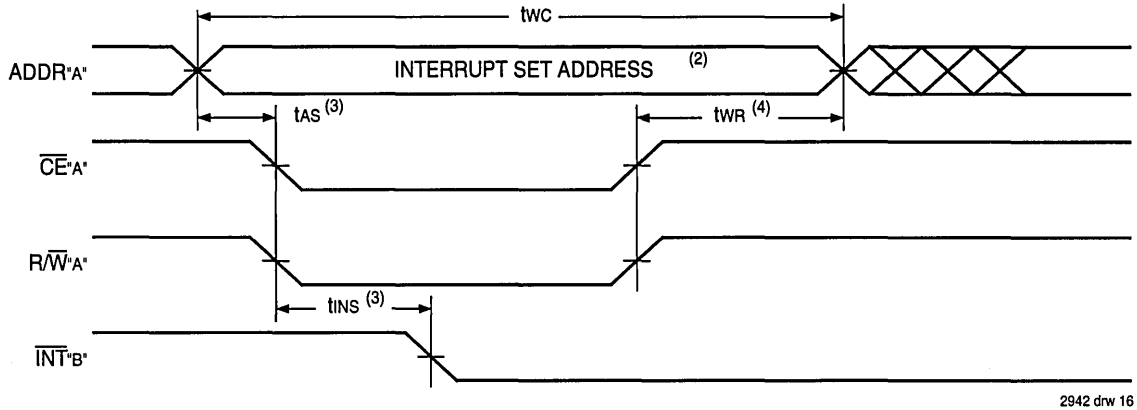
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1)

Symbol	Parameter	IDT70V06X25 Min.	IDT70V06X25 Max.	IDT70V06X35 Min.	IDT70V06X35 Max.	IDT70V06X55 Min	IDT70V06X55 Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	30	—	40	ns
tINR	Interrupt Reset Time	—	30	—	35	—	45	ns

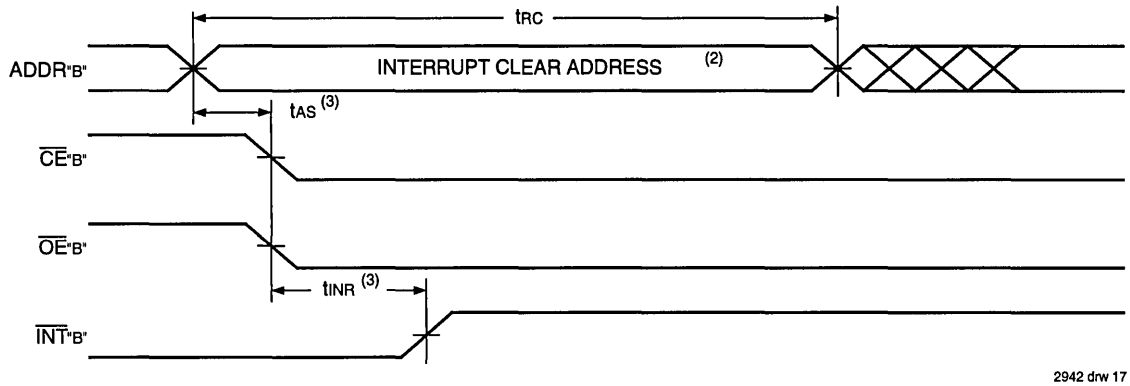
NOTE:
1. "x" in part numbers indicates power rating (S or L).

2942 tbl 14

WAVEFORM OF INTERRUPT TIMING[1]



2942 drw 16



2942 drw 17

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{13L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{13R}	$\overline{INT}_R$	Function
L	L	X	3FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	3FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R$ = H.
2. If $\overline{BUSY}_L$ = L, then no change.
3. If $\overline{BUSY}_R$ = L, then no change.

2942 tbl 15

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE_L}$	$\overline{CE_R}$	A_{0L}-A_{13L} A_{0R}-A_{13R}	$\overline{BUSY_L}$(1)	$\overline{BUSY_R}$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

NOTES: 2942 tbl 16

1. Pins $\overline{BUSY_L}$ and $\overline{BUSY_R}$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$x outputs on the IDT70V06 are push pull, not open drain outputs. On slaves the $\overline{BUSY}$x input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY_L}$ or $\overline{BUSY_R}$ = Low will result. $\overline{BUSY_L}$ and $\overline{BUSY_R}$ outputs cannot be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY_L}$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY_R}$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_7 Left	D_0 - D_7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2942 tbl 17

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V06.

FUNCTIONAL DESCRIPTION

The IDT70V06 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V06 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT_L}$) is set when the right port writes to memory location 3FFE (HEX). The left port clears the interrupt by reading address location 3FFE. Likewise, the right port interrupt flag ($\overline{INT_R}$) is set when the left port writes to memory location 3FFF (HEX) and to clear the interrupt flag ($\overline{INT_R}$), the right port must read the memory location 3FFF. The message (8 bits) at 3FFE or 3FFF is user-defined. If the interrupt function is not used, address locations 3FFE and 3FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical

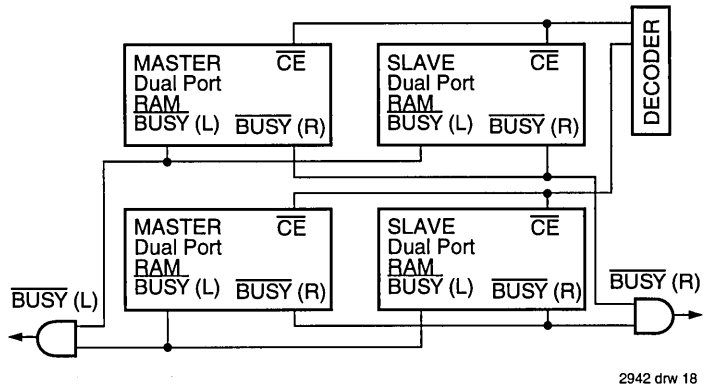


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70V06 RAMs.

operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 70V06 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT70V06 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT70V06 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with the R/$\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT70V06 is an extremely fast Dual-Port 16K x 8 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT70V06 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70V06's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70V06 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in

system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70V06 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

6

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT70V06's Dual-Port RAM. Say the 16K x 8 RAM was to be divided into two 8K x 8 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 8K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

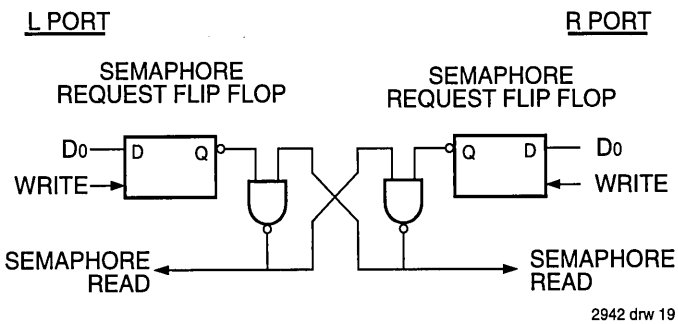
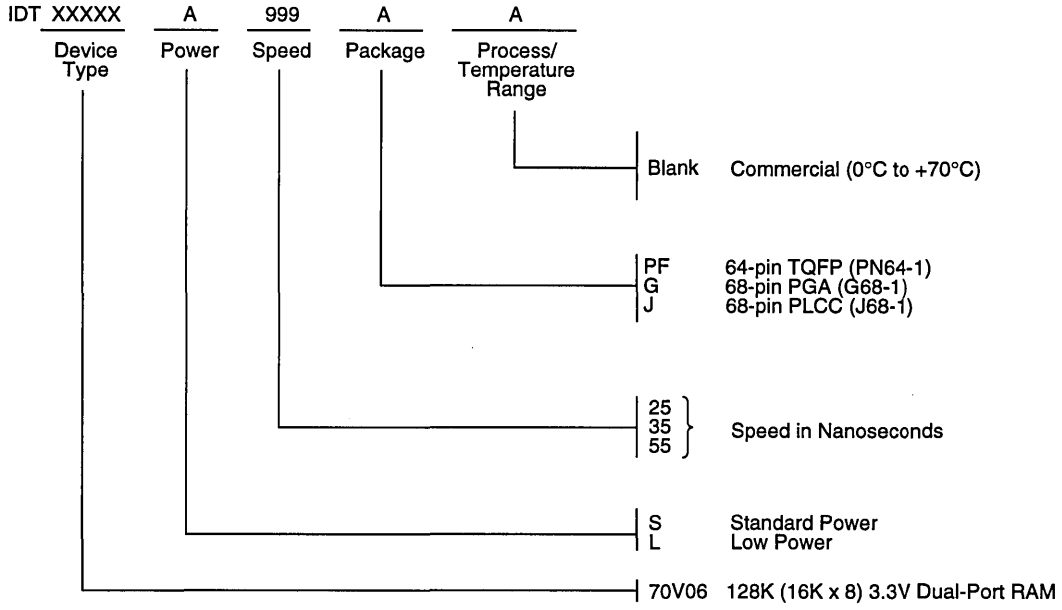


Figure 4. IDT70V06 Semaphore Logic

ORDERING INFORMATION



2942 drw 20

6

Integrated Device Technology, Inc.

HIGH-SPEED 3.3V 32K x 8 DUAL-PORT STATIC RAM

PRELIMINARY
IDT70V07S/L

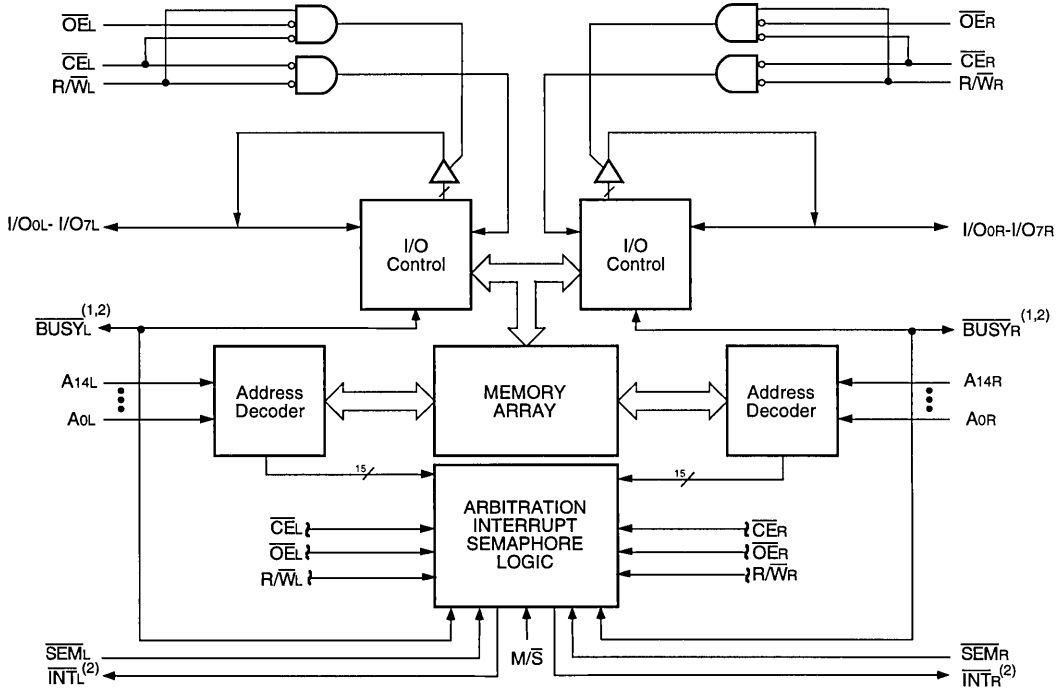
FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Commercial: 25/35/55ns (max.)
- Low-power operation
  - — IDT70V07S
    Active: 450mW (typ.)
    Standby: 5mW (typ.)
  - — IDT70V07L
    Active: 450mW (typ.)
    Standby: 5mW (typ.)
- IDT70V07 easily expands data bus width to 16 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Devices are capable of withstanding greater than 2001V electrostatic discharge
- TTL-compatible, single 3.3V (±0.3V) power supply
- Available in 68-pin PGA and PLCC, and a 64-pin TQFP

DESCRIPTION:

The IDT70V07 is a high-speed 32K x 8 Dual-Port Static RAM. The IDT70V07 is designed to be used as a stand-alone 256K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 16-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

FUNCTIONAL BLOCK DIAGRAM



2943 drw 01

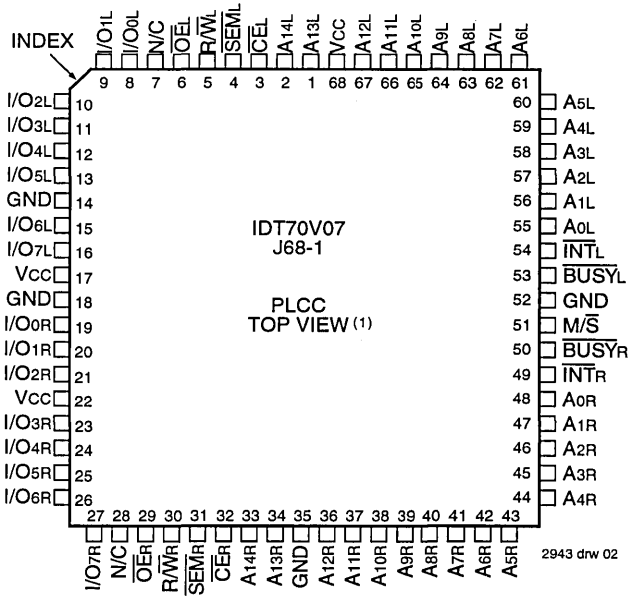
NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ and $\overline{INT}$ outputs are non-tri-stated push-pull.

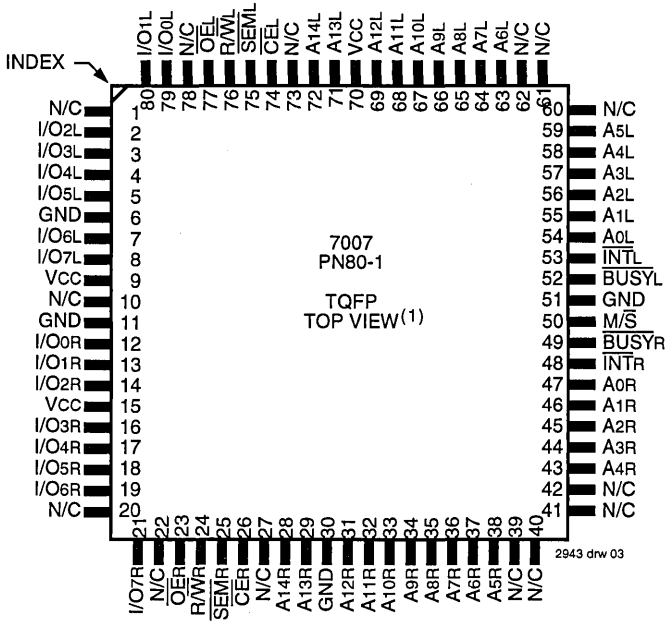
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 450mW of power.

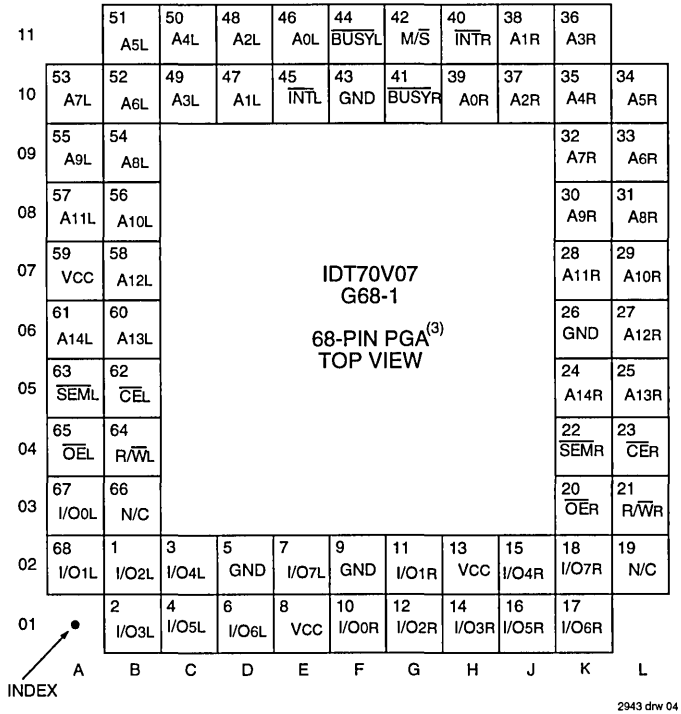
The IDT70V07 is packaged in a ceramic 68-pin PGA and PLCC and a 80-pin thin plastic quad flatpack (TQFP).

PIN CONFIGURATIONS





NOTE:
1. This text does not indicate orientation of the actual part-marking.



2943 drw 04

PIN NAMES (1,2)

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{14L}$	$A_{0R} - A_{14R}$	Address
$I/O_{0L} - I/O_{7L}$	$I/O_{0R} - I/O_{7R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2943 tbl 01

NOTES:
1. All V_{CC} pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	X	X	H	High-Z	Deselected: Power-Down
L	L	X	H	DATAIN	Write to Memory
L	H	L	H	DATAOUT	Read Memory
X	X	H	X	High-Z	Outputs Disabled

NOTE: 2943 tbl 02
1. $A_{0L} - A_{14L} \neq A_{0R} - A_{14R}$

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O0-7	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
H	↑	X	L	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	—	Not Allowed

2943 tbl 03

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTES: 2943 tbl 04
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq$ Vcc + 0.3V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V

2943 tbl 05

RECOMMENDED DC OPERATING CONDITIONS (2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	Vcc+0.3	V
V_{IL}	Input Low Voltage	–0.3(1)	—	0.8	V

NOTES: 2943 tbl 06
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.3V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

NOTE: 2943 tbl 07
1. This parameter is determined by device characterization but is not production tested. TQFP package only.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	IDT70V07S		IDT70V07L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2943 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V07X25		70V07X35		70V07X55		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L.	S	100	170	90	140	90	140	mA
				L	100	140	90	120	90	120	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L.	S	14	30	12	30	12	30	mA
				L	12	24	10	24	10	24	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5] Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L.	S	50	95	45	87	45	87	mA
				L	50	85	45	75	45	75	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	COM'L.	S	1.0	6	1.0	6	1.0	6	mA
				L	0.2	3	0.2	3	0.2	3	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{CC} - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open f = f_{MAX}[3]	COM'L.	S	60	90	55	85	55	85	mA
				L	60	80	55	74	55	74	

NOTES:

2943 tbl 09

1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 3.3V, T_A = +25°C, and are not production tested. I_{CCDC} = 80mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1 / t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2943 tbl 10

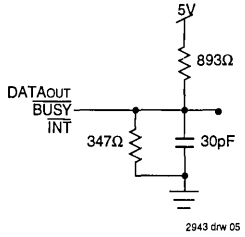


Figure 1. AC Output Test Load

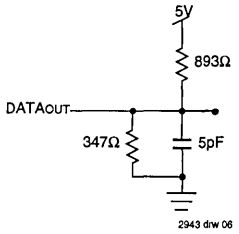


Figure 2. Output Test Load
(for tLZ, tHZ, twz, tow)
* Including scope and jig.

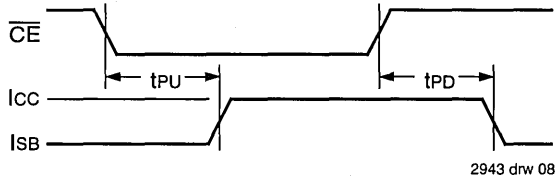
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

Symbol	Parameter	IDT70V07X25		IDT70V07X35		IDT70V07X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	25	—	35	—	55	—	ns
tAA	Address Access Time	—	25	—	35	—	55	ns
tACE	Chip Enable Access Time[3]	—	25	—	35	—	55	ns
tAOE	Output Enable Access Time	—	15	—	20	—	30	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time[1, 2]	3	—	3	—	3	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	20	—	25	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	25	—	35	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns
tSAA	Semaphore Address Access Time	—	35	—	45	—	65	ns

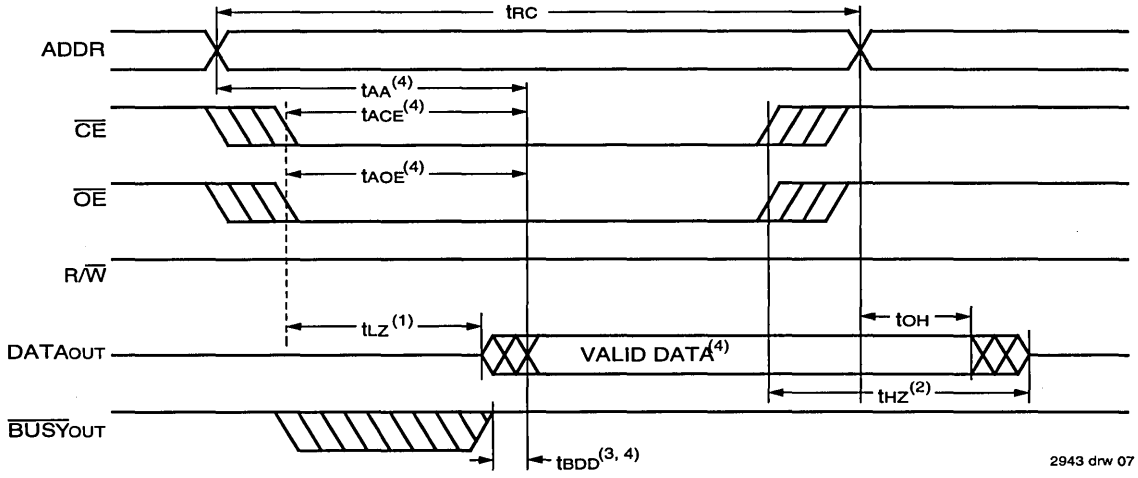
2943 tbl 11

NOTES:
1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL.
4. "X" in part numbers indicates power rating (S or L).

TIMING OF POWER-UP POWER-DOWN



WAVEFORM OF READ CYCLES[5]



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first, $\overline{CE}$ or $\overline{OE}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

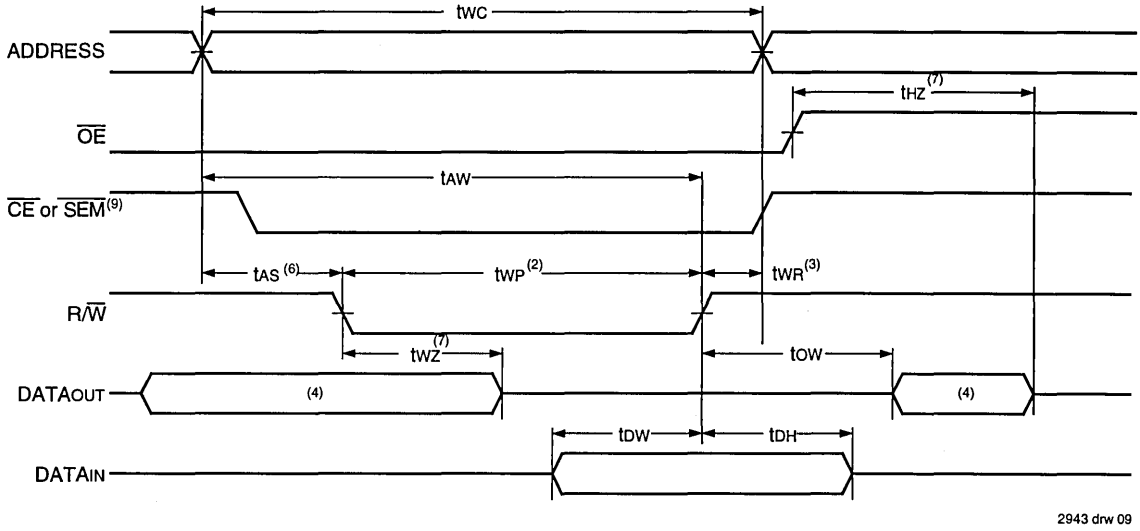
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[5]

		IDT70V07X25		IDT70V07X35		IDT70V07X55		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time	25	—	35	—	55	—	ns
tEW	Chip Enable to End-of-Write[3]	20	—	30	—	45	—	ns
tAW	Address Valid to End-of-Write	20	—	30	—	45	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	20	—	30	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	20	—	25	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	15	—	20	—	25	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

2943 tbl 12

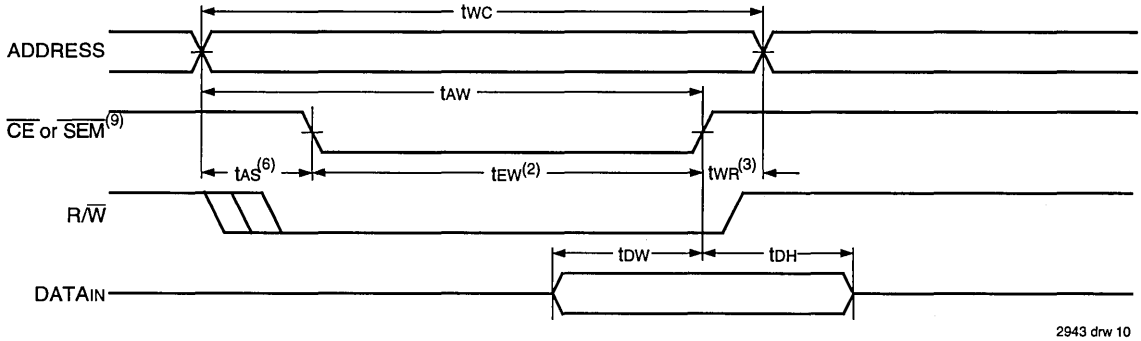
NOTES:
1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,5,8)



2943 drw 09

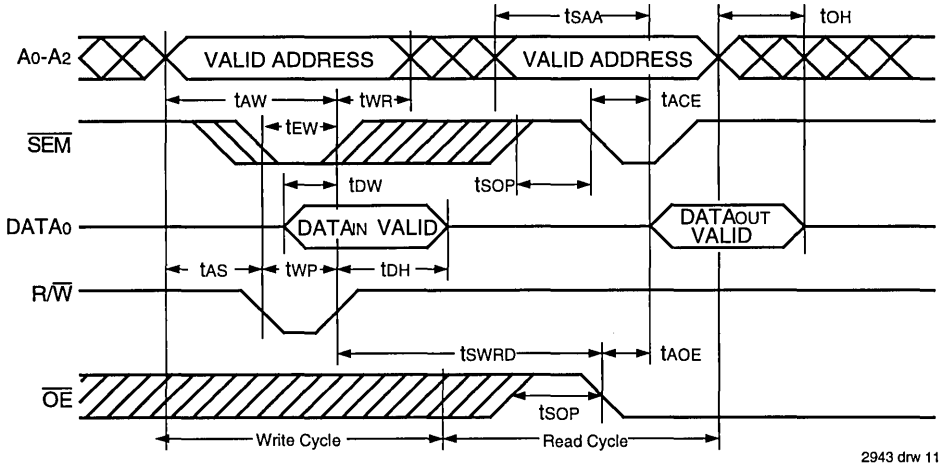
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,5)



2943 drw 10

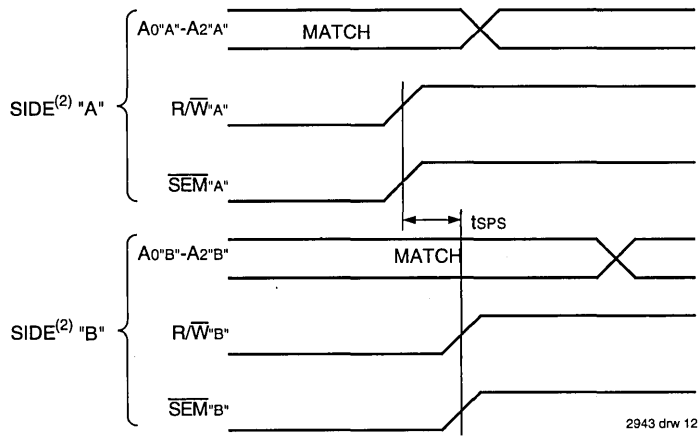
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a LOW $\overline{CE}$ and a LOW R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured ± 200mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. tEW must be met for either condition.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}_R$ = $\overline{CE}_L$ = VIH.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}_A$ or $\overline{SEM}_A$ going HIGH to R/$\overline{W}_B$ or $\overline{SEM}_B$ going HIGH.
4. If tSPS is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

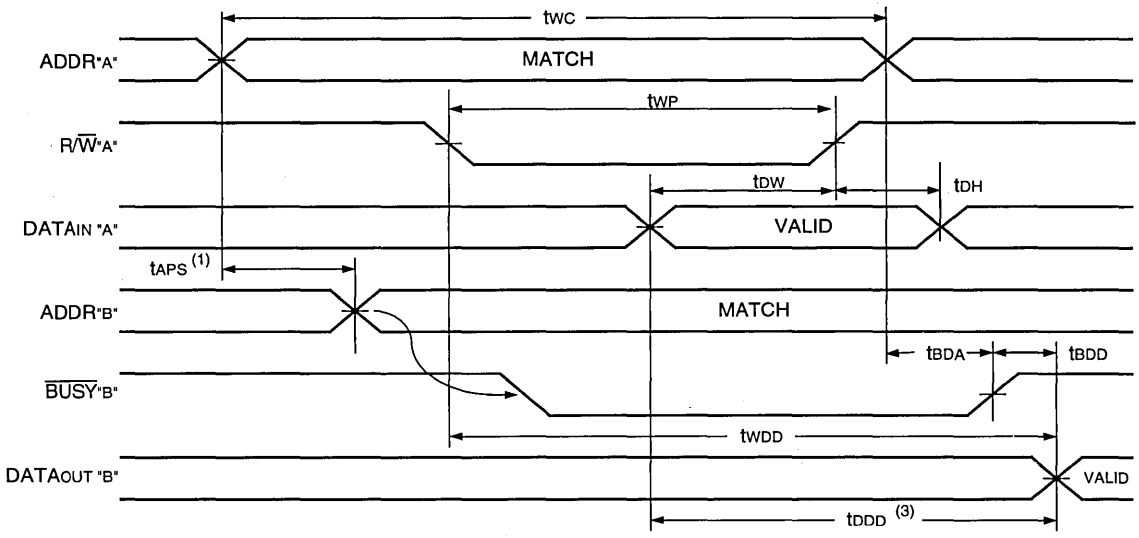
Symbol	Parameter	IDT70V07X25		IDT70V07X35		IDT70V07X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/$\overline{S}$ = VIH)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	25	—	35	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	25	—	35	—	45	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	25	—	35	—	45	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	25	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	25	—	35	—	55	ns
BUSY TIMING (M/$\overline{S}$ = VIL)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	20	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	55	—	65	—	85	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	50	—	60	—	80	ns

2943 tbl 13

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. "X" in part numbers indicates power rating (S or L).

6

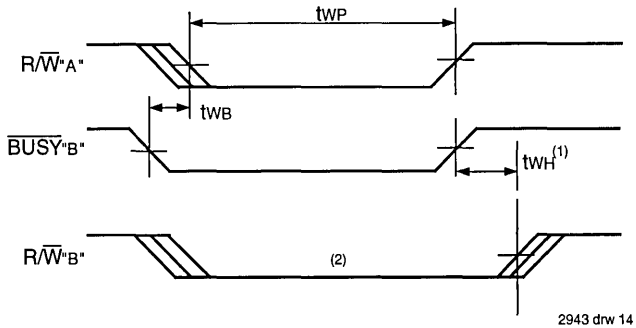
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$ (2,5)



2943 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins. t_{APS} is ignored for $M/\overline{S}$ = V_{IL} (SLAVE).
2. $\overline{CE}_L$ = $\overline{CE}_R$ = V_{IL}
3. $\overline{OE}$ = V_{IL} for the reading port.
4. If $M/\overline{S}$ = V_{IL} (SLAVE), then $\overline{BUSY}$ is an input ($\overline{BUSY}$"A" = V_{IH} and $\overline{BUSY}$"B" = "don't care", for this example).
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

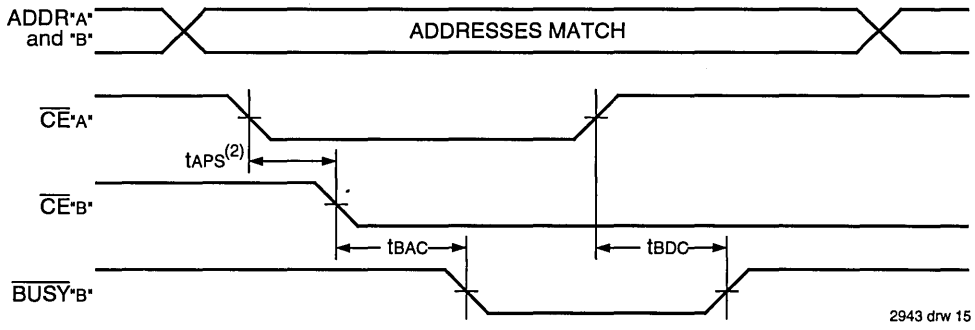
TIMING WAVEFORM OF WRITE WITH BUSY



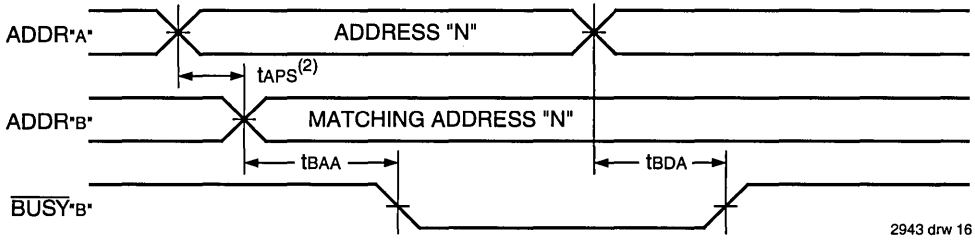
2943 drw 14

NOTES:
1. t_{WH} must be met for both $\overline{BUSY}$ input (SLAVE) and output (MASTER).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes High.

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING[1]



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING[1]



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or the other, but there is no guarantee on which side busy will be asserted.

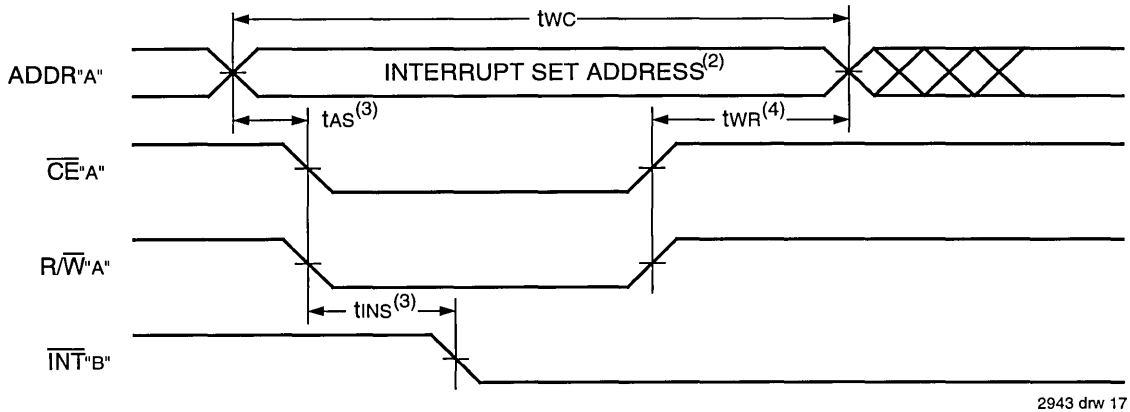
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

Symbol	Parameter	IDT70V07X25 Min.	IDT70V07X25 Max.	IDT70V07X35 Min.	IDT70V07X35 Max.	IDT70V07X55 Min.	IDT70V07X55 Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	30	—	40	ns
tINR	Interrupt Reset Time	—	30	—	35	—	45	ns

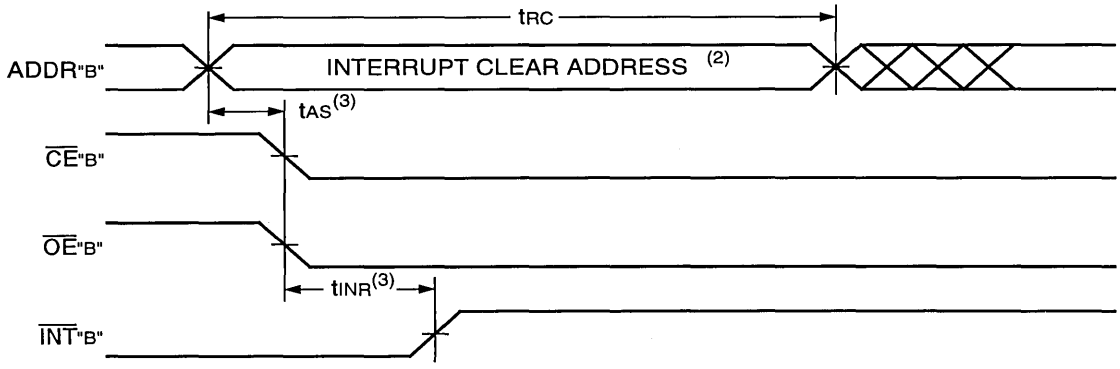
NOTE:
1. "X" in part numbers indicates power rating (S or L).

2942 tbl 14

WAVEFORM OF INTERRUPT TIMING[1]



2943 drw 17



2943 drw 18

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{14L}-A_{0L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{14R}-A_{0R}	$\overline{INT}_R$	Function
L	L	X	7FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	7FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = V_{IH}.
2. If $\overline{BUSY}_L$ = V_{IL}, then no change.
3. If $\overline{BUSY}_R$ = V_{IL}, then no change.

2942 tbl 15

TRUTH TABLE I — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{14L} A_{0R}-A_{14R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

2943 tbl 16

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$ outputs on the IDT7007 are push-pull, not open drain outputs. On slaves the $\overline{BUSY}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

TRUTH TABLE II — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_7 Left	D_0 - D_7 Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

2943 tbl 17

NOTE:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V07.

FUNCTIONAL DESCRIPTION

The IDT70V07 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V07 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FFE (HEX), where a write is defined as $\overline{CE}$ = R/$\overline{W}$ = V_{IL} per the Truth Table. The left port clears the interrupt through access of address location 7FFE when $\overline{CE}_R$ = $\overline{OE}_R$ = V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory 7FFF location 7FFF. The message (8 bits) at 7FFE or 7FFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FFE and 7FFF are not used as mail boxes, but as part of the random access memory. Refer to Table 1 for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical

operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 70V07 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT70V07 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a

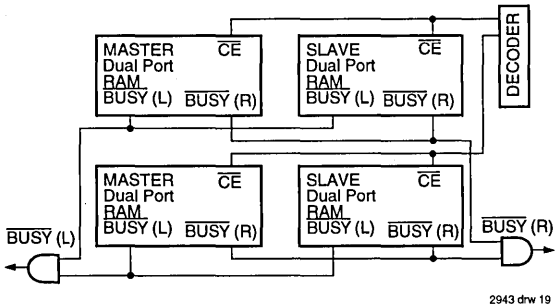


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70V07 RAMs.

write inhibit signal. Thus on the IDT70V07 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with the R/$\overline{W}$ signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT70V07 is an extremely fast Dual-Port 32K x 8 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT70V07 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70V07's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70V07 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that

semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70V07 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must

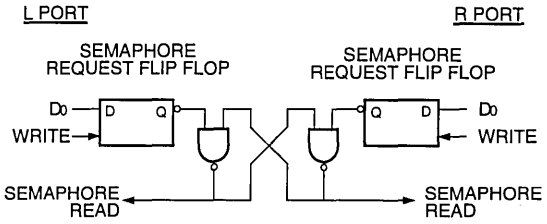


Figure 4. IDT70V07 Semaphore Logic

be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT70V07's Dual-Port RAM. Say the 32K x 8 RAM was to be divided into two 16K x 8 blocks which were to be dedicated at any one time to

servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 16K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 16K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 16K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 16K blocks of Dual-Port RAM with each other.

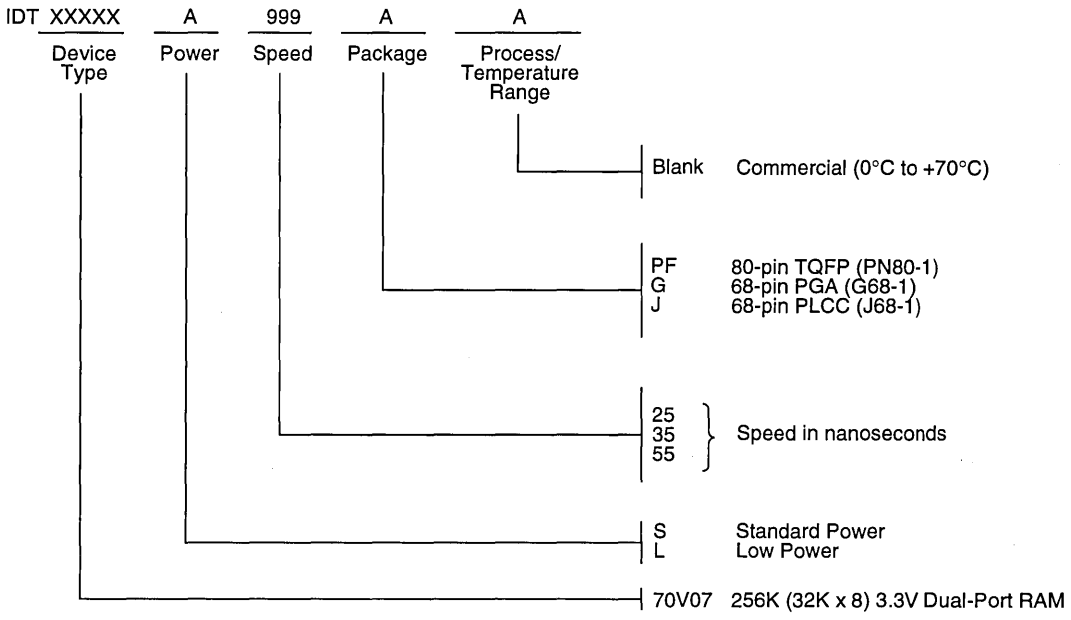
The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

ORDERING INFORMATION



2943 drw 22

6

Integrated Device Technology, Inc.

HIGH-SPEED 3.3V 4K x 16 DUAL-PORT STATIC RAM

PRELIMINARY
IDT70V24S/L

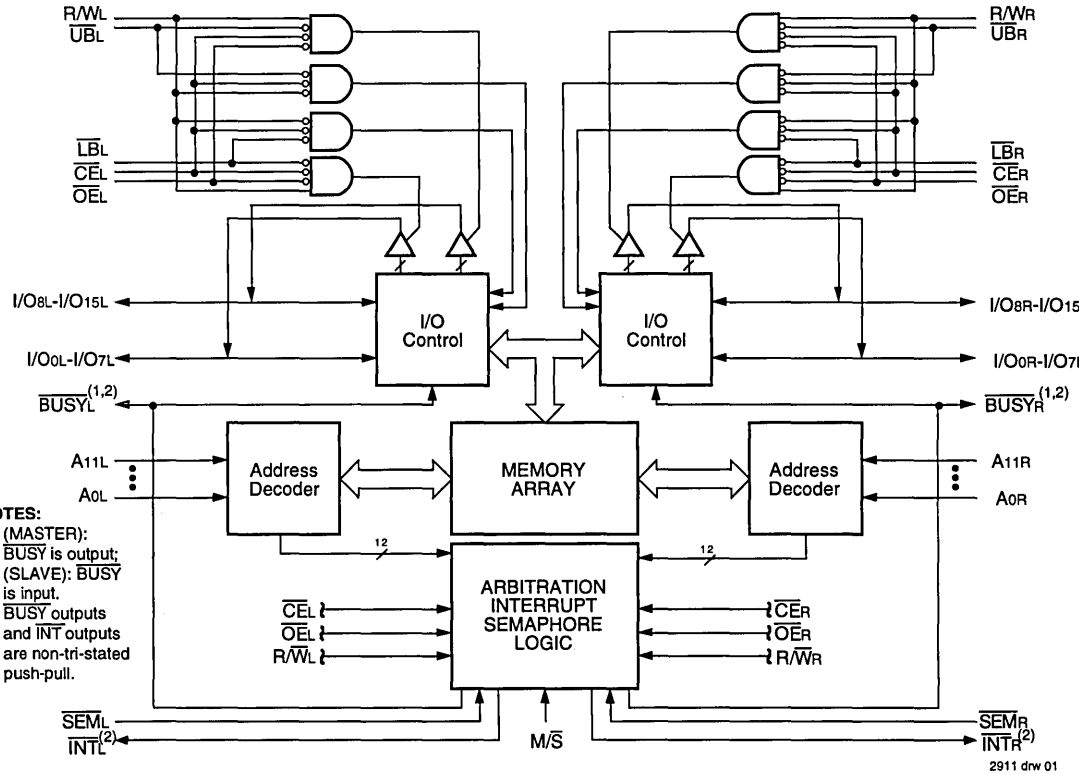
FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Commercial: 25/35/55ns (max.)
- Low-power operation
  - — IDT70V24S
    Active: 230mW (typ.)
    Standby: 3.3mW (typ.)
  - — IDT70V24L
    Active: 230mW (typ.)
    Standby: .66mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT70V24 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- Devices are capable of withstanding greater than 2001V electrostatic charge.
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- TTL-compatible, single 3.3V (±0.3V) power supply
- Available in 84-pin PGA, PLCC and 100-pin TQFP

DESCRIPTION:

The IDT70V24 is a high-speed 4K x 16 Dual-Port Static RAM. The IDT70V24 is designed to be used as a stand-alone 64K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit-or-more word systems. Using the

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.

2911 drw 01

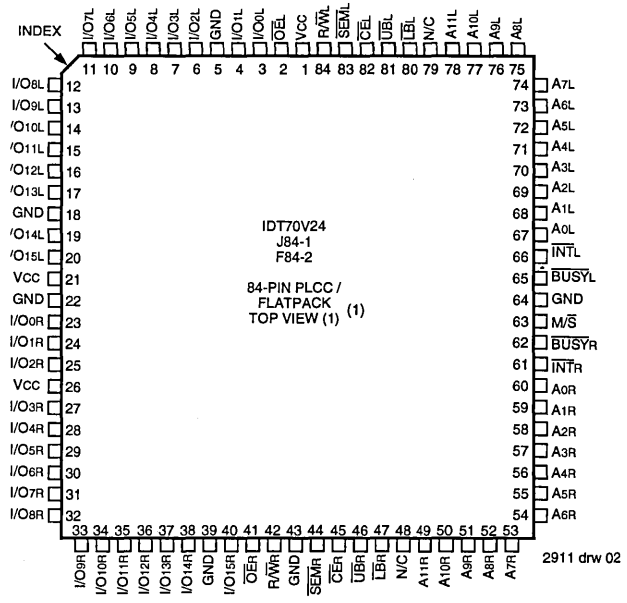
IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

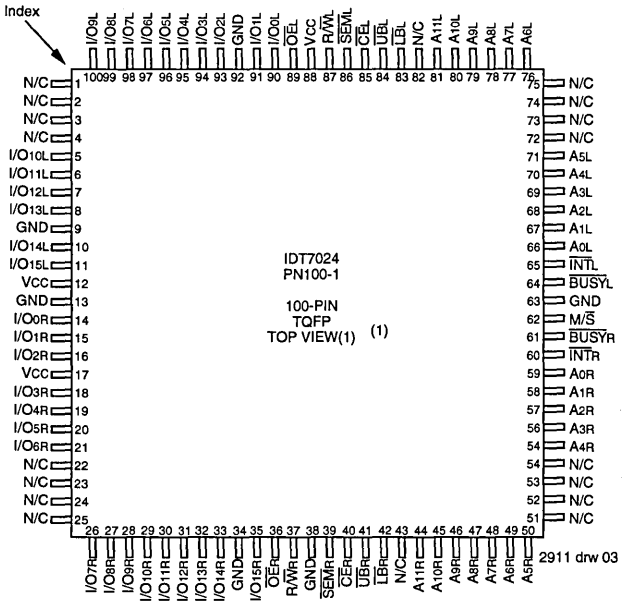
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS™ high-performance technology, these devices typically operate on only 350mW of power.

The IDT70V24 is packaged in a ceramic 84-pin PGA, an 84-Pin PLCC and a 100-pin Thin Quad Plastic Flatpack.

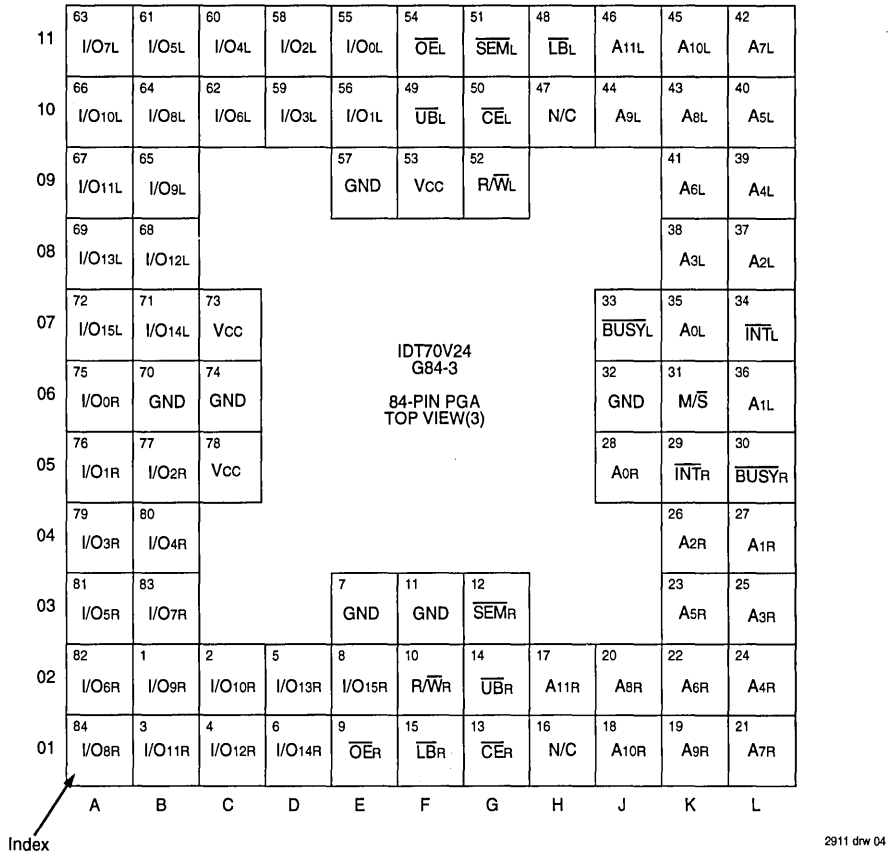
PIN CONFIGURATIONS





NOTE:
1. This text does not indicate the actual part-marking.

6



PIN NAMES[1,2]

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{11L}$	$A_{0R} - A_{11R}$	Address
$I/O_{0L} - I/O_{15L}$	$I/O_{0R} - I/O_{15R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
M/$\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

2911 tbl 1

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate the actual part-marking.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power Down
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	H	DATAIN	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	HighZ	High-Z	Outputs Disabled

NOTE: 2911 tbl 02

1. $A_{0L} — A_{11L} \neq A_{0R} — A_{11R}$

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
H	↓	X	X	X	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
X	↓	X	H	H	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

2911 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2911 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc +0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20ma for the period over $V_{TERM} \geq$ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military			
Commercial	0°C to +70°C	0V	3.3V ± 0.3

2911 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3[1]	—	0.8	V

NOTE: 2911 tbl 06

1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (TA = +25°C, F = 1.0MHZ) TQFP Pkg. Only

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	11	pF

NOTE: 2911 tbl 07

1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

6

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	IDT70V24S		IDT70V24L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2911 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V24X25		70V24X35		70V24X55		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM	S	80	140	70	115	70	115	mA
				L	80	120	70	100	70	100	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM	S	12	25	10	25	10	25	mA
				L	10	20	8	20	8	20	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_{"A"}$=V_{IL} and $\overline{CE}_{"B"}$=V_{IH}[5] Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM	S	40	82	35	72	35	72	mA
				L	40	72	35	62	35	62	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC}-0.2V	COM	S	1.0	5	1.0	5	1.0	5	mA
				L	0.2	2.5	0.2	2.5	0.2	2.5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2 and $\overline{CE}_{"B"}$ ≥ V_{CC} - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC}-0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[3]	COM	S	50	81	45	71	45	71	mA
				L	50	71	45	61	45	61	

NOTES:

2911 tbl 09

1. 'X' in part numbers indicates power rating (S or L)
2. V_{CC} = 3.3V, T_A = +25°C, and are not production tested. $I_{CC\,DC}$ = 70mA (TYP.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2911 tbl 10

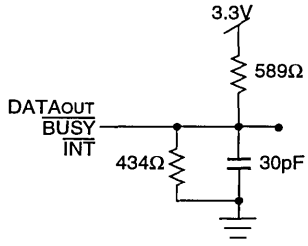


Figure 1. Output Test Load
(for tLZ, tHZ, twz, tow)

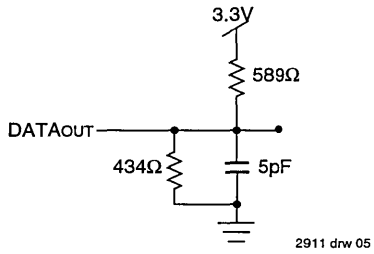


Figure 2. Output Test Load
(for tLZ, tHZ, twz, tow)
*** Including scope and jig.**

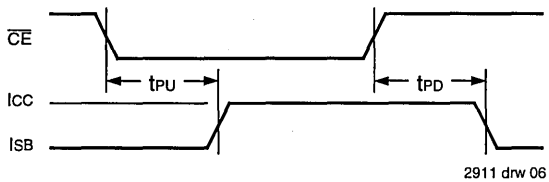
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

		IDT70V24X25		IDT70V24X35		IDT70V24X55		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	25	—	35	—	55	—	ns
tAA	Address Access Time	—	25	—	35	—	55	ns
tACE	Chip Enable Access Time[3]	—	25	—	35	—	55	ns
tABE	Byte Enable Access Time[3]	—	25	—	35	—	55	ns
tAOE	Output Enable Access Time	—	15	—	20	—	30	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time[1, 2]	3	—	3	—	3	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	20	—	25	ns
tPU	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time[2]	—	25	—	35	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns
tSAA	Semaphore Address Access Time	—	35	—	45	—	65	ns

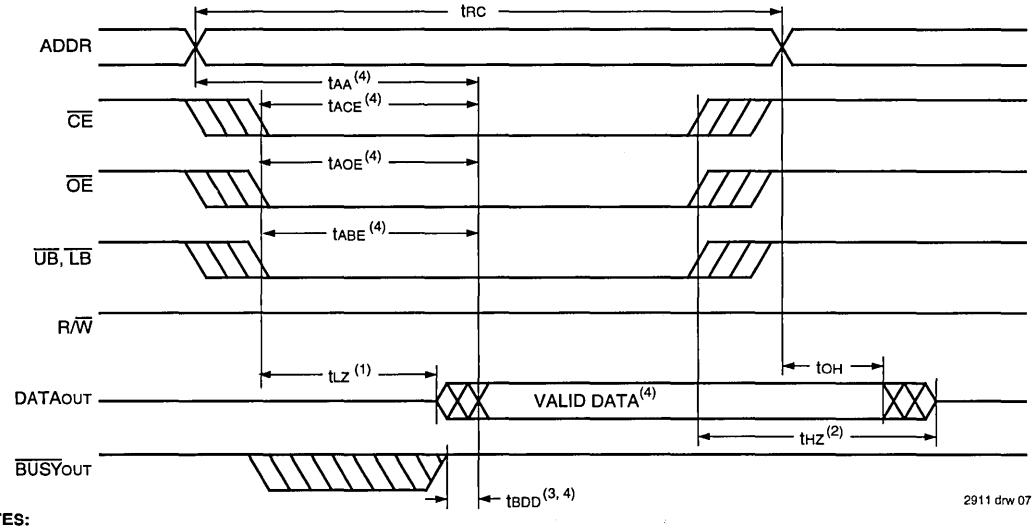
2911 tbl 11

NOTES:
1. Transition is measured ±200mV from low or high impedance voltage with load (figures 1 and 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{UB}$ or $\overline{LB}$ = VIL, and $\overline{SEM}$ = VI. To access semaphore, $\overline{CE}$ = VIH or $\overline{UB}$ and $\overline{LB}$ = VIH, and $\overline{SEM}$ = VIL.
4. "X" in part numbers indicates power rating (S or L).

TIMING OF POWER-UP POWER-DOWN



WAVEFORM OF READ CYCLES[5]



NOTES:
1. Timing depends on which signal is asserted last, OE, CE, LB, or UB.
2. Timing depends on which signal is de-asserted firs CE, OE, LB, or UB.
3. tBDD delay is required only in cases where opposite port is completing a write operation to the same address location. For simultaneous read operations BUSY has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tABE, tAOE, tACE, tAA or tBDD.
5. SEM = VIH.

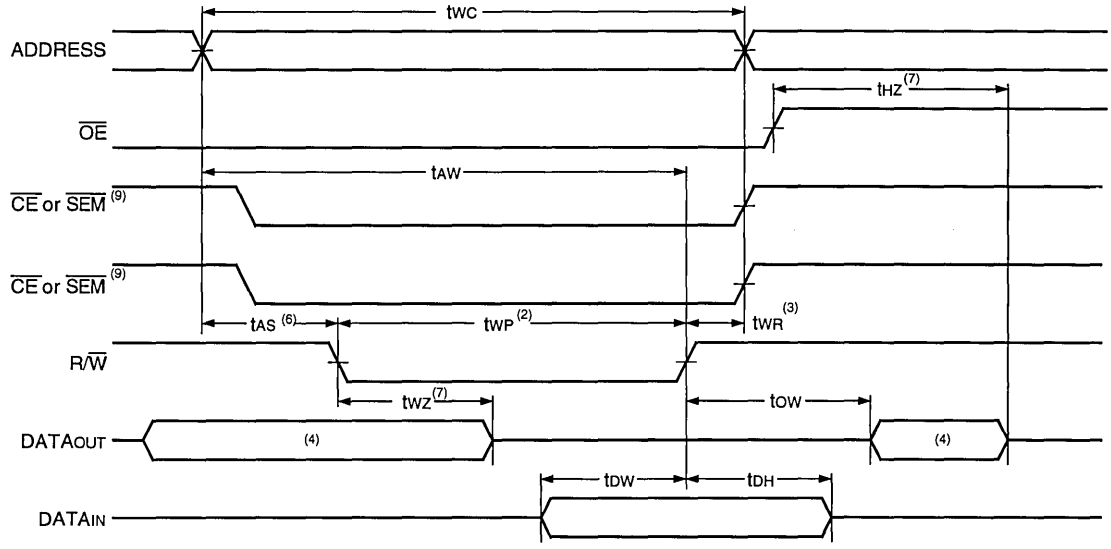
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[5]

Symbol	Parameter	IDT70V24X25 Min.	IDT70V24X25 Max.	IDT70V24X35 Min.	IDT70V24X35 Max.	IDT70V24X55 Min.	IDT70V24X55 Max.	Unit
WRITE CYCLE								
tWC	Write Cycle Time	25	—	35	—	55	—	ns
tEW	Chip Enable to End-of-Write[3]	20	—	30	—	45	—	ns
tAW	Address Valid to End-of-Write	20	—	30	—	45	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	20	—	30	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	20	—	25	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	15	—	20	—	25	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	SEM Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	SEM Flag Contention Window	5	—	5	—	5	—	ns

NOTES:
2911 tbl 12

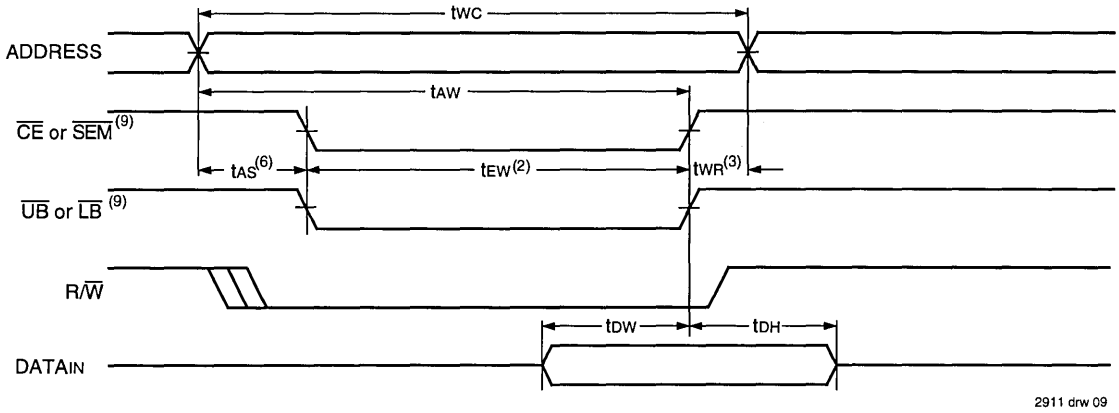
1. Transition is measured ±200mV from low or high impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, CE = VIL, UB or LB = VIL, SEM = VIH. To access semaphore, CE = VIH and SEM = VIL. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tow values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tow.
5. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,5,8)



2911 drw 08

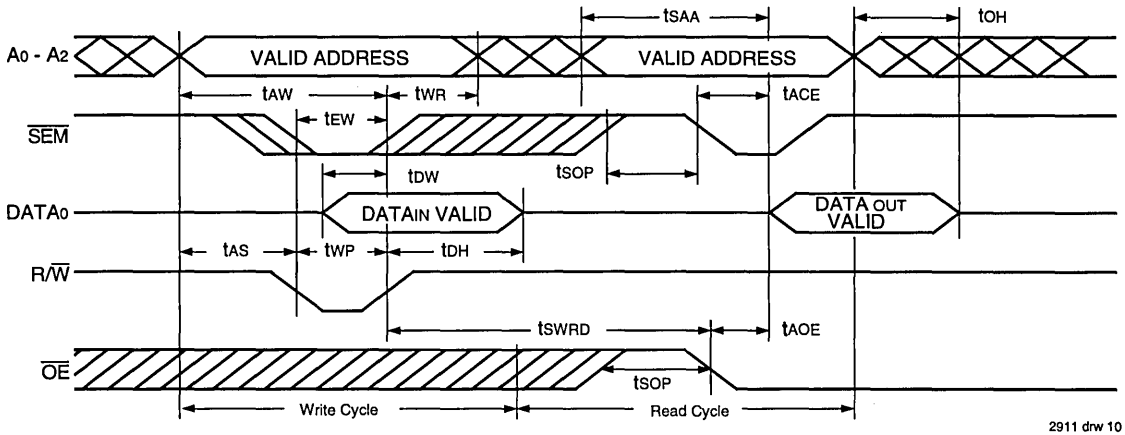
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING(1,5)



2911 drw 09

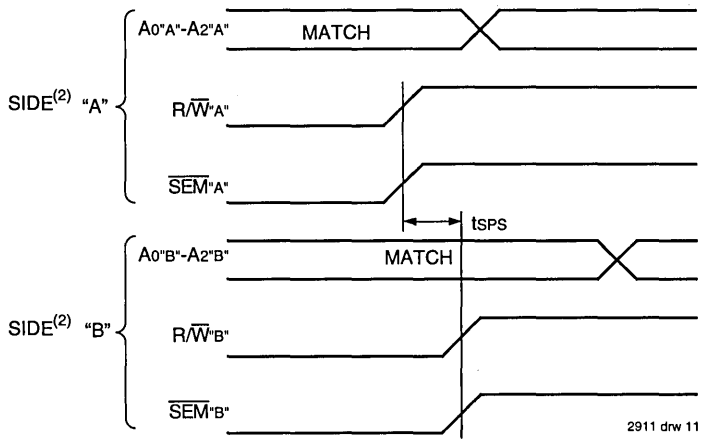
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ & $\overline{LB}$ must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{UB}$ or $\overline{LB}$ and a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, R/$\overline{W}$ or byte control.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured ±200mV from low or high impedance voltage with Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ = VIL, $\overline{UB}$ or $\overline{LB}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}_R$ = $\overline{CE}_L$ = VIH, or Both $\overline{UB}$ & $\overline{LB}$ = VIH Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from R/$\overline{W}_A$ or $\overline{SEM}_A$ going high to R/$\overline{W}_B$ or $\overline{SEM}_B$ going high.
4. If tSPS is not satisfied, the semaphore will fall positively to one side or the other, but there is not guarantee which side will obtain the flag.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	IDT70V24X35 Min.	IDT70V24X35 Max.	IDT70V24X55 Min.	IDT70V24X55 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)						
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	35	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	35	—	45	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Low	—	35	—	45	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip High	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	Note 3	—	Note 3	ns
BUSY TIMING (M/$\overline{S}$ = L)						
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING						
tWDD	Write Pulse to Data Delay[1]	—	65	—	85	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	60	—	80	ns

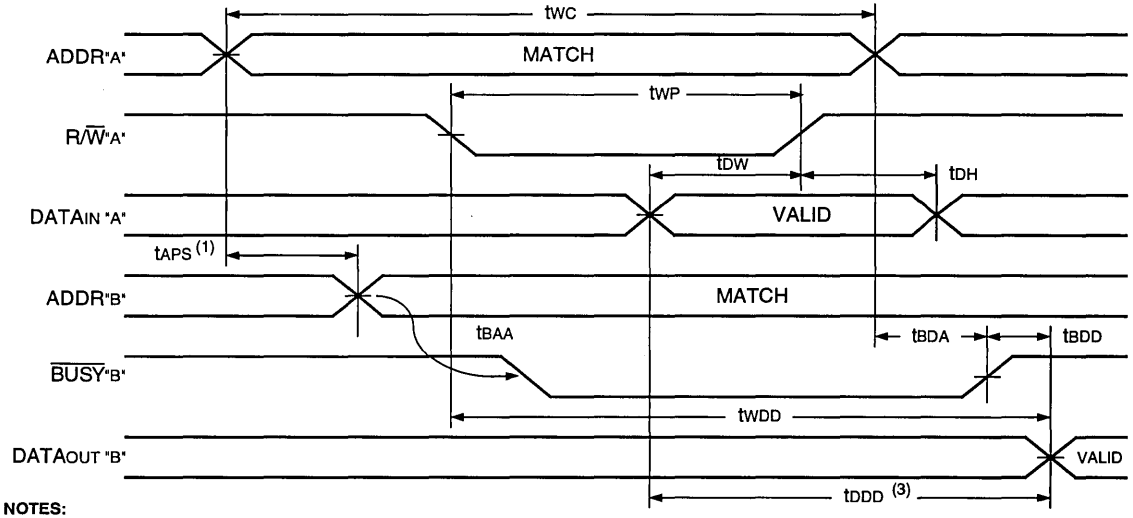
NOTES:

2740 tbl 13

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Read With $\overline{BUSY}$ (M / $\overline{S}$ = H)" or "Timing Waveform of Write With Port-To-Port Delay (M / $\overline{S}$ = L)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0ns, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port 'B' during contention with port 'A'.
5. To ensure that a write cycle is completed on port 'B' after contention with port 'A'.
6. "X" in part numbers indicates power rating (S or L).

6

TIMING WAVEFORM OF READ WITH $\overline{BUSY}$[2] (M/$\overline{S}$ = H)

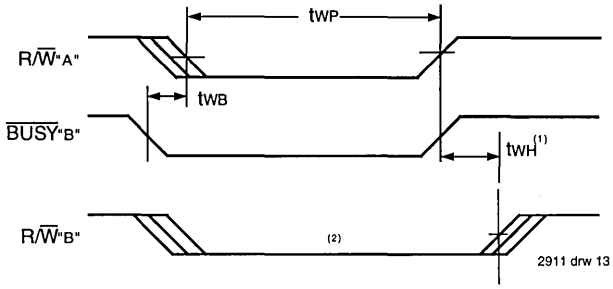


NOTES:

2911 drw 12

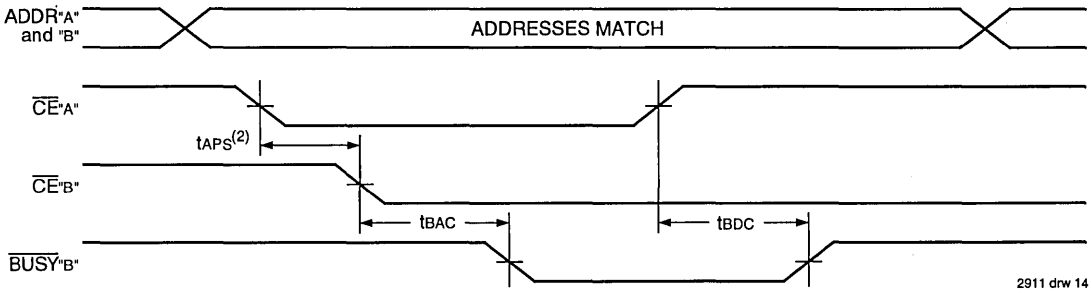
1. To ensure that the earlier of the two ports wins. tAPS is ignored for M/$\overline{S}$ = VIL (SLAVE).
2. $\overline{CEL}$ = $\overline{CER}$ = VIL.
3. $\overline{OE}$ = VIL for the reading port.
4. If M/$\overline{S}$ = VIL(slave) then $\overline{BUSY}$ is an input $\overline{BUSY}$"A" = VIL and $\overline{BUSY}$"B" = don't care, for this example.
5. All timing is the same for both left and right ports. Port "A" may be either the left or right Port. Port "B" is the port opposite from port "A".

TIMING WAVEFORM OF SLAVE WRITE (M/$\overline{S}$ = L)

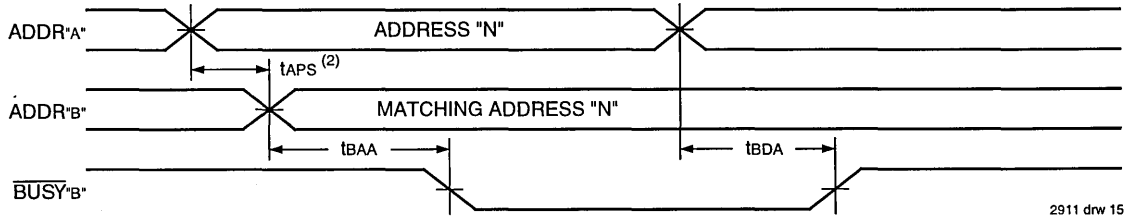


Note:
1. tWH must be met for both BUSY input (slave) and output (master).
2. Busy is asserted on port "B" Blocking R/W"B", until BUSY"B" goes High.

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1) (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)(M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

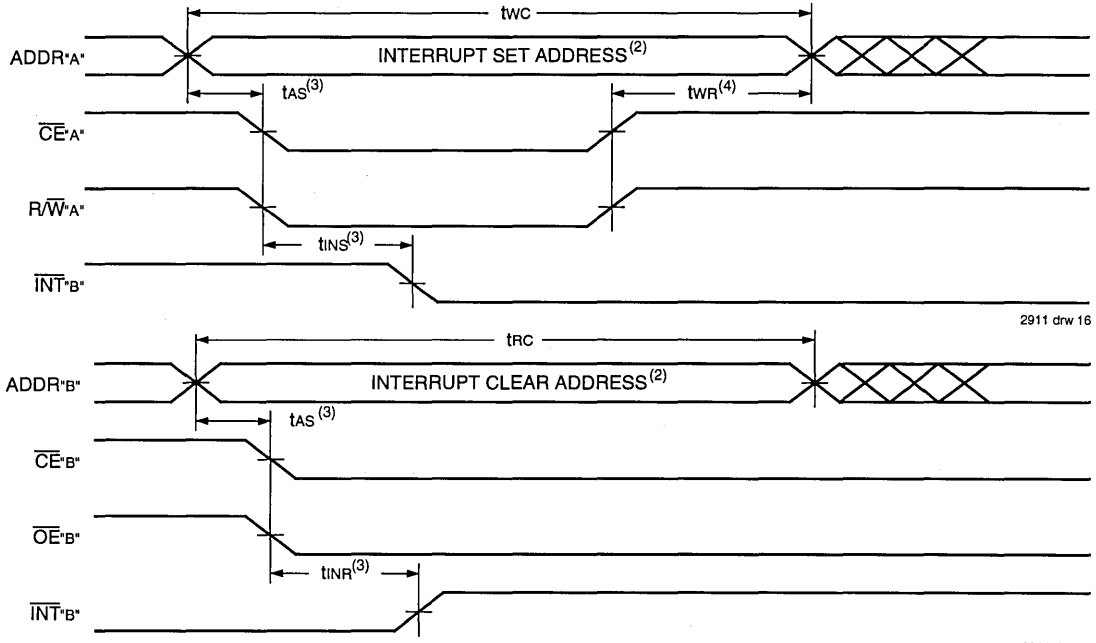
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

Symbol	Parameter	IDT70V24X35 Min.	IDT70V24X35 Max.	IDT70V24X55 Min.	IDT70V24X55 Max.	Unit
INTERRUPT TIMING						
tAS	Address Set-up Time	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tINS	Interrupt Set Time	—	30	—	40	ns
tINR	Interrupt Reset Time	—	35	—	45	ns

NOTE:
1. "X" in part numbers indicates power rating (S or L).

2911 tbl 14

WAVEFORM OF INTERRUPT TIMING[1]



2911 drw 16

2911 drw 17

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					
R/$\overline{W}$L	$\overline{CE}$L	$\overline{OE}$L	A11L-A0L	$\overline{INT}$L	R/$\overline{W}$R	$\overline{CE}$R	$\overline{OE}$R	A11R-A0R	$\overline{INT}$R	Function
L	L	X	FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}$R Flag
X	X	X	X	X	X	L	L	FFF	H[3]	Reset Right $\overline{INT}$R Flag
X	X	X	X	L[3]	L	L	X	FFE	X	Set Left $\overline{INT}$L Flag
X	L	L	FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}$L Flag

NOTES:
1. Assumes $\overline{BUSY}$L = $\overline{BUSY}$R = VIH.
2. If $\overline{BUSY}$L = VIL, then no change.
3. If $\overline{BUSY}$R = VIL, then no change.

2911 tbl 15

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{11L} A_{0R}-A_{11R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

NOTES:

2911 tbl 16

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$ outputs on the IDT70V24 are push pull, not open drain outputs. On slaves the $\overline{BUSY}$ input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_{15} Left	D_0 - D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE:

2911 tbl 17

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V24.

FUNCTIONAL DESCRIPTION

The IDT70V24 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V24 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location FFE (HEX), where a write is defined as the $\overline{CE}$=R/$\overline{W}$=V_{IL} per the Truthe Table. The left port clears the interrupt by accessing address location FFE when $\overline{CE}_R$=$\overline{OE}_R$=V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location FFF. The message (16 bits) at FFE or FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations FFE and FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all

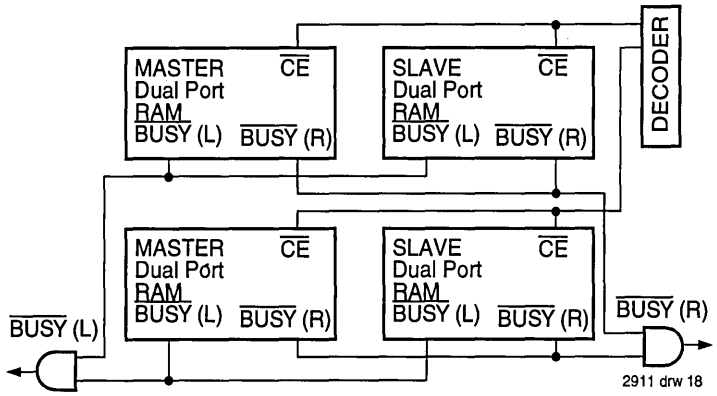


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70V24 RAMs.

applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 70V24 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT70V24 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT70V24 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT70V24 is an extremely fast Dual-Port 4K x 16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT70V24 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70V24's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources

6

to be allocated in varying configurations. The IDT70V24 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70V24 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a

resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT70V24's Dual-Port RAM. Say the 4K x 16 RAM was to be divided into two 2K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 2K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 2K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 2K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 2K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

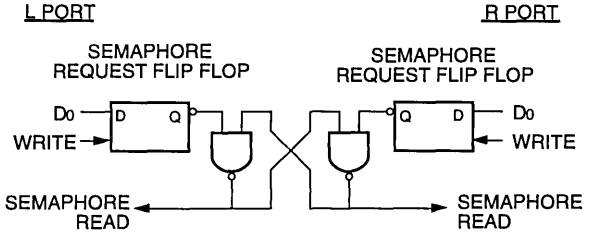
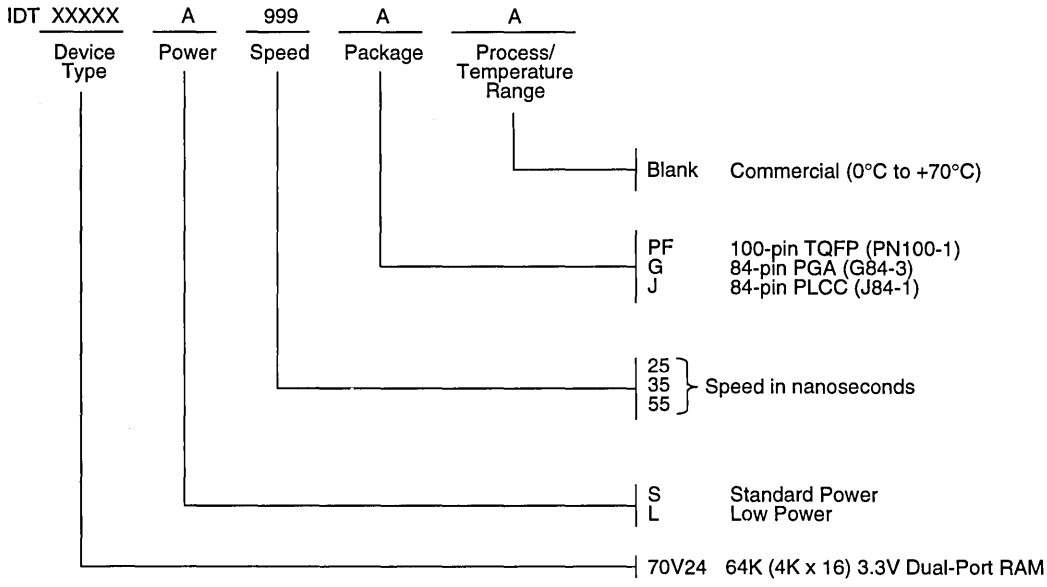


Figure 4. IDT70V24 Semaphore Logic

ORDERING INFORMATION



2911 drw 20

Integrated Device Technology, Inc.

HIGH-SPEED 3.3V 8K x 16 DUAL-PORT STATIC RAM

PRELIMINARY
IDT70V25S/L

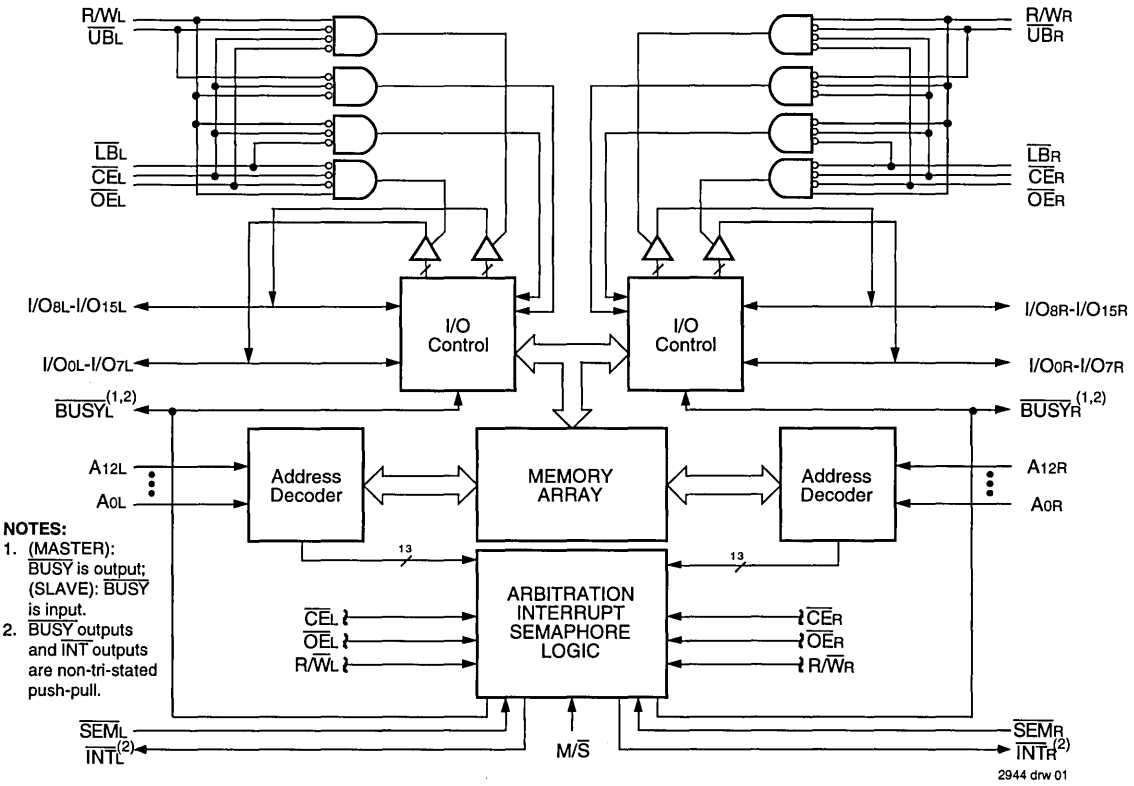
FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  — Commercial: 25/35/55ns (max.)
- Low-power operation
  — IDT70V25S
    Active: 230mW (typ.)
    Standby: 3.3mW (typ.)
  — IDT70V25L
    Active: 230mW (typ.)
    Standby: .66mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT70V25 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- Devices are capable of withstanding greater than 2001V electrostatic charge.
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- TTL-compatible, single 3.3V (±0.3V) power supply
- Available in 84-pin PGA, PLCC and 100-pin TQFP

DESCRIPTION:

The IDT70V25 is a high-speed 8K x 16 Dual-Port Static RAM. The IDT70V25 is designed to be used as a stand-alone 128K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit-or-more word systems.

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.

2944 drw 01

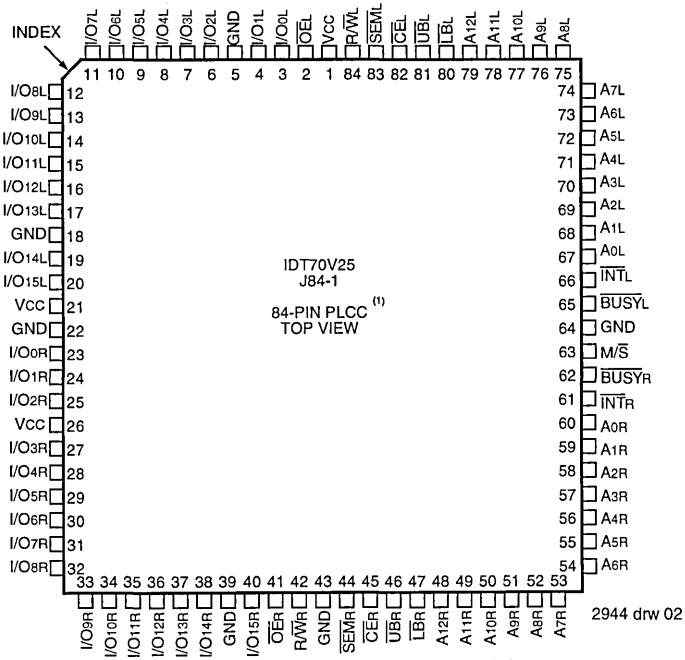
Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

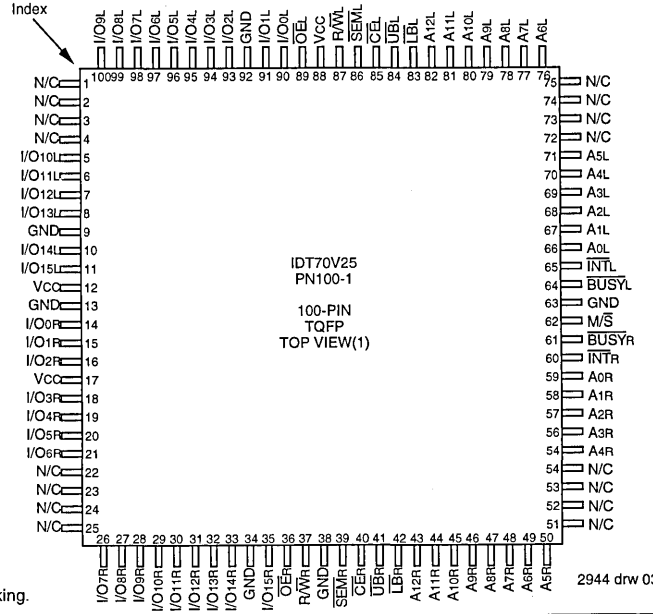
Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 350mW of power.

The IDT70V25 is packaged in a ceramic 84-pin PGA, an 84-Pin PLCC and a 100-pin Thin Quad Plastic Flatpack.

PIN CONFIGURATIONS

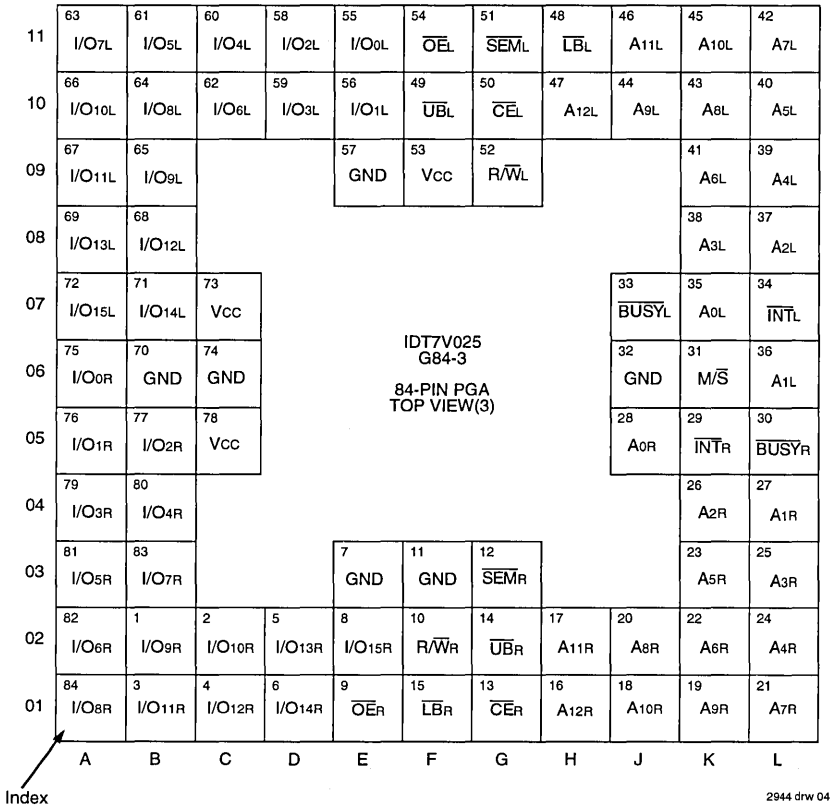


2944 drw 02



2944 drw 03

NOTE:
1. This text does not indicate orientation of the actual part- marking.



	A	B	C	D	E	F	G	H	J	K	L
11	63 I/O7L	61 I/O5L	60 I/O4L	58 I/O2L	55 I/O0L	54 $\overline{OE}_L$	51 $\overline{SEM}_L$	48 $\overline{LB}_L$	46 A11L	45 A10L	42 A7L
10	66 I/O10L	64 I/O8L	62 I/O6L	59 I/O3L	56 I/O1L	49 $\overline{UB}_L$	50 $\overline{CE}_L$	47 A12L	44 A9L	43 A8L	40 A5L
09	67 I/O11L	65 I/O9L			57 GND	53 Vcc	52 R/$\overline{W}_L$			41 A6L	39 A4L
08	69 I/O13L	68 I/O12L								38 A3L	37 A2L
07	72 I/O15L	71 I/O14L	73 Vcc						33 $\overline{BUSY}_L$	35 A0L	34 $\overline{INT}_L$
06	75 I/O0R	70 GND	74 GND						32 GND	31 M/$\overline{S}$	36 A1L
05	76 I/O1R	77 I/O2R	78 Vcc						28 A0R	29 $\overline{INT}_R$	30 $\overline{BUSY}_R$
04	79 I/O3R	80 I/O4R								26 A2R	27 A1R
03	81 I/O5R	83 I/O7R			7 GND	11 GND	12 $\overline{SEM}_R$			23 A5R	25 A3R
02	82 I/O6R	1 I/O9R	2 I/O10R	5 I/O13R	8 I/O15R	10 R/$\overline{W}_R$	14 $\overline{UB}_R$	17 A11R	20 A8R	22 A6R	24 A4R
01	84 I/O8R	3 I/O11R	4 I/O12R	6 I/O14R	9 $\overline{OE}_R$	15 $\overline{LB}_R$	13 $\overline{CE}_R$	16 A12R	18 A10R	19 A9R	21 A7R

PIN NAMES(1,2)

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A0L – A12L	A0R – A12R	Address
I/O0L – I/O15L	I/O0R – I/O15R	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
M/$\overline{S}$		Master or Slave Select
Vcc		Power
GND		Ground

2944 tbl 01

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part- marking.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power Down
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	H	DATAIN	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

NOTE: 2944 tbl 02

1. $A_{0L} — A_{12L} \neq A_{0R} — A_{12R}$

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
H	↑	X	X	X	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
X	↑	X	H	H	L	DATAIN	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

2944 tbl 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2944 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.5V for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq$ 20 mA for the period over $V_{TERM} \geq$ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military			
Commercial	0°C to +70°C	0V	3.3V ± 0.3

2944 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	Vcc+0.3	V
V_{IL}	Input Low Voltage	–0.3[1]	—	0.8	V

NOTE: 2944 tbl 06

1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

NOTE: 2944 tbl 07

1. This parameter is determined by device characterization but is not production tested (TQFP Package only).
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	IDT70V25S		IDT70V25L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

NOTE:
1. At Vcc = 2.0V input leakages are undefined.

2944 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V25X25		70V25X35		70V25X55		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L.	S	80	170	70	115	70	115	mA
				L	80	120	70	100	70	100	
I_{SB1}	Standby Current (Both Ports — TTL	$\overline{CE_R}$ = $\overline{CE_L}$ = V_{IH} $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH} Level Inputs)f = f_{MAX}[3]	COM'L.	S	12	25	10	25	10	25	mA
				L	10	20	8	20	8	20	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE_L}$ or $\overline{CE_R}$ = V_{IH}[5] Active Port Outputs Open f = f_{MAX}[3] $\overline{SEM_R}$ = $\overline{SEM_L}$ = V_{IH}	COM'L.	S	40	82	35	72	35	72	mA
				L	40	72	35	62	35	62	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE_L}$ and $\overline{CE_R}$ ≥ Vcc - 0.2V V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM_R}$ = $\overline{SEM_L}$ ≥ Vcc - 0.2V	COM'L.	S	1.0	5	1.0	5	1.0	5	mA
				L	0.2	2.5	0.2	2.5	0.2	2.5	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs) V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	One Port $\overline{CE_L}$ or $\overline{CE_R}$ ≥ Vcc - 0.2V[5] $\overline{SEM_R}$ = $\overline{SEM_L}$ ≥ Vcc - 0.2V	COM'L.	S	50	81	45	71	45	71	mA
				L	50	71	45	61	45	61	

NOTES:
1. 'X' in part numbers indicates power rating (S or L)
2. Vcc = 5V, Ta = +25°C, and are not production tested. Icc dc = 70mA (TYP)
3. At f = fMAX, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/ RC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

2683 tbl 09

6

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2944 tbl 11

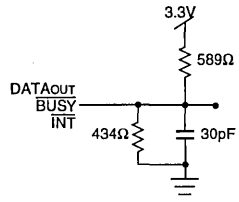


Figure 1. AC Output Load

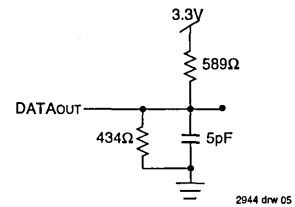


Figure 2. Output Test Load
(For tLZ, tHZ, twz, tow)
Including scope and jig.

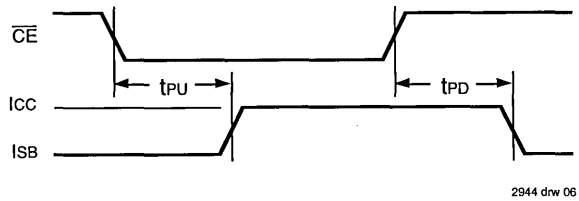
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(4)

Symbol	Parameter	IDT70V25 x25		IDT70V25 x35		IDT70V25 x55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
tRC	Read Cycle Time	25	—	35	—	55	—	ns
tAA	Address Access Time	—	25	—	35	—	55	ns
tACE	Chip Enable Access Time(3)	—	25	—	35	—	55	ns
tABE	Byte Enable Access Time(3)	—	25	—	35	—	55	ns
tAOE	Output Enable Access Time	—	15	—	20	—	30	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	3	—	3	—	3	—	ns
tHZ	Output High-Z Time(1, 2)	—	15	—	20	—	25	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	25	—	55	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns
tSAA	Semaphore Address Access Time	—	35	—	45	—	65	ns

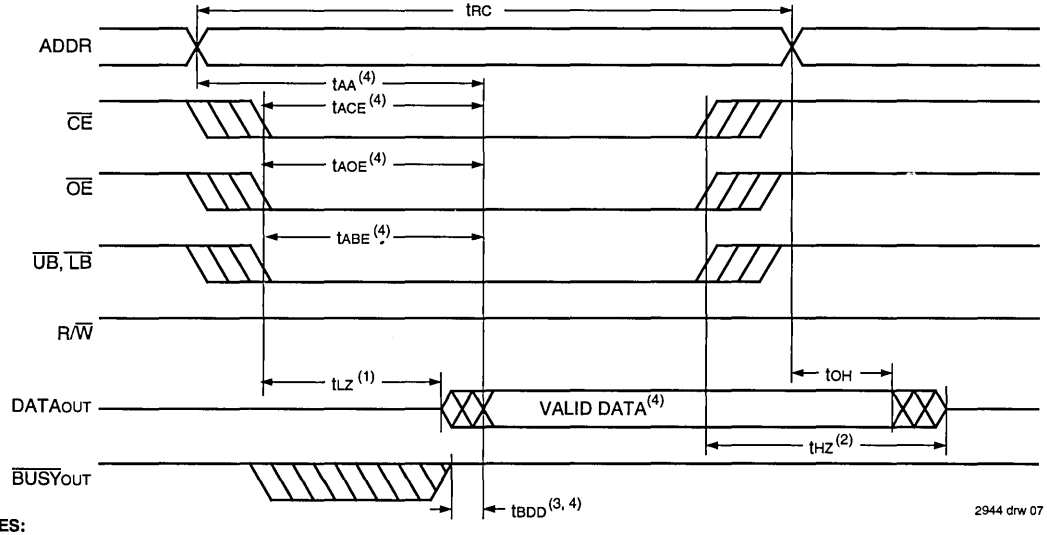
2944 tbl 12

NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterazation, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{UB}$ or $\overline{LB}$ = VIL, and $\overline{SEM}$ = VIH. To access semephore, $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIH, and $\overline{SEM}$ = VIL.
4. "X" in part numbers indicates power rating (S or L).

TIMING OF POWER-UP POWER-DOWN



WAVEFORM OF READ CYCLES[5]



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first, $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. tBDD delay is required only in case where opposite port is completing a write operation to the same address location for simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tABE, tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

6

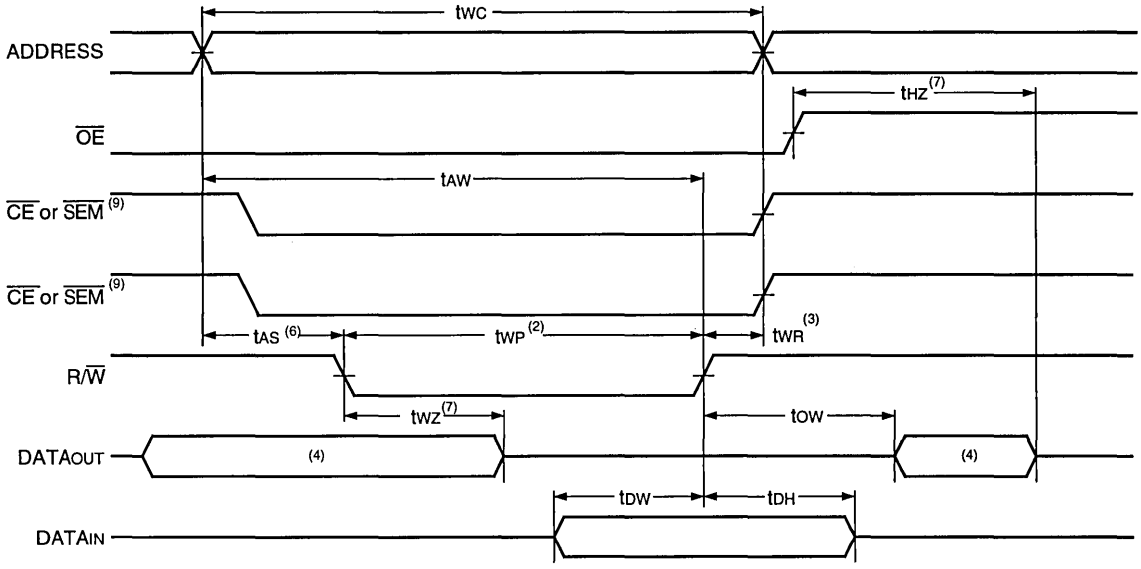
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE [5]

Symbol	Parameter	IDT70V25X25		IDT70V25X35		IDT70V25X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	25	—	35	—	55	—	ns
tEW	Chip Enable to End-of-Write[3]	20	—	30	—	45	—	ns
tAW	Address Valid to End-of-Write	20	—	30	—	45	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	20	—	30	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	20	—	25	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	15	—	20	—	25	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

2944 tbl 13

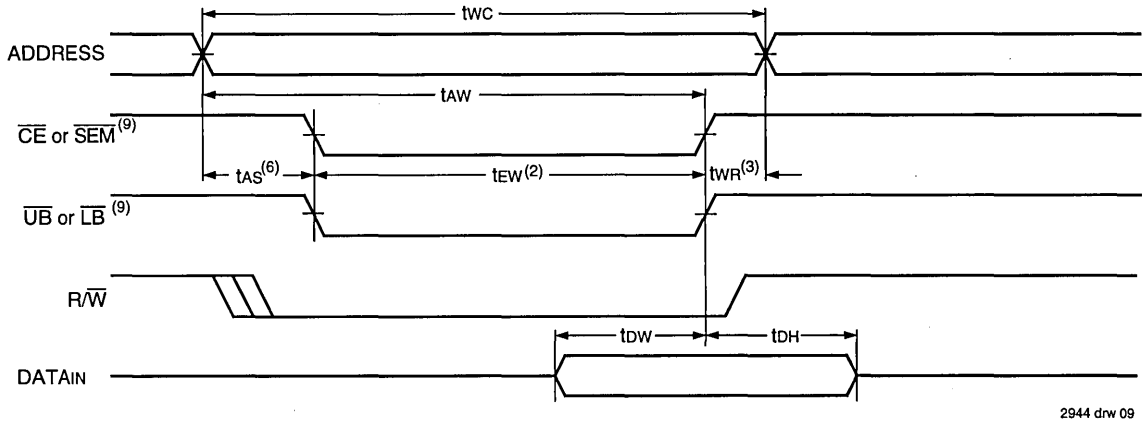
NOTES:
1. Transition is measured ±500mV from low or high impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL, $\overline{UB}$ or $\overline{LB}$ = VIL, $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIH, and $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,5,8)



2944 drw 08

TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING(1,5)

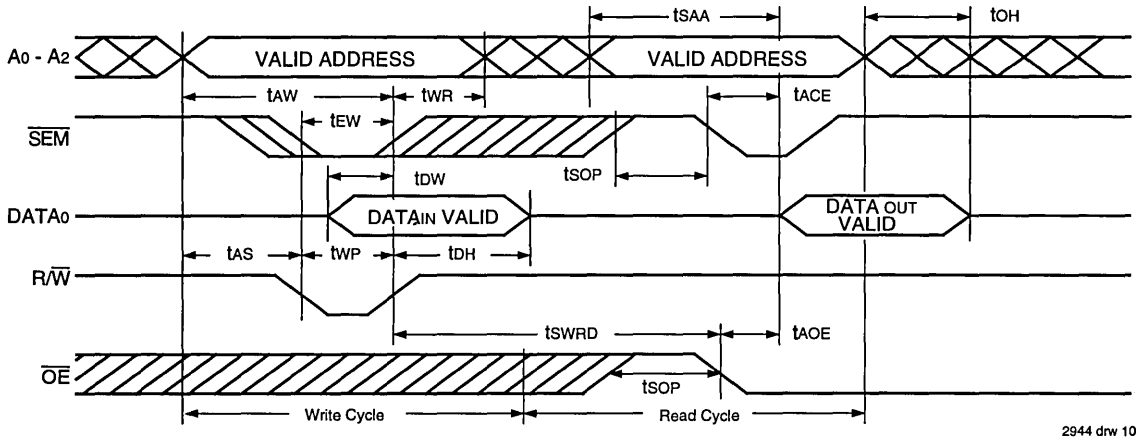


2944 drw 09

NOTES:

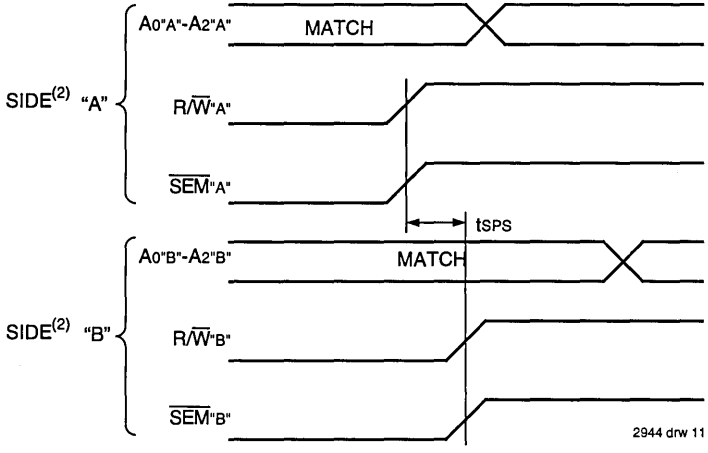
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ & $\overline{LB}$ must be High during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low $\overline{UB}$ or $\overline{LB}$ and a low $\overline{CE}$ and a low R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going high to the end-of-write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, R/$\overline{W}$, or byte control.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured +/- 500mV from steady state with Output Test Load (Figure 2).
8. If $\overline{OE}$ is low during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ = VIL, $\overline{UB}$ or $\overline{LB}$ = VIL, and $\overline{SEM}$ = VIH. To access Semephore, $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIL, and $\overline{SEM}$ = VIL. tEW must be met for either condition.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIH for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}_R$ = $\overline{CE}_L$ = VIH, or both $\overline{UB}$ & $\overline{LB}$ = VIH.
2. All timing is the same for left and right port. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going High to $R/\overline{W}_B$ or $\overline{SEM}_B$ going High.
4. If tSPS is not satisfied, there is no guarantee which side will obtain the semaphore flag.

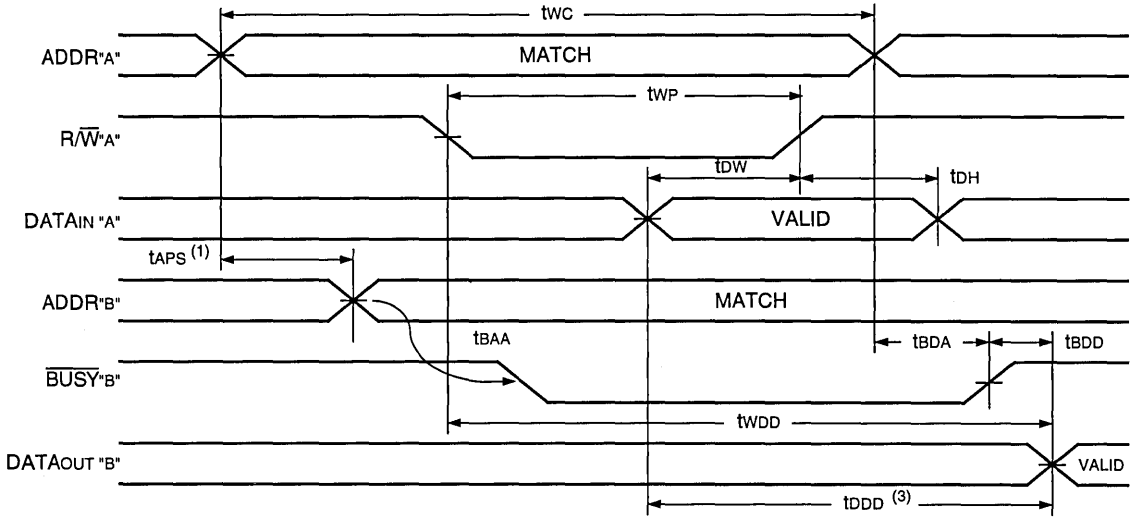
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	IDT70V25X25 Min.	IDT70V25X25 Max.	IDT70V25X35 Min.	IDT70V25X35 Max.	IDT70V25X55 Min.	IDT70V25X55 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = H)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	25	—	35	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	25	—	35	—	45	ns
tBAC	$\overline{BUSY}$ Access Time from Chip LOW	—	25	—	35	—	45	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip HIGH	—	25	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	25	—	35	—	55	ns
BUSY TIMING (M/$\overline{S}$ = L)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	20	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	55	—	60	—	80	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	50	—	55	—	75	ns

2944 tbl 14

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "TIMING WAVEFORM OF WRITE PORT-TO-PORT READ AND $\overline{BUSY}$ (M/$\overline{S}$ = VIH)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited during contention.
5. To ensure that a write cycle is completed after contention.
6. "x" is part numbers indicates power rating (S or L).

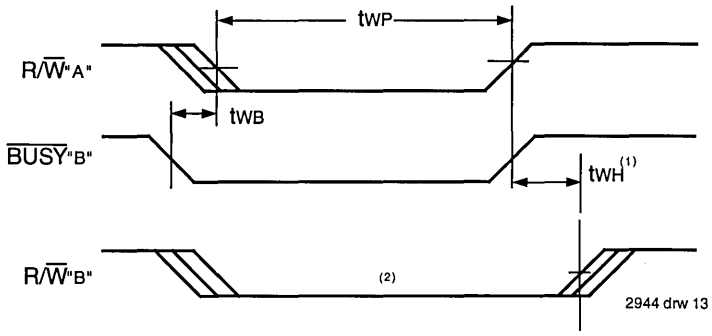
TIMING WAVEFORM OF WRITE PORT-TO-PORT READ AND $\overline{BUSY}$[2,5] (M/$\overline{S}$ = VIH)



2944 drw 12

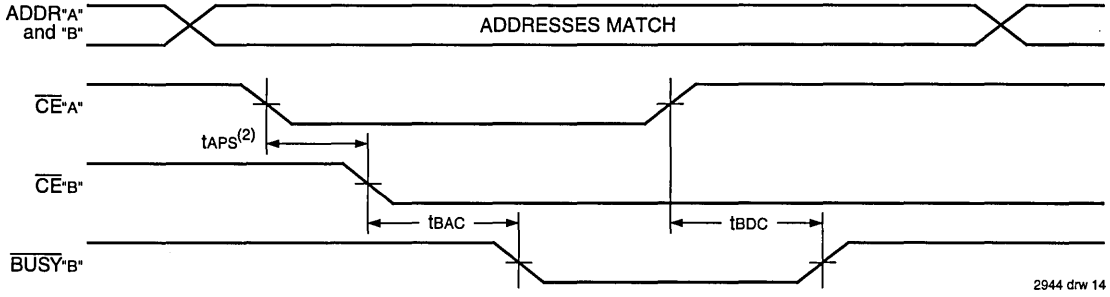
NOTES:
1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}_L$ = $\overline{CE}_R$ = L
3. $\overline{OE}$ = L for the reading port.

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$

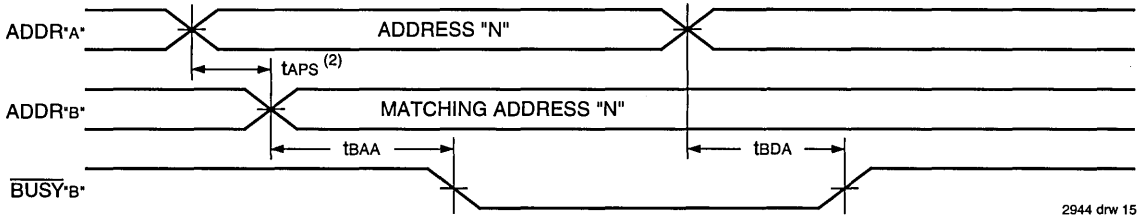


NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (slave) output master.
2. Busy is asserted on port "B" Blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes High

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING(1) (M/$\overline{S}$ = H)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)(M/$\overline{S}$ = H)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

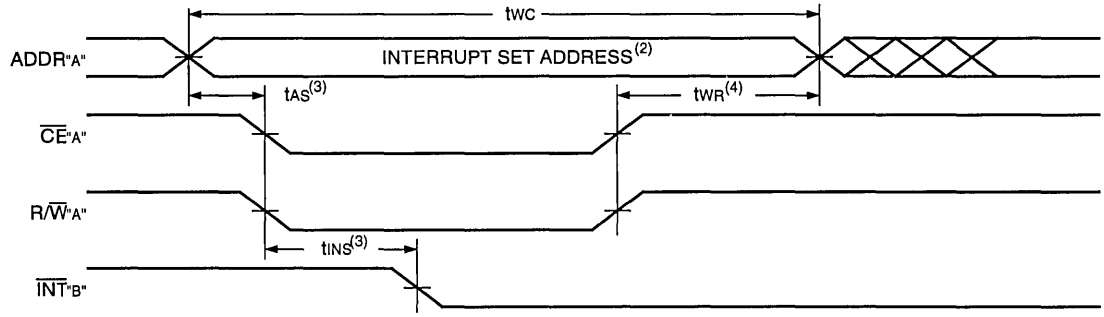
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

Symbol	Parameter	IDT70V25X25 Min.	IDT70V25X25 Max.	IDT70V25X35 Min.	IDT70V25X35 Max.	IDT70V25X55 Min.	IDT70V25X55 Max.	Unit
INTERRUPT TIMING								
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	30	—	40	ns
t_{INR}	Interrupt Reset Time	—	30	—	35	—	45	ns

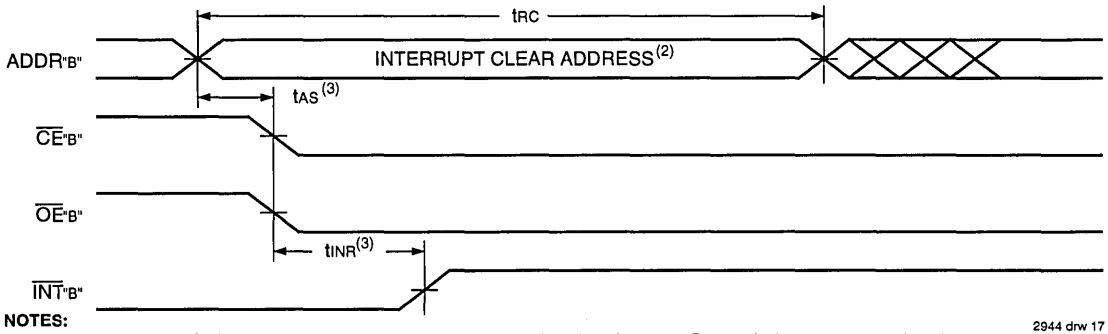
NOTE:
1. "X" in part numbers indicates power rating (S or L).

2944 tbl 15

WAVEFORM OF INTERRUPT TIMING[1]



2944 drw 16



2944 drw 17

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt Flag truth table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					Function
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{12L}-A_{0L}	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{12R}-A_{0R}	$\overline{INT}_R$	
L	L	X	1FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	1FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	1FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	1FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
1. Assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = VIH.
2. If $\overline{BUSY}_L$ = VIL, then no change.
3. If $\overline{BUSY}_R$ = VIL, then no change.

2944 tbl 16

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{12L} A_{0R}-A_{12R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

NOTES: 2944 tbl 17

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$ outputs on the IDT70V25 are push pull, not open drain outputs. On slaves the $\overline{BUSY}$ input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_{15} Left	D_0 - D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2944 tbl 18

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V25.

FUNCTIONAL DESCRIPTION

The IDT70V25 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V25 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 1FFE (HEX), where a write is defined as the $\overline{CE}_R$ = R/$\overline{W}_R$ = V_{IL} per the Truth Table. The left port clears the interrupt by an address location 1FFE access when $\overline{CE}_L$ = $\overline{OE}_L$ = V_{IL}, R/$\overline{W}_L$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is set when the left port writes to memory location 1FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must read the memory location 1FFF. The message (16 bits) at 1FFE or 1FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes, but as part of the random access memory. Refer to Table I for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all

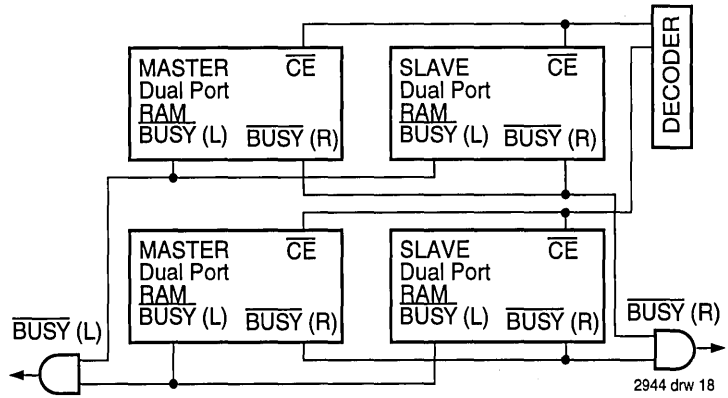


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70V25 RAMs.

applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 70V25 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT70V25 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT70V25 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT70V25 is an extremely fast Dual-Port 8K x 16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT70V25 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70V25's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be

allocated in varying configurations. The IDT70V25 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70V25 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0–A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a

6

resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT70V25's Dual-Port RAM. Say the 8K x 16 RAM was to be divided into two 4K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

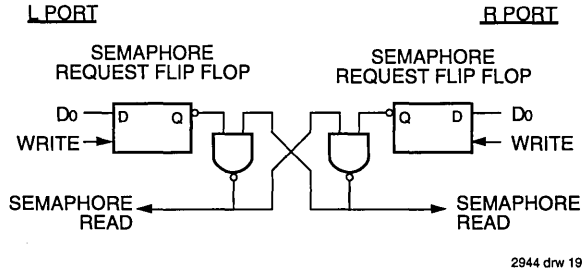
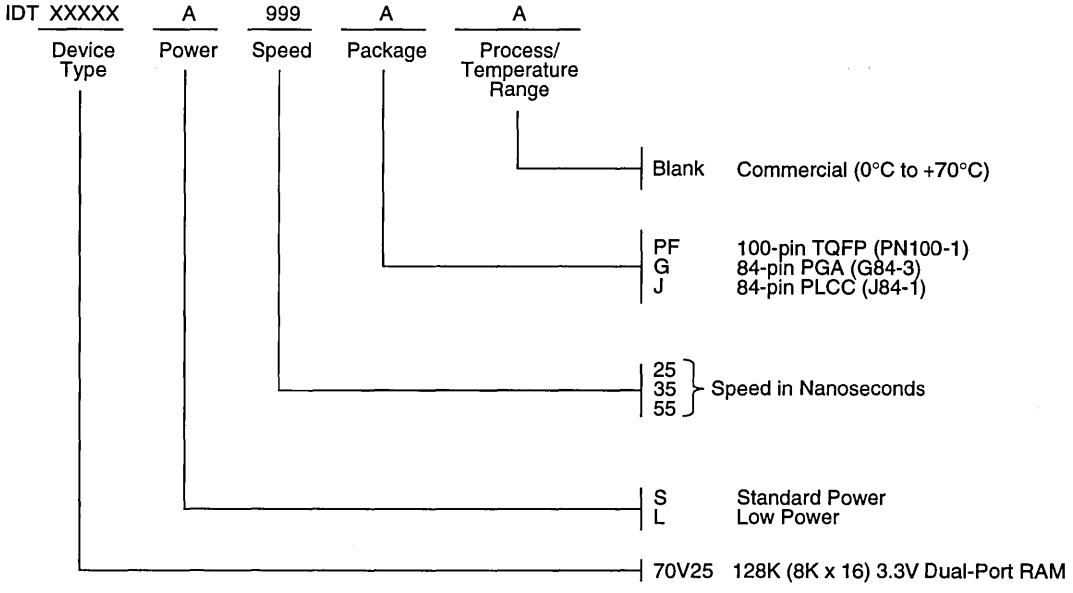


Figure 4. IDT70V25 Semaphore Logic

ORDERING INFORMATION



2944 drw 20

6

Integrated Device Technology, Inc.

HIGH-SPEED 3.3V 16K x 16 DUAL-PORT STATIC RAM

PRELIMINARY
IDT70V26S/L

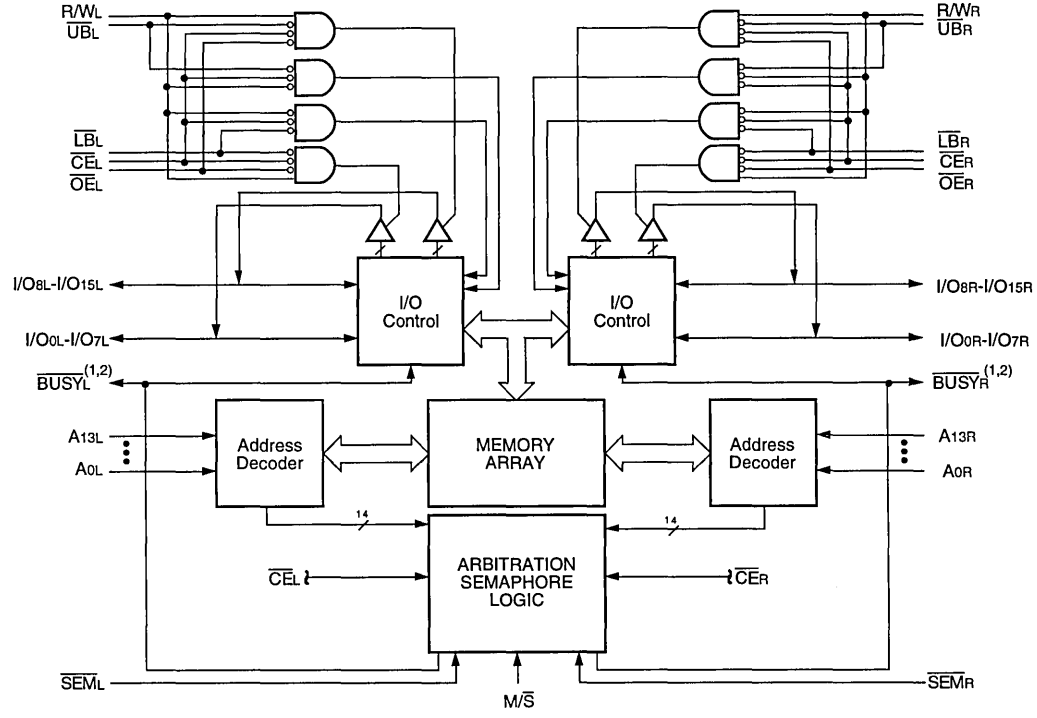
FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Commercial: 25/35/55ns (max.)
- Low-power operation
  - — IDT70V26S
    Active: 450mW (typ.)
    Standby: 5mW (typ.)
  - — IDT70V26L
    Active: 450mW (typ.)
    Standby: 5mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT70V26 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Devices are capable of withstanding greater than 2001V electrostatic charge.
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- TTL-compatible, single 3.3V (±0.3V) power supply
- Available in 84-pin PGA, and PLCC

DESCRIPTION:

The IDT70V26 is a high-speed 16K x 16 Dual-Port Static RAM. The IDT70V26 is designed to be used as a stand-alone 256K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit-or-more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ outputs are non-tri-stated push-pull.

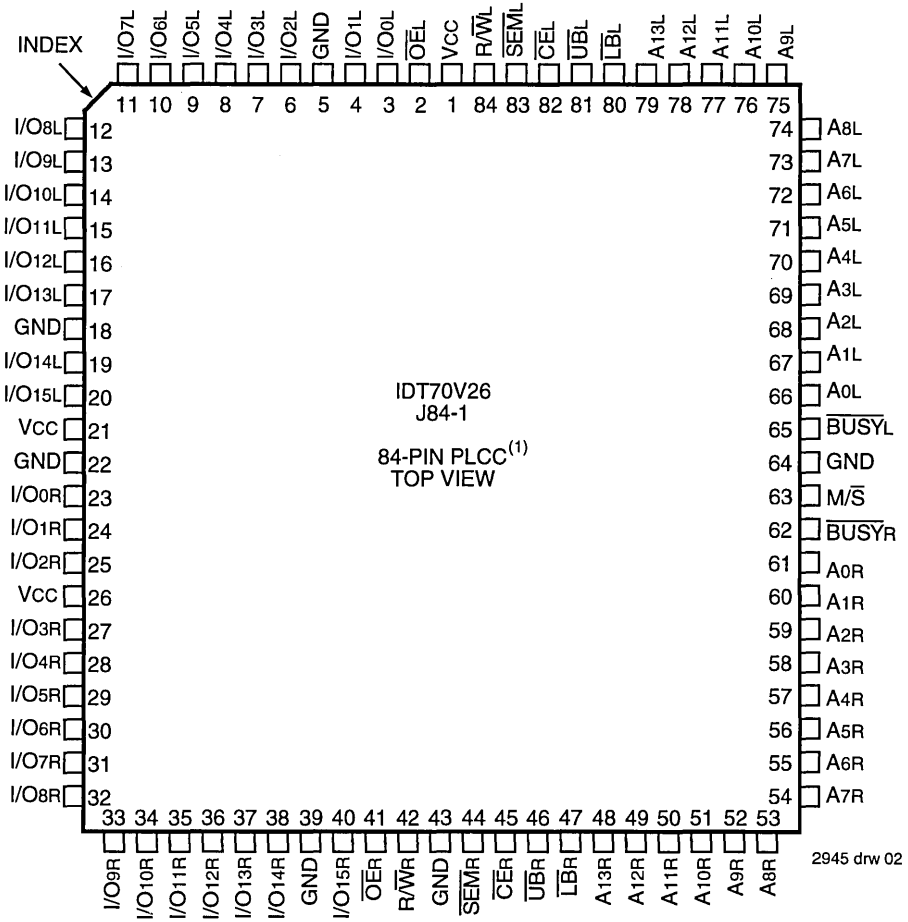
32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

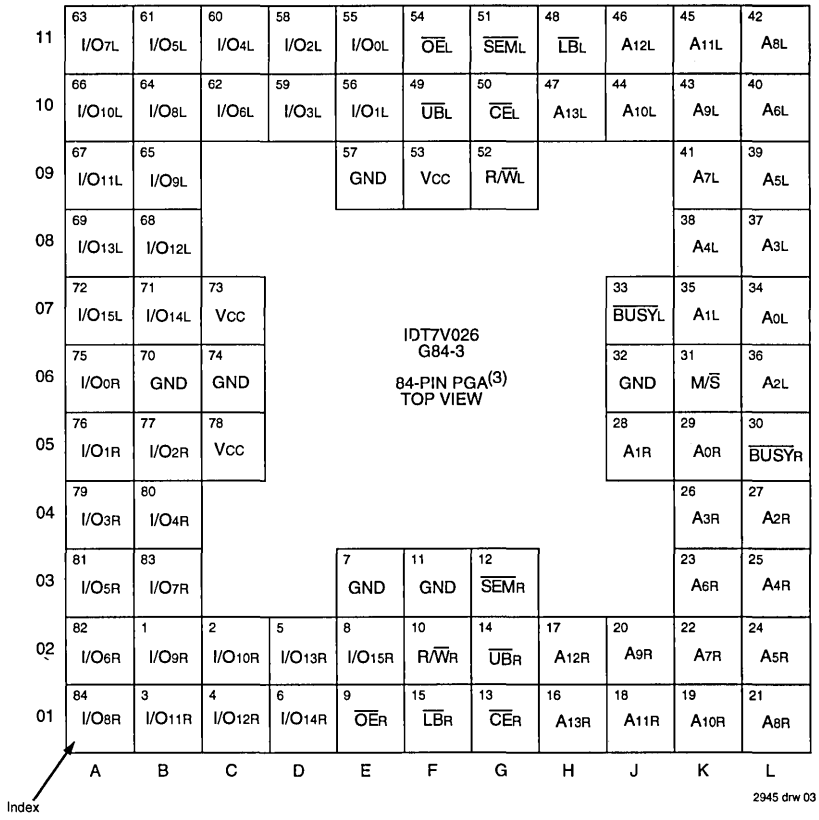
Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 450mW of power.

The IDT70V26 is packaged in a ceramic 84-pin PGA and 84-Pin PLCC.

PIN CONFIGURATIONS



NOTE:
1. This text does not indicate orientation of the actual part-marking.



	A	B	C	D	E	F	G	H	J	K	L
11	63 I/O7L	61 I/O5L	60 I/O4L	58 I/O2L	55 I/O0L	54 $\overline{OE}_L$	51 $\overline{SEM}_L$	48 $\overline{LB}_L$	46 A12L	45 A11L	42 A8L
10	66 I/O10L	64 I/O8L	62 I/O6L	59 I/O3L	56 I/O1L	49 $\overline{UB}_L$	50 $\overline{CE}_L$	47 A13L	44 A10L	43 A9L	40 A6L
09	67 I/O11L	65 I/O9L			57 GND	53 Vcc	52 R/$\overline{W}_L$			41 A7L	39 A5L
08	69 I/O13L	68 I/O12L								38 A4L	37 A3L
07	72 I/O15L	71 I/O14L	73 Vcc						33 $\overline{BUSY}_L$	35 A1L	34 A0L
06	75 I/O0R	70 GND	74 GND						32 GND	31 M/$\overline{S}$	36 A2L
05	76 I/O1R	77 I/O2R	78 Vcc						28 A1R	29 A0R	30 $\overline{BUSY}_R$
04	79 I/O3R	80 I/O4R								26 A3R	27 A2R
03	81 I/O5R	83 I/O7R			7 GND	11 GND	12 $\overline{SEM}_R$			23 A6R	25 A4R
02	82 I/O6R	1 I/O9R	2 I/O10R	5 I/O13R	8 I/O15R	10 R/$\overline{W}_R$	14 $\overline{UB}_R$	17 A12R	20 A9R	22 A7R	24 A5R
01	84 I/O8R	3 I/O11R	4 I/O12R	6 I/O14R	9 $\overline{OE}_R$	15 $\overline{LB}_R$	13 $\overline{CE}_R$	16 A13R	18 A11R	19 A10R	21 A8R

PIN NAMES (1,2)

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
R/$\overline{W}_L$	R/$\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A0L – A13L	A0R – A13R	Address
I/O0L – I/O15L	I/O0R – I/O15R	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
M/$\overline{S}$		Master or Slave Select
Vcc		Power
GND		Ground

2945 tbl 01

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power-Down
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected: Power-Down
L	L	X	L	H	H	DATAIN	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

NOTE:
1. $A_{0L} — A_{13L} \neq A_{0R} — A_{13R}$

2945 tbl 02

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
H	↓	X	X	X	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
X	↓	X	H	H	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

2945 tbl 03

6

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2945 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 0.3V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military			
Commercial	0°C to +70°C	0V	3.3V ± 0.3

2945 tbl 05

RECOMMENDED DC OPERATING CONDITIONS (2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	Vcc+0.3	V
V_{IL}	Input Low Voltage	–0.3(1)	—	0.8	V

NOTE: 2945 tbl 06

1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.3V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

NOTE: 2945 tbl 07

1. This parameter is determined by device characterization but is not production tested.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (Vcc = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	IDT70V26S		IDT70V26L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	Vcc = 3.6V, V_{IN} = 0V to Vcc	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to Vcc	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2945 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version	70V26X25 Typ.[2]	70V26X25 Max.	70V26X35 Typ.[2]	70V26X35 Max.	70V26X55 Typ.[2]	70V26X55 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L. S L	100 100	170 140	90 90	140 120	90 90	140 120	mA
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L. S L	14 12	30 24	12 10	30 24	12 10	30 24	mA
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}$"A" = V_{IL} and $\overline{CE}$"B" = V_{IH}[5] Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L. S L	50 50	95 85	45 45	87 75	45 45	87 75	mA
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V	COM'L. S L	1.0 0.2	6 3	1.0 0.2	6 3	1.0 0.2	6 3	mA
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}$"A" ≤ 0.2V and $\overline{CE}$"B" ≥ V_{CC} - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open f = f_{MAX}[3]	COM'L. S L	60 60	90 80	55 55	85 74	55 55	85 74	mA

2945 tbl 09

NOTES:
1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 3.3V, T_A = +25°C, and are not production tested. I_{CCDC} = 80mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1 / t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2945 tbl 11

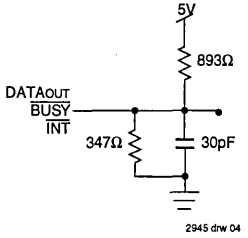


Figure 1. AC Output Test Load

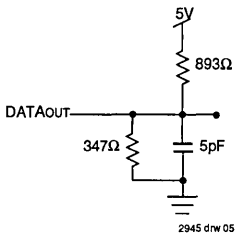


Figure 2. Output Test Load
(for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
* Including scope and jig.

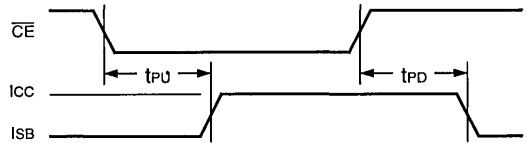
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[4]

Symbol	Parameter	IDT70V26X25		IDT70V26X35		IDT70V26X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25	—	35	—	55	—	ns
t_{AA}	Address Access Time	—	25	—	35	—	55	ns
t_{ACE}	Chip Enable Access Time [3]	—	25	—	35	—	55	ns
t_{ABE}	Byte Enable Access Time [3]	—	15	—	35	—	55	ns
t_{AOE}	Output Enable Access Time	—	15	—	20	—	30	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1, 2]	3	—	3	—	3	—	ns
t_{HZ}	Output High-Z Time[1, 2]	—	15	—	20	—	25	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	25	—	35	—	50	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns
t_{SAA}	Semaphore Address Access Time	—	35	—	45	—	65	ns

2945 tbl 12

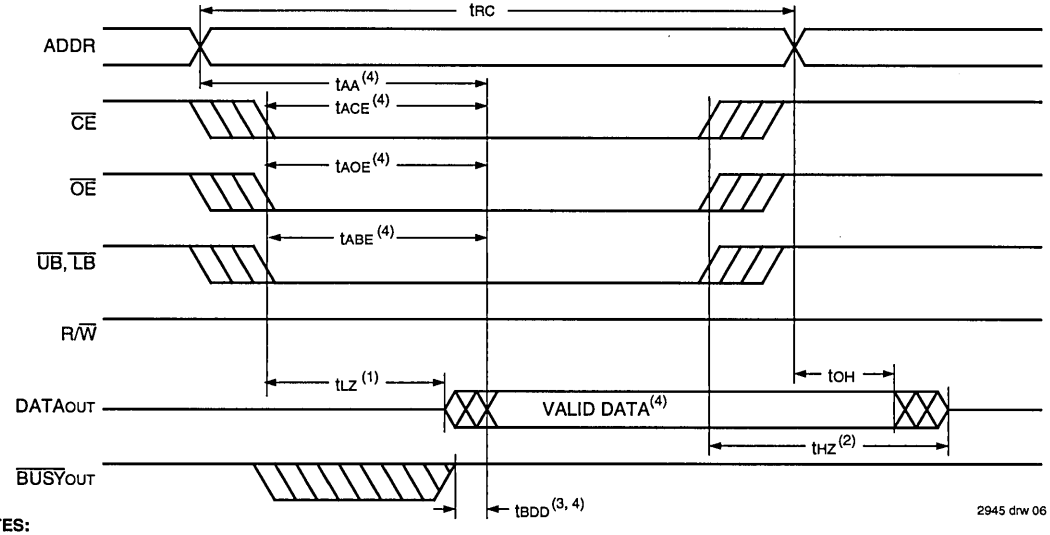
NOTES:
1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL} and $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} and $\overline{SEM}$ = V_{IL}.
4. "X" in part numbers indicates power rating (S or L).

TIMING OF POWER-UP POWER-DOWN



2945 drw 07

WAVEFORM OF READ CYCLES[5]



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

6

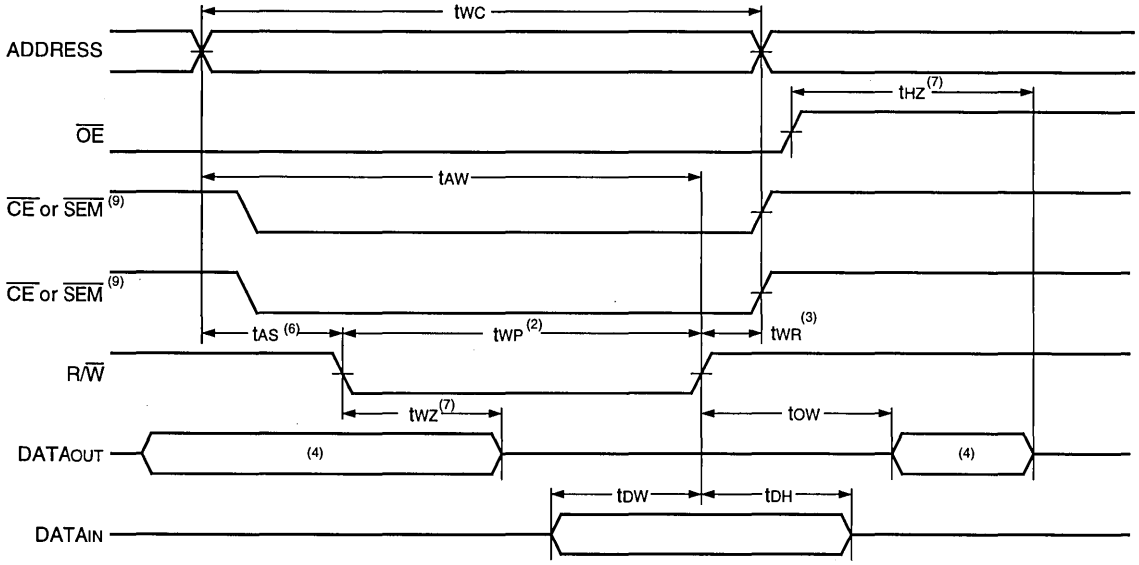
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[5]

Symbol	Parameter	IDT70V26X25		IDT70V26X35		IDT70V26X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	25	—	35	—	55	—	ns
tEW	Chip Enable to End-of-Write[3]	20	—	30	—	45	—	ns
tAW	Address Valid to End-of-Write	20	—	30	—	45	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	20	—	30	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	20	—	25	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	15	—	20	—	25	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

NOTES:
2945 tbl 13

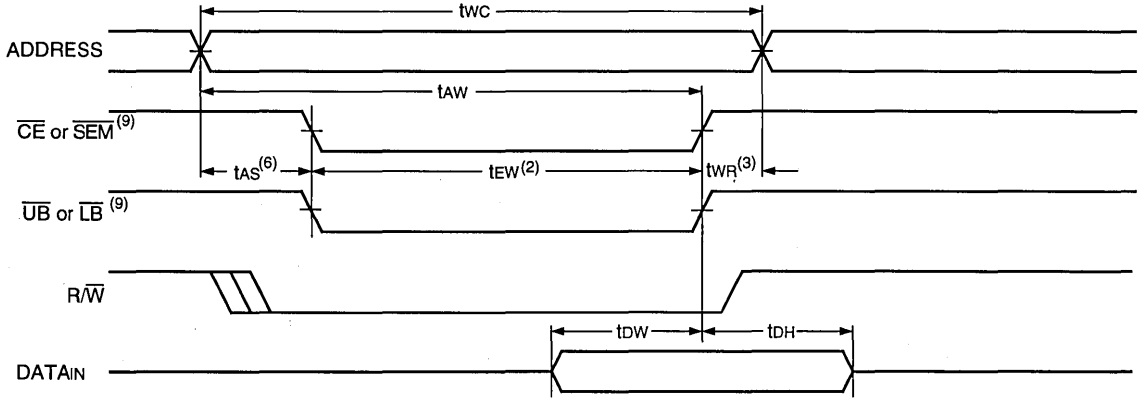
1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING(1,5,8)



2945 drw 08

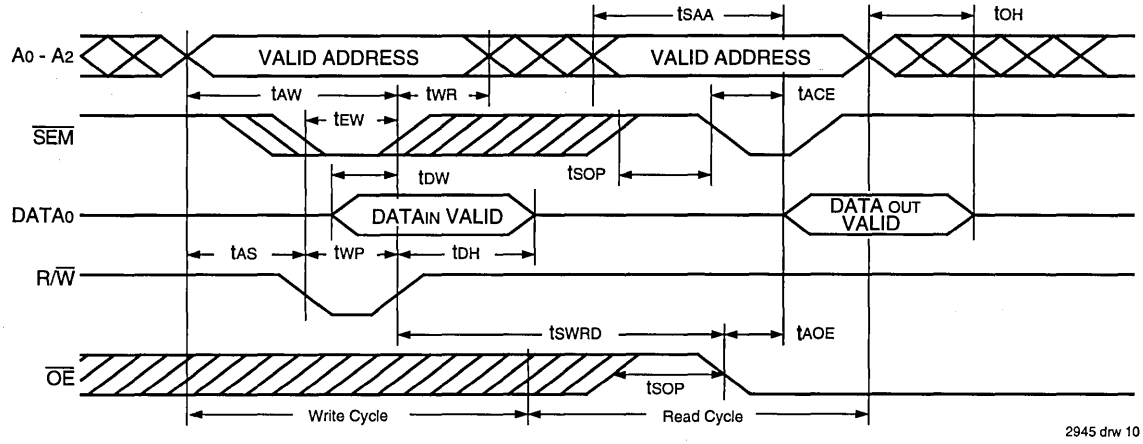
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING(1,5)



2945 drw 09

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ and $\overline{LB}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a LOW $\overline{CE}$ and a LOW R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured ±200mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. tEW must be met for either condition.

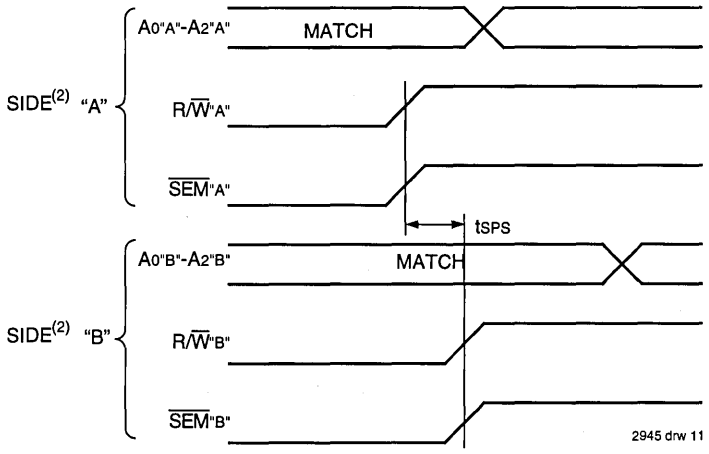
TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = H or $\overline{UB}$ & $\overline{LB}$ = H for the duration of the above timing (both write and read cycle).

6

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}_R$ = $\overline{CE}_L$ = VIH, or both $\overline{UB}$ & $\overline{LB}$ = VIH.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}$"A" or $\overline{SEM}$"A" going HIGH to R/$\overline{W}$"B" or $\overline{SEM}$"B" going HIGH.
4. If tSPS is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

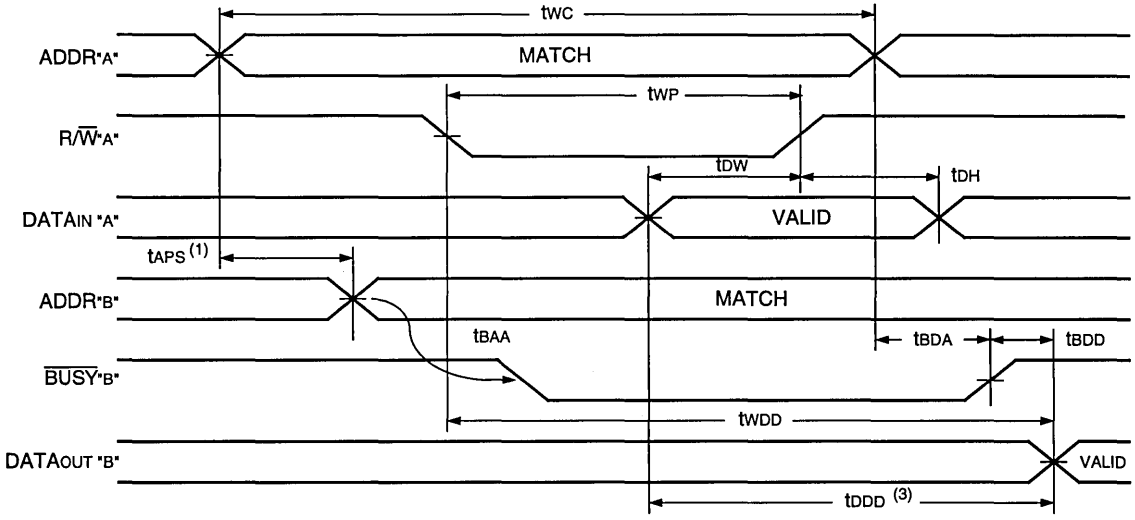
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	IDT70V26X25		IDT70V26X35		IDT70V26X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
BUSY TIMING (M/$\overline{S}$ = VIH)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	25	—	35	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	25	—	35	—	45	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	25	—	35	—	45	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	25	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	25	—	35	—	55	ns
BUSY TIMING (M/$\overline{S}$ = VIL)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	20	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	55	—	65	—	85	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	50	—	60	—	80	ns

2945 tbl 14

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ (M/$\overline{S}$ = VIH)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. "X" in part numbers indicates power rating (S or L).

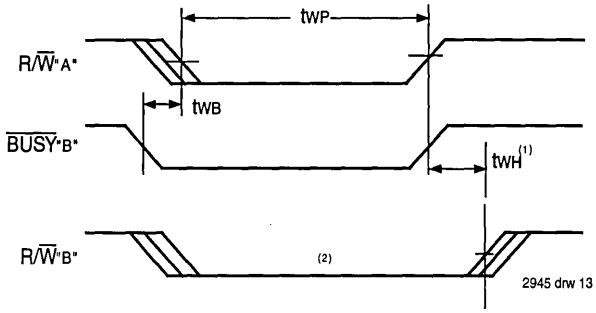
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$ [2,5]



2945 drw 12

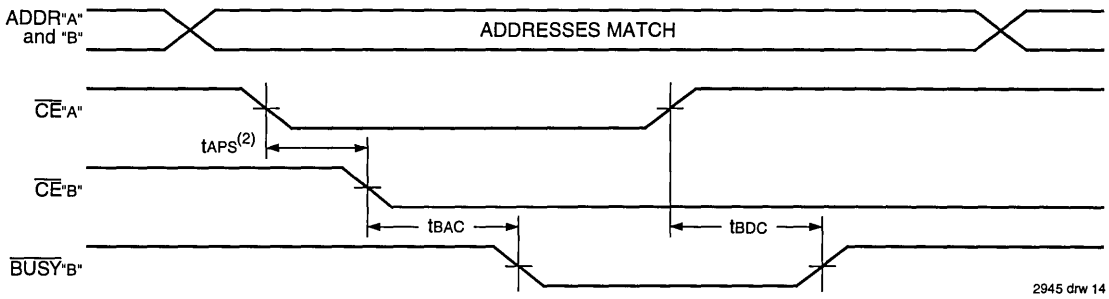
NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for M/$\overline{S}$ = VIL (SLAVE).
2. $\overline{CE}_L$ = $\overline{CE}_R$ = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. If M/$\overline{S}$ = VIL (SLAVE), then $\overline{BUSY}$ is an input ($\overline{BUSY}$"A" = VIH and $\overline{BUSY}$"B" = "don't care", for this example).
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

TIMING WAVEFORM OF WRITE WITH BUSY

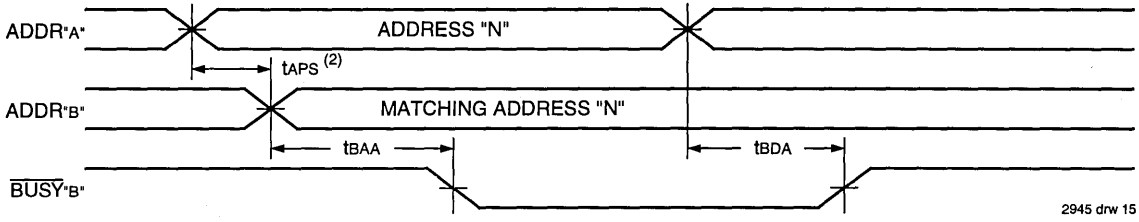


NOTES:
1. tWH must be met for both BUSY input (SLAVE) and output (MASTER).
2. BUSY is asserted on port "B" blocking R/W"B", until BUSY"B" goes High.

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY CE TIMING(1)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or the other, but there is no guarantee on which side busy will be asserted.

TRUTH TABLES

TRUTH TABLE I — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{13L} A_{0R}-A_{13R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

NOTES: 2945 tbl 15

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}x$ outputs on the IDT70V26 are push pull, not open drain outputs. On slaves the $\overline{BUSY}x$ input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE II — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_{15} Left	D_0 - D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

NOTE: 2945 tbl 16

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V26.

FUNCTIONAL DESCRIPTION

The IDT70V26 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V26 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. operation. If the write inhibit function of busy logic is not desirable, the busy logic can be disabled by placing the part in slave mode with the $M/\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 70V26 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT70V26 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT70V26 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in

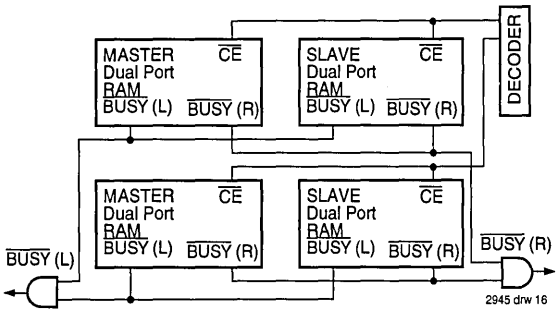


Figure 3. Busy and chip enable routing for both width and depth

width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT70V26 is an extremely fast Dual-Port 16K x 16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT70V26 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70V26's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70V26 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70V26 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of

6

the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT70V26's Dual-Port RAM. Say the 16K x 16 RAM was to be divided into two 8K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 8K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in

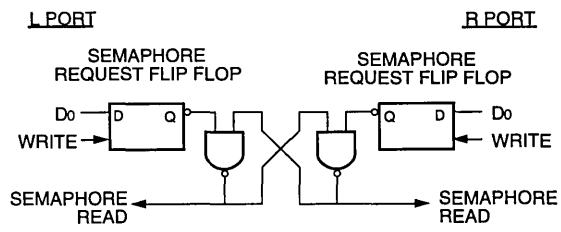


Figure 4. IDT70V26 Semaphore Logic

response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of Dual-Port RAM with each other.

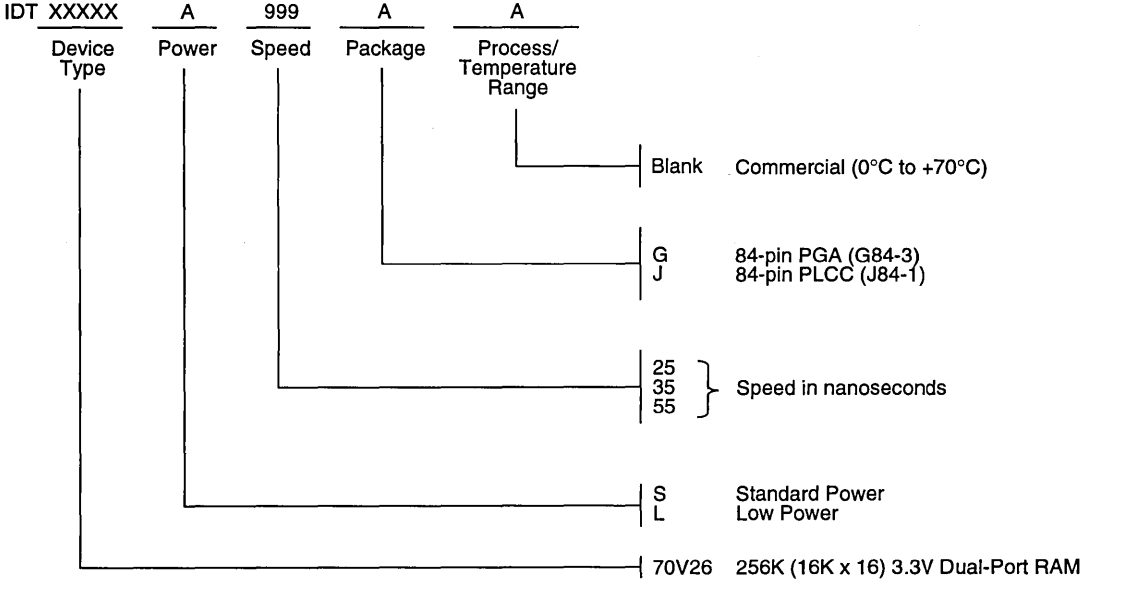
The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

ORDERING INFORMATION



2945 drw 19

Integrated Device Technology, Inc.

HIGH-SPEED 3.3V 16K x 16 DUAL-PORT STATIC RAM

PRELIMINARY
IDT70V261S/L

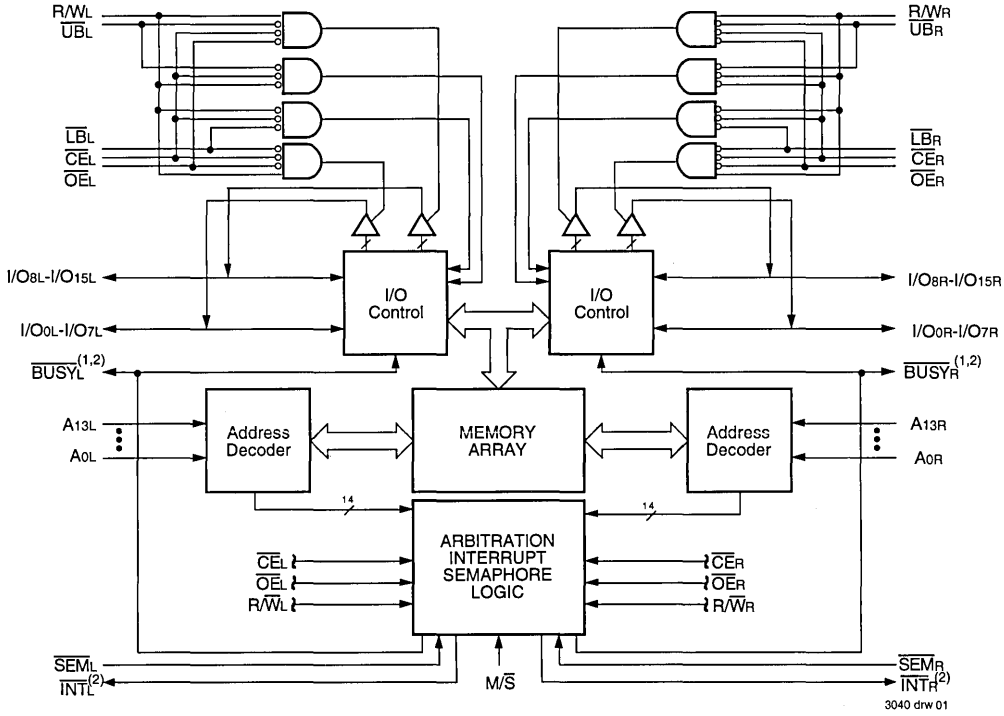
FEATURES:

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - — Commercial: 25/35/55ns (max.)
- Low-power operation
  - — IDT70V261S
    Active: 450mW (typ.)
    Standby: 5mW (typ.)
  - — IDT70V261L
    Active: 450mW (typ.)
    Standby: 5mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT70V261 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- Devices are capable of withstanding greater than 2001V electrostatic charge.
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- TTL-compatible, single 3.3V (±0.3V) power supply
- Available in a 100-pin TQFP, Thin Quad Plastic Flatpack

DESCRIPTION:

The IDT70V261 is a high-speed 16K x 16 Dual-Port Static RAM. The IDT70V261 is designed to be used as a stand-alone 256K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit-or-more word systems.

FUNCTIONAL BLOCK DIAGRAM



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ and $\overline{INT}$ outputs are non-tri-stated push-pull.

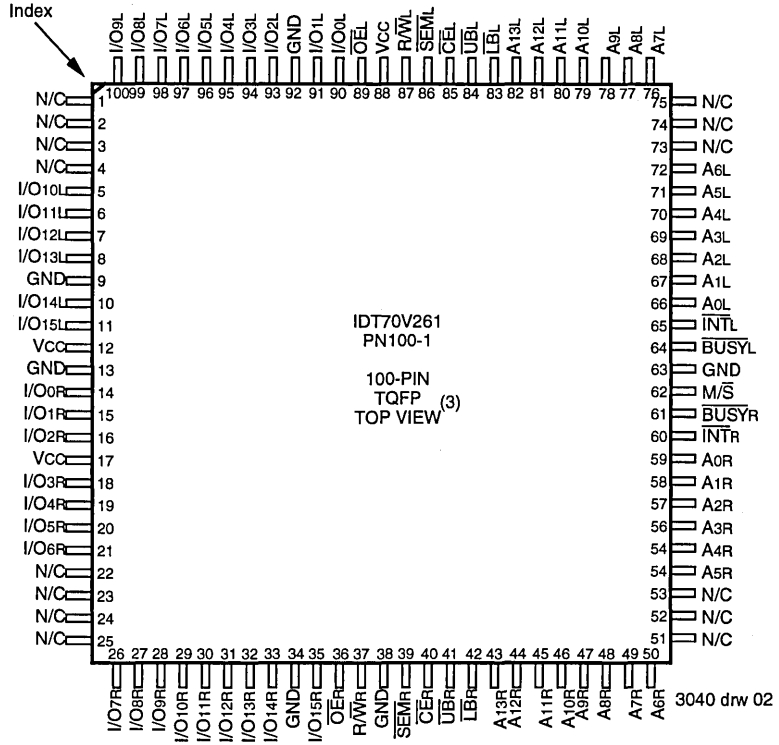
Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 450mW of power.

The IDT70V261 is packaged in a 100-pin Thin Quad Plastic Flatpack.

PIN CONFIGURATIONS



PIN NAMES (1,2)

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L} - A_{13L}$	$A_{0R} - A_{13R}$	Address
$I/O_{0L} - I/O_{15L}$	$I/O_{0R} - I/O_{15R}$	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground

3040 tbl 01

NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

6

TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

Inputs[1]						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	X	X	X	X	H	High-Z	High-Z	Deselected: Power-Down
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected: Power-Down
L	L	X	L	H	H	DATAIN	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	DATAIN	Write to Lower Byte Only
L	L	X	L	L	H	DATAIN	DATAIN	Write to Both Bytes
L	H	L	L	H	H	DATAOUT	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	DATAOUT	Read Lower Byte Only
L	H	L	L	L	H	DATAOUT	DATAOUT	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

NOTE:
1. $A_{0L} — A_{13L} \neq A_{0R} — A_{13R}$

3040 tbl 02

TRUTH TABLE: SEMAPHORE READ/WRITE CONTROL

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O8-15	I/O0-7	Mode
H	H	L	X	X	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
X	H	L	H	H	L	DATAOUT	DATAOUT	Read Data in Semaphore Flag
H	↓	X	X	X	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
X	↓	X	H	H	L	DATAIN	DATAIN	Write I/O0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

3040 tbl 03

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:

3040 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \geq$ Vcc + 0.3V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3

3040 tbl 05

RECOMMENDED DC OPERATING CONDITIONS (2)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	Vcc+0.3	V
V_{IL}	Input Low Voltage	–0.3(1)	—	0.8	V

NOTE:

3040 tbl 06

1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 0.3V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

NOTE:

3040 tbl 07

1. This parameter is determined by device characterization but is not production tested. TQFP package only.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	IDT70V261S		IDT70V261L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 3.6V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

3040 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		70V261X25		70V261X35		70V261X55		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L.	S	100	170	90	140	90	140	mA
				L	100	140	90	120	90	120	
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L.	S	14	30	12	30	12	30	mA
				L	12	24	10	24	10	24	
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L.	S	50	95	45	87	45	87	mA
				L	50	85	45	75	45	75	
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V	COM'L.	S	1.0	6	1.0	6	1.0	6	mA
				L	0.2	3	0.2	3	0.2	3	
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open f = f_{MAX}[3]	COM'L.	S	60	90	55	85	55	85	mA
				L	60	80	55	74	55	74	

3040 tbl 09

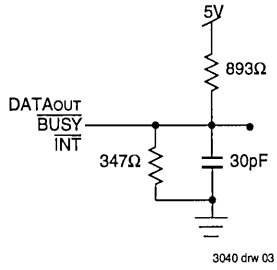
NOTES:
1. "X" in part numbers indicates power rating (S or L)
2. V_{CC} = 3.3V, T_A = +25°C, and are not production tested. I_{CCDC} = 80mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1 / t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

6

AC TEST CONDITIONS

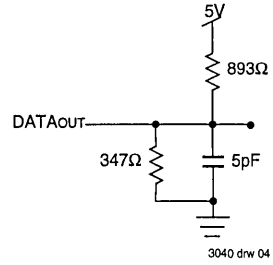
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

3040 tbl 11



3040 drw 03

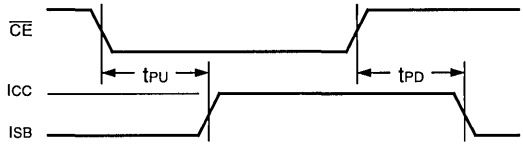
Figure 1. AC Output Test Load



3040 drw 04

Figure 2. Output Test Load
(for tLZ, tHZ, twz, tow)
* Including scope and jig.

TIMING OF POWER-UP POWER-DOWN



3040 drw 06

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(4)

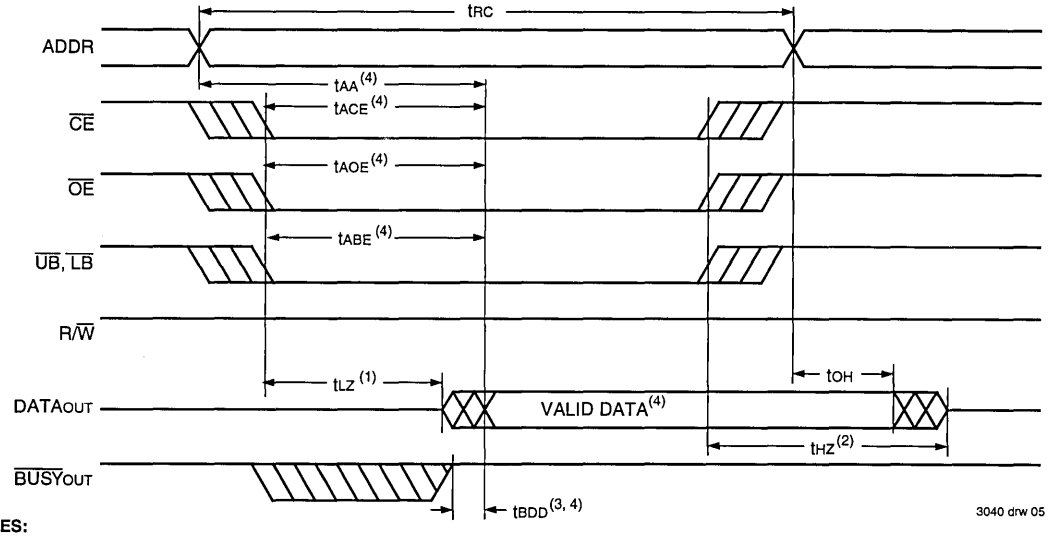
		IDT70V261X25		IDT70V261X35		IDT70V261X55		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	25	—	35	—	55	—	ns
tAA	Address Access Time	—	25	—	35	—	55	ns
tACE	Chip Enable Access Time (3)	—	25	—	35	—	55	ns
tABE	Byte Enable Access Time (3)	—	15	—	35	—	55	ns
tAOE	Output Enable Access Time	—	15	—	20	—	30	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	3	—	3	—	3	—	ns
tHZ	Output High-Z Time(1, 2)	—	15	—	20	—	25	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	25	—	35	—	50	ns
tSOP	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns
tSAA	Semaphore Address Access Time	—	35	—	45	—	65	ns

NOTES:

3040 tbl 12

1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL.
4. "X" in part numbers indicates power rating (S or L).

WAVEFORM OF READ CYCLES[5]



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = VIH.

6

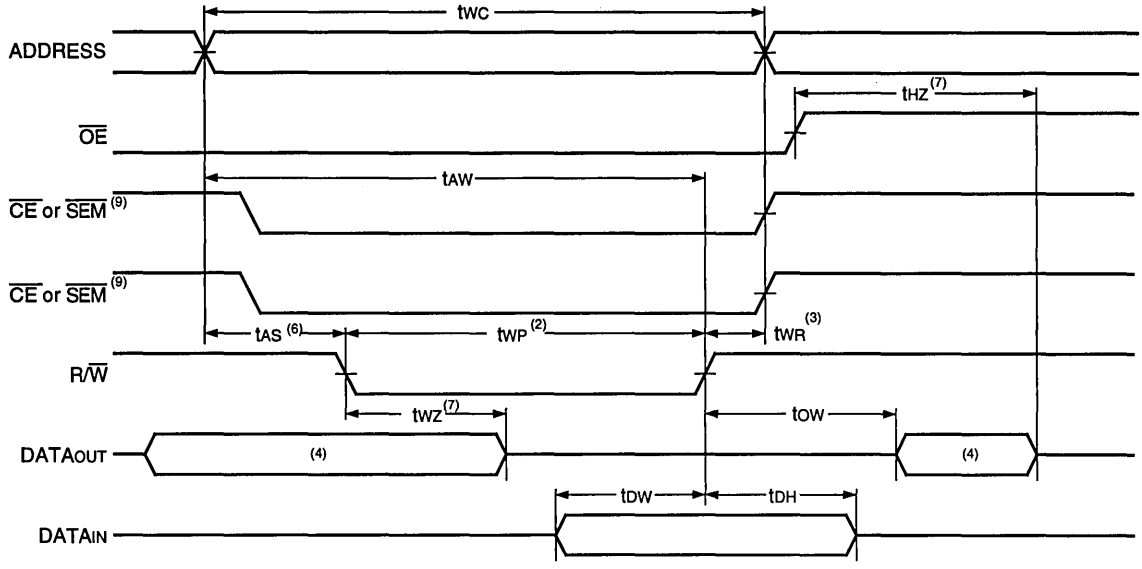
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE[5]

Symbol	Parameter	IDT70V261X25		IDT70V261X35		IDT70V261X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
tWC	Write Cycle Time	25	—	35	—	55	—	ns
tEW	Chip Enable to End-of-Write[3]	20	—	30	—	45	—	ns
tAW	Address Valid to End-of-Write	20	—	30	—	45	—	ns
tAS	Address Set-up Time[3]	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	25	—	40	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End-of-Write	15	—	20	—	30	—	ns
tHZ	Output High-Z Time[1, 2]	—	15	—	20	—	25	ns
tDH	Data Hold Time[4]	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High-Z[1, 2]	—	15	—	20	—	25	ns
tOW	Output Active from End-of-Write[1, 2, 4]	0	—	0	—	0	—	ns
tSWRD	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
tSPS	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

3040 tbl 13

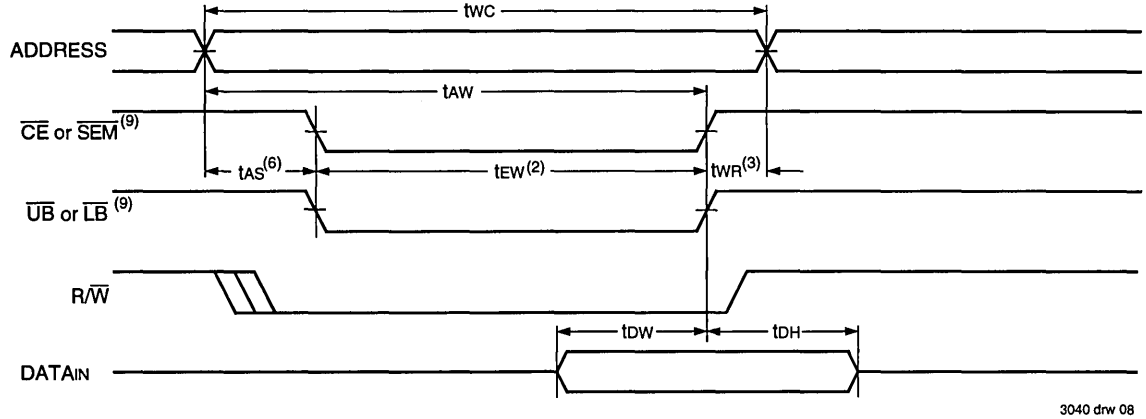
NOTES:
1. Transition is measured ±200mV from low- or high-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1, R/$\overline{W}$ CONTROLLED TIMING[1,5,8]



3040 drw 07

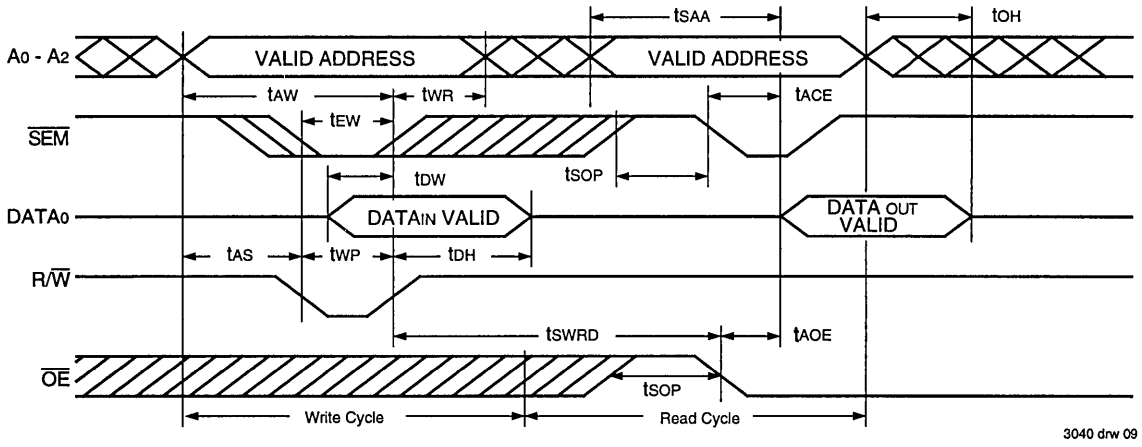
TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ CONTROLLED TIMING[1,5]



3040 drw 08

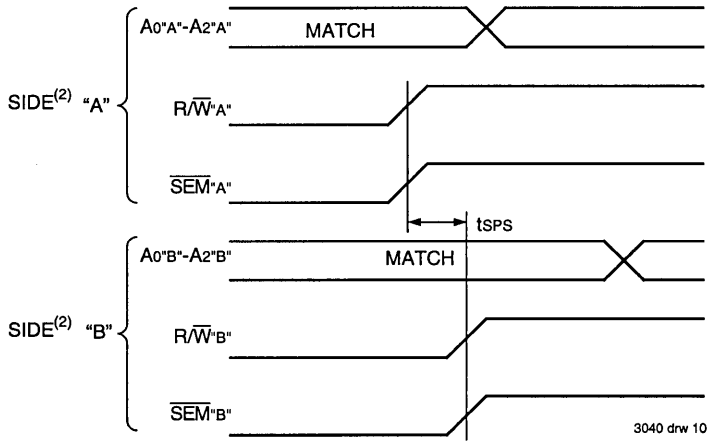
NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ and $\overline{LB}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a LOW $\overline{CE}$ and a LOW R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$ or R/$\overline{W}$.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured ± 200mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is LOW during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ = VIL and $\overline{SEM}$ = VIH. To access semaphore, $\overline{CE}$ = VIH and $\overline{SEM}$ = VIL. tEW must be met for either condition.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING, EITHER SIDE[1]



NOTE:
1. $\overline{CE}$ = H or $\overline{UB}$ & $\overline{LB}$ = H for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE WRITE CONTENTION[1,3,4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}_R$ = $\overline{CE}_L$ = VIH, or both $\overline{UB}$ & $\overline{LB}$ = VIH.
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}$"A" or $\overline{SEM}$"A" going HIGH to R/$\overline{W}$"B" or $\overline{SEM}$"B" going HIGH.
4. If tSPS is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

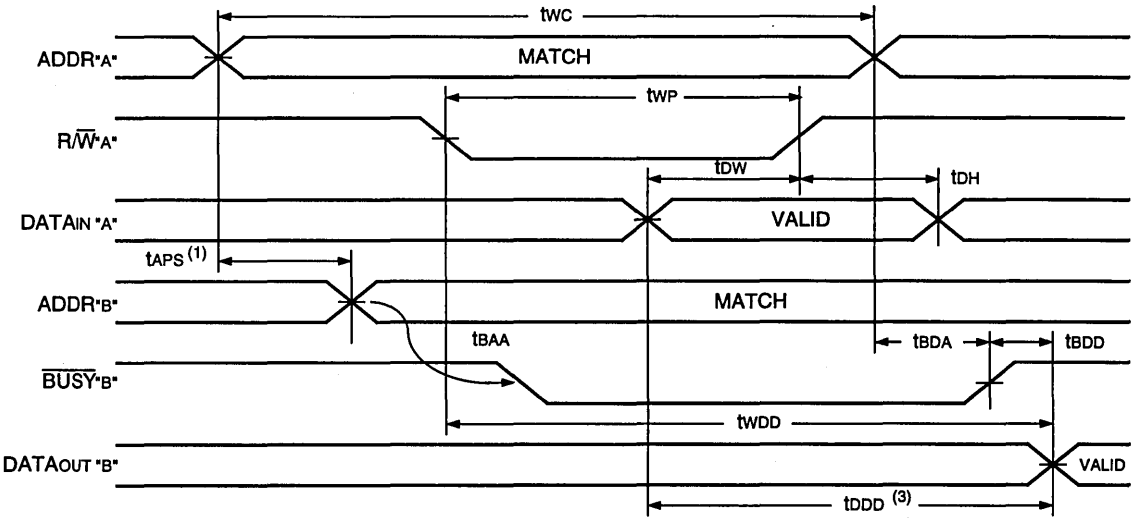
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[6]

Symbol	Parameter	IDT70V261X25 Min.	IDT70V261X25 Max.	IDT70V261X35 Min.	IDT70V261X35 Max.	IDT70V261X55 Min.	IDT70V261X55 Max.	Unit
BUSY TIMING ($M/\overline{S}$ = VIH)								
tBAA	$\overline{BUSY}$ Access Time from Address Match	—	25	—	35	—	45	ns
tBDA	$\overline{BUSY}$ Disable Time from Address Not Matched	—	25	—	35	—	45	ns
tBAC	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	25	—	35	—	45	ns
tBDC	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	25	—	35	—	45	ns
tAPS	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
tBDD	$\overline{BUSY}$ Disable to Valid Data[3]	—	25	—	35	—	55	ns
BUSY TIMING ($M/\overline{S}$ = VIL)								
tWB	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
tWH	Write Hold After $\overline{BUSY}$[5]	20	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
tWDD	Write Pulse to Data Delay[1]	—	55	—	65	—	85	ns
tDDD	Write Data Valid to Read Data Delay[1]	—	50	—	60	—	80	ns

3040 tbl 14

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$ ($M/\overline{S}$ = VIH)".
2. To ensure that the earlier of the two ports wins.
3. tBDD is a calculated parameter and is the greater of 0, tWDD – tWP (actual) or tDDD – tDW (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. "X" in part numbers indicates power rating (S or L).

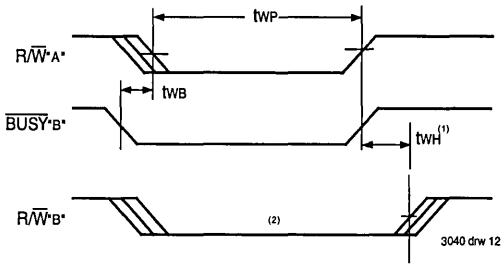
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT READ AND $\overline{BUSY}$ [2,5]



3040 drw 11

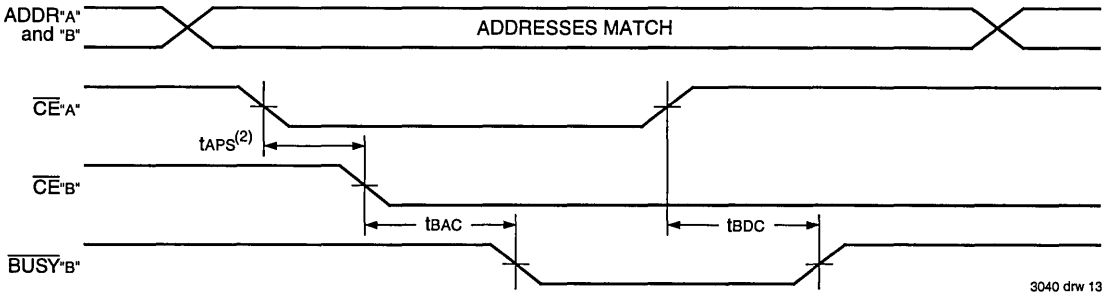
NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for $M/\overline{S}$ = VIL (SLAVE).
2. $\overline{CE}_L$ = $\overline{CE}_R$ = VIL
3. $\overline{OE}$ = VIL for the reading port.
4. If $M/\overline{S}$ = VIL (SLAVE), then $\overline{BUSY}$ is an input ($\overline{BUSY}$"A" = VIH and $\overline{BUSY}$"B" = "don't care", for this example).
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

TIMING WAVEFORM OF WRITE WITH BUSY

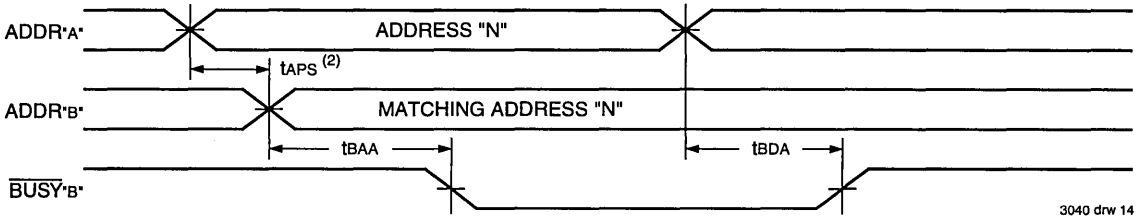


NOTES:
1. tWH must be met for both BUSY input (SLAVE) and output (MASTER).
2. BUSY is asserted on port "B" blocking R/W"B", until BUSY"B" goes High.

WAVEFORM OF BUSY ARBITRATION CONTROLLED BY CE TIMING(1)



WAVEFORM OF BUSY ARBITRATION CYCLE CONTROLLED BY ADDRESS MATCH TIMING(1)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the busy signal will be asserted on one side or the other, but there is no guarantee on which side busy will be asserted.

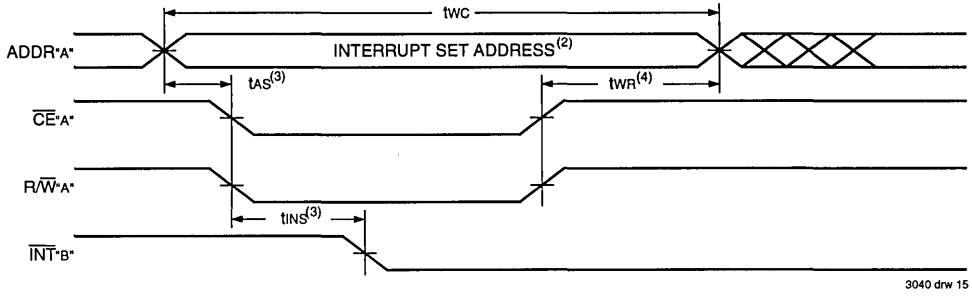
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1]

Symbol	Parameter	IDT70V261X25 Min.	IDT70V261X25 Max.	IDT70V261X35 Min.	IDT70V261X35 Max.	IDT70V261X55 Min.	IDT70V261X55 Max.	Unit
INTERRUPT TIMING								
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	30	—	40	ns
t_{INR}	Interrupt Reset Time	—	30	—	35	—	45	ns

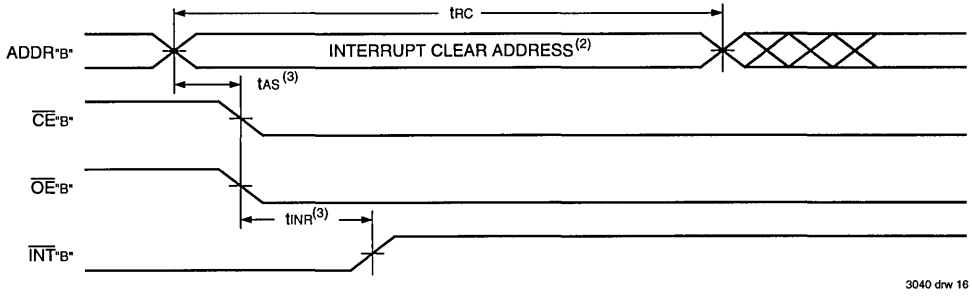
NOTE:
1. "X" in part numbers indicates power rating (S or L).

3040tbl 15

WAVEFORM OF INTERRUPT TIMING[1]



3040 drw 15



3040 drw 16

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

TRUTH TABLES

TRUTH TABLE I — INTERRUPT FLAG[1]

Left Port					Right Port					Function
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{13L}-A_{0L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{13R}-A_{0R}	$\overline{INT}_R$	
L	L	X	3FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	3FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	3FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	3FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$.
2. If $\overline{BUSY}_L = V_{IL}$, then no change.
3. If $\overline{BUSY}_R = V_{IL}$, then no change.

3040tbl 16

TRUTH TABLE II — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{13L} A_{0R}-A_{13R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

3040 tbl 16

NOTES:

1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. Both are inputs when configured as a slave. $\overline{BUSY}$x outputs on the IDT70V261 are push pull, not open drain outputs. On slaves the $\overline{BUSY}$x input internally inhibits writes.
2. L if the inputs to the opposite port were stable prior to the address and enable inputs of this port. H if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be low simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving low regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving low regardless of actual logic level on the pin.

TRUTH TABLE III — EXAMPLE OF SEMAPHORE PROCUREMENT SEQUENCE(1)

Functions	D_0 - D_{15} Left	D_0 - D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Right port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

3040 tbl 17

NOTE:

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT70V261.

FUNCTIONAL DESCRIPTION

The IDT70V261 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V261 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 3FFE (HEX), where a write is defined as $\overline{CE}$ = R/$\overline{W}$ = V_{IL} per the Truth Table. The left port clears the interrupt through access of address location 3FFE when $\overline{CE}_R$ = $\overline{OE}_R$ = V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 3FFF (HEX) and to clear the 3FFF location 3FFF. The message (8 bits) at 3FFE or 3FFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FFE and 3FFF are not used as mail boxes, but as part of the random access memory. Refer to Table 1 for the interrupt operation.

BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of busy logic is not in slave desirable, the busy logic can be disabled by placing the part

in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins high. If desired, unintended write operations can be prevented to a port by tying the busy pin for that port low.

The busy outputs on the IDT 70V261 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the busy indication for the resulting array requires the use of an external AND gate.

WIDTH EXPANSION WITH BUSY LOGIC MASTER/SLAVE ARRAYS

When expanding an IDT70V261 RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT70V261 RAM the busy pin is an output if the part is used as a master (M/$\overline{S}$ pin = H), and

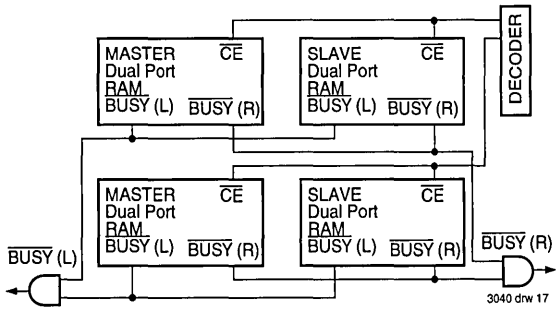


Figure 3. Busy and chip enable routing for both width and depth

the busy pin is an input if the part used as a slave (M/$\overline{S}$ pin = L) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The busy arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a busy flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

SEMAPHORES

The IDT70V261 is an extremely fast Dual-Port 16K x 16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table where $\overline{CE}$ and $\overline{SEM}$ are both high.

Systems which can best use the IDT70V261 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70V261's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70V261 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

HOW THE SEMAPHORE FLAGS WORK

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once

the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active low. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT70V261 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a low input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0 – A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a low level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussing on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag low and the other side high. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay low until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

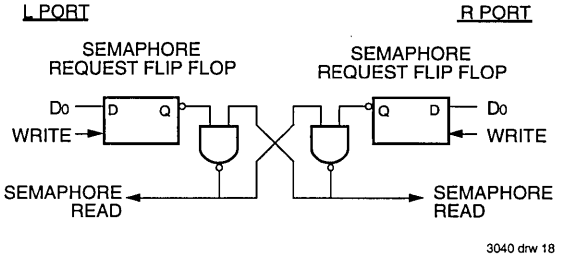


Figure 4. IDT70V261 Semaphore Logic

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

USING SEMAPHORES—SOME EXAMPLES

Perhaps the simplest application of semaphores is their application as resource markers for the IDT70V261's Dual-Port RAM. Say the 16K x 16 RAM was to be divided into two 8K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the

6

indicator for the upper section of memory.

To take a resource, in this example the lower 8K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 8K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 8K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 8K blocks of Dual-Port RAM with each other.

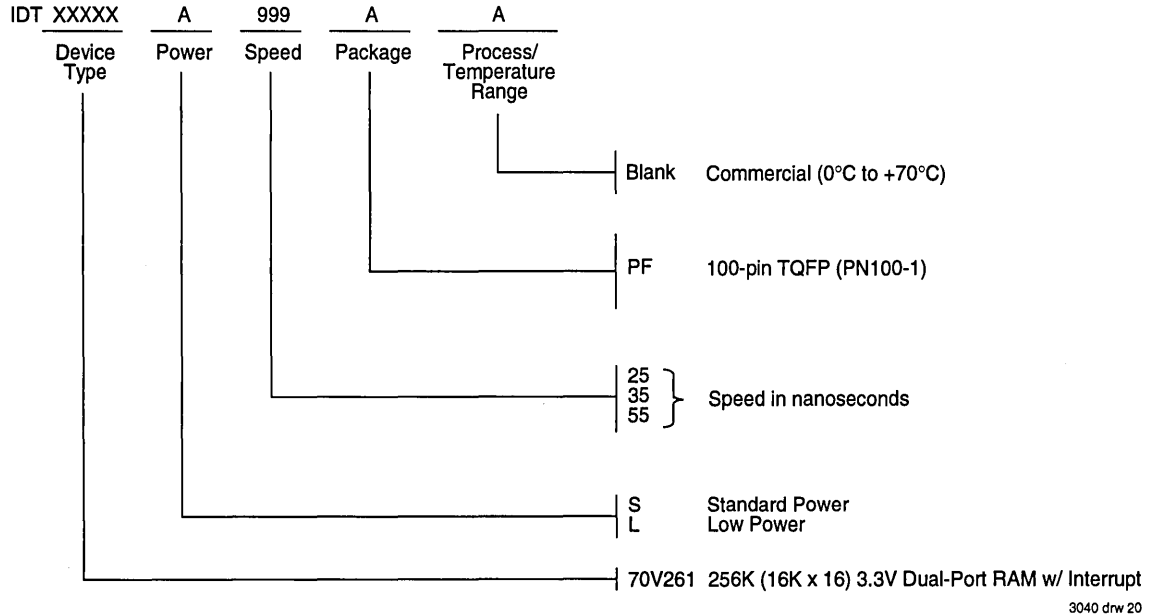
The blocks do not have to be any particular size and can even be variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

ORDERING INFORMATION



3040 drw 20

SUBSYSTEMS PRODUCTS

IDT Subsystems Division has the resources and experience to deliver the highest quality RAM module products. IDT's combination of advanced design, assembly, and test capabilities give customers the highest levels of quality, service and performance. Product offerings include a number JEDEC standards as well as specialized and application specific RAM modules, including the world's highest performance and densest SRAMs, Dual-Port RAMs, and FIFOs. Custom capabilities allow our customers to enjoy the benefits of modules for high performance caches for the leading microprocessors, multi-processor board level products and multi-chip modules (MCMs).

IDT modules products provide a number of benefits to the high performance system designer:

For system designers of high performance systems, modules solve a number of major problems through the benefits they provide. The biggest benefit of modules is that they save significant amounts of space for designers packing ever more performance in less area by utilizing double sided surface mount technology. In addition, decoupling capacitors are mounted next to or underneath the active memory components on the module, thus eliminating the need to consider them or the real estate they consume.

Numerous module packaging options are available which allow designers to trade-off board area, height and mechanical stability. Vertical mount module options (modules in which mounted components are oriented in a vertical fashion) such as Zig-zag In-Line packages (ZIPs), Single In-line Memory Modules (SIMMs) and Dual In-line Memory Modules (DIMMs) are ideal packages for applications requiring the highest density. Many of these vertical mount modules are maximum 0.65 inch tall, which is well within the board space requirements for card rack type systems. Horizontal mount module options include dual in-line packages (DIPs), and pin grid array packages (PGAs). These modules are ideal for those applications requiring the most in mechanical stability and those with many I/O pins.

Design, manufacturing, and marketing often disagree on the size of memory that their high performance system will offer. By allowing the decision to made at manufacturing time by having module solutions with different memory sizes and common pinouts, the module user lets the market dictate memory requirements. JEDEC has defined standards for memory pinouts including 256K x 32 and 1M x 32 SRAM in the same 72-lead package which are among the most common industry standard SRAM modules.

Testing is both a design and manufacturing problem that is often an afterthought. By providing a pretested higher level block, modules simplify the test issue for both design and manufacturing. Since the module is tested using full parametric AC/DC guardbanded test patterns, designers are guaranteed a level of performance for a larger block of their system versus a spec for an individual component. System board test is simplified because a major block of memory has been fully tested at the module level, thus simplifying the test method and debug cycle at the board level.

Time to market is always a very important issue. Studies have shown that a major portion of profits are made in the early part of the product life cycle before competition drives down prices to a level based on manufacturing costs rather than a unique level of value. Integrating the high performance memory into an module shortens the design cycle by simplifying board design by leveraging off the module manufacturer's design expertise. System board layout and the design cycle are simplified because the number of input/outputs (I/Os) are reduced by combining common component address, data, control and power pins.

Module solutions help reduce hidden costs that are not often taken into account. Since active and passive components necessary to realize an module solution are combined onto a single substrate, the module user reduces inventory and handling costs by combining a number of diverse components into one single component.

IDT Subsystems products provide an ideal solution for system designers to integrate high performance RAM in order to maximize density, performance and cost-effectiveness for both commercial and military applications.

TABLE OF CONTENTS

SUBSYSTEMS PRODUCTS

Integrated Device Technology, Inc.

32K x 32/64K x 32 CMOS DUAL-PORT STATIC RAM MODULES

PRELIMINARY
IDT7MP1015
IDT7MP1016

FEATURES

- Pin compatible 1Mb/2Mb CMOS Dual-Port static RAM modules
- Fast access times: 25ns
- Fully asynchronous read/write operation from either port
- Separate byte read/write signals for byte control
- Separate upper/lower chip select for 16-bit operation
- Full on-chip hardware support of semaphore signaling between ports
- High density surface mounted TQFP packages on a low cost, multilayer FR-4 substrate
- 64-position dual read-out DIMM (Dual In-line Memory Module) with 128 leads (socket information please reference AMP P/N: 6-382617-4)
- Single 5V (±10%) power supply
- Multiple GND pins and on-board decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

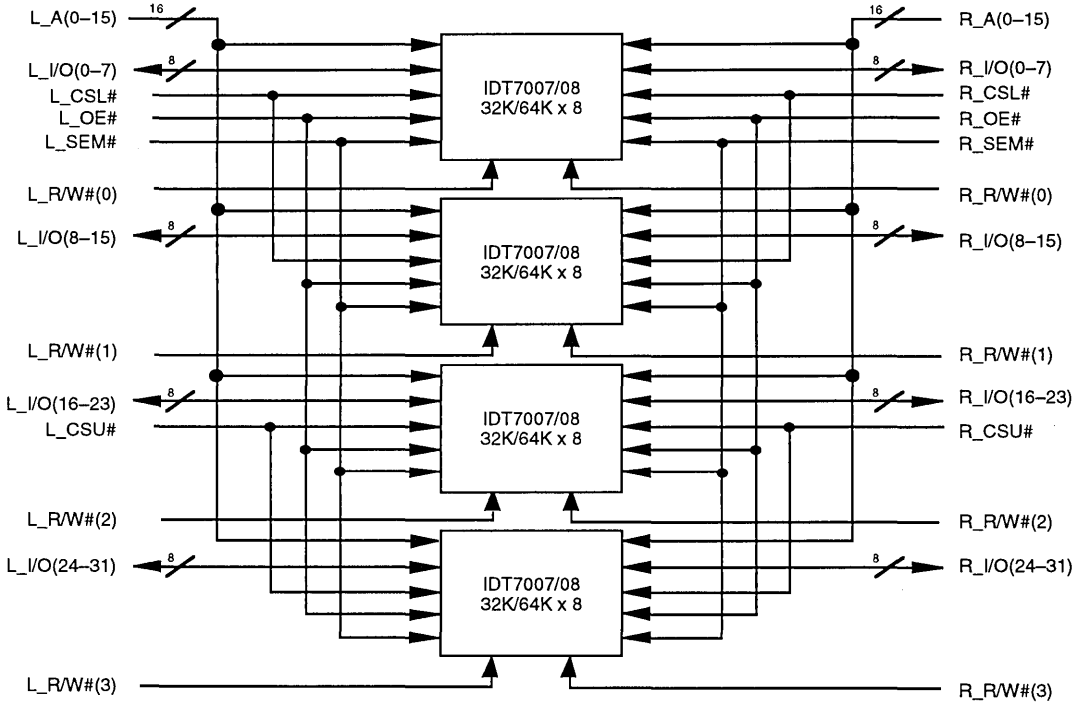
DESCRIPTION

The IDT7MP1015/7MP1016 are 32K x 32/64K x 32 high-speed CMOS Dual-Port Static RAM modules constructed on a low cost, multilayer FR-4 substrate using four IDT7007/08 Dual-Port Static RAMs (in slave mode) using TQFPs. The IDT7MP1015/7MP1016 modules are designed to be used as stand-alone Dual-Port RAM providing two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. Performance is enhanced by facilitating port-to-port communication via semaphore controls.

The IDT7MP1015/7MP1016 modules are packaged in 64-position dual read-out DIMMs (Dual In-line Memory Modules) with 128 leads and dimensions of 1.35" x 0.15" x 1.0" (LxWxH). The module is available with access times as fast as 25ns.

All inputs and outputs of the IDT7MP1015/7MP1016 are TTL-compatible and operate from a single 5V power supply. Multiple GND pins and on-board decoupling capacitors ensure maximum immunity from noise.

FUNCTIONAL BLOCK DIAGRAM



3197 drw 01

The IDT logo is a registered trademark of Integrated Device Technology Inc.

PIN CONFIGURATION [1]

Vcc	1	65	Vcc
L_A(0)	2	66	R_A(0)
L_A(1)	3	67	R_A(1)
L_A(2)	4	68	R_A(2)
L_A(3)	5	69	R_A(3)
L_A(4)	6	70	R_A(4)
L_A(5)	7	71	R_A(5)
L_A(6)	8	72	R_A(6)
L_A(7)	9	73	R_A(7)
GND	10	74	GND
L_A(8)	11	75	R_A(8)
L_A(9)	12	76	R_A(9)
L_A(10)	13	77	R_A(10)
L_A(11)	14	78	R_A(11)
L_A(12)	15	79	R_A(12)
L_A(13)	16	80	R_A(13)
L_A(14)	17	81	R_A(14)
L_A(15)	18	82	R_A(15)
GND	19	83	GND
L_R/W#(0)	20	84	R_R/W#(0)
L_R/W#(1)	21	85	R_R/W#(1)
L_R/W#(2)	22	86	R_R/W#(2)
L_R/W#(3)	23	87	R_R/W#(3)
L_CSL#	24	88	R_CSL#
L_CSU#	25	89	R_CSU#
L_SEM#	26	90	R_SEM#
L_OE#	27	91	R_OE#
Vcc	28	92	Vcc
L_I/O(0)	29	93	R_I/O(0)
L_I/O(1)	30	94	R_I/O(1)
L_I/O(2)	31	95	R_I/O(2)
L_I/O(3)	32	96	R_I/O(3)
L_I/O(4)	33	97	R_I/O(4)
L_I/O(5)	34	98	R_I/O(5)
L_I/O(6)	35	99	R_I/O(6)
L_I/O(7)	36	100	R_I/O(7)
GND	37	101	GND
L_I/O(8)	38	102	R_I/O(8)
L_I/O(9)	39	103	R_I/O(9)
L_I/O(10)	40	104	R_I/O(10)
L_I/O(11)	41	105	R_I/O(11)
L_I/O(12)	42	106	R_I/O(12)
L_I/O(13)	43	107	R_I/O(13)
L_I/O(14)	44	108	R_I/O(14)
L_I/O(15)	45	109	R_I/O(15)
GND	46	110	GND
L_I/O(16)	47	111	R_I/O(16)
L_I/O(17)	48	112	R_I/O(17)
L_I/O(18)	49	113	R_I/O(18)
L_I/O(19)	50	114	R_I/O(19)
L_I/O(20)	51	115	R_I/O(20)
L_I/O(21)	52	116	R_I/O(21)
L_I/O(22)	53	117	R_I/O(22)
L_I/O(23)	54	118	R_I/O(23)
Vcc	55	119	Vcc
L_I/O(24)	56	120	R_I/O(24)
L_I/O(25)	57	121	R_I/O(25)
L_I/O(26)	58	122	R_I/O(26)
L_I/O(27)	59	123	R_I/O(27)
L_I/O(28)	60	124	R_I/O(28)
L_I/O(29)	61	125	R_I/O(29)
L_I/O(30)	62	126	R_I/O(30)
L_I/O(31)	63	127	R_I/O(31)
GND	64	128	GND

DIMM
TOP VIEW

3197 drw 02

NOTE:
1. Pin numbers 18 and 82 are N.C. for the IDT7MP1015.

PIN NAMES

Left Port	Right Port	Description
L_A (0–15)	R_A (0–15)	Address Inputs
L_I/O (0–31)	R_I/O (0–31)	Data Inputs/Outputs
L_R/W# (0–3)	R_R/W# (0–3)	Read/Write Enables
L_CSL#	R_CSL#	Chip Select, Lower 16-bits
L_CSU#	R_CSU#	Chip Select, Upper 16-bits
L_OE#	R_OE#	Output Enable
L_SEM#	R_SEM#	Semaphore Control
N.C.		No Connect
Vcc		Power
GND		Ground

3197 tbl 01

CAPACITANCE[1] (TA = +25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN (1)	Input Capacitance ($\overline{CS}$, $\overline{OE}$, $\overline{SEM}$, Address)	VIN = 0V	40	pF
CIN(2)	Input Capacitance ($R/\overline{W}$, I/O)	VIN = 0V	12	pF
COUT	Output Capacitance (I/O)	VOUT = 0V	12	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

3197 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commerical	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3197 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE:
1. VIL ≥ –3.0V for pulse width less than 20ns

3197 tbl 04

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

3197 tbl 05

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

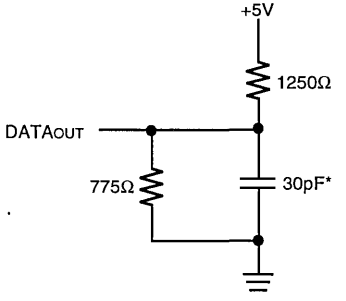
Symbol	Parameter	Test Conditions	Min.	Max.	Units
$\|I_{LI}\|$	Input Leakage (Address & Control)	Vcc = Max. VIN = GND to Vcc	—	40	µA
$\|I_{LI}\|$	Input Leakage (Data)	Vcc = Max. VIN = GND to Vcc	—	10	µA
$\|I_{LO}\|$	Output Leakage (Data)	Vcc = Max. $\overline{CS}$ ≥ VIH, VOUT = GND to Vcc	—	10	µA
V_{OL}	Output Low Voltage	Vcc = Min. IOL = 4mA	—	0.4	V
V_{OH}	Output High Voltage	Vcc = Min, IOH = –4mA	2.4	—	V
I_{CC2}	Dynamic Operating Current (Both Ports Active)	Vcc = Max., $\overline{CS}$ ≤ VIL, $\overline{SEM}$ = Don't Care Outputs Open, f = fMAX	—	1720	mA
I_{SB}	Standby Supply Current (Both Ports Inactive)	Vcc = Max., L_$\overline{CS}$ and R_$\overline{CS}$ ≥ VIH Outputs Open, f = fMAX	—	340	mA
I_{SB1}	Standby Suppy Current (One Port Inactive)	Vcc = Max., L_$\overline{CS}$ or R_$\overline{CS}$ ≥ VIH Outputs Open, f = fMAX	—	1200	mA
I_{SB2}	Full Standby Supply Current (Both Ports Inactive)	L_$\overline{CS}$ and R_$\overline{CS}$ ≥ Vcc – 0.2V VIN > Vcc – 0.2V or < 0.2V L_$\overline{SEM}$ and R_$\overline{SEM}$ ≥ Vcc – 0.2V	—	72	mA

3197 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

3197 tbl 07



3197 drw 03

Figure 1. Output Load
(For t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW})
*Including scope and jig capacitances.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

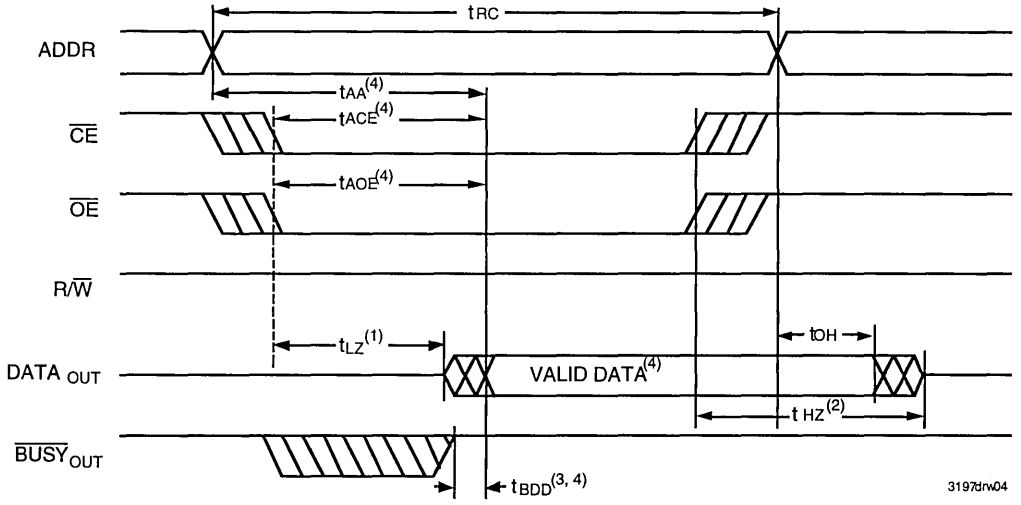
Symbol	Parameter	-25		-30		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	25	—	30	—	ns
t_{AA}	Address Access Time	—	25	—	30	ns
t_{ACS}[2]	Chip Select Access Time	—	25	—	30	ns
t_{OE}	Output Enable Access Time	—	15	—	17	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{LZ}[1]	Output to Low-Z	3	—	3	—	ns
t_{HZ}[1]	Output to High-Z	—	15	—	15	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Up Time	—	50	—	50	ns
t_{SOP}	Sem. Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	ns
Write Cycle						
t_{WC}	Write Cycle Time	25	—	30	—	ns
t_{CW}[2]	Chip Select to End-of-Write	20	—	25	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	25	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	18	—	22	—	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{HZ}[1]	Output to High-Z	—	15	—	15	ns
t_{OW}[1]	Output Active from End-of-Write	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	10	—	ns

NOTES:

3197 tbl 08

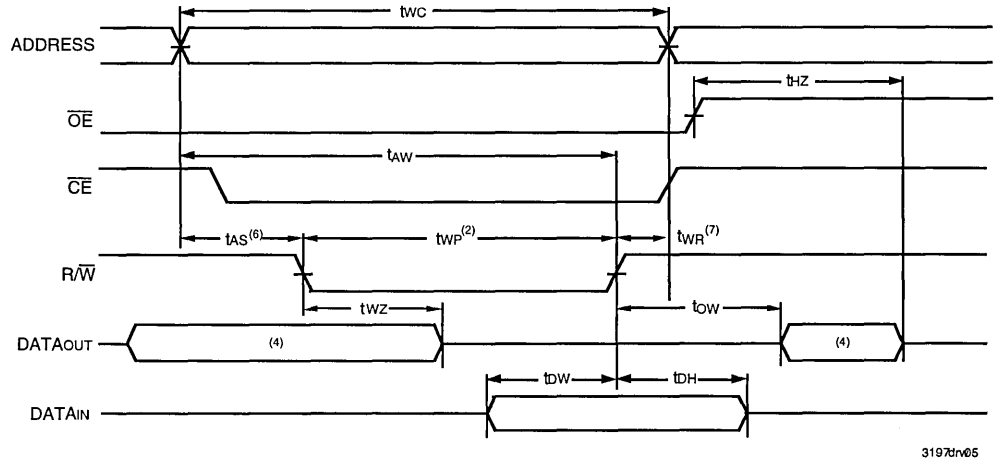
1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.

TIMING WAVEFORM OF READ CYCLES (1, 3, 5)

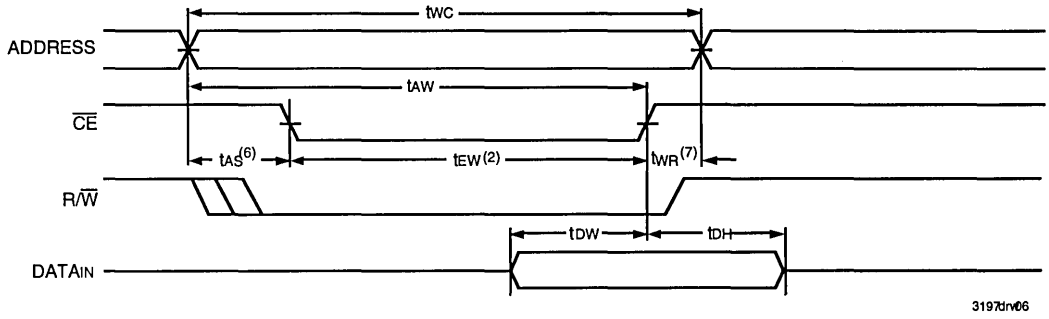


NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is de-asserted first $\overline{CE}$ or $\overline{OE}$.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations $\overline{BUSY}$ has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. $\overline{SEM}$ = HIGH.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1, 2, 4)

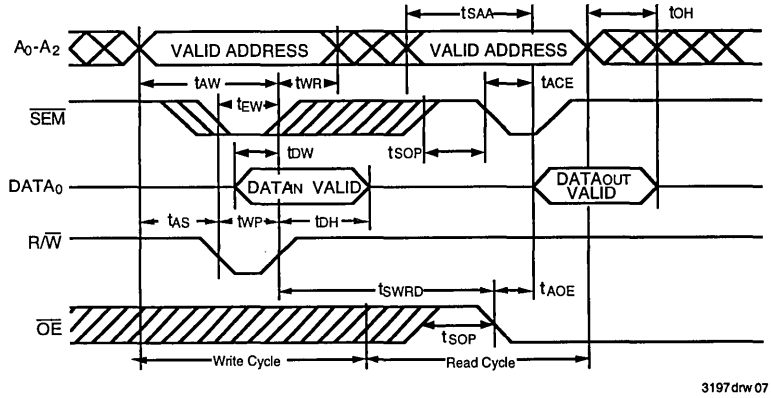


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 4]



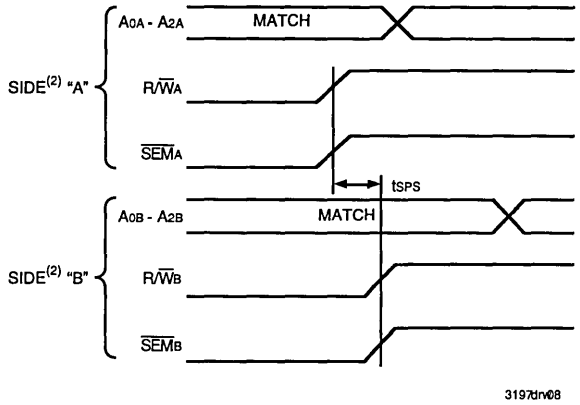
NOTES:
1. R/$\overline{W}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP or tEW) of a LOW $\overline{CS}$ and a LOW R/$\overline{W}$ for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CS}$, or R/$\overline{W}$.
7. Timing depends on which enable signal is de-asserted first, $\overline{CS}$, or R/$\overline{W}$.
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE, EITHER SIDE[1]



NOTE:
1. $\overline{CS}$ = H for the duration of the above timing (both write and read cycle).

TIMING WAVEFORM OF SEMAPHORE CONTENTION[1, 3, 4]



NOTES:
1. $D_{OR} = D_{OL} = L$, ($L\_\overline{CS} = R\_\overline{CS}$) = H, Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going HIGH to $R/\overline{W}_B$ or $\overline{SEM}_B$ going HIGH.
4. If t_{SPS} is not satisfied, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

TRUTH TABLE I: Non-Contention Read/Write Control[1]

Inputs				Outputs	Mode
$\overline{CS}$	$R/\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O	Description
H	X	X	H	High-Z	Deselected or Power Down
L	L	X	H	Data_IN	Write
L	H	L	H	Data_OUT	Read
X	X	H	X	High-Z	Outputs Disabled

NOTE:
1. The conditions for non-contention are L_A (0–13) ≠ R_A (0–13).
2. ⌐ denotes a LOW to HIGH waveform transition.

3197 tbl 09

TRUTH TABLE II: Semaphore Read/Write Control

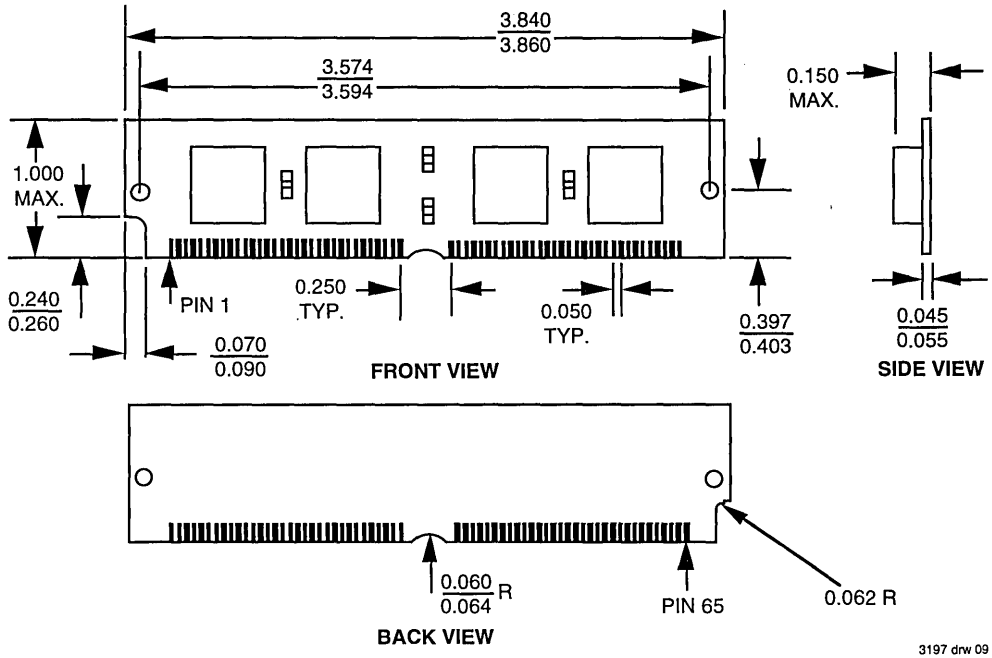
Inputs[2]				Outputs	Mode
$\overline{CS}$	$R/\overline{W}$	$\overline{OE}$	$\overline{SEM}$	I/O	Description
H	H	L	L	Data_OUT	Read Data_IN Semaphore Flag
H	⌐	X	L	Data_IN	Write Data_IN (0, 8, 16, 24)
L	X	X	L	—	Not Allowed

3197 tbl 10

DEPTH/WIDTH EXPANSION AND SEMAPHORES

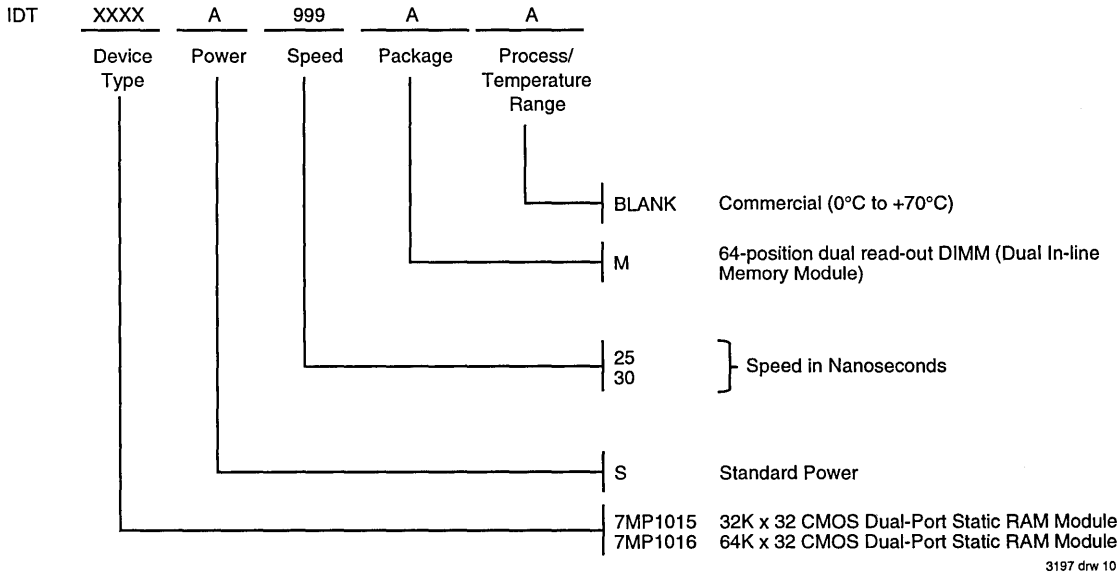
For more details regarding depth/width expansion or semaphore operations, please consult the IDT7007 or IDT7008 data sheets.

PACKAGE DIMENSIONS



3197 drw 09

ORDERING INFORMATION



3197 drw 10

Integrated Device Technology, Inc.

16K x 32 CMOS DUAL-PORT STATIC RAM MODULE

IDT7M1002

FEATURES

- High-density 512K CMOS Dual-Port RAM module
- Fast access times
  - —Commercial: 30, 35ns
  - —Military: 40, 45ns
- Fully asynchronous read/write operation from either port
- Easy to expand data bus width to 64 bits or more using the Master/Slave function
- Separate byte read/write signals for byte control
- On-chip port arbitration logic
- $\overline{INT}$ flag for port-to-port communication
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted fine pitch (25 mil) LCC packages allow through-hole module to fit into 121 pin PGA footprint
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible

DESCRIPTION

The IDT7M1002 is a 16K x 32 high-speed CMOS Dual-Port Static RAM Module constructed on a co-fired ceramic substrate using four 16K x 8 (IDT7006) Dual-Port Static RAMs in surface-mounted LCC packages. The IDT7M1002 module is designed to be used as stand-alone 512K Dual-Port RAM or as a combination Master/Slave Dual-Port RAM for 64-bit or more word width systems. Using the IDT Master/Slave approach in such system applications results in full-speed, error-free operation without the need for additional discrete logic.

The module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via additional control signals $\overline{SEM}$ and $\overline{INT}$.

The IDT7M1002 module is packaged in a ceramic 121 pin PGA (Pin Grid Array) 1.35 inches on a side. Maximum access times as fast as 30ns are available over the commercial temperature range and 40ns over the military temperature range.

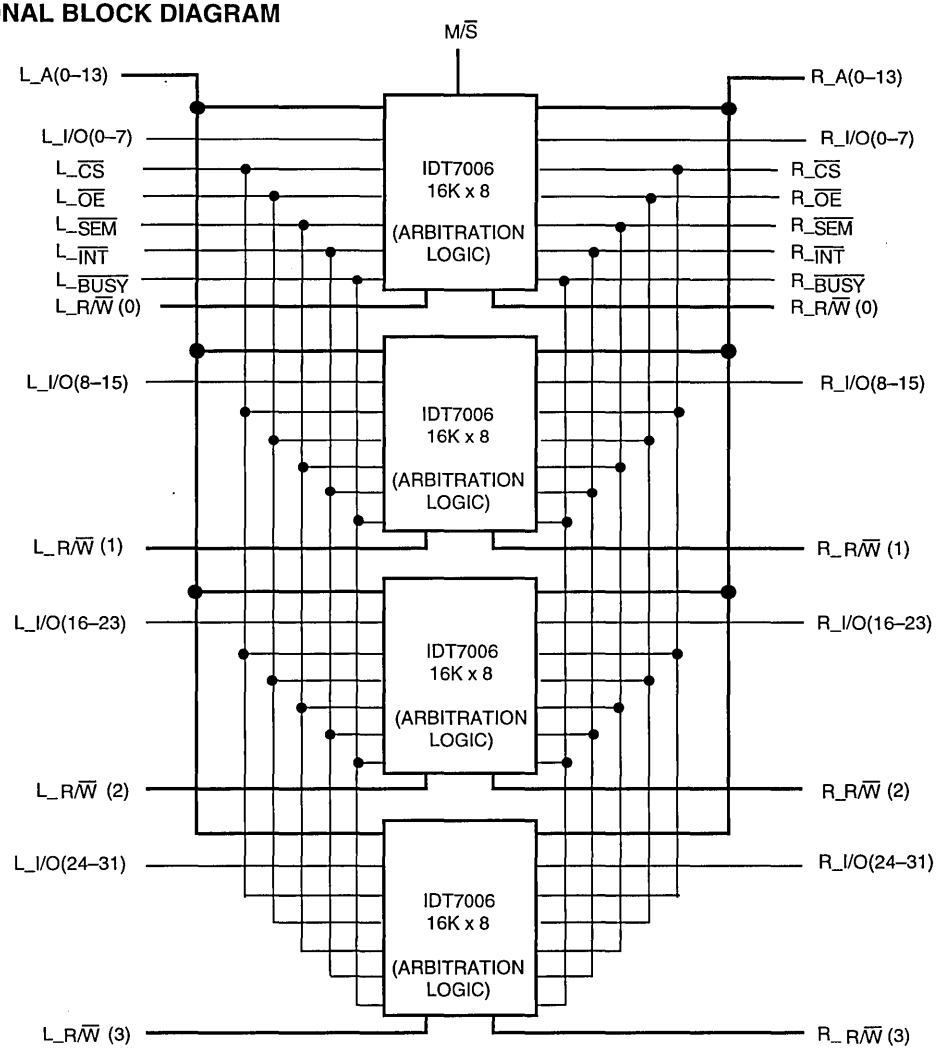
All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	L_I/O(24)	L_I/O(26)	L_I/O(28)	L_I/O(30)	L_$\overline{CS}$	L_$\overline{OE}$	L_R/$\overline{W}$(3)	R_$\overline{OE}$	R_$\overline{CS}$	R_I/O(30)	R_I/O(28)	R_I/O(26)	R_I/O(24)
B	L_I/O(23)	L_I/O(25)	L_I/O(27)	L_I/O(29)	L_I/O(31)	L_A(0)	L_R/$\overline{W}$(4)	R_A(0)	R_I/O(31)	R_I/O(29)	R_I/O(27)	R_I/O(25)	R_I/O(23)
C	L_I/O(21)	L_I/O(22)	VCC	L_A(3)	L_A(2)	L_A(1)	GND	R_A(1)	R_A(2)	R_A(3)	GND	R_I/O(22)	R_I/O(21)
D	L_I/O(19)	L_I/O(20)	L_A(4)	GND							R_A(4)	R_I/O(20)	R_I/O(19)
E	L_I/O(17)	L_I/O(18)	L_A(5)								R_A(5)	R_I/O(18)	R_I/O(17)
F	L_$\overline{SEM}$	L_I/O(16)	L_A(6)								R_A(6)	R_I/O(16)	R_$\overline{SEM}$
G	L_$\overline{BUSY}$	L_$\overline{INT}$	GND				PGA TOP VIEW				GND	R_$\overline{INT}$	R_$\overline{BUSY}$
H	L_R/$\overline{W}$(1)	L_R/$\overline{W}$(2)	L_A(7)								R_A(7)	R_R/$\overline{W}$ (2)	R_R/$\overline{W}$ (1)
I	L_I/O(15)	L_I/O(14)	L_A(8)								R_A(8)	R_I/O(14)	R_I/O(15)
J	L_I/O(13)	L_I/O(12)	L_A(9)								R_A(9)	R_I/O(12)	R_I/O(13)
K	L_I/O(11)	M/$\overline{S}$	GND	L_A(10)	L_A(11)	L_A(12)	GND	R_A(12)	R_A(11)	R_A(10)	VCC	GND	R_I/O(11)
L	L_I/O(10)	L_I/O(8)	L_I/O(6)	L_I/O(4)	L_I/O(2)	L_A(13)	R_R/$\overline{W}$ (4)	R_A(13)	R_I/O(2)	R_I/O(4)	R_I/O(6)	R_I/O(8)	R_I/O(10)
M	L_I/O(9)	L_I/O(7)	L_I/O(5)	L_I/O(3)	L_I/O(1)	L_I/O(0)	R_R/$\overline{W}$ (3)	R_I/O(0)	R_I/O(1)	R_I/O(3)	R_I/O(5)	R_I/O(7)	R_I/O(9)

2795 drw 01

FUNCTIONAL BLOCK DIAGRAM



2795 drw 02

PIN NAMES

Left Port	Right Port	Description
L_A (0–13)	R_A (0–13)	Address Inputs
L_I/O (0–31)	R_I/O (0–31)	Data Inputs/Outputs
L_R/W (1–4)	R_R/W (1–4)	Read/Write Enables
L_CS	R_CS	Chip Select
L_OE	R_OE	Output Enable
L_BUSY	R_BUSY	Busy Flag
L_INT	R_INT	Interrupt Flag
L_SEM	R_SEM	Semaphore Control
M/S		Master/Slave Control
Vcc		Power
GND		Ground

2795 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commerical	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

2795 tbl 02

NOTE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2795 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

2795 tbl 04

NOTE:
1. VIL ≥ –3.0V for pulse width less than 20ns

DC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
|ILI|	Input Leakage (Address & Control)	VCC = Max. VIN = GND to VCC	—	40	µA
|ILI|	Input Leakage (Data)	VCC = Max. VIN = GND to VCC	—	10	µA
|ILO|	Output Leakage (Data)	VCC = Max. $\overline{CS}$ ≥ VIH, VOUT = GND to VCC	—	10	µA
VOL	Output Low Voltage	VCC = Min. IOL = 4mA	—	0.4	V
VOH	Output High Voltage	VCC = Min, IOH = –4mA	2.4	—	V

2795 tbl 05

DC ELECTRICAL CHARACTERISTICS

(VCC = 5V ± 10%, TA = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Commercial		Military		Units
			Min.	Max.	Min.	Max.	
ICC2	Dynamic Operating Current (Both Ports Active)	VCC = Max., $\overline{CS}$ ≤ VIL, $\overline{SEM}$ = Don't Care Outputs Open, f = fMAX	—	1360	—	1600	mA
ISB	Standby Supply Current (Both Ports Inactive)	VCC = Max., L_$\overline{CS}$ and R_$\overline{CS}$ ≥ VIH Outputs Open, f = fMAX	—	280	—	340	mA
ISB1	Standby Suppy Current (One Port Inactive)	VCC = Max., L_$\overline{CS}$ or R_$\overline{CS}$ ≥ VIH Outputs Open, f = fMAX	—	1000	—	1160	mA
ISB2	Full Standby Supply Current (Both Ports Inactive)	L_$\overline{CS}$ and R_$\overline{CS}$ ≥ VCC – 0.2V VIN > VCC – 0.2V or < 0.2V L_$\overline{SEM}$ and R_$\overline{SEM}$ ≥ VCC – 0.2V	—	60	—	120	mA

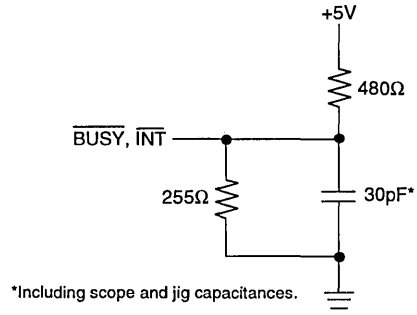
2795 tbl 06

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
$C_{IN(1)}$	Input Capacitance ($\overline{CS}$, $\overline{OE}$, $\overline{SEM}$, Address)	V_{IN} = 0V	40	pF
$C_{IN(2)}$	Input Capacitance (R/$\overline{W}$, $\overline{I/O}$, $\overline{INT}$)	V_{IN} = 0V	12	pF
$C_{IN(3)}$	Input Capacitance ($\overline{BUSY}$, M/$\overline{S}$)	V_{IN} = 0V	45	pF
C_{OUT}	Output Capacitance (I/O)	V_{OUT} = 0V	12	pF

2795 tbl 07

NOTE:
1. This parameter is guaranteed by design but not tested.



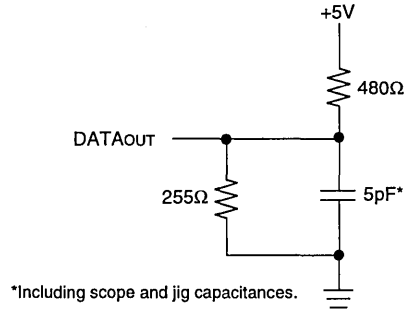
2795 drw 03

Figure 1. Output Load

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2795 tbl 08



2795 drw 04

Figure 2. Output Load
(For t_{CHZ}, t_{CLZ}, t_{OHZ}, t_{OLZ}, t_{WHZ}, t_{OW})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = −55°C to +125°C or 0°C to +70°C)

		7M1002SxxG				7M1002SxxGB				
		30		−35		−40		−45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	30	—	35	—	40	—	45	—	ns
t_{AA}	Address Access Time	—	30	—	35	—	40	—	45	ns
t_{ACS}[2]	Chip Select Access Time	—	30	—	35	—	40	—	45	ns
t_{OE}	Output Enable Access Time	—	17	—	20	—	22	—	25	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{LZ}[1]	Output to Low-Z	3	—	3	—	3	—	5	—	ns
t_{HZ}[1]	Output to High-Z	—	15	—	15	—	17	—	20	ns
t_{PU}[1]	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power Up Time	—	50	—	50	—	50	—	50	ns
t_{SOP}	Sem. Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	15	—	ns
Write Cycle										
t_{WC}	Write Cycle Time	30	—	35	—	40	—	45	—	ns
t_{CW}[2]	Chip Select to End-of-Write	25	—	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	25	—	30	—	35	—	40	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	35	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns

2795 tbl 09

(Continued on next page)

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 55°C to +125°C or 0°C to +70°C)

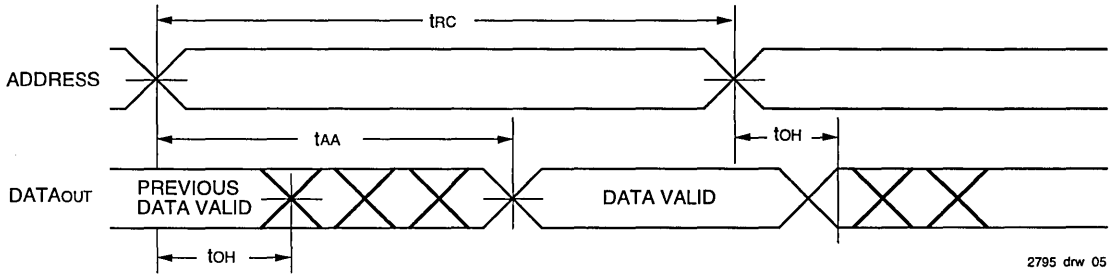
		7M1002SxxG				7M1002SxxGB				
		30		–35		–40		–45		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Write Cycle (continued)										
t_{DW}	Data Valid to End-of-Write	22	—	25	—	25	—	25	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{HZ}[1]	Output to High-Z	—	15	—	15	—	17	—	20	ns
t_{OW}[1]	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	10	—	10	—	10	—	10	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	10	—	10	—	10	—	10	—	ns
Busy Cycle-Master Mode[3]										
t_{BAA}	$\overline{BUSY}$ Access Time to Address	—	30	—	35	—	35	—	35	ns
t_{BDA}	$\overline{BUSY}$ Disable Time to Address	—	25	—	30	—	30	—	30	ns
t_{BAC}	$\overline{BUSY}$ Access Time to Chip Select	—	25	—	30	—	30	—	30	ns
t_{BDC}	$\overline{BUSY}$ Disable Time to Chip Deselect	—	25	—	25	—	25	—	25	ns
t_{WDD}[5]	Write Pulse to Data Delay	—	55	—	60	—	65	—	70	ns
t_{DDD}	Write Data Valid to Read Data Delay	—	40	—	45	—	50	—	55	ns
t_{APS}[6]	Arbitration Priority Set-Up Time	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Time	—	NOTE 9	—	NOTE 9	—	NOTE 9	—	NOTE 9	ns
Busy Cycle-Slave Mode[4]										
t_{WB}[7]	Write to BUSY Input	0	—	0	—	0	—	0	—	ns
t_{WH}[8]	Write Hold after BUSY	25	—	25	—	25	—	25	—	ns
t_{WDD}[5]	Write Pulse to Data Delay	—	55	—	60	—	65	—	70	ns
Interrupt Timing										
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	30	—	32	—	35	ns
t_{INR}	Interrupt Reset Time	—	25	—	30	—	32	—	35	ns

2795 tbl 10

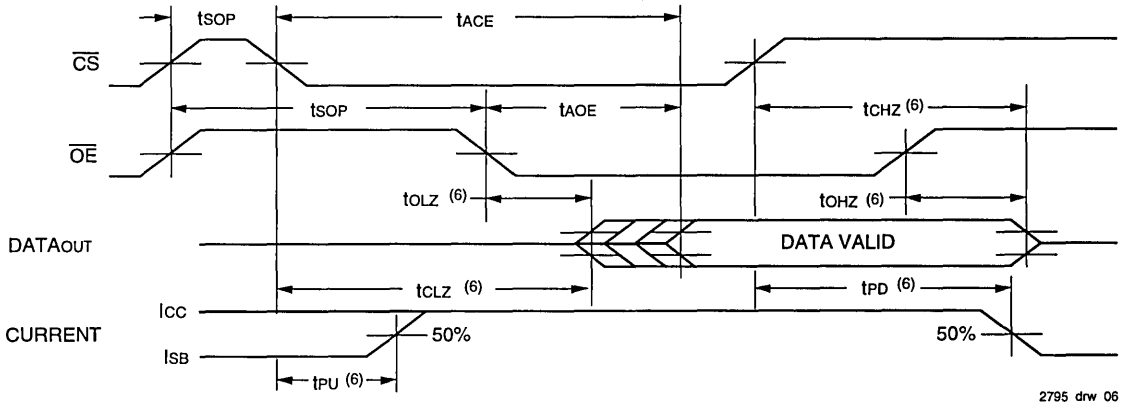
NOTES:
1. This parameter is guaranteed by design but not tested.
2. To access RAM, $\overline{CS} \le V_{IL}$ and $\overline{SEM} \ge V_{IH}$. To access semaphore, $\overline{CS} \ge V_{IH}$ and $\overline{SEM} \le V_{IL}$.
3. When the module is being used in the Master Mode ($M/\overline{S} \ge V_{IH}$).
4. When the module is being used in the Slave Mode ($M/\overline{S} \le V_{IL}$).
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.
6. To ensure that the earlier of the two ports wins.
7. To ensure that the write cycle is inhibited during contention.
8. To ensure that a write cycle is completed after contention.
9. tBDD is a calculated parameter and is the greater of 0, tWDD - tWP (actual), or tDDD - tWP (actual).

7

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE (1, 2, 4)

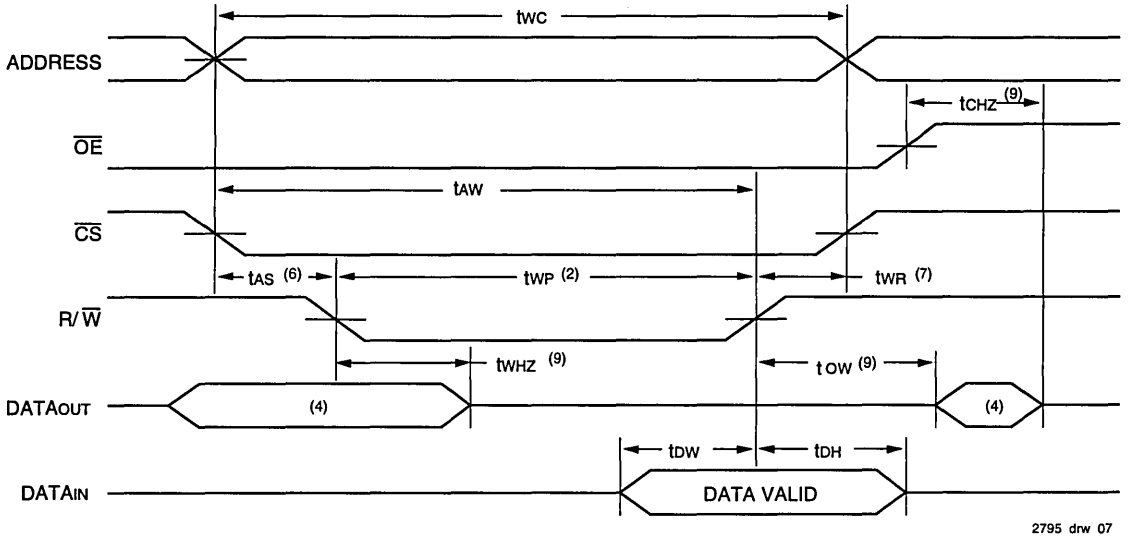


TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE (1, 3, 5)

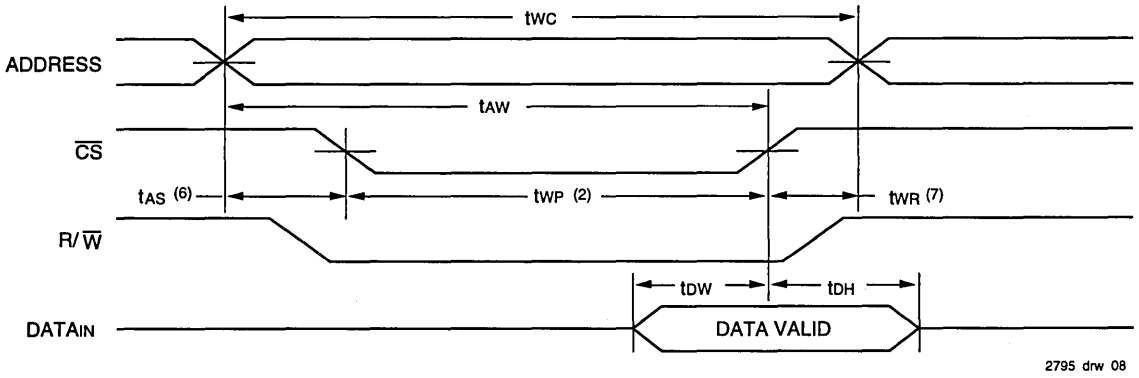


NOTES:
1. R/$\overline{W}$ is HIGH for Read Cycles
2. Device is continuously enabled $\overline{CS} \leq V_{IL}$. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE} \leq V_{IL}$
5. To access RAM, $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
6. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)[1, 2, 4]

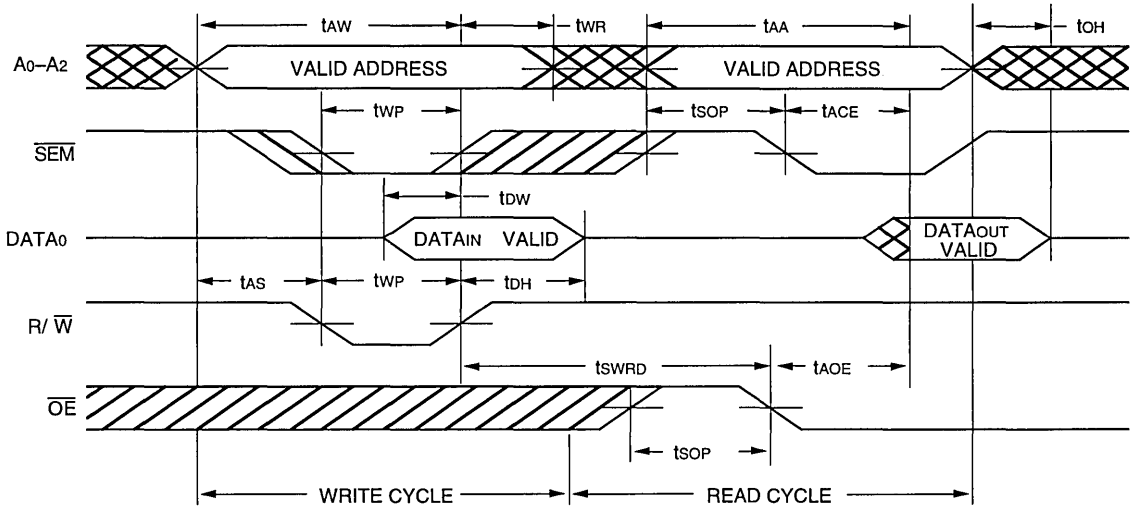


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 4]



NOTES:
1. R/$\overline{W}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (twp) of a LOW $\overline{CS}$ and a LOW R/$\overline{W}$.
3. twR is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ low transition occurs simultaneously with or after the R/$\overline{W}$ low transition, the outputs remain in the high impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of twp or (twz + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.

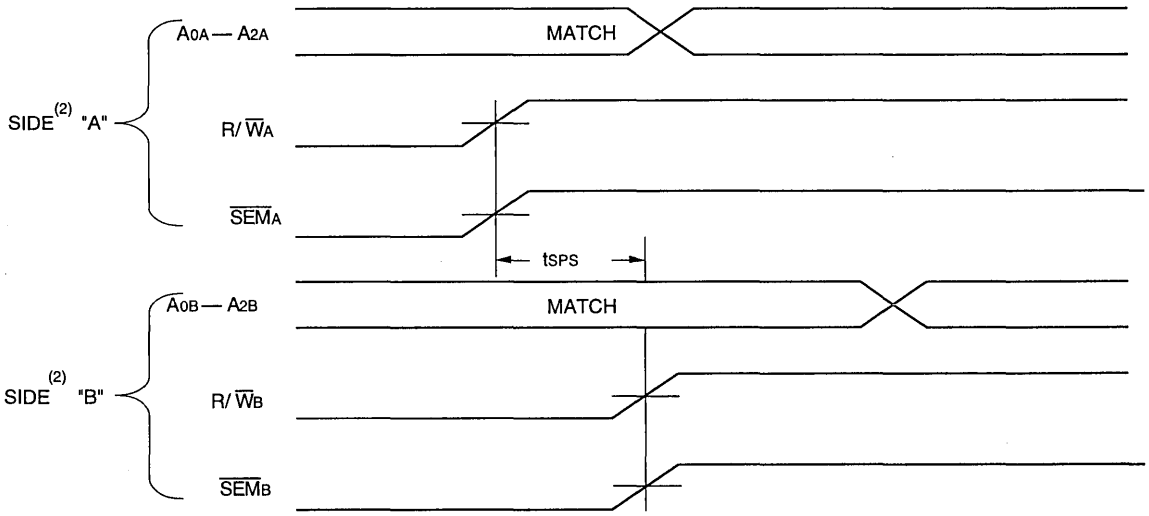
TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE, EITHER SIDE[1]



2795 drw 09

NOTE:
1. $\overline{CS} \geq V_{IH}$ for the duration of the above timing (both write and read cycle).

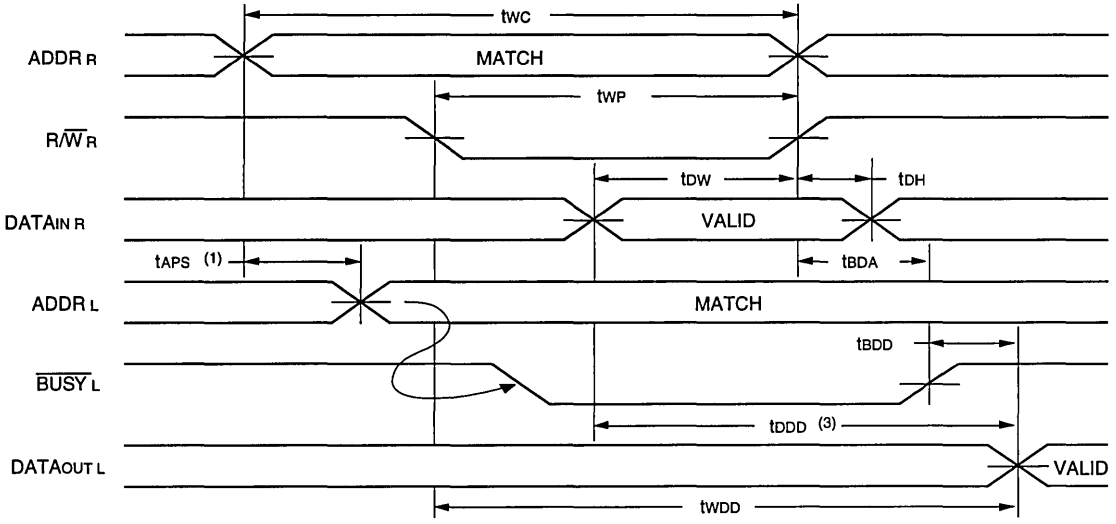
TIMING WAVEFORM OF SEMAPHORE CONTENTION[1, 3, 4]



2795 drw 10

NOTES:
1. $D_{OR} = D_{OL} \leq V_{IL}$ ($L\_\overline{CS} = R\_\overline{CS}$) $\geq V_{IH}$ Semaphore Flag is released from both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going HIGH to $R/\overline{W}_B$ or $\overline{SEM}_B$ going HIGH.
4. If tSPS is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

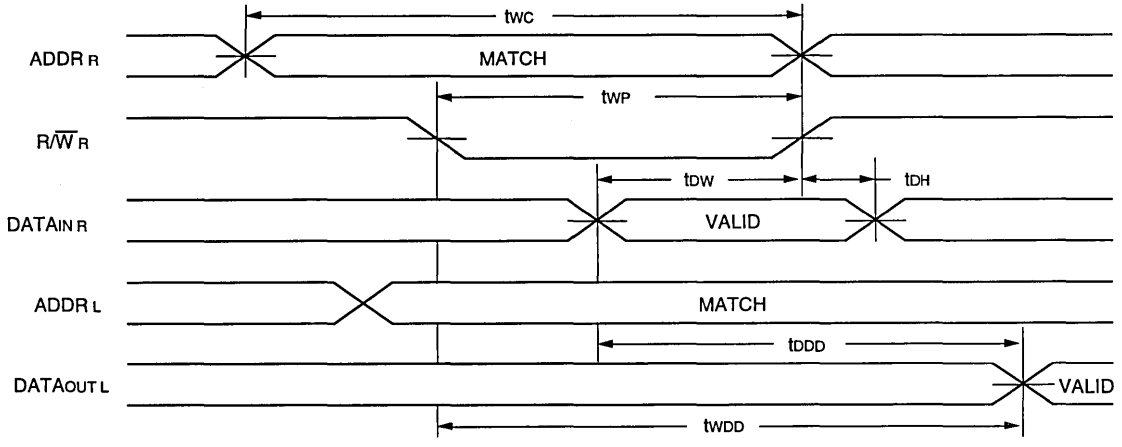
TIMING WAVEFORM OF READ WITH $\overline{BUSY}$ (M/$\overline{S}$ ≥ VIH)[2]



2795 drw 11

NOTES:
1. To ensure that the earlier of the two ports wins.
2. (L_ $\overline{CS}$ = R_ $\overline{CS}$) ≤ VIL
3. $\overline{OE}$ ≤ VIL for the reading port.

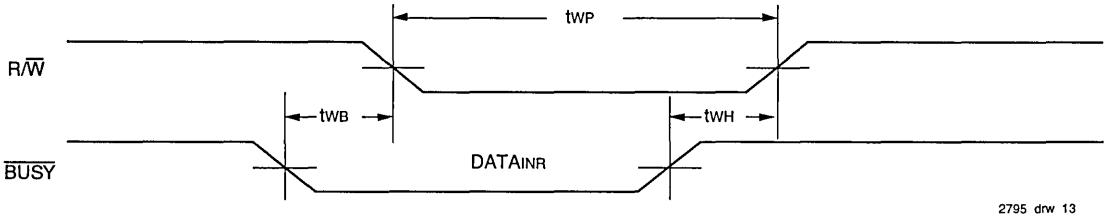
TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY (M/$\overline{S}$ ≤ VIH)[1, 2]



2795 drw 12

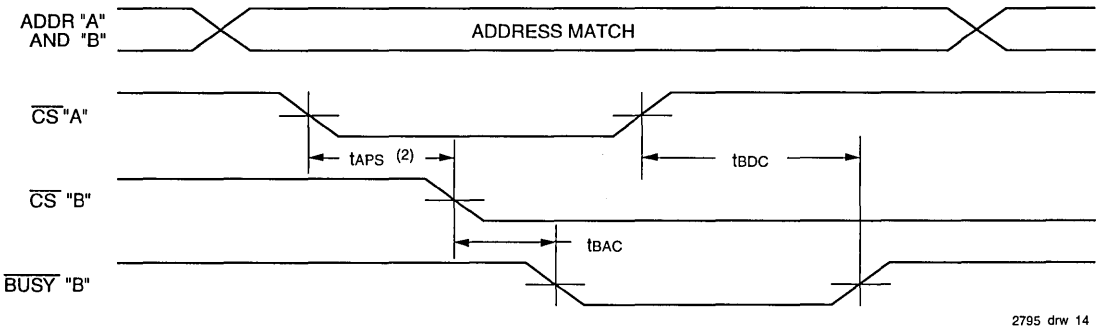
NOTES:
1. $\overline{BUSY}$ input equals HIGH for the writing port.
2. (L_ $\overline{CS}$ = R_ $\overline{CS}$) ≤ VIL

TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ INPUT (M/$\overline{S}$ ≤ VIL)



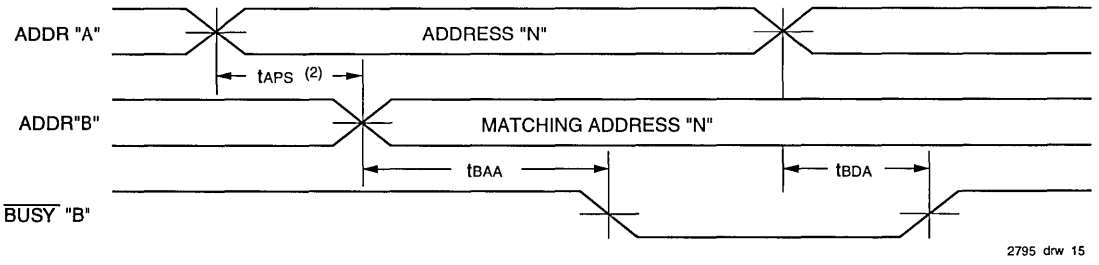
2795 drw 13

TIMING WAVEFORM OF BUSY ARBITRATION ($\overline{CS}$ CONTROLLED TIMING)(1)



2795 drw 14

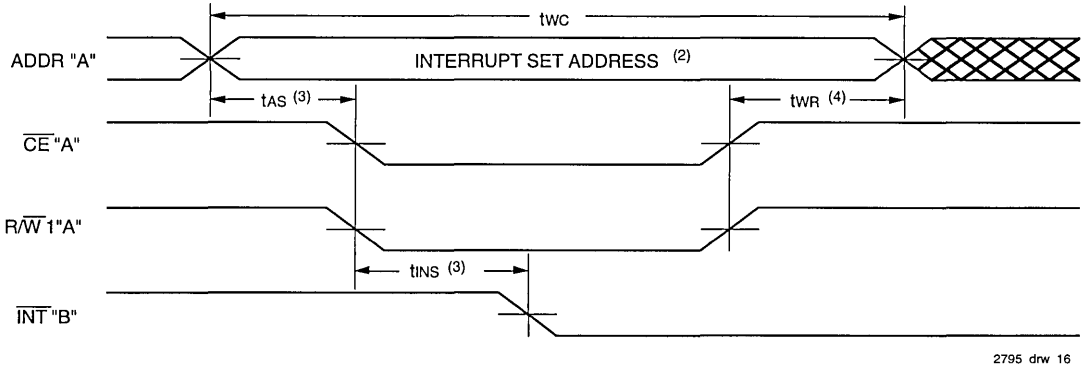
TIMING WAVEFORM OF BUSY ARBITRATION (CONTROLLED BY ADDRESS MATCH TIMING(1)



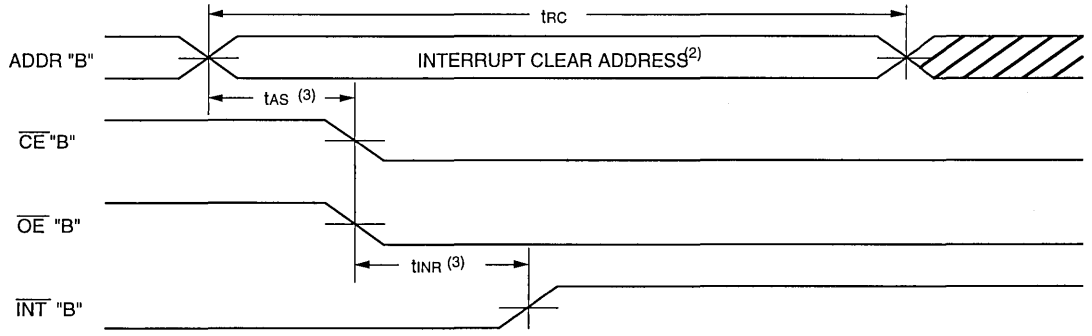
2795 drw 15

NOTES:
1. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is violated, the busy signal will be asserted on one side or another but there is no guarantee on which side busy will be asserted.

TIMING WAVEFORM OF INTERRUPT CYCLE[1]



2795 drw 16



2795 drw 17

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt truth table.
3. Timing depends on which enable signal is asserted last.
4. Timing depends on which enable signal is de-asserted first.

7

TRUTH TABLE I: Non-Contention Read/Write Control[1]

Inputs				Outputs	Mode
$\overline{CS}$	R/W	$\overline{OE}$	$\overline{SEM}$	I/O	Description
H	X	X	H	High-Z	Deselected or Power Down
L	L	X	H	Data_In	Write
L	H	L	H	Data_OUT	Read
X	X	H	X	High-Z	Outputs Disabled

NOTE:
1. The conditions for non-contention are L_A (0–13) ≠ R_A (0–13).
2. ⌐ denotes a LOW to HIGH waveform transition.

2795 tbl 13

TRUTH TABLE II: Semaphore Read/Write Control

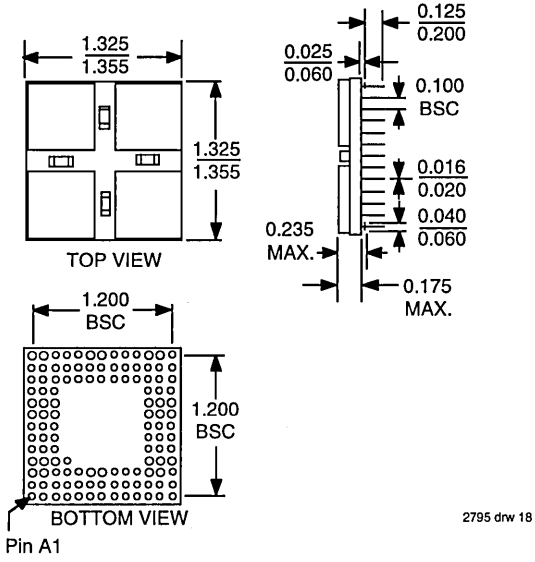
Inputs[2]				Outputs	Mode
$\overline{CS}$	R/W	$\overline{OE}$	$\overline{SEM}$	I/O	Description
H	H	L	L	Data_OUT	Read Data in Semaphore Flag
H	⌐	X	L	Data_IN	Write Data_IN (0, 8, 16, 24)
L	X	X	L	—	Not Allowed

2795 tbl 14

INTERRUPT/BUSY FLAGS, DEPTH & WIDTH EXPANSION, MASTER/SLAVE CONTROL, SEMAPHORES

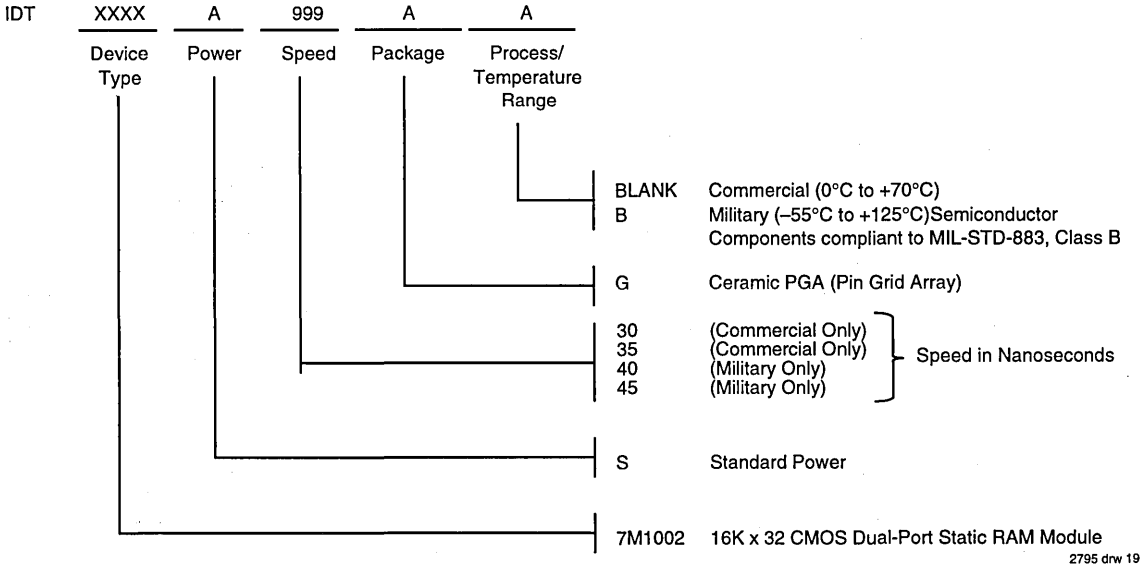
For more details regarding Interrupt/Busy flags, depth and/or width expansion, master/slave control, or semaphore operations, please consult the IDT7006 data sheet.

PACKAGE DIMENSIONS



2795 drw 18

ORDERING INFORMATION



2795 drw 19

Integrated Device Technology, Inc.

4K x 36 BiCMOS DUAL-PORT STATIC RAM MODULE

IDT7M1014

FEATURES

- High-density 4K x 36 BiCMOS Dual-Port Static RAM module
- Fast access times
  - — Commercial: 15, 20ns
  - — Military: 25, 30ns
- Fully asynchronous read/write operation from either port
- Surface mounted LCC packages allow through-hole module to fit on a ceramic PGA footprint
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

DESCRIPTION

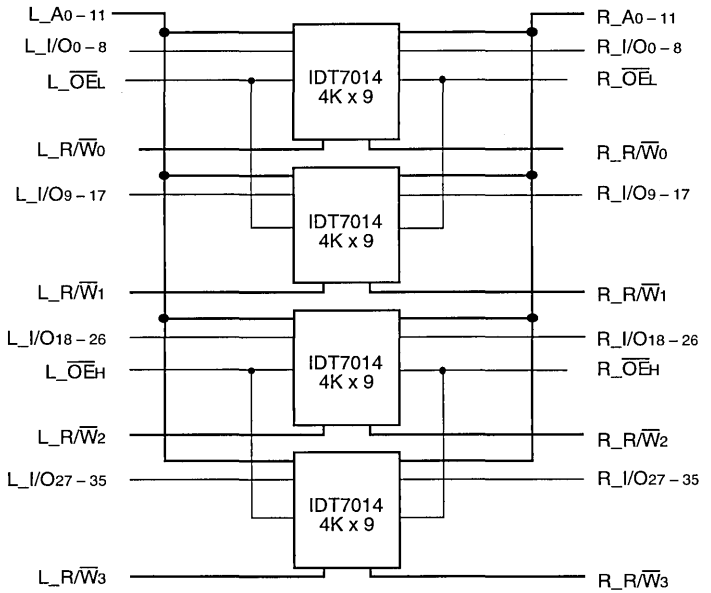
The IDT7M1014 is a 4K x 36 asynchronous high-speed BiCMOS Dual-Port static RAM module constructed on a co-fired ceramic substrate using 4 IDT7014 (4K x 9) asynchronous Dual-Port RAMs. The IDT7M1014 module is designed to be used as stand-alone 36-bit dual-port RAM.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory.

The IDT7M1014 module is packaged in a 142-lead ceramic PGA (Pin Grid Array). Maximum access times as fast as 15ns and 25ns are available over the commercial and military temperature ranges respectively.

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



2819 drw 01

7

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	L_I/O3	L_I/O2	GND	L_I/O1	L_I/O0	GND	R_I/O0	R_I/O1	GND	R_I/O2	R_I/O3	GND
B	L_I/O4	L_I/O5	L_I/O6	L_A2	L_A1	L_A0	N.C.	R_A0	R_A1	R_A2	R_I/O6	R_I/O5	R_I/O4
C	L_I/O8	Vcc	L_I/O7	GND	N.C.	N.C.	N.C.	N.C.	N.C.	GND	R_I/O7	Vcc	R_I/O8
D	L_I/O9	L_I/O10	L_I/O11	L_A3	GND			GND	R_A3	R_A4	R_I/O11	R_I/O10	R_I/O9
E	L_I/O12	N.C.	N.C.	L_A4						R_A5	N.C.	N.C.	R_I/O12
F	L_I/O13	L_$\overline{OE}$ L	L_$\overline{OE}$ H	L_A5						R_A6	R_$\overline{OE}$ H	R_$\overline{OE}$ L	R_I/O13
G	GND	L_R/$\overline{W}$0	L_R/$\overline{W}$1	GND						GND	R_R/$\overline{W}$1	R_R/$\overline{W}$0	GND
H	L_I/O14	L_R/$\overline{W}$2	L_R/$\overline{W}$3	L_A6						R_A7	R_R/$\overline{W}$3	R_R/$\overline{W}$2	R_I/O14
J	L_I/O15	L_I/O16	L_I/O17	L_A7						R_A8	R_I/O17	R_I/O16	R_I/O15
K	L_I/O20	L_I/O19	L_I/O18	GND	L_A10	L_A11	GND	R_A11	R_A10	GND	R_I/O18	R_I/O19	R_I/O20
L	L_I/O21	Vcc	L_I/O22	L_A8	L_A9	L_I/O31	R_I/O35	R_I/O34	R_I/O30	R_A9	R_I/O22	Vcc	R_I/O21
M	L_I/O23	L_I/O24	L_I/O25	L_I/O29	L_I/O30	L_I/O32	L_I/O35	R_I/O33	R_I/O31	R_I/O29	R_I/O25	R_I/O24	R_I/O23
N	GND	L_I/O26	L_I/O27	L_I/O28	GND	L_I/O33	L_I/O34	R_I/O32	GND	R_I/O28	R_I/O27	R_I/O26	GND

2819 drw 02

PIN NAMES

Left Port	Right Port	Names
L_R/$\overline{W}$ 0-3	R_R/$\overline{W}$ 0-3	Byte Read/Write Enables
L_$\overline{OE}$ L, H	R_$\overline{OE}$ L, H	Word Output Enables
L_A 0-11	R_A 0-11	Address Inputs
L_I/O 0-35	R_I/O 0-35	Data Input/Outputs
Vcc		Power
GND		Ground

2819 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTES: 2819 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Inputs and Vcc terminals only.
3. I/O terminals only.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage	2.2	—	6.0	V
V_{IL}	Input LOW Voltage	–0.5(1)	—	0.8	V

NOTE: 2819 tbl 03

1. $V_{IL} \geq -3.0V$ for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2819 tbl 04

CAPACITANCE TABLE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(1)	Input Capacitance (Address)	V_{IN} = 0V	50	pF
C_{IN}(2)	Input Capacitance (Data, R/$\overline{W}$)	V_{IN} = 0V	15	pF
C_{IN}(3)	Input Capacitance ($\overline{OE}$)	V_{IN} = 0V	25	pF
C_{OUT}	Output Capacitance (Data)	V_{OUT} = 0V	15	pF

NOTE: 2819 tbl 05

1. This parameter is guaranteed by design but not tested.

7

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage V_{IN} = GND to V_{CC}	V_{CC} = Max.	—	40	µA
I_{LO}	Output Leakage $\overline{OE} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	V_{CC} = Max.	—	10	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min. I_{OH} = -4mA	2.4	—	V

2819 ttbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{CC}	Operating Current	V_{CC} = Max., Outputs Open, f = f_{MAX}(1)	—	1040	mA

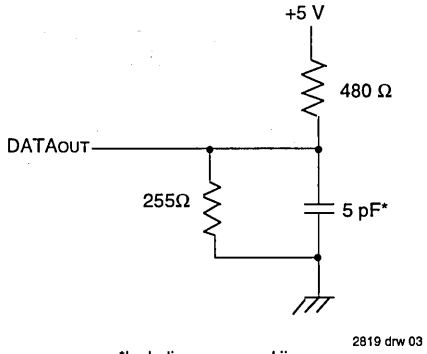
NOTE:
2819 tbl 07

1. At f=f_{MAX}, address and data inputs (except $\overline{OE}$) are cycling at the maximum frequency of read cycle of 1/tRC, and using "AC TEST CONDITIONS" of input levels of GND to 3V.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-3

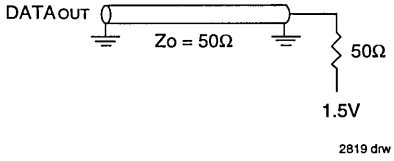
2819 tbl 08



2819 drw 03

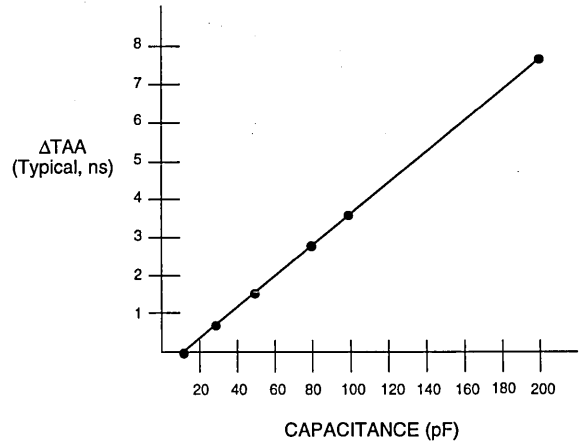
*Including scope and jig.

Figure 1. Output Load
(For tCHZ, tCLZ, tOHZ, tOLZ, tWHZ, tOW)



2819 drw 04a

Figure 2. Alternate Output Load



2819 drw 04b

Figure 3. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

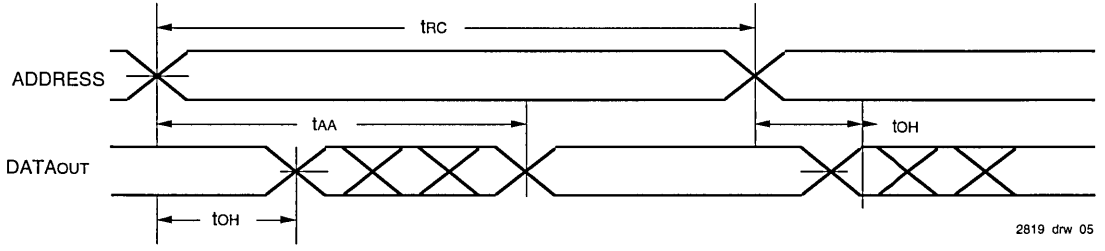
		7M1014SxxG				7M1014SxxGB				
		-15		-20		-25		-30		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20	—	25	—	30	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	—	30	ns
t_{OE}	Output Enable Access Time	—	8	—	10	—	12	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{OHZ}[1]	Output Disable to Output in Hi-Z	—	7	—	9	—	11	—	13	ns
Write Cycle										
t_{WC}	Write Cycle Time	15	—	20	—	25	—	30	—	ns
t_{AW}	Address Valid to End of Write	14	—	15	—	20	—	25	—	ns
t_{AS}	Address Set-Up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	25	—	ns
t_{WR}	Write Recovery Time	1	—	2	—	2	—	2	—	ns
t_{DW}	Data Valid to End of Write	10	—	12	—	15	—	20	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in Hi-Z	—	7	—	9	—	11	—	13	ns
t_{OW}[1]	Output Active from End of Write	0	—	0	—	0	—	0	—	ns
t_{WDD}	Write Pulse to Data Delay	—	30	—	40	—	45	—	50	ns
t_{DDD}[1]	Write Data Valid to Read Data Delay	—	25	—	30	—	35	—	40	ns

NOTES:
1. This parameter is guaranteed by design but not tested.
2. Port-to-Port delay through the RAM cells from the writing port to the reading port.

2819 tbl 09

7

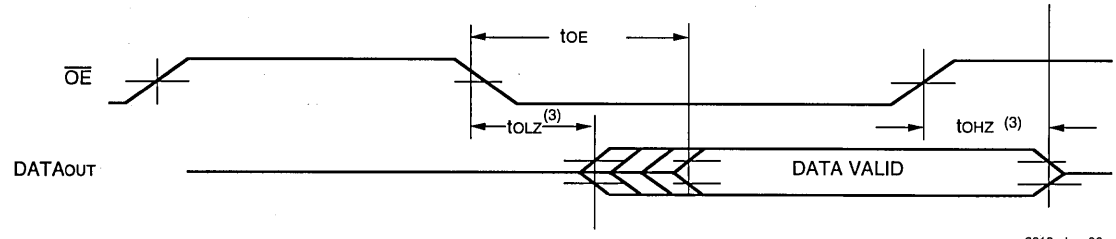
TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE) (1,2)



2819 drw 05

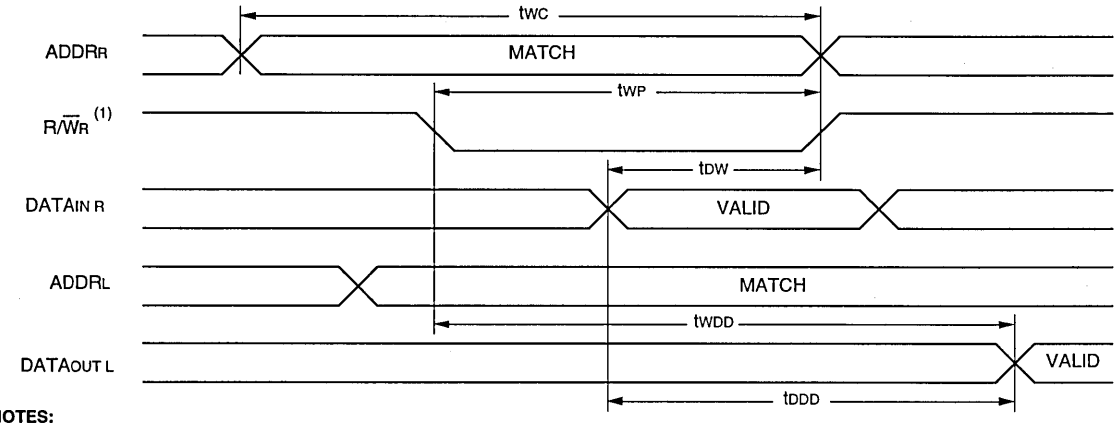
NOTES:
1. R/$\overline{W}$ is HIGH for Read Cycles.
2. $\overline{OE} \leq V_{IL}$.

TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE) (1, 2)



2819 drw 06

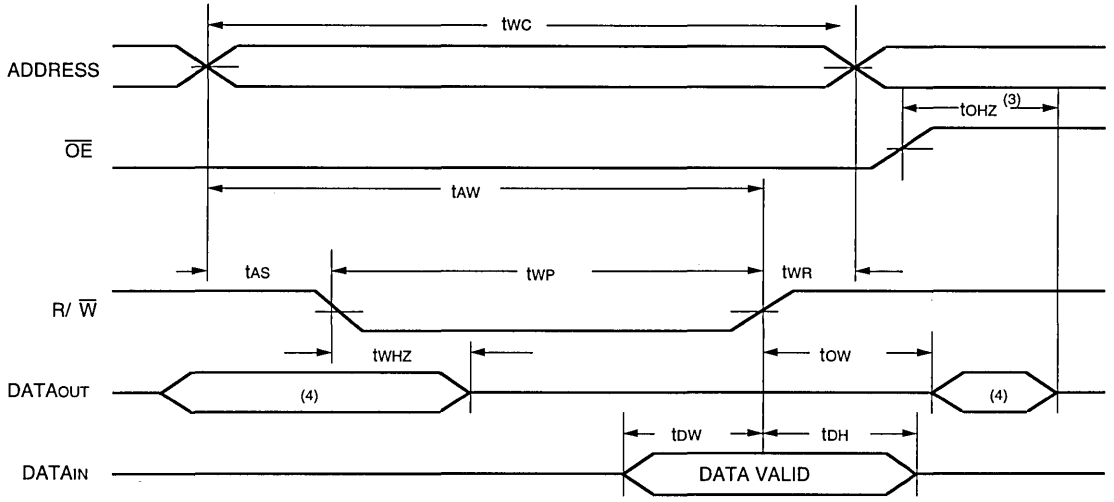
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY



2819 drw 07

NOTES:
1. R/W is HIGH for Read Cycles.
2. Adress valid prior to OE transition LOW.
3. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE (EITHER SIDE) (1,2)

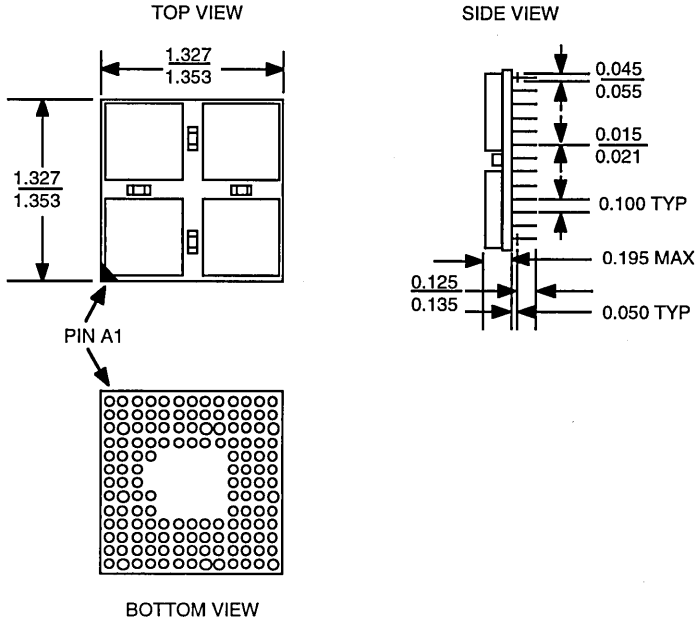


2819 drw 08

NOTES:
1. R/$\overline{W}$ is HIGH during all address transitions.
2. If $\overline{OE}$ is LOW during the write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH, this requirement does not apply, and the write pulse can be as short as the specified tWP.
3. This parameter is guaranteed by design but not tested.
4. During this period, the I/O pins are in the output state and input signals must not be applied.

7

PACKAGE DIMENSIONS



2819 drw 10

ORDERING INFORMATION

IDT	XXXX	A	999	A	A
	Device Type	Power	Speed	Package	Process/ Temperature Range

BLANK	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Semiconductor Components compliant to MIL-STD883, Class B
G	Ceramic PGA (Pin Grid Array)
15	(Commercial Only)
20	(Commercial Only)
25	(Military Only)
30	(Military Only)
	Speed in Nanoseconds
S	Standard Power
7M1014	4K x 36 BiCMOS Dual-Port static RAM Module

2819 drw 10

Integrated Device Technology, Inc.

4K x 36 BiCMOS SYNCHRONOUS DUAL-PORT STATIC RAM MODULE

IDT7M1024

FEATURES:

- High-density 4K x 36 Synchronous Dual-Port SRAM module
- Architecture based on Dual-Port RAM cells
  - — Allows full simultaneous access from both ports
- Synchronous operation
  - — 4ns set-up to clock, 1ns hold on all control, data, and address inputs
  - — Data input, address, and control registers
  - — Fast 20ns clock to data out
  - — Self-timed write allows fast write cycle
- Clock enable feature
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

DESCRIPTION:

The IDT7M1024 is a 4K x 36 bit high-speed synchronous Dual-Port Static RAM module constructed on a co-fired ceramic substrate using four IDT7099 (4K x 9) Dual-Port RAMs. The IDT7M1024 module is designed to be used as a stand-alone 36-bit Dual-Port Static RAM.

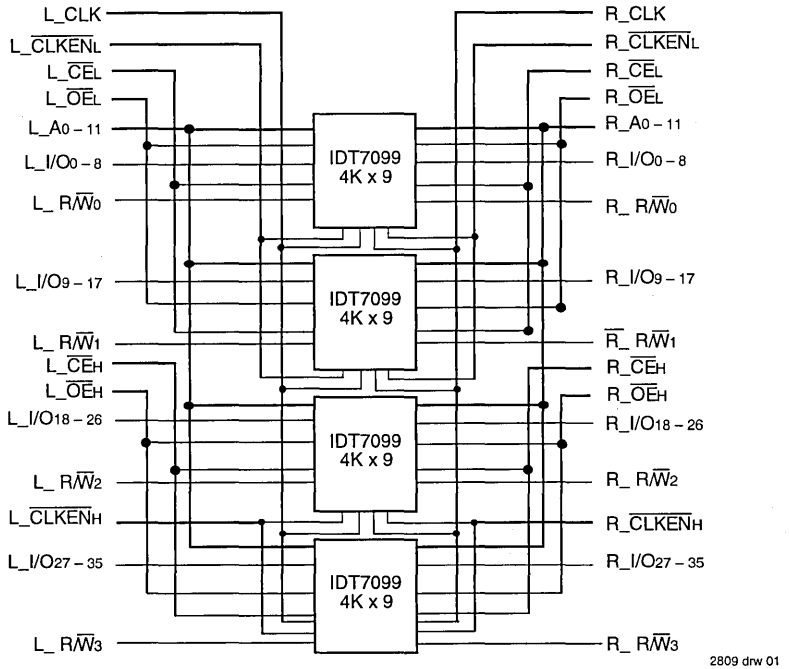
The IDT7M1024 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide very short set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. An asynchronous output enable is provided to ease asynchronous bus interfacing.

The internal write pulse width is independent of the HIGH and LOW periods of the clock. This allows the shortest possible realized cycle times. Clock enable inputs are provided to stall the operation of the address and data input registers without introducing clock skew for very fast interleaved memory applications.

The data inputs are gated to control on-chip noise in bussed applications. The user must guarantee that the R/$\overline{W}$ pins are LOW for at least one clock cycle before any write is attempted. A HIGH on the $\overline{CE}$ input for one clock cycle will power down the internal circuitry to reduce static power consumption.

The IDT7M1024 module is packaged in a 142-lead ceramic

FUNCTIONAL BLOCK DIAGRAM



2809 drw 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PGA (Pin Grid Array).

All IDT military modules are constructed with semiconductor components manufactured in compliance with the latest revision of MIL-STD-883, Class B making them ideally suited to applications demanding the highest level of performance and reliability.

PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	L_I/O3	L_I/O2	GND	L_I/O1	L_I/O0	GND	R_I/O0	R_I/O1	GND	R_I/O2	R_I/O3	GND
B	L_I/O4	L_I/O5	L_I/O6	L_A2	L_A1	L_A0	L_CLK	R_A0	R_A1	R_A2	R_I/O6	R_I/O5	R_I/O4
C	L_I/O8	VCC	L_I/O7	GND	L_$\overline{\text{CLKEN}}$ L	L_$\overline{\text{CLKEN}}$ H	R_CLK	R_$\overline{\text{CLKEN}}$ H	R_$\overline{\text{CLKEN}}$ L	GND	R_I/O7	VCC	R_I/O8
D	L_I/O9	L_I/O10	L_I/O11	L_A3	GND			GND	R_A3	R_A4	R_I/O11	R_I/O10	R_I/O9
E	L_I/O12	L_$\overline{\text{CE}}$ L	L_$\overline{\text{CE}}$ H	L_A4						R_A5	R_$\overline{\text{CE}}$ H	R_$\overline{\text{CE}}$ L	R_I/O12
F	L_I/O13	L_$\overline{\text{OE}}$ L	L_$\overline{\text{OE}}$ H	L_A5						R_A6	R_$\overline{\text{OE}}$ H	R_$\overline{\text{OE}}$ L	R_I/O13
G	GND	L_R/$\overline{\text{W}}$0	L_R/$\overline{\text{W}}$1	GND						GND	R_R/$\overline{\text{W}}$1	R_R/$\overline{\text{W}}$0	GND
H	L_I/O14	L_R/$\overline{\text{W}}$2	L_R/$\overline{\text{W}}$3	L_A6						R_A7	R_R/$\overline{\text{W}}$3	R_R/$\overline{\text{W}}$2	R_I/O14
J	L_I/O15	L_I/O16	L_I/O17	L_A7						R_A8	R_I/O17	R_I/O16	R_I/O15
K	L_I/O20	L_I/O19	L_I/O18	GND	L_A10	L_A11	GND	R_A11	R_A10	GND	R_I/O18	R_I/O19	R_I/O20
L	L_I/O21	VCC	L_I/O22	L_A8	L_A9	L_I/O31	R_I/O35	R_I/O34	R_I/O30	R_A9	R_I/O22	VCC	R_I/O21
M	L_I/O23	L_I/O24	L_I/O25	L_I/O29	L_I/O30	L_I/O32	L_I/O35	R_I/O33	R_I/O31	R_I/O29	R_I/O25	R_I/O24	R_I/O23
N	GND	L_I/O26	L_I/O27	L_I/O28	GND	L_I/O33	L_I/O34	R_I/O32	GND	R_I/O28	R_I/O27	R_I/O26	GND

2809 drw 02

PIN NAMES

Left Port	Right Port	Names
L_R/$\overline{\text{W}}$ 0-3	R_R/$\overline{\text{W}}$ 0-3	Byte Read/Write Enables
L_$\overline{\text{OE}}$ L, H	R_$\overline{\text{OE}}$ L, H	Word Output Enables
L_$\overline{\text{CE}}$ L, H	R_$\overline{\text{CE}}$ L, H	Word Chip Enables
L_$\overline{\text{CLKEN}}$ L, H	R_$\overline{\text{CLKEN}}$ L, H	Word Clock Enables
L_CLK	R_CLK	Clock Inputs
L_A 0-11	R_A 0-11	Address Inputs
L_I/O 0-35	R_I/O 0-35	Data Input/Outputs
Vcc		Power
GND		Ground

2809 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage	–0.5 to Vcc	–0.5 to Vcc	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2809 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Inputs and Vcc terminals only.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2809 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input HIGH Voltage	2.2	—	6.0	V
V_{IL}	Input LOW Voltage	–0.5(1)	—	0.8	V

2809 tbl 04

NOTE:
1. V_{IL} = -3.0V for pulse width less than 20ns.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	50	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

2809 tbl 05

TRUTH TABLES

TRUTH TABLE I: READ/WRITE CONTROL (1)

Inputs				Outputs	
Synchronous			Asynchronous		
Clk	$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	I/O_{0-35}	Mode
↑	h	h	X	High-Z	Deselected, Power Down, Data I/O Disabled
↑	h	l	X	$DATA_{IN}$	Deselected, Power Down, Data Input Enabled
↑	l	l	X	$DATA_{IN}$	Write
↑	l	h	L	$DATA_{OUT}$	Read
↑	l	h	H	High-Z	Data I/O Disabled

2809 tbl 06

TRUTH TABLE II: CLOCK ENABLE FUNCTION TABLE (1)

	Inputs		Register Inputs		Register Outputs	
Operating Mode	Clk	$\overline{CLKEN}$	ADDR	$DATA_{IN}$	ADDR	$DATA_{OUT}$
Load "1"	↑	l	h	h	H	H
Load "0"	↑	l	l	l	L	L
Hold (do nothing)	↑	h	X	X	N/C	N/C
	X	H	X	X	N/C	N/C

2809 tbl 07

NOTE:
1. H = HIGH voltage level steady state, h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition, L =LOW voltage level steady state l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition, X = Don't care, N/C = No change

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT7M1024 Min.	IDT7M1024 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	40	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = VIH, V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output LOW Voltage	I_{OL} = 4mA	—	0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA	2.4	—	V

2809 tbl 08

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version	IDT7M1024SxxG, IDT7M1024SxxGB –20 Typ.	–20 Max.	–25 Typ.	–25 Max.	–30 Typ.	–30 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \le V_{IL}$ Outputs Open f = f_{MAX}(1)	Mil.	—	—	—	1480	—	1440	mA
			Com'l.	—	1440	—	1360	—	—	
I_{SB1}	Standby Current (Both Ports—TTL Level Inputs)	L_$\overline{CE}$ and R_$\overline{CE}$ ≥ V_{IH} f = f_{MAX}(1)	Mil.	—	—	—	680	—	560	mA
			Com'l.	—	720	—	640	—	—	
I_{SB2}	Standby Current (One Port—TTL Level Inputs)	L_$\overline{CE}$ or R_$\overline{CE}$ ≥ V_{IH} Active Port Outputs Open, f = f_{MAX}(1)	Mil.	—	—	—	1080	—	1000	mA
			Com'l.	—	1080	—	1000	—	—	
I_{SB3}	Full Standby Current (Both Ports—CMOS Level Inputs)	Both Ports R_$\overline{CE}$ and L_$\overline{CE}$ ≥ V_{CC} – 0.2V $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, f = 0(2)	Mil.	—	—	—	80	—	80	mA
			Com'l.	—	40	—	40	—	—	
I_{SB4}	Full Standby Current (One Port—CMOS Level Inputs)	One Port L_$\overline{CE}$ or R_$\overline{CE}$ ≥ V_{CC} – 0.2V, $V_{IN} \ge V_{CC}$ – 0.2V or $V_{IN} \le$ 0.2V, Active Port Outputs Open, f = f_{MAX}(1)	Mil.	—	—	—	1040	—	960	mA
			Com'l.	—	1040	—	960	—	—	

NOTES:

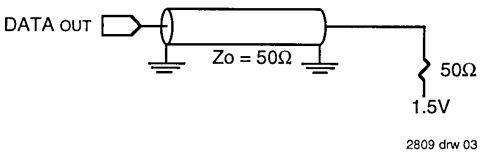
2809 tbl 09

1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/tCLK, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to inputs at CMOS level standby.

AC TEST CONDITIONS

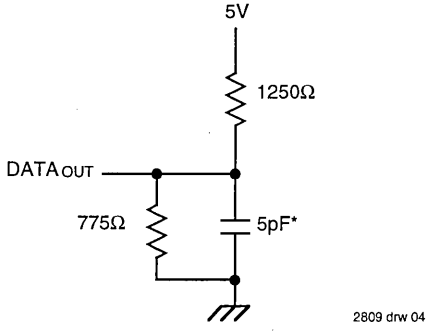
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1, 2 and 3

2909 tbl 10



2809 drw 03

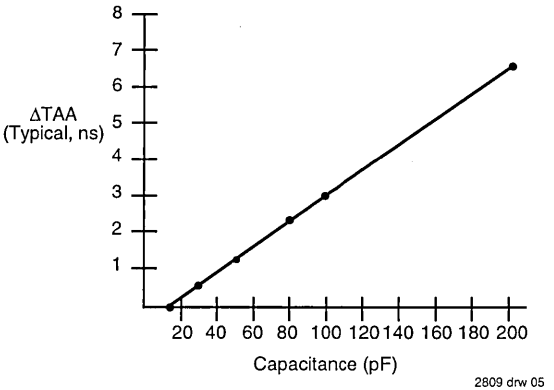
Figure 1. Output Load



2809 drw 04

Figure 2. Output Load (for tCLZ, tCHZ, tOLZ, and tOHZ)

*Including scope and jig.



2809 drw 05

Figure 3. Lumped Capacitive Load, Typical Derating

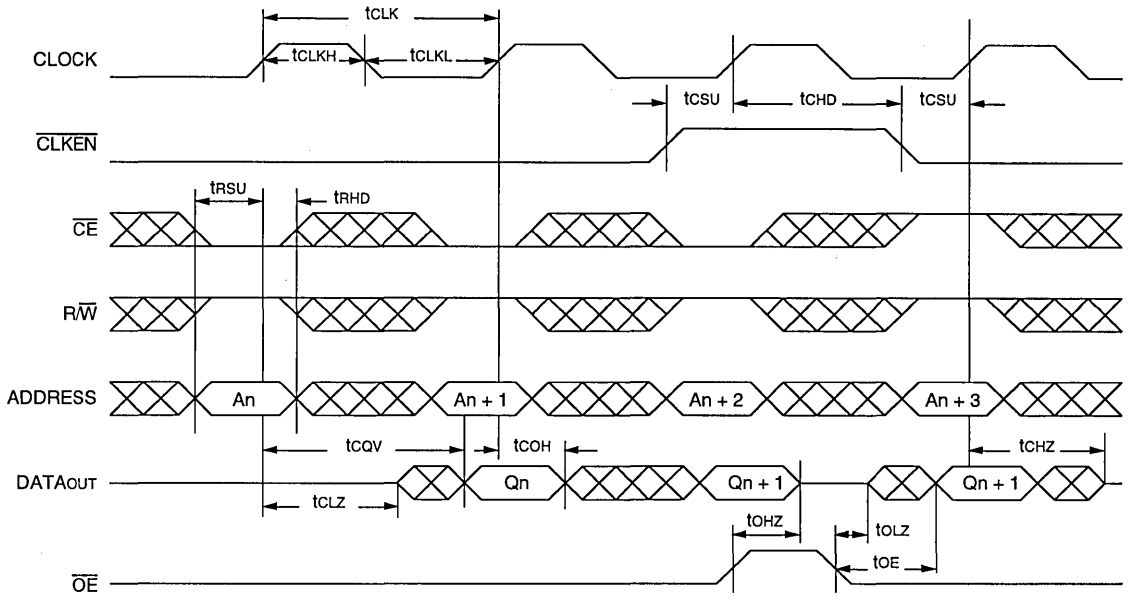
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE RANGE — (READ AND WRITE CYCLE TIMING)

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		7M1024SxxG, 7M1024SxxGB						
		–20		–25		–30		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
tCLK	Clock Cycle Time	20	—	25	—	30	—	ns
tCLKH	Clock HIGH Time	8	—	10	—	12	—	ns
tCLKL	Clock LOW Time	8	—	10	—	12	—	ns
tCQV	Clock HIGH to Output Valid	—	20	—	25	—	30	ns
tRSU	Registered Signal Set-up Time	5	—	6	—	7	—	ns
tRHD	Registered Signal Hold Time	2	—	2	—	2	—	ns
tCOH	Data Output Hold After Clock HIGH	3	—	3	—	3	—	ns
tCLZ	Clock HIGH to Output Low-Z	2	—	2	—	2	—	ns
tCHZ	Clock HIGH to Output High-Z	2	9	2	12	2	15	ns
tOE	Output Enable to Output Valid	—	10	—	12	—	15	ns
tOLZ	Output Enable to Output Low-Z	0	—	0	—	0	—	ns
tOHZ	Output Disable to Output High-Z	—	9	—	11	—	14	ns
tCSU	Clock Enable, Disable Set-up Time	5	—	6	—	7	—	ns
tCHD	Clock Enable, Disable Hold Time	3	—	3	—	3	—	ns
Port-to-Port Delay								
tCWDD	Write Port Clock HIGH to Read Data Delay	—	35	—	45	—	55	ns

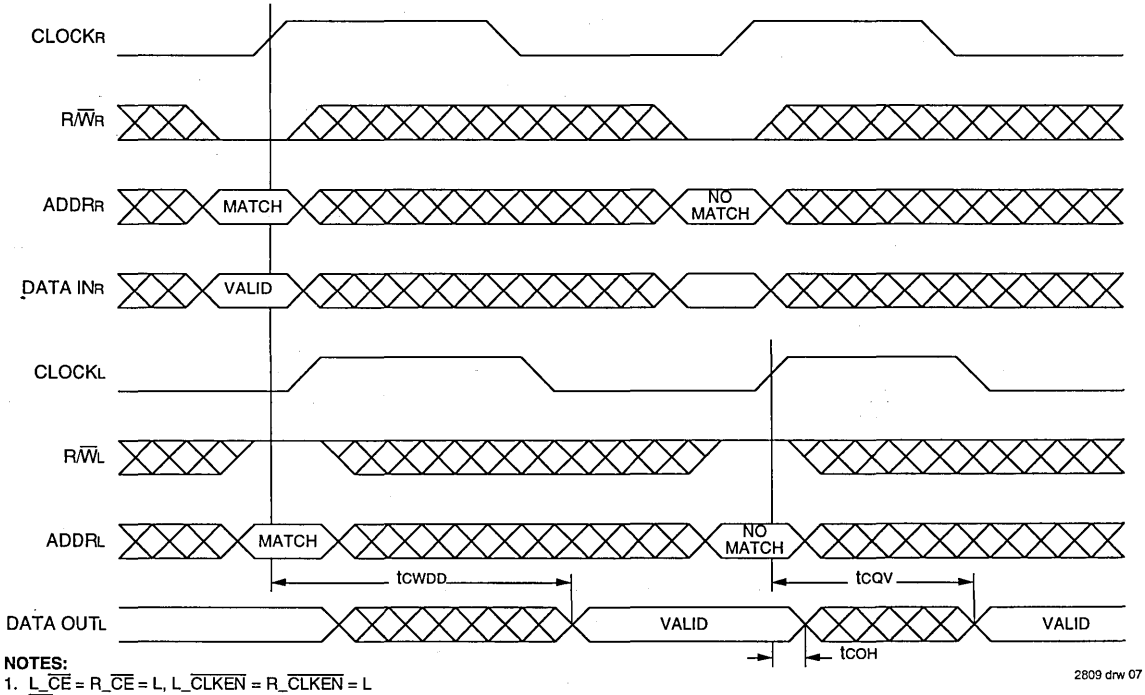
2809 tbl 11

TIMING WAVEFORM OF READ CYCLE, EITHER SIDE(1,2)



2809 drw 06

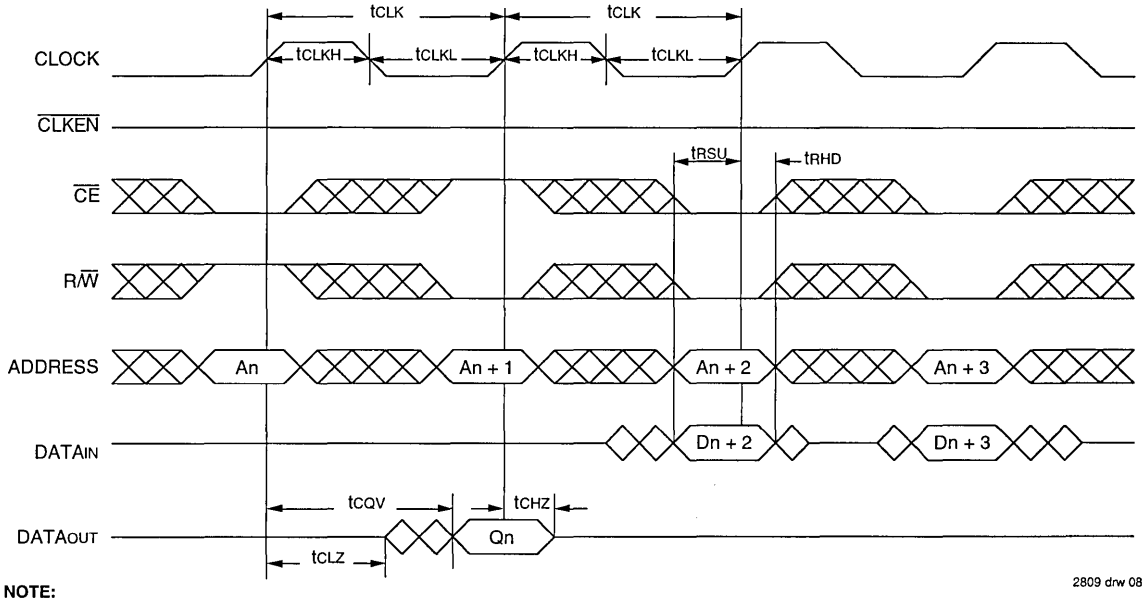
TIMING WAVEFORM OF READ CYCLE WITH PORT-TO-PORT DELAY



NOTES:
1. L_CE = R_CE = L, L_CLKEN = R_CLKEN = L
2. OE = L for the reading port.

2809 drw 07

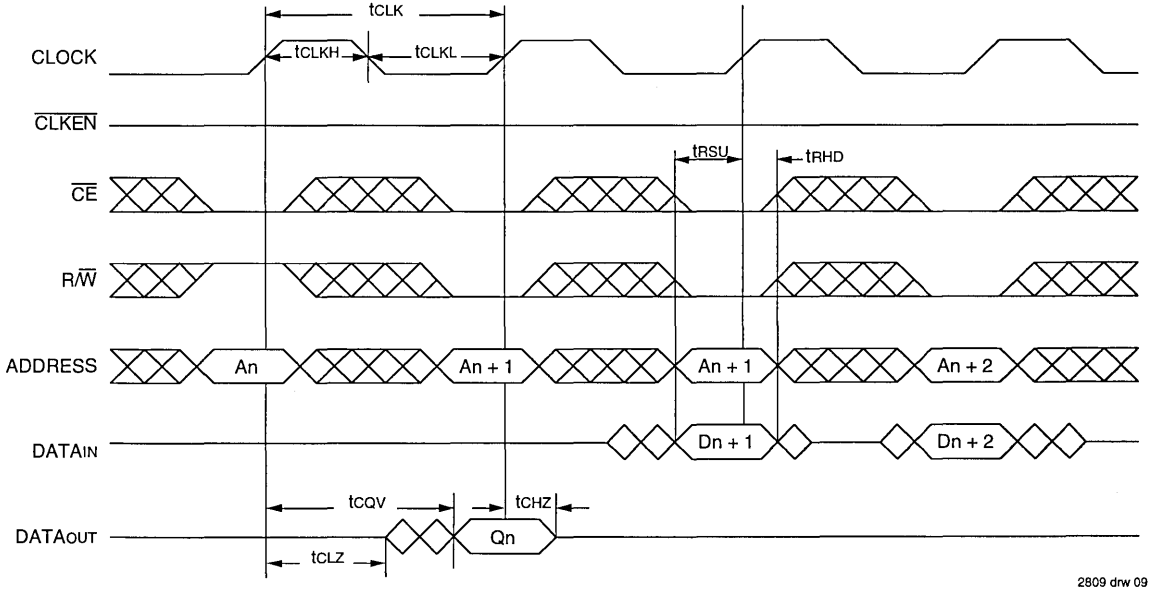
TIMING WAVEFORM OF READ-TO-WRITE CYCLE No. 1, CE HIGH[1]



2809 drw 08

NOTE:
1. $\overline{OE}$ LOW throughout.

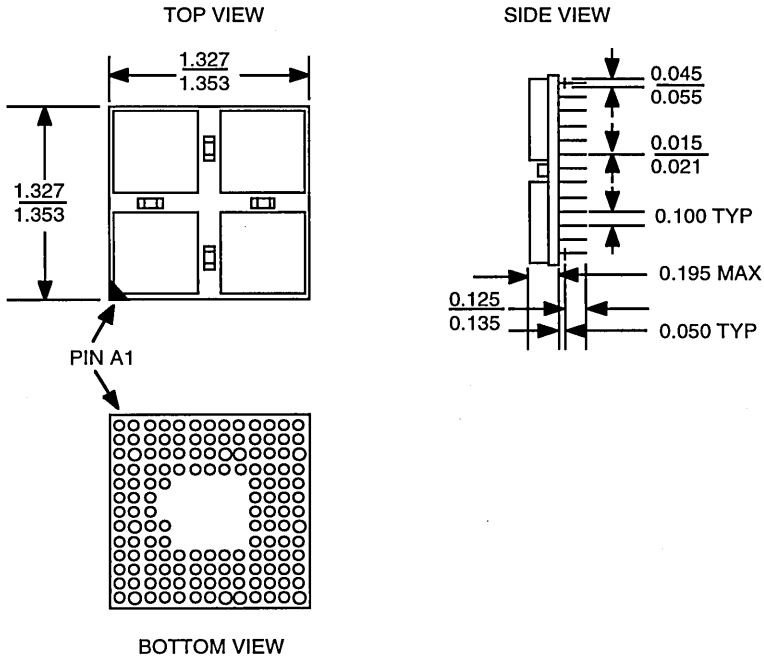
TIMING WAVEFORM OF READ-TO-WRITE CYCLE NO. 1, $\overline{CE}$ LOW[1,2]



2809 drw 09

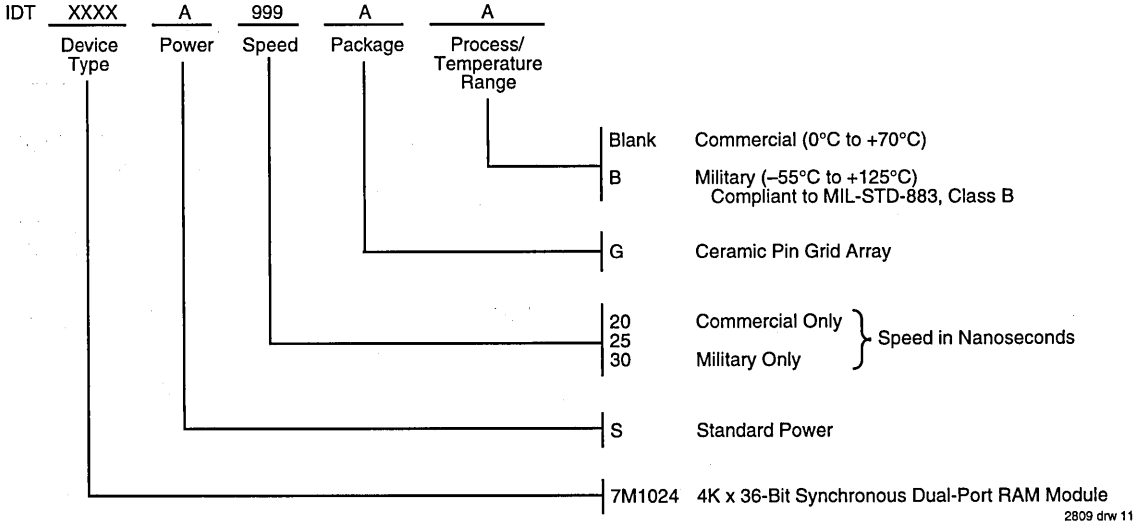
NOTES:
1. During dead cycle, if $\overline{CE}$ is LOW, data will be written into array.
2. $\overline{OE}$ LOW throughout.

PACKAGE DIMENSIONS



2809 drw 10

ORDERING INFORMATION



2809 drw 11

Integrated Device Technology, Inc.

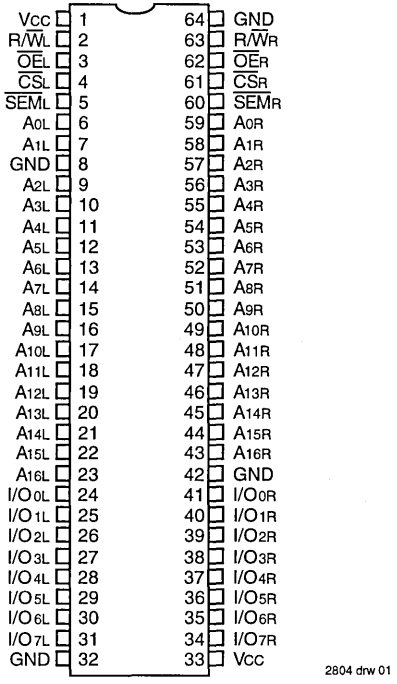
128K x 8
64K x 8
CMOS DUAL-PORT
STATIC RAM MODULE

IDT7M1001
IDT7M1003

FEATURES

- High-density 1M/512K CMOS Dual-Port Static RAM module
- Fast access times:
  —Commercial 35, 40ns
  —Military 40, 50ns
- Fully asynchronous read/write operation from either port
- Full on-chip hardware support of semaphore signaling between ports
- Surface mounted LCC (leadless chip carriers) components on a 64-pin sidebraze DIP (Dual In-line Package)
- Multiple Vcc and GND pins for maximum noise immunity
- Single 5V (±10%) power supply
- Input/outputs directly TTL-compatible

PIN CONFIGURATION[1]



2804 drw 01

DIP
TOP VIEW

NOTE:
1. For the IDT7M1003 (64K x 8) version, Pins 23 and 43 must be connected to GND for proper operation of the module.

DESCRIPTION:

The IDT7M1001/IDT7M1003 is a 128K x 8/64K x 8 high-speed CMOS Dual-Port Static RAM module constructed on a multilayer ceramic substrate using eight IDT7006 (16K x 8) Dual-Port RAMs and two IDT FCT138 decoders or depopulated using only four IDT7006s and two decoders.

This module provides two independent ports with separate control, address, and I/O pins that permit independent and asynchronous access for reads or writes to any location in memory. System performance is enhanced by facilitating port-to-port communication via semaphore ($\overline{SEM}$) "handshake" signaling. The IDT7M1001/1003 module is designed to be used as stand-alone Dual-Port RAM where on-chip hardware port arbitration is not needed. It is the users responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports.

The IDT7M1001/1003 module is packaged on a multilayer co-fired ceramic 64-pin DIP (Dual In-line Package) with dimensions of only 3.2" x 0.62" x 0.38". Maximum access times as fast as 35ns over the commercial temperature range are available.

All inputs and outputs of the IDT7M1001/1003 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation of the module.

All IDT military module semiconductor components are manufacured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

7

PIN NAMES

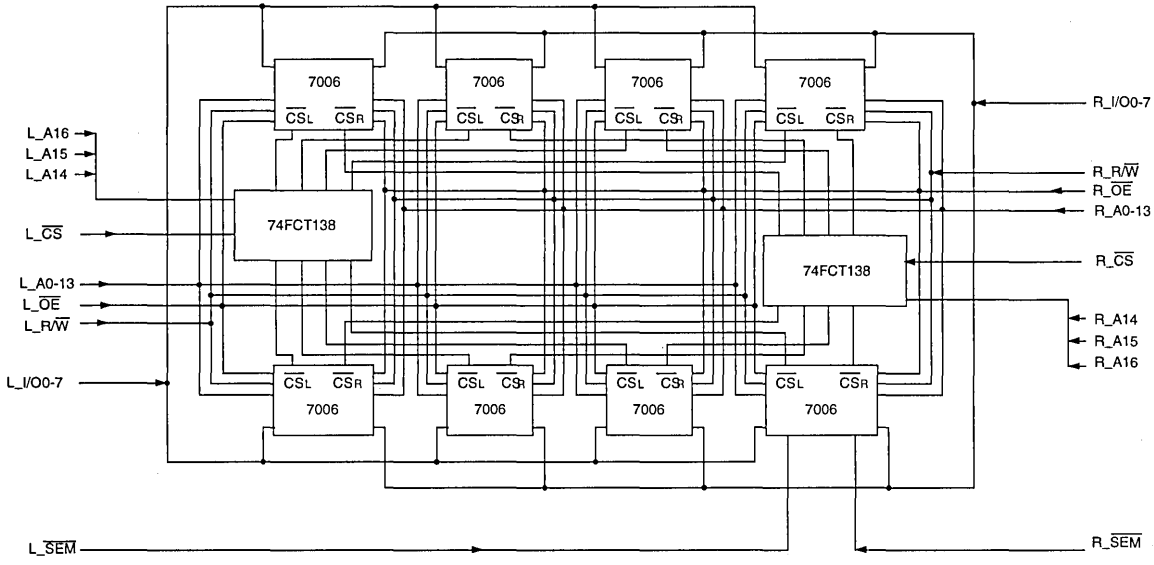
Left Port	Right Port	Description
A (0–16)L	A (0–16)R	Address Inputs
I/O (0–7)L	I/O (0–7)R	Data Inputs/Outputs
R/$\overline{W}$L	R/$\overline{W}$R	Read/Write Enables
$\overline{CS}$L	$\overline{CS}$R	Chip Select
$\overline{OE}$L	$\overline{OE}$R	Output Enable
$\overline{SEM}$L	$\overline{SEM}$R	Semaphore Control
VCC		Power
GND		Ground

2804 tbl 01

The IDT logo is a registered trademark of Integrated Device Technology, Inc.

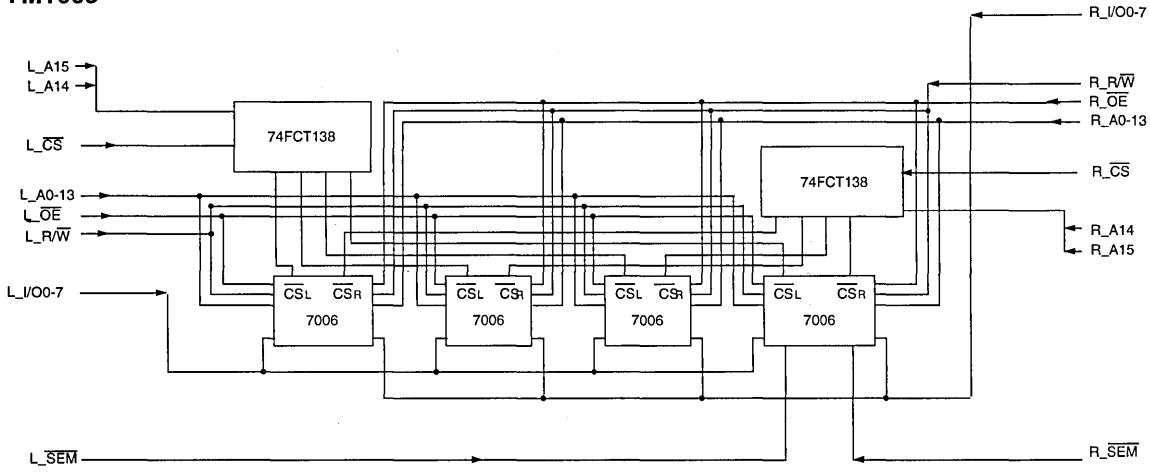
FUNCTIONAL BLOCK DIAGRAM

7M1001



2804 drw 02

7M1003



2804 drw 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2804 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Test Conditions	Max.	Unit
C_{IN1}	Input Capacitance ($\overline{CS}$ or $\overline{SEM}$)	V_{IN} = 0V	15	pF
C_{IN2}	Input Capacitance (Data, Address, All Other Controls)	V_{IN} = 0V	100	pF
C_{OUT}	Output Capacitance (Data)	V_{OUT} = 0V	100	pF

2804 tbl 03

NOTE:
1. This parameter is guaranteed by design but not tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2804 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	-	0.8	V

2804 tbl 05

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

(Vcc = 5V ± 10%, T_A = –55°C to +125°C or 0°C to +70°C)

Symbol	Parameter	Test Conditions	Commercial			Military			Unit
			Min.	Max.[1]	Max.[2]	Min.	Max.[1]	Max.[2]	
I_{CC2}	Dynamic Operating Current (Both Ports Active)	Vcc = Max., $\overline{CS} \le V_{IL}$, $\overline{SEM} \ge V_{IH}$ Outputs Open, f = f_{MAX}	—	940	660	—	1130	790	mA
I_{CC1}	Standby Supply Current (One Port Active)	Vcc = Max., L_$\overline{CS}$ or R_$\overline{CS} \ge V_{IH}$ Outputs Open, f = f_{MAX}	—	750	470	—	905	565	mA
I_{SB1}	Standby Supply Current (TTL Levels)	Vcc = Max., L_$\overline{CS}$ and R_$\overline{CS} \ge V_{IH}$ Outputs Open, f = f_{MAX} L_$\overline{SEM}$ and R_$\overline{SEM} \ge$ Vcc –0.2V	—	565	285	—	685	345	mA
I_{SB2}	Full Standby Supply Current (CMOS Levels)	L_$\overline{CS}$ and R_$\overline{CS} \ge$ Vcc –0.2V $V_{IN} >$ Vcc 0.2V or < 0.2V L_$\overline{SEM}$ and R_$\overline{SEM} \ge$ Vcc –0.2V	—	125	65	—	245	125	mA

2804 tbl 06

NOTES:
1. IDT7M1001 (128K x 8) version only.
2. IDT7M1003 (64K x 8) version only.

DC ELECTRICAL CHARACTERISTICS

(V_{CC}=5.0V ± 10%, T_A = −55°C to +125°C and 0°C to +70°C)

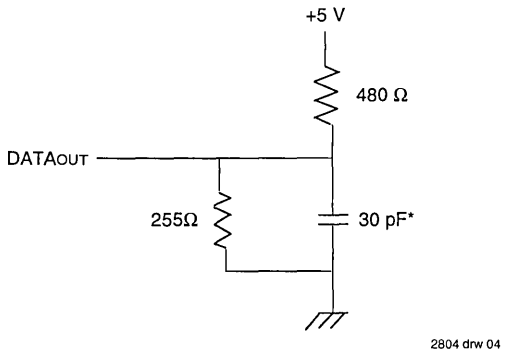
Symbol	Parameter	Test Conditions	IDT7M1001 Min.	IDT7M1001 Max.	IDT7M1003 Min.	IDT7M1003 Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address, Data & Other Controls)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	80	—	40	µA
$\|I_{LI}\|$	Input Leakage ($\overline{CS}$ and $\overline{SEM}$)	V_{CC} = Max. V_{IN} = GND to V_{CC}	—	10	—	10	µA
$\|I_{LO}\|$	Output Leakage (Data)	V_{CC} = Max. $\overline{CS} \geq V_{IH}$, V_{OUT} = GND to V_{CC}	—	80	—	40	µA
V_{OL}	Output Low Voltage	V_{CC} = Min. I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min. I_{OH} = −4mA	2.4	—	2.4	—	V

2804 tbl 07

AC TEST CONDITIONS

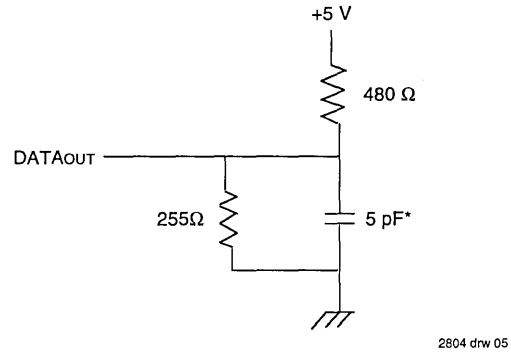
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2804 tbl 08



2804 drw 04

Figure 1. Output Load



2804 drw 05

Figure 2. Output Load
(for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{WHZ}, t_{OW})

*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C and 0°C to +70°C)

Symbol	Parameter	-35 Min.	-35 Max.	-40 Min.	-40 Max.	-50 Min.	-50 Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	35	—	40	—	50	—	ns
t_{AA}	Address Access Time	—	35	—	40	—	50	ns
t_{ACS}(2)	Chip Select Access Time	—	35	—	40	—	50	ns
t_{OE}	Output Enable Access Time	—	20	—	25	—	30	ns
t_{OH}	Output Hold From Address Change	3	—	3	—	3	—	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	3	—	3	—	3	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	—	20	—	20	—	25	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	3	—	3	—	3	—	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	20	—	20	—	25	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Disable to Power-Down Time	—	50	—	50	—	50	ns
t_{SOP}	$\overline{SEM}$ Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns
Write Cycle								
t_{WC}	Write Cycle Time	35	—	40	—	50	—	ns
t_{CW}(2)	Chip Select to End-of-Write	30	—	35	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	35	—	40	—	ns
t_{AS1}(3)	Address Set-up to Write Pulse Time	5	—	5	—	5	—	ns
t_{AS2}	Address Set-up to $\overline{CS}$ Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	30	—	35	—	40	—	ns
t_{WR}(4)	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	25	—	30	—	35	—	ns
t_{DH}(4)	Data Hold Time	0	—	0	—	0	—	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	20	—	20	—	25	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	—	20	—	20	—	25	ns
t_{OW}(1, 4)	Output Active from End-of-Write	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	15	—	15	—	15	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	15	—	15	—	15	—	ns
Port-to-Port Delay Timing								
t_{WDD}(5)	Write Pulse to Data Delay	—	60	—	65	—	70	ns
t_{DDD}(5)	Write Data Valid to Read Data Valid	—	45	—	50	—	55	ns

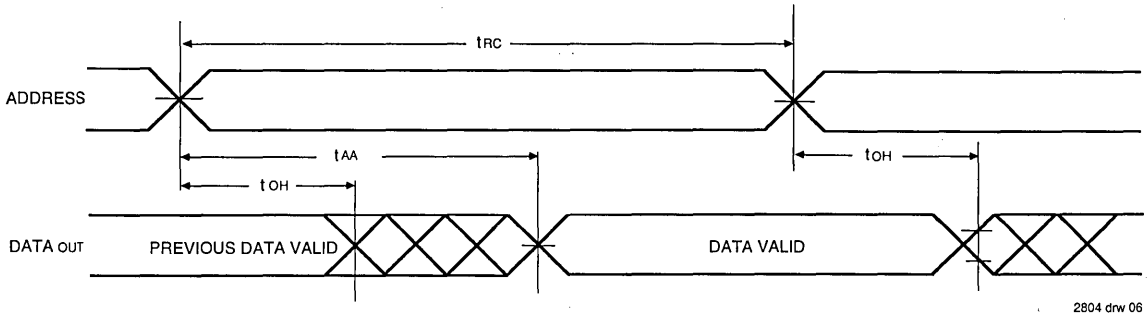
NOTES:

2804 tbl 09

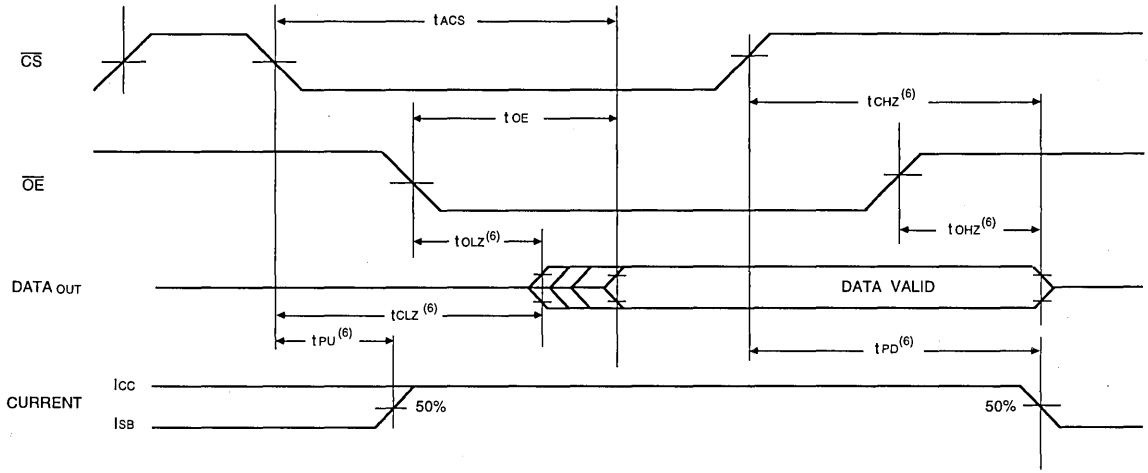
1. This parameter is guaranteed by design but not tested.
2. To access RAM $\overline{CS} \leq V_{IL}$ and $\overline{SEM} \geq V_{IH}$. To access semaphore, $\overline{CS} \geq V_{IH}$ and $\overline{SEM} \leq V_{IL}$.
3. t_{AS1}= 0 if R/$\overline{W}$ is asserted LOW simultaneously with or after the $\overline{CS}$ LOW transition.
4. For $\overline{CS}$ controlled write cycles, t_{WR}= 5ns, t_{DH}= 5ns, t_{OW}= 5ns.
5. Port-to-Port delay through the RAM cells from the writing port to the reading port.

7

TIMING WAVEFORM OF READ CYCLE NO. 1 (EITHER SIDE)[1,2,4]

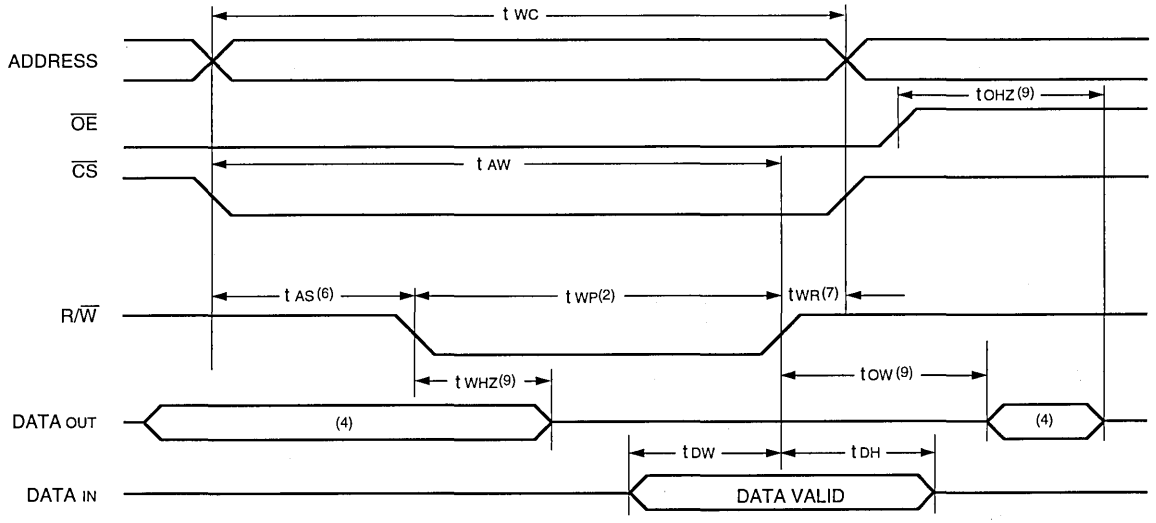


TIMING WAVEFORM OF READ CYCLE NO. 2 (EITHER SIDE)[1,3,5]



NOTES:
1. R/$\overline{W}$ is HIGH for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = LOW. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ = LOW.
5. To access RAM, $\overline{CS}$ = LOW, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = HIGH and $\overline{SEM}$ = LOW.
6. This parameter is guaranteed by design but not tested.

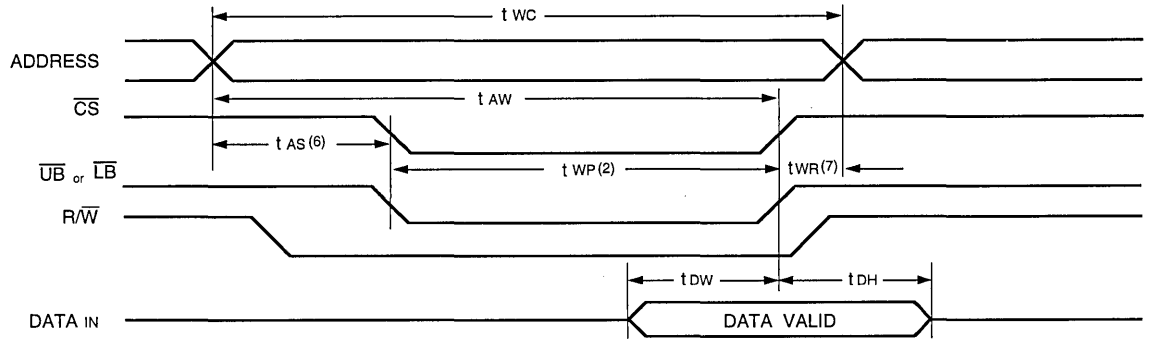
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (R/$\overline{W}$ CONTROLLED TIMING)(1,3,5,8)



2804 drw 08

NOTES:
1. R/$\overline{W}$ is HIGH for Read Cycles
2. Device is continuously enabled. $\overline{CS}$ = LOW. $\overline{UB}$ or $\overline{LB}$ = LOW. This waveform cannot be used for semaphore reads.
3. Addresses valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = LOW.
5. To access RAM, $\overline{CS}$ = LOW, $\overline{UB}$ or $\overline{LB}$ = LOW, $\overline{SEM}$ = H. To access semaphore, $\overline{CS}$ = HIGH and $\overline{SEM}$ = LOW.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be larger of twp or (twz + tdw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse width be as short as the specified twp.
9. This parameter is guaranteed by design but not tested.

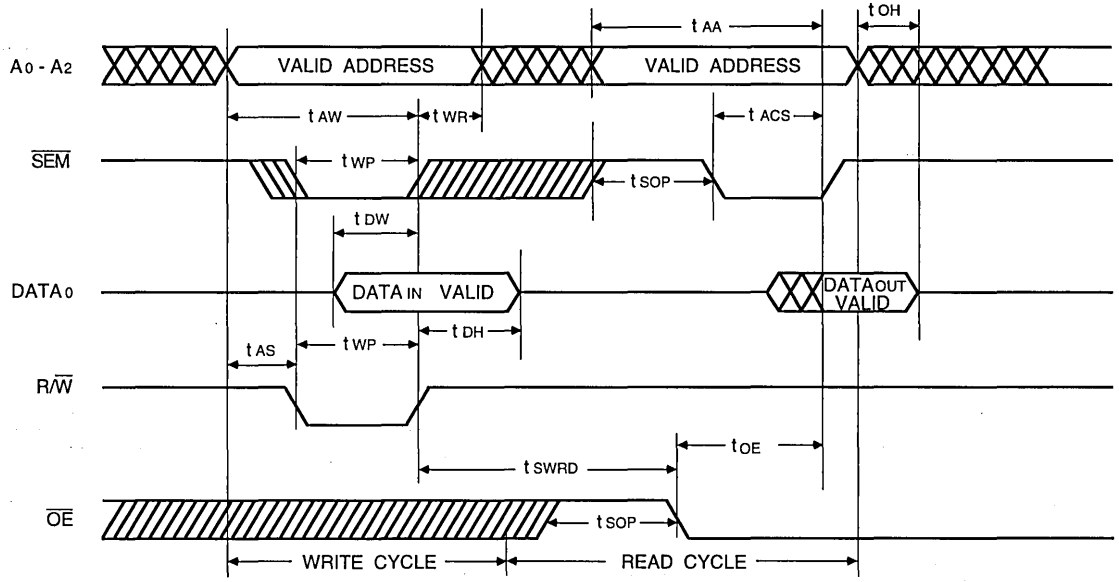
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,3,5,8)



2804 drw 09

NOTES:
1. R/$\overline{W}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (twp) of a LOW $\overline{UB}$ or $\overline{LB}$ and a LOW $\overline{CS}$ and a LOW R/$\overline{W}$ for memory array writing cycle.
3. twr is measured from the earlier of $\overline{CS}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CS}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.
6. Timing depends on which enable signal is asserted last.
7. Timing depends on which enable signal is de-asserted first.
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of twp or (twz + tdw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tdw. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.
9. This parameter is guaranteed by design but not tested.

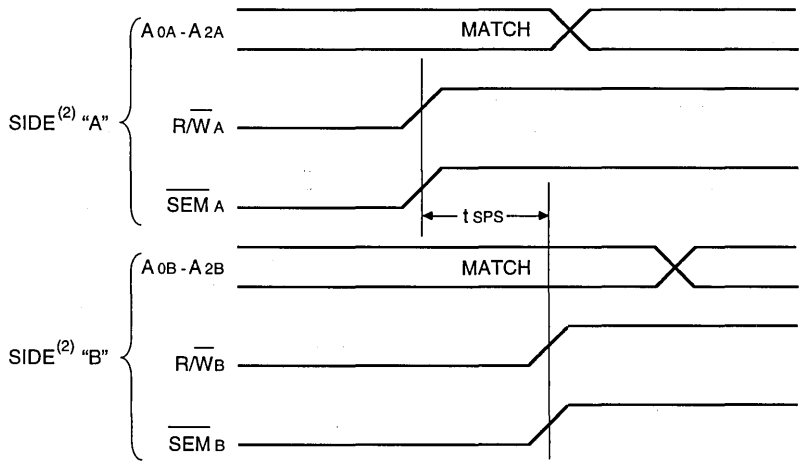
TIMING WAVEFORM OF SEMAPHORE READ AFTER WRITE TIMING (EITHER SIDE)[1]



2804 drw 10

NOTE:
1. $\overline{CS}$ = HIGH for the duration of the above timing (both write and read cycle).

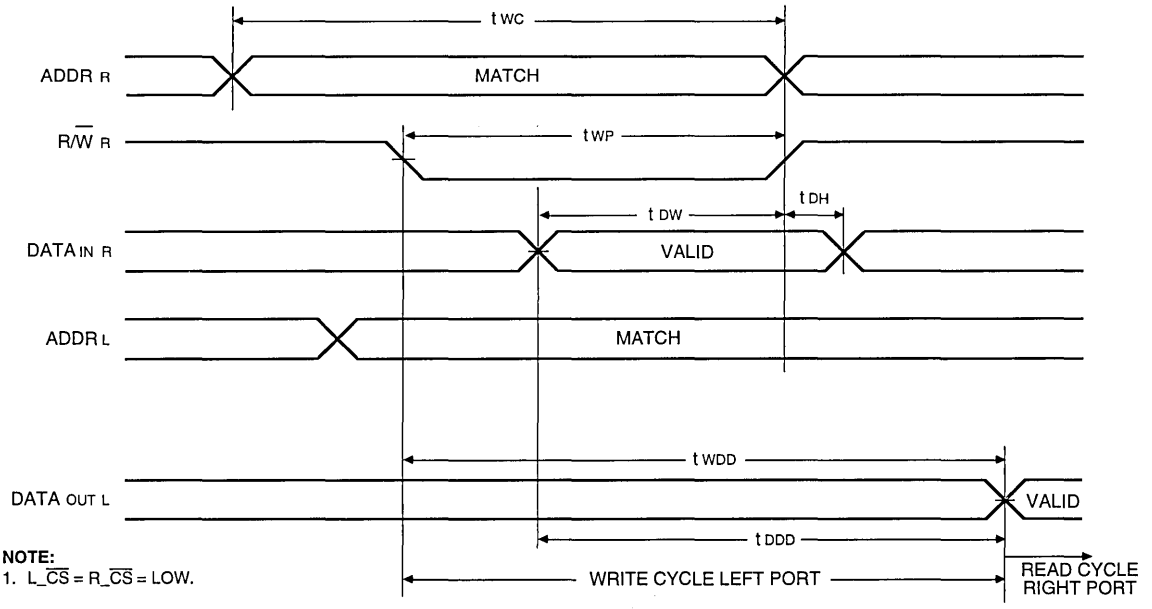
TIMING WAVEFORM OF SEMAPHORE CONTENTION[1,3,4]



2804 drw 11

NOTES:
1. $D_{0R} = D_{0L}$ = LOW, $L\_\overline{CS} = R\_\overline{CS}$ = HIGH. Semaphore Flag is released form both sides (reads as ones from both sides) at cycle start.
2. "A" may be either left or right port. "B" is the opposite port from "A".
3. This parameter is measured from $R/\overline{W}_A$ or $\overline{SEM}_A$ going HIGH to $R/\overline{W}_B$ or $\overline{SEM}_B$ going HIGH.
4. If t_{SPS} is violated, the semaphore will fall positively to one side or the other, but there is no guarantee which side will obtain the flag.

TIMING WAVEFORM OF WRITE WITH PORT-TO-PORT DELAY(1)



NOTE:
1. L_CS = R_CS = LOW.

2804 drw 12

TRUTH TABLES

TABLE I: NON-CONTENTION READ/WRITE CONTROL(1)

Inputs(1)				Outputs	
CS	R/W	OE	SEM	I/O0 - I/O7	Mode
H	X	X	H	High-Z	Deselected: Power Down
L	L	X	H	DATAIN	Write to Both Bytes
L	H	L	H	DATAOUT	Read Both Bytes
X	X	H	X	High-Z	Outputs Disabled

NOTE:
1. AOL — A12 ≠ AOR — A12R

2804 tbl 10

TABLE II: SEMAPHORE READ/WRITE CONTROL(1)

Inputs				Outputs	
CS	R/W	OE	SEM	I/O0 - I/O7	Mode
H	H	L	L	DATAOUT	Read Data in Semaphore Flag
X	↓	X	L	DATAIN	Write DIN0 into Semaphore Flag
L	X	X	L	—	Not Allowed

NOTE:
1. AOL — A12 ≠ AOR — A12R

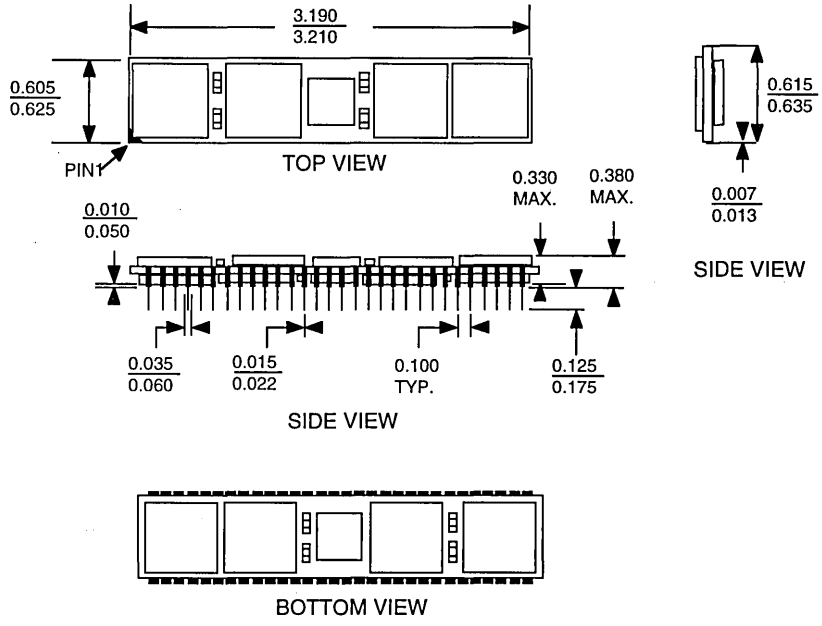
2804 tbl 11

SEMAPHORE OPERATION

For more details regarding semaphores & semaphore operations, please consult the IDT7006 datasheet.

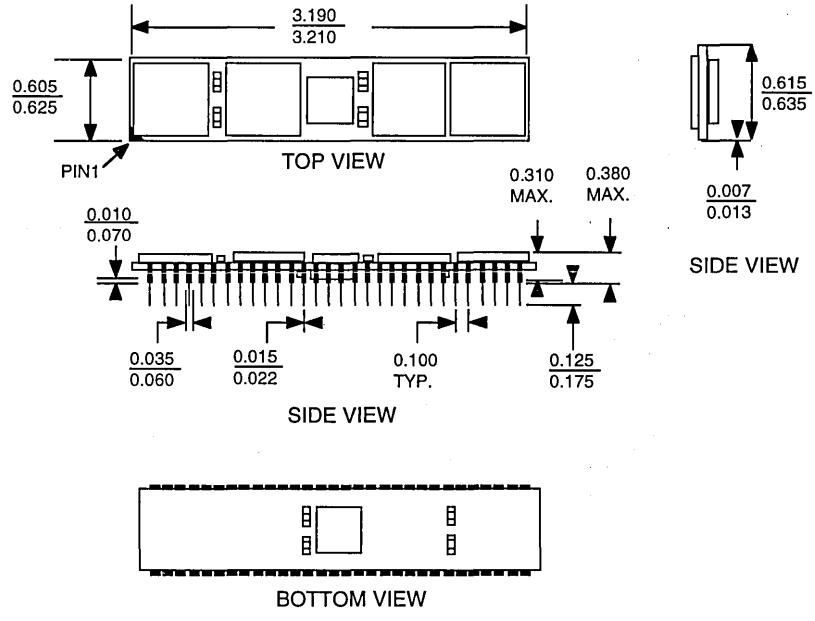
PACKAGE DIMENSIONS

7M1001



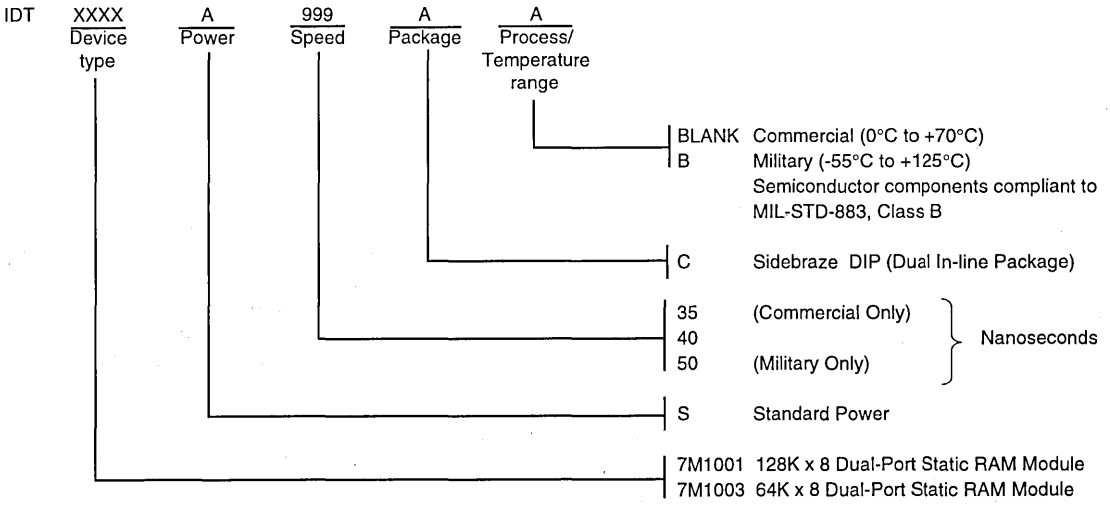
2804 drw 13

7M1003



2804 drw 14

ORDERING INFORMATION



2804 drw 15

7

Integrated Device Technology, Inc.

64K x 9/128K x 9 CMOS PARALLEL IN-OUT FIFO MODULE

PRELIMINARY
IDT7M208
IDT7M209

FEATURES:

- First-In/First-Out memory module
- 64K x 9 (IDT7M208) or 128K x 9 (IDT7M209)
- High speed: 20ns (max.) access time
- Asynchronous and simultaneous read and write
- Fully expandable: depth and/or width
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning-flags
- Single 5V (±10%) power supply

DESCRIPTION:

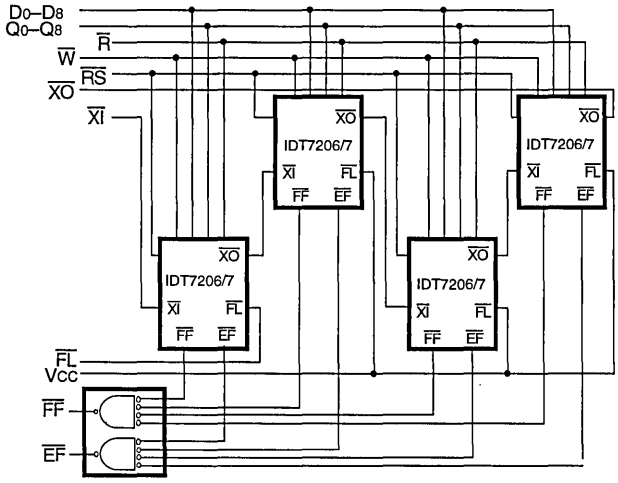
IDT7M208 and IDT7M209 are FIFO memory modules constructed on a multi-layered ceramic substrate using four IDT7206 (16K x 9) or IDT7207 (32K x 9) FIFOs in leadless chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7206/7s fabricated in IDT's high performance CMOS technology. These devices utilize an algorithm that loads and empties data on a first-in/first-out basis. The device uses Full and Empty flags as warnings for data overflow and underflow conditions and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins. The devices have a read/write cycle time of 20ns (min.) for commercial and 30ns (min.) for military temperature ranges.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

IDT's Military FIFO modules have semiconductor components manufactued in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

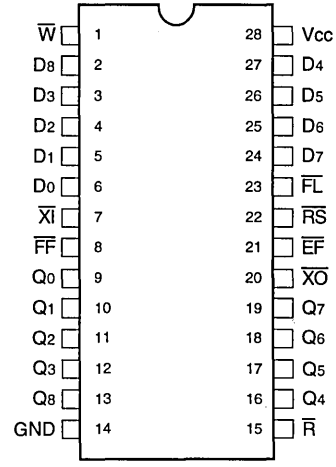
FUNCTIONAL BLOCK DIAGRAM



DUAL 4-INPUT OR GATE

3162 drw 01

PIN CONFIGURATION



DIP
TOP VIEW

3162 drw 02

PIN NAMES

$\overline{W}$ = WRITE	$\overline{FL}$ = FIRST LOAD	$\overline{XI}$ = EXPANSION IN	$\overline{EF}$ = EMPTY FLAG
$\overline{R}$ = READ	D = DATAIN	$\overline{XO}$ = EXPANSION OUT	V_{CC} = 5V
$\overline{RS}$ = RESET	Q = DATAOUT	$\overline{FF}$ = FULL FLAG	GND = GROUND

3162 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	–55 to +125	°C
TBIAS	Temperature Under Bias	–55 to +125	–65 to +135	°C
TSTG	Storage Temperature	–55 to +125	–65 to +150	°C
IOUT	DC Output Current	50	50	mA

NOTE: 3162 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
CIN	Input Capacitance	VIN = 0V	50	pF
COUT	Output Capacitance	VOUT = 0V	50	pF

NOTE: 3162 tbl 03

1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCM	Military Supply Voltage	4.5	5.0	5.5	V
VCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH(1)	Input High Voltage Commercial	2.0	—	—	V
VIH(1)	Input High Voltage Military	2.2	—	—	V
VIL(2)	Input Low Voltage Commercial and Military	—	—	0.8	V

NOTES: 3162 tbl 04

1. VIH = 2.6V for $\overline{XI}$ input (commercial)
   VIH = 2.8V for $\overline{XI}$ input (military)
2. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V±10%, TA = 0°C to +70°C; and –55°C to +125°C)

Symbol	Parameter	Commercial Min.	Commercial Max.	Military Min.	Military Max.	Unit
ILI(1)	Input Leakage Current (Any Input)	–5	5	-40	40	µA
ILO(2)	Output Leakage Current	–40	40	-40	40	µA
VOH	Output Logic "1" Voltage IOUT = –2mA	2.4	—	2.4	—	V
VOL	Output Logic "0" Voltage IOUT = 8mA	—	0.4	—	0.4	V
ICC1(3)	Vcc Power Supply Current	—	560	—	720	mA
ICC2(3)	Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/$\overline{RT}$ = VIH)	—	60	—	80	mA
ICC3(3)	Power Down Current (All Input = Vcc – 0.2V)	—	32	—	48	mA

NOTES: 3162 tbl 05

1. Measurements with 0.4 ≤ VIN ≤ Vcc.
2. R ≥ VIH, 0.4 ≤ VOUT ≤ Vcc.
3. Icc measurements are made with outputs open.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1 and 2

3162 tbl 06

7

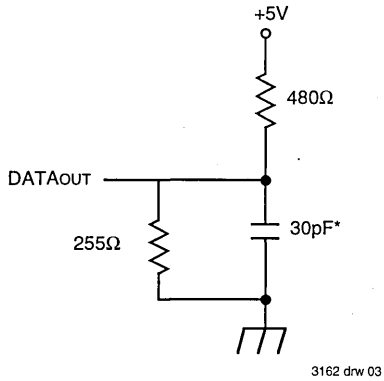


Figure 1. Output Load
*** Includes scope and jig capacitances.**

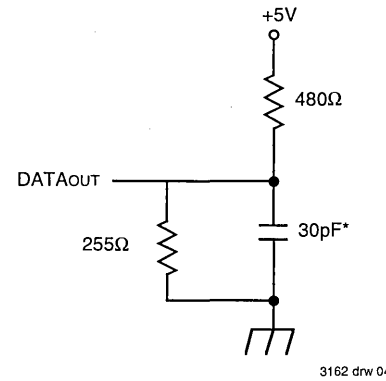


Figure 2. Output Load
(for tRLZ, tWLZ, and tRHZ)

* Includes scope and jig capacitances.

AC ELECTRICAL CHARACTERISTICS

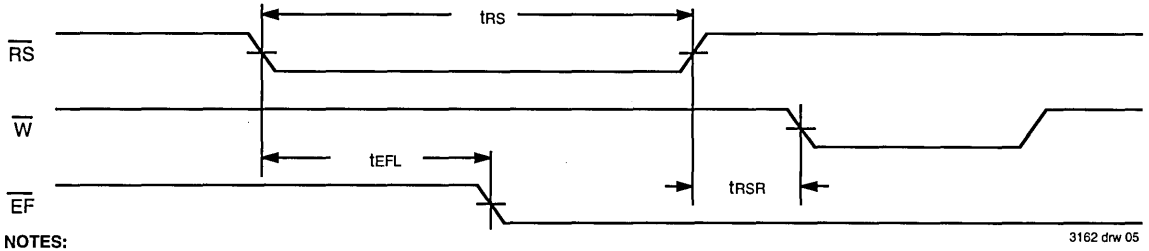
(V_{CC} = 5.0V±10%, T_A = 0°C to +70°C and –55°C to +125°C)

Symbol	Parameter	–20 (Com'l Only)		–25 (Com'l Only)		–30 (Mil Only)		–35 (Mil Only)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
fS	Shift Frequency	—	33.3	—	28.6	—	25	—	22.5	MHz
tRC	Read Cycle Time	30	—	35	—	40	—	45	—	ns
tA	Access Time	—	20	—	25	—	30	—	35	ns
tRR	Read Recovery Time	10	—	10	—	10	—	10	—	ns
tRPW(1)	Read Pulse Width	20	—	25	—	30	—	35	—	ns
tRLZ(2)	Read Pulse Low to Data Bus at Low Z	5	—	5	—	5	—	5	—	ns
tWLZ(2)	Write Pulse High to Data Bus at Low Z	5	—	5	—	5	—	10	—	ns
tDV	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
tRHZ(2)	Read Pulse High to Data Bus at High Z	—	16	—	20	—	20	—	20	ns
tWC	Write Cycle Time	30	—	35	—	40	—	45	—	ns
tWPW(1)	Write Pulse Width	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	10	—	10	—	10	—	10	—	ns
tDS	Data Set-up Time	15	—	18	—	18	—	20	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	ns
tRSC	Reset Cycle Time	30	—	35	—	40	—	45	—	ns
tRS(1)	Reset Pulse Width	20	—	25	—	30	—	35	—	ns
tRSR	Reset Recovery Time	10	—	10	—	10	—	10	—	ns
tEFL	Reset to Emtpy Flag Low	—	30	—	35	—	40	—	45	ns
tREF	Read Low to Emtpy Flag Low	—	23	—	25	—	30	—	35	ns
tRFF	Read High to Full Flag High	—	23	—	25	—	30	—	35	ns
tWEF	Write High to Empty Flag High	—	23	—	25	—	30	—	35	ns
tWFF	Write Low to Full Flag Low	—	23	—	25	—	30	—	35	ns

3162 tbl 06

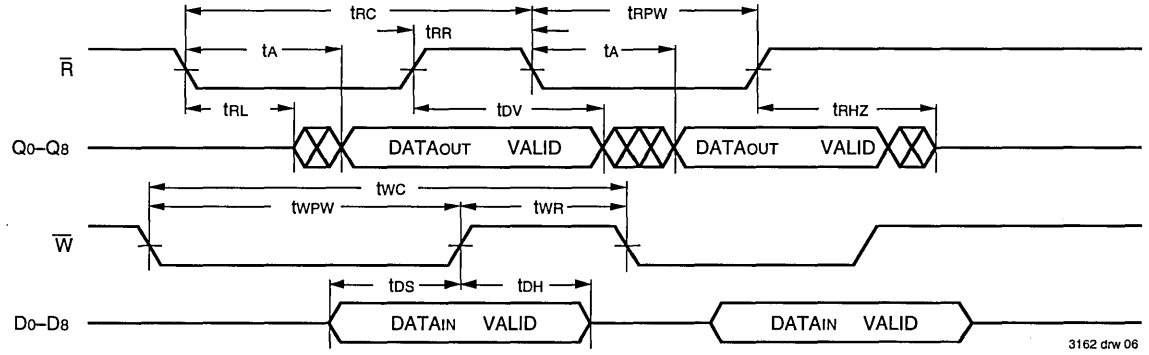
NOTES:
1. Pulse widths less than minimum value are not allowed.
2. Values guaranteed by design, not currently tested.

TIMING WAVEFORM OF RESET CYCLE[1,2]



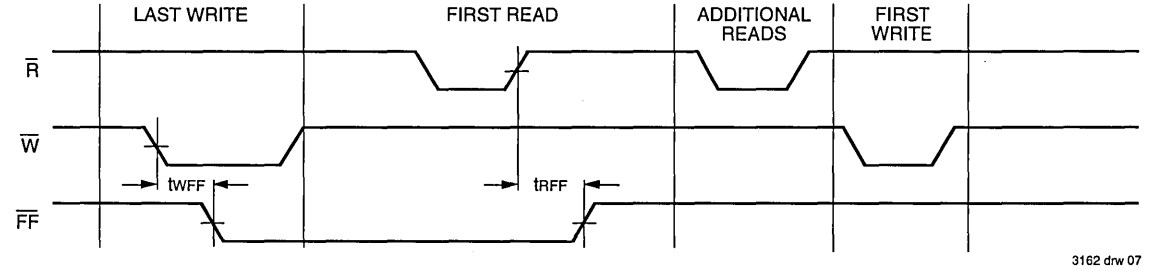
NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

TIMING WAVEFORM OF ASYNCHRONOUS WRITE AND READ OPERATION

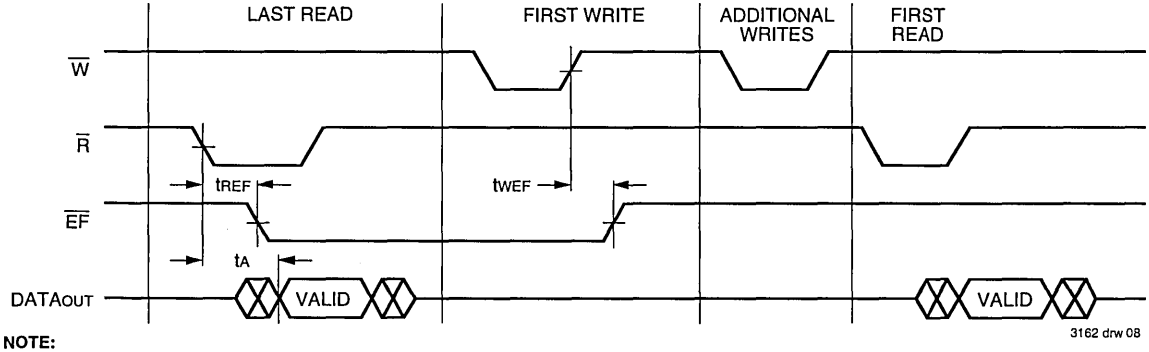


:

TIMING WAVEFORM FOR THE FULL FLAG FROM LAST WRITE TO FIRST READ

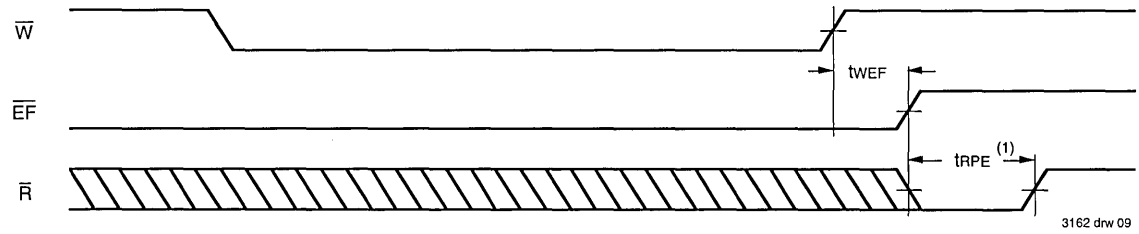


TIMING WAVEFORM FOR THE EMPTY FLAG FROM LAST READ TO FIRST WRITE



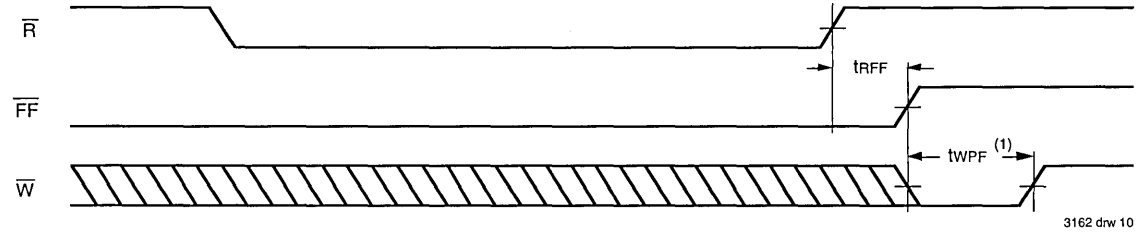
NOTE:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM FOR THE EMPTY FLAG CYCLE



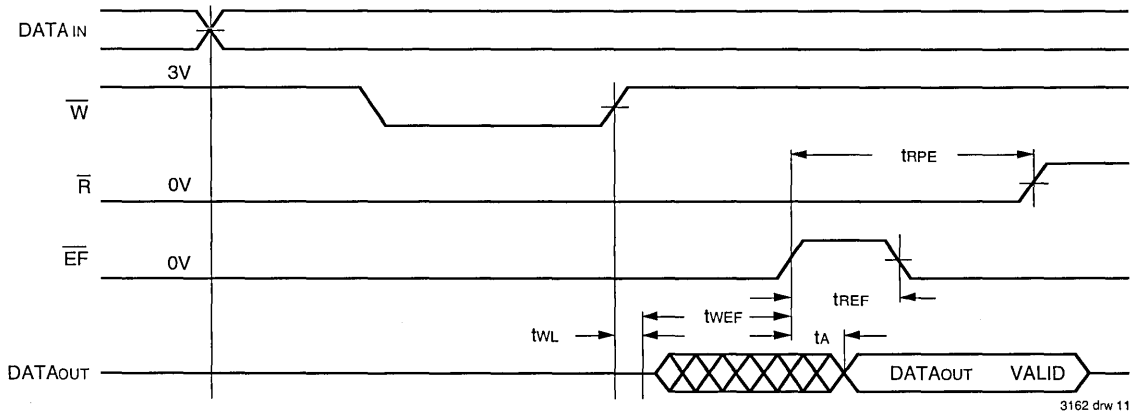
NOTE:
1. t_{RPE} must be ≥ $t_{RPW\ (min)}$. Refer to Technical Note TN-08 for details on this boundary condition.

TIMING WAVEFORM FOR THE FULL FLAG CYCLE

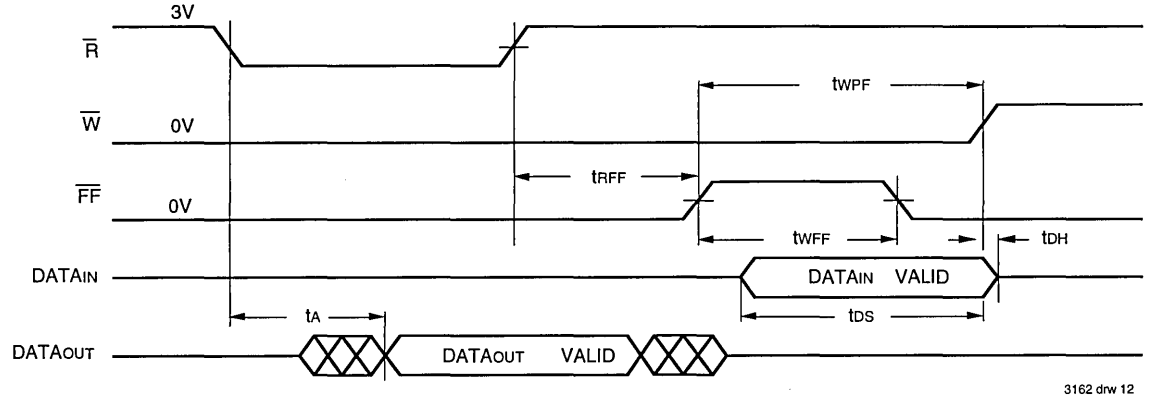


NOTE:
1. t_{WPF} must be ≥ $t_{WPW\ (min)}$. Refer to Technical Note TN-08 for details on this boundary condition.

TIMING WAVEFORM OF READ DATA FLOW-THROUGH MODE



TIMING WAVEFORM OF WRITE DATA FLOW-THROUGH MODE



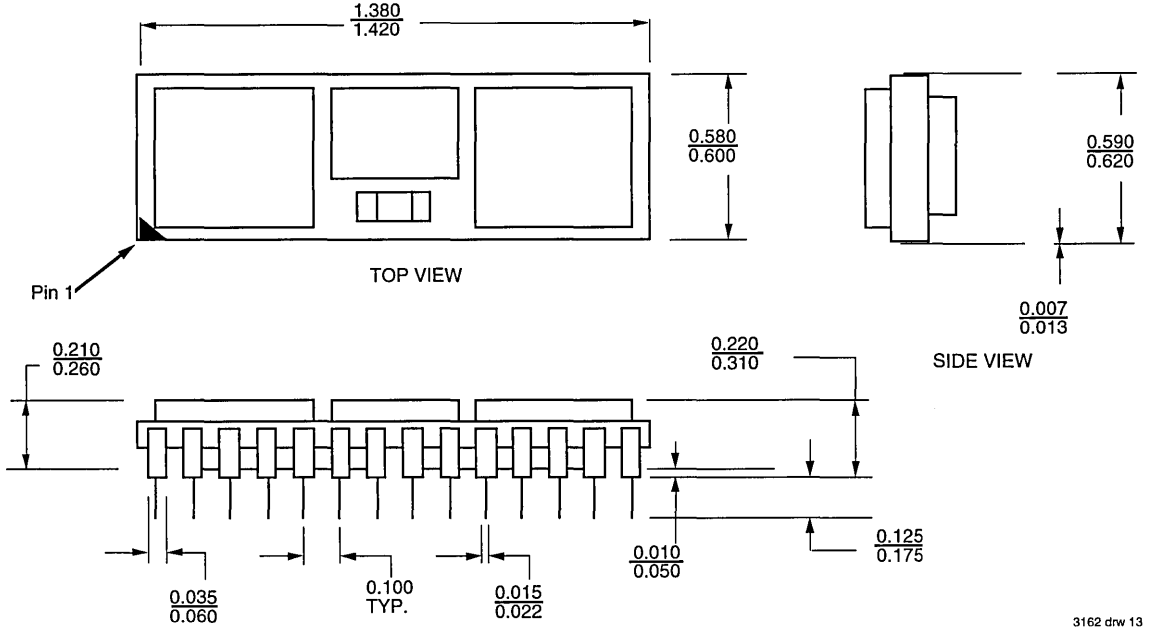
3162 drw 12

DEPTH/WIDTH EXPANSION & DATA FLOW-THROUGH MODES:

For more details on expanding FIFO modules in depth and/or width, please refer to the IDT7206 or IDT7207 data sheets.

For more details on data flow-through modes (read data fall through and write data fall-through), please refer to the IDT7206 or IDT7207 data sheets.

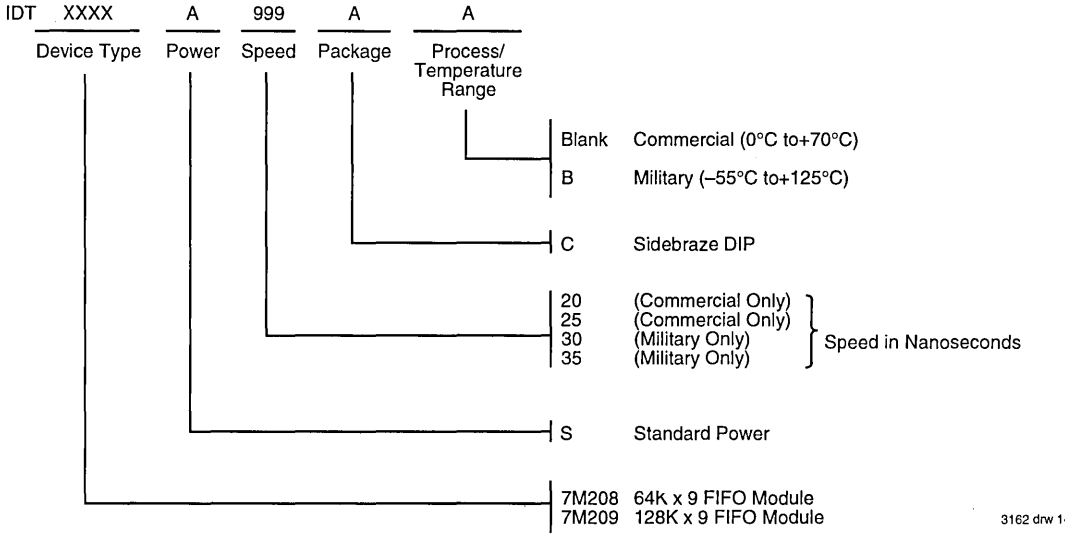
PACKAGE DIMENSIONS



3162 drw 13

7

ORDERING INFORMATION



3162 drw 14

Integrated Device Technology, Inc.

1M x 32 CMOS STATIC RAM MODULE

IDT7MP4120

FEATURES

- High-density 4MB Static RAM module
- Low profile 72-pin ZIP (Zig-zag In-line vertical Package) or 72-pin SIMM (Single In-line Memory Module)
- Fast access time: 20ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

PIN CONFIGURATION[1]

NC	2	1	NC	PD_0 - GND
PD_3	4	3	PD_2	PD_1 - NC
PD_0	6	5	GND	PD_2 - GND
I/O_0	8	7	PD_1	PD_3 - NC
I/O_1	10	9	I/O_8	
I/O_2	12	11	I/O_9	
I/O_3	14	13	I/O_{10}	
V_{CC}	16	15	I/O_{11}	
A_7	18	17	A_0	
A_8	20	19	A_1	
A_9	22	21	A_2	
I/O_4	24	23	I/O_{12}	
I/O_5	26	25	I/O_{13}	
I/O_6	28	27	I/O_{14}	
I/O_7	30	29	I/O_{15}	
$\overline{WE}$	32	31	GND	
A_{14}	34	33	A_{15}	
$\overline{CS_1}$	36	35	$\overline{CS_2}$	
$\overline{CS_3}$	38	37	$\overline{CS_4}$	
A_{16}	40	39	A_{17}	
GND	42	41	$\overline{OE}$	
I/O_{16}	44	43	I/O_{24}	
I/O_{17}	46	45	I/O_{25}	
I/O_{18}	48	47	I/O_{26}	
I/O_{19}	50	49	I/O_{27}	
A_{10}	52	51	A_3	
A_{11}	54	53	A_4	
A_{12}	56	55	A_5	
A_{13}	58	57	V_{CC}	
I/O_{20}	60	59	A_6	
I/O_{21}	62	61	I/O_{28}	
I/O_{22}	64	63	I/O_{29}	
I/O_{23}	66	65	I/O_{30}	
GND	68	67	I/O_{31}	
A_{19}	70	69	A_{18}	
NC	72	71	NC	

3019 drw 01

ZIP, SIMM
TOP VIEW

NOTE:

1. Pins 3, 4, 6 and 7 (PD_0, PD_1, PD_2 and PD_3 respectively) are read by the user to determine the density of the module. If PD_0 reads GND, PD_1 reads NC, PD_2 reads GND and PD_3 reads NC, then the module has a 1M depth.

DESCRIPTION

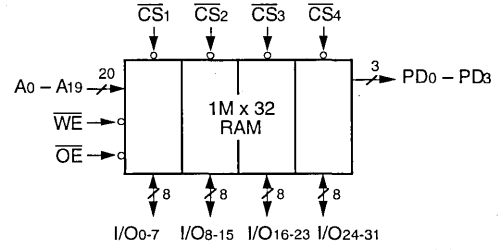
The IDT7MP4120 is a 1M x 32 Static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 1M x 4 Static RAMs in plastic packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. The IDT7MP4120 is available with access time as fast as 20ns with minimal power consumption.

The IDT7MP4120 is packaged in a 72-pin FR-4 ZIP (Zig-zag In-line vertical Package)or a 72-pin SIMM (Single In-line Memory Module). The ZIP configuration allows 72 pins to be placed on a package 4.05" long and 0.365" wide. At only 0.60" high, this low-profile package is ideal for systems with minimum board spacing while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4120 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Four identification pins (PD_0, PD_1, PD_2 and PD_3) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD_0, PD_1, PD_2 and PD_3 to determine a 1M depth.

FUNCTIONAL BLOCK DIAGRAM



3019 drw 02

PIN NAMES

I/O_0–I/O_{31}	Data Inputs/Outputs
A_0–A_{19}	Addresses
$\overline{CS_1}$-$\overline{CS_4}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD_0–PD_3	Depth Identification
V_{CC}	Power
GND	Ground
NC	No Connect

3019 tbl 01

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{I/O}$	Data I/O Capacitance	$V_{(IN)}$ = 0V	15	pF
C_{IN1}	Input Capacitance (Address)	$V_{(IN)}$ = 0V	60	pF
C_{IN2}	Input Capacitance ($\overline{WE}$, $\overline{OE}$)	$V_{(IN)}$ = 0V	75	pF
C_{IN3}	Input Capacitance ($\overline{CS}$)	$V_{(IN)}$ = 0V	20	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

3019 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE:
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.

3019 tbl 03

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

3019 tbl 04

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

3019 tbl 05

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3019 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output LOW	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output HIGH	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

3019 tbl 07

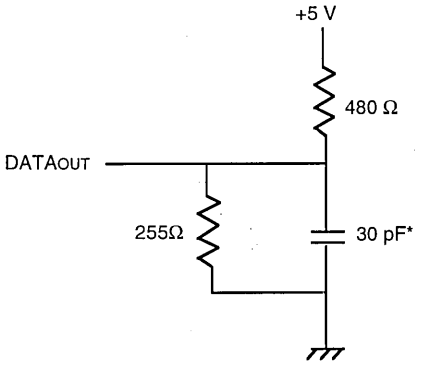
Symbol	Parameter	Test Conditions	7MP4120 Max.	Unit
I_{CC}	Dynamic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	1280	mA
I_{SB}	Standby Supply Current	$\overline{CS} \geq V_{IH}$, V_{CC} = Max. Outputs Open, f = f_{MAX}	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS} \geq V_{CC}$ – 0.2V; f = 0 $V_{IN} > V_{CC}$ – 0.2V or < 0.2V	120	mA

3019 tbl 08

AC TEST CONDITIONS

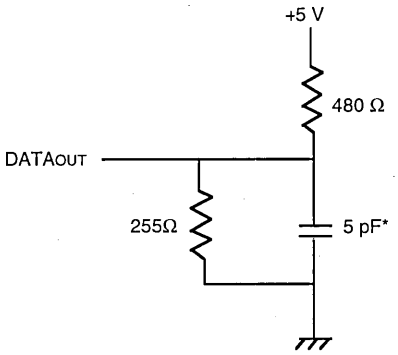
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2769 tbl 09



3019 drw 03

Figure 1. Output Load



3019 drw 04

Figure 2. Output Load
(for t_{OLZ},t_{OHZ}, t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW})

*Includes scope and jig.

7

AC ELECTRICAL CHARACTERISTICS

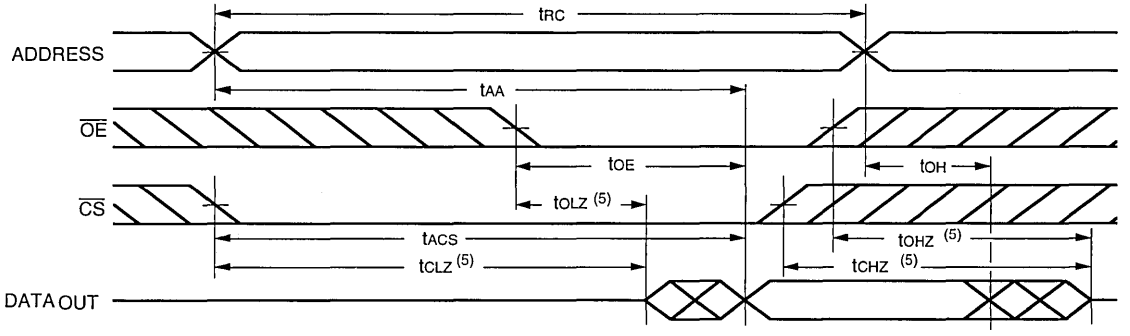
(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP4120SxxZ/M				Unit
		-20		-25		
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	20	—	25	—	ns
t_{AA}	Address Access Time	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	20	—	25	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High-Z	—	10	—	12	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	—	10	—	12	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	20	—	25	ns
Write Cycle						
t_{WC}	Write Cycle Time	20	—	25	—	ns
t_{CW}	Chip Select to End-of-Write	17	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	17	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	ns
t_{WR}	Write Recovery Time	3	—	3	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	—	10	—	15	ns
t_{DW}	Data to Write Time Overlap	12	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	ns
t_{OW}[1]	Output Active from End-of-Write	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

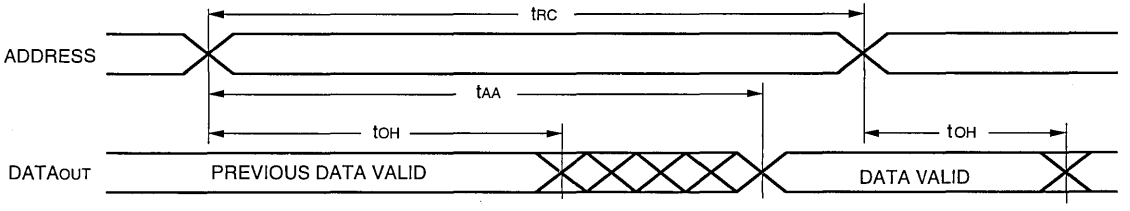
3019 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1[1]



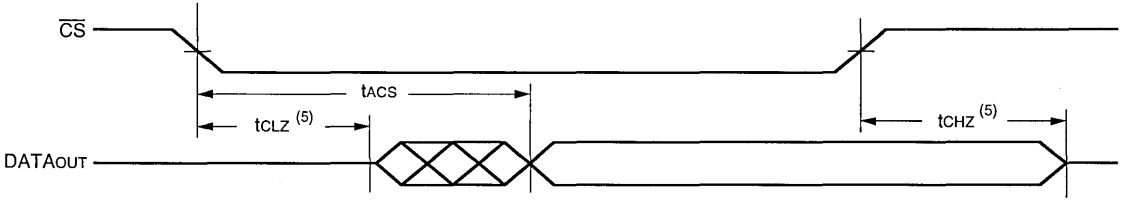
3019 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2[1,2,4]



3019 drw 06

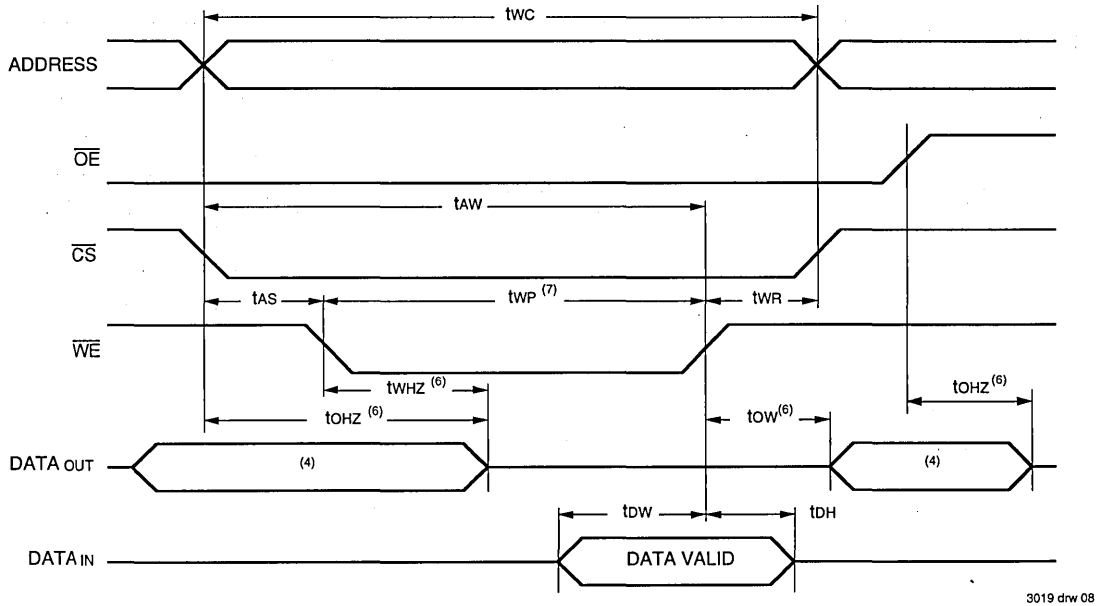
TIMING WAVEFORM OF READ CYCLE NO. 3[1,3,4]



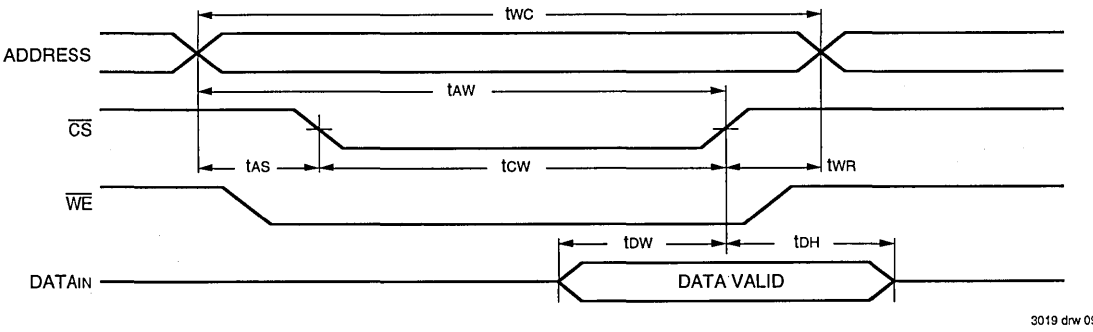
3019 drw 07

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (1, 2, 3, 7)



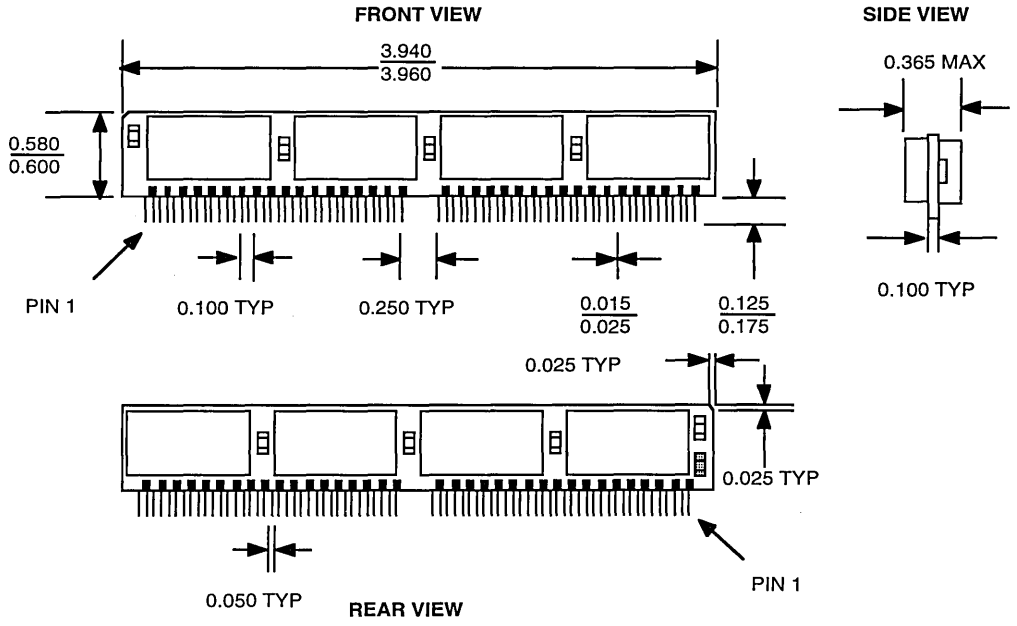
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

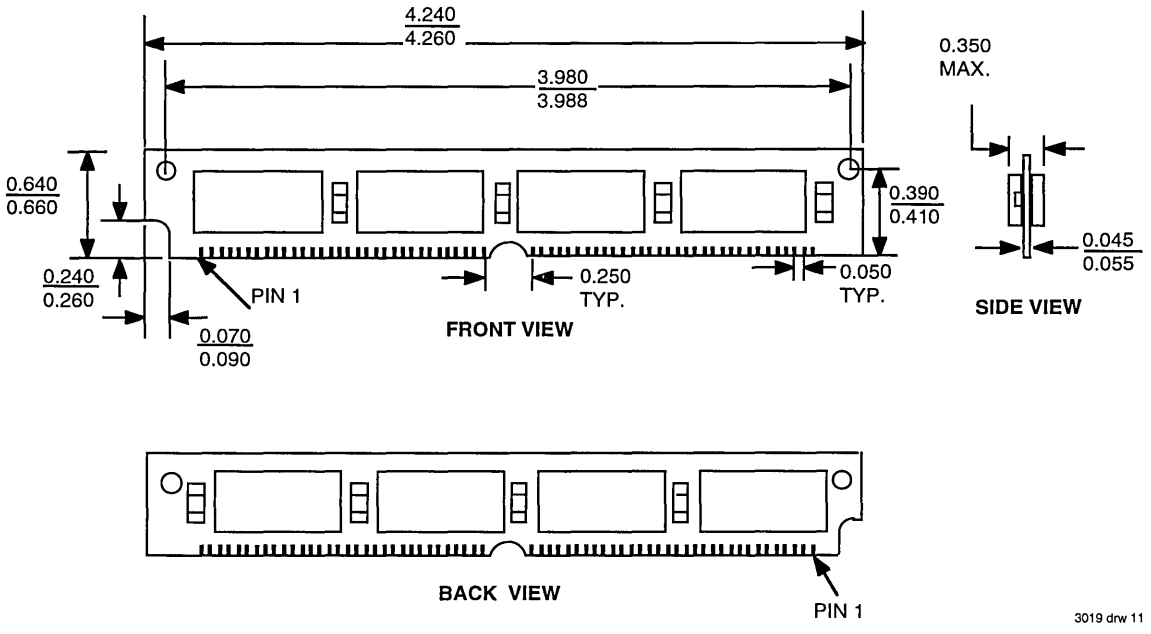
PACKAGE DIMENSIONS

ZIP VERSION



3019 drw 10

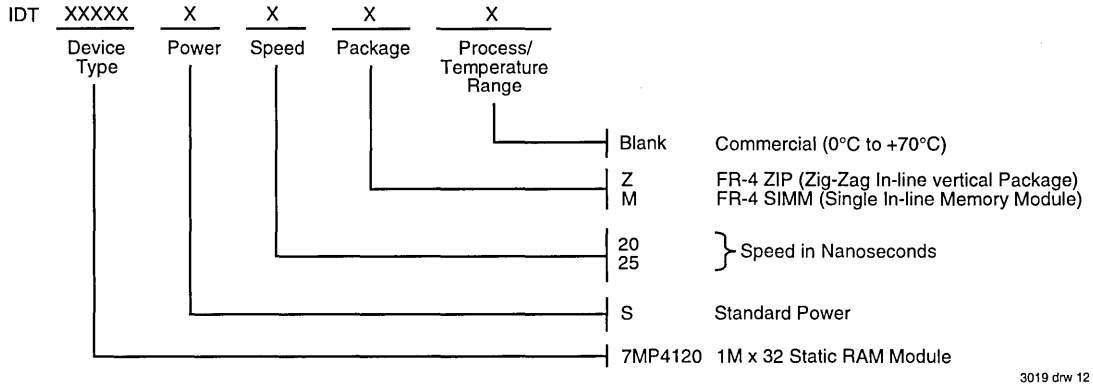
SIMM VERSION



3019 drw 11

7

ORDERING INFORMATION



3019 drw 12

Integrated Device Technology, Inc.

256K x 32 CMOS STATIC RAM MODULE

IDT7MP4145

FEATURES:

- High density 1 megabyte static RAM module (upgradeable to 4 megabyte, IDT7MP4120)
- Low profile 72 lead SIMM (Single In-line Memory Module)
- Very fast access time: 15ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

PIN CONFIGURATION[1]

NC	2	1	NC	PD0 - GND
PD3	4	3	PD2	PD1 - GND
PD0	6	5	GND	PD2 - OPEN
I/O0	8	7	PD1	PD3 - OPEN
I/O1	10	9	I/O8	
I/O2	12	11	I/O9	
I/O3	14	13	I/O10	
VCC	16	15	I/O11	
A7	18	17	A0	
A8	20	19	A1	
A9	22	21	A2	
I/O4	24	23	I/O12	
I/O5	26	25	I/O13	
I/O6	28	27	I/O14	
I/O7	30	29	I/O15	
$\overline{WE}$	32	31	GND	
A14	34	33	A15	
$\overline{CS_1}$	36	35	$\overline{CS_2}$	
$\overline{CS_3}$	38	37	$\overline{CS_4}$	
A16	40	39	A17	
GND	42	41	$\overline{OE}$	
I/O16	44	43	I/O24	
I/O17	46	45	I/O25	
I/O18	48	47	I/O26	
I/O19	50	49	I/O27	
A10	52	51	A3	
A11	54	53	A4	
A12	56	55	A5	
A13	58	57	VCC	
I/O20	60	59	A6	
I/O21	62	61	I/O28	
I/O22	64	63	I/O29	
I/O23	66	65	I/O30	
GND	68	67	I/O31	
NC	70	69	NC	
NC	72	71	NC	

3148 drw 01

SIMM
TOP VIEW

NOTE:

1. Pins 3, 4, 6 and 7 (PD_{0-3}) are read by the user to determine the density of the module. If PD_0, PD_1 read GND and PD_2, PD_3 read OPEN, then the module had a 256K depth.

DESCRIPTION:

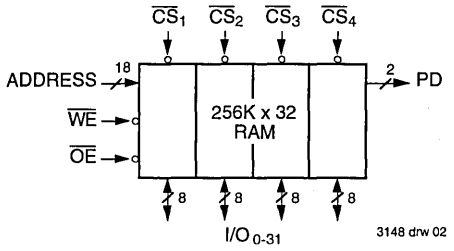
The IDT7MP4145 is a 256K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. The IDT7MP4145 is available with access time as fast as 15ns with minimal power consumption.

The IDT7MP4145 is packaged in a 72 lead SIMM (Single In-line Memory Module). The SIMM configuration allows 72 leads to be placed on a package 4.25 inches long and 0.365 inches wide. At only 0.65 inches high, this low profile package is ideal for systems with minimum board spacing; using angled SIMM sockets can reduce the effective module height even further.

All inputs and outputs of the IDT7MP4145 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Four identification pins (PD_{0-3}) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD_{0-3} to determine a 256K depth.

FUNCTIONAL BLOCK DIAGRAM



3148 drw 02

PIN NAMES

I/O_{0-31}	Data Inputs/Outputs
A_{0-17}	Addresses
$\overline{CS}_{1-4}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD_{0-1}	Depth Identification
VCC	Power
GND	Ground
NC	No Connect

3148 tbl 01

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance ($\overline{CS}$)	$V_{(IN)}$ = 0V	20	pF
$C_{IN(A)}$	Input Capacitance (Address & Control)	$V_{(IN)}$ = 0V	70	pF
$C_{I/O}$	I/O Capacitance	$V_{(OUT)}$ = 0V	12	pF

NOTE:
1. This parameter is guaranteed by design but not tested.

3148 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE:
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.

3148 tbl 03

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

3148 tbl 04

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

3148 tbl 05

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3148 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

3148 tbl 07

Symbol	Parameter	Test Conditions	Max.	Unit
I_{CC}	Dynamic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	1360	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	120	mA

3148 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

3148 tbl 09

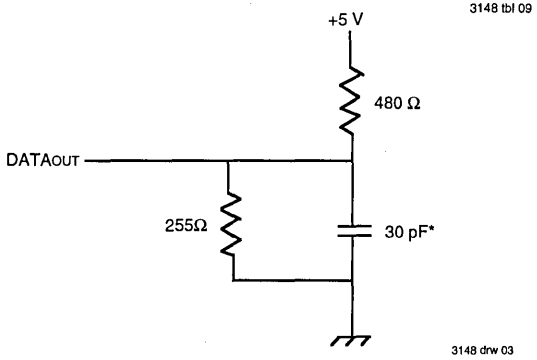


Figure 1. Output Load

*Includes scope and jig capacitances.

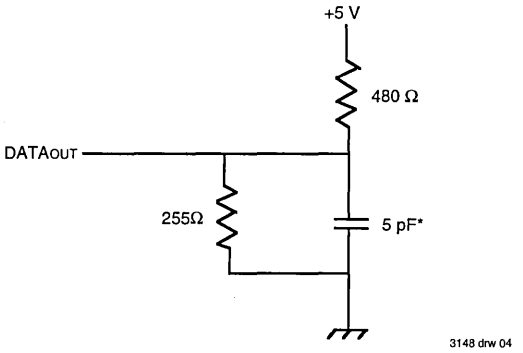


Figure 2. Output Load
(for tOLZ,tOHZ, tCHZ, tCLZ, tWHZ, tOW)

AC ELECTRICAL CHARACTERISTICS

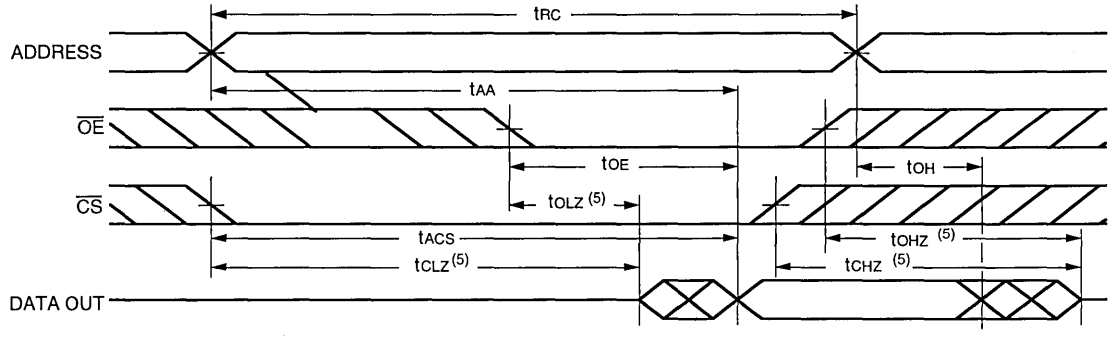
(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	-15 Min.	-15 Max.	-20 Min.	-20 Max.	-25 Min.	-25 Max.	Unit
Read Cycle								
tRC	Read Cycle Time	15	—	20	—	25	—	ns
tAA	Address Access Time	—	15	—	20	—	25	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	ns
tCLZ(1)	Chip Select to Output in Low-Z	3	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	8	—	10	—	12	ns
tOLZ(1)	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
tCHZ(1)	Chip Deselect to Output in High-Z	—	8	—	10	—	12	ns
tOHZ(1)	Output Disable to Output in High-Z	—	8	—	10	—	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tPU(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
tPD(1)	Chip Deselect to Power-Down Time	—	15	—	20	—	25	ns
Write Cycle								
tWC	Write Cycle Time	15	—	20	—	25	—	ns
tCW	Chip Select to End-of-Write	12	—	15	—	20	—	ns
tAW	Address Valid to End-of-Write	12	—	15	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	12	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tWHZ(1)	Write Enable to Output in High-Z	—	8	—	13	—	15	ns
tDW	Data to Write Time Overlap	10	—	12	—	15	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	ns
tOW(1)	Output Active from End-of-Write	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

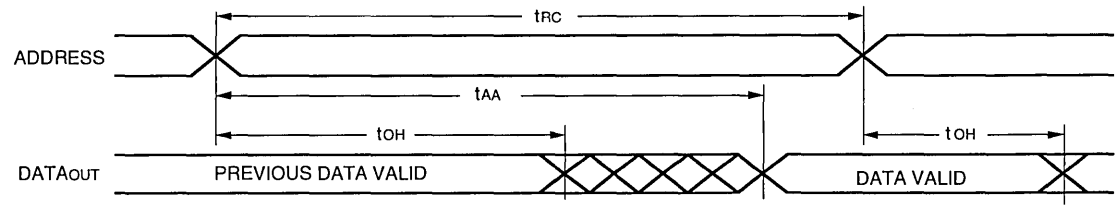
3148 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



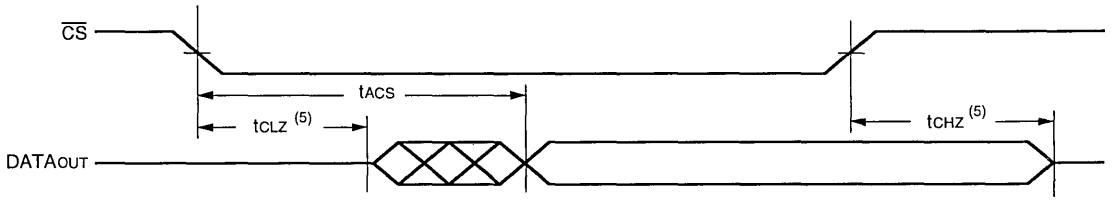
3148 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



3148 drw 06

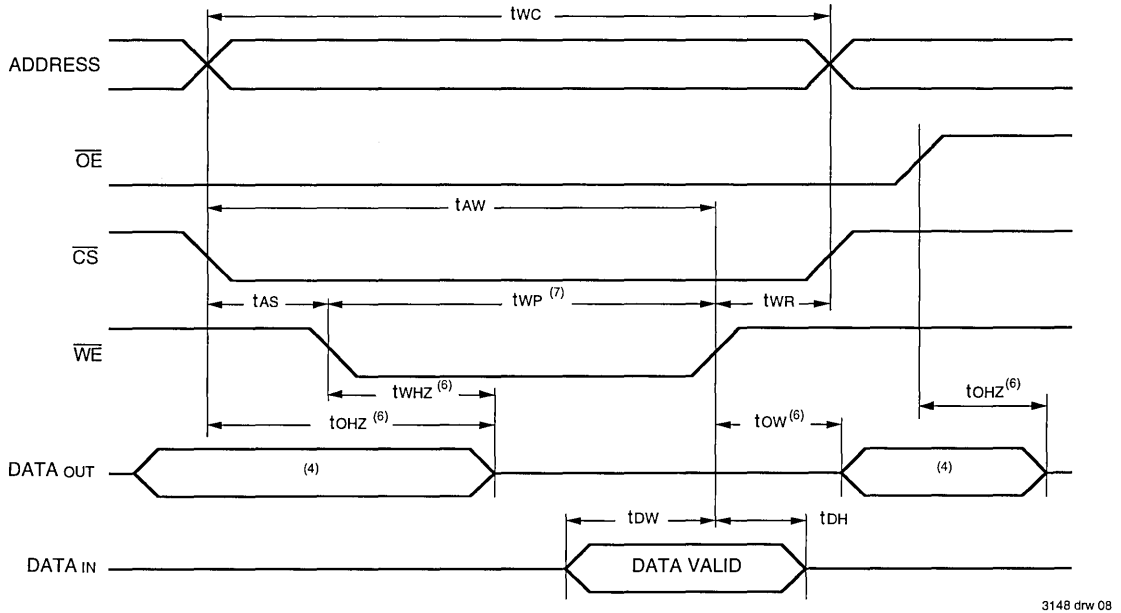
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



3148 drw 07

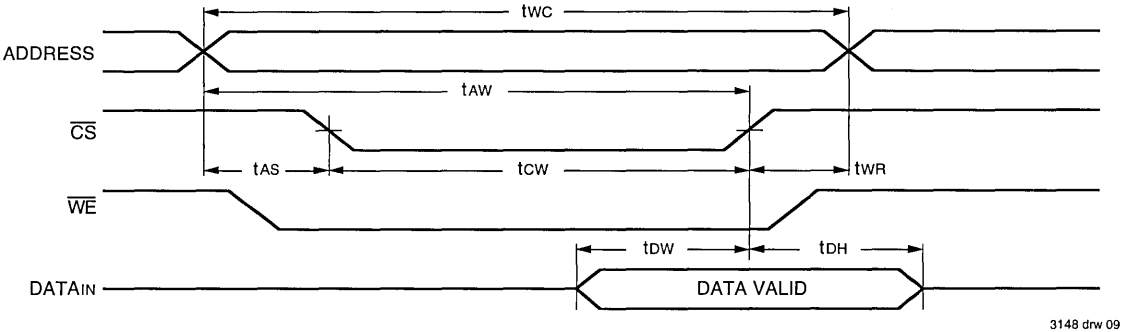
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (1, 2, 3, 7)



3148 drw 08

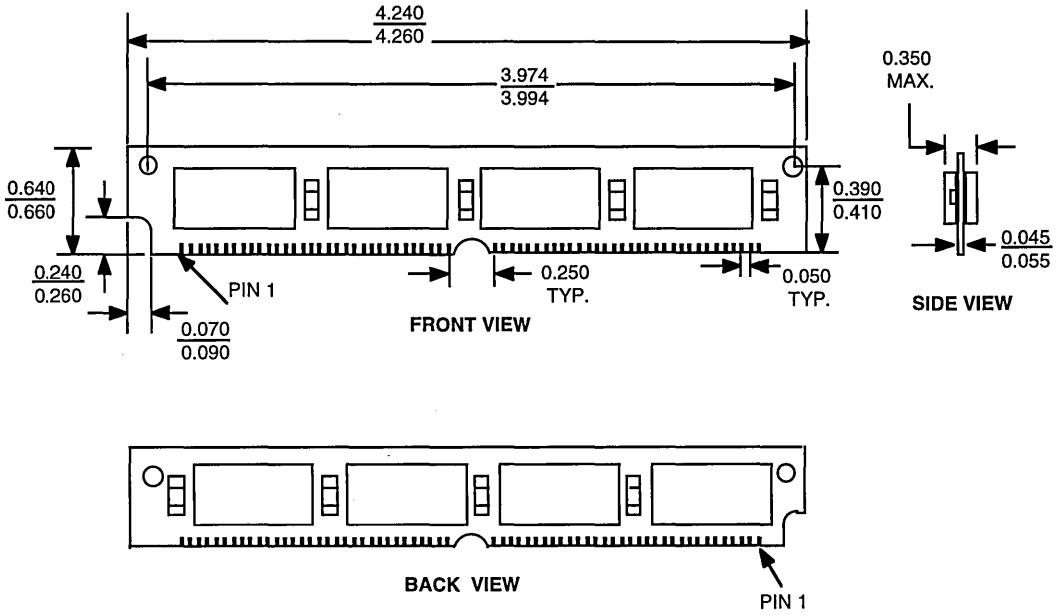
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (1, 2, 3, 5)



3148 drw 09

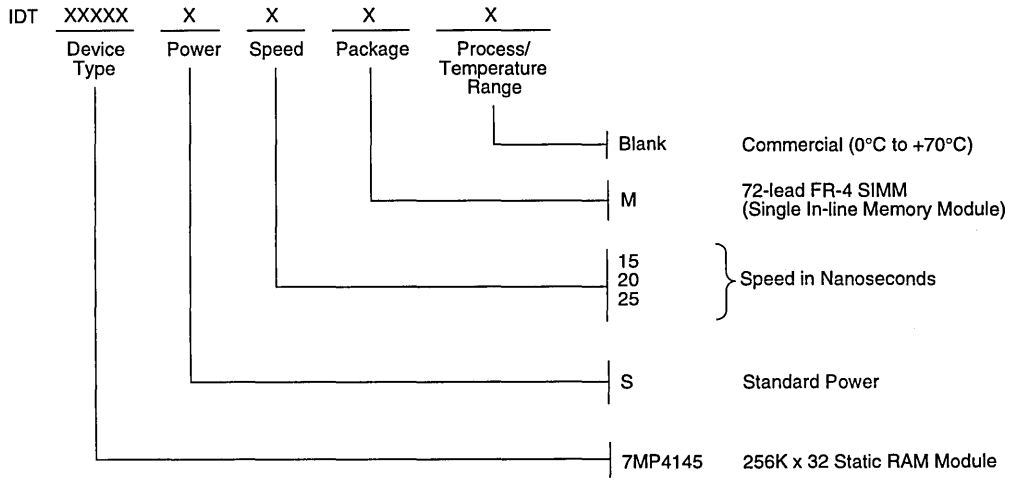
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS



3148 drw 10

ORDERING INFORMATION



3148 drw 11

Integrated Device Technology, Inc.

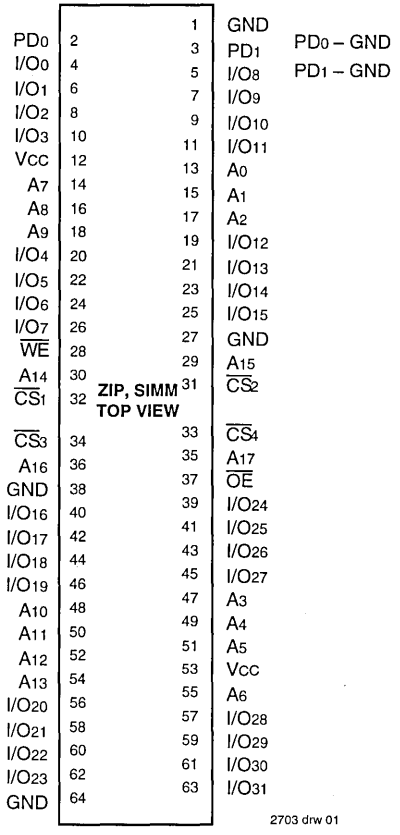
256K x 32 BiCMOS/CMOS STATIC RAM MODULE

IDT7MP4045

FEATURES:

- High density 1 megabyte static RAM module
- Low profile 64 pin ZIP (Zig-zag In-line vertical Package) or 64 pin SIMM (Single In-line Memory Module)
- Ultra fast access time: 10ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

PIN CONFIGURATION[1]



2703 drw 01

NOTE:

1. Pins 2 and 3 (PD_0 and PD_1) are read by the user to determine the density of the module. If PD_0 reads GND and PD_1 reads GND, then the module had a 256K depth.

DESCRIPTION:

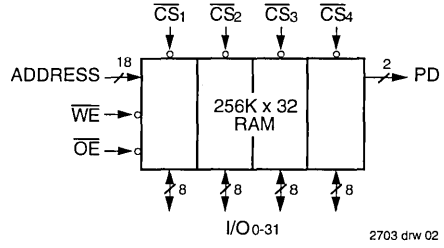
The IDT7MP4045 is a 256K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using 8 256K x 4 static RAMs in plastic SOJ packages. Availability of four chip select lines (one for each group of two RAMs) provides byte access. The IDT7MP4045 is available with access time as fast as 10ns with minimal power consumption.

The IDT7MP4045 is packaged in a 64 pin FR-4 ZIP (Zig-zag In-line vertical Package)or a 64 pin SIMM (Single In-line Memory Module). The ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.365 inches wide. At only 0.585 inches high, this low profile package is ideal for systems with minimum board spacing while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4045 are TTL-compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

Two identification pins (PD_0 and PD_1) are provided for applications in which different density versions of the module are used. In this way, the target system can read the respective levels of PD_0 and PD_1 to determine a 256K depth.

FUNCTIONAL BLOCK DIAGRAM



2703 drw 02

PIN NAMES

I/O_{0-31}	Data Inputs/Outputs
A_{0-17}	Addresses
$\overline{CS}_{1-4}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
PD_{0-1}	Depth Identification
VCC	Power
GND	Ground

2703 tbl 01

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	$V_{(IN)}$ = 0V	20	pF
$C_{IN(A)}$	Input Capacitance (Address & Control)	$V_{(IN)}$ = 0V	70	pF
$C_{I/O}$	I/O Capacitance	$V_{(OUT)}$ = 0V	12	pF

NOTE: 2703 tbl 02
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2703 tbl 03
1. V_{IL} (min) = –1.5V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2703 tbl 04

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

2703 tbl 05

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2703 tbl 06
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Address and Control)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	80	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output LOW	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output HIGH	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2703 tbl 07

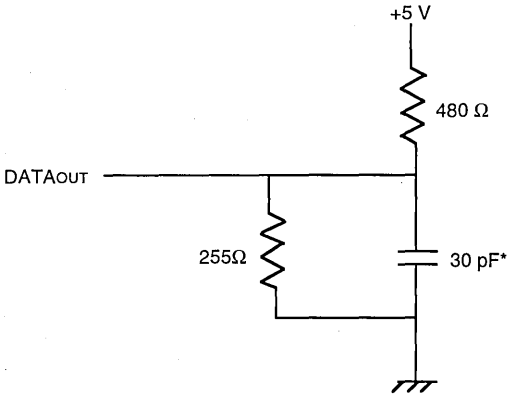
Symbol	Parameter	Test Conditions	10ns, 12ns Max.	15ns - 25ns Max.	Unit
I_{CC}	Dynamic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	1600	1360	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	480	480	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	320	120	mA

2703 tbl

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1-4

2703 tbl 09



*Includes scope and jig.

Figure 1. Output Load

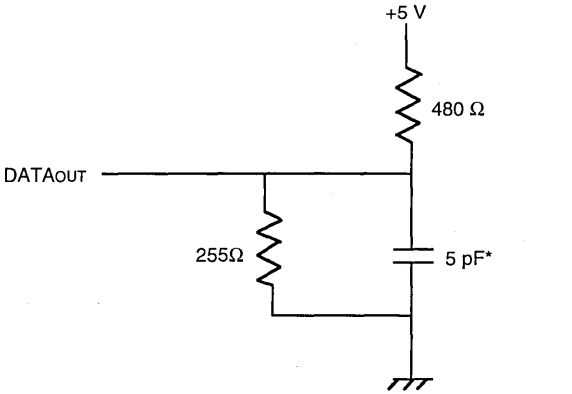


Figure 2. Output Load
(for t_{OLZ},t_{OHZ}, t_{CHZ}, t_{CLZ}, t_{WHZ}, t_{OW})

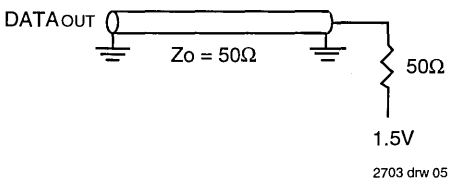


Figure 3. Alternate Output Load

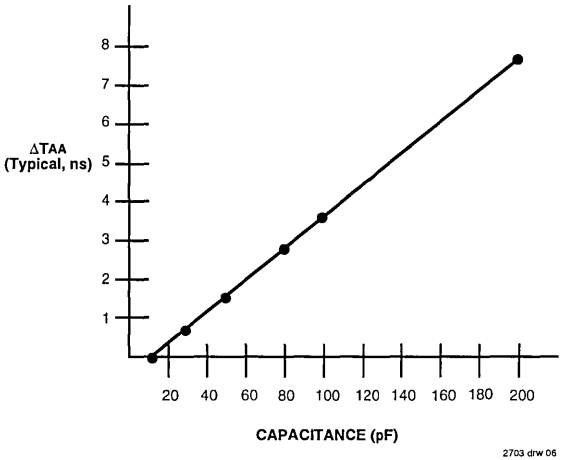


Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP4045SAxxZ, 7MP4045SAxxM -10 Min.	-10 Max.	-12 Min.	-12 Max.	Unit
Read Cycle						
t_{RC}	Read Cycle Time	10	—	12	—	ns
t_{AA}	Address Access Time	—	10	—	12	ns
t_{ACS}	Chip Select Access Time	—	10	—	12	ns
t_{CLZ}[1]	Chip Select to Output in Low Z	2	—	2	—	ns
t_{OE}	Output Enable to Output Valid	—	5	—	7	ns
t_{OLZ}[1]	Output Enable to Output in Low Z	0	—	0	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High Z	—	6	—	7	ns
t_{OHZ}[1]	Output Disable to Output in High Z	—	6	—	7	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
Write Cycle						
t_{WC}	Write Cycle Time	10	—	12	—	ns
t_{CW}	Chip Select to End of Write	8	—	10	—	ns
t_{AW}	Address Valid to End of Write	8	—	10	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	8	—	10	—	ns
t_{WR}	Write Recovery Time	1	—	1	—	ns
t_{WHZ}[1]	Write Enable to Output in High Z	—	5	—	6	ns
t_{DW}	Data to Write Time Overlap	6	—	7	—	ns
t_{DH}	Data Hold from Write Time	1	—	1	—	ns
t_{OW}[1]	Output Active from End of Write	1	—	1	—	ns

NOTE:
1. This parameter is guaranteed by design but not tested.

2703 tbl 10

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

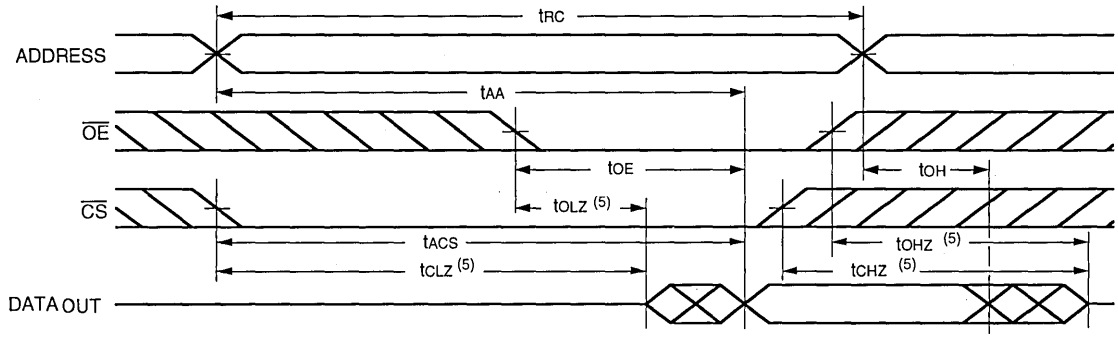
Symbol	Parameter	7MP4045SxxZ, 7MP4045SxxM						Unit
		-15		-20		-25		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	3	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	8	—	10	—	12	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	—	8	—	10	—	12	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	8	—	10	—	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	15	—	20	—	25	ns
Write Cycle								
t_{WC}	Write Cycle Time	15	—	20	—	25	—	ns
t_{CW}	Chip Select to End-of-Write	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	15	—	20	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	—	8	—	13	—	15	ns
t_{DW}	Data to Write Time Overlap	10	—	12	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End-of-Write	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design but not tested.

2703 tbl 11

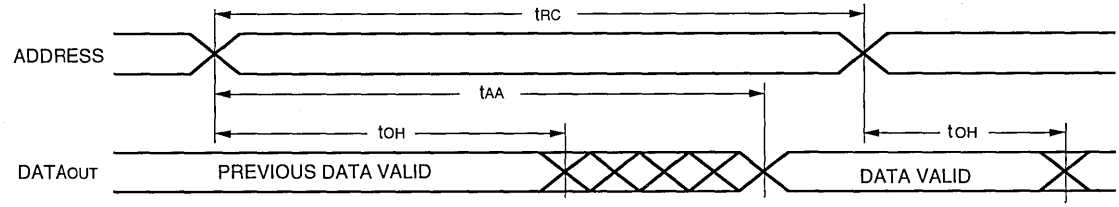
7

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



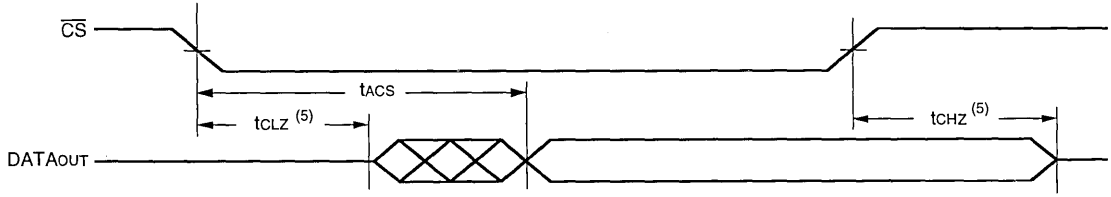
2703 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



2703 drw 08

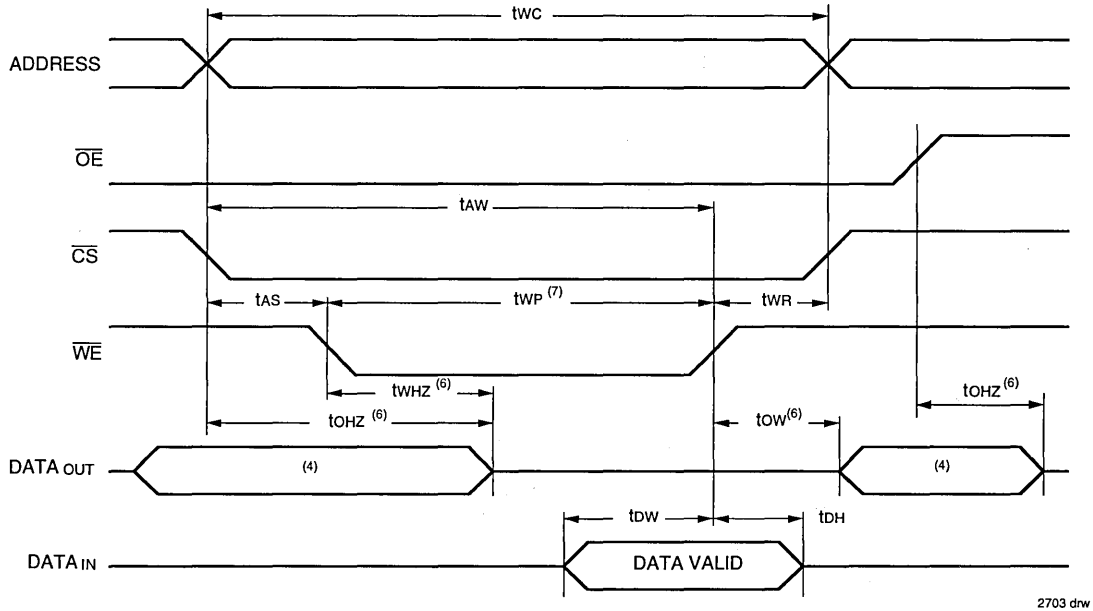
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



2703 drw 06

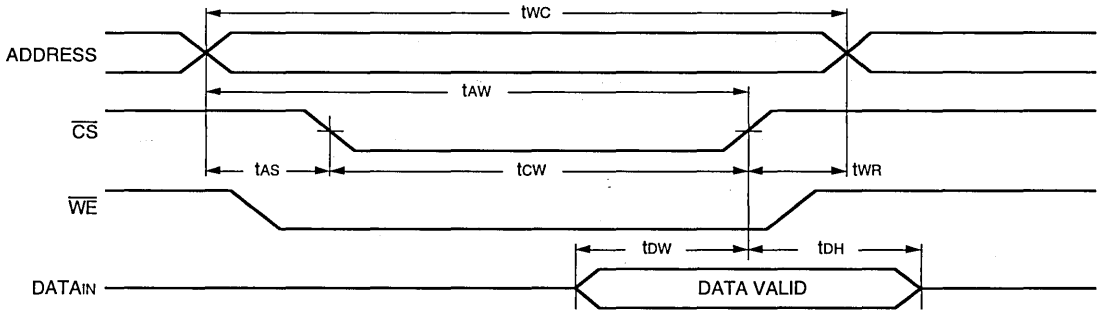
NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED) (1, 2, 3, 7)



2703 drw 10

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED) (1, 2, 3, 5)

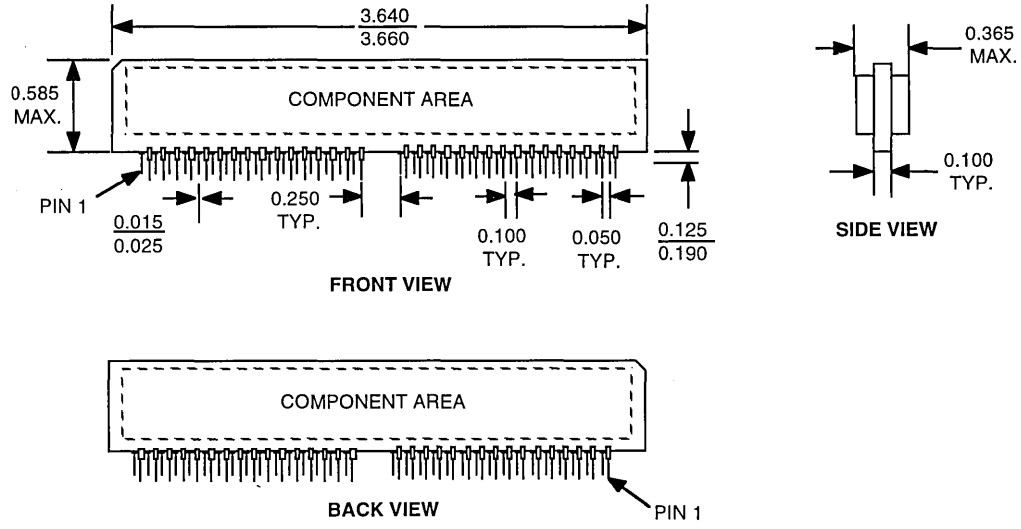


2703 drw 11

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

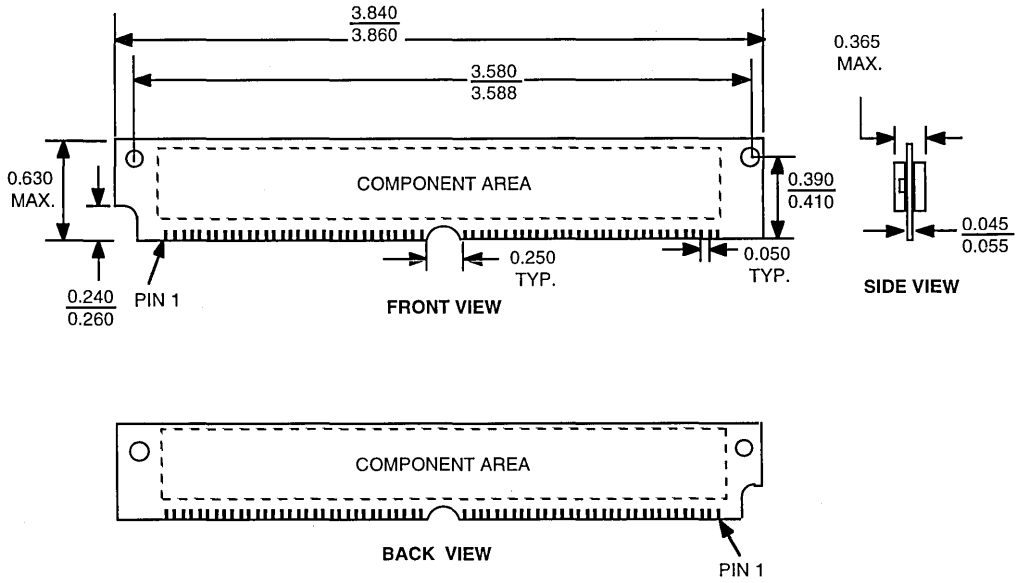
PACKAGE DIMENSIONS

ZIP VERSION



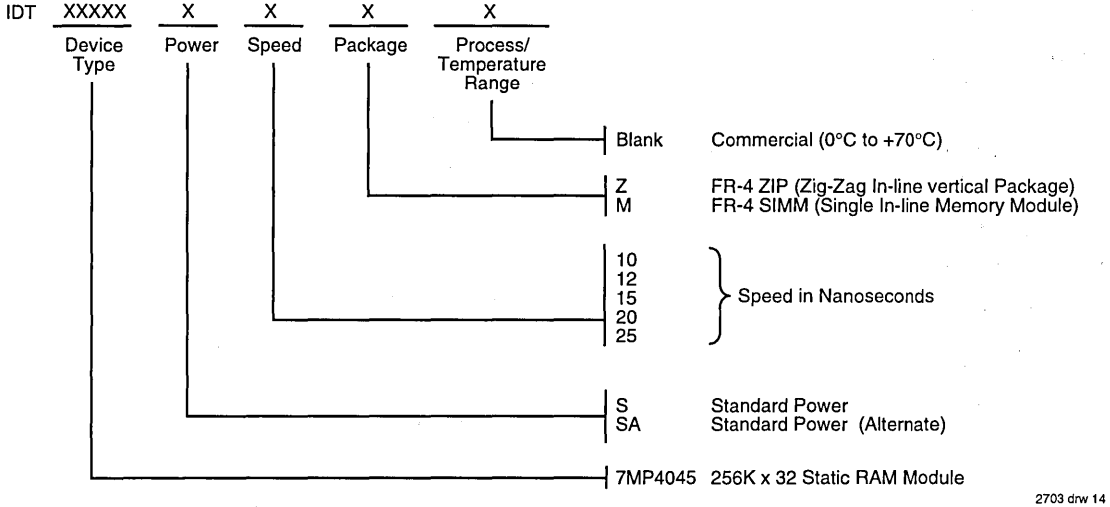
2703 drw 12

SIMM VERSION



2703 drw 13

ORDERING INFORMATION



2703 drw 14

7

Integrated Device Technology, Inc.

128K x 32 CMOS STATIC RAM MODULE

IDT7MP4095

FEATURES:

- High density 4 megabit static RAM module
- Low profile 64-pin ZIP (Zig-zag In-line vertical Package) or 64-pin SIMM (Single In-line Memory Module)
- Fast access time: 20ns (max.)
- Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- Single 5V (±10%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL compatible

PIN CONFIGURATION

PD_0 – GND
PD_1 – No Connect

		1	GND
PD_0	2	3	PD_1
I/O_0	4	5	I/O_8
I/O_1	6	7	I/O_9
I/O_2	8	9	I/O_{10}
I/O_3	10	11	I/O_{11}
V_{CC}	12	13	A_0
A_7	14	15	A_1
A_8	16	17	A_2
A_9	18	19	I/O_{12}
I/O_4	20	21	I/O_{13}
I/O_5	22	23	I/O_{14}
I/O_6	24	25	I/O_{15}
I/O_7	26	27	GND
$\overline{WE}$	28	29	A_{15}
A_{14}	30	31	$\overline{CS_2}$
$\overline{CS_1}$	32		
$\overline{CS_3}$		33	$\overline{CS_4}$
A_{16}	34	35	NC
GND	36	37	$\overline{OE}$
I/O_{16}	38	39	I/O_{24}
I/O_{17}	40	41	I/O_{25}
I/O_{18}	42	43	I/O_{26}
I/O_{19}	44	45	I/O_{27}
A_{10}	46	47	A_3
A_{11}	48	49	A_4
A_{12}	50	51	A_5
A_{13}	52	53	V_{CC}
I/O_{20}	54	55	A_6
I/O_{21}	56	57	I/O_{28}
I/O_{22}	58	59	I/O_{29}
I/O_{23}	60	61	I/O_{30}
GND	62	63	I/O_{31}
	64		

3147 drw 02

ZIP, SIMM
TOP VIEW

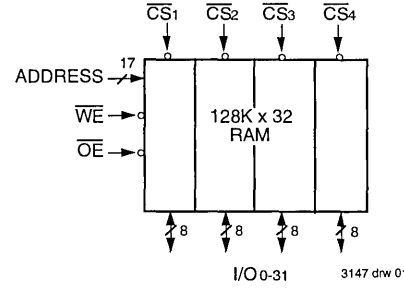
DESCRIPTION:

The IDT7MP4095 is a 128K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using four 128K x 8 static RAMs in plastic SOJ packages. The IDT7MP4095 is available with access times as fast as 20ns with minimal power consumption.

The IDT7MP4095 is packaged in a 64-pin FR-4 ZIP (Zig-zag In-line vertical Package) or a 64-pin SIMM (Single In-line Memory Module). The ZIP configuration allows 64 pins to be placed on a package 3.65 inches long and 0.21 inches thick. At only 0.60 inches high, this low-profile package is ideal for systems with minimum board spacing, while the SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the IDT7MP4095 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

I/O_{0-31}	Data Inputs/Outputs
A_{0-16}	Addresses
$\overline{CS_{1-4}}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground
NC	No Connect

3147 tbl 01

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
$C_{IN(D)}$	Input Capacitance (Data and $\overline{CS}$)	$V_{(IN)}$ = 0V	12	pF
$C_{IN(A)}$	Input Capacitance (Address, $\overline{WE}$, $\overline{OE}$)	$V_{(IN)}$ = 0V	40	pF
C_{OUT}	Output Capacitance	$V_{(OUT)}$ = 0V	12	pF

NOTE: 3147 tbl 04
1. This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	5.8	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 3147 tbl 05
1. V_{IL} (min) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

3147 tbl 06

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Read	L	H	H	High-Z	Active

3147 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTES: 3147 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage (Data and $\overline{CS}$)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI}\|$	Input Leakage (Address, $\overline{WE}$, and $\overline{OE}$)	V_{CC} = Max.; V_{IN} = GND to V_{CC}	—	40	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max.; $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
V_{OL}	Output Low	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

Symbol	Parameter	Test Conditions	Max.	Unit
I_{CC}	Dymanic Operating Current	f = f_{MAX}; $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	680	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max. Outputs Open, f = f_{MAX}	160	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} – 0.2V; f = 0 V_{IN} > V_{CC} – 0.2V or < 0.2V	60	mA

3147 tbl 07

7

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

3147 tbl 08

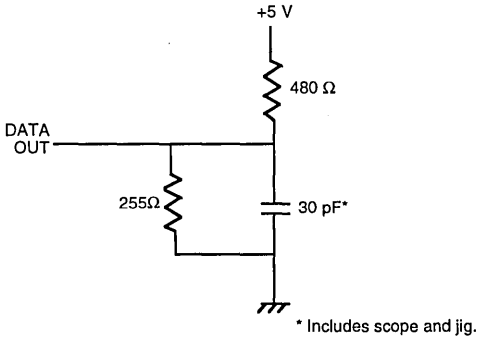


Figure 1. Output Load

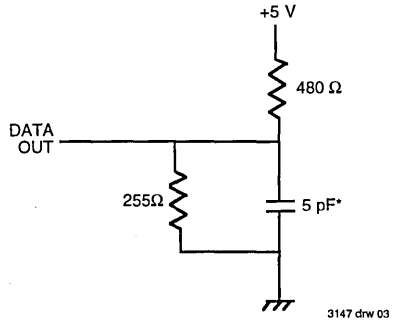


Figure 2. Output Load
(for tOLZ, tOHZ, tCHZ, tCLZ, tWHZ, tOW)

AC ELECTRICAL CHARACTERISTICS

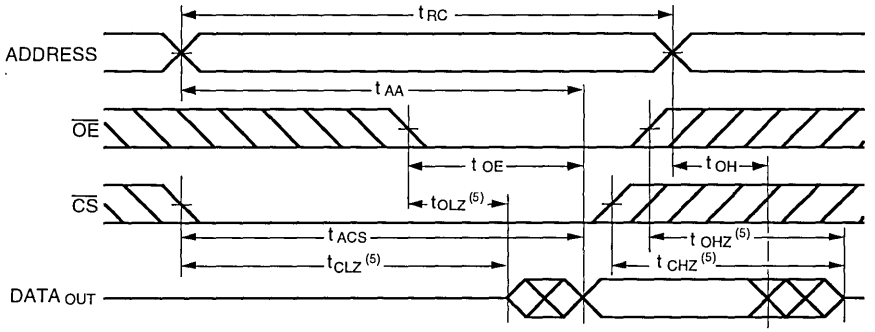
(V_{CC} = 5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	-20 Min.	-20 Max.	-25 Min.	-25 Max.	Unit
Read Cycle						
tRC	Read Cycle Time	20	—	25	—	ns
tAA	Address Access Time	—	20	—	25	ns
tACS	Chip Select Access Time	—	20	—	25	ns
tCLZ(1)	Chip Select to Output in Low Z	3	—	3	—	ns
tOE	Output Enable to Output Valid	—	10	—	12	ns
tOLZ(1)	Output Enable to Output in Low Z	0	—	0	—	ns
tCHZ(1)	Chip Deselect to Output in High Z	—	12	—	15	ns
tOHZ(1)	Output Disable to Output in High Z	—	12	—	15	ns
tOH	Output Hold from Address Change	3	—	3	—	ns
tPU(1)	Chip Select to Power-Up Time	0	—	0	—	ns
tPD(1)	Chip Deselect to Power-Down Time	—	20	—	25	ns
Write Cycle						
tWC	Write Cycle Time	20	—	25	—	ns
tCW	Chip Select to End of Write	18	—	20	—	ns
tAW	Address Valid to End of Write	18	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	ns
tWP	Write Pulse Width	18	—	20	—	ns
tWR	Write Recovery Time	3	—	3	—	ns
tWHZ(1)	Write Enable to Output in High Z	—	13	—	15	ns
tDW	Data to Write Time Overlap	12	—	15	—	ns
tDH	Data Hold from Write Time	0	—	0	—	ns
tOW(1)	Output Active from End of Write	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

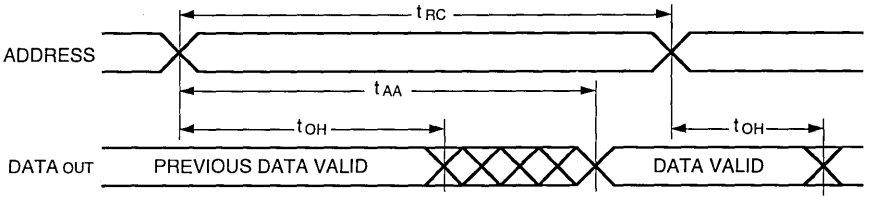
3147 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



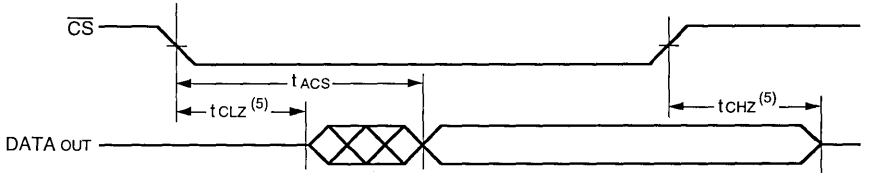
3147 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)



3147 drw 05

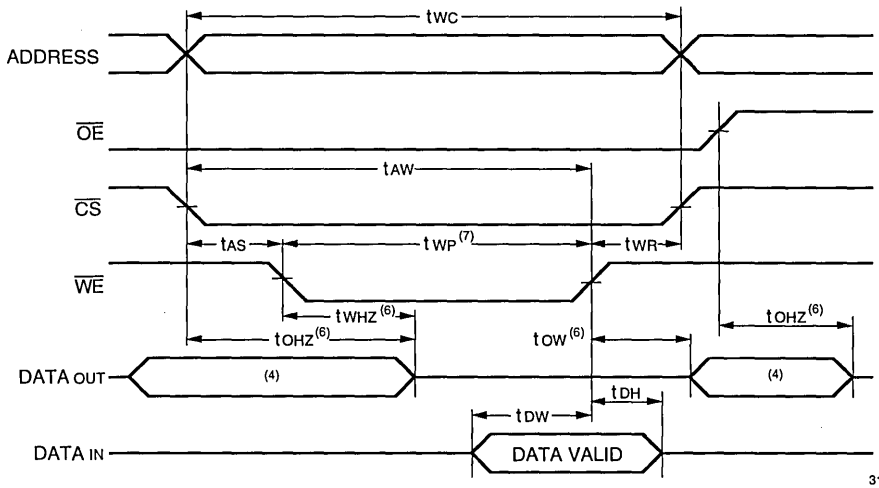
TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)



3147 drw 06

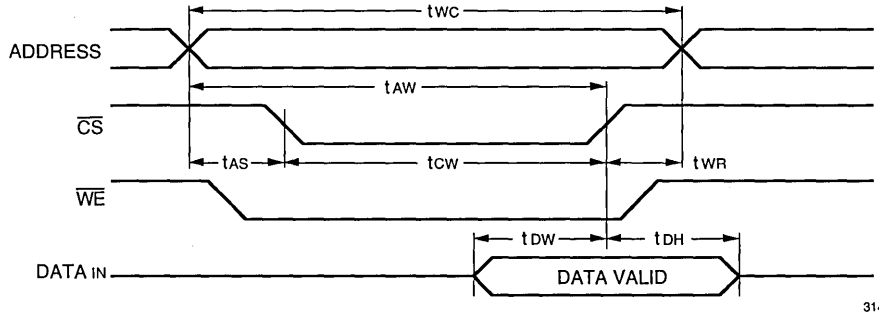
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected. $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



3147 drw 07

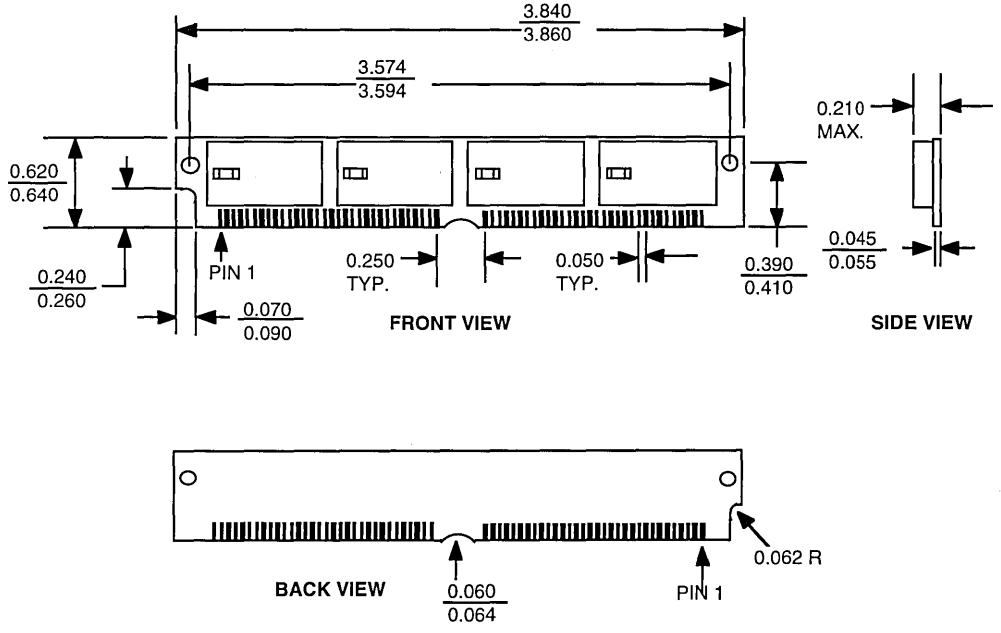
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



3147 drw 08

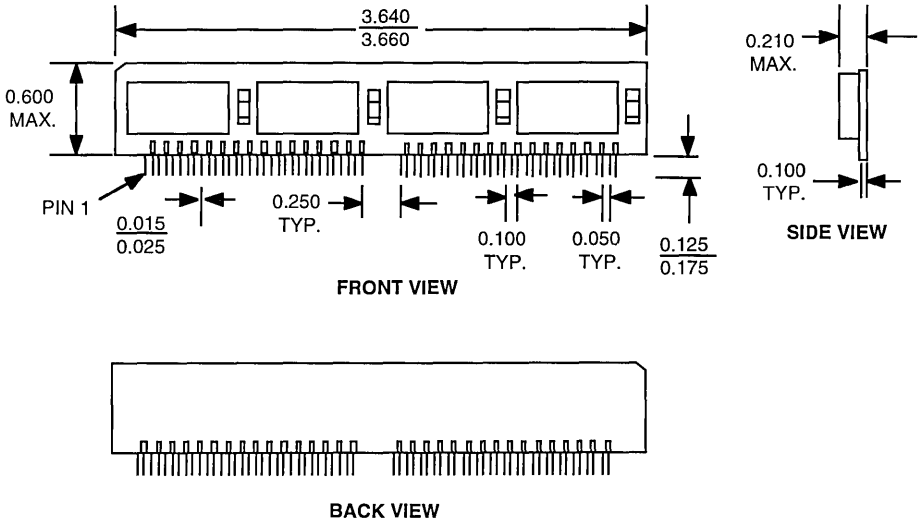
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW).

PACKAGE DIMENSIONS
SIMM VERSION



3147 drw 09

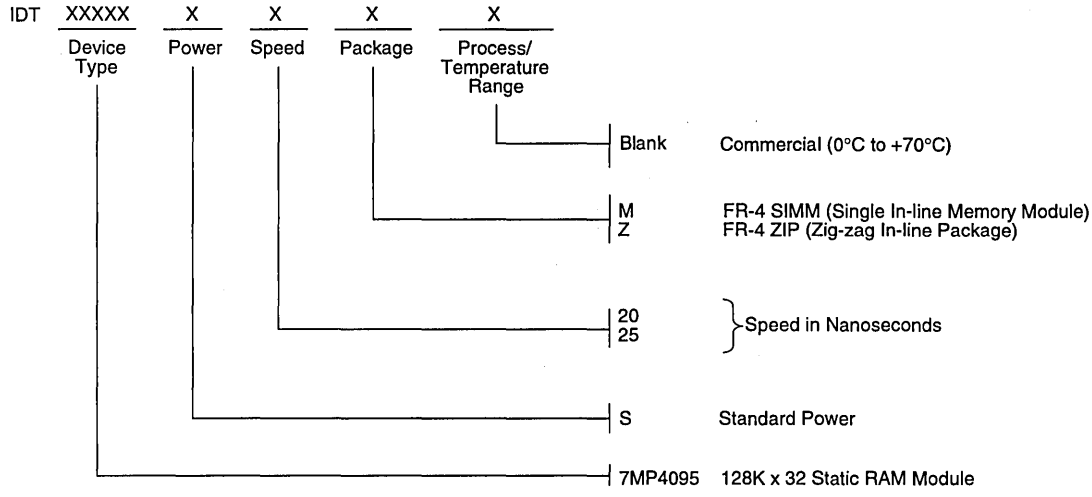
ZIP VERSION



3147 drw 10

7

ORDERING INFORMATION



3147 drw 11

Integrated Device Technology, Inc.

2M x 8 CMOS STATIC RAM MODULE

PRELIMINARY
IDT7M4084

FEATURES:

- High-density 16 megabit (2M x 8) Static RAM module
- Equivalent to the JEDEC standard for future monolithic
- Fast access time: 55ns (max.)
- Low power consumption
  - — Active: 110mA (max.)
  - — CMOS Standby: 450µA (max.)
  - — Data Retention: 250µA (max.) Vcc = 2V
- Surface mounted plastic packages on a 36-pin, 600 mil FR-4 DIP (Dual-In-Line Package) substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible

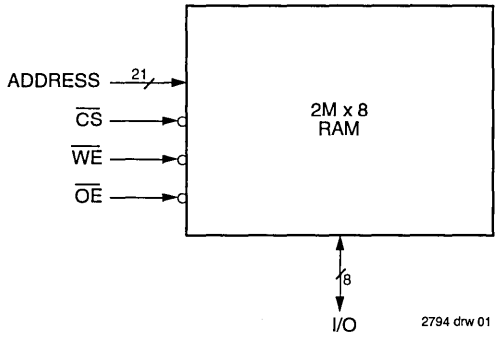
DESCRIPTION:

The IDT7M4084 is a 16 megabit (2M x 8) Static RAM module constructed on a co-fired ceramic substrate using four 512K x 8 Static RAMs and a decoder. The IDT7M4084 is available with access times as fast as 55ns, and a data retention current of 250µA and a standby current of 450µA.

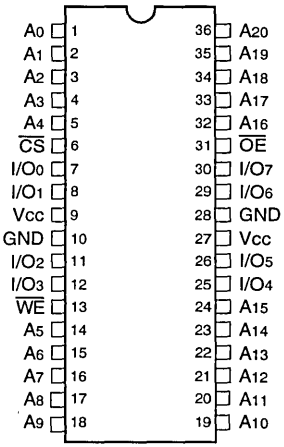
The IDT7M4084 is packaged in a 36-pin ceramic DIP resulting in the same JEDEC footprint in a package 1.8 inches long and 0.6 inches wide.

All inputs and outputs of the7M4084 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP
TOP VIEW

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-20	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2794 tbl 01

The IDT logo is a registered trademark of Integrated Device Technology Inc.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2794 tbl 02

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	35	pF
CIN(C)	Input Capacitance ($\overline{CS}$)	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	35	pF

NOTE:
2794 tbl 03

1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE:
2794 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
2794 tbl 04

1. VIL = -2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2794 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	7M4084LxxN		Unit
			Min.	Max.	
|ILI|	Input Leakage	VCC = Max., VIN = GND to VCC	—	20	µA
|ILO|	Output Leakage	VCC = Max., $\overline{CS}$ = VIH, VOUT = GND to VCC	—	20	µA
VOL	Output Low Voltage	VCC = Min., IOL = 2mA	—	0.4	V
VOH	Output High Voltage	VCC = Min., IOH = -1mA	2.4	—	V
ICC	Dynamic Operating Current	VCC = Max., $\overline{CS}$ ≤ VIL; f = fMAX,	—	110	mA
ISB	Standby Supply Current (TTL Levels)	$\overline{CS}$ ≥ VIH, VCC = Max., f = fMAX, Outputs Open	—	12	mA
ISB1	Full Standby Supply Current (CMOS Levels)	$\overline{CS}$ ≥ VCC - 0.2V, VIN ≥ VCC - 0.2V or ≤ 0.2V	—	450	µA

2794 tbl 07

DATA RETENTION CHARACTERISTICS

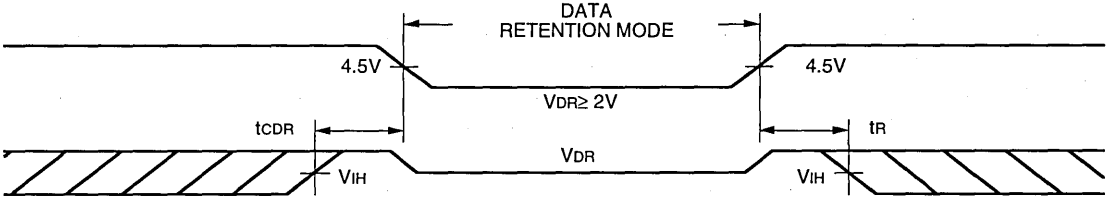
(T_A = 0°C to +70°C)

Symbol	Parameter	Test Condition	Min.	Max. V_{CC} @ 2.0V	Unit
V_{DR}	V_{CC} for Data Retention	—	2.0	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC}$ - 0.2V	—	250	µA
t_{CDR}(2)	Chip Deselect to Data Retention Time	$V_{IN} \leq V_{CC}$ - 0.2V or	0	—	ns
t_R(2)	Operation Recovery Time	$V_{IN} \geq 0.2V$	t_{RC}(1)	—	ns

NOTES:
1. t_{RC} = Read Cycle Time.
2. This parameter is guaranteed by design, but not tested.

2794 tbl 08

DATA RETENTION WAVEFORM

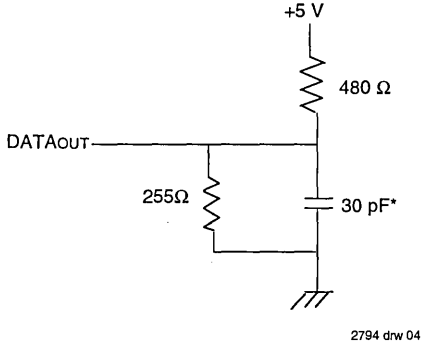


2794 drw 03

AC TEST CONDITIONS

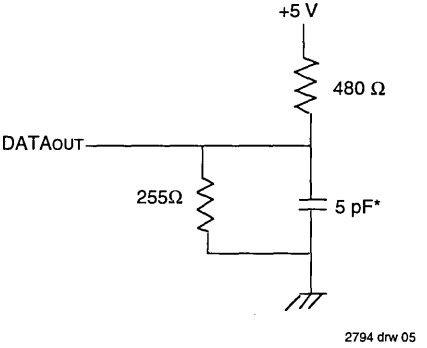
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2794 tbl 09



2794 drw 04

Figure 1. Output Load



2794 drw 05

Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

7

AC ELECTRICAL CHARACTERISTICS

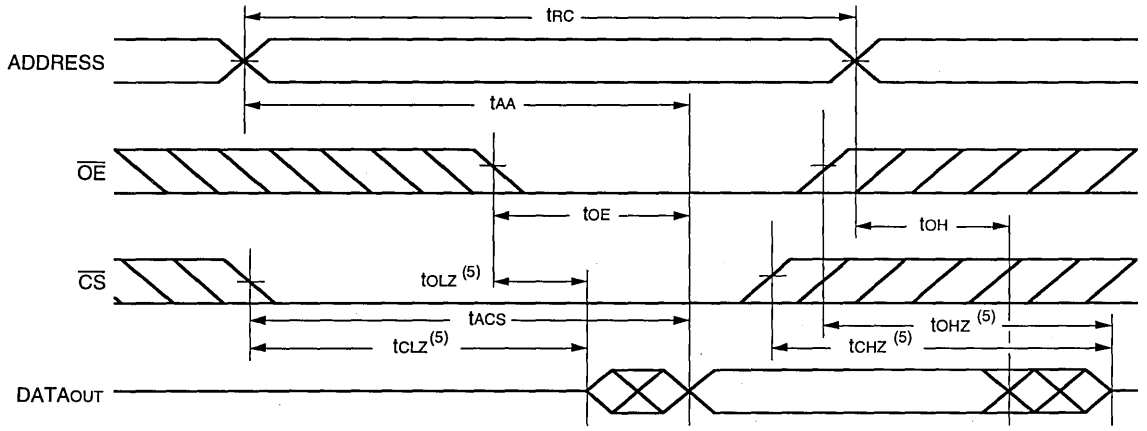
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7M4084LxxN						Unit
		-55		-70		-85		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	55	—	70	—	85	—	ns
t_{AA}	Address Access Time	—	55	—	70	—	85	ns
t_{ACS}	Chip Select Access Time	—	55	—	70	—	85	ns
t_{OE}	Output Enable to Output Valid	—	30	—	45	—	48	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	—	20	—	30	—	33	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	5	—	5	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High-Z	—	20	—	40	—	43	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	55	—	70	—	85	ns
Write Cycle								
t_{WC}	Write Cycle Time	55	—	70	—	85	—	ns
t_{WP}	Write Pulse Width	55	—	55	—	65	—	ns
t_{AS}	Address Set-up Time	5	—	0	—	2	—	ns
t_{AW}	Address Valid to End-of-Write	50	—	65	—	82	—	ns
t_{CW}	Chip Select to End-of-Write	50	—	65	—	80	—	ns
t_{DW}	Data to Write Time Overlap	20	—	35	—	38	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	—	20	—	30	—	33	ns
t_{OW}[1]	Output Active from End-of-Write	5	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design, but not tested.

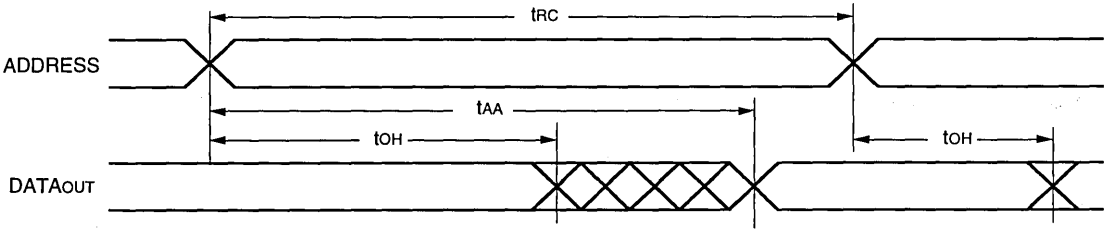
2794 tbl 10

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



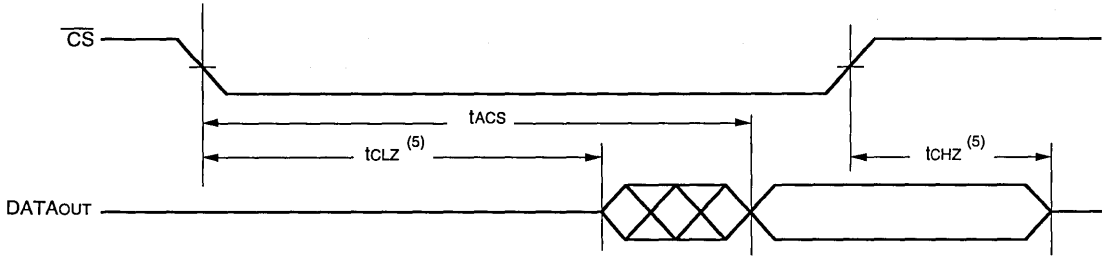
2794 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2794 drw 07

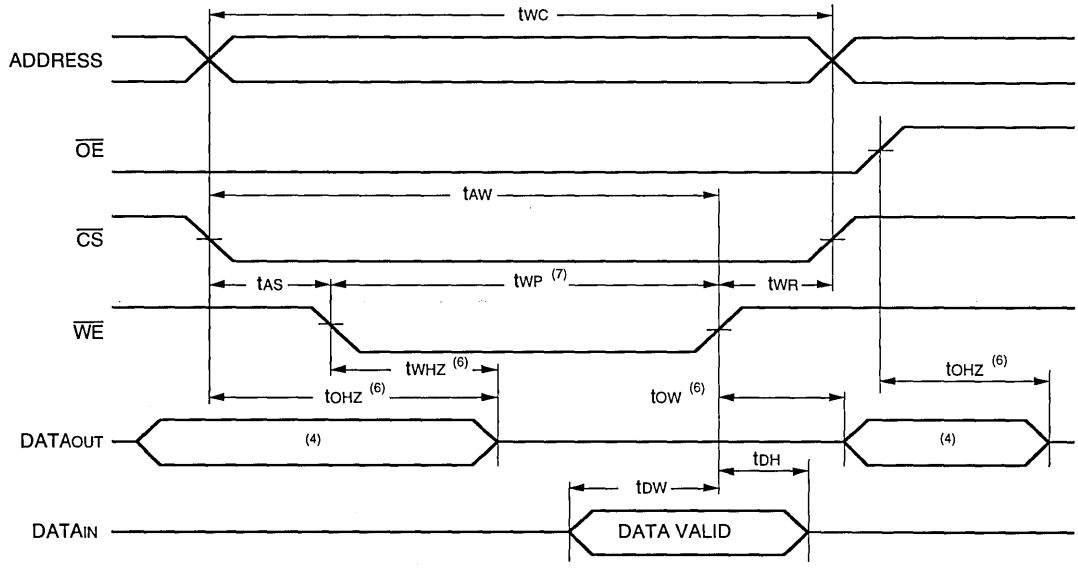
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



2794 drw 08

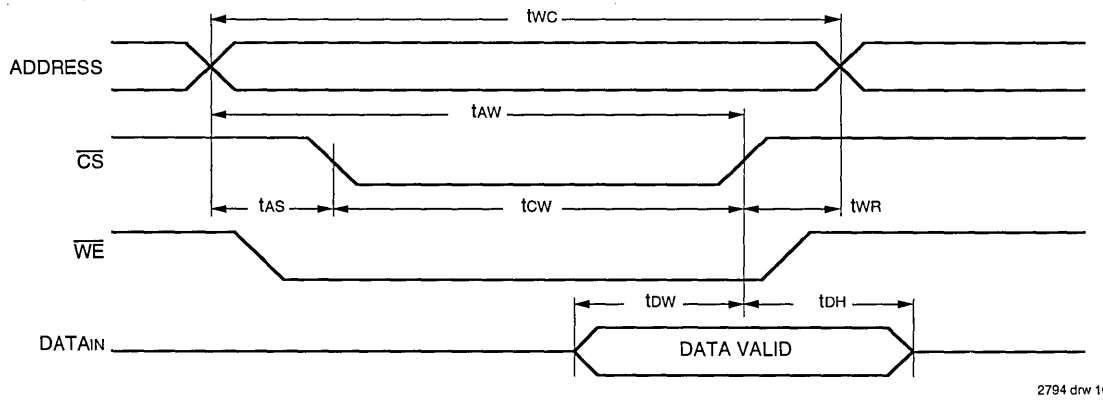
NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)



2794 drw 09

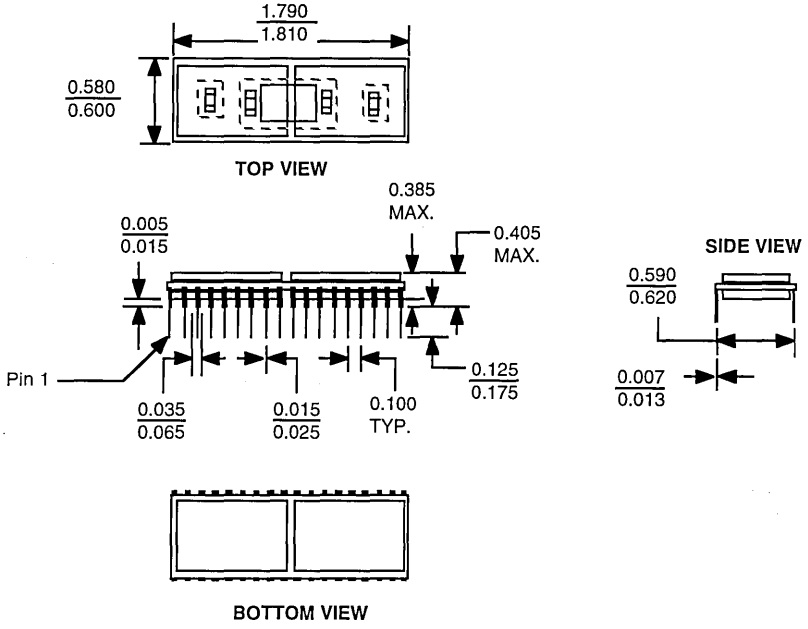
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



2794 drw 10

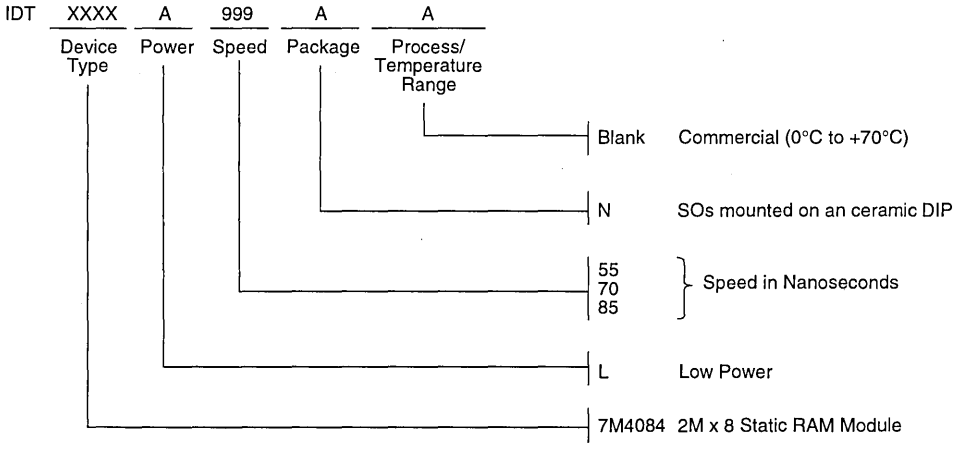
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the greater of tWP or tWHZ + tDW to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS



2794 drw 11

ORDERING INFORMATION



2794 drw 12

7

Integrated Device Technology, Inc.

512K x 8 CMOS STATIC RAM MODULE

IDT7MB4048

FEATURES:

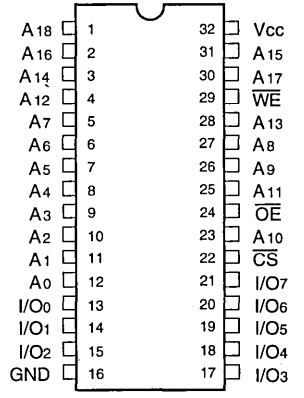
- High-density 4-megabit (512K x 8) Static RAM module
- Fast access time: 25ns (max.)
  Surface mounted plastic packages on a 32-pin, 600 mil FR-4 DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible

DESCRIPTION:

The IDT7MB4048 is a 4-megabit (512K x 8) Static RAM module constructed on a multilayer epoxy laminate (FR-4) substrate using four 1 megabit SRAMs and a decoder. The IDT7MB4048 is available with access times as fast as 25ns. The IDT7MB4048 is packaged in a 32-pin FR-4 DIP resulting in the JEDEC footprint in a package 1.6 inches long and 0.6 inches wide.

All inputs and outputs of the IDT7MB4048 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

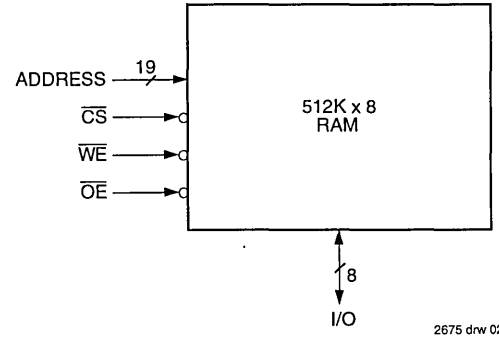
PIN CONFIGURATION



2675 drw 01

DIP
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



2675 drw 02

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-18	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
Vcc	Power
GND	Ground

2675 tbl 01

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2675 tbl 02

CAPACITANCE[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	35	pF
$C_{IN(C)}$	Input Capacitance ($\overline{CS}$)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	35	pF

NOTE: 2675 tbl 03
1. This parameter is guaranteed by design, but not tested.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2675 tbl 05
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 2675 tbl 04
1. V_{IL} = –2.0V for pulse width less than 10ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 10%

2675 tbl 06

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	7MB4048SxxP Min.	7MB4048SxxP Max.	Unit
$\|I_{LI}\|$	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	8	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	8	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –1mA	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$; f = f_{MAX}, Outputs Open	—	480	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	250	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2	—	170	mA

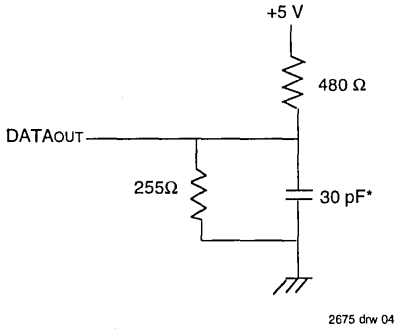
2675 tbl 07

7

AC TEST CONDITIONS

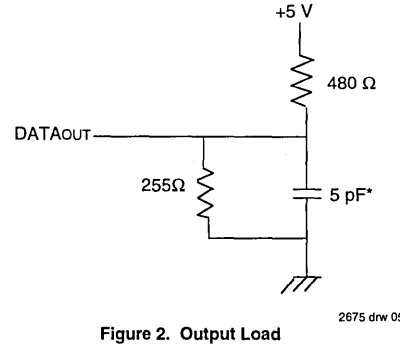
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2675 tbl 09



2675 drw 04

Figure 1. Output Load



2675 drw 05

Figure 2. Output Load
(for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, t_{OW} and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

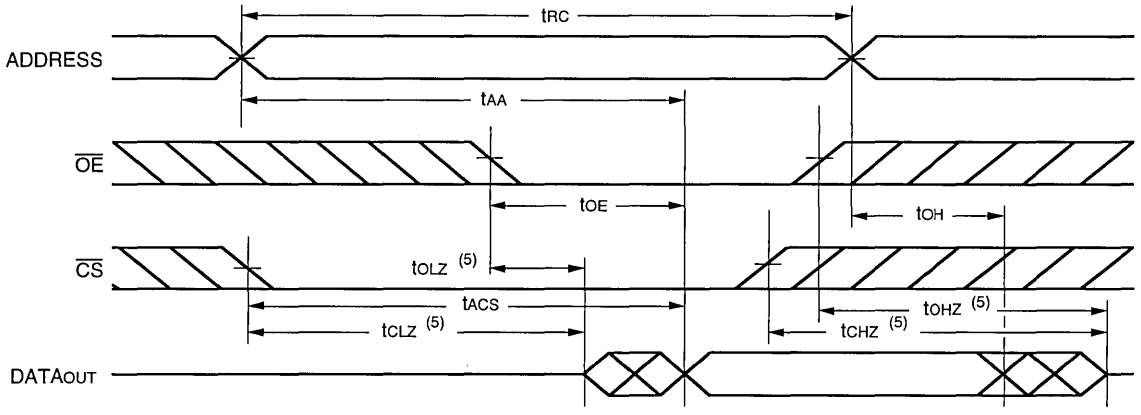
		7MB4048						
		-25		-30		-35		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle								
t_{RC}	Read Cycle Time	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	15	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	12	—	12	—	15	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	5	—	5	—	5	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	—	14	—	16	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	25	—	30	—	35	ns
Write Cycle								
t_{WC}	Write Cycle Time	25	—	30	—	35	—	ns
t_{WP}	Write Pulse Width	17	—	20	—	25	—	ns
t_{AS}(2)	Address Set-up Time	3	—	0	—	0	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End-of-Write	20	—	25	—	30	—	ns
t_{DW}	Data to Write Time Overlap	15	—	17	—	20	—	ns
t_{DH}(2)	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}(2)	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	—	15	—	15	—	15	ns
t_{OW}(1)	Output Active from End-of-Write	2	—	5	—	5	—	ns

NOTES

2675 tbl 10

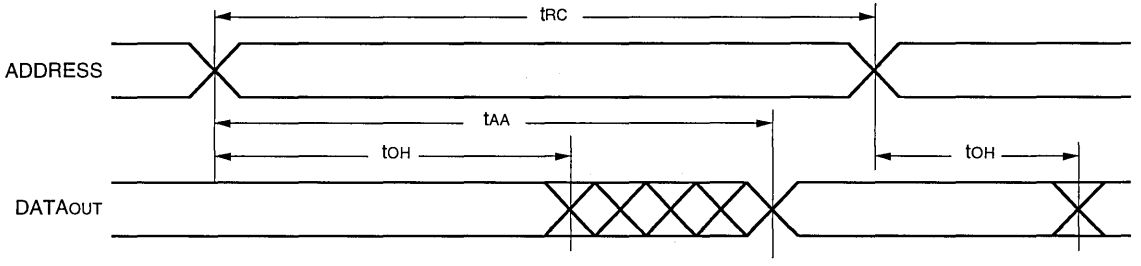
1. This parameter is guaranteed by design, but not tested.
2. t_{AS}=0ns for $\overline{CS}$ controlled write cycles. t_{DH}, t_{WR}= 3ns for $\overline{CS}$ controlled write cycles.

TIMING WAVEFORM OF READ CYCLE NO. 1(1)



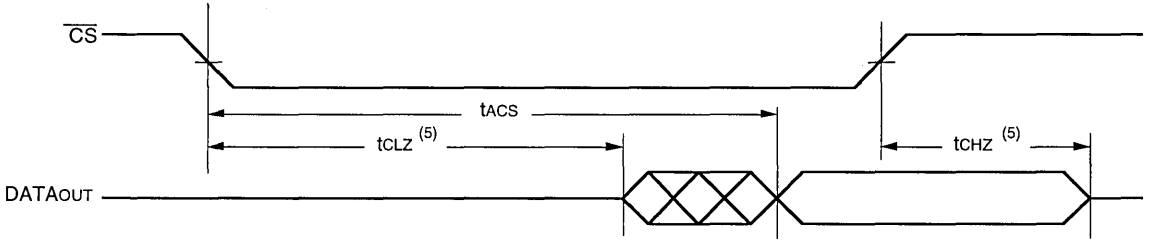
2675 drw 06

TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



2675 drw 07

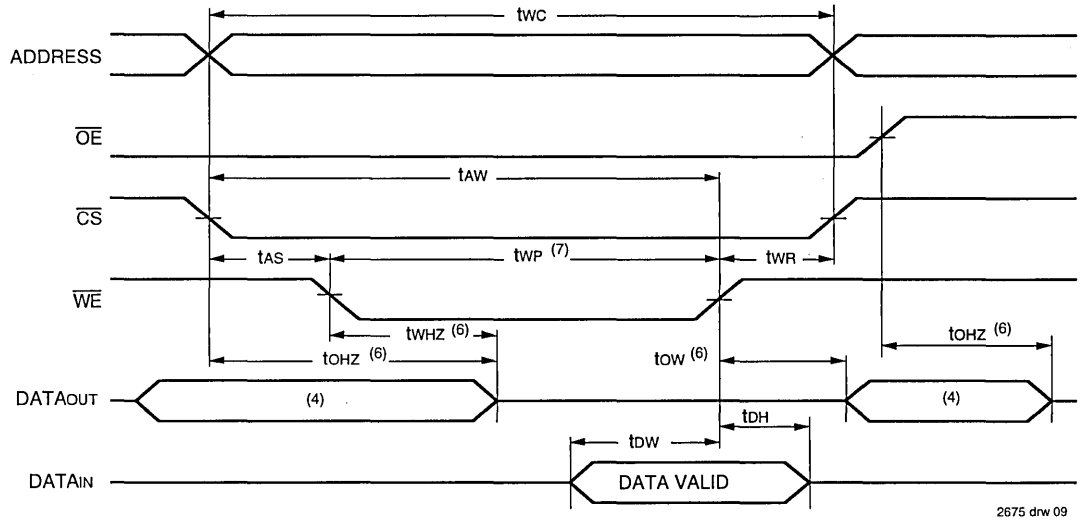
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



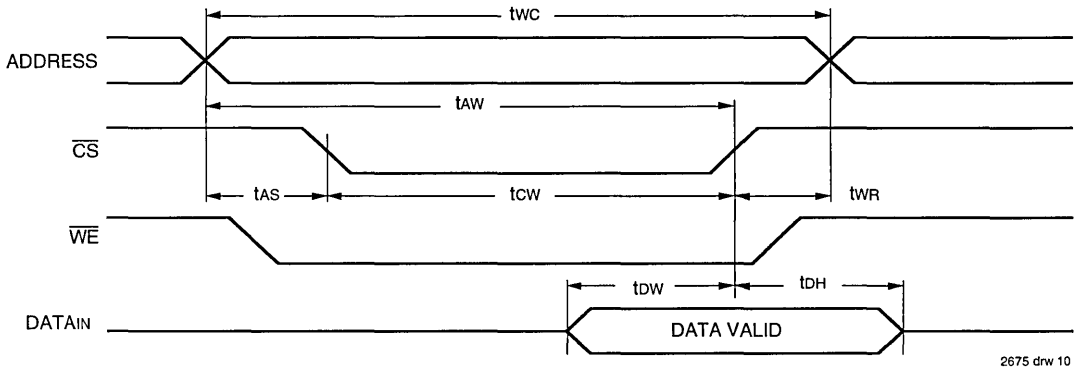
2675 drw 08

NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

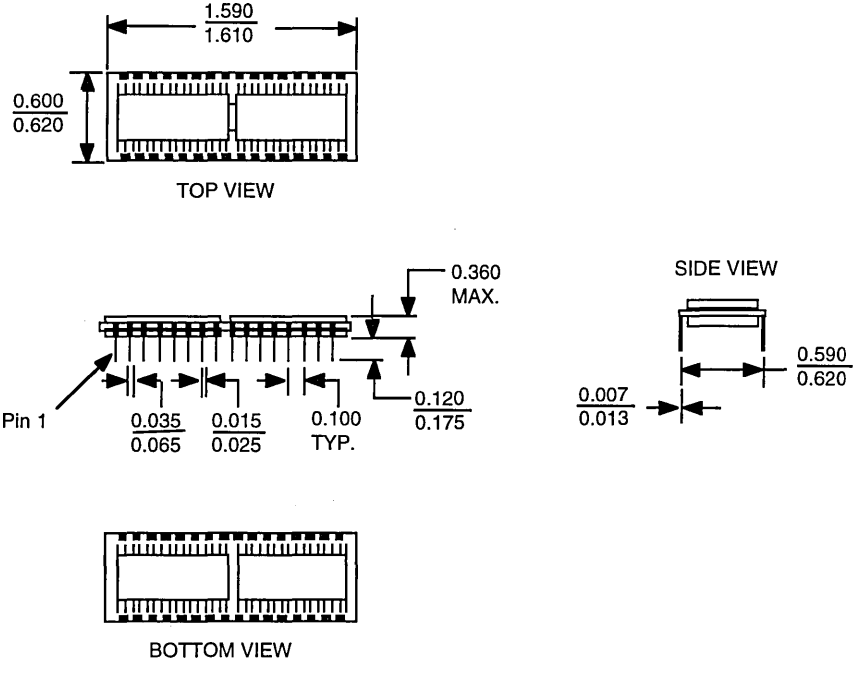


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



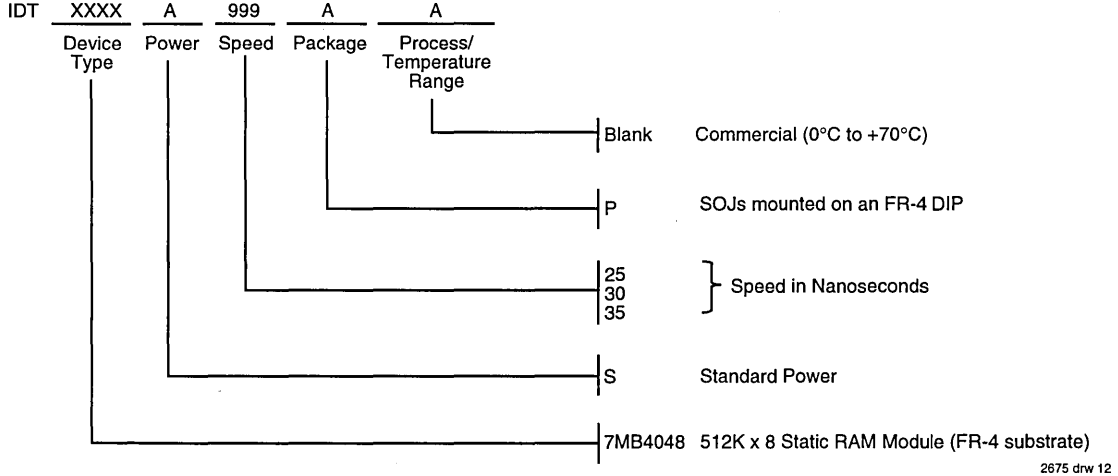
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS



2675 drw 11

ORDERING INFORMATION[1]



2675 drw 12

7

Integrated Device Technology, Inc.

512K x 8 CMOS STATIC RAM MODULE

IDT7M4048

FEATURES:

- High-density 4 megabit CMOS Static RAM module
- Equivalent to the JEDEC standard for future monolithic 512K x 8 StaticRAMs
- Fast access time: 25ns (max.)
- Surface mounted LCCs (leadless chip carriers) on a 32-pin, 600 mil ceramic DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible

DESCRIPTION:

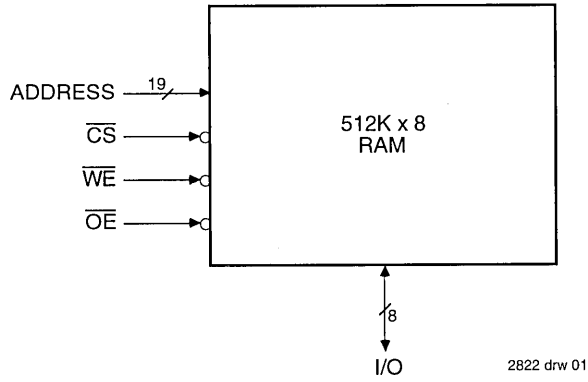
The IDT7M4048 is a 4 megabit (512K x 8) CMOS Static RAM module constructed on a co-fired ceramic substrate using four 1 Megabit StaticRAMs and a decoder. The IDT7M4048 is available with access times as fast as 25ns.

The IDT7M4048 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 0.6 inches wide, packing 4 megabits into the JEDEC DIP footprint.

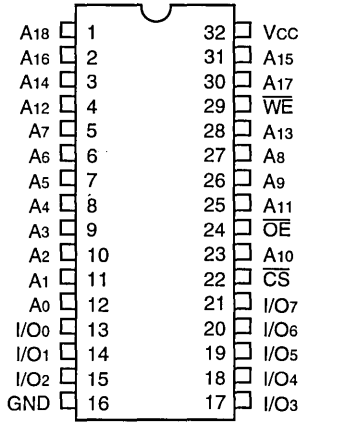
All inputs and outputs of the IDT7M4048 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



2822 drw 02

DIP
TOP VIEW

PIN NAMES

I/O0-7	Data Inputs/Outputs
A0-18	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power
GND	Ground

2822 tbl 04

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High-Z	Standby
Read	L	L	H	DOUT	Active
Read	L	H	H	High-Z	Active
Write	L	X	L	DIN	Active

2822 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Military	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	–55 to +125	°C
TBIAS	Temperature Under Bias	–65 to +135	°C
TSTG	Storage Temperature	–65 to +160	°C
IOUT	DC Output Current	50	mA

NOTE: 2822 tbl 05

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE(1) (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	50	pF
CIN(C)	Input Capacitance ($\overline{CS}$)	VIN = 0V	10	pF
COUT	Output Capacitance	VOUT = 0V	40	pF

NOTE: 2822 tbl 02

1. This parameter is guaranteed by design, but not tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Military	–55°C to +125°C	0V	5V ± 10%

2822 tbl 06

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2822 tbl 03

1. VIL = –1.5V for pulse width less than 10ns.

7

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

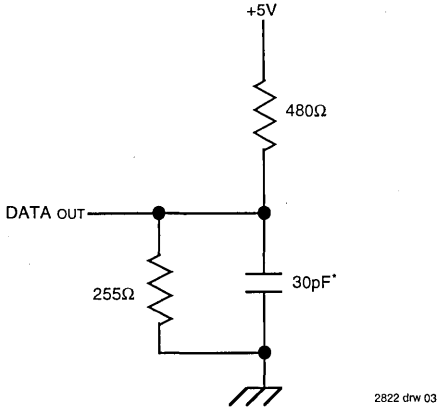
Symbol	Parameter	Test Conditions	7M4048SxxCB Min.	7M4048SxxCB Max.	Unit
I_{LI}	Input Leakage	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	µA
I_{LO}	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	20	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	—	V
I_{CC}	Dynamic Operating Current	V_{CC} = Max., $\overline{CS} \leq V_{IL}$; f = f_{MAX}, Outputs Open	—	300	mA
I_{SB}	Standby Supply Current (TTL Levels)	$\overline{CS} \geq V_{IH}$, V_{CC} = Max., f = f_{MAX}, Outputs Open	—	160	mA
I_{SB1}	Full Standby Supply Current (CMOS Levels)	$\overline{CS} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or ≤ 0.2V, V_{CC} = Max., f = 0, Outputs Open	—	85	mA

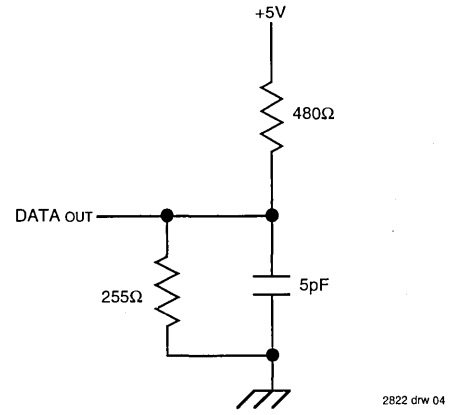
2822 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2822 tbl 08





* Including scope and jig capacitances

Figure 1. Output Load

Figure 2. Output Load (for t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, tow and t_{CLZ})

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

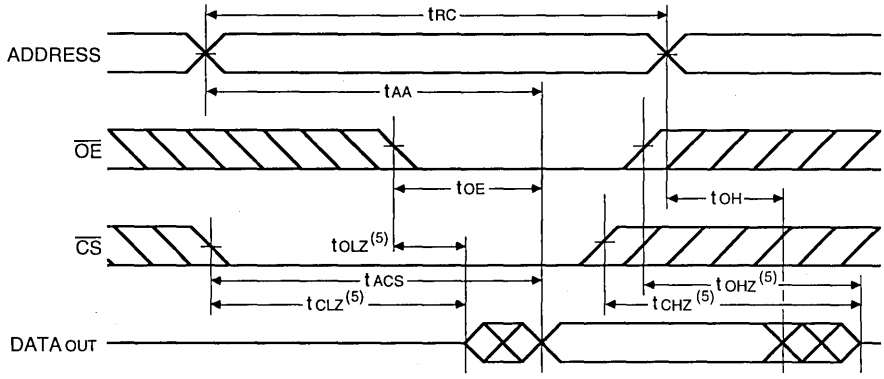
Symbol	Parameter	7M4048SxxCB						Unit
		-25[3]		-30		-35		
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	25	—	30	—	35	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	15	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	—	12	—	12	—	15	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
t_{CLZ}[1]	Chip Select to Output in Low-Z	5	—	5	—	5	—	ns
t_{CHZ}[1]	Chip Deselect to Output in High-Z	—	14	—	16	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{PU}[1]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
t_{PD}[1]	Chip Deselect to Power-Down Time	—	25	—	30	—	35	ns
Write Cycle								
t_{WC}	Write Cycle Time	25	—	30	—	35	—	ns
t_{WP}	Write Pulse Width	17	—	20	—	25	—	ns
t_{AS}[2]	Address Set-up Time	3	—	3	—	3	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End-of-Write	20	—	25	—	30	—	ns
t_{DW}	Data to Write Time Overlap	15	—	17	—	20	—	ns
t_{DH}[2]	Data Hold Time	0	—	0	—	0	—	ns
t_{WR}[2]	Write Recovery Time	0	—	0	—	0	—	ns
t_{WHZ}[1]	Write Enable to Output in High-Z	—	15	—	15	—	15	ns
t_{OW}[1]	Output Active from End-of-Write	3	—	3	—	3	—	ns

NOTES:
1. This parameter is guaranteed by design, but not tested.
2. t_{AS} = 0ns for $\overline{CS}$ controlled write cycles. t_{DH} , t_{WR} = 3ns for $\overline{CS}$ controlled write cycles.
3. Preliminary specifications only.

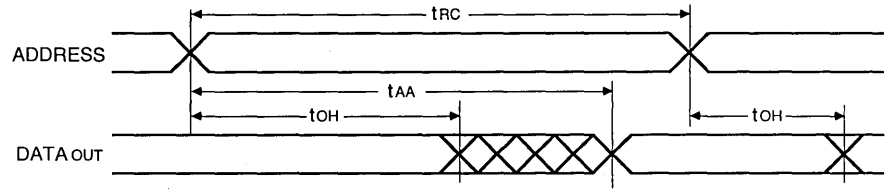
2822 tbl 09

7

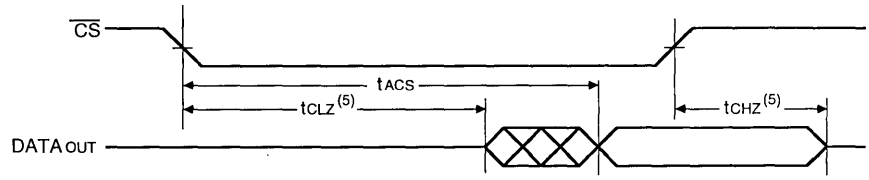
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

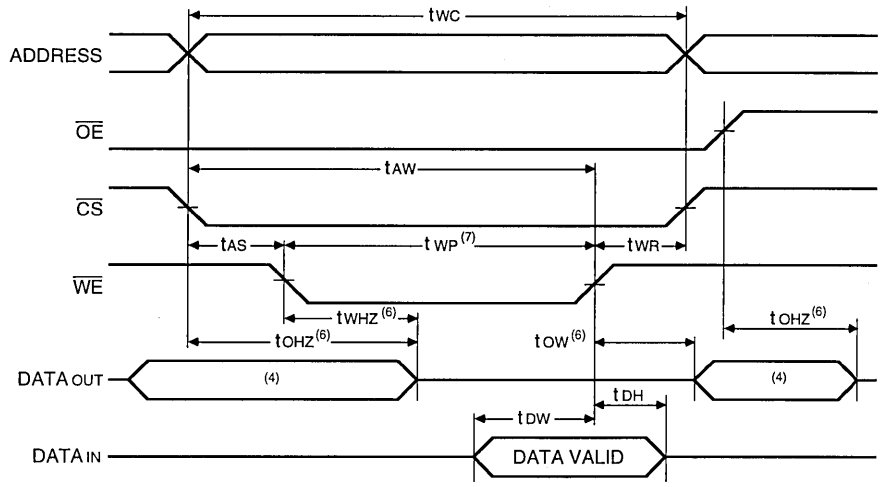


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

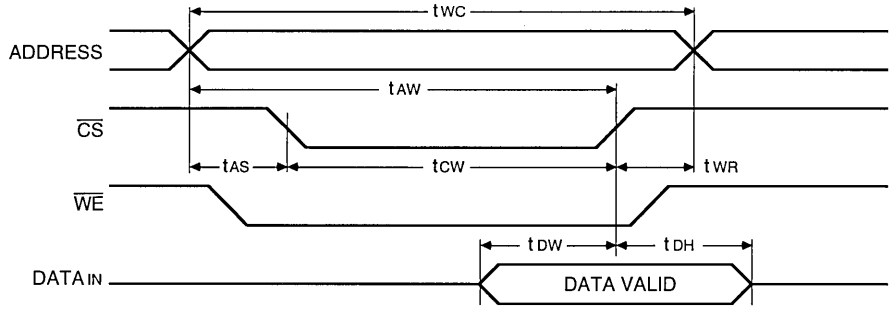


NOTES:
1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is guranateed by design, but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 7)

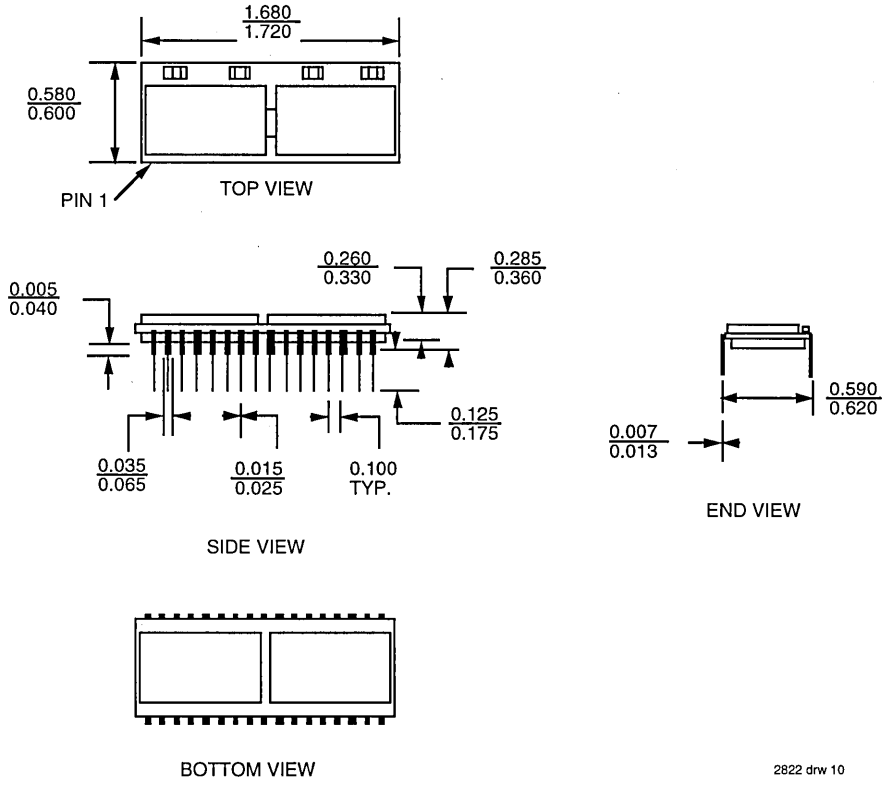


TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



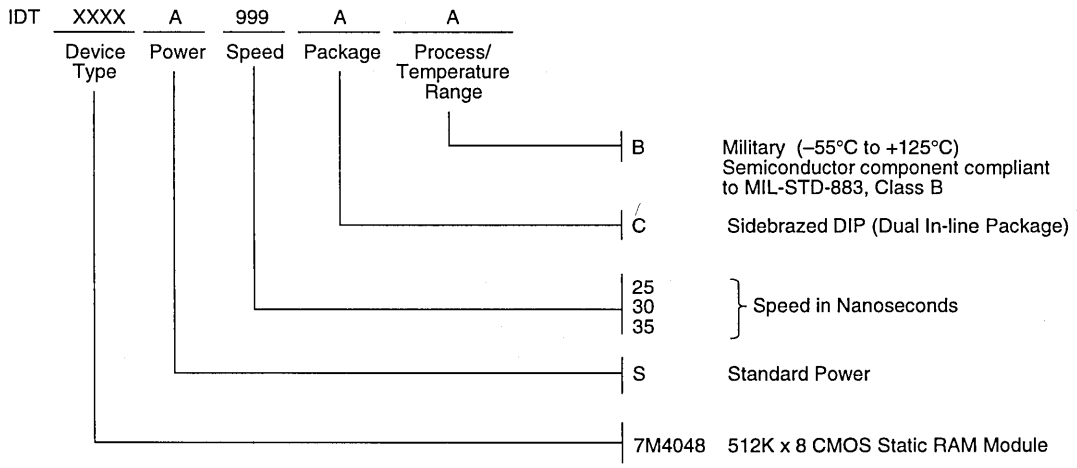
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig). This parameter is guaranteed by design, but not tested.
7. During a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

PACKAGE DIMENSIONS



2822 drw 10

ORDERING INFORMATION



2822 drw 11

One 800# does it all!

Dial 1-800-345-7015 to contact either your local sales office or corporate headquarters. Dial the 800 number above, then follow the instructions to be routed to your local sales office or corporate headquarters, and an operator will assist you in contacting technical support or customer service.

DOMESTIC SALES REPRESENTATIVES

ALABAMA

IDT
555 Sparkman Drive
Suite1238
Huntsville, AL 35816

ALASKA

Thorson Pacific, Inc.
14575 Bel-Red Road
Ste. 102
Bellevue, WA 98005

ARIZONA

Western High Tech Mktg.
9414 E. San Salvador
Suite 206
Scottsdale, AZ 85258

ARKANSAS

IDT
(S. Cen. Regional Office)
15851 Dallas Pkwy.,
Suite 1100
Dallas, TX 75248

CALIFORNIA

IDT
(Corporate Headquarters)
2975 Stender Way
P.O. Box 58015
Santa Clara, CA 95052

IDT
(Western Headquarters)
2975 Stender Way
Santa Clara, CA 95052

IDT
(SW Regional Office)
6 Jenner Drive
Suite 100
Irvine, CA 92718

IDT
(SW Regional Office)
17609 Ventura Blvd.
Suite 300
Encino, CA 91316

Quest-Rep
6494 Weathers Place
Suite 200
San Diego, CA 92121

CANADA (EASTERN)

Dynasty Components
110-1140 Morrison Drive
Ottawa, Ontario
Canada K2H 8S9

Dynasty Components
2339 Otami Trail
Mississauga, Ontario
Canada L5H 3N2

Dynasty Components
1870 Sources Boulevard
Suite 202
Pointe Claire, Quebec
Canada H9R 5N4

CANADA (WESTERN)

Thorson Co. Northwest
4170 Still Creek Drive
Ste. 200
Burnaby, British Columbia
Canada V5C 6C6

Dynasty Components
2 Mtn. River Estates
Ste 17, R.P. #2
P.O. Box 14
Calgary, Alberta
Canada T2P 2G5

Dynasty Components
1502-2041 Bellwood Ave
Burnaby, BC Canada
V5B 4V5

COLORADO

IDT
5299 DTC Blvd., Ste 350
Inglewood, CO 80111

Thorson Rocky Mountain
7108 "D" S. Alton Way
Suite A
Englewood, CO 80112

CONNECTICUT

SJ New England
10 Copper Ridge Circle
Guilford , CT 06437

SJ New England
15 Coventry Lane
Naugatuck, CT 06770

DELAWARE

IDT
(SE Regional Office)
Horn Point Harbor
105 Eastern Avenue
Suite 201
Annapolis, MD 21403

S-J Mid Atlantic, Inc.
131-D Gaither Drive
Mt. Laurel, NJ 08054

FLORIDA

IDT
(SE Headquarters)
1413 S. Patrick Drive
Suite10
Indian Harbor Beach, FL
32937

IDT
18167 U.S. 19 North
Suite 455
Clearwater, FL 34624

IDT
1500 N.W. 49th Street
Suite 500
Ft. Lauderdale, FL 33309

GEORGIA

IDT
(SE Regional Office)
18167 U.S. 19 North
Suite 455
Clearwater, FL 34624

HAWAII

IDT
(Western Headquarters)
2975 Stender Way
Santa Clara, CA 95052

IDAHO (NORTHERN)

Anderson Associates
270 S. Main Street
Suite 108
Bountiful, UT 84010

IDAHO (SOUTHERN)

Thorson Rocky Mountain
5505 South 900 East,
Ste. 140
Salt Lake City, UT 84117

ILLINOIS

IDT
(Central Regional Office)
1375 E. Woodfield Road
Suite 380
Schaumburg, IL 60173

TEQ Sales
820 Davis Road
Suite 304
Elgin, IL 60123

INDIANA

Arete Sales
2260 Lake Avenue
Suite 250
Ft. Wayne, IN 46805

Arete Sales
P.O. Box 24796
Indianapolis, IN 46224

IOWA

Rep Associates
4905 Lakeside Drive N.E.
Suite 107
Cedar Rapids, IA 52402

Rush and West Assoc.
4537 Brandy St.
Davenport, IA 52807

KANSAS

Rush & West Associates
333 E. Poplar Street
Olathe, KS 66061

KENTUCKY (EASTERN)

Norm Case Associates
21010 Center Ridge Road
Rocky River, OH 44116

KENTUCKY (WESTERN)

Arete Sales
P.O. Box 24796
Indianapolis, IN 46224

Norm Case Associates
303 Uhl Road
Melbourne, KY 41059

LOUISIANA

IDT
(S. Cen. Regional Office)
14285 Midway Road
Suite100
Dallas, TX 75244

MAINE

IDT
(NE Headquarters)
#2 Westboro Business Pk.
200 Friberg Pkwy,
Suite 4002
Westboro, MA 01581

MARYLAND

IDT
(SE Regional Office)
Horn Point Harbor
105 Eastern Avenue
Suite201
Annapolis, MD 21403

MASSACHUSETTS

IDT
(NE Headquarters)
#2 Westboro Business Pk.
200 Friberg PkWay,
Suite 4002
Westboro, MA 01581

SJ New England
11 Waterman Street
Worcester, MA 01603

MICHIGAN

Bergin-Milan Group, Ltd.
33900 W. Eight Mile Rd.
Suite 181
Farmington Hills, MI
48335

MINNESOTA

IDT
(N. Cen. Regional Office)
1650 W. 82nd Street
Suite 1040
Minneapolis, MN 55431

OHMS Technology Inc.
5780 Lincoln Drive
Suite 400
Edina, MN 55436

MISSISSIPPI

IDT
555 Sparkman Drive
Suite1238
Huntsville, AL 35816

MISSOURI

Rush & West Associates
2170 Mason Road
St. Louis, MO 63131

MONTANA

Thorson Rocky Mountain
7108 "D" S. Alton Way
Suite A
Englewood, CO 80112

NEBRASKA

Rush & West Associates
333 E. Poplar Street
Ste.C-3
Olathe, KS 66061

NEVADA (NORTHERN)

IDT
(Western Headquarters)
2975 Stender Way
Santa Clara, CA 95052

NEVADA (SOUTHERN)

Western High Tech Mktg.
9414 E. San Salvador,
Suite 206
Scottsdale, AZ 85258

NEW HAMPSHIRE

IDT
(NE Headquarters)
#2 Westboro Business Pk.
200 Friberg Pkwy,
Suite 4002
Westboro, MA 01581

NEW JERSEY

IDT
(SE Regional Office)
One Greentree Centre,
Suite 202
Marlton, NJ 08053

SJ Mid-Atlantic, Inc.
1331-D Gaither Drive
Mt. Laurel, NJ 08054

NEW JERSEY (NORTHERN)

SJ Associates
265 Sunrise HWay, #20
Rockville Centre, NY
11570

NEW MEXICO

Western High Tech Mktg.
9414 E. San Salvador
Suite 206
Scottsdale, AZ 85258

NEW YORK

IDT
(NE Regional Office)
1160 Pittsford Victor Rd.
Bldg. E
Pittsford, NY 14534

Quality Components
3343 Harlem Road
Buffalo, NY 14225

Quality Components
116 E. Fayette Street
Manlius, NY 13104

Quality Components
451 Brookwood Dr.
Webster, NY 14622

Quality Components
RD #2, Box 31E
Glassfactory Road
Holland Patent, NY 13354

SJ Associates
265 Sunrise HWay, #20
Rockville Centre, NY
11570

NORTH CAROLINA

IDT
213 Townsend Ct.
Cary, NC 27511

Tingen Technical Sales
304A W. Millbrook Road
Raleigh, NC 27609

NORTH DAKOTA

OHMS Technology Inc.
5780 Lincoln Drive
Suite 400
Edina, MN 55436

OHIO

Norm Case Associates
21010 Center Ridge Road
Rocky River, OH 44116

OKLAHOMA

IDT
(S. Cen. Regional Office)
14285 Midway Road
Suite 100
Dallas, TX 75244

OREGON

IDT
(NW RegionalOffice)
15455 NW Greenbriar PkWay
Suite 210
Beaverton, OR 97006

Thorson Pacific, Inc.
9600 S.W. Oak Street
Suite 320
Portland, OR 97223

PENNSYLVANIA (WESTERN)

Norm Case Associates
21010 Center Ridge Road
Rocky River, OH 44116

PENNSYLVANIA (EASTERN)

S-J Mid-Atlantic
131-D Gaither Drive
Mt. Laurel, NJ 08054

RHODE ISLAND

IDT
(NE Headquarters)
#2 Westboro Business Pk.
200 Friberg PkWay,
Suite 4002
Westboro, MA 01581

SOUTH CAROLINA

Tingen Technical Sales
304A W. Millbrook Road
Raleigh, NC 27609

SOUTH DAKOTA

OHMS Technology Inc.
5780 Lincoln Drive
Suite 400
Edina, MN 55436

TENNESSEE

IDT
555 Sparkman Drive
Suite 1200-D
Huntsville, AL 35816

TEXAS

IDT
(S. Cen. Regional Office)
14285 Midway Road
Suite 100
Dallas, TX 75244

IDT
6034 W. Courtyard Dr.
Ste. 305-60
Austin, TX 78730

UTAH

Anderson Associates
270 S. Main Street
Suite 108
Bountiful, UT 84010

Thorson Rocky Mountain
1831 E. Fort Union Blvd.
Suite 103
Salt Lake City, UT 84121

VERMONT

IDT (NE Headquarters)
#2 Westboro Business Pk.
200 Friberg Pkwy,
Suite 4002
Westboro, MA 01581

VIRGINIA

IDT (SE Regional Office)
Horn Point Harbor
105 Eastern Avenue
Suite201
Annapolis, MD 21403

WASHINGTON

Thorson Pacific, Inc.
12340 N.E. 8th St., #201
Bellevue, WA 98005

WEST VIRGINIA

Norm Case Associates
21010 Center Ridge Road
Rocky River, OH 44116

WISCONSIN

TEQ Sales
20720 W. Watertown Rd.
Suite 201
Waukesha, WI 53186

WYOMING

Thorson Rocky Mountain
7108 "D" S. Alton Way
Suite A
Englewood, CO 80112

AUTHORIZED DISTRIBUTORS (U.S. and Canada)

Future Electronics | **Hamilton Hallmark** | **Insight Electronics** | **Port Electronics** | **WYLE**

Contact your local office.

INTERNATIONAL SALES REPRESENTATIVES

AFRICA

Prime Source (PTY) Ltd.
Oraange Grove, So. Africa
Tel.: 2711-444-7237

AUSTRALIA

GEC Electronics Division
Rydalmere,NSW,
Australia
Tel.: 612-638-1999/1888

GEC Electronics Division
Adelaide, SA, Australia
Tel.: 618-223-1222

GEC Electronics Division
Burwood, Australia
Tel.: 613-245-3230

GEC Electronics Division
Perth, WA, Australia
Tel.: 613-381-4040

GEC Electronics Division
Bowen Hills, Australia
Tel.: 619-252-5801

AUSTRIA

Elbatex GmbH
Vienna, Austria
Tel.: 43-186-32110

BELGIUM

ACAL N.V.
Betea Components
Zaventem, Belgium
Tel.: 322-725-1080

CHINA

Lestina International, Ltd.
Beijing, China
Tel.: 86-1-849-9430

Lestina International, Ltd.
Guang Zhou
Tel.: 86-20-885-0613

DENMARK

Exatec A/S
Skovlunde, Denmark
Tel.: 45-44-927-000

AVNET Nortec A/S
Herlev, Denmark
Tel.: 45-42-842-000

FINLAND

AVNET Nortec OY
Helsinki, Finland
Tel.: 358-0670-277

FRANCE

IDT
(So. Europe Reg. Office)
15 Rue du Buisson aux Fraises
91300 Massy, France
Tel.: 33-1-69-30-89-00

A2M
Brignolles, France
Tel.: 33-1-94-59-2293

A2M
Bron, France
Tel.: 33-1-72-37-0414

A2M
Buc, France
Tel.: 33-1-39-56-8181

A2M
Cesson-Sevigne, France
Tel.: 33-1-99-63-3232

A2M
Le Chesnay Cedex, France
Tel.: 33-1-39-54-9113

A2M
Merignac, France
Tel.: 33-1-56-34-1097

COMPRESS
Rungis Cedex, France
Tel.: 331-4687-8020

AVNET EMG
Cesson-Sevigne, France
Tel.: 33-99-83-9898

AVNET EMG
Chantillon, France
Tel.: 33-149-652-2750

AVNET EMG
Rognes, France
Tel.: 33-42-50-1805

AVNET EMG
Saint-Etienne, France
Tel.: 33-77-79-7970

AVNET EMG
Schwerwiller, France
Tel.: 33-88-82-5514

GERMANY

IDT
(Cen. Europe Reg. Office)
GottfriedVonCramm-Str.1
8056 Neufahrn, Germany
Tel.: 49-8165-5024

AVNET E2000
Munich, Germany
Tel.: 089-45110-01

AVNET E2000
Berlin, Germany
Tel.: 030-2110761/0764

AVNET E2000
Dusseldorf, Germany
Tel.: 0211-92003-0

AVNET E2000
Frankfurt, Germany
Tel.: 069-973804-0

AVNET E2000
Hamburg, Germany
Tel.: 040-645570-0

AVNET E2000
Nurnberg, Germany
Tel.: 0911-995161-0

AVNET E2000
Gerlingen, Germany
Tel.: 07156-356-0

Jermyn GmbH
Limburg, Germany
Tel.: 49-6431/508-0

Jermyn GmbH
Berlin, Germany
Tel.: 49-30/2142056

Jermyn GmbH
Dusseldorf, Germany
Tel.: 49-211/25001-0

Jermyn GmbH
Heimstetten, Germany
49-89/909903-0

Jermyn GmbH
Herrenberg, Germany
Tel.: 49-7032/203-01

Jermyn GmbH
Pinneberg, Germany
Tel.: 49-40/5282041

Jermyn GmbH
Nornberg, Germany
Tel.: 49-911425095

Jermyn GmbH
Hermsdorf, Germany
Tel.: 49-3660142374

Scantec GmbH
Planegg, Gerrnany
Tel.: 49-898598021

Scantec GmbH
Kirchheim, Germany
Tel.: 49-702183094

Scantec GmbH
Ruckersdorf, Germany
Tel.: 49-91-157-9529

Topas Electronic GmbH
Hannover, Germany
Tel.: 49-51-113-1217

Topas Electronic GmbH
Quickborn, Germany
Tel.: 49-4106-73097

GREECE

Digital Electronics
Athens, Greece
Tel.: 30-1-533-5754

HONG KONG

IDT ASIA LTD.
Unit 1003
China Hong Kong City
Tower 6, 33 Canton Road
Tsimshatsui, Hong Kong
Tel.: 852-736-0122

Lestina International Ltd.
Kowloon, Hong Kong
Tel.: 852-735-1736

INDIA

Techno Trends
San José, CA
Tel.: (408) 294-2833

Sritech Information
Technology, Inc
Javanagar, Bangalore
0812-643608

IRELAND

Bloomer Electronics
Craigavon, County
Armagh, N. Ireland
Tel: 762-3398181

ISRAEL

Active Technologies
New Hyde Park, NY
Tel.: (516) 488-1226

Vectronics, Ltd.
Herzlia, Israel
Tel.: 972-9-55-60-70

ITALY

IDT (IDT Italia S.r.L.)
Central Direzionale
Colleoni
Palazzo Astolabia
Via Cardano 2
20041 Agrate Brianza,
Milan, Italy
Tel.: 39-39-68-99-987

AVNET De Mico
Cassina De Pecchi (MI)
Tel.: 02-95-34-36-00

AVNET De Mico
Torino, Italy
Tel.: 011-31-81-481/500

AVNET De Mico
Rome, Italy
Tel.: 06-33-32-283/284

AVNET DeMico
Bologna, Italy
Tel.: 051-55-56-14/00-64

AVNET De Mico
Rubano (Padova), Italy
Tel.: 049-63-35-55/36-00

AVNET De Mico
Campi Briseno, Italy
Tel.: 055-89-41-05/15

Lasi Electronica
Bologna, Italy
Tel.: 3951-353815/374556

Lasi Electronica
Firenze, Italy
Tel.: 3955-582627

Lasi Electronica
Milano, Italy
Tel.: 39-266-1431

Lasi Electronica
Roma, Italy
Tel.: 396-5405301/
5409614

Lasi Electronica
Torino, Italy
Tel.: 3911-328588/359277

JAPAN

IDT KK
(Japan Headquarters)
Sumitomo Fudosan
Sanbacho Bldg.
6-26 Sanbacho
Chiyoda-Ku
Tokyo 102, Japan
Tel.: 813-3221-9821

Dia Semicon Systems
Yokohama, Japan
Tel.: 045-476-7410

Kanematsu Semiconductor Corp.
Tokyo, Japan
Tel.: 813-3551-7791

Tachibana Tectron Co. Ltd
Tokyo, Japan
Tel.: 813-3793-1171

KOREA

Uniquest Korea
Seoul, Korea
Tel.: 822-562-8805

Uniquest Corporation
San José, CA
Tel.: 408-432-8805

NETHERLANDS

ACAL Auriema
Eindhoven, Netherlands
Tel.: 040-502-602

NEW ZEALAND

GEC Electronics Division
Auckland, New Zealand
Tel.: 649-526-0107

NORWAY

AVNET Nortec A/S
Hvalstad, Norway
Tel.: 47-66-84-62-10

PORTUGAL

Anatronic S.A.
Odivelas, Portugal
Tel.: 351-19376267/6287

SINGAPORE/ FAR EAST

Serial System PTE LTD
Singapore
Tel.: 65-280-0200

SPAIN

Anatronic, S.A.
Madrid, Spain
Tel.: 34-1-542-5566

Anatronic, S.A.
Barcelona, Spain
Tel.: 34-3-458-1906/7

SWEDEN

IDT (IDT AB)
Veddestavagen 13
S-175 62 Jarfalla, Sweden
Tel. :468-761-1130

AVNET Nortec AB
Vinthundsvagen, Sweden
Tel.: 46-8629-1400

AVNET Nortec AB
Solna, Sweden
Tel.: 46-8629-1400

AVNET Nortec OY
Helsinki, Sweden
Tel.: 358-0613-181

SWITZERLAND

Eljapex
Wettingen, Switzerland
Tel.: 011-41-56275-777

TAIWAN

Johnson Trading &
Engineering Co.
Taipei, Taiwan ROC
Tel.: 886-273-31211

Synnex Technology
International Corp.
Taipei, Taiwan ROC
Tel.: 886-2-506-3320

World Peace Industrial
Co., Ltd.
Nankang, Taipei,
Taiwan ROC
Tel: 886-2-788-5200

UNITED KINGDOM

IDT
(European Headquarters/
No. Europe Reg. Office)
Prime House
Barnett Wood Lane
Surrey, UK KT227DG
Tel.: 44-372-363-339/734

Avnet Access, Ltd.
Letchworth, Herfordshire,
UK
Tel.: 0462-480888

MicroCall, Ltd.
Thame Oxon, UK
Tel.: 44-844-261-939

M.M.D. Ltd
Reading, Berkshire
Tel.: 44-734-313232

Integrated
Device Technology, Inc.

2975 Stender Way
Santa Clara, CA 95054-3090
(800) 345-7015
FAX: (408) 492-8674

DBK-SMP-00065